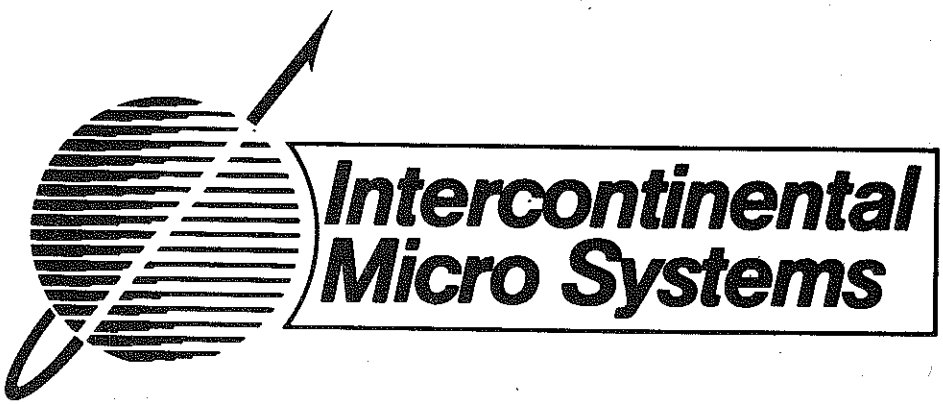
CPS - BMX

S-100 BUS
SINGLE BOARD SLAVE PROCESSOR



4015 Leaverton Court • Anaheim, California 92807 • (714) 630-0964 • Telex: 678401 - TAB-IRIN

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**** INTRODUCTION ****

The Intercontinental Micro Systems Corp. (ICM) CPS-BMX single board slave processor is a Z80A (tm) or Z80B (tm) based computer complying with the IEEE 696.1/D2 S100 Bus specification. This computer incorporates all features necessary for a complete stand alone system, each to be dedicated to a user in a distributed processor system utilizing operating systems such as TurboDOS (tm) and CP/NET (tm).

The CPS-BMX processors together with an S100 Bus master (host) like the ICM CPZ-4800X SBCP constitute a high performance, high throughput network which can be integrated into most S100 Bus mainframes. The master/slave communications take place over the S100 Bus via slave/host bidirectional memory transfers under control of the host processor. This memory mapping technique thoroughly enhances data throughput and reduces overhead hardware resulting in a high performance, low cost slave processor, making distributed processing comparable to mainframe performance at a fraction of the cost.

FEATURES
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* IEEE 696.1/D2 S100 Bus compliance.
* Z80A 4 mhz (CPS-B4X) or Z80B 6 mhz (CPS-B6X) operation.
* Compatible with CPZ 4800X SBCP, any Z80A based CPU with extended address compatibility or 16 bit based CPU's complying with IEEE 696.1/D2 Bus specification.
* Two synchronous (CPS-BMS) or asynchronous (CPS-BMA) serial I/O ports.
* Two parallel I/O ports; eight data bits and two handshake lines per port.
* TurboDOS and CP/NET compatible.
* 128 Kbytes (2 Bank Switched 64K banks) of onboard dynamic RAM.
* Master/Slave memory-to-memory transfers under DMA control at 571 Kbytes/sec transfer rate when used with CPZ-4800X SBCP.
* Master confiscation of slave memory for diagnostic purposes.
* Software selectable baud rates.
* Usable as an intelligent I/O processor in single user systems.
* Usable as a 64 Kbyte Bank Switched RAM (2-64k Banks) in either single-user or multi-user systems.

CPS SLAVE PROCESSORS

The ICM CPS-MX 64K SLAVE AND CPS-BMX 128K SLAVE computers are very fast, reliable slave processors compatible with ICM'S S-100 BUS master computer. Used in combination with the ICM CPZ-4800X MASTER SBC, the CPS offers a high throughput, high performance capability unmatched by any other master/slave combination available in the S-100 market today.

The CPS is a Z80 based processor using either the Z80A, 4MHZ or Z80B, 6MHZ architecture. It is in full compliance with the IEEE 696.1/D2 S-100 bus standard. This slave processor can be used with any S-100 Z80A SBC with extended address capability. It can also be used as an intelligent I/O processor in a single user system or in a 16 bit architecture .

The CPS is offered with 64K RAM and 128K RAM options. The 128K board has been designed specifically for TURBODOS 1.3 applications. TurboDOS 1.3 supports 128K bank-switched memory on Z80 computers, two banks of 64K RAM. One bank holds the operating system and a large pool of disk buffers. Almost all of the other bank (except the topmost 1K) is available of user programs. This 63K transient program area (TPA) gives applications significantly more space the on previous TurboDOS versions. Under TurboDOS 1.3, processing of console I/O functions is now more that twice as fast as before. This results in greatly improved performance with console-intensive applications such as WordStar. The 64K board is compatible with CP/NET and TurboDOS 1.22 & 1.3.

Using the CPS in a DIRECT MEMORY ACCESS (DMA) mode, as available with the CPZ master, will result in memory transfer that is 300% faster than the typical I/O mapped architecture. DMA relieves the master and slave CPU's of memory allocation code, bypassing them completely to do memory transfers. DMA also allows memory transfer in 128 byte blocks rather than the standard byte by byte transfer method.

The CPS can be used as a MEMORY MAPPED SLAVE using the MEMORY MANAGEMENT UNIT (MMU) available on the ICM CPZ MASTER. A memory mapped slave is at least twice as fast as a standard I/O mapped slave. Memory mapping also eliminates expensive on-board hardware such as EPROM and FIFO buffers. Memory mapping allows the master to download the Operating System and Application Software directly to the slave's memory eliminating the time and protocol code usually required by both the master's and slave's CPU's.

OPERATING SYSTEM COMPATIBILITY: The CPS has been specifically designed to operate under a TurboDOS OS. TurboDOS is compatible with virtually all off-the-shelf CP/M APPLICATION SOFTWARE. Since CP/M has been the standard 8-bit Operating System for a number of years, there are literally THOUSANDS of Application Software Packages readily available. TurboDOS will soon be MS-DOS/PC-DOS compatible, opening up the 16 bit world to as well. Save your 8 bit library and grow into the 16 bit arena. CP/NET compatible also.

MASTER/SLAVE TURBODOS NETWORK. 1 MASTER (CPZ 4800X) and up to 16 SLAVES (CPS) on one S-100 bus. Up to 256 masters can be networked together to build a 4000 user system with an ARCNET S-100 board. Each slave CPU acts independently of the master, resulting in a DEDICATED PROCESSOR FOR EACH USER. This type network is inherently faster than a SHARED PROCESSOR type network such as MP/M or UNIX because each user can work independently of the other users on the network. TurboDOS is also quite user friendly, unlike the scientific oriented UNIX. A TurboDOS network is very cost effective because all users can share common, costly peripherals. Approximately 1/3 the cost of networking personal computers under OMNINET. 1/5 the cost of an ETHERNET PC network.

8 BIT & 16 BIT NETWORKS: 8 bit & 16 bit processors can be networked together as soon as our 16 bit slave is available.

In short, the CPS-MX offers the best PRICE/PERFORMANCE package on the market. When networked with the CPZ-4800X, it offers unmatched speed and reliability.

OTHER STANDARD FEATURES:

-2 SERIAL I/O PORTS: Synchronous or Asynchronous. Can interface with Micro, Mini, or Mainframe level peripherals.

-2 PARALLEL I/O PORTS: Programmable I/O mode. Two 8-bit data lines and two handshake lines allows 2-way communication between CPU and peripheral.

-DISCRETE REFRESH CIRCUITRY: Relieves the CPU of having to refresh the memory. Putting the CPU into a HALT state will not result in memory loss.

-SOFTWARE SELECTABLE BAUD RATES: Allows very flexible peripheral interfacing. Eliminates complicated hardware jumpering or switching to change baud rates. Up to 800K BAUD in synchronous mode, 50K BAUD in asynchronous mode.

-INTERRUPT control of slave to master requests enhances master to slave communication. The master responds immediately to the slave's request for service.

-MASTER'S CONFISCATION of slave memory to download programs into slave's memory allows the slave to process independently of master, thus allowing the user to process at the slave's clock rate. Confiscation also allows the master to perform diagnostics on the slave board, or allows the master to use the slave as an expanded 64K RAM memory board.

WHAT IS A TURBODOS SYSTEM?

TURBODOS is an operating system that allows multiple processors to be networked together to support multiple users in a MASTER/SLAVE configuration. One of the processors, the Master Processor, acts as the program director for the network. The other processors, Slave Processors, service one user each, and can operate independently of the Master processor. When Turbodos is used on the S-100 BUS, up to 16 users can be networked together with one Master, in one chassis.

MASTER-TO-MASTER networking is also possible using an ETHERNET control card on the S-100 bus. Current technology will allow us to network 16 masters together, resulting in a very efficient, 256 USER network, with all the advantages of TURBODOS.

There are many advantages to a multi-user/multi-processor network:

1. Each user has a dedicated processor to work with. The master will transfer the operating system and the file down to the slave processor being used, and the user can then process independent of any other user on the system. Thus there is no "sharing" of a single processor between users, as with many other networks.

2. Since all processors and peripheral controllers are normally mounted on the S-100 Bus, all data transfers are parallel across the bus, rather than serially as with a network of personal computers. Thus, data transfers can be accomplished at a much faster speed than with a serial transfer protocol.

3. All users can share common peripherals, thus lowering the cost of a multi-user system. The common peripherals are usually connected to the Master processor. Although the PC network can put a printer on each PC, their users CAN NOT share those printers. On a Turbodos network we can put printers on the master, as well as each slave, and all users can share all printers.

4. All boards: Master, Slave, Memory Boards, and Peripheral Controllers are contained in a single chassis, therefore each user only needs a simple terminal. Again, this is less expensive than a complete personal computer at each work station.

5. The system is very versatile because each slave also has 2 serial and 2 parallel ports to allow connecting to dedicated peripherals if you don't want all users to share the common peripherals.

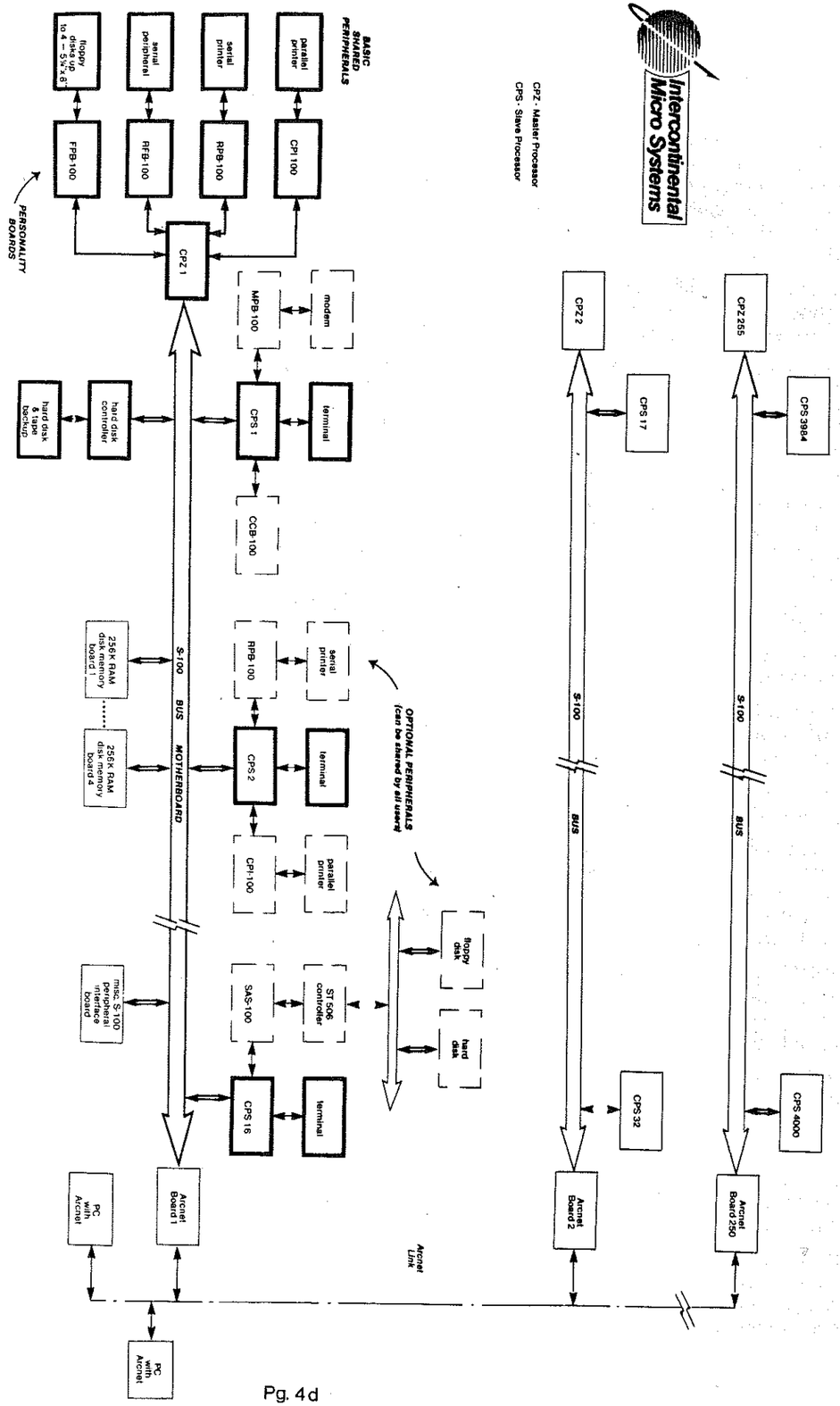
6. Most personal computer networks are designed to operate effectively at up to 10 users. More than 10 users will cause significant degradation in the network. A Turbodos network can accomodate 16 users per Master very efficiently. Current technology will allow up to 256 Masters to be networked, resulting in a very sophisticated 4000 user system. The networking of masters is accomplished through ARCNET S-100 boards.

7. TURBODOS multi-user systems have become as powerful as MINI-COMPUTERS, and yet are much less expensive. This type of network is a very cost-effective approach to the typical "4 user" system. The 4 user system can be expanded to additional users more quickly and at a much lower price than adding more PC's to a network.

8. The TURBODOS network allows all users to share the same files, and yet provides for record and file locking to prevent two or more users from modifying the same file at the same time. PC NETWORKS DO NOT YET FEATURE RECORD LOCKING.

9. ICM's MASTER/SLAVE processors are the most sophisticated, cost effective SINGLE BOARD COMPUTERS in the TURBODOS marketplace. They offer more processing power, faster throughput and excellent reliability. The features and advantages of using ICM's processors are discussed in the attached brochures.

10. FINALLY, the ICM MASTER/SLAVE Turbodos network was originally designed to operate as a network. The PC was not designed to operate in a network environment. Therefore, it is only logical that your clients will be sacrificing some of the advantages of a 16 bit PC when they begin networking them together.



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PERFORMANCE SPECIFICATIONS

Processor
  Clock Rate
    CPS-B4X.....4 MHz
    CPS-B6X.....6 MHz
  Type
    CPS-B4X.....Z80A
    CPS-B6X.....Z80B

Bus Interface.....IEEE 696.1/D2 S100
Status, control, data and address. Slave I/O port address switch selectable for address range from 00h to FFh. Slave memory address switch selectable for address range from 010000h to FFFFFFh.

I/O CHANNELS:
Serial I/O channels (two ports)
CPS-B4A (asynchronous).....up to 800 Kbaud
CPS-B6A (asynchronous).....up to 1.2 Mbaud
CPS-B4S (synchronous).....up to 800 Kbaud
CPS-B6S (synchronous).....up to 1.2 Mbaud

I/O Interface.....through personality boards such as Dumb terminal, RS232 modem, and RS422 interface boards.

Parallel I/O channels (two ports)
Data rate.....up to 300 Kbytes/sec.
Interface signals ..... eight data lines plus two handshaking lines per port.
I/O interface.....through personality boards such as Centronics Printer, Priam and ST506 intelligent hard disk interface boards.

128 KBYTE DYNAMIC RAM:
Wait states.....none required
Direct memory transfers.....to/from CPZ-4800X SBCP
Data transfer rate (non-DMA).....190 Kbytes/sec
Data transfer rate (DMA).....571 Kbytes/sec

Arranged as two 64 Kbyte banks, switchable under software control, permitting typical TPA of 64,253 bytes in user bank.

Memory address.....switch selectable in the 64 Kbyte boundries for a total of 256 Kbyte pages.

STATUS PORT BIT ASSIGNMENTS (as read by master):

```
D7  D6  D5  D4  D3  D2  D1  D0
!   !   !   !   !   !   !   !
!   !   !   !   !   !   !   +-----unused
!   !   !   !   !   !   +---------unused
!   !   !   !   !   +-------------unused
!   !   !   !   +---------------------unused
!   !   !   +-----------------------slave soft request for servi
!   !   +-------------------------slave interrupt request
!   +---------------------------slave in-service status
+-----------------------------slave hard request for servi
```

COMMAND PORT DATA BIT ASSIGNMENTS (as executed by master):

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	-----master clear slave request/r
0	0	0	0	0	0	0	1	-----master confiscate slave's me
0	0	0	0	0	0	1	0	-----master clear slave reset
0	0	0	0	0	0	1	1	-----master release slave to run
1	0	0	0	0	0	0	0	-----master reset slave
0	1	0	0	0	0	0	0	-----master request to slave
0	0	1	0	0	0	0	0	-----master interrupt to slave

COMMAND PORT ADDRESS BIT ASSIGNMENTS (as executed by slave):

A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	-----00H SIO Chan A Data
0	0	0	0	0	0	0	1	-----01H SIO Chan A Cmd/Status
0	0	0	0	0	0	1	0	-----02H SIO Chan B Data
0	0	0	0	0	0	1	1	-----03H SIO Chan B Cmd/Status
0	0	0	0	0	1	0	0	-----04H PIO Chan A Base
0	0	0	0	0	1	1	0	-----06H PIO Chan B Base
0	0	0	0	1	0	0	0	-----08H CTC0 Chan 0
0	0	0	0	1	0	0	1	-----09H CTC0 Chan 1
0	0	0	0	1	0	1	0	-----0AH CTC0 Chan 2
0	0	0	0	1	0	1	1	-----0BH CTC0 Chan 3
0	0	0	1	0	0	0	0	-----10H CTC1 Chan 0
0	0	0	1	0	0	0	1	-----11H CTC1 Chan 1
0	0	0	1	0	0	1	0	-----12H CTC1 Chan 2
0	0	0	1	0	0	1	1	-----13H CTC1 Chan 3
0	0	0	1	0	1	0	0	-----14H BANK SWITCH Bank 0
0	0	0	1	0	1	0	1	-----15H BANK SWITCH Bank 1

****** FUNCTIONAL DESCRIPTION ******

The CPS-BMX is functionally partitioned into the following major groups:

```
--CPU/128 Kbyte dynamic RAM/control
        --128 Kbyte Ram
        --CPU/S100 Address Multiplexer
        --Address Multiplexer
        --RAS/CAS Generator
        --REFRESH Generator/Control

--Slave Processor Control Logic
        --Slave Processor Chip Select/Command Decoder
        --Slave Request Logic
                --Hard Request Logic
                --Soft Request Logic
                --Interrupt Request Logic

--Slave Clock Generator

--Reset Generator

--Input/Output Structure
        --Serial I/O Port Control
        --Parallel I/O Port Control

--S100 Bus Interface
        --Status/Control Signals Receivers
        --Data Receivers/Data Transmitters
```

Each group is described below to give the user a clear understanding of the hardware and software setup option. Prior to describing each group, a "thumbnail sketch" of the overall function of the CPS-BMX is first described.

(1) Master/slave Action at Reset Time

At power-up, master reset or slave reset time, a slave service request flag (hard request) is raised and the slave CPU is tri-stated. During this time, the slave's 64 Kbyte RAM (bank 0) is addressable by the S100 Bus address lines A0-A23. Address lines A0-A15 address the 64 Kbyte RAM and A16-A23 select the page in which the 64 Kbyte section lies in the master's address range. The request flag in this case is referred to as the slave's "hard request" flag in that the slave CPU is immediately tri-stated and the memory is refreshed by the master. The master commences to poll slave request flags via I/O port status read commands. Upon determining that a slave requires service, the master transfers control of the slave memory to the master. The master can then "map" the slave memory into its address space. The master may then down-load the slave's operating system into the slave's memory. At the completion of this transfer, the master issues an I/O port reset command to the slave followed by a command which causes the slave's tri-state condition to be released. The slave then commences to execute program intructions deposited by the master resulting in execution of the slave's operating system. Thus, a "cold-boot" operation is executed.

(2) Master/slave Action during File Transfers

This operation is quite similar to the action described above. When a slave requires the transfer of files to or from the master, a "soft-request" flag is raised. This means that a flag is raised but without the slave's CPU going into tri-state immediately as in paragraph (1) above. The master, upon determining that slave service is required, will then issue a service acknowledge command as previously described. It is only then that the slave is tri-stated and that the slave's memory is relinquished to the master as previously described. The slave's program execution is suspended for the duration of the master's data transfer process. Files are transferred as required and at the completion, the master issues a release command so that the slave is reactivated.

The hardware is partitioned into two major groups: (1) the slave kernel and (2) the I/O structure. The I/O simply consists of the serial I/O and parallel I/O controllers and associated logic. The slave kernel consists of the slave CPU, 128 Kbytes of slave memory, slave CPU address/S100 Bus address multiplexer and the logic associated in asserting the slave CPU tri-state condition.

CPU/128 Kbyte Dynamic RAM/Control

The CPS-BMX is a Z80 based CPU which can be either a 4 mhz (Z80A) or 6 mhz (Z80B) CPU. 128 Kbytes of memory organized as two 64 Kbyte banks are implemented in such a manner that memory is accessed by either the slave CPU or by the master CPU via the S100 Bus address and control lines. Control logic is provided to issue a service request flag, switch memory control from the slave to the master and back, refresh the slave memory appropriately, switch the address lines from the slave to the S100 Bus and back and provide RAS/CAS control to the memory.

128 Kbytes RAM

The RAM consists of sixteen 64 Kbyte by one bit memory chips. The RAM is of 150ns access variety to provide reliable, non-wait state memory operation. It is configured for early-write mode to simplify internal buffering requirements. Address signals are sourced from either the slave CPU or the master CPU via the S100 Bus address lines. Data signals are transmitted in the slave's internal data bus or to/from the host processor via buffers connected to the S100 Data Bus lines.

CPU/S100 Address Multiplexer

Four Octal buffers are provided to switch address lines A0 through A15 to the slave memory from either the slave CPU or the master CPU via the S100 Bus address lines. Switching action is provided by the slave's CPU DMA acknowledge output line 'BUSAK'. When the slave CPU is successfully tri-stated, BUSAK is active and in turn, enables the S100 Bus address lines to the slave's address multiplexer.

Address Multiplexer

The slaves address multiplexer consists of two Octal buffers which multiplex address lines A0 through A15 to eight address lines which are input to the two 64 Kbyte bank memory address lines via 33 ohm series resistors. The series resistors limit voltage undershoot to less than 1.0 vdc to provide long term protection to the RAM chips.

RAS/CAS Generator

The slave's memory row address and column address strobe signals (RAS and CAS respectively) are generated by the slave CPU memory read or write cycle or by the master CPU memory read or write cycle. These signals are input to a delay line to generate precise timing signals (RAS and CAS) as required by the RAM devices. The delay line also generates a signal to switch the address multiplexer described in the previous paragraph. This section of logic also generates the write timing signal sourced by the slave CPU memory write line or the master CPU memory write line via the S100 Bus. RAS, CAS and write signals are input to the RAM via series 33 ohm resistors to provide long term damage protection to the RAM. The master CPU memory cycles are enabled by the Extended Address select logic described below.

Refresh Generator/Control

Logic is provided to generate refresh to the slave memory. Either the master or the slave generates the refresh signal appropriately. The RAM is refreshed from the slave when the slave CPU is active or from the master when the master CPU has taken control of the slave RAM. The logic is structured to generate refresh properly during the switching action from slave CPU control to master CPU control and back. If the slave has entered a hard request state, the slave memory is refreshed by the master until the master determines that a request is present and the master acknowledges the request.

Extended Address Select Logic

When the slave asserts a service request and is successfully acknowledged by the master, a comparator is enabled which compares the master's extended address lines A16(m) through A22(m) against an eight position jumper referred to as the EXTENDED ADDRESS SELECT jumper. If the master executes a memory transfer to the bus, the acknowledged slave whose comparator is enabled will cause a memory cycle to occur in the slave.

I/O Port Address Select Logic

The I/O Port Address Select Logic consists of the I/O Port Address Decoder and the Host Processor Status/Command Decoder//Logic.

I/O Port Address Decoder

The I/O Port Address Decoder consists of an eight bit comparator which compares the master's least significant address bits A0(m) through A7(m) against an eight position jumper referred to as the I/O PORT SELECT jumper. If the master executes an I/O cycles transfer to the bus, the slave whose address decoder compares, will respond to either a master's command or to the master's request for the slave's status.

Host Processor Status/Command Decoder//Logic

The master may issue one of eight commands to the slave, these commands are listed as follows:

** Clear Slave Request (00H)
The slave may issue two types of requests to the master. These are: (1) SOFT-REQUEST and (2) INTERRUPT REQUEST. The master is required to acknowledge the requests which is done through an I/O command, CLEAR SLAVE REQUEST.

** Confiscate Slave's Memory (01H)
The master may asynchronously issue a memory confiscation command and request the slave's central processor to tri-state itself. The slave will respond by setting the "request" status bit. The master should then poll the "service" status bit until it is set. This indicates that the slave's CPU has successfully been tri-stated and that the inputs to the slave RAM address multiplexer are transferred from the slave to the master. This completes the transfer of control over the slave's RAM from the slave processor to the master's processor. The master may transfer the control back to the slave by issuing a "Release Slave to Run" command (03H).

The master may maintain control indefinitely thereby treating the slave as a 64Kbyte RAM appearing in the master's extended address space.

** Clear Reset Latch (02H)
The master clears slave's reset latch. This command is normally issued only after the Reset Slave (80H) command.

** Release Slave to Run (03H)
The master may issue a release command to the slave following successful confiscation of the slave's memory. This command causes the RAM control to pass from the master to the slave processor. (see "CONFISCATE SLAVE'S MEMORY" command above.)

** Reset Slave (80H)
The master may reset a selected slave by issuing a RESET SLAVE command. This command causes the slave processor and other slave logic to be reset. The reset state is maintained until the master issues a "Clear Slave Request" command or the master "slave clear" line is asserted on the S100 Bus.

** Request Slave Service (40H)
A request/acknowledge handshake is implemented in the master-to-slave direction. This is done by the master issuing a Request Slave Service command. The command causes an interrupt to the slave's processor via the slave's CTC0 controller, channel 3. The slave may then issue an acknowledge command by asserting the SOFTREQ status signal. The cycle is completed by the master issuing a "Clear Slave Request" command.

** Interrupt Slave (20H)
The master has access to a second interrupt input in the slave's interrupt structure. This interrupt (CTC0 Channel 3) is asserted by the master's issuance of the "Interrupt Slave" command.

Slave Processor Control Logic

The slave control logic consists of two subdivisions. These are: (1) the Chip Select/Command Decoder and (2) the Slave Request Logic.

** Slave Processor Chip Select/Command Decoder
This logic decodes slave commands consisting of the following control functions:

** CSSIO
CSSIO is the chip select signal for the slave processor's seria
Input/Output (SIO) controller.

** CSPIO
CSPIO is the chip select signal for the slave processor's paral
Input/Output (PIO) controller.

** CSCTC
CSCTC is the chip select signal for the slave processor's count
timer (CTC) controller.

** CSSER
CSSER is the strobe signal utilized to assert one of the following functions:
- SOFT-REQUEST (I/O port address = 80H)
- HARD-REQUEST (I/O port address = 40H)
- SLAVE INTERRUPT REQUEST (I/O port address = 20H)

** Slave Request Logic

- SOFT-REQUEST
Soft-request is a signal asserted by the slave which may be read by the master. The slave asserts this signal when it requires service by the master but does not relinquish control to the master until the master initiates a slave memory confiscation process.

- HARD-REQUEST
Hard-request is a signal asserted by the slave processor which causes the slave processor to tri-state itself thereby suspending program execution. Note the difference between a soft and a hard request: the soft request does not cause immediate suspension of slave processor execution whereby the hard request does.

-SLAVE INTERRUPT REQUEST
The Slave Interrupt Request asserts a signal on the status port which may be polled by the master or asserts a signal via an Open collector driver which may be optionally connected to one of eight S100 Bus vectored interrupt lines (VI0-VI7).

Slave Clock Generator

The Slave Clock Generator consist of an 8 or 12 mhz oscillator, a divider and an active pull-up clock driver. An 8 mhz crystal is installed for the 4 mhz slave version and a 12 mhz crystal is installed for the 6 mhz version. A divider is used to shape the oscillator output for a 50% duty cycle. The resultant output is driven by an active pull-up which causes the clock logic to conform with the Z80 processor requirements.

Reset Generator

The slave's reset line is asserted to clear the slave's processor and internal logic. One of three reset sources cause the slave reset line to be asserted. These are:

- Master Prime
The master may issue a reset signal by asserting the I/O command "Reset Slave" (see HOST PROCESSOR STATUS/ COMMAND DECODER/LOGIC section).

- Slave Clear
The master may issue a reset signal by asserting the bus reset signal "Slave Clear" (S100 Bus pin 54).

- Slave Reset
The user may exercise a manual reset by providing a closure to ground on the slave reset input. A connector input located at the top of the slave circuit board is provided (J1). The input is debounced by a one-shot.

Input/Output Structure

The I/O structure consists of two serial I/O ports with associated baud rate generator and two parallel I/O ports.

Serial I/O Port Control

The Serial I/O Port Control consists of the Serial I/O Controller and the Baud Rate Clock Generator.

Serial I/O Controller

The Serial I/O (SIO) Controller is a programmable dual channel device which provides formatting for serial data communications. The channels can handle either asynchronous (Z80 SIO) or synchronous (Z80 Dart) data transfers to/from serial peripheral devices. The SIO operates either under programmed I/O or Interrupt Control. All lines necessary to handle asynchronous, synchronous, synchronous bit oriented protocols and other serial protocols are available to the user at the interface connectors. In addition, +/- 16 volt DC and +5 volt DC power are available at these connectors.

The SIO may be interfaced to peripheral devices requiring differing protocols. This interface is tailored to the exact device requirements by use of a Personality Module. The interface is implemented through two 16-pin Ansley connectors. Refer to the "Personality Board Users Guide" for a description of the serial Personality Modules currently available.

To program the SIO, the system software issues commands to initiate the mode of operation. Seven write registers exist for that purpose. In addition, three read registers allow the programmer to read the status of each channel.

Baud Rate Clock Generator

The Baud Rate Clock Generator consists of a clock generator and a CTC Programmable Interval Timer. The CTC 2.4576 MHz is a device which, under software control, can generate variable clock periods which are a multiple of the base input clock. The device has other modes of operation; however, only the modes applicable to the CPS-BMX operation will be described here.

The CTC consists of four channels, each with a signal input and all but one with a clock output. Channel 0 is tied to SIO channel A transmit and receiver clock inputs, channel 1 to SIO channel B transmit receiver clock inputs, channel 2 to interrupt 1 (master interrupt to slave) and channel 3 to interrupt 2 (master request to slave).

Channels 0 and 1 are connected to the SIO inputs via jumper options PJA and PJB. These signals are also tied to the serial interface connectors. If clock signals are originated by the interfacing devices, the jumpers are cut appropriately. The channel A jumper provides for separate transmit and receive clock inputs from the interface (connector J2) or may serve as baud rate generator outputs to the interface. This arrangement is intended to provide a clock to synchronous MODEM'S via "external" clock in accordance with the EIA RS-232C standards. The modem can then return a transmit/receive clock to the serial controller. In summary, means are provided to implement serial interfaces accommodating asynchronous, synchronous, HDLC and a great number of currently defined communications protocols.

For channels 0 and 1, the CTC generates a square wave whose period is defined by a count programmed into the respective channel's counter. The square wave will remain at a logical ZERO state for one half the count, and at logical ONE for the remaining half of the count. The counter decrements for each clock period that is received.

The CTC is programmed by the CPU specifying the mode, loading sequence and counter contents. The Baud rates that can be derived from the 2.4576 Megahertz clock are listed as follows:

Baud Rate	Theoretical Frequency (16 x clock)
600	9.6 kiloHertz
1200	19.2 kiloHertz
1800	28.8 kiloHertz
2000	32.0 kiloHertz
2400	38.4 kiloHertz
3600	57.6 kiloHertz
4800	76.8 kiloHertz
7200	115.2 kiloHertz
9600	153.6 kiloHertz
19200	307.2 kiloHertz

Parallel I/O Port Control Interface

The parallel I/O Port Control Interface consists of the Parallel I/O Controller (PIO). The Parallel I/O Controller is a programmable two-port LSI component, which interfaces peripheral devices to the Z80 microprocessor. The PIO provides data transfer to and from peripheral devices under programmed I/O or interrupt control. Handshaking data transfer control lines are provided to the interface in addition to the two eight-bit data ports. The CPU reset line and the CPU clock are also connected to this interface. The PIO is flexible and may be connected to peripheral devices requiring differing protocols.

The interface is tailored to the exact device requirements by use of a "Personality Module". The Personality Module is a small external circuit board which connects to the CPS-BMX to provide the hardware drivers and receivers, logic and other circuitry as required. Refer to Appendix A for a description of the parallel Personality modules currently available.

To program the PIO, the system software issues commands to initialize the mode of operation. Initialization is provided by loading the interrupt vector, mode, I/O and interrupt control registers.

S100 BUS INTERFACE

The CPS-BMX S100-BUS interface consists of 69 lines. These are grouped into sets used to transmit data, control & power. The groups are:

Group	No. of lines
Address Bus	24
Input Data Bus	8
Output Data Bus	8
Status Bus	4
Control Input Bus	4
Vectored Interrupt Bus	8
Utility Bus	4
System Power	9

Devices connected on the bus are classified as either bus masters or bus slaves and as either permanent or temporary masters. The CPS-BMX is a bus slave. It cannot take control of the bus. It can only request service by the master and once acknowledged, will be the only slave on the bus being serviced until the master releases the slave through an I/O command. File transfer to/from the slave are accomplished via memory-to-memory transfer from/to the master. Software may be configured to execute the transfers under DMA control in which case the transfer rate is approximately 571 Kbyte/second.

Each of the S-100 Bus signals utilized by the CPS-BMX are described on the following pages. A summary of the S-100 Bus signals in included in Appendix B.

ADDRESS BUS

The address bus consists of 24 lines designated as A0 through A23. The address lines A0 through A15 address one of 64 Kbytes of the slave memory whereby address lines A16 through A23 map the slave memory onto the master's address space. All address lines are sampled during master memory cycles. Address lines A0 through A7 are used by the slave during master I/O cycles to transfer I/O commands from the master and status inputs to the master.

INPUT DATA BUS

The input data bus consists of 8 lines designated as D00 through D07. Data inputs from the master to slave are accepted during master memory & I/O output cycles when the slave is addressed appropriately.

OUTPUT DATA BUS

The output data bus consists of 8 lines desiginated as DIO through DI7. Data outputs from the slave to the master are accepted during master memory & I/O input cycles when the slave is addressed appropriately.

STATUS BUS

The status bus consists of 4 master output lines which define the current master processor bus cycle. The status lines used by the slave are:

STATUS	FUNCTION
sMEMR	Master memory read cycle
sM1	Master Opcode fetch cycle
sINP	Master input cycle
sOUT	Master output cycle

-sMEMR

sMEMR is used by the slave to generate memory read cycles when the master confiscates the slave's memory & executes a read cycle.

-sM1

sM1 is used by the slave to detect master OPcode fetch cycles in order to subsequently generate refresh cycles in the

slave memory. This operation takes place only during the time that the master has confiscated the slave's memory.

-sINP
sINP is used in the slave to extract the slave's status:

Hard-Request	(Bit 7)
In-Service	(Bit 6)
Interrupt Request	(Bit 5)
Soft-Request	(Bit 4)

-sOUT
sOUT is used in the slave to execute one of the eight commands to the slave. See "Host Processor Status/Command Decoder//Logic".

CONTROL INPUT BUS

The control input bus consists of 4 master output lines which define the master's current processor cycle. These consist of:

Signal	Function
pDBIN	Master read cycle
pWR*	Master write cycle
pSYNC	Master processor start cycle
PSTVAL*	Master status valid

-pDBIN
pDBIN is used in combination with sM1 to detect master OPcode fetch cycles to generate refresh cycles in the slave's memory. It is also used to output memory read data to the master as well as slave status signals to the master.

-pWR*
pWR* is used to write input commands/data from the master to the slave.

-pSYNC
pSYNC is used to qualify sMEMR in generating memory read cycles during master confiscation of slave's memory. Connection of this signal to the read cycle generator is optional. See "Solder/Trace Cut Options - PJC".

-pSTVAL*
pSTVAL* is used to qualify sMEMR in generating memory read cycles during master confiscation of slave's memory. Connection of this signal to the read cycle generator is optional. See "Solder/Trace Cut Options - PJD".

VECTORED INTERRUPT BUS

The slave may generate an interrupt to the master via the vectored interrupt bus. The interrupt pulse is generated by the slaves processor's execution of an output write cycle to port 20H. See "Slave Processor Control Logic". The user may connect the interrupt pulse generator to one of the eight vectored interrupt lines (VI0 - VI7) through a jumper option. See "Solder/Trace Cut Options - VIX".

UTILITY BUS

The utility bus signals utilized by the slave consist of:

ϕ (Clock)	Master system clock
MWRITE	Master memory write strobe
SLAVE CLR	Master slave clear
SIXTN	Eight/Sixteendatatransfer status

-ϕ (Clock)
ϕ is used in the slave to synchronize the master's read slave's-memory cycle and the refresh pulse generator during the master's confiscation of the slave's memory.

-MWRITE
MWRITE is used by the master to generate memory write cycles during the master's confiscation of the slave's memory.

-SLAVE CLR
SLAVE CLR is used in the slave to generate a reset signal to internal logic and to the slave CPU when the master asserts the SLAVE CLR signal.

-SIXTN
SIXTN is a signal used by the master to determine if the slave is to transfer eight or sixteen data bits during a master read cycle. This line is optionaly connected through a jumper option. See "Solder/Trace Cut Option - PJF".

SYSTEM POWER

The system power utilized by the slave consists of:

+8 VDC	(2 lines)
+16 VDC	(1 line)
-16 VDC	(1 line)
Ground	(5 lines)

The +8 VDC is input to a +5 VDC regulator to generate the slaves +5 volt power. The +/- 16 VDC lines are routed to the serial I/O connectors where they may be utilized to generate regulated power

for such applications as RS232 receivers. The +/- 16 VDC lines are routed via fuse links (thin trace areas) on the PCB which "burn open" in the event of a short circuit on the personality board connected to the serial I/O connectors. The ground lines are connected to the PCB ground plane. Grounds from pins 20, 53 & 70 are optionally connected through jumper areas. See "Solder/Trace Cut Options - PJE, PJG , PJH".

**** OPERATING INSTRUCTIONS ****

Instructions are given herein to configure the CPS-BMX from both the hardware and software standpoint.

Hardware Setup Instructions

The hardware is configured via jumper options and solder/trace cut areas. The solder/trace cut areas are referred to as PJX, where X is the area designator. An exception is the jumper area designated as VI0 thru VI7 where a jumper may be installed to connect to the vectored interrupt lines of the S100 Bus. The PJX and VI0-7 options are located on the "solder" side of the board. Two jumper areas are provided on the "component" side. These are implemented by header jumpers.

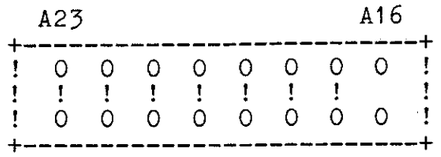
Jumper Options

Refer to figure 1 to locate the header jumper areas. These are designated as the EXT ADDR SEL and I/O PORT SEL jumpers.

EXTENDED ADDRESS SELECT (EXT ADDR SEL)

Logic is provided to map the slave's memory within the master's 16 megabyte memory address space by comparing the master's extended address lines [A16 (M) through A22 (M)] against a corresponding eight position jumper. Successful comparison results in master/slave memory transfers provided that the slave's service request was previously acknowledged by the master via a similar process for a master/slave I/O transfer. The extended address comparison jumper is designated as EXT ADDR SEL on the board's silk screen. The jumper setting designates the page within the master's 16 megabyte address space that the slave's memory will reside in during the master's confiscation of the slave's memory.

EXT ADDR SEL



EXAMPLE:

To map the slave memory into the first 64Kbyte page above the master's 64Kbyte on board address space (010000H to 01FFFF), install jumpers in positions corresponding to A17 through A23 and leave A16 position open.

Note: 1. A jumper installed corresponds to a logic 0 setting and the absence of a jumper corresponds to a logic 1 setting.

2. All slaves under the control of a common TURBOdos master must be set to reside in the same 64Kbyte pages; ie: all EXT ADDR SEL jumper settings must be the same for each slave. Factory settings are provided for all slaves with EXT ADDR SEL set at 01H. TurboDOS software is configured for that setting.

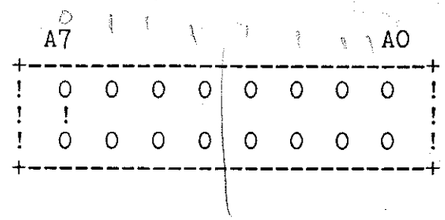
3. Any other S100 Bus device installed in the bus that is memory mapped may not reside within the address space assigned to the slave(s).

01-10-12 MIW
≤5 users 0 0 0 1 0 0 0 0

I/O PORT SELECT (I/O PORT SEL)

The master transfers commands to the slaves and receives status from the slaves through I/O Bus transfers. Logic is provided to map the slave within the master's 256 byte I/O address space by comparing the master's address lines [A0 (M) through A7 (M)] against a corresponding eight position jumper. Successful comparison results in a master/slave I/O transfer. It is through I/O status and command transfers that the master determines if a slave requires service and if a slave is to be confiscated for subsequent file transfers to/from the slave's memory.

I/O PORT SEL



EXAMPLE:

To map the slave into the I/O address space 7FH, install a jumper in position A7 and none in the remaining positions.

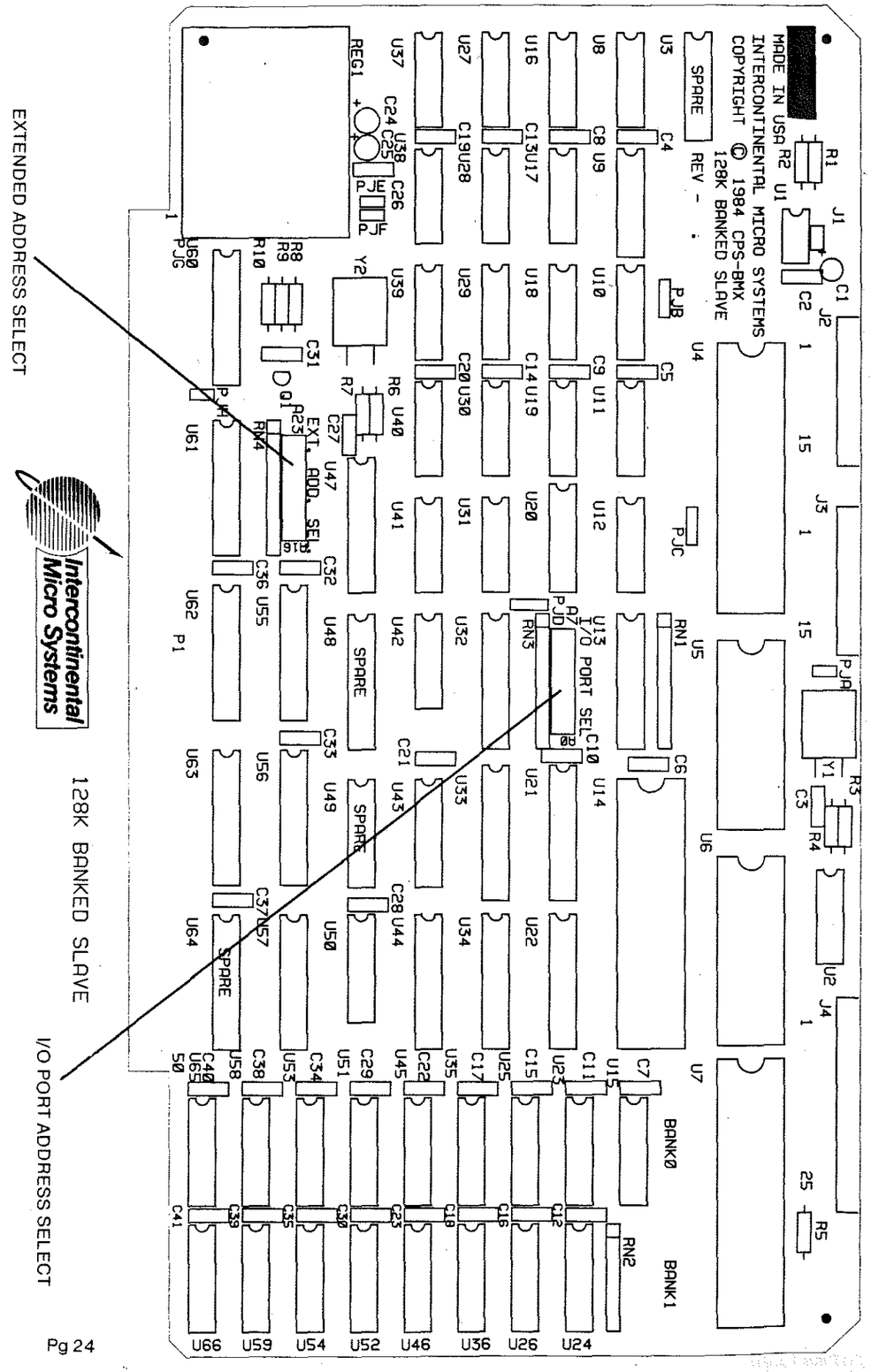
Note: 1. A jumper installed corresponds to a logic 0 setting and the absence of a jumper corresponds to a logic 1 setting.

2. Slaves under the control of a common master must be set to reside in individual I/O locations. ie: All I/O PORT SEL jumper settings are mutually exclusive. Factory settings are provided for all slaves with I/O PORT SEL set at 7FH. The customer must provide jumpers to map each slave at exclusive locations. The TURBOdos operating system is then configured as follows:

DEFAULT I/O PORT SETTING:

Slave Number:	1	2	3	4	5	6	7	8
I/O address :	7FH	7EH	7DH	7CH	7BH	7AH	79H	78H

Slave Number:	9	10	11	12	13	14	15	16
I/O address :	77H	76H	75H	74H	73H	72H	71H	70H



JUMPER OPTIONS
- FIGURE 1 -

SOLDER/TRACE CUT OPTIONS

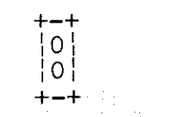
Refer to figure 2 to locate the solder/trace cut areas. These are listed as follows:

PJA - SIO Port B Clock Source Select
PJB - Master Address Multiplexer Timing Select
PJC - SIO Port A Clock Source Select
PJD - 512/1024 Common Memory Range Select
PJE - MasterMemoryCycle qualifiedon pSYNC
PJF - Master Memory Cycle qualified on pSTVAL
PJG - Connect Slave Interrupt Request VI Lines
PJH - Pull-up SIXTN Status

PJA

To source SIO Port B input from the SIO connector only, cut the trace at PJA. The source can now be connected through the personality board on pin P3-3.

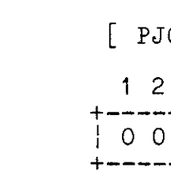
[PJA] area



PJB

This jumper allows the refresh cycle to start at the rising or trailing edge of the master's system clock to give the system integrator the flexability of adjusting the refresh timing to other master processors. The CPS-BMX comes configured with PJB connected from 2-to-3 which causes the refresh address multiplexer to sample refresh address at the early part of the refresh cycle. To configure the timing so that the multiplexer samples the refresh address at the late part of the refresh cycle, cut the etch from 2-to-3 and connect from 1-to-2.

[PJB] area



PJC

The CPS-BMX comes configured so that the SIO ports receive their baud clocks from an on-board programmable timer. The board could be reconfigured to source the clocks from the SIO serial port connectors. Such is the case when synchronous modems connect to the serial ports. The modem provides a clock to the SIO. Furthermore, the modem may receive the clock from the on-board timer, condition the clock and return it to the input of the SIO. The transmit and receive clocks may be sourced separately on Port A. All combinations are possible through this jumper.

To source SIO PORT A inputs from the SIO connector only, cut the trace from PJC 2 to PJC 3. The source can now be connected through the personality board on either PIN P2-2 or P2-3.

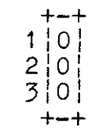
If the SIO PORT A inputs are to be sourced separately from the SIO connector, cut the trace from PJC 1 to PJC 2. The receive clock is now input on P2-3 and the transmit clock is input on P2-2.

[PJC] area

PJD

The CPS-BMX has 128 Kbytes of memory arranged as two 64 Kbyte banks, each selectable by the slave processor. In order for the slave processor to switch from one bank to the other, a section of memory referred to as "common memory" must be allocated. Common memory contains code which is executable regardless of which bank is active at the time. The CPS-BMX comes configured so that common memory resides at the uppermost part of the 64 Kbyte address space. Common memory is exactly one Kbyte in size thus allowing a possible TPA of 64,253 under TurboDOS. TPA may be increased further by reconfiguring PJD provided the operating system allows for a smaller common memory allocation. The CPS-BMX comes configured for a common memory size of 1 Kbyte. The common memory may be reduced to 512 bytes by cutting the etch from JD 2-to-3 and connecting from 1-to-2.

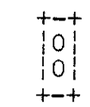
[PJD] area



PJE

When the host processor confiscates the slave's memory, the host processor generates memory read cycles based on the host's memory read status signal sMEMR. Option are provided to qualify the read cycle generation with pSYNC or pSTVAL or both. With the CPZ-4800X SBCP used as the host, neither pSYNC nor sSTVAL are used. PJE & PJF provide compatibility with IEEE timing signals requirements by connecting both jumpers.

[PJE] area



To qualify the memory read cycle with pSYNC, connect PJE.

PJF

See PJE jumper description above.

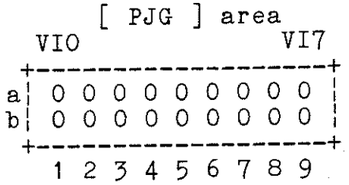
[PJE] area

To qualify the memory read cycle with pSTVAL, connect PJF.

PJG

The CPS-BMX may assert an interrupt to the host (Slave Interrupt Request). The interrupt may be connected to one of 8 VI lines of the S100 bus. This is accomplished by connecting a strap on the PJG jumper area. TurboDOS does not utilize this feature.

[PJG] area

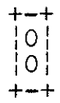


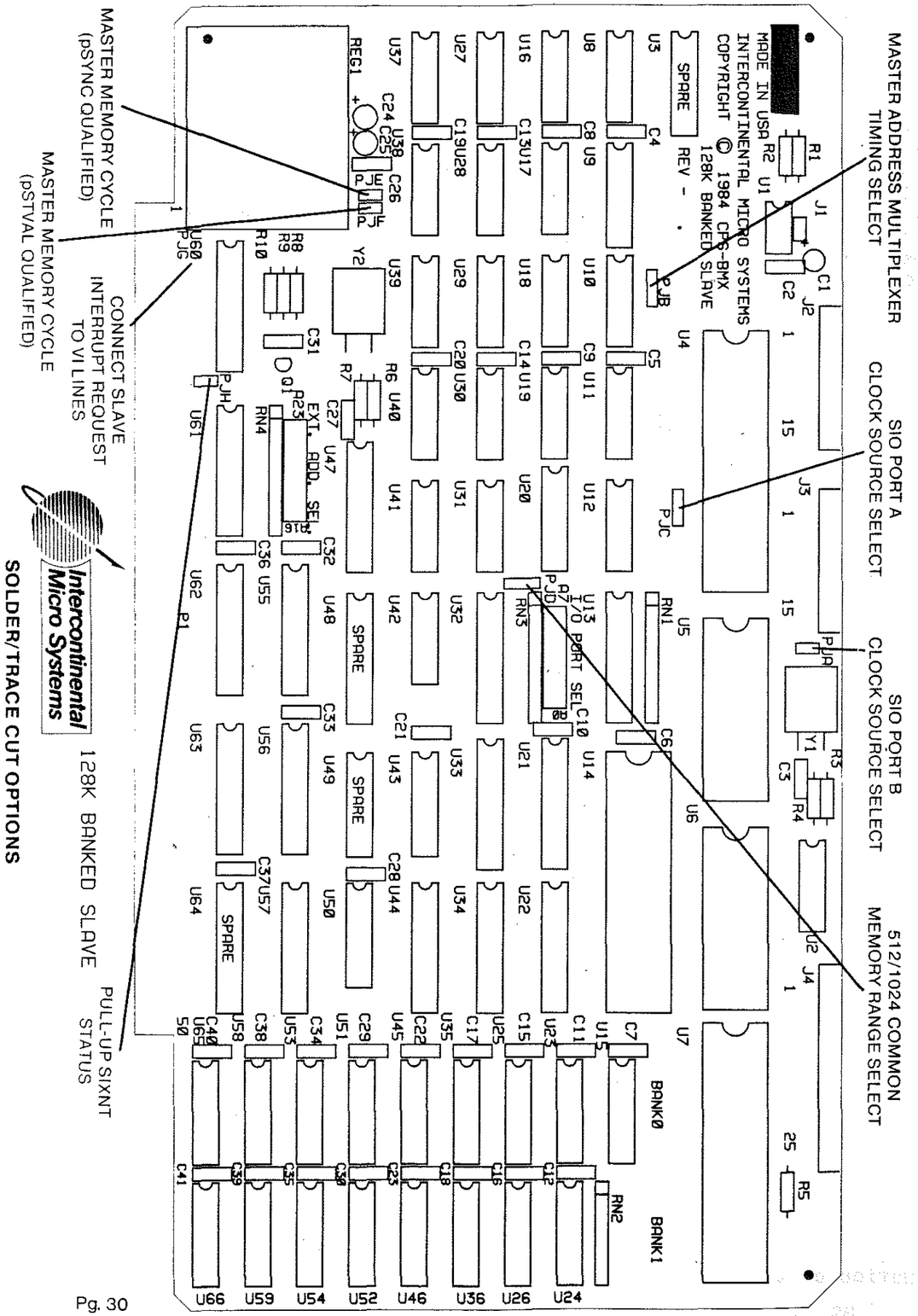
As an example, to connect Slave Interrupt Request to VI1, connect a jumper from a2-to-b2.

PJH

The CPS-BMX is compatible with IEEE 16 data bit processors such as 8086 based Cpu's; however the CPS-BMX transfers 8 bit data only. In accordance with the IEEE 696.1/D2 specification, SIXTN is interrogated by the host to determine if the data bus transfer consists of 16 or 8 data bits. If SIXTN* is found to be at a logic high, the host transfers 8 data bits. The CPS-BMX must be strapped to present a logic high on the SIXTN* line. This is accomplished by providing a strap on PJH.

[PJH] area





SOLDER/TRACE CUT OPTIONS
- FIGURE 2 -

PERSONALITY BOARD INTERCONNECTION INSTRUCTIONS

The CPS-BMX has four connectors at the top of the board numbered J1 through J4. These are listed below: (See Appendix A- Connector Tables)

J1 - Slave reset connector
J2 - SIO Port A Connector
J3 - SIO Port B Connector
J4 - PIO Connector

J2,J3 & J4 are typically connected to peripheral devices through personality boards which are small printed circuit boards customizing the above listed devices to a variety of peripherals. The slave may be reset by providing a switch closure across J1. J1 may be left open without adverse effect as this input is pulled-up.

Most S-100 Bus chassis provide a jumper plate at the rear of the chassis to which peripheral connectors are installed. Typically, the connectors are of the ITT CANNON DB25 type. The personality boards provided by ICM are boards with DB25 connectors at one end and header plugs at the other. The DB25 connector end is to be installed in the cutouts provided on the connector plate. Flat ribbon cable then connects the CPS-BMX connector to the personality board. See figure 3 showing a personality board installation.

At a minimum, a SIO Port B (RPB-100) personality board must be installed. The instructions follow:

1. - Select a DB25 connector cutout at the rear of the chassis for the RBP100 personality board.
2. - Insert and hold the RPB-100 personality board in the cutout.
3. - Install #6 nuts, washers and bolts passing the bolts through the personality board's DB25 connector.
4. - Install the flat ribbon cable provided at the personality board and at the CPS-BMX connector J3.
5. - Install a cable from the chassis connector to the peripheral.

Refer to the "Personality Board User's Guide" for a complete description of the Personality Boards available and for instructions on interfacing these boards.

**** SLAVE I/O ASSIGNMENTS ****

Master Side

Slave I/O Base Address ..... 0 - FF hex (Master R/W)
Slave Status ..... Slave I/O Base (Master Read)

Slave Status Bits .. (master read)

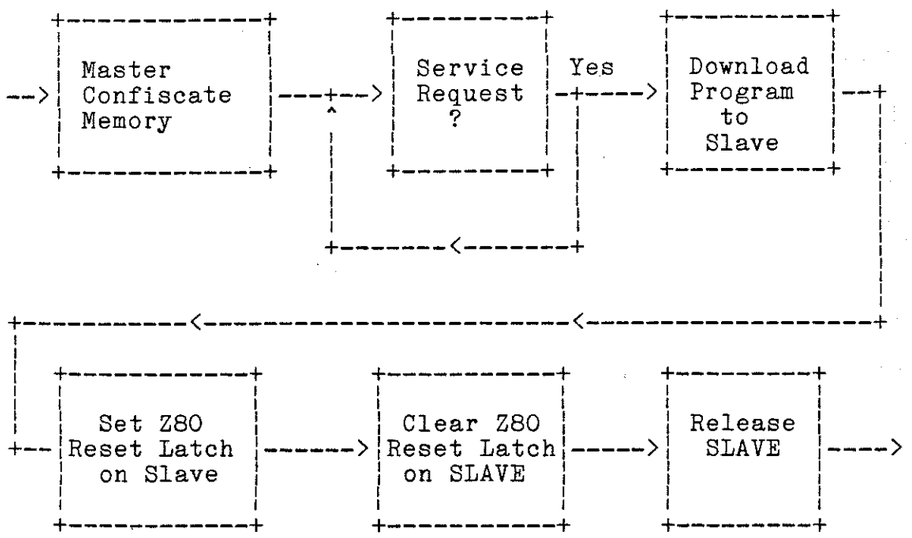
bit	7	6	5	4	3	2	1	0
	REQUEST	SERVICE	SLV INT REQ	SOFT REQUEST	UNDEF	UNDEF	UNDEF	UNDEF

CPZMCDBZ ⇒ MEMRQ
SVCREQ

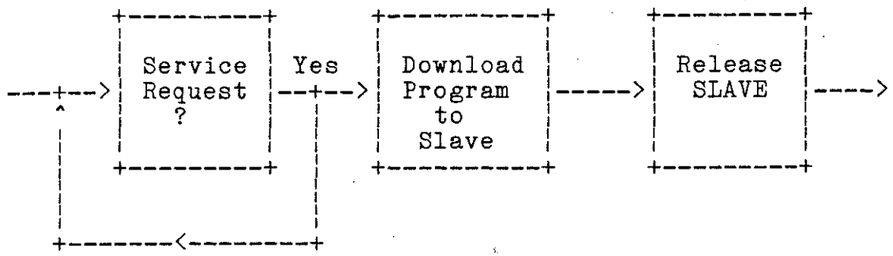
Slave Command Bits .. (master write) .. Slave I/O Base Address

bit	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	... Clear Slave Request/Reset
	0	0	0	0	0	0	0	1	... Master Confiscate of Slave
	0	0	0	0	0	0	1	0	... Clear Reset Latch only
	0	0	0	0	0	0	1	1	... Release Slave to Run
	1	0	0	0	0	0	0	0	... Reset SLAVE Z-80 CPU chip
	0	1	0	0	0	0	0	0	... Master Request to Slave
	0	0	1	0	0	0	0	0	... Master Intrp to Slave

Below is a flowchart of how a MASTER might confiscate a SLAVE for program down loading.



Below is an example of using the SLAVE for normal MASTER/SLAVE transactions.



Slave Side

All SLAVES have the following internal I/O ports defined.

SIO chan A	00 hex (read/write)
SIO chan B	02 hex (read/write)
PIO chan A	04 hex (read/write)
PIO chan B	06 hex (read/write)
CTC0 chan 0	08 hex (read/write)
CTC0 chan 1	09 hex (read/write)
CTC0 chan 2	0A hex (read/write)
CTC0 chan 3	0B hex (read/write)
CTC1 chan 0	10 hex (read/write)
CTC1 chan 1	11 hex (read/write)
CTC1 chan 2	12 hex (read/write)
CTC1 chan 3	13 hex (read/write)
BANK SWITCH (bank 0)	14 hex (write only)
BANK SWITCH (bank 1)	15 hex (write only)
REQUEST SERVICE (Hard)	4C hex (write only)
REQUEST SERVICE (Soft)	8C hex (write only)

NOTE: The Slave internal I/O ports can not be read or written by the Master CPU.

The slave executes a hard service request from the master by outputting to port 4C hex. The byte sent to port 4C hex has no meaning. Just the function of writing to Port 4C hex causes the Request to happen.

*** APPENDIX ***

J1

	SIGNAL	FUNCTION
J1-1	SRESET*	Slave Reset
J1-2	Ground	Ground

J2

	SIGNAL	FUNCTION
J2-1	ADSR*	Port A Data Set Ready
J2-2	ATXC*	Port A transmit clock
J2-3	ARXC*	Port A receive clock
J2-4	ATXD	Port A transmit data
J2-5	ARXD	Port A receive data
J2-6	ARTS*	Port A request-to-send
J2-7	ACTS*	Port A clear-to-send
J2-8	ADCD*	Port A data carrier detect
J2-9	ADTR*	Port A data terminal ready
J2-10	ARNG*	Port A ring indicator (not connected)
J2-11	ABRCLK	Port A baud rate clock
J2-12	GND	Ground
J2-13	+16 VDC	+16 VDC power
J2-14	-16 VDC	-16 VDC power
J2-15	+5 VDC	+5 VDC power
J2-16	GND	Ground

J3

	SIGNAL	FUNCTION
J3-1	BDSR*	Port B Data Set Ready
J3-2	BTXC*	Port B transmit clock
J3-3	BRXC*	Port B receive clock
J3-4	BTXD	Port B transmit data
J3-5	BRXD	Port B receive data
J3-6	BRTS*	Port B request-to-send
J3-7	BCTS*	Port B clear-to-send
J3-8	BDCD*	Port B data carrier detect
J3-9	BDTR*	Port B data terminal ready
J3-10	BRNG*	Port B ring indicator (not connected)
J3-11	BBRCLK	Port B baud rate clock
J3-12	GND	Port B Ground
J3-13	+16 VDC	Port B +16 VDC power
J3-14	-16 VDC	Port B -16 VDC power
J3-15	+5 VDC	Port B +5 VDC power
J3-16	GND	Port B Ground

J4

	SIGNAL	FUNCTION
J4-1	RDYA	Port A Ready
J4-2	STBA*	Port A Strobe
J4-3	RDYB	Port B Ready
J4-4	STBB*	Port B Strobe
J4-5	D0A	Port A DATA BIT 0
J4-6	D1A	Port A DATA BIT 1
J4-7	D2A	Port A DATA BIT 2
J4-8	D3A	Port A DATA BIT 3
J4-9	D4A	Port A DATA BIT 4
J4-10	D5A	Port A DATA BIT 5
J4-11	D6A	Port A DATA BIT 6
J4-12	D7A	Port A DATA BIT 7
J4-13	D0B	Port B DATA BIT 0
J4-14	D1B	Port B DATA BIT 1
J4-15	D2B	Port B DATA BIT 2
J4-16	D3B	Port B DATA BIT 3
J4-17	D4B	Port B DATA BIT 4
J4-18	D5B	Port B DATA BIT 5
J4-19	D6B	Port B DATA BIT 6
J4-20	D7B	Port B DATA BIT 7
J4-21	RESET*	RESET OUTPUT
J4-22	GND	GROUND
J4-23	INT3*	INTERRUPT
J4-24	GND	GROUND
J4-25	PCLK	CLOCK OUTPUT

**** WARRANTY ****

All products sold hereunder are under warranty on a return to factory basis against defects in workmanship and material for a period of one (1) year from the date of delivery.

Conditions of this warranty are as follows: Purchaser must 1) obtain a return material authorization (RMA) number and shipping instructions, 2) product must be shipped prepaid, 3) written description of the failure must be included with the defective product. All transportation charges inside the continental U.S. will be paid by Intercontinental Micro Systems (ICM) Corp. For products returned from all other locations, transportation must be prepaid. Should ICM determine that the products are not defective, the purchaser must pay all return transportation charges. All repairs will be provided at repair rates being charged at the time by ICM. Under the above product warranty, ICM may, at its option, either repair or replace any component which fails during the warranty period providing the purchaser has reported same in a prompt manner. All replaced products or parts shall become property of ICM.

All above warranties are contingent upon proper use of the product. These warranties will not apply 1) if any repair, parts replacement, or adjustments are necessary due to accident , unusual physical, electrical or electromagnetic stress, neglect, misuse, failure of electric power, air conditioning, humidity control, transportation, failure of rotating media not furnished by ICM, operation with media not meeting or not maintained in accordance with ICM specifications or causes other than ordinary use, 2) if the product has been modified by purchaser, 3) where ICM's serial numbers or warranty date decals have been removed or altered, 4) if the product has been dismantled by purchaser without the supervision of or prior written approval of ICM.

EXCEPT FOR THE EXPRESS WARRANTIES CONTAINED HEREIN, ICM DISCLAIMS ALL WARRANTIES ON THE PRODUCTS FURNISHED HEREUNDER, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS; and the stated express warranties are in lieu of all obligations or liabilities on the part of ICM arising out of or in connection with the performance of the products. ICM is not liable for any indirect or consequential damages.

After the warranty period, the products will be repaired for a service charge plus parts, provided that it is returned prepaid to ICM after retaining a return material authorization (RMA) number.