

# A one-megapixel reflective spatial light modulator system for holographic storage

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**A prototype reflective spatial light modulator (SLM) system has been developed for writing megabit pages of data into a holographic medium at a rate of 12 pages per minute. The SLM is based upon a crystalline-silicon reflective active-matrix array with integrated data drivers, using liquid crystal (LC) electro-optics and a personal computer system with an interface to provide data. The LC has been optimized for high contrast and efficiency with coherent illumination. The resolution-limited contrast was measured at 4:1, which was high enough to provide bit-error-free charge-coupled-device images using modulation and error-correction codes.**

## Introduction

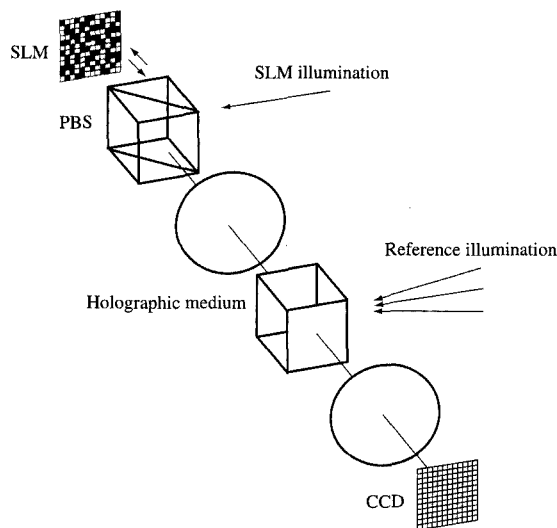
Recent development in spatial light modulators (SLMs) is helping to make volume holographic storage for digital

data a reality [1, 2]. SLMs consist of one- or two-dimensional arrays of light-modulating elements. Silicon technology as used in projection data monitors is now capable of producing small-sized, two-dimensional light-valve arrays having several hundred thousand to several million light-modulating elements. This allows imaging or writing very large amounts of information at one time. Given high image-update rates, high data-writing rates are possible. With increases in the speed of writing and reading with high-speed charge-coupled-device (CCD) cameras, holographic recording may be able to compete with other recording technologies. Efficient compact recording systems are possible through the use of projection-display, reflective-silicon light-valve technology [3]. The reflective-silicon light-valve technology has a high aperture ratio and the ability to match its pixel size with the CCD camera pixel size.

The development focus of our prototype holographic-recording reflective SLM system was aimed at 1) suitable light modulation of the LC; 2) the silicon back-plane or

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**Figure 1**

Holographic data storage system diagram in which the SLM is illuminated by and imaged through a polarizing beam splitter into the holographic medium interfering with reference illumination for writing. For reading, only the reference beam is used.

chip design; 3) a system to provide data to the SLM at a sufficient writing rate; and 4) testing of the SLM as it relates to holographic recording.

### Reflective SLM holographic recording

In developing an SLM system suitable for holographic recording, it is useful to look at how a reflective SLM is used in a holographic recording. Holographic recording is accomplished by the interference of an image beam and a reference laser beam within a holographic recording medium—in this case, a photorefractive material such as  $\text{LiNbO}_3$ . The optical interference pattern causes charges to be excited from impurity centers. After diffusion and re-trapping, the redistributed charge forms a grating in the photorefractive medium. Depending upon the medium material, a fixing process for long-term storage of data may be required. When the medium is exposed to only the reference beam, the light will diffract to reproduce the image. **Figure 1** shows the basic elements of a holographic data storage system. The spatial light modulator converts the digital data of ones and zeros into a two-dimensional array of bright and dark spots. The Fourier plane image of the array is the image to be stored in the holographic medium. A uniform laser beam is directed in an orthogonal manner onto the reflective surface of the SLM by a polarizing beam splitter (PBS). The PBS allows the polarization-converted image to be focused into the

holographic medium. The reconstructed data are imaged onto a CCD camera system, which detects the reconstructed hologram as digital information. Multiple images comprising a stack can be written separately into the same volume of the holographic medium by changing the angle of the reference beam or by selection of multiple reference beams into the medium. Multiple stacks provide the desired system capacity.

The method of producing the image beam for writing consists of sending data to the SLM while it is addressed by rows from top to bottom. The pixels retain their voltage long enough for the array to be addressed and exposed. The LC must respond to the voltage excitation of the last row in the array before the SLM image is illuminated. To avoid dc voltage across the LC, which may cause image sticking, the polarity of the pixel voltage is reversed in the next frame. The amount of exposure time depends upon the holographic material and on available laser power. The minimum exposure for  $\text{LiNbO}_3$  is between 50 and 100 milliseconds.

### Reflective twisted nematic liquid crystal

Development was focused on the properties of LC light modulation as it pertains to holographic recording. We concentrated on twisted nematic (TN) normally black (NB) LC modes, since they offer higher contrast with low drive voltages as compared to normally white (NW) modes [4]. The PBS allows efficient illumination and cross-polarization for NB operation with reflective SLMs. The normally black LC crystal mode provides electro-optic modulation by changing the polarization of reflected light by  $90^\circ$  with about  $3 V_{\text{RMS}}$  applied, while leaving the polarization unchanged for zero (or low) applied voltage. The cover glass has a transparent indium-tin oxide (ITO) conductor on the inside surface. On the cover-glass ITO and on the SLM mirror surfaces, thin polyimide layers are deposited and rubbed to provide for LC alignment. The LC molecules align with the rubbing direction. The ITO voltage is held constant at 3 V, and a 0–6-V square-wave voltage is applied to the pixel mirrors for LC electro-optic modulation. The equivalent of a transmissive  $90^\circ$ -twisted nematic LC mode is the reflective  $45^\circ$ -twisted nematic LC mode. **Figure 2** depicts the reflective  $45^\circ$ -twisted nematic LC operation. The rubbing direction on the mirrors is rotated  $45^\circ$  relative to the rubbing direction on the cover glass, providing a  $45^\circ$  twist in LC alignment between the two surfaces. The incoming polarized illumination is aligned with the rubbing direction of the cover glass. As the incoming illumination passes through the LC, the polarization is rotated  $45^\circ$ . After reflection, the direction of polarization and its rotation are reversed. Upon exiting the SLM, the polarization is the same as the incoming polarization. With applied voltage, the LC molecules try to orient with the electric field, which is perpendicular to

the cover-glass and SLM surfaces. The incident light theoretically becomes nearly circularly polarized as it reaches the mirror. After reflection, polarization becomes nearly linear again as it exits the cell, but is rotated 90°. If perfectly linear, the polarization conversion would be 100% efficient. Efficient polarization conversion for wavelengths and LC materials of interest was obtained by detailed LC modeling, cell fabrication, and evaluation.

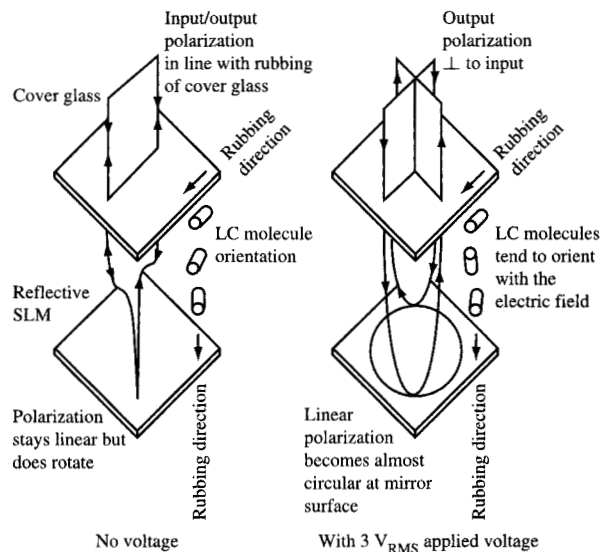
• *LC modeling*

Modeling of the electro-optical properties of LC spatial light modulators in order to optimize the modulator qualities in terms of contrast ratio, polarization conversion, and cell-gap fabrication tolerances has become increasingly important, because all relevant parameters may be varied easily and certain relations may be investigated specifically. The computer simulation of the static electro-optical behavior has been done in two steps. First, the orientation of the nematic director as a function of distance from each cell surface has to be computed. The theoretical analysis of the LC director profile in a cell with an applied field has been well documented in the literature [5–7]. We followed the papers by Deuling [6, 7] for the computations of the nematic director profile in the LC cell as a function of applied voltage.

The second step of the simulation deals with light propagation in the quiescent and deformed LC media, which are inhomogeneous and uniaxial. Although many methods have been developed for this application, we have made our computations based on the Jones-matrix method [8] and the  $4 \times 4$  matrix method described by Berreman [9] and by Wohler et al. [10]. We have found that at near normal incidence, the computed polarization-conversion efficiency of the Jones-matrix method, which ignores the reflection due to the interface between any two dielectric media, has a negligible difference from the result of the  $4 \times 4$  matrix method, provided that the reflective SLM has less than 0.5% reflection between the air and the cover-glass window. This is achieved by using antireflection coatings on the glass window and by making the ITO thickness approximately equal to half of the incident wavelength. We have constructed our SLMs to satisfy the latter two conditions. Hence, we have used the Jones-matrix method for both quiescent and deformed SLM states to take advantage of the polarization-conversion efficiency of the quiescent state of the SLM offered by the Jones-matrix method [4]. This facilitates our analysis of the quiescent state as the dark state of the SLM, to estimate the contrast ratio as well as the cell-gap tolerance.

*Quiescent (uniformly twisted) states*

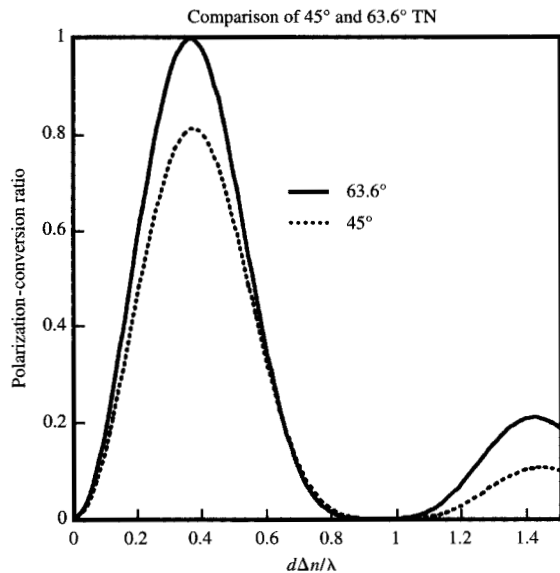
The LC polarization-conversion efficiency is determined by the bright or “on” state behavior, while the LC contrast



**Figure 2**

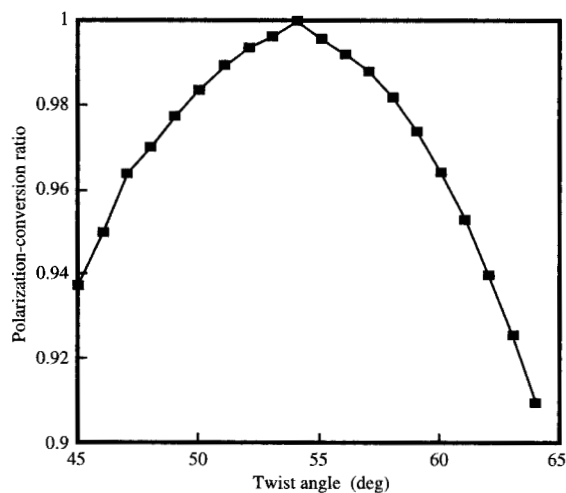
The 45°-twisted reflective LC mode. With no voltage, the LC molecules are aligned parallel with the cover glass and SLM surfaces, and the polarization rotates about 45° from the cover glass to the mirror. The rotation reverses its direction in the reflected path. With applied voltage the LC molecules tend to orient with the electric field, giving nearly circular polarization at the mirror surface. Upon exiting, the polarization rotates 90° and is nearly linear.

ratio is mostly determined by the dark or “off” state. The dark state of the reflective twisted nematic LC normally black mode is determined by the twist angle and the quantity  $d\Delta n/\lambda$ , where  $d$  is the cell gap,  $\Delta n$  is the anisotropy of the index of refraction of the LC material, and  $\lambda$  is the wavelength of the illuminating light. The Jones matrix is used to find an initial design point for different LC twist angles, assuming uniform twisting of LC molecules between the SLM mirror and the cover-glass surfaces. We also assumed that the LC molecules have a small uniform tilt angle (about 2°) from the substrate surface across the LC cell. **Figure 3** shows calculated polarization-conversion efficiencies as a function  $d\Delta n/\lambda$  for the 45°- and 63.6°-twisted angles. The polarization-conversion efficiencies are approximately 82% and 100%, respectively. For operation in the normally black mode, liquid crystal cells should be fabricated at the first minimum, where  $d\Delta n/\lambda = \sqrt{1 - (\alpha/\pi)^2}$  and  $\alpha$  is the twist angle; i.e., for  $\alpha = \pi/4$ ,  $d\Delta n/\lambda \approx 1$ . Test cells built and measured in the deformed states or “field-on” states showed that the 45°-twisted cells had higher polarization-conversion efficiency than 63.6°-twisted cells. This indicated to us that



**Figure 3**

Quiescent-state simulation of polarization-conversion efficiency with  $d\Delta n/\lambda$ . The 63.6°-twisted nematic LC has nearly 100% conversion efficiency. However, the 63.6°-twisted case has a greater insensitivity to parameter variations in the off state at  $d\Delta n/\lambda = 1$ .



**Figure 4**

Polarization-conversion ratio as function of twist angle using the deformed and tilted-state model. Maximum polarization conversion for LC material chosen occurred at 54°.

we cannot optimize the LC performance on the basis of the quiescent state alone.

*Deformed and tilted state (nonuniformly twisted)*

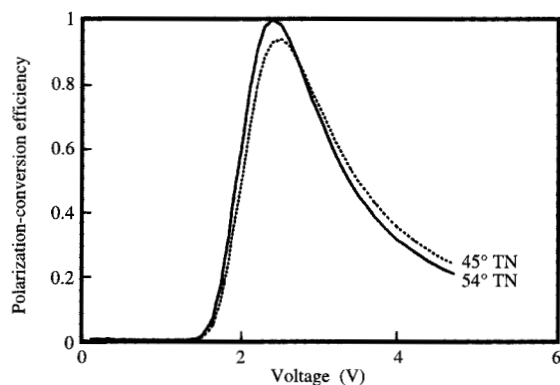
The deformed state is characterized by nonuniform tilting and twisting of the LC director. The director tries to align with the applied electric field but is constrained at the surfaces, so the orientation in the middle of the cell is a balance between the electric driving force and the elastic restraining forces. The resulting configuration is different from the quiescent configuration, as is the polarization-conversion behavior. The polarization-conversion efficiencies based upon deformed states as a function of the twist angle of the quiescent LC cell are shown in **Figure 4**. The conversion efficiency as a function of voltage is shown in **Figure 5**. Both figures show a polarization-conversion efficiency of approximately 93% and 100% for the 45°- and 54°-twisted angles, respectively. Both twist angles have contrast better than 200:1 with  $\pm 7\%$  dark-state assembly tolerance. Assembled SLMs have also shown that the 54°-twisted nematic LC has excellent efficiency, as well as large-area contrast with good assembly tolerance.

*Resolution-limited contrast*

Large-area contrast is an important measure of cell uniformity and process control and is very important in display applications. For holographic storage, resolution-limited contrast rather than large-area contrast is a more useful design criterion, since the data being stored may not be images and may lack spatial correlation. The use of modulation, interleaving, and error-correction codes further reduces the spatial coherence of the SLM image.

Typically, even SLMs having high large-area (all-on to all-off) contrast ( $>100:1$ ) will have much lower (about 4:1) pixel-resolution-limited (adjacent-pixel-on-to-off) contrast. The difference is due to a variety of effects, including scattered light from irregularities in the cell at the subpixel level; three-dimensional effects due to size and placement of spacer posts and to LC disclinations arising from the resulting fringing electric field at the pixel edges; electrical crosstalk between adjacent pixels; and index mismatching of the layers within the LC cell with the use of coherent illumination. Scattering, index mismatching, and three-dimensional effects appear to dominate the resolution-limited contrast in twisted nematic liquid crystal SLMs.

- Scattered light from irregularities in the cell can be reduced with improvements in via design, mirror design, metallurgy, and fabrication [11].
- The decision to use the normally black mode was fundamental to reducing the impact of three-

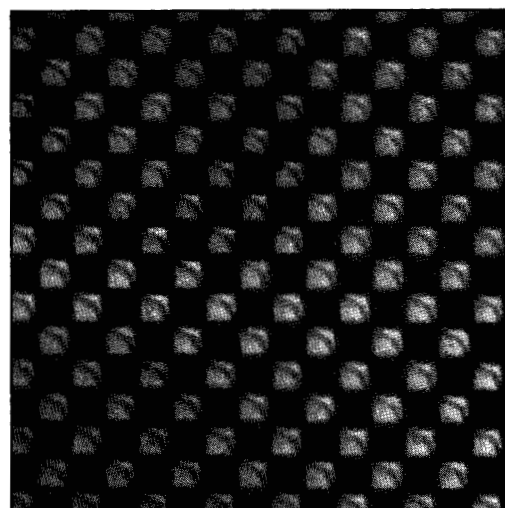


**Figure 5**

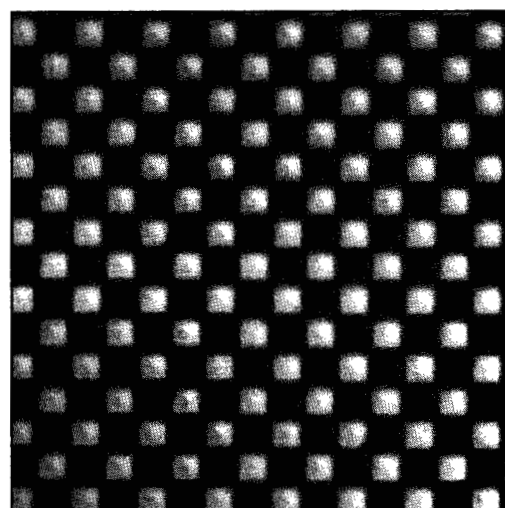
Deformed and tilted-state polarization-conversion efficiency as a function of voltage. The 54°-twisted reflectance is nearly 100% compared to 93% for the 45°-twisted case.

dimensional effects (disclinations) on the large-area contrast ratio. The disclinations affect the on-pixel brightness but not the off-pixel dark level. In addition, we have observed that the impact of disclinations on resolution-limited contrast is a function of the field difference between adjacent on and off pixels. Improvement in resolution-limited contrast has been obtained by driving all of the pixels in one frame with the same polarity and optimizing the off-pixel voltage to reduce the on-to-off-pixel voltage difference. Unlike displays, holographic storage is not sensitive to flicker, eliminating the need for row-, column-, or pixel-voltage polarity inversion. As a result, the zero electric field between pixels having the same optical state provided by frame inversion is used to eliminate the disclinations. As shown in **Figure 6**, if the off-pixel voltage is increased from 0  $V_{\text{RMS}}$  to 1.5  $V_{\text{RMS}}$ , the disclinations are reduced in size and move into the space between the mirrors. The disclinations are virtually eliminated while providing an improvement in the resolution-limited contrast.

To further understand and quantify the sources of scattered light, confocal microscopy [12] has been used. The confocal microscope provides very high-resolution images using a scanning laser and a linear CCD array. The very low numerical aperture of the system does not allow most of the scattered light to be detected. To first order, the point-by-point variation in intensity of the sum of images with and without a quarter-wave plate is due to absorption and scattering. Lasertech Model 1LM21 H confocal microscope images of a 45° TN SLM with and



(a)

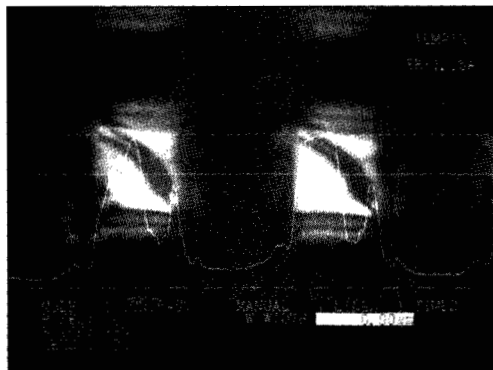


(b)

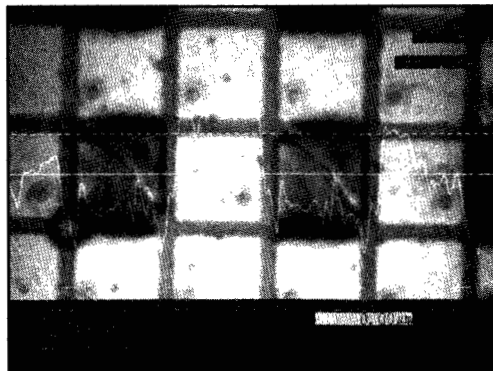
**Figure 6**

One-pixel checkerboard pattern shown with off-state voltages of (a) 0  $V_{\text{RMS}}$  and (b) 1.5  $V_{\text{RMS}}$ . The on-pixel disclinations are virtually eliminated and the image is 50% brighter in (b).

without a quarter-wave plate at best focus are shown in **Figure 7**. A repeated pattern having one pixel driven on at 3.1  $V_{\text{RMS}}$  with surrounding pixels driven at 0  $V_{\text{RMS}}$  is shown. The disclinations through the pixel and field-effect-illuminated regions around the pixel can be seen in the image without the quarter-wave plate. The via connecting the mirror and hillocks in the aluminum mirror surface are clearly shown in the quarter-wave-plate image. A bit-map-image-manipulation software program was used to



(a)



(b)

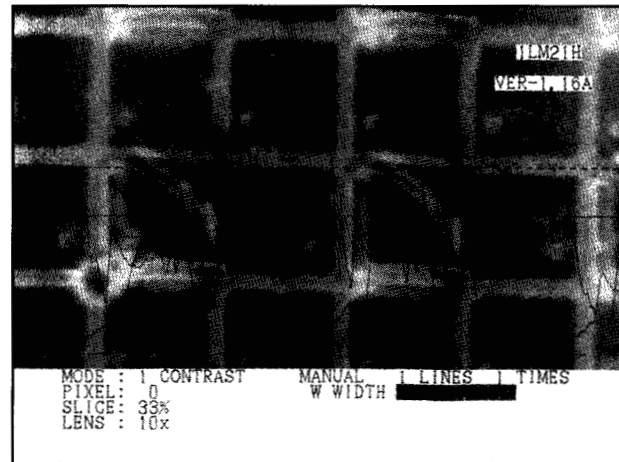
**Figure 7**

(a) Confocal microscope image of a  $3.1\text{-}V_{\text{RMS}}$  on pixel surrounded by  $0\text{-}V_{\text{RMS}}$  off pixels. (b) Same image but with a quarter-wave plate.

produce the scattered and absorbed light image in **Figure 8**. On an image point-by-point basis, the two images in **Figure 7** were added and the difference from maximum intensity obtained. The outline of the mirrors, disclinations, mirror via, mirror hillocks, and leading-edge rubbing-direction effects at the left and bottom edges of the on-pixels are seen as bright areas. The circular object visible in the lower left corner of the image is a spacer post used to control the cell gap. The edges of the spacer post also contribute to scattered light.

Pixel-to-pixel electrical crosstalk is not observed in our SLMs, apparently owing to the use of a fixed-potential-connected conductive light-absorbing layer just under the mirrors and a ground-connected substrate.

Initial characterization of  $45^\circ$ -twisted SLMs using coherent illumination revealed nonuniformity as high as 25%. Adding a broadband antireflection coating to the top glass virtually eliminated the interference of long-



**Figure 8**

Computed image showing scattered and absorbed light (lighter areas) using confocal microscope image with and without a quarter-wave plate. (See text for further discussion.)

coherence-length light that reflected off the SLM cover glass and the bottom surface of the polarizing beam splitter. However, 5% ringlike nonuniformity remained. A second source of interference was found to be a result of cell-gap variation. A spectral scan was performed on an unexcited  $45^\circ$ -twisted SLM using an analyzer parallel to the polarized incident illumination. It showed 10–20% intensity ripples with a peak-to-peak spacing of 7% of the wavelength. These are Fabry–Perot peaks arising within the SLM due to optical index mismatch at the LC/ITO interface. The ripple intensity was a minimum at about 550 nm, which corresponds to the half-wave design thickness of the ITO. Similarly, if the cell gap varies with a single wavelength, this is equivalent to a wavelength shift and can produce similar levels of nonuniformity. We performed an interference analysis as a function of wavelength and cell-gap variation. The optical path-difference analysis with wavelength gave  $\Delta\lambda = \lambda^2/(2nd) = 0.041 \mu\text{m}$  for interference for a cell gap  $d = 3 \mu\text{m}$ , wavelength  $\lambda = 0.6 \mu\text{m}$ , and LC index of refraction  $n = 1.5$ . This agrees well with the observed peak-to-peak ripple spacing observed. Similarly, interference occurs with a change in cell gap,  $\Delta d = \lambda/(2n)$ , or  $0.2 \mu\text{m}$ . The variation in cell gap corresponds to a 6.9% change in cell gap, which implies a need for cell-gap control of better than 3.5%. When voltage is applied to produce an on state, the effective LC index of refraction changes from 1.5 to 1.6, resulting in both  $\Delta\lambda$  and  $\Delta d$  values that are 6% lower. Improved cell-gap control to within the above tolerances has eliminated the remaining 5% nonuniformity.

### Switching times

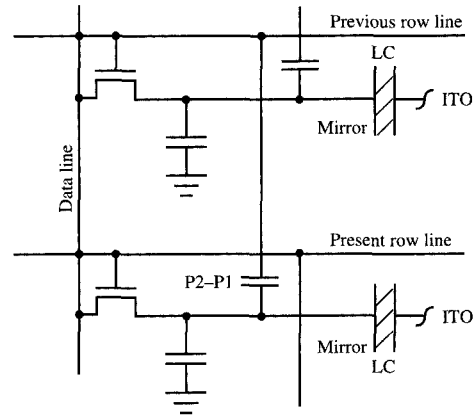
The LC switching time is also important since, along with the SLM addressing and exposure times, it determines the SLM image-writing rate. The 45°-twisted-angle TN LC mode was found to have a 0%–90% or 100%–10% response time of about 20 ms at room temperature. At present, this LC speed is consistent with the requirements of the holographic storage media, but with need in the future for higher writing speed, faster LC modes will be required. The TN LC switching speed increases with rising temperature, and LC-response-limited frame rates up to 100 Hz at 50°C appear possible with the 54° TN mode.

While other nematic LCs with faster switching times have been reported [13, 14], the fastest LC switching times are achieved with ferroelectric liquid crystal (FLC) materials [15]. Surface-stabilized FLC materials have binary optical states and high contrast, and do not have twisted nematic disclination-like structures. However, the submicron gaps for FLC cells are very difficult to fabricate. FLC is also difficult to drive with an ordinary active-matrix array, since the cell capacitor must provide the polarization charge for complete switching. The requirement for an inverted or complementary image for charge compensation requires that the illumination be shuttered off during the image-reversal period, which reduces the effective page-writing rate by half. Since higher-recording-speed materials do not exist at this time, these issues have not been fully addressed.

### Chip design

The fabrication technology used for the one-megapixel SLM is identical to the reflective liquid crystal light-valve-array technology developed for projection displays [16]. Unlike gray-scale-display light-valve designs, the design of an SLM suitable for holographic data storage uses only bilevel information. This simplifies the integration of both row and column drivers with the array. The potential for contrast, efficiency, speed, and uniformity in the LC is constrained by silicon technology voltage limits and pixel size requirements.

The technology used for fabricating the SLM chip was based upon a 1.2- $\mu\text{m}$ , 5-V CMOS process modified for 10 V and two levels of polysilicon. A 10-V gate driver was needed to write 0–6-V pixel voltages. A modified 0.8- $\mu\text{m}$  process was incorporated for the second- and third-level metal. The second-level metal was dedicated to absorbing light passing through the spacing between mirrors. The third-level metal was dedicated for the mirrors. This left only one level of metal for general-purpose wiring. The thin-film patterning of the chip fabrication produces nearly 1  $\mu\text{m}$  of bow in the chip. Patterned SiO<sub>2</sub> spacers were chosen for LC gap control for their strength and precise dimensional control. Design rules were also modified for 1 $\times$  lithography, which allowed the fabrication of large chips.

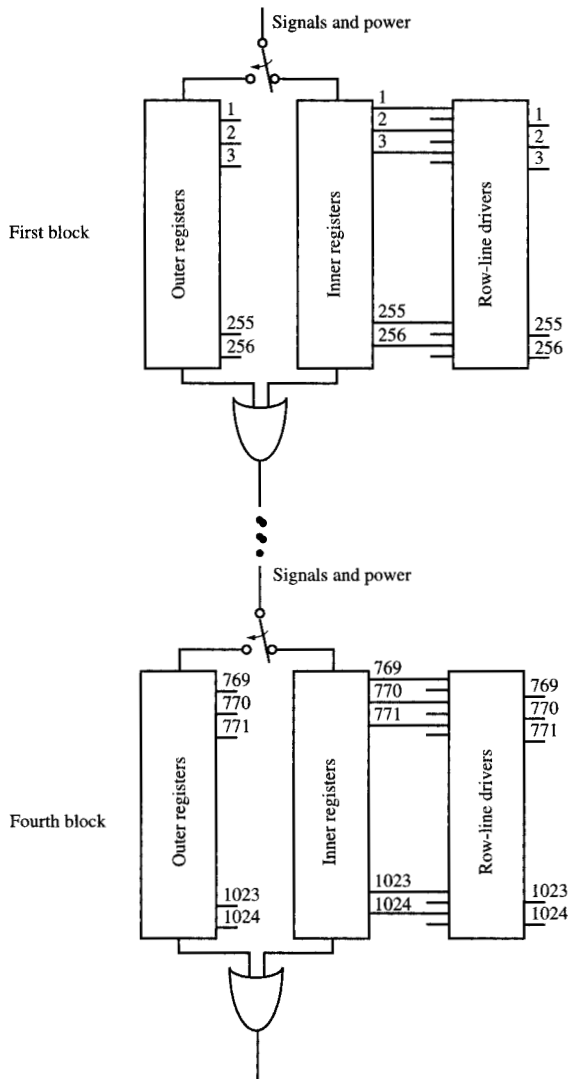


**Figure 9**

Equivalent pixel cell circuit consisting of an n-FET and two capacitors. The grounded capacitance is composed of stray and diffusion capacitance. The P2–P1 capacitor is a second-layer-polysilicon capacitance to the first-layer-polysilicon previous row line.

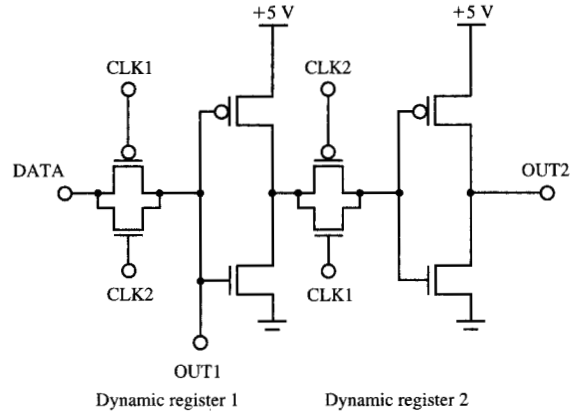
The holographic spatial light-modulator chip consists of an active-matrix array, row drivers at both the left and right sides of the array, and column drivers. In conventional active-matrix addressing, the rows are selected one at a time from top to bottom of the array. The data presented on the column lines are written in the pixels of the selected row. As shown in **Figure 9**, the active-matrix pixel circuit is essentially a DRAM circuit. It consists of a single n-FET transistor whose gate is connected to a row line. The source is connected to a data line and the drain is connected to the mirror electrode. Approximately half of the drain-connected storage capacitance is formed by coupling the second level of polysilicon to a first polysilicon layer that functions as the previous row line. The cell storage capacitance was estimated to be about 75 fF. The cell size was minimized, given the process ground rules. The resulting cell pitch was 15.6  $\mu\text{m}$ . Both row- and column-driver circuits were designed to match that cell pitch.

Row drivers drive both ends of each row to maximize the addressing rate using resistive polysilicon row lines. An improvement in line settling time by a factor of 4 is obtained by driving both ends. Redundancy was used in the row-selection data path. As shown in **Figure 10**, the row-driver circuit has four blocks of 256-row-selection circuitry. Each block has two groups of row-selection circuits. The inner group is used by default, but if it does not function, the outer group can be selected by grounding the appropriate input. The output of each



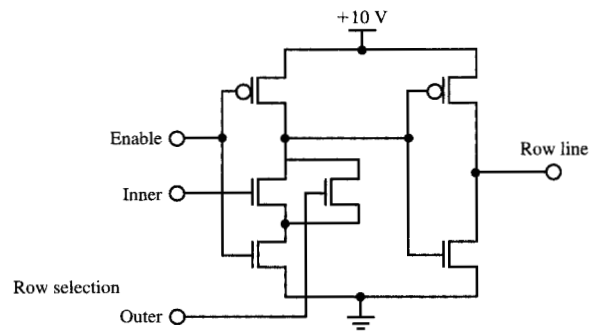
**Figure 10**

Overall arrangement of the row-driver circuitry. The row-selection circuitry consists of four 256-row-selection blocks, each containing an inner and outer group. The inner group is selected by default. An input signal can select the outer group if the inner group of registers fail.



**Figure 11**

The row-selection circuitry is composed of one dynamic register per row. The odd-row selection is achieved by using the inverter input of the dynamic register, while the even-row register output is the inverter output.



**Figure 12**

The row-line driver circuit is a clocked OR gate. The enable input provides the clocking function. When both enable input and either of the inner or outer row-selection inputs are high, the inverter input is pulled low, driving the row line high to 10 V. To pull the row line low, the enable input must be low.

group's row-selection data path is connected to an OR gate for signal propagation to the next block. One dynamic register is used for each row-selection circuit. The dynamic register consists of a complementary-clocked transmission gate for coupling data to an inverter. As shown in **Figure 11**, for odd-numbered rows, the inverter input is used for row-selection output, while for even rows, the inverter output is used. Use of the inverter input is possible if no other asynchronous transmission gates are

connected. Out-of-phase clock signals to the odd and even dynamic registers are used to shift the row-selection data. This arrangement inherently provides for row-line precharging, since row-selection data exist in two adjacent circuits.

The row-line driver circuit consists of an ENABLE-signal clocked-OR level-shifting circuit, as shown in **Figure 12**. The dynamic circuit relies on a low-level ENABLE signal to reset the circuit by pulling up the input

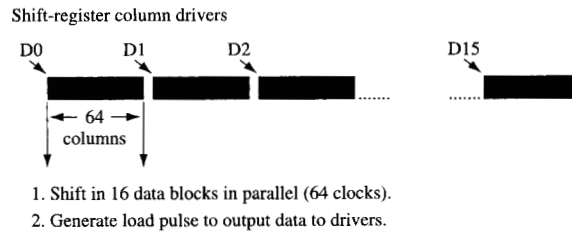


to the output inverter, thereby maintaining a low state on the row line. The high-level ENABLE state allows the row line to be driven high with a high row-selection input state. Edge control of two ENABLE signals, one for odd and one for even lines, allows control of row-line precharging and row-line turnoff.

The function of the column driver is to connect one of four reference voltages to the column line. Which reference is selected depends upon whether the data bit is logical 1 or 0 and whether the polarity input is 1 or 0. The overall organization of the row drivers is shown in **Figure 13**. Sixteen inputs provide data to sixteen 64-bit shift registers. Each bit in the 64-bit shift register provides data for an adjacent column line. The data-shifting direction is from left to right. To address 100 frames per second with data continuously supplied, a relatively low (6.5-MHz) clock rate is required. Two polarity-controlling inputs, each connecting only even- or odd-numbered columns, were incorporated to allow frame, row, column, or pixel inversion. **Figure 14** shows the data-driver circuit. The data shift register consists of two dynamic registers connected in series. Each dynamic register consists of a complementary transmission gate and an inverter. CK2 is the inversion of CK1. The data-loading register uses the same dynamic register design as that used in the data shift register. Both the input and the output of the inverter in the load register are used to drive transmission gates for the reference-selection circuitry. Two p-FET transistors are used for positive-reference selection, and the two n-FETs are used for negative-reference selection. If NPOL is high, the negative frame references are selected; otherwise, the positive frame references are selected. Two complementary transmission gates were used to connect the "on" (VN1 or VP1) or "off" (VP0 or VN0) reference to the data line.

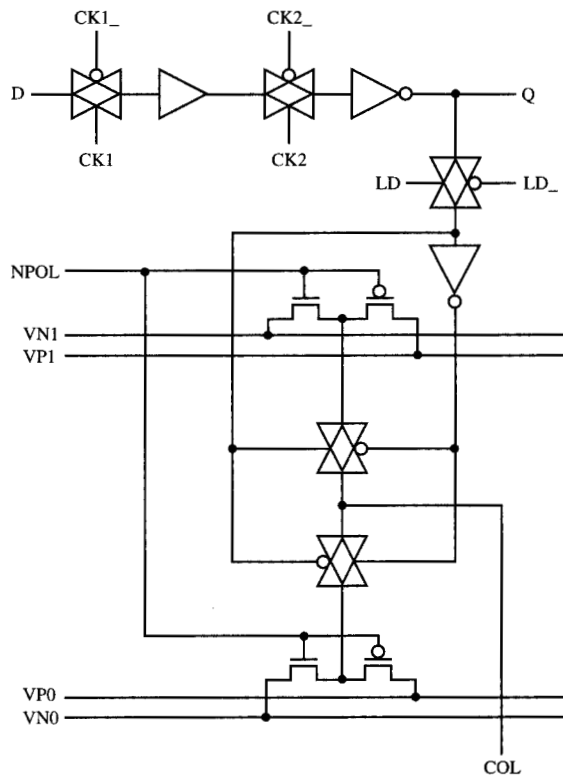
Simulations of the row-driver circuits driving the polysilicon row lines gave a worst-case row rise and fall time of approximately 1  $\mu$ s. The 0%-90% rise time and 100%-10% fall time at the ends of the row lines were each less than 100 ns. However, the row-line skew time, the end-to-middle row-line transition time difference, was approximately 1  $\mu$ s. Data-driver simulations show that the 0-7-V, 0%-90% rise time was also 1  $\mu$ s. Using just the rise time as the time needed for the LC voltage would not deliver the full RMS voltage to the pixel. The data-driver circuit takes nearly 3  $\mu$ s to settle to within 10 mV, which would be sufficient for 4-bit gray-level operation. However, such accuracy may not be needed in a binary holographic storage application. An error of 100 mV corresponding to 2  $\mu$ s may be acceptable. The data driver was simulated with 20-MHz clock rates.

If not limited by data-driver shift rates, the sum of row-line skew (1  $\mu$ s) and data-line settling time (2  $\mu$ s) times the number of rows (1024) determines the minimum



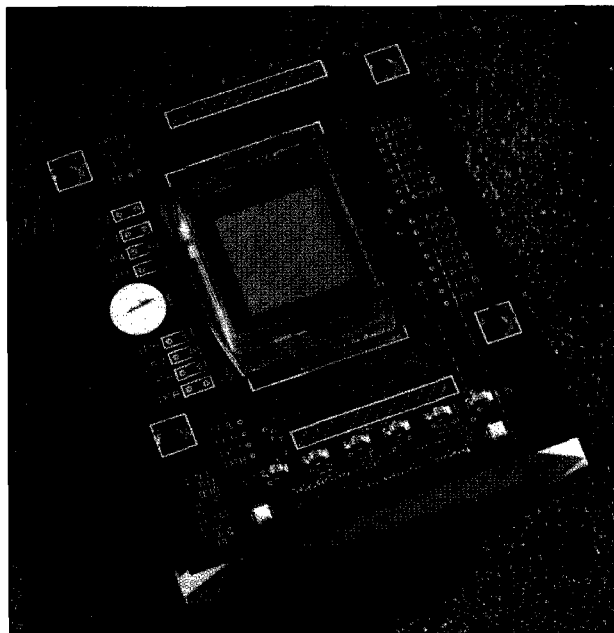
**Figure 13**

Diagram of data- or column-driver arrangement. The 16 groups of drivers have 64 adjacent drivers each. Data are shifted in from left to right and loaded to the column-driver output circuitry. Row addressing is incremented for writing to subsequent rows.



**Figure 14**

The integrated column-driver circuit consists of two dynamic registers forming a two-phase shift register; a dynamic register functioning as a holding latch; NPOL input-gate-driven transistors for positive (VP) or negative (VN) polarity reference selection; and two transmission gates for high (on or 1) and low (off or 0) state reference selection.



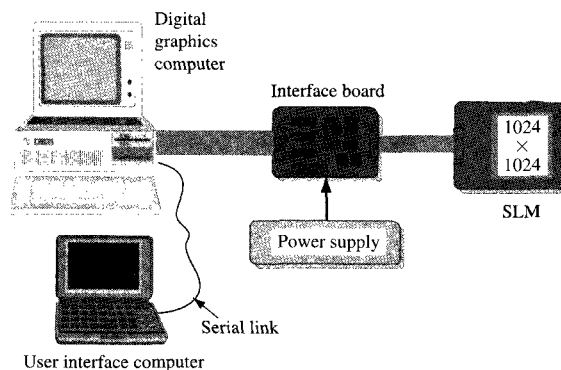
**Figure 15**

Photograph of the SLM card, in which epoxy is used to attach the SLM to a black anodized aluminum holder (not visible) held in place with screws. Wire bonds are used to connect the SLM chip to the card, and epoxy on the wire bonds is used for protection.

time (3.1 ms) required to address the array. The minimum address time provides a writing rate of about 300 frames per second using continuously clocked data at 20 MHz.

### Assembly and packaging

The LC cell process steps for the cover glass and silicon chip are, in sequence, inspection, cleaning, polyimide (PI) coating, PI pre-baking, PI final baking, buffing the PI films with a cotton cloth on a wheel, and cleaning. Peripheral sealant is then dispensed on the cover glass to form the surround for the LC cavity. The cover glass and the silicon chip are assembled into the LC cell with a bottom glass support for the silicon chip with a UV-curable glue between the support and the chip. Pressure is applied to the cover and bottom glass during curing. The cell gap is measured at the four corners and in the center by spectral interference [17]. The assembly is placed in a vacuum chamber for LC fill. The next step is the sealing of the injection hole with UV-curable glue. Afterward, cell-gap uniformity is checked using normally incident monochromatic light with a sheet polarizer placed on top of the cell and observing the fringes. One fringe corresponds to a variation in cell gap of about 0.2  $\mu\text{m}$ .



**Figure 16**

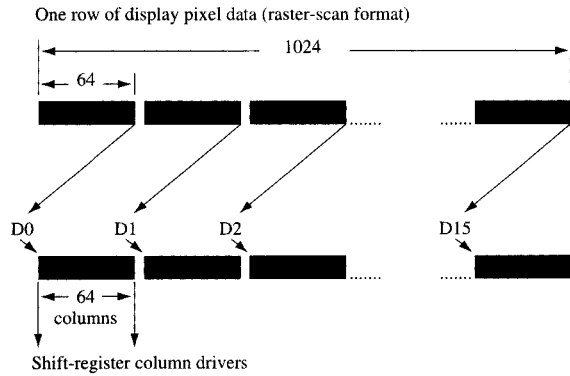
System configuration showing a remote-user-interface portable computer linked to a host computer via a serial link. The host computer has the digital and CRT-out display adapter and data-translation software running to supply data to the SLM in an appropriate manner.

Finally, the cell is tested as a function of applied voltage in which the reflected polarization conversion is measured with a photodiode.

The packaging of the SLM involves integrating the assembled liquid crystal cell onto an electronic card having a connector that is used for communication between an interface card and the SLM. The SLM is housed on an aluminum base assembly and anchored in place with a low-temperature-curing epoxy. This subassembly is attached to the card with four screws that have adequate clearance to permit the relative positioning of the card with respect to the SLM so that the wire-bonding pads on the two parts are aligned. The screws are then tightened to hold the pieces in alignment. The electrical connection between the silicon chip and the card is accomplished by wire bonding directly from the aluminum pads on the chip to gold-coated wire-bond pads on the card. This is the first example of a simplified light-valve or SLM package in which the SLM is directly connected to the gold-coated pads on the circuit board, eliminating the need for an intermediate flex circuit. **Figure 15** is a photograph of the packaged assembly. A black anodized aluminum frame and base plate serve not only to mechanically attach the SLM to the card but as a means to mount and align the SLM in an optical system.

### Data control and interface electronics

As shown in **Figure 16**, the approach for supplying data uses two computers; a remote-user-interface computer is connected by an RS-232 interface to a host PCI bus



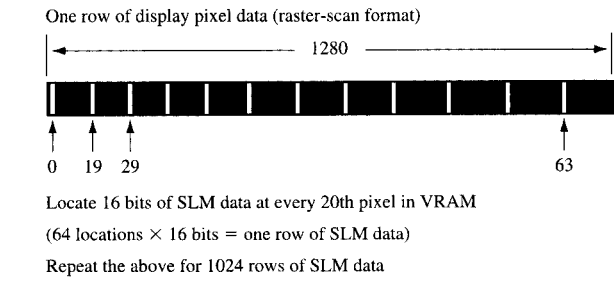
**Figure 17**

The 64th bit in each image block is translated to the first position in the frame-buffer image to account for the SLM data-driver data shifting direction.

computer with an SXGA graphics display adapter having both digital and analog outputs. A laptop running Visual Basic graphical user interface programs under Windows\*\* 3.1, 95, or NT was used as the remote computer. The display adapter software on the host computer runs from DOS and requires no other operating system. A host program was written to map or translate an SLM image into the frame-buffer image in the display adapter. This allows data to be written correctly to the SLM. The two-step process required that the proper 16 bits for the SLM data-driver inputs be extracted from the  $1024 \times 1024 \times 1$  SLM data image and positioned properly in the  $1280 \times 1024 \times 24$ -bit frame buffer for transfer. **Figure 17** shows that the left-to-right shift direction of the SLM column-driver data requires the data to be reversed in the frame buffer, since the frame-buffer contents are output in raster fashion from left to right. The 16 bits of SLM input data are remapped as a single 24-bit frame-buffer pixel. **Figure 18** illustrates that the SLM frame-buffer pixel data for one SLM row are separated every 20 frame-buffer pixels across the frame-buffer row. Reduction in the data separation has allowed encoding three and four SLM lines into a single frame-buffer line.

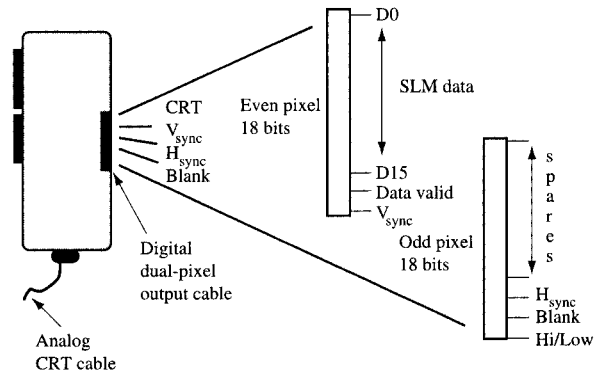
As shown in **Figure 19**, the digital output of the graphics card supplies dual, adjacent-color pixel data at 55 MHz. Only the even-pixel data outputs are used to provide data to the SLM. Each pixel output contains 24 bits of data; 16 are assigned as SLM data bits, two bits are used for the data-valid signal (providing clock edges for the SLM data) and SLM vertical sync, and the rest are unused. Two bits from the odd-pixel outputs are used for SLM horizontal sync and blanking. The third bit is

optional and is used for low- and high-speed addressing rates. Shown in **Figure 20** is the method used to provide two SLM data and timing-signal frames in the frame buffer. Each frame-buffer row provides three rows of SLM data. The SLM horizontal synchronizing signal (H) precedes each SLM data row, the SLM blanking signal (B) appears at the end of the frame buffer, and the SLM vertical sync signal is a full frame-buffer row preceding each frame of SLM data.



**Figure 18**

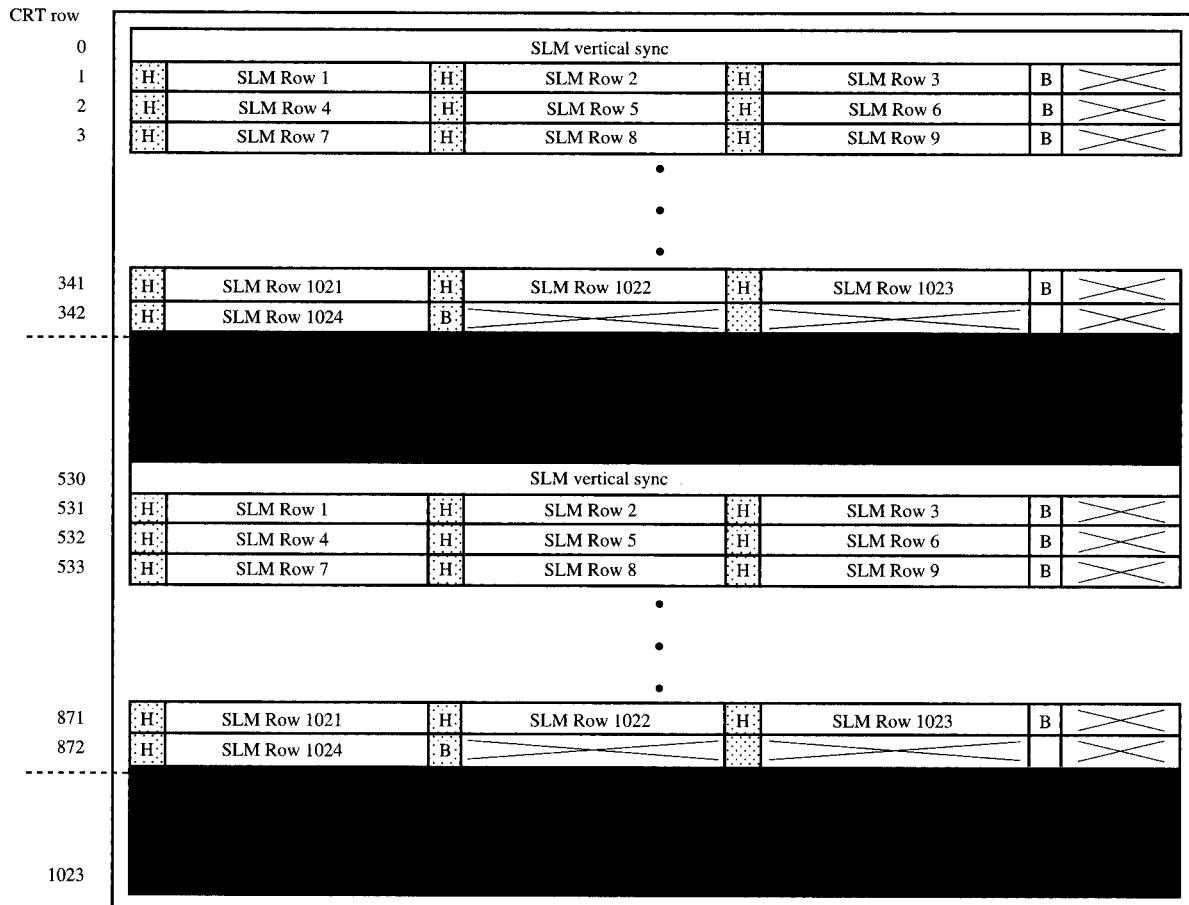
SLM data spacing relative to frame-buffer pixels for one SLM frame encoded into the frame buffer. The SLM pixel data are separated by 20 frame-buffer pixels.



**Figure 19**

Digital output of the display adapter card. Only even pixel-bit outputs are used with SLM pixel data. Four other signals are used for SLM timing. The Hi/Low signal is used here to indicate high- or low-speed SLM addressing.

An interface card between the display adapter and the SLM is needed to convert the SLM horizontal, vertical, and blanking signals into row-selection data, row-clock, row-enable, data-clock, data-load, and frame-polarity



**Figure 20**

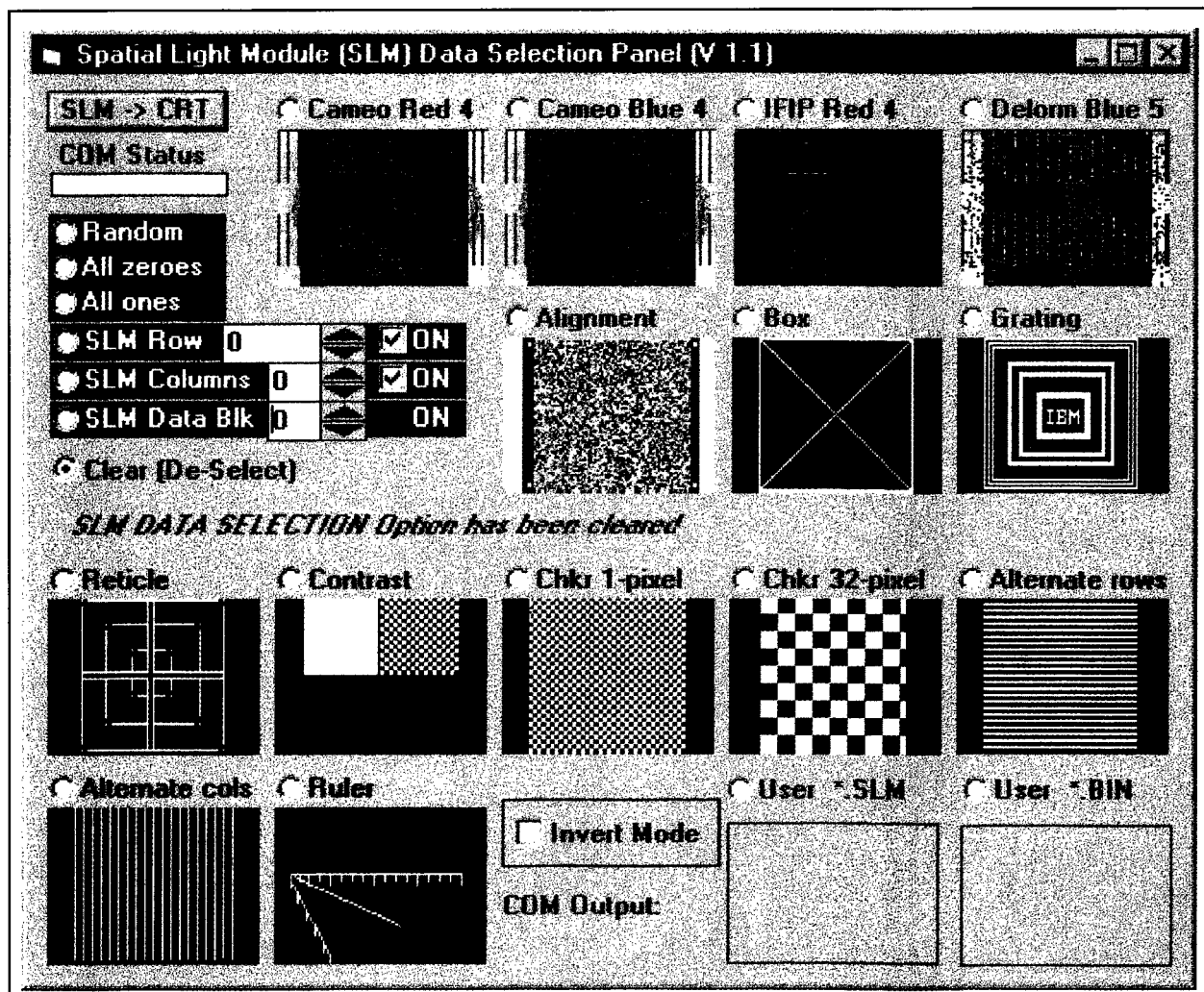
Method by which the SLM data and timing signals are written to the frame buffer of a PCI bus SXGA display adapter. The data for 16 SLM pixels are written to one 24-bit frame-buffer pixel. The SLM timing horizontal sync (H), vertical sync, and blanking (B) signals are interspersed.

signals. This is accomplished using a field-programmable gate array. A shutdown feature is provided to protect for over and under +5-V and +10-V input power. The interface card also contains the four reference voltages for the data drivers.

The remote-host graphical user interface consists of three screens. The first is the SLM User Interface, which is used to translate different image data types into a frame-buffer SLM data image. The second and most useful interface is the SLM Data Selection Panel, as shown in **Figure 21**. Most of the data-selection options were used for testing the SLM system. The user \*.SLM and \*.BIN options allow the user to specify lists of image files to be displayed. A third user interface panel is the SLM Pixel Write Utility for manually writing any arbitrary

pixel data pattern anywhere in the  $1024 \times 1024$  array, pixel by pixel.

The data translation software, graphical user interfaces, and an SLM interface card allow dynamic SLM verification with arbitrary images. With two SLM frames loaded into the frame buffer, an update of five different images per second has been demonstrated using a 90-MHz Pentium computer. With one SLM image loaded into the frame buffer, rates of 12 different images per second have been demonstrated. The rate is higher, since less information is written to the display adapter. However, since the frame-buffer writing process is asynchronous and does not take exactly an even number of frames, LC charge imbalance could occur. To avoid this, a 50% on/off-pixel data requirement over some predetermined

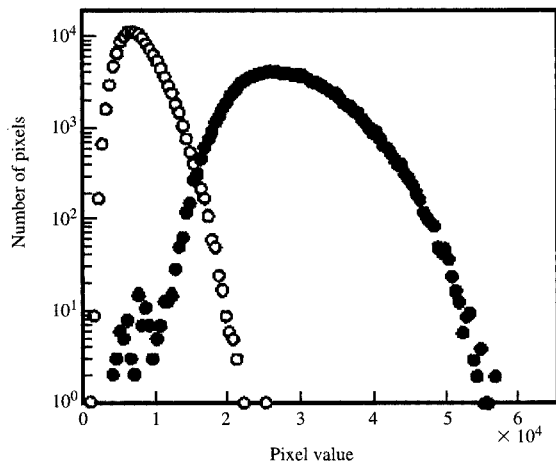


**Figure 21**

Graphical user interface developed for controlling data patterns to SLM. Sequential page patterns are obtained by selecting the User \*.SLM or \*.BIN buttons.

number of images would have to be encoded. This restriction can be circumvented by encoding two (one positive- and one negative-polarity) SLM frames into the frame buffer and updating both positive- and negative-polarity SLM pixel data simultaneously. Finally, three SLM frames were loaded into the frame buffer and were used to determine whether the SLM would function properly with a 180-Hz frame addressing rate and a 28-MHz data clock. If data could be provided continuously, the 28-MHz clock rate would correspond to an addressing rate of 430 frames per second. At this rate, nearly perfect images were obtained, but data chatter and data-driver block boundaries were observed.

This system is not limited to just encoding three SLM frames into the frame buffer. The SLM interface card can be modified to allow the odd-pixel spares in the adapter to be used for SLM data. If the data-valid signal edges were used, SLM data could be positioned on adjacent frame-buffer pixel positions. This would allow up to 12 SLM frames to be written for each frame image. The 12 SLM frames could comprise six separate images for a burst writing rate of 240 pages per second. However, the average page-writing rate is limited by being able to write only one byte at a time to the frame buffer and associated adapter card, and also by PC system clock rates.



**Figure 22**

Histogram of the CCD 16-bit digital output pixel value to a 256-kilobit data page, displayed on the SLM and pixel-matched to a CCD camera. Open circles denote off pixels; closed circles denote on pixels.

### CCD imaging test results

To test the suitability of the SLMs for holographic data storage, two SLM assemblies were viewed under conditions similar to those of a holographic storage system with a pixel-matched CCD camera. The collimated beam from an argon-ion laser (514 nm) illuminated the SLMs through a polarizing beam-splitting cube, which served as both polarizer and analyzer, and the light transmitted through the analyzer was imaged onto a CCD camera with  $1536 \times 1024$  pixels, a 100% pixel fill factor, and 16-bit gray-scale resolution. Because the pixel pitch of the CCD ( $9 \mu\text{m}$ ) did not match that of the SLM, a commercial photographic macro lens ( $f = 60 \text{ mm}$ , aperture  $f/2.8$ ) was used to demagnify the SLM image by a factor of 15.6/9, so that each SLM pixel was imaged onto one CCD pixel. In principle, this approach allows the inspection of the entire SLM in one operation. By applying various test patterns, it is possible to characterize response uniformity and contrast at all spatial frequencies. In this experiment, the use of an off-the-shelf objective lens limited the performance of the test system: The observed uniformity and point-spread function were degraded because of vignetting in the lens and uncompensated spherical aberration introduced by the beam-splitting cube. Also, the optical magnification was adjusted to an accuracy of only about 0.05%, or one quarter of a pixel. With custom optics and careful optomechanical design, it is possible to achieve considerably more accurate pixel matching

and more uniform illumination [18]. Hence, these measurements represent a lower limit for the performance of which the SLM is capable.

Despite the limitations of the optics, it was possible to show that the performance of the SLMs at high spatial frequencies was adequate to encode binary data for holographic storage. To minimize the impact of the imperfections in the viewing optics, and to avoid a few defective pixels on the SLMs, data patterns were programmed in a  $512 \times 512$ -pixel region at the center of the SLMs. This represents an error of about one tenth of a pixel, assuming perfect alignment of the SLM pixels to the CCD pixels. Restricting the measurements to a  $512 \times 512$ -pixel region in this test setup is representative of an actual recording system having registration to one tenth of a pixel. **Figure 22** shows the response of the CCD camera to a data pattern encoded using a balanced modulation code [19] and a Reed-Solomon error-correcting code. Comparable results were obtained for both of the tested SLMs. Ideally, the CCD pixels viewing "on" SLM pixels (closed circles) would see a uniformly high light level, while those viewing "off" SLM pixels (open circles) would see a uniformly low light level. In reality, finite SLM contrast, optical imperfections, misalignment, and diffraction all act to broaden the ideal response. Where the on and off distributions overlap, the input data cannot be reconstructed on the basis of CCD response alone; this applies to 0.8% of the pixels in **Figure 22**. However, by using the information in the modulation and error-correcting codes, the original data could be recovered without any errors.

### Concluding remarks

A one-megapixel SLM specifically designed for the holographic storage application has been designed and built. The writing capability of the reflective SLM produced bit-error-free CCD images using error-correction and modulation codes. Special antireflection coatings and cell-gap control of better than  $0.1 \mu\text{m}$  are needed to minimize interference using coherent monochromatic illumination. Adequate (4:1) resolution-limited contrast has been achieved by using frame inversion and minimizing the on-to-off-state voltage difference. While the  $54^\circ$  TN LC response speed is only about 20 ms, present holographic material recording rates are even slower. Data were clocked into the SLM at an equivalent rate of 300 frames per second. A system providing SLM data using a display adapter and an interface card was used to write arbitrary data to the SLM. SLM page-writing rates of up to 12 pages per second were demonstrated, which is also about the maximum page-writing rate for iron-doped  $\text{LiNbO}_3$ .

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