Aluminum-based gate structure for active-matrix liquid crystal displays

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This paper describes the development of an Al-based thin-film gate structure for use in large, high-resolution active-matrix liquid crystal displays (AMLCDs). Aluminum films are suitable for forming the data lines of such displays, but they are not suitable for forming the gate lines because of the hillock-induced shorts that can occur to overlying metal lines during the heating necessary for insulator deposition. Alloying with yttrium, gadolinium, and neodymium was examined with the aim of reducing hillock and whisker formation during such heating. Although Al films alloyed with 2 at.% of those metals exhibited low hillock densities (10–100 mm^{-2}), the densities were not low enough for the fabrication of SXGA (1280 × 1024 pixels) panels. After investigation of several means to further reduce the formation of hillocks and whiskers, the most effective approach was found to be anodization of the Al-alloy gate lines, suitably patterned for anodization, followed by photoresist application and laser-cutting steps. Illustratively, by use of an anodized Al–Nd (2 at.%) thin-film gate structure, the short-circuit defect rate and contact defect rate for an 11.3-in.-diagonal experimental SVGA (800 × 600 pixels) display could be effectively reduced to zero.

Introduction

Thin-film transistors having an inverted structure (gate beneath) have been studied extensively because of their use in active-matrix liquid crystal displays (AMLCDs) [1, 2]. In the 1990s, the panel size and resolution of AMLCDs were increased dramatically, and much effort was devoted to developing low-resistivity gate lines [3–6]. The aperture of displays with resolutions higher than SXGA has been significantly reduced by the use of gate alloys such as molybdenum–tantalum or molybdenum–tungsten. To achieve this, low-resistivity films are required (see **Table 1**). As shown in **Figure 1**, the use of a conventional MoW alloy with a resistivity of 16.5 $\mu\Omega$-cm results in an aperture ratio of less than 30% for a 12–15-in.-diagonal panel. This is unacceptable for a mobile computer display, because a small aperture requires a bright backlight and consumes a large amount of battery power. On the other hand, the use of an aluminum alloy film with a resistivity of 6 $\mu\Omega$-cm results in an aperture of more than 50% for a

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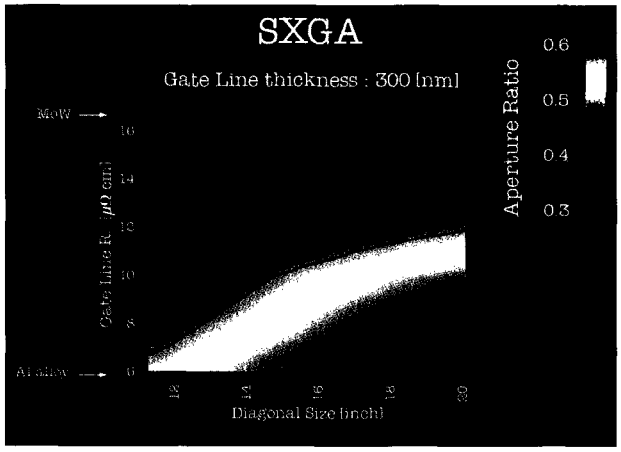


Figure 1

Relation between the aperture ratio and resistivity of gate lines in an SXGA panel. In each case, the thickness of the lines is 300 nm.

Table 1 Resistivities of some alloy films and metals.

	Resistivity ($\mu\Omega$-cm)
MoTa films	40
MoW films	16.5
Al-alloy films (alloyed with a rare-earth metal)	4–6 (after some annealing)
Al (bulk)	3.0
Cu (bulk)	2.0

12–15-in.-diagonal panel. Copper films have a lower (down to 2 $\mu\Omega$-cm) resistivity, but their adhesion to substrates is poor and such films are difficult to pattern with a tapered edge [4]. A tapered edge is important to ensure that the gate lines are properly covered by the gate insulator, protected from etchants, and isolated from overlying metal lines.

Al films are remarkably good for fabricating gate lines because of their low resistivity, low cost, high adhesion, and superior patternability. However, the thermal expansion mismatch between Al films and the glass substrate of display panels produces a large compressive stress in the Al films upon heating, and results in the formation of hillocks [7] or whiskers [8] in order to relieve the stress. Hillocks and whiskers can form during the heating associated with subsequent chemical vapor deposition (CVD) of insulating layers. Thus, if Al films are used to form gate lines, resulting shorting and leakage may occur between the gate lines and upper data lines.

To reduce hillock and whisker formation, use has been made of anodization [3], capping with refractory metals [6], and alloying [8–16]. We have found that anodization can adequately suppress the formation of hillocks and whiskers, but it requires the use of several additional processing steps. Capping with a metal such as Mo requires essentially no additional process steps, but it cannot suppress the formation of hillocks and whiskers on the sidewalls of the gate lines.

Preparation of samples

In this work, hillock and whisker studies were carried out using Al films alloyed with yttrium (Y), gadolinium (Gd), and neodymium (Nd). Previously, the alloying of Al with such rare-earth metals had been widely studied with the aim of controlling the formation of hillocks and whiskers under thermal stressing [6, 11–15]. Our films were deposited by sputtering on 5-in.-square LCD-grade glass substrates. Films having a range of compositions (0–2 at.%) were deposited at an argon pressure of 0.4 Pa and a substrate temperature of 150°C by means of a dc magnetron sputtering apparatus. Al–Y and Al–Gd films were sputtered from a composite target, while Al–Nd films were sputtered from an alloy target. The thicknesses of the Al–Y and Al–Gd films were 400–450 nm, and the thicknesses of the Al–Nd films were 250–300 nm. Annealing was carried out at 350°C in a nitrogen atmosphere for 20–60 min. The density of hillocks and whiskers was estimated by inspection over sample areas of 0.001–1 mm^2.

The breakdown voltage of insulators on gate lines was studied using Al–Nd-alloy gate lines that were either capped with Mo or anodized. Films having a nominal Nd composition of 2 at.% were deposited on 300 × 400-mm^2 LCD-grade glass substrates from an alloy target, at an argon pressure of 0.4 Pa and a substrate temperature of 150°C by means of dc magnetron sputtering. In the Mo-capped structure, 200 nm of Al–Nd alloy and 50 nm of Mo were sputtered and patterned into lines. In this process, Mo was used to taper the edge of the Al–Nd [16]. According to this taper-etching method, a taper angle of 20–35° was obtained. Each line had a total length of 90 mm and a width of 9–18 μm. SiO_x was then deposited on the Mo-capped lines to a thickness of 350 nm by CVD at a temperature of 330°C, and an upper electrode was formed.

In the anodized structure, the Al–Nd films were 350 nm thick and patterned into lines. In that case, the Al–Nd were not tapered because their edges become rounded upon anodization. The line pattern used was the same as that used for the Mo-capped structure. The alloy was then anodized at a voltage of 150 V for 18 min in an electrolyte consisting of a mixture of 3.68 wt.% ammonium tartrate solution and ethylene glycol, producing a 200-nm-thick layer of Al_2O_3. To cause the capacitance of the gate

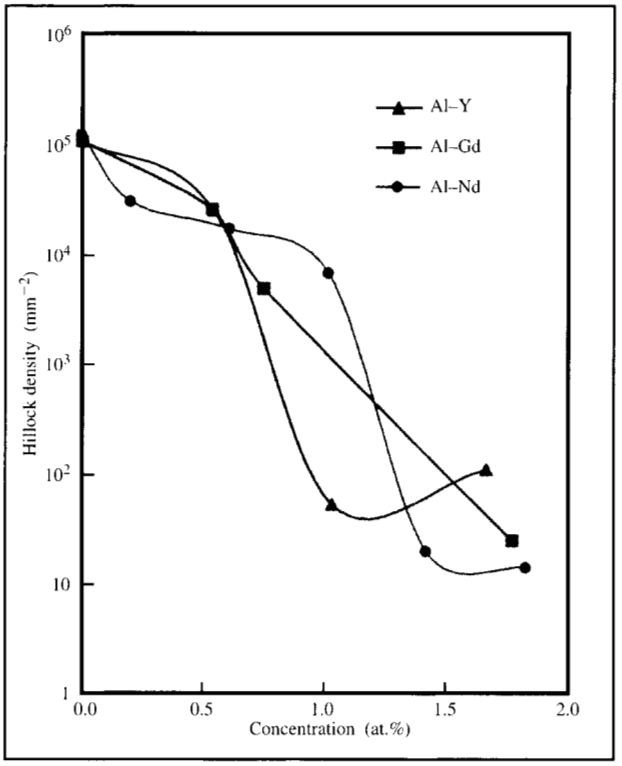


Figure 2

Hillock densities of Al-alloy films after annealing at 350°C in a N_2 atmosphere for 60 min. Their thicknesses were as follows: 400–500 nm for the Al–Y and Al–Gd films; 250–300 nm for the Al–Nd films.

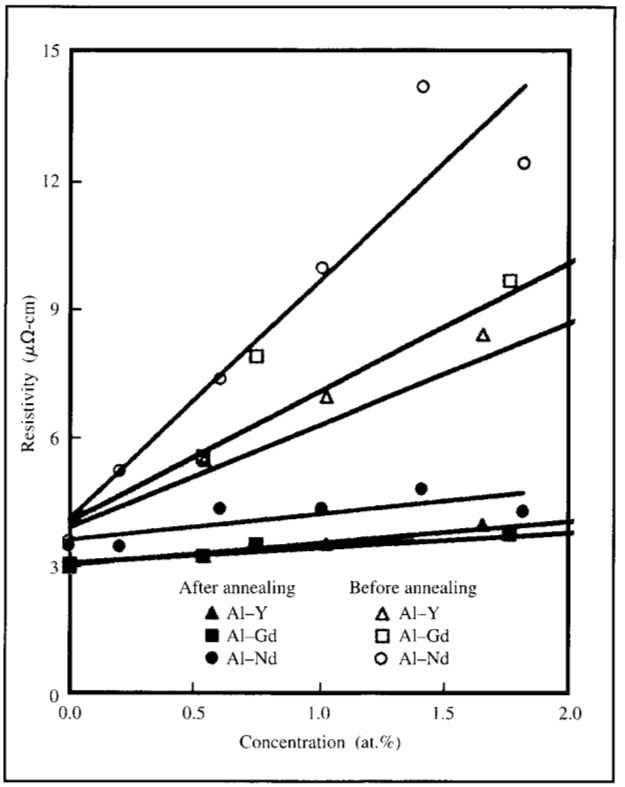


Figure 3

Resistivities of Al-alloy films before and after annealing at 350°C in a N_2 atmosphere for 20–60 min. Their thicknesses were as in Figure 2.

insulator to be equal to that of a 350-nm-thick SiO_x layer, SiN_x was then deposited on the Al_2O_3/Al–Nd lines to a depth of 300 nm by CVD at a temperature of 330°C, and an upper electrode was formed.

Thin-film and gate-structure studies

The hillock density observed after annealing at 350°C for 60 min is shown in **Figure 2**. The density was examined for concentrations of alloying elements ranging from 0 (pure Al) to 2 at.%. As indicated in the figure, it could be decreased significantly by the addition of about 1 at.% of a rare-earth metal. The suppression of hillock and whisker formation has been attributed to 1) a reduction of the thermally induced stress in the alloy films as a result of grain growth and the formation of intermetallic, second-phase precipitates, and 2) a reduction in the self-diffusion of the matrix Al in the films because of the presence of such precipitates at grain boundaries. The hillock densities of Al–Nd films were probably lower because they were slightly thinner than the other types [17].

Figure 3 shows the resistivity as a function of the concentration of alloying elements. The resistivities of annealed and as-deposited samples are shown. Note that the resistivities of the annealed samples were markedly lower than those of the as-deposited samples, which indicates that thermal processes such as CVD deposition at a temperature of 350°C can effectively reduce the resistivity of the as-deposited films. This decrease in resistivity is attributed to grain growth and the associated segregation of the alloying elements in second-phase precipitates at the grain boundaries. The Al–Nd film is seen to have a higher resistivity than the Al-Y or Al–Gd films. This is because the Al–Nd films were obtained by sputtering from an alloy target containing 920 ppm of oxygen and because they were thinner than the other films. At rare-earth concentrations of 1–2 at.%, the resistivity of the films could be reduced to 4–6 $\mu\Omega$-cm after annealing at 350°C. This resistivity is adequate for fabrication of AMLCDs with a higher resolution than an SXGA display.

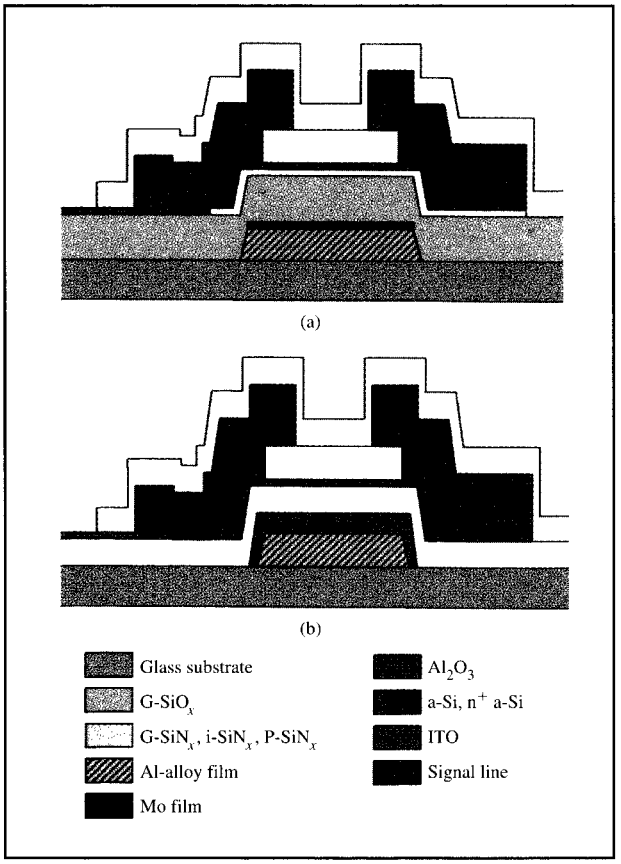


Figure 4

Cross sections of thin-film transistors containing two Al-alloy gate structures: (a) Mo-capped; (b) anodized.

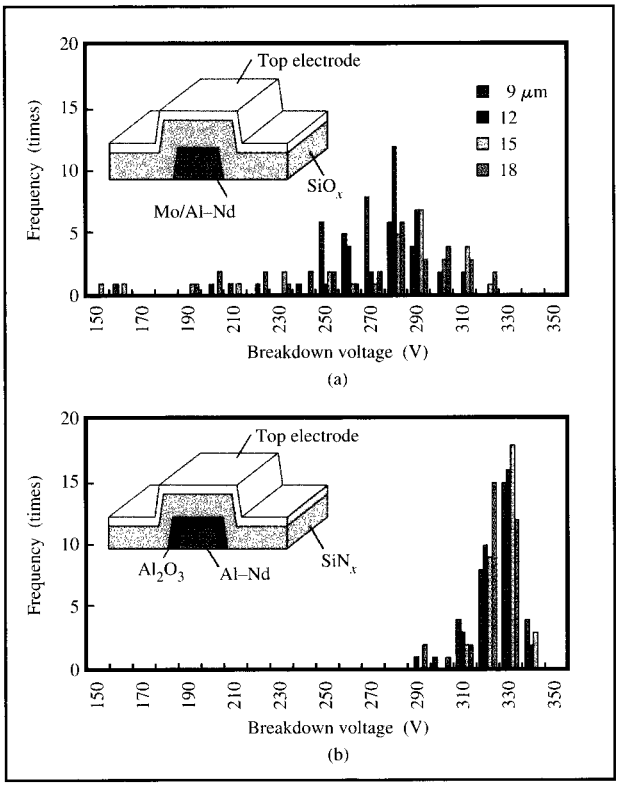


Figure 5

(a) Breakdown voltages in Mo-capped Al–Nd (2 at.%) insulated gate structure. The gate insulator was 350-nm-thick SiO$_x$. (b) Breakdown voltages in a gate structure containing anodized Al–Nd (2 at.%) gate metal. In the latter case, gate insulation was achieved using 300-nm-thick SiN$_x$ and 200-nm-thick Al$_2$O$_3$.

At a concentration of 1–2 at.%, the hillock density was found to be 10–100 mm^{-2} for each type of film. However, a hillock density of 10 mm^{-2} can cause more than 20 short-circuit defects in SXGA panels (assuming that each hillock causes a defect). This indicates that the hillock density levels of these Al-alloy films would not be low enough for the fabrication of high-resolution AMLCDs.

We have studied two gate structures to explore whether a further improvement could be achieved. This was done by measuring the breakdown voltage of the overlying insulator. Use was made of a Mo-capped Al–Nd gate structure and an anodized Al–Nd gate structure, both shown in **Figure 4**.

Breakdown voltages were measured by means of a curve tracer (Tektronix K213). Clearly, the breakdown voltage is a key indicator of the insulating efficiency of insulators on the gate lines and the defect rate due to short circuits between gate lines and data lines. The voltages applied to the Al–Nd gate lines were increased from 0 V to breakdown at a rate of 100 V/s. Measured values obtained are shown in **Figure 5**. The concentration of the alloying element was determined to be 2 at.% from the previous results. (Associated hillock densities and resistivities at a concentration of 2 at.% are shown in **Table 2**.)

Table 2 Hillock densities and resistivities of Al-alloy films at a concentration of 2 at.% after annealing at 350°C for 20–60 min.

	Hillock density (mm^{-2})	*Resistivity* ($\mu\Omega$-cm)
Al	10^5	3.0
Al–Y	10^2	4–5
Al–Gd	10^1–10^2	4–5
Al–Nd	10^1	4–6

In the case of the Mo-capped structure, SiO$_x$ deposited by CVD at a substrate temperature of 330°C was used as

the gate insulator. As indicated previously, the edges of the Al–Nd gate lines were tapered using Mo [16]. The formation of such a tapered edge was found to be important in ensuring adequate coverage by the overlying CVD films of SiO_x and the continuity of subsequent conductive layers.

The range of breakdown voltages was relatively wide (150–320 V), with the minimum voltage being about half the average voltage [Figure 5(a)]. By comparison, the range of breakdown voltages for a conventional MoW gate structure is 240–340 V. (This result is not shown in Figure 5.) The formation of hillocks and whiskers is considered to be affected by line width as well as film thickness. Accordingly, we examined 9–18-μm-wide lines, but the breakdown voltages were not found to vary. This implied that the hillock and whisker growth occurred mainly at the line edges—to which the Mo capping did not extend. That observation was consistent with a microscopic observation indicating that breakdown occurred mainly at the line edges.

In the case of the anodized aluminum structure, Al_2O_3 and SiN_x were used as gate insulators. The former was formed by anodic oxidation at room temperature, and the latter was deposited by CVD at a temperature of 330°C. The insulating ability of the anodized film was high [18]. As mentioned previously, in this case, the edges of the Al–Nd gate lines were not tapered because they became rounded upon anodization. The coverage by the subsequent CVD films was found to be adequate [3].

SiN_x was used as a gate insulator instead of SiO_x because it is known that the interface of amorphous silicon (a-Si:H)/SiN_x is better than that of a-Si:H/SiO_x [19]. In the case of the Mo-capped structure, we used an additional 50-nm-thick SiN_x layer beneath the amorphous silicon layer (see Figure 4). The breakdown field of Al_2O_3 (7 MV/cm) is almost equal to that of CVD insulators such as SiO_x (6 MV/cm) or SiN_x (8 MV/cm), and the corresponding pinhole density is 1–2 orders of magnitude lower than that of CVD insulators [18]. The breakdown voltage of the anodized Al–Nd gate structure was found to be appreciably higher than that of the Mo-capped Al–Nd structure, and its range (290–340 V) was found to be narrow [Figure 5(b)].

In the future, AMLCDs must provide higher resolution, and hence will require insulators having a high breakdown voltage. The anodized gate structure may therefore be advantageous for such AMLCDs.

Novel process for aluminum anodization

The anodic oxidation process used for forming the anodized gate structure has the disadvantage of requiring some additional process steps (**Figure 6**). In these processes, the photoresist acts as a mask for the contact holes, and the masked area is not oxidized during anodization. This resist is necessary because selective etching of Al_2O_3/Al is very difficult. To simplify these processes, we have developed a novel process in which use is made of a resist dispenser (**Figure 7**) that eliminates two steps and keeps production cost low. This dispensing process has further merits. One is that since resist development is not required, there is no developer-related damage to the Al alloy during development. The other

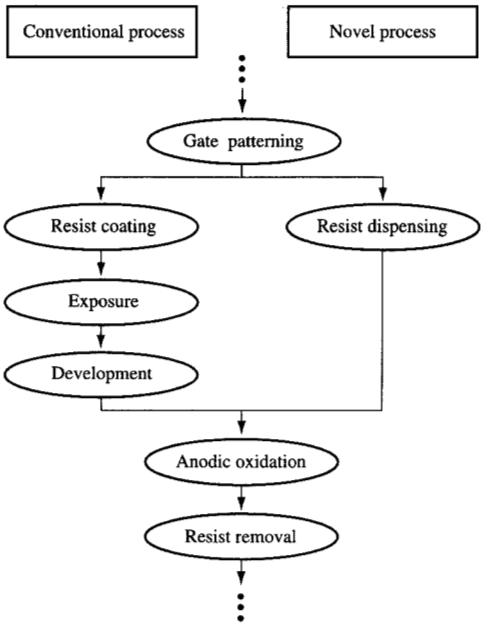


Figure 6

Comparative process flow for conventional vs. novel anodization process.

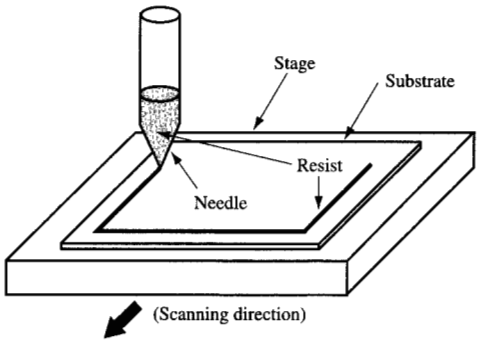
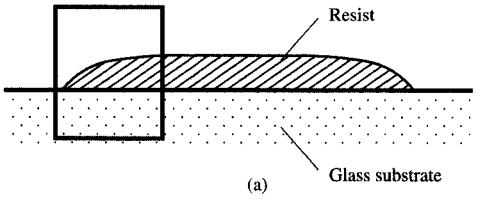
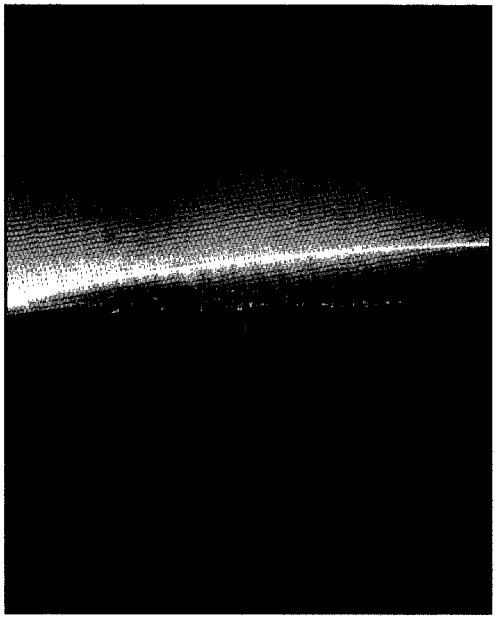


Figure 7

Schematic of resist dispenser.



(a)



(b)

Figure 8

(a) Schematic cross-sectional view of dispensed resist. (b) SEM micrograph corresponding to the micrograph indicated by the rectangle in part (a).

is that a greater resist thickness may be used than the approximately 1.5 μm which is usually required. For the latter thickness, resist peeling occurs if the voltage used for the anodic oxidation is increased. This peeling causes contact defects, but it can be avoided by increasing the resist thickness. In the usual exposure process, the use of a thick resist requires a long exposure time, resulting in poor productivity. In the dispensing process, the resist thickness can easily be increased by controlling the dispensing amount of the resist.

Accordingly, we have used a resist thickness of more than 2.0 μm and have thereby avoided the occurrence of contact defects. **Figure 8(a)** shows a schematic cross-sectional view of the dispensed resist, and **Figure 8(b)** shows an illustrative SEM cross-sectional micrograph corresponding to the location indicated by the rectangle

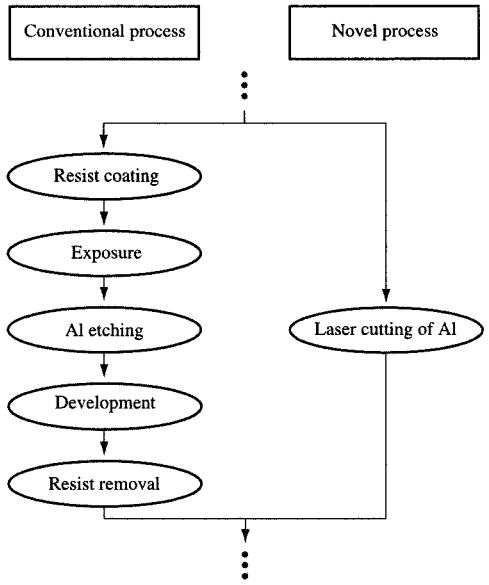


Figure 9

Process flow for gate-metal cutting.

in Figure 8(a). The edge of the resist was finely tapered, and its thickness was about 4.5 μm.

In the fabrication of AMLCDs, it is important to remove defective panels during fabrication in order to reduce production costs. After thin-film-transistor (TFT) fabrication, all of the pixels of a panel are tested with an array tester, and all of its defective lines and pixels are identified [20]. For anodic oxidation, the gate lines must be electrically connected so that a voltage can be applied to all of the lines. However, array testing requires that the lines be isolated to determine the addresses of defective lines and pixels. To isolate each line, many additional processes are currently required (**Figure 9**). As an alternative, we have developed a laser cutting process that allows the aluminum lines to be isolated.

Illustratively, **Figure 10(a)** shows gate lines cut for an array tester, with contact holes above them, and **Figure 10(b)** shows a schematic cross-sectional view corresponding to the position indicated by the "laser-cut area" region in Figure 10(a).

In this approach, resist is dispensed across the gate lines, and contact holes are formed on them. The gate lines are then cut with a laser to permit array testing of individual TFTs. All of the lines are cut concurrently, because too much time would be required to cut them selectively. The cut lines are reconnected by the data-line metallization through contact holes, if necessary. The

length of the contact area was designed to be longer than 50 μm so that contact defects would not occur if a small area of resist were to be peeled off. Use of the relatively thick resist layer and long contact regions reduces the occurrence of contact defects. With this design, resist-peeling defects have not occurred even at an anodizing voltage as high as 112 V.

Application to SVGA panels

We have fabricated two types of experimental 11.3-in.-diagonal SVGA panels in order to evaluate the structures described in this paper: One type contained a Mo-capped Al–Nd gate structure and the other an anodized Al–Nd gate structure. The I_D–V_G characteristics of the resulting a-Si:H TFTs are shown in **Figure 11**. The threshold voltages and field-effect mobilities obtained were, respectively, 3.6 V and 0.64 cm^2/V-s for the Mo-capped structure, and 2.1 V and 0.70 cm^2/V-s for the anodized structure. The difference in the two characteristics was due to the difference in the gate insulators. For the Mo-capped structure, the short-circuit defect rate was nearly equal to that of a panel containing a conventional MoW gate structure. For the anodized gate structure, the short-circuit defect rate and contact defect rate were each effectively zero.

Summary

The hillock and whisker densities of Al–Y, Al–Gd, and Al–Nd thin films (having concentrations of 0–2 at.%) were examined after heating to 350°C for 60 min. Hillock densities down to 10–100 mm^{-2} were achieved at the 2-at.% level. The following aluminum-based gate structures were fabricated and evaluated: a Mo-capped Al–Nd (2 at.%) thin-film gate structure and an anodized Al–Nd (2 at.%) thin-film gate structure. The latter was found to be superior with regard to breakdown voltage. To further decrease the defect rate and minimize the number of fabrication steps, a novel anodic oxidation process was developed in which use was made of a resist-dispensing step and a laser-cutting step. Using Al–Nd (2 at.%) gate lines and the anodization-related approach, we were able to fabricate 11.3-in.-diagonal experimental panels having a short-circuit defect rate and contact defect rate that were each effectively zero.

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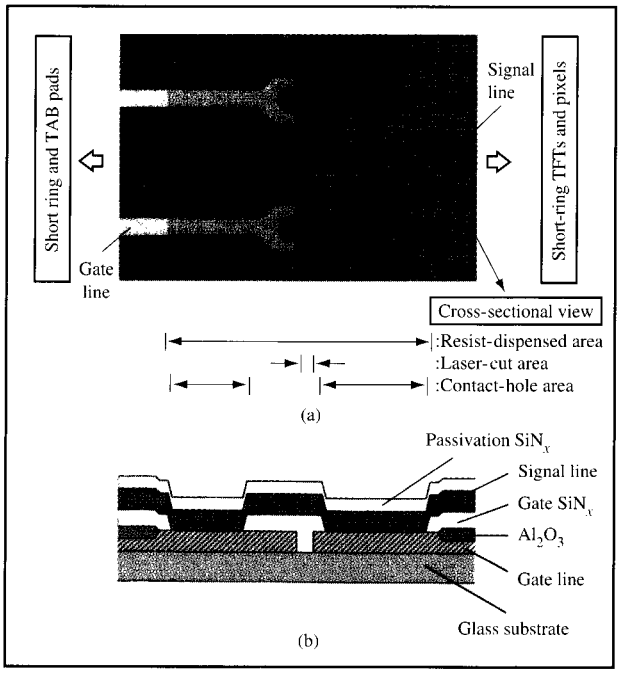

Figure 10

(a) Photograph of gate lines with resist-dispensed area, laser-cut area, and contact-hole area in close proximity. (b) Schematic cross-sectional view corresponding to location indicated by "Laser-cut area" designation in part (a).

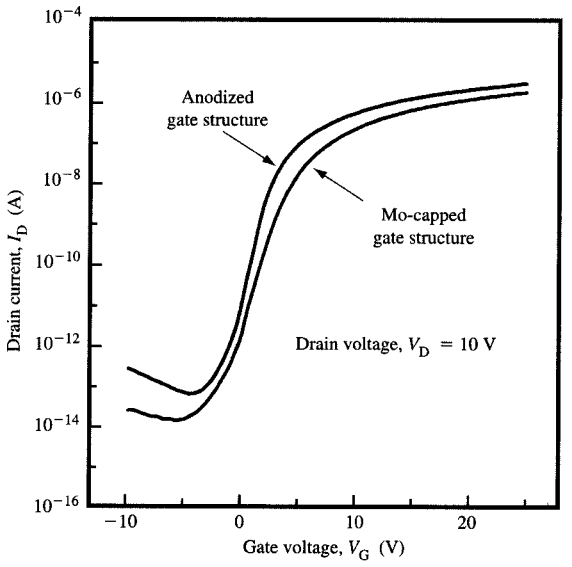

Figure 11

I_D–V_G characteristics of a-Si:H TFTs with Mo-capped Al–Nd gate structure and anodized Al–Nd gate structure.

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