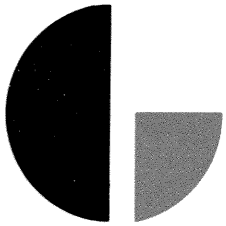

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TECHNICAL MANUAL

FOR THE

SUPERNOVA

DGC-TP-S39-41-02

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SECTION I
GENERAL DESCRIPTION

1-1. INTRODUCTION.

This manual contains a detailed technical presentation of the installation, operation, and maintenance procedures for the Supernova Computer. The Supernova computer, as described in this document, consists of the Supernova central processor with one or more 4K core memory assemblies. The Basic I/O Control assembly is also described in this manual. The Basic I/O Control can be configured to control three basic types of peripheral equipment, specifically the Teletype, the Paper Tape Reader, and the Paper Tape Punch. Both the memory and the Basic I/O Control with its various equipment configurations are options which may be purchased independent of the Supernova Central Processor. This manual, however, addresses its presentation to the classical definition of a computer and describes the Supernova Central Processor with 4K of Core memory and a Teletype I/O facility. It should be noted that Technical Manuals for each optional peripheral device is produced by the original manufacturer and is shipped under separate cover with the corresponding equipment. This accompanying documentation should be thoroughly reviewed immediately after the peripheral device is received and prior to installation.

This manual is intended to complement Data General Reference Manual, "How to Use the Nova and the Supernova". Operation and Programming information for the Supernova is provided in the Reference Manual and will not be repeated here except where necessary for expositional continuity. It is recommended that all potential users of this publication become familiar with the "How to Use the Nova and the Supernova" Reference Manual prior to reviewing this Technical Manual.

The detailed technical descriptions presented in this manual assumes the user of this document has a thorough knowledge of the operation of TTμL logic circuitry and the fundamentals of digital computer operations. All electrical drawings referenced in this text are compiled and bound into Section VII of this manual. The input/output pin definitions of the various types of integrated circuit (IC) packages constituting the Supernova and Basic I/O Control logic are summarized in Appendix A of this manual. The illustrated parts list,

presented in Section VI of this manual, can be used as a cross reference source which indexes the reference designator for the IC part (appearing on the logic diagram) with the corresponding manufacturer's part number. Once the IC manufacturer's part number has been retrieved from Section VI it can be used to reference the corresponding IC logic symbol and pin definitions listed in Appendix A.

1-2. GENERAL FUNCTIONAL DESCRIPTION.

The Supernova is a general purpose computer with a 16-bit word length. The Supernova core memory cycle time is 800 nanoseconds and 300 nanoseconds for read-only memory. The Supernova Processor contains an Overlap feature when used with read-only memory. This feature provides that if an instruction in the arithmetic and logical class is fetched from read-only memory the processor "overlaps" its execution with the fetching of the subsequent instruction so that the average time required is 300 nanoseconds. The Supernova contains four hardware accumulators which are used for data storage and manipulation during the execution of all arithmetic and logic class (ALC) instructions. The four accumulators also perform double duty as part of the input/output system. Data exchanges between the external device interface logic and the Supernova processor are performed under program control using the four accumulators.

The Supernova has two types of facilities for loading programs automatically (without relying on a program already stored in memory). The first of these is called Program Load and consists of hardware which reads a short loader program into core memory. This program is then executed to read in the object program. The Program Load switch is mounted on the Supernova console, and actuating this switch triggers special hardware which generates a sequence machine instruction codes simulating a series of 66 DIAS instructions, all of which address the device whose code is selected by data switches 10-15. To load a program automatically, the operator must set up the peripheral device to be used, set its code into data switches 10-15 (also located on the Supernova console), press the I/O Reset switch (also located on the Supernova console) to clear the I/O system, and then press the Program Load switch. The processor in executing the simulated DIAS instructions will place the device in operation and upon encountering the first nonzero byte reads 33 pairs of bytes into memory, starting at location 0. (The first byte of a pair read is placed in the left half of the word, with the second byte read becoming the right half of of the word.) Upon storing the thirty-third word in location 40, the processor executes the

contents of that location; the last word in the block in thus normally a jump instruction into the body of code just read (or a halt to stop the processor). If the block contains fewer than thirty-three words the processor simply reads the trailing blank tape as zeros. In this case the word stored in location 40 is also zero and is executed as JMP 0.

The second automatic loading facility, channel start, also operates in a similar manner with the exception data loading is performed via the Supernova data channels. Control procedures are similar in that the operator sets up the loading device, sets its code into data switches 10-15, clears with the I/O reset switch. However, the actuating control for loading through the data channels is the Channel Start switch (also located on the Supernova console). The processor places the device in operation, then stores the instruction JMP 377 in location 377 and begins normal program execution at that location. Hence the processor keeps repeating the instruction in 377 while the channel stores data beginning at location 0. Eventually location 377 receives a data word, which is then executed by the processor as an instruction; this is typically a jump into the data just read or a halt. (Several constrains governing the operation of the automatic program loading through the data channels are detailed in Section III of this manual.)

Supernova input/output instructions perform data transfers to and from peripheral equipment. The I/O instruction format allows 64 device code definitions, of which (octal) code 0 is not used and (octal) 77 is reserved for special functions. A 16-level programmed priority interrupt facilitates handling 16 different device speed classes within the interrupt control structure. Interrupts are enabled or disabled by a processor word, of which each bit position exercises disabling control over (the interrupt logic) the devices assigned to that bit position. In terms of interrupt timing, the time a device must wait depends on the number of devices capable of producing interrupts, the length of service routines for devices of higher priority, and whether the data channels are in use. Excluding the execution of indirect memory reference instructions the maximum interrupt waiting time (for any device interrupting the Supernova) is approximately 9 μsec (5 μsec without multiple-device). The instruction times for the Supernova are listed in Table 1-1.

Table 1-1. Supernova Instruction Execution Times (in Microseconds)

Instruction	Memory: Core	Memory: Read Only
LDA	1.6	1.4*
STA	1.6	1.4
ISZ, DSZ	1.8	1.6
JMP	.8	.6
JSR	1.4	1.2
Indirect addressing	.8	.6
Autoindexing	.2	
COM, NEG, MOV, INC	.8**	.3****
ADC, SUB, ADD, AND	.8**	.3****
I/O input (except INTA), I/O skips	2.9	2.8
NIO	3.3	3.2
I/O output	3.3	3.2
INTA	3.7	3.6
MUL		
Average	3.8	3.7
Maximum	5.4	5.3
DIV		
Successful	6.9	6.8
Unsuccessful	1.6	1.5
Interrupt	2.2	
Latency	9***	
Data channel		
Input	2.3	
Output, increment	2.8	
Add	2.8	
Latency		
Without multiply-divide	5	
With multiply-divice	9	
High speed data channel		
Input	.8	
Output	1	
Increment, add	1.2	
Latency		
With I/O	4.5	
Without I/O	2.5	

*If instruction and operand are from read-only memory time is 1.2 μsec.
**Time given must be doubled if a skip actually occurs.
***5 μsec without multiply-divice.
****If skip occurs, add .3 μsec if arithmetic or logical instruction is skipped, otherwise add .6 μsec.

The Supernova Processor is available with a number of functional options, e.g., power monitor and auto-restart, multiply-divide, memory allocation and protection, and high speed data channel. The documentation relative to each option is shipped as an addendum to this manual when the corresponding option is ordered.

1-2.1. Computer Organization.

The particulars covered in this paragraph are addressed primarily to the unique features of the Supernova architecture rather than to the fundamental operations characteristic of all general purpose computers. In this regard it is suggested that the Supernova logic diagrams bound into Section VII of this manual be referenced while reviewing this paragraph. Figure 1-1 is a general block diagram of the Supernova Computer. This diagram serves two important purposes; of which the first shows the function relationships of the major Supernova logic sections, the second identifies the physical locations of the major logic section (relative to the Printed Circuit board assemblies). Each printed circuit board assembly is shown as a dash line enclosing the logic sections physically mounted on that particular board. For example, the CPU-1 PCB assembly contains three major logic sections, the Console logic, Processor & Memory Timing, and Supernova Input/Output. The functional data paths for parallel (word or byte) data is depicted on the drawing by the heavy flow lines. A line with an arrowhead termination on both ends denotes a bi-directional data path. The function of each one of the major Supernova logic sections is briefly described in the following discussion.

The heart of the Supernova is the Major Registers Gating/Adder and Sel & Reg Drive logic sections located on CPU-3. The Major Registers Gating/Adder contains the four Accumulators AC0, AC1, AC2, and AC3, the Program Counter (PC), a Memory Address register (MA), an Adder, and a multiplexer controlling the inputs to the Adder. This section also contains gating to facilitate bi-directional transfer of data between the Adder and the Data Bus, between the Adder and the registers in the 4K Memory, between the Adder and Console. In the case of data transferred from Console, the Adder inputs read the outputs of the Console data switches (through the multiplexer). Address data is transferred to the Console from the MA for illuminating the Console display indicators. In this limited sense data transfers between the Console and the Major Registers Gating/Adder section is bi-directional. The multiplexer switch is driven by a two bit binary code which selects either

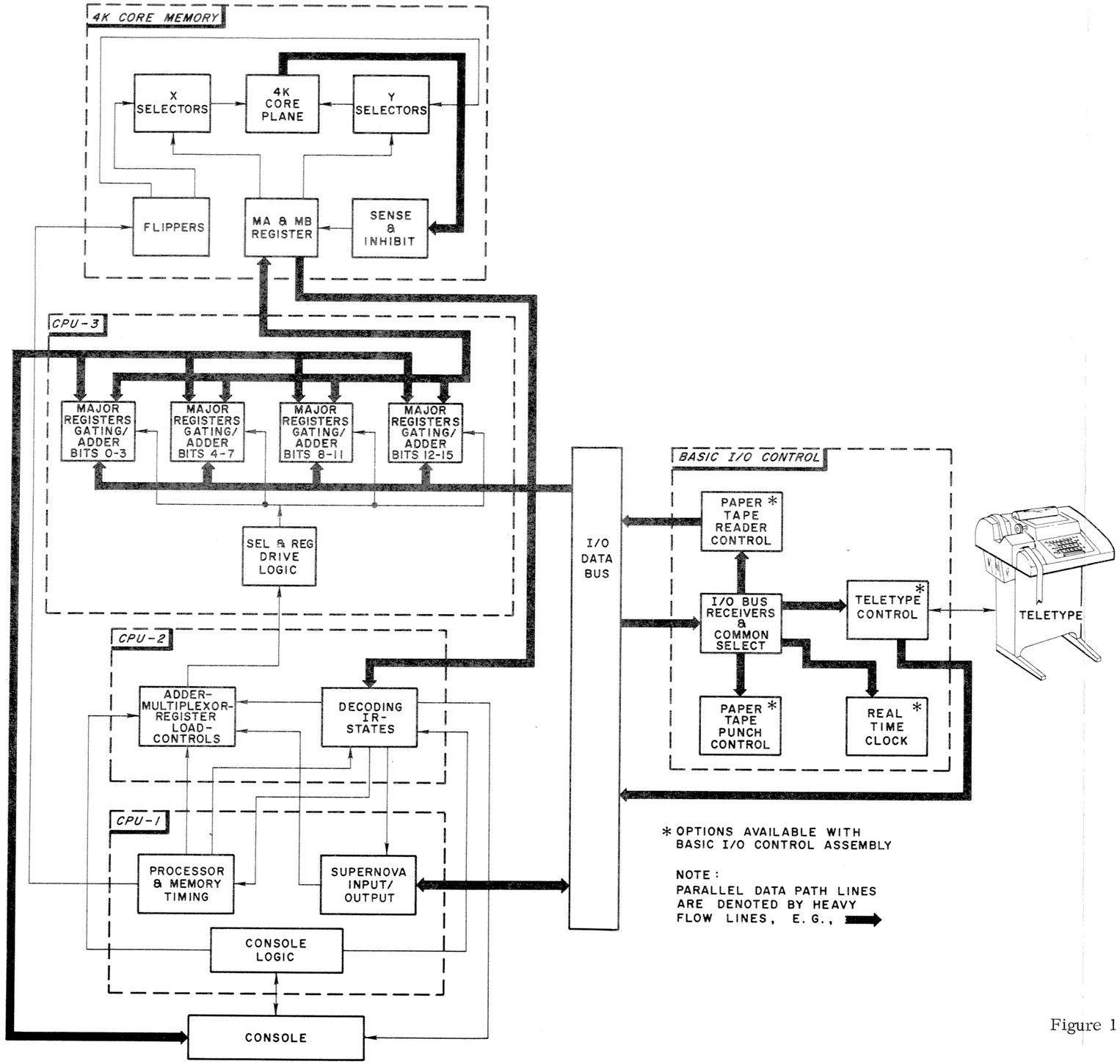

Figure 1-1. Supernova General Functional Block Diagram

no input or one discrete input from three input lines. The Multiplexer also is capable of complimenting any selected input. The primary signal codes for operating the multiplexer originate in the Adder-Multiplexer-Register Load-Controls logic of CPU-2, section and are converted from functional command signals to operational codes through the gating of the Sel & Reg Drive logic section.

The Adder-Multiplexer-Register Load-Controls section of CPU-2 receives signals from the Console logic, Decoding IR-States, and Input/Output sections relative to some specific operation to be performed by the Adder or some specific register operation, and produces the appropriate Command signals for the Sel & Reg Drive logic. The Adder-Multiplexer Register Load-Controls section is composed mainly of gating which combines signals of any one sequence or common events into one functional gate the output of which issues the required register or multiplexer command. A good example of collective gating in this section is shown in the generation of the increment the Program Counter (INC PC) signal. The gates associated with producing this signal are activated by the occurrence of any one of seven logical conditions. For example, the PC is incremented automatically at the start of a fetch cycle. This condition is sensed by a gate which in turn implements other logic to generate INC PC. This signal is transmitted to the Major Registers Gating-Adder section where the operational function is performed. An example of a signal generated in the Adder-Multiplexer Register Load-Controls logic section which is in turn coded in the Sel & Reg Drive logic section is found in the ACS COMP ENAB (Complement the source Accumulator). Anyone of four conditions present will cause gating to produce the complement signal, one of which is the AUTO DEC (automatic decrement) signal. The $\overline{\text{ACS COMP ENAB}}$ signal becomes (SX-COM) at the output of the Sel & Reg Drive logic. This signal complements the all zero output at the multiplexer producing a value at the adder input.

The Decoding-IR-States logic section also mounted on CPU-2 contains the Instruction register (IR) and decoding gates for deriving the instruction signals. This section also contains the Operational State Selector which determines which major operational cycle will be performed next (Fetch, Defer, Execute) in the flow of instruction processing. Data retrieved from memory during a Fetch cycle is transferred from a buffer register in the memory logic section directly into the IR register. The outputs of the IR register are decoded by logic to derive unique instruction signals, e.g., JMP, JSR, ISZ, etc. The

Operational State Selector effectively monitors the current operational state of the Processor a and uses this information in addition to any other outstanding or pending operations to be performed, to determine the next operational state of the Processor. The output signals from the Operational State Selector function as primary control signals for the Adder-Multiplexer Register Load-Controls logic and Processor & Memory Timing section. The IR output signals are used in the Input/Output section along with the outputs from the Operational State Selector.

The Processor & Memory Timing section located on the CPU-1 assembly contains the 20 Megacycle clock and associated timing pulse chains which control the various processor events. Logic is also provided in this section for generating the READ, WRITE and INHIBIT signals for the Memory Assemblies. These signals are also synchronized by the basic CPU clock source. The Input/Output section is identified with the Supernova prefix to differentiate between it and the I/O logic contained on the Basic I/O Control Assembly. The Supernova Input/Output section, also mounted on CPU-1 contains gates which generate the required Data Channel signals and standard I/O control signals for the I/O Data Bus. These gates generate device codes, DATO DATI, INT, IO SKIP, and DCH signal hierarchies. Bus control signals transmitted between the appropriate (Device) control and the processor pass through Supernova Input/Output logic section. The I/O timing generator is also contained in this section.

The Console Logic is mounted on the CPU-1 assembly and functions as an interface between the Console Manual Control switches (or Keys) and the control logic mounted on CPU-2. This section also contains the RUN, KEY SYNC, and STOP SYNC logic. These synchronizing signals are instrumental in implementing manual switch functions synchronously with the processing of instructions. For example, actuating the Deposit switch on the Console generates a DP+DPN signal in the Console logic section. This signal in turn produces (in conjunction with $\overline{\text{KEY2}}$ generated by the Operational State Selector) $\overline{\text{CON OUT}}$, which in turn generates D-R-L-S in the Sel & Reg Drive logic. D-R-L-S enables the multiplexer switch to select the Console switch lines as inputs to the Adder. (It should be noted that a memory cycle also occurs on a deposit to transfer the Adder outputs into memory.)

The 4K Memory Assembly contains the core plane, X and Y line selector logic, Flippers Sense & Inhibit logic, a Memory Address register, and an Inhibit-Buffer register.

The X and Y selector logic is driven by the Read and Write current signals from the Flippers logic section. The outputs from Memory Address register are decoded to generate the X and Y selection (Source and Return) signals. It should be pointed out that there is also a Memory Address register in the Major Registers section of CPU-3. This MA works in conjunction with the Adder and is used to facilitate high-speed relative address calculations. The memory address register in the memory assembly functions primarily as a buffer register for the X and Y selection logic. The Inhibit register is used as a data buffer register in the memory. Output data from the Adder is loaded into this register in preparation for writing it into memory. The outputs of this register controls the Inhibit Circuitry which either allows or prevents core storage as determined by the state of the corresponding Inhibit register flip-flop. When data is read out of memory, the Sense Amplifiers unconditionally set up the Inhibit register. The outputs of the Inhibit register are gated out over the $\overline{\text{MEM}}$ lines back to the Adder multiplexer.

The Basic I/O Control assembly contains provisions for four optional device control logic sections to be added to the assembly as a purchased option. However, the I/O Bus Receiver & Common Select is standard and contains bus gates which are common to each optional control logic section. In the particular case, it is assumed that the Teletype Control has been included as an option. The Teletype Control contains Busy, Done and Interrupt logic for controlling the operational data transmissions exchanged between the Teletype and the Central Processor. The Control also contains a teletype clock (for synchronizing transmission rates with the teletype), a serial to parallel converter, and a parallel to serial converter. The serial to parallel converter receives the serial input data from the teletype keyboard (or reader) and sequentionally shifts it into an 8 bit register. Once the register is loaded an interrupt is generated (if the interrupt request is enabled) requesting the processor read in the data. The parallel to serial converter is loaded with processor data from the bus, and this data is subsequently serially shifted from the register out to the Teletype Printer (or punch). Generally speaking, the I/O Bus signals generated by the Supernova Input/Output section are present on the Bus with I/O data going into or out of the Adder. For example, in performing a DOA instruction to send data to the Teletype, IR bits 5, 6, and 7 would be decoded in the Supernova Input/Output logic to generate Bus signal DATOA. If AC0 was designated as the accumulator holding the output data, the outputs of

AC0 would be gated through the Multiplexer and Adder out to the $\overline{\text{DATA}}$ Bus lines. The device code for the Teletype Output, Octal 11 would also be present on Bus lines $\overline{\text{DS0}}$-$\overline{\text{DS5}}$. These signals are also generated in the Supernova Input/Output logic section and are derived from $\overline{\text{MEM}}$ 10 through 15 from the memory Inhibit register. (Residual holding facility during the present execution of the I/O instruction nust read from core.)

1-3. PHYSICAL DESCRIPTION.

The Supernova Central Processor by definition consists of the Console/Enclosure Unit Power Supply Unit, Central Processor-1 (CPU-1) printed circuit board assembly, Central Processor-2 (CPU-2) printed circuit board assembly, and Central Processor-3 (CPU-3) printed circuit board assembly. An outline drawing of the printed circuit boards used in major Supernova Assemblies is provided in Appendix A of the "How to use the Nova Computers" reference manual (Fourth Edition). The Supernova Console/Enclosure Unit is so designed that seven 15 X 15 inch Printed Circuit Board (PCB) Assemblies may be plug mounted into a special printed circuit board connector in the Enclosure Chassis. The board assemblies are inserted horizontally into the Enclosure Chassis. A pair of guiding rails are built into the chassis frame (on each board level) to insure proper insertion of the board contacts into the corresponding socket of the multiple printed circuit board connector. The seven connector slots are numbered from the bottom of the chassis up to the top with slots 1, 2, and 3 reserved for the CPU-1, CPU-2, and CPU-3 assemblies respectively. The five remaining slots may be used for memory assemblies, I/O assemblies, or special control board assemblies. Figure 1-2 is a drawing showing the major components of the Supernova Computer. The Supernova power supply is mounted in the rear of the Console/Enclosure Unit and contains two fans (on each end) for cooling. The rear panel of the power supply also functions as the Input/Output connector panel for the processor. When optional peripheral equipment is purchased with the Supernova, the required I/O connector is wired into the multiple printed circuit board connector and mounted on Input/Output connector panel. (This wiring is direct from the pins of the selected PCB socket to the pins of the corresponding I/O connector.) It should be noted once a socket is wired for a specific Control PCB Assembly (used to control the optional peripheral device) that particular socket is dedicated to that purpose and must not be used for any other (different type) Control PCB Assembly. For example, a 4K Memory PCB Assembly can be mounted in any spare socket and will work

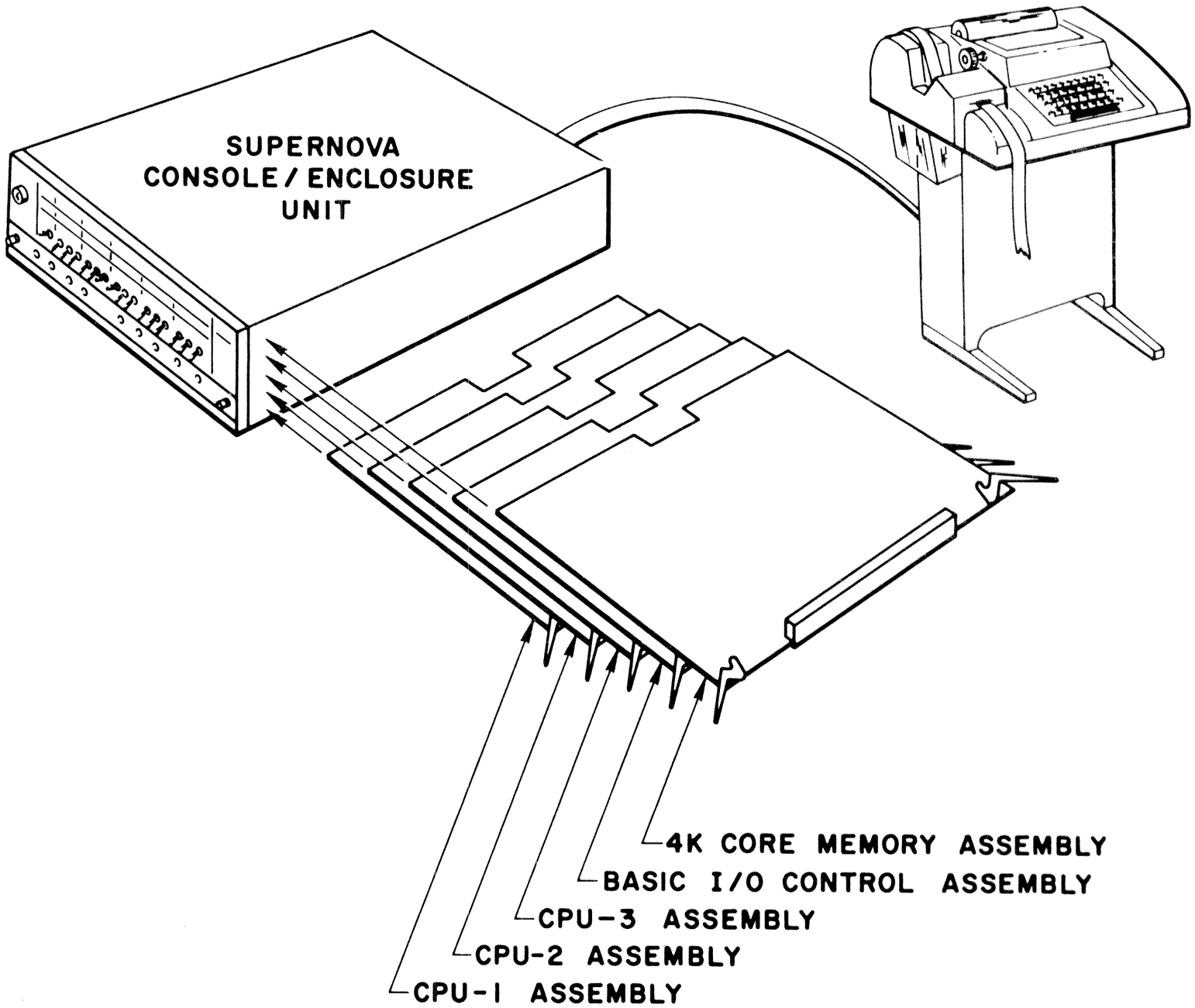

Figure 1-2, Major Components of the Supernova Computer

properly. However, since the Control PCB Assembly must be hardwired from the socket to the output I/O connector, it must be mounted in the (multiple printed circuit board) socket wired for it. Table 1-2 is a summary of the Supernova Physical Characteristics.

Table 1-2. Supernova Physical Characteristics

Physical Specifications	
Enclosure Height:	5 1/4 inches
Enclosure Width:	19 inches
Enclosure Depth:	22 inches (20 1/4 W/O Console)
Weight:	60 lbs.
ASR33 Teletype Height (on stand):	45 inches
ASR33 Teletype Width:	22 inches
ASR33 Teletype Depth:	19 inches
ASR33 Teletype Weight:	56 lbs.

Electrical Specifications	
Power Requirements:	115v or 230v* single phase, ±10%, 47 to 63 Hz, Minimum Current** 2.2 amperes (250 watts) Maximum Current 3.1 amperes (350 watts)
ASR33 Teletype:	115v single phase, 2 amperes, turn on surge 7 amperes, 92 watts.
Bus Signals:	Low = 0 volts to +.4 volt nominal High = +2.2 volts to 3.0 volts nominal
Processor Logic Signals	Low = 0 volts to +.4 volt nominal High = +2.5 volts to 5.0 volts, +3.5 volts nominal
Power Supply Voltages	
+5 Volt Output: ~4.80 V Lower chassis 9/6/77 ~5.11 V Upper chassis	+5 volts (nom.), +4.7 volts low limit, +5.45 high limit @ 25°C. Temperature variation: From +5.1v @ 25°C to +5.0v @ 55°C Typ.
-5 Volt Output:	-5 volts (nom.), -4.7 volts high limit, -5.45 low limit @ 25°C. Temperature variation: From -5.37V @ 25°C to -5.3V @ 55°C Typ.

*230v on Special order

**Based on Minimum Computer Configuration of Processor, teletype interface, and 4K of memory.

Table 1-2. Supernova Physical Characteristics (Continued)

Indicator Lamp Voltage (V_L)	+ 9 to + 11 Volts on ϕ1 line + 9 to + 11 Volts on ϕ2 line Temperature variation: N/A
+ VMEM Output:	*See Memory Drive Specification.* Temperature variation: From + 21.3v setting @ 25°C to + 19.5v (Max.) @ 55°C.
+ VINH Output:	*See Memory Drive Specification.* Temperature variation: From + 17.2v setting @ 25°C to + 15.5 (Max.) @ 55°C.
Power Supply Currents	
+ 5 Volt Output:	9.6 amps max.*
- 5 Volt Output:	0.8 amps max.
Memory Drive Nominal	
(+ VMEM) X and Y windings:	+ 21.7 Volts, 390 ma @ 25°C
(+ VINH) Inhibit windings:	+ 17.2 Volts, 740 ma @ 25°C

Functional

Memory Reference Cycle Time	
With Accumulator:	1.6 microseconds
Without Accumulator:	.8 microseconds
Word Length:	16 bits
Core Memory Size:	4096 words, expandable to 32,768 in increments of 4096 words

* + 5 Volt current specification is based on requirements of a Supernova with one 4K Memory only. Add 1 amp (as an approximation) for each additional 4K Memory installed.

Table 1-2. Supernova Physical Characteristics (Continued)

Instructions:	6 classes of instruction Move Data Modify Memory Jump Arithmetic and Logic Input/Output
Input/Output	62 Unique Device Addresses 1 Special Function Code (77)

Ambient Conditions

Operating Temperature:	+ 32° to + 130° F (0° to + 55° C)
Operating Humidity:	0 to 90% relative humidity
Storage Temperature:	+ 32° to + 130° F (0° to + 55° C)

1-4. PERTINENT DOCUMENTS.

The following documents serve as source material and complement the information in this manual:

How to Use the Nova and the Supernova (Third Edition) - OR - How to Use the Nova Computers (Fourth Edition)

Section 574-100-201 of Bulletin 273B, Volume 1, TECHNICAL MANUAL, 32 AND 33 TELETYPEWRITER SETS

Supernova Bootstrap & Binary Loader Manual #083-000001

Supernova Instruction Timer Manual #087-000002

Exerciser Manual #097-000004

Teletype Test II Manual #097-000009

Memory Checkerboard III Manual #097-000014

1-5. ABBREVIATIONS.

Listed below are the most commonly used abbreviations of registers, key operations, components, instructions, and signal names. Signal names not included in this list will be found in Appendix B Signal Origins. Appendix B contains an alphanumerical list of all signal names which appear on drawings, together with the drawing number which contains the generating circuits for the signal.

AC	Accumulator
ACC0	Accumulator 0 select switch at Console
ACD	Destination Accumulator

ABBREVIATIONS (Continued)

ACDP	Accumulator Deposit switch at Console
ACEX	Accumulator Examine switch at Console
ACS	Source Accumulator
ACSX	Source Accumulator X
ALC	Arithmetic Logic Class (instructions)
AUTO DEC	Automatic Decrement
AUTO INC	Automatic Increment
CHST	Channel Start (via Data Channels)
CLK	Clock
CLR	Clear
CODE 77	CPU Device Code
COMP	Complement
CON	Console
CONT	Continue switch at Console
CPU	Central Processor Unit
CRY	Carry
DATIA	Data In A (I/O instruction)
DATOA	Data Out A (I/O instruction)
DCH	Data Channels
DCHA	Data Channel Acknowledge
DCH INC	Data Channels Increment
DCHI	Data Channel In
DCHM(0 or 1)	Data Channel Mode (0 or 1) Code type of Data Channel Cycle requested by Device
DCHO	Data Channel Out
DCHP	Data Channel Priority
DCHR	Data Channel Request
DEFER	Defer (instruction execution state)
DIV	Divide (instruction)

ABBREVIATIONS (Continued)

DP	Deposit
DPN	Deposit Next
DSZ	Decrement and Skip if Zero (instruction)
DS0	Device Select line 0
EFA	Effective Address
EIS	Extended Instruction Set
EIS LD	Extended Instruction Set Load
EX	Examine
EXEC B	Variation of Execute Cycle
EXN	Examine Next
F SET	Fetch Set
HSC	High Speed Channel
INC PC	Increment Program Counter
IND DRIVE	Indicator Drive
INH	Inhibit Register
INHB	Inhibit (Memory Stack)
INTA	Interrupt Acknowledge
INTR	Interrupt (Bus Signal from Device)
IO or I/O	Input/Output
ION	Interrupt On
IO PLS	Input/Output Pulse
IO RLS	Input/Output Release (let Processor Continue)
IORST	Input/Output Reset
IO SKIP	Input/Output Skip (instruction)
IOTG	Input/Output Timing Generator
IO0	Input/Output Data Line 0
IR	Instruction Register
ISTP	Instruction Step (Console switch)
ISZ	Increment and Skip if Zero (instruction)

ABBREVIATIONS (Continued)

JMP	Jump (instruction)
JSR	Jump to Subroutine (instruction)
MA	Memory Address (register)
MB	Memory Buffer (register)
MBO	Adder Output Data to Memory Buffer
MEM	Data Inputs to Processor from Memory
MEM CY SET	Memory Cycle Set
MEM MOD	Memory Modify
MEM OK	+ VINH (Power Supply) Monitor Output
MSKO	Mask Out (instruction)
MSTP	Memory Step (Console switch)
MUL	Multiply
OVFLO	Signal to Device that memory location being incremented or added to (Via Data Channels) has Overflowed
PC	Program Counter
PEND	Pending, e.g., INT PEND
PI	Program Interrupt
PLC	Program Load Console
POT IO INST	Potential IO Instruction
PREV. CRY	Prevent Carry
PROT	(Memory) Protect
PTG	Processor Timing Generator
PWR FAIL	Power Fail (Power Supply Monitor)
RINH	(Collector) Resistor, Inhibit Driver
ROS	Read Only Storage
RQENB	Request Enable
RST	Restart (Console switch)
RXR	Resistor X (plane) Return (Memory Stack Drivers)
RXS	Resistor X (plane) Source (Memory Stack Drivers)
RYR	Resistor Y (plane) Return (Memory Stack Drivers)

ABBREVIATIONS (Continued)

RYS	Resistor Y (place) Source (Memory Stack Drivers)
SA	Sense Amplifier
SELB	Selected Busy (Bus signal)
SELD	Selected Done (Bus signal)
SELX	Select X (used with SELY in CPU-3 Adder for Shift, Swap and Load Control)
SELY	Select Y (used with SELX in CPU-3 Adder for Shift, Swap and Load Control)
SL	Sense Line (Memory Stack)
SNS	Sense (Amplifier outputs)
STA	Store Accumulator (instruction)
STRB	Strobe (Memory Stack)
STRT	Start (Console switch)
TS	Time State
TT	Teletype
TTI	Teletype In (Teletype Keyboard/Reader Buffer)
TTO	Teletype Out (Teletype Teleprinter/Punch Buffer)
VREF	Reference Voltage (Power Supply)
XRR	X (plane) Read Return (Memory Stack)
XRS	X (place) Read Source (Memory Stack)
YRR	Y (plane) Read Return (Memory Stack)
YRS	Y (plane) Read Source (Memory Stack)
+ VINH	+ (Memory) Inhibit Voltage
+ VMEM	+ Voltage Memory (Drivers)
+ 5 OK	+ 5 Volt (power) operating properly
+ 30 VNR	+ 30 Volts Not Regulated

SECTION II

INSTALLATION

2-1. GENERAL.

This section provides detailed information and procedures for installing the basic Supernova Computer. The Supernova and teletype are shipped in separate containers. Prior to performing any installation procedures inspect both shipping containers for any visible intransit damage such as would result from dropping or being punctured or crushed. Contact the carrier and Data General immediately if any damage is discovered, specifying the nature and extent of damage. Physical installation data and descriptions are provided in Appendix B of the "How to Use the Nova and The Supernova" reference manual, and Appendix B of the more recent "How to Use the Nova Computers" reference manual (Fourth edition).

2-2. UNPACKING INSTRUCTIONS.

The following two paragraphs describe the proper method of unpacking the Supernova Computer and an ASR33 Teletype. The first paragraph describes the approved procedures for unpacking the Supernova. The second paragraph describes the procedures for unpacking the Teletype. It is recommended that all shipping hardware, shims, packing and carton be saved and stored after unpacking in the event either machine is ever reshipped.

2-2.1. Unpacking the Supernova.

After opening the Supernova shipping container perform the steps of the following procedure:

a) Remove attached hardware (keys, mounting hardware, etc.).
b) Remove both U-shaped cardboard retaining frames.
c) Lift top layer of cardboard from box.
   Note: Top of computer should now be exposed.
d) Remove cardboard shims located on sides of computer.
e) Remove both restraining shims on the front of the console.
f) Lift the unit from the box. (Requires two people.)
   Do not lift from the sides of the computer. Hands should be placed on the rear and underside of the Power Supply and by the front of the console.
   Check unit for shipping damage. Remove keys from plastic bag, insert the key, turn completely counterclockwise to the "Off" position. Facing the rear of the machine, ensure the circuit breaker is placed to the right.

g) Remove all packing material and General Purpose frames from the system. Standard circuit boards should not be removed.
h) The computer is ready to apply power. It is suggested that the operator read the procedures listed under the Supernova Start-up and Checkout paragraph of this Section before applying power to the machine.

2-2.2. Unpacking the ASR33 Teletype.

The complete ASR33 is packaged in one carton. After opening the ASR33 shipping container perform the steps of the following procedure:

a) Remove Styroform pads (2). (See Figure 2-1.)
b) Remove corner braces (4) and Teletype Stand. (See Figure 2-2.) Manuals will be packed inside Teletype Stand.
c) Locate teletype bulletin 273B Vol. 1 in the manual set. Refer to page 1 of the section 574-100-201TC and read unpacking instructions.
d) Remove cardboard insets, accessory kit, and Typing Unit. (See Figure 2-3.) Typing Unit is mounted on a past board shipping pallet by seven screws.

NOTE: DO NOT USE OR ATTEMPT TO OPERATE TYPING UNIT BEFORE REMOVING THE (3) HEX HEAD BOLTS FROM THE BOTTOM OF THE SHIPPING PALLET.

e) Remove three pieces of adhesive nylon tape; two pieces are securing the paper supply and lid, the other piece is securing the paper tape supply, punch and reader.
f) Remove the Typing Unit Cover to expose the carriage. The carriage is tied to the chassis with a pipe cleaner. This securing wire must be removed before operating the Teletype.
g) Some Teletypes are equipped with a yellow spacer spring holding the reader fingers stationary. This must be removed prior to operating the Teletype.

2-3. SUPERNOVA START-UP AND CHECKOUT.

The procedures listed below describe the proper methods for initial turn-on and subsequent checkout of the Supernova Computer. These procedures should be performed

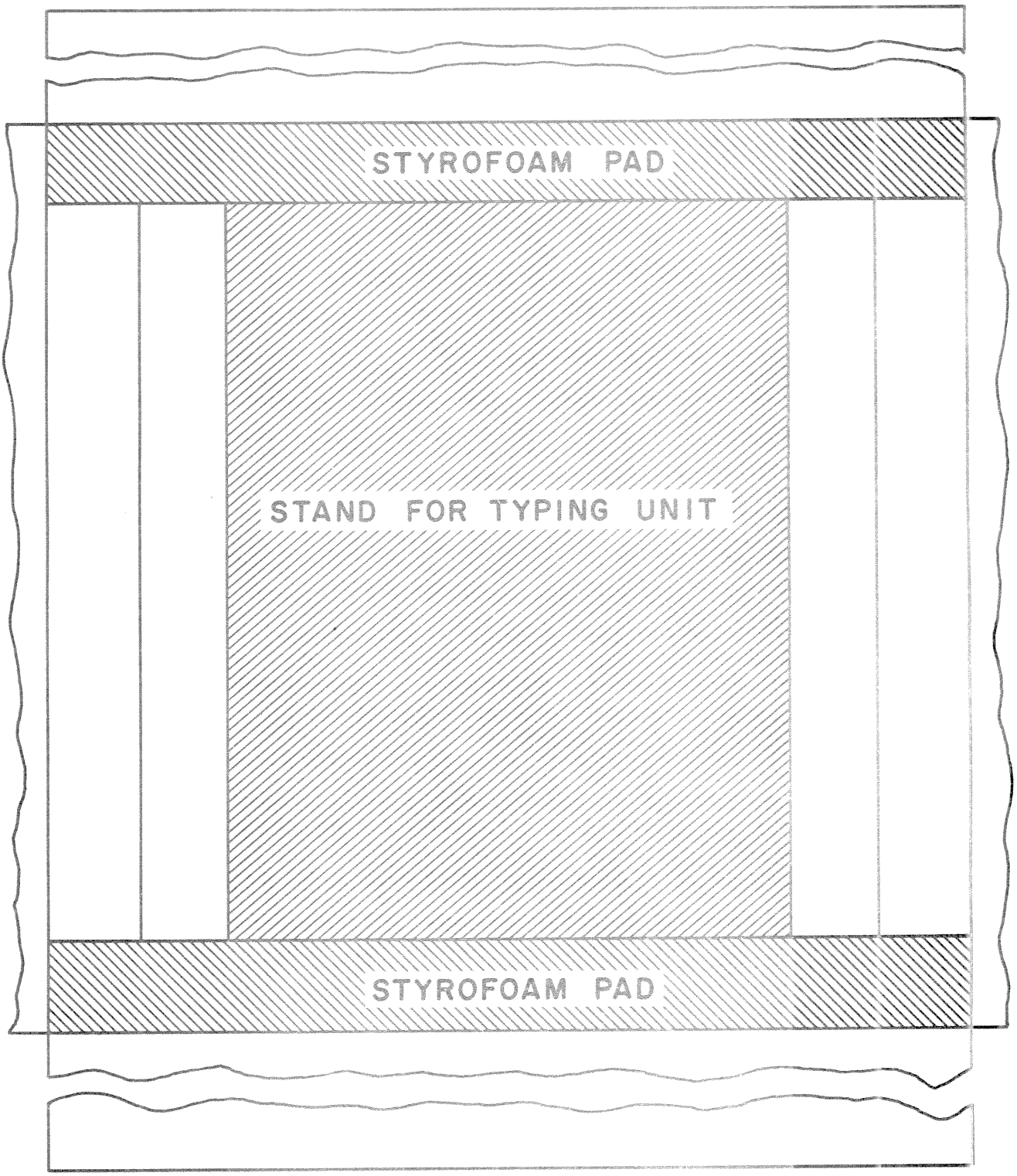

Figure 2-1. Location of Styrofoam Pads

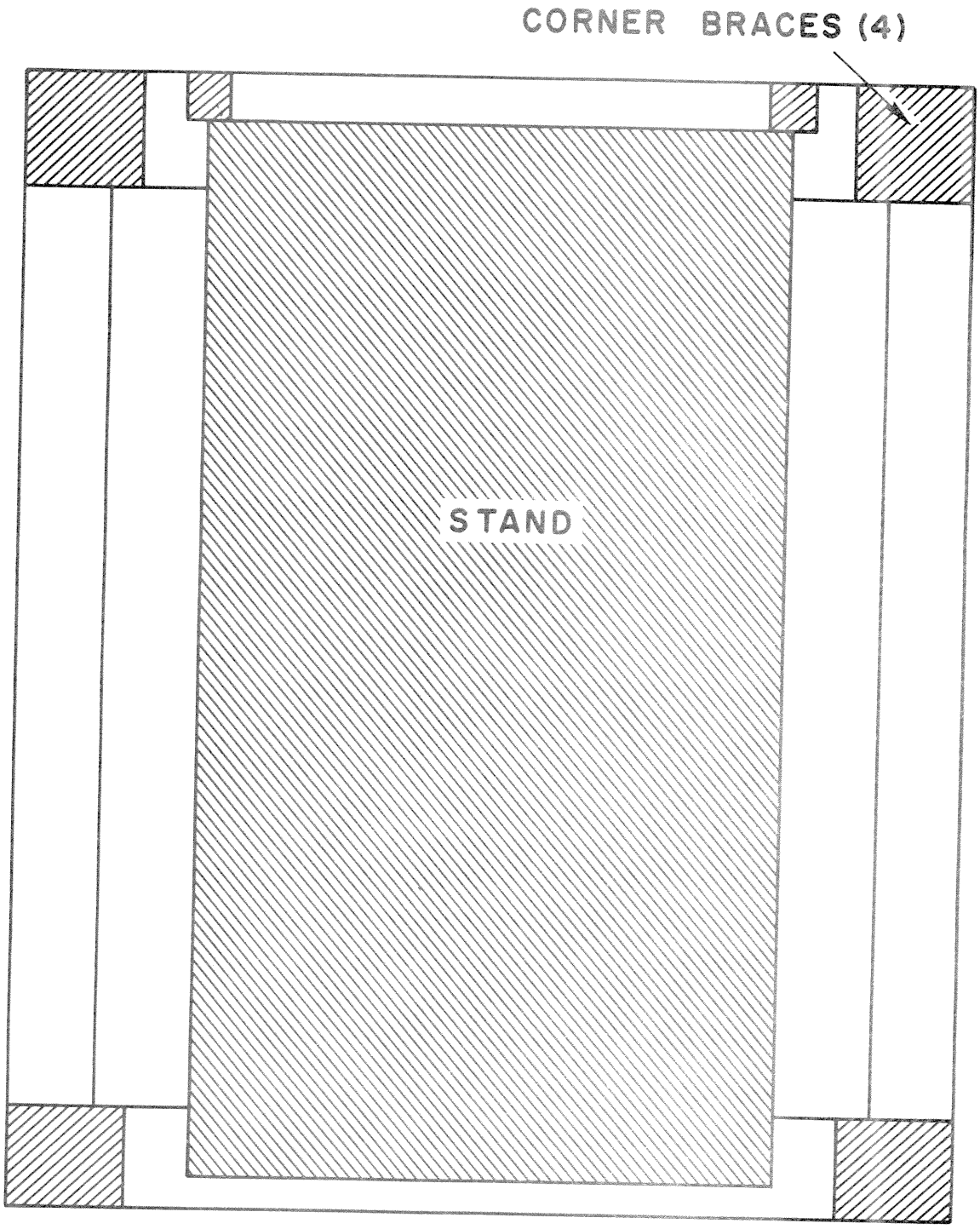

Figure 2-2. Location of Corner Braces in Teletype Carton

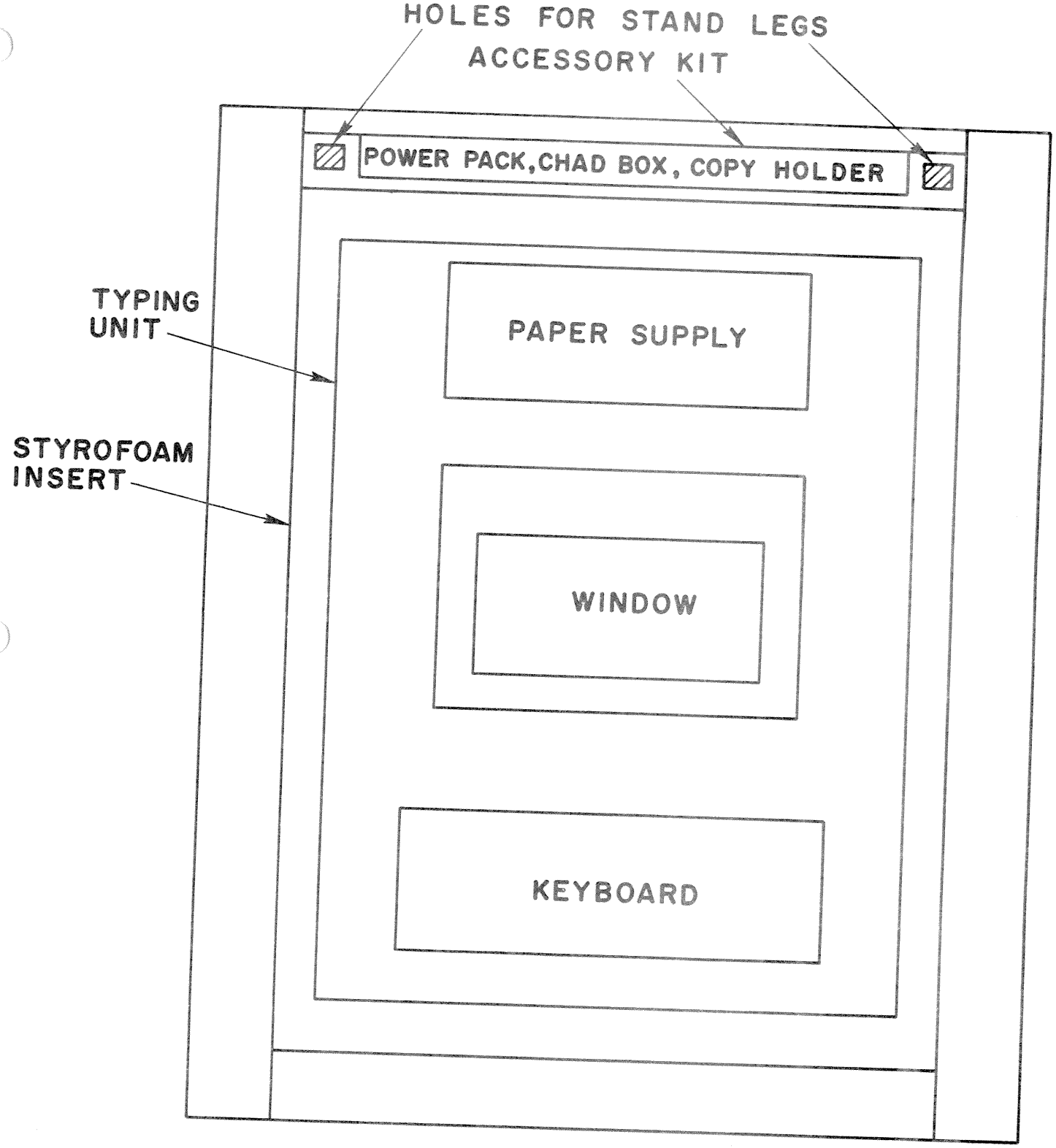

Figure 2-3. Location of Teletype Typing Unit in Carton

immediately after the Supernova has been unpacked. The procedures are listed below in the exact order of performance, and must be performed in the order of appearance, during initial turn-on.

2-3.1. Start-Up Procedure.

The general purpose Exerciser (Program Listing and Tape #095-000012, Manual #097-000004) is always the last program run in each Supernova prior to shipping. The Exerciser diagnostic program checks the entire instruction repertoire and all memory locations associated with that particular processor system. This program should still be intact within the memory and available for execution. To start this program, only Data Switch 14 on the operator's console should be raised. Turn power "ON" by setting the key to the vertical position. Raise the Reset/Stop switch momentarily and then lift the Start switch. Program should now be in execution with both the Fetch and Run indicators on. With typical operation of the program, a incrementing sequence from $1,000_8$ to approximately $3,400_8$ will be observed in the Address Register display. The cycle takes approximately one minute for a 4K system and becomes significantly longer depending on a maximum core size of the system. Any halt of the computer and improper indications constitutes an error. Should you encounter any difficulty with the start-up procedure, please contact the Data General representative in your area, or our Field Service Department at the Southboro factory (Area Code: 617-485-9100).

2-3.2. Check-Out Procedures.

The Supernova check-out sequence consists of static and dynamic tests. Static tests are performed manually at the Operator's Console. Dynamic tests, on the other hand, are a series of tests performed under program control, and either terminate successfully or halt at some specific location to indicate detection of some failure by the diagnostic. In the normal sequence of testing, the static tests are performed first to verify all of the manual controls are working properly. Once the Console is verified as operational, the dynamic testing may be performed. Successful completion of all the recommended diagnostic tests should be considered verification of the first check-out step. Complete verification is obtained when all of the Supernova diagnostic program tapes included in the documentation package have been run successfully.

2-3.2.1 Static Tests.

a) Power on and verify console indicators operate properly.
b) Check that both fans are operative.
c) Deposit and examine all zeros in Memory location 0.
d) Deposit and examine all ones in Memory location 0.
e) Deposit and examine all zeros in Accumulators ACC 0-3.
f) Deposit and examine all ones in Accumulators ACC 0-3.
g) Deposit 000017 in ACC 0.
h) Deposit 000360 in ACC 1.
i) Deposit 007400 in ACC 2.
j) Deposit 170000 in ACC 3.
k) Examine all accumulators and verify no data changed.
l) Deposit all zeros in Memory location 0.
m) Raise start switch. Verify run indicator on.
n) Lock computer. Verify reset/stop toggle functional inoperative.
o) Unlock computer.
p) Depress STOP.
q) Continually depress DEPOSIT NEXT. Verify PC increments.
r) Continually depress EXAMINE NEXT. Verify PC increments.

2-3.2.2 Dynamic Tests. At this point and prior to performing the first dynamic test it is necessary to connect the Teletype to the Supernova. These procedures assume all of the unpacking steps for the Teletype listed in paragraph 2-2.2 have been completed.

2-3.2.2.1 Teletype to Computer Connection Procedure.

a) Turn off computer.
b) Plug in TTY to 115v outlet in the rear of the Supernova Enclosure.
c) Plug in the 9 pin connector to the receptacle indicated by the connector layout diagram attached to the rear of the Supernova Enclosure. The proper connector is labeled 4010 (Data General Model number for TTY).
d) Turn the line/local switch on the lower-right-front-panel of TTY to local.
e) Place roll of tape in punch and turn on punch.
f) Type all characters on keyboard. Note correct typing and also that punch is operating. It is not necessary to verify tape produced. That will be done in the sequence of tests that follow.
g) Turn punch off and return line/local switch to line. The unit is now ready for use by the computer.

The next step in the dynamic test sequence is to load the Bootstrap and Binary Loader into the Supernova. The Bootstrap is loaded through the automatic Program Load facilities of the Supernova, and is used in turn to load the Binary Loader into the Supernova memory. Execution of the Binary Loader will bring the test programs into Core.

2-3.2.2.2 Bootstrap and Binary Loader.

a) Turn on Supernova. Verify Teletype is on-line.
b) Set Teletype reader switch to FREE.
c) Place Selfloading Bootstrap and Binary Loader (Special Format #081-000001, Manual #083-000001) into Teletype reader, and set reader switch to START.
d) Set the TTI device code 010_8 into the six rightmost Supernova Console switches (bits 10-15).
e) Lift the Program Load/Channel Start switch on the Supernova Console to the Program Load position.
f) Tape should move through the Teletype reader. When the tape halts verify Console Address register displays 00120_8 as the halt location.
g) Set Teletype reader switch to FREE, and remove Bootstrap and Binary Loader tape from Teletype reader.
h) Place the test program tape Checkerboard III (Binary tape #095-000031, Manual #097-000014) into the Teletype reader, and set reader switch to START.
i) Press Start/Continue switch on the Supernova Console to the Continue Position.
j) Verify tape moves through the Teletype reader. When tape halts Checkerboard III will be loaded and ready for execution.
k) It should be noted that for subsequent loading of other programs after a program other than the Binary loader has been executed, first place program tape in the Teletype reader, then load XX777 into the console switches and lift the Start/Continue switch to Start. This will rerun the Binary Loader and bring the new program into core.

2-3.2.2.3 Memory Test. After the memory test program, Checkerboard III has been loaded as per paragraph 2-3.2.2.2, perform the following steps to run the test program:

a) Modify location 4 to X7577 Memory location if larger than 4K.
b) Place 000002_8 in Console switches.
c) Lift Start switch.
d) Verify program cycle.
e) Lift Console switch 0 = 1 to include worst case. Verify program cycle.
f) Allow program to cycle 15 minutes.
g) Reset the computer.

2-3.2.2.4 Super Logic Test. Load the test program (Binary #085-000002) as per paragraph 2-3.2.2.2.

a) Place 000077_8 in Console switches.
b) Lift Start switch.
c) Verify computer halts. Press the Continue switch.
d) Program takes less than a second for one complete pass. Allow the program to run for several minutes, then stop the computer.
e) Note the stop location of the computer, and perform a series of single instructions by toggling the Instruction Step switch. Verify PC follows the program (as listed in program documentation).

f) Toggle the Memory Step switch as in step e. Verify PC follows the program (as listed in program documentation).

2-3.2.2.5 Teletype Test II. Load the test program (Binary #095-000015) as per paragraph 2-3.2.2.2.

a) Turn on Punch of TTY.
b) With the TTY in local, depress "Here is" to generate leader.
c) Return on-line and place tape in TTY Reader.
d) Place reader in start position.
e) Place 40_8 in Console switches. Lift Start switch.
f) Program will cycle and type "PASS" on the end of each pass.
g) Allow program to cycle for 5 passes.
h) Reset the computer.
i) Place reader of TTY in "Free" position.
j) Place 45_8 in Console switches and raise Start switch.
k) After teletype starts punching data, place leader of tape in TTY and push START on TTY reader.
l) Program should cycle for minimum 1 minute.

2-3.2.2.6 Supernova Instruction Timer. Load the test program (Binary #085-000003) as per paragraph 2-3.2.2.2.

a) Set 000003_8 into the Console switches.
b) Lift the Console Start switch.
c) Allow the program to run for several minutes, and verify no teletype type-outs occur. Program has a built-in tolerance of ±20 nanoseconds for the execution time of each instruction tested and will print out the time of any instruction exceeding this limit.
d) Depress Console Stop switch.
e) Set 000002_8 into the Console switches.
f) Lift the Console Start switch.
g) Starting at location 000002_8 causes the program to type out the execution time for each instruction in nanoseconds.
h) If excessive execution time was detected during step c above, contact the Data General representative in your area or our Field Service Department.
i) If step c was completed successfully save the listing of instruction execution times generated during step g. This listing should be filed as part of the maintenance record for the Supernova. Typical instruction execution times (within ±20 μsec) for the Supernova are listed below.

INSTRUCTION EXECUTION TIMES	
MOV 0,0	801
ADD 0,0	801
AND 0,0	800
LDA 0,0	1599
STA 0,0	1599
ISZ 0	1798
DSZ 0	1798
JMP .+1	801
JSR .+1	1399
LDA 0, @0	2396
LDA 0, @21	2596
LDA 0, @31	2596
LDA 0, @(GO)	3194
DIA 0,0	2895
DOA 0,0	3293
INTA 0	3694
SKPBN 0	2895
DIVIDE	6982
MULTIPLY	3891

2-3.2.2.7 Power Shutdown Test (No Power Monitor). Load test program (Binary #095-000013) as per paragraph 2-3.2.2.2.

a) If Supernova has Power Monitor option perform paragraph 2-3.2.2.8 instead of these procedures.
b) Set 000002 into Console switches.
c) Lift Console Start switch.
d) Program should type "Turn the computer off. Turn the computer on and start at location 40." Follow instructions on typewriter.
e) Restart at location 40_8. Program should type "No interrupt detected on power shutdown."
f) Turn computer off and then on and restart at 40_8. Observe computer cycles when restarted. Further restarts at location 40 should not cause typeouts.

2-3.2.2.8 Power Shutdown Test (with Power Monitor). Load test program (Binary #095-000013) as per paragraph 2-3.2.2.2.

a) Set 000002 into Console switches.
b) Lift Console Start switch.
c) Program will type instruction to turn off computer and restart at 40_8. Follow instructions on teletype.
d) Restart system. Program should type "Lock the console and pull the plug, then restore power."

e) Follow instructions on typewriter. Further tests will not issue messages.

2-3.2.2.9 Exerciser. Load test program (Binary #095-000012) as per paragraph 2-3.2.2.2.

a) Set Console switches to 000002.
b) Lift Console Start switch.
c) Computer will cycle. Any Halt constitutes error. After one pass raise Console switches 2 and 3.
d) Turn on TTY punch. Set reader switch to FREE.
e) After TTY starts punching data, place leader in TTY read station.
f) Push START on TTY.
g) Allow computer to cycle for five minutes.
h) Lower Console switches 2 and 3 to terminate teletype test.

This test completes the start-up checkout for the Supernova Computer.

2-3.3. Repacking.

In order to properly repack the Supernova or the Teletype, reverse the procedures listed in paragraph 2-2. Only strict adherence to the particulars described in each step will prevent serious damage to each machine during shipment. All retaining hardware and packing should be replaced into the original positions within the carton before the units are shipped. The following special packing considerations must be observed for the Teletype:

a) Make sure (3) hex head screws are replaced in the original position underneath the Shipping Pallet.
b) The Console front switches and keyboard must be protected with some form of resilient packing or extensive damage will occur during shipment.

SECTION III

OPERATION

3-1. GENERAL.

This section identifies and describes all of the manual controls and indicators used to operate the Supernova Computer. A description of the Supernova Controls and indicators is also provided in paragraph 2.7 of the "How to Use the Nova Computers" reference manual. Figure 3-1 is a drawing of the Supernova operator's Console showing the controls and indicators referenced throughout this section.

3-2. CONSOLE CONTROLS.

Used in conjunction with a teletypewriter and peripheral devices, the control console contains all controls necessary to operate the Supernova Computer system. Each console control is described briefly in the following paragraphs.

3-2.1 Power Switch.

The key-operated power switch controls the ac (primary power) input to the Supernova power supply. In the OFF position, the ac high side of the input line is removed from the Supernova power supply. In the ON position, there is ac power to the Supernova power supply and the Computer is operational. In the LOCK position there is ac power to the power supply and the computer is operational. However, all Console Control switches are disabled except for the power switch itself. The LOCK position allows a program to run without interference from occasional or accidental "switch diddling" or any other unscheduled attempts to operate the Computer. However, the Console Data switches remain operational to allow the operator to supply information to the program (when requested by the program). It should also be noted that all of the Console indicators remain operational when the power switch is in the LOCK position. The Console key can only be removed when the power switch is in the LOCK position.

3-2.2 AC0, AC1, AC2 and AC3 Deposit/Examine Switches.

These four switches are used both for depositing data into the corresponding Accumulator, and examining their contents. The DEPOSIT position of any switch operates in conjunction with the relative positions of the (16) Console Data switches. Lifting any one of the four AC switches to the DEPOSIT position will load the configuration of the Console Data

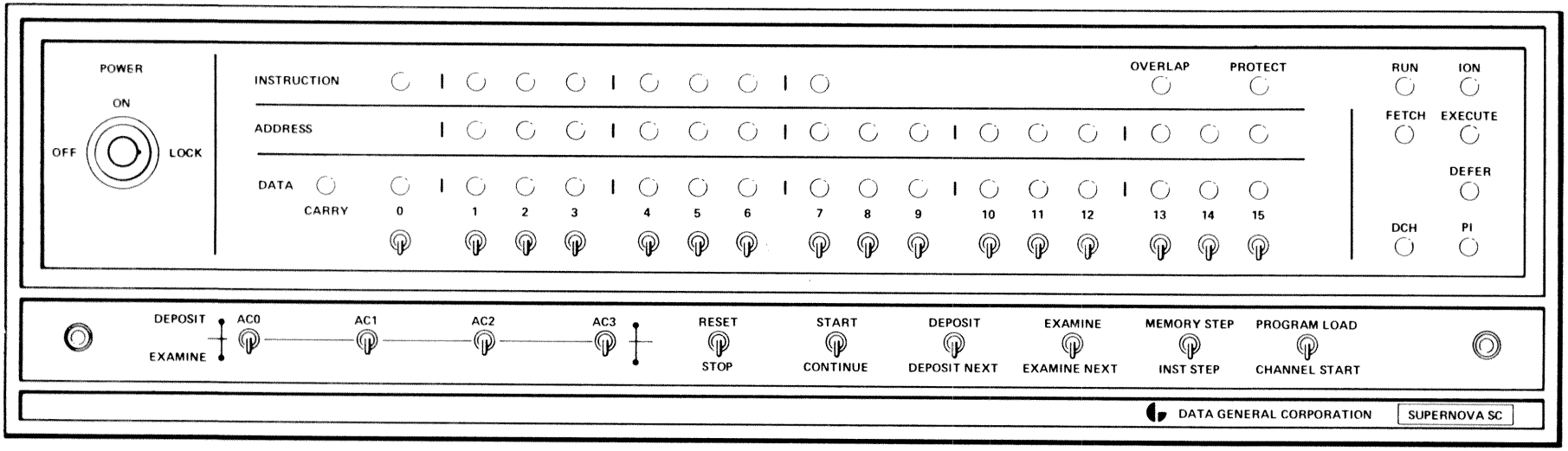

Figure 3-1. Supernova Operator's Console

switches into the specified Accumulator. Pressing any one of the four AC switches to the EXAMINE position will display the contents of the specified Accumulator in the Console DATA lights.

3-2.3 Reset/Stop Switch.

Lifting the RESET/STOP switch to the RESET position causes the Supernova to stop at the end of the current processor cycle. RESET also: clears flags in all I/O devices, clear Interrupt On, Places the processor in supervisor mode, and sets the clock to line frequency. Pressing the RESET/STOP switch to the STOP position causes the Supernova to stop before fetching the next instruction. Thus the processor finishes the current instruction, and then stops with the instruction lights displaying the instruction, unless a device is waiting for data channel access or a program interrupt, in which case it performs all such operations before stopping with the instruction indicators off. The address indicators point to the next instruction. If the current instruction contains an infinitely long indirect addressing chain or there are continuous data channel requests, pressing STOP will not stop the computer. Under these conditions it may be necessary to lift the switch to RESET rather than pressing it to the STOP position.

3-2.4 Start/Continue Switch.

Lifting the START/CONTINUE switch to the START position causes the Supernova to load the address contained in the data switches into PC light FETCH and RUN, and begin normal operation by executing the instruction at the location specified by the PC. Pressing the START/CONTINUE switch to the CONTINUE position causes the Supernova to turn on the RUN indicator and begin normal operation in the state indicated by the (seven) indicators on the right hand side of the Console (i.e., RUN, ION, FETCH, etc.) It should be noted that instruction stepping can be performed by lifting START while pressing STOP on.

3-2.5 Deposit/Deposit Next.

Lifting the switch to the deposit position will deposit the contents of the data switches in the memory location specified by the address lights. Upon completion of the deposit the data lights display the word deposited. Pressing the switch to the DEPOSIT NEXT position will add 1 to the PC address displayed in the address lights and deposit the contents of the data switches in the memory location specified by the incremented address. At completion the data lights display the word deposited. This switch is generally used in conjunction with the Examine/Examine Next switch. See paragraph below for an example switching sequence utilizing both switches.

3-2.6 Examine/Examine Next Switch.

Lifting the switch to the EXAMINE position will load the address contained in the data switches into PC (which is displayed in the address lights) and display the contents of the addressed location in the data lights. Pressing the switch to the EXAMINE NEXT position will add 1 to the PC address displayed in the address lights and display the contents of the location specified by the incremented address in the data lights. The Deposit/Deposit Next, Examine/Examine Next switches can be used for a sequence of operations on consecutive memory locations. The sequence must begin with EXAMINE to supply the initial address unless PC already points to the right location. Suppose we set the data switches to octal 100 initially. Then the following sequence of switch settings produces the effects listed.

EXAMINE	Display location 100.
EXAMINE	Display location 101.
EXAMINE NEXT	Display location 102.
DEPOSIT	Load data switches into 102.
EXAMINE NEXT	Display location 103.
DEPOSIT	Load data switches into 103.
DEPOSIT NEXT	Load data switches into 104.
EXAMINE NEXT	Display location 105.

It should be noted that the EXAMINE position can be used to load the PC for beginning any single step procedure.

3-2.7 Memory Step/Inst Step Switch.

Lifting the switch to the MEMORY STEP position will perform a single processor cycle in the state indicated by the lights and then stop. At completion the lights indicate the next state to be executed. The address lights display PC: the data lights display the address for the next memory step.

CAUTION

Using the AC switches between memory steps within an instruction usually destroys information (in the Accumulator) necessary for the execution of the rest of the instruction. To use the various examine and deposit switches between instruction steps, simply remember what PC is and restore it before continuing. Pressing the switch to the INST STEP position will begin operation in the state indicated by the lights but then stop as though STOP had been pressed at the same time. If the stop occurs at the end of an instruction, the data displayed by the

data lights depends on the instruction as follows.

LDA, STA	Operand
ISZ, DSZ	Operand
JMP	Effective address
JSR	Address loaded into AC3 (old PC + 1)
Arithmetic and logical	Unshifted result
In/out	Zero

Note that the AC switches can be used between instruction steps without requiring any readjustment.

3-2.8 Program Load/Channel Start Switch.

Lifting the switch to the PROGRAM LOAD position will read 33 words from the device selected by data switches 10-15 into locations 0-40, then light RUN and begin normal operation at location 40. Pressing the switch to the CHANNEL START position will issue a DIAS to the device selected by data switches 10-15, store JMP 377 in location 377, then light RUN and begin normal operation by executing the instruction at location 377.

NOTE: For proper channel operation, the device selected by the data switches must be initiated for reading by the combination of the I/O reset and the DIAS issued by the processor. Moreover it is up to the device to stop the transfer after 256 words have been read. The I/O reset clears the location and word counters in the channel interface of the device so the transfer begins at location 0, but since the word counter is also zero the transfer will continue and fill all of memory unless the device stops it. The disk is designed to read exactly 256 words; the magnetic tape stops at the end of the record and it is therefore up to the programmer to write a record of the proper length in the first place.

3-3. CONSOLE INDICATORS.

The Supernova Console indicators are composed of three (register driven) indicator strings and nine individual (flip-flop driven) function indicators. The three

indicator strings are displays for the (8 most significant bits of the) INSTRUCTION register, the ADDRESS (or present contents of the PC), and the DATA content of a memory location or an Accumulator. The nine function indicators indicate the operation state of the Supernova. A brief description of each display is presented in the following paragraphs.

3-3.1 Instruction Display.

This section of the Console displays the 8 most significant bits of the IR register and should change on each new Fetch cycle.

3-3.2 Address Display.

This section of the Console displays the present contents of the PC. When performing an EXAMINE, this display should be indentical to the Address configuration set into the Console Data switches.

3-3.3 Data Display.

This section of the Console can display either the contents of any one of the four Accumulators, or display the contents of a memory location. For example, during an EXAMINE, the selected (by the Console Data switches) address will be displayed by the ADDRESS indicators, and the contents of the selected memory location will appear in the DATA display. However, during a MEMORY STEP the DATA indicators display the address for the next memory reference.

3-3.4 Operational Indicators.

When any indicator is lit the associated flip-flop is in the 1 state or the associated function is true. A few indicators display useful information while the processor is running, but most change too frequently and are therefore discussed in terms of the information they display when the processor has stopped. Each functional indicator is listed below with its indicative interpretation.

RUN	The processor is in normal operation with one instruction following another. When the light goes off, the computer stops.
ION	The program interrupt is enabled (this is the Interrupt On flag).
FETCH	The next processor cycle will be used to fetch an instruction from memory.
DEFER	The next processor cycle will be used to fetch an address word in an indirectly addressed memory reference instruction.

EXECUTE	The next processor cycle will be used to reference memory for an operand in a move data or modify memory instruction.
DCH	The next processor cycle will be used by the data channel for direct access to memory by an in/out device.
PI	The next processor cycle will be used to start an interrupt by storing PC in location 0.
OVERLAP	Arithmetic and logical class instructions are being executed out of read-only memory and the processor is overlapping the execution of one with the fetching of the next. (This light is always off when the computer stops.)
PROTECT	The processor is in user mode. See Memory Allocation and Protection description in the "How to Use the Nova Computers" reference manual.

FETCH, DEFER, EXECUTE, DCH and PI are the state indicators: they specify the state (the type of cycle) the processor will enter if operations are continued by pressing the CONTINUE or MEMORY STEP switch. No light lit among the state indicators on the Supernova Console is equivalent to FETCH. Unless otherwise indicated, use of any operating switch leaves the processor ready to enter the fetch state.

SECTION IV

THEORY OF OPERATION

4-1. INTRODUCTION

This section contains detailed information describing the functional relationships of the major logic sections comprising the Supernova computer. This section is essentially a continuation of the general function description of the Supernova provided in paragraph 1-2.1 of this manual. It is pointed out here that this text is intended to familiarize personnel with the functional operation of the major Supernova logic sections, hence, the descriptions presented in this section are designed to provide basic conceptual information concerning the operation of the Supernova. In this regard it is suggested that Figure 4-1 (Supernova Detailed Functional Block Diagram) be referenced along with the Supernova logic diagrams (bound into Section VII of this manual) while reviewing the descriptions of this section.

The Integrated Circuits of the Supernova are operationally synchronized with the CPU Clock (CLK) signal. The clock timing is arranged such that when the required enabling signals are present simultaneously with the negative-going edge of the CPU CLK signal, the corresponding logical operation will occur. Detailed information concerning the pin nomenclature and the signal requirements of the Supernova IC packages is provided in Appendix A of this manual. The IC package referenced in this discussion are identified by their particular package number (such as a E67). Each IC package number is listed in Table 5-1 with the corresponding manufacturer's part number. This number may be referenced in Appendix A to find the pin nomenclature and signal data for that particular package.

4-2. DETAILED FUNCTIONAL DESCRIPTION

The discussion presented herein will consider the operation of the major logic sections of the Supernova relative to performing the following basic operations: turn-on initialization of the Supernova, Deposit, Examine, and Fetch. The drawing numbers of the Supernova logic diagrams of the major logic sections are listed below with their titles as a convenient reference.

CONSOLE	001-000060
CPU-1	001-000033
Processor & Memory Timing	(Sheet 1 of 3)
Input/Output	(Sheet 2 of 3)
Console Logic	(Sheet 3 of 3)
CPU-2	001-000047
Decoding-IR-States	(Sheet 1 of 2)
Adder-Multiplexer Register/Load Controls	(Sheet 2 of 2)
CPU-3	001-000035
Sel & Reg Drive Logic	(Sheet 1 of 5)
Major Registers Gating-Adder Bits 0-15	(Sheets 2 thru 5)
4K MEMORY	001-000029
Flippers	(Sheet 1 of 5)
MA & MB Register	(Sheet 2 of 5)
Sense & Inhibit	(Sheet 3 of 5)
X Selectors	(Sheet 4 of 5)
Y Selectors	(Sheet 5 of 5)

4-2.1 Turn-On Initialization

Power is applied to the Supernova by turning the Console key to the ON position. As shown on the Console logic diagram, setting the key to the ON position switches 115 VAC high into the Supernova power supply. After power has been turned on, the power supply produces the + and - 5 volt logic power along with the + VMEM and + VINH voltages for the memory. The power supply contains precision differential circuitry which monitors the + 5 volt, + VMEM, and + VINH voltage outputs. These circuits will produce a + O. K. logic signal to indicate the + 5 output level is correct and a MEM O. K. logic signal to indicate the + VMEM and + VINH voltage levels are correct. The power supply also contains a Power Failure (PWR FAIL) monitor circuit which is used in conjunction with the Power Monitor and Auto-restart option for the Supernova. Two half-wave lamp voltages, + 28 V ϕ1 and + 28 V ϕ2 are also produced. in the power supply. These signals represent half-wave rectifier outputs of each side of the power transformer secondary winding. These two lamp power lines split the Console indicator lamp load between the two phases (ϕ1 and ϕ2).

The + 5 O. K. and MEM O. K. lines carry signals from the power supply to the Console Logic section on CPU-1. When power is first turned on, the + 5 O. K. line provides a

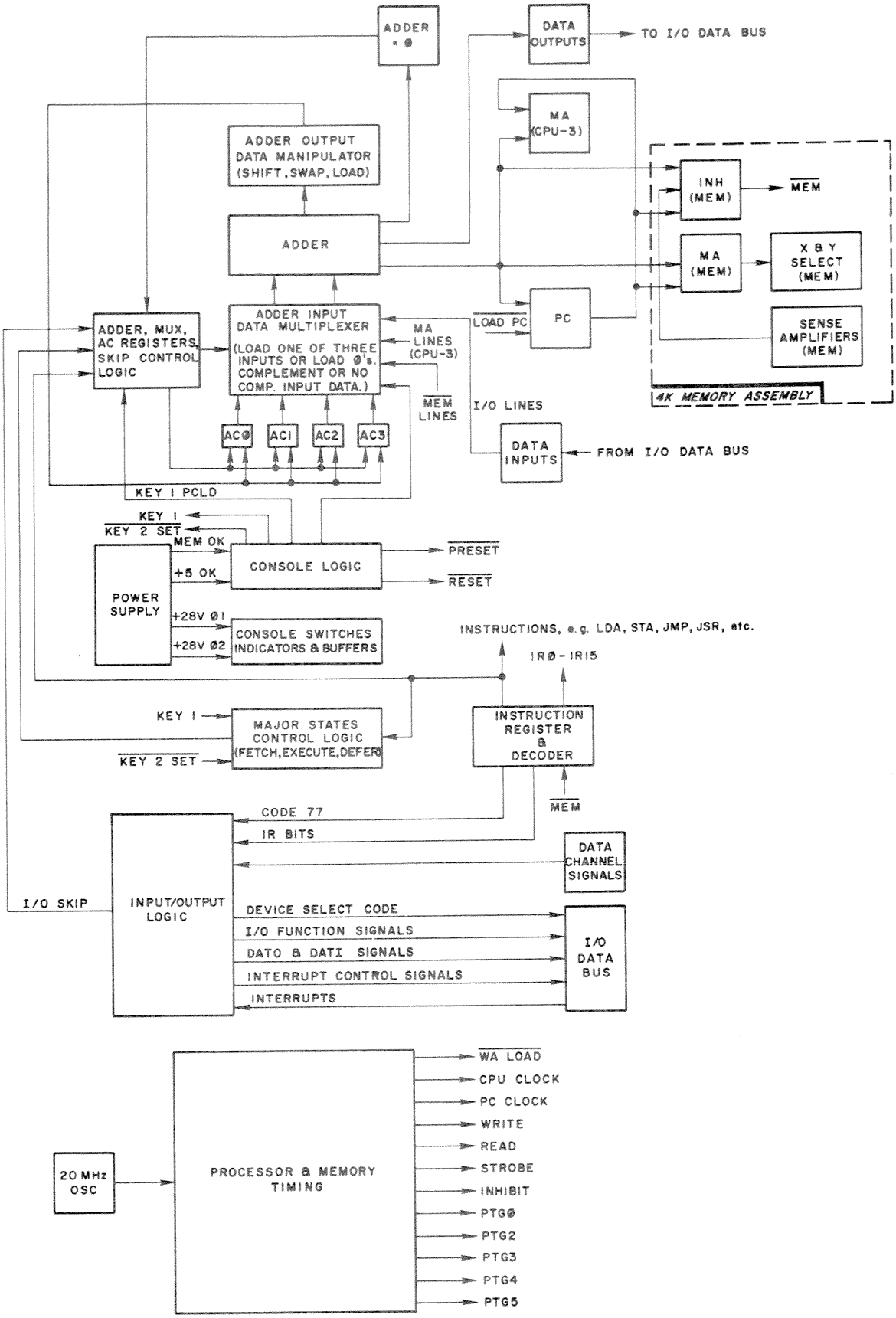

Figure 4-1. Supernova Detailed Functional Block Diagram

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positive transition (to approx. 5 volts) if the + 5 volt output is at the proper level. This positive transition is gated into a differentiating capacitor to produce a pulse which in turn drives the RESET and PRESET gates. $\overline{\text{RESET}}$ and $\overline{\text{PRESET}}$ initializes the control logic of the Supernova in preparation for operation. It will be noted (on the Console Logic diagram) that the $\overline{\text{RST}}$ (Reset) line from the Console is OR gated with + 5 O. K. and MEM O. K. Since $\overline{\text{RST}}$ becomes low when the Console Reset switch is actuated, the Positive-going trailing edge (caused by releasing the switch) of $\overline{\text{RST}}$ is differentiated to generate the $\overline{\text{RESET}}$ and $\overline{\text{PRESET}}$ signals. Hence, the Console Reset switch may also be actuated to initialize the Supernova. In its low state, $\overline{\text{RST}}$ also enables an OR gate (E87) which in turn sets the Stop Sync flip-flop on the next CPU CLK pulse. Setting Stop Sync enables a logical 0 OR gate (E79) the output of which causes the outputs of the two gates (E99 & E100 driving the inputs of the 4 Bit Shift Register) to switch low. The inputs to the 4 Bit Shift Register (E81) are loaded into the Shift Register every $\overline{\text{PTG}}$ 5 time (during time state 3). Therefore, with Stop Sync set, the RUN SET line into the 4 Bit Shift Register is low, and the next PTG 5 to occur will load a zero into the RUN stage of the register. This places a logic 0 level on the RUN output line from the Shift Register which prevents the processor from cycling into Time State 0 (TS0) and likewise stops the next memory cycle.

However, to return to the discussion concerning the $\overline{\text{PRESET}}$ and $\overline{\text{RESET}}$ functions, $\overline{\text{RESET}}$ also drives the Master Reset (MR) input of the 4 Bit Shift Register (E81) and unconditionally clears all of the outputs including RUN to the zero state. Hence, the main reason Reset ($\overline{\text{RST}}$) is bi-functional (i.e., sets Stop Sync at the zero level and generates $\overline{\text{RESET}}$ and $\overline{\text{PRESET}}$ on the zero-to-one transition) is to allow the processor to stop synchronously with the completion of the last instruction, thereby allowing the program to be continued from the last instruction when the processor is started again. It should be noted that since there is contact bounce in the switch - the $\overline{\text{preset}}$ action will occur before the switch is released but after the attempted synchronous stop.

One of the important functions of $\overline{\text{PRESET}}$ is to reset the clock timing chain in the Processor & Memory Timing section. This section contains the Clock Oscillator and timing chain (C1-C4) which generates the Processor timing signals (PTG0, PTG2 thru PTG5). ($\overline{\text{PTG5}}$ is instrumental in starting the computer.) At this point the Supernova logic is initialized and waiting for the actuation of a Console control switch as the next operational step. (It should

be noted that the PTG and CPU CLK signals, $\overline{\text{RESET}}$ and $\overline{\text{PRESET}}$ are universal signals to the Supernova logic. Under these conditions and in the interest of simplicity, the block diagram shows only the points of generation for each signal rather than its multitude of terminal points.)

4-2.2. Examine and Deposit.

The operational step after the Supernova has been initialized may be either to toggle in a small program at the Supernova Console, or to command an automatic program load at the Supernova Console. To simplify the discussion at this point it will be assumed that a single instruction loop is to be toggled in (e.g., deposit zero in location 000000 vis-a-vis jump .LOC0). This is accomplished by clearing the all of the Console Data switches to the (down) zero position, lifting the Examine switch, then lifting the Deposit switch. The Examine switch output, $\overline{\text{EX}}$, becomes true when the switch is actuated. EX in the zero state produces signals EX + STRT, KEY 1 PCLD, and EX + EXN + DP + DPN, of which the latter is gated through E99 and E82 and triggers off a Schmitt trigger at E106. At this time $\overline{\text{RUN}}$ will be high (Processor not running) and together with the output from the Schmitt will set the Manual Function flip-flop. The set output from Manual Function sets the Key Seen flip-flop. The trailing edge of the Schmitt (E106) resets the Manual Function flip-flop when the key is released triggering a second Schmitt (also E106) used as a delay. The set output from Key Seen (in the high state) allows the next CPU CLK pulse to set the Key Start flip-flop. The function of the latching network (2 Schmitts and 1 flip-flop) just described is to verify that the Key Seen flip-flop is set once and only once for each Console switch actuation. Without this network, a Console switch released very slowly or not released at all, would appear to be multiple switch actuations to the Key Start logic.

With the Key Start flip-flop in the set state, the reset output ($\overline{\text{KEY START}}$) will enable the load gate (E100) of the 4 Bit Shift Register. Since $\overline{\text{PTG5}}$ is not present $\overline{\text{KEY START}}$ will load a logic 1 into the Key Sync stage of the Shift Register. ($\overline{\text{PTG5}}$ = 1 and $\overline{\text{KEY START}}$ =0 loads KEY SYNC with a 1.) The logic 1 KEY SYNC enables the Shift (SH) control input for the Register so that the next CPU CLK pulse shifts the Register right once, setting the RUN stage of the Shift Register. RUN sets turns on the Console RUN indicator and releases TS0. The CPU CLK pulse that shifted a 1 into the RUN state of the Register also shifts a 1 into the KEY 1 stage of the Register. This operation is facilitated by the DS (Serial Data Entry) input of the

Register which is tied to + 3 volts, and shifts it (as a logic 1) into the first stage of the Register. Signal KEY 1 is gated with KEY 1 PCLD in the Adder-Multiplexor-Register Load-Controls section of CPU-2. Both signals in the high state will enable gate E62H (during TS0 time) and produce a $\overline{\text{LOAD PC}}$ signal. This signal is transmitted to the PC register section of CPU-3 (Major Registers Gating-Adder), where in the zero state it enables the parallel entry (PE) control of the PC Register.

The data flow during the Examine operation is from the Console Data switches through the Adder out through the Memory Buffer Output (MBO) gates onto the parallel inputs of the PC Register. Several signals are necessary to implement this particular data path. These signals are $\overline{\text{CON OUT}}$ and $\overline{\text{ADDER OUT}}$. $\overline{\text{CON OUT}}$ is produced by gate E19 at TS0 time with KEY 1 and EX + STRT (Examine OR Start) present in the logic 1 state. $\overline{\text{CON OUT}}$ drives an OR gate in the SEL & REG Drive Logic to produce a D-R-L-S signal for the Adder input multiplexor. Gate E46 also in the SEL & REG Drive Logic produces a D-R-E enable signal by virtue of the fact that the $\overline{\text{ACD OUT}}$ and $\overline{\text{EIS OUTPUT}}$ signals (not revelent to an Examine operation) are not present. D-R-L-S and D-R-E enable the ADDER input multiplexor to "look" at the Console Data switch lines $\overline{\text{CON0}}$ thru $\overline{\text{CON15}}$. This data passes through the multiplexor onto the "Y" inputs to the Adder. The other output lines from the multiplexor driving the "X" inputs into the Adder would all be in the zero state by virtue of the fact that none of the conditions for producing the required X multiplexor enable signals would be present during the Examine Operation. Hence, the Console data is added to 0 in the Adder and passes through unchanged. The outputs from the Adder are gated out from the Adder bus by the ADDER OUT signal generated by gate E16B of the Adder-Multiplexor Register Load-Controls section of CPU-2. E16B is an AND gate which keeps the ADDER OUT line high if all of its inputs are high. The inputs to E16B are controlled by a group of gates which sense certain unique conditions when it is necessary to inhibit the Adder output. In the case of our present example the ADDER OUT line will be lowered (to disable the Adder output gates) at $\overline{\text{TS3}}$ time of the KEY 1 cycle. Therefore, both $\overline{\text{CON OUT}}$ and $\overline{\text{LOAD PC}}$ are generated at TS0 time of an Examine cycle causing the Console Data to be loaded through the Adder into the PC Register.

At this point it is worthwhile to digress slightly to consider the construction of the Adder. The Adder is a 16 bit parallel adder with an Input Data Multiplexor and an Output Data Manipulator. The Input Data Multiplexor actually consists of two separate multiplexors,

one driving the "X" input lines of the Adder, and the other driving the "Y" input lines of the Adder. The outputs of each of the four Accumulators (AC0-AC3) are connected in parallel to both the X Data Multiplexor and the Y Data Multiplexor. This allows any Accumulator output to be either the source Accumulator or the destination Accumulator. From the point of view of generating multiplexor control pulses, the Y multiplexor is defined as the Destination Accumulator, and the X multiplexor is defined as the Source Index Accumulator. The MA (processor MA) and $\overline{IO}$ (Data bus inputs) inputs are connected to the X multiplexor, and the $\overline{CON}$ (Console) and $\overline{MEM}$ (from Buffer Register in the Memory Assembly) inputs are connected to the Y multiplexor. Therefore, MA and $\overline{IO}$ will always be source input selected, and $\overline{CON}$ and $\overline{MEM}$ inputs will always be destination selected.

The X multiplexor is divided again into two sections, defined as left and right. Likewise the Y multiplexor is also divided into a left and right section. Each section is enabled by high signals applied to pins 7, 8, and 9 of the multiplexor IC package. However, the outputs from both (left and right) sections are common to the corresponding X or Y input of the Adder, and normally only one section is enabled at a time. For example, if AC0 is to be the source input (X multiplexor) then the right X multiplexor section is enabled, and the left X multiplexor section is disabled. For another example, if the outputs of the Console switches are to be selected as the destination input (Y multiplexor) then the right Y multiplexor section would be enabled, and the left Y multiplexor section would be disabled. The converse of this would be true if AC2 was selected as the destination Accumulator.

Signals applied to pins 16 and 17 of each multiplexor IC package are decoded (in the package) to simultaneously select 4 of the 12 input lines. Decoding and selection is performed in a straightforward manner, i.e., pin 16 a "0," pin 17 a "1" selects input pins 3, 6, 21, & 18. Pin16 a "1," and pin 17 a "0" selects input pins 2, 5, 22, & 19. Pins 16 and 17 both a "1" selects input pins 1, 4, 23 & 20. Therefore, the control logic must first determine which halves of the source and destination multiplexors will be enabled, then it must determine which register is to supply data to the Adder and thus generate the unique 2 bit code for pins 16 and 17 to select the proper (4) input pins. The input Data multiplexor can also perform a complementing function by applying a high level to pin 15 of the IC package. All of control signals for each multiplexor are generated in the Sel & Reg Drive Logic section. The logic of this section decodes command signal functions such as $\overline{CON\ OUT}$ or $\overline{MEM\ OUT}$ to generate

the proper enabling-selecting-or complementing signals for the multiplexors. These signals have single letters, functioning as a form of short-hand for the name of the signal function. A few examples are listed as follows:

SX COM	= Source X Index input, Complement
SX-L-E-A	= Source X Index input-Left-Enable A
SX-L-E-B	= Source X Index input-Left-Enable B
SX-L-H-S	= Source X Index input-Left-High-Select
SX-L-L-S	= Source X Index input-Left-Low-Select
D-L-E-A	= Destination-Left-Enable A
D-L-E-B	= Destination-Left-Enable B
D-R-H-S-M	= Destination-Right-High-Select-Most Significant Bits
D-R-H-S-L	= Destination-Right-High-Select-Least Significant Bits

The control pins for the input Data Multiplexor are defined as follows:

Pin 15 - on a "1" - Complement multiplexor output
Pin 7, 8, 9 on a "1" - Enable multiplexor section
Pin 16 & 17
0 0 = Zero multiplexor section outputs
0 1 = Select data on input pins 3, 6, 21, 18
1 0 = Select data on input pins 2, 5, 22, 19
1 1 = Select data on input pins 1, 4, 23, 20

The Adder outputs feeding the four Accumulators are gated through a Data Manipulator is code selected to either shift, swap, or normally load (no manipulation) the Adder output data into one of the Accumulators. The Data Manipulator is essentially a (2 bit) code selected multiplexor input wired so that under the proper SEL X and SEL Y signal code Adder output data will be loaded into the Accumulator shifted 1 bit to the left, shifted 1 bit to the right, or as swapped bytes. The codes and manipulations thereof are listed as follows:

SEL X	SEL Y	
0	0	= Load AC Normally
1	0	= Load AC Shifted Right 1 Bit
0	1	= Load AC Shifted Left 1 Bit
1	1	= Load AC with Bytes Swapped

It will be noted that CARRY SET is connected into the Data Manipulator for the shift right function with the byte bits crossed connected (8-15 to 0-7 and 0-7 to 8-15) for the swap function.

To return to the Examine Operation, the Examine Cycle, like many other Key (Console Control switch) cycles requires a minimum of two cycles to complete the operation. The first cycle is labeled KEY 1, and in the case of Examine KEY 1 loads Console Data into the PC and then loads PC into the Memory Address Register in the Memory assembly. Signal $\overline{\text{MA LOAD}}$ loads the contents of the PC on the $\overline{\text{MBO}}$ lines into the Memory Address Register. The contents of the PC are gated out by signal PC OUT generated by gate E16B of the Adder-Multiplexor Register Load-Controls section of CPU-2. In the KEY 1 mode ADDER OUT and PC OUT are made mutually exclusive by $\overline{\text{TS3}}$. Hence, PC OUT is produced at Time State 3 while ADDER OUT is inhibited. The other signal required is $\overline{\text{MA LOAD}}$ which is derived in the Processor & Memory Timing section for this example) from MEM CY SET, C4 and TS3 (along with a logic 1 $\overline{\text{TS0}}$). MEM CY SET is produced in CPU 2 (Decoding-IR-States section). This gate produces MEM CY SET at all times except when the AND condition is sensed on anyone of its four input gates. C4 is equivalent to PTG5 or tail end of TS3, and the other requirement is the fact it is TS3 time and not TS0 time. Figure 4-2 is a timing diagram showing the relationships of the CPU Clock, PTG, and C2, C3, C4 signals during a non-memory cycle, i.e., memory is not accessed such as during KEY 1.

One of the last operations during PTG5 is to strobe the RUN Shift Register and the Major States Control Register. PTG5 enables the load inputs of both registers. In the case of this example signal KEY 2 SET would be present at gate E49 of the Decoding-IR-States section of CPU-2. ($\overline{\text{KEY 2 SET}}$ was produced by gate E101 of the Console Logic when KEY 1 went high. In this instance KEY 1 and the fact the Key actuated was not Cont + Inst + Mstp + Strt or a Restart signal will produce $\overline{\text{KEY 2 SET.}}$) The output of gate E49 (with $\overline{\text{KEY 2}}$ SET present) will place a high signal on the input to the KEY 2 stage of the Major States Control Register. When $\overline{\text{PTG5}}$ occurs this bit will be loaded initiating the KEY 2 cycle. During the KEY 2 cycle the memory will be allowed to run and read the contents of the location whose address was loaded into the Memory Address Register (Memory Assembly) on the end of the KEY 1 cycle. On the last part of the KEY 2 cycle the data read out from memory will be loaded from the memory assembly buffer register, through the Adder and into the Processor MA Register. The outputs from the MA Register enable the indicators in the Console Data display. A brief description of the logical operations performed by the KEY 2 cycle is provided in the following paragraph.

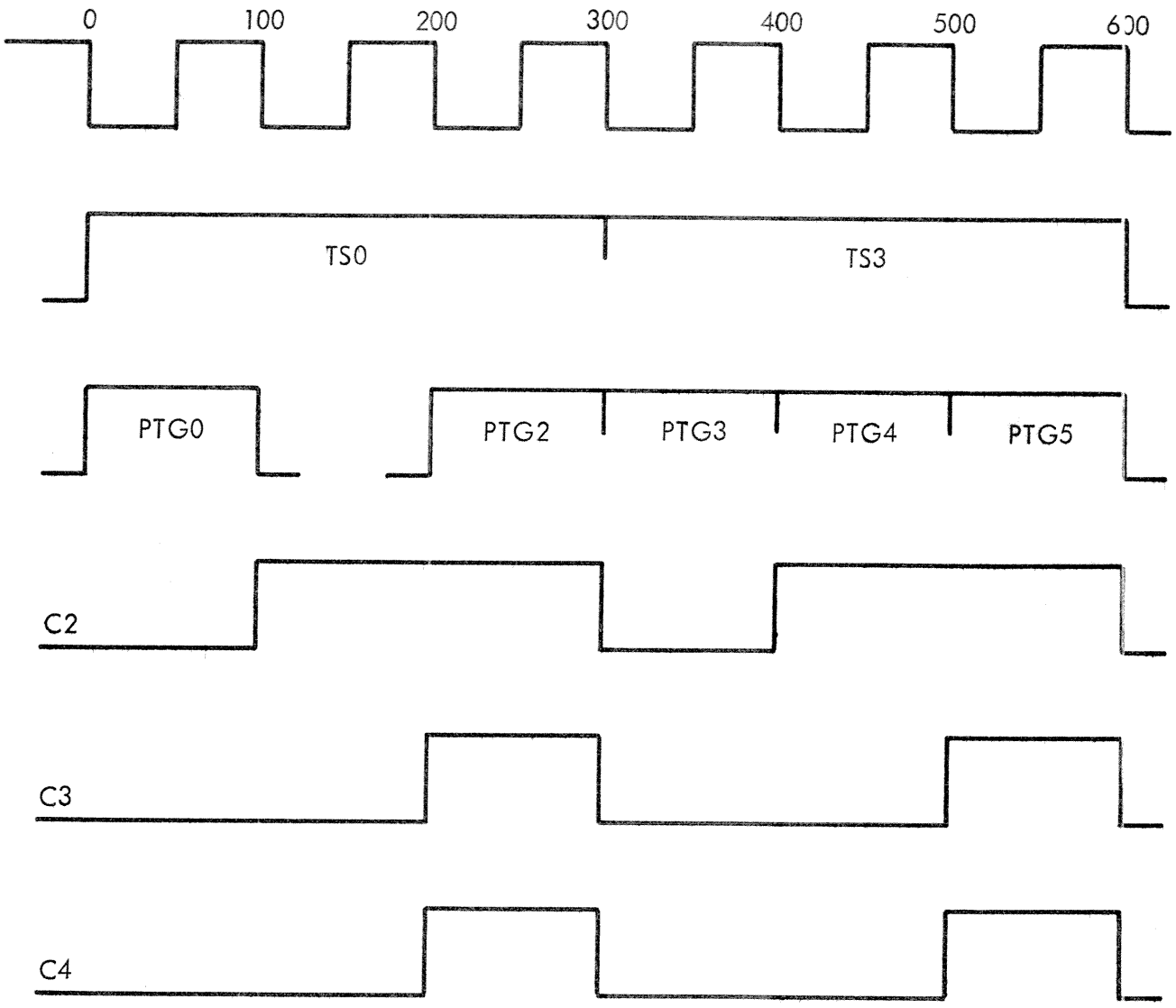


Figure 4-2. Timing Diagram of a Cycle with No Memory Access

As mentioned previously MEM CY SET would be high (during an Examine), RUN SET, and TS0 would also be high, and at PTG5 time gate E61H (Processor & Memory Timing, CPU 1) would provide one of the requirements for setting the Read CY flip-flop (E15). On the next CPU CLK after PTG5 the Read CY flip-flop will become set and start the memory read-write cycle. Figure 4-3 is a timing diagram of the Basic Read-Write Memory Cycle. This memory cycle will access memory for the data contents of the location whose address was loaded into the Memory Address Register during the KEY 1 cycle. After PTG5 the Read CY flip-flop will become set and start the memory read-write cycle. This memory cycle will access memory for the data contents of the location whose address was loaded into the Memory Address Register during the KEY 1 cycle. Memory reading is performed during TS0 of a basic (non-modify) memory cycle, and writing or rewriting is performed during the TS3 time of the same cycle. Under these conditions data is moved from the Inhibit Register (in the Memory Assembly) into the Adder by control pulse $\overline{\text{MEM OUT}}$ generated at TS3 time. (The Inhibit Register functions as a Memory Buffer Register in the Memory Assembly.) $\overline{\text{MEM OUT}}$, generated by gate E6 of the Adder-Multiplexor Register Load-Controls section of CPU-2, is derived from the KEY 2, TS3, and EX + EXN + DP + DPN signals. These functions indicate a $\overline{\text{MEM OUT}}$ signal is required (at TS3 time) if the KEY 2 operation is an Examine, or Examine Next, or Deposit, or Deposit Next. $\overline{\text{MEM OUT}}$ at the logic 0 level produces an ACD RIGHT HI SEL MSB signal in the SEL & REG Drive Logic section of CPU-3. This signal is short-hand coded D-R-H-S-M, and enables the Adder Input Data Multiplexor to place the $\overline{\text{MEM 0}}$ thru $\overline{\text{MEM 7}}$ signals on the 8 most significant Adder "Y" input lines. D-R-H-S-L is also generated to place MEM 8 thru MEM 15 on the 8 lease significant Adder "Y" input lines.

With $\overline{\text{MEM0}}$ thru $\overline{\text{MEM15}}$ input to the Adder, two other signals, ADDER OUT and LOAD MA, are necessary to complete the Examine operation. ADDER OUT is produced by gate E16B (Adder-Multiplexor Register Load-Controls of CPU-2) because of the false state of the following signals: FETCH SET (not in fetch), FETCH + PI 2, KEY 1, JSR, $\overline{\text{PL READ IO}}$, PI 1, and $\overline{\text{MBO INH}}$. The LOAD MA signal is produced automatically by gate E17H (Adder-Multiplexor Register Load-Controls of CPU-2) on every $\overline{\text{PTG5}}$ pulse. Hence, ADDER OUT gates the memory data from the Adder bus out onto the inputs to the (Processor) MA Register, where LOAD MA transfers the data into the MA Register. The MA Outputs are connected into

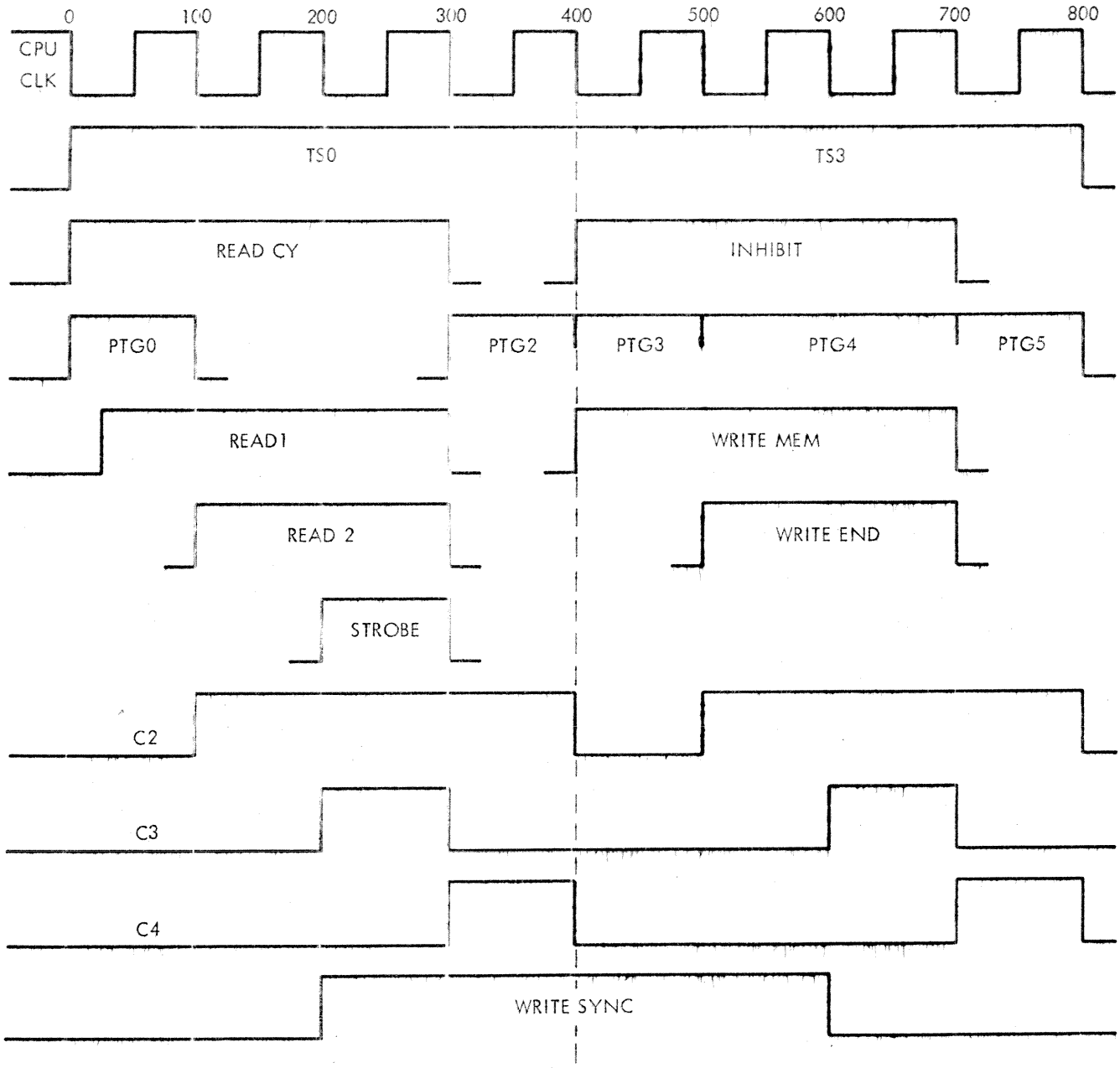


Figure 4-3. Timing Diagram of Basic Memory Cycle

gates generating the $\overline{IND}$ signals for the Console display. These gates are controlled by the ϕ1 IND DRIVE and ϕ2 IND DRIVE signals from the Console Logic sections of CPU-1. These signals allow the output data signals appearing on the $\overline{IND}$ lines to be alternately switched between the MA and PC Register outputs (and MA0 and CARRY). These signals are phased with + 28 V ϕ 1 and + 28 V ϕ 2 signals at the Console to alternately illuminate the various indicator rows on the Console. The data output gated by the ϕ 1 IND DRIVE signal (at the Adder) is in phase with the + 28 V ϕ 1 signal driving the Console indicators. Likewise, the data output gated by the ϕ 2 IND DRIVE signal (at the Adder) is in phase with the 28 V ϕ 2 signal driving the Console indicators.

The Deposit function operates similar to the Examine as far as the KEY detection logic is concerned. However, the DP + DPN (Deposit or Deposit Next) gating in the Console Logic section of CPU-1 also generates a KEY 2 MEM MOD signal. This signal will modify the memory read-write cycle during the KEY 2 cycle of the Deposit. The only KEY 1 operation of the Deposit function is to transfer the contents of the PC Register into the (Memory Assembly) Memory Address Register. This is performed by signal $\overline{MA\ LOAD}$ (when PTG5 occurs) exactly as described above for Examine.

During the KEY 2 cycle of the Deposit, gate E19 (Adder-Multiplexor Register Load-Controls) generates a $\overline{CON\ OUT}$ logic 0 signal. This gate is enabled at $\overline{TS0}$ time of the KEY 2 cycle with the DP + DPN signal present. All three signals present (TS0·KEY2·DP+DPN) enables CON OUT. CON OUT, in the low state, produces a D-R-L-S signal (in the SEL & REG Drive Logic of CPU-3) gating the Console Data switches into the Adder. The Adder OUT signal (from the Adder-Multiplexor Register Load-Controls section of CPU-2) gates the output of the Adder (in this case Console switch data) onto the $\overline{MBO0}$ thru $\overline{MBO15}$ lines to the Memory Assembly. This data is clocked into the Inhibit/Buffer Register (of the Memory Assembly) by a signal derived from MB LOAD. MB LOAD occurs during the memory modify cycle, and is produced by gate E69B of the Processor & Memory Timing section of CPU-1. Figure 4-4 is a timing diagram of the Memory Modify Cycle. KEY 2 MEM MOD (mentioned earlier) along with KEY 2 produce a MEM MOD signal (E64). MEM MOD is gated with the CPU CLK and $\overline{C4}$ (through an OR gate) to generate MB LOAD at E69B. MB LOAD is transmitted to the Memory Assembly where it is gated with SELECT (to verify it is the proper Memory assembly addressed) and the $\overline{RELOAD\ DISABLE}$ input (which is reserved for special

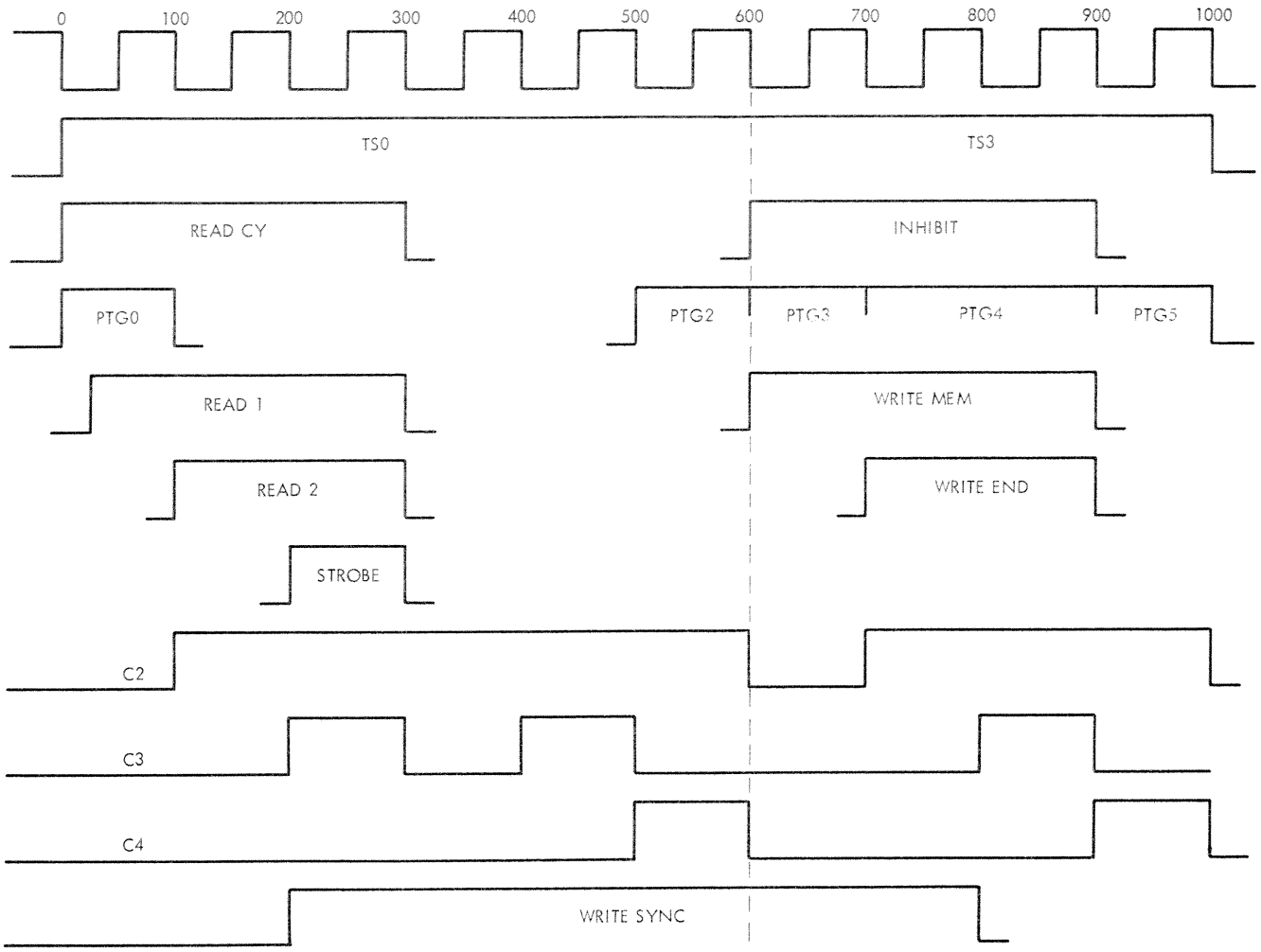


Figure 4-4. Timing Diagram of the Memory Modify Cycle

applications and is normally high). The output of this gate generates a clock input, loading the data on the $\overline{\text{MBO0}}$ thru $\overline{\text{MBO15}}$ lines into the Inhibit/Buffer Register. Normally, on a non-modify memory cycle the Inhibit/Buffer Register is loaded with the data read out of memory and data is written back into core through its inhibit function. However, on a modify memory cycle the contents of the Inhibit/Buffer Register are copies instead from the Adder output lines, and subsequently written into core.

During TS3 of the KEY 2 portion of the Deposit operation a $\overline{\text{MEM OUT}}$ signal is produced (by gate E6 of the Adder-Multiplexor Register Load-Controls section of CPU-2). MEM OUT transfers the data on the $\overline{\text{MEM0}}$ thru $\overline{\text{MEM15}}$ lines (from Memory) through the Adder and into the (Processor) MA register exactly as previously described for the Examine Operation. At the end of the KEY 2 cycle the RUN stage of the 4-Bit Register is reset but the KEY 2 stage of the Major States Register remains set.

4-2.3 Fetch.

All of the Supernova logic operations are shown diagramatically on Drawing 001-000061 bound in Section VII of this manual. The path of any particular flow on each chart may be traced through to determine the sequence of logical operations comprising any machine cycle. A Console Key (or switch) must be actuated in order to set the Supernova logic to the RUN state. Specifically, the starting Memory Address of the program to be run is loaded into the Console Data Switches, and then the Start switch is lifted. The processor will perform a Start (STRT) KEY 1 cycle in the same manner as that described for the Examine Operation. However, after the contents of the PC Register are loaded into the MA Register (in the Memory Assembly) the coincidence of $\overline{\text{PTG5}}$ with the negative-going edge of CPU CLK will load the Fetch stage of the Major States Register. MEM CY SET will be high at this time and with RUN SET, PTG5 and $\overline{\text{TS0}}$ in the logic 1 state, the next CPU CLK will set the READ CY flip-flop (Processor & Memory Timing of CPU-1) starting the memory read-write cycle of the Fetch. During PTG0 of the Fetch, gates E54 and E55 (Adder-Multiplexor Register Load-Controls section of CPU-2) develop a set input for flip-flop E52. On the next CPU CLK Pulse, E52 generates an INC PC pulse which increments the PC Register. The contents of Inhibit/Buffer Register are loaded into the Instruction Register (IR) of CPU-2 at PTG2 time. This section, Decoding-IR-States of CPU-2, loads the word read out of memory into the IR and decodes the IR bits to determine which instruction is to be performed.

ALC instructions are performed during the fetch cycle and contain provisions for setting control logic for skipping the next instruction. The next instruction is skipped depending on previously defined results of performing the ALC, e.g., skip on zero Accumulator. The ALC SKIP flip-flop essentially remembers that the (previously defined) conditions for skipping the next instruction were detected, and during the next fetch, the instruction accessed from memory is ignored. Operationally, the ALCSKIP logic is located in the Adder-Multiplexor Register Load-Controls section of CPU-2. The ALC SKIP flip-flop (E22) is set by the output from gates sensing the ALC SKIP instruction and the ADDER = 0 signal from the Adder logic. Setting the ALC SKIP flip-flop establishes the flow path that the next Fetch will follow. During the flow of the next fetch, ALC SKIP flip-flop is cleared and the PC + 1 is loaded into the Memory Address Register. This skips the execution of the next instruction. The exit from the ALC SKIP path is called F COM, and is a route to either Fetch (if no DCH or INT is pending) or to DCH (if DCH is Pending) or to PI (if INT is pending) or to HALT (if RUN stage is reset). There are five major paths after fetching non-skipping instructions; Multiply, Divide, Jump, JSR, E FA, IO class, and ALC. Multiply and the IO class instructions are extended fetch cycle instructions. The fetch cycle can end with the Major States Register being set to either the EXECUTE state of the DEFER state as well as F COM. The DEFER state is entered when the instruction requires an indirect memory reference for the actual operand. Flow through the DEFER path is modified depending on whether the instruction is Indexed or not. At TS3 if the deferred instruction is a JSR and not indirect, the contents of the Inhibit/Buffer Register in memory is stored into AC3 and the contents of the PC are loaded into the Memory Address Register in the memory assembly. If the deferred instruction is an LDA + STA + ISZ + DSZ + JSR (direct) the Major States Register will be set to the EXECUTE state. If the instruction is a JMP direct the flow will exit to F COM. Other indirect instructions will recycle through the DEFER path.

During the EXECUTE Major State, if the instruction is an LDA, memory is run and the contents of the Inhibit/Buffer Register are loaded into the destination Accumulator. The EXECUTE cycle is also extended for I/O instructions. If the instruction is an STA the contents of the ACD are loaded into the Inhibit/Buffer Register. The last operation for both the STA and LDA paths is to load the PC into the MA and exit via F COM. Each EXECUTION flow exits to F COM. The various instruction flows along with the PI (program interrupt) and

DCH (Data Channel) paths shown on the Supernova Flow Chart may be operationally examined relative to the actual signal mechanisms shown on the Supernova logic diagrams.

Timing diagrams of the IO Fetch and IO Execute, Execute STA, ROS (Read Only Storage) and OVLAP, and ROS and no OVLAP have been included here for reference purposes. Figure 4-5 is a timing diagram of the IO Fetch applicable to NIO, DOA, DOB and DOC instructions. Figure 4-6 is a timing diagram of the IO EXECUTE applicable to NIO, DOA, DOB and DOC instructions. Figure 4-7 is a timing diagram of the EXECUTE STA (with no STROBE). Figure 4-8 is a timing diagram of ROS with OVLAP. Figure 4-9 is a timing diagram of ROS without OVLAP.

4-2.4 Memory.

Drawing No. 001-000029, bound in Section VII of this manual is a 5 sheet logic drawing of a single 4K Supernova Memory Assembly. The timing for one or more Memory Assemblies is provided by the Processor & Memory Timing section of the Supernova CPU-1 (Drawing No. 001-000033, sheet 1). As shown on the logic drawing for this section, the Memory Timing logic is driven by the CPU CLK signal, which is the same pulse used to synchronize logical operations in the Supernova Central Processor. The timing waveforms for all Supernova Memory Operations are shown on Drawing No. 001-000062 (bound into Section VII of this manual).

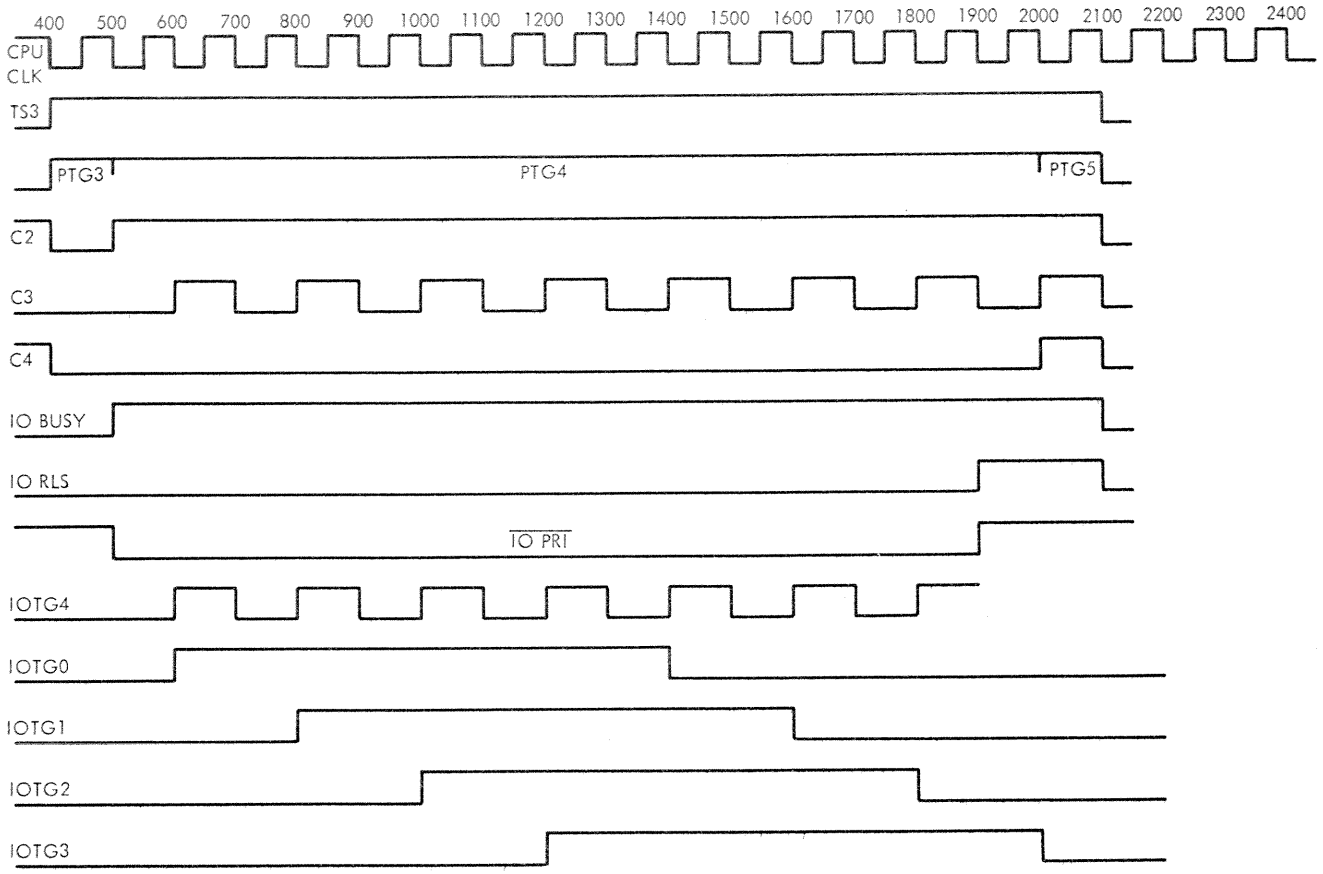


Figure 4-5. Timing Diagram of IO FETCH

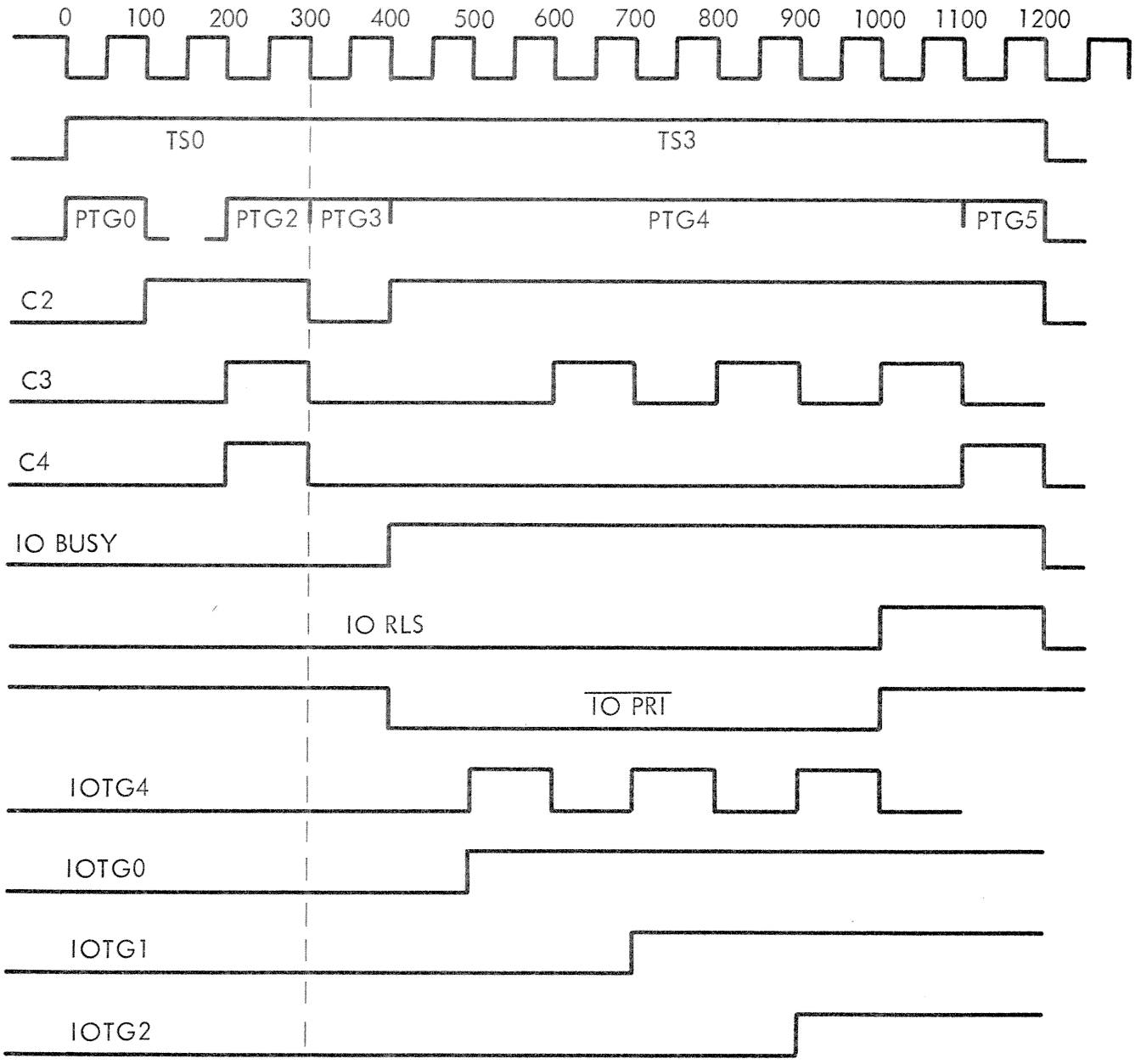


Figure 4-6. Timing Diagram of IO EXECUTE

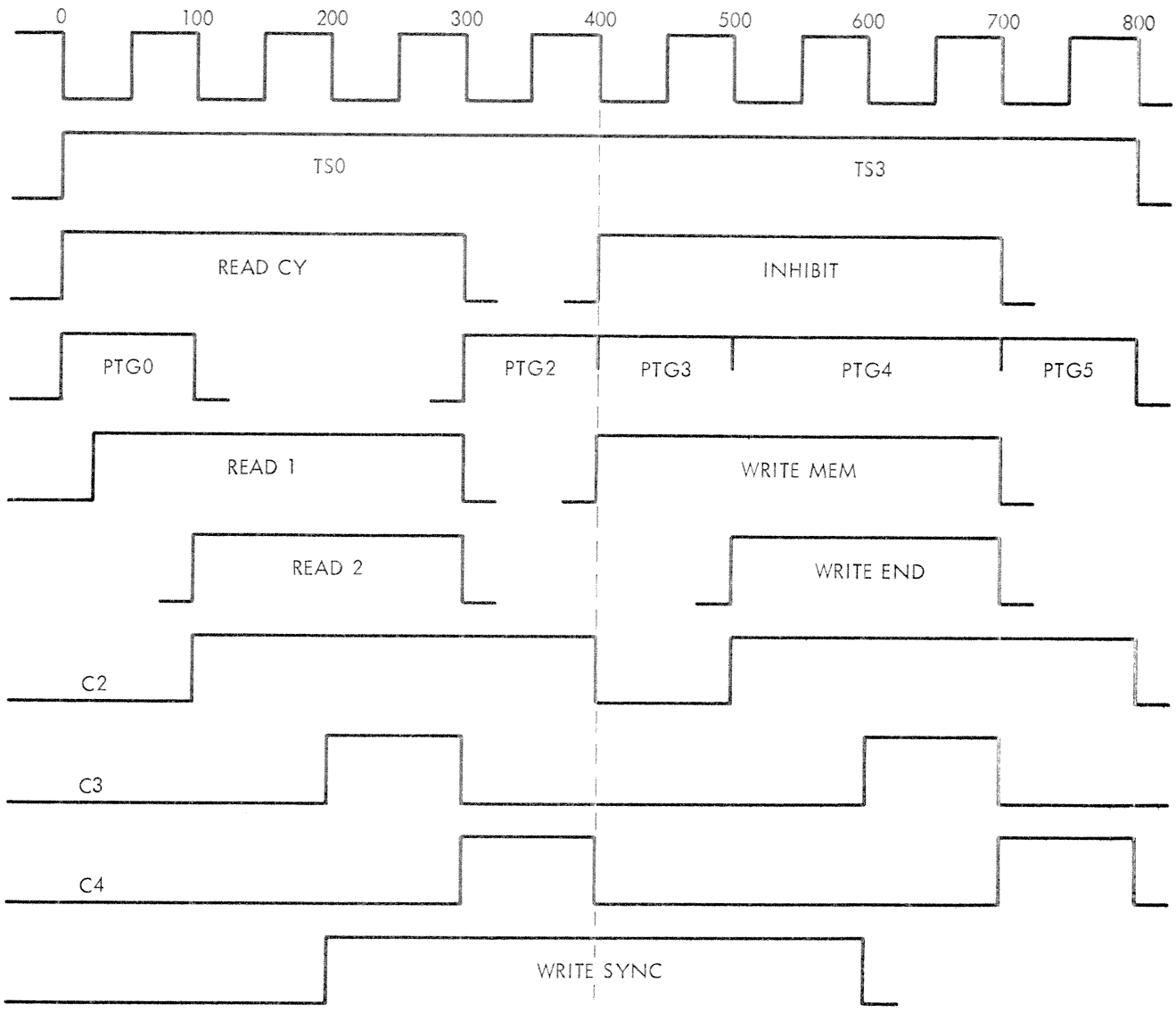


Figure 4-7. Timing Diagram of EXECUTE STA

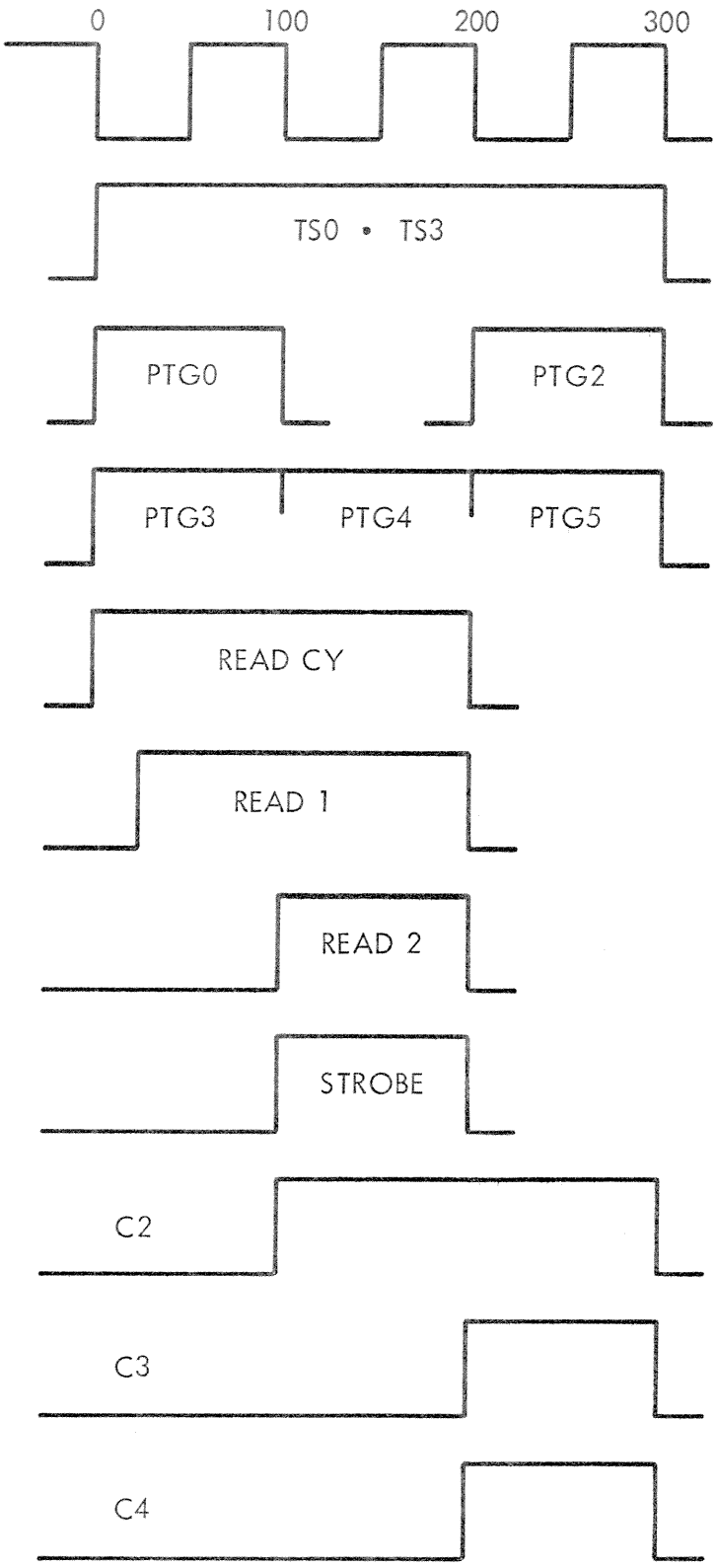


Figure 4-8. Timing Diagram ROS with OVLAP

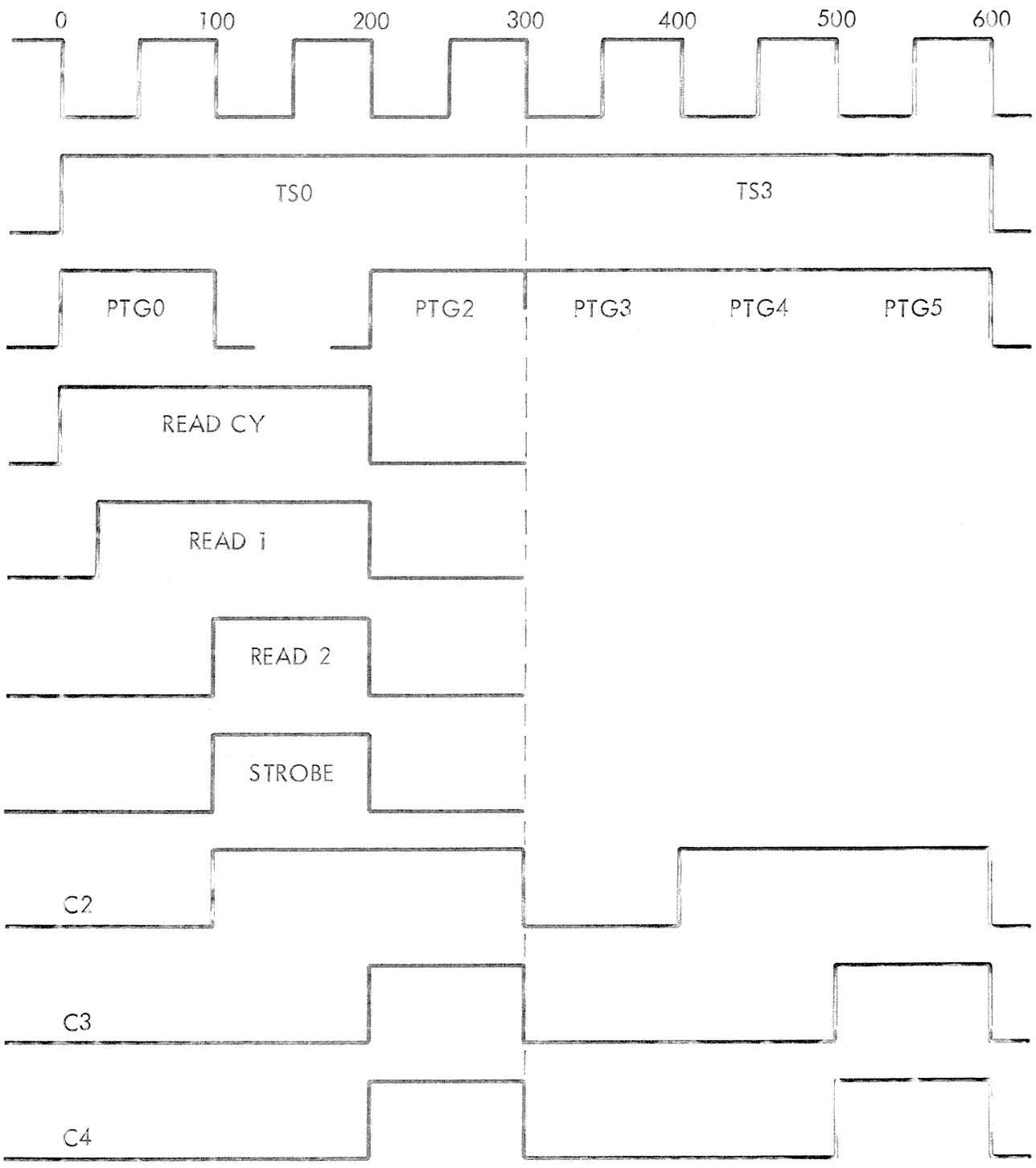


Figure 4-9. Timing Diagram ROS without OVLAP

Each memory cycle is started whenever the input gating conditions for setting the Read CY flip-flop are satisfied, e.g., RUN SET, PTG 5, $\overline{TS0}$ (on a 1), and MEM CY SET. (Other conditions are also available for starting a memory cycle, e.g., $\overline{KEY2}$(CONT + MSTP + ISTP), MEM CY SET, and KEY SYNC.) The input gating supplies a set level (logic 1) input to the READ CY flip-flop (Processor & Memory Timing, CPU-1) so that the next CPU CLK will set it. The set output from the Read CY flip-flop controls two gates. One gate generates the $\overline{READ\ 1}$ Memory Control pulse, while the other generates the $\overline{MB\ CLEAR}$ memory control pulse. Both pulses occur simultaneously but $\overline{MB\ CLEAR}$ is terminated when the READ 2 flip-flop becomes set (on the next CPU CLK). $\overline{MB\ CLEAR}$ clears out the memory Inhibit/Buffer Register prior to receiving the output from the memory Sense Amplifiers. The logic 0 output from the READ CY flip-flop (in the set state) enables the set input of the Read 2 flip-flop, so that READ 2 will set on the next CPU CLK pulse. The logic 0 output from READ 2 (in the set state) enables the set input of the WRITE SYNC flip-flop so it will set on the next CPU CLK. The logic 0 output from WRITE SYNC (in the set state) enables the set input of the INHIB flip-flop, allowing it to set on the next CPU CLK. The last flip-flop in the chain, WRITEEND, is set enabled by the INHIB flip-flop and sets on the next CPU CLK pulse. The set output from WRITE END is tied back to the reset input of the WRITE SYNC flip-flop so that the three flip-flops (WRITE SYNC, INHIB, and WRITE END) all reset on the next two CPU CLK pulses. It should be noted that the READ CY and READ 2 flip-flops are reset enabled when the WRITE SYNC flip-flop becomes set, and both (READ CY and READ 2) flip-flops reset on the next CPU CLK to occur (after WRITE SYNC set). The timing for the Memory Modify is similar with the exception memory data is modified in the Supernova Adder and loaded back into the memory Inhibit/Buffer Register just prior to the memory write cycle. It will be noted that a Sense Amplifier STROBE pulse is not generated during a STA instruction. Since Accumulator data is to be written back into memory it is not necessary to strobe the data sensed during the Read cycle. Deleting the strobe in the instance of the STA instruction saves Sense Amplifier settling time (approx. 200 μsecs). The STROBE pulse is generated by the STROBE flip-flop located in the Processor & Memory Timing section of CPU-1. Gate E51 which senses one set of conditions for generating a STROBE requires READ 2 (flip-flop set), $\overline{DCHIN}$ (on a 1), $\overline{HSC\ BUSY}$ (no high speed channel op present),

$\overline{\text{RELOAD DISABLE}}$ (on a 1), and STA (on a 0). If the other conditions remain the same and STA becomes a 1, the STROBE flip-flop will not become set. The STROBE flip-flop, after being set enabled, will toggle on the next two CPU CLK pulses, i.e., the first CPU CLK will set it, the second will reset it. STROBE cannot come up again until all of the input conditions described above are present at gate E51.

The selection circuitry for the 4K Memory is shown on sheet 2 of Drawing 001-000029, and consists of a jumper selected decode of Memory Address bits MA1, MA2, and MA3. When the proper memory address code is present gate E28 enables OR gate E33 producing $\overline{\text{SELECT}}$ and (through inverters E37) SELECT. The SELECT AND $\overline{\text{SELECT}}$ signals are used extensively throughout the memory logic as primary enabling signals. The address SELECT coding facilitates the addition of multiple 4K assemblies to the Supernova Configuration. Also shown on sheet 2 of Drawing 001-000029 are the MA (Memory Address) Register. The INH Register referred to as the MB (Memory Buffer) Register in the title Block of this drawing acts primarily as a buffer register for data flow in and out of memory. Data presented on the $\overline{\text{MBO0}}$ thru $\overline{\text{MBO15}}$ lines can be loaded into either register. MBO data is loaded into the MA by a $\overline{\text{MA LOAD}}$ signal from the Processor & Memory Timing section of CPU-1. MBO data is loaded into the INH Register by the MB LOAD signal also from the Memory Timing section of CPU-1. In the case of MB LOAD, it generates a clock pulse for the J and K inputs of the INH Register being driven (through inverters) by signals on the MBO lines. The outputs of the INH Register are gated out to the $\overline{\text{MEM0}}$ through $\overline{\text{MEM15}}$ lines for transmission back to the Adder section of the Processor. The INH Register is driven by two unconditional inputs, an $\overline{\text{MB CLEAR}}$ which clears the register to the reset state, and the $\overline{\text{SNS0}}$ thru $\overline{\text{SNS15}}$ output lines from the Sense Amplifiers. The $\overline{\text{SNS}}$ lines set the INH Register up to the configuration of the word read out of memory (after INH has been cleared).

The 4K X and Y Selectors are shown on sheets 4 and 5 of Drawing 001-000029. MA bits 4-9 are decoded to select the "Y" Source (YRS) and Return (YRR) drivers. MA bits 10-15 are decoded to select the "X" Source (XRS) and Return (XRR) drivers.

The Supernova uses a 3-wire memory in which the X and Y drive windings use bidirectional current polarities for reading and writing. Each X and Y threads through a plane of cores in such a way that every X winding intersects with a single Y winding at 16 core locations. Inhibit and sense windings thread through planes of cores so that each winding

intersects every location at the same bit. The two sets of switches at the right on sheet 1 of Drawing 001-000029 establish current paths to and from the X and Y windings in the selected memory. The lines at the right of the lower set are the current source and return lines for the X windings. RXR should be regarded as being connected through a resistance to some positive voltage, whereas RXS should be regarded as being connected through a resistance to ground. In the read part of the cycle, the left pair of switches connect the read source line to RXR and the read return line to RXS. Similarly for writing, the right pair connect the write source to RXR and the write return to RXS. The X and Y windings and associated selection logic are shown on sheets 4 and 5 of Drawing 001-000029. In each of the matrices a single winding is driven by turning on one switch in the group at the left of the matrix and one switch in the group below the matrix; this allows current to pass through only that winding that is connected to the two "on" switches. Consider the selection of the Y winding for location 0. MA is clear so the Y selection signals YRS00 and YRR0 are generated, turning on the switches associated with them. For read, a current path is established from the Y READ SOURCE through the upper diode at YRS00, through the winding at the left end of the bottom row, through the leftmost diode at YRR0, and through the switch to the Y READ RETURN. For write, the source and return wires are connected to the opposite switches so that current flows in the opposite direction. The path is from the Y WRITE SOURCE through the diode just at the left of the YRR0 switch, through the rightmost diode at that switch, through the winding at the left end of the bottom row, through the YRS00 switch, and the lower diode at that switch to the Y WRITE RETURN. In both read and write, half of the drive current is applied to an X winding and half to a Y winding so that a full drive current is applied to the core location at which the windings intersect. For read, the direction of the current is such that all the cores are driven to the 0 state. Hence any cores that were 1, change state, producing pulses on the sense windings threaded through those planes. These pulses, through the Sense Amplifiers, shown on sheet 3 of 001-000029, set individual bits of the INH Register. For write, the drive current is applied in the opposite direction and thus tends to drive all the cores in the selected location to the 1 state. But flip-flops in the INH Register that contain 0's enable inhibit drivers shown on sheet 3. Hence inhibit current that opposes the X and Y drive current is applied to those planes corresponding to 0's in the word to be written. In the selected location the X and Y drive currents, therefore, change the states

of only those cores that correspond to 1's in the data.

The Resistor Board shown in phantom on sheet 1 of Drawing 001-000029 is physically located underneath the Supernova Console/Enclosure Chassis. This board mounts the precision resistor terminations for memory currents. The components on the Resistor Board are electrically connected between memory and the Supernova power supply. See Drawing 001-0000101 (bound in Section VII of this manual) for a schematic of the Supernova Resistor Board. The RINH0 thru RINH15 current lines (shown on sheet 3 of Drawing 001-000029) are also terminated at the Resistor Board. (RINH stands for Resistor connection for INHibit driver.) The three power supply connections to the Resistor Board are + V MEM, + VINH, and GRD.

4-2.5 Input/Output.

The Basic IO Control for the Supernova is shown on Drawing 001-000070, titled IO BUS RECEIVERS & COMMON SELECT. The Bus Receivers for the Teletype input, Teletype output, Paper Tape Reader, Paper Tape Punch, and Real Time Clock are located on this drawing along with the priority chain and common select decode. The operation of this logic along with descriptions of the operation of the Busy and Done logic is presented in Appendix A of the "How to Use the Nova and the Supernova" or the "How to Use the Nova Computers" reference manual. This section also contains an example description of the operation of the Paper Tape Punch Control. Drawing 001-000071 shown the logic of the Teletype Control. The teletype keyboard (or reader) is defined as the TTI device (Teletype In), while the printer (OR punch) is defined as the TTO device (Teletype Out). Timing for the teletype transmissions is generated by an Oscillator driving a 4 bit count-down. The frequency of the crystal used in the oscillator depends on the Baud rate selected by the customer. However, the frequency of Y2 can be calculated by multiplying 128 X Baud Rate. Both input and output teletype transmissions use shift registers to handle the serial transmission of teletype characters. The upper register receives input from the incoming line. The logic in the upper left detects the start bit (space), prevents the receiver from responding to a transient on the line, and controls shifting so that each bit is read in the middle of its period. The lower register receives a character from the bus and supplies it serially to the output line with the necessary start and stop bits. As the character goes out, the register fills with 1's allowing the net at the left to determine when transmission is complete.

SECTION V

MAINTENANCE

5-1 PERIODIC INSPECTION.

The Supernova has very few mechanically operational components, hence it requires a negligible amount of mechanical inspection. Any lubrication schedules are confined to any mechanically operational peripherals used with the Supernova, e.g., card punch, line printer, tape punch or reader, etc. The Supernova Console switches should be checked periodically for proper operation and switch spring tension. The Console indicators of the various displays should also be observed to detect any burned out indicators. The Static Tests described in paragraph 2-3.2.1 of this manual may be performed to check out the Console controls and indicators.

5-2 PREVENTIVE MAINTENANCE.

It should be pointed out that it is impossible to compile a schedule of Preventive Maintenance routines which will satisfy the requirements of all customer applications. The routines outlined in this paragraph may be scheduled against two critical factors: the minimum down-time that can be tolerated by the installation, and the periods of least activity when these procedures may be performed. Obviously these two factors will vary from installation to installation, however, the smaller the minimum down-time becomes, the more frequent preventative maintenance is required, and this must be distributed over the periods of least activity.

IO devices, because of their general mechanical nature, benefit the most from a scheduled preventative maintenance program. In addition a certain percentage of malfunctions can be detected while in the process of occurring. Diagnostic routines should play a major role in preventive maintenance programs. Suggested items that should be included are as follows:

a) Diagnostics - Run exerciser daily for a reliability check of the entire system. All other diagnostics should be run at least once weekly.

b) IO devices - Clean daily, removing the dust that normally accumulates as the device is used. Check for excessive vibration, overheating of bearings, and signs of excessive mechanical play or wear. Check punch and teletype belts for wear and fraying. Empty the punch chad box and remove chad from within the device itself. Clean the type face of the teletype. Look for and remove excess oil and grease from within the devices.

c) General - Check all power and IO cables for fraying or wear. Check all plugs and connectors; tighten if necessary. Check the cooling fans on either end of the computer power supply removing lint and dust as necessary.

d) Lubrication - Following the lubrication schedules as set forth in the IO device pamphlets. This requirement is perhaps the most important phase of a preventive maintenance program.

5-3 SPECIAL TOOLS AND TEST EQUIPMENT.

The following is a list of special tools and test equipment recommended for efficient maintenance of the Supernova.

MULTIMETER	SIMPSON MODEL 260 OR EQUIVALENT
OSCILLOSCOPE	TEKTRONIX 453 OR EQUIVALENT
LONG LEAD PROBES	TEKTRONIX P6010-10X OR EQUIVALENT
CURRENT PROBE	TEKTRONIX P6022 OR EQUIVALENT
EXTENDER BOARD	DGC 107-000007-02
WIRE WRAP TOOL (24 GAUGE)	GARDNER DENVER Model 14AX2 OR EQUIVALENT
IC TEST CLIP	MANUFACTURED BY A P INC. Cleveland, Ohio (part no. 923700)
SOLDERING IRON	WELLER ISOLATED MODEL W-TCP OR EQUIVALENT

5-4 DIAGNOSTIC PROGRAMS.

The Supernova Diagnostics are individual programs which together test all logical operations of a Supernova system. Individually the programs test various logic areas of the computer and IO. The majority of the diagnostic routines are capable of diagnosing malfunctions down to the Logic Level. The diagnostics provide a means of measuring the performance of the system on a repeatable basis. Copies of diagnostic tapes as well as individual program documentation are part of the software package delivered with the Supernova. Individual program documentation provides information as to operating procedures, error interpretation, console switch settings and logical areas tested. Certain diagnostics are normally part of the daily and weekly preventive maintenance routines.

SUPERNOVA DIAGNOSTIC PROGRAMS

PROGRAM	DESCRIPTION
Address Test	Routine to test the memory address selection logic.
Checkerboard II	Worst case memory noise test.
Super Logic Test	Gate by gate test of CPU Logic (less IO)
Super Instruction Timer	Routine to test CPU clock logic, prints instruction times of basic Supernova instruction set.
Exerciser	Reliability test - tests CPU logic, TTY Reader, punch, high speed paper tape reader, paper tape punch and real time clock. Halts on error.
Super Teletype Test II	Gate by gate test of TTY logic, PI system and IO Bus logic.
Reader/Punch Test	Routine to test high speed paper tape reader and punch.
Real Time Clock Test	Routine to test Real Time Clock logic.
Power Shut Down Test	Test retention of memory data on power loss. Tests power monitor auto restart option.

5-5 TROUBLE SHOOTING PHILOSOPHY.

Effective trouble shooting is accomplished in a minimum of time by following a series of logical steps. The ultimate aim is to effectively pinpoint the actual problem using all information available. Locating the malfunction is then the next logical step. The following is a suggested plan for effective casualty analysis:

a) Investigation - record the state of the machine on error occurence. Look for obvious symtoms including operator error, loose plugs or connectors, blown fuses or tripped circuit breaker.

b) Isolation - through the use of diagnostic programs or console trouble shooting techniques attempt to isolate the malfunction to a particular board.

c) Component Isolation - Isolate the faulty component using an oscilloscope and short diagnostic loops either toggled in at the console or as part of a diagnostic. Selecting the correct external synch is of importance at this point.

d) Replace the faulty component and retest by running the diagnostic that originally failed.

e) Record for future reference, the symptoms, cause, unique trouble shooting method/s used to isolate the malfunction.

5-5.1 Memory.

Address decoding and data word transfer failures are the types of memory malfunctions most frequently encountered. The inability to store or fetch a word from or into a selected core location is usually an indication of the former while storing or fetching a word which is modified by one or two bits is an indication of the latter. Address test and checkerboard are memory diagnostics designed to verify memory reliability. The two programs will detect and, in most cases, identify the cause of a malfunction. Address test is primarily intended to test address selection logic and verifies the ability to address all core locations. Checkerboard is a worst case noise test designed to detect the picking up or dropping of bits in a data word transfer. In the case of intermittent failures it may be desirable to revert to console troubleshooting, utilizing short closed loop routines which are toggled in. Programs such as the one illustrated below are valuable in resolving failures.

SAMPLE DIAGNOSTIC LOOP PROCEDURE

1. Deposit data word in AC2
2. Deposit program in core
3. Start - Program halts - Load address in console switches and continue

LOC			
0000	063077	DOC 0, CPU	:Halt Inst.
0001	060477	DIA 1, CPU	:Reads Switches
0002	044011	STA 1, 11	:Store Addr
0003	052011	STA 2, @ 11	:Data to Addr
0004	000001	JMP. -3	:Loop

Note: The address can be varied by changing the contents of console switches.

The above routine will store the contents of AC2 (DATA word) into the address in AC1. It is useful in monitoring Read/Write currents and individual Inhibit currents. Two 2K trimpots, located on the circuit board in the power supply provide for the adjustment of Read/Write and Inhibit currents. The trimpot governing Read/Write current varies the value of + VMEM, that governing Inhibit current varies + VINH The nominal value of + VMEM is 21.7 volts, while that of + VINH is 17.2 volts. Read/Write and Inhibit currents are measured with a current probe attached to the appropriate drive current test loop adjustment procedure:

1. Machine running, executing a JMP to itself instruction.
2. Current probe attached on Read X or Y drive current test loop, located on the center left edge of the memory board (with the handle towards the viewer).
3. Adjust trimpot (VMEM) for a nominal value of 390 MA.
4. Repeat for Inhibit, with current probe on any one of 16 Inhibit current test loops adjusting trimpot (VINH) for 740 MA.

CAUTION

These trimpots should only be adjusted by trained service personnel and a record kept of all such adjustments.

Maintenance other than lubrication, minor adjustments and part changes should be performed by DGC personnel or respective manufacturer representatives. Lubrication shoule be performed in accordance with the appropriate manual listed below:

Applicable Manuals

Teletype - Technical Manual
33 Teletype writer sets
Bulletin 310B Volume I

VMEM: 21.9
VINH: 17.06
8/5/77

Fixed { VMEM: 21.90 / VINH 17.50 } 8/4/77

see also p. 1-15

		Technical Manual 33 Teletype writer sets Bulletin 310B Volume II
		33 Page Printer set ASR, KSR and RO Parts Bulletin 1184B
High Speed Punch	-	Technical Manual High Speed Tape Punch Set (BRPE) Bulletin 215B
		High Speed Tape Punch Set (BRPE) Parts Bulletin 1154B
High Speed Reader	-	(Digitronics Model) (2540EP)
		Perforated Tape Reader Operation and Maintenance Manual
Lubricating Materials Teletype - Keyboard		KS7470 (oil) KS7471 (grease)
Typing unit		KS7470 (oil) KS7471 (grease)
Reader		KS7470 (oil) KS7471 (grease) Lupriplate 105
High Speed Punch	-	(BRPE11) KS7470 (oil) 145867 (grease)
High Speed Reader	-	SAELO (oil)
Recommended spares	-	one each
High Speed Reader	-	Lamp incandescent Digitronics TLNBF009 GE (08805) (P/N1638)

5-6 COMPONENT REPLACEMENT.

The replacement of a component requires care to prevent damage to circuit board etch. Clipping a component from the circuit board rather than unsoldering is the preferred method. Excessive heat from a soldering iron may result in damage to the component being replaced. The use of a soldering iron with an isolation transformer, a small copper alligator clip as a heat sink and a delay between the soldering of individual pins of a chip are recommended. With the extender board in use the weight of the board under test should be supported by a non-conductive material. Replacing a console switch or Indicator requires the removal of the console subassembly. The following is the procedure to be followed when replacing a console (Data) switch:

1. Remove the four Allen head screws attaching the console subassembly to the main frame.

2. Remove four Phillip head screws holding the circuit board assembly to the console casting.

3. Remove the power switch and individual knurled nuts from each of the data switches. Separate the front panel from the circuit board.

4. Replace the defective switch and reassemble in reverse order.

To replace a console indicator follow steps 1-3 above and in addition remove two slotted flathead screws holding the Bendolex to the circuit board. Replace and reassemble in reverse order.

5-7 IC IDENTIFICATION.

Table 5-1 is included in this section to facilitate any troubleshooting procedures that require identification between any Supernova IC reference number (E1-En) and the original manufacturer's part number. This list also may be referenced as a bridge between the logic configurations shown on the various CPU logic diagrams and the IC (package) pin definitions summarized in Appendix A of this manual.

Table 5-1. IC Identification List

CHIP	CPU1	CPU2	CPU3	MEMORY(4K)
E1	7474/8828/5610*	9003/8879	8885/MC3002	MC3003
E2	9002/8889*	9008/8848	7438	9016/8H90
E3	9601*	9008/8848	7438	MC3061
E4	MC3061	9008/8848	8885/MC3002	7438
E5	MC3026	9008/8848	7438	MC3061
E6	9009/8859	9008/8848	8885/MC3002	9016/8H90
E7	9009/8859	8271	7438	7475
E8	9009/8859	9016/8H90	7438	9016/8H90
E9	MC3026	8271	8885/MC3002	MC3061
E10	9005/8840	8271	7438	7438
E11	9005/8840	9016/8H90	8885/MC3002	MC3061
E12	9005/8840	8271	7438	9016/8H90
E13	74H55	9005/8840	7438	7475
E14	MC3061	8885/MC3002	8885/MC3002	9016/8H90
E15	MC3061	9002/8889	7438	MC3061
E16	MC3061	MC3026	8885/MC3002	7438
E17	8885/MC3002	74H55	7438	MC3061
E18	9009/8859	9008/8848	7438	9016/8H90
E19	MC3061	9008/8848	8885/MC3002	7475
E20	9301	9002/8889	7438	9016/8H90
E21	9301	8885/MC3002	9005/8840	MC3061
E22	9007	MC3061	8885/MC3002	7438
E23	9009/8859	9008/8848	9002/8889	MC3061
E24	9009/8859	9016/8H90	9316	9016/8H90

*Power Monitor

Table 5-1. IC Identification List (Continued)

CHIP	CPU1	CPU2	CPU3	MEMORY(4K)
E25	9009/8859	9007	9005/8840	7475
E26	9009/8859		9005/8840	MC3026
E27	9009/8859		8271	MC3026
E28	9009/8859	MC3026	9316	9009/8859
E29	9009/8859	9003/8879	9005/8840	MC3003
E30	9009/8859	9005/8840	9005/8840	MC3003
E31	9009/8859	9005/8840	8271	MC3003
E32	9002/8889	MC3061	7438	MC3003
E33	8885/MC3002	9003/8879	9316	MC3026
E34	MC3061	9005/8840	9005/8840	9009/8859
E35	MC3061	9008/8848	9005/8840	MC3026
E36	8885/MC3002	9008/8848	8271	9009/8859
E37	9016/8H90	9008/8848	7438	9016/8H90
E38	9301	8885/MC3002	9316	7524
E39	8885/MC3002	9003/8879	9005/8840	7524
E40	9004/8819	74H55	9005/8840	7524
E41	9003/8879	74H55	8271	7524
E42	9004/8819	74H55	7438	7524
E43	9003/8879	9004/8819	9007	7524
E44	8885/MC3002	9003/8879	9004/8819	7524
E45	9016/8H90	9002/8889	9003/8879	7524
E46	9002/8889	9016/8H90	9002/8889	SH-6405
E47	9005/8840	9301	74H55	TIBC 728
E48	9016/8H90	9016/8H90	9003/8879	TIBC 728

Table 5-1. IC Identification List (Continued)

CHIP	CPU1	CPU2	CPU3	MEMORY(4K)
E49	9003/8879	8885/MC3002	9004/8819	TIBC 728
E50	9002/8889	9008/8848	8264	TIBC 728
E51	9004/8819	8271	8264	SH-6405
E52	9008/8848	MC3061	9309	9301
E53	9005/8840	74H55	9309	9016/8H90
E54	9004/8819	9008/8848	8264	SH-6405
E55	9009/8859	9002/8889	8264	SH-6405
E56	9002/8889	9005/8840	9309	9016/8H90
E57	8271	9008/8848	9309	9016/8H90
E58	74H55	9016/8H90	8264	9301
E59	9007	8885/MC3002	8264	9016/8H90
E60	9016/8H90	MC3061	9309	MC3026
E61	74H55	74H55	9309	9301
E62	74H55	74H55	8264	9301
E63	MC3061	9008/8848	8264	9016/8H90
E64	74H55	8885/MC3002	9309	9016/8H90
E65	9008/8848	9016/8H90	9309	TIBC 728
E66	9009/8859	9003/8879	9005/8840	SH-6405
E67	MC3026	8271	9016/8H90	MC3026
E68	9002/8889	9009/8859	74H55	9016/8H90
E69	MC3026	9004/8819	9016/8H90	SH-6405
E70	MC3061	9005/8840	8260	TIBC728
E71	MC3061	MC3061	8271	TIBC 728
E72	9003/8879		8271	SH-6405

Table 5-1. IC Identification List (Continued)

CHIP	CPU1	CPU2	CPU3	MEMORY(4K)
E73	MC3026		8260	SH-6405
E74	9002/8889		8271	TIBC 728
E75	9005/8840		8271	TIBC 728
E76	MC3061		8260	TIBC 728
E77	9008/8848		8271	TIBC 728
E78	9016/8H90	9016/8H90	8271	TIBC 728
E79	9003/8879	9003/8879	8260	TIBC 728
E80	9016/8H90	9002/8889	8271	TIBC 728
E81	8271	9007	8271	TIBC 728
E82	9004/8819	9007	9008/8848	TIBC 728
E83	9003/8879	8885/MC3002	9002/8889	
E84	9016/8H90	9002/8889	8885/MC3002	
E85	9002/8889		9005/8840	
E86	7474/8828/5610		8264	
E87	9003/8879		8264	
E88	9002/8889		8271	
E89	9016/8H90		8271	
E90	9005/8840		8264	
E91	9005/8840		8264	
E92	8271		8271	
E93	8885/MC3002		8271	
E94	74H55		8264	
E95	9008/8848		8264	
E96	9008/8848		8271	

Table 5-1. IC Identification List (Continued)

CHIP	CPU1	CPU2	CPU3	MEMORY(4K)
E97	9002/8889		8271	
E98	9009/8859		8264	
E99	8885/MC3002		8264	
E100	9002/8889		8271	
E101	9008/8848		8271	
E102	9008/8848			
E103	8885/MC3002			
E104	MC3061			
E105	9002/8889			
E106	SG-83			

5-8 POWER SUPPLY SPECIFICATIONS.

The Supernova power supply provides all of the power required to operate the Supernova Processor logic and memory circuits. The output voltages for the processor logic and memory circuits are regulated. Two 2K trimpots associated with the memory voltage regulators are the only voltage adjustment in the entire supply. The specifications are listed in the five following categories: Identification of Supply Output Circuits, Resistance Readings, Output Voltage Readings, Replacing Power Transistors, Power Supply Internal & External Plug Connections. Each side of the ac power line is fused by a 10 amp, 250 volt tube fuse (bus type). Both fuses are mounted in a 2 pole standard fuse holder which is mounted on top of the power transformer. A circuit breaker controlling the main dc power (+30VNR) in the supply is located mounted immediately behind the power transformer on the top rear chsssis panel. The fuses and circuit breaker should be checked first following any interruption of output power.

5-8.1 Identification of Supply Output Circuits.

All of the power supply output voltages and voltage monitor output signals are listed below with a description of each output and its regulating or amplifying circuit.

Signal	Output	Function
VL	Nonregulated	console lamps $\phi 1 + \phi 2$
+VMEM	Regulated (E7)	Memory READ/WRITE CURRENTS
+VINH	Regulated (E3)	Memory Inhibit current
-5V	Regulated (E4)	LOGIC VOLTAGE, CPU
+5V	Regulated (E8)	LOGIC VOLTAGE, CPU
+5 O.K.	Differential Amplifier (E1)	LOGIC SIGNAL
PWR FAIL	Differential Amplifier (E2)	LOGIC SIGNAL
MEM O.K.	Differential Amplifiers (E5 for + VINH) (E6 for +30 VNR)	LOGIC SIGNAL

5-8.2 Resistive Readings.

All readings taken with a Simpson model 260 or equivalent (RX1-scale)

Reading	Ohms
AC line to AC line	Inf
AC line to chassis	Inf
AC gnd to chassis	0
+5 to chassis Forward	> 50
+5 to chassis Reverse	5-15
+5 gnd to chassis	0
VMEM to chassis Forward	Inf
VMEM to chassis Reverse	> 50
VINH to chassis Forward	> 50
VINH to Chassis Reverse	5-15
VINH to gnd to chassis	0
VL to chassis Forward	Inf
VL to chassis Reverse	50
VL gnd to chassis	0
-5 to chassis Forward	> 50
-5 to chassis Reverse	> 50

5-8.3 Output Voltage Readings.

Taken with a Simpson Model 260 or equivalent. (Oscilloscope may be used).

Output	Reading
VL	10 VDC $\phi 1$ 10 VDC $\phi 2$
VINH	17.2 VDC (Adj by 2K Trimpot)
VMEM	21.7 VDC (Adj by 2K Trimpot)
+5VDC	+5VDC + .45 -.3
-5VDC	-5VDC -.45 +.3
+5 O.K.	7-8VDC
PWR FAIL	3-4VDC
MEM O.K.	3-4 VDC

5-8.4 Replacing Power Transistors.

Power Transistors MEM, INH and +5 volts are located on the underside of the heat sink. To replace, remove 4 Phillips head screws holding the heat sink in place. The -5 power transistor (2N3715) is located in a heat sink on the Power Supply Circuit Board. Figure 5-1 shows the heat sink mounting locations for the MEM, INH, and +5 volt power transistors.

5-8.5 Power Supply Internal & External Plug Connections.

Plugs P1 and P2 are shown below in Figure 5-2. Plug P1 is an external plug, the cable of which is wired from the Multiple PCB Connector and terminates in P1. P1 connects into a jack composed of pins permanently soldered into the etched surface of the Power Supply Regulator Board assembly. Connector P2 is the termination for an internal cable which connects the Regulator circuits on the Regulator Board assembly with the rest of the components of the power supply e.g., power transformer, heat sink power transistors, etc.

5-9 SUPERNOVA INTERCONNECTION CABLES.

The relationships of the Supernova interconnecting cables are shown on Figure 5-3. As shown cables are identified by the particular plug termination for that cable. For example, the cable run from the Supernova Console to the (male) connector P1 (mounted on the Multiple PCB Connector Board etch) terminates in a (female) connector also labeled P1. The P1 through P9 (male connectors) are basically plug connectors made up of individual pins permanently staked and soldered to the Multiple PCB Connector Board etch. The following five sheets of Figure 5-4 list the wiring for (female) connectors P1 through P9 as they terminate at the Multiple PCB Connector Board. The color codes listed in Figure 5-4 are shown in abbreviated notation which has the following meanings:

o/blk	Orange/Black	brn/r	Brown/Red
grn/blk	Green/Black	o/r	Orange/Red
r/blk	Red/Black	w/r	White/Red
w/blk	White/Black	blk/r	Black/Red
brn	Brown	brn/w	Brown/White
o	Orange	grn/w	Green/White
grn	Green	r/w	Red/White
r	Red	blk/w	Black/White
w	White	brn/blk	Brown/Black
blk	Black	yel	Yellow
r/grn	Red/Green	gry	Gray
blu	Blue	p	Purple

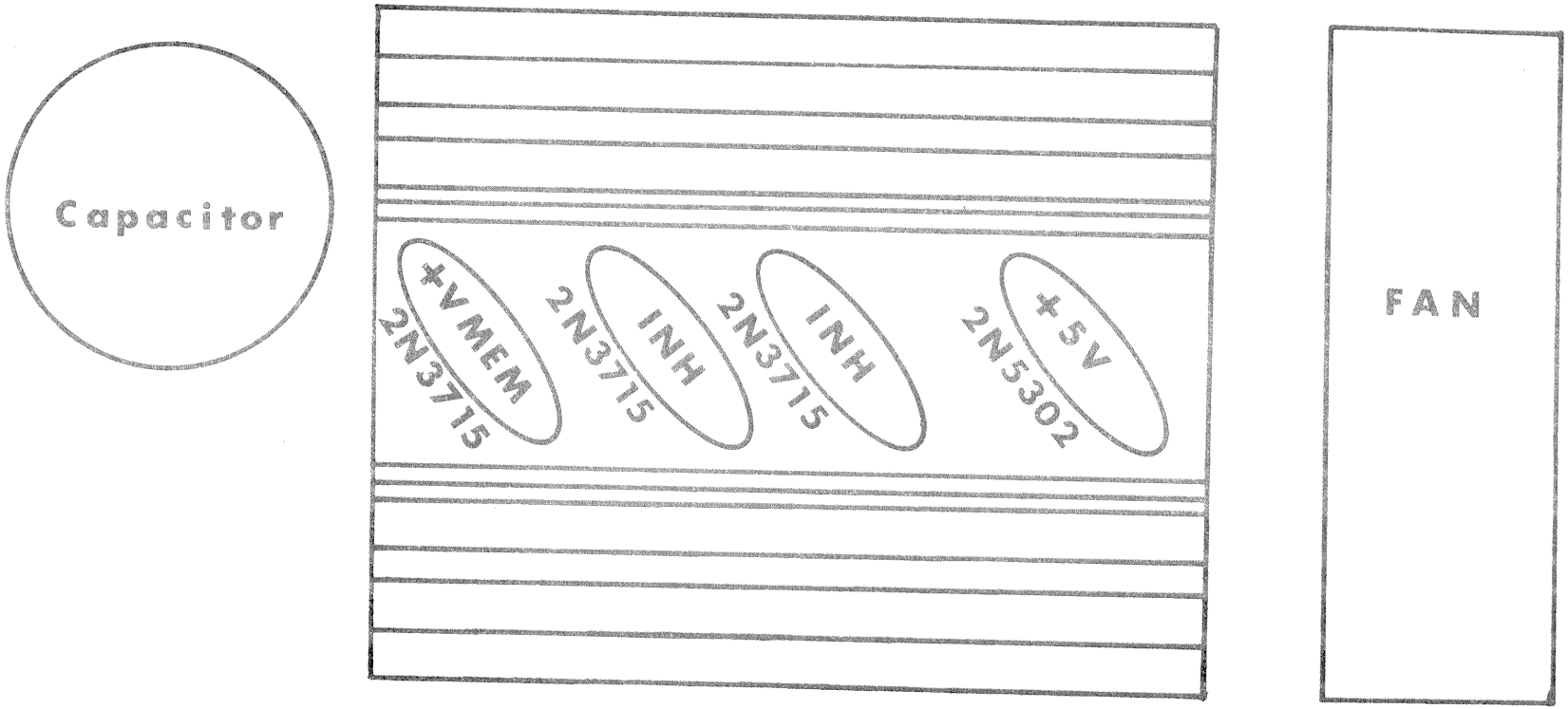
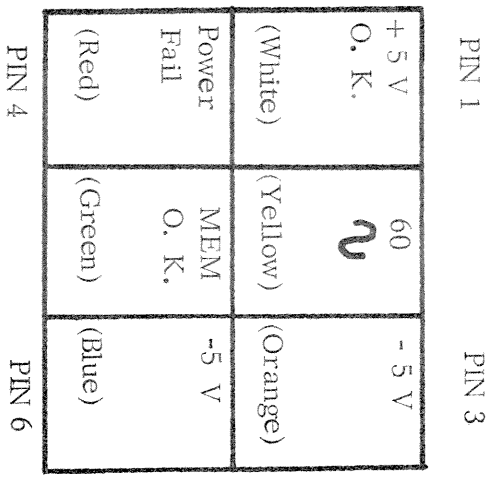


Figure 5-1. Location of Power Transistors of Heat Sink



TOP

P2

PIN 11		Base* + 5 (Red) — PIN 1
		+ 5 V Output (Red) See Note 1
	Emitter* + V MEM (Yellow)	Ground (Black) See Note 1
		+ 30 VNR (Blue)
	Base* + V MEM (White)	
	Jumper (Yellow)	Base* Inhibit (Green)
	Jumper (Yellow)	Jumper (Yellow)
	- 5 Volt (Orange) See Note 3	Sense Inhibit Out (Green) See Note 2
	Transformer T1 8 VAC (Yellow)	Ground (Black) See Note 2
PIN 20	Transformer T1 8 VAC (Yellow)	Jumper (Yellow) — PIN 10

*Power Transistors are mounted on Heat Sink

Note 1: + 5 and Ground Wires are twisted pair.

Note 2: Sense line for output Inhibit voltage and ground are twisted pair.

Note 3: Line to 6,000 μfd, 10 VDC Capacitor mounted under Heat Sink.

Figure 5-2. Power Supply Plug Connections

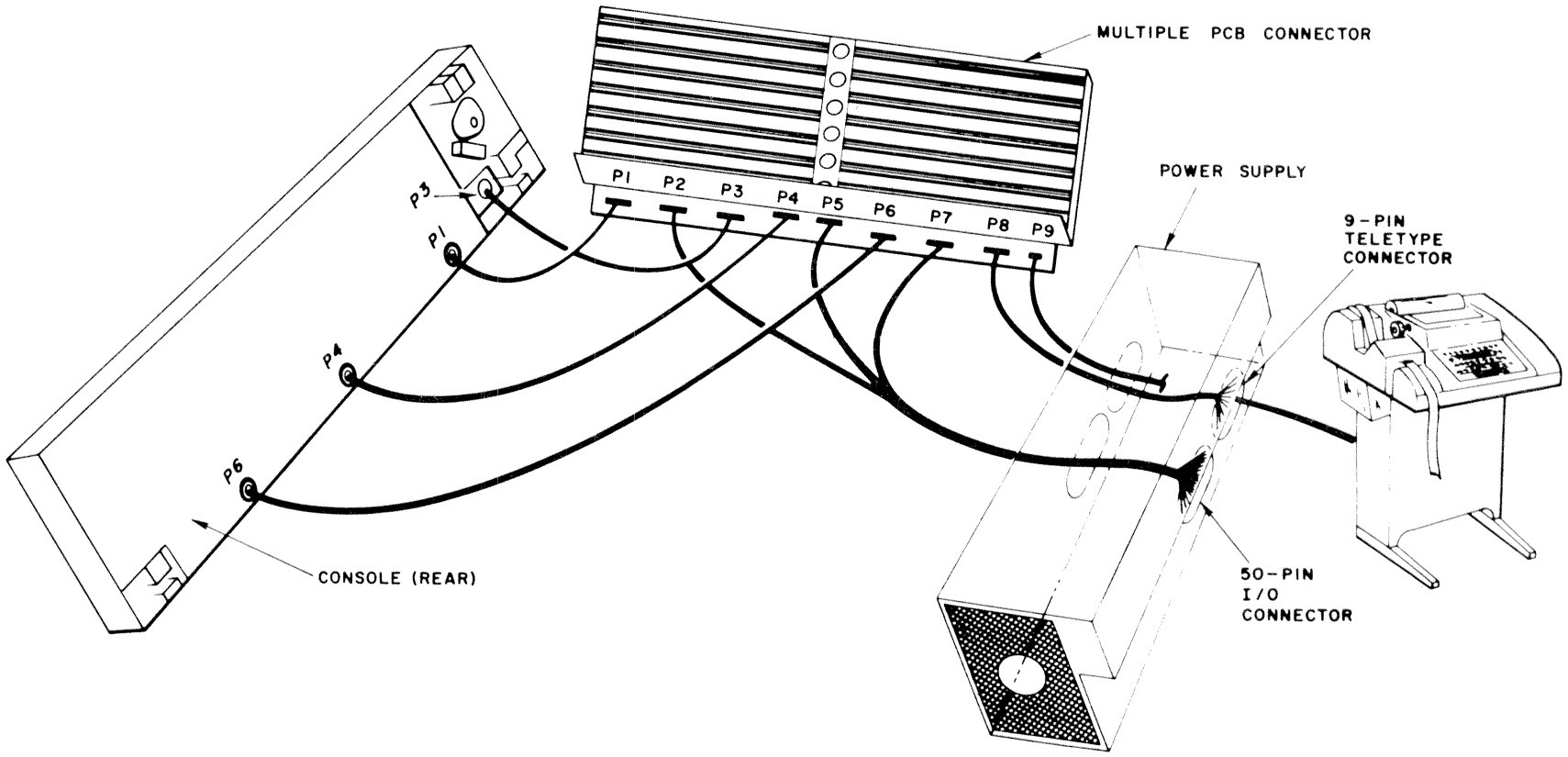


Figure 5-3. Relationships of Supernova Interconnecting Cables

P1 (Console Cable)

1	2	3	4	5	6	7	8	9	10
GND	$\overline{\text{IRIND0}}$	+5V	$\overline{\text{IRIND3}}$	IND0	$\overline{\text{IND3}}$	$\overline{\text{IND1}}$	$\overline{\text{CON3}}$	$\overline{\text{CON2}}$	GND
o/blk	grn/blk	r/blk	w/blk	brn	o	grn	r	w	blk
GND	GND	+5V	+5V	02 LOGICAL	$\overline{\text{IRIND1}}$	$\overline{\text{CON1}}$	$\overline{\text{CON0}}$	$\overline{\text{IND2}}$	GND
r/grn	brn/r	o/r	w/r	blk/r	brn/w	grn/w	r/w	blk/w	brn/blk
11	12	13	14	15	16	17	18	19	20

P2 (I/O Cable)

1	2	3	4	5	6	7	8	9	10
GND	$\overline{\text{DATA6}}$	$\overline{\text{DATA2}}$	$\overline{\text{DATA9}}$	$\overline{\text{DATA13}}$	$\overline{\text{DATA4}}$	$\overline{\text{DATA0}}$	$\overline{\text{DATA12}}$	$\overline{\text{DATA5}}$	GND
blk	yel	brn	gry	grn	p	o	blu	w	blk
GND	$\overline{\text{DATA}}$ 15	$\overline{\text{DATA}}$ 1	$\overline{\text{DATA}}$ 3	$\overline{\text{DATA}}$ 10	$\overline{\text{DATA}}$ 14	$\overline{\text{DATA}}$ 7	$\overline{\text{DATA}}$ 11	$\overline{\text{DATA}}$ 8	GND
blk	yel	brn	gry	grn	p	o	blu	w	blk
11	12	13	14	15	16	17	18	19	20

Figure 5-4. Supernova Interconnection Plug Wiring (Sheet 1 of 5)

P3 (Console Cable)

1	2	3	4	5	6	7	8	9	10
$\overline{EX}$	$\overline{RST}$	$\overline{CHST}$	$\overline{DP}$	$\overline{CONT}$	$\overline{STOP}$	$\overline{ISTP}$	$\overline{MSTP}$	RESTART ENB	$\overline{PLC}$
o/blk	grn/blk	r/blk	w/blk	brn	o	grn	r	w	blk
$\overline{STRT}$	$\overline{EXN}$	$\overline{DPN}$	$\overline{ACEX}$	$\overline{ACDP}$	ACC2	ACC1	ACC0	ACC3	$\overline{ACC\ ENB}$
r/grn	brn/r	o/r	w/r	blk/r	brn/w	grn/w	r/w	blk/w	brn/blk
11	12	13	14	15	16	17	18	19	20

P4 (Console Cable)

1	2	3	4	5	6	7	8	9	10
GND	$\overline{IND7}$	$\overline{CON5}$	$\overline{CON4}$	$\overline{CON2}$	$\overline{CON7}$	$\overline{IND8}$	$\overline{IND9}$	+5V	GND
o/blk	grn/blk	r/blk	w/blk	brn	o	grn	r	w	blk
GND	$\overline{IND6}$	$\overline{IND5}$	$\overline{IND4}$	$\overline{IRIND2}$	$\overline{CON9}$	$\overline{CON8}$	$\overline{IND10}$	+5V	GND
r/grn	brn/r	o/r	w/r	blk/r	brn/w	grn/w	r/w	blk/w	brn/blk
11	12	13	14	15	16	17	18	19	20

Figure 5-4. Supernova Interconnection Plug Wiring (Sheet 2 of 5)

P5 (I/O Cable)

1	2	3	4	5	6	7	8	9	10
GND blk	REQENB yel	OVFLO brn	DCHI gry	DCHR grn	DCHO p	INTP OUT o	DCHP OUT blu	+5V w	GND blk
GND blk	$\overline{\text{DCHM0}}$ yel	$\overline{\text{DCHM1}}$ brn	$\overline{\text{INTR}}$ gry	IORST grn	DS0 p	IOPLS o	$\overline{\text{SELD}}$ blu	$\overline{\text{SELB}}$ w	GND blk
11	12	13	14	15	16	17	18	19	20

P6 (Console Cable)

1	2	3	4	5	6	7	8	9	10
GND o/blk	$\overline{\text{CON10}}$ grn/blk	$\overline{\text{CON11}}$ r/blk	$\overline{\text{IND11}}$ w/blk	$\overline{\text{IND12}}$ brn	$\overline{\text{IND13}}$ o	$\overline{\text{IND14}}$ grn	$\overline{\text{IND15}}$ r	$\overline{\text{CON13}}$ w	GND blk
GND r/grn	$\overline{\text{DCH IND}}$ brn/r	$\overline{\text{FETCH IND}}$ o/r	$\overline{\text{PROT IND}}$ w/r	$\overline{\text{RUN IND}}$ blk/r	$\overline{\text{DEFER IND}}$ brn/w	$\overline{\text{CON15}}$ grn/w	$\overline{\text{CON14}}$ r/w	$\overline{\text{CON12}}$ blk/w	GND brn/blk
11	12	13	14	15	16	17	18	19	20

Figure 5-4. Supernova Interconnection Plug Wiring (Sheet 3 of 5)

P7 (I/O Cable)

1	2	3	4	5	6	7	8	9	10
GND blk	$\overline{\text{DCHA}}$ yel	DATOA brn	DATOB gry	DATIC grn	STRT p	CLR o	$\overline{\text{DS3}}$ blu	DATOC w	GND blk
GND blk	DS4 yel	DS5 brn	DS2 gry	DS1 grn	MSKO p	INTA o	DATIB blu	DATIA w	GND blk
11	12	13	14	15	16	17	18	19	20

P8 (TTY Cable)

1	2	3	4	5	6	7	8	9	10
GND o/blk	+5V grn/blk	RD RUN r/blk	DATA IN STOP w/blk	TT OUT brn	+V o	TT IN grn	-5V r		GND blk
GND r/grn									GND brn/blk
11	12	13	14	15	16	17	18	19	20

Figure 5-4. Supernova Interconnection Plug Wiring (Sheet 4 of 5)

P9 (Power Supply Cable)

1	2	3
+ 5 V O. K. w	60 ∿ yel	- 5 V o
Power Fail r	MEM O. K. grn	- 5 V blu
4	5	6

Figure 5-4. Supernova Interconnection Plug Wiring
(Sheet 5 of 5)

Table 5-2 is a wire run list for the Supernova I/O Cable. As shown on Figure 5-3, the I/O Cable terminates at the Multiple PCB Connector Board in three (20 pin AMP) Connectors (P2, P5, & P7). The other end terminates in a 50 pin (Cannon) (S) connector mounted in the lower rear panel of the power supply. Table 5-2 also lists the color for each wire.

Table 5-2. Wire List for Supernova Cable

20 Pin AMP Connector	Color	50S Cannon Connector
P2, P5, P7, Pins 1&11	Black	1
P2, P5, P7, Pins 10&20	Black	50
P7-7	Orange	2
P2-7	Orange	3
P2-13	Brown	4
P2-3	Brown	5
P2-14	Gray	6
P2-6	Purple	7
P2-9	White	8
P2-2	Yellow	9
P2-17	Orange	10
P2-19	White	11
P2-4	Gray	12
P2-15	Green	13
P2-18	Blue	14
P2-8	Blue	15
P2-5	Green	16
P2-16	Purple	17
P2-12	Yellow	18
P7-19	White	19
P7-18	Blue	20
P7-5	Green	21
P7-3	Brown	22
P7-4	Gray	23
P7-9	White	24
P7-2	Yellow	25
P5-4	Gray	26
P5-12	Yellow	27
P5-13	Brown	28
P5-6	Purple	29
P5-8	Blue	30
P5-5	Green	31
P5-16	Purple	32
P7-15	Green	33
P7-14	Gray	34

Table 5-2. Wire List for Supernova I/O Cable (Continued)

20 Pin AMP Connector	Color	50S Cannon Connector
P7-8	Blue	35
P7-12	Yellow	36
P7-13	Brown	37
P7-17	Orange	38
P5-7	Orange	39
P5-14	Gray	40
P5-17	Orange	41
P5-15	Green	42
P7-16	Purple	43
P5-3	Brown	44
P5-2	Yellow	45
P5-19	White	46
P5-18	Blue	47
P7-6	Purple	48
P5-9	Red	49

SECTION VI

ILLUSTRATED PARTS LIST

6-1. INTRODUCTION.

This chapter contains a complete list of replaceable parts for the Supernova Computer. To facilitate the procurement of parts not manufactured by Data General, the descriptions for such parts include an associated manufacturer's reference code number. Each number indexes the corresponding manufacturer's name and address as listed in Table 6-1 of this chapter. Manufacturer index numbers assignments are for reference purposes only and do not correspond to codes assigned by the Federal Supply Code. Personnel involved in provisioning from this document may consult the Federal Supply Code for Manufacturers, Cataloging Handbook H4-1, for the proper Federal reference codes for manufacturers listed in this chapter. The original manufacturer's part number is listed for all items including commercially available hardware to facilitate exact replacement of substitute parts.

Table 6-1. List of Manufacturers

Code Number	Manufacturer's Name and Address
0010	Data General Corp. Southboro, Massachusetts
0011	Allen Bradley Milwaukee, Wisconsin
0012	C & K Switching Co. Watertown, Massachusetts
0013	Fairchild Semiconductors Mountainview, California
0014	Signetics, Inc. Sunnyvale, California
0015	Sprague Newton, Massachusetts

Table 6-1. List of Manufacturers (Continued)

Code Number	Manufacturer's Name and Address
0016	Hudson Lamp Kearny, New Jersey
0017	Microswitch, Division Honeywell Freeport, Illinois
0018	Dale Electronics Columbus, Nebraska
0019	Erie Technological Prod. State College, Pennsylvania
0020	Airpax Cambridge, Maryland
0021	Belden Wire Chicago, Illinois
0022	Cannon Electric Los Angeles, California
0023	Leviton Manufacturing Co. Brooklyn, New York
0024	Triad Transformer Venice, California
0025	Littlefuse, Inc. Des Plaines, Illinois
0026	Motorola Phoenix, Arizona
0027	Ohmite Manufacturing Co. Skokie, Illinois
0028	Fenwal Electronics Framingham, Massachusetts
0029	Pamotor, Inc. Burlingame, California

Table 6-1. List of Manufacturers (Continued)

Code Number	Manufacturer's Name and Address
0030	Memcor, Inc. Huntington, Indiana
0031	Bourns, Inc. Riverside, California
0032	Central Switching Milwaukee, Wisconsin
0033	Wakefield Engineering Wakefield, Massachusetts
0034	Continental Device Corp. Hawthorne, California
0035	Sylvania, Inc. Woburn, Massachusetts
0036	Cornell-Dublier Newark, New Jersey
0037	Valpey-Fisher Corp. Holliston, Massachusetts
0038	Texas Instruments, Inc. Dallas, Texas
0039	RCA Corporation Mountain Top, Pennsylvania
0040	RBM Controls/Essex Int'l. Logansport, Indiana
0041	Corning Glassworks Bradford, Pennsylvania
0042	IRC Div. of TRW Inc. Burlington, Iowa
0043	AMP Inc. Harrisburg, Pennsylvania

Table 6-1. List of Manufacturers (Continued)

Code Number	Manufacturer's Name and Address
0044	Heyman Mfg. Co. Kenelworth, New Jersey
0045	Cinch Jones Elkgrove Village, Illinois
0046	Harvey Radio Laboratories, Inc. Cambridge, Massachusetts
0047	Dickson Electronics Corp. Scottsdale, Arizona
0048	South Co., Inc. Lester, Pennsylvania
0049	Advance Micro Devices Sunnyvale, California
0050	Sealectro Mamaroneck, New York
0051	Chicago Lock Company Chicago, Illinois
0052	Elmenco Willimantic, Connecticut
0053	Omtronics Omaha, Nebraska
0054	Ward Leonard Mount Vernon, New York
0055	Kapitol Magnetics Chicago, Illinois
0056	Sangamo Electrical Braintree, Massachusetts

6-1.1 Relationships of Main Group Assemblies to End Configurations.

The Supernova Central Processor by definition consists of the Console/Enclosure Unit, Power Supply Unit, Central Processor - 1 (CPU-1) Printed Circuit Board Assembly, Central Processor-2 (CPU-2) Printed Circuit Board Assembly, Central Processor-3 (CPU-3) Printed Circuit Board Assembly. The Console/Enclosure Unit is so designed that seven 15 X 15 inch Printed Circuit Board Assemblies may be plug mounted into a special printed circuit board connector in the Enclosure Chassis. The board assemblies are inserted horizontally into the Enclosure Chassis. A pair of guiding rollers are built into the chassis frame (on each board level) to insure proper insertion of the board contacts into the corresponding socket of the multiple printed circuit board connector. The seven connector slots are numbered from the bottom of the chassis up to the top with slots 1, 2, and 3 reserved for the CPU-1, CPU-2, and CPU-3 Assemblies respectively. The four remaining slots may be used for memory assemblies, I/O assemblies, or special control board assemblies. (BUT IN DIFFERENT PLACES!)

These assemblies represent a variety of optional equipment which is individually selected by each customer to provide a specific configuration in accordance with the required application. Under these conditions there is no top level assembly number available to define any one system configuration. The modular building block concept, while providing the greatest flexibility in the task of designing a system for a specific application does not lend itself to the top-down breakdown assembly designations normally applied to special purpose system hardware, e.g., military or aerospace computing systems. Supernova Memories, I/O and Peripheral Control Assemblies all have assembly level numbers of equal weight.

The illustrated parts list provided in this Section describes the Supernova Central Processor Unit. This Section of the manual also contains the parts list for the Supernova 4K Core Memory assembly, and the Basic I/O Control assembly. Additional illustrated parts listing material may also be added to this section of the manual in the event other memories are added to the configuration sometime after installation. In the same manner this section may be expanded to include documentation for any peripheral control assembly (e.g., parts listing for the Magnetic tape Control or Disk Control board assemblies) purchased with or added to the configuration. Parts lists for the other optional memory assemblies and peripheral control assembly boards are part of the documentation package for

each optional assembly, and is shipped along with the hardware. It is suggested that the accompanying illustrated parts listing be incorporated into the section immediately upon receipt of any optional assemblies.

Hence, the complete illustrated parts listing for any selected computer system will eventually be compiled in this section. The figure numbers, on the other hand, are organized to run concurrently up to Figure 6-21 (Supernova 4K Memory Assembly.) However, Figures from Figure 6-22 upward are numbered sequentially through the options, and as such will not necessarily preserve any numbering continuity for parts lists subsequently to this section. Figure numbers missing out of any sequence due to excluded options should be noted as "Not Applicable" on any provisioning lists.

The parts list for each major assembly lists the circuit reference designator for each part, along with the manufacturer's part number and description. The quantities per assembly are also listed. The manufacturer's name and address may be found by first referencing Table 6-2, Manufacturer's Parts List, for the Manufacturer Reference Code for the selected component. This code number locates the name and address of the manufacturer in Table 6-1, List of Manufacturers. For example, to locate the manufacturer of Capacitor C1 on CPU-1, first look up the circuit reference designator C1 in the CPU-1 parts list, which in this case is a 220 pf, 500 VDC Capacitor. Find the 220 pf, 500 VDC Capacitor entry in Table 6-2 and locate Manufacturer's Reference Code opposite as 0036. Look up 0036 in Table 6-1 and locate Cornell-Dublier, Newark, New Jersey as the manufacturer.

6-1.2 Inter-Assembly Wiring Information.

There are four main inter-assembly cabling runs in the Supernova; from the Console to the PCB Connector Panel, from the power supply to the Console, from the power supply to the resistor board subassembly, and from the resistor board subassembly to the PCB Connector Panel. Cabling to external devices is not part of the inter-assembly wiring and as such is not described in this chapter. Cabling between the Supernova PCB Connector Panel and external devices via the In-Out Bus is described in Appendix A of the "How to use the Nova and the Supernova," or "How to use the Nova Computers" manuals available under separate covers.

The cabling between the Console and the PCB Connector Panel originates at the Control Switches and Display and Switches Assemblies and terminates in four connectors, P1, P3, P4, and P6. These connectors mate with four printed circuit jack connectors located on the bottom edge of the Multiple PCB Connector Panel (part of the Enclosure Chassis Assembly). Paragraph 5-9 lists the Wiring Data for Connectors P1, P3, P4 & P6. Two individual lines from the Power Supply to the Console supply the console with + 28 volt $\phi 1$ and the + 28 volt $\phi 2$ power. Three other lines from the Power Supply connect into three terminals on the resistor board subassembly (part of the Enclosure Chassis Assembly), + V MEM, + VINH, and GRD. A cable composed of twisted pair sets connects the outputs from the resistor board subassembly to the various wire wrap pins of the Multiple PCB Connector Panel reserved for the Memory PCB Assembly connections. All cables assigned a part number in the Group Assembly Parts list are considered as replaceable components. All other wires are considered expendable equipment replaceable as required from standard wire stock supplies.

6-1.3 Attaching Hardware.

All attaching hardware (nuts, washers, and screws) for the various assemblies of the Supernova are considered expendable, as - required items. Table 6-3 lists the sizes of the various nuts, washers, and screws used in the Supernova. All hardware listed is stainless steel stock and as a group are commercially available.

Table 6-2. Manufacturer's Parts List

CAPACITORS

PART No.	DESCRIPTION	MANUFACTURER REFERENCE CODE
DM-15-330J	CAPACITOR, 33pf, 500VDC	0052
CD15FD101J	CAPACITOR, 100pf, 500VDC	0036
CD15FD221J	CAPACITOR, 220pf, 500VDC	0036
DM-15-471J	CAPACITOR, 470pf, 500VDC	0052
DM-15-561J	CAPACITOR, 560pf, 500VDC	0052
DM-15-821J	CAPACITOR, 820pf, 500VDC	0052
DM-15-122J	CAPACITOR, 1200pf, 500VDC	0052
CK103	CAPACITOR, .01μfd, 50VDC	0032
5635-000-Y5FO-503M	CAPACITOR, .05μfd, 12VDC	0019
Y5FO-503M	CAPACITOR, .05μfd, 50VDC	0019
250-48P9	CAPACITOR, .1ufd, 250VAC	0015
150D224X9020A2	CAPACITOR, .22μfd, 20VDC	0015
150D685X9006A2	CAPACITOR, 6.8μfd, 6V	0015
D6R8B35K	CAPACITOR, 6.8μfd, 35V	0047
150D825X9050R	CAPACITOR, 8 μfd, 50VDC	0015
150D476X9020R2	CAPACITOR, 47μfd, 20VDC	0015
500-4045-02	CAPACITOR, 600μfd, 10VDC	0056
500-4570-02	CAPACITOR, 21000μfd, 25VDC	0056
500-4044-02	CAPACITOR, 21000μfd, 40VDC	0056
	DIODES	
CD8434	DIODE	0034
MDA-950-1	DIODES	0026
MDA-962-1	DIODE, BRIDGE	0026
1N3879R	DIODE	0026
1N4997	DIODE	0026
	BULBS	
2176	BULB, Console, 28volt	0016
	FANS	
8500	FAN, AXIAL	0029
	INDUCTORS	
104 000 006	CLOCK CHOKE	0010
56-590-653B	FERRITE CORE INDUCTOR	0010
105 000 005	INDUCTOR, + VINH	0010
105 000 004	INDUCTOR, + 5V	0010

Table 6-2. Manufacturer's Parts List (Continued)

TRANSISTORS

PART No.	DESCRIPTION	MANUFACTURER REFERENCE CODE
MPS3640	TRANSISTOR	0026
2N3646	TRANSISTOR	0026
2N3715	TRANSISTOR	0038
2N3725	TRANSISTOR	0026
2N4123	TRANSISTOR	0026
2N4125	TRANSISTOR	0026
2N4403	TRANSISTOR	0026
2N4441	TRANSISTOR	0026
2N4919	TRANSISTOR	0026
2N5302	TRANSISTOR	0038

RESISTORS

CB1005	RESISTOR, 10Ω, 1/4W, 5%	0011
CB3905	RESISTOR, 39Ω, 1/4W, 5%	0011
CB4705	RESISTOR, 47Ω, 1/4W, 5%	0011
CB1015	RESISTOR, 100Ω, 1/4W, 5%	0011
CB1815	RESISTOR, 180Ω, 1/4W, 5%	0011
CB2215	RESISTOR, 220Ω, 1/4W, 5%	0011
CB3315	RESISTOR, 330Ω, 1/4W, 5%	0011
CB3915	RESISTOR, 390Ω, 1/4W, 5%	0011
CB4715	RESISTOR, 470Ω, 1/4W, 5%	0011
CB6815	RESISTOR, 680Ω, 1/4W, 5%	0011
CB7515	RESISTOR, 750Ω, 1/4W, 5%	0011
CB1025	RESISTOR, 1K, 1/4W, 5%	0011
CB1225	RESISTOR, 1.2K, 1/4W, 5%	0011
CB1525	RESISTOR, 1.5K, 1/4W, 5%	0011
CB2225	RESISTOR, 2.2K, 1/4W, 5%	0011
CB3325	RESISTOR, 3.3K, 1/4W, 5%	0011
CB4725	RESISTOR, 4.7K, 1/4W, 5%	0011
CB6825	RESISTOR, 6.8K, 1/4W, 5%	0011
CB8225	RESISTOR, 8.2K, 1/4W, 5%	0011
CB1035	RESISTOR, 10K, 1/4W, 5%	0011
CB3335	RESISTOR, 33K, 1/4W, 5%	0011
NA55	RESISTOR, 150Ω, 1/10W, 1%	0041
242E1815	RESISTOR, 180Ω, 3W, 5%	0011
2742	RESISTOR, 600, 3W, 5%	0030
3005P-1202	POTENTIOMETER, 2K	0031

Table 6-2. Manufacturer's Parts List (Continued)

THERMISTORS

PART No.	DESCRIPTION	MANUFACTURER REFERENCE CODE
KA	THERMISTOR	0028
	SWITCHES	
7205CSP	SWITCH, Toggle, DPDT	0012
7101CSP	SWITCH, Toggle, SPST	0012
7105CSP	SWITCH, Toggle, DPDT Spring Loaded	0012
J321D8	SWITCH, Micro	0017
J323D8	SWITCH, Micro	0017
122 000 001	LOCK, Console	0051
122 000 002	KEY, Console	0051
	TRANSFORMERS	
104 000 012	TRANSFORMER, MEMORY	0010
104 000 013	TRANSFORMER, BALUN	0010
T-7973	TRANSFORMER, POWER	0055
	INTEGRATED CIRCUITS	
BC728	16 DIODE ARRAY	0038
MC3002	Quad 2-Input NAND Interface Gates	0026
MC3003	Quad NAND Gates	0026
MC3026	Dual 4-Input AND Power Gate	0026
MC3061	Dual J-K Flip-Flop	0026
SG83	Dual Pulse Shaper/Delay AND Gate	0035
SH6405	Quad Transistor	0013
510A	Amplifier	0014
723	Precision Voltage Regulator	0013
74H55	Expandable 2-Wide, 4-Input Gates	0038
7438	Quad 2-Input Positive NAND Gates	0015
7474	Dual D-Type Edge-Triggered Flip-Flop	0038
7475	(Dual) Quadruple Latches	0038
7524	Sense Amplifier	0038
8T80	Quad 2-Input NAND Interface Gates	0014
8260	Arithmetic Logic Element	0014
8264	3-Input, 4-Bit Digital Multiplexer	0014
8271	4-Bit Shift Registers	0014
8280	Decade Counter	0014
8281	4-Bit Binary Counter	0014
8881	Quad 2-Input Gates	0014
8885	Quad 2-Input NOR Gates	0014

Table 6-2. Manufacturer's Parts List (Continued)

INTEGRATED CIRCUITS (Continued)

PART No.	DESCRIPTION	MANUFACTURER REFERENCE CODE
9002	Quad 2-Input Gates	0013
9003	Triple 3-Input Gates	0013
9004	Dual 4-Input NAND Gates	0013
9005	Dual 2 Wide AND-OR-INVERT Gates	0013
9006	Dual 4-Input AND-OR-INVERT Gates	0013
9007	Single 8-Input Gate	0013
9008	Single 4 Wide AND-OR-INVERT Gates	0013
9009	Dual 4-Input NAND Gates	0013
9016	HEX Inverters	0013
9300	4-Bit Shift Register	0013
9301	One-of-Ten Decoder	0013
9309	Dual 4-Input Multiplexer	0013
9316	4-Bit Binary Counter	0013
9601	Monostable Multivibrator	0013
	BREAKDOWN DIODES	
1N2864	DIODE, BREAKDOWN	0034
1N5231	DIODE, BREAKDOWN	0026
1N5240	DIODE, BREAKDOWN	0026
1N5250	DIODE, BREAKDOWN	0026
332864	DIODE, BREAKDOWN	0034
.5M5.1ZS	DIODE, BREAKDOWN	0026
	CRYSTALS	
No Number	CRYSTAL, 20MHz	0037
No Number	CRYSTAL, 14.08KHz	0037

Table 6-3. List of Attaching Hardware

MACHINE SCREW (Stainless Steel)

Thread	Head	Length
4-40	100° Countersink Phillips Flat	3/16, 1/4, 3/8, 1/2
4-40	Phillips Pan	5/8, 7/8
8-32	Phillips Pan	3/16, 5/16
6-32	100° Countersink Phillips Flat	1/4
4-40	Slotted B. H. (Teflon Coated)	5/16
2-56	Slotted B. H.	5/16
10-32	Allen Socket	3/8

MACHINE SCREWS (Stainless Steel)

(S. E. M. S - with captive internal tooth lockwasher)

Thread	Head	Length
4-40	Phillips Pan	3/16, 1/4, 7/16, 1/2
6-32	Phillips Pan	3/8, 5/8
8-32	Phillips Pan	3/4, 1 1/4
10-32	Phillips Pan	3/8, 5/8, 3/4

MACHINE SCREWS (Stainless Steel)

(S. E. M. S)

Thread	Head	Length
8-32	Slotted Hex	5/16, 3/8

MACHINE SCREWS (Nylon)

Thread	Head	Length
4-40	Slotted B. H.	1/4, 3/8

Table 6-3. List of Attaching Hardware (Continued)

MACHINE Nuts (Stainless Steel)

Thread	Type
2-56	Hex
4-32	Hex
6-32	Hex
8-32	Hex
10-32	Hex

WASHERS (Stainless Steel)

Type	Size
Internal Tooth	#2, 4, 6, 8, 10
Flat	#4, 6, 8

To be Supplied

Figure 6-1. Supernova Central Processor

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
6-1		8001	. SUPERNOVA CENTRAL PROCESSOR		
-1	1	005 000 326	. CONSOLE/ENCLOSURE UNIT (See Figure 6-2 for detailed breakdown)	1	
-2	2	005 000 047	. POWER SUPPLY UNIT(See Figure 6-7 for detailed breakdown). . . .	1	
-3	3	005 000 065	. . CENTRAL PROCESSOR-1 PCB ASSEMBLY(See Figure 6-17 for detailed breakdown).	1	
-4	4	005 000 067	. . CENTRAL PROCESSOR-2 PCB ASSEMBLY(See Figure 6-18 for detailed breakdown).	1	
-5	5	005 000 069	. . CENTRAL PROCESSOR-3 PCB ASSEMBLY(See Figure 6-19 for detailed breakdown.	1	
-6	6	005 000 009	. . BASIC I/O PCB ASSEMBLY, MODEL 4007(Interface for Teletype, Real Time Clock, Paper Tape Reader and Paper Tape Punch)(See Figure 6-20 for detailed breakdown). .	1	
-7	7	005 000 070	. . SUPERNOVA 4K MEMORY PCB ASSEMBLY, MODEL8003(See Figure 6-21 for detailed breakdown). .	1	

To be Supplied

Figure 6-2. Console/Enclosure Unit

Figure 6-3. Console Casting Assembly
Figure 6-4. Control Switches Assembly
Figure 6-5. Display & Switch Assembly
Figure 6-6. Enclosure/Chassis Assembly

To be Supplied

To be Supplied

Figure 6-7. Power Supply Unit

Figure 6-8. Fan Assembly, Left
Figure 6-9. Fan Assembly, Right
Figure 6-10. Current Amplifier Assembly
Figure 6-11. Inductor Assembly
Figure 6-12. Large Transformer Assembly
Figure 6-13. Capacitor Assembly
Figure 6-14. Chassis Base Assembly
Figure 6-15. Regulator Assembly
Figure 6-16. Connector Plate Assembly

To be Supplied

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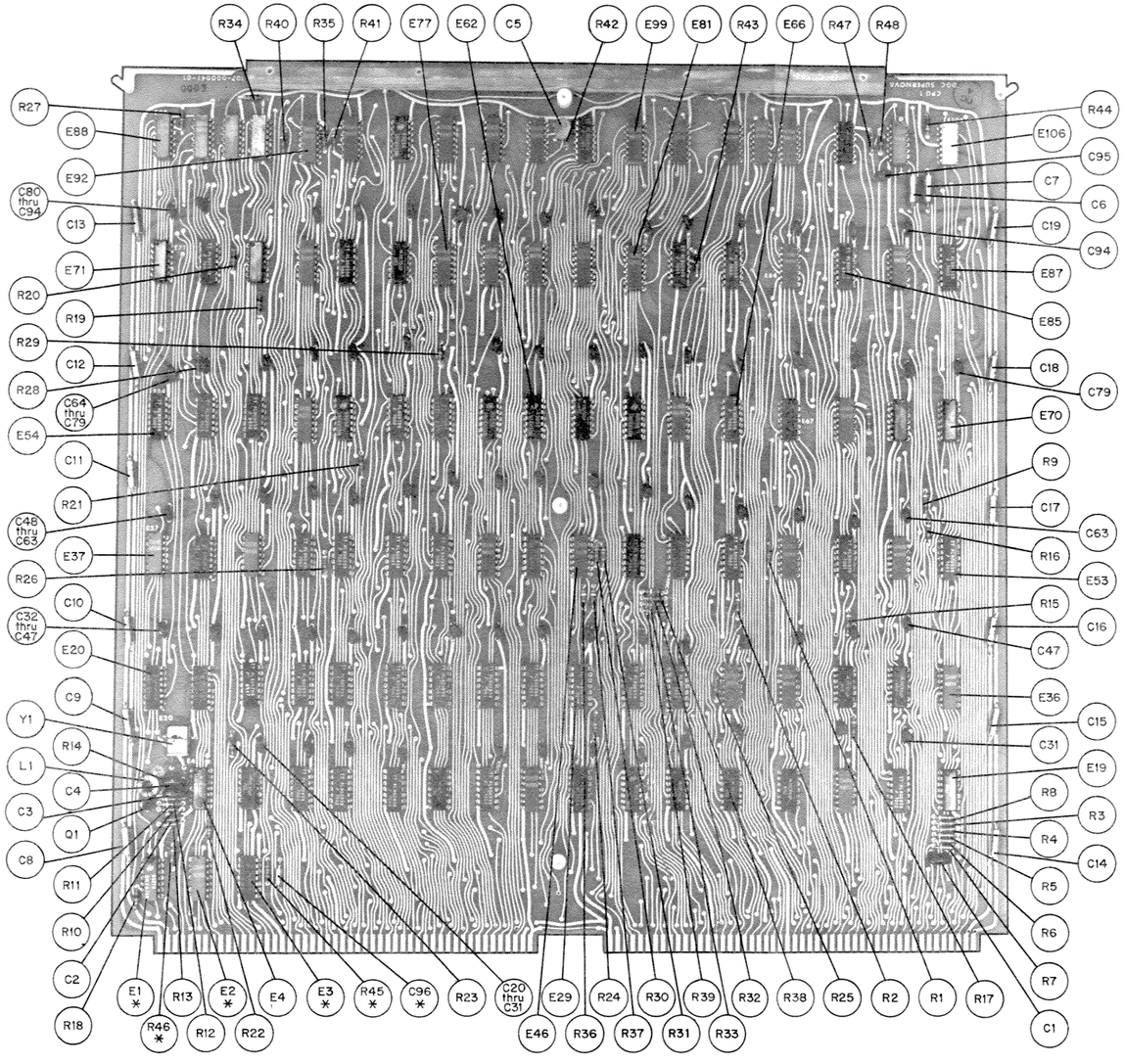
Page



UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES XX ± XXX ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010	DRAWN		**DATA GENERAL CORPORATION** SOUTHBORO, MASSACHUSETTS 01772
	CHECKED		
	ENGINEER		TITLE
	APPROVED		ILLUSTRATED PARTS LISTING, SUPERNOVA BOARD UNIT CPU-1
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES	FIRST USED ON		
MATERIAL			
FINISH	SCALE	SIZE D / CODE / DRAWING NUMBER 005 000 135 / REV	

Figure 6-17. Central Processor-1 PCB Assembly (Sheet 1)

HARDWARE

REF ITEM	DESCRIPTION	DRAWING NO.	REV	UNIT QTY.	TOTAL QTY.
1	SPACER, TOP PCB	002 000 051		3	
2	HANDLE, PCB	002 000 054		1	
3	PRINTED CIRCUIT BOARD, SUPERNOVA, CPU-1	107 000 041		1	
4	INJECTOR	123 000 001		2	
5	RIVET	123 000 002		2	
6	SCREW (HANDLE MTG)	106		4	
7	SCREW (SPACER MTG)	106		3	

REVISIONS

REV.	DESCRIPTION	DRFTG.	APP. BY	DATE

POWER MONITOR OPTION 8006 CIRCUIT REFERENCE	CENTRAL PROCESSOR UNIT 1 CIRCUIT REFERENCE	PART NO.	DESCRIPTION	DRAWING NO.	REV	QUANTITY BASIC	OPTION 8006	TOTAL
	C3, C4	CM05FD101J03	CAPACITOR, 100pf, 500V	103 000 031		2		2
	C1	CM05FD221J03	CAPACITOR, 220pf, 500V	103 000 006		1		1
	C2, C5		CAPACITOR, .01µf, 50V	103 000 001		2		2
	C6 thru C19	D6R8B35K	CAPACITOR, 6.8µf, 35V	103 000 002		14		14
	C20 thru C95	Y5F	CAPACITOR, .05µf, 12V	103 000 039		76		76
C96			CAPACITOR, 6.8µf, 6V	103 000 018			1	1
E2	E12, E32, E46, E50, E56, E68, E74 E85, E88, E97, E100, E105	9002/8889	DIP, QUAD 2-INPUT GATE	100 000 003		12	1	13
	E41, E43, E49, E72 E79, E83, E87	9003/8879	DIP, TRIPLE 3-INPUT GATE	100 000 004		7		7
	E40, E42, E51, E54, E82	9004/8819	DIP, DUAL INPUT GATE	100 000 005		5		5
	E10, E11, E47, E53, E75, E90, E91	9005/8840	DIP, DUAL 2 WIDE AND-OR-INVERT GATE	100 000 006		7		7
	E22, E59	9007	SINGLE 8-INPUT GATE	100 000 007		2		2
	E52, E65, E77, E95, E96, E101, E102	9008/8848	SINGLE 4 WIDE AND-OR-INVERT GATE	100 000 008		7		7
	E6, E7, E8, E18, E23, E24, E25, E26, E27, E28, E29, E30, E31, E55, E66, E98	9009/8859	DUAL 4-INPUT BUFFER	100 000 009		16		16
	E37, E45, E48, E60, E78, E80, E84, E89	9016/8H90	HEX INVERTER	100 000 010		8		8
	E20, E21, E38	9301	MSI ONE-OF-TEN DECODER	100 000 013		3		3
E3		9601	MONOSTABLE MULTIVIBRATOR	100 000 015			1	1
E1	E86	7474/8828/5610	DUAL D-TYPE EDGE-TRIGGERED FLIP FLOP	100 000 017		1	1	2
	E13, E58, E61, E62, E64, E94	74H55	EXPANDABLE 2-WIDE, 4-INPUT GATE	100 000 049		6		6
	E57, E81, E92	8271B	4-BIT SHIFT REGISTERS	100 000 042		3		3
	E17, E33, E36, E39, E44, E93, E99, E103	8885/MC3002	QUAD 2-INPUT NAND INTERFACE GATE	100 000 045		8		8
	E5, E9, E67, E69, E73	MC3026	DUAL 4-INPUT AND POWER GATE	100 000 054		5		5
	E4, E14, E15, E16, E19, E34, E35, E63, E70, E71, E76, E104	MC3061	DUAL J-K FLIP-FLOP	100 000 053		12		12
	E106	SG-83	DUAL PULSE SHAPER/DELAY AND GATE	100 000 023		1		1
	L1		CLOCK CHOKE	104 000 006		1		1
	Q1		TRANSISTOR MPS 3640	101 000 051		1		1
	R1, R18 thru R25, R27, R28, R29, R43		RESISTOR 1/4W 5% 10K	102 000 086		13		13
R46	R2 thru R9, R15, R16, R17, R26, R48		RESISTOR 1/4W 5% 470Ω	102 000 055		13	1	14
	R10 thru R14, R36 thru R41		RESISTOR 1/4W 5% 390Ω	102 000 053		11		11
	R30 thru R35		RESISTOR 1/4W 5% 330Ω	102 000 051		6		6
	R42		RESISTOR 1/4W 5% 220Ω	102 000 047		1		1
	R44		RESISTOR 1/4W 5% 8.2K	102 000 084		1		1
R45			RESISTOR 1/4W 5% 33K	102 000 098			1	1
	R47		RESISTOR 1/4W 5% 180Ω	102 000 045		1		1
	Y1		XTAL 20MHz	101 000 044		1		1

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± DECIMALS XX ± ANGLES XXX ± ±
PARTS TO BE FREE FROM BURRS
BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED · ALL MACH. SURFACES
MATERIAL
FINISH

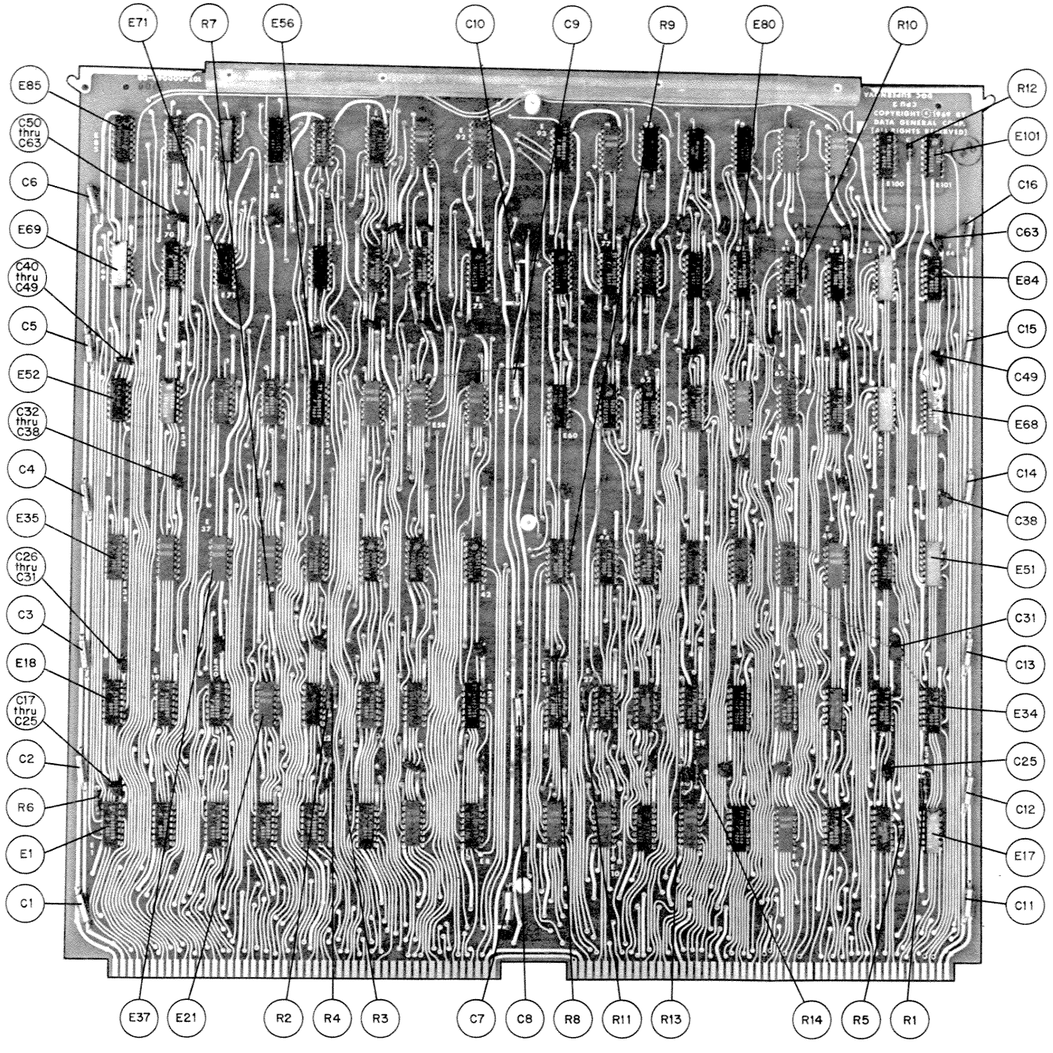
DRAWN
CHECKED
ENGINEER
APPROVED
FIRST USED ON
SCALE

DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

TITLE
ILLUSTRATED PARTS LISTING, SUPERNOVA BOARD UNIT CPU-1

SIZE	CODE	DRAWING NUMBER	REV.
D		005 000 135	

Figure 6-17. Central Processor-1 PCB Assembly (Sheet 2)



UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES XX ± ± .XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010	DRAWN	**DATA GENERAL CORPORATION** SOUTHBORO, MASSACHUSETTS 01772
	CHECKED	
	ENGINEER	TITLE ILLUSTRATED PARTS LISTING, SUPERNOVA BOARD UNIT CPU-2
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES ✓	APPROVED	
MATERIAL	FIRST USED ON	
FINISH	SCALE	SIZE D · CODE · DRAWING NUMBER 005 000 136 · REV.

Figure 6-18. Central Processor-2 PCB Assembly (Sheet 1)

HARDWARE

REF ITEM	DESCRIPTION	DRAWING NO.	REV	UNIT QTY.	TOTAL QTY.
1	SPACER, TOP PCB	002 000 051		3	
2	HANDLE, PCB	002 000 054		1	
3	PRINTED CIRCUIT BOARD, SUPERNOVA, CPU-2	107 000 040		1	
4	INJECTOR	123 000 001		2	
5	RIVET	123 000 002		2	
6	SCREW (HANDLE MTG)	106		4	
7	SCREW (SPACER MTG)	106		3	

REVISIONS

REV.	DESCRIPTION	DRFTG.	APP. BY	DATE

MULTIPLY/DIVIDE OPTION 8007	CENTRAL PROCESSOR UNIT 2					QUANTITY		
CIRCUIT REFERENCE	CIRCUIT REFERENCE	PART NO.	DESCRIPTION	DRAWING NO	REV	BASIC	OPTION 8007	TOTAL
	C1 thru C16	D6R8B35K	CAPACITOR, 6.8µf 35V	103 000 002		16		16
	C17 thru C63	Y5F	CAPACITOR, .05µf 12V	103 000 039		47		47
E86,E89,E100	E15,E20,E45, E55,E80,E84	9002/8889	DIP, QUAD 2-INPUT GATE	100 000 003		6	3	9
E73,E88,E97	E1,E29,E33,E39, E44,E66,E79	9003/8879	DIP, TRIPLE 3-INPUT GATE	100 000 004		7	3	10
	E43,E69	9004/8819	DIP, DUAL 4-INPUT GATE	100 000 005		2		2
	E13,E30,E31,E34, E56,E70	9005/8840	DIP, DUAL 2 WIDE AND-OR-INVERT GATE	100 000 006		6		6
E26,E27	E25,E81,E82	9007	DIP, SINGLE 8-INPUT GATE	100 000 007		3	2	5
E74,E77,E93	E2 thru E6,E18, E19,E23,E35, E36,E37,E50, E54,E57,E63	9008/8848	DIP, SINGLE 4 WIDE AND-OR-INVERT GATE	100 000 008		15	3	18
	E68	9009/8859	DIP, DUAL 4-INPUT BUFFER	100 000 009		1		1
E85,E90,E99	E8,E11,E24,E46, E48,E58,E65, E78	9016/8H90	DIP, HEX INVERTER	100 000 010		8	3	11
	E47	9301	DIP, MSI 1 OF 10 DECODER	100 000 013		1		1
E92,E98	E7,E9,E10,E12, E51,E67	8271	4-BIT SHIFT REGISTERS					
E91,E94	E14,E21,E38,E49, E59,E64,E83	8885/MC3002	QUAD 2-INPUT NAND INTERFACE GATE	100 000 042		6	2	8
E75,E76,E101	E17,E40,E41,E42, E53,E61,E62	74H55	EXPANDABLE 2-WIDE 4-INPUT GATE	100 000 045		7	2	9
E72,E95	E22,E32,E52, E60,E71	MC3061	DUAL J-K FLIP-FLOP	100 000 049		5	2	7
E87,E96	E16,E28	MC3026	DUAL 4-INPUT AND POWER GATE	100 000 053		2	2	4
R11,R12	R1,R2,R3,R4,R6, R8,R10		RESISTOR 1/4W 5% 10K	102 000 086		7	2	9
	R5,R13		RESISTOR 1/4W 5% 470Ω	102 000 055		2		2
	R14		RESISTOR 1/4W 5% 180Ω	102 000 045		1		1

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± XX ± XXX ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010

UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES

MATERIAL

FINISH

DRAWN

CHECKED

ENGINEER

APPROVED

FIRST USED ON

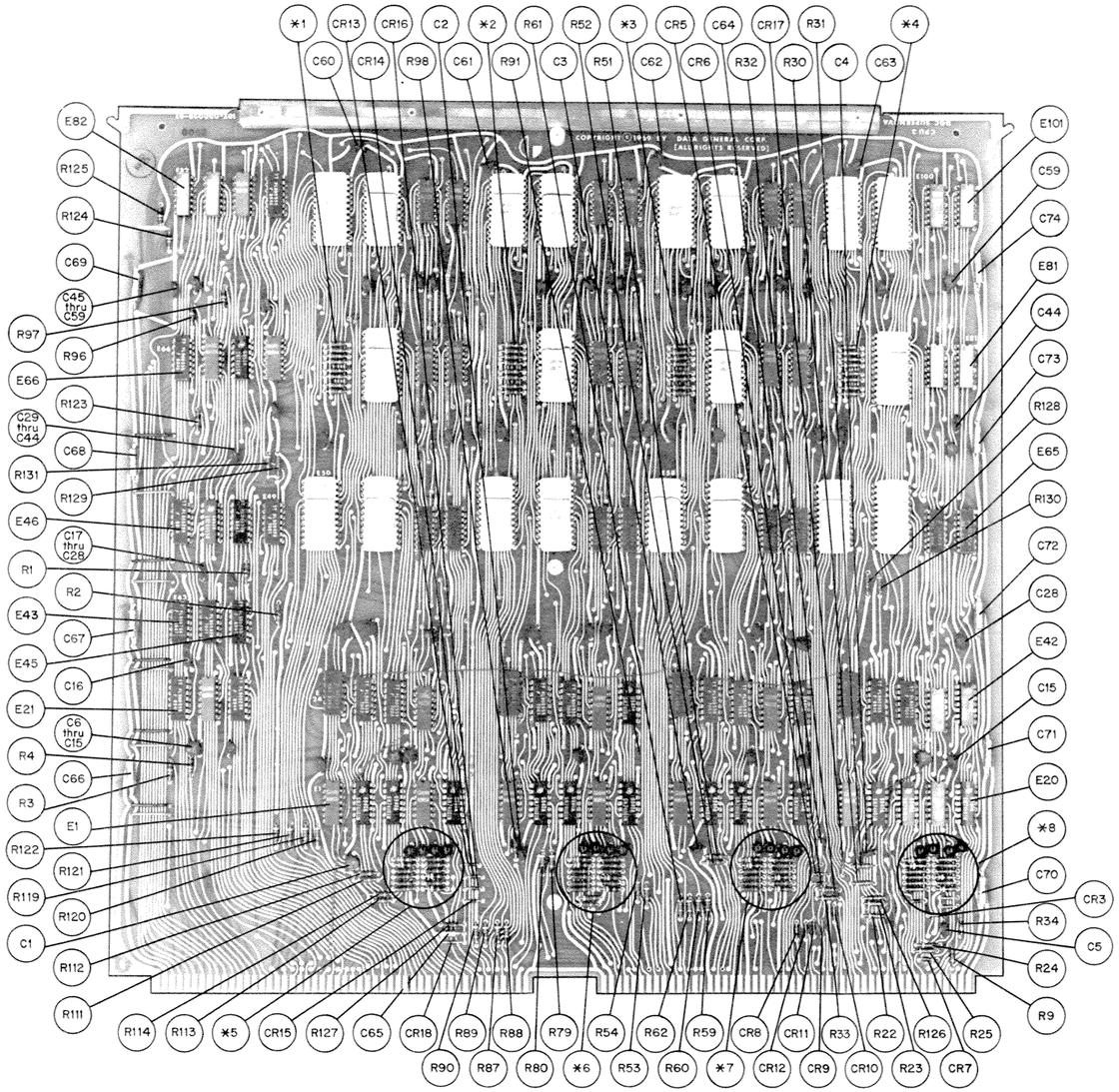
SCALE

DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

TITLE
ILLUSTRATED PARTS LISTING, SUPERNOVA BOARD UNIT CPU-2

SIZE	CODE	DRAWING NUMBER	REV
D		005 000 136	

Figure 6-18. Central Processor-2 PCB Assembly (Sheet 2)



*7

Q8 Q7 Q6 Q5

R45 R41
R46 R42
R50 R39
R49 R43
R48 R40
R47 R44

*8

Q4 Q3 Q2 Q1

R16 R12
R17 R13
R21 R10
R20 R14
R19 R11
R18 R15
CR4 CR2
CR1

*5

Q16 Q15 Q14 Q13

R105 R101
R106 R102
R110 R99
R109 R103
R108 R100
R107 R104

*6

Q12 Q11 Q10 Q9

R73 R69
R74 R70
R78 R67
R77 R71
R76 R73
R75 R72
R81
R82

*3

R55
R35
R56
R36
R57
R37
R58
R38

*4

R26
R5
R27
R6
R28
R7
R29
R8

*1

R115
R92
R116
R93
R117
R94
R118
R95

*2

R83
R63
R84
R64
R85
R65
R86
R66

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± XX ± ± .XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010	DRAWN	DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES	CHECKED	
MATERIAL	ENGINEER	TITLE ILLUSTRATED PARTS LISTING, SUPERNOVA BOARD UNIT CPU-3
FINISH	APPROVED	
	FIRST USED ON	SIZE D · CODE · DRAWING NUMBER 005 000 137 · REV.
	SCALE	

Figure 6-19. Central Processor Unit-3 PCB Assembly (Sheet 1)

HARDWARE

REF ITEM	DESCRIPTION	DRAWING NO.	REV	UNIT QTY.	TOTAL QTY.
1	SPACER, TOP PCB	002 000 051		3	
2	HANDLE, PCB	002 000 054		1	
3	PRINTED CIRCUIT BOARD, SUPERNOVA, CPU-3	107 000 039		1	
4	INJECTOR	123 000 001		2	
5	RIVET	123 000 002		2	
6	SCREW (HANDLE MTG)	106		4	
7	SCREW (SPACER MTG)	106		3	
8	TWISTED PAIR SETS	109		2	
9	WIRE JUMPER, W/SLEEVING			10	

REVISIONS

REV.	DESCRIPTION	DRFTG.	APP. BY	DATE

CENTRAL PROCESSOR UNIT 3

CIRCUIT REFERENCE	PART NO.	DESCRIPTION	DRAWING NO	REV	QTY. PER ASSEMBLY
C1 thru C63	Y5F	CAPACITOR, .05μf 12V	103 000 039		63
C64, C65	150D685X9006A2	CAPACITOR, 6.8μf 6V	103 000 018		2
C66 thru C74	150D685X9035B2	CAPACITOR, 6.8μf 35V	103 000 002		9
CR1 thru CR18	FDH 600	DIODE	101 000 002		18
E23,E46,E83	9002/8889	DIP, QUAD 2-INPUT GATE	100 000 003		3
E45,E48	9003/8879	DIP, TRIPLE 3-INPUT GATE	100 000 004		2
E44,E49	9004/8819	DIP, DUAL 4-INPUT GATE	100 000 005		2
E21,E25,E26,E29, E30,E34,E35,E39, E40,E66,E85	9005/8840	DIP, DUAL 2 WIDE AND-OR-INVERT GATE	100 000 006		11
E43	9007	DIP, SINGLE 8-INPUT GATE	100 000 007		1
E82	9008/8848	DIP, SINGLE 4 WIDE AND-OR-INVERT GATE	100 000 008		1
E67,E69	9016/8H90	DIP, HEX INVERTER	100 000 010		2
E27,E31,E36,E41, E71,E72,E74,E75, E77,E78,E80,E81, E88,E89,E92,E93, E96,E97,E100, E101,	N8271	4-BIT SHIFT REGISTERS	100 000 042		20
E70,E73,E76,E79	N8260	ARITHMETIC LOGIC ELEMENT	100 000 043		4
E50,E51,E54,E55, E58,E59,E62,E63, E86,E87,E90,E91, E94,E95,E98,E99	N8264	3-INPUT, 4-BIT DIGITAL MULTIPLEXER	100 000 044		16
E1,E4,E6,E9,E11, E14,E16,E19,E22, E84	8885/MC3002	QUAD 2-INPUT NAND INTERFACE GATE	100 000 045		10
E24,E28,E33,E38	9316	4-BIT BINARY COUNTER	100 000 047		4
E52,E53,E56, E57,E60,E61, E64,E65	9309	DUAL 4-INPUT MULTIPLEXER	100 000 048		8
E47,E68	74H55	EXPANDABLE 2 WIDE, 4-INPUT GATE	100 000 049		2
E2,E3,E5,E7,E8, E10,E12,E13,E15, E17,E18,E20,E32, E37,E42	74H01	QUAD 2-INPUT POSITIVE NAND GATE WITH OPEN – COLLECTOR OUTPUT	100 000 051		15
Q1-Q16	2N3646	TRANSISTOR	100 000 045		16
R14,R15,R16,R17, R43,R44,R45, R46,R71,R72, R73,R74,R103, R104,R105,R106		RESISTOR 1/4W 5% 39Ω	102 000 029		16
R126,R127		RESISTOR 1/4W 5% 100Ω	102 000 039		2
R128,R129		RESISTOR 1/4W 5% 180Ω	102 000 045		2
R10,R11,R12,R13 R39,R40,R41, R42,R67,R68, R69,R70,R99, R100,R101,R102		RESISTOR 1/4W 5% 220Ω	102 000 047		16
R5 thru R8, R22 thru R33, R35 thru R38, R51 thru R66, R79 thru R90, R92 thru R95, R111 thru R122, R130,R131		RESISTOR 1/4W 5% 470Ω	102 000 055		66
R18 thru R21, R47 thru R50, R75 thru R78, R107 thru R110		RESISTOR 1/4W 5% 750Ω	102 000 060		16
R9,R34,R91,R98		RESISTOR 1/4W 5% 1K	102 000 063		4
R1,R2,R3,R4,R96, R97,R123,R124, R125		RESISTOR 1/4W 5% 10K	102 000 086		9

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
PARTS TO BE FREE FROM BURRS
BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES
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DRAWN
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ENGINEER
APPROVED
FIRST USED ON
SCALE

DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

TITLE
ILLUSTRATED PARTS LISTING, SUPERNOVA BOARD UNIT CPU-3

SIZE D | CODE | DRAWING NUMBER 005 000 137 | REV.

Figure 6-19. Central Processor Unit-3 PCB Assembly (Sheet 2)

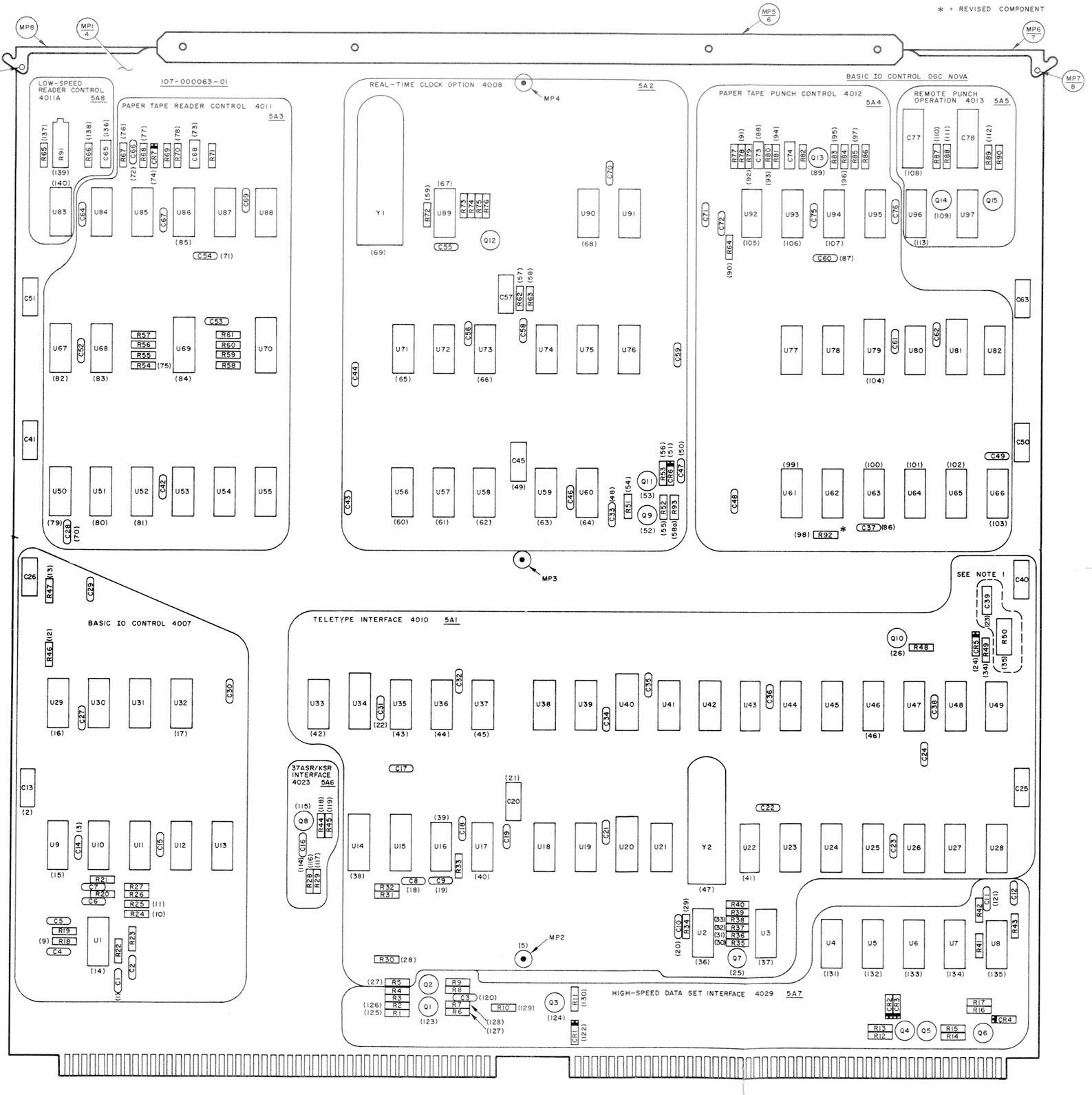


Figure 6-20. I/O Control PCB Assembly

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
4-24	5	007 000 011 01	. . BASIC I/O CONTROL PCB ASSEMBLY, Model 4007(See Figure 4-2-5 for NHA).	REF	C
-1	C1, C2, C6, C4, C5, C7	CD15FD101J	. . . CAPACITOR, 100pf, 500VDC (0036).	6	
-2	C13, C26, C41, C50, C51, C63	D6R8B35K	. . . CAPACITOR, 6.8μfd, 35VDC (0047).	6	
-3	C14, C15, C27, C29, C30	Y5FO-503M	. . . CAPACITOR, .05μfd, 50VDC (0019).	5	
-4	MP1	107 000 030	. . . PRINTED CIRCUIT BOARD, BASIC I/O CONTROL(0010)	1	
-5	MP2, MP3, MP4	002 000 051	. . . SPACER, Top PCB(0010). . . .	3	
-6	MP5	002 000 126	. . . HANDLE, PCB(0010).	1	
-7	MP6, MP8	90-0-6503-11	. . . INJECTOR(0048).	2	
-8	MP7, MP9	90-0-5858-24	. . . RIVET(0048).	2	
-9	R18, R19, R20, R21, R22, R23	CB1025	. . . RESISTOR, 1K, 1/4W, 5% (0011)	6	
-10	R24, R27	CB3315	. . . RESISTOR, 330Ω, 1/4, 5%(0011)	2	
-11	R25, R26	CB3915	. . . RESISTOR, 390Ω, 1/4W, 5%(0011)	2	
-12	R46	CB1815	. . . RESISTOR, 180Ω, 1/4W, 5%(0011)	1	
-13	R47	CB4715	. . . RESISTOR, 470Ω, 1/4W, 5%(0011)	1	
-14	U1, U10, U30	9002	. . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Gates(0013)	3	
		◇8889	. . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Gates(0014)		
-15	U9, U11, U12, U13, U31	9016	. . . INTEGRATED CIRCUIT PACKAGE, Hex Inverter(0013). .	5	
		◇8H90	. . . INTEGRATED CIRCUIT PACKAGE, (0014)		
-16	U29	9003	. . . INTEGRATED CIRCUIT PACKAGE, Three 3-Input NAND Gates(0013).	1	
		◇8879	. . . INTEGRATED CIRCUIT PACKAGE, Three-Input NAND Gates(0014)		

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
4-24	. Continued.	. . . . .	. . . . .		
-17	U32	USN7438	. . . INTEGRATED CIRCUIT FACK-AGE, Quad 2-Input Nand(OC) Gates(0015).	1	
	5A1	007 000 014 00	. . .**OPTIONAL SUBASSEMBLY TELE-TYPE INTERFACE, MODEL No. 4010(0010).	1	
-18	C8, C17 thru C19, C21 thru C24, C32, C34 thru C36, C38	5635-000-Y5FO-503M	. . . . CAPACITOR, .05μfd, 12VDC (0019).	13	
-19	C9	CD15FD101J	. . . . CAPACITOR, 100pf, 500VDC (0036).	1	
-20	C10	CD15FC561J	. . . . CAPACITOR, 560pf, 500VDC (0036)(See Note 1 below). . NOTE1: The value of this capacitor depends on the operating frequency of crystal Y2. C10 is 560pf when the basic 14.08Khz crystal is installed. See Note 2 for additional information concerning teletype crystal options.	1	
-21	C20, C25 C40	D6R8B35K	. . . . CAPACITOR, 6.8μfd, 35VDC (0047).	3	
-22	C31	CK103	. . . . CAPACITOR, .01μfd, 50VDC (0032).	1	
-23	C39	D1R0A35K1	. . . . CAPACITOR, 1μfd, 35VDC (0047).	1	
		◇CK103	. . . . CAPACITOR, .01μfd, 50VDC (0032)(Alternate Capacitor is installed under the 4023 option)		

**See Figure 4-21 for (Device/Computer) Connector information. See Figure 4-24a, Optional Assembly Model 4009, Teletype On-line control.

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
4-24	. Continued.	. . . . .	. . . . .		
-24	CR5	FDH600	. . . . DIODE(0034).	1	
-25	Q7	2N4125	. . . . TRANSISTOR(0026). . . .	1	
-26	Q10	2N4123	. . . . TRANSISTOR(0026). . . .	1	
-27	R5, R33	CB1025	. . . . RESISTOR, 1K, 1/4W, 5%(0011)	2	
-28	R30 thru R32, R48	CB3025	. . . . RESISTOR, 3K, 1/4W, 5%(0011)	4	
-29	R34	CB5625	. . . . RESISTOR, 5.6K, 1/4W, 5% (0011).	1	
-30	R35	CB2215	. . . . RESISTOR, 220Ω, 1/4W, 5% (0011).	1	
-31	R36	CB1815	. . . . RESISTOR, 180Ω, 1/4W, 5% (0011).	1	
-32	R37	CB2725	. . . . RESISTOR, 2.7K, 1/4W, 5% (0011).	1	
-33	R38 thru R40	CB3325	. . . . RESISTOR, 3.3K, 1/4W, 5% (0011).	3	
-34	R49	CB4725	. . . . RESISTOR, 4.7K, 1/4W, 5% (0011).	1	
-35	R50	4410	. . . . RESISTOR, 470Ω, 3W, 5%(0027) NOTE: R50 is deleted when option 4023 is installed.	1	
-36	U2	NE510A	. . . . INTEGRATED CIRCUIT PACKAGE, Dual Amplifier(0014)	1	
-37	U3	8281	. . . . INTEGRATED CIRCUIT PACKAGE, 4 Stage Binary Counter (0014).	1	
-38	U14, U15, U20, U34, U40	9300	. . . . INTEGRATED CIRCUIT PACKAGE, 4 Bit Shift Register (0013).	5	
-39	U16, U39	9004	. . . . INTEGRATED CIRCUIT PACKAGE, Dual 4-Input Gates (0013).	2	
		◇8819	. . . . INTEGRATED CIRCUIT PACKAGE, Dual 4-Input Gates (0013)		
-40	U17, U18 U19, U21	*8881	. . . . INTEGRATED CIRCUIT PACKAGE, 2-Input NAND Gates (0014).	1	

*Factory Selected Component

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
4-24	. Continued.	. . . . .	. . . . .		
-41	U22 thru U28, U41 thru U43	7474	. . . . INTEGRATED CIRCUIT PACKAGE, D-Flop(0038). . . .	10	
		◇8828	. . . . INTEGRATED CIRCUIT PACKAGE, D-Flop(0014)		
-42	U33, U38, U45	9016	. . . . INTEGRATED CIRCUIT PACKAGE, Hex Inverter(0013). .	3	
		◇8H90	. . . . INTEGRATED CIRCUIT PACKAGE, (0014)		
-43	U35	8T80	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Nand Interface Gates(0014). . .	1	
-44	U36	9007	. . . . INTEGRATED CIRCUIT PACKAGE, Single 8-Input Gates (0013).	1	
-45	U37, U44, U47 thru U49	9002	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Gates (0013).	5	
		◇8889	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Gates (0014)		
-46	U46	9003	. . . . INTEGRATED CIRCUIT PACKAGE, Three 3-Input NAND Gates(0013).	1	
		◇8879	. . . . INTEGRATED CIRCUIT PACKAGE, Three-Input NAND Gates(0014)		
-47	Y2	No Number	. . . . CRYSTAL, 14.08Khz(0037)	1	

NOTE 2: The size and frequency of the crystal installed with this optional subassembly depends on the operational Baud rate selected. The 14.08Khz crystal is installed in units operating at 110 Baud. The 19.2Khz crystal is installed in units operating at 150 Baud (under Option 4023 standard low speed for Bell type 103 Data set or equivalent). The 153.6Khz crystal is used in units operating at 1200 Baud (Option 4029 standard high speed for Bell type 202 Data set or equivalent). None-standard rates are also available on customer request, for example a unit selected to operate at 1800 Baud would require a 230.4Khz crystal.

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
4-24	. Continued.	. . . . .	. . . . .		
	5A2	007 000 012 00	. . . OPTIONAL SUBASSEMBLY REAL TIME CLOCK, MODEL No. 4008 (0010).	1	
-48	C33, C43, C44, C46, C47, C56, C58, C59, C70	5635-000-Y5FO-503M	. . . . CAPACITOR, .05μfd, 12VDC (0019).	9	
-49	C45, C57	D6R8B35K	. . . . CAPACITOR, 6.8μfd, 35VDC (0047).	2	
-50	C55	CD7FA821J	. . . . CAPACITOR, 820pf, 500VDC (0036).	1	
-51	CR6	FDH600	. . . . DIODE(0034).	1	
-52	Q9	2N4123	. . . . TRANSISTOR(0026). . . .	1	
-53	Q11, Q12	2N4125	. . . . TRANSISTOR(0026). . . .	2	
-54	R51	CB2225	. . . . RESISTOR, 2.2K, 1/4W, 5% (0011).	1	
-55	R52	CB1525	. . . . RESISTOR, 1.5K, 1/4W, 5% (0011).	1	
-56	R53, R73	CB3025	. . . . RESISTOR, 3K, 1/4W, 5% (0011)	2	
-57	R62	CB2715	. . . . RESISTOR, 270Ω, 1/4W, 5% (0011).	1	
-58	R63	CB2215	. . . . RESISTOR, 220Ω, 1/4W, 5% (0011).	1	
-58a	R93	CB4715	. . . . RESISTOR, 470Ω, 1/4W, 5% (0011).	1	
-59	R72, R74 thru R76	CB3325	. . . . RESISTOR, 3.3K, 1/4W, 5% (0011).	4	
-60	U56	9004	. . . . INTEGRATED CIRCUIT PACKAGE, Dual 4-Input Gates (0013).	1	
		◇8819	. . . . INTEGRATED CIRCUIT PACKAGE, Dual 4-Input Gates (0013)		
-61	U57, U75	9002	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Gates (0013).	2	
		◇8889	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Gates (0014)		

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
4-24	. Continued.	. . . . .	. . . . .		
-62	U58, U74	9016	. . . . INTEGRATED CIRCUIT PACKAGE, Hex Inverter(0013). .	2	
		◇8H90	. . . . INTEGRATED CIRCUIT PACKAGE, (0014)		
-63	U59, U72, U76	7474	. . . . INTEGRATED CIRCUIT PACKAGE, D-Flop(0038). . . .	3	
		◇8828	. . . . INTEGRATED CIRCUIT PACKAGE, D-Flop(0014)		
-64	U60	9008	. . . . INTEGRATED CIRCUIT PACKAGE, Single 4-Wide And-Or-Invert Gates(0013). . . .	1	
		◇8848	. . . . INTEGRATED CIRCUIT PACKAGE, Single 4-Wide And-Or-Invert Gates(0014)		
-65	U71	*8881	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Nand(OC) Gates(0014).	1	
-66	U73	8281	. . . . INTEGRATED CIRCUIT PACKAGE, 4 Stage Binary Counter (0014).	1	
-67	U89	NE510A	. . . . INTEGRATED CIRCUIT PACKAGE, Dual Amplifier(0014)	1	
-68	U90, U91	8280	. . . . INTEGRATED CIRCUIT PACKAGE, Decade Counter(0014)	2	
-69	Y1	No Number	. . . . CRYSTAL, 16KHz(0037). .	1	
	5A3	007 000 018 00	. . .**OPTIONAL SUBASSEMBLY PAPER TAPE READER CONTROL, MODEL No. 4011(0010)	1	
-70	C28, C42, C52, C53, C64, C67, C69	5635-000-Y5FO-503M	. . . . CAPACITOR, .05μfd, 12VDC (0019).	7	
-71	C54	CK103	. . . . CAPACITOR, .01μfd, 50VDC (0032).	1	
-72	C66	CD15FD471J	. . . . CAPACITOR, 470pf, 500VDC (0036).	1	
-73	C68	DR22A20KI	. . . . CAPACITOR, .22μfd, 20VDC (0047).	1	
-74	CR7	FDH600	. . . . DIODE(0034).	1	

*Factory Selected Component

**See Figure 4-21 for (Device/Computer) Connector information

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
4-24	. Continued.	. . . . .	. . . . .		
-75	R54 thru R61, R69 R71	CB3025	. . . . RESISTOR, 3K, 1/4W, 5%(0011)	10	
-76	R67	CB4715	. . . . RESISTOR, 470Ω, 1/4W, 5% (0011).	1	
-77	R68	CB2215	. . . . RESISTOR, 220Ω, 1/4W, 5% (0011).	1	
-78	R70	CB7525	. . . . RESISTOR, 7.5K, 1/4W, 5% (0011).	1	
-79	U50, U87	9016	. . . . INTEGRATED CIRCUIT PACKAGE, Hex Inverter(0013). .	2	
		◇8H90	. . . . INTEGRATED CIRCUIT PACKAGE, (0014)		
-80	U51, U54, U55	*8881	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Nand(OC) Gates(0014).	3	
-81	U52, U53, U85	7474	. . . . INTEGRATED CIRCUIT PACKAGE, D-Flop(0038). . . .	3	
		◇8828	. . . . INTEGRATED CIRCUIT PACKAGE, D-Flop(0014)		
-82	U67, U84, U88	9002	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Gates (0013).	3	
		◇8889	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Gates (0014)		
-83	U68	9004	. . . . INTEGRATED CIRCUIT PACKAGE, Dual 4-Input Gates (0013).	1	
		◇8819	. . . . INTEGRATED CIRCUIT PACKAGE, Dual 4-Input Gates (0013)		
-84	U69, U70	9300	. . . . INTEGRATED CIRCUIT PACKAGE, 4 Bit Shift Register (0013).	2	
		◇9300	. . . . INTEGRATED CIRCUIT PACKAGE, 4 Bit Shift Register (0049)		
-85	U86	9601	. . . . INTEGRATED CIRCUIT PACKAGE, DC Triggerable One Shot(0013).	1	

*Factory Selected Component

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
4-24	. Continued.	. . . . .	. . . . .		
	5A4	007 000 021 00	. . .**OPTIONAL SUBASSEMBLY PAPER TAPE PUNCH CONTROL, MODEL No. 4012(0010).	1	
-86	C37, C48, C49, C61, C62, C71, C75, C76	5635-000-Y5FO-503M	. . . . CAPACITOR, .05μfd, 12VDC (0019).	8	
-87	C60, C72	CK103	. . . . CAPACITOR, .01μfd, 50VDC (0032).	2	
-88	C73, C74	D1R0A35K1	. . . . CAPACITOR, 1μfd, 35VDC (0047).	2	
-89	Q13	2N4125	. . . . TRANSISTOR(0026). . . .	1	
-90	R64, R77	CB1015	. . . . RESISTOR, 100Ω, 1/4W, 5% (0011).	2	
-91	R78	CB7515	. . . . RESISTOR, 750Ω, 1/4W, 5% (0011).	1	
-92	R79	CB2725	. . . . RESISTOR, 2.7K, 1/4W, 5% (0011).	1	
-93	R80	CB1515	. . . . RESISTOR, 150Ω, 1/4W, 5% (0011).	1	
-94	R81, R82	CB1815	. . . . RESISTOR, 180Ω, 1/4W, 5% (0011).	2	
-95	R83	CB1535	. . . . RESISTOR, 15K, 1/4W, 5% (0011).	1	
-96	R84	CB1525	. . . . RESISTOR, 1.5K, 1/4W, 5% (0011).	1	
-97	R85, R86	CB3315	. . . . RESISTOR, 330Ω, 1/4W, 5% (0011).	2	
-98	R92	CB3025	. . . . RESISTOR, 3K, 1/4W, 5% (0011).	1	
-99	U61, U62	7474	. . . . INTEGRATED CIRCUIT PACKAGE, D-Flop(0038). . . .	2	
		◇8828	. . . . INTEGRATED CIRCUIT PACKAGE, D-Flop(0014)		
-100	U63, U71, U80, U82	*8881	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Nand (OC) Gates(0014).	4	
-101	U64, U90	9016	. . . . INTEGRATED CIRCUIT PACKAGE, Hex Inverter(0013). .	2	
		◇8H90	. . . . INTEGRATED CIRCUIT PACKAGE, 0014)		

**See Figure 4-21 for (Device/Computer) Connector information

*Factory Selected Component

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
4-24	. Continued.	. . . . .	. . . . .		
-102	U65, U78	9002	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Gates (0013).	2	
		◇8889	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Gates (0014)		
-103	U66	9004	. . . . INTEGRATED CIRCUIT PACKAGE, Dual 4-Input Gates (0013).	1	
		◇8819	. . . . INTEGRATED CIRCUIT PACKAGE, Dual 4-Input Gates (0013)		
-104	U79, U81	9300	. . . . INTEGRATED CIRCUIT PACKAGE, 4 Bit Shift Register (0013).	2	
		◇9300	. . . . INTEGRATED CIRCUIT PACKAGE, 4-Bit Shift Register (0049)		
-105	U92	9006	. . . . INTEGRATED CIRCUIT PACKAGE, Dual 4-Input And-Or-Invert Gates(0013). . . .	1	
-106	U93	9601	. . . . INTEGRATED CIRCUIT PACKAGE, DC Triggerable One Shot(0013).	1	
-107	U94	NE510A	. . . . INTEGRATED CIRCUIT PACKAGE, Dual Amplifier(0014)	1	
	5A5	007 000 023 00	. . . **OPTIONAL SUBASSEMBLY PAPER TAPE PUNCH REMOTE OPERATION, MODEL No. 4013(0010).	1	
-108	C77, C78	D47C20K1	. . . . CAPACITOR, 47μfd, 20VDC (0047).	2	
-109	Q14, Q15	2N4123	. . . . TRANSISTOR(0026). . . .	2	
-110	R87	CB2245	. . . . RESISTOR, 220K, 1/4W, 5% (0011).	1	
-111	R88, R90	CB3335	. . . . RESISTOR, 33K, 1/4W, 5% (0011).	2	
-112	R89	CB6835	. . . . RESISTOR, 68K, 1/4W, 5% (0011).	1	
-113	U96, U97	9601	. . . . INTEGRATED CIRCUIT PACKAGE, DC Triggerable One Shot(0013).	1	
	5A6	007 000 097 01	. . . **OPTIONAL SUBASSEMBLY 37ASR TELETYPE INTERFACE MODEL No. 4023 (0010).	1	

**See Figure 4-21 for (Device/Computer) Connector Information

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
4-24	. Continued.	. . . . .	. . . . .		
-114	C16	5635-000-Y5FO-503M	. . . . CAPACITOR, .05μfd, 12VDC (0019).	1	
-115	Q8	2N4125	. . . . TRANSISTOR(0026).	1	
-116	R28	CB1025	. . . . RESISTOR, 1K, 1/4W, 5% (0011)	1	
-117	R29	CB1115	. . . . RESISTOR, 110Ω, 1/4W, 5% (0011).	1	
-118	R44	CB7515	. . . . RESISTOR, 750Ω, 1/4W, 5% (0011).	1	
-119	R45	CB1525	. . . . RESISTOR, 1.5K, 1/4W, 5% (0011).	1	
	5A7	007 000 098 00	. . . OPTIONAL SUBASSEMBLY HIGH-SPEED DATA SET INTERFACE, MODEL No. 4029(0010). . .	1	
-120	C3	CD15FC821J	. . . . CAPACITOR, 820pf, 300VDC (0036).	1	
-121	C11, C12	CD15FD101J	. . . . CAPACITOR, 100pf, 500VDC (0036).	2	
-122	CR1 thru CR4	FDH600	. . . . DIODE(0034).	4	
-123	Q1, Q2	2N4125	. . . . TRANSISTOR(0026). . . .	2	
-124	Q3 thru Q6	2N4123	. . . . TRANSISTOR(0026). . . .	4	
-125	R1, R3, R41, R43	CB1025	. . . . RESISTOR, 1K, 1/4W, 5%(0011)	4	
-126	R2, R4	CB1015	. . . . RESISTOR, 100Ω, 1/4W, 5% (0011).	2	
-127	R6, R8	CB7515	. . . . RESISTOR, 750Ω, 1/4W, 5% (0011).	2	
-128	R7, R9	CB1525	. . . . RESISTOR, 1.5K, 1/4W, 5% (0011).	2	
-129	R10, R14, R15, R17, R42	CB3025	. . . . RESISTOR, 3K, 1/4W, 5% (0011)	5	
-130	R11, R12, R13, R16	CB4725	. . . . RESISTOR, 4.7K, 1/4W, 5% (0011).	4	
-131	U4	*8881	. . . . INTEGRATED CIRCUIT PACKAGE, 2-Input NAND Gates (0014).	1	
-132	U5	7474	. . . . INTEGRATED CIRCUIT PACKAGE, D-Flop(0038). . . .	1	
		◇8828	. . . . INTEGRATED CIRCUIT PACKAGE, D-Flop(0014)		

*Factory Selected Component

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
4-24	. Continued.	. . . . .	. . . . .		
-133	U6	9002	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Gates (0013).	1	
		◇8889	. . . . INTEGRATED CIRCUIT PACKAGE, Quad 2-Input Gates (0014)		
-134	U7	9016	. . . . INTEGRATED CIRCUIT PACKAGE, Hex Inverter(0013). .	1	
		◇8H90	. . . . INTEGRATED CIRCUIT PACKAGE, (0014)		
-135	U8	9003	. . . . INTEGRATED CIRCUIT PACKAGE, Three 3-Input NAND Gates(0013).	1	
		◇8879	. . . . INTEGRATED CIRCUIT PACKAGE, Three-Input NAND Gates(0014)		
	5A8	007 000 096 00	. . . OPTIONAL SUBASSEMBLY LOW SPEED READER CONTROL, MODEL No. 4011A(0010). . .	1	
-136	C65	DJR OA35K1	. . . . CAPACITOR, 1μfd, 35VDC (0047).	1	
-137	R65	CB3025	. . . . RESISTOR, 3K, 1/4W, 5%(0011)	1	
-138	R66	CB4725	. . . . RESISTOR, 4.7K, 1/4W, 5% (0011).	1	
-139	R91	3005P-1-203	. . . . POTENTIOMETER, 20K, (0031)	1	
-140	U83	9601	. . . . INTEGRATED CIRCUIT PACKAGE, DC Triggerable One Shot(0013).	1	

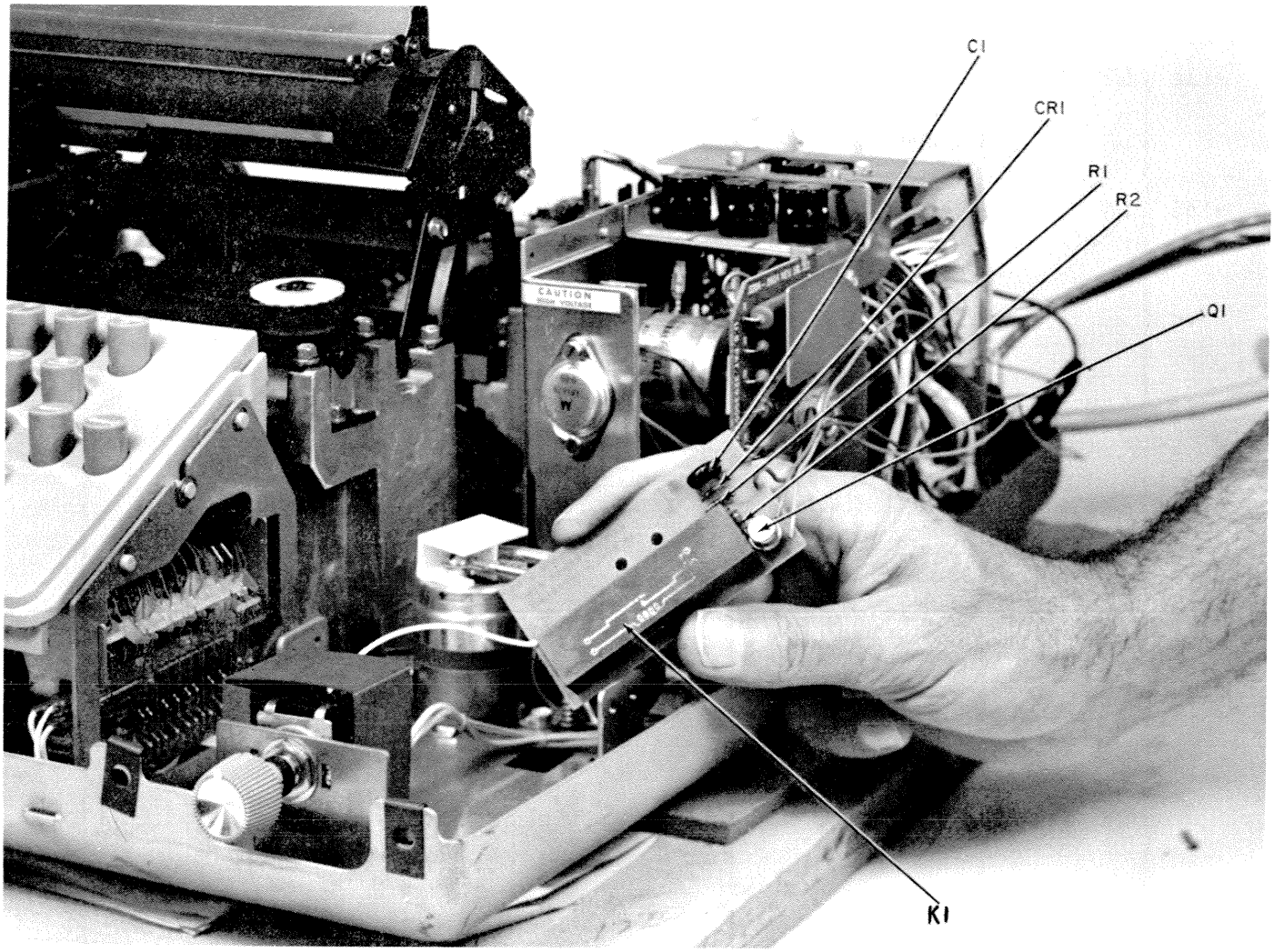
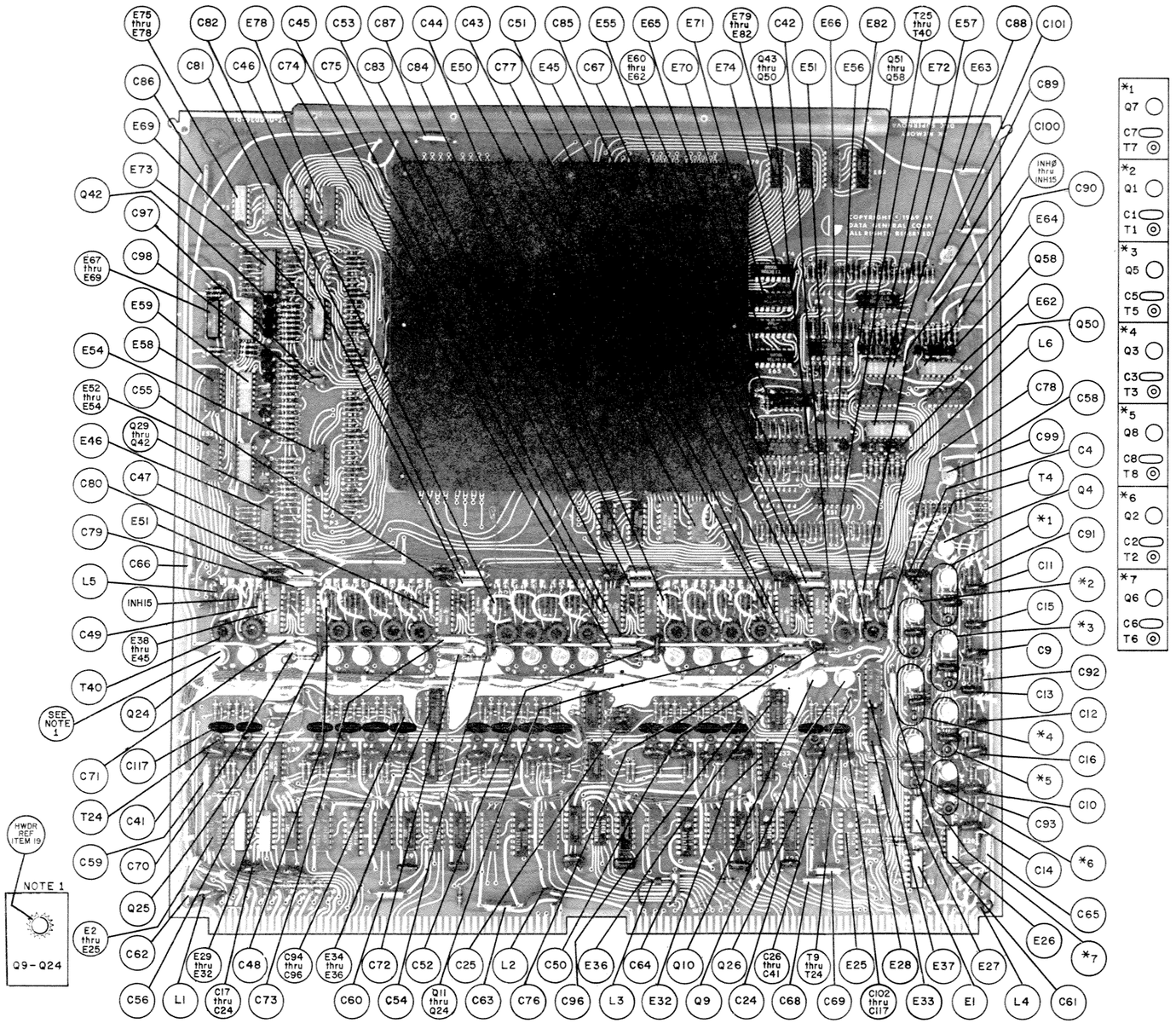
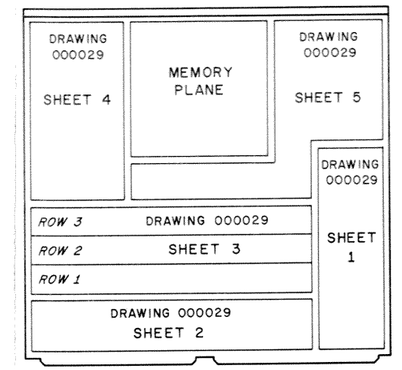


Figure 4-24a. Teletype Modification Kit, Optional Model 4009

Fig. & Index No.	Reference Designator	MFR Part No.	1 2 3 4 5 6 7 8 9 DESCRIPTION	Units Per Assy.	Usable On Code
4-24a	None	118 000 021	. . TELETYPE MODIFICATION KIT, Optional Model 4009. See Teletype Manual under separate cover for NHA. This kit is installed within the teletype to allow the Teletype Reader to be remotely controlled during on -line operation. Model 4009 is used with Optional Assembly Model 4010.		
-1	C1	CD7FA471J	. . . CAPACITOR, 470pf, 500VDC, (0036).	1	
-2	CR1	CD8434	. . . DIODE(0034).	1	
-3	K1	BRSR1-901	. . . RELAY(0040).	1	
-4	Q1	40526	. . . TRIODE THYRISTOR(0039). .	1	
-5	R1	CB1005	. . . RESISTOR, 10Ω, 1/4W, 5%(0011)	1	
-6	R2	CB1015	. . . RESISTOR, 100Ω, 1/4W, 5%(0011)	1	

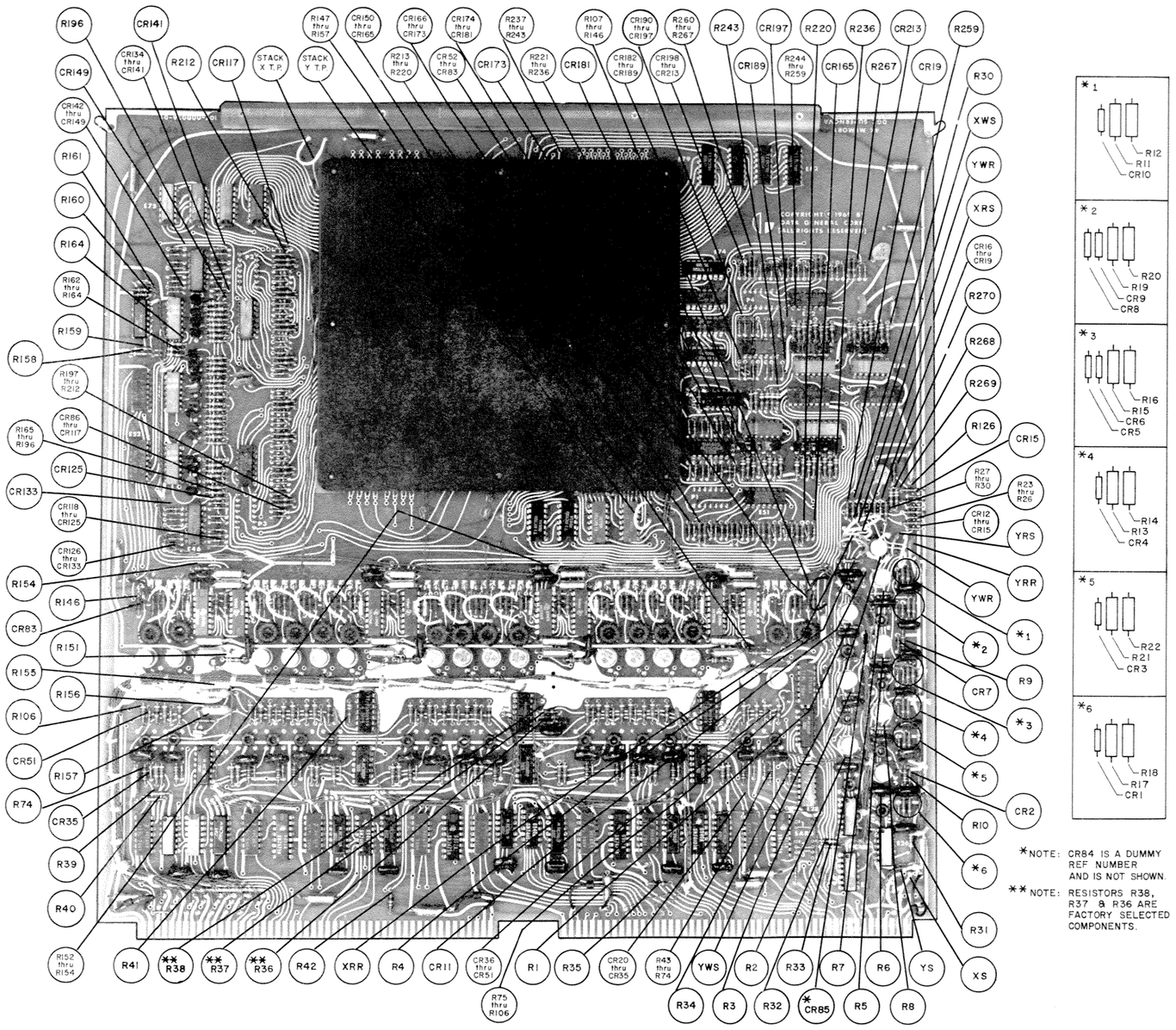




GENERAL LOCATION GUIDE (FOR COMPONENTS) P.C. BOARD-TO-SCHEMATIC RELATIONSHIPS

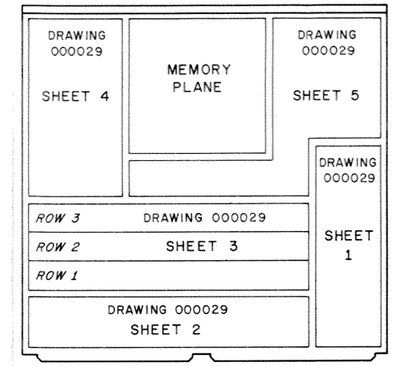
UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± .XX ± ± .XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010	DRAWN	**DATA GENERAL CORPORATION** SOUTHBORO, MASSACHUSETTS 01772
	CHECKED	TITLE ILLUSTRATED PARTS LISTING SUPERNOVA BOARD UNIT 4K MEMORY
	ENGINEER	
	APPROVED	
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES	FIRST USED ON	
MATERIAL		
FINISH	SCALE	SIZE D · CODE · DRAWING NUMBER 005 000 139 · REV. 001

Figure 6-21. Supernova 4K Memory PCB Assembly (Sheet 1)



*NOTE: CR84 IS A DUMMY REF NUMBER AND IS NOT SHOWN.

**NOTE: RESISTORS R38, R37 & R36 ARE FACTORY SELECTED COMPONENTS.



GENERAL LOCATION GUIDE (FOR COMPONENTS) P.C. BOARD-TO-SCHEMATIC RELATIONSHIPS

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010	DRAWN	DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES	CHECKED	TITLE: ILLUSTRATED PARTS LISTING SUPERNOVA BOARD UNIT 4K MEMORY
MATERIAL	ENGINEER	
FINISH	APPROVED	SIZE D · CODE · DRAWING NUMBER 005 000 139 · REV. 001
	FIRST USED ON	
	SCALE	

Figure 6-21. Supernova 4K Memory PCB Assembly (Sheet 2)

SUPERNOVA 4K MEMORY

CIRCUIT REFERENCE	PART NO.	DESCRIPTION	DRAWING NO.	REV	TOTAL QTY.
C94 thru C101		CAPACITOR, .01 μf 50 VDC	103 000 001		8
C58 thru C89	D6R8B35K	CAPACITOR, 6.8μf 35 VDC	103 000 002		32
C11,C12,C15,C16	DM-15-821J	CAPACITOR, 820 pf 500 VDC	103 000 005		4
C25, C102 thru C117	DM-15-221J	CAPACITOR, 220 pf 500 VDC	103 000 006		17
C42 thru C49 C90 thru C93	150D685X9006A2	CAPACITOR, 6.8 μf 6 VDC	103 000 018		12
C13,C14	DM-15-471J	CAPACITOR, 470 pf 500 VDC	103 000 004		2
C17 thru C24	DM-15-101J	CAPACITOR, 100 pf 500 VDC	103 000 031		8
C9,C10,C26 thru C41	DM-15-122J	CAPACITOR, 1200 pf 500 VDC	103 000 035		18
C50 thru C57	DM-15-330J	CAPACITOR, 33 pf 500 VDC	103 000 040		8
C1 thru C8	DM-15-561J	CAPACITOR, 560 pf 500 VDC	103 000 041		8
CR1 thru CR213	CD8434	DIODE	101 000 002		213
E46,E51,E54, E55,E66,E72, E70,E73,E69	-6405	QUAD TRANSISTOR	100 000 001		8
E28,E34,E36	9009/8859	DUAL 4-INPUT BUFFER	100 000 009		3
E2,E6,E8,E12, E14,E18,E20, E24,E37,E53, E56,E57,E59, E63,E64,E68	9016/8H90	HEX INVERTER	100 000 010		16
E52,E58,E61, E62	9301	MSI ONE-OF-TEN DECODER	100 000 013		4
E7,E13,E19, E25	7475	(DUAL) QUADRUPLE LATCHES	100 000 050		4
E4,E10,E16, E22	7438	QUAD 2-INPUT POSITIVE NAND GATE	100 000 051		4
E38,E39,E40 E41,E42,E43 E44,E45	7524	MEMORY SENSE AMPLIFIER	100 000 052		8
E3,E5,E9,E11, E15,E17,E21,E23	MC3061	DUAL J-K FLIP-FLOP	100 000 053		8
E26,E27,E33, E35,E60,E67	MC3026	DUAL 4-INPUT AND POWER GATE	100 000 054		6
E1,E29,E30, E31,E32	MC3003	QUAD NEGATIVE AND GATE	100 000 063		5
E47,E48,E49, E50,E65,E70, E71,E74,E75, E76,E77,E78, E79,E80,E81, E82	T1BC728	DIODE ARRAY	100 000 002		16
Q1 thru Q24	2N3725	TRANSISTOR	101 000 015		24
Q25	2N4403	TRANSISTOR	101 000 052		1
Q26 thru Q58	2N4123	TRANSISTOR	101 000 016		33
R112,R122,R132, R142		RESISTOR 1/4W ± 5% 10Ω	102 000 015		4
R162,R163,R164, R240,R241,R242 R243		RESISTOR 1/4W ± 5% 39Ω	102 000 029		7
R75,R77,R79 R81,R83,R85 R87,R89,R91 R93,R95,R97 R99,R101,R103, R105		RESISTOR 1/4W ± 5% 47Ω	102 000 031		16
R166,R168,R170 R172,R174, R176,R178,R180 R182,R184,R186 R188,R190,R192 R194,R196,R221 R223,R225,R227 R229,R231,R233 R235,R244,R246		RESISTOR 1/4W ±5% 390Ω	102 000 053		32

SUPERNOVA 4K MEMORY (CONT.)

CIRCUIT REFERENCE	PART NO.	DESCRIPTION	DRAWING NO.	REV	TOTAL QTY.
R248,R250,R252, R254,R256,R258,		RESISTOR 1/4 W ± 5% 390Ω	102 000 053		32
R1 thru R8, R39, R40,R45,R46,R48 R49,R53,R54,R56		RESISTOR 1/4 W ± 5% 470Ω	102 000 055		46
R57,R61,R62,R64 R65,R69,R70,R72 R73,R76,R78,R80 R82,R84,R86,R88 R90,R92,R94,R96					
R98,R100, R102,R104,R106, R158,R159,R238, R239					
R9,R10,R31,R160, R161, R237		RESISTOR 1/4W ± 5% 680Ω	102 000 059		6
R43, R44, R47, R50 R51, R52, R55, R58, R59,R60,R63,R66, R67,R68,R71,R74		RESISTOR 1/4W ± 5% 750Ω	102 000 060		16
R38		RESISTOR 1/4 W ± 5% 1.2K	102 000 065		1
R23 thru R30, R197 thru R220, R270		RESISTOR 1/4 W ± 5% 1.5K	102 000 067		33
R11 thru R22, R111, R121,R131,R141		RESISTOR 1/4W ± 5% 2.2K	102 000 071		16
R41,R147, thru R154, R165, R167 R169, R171, R173 R175, R177, R179 R181, R183, R185 R187, R189, R191 R193, R195, R222 R224, R226, R228 R230, R232, R234 R236, R245, R247 R249, R251, R253 R255, R257, R259 R268, R269		RESISTOR 1/4 W ± 5% 3.3K	102 000 075		43
R36		RESISTOR 1/4 W ± 5 %4.7K	102 000 078		1
R37		RESISTOR 1/4 W ± 5 %6.8 K	102 000 082		1
R32 thru R35, R42		RESISTOR 1/4W ± 5 % 10 K	102 000 086		5
R107 thru R110, R113 thru R120, R123 thru R130, R133 thru R140 R143 thru R146 R157		RESISTOR 1/10W ± 1% 150Ω	102 000 185		33
R155, R156		RESISTOR 3 W ± 5% 180Ω	102 000 192		2
T1 thru T24		TRANSFORMER MEMORY	104 000 012		24
T25 thru T40		TRANSFORMER-BALUN	104 000 013		16
L1 thru L6	56-590-653B	FERRITE CORE INDUCTOR	105 000 006		6

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
± XX ± ±
± XXX ± ±
PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES
MATERIAL
FINISH

DRAWN
CHECKED
ENGINEER
APPROVED
FIRST USED ON
SCALE

DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

TITLE
ILLUSTRATED PARTS LISTING
SUPERNOVA BOARD UNIT
4K MEMORY

SIZE	CODE	DRAWING NUMBER	REV.
D		005 000 139	01

Figure 6-21. Supernova 4K Memory PCB Assembly (Sheet 3)

SUPERNOVA MEMORY HARDWARE

REF ITEM	DESCRIPTION	DRAWING NO.	REV.	UNIT QTY.	TOTAL QTY.
1	SPACER, TOP PCB	002 000 051		3	
2	HANDLE, PCB	002 000 054		1	
3	PRINTED CIRCUIT BOARD, MEMORY, 4K SUPERNOVA	005 000 071		1	
4	INJECTOR	123 000 001		2	
5	RIVET	123 000 002		2	
6	SCREW (HANDLE MTG)	106		4	
7	SCREW (SPACER MTG)	106		3	
8	PLATE COVER-SUPERNOVA	002 000 108		1	
9	PCB, 4K MEMORY, SUPERNOVA (1ST ASSEMBLY)	107 000 036		1	
10	AMP MOD-U PINS	111 000 031		104	
11	PCB, SUB ASS'Y W/O CORE MAT SUPERNOVA 4K (2ND ASSEMBLY)	004 000 072		1	
12	SUPERNOVA CORE MAT 4K X 16	118 000 029		1	
13	CORE (P/O 104 000 001)	105 000 001		16	
14	CORE CF 101 0-6 (P/O 104 000 009)	105 000 009		24	
15	TRIPLET SETS	109		8	
16	TWISTED PAIR SETS	109		10	
17	CONTACT (AMP NO. 4-330808-9) COMPONENT LEAD SPRING	111 000 029		12	
18	TRANSIPAD (MILTON-ROSS #10007)	123 000 035		16	
19	HEAT SINK (BIRCHER)	123 000 036		16	

REVISIONS

REV.	DESCRIPTION	DRFTG.	APP. BY	DATE
001	AS PER ECO-012			4/29/70

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±
PARTS TO BE FREE FROM BURRS
BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES
MATERIAL
FINISH

DRAWN
CHECKED
ENGINEER
APPROVED
FIRST USED ON
SCALE

DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

TITLE
ILLUSTRATED PARTS LISTING
SUPERNOVA BOARD UNIT
4K MEMORY

SIZE	CODE	DRAWING NUMBER	REV.
D		005 000 139	001

Figure 6-21. Supernova 4K Memory PCB Assembly (Sheet 4)

SECTION VII

REFERENCE DRAWINGS

7-1. GENERAL

This section contains all of the Data General electrical reference drawings for the Supernova Central Processor, the Supernova 4K Memory, and the Basic I/O Control. Table 7-1 lists all of the reference drawings bound in this section.

Table 7-1. Reference Drawings

Title	Drawing No.
Supernova - Flow Chart (Fetch - Defer - Execute)	001 000 061 (Sheet 1)
Supernova - Flow Chart Key - DCH - PI	001 000 061 (Sheet 2)
Supernova Console	001 000 060
CPU-1 - Supernova Processor & Memory Timing	001 000 033 (Sheet 1)
CPU-1 - Supernova Input/Output	001 000 033 (Sheet 2)
CPU-1 - Supernova Console Logic	001 000 033 (Sheet 3)
CPU-2 - Supernova Decoding - IR - States	001 000 047 (Sheet 1)
CPU-2 - Supernova Adder - Multiplexor Register Load - Controls	001 000 047 (Sheet 2)
SEL & REG Drive Logic CPU-3	001 000 035 (Sheet 1)
Major Registers Gating - Adder Bits 0-3 CPU-3	001 000 035 (Sheet 2)

Title	Drawing No.
Major Registers Gating - Adder Bits 4-7 CPU-3	001 000 035 (Sheet 3)
Major Registers Gating - Adder Bits 8-11 CPU-3	001 000 035 (Sheet 4)
Major Registers Gating - Adder Bits 12-15 CPU-3	001 000 035 (Sheet 5)
Supernova Memory Timing	001 000 062 (Sheet 1)
4K Memory Flippers	001 000 029 (Sheet 1)
4K Memory MA & MB Register	001 000 029 (Sheet 2)
4K Memory Sense & Inhibit	001 000 029 (Sheet 3)
4K Memory X Selectors	001 000 029 (Sheet 4)
4K Memory Y Selectors	001 000 029 (Sheet 5)
Back Panel Supernova	001 000 046 (Sheet 1)
Supernova Power Supply	001 000 063 (Sheet 1)
Supernova Resistor Board Schematic	001 000 101
IO Bus Receivers & Common Select	001 000 070
Teletype Control	001 000 071

APPENDICES

APPENDIX A

LOGIC DIAGRAMS

AND

TRUTH TABLES

FOR

SUPERNOVA INTEGRATED

CIRCUIT PACKAGES

INTRODUCTION

This Appendix is a compilation of the Logic Diagrams and Truth Tables for the Integrated Circuit (IC) Packages used in the Supernova logic. Information presented in this section is intended to supplement the electrical (assembly logic diagrams) drawings and the Integrated Circuit list in Section VI of this manual (Parts Listing). The data presented herein is cataloged first alphabetically then by number, where the alphabetical prefixes of the number are germane to the manufacturer's identification of the part rather than defining operational parameters (e.g., temperature, case construction, etc.). Table A-1 is an index listing the types of IC's shown in this section and the corresponding page number. All of the logical elements listed use positive logic, i.e., the highest voltage equals a logic 1.

Table A-1. IC INDEX

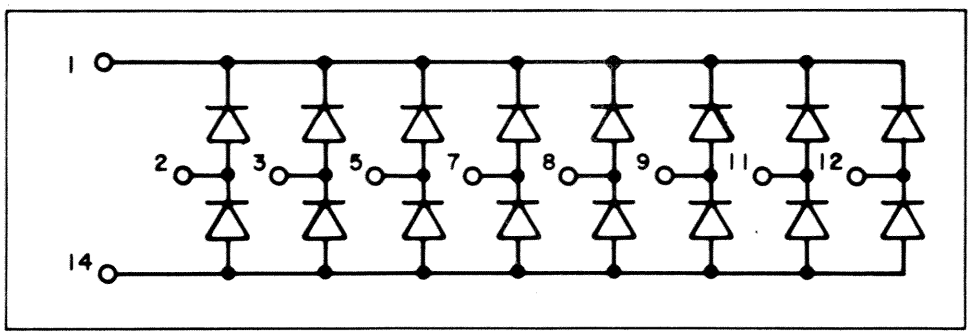
Table A-1. IC INDEX (Continued)

IC	Manufacturer	Page No.
8264	Signetics	
8271	Signetics	
8280	Signetics	
8281	Signetics	
8881	Signetics	
8885	Signetics	
9002	Fairchild	
9003	Fairchild	
9004	Fairchild	
9005	Fairchild	
9006	Fairchild	
9007	Fairchild	
9008	Fairchild	
9009	Fairchild	
9016	Fairchild	
9300	Fairchild	
9301	Fairchild	
9309	Fairchild	
9316	Fairchild	
9601	Fairchild	

BC728

16 Diode Array

LOGIC DIAGRAM

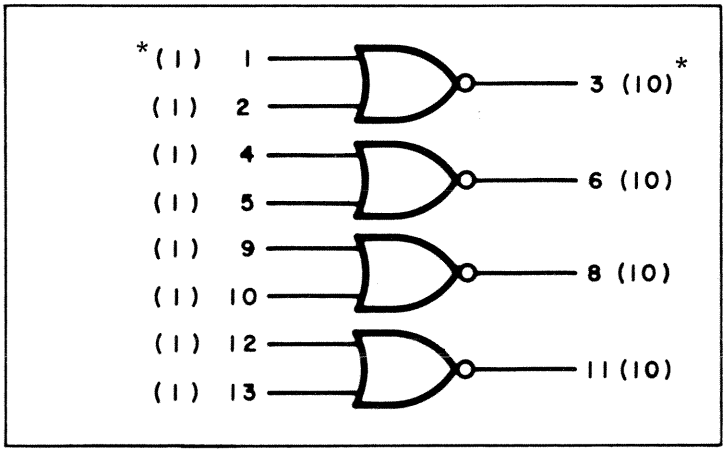


TRUTH TABLE N/A For BC728

MC3002

Quad 2 - Input NOR Gate

LOGIC DIAGRAM



*Loading Max. Shown in Parenthesis

t_{pd} = 6.0 ns typ

P_D = 122 mW typ/pkg

TRUTH TABLE

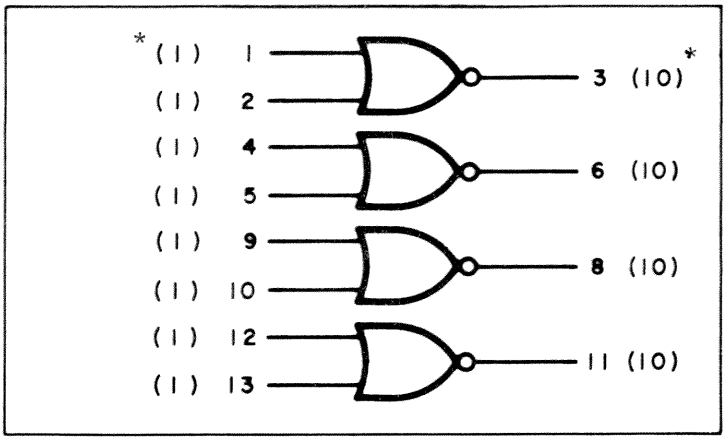
$3 = \overline{1 + 2}$
$6 = \overline{4 + 5}$
$8 = \overline{9 + 10}$
$11 = \overline{12 + 13}$

V_{CC} = Pin 14, GND = Pin 7

MC3003

Quad 2-Input OR Gate

LOGIC DIAGRAM



*Loading Max. Shown in Parenthesis

t_{pd} = 9.0 ns typ

P_D = 150 mW typ/pkg

TRUTH TABLE

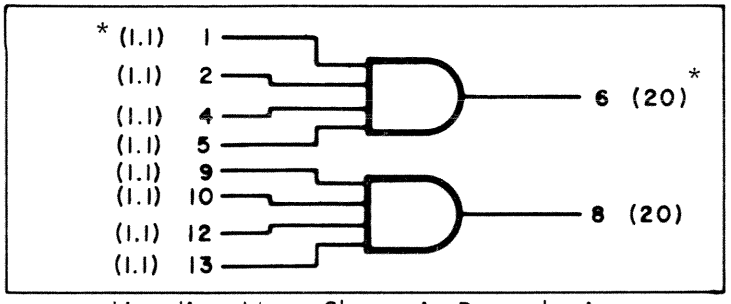
3 = 1 + 2
6 = 4 + 5
8 = 9 + 10
11 = 12 + 13

V_{CC} = Pin 14, GND = Pin 7

MC3026

Dual 4-Input AND Power Gate

LOGIC DIAGRAM



*Loading Max. Shown in Parenthesis

t_{pd} = 9.0 ns typ

P_D = 90 mW typ/pkg

TRUTH TABLE

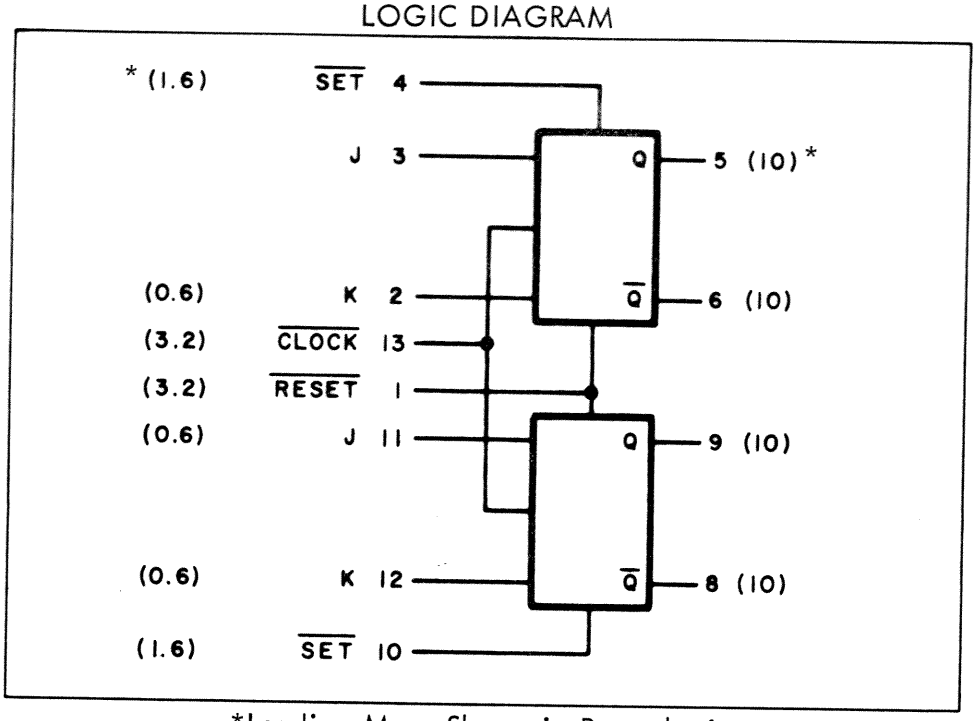
6 = 1·2·4·5
8 = 9·10·12·13

V_{CC} = Pin 14, GND = Pin 7

MC3061

Dual J-K Flip-Flop

LOGIC DIAGRAM



*Loading Max. Shown in Parenthesis

t = 50 MHz

P_D = 100 mW typ/pkg

TRUTH TABLE

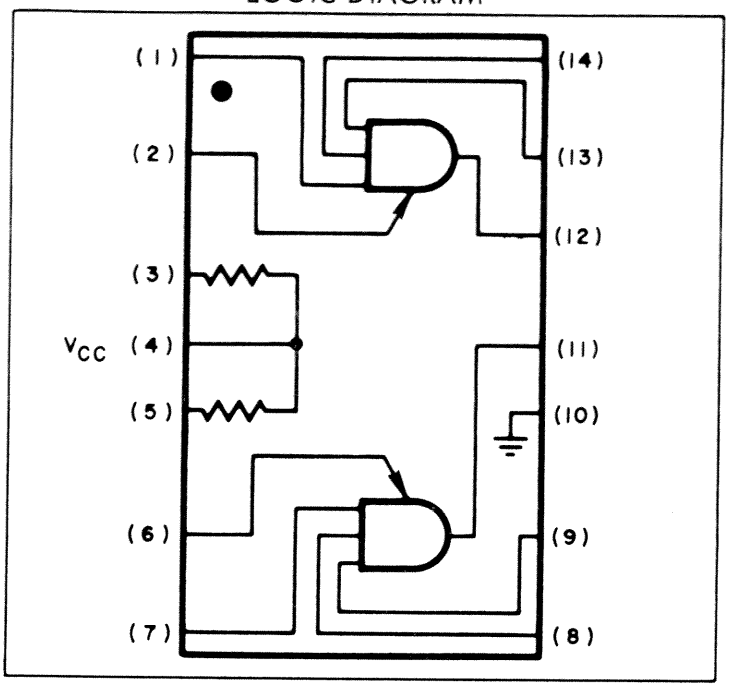
J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

V_{CC} = Pin 14, GND = Pin 7

SG83

Dual Pulse Shaper/Delay AND Gate

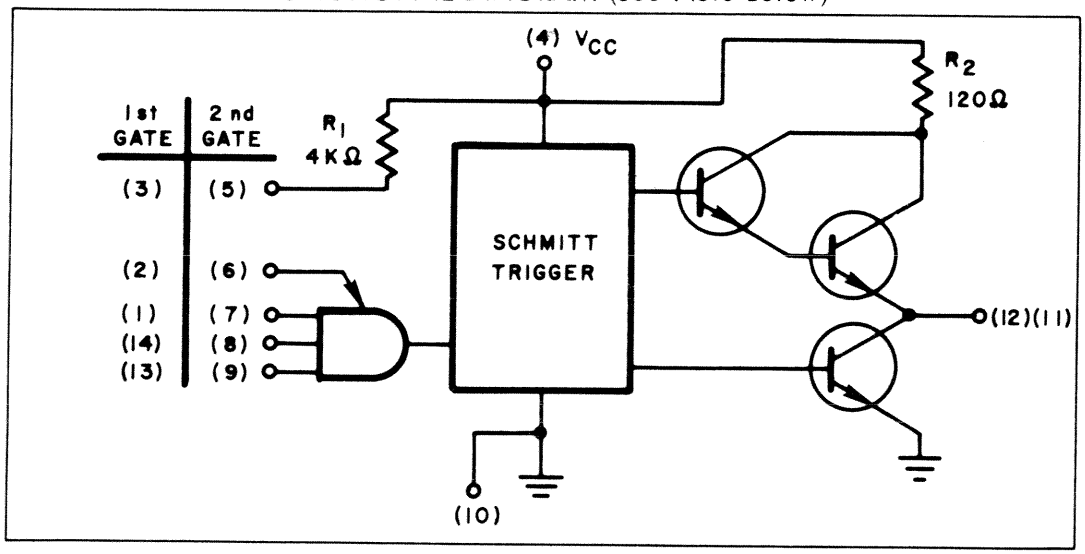
LOGIC DIAGRAM



TRUTH TABLE

$12 = (1 \cdot 14 \cdot 13) \cdot 2$
$11 = (7 \cdot 8 \cdot 9) \cdot 6$

FUNCTIONAL DIAGRAM (See Note Below)

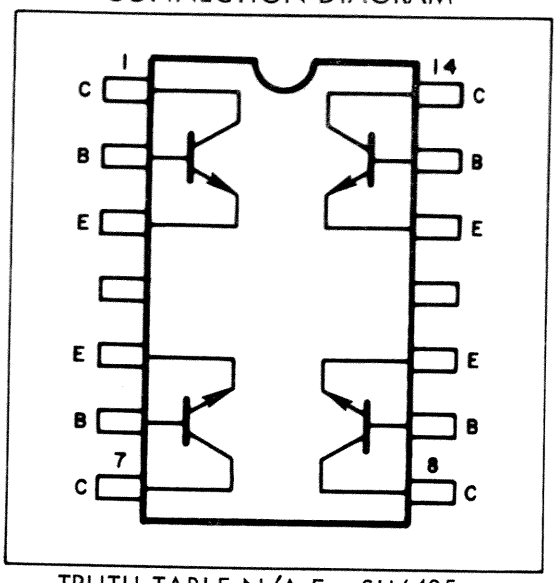


NOTE: Functionally, the SG83 is made up of two distinct AND gates with each gate consisting of a three-input multiple-emitter AND element, a Schmitt trigger type circuit and a SUHL output network. Each AND gate has a point brought out to an external terminal. An external capacitor may be connected to this point to delay the AND function until this capacitor is charged through an internal 4K resistor. This resistor is also brought out to allow external resistance coupling. The Schmitt trigger type circuit has a positive going threshold of approximately 1.2 volts, a negative going threshold of approximately 0.8 volts, and a hysteresis of approximately 0.4 volts. These trigger circuits drive typical SUHL output networks which provide high current and low voltage in the Logic "0" state, and high current and high voltage in the Logic "1" state.

SH6405

NPN Quad Core Drivers

CONNECTION DIAGRAM

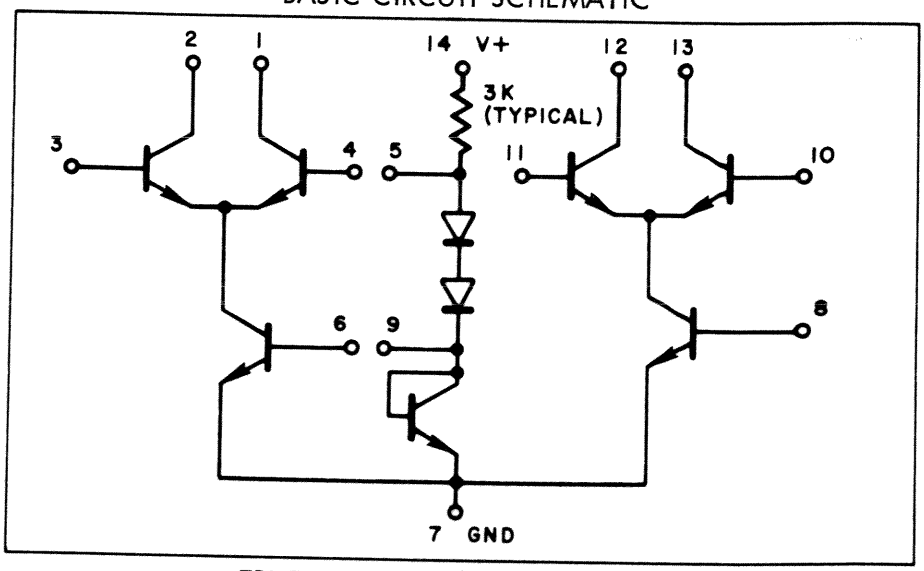


TRUTH TABLE N/A For SH6405

NE510A

Amplifier

BASIC CIRCUIT SCHEMATIC



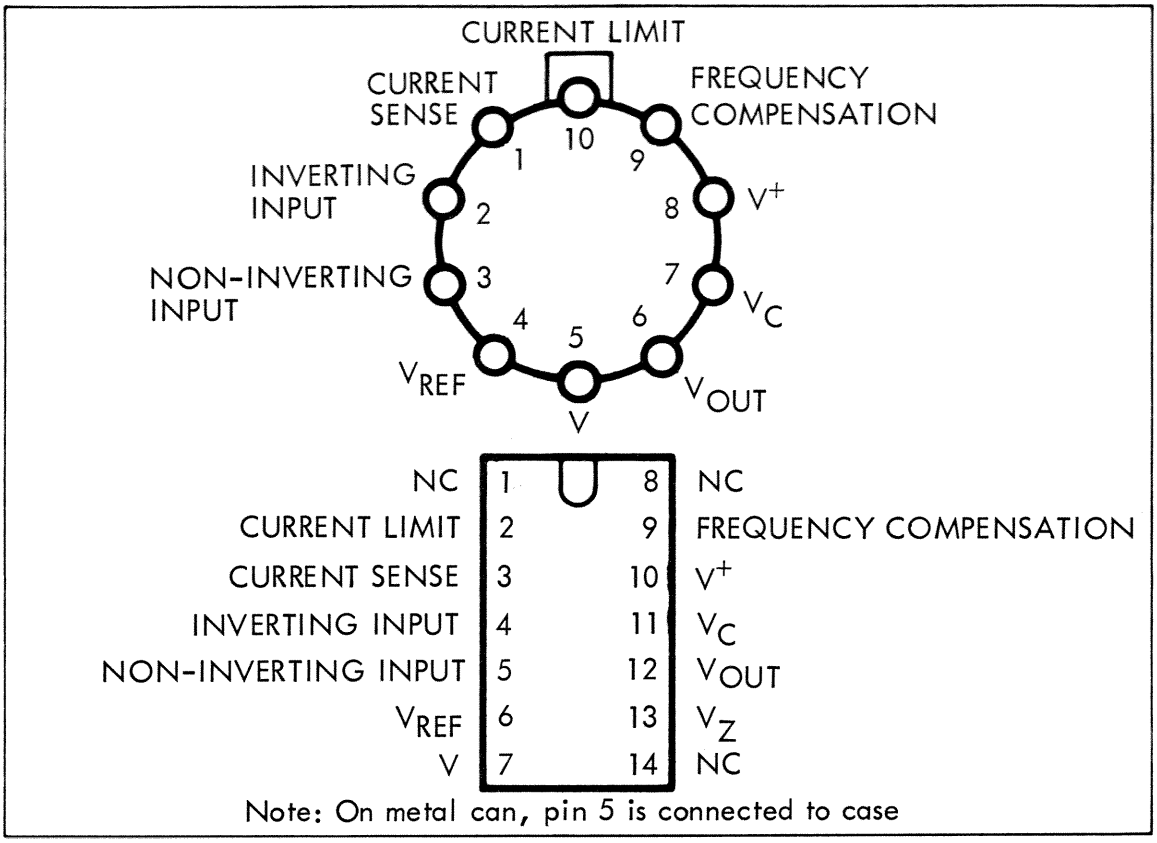
TRUTH TABLE N/A For NE 510A

NOTE: NE510 may be connected as either a high-gain, common-emitter, common-base, cascode amplifier or a common-collector, common-base, differential amplifier that is useful in critical limiter applications. Automatic gain control may be applied to either circuit.

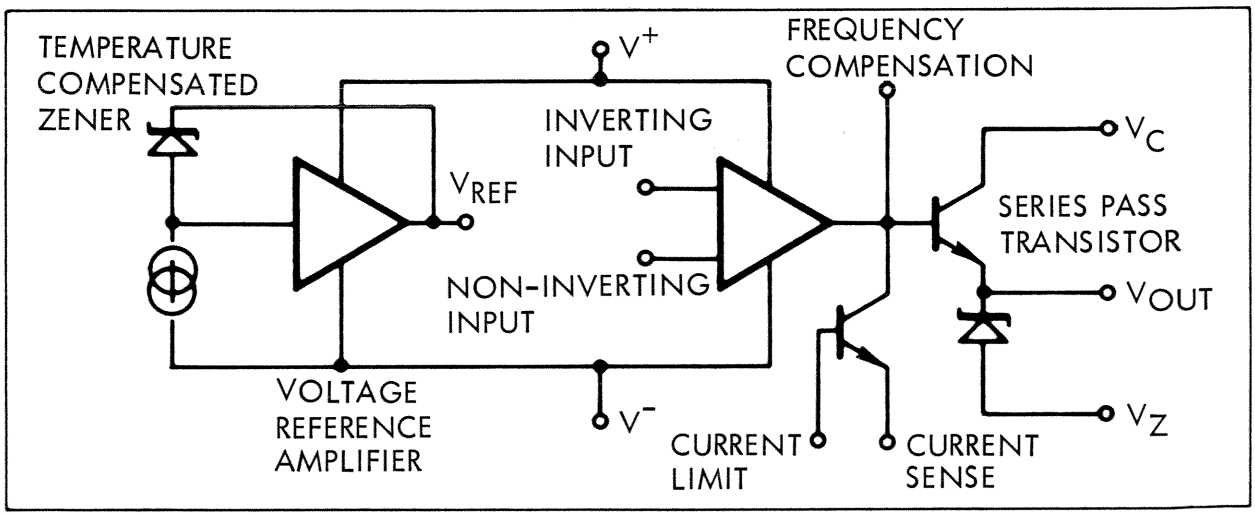
μA723C

Precision Voltage Regulator

CONNECTIONS DIAGRAMS (TOP VIEWS)



EQUIVALENT CIRCUIT

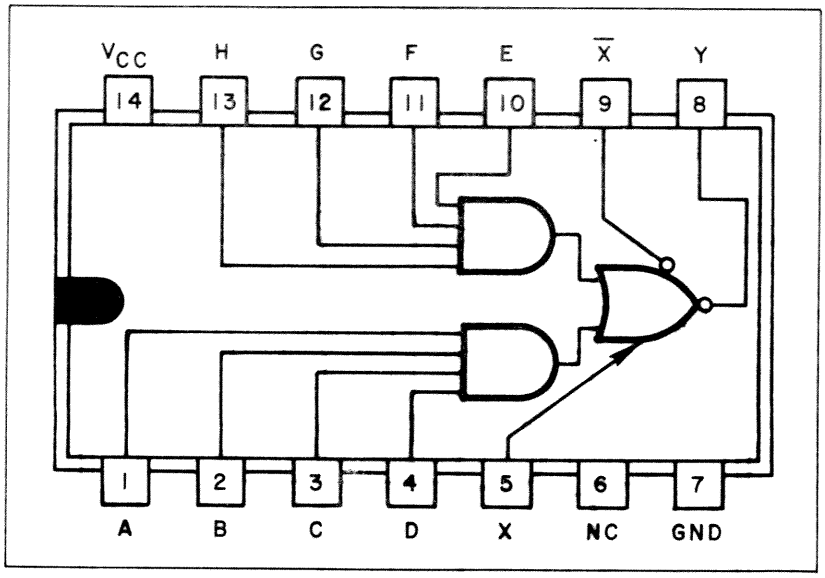


TRUTH TABLE N/A For μA723C

74H55

Expandable 4-Input AND-OR-INVERT Gates

LOGIC DIAGRAM



Both expander inputs are used simultaneously for expanding.
If expander is not used leave X and $\overline{X}$ pins open.

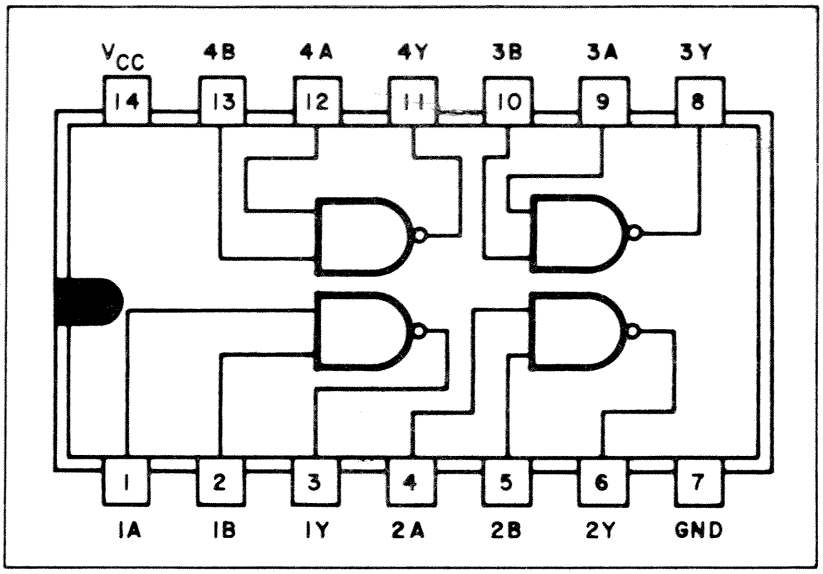
TRUTH TABLE

(positive logic)	Y = (ABCD) + (EFGH) + (X)
	X = Output of SN54H60/SN74H60 or SN54H62/SN74H62 circuit.

7438

Quadruple 2 - Input Positive NAND Gates
(With Open - Collector Outputs)

LOGIC DIAGRAM



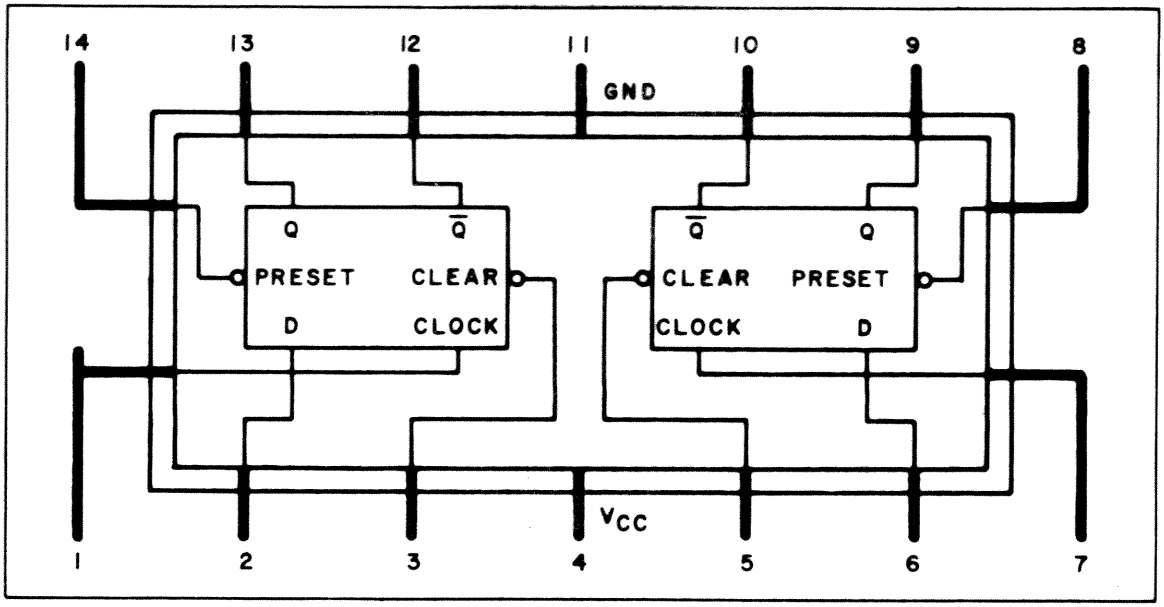
TRUTH TABLE

(positive logic) $Y = \overline{AB}$

7474

Dual D-Type edge-triggered flip-flop

LOGIC DIAGRAM



Propogation delay - 24 nsec

Power dissipation - 84 mW total for two flip-flops (42 mW per flip-flop)

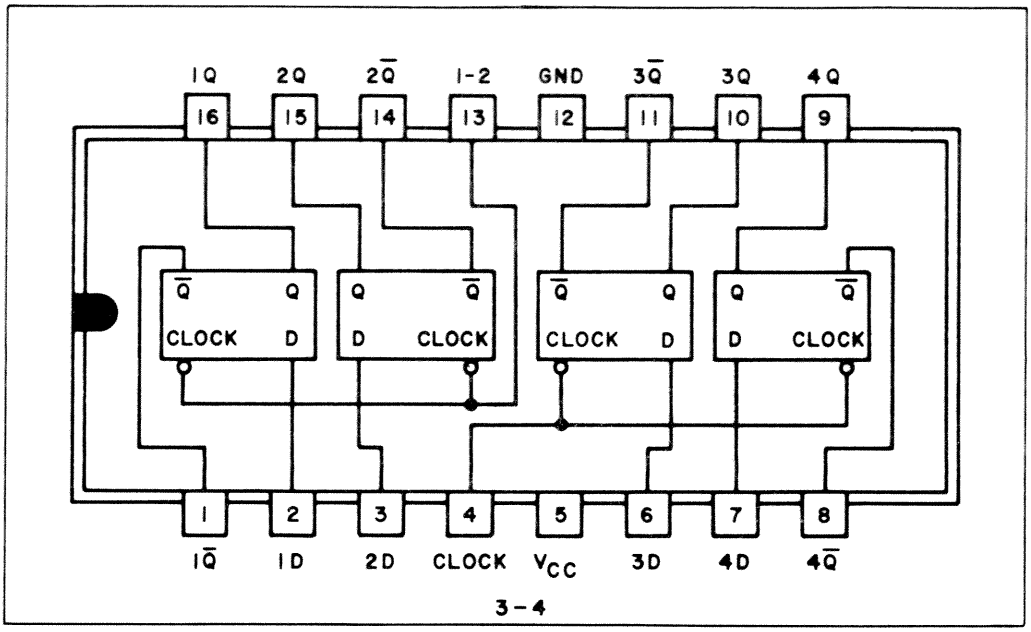
TRUTH TABLE

t_n	$t_n + 1$			
D	Q	$\overline{Q}$	PRESET	CLEAR
0 1	0 1	1 0		
	1	0	0	
	0	1		0

7475

4 - Bit Bistable Latch

LOGIC DIAGRAM



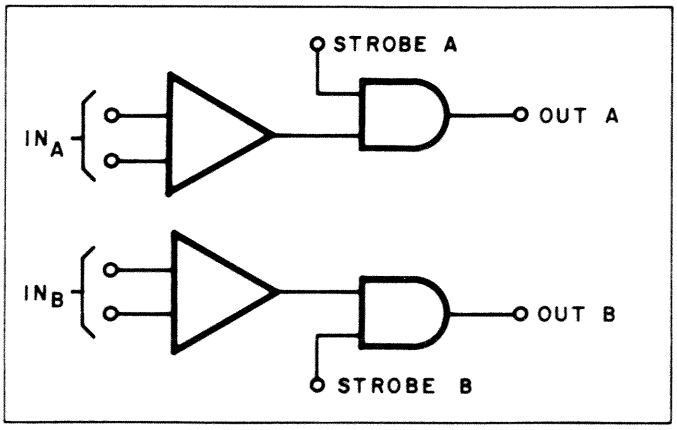
TRUTH TABLE
(EACH LATCH)

t_n	t_{n+1}
D	Q
1	1
0	0

7524

Dual Sense Amplifiers

LOGIC DIAGRAM



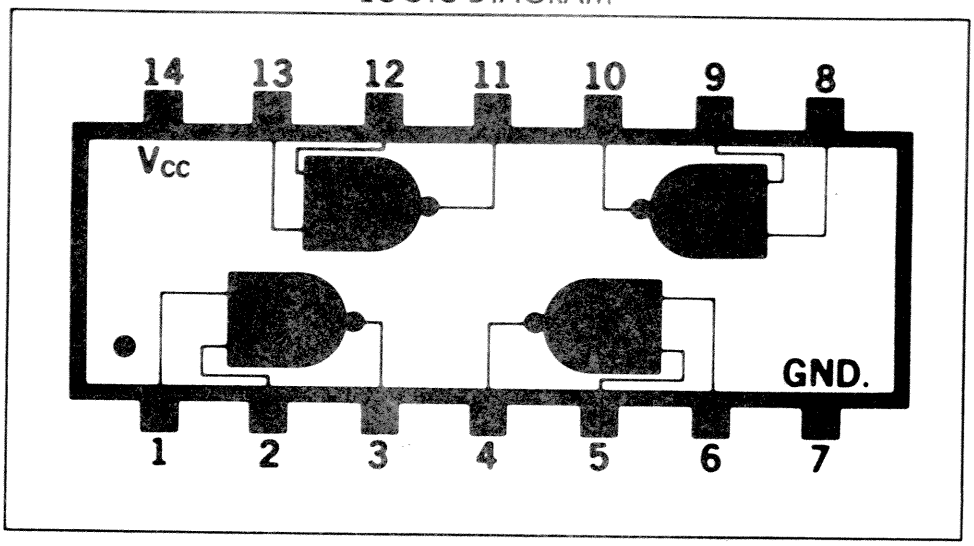
TRUTH TABLE

$IN_A \cdot$ STROBE A = OUT A
$\overline{IN_A} \cdot$ STROBE A = $\overline{\text{OUT A}}$
$IN_B \cdot$ STROBE B = OUT B
$\overline{IN_B} \cdot$ STROBE B = $\overline{\text{OUT B}}$

8T80

Quad 2 - Input NAND Interface Gate

LOGIC DIAGRAM



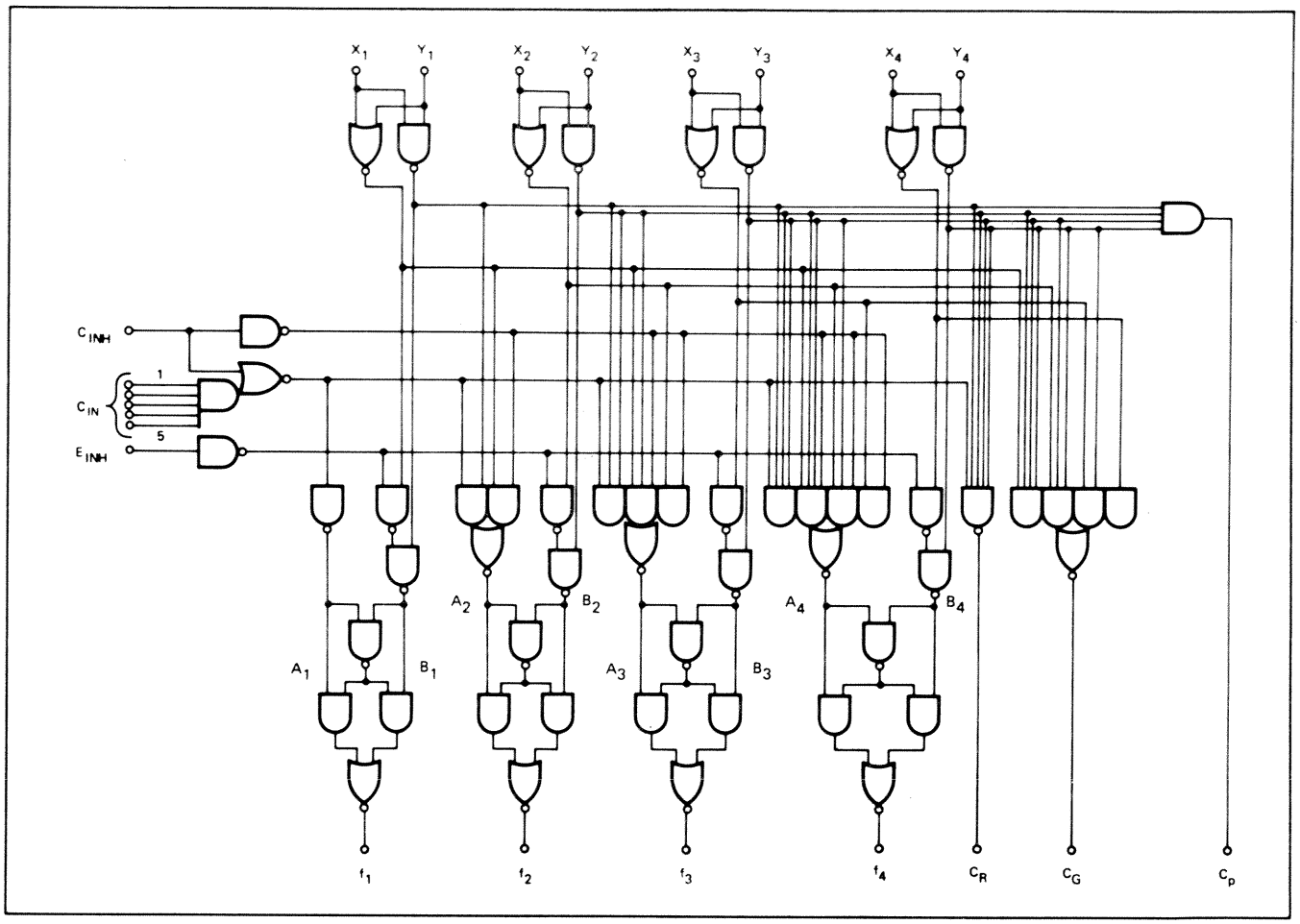
TRUTH TABLE

V_{IN}	V_{IN}	V_{OUT}
L	L	H
L	H	H
H	L	H
H	H	L

8260

Arithmetic Logic Element

LOGIC DIAGRAM



A and B refer to functional block diagram

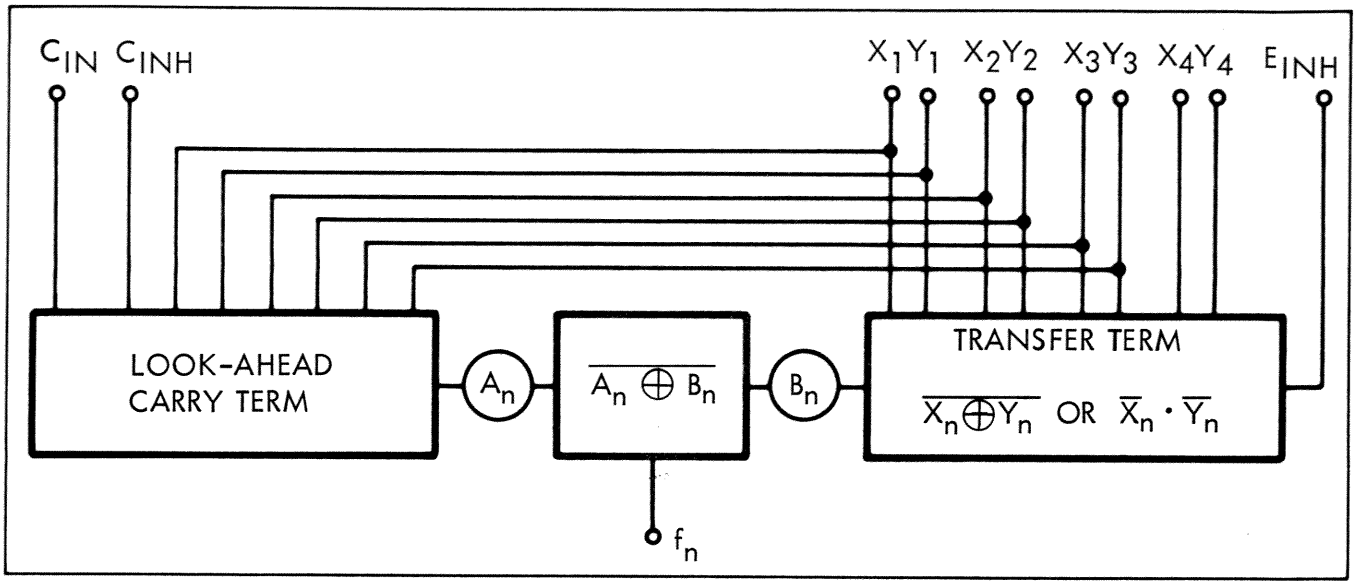
C_G = Internally Generated Carry

C_R = Ripple Carry

C_P = Propogated Carry

8260(cont.)

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLES

$C_{INH} = 1 \rightarrow A_n = 1$

$C_{INH} = 0 \rightarrow A_n =$

C_{IN}	A_1	A_1	X_1	Y_1	A_2	A_2	X_2	Y_2	A_3	A_3	X_3	Y_3	A_4
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	1	0	0	0	1	0
		0	1	0	0	0	1	0	0	0	1	0	0
		0	1	1	1	0	1	1	1	0	1	1	1
		1	0	0	0	1	0	0	0	1	0	0	0
		1	0	1	1	1	0	1	1	1	0	1	1
		1	1	0	1	1	1	0	1	1	1	0	1
		1	1	1	1	1	1	1	1	1	1	1	1

A_n	B_n	f_n
0	0	1
0	1	0
1	0	0
1	1	1

E_{INH}	X_n	Y_n	B_n
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

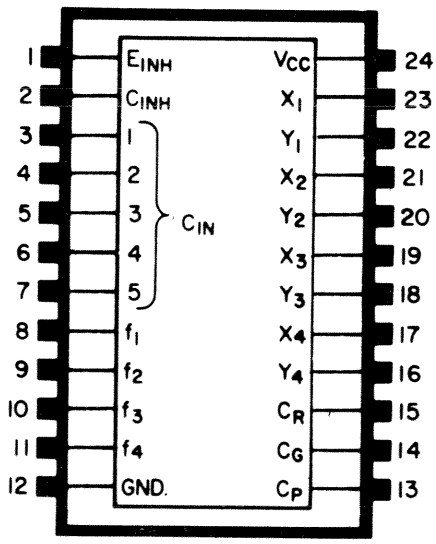
8260(cont.)

MODE OF OPERATION

INPUTS	Least Significant C_{IN} Inputs to be: *	CONTROLS		f	FUNCTION
		C_{INH}	E_{INH}		
X_n, Y_n ↓	0	0	0	Σ_n	Add
	0	0	1	- -	Not Used
	0	1	0	$X_nY_n + \overline{X}_n\overline{Y}_n$	Coincidence
	0	1	1	X_nY_n	AND
$\overline{X}_n$, $\overline{Y}_n$ ↓	1	C	0	$\overline{\Sigma}_n$	Add
	1	0	1	- -	Not Used
	1	1	0	$\overline{X}_n\overline{Y}_n + X_nY_n$	Coincidence
	1	1	1	$\overline{X}_n\overline{Y}_n$	AND

* Least significant of a "Multiple Package" adder system.

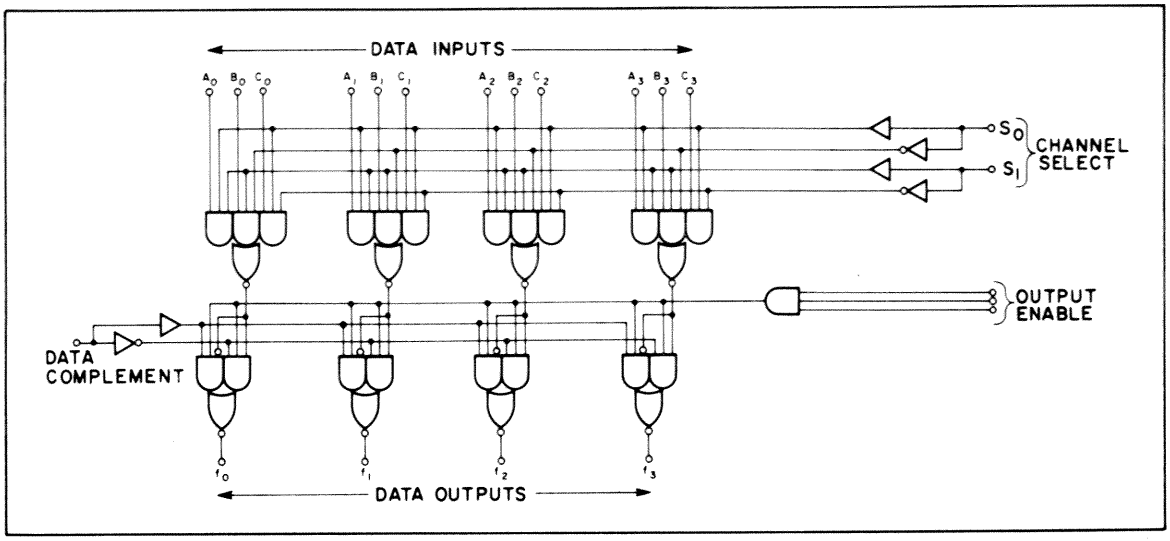
P PACKAGE



8264

3 - Input, 4-Bit Digital Multiplier

LOGIC DIAGRAM

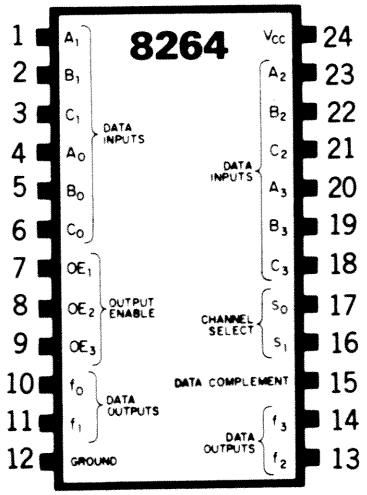


TRUTH TABLE

DATA INPUT A_n	DATA INPUT B_n	DATA INPUT C_n	CHANNEL SELECT S_0	CHANNEL SELECT S_1	DATA COMPLEMENT	OUTPUT ENABLE (8264)	DATA OUTPUTS
A_n	x	x	1	1	0	1	A_n
x	B_n	x	0	1	0	1	B_n
x	x	C_n	1	0	0	1	C_n
x	x	x	0	0	0	1	0
A_n	x	x	1	1	1	1	$\overline{A_n}$
x	B_n	x	0	1	1	1	$\overline{B_n}$
x	x	C_n	1	0	1	1	$\overline{C_n}$
x	x	x	0	**0**	1	1	1
x	x	x	x	x	x	0	1

x = Either State

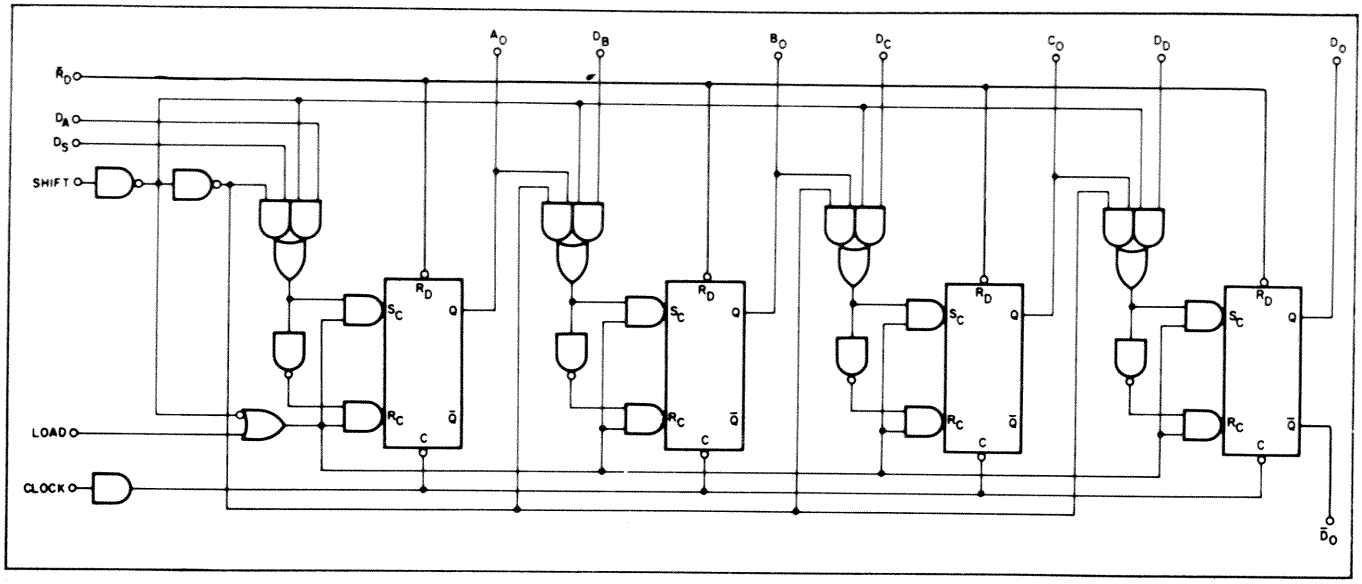
P, Y PACKAGE



8271

4 - Bit Shift Registers

LOGIC DIAGRAM

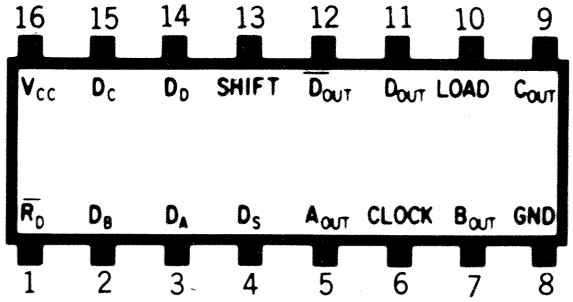


TRUTH TABLE

CONTROL STATE	LOAD	SHIFT
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1

B PACKAGE

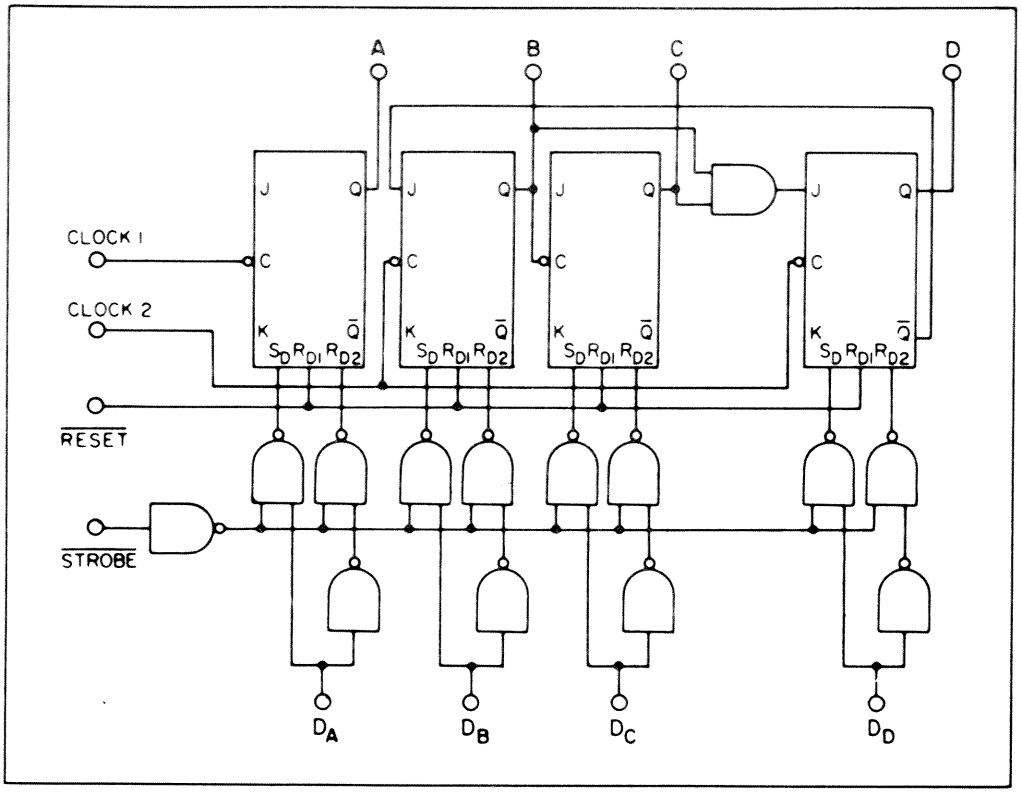
8271B



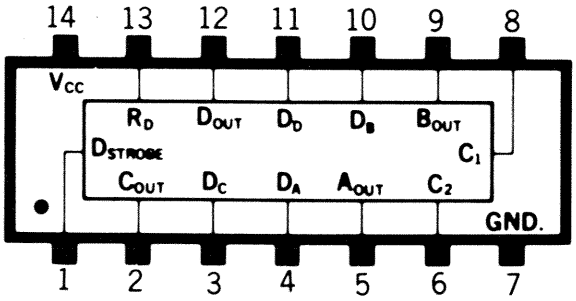
8280

BCD Decade Counter/Storage Element

LOGIC DIAGRAM



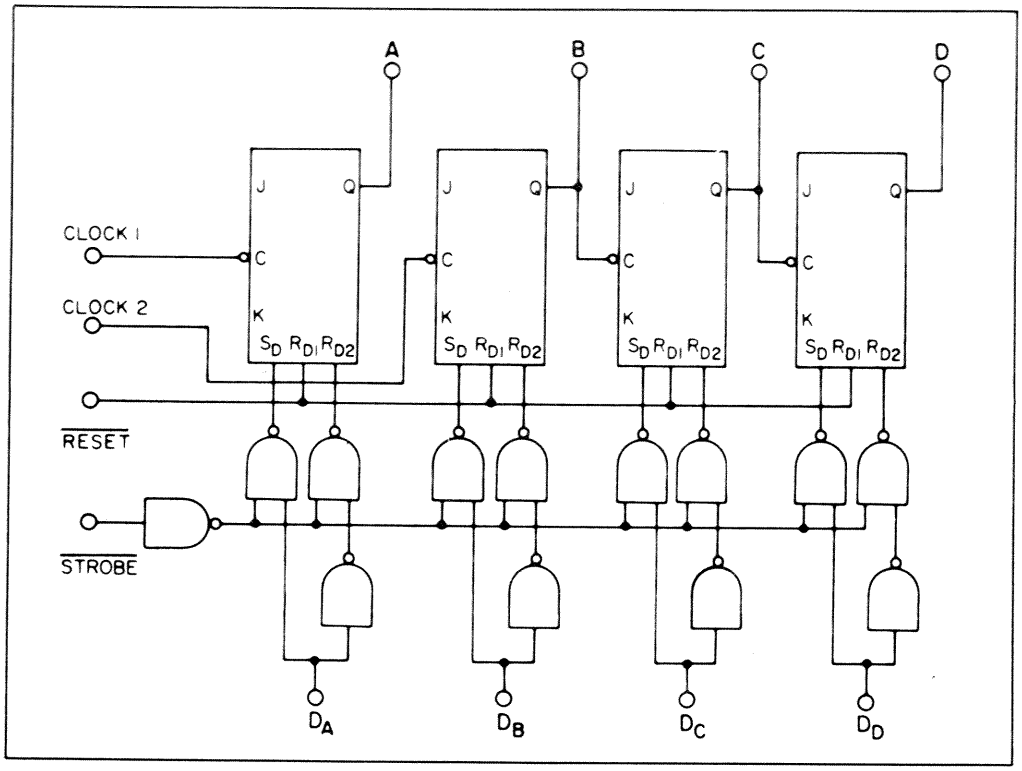
8280 has strobed parallel-entry for setting to any output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs. The counting operation is performed on the falling (negative-going) edge of the input clock pulse.



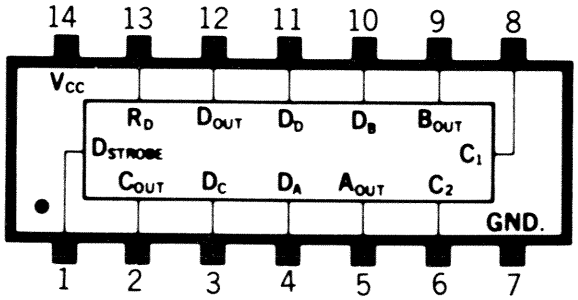
8281

4-Bit Binary Counter/Storage Element

LOGIC DIAGRAM



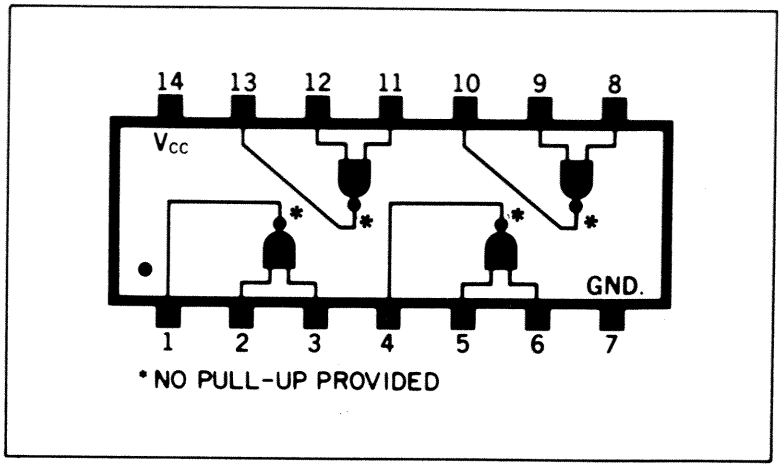
8281 has strobed parallel-entry for setting to any output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs. The counting operation is performed on the falling (negative-going) edge of the input clock pulse.



8881

Quad 2 - Input NAND Gate

LOGIC DIAGRAM



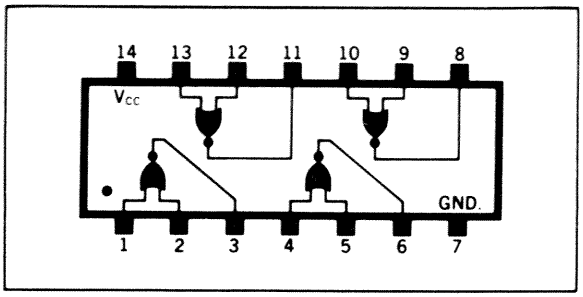
TRUTH TABLE

V_{IN}	V_{IN}	V_{OUT}
L	L	H
L	H	H
H	L	H
H	H	L

8885

Quad 2 - Input NOR Gate

LOGIC DIAGRAM



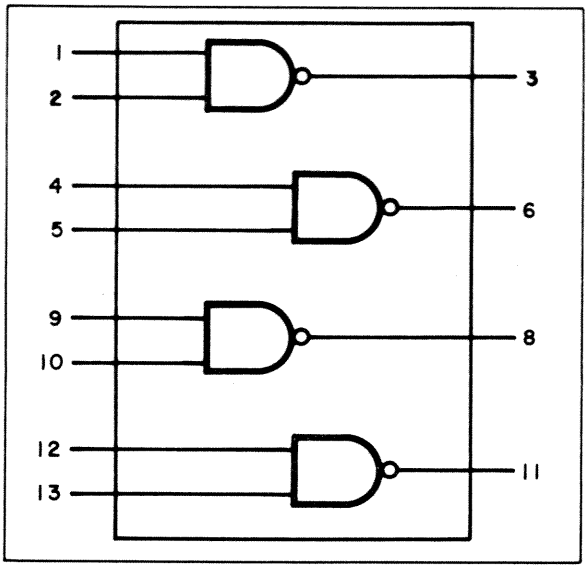
TRUTH TABLE

V_{IN}	V_{IN}	V_{OUT}
H	H	L
H	L	L
L	H	L
L	L	H

9002

Quad 2 - Input NAND Gates

LOGIC DIAGRAM



V_{CC} = Pin 14

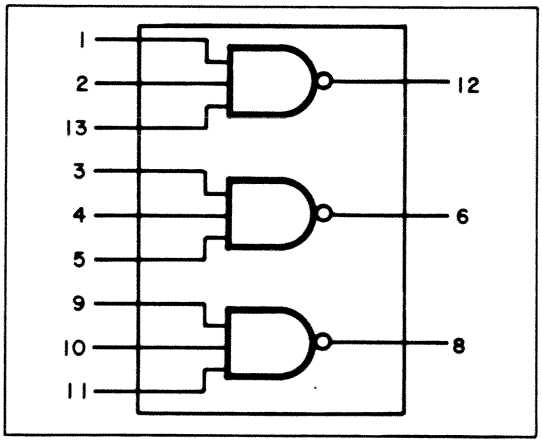
Gnd = Pin 7

TRUTH TABLE LISTED BELOW

9003

Triple 3 - Input NAND Gates

LOGIC DIAGRAM



V_{CC} = Pin 14

Gnd = Pin 7

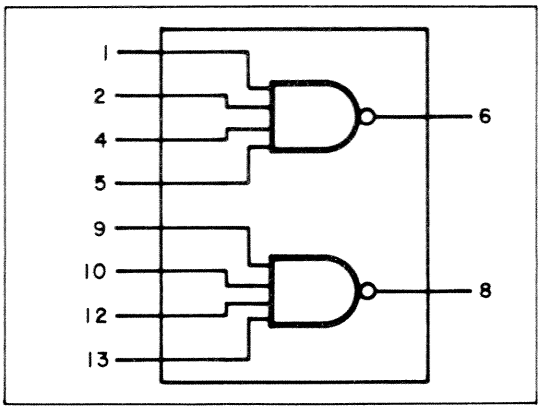
9002 & 9003 TRUTH TABLE

ALL INPUTS HIGH = LOW OUT
ALL INPUT LOW = HIGH OUT

9004/9009*

Dual 4 - Input NAND Gates

LOGIC DIAGRAM



V_{CC} = Pin 14

Gnd = Pin 7

*9009 Has Higher Input-Output Loading Parameters Than 9004

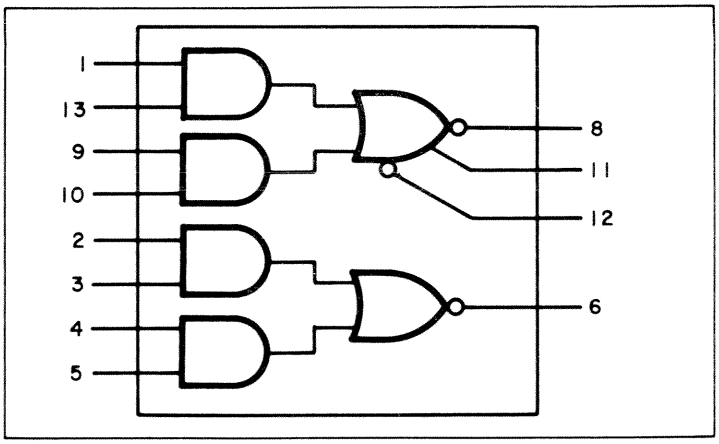
TRUTH TABLE

All Inputs High = Low Out
Any Input Low = High Out

9005

Dual Extendable AND-OR-INVERT Gates

LOGIC DIAGRAM



*Four Extenders (9006) may be tied to these terminals

V_{CC} = Pin 14

Gnd = Pin 7

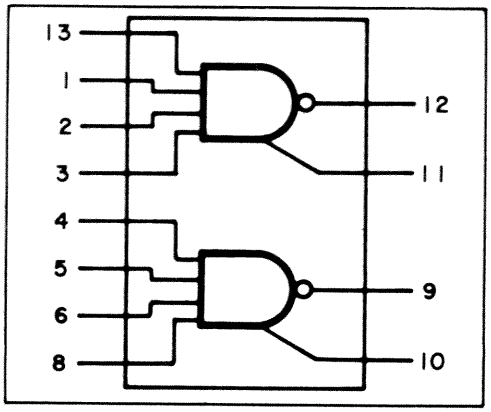
TRUTH TABLE

$(2 \cdot 3) \cdot (4 \cdot 5) = \overline{6}$
$(\overline{2} + \overline{3}) + (\overline{4} + \overline{5}) = 6$

9006

Dual Extender AND-OR-INVERT Gates

LOGIC DIAGRAM



Extender for use with 9005 & 9008

V_{CC} = Pin 14

Gnd = Pin 7

TRUTH TABLE

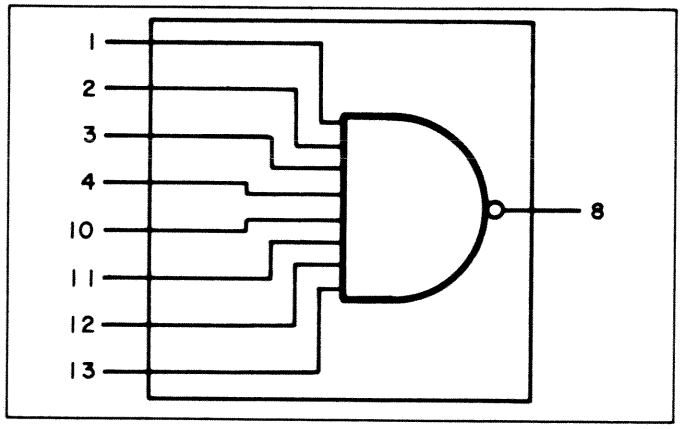
$4 \cdot 5 \cdot 6 \cdot 8 = \overline{9}$

$\overline{4}+\overline{5}+\overline{6}+\overline{8} = 9$

9007

8 - Input NAND Gate

LOGIC DIAGRAM



V_{CC} = Pin 14

Gnd = Pin 7

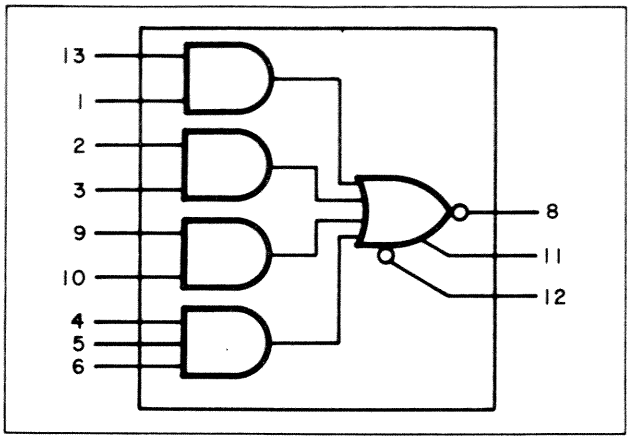
TRUTH TABLE

ALL INPUTS HIGH = LOW OUT
ANY INPUT LOW = HIGH OUT

9008

Single Extendable AND-OR-INVERT Gate

LOGIC DIAGRAM



*Four Extenders (9006) may be tied to these terminals

V_{CC} = Pin 14
Gnd = Pin 7

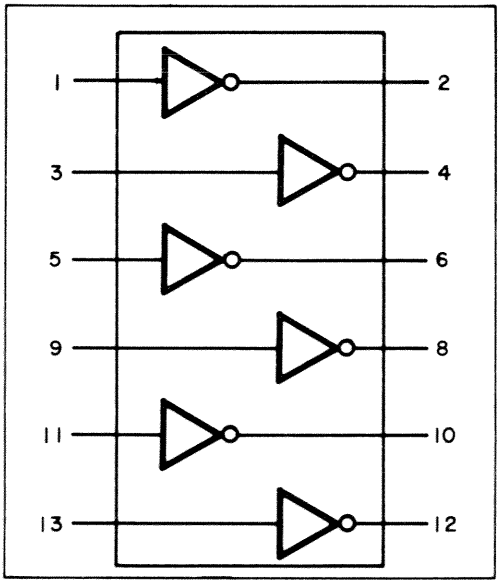
TRUTH TABLE

$(1 \cdot 13) \cdot (2 \cdot 3) \cdot (9 \cdot 10) \cdot (4 \cdot 5 \cdot 6) = \overline{8}$
$(1 + 13) + (2 + 3) + (9 + 10) + (4 + 5 + 6) = 8$

9016

Quad Hex Inverter

LOGIC DIAGRAM



V_{CC} = Pin 14
Gnd = Pin 7

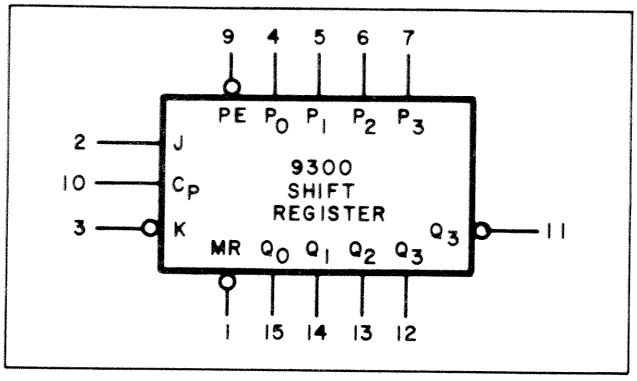
TRUTH TABLE

ANY INPUT LOW = HIGH PUT
ANY INPUT HIGH = LOW OUT

9300

4 - Bit Shift Register

LOGIC DIAGRAM



V_{CC} = Pin 14
Gnd = Pin 8

PIN NOMENCLATURE

$\overline{PE}$	Parallel Enable (Active Low) Input
P_0, P_1, P_2, P_3	Parallel Inputs
J	First Stage J (Active High) Input
$\overline{K}$	First Stage K (Active Low) Input
Cp	Clock Active High Going Edge Input
$\overline{MR}$	Master Reset (Active High) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
$\overline{Q_3}$	Complementary Last Stage Output

Data entry is synchronous with the registers changing state after each low to high transition of the clock. With the parallel enable low the parallel inputs determine the next condition of the shift register. When the parallel enable input is high the shift register performs a one bit shift to the right, with data entering the first stage flip-flop through $J\overline{K}$ inputs. By tying the two inputs together D type entry is obtained.

The asynchronous active low master reset when activated overrides all other input conditions and clears the register.

TRUTH TABLE FOR SERIAL ENTRY

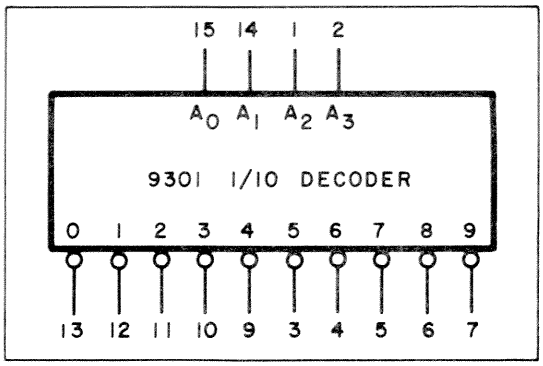
J	$\overline{K}$	Q_o at t_{n+1}
L	L	L
L	H	Q_o at t_n (no change)
H	L	$\overline{Q}_o$ at t_n (toggles)
H	H	H

$\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH (n + 1) indicates state after next clock

9301

One of Ten Decoder

LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

PIN NOMENCLATURE

A_0, A_1, A_2, A_3	Address Inputs
$\overline{0}$ to $\overline{9}$	Outputs (Active Low)

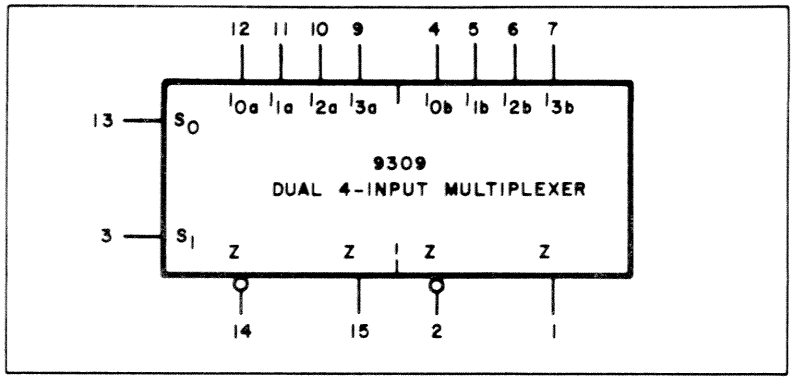
The 9301 accepts four binary weighted inputs and provides one of ten mutually exclusive active low outputs

TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Voltage Level
L = Low Voltage Level

9309
Dual 4-Input Multiplexer



V_{CC} = Pin 16
Gnd = Pin 8

PIN NOMENCLATURE

S_0, S_1	Common select Inputs
Multiplexer A	
I_{0a}, I_{1a}, I_{2a}, I_{3a}	Multiplexer Inputs
Z_a	Multiplexer Output
$\overline{Z_a}$	Complementary Multiplexer Output
Multiplexer B	
I_{0b}, I_{1b}, I_{2b}, I_{3b}	Multiplexer Inputs
Z_b	Multiplexer Output
$\overline{Z_b}$	Complementary Multiplexer Output

The 9309 consists of two 4 input multiplexers with common input select logic. It allows two bits of data to be switched in parallel to the appropriate outputs from two 4 bit data sources. Both polarities of outputs are available.

TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	$\overline{Z}_a$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

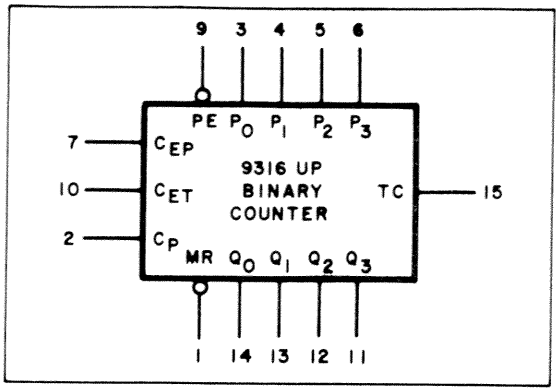
LOGIC EQUATION

$$Z_a = I_{0a} \cdot \overline{S}_0 \cdot \overline{S}_1 + I_{1a} \cdot S_0 \cdot \overline{S}_1 + I_{2a} \cdot \overline{S}_0 \cdot S_1 + I_{3a} \cdot S_0 \cdot S_1$$

$$Z_b = I_{0b} \cdot \overline{S}_0 \cdot \overline{S}_1 + I_{1a} \cdot S_0 \cdot \overline{S}_1 + I_{2a} \cdot \overline{S}_0 \cdot S_1 + I_{3a} \cdot S_0 \cdot S_1$$

9316
Binary Up Counter

LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

PIN NOMENCLATURE

$\overline{PE}$	Parallel Enable (Active Low) Input
P_0, P_1, P_2, P_3	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
Cp	Clock Active High Going Edge Input
$\overline{MR}$	Master Reset (Active Low) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
TC	Terminal Count Output

The counter is synchronous with the counter outputs changing state after the low to high transition of the clock. When conditions are satisfied for counting, a clock pulse will change the counter to the next state of a binary sequence. When the parallel enable is low the parallel inputs determine the next state of the counter synchronously with the clock.

Mode selection is accomplished as shown below. However a restriction is placed on the manner of selection. The transition of CEP or CET from high to low or of $\overline{PE}$ from low to high may only be done when CP is high.

By utilizing the two count enable inputs and terminal count output, multi-stage synchronous counting is obtained, with operating speeds equivalent to that of a single stage.

When the asynchronous master reset is active outputs Q_{0-3} will be forced low regardless of all other input conditions.

MODE SELECTION

$\overline{PE}$	CE (Count Enable)	MODE
H	H	Count Up
H	L	No Change
L	X	Presetting

Where CE (Count Enable) = CEP • CET

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

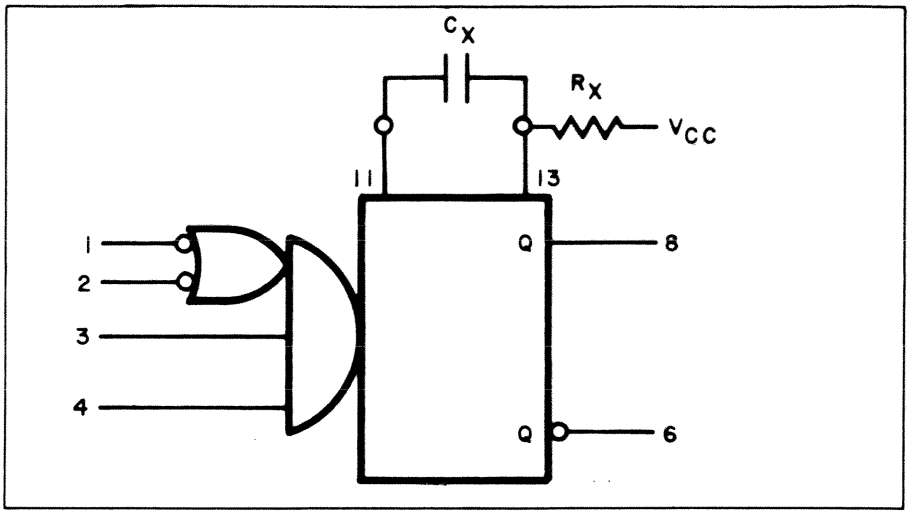
LOGIC EQUATION FOR TERMINAL COUNT

$$TC = CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$$

9601

Monostable Multivibrator (One Shot)

LOGIC DIAGRAM



V_{CC} = Pin 14

Gnd = Pin 7

The inputs are dc coupled hence triggering is independent of input transition times. If the input signal is applied to an active high input, triggering will occur on the rising edge of the waveform. By applying the input signal to an active low input, triggering will occur on the falling edge of the waveform.

Each time the input conditions for triggering are met, the external capacitor is discharged and a new cycle is started. Successive inputs with a period shorter than the delay time (R_XC_X) retrigger the monostable resulting in a continuous true output. Retriggering may be inhibited by tying the negation ($\overline{Q}$) output back to an active level low input.

The formula for calculating the delay time constant is:

$$0.36 \times R(\text{in ohms}) \times C(\text{in Farads}) = T(\text{in seconds})$$

APPENDIX B

SUPERNOVA SIGNAL LIST

SIGNAL ORIGIN

CENTRAL PROCESSOR

AND

MEMORY

NOTE: Blank entries in level column denote flip-flop outputs which may be in either logic state.
Accumulators, Adders, I/O DATA lines, memory INHIBIT lines MEMORY ADDRESS (MA) flip-flops, MEMORY BUFFER (MB) flip-flops, PROGRAM COUNTER (PC) flip-flops, and RINH flip-flops output levels are not defined in the level column.

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
ACØØ		E81	5	CPU3	Ø35-2
ACØ1		E81	7	"	"
ACØ2		E81	9	"	"
ACØ3		E81	11	"	"
ACØ3*		E81	12	"	"
ACØ4		E78	5	"	Ø35-3
ACØ5		E78	7	"	"
ACØ6		E78	9	"	"
ACØ7		E78	11	"	"
ACØ7*		E78	12	"	"
ACØ8		E75	5	"	Ø35-4
ACØ9		E75	7	"	"
ACØ1Ø		E75	9	"	"
ACØ11		E75	11	"	"
ACØ11*		E75	12	"	"
ACØ12		E72	5	"	Ø35-5
ACØ13		E72	7	"	"
ACØ14		E72	9	"	"
ACØ15		E72	11	"	"
ACØ15*		E72	12	"	"
AC1Ø		E1Ø1	5	"	Ø35-2
AC11		E1Ø1	7	"	"
AC12		E1Ø1	9	"	"
AC13		E1Ø1	11	"	"
AC13*		E1Ø1	12	CPU3	Ø35-2
AC14		E97	5	"	Ø35-3
AC15		E97	7	"	"
AC16		E97	9	"	"
AC17		E97	11	"	"
AC17*		E97	12	"	"
AC18		E93	5	"	Ø35-4
AC19		E93	7	"	"
AC11Ø		E93	9	"	"
AC111		E93	11	"	"
AC111*		E93	12	"	"
AC112		E89	5	"	Ø35-5
AC113		E89	7	"	"
AC114		E89	9	"	"
AC115		E89	11	"	"
AC115*		E89	12(A5)	"	"
AC20		E1ØØ	5	"	Ø35-2

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
AC21		E1ØØ	7	CPU3	Ø35-2
AC22		E1ØØ	9	"	"
AC23		E1ØØ	11	"	"
AC23*		E1ØØ	12	"	"
AC24		E96	5	"	Ø35-3
AC25		E96	7	"	"
AC26		E96	9	"	"
AC27		E96	11	"	"
AC27*		E96	12	"	"
AC28		E92	5	"	Ø35-4
AC29		E92	7	"	"
AC21Ø		E92	9	"	"
AC211		E92	11	"	"
AC211*		E92	12	"	"
AC212		E88	5	"	Ø35-5
AC213		E88	7	"	"
AC214		E88	9	"	"
AC215		E88	11	"	"
AC215*		E88	12	"	"
AC3Ø		E8Ø	5	"	Ø35-2
AC31		E8Ø	7	"	"
AC32		E8Ø	9	"	"
AC33		E8Ø	11	"	"
AC33*		E8Ø	12	"	"
AC34		E77	5	"	Ø35-3
AC35		E77	7	"	"
AC36		E77	9	"	"
AC37		E77	11	"	"
AC37*		E77	12	"	"
AC38		E74	5	"	Ø35-4
AC39		E74	7	"	"
AC31Ø		E74	9	"	"
AC311		E74	11	"	"
AC311*		E74	12	"	"
AC312		E71	5	"	Ø35-5
AC313		E71	7	"	"
AC314		E71	9	"	"
AC315		E71	11	"	"
AC315*		E71	12	"	"
ACCØ*		(S1)	-	CON	Ø6Ø-1

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
ACC1*	L	- (S2)	(A39) -	CPU2 CON	Ø47-2 Ø6Ø-2
ACC2*	L	- (S3)	(A37) -	CPU2 CON	Ø47-2 Ø6Ø-1
ACC3*	L	- (S4)	(A32) -	CPU2 CON	Ø47-2 Ø6Ø-1
ACCØ + 1	L	-	(A41)	CPU2	Ø47-2
ACCØ + 2	H	E2Ø	3	"	"
ACC ENABLE*	H	E2Ø	6	"	"
ACDØ*	L	E1ØØ	6(B24)	CPU1	Ø33-3
ACD1*	L	E47	5	CPU2	Ø47-1
ACD2*	L	E47	3	"	"
ACD3*	L	E47	1Ø	"	"
ACDØ + ACCØ	H	E47	12	"	"
ACD1 + ACC1	H	E55	6(A49)	"	Ø47-2
ACD2 + ACC2	H	E2Ø	11(A59)	"	"
ACD LEFT ENAB A (D-L-E-A)	L	E83	8(A62)	"	"
ACD LEFT ENAB B (D-L-E-B)	H	E46	11	CPU3	Ø35-1
ACD OUT*	L	E35	6	"	"
ACDP	H	E58	8(A19)	CPU2	Ø47-2
ACDP*	L	-	8	"	"
ACD RIGHT ENAB (D-R-E)	H	E46	(B95)	CPU1	Ø33-3
ACD RIGHT HI SEL LSB (D-R-H-S-L)	H	E44	3	CPU3	Ø35-2
ACD RIGHT HI SEL MSB (D-R-H-S-M)	H	E45	8	"	"
ACD RIGHT LOW SEL (D-R-L-S)	H	E45	6	"	"
AC3 ENAB*	L	E56	8	"	"
ACEX*	L	-	6(A42)	CPU2	Ø47-2
ACEX + ACDP	H	E68	(B94)	CPU1	Ø33-3
AC LOAD ENABLE	H	E55	6	"	"
AC3 OUT*	L	E7Ø	8(A61)	CPU2	Ø47-2
ACS COMP ENAB*	L	E4	8(A63)	"	"
ACSX COMP (SX-COM)	H	E48	8(A57)	"	"
ACSX LEFT ENAB A (SX-L-E-A)	H	E46	6	CPU3	Ø35-1
			8	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
ACSX LEFT ENAB B (SX-L-E-B)	H	E44	6	CPU3	Ø35-1
ACSX LEFT LOW SEL (SX-L-L-S)	L	E3	8(A31)	CPU2	Ø47-2
ACSX LEFT HI SEL (SX-L-H-S)	L	E2	8(A3Ø)	"	"
ACSX RIGHT ENAB (SX-R-E)	H	E47	8	CPU3	Ø35-1
ACSX RIGHT HI SEL LSB (SX-R-H-S-L)	H	E49	6	"	"
ACSX RIGHT HI SEL MSB (SX-R-H-S-M)	H	E48	8	"	"
ACSX RIGHT LOW SEL (SX-R-L-S)	H	E49	8	"	"
ADDERØ		E79	11	"	Ø35-2
ADDER1		E79	1Ø	"	"
ADDER2		E79	9	"	"
ADDER3		E79	8	"	"
ADDER4		E76	11	"	Ø35-3
ADDER5		E76	1Ø	"	"
ADDER6		E76	9	"	"
ADDER7		E76	8	"	"
ADDER8		E73	11	"	Ø35-4
ADDER9		E73	1Ø	"	"
ADDER1Ø		E73	9	"	"
ADDER11		E73	8	"	"
ADDER12		E7Ø	11	"	Ø35-5
ADDER13		E7Ø	1Ø	"	"
ADDER14		E7Ø	9	"	"
ADDER15		E7Ø	8	"	"
ADDER=Ø		F2Ø	3,6,8,11	"	Ø35-2
ADDER=Ø		E15	3,6,8,11	"	Ø35-3
ADDER=Ø		E1Ø	3,6,8,11	"	Ø35-4
ADDER=Ø		E5	3,6,8,11 (B96)	"	Ø35-5 "
ADDER OUT	H	E16	8(B83)	CPU2	Ø47-2
ADDER=ØSAVE		E6Ø	9	"	"
ADDER=Ø SAVE*		E6Ø	8	"	"
ADD ONE	H	E1	12(A91)	"	"
ALC		E32	9	"	Ø47-1
ALC*		E32	8	"	"
ALC + KEY2 .ACEX*	L	E21	6(A66)	"	Ø47-2
ALC SKIP		E22	5	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
ALC SKIP*		E22	6(B54)	CPU2	Ø47-2
ALC SKIP ENAB*	L	E85	6(A7)	CPU3	Ø35-1
AND	H	E49	8(B51)	CPU2	Ø47-2
AUTO-DEC	H	E59	6	"	"
AUTO-INC	H	E59	3	"	"
C2		E35	5	CPU1	Ø33-1
C2*		E35	6	"	"
C3		E35	9	"	"
C3*		E35	8	"	"
C4		E34	5(B22)	"	"
C4*		E34	6	"	"
CARRY		E22	9(B87)	CPU2	Ø47-2
CARRY*		E22	8	"	"
CARRY SET		E68	8(A17)	CPU3	Ø35-1
CG		E79	14	"	Ø35-2
4CG		E76	14	CPU3	Ø35-3
8CG		E73	14	"	Ø35-4
12CG		E7Ø	14	"	Ø35-5
CHST	H	E84	12(A57)	CPU1	Ø33-3
CHST*	L	(S1Ø) - (B6Ø)	-	CON	Ø6Ø-1
				CPU1	Ø33-3
CLR	H	E25	6(A5Ø)	"	Ø33-2
CODE 77	H	E24	8(A82)	CPU2	Ø47-1
CODE77*	L	E25	8	"	"
COMP RIGHT LSB & LEFT (D-RL-L-COM)	H	E43	8	CPU3	Ø35-1
COMP RIGHT MSB (D-RM-COM)	H	E45	12	"	"
CONØ*	L	(S11) - (B69)	-	CON	Ø6Ø-1
				CPU3	Ø35-2
CON1*	L	(S12) - (B72)	-	CON	Ø6Ø-1
				CPU3	Ø35-2
CON2*	L	(S13) - (B67)	-	CON	Ø6Ø-1
				CPU3	Ø35-2
CON3*	L	(S14) - (B53)	-	CON	Ø6Ø-1
				CPU3	Ø35-2
CON4*	L	(S15) - (B21)	-	CON	Ø6Ø-1
				CPU3	Ø35-3
CON5*	L	(S16) - (B23)	-	CON	Ø6Ø-1
				CPU3	Ø35-3
CON6*	L	(S17)	-	CON	Ø6Ø-1

* INDICATES "NOT"

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
		-	(B19)	CPU3	Ø35-3
CON7*	L	(S18)	-	CON	Ø6Ø-1
		-	(B17)	CPU3	Ø35-3
CON8*	L	(S19)	-	CON	Ø6Ø-1
		-	(A93)	CPU3	Ø35-4
CON9*		(S2Ø)	-	CON	Ø6Ø-1
		-	(A94)	CPU3	Ø35-4
CON1Ø*		(S21)	-	CON	Ø6Ø-1
		-	(A92)	CPU3	Ø35-4
CON11*		(S22)	-	CON	Ø6Ø-1
		-	(A91)	CPU3	Ø35-4
CON12*		(S23)	-	CON	Ø6Ø-1
		-	(A75)	CPU3	Ø35-5
CON13*		(S24)	-	CON	Ø6Ø-1
		-	(A77)	CPU3	Ø35-5
CON14*		(S25)	-	CON	Ø6Ø-1
		-	(A73)	CPU3	Ø35-5
CON15*		(S26)	-	CON	Ø6Ø-1
		-	(A71)	CPU3	Ø35-5
CON OUT*	L	E19	8(A25)	CPU2	Ø47-2
CONT*	L	(S6)	-	CON	Ø6Ø-1
		-	(B58)	CPU1	Ø33-3
CONT + ISTP + MSTP	H	E83	8(B47)	"	"
CONT + ISTP + MSTP*	L	E84	4	"	"
CPU CLK		E7	6, 8(A48)	CPU1	Ø33-1
CPU CLK		E6	6, 8(B83)	"	"
CR		E79	15	CPU3	Ø35-2
4CR		E76	15	"	Ø35-3
8CR		E73	15	"	Ø35-4
12CR		E7Ø	15	"	Ø35-5
CRY OUT*	L	E48	12(A22)	"	Ø35-1
CRY SAVE		E6Ø	5(A95)	CPU2	Ø47-2
CRY SAVE*		E6Ø	6	"	"
DATAØ*		(Q1)	(B62)	CPU3	Ø35-2
DATA1*		(Q2)	(B65)	"	"
DATA2*		(Q3)	(B82)	"	"
DATA3*		(Q4)	(B73)	"	"
DATA4*		(Q5)	(B61)	"	Ø35-3
DATA5*		(Q6)	(B57)	"	"
DATA6*		(Q7)	(B95)	"	"
DATA7*		(Q8)	(B55)	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
DATA8*		(Q9)	(B6Ø)	CPU3	Ø35-4
DATA9*		(Q1Ø)	(B63)	"	"
DATA1Ø*		(Q11)	(B75)	"	"
DATA11*		(Q12)	(B58)	"	"
DATA12*		(Q13)	(B59)	"	Ø35-5
DATA13*		(Q14)	(B64)	"	"
DATA14*		(Q15)	(B56)	"	"
DATA15*		(Q16)	(B66)	"	"
DATIA	H	E24	8(A44)	CPU1	Ø33-2
DATIB	H	E24	6(A42)	"	"
DATIC	H	E8	6(A54)	"	"
DATOA	H	E26	6(A58)	"	"
DATOB	H	E8	8(A56)	"	"
DATOC	H	E23	8(A41)	"	"
DCH	H	E65	8	CPU2	Ø47-1
DCH1	H	E67	7(B56)	"	"
DCH1*	L	E48	12	"	"
DCH2	H	E51	9(A64)	"	"
DCHA*	L	E9	8(A6Ø)	CPU1	Ø33-2
DCHI	H	E31	6(B37)	"	"
DCH IN*	L	E43	8(A87)	"	"
DCH INC	H	E44	8(A53)	"	"
DCH IND*	L	E34	6(B63)	CPU2	Ø47-1
DCH + INT PEND	H	E84	3	"	"
DCH1 IO*	L	E78	12	CPU1	Ø33-2
DCH2 (IO)*	L	E78	1Ø	"	"
DCHO	H	E3Ø	8(B33)	"	"
DCHO*	L	E42	8	"	"
DCH OUT*	L	E74	11	"	"
DCH PEND*	L	E92	12(B85)	"	"
DEFER	H	E51	7(B6Ø)	CPU2	Ø47-1
DEFER*	L	E48	2	"	"
DEFER IND*	L	E34	8(B92)	"	"
DEFER MEM MOD*	L	E43	6(A86)	"	Ø47-2
DEFER SET	H	E66	6	"	Ø47-2
DP*	L	(S7)	-	CON	Ø6Ø-1
		-	(B59)	CPU1	Ø33-3
DP + DPN	H	E85	8(A76)	"	"
DPN*	L	(S7)	-	CON	Ø6Ø-1
		-	(B7Ø)	CPU1	Ø33-3
DPN + EXN	H	E68	11(A83)	"	"
DSØ*	H	E28	8(A72)	"	Ø33-2
DS1*	H	E28	6(A68)	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
DS2*	H	E27	8(A66)	CPU1	Ø33-2
DS3*	H	E27	6(A46)	"	"
DS4*	H	E29	6(A62)	"	"
DS5*	H	E29	8(A64)	"	"
DSZ	H	E46	6	CPU2	Ø47-1
DSZ*	L	E47	13	"	"
EFA		E32	5	"	"
EFA*		E32	6(A21)	"	"
EIS	H	E49	6	"	"
ENAB ACD RIGHT MSB COMP*	L	E36	8(A43)	"	Ø47-2
ENAB CARRY*	L	E82	8(A13)	CPU3	Ø35-1
ENAB RIGHT LSB + LEFT COMP	L	E37	8(A27)	CPU2	Ø47-2
EX*	L	(S8)	-	CON	Ø6Ø-1
		-	(B64)	CPU1	Ø33-3
EXEC	H	E51	11	CPU2	Ø47-1
EXEC*	L	E51	12(B69)	"	"
EXEC B	H	E68	8	"	"
EXEC SET	H	E84	8	"	"
EXEC · DIV · TSØ*	L	E8Ø	6(A38)	"	Ø47-2
EX + EXN + DP + DPN	H	E83	6(A69)	CPU1	Ø33-3
EXN*	L	(S3)	-	CON	Ø6Ø-1
		-	(B68)	CPU1	Ø33-3
EX + STRT	H	E68	3(A55)	"	"
F COM	H	E78	12	CPU2	Ø47-1
F COM*	L	E79	6	"	"
FETCH	H	E68	6(B79)	"	"
FETCH*	L	E67	12	"	"
FETCH IND*	L	E65	1Ø(B59)	"	"
FETCH + IN2	H	E8Ø	8	"	"
FETCH SET	H	E83	3	"	"
F SET	H	E83	6(B67)	"	"
HALT*	L	E4Ø	6	CPU1	Ø33-2
HSC BUSY	H	E45	2	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
INC PC		E52	9(A92)	CPU2	Ø47-2
INC PC*		E52	8	"	"
INDØ*	L	E4Ø	8(B87)	CPU3	Ø35-2
IND1*	L	E4Ø	6(B85)	"	"
IND2*	L	E39	8(B78)	"	"
IND3*	L	E39	6(B86)	"	"
IND4*	L	E35	8(B37)	"	Ø35-3
IND5*	L	E35	6(B35)	"	"
IND6*	L	E34	8(B31)	"	"
IND7*	L	E34	6(B3Ø)	"	"
IND8*	L	E3Ø	8(B7)	"	"
IND9*	L	E3Ø	6(B6)	"	"
IND1Ø*	L	E29	8(A96)	"	"
IND11*	L	E29	6(A95)	"	"
IND12*	L	E26	8(A85)	"	Ø35-5
IND13*	L	E26	6(A83)	"	"
IND14*	L	E25	8(A81)	"	"
IND15*	L	E25	6(A79)	"	"
Ø1 IND DRIVE	H	E98	8(B13)	CPU1	Ø33-3
Ø2 IND DRIVE	H	E98	6(B11)	"	"
INHØ		E23	9	MEM	Ø29-2
INH1		"	5	"	"
INH2'		E21	9	"	"
INH3		"	5	"	"
INH4		E17	9	"	"
INH5		"	5	"	"
INH6		E15	9	"	"
INH7		"	5	"	"
INH8		E11	9	"	"
INH9		"	5	"	"
INH1Ø		E9	9	"	"
INH11		"	5	"	"
INH12		E5	9	"	"
INH13		"	5	"	"
INH14		E3	9	"	"
INH15		"	5	"	"
INHBØ		(Q9)	-	"	Ø29-3
INHB1		(Q1Ø)	-	"	"
INHB2		(Q11)	-	"	"
INHB3		(Q12)	-	"	"
INHB4		(Q13)	-	"	"
INHB5		(Q14)	-	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
INHB6		(Q15)	-	"	"
INHB7		(Q16)	-	"	"
INHB8		(Q17)	-	MEM	Ø29-3
INHB9		(Q18)	-	"	"
INHB1Ø		(Q19)	-	"	"
INHB11		(Q2Ø)	-	"	"
INHB12		(Q21)	-	"	"
INHB13		(Q22)	-	"	"
INHB14		(Q23)	-	"	"
INHB15		(Q24)	-	"	"
INH GATE A*	L	E36	6	"	Ø29-2
INH GATE B*	L	E36	6	"	"
INHIB		E14	9(B3Ø)	CPU1	Ø33-1
INHIB*		E14	8	"	"
INST	H	E66	8	CPU2	Ø47-1
INST. DEFER SET. . ALC SKIP	H	E64	6	"	"
INTA	H	E23	6(A4Ø)	CPU1	Ø33-2
INTA*	L	E21	4	"	"
INT PEND*	L	E72	6(B81)	"	"
IO	H	E78	2	"	"
IO*	L	E43	8(B6)	CPU2	Ø47-1
IOØ*		E63	2	CPU3	Ø35-2
IO1*		E63	5	"	"
IO2*		E63	22	"	"
IO3*		E63	19	"	"
IO4*		E59	2	"	Ø35-3
IO5*		E59	5	CPU3	Ø35-3
IO6*		E59	22	"	"
IO7*		E59	19	"	"
IO8*		E55	2	"	Ø35-4
IO9*		E55	5	"	"
IO1Ø*		E55	22	"	"
IO11*		E55	19	"	"
IO12*		E51	2	"	Ø35-5
IO13*		E51	5	"	"
IO14*		E51	22	"	"
IO15*		E51	19	"	"
IO BUSY		E76	9	CPU1	Ø33-2
IO BUSY*		E76	8	"	"
IO IN*	L	E88	3	"	"
ION	H	E41	6(B55)	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
ION*	L	E4Ø	8	CPU1	Ø33-2
ION SYNC	H	E89	12(A8)	"	"
IO OUT ENAB*	L	E55	6(A94)	"	"
IO OUT*	L	E55	8(B9Ø)	"	"
IO PLS	H	E3Ø	6(A74)	"	"
IO PRI*	L	E88	8	"	"
IO RLS		E71	5	"	"
IO RLS*		E71	6	"	"
IO RLS SET	H	E75	8(A3Ø)	"	"
IO RST	H	E26	8(A7Ø)	CPU1	Ø33-2
IO SKIP	H	E44	6(A88)	"	"
IOTGØ*	L	E89	1Ø	"	"
IOTG1*	L	E6Ø	6	"	"
IOTG2*	L	E6Ø	4	"	"
IOTG3*	L	E57	12	"	"
IOTG4		E76	5	"	"
IOTG4*		E76	6	"	"
IO TIME	H	E78	8(B38)	"	"
IO UNPROTECTED*	L	E44	6(B7)	CPU2	Ø47-1
IRØ	H	E11	8	"	"
IRØ*	L	E12	7	"	"
IR1	H	E1Ø	12	"	"
IR1*	L	E1Ø	11	"	"
IR2	H	E7	12	"	"
IR2*	L	E7	11	"	"
IR3	H	E11	4	"	"
IR3*	L	E1Ø	5(B52)	"	"
IR4	H	E11	1Ø	"	"
IR4*	L	E12	5(B49)	"	"
IR5	H	E12	12	"	"
IR5*	L	E12	11(B26)	"	"
IR6	H	E11	12	"	"
IR6*	L	E12	9(B24)	"	"
IR7	H	E9	12	"	"
IR7*	L	E9	11	"	"
IR8	H	E11	2	"	"
IR8*	L	E1Ø	1(A15)	"	"
IR9	H	E11	6	"	"
IR9*	L	E1Ø	9(A1Ø)	"	"
IR1Ø	H	E8	4	"	"
IR1Ø*	L	E7	5	"	"
IR11	H	E8	2	"	"
IR11*	L	E7	7	"	"
IR12	H	E8	6	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
IR12*	L	E7	9	CPU2	Ø47-1
IR13	H	E8	12	"	"
IR13*	L	E9	5	"	"
IR14	H	E8	1Ø	"	"
IR14*	L	E9	7	"	"
IR15	H	E8	8	"	"
IR15*	L	E9	9	"	"
IR7(IO)	H	E37	12	CPU1	Ø33-2
IR INDØ*	L	E13	6(B35)	CPU2	Ø47-1
IR IND1*	L	E13	8(P43)	"	"
IR IND2*	L	E3Ø	6(B42)	"	"
IR IND3*	L	E3Ø	8(B45)	"	"
ISTP*	L	(S9)	-	CON	Ø6Ø-1
		-	(B58)	CPU1	Ø33-3
ISZ	H	E46	4	CPU2	Ø47-1
ISZ*	L	E47	11	"	"
ISZ + DSZ	H	E45	6	"	"
ISZ + DSZ + LDA	H	E44	12	"	"
ISZ + DSZ + STA	H	E44	8(B9)		
JMP	H	E46	12	CPU2	Ø47-1
JMP*	L	E47	4	"	"
JSR	H	E46	2	"	"
JSR*	L	E47	9	"	"
JSR + IR = 3	H	E45	8	"	"
KEY1	H	E81	5	CPU1	Ø33-3
KEY2	H	E51	5(B32)	CPU2	Ø47-1
KEY2*	L	E65	12	"	"
KEY2. (CONT + ISTP + MSTP)	H	E1Ø3	8	CPU1	Ø33-3
KEY2 MEM MOD	H	E85	11	"	"
KEY1 PCLD	H	E82	8(B15)	"	"
KEY SEEN		E86	5	"	"
KEY SEEN*		E86	6	"	"
KEY1 SET	H	E8Ø	2(B19)	"	"
KEY2 SET	H	E84	6	CPU2	Ø47-1
KEY2 SET*	L	E1Ø1	8(B61)	CPU1	Ø33-3
KEY START		E1Ø4	9	"	"
KEY START *		E1Ø4	8	"	"
KEY SYNC	H	E81	9	"	"
KEY SYNC*	L	E8Ø	1Ø	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
LDA	H	E48	6	CPU2	Ø47-1
LDA*	L	E29	12	"	"
LOAD ACØ	H	E21	8	CPU3	Ø35-1
LOAD AC1	H	E21	6	"	"
LOAD AC2	H	E22	3	"	"
LOAD AC3	H	E22	11	"	"
LOAD CARRY*	L	E56	8	CPU2	Ø47-2
LOAD MA	H	E17	8(B91)	"	"
LOAD PC*	L	E62	8(B15)	"	"
Ø2 LOGICAL		E1	8(B12)	CON	Ø6Ø-1
MA1 (Ø)		E25	14	MEM	Ø29-2
MA1 (1)		E25	15	"	"
MA2 (Ø)		E25	11	"	"
MA2 (1)		E25	1Ø	"	"
MA3 (Ø)		E25	8	"	"
MA3 (1)		E25	9	"	"
MA4 (Ø)		E19	1	"	"
MA4 (1)		E19	16	"	"
MA5 (Ø)		E19	14	"	"
MA5 (1)		E19	15	"	"
MA6 (Ø)		E19	11	"	"
MA6 (1)		E19	1Ø	"	"
MA7 (Ø)		E19	8	"	"
MA7 (1)		E19	9	"	"
MA8 (Ø)		E13	1	"	"
MA8 (1)		E13	16	"	"
MA9 (Ø)		E13	14	"	"
MA9 (1)		E13	15	"	"
MA1Ø (Ø)		E13	11	"	"
MA1Ø (1)		E13	1Ø	"	"
MA11 (Ø)		E13	8	"	"
MA11 (1)		E13	9	"	"
MA12 (Ø)		E7	1	"	"
MA12 (1)		E7	16	"	"
MA13 (Ø)		E7	14	"	"
MA13 (1)		E7	15	"	"
MA14 (Ø)		E7	11	"	"
MA14 (1)		E7	1Ø	"	"
MA15 (Ø)		E7	8	"	"
MA15 (1)		E7	9	"	"
MAØ		E41	11	CPU3	Ø35-2
MAØ*		E41	12	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
MA1		E41	9	CPU3	Ø35-2
MA2		E41	7	"	"
MA3		E41	5	"	"
MA4		E36	11	"	Ø35-3
MA4*		E36	12	"	"
MA5		E36	9	"	"
MA6		E36	7	"	"
MA7		E36	5	"	"
MA8		E31	11	"	Ø35-4
MA8*		E31	12	"	"
MA9		E31	9	"	"
MA1Ø		E31	7	"	"
MA11		E31	5(B1Ø)	"	"
MA12		E27	11(A87)	"	Ø35-5
MA12*		E27	12(A88)	"	"
MA13		E27	9	"	"
MA14		E27	7	"	"
MA15		E27	5(A46)	"	"
MA LOAD*	L	E13	8(B7)	CPU1	Ø33-1
MA LOAD EN		E7Ø	5	"	"
MA LOAD EN*		E7Ø	6	CPU1	Ø33-1
MANUAL FUNCTION	H	E1Ø5	8	"	Ø33-3
MA OUT*	L	E5	8(A65)	CPU2	Ø47-2
MA ZERO BUS		E42	3,6,11	CPU3	Ø35-2
MA ZERO BUS		E37	3,6,8,11	"	Ø 35-3
MA ZERO BUS		E32	3,6,11	"	Ø35-4
		-	(B89)	"	Ø35-4
MBOØ*		E18	3(B79)	"	Ø35-2
MBO1*		E18	6(B77)	"	"
MBO2*		E18	8(B44)	"	"
MBO3*		E18	11(B43)	"	"
MBO4*		E13	3(B42)	"	Ø35-3
MBO5*		E13	6(B32)	"	"
MBO6*		E13	8(B16)	"	"
MBO7*		E13	11(B14)	"	"
MBO8*		E8	3(B12)	"	Ø35-4
MBO9*		E8	6(B9)	"	"
MBO1Ø*		E8	8(B8)	"	"
MBO11*		E8	11(B5)	"	"
MBO12*		E3	3(A39)	"	Ø35-5
MBO13*		E3	6(A37)	"	"
MBO14*		E3	8(A43)	"	"
MBO15*		E3	11(A41)	"	"
MB CLEAR*	L	E18	6(B86)	CPU1	Ø33-1

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
MB LOAD	H	E69	8(B74)	CPU1	Ø33-1
MC4		E34	9	"	"
MC4*		E34	8	"	"
MEMØ	H	E48	1Ø	CPU2	Ø47-1
MEMØ*	L	E22	8(B71)	MEM	Ø29-2
MEM1*	L	E22	11(B7Ø)	"	"
MEM2*	L	E22	6(B47)	"	"
MEM3*	L	E22	3(B68)	"	"
MEM4*	L	E16	8(B28)	"	"
MEM5*	L	E16	11(B26)	"	"
MEM6*	L	E16	6(B22)	"	"
MEM7*	L	E16	3(B24)	"	"
MEM8*	L	E1Ø	8(A55)	"	"
MEM9*	L	E1Ø	11(A53)	"	"
MEM1Ø*	L	E1Ø	6(A45)	"	"
MEM11*	L	E1Ø	3(A51)	"	"
MEM12*	L	E4	8(A36)	"	"
MEM13*	L	E4	11(A35)	"	"
MEM14*	L	E4	6(B76)	"	"
MEM15*	L	E4	3(B18)	"	"
MEM CY SET	L	E63	8(B31)	CPU2	Ø47-1
MEM ENABLE*	L	E34	8	MEM	Ø29-2
MEM MOD	H	E64	8	CPU1	Ø33-1
MEM OUT*	L	E6	8(A69)	CPU2	Ø47-2
MODEØ	H	E45	4	CPU1	Ø33-2
MSKO*	H	E9	6(A38)	"	"
MSTP*		(S9)	-	CON	Ø6Ø-1
		-	(B51)	CPU1	Ø33-3
MSTP. $\overline{\text{KEY2}}$	H	E1Ø3	3	"	"
OVFLO	H	E31	8(B39)	CPU1	Ø33-2
OVLAP	H	E81	7(A89)	"	Ø33-3
OVLAP LD MA*	L	E59	8(B65)	"	Ø33-1
PAGE WAIT		E15	5	CPU1	Ø33-1
PAGE WAIT*		E15	6	"	"
PCØ		E38	11	CPU3	Ø35-2
PC1		E38	12	"	"
PC2		E38	13	"	"
PC3		E38	14	"	"
PC4		E33	11	"	Ø35-3
PC5		E33	12	"	"
PC6		E33	13	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
PC7		E33	14	CPU3	Ø35-3
PC8		E28	11	"	Ø35-4
PC9		E28	12	"	"
PC1Ø		E28	13	"	"
PC11		E28	14	"	"
PC12		E24	11	CPU3	Ø35-5
PC13		E24	12	"	"
PC14		E24	13	"	"
PC15		E24	14	"	"
PC CLK		E5	8(A47)	CPU1	Ø33-1
		-	(B93)	"	"
PC OUT	H	E16	6(B73)	CPU2	Ø47-2
PI1	H	E67	9(B72)	"	Ø47-1
PI2	H	E67	5(B44)	"	"
PI2*	L	E65	2	"	"
PI CLR*	L	E48	2	CPU1	Ø33-1
PL		E86	8(A84)	"	Ø33-3
PL*		E86	9	"	"
PLC*		(S1Ø_	-	CON	Ø6Ø-1
		-	(B26)	CPU1	Ø33-3
PL + CHST	H	E85	3	"	"
PL CYCLE*	L	E87	12(B87)	"	"
PL LEAD Ø*	L	E87	8	"	"
PL READ IO*	L	E56	8(A43)	"	Ø33-2
POT IO INST	H	E28	8	CPU2	Ø47-1
POWER SELECT		(Q25)	-	MEM	Ø29-3
PRESET*	L	E69	6(B77)	CPU1	Ø33-3
PREV CRY	L	E23	8(A24)	CPU2	Ø47-2
PRI	L	E51	8	CPU1	Ø33-1
PROT IND*	L	E31	6(B53)	CPU2	Ø47-1
PTGØ	H	E17	11(A77)	CPU1	Ø33-1
PTG2	H	E67	8(B57)	"	"
PTG3	H	E17	8(A85)	"	"
PTG4	H	E33	11)B27)	"	"
PTG5	H	E67	6(A93)	"	"
PTG5*	L	E66	8(A39)	"	"
PTG2. CLK*	L	E79	12	CPU2	Ø47-2
READ1*	L	E18	8(B88)	CPU1	Ø33-1
READ2		E19	5	"	"
READ2*		E19	6(B91)	"	"
READ 1B*	L	E1	3	MEM	Ø29-1
READ 1C*	L	E56	8	"	Ø29-5

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
READ CY		E15	9	CPU1	Ø33-1
READ CY*		E15	8	"	"
READ IN	H	E97	3	"	Ø33-2
READS	H	E37	8(A34)	"	"
RESET*	L	E8Ø	12	"	Ø33-3
RINHØ		(Q9)	(A5)	MEM	Ø29-3
RINH1		(Q1Ø)	(A7)	"	"
RINH2		(Q11)	(A9)	"	"
RINH3		(Q12)	(A11)	"	"
RINH4		(Q13)	(A13)	MEM	Ø29-3
RINH5		(Q14)	(A15)	"	"
RINH6		(Q15)	(A18)	"	"
RINH7		(Q16)	(A17)	"	"
RINH8		(Q17)	(A19)	"	"
RINH9		(Q18)	(A24)	"	"
RINH1Ø		(Q19)	(A23)	"	"
RINH11		(Q2Ø)	(A21)	"	"
RINH12		(Q21)	(A28)	"	"
RINH13		(Q22)	(A25)	"	"
RINH14		(Q23)	(A29)	"	"
RINH15		(Q24)	(A27)	"	"
RI PRI*	L	E88	6	CPU1	Ø33-2
RI STRT*	L	E56	11	"	"
ROS	H	E48	12	"	Ø33-1
RQENB*	L	E73	6(B41)	"	Ø33-2
RST	L	(S5)	-	CON	Ø6Ø-1
		-	(B62)	CPU1	Ø33-3
RUN	H	E81	11	"	"
RUN*	L	E81	12	"	"
RUN IND*	L	E53	8(B72)	"	"
RUN SET	H	E1ØØ	3	"	"
RXR		-	(B93)	MEM	Ø29-1
RXS		-	(B91)	"	"
RYR		-	(B94)	"	"
RYS		-	(B96)	"	"
SELECT	H	E37	4, 1Ø	"	Ø29-2
SELECT*	L	E33	6	"	"
SEL X	H	E1	8(A26)	CPU2	Ø47-2
SEL Y	H	E69	6(A11)	"	"
SHIFT ACØ	H	E84	8	CPU3	Ø35-5
SHIFT AC1	H	E84	11	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
SHIFT MA	H	E67	6	CPU3	Ø35-2
SNSØ	H	E45	14	MEM	Ø29-3
SNSØ*	L	E24	12	"	"
SNS1	H	E45	12	"	"
SNS1*	L	E24	2	"	"
SNS2	H	E44	14	"	"
SNS2*	L	E2Ø	12	"	"
SNS3	H	E44	12	"	"
SNS3*	L	E2Ø	2	"	"
SNS4	H	E43	14	"	"
SNS4*	L	E18	12	"	"
SNS5	H	E43	12	"	"
SNS5*	L	E18	2	"	"
SNS6	H	E42	14	"	"
SNS6*	L	E14	12	"	"
SNS7	H	E42	12	"	"
SNS7*	L	E14	2	"	"
SNS8	H	E41	14	"	"
SNS8*	L	E12	12	"	"
SNS9	H	E41	12	"	"
SNS9*	L	E12	2	"	"
SNS1Ø	H	E4Ø	14	"	"
SNS1Ø*	L	E8	12	"	"
SNS11	H	E4Ø	12	"	"
SNS11*	L	E8	2	"	"
SNS12	H	E39	14	"	"
SNS12*	L	E6	12	"	"
SNS13	H	E39	12	"	"
SNS13*	L	E6	2	"	"
SNS14	H	E38	14	"	"
SNS14*	L	E2	12	"	"
SNS15	H	E38	12	"	"
SNS15*	L	E2	2	"	"
STA	H	E48	4(B4Ø)	CPU2	Ø47-2
STA*	L	E29	6	"	"
STOP*	L	(S5)	-	CON	Ø6Ø-1
		-	(B52)	CPU1	Ø33-3
STOP B*	H	E92	5	"	Ø33-2
STOP SYNC		E63	9	"	Ø33-3
STOP SYNC*		E63	8	"	"
STRB A	H	E35	6	MEM	Ø29-3
STRB B	H	E35	6	"	"
STRB C	H	E35	6	"	"

* INDICATES "NOT"

SUPERNOVA - SIGNAL ORIGIN

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
STRB D	H	E35	6	MEM	Ø29-3
STROBE		E14	5(B2Ø)	CPU1	Ø33-2
STROBE*		E14	6	"	"
STRT	H	E25	8(A52)	"	Ø33-2
STRT*	L	(S6)	-	CON	Ø6Ø-1
		-	(B66)	CPU1	Ø33-3
TSØ		E16	5(A96)	CPU1	Ø33-1
TSØ*		E16	6(B14)	"	"
TS3		E16	9(A67)	"	"
TS3*		E16	8(B45)	"	"
TC3		E38	15	CPU3	Ø35-2
TC7		E33	15	"	Ø35-3
TC11		E28	15	"	Ø35-4
TC15		E24	15	"	Ø35-5
TSØ. EXEC	H	E38	8	CPU2	Ø47-2
TSØ + TS3	H	E53	6	CPU1	Ø33-1
WRITE END		E19	9	"	"
WRITE END*		E19	8	"	"
WRITE MEM*	L	E36	8	MEM	Ø29-2
WRITE SYNCH		E63	5	CPU1	Ø33-1
WRITE SYNCH*		E63	6	"	"
XRRØ*	L	E52	13	MEM	Ø29-4
XRR1*	L	E52	12	"	"
XRR2*	L	E52	11	"	"
XRR3*	L	E52	1Ø	"	"
XRR4*	L	E52	9	"	"
XRR5*	L	E52	3	"	"
XRR6*	L	E52	4	"	"
XRR7*	L	E52	5	"	"
XRSØØ*	L	E58	13	"	"
XRS1Ø*	L	E58	12	"	"
XRS2Ø*	L	E58	11	"	"
XRS3Ø*	L	E58	1Ø	"	"
XRS4Ø*	L	E58	9	"	"
XRS5Ø*	L	E58	3	"	"
XRS6Ø*	L	E58	4	"	"
XRS7Ø*	L	E58	5	"	"

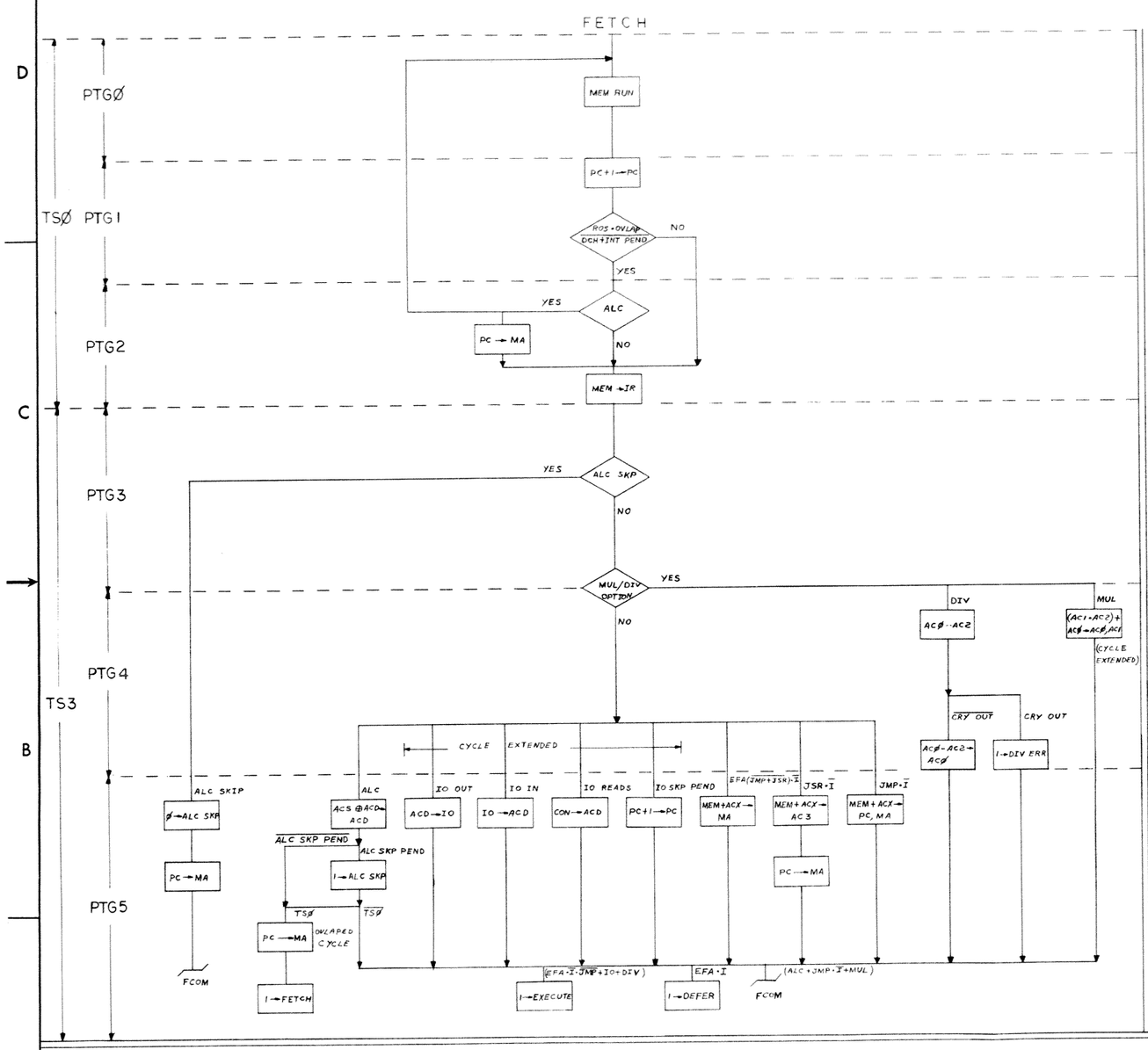
* INDICATES "NOT"

CENTRAL PROCESSOR AND MEMORY

LOGICAL SIGNAL	LEVEL	CHIP	PIN	BOARD	DWG.
XRRØ*	L	E61	13	MEM	Ø29-5
YRR1*	L	E61	12	"	"
YRR2*	L	E61	11	"	"
YRR3*	L	E61	1Ø	"	"
YRR4*	L	E61	9	"	"
YRR5*	L	E61	3	"	"
YRR6*	L	E61	4	"	"
YRR7*	L	E61	5	"	"
YRSØØ*	L	E62	13	"	"
YRS1Ø*	L	E62	12	"	"
YRS2Ø*	L	E62	11	"	"
YRS3Ø*	L	E62	1Ø	"	"
YRS4Ø*	L	E62	9	"	"
YRS5Ø*	L	E62	3	"	"
YRS6Ø*	L	E62	4	"	"
YRS7Ø*	L	E62	5	"	"

* INDICATES "NOT"

REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



QTY.	DESCRIPTION	PART NO.

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
PARTS TO BE FREE FROM BURRS
BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES ✓
MATERIAL
FINISH

DRAWN	DI VO DI PLACIDO	4-6-70
CHECKED		
ENGINEER	R. Grimes	4/23/70
APPROVED	[signature]	5/14/70
FIRST USED ON		

DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

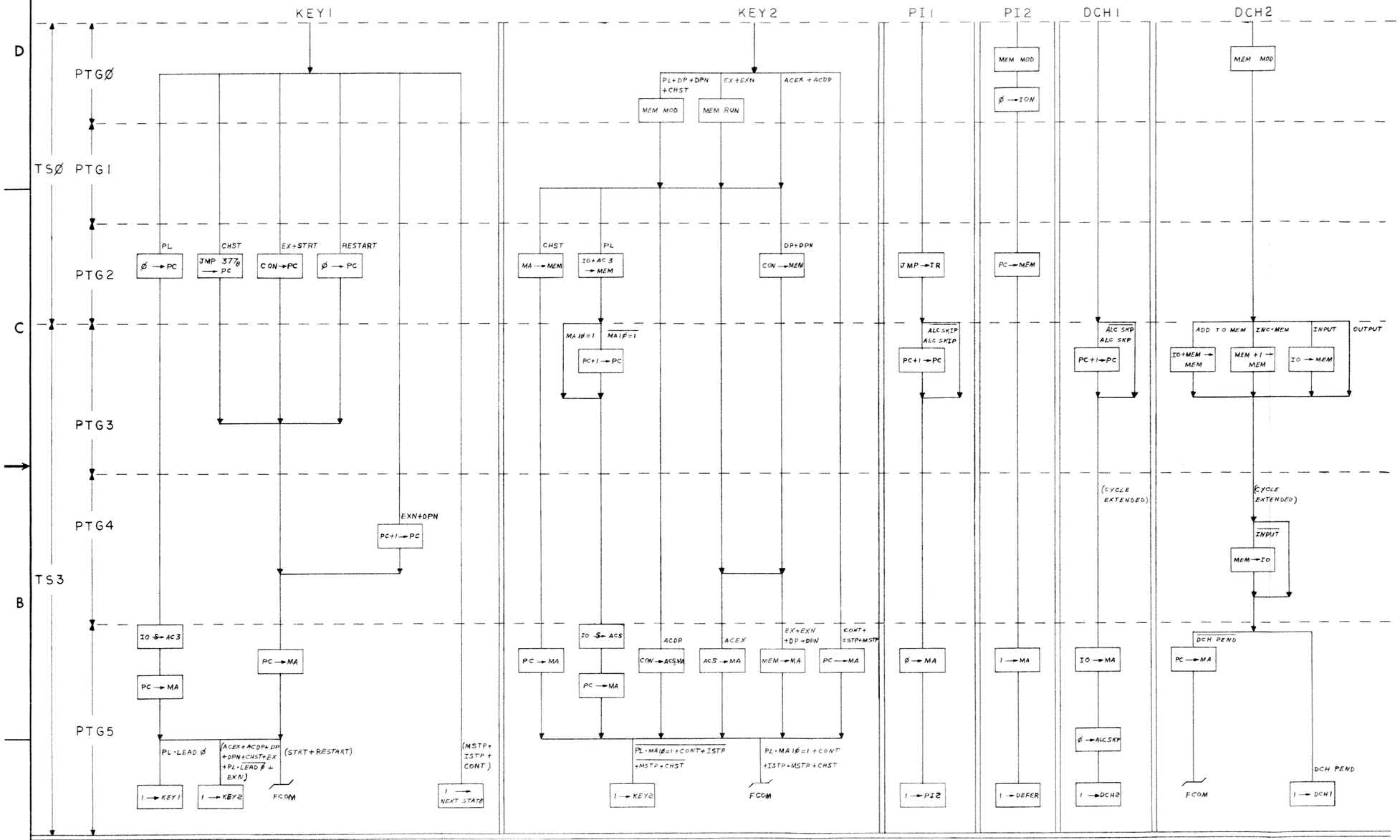
TITLE
SUPERNOVA / FLOW CHART
(FETCH / DEFER / EXECUTE)

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000081	00

SHEET SCALE 1 OF 2

SHEET OF

REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



QTY.	DESCRIPTION	PART NO.

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±
PARTS TO BE FREE FROM BURRS
BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED: ALL MACH. SURFACES ✓
MATERIAL
FINISH

DRAWN	DI VO DI PLACIDO	4-6-70
CHECKED		
ENGINEER	R. Grimm	4/23/70
APPROVED		5/19/70
FIRST USED ON		
SHEET SCALE	2 OF 2	

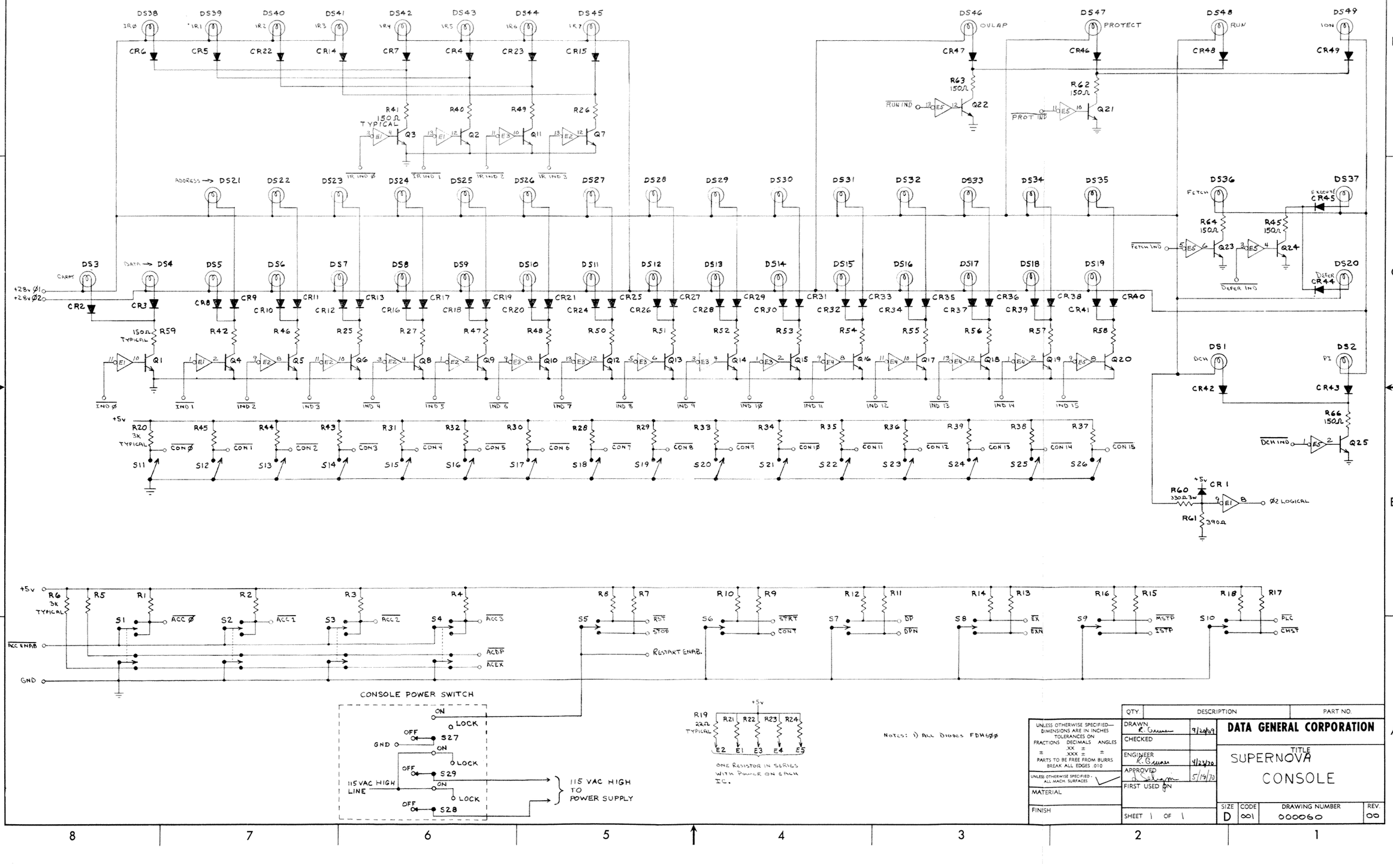
DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

TITLE
SUPERNOVA FLOW CHART
KEY · DCH · PI

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000061	00

SHEET OF

REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP. BY	DATE



UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES XX ± ± XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010

UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES

MATERIAL

FINISH

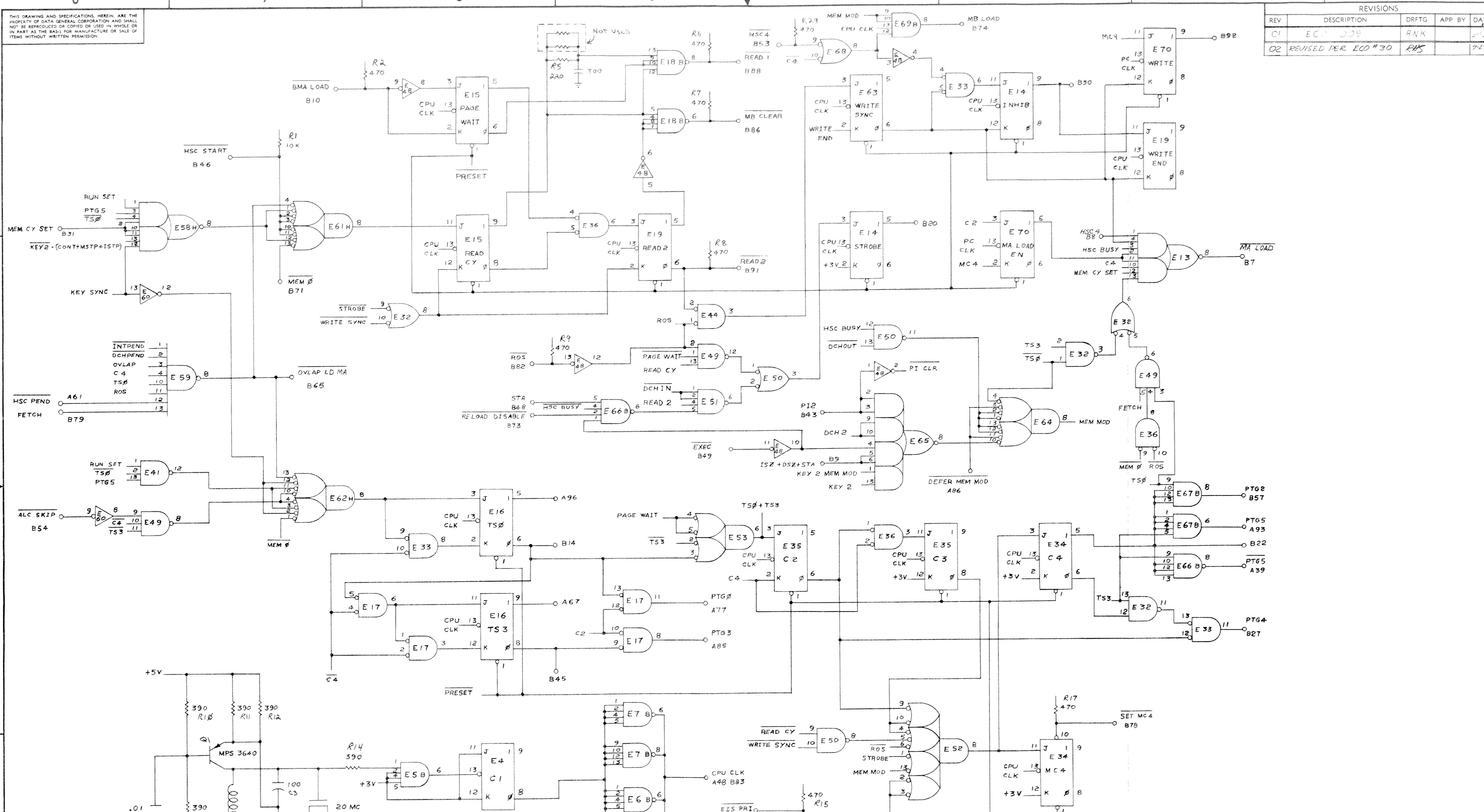
QTY.	DESCRIPTION	PART NO.
DRAWN R. Green	9/20/69	
CHECKED		
ENGINEER R. Green	4/24/70	
APPROVED	5/19/70	
FIRST USED ON		
SHEET 1 OF 1		

DATA GENERAL CORPORATION

TITLE
SUPERNOVA
CONSOLE

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000060	00

REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE
01	ECO 339	RNK		
02	REVISED PER ECO #30	RHS		7-27-70



BMA LOAD
B10
HSC START
B46
RUN SET
PTG5
MEM CY SET
B31
KEY SYNC
INTPEND
OVLAP
HSC PEND
FETCH
B79
RUN SET
ALC SKIP
B54
E15 PAGE WAIT
E15 READ CY
E19 READ 2
E18 B
READ 1
B88
MB CLEAR
B86
PRESET
MEM Ø
B71
STROBE
WRITE SYNC
OVLAP LD MA
B65
E16 TSØ
E16 TS3
A96
B14
A67
B45
PTGØ
A77
PTG3
A85
PAGE WAIT
READ CY
DCHIN
READ 2
STA
B48
HSC BUSY
RELOAD DISABLE
B73
MEM MOD
E69 B
MB LOAD
B74
E63 WRITE SYNC
WRITE END
E14 INHIB
B30
E14 STROBE
B20
E70 MA LOAD EN
E70 WRITE
B92
E19 WRITE END
MA LOAD
B7
HSC BUSY
DCHOUT
PI CLR
P12
B43
DCH 2
EXEC
B49
ISZ + DSZ + STA
KEY 2 MEM MOD
KEY 2
DEFER MEM MOD
A86
MEM MOD
FETCH
E35 C2
E35 C3
E34 C4
E34 MC4
PTG2
B57
PTG5
A93
B22
PTG5
A39
PTG4
B27
SET MC4
B78
READ CY
WRITE SYNC
EIS PRI
B34
RI PRI
IO PRI
WHOA
B84
PRI
+5V
MPS 3640
20 MC
E4 C1
CPU CLK
A48 B83
PC CLK
A47 B93
NOT USED

QTY.	DESCRIPTION	PART NO

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±. PARTS TO BE FREE FROM BURRS. BREAK ALL EDGES .010

UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES

MATERIAL

FINISH

DRAWN: DILYO / DI PLACIDO — 3-16-70

CHECKED

ENGINEER: R. G. — 4/23/70

APPROVED — 5/15/70

FIRST USED ON

SHEET 1 OF 3

DATA GENERAL CORPORATION

SOUTHBORO, MASSACHUSETTS 01772

TITLE

CPU 1 - SUPERNOVA PROCESSOR & MEMORY TIMING

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000033	02

SHEET OF

REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP BY	DATE
02	REVISED PER ECO # 089	[illegible]		7/27/70

R18 10K — PWR LOW — ION — CODE 77 — SELB* AB2 — SELB* AB0 — IR8 A15 — IR9 A10 — IO SKIP A88

R19 10K — R20 10K — RQENBF A23 — EIS RQ B75 — RQENB B41 — HSC BUSY — DCH — PT6Ø — PT6 3 — CPU CLK — IOTG1 — IOTG2 — DCHMØ — DCH 2(IO)

R27 10K — HALT — HSC LB RQ A21 — PTG 3 — STOPB — +3V — MR — CPU CLK — B52 STOP — ION SYNC AB — INT. PEND B81 — DCH PEND B85 — B29 INTR — PWR LOW — ION — FETCH — DCHR* B35 — RQ INH A7 — R28 10K — IO — INTA — IOTG2 — DCH2 — TS3 — PHASE — DCHR — FETCH — IR7 — IOTGØ — DCHØ — DCHIO — FAST DCH — C2 — IOTG3 — TSØ — IOTG1 — READ IN — IOTG1 — IOTG2 — HSC BUSY — IO IN — DCH2 — TSØ — IO OUT ENAB A94 — IO OUT B90 — IO RLS SET A30 — IO RLS — PRESET — C4 — READ IN — RI PRI — IO PRI

TSØ+TS3 — B56 DCH1 — DCHP A17 10K — IO — B6 — FETCH — IO TIME B38 — DCH1IO — IO — DCH — TS3 — PTG 5 — IO BUSY E76 — CPUCLK — PRESET — CHST — SELD — KEY 1 — FLAGHT — TS3 — KEY 2 — TS3+TS3 PL — WAIT — IOTG3 — READ IN — RI STRT — IOTG4 — IOTG E57 — +3V — FAST DCH — DCHP — PTG5 — CPU CLK — E104 FAST DCH — READ IN

IR5 B25 — IR6 B23 — IO — IR7(IO) — IOBUSY — IOTG2 — IO — EXEC B47 — IR7 B5 — CODE 77 A81 — IR8 — IR9 — HALT — E38 — RI STRT — R26 470 — EXT. ION ENAB A32 — PI CLR — RESET — B55 ION — ION — STRT A52 — CLR A50 — IO PLS A74

IOTG1 — IOTG3 — IO TIME — IR7 — IR7(IO) — E20 — MSKO A38 — DATOA A58 — DATOB A56 — DATOC A41

CON 10 A92 — MEM 10 A45 — CON 11 A91 — MEM 11 A51 — CON 12 A75 — MEM 12 A36 — CON 13 A78 — MEM 13 A35 — CON 14 A73 — MEM 14 A76 — CON 15 A71 — MEM 15 B18 — DS Ø A72 — DS 1 A68 — DS 2 A66 — DS 3 A46 — DS 4 A62 — DS 5 A64

R21 10K — HSC BUSY A59 — DCH 2(IO) — MODE Ø — DCHMØ B17 — DCHM1 B21 — IOTG1 — 220Ω — 330pF — IOTG3 — DCH IN A87 — CRYSNC A96 — A97 — TS3 — DCH INC A53 — DCH OUT — DCHMØ

R22 10K — DCHAT A31 — DCH ATN A60 — DCHA

R23 10K — DCHIF A25 — DCHI B37

R24 10K — DCHOF A29 — DCHO B33

R25 10K — OVFLOW A27 — OVFLO B39

E21 — IO IN A77 — PL READ IO — HSC BUSY — A34 READS — INTA — A40 INTA — RESET — A70 IO RST — DATIA A44 — DATIB A42 — DATIC A54

R30,31,32,33,34,35

R36,37,38,39,40,41

+5V — 330 — 390 — Typical Termination Net.

QTY.	DESCRIPTION	PART NO.

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± XX ± ± XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010 — UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES — MATERIAL — FINISH

DRAWN R. Gagnon 9/23/69 — CHECKED — ENGINEER R. Gagnon 4/23/70 — APPROVED [illegible] 5/19/70 — FIRST USED ON

DATA GENERAL CORPORATION

TITLE: CPU 1 - SUPERNOVA INPUT/OUTPUT

SIZE D — CODE 001 — DRAWING NUMBER 000033 — REV. 02 — SHEET 2 OF 3

REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

KEY START
CONT+ISTP+MSTP
E105
E69B
PRESET B77
RESET
+5 OK A9
RST B62
MEM OK A5
E97
E87
.05 C5
220
R42
0.01μf
E63 STOP SYNC
CPU CLK
E80
KEY SYNC
KEY1 B63
OVLAP A89
KEYSYNC RUN
E81
NR DS LD SH CLK
+3V
CPU CLK
E100
KEY START
PTG5 A39
E99
TS3
E53
RUN IND B72
E98B
Ø2 IND DRIVE B11
E98B
Ø1 IND DRIVE B13
Ø2 LOGICAL B12
KEY1
STOP B
E33
F SET B67
ISTP
MSTP
E103
KEY 2 B32
ACEX+ACDP
E100
B24 ACC ENABLE
MANUAL FUNCTION
E102
E103
CONT+ISTP+MSTP
CHST A57
E84
CHST B60
PL
E85
PL+CHST
DP+DPN A76
DP B59
DPN B70
EXN B68
E68
DPN+EXN A83
EX B64
STRT B66
EX+STRT A55
CONT+ISTP+MSTP B47
CONT B58
ISTP B51
MSTP B50
ACEX B94
ACDP B95
E83
RESTART
R43 10K
CONT+ISTP+MSTP
ISTP MSTP
E85
HALT
E79
MSTP+KEY2
MANUAL FUNCTION
E100
KEY2
E101
KEY2 SET B61
KEY2 MEM MOD
EX+EXN+DP+DPN A69
CHST
E99
KEY1 PCLD B15
PL LEAD Ø
KEY1 SET B19
RUN SET
TSØ
RUN
E105
C6 6.8μf
R44 8.2K
E106 SCHMIDT
E82
PLC B26
+5V
R47 180
+3V
R48 470
ADDER=Ø B96
KEY 1
E87
PL LEADØ
PL A89
E86 PL
PLC
D Ø
MA ZERO BUS B89
KEY2
E87
PL CYCLE B87
E104 KEY START
CPU CLK
+3V
MANUAL FUNCTION
C7 6.8μf
4K (INTERNAL)
E86 KEY SEEN
KEY SEEN
KEY SYNC

QTY	DESCRIPTION	PART NO.
DRAWN DI PLACIDO	3-17-70	
CHECKED		
ENGINEER R. Swan	4/22/70	
APPROVED J. Gay	5/11/70	
FIRST USED ON		

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES XX ± ± XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES
MATERIAL
FINISH

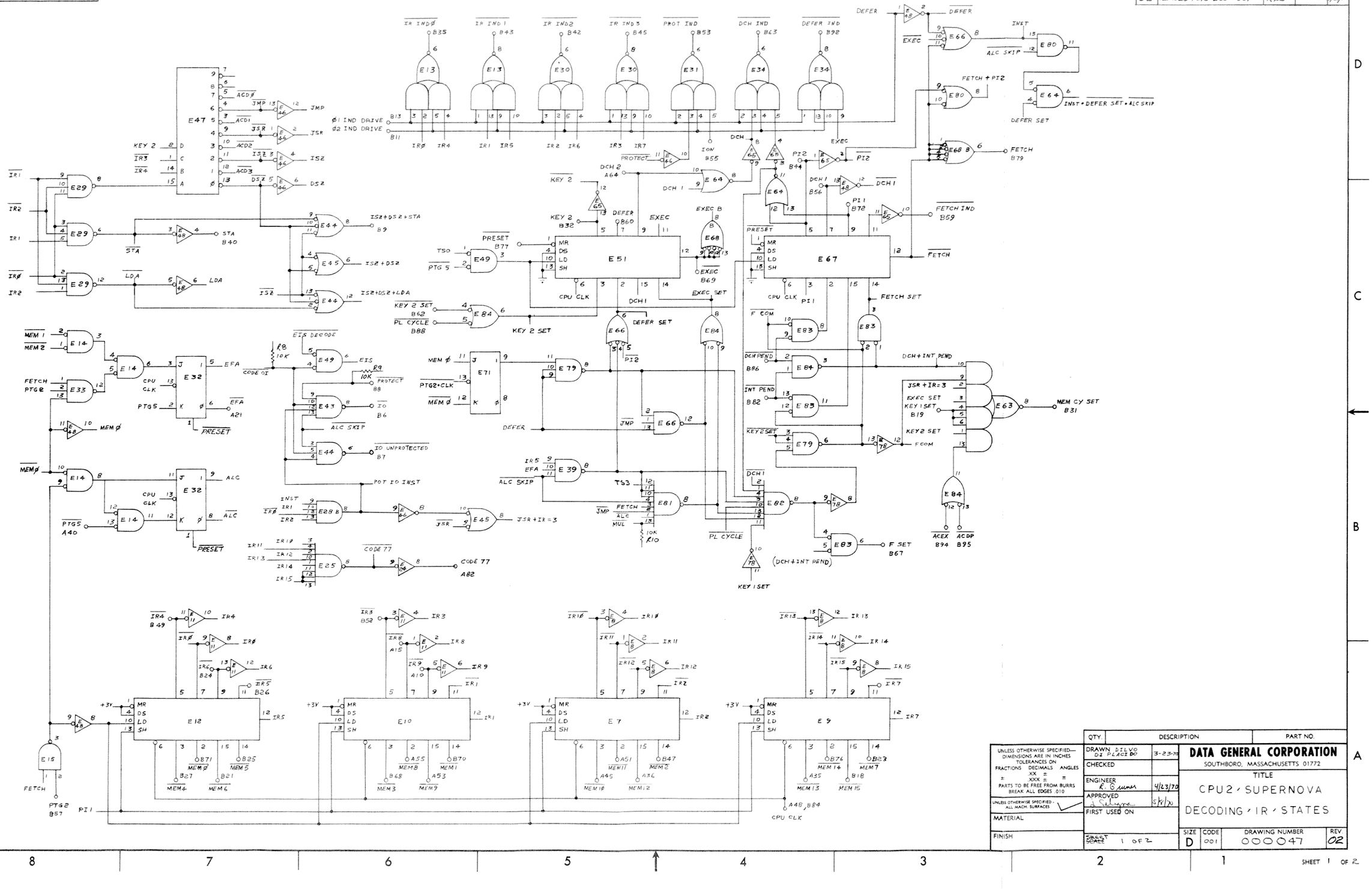
DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

TITLE
CPU 1, SUPERNOVA CONSOLE LOGIC

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000033	02

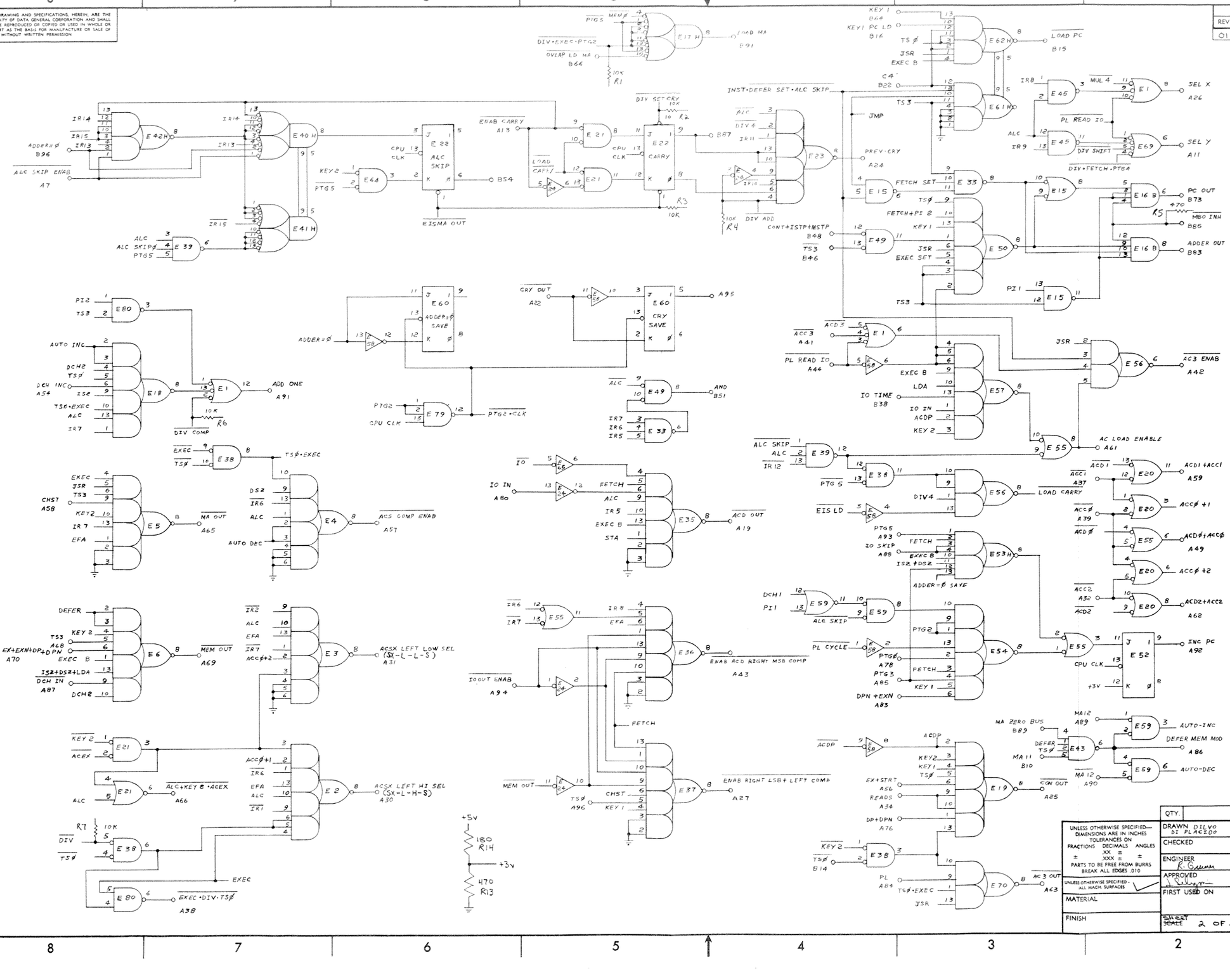
SHEET SCALE 3 OF 3
SHEET OF

REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE
02	REVISED PER ECO# 031	[illegible]		7/27/70



UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± XX ± ± ± XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010	QTY.	DESCRIPTION	PART NO.
UNLESS OTHERWISE SPECIFIED: ALL MACH. SURFACES ✓	DRAWN DILVO DI PLACIDO	3-23-70	DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772
MATERIAL	CHECKED		TITLE
FINISH	ENGINEER R. G. Jones	4/23/70	CPU2 - SUPERNOVA
	APPROVED A. Silverman	5/1/70	DECODING - IR - STATES
	FIRST USED ON		SIZE D · CODE 001 · DRAWING NUMBER 000047 · REV 02
	SHEET SCALE 1 OF 2		SHEET 1 OF 2

REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP. BY	DATE
01	REVISED PER ECO-003			



QTY.	DESCRIPTION	PART NO.

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES XX ± ± XXX ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010

UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES

MATERIAL

FINISH

DRAWN DILVO DI PLACIDO 3-25-70

CHECKED

ENGINEER R. Gumm 4/23/70

APPROVED A. Silvern 5/18/70

FIRST USED ON

DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

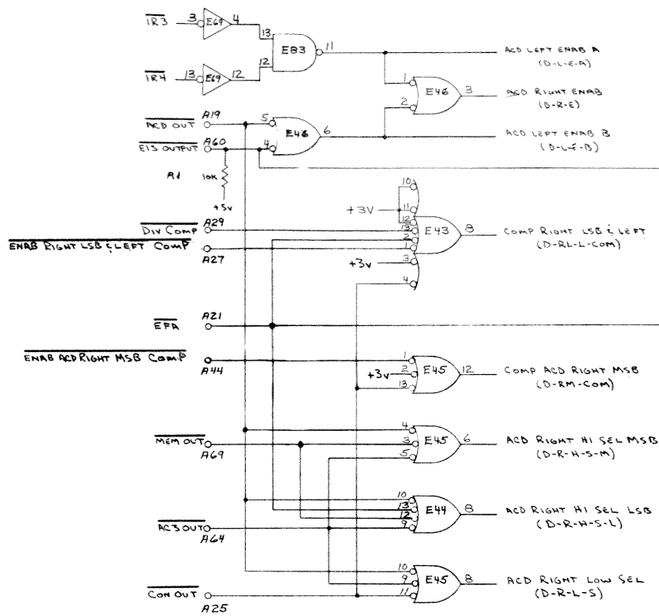
TITLE
CPU 2-SUPERNOVA
ADDER-MULTIPLEXOR
REGISTER LOAD-CONTROLS

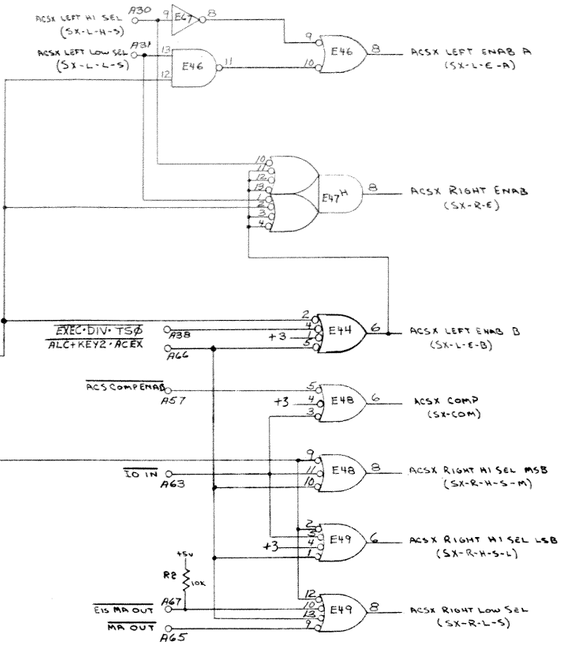
SIZE	CODE	DRAWING NUMBER	REV.
D	001	000047	02

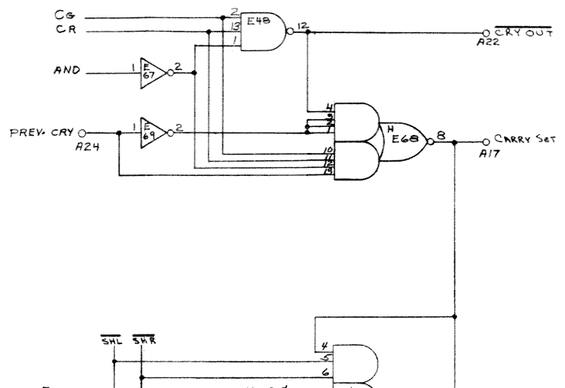
~~SHEET~~ ~~SCALE~~ 2 OF 2

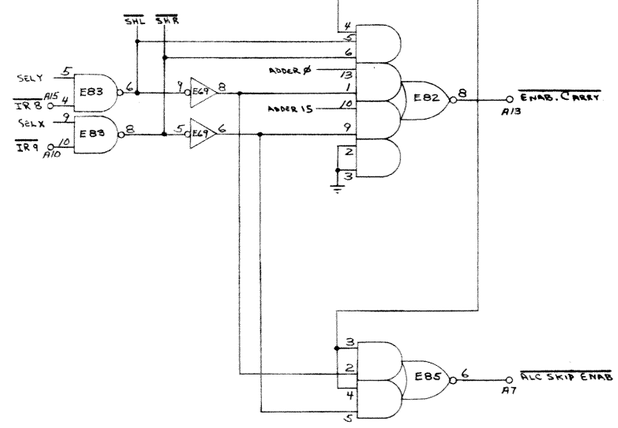
SHEET 2 OF 2

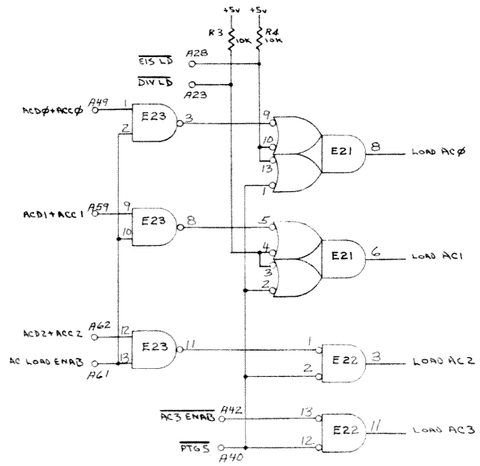
REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP. BY	DATE
01	CHANGED PER ECO- 00E			











UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES .XX ± .XXX ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED · ALL MACH. SURFACES ✓
MATERIAL
FINISH

QTY.	DESCRIPTION	PART NO.
DRAWN K. Gumm	9/17/69	
CHECKED		
ENGINEER K. Gumm	4/23/70	
APPROVED J. Silvagni	5/18/70	
FIRST USED ON		

DATA GENERAL CORPORATION

TITLE

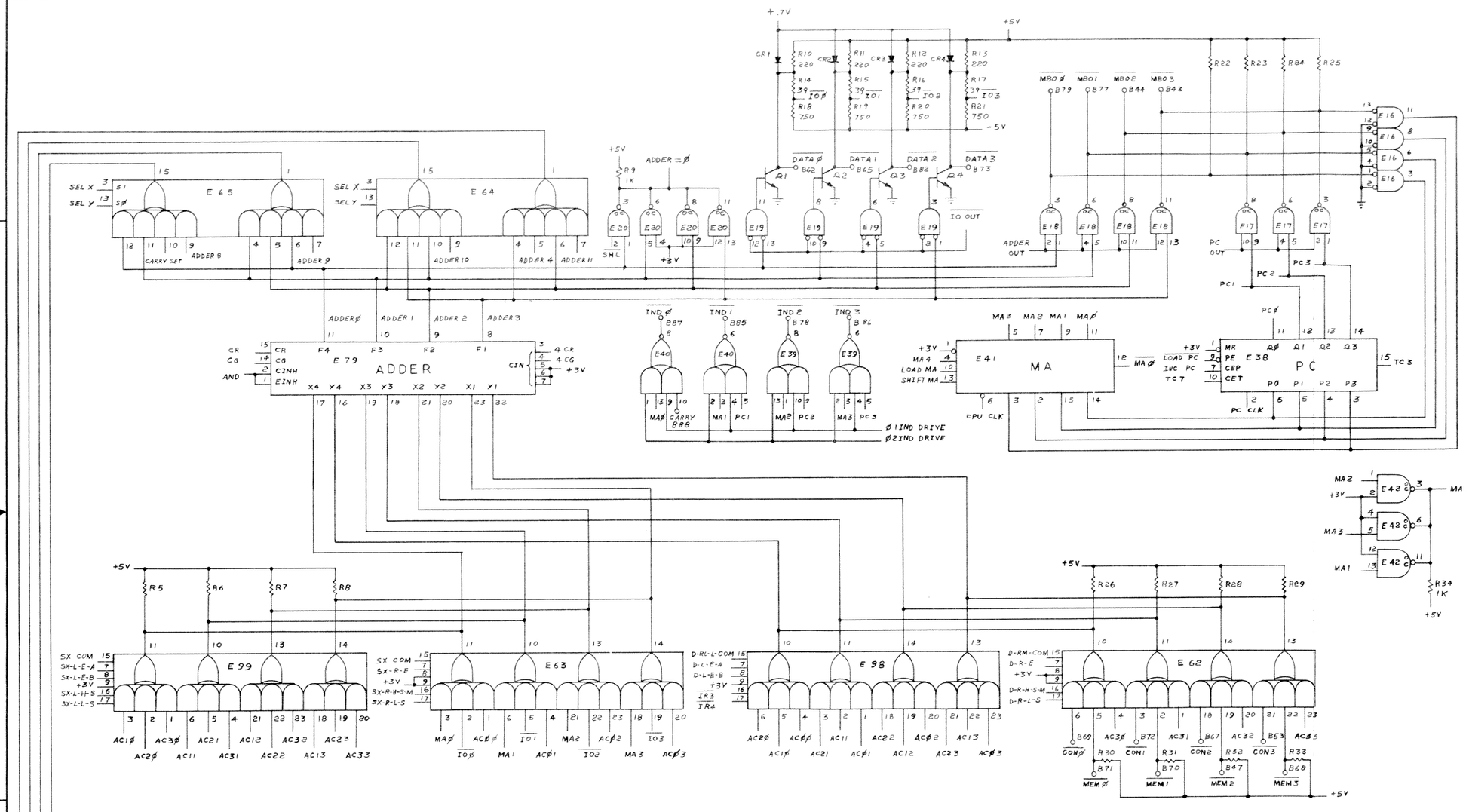
SEL & REG DRIVE LOGIC

CPU 3

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000035	01

SHEET 1 OF 5

REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP. BY	DATE

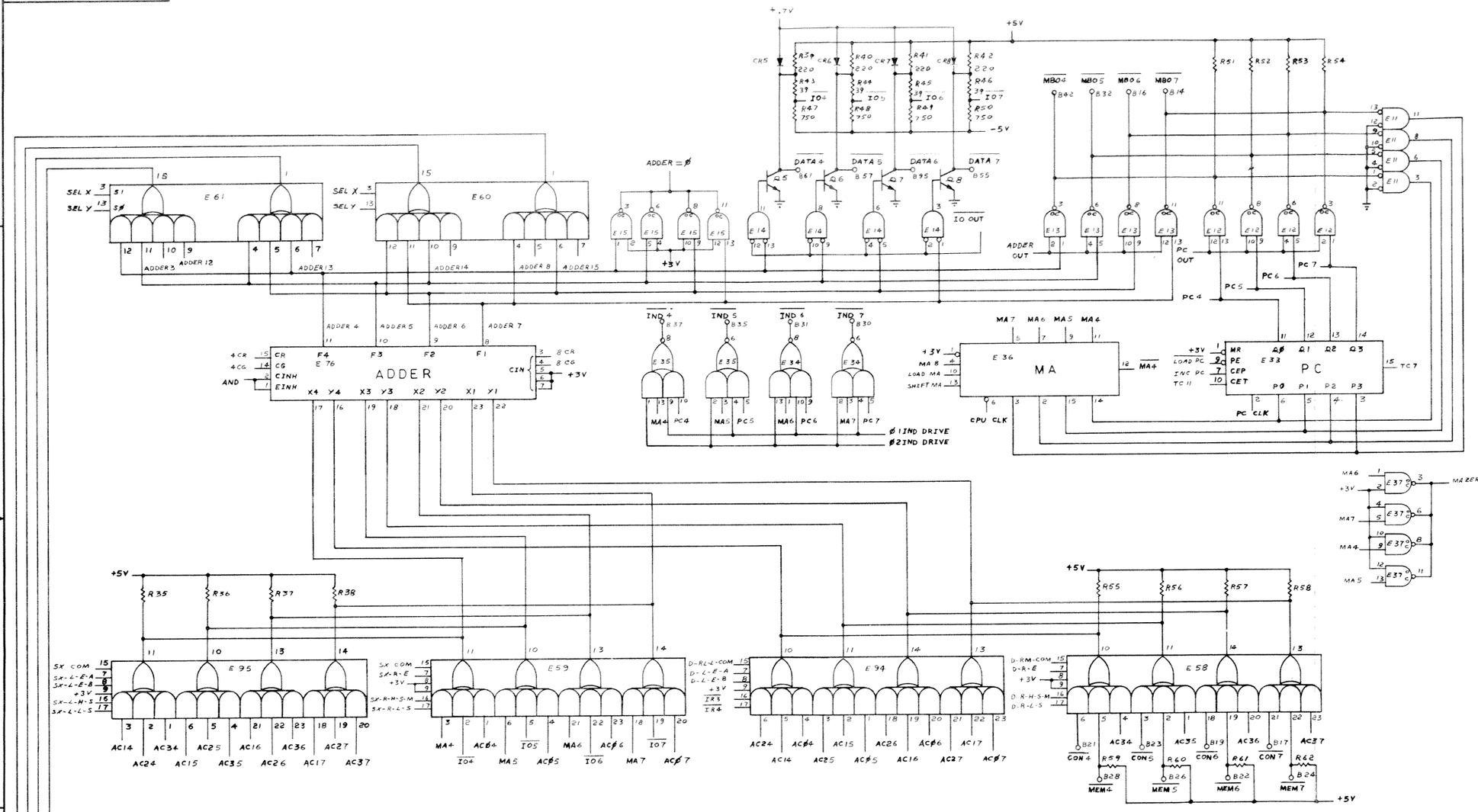


QTY.	DESCRIPTION	PART NO.
	DRAWN DILVO DI PLACIDO 5-19-70	DATA GENERAL CORPORATION
	CHECKED	SOUTHBORO, MASSACHUSETTS 01772
	ENGINEER K. Guenes 4/23/70	TITLE CPU3
	APPROVED J. Nelson 5/8/70	MAJOR REGISTERS
	FIRST USED ON	GATING, ADDER
	MATERIAL	BITS Ø-3
	FINISH	SIZE D · CODE 001 · DRAWING NUMBER 000035 · REV 01
		SHEET SCALE 2 OF 5

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS DECIMALS ANGLES XX ± XXX ± ± . PARTS TO BE FREE FROM BURRS. BREAK ALL EDGES .010. UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES.

SHEET OF

REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP BY	DATE



NOTE: UNLESS OTHERWISE NOTED ALL RESISTORS ARE 470Ω

QTY.	DESCRIPTION	PART NO.

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±
PARTS TO BE FREE FROM BURRS
BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED · ALL MACH. SURFACES
MATERIAL
FINISH

DRAWN DILVO DI PLACIDO	3-19-70	
CHECKED		
ENGINEER K. Ogumma	4/23/70	
APPROVED R. Swoboda	5/8/70	
FIRST USED ON		
SHEET SCALE	3 OF 5	

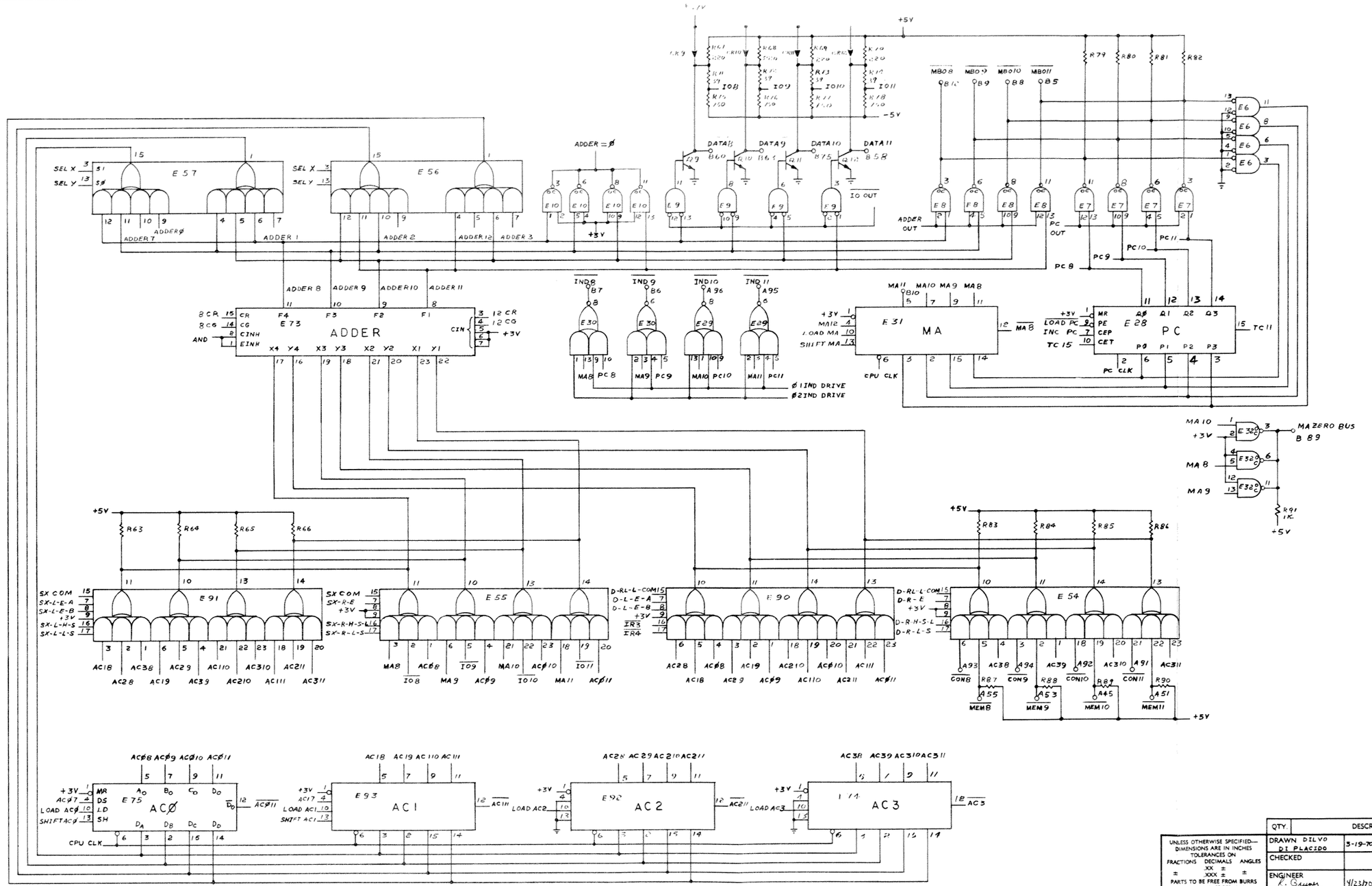
DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

TITLE CPU3
MAJOR REGISTERS
GATING, ADDER
BITS 4-7

SIZE	CODE	DRAWING NUMBER	REV
D	001	000035	01

SHEET OF

REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP. BY	DATE



NOTE: UNLESS OTHERWISE NOTED ALL RESISTORS ARE 470Ω

QTY.	DESCRIPTION	PART NO.

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± XX ± ± XXX ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010

UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES ✓

MATERIAL

FINISH

DRAWN DILVO DI PLACIDO 3-19-70

CHECKED

ENGINEER R. Gwinn 4/23/70

APPROVED J. Sobon 5/1/70

FIRST USED ON

SCALE 4 OF 5

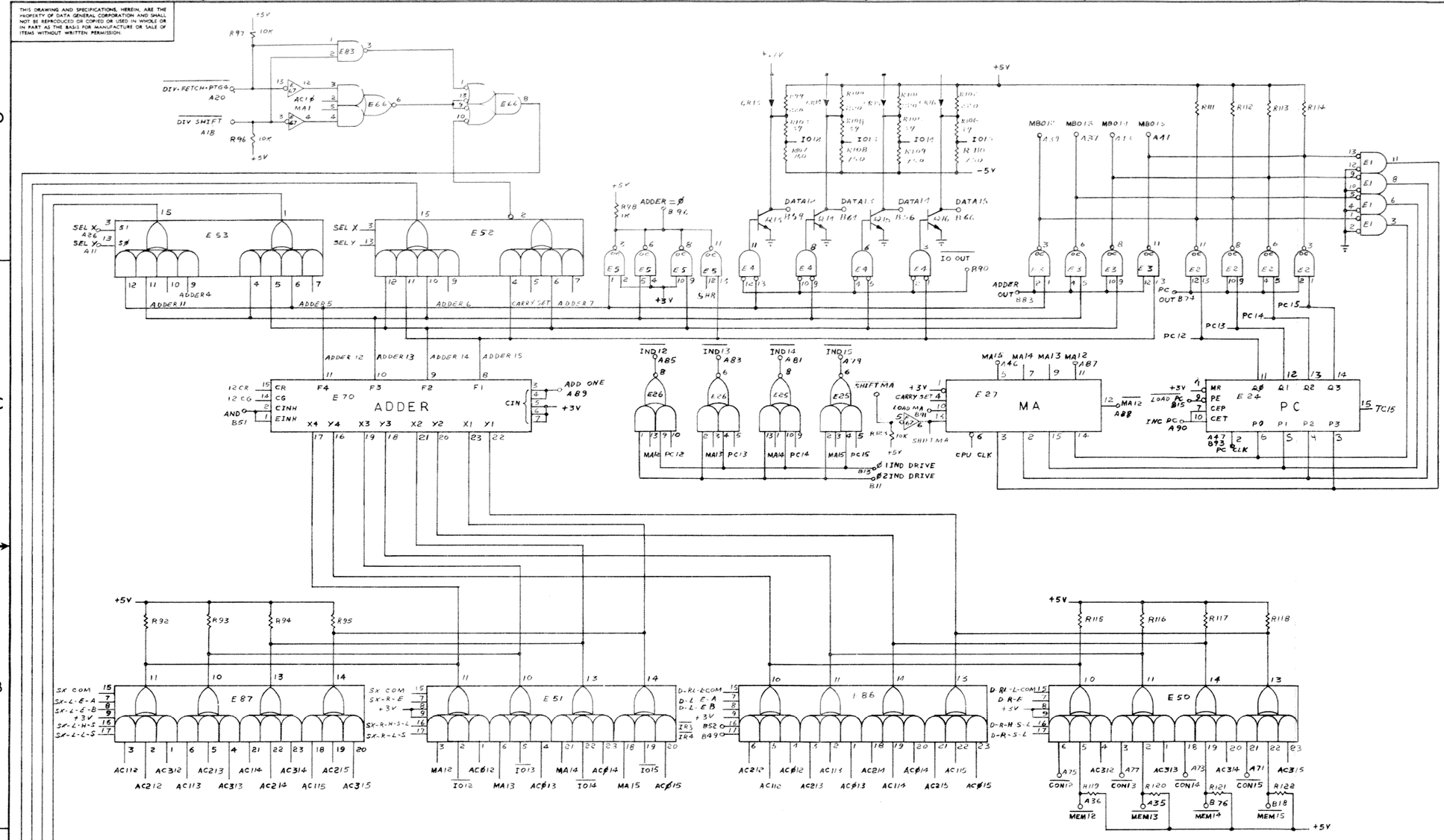
DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

TITLE CPU3
MAJOR REGISTERS
GATING / ADDER
BITS 8-11

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000035	01

SHEET OF

REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP. BY	DATE



NOTE: UNLESS OTHERWISE NOTED ALL RESISTORS ARE 470 Ω

QTY.	DESCRIPTION	PART NO.
DRAWN DILVO DI PLACIDO	3-19-70	
CHECKED		
ENGINEER R. Guma	4/23/70	
APPROVED J. Salvagni	5/5/70	
FIRST USED ON		

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES XX ± ± XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010

UNLESS OTHERWISE SPECIFIED — ALL MACH. SURFACES ✓

MATERIAL

FINISH

DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

TITLE CPU 3
MAJOR REGISTERS
GATING / ADDER
BITS 12 – 15

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000035	01

SHEET SCALE 5 OF 5

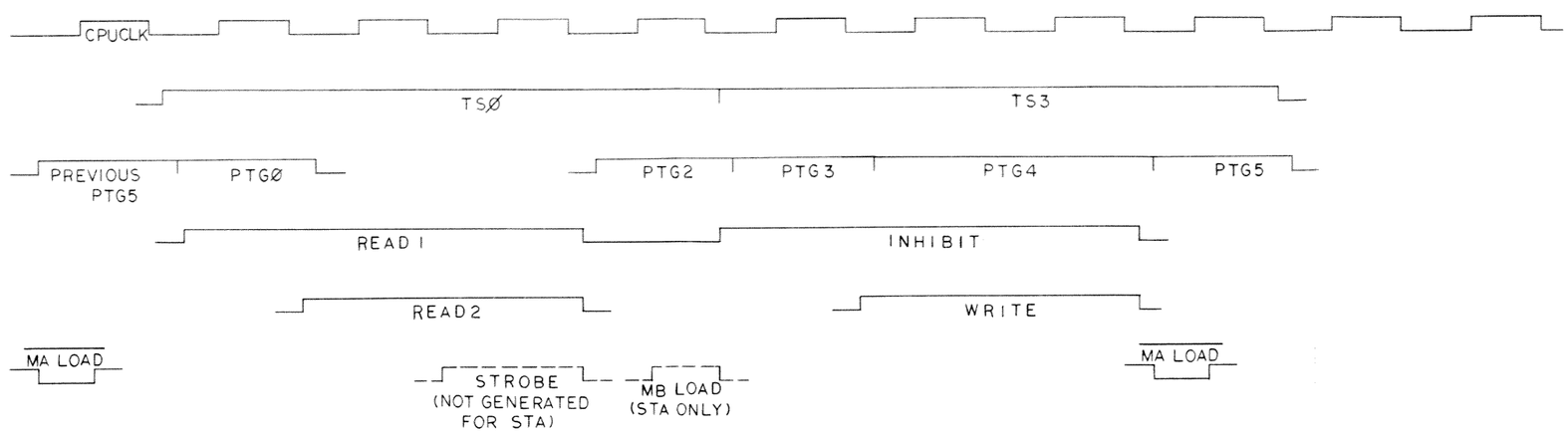
SHEET OF

REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

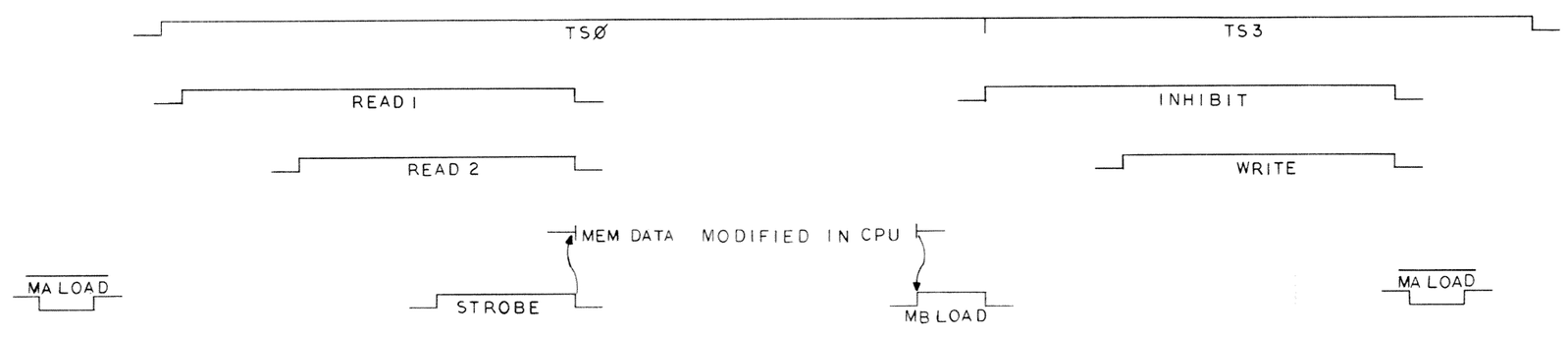
NS -100 Ø 100 200 300 400 500 600 700 800 900

BASIC MEMORY CYCLE FROM CORE:

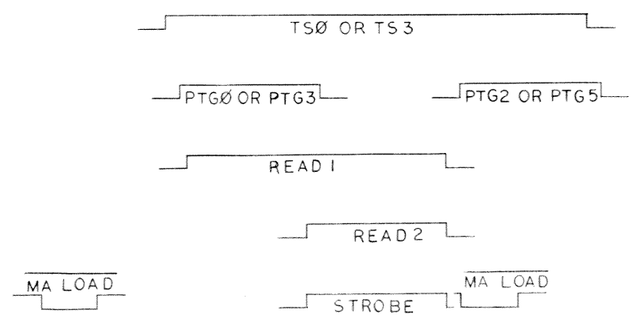
FETCH
DEFER (NOT AUTO-INDEX)
STA • EXECUTE
KEY2 • $\overline{CHST}$ • $\overline{DP}$ • $\overline{DPN}$



MEMORY MODIFY CYCLE(CORE)
DEFER (AUTO-INDEX)
ISZ • EXEC
DSZ • EXEC
P I 2
DCH 2
KEY2 (CHST + DP + DPN)



ROS MEMORY CYCLE



QTY	DESCRIPTION	PART NO.

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± XX ± ± ± XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES ✓
MATERIAL
FINISH

DRAWN D. LAVO D1 PLACIDO 4-9-70
CHECKED
ENGINEER R. Grimm 4/23/70
APPROVED J. Selwyn 5/19/70
FIRST USED ON

DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

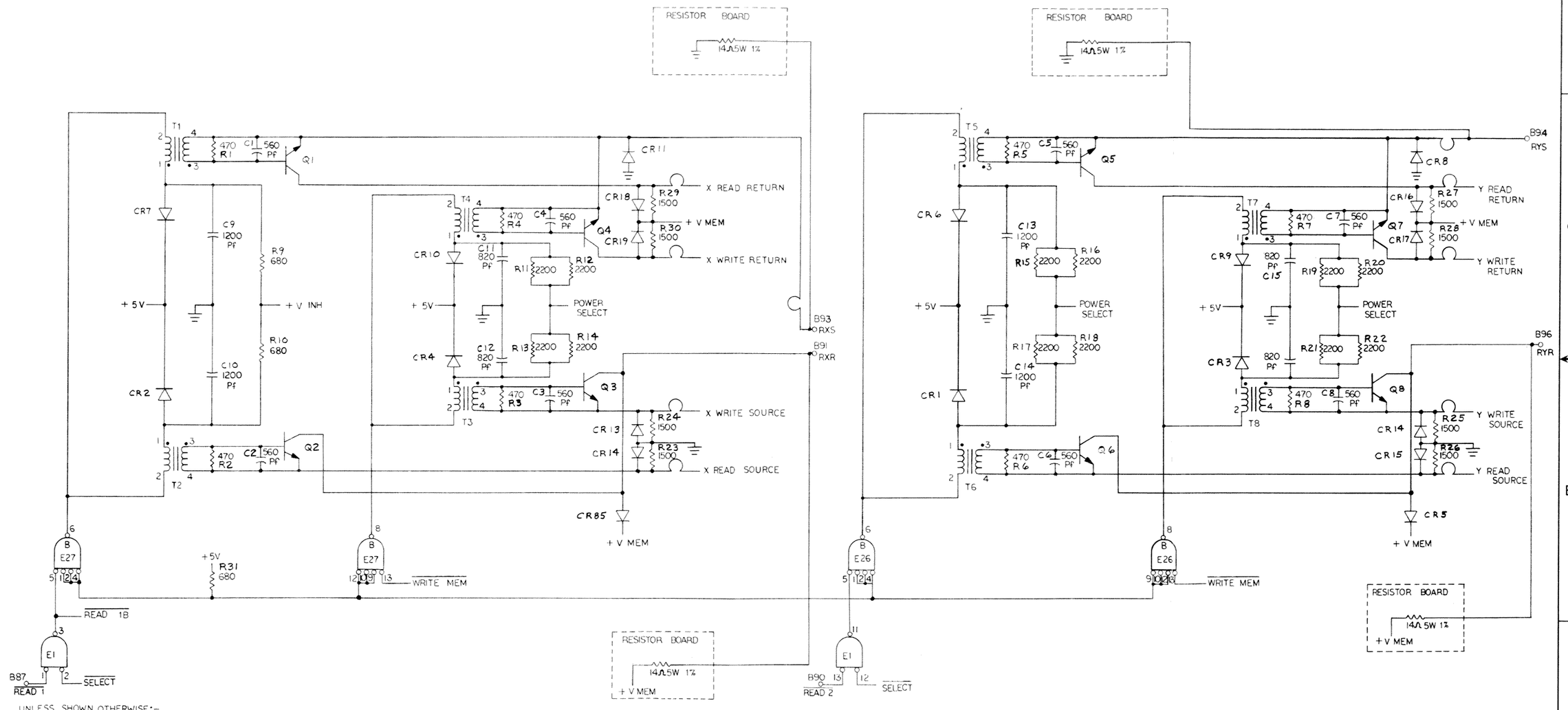
TITLE
SUPERNOVA
MEMORY TIMING

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000062	00

SHEET SCALE 1 OF 1

SHEET OF

REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP BY	DATE



UNLESS SHOWN OTHERWISE:-

RESISTORS ARE 1/4W 5%
DIODE = FDH600
TRANS = 2N3725
TRANSFORMER = 104000012

QTY.	DESCRIPTION	PART NO.

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
XX ± ± ±
XXX ± ±
PARTS TO BE FREE FROM BURRS
BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED — ALL MACH. SURFACES
MATERIAL
FINISH

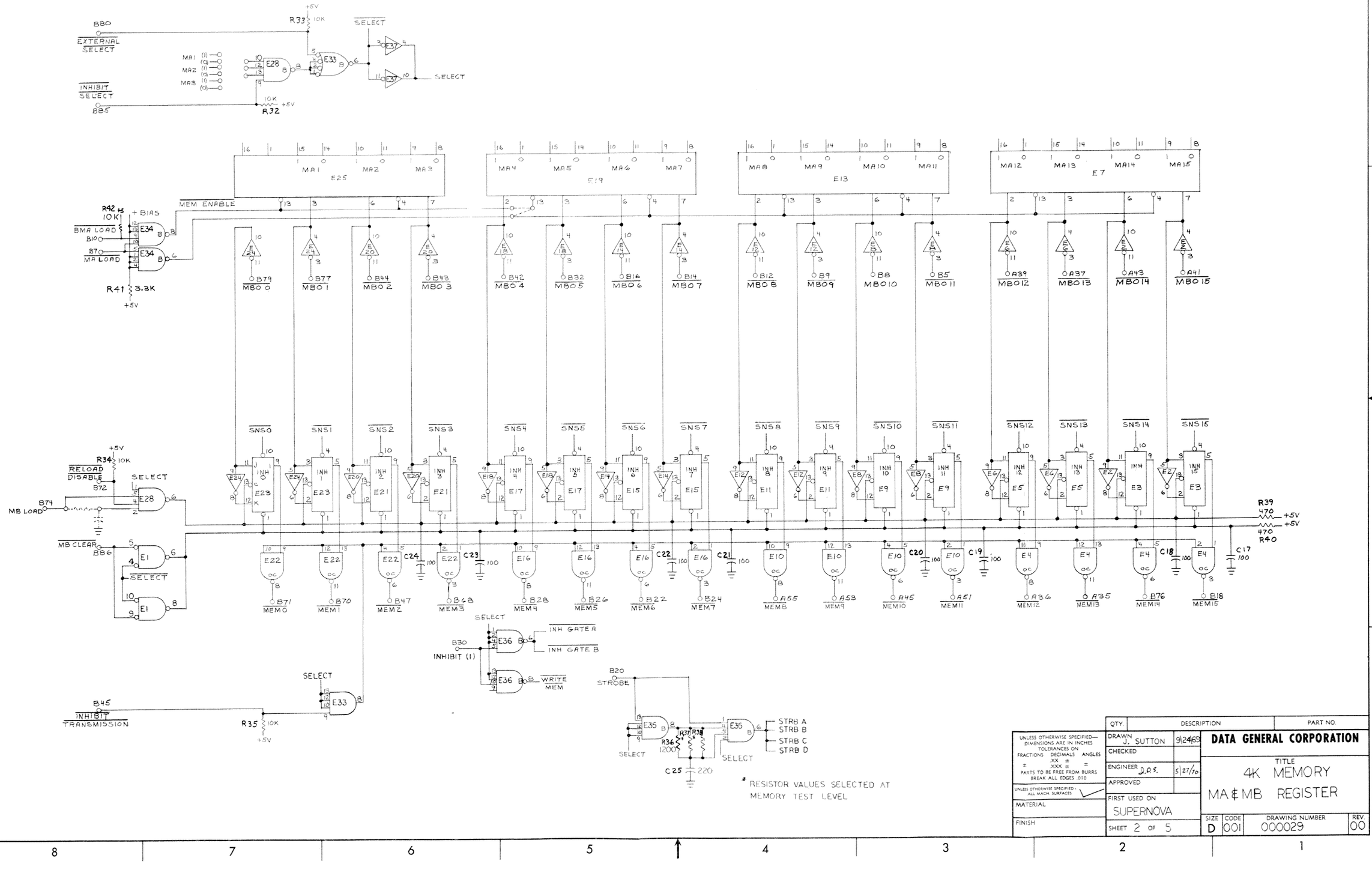
DRAWN CHET JOHNSON 9/24/69
CHECKED
ENGINEER D.D.S. 5/27/70
APPROVED
FIRST USED ON SUPERNOVA
SHEET 1 OF 5

DATA GENERAL CORPORATION

TITLE
4K MEMORY
FLIPPERS

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000029	00

REVISIONS				
REV.	DESCRIPTION	DRFTG	APP BY	DATE



UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± XX ± ± XXX ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010	QTY.	DESCRIPTION	PART NO.
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES ✓	DRAWN J. SUTTON	9/24/69	DATA GENERAL CORPORATION
MATERIAL	CHECKED		TITLE 4K MEMORY MA & MB REGISTER
FINISH	ENGINEER D.P.S.	5/27/70	
	APPROVED		
	FIRST USED ON SUPERNOVA		
	SHEET 2 OF 5		SIZE D · CODE 001 · DRAWING NUMBER 000029 · REV 00

REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP. BY	DATE

NOTE : COMPONENT VALUES SHOWN IN CIRCUITS RINHØ AND SNSØ ARE THE SAME FOR EACH TYPE OF COMPARABLE CIRCUIT, I.E., RINH1 - 15, SNS1 - 15.

INH GATE A

INH GATE B

POWER SELECT

STRB B

STRB D

+ V INH

QTY.	DESCRIPTION	PART NO.

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES XX ± XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010

UNLESS OTHERWISE SPECIFIED: ALL MACH. SURFACES

MATERIAL

FINISH

DRAWN CHET JOHNSON 9/29/69

CHECKED

ENGINEER D. Sutton 5/27/70

APPROVED

FIRST USED ON SUPERNOVA

SHEET 3 OF 5

DATA GENERAL CORPORATION

TITLE

4K MEMORY

SENSE & INHIBIT

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000029	00

UNLESS SHOWN OTHERWISE:-
RESISTORS ARE ¼ W 5%
CAP = 1200 PF
DIODE = FDH600
TRANSFORMER = 104000012
BALUN = 104000013
USE HEAT SINKS ON 2N3725 TRANS.
TRANSISTORS = 2N3725

REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

846 +V MEM

½ +V MEM

CR99

XRS70 XRS60 XRS50 XRS40 XRS30 XRS20 XRS10 XRS00

Q32 2N4123, Q37, Q34, Q35, Q33, Q36, Q31, Q38

R176 390, R175 3300, R185, R179, R181, R177, R183, R173, R187, R163 39

R186, R180, R182, R178, R184, R174, R188

E54, E69

CR98 CR101 CR102 CR103 CR105 CR104 CR94 CR95 CR97 CR96 CR106 CR107 CR109 CR108 CR90 CR91 CR93 CR92 CR110 CR111 CR113 CR112 CR86 CR87 CR89 CR88 CR114 CR115 CR117 CR116

R203 1500, R204 1500, R205, R206, R201, R202, R207, R208, R199, R200, R209, R210, R197, R198, R211, R212

P3 2, P3 3, P2 13, P2 12, P3 6, P3 7, P2 9, P2 8, P3 5, P3 4, P2 10, P2 11, P3 1, P3 14, P2 14, P2 1

E80 E76 E82 E78 E79 E75 E81 E77

TP CURRENT

X READ SOURCE

X WRITE RETURN

X WRITE SOURCE

X READ RETURN

CR147 CR148 CR128 CR127 CR143 CR144 CR131 CR132 CR135 CR136 CR121 CR119 CR139 CR140 CR123 CR124

CR146 CR149 CR129 CR126 CR145 CR142 CR130 CR133 CR137 CR134 CR120 CR118 CR138 CR141 CR122 CR125

E73 E46

R194 390, R168, R196, R166, R192, R172, R190, R170

R193 3300, R164 39, R162 4, R158 470, R159 470, R160 680, R161 680

Q41 2N4123, Q28, Q42, Q27, Q40, Q30, Q39, Q29

R167, R195, R165, R191, R171, R189, R169

+5V

READ 1B

WRITE MEM

READ 1C

XRR0 \RR1 \RR2 \RR3 \RR4 XRR5 /RR6 /RR7

E67

E58

$\overline{XRS}$

$\overline{MEM\ ENABLE}$ 2 D

MA 10 (1) 1 C

MA 11 (1) 14 B

MA 12 (1) 15 A

70 60 50 40 30 20 10 00

5 4 3 9 10 11 12 13

E52

$\overline{XRR}$

$\overline{MEM\ ENABLE}$ 2 D

MA 13 (1) 1 C

MA 14 (1) 14 B

MA 15 (1) 15 A

7 6 5 4 3 2 1 0

5 4 3 9 10 11 12 13

R268 3300, R269, ½ +V MEM

R270 1500, C58 62.4ff 35V.

846 +V MEM

UNLESS SHOWN OTHERWISE:—
RESISTORS ARE ¼ W 5%
DIODE = FDH600
D.I.P. DIODE = 100000001
Q27-Q42 ARE 2N4123

QTY	DESCRIPTION	PART NO

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
.. XX ± ... ° ±
... XXX ± ...
PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES
MATERIAL
FINISH

DRAWN CHET JOHNSON 10/5/69
CHECKED
ENGINEER J.D.S. 5/27/69
APPROVED
FIRST USED ON SUPERNOVA
SHEET 4 OF 5

DATA GENERAL CORPORATION

TITLE
4K MEMORY
X SELECTORS

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000029	00

REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP. BY	DATE

B46 +V MEM

½ +V MEM

$\overline{YRS70}$ $\overline{YRS60}$ $\overline{YRS50}$ $\overline{YRS40}$ $\overline{YRS30}$ $\overline{YRS20}$ $\overline{YRS10}$ $\overline{YRS00}$

2N4123 Q55 Q48 Q57 Q50 Q58 Q49 Q56 Q47

R252 390 R253 3300 R231 R232 R256 R257 R253 R236 R258 R259 R233 R234 R254 R255 R229 R230 R242 39 R243 39

CR201 CR200 1500 R261 R260 1500 CR198 CR199 CR165 CR164 R220 R219 CR162 CR163 CR205 CR204 R263 R262 CR202 CR203 CR161 CR160 R218 R217 CR158 CR159 CR209 CR208 R265 R264 CR206 CR207 CR157 CR156 R216 R215 CR154 CR155 CR213 CR212 R267 R266 CR210 CR211 CR153 CR152 R214 R213 CR150 CR151

E72 E51 E57 E64

P4 14 P4 1 P1 2 P1 3 P4 13 P4 12 P1 1 P1 14 P4 9 P4 8 P1 6 P1 7 P4 10 P4 11 P1 5 P1 4

E71 E49 E65 E47 E74 E50 E70 E48

(TP) CURRENT

Y READ SOURCE

Y WRITE RETURN

Y WRITE SOURCE

Y READ RETURN

CR176 CR175 CR185 CR182 CR179 CR181 CR186 CR189 CR168 CR167 CR193 CR190 CR177 CR172 CR194 CR197

CR174 CR183 CR178 CR180 CR184 CR187 CR188 CR169 CR166 CR191 CR173 CR196 CR192 CR170 CR195

E55 E66

B46 +V MEM

R224 R223 3300 Q44 2N4123 R246 Q52 R247 R221 Q43 R222 R244 Q51 R245 R227 Q46 R228 R250 Q54 R251 R225 Q45 R226 R248 Q53 R249 330

R240 39 R241 470 R239 +5V

470 R238 +5V

READ 1B

WRITE MEM

READ 1C

220 560 Pf

E60

E56

YRR0 YRR1 YRR2 YRR3 YRR4 YRR5 YRR6 YRR7

E62

$\overline{YRS}$

$\overline{MEM\ ENABLE}$ 2 D

MA 4 (1) 1 C

MA 5 (1) 14 B

MA 6 (1) 15 A

70 60 50 40 30 20 10 00

5 4 3 9 10 11 12 13

E61

$\overline{YRR}$

$\overline{MEM\ ENABLE}$ 2 D

MA 7 (1) 1 C

MA 8 (1) 14 B

MA 9 (1) 15 A

7 6 5 4 3 2 1 0

5 4 3 9 10 11 12 13

UNLESS SHOWN OTHERWISE:—
RESISTORS ARE ¼ W 5%
DIODE = FDH600
D.I.P. DIODE = 100000001

QTY	DESCRIPTION	PART NO.

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010

UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES

MATERIAL

FINISH

DRAWN	CHET JOHNSON	10/5/69
CHECKED		
ENGINEER	g.D.S.	5/27/70
APPROVED		

FIRST USED ON SUPERNOVA

SHEET 5 OF 5

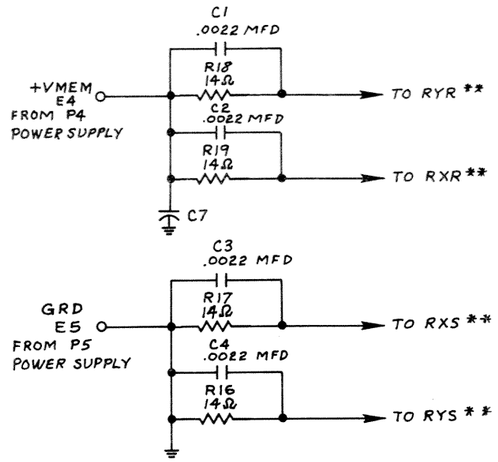
DATA GENERAL CORPORATION

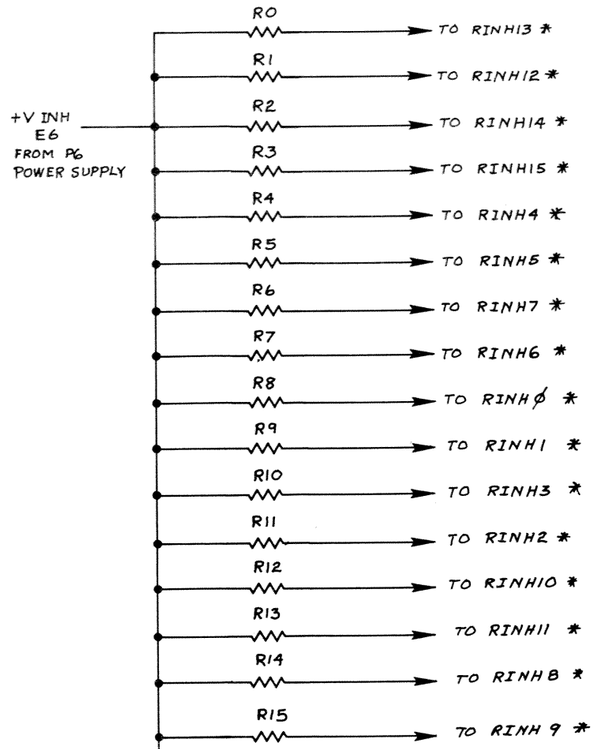
TITLE

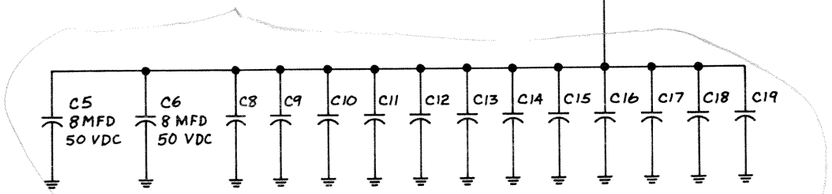
4K MEMORY
Y SELECTORS

SIZE	CODE	DRAWING NUMBER	REV
D	001	000029	00

REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP. BY	DATE







** SEE D.G. DRAWING NO. 001000029 (SHEET 1), 4K MEMORY FLIPPERS.

* SEE DG. DRAWING NO. 001000029 (SHEET 3), 4K MEMORY SENSE AND INHIBIT.

NOTE: ALL RESISTORS ARE 11.0Ω, 1% UNLESS SPECIFIED OTHERWISE
ALL CAPACITORS ARE 50 MFD, 50 VDC UNLESS SPECIFIED OTHERWISE

Replaced Aug, 1977

QTY.	DESCRIPTION	PART NO.

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
PARTS TO BE FREE FROM BURRS
BREAK ALL EDGES .010

UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES ✓

MATERIAL

FINISH

DRAWN	W. Beckett	
CHECKED	J. Sutter	12/15/77
ENGINEER		
APPROVED		
FIRST USED ON		
SCALE		

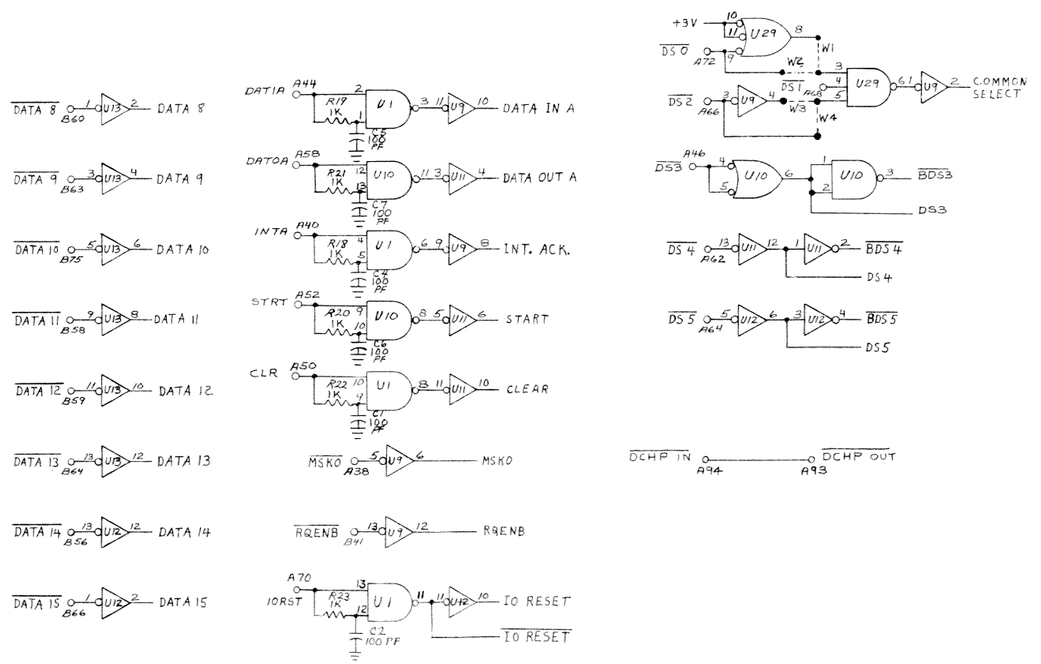
DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

TITLE
SUPERNOVA
RESISTOR BOARD
SCHEMATIC

SIZE	CODE	DRAWING NUMBER	REV.
C	001	000101	00

SHEET OF

REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



NOTE: CAPACITORS C11, C15, C27, & C30 ARE .05 MFD. CAPACITORS C13 & C26 ARE 0.8 MFD. THESE CAPACITORS ARE USED AS FILTERS AND AS SUCH ARE NOT SHOWN ON THIS DRAWING

QTY.	DESCRIPTION	PART NO.

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±
PARTS TO BE FREE FROM BURRS
BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES
MATERIAL
FINISH

DRAWN
CHECKED
ENGINEER
APPROVED
FIRST USED ON
SHEET OF

DATA GENERAL CORPORATION

TITLE
IO BUS RECEIVERS & COMMON SELECT

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000070	01

REVISIONS				
REV.	DESCRIPTION	DRFTG	APP BY	DATE

TTI START (0)
INLINE (0)
SYNC 1 (0)
INPUT CLOCK
TTI RUN
TTI START
SPIKE DET.
ILU (1)
IO RESET
+V MEM
B40
R50 470 Ω 2W
B69
C39 1 MFd.
-5V
CANNON DEC-95
R49 4.7K
Q10 2N4123
CR5 600
R48 3K
+5V
TTI START (0)
TTI RUN (0)
SYNC 0 (0)
SYNC 2
SYNC 1
SYNC 0
U49
U37
+3V
TTI RUN (1)
TTI START (0)
ILU (1)
DATA 8 A60
DATA 9 A63
DATA 10 A62
DATA 11 A58
DATA 12 A59
DATA 13 A64
DATA 14 A56
DATA 15 A66
O.C. U19
O.C. U21
TTI DATI
U 20
U 40
TTI0(1) TTI1(1) TTI2(1) TTI3(1)
TTI4(1) TTI5(1) TTI6(1) TTI7(1)
TTI3(0)
SPIKE DET(0)
READER START
READER RUN
READER STOP
SYNC 0 (1)
W9
W8
TTI3 (0)
OCH U35
C8 .01 MFD
A89
CANNON DEC-95
TTI RUN (0)
BREAK DET U5
IN LINE (0)
SPIKE DET (1)
U6
U7
TT RESET
SYNC 0 (1)
ILU
10PLS
R33 1K
R74
C9 100 PF
DATA 12
DATA 13
DATA 14
DATA 15
TTI SELECT
OC U4
C11 100 PF
R41 1K
R42
DAT1B
R11 4.7K
R10 3K
R15 3K
R14 3K
Q3 2N4123
Q5 2N4123
Q4 2N4123
CR3 600
CR2 600
CR1 600
R13 4.7K
R12 4.7K
CARRIER DETECTOR B52
DATA SET READY B54
RING INDICATOR B53
OPTION 4029
TTO0 (1)
TTO1 (1)
TTO2 (1)
TTO3 (1)
TTO4 (1)
TTO5 (1)
TTO6 (1)
TTO7 (1)
U36
U38
STOP1 (1)
START (1)
U16
TTO FINISH
OUTPUT CLOCK
U25
DATA OUT A
TTO SELECT
TTO BUSY (0)
U46
U47
STOP1 (1)
START+CLR+RST
U44
TTO BUSY (1)
U 15
U 14
U34
J STOP2 STOP1(1) TTO0(1) TTO1(1)
J TTO2(1) TTO3(1) TTO4(1) TTO5(1)
J TTO6(1) TTO7(1) START(1) LINE(1)
MR CP PE K
IO RESET
LINE (0)
+3V
+5V
P30 3K
P32 3K
P31 3K
A87
Q9
CANNON DEC-95
U 33
DATA 10
DATA 11
DATA 12
DATA 13
DATA 14
DATA 15
Y2 14.08 KC
C10 470 PF
R37 3.3K
R38 3.3K
R39 3.3K
R40 3.3K
R34 3.3K
U2
2N4125
R36 180
R35 220
+V MEM
R5 1K
A83
W7
A85
W6
C31 .01 MFD
CANNON DEC-95
INPUT CLOCK
U3
U22
OUTPUT CLOCK
OPTION 4023
R44 750
R45 1.5K
Q8 2N4125
R39 110
R28 1K
-5V
TTO BUSY (1)
R42 3K
R17 3K
Q6 2N4123
CR4 600
R16 4.7K
CLEAR TO SEND B81
OPTION 4029
RQENB
TTO INT. DISABLE (0)
TTO DONE (1)
U43
TTO INT. REQ
TTI INT. REQ
TTI INT. DISABLE (0)
TTI DONE (1)
INTR B29
DATA 8
DATA 9
MSK0
U42
TTO INT DISABLE
TTI INT DISABLE
DATA 15
DATA 14
TT RESET
DATA OB
R56
R43 1K
C12 100 PF
R8 750
R9 1.5K
Q2 2N4125
DATA TERMINAL READY A79
R4 110
R3 1K
TTI DONE (1)
SELD A80
TTO DONE (1)
TTO BUSY (1)
SELB A82
TTI SELECT
TT RDR BUSY (1)
BDS 3
BDS 4
BDS 5
COMMON SELECT
DATA IN A
TTI DATI
U39
U37
U38
U45
U41
TTO DONE
TTO BUSY
U23
TTI DONE
TT RDR BUSY
START
CLEAR
TTO SELECT
TTO FINISH
SPIKE DET (0)
ILU (0)
READER START
READER STOP
OPTION 4029
R6 750
R7 1.5K
Q1 2N4125
-5V
R1 1K
R2 110
C3 820 PF
REQUEST TO SEND A78
TTO DONE (0)
TTO BUSY (0)
INT ACK
TTO INT REQ (1)
TTO ACK
DATA 15

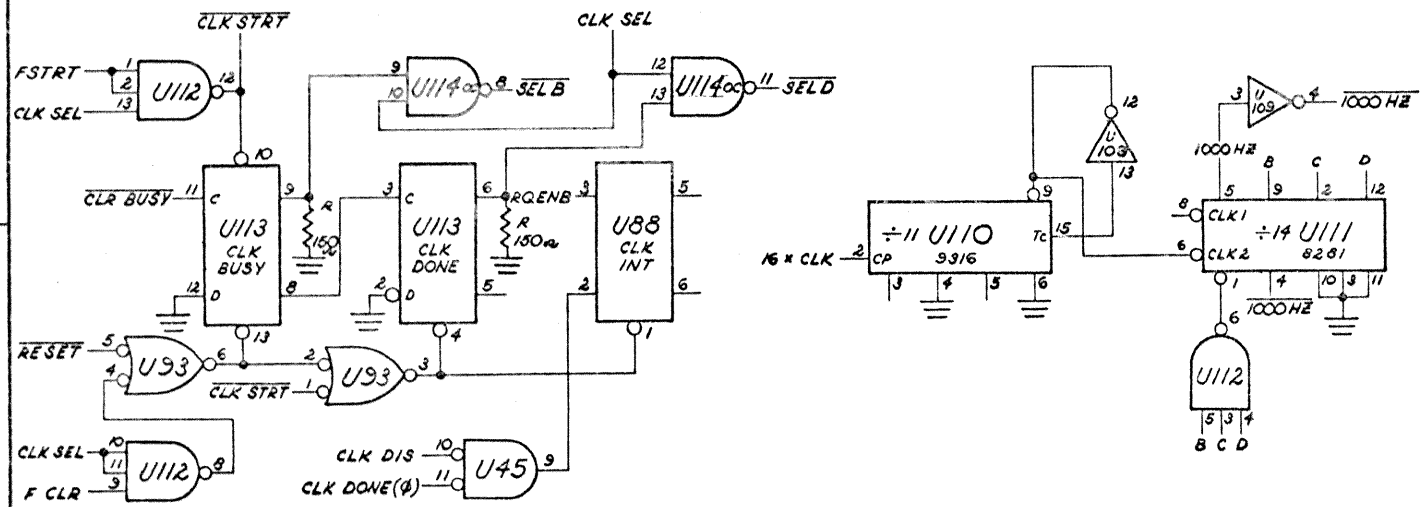
NOTE: CAPACITORS C16, C17, C18 C19, C21, C22, C23, C24 C32, C34, C35, C36, & C38 ARE .05 MFD. CAPACITORS C20, C25 & C40 ARE 6.8 MFD. THESE CAPACITORS ARE USED AS FILTERS AND AS SUCH ARE NOT SHOWN.

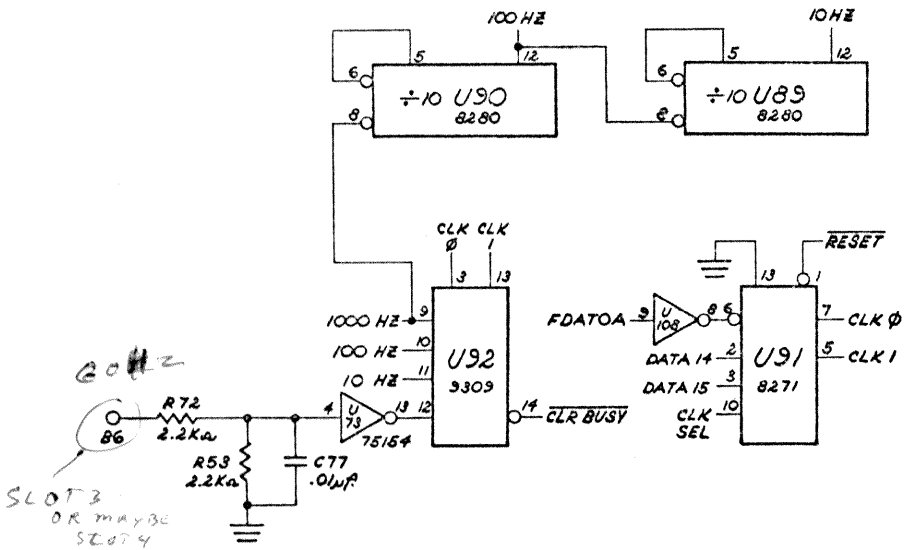
* CRYSTAL FREQUENCY OF Y2 DEPENDS ON BAUD RATE SPECIFIED BY THE CUSTOMER. (FREQ Y2 = 128 X BAUD RATE)

QTY.	DESCRIPTION	PART NO.
DRAWN		DATA GENERAL CORPORATION
CHECKED		
ENGINEER		TITLE: TELETYPE CONTROL
APPROVED		
FIRST USED ON		
SHEET OF		SIZE D · CODE 001 · DRAWING NUMBER 000071 · REV 01

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES XX ± ± XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES
MATERIAL
FINISH

REVISIONS			
REV.	DESCRIPTION	DRFTG.	APP.
01	ECO# 1371	R.W.C.	
02	ECO# 1494	R.W.C.	





QTY	DESCRIPTION	PART

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
± .XX ± ±
± .XXX ± ±
PARTS TO BE FREE FROM BURRS
BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES
MATERIAL

DRAWN	R.W.C, Jr.	11-13-72
CHECKED	R.W.C, Jr.	11-16-72
ENGINEER		11/72
APPROVED		
FIRST USED ON		

DATA GENERAL CORPOR
SOUTHBORO, MASSACHUSETTS

TITLE

REAL TIME CLOCK C
(MODEL NO. 40

REVISIONS				
REV.	DESCRIPTION	DRFTG	APP BY	DATE
01	ECO 028	PNK		10/14/76
02	ECO 439	WJG.		8/18/77

DCHAF
DATA OUT
DATA IN
HSCI
CPU CLK
IO RST
RESTORE MEM
MODE 1
MODE 1·SLOW
INH DCHOF
DCHOF
HSC BUSY
HSC INH
HSC START
HSC PEND
RQ INH
RQENB
RQENBF
WAIT
EXEC
FETCH
DEFER
EXEC+DCH2
IO INH
IO RIS SET
HSC LD RQ
WHOA
SET HSC4
HSC4
HSTG1
HSTG2
HSTG3
HSTG6
OVFLOF
CLR HSCO
INC OUTPUT
DCHR SYNC
RQENB SYNC
DCHP
DCHR SYNC
INPUT
OUTPUT
DATA OUT
DATA IN
IORST
JORST
SLOW
MBO0 MBO1 MBO2 MBO3 MBO4 MBO5 MBO6 MBO7 MBO8 MBO9 MBO10 MBO11 MBO12 MBO13 MBO14 MBO15
IT0 IT1 IT2 IT3 IT4 IT5 IT6 IT7
MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 MEM8 MEM9 MEM10 MEM11 MEM12 MEM13 MEM14 MEM15
U 31 U 33 U 50 U 46 U 29 U 48 U 44 U 27 U 67 U 66 U 63 U 60
SN7475
8260
8271
PT63 PT63B
A69
100pf
1K
10K
180Ω
470Ω
.05
.05μF 31 EACH
6.8μF 35VDC 8 EACH
+5V
+3V
CONNECTED FOR NORMAL OPERATION.
A94 A96

QTY	DESCRIPTION	PART NO.
DRAWN		
CHECKED		
ENGINEER		10/7/41
APPROVED		
FIRST USED ON	SUPERNOVA 107-000062	

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES XX ± ± XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES
MATERIAL
FINISH

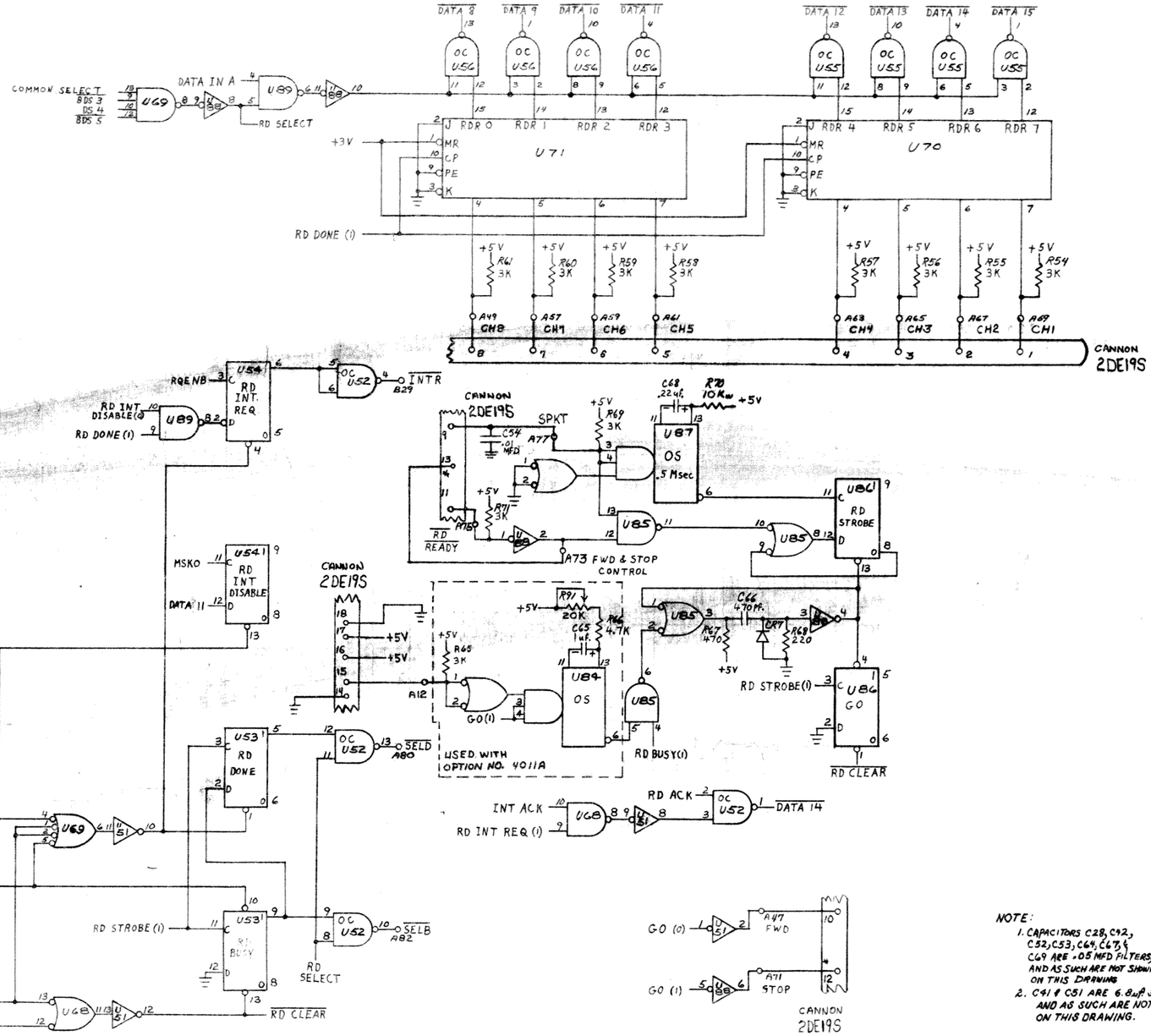
DATA GENERAL CORPORATION

TITLE
HIGH SPEED CHANNEL

SIZE	CODE	DRAWING NUMBER	REV
D	001	000075	02

SHEET 1 OF 1

REVISIONS				
REV	DESCRIPTION	DRFTG.	APP. BY	DATE
03	ECO # 1477	R.W.C.		3-26-74
04	ECO # 2377	R.W.C.		4-12-74
05	ECO # 2465	R.W.C.		4-18-74



NOTE:
1. CAPACITORS C28, C42, C52, C53, C64, C67, & C69 ARE .05 MFD FILTERS, AND AS SUCH ARE NOT SHOWN ON THIS DRAWING
2. C41 & C51 ARE 6.8μF 35V. FILTERS AND AS SUCH ARE NOT SHOWN ON THIS DRAWING.

NOTE
* USED WITH OPTION NO. 4011B

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±
PARTS TO BE FREE FROM BURRS
BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES
MATERIAL
FINISH

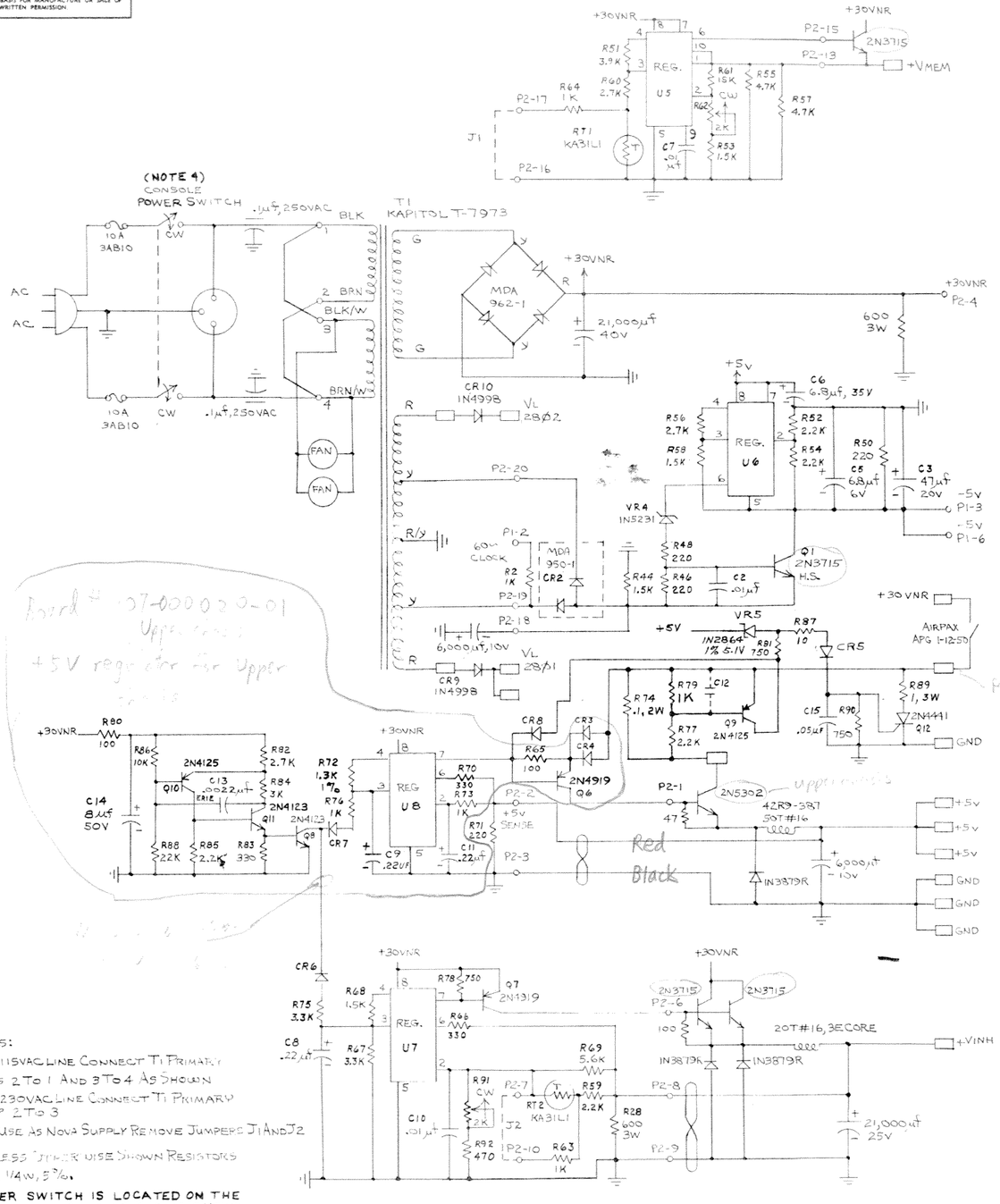
QTY.	DESCRIPTION	PART NO
DRAWN		
CHECKED		
ENGINEER		
APPROVED		
FIRST USED ON		
SHEET OF		

DATA GENERAL CORPORATION

TITLE
PAPER TAPE READER CONTROL 4011

SIZE	CODE	DRAWING NUMBER	REV
D	001	000072	05

REVISIONS			
REV	DESCRIPTION	DRFTG	APP
01	ECO # 019	[illegible]	[illegible]
02	ECO # 032+033	[illegible]	[illegible]
03	ECO # 061	RNK	[illegible]
04	ECO # 103	[illegible]	[illegible]
05	ECO # 121+127	[illegible]	[illegible]



Board # 07-000020-01
Upper
+5V regulator for Upper

Red
Black

Bt Red
BL-Blu
Blu-BL

R
O
G
R

NOTES:
1. FOR 115VAC LINE CONNECT T1 PRIMARY TAPS 2 TO 1 AND 3 TO 4 AS SHOWN
   FOR 230VAC LINE CONNECT T1 PRIMARY TAP 2 TO 3
2. FOR USE AS NOVA SUPPLY REMOVE JUMPERS J1 AND J2
3. UNLESS OTHER WISE SHOWN RESISTORS ARE 1/4W, 5%.
4. POWER SWITCH IS LOCATED ON THE SUPERNOVA CONSOLE AND IS SHOWN HERE FOR INFORMATION PURPOSES

QTY.	DESCRIPTION	PART NO.
DRAWN		
CHECKED		
ENGINEER	[illegible]	5/19/78
APPROVED	[illegible]	
FIRST USED ON		
SCALE		

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES XX ± ± XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES ✓
MATERIAL
FINISH

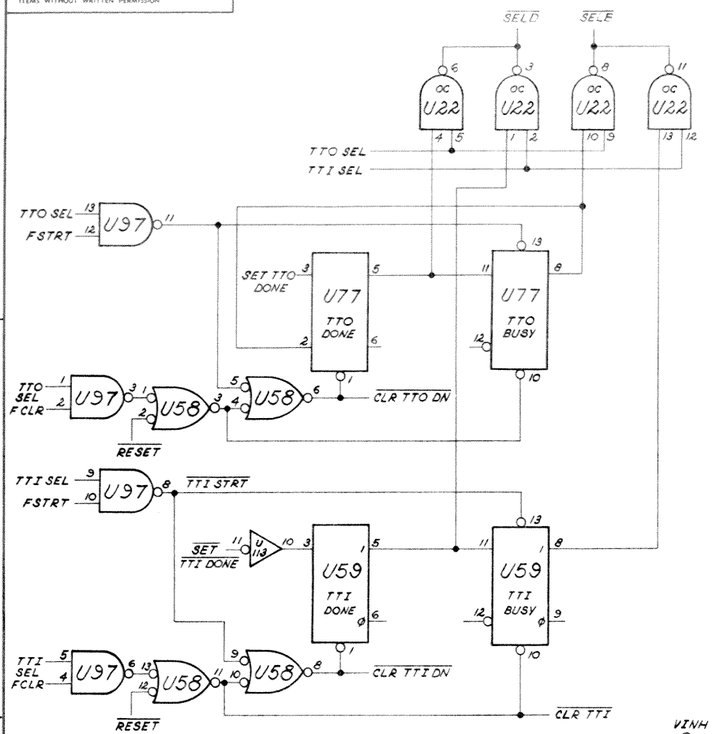
DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

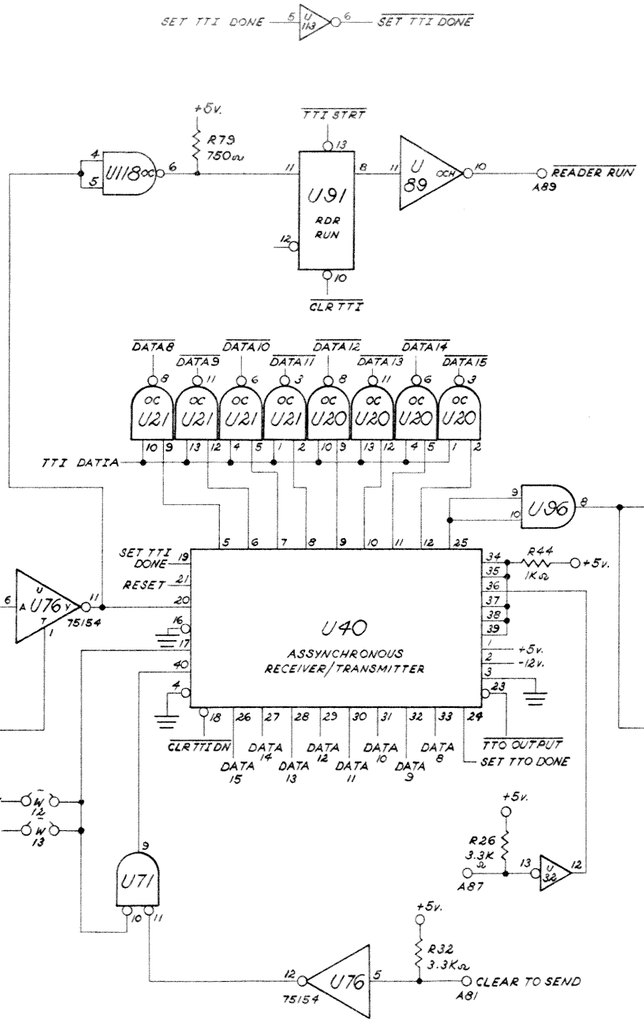
TITLE
SUPERNOVA POWER SUPPLY

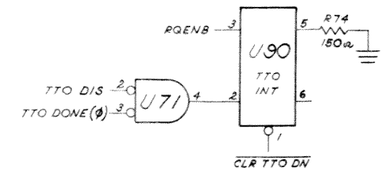
SIZE	CODE	DRAWING NUMBER	REV.
D	001	000063	05

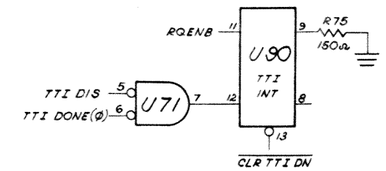
SHEET 1 OF 1

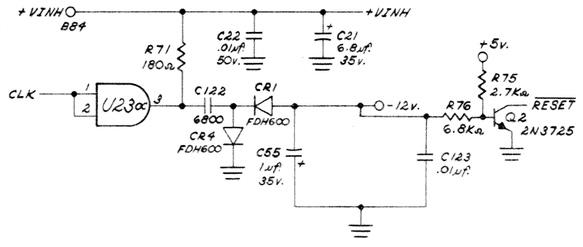
REVISIONS				
REV	DESCRIPTION	DRFTG	APP. BY	DATE
01	ECO # 1371	R.W.C.		2-20-73
02	ECO # 1464	R.W.C.		5-14-73
03	ECO # 1533	R.W.C.		6-7-73
04	ECO # 1876	R.W.C.		9-10-73
05	ECO # 1837	R.W.C.		12-31-73
06	ECO # 2419	R.W.C.		4-26-74
07	ECO # 2493	R.W.C.		5-9-74

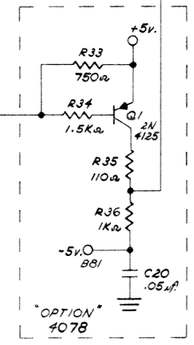


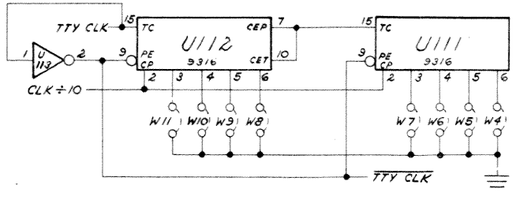












NOTES:

1. FOR THE 4078 OPTION, ADD CIRCUITRY IN DESIGNATED AREA & DELETE COMPONENTS W1, W2, R30 & C18 FROM CIRCUITRY.
2. ON THE 75154 TYPE I.C. PACK VCC CONNECTS TO PIN 15, NO CONNECTION TO PIN 16.
3. W5, W6, W9 & W11, ARE USED FOR STANDARD TTY.
4. REMOVE C18 1μf. CAP FOR ANY DEVICES OPERATING ABOVE 1200 BAUD.

ARTWORK: 107 000 151	
ARTWORK VS SCHEMATIC	
REV	SCHEMATIC REV(s)
1	0
2	0
5	1, 2, 3, 4
10	1, 2, 3, 4
13	5
16	6,7

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± XX ± ± XXX ± ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010

UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES

MATERIAL

FINISH

QTY.	DESCRIPTION	PART NO.
DRAWN	R.W.C, Jr.	11-1-72
CHECKED	R.W.C, Jr.	11-1-72
ENGINEER		11/72
APPROVED		
FIRST USED ON	4077/4078	
SCALE		

DATA GENERAL CORPORATION
SOUTHBORO, MASSACHUSETTS 01772

TITLE
TELETYPE OPTION
(MODEL NO'S 4077 & 4078)

SIZE	CODE	DRAWING NUMBER	REV.
D	001	000334	07

SHEET 1 OF 1

REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE
01	PER ECO # 1282	R.W.C.		12-13-72
02	PER ECO # 1463	R.W.C.		5-7-73
03	PER ECO # 1640	R.W.C.		5-7-74
04	PER ECO # 1837	R.W.C.		1-17-74
05	PER ECO # 2419	R.W.C.		4-16-74
06	PER ECO # 2757	RFU	JPB	8-1-74

IORST A70 — R10 1KΩ — C12 100pf — U7 — RESET

CLR A50 — R4 1KΩ — C6 100pf — U5 — F CLR

STRT A52 — R5 1KΩ — C7 100pf — U6 — FSTRT

DATOA A58 — R7 1KΩ — C9 100pf — C36 330pf — R78 150Ω — U6 — FDATOA

DATOB A56 — R6 1KΩ — C8 100pf — U6 — FDATOB

DATOC A48 — R3 1KΩ — C5 100pf — U5 — FDATOC

DATIA A44 — R2 1KΩ — C4 100pf — U5 — FDATIA

DATIB A42 — R1 1KΩ — C3 100pf — U5 — FDATIB

INTA A40 — R8 1KΩ — C10 100pf — U6 — FINTA

F CLR, FSTRT, FDATOA, FDATOB, FDATOC, FDATIA, FDATIB, FINTA → U27, U28

U7 (RESET, CLEAR) → U29 → CLEAR

U30 (CLEAR, CLEAR ALL) → U29 → CLEAR ALL

U28 (CAS STRT) → U29 → CAS STRT

U28 → CAS DATOA, CAS DATOB, CAS DATOC, CAS DATIA, CAS DATIB, CAS INTA

CAS SEL

DATA Ø B62 → U16 → DATA Ø

DATA 1 B65 → U16 → DATA 1

DATA 2 B62 → U16 → DATA 2

DATA 3 B73 → U16 → DATA 3

DATA 4 B61 → U16 → DATA 4

DATA 5 B57 → U16 → DATA 5

DATA 6 B35 → U16 → DATA 6

DATA 7 B55 → U16 → DATA 7

DATA 8 B60 → U16 → DATA 8

DATA 9 B63 → U16 → DATA 9

DATA 10 B75 → U16 → DATA 10

DATA 11 B58 → U16 → DATA 11

DATA 12 B59 → U16 → DATA 12

DATA 13 B64 → U16 → DATA 13

DATA 14 B56 → U16 → DATA 14

DATA 15 B66 → U16 → DATA 15

INTP IN → U14 → INTP OUT → U104 → CAS INTA

CAS INT REQ (1) → U49 → U330C → DATA 10, DATA 11, DATA 12, DATA 13

CLK ENB, CAS INTA → U10 → U49 → U112C → DATA 15

TTO ENB → U150C → DATA 10

TT ENB

DS4 A62, DS2 A66 → U1 → U7 → COM SEL

DS1 A68 → U1 → U26 → TT4 RTC COM

DS3 → U4 → U25 → TTO SEL

DS5 → U25 → TTI SEL

DSØ A72 → U1 → U1 → W16 → DSØ

BDSØ → W17

TT+RTC COM, BDSØ, DS3 → U4 → U26 → CLK SEL

DS5 A64 → U11

COM SEL, TT+RTC COM → U8 → U4 → U26 → CAS SEL

DS3 → U3 → DS5

DSØ → W18

BDSØ → W19

FOR LOW ORDER CASSETTE

R78 150Ω

+5V. R27 330Ω, R21 390Ω

INTP IN A96 → U10 → U49 → U31 → U11 → INTP OUT A95

TTI INT, TTO INT, CLK INT

TTO ENB, CLK ENB

U1 → TT ENB

CAS INT REQ (1), CLK INT, TTI INT, TTO INT → U71 → U14 → INTR B29

1.54 MHZ → C113 470Ω → U88 → C114 6800 → U88 → CLK

R67 470Ω, R68 470Ω

COUNT CLK, CLK ÷ 10 → U110 (÷ 10)

RESET → U53 OPTION DISABLE

TTO DIS, TTI DIS, CLK DIS, CAS DIS

LO, A38 MSKO

DATA 15, DATA 14, DATA 13, DATA 10

RQ ENB B41 → R9 1KΩ, C11 100pf → U7 → RQ ENB

+5V. R22 330Ω, R25 390Ω

DCHP IN A94 → U9 → DCHP IN

U30 → DCHP OUT A93, CAS DCH REQ (Ø)

SELB → A82

SELC → A80

ARTWORK: 107 000 151	
ARTWORK VS SCHEMATIC	
REV	SCHEMATIC REV(S)
-	0
-	2
-	1, 2, 3
10	1, 2, 3
13	4
16	5
17	6

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS ± DECIMALS ANGLES .XX ± .XXX ± PARTS TO BE FREE FROM BURRS, BREAK ALL SHARP EDGES. MATERIAL FINISH

QTY	DESCRIPTION	PART NO.
DRAWN	R. W. C, JR. 11-16-72	
CHECKED	R. W. C, JR. 11-16-72	
ENGINEER		
APPROVED		
FIRST USED ON		
SCALE		

DATA GENERAL CORPORATION
SOUTHBORO MASSACHUSETTS 01772

TITLE
CASSETTE BASIC OPTION
(MODEL NO. 4075)

SIZE	CODE	DRAWING NUMBER	REV
D	001	000336	C6

SHEET 1 OF 1

REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

Slots: 4K MEM OR I/O 7; 4K MEM OR I/O 6; 4K MEM OR I/O 5; 4K MEM OR I/O 4K 4; CPU 3; CPU 2; CPU 1

A — ODD

Pin	4K MEM OR I/O 7	4K MEM OR I/O 6	4K MEM OR I/O 5	4K MEM OR I/O 4	CPU 3	CPU 2	CPU 1
1	GND	GND	GND	GND	GND	GND	GND
3	+5V	+5V	+5V	+5V	+5V	+5V	+5V
5	RINH 0	RINH 0	RINH 0	RINH 0	AC115	AC115	MEM OK
7	RINH 1	RINH 1	RINH 1	RINH 1	ALC SKIP ENAB	ALC SKIP ENAB	RQ INH
9	RINH 2	RINH 2	RINH 2	RINH 2	EITGI	EITGI	+5 OK
11	RINH 3	RINH 3	RINH 3	RINH 3	SEL Y	SELY	
13	RINH 4	RINH 4	RINH 4	RINH 4	ENAB CARRY	ENAB CARRY	
15	RINH 5	RINH 5	RINH 5	RINH 5	IR8	IR8	IR8
17	RINH 7	RINH 7	RINH 7	RINH 7	CARRY SET	CARRY SET	DCHP
19	RINH 8	RINH 8	RINH 8	RINH 8	ACO OUT	ACO OUT	
21	RINH 11	RINH 11	RINH 11	RINH 11	EFA	EFA	HSC LD RQ
23	RINH 10	RINH 10	RINH 10	RINH 10	DIV LD	DIV LD	RQENBF
25	RINH 13	RINH 13	RINH 13	RINH 13	CON OUT	CON OUT	DCHIF
27	RINH 15	RINH 15	RINH 15	RINH 15	ENAB RIGHT LSB LEFT COMP	ENAB RIGHT LSB LEFT COMP	OVFLOF
29	RINH 14	RINH 14	RINH 14	RINH 14	DIV COMP	DIV COMP	DCHOF
31	INH GND	INH GND	INH GND	INH GND	SX-L-L-S	SX-L-L-S	DCHAF
33	GND	GND	GND	GND	GND	GND	GND
35	MEM 13	MEM 13	MEM 13	MEM 13	MEM 13	MEM 13	MEM 13
37	MBO13	MBO13	MBO13	MBO13	MBO13	ACC1	
39	MBO12	MBO12	MBO12	MBO12	MBO12	ACCO	PTG5
41	MBO15	MBO15	MBO15	MBO15	MBO15	ACC3	DATOC
43	MBO14	MBO14	MBO14	MBO14	MBO14	ENAB ACO RIGHT MSB COMP	PL READ10
45	MEM 10	MEM 10	MEM 10	MEM 10	MEM 10	MEM 10	MEM 10
47					PC CLK		PC CLK
49					ACCØ + ACCØ	ACCØ + ACCØ	GND
51	MEM 11	MEM 11	MEM 11	MEM 11	MEM 11	MEM 11	MEM 11
53	MEM 9	MEM 9	MEM 9	MEM 9	MEM 9	MEM 9	DCH INC
55	MEM 8	MEM 8	MEM 8	MEM 8	MEM 8	MEM 8	EXV STRT
57					ACS COMP ENAB	ACS COMP ENAB	CHST
59					ACD1 + ACC1	ACD1 + ACC1	HSC BUSY
61					AC LOAD ENAB	AC LOAD ENAB	HSC PEND
63					IO IN	AC3 OUT	IO N
65					MA OUT	MA OUT 65	DCH2
67					EIS MA OUT	EIS MA OUT 69	TS3
69					MEM OUT	MEM OUT	EXU EXN DPU DPN
71					CON 15		CON 15
73					CON 14		CON 14
75					CON 12		CON 12
77					CON 13		PTGØ
79					IND 15		IO IN
81					IND 14		CODE 77
83					IND 13	DPN + EXN	DPN + EXN
85					IND 12	PTG3	PTG3
87					MAI2	DCH IN	DCH IN
89					ADD ONE	MAI2	OVLAP
91					CON 11	ADD ONE	CON 11
93	DCHP OUT	DCHP OUT	DCHP OUT	DCHP OUT	CON 8	PTG 5	PTG 5
95	INTP OUT	INTP OUT	INTP OUT	INTP OUT	IND11	CRY SAVE	CRY SAVE
97	+5V	+5V	+5V	+5V	+5V	+5V	+5V
99	GND	GND	GND	GND	GND	GND	GND

A — EVEN

Pin	4K MEM OR I/O 7	4K MEM OR I/O 6	4K MEM OR I/O 5	4K MEM OR I/O 4	CPU 3	CPU 2	CPU 1
2	GND	GND	GND	GND	GND	GND	GND
4	+5V	+5V	+5V	+5V	+5V	+5V	+5V
6	-5V	-5V	-5V	-5V	-5V		PWR FAIL
8	INH GND	INH GND	INH GND	INH GND	MUL 4	MUL 4	ION SYNC
10	+VINH	+VINH	+VINH	+VINH	IR9	IR9	IR9
12					ACI14	ACI14	
14	INH GND	INH GND	INH GND	INH GND	SHIFT ACØ	SHIFT ACØ	
16	INH GND	INH GND	INH GND	INH GND	SHIFT MA	SHIFT MA	
18	RINH 6	RINH 6	RINH 6	RINH 6	DIV SHIFT	DIV SHIFT	
20	INH GND	INH GND	INH GND	INH GND	DIV·FETCH·PTG4	DIV FETCH PTG4	
22	INH GND	INH GND	INH GND	INH GND	CRY OUT	CRY OUT	
24	RINH 9	RINH 9	RINH 9	RINH 9	PREV·CRY	PREV CRY	
26	INH GND	INH GND	INH GND	INH GND	SELX	SELX	
28	RINH 12	RINH 12	RINH 12	RINH 12	EIS LD	EISLOAD	
30	INH GND	INH GND	INH GND	INH GND	SX-L-H-S	SX-L-H-S	IO RLS SET
32						ACC2	EXTION ENAB
34	GND	GND	GND	GND	GND	READS	READS
36	MEM 12	MEM 12	MEM 12	MEM 12	MEM 12	MEM 12	MEM 12
38	MSKO	MSKO	MSKO	MSKO	EXEC DIV TSØ	EXEC DIV TSØ	MSKO
40	INTA	INTA	INTA	INTA	PTG5	PTG5	INTA
42	DATIB	DATIB	DATIB	DATIB	AC3 ENAB	AC3E NAB	DATIB
44	DATIA	DATIA	DATIA	DATIA	ENAB ACØ RIGHT MSB COMP	PL READ 10	DATIA
46	DS3	DS3	DS3	DS3	MAI5	MAI5	DS3
48	DATOC	DATOC	DATOC	DATOC	CPU CLK	CPU CLK	CPU CLK
50	CLR	CLR	CLR	CLR	GND	GND	CLR
52	STRT	STRT	STRT	STRT			STRT
54	DATIC	DATIC	DATIC	DATIC		DCH INC	DATIC
56	DATOB	DATOB	DATOB	DATOB		EXV STRT	DATOB
58	DATOA	DATOA	DATOA	DATOA		CHST	DATOA
60	DCHA	DCHA	DCHA	DCHA	EIS OUTPUT	EIS OUTPUT	DCHA
62	DS4	DS4	DS4	DS4	ACD2 + ACC2	ACD2 + ACC2	DS4
64	DS5	DS5	DS5	DS5	AC3 OUT	DCH2	DS5
66	DS2	DS2	DS2	DS2	ALC + KEY 2 ACEX	ALC + KEY 2 ACEX 66	DS2
68	DS1	DS1	DS1	DS1		TS3	DS1
70	IORST	IORST	IORST	IORST		EXV EXNV DPU DPN	IORST
72	DS0	DS0	DS0	DS0			DS0
74	IOPLS	IOPLS	IOPLS	IOPLS			IOPLS
76						DP + DPN	DP + DPN
78						PTGØ	CON 13
80	SELD	SELD	SELD	SELD		IO IN	SELD
82	SELB	SELB	SELB	SELB		CODE 77	SELB
84						PL	PL
86						DEFER MEM MOD	DEFER MEM MOD
88					MAI2	IO SKIP	IO SKIP
90					INC PC	MAI2	
92					CON 10	INC PC	CON 10
94	DCHP IN	DCHP IN	DCHP IN	DCHP IN	CON 9	IO OUT ENAB	IO OUT ENAB
96	INTP IN	INTP IN	INTP IN	INTP IN	INDØ	TSO	TSO
98	+5V	+5V	+5V	+5V	+5V	+5V	+5V
100	GND	GND	GND	GND	GND	GND	GND

A

B — ODD

Pin	4K MEM OR I/O 7	4K MEM OR I/O 6	4K MEM OR I/O 5	4K MEM OR I/O 4	CPU 3	CPU 2	CPU 1
1	GND	GND	GND	GND	GND	GND	GND
3	+5V	+5V	+5V	+5V	+5V	+5V	+5V
5	MBO11	MBO11	MBO11	MBO11	MBO11	IR7	IR7
7	MA LOAD	MA LOAD	MA LOAD	MA LOAD	IND 8	IO UNPROTECTED	MA LOAD
9	MBO9	MBO9	MBO9	MBO9	MBO9	ISZ·DSZ·STA	ISZ·DSZ·STA
11					Ø2 IND DRIVE	Ø2 IND DRIVE	Ø2 IND DRIVE
13					Ø1 IND DRIVE	Ø IND DRIVE	Ø1 IND DRIVE
15					LOAD PC	LOAD PC	KEY 1 PC LD
17	DCHMO	DCHMO	DCHMO	DCHMO	CON 7		DCHMØ
19					CON 6	KEY 1 SET	KEY1 SET
21	DCHMI	DCHMI	DCHMI	DCHMI	CON 4	MEM 6	DCHMI
23					CON 5	MEM 7	IR6
25						MEM 5	IR5
27						MEM 4	PTG4
29	INTR	INTR	INTR	INTR	GND	GND	INTR
31					IND 6	MEM CY SET	MEMCYSET
33	DCHO	DCHO	DCHO	DCHO		EIS PRI	DCHO
35	DCHR	DCHR	DCHR	DCHR	IND 5	IRINDØ	DCHR
37	DCHI	DCHI	DCHI	DCHI	IND 4		DCHI
39	OV FLO	OV FLO	OV FLO	OV FLO	GND	GND	OV FLO
41	RQENB	RQENB	RQENB	RQENB			RQENB
43	MBO3	MBO3	MBO3	MBO3	MBO5	IRIND1	PI2
45	INHIBIT TRANSMISSION	INHIBIT TRANSMISSION	INHIBIT TRANSMISSION	INHIBIT TRANSMISSION		IRIND3	TS3
47	MEM 2	MEM 2	MEM 2	MEM 2	MEM 2	MEM 2	CONT+1STP+MSTP
49					IR4	IR4	GND
51					AND	AND	ISTP
53					CON 3	PROT IND	
55	DATA 7	DATA 7	DATA 7	DATA 7	DATA 7	ION	ION
57	DATA 5	DATA 5	DATA 5	DATA 5	DATA 5	PTG2	PTG2
59	DATA 12	DATA 12	DATA 12	DATA 12	DATA 12	FETCH IND	DP
61	DATA 4	DATA 4	DATA 4	DATA 4	DATA 4		KEY 2 SET
63	DATA 9	DATA 9	DATA 9	DATA 9	DATA 9	DCH IND	KEY 1
65	DATA 1	DATA 1	DATA 1	DATA 1	DATA 1		OVLAP LD MA
67					CON 2	F SET	F SET
69					CONØ	EXEC	EXEC
71	MEMØ	MEMØ	MEMØ	MEMØ	MEMØ	MEMØ	MEMØ
73	DATA 3	DATA 3	DATA 3	DATA 3	DATA 3	PC OUT	RELOAD DISABLE
75	DATA 10	DATA 10	DATA 10	DATA 10	DATA 10	EIS RQ	EIS RQ
77	MBO1	MBO1	MBO1	MBO1	MBO1	PRESET	PRESET
79	MBOØ	MBOØ	MBOØ	MBOØ	MBOØ	FETCH	FETCH
81	-5V	-5V	-5V	-5V	-5V		INT PEND
83					ADDER OUT	ADDER OUT	CPU CLK
85	INHIBIT SELECT	INHIBIT SELECT	INHIBIT SELECT	INHIBIT SELECT	IND1	MBO INH	DCH PEND
87	READ 1	READ 1	READ 1	READ 1	INDØ	CARRY	PL CYCLE
89	GND	GND	GND	GND	MA ZERO BUS	MA ZERO BUS	MA ZERO BUS
91	RXR	RXR	RXR	RXR	LOAD MA	LOAD MA	READ 2
93	RYS	RYS	RYS	RYS	PC CLK		PC CLK
95	DATA 6	DATA 6	DATA 6	DATA 6	DATA 6	ACDP	ACDP
97	+5V	+5V	+5V	+5V	+5V	+5V	+5V
99	GND	GND	GND	GND	GND	GND	GND

B — EVEN

Pin	4K MEM OR I/O 7	4K MEM OR I/O 6	4K MEM OR I/O 5	4K MEM OR I/O 4	CPU 3	CPU 2	CPU 1
2	GND	GND	GND	GND	GND	GND	GND
4	+5V	+5V	+5V	+5V	+5V	+5V	+5V
6					IND 9	IO	IO
8	MBO1Ø	MBO1Ø	MBO1Ø	MBO1Ø	MBO1Ø	PROTECT	HSC4
10	BMA LOAD	BMA LOAD	BMA LOAD	BMA LOAD	MAI1	MAI1	BMA LOAD
12	MBO8	MBO8	MBO8	MBO8	MBO8		Ø2 LOGICAL
14	MBO7	MBO7	MBO7	MBO7	MBO7	TSØ	TSO
16	MBO6	MBO6	MBO6	MBO6	MBO6	KEY 1 PC LD	
18	MEM 15	MEM 15	MEM 15	MEM 15	MEM 15	MEM 15	MEM 15
20	STROBE	STROBE	STROBE	STROBE	GND	GND	STROBE
22	MEM 6	MEM 6	MEM 6	MEM 6	MEM 6	C4	C4
24	MEM 7	MEM 7	MEM 7	MEM 7	MEM 7	IR6	ACC ENABLE
26	MEM 5	MEM 5	MEM 5	MEM 5	MEM 5	IR5	PLC
28	MEM 4	MEM 4	MEM 4	MEM 4	MEM 4	PTG 4	GND
30	INHIBIT (1)	INHIBIT (1)	INHIBIT (1)	INHIBIT (1)	IND 7		INHIBIT (1)
32	MBO5	MBO5	MBO5	MBO5	MBO5	KEY 2	KEY 2
34							EIS PRI
36							RESTART ENABLE
38						IO TIME	IO TIME
40						STA	GND
42	MBO4	MBO4	MBO4	MBO4	MBO4	IRIND2	
44	MBO2	MBO2	MBO2	MBO2	MBO2	PI2	
46	+V MEM	+V MEM	+V MEM	+V MEM		TS3	HSC START
48						CONT+1STP+MSTP	STA
50	GND	GND	GND	GND	GND	GND	MSTP
52					IR3	IR3	STOP
54						ALC SKIP	ALC SKIP
56	DATA 14	DATA 14	DATA 14	DATA 14	DATA 14	DCH 1	DCH 1
58	DATA 11	DATA 11	DATA 11	DATA 11	DATA 11		CONT
60	DATA 8	DATA 8	DATA 8	DATA 8	DATA 8	DEFER	CHST
62	DATA Ø	DATA Ø	DATA Ø	DATA Ø	DATA Ø	KEY 2 SET	RST
64	DATA 13	DATA 13	DATA 13	DATA 13	DATA 13	KEY 1	EX
66	DATA 15	DATA 15	DATA 15	DATA 15	DATA 15	OVLAP LD MA	STRT
68	MEM 3	MEM 3	MEM 3	MEM 3	MEM 3	MEM 3	EXN
70	MEM 1	MEM 1	MEM 1	MEM 1	MEM 1	MEM 1	DPN
72	RELOAD DISABLE	RELOAD DISABLE	RELOAD DISABLE	RELOAD DISABLE	CON 1	PI1	RUN IND
74	MB LOAD(1)	MB LOAD(1)	MB LOAD(1)	MB LOAD(1)	PC OUT		MB LOAD
76	MEM 14	MEM 14	MEM 14	MEM 14	MEM 14	MEM 14	MEM 14
78	ROS	ROS	ROS	ROS	IND 2	HSC INH	SET MC4
80	EXTERNAL SELECT	EXTERNAL SELECT	EXTERNAL SELECT	EXTERNAL SELECT	GND	GND	GND
82	DATA 2	DATA 2	DATA 2	DATA 2	DATA 2	INT PEND	ROS
84	+V INH	+V INH	+V INH	+V INH	CPU CLK	CPU CLK	WHOA
86	MB CLEAR	MB CLEAR	MB CLEAR	MB CLEAR	IND3	DCH PEND	MB CLEAR
88	WRITE 1	WRITE 1	WRITE 1	WRITE 1	CARRY	PL CYCLE	READ 1
90	READ 2	READ 2	READ 2	READ 2	IO OUT		IO OUT
92	GND	GND	GND	GND		DEFER IND	WRITE 1
94	RXS	RXS	RXS	RXS		ACEX	ACEX
96	RYR	RYR	RYR	RYR	ADDER=Φ	ADDER=Φ	ADDER=Φ
98	+5V	+5V	+5V	+5V	+5V	+5V	+5V
100	GND	GND	GND	GND	GND	GND	GND

B

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ± PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010	QTY.	DESCRIPTION	PART NO.
UNLESS OTHERWISE SPECIFIED - ALL MACH. SURFACES	DRAWN R. DelVecchio 3/13/70	DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772	
MATERIAL	CHECKED	TITLE BACK PANEL SUPERNOVA	
FINISH	ENGINEER R. Gruner 4/23/70		
	APPROVED J. Seligman 5/15/70		
	FIRST USED ON		
	SCALE	SIZE D CODE 001 DRAWING NUMBER 000046	REV. 00

SHEET 1 OF 1