VAX 9000 Family
Power System Technical Description

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About This Manual

This manual describes the VAX 9000 family power system. It includes a complete description of the major components of the VAX 9000 model 400 systems and VAX 9000 model 210 power systems, including the power front ends.

The physical description and voltage distribution for the Model 400 systems systems is not presented in this draft.

This manual is a reference for Customer Services personnel as well as a training resource for Educational Services.

Intended Audience

The content, scope, and level of detail in this manual assumes that the reader:

- Is familiar with the VAX architecture and VMS operating system at the user level

- Has experience maintaining midrange and large VAX systems

Manual Structure

This manual has ten chapters, two appendixes, and an index:

- Chapter 1, Power System Overview, gives an general overview of the power system.

- Chapter 2, Power System Physical Description and AC Distribution, provides a description of power system components and their physical locations. It also describes dc power distribution at the block diagram level, and ac power distribution.

- Chapter 3, Converter Group Operation, describes the purpose of, and interaction between, components of the various converter groups.

- Chapter 4, DC Power Distribution, details the dc power distribution.

- Chapter 5, Temperature Sensors and Air Moving Devices, describes the temperature sensors and the air moving devices.

- Chapter 6, Power System Functional Description, provides a functional description of the major components in the power system.

- Chapter 7, Power Control Subsystem and PCS Communication, covers the power control subsystem communication.

- Chapter 8, PEM and RIC Initialization and Diagnostics, describes the PEM and RIC initialization sequences.

- Chapter 9, Power Front End Description, describes the functional specifications of the power front end (PFE).

- Chapter 10, Utility Port Conditioner Description, describes the functional specifications of the utility port conditioner (UPC).

- Appendix A, CPU RIC Interface Signals, provides a table of CPU RIC status signals.

- Appendix B, Model 210 OCP Codes, provides tables containing PEM and RIC total off codes.

1
Power System Overview

This chapter gives a brief overview of the VAX 9000 family power system.

1.1 Overview

The VAX 9000 family power systems consume more power and are more complicated than previous power systems. Yet many functions can be compared to previous power systems. This manual details the power front ends, and the general makeup of the power system.

The following sections briefly describe the power system, and the two power front ends, PFE and UPC.

1.2 Power System

The VAX 9000 family power system components generate high voltage dc (280 Vdc) and step down the high voltage to the low voltage dc used to power the system logic units as in previous power systems. The number of these devices varies with system configurations. There are also components that measure cabinet temperature and air flow, and components used to monitor and control power system operation, and provide feedback and error information to the console subsystem.

Some previous systems used an environmental monitoring module (EMM) to control and monitor the regulators and environmental monitoring circuits. The VAX 9000 family power systems use regulator intelligence cards (RICs) to control and monitor up to five power converters, and monitor the environment. The RIC interface functions similar to the EMM interface. It even uses the same protocol, XXNET, although XXNET has been modified slightly.

Figure 1–1, VAX 9000 Family Power System Simplified Block Diagram, gives an overview of the VAX 9000 family power system.

Because a system may have multiple power converters, one RIC cannot monitor all the converters. Therefore there are numerous RICs, each one monitoring an individual voltage bus and responsible for certain environmental functions (Figure 1–1.) Also, the service processor does not have time to communicate with all the RICs, so an intermediary is introduced, the power and environmental monitor module, or PEM. The PEM polls and communicates with the RICs, notifies the service processor of abnormal conditions, and provides the service processor with error conditions that it receives from the RICs.

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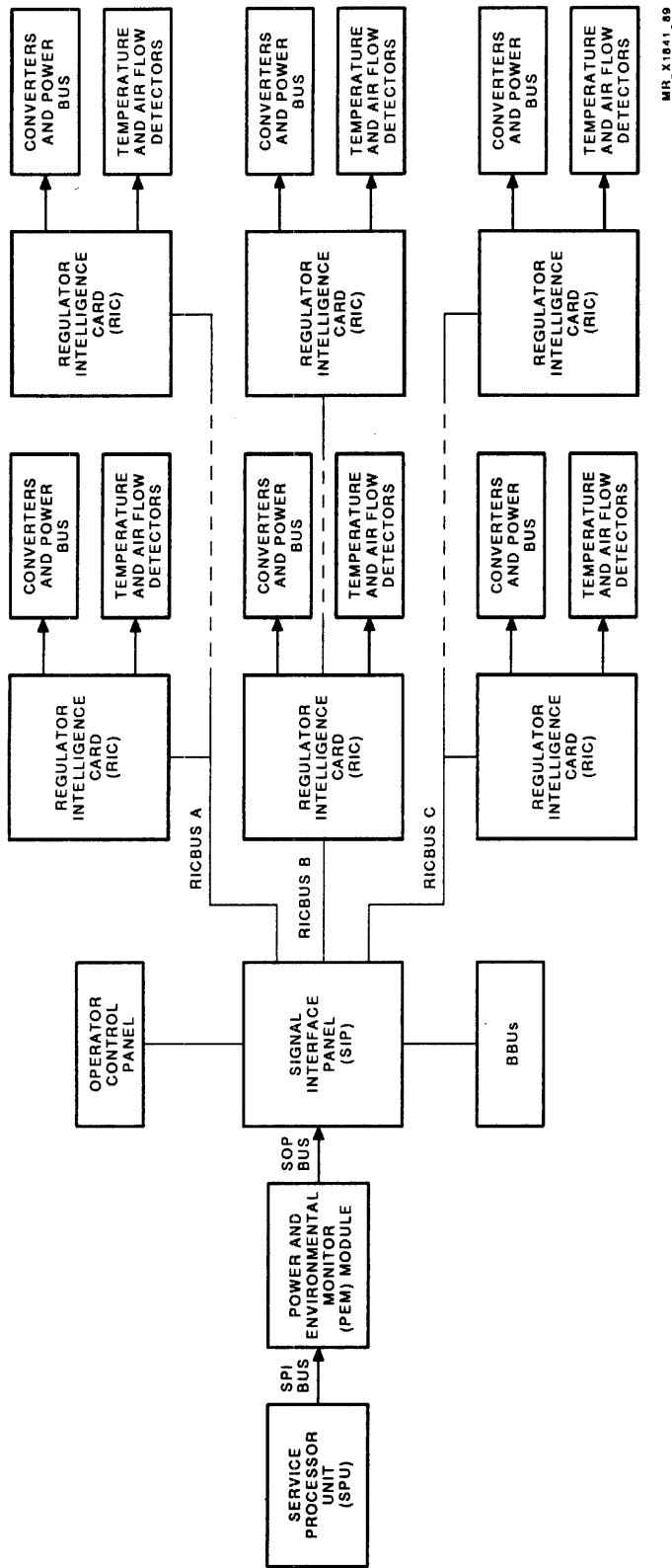
Figure 1–1   VAX 9000 Family Power System Simplified Block Diagram

The signal interface panel (SIP) provides a communication link between the PEM and the RICs, and the PEM and the remainder of the power control subsystem. The PEM writes and reads SIP registers, communicating directly with the RICs to keep abreast of power system status.

Communication between the PEM and the RICs is distributed to a maximum of three RICBUSes at the SIP. The model 210 uses one RICBUS and the model 400 systems use a maximum of three RICBUSes. There are a maximum of five RICs on a RICBUS.

1.3   Utility Port Conditioner (UPC)

The H7392 utility port conditioner (UPC) converts 3-phase ac input power to a regulated 280 Vdc output, with the capability to power a 20 kW load. The UPC can operate over a wide range of input voltages while maintaining a regulated output. The regulated 280 Vdc is distributed to sets of converters and air movers in VAX 9000 CPU, SCU, and XMI cabinets.

The UPC provides an optional or required power front end for all VAX 9000 systems. The UPC may be configured as:

*   An option on U.S. model 200 systems

*   Standard on non-U.S. model 200 systems

*   Standard on U.S. and non-U.S. model 400 systems

The UPC can be controlled at the unit, or remotely through the OCP. Its operational and environmental status is monitored by the SPU through the power control subsystem (PCS). The UPC ride-through capability can maintain the dc output for a short period in the event of an input power line sag or interruption.

1.4   Power Front End (PFE)

The H7390-A power front end (PFE) provides an optional power front end for U.S., VAX 9000 Model 200 systems. It converts 3-phase, 208 Vac input power to a 280 Vdc output. The PFE is able to power an 18.5 kW load, and provides EMI suppression.

The PFE can operate over a wide range of input voltages while maintaining a regulated output. The regulated 280 Vdc output is distributed to sets of dc/dc converters and air movers through the power input panel (PIP) in the model 200 IOA cabinet.

The PFE can be controlled locally at the unit, or remotely through the OCP. PFE operational and environmental status is monitored by the SPU through the power PCS. The PFE ride-through capability can maintain the dc output for a short period in the event of an input power line sag or interruption.

1.4.1   Safety Procedures and Guidelines

Follow these guidelines when working on the VAX 9000 family power system.

* All Customer Services personnel must attend power safety training as a prerequisite for power system maintenance.

* When performing preventive or corrective maintenance, use the following power lock-out/tag-out procedure specified in the *VAX 9000 Family System Maintenance Guide*.

* Never work on the power system alone.

* Observe all customer safety procedures.

* Assure that the power system is correctly grounded.

* Unless maintenance activity requires removal, do not remove any module safety shields when the power system is operational.

* Following any maintenance activity, assure that all test equipment and tools have been removed before applying power to the system.

2

Power System Physical Description and AC Distribution

This chapter provides a general overview of the VAX 9000 family power system and its components.

2.1 Overview

The power system is comparable to previous power systems. As in previous power systems it generates high voltage dc (280 Vdc) and step down the high voltage to the low voltage dc used to power the system logic units. There are also components that monitor and control system operation, and provide feedback and error information to the console subsystem.

There are differences between the model 210 system and model 400 systems in appearance and physical layout, and in power system component layout, although they use the same power system components.

Table 2–1 contains a list of power system components, and a brief description of each component. A more detailed description is found in Chapter 6, Power System Functional Description.

Table 2–1   Power System Components

Name	Number	Description
Power front end (PFE)	H7390	Located in the model 210 IOA cabinet, the H7390 receives building ac power and generates 280 Vdc used by the power system.
Utility port conditioner (UPC)	H7392	May be placed up to 50 feet from the system. Receives building ac power and generates 280 Vdc used by the power system. Optional on model 210 60 Hz systems, required on all 50 Hz and model 400 systems.
Power input panel (PIP)	70-27242-01	Receives 280 Vdc from H7390 or UPC for distribution to power system components.
Battery back up (BBU)	H7231	Provides 250 Vdc for up to 10 minutes to maintain memory refresh in case of power outage. Also provides +5 Vdc to the operator control panel (OCP) diagnostic display and service processor (SPU) time-of-day clock.
Power and environmental monitor (PEM)	T1060	Physically part of the service processor, as it is located on the SPU BI backpanel, but it is a central figure in the power control subsystem (PCS). It is the interface between the power system and the SPU, polling and reporting power system conditions to the service processor module (SPM).
CPU RIC (Regulator intelligence card)	H7388	Turn power converters on and off, monitoring and controlling the power converters voltage output, and monitors and measures various power and system functions, such as converter overtemperature and overcurrent conditions, and system air flow and temperature. The RICs provide information about power and system conditions to the PEM.
I/O RIC	H7389	Turns power converters on and off, and monitors power and system functions such as converter overtemperature and overcurrent conditions, H7390 or H7392 conditions, and system air flow and temperature. It also communicates with the PEM, and differs from the CPU RIC in that it does not have any analog measurement circuitry.
Signal interface panel (SIP)	54-19028-01	Provides a signal interface between various power control subsystem components, including the PEM, RICs, OCP, BBUs, SPU power converters, and H7390 or H7392. It contains circuitry to enable the battery backup units in case of power failure, and the total off circuitry. It also generates the clocks used by the power converters.
RICBUS	RICBUS A, RICBUS B, and RICBUS C	Provide the communication link between the PEM and RICs. There is a maximum of two RICBUSes on model 210 and three on model 400 systems. Each RICBUS connects the SIP to each of the RICs on the bus.

Table 2–1 (Cont.)   Power System Components

Name	Number	Description
Bias supply	H7382	Operate on 280 Vdc, and generates the bias voltages needed for the H7390 and power converters. They also provide power for the RICs, RICBUSes, OCP, OVP modules, and Ethernet transceivers.
Power converters	H7380	Step down 280 Vdc to between 3.2 and 5.5 Vdc, and generate the +5.0, -5.2, and -3.4 Vdc needed by the CPU, SCU, and memory. The voltage an H7380 generates depends on a control voltage supplied by the RIC which monitors the voltage bus. The H7380s are located in the CPU and SCU cabinets only. Multiple H7380 converters may be connected in parallel (current sharing) to provide power for a particular power bus (for instance the -5.2 Vdc bus). Each group of converters is monitored and controlled by a CPU RIC.
Power converters	H7214/H7215	Provides power for the service processor VAXBI backpanel, and each XMI card cage. They are monitored and controlled by an I/O RIC, except the SPU converter pair, which is monitored by the PEM. The circuitry for turning this pair on and off is located on the SIP. Each H7214/H7215 converter pair provides -5.2, -2.0, ±12 Vdc (H7215), and +5.0 Vdc and +13.5 Vdc (H7214).
Overvoltage protection module (OVP)	H7386	Monitors the +5.0, -3.4 and -5.2 Vdc buses in the CPU and SCU cabinets for an overvoltage condition. If a monitored bus exhibits an overvoltage condition, the OVP module informs the RIC of the overvoltage condition, and lights an OVP module LED to indicate which channel detected the condition. Also, if the overvoltage is detected on a -3.4 Vdc bus, the OVP fires an SCR, which shorts the -3.4 Vdc bus to ground to protect the ECL logic.

Figure 2–2 shows the IOA cabinet front view for a system with 280 Vdc provided by an H7390. The only difference in cabinets is the presence of the H7390. The items on the front of the H7390 are:

* J2 — 280 Vdc to PSB

* J5 — 15 Vdc bias from PSB

* J6 — Connection to I/O RIC backpanel to provide RIC monitoring

* AUX OUT RED LED

* 12 V ISO GREEN LED

* MOD OK GREEN LED

* H7390 blower fuse

* On/Off/Remote power switch

* 1 Ø fuses (3)

* Capacitor bank fuses (3)

* Interlock switch S1

IOA CABINET

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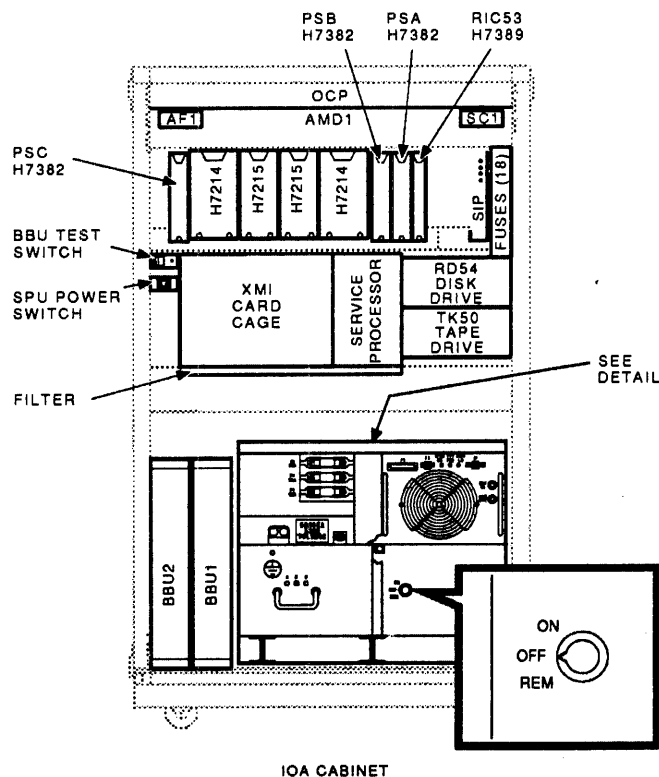
Figure 2–2 (Cont.)   Model 210 IOA Cabinet Configuration Using an H7390, Front View
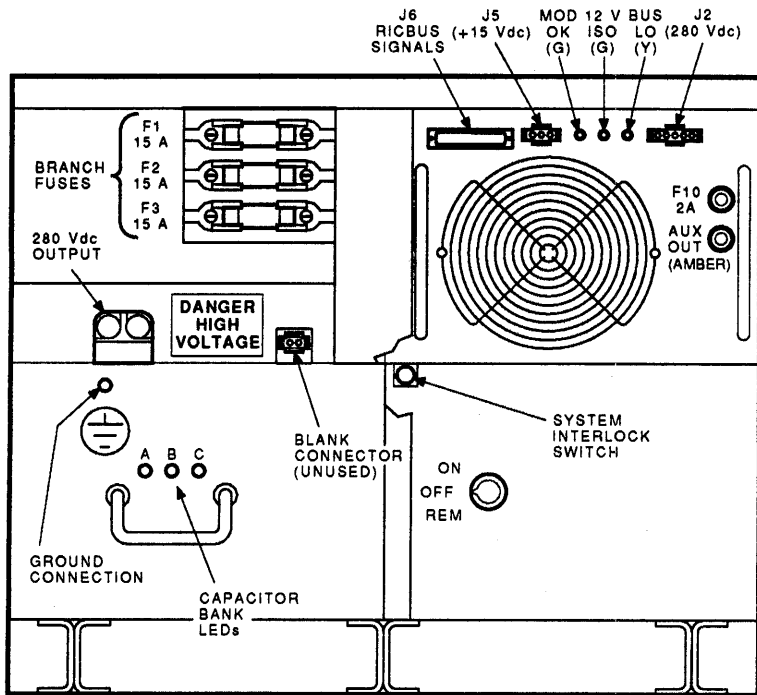
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Figure 2-2   Model 210 IOA Cabinet Configuration Using an H7390, Front View

Figure 2–3 shows the rear view of a model 210 system IOA cabinet. 280 Vdc is provided by an H7392. Only those components not visible from the front are mentioned.

- The transceiver adapter panel. It receives +15 Vdc from bias supply PSC and +13.5 Vdc from the XMI H7214 and powers H4000 Ethernet transceivers.

- PIP/fuse panel. The power input panel (PIP) distributes 280 Vdc through the fuses to the IOA, CPU, and SCU cabinets, including the battery backup circuit.

- The power bulkhead contains the following:

  — DEC power bus and delayed power bus.

  — UPC RICBUS signal cable connector, JC. Provides H7390 status to the I/O RIC.

  — Neon lamps DS1 and DS2. DS1 is across the +140 and -140 Vdc input from the H7392. DS2 is between the -140 Vdc line and +140 line on the BBU side of the blocking diode. DS1 and DS2 are polarized.

  — Total off switch, S1. This switch may be used from the back of the system to turn off system power.

  — CB1 isolates the incoming ac power from J3/J4 and J5/J6.

  — The 280 Vdc input. 280 Vdc is wired and filtered to the PIP.

  — Connector for ac power input from the H7392.

  — Service processor distribution (SPD) panel access plate. Access to the SPD distribution panel allows the CSE to install SPD jumpers for maintenance or troubleshooting purposes.

  — Terminal connectors for CTY, RTY, and PTY.

- The cutaway shows the two dual ac distribution boxes. One is mounted horizontal, the other is mounted vertical. Two outlets are for the H7231 battery backup units. The remaining two outlets are service outlets.
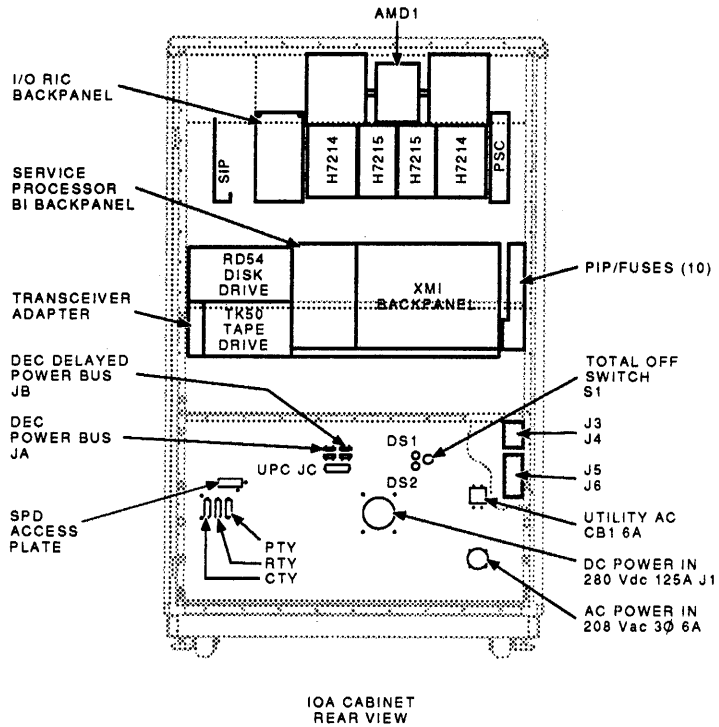
Figure 2-3   Model 210 IOA Cabinet Configuration Using an H7392, Rear View

Figure 2-4 shows the rear view of the model 210 IOA cabinet configured for use with an H7390.
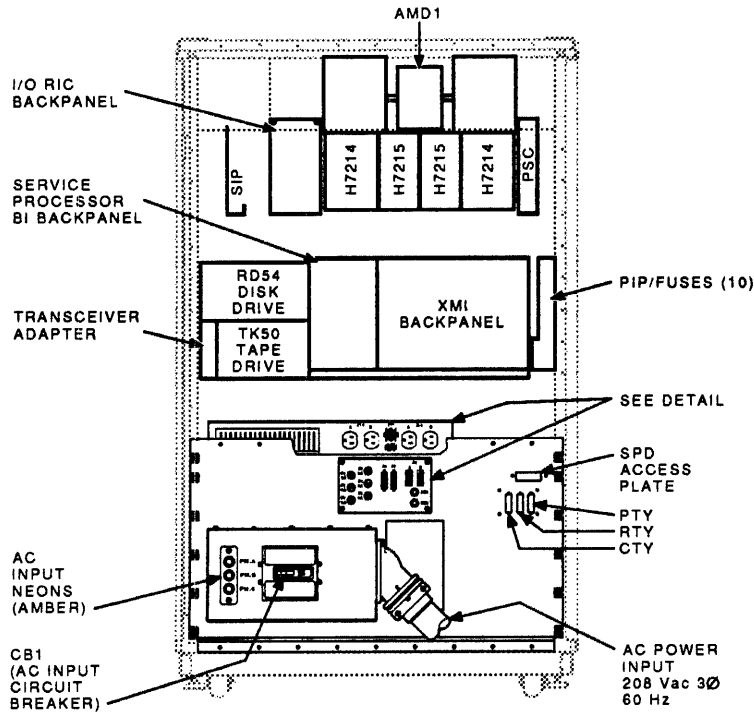
IOA CABINET
REAR VIEW

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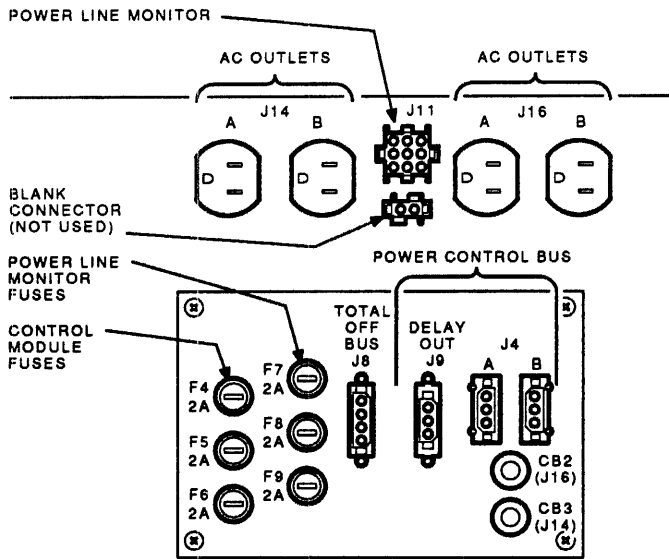
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Figure 2-4   Model 210 IOA Cabinet Configuration Using an H7390, Rear View

2.2.2 Model 210 CPA Cabinet, Front and Side View

See Figure 2-5 for the front and side view of the CPA cabinet. It contains the CPU. Starting at the top of the cabinet the following are found:

- AMD1. The air mover that cools the power components.

- AF2 and SC2. AF2 monitors the air flow that cools the power components. SC2 controls the speed of CPA AMD1.

- T1 measures the temperature of the air leaving the CPA cabinet.

- Two H7380 converters, converters C0 (on the left) and C1, make up part of bus C. They provide -3.4 Vdc to CPU0 logic and SCU logic. The other converter for this bus, C2, is located in the SCU cabinet.

- RIC 24, an H7388 CPU RIC. Communicates over RICBUS B, and monitors bus C, including the converter in the SCU cabinet.

- Three H7380 converters D0, D1, and D2. These bus D converters provide -5.2 Vdc to CPU0 logic, the SCU logic, and the clock module.

- RIC 14, an H7388 CPU RIC. Monitors bus D, and also communicates over RICBUS B.
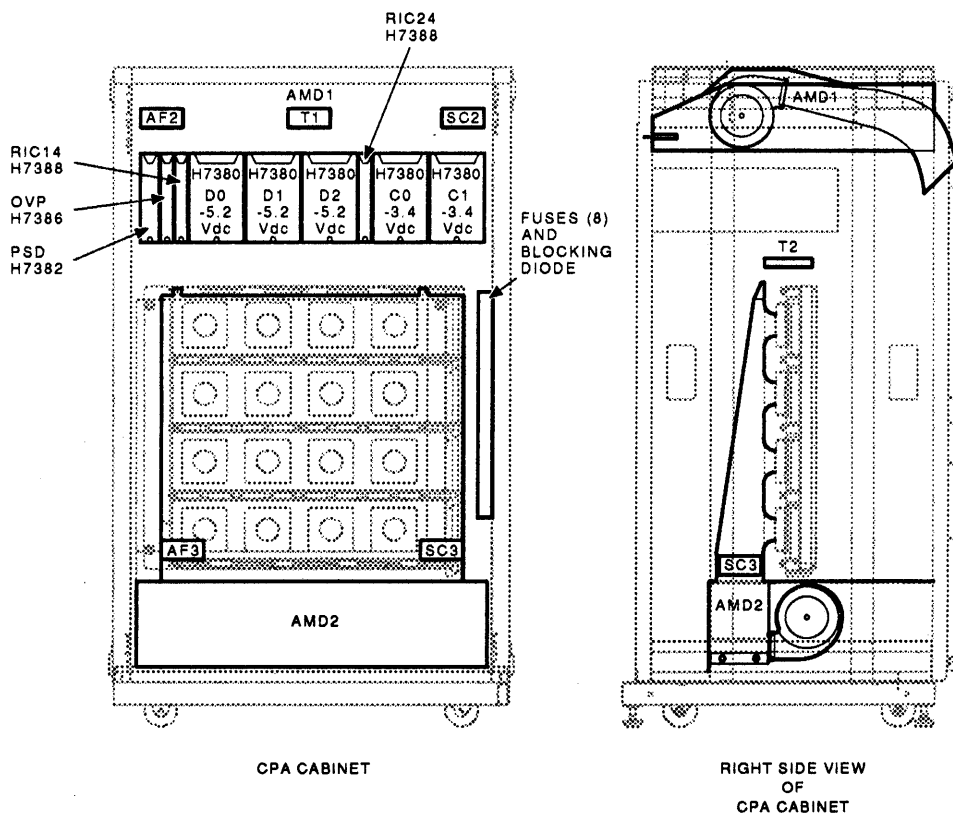
Figure 2-5   Model 210 CPA Cabinet Configuration, Front and Side View

- H7386 overvoltage protection (OVP) module. Monitors bus A, bus B, bus C and bus D, for overvoltage conditions, which are reported to the RICs.

- PSD, an H7382 bias supply. It provides power to RIC 14, 32, and 42, the H7386 OVP module, and bias power for the H7380s for bus A, B, and D.

- Thermistor T2. Monitors the temperature of the air leaving the CPU MCUs and entering the converters.

- AF3 and SC3. Air flow sensors AF3 and SC3 monitor the air flow over the CPU MCUs. SC3 also controls the speed of AMD2. They are located in the bottom of the plenum.

- The air mover for the CPU logic components. The plastic shroud between the air mover and CPU planar ensures proper air flow for each MCU.

Figure 2–6, the rear view of CPA cabinet, contains the following additional components:

- Bus C and D, and OVP backpanels.

- SCR. Shorts the -3.4 Vdc bus to ground when the OVP module detects an overvoltage condition on the -3.4 Vdc bus (bus C).

- SCR gate board. Provides rectification and filtering for the SCR gate fire signal.

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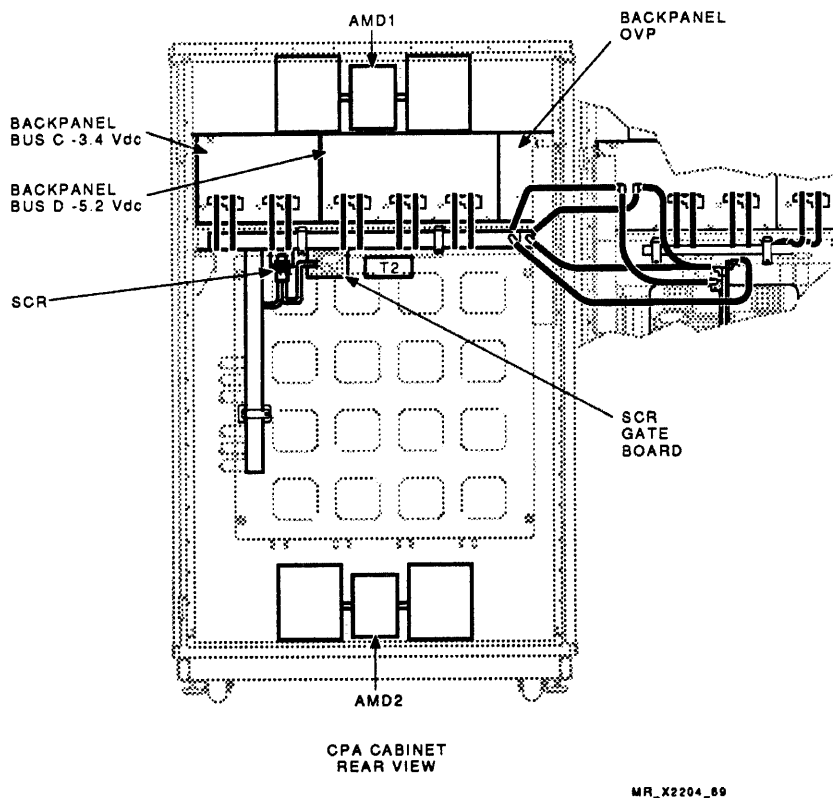
Figure 2–6   Model 210 CPA Cabinet Configuration, Rear View

2.2.3 Model 210 SCU Cabinet

Shown in Figure 2–7 is the SCU cabinet front and side view. It contains the system control unit, memory, and the clock module. The front view includes the following items:

- AMD1. The air mover for the power system components.

- T3, AF4, and SC4. AF4 and SC4 monitor the air flow leaving the power converters. SC4 also controls the speed of SCU cabinet AMD1. T3 measures the temperature of the air leaving the cabinet.

- Converter C2, an H7380 converter that is part of -3.4 Vdc bus C. The other two H7380s on this bus are located in the CPA cabinet.

- The next two H7380s converters; B0 (on the left) and B1. In case of ac power loss, they are powered by 250 Vdc BBU power. They provide +5 Vdc BBU for 10 minutes of memory refresh power.

- RIC 42, an H7388 CPU RIC. Monitors bus B, and communicates over RICBUS B.

- The H7380 converter A0. Provides +5 Vdc on bus A for the memory and clock module.

- RIC 32, an H7388 CPU RIC. Monitors bus A. It also communicates over RICBUS B.

- T4, AF5, and SC5. AF5 and SC5 monitor the air flow over the memory and master clock module. SC5 also controls the speed of SCU cabinet AMD2, the air mover that cools the memory and MCM. T4 measures the temperature of the air exiting the the memory and MCM card cages.

LEFT SIDE VIEW
OF
SCU CABINET
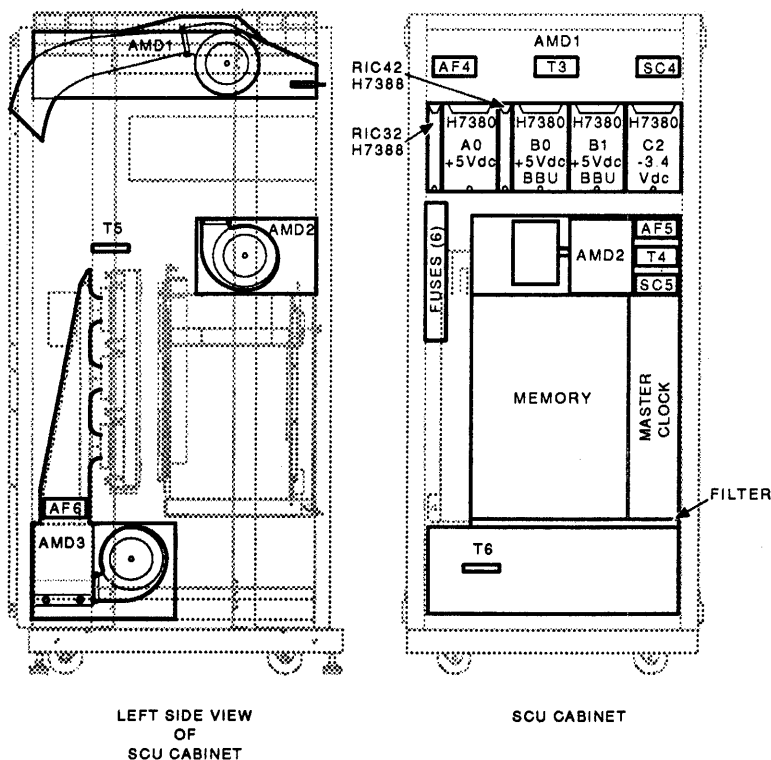
SCU CABINET

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Figure 2–7   Model 210 SCU Cabinet Configuration, Front and Side View

- AMD2. The air mover for the memory and clock modules.

- Fuse panel. Contains fuses for the three air movers in this cabinet.

- The memory subsystem and the clock subsystem.

- Filter under the memory and master clock module. A micro switch on this filter will shut the system down if the filter is removed.

- Thermistor T6. Measures ambient air temperature.

The rear view of the SCU cabinet (Figure 2–8) contains the following additional components:

- Backpanel for bus B and A.

- SC6 and AF6. Monitor the air flow over the SCU MCUs. SC6 also controls the speed of AMD3. These air flow detectors are located in the bottom of the plenum.

- SCU cabinet AMD3. Cools the SCU MCUs.
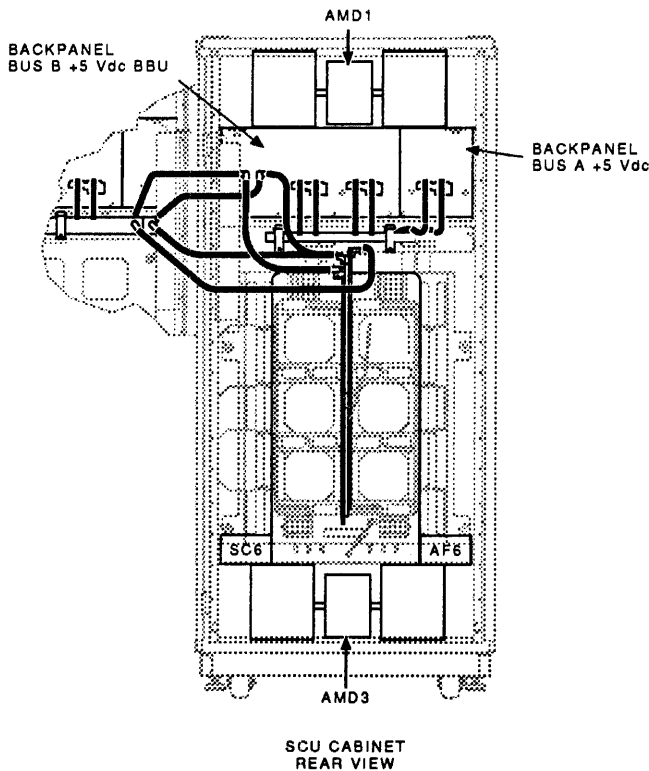
Figure 2–8   Model 210 SCU Cabinet Configuration, Rear View

2.3   VAXBI Expander Cabinet

The VAXBI expander cabinet, and VAXBI expander cabinet power are not covered in this manual. The D-card for BIX monitoring, 54-17961-01, has been designed to monitor the H7139 regulators in BI expander cabinets installed on a VAX 9000 system. This module allows the I/O RICs to monitor BI expander conditions. See Section 6.10.3.4.4, I/O RIC BI Expander Register and VAXBI Expander Cabinet Monitoring.

For more information on the BI expander cabinet, refer to the following manuals:

- VAXBI Expander Cabinet Installation Guide; EK-VBIEA-IN

- VAX 6200/6300, VAXserver 6200/6300 Options and Maintenance; EK-620AB-MG

- VAX 6300, VAX Fileserver 6300 Owner's Manual; EK-620AC-OM

2.4   Power System Block Diagrams and AC Distribution

Two simplified block diagrams depict the VAX 9000 model 210 power systems. The first diagram shows a model 210 system using an H7390 to provide 280 Vdc. The second is similar, but an H7392 provides the 280 Vdc. Because there is limited ac power distribution to the systems, ac distribution is also covered in the block diagram.

NOTE
The 280 Vdc is measured from the +140 to the -140 Vdc line, not to ground. Throughout this manual, it is shown as a single 280 Vdc line to simplify the drawings.

2.4.1   Model 210 Power System Block Diagrams and AC Distribution

The H7390, located in the IOA cabinet (Figure 2–9), receives 208 Vac 3Ø, 60 Hz, from the building utility power. It is routed through a 100 A circuit breaker, CB1, which is normally closed. This circuit breaker is only open if it has been tripped manually or by the system total off circuits. It requires manual resetting. As long as 208 Vac 3Ø is present, and CB1 is closed, the three neon lamps (indicating the presence of 3Ø) on the H7390 are lit.

The H7390 provides four, single phase, switched, service outlets, J14A and J14B, protected by CB3, and J16A and J16B, protected by CB2. The H7231 battery backup units are plugged into J14. J11 is the outlet for the power line monitor.

Although there are no PEM to RIC communications during periods of battery backup, the RICBUS still needs power. The converters providing the battery backup +5 Vdc need clock to operate. Also, if the output voltage gets too low, BBU GROUP LOW is needed to shut down the converter group. These signals are routed to and from the RICBUS by optical isolators, which are powered by RICBUS power.

The H7390 is located in the bottom of the IOA cabinet creating direct connections to the power system. The battery backup units plug directly into the H7390. The 280 Vdc is wired directly from the H7390 to the PIP with a short cable. The cable connection between the H7390 and power control subsystem for ground current measurement, power monitoring, and power control signals terminates at the bus D backpanel, XMI backpanel, and SIP.

If the model 210 system is a 50 Hz system, it requires an H7392 to provide the 280 Vdc (Figure 2–10). Only the differences between a system with an H7390 and a system with H7392 are discussed.

When the H7392 is used, it may be located up to 50 feet away from the system. The cable that carries ground current and so on, exits the H7392 at J10. One cable carries the signals between the H7392 and the IOA cabinet power bulkhead. As with an H7390, the power monitoring signals are terminated at J08 of the I/O RIC backpanel. The ground current goes to J14 of the bus D backpanel in the CPA cabinet, and the power control signals terminate at SIP J05.

The H7392 receives building utility power, 208 Vac 3Ø 60 Hz or 380/416 Vac 3Ø 50 Hz through the main 100 A circuit breaker A1 CB1. This main circuit breaker, is tripped for a total off condition and must be reset manually. It is normally on, and ensures that the H7392 can generate control voltages. When the system power switch is turned on, the H7392 enables 280 Vdc to be sent to the system.

A connection for a power line monitor at J11 is protected by A2 CB2. The ac power to the system leaves the H7392 at J02, and is protected by A2 CB1. The other end of the cable is plugged into AJ2 on the power bulkhead at the bottom rear of the IOA cabinet. It is isolated from two dual outlet ac distribution boxes by CB1. Two of the outlets are reserved for the battery backup units. The other two connections are used as service outlets.

The 280 Vdc is leaves the H7392 at J1. It is hardwired to TB1, filtered, then routed to the PIP.

The remainder of the block diagram is the same as in Figure 2–9.
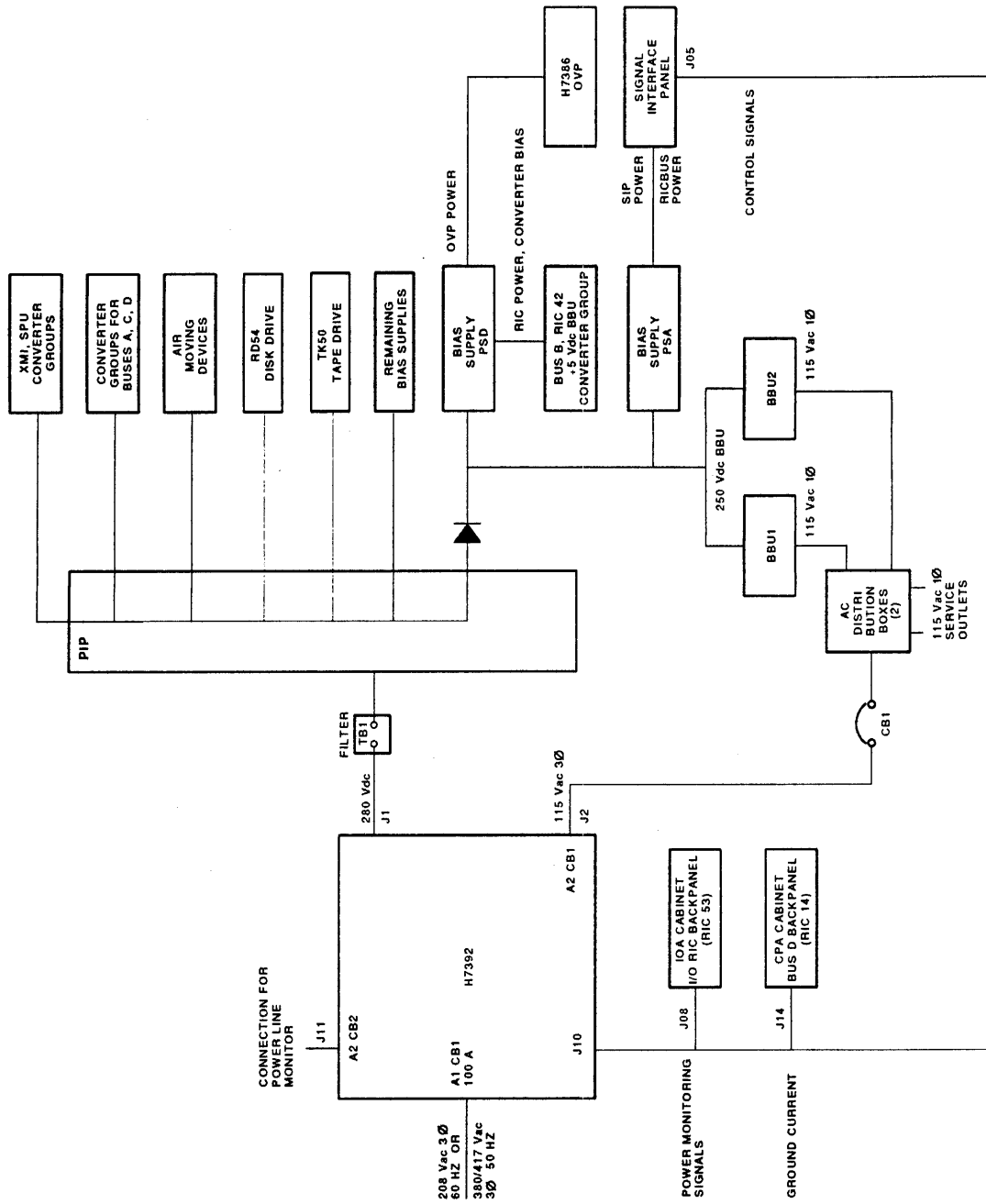
Figure 2-10   Model 210 Power System Basic Block Diagram With an H7392

3

Converter Group Operation

This chapter discusses the three types of converter groups used in VAX 9000 family systems. It describes the function of each component in a converter group, and the interaction between the components.

3.1 H7380 Converter Group

The H7380 converter group supplies +5 Vdc, -5.2 Vdc, +5 V BBU, and -3.4 Vdc to the CPU and SCU cabinets with the following converter groups (buses) (Table 3–1):

The H7380 converter receives 280 Vdc and generates its specific output voltage, a voltage determined by the CPU RIC that monitors and controls the associated output bus.

Table 3–1 H7380 Converter Groups

Model	Bus
210	A, B, C, D
410 or 420	A, B, C, D, J, K
440	A, B, C, D, J, K, M, N

3.1.1 Bias Power to H7380 Converters

The bias supply, operating on 280 Vdc, provides +15 Vdc bias to the converter (Figure 3–1). This +15 Vdc is used to power the control circuitry within the converter until the converter can supply the voltage itself. The +15 Vdc generated within the converter is ORed with the +15 Vdc from the bias supply, allowing the converter to supply its own bias once it is providing power.

The bias supply provides the power needed to operate the RICs: ±15 Vdc and +5 Vdc for the CPU RICs, and +15 Vdc and +5 Vdc for the I/O RIC.

The bias supply also supplies the ±15 Vdc that the OVP module needs for operation.

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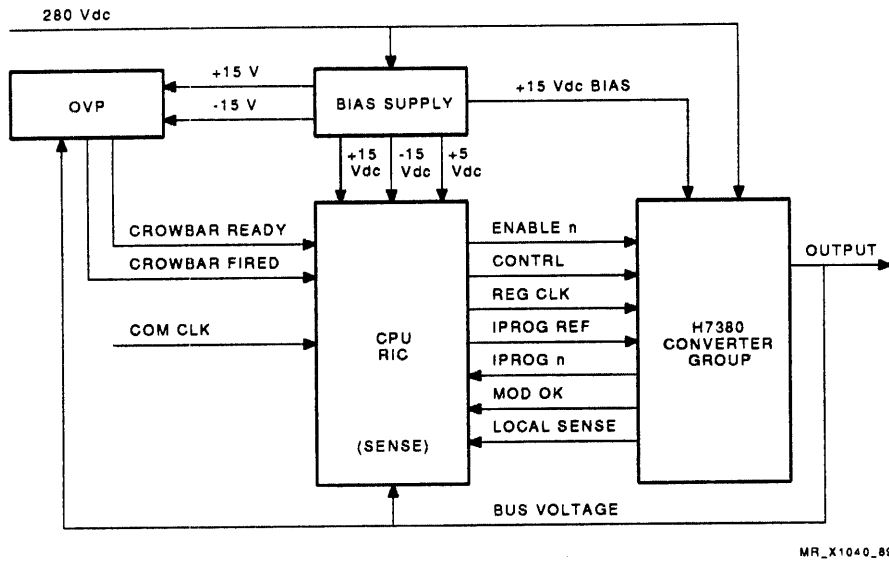
Figure 3–1   H7380 Converter Group Operation

3.1.2 Enabling H7380 Converters

The RIC microprocessor, when commanded by the PEM, asserts an enable line, ENABLE n, to turn on a converter. If the enable line is deasserted at any time, the converter shuts down. This feature is used during overcurrent situations to turn off a converter momentarily, reducing the overall output energy.

3.1.3 OVP in a Converter Group

When the over voltage protection (OVP) module receives ±15 V from the bias supply, the OVP logic generates an internal reset, which enables it to monitor bus voltage for an overvoltage condition. The OVP informs the RIC that it is powered up, has been reset, and enabled, by asserting CROWBAR READY.

When the OVP module detects an overvoltage condition, it informs the RIC of the overvoltage condition by asserting CROWBAR FIRED. CROWBAR FIRED is routed to the CPU RICs via STATUS[10]. The RIC shuts down the converter group. Although the OVP module is monitoring the +5.0, -5.2, and -3.4 Vdc buses, only the -3.4 Vdc bus is protected by an SCR. For an explanation of the OVP module, see Section 6.8, H7386 Overvoltage Protection (OVP) Module.

3.1.4 H7380 Operation in a Converter Group

The converters receive low current 280 Vdc and produce low voltage, high current outputs. The converters are current mode controlled, switching converters.

The RIC compares bus voltage to the reference voltage. The error voltage, CONTRL, determines the converter output current. CONTRL varies between 2.5 and 5.0 V. The H7380 provides a proportional output varying between 0 and 240 A.

3.1.5 RIC/H7380 Feedback Loop

The RIC generates a reference voltage that is dependent on the RIC's backpanel location and RIC software. See Section 6.10.2.4, Reference Voltages for a description of reference voltage generation. The reference voltage is compared to the actual converter output voltage (measured through the SENSE inputs to the RIC). The error voltage, CONTRL, is routed to the converters to control the converter output.

3.1.6 N + 1 Redundancy

The RIC generates another reference voltage, IPROG REF, which is routed to the converters. If the converter is installed, jumpers on the converter route this reference back to the RIC as IPROG n, which is used by the RIC to set the overcurrent trip level.

Also, the RIC microprocessor determines the number of converters present by reading IPROG n, and sets up the voltage reference D/A converter based on the number of converters installed.

For instance, if -5.2 Vdc at 500 A is needed, and there are 5 converters, each converter has to put out 100 A. The voltage reference is routed to the error amplifier that generates CONTRL at a voltage to ensure that each converter generates 100 A.

If one of the converters fails, the sudden drop in output voltage is recognized by the error amplifier through SENSE, which increases CONTRL to cause each of the 4 remaining converters to supply 125 A.

NOTE
N + 1 redundancy is only available on VAX 9000 model 400 systems, it is not available on VAX 9000 model 200 systems.

3.1.7 H7380 Converter Group Clock

The SIP generates COM CLK, which is routed to the RIC, then sent as REG CLK to the H7380's power converter pulse width modulator. The clock normally used is 162.5 kHz. The RIC has an oscillator used to generate a 158 kHz clock that provides the necessary clock if the SIP clock is lost. Circuitry on the RIC, upon detection of a loss of COM CLK, allows the backup clock to be sent to the H7380.

3.1.8 Monitoring the H7380 Converters

The RICs continually check MOD OK from each of the converters in the converter group to ensure that each converter is operating correctly. If a converter fails to function correctly, the RIC reports this, by way of the PEM, to the SPU.

3.2 SPU Converter Group

The SPU converter group, consisting of a bias supply, the SIP, and a H7214 and H7215 switching regulator, is used to power the service processor BI backpanel (Figure 3-2).
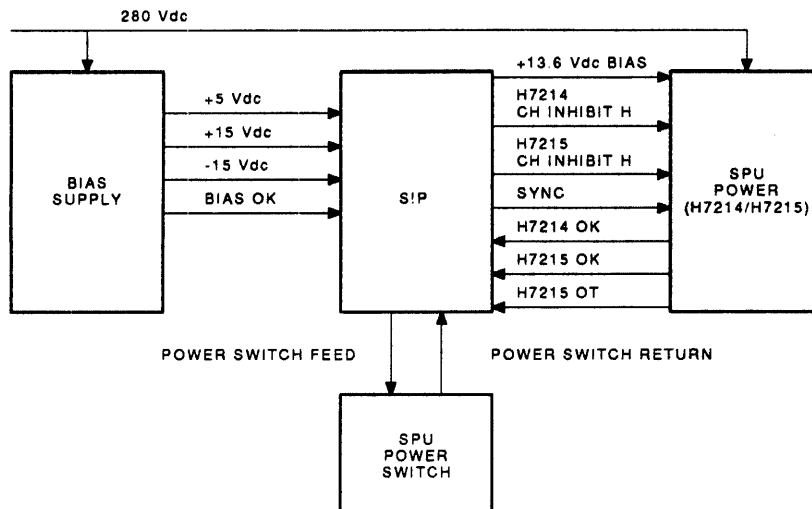
MR_X104'_89

Figure 3-2   SPU Converter Group Operation

3.2.1 SIP Power

The bias supply, operating on 280 Vdc, provides +5 Vdc and ±15 Vdc to the SIP. The +5 and +15 Vdc powers the SIP logic, and ±15 Vdc is used for relay logic. For more information on SIP power, see Section 6.2.1, SIP Power Distribution.

3.2.2 Enabling the H7214/H7215 Converters

If the SPU power switch is closed when the bias supplies serving the SIP, which also provide the bias voltage to the SPU H7214 and H7215, indicate to the SIP that they are operational, the H7214 CH INHIBIT H signal is deasserted, enabling the SPU H7214. When the H7214 voltage outputs are within tolerance, the assertion of H7214 OK at the SIP causes deassertion of H7215 CH INHIBIT H to enable the H7215.

When the SPU power switch is opened, the PEM is informed of an impending power loss, causing the PEM to initiate a BI power down sequence. After a 63 ms delay, H7214 CH INHIBIT H is asserted to disable the H7214. When H7214 OK is deasserted, H7215 CH INHIBIT H is asserted to disable H7215.

NOTE
These converters supply power to the BI backpanel where the PEM resides. Therefore, there is no wait for a command from the PEM.

The +15 Vdc from the bias supply to the SIP is attenuated by two diodes to 13.6 Vdc, and routed as bias to the SPU converters. The SIP also provides the regulators with a 32.5 kHz clock (SYNC), which is used to keep the regulators synchronized to each other.

When the inhibit is deasserted, 280 Vdc is converted to +5 and +13.5 Vdc by the H7214 and ±12, -2, and -5 Vdc by the H7215.

3.2.3 Monitoring the SPU Converters

The H7214 and H7215 assert H7214 OK and H7215 OK to indicate that their output voltages are within regulation. The PEM can read the status of these signals at the SIP. These signals are also used on the SIP to light a green LED for each of the asserted OK signals. This is in addition to the green LED on the rear of each of the regulators that also indicate the output voltages are within regulation.

Additionally, the H7215 provides the SIP with an indication of an overtemperature condition, a condition that initiates a system shutdown.

3.3 XMI Converter Group

The XMI converter group is located in an I/O (IOA or IOB) cabinet, with each converter group providing power for one XMI backpanel. There may be a maximum of two XMI backpanels in a model 400 I/O cabinet, and therefore two converter groups (Figure 3–3).

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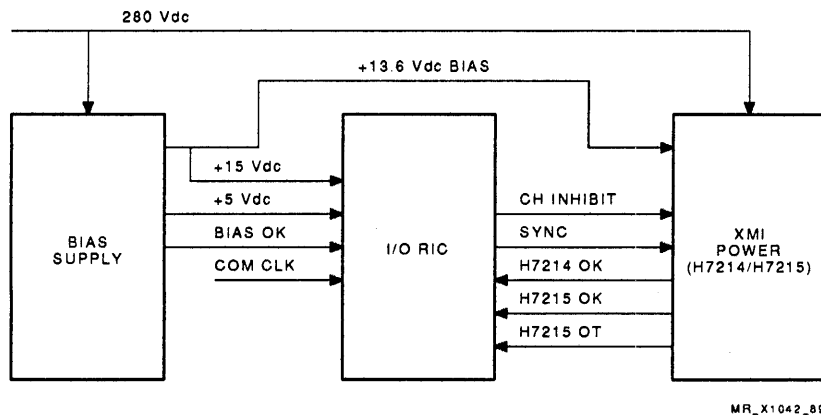
Figure 3–3   XMI Converter Group Operation

3.3.1 Bias Power to H7214/H7215 Converters

The bias supply, operating on 280 Vdc, provides +15 Vdc bias to the I/O RIC backpanel, where it is attenuated to 13.6 Vdc by 2 diodes. The 13.6 Vdc bias is then routed to the converters where it is used to power the control circuitry within the converter.

The bias supply provides the power needed to operate the I/O RIC: +5 Vdc and +15 Vdc.

The H7214 and H7215 generate +5 and +13.5 Vdc (H7214) and ±12, -2.0, and -5.2 Vdc (H7215) from 280 Vdc.
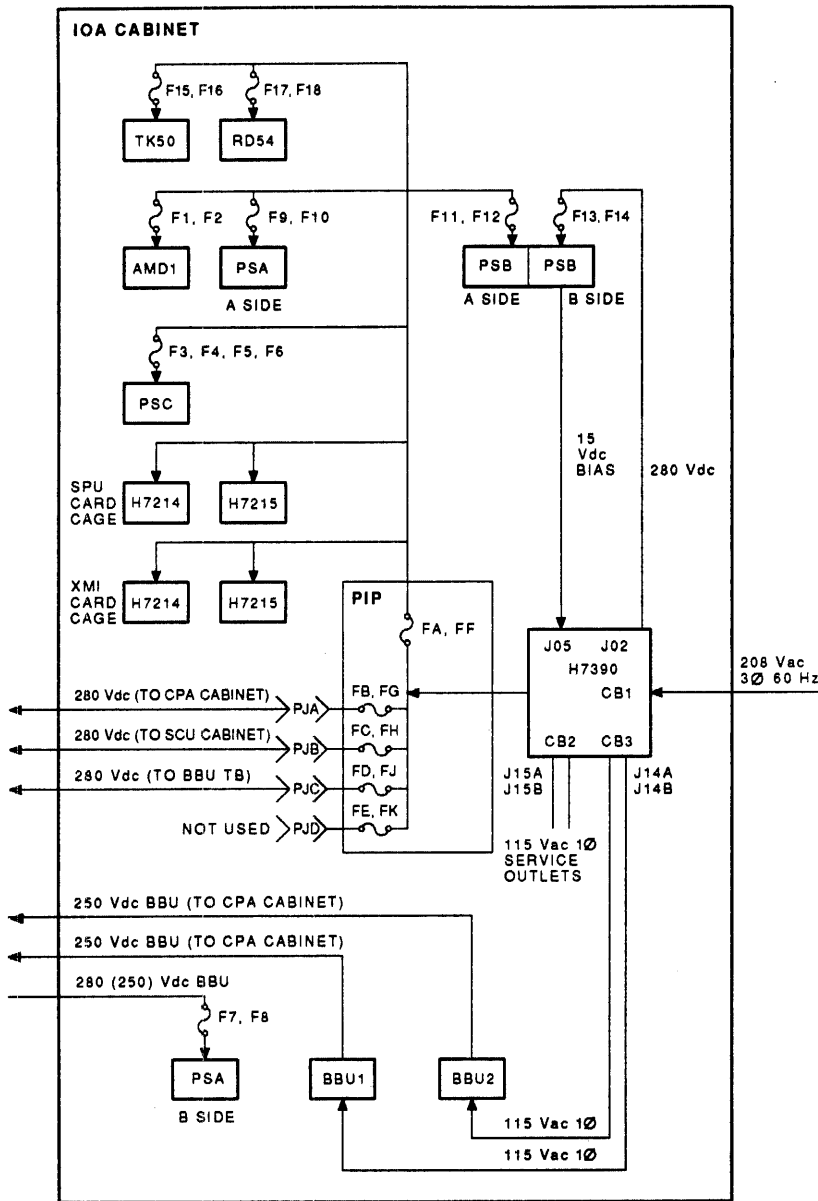
MR_X1848_89

Figure 4-1   Model 210 IOA Cabinet High Voltage DC Distribution Using an H7390

When the power switch is turned on, the power request is routed to the H7390 (or H7392 control circuits) to energize relays that route the 280 Vdc to the PIP and battery backup high voltage distribution line. At the same time, the H7390 or H7392 provides the 115 Vac 1Ø to the battery backup units and two additional service outlets.

If an H7392 is used to supply 280 Vdc, bias supply PSA B side does not have power applied before system power is turned on (the B side is not even used). The H7392 provides its own bias. In this case, when the power switch is turned on, the H7392 provides 280 Vdc to the PIP and 115 Vac 1Ø to the H7231s, by way of an ac distribution box (Figure 4-2).
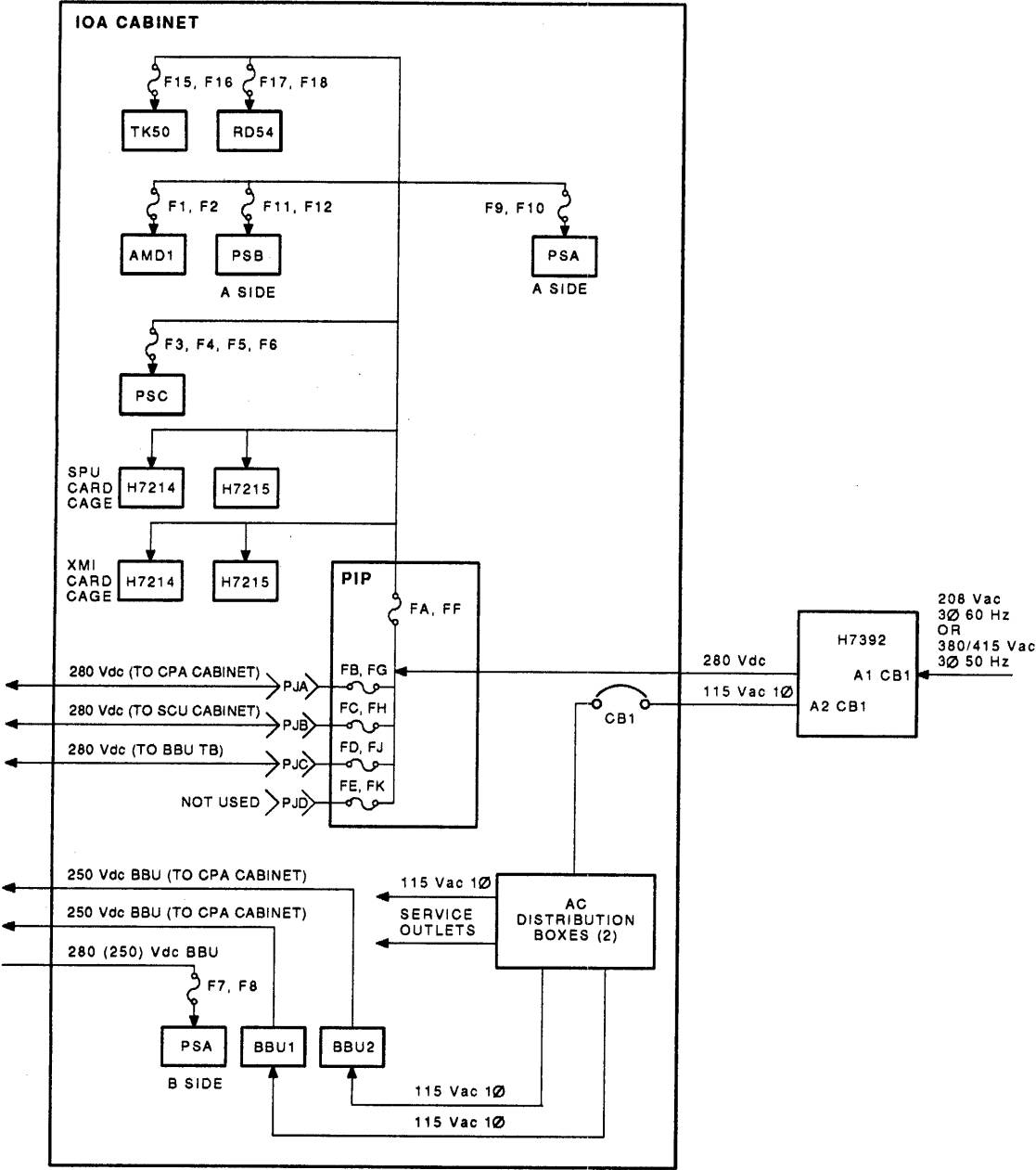
Figure 4–2   Model 210 IOA Cabinet High Voltage DC Distribution Using an H7392

The 280 Vdc voltage on the high voltage distribution line from the H7390 or H7392 is ORed with the 250 Vdc H7231 battery backup output. BBU power is present only if ac power has been lost and there is no voltage from the H7390 or H7392. The blocking diode prevents the battery backup power from supplying the rest of the 280 Vdc bus. The H7231 battery backup units contain diodes to protect them when normal power is being supplied by the H7390 or H7392.

Fuses F1 through F12 are located in the upper right corner in the front of the IOA cabinet. Fuses FA through FJ are located on the PIP, at the rear of the IOA cabinet. See Table 4–1 for a list of fuses and their uses.

For the remainder of the IOA cabinet high voltage distribution description, see either Figure 4–1 or Figure 4–2. Within the IOA cabinet, additional recipients of 280 Vdc from the PIP are:

- The A side of H7382 bias supply PSA

- The A side of H7382 bias supply PSB

- AMD1, which provides cooling for the cabinet

- H7382 bias supply PSC

- The H7214/H7215 converters that provide power to the SPU BI backpanel

- The H7214/H7215 converters that provide power to the XMI backpanel

For high voltage distribution in the other cabinets, see Figure 4–3.

Battery backup dc distribution (280 Vdc BBU) provides power to bias supply PSD (B side) in the CPA cabinet, and the H7380 converters for bus B in the SCU cabinet. For more information on the battery backup request circuitry, see Section 6.2.5, BBU Interface and Control.

In addition to the battery backup dc power in the CPA cabinet, 280 Vdc from the PIP is provided to:

- Two air movers. AMD1 (the top air mover) cools the power system components, while AMD2 (the bottom air mover) cools the CPU logic components.

- Two H7380 converters (of three) for bus C (-3.4 Vdc). The other converter for bus C is in the SCU cabinet.

- Three H7380 converters for bus D (-5.2 Vdc).

CPU cabinet fuses F1 through F8 and the blocking diode are located to the right of the CPU planar in the front of CPA cabinet.

In the SCU cabinet, 280 Vdc is provided to:

- Three air movers. AMD1 (the top air mover) cools the power system components, AMD2 (the middle air mover) cools the memory and clock, while AMD3 (the bottom air mover) cools the SCU logic components.

- The third H7380 for bus C (-3.4 Vdc). The other two H7380s for this bus are in the CPA cabinet.

- The H7380 converter for bus A (+5 Vdc).

SCU cabinet fuses F1 through F6 are located to the left and above the memory backpanel in the front part of the SCU cabinet.

Figure 4–3   Model 210 CPA and SCU Cabinet High Voltage DC Distribution
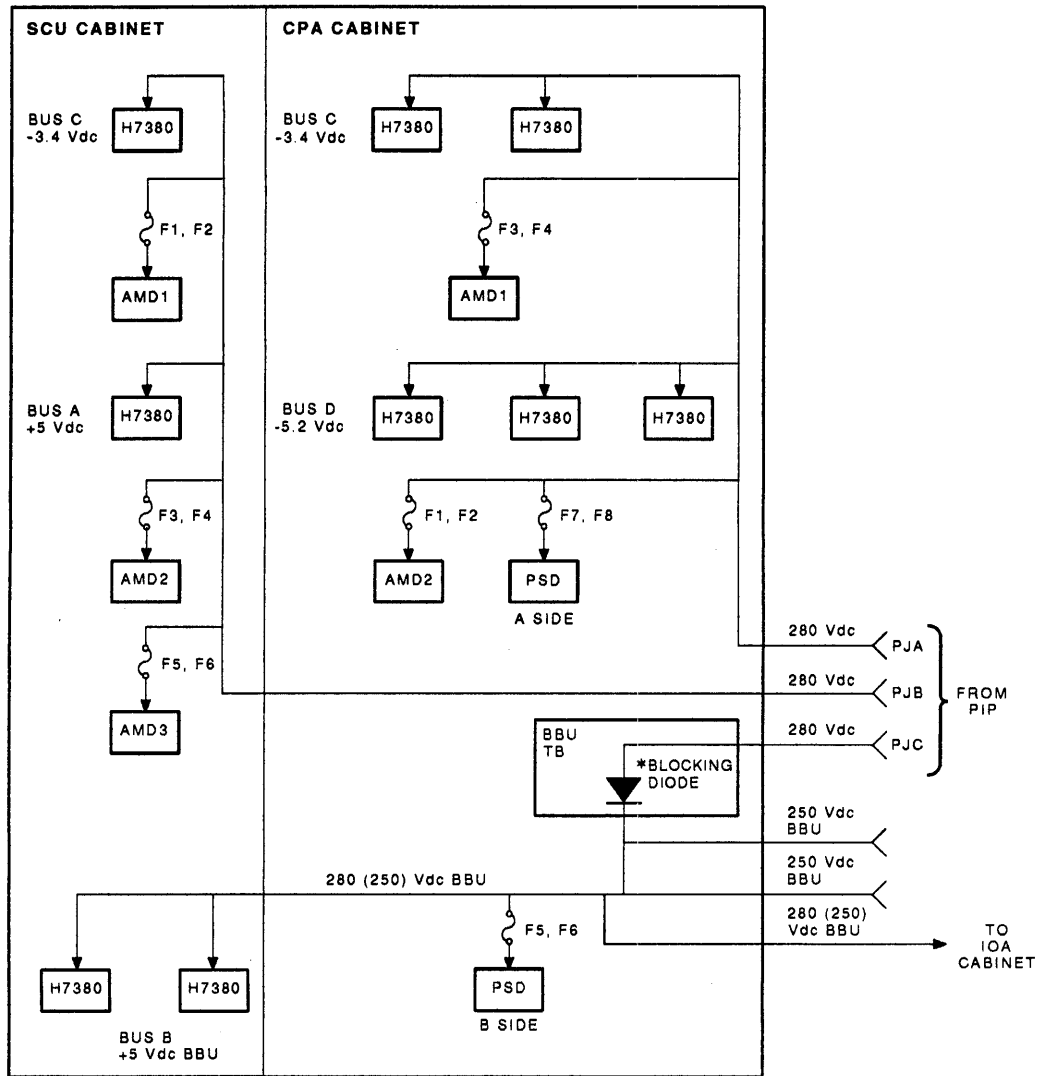
*THE BLOCKING DIODE IS ON THE +140 Vdc LINE ONLY.

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Table 4–1 Model 210 Fuses

Fuse	Voltage Polarity	Power Supplied to:
IOA Cabinet, PIP Fuses		
A, F	+, -	280 Vdc to the IOA cabinet
B, G	+, -	PJA, 280 Vdc to the CPA cabinet
C, H	+, -	PJB, 280 Vdc to the SCU cabinet
D, J	+, -	PJC, 280 Vdc to the BBU TB in the CPA cabinet
E, K	+, -	PJD, not used
IOA Cabinet, Fuses at the Front Right of Cabinet		
1, 2	-, +	AMD1
3, 4	-, +	PSC B side[1]
5, 6	-, +	PSC A side[2]
7, 8	-, +	PSC B side[1]
9, 10	-, +	PSC A side[2]
11, 12	-, +	PSC A side[2]
13, 14	-, +	PSC B side[1]
15, 16	-, +	TK50 tape drive
17, 18	-, +	RD54 TK50 disk drive
CPA Cabinet Fuses		
1, 2	-, +	AMD2
3, 4	-, +	AMD1
5, 6	-, +	PSD B side[1]
7, 8	-, +	PSD A side[2]
SCU Cabinet Fuses		
1, 2	-, +	AMD1
3, 4	-, +	AMD2
5, 6	-, +	AMD3

[1]H7382 bias supply connector pins 10, 3.

[2]H7382 bias supply connector pins 8, 1.

4.2 Model 210 Low Voltage DC Distribution

This section details the distribution of low voltage dc power by cabinets, starting with the IOA cabinet. The low voltage distribution includes the bias supply and converter outputs. The model 210 H7382 bias supply voltage distribution is summarized in Table 4–2.

Table 4–2   Model 210 Bias Supply Distribution

| Bias Supply | Location | Bias Supply Output | | | |
		A1	B1	A2	B2
PSA	IOA	SIP J26[1]	SIP J26[1]	SIP J15[2]	SIP J15[2]
PSB	IOA	I/O RIC backpanel J09, RIC 53, XMI H7214/H7215	Spare	Spare	H7390 control circuits[3]
PSC	IOA	Transceiver adapter[4]	Transceiver adapter[4]	RIC 24 bus C converter bias[5]	Spare
PSD	CPA	RIC 32, bus A converter bias	RIC 42, bus B converter bias	RIC 14, bus D converter bias	H7386 OVP

[1]The +5 V from SIP J26 is used to power all three RICBUSes.

[2]The +15 V from SIP J15 is used as bias to the H7214/H7215 for SPU power. The +5 V and ±15 V provides SIP power.

[3]Output is not used if an H7392 is used to supply 280 Vdc.

[4]The H4000 Ethernet transceivers require power in the range of 13 to 15.75 Vdc.

[5]Output is used in the SCU cabinet.

4.2.1 Model 210 IOA Low Voltage Distribution

For the discussion of IOA cabinet low voltage distribution, see Figure 4–4.

H7382 bias supply PSC provides +15 Vdc from J10 to the transceiver adapter (54-19045-01). This power is supplemented by +13.5 Vdc from the H7214 that supplies power to the XMI bus, to provide power to up to four H4000 Ethernet transceivers.

NOTE
The voltage for an H4000 varies from a minimum of +11.4 Vdc to a maximum of +15.75 Vdc.

The PSC A2 output is not used in the IOA cabinet.

Bias supply PSB is powered from two different sources. The B side receives 280 Vdc directly from the H7390, if installed. In return, PSB provides +15 V bias from the B2 output for the H7390 control circuit power. This power is available even if the system has not been turned on at the operator control panel (OCP), as long as CB1 on the H7390 is closed. Two cables carry these voltages between PSB and the H7390. The PSB B1 output is not used.

NOTE
The bias supply outputs are crossed; the A side outputs are A1 and A2.
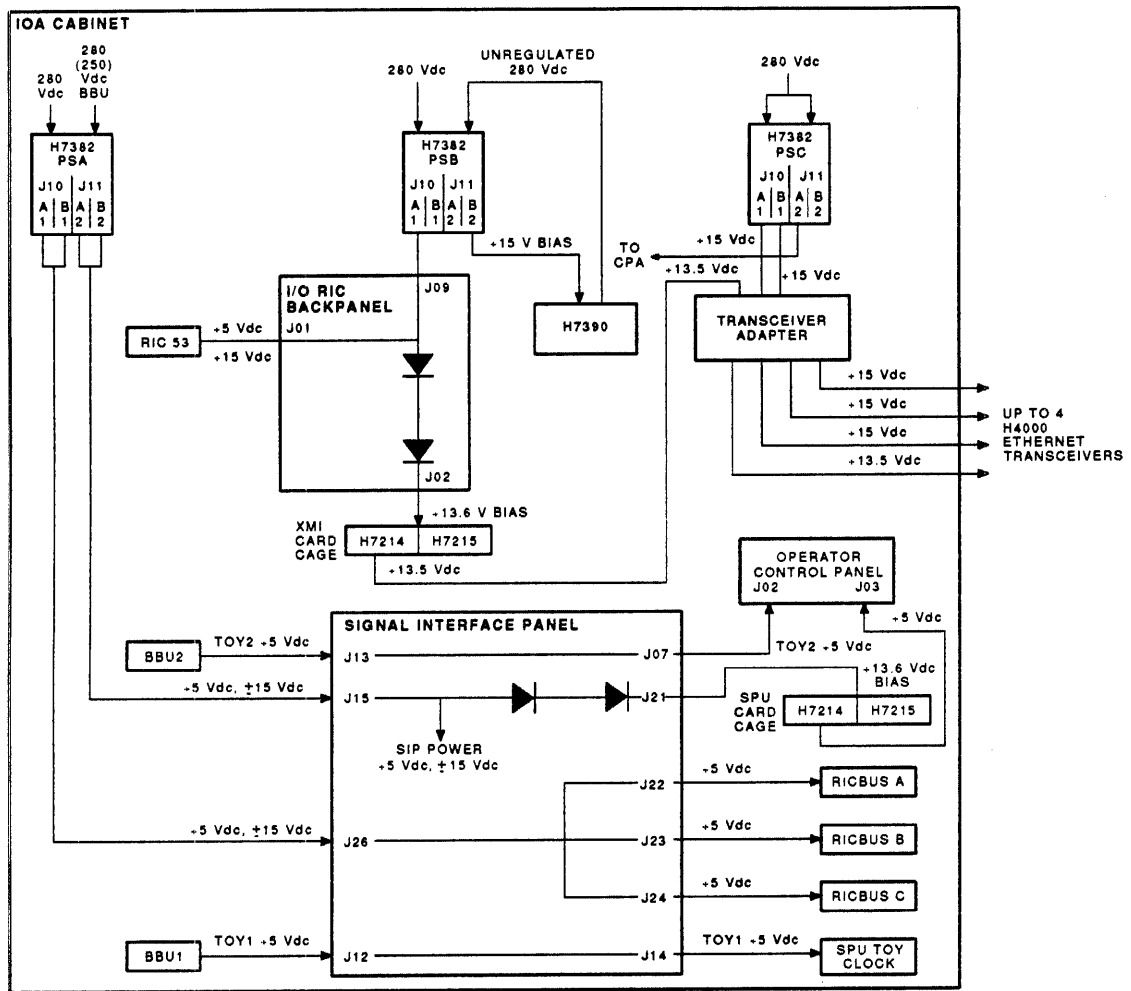
Figure 4–4   Model 210 IOA Cabinet Low Voltage Distribution

The other input to bias supply PSB is normal system 280 Vdc, which is not available until the system has been turned on with the keyswitch. The bias supply A1 output is routed to the I/O RIC backpanel at J09. It provides +5 and +15 Vdc to power RIC 53, the I/O RIC. The RIC is plugged into J01 of the I/O RIC backpanel. The +15 Vdc is attenuated across two diodes to +13.6 Vdc, and a cable from J02 routes this 13.6 Vdc bias to the H7214/H7215 converter pair that provides the XMI power. The PSA A2 output is not used.

TOY1 +5 V BBU is received on the signal interface panel (SIP) from BBU1 on J12. It is redirected by a cable from J14 to the service processor BI backpanel, where it powers the service processor time-of-year (TOY) clock.

TOY2 +5 V BBU is received on the SIP from BBU2 on J13. It is sent by a cable from J07 to the OCP. There, it provides power to the diagnostic display LEDs for up to 100 hours after a power loss (Section 6.1.1).

The remainder of the low voltage power distributed in the IOA cabinet is generated by bias supply PSA. The bias supply A1 and B1 outputs are routed to the J26 input on the SIP. The A2 and B2 outputs supply the SIP at J15. The J15 input provides SIP power, +5 Vdc, and ±15 Vdc. The +15 Vdc input is attenuated by two diodes to +13.6 Vdc, then routed as bias via J21 to the service processor H7214/H7215 converter pair. The H7214 provides the OCP with the remainder of its +5 Vdc power.

The J26 input to the SIP is routed out on J22 (RICBUS A), J23 (RICBUS B), and J24 (RICBUS C) to provide RICBUS power. Only +5 Vdc is used by the RICBUSes. It powers the signals that are common to all the RICs on that RICBUS (Section 6.11.2).

The B side of PSA is powered by the BBU 250 Vdc. During a power loss, the SIP and the RICBUSes still receive power. Although the SPU H7214/H7215 receive bias, they will not function because they do not receive 280 Vdc input power.

4.2.2 Model 210 CPA and SCU Low Voltage Distribution

The low voltage used within the CPA and SCU cabinets is provided by bias supplies PSC, located in the IOA cabinet, and PSD, located in the CPA cabinet (Figure 4–5).

The PSC A2 output provides +5 and ±15 Vdc to power RIC 24 and +15 Vdc bias to three H7380 converters. These converters make up bus C, which provides -3.4 Vdc power to CPU0, the SCU, and the clock. Note that one of these H7380s (C2) resides in the SCU cabinet.

H7382 PSD is supplied by normal 280 Vdc on the A side and 250 Vdc BBU on the B side. The PSD outputs are used as follows:

- The A1 output provides +5 Vdc and ±15 Vdc to power RIC 32 and +15 Vdc bias to the H7380, which provides bus A +5 Vdc power for the memory backpanel.

- The A2 output provides +5 Vdc and ±15 Vdc to power RIC 14 and +15 Vdc bias to three H7380 converters. These converters make up bus D, which provides -5.2 Vdc power to CPU0, the SCU, and the clock.

- The B1 (BBU powered) output provides +5 Vdc and ±15 Vdc to power RIC 42, and +15 Vdc bias to two H7380s, which generate +5 V BBU power for the memory and SCU backpanels. This memory refresh power is available for up to 10 minutes in case of a power outage. The +5 Vdc BBU is also sent to the array control interface (ACU) in the SCU to provide power to the handshaking circuits. The RIC needs power to keep the converters enabled. If the RIC lost power, the enables to the converters would be lost.

- The B2 (BBU powered) output provides +5 Vdc and ±15 Vdc to the H7386 OVP module. The OVP module monitors the -3.4, -5.2, and both +5 Vdc (+5 Vdc and +5 Vdc BBU) buses for overvoltage conditions. An OVP module can monitor only three buses, so the two +5 Vdc buses are ORed as one input. Any overvoltage condition on any bus is reported to the RIC responsible for that bus. When two +5 Vdc buses are monitored together, both RICs are informed. The RIC voltage measurement determines which of the two buses actually caused the overvoltage condition. See Section 6.8.2.1 for further discussion on the OVP module.

  The OVP is necessary during battery backup conditions as a backup to the RIC in case of overvoltage conditions.
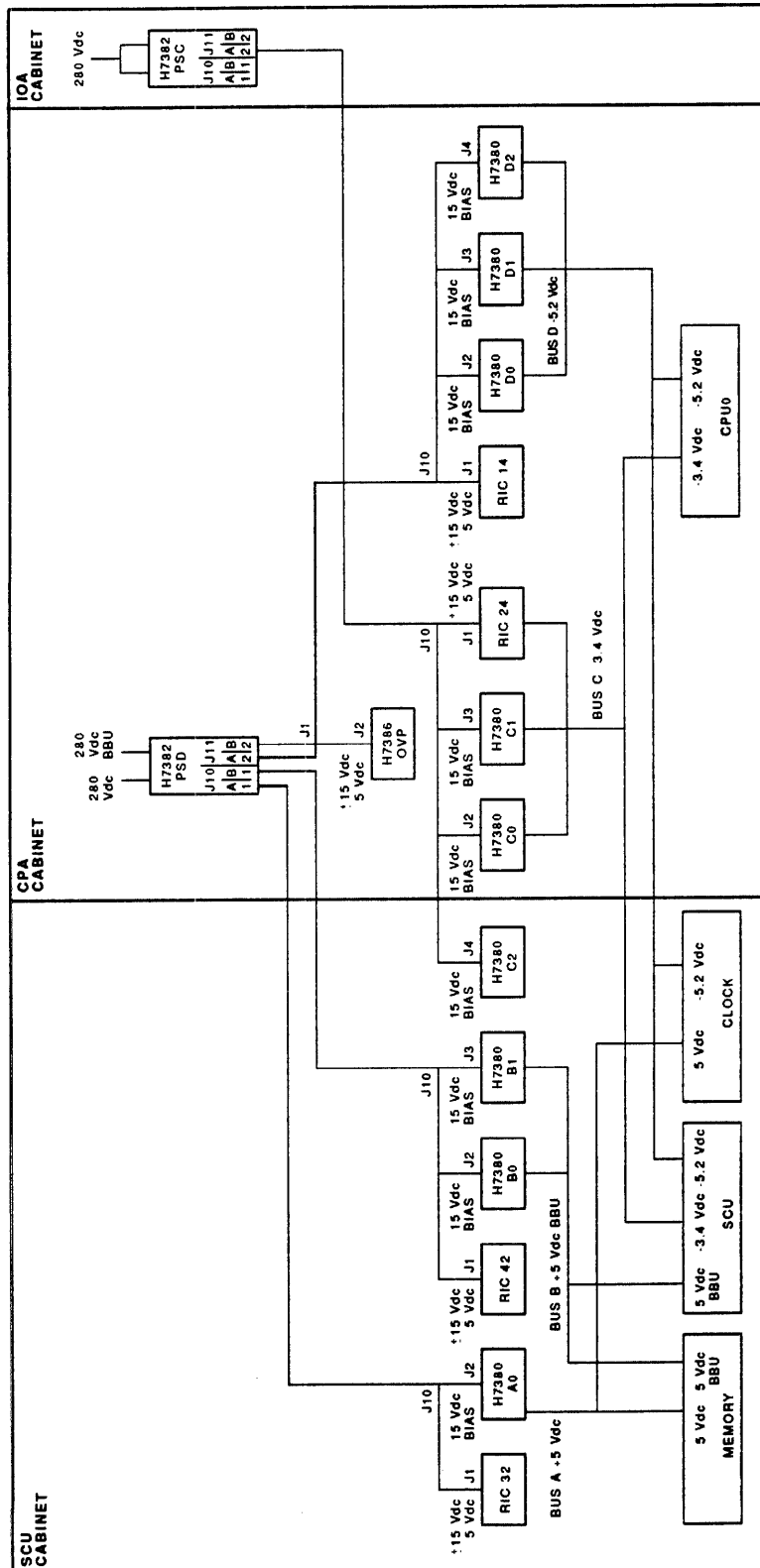
Figure 4–5   Model 210 CPA and SCU Cabinet Low Voltage Distribution

DIGITAL INTERNAL USE ONLY

5

Temperature Sensors and Air Moving Devices

This chapter describes the basic operation of the VAX 9000 temperature sensors and air moving devices (AMDs), including their location and source of power.

5.1 Cooling System Components

Locations of the air movers and temperature sensing devices are shown by system type.

5.1.1 Model 210 Cooling System Components

Figures 2-1, 2-5, 2-7, and 2-8, are repeated in this section for clarity as Figures 5-1 through 5-4. These show the locations of the model 210 air movers and temperature sensors.

The model 210 contains six air movers. All are 550 CFM blowers, except the air mover for the clock and memory: AMD2 in the SCU cabinet, which is a 350 CFM blower.

The IOA cabinet contains one air mover, AMD1, at the top of the cabinet. This air mover cools the contents of the entire cabinet. The air mover pulls air in from the bottom of the cabinet and discharges the heated air out the back of the cabinet.

The CPA cabinet contains two air movers. The bottom air mover, AMD2, pulls air in from the bottom of the cabinet, forcing it over the CPU MCU pin-fins to cool the CPU logic components. The air mover in the top of the cabinet, AMD1, draws on CPU0 exhaust air to cool the power system components. Heated air is discharged through the back door.

The SCU cabinet contains three air movers, with the bottom two air movers drawing air in from the bottom of the cabinet. The bottom air mover, AMD3, cools the SCU logic components by forcing the air over the MCU pin-fins. The middle air mover, AMD2, cools the master clock module and memory modules. The top air mover, AMD1, uses the discharge from the bottom two blowers to cool the power system components. All air is discharged by the top air mover through the back door.

Using a 350 CFM and a 550 CFM air mover seems to feed too much intake air to the top 550 CFM air mover, but the bottom air mover is not running at full capacity, decreasing the volume of intake air.

Except for the IOA cabinet, there is at least a thermistor, temperature sensor, and speed control sensor for each air mover. The IOA cabinet contains a temperature sensor and speed control sensor. There is no thermistor because the I/O RICs do not contain A/D converter hardware to translate the analog voltage to a temperature. Additionally, the SCU cabinet contains an extra thermistor used to measure ambient temperature.
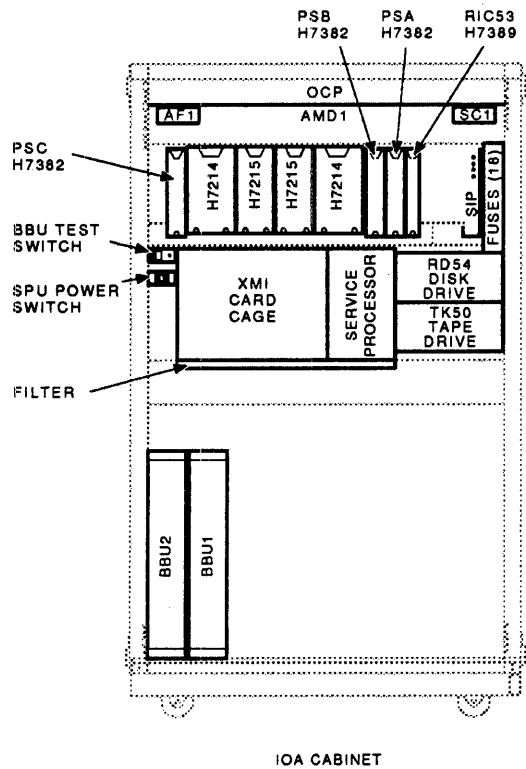
Figure 5-1   VAX 9000 Model 210 IOA Cabinet Configuration (Front View)
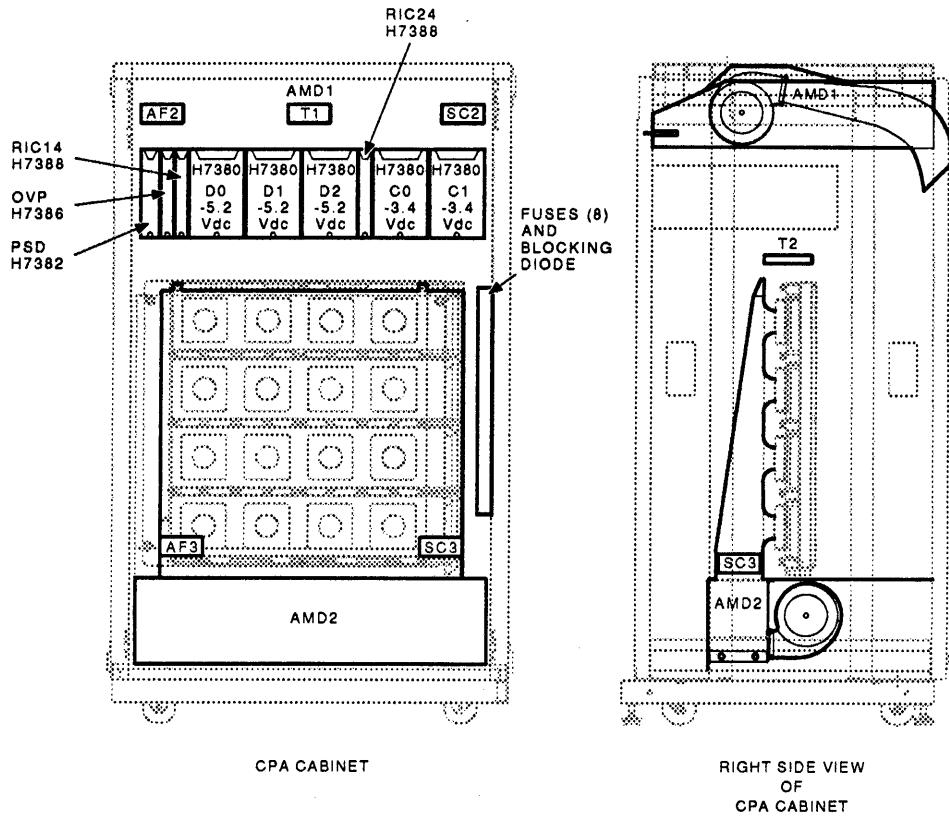
Figure 5-2   VAX 9000 Model 210 CPA Cabinet Configuration (Front and Side View)
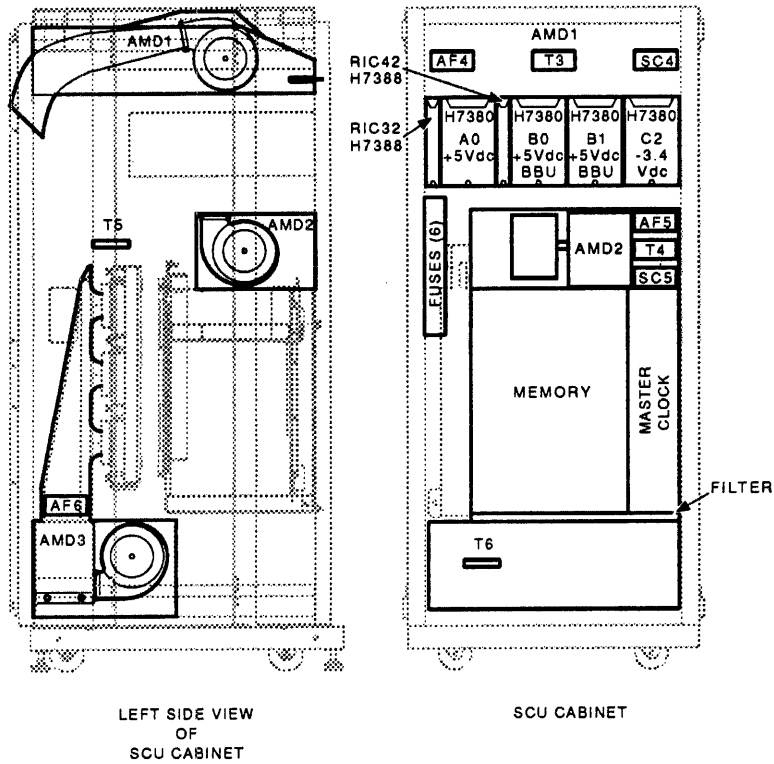
Figure 5–3   VAX 9000 Model 210 SCU Cabinet Configuration (Front View)

AMD1

BACKPANEL
BUS B +5 Vdc BBU

BACKPANEL
BUS A +5 Vdc

SC6 AF6

AMD3

SCU CABINET
REAR VIEW
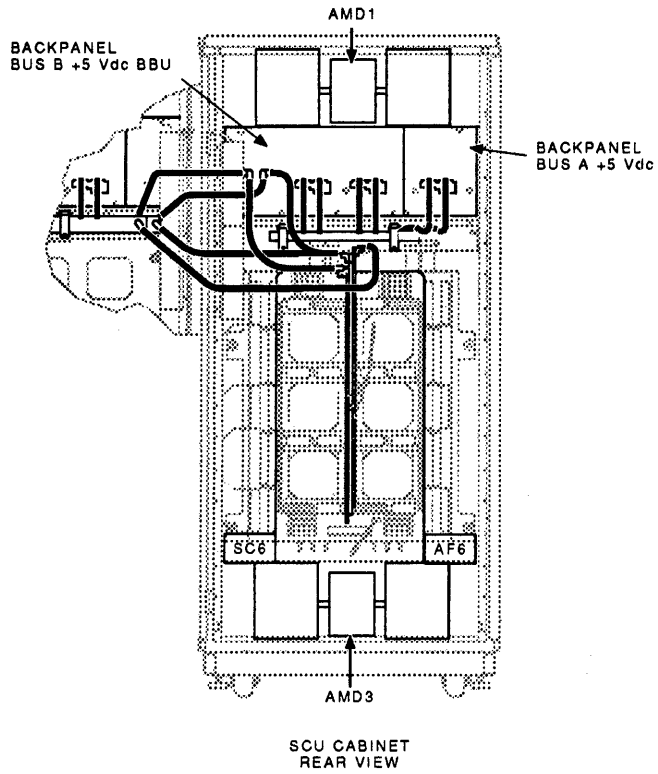
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Figure 5–4   VAX 9000 Model 210 SCU Cabinet Configuration (Rear View)

5.2 Basic Operation of Cooling System Components

Figure 5-5 describes the basic cooling system components, operation, and interaction.
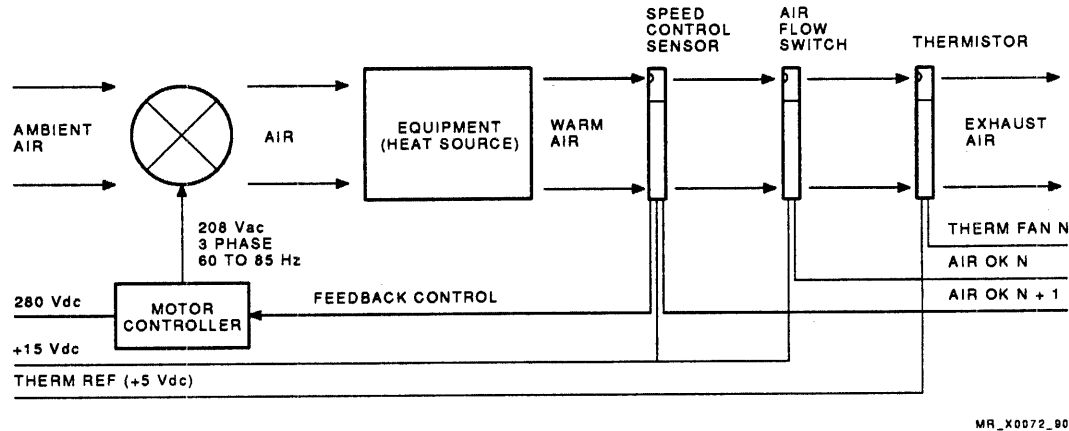
Figure 5-5   Cooling System Block Diagram

5.2.1 Air Movers

The blower impellers of all VAX 9000 air movers are driven by a ¼ Hp 208 Vac 3Ø induction motor. The input frequency is varied between 60 and 85 Hz to control the motor speed. As the frequency increases, the impellers turn faster, increasing the volume of air moved, providing additional component cooling.

All air movers have two impellers, except AMD2 in a model 210, which has one impeller. The capacities range from 350 CFM for the one impeller air mover to 900 CFM for AMD1 in the CPA and CPB cabinets in a model 440. The rest of the air movers have 550 CFM capacity.

Although Figure 5-5 shows the air mover pushing air across the devices to be cooled, they also work by pulling air across the devices. All three temperature sensing devices must be located in the path of air flow, somewhere in the area cooled by the air mover.

5.2.2 Thermistors

The thermistors receive +5 Vdc thermal reference (THERM REF) from the CPU RIC that monitors the thermistor. The thermistor output is an analog voltage proportional to the power dissipated in the thermistor. The thermistor measures the cooling capacity of the air flow: the capacity to dissipate heat, a function of air velocity, temperature, density, and specific heat.

The thermistor output, THERM FAN N, is monitored by a CPU RIC as one of the ASD conditions. The RIC reports any adverse temperature conditions to the PEM. Table 5-1 provides a reference indicating model 210 sensor locations, the source of reference voltages, and which RIC monitors the sensors.

5.2.3 Air Flow Switch

The air flow switch is unidirectional and discriminates between forward and reverse air flow, indicating a fault condition for inadequate or reversed air flow.

The air flow switch receives +15 Vdc from the bias supply that provides power to the RIC, which monitors the air flow switch. The switch is normally closed, opening for fault conditions. The switch output, AIR OK N, is one of the RIC status inputs. The RIC monitors for a fault/no-fault condition.

5.2.4 Speed Control Sensor

The speed control sensor is a dual purpose sensor. One purpose is to generate an analog voltage proportional to the power dissipated in the self-contained thermistor. This voltage is used by the motor controller to vary the speed of the blower motor.

The speed control sensor also contains the same normally closed switch as the air flow switch. It indicates a fault condition for inadequate or reversed air flow to the monitoring RIC. This fault condition is labeled AIR OK N-1 on Figure 5–5.

5.2.5 Motor Controller

The motor controller receives fused 280 Vdc, which it converts to 208 Vac 3Ø to drive the air mover motor. The frequency range (60 to 85 Hz) of the output depends on the feedback control input from the speed control sensors thermistor. If more cooling is required, the motor controller increases the frequency of the output to the air movers motor.

Table 5–1 provides a quick reference for air mover and temperature sensor locations and the source of +15 Vdc and +5 Vdc thermal reference for the thermistors.

Table 5–2 provides a cross-reference between the RIC backpanel signal name and the RIC module signal name for each of the model 210 temperature sensors.

Table 5–1   Model 210 Air Mover and Temperature Sensor Locations and Power Source

Cabinet/ Components Cooled or Monitored	Air Moving Device	Thermistor	Air Flow/ Speed Control Sensor	+15 Vdc Supply	+5 Vdc THERM REF/ Monitoring RIC
IOA/whole cabinet	AMD1	–	AF1, SC1	PSB A1	RIC 53[1]
CPA/power components	AMD1	T1	AF2, SC2	PSC A2	RIC 24
CPA/CPU logic	AMD2	T2	AF3, SC3	PSC A2	RIC 24
SCU/power components	AMD1	T3	AF4, SC4	PSD A2	RIC 14
SCU/memory, clock	AMD2	T4	AF5, SC5	PSD A1	RIC 32
SCU/SCU logic	AMD3	T5	AF6, SC6	PSD A1	RIC 32
SCU/ambient temperature	–	T6	–	PSD B1	RIC 42

[1]RIC 53, an I/O RIC, does not provide +5 Vdc thermal reference. There is no thermistor.

Table 5–2   Model 210 Temperature Sensor Signal Names

Backpanel Signal	RIC Module Signal	CPU RICs SCU Cabinet RIC 32 BUS A	RIC 42 BUS B	RIC 14 BUS D	CPU Cabinet RIC 24 BUS C	I/O RIC IOA Cabinet RIC 53
THERM FAN 2	MEAS 01	T5	–	–	T2	–
THERM FAN 1	MEAS 00	T4	T6	T3	T1	–
AIR OK 4	STATUS05	SC6	–	–	SC3	–
AIR OK 3	STATUS15	AF6	–	–	AF3	–
AIR OK 2	STATUS09	SC5	–	SC4	SC2	–
AIR OK 1	STATUS08	AF5	–	AF4	AF2	–
AF A FAULT H	XMI AIRFLOW A FAULT H	–	–	–	–	AF1
AF B FAULT H	XMI AIRFLOW B FAULT H	–	–	–	–	SC1

6

Power System Functional Description

This section contains the functional descriptions of the VAX 9000 power system.

6.1 Operator Control Panel (OCP)

The operator control panel (OCP) (Figure 6–1) is controlled by the power and environmental monitor (PEM) module, and contains the system power switch, the CPU state LEDs, the startup switch, the service processor access switch, remote access LEDs, and the diagnostic display. The PEM communicates with the OCP through the signal interface panel (SIP).

6.1.1 OCP Power

The OCP receives +5 Vdc from the H7214 that provides power to the service processor unit (SPU). Also, +5 Vdc time-of-year (TOY) power is required. It is provided by BBU 2 by way of the SIP. TOY power is used to maintain the contents of the diagnostic display for up to 100 hours in the case of power loss. This enables the PEM to read the error code after power is reapplied (as long as power is reapplied before the batteries discharge) for error logging. No power is drained from the batteries during normal operation.

H7214 OK from the SPU power supply is routed by the SIP to the OCP. On the OCP, it is used to enable the reception of the data/address lines and the control signals used to read or write the OCP registers, and partially enable the diagnostic display LEDs. H7214 OK is an indication to the SIP and OCP that the PEM has power. If the OCP does not receive this signal, the PEM cannot access the OCP.
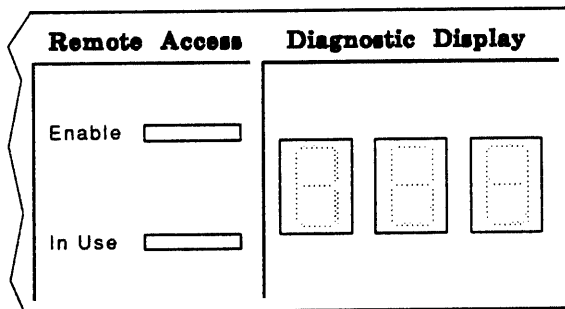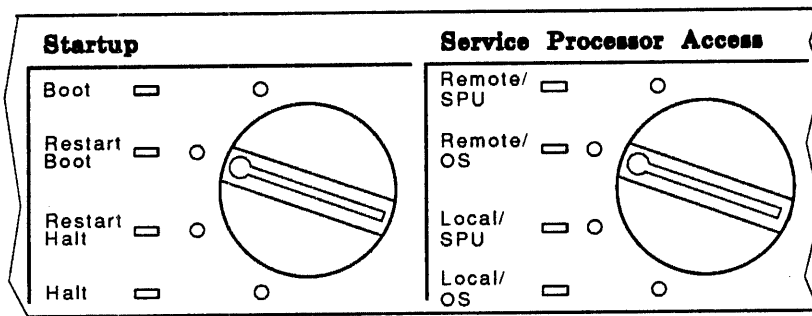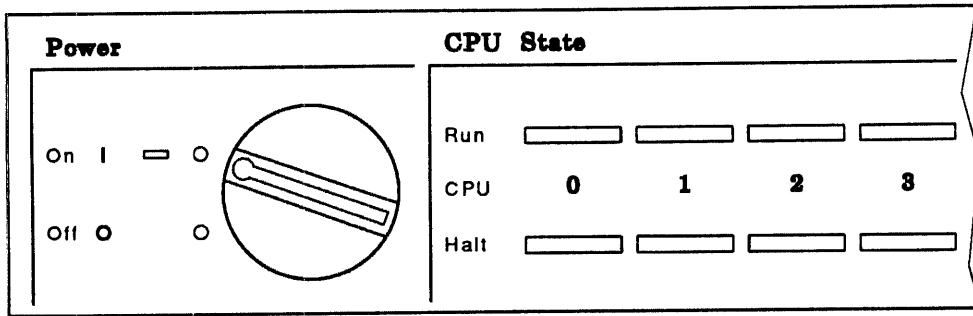
Figure 6–1   Operator Control Panel (OCP)

6.1.2 OCP Interface

The OCP interface consists of four connectors:

1. **J1: SIP OCP PEM (SOP) interface** — A parallel, time-multiplexed data and address bus by which the PEM communicates with the OCP. The bus, and therefore the register reads/writes, is controlled by the strobe, write, and read lines. The signals on the SOP interface are:

   WR SOP L
   RD SOP L
   SOP ADR STB L
   D[07:00] H

2. **J2: system power control cable** — Routes power request and BBU failsafe signals through the power switch (Figure 6–17), and provides the interface to the total off switch sense circuitry (Figure 6–18). LAT TOTAL OFF is latched on the OCP (powered by +5 Vdc TOY) for entry into the error log upon the reapplication of power. The +5 Vdc TOY power from TOY 2 is also carried by this cable.

3. **J3: power cable** — A cable from the SPUs H7214 to provide the +5 Vdc to the OCP. This power is separate from the TOY +5 Vdc.

4. **J4: BBU test connect** — Provides the circuit that enables testing the BBU (Figure 6–17 and Section 6.2.5.1).

6.1.3 PEM Access to OCP Registers

The OCP contains six registers that are accessible to the PEM over the SOP interface. Some are used for the diagnostic display and other LEDs, while others are used to read the position of the switches.

6.1.3.1 OCP Register Writes

The PEM writes the OCP registers (Figure 6–2) by:

1. Asserting the 4-bit register address (D[03:00]) on D[07:00] data and address lines. D[07:06] must be zero, and D[05:04] are not used.

   NOTE
   Data bit 7 must be zero. It is ANDed with H7214 OK to enable decoding the address. Also, the diagnostic display LEDs are enabled by address bit 6 equal to zero, ANDed with H7214 OK. If address bit 6 is asserted, the state of the diagnostic display (DD) LEDs cannot change.

2. Asserting, then deasserting SOP ADR STB L to strobe the address into the address holding register.

3. Asserting a byte of data on the D[07:00] lines. Simultaneously, WR SOP L (becomes WR L) is asserted low. This completes enabling the address decode, which generates a write pulse for the selected register.
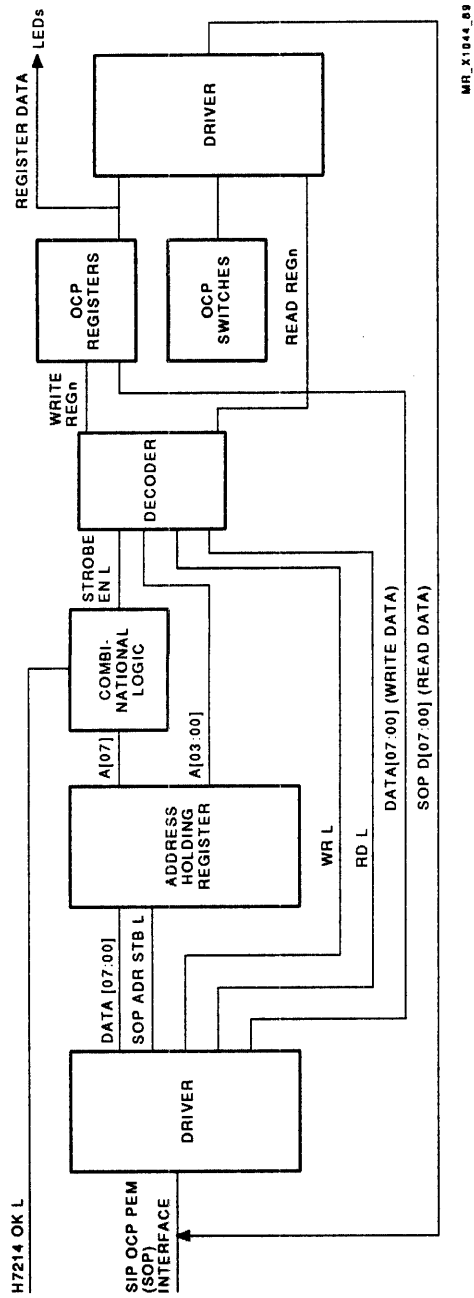
Figure 6–2   OCP Register Read/Write

6.1.3.2 OCP Register Reads

See Figure 6–2. The PEM reads the OCP registers by:

1. Asserting the 4-bit register address [D[03:00]] on D[07:00] data and address lines. D[07:06] must be zero, and D[05:04] are not used.

   NOTE
   Data bit 7 must be zero. It is ANDed with H7214 OK to enable decoding the address. Also, the diagnostic display LEDs are enabled by address bit 6 equal to zero, ANDed with H7214 OK. If address bit 6 is asserted, the state of the DD LEDs cannot change.

2. Asserting, then deasserting SOP ADR STB L to strobe the address into the address holding register for decoding.

3. Asserting RD SOP L (becomes RD L) low to cause the address to be decoded. READ REGx enables the driver for the selected register or switch to place the read data on the SOP interconnect D[07:00] lines.

6.1.4 OCP Registers

The OCP registers are listed in Table 6–1 and shown in Figure 6–3.

Table 6–1 OCP Registers

Register	SOP Address	Name	Access	Mnemonic
0[1]	00	Display high byte register (left)	R/W	DISHBREG[2]
1[1]	01	Display middle byte register (center)	R/W	DISMBREG[2]
2[1]	02	Display low byte register (right)	R/W	DISLBREG[2]
3	03	CPU A LED register	R/W	CPALEDREG[3]
4	04	CPU B LED register	R/W	CPBLEDREG[3]
5	05	Keyswitch LED register	R/W	SWLEDREG[4]
6	06	Latched status register	R/W	LATSTATREG[4]

[1]Address bit 6 deasserted and H7214 OK are required to enable the diagnostic display LEDs.

[2]The display registers are examined with the command: EXAMINE/PEM OCPDISREG.

[3]The LED registers are examined with the command: EXAMINE/PEM OCPLEDREG.

[4]The keyswitch registers and latched status register are examined with the command: EXAMINE/PEM OCPSWREG.
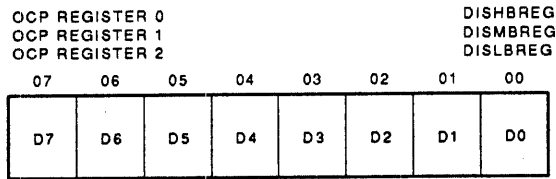
```
OCP REGISTER 0                        DISHBREG
OCP REGISTER 1                        DISMBREG
OCP REGISTER 2                        DISLBREG
   07    06    05    04    03    02    01    00

  ┌─────┬─────┬─────┬─────┬─────┬─────┬─────┬─────┐
  │     │  .  │     │     │     │     │     │     │
  │ D7  │ D6  │ D5  │ D4  │ D3  │ D2  │ D1  │ D0  │
  │     │     │     │     │     │     │     │     │
  └─────┴─────┴─────┴─────┴─────┴─────┴─────┴─────┘

NOTE: D7 MAY BE WRITTEN/READ, BUT IS NOT USED
TO LIGHT THE DD LEDs.
                              MR_X1045_89
```

Figure 6-3   OCP Diagnostic Display Registers

OCP registers 0, 1, and 2 contain the data needed to turn on the diagnostic display LEDs. Register 0 is the high byte, and provides the data for the left LED. Register 1 is for the middle LED, while register 2, the least significant byte, provides the data for the right LED.

Each of these registers are 8-bit read/write registers, but only 7 bits drive the diagnostic display LEDs. The registers and DD LEDs are powered by +5 Vdc TOY power. Therefore, the LEDs hold the error number until the registers are reset by being written to zeros or TOY power is lost. See Appendix B for a list of the DD codes.

NOTE
Address bit 6 has to be zero and H7214 OK asserted to enable changing the DD LEDs.

Register 3, CPU A LED register Figure 6-4, contains the halt, run, and legend bits for CPU0 and CPU1. These bits, when set, turn on the corresponding LEDs. The legend LED indicates that the CPU is present; halt indicates that the CPU has been initialized; and run indicates that the CPU is running macrocode.

Additionally, the other two bits indicate the status of the remote terminal. REMOTE ENABLE is set if the service processor access switch is in either the REMOTE SPU or REMOTE OS position. REMOTE IN USE is set if carrier has been received from the remote modem.
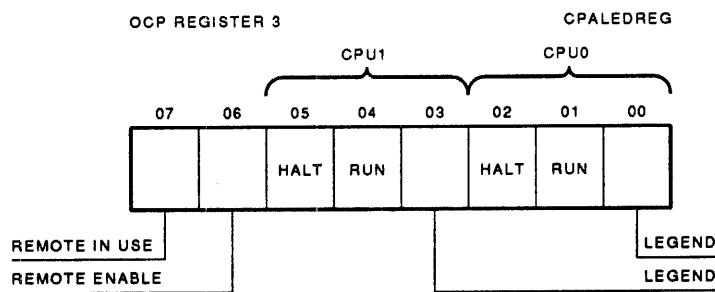
```
     OCP REGISTER 3                      CPALEDREG
                        CPU1              CPU0
                      ┌────────┐       ┌────────┐
     07    06    05    04    03    02    01    00

  ┌─────┬─────┬─────┬─────┬─────┬─────┬─────┬─────┐
  │     │     │     │     │     │     │     │     │
  │     │     │HALT │ RUN │     │HALT │ RUN │     │
  │     │     │     │     │     │     │     │     │
  └──┬──┴──┬──┴─────┴─────┴──┬──┴─────┴─────┴──┬──┘
REMOTE IN USE │              │                 │ LEGEND
─────────────┘               │                 ──────────
REMOTE ENABLE ───────────────┘              LEGEND

                              MR_X1046_89
```

Figure 6-4   CPU A LED Register

Register 4 is identical to register 3 except it refers to CPU2 and CPU3 (Figure 6–5). Bits [07:06] are spare bits, but can be written and read.

Register 5 bits indicate the positions of the startup keyswitch and the service processor access keyswitch (Figure 6–6). The PEM reads the register to determine the position of the switches, then writes the register to turn on the corresponding LED.

Register 6 contains four bits of information (Figure 6–7).
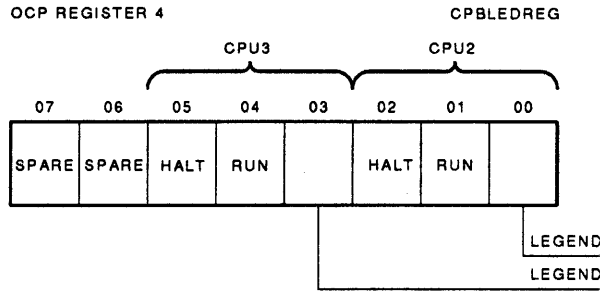
NOTE: BITS 6 AND 7 CAN BE WRITTEN AND READ,
BUT DO NOT DRIVE A LED.

MR_X1047_89

Figure 6–5   CPU B LED Register
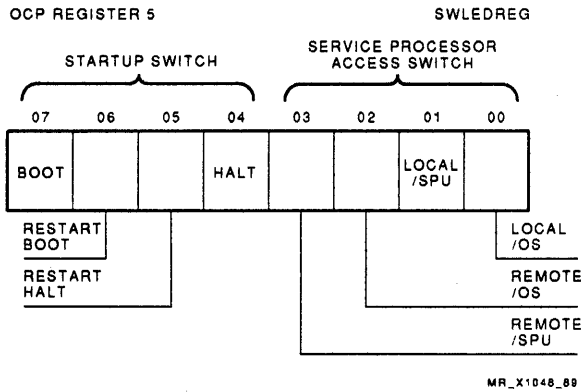
MR_X1048_89

Figure 6–6   Keyswitch LED Register
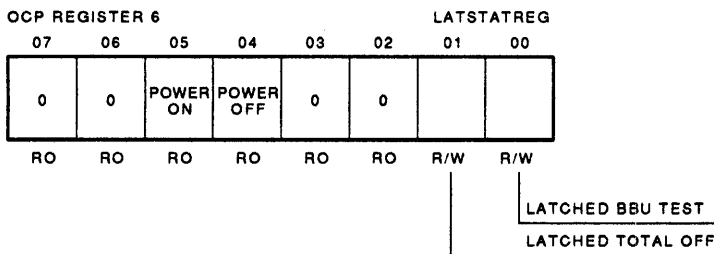
MR_X1049_89

Figure 6–7   Latched Status Register

LATCHED BBU TEST (Bit 00) — This bit indicates that the BBU test switch has been activated. The bit is powered by +5 Vdc TOY power, and remains set as long as TOY power is available. The PEM reads this bit for inclusion in the error log. This is necessary because it indicates that the system was powered down for a test, not a loss of power. This bit is reset by the PEM writing this bit, or TOY reset, generated after TOY power is lost then regained.

The flip-flop is shown in Figure 6–17. The BBU failsafe circuit is explained in Section 6.2.5.

LATCHED TOTAL OFF (Bit 01) — This bit indicates that a total off condition exists due to total off switch activation. It is an individual D-type flip-flop powered by +5 Vdc TOY. If set, this bit remains set as long as TOY power is available. When power is returned to normal, the PEM is able to read this bit for the error log entry. Normally it is reset by being written to a zero by the PEM. It is also reset on loss of TOY power. The flip-flop is shown in Figure 6–18. The total off circuit is explained in Section 6.2.7.

POWER ON/POWER OFF (Bits 05:04) — These read-only bits indicate the position of the power switch. A digital ground is connected to the power on/off switch. The ground is routed to the bit corresponding to the current switch position. If the switch is on, bits [05:04] are on. If the switch is off, bits [05:04] are 10.

6.1.5 Startup Keyswitch

The different positions of the startup keyswitch indicates to the SPU how to start the system. The keyswitch position is available to the PEM by reading SWLEDREG [07:04]. The positions of the keyswitch and the action taken is shown in Table 6–2.

Table 6–2   Startup Keyswitch Positions

Keyswitch Position	Action
Boot	Upon application of power, the system attempts a boot operation. If it fails, the system enters console I/O mode.
Restart Boot	Upon application of power, the system attempts to restart the operating system. If the restart fails, the system is booted. If that fails, the system enters console I/O mode.
Restart Halt	Upon application of power, the system attempts to restart the operating system. If the restart fails, the system enters console I/O mode.
Halt	Upon application of power, the system initializes the VAX processor and enters console I/O mode.

6.1.6 Service Processor Access Keyswitch

The service processor access keyswitch controls access to the system for the service processor and the remote terminal. The switch has four positions as shown in Table 6-3.

Table 6-3 Service Processor Access Keyswitch Positions

Keyswitch Positions	Action
Local/OS	The SPU behaves as a user terminal, passing $\boxed{\text{CTRL/P}}$ to the VAX processor as a normal character. The remote terminal is disabled.
Local/SPU	The service processor intercepts $\boxed{\text{CTRL/P}}$ and enters console I/O mode. The remote terminal is disabled.
Remote/OS	This position allows the local and remote terminal to access the VAX processor as a user terminal. Console I/O mode is not allowed.
Remote/SPU	This state allows both the local and remote terminals to access console I/O mode by typing $\boxed{\text{CTRL/P}}$.

6.1.7 Power Keyswitch

The power on/off switch is used to apply or remove power to the entire system. The switch routes a power request to the H7390 or H7392s to enable a power-up sequence.

Additionally, it is part of the circuit used to energize the BBU failsafe relay, the relay that enables but does not turn on the BBU. If all switches and breakers are initially closed, battery backup is enabled. If there is a subsequent power loss, battery backup power is used. If any of the switches or breakers in the circuit is opened, the enable for BBU is dropped, and battery backup power is not made available.

See Section 6.2.5 for a discussion of battery backup enable. The power switch is shown in Figure 6-17.

6.2 Signal Interface Panel (SIP)

The signal interface panel (SIP) (Figure 6-8) provides a common point of signal interconnection for the power system. It provides the logic required to support battery backup operation, total off, and SPU regulator control. It provides an interface between the PEM, RICs, OCP, H7392 or H7390, H7231 battery backup units, and SPU H7214/H7215 regulators. It also provides the power system clocks.

The SIP includes the SIP, OCP, and PEM interface (SOP interface), and the registers that allow the PEM and SIP to communicate. There are also four LEDs for monitoring BBU and H7214/H7215 status.

6.2.1 SIP Power Distribution

The SIP uses +5 and ±15 Vdc. For the VAX 9000 model 400 systems, these voltages are provided by H7382 bias supply PSE, located in the IOA cabinet. In the VAX 9000 model 210, the power is provided by H7382 bias supply PSA located in the IOA cabinet.

Most of the SIP logic uses +5 Vdc. The -15 Vdc is used for the BBU failsafe relay. The following circuitry uses +15 Vdc:

> Total off relays
> H7214/H7215 enabling circuit
> BBU control and status circuit

The SIP also routes +15 Vdc bias to the SPU H7214/H7215, TOY2 +5 Vdc to the OCP, TOY1 +5 Vdc to the SPU time-of-year circuitry, and +5 Vdc to all three RICBUSes for RICBUS power.

Other voltages used on the SIP include:

> +48 Vdc — From each BBU for the BBU failsafe feed circuit
> +7.5 Vdc — From each H7392 or the H7390 for total off feed circuits
> +15 Vdc — From each H7392 or the H7390 for the power control buses

The SIP may be divided into the major blocks shown in Figure 6-8.


```
┌─────────────┐        ┌─────────────┐      (R)  BBU1 STAT
│     SIP     │        │     BBU     │
│  REGISTERS  │        │  INTERFACE  │      (R)  BBU2 STAT
│             │        │   CONTROL   │
└─────────────┘        └─────────────┘      (G)  H7214 OK

┌─────────────┐        ┌─────────────┐      (G)  H7215 OK
│  SIP, OCP,  │        │ H7214/H7215 │
│  PEM (SOP)  │        │ (SPU POWER) │
│  INTERFACE  │        │   CONTROL   │
│             │        │AND MONITORING│
└─────────────┘        └─────────────┘

┌─────────────┐        ┌─────────────┐      ┌─────────────┐
│   AC/DC LO  │        │    POWER    │      │    TOTAL    │
│  MONITORING │        │    SYSTEM   │      │     OFF     │
│   CIRCUITS  │        │    CLOCKS   │      │  CIRCUITRY  │
└─────────────┘        └─────────────┘      └─────────────┘
```
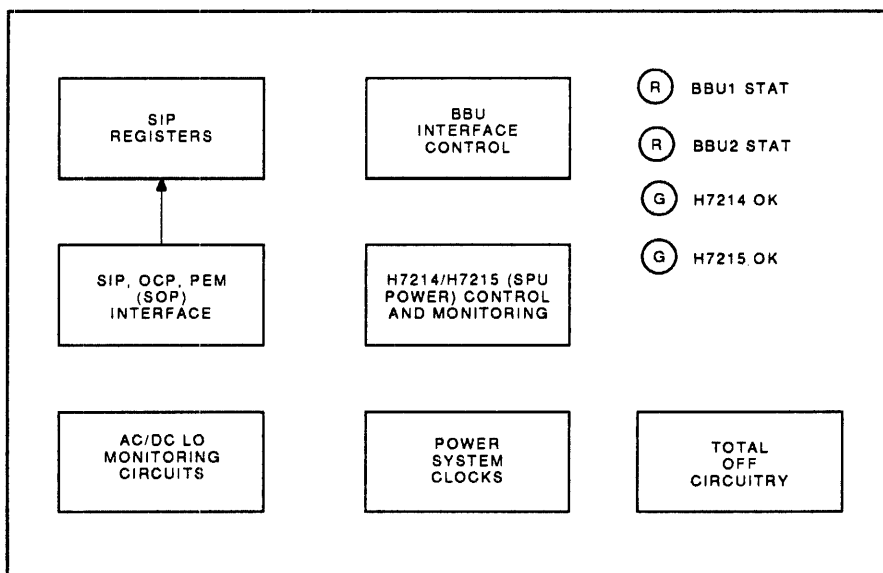
MR_X1050_89

Figure 6-8   SIP Simplified Block Diagram

6.2.2 SIP Register Access

The SIP contains eight registers accessible to the PEM over the SOP interface. Those registers that are write-only are used for enabling or testing. The read-only registers provide the PEM with status signals.

6.2.2.1 SIP Register Writes

The PEM uses the PEM SOPCNTRL and SOPDATA registers to control the SOP bus and write and read the SIP registers (Figure 6–9). The following SOP bus sequence writes to the SIP registers.

1. Register address bits (SOP D[02:00]) are asserted to select the address. D[07] is asserted to enable decoding the SIP register address.

2. The PEM asserts, then deasserts STROBE to load the address into the address holding register.

3. Data bit 7 partially enables decoding the address. The SPU BI H7214 must assert H7214 OK L. This is an indication to the SIP that the PEM is powered up. These two signals D[07] and H7214 OK L enable decoding the address when the write signal is asserted.

    NOTE
    TEST PWRFAIL L generates the enable when testing the SIP to PEM interface. One of the test conditions inverts H7214 OK L. With the deassertion, the PEM would not be able to read the SIP registers. TEST PWRFAIL L is asserted prior to the test to compensate for the inversion of H7214 OK L.

4. The PEM asserts a byte of data on the D[07:00] lines. Simultaneously, WR SOP L (becomes WR L) is asserted low. This completes the enabling of the address, with the subsequent generation of a write pulse to the selected register gating the write data into the register.

6.2.2.2 SIP Register Reads

See Figure 6–9. The SIP registers are read according to the following sequence:

1. The PEM asserts the 3-bit register address, SOP D[02:00], along with SOP D[07], which must be asserted to enable decoding of the address.

2. The PEM asserts, then deasserts SOP ADR STB L to load the address into the address holding register for decoding.

3. H7214 OK L must be asserted. It is ANDed with D[07] to generate EN L, which partially enables the address decode. TEST PWRFAIL L can also generate EN L. See the note in Section 6.2.2.1.

4. RD SOP L (becomes RD L) is asserted to complete the address decoding, which enables the selected register data onto SOP D[07:00].
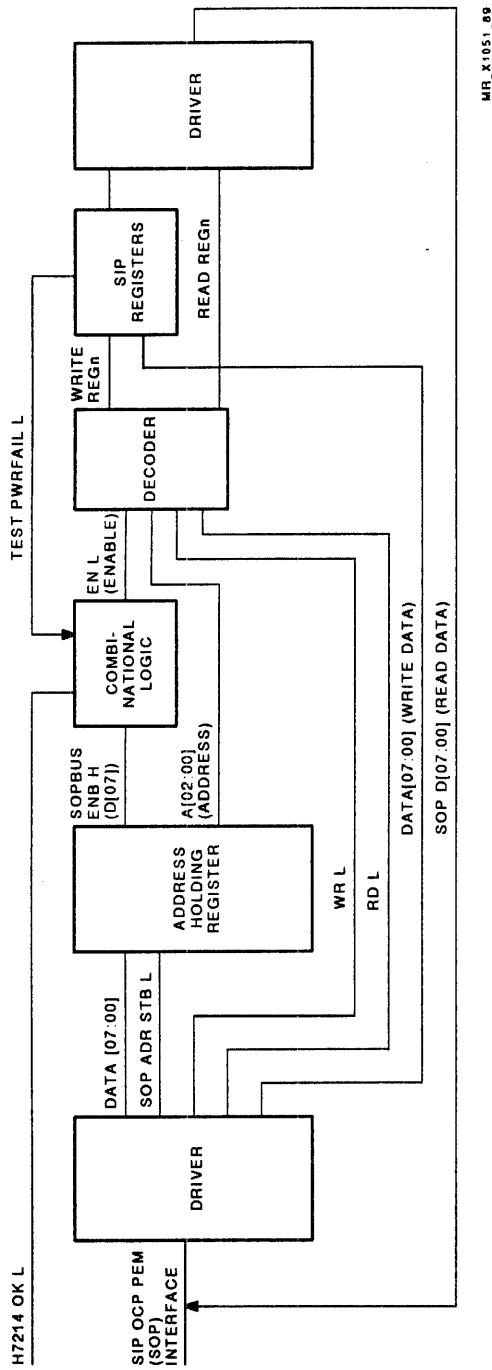
Figure 6–9   SIP Register Read/Write

6.2.2.3 SIP Registers

When examining a SIP register, you are not directly accessing the SIP hardware, but the PEMs interpretation of the SIP register. In some cases, there are differences between the actual hardware registers, and what the PEM indicates the register contains. Also, some SIP registers are write-only registers, but in the PEM, they are read/write. If you were to write one of these registers and then read it, you would read from the PEM what the PEM wrote to the SIP register. For more information on the SIP registers, see Chapter 7, Power Control Subsystem and PCS Communication.

The SIP registers are listed in Table 6–4. Refer to Figures 6–10 through 6–16 and Tables 6–5 through 6–11.

The register bit names are the same for model 210 and model 400 systems but the definitions of the bits in the bias register and keying registers are different for the two systems. Therefore, the tables describing the register bits differ for these three registers.

Table 6–4   SIP Registers

Number	SOP Address	Name	Access	Mnemonic
0	80	Test1 register	WO	TSTREG1
1	81	Test2 register	WO	TSTREG2
2	82	Test control register	WO	TSTCNTL
3	83	Battery backup unit register	R/W	BBUREG
4	84	Bias register	RO	BSCREG
5	85	Keying A and B register	RO	KEYABREG
6	86	Keying B and C register	RO	KEYBCREG

SIP REGISTER 0   TSTREG1

07	06	05	04	03	02	01	00
		TST ACLO2 H	TST ACLO1 H	TST H7215 OT H	TST TOFFC H	TST TOFFB H	TST TOFFA H

TST BUSLO1 H
TST BUSLO2 H

MR_X1052_89
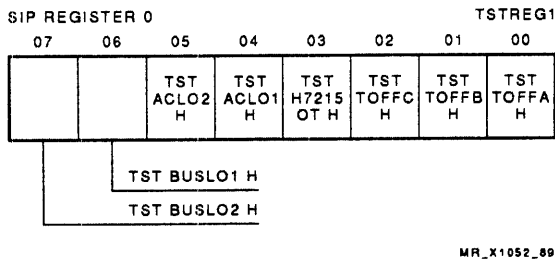
Figure 6–10   SIP Test1 Register

Table 6–5   Test1 Register

Bit Number	Signal Name	Description
00	TST TOFFA H	This test bit is set by the PEM to invert the total off line for RICBUS A. Total off would normally be asserted by an H7380 overtemperature (CPU RIC), XMI H7215 overtemperature (I/O RIC), H7392 unbalanced condition or H7392 thermal fault (I/O RIC), or any automatic shutdown (ASD) condition.
01	TST TOFFB H	Set by the PEM to invert the total off line for RICBUS B.
02	TST TOFFC H	Set by the PEM to invert the total off line for RICBUS C.
03	TST H7215 OT H	Set by the PEM to invert H7215 OT from the SPU BI H7215 regulator.
04	TST ACLO1 H	Set by the PEM to invert AC LO on RICBUS A (from H7392 1 or H7390).
05	TST ACLO2 H	Set by the PEM to invert AC LO on RICBUS C (H7392 2).
06	TST BUSLO1 H	Set by the PEM to invert BUS LO on RICBUS A (loss of 280 Vdc from H7392 1 or the H7390).
07	TST BUSLO2 H	Set by the PEM to invert BUS LO on RICBUS C (loss of 280 Vdc from H7392 2).

```
SIP REGISTER 1                                    TSTREG2
   07      06      05      04      03      02      01      00
 ┌──────┬──────┬──────┬──────┬──────┬──────┬──────┬──────┐
 │      │      │ TST  │ TST  │ TST  │ TST  │ TST  │ TST  │
 │      │      │H7215 │H7214 │ BBU  │GRP C │GRP B │GRP A │
 │      │      │ OK H │ OK H │ GRP  │ LO H │ LO H │ LO H │
 │      │      │      │      │ LO H │      │      │      │
 └──────┴──────┴──────┴──────┴──────┴──────┴──────┴──────┘
   └──────┬──────┘
   NOT CONNECTED
                                          MR_X1053_89
```
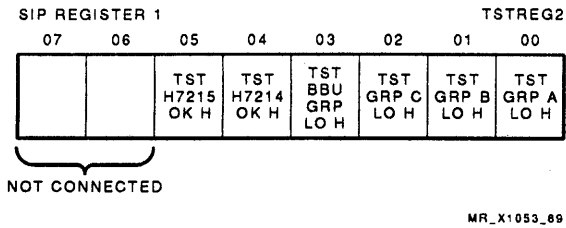
Figure 6–11   SIP Test2 Register

Table 6–6   Test2 Register

Bit Number	Signal Name	Description
00	TST GRP A LO H	Asserted by the PEM to invert GRP A LO from RICBUS A (any RIC on RICBUS A detects that the bus voltage is less than 95% of normal bus voltage).
01	TST GRP B LO H	Asserted by the PEM to invert GRP B LO from RICBUS B (any RIC on RICBUS B, except RIC 41 [model 400 systems] or RIC 42 [model 210], which monitor +5 Vdc BBU).
02	TST GRP C LO	Asserted by the PEM to invert GRP C LO from RICBUS C.
03	TST BBU GRP LO H	Asserted by the PEM to invert BBU GRP LO (+5 Vdc BBU is less than 95%).
04	TST H7214 OK H	Asserted by the PEM to invert H7214 OK from the SPU H7214 (LED on SIP changes state).
05	TST H7215 OK H	Asserted by the PEM to invert H7215 OK from the SPU H7215 (LED on SIP changes state).
06	Not connected	–
07	Not connected	–

MR_X1054_89
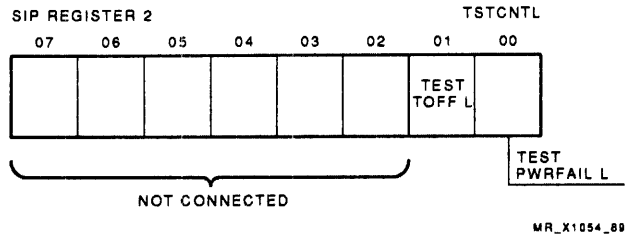
Figure 6–12 SIP Test Control Register

Table 6–7 Test Control Register

Bit Number	Signal Name	Description
00	TEST PWRFAIL L	Prevents sending an enable to the BBU, and MCM SPU DCLO and MCD PWR BAD to the master clock module (MCM) during tests. MCM SPU DCLO prevents changing clock control registers. MCM PWR BAD resets the master clock module. The assertion also disables the following BI signals: BI ACLO L, BI DCLO L, BI RESET L, and the following SPM interrupts: DCLO1 INT L, DCLO2 INT L, ACLO1 INT L, ACLO2 INT L, and SPU RCV TRANS SC INTS L.
01	TEST TOFF L	Used during tests to prevent asserting total off and the subsequent tripping of the H7392 or H7390 breakers.
02	Not used	–
03	Not used	–
04	Not used	–
05	Not used	–
06	Not used	–
07	Not used	–

```
SIP REGISTER 3                                          BBUREG
  07      06      05      04      03      02      01      00
┌───────┬───────┬───────┬───────┬───────┬───────┬───────┬───────┐
│ BBU   │       │ BBU2  │       │ BBU1  │       │ BBU2  │ BBU1  │
│ ENB H │   0   │ STAT  │   0   │ STAT  │   0   │ AVL H │ AVL H │
│       │       │  H    │       │  H    │       │       │       │
└───────┴───────┴───────┴───────┴───────┴───────┴───────┴───────┘

                                           MR_X1055_89
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Figure 6–13   SIP Battery Backup Register

Table 6–8   Battery Backup Register

Bit Number	Signal Name	Description
00	BBU1 AVL H	BBU 1 is ready to provide backup power.
01	BBU2 AVL H	BBU 2 is ready to provide backup power.
02	NA	Read as 0.

03	BBU1 STAT H[1]	The H7231 battery status and the state of the red BBU1 stat LED (if the bit is set, the LED is on):
		
		 • OFF (LED is off): BBU is not available.
		
		 • READY
		
		     LED is lit: System is ready to provide backup power.
		     LED blinks at a 1 Hz rate: Charging.
		
		 • ON (LED blinks at a 10 Hz rate): Discharging.

04	NA	Read as 0.
05	BBU2 STAT H [1]	Same as bit 3 except for BBU 2.
06	NA	Read as 0.
07	BBU ENB H	The BBU has been enabled to assume the ready state.

[1]The one bit for battery status in the BBUREG becomes two bits in the BBU status byte of the PEM state register. As these BBUREG bits may be changing (LED blinking), the PEM reads the BBUREG multiple times to determine the actual state of the battery backup. It then sets two bits in the PEM state register to specify the state of the BBU when the SIP BBUREG was last read.

SIP REGISTER 4   BSCREG

07	06	05	04	03	02	01	00
		SIP BIASB OK L	SIP BIASA OK L	H7215 OK L	H7214 OK L	0	0

RICBUS BIASA OK L

RICBUS BIASB OK L

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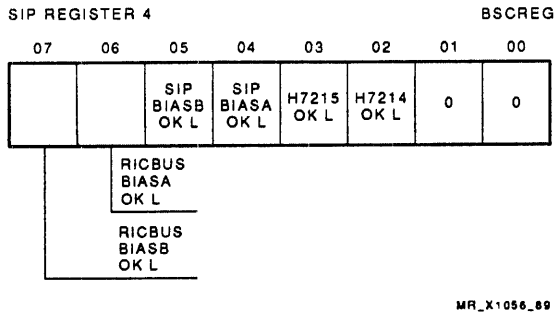
Figure 6–14   SIP Bias Register

Table 6–9   Model 210 Bias Register

Bit Number	Signal Name	Description
00	Not connected	–
01	Not connected	–
02	H7214 OK L	The status of the SPU H7214, and the state of the H7214 OK green LED.
03	H7215 OK L	The status of the SPU H7215, and the state of the H7215 OK green LED.
04	SIP BIASA OK L	PSA A2 BIAS OK. Provides SIP power and SPU H7214/H7215 bias.
05	SIP BIASB OK L	PSA B2 BIAS OK. Provides SIP power and SPU H7214/H7215 bias.
06	RICBUS BIASA OK L	PSA A1 BIAS OK. Provides RICBUS power.
07	RICBUS BIASB OK L	PSA B1 BIAS OK. Provides RICBUS power.

SIP REGISTER 5   KEYABREG

07	06	05	04	03	02	01	00
RBB KEY3 OK L	RBB KEY2 OK L	RBB KEY1 OK L	RBA KEY5 OK L	RBA KEY4 OK L	RBA KEY3 OK L	RBA KEY2 OK L	RBA KEY1 OK L
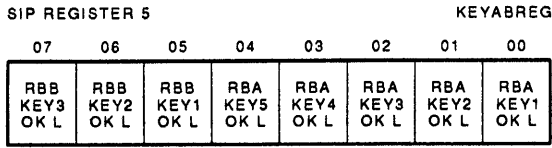
MR_X1057_89

Figure 6-15   SIP Keying A and B Register

SIP REGISTER 6   KEYBCREG

07	06	05	04	03	02	01	00
0	RBC KEY5 OK L	RBC KEY4 OK L	RBC KEY3 OK L	RBC KEY2 OK L	RBC KEY1 OK L	RBB KEY5 OK L	RBB KEY4 OK L
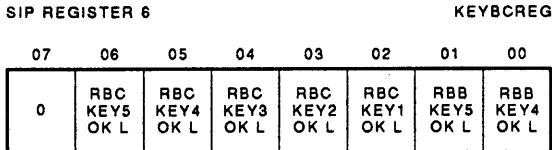
MR_X1058_89

Figure 6-16   SIP Keying B and C Register

Table 6-10   Model 210 Keying A and B Register

Bit Number	Signal Name	Description
00	RBA KEY1 OK L	RIC 15 installed
01	RBA KEY2 OK L	RIC 25 installed
02	RBA KEY3 OK L	RIC 54 installed
03	RBA KEY4 OK L	Not connected
04	RBA KEY5 OK L	Not connected
05	RBB KEY1 OK L	RIC 42 installed
06	RBB KEY2 OK L	RIC 32 installed
07	RBB KEY3 OK L	RIC 53 installed

Table 6-11   Model 210 Keying B and C Register

Bit Number	Signal Name	Description
00	RBB KEY4 OK L	RIC 14 installed
01	RBB KEY5 OK L	RIC 24 installed
02	RBC KEY1 OK L	Not connected
03	RBC KEY2 OK L	Not connected
04	RBC KEY3 OK L	Not connected
05	RBC KEY4 OK L	Not connected
06	RBC KEY5 OK L	Not connected
07	NA	Read as 0

6.2.3 Power System Clocks

An 11.059 MHz oscillator on the SIP generates the 162.5 kHz and 32.5 kHz clocks needed by the power system. These clocks are routed over the RICBUSes to the RICs for transfer to the H7380, H7214, and H7215 power converters. The H7380 converters use 162.5 kHz clock, while the H7214 and H7215 converters use 32.5 kHz clock. The SPU H7214 and H7215 converters receive the clock directly from the SIP. Also, each of the clocks is routed to the PEM so that during system initialization the PEM can verify that the clocks are being generated.

An oscillator on each RIC generates clocks that back up the SIP clocks for the power bus that the RIC is monitoring. If the SIP clock is lost, the RIC clock keeps the converters synchronized. See Section 6.10.2.9 or Section 6.10.3.1 for more information on the RIC generated clocks.

6.2.4 SPU Power, Control, and Monitoring

Two things are necessary to deassert H7214 CH INHIBIT H, enabling the SPU H7214:

*   SPU power switch is closed.

*   Bias supplies that power the SIP and provide bias power to the SPU H7214 and H7215 are operational.

When the H7214 voltage outputs are within tolerance, the assertion of H7214 OK at the SIP causes deassertion of H7215 CH INHIBIT H to enable the H7215.

When the SPU power switch is opened, the PEM is informed of an impending power loss, causing the PEM to initiate a BI power-down sequence. After a 63 ms delay, H7214 CH INHIBIT H is asserted to disable the H7214. When H7214 OK is deasserted, H7215 CH INHIBIT H is asserted to disable H7215.

The H7214 and H7215 provide the SIP with H7214 OK L and H7215 OK L if their outputs are within regulation. These signals are used on the SIP to:

> Illuminate LEDs to indicate the status of the SPU BI power
> Monitor for DC LO
> Provide enabling for register read/writes.

H7214 OK L is routed to the OCP where it also enables the register read/write circuitry.

6.2.5 BBU Interface and Control

The SIP contains the circuitry that indicates the status of the BBUs, allows testing battery backup capability, and allows the SPU (through the PEM) to control each of the H7231 BBU units.

Additionally, the TOY power from each BBU unit is used. The +5 Vdc TOY voltages are routed through the SIP to their destination. TOY1 +5 Vdc, from BBU1, is routed to the SPU BI backpanel, and powers the SPU time-of-year circuitry on the service processor module. TOY2 +5 Vdc, from BBU2, powers the diagnostic display LEDs on the OCP.

The battery backup interface signals are:

*   **Battery backup enable** — When the PEM sets BBUREG 07, BBU ENB (Figure 6–13), it is routed to the H7231s and if the BBU failsafe circuit is closed, enables the power relays to energize when they receive legitimate ac power. The H7231s are enabled to assume the ready state. See the description of BBU FAILSAFE ENA.

- **BBU failsafe enable** — The failsafe enable circuit provides a complete circuit for +48 Vdc battery voltage to energize the battery backup power relay, when enabled by battery backup enable (BBU ENB) and the presence of ac power. This circuit is made if the following switches/circuit breakers are closed (Figure 6–17):

  > H7292 2 A1-CB1
  > H7392 1 A1-CB1 or H7390 CB1
  > Total off switch
  > OCP power keyswitch (in parallel with the BBU test switch)

  NOTE
  If there is an H7390 or only one H7392 installed, a jumper plug (29-02426-01) is installed on SIP J6 to jumper J06-05 to J06-04 bypassing the contacts of H7392 2 A1-CB1.

  If power is lost due to the OCP power switch being turned off or any of the circuit breakers being manually tripped, the failsafe enable circuit opens, preventing the use of battery backup power.

- **Battery backup available** — After the H7231s have been enabled and are capable of providing battery power, each BBU asserts battery backup available (BBUA).
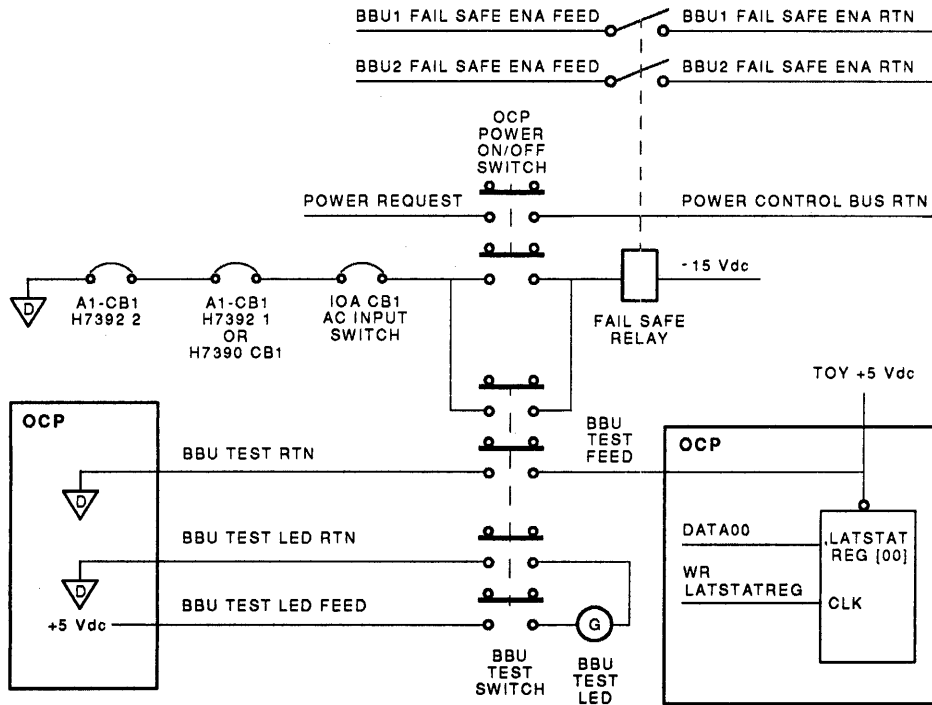
NOTE: BBU TEST LED RTN IS CONNECTED TO BBU TEST FEED IN THE OCP.

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Figure 6–17   BBU Failsafe Circuit

- **Battery backup request** — This is the request from the SIP to the H7231 BBU units requesting that battery power be supplied. If battery backup has been enabled, and is not providing battery power, the SIP asserts the request to the BBU units when ac power is lost. The request is not asserted if the output from the converters providing +5 Vdc BBU power is less than 95% of nominal voltage at the time ac power is lost.

- **Module enable** — When the batteries are supplying the power, the BBU units assert module enable. This prevents another request from being sent to the H7231s while battery power is being supplied.

   Module enable is not used to enable any of the H7380s, they are enabled by the RICs. RIC 42 (model 210) and RIC 41 (model 400 systems) keep the converters enabled, thereby keeping the +5 Vdc BBU power bus energized for 10 minutes (the time is determined by BBU circuitry within the H7231).

- **Battery status** — The battery status lines are variable condition lines that indicate the status of the battery backup units. Within the SIP, the status lines set a bit in the BBUREG for each BBU and control the BBU LED. The states of the lines, and therefore the BBU LEDs, are as follows:

   Off — The LED is off, and the battery is not available to provide power.
   Ready — The battery backup system is ready to provide power. The LED may be on continuously if the batteries are fully charged, or cycling at a 1 Hz rate if the batteries are charging.
   On — The batteries are supplying power and are discharging. In this case, the LED is cycling on and off at a 10 Hz rate.

- **TOY1 +5 Vdc** — Power to the SPU time-of-year clock.

- **TOY2 +5 Vdc** — Power to the OCP to keep OCP circuits (diagnostic display) energized during power outage.

- **BBU PHASE A OVERIDE FEED OUT H (BBU PHASE B OVERRIDE RTN OUT L)** — When the SIP asserts BBU REQ H to request battery power, the H7231 asserts MOD ENB H. At the SIP, MOD ENB H disables the battery backup request (deasserts BBU REQ H), which tries to disable battery power. BBU PHASE A OVERRIDE FEED OUT H and BBU PHASE B OVERRIDE RTN OUT L keep the H7231 supplying battery power until ac power returns to normal, or the 10 minute time limit expires.

   BBU PHASE A OVERRIDE FEED OUT H is asserted high and BBU PHASE A RTN OUT L is asserted low when the BBU request is asserted to request battery power. This condition of these two signals cause the H7231 to provide battery power regardless of the request being dropped, or the level of the input ac utility power.

   When ac power returns, the 280 Vdc gradually returns to normal. When dc voltage has reached about 160 Vdc, sufficient to support BBU converter group operation, ACLO is deasserted. The deassertion of ACLO causes BBU PHASE A OVERRIDE FEED OUT H and BBU PHASE A RTN OUT L to switch states, shutting down the BBU. The remaining converter groups are disabled, and stay disabled until reenabled by the RICs on command from the PEM (after a restart).

6.2.5.1 BBU Test Switch

The BBU test switch, located inside the front door of the IOA cabinet, is in parallel with the OCP Power keyswitch, and is used to test the battery backup units and associated circuitry. Assuming that the Startup keyswitch is in the Restart Boot position, and the system is booted up and running the VMS operating system, the following sequence of steps ensures that the BBU system is working properly (Figure 6–17).

1. Activate, and hold the BBU test switch. This keeps the failsafe relay energized. The BBU test LED (mounted with the BBU test switch) lights. Latched status register bit 0 (OCP) is unconditionally set. This is read and placed in the error log when power is returned to normal.

    NOTE
    Do not activate the BBU test switch for more than 10 minutes because the battery backup unit will time out in 10 minutes and cease to provide battery backup power.

2. Turn the system Power keyswitch to the Off position

    *   Opening of the Power keyswitch drops the power request on the power control bus, powering down the system.

    *   If the BBUs are functioning properly they will provide power, and the BBU status LEDs will start blinking at a 10 Hz rate.

3. Turn the system Power keyswitch back to the On position

4. Release the BBU test switch. The system performs a warm restart if the BBUs are functioning properly.

6.2.6 SIP LEDs

The SIP has four LEDs, visible from the front of the IOA cabinet with the door open. The two red LEDs indicate the status of BBU1 and BBU2. A green LED indicates the H7214 status, and a green LED indicates the H7215 status (Figure 6–8).

See Section 6.2.5 and the battery status control signal for an explanation of the status of the BBU LEDs.

The green LEDs light upon the receipt of H7214 OK or H7215 OK from the respective SPU converter modules.

6.2.7 SIP Total Off Circuitry

The total off circuitry trips A1-CB1 in H7392 1 or 2 or H7390 CB1 if one of the following occurs:

- Converter overtemperature

- Automatic shutdown conditions are detected by a RIC

- AC input phase unbalance (H7392 only)

- H7392 or H7390 thermal fault

- Loss of communications between the PEM and a RIC

The total off switch in parallel with the total off circuitry, and present on systems using an H7392, can be used to trip A1-CB1.

The total off circuitry can shut down a single zone (model 440) or the entire system, depending upon where the fault is detected. For a model 440, if the fault effects only part of the system, only the affected zone is shut down.

If a circuit breaker is tripped by the total off circuit, it must be manually reset.

If the PEM detects the fault condition, it routes the shutdown command to the SIP total off circuit, which trips the appropriate circuit breaker or breakers, depending on the fault. It writes the total off code into the DD LEDs (and associated registers) for use in error logging.

If a RIC detects the fault condition, the RIC asserts a command to the total off circuit to shut down part or all of the system. The assertion of the shutdown command is routed to the PEM, which commands all RICs to get off the RICBUS for 750 μs. At the end of the the 750 μs, the RIC that detected the fault sends its RIC ID and a fault code to the PEM. This message, which does not conform to the XXNET protocol, is the RIC ID and fault code only, and is sent three times. In case of a spurious line fault, the PEM uses two out of three voting to determine the fault code. The PEM then writes the fault code into the DD registers.

In Figure 6–18, DRIVE TOTAL OFF 1 L energizes TOTAL OFF1 relay (on the SIP) to route 7.5 Vdc to trip A1-CB1 (H7392) or CB1 (H7390), and shut down CPA and associated hardware. In systems containing only one H7392 (H7392 1), or an H7390, the entire system is shut down. DRIVE TOTAL OFF 2 L energizes TOTAL OFF2 relay, which routes 7.5 Vdc to trip A1-CB1 in H7392 1 and shuts down CPB and associated hardware.

In systems containing two H7392s, the diode OR maintains power to the SPU, SCU, memory, and clock in case of loss of power on one side or the other.

NOTE
The SIP routes a pair of total off signals to the BI expander cabinet connected to the XMI card cage that is shut down. This ensures that the BI adapters are also shut down.
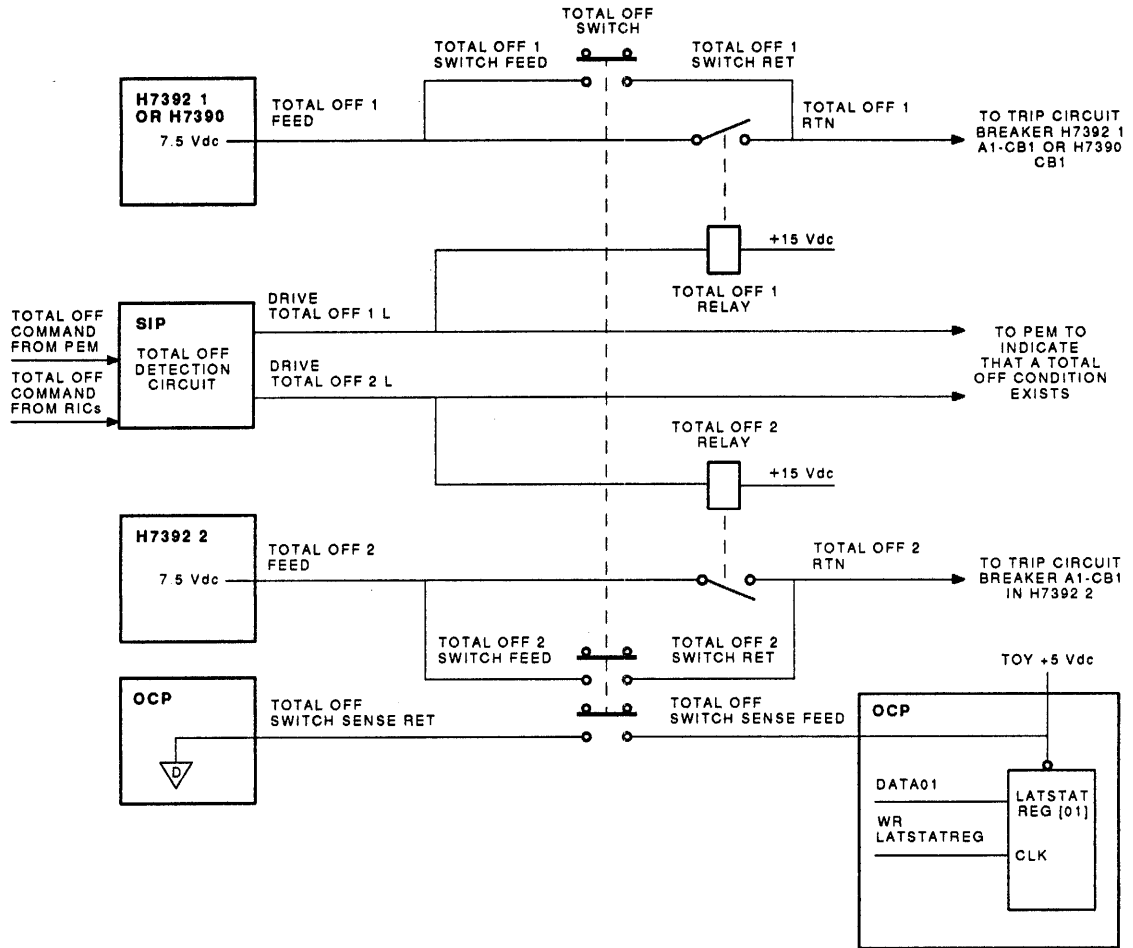
NOTE: ALL CIRCUITRY IS ON THE SIP EXCEPT THE TOTAL OFF SWITCH AND THE BOXES LABELED OTHERWISE.
A SYSTEM THAT HAS AN H7390 DOES NOT HAVE A TOTAL OFF SWITCH.

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Figure 6–18   SIP Total Off Circuit

In Table 6–12 the items listed assert DRIVE TOTAL OFF 1 or DRIVE TOTAL OFF 2, which trip the associated H7392 or H7390 circuit breaker.

Table 6–12   Drive Total Off

DRIVE TOTAL OFF 1	DRIVE TOTAL OFF 2
PEM loses communication with a RIC[1]	PEM loses communication with a RIC[1]
A RIC on RICBUS A asserts COM TOTAL OFF[2]	–
A RIC on RICBUS B asserts COM TOTAL OFF[2]	A RIC on RICBUS B asserts COM TOTAL OFF[2]
–	A RIC on RICBUS C asserts COM TOTAL OFF[2]
An overtemperature in the SPU H7215	An overtemperature in the SPU H7215

[1]The PEM determines which portion of the system needs to be shut down. The SPU H7214 must have H7214 OK asserted to enable the PEM to shut down any part of the system.

[2]A RIC asserts COM TOTAL OFF for an H7380 overtemperature, H7215 overtemperature, thermal fault (H7390 or H7392), voltage unbalance (H7390 or H7392), or if an automatic shutdown condition has exceeded its time limit.

6.2.8   Total Off Switch

NOTE
This switch is only present in systems using an H7392.

The system may be shut down from the rear of the IOA cabinet using the total off switch, provided that H7392 1 is providing 7.5 Vdc (Figure 6–18). This 3-pole switch is in parallel with the total off relay contacts. Two of the poles are used to power down the system by routing 7.5 Vdc to the H7392s to trip the main circuit breakers. These switch contacts bypass the total off relays. The third pole routes an OCP digital ground back to the OCP to set bit 1 in the latched status register. This bit informs the PEM that the system is being shut down because of total off switch activation. This information is available for the error log.

NOTE
In systems using an H7390, SIP J08-01 must be jumpered to J08-02 to complete the BBU failsafe circuit.

6.2.9 Power Control Bus

When the OCP power keyswitch is closed (Figures 6–18 and 6–19), it provides the required low for power request to turn on system power (providing that power inhibit is high). If either of the filters are removed far enough to activate the microswitches, the normally open contacts close, placing a low on the power inhibit line. Power inhibit asserted low causes a power shutdown, regardless of the state of the power request signal, and prevents the BBUs from providing battery power.

POWER INHIBIT1 is routed to both H7231 battery backup units to prevent supplying battery power when it is asserted low.

One filter is under the XMI and SPU card cages in the IOA cabinet. The other filter is under the memory and MCM card cages in the SCU cabinet.

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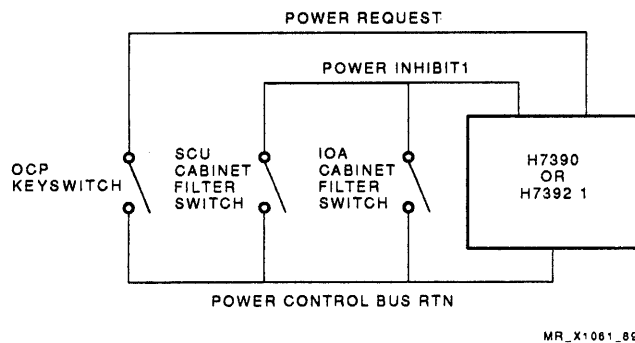
Figure 6–19   Model 210 Power Control Bus

6.2.10 AC Breaker Position

The SIP routes a digital ground to each of the H7392s (or H7390), where it is routed through normally open contacts of CB1. If the circuit breaker is closed, the ground potential is routed back to the SIP, and on to the PEM, where it is used to set a bit in the total off register. TOFF REG [06] is AC BRK1 OK L (H7390 or H7392 1) and TOFF REG [07] is AC BRK2 OK L. These bits are asserted low (reset) if the circuit breaker is closed. The pullup circuit sets bit 7 if the second H7392 is not installed.

6.3 H7214 Converter

The H7214 is a dc/dc switching converter that works with an H7215 to provide power for an XMI backpanel or the service processor BI backpanel. It requires 280 Vdc, and provides a regulated +5 Vdc (120 A) and an unregulated +13.5 Vdc (0.5 A).

The H7214 outputs are fixed voltages and cannot be adjusted or margined, nor can multiple H7214 converters be connected for current sharing. The +5.1 Vdc output is protected by a latching crowbar circuit, which is reset by removing dc power.

An XMI H7214/H7215 converter pair is controlled and monitored by an H7389 I/O RIC. The SPU H7214/H7215 converter pair is controlled and monitored by the PEM/SIP.

6.3.1 H7214 Output Voltage, Current, and Tolerances

Table 6–13 lists the voltage and current limits for the H7214 converter at +5.1 and +13.5 Vdc output.

Table 6–13   H7214 Output Voltage, Current, and Tolerances

	5.1 Vdc Output	13.5 Vdc Output
Nominal voltage	5.065 Vdc	13.5 Vdc
Voltage tolerance range	±0.192	+2.25/-2.10
Overvoltage trip	5.7–7 Vdc	NA
Rated current	120 A	0.5 A
Current limit	125–140 A	30 A
Ripple voltage	130 mV	NA

6.3.2 H7214 Inputs

The following signals are the H7214 converter inputs:

* **CH 1 INHIBIT** — When asserted high, this signal inhibits all converter outputs and resets the module to a ready state. Output power is restored when CH 1 INHIBIT goes low.

* **CLOCK** — The clock used to synchronize the module is a 32.5 kHz clock generated on the SIP. For the XMI H7214s, if SIP clock is lost, the associated I/O RIC provides a 30.5 kHz clock. The SPU H7214 has no backup clock. If SIP and RIC (for XMI H7214s) clock is lost, the free running frequency of the H7214 is used (approximately 29 kHz).

* **BIAS** — The H7214s require +15 Vdc startup voltage, which is supplied by a bias supply. The bias powers the control circuits until the H7214 can supply its own bias power.

6.3.3 H7214 Output Signal

The following signal is the H7214 converter output:

* **CH # OK** — When asserted high, indicates that the H7214 dc/dc regulator module is within regulation.

6.3.4 H7214 LEDs

A green LED is visible from the rear of the H7214. When lit, it indicates proper operation of the converter. The SPU H7214 also has a green LED on the SIP, which indicates that CH # OK is asserted.

6.3.5 H7214 Fuses

The H7214 converters are protected by internal fuses.

6.4 H7215 Converter

The H7215 is a dc/dc switching converter that works with an H7214 to provide power for an XMI backpanel or the service processor BI backpanel. It requires 280 Vdc, and provides -5.2, -2.0, and ±12.0 Vdc.

The H7215 outputs are fixed voltages and cannot be adjusted or margined, nor can multiple H7215 converters be connected for current sharing.

All of the H7215 outputs are protected by a latching, overcurrent detection circuit. When the module has been shut down due to overcurrent, the overcurrent detection circuit must be reset by the high assertion of CH INH, or a normal startup sequence.

An XMI H7214/H7215 converter pair is controlled and monitored by an H7389 I/O RIC. The SPU H7214/H7215 converter pair is controlled and monitored by the PEM/SIP.

6.4.1 H7215 Output Voltage, Current, and Tolerances

Table 6-14 lists the voltage and current limits for the H7215 converter at -5.2, -2.0 and ±12 Vdc output.

Table 6-14 H7215 Output Voltage, Current, and Tolerances

	-5.2 Vdc Output	-2.0 Vdc Output	±12 Vdc Output
Nominal voltage	-5.26	-2.15	±12.07
Voltage tolerance	±0.2 Vdc	±0.1 Vdc	±0.54 Vdc
Overvoltage trip range	5.9-7.2 Vdc	2.4-2.7 Vdc	13-14 Vdc
Rated current	30 A	12 A	5 A
Current limit	37-40 A	13-16 A	7-13 A
Ripple voltage	100 mV	50 mV	300 mV

6.4.2 H7215 Inputs

The following signals are H7215 converter inputs:

- **CH INHIBIT** — When CH INHIBIT is high, the converter outputs are disabled and the module is reset. When the signal goes low, the outputs are enabled.

- **SYNC** — SYNC is a clocking signal used to synchronize the module. It is provided by the SIP at 32.5 kHz to both the XMI and SPU H7215 converters. If the SIP clock is lost, an XMI H7215 receives a backup 30.5 kHz clock from the I/O RIC. There is no backup clock for the SPU H7215. If both clock sources are lost (XMI H7215) or SIP clock is lost (SPU H7215), the free running frequency of the H7215 is 27 kHz.

- **BIAS** — The H7215 converters require +15 Vdc startup voltage. This startup voltage, or bias, is supplied by a bias supply. The bias powers the control circuits until the H7215 can supply its own bias power.

6.4.3 H7215 Output Signals

The following signals are H7215 converter outputs:

*   **CH OK** — The channel OK signal, when in a high state, indicates that the regulation is within specification.

*   **OV TEMP L** — When asserted low, this signal indicates that the H7215 converter has experienced an overtemperature condition. The signal is routed to the H7389 I/O RIC fault detection circuitry for an XMI H7215, or to the SIP for the SPU H7215. If OV TEMP L is asserted, the system is shut down by the total off circuits.

6.4.4 H7215 LEDs

The H7215 has a green LED, which lights if all the outputs are within regulation. The SIP also has a green LED, which is lit if the SPU H7215 asserts CH OK.

6.4.5 H7215 Fuses

The H7215 converters are protected by internal fuses.

6.5   H7231 Battery Backup

The H7231 battery backup (BBU) is comprised of the H7230 battery and battery charger assembly and the H7240 converter assembly. The system provides an uninterruptible power source for any 250 Vdc bus powered regulator. Supplied from an ac utility power source, it is self sustaining and capable of charging and maintaining its self contained dc storage batteries (four 12 Vdc battery units). The system requires 24 hours to recharge from fully discharged batteries. During utility power interruptions, the system supplies hold-up power to the power converters.

The H7231 provides two primary power outputs:

*   250 Vdc 200 W for up to 10 minutes memory refresh during power interruptions

*   +5 Vdc 1 W (TOY output) continuous power, and for up to 100 hours during power interruptions

A detailed description of the H7231 is found in the *H7231A Battery Backup Unit User's Guide* (EK-H7231-UG).

6.5.1 Battery Backup General Description

The H7231 BBU consists of two major units:

- H7230 battery/battery charger
- H7240 power converter

6.5.1.1 Battery/Battery Charger Unit
The batteries consist of four 12 Vdc battery packs connected in series to provide a 48 Vdc source. Each battery pack is made up of six 2 Vdc lead-acid batteries. The battery packs and the TOY regulator board are easily replaced for corrective maintenance.

The battery charger unit consists of the battery charger and the TOY regulator. The batteries are charged at a 400 mA rate until they have reached 80% of full charge, at which time the charge rate is decreased to a trickle charge of 10 mA.

The TOY regulator is a switching regulator that converts the 48 Vdc from the batteries to a regulated +5 Vdc, 200 mA output. It also produces +12 Vdc bias control voltage and precision reference voltages of +4.0, +5.0, and +6.5 Vdc for TOY regulator control.

6.5.1.2 H7240 Power Converter
The H7240 power converter is a switching regulator that converts the 48 Vdc battery output to a 250 Vdc output for the high voltage dc buses. It monitors system ac power and control signals to enable or disable providing the 250 Vdc. If battery backup is enabled, the H7240 terminates battery backup after 10 minutes, or if system ac power is regained, or if the battery becomes discharged.

6.5.2 Modes of Operation

There are two modes of operation, charge mode (Section 6.5.1.1) and backup mode. In backup mode the BBU is supplying power to the 280 Vdc bus, but only if all of the following conditions have been met:

- The converter has received battery backup enable (BBUE).
- The converter has responded with battery backup available (BBUA). This signal indicates that the converter has received BBUE, ac power, and the power relay is energized (the H7231 is enabled to provide power).
- Battery voltage is sufficient.
- The converter receives battery backup request (BBUR) when system ac power is lost.

6.5.3 BBU Status

BBU status is indicated by a LED for each H7231. These LEDs are located on the SIP, and have three states:

- **Off** — Battery backup is not available.

- **On** — The batteries are fully charged and battery backup is available.

- **Blinking**

  - **Slow, at a 1 Hz rate** — The batteries are not fully charged, and are being charged.

  - **Fast, at a 10 Hz rate** — Battery backup is on and is providing 250 Vdc power. The batteries are being discharged.

6.5.4 BBU Usage

There are two H7231 battery backup units in VAX 9000 systems. Their 250 Vdc outputs are tied together and provide:

- Bias supply PSA. The B1 output provides power to the SIP while the B2 output provides RICBUS power.

- Bias supply PSD. The B1 output powers RIC 42, which monitors power bus B, and provides bias to H7380 converters B1 and B2. The B2 output provides power for the OVP module.

- Power is provided to H7380 B1 and B2, which provide BBU +5 V for memory refresh.

Additionally, TOY power is supplied for each system as follows:

- TOY1 +5 Vdc is provided to the SPU time-of-year circuitry.

- TOY2 +5 Vdc is provided to power the OCP (retain the contents of the DD LEDs).

TOY1 and TOY2 +5 V are available for up to 100 hours.

6.6 H7380 Converter

The H7380 is a dc/dc converter that steps down 280 Vdc to an output voltage ranging from +3.2 to +5.5 Vdc with a current between 20 A and 240 A. It requires bias voltage from a bias supply, an enabling signal, clock, and control signals from a RIC. Besides the output voltage, the converter supplies the RIC with a module OK signal, overtemperature indication, sense voltage, and a signal that indicates that the converter is installed. For a description of the interaction between the various components in a converter group, see Section 3.1, H7380 Converter Group.

H7380 converters are current sharing converters; up to five converters may be paralleled on a bus. This capability is required for model 400 systems n + 1 operation, where the number of converters is one greater than required for circuit operation.

6.6.1 H7380 Input Voltage and Current (280 Vdc)

The H7380 normally operates at 280 Vdc, but operates down to 190 Vdc with full output current. To accommodate battery backup support, the H7380 operates down to 165 Vdc, but at reduced current.

The input current is not to exceed 10 A, and the converter is protected from excess input current by two internal 15 A fuses, one on the high side, and one on the return side.

6.6.2 H7380 Output Voltage, Current, and Tolerances

The output voltage range is +3.2 to +5.5 Vdc for the normal input voltage range, and is determined by CONTRL from the controlling RIC. Table 6–15 lists the voltage and current limits for the H7380 converter at different ranges of input voltage.

Table 6–15   H7380 Voltage and Current Limits

Input Voltage (Volts)	Output Voltage (Volts)	Output Current (Amperes)
190–325	3.2–5.5	0–240
180–189	3.2–5.3	0–240
165–179	3.2–5.5	0–50

The normal H7380 output voltages are +5, -3.4, and -5.2 Vdc, as determined by the associated RIC (and CONTRL). The tolerance on each voltage is ±25 mV. The ripple voltage tolerance is ±2%, or ±100 mV for 5 Vdc, ±104 mV for -5.2 Vdc, and ±68 mV for -3.4 Vdc.

The H7380 converter may be margined ±5%. See Section 6.10.2.5, and Table 6–25 for information on voltage margining.

6.6.3 H7380 Overcurrent

Two types of overcurrent protection prevent excessive output current from damaging the H7380 converter.

- **Constant Current Limit** — When the output current exceeds the range of 275 to 290 (set within each converter), any attempt to draw more current results in a decrease in the output voltage.

- **Pulsed Overcurrent Limit** — The current limit for each converter present is 255, except for model 400 systems using n + 1 redundancy. In this case the current limit is 255 multiplied by the number of converters present -1 ($255[no.of converters - 1]$). The RIC monitors the total current, and if an overcurrent condition exists, it shuts down the entire converter group for 1.6 seconds by deasserting ENABLE L to each of the converters. ENABLE L is asserted again at the end of the 1.6 second period. If the overcurrent condition still exists, the RIC again turns off the converter group. This continues indefinitely or until power is removed from the system. If the cause of the overcurrent condition is removed, the converters resume normal operation (Section 6.10.2.8).

6.6.4 H7380 Voltage Distribution

Tables 6–16 and 6–17 provide information on bus voltages, and the number of H7380 converters required for the SCU and each of the CPU cabinet buses for the model 210 and 400 systems (n + 1 operation).

Table 6–16   Model 400 Systems H7380 Usage

Bus	Purpose	Number of Converters		
		Uni	Dual	Quad
A	BBU +5 Vdc	3	3	3
B	SCU -5.2 Vdc	2	2	2
C	SCU -3.4 Vdc	2	2	2
D	MEM +5 Vdc	2	2	2
J	CPU 0/1 -5.2 Vdc	3	5	5
K	CPU 0/1 -3.4 Vdc	3	5	5
M	CPU 2/3 -5.2 Vdc	–	–	5
N	CPU 2/3 -3.4 Vdc	–	–	5

Table 6–17   Model 210 Systems H7380 Usage

Bus	Purpose	Number of Converters
A	MEM +5 Vdc	1
B	BBU +5 Vdc	2
C	CPU0, SCU -3.4 Vdc	3
D	CPU0, SCU -5.2 Vdc	3

6.6.5 H7380 Input and Output Signals

The H7380 input/output signals are routed to the converter through a 34-pin connector, J1. The signals are divided into four classes: power, input, output, and pass-through. The pass-through signals are cases where the H7380 receives a signal or voltage from the RIC, and returns the signal or voltage, possibly modified, to the RIC.

NOTE
As there may be more than one H7380 converter on a power bus, the signal names at the H7380 (per the H7380 schematics) often differ from the signal names on the power backpanels. The primary signal names in this section are the H7380 signal names. Alternate signal names at the power backpanel are provided in brackets, [ ].

6.6.5.1 H7380 Power
The following signals are H7380 converter inputs.

- **+15 STARTUP [+15V]** — The H7380 receives startup voltage from a bias supply. It provides power to the pulse width modulator (PWM) and the converter control circuits. When the converter is supplying power, an internal supply (ORed with +15 STARTUP) supplies the voltage.

- **GNDA** — GNDA is an analog ground, the return for the +15 Vdc and all input and output signals.

6.6.5.2 H7380 Input Control Signals
The H7380 converter requires inputs from the RICs to function.

- **ENABLE L [ENABLE nn L]** — When asserted low by the RIC, ENABLE turns on the converter. If high, or disconnected, the converter is turned off. For further information, see Section 6.10.2.10.

- **CONTRL (CONTRL RTN)** — This signal, from the RICs error amplifier, controls the converter output current. It is a result of a comparison between the converter output voltage and a reference voltage. The operating range of this signal is between +2.5 and +9.0 Vdc. The output current follows CONTRL, increasing as CONTRL increases, and decreasing as CONTRL decreases.

- **REG CLK** — This input sets the operating frequency of the converter. REG CLK is generated on the SIP, and routed through the RIC. If the SIP oscillator malfunctions, an oscillator on the RIC provides the clock. The clock range is from 156 to 164 kHz, with the normal clock (from the SIP) being 162.5 kHz. The secondary clock source from the RIC is a 158 kHz clock.

6.6.5.3 H7380 Output Signals

The H7380 converter provides signals that allow the RIC to monitor its operation.

* **MOD OK L [MOD OK nn L]** — MOD OK L, if asserted low, indicates that the converter is operating properly. If either of the power transformers cease to operate or the module goes into an overcurrent state (245 to 260 A), MOD OK L is deasserted. MOD OK L controls the MOD OK LED on the converter, and is routed to the RIC. An overtemperature does not cause the deassertion of MOD OK L.

* **ISENSE [ISENSE nn]** — ISENSE is a dc signal with a voltage proportional to the converter output current (ISENSE = 1 V per 85 A or V = 0.0117 times output current). The RIC uses ISENSE to measure converter output current.

* **LOCAL SENSE NEG (POS)** — The LOCAL SENSE outputs provide a backup means of sensing the bus voltage. The LOCAL SENSE output is the converters output voltage routed through a 10-ohm resistor. LOCAL SENSE from each H7380 on the bus is wired ORed on the power backpanel to VOLT SENSE from the bus bar (Figure 6–20).

  The RICs monitor VOLT SENSE to determine bus voltage. VOLT SENSE is the input to the RICs error amplifier, and is compared to the reference voltage to produce CONTRL, which is the error voltage sent to the H7380 to control converter output voltage.

  If only VOLT SENSE was used, and if the VOLT SENSE wire was disconnected or broken between the bus bar and the backpanel, the RICs would sense no converter voltage and call for maximum voltage, obviously in error. LOCAL SENSE is used as a backup to VOLT SENSE in case of this problem.

* **DYNAMIC SENSE NEG (POS)** — This output is the same as LOCAL SENSE NEG (POS). This signal is not used.
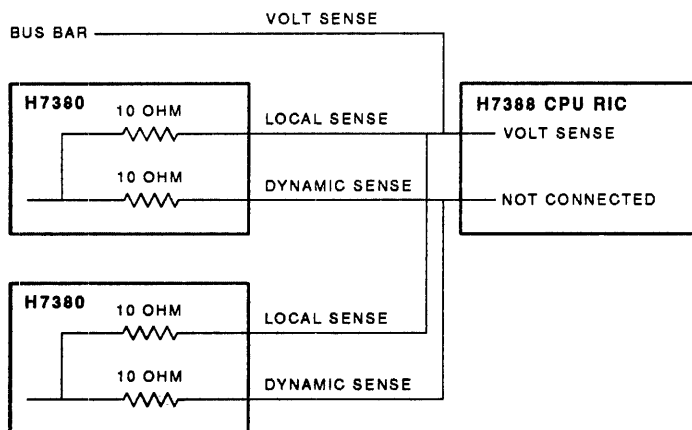
Figure 6–20   Sensing H7380 Converter Voltage

6.6.5.4 H7380 Pass-Through Signals

Three signals form loops between the RIC and the converter. The RIC provides the input and the converter provides a return to the RIC.

- **INDUCTOR OT H (INDUCTOR OT RTN)** — INDUCTOR OT H is connected to +5 Vdc through a pullup resistor in the RIC. It is routed to a thermal fuse located on the output inductor, which opens the normally closed path, at 150°C ±5°C.

  From the thermal fuse, the path leaves the converter as INDUCTOR OT RTN, and proceeds sequentially to each of the converters in a converter group. INDUCTOR OT RTN is connected to GNDA at the output of the last converter. As long as there is not an inductor overtemperature, the +5 Vdc travels to ground, keeping INDUCTOR OT H deasserted. If any of the converters in the group experience an inductor overtemperature condition (or is removed), the path is opened, and INDUCTOR OT H is asserted, which shuts down all the converters in the group (at the RIC). This signal cannot be reset except by replacing the output inductor unit.

  If an H7380 converter is not needed in the configuration, and therefore not installed, the series INDUCTOR OT circuit is broken, and the converter group is disabled. Installing jumper 17-02422-01 in place of the H7380 completes the circuit, allowing normal operation.

- **OT H (OT RTN)** — In the RIC, each of the OT n H signals is connected to +5 V through a pullup resistor. OT n H is routed to an individual converter in the group. A bimetallic thermal sensor mounted on the output rectifier heat sink opens at a temperature of 125°C ±5°C. If the temperature is within the operating range, the circuit is closed, and the voltage is routed out of the converter as OT RTN. OT RTN from each of the converters is wire ORed and routed back to ground in the RIC.

  As long as the temperature remains in the operating range, each of the OT n H signals remains at a ground potential. If the temperature in any of the converters becomes too high, or the converter is removed, OT n H is asserted to activate the RICs overtemperature detection circuit, which causes the RIC to assert COM TOTAL OFF L to the PEM to shut down the system. For more information, see Section 6.10.2.11.

  Jumper 17-02422-01 also jumpers OT H to OT H RTN to maintain this circuit in case of an H7380 that is not needed in the configuration.

- **IPROG (IPROG RTN)** — The RIC provides a +5 Vdc reference to each of the slots for converters in the converter group. If a converter is installed, it returns the voltage as IPROG RTN. At the RIC, the individual IPROG RTNs become IPROG n, which the RIC uses to determine how many converters are installed, and to set the overcurrent trip level.

6.6.6 H7380 LEDs

Each H7380 has two LEDs (Figure 6–21).

- **MOD OK** — This green LED is lit as long as MODULE OK is asserted indicating the output transformers are working properly and the converter is not in an overcurrent condition.

- **OVERCURRENT** — If this yellow LED is lit continuously, the converter is in an overcurrent condition. If it is pulsing (all converters in the group should be pulsing), the converter group is in the pulsed overcurrent mode. In this mode, the RIC shuts the converter down for 1.6 seconds, then reenables the converter. If the overcurrent condition reoccurs, the RIC again shuts down the converter for 1.6 seconds. This continues indefinitely, until the overcurrent condition clears up, or the system is shut down.

```
+-------------+
|             |
|    (G)       |   MOD OK
|             |
|    (Y)       |   OVERCURRENT
|             |
+-------------+
```

MR_X1062_89
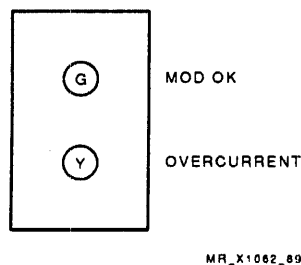
Figure 6–21   H7380 LEDs

6.6.7 H7380 Block Diagram and Description

The following is an explanation of the H7380 basic block diagram shown in Figure 6–22.

The input 15 A fuses receive ±140 Vdc, which provides a differential voltage of 280 Vdc. The fuses protect the H7380 from overcurrent input voltages. The H7380 will not operate if it receives only one side of the input voltage, as when -140 Vdc is present through the diode OR when one side of a quad processor system is shut down.

The input filter works both ways, reducing the noise radiated out of the H7380 to the high voltage dc lines, and reducing the noise that the high voltage dc lines transmit to the H7380. It eliminates the high frequency ac components from the dc voltages.

+15 Vdc BIAS

CONTROL CIRCUIT VOLTAGE (USED INTERNAL TO H7380)

AUXILIARY POWER SUPPLY

+18 Vdc

LOCAL SENSE POS
LOCAL SENSE NEG
DYNAMIC SENSE POS
DYNAMIC SENSE NEG

+140 Vdc
-140 Vdc

FUSE AND INPUT FILTER

INVERTER A

RECTIFIER A

OUTPUT VOLTAGE POS

LOW PASS FILTER

OUTPUT VOLTAGE NEG

PRIMARY CURRENT

MOD OK DETECTION CIRCUIT

MOD OK LED
MOD OK L

INVERTER B

RECTIFIER B

PRIMARY CURRENT

REG CLK
ENABLE
CONTRL

PULSE WIDTH MODULATOR

DRIVE A
DRIVE B

PEAK DETECTOR

OVERCURRENT LED
ISENSE

MR_X1805_89

Figure 6–22   H7380 Block Diagram

The inverters convert the high voltage low current input to low voltage high current pulsed dc. They are switching inverters and are controlled by the drive currents generated by the PWM. There are two inverters, inverter A and inverter B. The current flowing through the inverter primary winding is used as feedback to the PWM. Also, the primary current is monitored by the peak detector, which monitors for excess primary current flow. An overcurrent condition is indicated by the overcurrent LED on the front of the H7380 module. The peak detector also provides a voltage proportional to the primary current to allow the monitoring RIC to measure current.

The PWM is enabled by the RIC with the enable input. The drive frequency is established by the regulator clock input, normally at 162.5 kHz. CONTRL is the error voltage from the RIC. This input controls the pulse width of drive A and drive B. An increase in pulse width increases the output voltage; decrease the pulse width and decrease the output voltage.

The MOD OK detection circuit monitors the secondary voltage in the inverters and checks for proper amplitude. It also uses one of the peak detector outputs that indicates there is too much current flowing in the primary. If the current and voltage are within limits, the MOD OK LED on the front of the H7380 is lit, and the MOD OK L signal is sent to the monitoring RIC.

NOTE
The MOD OK LED may not be lit if there is no output load.

The pulsed dc inverter outputs are rectified, then added together in the low pass output filter.

The auxiliary power supply uses the pulsed dc to generate +18 Vdc. It is ORed with the +15 Vdc bias from the bias supply. At startup, the +15 Vdc bias is used in the control circuits. Once the +18 Vdc is generated by the auxiliary power supply, this voltage powers the control circuits.

6.7 H7382 Bias Supply

The bias supplies are dc/dc converter modules that receive power from the 280 Vdc buses. They are the primary source of power for the power control subsystem control and monitoring circuits (RICs and SIP), the H7386 OVP module, and H4000 Ethernet transceivers. They also provide startup power to the H7214, H7215, and H7380 converters.

The H7382 is used in parallel (redundant) mode in model 400 systems, supplying two buses at a time. In model 210, the H7382 is used in a nonredundant mode, supplying power to up to four buses. The mode of connection, and therefore the number of available outputs, is determined by system cabling.

The H7382 block diagram (Figure 6-23) describes the inputs, outputs, and basic operation of a bias supply. Distribution of bias supply voltages is covered in Chapter 4, DC Power Distribution.

6.7.1 Basic Bias Supply Operation

This section describes the basic operation of the H7382 bias supply.

6.7.1.1 Bias Supply Input Voltage
The bias supplies are powered by 280 Vdc, with a normal operating range of 165 to 325 Vdc. When power is increasing from no power, the outputs are off until the input voltage has reached 165 Vdc. When power is decreasing, the outputs remain within regulation until the input reaches 155 Vdc. Below 155 Vdc, the outputs are off. This allows for BBU operation.

There are two independent supplies of 280 Vdc to the bias supply. This allows one side to be powered separately from the other side, a feature that is used in systems with an H7390, and for battery backup.
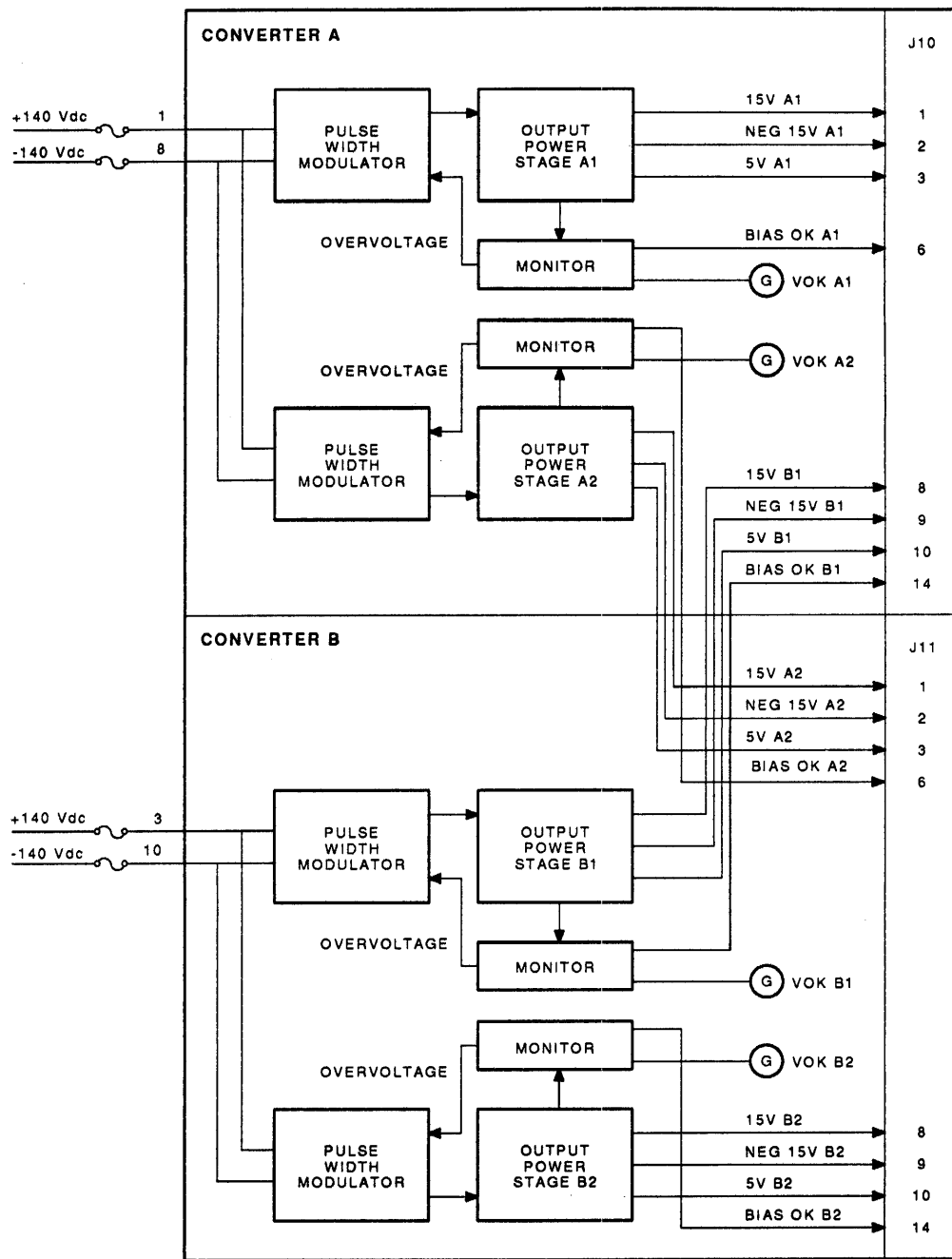
Figure 6–23   H7382 Bias Supply Block Diagram

6.7.1.2 Bias Supply Description

Each bias supply is composed of two independent, multiple output dc/dc converters, converter A and converter B, which are protected by independent fuses, two fuses for each converter. Each of the converters contains two primary side, pulse width modulators, which control a triple output power stage. One output power stage is referred to as the 1 side, while the other is referred to as the 2 side.

A monitor for each output stage monitors its three output voltages (Table 6–18), and shuts down the pulse width modulator for an overvoltage condition. The monitor also provides a status signal to the RIC (BIAS OK n) and lights a LED to indicate that the three voltages from a power stage (A1, A2, B1, B2) are within regulation (Figure 6–24).

The output voltages from output power stage A1 and B1 are combined by crossing the B1 voltages to the converter A side of the module. These voltages are cabled at J10. The output voltages from output power stage A2 and B2 are combined by crossing the A2 voltages to the converter B side of the module. These voltages are cabled at J11.

For model 400 systems, all voltage pairs from J10 and J11 (15 Vdc A1 and 15 Vdc B1) are tied together on the receiving backpanel to increase effective availability. This is not done for model 210.

MR_X1064_89
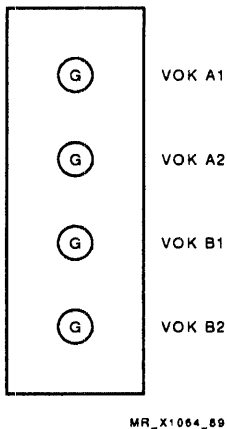
Figure 6–24   Bias Supply LEDs

6.7.2 Bias Supply Output Voltages

Each of the H7382 bias supply outputs, A1, A2, B1, and B2, provide ±15 and +5 Vdc. The A2 voltages are crossed to the B side and the B1 voltages are crossed to the A side.

The tolerance for each of the voltages generated is ±5%. If any output enters an overvoltage condition, the pulse width modulator is shut off. Input power must be removed, then reapplied to reset the bias supplies overvoltage protection circuit. Table 6–18 shows the overvoltage trip points and the current limits for the voltages developed by the bias supplies.

Table 6–18 Bias Supply Overvoltage Trip Points

Output Voltage (Vdc)	Overvoltage Trip Point (Vdc)	Current Limit (A)
5	6.5	2
15	19	2
-15	-20	0.2

6.7.3 Bias Supply Voltage Distribution

The H7382 connectors on the backpanel are not oriented physically as shown in Figure 6–23. Their orientation on the backpanel is shown in Figure 6–25.

Chapter 4, DC Power Distribution, describes the bias supply voltage distribution.

J11

15 BIAS OK L
14 BIAS OK H
13 GND
12 GND   } B2
11 GND
10 +5Vdc
09 -15Vdc
08 +15Vdc

07 BIAS OK L
06 BIAS OK H
05 GND
04 GND   } A2
03 +5Vdc
02 -15Vdc
01 +15Vdc

J10

15 BIAS OK L
14 BIAS OK H
13 GND
12 GND   } B1
11 GND
10 +5Vdc
09 -15Vdc
08 +15Vdc

07 BIAS OK L
06 BIAS OK H
05 GND
04 GND   } A1
03 +5Vdc
02 -15Vdc
01 +15Vdc

MR_X0115_90
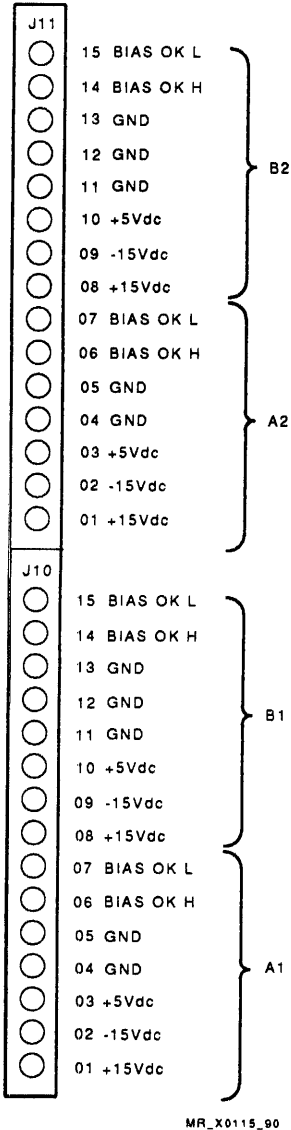
Figure 6–25   H7382 Output Connectors

6.8 H7386 Overvoltage Protection (OVP) Module

The H7386 OVP module monitors the +5, -3.4, and -5.2 Vdc buses for an overvoltage condition. If a monitored bus exhibits an overvoltage condition, the OVP module lights an OVP module LED to indicate which channel detected the condition and informs the RIC of the overvoltage condition by way of the status 10 input. This RIC input disables the converters on this bus. If the overvoltage is detected on a -3.4 Vdc bus, the OVP fires an SCR, which shorts the -3.4 Vdc bus to its return. Besides the -3.4 Vdc bus being disabled at the RIC, a sequencing signal from the -3.4 Vdc channel is applied to the -5.2 Vdc channel. This causes the -5.2 Vdc bus to be disabled also.

6.8.1 Purpose

If the -3.4 Vdc bus were to get too high (more negative), the transistor base to emitter junctions could become forward biased, causing heavy current flow, and possible damage to the emitter-coupled logic (ECL) circuitry. If any of the voltages become greater than 7 V, it could break down the ECL logic.

Each H7386 OVP module is capable of monitoring three different buses for overvoltage conditions. The module:

- Provides an output that can fire an SCR mounted between the bus and ground in the event of an overvoltage condition.

- Provides signals to the RIC indicating an overvoltage condition.

- Provides a sequencing capability whereby an overvoltage on one bus may be used to trigger the SCR for another bus.

- Provides an input to trigger any channel regardless of bus voltage.

- Provides an input to trigger all three channels regardless of bus voltage.

- Provides the RIC with the CROWBAR READY signal, indicating that the OVP module has powered up, been reset, and is capable of operation.

- Contains circuitry that allows disabling the SCR firing circuitry for channels B and C.

- Has power on reset circuitry that prevents the OVP from operating until it has received the proper operating voltages from the bias supply.

Not all of the OVP module capabilities are used. Those that are used are pointed out in the block diagram description. Table 6–19 shows the OVP module locations, which bias supply provides power to the OVP, the voltage bus being monitored by the OVP module, and which RIC is monitoring the OVP.

Table 6-19 H7386 OVP Module Usage

OVP Location	Power Supply	OVP Channel A -3.4 V Bus RIC	Bus	OVP Channel B -5.2 V Bus RIC	Bus	OVP Channel C +5.0 V Bus RIC	Bus
Model 210 OVP Module							
CPA	PSD B2[1]	24	C	14[2]	D	32,[3]42[3]	A, B[4]

[1]PSD B side is powered by 280 (250) Vdc BBU.

[2]RIC 14 monitors CROWBAR READY.

[3]RIC 32 monitors bus A and OVP channel C. RIC 42 monitors bus B.

[4]Bus A (+5 Vdc) and bus B (+5 Vdc BBU) are ORed on the model 210 OVP backpanel.

6.8.2 OVP Module Block Diagram

The H7386 OVP module is explained at the basic block diagram level. While referring to Figure 6-26, keep in mind that there is an on-board power supply and reset circuitry that is common to the entire module. Of the three channels, channels B and C are identical. The only difference in channels is that the gate drive circuit for channel A cannot be disabled individually, whereas it can be disabled individually in channel B or C. Because of the similarities, only channel B is explained.

6.8.2.1 Power Supply and Power-On Reset

The OVP module receives ±15 Vdc from an H7382 bias supply. The on-board power supply circuitry uses the +15 Vdc to generate internal +5 Vdc.

When power is first applied, all the channels are prevented from firing an SCR by the power-on reset circuitry. When the inputs to the OVP modules power-on reset circuit has reached at least ±11.4 Vdc, this circuitry resets the OVP logic (POR), and enables the OVP to monitor for an overvoltage condition. The OVP lights the green ready LED, on the front of the OVP module, and informs the RIC that it is operational by asserting CROWBAR READY L. The PEM will not direct the RICs to enable converters until the RIC has detected the assertion of CROWBAR READY L. If any channel detects an overvoltage condition, the ready LED goes out, and CROBAR READY L is deasserted, causing an exception.

NOTE
On the OVP module schematics, signals are spelled CROBAR. On the power system backpanel schematics, they are spelled CROWBAR. Even though this description refers to the signals on the OVP module, reflecting the OVP module schematics, the spelling used is CROWBAR because that is what will be seen most often.
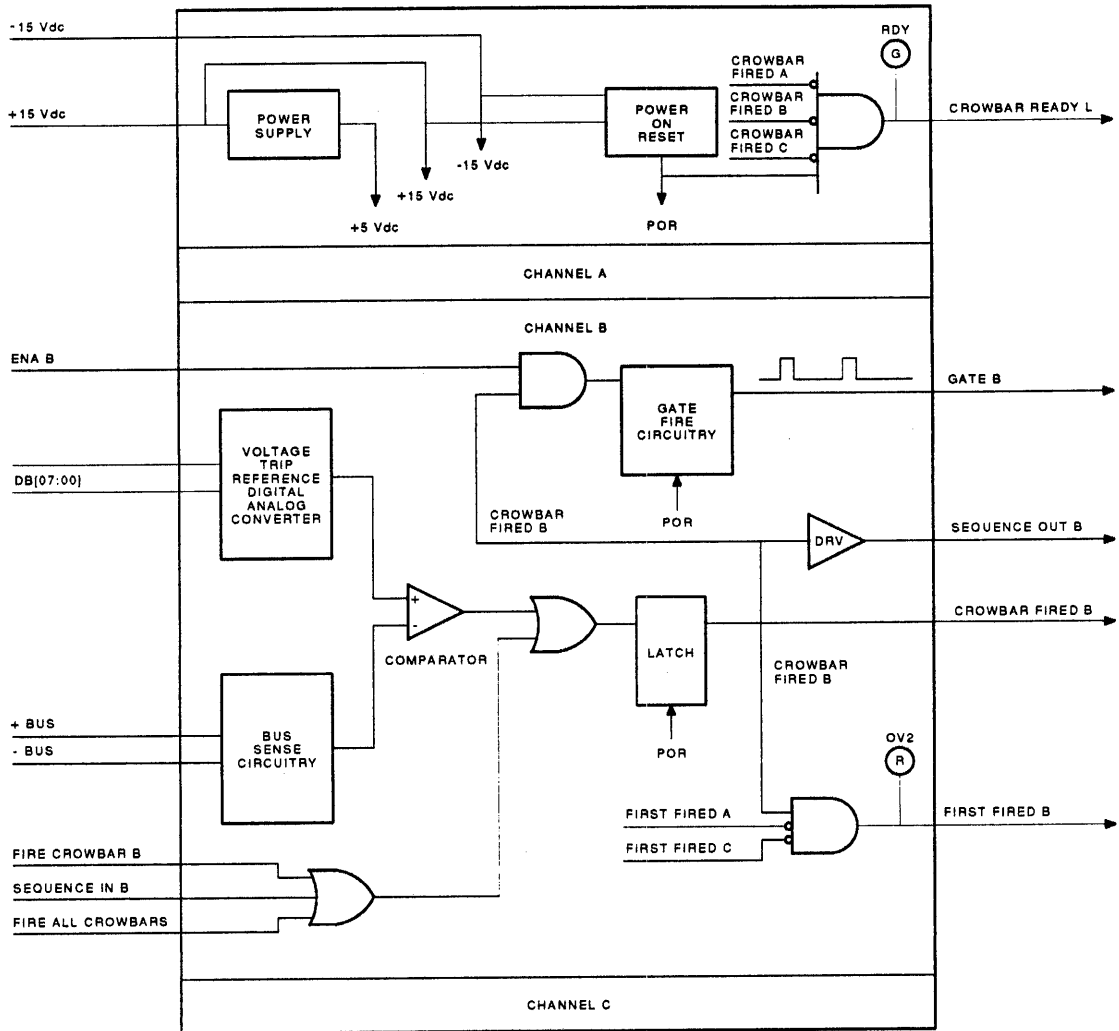
Figure 6–26   H7386 OVP Module Block Diagram

6.8.2.2 Voltage Trip Reference

The voltage trip reference is generated by a D/A converter programmed by DB[07:00]B, which is tied to common (logic 0), or left open (pulled up to +5 Vdc) for a logic 1. Backpanel connections provide the correct programming for each of the OVP modules' three channels. Table 6–20 shows the trip level (D/A converter output) and D/A converter binary input from DB[07:00] for each voltage bus.

There is a difference in the trip voltage for channel C from one system to the other. This is because the model 210 needs a four channel OVP module to handle -3.4 Vdc, -5.2 Vdc, +5 Vdc, and BBU +5 Vdc. To make this work with the three channel H7386 module, +5 Vdc and BBU +5 Vdc are diode ORed on the OVP backpanel. The difference in trip voltage is the voltage drop across the diodes, 0.7 Vdc.

Table 6–20   OVP Voltage Trip Reference Settings

Channel	Bus Voltage (Vdc)	Model 400 Systems		Model 210	
		Trip Voltage (Vdc)	DB[07:00]	Trip Voltage (Vdc)	DB[07:00]
A	-3.4	-4.219	6C	-4.219	6C
B	-5.2	-6.016	9A	-6.016	9A
C	5.0	6.016	9A	5.313	88

6.8.2.3 Setting the Latch

The bus voltage is compared to the voltage trip reference set by the D/A converter. If the bus voltage exceeds the reference, the latch is set. The latch may also be set by the following signals:

- **FIRE CROWBAR B H** — Provisions are made for external circuitry to activate an individual channel. All three channels have this crowbar fire signal but they are disabled because they are tied to FIRE CROWBAR RETURN.

- **SEQUENCE IN B H** — The sequence-out signal from one channel may be connected to the sequence-in signal of another channel, so if the crowbar of one channel (sequence-out) is fired, the other channel's crowbar is fired also. SEQUENCE OUT A is connected to SEQUENCE IN B on the OVP backpanel to allow a -3.4 V bus to disable the -5.2 V bus for a -3.4 V bus overvoltage condition.

- **FIRE ALL CROWBARS H** — FIRE ALL CROWBARS H is routed to each of the channels to allow all three channels to be fired at one time. FIRE ALL CROWBARS H is tied to FIRE ALL CROWBARS RTN H to disable this feature.

6.8.2.4 Gate Fire Circuitry

The gate fire circuitry is enabled when the latch sets, if the gate fire circuitry has not been disabled by tying the enable input (ENA B in this case) to common. Only channels B and C have the enable signal, channel A is not capable of being disabled. Channels B and C are both disabled for all OVP modules. This prevents firing an SCR for the +5 Vdc, BBU +5 Vdc, or -5.2 Vdc buses.

NOTE

The model 210 system does not have an SCR on the +5 Vdc or -5.2 Vdc buses.

The gate fire circuitry contains logic necessary to generate a clocking signal for the SCR gate. This clock is a 20 μs pulse every 120 μs, and fires the SCR each time it is asserted, shorting the bus to ground. The clock continues to be sent to the SCR until power is removed from the OVP module.

The SCR clocking signal is directed to the SCR gate board for rectification and filtering, before being applied to the SCR gate.

6.8.2.5 Other OVP Outputs

Setting the latch asserts SEQUENCE OUT B H. SEQUENCE OUT A is connected to SEQUENCE IN B on the OVP backpanel to ensure that an overvoltage condition detected on the -3.4 V bus shuts down the -5.2 V bus.

CROWBAR FIRED B H is also asserted. The crowbar fired signals are routed to the respective RIC STATUS [10] input to inform the RIC of an overvoltage condition. This input also disables all converters on the bus.

NOTE

Crowbar fired does not necessarily inform the RIC that the SCR has been fired unless channels B and C are enabled to fire the SCR (they are not). It only informs the RIC that an overvoltage condition exists, and if enabled, that the SCR has been fired.

Another signal that may be asserted by setting the latch is FIRED FIRST B H.

The signal is asserted if channel B is the first to detect an overvoltage condition, as noted by the deassertion of the FIRED FIRST A H (OV IND A) and FIRED FIRST C H (OV IND C). The assertion of any of the fired first signal lights the associated red LED (OV1, 2, or 3) on the OVP module, and prevents the other channels from asserting FIRED FIRST (and lighting their respective LED). The only way for all three LEDs to be lit is if FIRE ALL CROWBARS activated all three channels simultaneously, a feature that is disabled.

6.8.3 OVP LEDs

The OVP module has one green LED and three red LEDs (Figure 6–27).

* **RDY (green)** — The OVP module on-board power supply is providing enough voltage for the module to function, the module has been reset, it is ready for operation, and no OVP module channel has detected an overvoltage condition.

* **OV1 (red)** — Bus A is the first bus to go overvoltage and channel A is the first to be activated.

* **OV2 (red)** — Bus B is the first bus to go overvoltage and channel B is the first to be activated.

* **OV3 (red)** — Bus C is the first bus to go overvoltage and channel C is the first to be activated.

NOTE
The assertion of FIRE ALL CROWBARS activates all three channels simultaneously, and lights all three LEDs. This feature is disabled.

MR_X·066_89
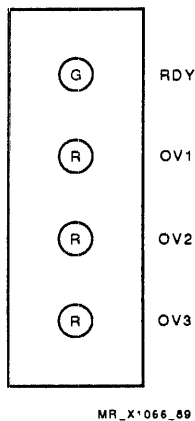
Figure 6–27   OVP LEDs

6.9 Power and Environmental Monitor (PEM)

The power and environmental monitor (PEM) is a module based on an 8031 microprocessor that resides in the service processor (SPU) BI card cage. It gathers power and environmental information from the power control system (PCS) and communicates exception conditions to the SPU. It also manages the operator control panel (OCP) and battery backup units (BBUs).

Figure 6–67 shows the relationship between the SPM, PEM, and the various units in a model 210 system configuration while Figure 6–68 shows the same relationship in a model 440 system configuration. The signal interface panel (SIP) collects and distributes all power system control and status signals between PEM and all units within the PCS, including the OCP, MCM, and the BBU subsystem.

Five 30-conductor cables connect the PEM and SIP, and a single 30-conductor SPM to PEM interface cable (SPI) connects the PEM and SPM. All six SPU BI bus backpanel cables are connected to the user pins in slots C through E. The BI AC LO, BI DC LO, and BI reset signals connect to the PEM using the standard BI bus pins in slot A.

6.9.1 SPI Communication

The SPM-to-PEM interface (SPI) provides the communication path between SPM and PEM. The SPM uses this path to:

- Command the PEM to power the system up and down

- Run invokable ROM based diagnostics

- Retrieve up-to-date environmental and power status/error information

6.9.2 PCS System Configuration

On system power-up or partial power-down, the PEM must configure or reconfigure the system. This involves determining which register intelligence cards (RICs) are both present and operable (no self-test failures) and which are not. The PEM also checks the legality of the configuration represented by these RICs.

6.9.3 RIC Regulator Intelligence Card Management

The PEM provides the following RIC management functions:

- Accepts RIC exception messages and passes them through to the SPM

- Manipulates RIC registers for specific SPM/PEM commands (poweron, poweroff, margin, set, sense, and so on)

- Performs exception polling to ensure that no RICs become unavailable during steady state operation

6.9.4 Powerfail Signal Management

The PEM hardware detects a number of emergency power-down conditions represented by the assertion of powerfail signals. The PEM firmware detects the assertion of these signals, posts error codes to the OCP diagnostic display, and prepares for a full or partial system shutdown.

6.9.5 OCP Management

The PEM maintains the diagnostic display LEDs on the OCP and monitors the state of the OCP keyswitches. It also provides the SPM with access to the state of the OCP LEDs (front panel indicators).

6.9.6 Diagnostics and Error Checking

The PEM contains firmware for detecting and isolating fault conditions. This firmware is executed on power-up or PEM reset, and can also be dispatched through service processor commands. The PEM also contains firmware for detecting and recovering from runtime errors.

6.9.7 PEM Physical Description

The T1060 PEM module mounts in slot 4 in the standard 6-slot VAXBI card cage that houses the SPU modules.

6.9.8 PEM Functional Overview

During typical operation, the SPU software, resident in RAM on the SPM module, communicates with the firmware, resident in EPROM or EEPROM on the PEM, using SPM-to-PEM interface (SPI). In turn, the PEM firmware communicates with the firmware, resident in EPROM or EEPROM on each RIC, using the RICBUS to access individual PCS control and status signals.

The communication involves sending and receiving message packets over the SPI and RICBUS, which is covered in in detail Chapter 7.

There are two major types of transactions. The first is initiated by the SPU and the second is initiated by the PCS.

- The SPU software sends a command packet to the PCS and receives a response packet from the PEM or RIC to acknowledge receipt of the command.

- The PEM or RIC sends an exception packet to the SPU software to signal detection of an atypical change in the power system or environment.

6.9.8.1 SPU-Initiated PCS Transaction

Figure 6–28 shows the relationship between the SPU software and the PEM/RIC firmware during an SPU-initiated transaction.

The transaction is initiated when the user types the following command on the console:

>>> SHOW ENV

to display the state of the system environment.

The following sequence is initiated:

1. The SPU software reads and parses the command.

2. The SPU software builds the required SPI command packet and sends it to PEM over the SPI.

3. The PEM firmware reads and decodes the SPI command packet, reformats it into a RIC command packet, and sends it out on the RICBUSes where all RICs receive the message. The designated RIC is responsible for recognizing the RIC ID in the message and accepting the message.

4. Each RIC reads and decodes the RIC command packet and reads the state of the environment that it is responsible for.

5. The RIC firmware then builds and returns a RIC reply packet to the PEM over the RICBUS.

6. The PEM receives the RIC reply packets, containing the environmental information, and builds and sends an SPI reply packet to the SPM over the SPI.

7. Finally, the SPU reads and decodes the SPI reply packets and displays the state of the environment on the user terminal.

MR_X0453_89
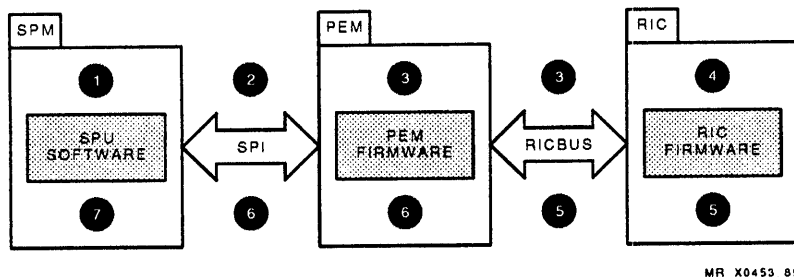
Figure 6–28 Command/Reply Message Sequence

6.9.8.2 PCS Exception Transaction

Figure 6–29 shows the relationship between the SPU software and the PEM/RIC firmware during a PCS-initiated transaction.

A RIC senses an overtemperature condition in a system cabinet and is required to signal the condition to the SPU software. The following sequence of events is initiated:

1. The RIC hardware senses the overtemperature condition during exception polling.

2. The RIC firmware builds the required RIC exception message and sends it to PEM over the RICBUS.

3. The PEM firmware reads and decodes the RIC exception packet, reformats it into an SPI exception packet, and sends it to the SPM over the SPI.

4. Finally, the SPU software reads and decodes the SPI exception packet, decodes and formats the overtemperature status information, and displays and logs the error.

NOTE
Depending upon the severity of the overtemperature alarm, the RIC firmware may initiate an automatic system shutdown sequence (ASD).

MR_X0454_89
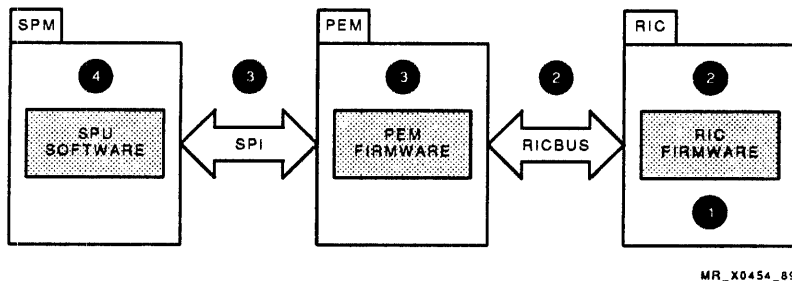
Figure 6–29   PCS Exception Message Sequence

6.9.9 PEM Block Diagram

This section describes the PEM hardware using the simplified module block diagram (Figure 6–30). Since the field replaceable unit (FRU) is the PEM module itself, detailed descriptions of the control logic contained on the PEM are not included. The level of detail is limited to describing the operation of the PEM in terms of the major logic components.

6.9.9.1 Major Components

For purposes of explaining the operation of the PEM, the logic on the module is partitioned into four major areas.

    An 8031 microprocessor chip
    Local storage (PROM, EEPROM, and RAM)
    The SPI register interface
    The SIP register interface
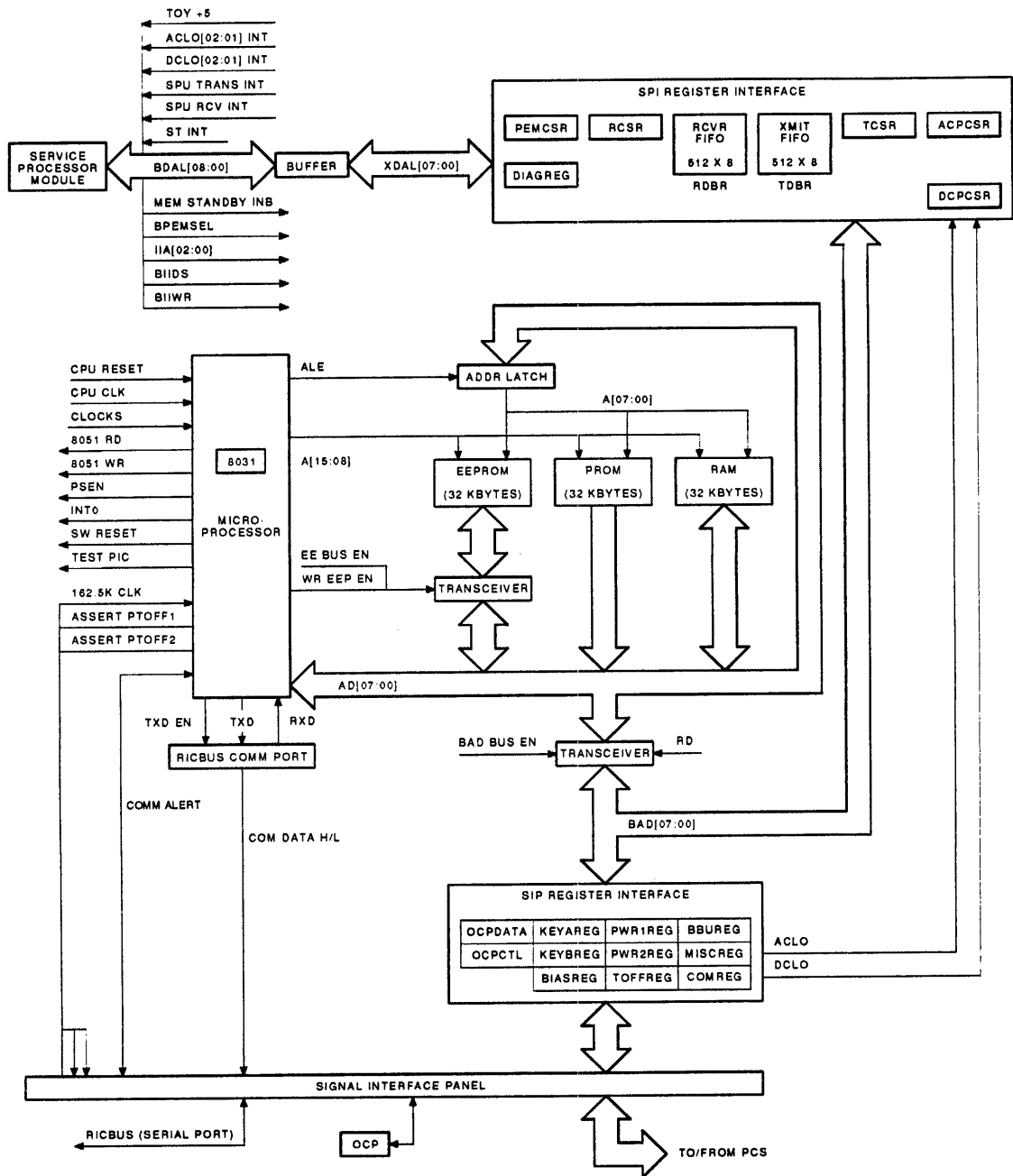
Figure 6–30   PEM Module Block Diagram

6.9.9.1.1 8031 Microprocessor Chip
An 8031 microprocessor chip provides the main processing element on PEM. It is driven by firmware stored in PROM and in EEPROM, which manages the orderly transmission of information packets between SPI and SIP.

6.9.9.1.2 Local Storage
The PEM contains three types of on-board storage.

* **EPROM** — Provides 32 Kbytes of read-only storage for fixed PEM firmware that includes the hard-core self-tests.

* **EEPROM** — Provides 32 Kbytes of storage for PEM firmware that may be down-line loaded from the SPM to facilitate field updates.

* **RAM** — Provides 32 Kbytes of read/write working storage, which is used by the firmware to hold operating limits and process message packets between SPM and PCS.

6.9.9.2 SPI Register Interface
A set of eight hardware registers provides the control and data paths between SPM and PEM. They are:

* DC power control and status register (DCPCSR)

* AC power control and status register (ACPCSR)

* Diagnostic register (DIAGREG)

* PEM control and status register (PEMCSR)

* Transmit control and status register (TCSR)

* Receive control and status register (RCSR)

* Transmit data buffer register (TDBR)

* Receive data buffer register (RDBR)

6.9.9.3 SIP Register Interface
A set of seven registers provides the control and data paths between PEM and the SIP. These registers are all located on the SIP. See Section 6.2.2.3.

6.9.9.4 OCP Register Interface
A set of seven registers provides the control and data paths between PEM and the OCP. These registers are all located on the OCP. See Section 6.1.4.

6.9.10 SPI Port Registers

The SPU software communicates with the PEM firmware at the port level by reading and writing one or more of eight hardware registers over the SPI. Table 6–21 lists the eight registers along with their address assignments in SPU space. These addresses are not used to access the registers directly, since the PEM is not a BI node. The addresses are simply decoded on the SPM and used to control the SPI PEM select and register address lines (low-order five bits).

Table 6–21   SPI Port Registers

SPM Address	Name	Register
200A8000	RCSR	Receive control and status register
200A8004	RDBR	Receive data buffer register
200A8008	TCSR	Transmit control and status register
200A800C	TDBR	Transmit data buffer register
200A8010	ACPCSR	AC power control and status register
200A8014	DCPCSR	DC power control and status register
200A8018	DIAGREG	Diagnostic register
200A801C	PEMCSR	PEM control and status register

6.9.11 PEM Port Registers

Each of the PEM port registers is an 8-bit register, but there is a ninth bit that is read each time a register is read. This bit, loopback, indicates that the PEM-to-SPM interface is in the tri-stated loopback mode. This mode allows the PEM to perform built-in self-tests (BIST). When loopback is asserted, any data the SPU reads from a register contains invalid information. Any bits the SPU writes to a PEM register will not be read by the PEM. The SPU should not access any of these registers if this bit is asserted.

6.9.11.1 Receive Control and Status Register (RCSR)

The receive control and status register (RCSR) controls the transfer of data from the PEM to the SPM through the receive data buffer register (RDBR). It contains status (done and error) bits, along with interrupt enable bits that allow the PEM to interrupt the SPU software when an error is encountered or an information packet is to be sent.

RCSR

07	06	05	04	03	02	01	00
RCV DON H	RCV IEN H	RCV ERR H	RNF H	RNE H	N/U	RTE H	CMD DON H

MR_X0504_90
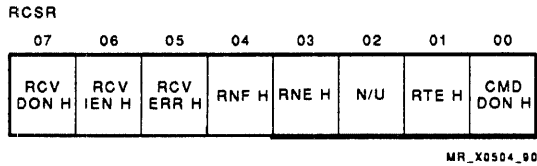
Figure 6-31 PEM RCSR

- **BIT 0: CMD DON H (COMMAND DONE)** — Set by the PEM upon completion of a PEM port command and issued by the SPM through the port command field of the PEMCSR. The SPM polls this bit to determine when the PEM has completed the command. The SPM, upon learning that the PEM has completed the command issues a null command, which directs the PEM to reset the command done bit.

- **BIT 1: RTE H (RUN TIME ERROR)** — When set, indicates to the SPM that a PEM runtime error has occurred or that a PEM hard-core diagnostic failed one or more times, than passed. It is cleared by the SPM with the port command, clear runtime error. The SPU actively polls this bit.

- **BIT 2: REMOTE SPU L** — Asserted Low when the service processor access switch is in the Remote position.

- **BIT 3: RNE H (RECEIVE FIFO NOT EMPTY)** — When asserted, indicates to the PEM that the SPM receive FIFO is not empty. RNE H is also bit 8 of the receive data buffer register. RNE H can be read through either the RCSR or the RDBR, but causes a byte of data to be extracted from the FIFO if read through the RDBR.

- **BIT 4: RNF H (RECEIVE FIFO NOT FULL)** — When asserted, indicates that the receive FIFO contains less than 512 bytes of data. Provided for status only.

- **BIT 5: RCV ERR H (RECEIVER ERROR)** — Set by the SPM to indicate that there was a checksum error in the last PEM-to-SPM message packet. RCV ERR H is set by the SPM before RCV DONE H is cleared. The PEM firmware checks RCV ERR H when it notices that RCV DONE H transitioned from high to low. If RCV ERR H is set, the PEM retransmits the message and clears RCV ERR H before setting RCV DONE H.

- **BIT 6: RCV IEN H (RECEIVER INTERRUPT ENABLE)** — When set by the SPM, enables SPM receiver interrupts if RCV DONE H is asserted. If RCV DONE H is not already asserted when this bit is set, an interrupt occurs on its assertion.

- **BIT 7: RCV DONE H (RECEIVER DONE)** — Set by the PEM to indicate that the receive FIFO contains a message. It is cleared by the SPM when it has read the message. If RCV IEN H is set, the transition of this bit from low to high will cause an SPM interrupt. The receiver interrupt is cleared by a read of RDBR.

6.9.11.2 Receive Data Buffer Register

The read-only receive data buffer register (RDBR) is the data extraction point in the physical link between PEM and SPM. It consists of an 8-bit parallel path that uses the output from a 512-Kbyte FIFO buffer called SPM receive FIFO. During PCS-initiated transactions, the SPU software retrieves response and exception packets from this buffer.

RDBR

07	06	05	04	03	02	01	00

RECEIVE FIFO DATA

MR_X0505_90
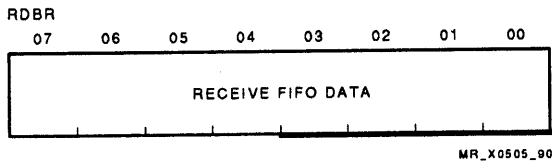
Figure 6–32   PEM RDBR

BITS [07:00]: RECEIVE FIFO DATA (COMMAND DONE) — This register holds the data written to the SPM by the PEM through the receive FIFO. Data is valid in this register for all reads if RNE H is high after each read, or if RNE H transitions from high to low as is the case on the last read.

6.9.11.3 Transmit Control and Status Register

The transmit control and status register (TCSR) controls the transfer of data from the SPM to the PEM through the transmitter data buffer register. Like the RCSR, it contains status and control bits that allow the SPU to control access to the transmit FIFO when sending information to PEM.

TCSR

07	06	05	04	03	02	01	00
TR RDY H	TR IEN H	TR ERR H	TNF H	TNE H	PEMBIT	N/U	CLR FIFO H

MR_X0506_90
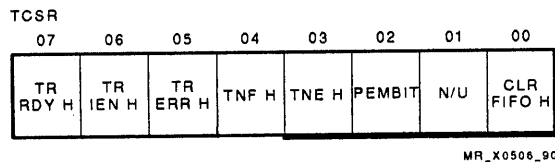
Figure 6–33   PEM TCSR

- **BIT 0: CLR FIFO H (Clear transmit FIFO)** — When set by the SPM, this bit clears the transmit FIFO and all data in the FIFO will be lost. It also causes the TNE H bit to clear and the TNF H bit to set.

- **BIT 1:** Unused, reserved — Reads as 0.

- **BIT 2: PEMBIT** — This bit reads as a zero on all T1060 boards prior to board revision C. On T1060 boards of revision C and higher, this bit will read as high.

- **BIT 3: TNE H (TRANSMITTER FIFO NOT EMPTY)** — When CLEAR, this bit indicates that the transmit FIFO is empty. This bit will be cleared if the CLR FIFO H bit (bit 0) is asserted.

- **BIT 4: TNF H (TRANSMITTER FIFO NOT FULL)** — This bit, when CLEAR, indicates that the transmit FIFO is full. This bit will be set if the CLR FIFO H bit (bit 0) is asserted.

- **BIT 5: TR ERR H (TRANSMITTER ERROR)** — Indicates that a checksum error occurred on the last message. The SPM should check TR ERR H whenever a transmitter interrupt is received from the PEM and retransmit the previous message and clear TR ERR H if TR ERR H has been set by the PEM. Note that TR ERR H is valid only when TR RDY H is set.

- **BIT 6: TR IEN H (TRANSMITTER INTERRUPT ENABLE)** — When set by the SPM, enables SPM transmitter interrupts. An interrupt will occur immediately if TR RDY H is asserted. If TR RDY H is not already asserted when this bit is set, an interrupt will occur on its assertion.

- **BIT 7: TR RDY H (TRANSMITTER READY)** — This bit is set by the PEM to indicate that it is ready to accept another message from the SPM. It is cleared by the SPM when the transmit FIFO contains a valid data message. If TR IEN H is set, the transition of this bit from low to high will cause the SPM to interrupt. The transmit interrupt is cleared by the SPM through a read of the TCSR.

6.9.11.4 Transmitter Data Buffer Register

The 8-bit write-only transmitter data buffer register (TDBR) is the data entry point in the physical link between SPM and PEM. It consists of an 8-bit parallel path that uses a 512-byte FIFO buffer called the SPM transmit FIFO.

```
TDBR
  07     06     05     04     03     02     01     00

|                    TRANSMIT FIFO DATA                    |

                                            MR_X0507_90
```
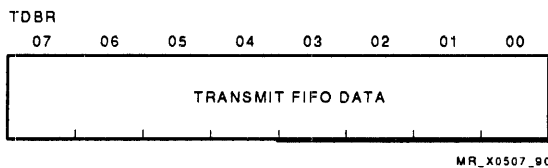
Figure 6–34   PEM TDBR

- **BITS [07:00]: TRANSMIT FIFO DATA** — This register holds the data that the SPM wishes to send to the PEM through the transmit FIFO. The PEM reset logic resets the transmit FIFO on power up.

6.9.11.5 AC Power Control/Status Register

The AC power control/status register (ACPCSR) is used by the SPM to monitor AC LO signals, to monitor the latched AC LO signals originating on PEM, and to enable or disable the interrupts to the SPM caused by a change in the state of an AC LO signal.

```
ACPCSR
  07        06       05      04       03      02       01      00

| L         | AC1    | ACLO1 | SIM     | L      | AC2    | ACLO2 | SIM    |
| ACLO1     | IEN H  | H     | MCM     | ACLO2  | IEN H  | H     | SPU    |
| H         |        |       | PF H    | H      |        |       | PF H   |

                                                    MR_X0508_90
```
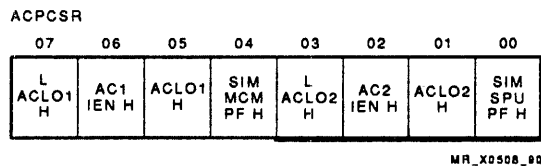
Figure 6–35   PEM ACPCSR

- **BIT 0: SIM SPU PF H (SIMULATED SPU POWER FAIL)** — Asserted by the SPU to simulate a power fail to test the functioning of the MCM module.

- **BIT 1: ACLO2 H (AC LO 2)** — Indicates that an AC LO condition has occurred on the portion of the system powered by this particular UPC 2. ACLO2 is the actual (as opposed to latched) AC LO signal provided by the UPC and reflects the actual state of the 280 Vdc bus. In a uni- or dual processor system, ACLO2 is invalid and undefined.

- **BIT 2: AC2 IEN H (LATCHED AC LO 2 INTERRUPT ENABLE)** — When set by the SPM, will enable SPM L ACLO2 interrupts. If set, an interrupt will occur on the next low to high transition of L ACLO2. AC2 IEN is cleared on power-up by the PEM reset logic.

- **BIT 3: L ACLO2 H (LATCHED AC LO 2)** — Indicates that an AC LO condition has occurred on the portion of the system powered by UPC2. In a uni- or dual processor system, L ACLO2 is asserted. L ACLO2 is cleared by the SPM during a power-up sequence. AC LO2 can be cleared only by the SPM when ACLO2 is deasserted. The low-to-high transition of L ACLO2 will interrupt the SPU if AC2 IEN is set. The L ACLO2 interrupt must be cleared by clearing AC2 IEN.

- **BIT 4: SIM MCM PF H (SIMULATED MCM POWER FAIL)** — Asserted by the console to simulate a power fail to test the functioning of the MCM module.

- **BIT 5: ACLO1 H (AC LO 1)** — Indicates that an AC LO condition has occurred on the portion of the system powered by the PFE or UPC1. ACLO1 is the actual (as opposed to latched) AC LO signal provided by the power front end and reflects the actual state of the 280 Vdc bus. In a uni- or dual processor system, ACLO1 is the only valid AC LO power fail signal.

- **BIT 6: AC1 IEN H (LATCHED AC LO 1 INTERRUPT ENABLE)** — When set by the SPM, enables SPM L ACLO1 interrupts. When set, an interrupt will occur on the next low-to-high transition of L ACLO1.

- **BIT 7: L ACLO1 H (LATCHED AC LO 1)** — Indicates that an AC LO condition has occurred on the portion of the system powered by the PFE or UPC1. In a uni- or dual processor system, L ACLO1 is the only valid latched AC LO power fail signal. It is cleared by the SPM during a power-up sequence. L ACLO1 can be cleared only by the SPM when ACLO1 is deasserted. The low-to-high transition of L ACLO1 interrupts the SPU if AC1 IEN is set. The L ACLO1 interrupt must be cleared by clearing AC1 IEN. L ACLO1 is set on power-up of the SIP.

6.9.11.6 DC Power Control/Status Register

The dc power control/status register (DCPCSR) is used by the SPM to monitor DC LO signals, to monitor the latched DC LO signals originating on PEM, and to enable or disable the interrupts to SPM caused by a change in the state of a DC LO signal.

DCPCSR

07	06	05	04	03	02	01	00
L DCLO1 H	DC1 IEN H	DCLO1 H	GRPB LO H	L DCLO2 H	DC2 IEN H	DCLO2 H	

STANDBY H

MR_X0509_90
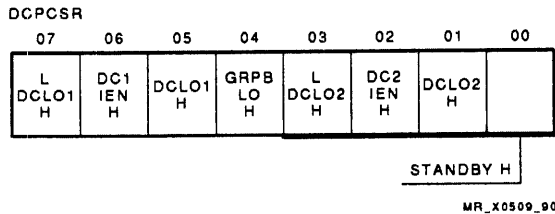
Figure 6-36   PEM DCPCSR

- **BIT 0: STANDBY H** — Asserted by the console at the time of a powerfail, to lock out the use of CPU memory.

- **BIT 1: DCLO2 H (DC LO 2)** — Indicates that a DC LO condition has occurred on the portion of the system powered by UPC2. DCLO2 is the actual (as opposed to latched) DC LO signal provided by UPC2 or converters and reflects the actual state of the 280 Vdc bus and the low voltage dc power buses. In a uni- or dual processor system, DCLO2 is the only valid DC LO power fail signal. It will be asserted if any of the following are asserted:

  - **BUS2 LO** — When asserted, indicates that the 280 Vdc bus is too low to support the regulators.

  - **GRPB LO** — When asserted, indicates that one or more of the regulator buses (with the exception of the BBU bus) in SCU CAB is not running at its specified output voltage.

  - **GRPC LO** — When asserted, indicates that one or both of the regulator buses in CPU CAB 2 is not running at its specified output voltage.

  - **GRP BBU LO** — When asserted, indicates that the BBU regulator bus in the SCU CAB is not running at its specified output voltage.

- **BIT 2: DC2 IEN H (LATCHED DC LO 2 INTERRUPT ENABLE)** — When set by the SPM, enables SPM L DCLO2 interrupts. An interrupt will occur on the next low-to-high transition of L DCLO2.

- **BIT 3: L DCLO2 H (LATCHED DC LO 2)** — Indicates that a DC LO condition has occurred on the portion of the system powered by UPC2. In a uni- or dual processor system, L DCLO2 is invalid and undefined. L DCLO2 is cleared by the SPM during a power-up sequence. DC LO2 can be cleared only by the SPM when DCLO2 is deasserted. The low-to-high transition of L DCLO2 will interrupt the SPM processor if DC2 IEN is set. The L DCLO2 interrupt must be cleared by clearing DC2 IEN.

- **BIT 4: GRPB LO H (GROUP B LO)** — When clear, indicates that the BBU regulator group output is not within specification. When set, GRPB LO indicates that BBU power to the memory is valid. GRPB LO should be checked by the SPM during its startup procedure to determine if a cold start or warm start is required.

- **BIT 5: DCLO1 H (DC LO 1)** — Indicates that a DC LO condition has occurred on the portion of the system powered by the PFE or UPC1. DCLO1 is the actual (as opposed to latched) DC LO signal provided by the PFE or converters and reflects the actual state of the 280 Vdc bus and the low voltage dc power buses. In a uni- or dual processor system, DCLO1 is the only valid DC LO power fail signal. DCLO1 is a function of the following signals.

  — **BUS1 LO** — When asserted, indicates that the 280 Vdc bus is too low to support the regulators.

  — **GRPA LO** — When asserted, indicates that one or both of the regulator buses in CPU CAB 1 is not running at its specified output voltage.

  — **GRPB LO** — When asserted, indicates that the BBU regulator bus in the SCU CAB is not running at its specified output voltage.

  — **GRPC BBU LO** — When asserted, indicates that the BBU regulator bus is not running at its specified output voltage.

- **BIT 6: DC1 IEN H (LATCHED DC LO 1 INTERRUPT ENABLE)** — When set by the SPM, enables SPM L DCLO1 interrupts. When set, an interrupt will occur on the next low-to-high transition of L DCLO1. DC1 IEN is cleared on power-up by the PEM reset logic.

- **BIT 7: L DCLO1 H (LATCHED DC LO 1)** — Indicates that a DC LO condition has occurred on the portion of the system powered by the PFE or UPC1. In a uni- or dual processor system, L DCLO1 is the only valid latched DC LO power fail signal. It is cleared by the SPM during a power-up sequence. DC LO1 can be cleared only by the SPM when DCLO1 is deasserted. The low-to-high transition of L DCLO1 will interrupt the SPM processor if DC1 IEN is set. The L DCLO1 interrupt must be cleared by clearing DC1 IEN.

6.9.11.7 Diagnostic Register

The diagnostic register (DIAGREG) is a read-only register that is used to communicate PEM diagnostic information to the SPM on a port level. The diagnostic register is the only register usable when in the uninitialized state.

```
DIAGREG
   07   06   05   04   03   02   01   00

 BROKE     PORT              DIAG
   H       STATE            STATUS

                              MR_X0510_90
```
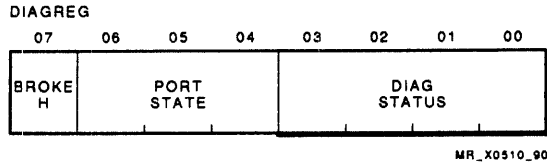
Figure 6-37   PEM DIAGREG

- **BITS [03:00]: DIAGNOSTIC STATUS** — This 4-bit field contains the diagnostic status of the PEM. It has the following diagnostic uses:

  — During the time that the port state is uninitialized, it contains the test number of the BIST currently executing. Initially, this field is cleared by the PEM reset logic, and is updated immediately before the first BIST is executed. Should a hard-core test fail, the PEM loops on the failing test, and the diagnostic status field contains the number of the hard-core test that failed.

  — When the PEM is in the enabled state and executing a command given to it by the SPM using the command/reply message interface, this register will be used to signal the SPM of PEM activity in place of the usual keep-alive packet. During the execution of the command, no keep-alive messages are accepted or returned. Upon receiving the command, this field will be set to 0000. Every 2 seconds this field will be incremented, up to a maximum count of 9, and upon completion of the command the field will be reset to 0000.

  — If an illegal port command is written to the PEMCSR, this field contains a status code of E_{16}. An illegal port command is one that requests an illegal state change.

  — If a legal port command is written to PEMCSR, but the PEM is unable to complete the command, this field will contain F_{16}.

- **BITS [06:04]: PORT STATE** — This 3-bit field contains the current port state. There are five possible states (Table 6-22).

Each time there is a change in the port state, the DIAGREG is written with the new contents for this field. Initially, this field is set by the PEM reset logic, and the initial state is uninitialized.

Table 6-22   PEM Port States

Code	PEM Port State
111	UNINITIALIZED
011	DIAGNOSTIC
001	DOWNLOAD
010	INITIALIZED
000	ENABLED

- **BIT 7: BROKE H (Adapter Broken)** — This bit is asserted upon power-up to indicate that the PEM is not operational. It is cleared if the PEM has passed all of its automatic built-in self-tests. The PEM's visual LED is directly connected to this bit, and is lit when this bit is clear and out when this bit is set.

6.9.11.8 PEM Control and Status Register

The PEM control and status register (PEMCSR) is a read/write register used by the SPM to control the operation of the PEM at the port level. It allows the SPU software to send commands to the PEM firmware to initiate changes in state during system initialization.

MR_X05·1_90
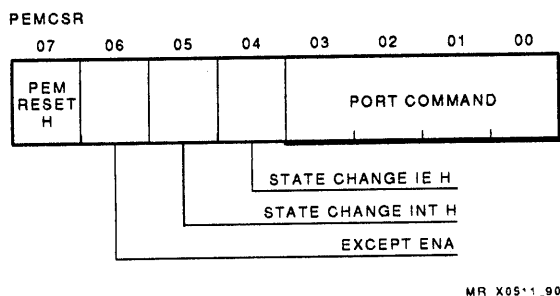
Figure 6–38   PEM PEMCSR

- **BITS [03:00]: PORT COMMAND** — This 4-bit field allows the SPM to issue a port command to the PEM. Table 6–23 lists the port commands.

  After executing the port commands, the PEM sets the CMD DON H bit in the RCSR register. To clear the CMD DON H bit, the SPM gives the PEM a NULL port command.

  An illegal port command, or a command given in the wrong state, causes the RTE H bit (RCSR) to set and prevents setting the CMD DON H bit (RCSR), causing the SPM to timeout.

Table 6–23   Port Commands — PEMCSR

Code	Port Command	Allowable Port States
0000	Null command (clear CMD DON H if set)	All
0001	Enter UNINITIALIZED State	All
0010	Enter INITIALIZED State	UNINITIALIZED
0011	Enter DOWNLOAD State	INITIALIZED/UNINITIALIZED
0100	Enter DIAGNOSTIC State	INITIALIZED
0101	Enter ENABLED State	INITIALIZED
0110	Clear the RTE H bit in the RCSR	All
0111	Clear the diagnostic status field in DIAGREG	All
1000–1111	Reserved for future use	NA

- **BIT 4: SC IEN H (STATE CHANGE INTERRUPT ENABLE)** — Enables the SCINT interrupt. If this bit is set by the SPM when there is an SCINT interrupt pending (SCINT is asserted), the interrupt is generated immediately. If there is no pending interrupt (SCINT deasserted) when this bit is set, an interrupt will occur upon the assertion of SCINT.

- **BIT 5: SCINT H** — This is a read-only field that is set when the PEM experiences a state change. It is up to the SPM to either use this transition to cause an interrupt or to ignore it and poll the state field in the DIAGREG for a state change. The bit is cleared when the SPM reads the DIAGREG.

- **BIT 6: XENA H (EXCEPTIONS ENABLED)** — This bit is set (cleared) at anytime by the SPM when it wishes to enable (disable) the sending of PEM and RIC exception messages. This bit is only polled for change by the PEM when the port state is enabled. Since this bit is polled, a time window of 1 ms exists in which exceptions may be disabled through this bit, but an exception message is still sent.

- **BIT 7: RST H (PEM RESET)** — Forces a CPU reset of the PEM 8031 processor and resets the port registers.

6.9.12 PEM Visual Indicators

The PEM LEDs are shown in Figure 6–39.


```
Ⓨ    BROKE
Ⓡ    PORT STATE 0
Ⓡ    PORT STATE 1
Ⓡ    PORT STATE 2
Ⓖ    FIFO TRANS
Ⓖ    FIFO RCV
Ⓖ    AC OK
Ⓖ    DC OK
Ⓡ    TEST
Ⓡ    LOOPBACK
Ⓡ    TOFFTEST
```

MR_X0512_90
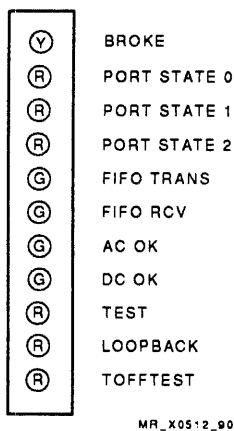
Figure 6–39   PEM LEDs

The description for each of the PEM LEDs follows:

- **BROKE** — The PEM has passed all its built-in self-tests. This LED is controlled by PEM DIAGREG[07], and is out when this bit is set.

- **PORT STATE[02::00]** — These three LEDs reflect the current PEM port state, the contents of PEM DIAGREG[06:04].

- **FIFO TRANS** — On when the PEM has control of the transmit FIFO. Off when the SPM has control of the transmit FIFO.

- **FIFO RCV** — On when the PEM has control of the receive FIFO. Off when the SPM has control of the receive FIFO.

- **AC OK** — On when SPU AC power is OK. Off when an SPU AC LOW condition exists.

- **DC OK** — On when SPU DC power is OK. Off when an SPU DC LOW condition exists.

- **TEST** — On when TEST PWRFAIL from the SIP (TSTCNTL[00]) is asserted. It is used during testing to block certain test signals. See Table 6–7.

- **LOOPBACK** — On when the PEM is running internal loopback. The SPM cannot communicate with the PEM at this time.

- **TOFF TEST** — On when TEST TOFF from the SIP (TSTCNTL[01]) is asserted. Used during testing to prevent test signals from tripping the AC input circuit breaker.

6.10 Regulator Intelligence Cards (RIC) (H7388/H7389)

This section addresses the purpose, general description, and block diagram of the H7388 CPU RIC and the H7389 I/O RIC. The H7388 is covered first, then the H7389.

These RICs share common firmware, diagnostics, and software update capability. The CPU RICs are located in the CPU and SCU cabinets, while the I/O RICs are located in the I/O adapter cabinets. The CPU RIC contains analog measurement circuitry (A/D and D/A).

The RIC is an 8031 microprocessor controlled board that turns power converters on and off, gathers power and environmental information, and compares it to expected values. If the values do not match expected values, the RIC issues a controlling response, or sends an exception mode message to the PEM to alert the system of an abnormal condition.

6.10.1 RIC Functional Description

The H7388 and H7389 RICs monitor and control the VAX 9000 H7380, H7214, and H7215 power converters, and monitor environmental parameters. The functions are to:

- Turn converters on and off for power-on and power-off conditions.

- Turn converters off for overvoltage or overcurrent conditions.

- Monitor power buses and provide error feedback to converters to control the converter output.

- Adjust H7380 output voltage for nominal voltage, high margin, or low margin conditions.

- Detect power bus undervoltage conditions.

- Provide a clock to the converters.

- Provide the converters with an overcurrent limit circuit.

- Monitor converter MOD OK signals for converter operational state.

- Control model 440 n + 1 operation.

- Monitor the state of the overvoltage protection circuit.

- Provide a reference voltage for the thermal switches.

- Monitor the state of the thermal switches.

- Monitor H7390 and H7392 conditions.

6.10.2 H7388 CPU RIC Block Diagram

This section describes the basic operation of the H7388 CPU RIC. For discussion, see Figure 6–40.
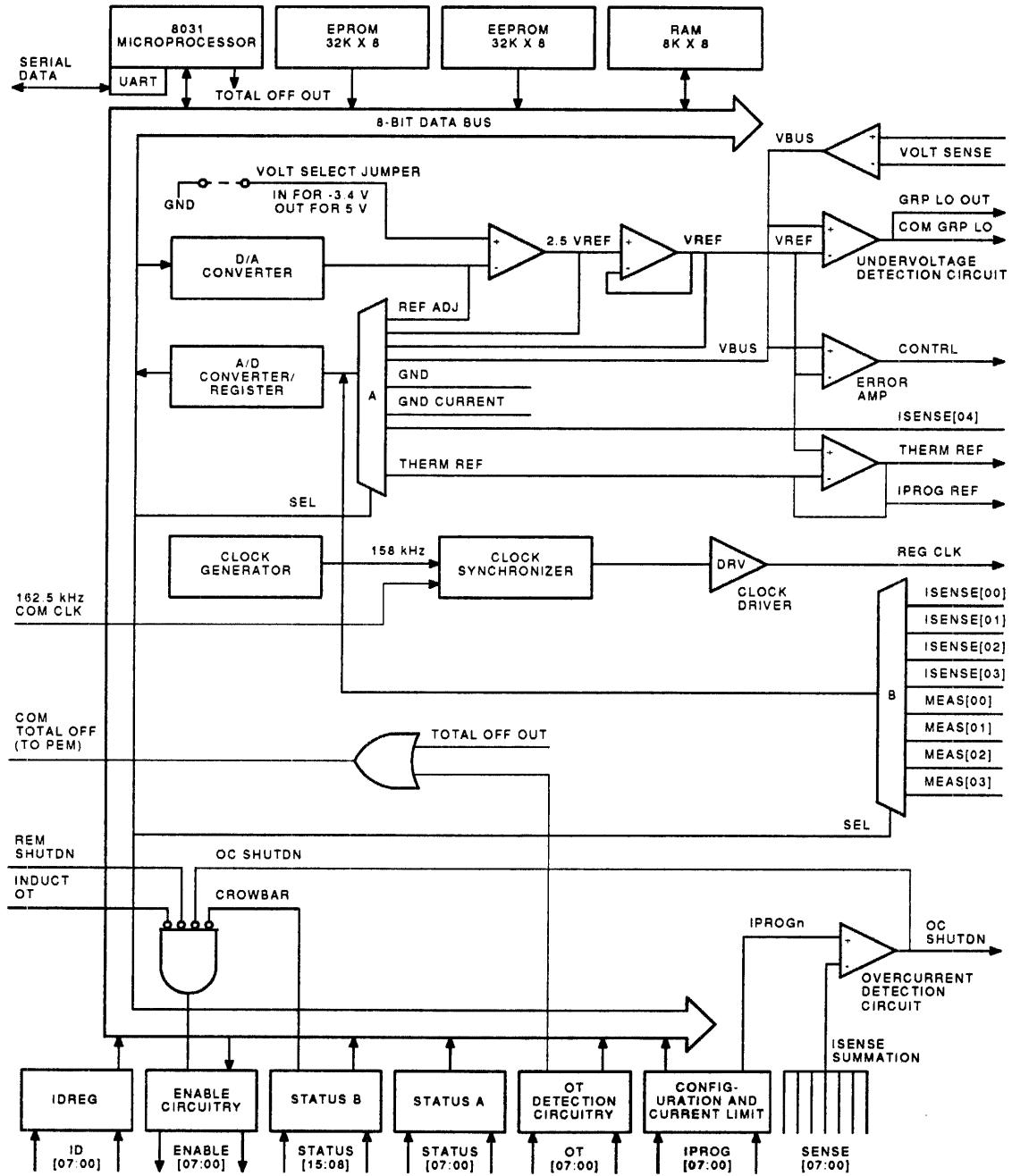
Figure 6–40   CPU RIC Block Diagram

6.10.2.1 RIC 8031 Microprocessor

The 8031 is an 8-bit 12 MHz microprocessor, which executes the program code to carry out the RIC functions. The microprocessor architecture allows it to access two separate 64-Kbyte memory spaces:

1. **Program memory space (execute code, reads, but never writes)** — Program memory space is divided into two 32-Kbyte segments (Figure 6–41). The lower half is dedicated to EPROM and the upper half is dedicated to EEPROM. Code may be executed from either of these spaces.

MR_X1068_89
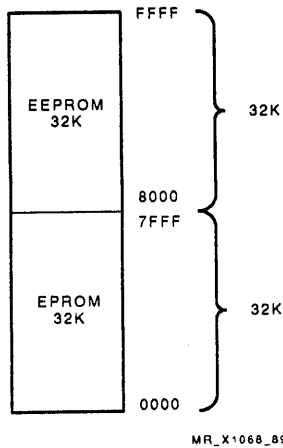
Figure 6–41   Program Memory Space

2. **Data memory space (read/write)** — Data memory space (Figure 6–42) is divided into 3 segments:

   • The lowest 16K is reserved for static RAM. Only 8K is used, 0000–1FFF.

   • The middle 16K is used to access the hardware registers. Only 2K is used, 4000–47FF.

   • The upper 32K is dedicated to writing the EEPROM.

MR_X1069_89
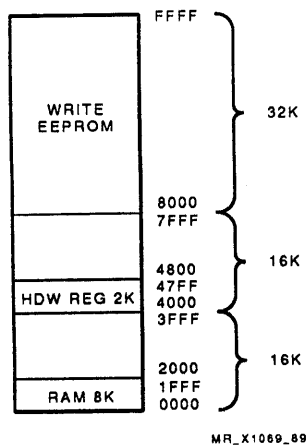
Figure 6–42   Data Memory Space

6.10.2.2 EPROM

The 32-Kbyte × 8-bit EPROM contains the code that the microprocessor executes upon power-up. This includes the hard-core tests: EPROM checksum, microprocessor internal RAM tests, external RAM tests, address bus tests, and EEPROM checksum. The EPROM executes read (register, RAM, and code), write (registers), BIS (registers), and download commands. Once EEPROM code is entered, EPROM code is not normally reentered, except for power loss, or to down-line load the EEPROM with updated code.

6.10.2.3 EEPROM

The 32-Kbyte × 8-bit EEPROM contains the BIST code, that the microprocessor executes once the EPROM completes the hard-core tests. It also contains the code that carries out the normal functions of the RIC, the code necessary to turn on or off converters, monitor temperatures or voltage conditions, or monitor power converter conditions.

If a fault is traced to the EEPROM, or the EEPROM code is out of revision, the EEPROM may be down-line loaded with new code, eliminating the necessity of physically changing the ROM.

6.10.2.4 Reference Voltages

There are three reference voltages generated by the CPU RIC:

- **VREF (5.2 Vdc or 3.4 Vdc)** — The reference voltage the error amplifier compares to the converter output, to generate a control voltage for the converters.

- **THERM REF (5.0 Vdc)** — The reference for the thermistors used in temperature measurement.

- **IPROG REF (5.0 Vdc)** — Routed to the converters to be returned as IPROG n if the converter is installed. The CPU RIC uses IPROG n to determine if a converter is installed and to set the overcurrent trip level.

The range of the reference voltages must be selected, and the voltage set up by the RIC as follows:

- Writing the D/A converter register (4080_{16}) causes the D/A converter to generate REF ADJ in increments of 19.5 mV (one bit change in the D/A register), with a range of 0–5 Vdc. REF ADJ is used to trim the voltage reference, VREF. The accuracy of VREF determines the overall accuracy of the converter output.

- The voltage reference range selection (nominal 5 Vdc or 3.4 Vdc) is determined by the RIC location in the backpanel. For 5 Vdc operation, VOLT SELECT (J1P054) remains open, whereas for 3.4 Vdc operation, VOLT SELECT is jumpered by the backpanel to VOLT SELECT RTN (J1P051), which is connected to ground on the RIC.

- With REF ADJ at midrange (2.5 Vdc), VREF is at its nominal value, 5.0 Vdc or 3.4 Vdc, depending on the RIC location. Because of the polarity of the circuit, an increase in REF ADJ causes a decrease in VREF. For nominal 5.0 Vdc, $VREF = 5.5Vdc - 0.003906* $ (D/A code). For nominal 3.4 Vdc, $VREF = 3.74Vdc - 0.002656*$ (D/A code). See Table 6–24 for D/A converter values for the voltage references.

Table 6-24   D/A Code for VREF

Voltage Selection	D/A Code	VREF
5.0^1	80_{16}	5.0
5.0^1	$4C_{16}$	5.2
3.4^1	80_{16}	3.4

[1]The voltage selection is the voltage range selected by RIC placement. It will be either 5 Vdc or 3.4 Vdc. See description of VOLT SELECT in Section 6.10.2.4

6.10.2.5 Voltage Margining

The D/A converter also margins the converters by ±5%. To prevent a sudden change in converter voltage causing an overvoltage or group low condition, margining is completed in eight steps. The RIC code increases or decreases the converter voltage by one-eighth the total margin value, allows it to stabilize for 125 ms, then increases or decreases the voltage by another one-eighth (Table 6-25).

Table 6-25   Voltage Margins

Nominal Voltage (Vdc)	Tolerance (mV)	High Margin (Vdc)	Low Margin (Vdc)
5.2	±25	5.46	4.94
5.0	±25	5.25	4.75
3.4	±25	3.57	3.23

6.10.2.6 Remote Sense, Error Amplifier, and Undervoltage Detection

The VOLT SENSE inputs (VOLT SENSE + and VOLT SENSE -) to the CPU RIC are provided by the output bus at the point of regulation. LOCAL SENSE from the H7380 is also tied to VOLT SENSE and used as a backup in case VOLT SENSE is lost (Section 6.6.5.3). They are routed through a differential amplifier (VBUS) to the error amplifier to generate the converter control voltage (CONTRL). The amplifier output, VBUS, is also routed to the A/D converter for measurement, and is an input to the undervoltage detection circuit.

The error amplifier compares the converter bus voltage (VBUS) with VREF, the reference, to generate the converter control voltage. CONTRL determines the peak of the primary current pulse in the switching regulator. When CONTRL is less than 2.5 Vdc, the converter is shut down. When CONTRL is greater than 9.0 Vdc, the converter output current is at maximum rated. For all voltages between 2.5 and 9.0 Vdc, the converter output current is proportional between 0 A and the maximum rated current.

The sensed bus voltage is an input to the undervoltage detection circuit, to be compared to VREF. If the bus voltage is less than 95% of the reference, COM GRP LO is asserted, routed to the SIP, then to the PEM, to notify the PEM that an undervoltage condition exists.

The VOK green LED on the CPU RIC remains lit as long as the bus voltage remains above 95% of nominal bus voltage.

Another signal asserted is GRP LO OUT H. For a -5.2 Vdc converter group, GRP LO OUT H is connected to REM SHUTDN H on the CPU RIC of the partner -3.4 Vdc converter group. This connection prevents the -3.4 Vdc converters from coming up until the -5.2 Vdc converters are operational, and also shuts down the -3.4 Vdc converters if the -5.2 Vdc converter bus voltage becomes more positive than -4.94 Vdc. For instance, in the model 210, bus D GRP LO OUT H is connected to bus C REM SHUTDN H (Table 6–26). REM SHUTDN H is grounded on bus D.

Table 6–26 Model 210 GRP LO OUT Connections

GRP LO OUT H		REM SHTDN H	
-5.2 Vdc Bus	RIC	-3.4 Vdc Bus	RIC
D	14	C	24

6.10.2.7 A/D Converter

The A/D converter measures system temperatures, voltage references, and ground current. It is capable of both 12-bit and 8-bit conversions, but only 12-bit conversions are used.

The data written to the multiplexer address register, 4100_{16}, selects the analog signal to be measured (Table 6–27).

Table 6–27 A/D Converter Multiplexer Address Register

Hex Data	Multiplexer	Signal Name	Signal Description
00	A	VBUS	Converter bus voltage
01	A	VREF	Converter reference voltage
02	A	GND CUR MON	Ground current voltage
03	A	REF ADJ	Converter reference adjustment
04	A	2.5 VREF	RIC 2.5 Vdc reference
05	A	5.0 VREF	RIC 5.0 Vdc reference
06	A	ISENSE 04	Voltage proportional to converters output current
07	A	GND	0 V
08	B	MEAS 0	Thermistor input 0
09	B	MEAS 1	Thermistor input 1
0A	B	MEAS 2	Thermistor input 2
0B	B	MEAS 3	Thermistor input 3
0C	B	ISENSE 00	Voltage proportional to converters output current
0D	B	ISENSE 01	Voltage proportional to converters output current
0E	B	ISENSE 02	Voltage proportional to converters output current
0F	B	ISENSE 03	Voltage proportional to converters output current

The A/D converter measures up to four temperature inputs using MEASURE[03:00]. Individual MEASURE inputs can be determined from Table 5–2.

It also measures RIC 5.0 Vdc reference (5.0 Vdc REF), 2.5 Vdc reference, reference adjust voltage (REF ADJ), ground current, VREF, ISENSE[04:00], and the converter bus voltage (VBUS).

The A/D register (Table 6–28) is a read-only register, with four addresses:

4400_{16} — initiates a 12-bit conversion
4401_{16} — initiates an 8-bit conversion (not used)
4402_{16} — reads the 8 most significant bits of the conversion
4403_{16} — reads the least significant bits of the conversion

The A/D converter deasserts A/D RDY L when the conversion is started. The microprocessor monitors A/D RDY L, and does not read the data until A/D RDY L is asserted.

Table 6–28 A/D Register Bits

Address	Data Bits	A/D Bits
4402_{16}	[07:00]	[11:04]
4403_{16}	[07:04]	[03:00]

The conversion factor defines the relationship between the value of the signal measured and the digital code that the microprocessor reads. The value of the signal is determined by multiplying the digital code (in decimal) by the conversion factor, except for the ground current measurement, which needs no conversion.

Ground Current

Ground Current: $I = A/D$ code (in decimal) mA

Voltage Conversion

$V = 0.002441 * (A/D$ code [in decimal])

Converter Current

$I = 0.02075 * (A/D$ code [in decimal])

Temperature

Temperatures are sensed by thermistors. One side of the thermistor is powered by 5.0 Vdc THERM REF from the CPU RIC. The other side is tied to a precision resistor terminated to ground. The voltage across the load resistor is a nonlinear function of temperature, which may be approximated by three linear segments over the working range of 0°C to 50°C. Over this range, the accuracy is ±1°C (Table 6–29).

Table 6–29 A/D Temperature Conversions

Temperature Range °C	A/D Code	Temperature Conversion
0 to 10	< 575	$T = 0.05251 * (A/D$ code) - 20.17
10 to 40	575–1257	$T = 0.04379 * (A/D$ code) - 15.26
40 to 50	> 1257	$T = 0.05222 * (A/D$ code) - 25.64

6.10.2.8 Overcurrent Detection and Shutdown

The current limit for each converter present is 255 A, except for model 400 systems using n + 1 redundancy. In this case, the current limit is 255 A * (number of converters present - 1).

Each converter provides a voltage level that is proportional to the output current (ISENSE n = 1 Vdc per 85 A). The CPU RIC monitors these voltage levels to determine if there is an overcurrent situation.

Each of the ISENSE inputs are summed at an analog summing junction (Figure 6–43) to provide one input to the overcurrent detection circuit. Another input is the analog sum of IPROG n (IPROG 00 to IPROG 07) from each of the installed converters with IPROG n. If the converter is installed, IPROG REF (+5 Vdc) is jumpered within the converter to IPROG n. (The microprocessor determines the number of converters present in the converter group by reading the configuration register, 4380_{16}.)

The IPROG n signals are summed to program the trip level for the overcurrent detector circuit, which compares the sum of ISENSE n inputs to the sum of the IPROG n inputs.
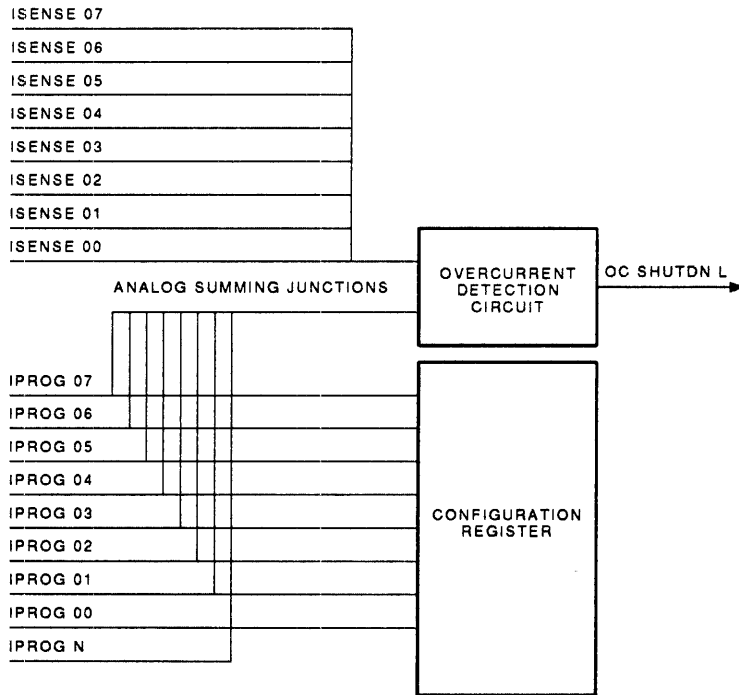
MR_X1070_89

Figure 6–43   n + 1 Redundancy

The overcurrent detection circuit works as follows. The IPROG [00] input is not connected to the overcurrent detection circuit. This provides the minus 1 factor for determining the current limit for model 400 systems. For the model 210, this indicates one less converter than is actually installed. There is an additional input to the overcurrent detection circuit, IPROG n, which is not connected for model 400 systems, but is jumpered on the backpanel to IPROG [00] for the model 210.

For example, in a model 210 with three H7380 converters on the bus, IPROG n is jumpered on the power backpanel to IPROG 00. Because three converters are installed, IPROG REF is jumpered to IPROG 00, IPROG 01, and IPROG 02 by the converters, and because IPROG n is jumpered to IPROG 00, the overcurrent detection circuit detects the reference for three converters. It compares the reference to the analog sum of ISENSE 00, ISENSE 01, and ISENSE 02.

For a model 410 system with five H7380 converters on the bus, wired for n + 1 redundancy, IPROG n is not connected to IPROG 0. The overcurrent detection circuit has ISENSE 00, ISENSE 01, ISENSE 02, ISENSE 03, and ISENSE 04 as the current sense inputs. For the reference, from IPROG REF, it only detects IPROG 01, IPROG 02, IPROG 03, and IPROG 04, or one less reference input than the actual number of converters installed.

If there is an overcurrent condition, overcurrent shutdown (OC SHUTDN L) is asserted for 1.6 seconds, which deasserts all of the enables (ENABLE n) to the converter group, to shut down the converters in the group. This is called pulsed overcurrent limiting. The converter clock is also disabled.

At the end of the 1.6 second interval, OC SHUTDN is deasserted, reenabling the converters in the converter group. If the overcurrent situation is still present, the RIC again disables the converters in the group. This continues indefinitely until the overcurrent situation ends or power is removed from the system.

When the converters are disabled for overcurrent (or by crowbar fired, remote shutdown, or inductor overtemperature), the CPU RICs power converter shutdown indicator (CONVERTER SHUT, a red LED) is lit.

6.10.2.9 CPU RIC Converter Clocks (REG CLK)
The RICs provide the clock for the power converter pulse width modulator. COM CLK, a 162.5-kHz clock from the SIP, normally provides clocking for the converters (REG CLK). An 11.059-MHz oscillator on the RIC module generates a 158-kHz clock. The clock synchronizer ensures that COM CLK is used if it is present, but allows the 158-kHz clock to take over the function of REG CLK if COM CLK is lost.

The hard-core tests verify that REG CLK is present, and that the frequency is within tolerance. If the clock speed is high or low, it is an error condition. But, if COM CLK from the SIP is missing, and the on-board clock is within tolerance, it is not an error condition. This is reported in the software control and status register (SCSREG).

6.10.2.10 Converter Enable

The converters are enabled when the microprocessor writes to the regulator enable register, 4000_{16}; are all disabled by a reset upon power-up; and are not enabled if any of the following signals are asserted:

- CROWBAR FIRED L

- REM SHUTDN L

- OC SHUTDN L

- INDUCTOR OT H

See the description of the SHUT indicator, Section 6.10.2.13, for an explanation of each of these signals.

6.10.2.11 H7380 Overtemperature Detection

Thermal switches mounted on the converter output rectifier heat sink provide a normally closed path to overtemperature return (OT RTN) in the CPU RIC. Signal contacts open at a temperature of 125°C ±5°C to open the path, which asserts OT H, the input to the RICs overtemperature detection circuit. See also Section 6.6.5.4.

OT[07:00] from the converters are prioritized, with OT07 having the highest priority. Any overtemperature latches the prioritized code, asserts LOCAL FLT L, an indication to the RIC that it detected an overtemperature condition, and asserts COM TOTAL OFF L, which is routed to the PEM and the SIP to trip H7390/H7392 CBI.

NOTE
If an overtemperature is generated due to an H7380 thermal switch failure, it will not cause CB1 to trip immediately when power is initially applied. An H7380 overtemperature cannot cause a TOTAL OFF condition until an H7380 converter has been enabled. Therefore, if the UPC/PFE CB1 trips immediately upon power-up before any H7380 converters are enabled, it is not caused by H7380 overtemperature. It has to be H7215 (SPU) OT, Thermal Fault (UPC/PFE) or voltage unbalance (UPC).

In response to COM TOTAL OFF L, the PEM asserts COM OFF ALERT L, which interrupts each of the RICs. The interrupt is a request to the RIC, which asserted COM TOTAL OFF L to send a message identifying the RIC, and the reason for asserting COM TOTAL OFF L.

The PEM determines if the entire system, or part of the system has to be shut down, and enables the total off circuits on the SIP to shut down the proper portion of the system (Section 6.2.7).

COM TOTAL OFF L may also be asserted by the microprocessor in response to an ASD condition. See Section 8.2 for a discussion on ASD checking.

When the PEM detects COM TOTAL OFF L, it asserts COM OFF ALERT L to each of the RICs. COM OFF ALERT L is routed to each RIC microprocessor to inform them of the impending power-down condition. Each RIC checks its own POWER FAIL 1 REGISTER (4280_{16}) to determine if it is responsible for COM TOTAL OFF L being asserted (LOCAL FLT L, bit 03 is asserted). If not, the RIC stops what it is doing to clear the RICBUS and resets its master interrupt enable bit. The RIC that has LOCAL FLT set informs the PEM of its RIC ID and fault code (Power Fail 1 Register[02:00]). These two bytes of information are sent to the PEM three times, a departure from the XXNET protocol. In case of line glitches, the PEM uses two out of three voting to determine the cause of the fault.

See description of SHUT indicators for information regarding inductor overtemperature (Section 6.10.2.13).

6.10.2.12 CPU RIC Registers

The CPU RIC register bitmaps are provided, with a brief description of the register. If the register is discussed in another section, a pointer to that section is provided. Table 6–30 provides the mnemonic used for console examine/deposit access.

Table 6–30   CPU RIC Registers

Address	Register Name	Access	SPU Access
4000	Enable	R/W	RENREG
4080	D/A	R/W	DAREG
4100	ID register	R/O	IDREG
4100	MUX address	W/O	MUXREG
4180	Status A	R/O	HWSREG BYTE 0
4200	Status B	R/O	HWSREG BYTE 1
4200	Warm start	W/O	NA
4280	Power fail 1	R/O	PFREG BYTE 0
4280	GRP LO LAT reset	W/O	NA
4300	Power fail 2	R/O	PFREG BYTE 1
4380	Configuration	R/O	NA
4380	Off-alert interrupt	W/O	NA
4400	A/D 12-bit conversion	R/O	ADREG[1]
4401	A/D 8-bit conversion	R/O	NA
4402	A/D data [11:04]	R/O	NA
4403	A/D data [0000 I 03:00]	R/O	NA

[1]Examining the ADREG will not initiate a measurement.

6.10.2.12.1 CPU RIC Enable Register

The enable register (Figure 6–44) is used by the RIC microprocessor to enable or disable an individual H7380 converter (Section 6.10.2.10).
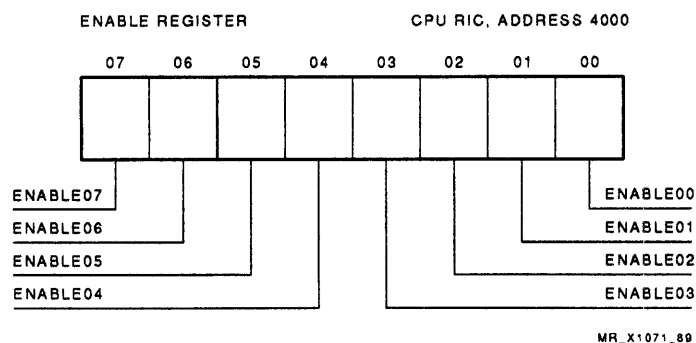
Figure 6–44   CPU RIC Enable Register

6.10.2.12.2 CPU RIC D/A Register

Writing to the D/A register (Figure 6–45) causes the D/A converter to provide an output voltage in the range of 0 to 10 volts, which is equivalent to the register contents. Section 6.10.2.4 describes the use of the D/A register, and the various CPU RIC reference voltages.

D/A REGISTER   CPU RIC, ADDRESS 4080

07	06	05	04	03	02	01	00
D/A BIT 7	D/A BIT 6	D/A BIT 5	D/A BIT 4	D/A BIT 3	D/A BIT 2	D/A BIT 1	D/A BIT 0

MR_X1072_89
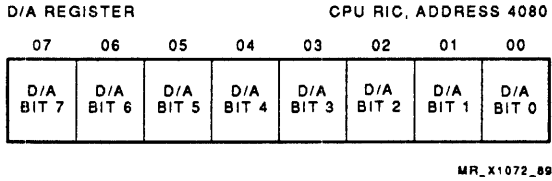
Figure 6–45   CPU RIC D/A Register

6.10.2.12.3 CPU RIC ID Register

The ID register (Figure 6–46) is a read-only register, which the microprocessor reads to determine the number that the RIC uses to identify itself on the RICBUS. The ID is determined by the backpanel location. ID[07:00] is tied to RTN (RIC ground, logic 0) or left open (float for a logic 1). The microprocessor only reads the register once during power-up initialization.

ID REGISTER   CPU RIC, ADDRESS 4100

07	06	05	04	03	02	01	00
ID07	ID06	1D05	ID04	ID03	ID02	ID01	ID00

MR_X1073_89
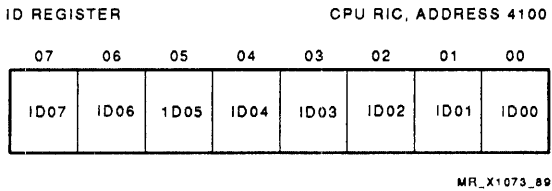
Figure 6–46   CPU RIC ID Register

6.10.2.12.4 CPU RIC MUX Address Register

The MUX address register (Figure 6–47) selects the analog signal to be measured by the A/D converter. There are two 8-to-1 multiplexers, multiplexer A and multiplexer B, which are controlled by this register. Once the signal has been selected, and after a time delay to allow the circuits to settle, the microprocessor reads the A/D converter register to determine the magnitude of the measurement. Section 6.10.2.7 describes the use of the MUX address register and the A/D converter.

MUX ADDRESS REGISTER   CPU RIC, ADDRESS 4100

07	06	05	04	03	02	01	00
				SEL MUX B			

NOT CONNECTED

MUX ADDRESS 00
MUX ADDRESS 01
MUX ADDRESS 02

MR_X1074_89
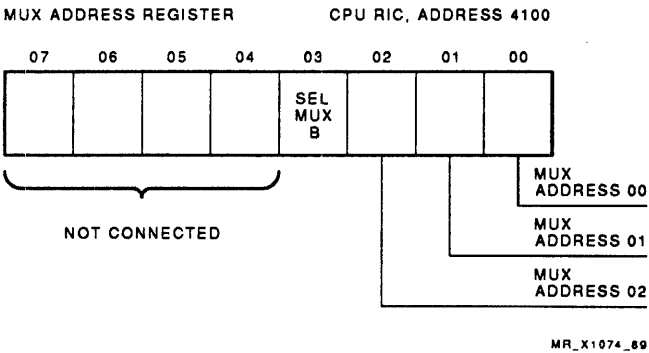
Figure 6–47   CPU RIC MUX Address Register

6.10.2.12.5 CPU RIC Status Registers

There are two status registers in the CPU RIC; STATUS A and STATUS B (Figure 6-48). They route status signals from the converters, bias supplies, and OVP module to the CPU RIC. The inputs to the status registers are system dependent and are shown for a model 210 in Appendix A. This table also provides other dynamic RIC interface signals.

STATUS A REGISTER   CPU RIC, ADDRESS 4180

07	06	05	04	03	02	01	00

STATUS 7 ─────── STATUS 0
STATUS 6 ─────── STATUS 1
STATUS 5 ─────── STATUS 2
STATUS 4 ─────── STATUS 3

STATUS B REGISTER   CPU RIC, ADDRESS 4200

07	06	05	04	03	02	01	00

STATUS 15 ─────── STATUS 8
STATUS 14 ─────── STATUS 9
STATUS 13 ─────── STATUS 10
STATUS 12 ─────── STATUS 11

MR_X1075_89
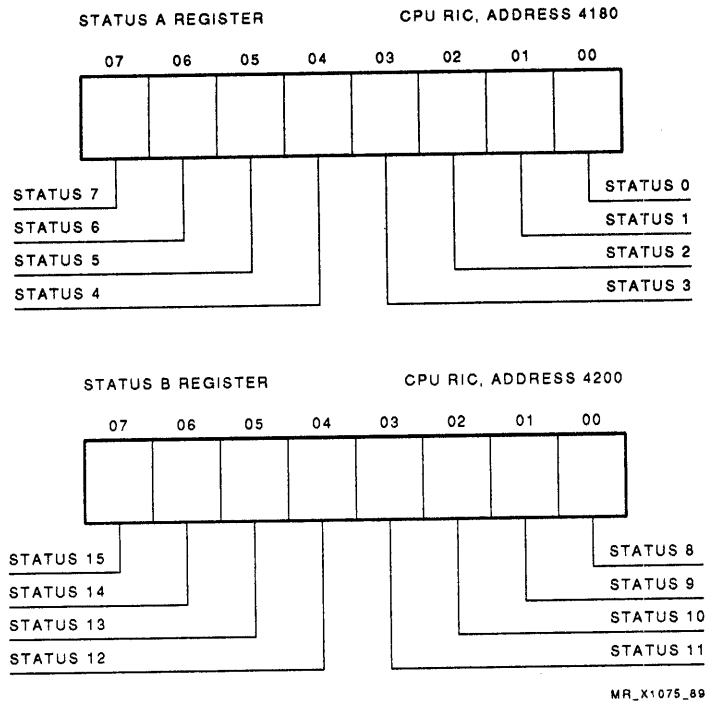
Figure 6-48   CPU RIC Status Registers

6.10.2.12.6 CPU RIC Power Fail 1 Register

Figure 6-49 shows the CPU RIC power fail 1 register bits, and Table 6-31 describes them.

POWER FAIL 1 REGISTER   CPU RIC, ADDRESS 4280

07	06	05	04	03	02	01	00
WARM START H	OFF ALERT H	CLK RUN L	GRP LO L	LOCAL FLT L	FLT 2 L	FLT 1 L	FLT 0 L

MR_X1076_89
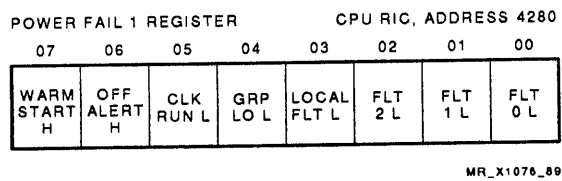
Figure 6-49   CPU RIC Power Fail 1 Register

Table 6–31   CPU RIC Power Fail 1 Register Bit Definitions

Bit Number	Signal Name	Description
0	FLT0 L	Used with FLT1 and FLT2 to indicate which overtemperature condition exists. See FLT2.
1	FLT1 L	Used with FLT0 and FLT2 to indicate which overtemperature condition exists. See FLT2.
2	FLT2 L	Used with FLT0 and FLT1 to indicate which overtemperature condition exists. These bits contain the 1's complement of the highest priority overtemperature condition. OT[07] has the highest priority. For more information on the overtemperature detection circuit see Section 6.10.2.11.

OT Line Asserted	Fault Code
OT 0	111
OT 1	110
OT 2	101
OT 3	100
OT 4	011
OT 5	010
OT 6	001
OT 7	000

Bit Number	Signal Name	Description
3	LOCAL FLT L	This bit is asserted if any of OT[07:00] are asserted. When read by the RIC it indicates that the bus monitored by this RIC is the problem.
4	GRP LO L	This bit is asserted when the converter group's output voltage drops below 95% of the reference voltage.
5	CLK RUN L	This bit is the output of a flip-flop used by the microprocessor during runtime to verify that the clock is running. The RIC hard-core tests verify that the regulator clock is running, and that the frequency is within tolerance. The frequency check cannot be made during normal operation. To check clock operation during runtime, the microprocessor resets the CLK RUN flip-flop, which should set on the next clock pulse. 6 µs later the microprocessor reads the power fail 1 register, and checks bit 5. If CLK RUN L has set, the clock is operating.

Table 6–31 (Cont.)   CPU RIC Power Fail 1 Register Bit Definitions

Bit Number	Signal Name	Description
6	OFF ALERT H	This bit is set when the PEM has asserted COM OFF ALERT L to notify the RICs that a shutdown is in progress. All RICs stop any RICBUS transmission in progress. Each RIC reads its power fail 1 register and checks LOCAL FLT L to determine if it detected the fault condition that caused the assertion of OFF ALERT. If so, it sends its RIC number and fault code to the PEM three times to inform the PEM of the problem.
		When OFF ALERT H is asserted, the RICs do not generate exception messages to the PEM. The PEM will leave OFF ALERT H asserted anytime it is unable to pass exceptions on to the SPM. Unless the PEM is in the enabled state, OFF ALERT H is asserted. When the system powers up, there could be air flow and startup type exceptions. Because it takes almost a minute for the service processor to boot and put the PEM in the enabled state, no exception messages are sent.
7	WARM START H	This bit determines if the microprocessor did a restart due to a power-up or a runtime error. Upon initial power-up, the warm start bit is cleared (this is the only way to clear this flip-flop). The microprocessor sets the bit during initialization by writing the warm start register 4200_{16}. Data is immaterial.

6.10.2.12.7 CPU RIC Power Fail 2 Register

See the description of the SHUT indication in Section 6.10.2.13 for more information on bits [04:00] of this register. Figure 6–50 shows the CPU RIC power fail 2 register bits, and Table 6–32 describes them.
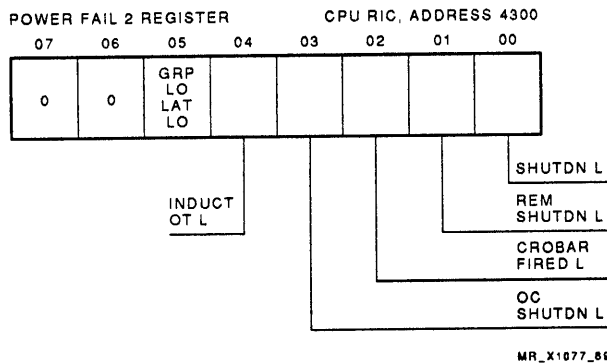
Figure 6–50   CPU RIC Power Fail 2 Register

Table 6–32   CPU RIC Power Fail 2 Register

Bit Number	Signal Name	Description
0	SHUTDN L	The shutdown bit is set when any of bits [04:01] in this register is set. It indicates that the converters on this bus are turned off.
1	REM SHUTDN L	Asserted by a -5.2 Vdc RIC to shut down its associated -3.4 Vdc bus.
2	CROBAR FIRED L	The STATUS 10 bit monitored by this RIC has been asserted to indicate that the OVP module has detected an overvoltage condition.
3	OC SHUTDN L	The RIC has detected an overcurrent condition. See Section 6.10.2.8.
4	INDUCT OT L	An overtemperature condition has been detected in the converter. The thermal fuse on the converter's output inductor has blown.
5	GRP LO LAT L	A latched version of the signal RIC9 GRP LO L. This signal is provided for debug purposes only. The signal indicates that the converter group output is less than 95% of rated output. This bit is reset by a write to the GRP LO LAT RESET L register.
6	0	
7	0	

6.10.2.12.8 CPU RIC Configuration Register

The inputs to the configuration register (Figure 6–51) indicate the number and position of the power converters in the converter group, and program the current limit set point for the converter bus (Section 6.10.2.8).
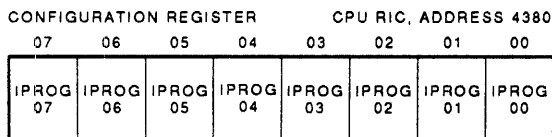
```
CONFIGURATION REGISTER          CPU RIC, ADDRESS 4380
  07     06     05     04     03     02     01     00
┌──────┬──────┬──────┬──────┬──────┬──────┬──────┬──────┐
│IPROG │IPROG │IPROG │IPROG │IPROG │IPROG │IPROG │IPROG │
│  07  │  06  │  05  │  04  │  03  │  02  │  01  │  00  │
└──────┴──────┴──────┴──────┴──────┴──────┴──────┴──────┘

                          MR_X1078_89
```

Figure 6–51   CPU RIC Configuration Register

6.10.2.12.9 CPU RIC Warm Start Register

The warm start register is not really a register, but the decode of a write to location 4200_{16} used to set the warm start bit. Any data is meaningless. Warm start, power fail 1 register [07] is set to indicate that any further restarts are to be warm starts.

6.10.2.12.10 GRP LO LAT RESET L Register

The GRP LO LAT RESET L register is not really a register, but the decode of a write to location 4280_{16} used to clear power fail 2 register [05], GRP LO LAT L. Any data is meaningless.

6.10.2.12.11 OFF ALERT INT Reset Register

The OFF ALERT INT reset register is not really a register, but the decode of a write to location, 4380_{16}. The data is meaningless. The OFF ALERT INT flip-flop, the flip-flop that interrupts the CPU RIC when it receives COM OFF ALERT L from the PEM, is reset.

6.10.2.12.12 A/D Register

The A/D register logic responds to reads to four addresses:

4400_{16} — initiates a 12-bit conversion
4401_{16} — initiates an 8-bit conversion (not used)
4402_{16} — reads the 8 most significant bits of the conversion
4403_{16} — reads the least significant bits of the conversion

Section 6.10.2.7 describes the A/D converter Figure 6–52 shows the A/D register bits.
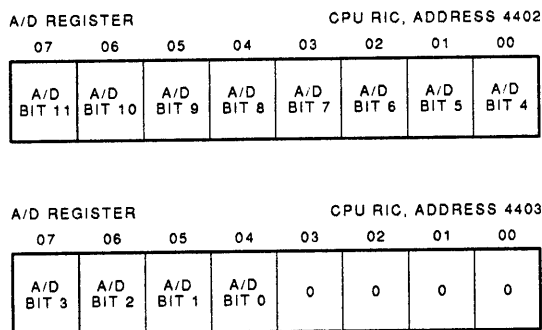
```
A/D REGISTER                      CPU RIC, ADDRESS 4402
  07     06     05     04     03     02     01     00
┌──────┬──────┬──────┬──────┬──────┬──────┬──────┬──────┐
│ A/D  │ A/D  │ A/D  │ A/D  │ A/D  │ A/D  │ A/D  │ A/D  │
│BIT 11│BIT 10│BIT 9 │BIT 8 │BIT 7 │BIT 6 │BIT 5 │BIT 4 │
└──────┴──────┴──────┴──────┴──────┴──────┴──────┴──────┘


A/D REGISTER                      CPU RIC, ADDRESS 4403
  07     06     05     04     03     02     01     00
┌──────┬──────┬──────┬──────┬──────┬──────┬──────┬──────┐
│ A/D  │ A/D  │ A/D  │ A/D  │      │      │      │      │
│BIT 3 │BIT 2 │BIT 1 │BIT 0 │  0   │  0   │  0   │  0   │
└──────┴──────┴──────┴──────┴──────┴──────┴──────┴──────┘

                              MR_X1079_89
```

Figure 6–52   A/D Register

6.10.2.13 CPU RIC LEDs
Each CPU RIC has six LEDs, which provide a visual indication of various RIC and converter functions (Figure 6-53).

MR_X1080_89
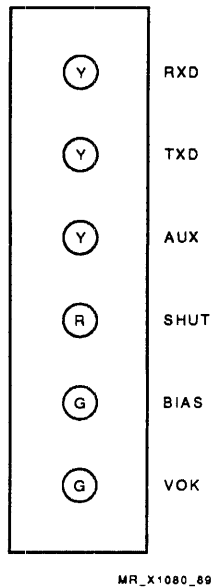
Figure 6-53   CPU RIC Indicator LEDs

- **RXD** — The RXD indicator, a yellow LED, lights each time the data received from the RICBUS is asserted high.

- **TXD** — The TXD indicator, a yellow LED, lights each time the data transmitted on the RICBUS is asserted high.

- **AUX** — AUX, the built in subtest indicator, is a yellow LED that has the following four states:

  — **OFF** — This is the initial state of the RIC. If the RIC fails to power up, or if it fails its hard-core diagnostics, the LED remains off.

  — **Blinking at a 1 Hz rate** — The RIC passed self-tests, but has not yet communicated with the PEM.

  — **Blinking at a 10 Hz rate** — The RIC detected a general self-test fault, but has successfully communicated with the PEM. The RIC does not power up the converter bus.

  — **ON** — This is the normal operating state of the RIC, and indicates that the RIC has passed both hard-core and general self-tests, and has successfully communicated with the PEM.

  — **Blinking at a 2 Hz rate with different patterns** — For hard-core failures, the RIC will loop on the failed test. While it is looping, it will blink the AUX LED for 100 ms every 2 seconds. The number of blinks depends on the failure.

    EPROM failure — one blink
    Internal RAM failure — two blinks
    External RAM failure — three blinks
    Address bus failure — four blinks

- **SHUT** — The power converter shutdown indicator is a red LED, and is lit to indicate that the converters have been shut down, and converter clock disabled for any of the following:

  - **Crowbar fired** — STATUS 10 has been asserted low to indicate that the OVP module for that converter group has detected an overvoltage condition. The SCR is fired for a -3.4 Vdc bus only.

    See Table 6–20 for the overvoltage protection bus limits.

  - **Remote shutdown** — Remote shutdown is asserted by a -5.2 Vdc CPU RIC if its -5.2 V bus drops below 95% of nominal voltage. It is used by a -3.4 Vdc RIC to shutdown the -3.4 Vdc converters in the same cabinet as the -5.2 Vdc RIC (Table 6–26).

  - **Overcurrent shutdown** — The CPU RIC shuts down the converter group for 1.6 seconds for an overcurrent condition.

  - **INDUCTOR OT H** — If a converters' output inductor overheats and the thermal fuse blows, INDUCTOR OT H is asserted to shut down the converter group. The thermal fuses for a group of converters are connected in series, with the fuse in the converter furthest from the RIC connected to ground. INDUCTOR OT H is tied to +5 Vdc in the RIC, with the voltage flowing through the fuses to ground, to keep INDUCTOR OT H deasserted. Any blown fuse causes the assertion of INDUCTOR OT H.

- **BIAS** — BIAS is a green LED, that is lit if +5 Vdc, +15 Vdc, and -15 Vdc power is being supplied to the CPU RIC by the bias supply.

- **VOK** — The VOK indicator is a green LED that is lit when the voltage sensed by the CPU RIC is at least 95% of nominal voltage.

6.10.3 H7389 I/O RIC Block Diagram

The I/O RIC is very similar to the CPU RIC. The major exception is that the I/O RIC does not have analog sensing and measurement circuitry or any A/D or D/A converters. The I/O RIC monitors different functions, and has more status registers than the CPU RIC. Also the CPU RIC needs +5 Vdc and ±15 Vdc power. The I/O RIC only needs +5 Vdc and +15 Vdc. The difference in voltage requirements is due to the lack of A/D and D/A circuitry in the I/O RIC.

For the block diagram description, items that are the same as the CPU RIC are not repeated here. See Section 6.10.2.
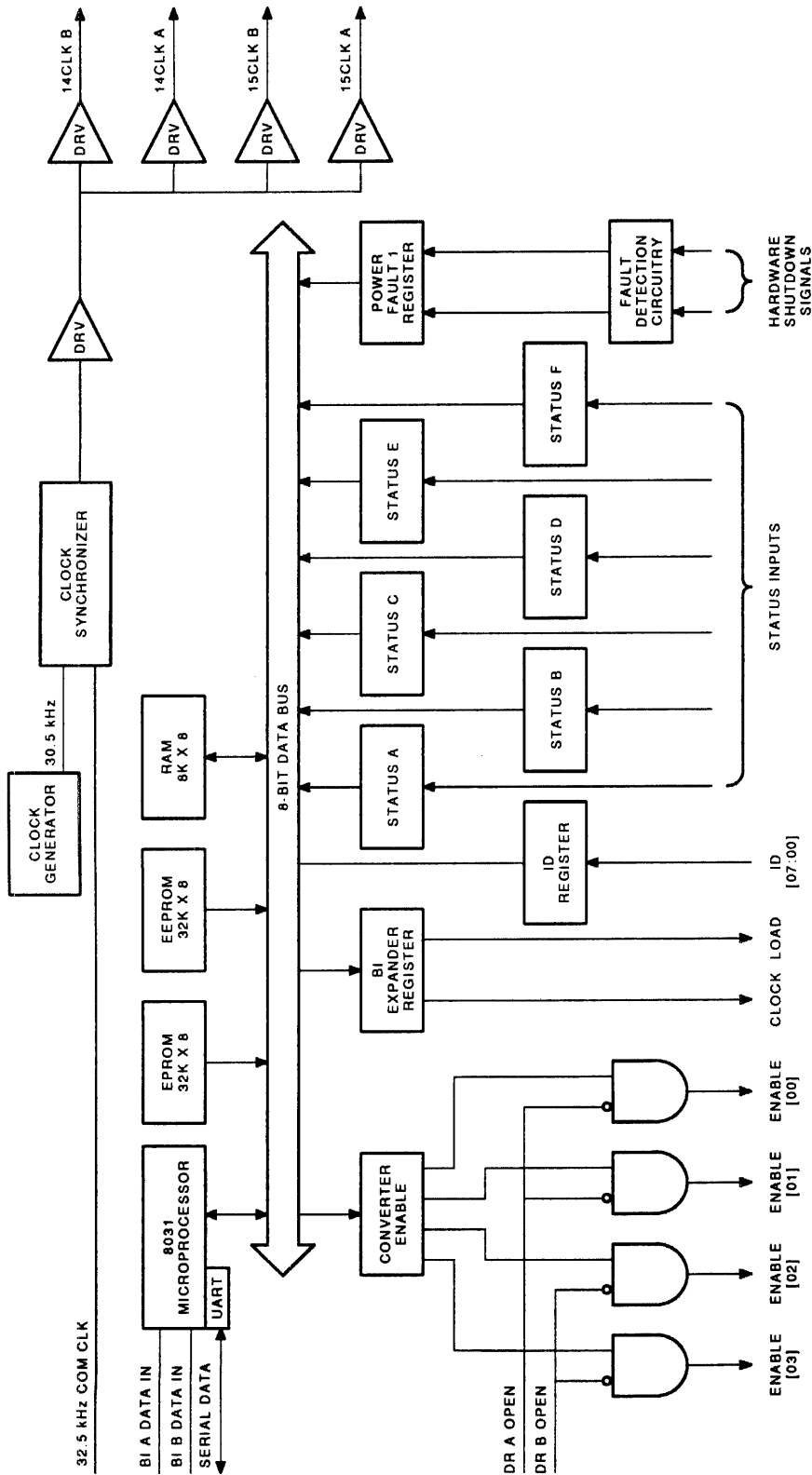
Figure 6–54   H7389 I/O RIC Block Diagram

DIGITAL INTERNAL USE ONLY

6.10.3.1 I/O RIC Regulator Clock (14CLK A and 14CLK B, 15CLK A and 15CLK B)

The clock circuitry on the I/O RIC is almost identical to the circuitry on the CPU RIC. The major difference is that the I/O RIC receives a 32.5 kHz clock from the SIP, and the on-board clock generated is 30.5 kHz.

6.10.3.2 I/O RIC Fault Detection Circuit

The fault detection circuit monitors seven inputs, four of which are used. These four fault signals are prioritized, with any of the faults causing the assertion of COM TOTAL OFF L, which is routed to the PEM, and powers down the system or one side of a model 440. The fault signals are listed in order of highest priority.

- THERM FAULT (H7392 or H7390)

- VOLT UNBALANCE (H7392)

- OV TEMP A (H7215 A overtemperature)

- OV TEMP B (H7215 B overtemperature)

There is no overtemperature detection circuitry in an H7214 regulator.

The fault detection priority encoder provides 1's complement fault code to the powerfail register (Section 6.10.3.4.1).

6.10.3.3 I/O RIC Registers

Table 6–33 describes the I/O RIC registers.

Table 6–33 I/O RIC Registers

Address	Register Name	Access	SPU Access
4000	Enable regulator	R/W	RENREG
4080	Power fault 1	R/O	PFREG
4100	ID	R/O	IDREG
4180	Status register A	R/O	HWSREG BYTE 0
4180[1]	BI expander	W/O	BIXREG
NA[1]	BI expander	R/O	BIXREG
4200	Status register B	R/O	HWSREG BYTE 1
4200	WR warm start	W/O	NA
4280	Status register C	R/O	HWSREG BYTE 2
4300	Status register D	R/O	HWSREG BYTE 3
4380	Status register E	R/O	HWSREG BYTE 4
4380	INT reset	W/O	NA
4400	Status register F	R/O	HWSREG BYTE 5

[1]A read of the BIXREG causes the microprocessor to write the BIXREG multiple times to shift the contents of two D-cards into microprocessor port 1 bits 04 and 05. The firmware then generates the 2-byte BIXREG (Section 6.10.3.4.4).

6.10.3.4 I/O RIC Regulator Enable Register

The converters are enabled when the microprocessor writes to the regulator enable register (RENREG), 4000_{16}, and are all disabled by a reset on power-up. Only ENABLE[03:00] are used to enable regulators.

This register is a read/write register used by the RIC to enable the XMI H7214/H7215 power converters. This register is reset upon power-up. Writing a 1 to a particular bit enables the corresponding converter (ENABLE[03:00] L). ENABLE[07:06] is not connected, but the register bits may still be written or read (Section 6.10.3.4). See Figure 6–55 and Table 6–34.

NOTE
The hardware has been designed to prevent enabling the H7214/H7215 converters if an XMI card cage access door is open (DR A OPEN H/DR B OPEN H). This feature is disabled by a jumper for each installed XMI card cage that grounds the DR A OPEN H/DR B OPEN H signal.

MR_X·082_89
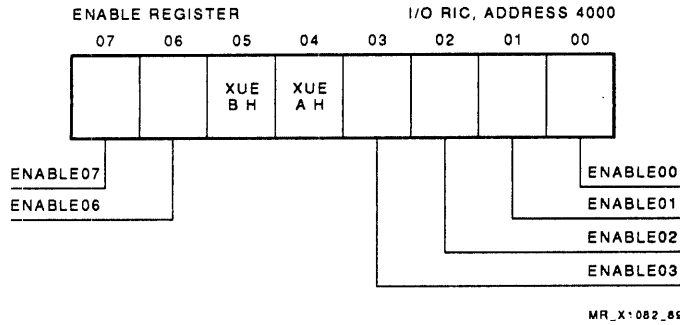
Figure 6–55   I/O RIC Regulator Enable Register

Table 6–34   I/O RIC Regulator Enable Register

Bit Number	Signal Name	Description
00	ENABLE00 L[1]	Enables the H7215 for XMI A.
01	ENABLE01 L[1]	Enables the H7214 for XMI A.
02	ENABLE02 L[1]	Enables the H7215 for XMI B.
03	ENABLE03 L[1]	Enables the H7214 for XMI B.
04	XUE A H	XMI update enable A enables XMI writing EEPROMs for any node on XMI A.
05	XUE B H	XMI update enable B enables XMI writing EEPROMs for any node on XMI B.
06	ENABLE06 L	Not used.
07	ENABLE07 L	Not used.

[1]The H7214 is powered up prior to the H7215 and the H7215 is powered down prior to the H7214.

6.10.3.4.1 I/O RIC Power Fault 1 Register

Section 6.10.3.2 describes the fault detection circuit. Figure 6–56 shows the I/O RIC power fault 1 register bits, and Table 6–35 describes them.

```
POWER FAULT 1 REGISTER          I/O RIC, ADDRESS 4080
   07      06      05      04      03      02      01      00
┌───────┬───────┬───────┬───────┬───────┬───────┬───────┬───────┐
│ WARM  │  OFF  │  CLK  │   1   │ LOCAL │  FLT  │  FLT  │  FLT  │
│ START │ ALERT │ RUN L │       │ FLT L │  2 L  │  1 L  │  0 L  │
│   H   │   H   │       │       │       │       │       │       │
└───────┴───────┴───────┴───────┴───────┴───────┴───────┴───────┘
```

MR_X1083_89
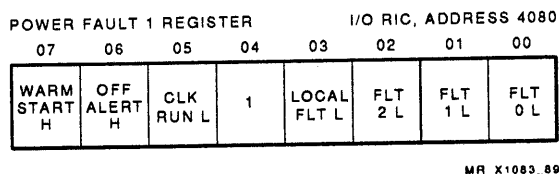
Figure 6–56   I/O RIC Power Fault 1 Register

Table 6–35   I/O RIC Power Fault 1 Register

Bit Number	Signal Name	Description
00	FLT0 L	Bit 0 of the 3-bit fault code.
01	FLT1 L	Bit 1 of the 3-bit fault code.
02	FLT2 L	Bit 2 of the 3-bit fault code. The prioritized fault codes, listed in order of highest priority, and their faults are: 100 — Thermal fault[1] 101 — Voltage unbalance[2] 110 — Overtemperature in XMI A H7215 111 — Overtemperature in XMI B H7215 (model 400 systems only)
03	LOCAL FLT L	The error detection circuitry has detected one of the four faults, as indicated by bits [02:00]. LOCAL FLT L informs the microprocessor that a fault has been detected. LOCAL FLT L cannot be set if the PEM has asserted COM OFF ALERT L (The assertion of COM OFF ALERT L by the PEM indicates that a RIC has detected a fault condition. It is a message to all RICs to cease RICBUS communication, and to the RIC that detected the fault to inform the PEM of its RIC ID and the fault code.)
04	1	This bit is tied high.
05	CLK RUN L	Clock is being provided to the H7214 and H7215 converters. At least one rising clock edge has been generated.

[1]H7392 ambient temperature has reached 55°C (131°F). H7390 SCR heat sink thermal switch has closed at 90°C (194°F).

[2]H7392 has detected that 10 mA leakage current exists between the 280 Vdc bus and the chassis. H7390 maintains this signal at a negated logic high.

Table 6–35 (Cont.)   I/O RIC Power Fault 1 Register

Bit Number	Signal Name	Description
06	OFF ALERT H	This bit is set when the PEM has asserted COM OFF ALERT L to notify the RICs that a shut down is in progress. All RICs stop any RICBUS transmission in progress. Each RIC reads its POWER FAULT 1 register and checks LOCAL FLT L to determine if it detected the fault condition that caused the assertion of OFF ALERT. If so, it sends its RIC number and fault code to the PEM three times to inform the PEM of the problem.
		When OFF ALERT H is asserted, the RIC does not generate any exception messages to the PEM. The PEM leaves OFF ALERT H asserted anytime it is unable to pass exceptions on to the SPM. Unless the PEM is in the enabled state, OFF ALERT H is asserted. When the system powers up, there may be air flow and startup type exceptions. Because it takes almost a minute for the service processor to boot and put the PEM in the enabled state, no exception messages are sent.
07	WARM START H	Determines if the microprocessor is restarting due to a power-up, or a runtime error. The bit is reset during a power-up, and is set by code during initialization.

6.10.3.4.2 I/O RIC ID Register

I/O RIC identification is determined by its position on the backpanel. ID[07:00] are tied to ground on the backpanel to provide a logic 0, or left open (logic 1 provided by pullup to +5 Vdc) to provide the I/O RIC ID. ID[07:00] are inputs to the ID register, which the microprocessor reads during power-up initialization at 4100_{16} (Figure 6–57).

ID REGISTER   I/O RIC, ADDRESS 4100

07	06	05	04	03	02	01	00
ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00

MR_X1840_89
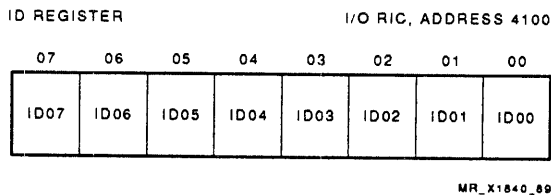
Figure 6–57   I/O RIC ID Register

6.10.3.4.3 I/O RIC Status Registers

The I/O RIC has six read-only status registers, A through F, located at addresses 4180_{16} (A), 4200_{16} (B), 4280_{16} (C), 4300_{16} (D), 4380_{16} (E), and 4400_{16} (F). They receive status from the H7214 and H7215 converters, and the H7392

The status registers are shown in Figures 6–58 through 6–63. The bits are defined for the I/O RIC in Table 6–36.
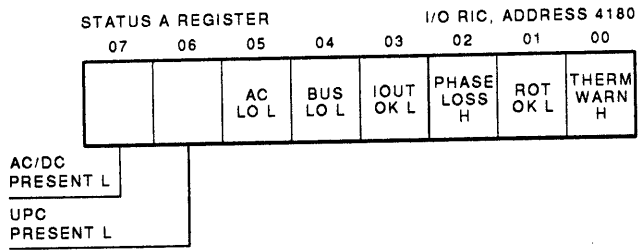
Figure 6-58   I/O RIC Status Register A
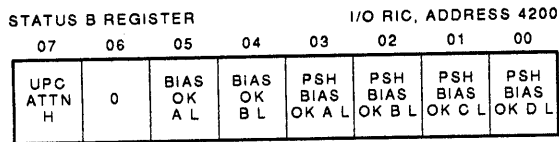
Figure 6-59   I/O RIC Status Register B
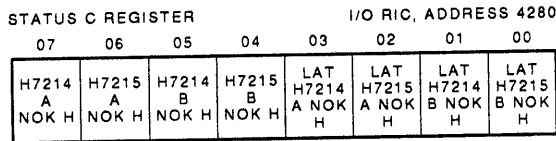
Figure 6-60   I/O RIC Status Register C
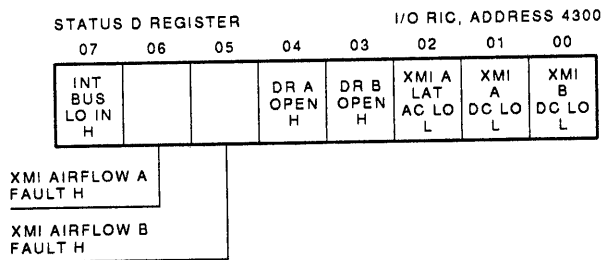
Figure 6-61   I/O RIC Status Register D
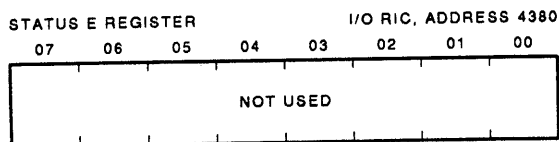
Figure 6-62   I/O RIC Status Register E

STATUS F REGISTER   I/O RIC, ADDRESS 4400

07   06   05   04   03   02   01   00

NOT USED

XMI B LAT
AC LO L

XMI A
PRESENT
L

XMI B
PRESENT
L

MR_X1089_89
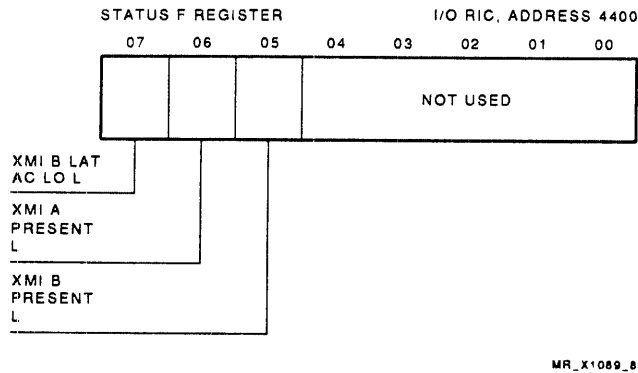
Figure 6–63   I/O RIC Status Register F

Table 6–36   I/O RIC Status Register Bit Definitions

Status Bit Number	RIC Signal	Register Bit Number	Description
			STATUS REGISTER A, 4180_{16}
00	THERM WARN H[1]	00	H7392 ambient temperature has reached 45°C (113°F).
01	ROT OK L[1]	01	H7392 phase rotation is incorrect.
02	PHASE LOSS H[1]	02	H7392 has lost one phase of the 3-phase input.
03	IOUT OK L[2]	03	H7392 output current is less than the rated current of 75 A. Deasserted if current is greater than 75 A.
04	BUS LO H	04	H7392 (H7390) has determined that the 280 Vdc bus is below 180 Vdc.
05	AC LO H	05	H7392 (H7390) has detected that the 200 Vdc bus has dropped below 195 Vdc.
06	UPC PRESENT L[2]	06	The H7392 is providing 280 Vdc.
07	AC/DC PRESENT L[3]	07	The H7390 is providing 280 Vdc.
			STATUS REGISTER B, 4200_{16}
08	PSH BIAS OK D L	00	Not used for the Model 210.
09	PSH BIAS OK C L	01	Not used for the Model 210.
10	PSH BIAS OK B L	02	The B1 section of bias supply PSC is providing bias voltages within specifications.
11	PSH BIAS OK A L	03	The A1 section of bias supply PSC is providing bias voltages within specifications.
12	BIAS OK B L	04	Only used for the Model 210 with H7390. The B section of bias supply PSB, which supplies bias to the H7390, is operating within specification.

[1]The H7390 maintains this signal at a logic low.

[2]The H7390 maintains this signal at a logic high.

[3]The H7392 maintains this signal at a logic high.

Table 6–36 (Cont.)   I/O RIC Status Register Bit Definitions

Status Bit Number	RIC Signal	Register Bit Number	Description
		STATUS REGISTER B, 4200_{16}	
13	BIAS OK A L	05	The A section of bias supply PSB, which supplies power to the I/O RIC, is operating within specifications.
14	NC	06	Read as 0.
15	UPC ATTN H	07	H7392 has detected a fault other than those reported individually in status register A.
		STATUS REGISTER C, 4280_{16}	
16	LAT H7215 B NOK H	00	Latched version of H7215 B NOK H.
17	LAT H7214 B NOK H	01	Latched version of H7214 B NOK H.
18	LAT H7215 A NOK H	02	Latched version of H7215 A NOK H.
19	LAT H7214 A NOK H	03	Latched version of H7214 A NOK H.
20	H7215 B NOK H	04	H7215 OK H has been deasserted by H7215 for XMI B.
21	H7214 B NOK H	05	CH OK H has been deasserted by H7214 for XMI B.
22	H7215 A NOK H	06	H7215 OK H has been deasserted by H7215 for XMI A.
23	H7214 A NOK H	07	CH OK H has been deasserted by H7214 for XMI A.
		STATUS REGISTER D, 4300_{16}	
24	XMI B DC LO L	00	Asserted by the RIC to notify the XMI card cage that the power front end has detected a loss of dc power.
25	XMI A DC LO L	01	Asserted by the RIC to notify the XMI cardcage that the power front end has detected a loss of dc power.
26	XMI A LAT AC LO L	02	This is a latched version of XMI A AC LO. If asserted it indicates that AC LO has been sent to the XMI A backpanel. XMI A LAT AC LO L will be asserted if the I/O RIC has detected AC LO from the H7390 or H7392 or if the I/O RIC has reset BI expander register [07], DR PRM A AC LO L, or BI expander register [05], DR PRM A RESET L for an XMI reset sequence.
27	DR B OPEN H[4]	03	The access door to XMI card cage B has been opened.
28	DR A OPEN H[4]	04	The access door to XMI card cage A has been opened.
29	XMI AIRFLOW B FAULT J	05	A loss of cooling air flow has been detected by SC1.
30	XMI AIRFLOW A FAULT H	06	A loss of cooling air flow has been detected by AF1.

[4]This feature has been disabled by connecting the DR A OPEN H/DR B OPEN H signal (I/O RIC backpanel J2-23) to ground.

Table 6-36 (Cont.) I/O RIC Status Register Bit Definitions

Status Bit Number	RIC Signal	Register Bit Number	Description
		STATUS REGISTER D, 4300_{16}	
31	COM INT BUS LO IN L	07	The other I/O RIC (if present) has been informed of a loss of dc bus voltage by the H7392 or H7390. If the receiving RIC does not have a power front end attached (Model 210) it uses this signal to assert XMI A (B) DC LO L, which is used to inform the XMI card cage of the loss of dc power.
		STATUS REGISTER E, 4380_{16}	
39:32			Not used.
		STATUS REGISTER F, 4400_{16}	
44:40	–	04:01	Not used, read as 1.
45	XMI B PRESENT L	05	A second XMI card cage is present in the I/O cabinet.
46	XMI A PRESENT L	06	The first XMI card cage is present in the I/O cabinet.
47	XMI B LAT AC LO L	07	This is the latched version of XMI B AC LO. If asserted it indicates that AC LO has been sent to the XMI BI backpanel. XMI B LAT AC LO L will be asserted if the I/O RIC has detected AC LO from the H7390 or H7392, or if the I/O RIC has reset BI expander register [04], DR PRM B AC LO L, or BI expander register [02], DR PRM B RESET L for an XMI reset sequence.

6.10.3.4.4 I/O RIC BI Expander Register and VAXBI Expander Cabinet Monitoring

Writing VAXBI expander register bits 0 and 1 control the monitoring of the VAXBI expander cabinet power signals. Bit 1 clock, and bit 0 load, enables loading and shifting of signals from a VAXBI cabinet shift register to the I/O RIC where they are direct inputs to a microprocessor port. The register outputs are fanned out to allow one I/O RIC to monitor two VAXBI expander cabinets. One RIC microprocessor port is used for each VAXBI expander cabinet. (See Figure 6-64.)

A new card has been designed to allow the VAX 9000 I/O RICs to monitor the VAXBI expander cabinet. The D-card for BIX monitoring, 54-17961-01, is mounted on the VAXBI expander cabinet MPS backpanel and provides an interface between the I/O RIC and the H9657-EA/H9657-EB VAXBI expander cabinet power components.

For any signal from the I/O RIC to the D-card for BIX monitoring, the I/O RIC provides +5 V to the optical isolator (see Figure 6-65). Conversely, for any signal that the D-card for BIX monitoring sends to the I/O RIC, +5 V is provided by the D-card (+5 CSP from the H7060 control/startup power module).

The RIC asserts LOAD BI DATA L to cause the BIX shift register (on each of two VAXBI expander cabinets) to be loaded on the next low to high CLOCK BI DATA H transition. This transition also provides the first bit of data. On each clock transition after load is deasserted, the shift register shifts one bit into the RIC microprocessor port.

BI EXPANDER REGISTER (WRITE ONLY)   I/O RIC, ADDRESS 4180

07	06	05	04	03	02	01	00
DR PRM A AC LO L	DR PRM A DC LO L	DR PRM A RESET L	DR PRM B AC LO L	DR PRM B DC LO L	DR PRM B RESET L	CLOCK BI DATA H	LOAD BI DATA L

BI EXPANDER REGISTER (READ ONLY)   I/O RIC

15	14	13	12	11	10	09	08
BI B CSP +5 V	BI B AC LO MOD H	BI B AFS 1 FAULT H	BI B EMM MOD J OK L	BI B BI 4 MOD OK L	BI B BI 3 MOD OK L	BI B BI 2 MOD OK L	BI B BI 1 MOD OK L

07	06	05	04	03	02	01	00
BI A CSP +5 V	BI A AC LO MOD H	BI A AFS 1 FAULT H	BI A EMM MOD J OK L	BI A BI 4 MOD OK L	BI A BI 3 MOD OK L	BI A BI 2 MOD OK L	BI A BI 1 MOD OK L

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Figure 6-64   I/O RIC BI Expander Register

The following VAXBI expander cabinet signals are monitored:

- The first bit shifted, CSP +5 V, is evaluated by the I/O RIC to determine if the VAXBI expander cabinet is present.

- AC LO MOD L — Asserted low when the dc bulk output drops below 200 Vdc ±4%.

- AFS 1 FAULT L — The VAXBI expander cabinet air flow sensor has detected a loss of air flow.

- EMM4 MOD J OK H — The H7176A power bulk box has asserted load enable low, which indicates that the ac/dc bulk conversion is operating correctly.

- BI 4 MOD OK H — The fourth H7189A regulator is providing output voltages within specifications.

- BI 3 MOD OK H — The third H7189A regulator is providing output voltages within specifications.

- BI 2 MOD OK H — The second H7189A regulator is providing output voltages within specifications.

- BI 1 MOD OK H — The first H7189A regulator is providing output voltages within specifications.

The I/O RIC firmware uses the bits shifted into the microprocessor port to generate the 2-byte read portion of the BI expander register. All bits are inverted except CSP +5 V. BI expander register [15:08] contain the monitored signals from BI expander cabinet B. BI expander register [07:00] contain the monitored signals from BI expander cabinet A.
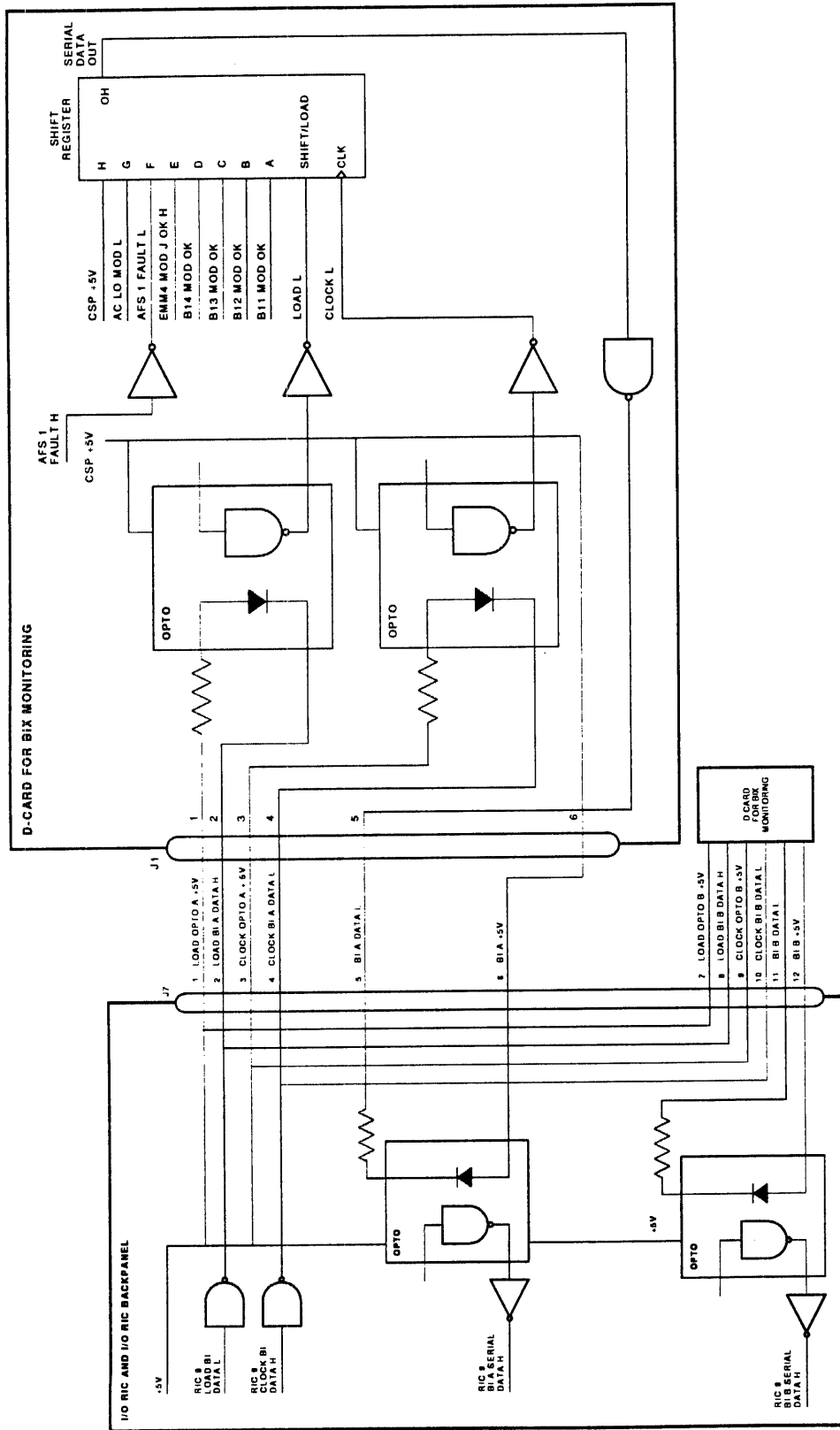
Figure 6-65   I/O RIC BI Expander Cabinet Interface

An XMI reset module controls the sequencing of AC LO, DC LO, and reset on the XMI bus during normal power up and power down. The VAX 9000 XMI bus does not have a reset module. The I/O RIC provides the reset module functionality using I/O RIC BI expander register [07:00].

When the I/O RIC enables or disables the H7214 and H7215 to provide XMI power by setting or resetting bits in the regulator enable register, it sequences the XMI AC LO, DC LO, and reset signals by setting and resetting bits in the BI expander register. If there is only one XMI bus present, the signals for XMI A will be asserted/deasserted. If there are two XMI buses present, then both the A and B signals will be asserted/deasserted. Timing for the signal assertion/deassertion is controlled by the I/O RIC EEPROM code, and conforms to XMI specifications. These register bits are ORed with the normal AC LO and DC LO signals the I/O RIC receives from the PFE or UPC. The signals are sent to the XMI card cage and the XMI bus.

- Sequence when the H7214/H7215s are enabled:

  1. Assert DR PRM A (B) RESET L

  2. Assert DR PRM A (B) DC LO L

  3. Assert DR PRM A (B) RESET L

  4. Assert DR PRM A (B) AC LO L

- Sequence when the H7214/H7215s are disabled:

  1. Assert DR PRM A (B) AC LO L

  2. Assert DR PRM A (B) DC LO L

6.10.3.4.5 I/O RIC Warm Start Register
The warm start register is not really a register, just the decode of a write to location (4200_{16}), used to set the warm start bit. Any data is meaningless. WARM START, power fail register[07] is set to indicate that any further restarts are to be warm starts.

6.10.3.4.6 I/O RIC INT RESET Register
The INT RESET register is not really a register, but the decode of a write to location (4380_{16}). The data is meaningless. The OFF ALERT INT flip-flop, the flip-flop that interrupts the CPU RIC when it receives COM OFF ALERT L from the PEM, is reset.

6.10.3.5 Other I/O RIC Status Signals
The following are other I/O RIC status signals:

- COM AC LO H is a copy of AC LO H from the UPC or H7390. It is an indication that the 280 Vdc bus has dropped below 195 Vdc. It is routed to the SIP for use in the BBU enable circuits. The SIP also forwards the information to the PEM.

- COM BUS LO H is a copy of BUS LO H from the H7392 or H7390, and an indication that the 280 Vdc bus has dropped below 180 Vdc. It is routed to the SIP for use in the powerfail circuits. The SIP informs the master clock and PEM of impending dc voltage loss.

6.10.3.6 I/O RIC LEDs

Each I/O RIC has six LEDs, which provide a visual indication of various RIC and converter functions (Figure 6–66).
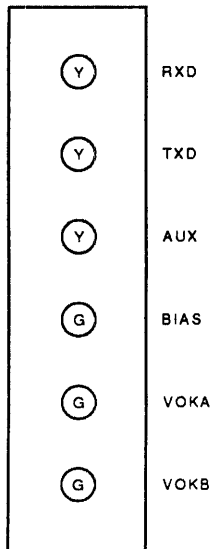
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Figure 6–66   I/O RIC Indicator LEDs

- **RXD** — The RXD indicator, a yellow LED, lights each time the data received from the RICBUS is asserted high.

- **TXD** — The TXD indicator, a yellow LED, lights each time the data to be transmitted on the RICBUS is asserted high.

- **AUX** — The AUX indicator, a yellow LED, has the following states:

  — **OFF** — This is the initial state of the RIC. If the RIC fails to power up, or if it fails its hard-core diagnostics, the LED remains off.

  — **Blinking at a 1 Hz rate** — The RIC passed self-tests, but has not communicated with the PEM.

  — **Blinking at a 10 Hz rate** — The RIC detected a general self-test fault, but has successfully communicated with the PEM. The RIC does not power up the converter bus.

  — **ON** — This is the normal operating state of the RIC, and indicates that the RIC has passed both hard-core and general self-tests, and has successfully communicated with the PEM.

  — **Blinking at a 2 Hz rate with different patterns** — For hard-core failures, the RIC will loop on the failed test. While it is looping, it will blink the AUX LED for 100 ms every 2 seconds. The number of blinks depends upon the failure.

    EPROM failure — one blink
    Internal RAM failure — two blinks
    External RAM failure — three blinks
    Address bus failure — four blinks

- **BIAS** — BIAS is a green LED that is lit if +5 Vdc (4.7 V minimum) and +15 Vdc (+13.2 Vdc minimum) is being supplied to the I/O RIC from the bias supply.

- **VOKA** — VOKA is a green LED that is lit if both CH OK A H (XMI H7215A) and CH # OK A H (XMI H7214A) are asserted (XMI A bus voltage OK).

- **VOKB** — VOKB is a green LED that is lit if both CH OK B H (XMI H7215B) and CH # OK B H (XMI H7214B) are asserted (XMI B bus voltage OK).

NOTE
If there is only one XMI installed, the CH OK B H and CH OK B H signals will float. This causes VOKB to light.

6.11   RICBUS

A RICBUS provides for communication between the PEM and RICs, and is a means of providing clock to the converters. Various power and control and status signals are routed between the power system components on the RICBUSes.

RICBUS communication is covered in Chapter 7, Power Control Subsystem and PCS Communication.

6.11.1   RICBUS Configuration

There is a maximum of three RICBUSes; RICBUS A, RICBUS B, and RICBUS C. Each RICBUS originates at the SIP, and is routed to each of the RICs it services. Model 400 systems may contain all three RICBUSes. RICBUS C is only present in a model 430 or 440 Model 210 systems have only RICBUS B. See Figure 6–67, Model 210 Power Control Subsystem Block Diagram, and Figure 6–68, Model 400 Systems Power Control Subsystem Block Diagram, for the RICBUS configurations.
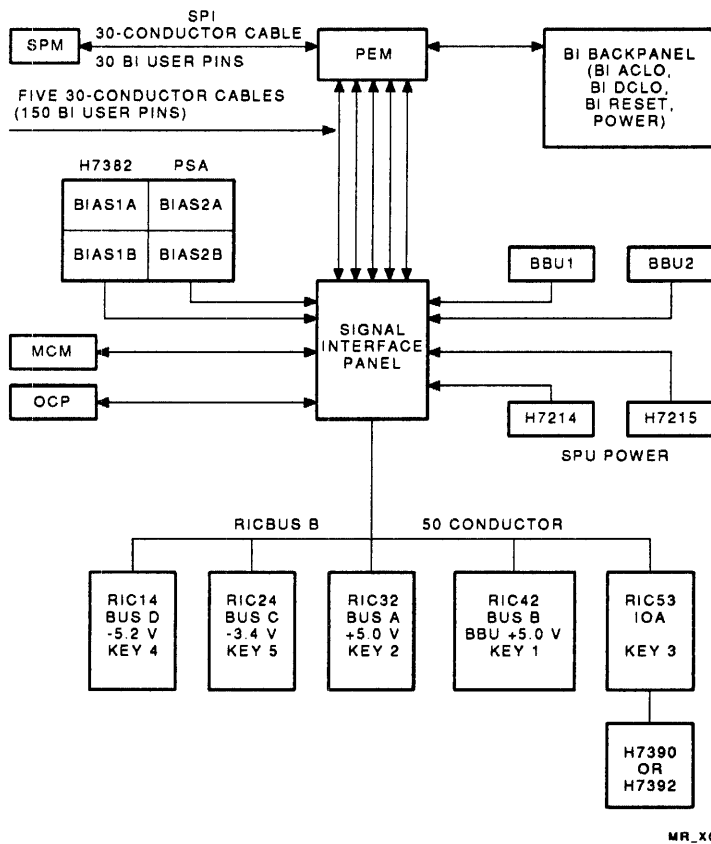
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Figure 6–67   Model 210 Power Control Subsystem Block Diagram
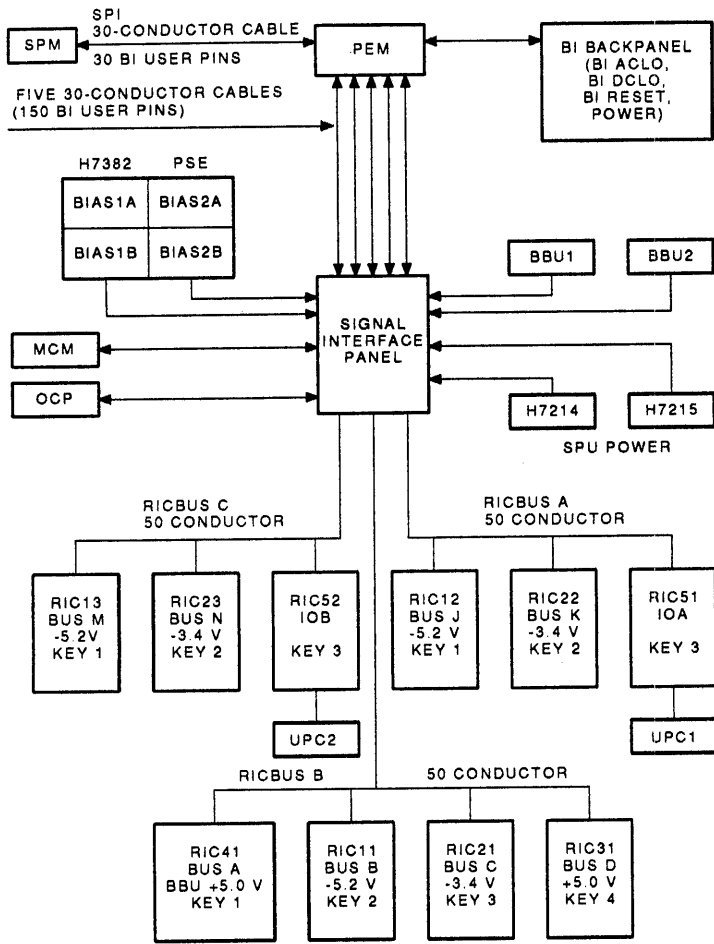
Figure 6-68   Model 400 Systems Power Control Subsystem Block Diagram

Table 6-37   RICBUS Configurations

RICBUS A	RICBUS B	RICBUS C
Model 210		
	RIC 14, bus D, -5.2 V	
	RIC 24, bus C, -3.4 V	
	RIC 32, bus A, +5.0 V	
	RIC 42, bus B, +5.0 V BBU	
	RIC 53, IOA	
Model 410 or 420		
RIC 12, bus J, -5.2 V	RIC 11, bus B, -5.2 V	
RIC 22, bus K, -3.4 V	RIC 21, bus C, -3.4 V	
RIC 51, IOA	RIC 31, bus D, +5.0 V	
	RIC 41, bus A, +5 V BBU	
Model 440		
RIC 12, bus J, -5.2 V	RIC 11, bus B, -5.2 V	RIC 13, bus M, -5.2 V
RIC 22, bus K, -3.4 V	RIC 21, bus C, -3.4 V	RIC 23, bus N, -3.4 V
RIC 51, IOA	RIC 31, bus D, +5.0 V	RIC 52, IOB
	RIC 41, bus A, +5 V BBU	

6.11.2 RICBUS Power

Each RICBUS is provided with +5 Vdc that is used by each RIC on the RICBUS to power
the signals that are common to all of the RICs on that RICBUS, the communication
data lines, keying signals, and clock drivers. This prevents a malfunctioning RIC from
rendering the RICBUS unusable. The PEM is still able to communicate with other RICs
on the RICBUS, and clocks are provided to the converters controlled by other RICs on the
same RICBUS.

RICBUS power is provided by the same bias supply that powers the SIP, PSE (H7382) for
model 400 systems, and PSA (H7382) for the model 210.

Power Control Subsystem and PCS Communication

This chapter details the power control subsystem (PCS) communication.

7.1 Power Control Subsystem Overview

The VAX 9000 power control subsystem (PCS) is a distributed intelligence system that controls the power system and monitors the system cabinet environment. It uses RICs, a maximum of ten in a model 440 and five in a model 210, that communicate with the PEM over up to three RICBUSs. The PEM is an intelligent message coordinator between the PCS and the service processor module (SPM). The PEM also has direct access to the BBU system, the power control bus, and the operator control panel (OCP).

Power control subsystem block diagrams are shown in Figure 6–67 and Figure 6–68. A tabulation of the RICs, by RICBUS, is provided in Table 6–37. The PEM communicates with the RICBUSs, BBUs, and OCP through the SIP. The model 440 may have up to three RICBUSs and the model 210 has one. Bias supply PSA (model 210) or PSE (model 400 systems) provides power for the SIP and RICBUSs. The PEM monitors the H7214 and H7215, which supply the SPU power and provide the master clock module with power loss information through the SIP.

The PEM is mounted in the SPU BI card cage and communicates with the SPU over the SPU-to-PEM interface (SPI), a 30 conductor cable using 30 BI user pins in the SPM and PEM slots.

The SPM and PEM communicate through the PEM's port interface, modeled after the BI VAX port architecture. They communicate through the port registers, a portion of the port interface. The communication link allows the SPM to command the PEM to power the system on or off, to run ROM-based diagnostics, to reload the EEPROM code, or to provide the SPM with environmental and power status or error information, or both. The PEM port interface may be in one of five states: uninitialized, initialized, enabled, download, or diagnostic.

7.2 PEM Port States

The PEM assumes the uninitialized state (Figure 7–1) upon power-up, when it is restarted, when the 8031 microprocessor generates a reset, or when commanded to the uninitialized state by the SPU. The SPU causes the PEM to change state by issuing port commands. These commands are generated when the SPU writes the PEM port control and status register (PEMCSR) (Figure 6–38).

The PEM state is available to the SPM through the port state field in DIAGREG (Figure 6–37). These bits drive the red port state LEDs on the PEM module. All three LEDs are lit when the PEM is in the uninitialized state.

POWER-UP   LOOP ON ERROR

UNINITIALIZED

EXECUTE HARD-CORE BISTs
FROM EPROM.

PORT STATE = 111

DIAGNOSTIC

INVOKE DIAGNOSTIC
FROM RBDIREG.

PORT STATE =011

INITIALIZED

ACCEPTS SPM COMMANDS VIA
PORT REGISTERS. PERFORMS
RIC KEEPALIVE POLLING. SPM
MAY EXAMINE VERSION NUMBER
OF RIC CODE AND DOWN-LINE
LOAD NEW VERSION TO RIC,
IF NECESSARY.

PORT STATE = 010

DOWNLOAD

DOWN-LINE LOAD TO
PEM's EEPROM.

PORT STATE =001

ENABLED

FULLY OPERATIONAL.

PORT STATE = 000

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Figure 7–1   PEM Port States

7.2.1 PEM Uninitialized State

Upon entering the uninitialized state, the PEM microprocessor sets the broke bit in the port DIAGREG, which turns off the yellow PEM broke LEDs. The PEM begins executing the EPROM code, starting with the hard-core tests. Before executing a hard-core test, the PEM places the test number in the diagnostic status field of the port DIAGREG, where it is available to the SPM. A hard-core test failure, other than EEPROM checksum, causes the PEM to loop indefinitely on the failing test, leaving the failing test number in the diagnostic status field.

If all the hard-core tests pass, before running the EEPROM checksum test, the broke bit is reset, lighting the PEM broke LEDs. The broke LEDs indicate that the PEM hard-core tests have completed satisfactorily.

The test number of the EEPROM checksum test is placed in the diagnostic status field. A failure is indicated by the test number only. In case of an EEPROM checksum failure, the PEM executes code in EPROM, waiting for the SPM to down-line load the EEPROM to correct the problem.

If the EEPROM checksum test passes, the diagnostic status field is cleared and the PEM waits for the SPM to command a port state change.

Ten seconds after the PEM enters the uninitialized mode, the BIST tests should be complete. If, after ten seconds, the SPM detects that the broke bit is still set, it recognizes that the PEM has failed one of the hard-core tests. The SPM checks the test number to determine which test failed. Even if the broke bit is reset, the SPM must check the diagnostic status field, as the EEPROM checksum test may have failed.

When all hard-core tests have completed satisfactorily, the PEM initializes the PEM software registers, determines the system configuration, and begins the RIC keep-alive process (determines which RICs are available, and if they are functioning correctly). The PEM also begins to monitor the OCP keyswitches, lighting the corresponding LEDs, and begins to monitor the bias OK and BBU available signals for state transitions.

After the hard-core tests and initialization is complete, the PEM waits for the SPM to issue a port command to change state to the initialized or download state. The PEM does not accept commands from the SPM received through the port transmit registers while in the uninitialized state.

For more information on PEM diagnostics and initialization, see Chapter 8, PEM and RIC Initialization and Diagnostics.

7.2.2 PEM Initialized State

When the PEM enters the initialized state (entered only from the uninitialized state), the port state LEDs are set to two (010_2). The PEM now accepts commands through the port transmit registers, and replies through the port receive registers. The PEM executes read, write, BIS, BIC, download, and sense commands from the SPM. The PEM is able to communicate with available RICs, and down-line load EEPROM code to the RICs (in response to commands from the SPM). To load the PEM EEPROM, the PEM has to be in the download state. In the initialized state, the PEM does not execute power-on, power-off, or margin commands. The PEM does not execute invokable ROM-based diagnostics, or accept exceptions from the RICs, or pass exceptions to the SPM.

From the initialized state, the PEM may be commanded to go to the enabled state, the diagnostic state (to execute invokable diagnostics, Chapter 8), or the download state.

7.2.3 PEM Enabled State

The enabled state is only reached from the initialized state. In this state, the PEM is fully operational. The port state LEDs are off. This state may be exited only by powerfail, runtime error, or a port command to enter the uninitialized state (which generates a reset). Table 7–1 describes the various tasks performed by the PEM in the enabled state.

Table 7–1   PEM Enabled State Tasks

Task	Description
SPM/PEM command management	The PEM processes commands sent by the SPM through the port transmit registers. Commands are issued by the SPM to retrieve PEM state information, or to instruct the PEM to perform an action, such as setting or resetting bits in PEM registers or memory space. Normally, these commands are responses to console terminal commands.
RIC command management	The PEM sends commands to the RICs to retrieve RIC state information, or instruct the RIC to perform specific actions. Normally, these commands are issued by the PEM when keep alive is performed, or in response to an SPM command issued by the operator at the console terminal.
RIC exception management	If the SPM has enabled exceptions (by writing the PEMCSR), the PEM passes RIC exceptions to the SPM. After successfully relaying the exception to the SPM, the PEM re-enables the RIC to send exception messages (when the RIC sends an exception message it disables exceptions).
PEM exception management	The PEM performs exception polling on the exception tasks that are enabled: RIC availability, BBU availability, BBU status, OCP keyswitch, and bias OKs. The PEM compares the current task state or status with the past task state or status. It sends the SPM an exception message for state or status changes. The PEM initiates (or terminates) an automatic shutdown (ASD) countdown if a RIC disappears from the RICBUS (or reappears on the RICBUS) (Section 8.1.1).
PEM timer management	The PEM updates its counters that provide timing functions for communication protocols, ASD management, timeout management, and other miscellaneous timing functions.
ASD pending management	The PEM tracks any pending ASD conditions. If an ASD times out, the PEM asserts the correct total off line. If conditions clear, the PEM cancels the pending ASD.
RIC keep-alive management	Every polling period, the PEM polls each possible RIC (present or not) and verifies that the present state matches the expected state. Items checked include BIST code, runtime error code, a bit indicating the RIC has converters enabled, ASD pending, and the RIC availability code.
	The polling interval is set by the POLLREG, and defaults to 500 ms. RICs on model 400 systems are polled every five seconds (10 RICs maximum * 500 ms). RICs on model 210 are polled every four seconds (8 RICs maximum * 500 ms).

Table 7–1 (Cont.) PEM Enabled State Tasks

Task	Description
SPM/PEM keep-alive management	The SPM sends the PEM a keep-alive packet every five seconds. The PEM loops the message back to the SPM. If the SPM never receives the loopback message it assumes the PEM is hung and issues a reset. If the PEM does not receive a keep-alive packet from the SPM in six seconds, it displays an SPM timeout code in the OCP diagnostic display LEDs (2L0).
	The exception occurs when the SPM sends a command to the PEM. The SPM does not send another message until it receives a reply to the current message but sends keep-alive packets.
	The PEM does not respond to a keep-alive packet while a command is active. The PEM clears the diagnostic status field in the port DIAGREG when it receives the command from the SPM, and increments this field every two seconds while the command is still active. The SPM verifies that the PEM is not hung by reading this field.

7.2.4 PEM Download State

The download state may be entered from the uninitialized or initialized state, and is used to down-line load code to the PEM's EEPROM. The code executes from EPROM. The PEM can only write the EEPROM, but it is able to read internal or external RAM registers, EPROM, or EEPROM. The PEM port state LEDs indicate a one (001_2).

7.2.5 PEM Diagnostic State

The diagnostic state is entered only from the initialized state, and exits only to the uninitialized state. The PEM port state LEDs indicate a three (011_2). The PEM executes invokable ROM-based diagnostics as directed by the ROM-based diagnostic invocation register (RBDIREG). See Section 8.1.2.

7.3 SPM/PEM Communication

SPM/PEM communication is carried out by the exchange of packets of information over the SPI (SPM-to-PEM interface) through the PEM port registers and transmit and receive FIFO buffers (Figure 7–2).
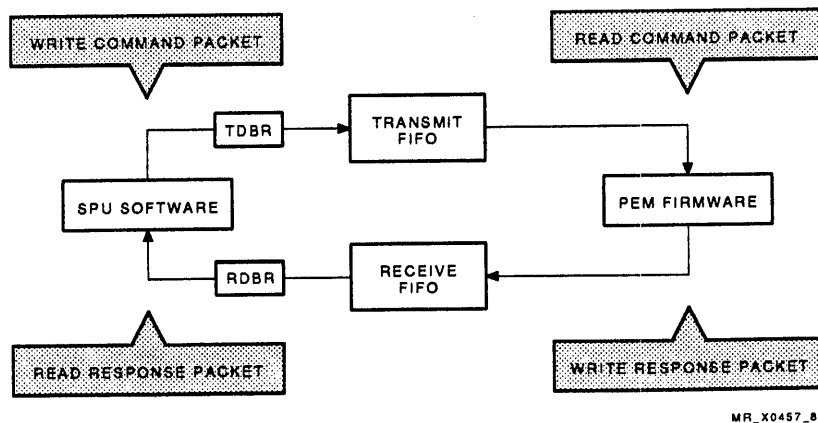
MR_X0457_89

Figure 7–2 SPM/PEM Data Link

Four of the eight PEM port registers, plus the transmit and receive FIFOs, are used for SPM/PEM communications. The registers are the receive control and status register (RCSR), receive data buffer register (RDBR), transmit control and status register (TCSR), and the transmit data buffer register (TDBR). The registers are used by the SPU software and PEM firmware to control the transfers and transfer data to and from the FIFOs. The port registers are covered in Section 6.9.11.

The SPM is the point of reference for SPM/PEM communications. The transmit registers control the transfer of packets to the PEM, while the receive registers control the transfer of packets to the SPM.

To send a command packet to the PEM, the SPU software writes the packet data, one byte at a time, into the TDBR. The PEM firmware reads the transmit FIFO, one byte at a time, to retrieve the data.

When the PEM firmware sends a response to the SPM, it writes the packet into the receive FIFO. The SPU reads the data from the RDBR.

7.3.1 SPM/PEM Command/Reply Protocol

All communication between the SPM and PEM is carried out by the transfer of data packets. Data packet structure is shown in Figure 7–3, and Table 7–2 provides a brief definition of data packet classes.

```
|◄────── HEADER ──────►|◄─ BODY ─►|◄── TERMINATOR ──►|
┌────────┬──────────┬──────────┬──────────────────┐
│        │          │          │                  │
│ CLASS  │ RESERVED │ DATAGRAM │ CHECKSUM (L, H)   │
│        │          │          │                  │
└────────┴──────────┴──────────┴──────────────────┘
  1 BYTE    1 BYTE    n BYTES       2 BYTES
```
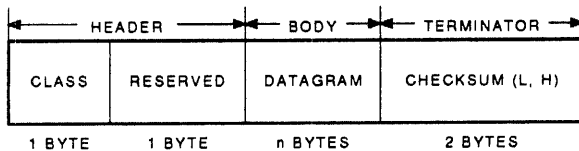
                                        MR_X0458_89

Figure 7–3   SPM/PEM Packet Structure

Table 7-2 SPM/PEM Packet Descriptions

Class	Type	Direction	Description
01	Command	To PEM	This allows the SPM to perform a data transfer to or from the PEM. Commands are always initiated by the SPM. Only one command is active at any one time. The SPM must wait for a response before initiating another command.
01	Reply	To SPM	This is the PEM's response to the command initiated by the SPM. The PEM returns the requested data to the SPM. The PEM is required to respond to the command within ten seconds or the command times out with the SPM retrying the command.
02	Exception	To SPM	If the PEM is in the enabled state, the transition of a state variable will cause the PEM to send an exception message to the SPM.
03	SPI test packet	To PEM	This is used to test the interface between the SPM and PEM. The SPM sends a test message with a maximum of 508 data bytes (the receive and transmit FIFO contain 512 bytes).
03	SPI test response	To SPM	The PEM loops back the test packet as the test response. This allows the SPM to verify correct message transmission. The PEM is allowed ten seconds to echo the test message.
04	Keep alive	To PEM	Every 10 seconds the SPM sends the PEM a keep-alive message.
04	Keep-alive response	To SPM	When the PEM is in the enabled state, within five seconds of receiving the keep-alive message from the SPM, the PEM echoes the message packet back to the SPM. If the PEM is executing a command, no keep-alive messages are accepted or returned. To maintain a keep-alive scheme, the diagnostic status field of the DIAGREG is used. This field is cleared on receipt of a message from the SPM. It is incremented every two seconds while the PEM is executing the command. The SPM reads this field to ensure the PEM is operational.

7.3.2 SPM/PEM Commands

When the SPM sends the PEM a command packet, the datagram portion of the packet contains the command information. The command format is shown in Figure 7-4, while the opcodes, modifiers, unit, and parameters are summarized in Table 7-3.

OPCODE	MODIFIER	UNIT	PARAMETER(S)
1 BYTE	1 BYTE	2 BYTES	n BYTES

MR_X0080_90
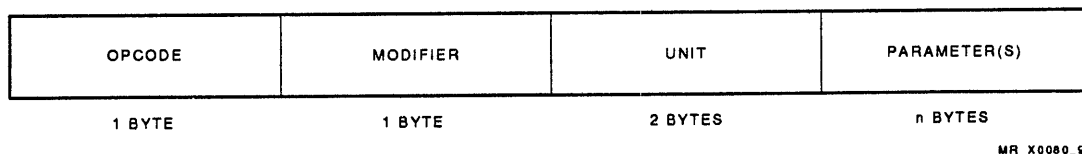
Figure 7-4 SPM/PEM Command Format

Table 7–3   SPM/PEM Opcode and Modifier, and Unit Field Descriptions

Opcode	Command	Mod.	Unit	Parameter(s)	Description
0	Read	0	RIC ID or zero for PEM	Two-byte address	Read RIC/PEM internal (8031 microprocessor) RAM.
		1		Two-byte address	Read RIC/PEM external RAM.
		2		Two-byte address	Read RIC/PEM program memory (EPROM or EEPROM).
		3		One-byte register number	Read RIC/PEM register.
1	Write	0	RIC ID or zero for PEM	Two-byte address and one byte of data	Write RIC/PEM internal (8031 microprocessor) RAM.
		1		Two-byte address and one byte of data	Write RIC/PEM external RAM.
		3		One-byte register number and one byte of data	Write RIC/PEM register.
2	BIS	0	RIC ID or zero for PEM	Two-byte address and one byte data mask	Set bits in RIC/PEM internal (8031 microprocessor) RAM where a bit is set in data mask.
		1		Two-byte address and one-byte data mask	Set bits in RIC/PEM external RAM where a bit is set in data mask.
		3		One-byte register number and one-byte data mask	Set bits in RIC/PEM register where a bit is set in data mask.
3	BIC	0	RIC ID or zero for PEM	Two-byte address and one byte data mask	Clear bits in RIC/PEM internal (8031 microprocessor) RAM where a bit is set in data mask.
		1		Two-byte address and one-byte data mask	Clear bits in RIC/PEM external RAM where a bit is set in data mask.
		3		One-byte register number and one-byte data mask	Clear bits in RIC/PEM register where a bit is set in data mask.
4	Download	0	RIC ID or zero for PEM	Up to 508 bytes (240 for the RIC) to be written to EEPROM	Download packet to either PEM or RIC EEPROM.
		1		Up to 508 bytes (240 for the RIC) to be written to EEPROM	Final download packet.
5	Margin[1]	0	Bus mask	One byte to indicate margin state[2]	Margin converter bus(es).

[1]For margin, poweron, or poweroff, the unit number consists of a bus mask that indicates which converter bus is to be turned on, off, or margined (Figure 7–5).

[2]00_{16} = Margin low, 01_{16} = Margin nominal, 02_{16} = Margin high.

Table 7-3 (Cont.) SPM/PEM Opcode and Modifier, and Unit Field Descriptions

Opcode	Command	Mod.	Unit	Parameter(s)	Description
6	Sense	0^3	NA	NA	Perform sense operation on the environment.
		1^4	Bus number	NA	Perform sense operation on power.
7	Poweron[1]	NA	Bus mask	NA	Turn on converter bus(es).
8	Poweroff[1]	NA	Bus mask	NA	Turn off converter bus(es).
9	Passthru	NA	RIC ID	NA	Send the command (up to 153 bytes) to the specified RIC.

[1]For margin, poweron, or poweroff, the unit number consists of a bus mask that indicates which converter bus is to be turned on, off, or margined (Figure 7-5).

[3]A sense environment command returns the entire environmental status.

[4]For a sense of a power bus, the unit field designates a bus number (Table 7-4).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IOB H7214B	IOB H7215B	IOB H7214A	IOB H7215A	IOA H7214B	IOA H7215B	IOA H7214A	IOA H7215A	BUS N	BUS M	BUS K OR BUS F	BUS J OR BUS E	BUS D	BUS C	BUS B	BUS A
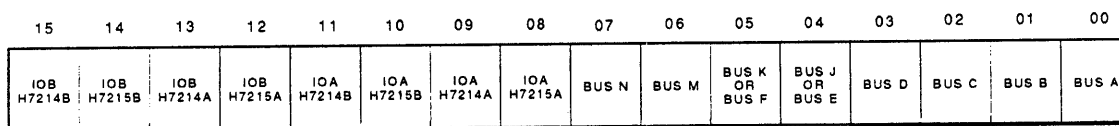
MR_X0076_90

Figure 7-5 SPM/PEM Command Bus Mask Field

Table 7-4 SPM/PEM Command Unit Field for Bus Number

Bus Number	Bus
0000	A
0001	B
0002	C
0003	D
0004	J or E
0005	K or F
0006	M
0007	N
0008	I/O
0009–FFFF	Not used

7.3.2.1 Poweron/Poweroff Commands

The poweron command may be executed only while the PEM is in the enabled state. It is used to turn power on to one or more buses without the SPU having to access specific RIC registers. The PEM first polls the RICs and saves the current state of each power bus. This is precautionary; if the command cannot be completed, the PEM returns the buses to their original state.

If the PEM cannot communicate with a RIC, or if a RIC has an ASD pending, the command is aborted.

The power buses are turned on sequentially, by cabinet, then by bus within the cabinet (Table 7–5). The -5.2 Vdc bus must be turned on before the -3.4 Vdc bus is turned on to prevent possible circuit damage (Section 6.8). Also, the -3.4 Vdc bus must be turned off before the -5.2 Vdc bus is turned off.

Table 7–5   Order of Poweron/Poweroff for Model 210

Poweron	Poweroff
1. SCU cabinet	1. IOA cabinet
Bus B	XMIA (H7214A, H7215A)
2. CPA cabinet	2. SCU cabinet
Bus D	Bus A
Bus C	3. CPA cabinet
3. SCU cabinet	Bus C
Bus A	Bus D
4. IOA cabinet	4. SCU cabinet
XMIA (H7214A, H7215A)	Bus B

7.3.3 SPM/PEM Reply Message Format

The PEM's reply to a command from the SPM is made up of one status byte and the reply data (Figure 7–6) generated in response to the SPU's command. The status byte indicates if the command was successful, and if not, the reason for failure. Data is returned only for read, sense, or passthru commands. For the passthru command, the data consists of the RIC command response. The status byte meanings are shown in Table 7–6.

STATUS	DATA
1 BYTE	n BYTES
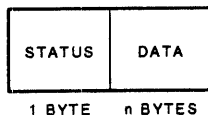
MR_X0077_90

Figure 7–6   SPM/PEM Command Reply Format

Table 7-6   SPU/PEM Reply Message Status Bytes

Status Code[1]	Message	Command
00	Operation successful	Any
01	Unknown opcode	Any
02	Bad PEM register	Any PEM register
03	Read from write only register	Any PEM register
04	Write to read only register	Any PEM register
05	Wrong number of data bytes	Any PEM
06	Illegal PEM memory address	Any PEM memory
07	Command data out of range	Any PEM
08	Command unit out of range	Any PEM
09	Command modifier out of range	Any PEM
0A	Cmd aborted - Bad bus combination	Poweron, poweroff
0B	RIC ACK timeout	Passthru or RIC
0C	Excessive XXNET collisions	Passthru or RIC
0D	XXNET command response timeout	Passthru or RIC
0E	Command/port_state mismatch	Any
0F	Bad PEM download	PEM download
10	Cmd aborted - RIC 11 not available	Margin, poweron, poweroff
11	Cmd aborted - RIC 12 not available	Margin, poweron, poweroff
12	Cmd aborted - RIC 13 not available	Margin, poweron, poweroff
13	Cmd aborted - RIC 21 not available	Margin, poweron, poweroff
14	Cmd aborted - RIC 22 not available	Margin, poweron, poweroff
15	Cmd aborted - RIC 23 not available	Margin, poweron, poweroff
16	Cmd aborted - RIC 31 not available	Margin, poweron, poweroff
17	Cmd aborted - RIC 41 not available	Margin, poweron, poweroff
18	Cmd aborted - RIC 51 not available	Poweron, poweroff
19	Cmd aborted - RIC 52 not available	Poweron, poweroff
1A	Cmd aborted - RIC 14 not available	Margin, poweron, poweroff
1B	Cmd aborted - RIC 15 not available	Margin, poweron, poweroff
1C	Cmd aborted - RIC 24 not available	Margin, poweron, poweroff
1D	Cmd aborted - RIC 25 not available	Margin, poweron, poweroff
1E	Cmd aborted - RIC 32 not available	Margin, poweron, poweroff
1F	Cmd aborted - RIC 42 not available	Margin, poweron, poweroff
20	Cmd aborted - RIC 53 not available	Poweron, poweroff
21	Cmd aborted - RIC 54 not available	Poweron, poweroff

[1]Status codes 01 through 7F are used for PEM return status codes. Status codes 81 through 90 are used for RIC return status codes.

Table 7–6 (Cont.)   SPU/PEM Reply Message Status Bytes

Status Code[1]	Message	Command
22	Cmd aborted - RIC 11 ASD pending	Poweron
23	Cmd aborted - RIC 12 ASD pending	Poweron
24	Cmd aborted - RIC 13 ASD pending	Poweron
25	Cmd aborted - RIC 21 ASD pending	Poweron
26	Cmd aborted - RIC 22 ASD pending	Poweron
27	Cmd aborted - RIC 23 ASD pending	Poweron
28	Cmd aborted - RIC 31 ASD pending	Poweron
29	Cmd aborted - RIC 41 ASD pending	Poweron
2A	Cmd aborted - RIC 51 ASD pending	Poweron
2B	Cmd aborted - RIC 52 ASD pending	Poweron
2C	Cmd aborted - RIC 14 ASD pending	Poweron
2D	Cmd aborted - RIC 15 ASD pending	Poweron
2E	Cmd aborted - RIC 24 ASD pending	Poweron
2F	Cmd aborted - RIC 25 ASD pending	Poweron
30	Cmd aborted - RIC 32 ASD pending	Poweron
31	Cmd aborted - RIC 42 ASD pending	Poweron
32	Cmd aborted - RIC 53 ASD pending	Poweron
33	Cmd aborted - RIC 54 ASD pending	Poweron
34	Cmd aborted - RIC 11 GRPLO BAD	Poweron
35	Cmd aborted - RIC 12 GRPLO BAD	Poweron
36	Cmd aborted - RIC 13 GRPLO BAD	Poweron
37	Cmd aborted - RIC 21 GRPLO BAD	Poweron
38	Cmd aborted - RIC 22 GRPLO BAD	Poweron
39	Cmd aborted - RIC 23 GRPLO BAD	Poweron
3A	Cmd aborted - RIC 31 GRPLO BAD	Poweron
3B	Cmd aborted - RIC 41 GRPLO BAD	Poweron
3C	Cmd aborted - RIC 51 MEDIC BAD	Poweron
3D	Cmd aborted - RIC 52 MEDIC BAD	Poweron
3E	Cmd aborted - RIC 14 GRPLO BAD	Poweron
3F	Cmd aborted - RIC 15 GRPLO BAD	Poweron
40	Cmd aborted - RIC 24 GRPLO BAD	Poweron
41	Cmd aborted - RIC 25 GRPLO BAD	Poweron
42	Cmd aborted - RIC 32 GRPLO BAD	Poweron
43	Cmd aborted - RIC 42 GRPLO BAD	Poweron

[1]Status codes 01 through 7F are used for PEM return status codes. Status codes 81 through 90 are used for RIC return status codes.

Table 7–6 (Cont.)   SPU/PEM Reply Message Status Bytes

Status Code[1]	Message	Command
44	Cmd aborted - RIC 53 MEDIC BAD	Poweron
45	Cmd aborted - RIC 54 MEDIC BAD	Poweron
46-7F	Reserved	
81	Undefined opcode	Any
82	Register number out of range	Any
83	Read error	Read
84	Write error	Write
85	Missing data in command	Any
86	Illegal modifier	Any
87	Improper command for EPROM	Measure, read, write, BIS, BIC
88	Improper EEPROM command	Download
89	Problem writing to the EEPROM	Download, write, BIS, BIC
8A	Cannot jump to EEPROM	BIS, write
8B	Timeout during AD conversion	Measure, read
8C	Illegal MUX channel select	Write, measure
8D	Illegal RIC state for download	Download
8E	Regulators may not be enabled	Write, BIS, BIC
8F	Not enough room left in the buffer	Any
90	BIS/BIC cannot be performed	BIS, BIC

[1]Status codes 01 through 7F are used for PEM return status codes. Status codes 81 through 90 are used for RIC return status codes.

7.4 PEM/RIC Communication

Five 30-pin cables connect the PEM to the SIP to allow SIP/OCP/PEM (SOP) bus communication. Each RICBUS originates at the SIP, the physical link providing communication between the PEM and RICs.

There are two communication modes, command mode and exception mode. The XXNET protocol is used, modified to reduce the number of collisions by fixing a RIC's backoff time to be proportional to the RIC ID number. An XXNET message does not exceed 256 bytes, the size of the RIC receive buffer.

7.4.1 XXNET Packet

The XXNET packet is shown in Figure 7–7 and the fields are described in Table 7–7.

SYN	CLASS	TO	FROM	FLAG	MESSAGE BYTES	CHKSM1	CHKSM2	EOT
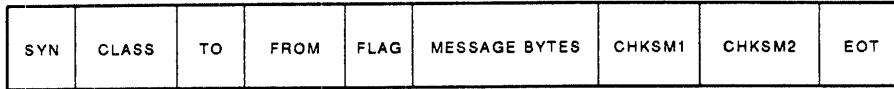
MR_X0078_90

Figure 7-7   XXNET Packet

Table 7-7   XXNET Packet Field Description

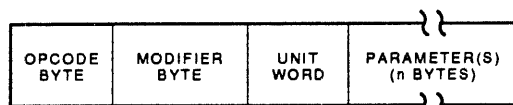| Field	Description
SYN	A synchronizing character (16_{16}) precedes all data messages and alerts the receiver that a message follows. The SYN character is discarded by the receiver, and is not included in the checksum.
CLASS	The class field indicates the class of message: SOH (01_{16}) for command mode and STX (02_{16}) for exception messages.
TO	The address of the device to receive the message. For the RICs, it is the RIC ID. It is zero for the PEM.
FROM	The address of the device that sent the message.
FLAG	The PEM uses the flag field to track commands to the various RICs. The flag field is incremented for each message the PEM sends to a RIC. The RIC stores the flag field, and places it in the flag field of the reply. The PEM then relates the reply to a certain command.
MESSAGE BYTES	The command mode or exception mode information bytes. The message may be up to 249 bytes in length, 256 minus the header length, seven. The SYN byte does not count.
CHKSM1	The 8 low-order bytes of the checksum.
CHKSM2	The 8 high-order bytes of the checksum.
EOT	The EOT character (04_{16}) signifies the end of the message.

7.4.2 Command Mode

To obtain status information from a RIC, or turn a converter on or off, the PEM sends a command mode message (the message bytes in the XXNET packet) to the RIC. The PEM allows the RIC up to 10 seconds to reply to the command. The commands from the PEM to the RIC described in (Table 7-8) are similar to the commands sent by the SPM to the PEM. The command format is shown in Figure 7-8. The unit field is not used in any RIC message.

OPCODE BYTE	MODIFIER BYTE	UNIT WORD	PARAMETER(S) (n BYTES)

MR_X0079_90

Figure 7-8   PEM/RIC Command Format

Table 7-8   PEM/RIC Command Format Description

Opcode	Command	Mod.	Parameter(s)	Description
0	Read	0	Two-byte address	Read RIC internal (8031 microprocessor) RAM.
		1	Two-byte address	Read RIC external RAM.
		2	Two-byte address	Read RIC program memory (EPROM or EEPROM).
		3	One-byte register number	Read RIC register.
1	Write	0	Two-byte address and one byte of data	Write RIC internal (8031 microprocessor) RAM.
		1	Two-byte address and one byte of data	Write RIC external RAM.
		3	One-byte register number and one byte of data	Write RIC register.
2	BIS	0	Two-byte address and one-byte data mask	Set bits in RIC internal (8031 microprocessor) RAM where a bit is set in a data mask.
		1	Two-byte address and one-byte data mask	Set bits in RIC external RAM where a bit is set in a data mask.
		3	One-byte register number and one-byte data mask	Set bits in RIC register where a bit is set in a data mask.
3	BIC	0	Two-byte address and one-byte data mask	Clear bits in RIC internal (8031 microprocessor) RAM where a bit is set in a data mask.
		1	Two-byte address and one-byte data mask	Clear bits in RIC external RAM where a bit is set in a data mask.
		3	One-byte register number and one-byte data mask	Clear bits in RIC register where a bit is set in a data mask.
4	Download	0	Starting address (low byte, high byte) and up to 240 bytes to be written to RIC EEPROM	Download packet to RIC EEPROM.

Table 7–8 (Cont.)   PEM/RIC Command Format Description

Opcode	Command	Mod.	Parameter(s)	Description
4	Download	1	Starting address (low byte, high byte) and up to 240 bytes to be written to RIC EEPROM	Final download packet to RIC EEPROM.
5	Measure	0 1[1]	One of 16 A/D converter channels to be measured. See Table 7–9.	The average of 64 A/D conversions is scaled and the result returned to the PEM. The RIC makes one measurement and returns the raw data result (without scaling) to the PEM.

[1]The measure command with modifier of one is used for testing only.

Table 7–9   RIC A/D Converter Input Selections

Channel	Measurement
00	Power voltage bus
01	Power bus reference voltage (VREF)
02	Ground current
03	Voltage reference adjust (REF_ADJ)
04	2.50 volt reference (2.50 VREF)
05	5.00 volt reference (5.00 VREF)
06	Converter 5 current
07	Ground
08	Thermistor 0 input
09	Thermistor 1 input
0A	Thermistor 2 input
0B	Thermistor 3 input
0C	Converter 0 current
0D	Converter 1 current
0E	Converter 2 current
0F	Converter 3 current

7.4.2.1 Command Mode Message Reply

When the RIC responds to a command from the PEM, it returns any necessary data, proceeded by a one-byte status field (Figure 7-9). The status field equals zero if there are no errors, or contains a numeric code between 81 and 90 for error conditions. The error codes are listed in Table 7-6. The length of the data field varies according to the length of the register for register reads but is one byte in length for memory addresses. The data returned for the measure command is discussed in Section 7.4.2.2.
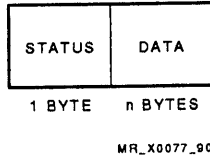
STATUS	DATA
1 BYTE	n BYTES

MR_X0077_90

Figure 7-9   PEM/RIC Reply Message Format

7.4.2.2 Measure Command Reply Data Representation

The data portion of the generic reply message format for the measure command is shown in Figure 7-10. As measurement results could be temperature, voltage, current, or the raw A/D converter output, the individual data format is discussed separately.

When the modifier byte for the measure command is one, the RIC makes one analog-to-digital conversion. The A/D converter output is not scaled, and the raw 12-bit measurement is returned to the PEM (Figure 7-11).

Voltage measurements are returned in the form of V = n. XYZ, where n is the hex voltage in volts, and XYZ is the hex equivalent in thousandths of volts.

MOST SIGNIFICANT RESULT DATA BYTE	LEAST SIGNIFICANT RESULT DATA BYTE

MR_X0081_90
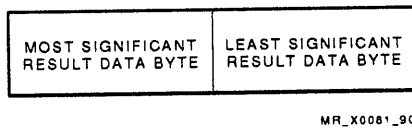
Figure 7-10   Generic PEM/RIC Reply Format for Measure Command

15	12	11	00
0 0 0 0		12 BIT A/D CONVERTER OUTPUT	

MR_X0082_90

Figure 7-11   RIC A/D Raw Result

15	14	10	09	00
SIGN BIT	VOLTAGE DATA WHOLE NUMBER (n)		VOLTAGE DATA FRACTION (XYZ)	

MR_X0083_90

Figure 7-12   RIC Voltage Data Representation

Temperatures are returned in the form T = n. XY, where n is the hex temperature in degrees centigrade and XY represents the hex equivalent in hundredths of degrees centigrade.
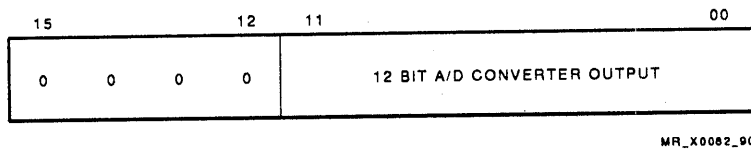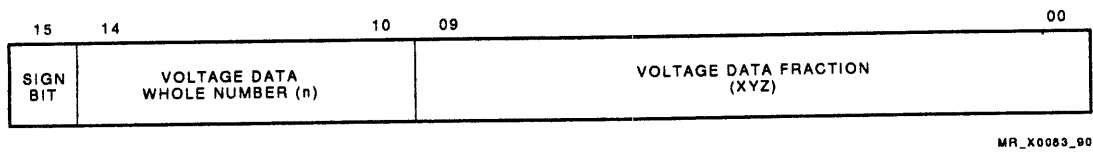
Ground current is measured only by the RIC controlling the -5.2 V buses. On all other RICs, the measurement is zero. The ground current is scaled by the hardware making the A/D converter reading a direct representation of the ground current in hexadecimal. The four upper bits are forced to zeros to provide a 16-bit representation of ground current.

Converter current is represented directly in hexadecimal with the unit of amperes.

15	14	08	07	00
SIGN BIT	DEGREES CENTIGRADE		HUNDREDTHS OF DEGREES CENTIGRADE	
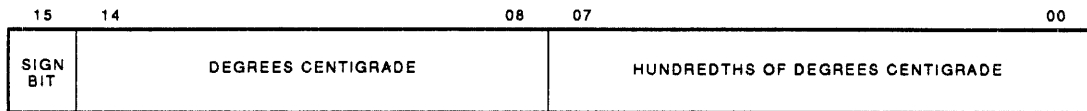
MR_X0084_90

Figure 7-13   RIC Temperature Data Representation

15	14	13	12	11	00
0	0	0	0	GROUND CURRENT IN mA	
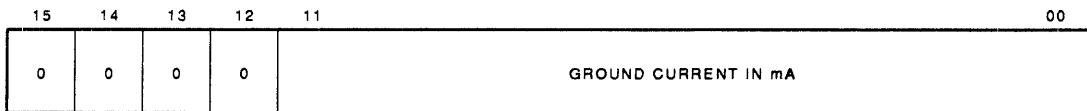
MR_X0085_90

Figure 7-14   RIC Ground Current Data Representation

15	14	13	12	11	00
0	0	0	0	CURRENT IN AMPERES	
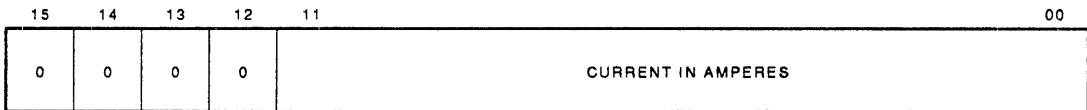
MR_X0086_90

Figure 7-15   RIC Converter Current Data Representation

7.5 Exceptions and Exception Messages

Both the PEM and the RIC send unsolicited messages to the SPM to inform the service processor of power system condition transitions, either to or from a warning condition, or to or from a potential shutdown condition. The PEM generates its own exception messages and passes RIC exception messages on to the SPM. The PEM monitors a fixed number of exception conditions, whereas the RIC uses an enabling register to control the conditions being monitored.

7.5.1 Enabling PEM and RIC Exceptions

If the PEM is in the enabled state, the service processor enables the PEM to send exception messages by setting the exception enable bit in the PEM control and status register (PEMCSR [06]). An individual exception condition is checked only if its enabling bit is set in the exception mask enable register, EMEREG, a 16-byte register. The first 10 bytes of the PEM EMEREG are shown in Figures 7-16 through 7-25. Bytes 10 through 15 are reserved for future use. See also Table 7-10.

Table 7-10 PEM Exception Message ID Bytes and EMEREG Bytes

Exception[1] ID Number	Severity	Model	Description
00	Warning, ASD[2]	400	RICBUS A availability (RICs 12, 22, and 51)
01	Warning, ASD[2]	400	RICBUS B availability (RICs 11, 21, 31, and 41)
02	Warning, ASD[2]	400	RICBUS C availability (RICs 13, 23, and 52)
03	Warning, ASD[2]	210	RICBUS B availability (RICs 14, 24, 32, and 42)
04	Warning, ASD[2]	210	RICBUS B availability (RIC 53)
05	–	–	Reserved
06	Warning	All	BBU availability
07	Warning	All	BBU status
08	Warning	All	OCP keyswitch
09	Warning	All	Bias OKs

[1]PEM exceptions are enabled by setting bits in the exception mask enable register, EMEREG. The EMEREG byte number is the same as the exception ID number.

[2]Automatic shutdown, ASD, if the RIC becomes unavailable. Warning for a RIC runtime error.
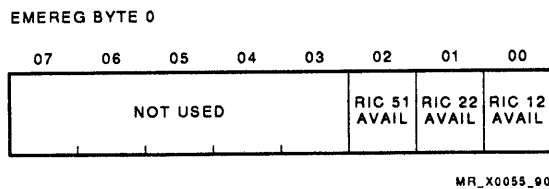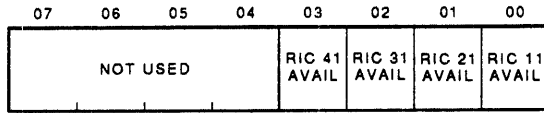
EMEREG BYTE 0

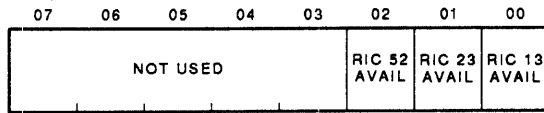| 07	06	05	04	03	02	01	00
		NOT USED			RIC 51 AVAIL	RIC 22 AVAIL	RIC 12 AVAIL

MR_X0055_90

Figure 7-16 EMEREG Byte 0 (Model 400 RICBUS A)

EMEREG BYTE 1

07	06	05	04	03	02	01	00
NOT USED				RIC 41 AVAIL	RIC 31 AVAIL	RIC 21 AVAIL	RIC 11 AVAIL

MR_X0056_90

Figure 7-17   EMEREG Byte 1 (Model 400 RICBUS B)

EMEREG BYTE 2

07	06	05	04	03	02	01	00
NOT USED					RIC 52 AVAIL	RIC 23 AVAIL	RIC 13 AVAIL

MR_X0057_90

Figure 7-18   EMEREG Byte 2 (Model 400 RICBUS C)

EMEREG BYTE 3

07	06	05	04	03	02	01	00
NOT USED				RIC 42 AVAIL	RIC 32 AVAIL	RIC 24 AVAIL	RIC 14 AVAIL
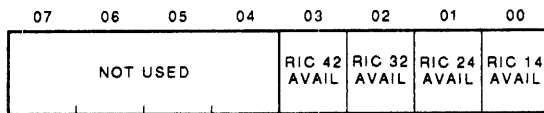
MR_X0058_90

Figure 7-19   EMEREG Byte 3 (Model 210 RICBUS B)

EMEREG BYTE 4

07	06	05	04	03	02	01	00
NOT USED							RIC 53 AVAIL
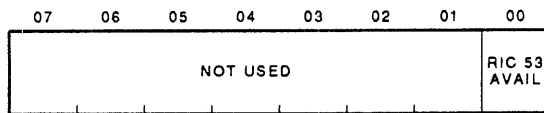
MR_X0059_90

Figure 7-20   EMEREG Byte 4 (Model 210 RICBUS B)

EMEREG BYTE 5

07	06	05	04	03	02	01	00
NOT USED							
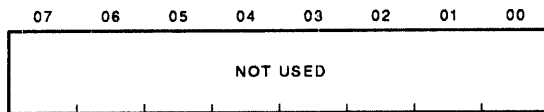
MR_X0060_90

Figure 7-21   EMEREG Byte 5 (Model 210 RICBUS A)

EMEREG BYTE 6

07	06	05	04	03	02	01	00
NOT USED						BBU 2 AVAIL	BBU 1 AVAIL

MR_X0061_90
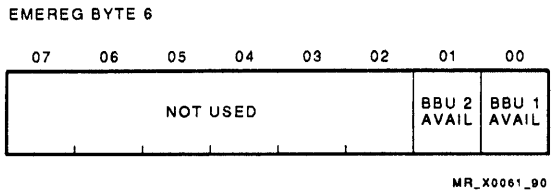
Figure 7-22   EMEREG Byte 6 (BBU Availability)

EMEREG BYTE 7

07	06	05	04	03	02	01	00
NOT USED							

BBU 2 STATUS
BBU 1 STATUS

MR_X0062_90
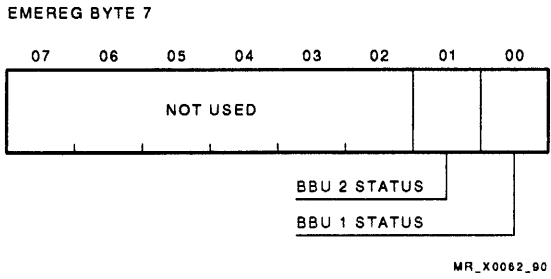
Figure 7-23   EMEREG Byte 7 (BBU Status)

EMEREG BYTE 8

07	06	05	04	03	02	01	00
NOT USED							

KEYSWITCH 2
KEYSWITCH 1

MR_X0063_90
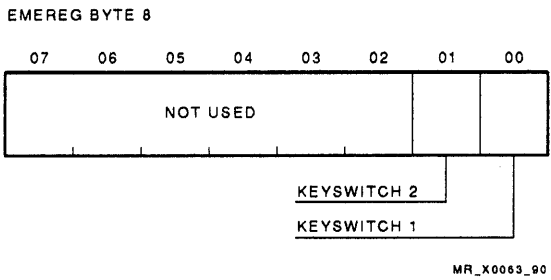
Figure 7-24   EMEREG Byte 8 (Keyswitch)

EMEREG BYTE 9

07	06	05	04	03	02	01	00
NOT USED		BIAS B1 OK	BIAS A1 OK	BIAS B2 OK	BIAS A2 OK	H7215 BIAS OK	H7214 BIAS OK

MR_X0064_90

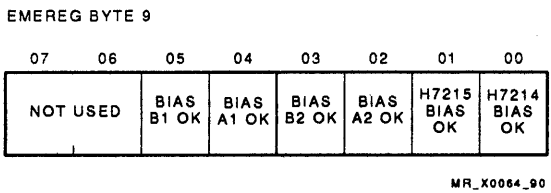**Figure 7-25   EMEREG Byte 9 (Bias OKs)**

In a RIC, each exception must be enabled individually by a set bit in a mask register, the exception mode enable register (EMEREG). This register is a 32-byte software register with 1 byte for each potential exception class. Each bit in a byte enables an individual exception task. The EMEREG is common to both the CPU and I/O RICs, but some bytes are specific to the CPU RIC, and some bytes are specific to the I/O RIC.

In addition to the the EMEREG register bits, the master exception mode enable bit in the software control and status register (SCSREG [00]) must be set to enable the RIC to send an exception message. Each RIC is programmed individually. Table 7-11 lists the various bytes of the exception mode enable register, the class of exception tasks, and indicates which type of RIC the exceptions are valid for.

The RIC monitors each of the tasks specified by a set bit in the EMEREG on a round-robin basis, reporting an exception when an abnormal condition is detected. Upon sending the exception message to the PEM, the RIC disables additional exception messages by clearing the master exception mode enable bit. The RIC continues to monitor all enabled exception tasks but cannot send further exception messages.

Table 7-11 RIC EMEREG

Byte Number	Exception Tasks	RIC Type
0	Bus voltage task	CPU
1	Bus status tasks	CPU
2	Converter MOD OKs	CPU
3	Bias OKs	CPU
4	Air temperature exception tasks	CPU
5	Reserved	–
6	Air flow exception tasks	CPU
7–11	Reserved	–
12	Thermal warning	I/O
13	Phase loss	I/O
14	Output current OK	I/O
15	Bus LO	I/O
16–18	Reserved	–
19	UPC attention	I/O
20	XMI MOD OKs	I/O
21	I/O cabinet air flow	I/O
22	Reserved	–
23	Phase rotation	I/O
24	Bias OKs	I/O
25	BI expander cabinet A	I/O
26	BI expander cabinet B	I/O
27–31	Reserved	–

When the PEM receives the exception message from the RIC, it forwards the message to the SPU, and then reenables the RIC to send exception messages (sets the RICs master exception mode enable bit). If, while the RIC exceptions are disabled, an exception task transitions from good to bad and back to good again (or vice versa), the exception would not be reported.

7.5.2 Exception Mode Messages

When the PEM or a RIC generates an exception message, it is sent from the PEM to the SPU in the datagram portion of the data packet. An exception message consists of a fixed length exception message header, which is different for the PEM and RICs, and a variable length exception message body. The exception message header for the PEM is 26 bytes long, while the exception message header for the RICs is 16 bytes long. The first five bytes of the RIC exception message header is the same as the PEM exception message header. The exception message body is dependent on the exception condition.

7.5.2.1 PEM Exception Message Header

The PEM exception message header is shown in Figure 7-26. The first byte (byte 0) is the origin byte. This byte contains the ID of the device that detected the state transition: the RIC number, or zero for the PEM. This byte, along with the exception ID byte, indicates to the SPU how it should interpret the exception message.
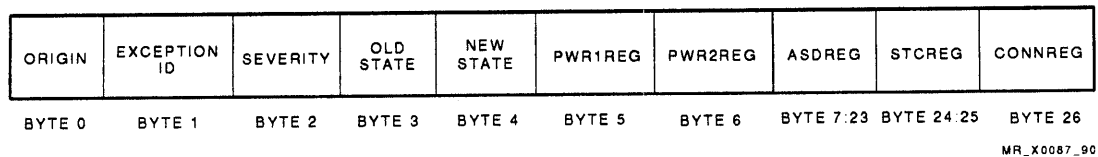
ORIGIN	EXCEPTION ID	SEVERITY	OLD STATE	NEW STATE	PWR1REG	PWR2REG	ASDREG	STCREG	CONNREG
BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7:23	BYTE 24:25	BYTE 26

MR_X0087_90

Figure 7-26   PEM Exception Message Header

The second byte is the exception ID byte. The PEM exception IDs are shown in Table 7-10, while the RIC exception IDs are shown in Table 7-12.

The third byte indicates the severity of the exception.

- 0 — Transition to the normal state
- 1 — Transition to the warning state
- 2 — Transition to the ASD state

The fourth byte contains the old state of the exception task, the state of the task the last time it was monitored. The fifth byte contains the new state of the exception task. This is the current state of the exception task. The remaining bytes contain the contents of the power 1 and power 2 registers, ASD register, system type and configuration register, and the connector register.

7.5.2.2 PEM Exception Message Body

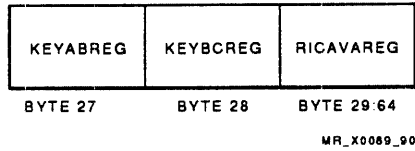The PEM-originated exception messages are specific for each exception (Figures 7–27 through 7–30).

KEYABREG	KEYBCREG	RICAVAREG
BYTE 27	BYTE 28	BYTE 29:64

MR_X0089_90

Figure 7–27   PEM Exception Message Body: RIC Availability Exception

BBUREG
BYTE 27

MR_X0090_90

Figure 7–28   PEM Exception Message Body: BBU Availability and BBU Status Exception

OCPSWREG	OCPDISREG
BYTE 27:28	BYTE 29:31

MR_X0091_90
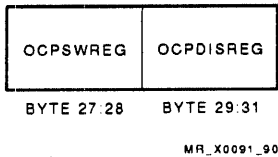
Figure 7–29   PEM Exception Message Body: Keyswitch Exception

BSCREG
BYTE 27

MR_X0092_90

Figure 7–30   PEM Exception Message Body: Bias OK Exception

7.5.2.3 RIC Exception Message Header

The RIC exception message header, beyond the first five bytes, contains the ASD register, hardware status register, powerfail register, software control and status register, and regulator configuration register (Figure 7–31). The hardware status register and powerfail register are multiple byte registers.
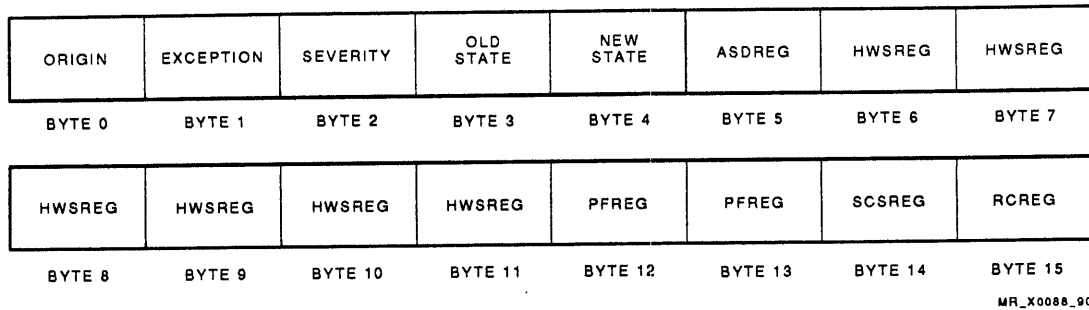
ORIGIN	EXCEPTION	SEVERITY	OLD STATE	NEW STATE	ASDREG	HWSREG	HWSREG
BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7

HWSREG	HWSREG	HWSREG	HWSREG	PFREG	PFREG	SCSREG	RCREG
BYTE 8	BYTE 9	BYTE 10	BYTE 11	BYTE 12	BYTE 13	BYTE 14	BYTE 15

MR_X0088_90

Figure 7–31   RIC Exception Message Header

Table 7–12   RIC Exception Message ID Bytes

Exception ID Number	Severity	RIC Type	Exception Description
00	Warning	CPU	Bus voltage exception
01	Warning	CPU	Bus status exception
02	Warning	CPU	Mod OK exception
03	Warning	CPU	BIAS OK exception
04	Warning, ASD[1]	CPU	Air temperature exception
05	–	–	Reserved
06	ASD	CPU	Air flow exception
07–0B	–	–	Reserved for CPU RIC
0C	Warning	I/O	Thermal warning
0D	Warning	I/O	Phase loss
0E	Warning	I/O	Output current
0F	Warning	I/O	BUS LO
10	–	–	Reserved
11	–	–	Reserved
12	–	–	Reserved
13	Warning	I/O	UPC attention
14	Warning	I/O	H7214/H7215 MOD OK
15	ASD	I/O	I/O cabinet air flow
16	–	–	Reserved
17	Warning	I/O	Phase rotation fault
18	Warning	I/O	BIAS OK exception
19	Warning	I/O	BI cabinet A
1A	Warning	I/O	BI cabinet B
1B–1F	–	–	Reserved

[1]A warning if in the yellow zone, otherwise, ASD.

7.5.2.4 RIC Exception Message Body

In most cases, the body of the CPU RIC exception messages contains many bytes in addition to the header. Due to the length of these messages, the body of the CPU RIC exception messages is shown in Table 7–13.

NOTE
Because the I/O RIC has no analog measurement circuitry, the I/O RIC exception message is limited to the header.

Table 7–13 CPU RIC Exception Message Body

Bytes	Exception Message Byte Contents
Air Flow Exceptions and Bias Exceptions	
0–15	Header
VBUS Exceptions, Bus Status Exceptions, and MOD OK Exceptions	
0–15	Header
16	Margin register (MGNREG)
17–18	Bus voltage measurement
19–20	Lower voltage limit[1]
21–22	Upper voltage limit[1]
23	Converter 0 current measurement
24	Converter 1 current measurement
25	Converter 2 current measurement
26	Converter 3 current measurement
27	Converter 4 current measurement
Air Temperature Exceptions	
0–15	Header
16–17	Temperature 1
18–19	Temperature 2
20–21	Thermistor 1 yellow zone[1]
22–23	Thermistor 1 red zone[1]
24–25	Thermistor 2 yellow zone[1]
26–27	Thermistor 2 red zone[1]
28–29	Thermistor open sensor limit[1]
30–31	Thermistor shorted sensor limit[1]

[1]Taken from the parameter limits register (PLREG).

8

PEM and RIC Initialization and Diagnostics

This chapter provides a description of the PEM and RIC diagnostics and initialization sequences. The PEM and RIC each have two categories of diagnostics. The PEM has hard-core (automatic) and invokable built-in self-tests (BISTs), while the RIC has hard-core and general built-in self-tests. The PEM invokable BISTs may be run on command from the SPU and include some of the hard-core tests. The RIC has no invokable tests.

The term BIST is synonymous with ROM-based diagnostic (RBD). All PEM and RIC diagnostics are located in the EPROM or EEPROM and, therefore, are RBDs and built-in self-tests.

The hard-core diagnostics test the integrity of the microprocessor, EPROM, EEPROM, and minimum kernel hardware necessary for the PEM or RIC to be considered operational. Additionally, in the PEM, the hard-core diagnostics test the hardware needed to allow the PEM to change state to the download state.

The PEM and RIC initialization and diagnostic sequences are described separately using flowcharts with corresponding callout lists. The function of each operation, or group of operations, is described.

Any register that is referenced in this chapter, but not present in this manual, may be found in the maintenance guide.

8.1 PEM Initialization Sequence and Diagnostics

The PEM initialization sequence and diagnostics is presented in two parts. The first section covers the initialization sequence and the hard-core diagnostics. Included is a description of the PEM main loop. The second section covers the invokable diagnostics.

8.1.1 PEM Initialization Sequence and Hard-Core Diagnostics

When power is turned on or if the SPU commands the PEM to go to the uninitialized state, a reset is generated and the microprocessor starts executing code at location zero in the EPROM. It executes the hard-core tests automatically, then if there are no problems, starts executing out of EEPROM. The hard-core (automatic) BISTs are listed in Table 8–1.

Table 8-1 PEM Hard-Core Tests

Test Number /DIAGREG Code[1]	Test Name	RTE Code[2]	Description
1	EPROM checksum	07	All locations in the EPROM, except locations containing revision data, are added together to generate the checksum.
2	IRAM	08	Tests the 8031 microprocessor internal RAM.
3	XRAM	09	Tests the PEM external RAM.
NA	Reset	NA	Certain register bits are checked to verify that they are in the expected state. The test cannot fail. The results are placed in the RBDSREG (Table 8-2).
4	BADBUS	0A	Tests the buffered address and data bus. Both the DIAGREG and OCPDREG (OCP data register on the PEM) are written and read back.
5	PIC	0B	Tests the 8031 microprocessor programmable interrupt controller.
6	EEPROM checksum	NA	All locations in the EEPROM, except locations containing revision data, are added together to generate the checksum.
7	RX FIFO	0C	Exercises the 512 location receive FIFO (data to the SPU).
8	TX FIFO	0D	Exercises the 512 location transmit FIFO (data from SPU).

[1]The test numbers do not indicate the order of execution, which is 1, 2, 3, reset test, 4, 5, 7, 8, and 6.

[2]Runtime error code written to RTEREG[07:00] for hard-core failures.

Table 8–2 shows the reset test result. A set bit indicates that a bit or bits for the named register are not in the expected state after a reset. A result of zero in the ROM-based diagnostic status register (RBDSREG) indicates that all pertinent registers contained the expected values.

Table 8–2 RBDSREG as Used for a Reset Test

Bit	Register
0	MISREG
1	DIAGREG
2	DIAGREG LOOPBACK
3	PEMCSR
4	PEMCSR LOOPBACK
5	TCSR
6	COMM XMIT
7	Not used
8	RCSR
9	COMM RCV
10	BIREG
11	ACPCSR
12	DCPCSR
13–55	Not used
56–63	0

The following steps are keyed to the PEM initialization and hard-core diagnostic flowchart (Figure 8–1.)
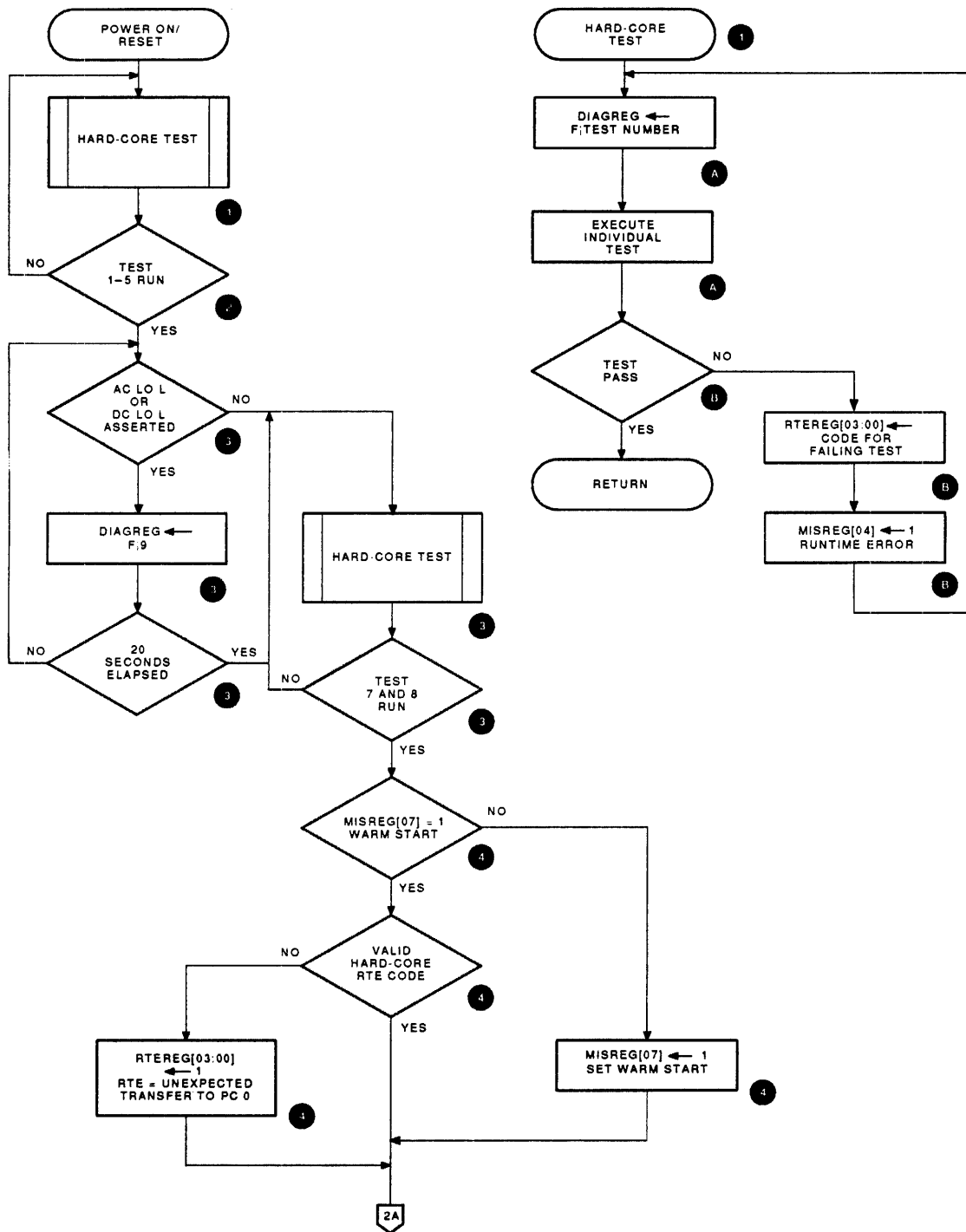
MR_X0051_90

Figure 8-1 (Cont.)   PEM Initialization and Hard-Core Diagnostics Flow Diagram
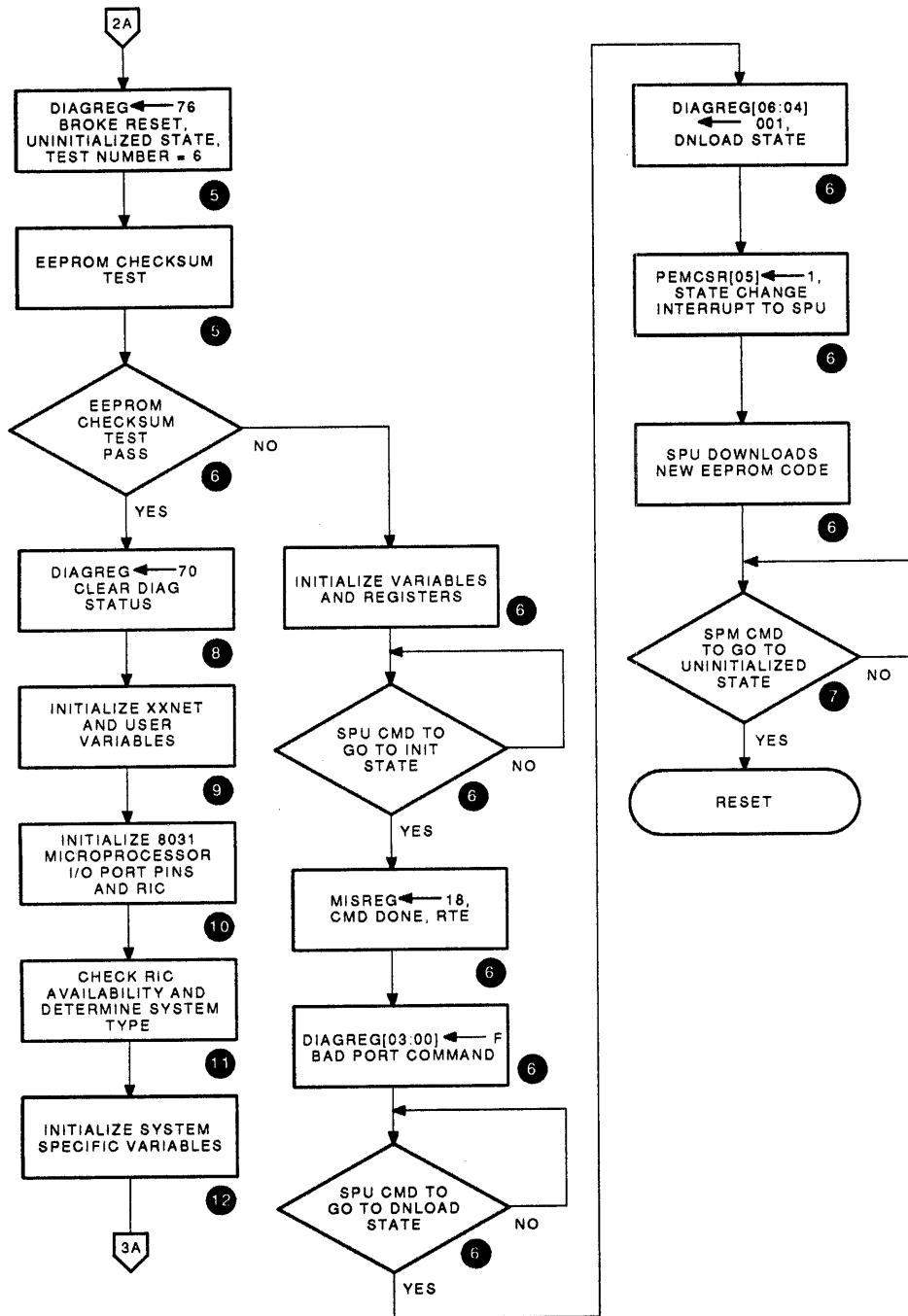
Figure 8-1 (Cont.)   PEM Initialization and Hard-Core Diagnostics Flow Diagram

MR_X0052_90
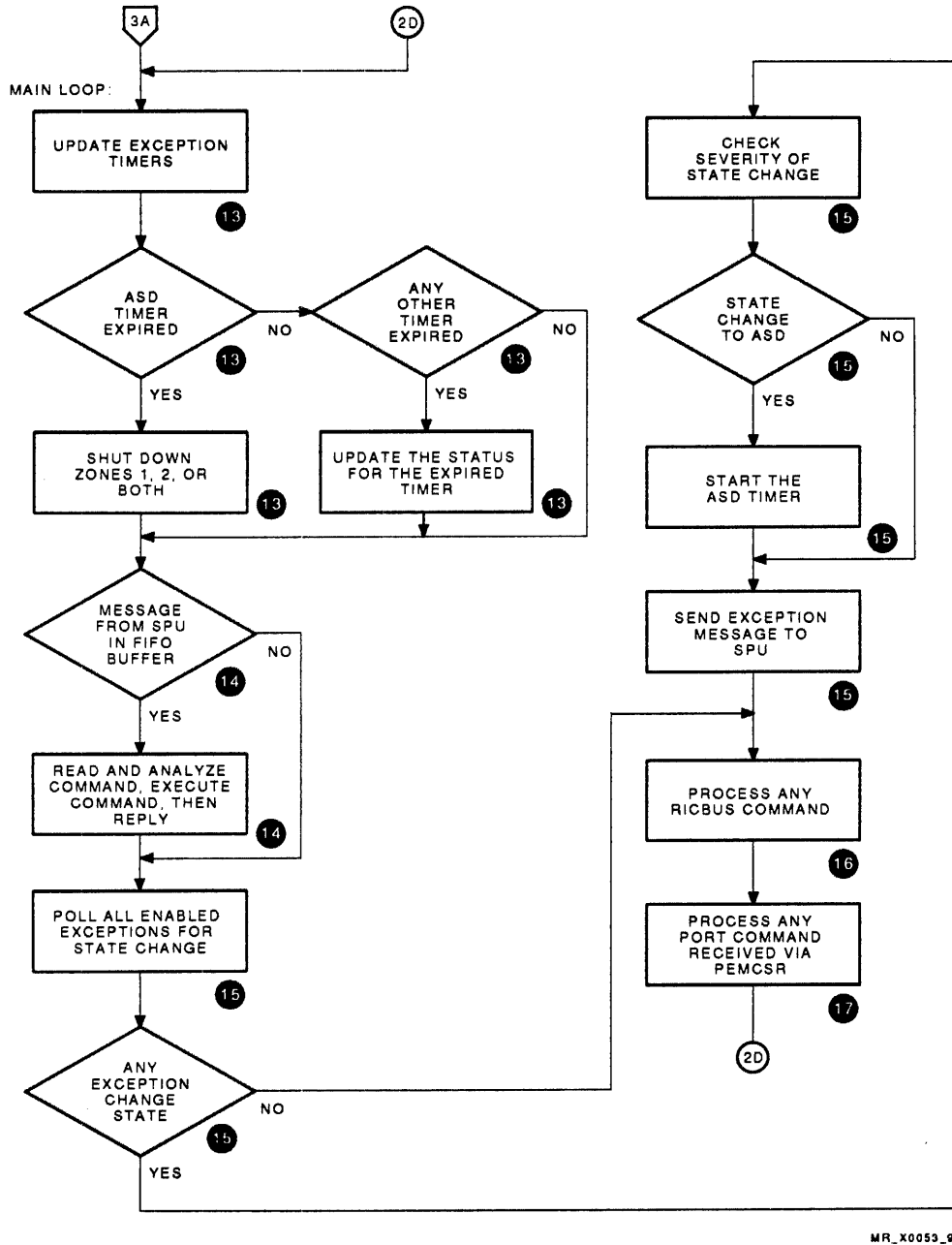
MR_X0053_90

Figure 8-1 PEM Initialization and Hard-Core Diagnostics Flow Diagram

❶ The next hard-core test in the sequence is executed.

    a. For tests 1 through 5, 7 and 8, before test execution, the PEM diagnostic register (DIAGREG, Figure 6-37) is loaded with F concatenated with the test number. Bit 7 (broke), being set, turns off the broke LED (yellow) to indicate that the PEM is not operational. Bits [06:04], port state equal to 111, indicate that the PEM is in the uninitialized state (Figure 7-1). Bits [03:00], diagnostic status, indicate the test number.

b. If any test fails, the test loops indefinitely. Before the next execution, runtime error register bits 3 through 0 (RTEREG[07:00]) are loaded with a code for the failing test (Table 8-1). Also, miscellaneous register bit 4 (MISREG [04]) is set to indicate a runtime error. (Those bits in MISREG involved with PEM initialization or diagnostics are shown in Figure 8-2. The remaining bits are not shown). This precautionary measure allows for the case when a test fails one or more times, then passes. When testing is complete, the DIAGREG no longer contains the test number of the failing test. The SPU, upon recognizing the runtime error in MISREG, reads the number of the last test that failed in the RTEREG.

MISREG

07	06	05	04	03	02	01	00
WARM START H			RTE H	CMD DON H			

MR_X0054_90
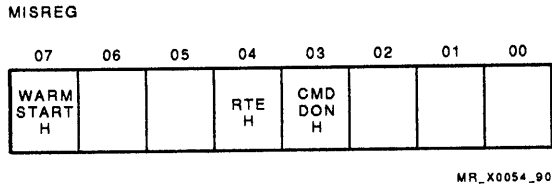
Figure 8-2   PEM MISREG (Partial)

The SPU is informed of a PEM hard-core failure through the following events. During a normal initialization sequence, the SPU reaches the point where it has to communicate with the PEM. The first thing the SPU does is to command the PEM to go to the initialized state. But, because the PEM failed a test and is looping on the failed test, it does not respond to commands from the SPU, nor does it set PEMCSR[05] (SCINT, state change interrupt, Figure 6-38), normally set by the PEM whenever it changes state. The SPU sets PEMCSR[04] (SC IEN, state change interrupt enable) to enable a state change interrupt. When the SPU does not receive a state change interrupt, it reads the DIAGREG to determine the PEM port state, status of the broke bit, and finds that a hard-core test is failing.

When in the uninitialized state, the diagnostic status bits of DIAGREG indicate which hard-core diagnostic is failing.

❷ Tests 1 through 5 are executed in the order 1, 2, 3, register reset test, 4, and 5. If the test passes, the next test in order is executed until each of these six hard-core tests have passed.

The register reset test is not actually a diagnostic. There are bits in some of the registers that are known to be in a certain state after a reset. These bits are monitored only. There is no test pass or fail.

RBDSREG bits are set to indicate that a particular register has unexpected bits set or reset. RBDSREG must be examined before the execution of any invokable diagnostic because, once an invokable diagnostic is run, RBDSREG contains the result of the invoked diagnostic. Table 8-2 shows the RBDSREG bit definition for the register reset test.

❸ If either AC LO or DC LO from the UPC or PFE is asserted, or H7214 OK or H7215 OK (SPU) is not asserted, the PEM waits before running hard-core tests 7 and 8. It loads the DIAGREG with F concatenated with 9_{16} and starts a 20 second timer. If, during the 20 second delay, the aforementioned power signals achieve the correct state, or the timer times out, the hard-core tests resume execution. If the timer times out without the signals in the correct state, it does not matter. The PEM continues executing; the SPM is necessarily in a hung state anyway.

The 20 second delay occurs because one of the signals used during the receive and transmit FIFO tests is a test powerfail signal. This blocks AC LO L and DC LO L. If AC LO L and DC LO L are slow to deassert, when the test powerfail signal is asserted for the hard-core test, the SPU recognizes this as the deassertion of AC LO L and boots. When the test is complete and the powerfail signal is deasserted, if AC LO L and DC LO L have not been deasserted, these signals are again asserted, disabling the SPU. With the true deassertion of AC LO L and DC LO L, the SPU reboots.

When the power signals are deasserted, or the 20 second timer has timed out, tests 7 and 8 are executed.

❹ When each of the seven tests have passed, a check is made for a warm start (MISREG[07] = 1). If it is not a warm start, the warm start bit is set.

If the warm start bit is already set, there has been an intermittent hard-core diagnostic failure or this part of the code has been executed at least one time. The latter case indicates that something has interrupted the normal operation of the PEM. The runtime error code (RTEREG[07:00]) is checked for validity (a hard-core test has failed). If it is not valid, it is set to 01, an indication that there has been an unexpected transfer to PC 0000.

❺ The hard-core tests have completed. Before the EEPROM checksum test is executed, the SPU loads the diagnostic register with 76. The broke bit ([07]) is cleared to light the broke LED, the state ([06:04]) is 7, uninitialized, and the test number ([03:00]) is 6. Each location in the EEPROM, except locations containing revision data, is summed to verify that the code is intact.

❻ An EEPROM checksum failure may be corrected by reloading the EEPROM code, a function of the SPU with the PEM in the download state. The SPU must first know that there has been an EEPROM checksum failure.

The PEM microprocessor, executing EPROM code, initializes variables and registers, and then waits for an SPU command to cause the PEM to change states to the initialized state. (SPU commands to cause the PEM to change state are directed to PEMCSR [03:00].) When the command to change state is received, the PEM loads the miscellaneous register with 18 to inform the SPU that the command is done, and that there is a runtime error. Also, an F is placed in DIAGREG [03:00], which indicates a bad port/state command. There is nothing wrong with the command, but a command to go to the initialized state with an EEPROM checksum failure is viewed as a bad command for the current state. This method is used as a means of notifying the SPU of the problem. The PEM now waits while the SPU reads the miscellaneous and diagnostic register to determine that a reload of EEPROM is necessary. The PEM is in the uninitialized state, the SPU has commanded the PEM to go to the initialized state, MISREG indicates a runtime error, and the DIAGREG diagnostic status bits equal F (EEPROM checksum error, which is preventing the state transition).

When the PEM receives a command from the SPU to go to the download state, it modifies the DIAGREG state bits to 001, and sets PEMCSR [05] to indicate a state change. The SPU reads DIAGREG [06:04] to determine that the PEM is in the download state and ready to accept messages to load the EEPROM with new code. The SPU then sends the PEM new EEPROM code through the transmit FIFO.

NOTE
The SPU obtains the PEM EEPROM code from file EWBPM_nn.BIN on the SPU load device, where nn is PEM code revision dependent.

❼ Once the EEPROM code has been loaded, the PEM waits for the SPU command to return to the uninitialized state. The transition to the uninitialized state generates a PEM reset, which starts the PEM executing at EPROM location 0. Once again, the PEM runs the hard-core diagnostics.

❽ If the checksum passes, the diagnostic register is loaded with 70. The broke bit remains reset to keep the broke LED lit. The state is still 7 (uninitialized), but bits 3 through 0 are cleared. The microprocessor begins executing EEPROM code, initializing PEM conditions.

❾ The XXNET variables and user variables are initialized. This includes setting up message buffers, clearing runtime error and communication flags. Once the XXNET variables are initialized, the PEM can communicate with the SPU. Later when it checks the message buffer for messages, it handles the SPU commands.

Also, timers for warning and ASD exceptions are initialized. Registers are cleared and initialized, and the exception table is initialized. Exception reporting is not enabled at this time.

The PEM is preparing for SPU commands to change state to the initialized, then the enabled state.

❿ The program interrupt controller and 8031 microprocessor port pins are initialized for correct interrupt handling and port I/O on the 8031 microprocessor.

⓫ The PEM polls each possible RIC in a VAX 9000 system, and initializes the RIC availability register (RICAVAREG) to indicate which RICs are available. The RICAVAREG contains two bytes for each possible RIC in a VAX 9000 system, a total of 36 bytes. A model 400 system contains a maximum of 10 RICs; a model 210 contains a maximum of 5 RICs.

Once the RICAVAREG has been initialized, its contents are used to initialize the system type and configuration register (STCREG). The STCREG indicates whether the system is a model 210 or 400, and the availability of a cabinet based on the presence of RICs in that cabinet. It indicates the availability of no RICs, some RICs, or all RICs on a cabinet-by-cabinet basis.

⓬ Other variables, flags, registers, and operating parameters specific to a system type are initialized. Of major importance is the exception mask enable register, EMEREG. This software register contains one byte for each specific PEM exception, with each bit in the byte enabling a particular exception task. The exceptions enabled by this register include RICBUS availability, BBU availability, BBU status, OCP keyswitch, and bias OK.

The first ten bytes of the EMEREG are shown in Figures 7-16 through 7-25. Some of the bytes are specific to model 400 systems, while others are specific to model 210 systems. The bytes not shown are reserved for future use.

This register enables the PEM to do only the exception polling. An exception message is not generated. The SPU enables the PEM to pass the exception to the SPU by setting the master exception mode enable bit, PEM control and status register (PEMCSR) bit 6. Also, the PEM cannot poll the enable bit or generate exception messages unless it is in the enabled state.

⓭ Each of the task timers (Table 8-3) is decremented by the amount of time that has elapsed since the timer was last counted down. If the ASD timer has expired, the PEM checks to see which RIC has lost communication with the PEM, causing the exception condition.

Table 8-3 PEM Exception and Task Timers

ID	Severity	Checked Every	Description
00	Warning, ASD	5 seconds	RICBUS A availability exception (model 400)
01	Warning, ASD	5 seconds	RICBUS B availability exception (model 400)
02	Warning, ASD	5 seconds	RICBUS C availability exception (model 400)
03	Warning, ASD	5 seconds	RICBUS B availability exception (model 210)
04	Warning, ASD	5 seconds	RICBUS B availability exception (model 210)
05	Warning, ASD	5 seconds	RICBUS A availability exception (model 210)
06	Warning	-[1]	BBU availability exception
07	Warning	40 ms	BBU status exception
08	Warning	50 ms	OCP keyswitch exception
09	Warning	-[1]	Bias OKs
NA	NA	2 seconds	Diagnostic timer
NA	NA	1 minute	BI BAD timer
NA	NA	5 seconds	Total off timer
NA	NA	250 ms	XXNET extension timer

[1]The BBU availability and bias OK exceptions are checked every time the exceptions are polled for a state change.

For a quad processor, if a RIC in the IOA or CPA cabinet (zone 1) caused the exception, zone 1 is shut down. If the RIC causing the condition is in the IOB or CPB cabinet, (zone 2) zone 2 is shut down. In either of these cases, because there are two H7392s, the remaining zone remains powered up. If, however, the RIC monitors memory, battery backup, or SCU power, the entire system is shut down.

The PEM continues to execute the EEPROM code. To shut down a zone, the PEM microprocessor sends a total off command to the SIP. When the appropriate SIP total off relay is energized to route the total off command to the power front end, the signal is routed back to the PEM, interrupting the PEM. The interrupt causes the PEM to exit the normal flow and handle the total off interrupt.

The PEM immediately writes a T and the contents of the total off register (TOFFREG) to the diagnostic display LEDs. This is a worst-case indication of what caused the problem. This code may be overwritten, and if that is the case, it happens so quickly that the T code is never seen. The TOFFREG is shown in Figure 8-3 and the bits are described in Table 8-4. The OCP diagnostic display LEDs hold T in the upper digit, TOFFREG [07:04] in the middle digit, and TOFFERG [03:00] in the low digit.
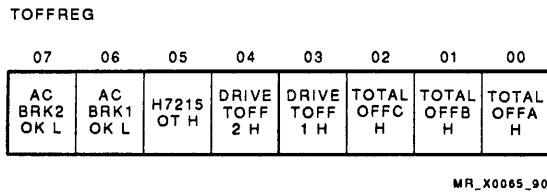
TOFFREG

07	06	05	04	03	02	01	00
AC BRK2 OK L	AC BRK1 OK L	H7215 OT H	DRIVE TOFF 2 H	DRIVE TOFF 1 H	TOTAL OFFC H	TOTAL OFFB H	TOTAL OFFA H

MR_X0065_90

Figure 8-3   PEM TOFFREG

Table 8-4   Total Off Register (TOFFREG) Bit Description

Bit	Signal	Description
0	TOTAL OFFA H	Total off generated by a RIC on RICBUS A
1	TOTAL OFFB H	Total off generated by a RIC on RICBUS B
2	TOTAL OFFC H	Total off generated by a RIC on RICBUS C
3	DRIVE TOFF 1 H	Master total off signal for UPC/PFE A
4	DRIVE TOFF 2 H	Master total off signal for UPC B
5	H7215 OT H	Overtemperature indicator for the SPU BI H7215
6	AC BRK1 OK L	AC breaker state for the UPC/PFE A
7	AC BRK2 OK L	AC breaker state for the UPC B

The PEM asserts COM TOTAL OFF, which forces each of the RICs to cease any RICBUS communication and interrupts their normal execution. Each RIC checks to determine if it is the cause of the total off. If so, the RIC sends a suicide message consisting of the RIC ID and an error code. These two bytes do not conform to XXNET protocol and are repeated three times.

While the PEM waits for the RICs to respond, it checks other possible total off conditions. First it checks if it is the PEM itself that initiated the total off due to an ASD exception (RIC not responding). If so, then the diagnostic display is written with a one or two concatenated with the ASD ID, and a zero (1 I ASD ID I 0 or 2 I ASD ID I 0). One (1) indicates an unknown configuration. Two (2) indicates a known configuration.

If the PEM did not initiate the total off, the PEM checks to see if the total off was caused by an H7215 (SPU) overtemperature condition. If so, the diagnostic display LEDs display 400.

The next check determines if the SPU initiated the total off in response to an operator command, in which case the diagnostic display LEDs contain 90L (both zones), 91L (zone 1), or 92L (zone 2).

If the total off was not caused by any of the preceding, the PEM waits for the response from the RIC detecting the error. The PEM needs two out of three of the messages to match to set up the diagnostic display for the error condition. The RIC ID and error code are used to look up the diagnostic display in a table. The entire list of OCP diagnostic display codes are shown in the Appendix B.

If there is not a match on two of the three suicide messages from the RIC, the diagnostic display indicates which RICBUS contained the offending RIC. The RIC availability bits in the PEM state register (PSREG) in the error log indicates which RIC caused the ASD exception.

The remaining exception and task timers (Table 8–3) are now covered:

a. Each time through the main loop, the PEM reads the SIP BBUREG to update the state of the BBU availability signals. They are checked when exceptions are monitored for change in state.

b. If the BBU status timer has expired, the PEM reads the SIP battery backup register (BBUREG) (Table 6–8) multiple times and records the present BBU status in the BBU status byte of the PEM state register (PSREG). There is only one bit per BBU in the SIP BBUREG, and it may be on, off, or cycling at 1 or 10 Hz. The PEM reads this register every 40 ms over a 2 second period to determine the BBU status, then it uses two bits to store the BBU state.

c. If the OCP keyswitch timer has expired, the PEM reads the OCP keyswitches and updates the keyswitch byte in the PSREG. If a switch has changed, the OCP LEDs corresponding to the switch are modified accordingly.

d. Each time through the main loop, the PEM reads the SIP bias register and verifies that the bias supplies that provide SIP power, SPU H7214/H7215 bias, and RICBUS power are operating correctly, and that the SPU H7214/H7215 are operating within specifications.

e. If the diagnostic register timer has expired, the PEM checks if an SPU command is being executed. If the PEM is executing an SPU command, no normal keep-alive message exchange can take place between the SPU and PEM (SPU cannot have more than one message active at one time). Therefore, the PEM increments the diagnostic status field of the diagnostic register (port register DIAGREG). The SPU monitors these bits during the time the command is active to ensure that they are incremented and the PEM has not hung.

f. If the SPU asserts BI BAD L (any module on the SPU BI backpanel has a bad BIIC) for 60 seconds, the PEM writes a 200 to the OCP diagnostic display LEDs.

g. The total off timer is a reciprocal lock-out timer with the AC LO interrupt. If either of these conditions interrupt the PEM, the associated timer is started. The timer prevents an interrupt from the other condition for five seconds.

For instance, a total off condition trips the power front end CB1, which causes an AC LO condition and an AC LO interrupt. The lock-out timer prevents the PEM from trying to handle the AC LO interrupt while still handling the total off interrupt.

h. The XXNET timer is not checked on a regular basis but is started each time the PEM sends a message to a RIC. The PEM allows the RIC 250 ms to respond to the message.

⑭ The PEM checks the FIFO buffer for messages from the SPU. If a message is present, the PEM analyzes the command to determine if it is for the PEM or a RIC. If the command is meant for a RIC, the PEM sends the command to the RICs at a later time. All RICs receive the message; it is up to the RIC whose ID matches the TO field in the message to respond to the message. If the command is for the PEM, it executes the command, then sends the SPU the reply (which includes data for a read).

⑮ Each exception condition is checked for a change in state. If the current state is different from the previous state, the exception is further checked to determine the severity of the exception condition. The exception condition may have transitioned to the ASD state, warning state, or back to the normal state. For a transition to the ASD state, the ASD timer is enabled.

An exception message, based on the severity of the state change, is constructed and sent to the service processor.

⑯ If there are any messages to or from a RIC, the PEM processes them at this time. SPU messages to the RICs are forwarded to the RICs, or RIC responses to SPU commands are forwarded to the SPU.

⑰ The PEM monitors the PEM control and status register port command bits (PEMCSR [03:00]) for a valid port command. The PEM changes state, clears the runtime error bit, or clears the diagnostic status field as a result of these commands (Figure 6-38).

Items 13 through 17 make up the PEM code main loop. This loop is executed indefinitely as long as the PEM remains in the enabled state. A change of state to uninitialized state (the only state the PEM can go to from the enabled state) causes a PEM reset, which restarts the hard-core diagnostics. Also, a total off interrupt or AC LO interrupt causes the PEM to exit the main loop code.

8.1.2 PEM Invokable Diagnostics

Each individual invokable test can be initiated by the console terminal operator (through the SPM) by writing the appropriate information into the ROM-based diagnostic invocation register (RBDIREG). Information pertaining to the success or failure of the test can be read from the ROM-based diagnostic status register (RBDSREG). A restriction, however, governs the acceptance of commands to run invokable tests: They are honored only when PEM is in the diagnostic state. The PEM can get only to the diagnostic state from the initialized state, and can go only to the uninitialized state from the diagnostic state (Figure 7-1).

The PEM invokable RBDs are classified by diagnostics numbers (Dn, where n = 8 to F), and up to 24 subtests, which are dispatched using a 24-bit mask. RBDIREG byte 0 designates which diagnostic is to be run, while bytes 1 through 3 designate which subtest within the diagnostic (Figure 8-4). A single diagnostic is made up of two or more subtests. Either all or a subset of the subtests with a single diagnostic can be executed with a single command. The diagnostic numbers and subtests (mask bits) are shown in Table 8-5.

8.1.2.1 RBDIREG and RBDSREG
Two software-defined registers allow the service processor to select the specific diagnostic and subtests to be executed and retrieve the results of the test.

The RBD invocation register (RBDIREG) is a 4-byte read/write register that, when written with an RBD diagnostic number and optional test mask, causes the PEM to execute that particular diagnostic subtest. Figure 8-4 shows the format of this register.

RBDIREG

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

SUBTEST MASK BIT [23:08]

BYTE 3   BYTE 2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

SUBTEST MASK BIT [07:00]   DIAGNOSTIC NUMBER

BYTE 1   BYTE 0

MR_X0066_90
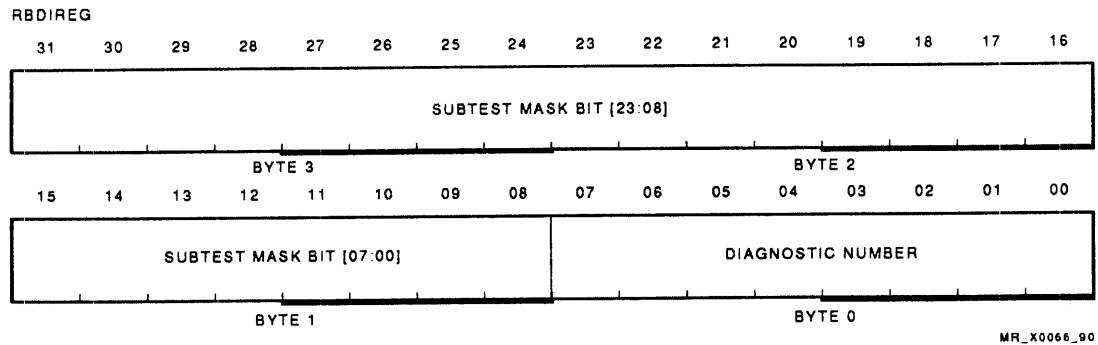
Figure 8–4   RBDIREG Format

To comply with the port protocol, which requires the PEM to send a return message on receipt of an SPM message, the PEM sends a reply message that indicates receipt of the command message. Therefore, a successful return message is not viewed as an indication of a successful self-test, only as an indication of the receipt of a command.

Byte 0 dispatches a specific diagnostic, while the three other bytes act as a mask depicting which of the 24 tests within that diagnostic are to be executed. Any 1, or all, of the 24 tests within the desired diagnostic may be executed by:

- **Diagnostic number** — This byte is written with the number of the RBD diagnostic to be executed. It selects the main test category and specifies the interpretation of the subtest mask in bytes 1 through 3.

- **Subtest mask** — The individual bits of these three bytes act as a mask to enable executing one or all subtests of a diagnostic.

Table 8–5   PEM Invokable Diagnostics

Diagnostic Number	Subtest Number Mask Bit	Subtest Definition
8	0	BI reset test 1
	1	BI reset test 2
	2	162.5 kHz clock test
	3	32.5 kHz clock test
	4	EEPROM checksum test
	5	Test powerfail/total off
	6–23	Not used
9	0	Total off test
	1	ACLO 1 test
	2	ACLO 2 test
	3	BUS LO 1 test
	4	BUS LO 2 test
	5	BBU test

Table 8–5 (Cont.)   PEM Invokable Diagnostics

Diagnostic Number	Subtest Number Mask Bit	Subtest Definition
	6	State change interrupt test
	7–23	Not used
A	0	RCV FIFO/RCSR test
	1	XMIT FIFO/TCSR test
	2–23	Not used
B	0	Transmit enable test
	1	RIC 11 available test
	2	RIC 12 available test
	3	RIC 13 available test
	4	RIC 21 available test
	5	RIC 22 available test
	6	RIC 23 available test
	7	RIC 31 available test
	8	RIC 41 available test
	9	RIC 51 available test
	10	RIC 52 available test
	11	RIC 14 available test
	12	RIC 15 available test
	13	RIC 24 available test
	14	RIC 25 available test
	15	RIC 32 available test
	16	RIC 42 available test
	17	RIC 53 available test
	18	RIC 54 available test
	19–23	Not used
C	0	OCP LED test
	1	OCP display test
	2–23	Not used
D	0	GRP A LO test
	1	GRP B LO test
	2	GRP C LO test
	3	GRP BBU LO test
	4–23	Not used
E	0	DIAGREG test
	1	PEMCSR test

Table 8–5 (Cont.)   PEM Invokable Diagnostics

Diagnostic Number	Subtest Number Mask Bit	Subtest Definition
	2	ACPCSR test
	3	DCPCSR test
	4–23	Not used
F	0	H7215 OK test
	1	H7214 OK test
	2–23	Not used

The RBD status register (RBDSREG) holds the completion result status of the RBDs. This register is updated on completion of the diagnostic tests, invoked through the SPU writing the RBDIREG. The register contains eight bytes. Byte 7 contains the diagnostic number. The remaining bits have a separate definition for each of the invokable diagnostic tests. The RBDSREG, for invokable diagnostics, is shown in Table 8–6.

Table 8–6   RBDSREG for Invokable Diagnostics

Diagnostic Number	Bit Number	Subtest Number	Error
8	0	0	Too long between BI RESET and BI ACLO - BI reset 1
	1	0	Too short between BI ACLO and BI DCLO - BI reset 1
	2	0	Too long between BI ACLO and BI DCLO - BI reset 1
	3	0	Too short BI DCLO - BI reset 1
	4	0	Too long BI DCLO - BI reset 1
	5	0	Too short between BI DCLO and BI ACLO - BI reset 1
	6	0	Too long between BI DCLO and BI ACLO - BI reset 1
	7	0	Too short between BI DCLO and BI RESET - BI reset 1
	8	1	Too long between BI RESET and BI ACLO - BI reset 2
	9	1	Too short between BI ACLO and BI DCLO - BI reset 2
	10	1	Too long between BI ACLO and BI DCLO - BI reset 2
	11	1	Too short BI DCLO - BI reset 2
	12	1	Too long BI DCLO - BI reset 2
	13	1	Too short between BI DCLO and BI ACLO - BI reset 2
	14	1	Too long between BI DCLO and BI ACLO - BI reset 2
	15	1	Too short between BI DCLO and BI RESET - BI reset 2
	16	2	162.5 kHz slow
	17	2	162.5 kHz fast
	18	3	32.5 kHz slow
	19	3	32.5 kHz fast

Table 8–6 (Cont.) RBDSREG for Invokable Diagnostics

Diagnostic Number	Bit Number	Subtest Number	Error
	20	4	EEPROM checksum fail
	21	5	Powerfail line stuck
	22	5	Total off line stuck
	23–55	–	Not used
	56–63	–	Contents = 8 (test number)
9	0	0	TOFFA stuck
	1	0	TOFFB stuck
	2	0	TOFFC stuck
	3	0	DRIVE TOFF1 stuck
	4	0	DRIVE TOFF2 stuck
	5	0	H7215 OT stuck
	6	–	Not used
	7	–	Not used
	8	0	PEM TOFF1 stuck (PTOFF in P1REG)
	9	0	PEM TOFF2 stuck (PTOFF in P1REG)
	10	0	PEM DRIVE TOFF1 interrupt fault
	11	0	PEM DRIVE TOFF2 interrupt fault
	12	–	Not used
	13	–	Not used
	14	–	Not used
	15	–	Not used
	16	1	ACLO 1 stuck in ACPCSR
	17	1	ACLO 1 stuck in PWR2REG
	18	1	LAT ACLO 1 stuck in ACPCSR
	19	1	LAT ACLO 1 stuck in PWR2REG
	20	1	ACLO 1 IEN stuck in ACPCSR
	21	1	ACLO 1 INT stuck in BIREG
	22	1	ACLO 1 interrupt fault
	23	–	Not used
	24	2	ACLO 2 stuck in ACPCSR
	25	2	ACLO 2 stuck in PWR2REG
	26	2	LAT ACLO 2 stuck in ACPCSR
	27	2	LAT ACLO 2 stuck in PWR2REG
	28	2	ACLO 2 IEN stuck in ACPCSR
	29	2	ACLO 2 INT stuck in BIREG

Table 8-6 (Cont.) RBDSREG for Invokable Diagnostics

Diagnostic Number	Bit Number	Subtest Number	Error
	30	2	ACLO 2 interrupt fault
	31	–	Not used
	32	3	DCLO 1 stuck in DCPCSR
	33	3	DCLO 1 stuck in PWR2REG
	34	3	LAT DCLO 1 stuck in DCPCSR
	35	3	LAT DCLO 1 stuck in PWR2REG
	36	3	DCLO 1 IEN stuck in DCPCSR
	37	3	DCLO 1 INT stuck in BIREG
	38	3	BUS LO 1 stuck in PWR1REG
	39	–	Not used
	40	4	DCLO 2 stuck in DCPCSR
	41	4	DCLO 2 stuck in PWR2REG
	42	4	LAT DCLO 2 stuck in DCPCSR
	43	4	LAT DCLO 2 stuck in PWR2REG
	44	4	DCLO 2 IEN stuck in DCPCSR
	45	4	DCLO 2 INT stuck in BIREG
	46	4	BUS LO 2 stuck in PWR1REG
	47	–	Not used
	48	5	BBU1 not functioning
	49	5	BBU2 not functioning
	50	6	SC INT stuck in PEMCSR
	51	6	SC INT stuck in PEMCSR (loopback)
	52	6	SC IEN stuck in PEMCSR
	53	6	SC IEN stuck in PEMCSR (loopback)
	54	6	SCU SC INT stuck in connector reg
	55	–	Not used
	56–63	–	Contents = 9 (test number)
A	0	0	RDBR DATA0 stuck
	1	0	RDBR DATA1 stuck
	2	0	RDBR DATA2 stuck
	3	0	RDBR DATA3 stuck
	4	0	RDBR DATA4 stuck
	5	0	RDBR DATA5 stuck
	6	0	RDBR DATA6 stuck
	7	0	RDBR DATA7 stuck

Table 8–6 (Cont.)   RBDSREG for Invokable Diagnostics

Diagnostic Number	Bit Number	Subtest Number	Error
	8	0	RCSR CMD DONE
	9	0	RCSR RTE
	10	–	Not used
	11	0	RCSR RNE
	12	0	RCSR RNF
	13	0	RCSR RCV ERR
	14	0	RCSR RCV IEN
	15	0	RCSR RCV DONE
	16	0	COMM RCV CLR RCV FIFO
	17	–	Not used
	18	–	Not used
	19	0	COMM RCV RNE
	20	0	COMM RCV RNF
	21	0	COMM RCV RCV ERR
	22	–	Not used
	23	0	COMM RCV SPU RCV DONE
	24	1	TDBR DATA0 stuck
	25	1	TDBR DATA1 stuck
	26	1	TDBR DATA2 stuck
	27	1	TDBR DATA3 stuck
	28	1	TDBR DATA4 stuck
	29	1	TDBR DATA5 stuck
	30	1	TDBR DATA6 stuck
	31	1	TDBR DATA7 stuck
	32	1	TCSR CLEAR FIFO
	33	–	Not used
	34	1	Not used
	35	1	TCSR TNE
	36	1	TCSR TNF
	37	1	TCSR TRANS ERR
	38	1	TCSR TRANS IEN
	39	1	TCSR TRANS RDY
	40	–	Not used
	41	–	Not used
	42	–	Not used

Table 8–6 (Cont.)   RBDSREG for Invokable Diagnostics

Diagnostic Number	Bit Number	Subtest Number	Error
	43	1	COMM XMIT TNE
	44	1	COMM XMIT TNF
	45	1	COMM XMIT TRANS ERR
	46	–	Not used
	47	1	COMM XMIT SPU TRANS RDY
	48–55	–	Not used
	56–63	–	Contents = 0Ah (test number)
B	0	0	Illegal character received
	1	1	RIC 11 not available
	2	2	RIC 12 not available
	3	3	RIC 13 not available
	4	4	RIC 21 not available
	5	5	RIC 22 not available
	6	6	RIC 23 not available
	7	7	RIC 31 not available
	8	8	RIC 41 not available
	9	9	RIC 51 not available
	10	0	RIC 52 not available
	11	1	RIC 14 not available
	12	2	RIC 15 not available
	13	3	RIC 24 not available
	14	4	RIC 25 not available
	15	5	RIC 32 not available
	16	6	RIC 42 not available
	17	7	RIC 53 not available
	18	8	RIC 54 not available
	19–55	–	Not used
	56–63	–	Contents = 0Bh (test number)
C	0	0	Bit0 - LED1 stuck
	1	0	Bit1 - LED1 stuck
	2	0	Bit2 - LED1 stuck
	3	0	Bit3 - LED1 stuck
	4	0	Bit4 - LED1 stuck
	5	0	Bit5 - LED1 stuck
	6	0	Bit6 - LED1 stuck

Table 8–6 (Cont.) RBDSREG for Invokable Diagnostics

Diagnostic Number	Bit Number	Subtest Number	Error
	7	0	Bit7 - LED1 stuck
	8	0	Bit0 - LED2 stuck
	9	0	Bit1 - LED2 stuck
	10	0	Bit2 - LED2 stuck
	11	0	Bit3 - LED2 stuck
	12	0	Bit4 - LED2 stuck
	13	0	Bit5 - LED2 stuck
	14	0	Bit6 - LED2 stuck
	15	0	Bit7 - LED2 stuck
	16	1	Bit0 - DISP1 stuck
	17	1	Bit1 - DISP1 stuck
	18	1	Bit2 - DISP1 stuck
	19	1	Bit3 - DISP1 stuck
	20	1	Bit4 - DISP1 stuck
	21	1	Bit5 - DISP1 stuck
	22	1	Bit6 - DISP1 stuck
	23	1	Bit7 - DISP1 stuck
	24	1	Bit0 - DISP2 stuck
	25	1	Bit1 - DISP2 stuck
	26	1	Bit2 - DISP2 stuck
	27	1	Bit3 - DISP2 stuck
	28	1	Bit4 - DISP2 stuck
	29	1	Bit5 - DISP2 stuck
	30	1	Bit6 - DISP2 stuck
	31	1	Bit7 - DISP2 stuck
	32	1	Bit0 - DISP3 stuck
	33	1	Bit1 - DISP3 stuck
	34	1	Bit2 - DISP3 stuck
	35	1	Bit3 - DISP3 stuck
	36	1	Bit4 - DISP3 stuck
	37	1	Bit5 - DISP3 stuck
	38	1	Bit6 - DISP3 stuck
	39	1	Bit7 - DISP3 stuck
	40–55	–	Not used
	56–63	–	Contents = 0Ch (test number)

Table 8-6 (Cont.) RBDSREG for Invokable Diagnostics

Diagnostic Number	Bit Number	Subtest Number	Error
D	0	0	DCLO 1 stuck in DCPCSR
	1	0	DCLO 1 stuck in PWR2REG
	2	0	LAT DCLO 1 stuck in DCPCSR
	3	0	LAT DCLO 1 stuck in PWR2REG
	4	0	DCLO 1 IEN stuck in DCPCSR
	5	0	DCLO 1 INT stuck in BIREG
	6	0	GRP A LO stuck in PWR1REG
	7	–	Not used
	8	1	DCLO 1 stuck in DCPCSR
	9	1	DCLO 1 stuck in PWR2REG
	10	1	LAT DCLO 1 stuck in DCPCSR
	11	1	LAT DCLO 1 stuck in PWR2REG
	12	1	DCLO 1 IEN stuck in DCPCSR
	13	1	DCLO 1 INT stuck in BIREG
	14	1	GRP B LO stuck in PWR1REG
	15	1	STANDBY H stuck in DCPCSR
	16	1	DCLO 2 stuck in DCPCSR
	17	1	DCLO 2 stuck in PWR2REG
	18	1	LAT DCLO 2 stuck in DCPCSR
	19	1	LAT DCLO 2 stuck in PWR2REG
	20	1	DCLO 2 IEN stuck in DCPCSR
	21	1	DCLO 2 INT stuck in BIREG
	22	–	Not used
	23	–	Not used
	24	2	DCLO 2 stuck in DCPCSR
	25	2	DCLO 2 stuck in PWR2REG
	26	2	LAT DCLO 2 stuck in DCPCSR
	27	2	LAT DCLO 2 stuck in PWR2REG
	28	2	DCLO 2 IEN stuck in DCPCSR
	29	2	DCLO 2 INT stuck in BIREG
	30	2	GRP C LO stuck in PWR1REG
	31	–	Not used
	32	3	DCLO 1 stuck in DCPCSR
	33	3	DCLO 1 stuck in PWR2REG
	34	3	LAT DCLO 1 stuck in DCPCSR

Table 8-6 (Cont.)   RBDSREG for Invokable Diagnostics

Diagnostic Number	Bit Number	Subtest Number	Error
	35	3	LAT DCLO 1 stuck in PWR2REG
	36	3	DCLO 1 IEN stuck in DCPCSR
	37	3	DCLO 1 INT stuck in BIREG
	38	3	GRP BBU LO stuck in PWR1REG
	39	–	Not used
	40	3	DCLO 2 stuck in DCPCSR
	41	3	DCLO 2 stuck in PWR2REG
	42	3	LAT DCLO 2 stuck in DCPCSR
	43	3	LAT DCLO 2 stuck in PWR2REG
	44	3	DCLO 2 IEN stuck in DCPCSR
	45	3	DCLO 2 INT stuck in BIREG
	46	3	GRP BBU LO stuck in DCPCSR
	47–55	–	Not used
	56–63	–	Contents = 0Dh (test number)
E	0	0	DIAGREG data00 stuck
	1	0	DIAGREG data01 stuck
	2	0	DIAGREG data02 stuck
	3	0	DIAGREG data03 stuck
	4	0	DIAGREG data04 stuck
	5	0	DIAGREG data05 stuck
	6	0	DIAGREG data06 stuck
	7	0	DIAGREG data07 stuck
	8	0	DIAGREG data00 stuck (loopback)
	9	0	DIAGREG data01 stuck (loopback)
	10	0	DIAGREG data02 stuck (loopback)
	11	0	DIAGREG data03 stuck (loopback)
	12	0	DIAGREG data04 stuck (loopback)
	13	0	DIAGREG data05 stuck (loopback)
	14	0	DIAGREG data06 stuck (loopback)
	15	0	DIAGREG data07 stuck (loopback)
	16	1	PEMCSR data00 stuck
	17	1	PEMCSR data01 stuck
	18	1	PEMCSR data02 stuck
	19	1	PEMCSR data03 stuck
	20	1	PEMCSR data04 stuck

Table 8-6 (Cont.)   RBDSREG for Invokable Diagnostics

Diagnostic Number	Bit Number	Subtest Number	Error
	21	1	PEMCSR data05 stuck
	22	1	PEMCSR data06 stuck
	23	1	PEMCSR data07 stuck
	24	1	PEMCSR data00 stuck (loopback)
	25	1	PEMCSR data01 stuck (loopback)
	26	1	PEMCSR data02 stuck (loopback)
	27	1	PEMCSR data03 stuck (loopback)
	28	1	PEMCSR data04 stuck (loopback)
	29	1	PEMCSR data05 stuck (loopback)
	30	1	PEMCSR data06 stuck (loopback)
	31	1	PEMCSR data07 stuck (loopback)
	32	2	STANDBY H stuck in DCPCSR
	33	3	SIM MCM PB H stuck in ACPCSR
	34	3	SIM SPU PF H stuck in ACPCSR
	35-55	–	Not used
	56-63	–	Contents = 0Eh (test number)
F	0	0	H7215 OK stuck in BIAS REG
	1	1	H7214 OK stuck in BIAS REG
	2	1	PTOFF 1 not gated by H7214 OK correctly
	3	1	PTOFF 2 not gated by H7214 OK correctly
	4-7	–	Not used
	8	1	LAT DCLO 1 stuck in DCPCSR
	9	1	LAT DCLO 1 stuck in PWR2REG
	10	1	LAT DCLO 2 stuck in DCPCSR
	11	1	LAT DCLO 2 stuck in PWR2REG
	12	1	LAT ACLO 1 stuck in ACPCSR
	13	1	LAT ACLO 1 stuck in PWR2REG
	14	1	LAT ACLO 2 stuck in ACPCSR
	15	1	LAT ACLO 2 stuck in PWR2REG
	16-55	–	Not used
	56-63	–	Contents = 0Fh (test number)

8.2   RIC Initialization Sequence and Diagnostics

This portion of the chapter covers the RIC power-up sequence, including the hard-core tests, RIC initialization, and the sequence of events executed during normal operation.

The RIC self-tests are executed on power-up or on command from the service processor by setting SCSREG [01], run self-test (RST). The hard-core tests are run first, followed by the general self-tests. The RICs have no callable diagnostics like the PEM. Therefore, if the Customer Services engineer wishes to run RIC diagnostics, it requires resetting the RIC.

The hard-core tests verify the integrity of the RICs kernel hardware, that logic which must be operational to allow the RIC to function minimally. The general tests verify the integrity of the nonkernel hardware, such as hardware registers, A/D converters, D/A converters, and clock circuitry.

A failure in a hard-core test results in a continuous loop on the failing test, with the RIC AUX LED blinking a pattern to indicate which hard-core test failed. A failure of the general self-tests is indicated by a failure code in the software error register (SEREG).

The action taken when a general self-test fails depends on which test failed. If the EEPROM checksum test fails, the RIC will not transfer control to the EEPROM but continues to execute out of EPROM, waiting for the PEM to down-line load new firmware to the EEPROM. A failure of the other general self-tests is fatal; the RIC does not enable any of the converters or even communicate with the PEM.

The RIC initialization and diagnostic sequence is covered using a flowchart, Figure 8–5, and corresponding callout list.
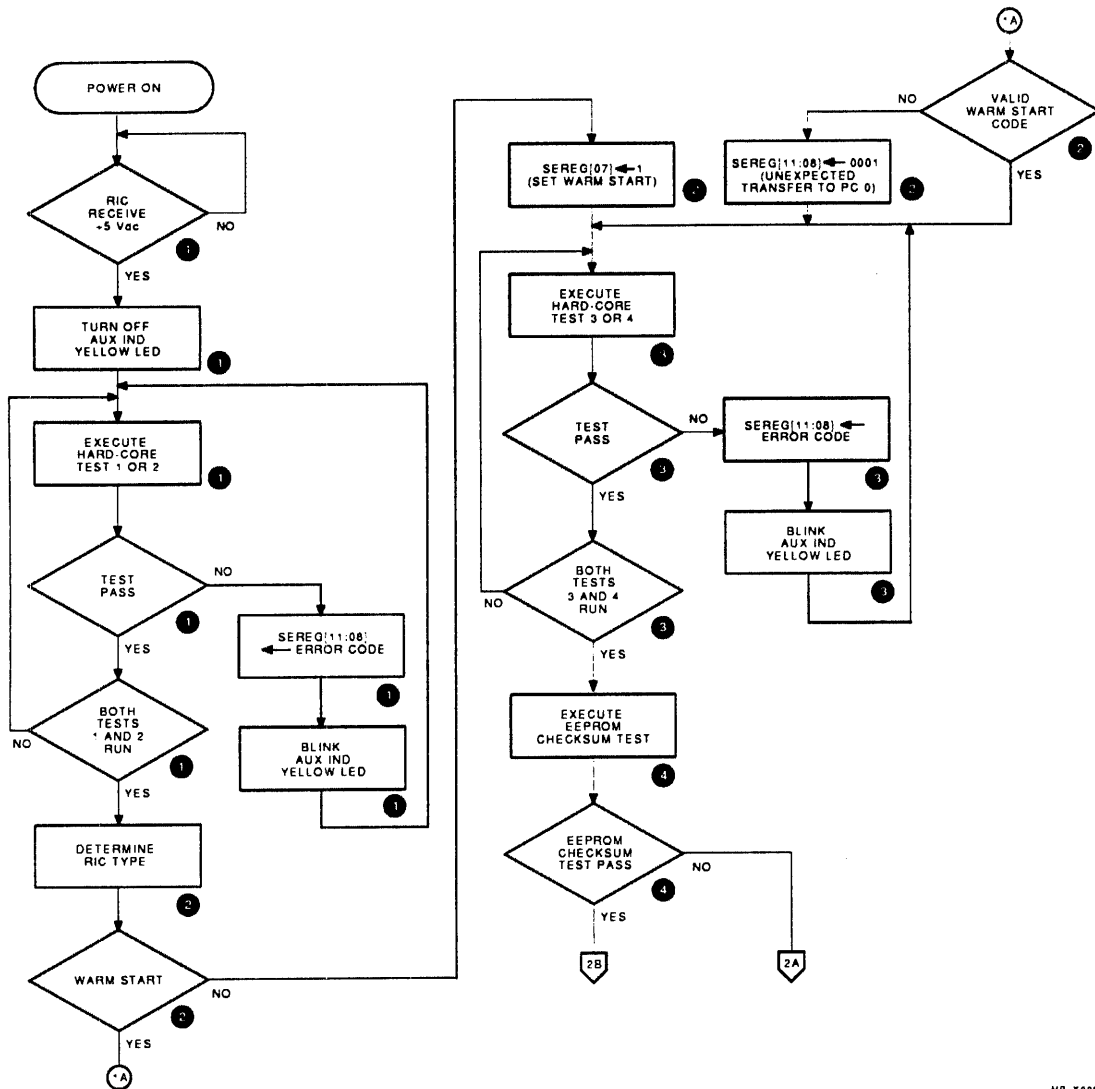
Figure 8-5 (Cont.) RIC Initialization and Diagnostics Flow Diagram
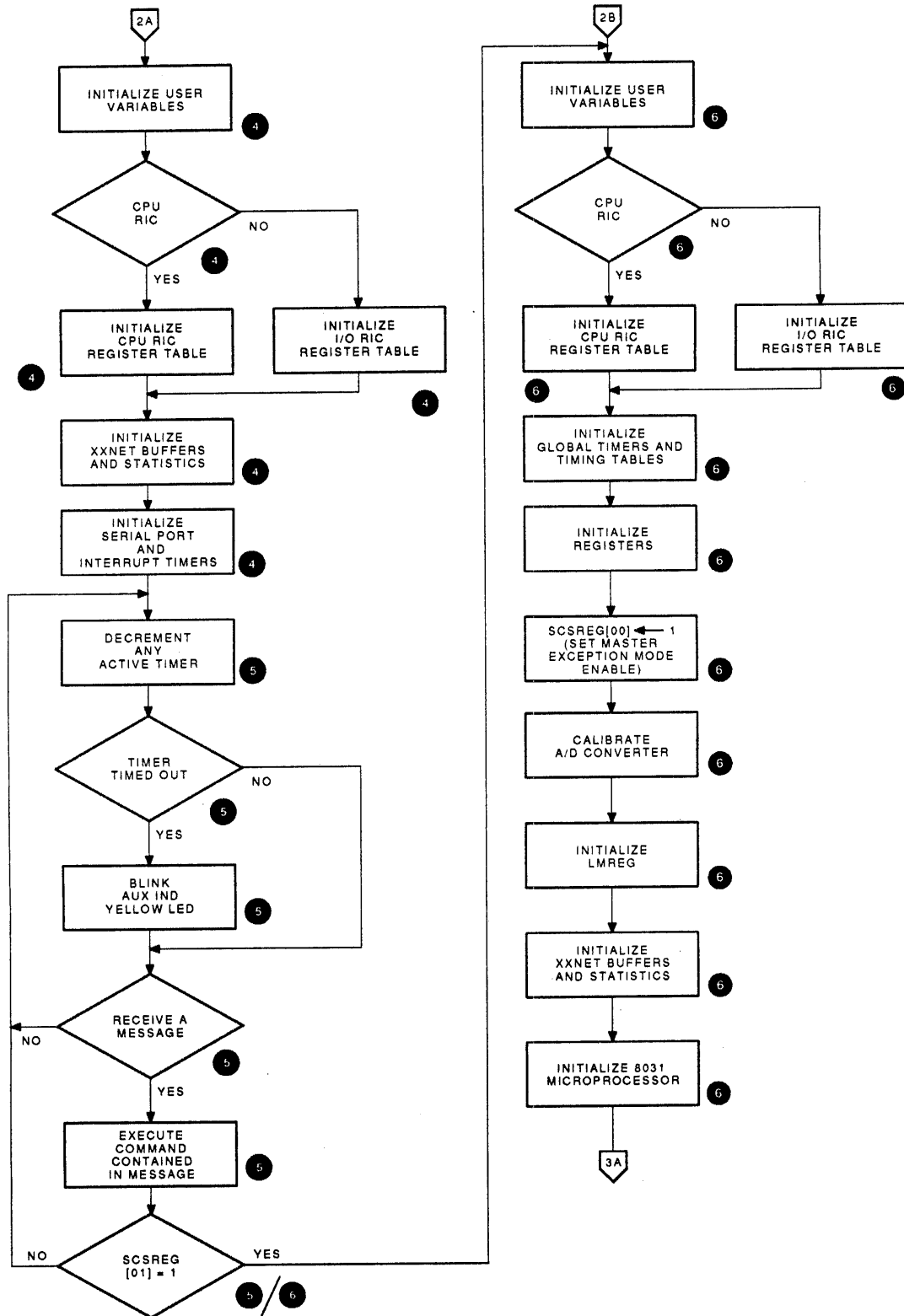
Figure 8–5 (Cont.)   RIC Initialization and Diagnostics Flow Diagram
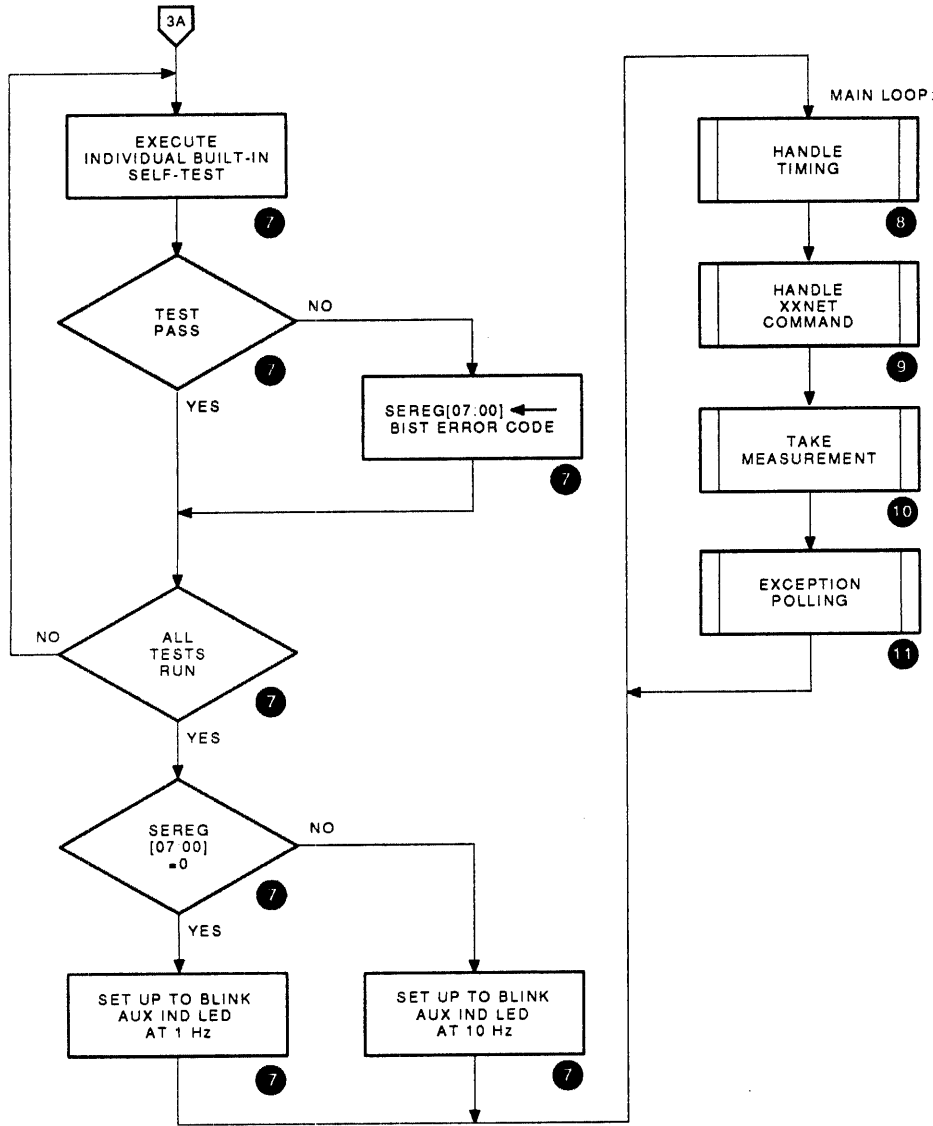
MR_X0069_90

MR_X0069_90

Figure 8–5 (Cont.)   RIC Initialization and Diagnostics Flow Diagram
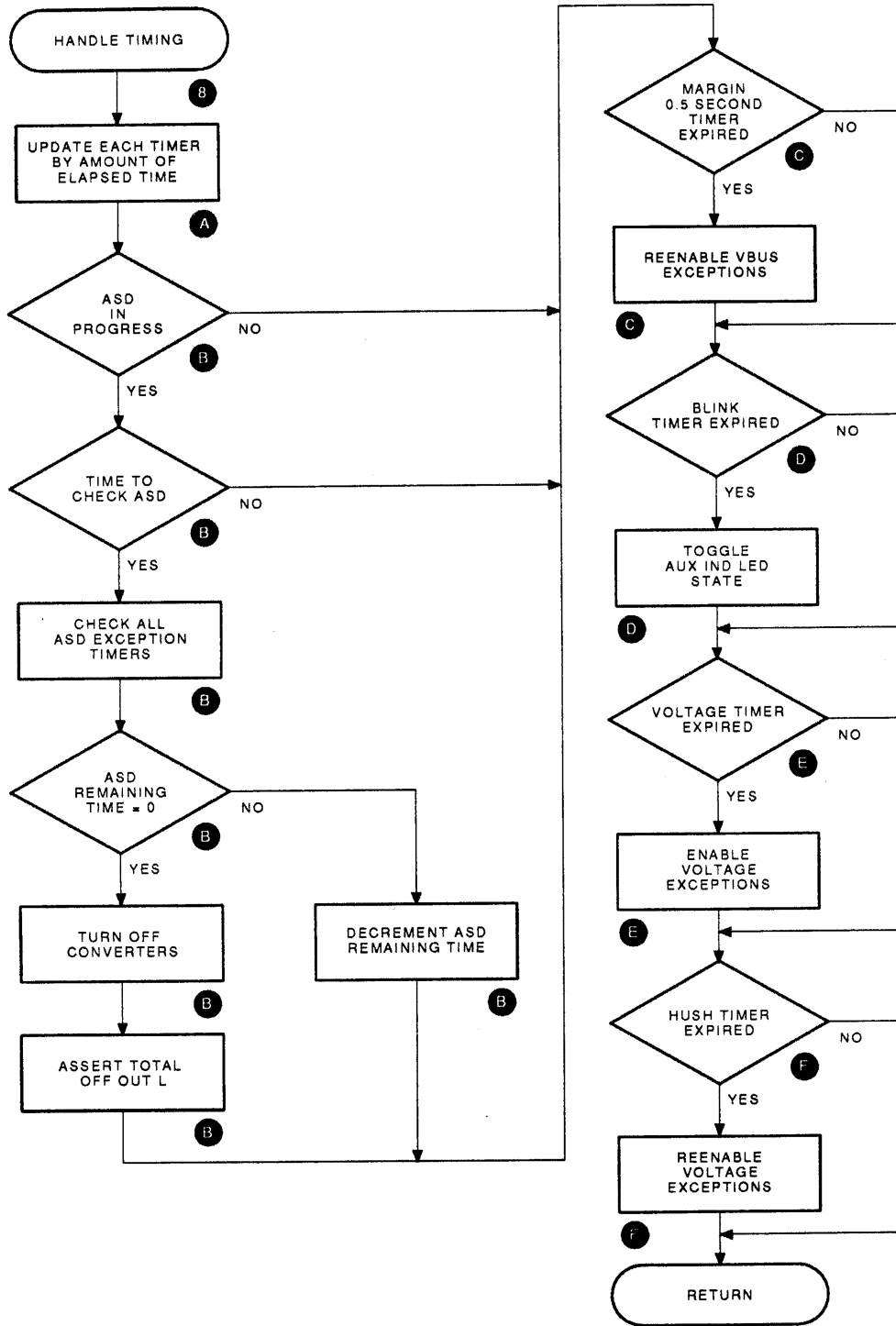
MR_X0070_90

Figure 8–5 (Cont.)   RIC Initialization and Diagnostics Flow Diagram
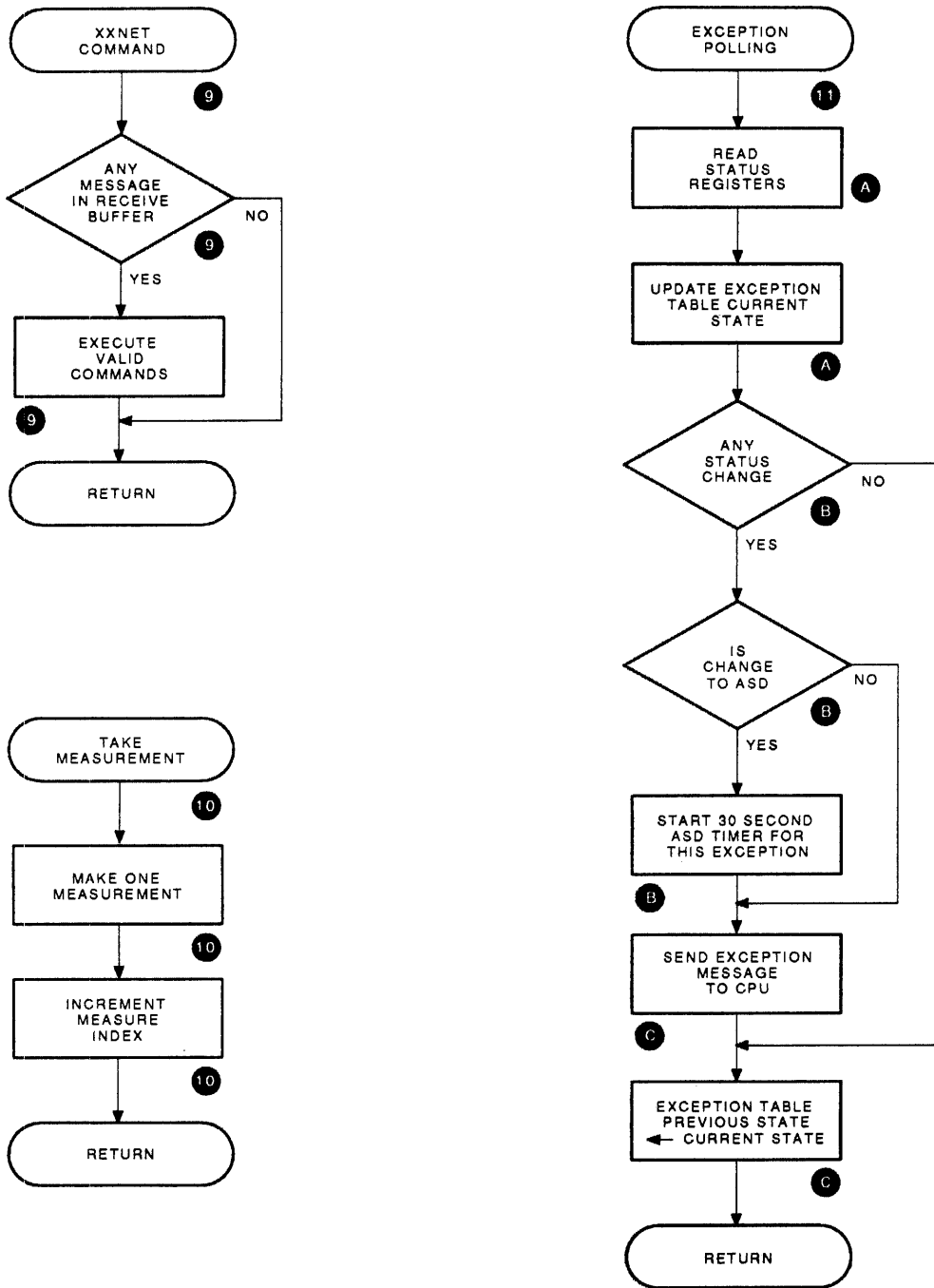
MR_X0071_90

Figure 8-5   RIC Initialization and Diagnostics Flow Diagram

❶ Turning the power on/off keyswitch to the on position routes 280 Vdc to the bias supplies, which generates the + 5 and ±15 Vdc used to power the RICs. A CPU RIC uses all three voltages, whereas an I/O RIC uses only the + 5 and +15 Vdc.

After receiving sufficient power, the RIC generates an internal reset and begins executing EPROM code. First it turns off the AUX IND yellow LED.

Hard-core tests 1 and 2 are executed. For a failure, software error register (SEREG) bits [11:08] are loaded with an error code and the AUX IND LED is blinked at a rate determined by the failing test (Table 8–7). The RIC loops on the failing test indefinitely. If, after failing once, the test passes, the SEREG contains an error code that indicates which hard-core test failed.

Table 8–7   RIC Hard-Core Test Error Codes

Test Number	Test Name	Blink Count	SEREG [11:08] Error Code
1	EPROM checksum	1	5
2	IRAM (internal 8031 micro-processor) RAM test	2	6
3	XRAM (external RAM test)	3	7
4	BBUS (buffered address bus test)	4	8
NA	EEPROM checksum test	NA	SEREG [07:00][1]

[1]The EEPROM failure code, 01_{16}, is placed in SEREG [07:00] by the RIC when the PEM reads the SEREG if there is an EEPROM checksum failure.

❷ The RIC reads the identification register (IDREG) to determine the type of RIC. The decision is based on the RIC ID. Each RIC reserves memory in external RAM for software registers for both a CPU and I/O RIC but only accesses registers according to the RIC type.

The powerfail register is checked to determine if this is a warm start (PFREG [07]). For a warm start, the software error register is checked to determine if it is a valid warm start code (SEREG [11:08]). The only valid warm start codes are two, unexpected hardware interrupt, and four, bad data structure, which indicates that the firmware has detected an out-of-range program parameter (read, write, BIS, or BIC with modifier greater than four, or an invalid LED state). If it is not a valid warm start code, SEREG [11:08] is set to 0001, unexpected transfer to PC 0.

If the warm start bit was not set, it is now set.

❸ Hard-core tests 3 and 4 are executed in the same manner as 1 and 2. A failure causes the failing test to cycle indefinitely, and the failing test is indicated by the number of times the AUX IND LED blinks (Table 8–7). Also, SEREG [11:08] is loaded with the error code for the failing test. If SEREG [11:08] contains a warm start code or runtime error code, and either of these hard-core tests fails, the error code is written over the warm start code.

❹ If both tests 3 and 4 pass, the EEPROM checksum test is run. If the EEPROM checksum fails, the RIC does not transfer control to the EEPROM but continues to execute code out of EPROM. First, variables and registers common to both types of RICs are initialized. The RIC sets up the XXNET backoff constant, initializes the timer array, clears buffers, clears the software control and status register (SCSREG), clears the SEREG except bits [11:08], which may contain a runtime error code, and enables writing the EEPROM.

The RIC register tables are initialized according to RIC type. The XXNET buffers and XXNET statistics are initialized to prepare for XXNET communications. The 8031 microprocessor serial port and interrupt timers are initialized. The PEM and RIC may now communicate, with the RIC executing out of EPROM.

❺ The RIC counts down the blink timer, the only active timer after an EEPROM checksum failure. When this timer times out, it causes the AUX IND LED to blink. The AUX IND LED is not lit at this time because of the EEPROM checksum error.

The receive buffer is checked for a message from the SPU. The legal commands that may be executed while the RIC is executing EPROM code are: read IRAM, XRAM, EPROM, EEPROM, or register; write register; BIS register; or DNLOAD. Not all registers may be written or have bits set by the BIS command, and no other commands are legal. Illegal commands or modifiers are indicated as errors in the reply message to the SPU.

The first message received from the PEM in its startup sequence is a read SEREG command. The PEM is checking for the status of the RIC self-tests. When the RIC decodes the command and determines that it is a read of the SEREG, before it sends the reply, it does two things:

- Loads SEREG [07:00] with 01_{16}, an indication that there has been an EEPROM checksum error.

- Enables the blink timer for 1/10 second, a 10 Hz blink rate. This indicates a self-test failure, but the RIC has received communication from the PEM. In one-tenth of a second, the blink timer expires, causing the firmware to light the AUX IND LED for 100 ms.

The RIC sends the command reply to the PEM, which is the contents of the SEREG. When the SPU decodes the failure in the SEREG, it down-line loads the RIC EEPROM with new code from EWBRC_nn.BIN, where nn is the revision number. The RIC responds to the DNLOAD commands that are received and writes the contents of the DNLOAD message into the EEPROM.

When the down-line load is complete, the RIC is stuck in this loop in EPROM CODE. The EEPROM error has presumably been corrected so the RIC no longer blinks the LED at 10 Hz. The RIC executes any commands it receives from the SPU. To get the code out of the loop, the SPU sets bit 1 in the RIC software control and status register (SCSREG), which causes the RIC to begin executing EEPROM code.

❻ When the EEPROM checksum test passes or the EEPROM has been down-line loaded with new code (and the SPU sets SCSREG [01]), the RIC starts executing code out of EEPROM. It first determines its RIC ID. If it is not a valid ID, the value is set to FF_{16}. It then initializes variables that are common to both types of RICs by reading values from EEPROM to set software registers and tables in external RAM. The XXNET backoff time is set according to the RIC number, and a suicide ID is set up. The suicide ID is sent to the PEM with the error code (suicide ID | error code | suicide ID | error code | suicide ID | error code) for total off conditions. The PEM writes this error code directly to the OCP diagnostic display LEDs. The OCP codes are found in Appendix B.

Based on the RIC type, the RIC-specific variables are initialized. These include the number of exceptions, number of BISTs, exception tables, register table, BIST table, and parameter limits register (PLREG). The PLREG contains the nominal voltage limits, temperature limits, and ASD time. The default voltage limits are shown in Table 8-8. The temperature limits are 49°C for yellow zone and 56°C for red zone. An open thermistor equates to -19°C and a shorted thermistor equates to 81°C. The default ASD time limit is 30 seconds.

Table 8-8   PLREG Default Voltage Limits

Bus	Low Margin		Nominal		High Margin	
	Low Limit	High Limit	Low Limit	High Limit	Low Limit	High Limit
5 V	4.51	4.98	4.75	5.25	4.98	5.51
3.4 V	3.07	3.39	3.23	3.57	3.39	3.75
5.2 V	4.69	5.19	4.94	5.46	5.19	5.73

The timers are set up and initialized and all timing tables are initialized. The margin register (MGNREG) is initialized with margins disabled. The exception mode enable register (EMEREG) is similar to the PEM exception mask enable register, where set bits enable exception reporting. Initialization is based on system type and RIC type. Once the individual exceptions have been enabled, the master exception mode enable bit is set. This allows enabled exceptions to be reported to the PEM.

The RIC automatically resets this bit after sending an exception. This prevents the RIC from sending more than one exception to the PEM at any one time. When the PEM forwards the message to the SPU, it reenables the RIC to send exception messages. During the time the RIC is disabled from sending exception messages to the PEM, it continues to monitor exception conditions. A condition that changes from good to bad and back to good again, during the time that exception reporting is disabled, is never seen. The same is true for a condition that changes from bad to good and back to bad again.

The A/D converter is calibrated and temperature measurements are taken and placed in the last measured register (LMREG). The bytes reserved for the voltage bus measurement and ground current are cleared before enabling the converters.

Voltage and MOD OK exceptions are enabled ½ second after the converters are turned on. By this time, the voltage is correct, so no exceptions are sent.

The XXNET buffers and XXNET statistics are initialized in preparation for XXNET communications, and the 8031 microprocessor serial port and total off interrupt timers are initialized. Communications with the PEM may now be carried out from the EEPROM, and the RIC can assert total off for ASD conditions.

❼ RIC type-dependent, built-in self-tests (BISTs) are executed (Table 8–9). For any BIST failure, an error code is written into SEREG[07:00]. When all tests have been run, the blink timer is set up according to these bits. If there were no errors, the blink timer is enabled to blink the AUX IND LED at a 1 Hz rate. This indicates that self-tests have passed, but the SPU has not communicated with the RIC. When the timer expires, the LED is blinked. Later, when the SPU reads the SEREG, the RIC lights the AUX IND LED.

If there were any BIST errors, the blink timer is set up for 10 Hz to indicate that there has been a BIST error. After the SPU reads the SEREG to open communications with the RIC, when the blink timer expires, the LEDs are blinked at 10 Hz.

Table 8–9   RIC Built-In Self-Tests

RIC Type	Test	Error[1] Code (Hex)	Error Description
CPU and I/O	Valid ID	8	Invalid ID
CPU and I/O	Regulator clock	2	Regulator clock low
		3	Regulator clock mid
		4	Regulator clock high
CPU	A/D converter	10	A/D converter timeout
		20	A/D converter offset too big
		30	A/D converter test low failure
		40	A/D converter test high failure
CPU	D/A converter	50	D/A converter test low failure
		60	D/A converter test high failure
CPU	VREF adjust	70	Unable to adjust VREF, too low
		80	Unable to adjust VREF, too high

[1]Written to SEREG[07:00]

NOTE
The next four blocks comprise the main loop of the EEPROM code. Each subprocedure is explained individually, with the steps of the subprocedure alphabetized.

❽ Handle timing.

a. Each of the timers is updated by the amount of time that has elapsed since the last update.

b. SEREG[07] is checked to determine if there is an ASD in progress. If not, the next timer is checked. ASD conditions (Table 7-12) are checked every five seconds. If they have been checked more recently than five seconds, the next timer is checked. If not, all ASD exception timers are checked. For any ASD timer that has not expired, the remaining time is decremented by five seconds.

When the 30 seconds has elapsed, the RIC turns off its converters and asserts TOTAL OFF OUT L to the SIP, which trips CB1 in the power front end.

If an ASD condition has cleared, that particular exceptions timer is reset and disabled. SEREG[13] (ASD pending) is cleared if all ASD conditions have cleared.

After initiating the total off condition, the RIC continues executing main loop code until interrupted by the PEM for the total off condition. It then determines if this RIC detected the total off condition. If so, it sends two bytes, the suicide ID and error code, to the PEM. These two bytes are repeated three times and do not conform to XXNET protocol.

c. If voltages are margined high or low in response to SPU commands, the voltage is changed in eight steps, 125 ms between each step. Therefore, the entire margin takes one second. A change from high margin or low margin to normal margin is carried out in the same manner; the voltage is increased or decreased in eight steps.

A change from high margin to low margin, or low margin to high margin, takes 16 steps, a total of 2 seconds.

At the time voltages are margined, EMEREG byte 0 bit 0 is reset to disable VBUS exceptions. As soon as the last step is completed, the exceptions are reenabled.

The handle timing procedure decrements the margin timer each time through the loop. If the ½ second timer has expired, the RIC disables the timer and reenables the VBus exceptions. This timer is enabled only when the margins are changed.

d. Each time the blink timer expires, the AUX IND LED state is toggled. The blink timer is enabled and set for either 1 second or 1/10 second, depending on the results of the BISTs. If the tests passed and the PEM has not communicated with the RIC yet, then the blink timer expires every second. Once the PEM communicates with the RIC, the blink timer is disabled and the LED is turned on.

If the BISTs failed and the PEM has not yet communicated with the RIC, then the LED is not lit. Once the PEM communicates with the RIC, then the timer is enabled, for 1/10 second, to blink the LED ten times a second.

e. The voltage timer is initialized to ½ second and enabled when the converters are enabled. When the voltage timer expires, the converter-specific exceptions are enabled by setting the appropriate bits of bytes 0, 1, 2, and 20 in the EMEREG (Table 8–10).

f. When interrupted by the PEM for a total off condition, each RIC determines if it is responsible for the total off condition (powerfail 1 register or ASD condition). The responsible RIC disables exceptions by clearing SCSREG[00]. This does not stop the RIC from polling for exceptions, it prevents the RIC from reporting exceptions.

All RICs initialize their hush timer to 5 seconds, and enable the timer. The hush timer disables any exception message reporting for 5 seconds.

The RIC responsible for the total off condition sends the suicide message (SUICIDE ID | ERROR | SUICIDE ID | ERROR | SUICIDE ID | ERROR) to the PEM, reinitializes the XXNET protocol, and returns to the main loop. The suicide message is unaffected by the hush timer.

❾ This procedure (XXNET command) monitors the receive buffer for incoming messages from the SPU. If there are any messages, the command is executed, with a reply, based on the command sent back to the SPU.

The RIC executes read, write, BIS, BIC, and measure commands. It cannot execute DOWNLOAD commands from EEPROM code. An error message is sent to the SPU for any message with an incorrect modifier or illegal opcode (DOWNLOAD). Messages with bad checksums are ignored.

❿ The take measurement procedure makes one measurement each time it is called. An index is incremented each time, causing the next item to be measured. The measurements include: temperature (thermistors), ground current, and VBus. The measured values are placed in the last measured register (LMREG). Only valid measurements are made. If the thermistor is not installed, this measurement is skipped.

⓫ There are two main steps in exception polling. The first step gathers information and updates the data for all exception conditions. The second step analyzes the data collected in the first step, deciding on actions to be taken, which may be sending an exception message to the SPU or initiating an ASD.

a. The RIC reads the status of the signals it is monitoring by reading the status registers. The CPU RICs read STATUSA, STATUSB, PWRFAIL1, and PWRFAIL2 registers. An I/O RIC reads STATUSA through STATUSF, PWRFAIL, BIREG0, and BIREG1.

The exception table current state is updated from the status registers, or for those exceptions based on measurements, the contents of the last measured register (LMREG).

b. The current state of the exception condition is compared to the the previous state to determine if there has been a status change. Status changes include voltage high, low, or nominal (margin state dependent). The temperature is checked for red zone, yellow zone, or open or shorted thermistor. For the remaining exceptions, the status bits are monitored for change. All RIC exception conditions, and the associated EMEREG enabling bit, are shown in Table 8–10.

Status changes consist of three types: to ASD, to normal, or to warning. If the change is to the ASD condition, the ASD 30 second timer is initialized and enabled. For any status change, an exception message is sent to the SPU.

c. The exception table previous state is updated to reflect the exception condition current state.

Table 8–10   RIC Exceptions

Exception Task	EMEREG Byte	Bit	Exception Condition
CPU RIC			
Bus voltage	0	0	VBus
Bus status	1	0	Group LO
		1	Overvoltage
		2	Overcurrent
		3	Crobar ready
Converter MOD OKs	2	0	MOD OK 0
		1	MOD OK 1
		2	MOD OK 2
		3	MOD OK 3
		4	MOD OK 4
Bias OKs	3	0	Crobar bias 1
		1	Crobar bias 2
		2	BIAS OK 1
		3	BIAS OK 2
Air temperature exception	4	0	Thermistor 0
		1	Thermistor 1
Reserved	5	–	–
Air flow exception	6	0	Air flow 0
		1	Air flow 1
		2	Air flow 2
		3	Air flow 3
Reserved	7–11	–	–

Table 8–10 (Cont.)   RIC Exceptions

| Exception Task | EMEREG | | Exception Condition |
	Byte	Bit	
I/O RIC			
Thermal warning	12	0	UPC thermal warning
Phase loss	13	0	UPC phase loss
Output current	14	0	UPC output current
Bus LO	15	0	PFE and UPC bus LO
Reserved	16–18		
UPC attention	19	0	UPC ATTN
XMI MOD OKs	20	0	H7215B MOD OK
		1	H7214B MOD OK
		2	H7215A MOD OK
		3	H7214A MOD OK
I/O cabinet air flow	21	0	Air flow 0
		1	Air flow 1
Reserved	22	–	–
Phase rotation	23	0	UPC phase rotation
Bias OKs	24	0	Transceiver adapter bias supply D
		1	Transceiver adapter bias supply C
		2	Transceiver adapter bias supply B
		3	Transceiver adapter bias supply A
		4	Bias supply B (XMI bias)
		5	Bias supply A (XMI bias)
BI expander cabinet A	25	0	NOK1A
		1	NOK2A
		2	NOK3A
		3	NOK4A
		4	DTFA
		5	OTFA
		6	BLKLOA
		7	Installed

Table 8–10 (Cont.)   RIC Exceptions

Exception Task	EMEREG Byte	Bit	Exception Condition
I/O RIC			
BI expander cabinet B	26	0	NOK1A
		1	NOK2A
		2	NOK3A
		3	NOK4A
		4	DTFA
		5	OTFA
		6	BLKLOA
		7	Installed
Reserved	27–31	–	–

9
Power Front End Description

This chapter provides an introduction and functional description of the H7390 power front end (PFE). Included are the major physical, electrical, and environmental specifications.

9.1 Power Front End Overview

The PFE is comprised of four major functional units. The majority of distribution, rectification, and control functions are contained within the functional units (Figure 9-1).

As shown in Figure 9-2, the PFE is contained in the bottom of the IOA cabinet. The PFE components (assemblies and modules) are integrated into a single cabinet component.
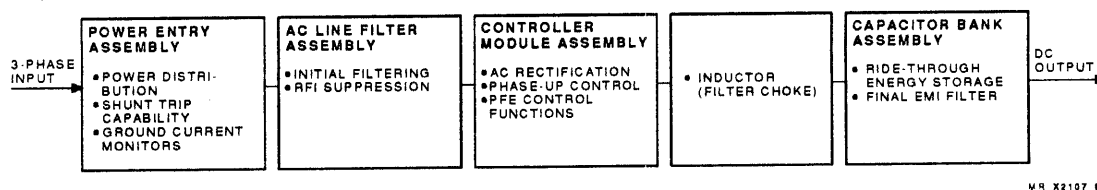
Figure 9-1 Basic PFE Block Diagram
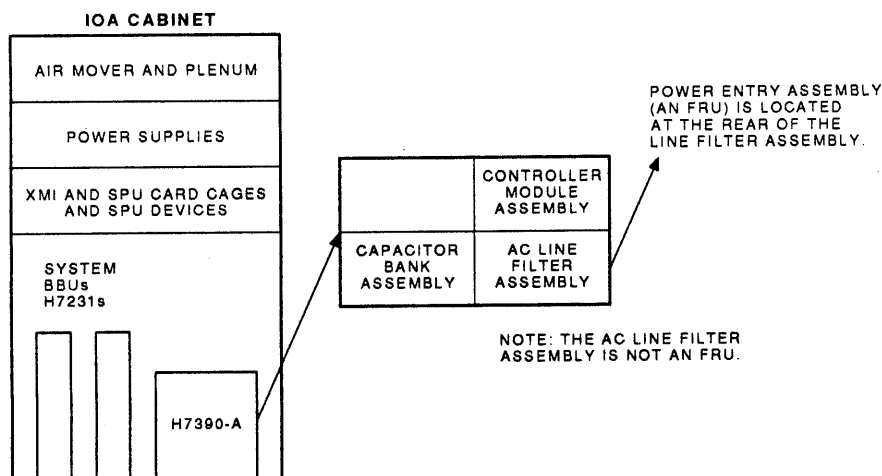
Figure 9-2 Basic IOA Cabinet Component Layout (Front Door Open)

The majority of the PFE components are contained in four assemblies: power entry, ac line filter, controller module, and capacitor bank assemblies. In addition, the PFE is highly modularized through extensive use of connectors on major components and modules.

9.1.1 Power Entry Assembly

The power entry assembly is accessed from the rear of the PFE (Figure 9-3) and is the ac power input entry point. In addition to the chassis, the assembly contains the main circuit breaker, the neon lamp assembly, and the ac power cable connections.

Power is distributed from the assembly through the main circuit (CB1), which serves as the main power switch. CB1 can be tripped off in the event of a severe internal failure and from the system through the TOTAL OFF function.

Input ground current is monitored from this assembly. The ground current is routed through the controller module assembly to the RICBUS and control module.

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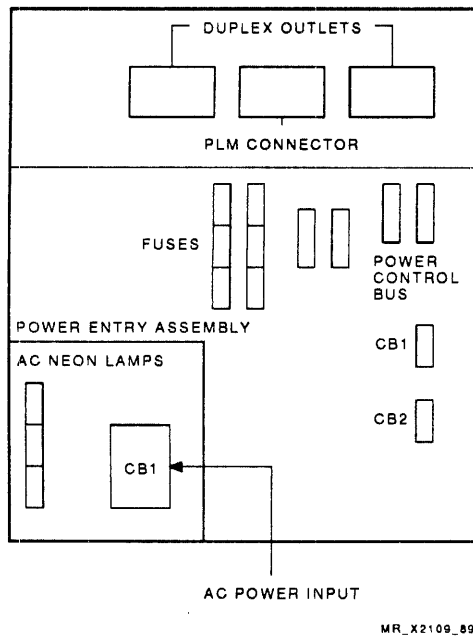
Figure 9-3   Power Front End (Rear View)

9.1.2 AC Line Filter Assembly

The ac line filter is *not* an FRU assembly. It is accessed from the front of the PFE (Figure 9–4). The filter suppresses input power EMI and PFE noise feedback into the utility. The assembly includes a set of metal oxide varistors (MOVs), which provide overvoltage and transient protection.

9.1.3 Controller Module Assembly

The controller module assembly is accessed from the front of the PFE (Figure 9–4). The assembly contains the SCRs that provide the full wave rectifier for the main dc output and phase-up (power-up).

The PFE control module is also in the assembly. The module provides the required PFE control and interfacing functions. The following list summarizes the major control and support functions:

- High-voltage dc output for the external bias supply

- SCR control logic for rectification and phase-up

- DC output bus monitoring

- Support of power control bus, total off, and RICBUS functions

- Generation of power-down and shunt trip coil functions

The assembly also contains the cooling fan, which provides cooling air for the entire PFE.
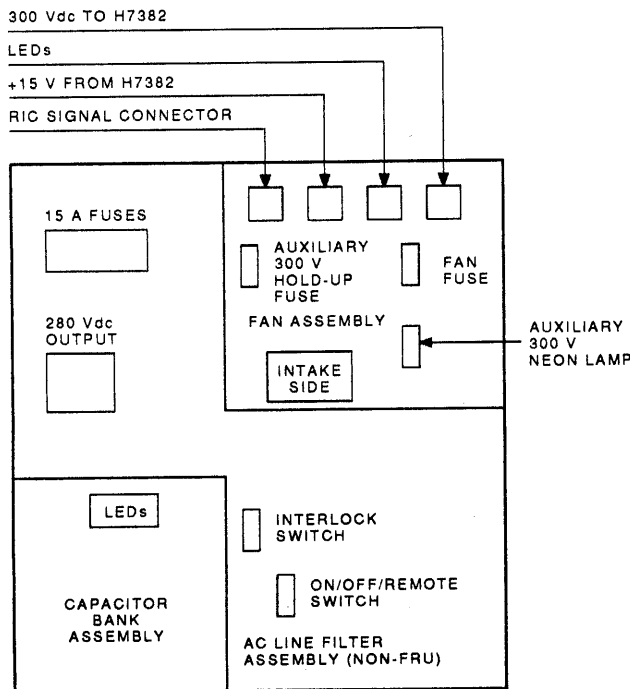
Figure 9–4   Power Front End (Front View)

9.1.4 Capacitor Bank Assembly

The capacitor bank assembly is accessed from the front of the PFE (Figure 9–4). The assembly provides the primary PFE energy storage required for the ride-through and hold-up times that allow the PFE to maintain its output in the event of a power interrupt or sag. Maintaining the output voltage during a power interruption allows the system to provide an orderly system shutdown.

The assembly consists of three banks of five capacitors each. The assembly also contains:

- A set of LEDs, which indicate charged/discharged capacitors
- Capacitor modules that serve as capacitor bank bus bars

In addition, the assembly also contains the final dc filter network.

9.1.5 Convenience Connectors

A pair of convenience outlets and a power line monitor (PLM) connector are located at the top rear of the PFE and above the capacitor bank.

9.2 Physical Specifications

Table 9–1 lists the PFE physical specifications.

Table 9–1 Physical Specifications

Parameter	Specification
Height	50.2 cm (19.75 in)
Width	56.5 cm (22.25 in)
Depth	62.2 cm (24.5 in)
Unit weight	157.5 kg (350 lb)

9.3 Electrical Specifications

The PFE is configured for a nominal operating source of 208 V rms at 60 Hz, with the specifications listed in Table 9–2.

Table 9–3 specifies the typical values for input phase currents with various line voltages at full load.

Table 9–2   Electrical Specifications

Parameter	Specification
Input voltage	161 (low line) – 229 (high line) Vac, 3-phase
Input frequency	57–63 Hz, 60 Hz nominal
Input current/phase	67 A rms maximum, 95 A peak
Input configuration	Wye input, 4-wire and ground
Neutral current	10 A rms maximum, 14.25 A peak
Ground current	5 A rms maximum
Input bias voltage	+15 Vdc, supplied externally
Input bias current	1 A maximum
Output voltage	210–324 Vdc, 280 Vdc nominal
Output voltage ripple	5 V p-p maximum
Output power rating	18.5 kW maximum
Auxiliary output voltage	210–324 Vdc, 280 Vdc nominal
Auxiliary voltage ripple	10 V p-p maximum
Auxiliary output power	325 W maximum
Power factor	90% minimum
Efficiency	95% minimum

Table 9–3   Input Current Load Specifications

Line Load	Phase Current	Phase-to-Phase Voltage	Output Load
Nominal line/full load	52 A rms, 74 A peak	208 Vac rms	18.5 kW
Low line/full load	67 A rms, 95 A peak	161 Vac rms	18.5 kW
High line/full load	47 A, 67 A peak	229 Vac rms	18.5 kW

9.4 PFE Functional Description

This section provides a functional overview and describes the main power path flow (Figure 9–5).

As an aid to correlating the functional description and its block diagrams with the schematic drawings, the text and functional block diagrams reference the related schematic drawing and sheet numbers wherever practical.

Also where practical, connector and pin numbers are referenced on the block diagrams. Major signal names and their mnemonics are also included in the text.

Diagrams and text references use the following notation:

- Schematic and sheet number references use the form: (54 19471-0-1, 2-7), and are read as: schematic number 54-19471-0-1, sheet 2 of 7.

- Connector references use the form: (J2-4), and are read as: connector J2, pin 4.

- Signal names include full titles with the mnemonics in parenthesis (if applicable): phase C ac low trigger (PHC ACLO TRIG).
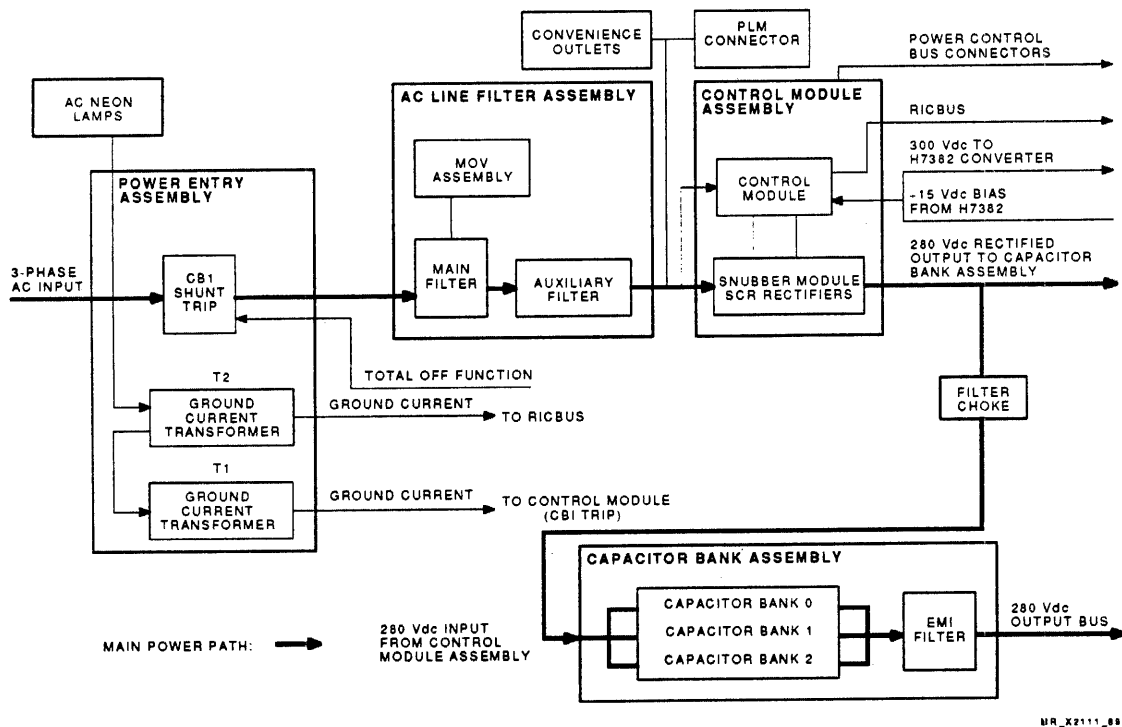
Figure 9–5 Basic PFE Functional Block Diagram

9.4.1 Power Input and Distribution

Three-phase ac power is supplied from the ac utility to the PFE through a 1-gauge, 5-wire, type W, power cable. The power cable is approximately 4.3 m (14 ft) long and is connected to the utility through a 5-pin, 100 A connector. The cable is routed to the ac connector panel in the power entry assembly.

9.4.2 Power Entry Assembly

As shown in Figure 9-6, the power entry assembly contains the main PFE input circuit breaker (CB1), which serves as the main power switch. The 3-phase ac utility power is applied to the line (input) side of CB1.

Incorporated into the CB1 assembly are a set of auxiliary switch contacts, and a shunt trip coil. The auxiliary switch contacts, which operate with the main contacts, are used in the PFE and the kernel to indicate CB1 status, and provide a BBU interlock circuit (C-DD-H7390-0-0, 1-7).

A set of three neon lamps (mounted on a module in the assembly) are connected, through J21, across each input phase to neutral. The neon lamps are on as long as ac power is applied to the PFE.

INPUT PHASE
MONITOR LEDs

PHASE A

PHASE B   TO AC LINE FILTER

PHASE C

PHASE A   CB1
SHUNT   TOTAL OFF FROM CONTROL MODULE
TRIP
COIL*

CB OK TO RICBUS

CB OK RETURN

BBU INTERLOCK TO RICBUS

BBU INTERLOCK RETURN
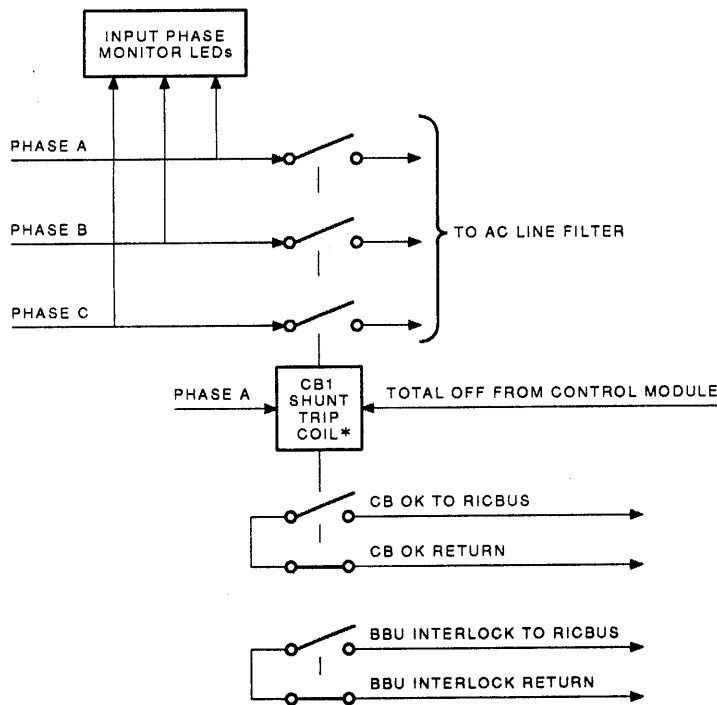
*CB1 SHOWN RESET

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Figure 9-6   Power Entry Block Diagram

9.4.2.1 Shunt Trip Capability and Auxiliary Functions

The shunt trip coil provides the circuit breaker trip capability; CB1 can be remotely tripped (forced to off). The trip capability disconnects the PFE from the input utility in the event of some internal PFE faults, or external kernel faults (Figure 9–3).

The shunt trip coil is activated from a relay located on the control module (54194471, 5-7). When energized by the TOTAL OFF function, the relay applies phase B input voltage to the shunt trip coil. The shunt trip coil trips CB1 off in approximately 18 ms.

When tripped off, CB1 must be manually set to off and then reset to on. With CB1 tripped, the shunt trip coil is opened to prevent the trip current from overheating the coil.

CB1 also contains a set of auxiliary contacts, which provide:

- The interrupt function for the BBU failsafe relay

- A short circuit for the ac breaker ok (AC BRK OK) function on the RICBUS.

With CB1 on (and auxiliary contacts closed) the BBU failsafe enable circuit in the kernel is armed through the failsafe relay. However, when CB1 is tripped off, either remotely or manually, the auxiliary contacts open and effectively disable the failsafe relay.

The AC BRK OK contacts complete a ground connection to the signal interface panel (SIP) in the kernel PCS. With CB1 closed, the ground circuit to the SIP is asserted low, which resets a status register bit in the PCS. With CB1 set (or tripped) to off, the ground circuit is broken. This action effectively asserts the related status register bit and initiates a PCS response.

9.4.2.2 Ground Current Monitors

The PFE contains two ground current monitors. The monitors detect unacceptable PFE or system ground currents due to incorrect system grounding, or major leakage between the power circuitry and chassis ground. The monitors consist of two current transformers (T1 and T2), with each transformer capable of sensing a continuous 5 A input (C-DD-H7390-0, 1-8).

Each transformer contains a 1-turn primary, and a 200-turn secondary. The primaries of both transformers are connected in series between the utility and PFE grounds. The secondary windings develop a current equal to the ground current divided by 200. Both transformer outputs are coupled to the control module through J1. (See Figure 9–7.)

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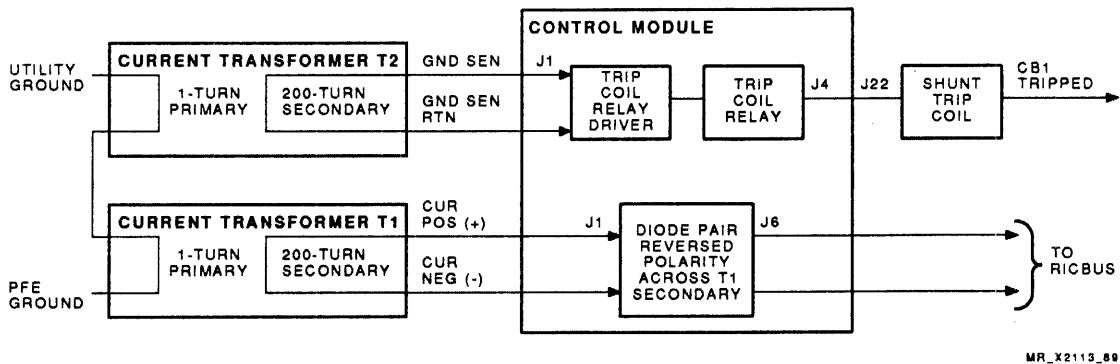
Figure 9–7   Ground Current Monitors

If the ground current reaches 10 A ± 5 A the T1 output effectively trips CB1. The output (GND SEN, GND SEN RTN) is coupled into the shunt trip driver circuit (54-19471-0-1, 5-7).

The ground current is rectified and turns on the shunt trip driver, energizing the trip coil relay (K501). The contacts of K501 apply the line voltage of phases B and C across the trip coil of CB1, tripping it to off (C-DD-H7390-0-0, 1-8).

The secondary output of T2 (CUR POS, CUR NEG) is directly coupled through J6 of the control module to the RICBUS. Two diodes within the module are connected across the secondary to prevent damage to the transformer (54-19471-0-1).

The ground current should be measured when the system is initially installed. This measurement can then be used for comparison during later maintenance activities (for example, PM checks).

9.4.3 AC Line Filter Assembly

The 3-phase input from the load side of CB1 is connected to the ac line filter assembly. The assembly consists of two ac filters connected in series: main filter and auxiliary filter (Figure 9-8).

A pair of MOVs are connected across each phase of the main filter input and ground. In addition, a MOV is connected across each phase and the neutral conductor (C-DD-H7390-0-0, 2-8). This wiring configuration provides input line overvoltage and transient protection.

The 3-phase output of the auxiliary filter is distributed to two points in the controller module assembly:

- Through a fuse block to J4 on the control module

- Through J30 to the rectifier and snubber module
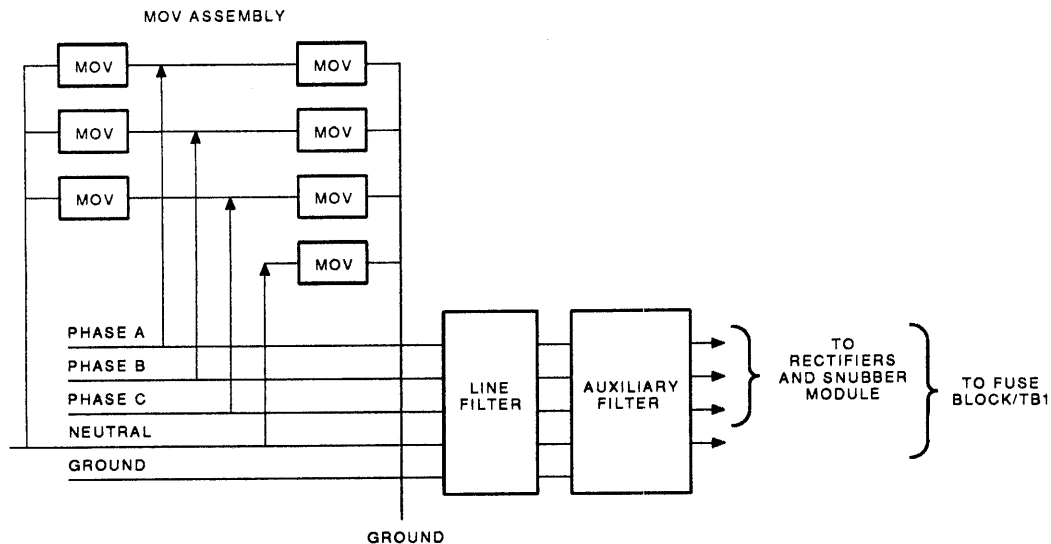
MR_X2115_89

Figure 9-8   AC Line Filter Assembly

9.4.4 Convenience Outlets and PLM Connector

Phases A and C are tapped off TB1 and supplied to the pair of duplex convenience outlets located at the rear and above the capacitor bank assembly (C-DD-H7390-0-0, 3-8) (Figure 9–3). As shown in Figure 9–9, phase C powers the BBU outlets (J15) through a 5 A circuit breaker (CB3). Phase A powers the auxiliary outlets (J14) also protected by a 5 A circuit breaker (CB2).

A PLM connector, located on the rear of the PFE, is connected across each phase and neutral on the line side of CB1. The connector provides an outlet for ac power line monitoring.

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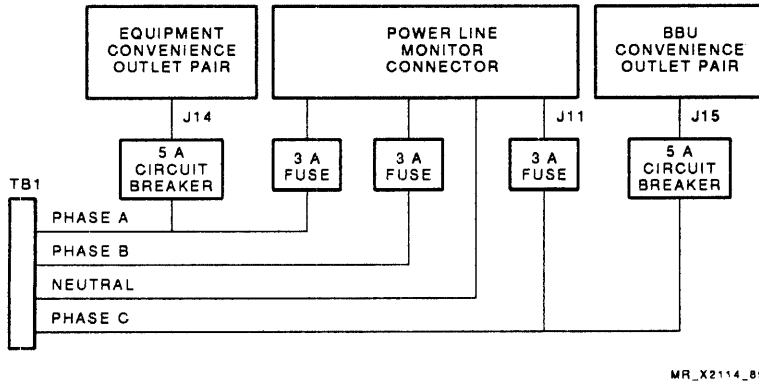
Figure 9–9   Convenience Outlets

9.4.5 Controller Module Assembly

The controller module assembly provides the rectification, control, phase-up, and cooling functions. Inputs and outputs of the other assemblies are monitored and controlled through the control module of the assembly.

9.4.5.1 AC Power Rectification
The SCRs provide the full wave rectification for the main dc output. The dc output from the rectifiers is passed through an inductor and the capacitor bank assembly to remove the 360 Hz ripple voltage.

9.4.5.2 Bias Supply Voltage
The 3-phase input to J4 of the control module is applied to a full wave rectifier. The rectifier output provides an auxiliary 280 Vdc to power an H7382 converter located in the IOA cabinet. The converter output returns a 15 Vdc bias voltage to the control module for development of the isolated logic circuit voltage.

The 300 Vdc auxiliary output to the H7382 is monitored by a neon lamp. The lamp, located on the front of the controller assembly, is connected across the rectifier output. The lamp remains on as long as the rectifier produces the 280 V output.

9.4.5.3 Main and Auxiliary Output Connection

The auxiliary 280 Vdc output is connected through diodes to the main 280 Vdc output. (See Figure 3-10.) The two outputs are connected through the output bus sense lines (DC BUS SENSE) on the control module (541971-0-1, 1-7). This connection allows the main 280 V output to maintain the auxiliary dc output if the input ac power should fail.

Without this connection and an input power failure, the auxiliary output would quickly drop to zero. This, in turn, would shut down the H7382 and turn off the +15 Vdc bias voltage to the control logic power supply on the control module. The control logic would not be able to sequence the AC LO and BUS LO functions (541971-0-1, 1-7) correctly.

In addition, a 2 A (F11) fuse is placed in series with the diode connection for protection in the event the auxiliary output is shorted. Should a short circuit occur, the main output will discharge into the auxiliary output and clear the fuse.
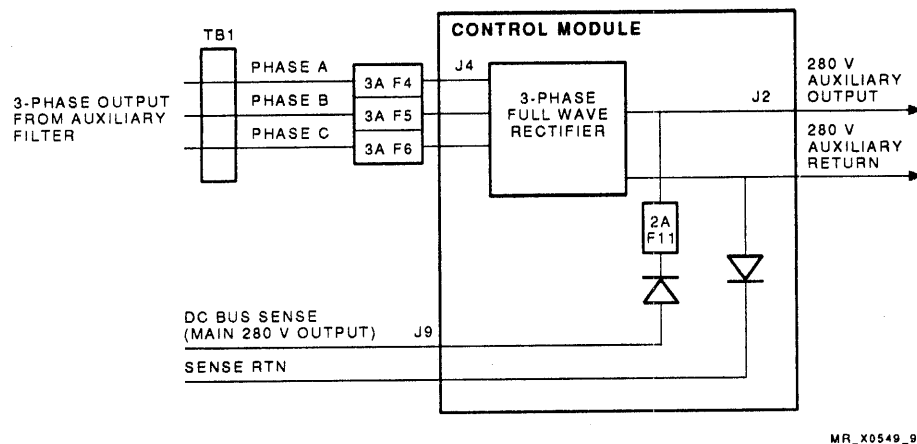
MR_X0549_90

Figure 9-10   Main and Auxiliary Output Connection

9.4.5.4 PFE Cooling

The assembly also contains the cooling fan. In addition to cooling the controller assembly, the air flow is shunted through louvers into the capacitor bank to provide cooling for the capacitors and related assembly components. Phases A and B from the 3-phase input of J4 are routed to J3 (of the control module). The fan is connected across phases A and B and protected with a 2 A fuse (C-DD-H7390-0-0, 4-8).

9.4.6 Capacitor Bank Assembly

As shown in Figure 9–11, the dc output voltage is split across each bank of the capacitor assembly. The input and output of the capacitor assembly are fused for 40 A (K-DD-5418779-0-0, 1-1). The banks provide the storage energy required to produce the ride-through and hold-up times. The capacitor banks are equipped with fast and slow bleeder resistors to protect service personnel.

The dc output is coupled to the EMI filter, which is part of the bank assembly. The filter acts as the final output filter network to remove any EMI on the dc output bus. The output bus cable connector (J32) is connected to the power input panel (PIP) of the IOA cabinet.
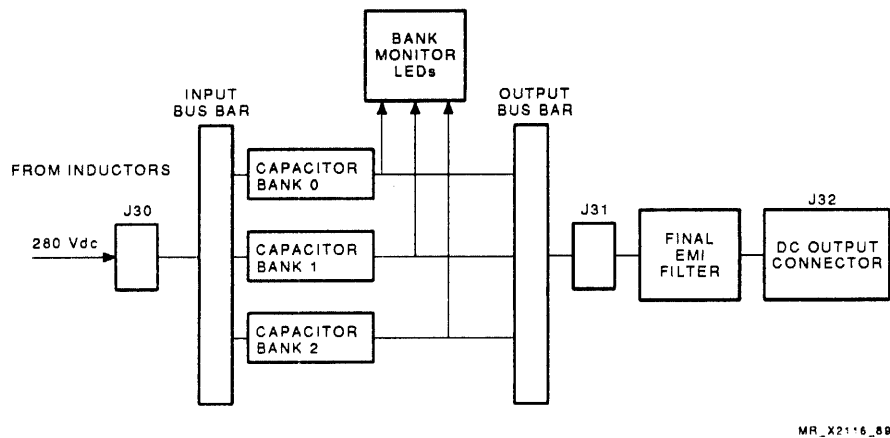
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Figure 9–11   Capacitor Bank Assembly

9.5 Control Module Operations

All PFE operations are controlled by the control module located in the controller module assembly. This section provides functional descriptions of each control circuit and the related operations.

9.5.1 Isolated Power Supply

The bias voltage from the H7382 is returned to the control module through J5. The 15 Vdc input is passed through a capacitor input filter to remove residual ripple and is applied to a pulse width modulator (PWM) chip (5419471-0-1, 4-7). The switching action of the PWM chip chops the 15 Vdc input to a high frequency square wave (Figure 9-12).

The square wave drives the primary of a transformer. The output of the transformer secondary is rectified and filtered through an LC filter network, producing a 12 Vdc output. The output voltage is unregulated and varies directly with the +15 Vdc input. The transformer also provides the required logic voltage isolation.

Power supply operation is monitored by an LED connected across the output. The LED (D522) remains on as long as the supply produces the 12 V output.
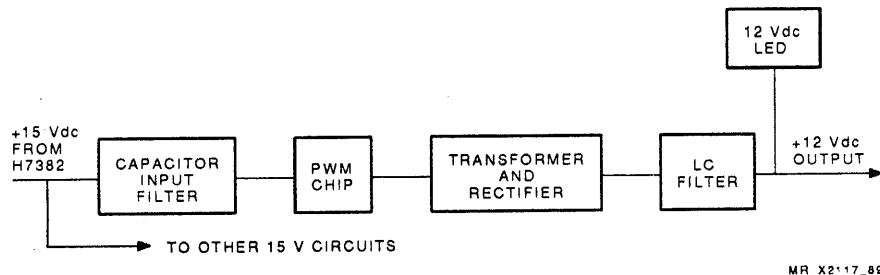
Figure 9-12   Isolated Power Supply

9.5.2 Local/Remote Operation

Remote and local operation is controlled through the 3-position, 3-pole ON/OFF/REMOTE switch located on the front of the controller module assembly. Remote operation is initiated from the remote position through the power control bus, while local operation is initiated through the ON position of the switch. The control bus is applied through J4A (and the parallel connection of J4B) of the power entry assembly to J1 of the control module.

Both remote and local phase-up and power-down functions share the same circuitry on the control module. However, the remote and local input functions are isolated by diodes. The power request (PWR REQ) of the control bus, and local (LOCAL) functions, initiate the phase-up operation. The power inhibit (PWR INH) of the control bus and local off (LOCAL OFF) functions initiate the power-down operation (5419471-0-1, 3-7). In the OFF position, the switch disables the BBU through the BBU interlock signal (BBU INTLK).

9.5.3 Phase-Up

The phase-up operation requires 18 seconds from initiation to full dc power output. To reduce the inrush current, phases A and B are initially switched on and begin a timed dc voltage buildup. Phase C is held off until the end of the 18-second period. At that point, it is turned on with a small amount of additional inrush current. Phase-up is controlled through the sequencing of the rectifier SCRs. Figure 9–13 illustrates the phase-up of phase A.

The phase A SCR is gated on just before the negative-going, zero-crossover point of the incoming phase A cycle. The ac current is rectified and produces a small dc output pulse. On each succeeding cycle, the SRC is triggered further up on the negative-going side of the incoming positive cycle. At the end of the 18-second time delay, phase C is gated on and:

- The dc output is increased to a nominal 280 Vdc

- BUS LO and AC LO are negated

- BUS LO LED is turned on

DC output is dependent on the ac input voltage. With an ac input of 208 Vac and a nominal load, the dc output is approximately 280 Vdc. If the ac input is higher than nominal, the dc output is also higher. Also, if the dc load is higher than nominal, the dc output voltage is lower.

9.5.3.1 Snubber Module Operation

The 3-phase ac input is applied to the snubber module (K-DD-5418662-0, 1-1). During phase-up, the module provides the outputs for the SCR turn-off functions. Both functions are coupled into the SCR gate driver circuits on the control module.

Each input phase is applied to an RC network on the snubber module (Figure 9–14). The ac voltage is sampled across the network. The sample represents the turn-off function and is coupled into the optical isolators of each phase SCR gate driver circuit (5419471-0-1, 6-7).

As the sampled ac voltage increases, the turn-off function output also increases. The ac voltage is coupled through a diode into the optical isolator driver. The driver is biased on, turning on the optical isolator, which in effect disables the SCR gate driver circuit.

PHASE A SCR GATED ON

PHASE A
INPUT

SCR
OUTPUT

PHASE C ENABLED

DC
OUTPUT

18 SECONDS

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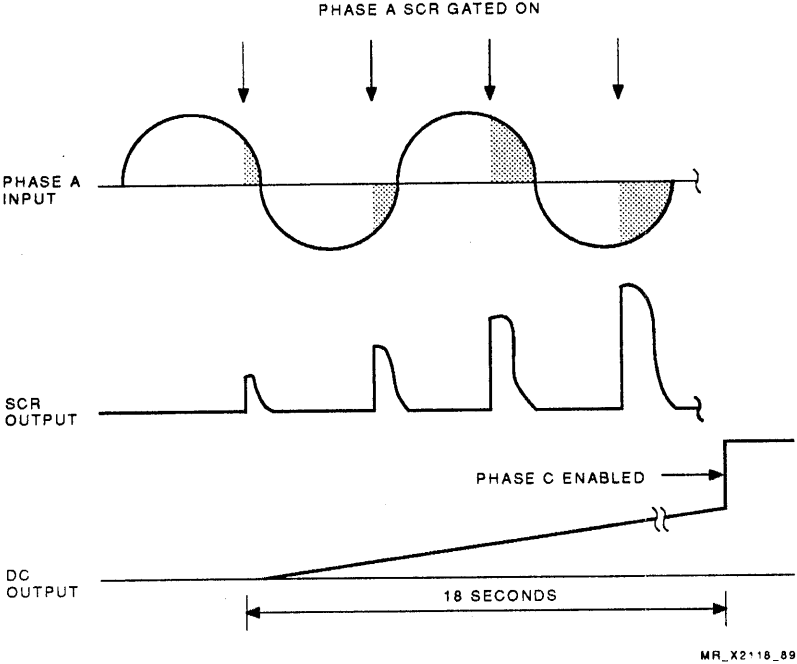
Figure 9–13   Basic Phase-Up Operation

SNUBBER
MODULE

PH A TRIG

PHASE A → SAMPLING
VOLTAGE
RC NETWORK

PHA OFF TRIG → OPTICAL
ISOLATOR
DRIVER

OPTICAL
ISOLATOR

GATE
GENERATING
LOGIC

PH A GATE

PHASE B → IDENTICAL TO PHASE A

PHASE C → IDENTICAL TO PHASE A

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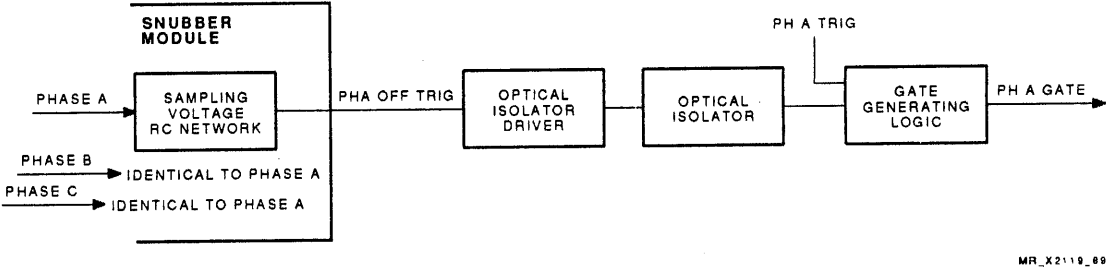
Figure 9–14   Snubber Module Simplified Block Diagram

9.5.3.2 Crossover and SCR Gate Drives

The ac input is also applied to a zero crossover detector on the control module (Figure 9–15). The detector drives an RC circuit, which provides the 18-second phase-up time (equivalent to 1080 cycles). The linear charging ramp provides a reference that determines the amount of the input ac waveform used in gating on the SCRs (5419471-0-1, 2-7).

The output also feeds an op amp and voltage comparator circuit, which generates the phase A trigger (PH A TRIG). PH A TRIG is an input to the SCR gate generating logic, which produces the phase A gate (PHA GATE). As shown in Figure 9–15, the turn-off optical isolator output is part of the logic network to serve as the gate disable function.

The output of the voltage detector monitors the voltage from phases A and C. The circuit will allow the loss of approximately 3 to 5 cycles before it will power down the PFE. If one of the phases is lost, the PFE will reset and power down. It will not phase up again until the input phase is restored.

The second input to the timing circuit is the output of an optical isolator that is in parallel with the BUS LO isolator. At the point in the phase-up ramp that BUS LO is negated, the timing circuit isolator output is also negated.

The output of the timing circuit generates a reset function (RESET) into the phase C trigger latch, effectively initiating the phase C trigger (PH C TRIG) function (5419471, 2-7). As with the other trigger functions (A and B), PH C TRIG is coupled into the SCR gate generating logic.

The phase C SCR gate generating logic produces two gate functions (PHC1 GATE and PHC2 GATE). The two driver gate functions are required since phase C incorporates two SCRs to hold that phase-off for the 18-second delay.

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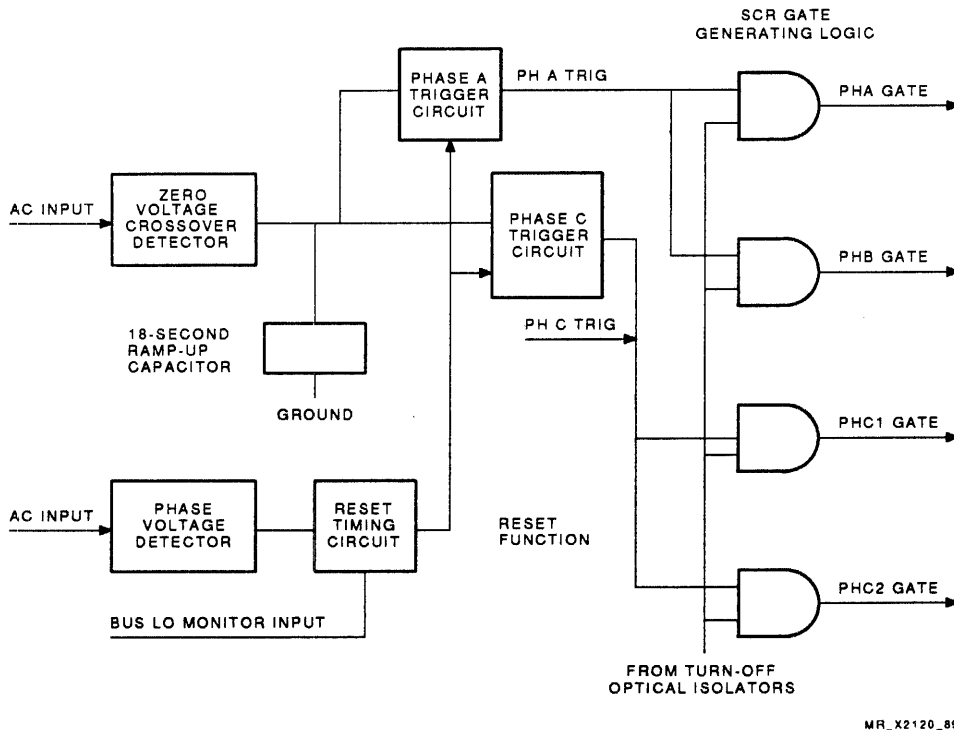
Figure 9–15   Crossover and SCR Gate Drives

9.5.3.3 SCR Driver Operation

Each phase gating function (for example, PHA GATE, ORPHC1 GATE) is applied to an identical SCR driver circuit (Figure 9-16). The gate function (PHx GATE) is applied to a transistor array. The push-pull output of the array is coupled into a MOSFET driver. The MOSFET, in turn, drives a 1:1 turns ratio isolation transformer.

Isolation is required since the array and MOSFET on the transformer primary operate at a logic level of 15 Vdc, while the SCRs on the transformer secondary are at 208 Vdc. The transformer output drive is developed across the 200-ohm load resistor (5419471-0-1, 7-7). The output is applied across the gate and cathode of the SCR, turning it on.
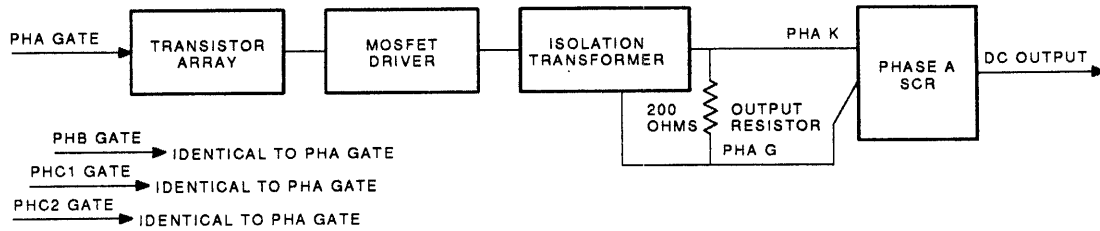
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Figure 9-16   SCR Driver Circuit

9.5.3.4 DC Output Monitor

During phase-up, the BUS LO and AC LO functions are disabled when phase C is triggered on. Following a 2-second delay, both functions are enabled and negated (H), indicating that the dc output has reached its nominal voltage (Figure 9-17).
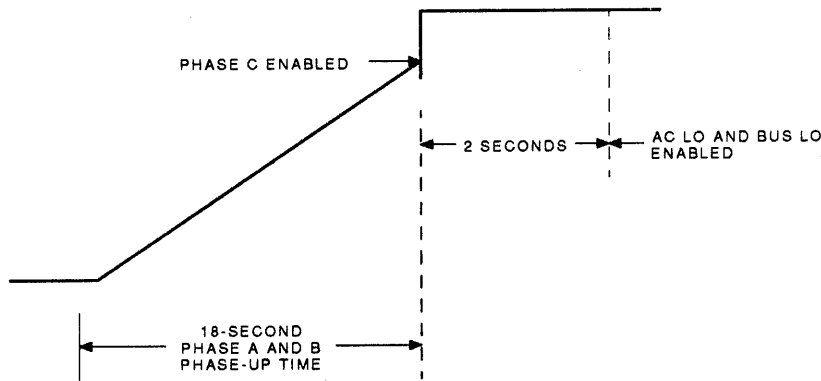
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Figure 9-17   AC LO/BUS LO Enable Timing

The dc output at the capacitor bank (DC SENSE) is monitored by the control module. DC SENSE is coupled into a set of precision voltage dividers and voltage comparators (Figure 9–18).

If the output voltage decreases below 195 Vdc (but remains above 180 Vdc), the decrease is sensed in the divider, an operational amplifier (op amp), and comparator circuits (5419471-0-1, 1-7). The AC LO optical isolator is turned on, asserting that function on the RICBUS. If the output voltage decreases below 180 Vdc, the decrease is sensed in the monitor circuits and the BUS LO optical isolator is turned on, asserting the function on the RICBUS.

If an input phase is lost, the SCRs are turned off. The output voltage decreases as the output capacitors discharge. AC LO and BUS LO are asserted (L) as the output voltage decreases beyond the respective thresholds. After a 2-second delay, the AC LO and BUS LO functions are disabled. This requires that the PFE has a minimum load specification. The minimum load specifies that the output capacitors discharge below the BUS LO level (<180 Vdc) within the 2-second delay (Figure 9–19).
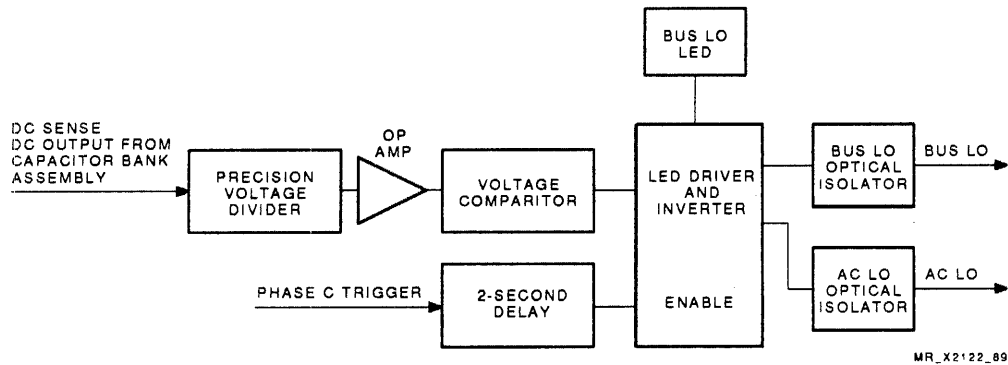
Figure 9–18   DC Output Monitor
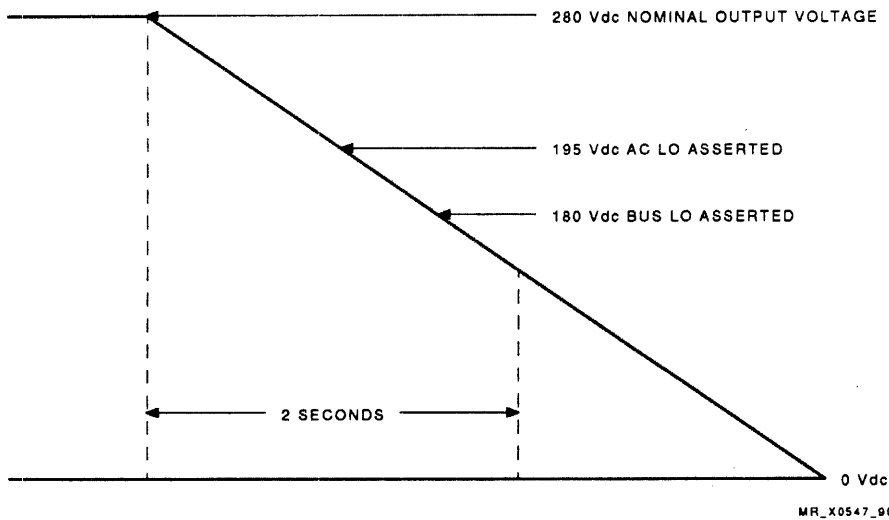
Figure 9–19   Minimum Load Specification Timing

9.5.3.5 Remote and Local Function Operation

The asserted PWR REQ (or LOCAL REQ) is applied through the isolation diode to a set of comparators (5419471, 3-7). The output of the op amp set is applied to the coil of a normally opened relay power on request (PWR ON REQ). (See Figure 9–20.)

The relay is energized, which drives a comparator. The op amp, in effect, turns on the MOD OK LED, and enables the phase A trigger (PH A TRIG) to drive the phase A SCR, and initiate the phase-up.

LOCAL and PWR REQ are applied to the same circuits. Consequently, setting the ON/OFF/REMOTE switch to the ON position asserts LOCAL with the same circuit operation as with PWR REQ, unless PWR INH is asserted.

If PWR INH is asserted, the PFE cannot be phased up because the action of the PWR INH function:

• Turns off the PWR REQ relay driver, deenergizing the relay

• Turns off the MOD OK LED

• Disables the SCR gate triggering circuits

LOCAL OFF and PWR INH are applied to the same circuits. Consequently, setting the ON/OFF/REMOTE switch to the OFF position asserts LOCAL OFF with the same circuit operation as with PWR INH asserted.
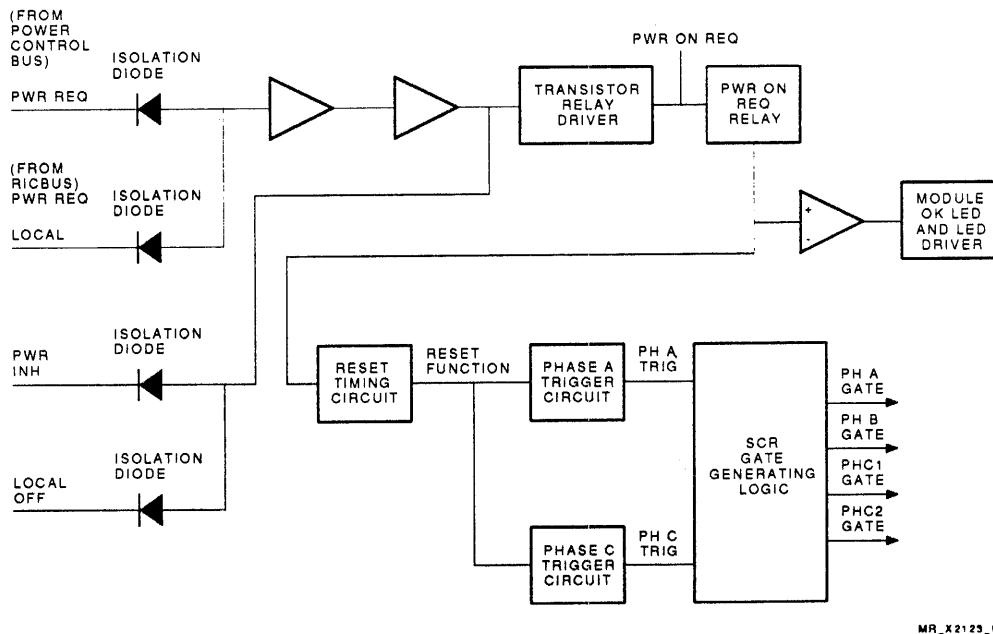
Figure 9–20   Remote Operation

9.5.3.6 Power Request Delay and Bypass

The PWR REQ or local on (LOCAL) functions can initiate a sequenced (delayed) power request (SEQ PWR REQ) to provide a delayed power request to other components of the system installation. The purpose of the delayed power request is to delay the inrush current of other system components, for example: another H7390 or disk subsystem.

As shown in Figure 9-21, an asserted PWR REQ or LOCAL function is applied through the isolation diodes to the set of comparators (5419471-0-1) to generate a PWR REQ (Section 9.5.3.5).

The output of the first op amp is coupled across an RC network to the SEQ PWR REQ comparator, which controls the SEQ PWR REQ transistor driver. The RC network provides an approximate 2-second delay between the asserted PWR REQ and the SEQ PWR REQ transistor driver. SEQ PWR REQ represents the power request to other system components and is distributed through J6 and its parallel connector J7. SEQ PWR REQ is not delayed if the PFE is off, that is, no input power or CB1 is set to off.

The power request bypass (PWR REQ BYPASS) function is used as a feed-through for the PWR REQ when the associated PFE is not used. The PWR REQ function is fed directly to the contacts of a normally closed relay (Figure 9-21).

If the PFE is not powered up, PWR REQ is passed through the relay contacts to the next power front end. However, if the PFE is powered up, the energized relay opens its contacts and interrupts the bypass path (5419471, 3-7).
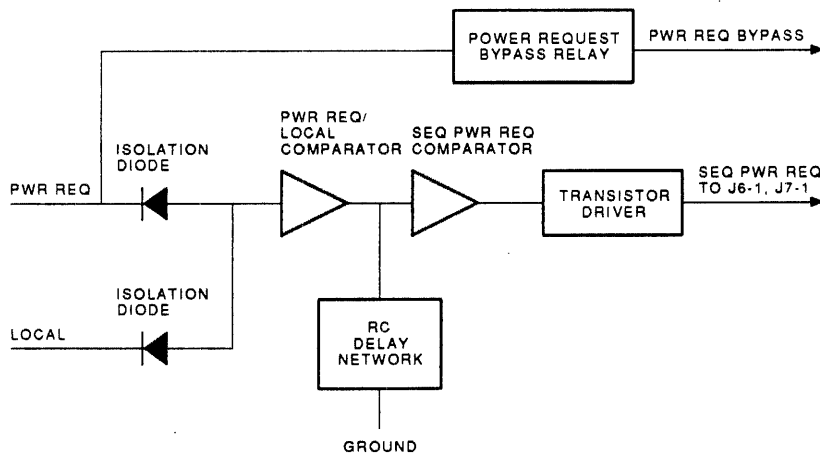
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Figure 9-21   Delayed Power Request Operation

9.5.4 Power-Down Mode

The circuits driven by PWR INH and LOCAL OFF (5419471-0-1, 3-7), or TOTAL OFF (5419471-0-1, 5-7) initiates one of the two following power-down modes:

- **Emergency shutdown (ESD)** — This mode is initiated by the detection of a thermal fault condition or a TOTAL OFF function. An ESD trips the input circuit breaker (CB1), turning the PFE off. In addition, the capacitor bank is discharged to a safe service level of 43 Vdc in a maximum of 1 minute.

- **Automatic shutdown (ASD)** — This is the normal shutdown mode that initiates a power-down sequence but does not trip the input circuit breaker CB1.

    NOTE
    The capacitor bank requires 5 minutes to discharge to the safe service level of 43 Vdc.

During all power-down sequences (AC LO, BUS LO), a ride-through capability provides the normal kernel shutdown period.

9.5.5 Ride-Through Capability

The ride-through function provided by the capacitor bank assembly allows the PFE to maintain the dc output during a momentary interruption of input power of up to 10 ms minimum. The ride-through is long enough to overcome approximately a majority of the power disturbances the PFE encounters.

With an input power interruption or sag, the control module detects the decrease in dc output voltage and effectively discharges the ride-through capacitors into the load.

As shown in Figure 9-22, the PFE encounters an ac power interruption. The T1 time represents the ride-through time during which the capacitors are discharged to maintain the dc output. (AC LO asserted at the end of T1.)
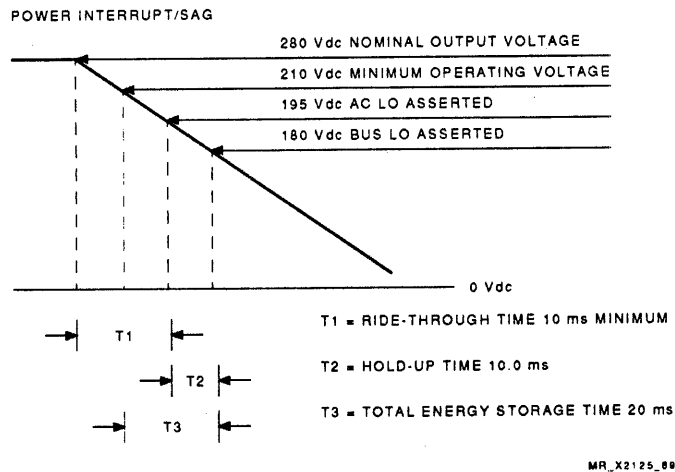
Figure 9-22   Ride-Through Function Timing

T2 is the hold-up time required to guarantee an orderly system power-down. BUS LO is asserted at the end of T2. T3 represents the minimum duration (measured in ms) of valid power.

When the PFE is initially set to on, or power is restored after a power interrupt or sag, the ride-through capacitors are recharged.

9.5.6 Safety Interlock and TOTAL OFF Functions

The safety interlock is a normally open, momentary switch, located above the controller module assembly (Figure 9–4). The switch is activated (opened) by removal of the safety bracket to access the front of the PFE.

The safety interlock and TOTAL OFF functions, and ground current are wire ORed into the shunt trip and capacitor bank fast discharge circuits. Using this input configuration allows any of the functions to shunt trip CB1 and discharge the capacitor bank (Figure 9–23).

When either TOTAL OFF is enabled, the interlock switch is opened, or the ground current exceeds 10 A ±5 A:

- The shunt trip coil transistor drivers conduct and trip CB1

- The mercury relay transistor drivers are driven into cutoff and deenergize the relay (K1), placing the 200 ohm fast discharge resistor across the capacitor bank output

Deenergizing K1 serves as a failsafe condition in the event of a power interrupt.
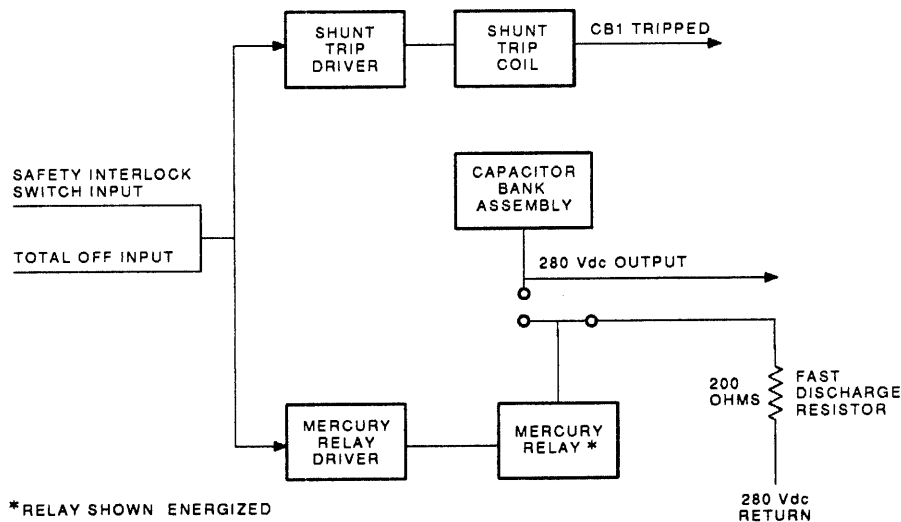
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Figure 9–23 Interlock and TOTAL OFF Circuits

The dc output is turned off (AC LO, BUS LO negated). The capacitor bank is discharged (through the fast discharge resistor) to a safe service level from a maximum of 324 Vdc to 43 Vdc. The maximum discharge period is 1 minute (worst case).

In addition, a set of four positive temperature coefficient (PTC), 8K ohm resistors are connected across each board of the capacitor bank output. During normal operation, the PTCs draw a small amount of current. When the PFE receives a PWR INH, the dc output is turned off and the capacitor bank is discharged through the PTCs.

NOTE
In this case, 5 minutes is required to discharge the capacitors to the service level of 43 Vdc.

9.5.7 Thermal Fault Detection

Two normally closed thermal switches monitor for abnormal internal temperature conditions. One switch is mounted on the SCR heat sink, while the other is located near the capacitor bank bleed-down resistors.

The heat sink switch opens at 70°C, with the closure sensed on the control module. The opened switch turns on the thermal fault optical isolator and asserts THERMAL FAULT on the RICBUS (Figure 9-24).

The bleed-down resistor switch also opens at 70°C. Should the mercury relay fail, the resistor would be permanently placed across the capacitor bank and overheat. The thermal switch will open (at 70°C), turn on the thermal fault optical isolator and assert THERMAL FAULT on the RICBUS.

THERMAL FAULT is passed over the RICBUS to the I/O RIC. The RIC initiates two actions:

- Generates a TOTAL OFF function back into the PFE that initiates an ESD

- Transmits a status message to the PEM, specifying its action
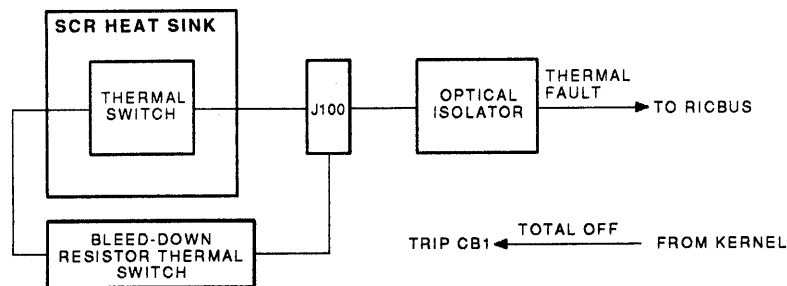
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Figure 9-24   Thermal Switch Operation

9.5.8 RIC Interface

The regulator intelligence card interface (RICBUS) provides an interface between the PFE and the PCS of the kernel system. Three of the signals are electrically isolated through optical isolators.

The RICBUS provides PFE status and error signals to the power control system (PCS) in the kernel. Signal isolation is provided by optical isolators located on the control module. The isolators are connected to the RICBUS through J6 of the module (5419471-0-1, 4-7).

Figure 9–25 shows the RIC cable connections from the control module to the RICBUS. Table 9–4 describes each RIC status signal.

Several of the RIC signals are set to a fixed logic level. The fixed levels are required to maintain compatibility with the H7392 utility port conditioner (UPC). The asserted logic levels of the compatibility signals do not cause an interrupt to the I/O RIC.

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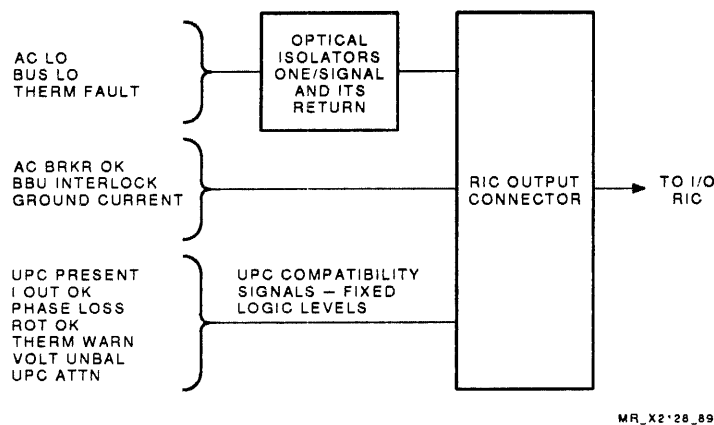
Figure 9–25   RIC Interface Connections

Table 9–4   RICBUS Description

RIC Status Line	Status Line Description
AC low (AC LO)	When asserted (L), this signal indicates that from an operating condition the ride-through energy is depleted and the bus is still within its regulation range.
	When negated (H), the line indicates that the bus is in its regulation range and the ride-through capability is restored.
Bus low (BUS LO)	When asserted (L), this line indicates that from an operating condition the hold-up energy is depleted and the bus is still out of its regulation range.
	When negated (H), the line indicates that the bus is within its regulation range and the hold-up energy is restored.
AC breaker OK (AC BRKR OK)	When asserted (L), this line indicates that the contacts on the input ac circuit breaker (CB1 A1 module) are closed.
UPC present (UPC PRESENT)	A UPC compatibility signal, fixed at a negated logic high.
Output current OK (I OUT OK)	A UPC compatibility signal, fixed at a negated logic high.
Phase loss (PHASE LOSS)	A UPC compatibility signal, fixed at a negated logic low.
Rotation OK (ROT OK)	A UPC compatibility signal, fixed at a negated logic low.
Thermal warning (THERM WARN)	A UPC compatibility signal, fixed at a negated logic low.
Thermal fault (THERM FAULT)	When asserted (L), this line indicates that a thermal fault condition exists within the PFE and it will power-down independently of any control function.
Voltage unbalance (VOLT UNBAL)	A UPC compatibility signal, and fixed at a negated logic high.
UPC attention (UPC ATTN)	A UPC compatibility signal, and fixed at an asserted logic high.
BBU interlock (BBU INTERLOCK)	A set of auxiliary contacts of CB1 are routed through the control module to the RICBUS. With CB1 and the BBU contacts closed, the RIC circuitry (in the kernel) inhibits the BBU from being enabled. With CB1 and the BBU contacts open, the kernel interlock circuit enables the BBU.
Ground current (GROUND CURRENT)	The ground current output is a measure of the current in the ground conductor. It provides an ac current proportional to the measured ac current. The ground current is coupled directly to the RICBUS.

9.5.9 Status and Fault Indication

The PFE is supplied with several status and fault indicators. Table 9–5 summarizes the visual indicators.

Table 9–5   Status and Fault Indicator Summary

Indicators	Color	Location	Description
Input ac voltage (PHA, PHB, PHC)	Red	Neon assembly, power entry assembly	Indicates the presence of primary ac input voltage.
Auxiliary output voltage (AUX OUT)	Red	Controller module assembly	Indicates the presence of the 280 Vdc auxiliary output.
BUS LO	Yellow	Controller module assembly	Indicates that the main output bus is above 190 Vdc.
Power on request	Green	Controller module assembly	Indicates that the PFE has been requested to phase up in local or remote mode.
+12 Vdc OK	Green	Controller module assembly	Indicates the presence of +12 Vdc from the external input bias voltage.
Capacitor bank OK (3)	Red	Capacitor bank assembly	Indicates the presence of voltage on the capacitor bank.

9.6 Input/Output Connectors

Table 9–6 provides a summary of the major power and control I/O connectors.

Table 9–6 I/O Connector Summary

Connector	Location	Function	Description
J1	Power entry assembly	AC input power	3-phase ac utility power input.
J2	Controller module assembly	Auxiliary 300 Vdc power output	3-phase ac auxiliary power to the kernel BBUs.
J3	Capacitor bank assembly	DC power output	280 Vdc output.
J4A	Fuse plate	Power control bus	Provides the remote power-on and power inhibit functions.
J4B	Fuse plate	Power control bus	Connected in parallel with J4A; same description.
J6	Controller module assembly	RICBUS	Provides the PFE status and alarm interface to the kernel.
J8	Fuse plate	TOTAL OFF bus	Provides the TOTAL OFF function from the kernel.
J9	Fuse plate	Delayed power control bus	Provides a 1-second delay power-on function.
J11	Top right rear cabinet component	Power line monitor connector	Provides an auxiliary output for a power line monitor.
J14	Same location as J11	Convenience outlet pair	Provides 120 V from ØC.
J15	Same location as J11	Convenience outlet pair	Provides 120 V from ØA.

10
Utility Port Conditioner Description

This chapter provides an introduction and functional description of the H7392 utility port conditioner (UPC). Included are the major physical, electrical, and environmental specifications.

10.1 UPC Overview

The H7392 UPC converts 3-phase ac input power to a regulated 280 Vdc output, with the capability to power a 20 kW load. The regulated 280 Vdc is distributed to sets of converters and air movers in VAX 9000 CPU, SCU, and XMI cabinets.

Single and dual VAX 9000 configurations require only one UPC. However, a model 440 system (quad processor configuration) requires two UPCs to support the additional CPUs. The model 440 has the capability of powering down one CPU pair, and its associated UPC, independently of the remainder of the system.

As shown in Figure 10–1, two UPCs are configured to support a model 440. Both UPCs are connected to the power input panels (PIPs) located in the IOA and IOB cabinets.

The PIP located in the IOA cabinet provides a logical OR function as well as the power interconnect. That is, with one CPU pair shutdown, the PIP directs primary dc power to the remaining CPU and its associated system components.

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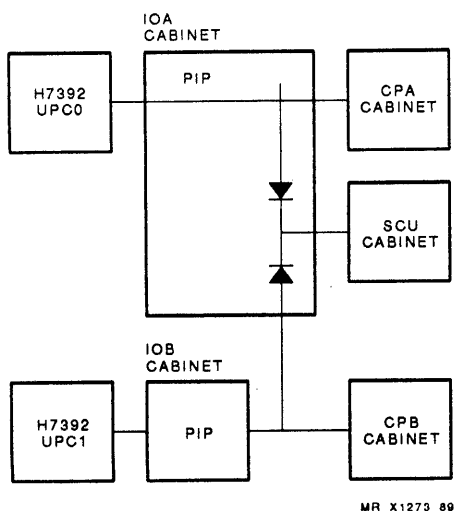
Figure 10–1   Model 440 UPC Configuration

The UPC provides reduced-harmonic rectification, high EMI suppression, and a high power factor. The UPC can be controlled at the unit, or remotely through the service processor unit (SPU). UPC operational and environmental status are also monitored by the SPU through the kernel power control subsystem (PCS).

DC voltage regulation is maintained using a pulse width modulation (PWM) technique. Using the ride-through capability, the UPC can maintain the dc output for a short period (<100 ms) in the event of an interrupt to the ac input power.

10.2 UPC Characteristics

This section provides an introduction and overview of the UPC characteristics. Included are the major physical, electrical, and environmental specifications.

10.2.1 Physical Overview

As shown in Figures 10-2 and 10-3, the UPC is housed in a custom-designed cabinet (similar to a VAX-11/780 cabinet). The UPC components, assemblies, and modules are assembled into two bays. Printed circuit boards (PCs) are also mounted on the assemblies as well as on panels in the bays.

NOTE
The term *module* here differs from the traditional Digital definition. The UPC module definition includes: PCs, rack-mounted assemblies with discrete components, and rack-mounted assemblies with discrete components and one or more PCs.
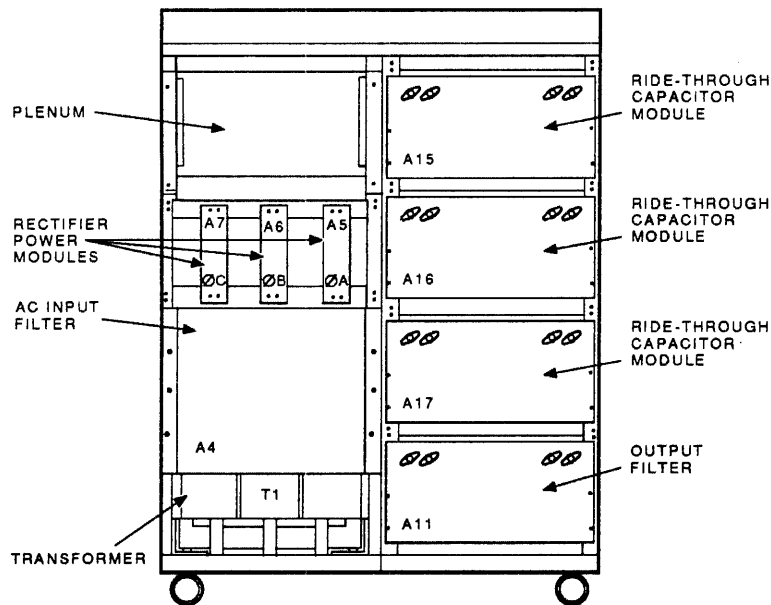
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Figure 10-2   Basic UPC Cabinet Component Layout (Front Doors Open)

RIDE-THROUGH CHARGE RESISTOR
RIDE-THROUGH SWITCH
HIGH VOLTAGE ATTENUATOR PC15
SYSTEM CONTROL PCB
RIDE-THROUGH RECOVERY
RIDE-THROUGH DISCHARGE RESISTOR
FAST DISCHARGE
PWM POWER MODULES
COOLING FAN ASSEMBLY
24 V ON/OFF SWITCH
+24 V POWER SUPPLY MODULE
AUXILIARY POWER MODULE
AUXILIARY POWER BREAKER
PLDM BREAKER
LOCAL/REMOTE SWITCH
CONNECTOR PANEL
LED ALARM PANEL
PWM CONTROL PCB
INPUT BREAKER ASSEMBLY
INPUT BREAKER
OUTPUT FILTER
AC INPUT
DC OUTPUT
PDLM
AUXILIARY POWER
POWER CONTROL BUS
RICBUS
ALARM RESET
AC ON INDICATOR

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Figure 10-3   Basic UPC Cabinet Component Layout (Rear Doors Open)

10.2.2 Physical Specifications

The UPC is contained in a custom-designed cabinet with the physical specifications listed in Table 10-1.

Table 10-1   Physical Specifications

Parameter	Specification
Height	152.4 cm (60.0 in)
Width	115.6 cm (8.5 in)
Depth	76.2 cm (30.0 in)
Gross weight	873.2 kg (1925 lb) including shipping crate
Unit weight	816.5 kg (1300 lb)

10.2.3 Electrical Specifications

The UPC can be configured in two nominal operating sources: 208 V rms source and 380/416 V rms source.

H7392-AA, nominal 208 V rms, 60 Hz:

* 208 V rms nominal line-to-line: 159 to 229 V rms, 3-phase delta, 3-wire without neutral, at a nominal 60 Hz.

* 202 V rms nominal line-to-line: 220 V rms (Japan). Internal switch must be configured for correct frequency.

NOTE
The 202 V nominal source may be used in Japan.

H7392-AB, nominal 380/416 V rms, 50 Hz:

* 380 V rms nominal line-to-line: 303 to 418 V rms, 3-phase wye, 5-wire at 55 A rms maximum.

* 416 V rms nominal line-to-line: 327 to 457 V rms, 3-phase wye, 5-wire 51 A rms maximum.

NOTE
Both H7392 -AB versions are factory-set to operate at 50 Hz.

All versions are configured as delta-connected loads. Except Japan, all areas where a wye source is available, a 5-wire connection should be provided. This provision allows for future equipment upgrades. Table 10–2 provides additional major electrical specifications.

Table 10–2 Electrical Specifications

Parameter	Specification
Output voltage deviation	±14 Vdc
Minimum power factor	0.87 at full lead
DC power output	20 kW
Minimum efficiency	90%
Maximum harmonic distortion	5%

10.2.4 Environmental Specifications

Table 10–3 provides the major environmental specifications.

Table 10–3 Environmental Specifications

Parameter	Specification
Operating temperature	15–32°C (59–90°F)
Nonoperating temperature	Low limit = -40°C (-40°F) and 50% relative humidity
	High limit = 66°C (151°F) and 96% relative humidity
Operating relative humidity	20–80% with maximum bulb temperature of 20°C (77°F) and minimum dew point of 2°C (31°F), based on operation at sea level
Operating altitude	2.4 km (8,000 ft)
Nonoperating altitude	4.8 km (16,000 ft)

10.3 Functional Overview

As shown in Figure 10–4, the UPC consists of several major functional units (blocks). The overview introduces and correlates the functions of each functional unit and the related modules identified in Figures 10–2 and 10–3.
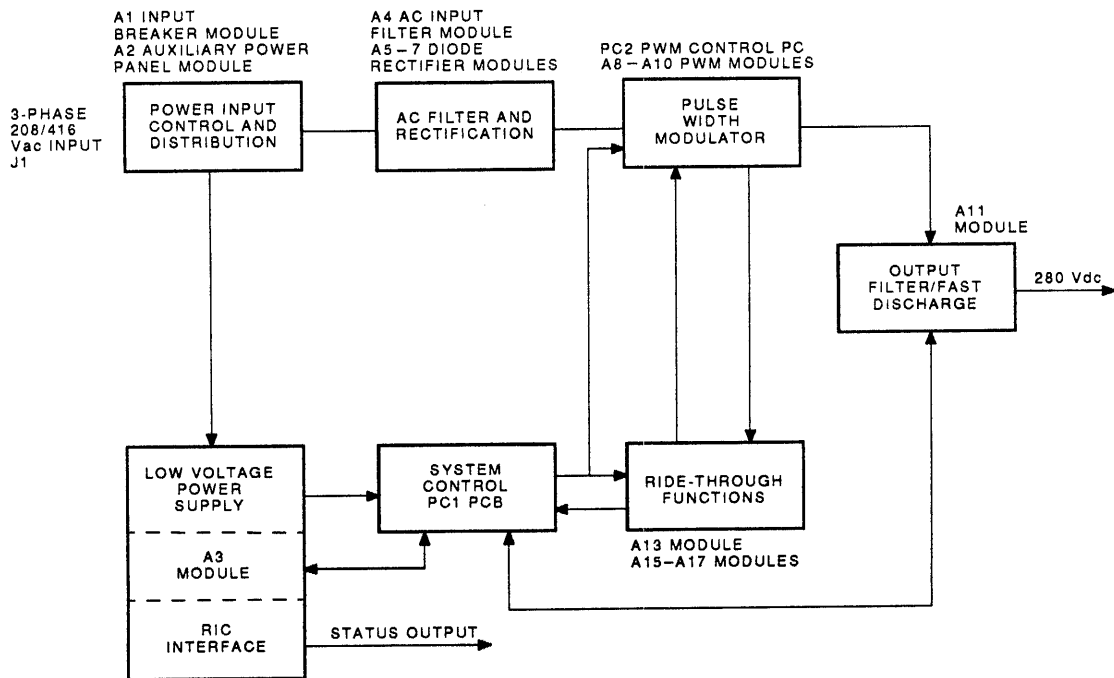
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Figure 10–4 Basic UPC Functional Block Diagram

10.3.1 Power Input Control and Distribution

The power input control and distribution functional unit provides the UPC on/off control through a high capacity circuit breaker. The unit distributes ac voltage to the main UPC power transformer, power control bus (DEC power bus), and the VAX 9000 BBUs. In addition, the unit supplies ac power to the A3 24 V power supply module used for the control and interface circuits.

The 3-phase ac input power (200 Vac line-to-line or 400 Vac line-to-line) is applied to the power input control and distribution block (Figure 10–4). This functional unit block represents the input breaker module A1, auxiliary power panel module A2, and main power transformer T1 (Figure 10–3).

A1 output power is distributed to:

- The input power transformer (T1) through the main circuit breaker of module A1 (Figure 10–3)

- The power control bus through module A2

- Module A3, low voltage power supply (bias supply)

A1 also contains a current transformer to monitor the UPC and kernel ground current, as well as providing EMI filtering.

The input power transformer (T1) consists of a delta-wound transformer primary. The secondary windings convert the 3-phase ac input to 3 single-phase outputs (phase A [ØA], phase B [ØB], and phase C [ØC]). Auxiliary secondary windings on T1 provide 3-phase output power through A2 to the kernel BBUs and UPC fan assemblies. In addition, the transformer is electrostatically shielded to reduce EMI and common mode noise.

10.3.2 AC Filter and Rectification

The ac filter and rectification functional unit represents the ac input filter module A4 and the three diode rectifier modules: A5 (ØA), A6 (ØB), and A7 (ØC) (Figure 10–2).

The A4 module provides the ac filter networks for each output phase of T1. The filter networks prevent input power disturbances from affecting UPC operation by attenuating input line EMI and transients.

The networks also prevent UPC power converter switching pulse width modulator ([PWM] ripple) from being coupled back into the utility. The networks reduce the PWM ripple by working with the T1 secondary winding leakage inductance.

In addition, a high voltage attenuator module reduces each phase of the filter output to a level compatible with the low voltage UPC control and monitoring circuits of the system control module (PC1).

Each diode rectifier module (A5 through A7) is protected by a high capacity fuse and contains a full wave rectifier and an additional filter. The output of the rectifiers are full-wave rectified with no dc filtering.

The rectified dc output current of each phase is passed through an associated current sensor. The sensor measures the rectifier output current to control the UPC input current, and provides input power overload protection.

10.3.3 Pulse Width Modulator

Each phase of a diode rectifier module output is applied to a PWM module through an associated choke (L4 [ØA], L5 [ØB], L6 [ØC]).

The functional unit blocks represent the PWM modules A8 (ØA), A9 (ØB), and A10 (ØC) (Figure 10–3). The PWM module output provides a regulated output over a wide range of ac input voltage and dc output voltage. During normal UPC operation, the PWM converters are programmed to draw ac input current. However, in ride-through mode, the converters draw dc current from the ride-through capacitors.

The PWM modules perform two major functions: wave shaping and amplitude control.

- Wave shaping controls the input current, to conform to the wave shape of the incoming voltage. This eliminates rectification harmonics.

- Amplitude control, controls the amplitude of the incoming current based on the output dc voltage. This provides output regulation.

A PWM module is a combination of power switching devices that can be turned on and off (modulated) by its associated drive and control circuits. Three base driver modules (PC4, PC5, PC6) provide the interface functions between the switching devices and the timing and driver controls located on the PWM rectifier control module (PC2).

Each PWM module operates with one of the PWM chokes (L4 through L6). The chokes provide the energy storage required to implement controlled power conversion by power switching techniques.

10.3.4 Ride-Through Unit

The ride-through unit and its control logic provides the capability to maintain the dc output during a momentary interruption of input power up to 100 ms. The ride-through time is long enough to overcome approximately 95% of the power interrupt problems the UPC encounters.

The ride-through unit block consists of several banks of high-capacitance electrolytic capacitors in modules A15, A16, and A17, and are charged to the full dc output.

With an input power interruption, the ride-through control logic — contained in A13 on PCs PC7, PC8, and PC16 — initiates the discharge of the capacitors. The discharge path is through the PWM module, which provides regulation during the ride-through period.

In Figure 10–5, the UPC encounters an ac power interruption. The T1 period represents the ride-through time during which the capacitors are discharged to maintain the dc output. (AC LO is asserted at the end of T1.)

T2 is the hold-up period required to guarantee an orderly system power-down. (BUS LO is asserted at the end of T2.) T3 represents the duration (measured in µs) of valid power remaining following completion of the power-down time (T2). Also included are the fast discharge and recovery circuits. These circuits control the discharge and recharge of the ride-through capacitors, and the discharge of the filter and load capacitors.

AC POWER INTERRUPTION

AC LOSS SENSE

AC LO ASSERTED

T1

POWER VALID

BUS LO ASSERTED

T2

DC POWER

LOWER DC POWER
OUTPUT LIMIT – 161 Vdc

T3
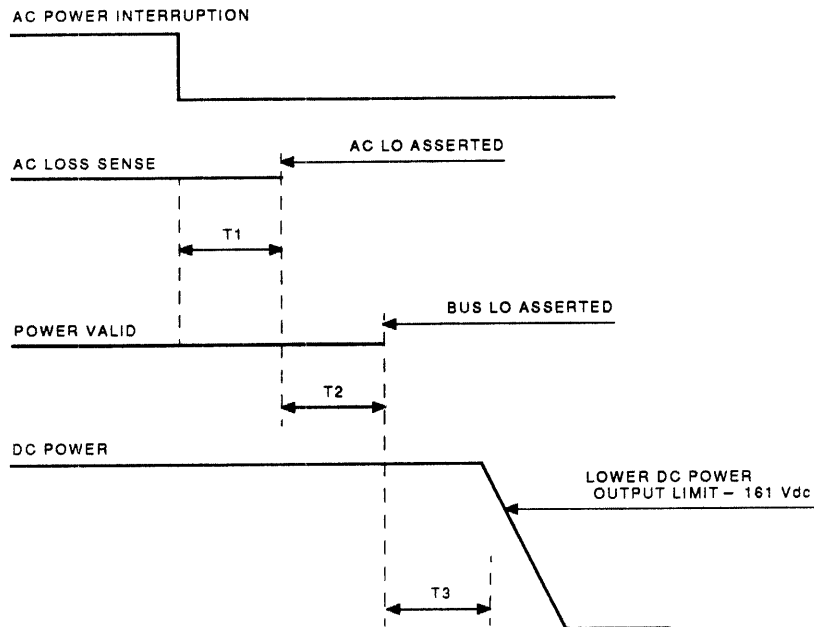
WHERE: T1 = TIME TO DETECT AC POWER INTERUPT (AC LO ASSERTED AT END OF T1)

T2 = TIME PROVIDED FOR ORDERLY POWER-DOWN (BUS LO ASSERTED AT
      END OF T2)

T3 = HOLD-UP TIME — DURATION OF VALID POWER REMAINING FOLLOWING
      COMPLETION OF THE POWER-DOWN (T2)

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Figure 10–5   Ride-Through Timing

The ride-through switch of PC7 is enabled when the ac input falls below the minimum voltage of 161 Vac. The switch discharges the ride-through capacitors through the PWM module (to maintain regulation), the output filter, the optional disconnect switch (if installed), and into the load.

When the UPC is initially set to on, or power is restored after a power interrupt, the ride-through recovery module (PC16) controls and provides a fast capacitor charging rate. With the UPC set to off, the fast discharge module (PC8) provides a discharge path for the ride-through and final output filter capacitors.

Indicators are included to verify that the circuit is operational, and that the voltage is discharged to a safe servicing level.

10.3.5 Output Filter and Disconnect Switch

The output filter and disconnect switch includes the final dc output filter network and optional output disconnect switch. The functional unit block represents the final dc output filter (A11 module) and the output disconnect switch (A12 module).

The output filter provides the common phase connection point and the final dc filter network that removes residual ripple. The filter module also contains a current sensor to monitor the output current. The sensor output is coupled into the output overload monitor circuit on the system control module.

The optional output switch provides a high-capacity circuit breaker and additional RFI filtering.

10.3.6 Low Voltage Power Supply

AC power from the A1 module is distributed to the low voltage dc power supply (A3 module). The supply provides a nominal, unregulated 24 V output that provides the required dc voltages for the UPC control and logic circuitry. The module is equipped with a self-contained, ride-through capability in the form of a set of fused, electrolytic capacitors.

The A3 module also provides the regulator intelligence card (RIC) bus interface. The RIC interface is isolated from the power control subsystem (PCS) of the kernel and routes the status and fault functions from the UPC to the PCS.

10.3.7 System Control

The majority of UPC control, and status and fault monitoring, is provided by the system control module (PC1). PC1 provides the UPC on/off and the ride-through initiation. It also provides the following general functions:

* Current monitoring, input current control, output regulation

* Operational status monitoring and related LED indicators

* Fault and error detection and related LED fault indicators

* Power-up, -down, and sequencing functions

The power-down functions consist of the three power-down sequences based on the following general UPC conditions:

* **Automatic shutdown (ASD)** — This is the normal shutdown sequence.

* **Immediate shutdown (ISD)** — A sequence initiated based on the detection of any one of a set of severe error conditions. Following power-down (including ride-through), the main UPC circuit breaker is automatically tripped.

* **Emergency shutdown (ESD)** — A power-down based on the detection of any one of a set of fatal errors. On error detection, the main UPC circuit breaker is immediately tripped, turning off the dc output and inhibiting the ride-through operation.

PC1 also contains an isolated power supply that provides the regulated +12 Vdc and -12 Vdc for the control and monitor circuits.

10.4 Functional Description

This section provides a detailed functional description of the UPC and its operations. Figure 10–6 presents the overall system block diagram. All other block diagrams are expansions of individual system blocks.

10.4.1 Block Diagram and Text Notations

As an aid to correlating the functional description and its block diagrams with the schematic drawings, the text and functional block diagrams reference the related schematic drawing and sheet numbers wherever practical. Where practical, connector and pin numbers are referenced on the block diagrams. Major signal names and their mnemonics are also included in the text.

Diagrams and text references use the following notation:

- Schematic and sheet number references use the form: (454388100, 2-7), and are read as: schematic number 454388100, sheet 2 of 7.

- Connector references use the form: (J10-17), and are read as: connector J10, pin 17.

- Signal names include full titles with the mnemonics in parenthesis: input breaker trip function (INPUT BRKR TRIP).

10.4.2 Input Breaker Module (A1)

The A1 input breaker module contains the main UPC input circuit breaker (CB1), which serves as the main power switch (Figure 10–7). The 3-phase ac utility power is applied to the line (input) side of CB1. The line side of the breaker also provides power to the step-down transformer in the A3 module.

NOTE
Although CB1 may be set to off (open), ac power remains applied to the A3 module, which supplies 24 Vdc to the control circuits.

The load (output) side of CB1 is passed through a set of filter capacitors to attenuate high frequency interference, and is applied to the:

- Primary of the main power transformer (T1)

- Auxiliary power module A2 for the external power line monitor (J11)

Incorporated into the CB1 assembly are a set of auxiliary switch contacts and a shunt trip coil. The auxiliary switch contacts, which operate with the main contacts, are used in the UPC and the kernel to indicate CB1 status, and for BBU control.

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DC
OUTPUT

| A12 OUTPUT DISCONNECT SWITCH |
| PC8 FAST DISCHARGE MODULE |

| A11 DC OUTPUT FILTER |
| RIDE-THROUGH RECOVERY MODULE PC16 |
| A15–A17 RIDE-THROUGH CAPACITORS |

| A8–A10 PWM POWER MODULES |
| RIDE-THROUGH SWITCH MODULE PC7 |

| A5–A7 DIODE MODULES |

| A4 AC INPUT FILTER |

BBU POWER J2
AUXILIARY AC POWER J2
LINE MONITOR J11

| T1 INPUT POWER TRANSFORMER |
| A2 INPUT BREAKER ASSEMBLY |

PWM MODULE CONTROL J1, J3, J5
RIDE-THROUGH SWITCH CONTROL J2

UPC CONTROL

| PC2 PWM CONTROL   J9   J8 |
| PC1 SYSTEM CONTROL |
| J8   J4   J1   J5 |

RIC, J10

POWER CONTROL BUS, J4
TOTAL OFF BUS, J4

| A1 INPUT BREAKER MODULE |
| A3 MODULE 24 V POWER SUPPLY |
| RICBUS |

AC INPUT

Figure 10–6   UPC System Block Diagram
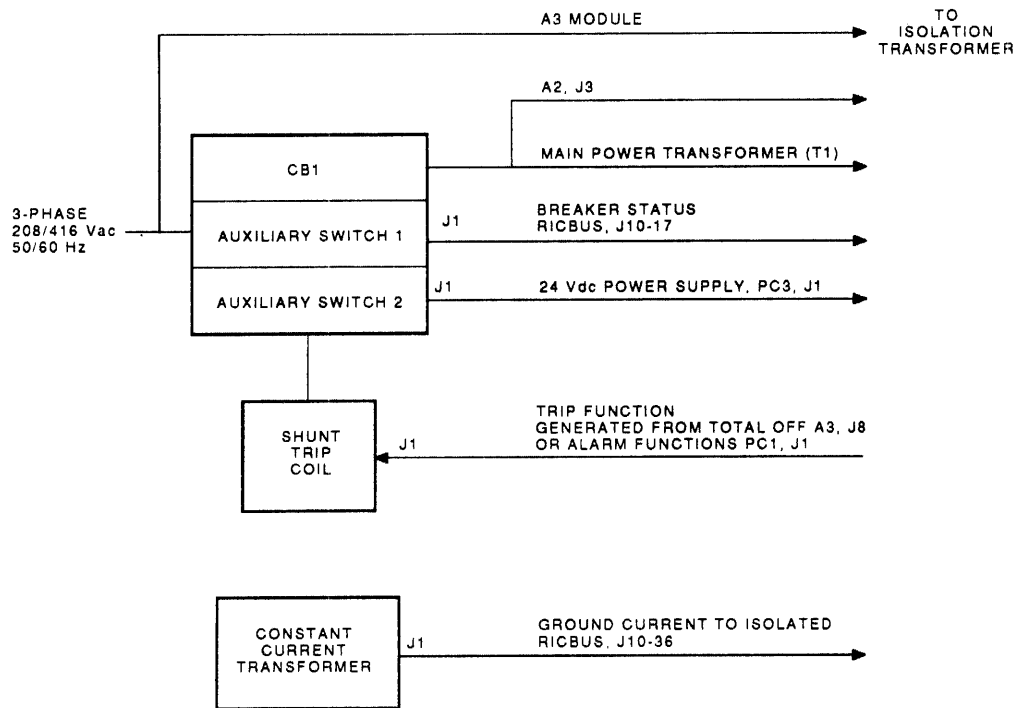
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Figure 10-7   Input Breaker Module (A1)

10.4.2.1 Remote Trip Capability

The shunt trip coil provides circuit breaker trip capability. CB1 can be remotely tripped (off). The trip capability disconnects the UPC from the input utility in the event of internal UPC faults or external kernel faults (Figure 10-7).

The shunt trip coil is activated from a power amplifier located on the rectifier supply and power control module (454408100, 2-2). When energized, the shunt coil will trip CB1 off in approximately 10 ms.

The trip coil is activated through one of the following:

- TOTAL OFF BUS, which turns on the power amplifier, on PC3 of the A3 module (454408100, 2-2), driving the trip coil and setting CB1 of the A1 module to off

- Through the emergency alarm detection logic on PC1 (454388100, 2-7), which generates the input breaker trip function (INPUT BRKR TRIP) to enable the optical isolator and turn on the power amplifier, tripping CB1

When tripped off, CB1 must be manually set to off and then reset to on. With CB1 tripped, the shunt trip coil is opened to prevent the high trip current from overheating the coil.

10.4.2.2 Ground Current Monitor

The A1 module also contains a ground current monitor. The monitor detects unacceptable UPC or system ground currents due to incorrect system grounding or major leakage between the power circuitry and chassis ground. The ground current monitor is a current transformer (CT1) with a frequency response of 50 Hz to 10 kHz, and is capable of sensing a continuous 5 A input.

The UPC chassis ground is routed through CT1 and serves as the transformer primary. The CT1 secondary consists of 200 turns generating a secondary current equal to the ground current divided by 200. The expected ground current level is in the order of 100 to 300 mA.

The transformer is terminated by less than 2 ohms resistive. Two diodes connected across the transformer secondary (in opposite polarity) prevent damage if the termination resistor is disconnected during operation. Ground current is coupled to the kernel system through the isolated RIC interface to J10.

10.4.3 Auxiliary Power Module (A2)

The A2 auxiliary power module contains the circuit breakers and connectors for distribution of unswitched power, and for the power distribution line monitor (PDLM). The A2 module receives 3-phase 120/208 Vac from a set of auxiliary secondary windings of T1, and 208/416 Vac from the primary of T1 (Figure 10–8).
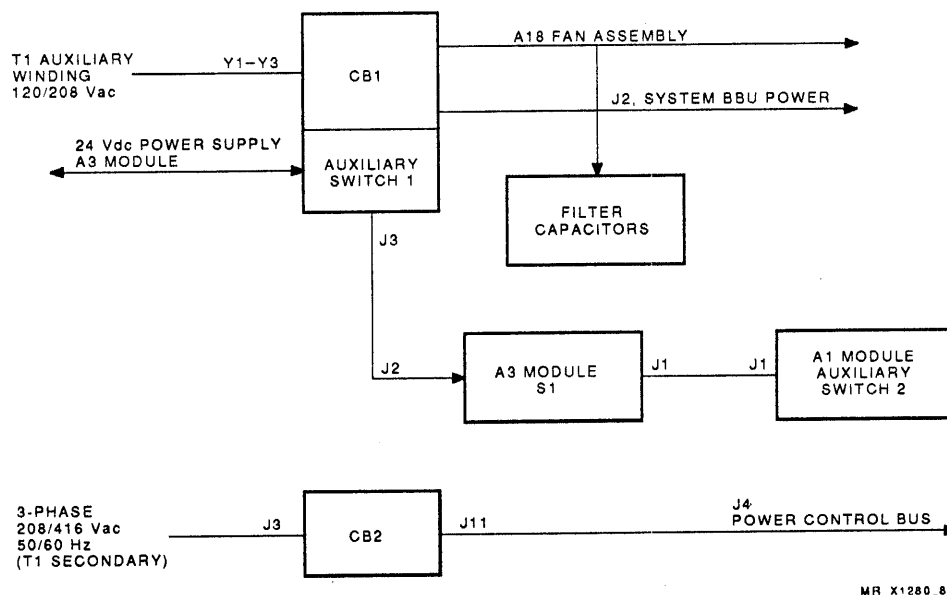
Figure 10–8   Auxiliary Power Module (A2)

A2 controls the distribution of the 120/208 Vac unswitched power through CB3 for the kernel BBUs and UPC fans. A set of filter capacitors connected across the unswitched power output attenuate any high frequency interference entering or exiting the UPC at this point.

The 208/416 Vac power is controlled through CB2 to switch the voltage monitor lines to the power disturbance line monitor (PDLM) connector J11. The auxiliary switch contacts of CB1 are wired in series through the:

* Auxiliary switch 2 contacts of CB1 on the A1 module

* LOCAL/REMOTE rotary switch on the A3 module

This switch loop provides a system interlock circuit to indicate normal operational status.

10.4.4 Rectifier Supply and Power Control (A3)

The A3 module contains two additional modules: rectifier supply and power control (PC3), ride-through capacitor PC (PC17), as well as the step-down transformer (Figure 10–9). The PC3 and PC17 provide several control and interfacing functions, two power supplies, and a ride-through capability.

10.4.4.1 24 V Supply and Power Control

The ac from the A1 module is applied to the 3-phase, step-down transformer (T1) (698000473, 1-1). T1 reduces the input to approximately 25 Vac for use by the control circuits (Figure 10–10). Two versions of the step-down transformer are required to accommodate the 200 V or 400 V UPC models.

Fuses (F1 through F3 on the A1 module) protect the transformer input lines and clear in case of a major fault or failure in the UPC controls. However, these fuses would not normally clear in the event of a minor fault in the control circuits.

The 3-phase voltage from the T1 transformer secondary is applied to the 24 V rectifier circuit (454408100, 1-2). Surge suppressers in the rectifier attenuate input transients. Monitor resistors (R22 through R24) couple the T1 secondary voltage (as signals ØA MON, ØB MON, ØC MON) to the system control module (PC1) to monitor for phase loss, rotation, and overvoltage faults.

The phase signals are coupled to error detection circuits and identify phase loss and phase rotation faults. The fault signals are coupled through optical isolators to the RICBUS as phase loss (PHASE LOSS) and rotation OK (ROT OK).

A LED (DS1) is connected across the rectifier output and indicates that ac power is applied to the UPC power cable. The LED (AC ON) is located on the connector panel and is visible with the cabinet doors closed.

NOTE
Since the 24 V power supply can operate on single-phase ac power, a lit LED does not necessarily indicate that 3-phase power is available, or within specifications. Usually, the UPC will not operate on one phase.
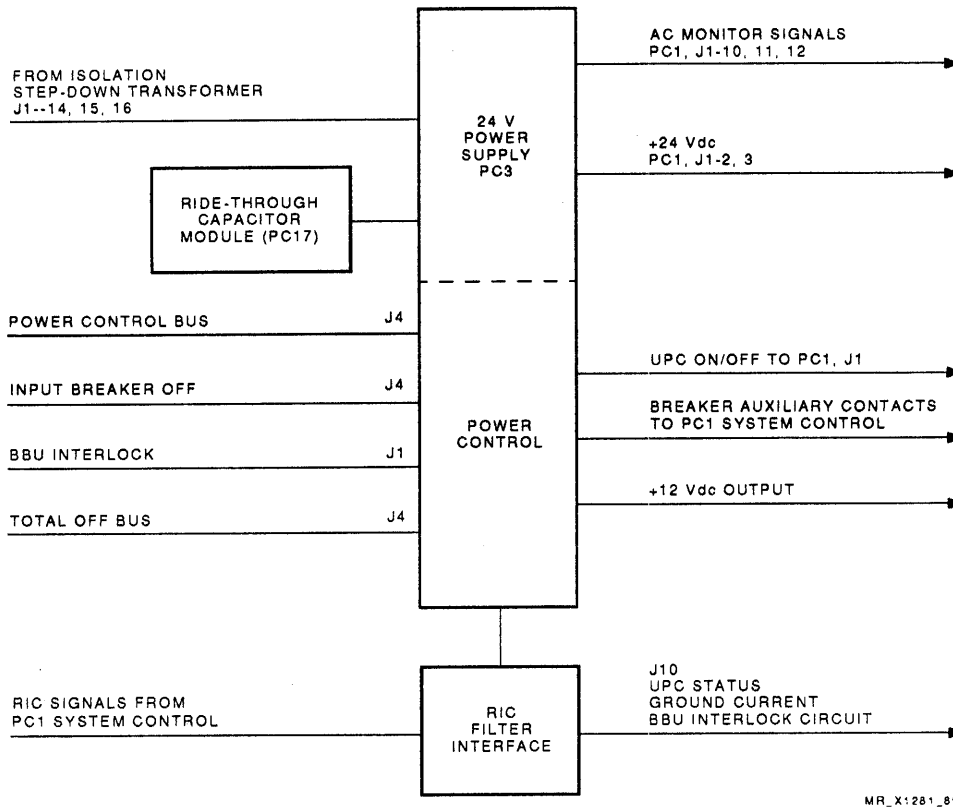
Figure 10-9   Basic Rectifier Supply and Power Control (A3)
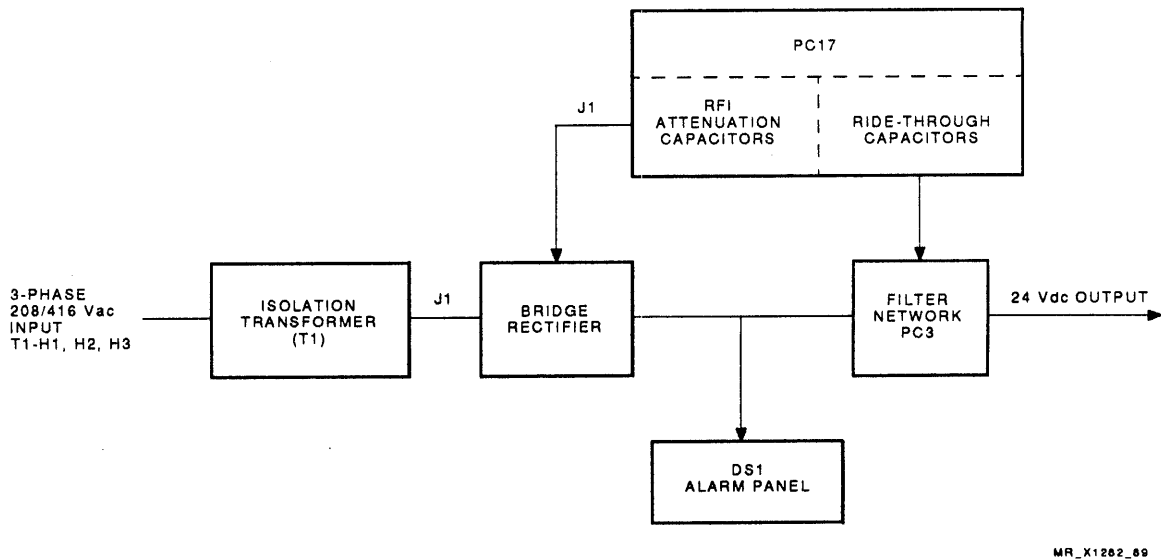
Figure 10-10   24 V Power Supply

The rectified dc is applied to a network of electrolytic capacitors that provide filtering as well as redundancy. Each filter capacitor on PC3 is equipped with a series fuse and resistor. The fuse enables a capacitor to fail and be cleared from the +24 Vdc output bus without causing an unacceptable dip in the bus voltage.

The capacitors are provided with a fuse failure detector circuit. If a fuse is blown, a LED (RECT FUSE) located on the system control module is turned on.

A series resistor limits the fault current during fuse clearing, and the inrush current during the ac input turn-on. The resistor also limits the rectifier peak current during normal rectification.

PC3 includes an electrolytic capacitor and associated components used to supply energy storage for the shunt trip coil of the main ac input circuit breaker (CB1 [A1]). The capacitor supplies approximately 5 A for 10 ms to trip CB1. If the capacitor fails to charge up to a 24 V level due to a faulty capacitor or abnormal loading of the shunt trip circuit, this fault condition is coupled to a LED on the alarm panel of the system control, PC1.

A ride-through capability is provided by the capacitors contained on the ride-through capacitor module (PC17). PC17 also contains a set of filter capacitors connected across the isolation transformer secondary that provide RFI attenuation.

10.4.4.2 12 V Isolated Power Supply
Since the power control bus circuits must be electrically isolated from other UPC circuits, a transformer-isolated switching power supply was incorporated into PC3 (454408100, 2-2). The 24 Vdc from the rectifier supply is applied to a semiconductor voltage regulator, which provides a regulated 15 Vdc (Figure 10-11).

The 15 Vdc output is applied to an oscillator and frequency divider combination. The divider produces two complementary square waves that drive a small toroid isolation transformer. The transformer provides isolation between the power control bus circuits and the UPC circuit ground system. The transformer secondary output is applied to a full wave rectifier and filter, which produces +12 Vdc for the power control bus control circuits.

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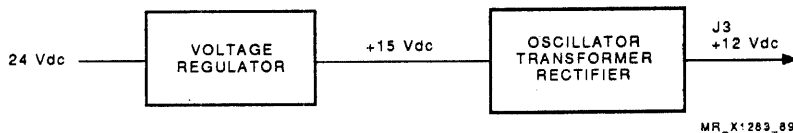
Figure 10-11   12 V Isolated Power Supply

10.4.4.3 Remote/Local Operation

Remote and local operation is controlled through the REMOTE/LOCAL switch located on the front panel of the A3 module.

The power control bus is applied to the control bus interface (J4) to provide remote operation. With the power request (PWR REQ) asserted and the REMOTE/LOCAL switch set to REMOTE, the logic effectively enables the output optical isolator (Figure 10–12). The optical isolator output enables the UPC on function (454408100, 2-2).

With the optical isolator on, the UPC becomes operational if no other interlocks or alarms prevent operation. With the optical isolator off, no operation of the UPC is possible. The UPC on/off function is controlled by the following conditions:

* If PWR INH (power control bus) is asserted (logic low), the UPC cannot be commanded on since the action of the PWR INH logic essentially inhibits turning on the UPC on/off optical isolator.

* If the REMOTE/LOCAL switch is in the REMOTE position, the PWR REQ function can turn the UPC on and off, unless the PWR INH or the power supply fail circuit inhibits operation.

* If the REMOTE/LOCAL switch is in the off position, the optical isolator drive is disabled and UPC operation is inhibited.

* If the REMOTE/LOCAL switch is in the LOCAL position, the optical isolator drive is enabled and the isolator turns the UPC on, unless PWR INH is asserted or the power supply fail circuit inhibits operation.
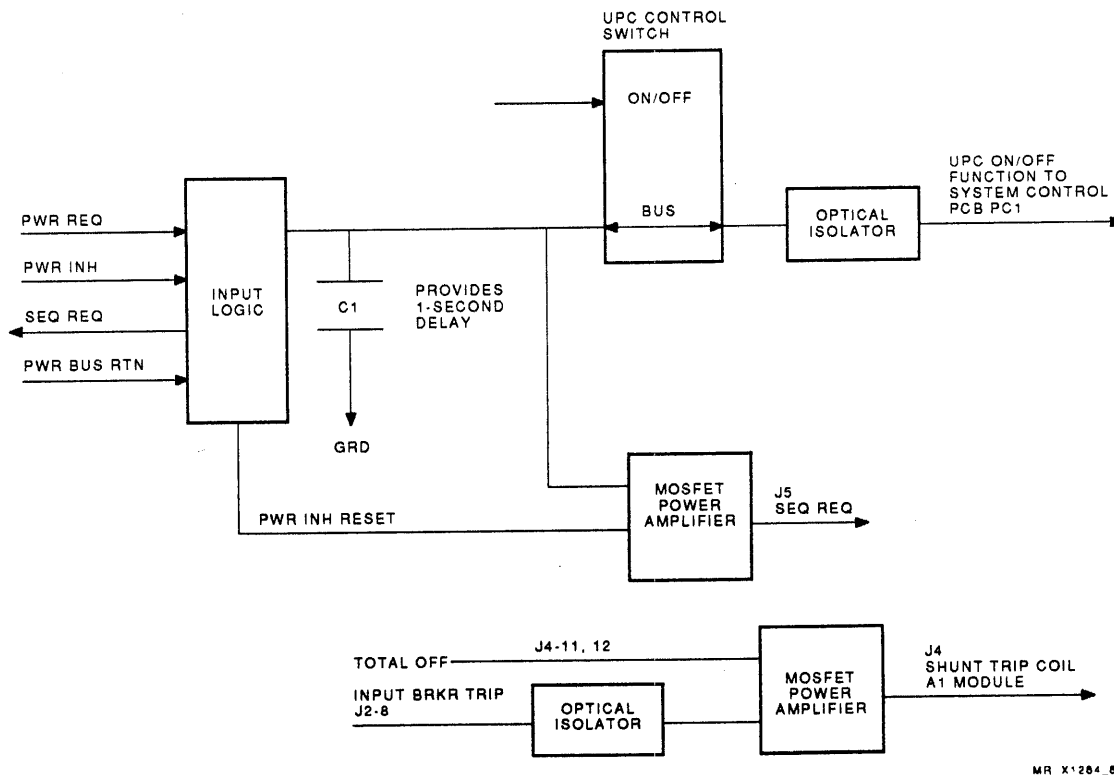
Figure 10–12   Remote Operation

The PWR REQ input may also be used to generate a delayed power request or sequenced request (SEQ REQ) and provide a delayed startup signal for other components of a system installation.

The basic circuit components consist of an RC network and a MOSFET (454408100, 2-2). With PWR REQ asserted, the RC network provides a nominal 1-second delay before the MOSFET is turned on. With the MOSFET conducting, it acts as a solid-state switch between SEQ REQ and PWR BUS RTN (power control bus return) for delayed power control bus output.

An isolated interlock of the PWR INH and the SEQ REQ with the UPC ac input breaker is provided through an optical isolator and the MOSFET switch. If the ac input breaker (CB1) is off, current flows in the input of the optical isolator, which turns on its output transistor. Turning on the transistor disables the SEQ REQ signal and sets PWR INH to a logic low.

A second set of contacts on the UPC REMOTE/LOCAL switch provides a BBU interlock function. In the off position, the circuit is open; in the LOCAL and REMOTE positions, the circuit is closed.

If the isolated 12 V power supply fails:

>   SEQ REQ is inhibited
>   PWR INH is asserted
>   UPC operation is inhibited

The UPC on function is monitored on the alarm panel of PC1. If the function is disabled, the UPC on LED will be on.

The drive circuits for the shunt trip coil of CB1 (module A1) are contained on PC3 (Figure 10-12). The power amplifier to drive the trip coil is comprised of a MOSFET amplifier and related circuit components. The MOSFET amplifier allows the breaker shunt trip to be actuated with a momentary (at least 1 ms) application of a short circuit across the TOTAL OFF function input.

The shunt trip coil of CB1 may also be actuated by internal shunt trip signals. The input breaker trip function (INPUT BRKR TRIP) is applied to an optical isolator (454408100, 2-2). The isolator simulates the same input to the MOSFET amplifier as the TOTAL OFF function. The amplifier drive trips the shunt coil.

10.4.4.4 RIC Interface

The regulator intelligence card (RIC) interface (located on the A3 module) provides an electrically isolated interface between the UPC and the kernel system. The RIC interface provides control and status functions between the UPC and the kernel system. Signal isolation is provided by optical isolators. The isolators are connected to J10 (454398100, 2-2).

Figure 10-13 shows the RIC cable connections from PC1 to the RIC interface board and the common mode baluns (454398100, 1-2 and 2-2).

The RICBUS provides UPC status signals to the power control system (PCS) in the kernel. Table 10-4 describes each RIC status signal.
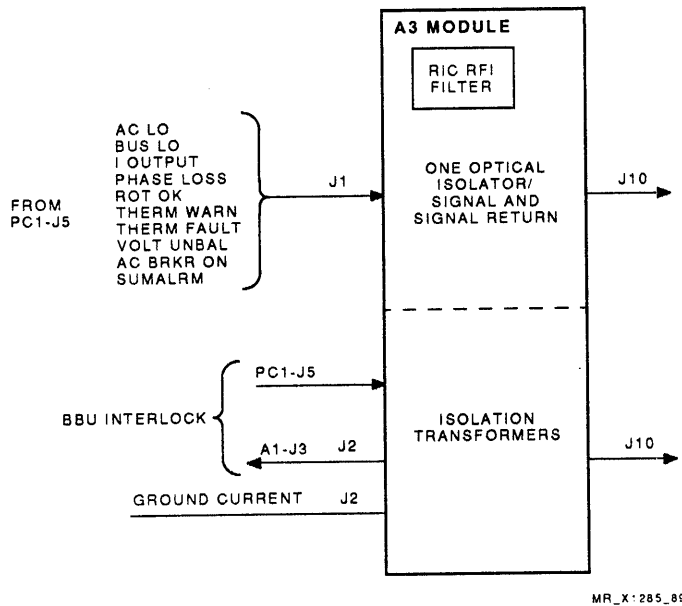
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Figure 10-13   RIC Interface Connections

Table 10-4   RICBUS Status Line Description

RIC	Description
AC low (AC LO)	When asserted (L), this signal indicates that from an operating condition the ride-through energy is depleted and the bus is still within its regulation range.
	When negated (H), the line indicates that the bus is in its regulation range and the ride-through capability is restored.
Bus low (BUS LO)	When asserted (L), this line indicates that from an operating condition the hold-up energy is depleted and the bus is still in its regulation range.
	When negated (H), the line indicates that the bus is within its regulation range and the hold-up energy is restored.
AC breaker OK (AC BRKR OK)	When asserted (L), this line indicates that the contacts on the input ac circuit breaker (CB1 on the A1 module) are closed.
UPC present (UPC PRESENT)	An installed UPC provides a pin-to-pin short circuit indicating that a UPC is present.
Output current OK (I OUT OK)	When asserted (L), this signal indicates that the output current is less than 100% of the rated current (75 A).
	When negated (H), the line indicates that the output current is greater than 100% of the rated current.
Phase loss (PHASE LOSS)	When asserted (H), this line indicates that one or more of the ac phases has dropped below the low limit for its specified range.
	When negated (L), the line indicates that the three phases are above the low limit for its specified range.

Table 10–4 (Cont.)   RICBUS Status Line Description

RIC	Description
Rotation OK (ROT OK)	When asserted (L), this line indicates that the ac line phase rotation is in the correct sequence.
	When negated, (H) this line indicates that a phase is out of sequence.
Thermal warning (THERM WARN)	When asserted (L), this line indicates that an overtemperature condition exists within the UPC.
	NOTE **The line is a warning and indicates that the temperature is not at a destructive level. The UPC can operate for an indefinite period of time under the warning condition.**
Thermal fault (THERM FAULT)	When asserted (L), this line indicates that a thermal fault condition exists, and the UPC will be shut down independently of any control function.
Voltage unbalance (VOLT UNBAL)	When asserted (L), this line indicates that a condition of 10 mA of leakage current exists between the 280 Vdc output bus and the chassis.
	In this case, the kernel initiates an automatic shutdown (ASD).
Summary alarm (SUM ALRM)	When asserted (H), this line indicates that a fault other than those on the RICBUS exists within the UPC. When negated, the line indicates that no reportable faults exist within the UPC.
BBU interlock (BBU INTERLOCK)	The auxiliary contacts of CB1 (A1 module) and CB1 (A2 module) are connected in series with a set of contacts on the REMOTE/LOCAL switch in the A3 module.
	With all contacts closed, the RIC circuitry (in the kernel) inhibits the BBU from being enabled. Any open contact in the interlock circuit enables the BBU. The interlock is coupled to the RICBUS through an isolation transformer.
Ground current (GROUND CURRENT)	The ground current measurement measures the current in the ground conductor. It provides an ac current proportional to the measured ac current. The current is coupled to the RICBUS through an isolation transformer.

10.4.5 AC Input Filter (A4)

The A4 ac filter module provides each phase of the T1 secondary with a low-pass LC filter. The filters attenuate EMI and transient disturbances on the input line, and current ripple and EMI within the UPC. A pair of capacitors on each power line input also contribute to EMI attenuation (Figure 10–14).

Each filter has a cutoff frequency of approximately 1200 Hz. This frequency is high when compared to the input line frequency (50/60 Hz) but low when compared to the pulse width modulator (PWM) switching frequency (3700 Hz). The filter frequency response rejects the low frequency harmonics of the input lines, and attenuates the PWM switching frequency without interacting with the PWM control circuits.

The high voltage attenuator module (PC14) is mounted on the A4 module. The attenuator circuits (454258100, 1-1) allow each phase to be monitored, and provide attenuation of the 185 V rms input to a level compatible with the control circuits located on PC1. The attenuated phase voltages are applied to secondary voltage monitoring circuits as V SEC ØA, V SEC ØB, and V SEC ØC.

The output cables are routed through a set of common mode chokes (one per phase).
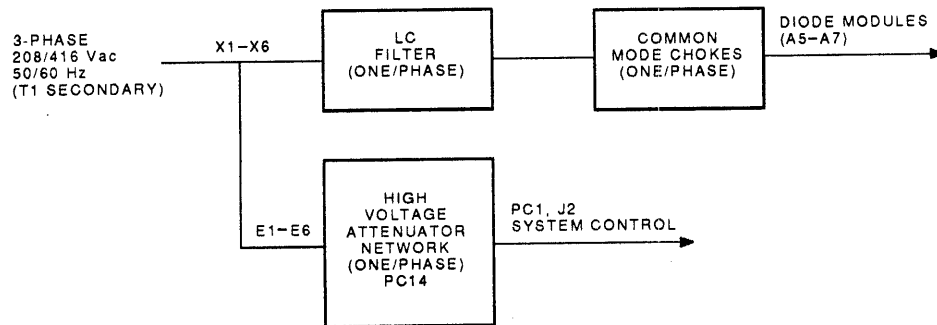
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Figure 10–14   AC Input Filter Module (A4)

10.4.6 Rectifier Power Module (A5, A6, A7)

After passing through the ac input filter (A4), each phase of the T1 output is converted to a full wave rectified dc voltage in rectifier power modules A5 (ØA), A6 (ØB), and A7 (ØC). (Figure 10–15.) The nominal and average ac and dc input and output specifications are listed in Table 10–5. For line voltages higher or lower than nominal, the current varies inversely with the line voltage.

Table 10–5   Rectifier Module I/O

Parameter	Specification
Input voltage	185 V rms, nominal
Input current	40 A rms, nominal @ full load
Output voltage	260 Vdc, nominal
Output current	24 A dc, average @ full load

10.4.6.1 Bridge Rectifier

Each rectifier input is fused to isolate the module and the circuits following T1 in the event of failure. The fuse is rated to accommodate low line and redundant operation in the case where one phase has failed and only two phases are operating normally. The fuse is a special fast-acting type and must be replaced with an exact duplicate.

The bridge rectifier consists of two half-wave bridge power rectifier assemblies connected as a full-wave bridge circuit (688000482, 1-1). The rectifier modules are mounted on a heat sink to provide cooling. The rectifiers are electrically isolated from the heat sink by a high-voltage insulating barrier incorporated within the rectifier assembly.

A filter capacitor attenuates EMI and current ripple generated by PWM power converter that follows.
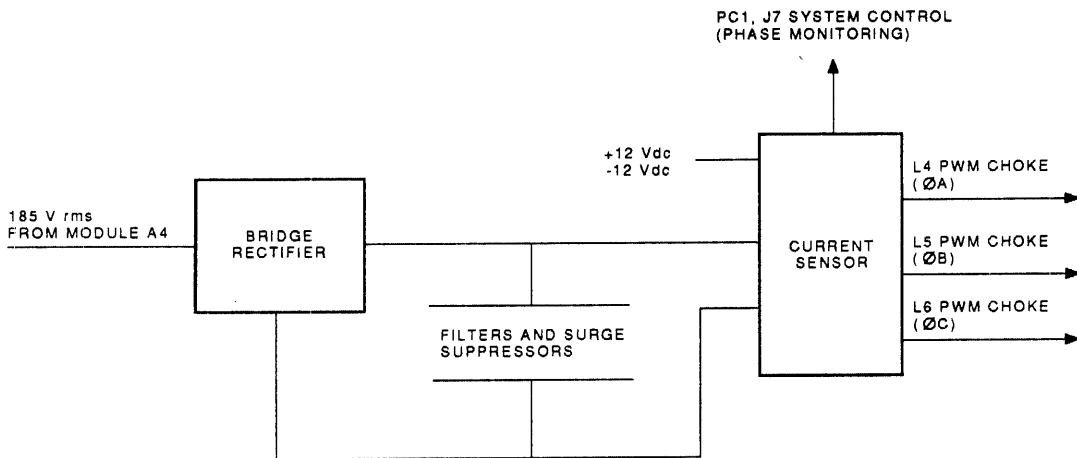
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Figure 10-15   Rectifier Diode Module

10.4.6.2 Current Sensor

A current sensor PC module (I SENSOR) is included on each diode rectifier module output (PC11 on A5, PC12 on A6, and PC13 on A7) to measure the rectifier output current (454318100, 1-1).

The current measurement controls the UPC current and provides input overload detection. The I SENSOR is installed so that the current in either the primary or secondary of the following PWM chokes are measured (L4, L5, and L6). The measurement is required because during UPC power-up and input overvoltage, current flows in both the primary and secondary of the chokes and is taken into account by the control logic.

The I SENSOR consists of a magnetic core (toroid) that surrounds the power cables from the rectifier. The core is incorporated with a Hall effect sensor and related circuitry to sense the flux generated by the rectifier output current. DC power for the sensor (+12 and -12 Vdc) is provided from the 12 Vdc power supply on PC1 (454388100, 2-7). Both dc voltages are monitored on PC1. The loss of either or both outputs initiates an emergency shutdown (ESD) of the UPC (Section 10.4.10).

The sensor output is coupled to PC1 as I (ØA), I (ØB), and I (ØC). Monitoring circuits compare the phase averages. The monitors turn on phase-related LEDs if the averages exceed the specified high or low limits.

10.4.7 PWM Power Module (A8, A9, A10)

The pulse width modulated (PWM) power modules use moderately high frequency switching in a PWM mode to convert the unregulated rectifier output voltage into a regulated dc output voltage. A power module is provided for each input phase (A8 [ØA], A9 [ØB], and A10 [ØC]). In addition, the power module drive circuits and control logic are replicated for each phase.

A power module (Figure 10-16) is a combination of power switching devices (SCRs, power transistors, and power diodes) that can be turned on and off by their related drive and control logic (698000479, 1-1). A PWM base driver module (replicated three times as PC4, PC5, and PC6) provides interface and control functions between the switching devices and the timing and driver controls located on the PWM rectifier control PC (PC2).

NOTE
If one of the power modules fail, the UPC continues to operate with this type of phase loss. However, the UPC will not operate if the phase loss is due to an ac input phase loss.

Each PWM module operates with one of the PWM chokes (L4 through L6) connected between the bridge rectifiers (A5 through A7) and the power modules. The chokes provide the energy storage mechanism required to implement controlled power conversion by power switching techniques.

During normal operation of the UPC, the load current supplied by a diode module rectifier flows through the PWM choke primary and, in turn, flows either in the power transistor, when it is turned on, or in the SCR (Figure 10-16). The ratio of time the power transistor is on, to the time that the SCR is on, determines the ratio of output voltage to input voltage.

With both the power transistor and the SCR off, current flows in the PWM choke secondary, through the power diode, to the output. This operating mode is used when the input voltage exceeds the output voltage.

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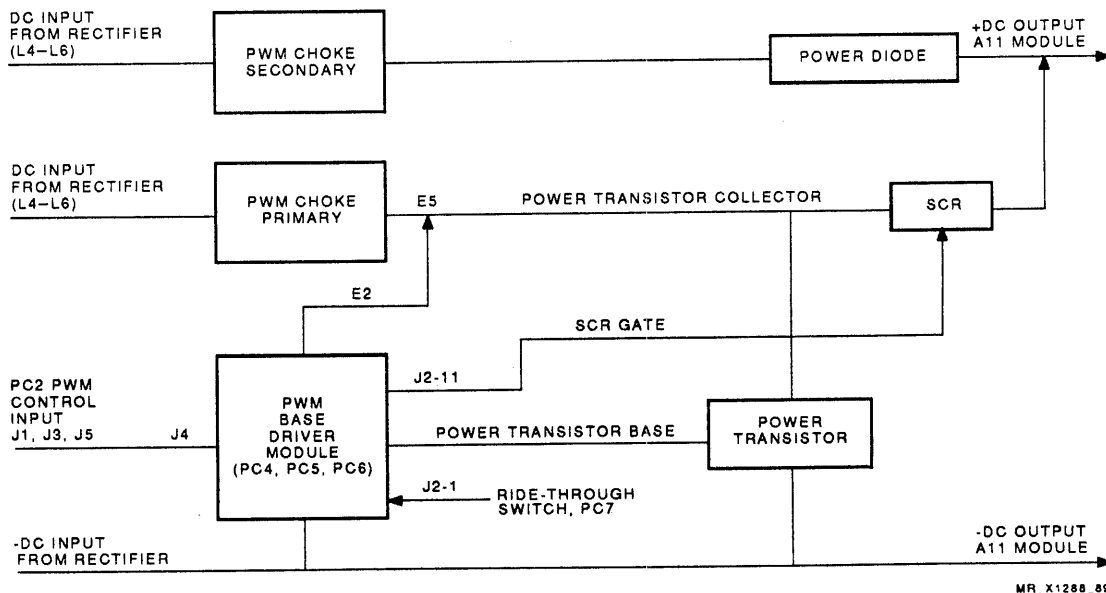
Figure 10-16   PWM Power Module (A8, A9, A10)

10.4.7.1 Base Driver Module

The PWM base driver modules (PC4, PC5, and PC6) contain the power transistor base and SCR gate drive circuits, the drive power supply (454328100, 2-2). Also included are the monitoring and fault detection circuits.

Power for the base driver modules is provided by a switching power supply (45438100, 2-2). The power supply derives its high voltage input from either the rectifier output or the dc output bus. The switching power supply converts the input voltage (ranging from approximately 120 to 300 Vdc) to the required low voltage outputs.

Power conversion is accomplished by a high voltage switching transistor driving the primary of a power transformer. The output of the transformer secondary is rectified and filtered to produce the +6 and -5 Vdc outputs.

The base drive control signal from the rectifier control module (PC2) is applied to an optical isolator to provide a noise-free coupling into the drive circuits and the power transistor base circuit (454328100, 2-2). If the power supply output drops to an unacceptable level, the optical isolator output would be disabled.

The output of the optical isolator is coupled to the power transistor drive circuits (Figure 10–17). These circuits include a power transistor and its related control and protection circuits. The protection circuit allows the power transistor to survive a momentary overload without damage.
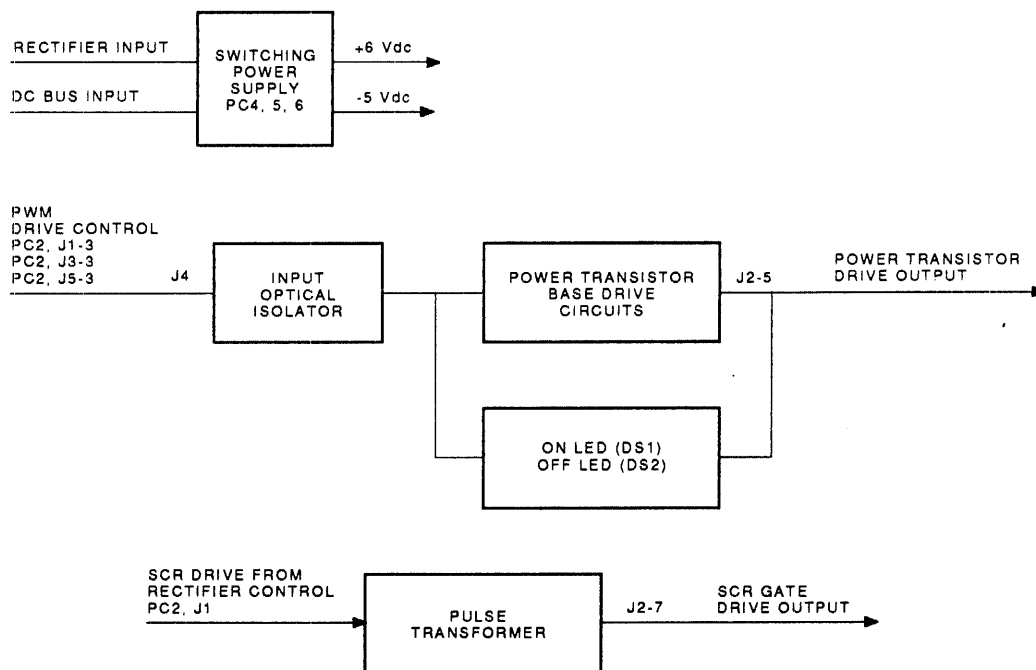
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Figure 10–17 Base Driver PC

The drive circuit for the power module SCR is provided through the pulse transformer (T2) on the base driver module. The transformer converts the low power drive pulses generated on the rectifier control module, to the high power SCR gate circuit on the power module. The gate circuit output provides very fast SCR triggering.

Two RC networks (snubber circuits of 454328100, 1-2) are included on the driver module. These circuits control the switching characteristics of the power transistor, SCR, and power diode of the power module. The circuits control voltage and current rise times, and limit EMI and transient voltages across the power devices.

The drive module contains two LEDs (DS1 and DS2) to indicate drive circuit status. DS1 is defined as the on LED; DS2 is defined as the off LED. Table 10–6 lists status and fault conditions.

Table 10–6   Drive Circuit Status

LED Status		
DS1	**DS2**	**Fault Condition**
On	On	UPC is operating normally with load.
DIM	On	UPC is operating normally with no load.
Off	On	CBI is on; UPC is turned off by LOCAL/REMOTE switch.
Off	Off	CBI (input breaker module) is on.

10.4.7.2 Thermal Sensors

Two positive, temperature coefficient, thermal sensors (PTCR1 and PTCR2) are located on the drive module. Although the sensors are mounted on the module, they are thermally connected to the power module heat sink through the mounting screws and thermally conducting spacers.

The sensors monitor the power module heat sink and provide the following status to the alarm circuits of the system control module:

- PTCR1 has a nominal rating of 70°C and provides a thermal warning.

- PTCR2 has a nominal rating of 90°C and provides a thermal fault.

In addition, the thermal fault is coupled to the PWM rectifier control module (PC2). The fault effectively inhibits the drive pulses for the power transistor and SCR. In effect, the thermal fault turns off that particular PWM module. At this point, the on LED (DS1) is off and the off LED (DS2) is on.

It is not unusual for a PWM module to be cooled sufficiently by the A18 fan assembly to restart, overheat, and turn off again. The module may continue to cycle in this manner for an indefinite period. This condition is indicated by the on/off LED cycling.

10.4.7.3 PWM Rectifier Control (PC2)

The PC2 input functions represent operating conditions within the UPC. These functions generate drive signals that control the PWM power transistors and SCRs on A8 through A10, and the ride-through switch (PC7). Major input signals include the:

- UPC input voltage as measured from the T1 input transformer secondary (V SEC)

- Phase currents (ILA, ILB, ILC) from the current sensor (I SENSOR) outputs on each of the diode modules (A5 through A7)

- UPC output voltage and current (V OUT and I OUT) from PC1, system control module

- Ride-through capacitor output voltage from A15 through A17 (VRT)

The rectifier control module is divided into two major sections: one PWM control section and three base driver control sections (Figure 10-18). A driver control section is provided for each PWM power module. In addition, power for PC2 is supplied from the +12 and -12 Vdc power supply on the system control module (PC1).

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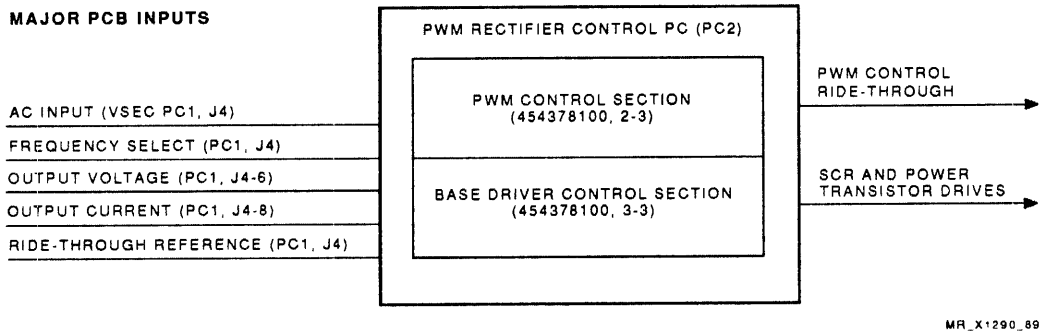
Figure 10-18   Basic PC2 Module

10.4.7.4 PWM Control

The PWM reference or clock pulses are derived from the phase-locked oscillator, which is synchronized to the incoming power frequency by the phase A reference function (ØA REF) (Figure 10-19). This assures that the PWM power converter pulses have a fixed-phase relationship to the power waveform.

The line frequency operation is selected through a semiconductor switch. The select function is applied to the frequency dividers. This produces a 3700 Hz output at 50 Hz and 3720 Hz at 60 Hz, which are used as a reference for the PWM converters. The divider output is replicated for each phase (CSA, CSB, and CSC) and applied to each base driver control section.

50/60 Hz SELECT   J8-12

Ø A REFERENCE
(50/60 Hz)   J8-15   PHASE-LOCKED OSCILLATOR   50/60 Hz   FREQUENCY DIVIDERS   3700/3720 PWM REFERENCE
CSA, CSB, CSC
J11-7, J12-7, J13-7

UPC ON/OFF   J8-2
VFF   VOLTAGE AND CURRENT FEED FORWARD
RT   J8-1

V OUT   J8-10   VOLTAGE FEEDBACK AND RAMP UP   VOLTAGE AND CURRENT FEED FORWARD   PWM LEVEL CONTROL   PWM CONTROL (Ip CONT) TO BASE DRIVER CIRCUITS

NO-LOAD FEEDBACK   NO-LOAD FEEDBACK (NLFB)

UPC ON/OFF
FROM DRIVER CIRCUITS

ILA, B, C
J8-5, 6, 7   CURRENT SUMMING AMPLIFIER   CURRENT OVERLOAD COMPARATOR   RIDE-THROUGH DRIVE CIRCUIT   J2-5, 6
RIDE-THROUGH DRIVE TO RIDE-THROUGH SWITCH (RT POS/NEG)

VRT   J8-9   RIDE-THROUGH REFERENCE CIRCUIT   CURRENT LIMIT THRESHOLD CIRCUIT   CURRENT LIMIT THRESHOLD (I LIM THLD) TO DRIVER CIRCUITS

MR_X'29'_89

Figure 10–19   PWM Control

The frequency dividers also produce:

- Line frequency feedback control to set the phase-locked oscillator frequency at 22.32 kHz at 60 Hz and 22.20 kHz at 50 Hz

- An error voltage used to hold the oscillator output synchronized with the phase A reference input (ØA REF)

The 22 kHz oscillator output is applied to the PWM level control circuit, with the outputs of the voltage and current feed forward circuits. The level control circuit produces a 22 kHz square wave (Ip CONT) having a duty cycle based on the feed forward inputs. Ip CONT is coupled to the PWM modulator circuit (base driver control section) and controls the operating current levels of the PWM converters. This action forces a slow ramp-up of the UPC output voltage.

If any of the phase currents exceeds its limit, the PWM pulse of that phase must be terminated. This is accomplished by deriving a current limit threshold that responds to the phase currents. The phase currents (ILA, ILB, ILC) are applied to the current summing amplifier and, in turn, to the current limit threshold circuit.

As a phase current increases above an acceptable level, the current limit threshold circuit enables the current limit threshold function (I LIM THLD). I LIM THLD is applied to the appropriate drive control section, effectively turning off the PWM SCR and power transistor drive circuits. If the current increases further during ride-through mode, the ride-through (RT) drive circuit output (RT POS and RT NEG) of the control section turns off the input optical isolator of the ride-through switch (PC7).

10.4.7.5 Base Driver Control
The reference voltage for the base driver control sections is derived from one of the following:

- The ac input (V SEC) during normal operation coupled through the bandpass filter and operational amplifier and applied to the PWM reference selector and amplifier

- The ride-through voltage (V RT) during ride-through operation through the ride-through reference circuit and also applied to the PWM reference selector and amplifier

The selector and amplifier output is the reference (or program) level of current from each PWM converter that satisfies the current conditions of input voltage, output voltage, and load. The output is applied to the PWM control and summing amplifier (Figure 10-20).

An additional input to the summing amplifier is the no load feedback function (NLFB). The NLFB function provides an override to reduce further the PWM pulses during no-load and extremely light-load conditions. This override prevents the UPC output voltage from increasing above the specified limit.

The summing amplifier output is applied to the square root circuit that produces an approximated square root output to the PWM ramp and pulse generators. The ramp and pulse generator charges and discharges the timing capacitor PWM pulse width set capacitor (Figure 10-20).

The level of capacitor charge voltage effectively determines the pulse width of the power transistor and SCR drive pulses. The capacitor is discharged at the start of each PWM pulse in response to clock signals CSA, CSB, and CSC. Once the capacitor is discharged, the current source begins to charge the capacitor. The charge time determines the PWM power pulse width.
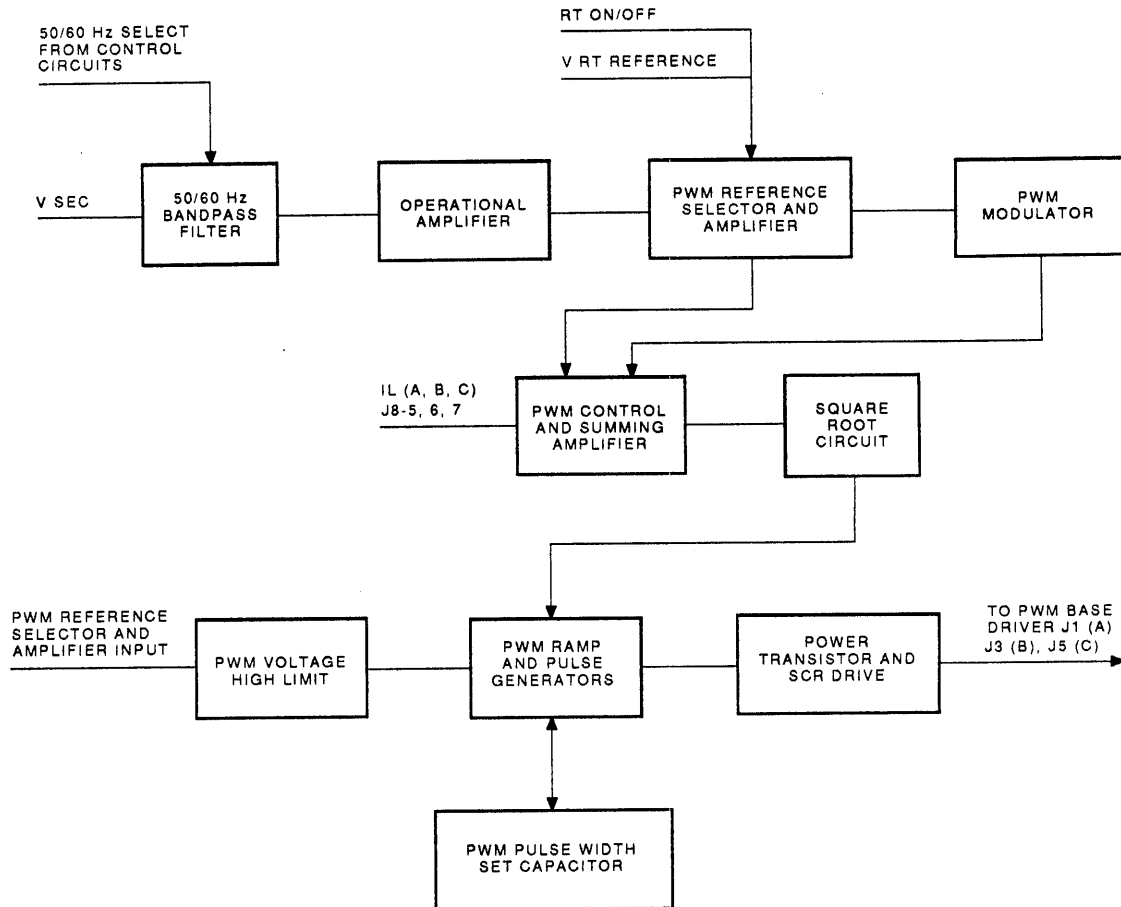
MR_X1292_89

Figure 10-20   PWM Driver Layout

The capacitor discharge voltage setting continuously varies in response to the current UPC programming (as represented by the square root input). However, if the capacitor is initially discharged to 0 V, the capacitor voltage will charge to 6 V between PWM pulses. This condition represents the maximum pulse width of the power converter.

The power transistor driver generates the power transistor drive pulse. The drive pulse (PWM DRIVE POS and PWM DRIVE NEG) is applied to the PWM base driver module and effectively turns on the bipolar power transistor on the PWM power modules.

The SCR gate driver initiates the SCR trigger pulse. The trigger (SCR DRIVE POS and SCR DRIVE NEG) is applied to the pulse transformer of the PWM base driver module, effectively triggering the SCR at the end of the power transistor pulse.

If the capacitor voltage is greater than the output voltage (V OUT) input, a shorter duration pulse is indicated. When this condition is detected, the power transistor is inhibited until the timing capacitor voltage is less than the V OUT input. When the voltage is sufficiently lower, a delayed transistor power pulse can be initiated followed by the SCR trigger.

During power-up and input voltage surges, the timing capacitor voltage may increase to approximately 6.6 V where an even shorter duration pulse is indicated. In these cases, the transistor and gate driver logic essentially delays the transistor pulse and SCR trigger until the capacitor voltage decreases to the acceptable level.

During initial ramp-up, the input voltage (V SEC) to the PWM rectifier may exceed the output voltage (V OUT). In this case, the SCR driver is inhibited by the PWM voltage high limit circuit until V SEC decreases to the acceptable level.

10.4.7.6 Thermal Fault Detection

An overtemperature condition (thermal fault) is detected by the thermal sensor on the base driver module (PC4 through PC6) of the PWM power modules. The sensor output is applied to a fault detector circuit in the ramp and pulse generator circuit. The fault detector effectively disables the power transistor and SCR driver circuits.

10.4.8 Ride-Through Components

The UPC includes very high capacitance electrolytic capacitors contained in modules A15 through A17, and the dc output filter (A11 module). The ride-through control circuits are located in the A13 compartment and consist of the following modules:

- Ride-through recovery, PC16

- Ride-through switch, PC7

- Fast discharge circuit, PC8

10.4.8.1 Ride-Through Recovery (PC16)

The ride-through capacitors are initially charged when the UPC is turned on, or recharged after a ride-through operation. An optical isolator input drive enables the recharge circuit (454308100, 2-2). The input drive is turned off during the ride-through operation to prevent the recycling of power from the dc output to the discharging ride-through capacitors.

An active regulator included in the ride-through recovery circuit recharges the capacitors (in approximately 500 ms) to a voltage essentially equal to the dc output. The regulator circuit consists of a bipolar power transistor, power diode, and choke (mounted on the chassis) control circuits, and a floating power supply. The power transistor, diode, and choke are configured as a buck switching constant current regulator. This configuration provides a controlled current from the dc output to the ride-through capacitors as their voltage is initially charged or recharged (Figure 10–21).

The control is approximately a constant current mode. This is accomplished by:

1. Switching the power transistor off when the current in the transistor and choke reach a preset limit (approximately 20 A)

2. Restarting the power transistor after a fixed-time delay

The power transistor pulse frequency during the constant current operation is several thousand pulses per second, with the choke ripple current varying accordingly. Once the ride-through capacitors are fully charged, the power transistor remains on, providing a low impedance recharge path for the capacitors.

NOTE
The recharge cycle produces a high-frequency whine. This is a normal condition.
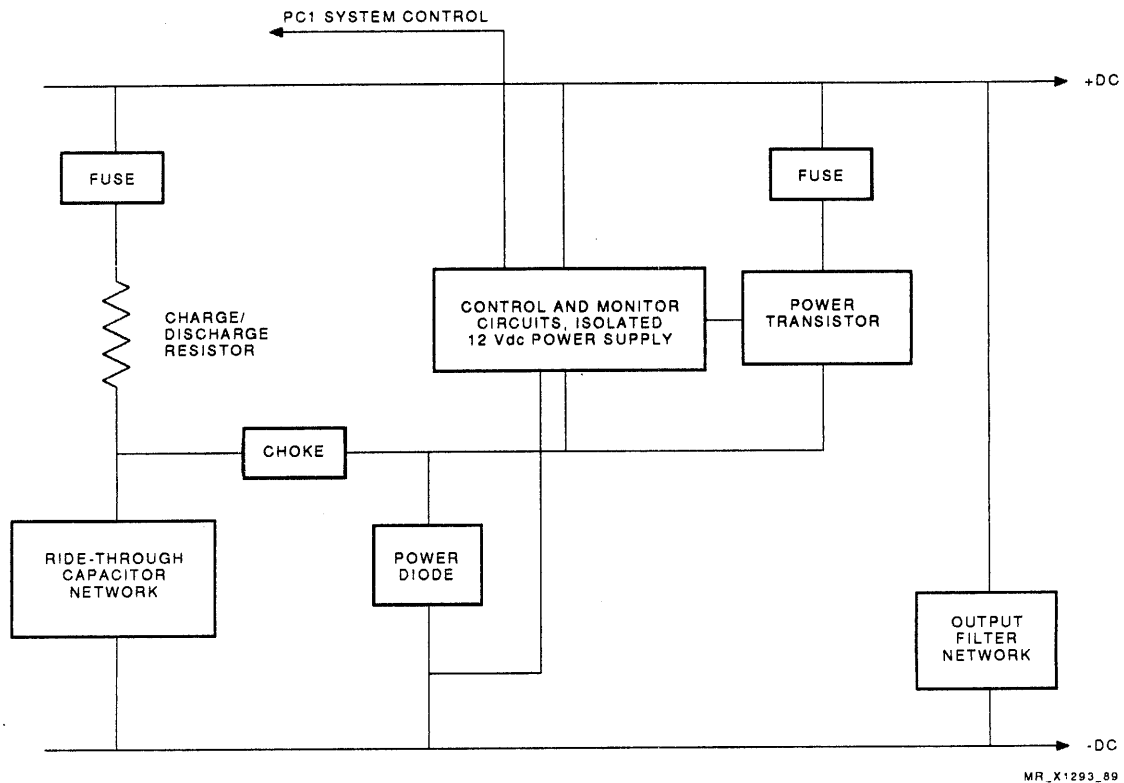
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Figure 10-21   Ride-Through Recovery

Drive for the power transistor is provided through a power MOSFET. During normal operation, the power transistor is switched on, unless one of the following conditions exists:

- The output current exceeds the current limit threshold.

- The power supply has failed as detected by the power supply monitor.

- The input control to the optical isolator is negated.

Each side of the dc output (+ and -) is protected by a fuse.

The floating power supply derives its input power from the dc output bus. Through a combination of oscillator, transformer, rectifier, and zener diode, the power supply produces a +12 Vdc regulated output. Power supply operation is identical to the +12 Vdc isolated power supply of the A3 module (Figure 10-11).

The output is coupled, through an optical isolator to an alarm circuit driving an LED on the system control module. The circuit drives the ride-through recovery fault (RT REC FLT) LED on the alarm panel of PC1. Loss of the +12 V turns the LED on.

10.4.8.2 Ride-Through Switch (PC7)

The ride-through switch module (PC7) is a semiconductor power switch that is switched on when the dc output must be supplied by the ride-through capacitors, and switched off during normal operation (454368100, 1-1).

PC7 consists of a bipolar power transistor switch, phase isolation diodes and fuses, drive and monitoring circuits, and a self-contained power supply (Figure 10-22). The drive and monitoring circuits are optically coupled to the UPC system controls.

The high voltage from the ride-through capacitors is a single-source input. However, the ride-through output must be coupled to each phase of the output circuit. The output isolation diodes provide the coupling but prevent the three phases from interacting during normal operation. In addition, the outputs from the isolation diodes are protected by fuses.

The control signal is applied to the control input optical isolator from the system controls. The isolator output effectively turns on the MOSFET driver, which turns on the power transistor switch. The ride-through capacitors are then discharged through the power transistor, and through the isolation diodes, into each output phase.

The low voltage power supply receives its power input from the high voltage dc bus through an RC network. The high voltage is first regulated to +24 Vdc and then to +12 Vdc. A power supply monitor prevents the circuit from operating when the supply voltage is insufficient. In addition, the power supply has a ride-through capability provided by a ride-through capacitor.
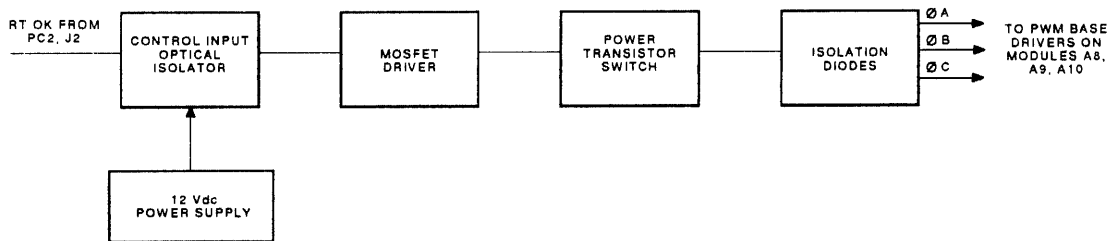
Figure 10-22   Ride-Through Switch

10.4.8.3 Fast Discharge Circuit (PC8)

The UPC includes high capacitance electrolytic capacitors in the ride-through modules (A15 through A17) and in the dc output filter (A11 module). When the UPC is turned off — and after the ride-through and shutdown sequence — the capacitors are automatically discharged to a safe servicing level through the fast discharge circuit.

Since the bleeder resistors connected across each capacitor do not provide an adequate high-speed discharge path, the discharge circuit provides two major functions:

• The dc output is discharged to less than 140 Vdc in approximately 30 ms.

• All capacitors are discharged to less than 25 Vdc in approximately 15 additional seconds.

LEDs are included to indicate operational status of the circuit, and that the voltage is at a safe service level. Capacitor voltage test points are also included on the module.

The fast discharge circuit includes a discharge resistor, and a SCR and power MOSFET combination (Figure 10–23). Discharge control is provided through an optical isolator. Whenever the discharge circuit is enabled, the SCR is triggered on and provides a 2-ohm discharge resistance across the dc output. This low resistance quickly discharges the output filter capacitors and any capacitors associated with the load. The peak discharge current is approximately 140 A with a time constant of 10 to 40 µs, depending on load and load capacitance.

While the control input of the optical isolator is driven, the fast discharge circuit is inhibited. However, when the input drive is removed, the discharge circuit is enabled. The circuit is fail safe in that it discharges the capacitors even if the low voltage power supply fails.

The ride-through capacitors are also discharged (Figure 10–23). However, they discharge at a slower rate due to the 50 ohm ride-through charge/discharge resistor. In addition, the lower level of current from the ride-through circuit (6 A peak) is diverted through the MOSFET, commutating the SCR off. This is required since the SCR must be commutated off before the UPC can be restarted.

A fuse (F3) is included in the SCR discharge circuit to prevent failures in the circuit from causing additional damage. Two fuse status LEDs are incorporated into the circuit: DS2 indicates that F3 is OK; DS3 indicates that F3 is cleared. In addition, if the dc output voltage is not present, DS2 and DS3 are turned off.

The ride-through voltage monitor consists of a current source that turns on the DS1 LED (BUS NOT DISCHGD) when the voltage exceeds 25 Vdc. When the ride-through voltage is discharged to less than 25 Vdc, DS1 turns off, indicating a safe bus status.
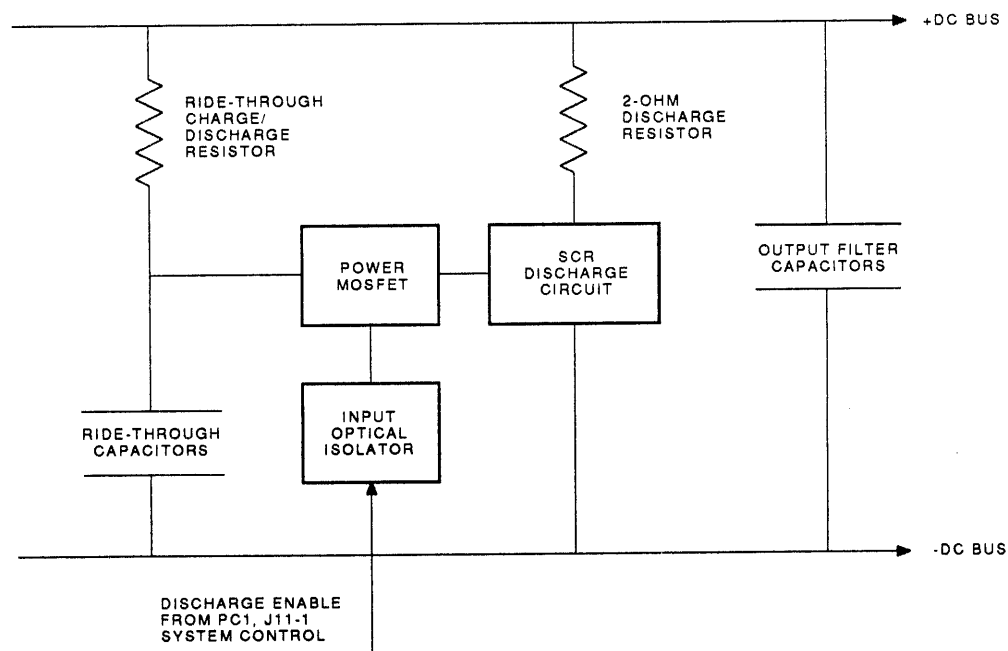
Figure 10–23   Fast Discharge Circuit (PC8)

10.4.9 System Control Module (PC1)

The system control module (PC1) includes circuits that provide a major part of the overall UPC control and monitoring. PC1 functions include:

*   An isolated regulated power supply

*   Voltage and current monitoring

*   Fault detection, status, and alarm indicators

*   Inputs to the control and status RIC interface

In addition, PC1 provides the UPC on/off functions and ride-through control capabilities.

PC1 is equipped with an alarm panel (Figure 10–24). The panel contains a number of LEDs that indicate UPC status, operating conditions, and faults. Several of the LEDs are latched through flip-flops on particular fault and condition detection. Once the fault or condition is cleared, the LEDs may be turned off by initiating a reset function to the affected flip-flops by pressing the RESET switch located on the A3 module face panel. The switch also resets two alarm functions on the RICBUS. The latched panel LEDs and the RIC signals cleared by the RESET switch are:

*   Alarm panel:

    ± Volt fault
    Input overvoltage (IN OVVLT)
    Ride-through unbalance (RT UNBAL)
    Input overload (I OVLD)
    Output overload (OUT OVLD)
    Output overvoltage (OUT OVVLT)

*   RICBUS:

    Thermal fault (THERM FAULT)
    Voltage unbalance (VOLT UNBAL)
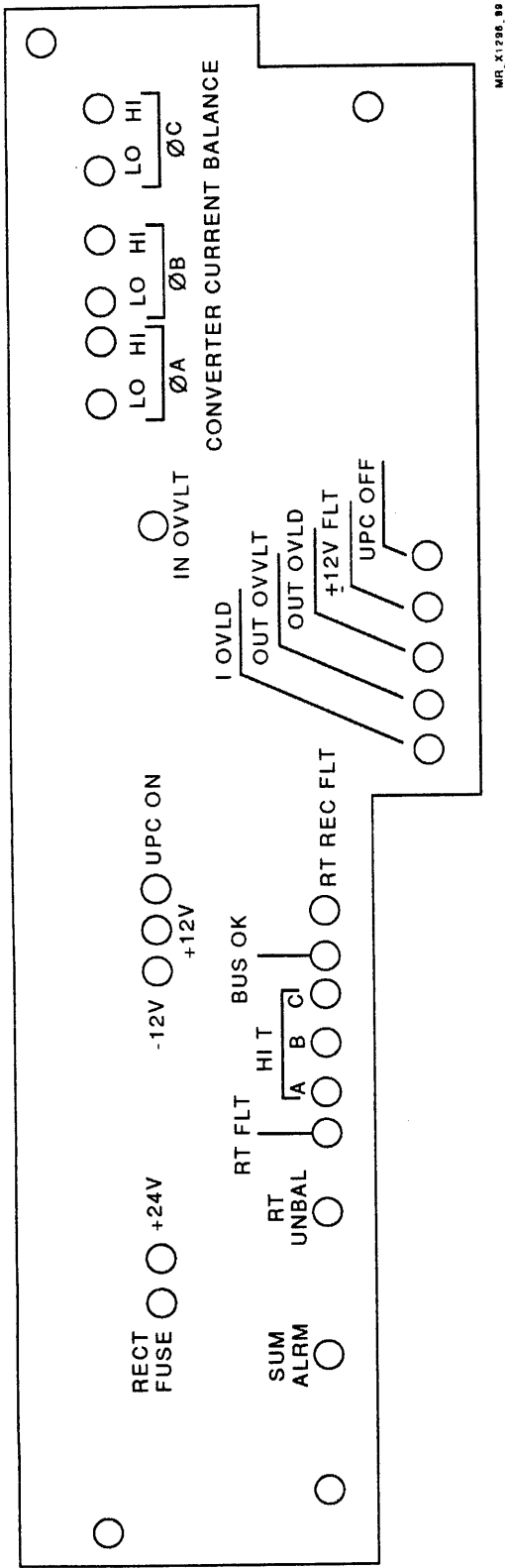
Figure 10–24   PC1 Alarm Panel

10.4.9.1 12 V Power Supply

The 24 Vdc power input (24V POS) to PC1 (454388100, 2-7) is applied to a flyback switching regulator circuit (Figure 10–25). The regulator drives a MOSFET (Q1), which drives an isolation transformer/inductor combination (T1) to produce regulated outputs of +15 and -15 Vdc. Feedback for voltage regulation is derived from an auxiliary primary winding of T1.

Each 15 V supply output is applied to an adjustable integrated circuit voltage regulator, which produces the precision regulated +12 and -12 Vdc. These outputs supply the PC1 control circuits. In addition, two LEDs monitor the 12 Vdc outputs (DS3 labeled +12 Vdc and DS4 labeled -12 Vdc).

NOTE
The 12 V LEDs imply only active supplies and do not represent accurate voltage outputs.

The 12 V outputs are also applied to an unbalance level detector. Should an unbalance between the supply outputs be detected, the detector output is latched (if the enable function, ALARM ENABLE, is set). The latched output (±12 ALARM):

*   Turns on DS17 (labeled ±12 ALARM) on the alarm panel

*   Initiates an emergency shutdown (ESD)

*   Trips the main circuit breaker (CB1) in the A1 module

10.4.9.2 24 V Fault Monitor

The 24 V input is also applied to a monitoring circuit (454388100, 2-7). However, since the monitoring circuit is on the input side of a fuse (F1), the circuit responds to the 24 V input even though that fuse is cleared. The presence of 24 V is indicated by a lit LED (DS2) on the alarm panel and is labeled +24 V (Figure 10–25).

The monitor has two threshold levels:

1. An impending power supply failure, which sets the UPC power-down function (UPC PWR DN) and initiates a UPC automatic shutdown (ASD)

2. A power supply failure, which sets the 24 V fault function (24V FLT) and turns off the 24 V LED (DS2), and initiates an immediate shutdown (ISD)

In both cases, the UPC off LED (on the alarm panel) turns off. No alarms are generated unless the ac input voltage falls below the lowest specified level, or there is a circuit failure.
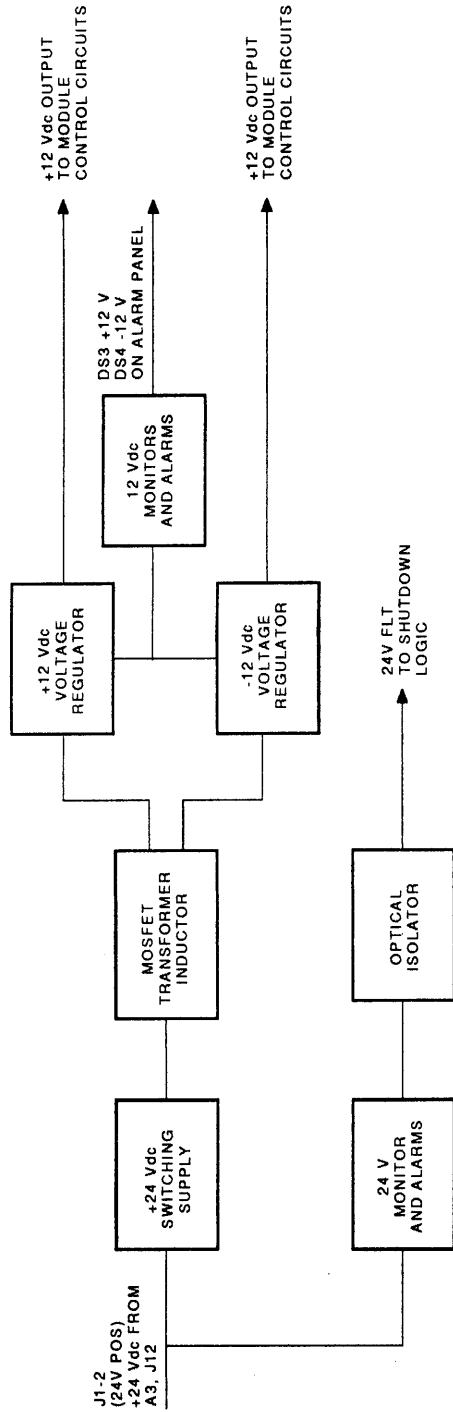
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Figure 10–25   12 V Power Supply

10.4.9.3 Input/Output Voltage Monitors

AC input and dc monitors are provided by PC1 (454388100, 3-7). The ac input voltage from the isolation step-down transformer of the A3 module (ØA MON, ØB MON, ØC MON) is monitored by two input voltage monitors (Figure 10–26).

The first monitor detects a loss of an input voltage phase. The ØA MON, ØB MON, and ØC MON signals are applied to a set of differential amplifiers (one per phase). The outputs of the differential amplifiers are rectified, combined, and coupled to a phase level comparator. This input is compared against an equivalent 3-phase input. A loss of one phase causes the comparator to drive an optical isolator, producing the phase loss output function (PHASE LOSS) on the RICBUS. PHASE LOSS causes an automatic shutdown (ASD) and turns the UPC off LED (DS9) on the alarm panel off.

The second monitor detects an incorrect phase rotation (sequence). ØA MON and ØC MON are applied to a phase rotation sequence detector. If an incorrect phase sequence is detected, the detector output turns its associated optical isolator off, producing the rotation not OK function (ROT OK H), negating the ROT OK function on the RICBUS.

The rectified MON output is applied to an input overvoltage detector. If an input overvoltage condition (over the maximum steady-state level) is detected, the detector output sets the input overvoltage latch (INPUT OVVLT). INPUT OVVLT sets the input overvoltage LED (IN OVVLT) on (DS25 on the alarm panel) and initiates an emergency shutdown (ESD). A time constant of approximately 2 seconds in the detector prevents a false alarm for overvoltage transients.
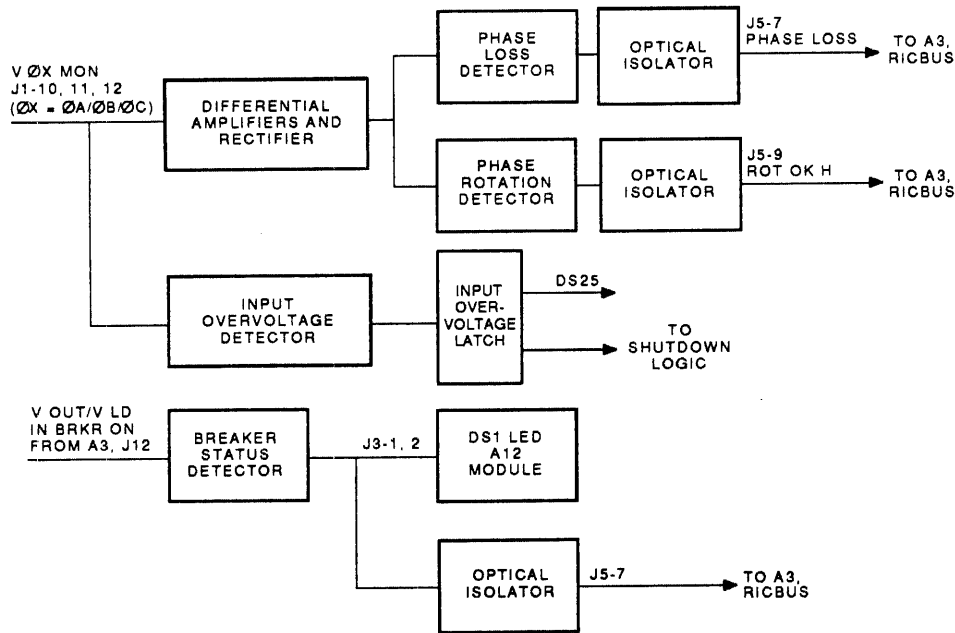
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Figure 10–26   Input/Output Voltage Monitors

The A12 module is installed only on tri- and quad processor VAX 9000 systems. The output switch LED (DS1 located on the A12 module) is on if the input circuit breaker (CB1 on the A1 module) is on (IN BRKR ON) and one of the following is present:

    The output voltage (V OUT)
    The load voltage (V LOAD)

NOTE
If the ac on LED is on, the switch must not be operated.

10.4.9.4 Current Unbalance Monitor

During normal UPC operation, the input phase currents are balanced within approximately 10% of each other. However, if the input line voltage becomes excessively unbalanced, or one phase of the PWM power converters fails, the phase currents become unbalanced. This condition is detected by the unbalance monitor circuit (454388100, 4-7).

The output phase of each diode rectifier module is monitored (Figure 10–27). The rectified current (I$\emptyset$A, I$\emptyset$B, and I$\emptyset$C) is monitored from the current sensors of the A5 through A7 modules (PC11, PC12, and PC13). The dc output current (I OUT) is monitored from the current sensor (PC10) of the A11 output filter module.

An unbalance condition of approximately 10% is detected by a set of operational amplifiers. The three input phases from the diode modules are applied to the operational amplifiers to produce a three-phase average. This average produces a high average limit and a low average limit.

The phase input currents (I $\emptyset$A, I $\emptyset$B, I $\emptyset$C) are compared to these limits. Any phase exceeding a limit is detected through a set of voltage comparators (high and low comparators for each phase). Each comparator drives a corresponding converter current balance LED located on the alarm panel ($\emptyset$A HI, LO, $\emptyset$B HI, LO, and so on). If an unbalance condition is detected, the affected comparator output turns on the summary alarm LED (SUM ALRM), DS12 on the alarm panel, and drives its associated RICBUS optical isolator.

The same unbalance functions are monitored during ride-through operation. Since ride-through events are momentary, the detected unbalance is latched and indicated by turning on the ride-through unbalance LED (RT UNBAL), DS24 on the alarm panel.
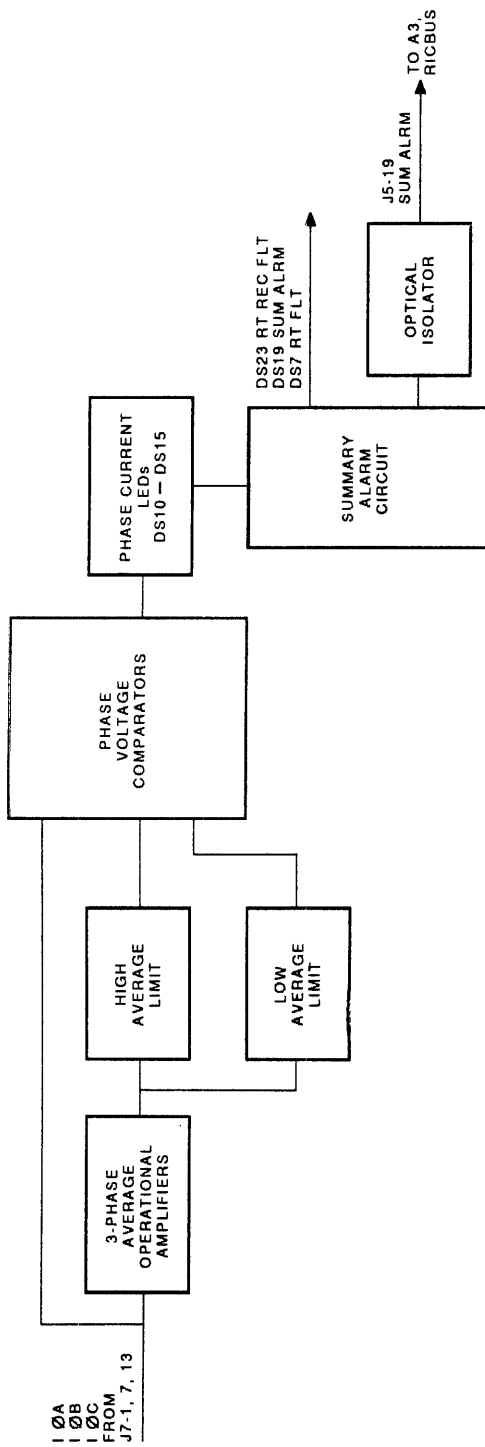
Figure 10-27   Input Unbalance and Overload Monitors

Failures detected on the ride-through switch module (PC7) or the ride-through recovery module (PC16) are also applied to the summary alarm circuit and its RICBUS optical isolator (Figure 10–28). Ride-through switch faults set the ride-through fault LED (RT FLT), DS7 on the alarm panel, to on. Ride-through recovery faults turn the RT REC FLT LED on. Both LEDs are normally on until the output voltage reaches its nominal operating level, or if the modules are disconnected.

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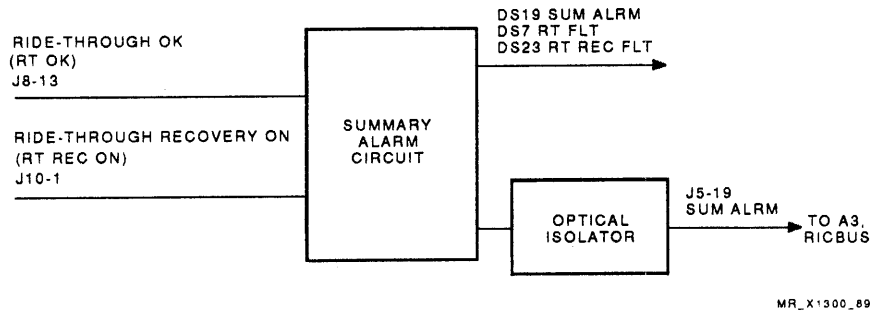
Figure 10–28   Ride-Through Faults

10.4.9.5 Input/Output Overcurrent Monitors

The phase currents (I ØA, I ØB, I ØC) are also applied to an input overcurrent detector circuit (454388100, 4-7) (Figure 10–29). The circuit is a set of comparators (one per phase) that detect phase currents that exceed the maximum design limits of the PWM power modules. The comparator outputs are filtered and applied to the input overload latch (I OVLD). If an overload is detected, the comparators set the I OVLD latch and initiate an ISD (Section 10.4.10).

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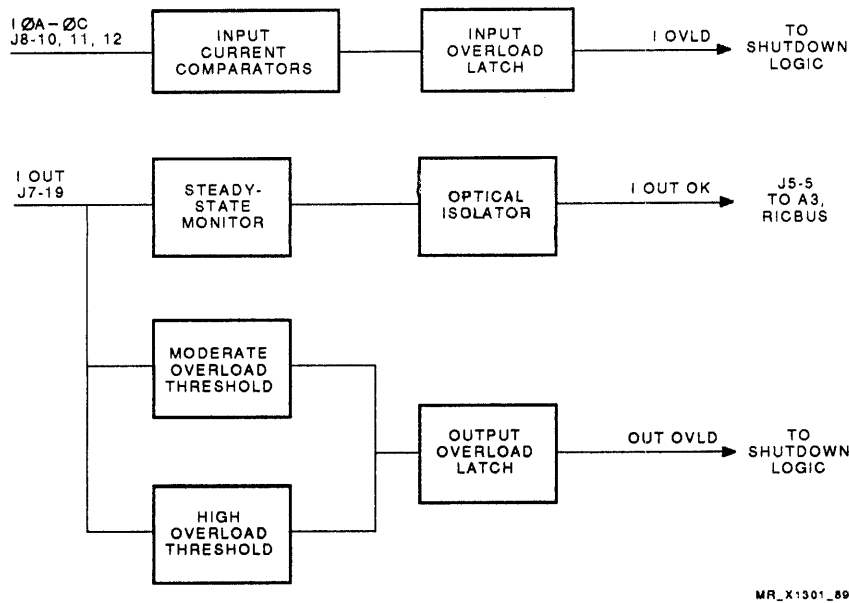
Figure 10–29   Input/Output Current Monitors

The output current (I OUT) from the A11 output filter module is monitored. I OUT is applied to two level detectors. One detector monitors the steady-state output current to assure it does not exceed the rated full load (I OUT OK). I OUT OK is applied to the A3 module and is returned to the kernel through the RICBUS.

The second level detector indicates overload conditions that exceed the momentary overload ratings and initiate an ESD. Two overload threshold levels are determined by a pair of comparators, each having a different response time:

● A fast response for high overloads

● A slower response for moderate overloads

Should an overload condition (either moderate or high) be detected, the affected comparator output sets the output overload latch (OUT OVLD). OUT OVLD turns on DS16 (on the alarm panel) and initiates an ESD.

10.4.9.6 Thermal Condition Monitors

Should one of the PWM power modules (A8, A9, A10) reach a temperature above normal, the condition is detected by a set of voltage comparators (one per phase) (454388100, 4-7). Each comparator drives an associated phase LED (HI T A, HI T B, and HI T C) located on the alarm panel. In addition, the high temperature condition is coupled into the summary alarm circuit, turning the SUM ALRM LED on and enabling the SUM ALRM optical isolator to the RICBUS.

Two temperature sensors (RT1 and RT2) are located on PC1 to monitor the UPC internal ambient temperature (Figure 10–30). Each sensor is an input to a voltage comparator. RT1 is enabled at 30°C. Its voltage comparator output drives the thermal warning (THERM WARN) optical isolator, in turn asserting the THERM WARN function on the RICBUS.

RT2 is enabled at 40°C. The RT2 output turns on the thermal fault (THERM FAULT) optical isolator, and asserts the THERM FAULT function on the RICBUS. The RT2 output also enables its voltage comparator. The comparator output sets the high temperature fault (HI T FLT) latch, which initiates an ISD.

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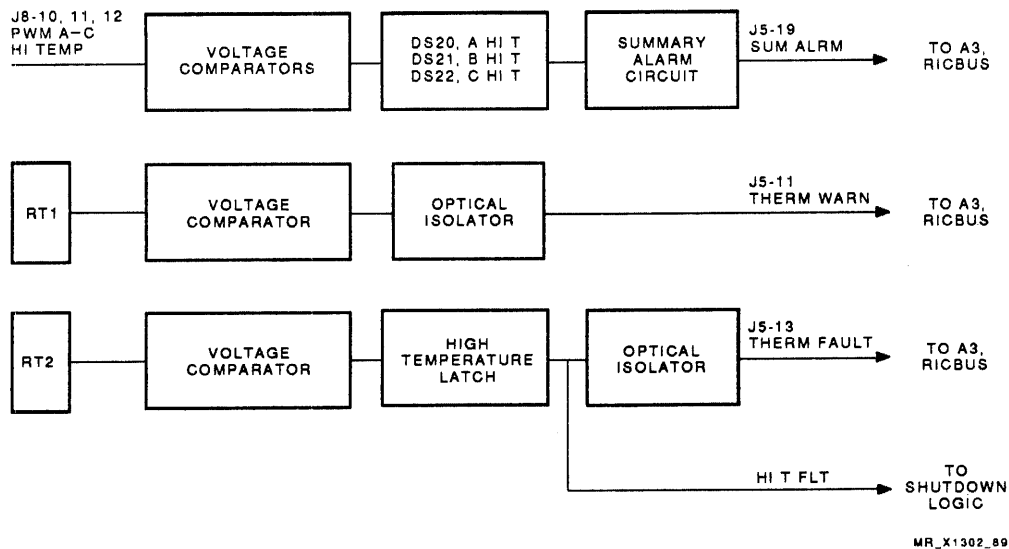
Figure 10–30 Thermal Condition Monitors

10.4.9.7 Ride-Through Operation Control

A ride-through operation is initiated whenever the UPC ac input falls below the specified input limit of 161 Vac. The ac input voltage (VSEC ØA through ØC) is monitored through a set of differential amplifiers (one per phase) (454388100, 5-7). Since VSEC is the secondary voltage on the input transformer T1, the differential amplifiers can detect when CB1 has been tripped, and the loss of ac input.

The differential amplifier outputs are rectified, combined, and applied to an operational amplifier (Figure 10–31). The amplifier output is applied to an RC circuit that exhibits:

- A fast response to ac voltage dropouts

- A slow response as the voltage recovers

The RC circuit output is then applied to a comparator with a threshold set to respond to an ac input voltage lower than the specified operating range. The comparator output enables the function V SEC OK into the shutdown logic. V SEC OK is also ANDed with the BUS OK function (output voltage normal) to generate the ride-through recovery off function (RT REC OFF NEG) to PC16 on the A13 module, and the not ride-through function (not RT) to PC2.

These functions:

- Initiate the ride-through operation, provided the output voltage is normal (BUS OK asserted)

- Initiate an ISD if the ride-through operation is excessively initiated, where the ride-through initiation duty cycle exceeds approximately 20% for more than 5 seconds

The ISD is initiated by a negated V SEC OK function into the shutdown logic. The UPC then requires an approximate 5-second delay before initiating a restart operation.

When a ride-through operation is initiated, the ride-through recovery circuits on PC16 must be disabled. The enabled RT REC OFF NEG function is applied to an optical isolator on PC16 (ride-through recovery module), effectively inhibiting the ride-through capacitor recharge power transistor.
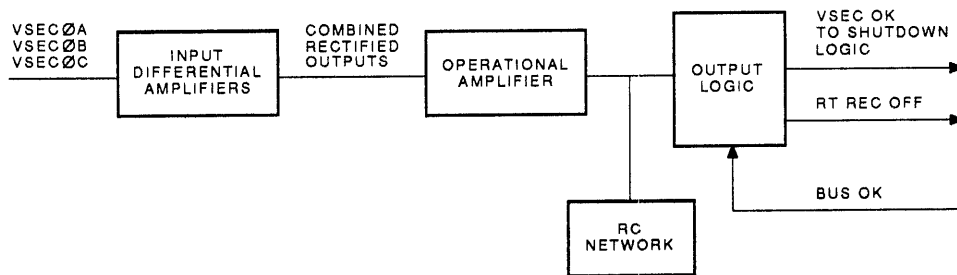
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Figure 10–31   Ride-Through Control

The ride-through capacitor voltage (V CRT POS) is applied through a set of buffer amplifiers (454388100, 6-7). The buffer amplifier output is coupled to a monitor circuit that determines the remaining storage time in the ride-through capacitors (Figure 10–32). The monitor circuit can be overridden by the power-down ramp function (PWR DN RMP) from the shutdown logic if an alarm condition requires a UPC shutdown.

A dual DIP switch (S1/S2) controls two RC circuits at the input of the monitor (454388100, 6-7). The RC circuits control the point at which the monitor output is enabled. The enabled monitor output drives the ac low (AC LO) optical isolator to the RICBUS on the A3 module. S1 effectively sets AC LO when 10 µs of hold-up are left before shutdown. S2 provides 100 µs of hold-up before AC LO is asserted.

When the ride-through capacitors are fully recharged and the ride-through function (RT) is asserted, the monitor output effectively negates AC LO. With RT asserted, the capacitors should be fully charged. However, if they are partially discharged, then AC LO remains asserted until the capacitors are fully charged or the deficiency is corrected.

A comparator circuit detects when the ride-through capacitors are discharged. The output of the comparator effectively enables the bus low (BUS LO) optical isolator, which is coupled to the RICBUS.
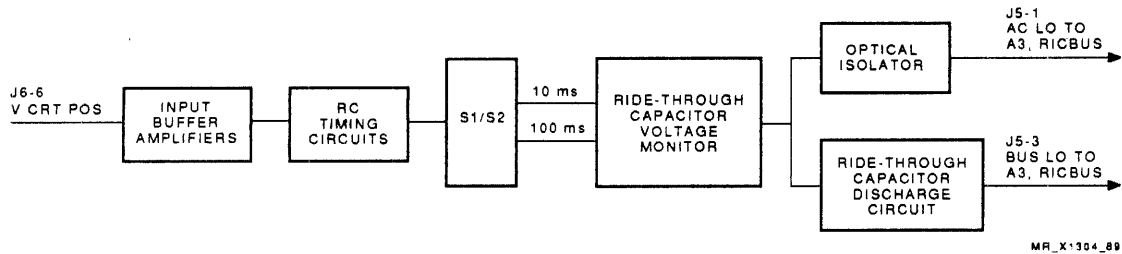
Figure 10–32   Ride-Through Capacitor Voltage Monitor

10.4.9.8 Output Overvoltage Monitor

The positive and negative output voltages (V OUT POS and V OUT NEG) are monitored by a pair of buffer amplifiers driving a differential amplifier (454388100, 6-7). These circuits provide input for:

- Output voltage regulation through V OUT to PC2, modifying the PWM module operating characteristics

- Output overvoltage detection through the output overvoltage function (OUT OVVLT)

- Output disconnect switch (A12) status

The differential amplifier output is applied to an overvoltage filter circuit that also serves as a coupling circuit into a comparator (Figure 10–33). An input representing the load voltage (V LOAD POS and V LOAD NEG from the high voltage attenuator PC15 on the A13 module) is also applied to the overvoltage filter. The filter allows short-term overvoltages but prohibits longer term overvoltages.

The filter output couples an overvoltage condition into the comparator that sets the output overvoltage latch (OUT OVVLT). OUT OVVLT is applied to the shutdown logic, and initiates an ESD, turning on DS6 (OUT OVVLT) on the alarm panel.
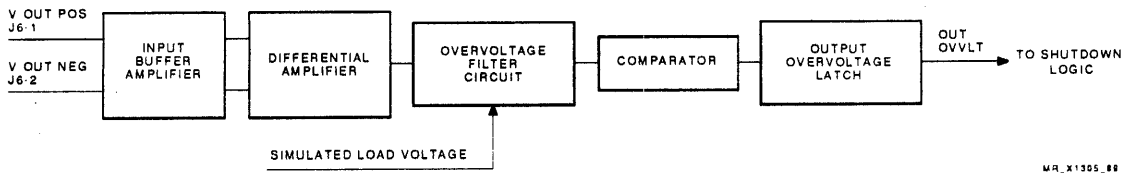
Figure 10–33   Output Overvoltage Monitor

10.4.9.9 Leakage Current Detection

The output of the UPC is floating with respect to chassis ground. The positive and negative voltage outputs (V OUT POS and V OUT NEG) are nominally balanced with respect to ground. However, they become unbalanced when a leakage path exists. An unbalance monitor circuit is provided to detect leakage current to chassis ground (454388100, 6-7).

The V OUT POS and V OUT NEG buffer amplifier outputs are coupled to a summing amplifier and rectifier circuit (Figure 10–34). The amplifier/rectifier circuit output increases with an imbalance at its input. An output increase is detected in the following comparator, which sets the voltage unbalance latch (VOLT UNBAL). VOLT UNBAL is coupled into the shutdown logic, initiating an ISD, and enables its optical isolator to the RICBUS.

NOTE
This condition may also reflect a fault in the VAX 9000 system rather than a UPC fault.

10.4.10 Shutdown Logic

The shutdown logic (454388100, 7-7) is driven from the operating condition and alarm monitor circuits. The logic initiates one of the three following shutdown modes:

- **Emergency shutdown (ESD)** — This mode is initiated by the detection of any one of a set of fatal error conditions or the TOTAL OFF function. An ESD immediately trips the input circuit breaker (CB1), turning the UPC off.

- **Immediate shutdown (ISD)** — This mode is initiated by the detection of any one of a set of severe error conditions that cause a power-down sequence. When the sequence has completed, the input circuit breaker CB1 is tripped.

- **Automatic shutdown (ASD)** — This is the normal shutdown mode, which initiates a power-down sequence but does not trip the input circuit breaker CB1.

Table 10-7 lists the shutdown modes, associated error conditions, and the related LEDs. Figure 10-35 provides an overview of the shutdown logic (45438100, 7-7).
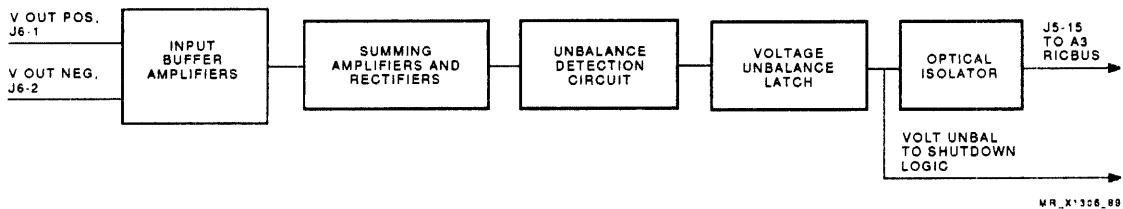
Figure 10-34   Leakage Current Detection

Table 10-7   Shutdown Modes and Related Conditions

Shutdown Mode	Error Condition	Associated LED
Emergency shutdown	Output overvoltage	DS6, OVVLT.
	Output overload	DS16, OVLD.
	±12 V alarm	DS17, ±12 V.
	Input overvoltage	DS25, IN OVVLT.
The TOTAL OFF function also initiates an ESD	NA	NA.
Immediate shutdown	High temperature fault	HI T A (DS20), HI T A (DS21), HI T A (DS22). Also enable the THERM FAULT line on the RICBUS.
	Voltage unbalance	No associated LED. Enables the VOLT UNBAL line on the RICBUS.
Automatic shutdown	Normal shutdown mode	NA.

NOTE
The UPC off LED (DS9) is turned on and the UPC on LED (DS8) is turned off for all modes.

AUTOMATIC SHUTDOWN (ASD)

UPC OFF FUNCTION

UPC POWERED DOWN

IMMEDIATE SHUTDOWN (ISD)

POWER-
DOWN
CIRCUITS

HIGH TEMPERATURE FAULT (HI T FLT)
VOLTAGE UNBALANCE (VOLT UNBAL)

SEVERE
ERROR
LOGIC

UPC
POWERED
DOWN

CB1
SHUNT
TRIP
CIRCUIT

CB1
TRIPPED

EMERGENCY SHUTDOWN (ESD)

OUTPUT OVERVOLTAGE (OVVLT)
OUTPUT OVERLOAD (OVLD)
±12 V ALARM (±12 V)
INPUT OVERVOLTAGE (I OVVLT)

FATAL
ERROR
LOGIC

MR_X1307_89

Figure 10–35   Shutdown Logic Overview

During all power-down sequences (AC LO, BUS LO), a ride-through operation is initiated
to provide the normal kernel shutdown period.

An enabled TOTAL OFF function essentially initiates an ESD. The TOTAL OFF function
is connected directly into the power amplifier circuit (454408100, 2-2) that drives and
trips the CB1 shunt trip coil.

10.4.11 Input/Output Connector

Table 10-8 provides a summary of the major power and control I/O connectors.

Table 10-8 I/O Connector Summary

Connector	Module	Function	Description
J1	A1	AC input power	3-phase ac utility power input.
J2	A2	Auxiliary ac power output	3-phase ac auxiliary power to the kernel BBUs.
J3	A1	DC power output	Regulated 280 Vdc output.
J4	A3	Power control bus	Provides the remote power-on and power inhibit functions.
J5	A3	Power control bus	Connected in parallel with J4; same description.
J6	A3	Sequenced power control bus	Provides 1-second delay power-on functions.
J7	A3	Sequenced power control bus	Connected in parallel with J6; same description.
J8	A3	TOTAL OFF bus	Provides the TOTAL OFF function from the kernel.
J9	A3	TOTAL OFF bus	Connected in parallel with J8; same description.
J10	A3	RICBUS	Provides the UPC status and alarm interface to the kernel.
J11	A3	Power line monitor	Provides an auxiliary output for a power line monitor.

A
CPU RIC Interface Signals

The table in this appendix provides a cross-reference between the RIC module signal names and the signals for a specific RIC at the RIC backpanel. Only dynamic signals of special interest are shown; static signals are not shown. For instance, it is easy to determine from the RIC number which ID lines should be connected to ID RTN on the backpanel.

Table A-1 Model 210 CPU RIC Interface

	SCU Cabinet		CPA Cabinet	
RIC Signal Name	Bus B +5 V BBU RIC 42	Bus A +5 V RIC 32	Bus D -5.2 V RIC 14	Bus C -3.4 V RIC 24
STATUS 00	MOD OK 00 L	MOD OK 00 L	MOD OK 00 L	MOD OK 00 L
STATUS 01	MOD OK 01 L		MOD OK 01 L	MOD OK 01 L
STATUS 02			MOD OK 02 L	MOD OK 02 L
STATUS 03				
STATUS 04				
STATUS 05		AIR OK 4 L (SC6)		AIR OK 4 L (SC3)
STATUS 06			OVP BIAS OK 1 L (PSD-B2)	
STATUS 07				
STATUS 08		AIR OK 1 L (AF5)	AIR OK 1 L (AF4)	AIR OK 1 L (AF2)
STATUS 09		AIR OK 2 L (SC5)	AIR OK 2 L (SC4)	AIR OK 2 L (SC2)
STATUS 10		CROWBAR FIRED C H	CROWBAR FIRED B H	CROWBAR FIRED A H
STATUS 11		FIRED FIRST C (Bus A or bus B)	FIRED FIRST B (Bus D)	FIRED FIRST A (Bus C)
STATUS 12			CROWBAR READY L	
STATUS 13	BIAS OK L (PSD-B1)	BIAS OK 1 L (PSD-A1)	BIAS OK L (PSD-A2)	BIAS OK L (PSC-A2)
STATUS 14				

Table A-1 (Cont.)   Model 210 CPU RIC Interface

	SCU Cabinet		CPA Cabinet	
RIC Signal Name	Bus B +5 V BBU RIC 42	Bus A +5 V RIC 32	Bus D -5.2 V RIC 14	Bus C -3.4 V RIC 24
STATUS 15		AIR OK 3 L (AF6)		AIR OK 3 L (AF3)
MEAS 00	THERM FAN 1 (T6)	THERM FAN 1 (T4)	THERM FAN 1 (T3)	THERM FAN 1 (T1)
MEAS 01		THERM FAN 2 (T5)		THERM FAN 2 (T2)
MEAS 02				
MEAS 03				
GRP LO OUT H			REM SHUTDN H (RIC 24)[1]	
GRP LO OUT RTN			GND	
REM SHUTDN H	GND	GND	GND	GRP LO OUT H (RIC 14)[1]
GND CUR +			GND CUR +	
GND CUR -			GND CUR -	

[1]GRP LO OUT H on RIC 14 is shorted to REM SHUTDN H on RIC 24 to allow the detection of a group low condition on the -5.2 Vdc bus to shut down the -3.4 Vdc bus.

B

Model 210 OCP Codes

The tables in this appendix consist of the OCP codes generated for total off conditions. Tables B-1 through B-7 are individual listings for the PEM, SPU, and each RIC. In these tables, the least significant bit of the OCP code indicates the RIC number. Table B-8 is a numerical listing of all of the OCP codes.

Table B-1 OCP Codes — PEM Generated

Code	Fault	Location	FRU
110	RIC 11[1]	SCU CAB BUS B	CPU RIC 11
120	RIC 12[1]	CPA CAB BUS J	CPU RIC 12
130	RIC 13[1]	CPB CAB BUS M	CPU RIC 13
140	RIC 21[1]	SCU CAB BUS C	CPU RIC 21
150	RIC 22[1]	CPA CAB BUS K	CPU RIC 22
160	RIC 23[1]	CPB CAB BUS N	CPU RIC 23
170	RIC 31[1]	CPA CAB BUS D	CPU RIC 31
180	RIC 41[1]	SCU CAB BUS A	CPU RIC 41
190	RIC 51[1]	IOA CAB	IO RIC 51
1A0	RIC 52[1]	IOB CAB	IO RIC 52
1B0	RIC 14[1]	CPA CAB BUS D	CPU RIC 14
1C0	RIC 15[1]	CPB CAB BUS F	CPU RIC 15
1D0	RIC 24[1]	CPA CAB BUS C	CPU RIC 24
1E0	RIC 25[1]	CPB CAB BUS E	CPU RIC 25
1F0	RIC 32[1]	SCU CAB BUS A	CPU RIC 32
1H0	RIC 42[1]	SCU CAB BUS B	CPU RIC 42
1J0	RIC 53[1]	IOA CAB	IO RIC 53
1K0	RIC 54[1]	IOB CAB	IO RIC 54
200	BI BAD	SPU BI backpanel	An SPU BI module
210	RIC 11 off line	SCU CAB BUS B	CPU RIC 11
220	RIC 12 off line	CPA CAB BUS J	CPU RIC 12

[1]An OCP code from this group indicates that the RIC identified by the code is missing from the list of expected RIC IDs, and that there were also one or more RICs having IDs not associated with the current configuration. The most likely explanation would be that the RIC is not correctly reading its ID code from the backpanel.

Table B–1 (Cont.)   OCP Codes — PEM Generated

Code	Fault	Location	FRU
230	RIC 13 off line	CPB CAB BUS M	CPU RIC 13
240	RIC 21 off line	SCU CAB BUS C	CPU RIC 21
250	RIC 22 off line	CPA CAB BUS K	CPU RIC 22
260	RIC 23 off line	CPB CAB BUS N	CPU RIC 23
270	RIC 31 off line	CPA CAB BUS D	CPU RIC 31
280	RIC 41 off line	SCU CAB BUS A	CPU RIC 41
290	RIC 51 off line	IOA CAB	IO RIC 51
2A0	RIC 52 off line	IOB CAB	IO RIC 52
2B0	RIC 14 off line	CPA CAB BUS D	CPU RIC 14
2C0	RIC 15 off line	CPB CAB BUS F	CPU RIC 15
2D0	RIC 24 off line	CPA CAB BUS C	CPU RIC 24
2E0	RIC 25 off line	CPB CAB BUS E	CPU RIC 25
2F0	RIC 32 off line	SCU CAB BUS A	CPU RIC 32
2H0	RIC 42 off line	SCU CAB BUS B	CPU RIC 42
2J0	RIC 53 off line	IOA CAB	IO RIC 53
2K0	RIC 54 off line	IOB CAB	IO RIC 54
2L0	SPM timeout	SPU backplane	SPU
300	Power loss	Loss of ac power	None
310	Key switch	Normal shutdown	None
320	Maintenance switch	CPU CAB 1	SPU shutdown
330	Total off request switch	IOA CAB	SPU shutdown
340	Breaker 1	–	Breaker 1 open
350	Breaker 2	–	Breaker 2 open
360	Breaker 1 + breaker 2	–	Breakers open
400	H7215 overtemp	SPU power supply	H7215 IOA CAB
900	Operator command to P1REG	RIC 41	–
Txx	Unidentified total off (xx = contents of TOFF register)	–	–

Table B–2   OCP Codes — RIC 14 Generated

Code	Fault	Location	FRU
40B	Overtemp 1	CPA CAB BUS D	Converter D0
41B	Overtemp 2	CPA CAB BUS D	Converter D1
42B	Overtemp 3	CPA CAB BUS D	Converter D2
43B–4FB	Spare overtemp codes	--	--
50B	Temp red zone T3	SCU CAB	Blower
51B	Thermistor open T3	SCU CAB	Thermistor
52B	Thermistor shorted T3	SCU CAB	Thermistor
53B–5EB	Spare thermistor codes	--	--
5FB	Data acquisiton failure	SCU CAB	RIC/BIAS
60B	Air flow 0 AF4	SCU CAB	Blower
61B	Air flow 1 SC4	SCU CAB	Blower
63B	Spare air flow code	--	--
64B	Air flow 0 and 1	SCU CAB	Blower
65B–6FB	Spare air flow codes	--	--
90B	Operator command to P1REG	RIC 14	--

Table B–3 OCP Codes — RIC 24 Generated

Code	Fault	Location	FRU
40D	Overtemp 1	CPA CAB BUS C	Converter C0
41D	Overtemp 2	CPA CAB BUS C	Converter C1
42D	Overtemp 3	CPA CAB BUS C	Converter C2
42D–4FD	Spare overtemp codes	–	–
50D	Temp red zone T1	CPA CAB	Blower
51D	Thermistor open T1	CPA CAB	Thermistor
52D	Thermistor shorted T1	CPA CAB	Thermistor
53D	Temp red zone T2	CPA CAB	Blower
54D	Thermistor open T2	CPA CAB	Thermistor
55D	Thermistor shorted T2	CPA CAB	Thermistor
56D–5ED	Spare thermistor codes	–	–
5FD	Data acquisiton failure	SCU CAB	RIC/BIAS
60D	Air flow 0 AF2	CPA CAB	Blower
61D	Air flow 1 SC2	CPA CAB	Blower
62D	Air flow 2 AF3	CPA CAB	Blower
63D	Air flow 3 SC3	CPA CAB	Blower
64D	Air flow 0, 1	CPA CAB	Blower
65D	Air flow 2, 3	CPA CAB	Blower
66D–6FD	Spare air flow codes	–	–
90D	Operator command to P1REG	RIC 24	–

Table B-4   OCP Codes — RIC 32 Generated

Code	Fault	Location	FRU
40F	Overtemp 1	SCU CAB BUS A	Converter A0
42F-4FF	Spare overtemp codes	--	—
50F	Temp red zone T4	SCU CAB	Blower
51F	Thermistor open T4	SCU CAB	Thermistor
52F	Thermistor shorted T4	SCU CAB	Thermistor
53F	Temp red zone T5	SCU CAB	Blower
54F	Thermistor open T5	SCU CAB	Thermistor
55F	Thermistor shorted T5	SCU CAB	Thermistor
56F-5EF	Spare thermistor codes	--	—
5FF	Data acquisiton failure	SCU CAB	RIC/BIAS
60F	Air flow 0 AF5	SCU CAB	Blower
61F	Air flow 1 SC5	SCU CAB	Blower
62F	Air flow 2 AF6	SCU CAB	Blower
63F	Air flow 3 SC6	SCU CAB	Blower
64F	Air flow 0, 1	SCU CAB	Blower
65F	Air flow 2, 3	SCU CAB	Blower
66F-6FF	Spare air flow codes	-	—
90F	Operator command to P1REG	RIC 32	—

Table B-5   OCP Codes — RIC 42 Generated

Code	Fault	Location	FRU
40H	Converter overtemp 1	SCU CAB BUS B	Converter B0
41H	Converter overtemp 2	SCU CAB BUS B	Converter B1
42H	Converter overtemp 3	SCU CAB BUS B	Converter B2
43H-4FH	Spare converter overtemp codes	–	–
50H	Temp red zone T6 (ambient)	Computer room	Customer air conditioning
51H	Thermistor open T6	SCU CAB	Thermistor
52H	Thermistor shorted T6	SCU CAB	Thermistor
53H-5EH	Spare thermistor codes	–	–
5FH	Data acquisiton failure	SCU CAB	RIC/BIAS
60H-6FH	Spare air flow codes	–	–
90H	Operator command to P1REG	RIC 42	–

Table B–6 OCP Codes — RIC 53 Generated

Code	Fault	Location	FRU
40J	Overtemp 1	IOA CAB	7215 -1
41J–4FJ	Spare overtemp codes	–	–
60J	Air flow AF1	IOA CAB	Blower IOA CAB
61J	Air flow SC1	IOA CAB	Blower IOA CAB
62J	Air flow 0 or 1	IOA CAB	Blower IOA CAB
63J–6FJ	Spare air flow codes	–	–
70J	UPC thermal fault	UPC 1	UPC 1
71J	UPC voltage unbalance ind	UPC 1	UPC 1
73J–7FJ	Spare UPC codes	–	–
80J–8FJ	Spare codes	–	–
90J	Operator command to P1REG	RIC 53	–

Table B–7 OCP Codes — SPU Generated

Code	Fault	Location
90L	Total off sides 1 and 2	SPU
91L	Total off side 1	SPU
92L	Total off side 2	SPU

Table B–8 OCP Codes — Numerically Ordered

Code	Detected by	Fault	Location	FRU
110	PEM	RIC 11[1]	SCU CAB BUS B	CPU RIC 11
120	PEM	RIC 12[1]	CPA CAB BUS J	CPU RIC 12
130	PEM	RIC 13[1]	CPB CAB BUS M	CPU RIC 13
140	PEM	RIC 21[1]	SCU CAB BUS C	CPU RIC 21
150	PEM	RIC 22[1]	CPA CAB BUS K	CPU RIC 22
160	PEM	RIC 23[1]	CPB CAB BUS N	CPU RIC 23
170	PEM	RIC 31[1]	CPA CAB BUS D	CPU RIC 31
180	PEM	RIC 41[1]	SCU CAB BUS A	CPU RIC 41
190	PEM	RIC 51[1]	IOA CAB	IO RIC 51
1A0	PEM	RIC 52[1]	IOB CAB	IO RIC 52
1B0	PEM	RIC 14[1]	CPA CAB BUS D	CPU RIC 14
1C0	PEM	RIC 15[1]	CPB CAB BUS F	CPU RIC 15

[1]An OCP code from this group indicates that the RIC identified by the code is missing from the list of expected RIC IDs, and that there were also one or more RICs having IDs not associated with the current configuration. The most likely explanation would be that the RIC is not correctly reading its ID code from the backpanel.

Table B–8 (Cont.)   OCP Codes — Numerically Ordered

Code	Detected by	Fault	Location	FRU
1D0	PEM	RIC 24[1]	CPA CAB BUS C	CPU RIC 24
1E0	PEM	RIC 25[1]	CPB CAB BUS E	CPU RIC 25
1F0	PEM	RIC 32[1]	SCU CAB BUS A	CPU RIC 32
1H0	PEM	RIC 42[1]	SCU CAB BUS B	CPU RIC 42
1J0	PEM	RIC 53[1]	IOA CAB	IO RIC 53
1K0	PEM	RIC 54[1]	IOB CAB	IO RIC 54
200	PEM	BI BAD	SPU BI backpanel	An SPU BI module
210	PEM	RIC 11 off line	SCU CAB BUS B	CPU RIC 11
220	PEM	RIC 12 off line	CPA CAB BUS J	CPU RIC 12
230	PEM	RIC 13 off line	CPB CAB BUS M	CPU RIC 13
240	PEM	RIC 21 off line	SCU CAB BUS C	CPU RIC 21
250	PEM	RIC 22 off line	CPA CAB BUS K	CPU RIC 22
260	PEM	RIC 23 off line	CPB CAB BUS N	CPU RIC 23
270	PEM	RIC 31 off line	CPA CAB BUS D	CPU RIC 31
280	PEM	RIC 41 off line	SCU CAB BUS A	CPU RIC 41
290	PEM	RIC 51 off line	IOA CAB	IO RIC 51
2A0	PEM	RIC 52 off line	IOB CAB	IO RIC 52
2B0	PEM	RIC 14 off line	CPA CAB BUS D	CPU RIC 14
2C0	PEM	RIC 15 off line	CPB CAB BUS F	CPU RIC 15
2D0	PEM	RIC 24 off line	CPA CAB BUS C	CPU RIC 24
2E0	PEM	RIC 25 off line	CPB CAB BUS E	CPU RIC 25
2F0	PEM	RIC 32 off line	SCU CAB BUS A	CPU RIC 32
2H0	PEM	RIC 42 off line	SCU CAB BUS B	CPU RIC 42
2J0	PEM	RIC 53 off line	IOA CAB	IO RIC 53
2K0	PEM	RIC 54 off line	IOB CAB	IO RIC 54
2L0	PEM	SPM timeout	SPU backplane	SPU
300	PEM	Power loss	Loss of ac power	None
310	PEM	Key switch	Normal shutdown	None
320	PEM	SPU power switch	CPU CAB 1	SPU shutdown
330	PEM	Total off switch	IOA CAB	SPU shutdown
340	PEM	Breaker 1	–	Breaker 1 open

[1]An OCP code from this group indicates that the RIC identified by the code is missing from the list of expected RIC IDs, and that there were also one or more RICs having IDs not associated with the current configuration. The most likely explanation would be that the RIC is not correctly reading its ID code from the backpanel.

Table B-8 (Cont.) OCP Codes — Numerically Ordered

Code	Detected by	Fault	Location	FRU
350	PEM	Breaker 2	–	Breaker 2 open
360	PEM	Breaker 1 + breaker 2	–	Breakers open
400	PEM	H7215 overtemp	SPU power supply	H7215 IOA CAB
40B	RIC 14	Overtemp 1	CPA CAB BUS D	Converter D0
40D	RIC 24	Overtemp 1	CPA CAB BUS C	Converter C0
40F	RIC 32	Overtemp 1	SCU CAB BUS A	Converter A0
40H	RIC 42	Converter overtemp 1	SCU CAB BUS B	Converter B0
40J	RIC 53	Overtemp 1	IOA CAB	7215 -1
41B	RIC 14	Overtemp 2	CPA CAB BUS D	Converter D1
41D	RIC 24	Overtemp 2	CPA CAB BUS C	Converter C1
41H	RIC 42	Converter overtemp 2	SCU CAB BUS B	Converter B1
41J–4FJ	RIC 53	Spare overtemp codes	–	–
42B	RIC 14	Overtemp 3	CPA CAB BUS D	Converter D2
42D	RIC 24	Overtemp 3	CPA CAB BUS C	Converter C2
42D–4FD	RIC 24	Spare overtemp codes	–	–
42F–4FF	RIC 32	Spare overtemp codes	–	–
42H	RIC 42	Converter overtemp 3	SCU CAB BUS B	Converter B2
43B–4FB	RIC 14	Spare overtemp codes	–	–
43H–4FH	RIC 42	Spare converter overtemp codes	–	–
50B	RIC 14	Temp red zone T3	SCU CAB	Blower
50D	RIC 24	Temp red zone T1	CPA CAB	Blower
50F	RIC 32	Temp red zone T4	SCU CAB	Blower
50H	RIC 42	Temp red zone T6 (ambient)	Computer room	Customer air conditioning
51B	RIC 14	Thermistor open T3	SCU CAB	Thermistor
51D	RIC 24	Thermistor open T1	CPA CAB	Thermistor
51F	RIC 32	Thermistor open T4	SCU CAB	Thermistor
51H	RIC 42	Thermistor open T6	SCU CAB	Thermistor
52B	RIC 14	Thermistor shorted T3	SCU CAB	Thermistor
52D	RIC 24	Thermistor shorted T1	CPA CAB	Thermistor
52F	RIC 32	Thermistor shorted T4	SCU CAB	Thermistor
52H	RIC 42	Thermistor shorted T6	SCU CAB	Thermistor
53B–5EB	RIC 14	Spare thermistor codes	–	–
53D	RIC 24	Temp red zone T2	CPA CAB	Blower

Table B-8 (Cont.)   OCP Codes — Numerically Ordered

Code	Detected by	Fault	Location	FRU
53F	RIC 32	Temp red zone T5	SCU CAB	Blower
53H–5EH	RIC 42	Spare thermistor codes	–	–
54D	RIC 24	Thermistor open T2	CPA CAB	Thermistor
54F	RIC 32	Thermistor open T5	SCU CAB	Thermistor
55D	RIC 24	Thermistor shorted T2	CPA CAB	Thermistor
55F	RIC 32	Thermistor shorted T5	SCU CAB	Thermistor
56D–5ED	RIC 24	Spare thermistor codes	–	–
56F–5EF	RIC 32	Spare thermistor codes	–	–
5FB	RIC 14	Data acquisiton failure	SCU CAB	RIC/BIAS
5FD	RIC 24	Data acquisiton failure	SCU CAB	RIC/BIAS
5FF	RIC 32	Data acquisiton failure	SCU CAB	RIC/BIAS
5FH	RIC 42	Data acquisiton failure	SCU CAB	RIC/BIAS
60B	RIC 14	Air flow 0 AF4	SCU CAB	Blower
60D	RIC 24	Air flow 0 AF2	CPA CAB	Blower
60F	RIC 32	Air flow 0 AF5	SCU CAB	Blower
60H–6FH	RIC 42	Spare air flow codes	–	–
60J	RIC 53	Air flow AF1	IOA CAB	Blower IOA CAB
61B	RIC 14	Air flow 1 SC4	SCU CAB	Blower
61D	RIC 24	Air flow 1 SC2	CPA CAB	Blower
61F	RIC 32	Air flow 1 SC5	SCU CAB	Blower
61J	RIC 53	Air flow SC1	IOA CAB	Blower IOA CAB
62D	RIC 24	Air flow 2 AF3	CPA CAB	Blower
62F	RIC 32	Air flow 2 AF6	SCU CAB	Blower
62J	RIC 53	Air flow 0 or 1	IOA CAB	Blower IOA CAB
63B	RIC 14	Spare air flow code	–	–
63D	RIC 24	Air flow 3 SC3	CPA CAB	Blower
63F	RIC 32	Air flow 3 SC6	SCU CAB	Blower
63J–6FJ	RIC 53	Spare air flow codes	–	–
64B	RIC 14	Air flow 0 and 1	SCU CAB	Blower
64D	RIC 24	Air flow 0, 1	CPA CAB	Blower
64F	RIC 32	Air flow 0, 1	SCU CAB	Blower
65B–6FB	RIC 14	Spare air flow codes	–	–
65D	RIC 24	Air flow 2, 3	CPA CAB	Blower
65F	RIC 32	Air flow 2, 3	SCU CAB	Blower

Table B–8 (Cont.)   OCP Codes — Numerically Ordered

Code	Detected by	Fault	Location	FRU
66D–6FD	RIC 24	Spare air flow codes	–	–
66F–6FF	RIC 32	Spare air flow codes	–	–
70J	RIC 53	UPC thermal fault	UPC 1	UPC 1
71J	RIC 53	UPC voltage unbalance ind	UPC 1	UPC 1
73J–7FJ	RIC 53	Spare UPC codes	–	–
80J–8FJ	RIC 53	Spare codes	–	–
900	PEM	Operator command to P1REG	RIC 41	–
90B	RIC 14	Operator command to P1REG	RIC 14	–
90D	RIC 24	Operator command to P1REG	RIC 24	–
90F	RIC 32	Operator command to P1REG	RIC 32	–
90H	RIC 42	Operator command to P1REG	RIC 42	–
90J	RIC 53	Operator command to P1REG	RIC 53	–
90L	SPU	Total off sides 1 and 2	SPU	–
91L	SPU	Total off side 1	SPU	–
92L	SPU	Total off side 2	SPU	–
Txx	PEM	Unidentified total off (xx = contents of TOFF register)	–	–

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