

```

    :31689 ;HERE OFF A-FORK WHEN THERE IS A TRAP, INTERRUPT, OR CONSOLE REQUEST UP
    :31690 ;AND FPA OP-CODE IN IBO.
    :31691
    :31692
    U 1020, 0000,003C,0180,F800,0000,0020 :31693 1020: -----:
    :31694 J/020
    :31695
    U 1024, 0000,003C,0180,F800,0000,0024 :31696 1024: -----:
    :31697 J/024 ;TRACE TRAP PENDING
    :31698
    U 1028, 0000,003C,0180,F800,0000,0028 :31699 1028: -----:
    :31700 J/028
    :31701
    U 102C, 0000,003C,0180,F800,0000,002C :31702 102C: -----:
    :31703 J/02C
    :31704
    U 1030, 0000,003C,0180,F800,0000,0030 :31705 1030: -----:
    :31706 J/030 ;INTERNAL INTERRUPT REQUEST
    :31707
    U 1034, 0000,003C,0180,F800,0000,0034 :31708 1034: -----:
    :31709 J/034 ;HALT PENDING
    :31710 ;UNDO EXTRA PC ADVANCE
    :31711
    U 1038, 0000,003C,0180,F800,0000,0038 :31712 1038: -----:
    :31713 J/038 ;SBI INTERRUPT REQUEST
    :31714
    U 103C, 0000,003C,0180,F800,0000,003C :31715 103C: -----:
    :31716 J/03C ;ARITHMETIC TRAP
    :31717
    U 1060, 0000,003C,0180,F800,0000,0060 :31718 1060: ;00-----:
    :31719 J/060 ;STOPPED WITH TB MISS. GO FILL TB
    :31720
    U 1061, 0000,003C,0180,F800,0000,0061 :31721 1061: ;01-----:
    :31722 J/061 ;STOPPED WITH AN ERROR
    :31723
    U 1062, 0000,003C,0180,F800,0000,0062 :31724 1062: ;10-----:
    :31725 J/062 ;WAITING FOR DATA. LOOP ON IT
  
```

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:31726 .TOC " FPA Interface : ADDF2, ADDF3, SUBF2, SUBF3 - (REG,REG), (S^#,REG)"
:31727
:31728 :ASSUMPTIONS ARE: 1) DST SPECIFIER IN IBUF<01>
:31729 :
:31730 : 2) IF TWO OPERAND TYPE, NO MORE DATA NEEDED BY FPA
:31731 : IF THREE OPERAND TYPE, OPERAND IN D-REG FOR FPA
:31732
:31733
:31734 :ADDF2, SUBF2(REG, REG) AFORK ENTRY
:31735 1044: -----
:31736 RC[TO]_LA, : ACCEPT ACCEL RESULT IF RDY
:31737 J/XF.A.01 : TEST FOR FPA SYNC
:31738
:31739
:31740
:31741 :ADDF2, SUBF2 (S^#, REG) A-FORK ENTRY
:31742 1040: -----
:31743 RC[TO]_LA, : ACCEPT ACCEL RESULT IF RDY
:31744 J/XF.A.01 : TEST FOR FPA SYNC
:31745
:31746
:31747
:31748 :ADDF3, SUBF3 (*, REG, REG) B-FORK ENTRY
:31749 1244: -----
:31750 ID_D.SYNC,RC[TO]_LA,J/XF.A.01 : SEND LAST OPERAND IN DREG TO ACCEL
:31751
:31752
:31753
:31754 :ADDF3, SUBF3 (*, S^#, REG) B-FORK ENTRY
:31755 1240: -----
:31756 ID_D.SYNC,RC[TO]_LA,J/XF.A.01 : SEND LAST OPERAND IN DREG TO ACCEL
:31757
:31758 XF.A.01: -----
:31759 ALU R(SP1)+K[ZERO].RLOG, : SAVE REGISTER #
:31760 Q_ACCEL&SYNC,ACCEL? : ACCEPT FPA RESULT IF READY
:31761
:31762 =100
:31763 XF.A.02: 100-----
:31764 Q_ACCEL&SYNC,ACCEL?,J/XF.A.02 : ACCEPT FPA RESULT IF RDY
:31765
:31766 :101----- : ** GOT RESULT & NO EXCEPTION **
:31767 R(SP1) Q, : RESULT TO DST REG/ID<R>
:31768 LOAD.ACC.CC, : LOAD FPA CONDITION CODES INTO PSL
:31769 PC+2,CLR.IB0-1, : PREPARE FOR NEXT INSTRUCTION
:31770 ?J/EXITF.SP
:31771
:31772 :110----- : ** RESERVED OPERAND EXCEPTION **
:31773 LOAD.ACC.CC,J/XD.B.09 : LOAD FPA CONDITION CODES IN PSL<<C>>
:31774
:31775 :111----- : ** GOT RESULT & ARITH EXCEPT **
:31776 LOAD.ACC.CC, : LOAD INTO PSL FPA CONDITION CODES
:31777 PC_PC+2,CLR.IB0-1,J/OUTF.SP : PREPARE FOR NEXT INSTRUCTION
    
```

U 1044, 0000,003C,0180,F980,0000,14D2

U 1040, 0000,003C,0180,F980,0000,14D2

U 1244, 0000,007C,1580,BD80,0000,14D2

U 1240, 0000,007C,1580,BD80,0000,14D2

U 14D2, 0018,0658,19D8,F840,0000,13D4

U 13D4, 0000,067C,01D8,F800,0000,13D4

U 13D5, 4001,263C,0180,F8C5,5800,13E5

U 13D6, 0000,003C,0180,F800,1800,14EA

U 13D7, 4000,003C,0180,F805,5800,13E7

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:31778 =101
:31779 EXITF.SP:
:31780 ;101-----: FINISHED
U 13E5, F80C,003B,01F1,F857,139B,6000 :31781 IRD ; NEXT INSTRUCTION
:31782
:31783 OUTF.SP:;111-----: EXCEPTION
U 13E7, 0840,0038,0180,F800,1C00,14D3 :31784 D_RLOG.RIGHT ; REGET REGISTER #
:31785
:31786
:31787 RC[7]_K[.8] ; PRELOAD T7 WITH OVERFLOW CODE
:31788
:31789
:31790 Q_ID[PSL],SC_D(EXP)(A), ; BRANCH ON V BIT
U 14D4, 0811,1A38,3DF0,2D00,0088,72FC :31791 D_RC[T0],PSL.V? ; D GETS ORIGINAL DESTINATION
:31792
:31793 =1100 ;1100-----: UNDERFLOW
U 12FC, 0000,003C,01A8,F800,0000,14D6 :31794 Q_Q.LEFT,J/UNFL1 ; MOVE PSL<FU> TO BIT POSITION 7
:31795
:31796 =1110 ;1110-----: OVERFLOW
U 12FE, 0001,003C,0180,F8E8,0000,12B4 :31797 R(SC)_D,J/FLOAT.FAULT ; RESTORE DEST
:31798
:31799 ;1111-----:
U 12FF, F80C,003B,01F1,F857,139B,6000 :31800 IRD ;
:31801
:31802
:31803 UNFL1: ;-----:
U 14D6, 0019,2038,F580,F9B8,1408,74D8 :31804 STATE_Q(EXP),RC[7]_K[A] ; MOVE PSL<FU> TO STATE BIT 0
:31805
:31806 ;-----:
U 14D8, C000,173C,0180,F800,0000,132E :31807 STATE0? ; TEST FOR FU BIT SET
:31808
:31809 =1110 ;1110-----: FU NOT SET IGNORE UNDERFLOW, OUTPUT 0
U 132E, 0018,0038,1980,F8E8,0000,0062 :31810 R(SC)_K[ZERO],J/IRD ; LOAD DEST WITH ZERO
:31811
:31812 ;1111-----: FU SET
U 132F, 0001,003C,0180,F8E8,0000,12B4 :31813 R(SC)_D,J/FLOAT.FAULT ; RESTORE DEST

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```

:31814 =101
:31815 EXITF.PRN:
:31816 :101-----: FINISHED
U 13F5, F80C,003B,01F1,F857,139B,6000 :31817 IRD : NEXT INSTRUCTION
:31818
:31819 OUTF.PRN:
:31820 :111-----:
U 13F7, 0018,0038,0180,F9B8,0000,14D9 :31821 RC[T7]_K[.8] : PRELOAD T7 WITH OVERFLOW CODE
:31822
:31823 :-----: EXCEPTION
:31824 D RC[T0],Q_ID[PSL], : PREFETCH ORIGINAL CONTENTS OF DEST,FETCH PSL
U 14D9, 0810,1A38,3DF0,2D00,0000,133C :31825 PSL.V? : BRANCH ON V-BIT
:31826
:31827 =1100
:31828 :1100-----: UNDERFLOW
U 133C, 0000,003C,01A8,F800,0000,14DA :31829 Q_Q.LEFT,J/UNFL2 : MOVE PSL<FU> TO BIT POSITION 7
:31830 =1110
:31831 :1110-----: OVERFLOW
:31832 R(PRN) D, : RESTORE DEST
U 133E, 0001,003C,0180,F8D8,0000,12B4 :31833 J/FLOAT.FAULT :
:31834
:31835 :1111-----:
U 133F, F80C,003B,01F1,F857,139B,6000 :31836 IRD :
:31837
:31838 UNFL2: :
U 14DA, 0001,203C,0180,F800,1408,74DB :31839 STATE_Q(EXP) : MOVE PSL<FU> TO STATE BIT 0
:31840
:31841 :-----:
U 14DB, 0018,1738,F580,F9B8,0000,134E :31842 STATE0?,RC[T7]_K[.A] : TEST FOR FU BIT SET
:31843
:31844 =1110 :1110-----: FU NOT SET IGNORE UNDERFLOW, OUTPUT 0
:31845 R(PRN)_K[ZERO], : LOAD DEST WITH ZERO
U 134E, 0018,0038,1980,F8D8,0000,0062 :31846 J/IRD :
:31847
:31848 :1111-----: FU SET
U 134F, 0001,003C,0180,F8D8,0000,12B4 :31849 R(PRN) D, : RESTORE DEST
:31850 J/FLOAT.FAULT :
```

```

:31851 .TOC " FPA Interface : (ADD,SUBD,MULD,DIVD)(2,3) - (REG,REG), (S^#,REG)"
:31852
:31853 ;ASSUMPTIONS ARE: 1) DST SPECIFIER IN IBUF<01>
:31854 ; 2) IF TWO OPERAND TYPE, NO ADDITIONAL DATA NEEDED BY FPA
:31855 ; IF THREE OPERAND TYPE, LAST OPERAND FOR FPA IN D-REG
:31856
:31857
:31858 ;ADD2, SUBD2 (REG, REG) A-FORK ENTRY
:31859 1046: -----
U 1046, 0000,003C,0180,F980,0000,14DC :31860 RC[T0]_LA,J/DBL.SYNC ; Save dest. operand in case fault
:31861
:31862
:31863 ;DIV2, MULD2 (REG, REG) A-FORK ENTRY
:31864 1006: -----
U 1006, 0000,003C,0180,F980,0000,14DC :31865 RC[T0]_LA,J/DBL.SYNC ; Save dest. operand in case fault
:31866
:31867
:31868 ;ADD2, SUBD2 (S^#, REG) A-FORK ENTRY
:31869 1042: -----
U 1042, 0000,003C,0180,F980,0000,14DC :31870 RC[T0]_LA,J/DBL.SYNC ; Save dest. operand in case fault
:31871
:31872
:31873 ;DIV2, MULD2 (S^#, REG) A-FORK ENTRY
:31874 1002: -----
U 1002, 0000,003C,0180,F980,0000,14DC :31875 RC[T0]_LA,J/DBL.SYNC ; Save dest. operand in case fault
:31876
:31877
:31878 ;ADD3, SUBD3 (*, REG, REG) B-FORK ENTRY
:31879 1246: -----
U 1246, 0000,007C,1580,BD80,0000,14DC :31880 ID_D.SYNC,RC[T0]_LA,J/DBL.SYNC ; Send last operand to FPA
:31881 ; Save dest. operand in case fault
:31882
:31883 ;DIV3, MULD3 (*, REG, REG) B-FORK ENTRY
:31884 1206: -----
U 1206, 0000,007C,1580,BD80,0000,14DC :31885 ID_D.SYNC,RC[T0]_LA,J/DBL.SYNC ; Send last operand to FPA
:31886 ; Save dest. operand in case fault
:31887
:31888 ;ADD3, SUBD3 (*, S^#, REG) B-FORK ENTRY
:31889 1242: -----
U 1242, 0000,007C,1580,BD80,0000,14DC :31890 ID_D.SYNC,RC[T0]_LA,J/DBL.SYNC ; Send last operand to FPA
:31891 ; Save dest. operand in case fault
:31892
:31893 ;DIV3, MULD3 (*, S^#, REG) B-FORK ENTRY
:31894 1202: -----
U 1202, 0000,007C,1580,BD80,0000,14DC :31895 ID_D.SYNC,RC[T0]_LA,J/DBL.SYNC ; Send last operand to FPA
:31896 ; Save dest. operand in case fault
  
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7Z-ESOAA-124.0 : FPA .MIC [600,1204]
: 01W124.MCR 600,1204]
: FPA .MIC [600,1204]

MICRO2 1L(03)
FPA Interfacr

FPA Interface
14-Jan-82 15:30:16

G 1
14-Jan-82

Fiche 5 Frame G1

Sequence 830

Page 829

14-Jan-82 15:30:16 VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124
: (ADDD,SUBD,MULD,DIVD)(2,3) - (REG,REG), (S^#,REG)

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:31896 DBL.SYNC:
:31897 -----:
:31898 ALU R(SP1)+K[ZERO].RLOG, : SAVE REGISTER #
U 14DC, 0018,0658,19D8,F840,0000,1434 :31899 Q_ACCEL&SYNC,ACCEL? : ACCEPT FIRST FPA RESULT IF RDY
:31900
:31901
:31902 =100 :100-----: FPA result not ready
U 1434, 0000,067C,01D8,F800,0000,1434 :31903 Q_ACCEL&SYNC,ACCEL?,J/<.> : ACCEPT FIRST FPA RESULT IF RDY
:31904
:31905 :101-----: FPA result ready
U 1435, 0001,203C,0180,F8C0,1800,1456 :31906 R(SP1)_Q,LOAD.ACC.CC,J/DBL.SYNC2: Dest <- FPA result, PSL <- FPA<cc>
:31907
:31908 :110-----: Reserved operand or divide by 0
U 1436, 0000,003C,0180,F800,180C,14EA :31909 LOAD.ACC.CC,J/XD.B.C9 : LOAD FPA CONDITION CODES IN PSL<CC>
:31910
:31911 :111-----: FPA result ready
U 1437, 0001,203C,0180,F8C0,1800,1456 :31912 R(SP1)_Q,LOAD.ACC.CC : Dest <- FPA result, PSL <- FPA<cc>
:31913
:31914 =110
:31915 DBL.SYNC2:
:31916 :110-----: FPA result not ready
U 1456, 0000,067C,01D8,F870,0000,1456 :31917 LAB R(SP1+1), : Save 2nd half of dest operand
:31918 Q_ACCEL&SYNC,ACCEL?,J/<.> : Accept 2nd half of result if ready
:31919
:31920 :111-----: FPA result ready
U 1457, 4001,263C,0180,F8F5,4000,1425 :31921 R(SP1+1)_Q,PC_PC+2,CLR.IB0-1, : Accept data, setup for next inst.
:31922 ACCEL?,J7EXITD.SP : Go see if exception occurred
```

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:31923 =101
:31924 EXITD.SP::101-----: FINISHED
U 1425, F80C,003B,01F1,F857,139B,6000 :31925 IRD : NEXT INSTRUCTION
:31926
:31927 :111-----: EXCEPTION
U 1427, 0840,0038,0180,F800,1C00,14DD :31928 D_RLOG.RIGHT : REGET REGISTER #,
:31929
:31930 -----:
U 14DD, 0018,0038,0180,F9B8,0000,14DE :31931 RC[7]_K[.8] : PRELOAD ?7 WITH OVERFLOW CODE
:31932
:31933 -----:
:31934 SC_D(EXP)(A),LC_RC[0], : MOVE REG# TO SC,PSL TO G
U 14DE, 0001,1A3C,3DF0,2D00,0088,735C :31935 Q_ID[PSL],PSL.V? : BRANCH ON PSL<V> BIT
:31936
:31937 =1100
:31938 :1100-----: UNDERFLOW
U 135C, 0000,003C,01A8,F800,00C0,14E1 :31939 Q_Q.LEFT,J/UN.D : ROTATE Q
:31940
:31941 =1110
:31942 :1110-----: OVERFLOW
U 135E, 0010,0038,0580,F8E8,0084,94E0 :31943 R(SC)_LC,SC_SC+K[.1], : RESTORE DEST TO ORIGINAL VALUE
:31944 J/OVR.KJC
:31945
:31946 :1111-----:
U 135F, 0000,003C,0180,F800,0000,0062 :31947 J/IRD
:31948
:31949 OVR.KJC:-----:
U 14EC, 0000,003C,0180,F8E8,0000,12B4 :31950 R(SC)_LA,J/FLOAT.FAULT : RESTORE SECOND HALF OF DEST
:31951
:31952 UN.D:-----:
U 14E1, 0001,203C,0180,F800,1408,74E2 :31953 STATE_Q(EXP) : MOVE PSL<fu> TO STATE BIT ZERO
:31954
:31955 :-----:
U 14E2, 0018,1738,F580,F9B8,0000,136E :31956 STATEO?,RC[7]_K[A] : BRANCH ON STATEO
:31957
:31958 =1110
:31959 :1110-----: PSL<fu>=0, IGNORE UNDERFLOW
U 136E, 0018,0J38,1980,F8E8,0000,14E8 :31960 R(SC)_K[ZERO], : ZERO OUT DESTINATION
:31961 J/FT1
:31962
:31963 :1111-----: PSL<fu>=1, TAKE UNDERFLOW FAULT
U 136F, 0010,0038,0580,F8E8,0084,94E3 :31964 R(SC)_LC,SC_SC+K[.1] : RESTORE DEST
:31965
:31966 :-----:
U 14E3, 0000,003C,0180,F8E8,0000,12B4 :31967 R(SC)_LA, : RESTORE SECOND HALF OF DEST
:31968 J/FLOAT.FAULT
:31969
:31970 FT1:-----:
U 14E8, 0000,003C,0580,F800,0084,94E9 :31971 SC_SC+K[.1] : INC SC
:31972
:31973 :-----:
U 14E9, 0018,0038,1980,F8E8,0000,0062 :31974 R(SC)_K[ZERO],J/IRD : ZERO OUT SECOND HALF Of DEST

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:31973 .TOC " FPA Interface : ADDF2, SUBF2, MULF2, DIVF2 - ( * ,REG)"
:31974
:31975 :ASSUMPTIONS ARE: 1) DST REG IN PRN-REG
:31976 :
:31977 : 2) LAST OPERAND FOR FPA IN D-REG
:31978
:31979
:31980 :ADDF2, SUBF2 (*, REG) B-FORK ENTRY
:31981 122F: -----
:31982 ID_D.SYNC,RC[T0]_LA,J/XF.B.01 ; SEND LAST OPERAND IN DREG TO ACCEL
:31983
:31984
:31985
:31986 :MULF2: (*, REG) B-FORK ENTRY
:31987 1220: -----
:31988 ID_D.SYNC,RC[T0]_LA,J/XF.B.01 ; SEND LAST OPERAND IN DREG TO ACCEL
:31989
:31990
:31991
:31992 :DIVF2: (*, REG) B-FORK ENTRY
:31993 1221: -----
:31994 ID_D.SYNC,RC[T0]_LA,J/XF.B.01 ; SEND LAST OPERAND TO FPA
:31995
:31996
:31997
:31998 =100
:31999 XF.B.01: :100-----
:32000 Q_ACCEL&SYNC,ACCEL?,J/XF.B.01 ; ACCEPT FPA RESULT IF RDY
:32001
:32002 :101----- ** GOT RESULT & NO EXCEPTION **
:32003 R(PRN) Q, ; RESULT TO DST REG/PRN
:32004 LOAD.ACC.CC, ; LOAD FPA CONDITION CODES INTO PSL
:32005 PC_PC+1,CLR.IB.OPC, ; SETUP FOR NEXT INSTRUCTION
:32006 ACCEL?,J/EXITF.PRN ;
:32007
:32008 ; 0----- ** RESERVED OPERAND EXCEPTION **
:32009 L D.ACC.CC,J/XD.B.09 ;
:32010
:32011 :111----- ** GOT RESULT & ARITH EXCEPT **
:32012 D Q,Q ID[PSL], ;
:32013 LOAD.ACC.CC, ; LOAD INTO PSL FPA CONDITION CODES
:32014 PC_PC+1,CLR.IB.OPC,J/OUTF.PRN ; SETUP FOR NEXT INSTRUCTION
  
```

U 122F, 0000,007C,1580,BD80,0000,1464

U 1220, 0000,007C,1580,BD80,0000,1464

U 1221, 0000,007C,1580,BD80,0000,1464

U 1464, 0000,067C,01D8,F800,0000,1464

U 1465, C001,263C,0180,F8DC,5800,13F5

U 1466, 0000,003C,0180,F800,1800,14EA

U 1467, CC00,003C,3DF0,2C04,5800,13F7


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:32015 .TOC " FPA Interface : ADD2, SUBD2, MUL2, DIVD2 - ( * ,REG)"
:32016
:32017 :ASSUMPTIONS ARE: 1) DST REG/PRN & PRN+1
:32018 : 2) LAST OPERAND FOR FPA IN D-REG
:32019
:32020
:32021 :ADD2, SUBD2 (*, REG) B-FORK ENTRY
:32022 122E: -----
U 122E, 0000,007C,1580,BC58,0000,1474 :32023 ID_D.SYNC,LAB_R(PRN),J/XD.B.01 ; SEND LAST OPERAND/D-REG TO FPA
:32024
:32025
:32026 :MUL2: (*, REG) B-FORK ENTRY
:32027 1228: -----
U 1228, 0000,007C,1580,BC58,0000,1474 :32028 ID_D.SYNC,LAB_R(PRN),J/XD.B.01 ; SEND LAST OPERAND/D-REG TO FPA
:32029
:32030
:32031 :DIVD2: (*, REG) B-FORK ENTRY
:32032 1229: -----
U 1229, 0000,007C,1580,BC58,0000,1474 :32033 ID_D.SYNC,LAB_R(PRN),J/XD.B.01 ; SEND LAST OPERAND TO FPA
:32034
:32035 =100
:32036 XD.B.01:
:32037 :100-----; ** NO FPA RESULT **
:32038 Q ACCEL&SYNC,RC[TO]_LA,
:32039 ACCEL?,J/XD.B.01 ; ACCEPT FIRST FPA RESULT IF RDY
:32040
:32041 :101-----; ** GOT RESULT **
:32042 R(PRN)_Q,LOAD.ACC.CC,J/XD.B.05 ; FPA RESULT TO R/PRN, GET CC'S
:32043
:32044 :110-----; ** RESERVED OPERAND EXCEPTION **
:32045 LOAD.ACC.CC,J/XD.B.09
:32046
:32047 :111-----; ** GOT RESULT **
:32048 R(PRN)_Q,LOAD.ACC.CC ; FPA RESULT TO R/PRN, GET CC'S
:32049
:32050 =110
:32051 XD.B.05:;110-----; ** 2ND RESULT NOT RDY **
:32052 Q ACCEL&SYNC,LAB_R(PRN+1),
:32053 ACCEL?,J/XD.B.05 ; ACCEPT 2ND RESULT OPERAND IF RDY
:32054
:32055 :111-----; ** GOT 2ND FPA RESULT **
:32056 R(PRN+1) Q,PC_PC+1,CLR.IB.OPC, ; FPA RESULT TO R/PRN+1
:32057 ACCEL?,J7EXITD.PRN
:32058
:32059
:32060 :Reserved floating operand or divide by zero
:32061 XD.B.09:;
:32062 PSL.V? ; See which it is
:32063
:32064 =110* :110*-----; ** RSVD FLT OPERAND **
:32065 J/RSVOPR
:32066
:32067 :111*-----; ** DIVIDE BY ZERO **
U 108E, 0018,0038,D980,F9B8,0000,12B4 :32068 RC[7]_KC.9],J/FLOAT.FAULT
    
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:32069 =101
:32070 EXITD.PRN:;101-----: FINISHED
U 1545, F80C,003B,01F1,F857,139B,6000 :32071 IRD : NEXT INSTRUCTION
:32072
:32073 :111-----: EXCEPTION
U 1547, 0018,0038,0180,F9B8,0000,14EB :32074 RC[T7]_K[E.8] : PRELOAD T7 WITH OVERFLOW CODE
:32075
:32076 :-----:
:32077 LC RC[T0],Q_ID[PSL], : Q GETS PSL
:32078 PSC.V? : BRANCH ON V BIT
:32079
:32080 =1100
:32081 :1100-----: UNDERFLOW
U 139C, 0000,003C,01A8,F800,0000,14ED :32082 Q_Q.LEFT,J/UN.D.1 : ROTATE Q
:32083
:32084 =1110
:32085 :1110-----: OVERFLOW
U 139E, 0000,003C,0180,F8E0,0000,14EC :32086 R(PRN+1)_LA,J/OVR.DPR : RESTORE SECOND HALF OF DEST
:32087
:32088 :1111-----:
U 139F, 0000,003C,0180,F800,0000,0062 :32089 J/IRD :
:32090
:32091 OVR.DPR:-----:
U 14EC, 0010,0038,0180,F8D8,0000,12B4 :32092 R(PRN)_LC,J/FLOAT.FAULT : RESTORE FIRST HALF OF DEST
:32093
:32094 UN.D.1:-----:
U 14ED, 0001,203C,0180,F800,1408,74EE :32095 STATE_Q(EXP) : MOVE PSL<fu> TO STATE BIT ZERO
:32096
:32097 :-----:
U 14EE, 0018,1738,F580,F9B8,0000,13AE :32098 STATE0?,RC[T7]_K[E.A] : BRANCH ON PSL<fu> BIT
:32099
:32100 =1110
:32101 :1110-----: PSL<fu>=0,IGNORE UNDERFLOW
U 13AE, 0018,0038,1980,F8D8,0000,14F1 :32102 R(PRN)_K[ZERO], : ZERO OUT DEST
:32103
:32104 :1111-----: PSL<fu>=1,TAKE UNDERFLOW FAULT
U 13AF, 0000,003C,0180,F8E0,0000,14F0 :32105 R(PRN+1)_LA : RESTORE DEST+1
:32106
:32107 :-----:
U 14F0, 0010,0038,0180,F8D8,0000,12B4 :32108 R(PRN)_LC,J/FLOAT.FAULT : RESTORE DEST
:32109
:32110 FT2:-----:
U 14F1, 0018,0038,1980,F8E0,0000,0062 :32110 R(PRN+1)_K[ZERO],J/IRD : ZERO OUT SECOND HALF OF DEST
    
```

ZZ-ES0AA-124.0 : FPA
: P1W124.MCR 600,1204]
: FPA .MIC [600,1204]

.MIC [600,1204]
MICRO2 1L(03)
FPA Interface

FPA Interface
14-Jan-82 15:30:16

L 1
14-Jan-82

Fiche 5 Frame L1

Sequence 835

Page 834

VAX11/780 Microcode : PCS 01, FPLA 0E, WCS124
: (ADDF,SUBF,MULF,DIVF)(2,3) - Memory destination

```
:32111 .TOC '' FPA Interface : (ADDF,SUBF,MULF,DIVF)(2,3) - Memory destination''
:32112
:32113 ;ASSUMPTIONS ARE: 1) IF DST/REG & TWO OPERAND TYPE, DST/PRN-REG
:32114 : 2) IF DST/MEM & TWO OPERAND TYPE, DST/VA
:32115 : 3) LAST OPERAND TO PASS TO FPA IN D-REG
:32116
:32117
:32118
:32119 ;ADDF2, SUBF2(*,*) & ADDF3, SUBF3(*,*,*) C-FORK ENTRY
:32120 138E: -----:
:32121 ID D.SYNC, : SEND LAST OPERAND TO FPA
:32122 CALL,IRO?,J/XF.C.02 : SET UP RETURN ADDR FOR ASPC RTN
:32123
:32124 13EE: :00-----: ** ASRC RETURN60, MEM DST **
:32125 D_ACCEL&SYNC,ACCEL?,J/XF.C.03 : ACCEPT FPA RESULT IF RDY
:32126
:32127 13EF: :01-----: ** ASRC RETURN61, REG DST **
:32128 Q ACCEL&SYNC,RC[TO]_LA, : ACCEPT FPA RESULT IF RDY
:32129 ACCEL?,J/XF.B.01 : MERGE INTO DST/PRN ROUTINE
:32130
:32131
:32132
:32133
:32134 ;MULF2(*,*), MULF3(*,*,*) C-FORK ENTRY
:32135 138F: -----:
:32136 ID D.SYNC,ALU_0(A),CLK.UBCC, : CLEAR ALU CONDITION CODES
:32137 J/XF.C.01 :
:32138
:32139
:32140
:32141
:32142 ;DIVF2(*,*), DIVF3(*,*,*) C-FORK ENTRY
:32143 138D: -----:
:32144 ID D.SYNC,ALU_0(A),CLK.UBCC, : CLEAR ALU CONDITION CODES
:32145 J/XF.C.01 :
```

U 138E, 0000,1B7D,1580,BC00,0000,138D

U 13EE, 0A00,067C,0180,F800,0000,1554

U 13EF, 0000,067C,01D8,F980,0000,1464

U 138F, 0003,007C,1580,BC00,0010,1218

U 138D, 0003,007C,1580,BC00,0010,1218

```

:32146 =00****0
:32147 XF.C.01:
:32148 :00****0-----:
U 1218, 0000,1B3D,0180,F800,0000,13BD :32149 CALL,IRO?,J/XF.C.02 ; SET UP RETURN FROM ASPC ROUTINE
:32150
:32151 =11****0
:32152 :11****0-----: ** ASRC RETURN60, MEM DST **
U 1278, 0A00,067C,0180,F800,0000,1554 :32153 D_ACCEL&SYNC,ACCEL?,J/XF.C.03 ; ACCEPT FPA RESULT IF RDY
:32154
:32155 :11****1-----: ** ASRC RETURN61, REG DST **
U 1279, 0000,067C,01D8,F980,0000,1464 :32156 Q_ACCEL&SYNC,RC[T0]_LA, ; ACCEPT FPA RESULT IF RDY
:32157 ACCEL?,J/XF.B.01 ; MERGE INTO DST/PRN ROUTINE
:32158
:32159
:32160 =1101
:32161 XF.C.02: :1101-----: ** TWO ADDRESS TYPE **
U 138D, 0A10,0678,0180,F938,0200,1554 :32162 D_ACCEL&SYNC,VA RC[T7], ; ACCEPT FPA DATA IF RDY
:32163 ACCEL?,J/XF.C.03 ;
:32164
:32165 :1111-----: ** THREE ADDRESS TYPE **
:32166 Q_IB.DATA, ; GET SPECIFIER DATA FROM ISTREAM
:32167 LAB_R(SP1), ; LOAD LATCHES FROM BASE SPECIFIER
:32168 CLR_IB.COND, ; DISCARD BASE OPERAND SPECIFIER
:32169 PC_PC+N, ; STEP PC OVER IT
U 13BF, F000,003F,01F0,F847,0000,0400 :32170 MCT/ALLOW_IB.READ, ; LET IB GE. NEEDED DATA
:32171 SUB/SPEC,J/ASPC.B ; EVALUATE THE SPECIFIER
:32172
:32173
:32174
:32175 =100
:32176 XF.C.03: :100-----: ** FPA DATA NOT RDY **
U 1554, 0A00,067C,0180,F800,0000,1554 :32177 D_ACCEL&SYNC,ACCEL?,J/XF.C.03 ;
:32178
:32179 :101-----: ** FPA RESULT ACCEPTED **
U 1555, 0000,063C,0180,F800,1800,1565 :32180 LOAD.ACC.CC,ACCEL?,J/EXITF.MEM ; LOAD PSL<CC>/ACCEL<CC>
:32181
:32182 :110-----: ** RSVD OPND + DIV CHR **
U 1556, 0000,003C,01E0,F800.1800,14EA :32183 LOAD.ACC.CC,Q_D,J/XD.B.09 ;
:32184
:32185 :111-----: ** GOT RESULT & ARITH EXCEPT **
U 1557, 0000,003C,0180,F800,1800,1567 :32186 LOAD.ACC.CC,J/OUTF.MEM ; ; LOAD PSL<CC>/ACCEL<CC>
```

```

:32187 =101
:32188 EXITF.MEM:;101-----: GOOD ANSWER
:32189 CACHE D[LONG],PC_PC+1, : WRITE ANSWER,INC PC,NEXT INSTRUCTION
U 1565, C000,003C,0180,3004,4000,0062 :32190 CLR.IB.OPC,J/IRD :
:32191
:32192 OUTF.MEM:
:32193 ;111-----: EXCEPTION
U 1567, 0018,0038,0180,F988,0000,14F2 :32194 RCLT7]_K[.8] : PREFETCH OVERFLOW CODE
:32195
:32196
:32197 Q_ID[PSL],PSL.V? : GET PSL,BRANCH ON V BIT
U 14F2, 0000,1A3C,3DF0,2C00,0000,13CC :32198
:32199 =1100 ;1100-----: UNDERFLOW
U 13CC, 0000,003C,01A8,F800,0000,14F3 :32200 Q_Q LEFT,J/UNFLMEM : ROTATE Q
:32201
:32202 =1110 ;1110-----: OVERFLOW
U 13CE, 0000,003C,0180,F800,0000,12B4 :32203 J/FLOAT.FAULT :
:32204
:32205 ;1111-----:
U 13CF, 0000,003C,0180,F800,0000,0062 :32206 J/IRD :
:32207
:32208 UNFLMEM:;-----:
U 14F3, 0001,203C,0180,F800,1408,74F8 :32209 STATE_Q(EXP) : STATE GETS PSL
:32210
:32211
:32212 STATEO?_RCLT7]_K[.A] : BRANCH ON STATEO (PSL<fu>)
U 14F8, 0018,1738,F580,F988,0000,13DE :32213
:32214 =1110 ;1110-----: PSL<fu>=0, IGNORE UNDERFLOW
U 13DE, 0818,0038,1980,F800,0000,14F9 :32215 D_K[ZERO],J/ENDITF : PREPARE TO ZERO OUT DEST
:32216
:32217 ;1111-----: 'SL<fu>=1, TAKE UNDERFLOW FAULT
U 13D, C000,003C,0180,F804,4000,12B4 :32218 PC_PC+1, : RESTORE DEST
:32219 CLR.IB.OPC,J/FLOAT.FAULT: NEXT INSTRUCTION
:32220
:32221 ENDITF:;-----:
U 14F9, C000,003C,0180,3004,4000,0062 :32222 CACHE D[LONG],PC_PC+1, : ZERO OUT DEST
:32223 CLR.IB.OPC,J/IRD :
    
```

```

:32224 .TOC '' FPA Interface : (ADDD,SUBD,MULD,DIVD)(2,3) - Memory destination''
:32225
:32226 ;ASSUMPTIONS ARE 1) IF DST/REG & TWO OPERAND TYPE, DST/PRN-REG
:32227 ; 2) IF DST/MEM & TWO OPERAND TYPE, DST/(RC[7])
:32228 ; 3) LAST OPERAND FOR FPA IN D-REG
:32229
:32230 ;ADDD2, SUBD2(*,*) & ADDD3, SUBD3(*,*,*) C-FORK ENTRY
:32231
:32232 138A: -----
:32233 ID D.SYNC, : SEND LAST OPERAND TO FPA
:32234 CALL, : SETUP RETURN ADDR FOR ASPC RTN
U 138A, 0000,1B7D,1580,BC00,0000,13FD :32235 IRO?, J/XD.C.02 : TEST FOR TWO ADDR TYPE
:32236
:32237 13EA: :00----- ** ASRC RETURN60, MEM DST **
:32238 D ACCEL&SYNC,RC[7]_D, : ACCEPT FPA RESULT IF RDY
U 13EA, 0A01,067C,0180,F9B8,0000,1574 :32239 ACCEL?, J/XD.C.03 :
:32240
:32241 13EB: :01----- ** ASRC RETURN61, REG DST **
:32242 RC[0] LA, :
:32243 Q ACCE[&SYNC, : ACCEPT FPA RESULT IF RDY
U 13EB, 0000,067C,01D8,F980,0000,1474 :32244 ACCEL?, J/XD.B.01 : MERGE INTO DST/PRN & PRN+1 ROUTINE
:32245
:32246 ;MULD2(*,*) & MULD3(*,*,*) C-FORK ENTRY
:32247
:32248 138C: -----
:32249 ID D.SYNC, : SEND LAST OPERAND TO FPA
:32250 ALU 0(A),CLK.UBCC, : CLEAR ALU CONDITION CODE
U 138C, 0003,007C,1580,BC00,0010,1288 :32251 J/XD.C.01 :
:32252
:32253 ;DIVD2(*,*) & DIVD3(*,*,*) C-FORK ENTRY
:32254
:32255 138B: -----
:32256 ID D.SYNC, : SEND LAST OPERAND TO FPA
:32257 ALU 0(A), CLK.UBCC, : CLEAR ALU CONDITIONS CODES
U 138B, 0003,007C,1580,BC00,0010,1288 :32258 J/XD.C.01 :
:32259
:32260 =00****0 ; CALL CONSTRAINT BLOCK
:32261
:32262 XD.C.01:-----
:32263 CALL, : SET UP RETURN FROM ASPC ROUTINE
U 1288, 0000,1B3D,0180,F800,0000,13FD :32264 IRO?, J/XD.C.02 :
:32265
:32266 =11****0:00----- ** ASRC RETURN60, MEM DST **
:32267 D ACCEL&SYNC,RC[7]_D, : ACCEPT FPA RESULT IF RDY
U 12E8, 0A01,067C,0180,F9B8,0000,1574 :32268 ACCEL?, J/XD.C.03 :
:32269
:32270 :01----- ** ASRC RETURN61, REG DST **
:32271 RC[0] LA, :
:32272 Q ACCE[&SYNC, : ACCEPT FPA RESULT IF RDY
U 12E9, 0000,067C,01D8,F980,0000,1474 :32273 ACCEL?, J/XD.B.01 : MERGE INTO DST/PRN & PRN+1 ROUTINE
:32274 =;END
  
```

```
:32275 =1101 ;BRANCH ON NUMBER OF SPECIFIERS (BEN/ALU)
:32276
:32277 XD.C.02::00-----: ** TWO ADDRESS TYPE **
:32278 D ACCEL&SYNC, :
:32279 VA RC[T7], : ACCEPT FPA DATA IF RDY
U 13FD, 0A10,0678,C180,F938,0200,1574 :32280 ACCEL?, J/XD.C.03 :
:32281
:32282 :01-----: ** THREE ADDRESS TYPE **
:32283 Q IB.DATA, : GET SPECIFIER DATA FROM ISTREAM
:32284 LAB R(SP1), : LOAD LATCHES FROM BASE SPECIFIER
:32285 CLR IB.COND, : DISCARD BASE OPERAND SPECIFIER
:32286 PC PC+N, : STEP PC OVER IT
U 13FF, F000,003F,01F0,F847,0000,0400 :32287 MCT/ALLOW.IB.READ, : LET IB GET NEEDED DATA
:32288 SUB/SPEC,J/ASPC.B : EVALUATE THE SPECIFIER
:32289
:32290
:32291
:32292 =100 ;BRANCH ON FPA SYNC & FPA ERROR (BEN/ACCEL)
:32293
:32294 XD.C.03::00-----: ** FPA NOT FINISHED **
:32295 D ACCEL&SYNC, :
:32296 ACCEL?, J/XD.C.03 : ACCEPT FPA RESULT IF RDY
:32297
:32298 :01-----: ** GOT 1ST FPA RESULT **
:32299 Q D,VA VA+4, : STORE 1ST HALF OF RESULT
U 1574, 0A00,067C,0180,F800,0000,1574 :32300 MSC/LOAD.ACC.CC, : LOAD PSL<CC>/ACC<CC>
:32301 J/XD.C.05 :
:32302
:32303 :10-----: ** FPA RSVD OPND + DIV CK **
:32304 MSC/LOAD.ACC.CC, :
:32305 Q D, :
U 1575, 0000,003C,01EC,F803,1800,15B6 :32306 J7XD.B.09 :
:32307
:32308 :11-----: ** GOT IT & FPA EXCEPTION **
:32309 Q D,VA VA+4, : 1ST HALF OF RESULT TO MEM
U 1576, 0000,003C,01E0,F800,1800,14EA :32310 MSC/LOAD.ACC.CC : LOAD PSL<CC>/ACC<CC>
:32311
:32312 =110 ;BRANCH ON FPA SYNC (BEN/ACCEL)
:32313
:32314 XD.C.05::00-----: ** FPA NOT RDY **
:32315 D ACCEL&SYNC, : ACCEPT 2ND HALF IF RDY
U 1577, 0000,003C,01E0,F803,1800,15B6 :32316 ACCEL?, J/XD.C.05 :
:32317
:32318 :01-----: ** GOT 2ND HALF OF RESULT **
U 15B6, 0A00,067C,0180,F800,0000,15B6 :32319 ACCEL?, J/EXITD.MEM :
```

```

:32320 =101
:32321 EXITD.MEM::101-----: GOOD RESULT
:32322 CACHE_D[LONG], : WRITE SECOND PART OF ANSWER
:32323 J/EXTRA.D :
:32324
:32325 :111-----: EXCEPTION
:32326 Q_ID[PSL],PSL.V? : Q GETS PSL, BRANCH ON V BIT
:32327
:32328 =1100 :1100-----: UNDERFLOW
:32329 Q_Q.LEFT,J/UN.D.MEM : ROTATE Q
:32330
:32331 =1110 :1110-----: OVERFLOW
:32332 RC[7] K[.8], : LOAD OVERFLOW CODE
:32333 J/FLOAT.FAULT :
:32334
:32335 :1111-----:
:32336 J/IRD :
:32337
:32338 UN.D.MEM::-----:
:32339 STATE_Q(EXP) : STATE GETS PSL
:32340
:32341 :-----:
:32342 STATE0? : BRANCH ON PSL<fu>
:32343
:32344 =1110 :1110-----: PSL<fu>=0, IGNORE UNDERFLOW
:32345 D_K[ZERO],J/ENDITD : PREPARE TO ZERO OUT DEST
:32346
:32347 :1111-----: PSL<fu>=1 TAKE UNDERFLOW FAULT
:32348 PC_PC+1,CLR.IB.OPC, : NEXT INSTRUCTION
:32349 RC[7] K[A], : LOAD UNDERFLOW CODE
:32350 J/FLOAT.FAULT :
:32351
:32352 ENDITD: :-----:
:32353 CACHE_D[LONG] : ZERO OUT SECOND HALF OF DEST
:32354
:32355 :-----:
:32356 VA_RC[7] : RESET ADDRESS
:32357
:32358 :-----:
:32359 CACHE_D[LONG],PC_PC+1, : ZERO OUT FIRST HALF OF DEST
:32360 CLR.IB.OPC,J/IRD : PREPARE FOR NEXT INSTRUCTION
:32361
:32362 EXTRA.D: :-----:
:32363 VA_RC[7],D_Q :
:32364
:32365 :-----:
:32366 CACHE_D[LONG],PC_PC+1, :
:32367 CLR.IB.OPC,J/IRD :
    
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U 15D5, 00C0,003C,0180,3000,0000,150E

U 15D7, 0000,1A3C,3DF0,2C00,0000,145C

U 145C, 0000,003C,01A8,F800,0000,14FA

U 145E, 001,0038,0180,F988,0000,12B4

U 145F, 0000,003C,0180,F800,0000,0062

U 14FA, 0001,203C,0180,F800,1408,74FB

U 14FB, 0C00,173C,0180,F800,0000,146E

U 146E, 0818,0038,1980,F800,0000,14FC

U 146F, C018,0038,F580,F98C,4000,12B4

U 14FC, 0000,003C,0180,3000,0000,14FD

U 14FD, 0010,0038,0180,F938,0200,14FE

U 14FE, C000,003C,0180,3004,4000,0062

U 150E, 0C10,0038,0180,F938,0200,1510

U 1510, C000,003C,0180,3004,4000,0062

:32368 .TOC " FPA Interface : MULL2 - (*,REG)"

:32369

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:32371

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:32373

:32374

:32375

:32376

:32377

:32378

:32379

:32380

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:32400

:32401

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:32406

:32407

:32408

:32409

:32410

:32411

:32412

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:32414

:32415

:*****

:DESCRIPTION:

: THIS ROUTINE ACCEPTS THE MAGNITUDE PRODUCT OF THE MULR AND MULD(PROD)
: FROM THE FPA. SINCE THE FPA CREATES AN UNSIGNED 64 BIT PRODUCT USING
: 32 BIT SIGNED OPERANDS, THE CP MICRO-CODE MUST CORRECT THE RESULT BY
: SUBTRACTING OUT EFFECTS OF NEGATIVE SIGNS ON THE MAGNITUDE RESULT AND
: CREATE THE PROPER SIGNED RESULT, SET THE CONDITION CODES, AND TEST
: FOR OVERFLOW.

: THIS ROUTINE OVERLAPS SETUP FOR THE CORRECTION, EVALUATION OF THE 3RD
: SPECIFIER, AND DETERMINES WHICH CORRECTION SEQUENCE TO USE
: IN PARALLEL WITH THE FPA'S DOING THE MAGNITUDE MULTIPLY.
: IT SAVES THE MULR AND MULD(PROD) IN A FORM THAT CAN BE
: LATER USED AS SURTRAHEND OPERANDS TO CORRECT THE PRODUCT. IF THE
: MULTIPLY IS A MULL3, THE 3RD SPECIFIER IS EVALUATED USING THE ASPC ROUTINE.
: AND IT EXAMINES THE INPUT OPERAND SIGNS TO DETERMINE WHICH OF THE FOUR
: CORRECTION SEQUENCES IS REQUIRED FOR THE MULTIPLY BEING DONE.

:THE CORRECTIONS PERFORMED ARE:

- 1) SIGNS POSITIVE, NO CORRECTION
- 2) MULR(+), MULD/PROD(-): MAGNITUDE PRODUCT-MULR*(2**32)
- 3) MULR(-), MULD/PROD(+): MAGNITUDE PRODUCT-MULD/PROD*(2**32)
- 4) MULR(-), MULD/PROD(-): MAGNITUDE PRODUCT-MULD/PROD*(2**32)
-MULR*(2**32)

:MULL ENTRIES:

THE FOLLOWING SEVEN(7) ENTRIES INTO THE MULL INTERFACE ROUTINE ARE
SCATTERED THROUGH-OUT THE FOLLOWING MICRO-CODE :

- A-FORK: DIVF2,MULF2,MULL2(REG, REG)
DIVF2,MULF2,MULL2(S^#, REG)
- B-FORK: DIVF3, MULF3, MULL3(*, REG, REG)
DIVF3, MULF3, MULL3(*, S^#, REG)
MULL2(*, REG)
- C-FORK: MULL2(*, *)
MULL3(*, *, *)

NOTES: '*' ANY SPECIFIER
'S^#' SHORT LITERIAL SPECIFIER
'REG' GENERAL REGISTER SPECIFIER

```
:32416 :MULL2(*,R) B-FORK ENTRY
:32417 :-----
:32418 :
:32419 :STATUS ON ENTRY:      1) PROD/GENERAL REG<PRN>
:32420 :                      2) MULR OPERAND IN D-REG
:32421 :                      3) PROD OPERAND IN LAB
:32422 :
:32423 :
:32424 122D: :-----
U 122D, 000F,0040,1580,BEF8,0000,1511 : R[R15] 0-LB,      : SAVE ADJUSTED PROD OPERAND
:32425 : ID_D.SYNC      : SEND LAST OPERAND TO FPA
:32426 :
:32427 :-----
:32428 :
:32429 :RC[TO] D-K[.1],   : SAVE (MULR-1) OPERAND
U 1511, 0019,0000,0580,F980,0030,1512 : N_AMX.Z_TST     : SAVE PROD SGN IN PSL<N>
:32430 :
:32431 :-----
:32432 :
:32433 :Q LA,             : PROD OPERAND TO Q-REG
U 1512, 0000,003C,01C0,F900,0000,12F8 : LC_RC[TO]      : LOAD LC WITH MULR-1
:32434 :
:32435 :
:32436 :
:32437 ==*0 :BRANCH ON FPA SYNC (BEN/ACCEL)
:32438 :
:32439 X.MUL.1:==*0-----:
:32440 :D ACCEL&SYNC,    : GET RESULT <31-00> IF RDY
U 12F8, 0A00,067C,0180,F800,0000,12F8 : ACCEL?, J/X.MUL.1
:32441 :
:32442 :-----
:32443 :==*1-----:
:32444 :Q ACCEL&SYNC,    : GET RESULT<63-32> IF RDY
U 12F9, 0000,0D7C,01D8,FA78,0000,15E3 : LAB R[R15],     : LOAD ADJUSTED PROD OPERAND IN LA
:32445 : Q31?           :
:32446 :
:32447 :
:32448 =011 :BRANCH ON Q31(BEN/SIGNS)
:32449 :
:32450 X.MUL3: :011-----: **MULD/PROD OPERAND SIGN=0 **
:32451 :R(PRN) D,        : RESULT TO DEST REG
:32452 :N&Z_ALD.V&C_0,  : SET N & Z PER RESULT, CLEAR C&V
U 15E3, 0001,1A3C,0180,F8D8,0050,1497 : PSL.N?, J/X.MUL5
:32453 :
:32454 :-----
:32455 : :111-----: **MULD/PROD OPERAND SGN =1 **
:32456 :R(PRN) D,        : RESULT TO DEST REG
:32457 :N&Z_ALD.V&C_0,  : SET N & Z PER RESULT, CLEAR C&V
U 15E7, 0001,1A3C,0180,F8D8,0050,14A7 : PSL.N?, J/X.MUL11
:32458 :
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:32459 =0111
:32460 X.MUL5:;0111-----: MULR SGN=0, MULD/PROD SGN=0
:32461 ALU Q, SET.CC(INST), : TEST UPPER HALF FOR OVERFLOW
:32462 Q ID[CES], : GET CP ERROR STATUS REGISTER
:32463 CLR.IB.OPC, PC PC+1, : SETUP FOR NEXT INSTR
:32464 D31?, J/X.MUL7 :
:32465
:32466 :111-----: MULR SGN=1, MULD/PROD SGN=0
:32467 ALU Q+LB+1, D_Q, : [RESULT<63-32>+(-MULD/PROD)+1]
:32468 SET.CC(INST), : TEST UPPER HALF FOR OVERFLOW
:32469 Q ID[CES], : GET CP ERROR STATUS REGISTER
:32470 CLR.IB.OPC, PC PC+1, : SETUP FOR NEXT INSTR
:32471 SIGNS?, J/X.MUL9 :
:32472
:32473 =110
:32474 X.MUL7: ;110-----: ** RESULT SGN=0 **
:32475 IRD : FINISHED
:32476
:32477 :111-----: **OVERFLOW, POS RESULT SIGN =1 **
:32478 D_Q.OR.K[.10] : SET EXCEPTION FLAG
:32479
:32480 X.MUL8: :-----:
:32481 ID[CES]_D, : RESTORE CES
:32482 SET.V, :
:32483 J/IRD : GO TAKE EXCEPTION IF ENABLED
:32484
:32485 =110
:32486 X.MUL9: :110-----: ** OVERFLOW, NEG RESULT SIGN =0 **
:32487 : SET EXCEPTION FLAG
:32488 Q_Q.OR.K[.10], D_Q, :
:32489 D.NE.0?, J/X.MUL10 :
:32490
:32491 :111-----: **GOOD RESULT**
:32492 IRD : FINISHED
:32493
:32494 =101
:32495 X.MUL10:;101-----: ** ZERO RESULT**
:32496 ID[CES]_D, : RESTORE CES REG TO ORIGINAL CONTENTS
:32497 ALU 0(A),N&Z_ALU.V&C_0, : SET PSL<Z>
:32498 J/IRD :
:32499
:32500 :111-----:
:32501 D_Q : CES CONTENTS WITH EXCEPTION FLAG SET
:32502
:32503 :-----:
:32504 ID[CES]_D, : RESTORE CES
:32505 SET.V, :
:32506 J/IRD : GO TAKE EXCEPTION IF ENABLED
  
```

U 1497, C001,ED3C,31F0,2C04,4070,15F6

U 149F, CC0D,ED10,31F0,2C04,4070,1606

U 15F6, F80C,003B,01F1,F857,139B,6000

U 15F7, 0819,2030,6580,F800,0000,1513

U 1513, 0000,003C,3180,3C00,0020,0062

U 1606, 0C19,2D30,65C0,F800,0000,1655

U 1607, F80C,003B,01F1,F857,139B,6000

U 1655, 0003,003C,3180,3C00,0050,0062

U 1657, 0C00,003C,0180,F800,0000,1520

U 1520, 0000,003C,3180,3C00,0020,0062

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        :32507 =0111 ;BRANCH ON PSL.N(BEN/PSL CC)
        :32508
        :32509 X.MUL11:;0111-----; ** MULR SGN=0, MULD/PROD SGN=1 **
        :32510 ALU Q-LC, D_Q, ; [RESULT<63-32>-(MULR-1)]
        :32511 SET.CC(INST), ; SET OVERFLOW IF RESULT<63-32>+1 NOT ZERO
        :32512 Q_ID[CES], ; GET CP ERROR/STATUS REG
        :32513 C[R.IB.OPC, ;
        :32514 PC PC+1, ;
        U 14A7, CC11,ED00,31F0,2C04,4070,1606 :32515 SIGNS?, J/X.MUL9 ;
        :32516
        :32517
        :32518 ;1111-----; ** MULR SGN=1, MULD/PROD SGN=1 **
        U 14AF, 0011,2008,01C0,F800,0000,1521 :32519 Q_Q-LC-1 ; [RESULT<63-32>-(MULR-1)-1]
        :32520
        :32521 -----;
        :32522 ALU Q+LB, ; [(RESULT<63-32>-MULR)+(-MULD/PROD)]
        :32523 SET.CC(INST), ; SET OVERFLOW IF RESULT<63-32> NOT ZERO
        :32524 Q_ID[CES], ; GET CP ERROR/STATUS REG
        :32525 C[R.IB.OPC, ;
        U 1521, C00D,ED14,31F0,2C04,4070,15F6 :32526 PC PC+1, ;
        :32527 D3T?, J/X.MUL7 ;
    
```

```
:32528 .TOC " FPA Interface : MULL2, MULL3 - Memory destination"  
:32529  
:32530 :  
:32531 : 1) IF (*,*), PROD ADDR/VA-REG  
:32532 : 2) MULR OPERAND/Q-REG  
:32533 : 3) PROD/MULD OPERAND IN D-REG  
:32534  
:32535 :MULL2,3(*,*) & (*,*,*) C-FORK ENTRY  
:32536 1381:-----  
:32537 ID D.SYNC, : SEND LAST OPERAND TO FPA  
U 1381, 001F,2040,1580,BEF8,0000,1410 :32538 R[R15]_0-D : SAVE 2'S COMPLEMENT OF MULD/PROD OPERAND  
:32539  
:32540 =00****0 : CALL CONSTRAINT BLOCK  
:32541  
:32542 :-----  
:32543 RC[0] Q-K[.1], : SAVE ADJUSTED MULR  
:32544 N.AMX.Z_TST, : SAVE MULR SGN IN 'N'  
:32545 Q.D, :  
U 1410, 0019,3B01,05E0,F980,0030,14BD :32546 CALL, : SET UP RETURN FROM ASPC ROUTINE  
:32547 IRO?, J/X.MUL21 :  
:32548  
:32549 =11****0  
:32550  
:32551 X.MUL19:;11****0----- : ** ASRC RETURN60, MEM DST **  
:32552 D.ACCEL&SYNC, : ACCEPT ANSWER<31-00>/FPA  
U 1470, 0A00,0D7C,0180,FA/8,0000,1633 :32553 LAB_R[R15], : GET -(MULD/PROD OPERAND)  
:32554 Q31?, J/X.MUL25 :  
:32555  
:32556 :;11****1----- : ** ASRC RETURN61, REG DST **  
U 1471, 0A00,007C,0180,FA78,0000,1522 :32557 D.ACCEL&SYNC, : ACCEPT ANSWER<31-00>/FPA  
:32558 LAB_R[R15] : GET -(MULD/PROD OPERAND)  
:32559  
:32560 :-----  
U 1522, 0000,0D7C,01D8,F900,0000,15E3 :32561 LC RC[0], : GET (MULR-1)  
:32562 Q.ACCEL&SYNC, : ACCEPT RESULT<63-32>/FPA  
:32563 Q31?, J/X.MUL3 : MERGE IN (*,R) FLOW  
:32564  
:32565  
:32566 =1101 ;BRANCH ON NUMBER OF SPECIFIERS (BEN/ALU)  
:32567  
U 148D, 0000,003C,0180,F800,0000,1523 :32568 X.MUL21:;1101----- : ** TWO ADDRESS TYPE **  
:32569 J/X.MUL23 : WAIT, FPA NOT READY  
:32570  
:32571 :;1111----- : ** THREE ADDRESS TYPE **  
:32572 Q_IB.DATA, : GET SPECIFIER DATA FROM ISTREAM  
:32573 LAB_R(SP1), : LOAD LATCHES FROM BASE SPECIFIER  
:32574 CLR_IB.COND, : DISCARD BASE OPERAND SPECIFIER  
:32575 PC_PC+N, : STEP PC OVER IT  
U 14BF, F000,003F,01F0,F847,0000,0400 :32576 MCT/ALLOW_IB.READ, : LET IB GET NEEDED DATA  
:32577 SUB/SPEC,J/ASPC.B : EVALUATE THE SPECIFIER  
:32578  
U 1523, 0000,003C,0180,F800,0000,1470 :32579 X.MUL23:;----- :  
:32580 J/X.MUL19 : WAIT, FPA NOT READY WITH RESULT
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:32581 =011 ;BRANCH ON Q31(BEN/SIGNS)
:32582
:32583 X.MUL25::011-----: ** MULD/PROD SGN=0 **
:32584 CACHE_D[LONG], : STORE RESULT<31-00> IN MEM DST
:32585 ALU D, N&Z ALU.V&C_0, : SET PSL N&Z /RESULT
:32586 Q ACCEL&SYNC, : GET RESULT<63-32>
:32587 LC RC[T0], : GET (MULR-1)
U 1633, 0001,1A7C,01D8,3100,0050,1497 :32588 PSE.N?, J/X.MUL5 :
:32589
:32590 :111-----: ** MULD/PROD OPERAND SGN=1 **
:32591 CACHE_D[LONG], : STORE RESULT<31-00> IN MEM DST
:32592 ALU D, N&Z ALU.V&C_0, : SET PSL N&Z /RESULT
:32593 Q ACCEL&SYNC, : GET RESULT<63-32>
U 1637, 0001,1A7C,01D8,3100,0050,14A7 :32594 LC RC[T0], : GET (MULR-1)
:32595 PSE.N?, J/X.MUL11 :
  
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:32596 .TOC " FPA Interface : (MULL, MULF, DIVF)(2,3) - (REG,REG) and (S^#,REG)
:32597
:32598 ;DIVF2,MULF2,MULL2 (REG,REG) A-FORK ENTRY
:32599 ;ENTRY STATUS: 1) MULF/PROD IN GPR<SP1>
:32600 ; 2) MULR OPERAND IN D-REG
:32601 ; 3) MULF/PROD OPERAND IN LA-REG
:32602
:32603 1004: -----:
U 1004, 001F,2600,0180,FAF8,0000,1673 :32604 R[R15]_0-D,ACCEL?,J/X.OML ; 2'S COMPLEMENT OF MULR OPERAND
:32605
:32606
:32607 ;DIVF2,MULF2,MULL2 (S^#, REG) A-FORK ENTRY
:32608 ;ENTRY STATUS: 1) MULF/PROD<SP1>
:32609 ; 2) MULR OPERAND IN Q-REG
:32610 ; 3) MULF/PROD OPERAND IN LA-REG
:32611
:32612 1000: -----:
U 1000, 0C1F,0600,0180,FAF8,0000,1673 :32613 R[R15]_0-Q,D_Q,ACCEL?,J/X.OML ; 2'S COMPLEMENT OF MULR OPERAND
:32614
:32615
:32616 ;DIVF3,MULF3,MULL3 (*,REG,REG) B-FORK ENTRY
:32617 ;ENTRY STATUS: 1) MULF/PROD IN GPR<SP1>
:32618 ; 2) MULR OPERAND IN D-REG
:32619 ; 3) MULF/PROD OPERAND IN LA-REG
:32620
:32621 1204: -----:
U 1204, 001F,2640,1580,BEF8,0000,1673 :32622 ID_D.SYNC,R[R15]_0-D, ; SEND MULR OPERAND, 2'S COMP OF MULR
:32623 ACCEL?,J/X.OML ;
:32624
:32625 =011
:32626 X.OML: :011-----:
U 1673, 0018,0000,0580,F980,0030,1528 :32627 RC[TO] LA-K[.1], ; SAVE MULF/PROD OPERAND -1
:32628 N_AMX.Z_TST,J/X.OML.1A ; SAVE MULF/PROD OPERAND SIGN IN PSL<N>
:32629
:32630 ;111-----:
U 1677, 0000,003C,0180,F980,0000,14D2 :32631 RC[TO] LA, ; *** NOT MULL, GO TO FLOATING RTN ***
:32632 J/XF.A.01 ; GET FPA RESULT IF READY,SAVE OPERAND
:32633
:32634
:32635 ;DIVF3,MULF3,MULL3 (*,S^#,REG) B-FORK ENTRY
:32636 ;ENTRY STATUS: 1) MULF/PROD IN GPR<SP1>
:32637 ; 2) MULR OPERAND IN D-REG
:32638 ; 3) MULF/PROD OPERAND IN Q-REG
:32639
:32640 1200: -----:
U 1200, 001F,2640,1580,BEF8,0000,1683 :32641 ID_D.SYNC,R[R15]_0-D,ACCEL? ; LAST OP TO ACC,2'S COMP OF MULR
:32642
:32643 =011
:32644 :011-----:
U 1683, 0019,2000,0580,F980,0030,1528 :32645 RC[TO] Q-K[.1],N_AMX.Z_TST, ; SAVE RESULT -1, PSL<N> <- SIGN
:32646 J/X.OML.1A ;
:32647
:32648 ;111-----:
U 1687, 0000,003C,0180,F980,0000,14D2 :32649 RC[TO] LA, ; *** MULF OR DIVF INSTRUCTION ***
:32649 J/XF.A.01 ; GET FPA RESULT IF READY,SAVE OPERAND

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:32650 X.OML.1A:
:32651 -----:
:32652 Q_D,D ACCEL&SYNC, : GET RESULT IF READY
U 1528, 0A00,067C,01E0,F900,0000,1314 :32653 LC_RC[TO],ACCEL?,J/X.OML.1 : GET MULD/PROD-1
:32654 ==*0
:32655 X.OML.1: :**0-----:
U 1314, 0A00,067C,0180,F800,0000,1314 :32656 D_ACCEL&SYNC,ACCEL?,J/X.OML.1 : GET RESULT <31-00> IF RDY
:32657
:32658 :**1-----:
U 1315, 0000,0D7C,01D8,FA78,0000,1693 :32659 Q_ACCEL&SYNC,LAB_R[R15],Q31? : GET RESULT<63-32>, LA_ADJUSTED MULR
:32660 =011
:32661 X.OML3: :011-----: ** MULR SIGN=0 **
:32662 R(SP1)_D,N&Z ALU.V&C_0, : RESULT TO DEST REG
U 1693, 0001,1A3C,0180,F8C0,0050,14C7 :32663 PSL.N?,J/X.OML5 :
:32664
:32665 :111-----: ** MULR SGN =1 **
:32666 R(SP1)_D,N&Z ALU.V&C_0. : RESULT TO DEST REG
U 1697, 0001,1A3C,0180,F8C0,0050,14D7 :32667 PSL.N?,J/X.OML11 :
:32668 =0111
:32669 X.OML5: :0111-----: MULD/PROD SGN=0, MULR SGN=0
:32670 ALU Q,SET.CC(INST), : TEST UPPER HALF FOR OVERFLOW
U 14C7, 4001,ED3C,31F0,2C05,4070,16B6 :32671 Q_ID[CES], : GET CP ERROR STATUS REGISTER
:32672 CLR.IB0-1,PC_PC+2,D31?,J/X.OML7 : SETUP FOR NEXT INSTR
:32673
:32674 :1111-----: MULD/PROD SGN=1, MULR SGN=0
:32675 ALU Q+LB+1,D_Q, : [RESULT<63-32>+(-MULR)+1]
:32676 SET.CC(INST), : TEST UPPER HALF FOR OVERFLOW
U 14CF, 4C0D,ED10,31F0,2C05,4070,1606 :32677 Q_ID[CES],CLR.IB0-1, : GET CP ERROR STATUS REGISTER
:32678 PC_PC+2,SIGNS?,J/X.MUL9 :
:32679 =110
:32680 X.OML7: :110-----: ** RESULT SGN=0 **
U 16B6, F80C,003B,01F1,F857,139B,6000 :32681 IRD : FINISHED
:32682
:32683 :111-----: **OVERFLOW, POS RESULT SIGN =1 **
U 16B7, 0819,2030,6580,F800,0000,1529 :32684 D_Q.OR.KC.10] : SET EXCEPTION FLAG
:32685
:32686 X.OML8: :-----:
U 1529, 0000,003C,3180,3C00,0020,0062 :32687 ID[CES]_D,SET.V,J/IRD : RESTORE CES
:32688 =0111
:32689 X.OML11: :0111-----: ** MULD/PROD SGN=0, MULR SGN=1 **
:32690 ALU Q-LC,D_Q, : [RESULT<63-32>- (MULD/PROD-1)]
:32691 SET.CC(INST), : SET V IF RESULT<63-32>+1 NOT ZERO
U 14D7, 4C11,ED00,31F0,2C05,4070,1606 :32692 Q_ID[CES],CLR.IB0-1, : GET CP ERROR/STATUS REG
:32693 PC_PC+2,SIGNS?,J/X.MUL9 :
:32694
:32695 :1111-----: ** MULD/PROD SGN=1, MULR SGN=1 **
U 14DF, 0011,2008,01C0,F800,0000,152A :32696 Q_Q-LC-1 : [RESULT<63-32>- (MULD/PROD-1)-1]
:32697
:32698 :-----:
:32699 ALU Q+LB, : [(RESULT<63-32>-MULD/PROD)+(-MULR)]
:32700 SET.CC(INST), : SET V IF RESULT<63-32> NOT ZERO
U 152A, 400D,ED14,31F0,2C05,4070,16B6 :32701 Q_ID[CES],CLR.IB0-1, : GET CP ERROR/STATUS REG
:32702 PC_PC+2,D31?,J/X.OML7 :
    
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:32703 .TOC " FPA Interface : POLYF, and POLYD"
:32704
:32705 ;THE FPA HANDLES DETECTION OF
:32706 ; A) UNDER & OVERFLOW
:32707 ; B) RESERVED OPERANDS ON COEFFICIENTS
:32708
:32709
:32710
:32711 ;POLYF C-FORK ENTRY
:32712 ; D-REG=DEGREE OPERAND
:32713 ; Q-REG=ARGUMENT OPERAND(ALREADY SENT TO FPA)
:32714
:32715 13C2: ;-----:
:32716 ; ALU.D.ANDNOT.K[.1F],WORD, ; TEST FOR DEGREE GREATER THAN 31
:32717 ; CLK.UBCC,D_Q,Q_D,J/X.POLY1 ; MOVE ARG TO D-REG, DEGREE TO Q-REG
:32718
:32719
:32720
:32721 ;POLYD C-FORK ENTRY
:32722 ; D-REG=DEGREE OPERAND
:32723 ; Q-REG=ARGUMENT OPERAND (L.O.), SENT TO FPA
:32724 ; RC[0]=ARGUMENT OPERAND (H.O.), SENT TO FPA
:32725
:32726 1385: ;-----:
:32727 ; ALU.D.ANDNOT.K[.1F],WORD, ; TEST DEGREE FOR GREATER THAN 31
:32728 ; CLK.UBCC,D_Q,Q_D ; MOVE ARG(L.O.) TO D, DEGREE TO Q-REG
:32729
:32730 ;-----:
:32731 ; D_RC[0] ; MOVE ARG(HO) INTO D-REG
:32732
:32733
:32734 =00*****
:32735 X.POLY1:;00*****-----:
:32736 ; CALL,ALU.D.MSC/CHK.FLT.OPR, ; TRAP IF ARG IS RESERVED OPERAND
:32737 ; D_Q,Z?,J7X.POLY3 ; WAS DEGREE RESERVED OPERAND?
:32738
:32739 =11*****:11*****-----: *** RETURN 60 FROM ASPC ***
:32740 ; RC[2] Q.OXT[BYTE],CLK.UBCC, ; SAVE DEGREE IN RC<2>, CHECK FOR 0
:32741 ; SUB/SPEC ; ADVANCE DATA TYPE TO SINGLE OR DOUBLE
:32742
:32743 1048: ;-----:
:32744 ; D[LONG] CACHE,RC[3]_D+K[.4], ; GET COEFFICIENT, ADVANCE TABLE ADDRESS
:32745 ; Z?,J/X.POLY7 ; WAS DEGREE=0?
:32746
:32747 =0
:32748 X.POLY3:;0-----: *** DEGREE GREATER THAN 31 ***
:32749 ; J/RVOPR ; TAKE RESERVED OPERAND TRAP
:32750
:32751 ;01-----: *** DEGREE OPERAND OK ***
:32752 ; Q_IB.DATA,LAB_R(SP1),LAB_R(SP1) ; EVALUATE TABLE ADDRESS SPECIFIER
:32753 ; CLR_IB.COND,PC_PC+N,
:32754 ; MCT/ALLOW_IB.READ,
:32755 ; SUB/SPEC,J/ASPC.B
    
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U 13C2, 0C19,4024,8DE0,F800,0010,101A

U 1385, 0C19,4024,8DE0,F800,0010,152B

U 152B, 0810,0038,0180,F900,0000,101A

U 101A, 0C01,013D,0180,F800,0800,132C

U 107A, 0003,A03F,0180,F990,0010,1048

U 1048, 0019,0114,1180,4198,0000,1334

U 132C, 0000,003C,0180,F800,0000,0106

U 132D, F000,003F,01F0,F847,0000,0400

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:32756 =0100
:32757 X.POLY5:;0100-----: *** BASIC SYNC LOOP ***
:32758 Q_RC[T3],ID_D.SYNC, : GET TABLE ADDRESS, COEFFICIENT TO FPA
U 14E4, 0010,0678,15C0,BD18,0000,14E4 :32759 ACCEL?,J/X.POLY5 : DID FPA TAKE IT?
:32760
:32761 :0101-----: *** FPA TOOK IT & LAST ONE OK ***
:32762 D[LONG] CACHE,RC[T3]_Q+K[.4], : GET NEXT COEFF, ADVANCE TABLE ADDRESS
U 14E5, 0019,2114,1180,4198,0000,1334 :32763 Z?,J/X.POLY7 : WAS DEGREE=0?
:32764
:32765 :0110-----: *** EXCEPTION ON LAST COEFFICIENT ***
:32766 Q_RC[T3],ID_D.SYNC, : GET TABLE ADDRESS, COEFFICIENT TO FPA
U 14E6, 0010,0678,15C0,BD18,0000,14E4 :32767 ACCEL?,J/X.POLY5 : DID FPA TAKE IT?
:32768
:32769 :0111-----: *** EXCEPTION ON LAST COEFFICIENT ***
:32770 LOAD.ACC.CC,SC.KE.1B], : LOAD PSL<CC>S, '27' TO SC
U 14E7, 0000,003D,ED80,F800,1884,7533 :32771 CALL,J/X.POLY40 : GO AND HANDLE EXCEPT
:32772
:32773 =1111 ;1111-----: *** RETURN9, UNDERFLOW RETURN ***
:32774 ACF/SYNC,D[LONG] CACHE, : TELL FPA TO PROCEED, GET NEXT COEFF
U 14EF, 0019,2154,1180,4198,0000,1334 :32775 RC[T3]_Q+K[.4],Z?,J/X.POLY7 : ADVANCE TABLE ADDRESS, WAS DEGREE=0?
:32776
:32777 =0
:32778 X.POLY7:;0-----: *** -GREE NEG ***
:32779 VA VA+4,Q_RC[T2], : ADVANCE TAB, GET DEGREE
U 1334, 0010,0E38,01C0,F913,0000,16BE :32780 INTERRUPT.REQ?,J/X.POLY9 : GO & CHECK FOR INTERRUPT REQUEST
:32781
:32782 :1-----: *** POLY DONE ***
U 1335, 0010,0838,01C0,F91B,C000,16D6 :32783 Q_RC[T3],VA_VA+4,DBL?,J/X.POLY20: Q GET TAB ADDR, ADVANCE TAB ADDR IN VA
:32784
:32785 =110
:32786 X.POLY9:;110-----: *** NO INTERRUPT ***
:32787 RC[T2]_Q-K[.1],CLK.UBCC,BYTE, : SET ALU.Z IF ZERO, DEC DEGREE BY ONE
U 16BE, 0019,A800,0580,F990,0010,16C6 :32788 DBL?,J/X.POLY11 : GO CHECK FOR POLYD
:32789
:32790 :111-----: *** INTERRUPT PENDING ***
U 16BF, 0000,003C,0180,F800,0000,121C :32791 J/POLY.INT :
:32792
:32793 =110
:32794 X.POLY11:
:32795 :110-----: *** SINGLE PRECISION ***
:32796 Q_RC[T3],ID_D.SYNC, : GET TAB ADDR OP, SEND COEF TO FPA
U 16C6, 0010,0678,15C0,BD18,0000,14E4 :32797 ACCEL?,J/X.POLY5 : DID IT GET IT?
:32798
:32799 :111-----: *** DOUBLE PRECISION ***
U 16C7, 0010,0678,15C0,BD18,0000,16CE :32800 Q_RC[T3],ID_D.SYNC,ACCEL? : GET TABLE ADD, SEND 1st HALF TO FPA
:32801
:32802 =110 ;110-----: WAIT FOR FPA RESPONSE
U 16CE, 0000,067C,1580,BC00,0000,16CE :32803 ID_D.SYNC,ACCEL?,J/<. > : GIVE FIRST HALF TO FPA (H.O.)
:32804
:32805 :111-----: *** FPA TOOK IT ***
U 16CF, 0019,2014,1180,4198,0000,152C :32806 D[LONG]_CACHE,RC[T3]_Q+K[.4] : INCREMENT TABLE ADDRESS
:32807
:32808
:32809 Q_RC[T3],VA_VA+4, : GET TABLE ADDR OPERAND
U 152C, 0010,0678,15C0,BD18,0000,14E4 :32810 ID_D.SYNC,ACCEL?,J/X.POLY5 : SEND COEFFICIENT TO FPA
    
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:32811 :POLY DONE
:32812 =110
:32813 X.POLY20:
:32814 :110-----: *** SINGLE PRECISION ***
:32815 ID D&NO.SYNC,POLY.DONE, : SEND CUEF TO FPA, SEND POLYDONE SIGNAL
U 16D6, 0000,06FC,1700,BC00,0000,14F4 :32816 ACCEL?,J/X.POLY21 : DID IT GET IT?
:32817
:32818 :111-----: *** DOUBLE PRECISION ***
U 16D7, 0000,06FC,1700,3C00,0000,16DE :32819 ID_D&NO.SYNC,POLY.DONE,ACCEL? : GIVE 1st HALF TO FPA, SEND DONE SIGNAL
:32820
:32821 =110 :110-----: WAIT FOR FPA RESPONSE
:32822 ID D&NO.SYNC,POLY.DONE, : GIVE 1st HALF TO FPA, SEND DONE SIGNAL
U 16DE, 0000,06FC,1700,BC00,0000,16DE :32823 ACCEL?,J/<.> :
:32824
:32825 :111-----: *** FPA TOOK IT ***
U 16DF, 0019,2014,1180,4198,0000,152D :32826 D[LONG]_CACHE,RC[3]_Q+K[.4] : INCREMENT TABLE ADDRESS
:32827
:32828
:32829 VA VA+4, : UPDATE VA-REG
:32830 Q RC[3], : GET TABLE ADDR OPERAND
U 152D, 0010,06F8,1740,BD1B,0000,14F4 :32831 ID D&NO.SYNC, : SEND COEFFICIENT TO FPA
:32832 POLY.DONE,ACCEL?,J/X.POLY21 : DID IT GET IT?
:32833
:32834 =0100
:32835 X.POLY21:
:32836 :0100-----: *** BASIC SYNC LOOP ***
:32837 Q RC[3], : GET TABLE ADDRESS
:32838 ID D&NO.SYNC, : SEND COEFFICIENT TO FPA
U 14F4, 0010,06F8,1740,BD18,0000,14F4 :32839 POLY.DONE, : SEND POLY DONE TO FPA
:32840 ACCEL?,J/X.POLY21 : DID FPA TAKE IT?
:32841
:32842 :0101-----: *** FPA TOOK IT & LAST ONE OK ***
:32843 D ACCEL&SYNC, : GET FIRST HALF OF RESULT
U 14F5, 0A10,0678,0180,F910,0010,1534 :32844 ALU RC[2],CLK.UBCC, : SET ALU.Z IF NO UNDERFLOW
:32845 ACCEL?,J/X.POLY31 : DID IT SET IT?
:32846
:32847 :0110-----: *** EXCEPTION ON LAST COEFFICIENT ***
:32848 Q RC[3], : GET TABLE ADDRESS
:32849 ID D&NO.SYNC, : SEND COEFFICIENT TO FPA
U 14F6, 0010,06F8,1740,BD18,0000,14F4 :32850 POLY.DONE, : SEND POLY DONE TO FPA
:32851 ACCEL?,J/X.POLY21 : DID FPA TAKE IT?
:32852
:32853 :0111-----: *** EXCEPTION ON LAST COEFFICIENT ***
U 14F7, 0000,003D,ED80,F800,1884,7533 :32854 LOAD.ACC.CC,SC K[.1B], : LOAD PSL<CC>S, '27' TO SC
:32855 CALL,J/X.POLY40 : GO AND HANDLE EXCEPT
:32856
:32857 =1111 :1111-----: *** RETURN, UNDERFLOW RETURN ***
U 14FF, 0010,0078,0180,F910,0010,1534 :32858 ACF/SYNC, : TELL FPA TO PROCEED
:32859 ALI_RC[2],CLK.UBCC,J/X.POLY31 : SET ALU.Z IF NO UNDERFLOW
  
```

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:32860 :POLY DONE CLEANUP ROUTINE
:32861 =0100
:32862 X.POLY31:
:32863 :0100-----: *** WAIT LOOP **
U 1534, 0A00,067C,0180,F800,0000,1534 :32864 D_ACCEL&SYNC,ACCEL?,J/X.POLY31 : ACCEPT H.O. RESULT
:32865
:32866 :0101-----: *** GOT H.O. RESUT & OK ***
U 1535, 0000,083C,0180,F800,1800,16E6 :32867 LOAD.ACC.CC,DBL?,J/X.POLY33 : LOAD PSL<CC>S
:32868
:32869 :0110-----: *** EXCEPTION ON LAST COEFFICIENT ***
U 1536, 0000,003D,ED80,F800,1884,7533 :32870 LOAD.ACC.CC,SC_K[.1B], : LOAD PSL<CC>S, '27' TO SC
:32871 CALL,J/X.POLY40 : GO AND HANDLE EXCEPT
:32872
:32873 :0111-----: *** EXCEPTION ON LAST COEFFICIENT ***
U 1537, 0000,003D,ED80,F800,1884,7533 :32874 LOAD.ACC.CC,SC_K[.1B], : LOAD PSL<CC>S, '27' TO SC
:32875 CALL,J/X.POLY40 : GO AND HANDLE EXCEPT
:32876
:32877 =1111 :1111-----: *** UNDERFLOW RETURN ***
U 153F, 0818,0038,19F8,F800,0050,16E6 :32878 D_K[ZERO],Q_0, : RESULTS GET ZERO
:32879 NZ_ALU.V&C_0,D_K[ZERO] : SET PSL<cc>'S
:32880
:32881 =110
:32882 X.POLY33:
U 16E6, 0000,063C,0180,F918,0000,1525 :32883 :110-----: *** SINGLE PRECISION ***
:32884 LC_RC[T3],ACCEL?,J/X.POLY37 : PREFETCH TABLE ADDRESS
:32885
:32886 :111-----: *** DOUBLE PRECISION ***
U 16E7, 0000,067C,01D8,F800,0000,16EE :32887 Q_ACCEL&SYNC,ACCEL? : ACCEPT 2ND HALF (L.O.)
:32888
:32889 =110 :110-----: *** WAIT LOOP ***
U 16EE, 0000,067C,01D8,F800,0000,16EE :32890 Q_ACCEL&SYNC,ACCEL?,J/<. > : ACCEPT 2ND HALF (L.O.)
:32891
:32892 :111-----: *** GOT 2ND HALF ***
U 16EF, 0000,063C,0180,F918,0000,1525 :32893 LC_RC[T3],ACCEL? : GET TAB ADD,OVERFLOW OR UNDERFLOW?
:32894
:32895 =0101
:32896 X.POLY37:
U 1525, 0010,0038,0180,FA98,0000,152E :32897 :0101-----: *** NO EXCEPTIONS ***
:32898 R[R3]_LC,J/X.POLY38 : LOAD TABLE ADDRESS
:32899
:32900 :0111-----: *** EXCEPTION ***
U 1527, 0000,003D,ED80,F800,0084,7533 :32901 SC_K[.1B],CALL,J/X.POLY40 :
:32902
:32903 =1111 :1111-----: RET HERE IF UNDERFLOW WITH PSL<FU>=0
U 152F, 0F01,203C,01F8,FA98,0000,152E :32904 R[R3]_Q,D_0,Q_0 : R3 GETS TABLE ADDRESS AND ZERO ANSWER
    
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    :32905 X.POLY38:
    :32906 -----:
U 152E, 0001,003C,0180,FA80,0000,1530 :32907 R[R0]_D : STORE FIRST PART OF ANSWER
    :32908 -----:
    :32909 :
U 1530, 0018,0838,1980,FA90,0000,16F6 :32910 R[R2]_K[ZERO],DBL? : ZERO REGISTER 2
    :32911 :
    :32912 =110 :110-----: SINGLE PRECISION
    :32913 R[R1]_K[ZERO], :
U 16F6, C018,0038,1980,FA8C,4000,0062 :32914 CLR.IB.OPC,PC_PC+1,J/IRD :
    :32915 :
    :32916 :111-----: DOUBLE PRECISION
U 16F7, 0018,0038,1980,FAA0,0000,1531 :32917 R[R4]_K[ZERO] : ZERO REGISTER 4
    :32918 :
    :32919 :
U 1531, 0018,0038,1980,FAA8,0000,1532 :32920 R[R5]_K[ZERO] : ZERO REGISTER 5
    :32921 :
    :32922 :
U 1532, C001,203C,0180,FA8C,4000,0062 :32923 R[R1]_Q, : STORE LOW ORDER OF RESULT
    :32924 CLR.IB.OPC,PC_PC+1.J/IRD :
  
```

```

:32925 ;POLY EXCEPTION SETUP ROUTINE
:32926 X.POLY40:
:32927 -----:
U 1533, 0000,003C,5DF0,2C00,0000,1538 : Q_ID[ACC.CS] ; GET FPA STATUS/CONTROL REG
:32928 -----:
:32929 -----:
U 1538, 0001,2024,0180,F800,0010,1539 : ALU_Q.ANDNOT.MASK,CLK.UBCC ; SET ALU<Z> IF NO RESERVED OPERAND
:32930 -----:
:32931 -----:
U 1539, 0000,013C,3DF0,2C00,0000,1340 : Q_ID[PSL],Z? ; GET PSL IN CASE IT IS UNDERFLOW
:32932 -----:
:32933 -----:
U 1340, 0000,003C,0180,F800,0000,0106 : =0 ;0-----: RESERVED OPERAND
:32934 -----:
:32935 -----:
:32936 -----:
U 1341, 0019,3A34,3180,F800,0082,154D : J/RSVOPR ;
:32937 -----:
:32938 -----:
:32939 -----:
U 154D, 0000,123C,0180,F800,0000,155D : :1-----: OVERFLOW OR UNDERFLOW
:32940 -----: SC_Q.AND.K[.40],PSL.V? ; ISOLATE PSL<fu> FOR UNDERFLOW
:32941 -----:
:32942 -----:
U 154F, 0018,0038,0180,F9B8,0000,12B4 : =1101 ;1101-----: UNDERFLOW
:32943 -----: EALU?,J/X.POLY43 ; SEE IF PSL<fu> IS SET
:32944 -----:
:32945 -----:
:32946 -----:
U 155D, 0818,0038,4580,F800,0000,153A : :111-----: OVERFLOW
:32947 -----: RC[7]_K[.8],J/FLOAT.FAULT ; LOAD OVERFLOW FAULT CODE
:32948 -----:
:32949 X.POLY43:
:32950 -----:
U 155F, 0018,0038,F580,F9B8,0000,12B4 : :1101-----: PSL<fu> IS 0
:32951 -----: D_K[.8000],J/X.POLY45 ; VALUE TO RESET ACC.CS REG
:32952 -----:
:32953 -----:
:32954 -----:
U 153A, 0010,0038,5D80,3D10,0010,153B : :111-----: PSL<fu> IS 1
:32955 -----: RC[7]_K[.A],J/FLOAT.FAULT ; LOAD UNDERFLOW CODE
:32956 -----:
:32957 X.POLY45:
:32958 -----:
U 153B, 0010,003A,01C0,F918,0000,0009 : -----: UNDERFLOW *****
:32959 -----: ALU_RC[?],CLK.UBCC, ; SET ALU.Z IF DEGREE EQ ZERO
:32960 -----: ID[ACC.CS]_D ; RESET FPA STATUS AND CNTL REG
:32961 -----:
:32962 -----:
: Q_RC[3],RETURN9 ; GET TABLE ADDRESS, RETURN TO CALLER
    
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:32963
:32964
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.TOC " FPA Interface : EMODF"  
-----  
:EMODF (54) MULR.RF, MULRX.RB, MUL.D.RF, INT.WL, FRACT.WF  
:*****  
:THIS ROUTINE PROVIDES THE CPU INTERFACE TO THE FPA WHICH IS USED  
:TO DO THE FRACTION MULTIPLY FOR EMODF. WHILE THE FPA IS  
:MULTIPLYING THE FRACTIONS, THIS ROUTINE ADDS THE  
:EXPONENTS, CHECKS FOR RESERVED OPERANDS, CHECKS FOR A ZERO RESULT,  
:ACCEPTS FROM THE FPA THE RESULTS OF THE FRACTION MULTIPLY, AND  
:SETS-UP THE STATE NEEDED TO MERGE INTO THE BASIC EMODF FLOWS.  
:IT THEN TRANSFERS CONTROL TO THE BASIC ROUTINE WHICH CONVERTS  
:THE RESULT INTO ITS RESPECTIVE INTEGER AND FRACTION PARTS.  
:EMODF ENTRY CONDITIONS:  
:-----  
:ENTER WITH Q = MULR.RF, D = MULRX.RB AT C.FORK.  
13C8:  
X.EMODF :-----  
ID D.SYNC, : SEND MULTIPLIER EXTENTION TO FPA  
ALD Q, :  
SC_Q(EXP), : MUL'IER EXP  
SS_ALU15, : MUL'IER SIGN  
CHR.FLT.OPR, : CHECK FOR -0  
CALL, INTERRUPT.REQ?, :  
J/SPEC : GO GET M'CAND  
13D8: :-----  
ID D.SYNC, : RETURN FROM 'SPEC'  
ALD D, : SEND M'CAND TO FPA  
FE_D(EXP), CLK.UBCC, : M'CAND EXP  
SS_SS.XOR.ALU15&SD_ALU15, : SS GETS RESULT SIGN  
CHR.FLT.OPR, : CHECK FOR -0  
J/X.EMDF1 :  
13DA: :-----  
ID D.SYNC, : RETURN FROM 'SPEC'  
ALD D, : SEND M'CAND TO FPA  
FE_D(EXP), CLK.UBCC, : M'CAND EXP  
SS_SS.XOR.ALU15&SD_ALU15, : SS GETS RESULT SIGN  
CHR.FLT.OPR : CHECK FOR -0  
=:END  
X.EMDF1 :-----  
SC_SC+FE, : SC GETS SUM OF EXP'S  
EALU? : M'IER OR M'CAND = 0?  
=1001 :00----- : MUL.D/PROD = 0 (M'IER IS 0)  
SC_K[ZERO], Q_0, D_0, :  
TRAP.ACC[1], : ABORT FPA  
J/X.EMDF5 :
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U 13C8, 0001,2E7D,1581,BC00,0888,637E

U 13D8, 0001,007C,1585,BC00,0918,753C

U 13DA, 0001,007C,1585,BC00,0918,753C

U 153C, 0000,123C,0180,F800,0080,9569

U 1569, 0F00,00BC,18F8,F800,0084,76FF

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:33018          :01-----: MULD/PROD .NE. 0
U 156B, 0000,003C,4180,F800,0084,B6FE :33019 SC SC-K[.80], : SAVE EXP WITH BIAS ADJUSTED
:33020 J/X.EMDF3 :
:33021
:33022          :10-----: MULD/PROD = 0 (M'IER, M'CAND ARE 0)
U 156D, 0F00,00BC,18F8,F800,0084,76FF :33023 SC K[ZERO], Q_0, D_0, :
:33024 TRAP.AC[C1], : ABORT FPA
:33025 J/X.EMDF5 :
:33026
:33027          :11-----: MULD/PROD = 0 (M'CAND IS 0)
U 156F, 0F00,00BC,18F8,F800,0084,76FF :33028 SC K[ZERO], Q_0, D_0, :
:33029 TRAP.AC[C1], : ABORT FPA
:33030 J/X.EMDF5 :
:33031 =;END
:33032
:33033 =110 ;BRANCH ON FPA SYNC SIGNAL(BEN/ACCEL)
:33034
:33035 X.EMDF3: :00-----:
U 16FE, 0A00,067C,0180,F800,0000,16FE :33036 D ACCEL&SYNC, : GET FRACTION IF READY(H.O.)
:33037 ACCEL?, J/X.EMDF3 :
:33038
:33039 X.EMDF5: :01-----:
:33040 SC SC-K[.80], : REMOVE BIAS FOR CONVERT RTN
:33041 RC[T1]_0,N&Z_ALU.V&C_0, : SET PSL<Z>
:33042 SD SS, Q_0, :
U 16FF, 0003,003C,41FC,F988,00D4,B02E :33043 J/EMDF.6 : MERGE INTO NORMAL EMOF FLOWS

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:33044 .TOC " FPA Interface : EMODD"
:33045
:33046 -----
:33047
:33048 :EMODD (74) MULR.RD, MULRX.RB, MULD.RD, INT.WL, FRACT.WD
:33049 :*****
:33050
:33051 :THIS ROUTINE PROVIDES THE CPU INTERFACE TO THE FPA WHICH IS USED
:33052 :TO DO THE FRACTION MULTIPLY FOR EMODD. WHILE THE FPA IS
:33053 :MULTIPLYING THE FRACTIONS, THIS ROUTINE ADDS THE
:33054 :EXPONENTS, CHECKS FOR RESERVED OPERANDS, CHECKS FOR A ZERO RESULT,
:33055 :ACCEPTS FROM THE FPA THE RESULTS OF THE FRACTION MULTIPLY, AND
:33056 :SETS-UP THE STATE NEEDED TO MERGE INTO THE BASIC EMODD FLOWS.
:33057 :IT THEN TRANSFERS CONTROL TO THE BASIC ROUTINE WHICH CONVERTS
:33058 :THE RESULT INTO ITS RESPECTIVE INTEGER AND FRACTION PARTS.
:33059
:33060 :EMODD ENTRY CONDITIONS:
:33061 -----
:33062 :ENTER WITH <RC 0, Q> = MULR.RD, D = MULRX.RB AT C.FORK.
:33063
:33064 1386:
:33065 -----
:33066 ID_D.SYNC, : SEND MULTIPLIER EXTENTION TO FPA
:33067 SC_RC[T0](EXP), : MUL'IER EXP
:33068 SS_ALU15, : MUL'IER SIGN
:33069 CHR.FLT.OPR, : CHECK FOR -0
:33070
:33071 =0**0* :-----
:33072 CALL, INTERRUPT.REQ?, :
:33073 J/EMODD.SPEC : GO GET M'CAND
:33074
:33075 =1**0* X.EMDD0: :-----
:33076 ID_D.SYNC, : RETURN WITH MULD IN <RC 2, D>
:33077 FE_SC, : SEND M'CAND TO FPA
:33078 SC_RC[T2](EXP), CLK.UBCC, : MUL'ER EXP TO FE-REG
:33079 SS_SS.XOR.ALU15&SD_ALU15, : M'CAND EXP
:33080 CHR.FLT.OPR, : SS GETS RESULT SIGN
:33081 J/X.EMDD1, : CHECK FOR -0
:33082
:33083 =1**1* :-----
:33084 D_RC[T2], Q_D : REFETCH FIRST HALF OF M'CAND
:33085
:33086 ID_D.SYNC, D_Q, : SEND FIRST HALF OF M'CAND
:33087 J/X.EMDD0
:33088
:33089 X.EMDD1: :-----
:33090 SC_SC+FE, SD_SS, : SC GETS SUM OF EXP'S
:33091 EACU? : M'IER OR M'CAND = 0?
    
```

U 1386, 0010,0078,1581,BD00,0883,10C8

U 10C8, 0000,0E3D,0180,F800,0000,137E

U 10D8, 0010,0078,1585,BD10,0993,153E

U 10DA, 0810,0038,01E0,F910,0000,153D

U 153D, 0C00,007C,1580,BC00,0000,10D8

U 153E, 0000,123C,0184,F800,0080,9589

```
:33092 =1001 :00-----: PROD = 0 (M'IER IS 0)
:33093 SC K[ZERO], D_0, Q_0, :
:33094 ALU_0(A), N&Z_ALU.V&C_0, : SET PSL<Z> AS ENTRY FLAG TO BASIC CODE
:33095 J/X.EMDD7 :
:33096
:33097 :01-----: PROD .NE. 0
:33098 SC SC-K[.80], : SAVE EXP WITH BIAS ADJUSTED
:33099 J/X.EMDD3 :
:33100
:33101 :10-----: PROD = 0 (M'IER, M'CAND ARE 0)
:33102 ALU_0(A), N&Z_ALU.V&C_0, : SET PSL<Z> AS ENTRY FLAG TO BASIC CODE
:33103 SC K[ZERO], D_0, Q_0, :
:33104 J/X.EMDD7 :
:33105
:33106 :11-----: PROD = 0 (M'CAND IS 0)
:33107 SC K[ZERO], D_0, Q_0, :
:33108 ALU_0(A), N&Z_ALU.V&C_0, : SET PSL<Z> AS ENTRY FLAG TO BASIC CODE
:33109 J/X.EMDD7 :
:33110 =:END
:33111
:33112 =110 ;BRANCH ON FPA SYNC SIGNAL(BEN/ACCEL)
:33113
:33114 X.EMDD3: :00-----:
:33115 ALU_0(A), N&Z_ALU.V&C_0, : SET PSL<Z> AS ENTRY FLAG TO BASIC CODE
:33116 D ACCEL&SYNC, : GET FRACTION IF READY(H.O.)
:33117 ACCEL?, J/X.EMDD3 :
:33118
:33119 :01-----:
:33120 ALU_0(A), N&Z_ALU.V&C_0, : SET PSL<Z> AS ENTRY FLAG TO BASIC CODE
:33121 Q ACCEL&SYNC, : GET FRACTION(L.O.)
:33122 ACCEL?, J/X.EMDD5 :
:33123
:33124 =110 ;BRANCH ON FPA SYNC SIGNAL(BEN/ACCEL)
:33125
:33126 X.EMDD5: :00-----:
:33127 Q ACCEL&SYNC, : GET FRACTION IF READY
:33128 ALU_0(A), N&Z_ALU.V&C_0, : SET PSL<Z> AS ENTRY FLAG TO BASIC CODE
:33129 ACCEL?, J/X.EMDD5 :
:33130
:33131 X.EMDD7: :01-----:
:33132 STATE K[.10], : SET FLAG FOR P/O OVERFLOW
:33133 RC[T2] Q, Q_0, : SAVE FRACTION (L.O.)
:33134 TRAP.AC[1], : ABORT FPA
:33135 J/EMODD.2 : MERGE INTO NORMAL EMODD FLOW
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:33136 : Here is a copy of certain states from C.FORK, which are used by
:33137 : EMODD to obtain the third specifier when the FPA is attached. This is
:33138 : necessary to fix a bug when the third specifier is a short literal
:33139 : because the FPA expects the base machine to explicitly pass the operand.
:33140
:33141 1300: -----;
:33142 EMODD.C.FORK:
:33143
:33144 1302: -----;
:33145 RC[T2] Q, :QUAD/DOUBLE SHORT LITERAL
:33146 Q_D,D_Q :GET LITERAL INTO D, SAVE D
:33147
:33148 -----;
:33149 ID D.SYNC, :SEND LITERAL TO FPA
:33150 D_0,RETURN10 :RETURN OLD D IN Q, REST IS ZERO
:33151
:33152 1306: -----;
:33153 RC[T2]_LA,Q_D,J/36E :QUAD REGISTER, TO READ
:33154
:33155 1308: -----;
:33156 VA_LA,Q_D,DATA.TYPE?,J/C.M : (R)
:33157
:33158 1309: -----;
:33159 R(PRN)_LA+K[SP1.CON].RLOG, : (R)+ UPDATE THE STACK POINTER
:33160 J/C.DR :THEN LOAD UN-INCREMENTED ADDR
:33161
:33162 130A: -----;
:33163 R(PRN)_LA-K[SP1.CON].RLOG, :-(R) AUTO DECREMENT
:33164 VA_ALU,Q_D,DATA.TYPE?,J/C.M : USE DECREMENTED ADDR
:33165
:33166 130B: -----;
:33167 VA LA, :@ (R)+ AUTO INCREMENT DEFERED
:33168 Q_D,J/394 :SAVE DATA WHILE GETTING INDIRECT
:33169
:33170 130C: -----;
:33171 RC[T7]_LA.CTX, :INDEX MODE, CONTEXT SHIFT INDEX
:33172 CALL,J7ASPC : AND GO EVALUATE BASE OPERAND ADDRESS
:33173
:33174 136C: -----;
:33175 D Q, :RETURN HERE WITH BASE OPERAND ADDRESS
:33176 VA D+LC, :RESTORE DATA TO BE STORED
:33177 DATA.TYPE?,J/C.M :COMPUTE INDEXED ADDRESS
:33178 :GET OR STORE NORMAL OR QUAD
:33179
:33180 130D: -----;
:33181 VA Q+LB.PC, :D(R) DISPLACEMENT MODE.
:33182 Q_D, :SAVE OLD D
:33183 CLR.IB.SPEC, :DISCARD THE SPECIFIER
:33184 DATA.TYPE?,J/C.M :GO GET THE OPERAND
:33185
:33186 130F: -----;
:33187 Q_D,VA Q+LB.PC, :@D(R) DISPLACEMENT DEFERED
: CLR.IB.SPEC,J/3BE :DROP THE SPECIFIER
    
```

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:33188 .TOC " FPA Interface : CFORK entry points for R=PC & special CFORK states"
:33189
:33190 :HERE ARE VARIANTS OF THE C-FORK ENTRY POINTS FOR R=PC
U 1316, 0000,003C,0180,F800,0000,0001 1316: -----:
:33191 : J/RSVMOD :PC QUAD REGISTER MODE
:33192
:33193
:33194 1317: -----:
U 1317, 0000,003C,0180,F800,0000,0001 : J/RSVMOD :ILLEGAL QUAD REGISTER MODE, R=PC
:33195
:33196
:33197 1318: -----:
U 1318, 0000,003C,0180,F800,0000,0001 : J/RSVMOD : (PC)
:33198
:33199
:33200 131A: -----:
U 131A, 0000,003C,0180,F800,0000,0001 : J/RSVMOD :-(PC)
:33201
:33202
:33203 131B: -----:
U 131B, D001,283C,01E0,F800,0200,02D2 : VA Q,Q D,CLR.IB.SPEC, :a(PC)+ ABSOLUTE MODE
:33204 : DATA.TYPE?,J/C.M
:33205
:33206
:33207 131C: -----:
U 131C, 0000,003C,0180,F800,0000,0001 : J/RSVMOD :INDEX MODE, R=PC
:33208
:33209
:33210 131D: -----:
U 131D, 0000,003C,0180,F800,0000,0001 : J/RSVMOD :NESTED INDEX MODE, R=PC
:33211
:33212
:33213 131F: -----:
U 131F, 0C01,203C,0180,F990,0000,1541 : RC[T2]_Q,D_Q : SAVE THE LOW ADDRESSED HALF
:33214
:33215
:33216 : ID_D.SYNC : SEND THE LOW HALF TO FPA
U 1541, 0000,007C,1580,BC00,0000,1542 :
:33217
:33218
:33219 : Q_IB.DATA,CLR.IB.COND, :GET SECOND PART INTO Q
U 1542, F000,0B3C,01F0,F806,0000,04D0 : PC_PC+4,IB.TEST?,J/C.IQ :PUSH PC PAST SECOND PART
:33220
:33221
:33222 :SPECIAL CFORK STATES
:33223 1387: -----:HERE WE SHOULD NEVER GET
U 1387, 0000,003D,0180,F800,0000,0EE0 : CALL,J/EH.USEQ :'UNUSED' LOCATION FOUND IN IB ROM
:33224
:33225
:33226
:33227 137C: -----:IB HAD NO DATA BECAUSE OF
U 137C, 0000,003D,0180,F800,0000,0E64 : CALL,J/IB.TBM :TB MISS. REFILL IT
:33228
:33229
:33230 137D: -----:IB HAD NO DATA BECAUSE OF
U 137D, 0000,003D,0180,F800,0000,0B80 : CALL,J/IB.ERR :ANY ERROR. FIND OUT WHAT HAPPENED
:33231
:33232 137E:
:33233 EMODD.SPEC:
:33234 : :IB IS WAITING FOR DATA
:33235 : LAB R(SP1),Q_IB.DATA,PC_PC+N, :STALL
U 137E, F000,003F,01F0,F847,0000,1300 : CLR.IB.COND,ACT/ALLOW.IB.READ,
:33236 : SUB/SPEC,J/EMODD.C.FORK
:33237
:33238
:33239 137F: -----:HERE IF INTERRUPT REQUEST UP
U 137F, C000,003C,0180,F800,0000,04F8 : J/INT.B :GO BACKUP REGISTERS, SERVE INTERRUPT
:33240
:33241 .NOLIST

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33241; This page intentionally left blank.

:33242 .TOC 'GANDH.MIC'
 :33243 .TOC 'Revision 0.8'
 :33244 : Kevin J. Cassidy,P. R. Guilbault
 :33245

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:33246 .NOBIN
:33247 .REGION/<WCSR3L>,<WCSR3H>/<WCSR1L>,<WCSR1H>,<WCSR2L>,<WCSR2H>
:33248
:33249 .TOC " Revision History"
:33250
:33251 : 08 Changes to POLYG/H,CVTRHL
:33252 : 07 ACBH-add branch to detect cases where sign of index and sign of limit
:33253 : are different.
:33254 : CVTHF-remove SET.CC(INST) macro from SPECG which was setting vbit and
:33255 : causing integer overflow traps.
:33256 : CVTHD-replace PACK.D routine with new code in wcs that does not use
:33257 : SET.CC(INST) macro that caused integer overflow traps.
:33258 : 06 ACBH-correct routine for reading and writing index when in register.
:33259 : initialize state during register read so ADD functions correctly.
:33260 : interchange ADDEND=0 and INDEX=0 return from unpack routine.
:33261 : and add cc macro to those paths.
:33262 : POLYH-change fault code in PACKH to do POLY.FAULT when FPD is set.
:33263 : 05 Change macro names that deal with conditions codes.
:33264 : 04 ACBH-change ADD.SUBR to loop on bit 6 of state instead of bit 5,
:33265 : also change CMPH so it leaves state bit 5 alone.Remove useless branch
:33266 : on SS in CMPH and clear sign bits of exponents so exp comparison
:33267 : works correctly.
:33268 : EMOBH- v bit cleared by ADDH.310,change cc macro
:33269 : ACBG-c bit lost in pack.g,save c-bit and restore after pack.
:33270 : 03 CVTHF change constraint so fault branch works.
:33271 : EMOBH/H CC problem fixed by clearing V and C bits at start.
:33272 : CVTGH problem:improper setup for call of pack routine,
:33273 : in ADDH.380 load LC_RC[T6] before call.
:33274 : CVTHD Packd subroutine includes SET.CC(INST) macro which,in this case,
:33275 : incorrectly sets C-bit,use SET.CC(INST) with proper conditions to
:33276 : zero c and v bits after return from pack.
:33277 : ACBG add condition code macros to ADDEND=0,INDEX=0 return paths from
:33278 : unpack routine to set CCs in those cases.
:33279 : DIVH C-hit set,modify PSL at end of instruction to clear C-bit.
:33280 : CVTRHL V-bit set,change SET.CC(INST) at start with NZ_ALU.V&C_0.
:33281 : CVTHW/HL/HB install test for intoverflow on return to CVTHB.
:33282 : 02 CVTGF.2-ADD SET.CC TO UNDERFLOW PATH
:33283 : CVTHD ADJUST UNDERFLOW,FU=0 PATH
:33284 : 01 Great error detection and fault code for CVTHD and CVTHG
:33285 : Convert CVTGF code from trap to faults.
:33286 : Start of history
:33287

```

:33288 .BIN

```

:33289 .TOC " G & H floating point : G-FORK Specifier Evaluation Subroutine"
:33290
:33291 :FPLA trap When there is no G & H
:33292 :1180: -----
:33293 : RC[T0]_K[.10],J/EXCPT : No G&H take fault
:33294 :
:33295 :FPLA trap when G & H is present
:33296 :11A3: -----
:33297 : ALU_K[.8000],RC[T4]_ALU, : FOR MOV0, SHORT LITERAL DETECT
:33298 : CLR_IB.OPC, : CLEAR ESCAPE-CODE,
:33299 : PC_PC+1, : INCREMENT PC PAST OP-CODE
:33300 : J/XFD : AND STROBE INTERRUPTS
:33301
:33302 =0*01*
:33303 XFD: :0*01*----- : CALL SITE FOR SPECG
:33304 : STATE_K[ZERO], : IN PARTICULAR FOR MOVH
:33305 : BEN/IB.0, : WAIT FOR OPCODE TO SETTLE
:33306 : CALL,J/XFD.1 : BRANCH ON IBO
:33307
:33308 =1*01* :1*01*----- : RETURN FROM SPECG WITH :
:33309 : : G = FORMAT 1. OPERAND
:33310 : : D = OP1 LONG FRAC
:33311 : : RC2 = OP1 LONG EXP
:33312 : : HERE FOR: ADDG*,SUBG*,MULG*,DIVG*,
:33313 : : ACBG,MOVG,CMPG,MNEGG,TSTG,CVTGB,
:33314 : : CVTGW,CVTGL,CVTRGL
:33315 : TRAP.ACCE[1],Q_RC[T2],J/XFD.G : RESET ACCEL, LATCH OP1 LONG EXP IN Q
:33316
:33317 =1*11* :1*11*----- : RETURN FROM SPECG WITH :
:33318 : : H FORMAT 1. OPERAND
:33319 : : Q = LONG EXP = RC[T2]
:33320 : : ID[T2]= OP1 LONG FRAC1
:33321 : : RC3 = OP1 LONG FRAC2
:33322 : : ID[T3]= OP1 LONG FRAC3
:33323 : : HERE FOR THE CORRESPONDING H-SOURCES
:33324 : TRAP.ACCE[1],RC[T0]_Q, : RESET ACCEL, STORE LONG EXP IN RC0
:33325 : Q_ID[T2] : Q GETS LONG FRAC1
:33326
:33327 :-----
:33328 : D_Q,Q_ID[T3], : MOVE DATA AROUND
:33329 : LC_RC[T3] : LATCH LONG FRAC2
:33330
:33331 :-----
:33332 : ID[T0]_D, : STORE LONG FRAC1 IN T0
:33333 : RC[T1]_LC, : RC1 GETS LONG FRAC2
:33334 : D_Q : D GETS LONG FRAC3
    
```

U 182A, 0000,053D,1980,F800,1404,7902

U 183A, 0010,00B8,00C0,F910,0000,180A

U 183E, 0001,20BC,C8F0,2D80,0000,180B

U 180B, 0C00,003C,CDF0,2D18,0000,1812

U 1812, 0C10,0038,C180,3D88,0000,1866

```
:33335 =0*11* ;0*11*-----:
:33336 IDET1] D, ; FINALLY STOR LONG FRAC3
:33337 D_RC[T0],CALL,J/SPECG ; D GETS LONG EXP
:33338
:33339 ;1*11*-----:
:33340 ; RETURN WITH:
:33341 ; RCO = OP1 LONG EXP
:33342 ; T0 = OP1 LONG FRAC1
:33343 ; RC1 = OP1 LONG FRAC2
:33344 ; T1 = OP1 LONG FRAC3
:33345 ; RC2 = OP2 LONG EXP
:33346 ; T2 = OP2 LONG FRAC1
:33347 ; RC3 = OP2 LONG FRAC2
:33348 ; T3 = OP2 LONG FRAC3
:33349 ; Q = OP2 LONG EXP
U 1866, 0810,0039,C580,3D00,0000,147E :33350 TRAP.AC[C1],G.FORK ; RESET THE ACCELLARATOR
:33351
:33352 =0**1*
:33353 XFD.G: ;0**1*-----:
:33354 TRAP.AC[C1], ; RESET THE ACCELLARATOR
:33355 RC[T0]_LC, ; STORE OP1 LONG EXP IN RCO
:33356 CALL, J/SPECG ; EVALUATE THE SECOND OPERAND
:33357 ; OR EXECUTION POINT
:33358
:33359 ;1**1*-----:
:33360 ; RETURN WITH:
:33361 ; Q = OP1 LONG FRAC
:33362 ; RCO = OP1 LONG EXP
:33363 ; D = OP2 LONG FRAC
:33364 ; RC1 = OP2 LONG EXP
U 1876, 0000,00BF,0080,F800,0000,1400 :33365 TRAP.AC[C1],E.FORK ; RESET THE ACCELLARATOR
```



```
:33366 =000  
:33367 =010  
:33368 XFD.1: ;010-----; BRANCH ON IB BYTE 0  
:33369 TRAP.ACC[1], ; RESET THE ACCELLARATOR  
:33370 RC[T5] K[.3FF], ; NOTHING BETTER TO DO  
U 1902, 0018,04B8,8080,F9A8,0000,1800 :33371 BEN/IRC.ROM,J/XFD.2 ; BRANCH ON OUTPUT OF IB-ROM  
:33372 =100  
:33373 XFD.10: ;100-----;   
:33374 TRAP.ACC[1], ; RESET THE ACCELLARATOR  
U 1904, 0000,00BD,0080,F800,0000,0E64 :33375 CALL,J/IB.TBM ; TB MISS  
:33376  
:33377 ;101-----;   
:33378 TRAP.ACC[1], ; RESET THE ACCELLARATOR  
U 1905, 0000,00BD,0080,F800,0000,0B80 :33379 CALL,J/IB.ERR  
:33380  
:33381 ;110-----;   
:33382 TRAP.ACC[1], ; RESET THE ACCELLARATOR  
U 1906, 0000,0BBC,0780,F800,0000,1904 :33383 MCT/ALLOW.IB.READ, ; KEEP READING  
:33384 IB.TEST?,J/XFD.10 ; TEST IB  
:33385  
:33386 ;111-----;   
:33387 TRAP.ACC[1], ; RESET THE ACCELLARATOR  
:33388 INTRPT.STROBE ; STROBE INTERRUPTS  
:33389 RC[T5] K[.3FF], ; NOTHING BETTER TO DO  
U 1907, 0018,04B8,8080,F9A8,4000,1800 :33390 BEN/IRC.ROM,J/XFD.2 ; BRANCH ON OUTPUT OF IB-ROM
```

```

:33391 =00*000
:33392 XFD.2: :00*000-----: FLOW FOR:
:33393 TRAP.ACC[1], : RESET THE ACCELLARATOR
U 1800, 0018,00B8,6480,F980,0000,08FC :33394 RC[T0]_K[.10],J/EXCPT : UNIMPLEMENTED OP-CODES
:33395
:33396 :00*001-----:
:33397 TRAP.ACC[1], : RESET THE ACCELLARATOR
U 1801, F000,00BF,00F0,F847,0000,1400 :33398 SPECG : ADDG*,SUBG*,MULG*,DIVG*,
:33399 : ACBG,MOVG,CMPG,MNEGG,TSTG,
:33400 : CVTGB,CVTGW,CVTGL,CVTRGL,
:33401
:33402 :00*010-----:
U 1802, F000,003F,01F0,F847,0000,0300 :33403 SPEC : CVTBG,CVTWG,C'TLG,CVT*H
:33404
:33405 :00*011-----:
U 1803, 0000,003D,0180,F800,0000,147E :33406 CALL,J/SPECG : EMOD AND POLY, EVALUATE 1st SPECIFIER
:33407
:33408 :00*100-----:
U 1804, 0000,00BD,0080,F800,0000,147E :33409 TRAP.ACC[1], : RESET THE ACCELLARATOR
:33410 CALL,J/SPECG : MOV0 ONLY
:33411
:33412 :00*101-----:
U 1805, 0018,00B8,6480,F980,0000,08FC :33413 TRAP.ACC[1], : RESET THE ACCELLARATOR
:33414 RC[T0]_K[.10],J/EXCPT : NO INSTRUCTION SHOULD GET HERE
:33415
:33416 :00*110-----:
:33417 TRAP.ACC[1], : RESET THE ACCELLARATOR
:33418 ALU_0(A),Q_ALU, : CVTFG,CVTDH,CVTFH
:33419 CLK_UBCC, : Q GETS COUNT FOR ADVANC EXEC.COUNT
U 1806, 7003,00BD,00C0,F800,0010,1810 :33420 IBC/BDEST, : ADVANCE IT ONCE
:33421 CALL,J/INCR.EXEC.PTR : ADVANCE IT 3 MORE TIMES
:33422
:33423 :00*111-----:
:33424 TRAP.ACC[1], : RESET THE ACCELLARATOR
:33425 ALU_0(A),Q_ALU, : CVTGF,CVTHD,CVTHF
:33426 CLK_UBCC, : Q GETS COUNT FOR ADVANC EXEC.COUNT
U 1807, 7003,00BD,00C0,F800,0010,1810 :33427 IBC/BDEST, : ADVANCE IT ONCE
:33428 CALL,J/INCR.EXEC.PTR : ADVANCE IT 3 MORE TIMES
  
```

```

:33429 =01*011 ;01*011-----: RETURN FROM SPECG EMODG/POLYG WITH :
:33430 : D = OP1 LONG FRAC
:33431 : RC2 = OP1 LONG EXP
:33432 TRAP.ACC[1], : RESET THE ACCELLARATOR
:33433 ID[T9] D, : SAVE ARG LONG FRAC IN POLYG
:33434 LC RC[T2], : LATCH OP1 LONG EXP
U 1813, 0000,1B8C,E480,3D10,0000,18AD :33435 IRD?,J/EMOD.POLY : IS THIS EMOD OR POLY ?
:33436
:33437 =01*100 ;01*100-----: RETURN FROM SPECG WITH :
:33438 : H FORMAT 1. OPERAND
:33439 : Q = LONG EXP = RC[T2]
:33440 : ID[T2]= OP1 LONG FRAC1
:33441 : RC3 = OP1 LONG FRAC2
:33442 : ID[T3]= OP1 LONG FRAC3
:33443 : HERE FOR THE CORRESPONDING H-SOURCES
U 1814, 0001,E08C,C8F0,2D80,0070,155B :33444 TRAP.ACC[1],RC[T0] Q, : RESET ACCEL, STORE LONG EXP IN RCO
:33445 Q_ID[T2],SET.CC(INST),J/NEWMOVO : Q GETS LONG FRAC1
:33446
:33447 =01*110 ;01*110-----: THIS GETS RET16 FROM READ REG ON MOVO
:33448 TRAP.ACC[1],RC[T0] Q, : RESET ACCEL, STORE LONG EXP IN RCO
U 1816, 0001,E08C,C8F0,2D80,0070,155B :33449 Q_ID[T2],SET.CC(INST),J/NEWMOVO : Q GETS LONG FRAC1
:33450
:33451 =01*111 ;01*111-----: RETURN FROM SPECG EMODH/POLYH WITH :
:33452 : RETURN WITH:
:33453 : Q = LONG EXP = RC2
:33454 : T2 = OP1 LONG FRAC1
:33455 : RC3 = OP1 LONG FRAC2
:33456 : T3 = OP1 LONG FRAC3
:33457 TRAP.ACC[1], : RESET THE ACCELLARATOR
:33458 RC[T0] Q, : SAVE OP1 LONG EXP IN RCO
:33459 Q_ID[T2], : GET OP1 LONG FRAC1
U 1817, 0001,208C,C8F0,2D80,0000,1680 :33460 J7EMODH.POLYH : SPECIAL FLOW
:33461
:33462 =10*110 ;10*110-----: RETURN WITH EXE.POINTER ADVANCED BY 3
:33463 IBC/BDEST, : ONCE MORE
U 1826, 7000,003D,0180,F800,0000,037E :33464 CALL,J/SPEC : CVTFG,CVTDH,CVTFH
:33465
:33466 :10*111-----:
:33467 IBC/BDEST, : ONCE MORE
:33468 STATE K[ZERO], : CLEAR STATE REGISTER
U 1827, 7000,003D,1980,F800,1404,747E :33469 CALL,J/SPECG : CVTGF,CVTHD,CVTHF
:33470
:33471 =11*110 ;11*110-----:
:33472 TRAP.ACC[1], : RESET THE ACCELLARATOR
U 1836, 0000,00BF,0080,F800,0000,1400 :33473 G.FORK : CVTFG,CVTDH,CVTFH
:33474
:33475 :11*111-----:
:33476 TRAP.ACC[1] : RESET THE ACCELLARATOR
:33477 ALU 0+K[.30]+1,SC_ALU, : SC GETS .31
U 1837, 001B,0093,7880,F800,0082,1400 :33478 G.FORK : CVTGF,CVTHD,CVTHF

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:33479 =01101
:33480 EMOD.POLY:
:33481 :01101-----: BRANCH ON IR<0>
:33482 RC[T0] LC, : RCO GETS MULTIPLIER LONG EXP
U 18AD, 0010,0038,0180,F980,0000,1883 : J/EMODG : EMOD
:33483
:33484
:33485 :01111-----: POLY
:33486 RC[T0] LC, : STORE OP1 LONG EXP IN RCO
U 18AF, 0010,0039,0180,F980,0000,037E : CALL, J/SPEC : EVALUATE THE DEGREE
:33487
:33488
:33489 =11111 :11111-----:
:33490 : RETURN WITH:
:33491 : Q = OP1 LONG FRAC
:33492 : RCO = OP1 LONG EXP
:33493 : D = DEGREE
U 18BF, 0000,003F,0180,F800,0000,1400 : G.FORK : EXECUTION TIME
:33494
:33495
:33496
:33497
:33498 :SUBROUTINE FOR ADVANCING EXECUTION POINT COUNTER
:33499 =0
:33500 INCR.EXEC.PTR:
:33501 :0-----: BRANCH ON ALU Z-BIT
:33502 ALU Q-K[.1],CLK.UBCC, : DECREMENT COUNT
:33503 IBC/BDEST, : ADVANCE POINTER
U 1810, 7019,2100,0580,F800,0010,1810 : Z?,J/INCR.EXEC.PTR : FINISHED ?
:33504
:33505
:33506 :1-----:
U 1811, 7000,003E,0180,F800,0000,0022 : IBC/BDEST,RETURN[22] : ADVANCE POINTER A LAST TIME
:33507
    
```

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:33508 ;Control passes to this point by 'CALL,J/SPEC' or from any 'WRITE.G.DEST' state.
:33509 ;LA, LB = Register selected by bits <3:0> of IB byte 1
:33510 ;D = Result to be stored, if WRITE.G.DEST; otherwise returned in Q
:33511 ;Q = Instruction stream data, if any
:33512 ;If the specifier evaluated is of 'READ' or 'MODIFY' type, control returns
:33513 ; at the call site ored with 10, for literal and memory operands, or the
:33514 ; call site ored with 12 for register operands. If 'WRITE' type, control
:33515 ; passes to IRD to perform the next instruction.
:33516
:33517 1400:
:33518 WRG:
:33519 G.FORK: ;-----: G FORMAT SHORT LITERAL
:33520 ALU Q.ANDNOT.K[E003], ; ISOLATE EXP AND FRACTION BITS
U 1400, 0899,2024,99E0,F800,0000,182D :33521 D_A[U.RIGHT2, Q_D ; STORE IN D, Q GETS OLD D
:33522
:33523 ;-----:
:33524 ALU D.OR.K[.8000], ; ADD IN NEW BIAS
U 182D, 0F59,0032,4580,F990,0000,0010 :33525 RC[T2]_ALU.RIGHT,D_0,RETURN10 ; RC2 GETS HIGH DATA, LONG FRAC<LS> IS 0
:33526
:33527 1401: ;-----:
:33528 J/RSVMD ;RESERVED MODE
:33529
:33530 1402: ;-----: H FORMAT SHORT LITERAL
:33531 ALU Q, ; GET I-STREAM DATA
:33532 RC[T4]_ALU, ; SAVE IT IN RC4 FOR MOVQ
:33533 SC_ALU(EXP), ; SC GETS EXPONENT
:33534 FE_K[.80], ; NEED TO GET RID OF OLD BIAS
:33535 STATE_K[.80], ; SET SHORT LITERAL FLAG
U 1402, 0F01,203C,41C8,F9A0,1587,7834 :33536 Q_ALU(FRAC), ; Q GETS FRACTION PART
:33537 D_0 ; GET READY TO CLEAR ID[T3]
:33538
:33539 ;-----:
:33540 ID[T3] D, ; CLEAR LONG FRAC3
:33541 Q Q.LEFT2, ; Q GETS REAL FRACTION PART
:33542 RC[T3] 0, ; CLEAR LONG FRAC2
U 1834, 0003,0C3C,CD88,3D98,0080,8841 :33543 SC_SC-FE,SC.NE.0? ; CLEAR BIAS
:33544
:33545 =0** ;0**-----: MOVQ
:33546 ID[T3]_D,Q_RC[T4], ;
U 1841, 0010,0038,CDC0,3D20,0000,1844 :33547 J/MOVQ ;
:33548
:33549 ;1**-----:
:33550 LC_RC[T3],Q_Q.OR.K[ESC] ; LATCH LONG FRAC2, GENERATE LONG EXP
:33551
:33552 ;-----:
:33553 Q_Q.OR.K[.4000] ; Q GETS BIAS
:33554 MOVQ: ;-----:
U 1844, 0000,003C,C980,3C00,0000,184D :33555 ID[T2]_D ;
:33556
:33557 K[.30], ; HAVE TO CLEAR ID[T2] AS WELL
U 184D, 0001,203E,7980,F990,0000,0014 :33558 RC[T2]_Q,RETURN[14] ; RETURN 14 FOR H FORMAT WITH :
:33559 ; Q = RC[T2] = LONG EXP
:33560 ; D = ID[T2] = LONG FRAC1
:33561 ; RC[T3] = LONG FRAC2
:33562 ; ID[T3] = LONG FRAC3
    
```

```

:33563 1403: :-----:
U 1403. 0000,003C,0180,F800,0000,0001 :33564 J/RSVMOD : RESERVED MODE
:33565
:33566 1404: :-----: G FORMAT REGISTER
U 1404. 0000,003C,01E0,F990,0000,1850 :33567 Q_D,RC[T2]_LA : SAVE D IN Q, RC2 GETS FIRST PART
:33568
:33569 :-----:
U 1850. 0800,003E,0180,F860,0000,0012 :33570 D_R(PRN+1),RETURN12 : D GETS LONG FRAC
:33571
:33572 1424: :-----: WRITE G FORMAT REGISTER
U 1424. 0001,00BC,0080,F8D8,0000,1855 :33573 WRDG.R: TRAP.ACC[1],R(PRN)_D : RESET ACCEL, WRITE LOW REGISTER FIRST
:33574
:33575 :-----:
U 1855. 0810,0038,0180,F908,0000,185A :33576 D_RC[T1] : GET DATA FOR HIGH ADDRESS
:33577
:33578 :-----:
U 185A. C001,003C,0180,F8E4,4000,0062 :33579 R(PRN+1) D, : WRITE HIGH REGISTER
:33580 CLR.IB.OPC,PC_PC+1,J/IRD : CLEAR IB
:33581
:33582 1405: :-----:
U 1405. 0000,003C,0180,F800,0000,0001 :33583 J/RSVMOD :
:33584
:33585 1406: :-----: *****HUGE REGISTER*****
U 1406. 0F00,003C,4180,F990,0000,1862 :33586 RC[T2]_LA, : HUGE REGISTER, TO READ
:33587 K[.80],D_0 : SET UP SLOW CONSTANT
:33588
:33589 HUGE.REG.READ.1:
:33590 :-----:
:33591 LAB_R(PRN+1), : LATCH LONG FRAC1
U 1862. 0839,0018,4180,F860,0000,1882 :33592 ALU_D+K[.80].RLOG, : PUT PRN+1 IN RLOG
:33593 D_ALU.LEFT : D GETS 100
:33594
:33595 :-----:
U 1882. 0041,0014,01C0,F800,1C00,1884 :33596 ALU_D+RLOG,Q_ALU.RIGHT : Q GETS PRN+2 (IN WRONG PLACE)
:33597
:33598 :-----:
U 1884. 080D,2038,0180,F800,0088,7891 :33599 D_LB, : D GETS LONG FRAC1
:33600 SC_2(EXP) : SC GETS PRN+2
:33601
:33602 :-----:
:33603 ID[T2]_D, : STORE LONG FRAC1 IN T2
U 1891. 0000,003C,C9C0,3C68,0080,D884 :33604 Q_R(SC), : Q GETS LONG FRAC2
:33605 SC_SC+1 : POINT TO NEXT REGISTER
:33606
:33607 :-----:
U 1884. 0800,003C,0180,F868,0000,18C2 :33608 D_R(SC) : D GETS LONG FRAC3
:33609
:33610 :-----:
:33611 RC[T3]_Q, : RC3 GETS LONG FRAC3
U 18C2. 0001,203C,CD80,3D98,0000,18D1 :33612 ID[T3]_D : T3 GETS LONG FRAC3
:33613
:33614 :-----:
U 18D1. 0010,003A,01C0,F910,0000,0016 :33615 Q_RC[T2], : Q GETS LONG EXP
:33616 RETURN[16] : RETURN16 FOR H FORMAT REGISTER
    
```

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:33617 1426: ;-----: *****HUGE REGISTER *****
:33618 ; ENTER WITH:
:33619 ; RC[0] = DST LONG EXP
:33620 ; T0 = DST LONG FRAC1
:33621 ; RC1 = DST LONG FRAC2
:33622 ; T1 = DST LONG FRAC3
:33623 TRAP.ACCT1], ; RESET THE FPA
:33624 D_RC[0] ; GET DST LONG FRAC
:33625
:33626 HUCE.REG.WRITE.1:
:33627 ;-----:
:33628 R(PRN) 0+D.RLOG,D_0, ; QUAD REGISTER. STUFF LOW ADDRESS PART
:33629 Q_ID[0] ; Q GETS LONG FRA1
:33630
:33631 ;-----:
:33632 ALU D+RLOG,Q_ALU.RIGHT, ; Q GETS REGISTER NUMBER
:33633 SC_RC[2],D_Q, ;
:33634 LC_RC[1] ; LATCH UP LONG FRAC2
:33635
:33636 ;-----:
:33637 SC SC+EXP(Q) (A), ; SC GETS PRN+2
:33638 ALU D(B),R(PRN+1)_ALU, ; STORE LONG FRAC1
:33639 Q_ID[1] ; Q GETS LONG FRAC3
:33640
:33641 WRITE.HUGE.PEGISTER:
:33642 ;-----:
:33643 ALU LC,R(SC)_ALU, ; STORE LONG FRAC2
:33644 SC_SC+1 ;
:33645
:33646 ;-----:
:33647 ALU Q,R(SC)_ALU, ; STORE LONG FRAC3 IN R(SC)
:33648 CLR_IB.OPC,PC_PC+1,J/IRD ;
:33649
:33650 WRITE.DEST.0:
:33651 ;-----:
:33652 SET.CC(INST), ;
:33653 RC[0]_D,ID[0]_D ; CLEAR OPERAND
:33654
:33655 ;-----:
:33656 RC[1]_D,ID[1]_D,N_AMX.Z_TST, ;
:33657 J/WRITE.G ;

```

U 1426, 0810,00B8,00E0,F900,0000,18D4

U 18D4, 0F1F,2018,C1F0,2CD8,0000,18DA

U 18DA, 0C41,0014,09C0,F908,1C84,78F5

U 18F5, 001D,2038,C5F0,2CE0,0088,98FD

U 18FD, 0010,0038,0180,F8E8,0080,D900

U 1900, C001,203C,0180,F8EC,4000,0062

U 190E, 0001,C03C,C180,3D80,0070,191C

U 191C, 0001,003C,C580,3D88,0030,18B0

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U 1407, 0000,003C,0180,F800,0000,0001 :33658 1407: :-----:
:33659 J/RSVMOD
:33660 1408: :-----:
:33661 G.DR: :-----:
:33662 TRAP.ACC[1], : RESET THE FPA
:33663 VA_LA, : (R) G OR H FORMAT, READ OR WRITE
:33664 Q_ALU, : SAVE ADDRESS IN Q FOR 2-OPERAND
U 1408, 0000,088C,00C0,F800,0200,1910 :33665 DATA.TYPE?,J/G.M : TEST FOR READ/WRITE, G/H-FORMAT
:33666
:33667 1409: :-----: G OR H FORMAT, (R)+
:33668 TRAP.ACC[1] : RESET THE FPA
:33669 R(PRN)_LA+K[SP1.CON].RLOG, : (R)+ UPDATE THE STACK POINTER
:33670 Q_ALU
:33671
:33672 :-----:
:33673 R(PRN)_Q+K[SP1.CON].RLOG, : UPDATE POINTER TWICE
U 192C, 0019,2018,1580,F8D8,0000,1408 :33674 J/G.DR : THEN LOAD UN-INCREMENTED ADDR
:33675
:33676 140A: :-----: G OR H FORMAT, -(R)
:33677 TRAP.ACC[1] : RESET THE FPA
:33678 R(PRN)_LA-K[SP1.CON].RLOG, : -(R) AUTO DECREMENT
:33679 Q_ALU
:33680
:33681 :-----:
:33682 R(PRN)_Q-K[SP1.CON].RLOG, : AUTO DECREMENT TWICE
:33683 VA_ALU, : USE DECREMENTED ADDR
:33684 Q_ALU, : SAVE ADDRESS IN Q FOR 2-OPERAND
U 193B, 0019,2804,15C0,F8D8,0200,1910 :33685 DATA.TYPE?,J/G.M : TEST FOR READ/WRITE, G/H-FORMAT
:33686
:33687 140B: :-----: G OR H FORMAT
:33688 TRAP.ACC[1], : RESET THE FPA
:33689 VA_LA, : @ (R)+ AUTO INCREMENT DEFERED
:33690 Q_D : SAVE DATA WHILE GETTING INDIRECT
:33691
:33692 :-----:
:33693 D[LONG] CACHE, : GET INDIRECT WORD
:33694 R(PRN)_A+K[.4].RLOG, : WHILE UPDATING REGISTER
U 1944, 0018,0018,1180,40D8,0000,195D :33695 J/G.DF : THEN JOIN COMMON CODE
  
```



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:33696 140C: -----: INDEX MODE, G OR H FORMAT
:33697 RC[T7] LA+LB.CTX, : INDEX MODE, CONTEXT SHIFT INDEX
:33698 INTERRUPT.REQ?, : TEST FOR INTERRUPTS
U 140C, 006C,CE15,0180,F9B8,0000,157E :33699 CALL,J/ASPCG : AND GO EVALUATE BASE OPERAND ADDRESS
:33700 : RETURN WITH:
:33701 : D = BASE ADDRESS
:33702 : LC = INDEX
:33703 : Q = OLD D-VALUE
:33704
:33705 146C: -----: RETURN HERE WITH BASE OPERAND ADDRESS
:33706 TRAP.AC[C1], : RESET THE FPA
:33707 D_Q, : RESTORE DATA TO BE STORED
:33708 VA_D+LC, : COMPUTE INDEXED ADDRESS
U 146C, 0C11,0894,00C0,F800,0200,1910 :33709 Q_ALU, : SAVE ADDRESS IN Q FOR 2-OPERAND
:33710 DATA.TYPE?,J/G.M : GET OR STORE G OR H-FORMAT
:33711
:33712 140D: -----: G OR H FORMAT
:33713 TRAP.AC[C1], : RESET THE FPA
:33714 VA_Q+LB.PC, : D(R) DISPLACEMENT MODE.
:33715 Q_ALU, : SAVE ADDRESS IN Q FOR 2-OPERAND
U 140D, D005,2894,00C0,F800,0200,1910 :33716 C[R.IB.SPEC, : DISCARD THE SPECIFIER
:33717 DATA.TYPE?,J/G.M : GO GET THE OPERAND
:33718
:33719 140F: -----: G OR H FORMAT
:33720 TRAP.AC[C1], : RESET THE FPA
:33721 Q_D,VA_Q+LB.PC, : @D(R) DISPLACEMENT DEFERED
U 140F, D005,2094,00E0,F800,0200,194E :33722 C[R.IB.SPEC : DROP THE SPECIFIER
:33723
:33724
U 194E, 0000,003C,0180,4000,0000,195D :33725 D[LONG]_CACHE :GET INDIRECT, GO USE IT AS ADDR
:33726
:33727 G.DF: -----:
:33728 VA_D, :USE POINTER AS ADDRESS
:33729 TRAP.AC[C1], : RESET THE FPA
:33730 D_Q, :GET DATA TO STORE BACK TO D
:33731 Q_ALU, : SAVE ADDRESS IN Q FOR 2-OPERAND
U 195D, 0C01,088C,00C0,F800,0200,1910 :33732 DATA.TYPE?,J/G.M : READ/WRITE, G OR H ?

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:33733 :HERE ARE VARIANTS OF THE G-FORK ENTRY POINTS FOR R=PC
:33734
U 1414, 0000,003C,0180,F800,0000,0001 :33735 1414: -----:
:33736 J/RSVMOD :PC REGISTER MODE
:33737
U 1415, 0000,003C,0180,F800,0000,0001 :33738 1415: -----:
:33739 J/RSVMOD :ILLEGAL REGISTER MODE, R=PC
:33740
U 1416, 0000,003C,0180,F800,0000,0001 :33741 1416: -----:
:33742 J/RSVMOD :PC QUAD REGISTER MODE
:33743
U 1417, 0000,003C,0180,F800,0000,0001 :33744 1417: -----:
:33745 J/RSVMOD :ILLEGAL QUAD REGISTER MODE, R=PC
:33746
U 1418, 0000,003C,0180,F800,0000,0001 :33747 1418: -----:
:33748 J/RSVMOD :(PC)
:33749
:33750 1419: -----:
:33751 TRAP.ACC[1], : RESET THE FPA
:33752 RC[2] Q, : (PC)+, G IMMEDIATE
:33753 Q IB.DATA, : GET SECOND PART INTO Q
:33754 CLR.IB.COND, : CLEAR IT
:33755 PC PC+4, : PUSH PC PAST SECOND PART
:33756 IB.TEST?,J/C.IQ : USE OLD C-FORK
:33757
U 141A, 0000,008C,0080,F800,0000,0001 :33758 141A: -----:
:33759 TRAP.ACC[1], : RESET THE FPA
:33760 J/RSVMOD :-(PC)
:33761
:33762 141B: -----:
:33763 TRAP.ACC[1], : RESET THE FPA
:33764 VA Q, : @ (PC)+ ABSOLUTE MODE
:33765 CLR.IB.SPEC, :
:33766 DATA.TYPE?,J/G.M : TEST FOR READ/WRITE, G/H-FORMAT
:33767
U 141C, 0000,003C,0180,F800,0000,0001 :33768 141C: -----:
:33769 J/RSVMOD :INDEX MODE, R=PC
:33770
U 141D, 0000,003C,0180,F800,0000,0001 :33771 141D: -----:
:33772 J/RSVMOD :NESTED INDEX MODE, R=PC
:33773
    
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:33774 141F: :-----:****HUGE FORMAT IMMEDIATE****
:33775 RC[2] Q, :QUAD IMMEDIATE
U 141F, 0001,203C,0180,F996,006C,1885 :33776 PC_PC+4 :PUSH PC PAST SECOND PART
:33777
:33778 =0**** :0****:
:33779 Q_IB.DATA, :GET SECOND PART INTO Q
U 1885, F000,0B3D,01F0,F800,0000,1870 :33780 CLR_IB.COND,IB.TEST?,CALL,J/G.IQ;
:33781
:33782 :1****:
:33783 ID[2] D, :STORE LONG FRAC1
U 1895, 0000,003C,C980,3C06,0C00,188C :33784 PC_PC+4 :PUSH PC PAST SECOND PART
:33785
:33786 =0**** :0****:
:33787 Q_IB.DATA, :GET SECOND PART INTO Q
U 188C, F000,0B3D,01F0,F800,0000,1870 :33788 CLR_IB.COND,IB.TEST?,CALL,J/G.IQ;
:33789
:33790 :1****:
:33791 RC[3] D, :STORE LONG FRAC2 IN RC3
U 189C, 0001,003C,0180,F99E,0000,188D :33792 PC_PC+4 :PUSH PC PAST SECOND PART
:33793
:33794 =0**** :0****:
:33795 Q_IB.DATA, :GET SECOND PART INTO Q
U 188D, F000,0B3D,01F0,F800,0000,04D0 :33796 CLR_IB.COND,IB.TEST?,CALL,J/C.IQ;
:33797
:33798 :1****:
:33799 ID[3] D, :STORE LONG FRAC3 IN T3
U 189D, 0010,003A,CDC0,3D10,0000,0014 :33800 Q_RC[2], :Q GETS LONG EXP
:33801 RETURN[14] :RETURN14 FOR H FORMAT IMMEDIATE
:33802 =00
:33803 G.IQ: :00:
U 1870, 0000,003D,0180,F800,0000,0E64 :33804 CALL,J/IB.TBM :TB MISS IN IB
:33805
:33806 :01:
U 1871, 0000,003D,0180,F800,0000,0B80 :33807 CALL,J/IB.ERR :IB ERROR
:33808
:33809 :10:
:33810 Q_IB.DATA, :KEEP ON TRYING
U 1872, F000,0B3C,01F0,F800,0000,1870 :33811 CLR_IB.COND,
:33812 IB.TEST?,J/G.IQ
:33813
:33814 :11:
U 1873, 0C00,003E,01E0,F800,0000,0010 :33815 D_Q,Q_D,RETURN10 :GOT THE DATA, LEAVE IT IN D

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:33816 ;SPECIAL G-FORK STATES
:33817
J 1487, 0000,003D,0180,F800,0000,0EEC :33818 1487: :-----: HERE WE SHOULD NEVER GET
:33819 CALL,J/EH.USEQ : 'UNUSED' LOCATIGN FOUND IN IB ROM
:33820
J 147C, 0000,003D,0180,F800,0000,0E64 :33821 147C: :-----: IB HAD NO DATA BECAUSE OF
:33822 CALL,J/IB.TBM : TB MISS. REFILL IT
:33823
J 147D, 0000,003D,0180,F800,0000,0B80 :33824 147D: :-----: IB HAD NO DATA BECAUSE OF
:33825 CALL,J/IB.ERR : ANY ERROR. FIND OUT WHAT HAPPENED
:33826
:33827 147E:
:33828 SPECG: :-----: IB IS WAITING FOR DATA
:33829 LAB R(SPI), : STALL
:33830 C IB.DATA,CLR.IB.COND,PC_PC+N,
:33831 MCT/ALLOW.IB.READ,
:33832 SUB/SPEC,J/G.FORK
:33833
U 147F, 0000,003C,0180,F800,0000,04F8 :33834 147F: :-----: HERE IF INTERRUPT REQUEST UP
:33835 J/INT.B : GO BACKUP REGISTERS, SERVE INTERRUPT
:33836
:33837
:33838 ;HERE TO WRITE BACK THE RESULT OF AN INSTRUCTION WITH A MODIFY DESTINATION.
:33839 ; ASSIGNED AN ADDRESS ON CFORK BECAUSE MANY 2-OPERAND INSTRUCTIONS ARE
:33840 ; EXECUTED BY THE SAME CODE AS THE 3-OPERAND COUNTERPART, AND CONCLUDE WITH
:33841 ; THE WRITE.G.DEST OPERATION, WHICH EVALUATES THE THIRD SPECIFIER IN THE
:33842 ; 3-OPERAND FORM, AND COMES HERE FOR THE 2-OPERAND FORM.
:33843 1441:
:33844 STORE.G: :-----: STORE MODIFIED G FORMAT
:33845 TRAP.ACCE1], : RESET THE FPA
:33846 VA RCET7], : RESTORE OPERAND ADDRESS
:33847 STATE0? : IS THIS MOVH ?
:33848
:33849 =0 :0-----:
:33850 J/MOVH
:33851
:33852 :1-----:
:33853 CACHE_D[LONG], : WRITE LONG EXP
:33854 J/C.WQ1 : USE OLD DOUBLE WRITE ROUTINE
:33855
:33856 ;HERE IS THE SAME FUNCTION FOR OCTO/HUGE OPERATIONS
:33857 1444:
:33858 STOR.H: :-----: STORE MODIFIED H FORMAT
:33859 TRAP.ACCE1], : RESET THE FPA
:33860 VA RCET7],Q_ALU, : RELOAD OPERAND ADDRESS, WHICH GOT
:33861 J/G.WH : INCREMENTED IN FETCHING OPERAND (??)

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:33862 :HERE FOR THE SECOND AND SUBSEQUENT STATES OFF C-FORK SUBROUTINE
:33863 =000
:33864 G.M: :000-----: GET HERE BY DATA.TYPE, WRITE G -FORMAT
:33865 TRAP.ACC[1], : RESET THE FPA
:33866 RC[T0]_Q, : DO NOT WRITE YET
:33867 Q_D, : SAVE DATA
:33868 D[LONG] CACHE.WCHK, : READ FIRST LONGWORD WITH WRITECHECK
U 1910, 0001,20BC,00E0,5180,0000,1966 :33869 J/WRITE.GRAND
:33870
:33871 G.WH: :001-----: WRITE HUGE FORMAT
:33872 TRAP.ACC[1], : RESET THE FPA
:33873 ALU Q+K[.8],VA_ALU, : VA GETS ADDRESS OF LONG FRAC2
U 1911, 0019,2094,0080,F800,0200,1982 :33874 J/WRITE.HUGE
:33875
:33876 =100 :100-----:
:33877 TRAP.ACC[1], : RESET THE FPA
:33878 D[LONG] CACHE.IBCHK, : READ LONG EXP WITH IB-CHECK
:33879 RC[T7]_Q, : SAVE ADDRESS IN RC7
:33880 Q_D, : SAVE PREVIOUS OPERAND
U 1914, 0001,20BC,00E0,5988,0000,1A41 :33881 J7G.RQ : LABEL IN C-FORK (=C.M+4)
:33882
:33883 :101-----: READ HUGE FORMAT
:33884 TRAP.ACC[1], : RESET THE FPA
:33885 D[LONG] CACHE.IBCHK, : READ LONG EXP WITH IB-CHECK
:33886 RC[T7]_Q, : SAVE ADDRESS IN RC7
:33887 Q_D, : SAVE PREVIOUS OPERAND
U 1915, 0001,20BC,00E0,5988,0000,19E9 :33888 J7READ.HUGE
:33889
:33890 :110-----:
U 1916, 0000,003E,0180,F800,0000,0010 :33891 RETURN10 : Q HAS ADDRESS
:33892
:33893 :111-----: H-FORMAT ADDRESS
:33894 ALU Q,SET.CC(INST), : MOVAH OR PUSHAH
:33895 D_Q,LAB_R[SP], : D GETS ADDRESS,LATCH SP
U 1917, 0C01,FB3C,0180,FA70,0070,191D :33896 IRO? : WHICH INSTRUCTION IS IT ?
:33897
:33898 =1101 :1101-----:
U 191D, F000,003F,01F0,F847,0000,0200 :33899 B.FORK : MOVAH (7EFD)
:33900
:33901 :111-----: PUSHAH (7FFD)
:33902 R[SP]&VA_LA-K[.4].RLOG, : LOAD DECREMENTED ADDR INTO SP
U 191F, 0018,0004,1180,FAF0,0200,0341 :33903 J/STORE : STORE ADDRESS ON STACK
:33904
:33905 WRITE.GRAND:
:33906
:33907 TRAP.ACC[1], : RESET THE FPA
:33908 VA VA+4, : POINT TO NEXT LONGWORD
U 1966, 0810,00B8,0080,F90B,0000,196A :33909 D_RC[T1] : GET LONG FRAC
:33910
:33911
:33912 :-----:
U 196A, 0000,003C,0180,3000,0000,197E :33912 CACHE_D[LONG] : WRITE LONG FRAC
:33913
:33914
:33915 :-----:
U 197E, 0C10,0038,0180,F900,0200,03FD :33915 VA_RC[T0], : LOAD ADDRESS OF LONG EXP
:33916 D_Q,J/STOR.L : WRITE LONG EXP
    
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:33917 WRITE.HUGE:
:33918 -----:
:33919 RC[T2] Q, : RC2 GETS ADDRESS OF LONG EXP
U 1982, 0001,E03C,0180,5190,0000,1991 :33920 D[INST.DEP]_CACHE.WCHK : TEST LAST TWO LONGWORDS
:33921
:33922 -----:
:33923 VA RC[T2], : VA GETS LOW ADDRESS
U 1991, 0010,0038,C1F0,2D10,0200,19A3 :33924 Q_ID[T0] : Q GETS LONG FRAC1
:33925
:33926 -----:
:33927 D_RC[T0] : D GETS LONG EXP
:33928
:33929 WRITE.HUGE.1:
:33930 -----: ENTER HERE FROM EMODH
U 19A9, 0000,003C,0180,3000,0000,19B1 :33931 CACHE_D[LONG] : WRITE LONG EXP
:33932
:33933 -----:
:33934 D Q, : D GETS LONG FRAC1
U 19B1, 0C10,0038,01C0,F90B,0000,19B6 :33935 VA VA+4, : POINT TO ITS ADDRESS
:33936 Q_RC[T1] : Q GETS LONG FRAC2
:33937
:33938 -----:
U 19B6, 0000,003C,0180,3000,0000,19C1 :33939 CACHE_D[LONG] : WRITE LONG FRAC1
:33940
:33941 -----:
:33942 VA VA+4, : KEEP ON INCREMENTING
U 19C1, 0C00,003C,C5F0,2C03,0000,19D4 :33943 D Q, : D GETS LONG FRAC2
:33944 Q_ID[T1] : Q GETS LONG FRAC3
:33945
:33946 -----:
U 19D4, 0001,203C,0180,3188,0000,03F8 :33947 CACHE_D[LONG], : WRITE LONG FRAC2
:33948 RC[T1] Q, : TO USE OLD CODE
:33949 J/C.WQT :
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:33950 READ.HUGE:
:33951 -----:
:33952 RC[T2] D, : STORE IT IN RC2
U 19E9, 0001,003C,0180,F993,0000,19FB :33953 VA_VA+4 : POINT TO LONG FRAC1
:33954 -----:
:33955 :
:33956 D[LONG]_CACHE : READ LONG FRAC1
:33957 -----:
:33958 :
:33959 Q D, ID[T2] D, : STORE IT IN T2
U 1A09, 0000,003C,C9E0,3C03,0000,1A1D :33960 VA_VA+4 : INCREMENT ADDRESS TO LONG FRAC2
:33961 -----:
:33962 :
:33963 D[LONG]_CACHE : READ LONG FRAC2
:33964 -----:
:33965 :
:33966 RC[T3] D, : STORE LONG FRAC2 IN RC3
U 1A25, 0001,003C,0180,F99B,0000,1A29 :33967 VA_VA+4 : POINT TO LONG FRAC3
:33968 -----:
:33969 :
:33970 D[LONG]_CACHE : D GETS LONG FRAC3
:33971 -----:
:33972 :
:33973 ID[T3] D, : STORE LONG FRAC3 IN ID[T3]
:33974 Q_RC[T2], : Q GETS LONG EXP
:33975 D_Q, : D GETS LONG FRAC1
U 1A3A, 0C10,003A,CDC0,3D10,0000,0014 :33976 RETURN[14] : RETURN14 FOR H FORMAT
:33977 -----:
:33978 G.RQ: : HERE TO READ 2nd PART OF A G OPERAND
U 1A41, 0001,003C,0180,F993,0000,1A49 :33979 RC[T2] D, : SAVE FIRST PART IN RC2
:33980 VA_VA+4 :
:33981 -----:
:33982 :
:33983 D[LONG]_CACHE.IBCHK, : READ SECOND LONGWORD
U 1A49, 0000,003E,0180,5800,0000,0010 :33984 RETURN10

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:33985 .TOC " G & H floating point : Address Specifier Evaluation"  
:33986 :Control passes to this point by CALL,J/ASPCG  
:33987 : and returns to the call site 'or' 60, if the specifier is valid,  
:33988 : or the call site 'or' 61 if the specifier is register mode, which will  
:33989 : be invalid unless the specifier is a field source. At the return, Q  
:33990 : contains the longword that was in D at the entry, D and VA contain  
:33991 : the address implied by the specifier.  
:33992 157E:  
:33993 ASPCG: -----:HANG HERE IF IB MUST STALL  
:33994 Q IB.DATA, :GET SPECIFIER DATA FROM ISTREAM  
:33995 LAB R(SP1), :LOAD LATCHES FROM BASE SPECIFIER  
:33996 CLR IB.COND, :DISCARD BASE OPERAND SPECIFIER  
:33997 PC PC+N, :STEP PC OVER IT  
:33998 MCT/ALLOW.IB.READ, :LET IB GET NEEDED DATA  
:33999 SUB/SPEC,J/ASPCG.B :EVALUATE THE SPECIFIER  
:34000  
:34001 1500:  
:34002 ASPCG.B:-----:  
:34003 J/RVSMOD :S*# SHORT LITERAL NOT LEGAL AS ASRC  
:34004  
:34005 1501: :-----:  
:34006 J/RVSMOD :RESERVED MODE  
:34007  
:34008 1502: :-----:  
:34009 J/RVSMOD :QUAD/DOUBLE SHORT LITERAL  
:34010  
:34011 1503: :-----:  
:34012 J/RVSMOD :RESERVED MODE  
:34013  
:34014 1504: :-----:  
:34015 Q D, :REGISTER  
:34016 RT(PRN)_LA+K[ZERO].RLOG, :RECORD REGISTER NUMBER IN RLOG  
:34017 D ALU, :GET REGISTER CONTENTS TO D  
:34018 RETURN61 :RETURN IT IN CASE FIELD SOURCE  
:34019  
:34020 1524: :-----:  
:34021 Q D, :WRITE REGISTER  
:34022 RT(PRN)_LA+K[ZERO].RLOG, :RECORD REGISTER NUMBER IN RLOG  
:34023 D ALU, :GET REGISTER CONTENTS TO D  
:34024 RETURN61 :RETURN IT IN CASE FIELD SOURCE  
:34025  
:34026 1505: :-----:  
:34027 J/RVSMOD  
:34028  
:34029 1506: :-----:  
:34030 Q D, :QUAD REGISTER  
:34031 RT(PRN)_LA+K[ZERO].RLOG, :RECORD REGISTER NUMBER IN RLOG  
:34032 D ALU, :RETURN CONTENTS TO CALLER  
:34033 RETURN61  
:34034  
:34035 1526: :-----:  
:34036 Q D, :WRITE QUAD REGISTER  
:34037 RT(PRN)_LA+K[ZERO].RLOG, :RECORD REGISTER NUMBER IN RLOG  
:34038 D ALU, :RETURN CONTENTS TO CALLER  
:34039 RETURN61  
:
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U 1507, 0000,003C,0180,F800,0000,0001 :34040 1507: :-----:
:34041 J/RSVMOD ;ILLEGAL QUAD REG
:34042 1508:
:34043 ASPCG.DR:
:34044 :-----: (R)
U 1508, 0800,003E,01E0,F938,0200,0060 :34045 Q D,D&VA_LA,LC_R[CT7], ;RECOVER INDEX(PROPERLY SHIFTED),IF ANY
:34046 RETURN60 ;RETURN IT
:34047
:34048 1509: :-----:
:34049 R(PRN)_LA+K[SP1.CON].RLOG, ;UPDATE THE STACK POINTER
U 1509, 0018,0018,15C0,F8D8,0000,1A5D :34050 Q_ALU ;
:34051
:34052 :-----:
:34053 R(PRN) Q+K[SP1.CON].RLOG, ;UPDATE THE STACK POINTER
U 1A5D, 0019,2018,1580,F8D8,0000,1508 :34054 J/ASPCG.DR ;THEN LOAD UN-INCREMMENTED ADDR
:34055
:34056 150A: :-----:
U 150A, 0018,0004,15C0,F8D8,0000,1A95 :34057 R(PRN)_LA-K[SP1.CON].RLOG,Q_ALU ; -(R) AUTO DECREMENT
:34058
:34059 :-----:
:34060 Q D,R(PRN) Q-K[SP1.CON].RLOG, ;-(R) AUTO DECREMENT
U 1A95, 0819,2004,15E0,F8D8,0000,1AAD :34061 D_ALU ; USE DECREMENTED ADDR
:34062 J7ASPCG.DF ;GO LOAD LC BEFORE RETURNING
:34063
:34064 150B: :-----:
U 150B, 0000,003C,01E0,F800,0200,1A9E :34065 Q_D,VA_LA ;@ (R)+ AUTO INCREMENT DEFERED
:34066
:34067 :-----:
:34068 D[LONG]_CACHE, ;GET INDIRECT WORD
U 1A9E, 0018,0018,1180,40D8,0000,1AAD :34069 R(PRN) [A+K[.4].RLOG, ; WHILE UPDATING REGISTER
:34070 J/ASPCG.DF ;THEN JOIN COMMON CODE
:34071
:34072 150C: :-----:
U 150C, 006C,C015,0180,F988,0000,157E :34073 RC[CT7] LA+LB.CTX, ;INDEX MODE, CONTEXT SHIFT INDEX
:34074 CALL,J7ASPCG ;GO AROUND AGAIN
:34075
:34076 156C: :-----:
U 156C, 0811,0016,0180,F800,0200,0060 :34077 D&VA_D+LC,RETURN60 ;RETURN THE INDEXED VALUE
:34078
:34079 150D: :-----:
:34080 Q D,D&VA Q+LB.PC, ;D(R) DISPLACEMENT MODE.
U 150D, D805,2016,01E0,F938,0200,0060 :34081 C[R.IB.SPEC, ;DISCARD THE SPECIFIER
:34082 LC_R[CT7],RETURN60 ;LOAD UP INDEX, IF ANY
:34083
:34084 150F: :-----:
U 150F, D005,2014,01E0,F800,0200,1AA1 :34085 Q D,VA Q+LB.PC, ;@D(R) DISPLACEMENT DEFERED
:34086 C[R.IB.SPEC ;DROP THE SPECIFIER
:34087
:34088 :-----:
U 1AA1, 0000,003C,0180,4000,0000,1AAD :34089 D[LONG]_CACHE ;GET INDIRECT, GO USE IT AS ADDR
:34090
:34091 ASPCG.DF:
:34092 :-----:
U 1AAD, 0001,003E,0180,F938,0200,0060 :34093 VA_D, ;****COULD USE GLD CODE HERE****
:34094 LC_R[CT7],RETURN60 ;USE POINTER AS ADDRESS
;RECOVER INDEX, IF ANY
    
```

```

:34095 ;HERE ARE VARIANTS OF THE ASPC ENTRY POINTS FOR R=PC
:34096
J 1514, 0000,003C,0180,F800,0000,0001 :34097 1514: :-----:
:34098 J/RSVMOD ;PC REGISTER MODE
:34099
:34100 1515: :-----:
J 1515, 0000,003C,0180,F800,0000,0001 :34101 J/RSVMOD ;ILLEGAL REGISTER MODE, R=PC
:34102
:34103 1516: :-----:
J 1516, 0000,003C,0180,F800,0000,0001 :34104 J/RSVMOD ;PC QUAD REGISTER MODE
:34105
:34106 1517: :-----:
U 1517, 0000,003C,0180,F800,0000,0001 :34107 J/RSVMOD ;ILLEGAL QUAD REGISTER MODE, R=PC
:34108
:34109 1518: :-----:
U 1518, 0000,003C,0180,F800,0000,0001 :34110 J/RSVMOD ;(PC)
:34111
:34112 1519: :-----:
:34113 Q D, ;(PC)+ IMMEDIATE MODE
U 1519, D814,0038,01E0,F800,0000,1AB2 :34114 D PC, ;GET PC WHICH THE IB INCREMENTED
:34115 CLR.IB.SPEC
:34116
:34117 :-----:
:34118 D&VA D-K[SP1.CON], ;COMPUTE THE UNINCREMENTED ADDRESS
U 1AB2, 0819,0002,1580,F938,0200,0060 :34119 LC RC[7], ;RECOVER INDEX, IF ANY
:34120 RETURN60
:34121
:34122 151A: :-----:
U 151A, 0000,003C,0180,F800,0000,0001 :34123 J/RSVMOD ;-(PC)
:34124
:34125 151B: :-----:
:34126 Q D,D&VA Q, ;a(PC)+ ABSOLUTE MODE
:34127 LC RC[7], ;GET BACK INDEX
U 151B, DC01,203E,01E0,F938,0200,0060 :34128 CLR.IB.SPEC,
:34129 RETURN60
:34130
:34131 151C: :-----:
U 151C, 0000,003C,0180,F800,0000,0001 :34132 J/RSVMOD ;INDEX MODE, R=PC
:34133
:34134 151D: :-----:
U 151D, 0000,003C,0180,F800,0000,0001 :34135 J/RSVMOD ;NESTED INDEX MODE, R=PC

```

```

:34136 ;HERE WHEN IB ROMS BELIEVE WE SHOULDN'T GET HERE
:34137
U 1587, 0000,003D,0180,F800,0000,0EE0 :34138 1587: -----:
:34139 CALL,J/EH.USEQ ;'UNUSED' LOCATION IN IB ROM
:34140
:34141 ;HERE OFF ASPCG, WHEN INSTRUCTION BUFFER DOES NOT HAVE ENOUGH DATA
:34142
U 157C, 0000,003D,0180,F800,0000,0E64 :34143 157C: -----:
:34144 CALL,J/IB.TBM ;TB MISS. REFILL IT
:34145
U 157D, 0000,003D,0180,F800,0000,0B80 :34146 157D: -----:
:34147 CALL,J/IB.ERR ;ANY ERROR. FIND OUT WHAT HAPPENED
:34148
:34149 ;157E: -----:
:34150 ; ASPCG: ;STALL, WAITING FOR THE DATA
:34151
U 157F, 0000,003C,0180,F800,0000,04F8 :34152 157F: -----:
:34153 J/INT.B ;INTERRUPT REQUEST DETECTED
;BACKUP REGISTERS AND TAKE INTERRUPT

```

```
:34154 .TOC '' G & H floating point : E-FORK''
:34155
:34156 :BRANCH POINT FOR EMOD-EXTENDER AND OTHER ODD SPECIFIER EVALUATIONS.
:34157
:34158 1600:
:34159 E.FORK: -----:
U 1600, 0C00,003E,01E0,F800,0000,0010 :34160 D_Q,Q_D, RETURN10 ; SHORT LITERAL
:34161
:34162 1604: -----:
U 1604, 0800,003E,01E0,F800,0000,0010 :34163 Q_D,D LA, ; D GETS REGISTER VALUE
:34164 RETURN10
:34165 1608:
:34166 E.DR: -----:
:34167 VA LA, ; MODE IS (R)
:34168 Q_D, ; SAVE OLD D-VALUE IN Q
U 1608, 0000,003C,01E0,F800,0200,1AC9 :34169 J/E.M ; JOIN EMOD-MEMORY-REFERENCE
:34170
:34171 1609: -----:
U 1609, 0018,0018,0980,F8D8,0000,1608 :34172 R(PRN)_LA+K[.2].RLOG, ; (R)+
:34173 J/E.DR
:34174
:34175 160A: -----:
U 160A, 0018,0004,09E0,F8D8,0200,1AC9 :34176 R(PRN)_LA-K[.2].RLOG, ; (R)-
:34177 VA ALU, Q_D, ; LOAD VA WITH OPERAND ADDRESS
:34178 J/E.M
:34179
:34180 160B: -----:
U 160B, 0000,003C,01E0,F800,0200,1AB4 :34181 VA LA, ; @ (R)+
:34182 Q_D
:34183
:34184 -----:
:34185 D[LONG] CACHE, ; D GETS OPERAND ADDRESS
U 1AB4, 0018,0018,1180,40D8,0000,1AB7 :34186 R(PRN)_LA+K[.4].RLOG, ; AUTO INCREMENT REGISTER
:34187 J/E.DF
:34188
:34189 E.DF: -----:
U 1AB7, 0001,003C,0180,F800,0200,1AC9 :34190 VA_D, J/E.M ; VA GETS OPERAND ADDRESS
:34191
:34192 E.M: -----:
:34193 D[WORD] CACHE, ; READ OPERAND
U 1AC9, 0000,403E,0180,4000,0000,0010 :34194 RETURN10
:34195
:34196 160C: -----:
U 160C, 006C,C015,0180,F9B8,0000,157E :34197 RC[T7]_LA+LB.CTX, ; INDIRECT
:34198 CALL,J7ASPCG
:34199
:34200 166C: -----:
U 166C, 0C11,0014,0180,F800,0200,1AC9 :34201 D_Q,VA_D+LC, ; VA GETS OPERAND ADDRESS
:34202 J/E.M ; MAKE MEMORY REFERENCE
:34203
:34204 160D: -----:
U 160D, D005,2014,01E0,F800,0200,1AC9 :34205 VA Q+LB.PC, ; INDIRECT
:34206 Q_D,CLR.IB.SPEC,J/E.M ;
```

```

:34207 160F: :-----:
:34208 Q_D,VA_Q+LB.PC,
U 160F, D005,2014,01E0,F800,0200,1ACC :34209 CLR.IB.SPEC
:34210 :-----:
:34211 :-----:
U 1ACC, 0000,003C,0180,4000,0000,1AB7 :34212 D[LONG]_CACHE, J/E.DF
:34213 :-----:
:34214 1619: :-----:
:34215 D_Q, : IMMEDIATE
U 1619, 0C00,003C,7180,F804,0084,78C5 :34216 SC_K[.FFF8], : SHIFT COUNT OF -8.
:34217 PC_PC+1
:34218 :-----:
:34219 =0**** :0****:-----:
:34220 Q_IB.DATA, : GET SECOND PART OF WORD
:34221 CLR.IB.COND, : CLEAR SPECIFIER
U 18C5, F000,0B3D,01F0,F800,0000,04D0 :34222 IB.TEST?, : NEED ONE MORE BYTE
:34223 CALL,J/C.IQ
:34224 :-----:
:34225 :1****:-----:
:34226 D_DAL.SC, : GET NEW BYTE INTO D<31:24>
U 18D5, 0D00,003C,69E0,F800,0084,7ACE :34227 Q_D, : Q GETS LOW BYTE
:34228 SC_K[.FFF8] : -24
:34229 :-----:
:34230 :-----:
U 1ACE, 0D00,003E,E5F0,2C00,0000,0010 :34231 Q_ID[T9], : RESTORE MULTIPLIER FRAC LONG
:34232 D_DAL.SC, RETURN10 : GET THE DATA IN RIGHT ORDER
:34233 :-----:
:34234 161B: :-----:
:34235 VA_Q, Q_D, : IMMEDIATE DEFERRED
U 161B, D001,203C,01E0,F800,0200,1AC9 :34236 CLR.IB.SPEC,
:34237 J/E.M
:34238 :-----:
:34239 167C: :-----:
U 167C, 0000,003D,0180,F800,0000,0E64 :34240 CALL,J/IB.TBM
:34241 :-----:
:34242 167D: :-----:
U 167D, 0000,003D,0180,F800,0C00,0B80 :34243 CALL,J/IB.ERK
:34244 :-----:
:34245 167E: :-----:
:34246 SPECE: :-----:
:34247 LAB R(SP1), : LA AND LB GETS REGISTER VALUE
:34248 Q_IB.DATA, : Q GETS INSTRUCTION STREAM DATA
:34249 CLR.IB.COND,
U 167E, F000,003F,01F0,F847,0000,1600 :34250 PC_PC+N, : INCREMENT PC
:34251 MCT/ALLOW.IB.READ, : TURN ON IB-READ
:34252 SUB/SPEC,J/E.FORK
:34253 :-----:
:34254 167F: :-----:
U 167F, 0000,003C,0180,F800,0000,04F8 :34255 J/INT.B
  
```

:34256 .TOC " G & H floating point : GRAND FLOATING NOTATION"

:34257
:34258 : THE FOLLOWING NOTATION IS USED IN COMMENTS BELONGING TO THE
:34259 : MICROCODE FOR THE GRAND FLOATING INSTRUCTION SET.

:34260
:34261 : OP1 LONG EXP = LONGWORD OF 1. OPERAND CONTAINING EXPONENT
:34262 : AND HIGH FRACTION BITS.

:34263 : OP1 LONG FRAC = LONGWORD OF 1. OPERAND CONTAINING FRACTION BITS ONLY

:34264 : OP1 EXP = EXPONENT OF OPERAND 1

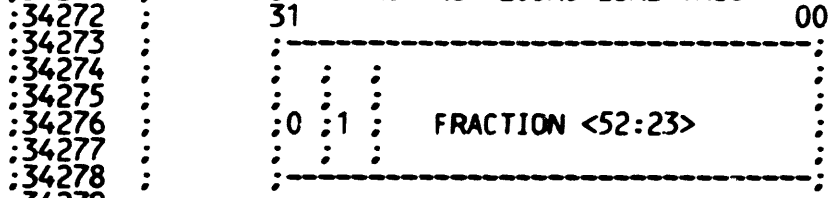
:34265 : OP1 FRAC <LS> = LONGWORD CONTAINING LOW PART OF ALIGNED FRACTION

:34266 : OP1 FRAC <MS> = LONGWORD CONTAINING MOST SIGNIFICANT BITS OF ALIGNED
:34267 : FRACTION.

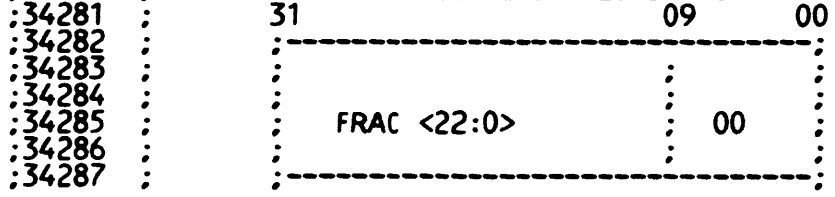
:34268 : SRC = OP1

:34269 : DST = OPX WHERE X IS NUMBER OF OPERANDS.

:34270 : OP1 FRAC <MS> LOOKS LIKE THIS:



:34280 : OP1 FRAC <LS> LOOKS LIKE THIS:



```

:34288 .TOC " G & H floating point : MODIFIED DOUBLE FLOATING -- CMPG"
:34289
:34290 ;DOUBLE PRECISION FLOATING POINT CMP.
:34291
:34292 ;INPUTS:
:34293 : Q = OP1 LONG FRAC
:34294 : RC0 = OP1 LONG EXP
:34295 : D = OP2 LONG FRAC
:34296 : RC2 = OP2 LONG EXP
:34297
:34298 ;ALGORITHM:
:34299 ; THE FOLLOWING TESTS ARE BEING PERFORMED IN ORDER:
:34300 ; 1. EXPONENTS
:34301 ; 2. FRACTION <0:20>
:34302 ; 3. FRACTION <21:36>
:34303 ; 4. FRACTION <37:52>
:34304
:34305 ;OUTPUTS:
:34306 ; SETS CONDITION CODES ON SRC-DST
:34307
:34308 ;TEMPORARIES:
:34309 ;
:34310
:34311 16C1: ;-----: C1 + 1400
:34312 CMPG: TRAP.ACCE1], ; RESET THE FPA
:34313 ID[T1]_D, ; Save OP2 LONG FRAC IN T1
:34314 D_Q, ; D GETS OP1 LONG FRAC
:34315 Q_RC[T0], ; Get OP1 LONG EXP FROM RC0
:34316 SS_ALU15 ; STORE IT IN Q-REG. SS GETS OP1 SIGN
:34317
:34318 ;-----: CMPG
:34319 TRAP.ACCE1], ; RESET THE FPA
:34320 ALU_Q.AND.K[.7FF0], CLK.UBCC ; CLOCK OP1 EXPONENT FOR 0
:34321
:34322 ;-----:
:34323 ID[T2]_D, ; SAVE OP1 LONG FRAC IN T2
:34324 D_RC[T2], ; D GETS OP2 LONG EXP FROM RC2
:34325 SS_SS.XOR.ALU15&SD_ALU15, ; SS gets XOR of two signs,
:34326 ; SD GETS OP2 SIGN
:34327 Z? ; Test OP1 for ZERO
:34328 ;-----:
:34329 =0 ;BRANCH ON ALU Z-BIT
:34330 ;0-----: OP1 NE 0
:34331 CMPG0: ALU_D.AND.K[.7FF0], ; ISOLATE EXPONENT BITS OF OP2
:34332 CLK.UBCC, J/CMPG01
:34333
:34334 ;1-----: OP1 = 0
:34335 ALU_Q.AND.K[.8000], ; ISOLATE SIGN BIT
:34336 CHK_FLT.OPR, ; CHECK FOR -0
:34337 J/CMPG0
:34338 ;-----:

```

J 16C1, 0C10,00B8,C4C1,3D00,0000,1AD6

J 1AD6, 0019,20B4,3880,F800,0010,1ADE

U 1ADE, 0810,0138,C985,3D10,0000,186C

U 186C, 0019,0034,3980,F800,0010,1AE2

U 186D, 0019,2034,4580,F800,0800,186C

```

U 1AE2, 0000,013C,0180,F800,0000,1874 :34339 CMPG01: Z? : TEST FOR OP2 = 0
:34340 :-----:
:34341 =0 :Branch on ALU Z-bit
:34342 :0 : OP2 .NE. 0
:34343 ALU_Q-D, WORD, CLK.UBCC, : Compare exponents, OP1 - OP2
U 1874, 001D,7200,0180,F800,0010,196E :34344 EALD?,J/CMPG1 : Test XOR of signs
:34345 :-----:
:34346 :1 : OP2 .EQ. 0
:34347 ALU_D.AND.K[.8000], : ISOLATE SIGN-BIT OF OP2
U 1875, 0019,0034,4580,F800,0800,1AE6 :34348 CHK.FLT.OPR : CHECK FOR -0
:34349 :-----:
:34350 :-----:
:34351 ALU_Q.AND.K[.FFFF], : Get exponent part of OP1
:34352 N&Z_ALU.V&C_0, WORD, : Set CC FROM OP1
U 1AE6, C019,6034,6D80,F804,4050,0062 :34353 CLR.IB.OPC,PC_PC+1,J/IRD : Complete
:34354 :-----:
:34355 :-----:
:34356 =1110 :Branch on SS-bit
:34357 :1110 : SAME SIGN
:34358 CMPG1: ALU_Q-D, LONG, CLK.UBCC, : CLOCK MS FRACTION BITS, OP1 - OP2
U 196E, 001D,3800,0180,F800,0010,1923 :34359 ALU?, J/CMPG2 : Same sign, BRANCH ON exponents
:34360 :-----:
:34361 :1111 : OPPOSITE SIGNS
:34362 ALU_D.XOR.K[.8000], : Set condition codes on -dst
:34363 :-----:
:34364 N&Z_ALU.V&C_0,WORD, : SINCE SRC MAY BE 0
U 196F, C019,4020,4580,F804,4050,0062 :34365 CLR.IB.OPC,PC_PC+1,J/IRD : Set N and Z from -dst
:34366 :-----:
:34367 :-----:
:34368 =0011 :Branch on ALU z and n-bits
:34369 :0011 :
:34370 CMPG2: ALU_Q.AND.K[.FFFF], : Dst exp is < src exp
:34371 N&Z_ALU.V&C_0, WORD, : Set N and Z from src
U 1923, C019,6034,6D80,F804,4050,0062 :34372 CLR.IB.OPC,-PC_PC+1, J/IRD : COMPLETE
:34373 :-----:
:34374 :0111 :
:34375 R[R15]_D, : Save dst exponent in R15
:34376 Q_ID[T2], : Same exponents, get OP1 LONG FRAC
U 1927, 0001,1B3C,C9F0,2EF8,0000,197A :34377 ALU?, J/CMPG3 : Test high fraction part
:34378 :-----:
:34379 :1011 :
:34380 ALU_D.XOR.K[.8000], :
:34381 N&Z_ALU.V&C_0,WORD, : Set cc from -dst
U 1928, C019,4020,4580,F804,4050,0062 :34382 CLR.IB.OPC,-PC_PC+1, J/IRD : COMPLETE
:34383 =;END :

```



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:34384 : Q = OP1 LONG FRAC
:34385 : R15 = OP2 LONG EXP
:34386 : RCO = OP1 LONG EXP
:34387 : T1 = OP2 LONG FRAC
:34388 : T2 = OP1 LONG FRAC
:34389 :
:34390 =1010 :Branch on ALU Z and C31-bits
:34391 :1010-----: BORROW
:34392 CMPG3: ALU_R[R15].XOR.K[.8000], : Set CC on -dst
:34393 N&Z_ALU.V&C_0, WORD,
:34394 CLR_IB.OPC, -PC_PC+1, J/IRD
:34395
:34396 :1011-----: NO BORROW, NON-ZERO
:34397 ALU_R[R15].XOR.K[.8000], : Set CC on src
:34398 CLR_IB.OPC, -PC_PC+1, J/IRD
:34399
:34400 :1111-----: NO BORROW, ZERO
:34401 =1111 ALU_Q.0XT[WORD], : ISOLATE BITS <47:32> OF DST
:34402 D_ALU, : SAVE IT IN D
:34403 Q_ID[T1] : GET OP2 LONG FRAC
:34404 =;END
:34405
:34406 ALU_Q.0XT[WORD]-D, : CLOCK DIFFERENCE IN BITS <47:32>
:34407 CLK_UBCC, WORD, : DST-SRC
:34408 D_Q.Q_ID[T2] : D GETS DST, Q GETS SRC
:34409
:34410
:34411 CMPG4: ALU_D-Q,CLK_UBCC,ALU? : Clock difference of high fract bits
:34412 : CLOCK DST - SRC
:34413
:34414 =1010 :Branch on ALU Z and C31 bits
:34415 :1010-----: NO BORROW, SRC > DST
:34416 ALU_R[R15].XOR.K[.8000], : Set CC on src
:34417 N&Z_ALU.V&C_0, WORD, : Set N and Z from src
:34418 CLR_IB.OPC, -PC_PC+1, J/IRD
:34419
:34420 :1011-----: BORROW, DST > SRC
:34421 ALU_R[R15].XOR.K[.8000], : set CC on -dst
:34422 N&Z_ALU.V&C_0, WORD,
:34423 CLR_IB.OPC, -PC_PC+1, J/IRD
:34424
:34425 :1111-----:
:34426 =1111 ALU?, J/CMPG5 : TEST DST - SRC <31:0>
:34427 =;END
:34428
:34429 =1010 :Branch on ALU Z and C31 bits
:34430 :1010-----: BORROW, SRC > DST
:34431 CMPG5: ALU_R[R15].XOR.K[.8000],
:34432 N&Z_ALU.V&C_0,
:34433 CLR_IB.OPC, -PC_PC+1, J/IRD
:34434
:34435 :1011-----: NO BORROW, DST > SRC
:34436 ALU_R[R15].XOR.K[.8000], WORD, : Set CC on -dst
:34437 N&Z_ALU.V&C_0,
:34438 CLR_IB.OPC, -PC_PC+1, J/IRD
  
```

U 197A, C018,4020,4580,FA7C,4050,0062

U 197B, C010,4038,0180,F904,4050,0062

U 197F, 0803,603C,C5F0,2C00,0000,1AEA

U 1AEA, 0C1F,6000,C9F0,2C00,0010,1AEE

U 1AEE, 001D,1B00,0180,F800,0010,198A

U 198A, C010,4038,0180,F904,4050,0062

U 198B, C018,4020,4580,FA7C,4050,0062

U 198F, 0C00,1B3C,0180,F800,0000,199A

U 199A, C010,4038,0180,F904,4050,0062

U 199B, C018,4020,4580,FA7C,4050,0062

U 199F, C01D,0000,0180,F804,4050,0062 :34439
:34440 :1111-----: :
:34441 =1111 ALU_D-Q, N&Z ALU.V&C_0, : EQUALITY
:34442 CLR.IB.OPC, PC_PC+1, J/IRD :
:34443 =:END :-----: :

```
.TOC      "      G & H floating point : G FORMAT UNPACK ROUTINE"  
:34444  
:34445  
:34446 :ROUTINE TO UNPACK MODIFIED DOUBL FLOATING OPERANDS.  
:34447  
:34448 :INPUTS:  
:34449 :      Q = OP1 LONG FRAC  
:34450 :      RCO = OP1 LONG EXP  
:34451 :      D = OP1 LONG FRAC (WORD SWAPPED)  
:34452 :      RC2 = OP2 LONG EXP  
:34453 :      RC[16] = OP2 LONG FRAC  
:34454 :      RC3 = OP1 LONG FRAC  
:34455 :      SC = -7  
:34456 :      IR<2:1> = TYPE OF OPERATION BEING PERFORMED:  
:34457 :      00 = ADD, 01 = SUB, 10 = MUL, 11 = DIV  
:34458 :      IN CASE OF EMOVG, HIGH WORD OF RC4 EQUALS EXTENDER  
:34459 :      SS=0 EXCEPT FOR ACBG, WHEN IT IS 1  
:34460  
:34461  
:34462 :OUTPUTS:  
:34463 :      ID[10] = OP1 FRAC <MS>  
:34464 :      Q = ID[2] = OP1 FRAC <LS>  
:34465 :      ID[11] = OP2 FRAC <MS>  
:34466 :      D = OP2 FRAC <LS>  
:34467 :      RC1 = EXP2-EXP1 IF DIVG  
:34468 :      RC[15] = OP1 EXPONENT  
:34469 :      RC[4] = OP2 EXPONENT  
:34470 :      SS = (SIGN OF OPERAND 1) .XOR. (SIGN OF OPERAND 2) .XOR. IR<1>  
:34471 :      EXCEPT FOR ACBG WHEN SS IS COMPLEMENT OF ABOVE  
:34472 :      R15 = (EXPONENT OF OPERAND 2) - (EXP OF OPER 1)  
:34473 :      FE = NABS (LOW BITS OF EXPONENT DIFFERENCE)  
:34474 :      IF IR<2> = 0 (ADD OR SUB)  
:34475  
:34476 :TEMPORARIES:  
:34477 :  
:34478 :      ID[13] = OP1 LONG FRAC (SWAPPED)  
:34479  
:34480 :RETURNS:  
:34481 :  
:34482 :      RETURN @ 1 IF OPERAND 1 = 0  
:34483 :      RETURN @ 2 IF OPERAND 1 <> 0, OPERAND 2 = 0  
:34484 :      RETURN @ 3 IF BOTH OPERANDS ARE NON-ZERO  
:34485
```

```

:34486 UNPACKG:
:34487 -----:
:34488 TRAP.ACC[1], : RESET THE FPA
:34489 ID[T3] D,Q_D, : SAVE OP1 LONG FRAC (SWAPPED) IN T3
:34490 D_RC[T0], : D GETS OP1 LONG EXP
U 1AF2, 0810,00B8,CC5,3D00,0000,1AF3 :34491 SGN/SS.XOR.ALU : SS GETS SIGN (EXCEPT FOR ACBG)
:34492 -----:
:34493
:34494 ALU D.AND.K[.7FF0], : ISOLATE EXPONENT
U 1AF3, 0099,0034,3980,FAF8,0010,1AF4 :34495 R[R15] ALU.RIGHT2, : STORE IT IN R15
:34496 CLK.LBCC : CLOCK ALU Z-BIT
:34497 -----:
:34498
:34499 D D.OR.K[.10], : SET HIDDEN BIT
U 1AF4, 0819,0030,6580,FA78,0000,1AF5 :34500 LAB_R[R15] : LATCH EXPONENT
:34501 -----:
:34502
:34503 ALU D.ANDNOT.K[.20], : CLEAR BIT 5
U 1AF5, 0919,0024,7580,F800,0000,1AF6 :34504 D_ALU(FRAC) : UNPACK OP1
:34505 -----:
:34506
:34507 D DAL.SC, : SHIFT RIGHT 7 BITS (SC=-7)
:34508 SD_SS, : SAVE SS IN SD
:34509 SC_K[A], : SC GETS 10.
U 1AF6, 0D80,173C,F584,FAF8,0084,792D :34510 ALU LA,R[R15]_ALU.RIGHT2, : R15 GETS EXPONENT
:34511 STATE1? : IS THIS EMOG ?
:34512 -----:
:34513
:34514 =1101 : BRANCH ON STATE<1>
:34515 :1101
:34516 LAB_R[R15], : LATCH EXPONENT
U 192D, 0D00,003C,0180,FA78,0000,1AFA :34517 D DAL.SC, : GENERATE SRC FRACTION <MS>
:34518 J/UNPKG.1
:34519 -----:
:34520 :1111
:34521 LAB_R[R15], : EMOG, SHIFT IN EXTENSION
U 192F, 0000,003C,0580,FA78,0084,9AF8 :34522 SC_SC+K[.1] : LATCH EXPONENT
:34523 -----:
:34524
:34525 D_DAL.SC
U 1AF8, 0D00,003C,0180,F800,0000,1AF9 :34526
:34527 -----:
:34528
:34529 ID[T0]_D, : SAVE M'PLIER FRAC <LS> IN TO
:34530 D_Q, : D GETS SRC FRACTION <LS>
U 1AF9, 0C10,0138,C1C0,3D20,0000,18BC :34531 Q_RC[T4], : Q GETS EXTENDER
:34532 Z?,J/UNPKG.2
:34533 -----:
:34534 UNPKG.1:
:34535 ID[T0]_D, : SAVE SRC FRACTION <MS> IN TO
:34536 D_Q, : GET LOW FRACTION READY FOR SHIFT
U 1AFA, 0C00,013C,C1F8,3C00,0000,18BC :34537 Q_Q, : GET READY FOR SHIFT
:34538 Z? : TEST OP1 EXPONENT
```

```

:34539 ;-----:
:34540 =0 ;Branch on alu z-bit
:34541 ;0-----: SRC NE 0
:34542 UNPKG.2:
:34543 D_DAL.SC, ; D GETS SRC FRACTION <LS>
:34544 Q_RC[2], ; GET OPER 2 LONG EXP
:34545 SGN/ADD.SUB,
:34546 FE_K[.10], ; GET READY TO SWAP OP2 LONG FRAC
:34547 J/SRCL0
:34548
:34549 ;1-----: SRC EQ 0
:34550 ALU_RC[0], ; PASS OP1 LONG EXP THRU ALU
:34551 CHK.FLT.OPR ; TEST FOR RESERVED OPERAND
:34552
:34553 ;-----:
:34554 D_RC[2] ; D gets DST LONG EXP
:34555
:34556 ;-----:
:34557 ALU D.AND.K[.7FF0],
:34558 Q_ALU.RIGHT2,
:34559 C[K.UBCC,
:34560 LC_RC[6] ; GET DST <L>
:34561
:34562 ;-----:
:34563 RC[4]_Q.RIGHT2, ; RC4 GETS OP2 EXPONENT
:34564 Z? ; TEST FOR OPER 2 = 0
:34565
:34566 ;-----:
:34567 =0 ;Branch on alu z-bit
:34568 ;0-----: DST.NE.0, SRC = 0
:34569 RC[1]_LC, ; RC1 GETS DST0 <L>
:34570 Q_0, ; CLEAR Q
:34571 RETURN1 ; RETURN1 FOR SRC=0, DST.NE. 0
:34572
:34573 ;1-----: SRC = 0, DST = 0
:34574 ALU D.AND.K[.800C], ; CHECK FOR -0
:34575 CHK.FLT.OPR, ; WHICH IS RESERVED OPERAND
:34576 D_0,Q_0 ; EVERYTHING IS 0
:34577
:34578 ;-----:
:34579 RC[1]_K[ZERO], ; MAKE RESULT 0
:34580 RETURN1
:34581 ;-----:
:34582
:34583
    
```

```

:34584 SRCL0: Q Q.AND.K[.7FF0].RIGHT2,      : ISOLATE OP2 EXPONENT BITS
:34585      CLK.UBCC,                          : CLOCK OPER 2 EXP
U 1B00, 0099,2034,39C0,F928,0010,1B01 :34586      LC_RC[5],                                  : LATCH OPER 1 EXPONENT
:34587      -----
:34588      -----
:34589      ID[2]_D,                            : SAVE OPER 1 FRACTION <LS>
:34590      RC[4]_Q.RIGHT2,Q_SHF,             : STORE OPER 2 EXP IN RC4 AND Q
U 1B01, 0081,213C,C9C0,3DA0,0000,18E4 :34591      Z?,                                : TEST OPER 2 EXPONENT
:34592      -----
:34593      -----
:34594 =0 : BRANCH ON ALU Z-BIT
:34595      0,
:34596      FE K[ZERO],                          : DST NE 0
:34597      D RC[6],                            : FE GETS 16. FOR SWAPPING
U 18E4, 0810,0938,1980,F930,0104,7898 :34598      IR2-1?,J/UNPG2                    : D GETS OP2 LONG FRAC
:34599      -----
:34600      -----
:34601      :1-----
:34602      ALU_RC[2],                          : OPER 2 = 0, OPER 1 NE 0
:34603      CHK.FLT.OPR                          : NEED TO CHECK OP2 FOR -0
U 18E5, 0010,0038,0180,F910,0800,1B02 :34604      -----
:34605      -----
U 1B02, 0810,0038,0180,F900,0000,1B03 :34606      D_RC[0],                            : D GETS OP1 LONG EXP
:34607      -----
:34608      LC_RC[3],                          : LC GETS OP1 LONG FRAC
U 1B03, 0000,003E,0180,F918,0000,0002 :34609      RETURN2
:34610      -----
:34611      -----
:34612 =00 : Branch on low two bits of opcode
:34613 UNPG2: 00-----
:34614      ALU Q-LB,R[R15]_ALU,                : ADDG
:34615      SC_ALU,CLK.UBCC,                    : R15 GETS EXPONENT DIFFERENCE
U 1898, 000D,2000,0180,FAF8,0092,1B04 :34616      J/GH.DSTTST                            : CLOCK DIFFERENCE
:34617      -----
:34618      -----
:34619      :01-----
:34620      ALU Q-LB,R[R15]_ALU,                : SUBG
:34621      SC_ALU,CLK.UBCC,                    : R15 GETS EXPONENT DIFFERENCE
U 1899, 000D,2000,0180,FAF8,0092,1B04 :34622      J/GH.DSTTST                            : CLOCK DIFFERENCE
:34623      -----
:34624      -----
:34625      :10-----
:34626      ALU Q+LB,RC[4]_ALU,                : MULG
:34627      SC_ALU,CLK.UBCC,                    : RC5 GETS EXPONENT SUM
U 189A, 000D,2014,0180,F9A0,0092,1B04 :34628      J/GH.DSTTST                            : CLOCK SUM
:34629      -----
:34630      -----
:34631      :11-----
:34632      ALU Q-LB,R[R15]_ALU,                : DIVG & ACBG
:34633      SC_ALU,CLK.UBCC,                    : R15 GETS EXPONENT DIFFERENCE
U 189B, 000D,2000,0180,FAF8,0092,1B04 :34634      J/GH.DSTTST                            : CLOCK DIFFERENCE
:34635      -----
:34636      -----
    
```

	:34633	GH.DSTTST:	
	:34634	FE NABS(SC-FE),	: GET NEGATIVE EXPONENT DIFFERENCE
U 1B04, 0018,0038,65E0,F800,0182,F805	:34635	ALU_K[.10],SC_ALU,	: SC GETS 16.
	:34636	Q_D	: GET OP2 LONG FRAC
	:34637		
	:34638	-----	
	:34639	D_DAL.SC,	: SWAP WORD DST LONG FRAC
U 1B05, 0D10,0038,BDC0,F910,0084,7B06	:34640	Q_RC[T2],	: GET DST LONG EXP
	:34641	SC_K[.FFF9]	: SC GETS -7
	:34642		
	:34643	-----	
U 1B06, 0019,2030,65C0,F800,0000,1B07	:34644	Q_Q.OR.K[.10]	: SET HIDDEN BIT
	:34645		
	:34646	-----	
	:34647	ALU_Q.ANDNOT.K[.20],	: CLEAR NEXT BIT
U 1B07, 0919,2024,75E0,F800,0000,1B08	:34648	Q_D,	: Q GETS LONG FRAC (SWAPPED)
	:34649	D_ALU(FRAC)	: UNPACK DST LONG EXP
	:34650		
	:34651	-----	
	:34652	ALU_LA,RC[T5]_ALU,	: RC[T5] GETS OP2 EXPONENT
U 1B08, 0D00,003C,F580,F9A8,0084,7B09	:34653	D_DAL.SC,	: SHIFT DST FRAC RIGHT 7 PLACES
	:34654	SC_K[.A]	: SHIFT COUNT OF 10.
	:34655		
	:34656	-----	
U 1B09, 0D00,003C,0180,F800,0000,1B0A	:34657	D_DAL.SC	: GET DST FRAC <MS>
	:34658		
	:34659	-----	
	:34660	LAB_R[R15],	: LATCH EXPONENT DIFFERENCE
U 1B0A, 0C00,003C,C5F8,3E78,0000,1B0B	:34661	ID[T1]_D,	: SAVE DST FRAC <MS> IN T1
	:34662	D_Q, Q_0	: SET UP FRAC <LS>
	:34663		
	:34664	-----	
	:34665	D_DAL.SC,	: D GETS DST FRAC <LS>
	:34666	Q_ID[T2],	: Q GETS SRC FRAC <LS>
U 1B0B, 0D10,003A,C9F0,2D20,0082,0003	:34667	ALU_RC[T4],SC_ALU,	: SC GET DST EXPONENT
	:34668	RETURN3	: RETURN ADDRESS 3 FOR DST AND SRC NE 0
	:34669		

```

:34670 .TOC " G & H floating point : GRAND FLOATING PACK ROUTINE"
:34671
:34672 ;ROUTINE TO PACK GRAND FLOATING POINT RESULT.
:34673
:34674 ;ENTRY: AT 'PACKG'
:34675
:34676 ;INPUTS:
:34677 : D=NORMALIZED FRACTION <MS>, UNROUNDED
:34678 : Q=NORMALIZED FRACTION <LS>, ROUNDED
:34679 : C31=REFLECTS RESULT OF ROUNDING
:34680 : R15=BIASED EXPONENT
:34681 : SD=SIGN
:34682 : STATE<0>=1 IF CALLED FROM POLYG
:34683 : STATE<0>=0 IF NOT CALLED FROM POLYG
:34684 : FE=
:34685 : SC=.FFF5
:34686
:34687 ;OUTPUTS:
:34688 : D=RESULT LONG EXP
:34689 : Q=RC[T1]=RESULT LONG FRAC
:34690 : CONDITION CODES SET ON RESULT
:34691 : TRAP CODES SET IN IDCES] IF UNDERFLOW OR OVERFLOW OCCURS
:34692
:34693 ;TEMPORARIES:
:34694 : T9 = RESULT LONG FRAC
:34695
:34696 -----
:34697 =0* ;BRANCH ON ALU C31
:34698 ;0* -----
:34699 PACKG: TRAP.ACC[1], ; RESET THE FPA
:34700 SC.SC.ANDNOT.K[.FFE0], ; GET SHIFT COUNT OF 21. (= .15)
:34701 LAB R[R15], ; LOAD LATCHES WITH EXPONENT
:34702 C31?,J/PACKG.0 ; TEST CARRY FROM ROUNDING
:34703
:34704 ;1* -----
:34705 R[R15]_LA+K[.1], J/PACKG ; INCREMENT EXPONENT
:34706
:34707 -----
:34708 =0* ;BRANCH ON ALU C31
:34709 ;0* -----
:34710 PACKG.0: ; NO CARRY
:34711 Q_D, ; SAVE FRAC <MS>
:34712 D_DAL.SC, ; D GETS FRAC <LS>
:34713 ALU LA+LB,R[R15]_ALU.LEFT3, ; SHIFT EXPONENT LEFT 4 PLACES
:34714 SC.R[.FFFC], CLK.UBCC, ; SC GETS -4
:34715 J/PACKG.2
:34716
:34717 ;1* -----
:34718 D_D+K[.1], CLK.UBCC ; INCREMENT FRAC <MS>
:34719
:34720 -----
:34721 ALU 0+K[.1], CLK.UBCC, ; CLEAR CARRY
:34722 C31?, J/PACKG ; DID ROUNDING RESULT IN CARRY?
:34723 ;-----

```

U 1889, 0000,03BC,A080,FA78,0084,58B0

U 188B, 0018,0014,0580,FAF8,0000,1889

U 1880, 0DAC,0014,F1E0,FAF8,0094,7B0D

U 1882, 0819,0014,0580,F800,0010,1B0C

U 1B0C, 001B,0314,0580,F800,0010,1889


```

:34724 PACKG.2:
:34725 SC KC.10], : 16. FOR SWAPPING FRAC <LS>
:34726 RC[T1] Q.RIGHT2, : START SHIFTING FRAC <MS> RIGHT
U 1B0D, 0081,373C,65E0,F988,0084,79AB : Q_D.STATE2? : DUPLICATE FRAC <LS>
:34727
:34728
:34729 =1011 :1011-----: NOT ACBG
U 19AB, 0000,003C,0180,F800,0050,19AF : N&Z_ALU.V&C_0 : CLEAR V&C
:34730
:34731
:34732 :1111-----: ACBG,LEAVE V&C ALONE
:34733 D_DAL.SC : GET LONG FRAC IN ORDER
:34734 ALU RC[R15], CLK.UBCC, WORD, : CLOCK EXPONENT
:34735 Q_ALU,
U 19AF, 0D00,573C,01C0,FA78,0010,19BE : STATE0? : IS THIS POLYG?
:34736
:34737
:34738
:34739 =1110 :BRANCH ON STATE<0>
:34740 :1110-----:
:34741 ID[T9] D, : SAVE LONG FRAC IN T9
U 19BE, 0850,1B38,E580,3D08,0000,19C3 : ALU RC[T1],D_ALU.RIGHT, : GET FRAC <MS>
:34742 : ALU?,J/PACKG.3 : TEST FOR OVER/UNDERFLOW
:34743
:34744
:34745 :1111-----:
:34746 ID[T9] D, : SAVE LONG FRAC IN T9
U 19BF, 0850,0038,E580,3D08,0000,19C3 : ALU_RC[T1],D_ALU.RIGHT : GET FRAC <MS>
:34747
:34748
:34749
:34750 =0011 :BRANCH ON ALU Z AND N-BITS
:34751 :0011-----:
:34752 PACKG.3:
U 19C3, 0808,0038,0190,F800,0000,1B11 : D_PACK.FP, : PACK D IN FLOATING FORMAT
:34753 QR/RIGHT2,J/PACKG.4
:34754
:34755
:34756 :0111-----:
:34757 D_0,Q_0,EALU K[ZERO], : FLOATING UNDERFLOW
:34758 RC[T1] K[ZERO], : SET RESULT TO 0
U 19C7, 0F18,0038,19F8,F988,0064,7867 : N&Z_ALU, : SET Z, CLEAR N
:34759 J/PACKG.9
:34760
:34761
:34762 :1011-----:
:34763 D_0,QK/LEFT, : FLOATING OVERFLOW
U 19CB, 0F18,0038,19A8,F988,0060,1B10 : RC[T1] K[ZERO], : SET RESULT TO 0
:34764 : N&Z_ALU : SET Z, CLEAR N
:34765 =:END
:34766
:34767
:34768 Q_0,Q31?,J/PACKG.7 : TEST FOR NEGATIVE EXPONENT
:34769

```

```

:34770
:34771 PACKG.4:
:34772 D D.ANDNOT.K[.7FF0], : CLEAR OUT EXPONENT BITS
U 1B11, 0819,1724,3990,F800,0000,19CE :34773 QR/RIGHT2,STATE0? : KEEP SHIFTING EXPONENT RIGHT
:34774 -----:
:34775 =1110 :BRANCH ON STATE0
:34776 :1110-----:
:34777 D D.OR.R[R15], : ASSEMBLE DATA
:34778 N&Z ALU, WORD, : SET CC
:34779 Q_ID[9], : GET BACK LONG FRAC
U 19CE, 080D,4030,E5F0,2E78,0060,1B14 :34780 J7PACKG.40
:34781 -----:
:34782 :1111-----:
:34783 D D.OR.R[R15],
U 19CF, 080D,4030,0180,FA78,0060,1B12 :34784 N&Z ALU, WORD
:34785 -----:
U 1B12, 0001,203C,0180,F988,0000,1B13 :34786 RC[T1]_Q
:34787 -----:
:34788 :
:34789 Q R[R15],ALU?, : TEST EXPONENT,WORD
U 1B13, 0000,1B3E,01C0,FA78,0000,0010 :34790 RETURN[10]
:34791 -----:
U 1B14, 0001,203E,0180,F988,0000,0010 :34792 PACKG.40:
:34793 RC[T1]_Q, RETURN[10] : FINISHED
:34794 -----:
:34795 :
:34796 =011 :BRANCH ON Q31
:34797 :011-----:
:34798 PACKG.7:
:34799 RC[T7] K[.8], : OVERFLOW CODE
U 1863, 0018,4038,0180,F988,0060,12B4 :34800 N&Z ALU,WORD,
:34801 J/FLOAT.FAULT
:34802 -----:
:34803 :111-----: UNDERFLOW
U 1867, 0000,003C,3DF0,2C00,0000,19D5 :34804 PACKG.9:Q_ID[PSL]
:34805 -----:
:34806 :0101-----:
U 19D5, 0000,003D,0180,F800,0000,12AE :34807 =0101 CALL[PSL.FU.A] : TEST FU
:34808 -----:
:34809 =1101 :1101-----: FU NOT SET IGNORE UNDERFLOW
U 19DD, 0018,003A,19F8,F988,0000,0010 :34810 RC[T1]_K[ZERO],Q_0,RETURN[10]
:34811 -----:
:34812 :1111-----: FU SET, TAKE UNDERFLOW
U 19DF, 0018,0038,F580,F988,0000,12B4 :34813 RC[T7]_K[A],J/FLOAT.FAUL
  
```

```

:34814
:34815 :G-FORMAT FLOATING ADD AND SUBTRACT, *-R.
:34816 :ENTER WITH SRC OPND IN RCO,D, AND DST OPND IN LA.
:34817 142F:
:34818 -----
:34819 TRAP.ACC[1], : RESET THE FPA
:34820 STATE_K[ZERO], : CLEAR POLY FLAG
U 142F, 0000,00BC,1880,F990,1404,7B15 :34821 RC[2]_LA : RC2 GETS OP2 LONG EXP
:34822 -----
:34823 TRAP.ACC[1], : RESET THE FPA
:34824 Q_D, : Q GETS SRC LONG FRAC
U 1B15, 0800,00BC,00E0,F860,0000,18E1 :34825 D_R(PRN+1) : D GETS DST LONG FRAC
:34826 :0****-----
:34827 =0****
:34828 RC[6]_D, : SAVE DST LONG FRAC
:34829 D_Q, : D GETS OP1 LONG FRAC
U 18E1, 0C01,003D,6580,F9B0,0084,78A8 :34830 ST_K[.10], : SC GETS 16. FOR WORD SWAP
:34831 CALL,J/ADDG.S : CALL ADDG SUBROUTINE
:34832 :1****-----
:34833 :RETURN WITH RESULT IN <D,RC1>
:34834 TRAP.ACC[1], : RESET THE FPA
U 18F1, 0001,00BC,0080,F8D8,0000,0796 :34835 R(PRN)_D, J/ADD.P : USE DOUBLE ROUTINE
:34836 =:END
:34837 -----
:34838 :G-FORMAT FLOATING ADD AND SUBTRACT *-***, AND *-MEMORY.
:34839 :ENTER WITH SRC OPND IN <RC0, Q>, DST OPND INN <RC2, D>
:34840 :YIELDS NORMALIZED AND ROUNDED RESULTS.
:34841
:34842 168E: : 1600+8E
:34843 ADDG: -----
U 168E, 0000,00BC,1880,F800,1404,78EC :34844 TRAP.ACC[1], : RESET THE FPA
:34845 STATE_K[ZERO] : CLEAR POLY/EMOD FLAG
:34846 :0****-----
:34847 =0****
:34848 TRAP.ACC[1], : RESET THE FPA
:34849 RC[6]_D, : SAVE OP2 LONG FRAC IN RC6
:34850 D_Q, : D GETS OP1 LONG FRAC
U 18EC, 0C01,00BD,6480,F9B0,0084.78A8 :34851 ST_K[.10], : SC GETS 16. FOR SWAP WORD OF FRAC <L>
:34852 CALL, J/ADDG.S : CALL ADDG/SUBG SUBROUTINE
:34853 -----
:34854 :1****-----
:34855 STATE_K[.1],
U 18FC, F000,003F,05F0,F847,1404,7400 :34856 WRITE_G.DEST, J/WRG : WRITE RESULT
:34857 =:END
:34858 -----

```

```

:34858 :      COMMON GRAND FLOATING ADD/SUB ROUTINE
:34859 :
:34860 :INPUTS:
:34861 :      RC[T0] = OP1 LONG EXP
:34862 :      D = Q = OP1 LONG FRAC
:34863 :      RC[T2] = OP2 LONG EXP
:34864 :      RC[T6] = OP2 LONG FRAC
:34865 :      SC = .10 (HEX)
:34866 :      STATE = 0
:34867 :      IR<1> = 0 IF ADD, 1 IF SUB
:34868 :
:34869 :OUTPUTS:
:34870 :      D= PACKED ROUNDED SUM LONG EXP
:34871 :      RC[T1] = PACKED ROUNDED SUM LONG FRAC
:34872 :      CONDITION CODES AND ID[CES] SET ON SUM
:34873 :
:34874 :TEMPORARIES:
:34875 :      RC3 = OP1 LONG FRAC
:34876 :      T0 = OP1 FRAC <MS>
:34877 :      T1 = OP2 FRAC <MS>
:34878 :      T2 = OP1 FRAC <LS>
:34879 :      R15 = EXPONENT DIFFERENCE
:34880 :
:34881 :
:34882 :RETURNS:
:34883 :      RETURNS AT 10
:34884 :
:34885

```

```

:34886 =00
:34887 ADDG.S:
:34888 -----:
:34889 TRAP.ACC[1], : RESET THE FPA
:34890 SGN/CLR.SD+SS, : CLEAR OUT SS
:34891 RC[3] D, : SAVE OP1 LONG FRAC IN RC3
:34892 D DAL.SC, : SWAP WORDS OF OP1 LONG FRAC
:34893 SC K[.FFF9], : SET UP SHIFT AMOUNT OF -7
U 18A8, 0D01,00BD,BC87,F998,0084,7AF2 :34894 CALL, J/UNPACKG : UNPACK MODIFIED DOUBLE
:34895
:34896 :01-----:
:34897 ALU D,AND.K[.FFF0], : RETURN1, SRC=0, DST MAY BE 0
:34898 NZ ALU.V&C_0,WORD, : CLOCK CONDITION CODES ON EXP & SIGN
:34899 RETURN10 : NO OVERFLOW POSSIBLE
:34900
:34901 :10-----:
:34902 RC[1] LC, : RETURN2, DST = 0, SRC NE 0
:34903 IR1?, J/ADDG.8 : RC1 GETS SRC0 <L>
:34904 : TEST FOR ADD OR SUB
:34905 :11-----:
:34906 : : RETURN3, SRC NE 0, DST NE 0
:34907 : :
:34908 : :
:34909 : :
:34910 : :
:34911 : :
:34912 : :
:34913 : :
:34914 : :
:34915 : :
:34916 : :
:34917 : :
:34918 ADDG.6:
:34919 :RETURN HERE WITH BOTH OPERANDS NON-ZERO.
:34920 :ALU CC REFLECT EXP2-EXP1
:34921
:34922 LC RC[4], : LATCH UP OP1 EXP
:34923 ALD?, J/ADDG.10 : TEST ALU N,Z (FROM EXP2-EXP1)
:34924
:34925 -----:
:34926 =10 :BRANCH ON IR1
:34927 :10-----:
:34928 ADDG.8:
:34929 ALU D,RC[0] ALU,N&Z_ALU.V&C_0, : CALLED BY ADDH AS WELL
:34930 WORD, RETURN10 : RC[0] GETS LONG EXP
:34931 : SET CC ON SRC
:34932 :11-----:
:34933 D D.XOR.K[.8000],RC[0]_ALU, : RESULT IS -SRC
:34934 NZ ALU.V&C_0,WORD, : SET CC
:34935 RETURN10
:34936 -----:
    
```

:34937 : MAIN BRANCHING POINT OF ADDG - ALSO USED BY POLYG AND ACBG.
:34938 : AT THIS POINT, MACHINE STATE IS AS FOLLOWS:
:34939 : INPUTS:
:34940 : D = OP2 FRAC <LS>
:34941 : Q = ID[T2] = OP1 FRAC <LS>
:34942 : ID[T0] = OP1 FRAC <MS>
:34943 : ID[T1] = OP2 FRAC <MS>
:34944 : SD = OP2 SIGN
:34945 : LC = RC4 = OP2 EXP
:34946 : RC6 = OP2 LONG FRAC
:34947 : RC0 = OP1 LONG EXP
:34948 : SS = OP2 SGN.XOR.OP1 SGN.XOR.SUBG
:34949 : R15 = EXP2-EXP1
:34950 : RC4 = EXP2
:34951 : RC5 = EXP1
:34952 : FE = NABS(ALIGNMENT SHIFT)

:34953 :
:34954 : TEMPORARIES:
:34955 : ID[T4] = OP2 FRAC <LS>
:34956 :

:34957 =0011
:34958 ADDG.10:
:34959 :0011-----
:34960 RC[T5]_LC,
:34961 ID[T4]_D,
:34962 D_Q,
:34963 :
:34964 SC FE,
:34965 EALU?,
U 19E3, 0C10,1238,D180,3DA8,0081,184E :34966 J/A:DG.100
:34967

: DST EXP > SRC EXP
: RC5 GETS BIGGEST EXPONENT
: SAVE DST FRAC <LS> IN T4
: D GETS OP1 FRAC <LS>
: SETUP FOR ALIGN SRC FRACTION
: GET SHIFT AMOUNT
: ADD OR SUBTRACT ?

:34968 :0111-----
:34969 SC_K[ZERO],
:34970 FE_K[ZERO],
:34971 LC_RC[T5],
U 19E7, 0000,123C,1980,F928,0184,7A0E :34972 EALU?, J/ADDG.14
:34973

: DST EXP = SRC EXP
: CLEAR EXP-DIFFERENCE
: DO IT THOROUGHLY
: LATCH UP EXPONENT
: ADD OR SUBTRACT ?

:34974 :1011-----
:34975 SC FE,
:34976 Q ID[T1],
:34977 R[R15]_0-LB,
U 19EB, 000F,1200,C5F0,2EF8,0081,180E :34978 EALU?
:34979 =:END ;-----

: DST EXP < SRC EXP
: GET EXPONENT DIFFERENCE
: Q GETS DST FRAC <MS>
: NEGATE EXP2-EXP1
: ADD OR SUBTRACT ?

```

:34980 : ENTER HERE TO DO ADD OR SUBTRACT WHEN DST EXP < SRC EXP
:34981 : EXPECTS:
:34982 : <D,Q> = DST FRACTION, WHICH NEEDS TO BE ALIGNED
:34983 : RC[T5] = SRC EXP
:34984 : SD = DST SIGN
:34985 : SS = SRC SGN.XOR. DST SGN.XOR.IR<1>
:34986
:34987 =001110 :BRANCH ON SS
:34988 :001110-----: DO AN ADDITION
:34989 LC_RC[T5], : LATCH UP EXPONENT
U 180E, 0000,003D,0180,F928,000C,182B :34990 : CALL,J/ALNPOSG : ALIGN DST FRACTION
:34991
:34992 :001111-----: DO A SUBTRACTION
:34993 SD_NOT_SD, : COMPLEMENT DST-SIGN
:34994 LC_RC[T5], : LATCH UP EXPONENT
U 180F, 0000,003D,0183,F928,0000,1B38 :34995 : CALL, J/ALNNEGG
:34996
:34997 =011110 :011110-----: EXP DIFF < 32, ADD
:34998 RC[T2]_D, : SAVE ALIGNED DST FRAC <LS>
:34999 D_Q,Q_0 : GET READY TO ALIGN DST <MS>
U 181E, 0C01,003C,01F8,F990,0000,1B22 :35000 : J7ADDG.24
:35001
:35002 :011111-----: EXP DIFF < 32, SUB
:35003 RC[T2]_D, : SAVE ALIGNED DST FRAC <LS>
U 181F, 0C01,003C,0180,F990,0000,1B21 :35004 : D_Q,J/ADDG.23
:35005
:35006 =101111 :101111-----: 31<EXP DIFF<64, ADD/SUB
:35007 RC[T2]_D, : STORE ALIGNED DST FRAC <LS>
:35008 D_Q, : D GETS 0 OR 1'S
:35009 Q_ID[T2], : GET SRC FRAC <LS>
U 182F, 0C01,003C,C9F0,2D90,0000,1B24 :35010 : J7ADDG.25
:35011
:35012 =111111 :111111-----: 63< EXP DIFF, ADD/SUB
:35013 Q_ID[T0], : Q GETS OP1 FRAC <MS>
:35014 SC_FE
:35015 LC_RC[T5]
U 183F, 0000,003C,C1F0,2D28,0081,1B16 :35016 =:END
:35017
:35018 D_Q,Q_ID[T2], : <D,Q> GETS FRACTION OF OP1
:35019 SC_SC_ANDNOT_FE, : CLEAR SC
U 1B16, 0C00,173C,C9F0,2C00,0080,59EE :35020 : STATE0? : IS THIS POLYG?
:35021
:35022 =1110 :-----: NO
:35023 J/ADDG.31
:35024
:35025 :1111-----: YES
U 19EE, 0000,003C,0180,F800,0000,1A1B :35026 : SS? : SIGNS DIFFERENT?
:35027
:35028 =1110 :-----: NO
:35029 J/ADDG.31
:35030
:35031 :1111-----: YES
U 19FE, 0000,003C,0180,F800,0000,1A1B :35032 : SC_SC+SHF.VAL,D_DAL.NORM : D GETS NORMALIZED FRAC<MS>
:35033
```

```

:35033
:35034
U 1B17, OCC1,003C,01F8,FAF8,0000,1B18 :-----: SAVE FRAC<MS>,SET UP NORM FRAC<LS>
:35035 R[R15]_D,D_Q,Q_0
:35036
:35037
:35038
U 1B18, OD1B,0010,81C0,F800,0000,1B19 :-----: NORM FRAC<LS>,CREATE CONSTANT
:35039 D_DAL.SQ.Q_K[.3FF]+1
:35040
:35041
U 1B19, 001D,2034,0180,F800,0010,1B1A :-----: SEE IF ROUND BIT IS SET
:35042 ALU_Q.AND.V,CLK.UBCC
:35043
:35044
U 1B1A, 0000,013C,01C0,FA78,0000,1B18 :-----: Q_[R15],Z?
:35045
:35046 =0 :0-----: ROUND BIT IS ONE
U 18F8, 0819,0000,0580,F800,0000,18F9 :-----: DECREMENT GUARD BITS
:35047 D_D-K[.1]
:35048
:35049
:35050
U 18F9, 0C01,003C,01F8,FAF8,0000,1B31 :-----: R[R15]_D,D_Q,Q_0,J/ADDG.37
:35051
:35052
:35053 =001110 :BRANCH ON SS
:35054 :001110-----:
:35055 ADDG.100:
:35056 Q_ID[T0],
:35057 CALL[ALNPOSG]
:35058
:35059 :001111-----: SUBTRACT
:35060 Q_ID[T0],
U 184F, 0000,003D,C1F0,2C00,0000,1B38 :-----: GET SRC FRAC <MS>
:35061 CALL[ALNNEGG]
:35062 :011110-----: NEGATE BEFORE ALIGNING
:35063
:35064 ADDG.100.R10:
:35065 : D = ALIGNED SRC FRAC <LS>
:35066 : Q = SRC FRAC <MS>
:35067
:35068 ID[T2]_D,
:35069 D_Q,Q_0,
U 185E, 0C00,003C,C9F8,3C00,0000,1B1C :-----: D = ALIGNED SRC FRAC <LS>
:35070 J7ADDG.21
:35071 :
:35072 :011111-----: SUBTRACT, DST EXP >SRC EXP, <32.
:35073 ID[T2]_D, : SAVE ALIGNED SRC FRAC <LS> IN T2
:35074 D_Q, : D GETS SRC FRAC <MS>
:35075 ACU -1, Q_ALU, : NEED TO SHIFT IN 1'S
U 185F, 0C03,0028,C9C0,3C00,0000,1B1C :-----: GO TO ALIGN <MS>
:35076 J/ADDG.21
:35077
:35078 =101111 :101111-----: ADD/SUB, 31<DIFF EXP < 64
:35079 ID[T2]_D, : SAVE ALIGNED FRAC <LS>
:35080 D_Q, : D GETS SIGN EXTENSION
:35081 Q_D, : Q GETS ALIGNED FRAC <LS>
U 186F, 0C00,003C,C9E0,3C00,0000,1B1E :-----:
:35082 J7ADDG.22
:35083
:35084 =111111 :111111-----: ADD/SUB, 63 < EXP DIFF
:35085 Q_ID[T1], : Q GETS OP2 FRAC <MS>
:35086 ST_FE
U 187F, 0000,003C,C5F0,2C00,0081,1B1B :-----:
:35087 =:END
  
```



```
:35088  
:35089  
:35090 D Q,Q ID[4],  
:35091 SC SC.ANDNOT.FE, <D,Q> GETS FRACTION (=OP2)  
:35092 J/ADDG.31 CLEAR SC  
:35093  
U 1B1B, 0C00,003C,D1F0,2C00,0080,5A1B  
:35094 =1110 ;BRANCH ON SS-BIT  
:35095 ADDG.14:  
:35096 ;1110-----: DST EXP=SRC EXP,ADD  
:35097 R[R15] D+Q, ADD FRAC <LS>'S  
:35098 CLK.UBCC, CLOCK CARRY IF ANY  
:35099 Q ID[1], Q GETS DST FRAC <MS>  
:35100 J7ADDG.26  
:35101  
:35102 ADDG.16:;1111-----: DST EXP= SRC EXP, SUBTRACT  
:35103 R[R15] D-Q, SUBTRACT FRACTIONS <LS>  
:35104 CLK.UBCC, CLOCK BORROW IF ANY  
:35105 Q ID[1], GET DST FRAC <MS>  
:35106 J7ADDG.30  
:35107  
:35108  
U 1A0E, 001D,0014,C5F0,2EF8,0010,1B25  
:35109 ADDG.21:D_DAL.SC, D GETS ALIGNED SRC FRAC <MS>  
:35110 Q_ID[2] Q GETS SRC FRAC <LS>  
:35111  
:35112 ADDG.22:-----: COME HERE IF SRC FRACTION IS ALIGNED  
:35113 ID[0] D, SAVE ALIGNED SRC FRAC <MS> IN TO  
:35114 D_Q D GETS SRC FRAC <LS>  
:35115  
:35116  
U 1A0F, 001D,0000,C5F0,2EF8,0010,1B28  
:35117 ;1110-----: Q GETS DST FRAC <LS>  
:35118 (Q_ID[4],J/ADDG.14  
:35119  
U 1B1C, 0D00,003C,C9F0,2C00,0000,1B1E  
:35120 ADDG.23:-----:  
:35121 ALU_-1, Q_ALU  
:35122  
:35123 ADDG.24:-----: ALIGN DST FRAC <MS>  
:35124 D_DAL.SC, Q GETS SRC FRAC <LS>  
:35125 Q_ID[2]  
:35126  
:35127 ADDG.25:-----: STORE AWAY DST FRAC <MS>  
:35128 ID[1] D, RETRIEVE DST FRAC <LS>  
:35129 D_RC[2], GO AND DO THE ADD  
:35129 J7ADDG.14
```

```

:35130
:35131 ADDG.26:-----:
:35132 D Q, : D GETS ALIGNED DST FRAC <MS>
:35133 Q_ID[T0], : Q GETS ALIGNED SRC FRAC <MS>
U 1B25, 0C00,033C,C1F0,2C00,0000,1901 :35134 C31? : CARRY FROM LS ADD ?
:35135
:35136 -----:
:35137 =0* :BRANCH ON ALU CARRY
:35138 :0*-----:
:35139 D D+Q, : ADD ALIGNED FRAC <MS>'S
:35140 LAB R[R15], CLK.UBCC, : LATCH RESULT FRAC <LS>,
:35141 J/ADDG.27 : SET Z ON FRAC <MS>
:35142
:35143 :1*-----:
:35144 D D+Q+1, : ADD ALIGNED FRAC <MS>'S +1
:35145 LAB_R[R15], CLK.UBCC : LATCH RESULT FRAC <LS>
U 1903, 081D,0010,0180,FA78,0010,1B26 :35146 =:END
:35147 -----:
:35148 ADDG.27:-----:
:35149 SC K[ZERO], : INITIALIZE SHIFT VALUE
:35150 Q R[R15], : Q GETS RESULT FRAC <LS>
U 1B26, 0000,1B3C,19C0,FA78,0084,7A1B :35151 ALU?, J/ADDG.31 : GO TO NORMALIZE
:35152
:35153 -----:
:35154 ADDG.30:-----:
:35155 D Q, : D GETS DST FRAC <MS>
:35156 Q_ID[T0], : Q GETS SRC FRAC <MS>
U 1B28, 0C00,033C,C1F0,2C00,0000,1928 :35157 C31? : WAS THERE A BORROW?
:35158
:35159 -----:
:35160 =0* :BRANCH ON ALU C31
:35161 :0*-----:
:35162 D D-Q-1, : SUBTRAC FRAC'S <MS> WITH BORROW
:35163 CLK.UBCC, : CLOCK ALU N-BIT
:35164 LAB R[R15], : LATCH RESULT FRAC <LS>
U 1928, 081D,0008,0180,FA78,0010,1B29 :35165 J/ADDG.32
:35166
:35167 :1*-----:
:35168 D D-Q, : NO BORROW, SUBTRACT FRAC <MS>
:35169 CLK.UBCC, : CLOCK ALU N-BIT
:35170 LAB R[R15], : LATCH RESULT FRAC <LS>
U 192A, 081D,0000,0180,FA78,0010,1B29 :35171 J/ADDG.32
:35172 =:END
  
```

```

:35173
:35174
:35175 ADDG.32: -----:
:35176 Q R[R15], : Q GETS FRAC <LS>
:35177 ALU? : IS FRAC NEGATIVE ?
:35178
:35179
:35180 =1010 :BRANCH ON ALU Z-BIT AND C31
:35181 :1010 -----:
:35182 SD NOT.SD, : BORROW
:35183 Q 0-Q, : CHANGE SIGN
:35184 CLK.UBCC, : COMPLEMENT FRAC <LS>
:35185 J/ADDG.33 : CLOCK BORROW IF ANY
:35186
:35187 :1011 -----:
:35188 : ENTER HERE FROM EMOVG-ROUTINE.
:35189 : EXPECTS:
:35190 : RC[R15] = BIASSED EXONENT -1
:35191 : <D,Q> = FRACTION
:35192 =1011
:35193 ADDG.31:
:35194 SC SC+SHF.VAL, : POS. DIFF,NORMALIZE RESULT
:35195 D DAL.NORM, : D GETS NORMALIZED FRAC<MS>
:35196 J7ADDG.36
:35197
:35198 :1111 -----:
:35199 =1111
:35200 SC K[.20], : SHIFT VALUE OF 32
:35201 D 0, 0 0, : SET FRAC <MS>, CLEAR FRAC <LS>
:35202 J7ADDG.31
:35203
:35204
:35205 ADDG.33:
:35206 D NOT.D, CLK.UBCC, : 1'S COMPLEMENT OF FRAC <MS>
:35207 Z? : IS FRAC <LS> = 0 ?
:35208
:35209
:35210 =0 :BRANCH ON ALU Z-BIT
:35211 :0 -----:
:35212 ALU?, J/ADDG.31 : NO, IS FRAC<MS> = 0 ?
:35213
:35214 :1 -----:
:35215 D D+K[.1], : YES, MAKE FRAC <MS> 2'S COMPLEMENT
:35216 J7ADDG.31
:35217 =:END :
:35218
  
```

```

:35219 :      D = FRAC <MS>
:35220 :      Q = FRAC <LS>
:35221 :      LC = EXP
:35222 :      SC = NUMBER OF LEADING 0'S
:35223
:35224 ADDG.36:
:35225 -----:
:35226 R[R15]_D,      : ENTER WITH FRAC<MS> NORMALIZED
:35227 D_Q, Q_0      : SAVE FRACTION <MS> IN R15
:35228 :              : SETUP FOR NORMALIZE FRAC <LS>
:35229 -----:
:35230 D_DAL.SC,      : NORMALIZE FRAC <LS>
:35231 Q_R[R15]     : Q GETS BACK FRAC <MS>
:35232 -----:
:35233
:35234 R[R15]_D,      : SAVE NORMALIZED FRAC <LS>
:35235 D_Q, Q_0      : D GETS FRAC <MS>
:35236
:35237 ADDG.37:
:35238 LAB R[R15],    : LATCH FRAC <LS>
:35239 ALU_LA[OR]D,CLK.UBCC, : CHECK IF RESULT FRAC IS 0
:35240 FE_R[.18]    : GET READY TO PACK RESULT
:35241 -----:
:35242
:35243 LC_RC[5],     : LATCH EXPONENT
:35244 K[.3FF], Z?  : SLOW CONSTANT FOR ROUNDING
:35245
:35246 =0           : 0-----:
:35247 R[R15]_LA+K[.3FF]+1, : ROUND FRACTION
:35248 CLK.UBCC     : CLOCK CARRY IF ANY
:35249 J/ADDG.38   : PACK UP RESULT
:35250 -----:
:35251 : 1-----:
:35252 RC[1]_K[ZERO], D_0,   :
:35253 SET.CC(INST),      :
:35254 Q_0               :
:35255 =:END           :
:35256 -----:
:35257 ID[9]_D,RETURN10   : CLEAR LOW FRAC AND RETURN
:35258
:35259 ADDG.38:
:35260 -----:
:35261 Q_0+LC+1,      : INCREMENT EXPONENT TO COMPENSATE
:35262 :              : FOR SHIF'T VALUE
:35263 LAB_R[R15]     : LATCH FRAC <LS> ROUNDED
:35264 -----:
:35265
:35266 R[R15]_Q-K[SC]   : SUBTRACT # OF LEADING 0'S FROM EXP
:35267 -----:
:35268
:35269 SC_K[.FFF5],    : GET READY FOR PACKG-ROUTINE
:35270 Q_LA,          : Q GETS FRAC <LS>
:35271 J7PACKG       : PACK UP THE RESULT
    
```

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:35272 :ADDG/SUBG ALIGNMENT SUBROUTINE, ENTER FROM ADDG.100 BRANCH TARGETS WITH:
:35273 :INPUTS:
:35274 : <Q,D>=FRACTION TO BE ALIGNED
:35275 : TO = SRC FRAC <MS>
:35276 : FE=SC=AMOUNT TO ALIGN IT
:35277 : LC=LARGER OF SRC EXP AND DST EXP
:35278 : R15 = OP2 EXP - OP1 EXP
:35279 : ALU CC REFLECT R15
:35280 : ENTRY IS AT ALNNEGG IF <Q,D> SHOULD BE NEGATED FIRST. ELSE AT ALNPOSG.
:35281 :
:35282 : THERE ARE SEVERAL RETURN POINTS:
:35283 : RETURN10 IF EXP DIFF < 32.
:35284 : RETURN21 IF 32.<=EXP DIFF
:35285 : RETURN31 IF EXP DIFF > 63
:35286 :
:35287 ALNNEGG:
:35288 :-----:
U 1B38, 081F,2000,0180,F800,0010,1B39 : D_0-D, CLK.UBCC ; NEGATE LOW PART FIRST
:35289 :
:35290 :-----:
:35291 :
U 1B39, 001F,0300,01C0,F800,0000,1B29 : Q_0-Q, C31? ; NEGATE HIGH PART, CHECK BORROW
:35292 :
:35293 :
:35294 =01 :01-----:BRANCH ON BORROW
U 1829, 0019,2000,05C0,F800,0000,182B : Q_Q-K[.1] ; SUBTRACT BORROW FROM HIGH PART
:35295 :
:35296 :
:35297 ALNPOSG:
:35298 :11-----:
U 182B, 0018,0024,8D80,FA78,0010,1B3A : LAB_R[R15], ; LATCH UP EXPONENT DIFFERENCE
:35299 : ALU_LA.ANDNOT.K[.1F], CLK.UBCC ; CLEAR ALU Z IF EXP DIFF >= 32.
:35300 :
:35301 :-----:
:35302 :
U 1B3A, 0018,0124,5580,F800,0010,193C : ALU_LA.ANDNOT.K[.3F], CLK.UBCC, ; CLEAR ALU Z IF EXP DIFF > 63
:35303 : Z? ; TEST FOR >= 32.
:35304 :
:35305 :
:35306 =0 :0-----:BRANCH ON ALU Z-BIT
U 193C, 0C03,1228,75C0,F800,0084,9A2E : SC_SC+K[.20] D_Q,ALU_-1,Q_ALU, ; EXP DIFF >= 32
:35307 : EALU?,J/ALN.00 ; TEST FOR NEGATIVE FRACTION
:35308 :
:35309 :
:35310 :1-----:
U 193D, 0D00,003E,0180,F800,0000,0010 : D_DAL.SC, RETURN[10] ; EXP DIFF < 32
:35311 :
:35312 :
:35313 =1110
:35314 ALN.00: :1110-----:BRANCH ON SS
U 1A2E, 0000,013C,01F8,F800,0000,1940 : Q_0,Z?,J/GH.ALN.01
:35315 :
:35316 :
:35317 :1111-----:
U 1A2F, 0000,013C,0180,F800,0000,1940 : Z? ; TEST FOR EXP DIFF >= 64
:35318 :
:35319 =0
:35320 GH.ALN.01:
:35321 :0-----:BRANCH ON ALU Z-BIT
U 1940, 0810,003A,C1F0,2D10,0000,0031 : D_RC[T2], ; EXP DIFF > 63, READ DST LONG EXP
:35322 : Q_ID[T0], RETURN[31] ; HOPELESS, GET SRC FRAC <MS>
:35323 :
:35324 :
:35325 :1-----:
U 1941, 0D00,003E,0180,F800,0000,0021 : D_DAL.SC, RETURN[21] ; 31< EXP DIFF < 64
:35326 :
    
```

```
:35327 .TOC " G & H floating point : GRAND FLOATING POINT MULTIPLY"  
:35328  
:35329 : GRAND FLOATING MULTIPLY ROUTINE.  
:35330  
:35331 : FIRST MULG2, *-R  
:35332  
:35333 :INPUTS:  
:35334 : D = OP1 LONG FRAC  
:35335 : RCO = OP1 LONG EXP  
:35336 : LA = LB = OP2 LONG EXP  
:35337  
:35338 :-----:  
U 1420, 0000,00BC,18E0,F990,1404,7921 :35339 1420: TRAP.ACC[1], : RESET THE FPA  
:35340 STATE_K[ZERO], : CLEAR POLYG FLAG  
:35341 RC[2]_LA, : RC2 GETS OP2 LONG EXP  
:35342 Q_D : Q GETS OP1 LONG FRAC  
:35343  
:35344 =0**** :0****:-----: CALL SITE FOR ADD/SUB  
U 1921, 0800,003D,0180,F860,0000,184C :35345 D_R(PRN+1), : D GETS OP2 LONG FRAC  
:35346 CALL, J/MULG.00 : CALL MULTIPLY ROUTINE  
:35347  
:35348 :1****:-----:  
U 1931, 0001,003C,0180,F8D8,0000,0796 :35349 R(PRN)_D, : STORE RESULT LONG EXP  
:35350 J/ADD.P : STORE RESULT LONG FRAC  
:35351 =:END :-----:  
:35352  
:35353 :MULG, *-MEMORY, AND *-*-  
:35354  
:35355 :INPUTS:  
:35356 : <RC0,Q> = PACKED MULTIPLIER  
:35357 : <RC2,D> = PACKED MULTIPLICAND  
:35358  
:35359 168F: :-----: 1600+8F  
:35360 MULG: :-----:  
U 168F, 0000,00BD,1880,F800,1404,7B4C :35361 TRAP.ACC[1], : RESET THE FPA  
:35362 STATE_K[ZERO], : Clear POLY-flag  
:35363 CALL,J/MULG.00 : MULTIPLY SUBROUTINE  
:35364  
:35365 169F: :-----:  
U 169F, F000,003F,05F0,F847,1404,7400 :35366 STATE_K[.1], : FLAG TO SIGNAL WRITE-DEST AT 1441  
:35367 WRITE.G.DEST, J/WRG : WRITE RESULT  
:35368 :-----:
```

```

:35369 .TOC " G & H floating point : DIVIDE GRAND FLOATING ROUTINE"
:35370
:35371 :DIVG2, *-R
:35372 :INPUTS:
:35373 :
:35374 : D = OP1 LONG FRAC
:35375 : RCC = OP1 LONG EXP
:35376 : LA = LB = OP2 LONG EXP
:35377 1421: -----:
:35378 TRAP.ACC[1], : RESET THE FPA
:35379 RC[T2]_LA, : RC2 GETS OP2 LONG EXP
:35380 Q_D
:35381
:35382 -----:
:35383 D_R(PRN+1) : D GETS DST LONG FRAC
:35384
:35385 =0**** :0****-----: CALLSITE FOR DIVIDE SUBR
:35386 RC[T6]_D, : SAVE DST LONG FRAC
:35387 D_Q, : D GETS OP1 LONG FRAC
:35388 ST K[.10], : 16. FOR WORD SWAP
:35389 CALL, J/DIVG.S
:35390
:35391 :1****-----:
:35392 ALU_D,N&Z,ALU.V&C_0, WORD, : SET CONDITION CODES
:35393 PSL.V?, J7ADDD.M : TEST FOR OVERFLOW
:35394 =:END :-----:
    
```

U 1421, 0000,00BC,00E0,F990,0000,1B3B

U 1B3B, 080C,003C,0180,F860,0000,196C

U 196C, 0C01,003D,6580,F9B0,0084,78B8

U 197C, 0001,5A3C,0180,F800,0050,00FC

```

:35395 :DIVG, *-MEMORY, AND *-*-
:35396
:35397 :INPUTS:
:35398 :           D = OP2 LONG FRAC
:35399 :           RC2 = OP2 LONG EXP
:35400 :           Q = OP1 LONG FRAC
:35401 :           RCO = OP1 LONG EXP
:35402
:35403 168D: :-----: 1600 + 8D
:35404 DIVG: TRAP.ACC[1], : RESET THE FPA
:35405 : RC[6]_D, : SAVE OP2 LONG FRAC IN RC6
:35406 : D_Q, : D GETS OP1 LONG FRAC
:35407 : ST_K[.10], : 16. FOR WORD SWAP
U 168D, 0C01,00BD,6480,F9B0,0084,78B8 :35408 : CALL, J/DIVG.S : CALL DIVIDE GRAND SUBROUTINE
:35409
:35410 169D: :-----:
U 169D, 0001,5A3C,0180,F800,0050,182C :35411 : ALU_D,N&Z_ALU.V&C_0, WORD, : SET CC ON DST
:35412 : PSL.V? : NEED TO RESET V?
:35413 =:END
:35414 :-----:
:35415 =110* :BRANCH ON PSL V-BIT
:35416 :110* :-----:
U 182C, F000,003F,05F0,F847,1404,7400 :35417 : STATE_K[.1], : SIGNAL WRITE-DEST AT 1441
:35418 : WRITE.G.DEST, J/WRG : NO, JUST WRITE DESTINATION
:35419
:35420 :111* :-----:
:35421 : STATE_K[.1], : SIGNAL WRITE-DEST AT 1441
U 182E, F000,003F,05F0,F847,1424,7400 :35422 : SET.V, : SET V
:35423 : WRITE.G.DEST, J/WRG
:35424 :-----:
  
```



```

:35425 :GRAND FLOATING DIVIDE SUBROUTINE
:35426
:35427 :ALGORITHM:
:35428 :           NON-RESTORING DIVIDE IN TWO LOOPS, ONE FOR
:35429 :           FIRST 32 BITS OF QUOTIENT, AND ONE FOR NEXT 18 BITS.
:35430
:35431 :INPUTS:
:35432 :           RCO = OP1 LONG EXP
:35433 :           D = Q = OP1 LONG FRAC
:35434 :           RC1 = OP2 LONG EXP
:35435 :           RC6 = OP2 LONG FRAC
:35436 :           SC = 16.
:35437 :OUTPUTS:
:35438 :           D = PACKED ROUNDED QUOTIENT (LONG EXP)
:35439 :           RC1 = ROUNDED QUOTIENT LONG FRAC
:35440 :           CC AND ID[CCES] SET FROM QUOTIENT
:35441 :TEMPORARIES:
:35442 :           RC3 = OP1 LONG FRAC
:35443 :           RC4 = DIVISOR FRAC <MS>
:35444 :           R15 =
:35445 :           ID[3] = R1 DURING MAIN LOOP
:35446 :           ID[4] = OP2 FRAC <LS>
:35447 :RETURNS:
:35448 :           RETURN @ 10
:35449
:35450 =00
:35451 DIVG.S: -----;
:35452 TRAP.AC[C1], ; RESET THE FPA
:35453 SGN/CLR.SD+SS, ; CLEAR OUT SS
:35454 RC[3] D, ; SAVE OP1 LONG FRAC IN RC3
:35455 D DAL.SC, ; SWAP THE TWO WORDS OF OP1 LONG FRAC
:35456 ST KC.FFF9], ; SET UP SHIFT AMOUNT OF -7
:35457 CALL, J/UNPACKG ; UNPACK GRAND SUBROUTINE
:35458
:35459 :01-----; DIVISOR IS 0
:35460 D K[.8000], ; RESERVED OPERAND
:35461 N&Z ALU.V&C_0, ; CLOCK CONDITION CODES
:35462 J/DIVD.20 ; USE DIVIDE DOUBLE ROUTINE
:35463
:35464 :10-----; DIVIDEND IS 0
:35465 RC[1] K[ZERO], D 0, ; CLEAR OUT QUOTIENT
:35466 N&Z ALU.V&C_0,WORD, ; SET CONDITION CODES
:35467 RETURN10
:35468
:35469 :11-----; SRC NE 0, DST NE 0
:35470
:35471 :           ID[0] = OP1 FRAC <MS> = DIVISOR FRAC <MS>
:35472 :           Q = ID[2] = OP1 FRAC <LS> = DIVISOR FRAC <LS>
:35473 :           ID[1] = OP2 FRAC <MS> = DIVIDEND FRAC <MS>
:35474 :           D = OP2 FRAC <LS> = DIVIDEND FRAC <LS>
:35475 :           RC5 = OP1 EXP
:35476 :           RC4 = OP2 EXP
:35477 :           R15 = LAB = EXP2-EXP1
:35478
U 188B, 0000,0C3C,0180,F988,0000,1B3C :35478 ALU_LA,RC[1]_ALU ; STORE EXP2-EXP1 IN RC1
    
```

```

:35479
:35480 R[R15]_Q, : STORE DIVISOR FRAC <LS> IN R15
:35481 Q_D, : Q GETS DIVIDEND FRAC <LS>
:35482 SD_SS, : SD GETS MINUS RESULT SIGN
U 1B3C, 0001,203C,51E4,FAF9,0184,7B3E : FE_K[.1E],SC_K[.1E] : LOOP COUNT
:35484
:35485
:35486 SD NOT_SD, : FIX UP RESULT SIGN
U 1B3E, 0800,003C,0183,FA08,0000,1B40 : D_[R1] : NEED TO SAVE R1
:35487
:35488
:35489
:35490 ID[T3]_D, : SAVE R1 IN T3
:35491 D_Q, : D GETS DIVIDEND FRAC <LS>
U 1B40, 0C03,0028,CD80,3E78,0050,1B41 : ALU_-1,NBZ_ALU.V&C_0, : SET PSL N-BIT
:35492 : LAB_[R15] : LATCH D'SOR FRAC <LS>
:35493
:35494
:35495
:35496 ALU D-LB.RLOG, : SUBTRACT <LS> FRACTIONS
:35497 R[R1] ALU.LEFT,SI/ZERO, : STORE RESULT IN R1
U 1B41, 002D,0004,C1F0,2E88,0010,1B42 : CLK.UBCC, : CLOCK BORROW
:35498 : Q_ID[T0] : GET D'SOR FRAC <MS>
:35499
:35500
:35501
:35502 RC[T4]_Q, : RC4 GETS D'SOR FRAC <MS>
U 1B42, 0001,203C,C5F0,2DA0,1C00,1B54 : Q_ID[T1], : Q GETS DIVIDEND FRAC <MS>
:35503 : MSC/READ.RLOG : POP REGISTER-LOG
:35504
:35505
:35506 :10*-----:
:35507 =10*
:35508 LC_RC[T4], : LATCH D'SOR FRAC <MS>
:35509 D_Q_Q_0 : D GETS D'END FRAC <MS>
:35510 SC_SC-K[.1], : ADJUST LOOP COUNT
U 1B54, 0C00,1B3D,05F8,F920,0084,BA36 : ALU?, : TEST FOR BORROW
:35511 : CALL,J/DIVG.0
:35512
:35513
:35514 :11*-----:
:35515 D_Q, : D GETS QUOTIEN FRAC <LS>
:35516 Q_ID[T3], : Q GETS OLD VALUE OF R1
U 1B56, 0C00,003C,CDF0,2E78,0000,1B46 : LAB_[R15], : LATCH QUOTIEN FRAC <MS>
:35517 : J/DIVG.16
:35518
:35519 =:END :

```

```

:35520 =0110
:35521 DIVG.0: :0110-----:
:35522 ALU D-LC-1, :
:35523 D_ALU.LEFT, :
:35524 Q_Q.LEFT,S1/DIV, :
:35525 CLK.UBCC, :
U 1A36, 0831,0008,02A8,F888,0010,1B44 :35526 LA_RA[R1],J/DIVG.00 :
:35527
:35528 :0111-----:
:35529 ALU D-LC, :
:35530 D_ALU.LEFT, :
:35531 Q_Q.LEFT,S1/DIV, :
:35532 CLK.UBCC, :
U 1A37, 0831,0000,02A8,F888,0010,1B44 :35533 LA_RA[R1],J/DIVG.00 :
:35534
:35535 :1110-----:
:35536 ALU D-LC-1, :
:35537 D_ALU.LEFT, :
:35538 Q_Q.LEFT,S1/DIVD, :
:35539 CLK.UBCC, :
U 1A3E, 0831,0008,0028,F888,0010,1B44 :35540 LA_RA[R1],J/DIVG.00 :
:35541
:35542 :1111-----:
:35543 ALU D-LC, :
:35544 D_ALU.LEFT, :
:35545 Q_Q.LEFT,S1/DIVD, :
:35546 CLK.UBCC, :
U 1A3F, 0831,0000,0028,F888,0010,1B44 :35547 LA_RA[R1] :
:35548 =:END
:35549 DIVG.00: :
:35550 C31? :
:35551
:35552 =00* :00*-----:
:35553 LC_RC[T4]&R1_(LA+LB+PSL.C).LEFT, :
:35554 SI7ZERO, :
:35555 CLK.UBCC, :
U 18D0, 002C,002D,0180,FBA0,0090,D9CA :35556 SC_SC+1, :
:35557 CALL,J/DIVG.081 :
:35558
:35559 :01*-----:
:35560 STATE_STATE.OR.K[.80], :
:35561 LC_RC[T4]&R1_(LA-LB.RLOG).LEFT, :
:35562 SI7ZERO, :
:35563 CLK.UBCC, :
U 18D2, 002C,0005,4180,FBA0,1414,398E :35564 CALL,J/DIVG.061 :
:35565
:35566 :11*-----:
:35567 SC_SC-K[.1], :
:35568 R[R15]_Q, :
:35569 Q_0, :
U 18D6, 0001,233C,05F8,FAF8,0084,B99C :35570 C31?,J/DIVG.063 :
:35571 =:END
    
```

BORROW
 SUBTRACT <MS> FRACS WITH BORROW
 SHIFT TO GET READY FOR NEXT OPERATION
 SHIFT IN QUOTIENT BIT (=ALU31=0)
 FLAG RESULT FOR NEXT OPERATION, +/-
 GET LA READY

NO BORROW
 SUBTRACT <MS> FRACS
 SHIFT TO GET READY FOR NEXT OPERATION
 SHIFT IN QUOTIENT BIT (=ALU31)
 FLAG RESULT FOR NEXT OPERATION, +/-
 GET LA READY

BORROW
 SUBTRACT <MS> FRACS WITH BORROW
 SHIFT TO GET READY FOR NEXT OPERATION
 SHIFT IN QUOTIENT BIT (=ALU31=1)
 FLAG RESULT FOR NEXT OPERATION, +/-
 GET LA READY

NO BORROW
 SUBTRACT <MS> FRACS
 SHIFT TO GET READY FOR NEXT OPERATION
 SHIFT IN QUOTIENT BIT (=ALU31=1)
 FLAG RESULT FOR NEXT OPERATION, +/-
 GET LA READY

ADD OR SUBTRACT NEXT ?

BORROW
 ADD DIVISOR<LS> TO D'END <LS>
 SHIFT IN ZEROS
 CLOCK ALU CARRY
 INCREMENT LOOP COUNT BY 1
 SINCE FIRST QUOTIENT BIT IS 0

NO BORROW
 SET FLAG TO INCREMENT EXP BY 1
 SUBTRACT DIVISOR<LS> FROM DIV<MS>
 SHIFT IN ZEROS
 CLOCK ALU BORROW

ADJUST LOOP COUNT
 FRACTION <MS>
 INITAILIZE QUOTIENT

```

:35572 ; ENTER HERE TO DO THE SECOND HALF OF A SUBTRACT-OPERATION
:35573 ; BRANCH ON SC GT 0.
:35574
:35575 =*0* ;BRANCH ON SC GT 0
:35576 :*0*-----:
:35577 DIVG.06:SC K[.18], ; LOOP COUNT FOR NEXT PASS
:35578 MSC/READ.RLOG, ; POP REGISTER-LOG
U 198C, 0000,1B3C,7D80,F800,1C84,7A66 :35579 ALU?,J/DIVG.064 ; END OF FIRST LOOP
:35580
:35581 :*1*-----:
U 198E, 0000,003C,0180,F800,1C00,1B45 :35582 DIVG.061:MSC/READ.RLOG ; POP REGISTER-LOG
:35583 =;END
:35584
:35585 ALU D-LC,CLK.UBCC, ; CLOCK DIFFERENCE
U 1B45, 0011,1B00,0180,F800,0010,1A46 :35586 ALU? ; TEST RESULT OF <LS> SUBTRACT
:35587
:35588
:35589 =0110 ;BRANCH ON ALU N&Z-BITS
:35590 :0110-----:
:35591 ALU D-LC-1, ; BORROW
:35592 D_ACU.LEFT,SI/DIV, ; SUBTRACT WITH BORROW
:35593 Q_Q.LEFT ; SHIFT IN QUOTIENT BIT
:35594 LA RA[R1],
:35595 CLR.UBCC,
U 1A46, 0831,1B08,02A8,F888,0010,1A5A :35596 ALU?,J/DIVG.062
:35597
:35598 :0111-----: NO BORROW
:35599 ALU D-LC, ; SUBTRACT
:35600 D_ACU.LEFT,SI/DIV, ; SHIFT IN QUOTIENT BIT
:35601 Q_Q.LEFT,
:35602 LA RA[R1],
U 1A47, 0831,0300,02A8,F888,0010,199C :35603 CLR.UBCC,
:35604 C31?,J/DIVG.063
:35605
:35606 :1110-----: BORROW
:35607 ALU D-LC-1, ; SUBTRACT WITH BORROW
:35608 D_ACU.LEFT,SI/DIVD, ; SHIFT IN QUOTIENT BIT
:35609 Q_Q.LEFT,
:35610 LA RA[R1],
U 1A4E, 0831,1B08,0028,F888,0010,1A5A :35611 CLR.UBCC,
:35612 ALU?,J/DIVG.062
:35613
:35614 :1111-----: NO BORROW
:35615 ALU D-LC, ; SUBTRACT
:35616 D_ACU.LEFT,SI/DIVD, ; SHIFT IN QUOTIENT BIT
:35617 Q_Q.LEFT,
:35618 LA RA[R1],
U 1A4F, 0831,0300,0028,F888,0010,199C :35619 CLR.UBCC,
:35620 C31?,J/DIVG.063
```

```

:35621 -----;
:35622 =1010 ;BRANCH ON ALU Z AND C-BITS
:35623 ;1010-----;
:35624 DIVG.062:LC RC[T4]&R1_(LA+LB+PSL.C).LEFT,; R1 GETS D'END FRAC <LS>
:35625 SI/ZERO,; SHIFT IN ZEROES
:35626 CLK.UBCC,; CLOCK THE CARRY
:35627 SC_SC-K[.1],
:35628 SC.GT.0?,J/DIVG.08
:35629
:35630 ;1011-----;
:35631 LC RC[T4]&R1_(LA-LB.RLOG).LEFT,; R1 GETS D'END FRAC <LS>
:35632 SI7ZERO,; SHIFT IN ZEROES
:35633 CLK.UBCC,; CLOCK THE CARRY
:35634 SC_SC-K[.1],
:35635 SC.GT.0?,J/DIVG.06
:35636
:35637 =1111 ;1111-----; ACTUALLY A BORROW RESULTED
:35638 LC RC[T4]&R1_(LA+LB+PSL.C).LEFT,; R1 GETS D'END FRAC <LS>
:35639 SI7ZERO,; SHIFT IN ZEROES
:35640 CLK.UBCC,; CLOCK THE CARRY
:35641 SC_SC-K[.1],
:35642 SC.GT.0?,J/DIVG.08
:35643 =:END
:35644 -----;
:35645 =0* ;BRANCH ON ALU C31
:35646 ;0*-----;
:35647 DIVG.063:LC RC[T4]&R1_(LA+LB+PSL.C).LEFT,; R1 GETS D'END FRAC <LS>
:35648 SI/ZERO,; SHIFT IN ZEROES
:35649 CLK.UBCC,; CLOCK THE CARRY
:35650 SC_SC-K[.1],
:35651 SC.GT.0?,J/DIVG.08
:35652
:35653 ;1*-----;
:35654 LC RC[T4]&R1_(LA-LB.RLOG).LEFT,; R1 GETS D'END FRAC <LS>
:35655 SI7ZERO,; SHIFT IN ZEROES
:35656 CLK.UBCC,; CLOCK THE CARRY
:35657 SC_SC-K[.1],
:35658 SC.GT.0?,J/DIVG.06
:35659 =:END
  
```

U 1A5A, 002C,142C,0580,FBA0,0094,B9C8
 U 1A5B, 002C,1404,0580,FBA0,0094,B9C8
 U 1A5F, 002C,142C,0580,FBA0,0094,B9C8
 U 199C, 002C,142C,0580,FBA0,0094,B9C8
 U 199E, 002C,1404,0580,FBA0,0094,B9C8

```

:35660 :-----:
:35661 =0110 :BRANCH ON ALU N&C-BITS
:35662 :0110 :-----:
:35663 DIVG.064:ALU D-LC-1, : BORROW
:35664 D_ALU.LEFT,SI/DIV, : SUBTRACT WITH BORROW
:35665 Q_Q.LEFT : SHIFT IN QUOTIENT BIT
:35666 LA RA[R1],
:35667 CLR.UBCC,
:35668 RETURN[6]
U 1A66, 0831,000A,02A8,F888,0010,0006
:35669
:35670 :0111:-----: NO BORROW
:35671 ALU D-LC, : SUBTRACT
:35672 D_ALU.LEFT,SI/DIV, : SHIFT IN QUOTIENT BIT
:35673 Q_Q.LEFT,
:35674 LA RA[R1],
:35675 CLR.UBCC,
:35676 RETURN[6]
U 1A67, 0831,0002,02A8,F888,0010,0006
:35677
:35678 :1110:-----:
:35679 ALU D-LC-1, : SUBTRACT WITH BORROW
:35680 D_ALU.LEFT,SI/DIVD, : SHIFT IN QUOTIENT BIT
:35681 Q_Q.LEFT,
:35682 LA RA[R1],
:35683 CLR.UBCC,
:35684 RETURN[6]
U 1A6E, 0831,000A,0028,F888,0010,0006
:35685
:35686 :1111:-----: NO BORROW
:35687 ALU D-LC, : SUBTRACT
:35688 D_ALU.LEFT,SI/DIVD, : SHIFT IN QUOTIENT BIT
:35689 Q_Q.LEFT,
:35690 LA RA[R1],
:35691 CLR.UBCC,
:35692 RETURN[6]
U 1A6F, 0831,0002,0028,F888,0010,0006
:35693
  
```

```

:35694 :-----;
:35695 =0* :BRANCH ON SC GT 0
:35696 :0*-----;
U 19C8, 0000,1B3C,7D80,F800,0084,7A86 :35697 DIVG.08:SC KC.18],ALU?,
:35698 :J/DIVG.084
:35699
:35700 :1*-----;
:35701 DIVG.081:ALU D+LC+1,
:35702 CLK.UBCC,
U 19CA, 0011,1B10,0180,F888,0010,1A76 :35703 LA RA[R1],
:35704 ALU? ; CHECK FOR CARRY AND N-BIT
:35705
:35706 :-----;
:35707 =0110 :BRANCH ON ALU N&C-BITS
:35708 :0110-----; NO CARRY
:35709 ALU D+LC,
:35710 D ACU.LEFT,SI/DIV, ; ALU N-BIT IS 0
:35711 Q Q.LEFT,
:35712 LA RA[R1],
U 1A76, 0831,1B14,02A8,F888,0010,1A5A :35713 CLR.UBCC,
:35714 ALU?,J/DIVG.062 ; CHECK FOR CARRY OR ZERO
:35715
:35716 :0111-----;
:35717 ALU D+LC+1, ; ADD WITH CARRY
:35718 D ACU.LEFT,SI/DIV,
:35719 Q Q.LEFT,
:35720 LA RA[R1],
U 1A77, 0831,0310,02A8,F888,0010,199C :35721 CLR.UBCC,
:35722 C31?,J/DIVG.063
:35723
:35724 :1110-----;
:35725 ALU D+LC,
:35726 D ACU.LEFT,SI/DIVD, ; ALU N-BIT IS 1
:35727 Q Q.LEFT,
:35728 LA RA[R1],
U 1A7E, 0831,1B14,0028,F888,0010,1A5A :35729 CLR.UBCC,
:35730 ALU?,J/DIVG.062 ; CHECK FOR CARRY OR ZERO
:35731
:35732 :1111-----;
:35733 ALU D+LC+1,
:35734 D ACU.LEFT,SI/DIVD,
:35735 Q Q.LEFT,
:35736 LA RA[R1],
U 1A7F, 0831,0310,0028,F888,0010,199C :35737 CLR.UBCC,
:35738 C31?,J/DIVG.063
:35739
  
```

```

:35740 :-----:
:35741 =0110 :BRANCH ON ALU N&C BITS
:35742 :0110-----: NO CARRY
:35743 DIVG.084:ALU D+LC,
:35744 D_ALU.LEFT,SI/DIV,
:35745 Q_Q.LEFT,
:35746 LA_R[R1],
:35747 CLR_UBCC,
U 1A86, 0831,0016,02A8,F888,0010,0006 :35748 RETURN[6]
:35749
:35750 :0111-----:
:35751 ALU D+LC+1,
:35752 D_ALU.LEFT,SI/DIV,
:35753 Q_Q.LEFT,
:35754 LA_R[R1],
U 1A87, 0831,0012,02A8,F888,0010,0006 :35755 CLR_UBCC,
:35756 RETURN[6]
:35757
:35758 :1110-----:
:35759 ALU D+LC,
:35760 D_ALU.LEFT,SI/DIVD,
:35761 Q_Q.LEFT,
:35762 LA_R[R1],
U 1A8E, 0831,0016,0028,F888,0010,0006 :35763 CLR_UBCC,
:35764 RETURN[6]
:35765
:35766 :1111-----:
:35767 ALU D+LC+1,
:35768 D_ALU.LEFT,SI/DIVD,
:35769 Q_Q.LEFT,
:35770 LA_R[R1],
U 1A8F, 0831,0012,0028,F888,0010,0006 :35771 CLR_UBCC,
:35772 RETURN[6]
:35773 =:END
:35774 :-----:
:35775 DIVG.16:LC_RC[T1]&R1_Q, : RESTORE R1,LATCH EXPONENT
:35776 SC_K[.8], : SC GET 32.-#OF BITS IN <LS>
:35777 Q_0
:35778
:35779 :-----:
:35780 D_DAL.SC, : RIGHT ADJUST <LS> FRACTION
:35781 ALU_K[.80],Q_ALU.LEFT3, : Q GETS BIAS OF .400
:35782 LAB_R[R15] : LATCH FRACTION <MS>
:35783
:35784 :-----:
:35785 ALU D+Q,Q_ALU,D_Q,CLK_UBCC, : ROUND FRACTION <LS>
:35786 SC_RC[FFF5],
U 1B49, 0C1D,1614,E1C0,F800,0094,7A97 :35787 STATE7-4? : NEED TO ADJUST EXPONENT ?
:35788
  
```



```

:35789 :-----:
:35790 =0111 :BRANCH ON STATE 7
:35791 :0111-----:
:35792 DIVG.170:
:35793 ALU D+LC,R[R15]_ALU, : EXPONENT IS RIGHT
U 1A97, 0011,0014,0180,FAF8,0000,1B4A :35794 J/DIVG.17
:35795
:35796 :1111-----:
:35797 ALU D+LC+1,R[R15]_ALU, : INCREMENT EXPONENT
U 1A9F, 0011,0010,0180,FAF8,0000,1B4A :35798 J/DIVG.17
:35799
:35800 :-----:
U 1B4A, 0800,003C,0180,F800,0000,1889 :35801 DIVG.17:D_LA, J/PACKG : D GETS FRACTION <MS>
:35802 :-----:

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```

:35803 .TOC " G & H floating point : MULTIPLY GRAND FLOATING"
:35804
:35805 : USED BY POLYG AND EMODG AS WELL AS MULG.
:35806 : INPUTS:
:35807 : RCO = OP1 LONG EXP
:35808 : Q = OP1 LONG FRAC
:35809 : RC2 = OP2 LONG EXP
:35810 : D = OP2 LONG FRAC
:35811
:35812 : TEMPORARIES:
:35813 :
:35814 : T0 =
:35815 : T9 = SCRATCH REGISTER
:35816 : R15 = SCRATCH REGISTER
:35817
:35818 -----
:35818 MULG.00: TRAP.ACCE[1], : RESET THE FPA
:35819 RC[6]_D, : SAVE OP2 LONG FRAC IN RC6
:35820 D_Q, : DUPLICATE OP1 LONG FRAC
:35821 SC_KC.10] : 16. FOR SWAPPING
:35822
:35823 =00
:35824 MULG.02: SGN/CLR.SD+SS, : ENTER HERE FROM POLYG
:35825 RC[3]_D, : CLEAR OUT SS
:35826 D.DAL.SC, : SAVE OP1 LONG FRAC IN RC3
:35827 SC_KC.FFF9], : WORD SWAP OP1 LONG FRAC
:35828 CALL,J/UNPACKG : SETUP SHIFT AMOUNT OF -7
:35829
:35830 :01-----
:35831 D_0,Q_0, : RETURN1, SRC = 0
:35832 RC[1]_0, : PRODUCT IS 0
:35833 SC_ALU, FE_KC.10], : CLEAR PROD LONG EXP
:35834 NZ_ALU.V&C_0, :
:35835 RETURN10 : CLOCK CONDITION CODES
:35836
:35837 :10-----
:35838 D_0,Q_0, : RETURN2, DST = 0
:35839 RC[1]_0, : PRODUCT IS 0
:35840 SC_ALU, FE_KC.10], :
:35841 NZ_ALU.V&C_0, : CLOCK CONDITION CODES
:35842 RETURN10
:35843
:35844 :11-----
:35845 : RETURN3, SRC NE 0, DST NE 0
:35846 :
:35847 : T0 = M'PLIER FRAC <MS>
:35848 : T2 = Q = M'PLIER FRAC <LS>
:35849 : M'CAND<MS> = T1
:35850 : D = M'CAND FRAC <LS>
:35851 : RC4 = EXP2+EXP1
:35852
:35852 RC[2]_D, : SAVE M'CAND FRAC <LS> IN RC2
:35853 D.D.RIGHT, SI/ZERO, : DIVIDE IT BY 2
:35854 SC_FE, : SC GETS NABS(EXP2+EXP1)
:35855 : LOW BITS ONLY
:35856 SD_SS : SD GETS XOR OF SIGNS
:35857 =:END : NOT EMODG
    
```

U 184C, 0C01,00BC,6480,F9B0,0084,78C8

U 18C8, 0D01,003D,BD87,F998,0084,7AF2

U 18C9, 0F03,003E,65F8,F988,01D6,6010

U 18CA, 0F03,003E,65F8,F988,01D6,6010

U 18CB, 0601,003C,0184,F990,0081,1B4D

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:35858 :-----:
:35859 R[R15]_D, CLK.UBCC, : STORE M'CAND/2 IN R15
:35860 D_Q, Q_0 : D GETS M'PLIER FRAC <LS>
U 1B4D, 0C01,003C,01F8,FAF8,0010,19DC :35861 J7MULG.03
:35862
:35863 =0* :0*-----: CALL SITE FOR MULTIPLY ROUTINE
:35864 MULG.03:LC_RC[T2], : LATCH M'CAND FRAC <LS>
:35865 SC_K[F], : LOAD LOOP COUNT FOR 16 PASSES
:35866 CALL, Z?, : CALL WHILE BRANCHING ON M'CAND
U 19DC, 0000,013D,6180,F910,0084,70E8 :35867 J/MULDMPY : USE MULTIPLY DOUBLE ROUTINE
:35868
:35869 :RETURN WITH:
:35870 <Q,D> = NEWLY FORMED PRODUCT
:35871 : NOTICE THAT WE NEED ONLY HIGH BIT OF D (=LOW BIT OF MIDDLE PRODUCT)
:35872
:35873 :1*-----: RETURN2
:35874 ALU_D, N_AMX.Z_TST, : STORE LOW BIT IN PSL<N>
:35875 D_Q, : D GETS PROD <LS>
:35876 Q_ID[T0], : Q GETS M'PLIER <MS>
U 19DE, 0C01,003C,C1F0,2D10,0030,19E8 :35877 LC_RC[T2] : LATCH M'CAND <LS>
:35878 =:END
:35879 =0* :0*-----: CALL SITE FOR MULTIPLY ROUTINE
:35880 D_Q, : D GETS M'PLIER <MS>
:35881 Q_D, : Q GETS <MS> OF LOW PRODUCT
:35882 SC_K[F], : SET LOOP COUNT TO 16 PASSES
U 19E8, 0C00,013D,61E0,F800,0084,70E8 :35883 CALL, Z?, J/MULDMPY : CALL MULTIPLY LOOP
:35884 : STILL BRANCHING ON M'CAND<LS>
:35885 :RETURN WITH:
:35886 <Q,D> = NEWLY FORMED PRODUCT (A MIDDLE PRODUCT)
:35887
:35888 :1*-----: RETURN2
U 19EA, 0C00,003C,01E0,F800,0000,1B50 :35889 D_Q, Q_D : PREPARE FOR LEFT SHIFT
:35890 =:END
:35891 :-----:
:35892 ALU_Q, RC[T6] ALU.LEFT, : SHIFT DATA TO MAKE
:35893 D_D.LEFT, SI/DIVD, : <D,RC6> = 64 <LS> BITS OF
U 1B50, 0521,203C,C470,2DB0,0000,1B51 :35894 Q_ID[T1] :
:35895 : M'CAND<LS>xM'PLIER
:35896
:35897 R[R15]_Q, : STORE M'CAND <MS> IN R15
U 1B51, 0001,203C,CD80,3EF8,0000,1B52 :35898 ID[T3]_D : SAVE PROD <LS> FOR LATER ADD IN T3
:35899
:35900 :-----:
:35901 RC[T0] Q.LEFT, : RCO GETS M'CAND <MS> *2
:35902 SI/ZERO, :
U 1B52, 0021,203C,C9F0,2D80,0000,1A1C :35903 Q_ID[T2] : GET M'PLIER <LS>
:35904 :-----:
  
```

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:35905 =0* :0*-----: CALL SITE FOR MULTIPLY ROUTINE
:35906 D_Q, Q_0, : D GETS M'PLIER <LS>
:35907 LC_RC[TO], : LATCH 2*M'CAND IN LC
:35908 SC_K[F], : LOOP COUNT GETS 16.
U 1A1C, 0C00,003D,61F8,F900,0084,70E8 :35909 CALL, J/MULDMPY : CALL MULTIPLY LOOP
:35910
:35911 :RETURN WITH:
:35912 : <Q,D> = NEWLY FORMED PRODUCT (ANOTHER MIDDLE PRODUCT)
:35913
:35914 :1*-----: RETURN2
:35915 D_D+LC, : ADD [DST<LS>XSRC<MS>]<LS> TO
U 1A1E, 0811,0014,0180,F800,0010,1B53 :35916 CLK_UBCC : [DST<MS>XSRC<LS>]<LS>
:35917 : AND CLOCK CARRY
:35918 =:END
:35919
:35920 ALU_D, N_AMX.Z_TST, : SAVE CURRENT LOW BIT IN PSL<N>
:35921 D_Q, : D GETS M'PLIER <MS>
U 1B53, 0C01,033C,CDF0,2C00,0030,1A5C :35922 Q_ID[T3], : Q GETS PROD<LS>
:35923 C31? : TEST CARRY FROM PREVIOUS ADD
:35924
:35925
:35926 =C* :BRANCH ON ALU C31
:35927 :0*-----: NO CARRY
:35928 ALU_D+Q, RC[T6]_ALU, : ADD AND SAVE RESULT IN RC6
:35929 CLK_UBCC, LONG, : WE MIGHT HAVE A CARRY HERE
U 1A5C, 001D,0014,C1F0,2DB0,0010,1A68 :35930 Q_ID[T0], : Q GETS M'PLIER <MS>
:35931 J7MULG.04
:35932
:35933 :1*-----: CARRY
:35934 ALU_D+Q+1, RC[T6]_ALU, : ADD AND SAVE RESULT IN RC6
:35935 CLK_UBCC, LONG, : WE MIGHT HAVE A CARRY HERE
U 1A5E, 001D,0010,C1F0,2DB0,0010,1A68 :35936 Q_ID[T0], : Q GETS M'PLIER <MS>
:35937 J7MULG.04
:35938 =:END
:35939 =0* :0*-----: CALL SITE FOR MULTIPLY ROUTINE
:35940 MULG.04:LC_RC[TO], : LATCH UP 2*M'CAND<MS>
:35941 D_Q, : D GETS M'PLIER <MS>
:35942 Q_0,
:35943 SC_K[F], : LOOP COUNT IS SET TO 16 PASSES
U 1A68, 0C00,003D,61F8,F900,0084,70E8 :35944 CALL, J/MULDMPY
:35945
:35946 :1*-----: RETURN2
:35947 SC_K[FFF5], : GET SC READY FOR PACKG-ROUTINE
:35948 Q_D+LC, CLK_UBCC, : ADD RESULTS TOGETHER
U 1A6A, 0C11,0314,E1C0,F800,0094,7A69 :35949 : CLOCK CARRY
:35950 D_Q,C31? : WAS THERE AN OLD CARRY ?
:35951 =:END
  
```

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:35952 -----:
:35953 =0* :BRANCH ON ALU C31
:35954 :0* -----: NO CARRY
U 1A69, 0000,033C,0180,F920,0000,1A70 :35955 LC RC[4], : LATCH PRODUCT EXPONENT
:35956 C31?,J/MULG.05 : TEST CARRY
:35957 -----:
:35958 :-----:
:35959 LC RC[4], : LATCH PRODUCT EXPONENT
U 1A6B, 0819,0314,0580,F920,0000,1A70 :35960 D D+K[.1], : ADD IN PREVIOUS CARRY
:35961 C31?,J/MULG.05 : TEST CARRY
:35962 =;END
:35963 -----:
:35964 =0* :BRANCH ON ALU C31
:35965 :0* -----: NO CARRY
:35966 MULG.05:ALU Q, Q ALU.LEFT, : SHIFT <D,Q,PSL<N>> LEFT ONCE
:35967 D D.LEFT, SJ/DIVD,
:35968 FE SHF.VAL, : NEED IT TO CLR STATED IF FRACT<.5
U 1A70, 0521,203C,0040,F800,010C,7B54 :35969 J/MULG.51
:35970 -----:
:35971 :1* -----: CARRY
U 1A72, 0819,0014,0580,F800,0000,1A70 :35972 D D+K[.1], J/MULG.05 : ADD IN CARRY TO PROD<MS>
:35973 -----:
:35974 MULG.51:-----:
:35975 ID[9] D, : NEED D TEMPORARILY
U 1B54, 0010,0038,E580,3EF8,0000,1B56 :35976 R[R15]_LC : R15 GETS EXPONENT
:35977 -----:
:35978 :-----:
U 1B56, 0318,0038,8180,FA78,0000,1B57 :35979 LAB R[R15], : LATCH EXPONENT
:35980 D_K[.3FF] : D GETS .400-1 (=BIAS-1)
:35981 -----:
:35982 :-----:
:35983 R[R15]_LA-D, : GET BIASED EXPONENT
:35984 D Q, Q ID[9], : RESTORE PREVIOUS D AND Q
:35985 STATE STATE.ANDNOT.FE, : MAYBE CLEAR STATED
U 1B57, 0C1C,3700,E5F0,2EF8,1400,586A :35986 STATE0? : SEPARATE MULG FROM EMODG/POLYG
:35987 -----:
:35988 :-----:
:35989 =**10 :BRANCH ON LOW BIT OF STATE
:35990 :**10 -----: MULG
U 186A, 0C00,003C,7DE0,F800,0104,7B58 :35991 D Q,Q D, : GET FRACTION IN ORDER
:35992 FE_K[.18],J/MULG.07
:35993 -----:
:35994 :-----:
U 186B, 0C00,173E,01E0,FA78,0000,0012 :35995 LAB R[R15], : POLYG/EMODG
:35996 D_Q,Q_D, STATE0?, RETURN12 : LATCH UP EXPONENT
:35997 -----:
:35998 MULG.07:-----:
U 1B58, 0000,0D3C,8180,FA78,0000,1886 :35999 LAB R[R15], : LATCH EXPONENT
:36000 K[.3FF], D31? : GET READY TO ROUND, NORMALIZED?
:36001 -----:
  
```

	:36002	:	-----	:	
	:36003	=110	:	:BRANCH ON D31 (NORMALIZED?)	:
	:36004		:	:110	:
	:36005		:	:D D.LEFT,Q_Q.LEFT,	: NOT NORMALIZED
	:36006		:	:SI/DIVD,	: NORMALIZE
U 1886, 0518,0000,0428,FAF8,0000,1B58	:36007		:	:R[R15]_LA-K[.1],	: DECREMENT EXPONENT
	:36008		:	:J/MULG.07	:
	:36009		:		:
	:36010		:	-----	:
	:36011		:	:Q_Q+K[.3FF]+1,	: ROUND FRAC <LS>
U 1887, 0019,2010,81C0,F800,0010,1889	:36012		:	:CK.LBCC,	: CLOCK CARRY
	:36013		:	:J/PACKG	: PACK UP RESULT
	:36014		:	-----	:

```

:36015 .TOC '' G & H floating point : GRAND FLOATING POLY''
:36016
:36017 : GRAND FLOATING POINT POLYNOMIAL EVALUATION.
:36018 : INPUTS:
:36019 : RCO = ARG LONG EXP
:36020 : Q = ARG LONG FRAC
:36021 : D = DEGREE
:36022
:36023 : OUTPUTS:
:36024 : R0 = RESULT LONG EXP
:36025 : R1 = RESULT LONG FRAC
:36026 : R2 = 0
:36027 : R3 = TABLE ADDRESS + DEG*8 + 8
:36028 : R4 = 0
:36029 : R5 = 0
:36030
:36031 : TEMPORARIES:
:36032 : ID[T0] = DEGREE
:36033 : ID[T1] =
:36034 : ID[T2] =
:36035 : ID[T3] =
:36036 : ID[T4] =
:36037
U 14C2, 0000,11BC,0080,F800,0000,1AA7 :36038 :-----: TRAP.AC[C1],FPD? : RESET THE FPA
:36039
:36040 =0111
:36041 POLYG.FPD:
:36042 :0111-----: FPD IS SET
:36043 : D,R[R2],Q,0, : SETUP TO GET PC DELTA
:36044 : SC,K[.FFF8], : GET READY TO SHIFT IT
:36045 : J/POLYG.FPD.1
:36046
:36047 POLYG: :1111-----: FPD NOT SET
:36048 : D,D.OXT[WORD], : GET DEGREE
:36049 : STATE,K[.1], : SET POLYG FLAG IN STATE
:36050 : J/POLYG.0
:36051
:36052 POLYG.FPD.1:
:36053 :-----:
U 1B59, 0D00,003C,0180,F800,0000,1B5A :36054 : D_DAL.SC : PC DELTA NOW IN D<07:00>
:36055
:36056 :-----:
U 1B5A, 0819,0000,0580,F800,0000,1908 :36057 : D_D-K[.1] : ADJUST FOR THE ESCD
:36058
:36059 =00 :00-----:
:36060 : PC&VA_D.OXT[BYTE]+PC, : BYPASS SPECIFIERS
:36061 : CALL, J/SETFPD
:36062
:36063 =10 :10-----:
U 190A, 0014,0038,01C0,F800,0000,0EB8 :36064 : Q_PC, J/BAKUP.PC : MEM MGMT CODE HERE ON READ ERRORS
:36065
:36066 =11 :11-----:
U 190B, 0000,003C,01E0,FA18,0200,1896 :36067 : VA_R[R3], J/POLYG.9 : VA GETS TABLE ADDRESS
    
```

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:36068 :-----:
:36069 POLYG.0: :
:36070 LC RC[T0], : LATCH ARG LONG EXP
:36071 ALU_D.ANDNOT.KC[1F], : CHECK IF DEGREE > 31
:36072 CLK.UBCC : CLOCK ALU Z-BIT
:36073 :
:36074 :-----:
:36075 ID[T0]_D, : SAVE DEGREE IN T0
:36076 D_LC, : D GETS ARG LONG EXP
:36077 INTRPT.STROBE, : STROBE FOR INTERRUPTS
U 1B5C, 0810,0138,C180,3C00,4000,1978 : Z? : TEST FOR RESERVED DEGREE
:36079 :
:36080 :-----:
:36081 =0 : BRANCH ON ALU Z-BIT
:36082 :0 :
:36083 J/RSVOPR : RESERVED OPERAND
:36084 :
:36085 :1 :
:36086 ALU_D.AND.KC[7FF0],CLK.UBCC : SEE IF ARG EXP IS ZERO
:36087 :
:36088 :-----:
:36089 Z? :
:36090 :
:36091 =0 :0 :
:36092 J/POLYG.A1 : EXP NOT ZERO,CARRY ON AS USUAL
:36093 :
:36094 :1 :
:36095 ALU_D,CHK.FLT.OPR : EXP=0,CHECK FOR RES OP
:36096 :
:36097 =01*****:-----:
:36098 POLYG.A1:ID[T2] D, : SAVE ARG LONG EXP IN T2
:36099 RC[T2] Q, : SAVE ARG LONG FRAC IN RC2
:36100 INTERRUPT.REQ?, : TEST FOR INTERRUPTS
U 1824, 0001,2E3D,C980,3D90,0000,047E : CALL,J/ASPC : EVALUATE TABLE ADDRESS
:36102 :
:36103 :-----:
:36104 =11*****: :
:36105 R[R15] D, : RETURN WITH TABLE ADDR IN D
:36106 D[LONG]_CACHE : SAVE TABLE ADDRESS IN R15
:36107 =:END : GET FIRST COEFFICIENT LONG EXP
:36108 :
:36109 ALU_D.AND.KC[7FF0],CLK.UBCC, : CLOCK EXPONENT
:36110 LAB[R15], : LATCH TABLE ADDRESS IN LAB
:36111 VA_VA+4 : VA POINTS TO CO LONG FRAC
:36112 :
:36113 :-----:
:36114 ID[T1]_D, : STORE CO LONG EXP IN T1
U 1B61, 0000,013C,C580,3C00,0000,1918 : Z? : TEST FOR 0
:36115
  
```



```
:36116 :00-----:
:36117 =00
:36118 POLYG.1:
:36119 D[LONG] CACHE, : READ CO LONG FRAC
:36120 LC_RC[T0], : LATCH ARG LONG EXP
U 1918, 0000,003D,0180,4100,0000,0E16
:36121 CALL,J/SETFPD
:36122
:36123 :01-----:
:36124 ALU D,CHK.FLT.OPR, : CHECK FOR -0
U 1919, 0001,003C,0180,F8C0,0800,1918
:36125 J/POLYG.1
:36126
:36127 :10-----:
U 191A, 0014,0038,01C0,F800,0000,0EB8
:36128 =10 Q_PC, J/BAKUP.PC : READ ERROR, BACK UP PC
:36129
:36130 :11-----:
U 191B, 0010,0038,D180,3EA0,0000,1B62
:36131 =11 ID[T4] D, : SAVE CO LONG FRAC IN T4
:36132 R[R4]_LC : STORE ARG LONG EXP IN R4
:36133 =:END
:36134
U 1B62, 0000,003C,0180,FA98,0000,1988
:36135 R[R3]_LA : R3 GETS THE TABLE ADDRESS
:36136
:36137 =0 :0-----:
:36138 ALU 0(A) : CLEAR RUNNING PRODUCT <LS>
:36139 LC_RC[T2]&R1_ALU, : STORE IT IN R1
U 1988, 0003,003D,0180,FB90,0000,13E8
:36140 CALL,J/POLY.PC : LATCH ARG LONG FRAC IN LC
:36141 : GO GET PC-DELTA
:36142
:36143 :1-----:
U 1989, 001D,0030,C5F0,2E90,0000,1B64
:36144 R[R2] D.OR.Q, : R2 STORES PC DELTA, DEGREE
:36145 Q_ID[T1] : Q GETS CO LONG EXP
:36146 =:END
:36147
:36148 R[R5]_LC, : STORE ARG LONG FRAC IN R5
U 1B64, 0C10,0038,C1F0,2EAB,0000,1B65
:36149 D_Q, : Q GETS CO LONG EXP
:36150 Q_ID[T0] : Q GETS DEGREE
:36151
:36152
:36153 ALU D.AND.K[.7FF0], CLK.UBCC, : CLOCK CO EXPONENT
U 1B65, 0019,4034,3980,F800,0010,1B66
:36154 WORD
:36155
:36156
:36157 R[R0]_D, : STORE CO LONG EXP IN R0
U 1B66, 0C01,003C,D1F0,2E80,0000,1B68
:36158 D_Q, : D GETS DEGREE
:36159 Q_ID[T4] : Q GETS CO LONG FRAC
:36160
:36161
:36162 R[R1] Q, : STORE CO LONG FRAC AS SUM LONG FRAC
U 1B68, 0101,203C,0180,FA88,0000,1B69
:36163 D_D.LEFT2, SI/ZERO : D GETS DEGREE * 4
:36164
```

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:36165
:36166 R[R3]&VA_LA+K[.8], ; SET UP TABLE ADDRESS IN R3 AND VA
:36167 D D.LEFT, SI/ZERO, ; D GETS DEGREE * 8
:36168 SGN/CLR.SD+SS, ; CLEAR SS FOR BRANCH
U 1B69, 0518,0D14,0187,FA98,0200,18F4 :36169 D.NE.0? ; DEGREE NE 0 ?
:36170
:36171
:36172 =10* ;BRANCH ON D.NE.0
:36173 ;10* ; DEGREE EQ 0
U 18F4, 0000,013C,0180,F800,0000,1998 :36174 Z?, J/POLYG.4 ; TEST CO = 0
:36175
:36176 ;11*
:36177 ALU R[R4].AND.K[.7FF0], ;
U 18F6, 0018,0034,3980,FA20,0010,1B6A :36178 CLK.LBCC ; CLOCK EXPONENT OF ARGUMENT
:36179
:36180
:36181 LAB_R[R15],Z? ; TEST ARGUMENT FOR 0
:36182
:36183
:36184 =0 ;BRANCH ON ALU Z-BIT
:36185 ;0 ; ARG NE 0
U 19 4, 0800,003C,0180,FA20,0000,1B71 :36186 D_R[R4], J/POLYG.10 ; D GETS ARG LONG EXP
:36187
:36188 ;1
U 199 , 001C,2014,0180,FA98,0200,1B6C :36189 R[R3]_LA+D, VA_ALU ; ARG = 0
:36190 =;END ; ADVANCE TABLE TO LAST COEFF
:36191
:36192 ALU R[R4].CHK.FLT.OPR, ; CHECK FOR RESERVED OPERAND
U 1B6C, 0000,003C,0180,FA20,0800,1B70 :36193 J/POLYG.8 ; BY ADDING 8*DEGREE
:36194
:36195
:36196 =0 ;BRANCH ON ALU Z-BIT
:36197 ;0
:36198 POLYG.4: ; DEGREE EQ 0, CO NE 0
U 1998, 0003,003C,0180,FAA0,0000,19AD :36199 R[R4] 0, ; CLEAR R4
:36200 J/POLYG.35 ; AND EXIT
:36201
:36202 ;1
U 1999, 0003,003C,0180,FA80,0000,1B6D :36203 R[R0]_0 ; CO EQ 0, DEGREE EQ 0
:36204
:36205
:36206 U 1B6D, 0003,003C,0180,FA88,0000,1998 :36206 R[R1]_0, J/POLYG.4 ; CLEAR RESULT
:36207
:36208
:36209 POLYG.8:
U 1B70, 0018,8038,0580,FA90,0000,1896 :36210 R[R2]_K[.1], BYTE ; ARG =0, SET DEGREE TO ONE FOR
:36211 ; SINGLE PASS THRU LOOP
:36212 ;

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:36213
:36214 ;POLYG LOOP BEGINS HERE
:36215 =110 ;BRANCH ON PENDING INTERRUPTS
:36216 -----;
:36217 POLYG.9:
U 1896, 0800,003C,0180,FA20,0000,1B71 :36218 D_R[R4], J/PCLYG.10 ; GET ARG LONG EXP
:36219 -----;
:36220 ;
U 1897, 0014,0038,01C0,F800,0000,1A71 :36221 Q_PC ; BAKUP.PC WANTS PC IN Q
:36222 =;END
:36223 ;0*-----;
U 1A71, 0000,003D,0180,F800,0000,0EB8 :36224 =0* CALL,J/BAKUP.PC ; GO TO BACK UP PC
:36225 -----;
:36226 ;1*-----;
U 1A73, 0000,003C,0180,F800,0000,04FA :36227 J/INT.I ; TAKE PENDING INTERRUPT
:36228 -----;
:36229 ;
U 1B71, 0001,003C,0180,F980,0000,1B72 :36230 POLYG.10:
:36231 RC[T0]_D ; RC0 GETS ARG LONG EXP
:36232 -----;
:36233 ;
U 1B72, 0000,003C,01C0,FA28,0000,1B73 :36234 Q_R[R5] ; Q GETS ARG LONG FRAC
:36235 -----;
:36236 ;
U 1B73, 0800,003C,0180,FA00,0000,1B74 :36237 D_R[R0] ; D GETS PARTIAL POLY. LONG EXP
:36238 -----;
:36239 ;
U 1B74, 0001,003C,0580,FB10,1404,7820 :36240 ALU D, STATE_K[.1], ; SET POLYG FLAG FOR RETURN
:36241 LAB_R1&RCL[2]_ALU ; RC1 GETS PARTIAL POLY. LONG EXP
:36242 -----;
:36243 ;0**00-----;
:36244 =0**00
:36245 D Q, SC K[.10], ; D GETS ARG LONG FRAC
:36246 RC[T6] [A, ; SAVE ARG LONG FRAC IN T6
U 1820, 0C00,003D,6580,F9B0,0084,78C8 :36247 CALL, J/MULG.02 ; CALL MULTIPLY ROUTINE
:36248 -----;
:36249 ;1**00-----; POLYNOMIAL EQ 0
:36250 =1**00 ; RETURN WITH VA POINTING TO COEFF.
:36251 D[LONG] CACHE, ; GET NEXT COEF LONG EXP
:36252 LAB_R[R3], ; LATCH TABLE ADDRESS
U 1830, 0000,003C,0180,4218,0000,1B77 :36253 J/POLYG.12
:36254 -----;
:36255 ;1**10-----;
:36256 =1**10 ; .25 <= PARTIAL POLY FRACTION < .5
:36257 D D.LEFT, SI/DIVD, ; NORMALIZE
:36258 R[R15] LA-K[.1], ; DECREMENT EXPONENT
U 1832, 0518,0000,0400,FAF8,0000,1B76 :36259 J/POLYG.11
:36260 -----;
:36261 ;1**11-----;
:36262 =1**11 ; POLY FRACTION IS NORMALIZED
:36263 ID[T0] D, ; SAVE POLY FRAC <MS> IN T0
:36264 LAB_R[R15],
:36265 D Q, Q D, ; SWAP HALVES TO SAVE <LS> PART
U 1833, 0C00,003C,C1E0,3E78,0000,1B78 :36266 J7POLYG.13
:36267 =;END ;
    
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:36268 POLYG.11:
:36269 -----:
:36270 ID[T0] D, : SAVE POLY FRAC <MS> IN TO
:36271 LAB_R[R15], : LATCH EXPONENT
:36272 ALU_Q,D_ALU.LEFT,Q_D, : SWAP HALVES TO SAVE <LS> PART
:36273 J/POLYG.13
:36274
:36275
:36276 POLYG.12:
:36277 ALU_D.AND.K[.7FF0], : PARTIAL POLY IS 0
:36278 CLK.LBCC, : CLOCK EXP OF NEXT COEFF
:36279 Q_D, : Q GETS COEFF LONG EXP
:36280 VA_VA+4 : VA NOW POINTS TO COEFF LONG FRAC
:36281
:36282
:36283 D[LONG]_CACHE, : READ NEXT COEFF LONG FRAC
:36284 Z? : IS COEFF = 0 ?
:36285
:36286 -----:
:36287 =0 : BRANCH ON ALU Z-BIT
:36288 :0 : NOT 0
:36289 R[R1]_D, : STORE COEFF LONG FRAC
:36290 D_Q,Q_D, : MAIN FLOW EXPECTS THEM THIS WAY
:36291 J7POLYG.12A
:36292
:36293 :1-----:
:36294 ALU_Q.AND.K[.8000],CHK.FLT.OPR, : CHECK FOR RESERVED OP
:36295 Q_0,D_0 : COEFF IS TRUE 0
:36296
:36297 -----:
:36298 R[R0]_K[ZERO], : ZERO PARTIAL PRODUCT
:36299 J/POLYG.12A
:36300 =:END
:36301
:36302 POLYG.12A:
:36303 R[R3]_LA+K[.8],J/POLYG.22 : INC TABLE ADDRESS
  
```

U 1B76, 0821,203C,C1E0,3E78,0000,1B7B

U 1B77, 0019,0034,39E0,F803,0010,1B78

U 1B78, 0000,013C,0180,4000,0000,19A4

U 19A4, 0C01,003C,01E0,FA88,0000,1B7A

U 19A5, 0F19,2034,45F8,F800,0800,1B79

U 1B79, 0018,0038,1980,FA80,0000,1B7A

U 1B7A, 0018,0014,0180,FA98,0000,1B89

```

:36304 POLYG.13:
:36305 -----
:36306 ID[2] D, ;
:36307 ALU Q, D, ALU.LEFT, SI/ZERO, ; SAVE POLY FRAC <LS> IN T2
:36308 LAB R[R15], ; D GETS NORMALIZED POLY FRAC <MS>
:36309 J/POLYG.14 ; LATCH POLYNOMIAL EXPONENT
:36310 -----
:36311
:36312 POLYG.14:
:36313 : RC[0] GETS PACKED EXPONENT
:36314 -----
:36315 ALU LA-K[.1], RC[5] ALU, ; SAVE POLY EXP IN RC5
:36316 CLK.UBCC,D[LONG]_CACHE ; READ NEXT COEFF LONG EXP
:36317 -----
:36318
:36319 RC[1] D, ; SAVE IT IN RC1
:36320 Q_D, VA_VA+4 ; AND IN Q
:36321 -----
:36322
:36323 LAB R[R3], ; LATCH COEFF TABLE ADDRESS
:36324 D[LONG]_CACHE ; READ COEFF LONG FRAC
:36325 -----
:36326
:36327 =00 ; CALL CONSTRAINT BLOCK
:36328 POLYG.14A:STATE.STATE.OR.K[.1], ; SET POLYG FLAG AGAIN FOR ADDG
:36329 RC[6] D, ; SAVE COEFF LONG FRAC IN RC6
:36330 CALL, J/UNPKG ; UNPACK COEF
:36331 -----
:36332
:36333 SD SS, Q ID[2], ; GET POLY FRAC <LS>
:36334 J/POLYG.16 ;
:36335 -----
:36336 ; COEFF NE 0
:36337 : D = COEFF FRAC <LS>
:36338 : RC4 = COEFF EXP
:36339 : RC5 = POLY EXP
:36340 : RC6 = COEFF LONG FRAC
:36341 : R[R15] = COEFF EXP-POLY EXP
:36342 : ID[1] = COEFF FRAC <MS>
:36343 : ALU CC REFLECT R15
:36344 : SC = LOW BITS OF EXP DIFF
:36345 : FE = 0
:36346 -----
:36347 LAB R[R3], ; LATCH TABLE ADDRESS
:36348 J/POLYG.140 ;
:36349 =:END ;
:36350 -----
:36351 POLYG.140:
:36352 R[R3]_LA+K[.8] ; INC TABLE ADDRESS
:36353 -----
:36354
:36355 LAB_R[R15] ; LATCH EXPONENT DIFFERENCE
    
```

U 1B7B, 0821,203C,C980,3E78,0000,1B7C

U 1B7C, 0018,0000,0580,41A8,0010,1B7E

U 1B7E, 0001,003C,01E0,F98B,0000,1B80

U 1B80, 0000,003C,0180,4218,0000,1938

U 1938, 0001,003D,0580,F980,1404,3B93

U 1939, 0000,003C,C9F4,2C00,0000,1B84

U 193A, 0000,003C,0180,FA18,0000,1B81

U 1B81, 0018,0014,0180,FA98,0000,1B82

U 1B82, 0000,003C,0180,FA78,0000,18C3

```

:36356 =00011 :00011-----: CALL SITE FOR ADDG-ROUTINE
:36357 Q_ID[T2], : Q GETS RUNNING POLY FRAC <LS>
:36358 LC_RC[T4], : LATCH POLY EXPONENT
:36359 FE_NABS(SC-FE), : FE GETS NEGATIVE EXP DIFF
:36360 ALD?, : TEST EXPONENT DIFFERENCE
:36361 CALL,J/ADDG.10
U 18C3, 0000,1B3D,C9F0,2D20,0100,F9E3
:36362
:36363 =10011 :10011-----: RETURN FROM ADDG THRU PACKG
:36364 Q_ID[T9],R[R0]_D,J/POLYG.22A : NORMAL FLOW,STORE NEW ANSWER AND CON
:36365
:36366 :10111-----: EXPONENT WAS ZERO,UNDERFLOW
:36367 J/POLYG.17 : GO TEST PSL<FU> SET?
:36368
:36369 :11011-----: BIT 15 WAS SET
:36370 Q_ID[T9],Q31? : OVERFLOW OR UNDERFLOW?
:36371 =:END
:36372
:36373 =011 : : BRANCH ON Q 31
:36374 POLYG.15: :
:36375 D_K[.8],LAB_R[R3],J/POLYD.FAULT : OVERFLOW
:36376 TAKE FAULT
:36377
:36378 J/POLYG.17 : UNDERFLOW
:36379
:36380
:36381 POLYG.16: :
:36382 D_Q,LAB_R[R3], : D GETS RESULT FRAC <MS>
:36383 Q_ID[T0] : Q GETS RESULT FRAC <LS>
:36384
:36385
:36386 R[R3]_LA+K[.8] : INC TABLE ADDRESS
:36387
:36388
:36389 D D.LEFT, Q Q.LEFT, : DOUBLE SHIFT FRACTION PART
:36390 SI/ASHL, K[.3FF] : GET READY TO ROUND
:36391
:36392
:36393 D Q, Q D+K[.3FF]+1, : ROUND LOW FRACTION PART
:36394 C[K.LBCC] : CLOCK CARRY IF ANY
:36395
:36396 :00011-----:
:36397 =00011 SC K[.FFF5], : CONSTANT NEEDED FO PACKG-ROUTINE
:36398 CALL, J/PACKG : PACK IT UP
:36399
:36400
:36401 =10011 :10011-----: OK
:36402 Q_ID[T9],R[R0]_D,J/POLYG.22A : RESTORE LOW FRAC
:36403
:36404 :10111-----: UNDERFLOW
:36405 J/POLYG.17
:36406
:36407 :11011-----:
:36408 Q_ID[T9],Q31?,J/POLYG.15
:36409 =:END
  
```

```

:36410 =0101 :-----:
U 1AB5, 0000,003D,3DF0,2C00,0000,12AE :36411 POLYG.17:Q_ID[PSL],CALL[PSLFU.A] : TEST FU BIT
:36412 :-----:
:36413 =1101 :-----:
U 1ABD, 0F00,003C,01F8,F800,0000,1B89 :36414 Q_0,D_0,J/POLYG.22 : PSL<FU>=0,IGNORE UNDERFLOW
:36415 :-----:
:36416 :-----:
U 1ABF, 0818,0038,F580,FA18,0000,13F1 :36417 LAB_R[R3],D_K[A],J/POLYD.FAULT : TAKE UNDERFLOW FAULT
:36418 :-----:
:36419 :-----:
:36420 POLYG.22:-----:
U 1B89, 0001,003C,0180,FA80,0000,1B8A :36421 R[R0]_D : R0 GETS NEW PARTIAL PROD<MS>
:36422 :-----:
:36423 :-----:
:36424 POLYG.22A:-----:
U 1B8A, 0000,003C,0180,FA10,0000,1B8C :36425 LAB_R[R2] : LATCH UP DEGREE
:36426 :-----:
:36427 POLYG.26:-----:
:36428 VA VA+4, : INCREMENT COEFF ADDR
U 1B8C, 0018,8000,0580,FA93,0010,1B8E :36429 R[R2] LA-K[ 1], BYTE, : DECREMENT DEGREE,
:36430 CLK.UCC : WITHOUT CHANGING PC-DELTA
:36431 :-----:
:36432 :-----:
:36433 R[R1] Q, : STORE RESULT <LS>
:36434 SC.K[1F], : GENERATE UNDERFLOW MASK BIT
U 1B8E, 0001,213C,8D80,FA88,4084,79AC :36435 INTRPT.STROBE, : STROBE INTERRUPTS
:36436 Z? : ARE WE DONE ?
:36437 :-----:
:36438 :-----:
:36439 =0 : BRANCH ON ALU Z-BIT
U 19AC, 0000,0E3C,0180,F800,0000,1896 :36440 :0:-----:
:36441 INTERRUPT.REQ?, J/POLYG.9 : KEEP LOOPING
:36442 :-----:
:36443 :1-----:
:36444 POLYG.35:-----:
U 19AD, 0003,003C,0180,FAA8,2000,1B90 :36445 CLR.FPD, : CLEAR FPD-FLAG IN PSL
:36446 R[R5]_0 : CLEAR R5
:36447 :-----:
:36448 :-----:
U 1B90, 0003,003C,0180,FAA0,0000,1B91 :36449 R[R4]_0 : CLEAR R4
:36450 :-----:
:36451 :-----:
U 1B91, 0003,003C,0180,FA90,0000,1B92 :36452 R[R2]_0 : CLEAR R2
:36453 :-----:
:36454 :-----:
:36455 POLYG.C:-----:
:36456 ALU_R[R0].AND.K[.FFF0],
U 1B92, 0018,4034,6D80,FA00,0050,13C3 :36457 NZ_ALU.V&C_0,WORD, : CLOCK PSL CONDITION CODES
:36458 J/POLY.0 : JOIN COMMON CODE
:36459 :-----:
    
```

```

:36460 .TOC      "      G & H floating point : UNPACK SINGLE G FLOATING"
:36461
:36462 ;ROUTINE TO UNPACK A SINGLE G FLOATING POINT NUMBER.
:36463
:36464 ;INPUTS:
:36465           :      D = OP LONG FRAC
:36466           :      Q = OP LONG EXP
:36467           :      RC[15] = OP1 EXPONENT
:36468
:36469 ;OUTPUTS:
:36470           :      SS = SD = SIGN
:36471           :      ID[1] = OP FRAC <MS>
:36472           :      D = OP FRAC <LS>
:36473           :      RC4 = EXPONENT
:36474           :      R15 = RC5 - RC4
:36475           :      ALU CC REFLECT R15
:36476           :      SC = LOW 10 BITS OF R15
:36477           :      FE = 0
:36478
:36479 ;TEMPORARIES:
:36480           :      SC = VARIOUS SHIFT COUNTS
:36481
:36482 ;RETURNS:
:36483           :      RETURN1 IF RESULT IS 0
:36484           :      RETURN2 IF RESULT IS NOT 0
:36485
:36486 UNPKG:
:36487 -----:
:36488 R[R15]_Q,      :      STORE LONG EXP IN R15
:36489 Q_D,          :      DUPLICATE LONG FRAC FOR SWAP
:36490 SC_K[.10]    :      SHIFTER GETS 16.
:36491
:36492 -----:
:36493 UNPKG.0:
:36494 D_DAL.SC,     :      SWAP WORDS OF LONG FRAC
:36495 Q_R[R15].OR.K[.10], :      SET HIDDEN BIT
:36496 SS_SS.XOR.ALU15&SD_ALU15 :      SD GETS SIGN BIT
:36497
:36498 -----:
:36499 Q_Q.ANDNOT.K[.20] :      CLEAR NEXT BIT
:36500
:36501 -----:
:36502 Q_Q(FRAC),    :      UNPACK IT
:36503 SC_K[.19]    :      SHIFT COUNT OF 25
:36504 -----:
    
```

U 1B93, 0001,203C,65E0,FAF8,0084,7B94

U 1B94, 0D18,0030,65C5,FA78,0000,1B95

U 1B95, 0019,2024,75C0,F800,0000,1B96

U 1B96, 0001,203C,B9C8,F800,0084,7B97


```

:36505      D_DAL.SC,           : RIGHT JUSTIFIED FRAC <MS>
:36506      Q_D,             : Q GETS LONG FRAC (SWAPPED)
U 1B97, 0D00,003C,F5E0,F800,0084,7B98 : SC_K[A]           : SHIFT COUNT OF 10
:36508      -----
:36509      -----
:36510      LC_R[R15],       : LATCH UP OP1 EXPONENT
U 1B98, 0D00,003C,0180,F928,0000,1B99 : D_DAL.SC         : GENERATE FRAC <MS>
:36511
:36512      -----
:36513      -----
:36514      ID[R1]_D,       : SAVE FRAC <MS>
U 1B99, 0C00,003C,C5F8,3C00,0000,1B9A : D_Q, Q_0
:36515
:36516      -----
:36517      -----
:36518      D_DAL.SC,       : GENERATE FRAC <LS>
:36519      ALU_R[R15].AND.K[.7FF0],
U 1B9A, 0D98,0034,39C0,FA78,0010,1B9B : Q_ALU.RIGHT2,    : Q GETS EXPONENT/4
:36520      CLK_UBCC        : CLOCK IT ON ITS WAY THRU
:36521
:36522      -----
:36523      -----
:36524      RC[R4]_Q.RIGHT2, : RC4 GETS EXPONENT
U 1B9B, 0081,213C,01C0,F9A0,0000,1B9C : Q_ALU.RIGHT2,Z? : IS IT 0?
:36525
:36526      -----
:36527      -----
:36528      =0             : BRANCH ON ALU Z-BIT
:36529      :0
:36530      ALU_Q-LC,       : NO
:36531      R[R15]_ALU,    : SUBTRACT EXP1 FROM EXP2
:36532      SC_ALU,        : STORE RESULT IN R15
:36533      FE_K[ZERO],    : SC GETS LOW BITS OF DIFFERENCE
U 1B9C, 0011,2002,1980,FAF8,0196,6002 : CLR_UBCC,        : CLOCK IT FOR USE IN ADDG
:36534      RETURN2
:36535
:36536      -----
:36537      :1-----●----- : YES
:36538      ALU_LA.AND.K[.8000], : PASS JUST SIGN BIT THROUGH ALU
U 1B9D, 0F18,0034,4580,F800,0800,1B9C : CHK_FLT.OPR,    : IS IT -0 ?
:36539      D_0
:36540
:36541      =;END
:36542      -----
:36543      ALU_LC,R[R15]_ALU, : STORE ORIGINAL EXP IN R15
U 1B9C, 0010,003A,0180,FAF8,0000,0001 : RETURN1
:36544
:36545      -----
  
```

```

:36546 .TOC " G & H floating point : FLOATING POINT ARITHMETIC -- EMOGD"
:36547
:36548
:36549 : EMOGD MULR.RG, MULRX.RB, MUL.D.RG, INT.WL, FRACT.WD
:36550
:36551 :INPUTS:
:36552 : RCO = MULTIPLIER LONG EXP
:36553 : Q = MULTIPLIER LONG FRAC
:36554 : D = MULTIPLIER EXTENSION
:36555
:36556 :TEMPORARIES:
:36557 : RC1 = M'CAND LONG EXP
:36558 : RC2 = M'CAND LONG EXP
:36559 : RC4 = M'PLIER EXTENSION IN HIGH 11 BITS
:36560
:36561 =0**1* :0**1*-----;
:36562 EMOGD: CALL,J/SPEC : EVALUATE EXTENSION
:36563 :1**1*-----;
:36564 SC KC.10],
:36565 SUB/SPEC,J/G.FORK
:36566
:36567 =:END
:36568
:36569 14C8: : EMOGD
:36570 TRAP.ACC[1], : RESET THE FPA
:36571 INTRPT.STROBE, : STROBE INTERRUPTS
:36572 D_DAL.SC : PUT EXTENDER IN HIGH WORD
:36573
:36574 :0**1*-----;
:36575 =0**1* RC[4]_D, : GET 16 BIT EXTENDED MULTIPLIER
:36576 D Q, : D GETS M'PLIER LONG FRAC
:36577 CALL, INTERRUPT.REQ?, : EVALUATE MUL'CAND
:36578 J/SPECG
:36579
:36580 :-----;
:36581 :RETURN WITH :
:36582 : D = M'CAND LONG FRAC
:36583 : RC2 = M'CAND LONG EXP
:36584 : Q = M'PLIER LONG FRAC
:36585 :1**1*-----;
:36586 TRAP.ACC[1], : RESET THE FPA
:36587 LC RC[2], : LATCH UP M'CAND LONG EXP
:36588 J/EMODG.1
:36589 =:END :-----;

```

U 1883, 0000,003D,0180,F800,0000,167E

U 1893, 0000,003F,6580,F800,0084,7400

U 14C8, 0D00,008C,0080,F800,4000,18CE

U 18CE, 0C01,0E3D,0180,F9A0,0000,147E

U 18DE, 0000,008C,0080,F910,0000,1809

```
:36590 =0**01 ;0**01-----;
:36591 EMOG.1:
:36592 RC[1] LC, ; STORE M'CAND LONG EXP IN RC1
:36593 STATE RC.3], ; SET STATE-CODE FOR EMOG
U 1809, 0010,0039,0D80,F988,1404,7B4C :36594 CALL,J/MULG.00 ; CALL MULTIPLY ROUTINE
:36595
:36596 : WHEN WE ENTER MULTIPLY-ROUTINE:
:36597 : D = M'CAND LONG FRAC
:36598 : RC1 = RC2 = LC = M'CAND LONG EXP
:36599 : RC4 = EXTENDER IN HIGH 11 BITS
:36600 : RC0 = M'PLIER LONG EXP
:36601 : Q = M'PLIER LONG FRAC
:36602 : STATE = 3
:36603
:36604 :1**01-----; PRODUCT = 0
:36605 : FE = 10
:36606 : D = Q = RC1 = 0
:36607 =1**01
:36608 EMOG.ZERO:
:36609 ID[0] D, ; SAVE ? IN TO
:36610 STATE FE, ; SHARE CODE WITH EMOG
:36611 RC[1] 0, ; RESULT IS 0
U 1819, 0003,003C,C180,3D88,1450,7BA3 :36612 NBZ ALU.VBC 0, ; CLOCK PSL CONDITION CODES
:36613 J/EMOG.0000 ; SHARE CODE WITH EMOG AND EMOG
:36614
:36615 :1**11-----; PRODUCT NE 0
:36616 : < D,Q> = FRACTION
:36617 : AB = R15 = BIASED EXPONENT + 1 OR 2
:36618
:36619 RC[2] Q, ; SAVE PROD FRAC <LS> IN RC2
:36620 STATE_RC.10], ; SET DOUBLE FLAG
U 181B, 0001,203C,65F8,F990,1404,7B9D :36621 Q_0 ; BRANCHING CONVENIENCE
:36622
:36623 -----;
:36624 ALU_K[.80],Q_ALU.LEFT3, ; Q GETS BIAS OF 400
U 189D, 0088,0038,41C0,F910,0000,1BA0 :36625 LC_RC[2] ; LATCH PROD FRAC <LS>
:36626
:36627 -----;
:36628 ALU_LA-Q-1,SC_ALU, ; UNBIAS EXPONENT
U 1BA0, 001C,0008,0180,FAF8,0092,196D :36629 RC[5]_ALU,CLR.UBCC
:36630 -----;
```

```

:36631 =0**** ;0****-----:
:36632 EMODG.2:
:36633 Q LC : RESTORE Q TO PROD FRAC <LS>
:36634 SC K[.1], : IN CASE WE NEED TO SHIFT
:36635 SET.CC(INST) : CLEAR VBIT
:36636 LAB R[R15],D31?, : TEST LEADING BIT OF D
:36637 CALC[EMODG.5]
:36638
:36639 ;1****-----:
:36640 ;return with:
:36641 RC1 = FRACTION <MS>
:36642 RC2 = FRACTION <LS>
:36643 SC = EXPONENT MODULO 32.
:36644 R15 = EXPONENT
:36645 D = INTEGER
:36646 PSL<V> SIGNALS OVERFLOW
:36647
:36648 ALU R[R15].ANDNOT.K[.3FF], : ISOLATE UPPER BITS
:36649 CLK.UBCC : SEE IF THEY ARE ZERO
:36650
:36651 -----:
:36652 ALU?
:36653 =0011 :0011-----: UPPER BITS NOT ZERO
:36654 SET.V : SET V-BIT
:36655
:36656 :0111-----:
:36657 ALU R[R15],CLK.UBCC, : CLOCK EXPONENT
:36658 SC.SC.ANDNOT.K[.FFE0],J/EMODG.2A: CLEAR OUT IRRELEVANT BITS
:36659
:36660 :1011-----:
:36661 ALU R[R15],CLK.UBCC, : CLOCK EXPONENT
:36662 SC.SC.ANDNOT.K[.FFE0] : CLEAR OUT IRRELEVANT BITS
:36663 =:END
:36664 EMODG.2A:-----:
:36665 ID[T?] D, : STORE INTEGER IN T0
:36666 D RC[T2],Q_0, : D GETS MANTISSA <L>
:36667 FE STATE, : TRICK TO CLEAR STATE
:36668 PSL.V? : TEST FOR INTEGER OVERFLOW
:36669
:36670 =1101 :1101-----: NO OVERFLOW
:36671 Q RC[T1], : GET MANTISSA <MS> IN Q
:36672 CLK.UBCC, : SET CONDITION CODES ON IT
:36673 ID[T2] D, : SAVE FRACTION <LS> IN T2
:36674 D DAL.SC, : FIRST PART OF 64 BIT FRACTION SHIFT
:36675 ACU?, J/EMODG.30 : CHECK FOR POSITIVE EXPONENT
:36676
:36677 -----: OVERFLOW
:36678 STATE STATE.ANDNOT.FE, : CLEAR STATE FOR OVERFLOW
:36679 Q RC[T1], : GET MANTISSA <MS> IN Q
:36680 CLK.UBCC, : SET CONDITION CODES ON IT
:36681 ID[T2] D, : SAVE FRACTION <LS> IN T2
:36682 D DAL.SC, : FIRST PART OF 64 BIT FRACTION SHIFT
:36683 ACU?, J/EMODG.30 : CHECK FOR POSITIVE EXPONENT
:36684 -----:
  
```

U 196D, 0010,CD39,05C0,FA78,00F4,787A

U 197D, 0018,0024,8180,FA78,0010,1BA1

U 1BA1, 0000,1B3C,0180,F800,0000,1AC3

U 1AC3, 0000,003C,0180,F800,0020,1AC7

U 1AC7, 0000,003C,A180,FA78,0094,5BA2

U 1ACB, 0000,003C,A180,FA78,0094,5BA2

U 1BA2, 0810,1A38,C1F3,3D10,1500,1ACD

U 1ACD, 0D10,1B38,C9C0,3D08,0010,1AD7

U 1ACF, 0D10,1B38,C9C0,3D08,1410,5AD7

```

:36685
:36686
:36687 EMOFG.0000:
:36688 SGN/CLR.SD+SS, ; RESULT IS 0
:36689 RC[T1]_D,J/EMODFG.11
:36690
:36691 -----
:36692 =0111 ;BRANCH ON ALU N-BIT
:36693 ;0111-----
:36694 EMOFG.30: ; EXPONENT IS >= 0
:36695 RC[T2]_D, ; SAVE NEW FRACTION <LS> IN RC2
:36696 D Q, Q_ID[T2], ; GET READY TO SHIFT FRAC <MS>
:36697 J7EMODFG.4
:36698
:36699 ;1111----- ; EXP < 0, DON'T SHIFT
:36700 EMOFG.3:
:36701 D Q, ; RESTORE ORIGINAL FRACTION
:36702 Q_RC[T2], ; Q GETS FRACTION <MS>
:36703 SC_FE, ; NEEDED FOR CALL
:36704 K[-3FF]
:36705 =;END
:36706 ;0****-----
:36707 =0****
:36708 ALU LA+K[-3FF],RC[T5]_ALU, ; ADD BIAS-1 TO EXPONENT
:36709 SC SC-FE, ; CLEAR SC
:36710 ALU?, ; BRANCH ON FRAC <MS>
:36711 CALL,J/ADDG.31
:36712
:36713 ;1****-----
:36714 ;RETURN FROM ADDG-ROUTINE.
:36715 STATE K[-8], FE_K[-8],
:36716 Q K[-8].RIGHT, ; USED FOR FLAG TO PROBE-ROUTINE
:36717 INTRPT.STROBE, ;
:36718 STATE4? ; WAS THERE OVERFLOW?
:36719 =;END
:36720
:36721 =***0 ;BRANCH ON STATE<4>
:36722 ;***0----- ; YES
:36723 SET.V, ; SET INTEGER OVERFLOW FLAG
:36724 STATE_STATE+FE, ; STATE GETS 10
:36725 SC Q, ; SC GETS 4
:36726 Q_ID[CES], ; GET CES-REGISTER FOR OVERFLOW
:36727 J7EMODFG.V
:36728
:36729 ;***1----- ; NO
:36730 STATE_STATE+FE, ; STATE GETS 10
:36731 INTRPT.STROBE, ; STROBE FOR INTERRUPTS
:36732 SC Q, ; SC GETS 4
:36733 J/EMODFG.11
    
```

U 1BA3, 0001,003C,0187,F988,0000,181C

U 1AD7, 0C01,003C,C9F0,2D90,0000,1BA4

U 1ADF, 0C10,0038,81C0,F910,0081,198D

U 198D, 0018,1B15,8180,F9A8,0080,BA1B

U 199D, 0058,1638,01C0,F800,5504,79C4

U 19C4, 0001,203C,31D,2C00,14A2,9BA6

U 19C5, 0001,203C,0180,F800,5482,981C

```

:36734 :-----:
:36735 EMODG.4: :
:36736 R[R15] 0, : CLEAR EXPONENT
:36737 D_DAL.SC : KEEP SHIFTING FRACTION
:36738 :-----:
:36739 :
:36740 SC_K[ZERO], :
:36741 LAB_R[R15], : LATCH 0 IN LAB
:36742 Q_D, ALU_D, CLK.UBCC, : CLOCK ALU CC ON FRAC <MS>
:36743 J7EMODG.3
:36744 :
:36745 :00****0-----:
:36746 =00****0
:36747 EMODFG.11:
:36748 ID[T1] D, : SAVE FRACTION <MS>
:36749 D_RC[T1], : GET FRACTION <LS>
:36750 CALL, INTERRUPT.REQ?, :
:36751 J/ASPC : EVALUATE INTEGER ADDRESS
:36752 :
:36753 :01****0-----:
:36754 =01****0
:36755 EMODFG.110:
:36756 ID[T1] D, : SAVE FRACTION <MS>
:36757 D_RC[T1], : GET FRACTION <LS>
:36758 CALL, :
:36759 J/ASPC : EVALUATE INTEGER ADDRESS
:36760 :
:36761 :11****0-----:
:36762 =11****0
:36763 TRAP.ACC[1], : RESET THE FPA
:36764 RC[T2]_D, : SAVE INT.WL ADDRESS IN RC2
:36765 D_Q, : D GETS FRACTION <LS>
:36766 STATE STATE+1, : SET FLAG FOR MEMORY MODE
:36767 INTRPT.STROBE, : STROBE FOR INTERRUPTS
:36768 J/EMODGF.12
:36769 :
:36770 :11****1-----:
:36771 =11****1
:36772 TRAP.ACC[1], : REGISTER OPERAND
:36773 D_Q, : RESET THE FPA
:36774 RC[T2]_RLOG.RIGHT, : D GETS FRACT<LS>
:36775 INTRPT.STROBE, : SAVE REGISTER NUMBER
:36776 J/EMODGF.12 : STROBE FOR INTERRUPTS
:36777 =:END
:36778 :-----:
:36779 EMODFG.V:
:36780 Q_D, D_Q.OR.K[.10], : SET INTEGER OVERFLOW CODE IN CES
:36781 INTRPT.STROBE : STROBE FOR INTERRUPTS
:36782 :
:36783 :-----:
:36784 ID[CES] D, D_Q, : WRITE TRAP CODE IN CES
:36785 J/EMODFG.110 : DON'T TEST FOR INTERRUPTS, TOO LATE
:36786 :-----:
  
```

U 1BA4, 0D03,003C,0180,FAF8,0000,1BA5

U 1BA5, 0001,003C,19E0,FA78,0094,7ADF

U 181C, 0810,0E39,C580,3D08,0000,047E

U 183C, 0810,0039,C580,3D08,0000,047E

U 187C, 0C01,00BC,0080,F990,5400,D888

U 187D, 0C40,00B8,0080,F990,5C00,1888

U 1BA6, 0819,2030,65E0,F800,4000,1BA7

U 1BA7, 0C00,003C,3180,3C00,0000,183C

```

:36787 ;:00****0-----:
:36788 =00****0
:36789 EMODGF.12:
:36790 ID[T2]_D, ; T2 SAVES FRACTION <LS>
:36791 CALL, ;
:36792 J/ASPCG ; NEED TO DOUBLE THE CONTEXT
:36793
:36794 ;:11****0-----:
:36795 =11****0
:36796 TRAP.AC[C1], ; RESET THE FPA
:36797 RC[T4]_D, ; SAVE FRACT ADDRESS
:36798 STATE STATE+K[.2], ; REMEMBER MEMORY MODE
:36799 J/EMODF.14
:36800
:36801 ;:11****0-----:
:36802 TRAP.AC[C1], ; RESET THE FPA
:36803 Q_ID[T0], ; REGISTER MODE,
:36804 STATE?,J/EMODF.16
:36805 =:END
:36806
:36807 -----:
:36808 =*10 ;BRANCH ON D31 (WHETHER PRODUCT IS NORMALIZED)
:36809 ;*10-----:
:36810 EMODG.5: ; NOT NORMALIZED
:36811 Q_Q.LEFT, ; SHIFT FRACTION 1 BIT
:36812 D-DAL.SC, SI/ZERO, ; <MS> FRACTION AS WELL
:36813 ACU LA-K[.1], R[R15]_ALU, ; ADJUST EXPONENT
:36814 SC_ALU,CLK_UBCC,
:36815 J/EMODG.50
:36816
:36817 ;*11-----:
:36818 ALU_R[R15],CLK_UBCC,LONG, ; NORMALIZED
:36819 SC_ALU,J/EMODG.6
:36820 =:END
:36821 -----:
:36822 EMODG.50:
:36823 RC[T2]_Q ; SAVE FRACTION <LS> IN RC2
:36824
:36825 -----:
:36826 EMODG.6:
:36827 FE_SC, ; BACK UP EXPONENT IN FE
:36828 Q_0,
:36829 RC[T1]_0,
:36830 ALU? ; INITIALIZE AND CALL CONVERT ROUTINE
:36831
:36832 ;:0011-----:
:36833 =0011 ALU_R[R15].ANDNOT.K[.1F], ; EXP>0
:36834 CLK_UBCC,J/EMODG.N1 ; MASK OUT LOWER FIVE BITS
:36835
:36836 ;:0111-----:
:36837 Q_D,RC[T1]_D,D_0.RETURN10 ; EXP=0
:36838 ; Q,RC1 GETS FRAC<MS>,INT=0
:36839
:36840 ;:1011-----:
:36840 RC[T1]_D,D_0,Q_0,RETURN10 ; EXP<0
: RC1 GETS FRAC<MS>,INT=0,Q=0
  
```

U 1888, 0000,003D,C980,3C00,0000,157E

U 18E8, 0001,00BC,0880,F9A0,1404,9114

U 18E9, 0000,17BC,C0F0,2C00,0000,12EA

U 187A, 0D18,0000,05A8,FAF8,0092,1BA8

U 187B, 0000,003C,0180,FA78,0092,1BA9

U 1BA8, 0001,203C,0180,F990,0000,1BA9

U 1BA9, 0003,1B3C,01F8,F988,0100,1AE3

U 1AE3, 0018,0024,8D80,FA78,0010,1AEF

U 1AE7, 0F01,003E,01E0,F988,0000,0010

U 1AEB, 0F01,003E,01F8,F988,0000,0010

```

:36841 EMOVG.N1:-----:
:36842 SC_SC-K[.20],FE_SC-K[.20],Q_0, : SUBTRACT 32 FROM EXP
:36843 ? : EXP>=32?
:36844
:36845 =0 :0-----: EXP>=32
:36846 ALU_R[R15].ANDNOT.K[.3F], :
:36847 CLK_UBCC,J/EMOVG.N2 : MASK LOWER SIX BITS
:36848
:36849 :1-----: 1<=NUMBER<2**31
:36850 RC[T1]_D,Q_D,D_DAL.SC,SS?, : D GETS INTEGER,SAVE FRAC<MS> IN RC2,Q
:36851 J/CVTGI.4 :
:36852
:36853 EMOVG.N2:-----:
:36854 Q_RC[T2],Z? : EXP>=64?
:36855
:36856 =0 :0-----: EXP>=64
:36857 ALU_R[R15]-K[.60],CLK_UBCC, : SUBTRACT 96
:36858 J/EMOVG.N3 :
:36859
:36860 :1-----: 2**31<=NUMBER<2**63
:36861 EALLI FE,Q_D,OX[BYTE].OR.PACK.FP, : GENERATE FUNNY PACKED NUMBER
:36862 D_DAL.SC,J/CVTGI.3 : GET INTEGER
:36863
:36864 EMOVG.N3:-----:
:36865 SC_SC-K[.20],RC[T2]_0,D_Q, :
:36866 Q_0,ALU? :
:36867
:36868 =0111 :0111-----: EXP>=96
:36869 D_0,Q_0,RC[T1]_0,SET.V,RETURN10 : SET OVERFLOW BIT
:36870
:36871 :1111-----: 2**63<NUMBER<2**95
:36872 D_DAL.SC,RC[T1]_0,Q_0, : D GETS LOW BITS OF INTEGER
:36873 SET.V,SS? : SAVE MANTISSA,SET OVERFLOW BIT
:36874
:36875 =1110 :1110-----: SS CLEAR
:36876 RETURN10 : WE ARE DONE
:36877
:36878 :1111-----: SS SET
:36879 D_0-D,RETURN10 : COMPLIMENT INTEGER
    
```



```

:36880 .TOC " G & H floating point : G FORMAT MOVE AND TEST INSTRUCTIONS"
:36881
:36882 :INPUT:
:36883 : D = SRC LONG FRAC
:36884 : RCO = SRC LONG EXP
:36885
:36886 -----:
:36887 1485:
:36888 MOVG: TRAP.ACC[1], ; RESET THE FPA
:36889 ALU.RC[T0], Q_ALU, ; GET SRC LONG EXP
:36890 SET.CC(LONG) ;
:36891
:36892 -----:
:36893 ALU.Q.AND.K[.7FF0], ; MOVG/MNEG
:36894 CLK.LBCC,J/MOVG.1 ; CHECK EXPONENT FOR 0
:36895
:36896 -----:
:36897 MOVG.1:
:36898 ALU.D.RC[T1]_ALU, ; STORE LONG FRAC WHERE G-FORK WANTS IT
:36899 D_Q,Z? ; IS SRC 0 ?
:36900
:36901 -----:
:36902 =0 ; BRANCH ON ALU Z-BIT
:36903 ; 0
:36904 -----:
:36905 D.D[INST.DEP]K[.8000], ; CHANGE SIGN IF MNEGG
:36906 NZ.ALU,WORD, ; CLOCK Z & N-BITS, LEAVE C AND V
:36907 WRITE.G.DEST ; WRITE DESTINATION
:36908
:36909 -----:
:36910 RC[T1] D.AND.K[.8000],
:36911 CHK.FLT.OPR,D_0, ; CHECK FOR RESERVED OPERAND
:36912 NZ.ALU, ; CLOCK Z & N-BITS, LEAVE C AND V
:36913 WORD,J/WRITE.G
:36914 =:END
:36915 WRITE.G: WRITE.G.DEST
:36916 -----:
  
```

U 1485, 0010,00B8,00C0,F900,0070,1BAC

U 1BAC, 0019,2034,3980,F800,0010,1BAD

U 1BAD, 0C01,013C,0180,F938,0000,19EC

U 19EC, F819,400F,45F0,F847,0060,1400

U 19ED, 0F19,4034,4580,F988,0860,1BB0

U 1BB0, F000,003F,01F0,F847,0000,1400

```

:36917 : TESTG INSTRUCTION
:36918 :INPUTS: RCO = LONG EXP
:36919
U 14A9, 0000,003C,15C0,F800,1404,7BB1 :36920 14A9: STATE_K[ESP1.CON], : STATE GETS 4 OR 8
:36921 Q_LA : Q GETS SRC EXP
:36922
:36923 -----:
:36924 STATE3-0?, : TEST FOR G OR H-FORMAT
:36925 J/TSTG.0
:36926
U 148D, 0010,0038,01C0,F900,0000,1815 :36927 148D: -----:
:36928 Q_RC[0] : Q GETS SRC EXP
:36929
:36930 -----:
:36931 =01** :BRANCH ON STATE<3>
:36932 :01**-----:
:36933 TSTG.0:
:36934 TRAP.ACCE[1], : RESET THE FPA
:36935 ALU_Q.AND.K[.7FF0], :
:36936 CLK.UBCC, : CLOCK Z-BIT ON EXPONENT
:36937 J/TSTG.01
:36938
:36939 -----:
:36940 TSTH.00: :11**-----:
:36941 TRAP.ACCE[1], : RESET THE FPA
:36942 ALU_Q.ANDNOT.K[.8000], : CLOCK EXPONENT
:36943 CLK.UBCC,WORD
:36944
:36945 -----:
:36946 ALU_Q,NBZ_ALU.V&C_0,WORD,
:36947 Z?,J/TSTG.1
:36948
:36949 -----:
:36950 TSTG.01:
:36951 ALU_Q.AND.K[.FFF0], :
:36952 NBZ_ALU.V&C_0,WORD,Z?
:36953
:36954 -----:
:36955 =0 :BRANCH ON ALU Z-BIT
:36956 :0-----:
:36957 TSTG.1: PC_PC+1, : INCREMENT PC
:36958 CLR.IB.OPC, : CLEAR OP CODE FROM IB
:36959 J/IRD
:36960
:36961 -----:
:36962 ALU_Q, :
:36963 CHK.FLT.OPR, : TEST FOR -0
:36964 PC_PC+1, : INCREMENT PC
:36965 CLR.IB.OPC, : CLEAR OP CODE FROM IB
:36966 J/IRD
:36967 =;END :-----:
    
```

```

:36968 .TOC " G & H floating point : FORMAT CONVERSION -- CVTFG,CVTDH,CVTFH"
:36969 : FOR CVTFG AND CVTFH :D = SRC OPERAND, A F FLOATING POINT NUMBER
:36970 : FOR CVTDH: RC[2]= LONG EXP, D = LONG FRAC
:36971 : OPCODES ARE: 99FD FOR CVTFG, 98FD FOR CVTFH, 32FD FOR CVTDH
:36972
:36973 144C: -----
:36974 CVTFG: TRAP.ACC[1], : RESET THE FPA
:36975 ALU D, : D HAS SRC OPERAND
:36976 SC_D(EXP), : SC GETS BIASED EXP
:36977 SS_ALU!5, : SS GETS SIGN
:36978 NZ_ALU.V&C_0,WORD, : CLOCK CONDITION CODES
:36979 RC[3]_ALU, : SAVE IT IN RC3
:36980 D_ALU(FRAC), : D GETS UNPACKED FRACTION
:36981 Q_D, : Q GETS SRC
:36982 IR0? : IS THIS CVTFG OR CVTFH ?
:36983
:36984 -----
:36985 =1101 :BRANCH ON IR<0>
:36986 :1101----- : CVTFH OR CVTDH
:36987 Q_D,D_0,
:36988 IR2-1?,J/CVTFH
:36989
:36990 :111----- : CVTFG
:36991 R[R15]_K[.3FF], : NEW BIAS -1
:36992 DK/RIGHT2, : SHIFT FRACTION RIGHT TWICE
:36993 FE_SC,CLK_UBCC, : DUPLICATE EXPONENT IN FE
:36994 SD_SS, : SD GETS SIGN
:36995 SC.NE.0? : IS EXPONENT = 0 ?
:36996
:36997 -----
:36998 =0** :BRANCH ON SC NE 0
:36999 :0**-----
:37000 ALU_Q.AND.K[.8000],RC[1]_ALU, : CLEAR RC1
:37001 CHK_FLT.OPR, : CHECK FOR -0
:37002 D_0,Q_0, : MAKE IT A CLEAN 0
:37003 NZ_ALU.V&C_0,J/CVTFG.2 : SET PSL Z-BIT
:37004
:37005 :1**-----
:37006 QK/RIGHT2, : SHIFT SRC RIGHT TWICE
:37007 D_PACK.FP : PACK NEW FRACTION <MS>
:37008 :END
:37009 -----
:37010 ALU_Q.ANDNOT.R[R15], : GET RID OF BITS <9:0>
:37011 Q_ALU.RIGHT, : SHIFT 3 LOW ORDER FRACTION BITS
:37012 ST_SC-K[.80] : UNBIAS EXPONENT
:37013
:37014 -----
:37015 ALU_Q.AND.K[.E003], : ISOLATE UPPER 3 BITS OF FRAC <LS>
:37016 RC[1]_ALU
:37017
:37018 -----
:37019 ALU_K[SC],Q_ALU : Q GETS LOW 8 BITS OF EXPONENT
    
```

```

:37020
:37021
U 1BB9, 00AE,A010,01C0,F800,0000,1BBA :-----:
:37022 ALU_Q.SXT[BYTE]+LB+1,Q_ALU.LEFT3 ; GET NEW EXPONENT*4
:37023
:37024 :-----:
:37025 ALU_D.ANDNOT.K[.7FF0],D_ALU, ; CLEAR EXPONENT BITS
U 1BBA, 0819,0024,39A8,F800,0000,1BBC :37026 Q_Q.LEFT ; Q GETS EXPONENT * 16.
:37027
:37028 :-----:
:37029 CVTFG.2: D_D.OP.Q, WRITE.G.DEST ; NOT ZERO, WRITE DESTINATION
U 1BBC, F81D,0033,01F0,F847,0000,1400 :37030
:37031

```

```

:37032 .TOC " G & H floating point : CONVERT G/H-FORMAT TO F/D-FORMAT"
:37033
:37034 : ENTRY POINT FOR CVTHF (OPC = F6), CVTHD ( F7 ), CVTGF ( 33 ).
:37035 : INPUTS:
:37036 : FOR CVTGF:
:37037 : RC2 = SRC LONG EXP
:37038 : D = SRC LONG FRAC
:37039 : FOR CVTHF AND CVTHD:
:37040 : RC2-ID3 = SRC OPERAND
:37041 : STATE = 0
:37042 : SC = .31
:37043
:37044 144B: -----:
:37045 CVTGF: TRAP.ACC[1], : RESET THE FPA
:37046 SC_SC+1,FE_SC+1, : SC AND FE GET .32
:37047 LC_RC[2], : LATCH SRC LONG FRAC
:37048 ALU_K[.80], Q_ALU.LEFT3, : Q GETS .400 (=OLD BIAS)
:37049 IR2=1? : IS SRC = H OR G ?
:37050
:37051 -----:
:37052 =01 : BRANCH ON IR<2>
:37053 :01-----:
:37054 ALU_Q-K[.80], RC[5]_ALU, : RC5 GETS DIFFERENCE BETWEEN BIASSES
:37055 J/CVTGF.0
:37056
:37057 :11-----:
:37058 STATE_K[.80], : SET NORMALIZE BIT
:37059 J/CVTR
:37060 =:END
:37061 =00-----:
:37062 CVTGF.0: :00-----: CALL SITE FOR UNPACK ROUTINE
:37063 R[R15]_LC, : R15 GETS SRC LONG FRAC
:37064 Q_D, : Q GETS SRC LONG FRAC
:37065 SC_K[.10],
:37066 CALL, J/UNPKG.0
:37067
:37068 :01-----: SRC = 0
:37069 D_0, ALU_K[ZERO], : SET DEST = 0
:37070 NZ ALU.V&C_0, : SET Z, CLEAR OTHER CC
:37071 WRITE.DEST : GO AND STORE IT (F-FORMAT)
:37072
:37073 :10-----: SRC NE 0
:37074 :RETURN WITH:
:37075 SS = SD = SIGN BIT
:37076 ID[1] = SRC FRAC <MS>
:37077 D = SRC FRAC <LS>
:37078 RC4 = SRC BIASED EXPONENT
:37079 R15 = DST BIASED EXPONENT
:37080 SC = LOW 10 BITS OF R15
:37081 ALU CC REFLECT R15
:37082
:37083 D_K[.40] : ROUNDING CONSTANT
:37084 =:END
    
```

U 144B, 00B8,09B8,40C0,F910,0180,D839

U 1839, 0019,2000,4180,F9A8,0000,1948

U 183B, 0000,003C,4180,F800,1404,7980

U 1948, 0010,0039,65E0,FAF8,0084,7B94

U 1949, FF18,003B,19F0,F847,0050,0300

U 194A, 0818,0038,3180,F800,0000,1BBD

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:37085
U 18BD, 0000,003C,C5F0,2C00,0000,18C0 :37086 Q_IDET1]
:37087
:37088
:37089 ALU D+Q, : ADD 80 TO ROUND
U 18C0, 081D,0014,0180,F800,0050,18C1 :37090 D ALU, : STORE ROUNDED FRAC <MS> IN D
:37091 NZ_ALU.V&C_0 : SET PSL CONDITION CODES
:37092
:37093
:37094 CVTGF.01: : JOIN HERE FROM CVTHF-FLOWS
:37095 ALU_R[R15],CLK.UBCC, : CLOCK WHOLE EXPONENT
U 18C1, 0000,1A3C,0180,FA78,0010,1835 :37096 PSL.N? : DID ROUNDING PROPAGATE ?
:37097
:37098
:37099 =01** :BRANCH ON PSL N-BIT
:37100 :01**
:37101 CVTGF.1:
:37102 D D.LEFT, SI/ZERO, : LEFT ADJUST FRACTION <MS>
:37103 ALU_R[R15].AND.K[.FF00], : ISOLATE UPPER BITS
:37104 CLK.UBCC, : CLOCK THEM FOR OVERFLOW TEST
U 1835, 0518,1B34,4D80,FA78,0010,1823 :37105 ALU?, J/CVTGF.2 : TEST FOR UNDERFLOW
:37106
:37107 :11**
:37108 R[R15] LA+K[.1],CLK.UBCC, : INCREMENT EXPONENT
:37109 SC SC+T, : INCREMENT LOW 10 BITS AS WELL
U 183D, 0618,0014,0580,FAF8,0090,D835 :37110 D D.RIGHT, : TO COMPENSATE FOR NEXT SHIFT
:37111 J7CVTGF.1
:37112 =:END
:37113
:37114 =0011 :BRANCH ON ALU Z AND N-BITS
:37115 :0011
:37116 CVTGF.2:
:37117 EALU SC, : GET EXPONENT
:37118 D PACK.FP, : PACK RESULT
U 1823, 0808,4138,0180,F800,0050,19FC :37119 NZ_ALU.V&C_0,WORD, : CLOCK CC ON EXPONENT AND SIGN
:37120 Z?,J/CVTGF.3 : TEST FOR OVERFLOW
:37121
:37122 :0111
:37123 D_0,ALU_K[ZERO],NZ_ALU.V&C_0, : ZERO EXPONENT on underflow
U 1827, 0F18,0038,1980,F800,0050,1835 :37124 J7CVTGF.4
:37125
:37126
:37127 D_0,ALU_K[ZERO],NZ_ALU.V&C_0, : NEGATIVE EXPONENT
U 182B, 0F18,0038,1980,F800,0050,1835 :37128 J7CVTGF.4 : UNDERFLOW
:37129 =:END
:37130
:37131 =:0 :BRANCH ON ALU Z-BIT
:37132 :0
:37133 CVTGF.3:RC[T7]_K[.8],J/FLOAT.FAULT : HIGH BITS NOT 0, OVERFLOW
U 19FC, 0018,0038,0180,F988,0000,1284 :37134 : OVERFLOW FAULT
:37135
:37136 :1
U 19FD, F000,003F,01F0,F847,0000,0300 :37136 WRITE.DEST : HIGH BITS ZERO.OK
    
```

```

:37137 =0101
:37138 CVTGF.4:;0101-----; UNDERFLOW
U 1B35, 0000,003D,3DF0,2C00,0000,12AE :37139 Q_ID[PSL],CALL[PSLFU.A] ; TEST FU
:37140
:37141 =1101 ;1101-----; FU NOT SET, IGNORE UNDERFLOW
U 1B3D, F000,003F,01F0,F847,0000,0300 :37142 WRITE.DEST ;
:37143
:37144 ;1111-----; FU SET, TAKE UNDERFLOW
U 1B3F, 0018,0038,F580,F9B8,0000,12B4 :37145 RC[T7]_K[A],J/FLOAT.FAULT ;

```

```

:37146 1447: ; ENTER HERE FOR CVTGH, OPCODE 56FD
:37147 ; EXPECTS: RC2 = SRC LONG EXP
:37148 ; D = SRC LONG FRAC
:37149
:37150 CVTGH: TRAP.ACC[1], ; CALM DOWN THE ACC.
:37151 CLR.SD&SS,
:37152 ALU K[.80],Q ALU.LEFT3, ; Q GETS 400
:37153 RC[5]_ALU.LEFT3 ; RC5 GETS 400
:37154
:37155 :00-----:
:37156 =00 STATE K[.7], ; STATE-REGISTER SET TO 7
:37157 SET.CC(INST), ; CLEAR V
:37158 Q RC[2], ; Q GETS LONG EXP
:37159 CALL,J/UNPKG ; UNPACK THE G-SRC
:37160
:37161 :01-----:
:37162 J/CLRH ; 0 SOURCE, CLEAR EVERYTHING
:37163
:37164 :10-----:
:37165 ; RETURN WITH:
:37166 ; SS = SD = SIGN
:37167 ; ID[1] = SRC FRAC <MS>
:37168 ; D = SRC FRAC <LS>
:37169 ; RC4 = BIASSED EXP
:37170 ; R15 = 400-BIASSED EXP
:37171 ; SC = LOW 10 BITS OF R15
:37172
:37173 Q K[.4000], ; GET NEW BIAS
:37174 LAB_R[R15] ; LATCH 400-EXP
:37175 =:END
:37176
:37177 ALU Q+LB,RC[6]_ALU, ; RC6 GETS DST EXP BIASSED
:37178 Q_ID[1]
:37179
:37180 :-----:
:37181 ; NOW <Q,D> = FRACTION PARTS
:37182 ; RC6 = BIASSED EXP
:37183 ; SD = SIGN
:37184 RC[0]_Q, ; RC0 GETS FRAC <MS>
:37185 ID[0]_D, ; TO GETS FRAC <LS>
:37186 D_0,Q_0
:37187
:37188 :0****-----:
:37189 =0****
:37190 CVTGH.W: ; ENTER HERE FROM CVTDH
:37191 RC[1]_D,ID[1]_D,
:37192 SC ALU, ; ALL GETS 0
:37193 CALL,J/ADDH.310
:37194
:37195 :1****-----:
:37196 U 19D9, F000,003F,01F0,F847,0000,1400 WRITE.G.DEST,J/WRG ; WRITE THE H-FORMAT DEST
:37197 =:END ;-----:
    
```



```

:37198 14CD: ; ENTER HERE FOR CVTHG, WITH OPCODE 76
:37199 CVTHG:
:37200 CLR.SD&SS, ; INITIALIZE SIGN-BITS
:37201 TRAP.ACC[1], ; CALM DOWN THE ACC.
U 14CD, 0000,00BC,4087,F800,1404,7BC4 :37202 STATE_KC.80] ; SET NORMALIZE-BIT
:37203
:37204 -----:
U 1BC4, 0000,003C,7980,F800,0084,7968 :37205 SC_KC.30] ; SET UP POINTER
:37206
:37207 :00-----:
:37208 =00
:37209 CLR.SD&SS, ; INITIALIZE SIGN-BITS
:37210 SC.SC.OR.KC.2],
:37211 FE.SC.OR.KC.2], ; FE GETS .32 AS WELL
U 1968, 0000,003D,0987,F800,0184,363A :37212 CALL,J/UNPACK1H ; UNPACK OPERAND IN RC2-ID3
:37213
:37214 :01-----:
:37215 =01 D 0,ALU_0(A),RC[1]_ALU, ; STORE 0 IN D AND RC1
:37216 NZ.ALU.V&C_0, ; SET PSL Z-BIT
U 1969, 0F03,003C,0180,F988,0050,1BB0 :37217 J/WRITE.G ; WRITE F OR D -FORMAT
:37218
:37219 :11-----:
:37220 =11 ;RETURN WITH:
:37221 ; RC2-ID3 = UNPACKED FRACTION
:37222 ; RC6 = BIASSED EXPONENT
:37223 ; R15 = UNBIASSED EXPONENT
:37224 ; ALU CC REFLECT R15
:37225 ; SC = LOW 10 BITS OF R15
U 196B, 0000,003C,C9F0,2C00,1400,7BC5 :37226 STATE.FE, ; NEED TO CLEAR STATE
:37227 Q_ID[2] ; Q GETS FRAC<AMS>
:37228 =:END
:37229 -----:
:37230 STATE.STATE.ANDNOT.FE, ; CLEAR STATE
:37231 KC.3FF], ; NEED TO ROUND
U 1BC5, 0000,003C,8180,FA78,1400,5BC6 :37232 LAB_R[R15] ; LATCH UNBIASSED EXP
:37233
:37234 -----:
:37235 ALU.LA+K[.3FF]+1, ; BIAS EXPONENT
U 1BC6, 0018,0010,8180,FAF8,0010,1BC7 :37236 R[R15]_ALU,CLK.UBCC ; WITH G-BIAS
:37237
:37238 -----:
U 1BC7, 0000,003C,0180,FA78,0000,1BC8 :37239 LAB_R[R15] ;
    
```

```

:37240
:37241
:37242
U 1B08, 00B8,1B38,9180,F9B8,0000,1B43 :-----:
:37243 RC[R7]_K[.1F00].LEFT3,SI/ZERO, : CREATE MASK FOR HIGH BITS OF EXPONENT
:37244 ALU? : TEST N,Z BITS FOR UNDERFLOW
:37245 =0011
:37246 :0011-----: NOT UNDERFLOW
U 1B43, 0000,003C,0180,F938,0000,1B09 :-----:
:37247 LC_RC[R7],J/CVTHG.0 : PREFETCH MASK FOR NEXT TEST
:37248
:37249 :0111-----: EXP=0,UNDERFLOW
U 1B47, 0000,003C,3DF0,2C00,0000,1B55 :-----:
:37250 Q_ID[PSL],J/UNFLG : PREPARE TO TAKE FAULT
:37251
:37252 :1011-----: EXP<0,UNDERFLOW
U 1B48, 0000,003C,3DF0,2C00,0000,1B55 :-----:
:37253 Q_ID[PSL],J/UNFLG : PREPARE TO TAKE FAULT
:37254 =:END
:37255 =0101
:37256 UNFLG: :0101-----: CALL SITE FOR TEST OF PSL<FU>
U 1B55, 0000,003D,0180,F800,0000,12AE :-----:
:37257 CALL[PSLFU.A] :
:37258 =1101
:37259 :1101-----: RETURN HERE IF FU=0,IGNORE UNDERFL
U 1B5D, 0018,0038,1980,FAF8,0000,1A0D :-----:
:37260 RC[R15]_K[ZERO],J/CVTHG.1 : ZERO OUT EXP,REJOIN CODE
:37261
:37262 :1111-----: RETURN HERE IF FU=1
U 1B5F, 0018,0038,F580,F9B8,0000,12B4 :-----:
:37263 RC[R7]_K[.A],J/FLOAT.FAULT : TAKE FAULT
:37264
:37265 CVTHG.0: :-----:
U 1B09, 0010,0034,0180,FA78,0010,1B0C :-----:
:37266 ALU_R[R15].AND.LC,CLK.UBCC : TEST HIGH BITS OF EXP
:37267
:37268 :-----:
U 1B0C, 0000,013C,8180,F800,0000,1A0C :-----:
:37269 K[.3FF],Z? :
:37270 =0
:37271 :0-----: HIGH BITS NOT 0,OVERFLOW
U 1A0C, 0018,0038,0180,F9B8,0000,12B4 :-----:
:37272 RC[R7]_K[.8],J/FLOAT.FAULT :
:37273
:37274 CVTHG.1: :1-----: HIGH BITS ZERO,OK
U 1A0D, 0019,2010,81C0,F800,0010,19E1 :-----:
:37275 ALU_Q+K[.3FF]+1,Q_ALU. : ROUND LOW FRACTION
:37276 CLK.UBCC : CLOCK CARRY
:37277
:37278 =0**** :0****-----:
U 19E1, 0810,0039,E180,F910,0084,7889 :-----:
:37279 SC_K[.FFF5], :
:37280 D_RC[R2], : GET FRAC<MS>
:37281 CALL,J/PACKG : CALL PACKG-ROUTINE
:37282
:37283 :1****-----:
U 19F1, F000,003F,01F0,F847,0000,1400 :-----:
:37284 : RETURN WITH <D,RC1> = RESULT
:37285 WRITE.G.DEST
:37286
    
```

```

:37287 =00
:37288 CVTH:
:37289 TRAP.ACC[1], : CALM DOWN THE ACC.
:37290 SC.SC.OR.K[.2],
:37291 FE.SC.OR.K[.2], : FE GETS .32 AS WELL
U 1980, 0000,00BD,0880,F800,0184,363A :37292 CACL,J/UNPACK1H : UNPACK OPERAND IN RC2-ID3
:37293
:37294 -----:
:37295 =01 D 0,ALU_0(A),RC[1]_ALU, : STORE 0 IN D AND RC1
:37296 NZ.ALU.V&C_0,Q_0, : SET PSL Z-BIT
U 1981, 0F03,003C,01F8,F988,0050,1A2C :37297 J/CVTHD.2C : WRITE F OR D -FORMAT
:37298
:37299 -----:
:37300 =11 :RETURN WITH:
:37301 RC2-ID3 = UNPACKED FRACTION
:37302 RC6 = BIASSED EXPONENT
:37303 R15 = UNBIASSED EXPONENT
:37304 ALU CC REFLECT R15
:37305 SC = LOW 10 BITS OF R15
:37306 [ RC[2], : D GETS FRAC0
:37307 Q ID[2], : Q GETS FRAC1
U 1983, 0810,1B38,C9F0,2D10,0000,1B2D :37308 IR0? : TEST FOR CVTHF OR CVTHD
:37309 =:END
:37310 -----:
:37311 =1101 :BRANCH ON IR<0>
:37312 :1101-----:
:37313 DK/RIGHT,SI/ZERO, : UNNORMALIZE FRAC<MS>
:37314 Q K[.40],LAB_R[R15], : LATCH UNBIASSED EXPONENT
U 1B2D, 0618,0038,31C0,FA78,0000,1BCD :37315 J7CVTHF.2
:37316
:37317 :1111-----:
:37318 FE_K[.18],LAB_R[R15], : TOO BAD
U 1B2F, 0000,003C,7D80,FA78,0104,7BD0 :37319 J/CVTHD.2
:37320 =:END
:37321 -----:
:37322 CVTHF.2:
:37323 K[.80], : GET SLOW CONSTANT
:37324 ALU_D+Q,D,ALU, : ROUND FRAC0
U 1BCD, 081D,0014,4180,F800,0050,1BCE :37325 NZ.ALU.V&C_0 : CLOCK PSL N-BIT
:37326
:37327 -----:
:37328 ALU_LA+K[.80],R[R15]_ALU,
:37329 SC,ALU, : SC AND R15 GET BIASSED EXP
:37330 CLR,UBCC, : CLOCK CC ON IT
U 1BCE, 0018,0014,4180,FAF8,0092,1BC1 :37331 J/CVTGF.01 : JOIN CVTGF-FLOWS
:37332
:37333
    
```

```
:37334 CVTHD.2:
:37335 SC_ALU,R[R15]_LA+K[.80], : ADD IN BIAS
:37336 N&Z_ALU.V&C_0 : CLEAR V&C
:37337 -----
:37338 -----
:37339 Q_ALU,ALU_Q+K[.80],CLK.UBCC, : ADD ROUND BIT TO LOW FRAC
:37340 J/KJC.0 :
:37341 -----
:37342 =0* :0*-----
:37343 KJC.1: D_DAL.SC,SC_FE, : D GETS FRAC<L>,SC GETS EXP
:37344 EALU_K[.1],CLK.UBCC,J/KJC.2 : CLEAR EALUCC'S
:37345 -----
:37346 :1*-----
:37347 D_D+K[.1],SC_FE,FE_SC,CLK.UBCC : INC FRAC<H>,SC GETS EXP,FE GETS 24
:37348 =:END :
:37349 -----
:37350 ALU_0+K[.1],CLK.UBCC, : CLR C31,MUST WE INC EXP?
:37351 LAB_R[R15],C31? :
:37352 =0* :0*-----
:37353 KJC.0: SC_FE,FE_SC,RC[1]_PACK.FP, : NO PACK RESULT <H>
:37354 C3T?,J/KJC.1 : SC GETS 24,FE GETS EXP,PACK RESULT
:37355 : NEED TO INC FRAC <H> ?
:37356 -----
:37357 :1*-----
:37358 SC_SC+1,R[R15]_LA+K[.1],J/KJC.0 : YES INC EXP BY 1
:37359 =:END :
:37360 KJC.2: -----
:37361 SC_K[.10].ALU,FE_SC,Q_D : SC GETS 16 FE GETS EXP
:37362 -----
:37363 -----
:37364 D_DAL.SC,Q_RC[1] : SWAP WORD,Q GETS RESULT<H>
:37365 -----
:37366 -----
:37367 ALU_R[R15].ANDNOT.K[.FF], : TEST HIGH BITS OF EXP
:37368 CLK.UBCC :
:37369 -----
:37370 -----
:37371 RC[1]_D,Q_D,D_Q : RC1,Q HAVE RESULT<L> D HAS RESULT<H>
:37372 -----
:37373 -----
:37374 ALU_R[R15],CLK.UBCC,Z? : TEST HIGH BITS OF EXP
:37375 -----
:37376 =0 :0-----
:37377 ALU?,J/CVTHD.4 : HIGH BITS NOT ZERO
:37378 : FAULT FIND OUT WHICH ONE
:37379 -----
:37379 :1-----
:37380 Z? : HIGH BITS ZERO
:37381 : TEST REST OF EXP
:37382 =0 :0-----
:37382 CVTHD.2C: : FF>EXP>0
:37383 ALU_D.ANDNOT.K[.1F],WORD, :
:37384 N&Z_ALU, : SET CONDITION CODES
:37385 WRITE.DEST,J/WRD : WRITE THE D-DEST
:37386 -----
:37387 :1-----
:37388 Q_ID[PSL],J/UNFLHD : EXP=0
: UNDER FLOW
```

```

:37389 =0011
:37390 CVTHD.4: :0011-----: OVERFLOW
U 1B63, 0018,0038,0180,F988,0020,12B4 :37391 SET.V,RC[7]_K[.8],J/FLOAT.FAULT: TAKE FAULT
:37392
:37393 :0111-----: EXP=0,UNDERFLOW
U 1B67, 0000,003C,3DF0,2C00,0000,1B75 :37394 Q_ID[PSL],J/UNFLHD : ZERO OUT EXP,PREPARE TO TEST FU
:37395
:37396 :1011-----: EXP<0,UNDERFLOW
U 1B6B, 0000,003C,3DF0,2C00,0000,1B75 :37397 Q_ID[FSL],J/UNFLHD : ZERO OUT EXP,PREPARE TO TEST FU
:37398 =:END
:37399 =0101
U 1B75, 0000,003D,0180,F800,0000,12AE :37400 UNFLHD: :0101-----: CALL SITE FOR PSL<FU> TEST
:37401 CALL[PSLFU.A]
:37402 =1101
:37403 :1101-----: RETURN HERE IF FU=0,IGNORE UNDERFLOW
U 1B7D, 0F18,0038,19F8,F988,0094,7A2C :37404 SC_K[ZERO],D_0,RC[1]_K[ZERO], : ZERO OUT ANSWER
:37405 Q_0,CLK.UBCC,J/CVTHD.2C : CLOCK ALU CARRY
:37406
:37407 :1111-----: FU IS SET,TAKE FAULT
U 1B7F, 0018,0038,F580,F988,0020,12B4 :37408 SET.V,RC[7]_K[.A],J/FLOAT.FAULT:
:37409

```

```

:37410 .TOC " G & H floating point : CVTBG,CVTWG,CVTLG"
:37411
:37412 :INPUT:
:37413 : D = SRC
:37414
:37415 144F: -----
:37416 CVTBG: D D.SXT[INST.DEP], : SIGN EXTEND SRC TO ALL OF D
:37417 SET.CC(INST), : SET CONDITON CODES
:37418 Q 0,
:37419 C[R.SD&SS, : INITIALIZE TO POSITIVE
:37420 SC_KC.20] : INITIAL EXPONENT
:37421
:37422 -----
:37423 ALU_KC[.3FF], R[R15]_ALU, : INITIALIZE EXP TO BIAS
:37424 SIGNS?
:37425 -----
:37426 =00 : BRANCH ON D31 AND D NE 0
:37427 : 00
:37428 D 0,RC[1]_0,J/WRITE.G : RESULT IS 0
:37429 =10 : 10
:37430 CVTIG.1:
:37431 D DAL.NORM, : NORMALIZE FRACTION
:37432 FE_SC-SHF.VAL, : ADJUST EXPONENT
:37433 ALD_0+K[.4]+1,SC_ALU, : GET LOW SHIFT COUNT
:37434 LAB_R[R15], : LATCH EXPONENT
:37435 J/CVTIG.2
:37436
:37437 -----
:37438 D 0-D, : NEGATE INTEGER
:37439 SD_NOT.SD, : SET SIGN BIT
:37440 J/CVTIG.1
:37441 =:END
:37442 -----
:37443 CVTIG.2:
:37444 SC FE, : SC GETS UNBIASSED EXPONENT
:37445 D DAL.SC, : D GETS FRACTION <LS>
:37446 ALU_D, RC[2]_ALU.RIGHT2 : START SHIFTING RIGHT
:37447
:37448 -----
:37449 ALU_LA+K[SC]+1, : GENERATE EXPONENT
:37450 Q ALU.LEFT3, : START SHIFTING IT LEFT
:37451 LC_RC[2] : LATCH FRACTION <MS> IN LC
:37452 -----
:37453 ALU_D.OXT[WORD], RC[1]_ALU, : STORE LONG FRAC IN RC1
:37454 Q_Q.LEFT : EXPONENT IS IN PLACE
:37455 -----
:37456 ALU_RC[2],D_ALU.RIGHT : D GETS FRAC<MS>
:37457 -----
:37458 D_PACK.FP : PACK FRACTION INTO D
:37459 -----
:37460 D_D.ANDNOT.K[.7FF0] : CLEAR EXPONENT BITS
:37461 -----
:37462 D D.OR.Q, : GENERATE LONG EXP
:37463 WRITE.G.DEST
:37464 -----
    
```

```

:37465 .TOC " G & H floating point : CONVERT G FLOATING TO INTEGER"
:37466
:37467 :INPUTS:
:37468 : RCO = SRC LONG EXP
:37469 : D = SRC LONG FRAC
:37470 1445: : 1400 + 45
:37471 :-----:
:37472 CVTGI.00:
:37473 Q D, : Q GETS SRC LONG FRAC
:37474 D_RC[TO], : D GETS SRC LONG EXP
:37475 CALL, J/CVTGI : CALL CONVERT ROUTINE
:37476 :-----:
:37477 :
:37478 : RETURN WITH DST IN D
:37479 1455:
:37480 ALU D,
:37481 N&Z_ALU, : THIS WORKS FOR LONG, WORD, AND BYTE
:37482 DT/INST.DEP,PSL.V?,J/GOUT.1 : USE GOUT TO CHECK FOR OVERFLOW
:37483
:37484 14C1: :-----:
:37485 CVTRGL:
:37486 Q D, : Q GETS SRC LONG FRAC
:37487 D_RC[TO], : D GETS SRC LONG EXP
:37488 CALL, J/CVTGI
:37489 :-----:
:37490 14D1:
:37491 ALU_0(A),Q ALU.LEFT,SI/DIV, : SHIFT HIGH BIT OF Q TO BIT 0
:37492 SS?,J/CVTRDL.0
:37493 =:END
:37494 =00 :00-----:
:37495 CVTGI: : ENTER HERE FOR G-FORMAT SOURCE
:37496 : < D , Q > = SRC
:37497 CVTGI.1:
:37498 Q D,D Q, : SWAP D AND Q
:37499 ALU_KT.80],RC[5]_ALU.LEFT3, : LOAD BIAS IN RC5
:37500 N&Z_ALU.V&C_0, : CLEAR PSL N& Z BITS
:37501 SS 0&SD 0, : CLEAR SS AND SD
:37502 CALL, J7UNPKG : CALL ROUTINE TO UNPACK G-FORMAT SRC
:37503 :01-----:
:37504 D 0, Q 0, RC[2]_0, : SRC = 0
:37505 N&Z_ALU.V&C_0, : SET PSL Z-BIT
:37506 SC R[ZERO],
:37507 RETURN10
:37508
:37509 :10-----: SRC NE 0
:37510 :
:37511 : SS = SD = SIGN
:37512 : ID[1] = SRC FRAC <MS>
:37513 : D = SRC FRAC <LS>
:37514 : RC4 = BIASSED EXPONENT
:37515 : R15 = UNBIASSED EXPONENT
:37516 : SC = LOW 10 BITS OF R15
:37517 : ALU CC REFLECT R15
:37518 U 19A2, 0000,003C,C5F4,2C00,0000,1BE3 Q_ID[1], SD_SS
:37519 =:END
    
```

```

:37520
:37521
U 1BE3, 0C00,003C,01E0,F800,0000,1BE4 :-----:
:37522 Q_D,D_Q
:37523
:37524 :-----:
:37525 D D.LEFT, SI/DIVD, Q Q.LEFT, : NORMALIZE FRACTION
:37526 ALU 0+Q, RC[2]_ALU.LEFT, : RC2 GETS NORM.FRAC<LS>
:37527 FE SC, : BACK UP EXPONENT IN FE
U 1BE4, 053F,1B14,0028,F990,0100,1B83 :37528 ALD? : TEST EXPONENT
:37529 :-----:
:37530 : D = FRACTION <MS>
:37531 : SC = LOW 10 BITS OF EXPONENT
:37532 : R15 = UNBIASSED EXPONENT
:37533 : RC[2] = FRACTION <LS>
:37534 : SD = SIGN BIT OF DESTINATION
:37535
:37536 :
:37537 : RETURNS:
:37538 : D = INTEGER
:37539 : Q<31> = ROUNDING BIT
:37540 : RC1 = FRACTION <MS>, RC2 = FRACTION <LS>
:37541 : EXCEPT FOR INTEGER SHIFT < 32.
:37542 : LOW 5 BITS OF SC = LOW 5 BITS OF EXPONENT
:37543
:37544 : USES:
:37545 : FE FOR EXPONENT
:37546 =0011 :BRANCH ON ALU Z AND N-BITS
:37547 :0011-----: EXP > 0
:37548 CVTGI.2:
:37549 SC SC-K[.20],FE SC-K[.20], : SUBTRACT 32. FROM EXPONENT
U 1B83, 0000,143C,75F8,F800,0184,B8A6 :37550 Q_0,SC?, J/CVTGI.20 : SC CONTAINS ALL OF EXP, TEST IT
:37551
:37552 :0111-----: EXP = 0
:37553 Q D, : Q GETS FRACTION <MS>
:37554 RC[1] D, : SAVE IT IN RC1 AS WELL
U 1B87, 0F01,003E,01E0,F988,0000,0010 :37555 D_0, RETURN10 : INT = 0, ROUND BIT = 1
:37556
:37557 :1011-----: EXP < 0
:37558 RC[1]_D, : SAVE FRAC <MS> IN RC1
:37559 D_0, : INT = 0
U 1B8B, 0F01,003E,01F8,F988,0000,0010 :37560 Q_0, RETURN10 : ROUND BIT = 0
:37561 =:END
:37562
:37563 =110 :BRANCH ON SC <9:5> NE 0
:37564 :110-----: 1<= NUMBER < 2**31
:37565 CVTGI.20:
:37566 RC[1]_D, : SAVE FRAC <MS> IN RC1
:37567 Q_D, : AND IN Q
:37568 D-DAL.SC, : D NOW GETS INTEGER
U 18A6, 0D01,123C,01E0,F988,0000,1B6E :37569 SS?, J/CVTGI.4 : TEST SIGN
:37570
:37571 :111-----: NUMBER >= 2**31
:37572 Q RC[2], : RESTORE FRAC <LS>
U 18A7, 0010,1438,01C0,F910,0000,18B6 :37573 SC? : IS IT >= 2**63 ?
:37574 =:END

```



```

:37575
:37576
:37577 =110 :-----:
:37578 :BRANCH ON SC<9:5> NE 0
:10-----: 2**31 <= NUMBER < 2**63
:37579 EALU FE,
:37580 D_DAL.SC, : CREATE INTEGER
:37581 Q_D.OXT[BYTE].OR.PACK.FP, : GENERATE FUNNY PACKED NUMBER
:37582 J7CVTGI.3 : IF INTEGER IS 80000000,SD=1,
:37583 : THEN THIS NUMBER IS 00008000
:37584 :111-----: 2**63<= NUMBER
:37585 SC_SC-K[.20] : SUBTRACT FOR LATER TEST
:37586 =;END
:37587 :-----:
:37588 RC[2]_0, : CLEAR OUT FRACTION <LS>
:37589 D_Q, Q_0, : SHIFT 32 TIMES LEFT
:37590 SC? : IS SC > 95 ?
:37591
:37592 :-----:
:37593 =110 :BRANCH ON SC<9:5>
:37594 :110-----: 2**63<= NUMBER < 2**95
:37595 D_DAL.SC, : D GETS LOW BITS OF INTEGER
:37596 RC[1]_D, : SAVE MANTISSA
:37597 Q_0,SET.V,SS?,J/CVTGI.X : SEE IF INT SHOULD BE PLUS OR MINUS
:37598
:37599 :111-----:
:37600 D_0,Q_0, RC[1]_0, : NUMBER >= 2**95
:37601 SET.V, RETURN10 : SET OVERFLOW BIT
:37602
:37603 =1110
:37604 CVTGI.X: :1110-----: POSITIVE
:37605 RETURN10
:37606
:37607 :1111-----: MINUS
:37608 D_0-D,RETURN10 : COMPLIMENT INTEGER
:37609
:37610 CVTGI.3:
:37611 ALU_Q.XOR.K[.8000],CLK.UBCC, : CHECK FOR MOST NEGATIVE NUMBER
:37612 Q_0
:37613
:37614 :-----:
:37615 :1-----:
:37616 RC[1]_LC, Q_LC,SC_SC-K[.20], : MOD SC SO ROUND BIT LINES UP
:37617 Z?
:37618
:37619 :-----:
:37620 =0 :BRANCH ON ALU Z-BIT
:37621 :0-----:
:37622 RC[2]_0, SET.V, SS?, J/CVTGI.4
:37623
:37624 :1-----:
:37625 RC[2]_0, SS?, J/CVTGI.4
:37626

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:37627 -----:
:37628 =1110 :BRANCH ON SS-BIT
:37629 :1110-----:
:37630 CVTGI.4:
:37631 RC[3]_D.SXT[INST.DEP], : CONVERT LONGWORD TO TARGET DT
:37632 Q_D, D_DAL.SC, : SAVE INTEGER IN Q, GET ROUND-BIT
:37633 J7CVTGI.5
:37634
:37635 :1111-----: NEGATIVE
:37636 Q_0-D, : NEGATE INTEGER
:37637 D_DAL.SC : D GETS ROUND BIT
:37638
:37639 -----:
:37640 RC[3]_Q.SXT[INST.DEP] : CONVERT LONGWORD TO TARGET DT
:37641
:37642 -----:
:37643 CVTGI.5:
:37644 LC_RC[3], ALU_Q.XOR.LC, : TEST UPPER BITS
:37645 CLR_UBCC, : CLOCK UPPER BITS
:37646 D_Q, Q_D : D GETS INTEGER, Q GETS ROUND BIT
:37647
:37648 -----:
:37649 Z? : TEST FOR OVERFLOW DUE TO DATATYPE
:37650
:37651 -----:
:37652 =0 :BRANCH ON ALU Z-BIT
:37653 :0-----: INTEGER OVERFLOW
:37654 SET.V, RETURN10
:37655
:37656 :1-----: NO OVERFLOW
:37657 RETURN10
:37658 -----:

```

U 1B6E, 0D02,C03C,01E0,F998,0000,1BEA

U 1B6F, 0D1F,2000,01C0,F800,0000,1BE9

U 1BE9, 0002,E03C,0180,F998,0000,1BEA

U 1BEA, 0C11,2020,01EC,F918,0010,1BEB

U 1BEB, 0000,013C,0180,F800,0000,1A3C

U 1A3C, 0000,003E,0180,F800,0020,0010

U 1A3D, 0000,003E,0180,F800,0000,0010

```

:37659 .TOC " G & H floating point : ACBG"
:37660
:37661 :INPUTS:
:37662 : RCO = LIMIT LONG EXP
:37663 : Q = LIMIT LONG FRAC
:37664 : RC2 = ADDEND LONG EXP
:37665 : D = ADDEND LONG FRAC
:37666
:37667 :TEMPORARIES:
:37668 : RC6 = ADDEND LONG FRAC
:37669 : T5 = LIMIT LONG EXP
:37670 : T6 = LIMIT LONG EXP
:37671 : T7 = INDEX ADDRESS
:37672 : RCO = INDEX LONG EXP
:37673 : RC1 = INDEX LONG FRAC
:37674 : RC7 = BRANCH ADDRESS
:37675
:37676
:37677 16C5: -----: 1600+C5
:37678 ACBG: TRAP.ACC[1], : RESET THE FPA
:37679 RC[T6]_D, : SAVE ADDEND LONG FRAC IN RC6
:37680 D_Q, : D GETS LIMIT LONG FRAC
:37681 SC_K[ZERO], : CLEAR SC
:37682 STATE_K[ZERO], : INITIALIZE STATE
:37683 SET.CC(LONG) : DO THIS TO CLEAR V-BIT
:37684
:37685 -----:
:37686 ID[T6] D, : SAVE LIMIT LONG FRAC IN T6
:37687 D_RC[T0], : READY TO SAVE LIMIT LONG EXP
:37688 INTRPT.STROBE : SO MANY OPERANDS, STROBE INTRPT
:37689
:37690 -----:
:37691 ALU D.AND.K[.7FF0], : C-BIT NOT SET
:37692 EALD_SC, CLK.UBCC : ISOLATE LIMIT EXPONENT
:37693 =10****0 : CLOCK EXPONENT
:37694 :10****0-----:
:37695 ID[T5] D, : SAVE LIMIT LONG EXP IN T5
:37696 ALU RC[T2], SS_ALU15, : SS GETS SIGN OF ADDEND
:37697 INTERRUPT.REQ?, : TEST FOR INTERRUPTS
:37698 CALL,J/ASPCG : EVALUATE INDEX ADDRESS
:37699
:37700 =11****0:11****0-----: MEMORY OPERAND
:37701 TRAP.ACC[1], : RESET THE FPA
:37702 ID[T7] D, : SAVE INDEX ADDRESS IN T7
:37703 J/ACBG.2
:37704
:37705 :11****1-----: REGISTER OPERAND
:37706 TRAP.ACC[1], : RESET THE FPA
:37707 Q_D, : SAVE INDEX LONG EXP IN RCO
:37708 D'R(PRN+1), : GET INDEX LONG FRAC
:37709 Z?, J/ACBG.3 : TEST FOR 0 LIMIT
:37710 -----:

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U 16C5, 0C01,00BC,1880,F9B0,14F4,7BEC

U 1BEC, 0810,0038,D980,3D00,4000,1BED

U 1BED, 0019,0034,3980,F800,0010,1840

U 1840, 0010,0E39,D581,3D10,0000,157E

U 1860, 0000,00BC,DC80,3C00,0000,1BEE

U 1861, 0800,01BC,00E0,F860,0000,1A44

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:37711 ACBG.2:
:37712 D[LONG] CACHE.WCHK, : READ INDEX LONG EXP
U 1BEE, 0000,003C,6580,5000,1404,7BF0 :37713 STATE_K[.10] : SET MEMORY OPERAND FLAG IN STATE
:37714 -----:
:37715 :
U 1BF0, 0000,003C,01E0,F803,0000,1BF1 :37716 Q_D, VA_VA+4 : SAVE INDEX LONG EXP IN Q
:37717 -----:
:37718 :
:37719 D[LONG] CACHE.WCHK, : READ INDEX LONG FRAC
U 1BF1, 0000,013C,0180,5000,0000,1A44 :37720 Z?, J/ACBG.3 : TEST FOR 0 LIMIT
:37721 -----:
:37722 :
:37723 =0 :BRANCH ON ALU Z-BIT
:37724 -----:
:37725 ACBG.3: RC[T0] Q, : SAVE INDEX LONG EXP IN TO
U 1A44, 0001,323C,0130,F980,0000,180C :37726 EALU?,J/ACBG.4 :
:37727 -----:
:37728 :1-----:
:37729 ALU_RC[T0], : GET LIMIT LONG EXP
U 1A45, 0010,0038,0180,F900,0800,1BF2 :37730 CHK.FLT.OPR : CHECK FOR -0
:37731 =:END
:37732 -----:
:37733 RC[T0] Q, : SAVE INDEX LONG IN TO
U 1BF2, 0F01,203C,01E0,F980,0000,1BF3 :37734 Q_D, D_0 : Q GETS INDEX LONG FRAC
:37735 -----:
:37736 :
U 1BF3, 0000,003C,D580,3C00,0000,1BF4 :37737 ID[T5]_D : CLEAR LIMIT LONG EXP
:37738 -----:
:37739 :
:37740 ID[T6] D, : CLEAR LIMIT LONG FRAC
U 1BF4, 0C00,123C,D980,3C00,0000,180C :37741 D_Q,EALU? :
:37742 -----:
:37743 :
:37744 =1*0 :BRANCH ON SS
:37745 -----:
:37746 ACBG.4:
:37747 RC[T3] D, : SAVE INEX LONG FRAC IN RC3
U 180C, 7001,0B3C,01F0,F99C,0000,19B8 :37748 Q IB.BDEST, PC PC+1, : GET BRANCH DISPLACEMENT
:37749 IB.TEST?, J/ACBG.5 : WAIT UNTIL IT ARRIVES
:37750 -----:
:37751 :1*1-----:
:37752 STATE_STATE.OR.K[.20], : REMEMBER THAT ADDEND IS NEGATIVE
:37753 RC[T3] D, : SAVE INEX LONG FRAC IN RC3
U 180D, 7001,0B3C,75F0,F99C,1404,39B8 :37754 Q IB.BDEST, PC PC+1, : GET BRANCH DISPLACEMENT
:37755 IB.TEST?, J/ACBG.5 : WAIT UNTIL IT ARRIVES
:37756 =:END

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:37757 =00 :-----:
:37758 ACBG.5:
U 1988, 0000,003D,0180,F800,0000,0E64 :37759 CALL,J/IB.TBM ; REFILL TB
:37760 :-----:
:37761 :-----:
U 1989, 0000,003D,0180,F800,0000,0B80 :37762 CALL, J/IB.ERR ; SERVE ERROR
:37763 :-----:
:37764 :-----:
U 198A, 7000,0B3C,01F0,F800,0000,1988 :37765 Q IB.BDEST, ; GET BRANCH DISPLACEMENT
:37766 IB.TEST?, J/ACBG.5
:37767 :-----:
:37768 :-----:
:37769 RC[T7] Q+PC+1, ; CALCULATE BRANCH ADDRESS
:37770 PC PC+T, ; PC GETS INCREMENTED TWICE
:37771 Q D, ; COPY INDEX LONG FRAC FOR SWAP
:37772 C[R.IB.SPEC, ; CLEAR FIRST BYTE OF BDEST
:37773 SC_K[.10] ; SHIFT COUNT FOR WORD SWAP
:37774 =:END
:37775 :-----:
U 1BF5, 0000,003C,1180,F800,1404,3848 :37776 STATE_STATE.OR.K[.4] ; THIS TELLS PACKG TO LEAVE C-BIT ALONE
:37777 =0**00
:37778 :0**00-----:
:37779 ALU K[.FFF9],SS_ALU15, ; SET SIGN-BIT
:37780 D DAL.SC, ; SWAP INDEX LONG FRAC
:37781 SC_K[.FFF9], ; SC GETS -7
:37782 CLR.IB.SPEC, ; CLEAR 2. BYTE OF BDEST
U 1848, DD18,0039,BD81,F800,0084,7AF2 :37783 CALL, J/UNPACKG ; G FORMAT UNPACK ROUTINE
:37784 :-----:
:37785 :0**01-----: INDEX = 0
U 1849, 0010,0038,01C0,F910,0000,1BF6 :37786 Q RC[T2], ; Q GETS ADDEND LONG EXP
:37787 J7ACBG.6A
:37788 :-----:
:37789 :0**10-----: ADDEND = 0
U 184A, 0010,0038,01C0,F900,0000,1BF8 :37790 Q RC[T0], ; Q GETS INDEX LONG EXP
:37791 J7ACBG.6B
:37792 :-----:
:37793 =0**11 :0**11-----: BOTH OPERANDS NON-ZERO
U 184B, 0000,1B3D,C9F0,2D20,0000,19E3 :37794 LC RC[T4],Q ID[T2], ; LATCH EXPONENT
:37795 ALD?,CALL, J/ADDG.10 ; CALL ADDG SUBROUTINE
:37796 :-----:
:37797 :1**11-----:
:37798 =1**11
:37799 Q ID[T7], ; GET ADDRESS OF INDEX IF MEMORY
:37800 LC RC[T1], ; LATCH INDEX LONG FRAC
U 185B, 0000,163C,DDF0,2D08,0000,1912 :37801 STATE4?, J/ACBG.6 ; MEMORY OR REGISTER ?

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:37802
:37803
:37804 ACBG.6A:
:37805 ALU_Q.ANDNOT.K[F], : ISOLATE SIGN AND EXPONENT BITS
U 1BF6, 0019,6024,6180,F800,0070,1BF7 :37806 SET_CC(WORD) : SET CC
:37807
:37808
:37809 Q_ID[T7],LC_RC[T1], : LOAD INDEX ADDRESS AND ADDEND FRAC
U 1BF7, 0000,163C,DDF0,2D08,0000,1912 :37810 STATE4?,J/ACBG.6 : MEM OR REG?
:37811
:37812 ACBG.6B:
:37813
:37814 ALU_Q.ANDNOT.K[F], : ISOLATE SIGN AND EXP
U 1BF8, 0019,6024,6180,F800,0070,1BF9 :37815 SET_CC(WORD) : SET CC
:37816
:37817
:37818 Q_ID[T7],LC_RC[T3] : LOAD INDEX ADDRESS AND LONG FRAC
U 1BF9, 0000,003C,DDF0,2D18,0000,1BFA :37819
:37820
:37821 RC[T1] LC, : PUT NEW INDEX FRAC INTO RC1
U 1BFA, 0010,1638,0180,F988,0000,1912 :37822 STATE4?,J/ACBG.6 : MEM OR REG?
:37823
:37824
:37825 =10 :BRANCH ON BIT 4 OF STATE
:37826 :10
:37827 ACBG.6: R(PRN)_D, SS_ALU15, : STORE INDEX LONG EXP
U 1912, 0001,003C,C181,3CD8,0000,1543 :37828 ID[T0]_D, : SAVE INDEX LONG EXP IN TO
:37829 J/ACBG.7
:37830
:37831 :11
:37832 VA_Q, : RELOAD ADDRESS OF INDEX
U 1913, 0001,203C,C180,3C00,0200,1BFB :37833 ID[T0]_D : SAVE INDEX LONG EXP IN TO
:37834 =:END
:37835
:37836 CACHE_D[INST.DEP], : STORE INDEX LONG EXP
U 1BFB, 0001,C03C,0181,3000,0000,1BFC :37837 ALU_D,SS_ALU15 : SAVE SIGN
:37838
:37839
:37840 VA_VA+4, : ADVANCE ADDRESS
U 1BFC, 0810,0038,D5F0,2C03,0000,1BFD :37841 D [C : D GETS INDEX LONG FRAC
:37842 Q_ID[T5] : GET LIMIT LONG EXP FOR COMAPRE
:37843
:37844
:37845 CACHE_D[LONG], : STORE INDEX LONG FRAC
U 1BFD, 0000,163C,0180,3000,0000,1851 :37846 STATE5?, J/ACBG.8 : TEST ADDEND SIGN

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:37847
:37848
:37849 ACBG.7: R(PRN+1) LC, : STORE INDEX LONG FRAC
:37850 Q ID[T5], : Q GETS LIMIT LONG EXP
U 1543, 0010,1638,D5F0,2CE0,0000,1851 :37851 STATES? : TEST ADDEND SIGN
:37852
:37853
:37854 =01 :BRANCH ON BIT 5 OF STATE
:37855 :01
:37856 ACBG.8:
:37857 RC[T3] Q, : PUT LIMIT WHERE ACBF WANTS IT
:37858 Q ID[T0], : GET INDEX TO
U 1851, 0001,203C,C1F0,2D98,0000,1544 :37859 J/ACBG.60 : JOIN ACBF ROUTINE
:37860
:37861 :11
:37862 ALU K[.8000], : SET ALU15
U 1853, 0018,0038,4585,F800,0000,1851 :37863 SS SS.XOR.ALU15&SD_ALU15, : COMPLEMENT INDEX SIGN IN SS
:37864 J/ACBG.8
:37865 :END
:37866
U 1544, 0000,1A3C,1180,F800,1404,5B8D :37867 ACBG.60:STATE_STATE.ANDNOT.K[.4],PSL.V? : CLEAR STATE2
:37868
:37869
:37870 =1101 :BRANCH ON PSL V-BIT
:37871 :1101
:37872 D Q.XOR.RC[T3], : D GETS DIFF. BETWEEN INDEX AND LIMIT
:37873 WORD, CLK.UBCC, : TESTING ONLY SIGN, EXP, AND MSB
:37874 SD SS, : SD GETS INDEX SIGN
U 1B8D, 0811,6020,0584,F918,0114,7057 :37875 FE_K[.1], CLK.UBCC, : CLEAR EALU CC
:37876 J/ACBF.00 : JOIN ACBF-EC
:37877
:37878 :1111
U 1B8F, C000,003C,0180,F804,4000,0062 :37879 CLR.IB.OPC, PC_PC+1, J/IRD : DO NOT BRANCH
:37880 =:END

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.TOC " G & H floating point : HUGE FLOATING NOTATION"  
:37881  
:37882  
:37883 : THE FOLLOWING NOTATION IS USED IN COMMENTS BELONGING TO THE MICROCODE FOR THE  
:37884 : IMPLEMENTATION OF THE HUGE INSTRUCTION SET ON THE VAX11/780  
:37885 : IN ORDER OF SIGNIFICANCE, THE PACKED LONGWORDS ARE NAMED:  
:37886 : OP LONG EXP  
:37887 : OP LONG FRAC1  
:37888 : OP LONG FRAC2  
:37889 : OP LONG FRAC3  
:37890  
:37891 : AFTER EVALUATION OF TWO OPERANDS,  
:37892 : THE VARIOUS LONGWORDS ARE STORED AS FOLLOWS, IN ORDER OF SIGNIFICANCE:  
:37893  
:37894 : OP1: RC0, ID[T0], RC1, ID[T1]  
:37895 : OP2: RC2, ID[T2], RC3, ID[T3]  
:37896 : IN ADDITION,  
:37897 : D = OP1 LONG EXP  
:37898  
:37899 : AFTER UNPACKING, THE OPERANDS ARE STORED AS FOLLOWS:  
:37900 : OP1:  
:37901 : EXPONENT IN RC4  
:37902 : RC0 = OP1 FRAC <VMS> (VERY MOST SIGNIFICANT)  
:37903 : T0 = OP1 FRAC <AMS> (ALMOST MOST SIGNIFICANT)  
:37904 : RC1 = OP1 FRAC <ALS> (ALMOST LEAST SIGNIFICANT)  
:37905 : T1 = OP1 FRAC <VLS> (VERY LEAST SIGNIFICANT)  
:37906  
:37907 : OP2:  
:37908 : EXPONENT IN RC6  
:37909 : RC2 = OP2 FRAC <VMS>  
:37910 : T2 = OP2 FRAC <AMS>  
:37911 : RC3 = OP2 FRAC <ALS>  
:37912 : T3 = OP2 FRAC <VLS>  
:37913  
:37914 : WHEN WRITING DESTINATION, THE PACKED OPERANDS SHOULD BE AS FOLLOWS:  
:37915 : DST:  
:37916 : RC[T0] = DST LONG EXP  
:37917 : ID[T0] = DST LONG FRAC1  
:37918 : RC[T1] = DST LONG FRAC2  
:37919 : ID[T1] = DST LONG FRAC3  
:37920  
:37921 : STATE REGISTER USAGE:  
:37922 : UNPACK ROUTINE USES STATE<4> FOR LOOP COUNT.  
:37923 : STATE<1> SIGNALS EMOD
```



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:37924 .TOC " G & H floating point : FLOATING H FORMAT COMPARE"
:37925
:37926 :INPUTS:
:37927 : RC0-ID[T1] CONTAINS OPERAND 1
:37928 : RC2-ID[T3] CONTAINS OPERAND 2
:37929
:37930 1482:
:37931 CMPH: -----:
:37932 D_RC[T0], : GET OP1 LONG EXP
:37933 SS_ALU15 : SS GETS SIGN
:37934
:37935 -----:
:37936 ALU D.ANDNOT.K[.8000], : ISOLATE EXPONENT
:37937 WORD, CLK.UBCC : CLOCK EXPONENT
:37938
:37939 :00-----:
:37940 =00 CALL,J/CMPH.S : CALL SUBROUTINE
:37941
:37942 :01-----:
:37943 CMPH.A: ALU_RC[T0], : SET PSL CC ON OP1
:37944 N&Z_ALU.V&C 0,WORD, : CLOCK IT ON SIGN AND EXP
:37945 CLR.IB.OPC,PC_PC+1,J/IRD : FINISHED
:37946
:37947 :10-----:
:37948 SS_SD.SS?,J/CMPH.C : ABSOLUTE VALUES ARE EQUAL,TEST SIGNS
:37949
:37950 CMPH.B: :11-----:
:37951 ALU_R[R15].XOR.K[.8000], : SET CC ON -OP2
:37952 N&Z_ALU.V&C 0,WORD, : CLOCK PSL CC
:37953 CLR.IB.OPC,PC_PC+1,J/IRD
:37954 =:END
:37955 =1110
:37956 CMPH.C: :1110-----: EQUAL
:37957 ALU 0(A),N&Z_ALU.V&C 0, : EQUALITY
:37958 CLR.IB.OPC,PC_PC+1,J/IRD
:37959
:37960 :1111-----: SIGNS ARE DIFFERENT
:37961 SS? : FIND OUT WHICH ONE IS POSITIVE
:37962
:37963 =1110 :1110-----:
:37964 J/CMPH.B : OP2 IS POS
:37965
:37966 :1111-----:
:37967 J/CMPH.A : OP1 IS POS
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:37968 CMPH.S: :-----:
:37969 STATE_STATE.ANDNOT.K[.F], : CLEAR FIRST FOUR BITS OF STATE
:37970 Q_RC[T2], : Q GETS OP2 LONG EXP
:37971 SS_SS.XOR.ALU15&SD_ALU15, : TAKE XOR OF SIGN BITS
U 1548, 0010,0138,61C5,F910,1404,5A4C :37972 Z? : IS OP1 = 0?
:37973
:37974 :-----:
:37975 =0 :BRANCH ON ALU Z-BIT
:37976 :0
:37977 CMPHO: ALU_Q.ANDNOT.K[.8000], : ISOLATE OP2 EXPONENT
:37978 CLK_UBCC,WORD, : CLOCK OP2 EXPONENT
U 1A4C, 0019,6024,4580,F800,0010,1549 :37979 J/CMPHO1
:37980
:37981 :1-----:
:37982 ALU_D.AND.K[.8000], : ISOLATE SIGN BIT
:37983 CHK.FLT.OPR, : CHECK FOR -0
U 1A4D, 0019,0034,4580,F800,0800,1A4C :37984 J/CMPHO
:37985 =;END
:37986
:37987 CMPHO1: ALU_Q,R[R15]_ALU : SAVE OP2 LONG EXP IN R15
:37988
:37989 :-----:
:37990 D_D.ANDNOT.K[.8000], : CLEAR SIGN BIT
:37991 Z? : TEST FOR OP2 = 0
:37992
:37993 :-----:
:37994 =0 :BRANCH ON ALU Z-BIT
:37995 :0
:37996 Q_Q.ANDNOT.K[.8000], : CLEAR SIGN BIT OF LIMIT
U 1A54, 0019,2024,45C0,F800,0000,154B :37997 J7CMPH1 : BRANCH ON SS REMOVED
:37998
:37999 :1-----:
:38000 ALU_Q.AND.K[.8000], : ISOLATE SIGN BIT
:38001 CHK.FLT.OPR, : CHECK FOR -0
U 1A55, 0019,2036,4580,F800,0800,0001 :38002 RETURN1
:38003 =;END
:38004
:38005 CMPH1: ALU_D-Q, WORD, CLK_UBCC : COMPARE EXPONENTS, OP1 - OP2
:38006
:38007 :-----:
:38008 STATE_STATE.OR.K[.1], : STATE GETS 1, TO DO ID[TO] NEXT
:38009 ALU_Q-D, LONG, CLK_UBCC, : COMPARE HIGH FRACTION BITS, OP2-OP1
U 154C, 001D,3B00,0580,F800,1414,3BB3 :38010 ALU?, J/CMPH2 : TEST EXPONENT-DIFFERENCE, OP1-OP2
:38011
:38012 :-----:
U 154E, 0000,003E,0180,F800,0000,0003 :38013 RETURN3
:38014
    
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:38015 :-----;
:38016 =0011 :BRANCH ON ALU N&Z BITS
:38017 :0011-----;
U 1883, 0000,003E,0180,F800,0000,0001 :38018 CMPH2: RETURN1 ; SET PSL ON OP1
:38019 :-----;
:38020 :0111-----;
:38021 SC_K[.30], ; START WITH ID[T0]
U 1887, 0000,1B3C,7980,F800,0084,7BDA :38022 ALD?,J/CMPHL.3 ; BRANCH ON OP2-OP1
:38023 :-----;
:38024 :1011-----;
U 1888, 0000,003E,0180,F800,0000,0003 :38025 RETURN3 ; SET PSL ON -OP2
:38026 =:END
:38027 :-----;
:38028 =010 :BRANCH ON STATE BITS 0 AND 2
:38029 :010-----;
U 1942, 0803,403C,E580,3C00,0000, 51 :38030 CMPHL.0:ALU D.OXT[WORD],D_ALU, ; ISOLATE WORD PART
:38031 ID[T9], ; SAVE LONGWORD IN T9
:38032 J/CMPHL.02
:38033 :-----;
:38034 :011-----;
:38035 ALU Q.OXT[WORD],D_ALU, ; ISOLATE WORD PART
:38036 Q ID(SC), ; Q GETS OP2 FRACTION PART
U 1943, 0803,603C,09F0,2400,0084,B550 :38037 SC_SC-K[.2], ; POINT TO OP1 AGAIN
:38038 J/CMPHL.01
:38039 :-----;
:38040 :110-----;
U 1946, 0000,003E,0180,F800,0000,0002 :38041 RETURN2 ; EQUALITY
:38042 =:END
:38043 :-----;
:38044 CMPHL.01:ALU Q.OXT[WORD]-D, ; COMPARE LOW WORD FIRST, OP2-OP1
:38045 CLK.[BCC,WORD, ; CLOCK DIFFERENCE
:38046 D,Q,Q ID(SC), ; RETRIEVE ORIGINAL OP1, D GETS OP2
U 1550, 0C1F,6000,01F0,2400,0090,D553 :38047 SC_SC+1, ; POINT TO NEXT OPERANDS
:38048 J/CMPHL.2
:38049 :-----;
:38050 :-----;
U 1551, 0010,0038,09C0,F830,0084,B552 :38051 CMPHL.02:Q_RC(SC),SC_SC-K[.2] ; Q GETS OP2 FRACTION PART
:38052 :-----;
:38053 :-----;
:38054 ALU_Q.(OXT[WORD]-D, ; COMPARE WORD PARTS, OP2-OP1
:38055 CLK.[BCC,WORD, ; CLOCK DIFFERENCE
U 1552, 0C1F,6000,E5F0,2C00,0010,1553 :38056 D,Q,Q ID[T9], ; RETRIEVE WHOLE OP1 LONGWORD
:38057 J7CMPHL.2
:38058
  
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:38059 :-----:
:38060 CMPHL.2:ALU D-Q, LONG, CLK.UBCC, : CLOCK NEXT WORD DIFFERENCE, OP2-OP1
:38061 STATE_STATE+1, : GET TO NEXT STATE
U 1553, 001D,1B00,0180,F800,1410,DBCA :38062 ALU? : BRANCH ON WORD DIFF, OP1-OP2
:38063 :-----:
:38064 :-----:
:38065 =1010 :BRANCH ON ALU Z AND C BITS
:38066 :1010-----: BORROW ON OP2-OP1
U 1BCA, 0000,003E,0180,F800,0000,0001 :38067 RETURN1 : SET PSL CC ON OP1
:38068 :-----:
:38069 :1011-----: NO BORROW ON OP2-OP1
U 1BCB, 0000,003E,0180,F800,0000,0003 :38070 RETURN3 : SET PSL ON -OP2
:38071 :-----:
:38072 =1111 :1111-----:
U 1BCF, 0000,1B3C,0180,F800,0000,1BDA :38073 ALU? : TEST NEXT WORD DIFFERENCE
:38074 =:END
:38075 :-----:
:38076 =1010 :BRANCH ON ALU Z AND C BITS
U 1BDA, 0000,003E,0180,F800,0000,0001 :38077 :1010-----: BORROW ON OP2-OP1
:38078 CMPHL.3:RETURN1 : SET PSL CC ON OP1
:38079 :-----:
:38080 :1011-----: NO BORROW ON OP2-OP1
U 1BDB, 0000,003E,0180,F800,0000,0003 :38081 RETURN3 : SET PSL CC ON -OP2
:38082 =1111
:38083 :1111-----: EQUALITY
:38084 D_RC(SC), : GET NEXT OP1 FRACTION PART
:38085 Q_ID(SC), : FROM RC OR ID
:38086 SC_SC+K[.2], : POINT TO OP2 FRACTION
U 1BDF, 0810,1738,09F0,2430,0084,9942 :38087 STATE3-0?,J/CMPHL.0
:38088 =:END :-----:

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:38089
:38090 .TOC " G & H floating point : MOVE H FORMAT FLOATING POINT NUMBERS"
:38091
:38092
:38093 : INPUTS:
:38094 : RC[TO] = OP LONG EXP
:38095 : ID[TO] = OP LONG FRAC1
:38096 : RC[T1] = OP LONG FRAC2
:38097 : ID[T1] = OP LONG FRAC3
:38098
:38099 : OUTPUTS:
:38100 : D = RCO =DST LONG EXP
:38101 : ID[TO] = DST LONG FRAC1
:38102 : RC1 = DST LONG FRAC2
:38103 : ID[T1] = DST LONG FRAC3
:38104
:38105 -----
:38106 MOVH: : ENTER HERE FROM 1441 ON G-FORK
:38107 ALU RC[TO], Q_ALU, : GET OP LONG EXP
:38108 SET.CC(INST), : NEED TO CLEAR PSL-V
:38109 D_0 : IN CASE WE NEED TO CLEAR FRACTION
:38110
:38111 -----
:38112 ALU Q.ANDNOT.K[.8000], : ISOLATE EXPONENT
:38113 CLK.LBCC, WORD : CLOCK ALU Z-BIT
:38114
:38115 -----
:38116 D Q[INST.DEP]K[.8000], : AND OR XOR, MOV OR MNEG
:38117 RC[TO] ALU, : NEW LONG EXP IN RCO
:38118 NZ_ALU,WORD, : CLOCK PSL N AND Z
:38119 ? : IS IT 0 ?
:38120
:38121 -----
:38122 =0 : BRANCH ON ALU Z-BIT
:38123 : 0
:38124 WRITE.G.DEST : NON-ZERO, WRITE DESTINATION
:38125
:38126 : 1-----
:38127 RC[T1] Q.OXT[WORD], : CLEAR RC1
:38128 CHK.FLT.OPR, : CHECK FOR -0
:38129 D_0,
:38130 NZ_ALU,WORD, : CLOCK PSL N AND Z
:38131 J/WRITE.DEST.0
:38132 =:END :
    
```

U 1558, 0F10,C038,01C0,F900,0070,1559

U 1559, 0019,6024,4580,F800,0010,155A

U 155A, 0819,610C,4580,F980,0060,1A58

U 1A58, F000,U03F,01F0,F847,0000,1400

U 1A59, 0F03,603C,0180,F988,0860,190E

```

:38133 NEWMOVO:
:38134 -----
U 155B, 0801,203C,CDF0,2D18,0030,155C :38135 ALU Q,D,ALU,Q,IDE[T3], : MOVE DATA AROUND
:38136 LC_RC[T3],N_AMX.Z_TST : LATCH LONG FRAC2
:38137 -----
:38138 :
:38139 IDE[T0]_D, : STORE LONG FRAC1 IN T0
U 155C, 0C10,0038,C180,3D88,0030,155E :38140 RC[T1]_LC,N_AMX.Z_TST, : RC1 GETS LONG FRAC2
:38141 D_Q : D GETS LONG FRAC3
:38142 -----
:38143 :
U 155E, 0001,003C,C580,3C00,0030,1560 :38144 IDE[T1]_D,ALU_D,N_AMX.Z_TST : FINALLY STOR LONG FRAC3
:38145 -----
:38146 :
U 1560, 0810,0039,0180,F900,0000,147E :38147 D_RC[T0],CALL,J/SPECG : D GETS LONG EXP

```

```

:38148 .TOC " G & H floating point : CONVERT INTEGER TO H-FLOATING"
:38149
:38150 14CC: : CONVERT BYTE,WORD, OR LONG TO H-FORMAT FLOATING
:38151 : EXPECTS SRC OPERAND IN D
:38152 CVTIH:
:38153 -----
:38154 D D.SXT[INST.DEP], : SIGN EXTEND SRC TO ALL OF D
:38155 SET.CC(INST), : SET CONDITION CODES
:38156 Q 0, : FOR NORMALIZING
:38157 C[R.SD&SS, : INITIALIZE TO POSITIVE
:38158 SC_KC.20] : MAXIMAL EXPONENT
:38159
:38160 -----
:38161 ALU_KC[.4000], R[R15]_ALU, : STORE BIAS IN R15
:38162 SIGNS? : BRANCH ON SIGN AND ZERONESS
:38163
:38164 -----
:38165 =00 : BRANCH ON D31 AND D NE 0
:38166 :00
:38167 D 0,RC[1] 0, : SRC IS 0
:38168 J/WRITE.DEST.0
:38169 =10 :10
:38170 CVTIH.1:D DAL.NORM, : NORMALIZE SRC
:38171 SC_SC-SHF_VAL, : ADJUST EXPONENT FOR LEADING 0'S
:38172 LAB_R[R15],
:38173 J/CVTIH.2
:38174
:38175 -----
:38176 D 0-D : NEGATE INTEGER
:38177 LAB_R[R15] : LATCH EXPONENT
:38178 =;END
:38179
:38180 -----
:38181 ALU_LA.OR.KC[.8000], : SET SIGN BIT IN EXPONENT
:38182 R[R15]_ALU,J/CVTIH.1
:38183
:38184 -----
:38185 CVTIH.2:ALU_LA.OR.K[SC],R[R15]_ALU, : R15 GETS EXPONENT
:38186 DK/[LEFT] : GET RID IF HIDDEN BIT
:38187
:38188 -----
:38189 ALU_D.OXT[WORD],D_ALU, : D GETS LONG FRAC1
:38190 Q D, : Q GETS INTEGER
:38191 LAB_R[R15] : LATCH EXPONENT
:38192
:38193 -----
:38194 ID[TO] D, : WRITE ID[TO] WITH LONG FRAC1
:38195 ALU_Q-D,D_ALU : D GETS HIGH WORD OF FRACTION
:38196
:38197 -----
:38198 ALU D+LB,Q_ALU,D_0, : Q GETS LONG EXP
:38199 RC[TO]_ALU : AND SO DOES RC0
:38200
:38201 -----
:38202 CVTIG.3:ID[1] D,RC[1]_D,D_Q,
: J/WRITE.G

```

U 14CC, 0802,C03C,75FF,F800,00F4,7561

U 1561, 0018,0D38,B180,FAF8,0000,19D8

U 19D8, 0F03,003C,0180,F988,0000,190E

U 19DA, 0E00,003C,0180,FA78,008C,B563

U 19DB, 081F,2000,0180,FA78,0000,1562

U 1562, 0018,0030,4580,FAF8,0000,19DA

U 1563, 0518,0030,1D80,FAF8,0000,1564

U 1564, 0803,403C,01E0,FA78,0000,1566

U 1566, 081D,2000,C180,3C00,0000,1568

U 1568, 0F0D,0014,01C0,F980,0000,156A

U 156A, 0C01,003C,C580,3D88,0000,18B0

```

:38203 .TOC " G & H floating point : CONVERT H FORMAT FLOATING POINT"
:38204
:38205 : ENTER HERE FROM CVTFG-INSTRUCTION,
:38206 : FOR CVTFH, WITH OPCODE 98FD, WE HAVE:
:38207 : WITH Q=UNPACKED OPERAND, SC = EXPONENT,
:38208 : SS = SIGN
:38209 : FOR CVTDH, WITH OPCODE 32FD, WE HAVE:
:38210 : RC2 = LONG EXP
:38211 : RC3 = LONG FRAC OF SRC
:38212
:38213 =10 : BRANCH ON IR<1>
:38214 :10-----: CVTFH
:38215 CVTFH: QK/LEFT2,SI/ZERO, : GET RID OF OVERFLOW AND HIDDEN BIT
:38216 : FE,SC-K[.80], : SUBTRACT F-BIAS OF .80
:38217 : CLR.UBCC, : CHECK FOR NEGATIVE EXPONENT
:38218 : ALU D,RC[T1] ALU, : CLEAR RC[T1]
:38219 : SD_SS,J/CVTFH.00 : SD GETS SIGN
:38220
:38221 :11-----: CVTDH
:38222 : Q RC[T2], : Q GETS LONG EXP
:38223 : J7CVTDH
:38224 =:END
:38225
:38226 CVTFH.00:ID[T1] D, : CLEAR OUT ID1
:38227 : ALU_Q.0XT[WORD],D_ALU : D GETS FRAC1
:38228
:38229 :-----:
:38230 : ALU Q.XOR.D,Q_ALU, : Q GETS HIGH WORD OF FRACTION PART
:38231 : ID[T0]_D, : STORE FRAC1 IN T0
:38232 : D_0
:38233
:38234 :-----:
:38235 : Q Q.OR.K[.4000], : ADD IN BIAS
:38236 : SC_FE, : GET UNBIASSED EXPONENT
:38237 : SC.NE.0? : IS SRC = 0?
:38238
:38239 :-----:
:38240 =0** :BRANCH ON SC NE 0
:38241 :0**-----:
:38242 : ALU RC[T3],CHK.FLT.OPR, : CHECK FOR -0
:38243 : ID[T0]_D,SC_SC-FE,Q_0 : MAKE IT A CLEAN 0
:38244
:38245 :1**-----:
:38246 =:END : D_K[SC] : GET EXPONENT
:38247
:38248 :-----:
:38249 : ALU D.SXT[BYTE]+Q, : ADD IN EXPONENT
:38250 : RC[T0] ALU, : STORE LONG EXP
:38251 : D_ALU,EALU? : TEST SIGN
:38252

```

U 1982, 0001,003C,418C,F988,0114,B56E

U 1983, 0010,0038,01C0,F910,0000,19F8

U 156E, 0803,603C,C580,3C00,0000,1570

U 1570, 0F1D,2020,C1C0,3C00,0000,1571

U 1571, 0019,2C30,B1C0,F800,0081,1A11

U 1A11, 0010,0038,C1F8,3D18,0880,BA15

U 1A15, 0818,0038,1D80,F800,0000,1572

U 1572, 081E,9214,0180,F980,0000,1BBE


```

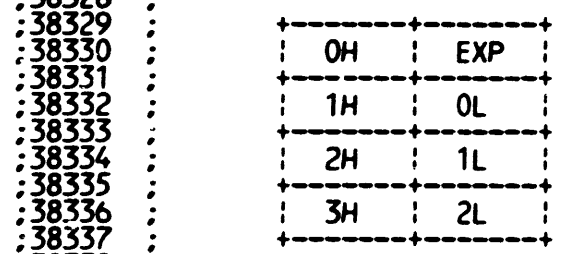
:38253 :-----:
:38254 =1110 :BRANCH ON SS
:38255 :1110-----:
U 1BBE, 0010,4038,0180,F900,0060,1880 :38256 CVTFH.2:ALU RC[T0],N&Z_ALU,WORD, : SET CONDITION CODES
:38257 J/WRITE.G
:38258 :-----:
:38259 :1111-----:
U 1BBF, 0819,0030,4580,F980,0000,18BE :38260 D D.OR.K[.8000],RC[T0]_ALU, : STORE LONG EXP IN RC0
:38261 J7CVTFH.2
:38262 =:END
:38263 =00 :00-----:
:38264 CVTDH: CLR.SD&SS,
:38265 D RC[T3], : GET LONG FRAC
:38266 CALL,J/UNPK : UNPACK THE DOUBLE OPERAND IN <Q,D>
:38267 :-----:
:38268 =01 :01-----: SRC = 0
:38269 D 0,Q 0, : WRITE ZERO
U 19F9, 0F00,003C,01F8,F800,0000,190E :38270 J7WRITE.DEST.0
:38271 :-----:
:38272 : RETURN WITH:
:38273 : SC = BIASSED EXP
:38274 : RC5 = UNPACKED FRAC <MS>
:38275 : D = UNPACKED FRAC <LS>
:38276 : SS= SD = SIGN
:38277 :-----:
:38278 =10 :10-----: SRC IS NON-ZERO
U 19FA, 0F10,0038,C1C0,3D28,0000,1573 :38279 ID[T0] D, : STORE FRAC <AMS>
:38280 Q_RC[T5],D_0
:38281 =:END
:38282 :-----:
U 1573, 0001,203C,4180,F980,0084,B578 :38283 RC[T0] Q,
:38284 SC_SC-RC[.80] : UNBIAS THE EXP
:38285 :-----:
:38286 :-----:
U 1578, 0018,0038,B1C0,F800,0000,1579 :38287 Q_K[.4000] : H-FORMAT BIAS
:38288 :-----:
:38289 :-----:
U 1579, 0818,0038,1D80,F800,0000,157A :38290 D_K[SC] : D GETS OLD UNBIASSED EXP
:38291 :-----:
:38292 :-----:
:38293 : ALU D.SXT[BYTE]+Q, : NEW BIASSED EXP
:38294 RC[T6] ALU, : STORE IT IN RC6
U 157A, 0F1E,8014,01F8,F980,0000,19C9 :38295 D_0,Q_0,J/CVTGH.W
:38296 :-----:

```

```
:38297 .TOC " G & H floating point : H FORMAT UNPACK ROUTINE"  
:38298  
:38299 :ROUTINE TO UNPACK H FORMAT FLOATING OPERANDS.  
:38300  
:38301 :INPUTS:  
:38302 : RC0-T3 CONTAIN THE TWO INPUT OPERANDS  
:38303 : IR<2:1> = TYPE OF OPERATION BEING PERFORMED  
:38304 : FOR EMODH, LOW 15 BITS OF RC6 = EXTENDER  
:38305 : STATE<1> SIGNALS EMODH(WHEN=1) OR NOT  
:38306 :OUTPUTS:  
:38307 : RC0-ID[T3] = FRACTION PARTS  
:38308 : RC4 = OP1 EXPONENT  
:38309 : RC6 = OP2 EXPONENT  
:38310 : SS = SIGN1.XOR.SIGN2.XOR.IR<1>  
:38311 : R15 = OP2 EXP -OP1 EXP  
:38312 : FE = NABS OF LOW BITS OF EXPONENT DIFFERENCE  
:38313 : IF ONE OPERAND IS 0, THE OTHER IS LEFT UNCHANGED  
:38314 :TEMPORARIES:  
:38315 : STATE<4> IS USED FOR LOOP FLAG  
:38316 : D,Q,SC ARE USED FOR A VARIETY OF OPERATIONS.  
:38317 : SD IS USED  
:38318 :RETURNS:  
:38319 : RETURN @ 1 IF OP1 = 0 , OP2 <> 0  
:38320 : RETURN @ 2 IF OP1 <> 0, OP2 = 0  
:38321 : RETURN @ 3 IF BOTH OPERANDS ARE NON ZERO  
:38322 : RETURN @ 4 IF BOTH OPERANDS ARE 0  
:38323
```

:38324 :IN ADDTION TO UNPACKING, BOTH OPERANDS ARE CHECKED FOR -0
:38325

:38326 : NOTATION:
:38327 : BELOW, THE PIECES OF THE NUMBER IS REFERRED TO AS:



U 157B, 0810,0038,7980,F910,0084,7580

```
:38338  
:38339 UNPACKH:  
:38340 SC_K[.30], : POINTER, X, TO OPERAND  
:38341 ALU_RC[T2],D_ALU  
:38342  
:38343
```

U 1580, 0019,4024,4580,F800,0010,1581

```
:38344 :-----;  
:38345 ALU_D.ANDNOT.K[.8000],  
:38346 CLK.UBCC,WORD  
:38347 :-----;
```

U 1581, 0010,0038,C1C5,F900,0104,78CC

```
:38348 Q_RC[T0], : GET LONG EXP  
:38349 SS_SS.XOR.ALU15&SD_ALU15, : USE SIGN TO COMPLEMENT SS  
:38350 FE_K[.FFFF] : SHIFT COUNT OF -1
```

```

:38351 =01100 ;01100-----;
:38352 ALU Q.OXT[WORD].ANDNOT.K[.8000], ; ISOLATE EXPONENT PART
:38353 RC[4]_ALU, ; SAVE IT
:38354 CLK.UBCC, ; CLOCK IT
:38355 D_Q, ; D GETS 0HEXP
:38356 Q_ID(SC), ; Q GETS 1HOL
:38357 SC_FE,FE_SC, ; FE GETS X, SC GETS -1
:38358 Z?, ; IS OP2 = 0 ?
U 18CC, 0C1B,6125,45F0,25A0,0191,1A64 :38359 CALL,J/UNP.SUBR.2 ; CALL UNPACK SUBROUTINE
:38360
:38361 =11100 ;11100-----;
:38362 RETURN1 ; OP1 = 0
:38363
:38364 ;RETURN WITH:
:38365 ;BRANCH ON EMOD-BIT
:38366
:38367 =11101 ;11101-----;
:38368 UNPACKH.1:SC_SC+1, ; NOT EMODH
:38369 ID(SC) D, ; POINT TO NEXT LONG EXP
:38370 Q_RC[2], ; STORE LAST FRACTION WORD
:38371 SGN/ADD.SUB, ; Q GETS LONG EXP
U 18DD, 0010,0038,01C6,3510,0080,D8EE :38372 J/UNPH1 ; SD_ALU15,SS_SS.XOR.ALU15.XOR.IR1
:38373
:38374 ;11111-----;
:38375 =11111 STATE.STATE.ANDNOT.K[.80], ; EMODH
:38376 LC_RC[6], ; DON'T NORMALIZE 2. OPERAND
:38377 ALU D.OR.LC,D_ALU, ; LATCH LAST PIECE OF MULTIPLIER
U 18DF, 0811,0030,4180,F930,1404,58DD :38378 J/UNPACKH.1 ; OR IN LAST 15 BITS OF MULTIPLIER
:38379 =;END
:38380 =01110
:38381 UNPH1: ;01110-----;
:38382 ALU Q.OXT[WORD].ANDNOT.K[.8000], ;
:38383 RC[6]_ALU, ;
:38384 D_Q, ; D GETS 0LEXP
:38385 CLK.UBCC, ; ACTUALLY NON ZERO
:38386 Q_ID(SC), ; Q GETS 1HOL
:38387 FE_SC, ; FE GETS X, THE NEW OP-POINTER
U 18EE, 0C1B,6025,45F0,25B0,0191,1A64 :38388 CALL,J/UNP.SUBR.2 ; SC GETS -1
:38389
:38390
:38391 =11110 ;11110-----;
U 18FE, 0000,003E,0180,F800,0000,0002 :38392 RETURN2 ;
:38393
:38394 ;RETURN AFTER UNPACKING ALL THE OPERANDS
:38395 =11111 ;11111-----;
:38396 ID(SC) D, ; STORE LOW FRACTION IN ID[3]
U 18FF, 0810,0038,0180,3530,0000,1582 :38397 D_RC[6] ; D GETS EXPONENT 2
:38398 =;END
:38399
:38400 ;-----;
U 1582, 0000,003E,1980,F920,0104,6003 :38401 LC_RC[4], ; LATCH UP EXP1
:38402 FE_K[ZERO], ; NEEDED FOR NABS-FUNCTION
:38403 RETURN3 ;
    
```

```

:38403 :-----:
:38404 =0 :BRANCH ON ALU Z-BIT
:38405 :0-----: OP2 IS NOT ZERO
:38406 UNP.SUBR.2:
:38407 : EXPECTS:
:38408 : D = 0HEXP
:38409 : Q = 1HOL
:38410 : FE = X = ARGUMENT POINTER (.30 OR .32)
:38411 : SC = -1
:38412 : ALU D.ANDNOT.K[.FFFF],D_ALU, : ISOLATE UPPER 16 BITS OF FRACTION
:38413 : FE_SC, : FE GETS -1
:38414 : SC_FE, : SC GETS X
:38415 : Z?, : WAS EXPONENT 0 ?
U 1A64, 0819,0124,C190,F800,0181,1A6C :38416 : J/UNP.SUBR.3
:38417 :
:38418 :1-----: OP2 = 0
:38419 : ALU RC[T2],CHK.FLT.OPR, : CHECK FOR -0
:38420 : Z?,0 [D]EUSTACK], : POP STACK ONCE
U 1A65, 0019,0138,81F0,2D10,0800,1A74 :38421 : J/UNP.SUBR.7
:38422 =:END
:38423 :-----:
:38424 =0 :BRANCH ON ALU Z-BIT
:38425 :0-----:
:38426 : ENTER HERE FROM UNPACK1-ROUTINE
:38427 : EXPECTS: FE = -1
:38428 : SC = X
:38429 UNP.SUBR.3:
:38430 : ALU Q.OXT[WORD].OR.D, : ASSEMBLE 0HOL
:38431 : RC(SC) ALU.RIGHT,SI/MUL-, : SHIFT IN HIDDEN BIT
:38432 : Q_ALU.RIGHT, : IN CASE OF DOUBLE SHIFT
:38433 : D_Q, : D GETS 1HOL
:38434 : STATE7-4?, : TEST NORMALIZE-BIT
U 1A6C, 0C5F,7630,0300,F838,0000,1BE7 :38435 : J/UNP.SUBR.4
:38436 :
:38437 :1-----: OP IS 0
:38438 : ALU_RC(SC), : GET OP1 LONG EXP
:38439 : CHK.FLT.OPR, : CHECK FOR -0
U 1A6D, 0010,003A,0180,F830,0800,0010 :38440 : RETURN[10]
:38441 =:END
:38442 :-----:
:38443 =0111 :BRANCH ON STATE<7>
:38444 :0111-----:
:38445 UNP.SUBR.4:ALU_Q,RC(SC)_ALU.RIGHT, : STORE OHOL (SHIFTED TWICE)
:38446 : SI/MUL+, : SHIFT IN OVERFLOW-BIT
:38447 : SC_FE, : SC GETS -1
:38448 : FE_SC+1, : FE GETS X+1
U 1BE7, 0041,203C,0300,F838,0181,D583 :38449 : J/UNP.SUBR.5
:38450 :
:38451 :1111-----:
:38452 : SC_SC+1, : SC GETS X+1, FE STAYS AT -1
:38453 : ALU D.ANDNOT.K[.FFFF],D_ALU, : D GETS 1H
U 1BEF, 0819,0024,C180,F800,0080,D584 :38454 : J/UNP.SUBR.6
:38455 =:END
  
```

	:38456	:	:
	:38457	UNP.SUBR.5:SC_FE,	: SC GETS X+1
	:38458	FE_SC+K[.FFFF],	: FE GETS -2
U 1583, 0819,0024,C180,F800,0185,9584	:38459	ALU_D.ANDNOT.K[.FFFF],D_ALU	: D GETS 1H
	:38460	:	:
	:38461	:	:
	:38462	UNP.SUBR.6:Q_RC(SC),	: Q GETS 2H1L
U 1584, 0010,0038,05C0,F830,0084,8585	:38463	SC_SC-K[.1]	: SC GETS X
	:38464	:	:
	:38465	:	:
	:38466	ALU_Q.OXT[WORD].OR.D,	: ASSEMBLE 1L WITH 1H
	:38467	D_ALU,	: D GETS 1H1L
	:38468	Q_ID(SC),	: Q GETS 1H0L
U 1585, 081F,6030,01F0,2400,0181,1586	:38469	FE_SC,	: FE GETS X
	:38470	SC_FE	: SC GETS -1 OR -2
	:38471	:	:
	:38472	:	:
	:38473	D_DAL.SC,	: SHIFT 1H1L RIGHT
	:38474	ID[T9]_D,	: SAVE 1H1L IN T9
U 1586, 0D10,0038,E5C0,3C00,0181,1588	:38475	Q_LC,	: Q GETS 2H1L
	:38476	SC_FE,FE_SC	: SC GETS X, FE GETS -1 OR -2
	:38477	:	:
	:38478	:	:
	:38479	ID(SC) D,	: STORE 1H1L (SHIFTED)
	:38480	ALU_Q.ANDNOT.K[.FFFF],	: ISOLATE 2H
U 1588, 0819,2024,C180,3400,0080,D58A	:38481	D_ALU,	: D GETS 2H
	:38482	SC_SC+1	: SC GETS X+1
	:38483	:	:
U 158A, 0000,003C,01F0,2400,0000,158C	:38484	:	:
	:38485	Q_ID(SC)	: Q GETS 3H2L
	:38486	:	:
	:38487	:	:
	:38488	ALU_Q.OXT[WORD].OR.D,D_ALU,	:
U 158C, 081F,6030,E5F0,2C00,0181,158E	:38489	Q_ID[T9],	: Q GETS 1H1L
	:38490	SC_FE,FE_SC	: SC GETS X+1, FE GETS -1 OR -2
	:38491	:	:
	:38492	:	:
	:38493	ID[T9]_D,	: SAVE 2H2L IN T9
	:38494	D_DAL.SC,	: D GETS 2H2L (SHIFTED)
U 158E, 0D00,003C,E5E0,3C00,0181,1590	:38495	Q_D,	: Q GETS 2H2L
	:38496	SC_FE,FE_SC	: SC GETS -1 OR -2, FE GETS X+1
	:38497	:	:
	:38498	:	:
U 1590, 0C01,003C,01F0,2438,0000,1591	:38499	RC(SC) D,	: STORE 2H2L (SHIFTED)
	:38500	D_Q,Q_ID(SC)	: Q GETS 3H2L
	:38501	:	:
	:38502	:	:
	:38503	FE_SC,SC_FE,	: SC GETS -1 OR -2
U 1591, 0819,2024,C1E0,F800,0181,1592	:38504	ALU_Q.ANDNOT.K[.FFFF],D_ALU,	:
	:38505	Q_D	: Q GETS 2H2L
	:38506	:	:

```

:38507 :-----:
:38508 D DAL.SC,
:38509 SC FE, : SC GETS X+1
:38510 FE_K[.FFFF], : FE GETS -1
:38511 STATE1? : BRANCH ON EMDH-BIT
U 1592, 0D00,173E,C180,F800,0185,6011 :38512 RETURN[11]
:38513
:38514 :-----:
:38515 =0 : BRANCH ON ALU Z-BIT
:38516 :0
U 1A74, 0000,003E,0180,F800,0000,0002 :38517 UNP.SUBR.7:RETURN2 : OP2 = 0, OP1 NE 0
:38518
:38519 :1-----:
:38520 ALU RC[T0],CHK.FLT.OPR, : CHECK FOR -0
U 1A75, 0010,005A,0180,F900,0800,0004 :38521 RETURN4 : BOTH OPERANDS ARE 0
:38522 =:END ;

```

```

:38523 .TOC      "      G & H floating point : H-FORMAT FLOATING PACK-ROUTINE"
:38524
:38525 :INPUTS:
:38526          RCO-IDT1 = DST, ROUNDED AND SHIFTED LEFT ONE BIT BEYOND
:38527          NORMALIZATION I.E. THE HIDDEN BIT IS ALREADY
:38528          LEFT OF THE MSB.
:38529          ALU CARRY TELLS WHETHER THIS
:38530          RESULTED IN A CARRY OUT OF THE LEADING DIGIT
:38531          LC = RC6 = DST EXPONENT, BIASED
:38532          ENTER WHILE BRANCHING ON ALU CARRY
:38533 :OUTPUTS:
:38534          RCO-ID1 = PACKED H FORMAT EXPONENT
:38535          RC6 = DST EXPONENT, BIASED
:38536          CHECKS FOR OVERFLOW AND UNDERFLOW
:38537 :RETURN:
:38538          RETURN10
:38539
:38540 -----;
:38541 =0*      ;BRANCH ON C31
:38542          ;-----;
:38543 PACKH:  D_RC[1],      ; NO CARRY
:38544          Q_ID[1],      ; D GETS 2H2L
:38545          J7PACKH.1     ; Q GETS 3H3L
:38546
:38547          ;1*-----;
:38548          ALU_0+LC+1,RC[6]_ALU, ; CARRY PROPAGATED ALL THE WAY
:38549          CLK_UBCC,J/PACKH    ; INCREMENT EXPONENT
:38550 =;END
:38551 PACKH.1:-----;
:38552          ALU_Q.ANDNOT.K[.FFFF], ; NOW WE PACK FRACTION WORDS TOGETHER.
:38553          Q_ALU                ; ISOLATE HIGH 16 FRACTION BITS
:38554                          ; Q GETS 3H00
:38555
:38556          ;-----;
:38557          ALU_D.OXT[WORD].OR.Q,  ; ASSEMBLE LONG FRAC1
:38558          D_ALU,                ; D GETS 3H2L
:38559          Q_ID[0]                ; Q GETS 1H1L
:38560
:38561          ;-----;
:38562          ID[1]_D,                ; WRITE LONG FRAC3, 3H2L
:38563          D_Q,                  ; D GETS 1H1L
:38564          Q_RC[1]                ; Q GETS 2H2L
:38565
:38566          ;-----;
:38567          ALU_Q.ANDNOT.K[.FFFF],Q_ALU ; Q GETS 2H00
:38568
:38569          ;-----;
:38570          ALU_D.OXT[WORD].OR.Q,  ; ASSEMBLE 2H1L
:38571          RC[1]_ALU            ; STORE IT IN RC1
:38572
:38573          ;-----;
:38574          Q_D,                  ; Q GETS 1H1L
:38575          D_RC[0]                ; D GETS 0H0L
:38576
:38577          ;-----;
:38578          ALU_Q.ANDNOT.K[.FFFF],Q_ALU ; Q GETS 1H00
    
```

U 1A80, 0810,0038,C5F0,2D08,0000,1593

U 1A82, 0013,0010,0180,F9B0,0010,1A80

U 1593, 0019,2024,C1C0,F800,0000,1594

U 1594, 081F,4030,C1F0,2C00,0000,1595

U 1595, 0C10,0038,C5C0,3D08,0000,1596

U 1596, 0019,2024,C1C0,F800,0000,1598

U 1598, 001F,4030,0180,F988,0000,1599

U 1599, 0810,0038,01E0,F900,0000,159A

U 159A, 0019,2024,C1C0,F800,0000,159B

```

:38578
:38579 ALU_D.OXT[WORD].OR.Q,D_ALU, : D GETS 1HOL
U 159B, 081F,4030,01E0,F800,0000,159C :38580 Q_D : Q GETS 0HOL
:38581
:38582
:38583 ID[TO] D,
:38584 D RC[TO], : D GETS BIASSED EXPONENT
U 159C, 0810,5238,C180,3D30,0010,1BFE :38585 CLK.UBCC,WORD, : CLOCK ALU-N-BIT ON BIT15
:38586 EALU? : TEST SIGN-BIT
:38587
:38588
:38589 =1110 : BRANCH ON SS-FF
:38590 :1110
:38591 PACKH.2:ALU Q.ANDNOT.K[.FFFF],Q_ALU, : Q GETS 0H00
U 1BFE, 0019,3724,C1C0,F800,0000,1597 :38592 STATE3?,J/PACKH.3 : BRANCH ON STATE3
:38593
:38594 :1111
:38595 ALU D.OR.K[.8000],D_ALU, : NEGATIVE
U 1BFF, 0819,0030,4580,F800,0000,1BFE :38596 J/PACKH.2 : OR SIGN-BIT INTO EXP
:38597 =;END
:38598
:38599 =0111 : BRANCH ON STATE3
:38600 :1110
U 1597, 0000,0D3C,0180,F800,0000,18E6 :38601 PACKH.3:SIGNS?,J/PACKH.3A : NOT POLYH,CONTINUE
:38602 : BRANCH ON EXP<31>
:38603 :1111
U 159F, 0000,0D3C,0180,F800,0000,19D6 :38604 SIGNS?,J/POLYH.X : POLYH
:38605
:38606
:38607 : BRANCH ON D<31>
:38608 =110 :110
:38609 PACKH.3A:ALU D.OXT[WORD].OR.Q, : ASSEMBLE LONG EXP
U 18E6, 081F,5B30,0180,F980,0000,15A3 :38610 RC[TO] ALU,D_ALU, : STORE IT IN RCO
:38611 ALU?,J7PACKH.4 : TEST FOR OVERFLOW
:38612
:38613 :111
:38614 Q_ID[PSL], : UNDERFLOW
U 18E7, 0F03,003C,3DF0,2D80,0000,15B5 :38615 D_0,ALU 0(A),RC[TO]_ALU, : GET PSL TO TEST FU-BIT
:38616 J7FL.UNDER
:38617 =;END

```



```

:38618 :-----:
:38619 =0011 : BRANCH ON ALU N-BIT
:38620 :0011 : NO OVERFLOW
:38621 PACKH.4:ALU,RC[0],N&Z_ALU, :
:38622 WORD, : CLOCK N AND Z ON RESULT
U 15A3, 0010,403A,0180,F900,0060,0010 :38623 RETURN10
:38624 :
:38625 :0111 : UNDERFLOW
:38626 Q_ID[PSL], : GET PSL TO TEST FU-BIT
U 15A7, 0F03,003C,3DF0,2D80,0000,15B5 :38627 D_0,ALU 0(A),RC[0]_ALU, : MAKE THINGS ZERO
:38628 J7FL.UNDER : TAKE FAULT
:38629 :
:38630 :1011 : OVERFLOW
:38631 RC[7]_K[.8], : RCT7 GETS OVERFLOW FAULT CODE
U 15AB, 0018,0038,0180,F9B8,0000,12B4 :38632 J/FLOAT.FAULT
:38633 =:END
:38634 =0101 :0101 :
U 15B5, 0003,003D,C180,3D88,0000,12AE :38635 FL.UNDER:RC[1]_ALU,ALU_0(A),ID[0]_D, : MAKE MORE THINGS ZERO
:38636 CALL[PS[FU.A] : SEE IF FU-BIT IS SET
:38637 :
:38638 =1101 :1101 : FU NOT SET IGNORE UNDERFLOW
:38639 ALU 0(A),N&Z_ALU, :
U 15BD, 0003,003E,C5F8,3C00,0060,0010 :38640 ID[1]_D,Q_0,RETURN10 : SET THINGS TO ZERO
:38641 :
:38642 :1111 : FU SET TAKE FAULT
U 15BF, 0018,0038,F580,F9B8,0000,12B4 :38643 RC[7]_K[.A],J/FLOAT.FAULT :
    
```

```

:38644 .TOC " G & H floating point : H-FORMAT FLOATING ADD AND SUBTRACT"
:38645
:38646 :HERE FOR *--* AND *-MEMORY
:38647 :ENTER HERE WITH SRC OPND IN RC0-ID1
:38648 :AND DST OPND IN RC2-ID3
:38649
:38650 148A:
:38651 STATE_K[ZERO], ; FIND SOMETHING BETTER TO DO
U 148A, 0000,003D,1980,F800,1404,7950 :38652 CALL,J/ADDH.ROUTINE ; CALL ADD H-FORMAT SUBR.
:38653
:38654 149A: ;-----;
U 149A, F000,003F,01F0,F847,0000,1400 :38655 WRITE.G.DEST,J/WRG
:38656 =:END
:38657
:38658 :HERE FOR *-REG
:38659 :ENTER WITH SRC-OPERAND IN RC0-ID1
:38660 :AND WITH DST-OPND IN LA,R(PRN),ETC.
:38661
:38662 ;-----;
:38663 142E: RC[2] LA, ; RC2 GET OP2 LONG EXP
:38664 K[.80], ; CONSTANT FOR FINDING REG #
U 142E, 0F00,003C,4180,F990,0000,186E :38665 D_0 ; NEEDED FOR REG-ROUTINE
:38666
:38667 ;0*11*-----;
U 186E, 0000,003D,0180,F800,0000,1862 :38668 =0*11* CALL,J/HUGE.REG.READ.1 ; READ 2. OPERAND
:38669
:38670 ;-----;
U 187E, 0000,003C,1980,F800,1404,7A21 :38671 STATE_K[ZERO] ; NOTHING TO DO
:38672 =:END
:38673 ;0****-----;
U 1A21, 0000,003D,0180,F800,0000,1950 :38674 =0**** CALL,J/ADDH.ROUTINE ; CALL ROUTINE FOR ADDING
:38675
:38676 ;1****-----;
:38677 TRAP.AC[1], ; RESET THE ACCELLARATOR
U 1A31, 0810,00B8,0080,F900,0000,18D4 :38678 D_RC[0], ; D GETS RESULT LONG EXP
:38679 J7HUGE.REG.WRITE.1 ; STORE RESULT
:38680 =:END ;-----;
  
```

```

:38681 =000 :000-----:
:38682 ADDH.ROUTINE:
:38683 CLR.SD&SS, : INITIALIZE SS AND SD
:38684 ALU RC[T0],N&Z,ALU.V&C_0,WORD, : CLEAR V AND C OF PSL
U 1950, 0010,4039,0187,F900,0050,157B :38685 CALL,J/UNPACKH
:38686
:38687 : RETURN WITH RC2-ID3 CONTAINING DESTINATION
:38688 : IN PACKED FORM
:38689 =001 :001-----: SRC = 0
:38690 ALU RC[T2],N&Z,ALU.V&C_0,WORD, : SET CONDITON CODES ON DST
:38691 D,ALU,Q_ID[T2], : D GETS LONG EXP, Q GETS LONG FRAC1
U 1951, 0810,4038,C9F0,2D10,0050,1636 :38692 J7SHIFT.H
:38693
:38694 :RETURN WITH RCO-ID1 CONTAINING SRC IN PACKED FORM.
:38695 :010-----: DST = 0
:38696 =010 D RC[T0], : D GETS SRC LONG EXP
U 1952, 0810,0938,0180,F900,0000,1822 :38697 IR?, J/ADDG.8 : TEST FOR ADD OR SUBTRACT
:38698
:38699 :RETURN WITH:
:38700 : D=EXP2
:38701 : LC=EXP1
:38702
:38703 =011 :011-----: BOTH OPERANDS NON ZERO
:38704 ADDH.00: : ENTER HERE FROM POLYH
:38705 ALU_D-LC,R[R15]_ALU, : GENERATE EXP2-EXP1
:38706 CLK,UBCC, : CLOCK IT
:38707 SC,ALU, :
:38708 FE_K[ZERO], : USE IN NABS-FUNCTION BELOW
U 1953, 0011,0000,1980,FAF8,0196,759D :38709 J/ADDH.01
:38710
:38711 : BOTH OPERANDS ARE 0
:38712 : CLEAR OUT DIRTY 0'S
:38713 =100 :100-----:
:38714 ALU_0(A),N&Z,ALU.V&C_0, : SET PSL Z-BIT
U 1954, 0F03,003C,79F8,F800,00D4,7632 :38715 D_0,Q_0,SC_K[.30],
:38716 J7CLEAR.DIRTY.0
:38717 =;END
:38718
:38719 ADDH.01:FE NABS(SC-FE), : FE GETS NABS OF EXP DIFFERENCE
:38720 ALU_K[.30],SC,ALU, : FOR POINTING TO OPERANDS
:38721 LAB,R[R15], : LATCH EXPONENT DIFFERENCE
U 159D, 0018,1B38,7980,FA78,0182,F5C3 :38722 ALU?,J/ADDH.10 : TEST RESULT OF EXP2-EXP1
:38723

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:38724 =0011 ; BRANCH ON ALU Z AND N-BITS
:38725 ;:0011-----:
:38726 ADDH.10:SC SC.OR.K[.1], ; ALIGN SRC-OPERAND
:38727 D 0, ; INITIALIZE FILLER
:38728 EALU?,
:38729 J/ADDH.100
:38730
:38731 ;:0111-----:
:38732 SC SC.OR.K[.1], ; NEGATE SRC IF ANY
:38733 ALD -1,D ALU, ; D GETS FILLER
:38734 EALD?,J/ADDH.EQUAL ; EXPONENTS ARE EQUAL
:38735
:38736 ;:1011-----:
:38737 ALU_0-LB,R[R15]_ALU, ; NEGATE EXP DIFFERENCE
:38738 D 0, ; INITIALIZE FILLER
:38739 SC SC.OR.K[.3], ; ALIGN DST-OPERAND
:38740 EALU? ; TEST FOR ADD OR SUBTRACT
:38741 =:END
:38742 ;-----:
:38743 =1110 ; BRANCH ON SS-FLIP FLOP
:38744 ;:1110-----:
:38745 ALU LC,RC[6]_ALU, ; RC6 GETS LARGEST EXP
:38746 J/ADDH.100
:38747
:38748 ;:1111-----:
:38749 ALU LC,RC[6]_ALU, ; RC6 GETS LARGEST EXP
:38750 SGN/NOT.SD, ; SUBTRACT, SO COMPLEMENT SIGN
:38751 J/ADDH.101
:38752 =:END
  
```

U 15C3, 0F00,123C,0580,F800,0084,388E

U 15C7, 0803,1228,0580,F800,0084,3846

U 15CB, 0F0F,1200,0D80,FAF8,0084,348E

U 148E, 0010,0038,0180,F9B0,0000,188E

U 148F, 0010,0038,0183,F9B0,0000,188F

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:38753 -----;
:38754 =001110 :BRANCH ON SS
:38755 :001110 -----; ADD
U 188E, 0001,003D,E580,3DA0,0000,15C4 :38756 ADDH.100:ID[T9] D, ; T9 GETS 0 OR -1
:38757 ALU D,RC[T4] ALU,
:38758 CALL,J/ALNPOSH
:38759 -----;
:38760 =001111 :001111 -----; SUBTRACT
:38761 ADDH.101:Q_ID(SC), ; GET LOWEST FRACTION BITS
:38762 LC_RC(SC), ; AND THE NEXT LOWEST ONES
U 188F, 0000,003D,05F0,2430,0084,B5C1 :38763 SC_SC-K[.1], ; DECREMENT POINTER
:38764 CALL,J/ALNNEGH ; DOES A RETURN10
:38765 -----;
:38766 :RETURN WITH :
:38767 :
:38768 : RCO-ID3 ARE THE ALIGNED OPERANDS
:38769 -----;
U 189E, 0013,0015,0D80,F800,0094,359E :38770 ADDH.SUBR.0:SC_SC.OR.K[.3], ; SC GETS .33
:38771 ALU 0+[C,CLK.UBCC, ; CLEAR ALU CARRY
:38772 CALL,J/ADDH.SUBR ; DOES A RETURN20
:38773 -----;
:38774 : RETURN FROM NEGATING SMALLEST NUMBER
:38775 : WITH: D = -1, THE FILLER CHARACTER
:38776 : SC = POINTER TO MS FRACTION
:38777 =011111 :011111 -----;
U 189F, 0000,003C,0580,F800,0084,388E :38778 SC_SC.OR.K[.1], ; POINT TO FRACTIONS <LS>
:38779 J/ADDH.100 ; ALIGN FRACTION
:38780 -----;
:38781 =111110 : RETURN FROM ADDH.SUBR
:38782 :111110 -----;
U 18BE, 0000,003C,1980,F800,0084,75A5 :38783 SC_K[ZERO], ; INITIALIZE SHIFT-COUNT
:38784 J/ADDH.310
:38785 =:END ;
    
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:38786 ; ENTER HERE IF EXPONENTS ARE EQUAL
:38787 ; NO ALIGNMENT IS NECESSARY
:38788
:38789 =00*110 ; BRANCH ON SS-FF
:38790 ;00*110-----;
U 1846, 0000,003C,E580,3C00,0000,189E :38791 ADDH.EQUAL:ID[T9]_D,J/ADDH.SUBR.0
:38792
:38793 ;00*111-----;
:38794 Q_ID(SC), ; GET LOWEST FRACTION BITS
:38795 LC_RC(SC), ; AND THE NEXT LOWEST ONES
:38796 SC_SC-KC.1], ; DECREMENT POINTER
:38797 CALL,J/ALNNEG
:38798
:38799 ; RETURN WITH RC[T0]-ID[T1] NEGATED
:38800 ; SC = .30
:38801 =01*111 ;01*111-----;
:38802 SC_SC.OR.KC.3], ; MAKE SC = .33
:38803 ALD 0+LC,CLK.UBCC, ; CLEAR ALU CARRY
U 1857, 0013,0015,0D80,F800,0094,359E :38804 CALL,J/ADDH.SUBR
:38805
:38806 ;11*111-----;
:38807 =11*111 SC_KC.30], ; POINT TO RC0-ID1
:38808 LC_RC[T1],
:38809 C3T? ; TEST FOR BORROW
:38810 =;END
:38811 ;0**0*-----;
:38812 =0**0* LC_RC[T1],
:38813 SGN/NOT.SD, ; COMPLEMENT DST-SIGN
:38814 Q_ID[T1],
U 18E0, 0000,003D,C5F3,2D08,0000,15C1 :38815 CALL,J/ALNNEG
:38816
:38817 ;0**1*-----;
:38818 =0**1* SC_KC[ZERO], ; INITIALIZE SHIFT-COUNT
:38819 J/ADDH.310
:38820
:38821 ;1**0*-----;
U 18F0, 0000,003C,1980,F800,0084,75A5 :38822 =1**0* SC_KC[ZERO],J/ADDH.310 ;RETURN10 FROM ALNNEG-Routine
:38823 =;END ;-----;

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:38824 ADDH.SUBR:
:38825 :EXPECTS:
:38826 : RCO-ID3 ARE THE ALIGNED OPERANDS
:38827 : SC = .33 OR .31
:38828 : ALU CARRY MUST BE CLEAR
:38829 :
:38830 : RETURN20
:38831 :
:38832 :-----:
U 159E, 0000,003C,3180,F800,1404.55A0 :38833 STATE_STATE.ANDNOT.K[.40] : CLEAR BIT 6 OF STATE
:38834 :-----:
:38835 :
:38836 ADDH.SUBR.1:
:38837 Q_ID(SC), : GET LOWER FRACTION (1 OP 3)
:38838 D_RC(SC), : NEXT HIGHER FRACTION
U 15A0, 0810,0038,09F0,2430,0084,B5A1 :38839 SC_SC-K[.2] : POINT TO OP1
:38840 :
:38841 :-----:
:38842 R[R15]_D, : STORE IT IN R15
:38843 D_Q, : D GETS OP2 FRACTION
U 15A1, 0C01,033C,01F0,26F8,0000,1A81 :38844 Q_ID(SC), : Q GETS OP1 LOWER FRACTION
:38845 C31? : CARRY ?
:38846 :
:38847 :-----:
:38848 =0* :BRANCH ON ALU C31
:38849 :0*-----:
:38850 D_D+Q, : ADD LOW FRACTION PARTS
:38851 LAB_R[R15], : LATCH FRACTION PART
U 1A81, 081D,0014,0180,FA78,0010,15A2 :38852 CLK_UBCC, : CLOCK CARRY IF ANY
:38853 J/ADDH.13
:38854 :
:38855 :1*-----:
:38856 D_D+Q+1, : ADD LOW FRACTION PARTS
:38857 LAB_R[R15], : LATCH FRACTION PART
U 1A83, 081D,0010,0180,FA78,0010,15A2 :38858 CLK_UBCC, : CLOCK CARRY IF ANY
:38859 =:END :-----:

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:38860 ADDH.13:
:38861 FE_K[.60], : FOR USE LATER ON
:38862 ID(SC) D, : STORE RESULT IN OP1 LOCATION
:38863 LC_RC(SC), : LATCH UP HIGHER FRACTION
:38864 C3T? : WAS THERE A CARRY ?
:38865
:38866 -----:
:38867 =0* :BRANCH ON ALU CARRY
:38868 :0*-----:
:38869 ALU_LA+LC, RC(SC)_ALU, : ADD HIGHER FRACTIONS TOGETHER
:38870 CLK_UBCC, : CLOCK CARRY IF ANY
:38871 STATE_STATE.OR.K[.40], : SET FIRST PASS BIT
:38872 STATE7-4?,J/ADDH.14
:38873
:38874 :1*-----:
:38875 ALU_LA+LC+1, RC(SC)_ALU, : ADD HIGHER FRACTIONS TOGETHER
:38876 CLK_UBCC, : CLOCK CARRY IF ANY
:38877 STATE_STATE.OR.K[.40], : SET FIRST PASS BIT
:38878 STATE7-4?,J/ADDH.14
:38879
:38880 -----:
:38881 =1011 :BRANCH ON STATE<6>
:38882 :1011-----:
:38883 ADDH.14:SC_SC+1,J/ADDH.SUBR.1 : NOW ADD TWO MOST SIGNIF. FRACS
:38884
:38885 :1111-----:
:38886 STATE_STATE.ANDNOT.K[.40] : ADDITION COMPLETE
:38887 : : CLEAR BIT 6 OF STATE
:38888
:38889 -----:
:38890 SC_K[ZERO],RETURN[20]
:38891

```

U 15A2, 0000,033C,A580,3430,0104,7A88

U 1A88, 0010,1614,3180,F838,1414,35DB

U 1A8A, 0010,1610,3180,F838,1414,35DB

U 15DB, 0000,003C,0180,F800,0080,D5A0

U 15DF, 0000,003C,3180,F800,1404,55A4

U 15A4, 0000,003E,1980,F800,0084,6020


```

:38891 ADDH.310:
:38892 : ENTER HERE TO NORMALIZE, ROUND AND PACK H-FORMAT
:38893 : EXPECTS:
:38894 : RC0-ID1 = NEW FRACTION, MAY BE UNNORMALIZED
:38895 : RC[6] = BIASSED EXPONENT
:38896 : SC = 0
:38897 : SD = DST-SIGN
:38898 -----;
:38899 FE KC.60],
:38900 SGV/SS.FROM.SD, : LOAD SS WITH DEST-SIGN
U 15A5, 0810,0038,A582,F900,0114,75A6 :38901 D_RC[6],CLK.UBCC ; CLOCK FRAC 0
:38902 -----;
:38903
:38904 ADDH.311:LC RC[6], : GET READY TO ADJUST EXP
:38905 Q_ID[0], : GET FRAC1
U 15A6, 0000,013C,C1F0,2D30,0010,BA7C :38906 EALU_SC-FE,CLK.UBCC, : CLOCK NORMALIZE COUNT
:38907 Z? : FIRST LONGWORD 0 ?
:38908 -----;
:38909
:38910 =0 :BRANCH ON ALU Z-BIT
:38911 0-----;
U 1A7C, 0000,003C,0180,F800,008C,95AA :38912 SC_SC+SHF.VAL, : SC GETS NORMALIZE COUNT
:38913 J/ADDH.36
:38914 -----;
:38915 :1-----;
:38916 SC_SC+KC.20], : ONE MORE LONGWORD
U 1A7D, 0001,323C,7580,F980,0094,95EB :38917 RC[0]_Q,CLK.UBCC, : CLOCK LEADING FRACTION BIT
:38918 EALU? : IS IT ALL 0 ?
:38919 =:END
:38920 -----;
:38921 =1011 :BRANCH ON EALU Z-BIT
:38922 :1011-----;
U 15EB, 0810,0038,C5F0,2D08,C000,15A8 :38923 D_RC[1],Q_ID[1], : GET NEXT TWO FRACTION WORDS
:38924 J7ADDH.312
:38925 -----;
:38926 :1111-----;
:38927 ALU 0(A),N&Z_ALU, : ALL FRACTION WORDS ARE 0
:38928 RC[0]_ALU,D_0,Q_0, : RESULT IS 0
U 15EF, 0F03,003C,79F8,F980,00E4,7632 :38929 SC KC.30],
:38930 J/CLEAR DIRTY.0 ; RETURN10 FROM THAT ROUTINE
:38931 =:END
:38932 -----;
:38933 ADDH.312:
:38934 ID[0]_D, : WRITE FRAC1
U 15A8, 0F01,203C,C180,3D88,0000,15A9 :38935 RC[1]_Q, : WRITE FRAC2
:38936 D_0
:38937 -----;
:38938
:38939 ID[1]_D, : WRITE FRAC3
U 15A9, 0810,0038,C580,3000,0000,15A6 :38940 D_RC[0], : GET FRAC1
:38941 J7ADDH.311
:38942 -----;
    
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:38943 : ENTER HERE AFTER FINDING NON-ZFRO LONGWORD IN RESULT.  
:38944 : RC[0] CONTAINS THAT LONGWORD.  
:38945 : SC CONTAINS TOTAL NUMBER OF LEADING 0-BITS IN RESULT.  
:38946 : THIS ROUTINE SHIFTS THIS FRACTION ONE BIT BEYOND NORMALIZING,  
:38947 : I.E. THE HIDDEN BIT IS NO LONGER WITH US AFTER THIS.  
:38948 : EXPONENT IN RC6 IS ADJUSTED BY SC, TO REFLECT NORMALIZE-PROCESS  
:38949 :-----:-----:  
U 15AA, 001B,0000,1DC0,F930,0080,D5AD :38950 ADDH.36:SC SC+1, : WE WANT TO ADJUST BEYOND HIDDEN BIT  
:38951 ALU 0-K[SC],Q_ALU, : Q GETS NEGATIVE ADJUSTMENT  
:38952 LC_RC[6] : LATCH EXP  
:38953 :-----:-----:  
U 15AD, 0000,003C,A180,F800,0014,55B0 :38954 : :  
:38955 EALU SC.ANDNOT.K[.FFE0], : ISOLATE LOW FIVE BITS  
:38956 CLK.DBCC : TEST FOR ALIGNMENT OF 32.  
:38957 :-----:-----:  
U 15B0, C011,3210,C1F0,2DB0,0000,15FB :38958 : :  
:38959 ALU_Q+LC+1,RC[6]_ALU, : RC6 HAS CORRECT BIASED EXP.  
:38960 : EXCEPT FOR ROUND  
:38961 Q_ID[0], : Q GETS FRAC <AMS>  
:38962 EALU? : TEST FOR ALIGNMENT OF 32.  
:38963 :-----:-----:  
U 15FB, 0D00,003C,0180,F800,0000,15B1 :38964 : :  
:38965 =1011 : BRANCH ON EALU Z-BIT  
:38966 :1011 : :  
:38967 D_DAL.SC,J/ADDH.361 : NORMALIZE FIRST PART  
:38968 :-----:-----:  
U 15FF, 0C00,003C,4D80,F800,0084,35B1 :38969 : :  
:38970 :1111 : :  
:38971 SC.SC.OR.K[.FF00], : SHIFTCOUNT OF -32.  
:38972 D_Q : :  
:38973 :-----:-----:  
U 15B1, 0C01,003C,0180,F980,0000,15B2 :38974 ADDH.361:RC[0]_D,D_Q  
:38975 : :  
:38976 :-----:-----:  
U 15B2, 0010,0038,01C0,F908,0000,15B3 :38977 Q_RC[1]  
:38978 : :  
:38979 :-----:-----:  
U 15B3, 0D00,003C,C5F0,2C00,0000,15B4 :38980 D_DAL.SC,Q_ID[1]  
:38981 : :  
:38982 :-----:-----:  
U 15B4, 0810,0038,C180,3D08,0000,15B8 :38983 ID[0]_D,D_RC[1]  
:38984 : :  
:38985 :-----:-----:  
U 15B8, 0D00,003C,0180,F800,0000,15B9 :38986 D_DAL.SC  
:38987 : :  
:38988 :-----:-----:  
U 15B9, 0C01,003C,01F8,F988,0000,15BA :38989 RC[1]_D,D_Q,Q_0  
:38990 : :  
:38991 :-----:-----:  
U 15BA, 0D10,0038,45C0,F908,0000,15BB :38992 ADDH.37:D_DAL.SC, : LEFT ADJUST LOW FRACTION PART  
:38993 Q_RC[1], : Q GETS FRAC2  
:38994 K[.8000]  
:38995 :-----:-----:
```

```
:38996 : ENTER HERE FROM MULH-ROUTINE.  
:38997 : THIS ROUTINE ROUNDS THE ALREADY NORMALIZED FRACTION.  
:38998 : EXITS TO PACK H-FORMAT ROUTINE, WHICH DOES A RETURN10  
:38999 : EXPECTS:  
:39000 : RC0-ID1 = FRACTION LEFT-ADJUSTED, ONE BIT BEYOND NORMALIZATION  
:39001 : RC6 = BIASSED EXPONENT  
:39002 : D = DST FRAC3 (UNROUNDED)  
:39003 : Q = DST FRAC2  
:39004 : SLOW CONSTANT .8000 HAS BEEN SELECTED ONCE ALREADY.  
:39005 : SD = SS = DEST-SIGN  
:39006  
:39007 ADDH.380:-----: ROUND LOW FRACTION PART  
:39008 D,D+K[.8000], :  
:39009 LC,RC[10], :  
U 158E, 0819,0014,4580,F900,0010,15BC :39010 CLR,UBCC :  
:39011  
:39012 ADDH.39:-----: ADD TO NEXT FRACTION WORD  
:39013 ID[1] D, :  
:39014 ALU_0+Q+1,Q_ALU, :  
U 158C, 001F,0310,C5C0,3C00,0010,1A89 :39015 CLK,UBCC, :  
:39016 C31? :  
:39017  
:39018 :-----: :  
:39019 =0* :BRANCH ON ALU C31 :  
:39020 :0* :-----: :  
U 1A89, 0000,003C,0180,F930,0000,1A80 :39021 LC,RC[6],J/PACKH :  
:39022  
:39023 :1*-----: :  
:39024 ALU_Q,RC[1]_ALU, :  
:39025 Q_ID[10], :  
U 1A8B, 0001,233C,C1F0,2D88,0000,1A90 :39026 C31? :  
:39027 =;END :  
:39028 :-----: :  
:39029 =0* :BRANCH ON ALU C31 :  
:39030 :0* :-----: :  
U 1A90, 0000,003C,0180,F930,0000,1A80 :39031 LC,RC[6],J/PACKH :  
:39032  
:39033 :1*-----: :  
:39034 ALU_0+Q+1,D_ALU, :  
:39035 CLK,UBCC :  
U 1A92, 081F,0010,0180,F800,0010,15BE :39036 =;END
```

```

:39037 :-----:
:39038 ID[0] D, : STORE ROUNDED FRAC1
:39039 ALU_0+[C+1,
:39040 Q_D,
:39041 RC[0]_ALU,D_ALU,
:39042 CLK_UBCC,
U 15BE, 0813,0310,C1E0,3D80,0010,1A91 :39043 C31?
:39044
:39045 :-----:
:39046 =0* :BRANCH ON ALU C31
:39047 :0*-----:
:39048 RC[0]_LC,D_ALU,
U 1A91, 0810,0038,0180,F980,0000,15C0 :39049 J/ADDH.390
:39050
:39051 :1*-----:
:39052 Q_RC[6],LC_RC[6], : GET EXPONENT
:39053 C31?,J/PACKH : TEST FOR LEADING CARRY
:39054 =:END
:39055 ADDH.390:-----:
U 15C0, 0000,003C,0180,F930,0000,1A80 :39056 LC_RC[6],J/PACKH
:

```

:39057 : ROUTINE TO NEGATE 4 LONGWORDS, STORED IN RC(SC-),ID(SC),RC(SC+1),ID(SC+1)
:39058 : EXPECTS:
:39059 : LC = RC(SC+1)
:39060 : Q = ID(SC+1)
:39061 :
:39062 : THIS ROUTINE RELIES ON STEVE JENKINS' STATEMENT THAT
:39063 : THE ALU OPERATION A-B-1 WITH A=0,B=FFFFFFF, WILL CAUSE CARRY TO BE CLEARED.
:39064 :
:39065 : ALNNEG:

:39066 :-----:
:39067 : D_0-Q, : NEGATE FRAC <VLS>
:39068 : Q_ID(SC), : GET FRAC <AMS>
:39069 : SC SC+1, : INCREMENT POINTER AGAIN
:39070 : CLR.UBCC
U 15C1, 081F,0000,01F0,2400,0090,D5C2

:39071 :-----:
:39072 : ID(SC) D, : STORE NEGATED FRAC <VLS>
:39073 : RC(SC)-0-LC, : NEGATE FRAC <ALS>
:39074 : CLK.UBCC, :
:39075 : C31? : WAS THERE A BORROW?
:39076 :
:39077 :-----:
:39078 :
:39079 =0* : BRANCH ON ALU C31

:39080 :0* : BORROW
:39081 : ALU_0-LC-1,RC(SC)_ALU, : STORE FRAC <ALS>
:39082 : CLK.UBCC : WE COULD HAVE A BORROW
:39083 :
:39084 :1* : NO BORROW
:39085 : D_0-Q,CLK.UBCC, : NEGATE FRAC <ALS>
:39086 : SC SC-K[.1], : POINT TO <MS> FRACTIONS
:39087 : C31?
U 1A94, 0013,0008,0180,F838,0010,1A96

:39088 =:END
:39089 :-----:
:39090 =0* : BRANCH ON ALU C31
:39091 :0* :
:39092 : D_0-Q-1, : SUBTRACT WITH BORROW
:39093 : LC RC(SC), : LATCH UP FRAC <VMS>
:39094 : CLR.UBCC
U 1A96, 081F,0300,0580,F800,0094,BA98

:39095 :-----:
:39096 :1* :
:39097 : ALU -1,D_ALU, : GET EXTENDER
:39098 : ID(SC) D, : STORE FRAC <ALS>
:39099 : LC RC(SC), : LATCH UP FRAC <VMS>
:39100 : C31?
U 1A9A, 0803,0328,0180,3430,0000,1A99

:39101 =:END
:39102 :-----:
:39103 =0* : BRANCH ON ALU C31
:39104 :0* :
:39105 : ALU_0-LC-1,RC(SC)_ALU, : STORE FRAC <VMS>
:39106 : RETURN[10]
U 1A99, 0013,000A,0180,F838,0000,0010

:39107 :-----:
:39108 :1* :
:39109 : ALU_0-LC,RC(SC)_ALU, : STORE FRAC <VMS>
:39110 : RETURN[10]
U 1A9B, 0013,0002,0180,F838,0000,0010
:39111 =:END :-----:

```
:39112 : ROUTINE TO ALIGN ONE OF THE TWO ADDENDS, TO PREPARE FOR ADD
:39113 : INPUTS:
:39114 :     SC = ARGUMENT POINTER, (31 OR 33)
:39115 :     R15 IS POSITIVE EXPONENT DIFFERENCE
:39116 :     FE = NEGATIVE EXPONENT DIFFERENCE (LOW BITS ONLY)
:39117 :     ID9 = FILLER, EITHER 0 OR -1
:39118 :     IN COMMENTS BELOW, X REFERS TO SC-1, I.E. 30 OR 31
:39119 :
:39120 : OUTPUTS:
:39121 :     SC = X, RC(X), ID(X), RC(X+1), ID(X+1) HAVE ALL BEEN SHIFTED RIGHT
:39122 :
:39123 : RETURN10
:39124 :
:39125 :
:39126 ALNPOSH:
:39127 :-----:
:39128 LAB_R[R15],ALU_LA.ANDNOT,K[.1F],:
:39129 CLK_UBCC : CLOCK ALL BUT LOW 4 BITS
:39130 :
:39131 :-----:
:39132 LAB_R[R15],:
:39133 ALU_LA.ANDNOT,K[.7F],:
:39134 CLK_UBCC, : LATCH POSITIVE EXP DIFF
:39135 Q_ID(SC), : CLOCK ALL BUT LOW 7 BITS
:39136 Z? : GET LOW LONGWORD
:39137 : CHECK SIZE OF SHIFT
:39138 :-----:
:39139 =0 : BRANCH ON ALU Z-BIT
:39140 :0 :
:39141 ALU_LA-K[.20],R[R15]_ALU, : SUBTRACT 32 FROM EXPONENT DIFFERENCE
:39142 CLK_UBCC, LONG, : CLOCK ALU Z-BIT ON NEW DIFFERENCE
:39143 Z?,J/ALNPOSH.1 : TEST FOR SHIFTS > 127
:39144 :
:39145 :1 :-----:
:39146 D_Q,Q_RC(SC), : GET LOW TWO FRACTION PARTS
:39147 SC_FE,FE_SC : GET SHIF? COUNT
:39148 =:END :
:39149 :-----:
:39150 D_DAL.SC, : SHIFT INTO FRAC<VLS>
:39151 SC_FE,FE_SC : SC GETS X+1, FE GETS SHIFT-COUNT
:39152 :
:39153 :-----:
:39154 ID(SC)_D, : STORE FRAC<VLS>
:39155 D_Q, : D GETS OLD FRAC <ALS>
:39156 SC_SC-K[.1] : POINT TO MS FRACTIONS INSTEAD
:39157 :
:39158 :-----:
:39159 Q_ID(SC), : Q GETS FRAC<AMS>
:39160 LC_RC(SC), : LATCH FRAC <VMS>
:39161 SC_FE,FE_SC+1 : SC GETS SHIFT-COUNT, FE GETS X+1
:39162
```

```

:39163
:39164 D_DAL.SC, : SHIFT INTO FRAC <ALS>
U 15CA, 0D00,003C,0180,F800,0181,15CC : SC_FE,FE_SC : SC GETS X+1, FE GETS SHIFT-COUNT
:39165
:39166
:39167
:39168 RC(SC)_D, : STORE FRAC<ALS>
:39169 D_Q, : D GETS FRAC<AMS>
U 15CC, 0C01,003C,0580,F838,0185,B5CE : FE_SC-K[.1], : FE GETS X
:39170 : SC_FE : SC GETS SHIFT-COUNT
:39171
:39172
:39173
:39174 Q_LC : Q GETS FRAC<VMS>
:39175
:39176
:39177 D_DAL.SC, : SHIFT INTO FRAC<AMS>
:39178 SC_FE,FE_SC, : SC GETS X, FE GETS SHIFT-COUNT
U 15D0, 0D00,003C,E5F0,2C00,0181,15D1 : Q_ID[T9] : GET 0 OR -1
:39179
:39180
:39181
:39182 ID(SC)_D, : STORE FRAC<AMS>
:39183 D_LC, : D GETS FRAC<VMS>
U 15D1, 0810,0038,0180,3400,0181,15D2 : SC_FE,FE_SC : SC GETS SHIFT-COUNT, FE GETS X
:39184
:39185
:39186
:39187 D_DAL.SC, : SHIFT INTO FRAC<VMS>
:39188 SC_FE,FE_SC : SC GETS X,FE GETS SHIFT-COUNT
:39189
:39190
:39191 RC(SC)_D,RETURN10 : STORE FRAC<VMS> IN RC(X)
:39192
:39193
:39194 =0 : BRANCH ON ALU Z-BIT
:39195 : 0
:39196 ALNPOSH.1 : ALIGNMENT > 127
U 1A8C, 0000,003C,E5F0,2C00,0000,15D9 : Q_ID[T9], : GET FILLER, -1 OR 0
:39197 : J7ALNPOSH.2
:39198
:39199
:39200 : 1
U 1A8D, 0810,0038,0580,F830,0084,B5D4 : D_RC(SC),SC_SC-K[.1] : 31 < ALIGMENT < 128
:39201
:39202 =;END
:39203
:39204 Q_ID(SC),SC_SC+1,LC_RC(SC)
:39205
:39206
:39207 ID(SC)_D,RC(SC)_Q, : WRITE FRAC3 AND FRAC2
U 15D6, 0001,203C,0580,3438,0084,B5D8 : SC_SC-R[.1]
:39208
:39209

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```

:39210 ;-----;
:39211 D LC ; D GETS FRAC0
:39212 Q-ID[T9], ; Q GETS FILLER
U 15D8, 0810,0138,E5F0,2C00,0000,iA9C :39213 Z? ; TEST NEW ALIGNMENT SHIFT
:39214 ;-----;
:39215 ;-----;
:39216 =0 ; BRANCH ON ALU Z-BIT
:39217 ;-----;
:39218 ID(SC) D,RC(SC) Q, ; WRITE FRAC0 AND FRAC1
:39219 SC SC+T, ; RESTORE ORIGINAL POINTER
U 1A9C, 0001,203C,0180,3438,0080,D5C4 :39220 J/ALNPOSH
:39221 ;-----;
:39222 ; 1-----;
:39223 ID(SC) D,RC(SC) Q, ; WRITE FRAC0 AND FRAC1
:39224 RETURNTO
U 1A9D, 0001,203E,0180,3438,0000,0010 :39225 =:END
:39226 ;-----;
:39227 ALNPOSH.2:D Q, ; D GETS FILLER
:39228 RC(SC) Q ; SO DOES RC(SC)
:39229 ;-----;
:39230 ;-----;
:39231 ID(SC) D, ; FILL WHOLE FRACTION WITH FILLER
:39232 SC SC-R[.1] ; POINT TO MS FRACTIONS
:39233 ;-----;
:39234 ;-----;
:39235 RC(SC) D,
:39236 ID(SC) D,RETURNIO
U 15DC, 0001,003E,0180,3438,0000,0010 :39237 ;-----;

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:39238 .TOC '' G & H floating point : H-FORMAT FLOATING DIVIDE''
:39239
:39240 : DIVH2, *-R
:39241
:39242 :INPUTS:
:39243 : RCO-ID1 = DIVISOR
:39244 : LA = LB = DIVIDEND LONG EXP
:39245
:39246 1429: -----:
:39247 RC[2] LA, : GET DIVIDEND LONG EXP
:39248 K[.80], : FOR READ HUGE ROUTINE
:39249 D 0, :
:39250 CALL,J/HUGE.REG.READ.1 :
:39251
:39252 143F: -----:
:39253 STATE_K[ZERO] : NOTHING TO DO
:39254
:39255 =0**** :0****-----:
:39256 CALL,J/DIVH.SUBR :
:39257
:39258 :1****-----:
:39259 TRAP.ACC[1], : RESET THE ACCEL
:39260 J/HUGE.REG.WRITE.1 :
:39261 =:END ;-----:
:39262
:39263
:39264 : DIVIDE H FORMAT FLOATING
:39265 : ENTER HERE FOR *-MEMORY, AND *-*-
:39266
:39267 :INPUTS:
:39268 : RCO-ID1 = DIVISOR
:39269 : RC2-ID3 = DIVIDEND
:39270
:39271 148B: -----:
:39272 STATE_K[ZERO], : NEED THIS FOR UNPACKH-ROUTINE
:39273 CALL,J/DIVH.SUBR :
:39274
:39275
:39276 149B: -----:
:39277 WRITE.G.DEST :

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U 1429, 0F00,003D,4180,F990,0000,1862

U 143F, 0000,003C,1980,F800,1404,7AA0

U 1AA0, 0000,003D,0180,F800,0000,1960

U 1AB0, 0000,00BC,0080,F800,0000,18D4

U 148B, 0000,003D,1980,F800,1404,7960

U 149B, F000,003F,01F0,F847,0000,1400

```

:39278 :DIVIDE H FORMAT SUBROUTINE
:39279
:39280 :INPUTS:
:39281 :          RCO-ID1 = DIVIDOR
:39282 :          RC2-ID3 = DIVIDEND
:39283
:39284 =000
:39285 DIVH.SUBR.:000-----:
:39286 CLR.SD&SS, : CLEAR SIGN-FLIP-FLOPS
:39287 ALU RC[2],N&Z_ALU.V&C_0,WORD,
:39288 CALL,J/UNPACKH
:39289
:39290 DIVH.20.:001-----: DIVISOR = 0
:39291 RC[7]_K[.9],J/FLOAT.FAULT
:39292
:39293 :010-----: DIVIDEND = 0, DIVISOR NE 0
:39294 D 0,Q 0,RC[0]_0,
:39295 SC K[.30],
:39296 N&Z ALU.V&C 0,
:39297 J/CLEAR.DIRTY.0
:39298
:39299 =011 :011-----: BOTH OPERANDS NON-ZERO
:39300
:39301 :RETURNS WITH:
:39302 : D= RC[6] = DIVIDEND EXPONENT
:39303 : RCO-ID1 = DIVISOR FRACTION
:39304 : RC4 = DIVISOR EXPONENT (BIASSED)
:39305 : RC2-ID3 = DIVIDEND FRACTION
:39306 : RC6 = DIVIDEND EXPONENT(BIASSED)
:39307 : SS = -SIGN
:39308
:39309 LC RC[4], : LATCH EXPONENT OF DIVISOR
:39310 Q ID[1], : Q GETS FRAC1
:39311 J7DIVH.S.1
:39312
:39313 :100-----:
:39314 =100 J/DIVH.20 : BOTH OPERANDS ARE 0
:39315 =:END
:39316
:39317 DIVH.S.1:SD SS, : NEED TO COMPLEMENT SIGN-FF
:39318 ALU_D-LC,D_ALU, : EXP2-EXP1
:39319 LAB_R[R1], : NEED TO SAVE R1
:39320 K[.4000] : BIAS
:39321
:39322 :-----:
:39323 SD NOT.SD, : COMPLEMENT SIGN
:39324 ALU D+K[.4000], : BIASSED QUOTIENT EXPONENT
:39325 RC[6]_ALU, : STORE EXPONENT IN RC6
:39326 D_0
:39327
:39328 :-----:
:39329 ID[1]_D, : CLEAR QUOTIENT
:39330 D LA, : D GETS R1
:39331 LC_RC[0] : LATCH FRAC 1

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U 1960, 0010,4039,0187,F910,0050,157B

U 1961, 0018,0038,D980,F9B8,0000,12B4

U 1962, 0F03,003C,79F8,F980,00D4,7632

U 1963, 0000,003C,C5F0,2D20,0000,15DD

U 1964, 0000,003C,0180,F800,0000,1961

U 15DD, 0811,0000,B184,FA08,0000,15DE

U 15DE, 0F19,0014,B183,F980,0000,15E0

U 15E0, 0800,003C,C580,3D00,0000,15E1

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:39332 :-----:
:39333 ID[T8] D : SAVE R1 IN T8
U 15E1, 0010,0038,E180,3EF8,0000,15E2 :39334 ALU_LC,R[R15]_ALU : R15 GETS DI'END FRAC0
:39335 :-----:
:39336 :-----:
:39337 ALU_Q,RC[T5]_ALU, : STORE FRAC3 IN RC5
:39338 D_Q : D GETS FRAC3 AS WELL
U 15E2, 0C01,203C,C1F0,2DA8,0000,15E4 :39339 Q_ID[T0] : Q GETS FRAC1
:39340 :-----:
:39341 :-----:
U 15E4, 0001,203C,0180,F9A0,0000,15E5 :39342 RC[T4]_Q
:39343 :-----:
:39344 :-----:
U 15E5, 0000,003C,0180,F908,0000,15E6 :39345 LC_RC[T1]
:39346 :-----:
:39347 :-----:
U 15E6, 0010,0038,CDF0,2E88,0000,1AA2 :39348 Q_ID[T3], : Q GETS D'END FRAC3
:39349 R[R1]_LC : R1 GETS D'SOR FRAC2
:39350 :-----:
:39351 =0 :0 :-----: CALL INNER DIVIDE LOOP
:39352 SC_KC.20], : INITIAL LOOP-COUNT
:39353 ALU_Q-D, : SUBTRACT
:39354 D_ALU.LEFT, : SHIFT RESULT LEFT
:39355 SET_CC(LONG), : CLOCK BORROW
:39356 SI/ZERO, :
:39357 LAB_R[R1], :
U 1AA2, 083D,2001,7580,FA08,00F4,75F1 :39358 CALL,J/DIVH.LOOP.1 : START WITH A SUBTRACT
:39359 :-----:
:39360 :1 :-----:
:39361 RC[T0] D,D_0, : SAVE HIGH QUOTIENT IN RCO
U 1AA3, 0F01,003C,7580,F980,0184,7AA4 :39362 SC_KC.20],FE_KC.20]
:39363 =:END
:39364 =0 :0 :-----: CALL INNER DIVIDE LOOP
:39365 ID[T1] D, : CLEAR QUOTIENT
:39366 D_RC[T5], : GET D'SOR FRAC3
U 1AA4, 0810,0339,C580,3D28,0000,1AAC :39367 C31?,CALL,J/DIVH.LOOP : DO A RETURN1
:39368 :-----:
:39369 :1 :-----:
:39370 ID[T0]_D,D_0 :
U 1AA5, 0F00,003C,C180,3C00,0000,1AA8 :39371 =:END
:39372 =0 :0 :-----: CALL INNER DIVIDE LOOP
:39373 SC_FE, :
:39374 D_RC[T5], :
:39375 ID[T1] D, : CLEAR QUOTIENT
U 1AA8, 0810,0339,C580,3D28,0081,1AAC :39376 C31?,CALL,J/DIVH.LOOP
:39377 :-----:
:39378 :1 :-----:
:39379 RC[T1] D, : STORE QUOTIENT FRAC2
:39380 SC_KC.T4], : FEWER PASSES IN LAST PASS
U 1AA9, 0F01,003C,2180,F988,0084,7AAA :39381 D_0
:39382 =:END

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:39383 =0 ;0-----; CALL INNER DIVIDE LOOP
:39384 D RC[T5], ; D GETS DIVISOR FRAC3
:39385 ID[T1] D, ; CLEAR INITIAL QUOTIENT
U 1AAA, 0810,0339,C580,3D28,0000,1AAC :39386 C31?,CALL,J/DIVH.LOOP
:39387
:39388 ;1-----;
U 1AAB, 0000,003C,E1F0,2C00,0000,15E8 :39389 Q_ID[T8] ; RETRIEVE ORIGINAL R1
:39390
:39391 ;-----;
U 15E8, 0001,203C,3DF0,2E88,0000,15E9 :39392 R[R1]_Q,Q_ID[PSL] ; RESTORE OLD R1,GET PSL
:39393
:39394 ;-----;
U 15E9, 0000,003C,8580,F800,0084,75EA :39395 SC_K[C] ; NEED TO LEFT-ADJUST LOW FRAC
:39396
:39397 ;-----;
U 15EA, 0D19,2024,05C0,F800,0000,15EC :39398 Q_Q.ANDNOT.K[.1], ; CLEAR C BIT
:39399 D_DAL.SC
:39400
:39401 ;-----;
U 15EC, 0000,003C,1980,F800,0084,75ED :39402 SC_K[ZERO] ;
:39403
:39404 ;-----;
U 15ED, 0C00,003C,C580,3C00,0000,15EE :39405 ID[T1]_D,D_Q ; STORE QUOTIENT FRAC <VLS>
:39406
:39407 ;-----;
U 15EE, 0000,003C,3D80,3C00,0000,15A5 :39408 ID[PSL]_D,J/ADDH.310 ; GO TO ROUND AND PACK RESULT
:39409 =;END ;-----;

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:39410 : INNER LOOP FOR DIVH
:39411 : EXPECTS:
:39412 : DIVISOR IN R15,RC4,R1 (=LA),RC5
:39413 : DIVIDEND IN RC2-ID3
:39414 :
:39415 : QUOTIENT IN ID1
:39416 :
:39417 : LOOP COUNT IS IN SC
:39418 : ALU CARRY DETERMINES WHETHER WE DO ADD OR SUBTRACT
:39419 : STATE<4> TELLS US OF FIRST TIME PASS
:39420 :
:39421 DIVH.LOOP.0:
:39422 -----
:39423 D_RC[T5], : D GETS D'SOR FRAC3
:39424 Q_ID[T3], : Q GETS D'END FRAC3
:39425 C31? : ADD OR SUBTRACT
:39426 :
:39427 -----
:39428 =0* : BRANCH ON ALU C31
:39429 : 0* -----
:39430 DIVH.LOOP:ALU D+Q,D_ALU.LEFT, : BORROW
:39431 SI/ZERO, : ADD AND SHIFT LEFT
:39432 SET.CC(LONG), : LOW BITS
:39433 LC RC[T3], : CLOCK C AND N OF PSL
:39434 Q_ID[T2], : LATCH D'END FRAC 2
:39435 J7DIVH.LOOP.ADD.2 : READ D'END FRAC 1
:39436 :
:39437 : 1* -----
:39438 STATE.STATE.ANDNOT.K[.10], : NO BORROW, SUBTRACT
:39439 ALU Q=D, : CLEAR FIRST TIME FLAG
:39440 D ALU.LEFT, : SUBTRACT WITH BORROW
:39441 SET.CC(LONG), : SHIFT LEFT
:39442 SI/ZERO, : CLOCK C AND N OF PSL
:39443 LAB_R[R1] : LOW BITS
:39444 =:END : LATCH D'SOR FRAC2
:39445 DIVH.LOOP.1:-----
:39446 ID[T3] D, : STORE IN T3
:39447 D_RC[T3] : GET D'END FRAC2
:39448 :
:39449 -----
:39450 ALU D[INST.DEP]LB, : SUBTRACT WITH BORROW
:39451 SET.CC(LONG), : CLOCK PSL-C FOR POSSIBLE BORROW
:39452 RC[T3] ALU.LEFT, : RESTORE D'END FRAC2
:39453 Q_ID[T2], : Q GETS D'END FRAC1
:39454 SI/DIVD : SHIFT IN PSL N-BIT
:39455 :
:39456 -----
:39457 LC_RC[T4], : LATCH D'SOR FRAC1
:39458 D_Q, : D GETS D'END FRAC1
:39459 Q_ID[T1] : Q GETS QUOTIENT
:39460

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U 15F0, 0810,0338,CDF0,2D28,0000,1AAC

U 1AAC, 083D,0014,C9F0,2D18,0070,15F9

U 1AAE, 083D,2000,6580,FA08,1474,55F1

U 15F1, 0810,0038,CD80,3D18,0000,15F2

U 15F2, 002D,000C,C870,2D98,0070,15F3

U 15F3, 0C00,003C,C5F0,2D20,0000,15F4

```

:39461 :-----:
:39462 SC SC-K[.1], : DECREMENT COUNT
:39463 ALU D[INST.DEP]LC, : SUBTRACT WITH BORROW
:39464 D ALU.LEFT, : D GETS RESULT*2
:39465 SI/DIVD, : SHIFT IN PSL N-BIT
:39466 SET.CC(LONG), : CLOCK C AND N OF PSL
U 15F4, 0831,000C,0400,FA78,00F4,B5F5 :39467 LAB_RCR15] : LATCH D'SOR FRACO
:39468 :-----:
:39469 :
:39470 ID[2] D, : RESTORE D'END FRAC1
U 15F5, 0810,0038,C980,3D10,0000,15F8 :39471 D_RC[2] : GET D'END FRACO
:39472 :-----:
:39473 :
:39474 ALU D[INST.DEP]LB, : SUBTRACT WITH BORROW
:39475 CLK.LBCC, : CLOCK ALU BORROW
:39476 RC[2] ALU.LEFT, :
:39477 QK/LEFT, : SHIFT QUOTIENT LEFT
:39478 SI/DIVD, : SHIFT IN PSL N-BIT
U 15F8, 002D,140C,0028,F990,0010,1AB1 :39479 SC.GT.0? : COUNTER STILL POSITIVE ?
:39480 J/DIVH.LOOP.ADD3
:39481 :-----:
:39482 DIVH.LOOP.ADD.2: :
:39483 ID[3] D, : REWRITE NEW D'END
:39484 ALU LA+LC+PSL.C, : NOTE THAT LA = R1
:39485 RC[3] ALU.LEFT, : ADD AND SHIFT
U 15F9, 0030,002C,CC00,3D98,0070,15FA :39486 SET.CC(LONG), : CLOCK C AND N OF PSL
:39487 SI/DIVD : SHIFT IN PSL N-BIT
:39488 :-----:
:39489 :
:39490 SC SC-K[.1], : DECREMENT COUNT
U 15FA, 0810,0038,0580,F920,0084,B5FC :39491 D_RC[4] : GET D'SOR FRAC1
:39492 :-----:
:39493 DIVH.ADD.LOOP.20: :
:39494 ALU D+Q+PSL.C,D_ALU.LEFT, : ADD TO GET NEW D'END FRAC1
:39495 SI/DIVD, : SHIFT IN PSL N-BIT
:39496 SET.CC(LONG), : CLOCK C AND N OF PSL
U 15FC, 083D,002C,C470,2D10,0070,15FD :39497 LC RC[2], : LATCH D'END FRACO
:39498 Q_ID[1] : GET QUOTIENT
:39499 :-----:
:39500 :
U 15FD, 0000,003C,C980,3E78,0000,15FE :39501 LAB_RCR15],ID[2]_D : TOO BAD, WE NEED THIS STATE
:39502 :-----:
:39503 :
:39504 ALU LA+LC+PSL.C, : ADD FRACO'S
:39505 RC[2] ALU.LEFT, : STORE IN RC2
:39506 SI/DIVD, : SHIFT IN PSL N-BIT
:39507 CLK.LBCC, : USE ALU CARRY FOR ADD/SUB
U 15FE, 0030,142C,0028,F990,0010,1AB1 :39508 QK/LEFT, : SHIFT QUOTIENT
:39509 SC.GT.0? : END OF COUNT ?
:39510

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```

:39511 -----:
:39512 =*0* :BRANCH ON SC GT 0
:39513 -----:
:39514 DIVH.LOOP.ADD3:LAB_RCR1], LATCH DIVISOR FRAC 2
:39515 D_Q,Q_ID[3],RETURN1
:39516 -----:
:39517 :*1*-----:
:39518 D_Q,Q_ID[3], GET D'END FRAC3
:39519 LAB_RCR1] LATCH DIVISOR FRAC 2
:39520 =:END
:39521 -----:
:39522 D_RCR[5], GET D'SOR FRAC3
:39523 ID[1]_D, STORE QUOTIENT
:39524 C31?, ADD AOR SUBTRACT NEXT ?
:39525 J/DIVH.LOOP
:39526 -----:
    
```

U 1AB1, 0C00,003E,CDF0,2E08,0000,0001

U 1AB3, 0C00,003C,CDF0,2E08,0000,1601

U 1601, 0810,0338,C580,3D28,0000,1AAC

```
:39527 .TOC '' G & H floating point : MULTIPLY H FLOATING''  
:39528 : MULH  
:39529 : HERE FOR *-R  
:39530  
:39531 : INPUTS:  
:39532 : RCO-ID1 = M'PLIER  
:39533 : LA = LB = M'CAND LONG EXP  
:39534  
:39535 1428: -----  
:39536 RC[2] LA, : GET DIVIDEND LONG EXP  
:39537 N&Z_ALU.V&C_0,WORD, : CLEAR C AND V OF PSL  
:39538 K[.80], : FOR READ HUGE ROUTINE  
:39539 D 0, :  
U 1428, CF00,403D,4180,F990,0050,1862 :39540 CALL,J/HUGE.REG.READ.1 :  
:39541  
:39542 143E: -----  
U 143E, 0000,003C,1980,F800,1404,7AA6 :39543 STATE_K[ZERO] : NOTHING TO DO  
:39544  
:39545 =0**** :0****-----  
U 1AA6, 0000,003D,0180,F800,0000,1970 :39546 CALL,J/MULH.00 : MULTIPLY HUGE SUBROUTINE  
:39547  
:39548 :1****-----  
U 1AB6, 0000,00BC,0080,F800,0000,18D4 :39549 TRAP.ACC[1], : RESET THE ACCEL  
:39550 J/HUGE.REG.WRITE.1 :  
:39551 :-----  
:39552  
:39553 : HERE FOR MULH *-M, AND *-*-  
:39554  
:39555 : INPUTS:  
:39556 : RCO-ID1 = M'PLIER  
:39557 : RCO-ID3 = M'CAND  
:39558  
:39559  
U 148C, 0000,093C,0180,F800,0000,1842 :39560 148C: IR2-1? : IS THIS MULH OR TSTH ?  
:39561  
:39562 -----  
:39563 =0**10 : BRANCH ON IR<2:1> :  
:39564 :0**10-----  
:39565 STATE_K[ZERO], :  
U 1842, 0010,4039,1980,F900,1454,7970 :39566 ALU_RC[0],N&Z_ALU.V&C_0,WORD, : CLEAR C AND V OF PSL  
:39567 CALL,J/MULH.00 :  
:39568  
:39569 :0**10-----  
U 1843, 0010,0038,01C0,F900,0000,181D :39570 ALU_RC[0],Q_ALU,J/TSTH.00 : TSTH, M-FORMAT  
:39571  
:39572 :1**10-----  
U 1852, F000,003F,01F0,F847,0000,1400 :39573 WRITE.G.DEST :  
:39574 =:END :-----  
:39575
```



```
:39576 : MULTIPLY-ROUTINE
:39577 : USED BY POLYH AND EMODH AS WELL
:39578
:39579 : INPUTS:
:39580 :          RC0-ID1 = MULTIPLIER (REFERRED TO AS A0-A3)
:39581 :          RC2-ID3= MULTIPLICAND (= B0-B3)
:39582 : OUTPUTS:
:39583 :          RC0-ID1 = PRODUCT FRACTION
:39584 : TEMPORARIES:
:39585 :          T6-T9 TEMPORARILY HOLDS PRODUCT
:39586 :          RC4-RC6 USED FOR EXPONENT AND TEMP. STORAGE
:39587
:39588 =000
:39589 MULH.00:;000-----;
:39590 CLR.SD&SS,          ; CLEAR SIGN-FLIP-FLOPS
:39591 CALL,J/UNPACKH
:39592
:39593 :001-----; MULTIPLIER = 0
:39594 SC,K[.30],          ; POINTER FOR DEST
:39595 D 0,Q 0,            ; PRODUCT IS 0
:39596 RC[1] 0,           ; STORE 0
:39597 NZ ALD.V&C 0,    ; SET Z, CLEAR N
:39598 J/CLEAR.DIRTY.0
:39599
:39600 :010-----; MULTIPLICAND = 0
:39601 SC,K[.30],          ; POINTER FOR DEST
:39602 D 0,Q 0,            ; PRODUCT IS 0
:39603 RC[1] 0,           ; STORE 0
:39604 NZ ALD.V&C 0,    ; SET Z, CLEAR N
:39605 J/CLEAR.DIRTY.0
:39606
:39607 :011-----; BOTH OPERANDS NON-ZERO
:39608 ;RETURN WITH:
:39609 :          RC0-ID1 = MULTIPLIER FRACTION = A0,A1,A2,A3
:39610 :          RC2-ID3 = MULTIPLICAND FRACTION = B0,B1,B2,B3
:39611 :          RC4 = MULTIPLIER EXPONENT (BIASSED)
:39612 :          RC6 = MULTIPLICAND EXPONENT (BIASSED)
:39613 :          D = 'CAND EXPONENT
:39614 :          SS = SIGN, FOR MULH AT LEAST
:39615 :
:39616 : THE PROBLEM IS THAT THE MULTIPLICAND FRACTION IS NOT ALIGNED QUITE
:39617 : THE WAY WE WANT IT, NAMELY WITH A LEADING ZERO IN EACH LONGWORD.
:39618
:39619 SD SS,              ; DUPLICATE SIGN FLIP-FLOP
:39620 Q ID[2],           ; GET LOW 'CAND FRAC1
:39621 LC RC[4],         ; LATCH 'PLIER EXPONENT
:39622 J/MULH.01
:39623
:39624 =100 :100-----; BOTH ARE 0
:39625 SC,K[.30],          ; POINTER FOR DEST
:39626 D 0,Q 0,            ; PRODUCT IS 0
:39627 RC[1] 0,           ; STORE 0
:39628 NZ ALD.V&C 0,    ; SET Z, CLEAR N
:39629 J/CLEAR.DIRTY.0
:39630 =;END ;-----;
```

U 1970, 0000,003D,0187,F800,0000,157B

U 1971, 0F03,003C,79F8,F988,00D4,7632

U 1972, 0F03,003C,79F8,F988,00D4,7632

U 1973, 0000,003C,C9F4,2D20,0000,1602

U 1974, 0F03,003C,79F8,F988,00D4,7632

	:39631	MULH.01:-----	:	
U 1602, 0C11,0014,01B0,F9B0,0000,1603	:39632	ALU D+LC,RC[6] ALU,	:	SUM THE TWO EXPONENTS
	:39633	QK/RIGHT,SI/ZERO,D_Q	:	M' CAND FRAC1 GETS LEADING 0
	:39634	-----	:	
	:39635		:	
	:39636	D_Q,Q_D,	:	D GETS FRAC1/2
U 1603, 0C1B,001C,F1E0,FAF8,0084,7605	:39637	ALU NOT.K[.FFFC],RC[R15]_ALU,	:	R15 GETS 3
	:39638	SC_RC[.FFFC]	:	SC GETS -4
	:39639	-----	:	
	:39640		:	
	:39641	ID[2] D,	:	RESTORE FRAC1
U 1605, 0810,0038,C980,3D18,0000,160E	:39642	D_RC[3]	:	D GETS FRAC2
	:39643	-----	:	
	:39644		:	
	:39645	DK/RIGHT,SI/ASHR,	:	SHIFT IN ONE BIT FROM FRAC1
U 160E, 0600,003C,CCF0,2C00,0000,1610	:39646	Q_ID[3]	:	GET FRAC3
	:39647	-----	:	
	:39648		:	
	:39649	ALU_D,RC[3]_ALU.RIGHT,SI/ZERO,	:	RESTORE SHIFTED FRAC2
U 1610, 0C41,003C,0180,F998,0000,1611	:39650	D_Q	:	
	:39651	-----	:	
	:39652		:	
	:39653	LAB_R[R15],	:	LATCH 3
U 1611, 0010,0034,01C0,FA78,0080,D612	:39654	ALU_LA.AND.LC,Q_ALU,	:	ISOLATE LOW 2 BITS OF FRAC2
	:39655	SC_SC+1	:	SC NOW HAS -3
	:39656	-----	:	
	:39657		:	
	:39658	D_DAL.SC,	:	GENERATE NEW FRAC3
U 1612, 0D00,003C,C5F0,2C00,0000,1AB8	:39659	Q_ID[1]	:	GET READY TO MULTIPLY BY A3
	:39660	-----	:	
	:39661	:0*	:	
	:39662	=0* ALU D,RC[4] ALU.LEFT,	:	RC 4 GETS B3*2
	:39663	ID[3] D,SI/ZERO,	:	ID3 GETS B3
U 1AB8, 0C21,003D,CDE0,3DA0,0000,1947	:39664	D_Q,Q_D,	:	D GETS A3, Q GETS B3
	:39665	CALL,J/MPY.HUGE.1	:	
	:39666	-----	:	
	:39667		:	
	:39668	:1* LC_RC[3],	:	RETURN WITH: <Q,D> = A3*B3
U 1ABA, 0000,003C,0128,F918,0000,1613	:39669	QK7LEFT, SI/ASHL	:	LATCH B2
	:39670	-----	:	NEED TO SAVE HIGH 32 BITS ONLY
	:39671		:	
	:39672	ALU_LC,RC[4]_ALU.LEFT,SI/ZERO,	:	RC4 GETS B2*2
U 1613, 0C30,0038,C5F0,2DA0,0000,1614	:39673	D_Q,Q_ID[1]	:	Q GETS A3
	:39674	-----	:	
	:39675		:	
	:39676	ID[9] D,D_Q,	:	STORE PARTIAL PRODUCT <LS>
U 1614, 0F10,0038,E580,3EF8,0000,1A00	:39677	ALU_LC,RC[R15]_ALU	:	R15 GETS B2
	:39678	-----	:	

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:39679 :00-----:
:39680 =00 ID[T8]_D, : CLEAR PARTIAL PROD <MS>
:39681 D_LC, : D GETS B2
U 1A00, 0810,0039,E180,3C00,0000,1956 :39682 CALL,J/MULTIPLY.HUGE.SUBR
:39683 :
:39684 :10-----: RETURN WITH: <Q,D> = A3*B2
:39685 =10 SC_KC.FFFF], : SC GETS -1
U 1A02, 0000,003D,C180,F800,0084,7626 :39686 CALL,J/HUGE.MUL.ADD.SHF : ADD TO PARTIAL PRODUCT AND SHIFT
:39687 :
:39688 =11 :11-----:
:39689 Q_ID[T3], : Q GETS B3
U 1A03, 0810,0038,CDF0,2D08,0000,1A04 :39690 D_RC[T1] : D GETS A2
:39691 =:END
:39692 =00 :00-----:
:39693 ALU Q,RC[T4]_ALU.LEFT, : RC4 GETS B3*2
U 1A04, 0021,203D,0180,F9A0,0000,1947 :39694 SI/ZERO,
:39695 CALL,J/MPY.HUGE.1
:39696 :
:39697 :10-----: RETURN WITH : <Q,D> = A2*B3
U 1A06, 0000,003D,0980,F800,0084,7626 :39698 =10 SC_KC.2], : RIGHT SHIFT OF 32.
:39699 CALL,J/HUGE.MUL.ADD.SHF
:39700 :
:39701 :11-----:
U 1A07, 0000,003C,C9F0,2C00,0000,1A08 :39702 =11 Q_ID[T2] : Q GETS B1
:39703 =:END
:39704 :00-----:
:39705 =00 D_Q, : D GETS B1
U 1A08, 0C00,003D,C5F0,2C00,0000,1956 :39706 Q_ID[T1], : Q GETS A3
:39707 CALL,J/MULTIPLY.HUGE.SUBR
:39708 :
:39709 :10-----: RETURN WITH: <Q,D> = A3*B1
U 1A0A, 0000,003D,C180,F800,0084,7626 :39710 =10 SC_KC.FFFF], : SC GETS -1 FOR RIGHT SHIFT
:39711 CALL,J/HUGE.MUL.ADD.SHF
:39712 :
:39713 :11-----:
U 1A0B, 0F10,0038,01C0,F918,0000,1A10 :39714 =11 Q_RC[T3], : Q GETS B2
:39715 D_0 : NEED TO CLEAR OUT T7
:39716 =:END
:39717 :00-----:
:39718 =00 ID[T7]_D, : CLEAR OUT PARTIAL PRODUCT FRAC1
:39719 D_Q, : D GETS B2
U 1A10, 0C10,0039,DDC0,3D08,0000,1956 :39720 Q_RC[T1], : Q GETS A2
:39721 CALL,J/MULTIPLY.HUGE.SUBR
:39722 :
:39723 :10-----: RETURN WITH: <Q,D> = A2*B2
U 1A12, 0000,003D,C180,F800,0084,7626 :39724 =10 SC_KC.FFFF], : SC GETS -1
:39725 CALL,J/HUGE.MUL.ADD.SHF
:39726 :
:39727 :11-----:
U 1A13, 0000,003C,CDF0,2C00,0000,1A14 :39728 =11 Q_ID[T3] : Q GETS B3
:39729 =:END
  
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:39730 :00-----:
U 1A14, 0C00,003D,C1F0,2C00,0000,1956 :39731 =00 D_Q,Q_ID[T0], : D GETS B3, Q GETS A1
:39732 CALL,J/MULTIPLY.HUGE.SUBR :
:39733
:39734 :10-----:
U 1A16, 0000,003D,0D80,F800,0084,7626 :39735 =10 SC_K[.3], : RETURN WITH: <Q,D> = A1*B3
:39736 CALL,J/HUGE.MUL.ADD.SHF : LOAD SC FOR RIGHT SHIFT OF 29.
:39737
:39738 :11-----:
U 1A17, 0810,0038,C5F0,2D10,0000,1A20 :39739 =11 Q_ID[T1], : Q GETS A3
:39740 D_RC[T2] : D GETS B0
:39741 =:END
:39742 :00-----:
:39743 =00 ALU_D,RC[T4]_ALU.LEFT, : RC4 GETS B0*2
:39744 SI/ZERO,
U 1A20, 0C21,003D,01E0,F9A0,0000,1947 :39745 D_Q,Q_D, : SWAP A3 AND B0
:39746 CALL,J/MPY.HUGE.1
:39747
:39748 :10-----:
U 1A22, 0000,003D,C180,F800,0084,7626 :39749 =10 SC_K[.FFFF], : RETURN WITH: <Q,D> = A3*B0
:39750 CALL,J/HUGE.MUL.ADD.SHF : SC GETS -1
:39751
:39752 :11-----:
U 1A23, 0810,0038,C9F0,2D08,0000,1A24 :39753 =11 Q_ID[T2], : Q GETS B1
:39754 D_RC[T1] : D GETS A2
:39755 =:END
:39756 :00-----:
:39757 =00 ALU_Q,RC[T4]_ALU.LEFT, : RC4 GETS B1*2
:39758 SI/ZERO,
U 1A24, 0021,203D,0180,F9A0,0000,1947 :39759 D_Q,Q_D, : SWAP A1 WITH B2
:39760 CALL,J/MPY.HUGE.1
:39761
:39762 :10-----:
U 1A26, 0000,003D,C180,F800,0084,7626 :39763 =10 SC_K[.FFFF], : RETURN WITH : <Q,D> = A2*B1
:39764 CALL,J/HUGE.MUL.ADD.SHF : SC GETS -1
:39765
:39766 :11-----:
U 1A27, 0810,0038,C1F0,2D18,0000,1A28 :39767 =11 Q_ID[T0], : Q GETS A1
:39768 D_RC[T3] : D GETS B2
:39769 =:END
:39770 :00-----:
:39771 =00 ALU_D,RC[T4]_ALU.LEFT, : RC4 GETS B2*2
:39772 SI/ZERO,
U 1A28, 0C21,003D,01E0,F9A0,0000,1947 :39773 D_Q,Q_D, : SWAP A1 WITH B2
:39774 CALL,J/MPY.HUGE.1
:39775
:39776 :10-----:
U 1A2A, 0000,003D,C180,F800,0084,7626 :39777 =10 SC_K[.FFFF], : RETURN WITH: <Q,D> = A1*B2
:39778 CALL,J/HUGE.MUL.ADD.SHF : SC GETS -1
:39779
:39780 :11-----:
U 1A2B, 0810,0038,CDF0,2D00,0000,1A30 :39781 =11 D_RC[T0], : D GETS A0
:39782 Q_ID[T3] : Q GETS B3
:39783 =:END
  
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:39783 :00-----:
:39784 =00 ALU Q,RC[4]_ALU.LEFT, : RC4 GETS B3*2
:39785 SI/ZERO, :
:39786 CALL,J/MPY.HUGE.1 :
:39787 :
:39788 :10-----: RETURN WITH: <Q,D> = A0*B3
:39789 =10 SC_K[.4], : SHIFT 28. TO KEEP 3 GUARD BITS
:39790 CALL,J/HUGE.MUL.ADD.SHF :
:39791 :
:39792 :11-----:
:39793 =11 SC_K[.30], : BASE FOR ID-REGISTERS
:39794 D_RC[2] : GET B0
:39795 :
:39796 :00*-----:
:39797 =00* FE_SC+K[.9], : FE GETS .39 = ADDRESS OF T9
:39798 Q_RC[1], : Q GETS A2
:39799 CALL, J/MULTIPLY.HUGE.SUBR :
:39800 :
:39801 :01*-----: RETURN WITH: <Q,D> = A2*B0
:39802 =01* SC_K[.1], : FE = .39
:39803 : SHIFT COUNT OF 31.
:39804 CALL,J/MULH.ADD : ADD IN NEW PRODUCT
:39805 :
:39806 :11*-----:
:39807 =11* ID(SC)_D, : WRITE BACK PARTIAL PROD <MS>
:39808 FE_SC+R[.2] : FE GETS .39
:39809 =:END :
:39810 :
:39811 Q_ID[2] : Q GETS B1
:39812 :
:39813 :00*-----:
:39814 =00* D_Q,Q_ID[0], : D GETS B1, Q GETS A1
:39815 CALL,J/MULTIPLY.HUGE.SUBR :
:39816 :
:39817 :01*-----: RETURN WITH: <Q,D> = A1*B1
:39818 =01* SC_K[.2], : OFFSET OF 30.
:39819 CALL,J/MULH.ADD :
:39820 :
:39821 :11*-----:
:39822 =11* FE_SC+K[.2], : SC GETS .39
:39823 ID(SC)_D, : WRITE PARTIAL PROD <MS>
:39824 D_Q, : NEEDED FOR INITIALIZATION OF T6
:39825 Q_RC[3] : Q GETS B2
:39826 =:END

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:39827      :00*-----:
:39828 =00*  ID[6]_D,      : CLEAR OUT PARTIAL PROD FRACO
:39829      D_Q,          : D GETS B2
:39830      Q_RC[0],     : Q GETS A0
U 19A8, 0C10,0039,D9C0,3D00,0000,1956 :39831      CALL,J/MULTIPLY.HUGE.SUBR
:39832
:39833      :01*-----: RETURN WITH: <Q,D> = A0*B2
:39834 =01*  SC_K[.3],   : FE = .39
:39835      CALL,J/MULH.ADD      : OFFSET OF 29.
U 19AA, 0000,003D,0D80,F800,0084,7AC0 :39836
:39837
:39838      :11*-----:
:39839 =11*  ID(SC) D,      : REWRITE PARTIAL PROD <MS>
:39840      FE_SC+R[.1],    : FE GETS .38
U 19AE, 0810,0038,0580,3510,0104,99C0 :39841      D_RC[2]      : D GETS B0
:39842 =:END
:39843      :00*-----:
:39844 =00*  Q_ID[0],      : Q GETS A1
:39845      CALL,J/MULTIPLY.HUGE.SUBR
U 19C0, 0000,003D,C1F0,2C00,0000,1956 :39846
:39847 =01*  :01*-----: RETURN WITH: <Q,D> = A1*B0
:39848      SC_K[.1],      : FE = .38
:39849      CALL,J/MULH.ADD      : OFFSET OF 31.
U 19C2, 0000,003D,0580,F800,0084,7AC0 :39850
:39851
:39852      :11*-----:
:39853 =11*  ID(SC) D,      : REWRITE LAST PARTIAL PRODUCT
:39854      D_RC[0],      : D GETS A0
U 19C6, 0810,0038,0980,3500,0104,9616 :39855      FE_SC+K[.2]    : FE GETS .38
:39856 =:END
:39857      :-----:
U 1616, 0000,003C,C9F0,2C00,0000,19E0 :39858      Q_ID[2]      : Q GETS B1
:39859
:39860      :00*-----:
:39861 =00*  ALU Q,RC[4] ALU.LEFT,SI/ZERO, : RC4 GETS B1*2
:39862      CALL,J/MPY.HUGE.1
:39863
:39864      :01*-----: RETURN WITH:<Q,D> = A0*B1,FE = .38
:39865 =01*  SC_K[.2],      : OFFSET OF 30.
:39866      CALL,J/MULH.ADD
U 19E2, 0000,003D,0980,F800,0084,7AC0 :39867
:39868
:39869 =11*  :11*-----: REWRITE LAST PARTIAL PROD
:39870      ID(SC) D,      : Q GETS A0
:39871      Q_RC[0],      : NEED TO CLEAR IDS
U 19E6, 0F10,0038,05C0,3500,0104,99F0 :39872      D_0,          : FE GETS .37
:39873 =:END      FE_SC+K[.1]
    
```

```
:39874 :00*-----:
:39875 =00* ID[T5] D, : CLEAR ID5
:39876 D RC[T2], : D GETS B0
U 19F0, 0810,0039,D580,3D10,0000,1956 : CALL,J/MULTIPLY.HUGE.SUBR
:39877
:39878
:39879 :01*-----: RETURN WITH <Q,D> = A0*B0
:39880 =01* SC_K[.1], : OFFSET OF 31.
:39881 CALL,J/MULH.ADD
:39882
:39883 :11*-----: RETURN ID6-ID9 = PRODUCT-FRACTION
:39884 =11* : Q = ID6
:39885 D_Q, : D GETS FRAC 0
:39886 Q_ID[T7] : Q GETS FRAC 1
:39887 =:END
:39888
:39889 FE_SHF.VAL, : FE GETS SHIFT-VALUE
:39890 SC_SHF.VAL, : SC GETS SHIFT-VALUE AS WELL
:39891 STATE3-0? : TEST FOR POLY OR EMOD
:39892
:39893
:39894 =01100 : BRANCH ON STATE<1:0>
:39895 :01100-----:
:39896 SC_SC+1, : MULH, SHIFT OUT HIDDEN BIT
:39897 CALL,J/SHIFT.MULH.ID : SHIFT ID5-8 INTO RCO-ID1
:39898
:39899 :01101-----:
:39900 SC_SC-K[.1], : POLYH, LEAVE OVERFLOW-BIT
:39901 J/SHIFT.MULH.ID
:39902
:39903 =01111 :01111-----:
:39904 SHIFT.MULH.ID:
:39905 D_DAL.SC, : D GETS FRAC <VMS>
:39906 J7SHIFT.MULH.ID.1 : EMODH, JUST NORMALIZE
:39907
:39908 =11110 :11110-----:
:39909 : D = LEAST FRACTION
:39910 : FE = LEADING 0S IN FRACTION (BEFORE THE RECENT NORMALIZING)
:39911 : Q = BIASSED EXPONENT
:39912 : R06 = BIASSED EXP
:39913 K[.8000], : ROUNDING CONSTANT
:39914 Q_RC[T1], : NEED FRAC <ALS>
:39915 J7ADDDH.380 : GO TO ROUND AND PACK RESULT
:39916 =:END
```

```

:39917 : ROUTINE TO NORMALIZE FRACTION AFTER MULTIPLYING.
:39918 : SC HAS NUMBER OF POSITIONS TO SHIFT LEFT.
:39919 : FOR MULH, THE SHIFT GOES ONE BIT BEYOND THE HIDDEN BIT.
:39920 : FOR POLYH, THE SHIFT LEAVES AN OVERFLOW BIT FOR THE ADD.
:39921 : FOR EMODH, THE NUBER IS NORMALIZED, FOR THE CONVERSION TO INTEGER.
:39922 :
:39923 : RETURN12
:39924 :
:39925 SHIFT.MULH.ID.1:
:39926 -----:
U 161A, 0C01,003C,E1F0,2D80,0000,161C :39927 RC[T0] D, : STORE IT IN RCO
:39928 D_Q,Q_ID[T8] :
:39929 :
:39930 -----:
U 161C, 0D01,203C,E5F0,2D88,0000,161D :39931 D_DAL.SC, :
:39932 RC[T1]_Q,Q_ID[T9] :
:39933 :
:39934 -----:
U 161D, 0810,0038,C180,3D08,0000,161E :39935 ID[T0] D, :
:39936 D_RC[T7] :
:39937 :
:39938 -----:
U 161E, 0D00,003C,0180,F800,0000,1620 :39939 D_DAL.SC :
:39940 :
:39941 -----:
U 1620, 0C01,003C,01F8,F988,0000,1621 :39942 RC[T1] D, :
:39943 D_Q,Q_0 :
:39944 :
:39945 -----:
U 1621, 0D10,0038,B1C0,F930,0000,1622 :39946 Q_RC[T6], : Q GETS EXPONENT+4000
:39947 D_DAL.SC, :
:39948 KC.4000] : EXPONENT IS DOUBLY BIASSED
:39949 :
:39950 -----:
U 1622, 0019,2000,B1C0,F9B0,0081,1624 :39951 ALU Q-KC.4000],RC[T6]_ALU, : RC6 GETS BIASSED EXP
:39952 SC_FE, : SC GETS # OF LEADING 0'S
:39953 Q_ALU : Q GETS BIASSED EXP AS WELL
:39954 :
:39955 -----:
U 1624, 001F,0010,C5C0,3C00,0000,1625 :39956 ID[T1] D, :
:39957 ALU 0+Q+1, : ADJUST EXP FOR ONE LEADING 0
:39958 Q_ALU :
:39959 :
:39960 -----:
U 1625, 0019,2002,1DC0,F9B0,0000,0012 :39961 ALU Q-K[SC],RC[T6]_ALU, : RC6 GETS ADJUSTED EXP (PRE ROUNDING)
:39962 Q_ALU, : LEAVE IT HERE FOR EMODH-ADJUSTMENT
:39963 RETURN12 : RETURN TO POLY,EMOD OR MULH ROUTINES
:39964 :
    
```



```

:39965 =110
:39966 MULTIPLY.HUGE.SUBR:
:39967 : EXPECTS:
:39968 : D = 31 BITS OF MULTIPLICAND = B-OPERAND
:39969 : Q = 32 BITS OF MULTIPLIER = A-OPERAND
:39970
:39971 : BRANCH ON PENDING INTERRUPTS
:39972 :-----:
:39973 ALU_D,RC[4]_ALU.LEFT, : RC4 GETS M'CAND*2
:39974 SI/ZERO, :
:39975 D_Q,Q_D, : SWAP M'CAND WITH M'PLIER
:39976 D.NE.0?, : TEST FOR MULTIPLICAND = 0?
U 1956, 0C21,0D3C,01E0,F9A0,0000,1945 :39977 J/MULH.SUBR.0
:39978
:39979 H.FORMAT.INTRPT:
:39980 :111-----:
U 1957, 0000,003C,0180,F800,0000,04FA :39981 J/INT.I
:39982 =:END
:39983 :-----:
:39984 =101 : BRANCH ON D.NE.0
:39985 :101-----:
U 1945, 0F00,003E,01F8,F800,0000,0002 :39986 MULH.SUBR.0:
:39987 D_0,Q_0,RETURN2 : PRODUCT IS 0
:39988
:39989 :111-----:
:39990 MPY.HUGE.1:
:39991 : EXPECTS:
:39992 : D = A-OPERAND
:39993 : Q = 31-BITS B-OPERAND
:39994 : RC4 = B-OPERAND*2
:39995 ALU_Q,R[R15]_ALU, : R15 GETS M'CAND
:39996 CLK.LBCC, : CLOCK ALU Z-BIT
U 1947, 0001,2D3C,01F8,FAF8,0010,1965 :39997 Q_0, : CLEAR PRODUCT
:39998 D.NE.0? : IS MULTIPLIER = 0?
:39999
:40000 :-----:
:40001 =101 :BRANCH ON D NE 0
:40002 :101-----:
U 1965, 0F00,003E,01F8,F800,0000,0002 :40003 D_0,Q_0,RETURN2 : PRODUCT IS 0
:40004
:40005 :-----:
:40006 LC_RC[4], : LATCH M'CAND*2
U 1967, 0000,013C,0180,F920,0000,10E8 :40007 Z?,J/MULDMPY : BRANCH ON M'CAND =0
:40008 =:END :-----:
  
```

```

:40009 HUGE.MUL.ADD.SHF:
:40010 ;ROUTINE TO ADD NEW PRODUCT TO RUNNING PARTIAL PRODUCT.
:40011 ;AND SHIFT AND STORE RESULT.
:40012 ; INPUTS:
:40013 <Q,D> = NEW PRODUCT
:40014 SC = SHIFT COUNT (BIT 9 NEED NOT HAVE BEEN SET)
:40015 <T8,T9> = PARTIAL PRODUCT
:40016
:40017 -----
:40018 RC[T5] Q, ; SAVE HIGH PART TEMPORARILY
:40019 Q_ID[T9] ; GET LOW PART OF PARTIAL PRODUCT
:40020
:40021 -----
:40022 ALU D+Q,CLK.UBCC, ; ADD LOW PARTS, CLOCK CARRY
:40023 D,ALU ; D GETS RESULT
:40024 LC,RC[T5], ; LATCH HIGH PART
:40025 Q_ID[T8] ; Q GETS PARTIAL PROD <MS>
:40026
:40027 -----
:40028 SC,SC.OR.K[.FF00], ; SET BIT 9 FOR RIGHT SHIFT
:40029 C3T? ; WAS THERE A CARRY FROM <LS> ADD
:40030
:40031 =0* ;0*-----
:40032 ALU Q+LC,Q_ALU, ;
:40033 CLK.UBCC, ; CLOCK CARRY
:40034 J/HUGE.ASH.1
:40035
:40036 ;1*-----
:40037 ALU Q+LC+1,Q_ALU, ;
:40038 CLK.UBCC, ; CLOCK CARRY
:40039 J/HUGE.ASH.1
:40040
:40041 HUGE.ASH.1:
:40042 -----
:40043 D,DAL.SC, ; D GETS NEW PARTIAL PRODUCT
:40044 C3I? ; ANOTHER CARRY ?
:40045
:40046 =0* ;0*-----
:40047 ID[T9]_D,D_Q,Q_0, ;
:40048 J/HUGE.ASH.2
:40049
:40050 ;1*-----
:40051 ID[T9]_D,D_Q, ;
:40052 ALU_0(A),Q_ALU.LEFT,SI/MUL- ; Q GETS 1
:40053
:40054 HUGE.ASH.2:
:40055 -----
:40056 D,DAL.SC, ; SHIFT <MS> INTO PLACE
:40057 Q_ID[T9] ; NOTHING BETTER TO DO
:40058
:40059 -----
:40060 ID[T8]_D,RETURN1 ; STORE <LS> IN T8
  
```

U 1626, 0001,203C,E5F0,2DA8,0000,1628

U 1628, 081D,0014,E1F0,2D28,0010,1629

U 1629, 0000,033C,4D80,F800,0084,3AB9

U 1AB9, 0011,2014,01C0,F800,0010,162A

U 1ABB, 0011,2010,01C0,F800,0010,162A

U 162A, 0D00,033C,0180,F800,0000,1ABC

U 1ABC, 0C00,003C,E5F8,3C00,0000,162C

U 1ABE, 0C23,003C,E7C0,3C00,0000,162C

U 162C, 0D00,003C,E5F0,2C00,0000,162D

U 162D, 0000,003E,E180,3C00,0000,0001

```

:40061 : ROUTINE TO ADD NEWLY FORMED PRODUCT INTO PARTIAL PRODUCT.
:40062 : ALL THE BITS ARE CONSIDERED SIGNIFICANT
:40063
:40064 : EXPECTS:
:40065 : <Q,D> = NEWLY FORMED PRODUCT
:40066 : FE = STARTING ID-REGISTER ADDRESS
:40067 : SC = OFFSET INTO THAT REGISTER
:40068
:40069 : OUTPUTS:
:40070 : D = MOST SIGNIFICANT 32 BITS OF PARTIAL PRODUCT
:40071 : Q = ID[16]
:40072 : SC = ID-ADDRESS OF MOST SIGNIF PARTIAL PRODUCT
:40073 : ALU CARRY REFLECTS RESULT OF LAST ADD
:40074 : AND WILL BE CLEARED IN ALL CASES EXCEPT THE LAST ONE
:40075 : WHEN IT INDICATES THAT A RIGHT SHIFT IS REQUIRED
:40076
:40077 : TEMPORARIES:
:40078 : RC5 AND R15 ARE USED FOR STORAGE
:40079
:40080 =0** :0**-----:
:40081 MULH.ADD:
:40082 SC SC.OR.K[.FF00], : SET SIGN BIT FOR RIGHT SHIFT
:40083 ALU 0+Q,CLK.UBCC, : CLEAR ALU CARRY-BIT
:40084 RC[15] ALU, : SAVE NEW PROD <MS> IN RC5
:40085 Q D,D 0, : SHIFT IN 0'S ON RIGHT
:40086 CALL,J/MULH.ADD.SUBR
:40087
:40088 :1**-----:
:40089 ID(SC) D, : STORE NEW PARTIAL PRODUCT <LS>
:40090 D RC[15], : D GETS NEW PROD <LS>
:40091 SC_SC-K[.1] : DECREMENT ID-POINTER
:40092 =:END
:40093 =0** :0**-----:
:40094 Q RC[15], : Q GETS NEW PROD <MS>
:40095 SC FE,FE SC,
:40096 CALL,J/MULH.ADD.SUBR
:40097
:40098 :1**-----:
:40099 ID(SC) D, : STORE NEW PARTIAL PROD
:40100 D RC[15], : D GETS NEW PROD <MS>
:40101 Q 0, : SHIFT IN 0'S
:40102 SC FE,FE SC-K[.1],
:40103 J/MULH.ADD.SUBR : NOT A CALL THIS TIME
:40104 =:END
:40105

```

U 1AC0, 0F1F,0015,4DE0,F9A8,0094,3630

U 1AC4, 0800,003C,0580,3678,0084,BAC1

U 1AC1, 0010,0039,01C0,F928,0181,1630

U 1AC5, 0810,0038,05F8,3528,0185,B630

```

:40106 MULH.ADD.SUBR:
:40107 ; SUBROUTINE USED IN THE MULH.ADD ROUTINE
:40108
:40109 -----:
:40110 R[R15] Q, ; SAVE NEW PRODUCT <LS> IN R15
:40111 D DAL.SC, ; SHIFT THE NEW PRODUCT
:40112 SC_FE,FE_SC ; SC GETS ID-ADDRESS, FE GETS SHIFT
:40113
:40114 -----:
:40115 Q_ID(SC),C31? ; Q GETS PARTIAL PRODUCT
:40116
:40117 -----:
:40118 =0* ; BRANCH ON ALU CARRY
:40119 :0* -----:
:40120 ALU D+Q,D_ALU,CLK_UBCC, ; ADD IN NEW PRODUCT
:40121 Q_ID[6],RETURN4
:40122
:40123 -----:
:40124 :1* ; ADD WITH CARRY
:40125 ALU D+Q+1,CLK_UBCC,D_ALU,
:40126 Q_ID[6],RETURN4
:40127 =:
:40128 ; ROUTINE TO CLEAR OUT DIRTY 0 H-FORMAT NUMBERS
:40129
:40130 ; EXPECTS:
:40131 ; SC POINTS TO BASE REGISTER IN RC (TYPICALLY =.30)
:40132 ; D = 0, Q = 0
:40133
:40134 ; RETURNS:
:40135 ; RC(SC),ID(SC),RC(SC+1),ID(SC+1) = 0
:40136 ; SC = SC +1
:40137 ; RETURN1
:40138
:40139 -----:
:40140 CLEAR.DIRTY.0:
:40141 ID(SC)_D, ; CLEAR OUT FRACTION 1
:40142 RC(SC)_Q, ; CLEAR OUT LONG EXP
:40143 SC_SC+T
:40144
:40145 -----:
:40146 ID(SC)_D, ; CLEAR OUT FRACTION 3
:40147 RC(SC)_Q, ; CLEAR OUT FRACTION 2
:40148 RETURNTO
:40149 144D:
:40150 CLRH:
:40151 ; ENTER HERE FOR CLRO AND CLRH
:40152 D 0,Q 0,ALU 0(A), ; CLEAR EVERYTHING
:40153 SET.CC(LONG),
:40154 J/WRITE.DEST.0
:40155 -----:
  
```

U 1630, 0D01,203C,0180,FAF8,0181,1631

U 1631, 0000,033C,01F0,2400,0000,1AC8

U 1AC8, 081D,0016,D9F0,2C00,0010,0004

U 1ACA, 081D,0012,D9F0,2C00,0010,0004

U 1632, 0001,203C,0180,3438,0080,D634

U 1634, 0001,203E,0180,3438,0000,0010

U 144D, 0F03,003C,01F8,F800,0070,190E

```

:40156 : ROUTINE TO MOVE H-FORMAT OPERAND FROM RC2-ID3 TO RCO-ID1
:40157 :
:40158 : EXPECTS:
:40159 : D = RC2
:40160 : Q = ID2
:40161 :
:40162 : RETURNS:
:40163 : RCO-ID1 = RC2-ID3
:40164 : RETURN10
:40165 :
:40166 SHIFT.H:
U 1636, 0C01,003C,CDF0,2D80,0000,1638 :40167 RC[T0] D, : RC[T0] GETS LONG EXP
:40168 D,Q,Q_ID[T3] : D GETS LONG FRAC1
:40169 :
:40170 :-----:
:40171 ID[T0]_D, : TO GETS LONG FRAC1
U 1638, 0C00,003C,C180,3D18,0000,1639 :40172 D,Q, : D GETS LONG FRAC3
:40173 LC_RC[T3] : LATCH LONG FRAC2
:40174 :
:40175 :-----:
:40176 ID[T1]_D, : STORE LONG FRAC3 IN T1
U 1639, 0010,003A,C580,3D88,0000,0010 :40177 RC[T1]_LC, : STORE LONG EXP IN RCO
:40178 RETURN10
:40179 :-----:

```

```

:40180 ;ROUTINE TO UNPACK SINGLE H-FORMAT OPERAND.
:40181
:40182 ;INPUTS:
:40183 RC(SC),ID(SC),RC(SC+1),ID(SC+1) CONTAIN OPERAND
:40184 FE = SC POINTS TO OPERAND
:40185 STATE<7> DETERMINES WHETHER TO NORMALIZE OR NOT
:40186
:40187 ;OUTPUTS:
:40188 RC(SC),ID(SC),RC(SC+1),ID(SC+1) CONTAIN FRACTION
:40189 RC(SC+4) CONTAIN EXPONENT
:40190 R[R15] CONTAINS UNBIASED EXPONENT
:40191 SC CONTAINS LOW 10 BITS OF UNBIASED EXP
:40192
:40193 ;TEMPORARIES:
:40194
:40195 ;RETURNS:
:40196 3 IF NON-ZERO
:40197 1 IF 0
:40198
:40199 -----:
:40200 UNPACK1H:
:40201 Q,RC(SC) ; Q GETS LONG EXP
:40202 SS,SS.XOR.ALU15&SD_ALU15, ; STORE SIGN IN SS AND SD
:40203 SC,SC+K[.4] ; POINT TO EXPONENT ADDRESS
:40204
:40205 -----:
:40206 ALU Q,0XT[WORD].ANDNOT.K[.8000], ; CLEAR SIGNBIT
:40207 RC(SC) ALU, ; STORE EXPONENT IN RC(SC+4)
:40208 CLK,UBCC,WORD, ; CLOCK ALU Z-BIT ON EXPONENT
:40209 D,Q ; D GETS OLEXP
:40210 SC,FE ; SC GETS BASE ADDRESS BACK
:40211
:40212 =01110 ;01110-----:
:40213 ALU Q,ANDNOT.K[.FFFF],D_ALU, ; D GETS HIGH FRACTION WORD
:40214 FE,K[.FFFF], ; FE GETS -1
:40215 Q,ID(SC), ; Q GETS LONG FRAC1
:40216 Z? ; IS OPERAND 0 ?
:40217 CALL,J/UNP.SUBR.3
:40218
:40219 =11110 ;11110-----:
:40220 D,RC[4], ; NEEDED FOR POLYH
:40221 RETURN
:40222
:40223 ;11111-----:
:40224 =11111
:40225 ;RETURN WITH:
:40226 ; RC(SC),ID(SC), RC(SC+1) ARE LOADED WITH 3 MS FRACTION LONGWORDS
:40227 ; D = VLS FRACTION
:40228 ; SC = SC+1 (ORIGINAL SC)
:40229 ; RC(SC+4) = BIASSED EXPONENT
:40230
:40231 ID(SC) D, ; WRITE LAST FRACTION WORD
:40232 SC,SC+R[.3] ; POINT TO EXPONENT
:40233 =:END
:40234 -----:
    
```

ZZ-ES0AA-124.0 : GANDH .MIC [600,1204]

G & H floating poin14-Jan-82

Fiche 5 Frame E16 Sequence 1023

U 163C, 0810,0038,B180,F830,0000,163E

:40235
:40236
:40237
:40238
:40239
:40240
:40241
:40242
:40243

D RC(SC),
K[.4000]

ALU D-K[.4000],R[R15]_ALU,
SC ALU,
CLR UBCC,
RETURN3

: D GETS BIASSED EXPONENT
: SET UP SLOW CONSTANT
:
: R15 GETS UNBIASSED EXPONENT
: SC GETS 10 LOW ORDER BITS
: SET ALU CC ON EXPONENT

U 163E, 0019,0002,B180,FAF8,0092,0003

```

:40244 : ROUTINE TO CONVERT H-FORMAT FLOATING FORMATS TO INTEGERS.
:40245
:40246 :-----:
:40247 1443: :
:40248 CVTHB: ; EXPECTS SRC IN RCO-ID1
:40249 SGN/CLR.SD+SS, ; CLEAR SIGN-FLIPFLOPS
:40250 SC_K[.30],FE_K[.30], ; LOAD BASE OPERAND POINTER
:40251 D_RC[0], ; D GETS LONG EXP
:40252 N&Z_ALU.V&C 0, ; CLEAR C AND V-BITS OF PSL
:40253 CALL,J/CVTHI
:40254
:40255 :-----:
:40256 1453: :
:40257 ALU D,N&Z ALU, ; CLOCK PSL N & Z
:40258 DT/INST.DEP, ; WORKS FOR BYTE,WORD,LONG
:40259 PSL.V? ; CHECK FOR INT OVERFLOW
:40260
:40261 =1100 :1100-----:
:40262 WRITE.DEST ; V-BIT NOT SET,NORMAL
:40263
:40264 =1110 :1110-----:
:40265 Q_ID[CES],CALL[INOVFL] ; V-BIT SET,OVERFLOW
:40266
:40267 =1111 :1111-----:
:40268 WRITE.DEST ;
:40269 :-----:
:40270
:40271
:40272 14C5: :-----:
:40273 CVTRHL: ; CONVERT H TO LONGWORD AND ROUND
:40274 ; EXPECTS RCO-ID1 = SRC
:40275 SGN/CLR.SD+SS, ; CLEAR SIGN-FLIPFLOPS
:40276 SC_K[.30],FE_K[.30], ; POINTERS TO SRC-OPERAND
:40277 D_RC[0], ; D GETS LONG EXP
:40278 N&Z_ALU.V&C 0, ; USED ONLY TO CLEAR V BIT
:40279 CALL,J/CVTHI ; CALL CONVERSION ROUTINE
:40280
:40281 :-----:
:40282 14D5: ; RETURN WITH: D = INTEGER
:40283 ; Q<31>=ROUNDING BIT
:40284 ; SS = SIGN OF SRC-OPERAND
:40285
:40286 ALU 0(A),Q ALU.LEFT,SI/DIV, ; SHIFT Q<31> INTO Q<0>
:40287 SS?,J/CVTRDL.0 ; TEST SIGN-BIT, AND JOIN D-FORMAT
:40288 :-----:
    
```

U 1443, 0810,0039,7987,F900,01D4,7A38

U 1453, 0001,DA3C,0180,F800,0060,15AC

U 15AC, F000,003F,01F0,F847,0000,0300

U 15AE, 000C,003D,31F0,2C00,0000,0DFC

U 15AF, F000,003F,01F0,F847,0000,0300

U 14C5, 0810,0039,7987,F900,01D4,7A38

U 14D5, 0023,123C,02C0,F800,0000,041E


```

:40289 ; SUBROUTINE TO CONVERT FROM H-FORMAT TO INTEGER
:40290
:40291 ; EXPECTS:
:40292 ; RCO-ID1 = SRC H-FORMAT NUMBER
:40293 ; EXPECTS SC TO POINT TO RC[0], I.E. SC =.30
:40294 ; FE MUST BE .30 AS WELL
:40295 ; RETURNS:
:40296 ; D = INTEGER
:40297 ; Q<31> = ROUND BIT
:40298 ; RCO - ID1 = UNPACKED FRACTION PART
:40299 ; R15 = EXPONENT OF FRACTION (<=0)
:40300 ; SC = LOW 5 BITS OF EXPONENT
:40301 ; FE = # OF LONGWORDS OF FRACTION TO BE SHIFTED LEFT
:40302
:40303 ; RETURN10 IF ALL DATA IS CORRECT
:40304 ; RETURN11 IF FRACTION MAY NEED CLEARING
:40305 =00
:40306 CVTHI: ;00-----;
:40307 STATE K[.80], ; SET NORMALIZE-BIT OF STATE
:40308 CALL,J/UNPACK1H ; UNPACK SRC IN RCO-ID1
:40309
:40310 ;01-----;
:40311 D 0,Q 0, ; EVERYTHING IS 0
:40312 RETURN[11]
:40313
:40314 ;11-----;
:40315 =11 ;RETURN WITH:
:40316 ; RCO-ID1 = UNPACKED FRACTION (NORMALIZED)
:40317 ; SS=SD= SIGN
:40318 ; R15 = UNBIASSED EXPONENT
:40319 ; SC = LOW 10 BITS OF R15
:40320 ; ALU CC REFLECT R15
:40321
:40322 CVTHI.EMODH: ;ENTER HERE FOR EMODH
:40323 LAB_R[R15], ; LATCH UNBIASSED EXPONENT
:40324 ALU_LA.ANDNOT.K[.FF], ; TEST HIGH ORDER BITS
:40325 CLK.UBCC,WORD, ; CLOCK ALU CC ON HIGH BITS
:40326 ALU? ; TEST UNBIASSED EXP
:40327
:40328 ;-----;
:40329 =0011 ;BRANCH ON ALU N&Z BITS
:40330 ;0011-----; POSITIVE EXPONENT, INTEGER PORTION
:40331 ALU_LA-K[.A0]-1,CLK.UBCC, ;
:40332 J/CVTHI.20 ; TEST FOR EXP >=160
:40333
:40334 ;0111-----;
:40335 FE K[ZERO], ; NO LONGWORDS TO ALIGN
:40336 Q_RC[0], ; Q GETS FRAC <VMS> FOR ROUNDING
:40337 D 0, ; INTEGER = 0
:40338 RETURN10
:40339
:40340 ;1011-----;
:40341 FE K[ZERO], ; NO LONGWORDS TO ALIGN
:40342 Q_0,D_0,RETURN10 ; NEGATIVE EXPONENT
:40343 =:END

```

U 1A38, 0000,003D,4180,F800,1404,763A
 U 1A39, 0F00,003E,01F8,F800,0000,0011
 U 1A3B, 0018,5B24,4980,FA78,0010,1623
 U 1623, 0018,0008,2580,F800,0010,1640
 U 1627, 0F10,003A,19C0,F900,0104,6010
 U 162B, 0F00,003E,19FE,F800,0104,6010

```

ZZ-ES0AA-124.0 : GANDH .MIC [600,1204]
                                H 16
                                G & H floating point 14-Jan-82
                                Fiche 5 Frame H16
                                Sequence 1026
:40344 -----;
:40345 CVTHI.20:
:40346 FE K[.20],
:40347 D RC[TO],
U 1640, 0810,1B38,75F8,F900,0104,7617 :40348 Q_0,ALU? ; D GETS FRAC<VMS>
:40349 ; SHIFT IN 0'S
:40350
:40351 =0111 :0111-----;
:40352 D 0,Q 0,SET.V, ; NUMBER GT 2**160
:40353 RC[TO]_0,RETURN[11] ; REMEMBER TO CLEAR FRACTION
:40354
:40355 :1111-----;
U 161F, 0000,143C,7580,F800,0084,B976 :40356 SC_SC-K[.20], ; ALL OF EXP IS IN SC
:40357 SC? ; TEST SC<9:5>
:40358 =;END
:40359 =110 :BRANCH ON SC<9:5> NE 0
:40360 :110-----;
:40361 FE K[ZERO], ; NUMBER < 2**31
:40362 D_DAL.SC, ; FE GETS # OF LONG SHIFTS
:40363 Q_D, ; D GETS INTEGER, SHIFT'NG RIGHT
U 1976, 0D00,123C,19E0,F800,0104,7B6E :40364 SS?, J/CVTGI.4 ; Q GETS ROUND BIT
:40365 ; JOIN G-CODE
:40366 :111-----;
U 1977, 0000,143C,C1F0,2C00,0000,1986 :40367 Q ID[TO], ; 2**31<=NUMBER
:40368 SC? ; Q GETS FRACTION <AMS>
:40369 =;END ; TEST FOR SC NEGATIVE
:40370
:40371 =110 :BRANCH ON SC<9:5> NE 0
:40372 :110-----;
:40373 EALU SC, ; 2**31 <= NUMBER < 2**63
:40374 Q_D.OXT[BYTE].OR.PACK.FP, ; GET EXPONENT-32. FOR OVERFLOW CHK
:40375 ; GENERATE 8000 IF
U 1986, 0D0B,8030,01C0,F800,0000,1645 :40376 D_DAL.SC, ; INTEGER IS 8000000 AND SD = 1
:40377 J7CVTHI.3 ; D GETS INTEGER STILL
:40378
:40379 :111-----;
U 1987, 0000,003C,0180,F800,00A0,B641 :40380 SC_SC-FE, ; 2**63 <= NUMBER
:40381 SET.V ; SUBTRACT 32. FROM EXPONENT
:40382 =;END ; DEFINITELY OVERFLOW
:40383
:40384 :REMINDER:
:40385 ; D = FRAC <VMS> = RCO
:40386 ; Q = FRAC <AMS> = IDO
:40387 ; SC = EXPONENT-64.
:40388 ; FE = 32.
:40389 D RC[1], ; <Q,D> NOW EQUALS FRAC2,FRAC3
U 1641, 0810,1438,0180,F908,0080,B996 :40390 SC_SC-FE, ; SUBTRACT 32. MORE FROM EXP
:40391 SC?
:40392

```

```

:40393 -----:
:40394 =110 :BRANCH ON SC<9:5> NE 0
:40395 :110-----:
:40396 FE_K[.2], : 2**63 <= NUMBER < 2**95
:40397 D_DAL.SC, : NUMBER OF LONG WORDS
:40398 Q_D, : D GETS INTEGER
:40399 SS?,J/CVTGI.4 : NEEDED FOR ROUND BIT
:40400 : : TEST SIGN, JOIN G-CODE
:40401 :111-----:
:40402 Q_ID[T1], : 2**95 <= NUMBER
:40403 SC_SC-FE, : Q GETS FRAC4
:40404 SC? : SUBTRACT 32. MORE FROM EXP
:40405 =:END : : TEST IT
:40406 =110 :BRANCH ON SC<9:5> NE 0
:40407 -----:
:40408 D_Q,Q_D, : 2**95 <= NUMBER < 2**127
:40409 J7CVTHI.4 : <Q,D> NOW EQUALS FRAC3,FRAC4
:40410 -----:
:40411 SC_SC-FE, : 2**127 <= NUMBER < 2**160
:40412 D_0
:40413 =:END
:40414 FE_K[.4], : NO MORE FRACTION BITS
:40415 D_DAL.SC, : D GETS INTEGER
:40416 Q_0, : DO THIS FOR ROUND
:40417 SS?,J/CVTGI.4 : TEST SIGN, JOIN G-CODE
:40418 -----:
:40419 CVTHI.4:
:40420 FE_K[.3], : CLEAR 3 LOW LONG WORDS OF FRACTION
:40421 D_DAL.SC, : D GETS INTEGER
:40422 Q_D, : NEEDED TO ROUND
:40423 SS?,J/CVTGI.4 : TEST SIGN, JOIN G-CODE
:40424 -----:
:40425 :
:40426 CVTHI.3:
:40427 ALU_Q.XOR.K[.8000], : COMPARE WITH MOST NEG #
:40428 CLK_UBCC, LONG
:40429 -----:
:40430 :
:40431 SC_SC-K[.20] : LOWER EXP SO WE CAN GET ROUND BIT
:40432 -----:
:40433 :
:40434 FE_K[.1], : NUMBER OF WHOLE LONGWORDS TO SHIFT
:40435 : : FRACTION
:40436 Z? : INTEGER = MOST NEG NUMBER ?
:40437 -----:
:40438 :0-----:
:40439 =0 Q_ID[T0],SET.V, : NO THERE IS OVERFLOW
:40440 SS?,J/CVTGI.4 : JOIN G-CODE
:40441 -----:
:40442 :1-----:
:40443 Q_ID[T0], : YES, NO OVERFLOW
:40444 SS?,J/CVTGI.4
:40445 =:END :
    
```

```

:40446 .TOC " G & H floating point : H-FORMAT POLYNOMIAL EVALUATION"
:40447
:40448 ; THIS INSTRUCTION HAS TWO ENTRY POINTS, DEPENDING ON FPD.
:40449
:40450 14C3: -----;
U 14C3, 0800,003C,0180,FA08,0000,1649 :D_R[R1] ; THE NEXT SIX WORDS RELOAD THE PARTIAL
:40451 :-----;
:40452 :D[R0]_D ; PRODUCT FROM R0-R3 TO RCO-ID1
:40453
:40454 :-----;
U 1649, 0000,003C,C180,3C00,0000,164A :LAB_R[R0]
:40455
:40456 :-----;
U 164A, 0000,003C,0180,FA00,0000,164C :RC[R0]_LA
:40457
:40458 :-----;
:40459 :LAB_R[R2]
:40460
:40461 :-----;
U 164C, 0000,003C,0180,F980,0000,164D :RC[R1]_LA
:40462
:40463 :-----;
U 164D, 0000,003C,0180,FA10,0000,1650 :D_R[R3],
:40464 :SC_K[.FFF8] ; GET READY TO SHIFT IT
:40465
:40466 :-----;
U 1650, 0000,003C,0180,F988,0000,1651 :ID[R1]_D,D_R[R4] ; SETUP TO GET PC DELTA
:40467
:40468 :-----;
:40469 :D_DAL.SC ; PC DELTA NOW IN D<07:00>
:40470
:40471 :-----;
U 1651, 0800,003C,7180,FA18,0084,7652 :D_D-K[.1] ; ADJUST FOR THE ESCD
:40472
:40473 :-----;
U 1652, 0800,003C,C580,3E20,0000,1653 :00-----;
:40474 :PC&VA_D.OXT[BYTE]+PC, ; BYPASS SPECIFIERS
:40475 :CALL,J/SETFPD
:40476
:40477 :-----;
U 1653, 0D00,003C,0180,F800,0000,1654 :10-----;
:40478 :Q_PC,J/BAKUP.PC ; ENTER HERE ON READ ERRORS
:40479
:40480 :-----;
U 1A40, 0017,8015,0180,F801,0200,0E16 :11-----;
:40481 :J/POLYH.REEN ; REENTER MAIN LOOP BY READING ARGUMENT
:40482
:40483 :-----;
U 1A42, 0014,0038,01CC,F800,0000,0EB8 :
:40484
:40485 :-----;
U 1A43, 0000,003C,0180,F800,0000,18C0 :
:40486
:40487 :-----;
:40488 :
:40489 :
:40490 =,END
```

```

:40491
:40492      :-----:
:40493      : SUBROUTINE TO READ 4 LONGWORDS IN MEMORY
:40494      : STARTING AT VA, AND STORING THEM IN RC(SC),ID(SC),RC(SC+1),ID(SC+1)
:40495      : RETURNS SC = SC.OR.K[.30]+1
:40496      : VA = VA+K[.10]
:40496      =0**      :0**-----:
:40497      READ.H.SUBR:
:40498      D[LONG] CACHE,      : READ FIRST LONGWORD
:40499      SC SC.OR.K[.30],      : MAKE IT POINT TO TEMP AREA ON ID-BUS
U 1AC2, 0000,003D,7980,4000,0084,38F2
:40500      CALL,J/READH.SUBR.SUB      : SUBROUTINE WITHIN THIS ROUTINE
:40501
:40502      :1**-----:
:40503      D[LONG] CACHE,      : READ 3. LONGWORD
:40504      SC SC+1,
:40505      J/READH.SUBR.SUB
U 1AC6, 0000,003C,0180,4000,0080,D8F2
:40506      =:END
:40507      =0***      :0***-----:
:40508      READH.SUBR.SUB:
:40509      RC(SC) D,      : STORE FIRST LONGWORD IN RC(SC)
:40510      VA VA+Z,      : INCREMENT MEMORY POINTER
U 18F2, 0001,003D,0180,F83B,0000,1656
:40511      CALL,J/READ.CACHE.LONG      : SINGLE LINE SUBROUTINE
:40512
:40513      :1***-----:
:40514      ID(SC) D,      : STORE 2. LONGWORD IN ID(SC)
:40515      VA VA+Z,      : INCREMENT MEMORY POINTER
U 18FA, 0000,003E,0180,3403,0000,0004
:40516      RETURN4
:40517      =:END
:40518      :-----:
:40519      READ.CACHE.LONG:
:40520      D[LONG] CACHE,
U 1656, 0000,003E,0180,4000,0000,0008
:40521      RETURN[8]
:40522      :-----:
  
```

```

:40523 1685:
:40524 : ENTER HERE FOR POLYH WITHOUT FPD SET.
:40525 : EXPECTS : RC2-ID3 = PACKED ARGUMENT
:40526 : D = DEGREE
:40527
:40528 -----
:40529 D D.0XT[WORD],RC[6]_ALU, : STORE DEGREE IN RC6 TEMPORARILY
U 1685, 0803,403C,0580,F9B0,1404,7825 :40530 STATE_K[.1] : INITIALIZE STATE TO POLY-FLAG
:40531
:40532 =01****1:01****1-----
:40533 ALU_D.ANDNOT.K[.1F], : ISOLATE RESERVED BITS
U 1825, 0019,4025,8D80,F800,0010,047E :40534 CLK_UBCC,WORD, : EVALUATE TABLE ADDRESS
:40535 CALL,J/ASPC :
:40536
:40537 =11****1:11****1-----
:40538 RC[5] D, : SAVE TABLE ADDRESS IN RC5
:40539 Q_ID[2], : GET ARG LONG FRAC 1
U 1865, 0001,013C,C9F0,2DA8,0000,1AD2 :40540 Z? : TEST FOR ILLEGAL DEGREE (>31.)
:40541
:40542 -----
:40543 =0 : BRANCH ON ALU Z-BIT
:40544 :0-----
U 1AD2, 0000,003C,0180,F800,0000,0106 :40545 J/RSVOPR
:40546
:40547 :1-----
:40548 D_RC[2], : D GETS ARG LONG EXP
U 1AD3, 0810,0038,0180,F910,0000,1658 :40549 J7POLYH.I.1
:40550
:40551 -----
:40552 : ENTER HERE WITH ARGUMENT IN RC2-ID3
:40553 : TABLE ADDRESS IN RC5
:40554 : RC6 = DEGREE
:40555 : EXPECT D = RC[2]
:40556 : EXPECTS Q = ID[2]
:40557 POLYH.I.1:
U 1658, 0000,003C,6580,FA70,0000,1659 :40558 LAB_RSP,K[.10] : ALLOCATE STORAGE ON STACK FOR ARG
:40559
:40560 -----
:40561 ALU_LA-K[.10],
U 1659, 0018,0000,6580,F800,0200,165A :40562 VA_ALU
:40563
:40564 -----
:40565 CACHE_D[LONG] : WRITE LONG EXP ON STACK
:40566
:40567 -----
:40568 VA VA+4, : INCREMENT STACK ADDRESS
:40569 ALU_D.ANDNOT.K[.8000], : ISOLATE EXPONENT
U 165C, 0C19,4024,45E0,F803,0010,165D :40570 CLK_UBCC,WORD, : CLOCK ALU Z-BIT ON EXPONENT
:40571 D_Q,Q_D : D GETS LONG FRAC 0
:40572
:40573 -----
:40574 CACHE_D[LONG], : WRITE LONG FRAC 0 ON STACK
U 165D, 0000,013C,0180,3000,0000,1AD4 :40575 Z? : TEST FOR 0 EXPONENT
:40576
  
```


M 14	:	GANDH	.MIC	[600,1204]	G
N 14	:	GANDH	.MIC	[600,1204]	G
B 15	:	GANDH	.MIC	[600,1204]	G
C 15	:	GANDH	.MIC	[600,1204]	G
D 15	:	GANDH	.MIC	[600,1204]	G
E 15	:	GANDH	.MIC	[600,1204]	G
F 15	:	GANDH	.MIC	[600,1204]	G
G 15	:	GANDH	.MIC	[600,1204]	G
H 15	:	GANDH	.MIC	[600,1204]	G
I 15	:	GANDH	.MIC	[600,1204]	G
J 15	:	GANDH	.MIC	[600,1204]	G
K 15	:	GANDH	.MIC	[600,1204]	G
L 15	:	GANDH	.MIC	[600,1204]	G
M 15	:	GANDH	.MIC	[600,1204]	G
N 15	:	GANDH	.MIC	[600,1204]	G
B 16	:	GANDH	.MIC	[600,1204]	G
C 16	:	GANDH	.MIC	[600,1204]	G
D 16	:	GANDH	.MIC	[600,1204]	G
E 16	U	163C, 0810, 0038, B180, F830, 00			
F 16	:	GANDH	.MIC	[600,1204]	G
G 16	:	GANDH	.MIC	[600,1204]	G
H 16	:				
I 16	:	GANDH	.MIC	[600,1204]	G
J 16	:	GANDH	.MIC	[600,1204]	G
K 16	:	GANDH	.MIC	[600,1204]	G
L 16	:	GANDH	.MIC	[600,1204]	G