D I G I T A L E Q U I P M E N T C O R P O R A T I O N

AURORA PROGRAM BUSINESS PLAN

At Exit From Phase 0

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INTRODUCTION

The Aurora Program is a central engineering effort directed by the Polaris (BI Systems) Development Group in the 32-Bit Systems organization. To put Aurora into perspective, it is helpful to understand the overall mission of the Polaris Program:

1. to develop a set of competitive, profitable, high-quality VAX systems products and options for the $16K to $200K price range for both the end-user and OEM markets

2. to use the system components wherever possible for the OEM board and box market

3. to make these systems attractive for third party hardware and software vendors who make complementary products

To achieve these goals, Polaris (currently Aurora and Scorpio systems) will develop and use a common BI bus structure, being developed within the program, across a range of systems. Aurora is the system which will drive VAX into new low-end markets and which will introduce the BI bus, the Unibus I/O replacement for future VAXes. Aurora is targetted at the $16 - 40K price band. Scorpio will cover the $40 - 200K price band and is the mid-range product. At the high end, Nautilus (a separate development effort within 32-Bit Systems Engineering) will also be BI-based. Thus, the BI will become the DEC bus of the future, and hopefully, as an open bus, a true industry standard.

The Aurora Program involves development efforts in several engineering organizations:

1. the MicroVAX and BI chips by Semiconductor Engineering

2. the Aurora memory array modules, RD52-53 (and follow-on) 5 1/4" disks, and MAYA tape by Storage Systems Engineering

3. MicroVMS, MicroULTRIX, VAXELAN operating systems by Software Systems Engineering

Polaris Engineering has responsibility for:

- Specifications for the BI bus and BI interface chip

- the BI physical interconnect

- the BI power and packaging

for the corporation.

Aurora Engineering has responsibility for specific deliverables which include the Aurora CPU board, Aurora I/O board set, and Aurora systems based on these components. The Aurora Project Team consists of the above engineering groups as well as Manufacturing and Customer Services.

This document, which follows DEC STD 130 (Business Plan, Rev B, 3 December 1981), summarizes the product goals, defines and describes deliverables and schedules, and provides preliminary forecasts and financial analyses.

Accompanying documents include:

- Marketing/Product Requirements
- Product Requirements
- Manufacturing Impact Statement
- Customer Services Impact Statement
- Preliminary System Specification
- Preliminary Project Plan

(although the latter are not formally required at Phase 0).

As Aurora represents a major new system product offering with major impact on corporate profitability and strategy, offering, you are encouraged to consult the Business Plan Reference Documents (Chapter 7) for additional related information.

CHAPTER 1 EXECUTIVE SUMMARY

1.1 PRODUCT DEFINITION

Aurora is a low-end VAX, its CPU being implemented on a single module. However, Aurora as a generic term currently encompasses three separate Digital products: Aurora board sets, Aurora systems, and Aurora based VAXstations. Although this document focuses specifically on Aurora boards and Aurora systems, certain information and forecast data emcompasses VAXstations (1) to identify the total market breadth and potential volume magnitude of the Aurora CPU, and (2) to overcome a current product definition ambiguity of Aurora systems in a workstation application vs VAXstations in the same application. For additional information about the Aurora VAXstation, contact Bruce Campelia, VAXstation Product Manager.

The Aurora CPU utilizes the MicroVAX chip and interfaces to the new Backplane Interconnect (BI) bus. The BI has a 13.3 MB/sec bandwidth, implements a new Euro-compatible module form factor, and directly supports multiple processors. There is a custom two-chip interface also being designed for this bus (as part of the "umbrella" Polaris Program). Refer to Chapter 2.2 for a diagram of the system architecture.

The design center for system packaging is a desk-height pedestal, compatible with open-office environments. There is room for up to four 5 1/4" storage devices, initially an RX50 floppy disk, and up to three RD53 50+ MB Winchester disks, with optional streaming tape (MAYA) for a backup device. As storage technology improves, lower cost/higher performance storage subsystems can easily be accommodated, with provision being made for optical disks and half-height devices.

It is hoped that future product offerings will include a 10.5" OEM Box with slides and a Eurocard Rack Mount, although these are not currently deliverables at FRS. For the purposes of realistic financial analyses, an OEM box has been forecast as it is urgently requried, especially in government and OEM markets.

1.2 PRODUCT GOALS (Non-prioritized)

1.2.1 Marketing Goals

1. Drive VAX systems into new low-end markets--specifically via board sets, VAXstations and open office compatible systems in hardware, and the VAXElan run-time system, and MicroVMS/MicroUltrix operating systems in software.

2. Introduce and ensure acceptance of the BI bus, the Unibus I/O replacement for future VAX systems. Pursue making the BI an industry standard 32-bit bus.

3. Announce Aurora MicroVMS system with an MLP of less than $20,000; announce the Aurora CPU module with an MLP of less than $3,000.

4. Ensure local language "country kits" are available at FRS.

5. Establish a corporate open-office enclosure family common to Aurora and Scorpio systems.

6. Ensure Aurora systems are easily installable, diagnosable, and repairable, adding up to low cost-of-ownership over the life of the product.

7. Ensure an aggressive add-on/upgrade program helps establish Aurora as a true industry standard BI/MicroVAX solution.

8. Help penetrate new markets and application with other Digital products areas such as artifcial intelligence tools (languages, graphics).

9. Achieve the above goals in conjunction with responding to the Product Groups' mandate of "time-to-market" and "cost/performance" as critical product/market requirements.

10. Make these systems attractive for third party hardware and software vendors who make complimentary products.

1.2.2 Engineering Goals

1.2.3 Manufacturing Goals

1.2.4 Service Goals

Because of the critical importance of a JOINT Engineering/Manufacturing/Service TEAM approach to the successful development and introduction of Aurora, the entire Aurora Program is committed to the following priorities, which have been jointly set:

RANK	PRIORITY	TARGET
1	QUALITY/RELIABILITY	See Below
2	TIME-TO-MARKET	8 Quarters
3	COST	$5K (System)
4	FUNCTIONALITY	MicroVAX SRM
5	PERFORMANCE	90% 11/780

1. QUALITY/RELIABILITY--Quality and Reliability goals including MTBF and MTTR have been established based on an analysis of competitors' products and other VAX family members

   - Mean Time Between Failures (MTBF) = 10,000 hours or 17.4 months for Aurora Kernal without maintenance service at 100% duty cycle
   - Average Mean Time to Repair (MTTR) < 1.5 hours
   - Problem Installations < 5%
   - Dead on Arrivals < 2%
   - Basic Monthly Charges (BMC):
     Aurora Kernal = $53.
     Aurora 8-user system = $97.

2. TIME-TO-MARKET--The Aurora Program officially began in Q3FY83 (January) and the current schedule commits an FRS in Q3FY85. The program strategy is to maintain the VLSI chip availability as the critical path. All decisions will be made with the objective of keeping other program paths within the timeframe of the DC chip schedules.

3. COST--The desired pricing for the pedestal system is in the $16-17K range. In keeping with a mark-up objective of 3-3.5, the target transfer cost is $5K. Low total cost of ownership is a key goal of Aurora. Low cost to Digital is also (e.g. Aurora requires no preventive maintenance).

4. FUNCTIONALITY--The VAX compatible subset functionality is defined in the MicroVAX System Reference Manual.

5. PERFORMANCE--The expected performance is between 70% and 90% of the 11/780 for native MicroVAX instructions when using on-board memory. The target is 90% with the MicroVAX CPU chip being the dominant factor.

1.2.5 FINANCIAL GOALS

The following financial goals result from BURP analysis incorporating AURORA transfer cost and markup goals:

1. Net Present Value (NPV) = $64.7M @40%

   The goal is to maximize Net Present Value given the constraints of introducing a new 32-bit board product, a new VAX bus architecture, a new MicroVAX architecture and increasing market share in open office and workstation applications.

2. Internal Rate of Return (IRR) = $61.8%

   The goal is to exceed the engineering new product hurdle rate of 40%.

3. Profit Before Tax (PBT) based on BURP Analysis = 33%.
   = $1.6 Billion

1.3 RELATIONSHIP TO CORPORATE PRODUCT STRATEGY

Corporate Product Strategy statements (per Engineering Strategy Overview -- March 1982) and Aurora relationships:

1. "Adopt a single VAX-11/VMS architecture."

   Aurora, in addition to providing complete conformance to MicroVAX architectural specifications also extends this architecture via the introduction and definition of the BI bus and its physical interconnect implementation. The BI, which inherently supports multiple processors, is the primary bus structure of both Aurora and Scorpio. In addition, on future VAXes the BI (through bus adaptors) will replace the Unibus as a system I/O bus.

2. "Implement a wide price range of products covering the computing styles of personal (individual) computing, timeshared departmental computing, and central computing."

   Aurora extends VAX applicabiltiy into new low-end markets via three new low-end products: boards, systems and VAXstations. Additionally, further low-end extensions may be achieved through future system implementations of the MicroVAX chip.

3. "Interconnect these in a homogeneous network, including the formation of personal computer clusters."

   Aurora will contain an integral NI interface, requiring only an H4000 transceiver to complete a network connection. NI interconnect via an I/O processor is provided by the BNA when available. CI capability is not planned as part of this project.

4. "Build critical and unique applications."

   The Aurora pedestal system is the first VAX specifically designed for open-office compatibility. Aurora Vaxstations will be marketed as single-user and multi-user VAX workstations. Aurora boards with VAXElan wll become customer tools for unique application implementation. The combination of low price, office environment compatibility and NI support presents the beginning of DEC Local Area Networks (LAN) with "private" VAX computers. The introduction of "office" software on MicroVMS will permit sales of entry VAX systems with word-processing that are easily expanded via the LAN cluster concept.

Additionally, please reference the VAX Strategy Book (Spring '83), Chapter 5, for further detail on Aurora and Corporate Product Strategy).

1.4 NUMERICAL HIGHLIGHTS*

FY'85 - FY'90 Base Data		Schedule: Q/FY	Financial Metrics
# CPU Boards Shipped	57,295	Announcement: Q2FY'85	# Qtrs to Payback from System FRS: 10 Qtrs
# Total Systems & Boards Shipped	136,000	CPU Boards FRS: Q3 FY'85	
FY'85 - FY'90 NOR	$4.7B	Systems FRS: Q3 FY'85	Development Cost % NOR: 2.3%
Gross Margin %NOR	59%	Prod Availability: TBD	NPV @ 40%: $64.7M
PBT % NOR	33%	Cash Payback: Q2 FY88	IRR: 61.8%
		Last Ship: FY'93	

SYSTEM CONFIGURATIONS (VAX/VMS LICENSE-ONLY)

	Entry System	TypicalSystem	Large System
Maynard List Price	$14K	$21.0K	$34.5K
Transfer Cost	$3.5K	$5.4K	$9.3K
Memory (MB)	1 MB	1 MB	5 MB
Disk Type - MB	.8 MB	50MB	100MB
Tape Type	None	MAYA	MAYA
Performance (11/780 = 1.0)	.8 - .9	.8 - .9	.8 - .9

CRITICAL DEPENDENCIES

Critical dependencies for a successful Aurora program include:

1. Sufficient program funding.
2. Semiconductor technologies and CAD tools to ensure the availability of the MicroVAX chip, BI interface chips (BIIC, BCI3) and NI chip set.
3. Achieve transfer cost goals of $58 for the MicroVAX chip and $45 for the BIIC and BCI3 in FY'86.
4. Optimal architecture and implementation of the BI bus physical interconnect.
5. Availability of VAX/MicroVMS, MicroULTRIX, and VAXElan at FRS.
6. Availability of a full complement of native BI peripherals and controllers prior to the availability of same from external vendors.

* Forecast data includes Aurora boards and systems. Forecast source is Aurora systems product management.

1.5 MARKETING STRATEGY

Aurora will be a general purpose system adaptable to all VAX technical and commercial applications. At the system level, it will be a lower price replacement for the current 11/725, 11/730, and 11/750. Aurora also provides a clear upgrade migration path from 16-bit and Q-bus to BI systems. The marketing message will stress the enhanced VAX price/performance, networking and high I/O bandwidth compared to previous VAX offerings. These improvements, combined with the compatibility and transportability of VAX/VMS applications across the entire VAX Family will make Aurora a very appealing system both for new customers and for migrating existing VAX customers.

Primary markets for Aurora will include technical, commercial and OEM customers with applications which:

* are price sensitive
* are space constrained
* require high speed real time I/O
* require single and multi-user workstations
* lend themselves to Local Area Networking

The Aurora system competitive advantages will occur in the areas of:

* Price/Performance
* MicroVMS, MicroULTRIX and VAXElan compatibility
* Layered Software
* Ease of installability, maintainability
* BI family of products with Scorpio and Nautilus
* Ease of networking
* Low cost of ownership
* Applicability to a broad range of compute requirements
* High speed I/O for custom applications
* Large VAX installation base with applications software

1.5.1 FORECASTING PROCEDURES AND RISK MANAGEMENT

The Aurora demand forecast is a top-down forecast, specifically, the projected volumes within certain defined price range boundaries. As with any top-down approach, the overriding risk is in the correct projection of the size of the total available market (TAM). The Aurora specific case is based upon the following assumptions, all of which have been developed in conjunction with the 32-Bit Base Product Marketing Group and the MicroVAX Program Office:

1. Aurora systems will be sold in the $16 - 40K price band

2. The DEC marketshare within this price band will grow to 20% by 1990.

3. The total available market will grow approximately 27% per year through 1990.

Thus, the major risks inherent in the demand volume projections are:

1. TAM projections could be overstated or understated
2. DEC either fails to maintain or exceeds market share projections
3. The underlying economic growth projections upon which risk 1 and risk 2 depend are either too low or too high.

Although Aurora has been prudent in projecting demand in the face of the given assumptions, some downside and upside risk obviously exists. While the effect of this risk is difficult to quantify exactly, several different scenarios have been analyzed in order to bound the range of alternatives. For the purposes of Phase 0 financial analyses, we have selected the "opportunity space" alternative.

However, recognizing the importance of good planning when manufacturing in such high-volumes, we and Manufacturing have also agreed upon a "Baseline" scenario which represents a lower bound on the forecast. Using this additional approach, which is also reflected in the Manufacturing Impact Statement, Manufacturing is now able to deal with suppliers with consideration of "Baseline Plus Upside (or Downside) Potential". Until real data begins to help us tune the model (as every forecasts should be a "living" model), it will be difficult to project such industry trends as:

- movement from -16 to -32 bit
- movement from Q-bus and Unibus to BI
- movement to MicroVAX from 68000+
- movement to VAX workstations

We hope that manufacturing can more effectively manage the risks associated with plant loading parts, supply, heavy investment in test equipment, staffing by knowing "up front" that we jointly must build an inherently flexible series of modules and continually monitor reality against them.

Our sensitivity analysis has also included study of the "baseline" scenario and is referenced in Chapter 5. Full details will be made available in a later revision of this plan.

1.5.2 MARKET SIZE

The matrix below is based upon a semi-logarithmic market price band segmentation model which defines market segments as a function of system sell price. Total Available Market (TAM) size estimates have been provided by the 32 bit Base Product Marketing group, using data compiled from industry analysis of such research groups as International Data Corporation (IDC), Arthur D. Little, Dataquest, Gnostic Concepts, the Gartner Group and other similar industry indicators. These TAM estimates are for NES (Net Equipment Sales) of domestic manufacturers of systems. Aurora systems will be sold in the $16-40K price band. Further detail is available in Chapter 3.

$16 - 40K Total Market in Units (000's)	FY84	FY85	FY86	FY87	FY88
	160	210	275	340	420
Total DEC Share Goal	20%	20%	20%	20%	20%
DEC 16-BIT SHARE	17%	5%	5%	1%	1%
DEC 32-BIT MARKETSHARE GOAL	3%	15%	15%	19%	19%
$16 - 40K DEC UNITS (000's)	4	31	40	65	80
SEAHORSE	2	14	0	0	0
MAYFLOWER	0	9	25	30	25
AURORA	0	2	14	35	55
11/725	2	6	1	0	0
AURORA NES (@3.5 MARKUP)		$78.4M	$550.6M	$1,388B	$2,203B

1.5.3 Applications (Market Segmentation)

The following is a summary of targeted application areas for Aurora:

Application/Segment Description	Marketing Message	Channels Product Group
Components OEM; End User In-House System Assembly (many actual application areas)	First VAX board set.	OEM Groups TVG--Micros
Technical System OEM; Systems House (many actual application areas)	VAX system for < $20K	OEM Groups TVG--Systems
VAXElan Program Development	Least expensive VAX system	OEM Groups TVG--Micros, TVG--Systems
Professional Workstation*	In-expensive single user VAX workstations with integral NI	CAEM, LDP
General Business/EDP and Office Automation	Small system member of large family.	OEM Groups, GSG, CAEM, BOS
Front-End Real-Time	Best VAX price/performance	GSG, LDP, CAEM
Network Servers	Best VAX price/performance	GSG, LDP, CAEM

* Aurora systems (in addition to Aurora VAXstations) will be purchased as "workstations".

1.5.4 Geographic Considerations

1. Distribution: Aurora boards and Aurora systems are planned to be sold in every country served by Digital and its distributors. Anticipated distribution by area is as follows:

   - Aurora Boards

U.S.	60%
Europe	30%
GIA	10%

- Aurora Systems

U.S.	60%
Europe	30%
GIA	10%

2. Product Variants

Aurora is being designed as a truly international product.

- Country Kits: The implementation of local language kits is planned at FRS, including local language diagnostics, error message ROM's, cables and power cords.

1.6 PHASE PLANNER

AURORA phase transition dates are as follows:

Phase	Date of Exit from Phase (Q/FY)
0 (Strategy & Requirements)	November 1983
1 (Planning)	Q3 FY84
2 (Implementation)	Q4 FY'84
3 (Qualification)	Q4 FY'85
4 (Production and Support)	TBD
5 (Retirement)	TBD

1.7 RISK ASSESSMENT

The asterisk (*) on each of the following scales indicated the relative risk associated with that subject.

Low Risk ____*____ High Risk
0 1 2 3 4 5 6 7 8 9 10

1.7.1 Technology

AURORA SYSTEM

- For Industry

Well established, know how to do ____*____ Never done before
0 1 2 3 4 5 6 7 8 9 10

- For Digital

Well established, know how to do ____*____ Never done before
0 1 2 3 4 5 6 7 8 9 10

COLOR WORKSTATION

- For Industry

Well established, know how to do — 0 1 2 3 4 5 6 7 8 9 10 — Never done before

- For Digital

Well established, know how to do — 0 1 2 3 4 5 6 7 8 9 10 — Never done before

WORKSTATION SOFTWARE

- For Industry

Well established, know how to do — 0 1 2 3 4 5 6 7 8 9 10 — Never done before

- For Digital

Well established, know how to do — 0 1 2 3 4 5 6 7 8 9 10 — Never done before

1.7.2 Manufacturing

- Test Procedures

Well established — 0 1 2 3 4 5 6 7 8 9 10 — New techniques

- Processes

Well established — 0 1 2 3 4 5 6 7 8 9 10 — New

1.7.3 Service

Similar to many products, high ease of diagnosis — 0 1 2 3 4 5 6 7 8 9 10 — New techniques, new service procedures, much training, sparing

1.7.4 Marketing

- Distribution Channels

Traditional end-user direct sales, or OEM/reseller; standard terms and conditions	0 1 2 3 4 5 6 7 8 9 10 (*)	New distribution channels, new terms and conditions, new order processing procedures

- Customer Base

Current Digital customers	0 1 2 3 4 5 6 7 8 9 10 (*)	New Digital customers

- Customer Capability

Highly technical	0 1 2 3 4 5 6 7 8 9 10 (*)	Computer naive

- Applications

  - Graphics Workstation

Well Understood, done before	0 1 2 3 4 5 6 7 8 9 10 (*)	New Applications

- "Solutions" Software Packages

Well Understood, done before	0 1 2 3 4 5 6 7 8 9 10 (*)	New Applications

- "Traditional" Computing

Well Understood done before	0 1 2 3 4 5 6 7 8 9 10 (*)	New Applications

1.8 PROGRAM ISSUES

The following are currently identified as AURORA program issues requiring resolution:

- Availability and performance of processor and interface chips
- Volume availability of 256K-bit RAM's allocated to AURORA
- 50+ MB Winchester disks with ST506 interface by AURORA FCS
- Volume availability and operating system support of streaming tape backup device
- MicroVMS support at FCS
- Integrated workstation availability at FCS of AURORA system
- Aggressive applications software support at FCS
- Diskless system support for down-line load.

CHAPTER 2 PRODUCT DESCRIPTION

2.1 PRODUCT LIFE CYCLE OVERVIEW

2.1.1 Product Offerings and Potential Migration Strategy

The following matrix defines the FRS and primary shipment years (denoted by an ("X") of the anticipated Aurora products:

AURORA PRODUCT	FY85	FY86	FY87	FY88	FY89	FY90	FY91	FY92
CPU Board	Q3	X	X	X	X	X		
AIO/AIE Boards	Q3	X	X	X	X	X		
Memory Boards	Q3	X	X	X	X	X		
OEM Box	Q4	X	X	X	X	X		
Single RD53 System	Q3	X	X	—	—	—		
Dual RD53 System	Q3	X	X	—	—	—		
RD53/MAYA System	Q3	X	X	—	—	—		
Eurocard Rack	—	X	X	—	—	—		
Single RDZX System	—	—	X	X	X	X		
Dual RDZX System	—	—	X	X	X	X		
RDZX/MAYA System	—	—	X	X	X	X		
	—	—	X	X	X	X		
Optical Disk Systems	—	—	—	X	X	X		
Aurora VAXstation	—	Q1	X	X	X	X		

2.1.2 Affected and Successor Products

The primary products affected by Aurora are the VAX-11/725, VAX-11730, and VAX-11/750. Successor products may include V-11 based CPU's in the Aurora pedestal and Aurora CPU's in the H9640 cabinet with RAxx disks. More 5 1/4" disk capacity in an Aurora expander cab is also being considered.

More detail will be provided in a later revision of this plan.

2.2 KEY FEATURES -- INITIAL PRODUCT OFFERINGS

2.2.1 Initial Aurora Architecture

The heart of the Aurora architecture is the new Backplane Interconnect (BI) bus, a bus optimized for bandwidth, multiple processors, integrity and RAMP. Integral to the BI is a new physical interconnect scheme which includes a new Euro compatible module form factor of 8.00" x 9.18".

The processor, memory, and I/O modules conform to this new module size. The processor and I/O modules connect directly to the BI, while memory connects to a private Aurora Memory Interconnect bus. A diagram of the Aurora System follows on the next page.

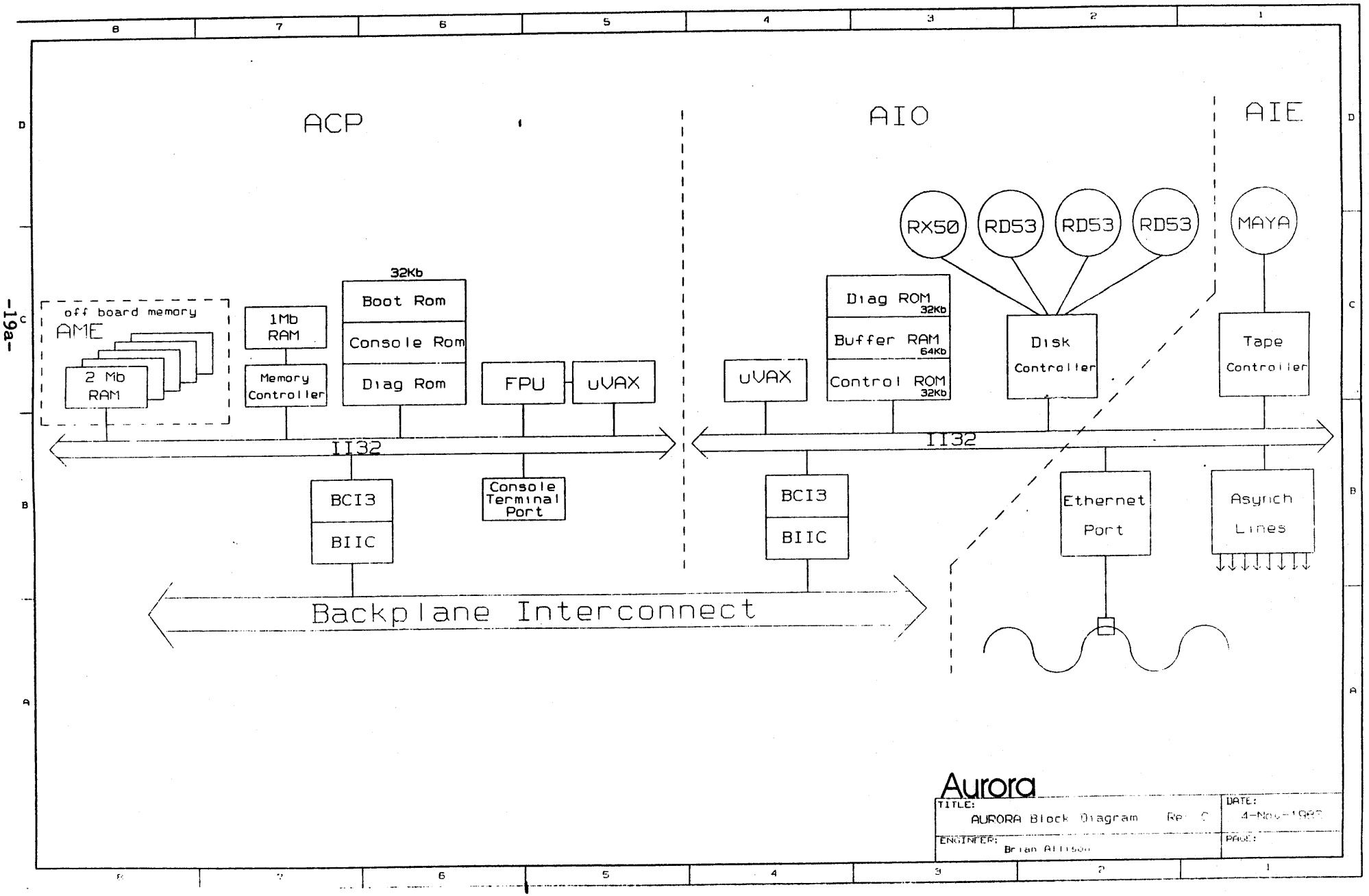
2.2.2 System Component Descriptions

Three levels of products will result from the Aurora project: components, options, and systems. Components are intended for OEMs who will build their own systems. A component consists of a piece of hardware (such as a single module), along with minimal or no documentation. Options are intended for additions to existing DEC systems, although they may also be used for additions to OEM systems. An option consists of a component, plus cables and distribution panels to marry the component to a system. Each option includes full documentation for installation, verification, and operation of the option, as well as a technical description of the option. Systems are integrated pre-configured packages, ready to run. Packaged systems will typically be shipped with software. The operating systems available for Aurora systems will be MicroVMS, MicroULTRIX, and VAXElan.

A. COMPONENT PRODUCTS

The following components will be available within 6 months of FCS.

- Aurora Central Process Module (ACP).
- Aurora Memory Extension Module (AME).
- Aurora I/O Module (AIO).
- Aurora I/O Extension Module (AIE).
- Aurora Power Supply (The power supply may be sold by our vendor directly to OEM customers).
- Aurora Control Panel assembly.
- Eurorack to accept BIcage assemblies.


ACP
AIO
AIE
off board memory
AME
2 Mb RAM
1Mb RAM
Memory Controller
32Kb
Boot Rom
Console Rom
Diag Rom
FPU
uVAX
II32
BCI3
BIIC
Console Terminal Port
Backplane Interconnect
RX50
RD53
RD53
RD53
MAYA
Diag ROM 32Kb
Buffer RAM 64Kb
Control ROM 32Kb
Disk Controller
Tape Controller
uVAX
II32
BCI3
BIIC
Ethernet Port
Asynch Lines
Aurora
TITLE: AURORA Block Diagram Rev C
DATE: 4-Nov-1982
ENGINEER: Brian Allison
PAGE:

The following component products are deliverables of the Scorpio program but are relevant to Aurora OEM customers. FCS of these components is TBD. These components are described in detail in the Scorpio system specification:

- A six-slot BI backplane
- A six-slot BI/cage (BI backplane and cardcage)

The following component products are deliverables of the Storage Systems group and may be of interest to Aurora OEM customers.

- RX50 800Kb floppy disk
- RD53 50Mb Winchester disk
- MAYA 100Mb streaming magtape

B. OPTION PRODUCTS -

The following options will be available within 6 months of FCS:

- Aurora Memory Extension module (AME)
- Aurora I/O Extension module (AME) with distribution cable and panel
- RD53 50Mb Winchester disk
- MAYA 100Mb streaming magtape
- Power supply/cardcage/BI backplane assembly

C. SYSTEM PRODUCTS -

The following system products will be offered. It is expected that the pedestal system will FRS about 6 months before the OEM Box.

PEDESTAL SYSTEM -

This configuration is targetted at the open office environment. It can have up to 150Mb of disks (presuming the RD53 is 50Mb), and will support 8 - 24 users. The acoustic noise level will be 5.5 bels or less (this is much quieter than any computer currently manufactured by DEC with exception of the 11/725).

The pedestal system will be a complete VAX in a 14" wide, 28.5" deep, 28.25" high (including castors) box. Standard features include:

- A six-slot BI backplane and cardcage
- ACP processor module with 1Mb parity memory
- AIO module capable of interfacing to 1 RX50 and 3 RD53s

- RX50 800Kb floppy disk
- RD53 50Mb Winchester disk
- 400 watt power supply
- Reserved power and space for either 2 additional RD53s or 1 additional RD53 and 1 MAYA magtape drive

OEM BOX -

This configuration is targetted at Original Equipment Manufacturers who will install the OEM box in a cabinet, using the rack-and-stack approach. The OEM box is a 10.5" x 19" slide-mounted box which contains.

- A six-slot BI backplane and cardcage
- ACP processor module with 1Mb parity memory
- AIO module capable of interfacing to 1 RX50 and 3 RD53s
- RX50 800Kb floppy disk
- A control panel sub-assembly
- A bulkhead distribution panel for connection from the processor module to a console terminal
- Power supply and fans
- Reserved space and power for either a Unibus sub-assembly or for a BI expander

2.2.2.1 Aurora Processor Module: Aurora Central Processor Module (ACP)

All Aurora systems have at least one Aurora Central Processor module (ACP). The ACP board provides the Aurora system with its compute engine and is comprised of these various parts:

A. MicroVAX CPU -

The ACP compute power is provided by a 68 pin ZMOS MicroVAX chip being designed by DEC Hudson. It executes the MicroVAX instruction set as defined by DEC Standard 32. The MicroVAX chip will be clocked at 20Mhz with a microcycle time of 200ns. This should provide about 0.9 times the processing power of a VAX 11/780 for the implemented instructions. The MicroVAX chip communicates with the rest of the logic on the module with a set of signals which form a bus called II32. The MicroVAX chip is the arbitrator of this bus and is capable of being interrupted at 4 different hardware levels. It also has the capability of relinquishing control of the II32 to other "master" devices who can do DMA accesses.

B. Floating Point Unit -

The floating point instruction processor is a slave chip to the MicroVAX chip that will execute the VAX D, F and G floating point instruction types. Instruction execution speeds will be about 0.9 times the speed of an 11/780 floating point accelerator option. If the floating point chip is not present the MicroVAX chip will trap to a software routine that may emulate the floating point instructions.

C. Memory controller and 1Mb RAM -

The memory controller logic interprets II32 read/write commands and provides the proper control signals to a bank of 36 256K dynamic RAMs to execute the commands. Parity bits are generated on all writes and checked on all reads to provide error detection. The MicroVAX chip may read or write memory in 400ns. The BI interface reads or writes memory in 600ns. There is also logic to generate a private memory interconnect. This allows up to 5 Aurora-unique memory array cards to connect to the memory controller, allowing multiple ACP modules to be uniquely addressed by the BI.

D. Console Terminal Line -

An RS232 asynchronus communications line is provided for a console terminal. This line is capable of software selectable speeds up to 38.4K baud. Extra signals will be supplied to the distribution panel to allow manufacturing to hard select a baud rate for SAVES/APT. A break detected on this line will force the MicroVAX to pass control to a console program contained in ROM which will interpret and execute VAX console commands as described in Aurora Console Specification. (Note... The traditional VAX RXCD and RXCS registers are implemented as CSRs instead of IPRs on the ACP module).

E. TOY Clock -

A time of year clock is provided so correct time and date information is maintained while the system is powered off. Power to the circuit will be provided for at least 100 hours. There are also 60 bytes of RAM in the circuit that are used by the console program to store system defaults when power is removed from the system.

F. Self Test Diagnostic ROMs -

TBD K bytes of ROM storage are included which contain a self test program that is executed upon power up or board initialization. This test will attempt to verify proper operation of all logic on the ACP board and all logic on AME array cards. This test will complete in TBD seconds when the ACP is the primary processor in a system and will complete within 10 seconds when the ACP is not the primary processor.

G. BI Interface -

The BIIC and BCI3 chips provide an interface to the BI bus. This allows the MicroVAX processor to access memory and device CSRs not local to the ACP. It also allows memory on the ACP or AME boards to be accessed by other nodes on the BI. When data is read from the ACP or AME memory a "don't cache me" message is transmitted with the data to allow cached BI nodes to function properly with the ACP module. (At present the KDZ processor module ignores the "don't cache me" message and may not work properly in a system with an ACP module).

2.2.2.2 Aurora Memory Array: Aurora Memory Extender Module (AME)

The AME board is an Aurora unique memory array that interfaces to a buffered, parity protected version of the II32 that is generated by the memory controller portion of the ACP module. Current plans are to put 2Mb of 256K RAMs on the AME module. The company wide shortage of 256K RAMs may force the use of 64K SIP mounted RAMs which would only provide 1 Mb of storage. This is very undesirable because of the higher power consumption and increased cost per Mb this would cause. The AME module is being designed by the Storage Systems group in Maynard/Shrewsbury.

2.2.2.3 Aurora I/O Module (AIO) -

The AIO board provides a BI interface for RX50 floppies and RDxx drives which talk ST506/ST412 at 5Mhz. 1 Floppy will be supported and up to 3 RDxx drives will be supported. The AIO module also provides an interface to the Aurora I/O Extension (AIE) module for additional I/O interfaces. There are 16 CSRs accessable over the BI that control the operation of the AIO/AIE.

A1. MicroVAX CPU -

The AIO board uses a MicroVAX chip to do all control functions. The MicroVAX chip interprets all MSCP, TMSCP and NI messages. It also maintains all CSRs visible over the BI and initiates all data transfers over the BI. The MicroVAX chip will be clocked at 20Mhz with a microcycle time of 200ns. The MicroVAX chip communicates with the rest of the logic on the module with a set of signals which form a bus called the II32. The MicroVAX chip is the arbitrator of this bus and is capable of being interrupted at 4 different hardware levels. It also has the capabiltiy of relinquishing control of the II32 to other "master" devices who can do DMA accesses to local memory.

A2. Control ROM -

32Kb of control ROM will be available for the VAX code to communicate with all peripherals and the BI. The control code for the devices on the slave AIE board will also reside in this ROM. The MicroVAX will be able to access ROM code/data in 400ns. There will be no parity protection but there will be a ROM checksum that will be verified by the self test diagnostics.

A3. Buffer RAM -

32K bytes of static RAM are available to the control programs to buffer data between system memory and the peripheral devices. Some portion of this RAM is also used for storage of variables for the control program. The MicroVAX chip may read or write RAM in 400ns. The BI interface reads or writes RAM in 600ns. Because this is static RAM located on the same board as the microprocessor chip there is no parity protection.

A4. Self Test Diagnostic ROM -

32K bytes of ROM storage are included which contain a self test program that is executed upon power up or board initialization. This test will attempt to verify proper operation of all logic on the AIO, (and AIE if present). The module self test will complete in 10 seconds or less. There will also be tests for the winchester disks that will be run after the disks have spun up. The status of this test will be checked by control program before a MSCP online command is allowed.

A5. Disk Controller -

The AIO board provides an interface to 1 RX50 800Kb floppy disk drive and up to 3 RDxx winchester disk drives. It is expectd that at FCS the RD53 will be available at a capacity of 50-70Mb. The control program will accept MSCP commands from the host and translate them into the appropriate CSR level commands to access the disks. The winchester disks will be formatted with a sector interleave factor of 1 to maximize long transfer times. Short transfers will be dominated by the access time of the disk, (expected to be about 30Ms). The disk controller logic is capable of overlapped seeks but only 1 disk may actually be transferring data at a time. Multiple commands with optimized seeks may be included but is not a commitment at FRS.

A6. BI Interface -

The BIIC and BCI3 chips provide an interface to the BI bus. This allows the MicroVAX control processor on the AIO to access memory not local to the AIO. The BCI3 also provides a DMA engine to transfer data between AIO buffer RAM and memory located in a BI node without intervention from the MicroVAX control processor. The DMA engine in the BCI3 is capable of doing VAX memory mapping when provided with the appropriate page table entries in local AIO buffer RAM. The BCI3 chip contains 16 32-bit registers that may be accessed by other BI nodes that form the CSRs that control the AIO/AIE modules.

B. Aurora I/O Extension Module (AIE) -

The AIE module is a slave module to the AIO that provides a MAYA 100Mb magtape interface, 8 RS232 serial lines and an Ethernet port. There is no inteligence contained on the AIE nor is there a BI interface. It must be used in conjunction with the AIO board. The AIO moudle will function without the AIE board.

B1. MAYA Interface -

The MAYA interface will allow the AIO/AIE modules to control 1 100Mb streaming magtape drive. Current plans are to borrow the Qbus interface logic being designed by the MAYA tape engineering group in Shrewsbury and adapt it to the II32. This will allow the existing TMSCP code to be used. The MicroVAX control processor on the AIO board will fetch TMSCP commands and data from the host and pass them off to the MAYA interface. The MAYA interface uses an 80186 to parse TMSCP commands and control the drive logic.

B2. Ethernet Interface -

The AMD/Mostek NI chip set provides the AIO/AIE with an Ethernet interface. CSRs in the BCI3 are used by the host to communicate with the MicroVAX control processor. All incoming messages from the Ethernet are examined by the MicroVAX control processor and appropriate action is taken on DUP and multicast messages. All other messages are passed to the host.

B3. RS232 Interface -

The OCTART chip being designed in Hudson is used to provide 8 asynchronous lines. All lines have limited (DZ11 style) modem control. CSRs in the BCI3 are used for communications with the host. Current plans are to produce a dumb interrupt per character interface. DMA transfers from the host to the terminal lines is a possibility if the Aurora group has enough microcode resources.

2.2.2.3 Backplane Interconnect (BI Bus)

The BI is a Backplane Interconnect bus used to join a processor to integral I/O controllers, I/O bus adapters, memories, and other processors. Its characteristics are low cost, short length, high bandwidth, a moderate number of drops, a large addressing range, and data integrity. The BI is the interconnect successor to the SBI, CMI, and UNIBUS for VAX systems. It is the first totally new system interconnect since the PDP-8 "black block" implementation in 1965.

BI features include:

- High degree of data integrity
- Extensive error logging in all nodes
- Supports symmetrical and asymmetrical multiprocessing
- Distributed arbitration - no central arbitrator node required
- Slot interchangeability
- Standardized interface for all designs
- 1 Gigabyte address capability
- Up to 16 full master/slave/interrupt type devices
- Parity on bus datapath
- Worst-case design analyzed
- Power-up selftest in all nodes

The BI is public/licensed bus. The availability of interface chips, backplane/connectors, interface specifications and application notes provide a user with the necessary tools to interface to this new bus. Thus, Scorpio becomes the First VAX to allow a user to design an interface to a bus with greater bandwidth than the Unibus. These interface tools being available to external customers in FY85 should provide adequate incentive for Digital design organizations to expeditiously bring native BI peripherals to market.

BI Structural Overview -

The BI is a double clock synchronously operated interconnect with bus events occurring at fixed intervals. Data is clocked onto the bus at the leading edge of a transmit clock and received and latched with a receive clock at the end of a bus cycle. The bus cycle time is set at a rate which only allows transmission of information from one node to another. Information processing occurs during the cycle following the one in which it was transmitted.

Transactions on the bus are interlocked in the sense that only one command can be in progress at any given time. Both single and multi-responder commands are supported. Every single-responder command is confirmed with a positive acknowledgement for command accepted or command retry, a negative acknowledgement for no responder selected or error detected, or a stall acknowledgement to delay either of the two positive acknowledgements. Multiple-repsonder commands are confirmed as command accepted (by at least one responder) or no responder selected.

Bus arbitration, address and data tramsmissions are time multiplexed over 32 data lines. Interrupt sequences are accomplished via command transactions and may be directed to a single processor or a set of processors. Arbitration logic is distributed among all devices, and a round robin priority scheme will normally be used.

Data transmission is at fixed lengths of 4, 8, or 16 bytes on naturally aligned addressing boundaries. Data transferred within these lengths however, may be from one to sixteen bytes in any nominal clock period of 200 nanoseconds are 3.3 million bytes per second for 2 byte transfer lengths to 13.3 million bytes per second for 16 byte lengths.

BI Physical Description -

The current design strategy for the BI is based on complete BIs formed from one or more 6-slot BI backplanes, interconnected by cables.

The BI is limited to 60 inches (or less, TBD) overall, including the standard cables for interconnecting backplane segments of 4 and 12 inches.

BI module boards are nominally 8.00 inches deep by 9.18 inches high by .093 inches thich. BI modules connect to the BI backplane on 0.8 inch spacing.

The modules are connected to the BI backplane by a ZIF (Zero Insertion Force) connector surface mounted to a backplane.

Each BI node has a system unique one-of-16 BI node identification number. Each BI node receives an encoded 4-bit binary number obtained via a pinned encapsulated plug on the BI backplane. Each BI ID plug will have a decimal number in contrasting color printed or engraved on the surface of the plug. The decimal number corresponds to the binary equivalent number formed by the internal jumpers.

Each module slot position has 120 pins for BI signals. Modules which do not use all the BI signals must reserve these 120 pins.

Each module slot position has up to 180 input/output pins which correspond to up to 3 groups of 60 contacts on the module connector not used for BI.

Most of the BI signals are bussed, may be driven from any BI slot on the bus, and must be terminated. The clock signals are driven from one end of the bus, and must be terminated at the far end of the bus. A BI terminator set is supplied with every Aurora system; the clock terminator must be moved if a BI expander is installed, but the data terminator need not be moved.

BCI to II32 Chip (BCI3) -

The BCI3 is a custom ZMOS chip being developed for the Aurora system. It is a complete interface from the BCI bus (user bus of the BIIC), to the II32 bus generated by the MicroVAX chip.

II to BI Windowing Logic -

The BCI3 contains logic to window II32 transactions onto the BI. For program space external logic must assert an input signal to the BCI3 to force the windowing transaction. For I/O space the BCI3 windows all addresses except II32 boot ROM space and a region called node private space that contains private CSRs for each BI node. This windowing logic allows the ACP module to transparently (to the software), access memory on BI memory array cards, other ACP boards and CSRs in BI adapters. The AIO module uses the windowing logic to access rings and queues in the host processor(s) memory space.

II <--> BI Data Mover -

The BCI3 contains a DMA engine that executes medium speed data transfers between the II and the BI. Once set up this logic does not require any assistance from the local MicroVAX. PTEs must be established in local memory to allow mapping of the input and output data streams. The data mover can only move to and from octaword aligned locations. For optimal performance software must use octaword aligned buffers. The AIO module uses the data mover to read/write I/O buffers in host processor memory. The ACP board will not use the data mover under operating systems control. The data mover logic on the ACP module will be available to be used by OEM customers.

BCI3 Slave Port -

The BCI3 slave port receives read/write requests from the BI and will execute any program space request that falls within an address ranges defined by a register pair in the BCI3. All nodespace I/O requests are also handled. Interrupts and vectors received on the BI are translated into II interrupts and vectors.

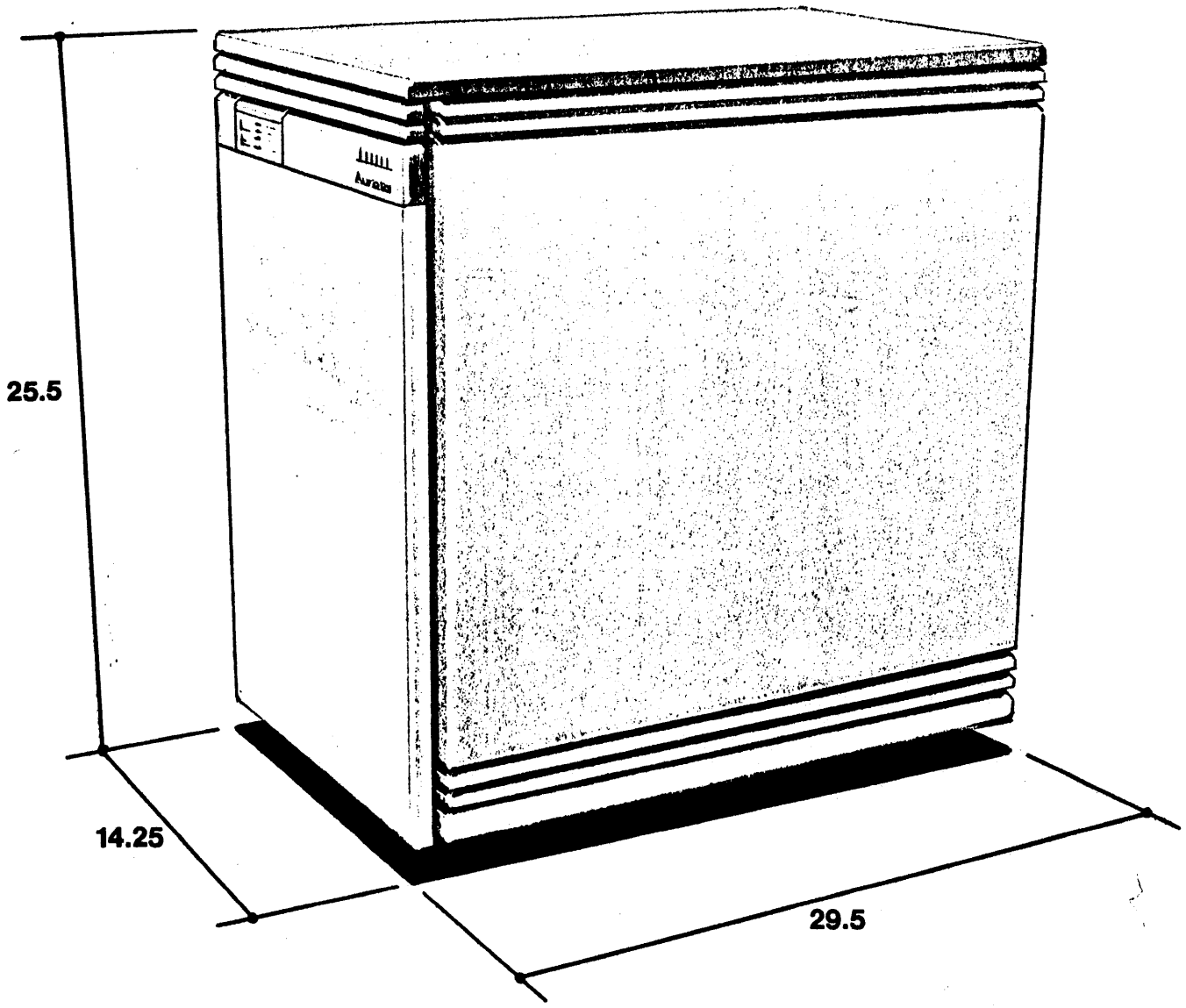
2.2.2.5 Power and Packaging

The Aurora system design center is a new desk height pedestal package that contains the BI backplane and four 5 1/4" mass storage slots. Compatibility with open-office environments is addressed by specific attention to cosmetics, form factor and acoustic management. The current pedestal design is only 25.5 inches high and 29.5 inches deep allowing it to fit under a table or work surface without protrusion. Acoustic management is achieved by a single custom designed, low acoustics air mover for the entire enclosure. The power supply design concept is that of a two modular supply; each power supply can power one 6-slot BI backplane to power internal systems components. The pedestal power supply requires a 15 amp maximum line cord and wall receptacle at 120 VAC for the first backplane/power supply. Only with the addition of the second backplane power supply subassembly is a 20 amp line cord required. Pedestal FCC compliance is achieved through RF gasketing and bulkhead I/O connectors.

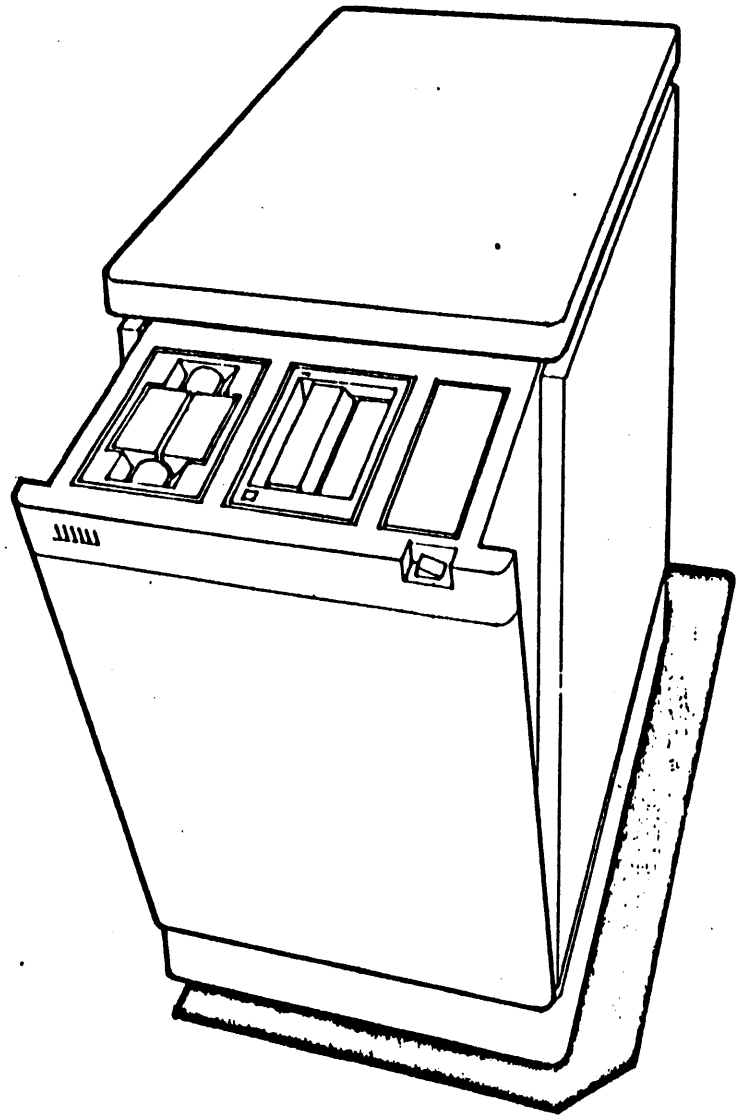
A second Aurora package is a 10.5 inch high OEM box with slides. This chassis also contains a BI backplane and associated power distribution.

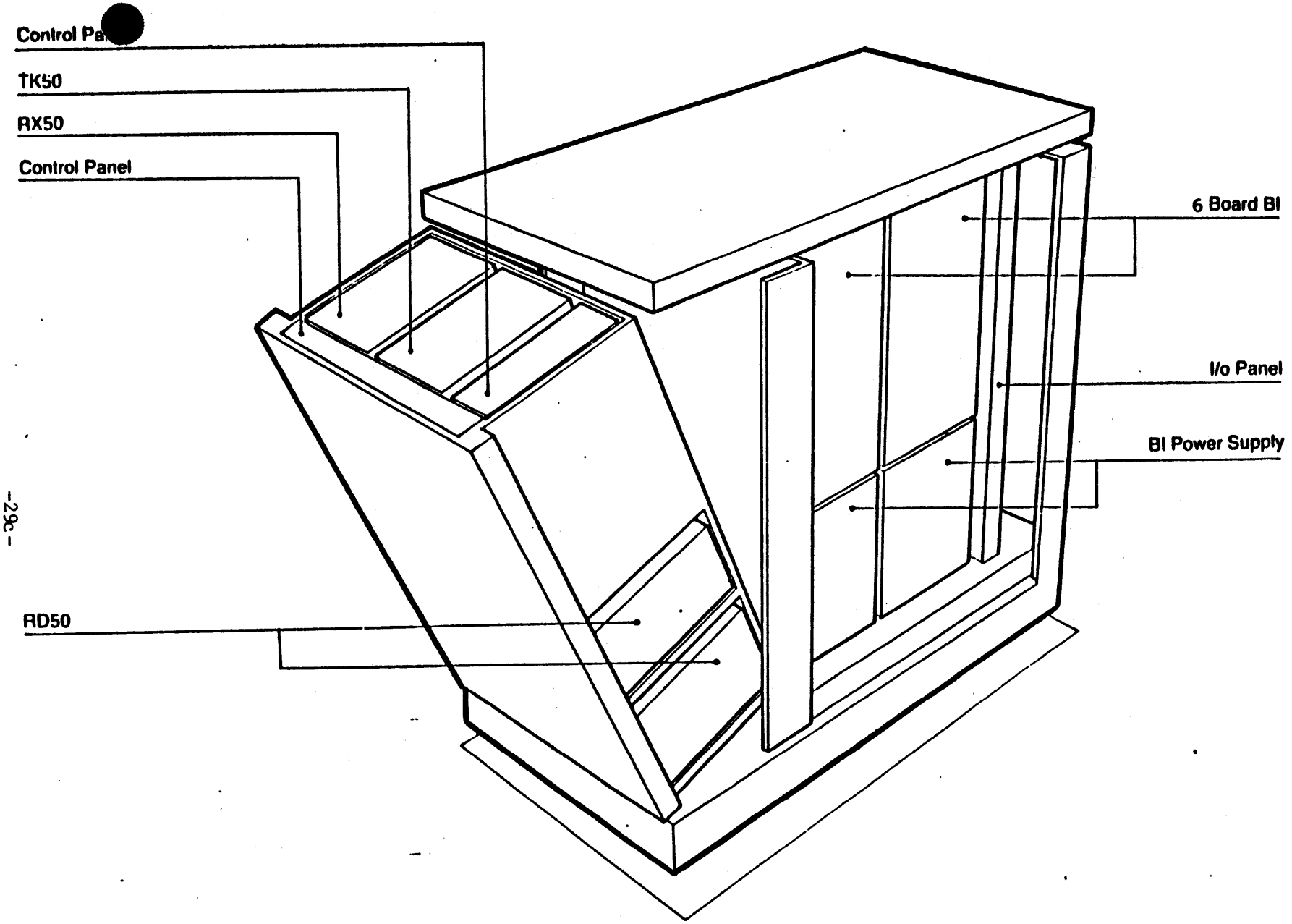
Packaging for TVG-Micros board products consists of a six slot BI backplane and an inter-backplane connector/cable for BI extension. Currently, no power supply products are planned for board set products.

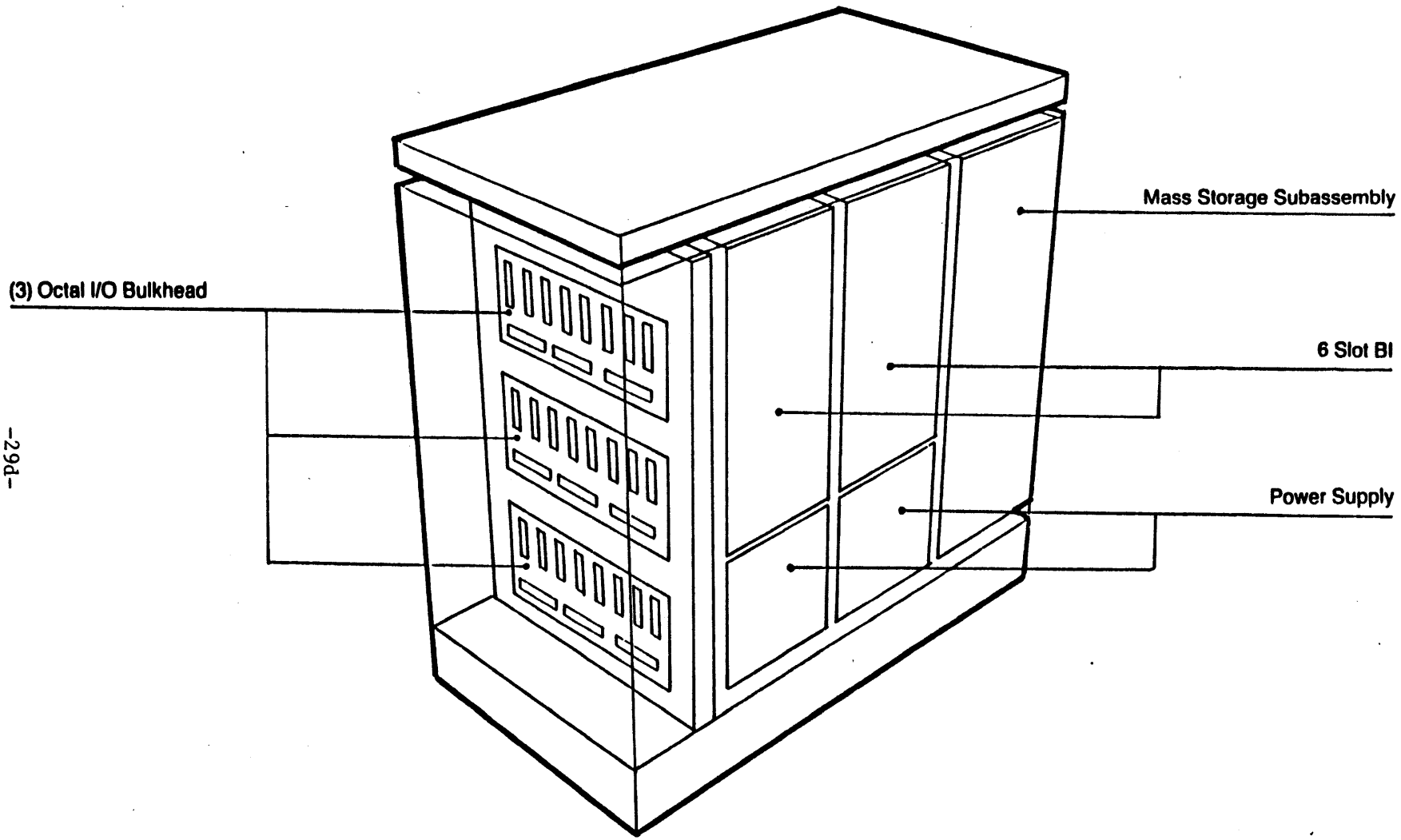
Some Aurora package renderings are on the following pages.



Aurora



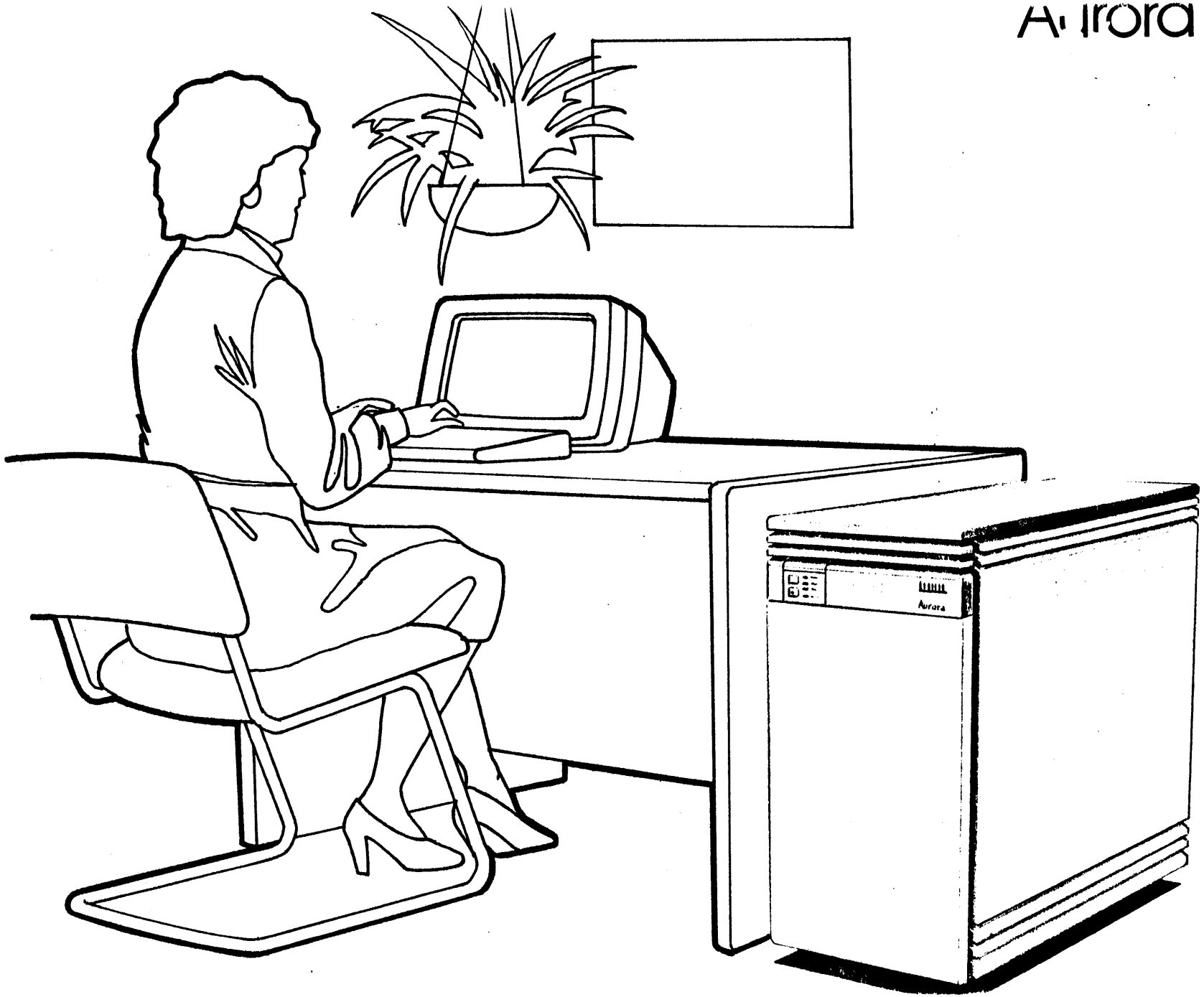

Control Pa
TK50
RX50
Control Panel
6 Board BI
I/o Panel
BI Power Supply
RD50



Aurora (Rear View)

Koepke 9/20

Aurora



2.2.3 Primary Product Deliverables

AURORA TEAM MACHINE

General Timesharing for 8-24 Users
POLARIS Pedestal Package
High Performance BI Bus
Up to 150+ mb of Disk Storage
100Mb Streaming Tape Backup
Up to 11Mb of Memory
- MicroVAX CPU
- 1Mb Memory
- 50+Mb Winchester Disk
- 800Kb Floppy Disk
- 100Mb Streaming Tape
- Ethernet Port
- 9 Terminal Lines
- 3 Expansion BI Slots
- Console Terminal (VT200/LA100 ?)

Options Include
- 2Mb Memory Board
- 50+Mb Winchester Disk
  - System Total of 3 Allowed if Floppy Removed
- BICOMBO Board (8 Asynch, 1 synch, 1 LP)
- Expansion 6 Slot BI Card Cage and Power Supply

AURORA Run TIme Only Machine

High Performance Run Time Environment
POLARIS Pedestal Package
High Performance BI Bus
- MicroVAX CPU
- 1Mb Memory
- 800Kb Floppy Disk
- 1 Terminal Line
- Console Terminal (VT200/LA100 ?)

Options Include
- Tape Controller/Ethernet/8 Terminal Line Board
- 100Mb Streaming Tape
- all Other Options Listed Above

AURORA System Configurations

AURORA OEM Box

POLARIS 10.5 inch OEM Box Package
6 Slot BI Backplane
585 Watt Power Supply
High Performance BI Bus
AURORA ACP Module (uVAX, 1Mb memory, 1 terminal line)
AURORA AIO Module (controller for 1 floppy, 3 winchesters)
800Kb Floppy Disk

Options Include

AURORA AIE Module
(Controller for Ethernet, Tape, 8 asynch lines)
2Mb Memory Board
BICOMBO Board (8Asynch, 1 synch, 1 LP)
Expansion 6 Slot BI Backplane
50+Mb Winchester Disk
100Mb Streaming Tape

AURORA Board Products

ACP Aurora CPU Module

MicroVAX Processor
1 Mb Memory
750 Speed
BI Interface

AIO Aurora I/O Module

BI Interface
Controls 1 Floppy
Controls 3 Winchesters
MicroVAX Chip used for Control
Implements MSCP

AIE Aurora I/O Extender Module

Slave Module to the AIO
Controls Ethernet Port
Controls Streaming Tape

AME Aurora Memory Extender Module

2Mb Memory
400 Access Time
Connects to Aurora Private Memory Bus

Aurora Software Options*

- MicroVMS
  General Purpose Computing Environments

- VAXElan
  Dedicated/Real-Time Environments

- MicroULTRIX
  Academic/Research Environments

- Layered Applications Software

* MLP and support dates TBD (To Be Determined)

2.2.4 Marketable Features--Relating to Customer Utility

Hardware and Packaging: The open-office pedestal packaging with its acoustic management (an overdue departure from previous Digital designs) provides considerable customer utility. Additional features of importance include greater than VAX-11/750 performance on a single module, the integral NI, multi-processor support, greatly improved system integrity provided by the BI, and the ability of a user to interface to this 13.3 MB/sec bus. Aurora board sets, utilizing only the BI bus (no Unibus), create a new benchmark for micro system integrity.

Software: MicroVMS and layered product support of Aurora, of course, extend the availability and applicability of VAX systems and further extends VAX/VMS functionality into new, less sophisticated markets. VAXElan, with its real time tuning and symmetric multiple processor support, provides new Digital solutions to 32-bit application problems. MicroULTRIX is growing in popularity as an industry-standard, transportable operating system and is expected to continue its high growth, especially in Aurora-class systems.

Services: Planned is a tailoring of service offerings to be more closely aligned wiht customer needs and industry trends. Service features include:

- Module mailer
- Parts dispatch
- Telephone support centers
- Tailored contracts
- Distributed remote diganosis as a system support tool

RAMP: Reliability, accessability and maintainability features include:

- Self test diagnostics in hardware (to the 90% confidence level) for each BI option at power-up.
- High reliability (MTBF).
- Low repair time (MTTR).
- Visual fault indication on each BI option.
- BI peripheral I/O cable connector on backplane rather than module.
- Customer Runnable Diagnostics (CRD).
- The inherent BI bus integrity providing new levels of system integrity.
- New BI module form factor provides for more efficient cooling.

- Thermally efficient system packaging.

- Accessability designed into the pedestal package and OEM box.

Price: Aggressive low-end pricing is planned to ensure an increased marketshare in this 32-bit price band. Pedestal packaging, customer-installable software and ease of installability contribute heavily toward the ability to price Aurora systems very competively.

Customer Cost of Ownership Minimization: Features to ensure low cost of ownership include:

- Low purchase price.

- High reliability.

- Low BMC; tailorable service offerings.

- Reduced AC power consumption.

- Less stringent environmental requirements.

International: Primary international features are:

- Euro compatible module form factor.

- Universal power supplies.

- CSA certification; VDE compliance.

- Local language customer runnable diagnostics.

- Country kits with local language system documentation and error ROMs.

2.2.5 Features to Reduce Life Cycle Cost to Digital

Maximization of corporate return on investment is achieved by specific attention to the following Aurora program components.

Transfer Cost: Transfer cost is minimized by:

- Aurora's CPU being a single, Euro compatible module with performance greater than a VAX-11/750 (four extended Hex CPU modules).

- Pedestal package design of single air mover, and modular power supply.

- Process testing, rather than product testing, resulting in increased yields and a reduction of test times and test equipment.

- Utilization of high reliability components and requiring burn-in at the component level.

- Manufacturing team's early participation in the program to develop high volume manufacturing processes and to ensure timely maturity of these processes.

Installation Cost and Quality: Cost is reduced while maintaining quality via:

- Ease of installation of systems.

- Installation "hot-line" telephone support.

Warranty and Service costs: These costs are minimized by:

- Ease of installation of systems and options.

- Self test diagnostics in hardware.

- Customer runnable diagnostics.

- Low MTTR.

- Remote diagnosis support.

- Low parts count for branch inventory.

Manufacturing Inventory: The associated costs are minimized by:

- A reduction of Stage 2 inventory to 3.9 weeks.

- A reduction of Stage 1 inventory by requiring weekly delivery of raw material.

2.3 FUTURE SYSTEM/FOLLOW-ON PRODUCT OFFERINGS

The Aurora will evolve over time as new technology allows. The following events in the near future will cause product definition changes.

1. CMOS MicroVAX chip (2x780 with cache on board)
2. 1Mbit dynamic RAMs
3. 10Mhz winchester data rates

A "mid-life kicker" product (about 24 months after FVS) may have the following attributes:

1. ACP board with CMOS MicroVAX and 4Mb onboard memory. Since the CMOS MicroVAX will have a cache onboard it will probably be feasible to use 8Mb BI array cards instead of continuing to use the current Aurora private memory bus and array cards. Given the apparent lack of a next generation of V-11 chips, this product may replace the KDZ-11 as well as the ACP. The cache/BI memory array structure will allow good multi-processing attributes. The onboard memory will still allow us a good SBC product. Presuming a VLSI memory controller chip from Hudson there will probably be enough room on the processor module to include either 8 terminal lines or an NI port.

2. The AIO/AIE board set will probably collapse into a single board capable of controlling RXZX's), a tape of some sort and either 8 terminal lines or an NI port (which ever is left off the CPU card).

The pedestal and it's power system as defined today should provide adequate functionality for the next generation of products. Since the CMOS MicroVAX will probably replace the V-11, many systems would be sold in cabinets as well.

Future Products Based on Aurora

We are currently planning two advanced development projects that will likely use the Aurora CPU module. One project is a security kernel system and the second is a high availability system.

Advanced development work on the software for kernel system has already started in Steve Lipner's group. We hope to start AD for the hardware in Q4 FY85. The present system architecture includes up to ten Aurora slave processors that would be running at selected security levels and one kernel (master) processor that would have absolute control of the BI traffic and the slaves. The initial market for the system will be secure government installations but we believe that the system will also have a substantial commercial market. Because of the available computing power in the system and because of the VMS and ULTRIX operating systems, it will be a leadership product at a time when commercial and industrial users will be demanding increased security.

The advanced development work for the high availabilty system(s) will be done in conjunction with Verell Boaen's group in TWO. We plan to start the AD work in Q4. We will be studying three application areas, process control, machine control, and communicatons. We will be developing architectures that will expand on clusters and target market areas that we do not currently address. The cost-performance of MicroVAX systems will allow us to sell high availability products that have a small incremental cost over standard systems of equivalent performance. The AD work will lead to product developments to start in FY85.

2.4 SYSTEM/PRODUCT POSITIONING

More detailed product positioning data will be provided in future revisions of this plan.

2.4.1 Digital Products

2.4.1.1 Digital Systems

Relative processor performance is shown graphically on the next page. Relative processor/system specifics are summarized below, for Aurora compared to a VAX-11/780:

- Processor performance is 1.0 vs .8-.9 for Aurora.
- The 11/780 CPU has 20 extended Hex modules vs a single Euro module for the Aurora CPU.
- The maximum 11/780 memory is 32MB vx 11MB for Aurora.
- The minimum 11/780 processor with memory and I/O is 28 extended Hex modules vs 2 Euro modules for Aurora.
- The 11/780 floating point accelerator is five extended Hex modules compared to a chip for Aurora.
- WCS is an option on the 11/780 but not available on Aurora.
- The 11/780 is packaged in H9600 corporate cabinets only, the CPU alone requiring a double-width high-boy. Aurora is available in a pedestal, 10 1/2" box and eventually in H9640 cabinets.

2.4.1.2 Digital Board Sets

Board set comparison will be provided in future revisions of this plan.

2.4.2 Competitive Products

General Competitive Environment

32-bit computers appear to be supplanting 8 and 16 bit architectures in many technical, commercial and business applications. 32 bit markets will emerge as one of the most hotly contested areas in the mid to late 1980's. There will be competition from all of our current competitors as well as new competition from Japan Inc. and American BELL. In order to minimize any erosion of DEC marketshare, time to market is the primary goal of the Aurora program.

It is likely that successful competitors in the mid to late 1980's will also possess meaningful semiconductor experience and relationships. At the Aurora performance level and beyond, considerable co-development efforts are required between semiconductor design and CPU design. Competitors failing to develop such relationships must rely on generic devices which will likely result in sub-optimal CPU desgins and performance.

Chip info: good for cost data. Go estimate competitive system's cost.

2.4.2.3 32-Bit Supermicro Product Analysis

Shipments of superminicomputers (systems with 32-bit data paths) are expected to grow at a compounded annual rate of 31.9% from $1.2 billion in 1981 to $4.8 billion in 1986, according to a recent study by Venture Development Corp.

These growth rate figures for the superminicomputers market are quite high, even for the fast growing electronics industry. There are several reasons for this. First, many new vendors are expected to enter the supermini industry during the next five years. Second, existing vendors of 32-bit systems are sure to expand their product lines both up and down. A good example of this would be to look at our own efforts in this area, Seahorse, Mayflower, Aurora, PC32, PRO32, WS32.... Third, prices will be falling dramatically, largly because of the recent advances in 32-bit VLSI CPU's.

The following is a competitive look at the 32-bit micro's being offered to the market place by the leading semiconductor manufacturers in the U.S. Most of these devices are expected to arrive in quantity during 1984 or 1985.

****
** ZILOG **
****

The Z80000 CPU is a 10MHZ, 32-bit, 1.7 MIPS pipeline processor with both virtual memory management and cache memory-all on the same chip. It has an advanced NMOS process that uses 2um rule, step repeat lithography, and dry plasma etching.

The Z80000 uses a 5-MHz internal processor cycle. A 5-stage pipeline combined with the cache can be interrogated by instructions and operand fetch on the same cycle. This allows a peak performance of 5 MIPS. With cache misses and pipeline gaps, the performance runs from 1.7 to 5 MIPS.

Through a varity of selectable options such as segmented or linear addressing, size of address space, organization of translation tables, designers gain the ability to configure the Z80000 to their specialized applications.

The Z80000 has a time-multiplexed 32-bit data and address bus to handle a linear address space of 4G bytes. It also offers two other modes of addressing, Compact, for addressing less then 64k bytes and Segmented Addressing, which allows the user to select either, a segmented address with a 15-bit segment number and a 16-bit offset or one with 7-bit segment number and a 24-bit offset.

In addition, the Z80000 supports nine general addressing modes with most instructions. These modes are Register, Direct address, Indirect address, Index base, Immediate, Base index plus displacement, Program counter relative, and Program counter relative plus index. The last three are used in segmented operation only.

The Z80000 evolved from the Z8000 product line and will be compatible with the Z80 and Z800. It will support a memory-management unit, a DMA controller, serial and parallel I/O controllers extended arithmetic units, and will be Z-buss compatible.

Zilog also offers a Arithmetic Processing Unit called the Z8070. This co-processor complies with the complete P754 IEEE standard for floating-point arithmetic.

The Z8000 will be housed in a 64 pin package, and has clock frequenies of 10/18/25 MHz along with a direct address range of 32M bytes.

****
** NCR-32 **
****

This 4 chip set, designated the NCR-32, offers full 32 bit architecture both internally and externally. The 4 chips that comprise the set plus the control store are:

NCR 32-000	32 Bit CPU
NCR 32-010	Address Translation Chip
NCR 32-020	Floating Point Co-Processor
NCR 32-500	System Interface Chip
NCR 2264	Control Store RAM

The chip set allows machine language emulation of virtually any computer system up to a medium sized mainframe. The main selling point is compatibility with the user's operating system.

The n-channel MOS CPU chip includes 4 internal 32-bit and (2) 16-bit data paths plus a 32 bit arithmetic logic unit. Micro instructions are implemented by means of an external 128K byte store plus on chip control ROM containing 256 micro instructions by 95 bits wide. The 16-bit external micro instructions are input vertically to the CPU where they select and sequence any of the 256 on-chip micro instructions. Functions are typically implemented in one 150 ns micro cycle.

The 4 chips are linked using a dual-channel, bi-directional 24 MB/sec/channel bus that relies on a carrier sense, multiple access, collision detection scheme.

System clock speed is 13.3 MHz. Fully configured, the NCR 32 provides full virtual memory support for addressing up to 3G bytes. High performance, floating point and decimal arithmetic are also fully supported. The CPU also contains (16) 32-bit general purpose registers. There is currently no cache support.

NCR has recently announced a 4K by 16-bit MOS ROM, designated the 2264, with an access time of 75 ns to be used as the external micro instruction store. It is a mask programmable device which allows the two chip select lines to be decoded without off-chip decoding circuitry. This feature supposedly reduces the access time by about 25 ns. As many as 16 of the 64K devices will typically be used which would fulfill the 128K byte control store capability.

The process used to fabricate the chips is similar to HMOS II, single metal, single polycilicide. A future selective shrink is expected to yield a 90ns cycle time. The 4 CPU chips are about 80K sq. mils. each.

Samples of the 4 chips, priced around $500/chip, will be available during now with production volumes, priced around $100/chip, coming in late '83, early '84.

Development support software, including an assembler, link editors, simulator and utility package for NCR mainframes are also availiable now. Similar tools for use on IBM 370, VAX, and "other large engineering computers" will be available by the second half of '83 according to NCR.

This is NCR's initial offering in the 32-bit market and it is questionable as to the impact they will have. The performance of the chip set is not very good (.3-.5 X 11/780) and thus far, the software tested is limited to the NCR architecture.

****
** Hewlett-Packard **
****

The HP Focus is a full 32-bit microprocessor with demand paged virtual memory, an address rang of 500M bytes and as much as 2.5M bytes of on-line RAM.

The single chip CPU contains 450K transistors and operates at an 18Mhz clock frequency. It has a ROM control store that contains 9K 38-bit words that implement an "extensive" 32-bit instruction set (230 instructions). The register stack contains (28) 32-bit registers. The CPU instruction set is stack oriented and contains several broad classes of instructions:

- Load and store - transfers data (bits, bytes, half words, words, and double words) between memory and top of the stack.
- Stack and register manipulation instructions for interchanging quantities on the stack, shifting and rotating the TOS, and pushing (setting) register values onto (from) the stack.
- Arithmetic and logical instructions which perform 32-bit integer math, 32B and 64B IEEE STD floating point math, conversions among the different formats and 32B logical operations.
- Program control and branching instructions including conditional and unconditional branches, procedure call and exit, support for dispatching tasks and debugging aids for high level languages.
- Move and string instructions which manipulate both unstructured byte arrays and a structured string data type.
- I/O and interrupt instructions for handling I/O.
- Special instructions to aid the development of operating systems.

A standard load instruction takes 550 ns and a 64-bit floating point multiply takes 10.4 us.

The total execution cycle of a micro-instruction takes three 55 ns clock cycles or 165 ns. Pipelining allows the overlap of all 3 of these operations; thus the net execution rate of sequential micro instructions is one per clock cycle.

The performance of the CPU is enhanced by making extensive use of pipelining; especially in machine instruction execution, micro-instruction execution, ALU operations and memory operations.

The pipelining of memory operations allows a 32B memory read to be initiated every two states (110 ns) even though the access time is longer.

During the power-up sequence, the CPU executes self-test microcode that tests the operations internal to the chip. Once this is completed, a set of processor-to-memory operations are performed to fully test these functions.

The H-P Focus is fabricated with an advanced 8 mask silicon-gate NMOS III process which has three and one-half layers of interconnect and 1-um spacing between the signal carrying lines. The second layer metal is 5 um lines and 3 um spaces. The interconnection of the devices is achieved with diffusion, polysilicon and two layers of refractory metal. The reticles used are 10X E-Beam generated.

The H-P Focus is intended for use only in HP products and will not be sold separately. Their first product using the Focus is called the HP9000. The 9000 is a desk top computer that is said to have the power of a Vax supermini. They are taking orders on a $20K box, $30K workstation, and a $50K multi-user system. Shipments began in February of 83.

Additional products based on the chip are in development and are expected to be announced soon.

H-P is considered by many to be DEC's primary competitor in the foreseeable future. H-P, itself, has stated that it considers DEC to be its chief competitor and this introduction puts H-P squarely in the 32-bit market space occupied by VAX. Performance of the HP9000, according to H-P, ranges from 1 - 2.7 MIPS, depending on the number of CPU modules used (1-3).

DEC's major advantages vs H-P in this market is our 5 year experience lead with 32-bit systems, our software compatability across the VAX family and our extensive software offerings both DEC and 3rd party.

****
** National Semiconductor **
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NS 16032 CPU
NS 16082 MMU
NS 16081 FPU
NS 16201 Clock
NS 16202 Interrupt
NS 16203 DMA

The National 16032 CPU is part of a 4 chip set that features a variable length, demand paging virtual memory system. Internally, the processor uses 32-bit data paths and 32-bit address arithmetic to directly address memory without the overhead of setting up segmentation registers. It contains a 16-bit data bus and a 24-bit address bus that gives it access to 16M bytes of virtual address space.

Bus cycles are overlapped with internal processing and are controlled by a bus interface. Instruction execution uses a 3-stage pipeline. One to two instruction bytes are decoded every 100ns.

The microcode store size is 1300 X 18 bits including 127 words of chip self test routines.

The 16082 MMU employs a demand-paged scheme to carry out its virtual memory operation. Two hierarchical levels of protection are offered. An optional FPU (16081) is functional at 6 Mhz. With parts running at 10 Mhz, the 16032 with FPA will probably have a performance of 50% of a VAX 11/780. The FPU carries out add, subtract, multiply and divide operations in hardware with remaining operations being carried out in software.

The process used to fab the 16032 is 3.5um, NMOS. There are 60K transistors on the 84K sq. mil. chip with power consumption being 1.2W.

Samples of 10 Mhz parts priced at $162 are scheduled to be available in the middle of '83.

Along with the 16- and 32-bit CPU's, National is creating a reduced bus version of the same chips. Designated as the NS16008, this 8-bit CPU will offer system designers a low cost system solution.

National is also offering a single board computer with a 16032 and sockets for peripheral chips and has licensed Bell Lab's Unix operating system so developers will be able to use any system that runs Unix. National will soon be introducing its first system-level Unix box, named Mesa, using the 16032 with the 16082 MMU and a socket for the 16081 FPU. Mesa will support a full 32-bit virtual memory space and be an 8 user time-sharing sytem.

Advertised as being availiable this this year, National has come up with an enhanced 16032 called the NS32032. This device offers a data-bus width to 32-bits and an address bus of 24 bits, providing a proportionate improvement in execution speed. The NS32032"s has demand-page, virtual memory capability and a on-chip floating point unit. These features added with their memory-management slave processor, make a very attractive package.

Sometime in 1984, National will begin sampling its low-power version, the 16C032. This will be their first part in C-MOS. Power consumption is projected to be 0.7W versus the 16032's 1.2W.

Around 1985, National is planning a full-blown 20MHZ 32-bit CPU, the 32132. It will be based on National's 1.5 micrometer C-MOS process. National plans to bring on chip demand-page memory management, floating-point math based on the IEEE standard, and interrupt control, resulting in a device estimated to contain 500,000 transistors. It will have a 32-bit data and address bus with a virtual memory space of 4GB and memory management on chip. National is claiming performance improvement of 5 to 10 times over the 16032.

****
** Motorola **
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MC68020 CPU
MC68451 MMU
MC68881 FPU

The MC68020 is an enhanced 32-bit version of the highly successful MC68000 and is software compatible with the MC68000, MC68010, and MC68008.

The 68020 has all the features and functions of the 68000 and 68010, plus, it is upward object-code compatible and has an extended address space of 4GB virtual. It provides some extensions to the 14 addressing modes available in the 68000 and 68010 such as 32-bit displacement addressing for all branch instructions.

Besides it's full 32-bit architecture, the 68020 differs from the earlier 68XXX processors in it's instruction-set enhancements, co-processor operations, and improved operating-system support. System performance is also enhanced by means of an on-chip instruction cache which is 128 words by 59 Bits. Fetches from cache take 2 cycles versus 4 cycles needed for fetches from memory. The cache holds only instruction stream data; no memory data is held.

The floating point co-processor, the 68881 (Motorola's first co-processor for the 68000 family), has an interface which allows multiple co-processors to be utilized in a system. The FPU is fully IEEE compatible, has single, double and extended precision, and does an 80B X 80B multiply in 12.6 us. To conform to IEEE, it does all the operations in extended (80-bit) precision which causes the single (32B) and double (64B) times to be longer, not shorter. This is in contrast to the National FPU which, by utilizing software to carry out the FP operations other than the basic four, is able to use 32-bit registers.

The process Motorola uses to fab the 68020 is H(c) MOSIII. It uses a 2.5um rule, is 78.4K sq. mils and contains 150K transistors. Through a mixture of N-channel and complementary-MOS hopes to keep power dissipation down to 1.5 to 2 watts-about the same as the 68000. Acceptance of the 68000 architecture among users has resulted in a wide variety of 68000 based software packages from 3rd party vendors. This will undoubtedly help the 68020 being accepted in the 32-bit marketplace.

The 68020 will be packaged in a R-Pack, which is a square ceramic pin-grid array that can cope with up to 100 connections from chip to printed-circuit board.

One weakness Motorola will need to overcome is its poor virtual memory support (68451 MMU). They hope to do this with the 68441 MMU.

Samples of the 68020 CPU and 68881 FPU are scheduled for spring of '84 with the 68441 MMU to follow sometime "later".

Pricing of the CPU will be around $100 at availability and dropping to 10-15% premium over the 68000 around 1985.

****
** Intel **
****

43201 GDP
43202 GDP
43203 IP

The Intel 432 is a three chip set comprised of a two chip General Data Processor (GDP) and an Interface Processor (IP). The GDP performs instruction decoding, address generation and data manipulations. It recognizes and provides a virtual address space of 1GB with a physical address space of 16MB. The IP provides a bridge from an I/O subsystem to the protected access environment of the central system. Each I/O subsystem uses an 8- or 16-bit micro processor as an attached processor, thus making I/O completely independent of the central system. With this architecture, Intel provides a link between its older 8086 and newer 432. It appears the only way the 432 can be used effectively is as a distributed interactive system with multiple processors attached. It's performance as a three chip, stand alone system has been criticized by users.

The GDP's basic data manipulation operators and addressing modes are implemented in less than 250 X 16B of microcode which leaves the remaining 3.75K of micro instructions for floating point and the object-oriented functions of the system. The structure is a 4K by 16B shared-ground line ROM with an access time of 75ns.

The 432 process is HMOSI with geometries of 3.5um. The number of transistors per chip ranges from 50K to 110K with the largest die being 116K sq. mils. Performance has been described by Intel as a range defined at the low end by the IBM 370/148 and at the high end by the 370/158. While Intel sees the 432 as being directly comparable in performance to the VAX 11/780, a Berkeley article bench marked a single 432 as being .12 X the VAX 11/780. The 432 and its unique architecture has not been well received in the marketplace and Intel is developing the iAPX386 as its replacement.

The 386 is a full 32-bit chip with demand-pageed virtual memory, an address range of 32M bytes and on-line memory support of as much as 4G bytes. The chip will resemble the 16-bit 286 in it's use of HMOS III technology and have a similar power dissipation of 2.5W.

Intel expects that the 68-pin 111 instuction 386, to double the performance of the 286. In addition to its on-chip cache, it will also have a pipelined CPU and be software compatible with the iAPX 286 family. It will include on chip paging and virtual memory via segmentation.

The 386 is scheduled to sample in the second half of 1984.

****
** uVAX32000 **
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The uVAX32000 is a high performance single chip microprocessor that delivers the architecture and functionality of DEC's super-mini, the VAX-11. The uVAX32000 is housed in a 32-bit package and fabricated in ZMOS (double metal NMOS). It implements a full 32-bit address and data architecture that can directly access 4 gigabytes of virtual memory and 1 gigabyte of physical memory.

The uVAX32000 is VAX-11 compatable through its implementation of a subset of VAX-11 instruction set and memory management. The uVAX32000 has 245 instructions with 21 modes and 9 data types. It also offers an efficient interrupt stucture to increase system thruput.

All VAX-11 native-mode instuctions and data types are not implemented directly by the uVAX32000. Some are emulated by microcode-assisted software routines. Any non-priviledged native mode code written for any VAX/VMS system will execute correctly on the uVAX32000 using MicroVMS.

****
Statistical Comparison **
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32 BIT MICROPROCESSOR COMPETITIVE ANALYSIS

	Zilog	Motorola	National		Intel	NCR	H-P	DEC	DEC
Part Number	Z80000	68020	16032	32032	386	NCR32	Focus	uVAX	V-11
Performance MIPS	1.5 2.5-3.7	1.5	.5	.7	1.2	.3-.5	1-2.7	.9-1.0	.9-1.0
Internal Data Path	32B	32B	32B	32B	32B	32B	32B	32B	32B
External Data Path	32B	32B	16B	32B	32B	32B	32B	32B	32B
Micro Cycle Time	?	?	100ns	?	?	150ns	165ns	200ns	200ns
Effective Memory Cycle Time	600ns 250ns	?	?	?	?	?	110ns	400ns	380ns
Clock Speed	10MHz 25MHz	8MHz- 16MHz	10MHz	?	16-20	13.3MHz	18MHz MHz	20MHz	20MHz
Physical Address Space	16MB	16MB	16MB	16MB	?	?	2.5MB	1GB	1GB
Virtual Address Space	4GB	4GB	16MB	4GB	4GB	3GB	500MB	4GB	4GB

	Zilog	Motorola	National		Intel	NCR	H-P	DEC	DEC
Part Number	Z80000	68020	16032	32032	386	NCR32	Focus	uVAX	V-11
# Instructions	-	65	86	86	111	?	230	245	
Control Store	?	? x 18B	1.3K x 18B	1.3K	?	128KB	9K x 38B	1.7K x 39B	16K x 40B
# of Chips**	1	3		4	4	?	5		4
2 8									
Hot Floating Point	Opt.	Opt.		Opt.	Opt.	Opt.	Opt.		-
Opt. Opt.									
# Trans	?	170K		60K	65K	270K	45K		85K-
110K 55K-150K per Chip					110K	450K			
Process	NMOS	HCMOSIII		NMOS	NMOS	CMOS	NMOS		NMOSIII
N(Z)MOS N(Z)MOS									
# Pins	68	100		48	60	68	68		84
68 128									
Proto-typing System	ZSCAN	Exormac	|<Starplex > VAX|			Intel-lec MDS			HP9000
Feature Size		2.5um		3.5um	3.5um	?	3.0um		2.5um
3.0um 3.0um									
Package	Leadless Carrier								
Samples Available	Q2 84	Q1/84		Q3/83	Q1/84	Q2/84	NOW		NOW
Q2/84 Q2/84									
Volume Ship	?	Q3/84		??/83	Q2/84	Q1/85	Q4/83		Q4/83
Q3/84 83/84									
Price (*+**)	?	$300		?	?	?	$500		Captive
$95 $300									
Second Source	_	Hitachi		Fairchild		AMD	Motorola		None
None None		Rockwell Mostek Thompson		Synertek Eurotec		Siemans Intellec MDS			

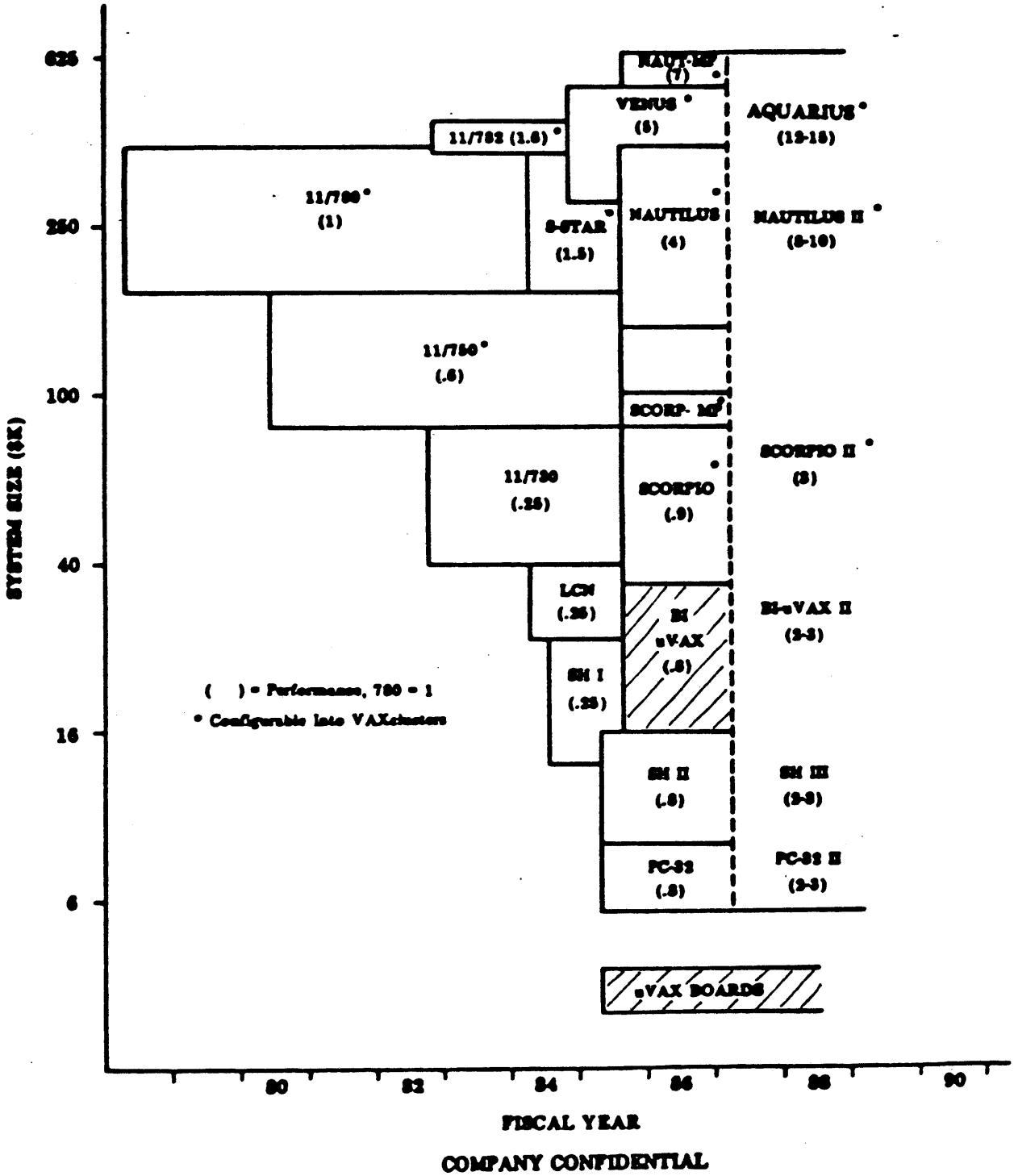
* Price is mature price except for DEC which is mature transfer cost.

** Full chip set (CPU, MMU, FPU, clock)

2.4.3 Price Positioning Charts

The following pages summarize relative price/performance position for Aurora systems and workstations. Other references are listed in Chapter 7.

VAX SYSTEM
PRICEBAND POSITIONING



COMPANY CONFIDENTIAL

J. Tuttle
10 Oct 83
JT1.5

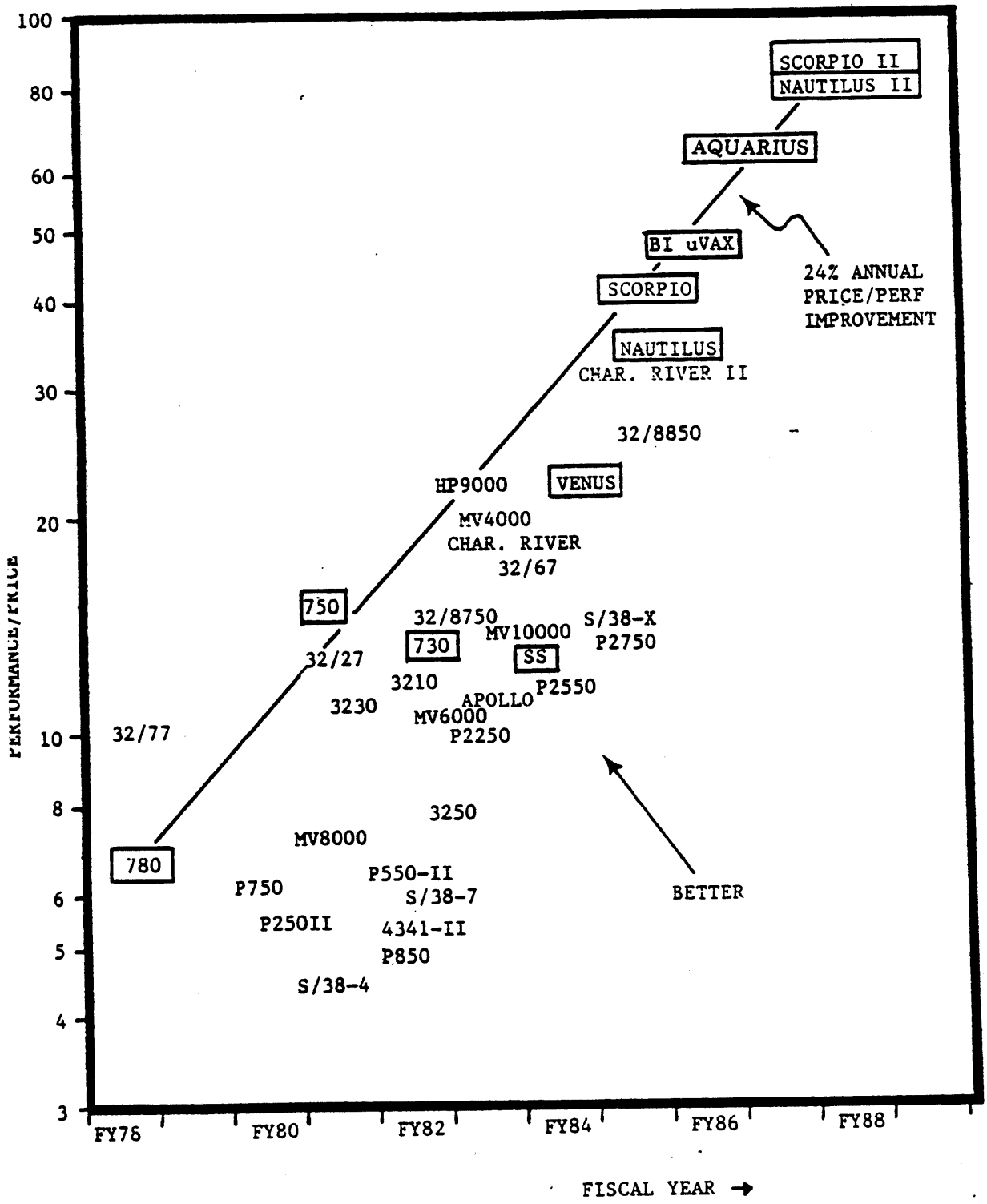
SYSTEM FEATURES

	AURORA	MOTOROLA SYSTEM INTEGRATOR	INTEL SYSTEM INTEGRATOR
CPU	uVAX	68020	386
Performance (vs. a 780)	.9	1.0	1.2
Address Space	1 GB	4 GB	4 GB
Virtual Memory	Yes	Yes	Yes
Bus	BI	VME	Multibus II

TYPICAL CONFIGURATION

	AURORA	MOTOROLA SYSTEM INTEGRATOR	INTEL SYSTEM INTEGRATOR
Users	8	8	8
Memory	3 MB	2 MB	2 MB
Disk	50 MB	30-50 MB	30-50 MB
Tape	100 MB	50-100 MB	50-100 MB
Software	uVMS ULTRIX ELAN	UNIX	UNIX CPM MS-DOS
Price	$20K	$15-20K	$15-20K

BOX LEVEL PERFORMANCE/PRICE



SINGLE USER WORKSTATIONS

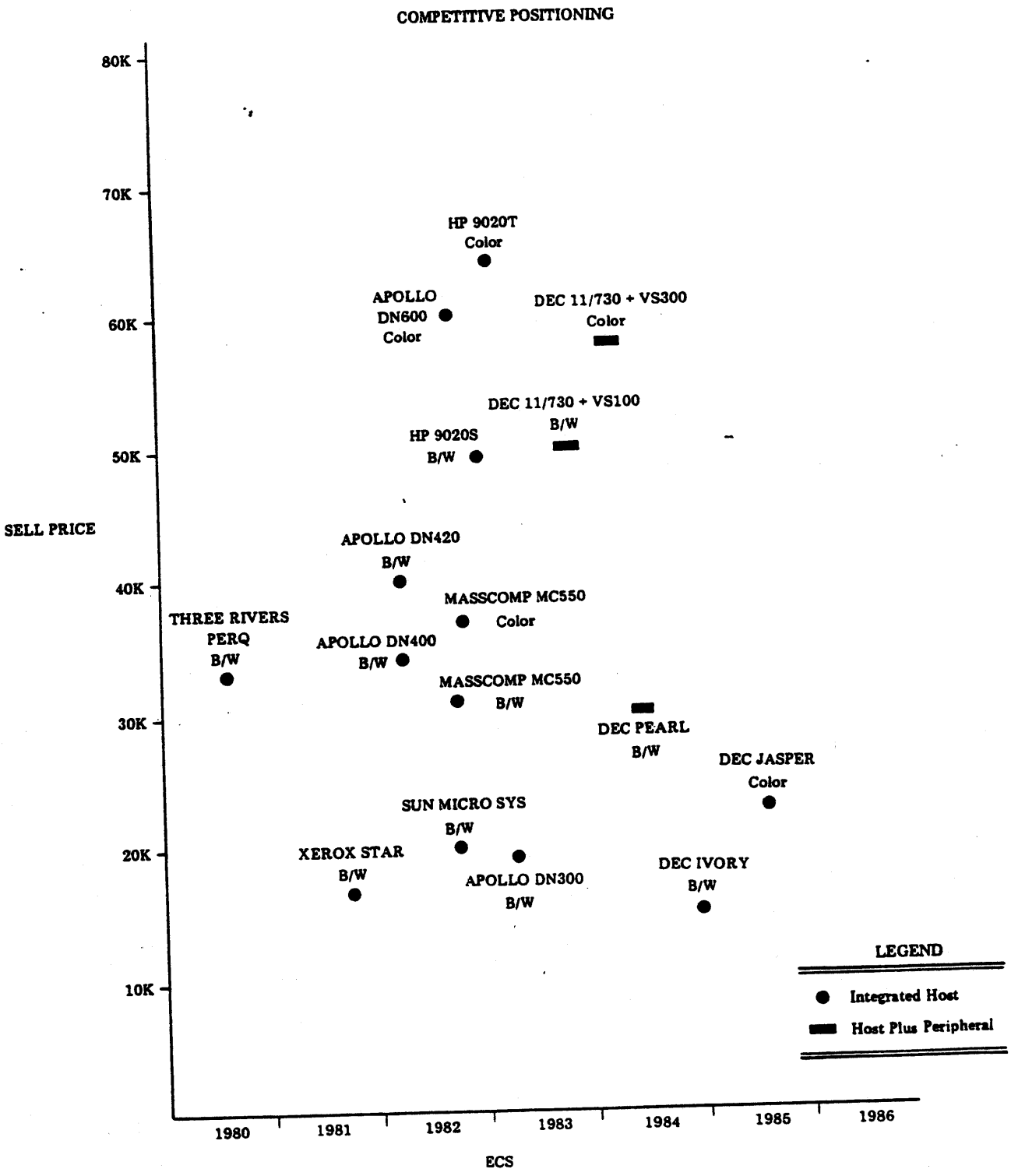
	VS125	HP9020	Apollo DN300	Sun
CPU	730	HP9000	68010	68010
Performance (vs 780)	.25	.45	.2 to .5	.2 to .5
Memory	2 MB	512 KB	1 MB	1 MB
Floppy	-	270 KB	1.2MB	-
Disk	26 MB Fixed 26 MB Removable	10 MB	68 MB	8 MB Fixed 8 MB Removable
Terminal	19" B/W	13" B/W	17" B/W	17" B/W
Communications	Ethernet	Ethernet	Domain	Ethernet
O/S	VMS	HP-UX	Aegis	UNIX
Price	$33,000	$39,000	$33,900	$19,900

Notes

All performance metrics are estimates. For Sun and Apollo, the lower number represents floating point performance, the higher integer performance.

TYPICAL MULTIUSER CONFIGURATIONS TODAY

	Micro/PDP11	MicroVAX I	DG Model/30	Altos ACS	C.R. Data Universe/47
Processor	F-11	Cust. Design	uECLIPSE	68000	68000
Performance (vs 780)	.15	.35	.15	.3	.2 to .5
Users	4	4	4	?	8
Memory	1 MB	1 MB	1 MB	512 KB	1 MB
Floppy	800 KB	800 KB	368 KB	-	1.25 MB
Disk	28 MB	28 MB	15MB	62 MB	32MB
Tape	-	-	15 MB (Cartridge)	Streamer	-
O/S	uRSX	uVMS uUltrix	AOS	Altos Xenix	Unos
Price	$14,850	$18,885	$16,850	$20,500	$27,350



VAXSTATION

COMPETITION CHART

	APOLLO DN400	APOLLO DN420	APOLLO DN600	THREE RIVERS COMPUTER PERQ	DEC VS100 (1 TERM. + 11/730)	DEC VS300 (1 TERM. + 11/730)
CPU	32-bit 10 MHZ	32-bit 10 MHZ	32-bit 10 MHZ	16-bit 4K WCS	32-bit 11/730	32-bit 11/730
MAIN MEMORY	0.5-3.5Mb	0.5-3.5Mb	0.5-3.5Mb	0.5-1.0Mb	1.0Mb	1.0Mb
DISPLAY TYPE	RASTER	RASTER	RASTER	RASTER	RASTER	RASTER
DISPLAY SIZE	15" Vert Portrait	19" Horz Landscape	19" Horz Landscape	15" Vert Portrait	19" Horz Landscape	19"
RESOLUTION	800 x 1024	1024 x 800	1024 x 1024	768 x 1024	1088 x 864	1088 x 864
COLOR CAPABILITY	B/W	B/W	16-262K CLUT	B/W	B/W	256/16M CLUT
LOCAL INTELLIGENCE	68000	68000	68000	Spec. H/W & ucode	68000	68000
LOCAL MEMORY (Kbytes)	128 Kbytes	128 Kbytes	1-2 Mbytes	part of main mem.	512Kb	1-2 Mbytes
I/O DEVICES	KBD w/ touch pad	KBD w/ touch pad	KBD w/ touch pad	KBD, table w/pen or puck	KBD, mouse tablet	KBD, mouse tablet
SOFTWARE	AEGIS, D3M,CORE STANDARD	AEGIS, D3M,CORE STANDARD	AEGIS, D3M,CORE STANDARD	PERQ OS, COMPILER EDITOR	VMS,SDA CORE STANDARD	VMS,SDA CORE STANDARD
NETWORK CAPABILITY	12 Mbit/ SEC	12 Mbit/ SEC	12 Mbit/ SEC	ETHERNET 10 Mbit/ SEC	DECNET	DECNET
PRICE	$34.5K	$37K-$45K	$59K-$75K	$33.3K	$60.5K Display Services S/W $3K	$68K-$73K Display Services S/W $3K

TECHNICAL MARKETPLACE

Functionality	MicroVAX I	SUN Syst.A	SUN Syst.B	Apollo DN300	HP 9020B	HP 9020S	DG Model 30
CPU Implement.	Cust.design MOS	M68000	M68000	M68000	HP9000	HP9000	8086
Address size	32-bit	23-bit	23-bit	23-bit	32-bit	32-bit	20-bit
Memory	1 MB	1 MB	1 MB	1.5 MB	512 KB	1 MB	1 MB
Disk (Formatted)							
- Floppy	800 KB	-	-	1.2 MB	270 KB	270 KB	Yes
- Winchester	25+ MB	8+8 MB	64 MB	34 MB	-	10 MB	15 MB
- Streaming tape	-	-	20 MB	-	-	-	-
Asynch line	1	2	2	2	?	?	4
Terminal	VT125 B/W	17" B/W	19 " Color	17 " B/W	13" B/W	13" Color	DASHER B/W
Comm.	Ethernet	Ethernet	Ethernet	-	-	-	-
Oper. system	MicroVMS MicroVAX ULTRIX	UNIX	UNIX	AEGIS	-	HP-UX	AOS
Claimed Performance (11/780) Not measured by Digital	.3	.6-.9	.6-.9	.3	.3	.3	.3
Price(MLP)	$ 20.8K	$ 19.9K	$ 36K	$ 31.9K	$ 28K	$ 50K	$ 17K

Notes:

Sun: Sys A: The 13" B/W landscape monitor offers 1024x800 pixel resolution.
Sys B: The 19" Color monitor offers 640x480x8 pixel resolution, with the Color Graphic frame buffer option included.

Apollo: The price for additional lanquages in the DN300 , such as FORTRAN, Pascal is $1,500 each.

HP: HP-UX is a single-user operating system
HP9020B includes no software.
HP9020S includes thermal printer.
Ethernet is an option to both systems and will be priced at $6K.

DG: The price includes a printer.

COMMERCIAL MARKETPLACE

Functionality	MicroVAX I	IBM9000	LINK-DATA	ALTOS ACS 68000-RMC3	IBM Sys.36
CPU Implement.	Cust.design MOS	68000	68000	68000	IBM Proprietary
Address size	32-bit	23-bit	23-bit	23-bit	24-bit
Memory	1 MB	1 MB	256 KB	512 KB	128 KB
Disk (Formatted)					Yes
- Floppy	800 KB	327 KB	5 MB	-	
- Winchester	254 MB	20 MB	30 MB	64 MB	30 MB
- Streamer tape				Yes	
Asynch line	1	4	4	?	2
Terminal	1	1	2	None	2
Communication	Ethernet	-	-	-	-
Operating system	MicroVMS MicroVAX ULTRIX	UNIX	LINK-DOS	?	System Support Program
Performance (11/780)	.3	.3	.3	.3	?
Price(MLP)	$ 20.8K	$ 18.2K	$ 19.3K	$ 20.5K	$ 34K

Notes:

IBM: The IBM9000 includes a 12" raster scan CRT with graphic resolution of 768x480 pixels. The price for System 36 includes a printer.

LINK-DATA: Link-Data system includes the layered software DYBALL (DIBOL) and 2 each VT100 compatible terminals. The Link-Data product is built around the IBM9000 base system, priced at $ 5,695.

COMPETITIVE ANALYSIS

Competition is changing and getting tougher. There is a brand new style of competition based on easy to use commodity VLSI chips. We are now seeing startup companies like SUN and APPOLO able to go from startup to product in a very short time. The traditional micro/mini/mainframe distinctions of the 70s are gone. The 68020 chip has about the same CPU power as a DECsystem-10. In this new competitive environment, particularily at the low end, DEC needs product and marketing uniqueness to win.

The table below highlights the key strengths and weaknesses of the competition in the low end computer market.

	STRENGTHS	WEAKNESSES
Vertically Integrated Companies (IBM, Intel etc.)	o Total product integration o Non-duplicable features o Time to market (technology) o Economies of scale o Architectural control	o Heavy capital investment o Technology obsolescence o Business focus issues
Application-Oriented System Integrators (Apollo, Wang etc.)	o Superior point product capability o Low capital investment o Time to market (applications) o Flexibility	o Dependence on industry standard products o Weak product differentiation o Exposure to price competition o Architectural management

Appendix 2 analyzes the specific competition for the MicroVAX product family.

High-Resolution Graphic Display Systems

Manufacturer	Apollo	Adage	Aydin Controls	CalComp
Model	Domain	4100, 4250, 4370, 4177	AYCON 16 Series	Visigraphic 4000
Display Size/ Resolution	19"/1024 x 1024	21"/N.A.	19", 25"/1024 x 1024	19"/1024 x 1024
Color Palette/ Displayable	16.7 million/256	Monochrome	16.7 million/65,536	4096/8 - 256
Display Technology/ Refresh Rate	Raster/60 Hz non-interlaced, 30 Hz interlaced	Vector/N.A.	Raster/60 Hz non-interlaced, 30 Hz interlaced	Raster/30 Hz interlaced
Internal Graphics Processor	Apollo 290	Proprietary	Intel 8086	Two Motorola M68000's
Software	Display manager, SIGGRAPH 3-C core	Third party	AYGRAPH-CORE, List & 3-D	FSP, GCT
Expandability	1 - 2Mb memory	Data tablet, keyboard, programmable function switches, control dials	Peripheral & mass storage controllers, host interfaces	Keyboard, data tablet, joystick, plotters
Date Introduced/Units Placed	1982/75+	N.A./1,382 combined	1978/400+	1982/N.A.
Price	$59,000	$42,920 - $100,000	$16,000	$24,500 - $50,000
	Apollo Computer, Inc. 17 Alpha Rd. Chelmsford, MA 01824 (617) 256-6600	**Adage, Inc.** One Fortune Dr. Billerica, MA 01821 (617) 667-7070	**Aydin Controls** 414 Commerce Dr. Fort Washington, PA 19034 (215) 542-7800	**CalComp** 2411 W. LaPalma Ave. Anaheim, CA 92801 (714) 821-2541

Manufacturer	Chromatics	Evans & Sutherland	Genisco	Grinnell
Model	7900 Series	Calligraphic PS-300	G-6110	2764; 2768
Display Size/ Resolution	19"/1024 x 1024	19"/4096 x 4096	19"/1024 x 1024	19"/1024 x 1024
Color Palette/ Displayable	16.7 million/256	1800/440	64/16	4096/16 or 32; 4096/256
Display Technology/ Refresh Rate	Raster/30 Hz interlaced	Raster/30 Hz interlaced	Raster/30 Hz interlaced	Raster/30 Hz interlaced
Internal Graphics Processor	Motorola 68000	Proprietary	Proprietary	None
Software	"C", Pascal, FORTRAN	FORTRAN based, ROMULUS	PROM resident, GenCor operating system	FORTRAN library of subroutines
Expandability	8Mb memory, hard disk, digitizer, light pen, joystick	6 standard I/O ports	Overlay memory planes, disk controller	Cursor, joystick, additional memory
Date Introduced/Units Placed	1980/N.A.	1980/N.A.	1982/10+	1982/4+
Price	$12,995	$80,000	$32,250	$16,000+ $23,000+
	Chromatics, Inc. 2558 Mountain Industrial Blvd. Tucker, GA 30084 (404) 493-7000	**Evans & Sutherland** 581 Arapeen Dr. Salt Lake City, UT 84108 (801) 582-5847	**Genisco Computer Corp.** 3545 Cadillac Ave. Costa Mesa, CA 92626 (714) 556-4916	**Grinnell** 6410 Via Del Oro Dr. San Jose, CA 95119 (408) 629-9191

Manufacturer	Hewlett-Packard	Ikonas	Japan Radio	Lexidata
Model	1345F	RDS-3000	NWX-220/230, NWX-225/235	2400; 2410, 8100/GS
Display Size/ Resolution	14", 17", 19", 21"/1024 x 1024	19"/1024 x 1024	19"; 25"/1024 x 1024	19"/1280 x 1024
Color Palette/ Displayable	Monochrome	16.7 million/1 million	4096/16 (230,235); monochrome (220,225)	Monochrome; 4096/16
Display Technology/ Refresh Rate	Vector/50 Hz random	Raster/N.A.	Raster/30 Hz interlaced	Raster/50-60 Hz non-interlaced; 30 Hz interlaced (2410 & 8100/GS)
Internal Graphics Processor	Discrete	Motorola 68000	32-bit dedicated	Motorola 68000 & proprietary (8100/GS)
Software	10186A binary graphing program, 52113A integral 60	IKASM micro-code, FORTRAN	GRAPAC written in FORTRAN IV	Plot 10 compatible, Eng. command set (2400 series) LX/GP1, ACM/SIGGRAPH Core (8100/GS)
Expandability	Removable I/O card	Parallel DMA or PIO, video digitizer, dual display, DAC	Add-on segment buffer-512 Kb (225/235), Emulator for IBM 3270 Series and Tektronix 4104 (220/230,235)	5 option slots, 3 RS232 (2400 series) 4 serial I/O ports, 2.25 virtual image (8100/GS)
Date Introduced/Units Placed	1980/500	N.A./100	1981; 1982/300; 150	1981-82/N.A.
Price	$11,950 +	$20,000 +	Contact manufacturer	$11,000; $15,495; $15,950 (mono), $20,050
	Hewlett-Packard 3000 Hanover St. Palo Alto, CA 94304 (415) 857-4101	Ikonas Graphics Systems, Inc. One Fortune Dr. Billerica, MA 01821 (617) 667-7070	Japan Radio Co., Ltd. 120 East 56th St. New York, NY 10022 (212) 355-1180	Lexidata Corp. 755 Middlesex Turnpike Billerica, MA 01865 (617) 663-8550

Manufacturer	Lundy	Megatek	Megatek	Metheus
Model	5470; R5680	6245; 6255	7245; 7255 & 7645; 7655	Omega 400 Series
Display Size/ Resolution	15", 19"/1536 x 1024; 19"/1280 x 1024	19"/1024 x 1024	Same	19"/1024 x 768
Color Palette/ Displayable	Monochrome; 4096/256	Monochrome; 8/8	Monochrome; 4096/16	16.7 million/256
Display Technology/ Refresh Rate	Raster/60 Hz interlaced	Raster/60 Hz non-interlaced; 30 Hz interlaced	Same	Raster/33 Hz interlaced
Internal Graphics Processor	Motorola 6809	AMD 2901	Same	AMD 2901 bit-slice
Software	FORTRAN subroutines	WAND core compatible, Template	Same	AXIA
Expandability	RS 232, 8-bit parallel interface, RGB output for hard copy	RS 232, keyboard, data tablet, digitizer, printers	Same plus IEEE or parallel interface	Host parallel, RS 232, IEEE, tablet port
Date Introduced/Units Placed	1981/40; 1982/N.A.	1981/N.A.	1981 & 82/N.A.	1982/N.A.
Price	$10,000 +; N.A	$17,900	$40,000 + & $50,000 +	$18,100
	Lundy Electronics & Systems, Inc. 1 Robert Lane Glen Head, NY 11545 (516) 671-9000	Megatek Corp. 3985 Sorrento Valley Blvd. San Diego, CA 92121 (714) 455-5590		Metheus Corp. 5289 NE Elam Young Pkwy Hillsboro, OR 97123 (503) 640-8000

High-Resolution Graphic Display Systems

Manufacturer	Norpak	Orcatech	Phoenix	Ramtek
Model	Visual Data Processor	Orcatech Graphic Computer	1024	9400 Series, 6412
Display Size/ Resolution	13", 19"/1024 x 1024	19"/1024 x 1024	19"/1024 x 1024	13", 19", 25"/1280 x 1024
Color Palette/ Displayable	4096/16	16.7 million/256	4096/16(4 bit), 16.8 million/ 256 (8 bit)	16.7 million/1.2 million; 256
Display Technology/ Refresh Rate	Raster/30 Hz interlaced	Raster/30 Hz interlaced	Raster/30 Hz interlaced	Raster/30 Hz interlaced
Internal Graphics Processor	AMD 2903	Intel 8086/8087	Intel 8086/8087	AMD 2900, Motorola 68000, Z80A; Z80
Software	FORTRAN subroutines	Operating system, FORTRAN, core graphics system, 2-D	CP/M 86, Pascal MT, C, BASIC; FORTRAN-77	FORTRAN subroutine library; None
Expandability	DMA interface, control unit, memory extension	Full serial & parallel access to host and output	10Mb hard disk, Centronics interface, input ports	To 32-bit planes, workstations, keyboards, cursors; to 8-bit planes, cursor, RS 232, data tablet
Date Introduced/Units Placed	1979/45+	1981/75+	1982/12	1979/575+; 1982/N.A.
Price	$38,718	$18,000 - $60,000	$27,300	$38,250; $19,600+
	Norpak, Ltd. 10 Hearst Way Kanata, Ontario K2L 2P4 (613) 592-4164	Orcatech, Inc. 2680 Queensview Dr. Ottawa, Ontario Canada K2B 8N6 (613) 820-9602	Phoenix Computer-Graphics 1309 W. Pinhook Rd. Lafayette, LA 70503 (318) 234-0063	Ramtek 2211 Lawson Lane Santa Clara, CA 95050 (408) 988-2211

Raster Technologies	Seiko Instruments	Transiac	Vector General	Vector Automation
ONE/40	CR2412	TR1024	VG8250; 3300; 3400	Graphicus/80
19"/1024 x 1024	19"/1024 x 780	15"/1024 x 780	21"/4096 x 4096	21"/4096 x 4096
16.7 million/64	40/7	Monochrome	4/4	Monochrome
Raster/30 Hz interlaced	Raster/36 Hz anti-aliased interlaced	Raster/60 Hz interlaced	Vector/40 Hz stroke	Vector/automatically adjusted to 60Hz
Z8002, vector generator, pixel AEU	Two Z8002's, Z80A	TI 9900	Bit-slice	Proprietary 16-bit bit-slice
Host command execution, local command with parameter passing, interactive debugger, local rubber-banding & dragging	FORTRAN call support	Tektronix 4010 compatible	FORTRAN library of subroutines	Mechanical, electrical
Keyboard, joystick, data tablet	Video output RS232	Up to 4 additional image planes	Standard I/O ports, host interface for DEC, Varian, Prime, SEL, IBM	6 RS232 I/O ports, parallel ports, to 56 workstations
1982/50+	1982/N.A.	1982/50	1981; 1977; 1975/N.A.	1981/70
$11,000 - $20,000	$21,850	$4,500	$230,000; $60,000+; $45,000	$28,500
Raster Technologies 9 Executive Park Dr. North Billerica, MA 01862 (617) 667-8900	Seiko Instruments USA, Inc. 2620 Augustine Dr. Ste. 140 Santa Clara, CA 95051 (408) 727-0768	Transiac 2375 Garcia Ave. Mountain View, CA 94043 (415) 969-0151	Vector General 21300 Oxnard St. Woodland Hills, CA 91367 (213) 346-3410	Vector Automation, Inc. Village of Cross Keys Baltimore, MD 21210 (301) 433-4202

2.5 TECHNOLOGY

Technology advancements critical to Aurora Include:

- ZMOS process for the MicroVAX chip and BIIC.
- CAD tools necessary for the execution of custom MOS development.
- BI physical interconnect including new module connector, I/O connector and backplane.
- 256K MOS RAM chip for memory.
- BI printed circuit board packaging technology.
- Winchester technology for RD5X disks.
- Custom pedestal air mover design--an existing technology, but new to Digital.
- Power supply design--an existing technology, but new to Digital.

Product positioning relative to state-of-the-art is characterized as:

- ZMOS process is state-of-the-art for Digital.
- As a system, Aurora is highly competitive, but not leading edge, state-of-the-art technology.

Likely replacement technologies include:

- CMOS Nano-VAX CPU.
- 1M bit MOS RAM for memory.
- Advanced Winchester technology for RDZX.
- Optical disk technology.

Chapter 3 SHIPMENT FORECAST

3.1 WORLD-WIDE FORECAST

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AURORA WORLD-WIDE SYSTEM/BOX/BOARD SHIP FORECAST

****

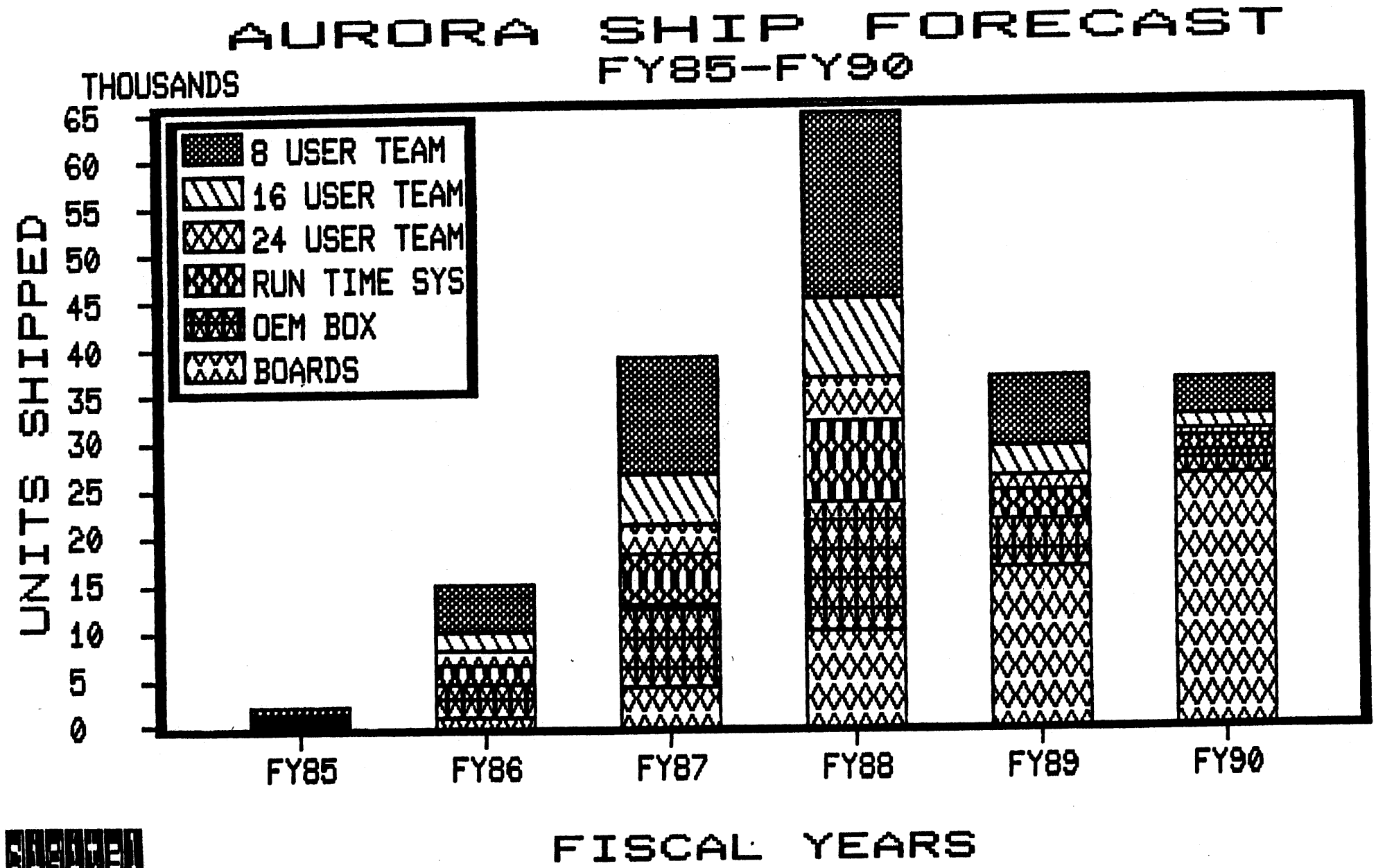
	FY85	FY86	FY87	FY88	FY89	FY90	FY85-90 TOTAL
TEAM MACHINE (1-9 USERS)	720	5040	12,600	19,800	7200	3600	48,960
TEAM MACHINE (10-16 USERS)	300	2100	5250	8250	3000	1500	20,400
TEAM MACHINE (17-24 USERS)	180	1260	3150	4950	1800	900	12,240
RUN TIME SYSTEM	300	2100	5250	8250	3000	1500	20,400
OEM BOX	500	3500	8750	13,750	5000	2500	34,000
TOTAL SYSTEMS/BOXES/SHIPS (1)	2000	14,000	35,000	55,000	20,000	10,000	136,000
BOARDS (2)	95	950	4000	9750	16,500	26,000	57,295

NOTES:

1) SOURCE: VAX Base Product Marketing and MicroVAX Program Office Top-Down Market Forecast

2) SOURCE: Components Group Forecast

3) This forecast represents opportunity space and is aggressive but achievable.


AURORA SHIP FORECAST
FY85-FY90
THOUSANDS
UNITS SHIPPED
65
60
55
50
45
40
35
30
25
20
15
10
5
0
8 USER TEAM
16 USER TEAM
24 USER TEAM
RUN TIME SYS
OEM BOX
BOARDS
FY85
FY86
FY87
FY88
FY89
FY90
FISCAL YEARS

[redacted]

3.1.1

AURORA TOTAL REVENUE PROJECTIONS @ $MLP
(FY85 - FY90)

FY85	FY86	FY87	FY88	FY89	FY90	TOTAL
78.4 M	550.6 M	1387.B	2203.B	887 M	561 M	5668 B

3.2 DETAILED WORLD-WIDE FORECAST BY APPLICATION AREA

Marketshare

The pedestal market is assumed to be in the $16-40K priceband. Based on available market forecast data, the following market projection of the $16-40K priceband was assumed (this is a projection of the total market including all architectures). The Marketshare information is based on work done by Joe Menard in the VAX Base Product Marketing group.

MARKET	FY84	FY85	FY86	FY87	FY88
UNITS (000's)	160	210	275	340	420

The market was then split by 5 generic application segments as follows (note that office includes word processing etc. for all offices, including technical offices).

UNIT AND % FORECAST BY APPLICATION
FOR THE TOTAL MARKET

	FY84	%	FY85	%	FY86	%	FY87	%	FY88	%
REAL TIME	16	(10)	20	(10)	25	(9)	32	(9)	40	(10)
WORKSTATION	10	(6)	20	(10)	35	(13)	47	(14)	57	(14)
OTHER TECH	57	(36)	63	(30)	70	(25)	74	(22)	84	(20)
OFFICE	45	(28)	65	(30)	90	(33)	119	(35)	155	(36)
COMMERCIAL	32	(20)	42	(20)	55	(20)	68	(20)	84	(20)
	160		210		275		340		420	

This represents our best estimate of how applications are likely to grow in the $16-40K.

Aurora Pedestal

The following marketshare figures in the table below were assumed to be reasonable marketshares for DEC with a full compliment of products (Mayflower and Aurora pedestals and Scorpio systems). These are some basic assumptions.

- Our share in the Real-time market is based on past successes with 16-Bit products. The BI is expected to be important in this market.
- Workstations growth reflects DEC's current push in that market. The BI should also be important here.
- We have traditionally been strong in Technical markets which should continue.
- The 15% Office share assumes whe have a well-integrated software package for the low-end office market.
- The Commercial forecasts also assume we have the necessary software to be successful.

MARKETSHARE ASSUMPTIONS BY SEGMENT

	FY84	FY85	FY86	FY87	FY88
REAL TIME	30	30	30	30	30
WORKSTATION	10	15	20	25	25
OTHER TECH	30	30	30	30	30
OFFICE	15	15	15	15	15
COMMERCIAL	10	10	10	10	10

Given the above marketshare assumptions, this table then represents DEC unit goals by Application. This is based on an assumption that a 20% share is aggressive but achievable.

$16-40K DEC UNIT GOALS

	FY84	FY85	FY86	FY87	FY88
REAL TIME	5	6	8	10	12
WORKSTATION	1	3	7	12	14
OTHER TECH	17	19	21	22	25
OFFICE	7	10	14	18	23
COMMERCIAL	3	4	6	7	8
TOTALS	33	42	55	68	83
MARKETSHARE	0.21	0.20	0.20	0.20	0.20

Based on the product requirements for each of the Application markets, we believe the distribution of products will be as follows: Aurora will be the choice in those applications where performance and 32-bit "bus-ness" is important while Mayflower will be preferred in applications where cost is the major issue.

FORECASTS ASSUMING AN AURORA PEDESTAL

	FY84	FY85	FY86	FY87	FY88
SEAHORSE	2	14	0	0	0
MAYFLOWER	0	9	25	30	25
AURORA	0	2	14	35	55
11/725	2	6	1	0	0
TOTAL	4	31	40	65	80
MARKETSHARE	0.03	0.15	0.15	0.19	0.19

Note: The differences in DEC's marketshare versus the pedestal forecast are DEC's 16-Bit products.

Revenue and Product Margin Impact

The Aurora pedestal should result in a product set that generates more revenue and product margin for DEC, based on the previous product forecasts. The resulting revenue and product margin impact is as follows.

Assumptions:

(a) Seahorse and 11/725 are ignored because of the minimal impact.
(b) Product Margin ignores Field and Corporate Costs.
(c) Mayflower product margin is 50% from Mayflower Business Plan.

(1) Aurora Pedestal

($M)

	FY84	FY85	FY86	FY87	FY88
Revenue					
Mayflower	—	225	625	750	625
Aurora	—	58	408	1031	1641
Total	—	383	1033	1781	2266
Product Margin					
Mayflower	—	112	312	375	312
Aurora	—	37	260	658	1048
Total	—	249	572	1033	1360

3.3 IMPACTED PRODUCTS: PHASEOVER PRODUCT SUMMARY

3.3.1 World-Wide System Phaseover Forecast Summary

The primary products impacted by Aurora are the VAX-11/725, VAX-11/730, and VAX-11/750. This data to be provided in a later revision of this document.

VAX-11/725 and VAX-11/730	Actual			Forecast				
	FY'82	FY'83	FY'84	FY'85 FR$	FY'86	FY'87	FY'88	FY'89
Unit Shipments #								
NES	$	$	$	$	$	$	$	$
Service Revenues	$	$	$	$	$	$	$	$
NOR	$	$	$	$	$	$	$	$

VAX-11/750	Actual			Forecast				
	FY'82	FY'83	FY'84	FY'85 FRS	FY'86	FY'87	FY'88	FY'89
Unit Shipments #								
NES	$	$	$	$	$	$	$	$
Service Revenues	$	$	$	$	$	$	$	$
NOR	$	$	$	$	$	$	$	$

3.3.2 IMPACT OF NOT BRINGING AURORA TO MARKET

Not bringing Aurora to market has an adverse effect on all market segments for which Aurora is intended. At the board level, a low-cost MicroVAX on the BI is considered essential by the OEM groups if we are to establish both the BI and the MicroVAX as industry leaders and design wins. Not having Aurora boards forces Scorpio boards to be the lowest-cost BI choice. To be competitive and protect the systems business, Scorpio board must be priced artificially low. This causes a ripple effect up through all Scorpio products, creating a much less favorable overall profitability to the corporation over the life of the Scorpio product set.

Additionally it is widely expected that if Digital does not put its new MicroVAX chip on its new 32-bit BI "bus for the future" as soon as possible, someone else will, thus eroding even further the potential VAX system base. Many important customers are eagerly awaiting an Aurora to help them stay competitive. They continually ask if we could deliver a system sooner than Q3FY85. When told that is our most realistic, aggressive but achievable commitment, most of them feel willing to wait (they say, "Good things are worth waiting for"). It is encouraging to note that recent MicroVAX presentations have already begun to turn the tide of 68000 design-starts. If VME and Multibus II are, as expected, found lacking versus the BI and if Aurora is the major thrust of the BI debut, it appears we truly can gain the 20% DEC market share goal by 1990.

The question of Q-bus/MicroVAX and BI-bus/MicroVAX has been analyzed. It appears that DEC wins if we have both products with workstations based on both and a clear migration path for both 16- to 32-bits and Q-bus to BI. The Add-On/Upgrade Group has an aggressive strategy to help maximize overall profitability for DEC.

Clearly, if DEC is to win in the next decade against fierce external competition, we must corporately plan a complementary product set which makes us appear as one company with a long-term, customer-oriented, overall product/services strategy. We must work together to help DEC succeed, or we leave ourselves wide open to the other vendors nipping at our heels, many of whom use our internal devisiveness to their advantage. Let's show them!!

CHAPTER 4 ASSUMPTIONS

4.1.1 Competition and Market

1. No major technological or manufacturing breakthroughs will occur which will alter the projected performance/price ratios of products available in the market.

2. Projected market size estimated by the 32-bit Program Office will remain essentially correct.

3. DEC marketshare can successfully grow from 12-14% to 19-20% by 1990 because of the penetration of additional markets.

4. There will be no mass exodus of DEC customers prior to introduction of Aurora.

5. IBM, ABI, and JAPAN INC. will be major competitive threats in the Aurora timeframe.

6. Major board-level competitors are assumed to be:

   - National--The 16032 is expected to be the primary competition, due to its architectural features and anticipated availability date.

   - Motorola--Although the 68000 series has become a well accepted architecture, the 68020 will not be available until after National's 16032. Thus, Motorola is assumed to be the number two competitor.

   - Intel--Intel is expected to be the number three competitor. Although the 432 was the first 32-bit chip to market, its success has been less than anticipated. It now appears that this architecture is being placed "on the back burner" in favor of the 386, an 8080 compatible 32-bit upgrade.

4.1.2 Geography

Aurora will be sold in all countries served by Digital and its distributors. However, this plan is subject to U.S. State Department approval of Aurora technologies being permitted into sensitive geographies such as communist bloc countries.

4.1.3 Regulatory Compliance

Aurora products take no exception to DEC STD 060, and plan to be UL, CSA and FCC certified, and VDE compliant.

4.1.4 Economic Factors

Sensitivity of revenue forecast/projections to (1) fluctuations in U.S. and international economies, (2) price/performance trends in Digital's markets, and (3) price elasticity of demand cannot be defined at this time.

4.1.5 Operating Environment

Aurora board sets, power supplies, and the OEM box all meet Class C requirements per DEC STD 062.

4.2 TECHNOLOGY

4.2.1 New Processes and Components

The following assumptions are made:

- The ZMOS process becomes mature and produces the necessary chips at cost goals, on schedules.
- The 50 mil center connector technology is available, reliable and meets specifications.
- NI lance chips available to specifications and on schedule.
- PCB technology can be manufactured cost effectively by Digital.
- Power supply available per specification and on schedule.
- New zif connector for BI logic modules will be available per specification and on schedule.
- 256K bit DRAMS will be available in quantities sufficient to meet Aurora requirements.

4.2.2 Design Tools

It is assumed:

1. That the VALID hierarchical design system is capable of meeting Aurora design and schedule.
2. Timing and simulation tools capable of meeting Aurora design requirements are available.

Much greater detail on design methodology and verification tools is available in the Project Plan.

4.2.3 Key Suppliers of Components

The following components are assumed to be available from their respective suppliers:

- 256K MOS RAMS: The industry
- 300 Pin Connector: Burndy
- NI Chips: AMD and Mostek
- Power Supply: Boschert

4.3 INTERNAL FUNCTIONS

The following assumptions highlight product requirements that cross functional and organizational lines.

4.3.1 Engineering Dependencies

- MicroVMS with Aurora support from BSSG.
- MicroULTRIX with Aurora support from BSSG.
- VAXElan with Aurora support from BSSG.
- RD52/RD53 disks from Storage Systems.
- MAYA streaming tape from Storage Systems.
- Aurora 2 MB memory arrays from Storage Systems.
- BI Combo Board from Distributed Systems.

4.3.2 High-Volume Manufacturing Dependencies

- Engineering to supply BI and NI test equipment per specifications and delivery schedule.
- Engineering to design self test diagnostics to a 90% level for all BI modules.
- Engineering to supply micro and macro diagnostics that provide 100% test coverage.

- Advanced Technology Group (ATG) to provide design and qualification of all BI module hybrids as well as associated assembly and test processes.

- ATG to provide development and qualification of new BI connectors, and an inspection process for 128-pin chip carriers.

- ATG to provide development and qualification of a process for fine line/controlled impedance/multi-layer/H3D printed circuit boards as required.

4.3.3 Final Assembly and Test Dependencies

- All system options to be site mergable.

- Mass storage assemblies to be site mergable.

- BI options to be easily installable by qualified customers.

4.3.4 Customer Services Dependencies

- Easily installable systems that include appropriate system packaging design, documentation, and carton labeling.

- Field Service installation available for a competitive/low price.

- A UETP replacement, currently being defined in a new systems acceptance procedure.

- Product Groups to provide warranty funding:

  - End User--90 days on site.
  - OEM--30 days on site.
  - Boards--Return to exchange facility.

- Manufacturing to deliver a high quality product.

- Engineering to design reliable hardware with self test features (90% level) on each BI module.

- RAMP must be designed in.

- All system components to meet their individual MTBF (BMC) goals.

- Training courses implemented as defined.

- Manufacturing to supply the required CD kits and spares per Field Service plan.

4.3.5 Marketing

Development priorities, as defined by Product Groups, are as follows:

1. Time to Market
2. Transfer Cost/MLP
3. Performance
4. Quality
5. Reliability/Availability

Product parameters of extreme importance to selected Product Groups include:

- Real time performance
- Office Packaging
- Public BI bus

Advertising and promotion priorities will be defined in later revisions.

4.3.6 Sales

Aurora distribution channels are as follows:

Market/Product Group	Distribution Channels
OEM Group	Direct Sales Industrial distribution Distributors
Technical Group	Direct end user Government end user Government prime contractors Medical OEM's
CAEM Group	Direct end user
Business and Office Systems Group	OEM's Distributors Retail stores
Add-on/Upgrade Group	Direct Sales

4.3.7 Asset Management

The Stage 2 inventory goal is 8 weeks maximum in FY85, falling to 3.9 weeks in FY87. The overall inventory goal will be defined in future business plan revisions.

The Days Sales Outstanding (DSO) goals cannot be identified at this time.

4.4 CUSTOMERS

4.4.1 Impact on Key Accounts

Aurora is expected to have major positive impact on key customers and many have requested early non-disclosures to allow them ample design-in/and planning time before FRS. Some representative comments follow which further describe the impact expected:

> "Aurora--the price/performance leader. A critical product for capturing OEM designs against Motorola, Intel and National chip-based solutions. A high-volume product sold in low-end systems ($16-40K) and as a component. Will be the preferred 32-bit CPU for most OEM applications: CAD/CAM (workstations), process control, telecommunications, etc."
>
> "Medical field requirements for both Aurora and Scorpio appear to be excellent. We would anticipate that 75% of the Medical OEM's will switch their product offerings to these products within the first year of introduction because of cost and potential redundancy due to the BI. Medical OEM's are especially well-suited to convert easily due to their value added being mostly, if not all, software. The current projected Medical OEM business is $30 million and is expected to grow at a 35% rate compounded for the next three to five years."
>
> "The End User environment is somewhat difficult in that most systems are sold with specific applications in mind, and we would see conversion taking somewhat longer. End-user sale for this product would be in the $6 to 8 million range in FY85, $10 to 12 million in FY86. The Medical Group would focus on these new products very heavily and push the networking cpabilities plus the capability of increase in performance as more applications come on line."
>
> "This MicroVAX - VAX implementation will be attractive in the Education market as a low-end ULTRIX system particularly in Computer Science departments and in smaller departments requiring entry-level systems with reasonable performance levels. A specific configuration is ULTRIX - based PRO 350-networked to Aurora ULTRIX Systems. We expect third party vendors to develop applications for Aurora using VAXElan."

4.4.2 New Opportunities

Aurora boards and systems are expected to help Digital achieve new market opportunities for emerging markets such as workstations, robotics, and expert systems. More details will be provided in a later revision of this document.

4.5 SCHEDULES

4.5.1 Project Schedule

See Page 9 of Project Plan Part II 3.3.5.0, Aurora Systems Integration---Milestones.

See Section 1.6 Phase Planner for tentative schedule. More detailed schedule and commitments will be made upon Phase 1 exit.

4.5.2 Phase Planners

Phase Planners follow on the next three pages.

PHASE REVIEW PLANNER

17-November 1983
REVISION DATE

PROJECT NAME: AURORA

PROJECT TEAM

Product Manager: Jan Tuttle
Program Manager: Bill McBride
Engineering Manager: Pauline Nist
Manufacturing: Peg Wesley
Customer Services: Ted Gent
Project Start Date (Actual): FY'83

Phase	Title	Estimated/Actual Completion Date
Phase 0	Strategy & Requirements	November 1983
Phase 1	Planning	Q3 FY'84
Phase 2	Implementation	Q4 FY'84
Phase 3	Qualification	Q4 FY'85
Phase 4A	Engineering, Manufacturing Transition	TBD
Phase 4B	Manufacturing Volume Production	TBD
Phase 5	Retirement	TBD

FIRST REVENUE SHIP:

Aurora Board Sets	Q3 FY'85
BI Interface Chips	Q3 FY'85
Aurora Systems	Q3 FY'85

PHASE REVIEW PLANNER

PHASE 0

STRATEGY AND REQUIREMENTS

PRODUCT NAME: AURORA

PRODUCT MANAGER: Jan Tuttle LOC: LTN1-1/D03 DTN: 229-6350

PROGRAM MANAGER: Bill McBride LOC: LTN1-1/D03 DTN: 229-6341

MILESTONE	RESPONSIBLE INDIVIDUAL	COMPLETION DATE		LATEST FORECAST
		ORIG PLAN	ACTUAL	
1. Business Plan (Preliminary)	Jan Tuttle			November 83
2. Market®Product Requirements Document	Jan Tuttle			November 83
3. Alternative/Feasibility Examined	Pauline Nist			November 83
4. Manufacturing Impact Statement	Peg Wesley			November 83
5. Customer Services Impact and Requirement Statement	Ted Gent			November 83
Phase 0 Complete	Jan Tuttle			November 83

Date: 17 November 1983

Rev: 0

PHASE REVIEW PLANNER

PHASE 1

PLANNING

PRODUCT NAME: AURORA

PRODUCT MANAGER: Jan Tuttle LOC: LTN1-1/D03 DTN: 229-6350

PROGRAM MANAGER: Bill McBride LOC: LTN1-1/D03 DTN: 229-6341

MILESTONE	RESPONSIBLE INDIVIDUAL	COMPLETION DATE		LATEST FORECAST
		ORIG PLAN	ACTUAL	
1. Business Plan	Jan Tuttle	Q3FY84		Q3FY84
2. Functional Specification	Brian Allison	Q3FY84		Q3FY84
3. Project Plan	Pauline Nist	Q3FY84		Q3FY84
4. Manufacturing Plan	Peg Wesley	Q3FY84		Q3FY84
5. Customer Services Plan	Ted Gent	Jan 84		Jan 84
Phase 1 Complete	Jan Tuttle			Q3FY84

Date: 17 November 1983

Rev: 0

CHAPTER 5

FINANCIAL/SENSITIVITY ANALYSIS

5.1 SUMMARY AND CONCLUSIONS

The objective of this system level financial analysis is to evaluate whether or not the Aurora engineering goals for prices, transfer costs, volumes, development costs, etc. will provide the corporation with a financially viable product.

The analysis covers the entire expected life of the Aurora product (FY83-FY91), and contains numerous assumptions because Aurora is early in the development cycle and because of the aggressiveness of the development team goals. Special attention should therefore be paid to the sensitivity analyses included as Section 5.6.

Results of the Base Case Analysis show the Aurora combined System and Board products yielding a 61.8% Internal Rate of Return (IRR)* and a Net Present Value (NPV) at 40% of $64.7M. Breakeven is reached 10 quarters after an expected FRS of Q3 FY85. These metrics are similar to other low-end 32-Bit product analyses at Phase 0.

Major assumptions include an Average System and Board set MLP of $34,495 and $6,623 respectively (with FY87 transfer costs of $9,250 and $1,758) and a shipment forecast of 136,000 systems and 57,295 Boards between FY85 and FY90. 36% of the systems are expected to be color workstations.

Development costs include 34% of the cost of developing the MicroVAX chip, 48% of BI development costs and 16% of the BICOMBO. All allocations were made on the basis of lifetime estimated Aurora chip usage as a percentage of total chips used in all relevant products (Mayflower, Scorpio, and Nautilus).

Development costs also include 100% of the expected WS32 development effort.

Sensitivities performed around major assumptions showed that transfer cost was the most sensitive factor impacting Aurora profitability. Price increases impacting volume were second, followed by adverse changes in volume not caused by higher pricing. Finally, inventory management was considered to be important, particularly as a means of minimizing financing requirements caused by adverse cash flows associated with rapid shipment and build ramps.

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*without asset factors. For an analysis with asset factors, see Section 5.6.

Sensitivity findings are summarized below:

VARIABLE CHANGED	IMPACT
Transfer costs increase 10%	NPV falls to $43.6M (33% decrease)
Prices increase 10%, volumes decrease 20%	NPV falls to $56.4M (12.8% decrease)
Shipments decrease 10%	NPV falls to $54.6M (15.6% decrease)
Inventories increase 20%	Cash requirements in FY87 increase by $29.5M (19.6% increase)
2 Qtr FRS Slip	21% decrease in shipments, NPV falls to $42.5M (34% decrease)
Mid-Life Repricing (-15%)	NPV falls to $43.6M (33% decrease)

An analysis performed using the "Baseline" shipments from Section 4.2 of the Manufacturing Impact Statement Executive Summary was performed. These shipments may be thought of as a 90% confidence near "worst case" minimums (as opposed to "opportunity space" numbers).

Using these numbers (peak year systems shipments equalling 20,800 units), Aurora is still a financially viable product, with an IRR of 46.3% and an NPV of $12.1M. Gross Margin is $1443M with total lifetime NOR of $2495M. Shipments 53% below the Base Case thus reduce IRR by 25% and NPV by $52.6M.

5.2 FINANCIAL BASE CASE ANALYSIS -- NUMERICAL SUMMARY*

	FY83-FY91 ($M)
Total Net Operating Revenue (Equipment & Service)	$ 4,688
Less: Cost of NOR	1,903
Gross Margin	2,786
Gross Margin as % of Total NOR	59%
Less: Development Expense	98
Selling, Marketing, G & A Expense	1,122
Profit Before Tax	1,566
PBT as % of Total NOR	33%
Profit after Tax (Tax Rate = 38%)	971
After Tax NPV @ 40%	64.7
After Tax IRR	61.8%
Breakeven Date	Q2 FY88 (Oct'87)
Number of Quarters to Breakeven from System FRS	10
Development Expense as % of Total NOR	2.3%

*Analysis was performed using the Business Review Program (BURP).

5.3 FINANCIAL MODEL ASSUMPTIONS

The following are the major assumptions used in the Aurora BURP Analysis:

1. Ship Forecast

The ship forecast for Aurora Systems and CPU Boards is as follows:

	FY85	FY86	FY87	FY88	FY89	FY90	TOTAL
Systems/Boxes	2000	14000	35000	55000	20000	10000	136000
Boards	95	950	4000	9750	16500	26000	57295
TOTAL	2095	14950	39000	64750	36500	36000	193295

FRS for Aurora Boards and Systems is Q3 FY85. The System's forecast is from Aurora product management. The Board's forecast is from TOEM-Microcomponents.

2. Transfer Cost

Aurora Manufacturing Finance provided the following transfer cost goals. Configurations were provided by Aurora Product Management.

	FY85	FY87	FY89
1-8 User "Team Machine"	$8744	$5434	$4966
Run Time System	5735	3493	3291
CPU Board	1831	1003	1003
Avg Configured System	13870*	9250	8554
Avg Board	3186	1758	1664

*includes some relatively high cost (& high MLP) Jasper Workstations in FY85 weighted average. Later years incorporate less expensive WS32 product.

3. MLP

Systems MLPs were proposed by Aurora product management and board MLPs by TOEM-Micros. All MLPs are held constant throughout the estimated life of the product. All Systems MLPs include a MicroVMS Kernal UZ License.

	MLP	Markup (FY87)
1-8 User "Team Machine"	$21000	3.86
Run Time System	14000	4.01
CPU Board	2700	2.69
Avg Configured Sytem	$34495	3.73
Avg Board	6623	3.77

Add-on's shipped with a system Represented 47.6% of System MLP with a 3.55 mark-up. Boards add-ons represented 59.2% of MLP with a 5.2 markup.

4. Engineering Hardware Development Expense

Engineering hardware development expense includes a burden rate to reflect additional engineering costs for non-product related projects within 32-Bit systems and Central Engineering. Mass Storage, MicroVAX Chip, Workstations, and BI expenses are an allocation of development costs based on the lifetime number of each device expected to ship with Aurora as a percentage of the total for each device expected to ship with all CPU products and as an add-on.

($K)

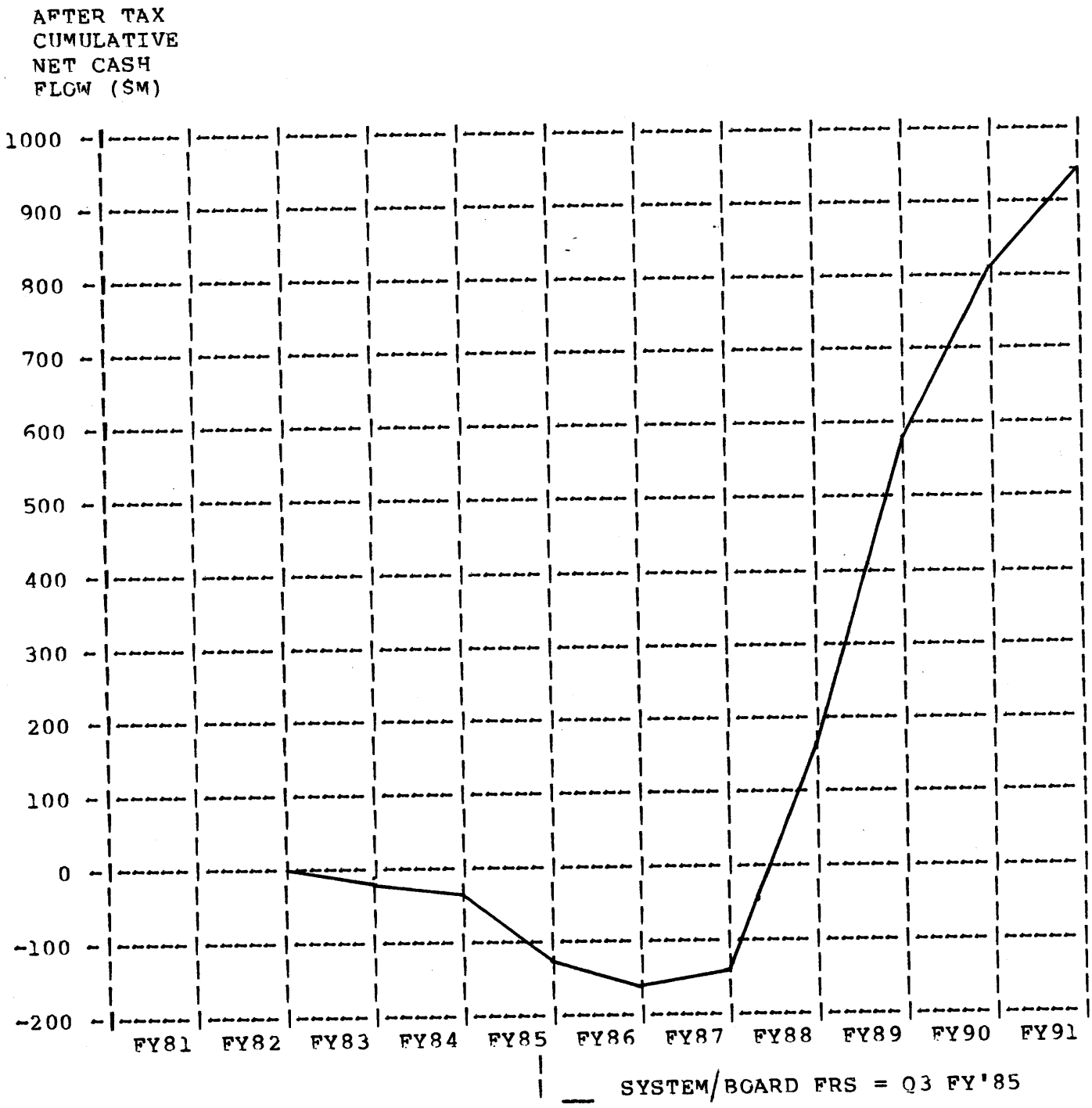
Mass Storage	FY83	FY84	FY85	FY86	FY87	FY88
RX50 Burdened	3123.0	606.0	657.0	--	--	--
Aurora Alloc. (1)	384.0	75.0	81.0	--	--	--
RD53 Burdened	--	850.0	1131.0			
Aurora Alloc. (2)	--	795.0	1058.0	500.0*	250.0*	250.0*
Maya Burdened	5493.0	7878.0	6868.0			
Aurora Alloc. (3)	776.0	1112.0	970.0	500.0*	250.0*	250.0*
Workstations						
Jasper Burdened	3656.0	6426.0	1702.0	616.0	352.0	--
Aurora Alloc. (4)	59.0	103.0	27.0	10.0	6.0	--
WS32 Burdened	--	3200.0	4000.0	800.0	350.0	--
Aurora Alloc. (5)	--	3200.0	4000.0	800.0	350.0	--

32-Bit

	FY83	FY84	FY85	FY86	FY87	FY88	FY89	FY90
MicroVAX Chip**	1485.0	2393.0	1786.0					
Aurora Alloc	500.0	806.0	601.0					
BI Development**	2624.0	3571.0	2225.0	1100.0				
Aurora Alloc	1260.0	1714.0	1068.0	528.0				
BICOMBO**	45.0	868.0	600.0					
Aurora Alloc	7.0	139.0	96.0					
32-Bit Engin**	658.0	4902.0	7056.0	3000.0				
Total Engin	2425.0	7561.0	8821.0	3528.0				
Burdened (6)	5675.0	18373.0	21435.0	8573.0	3400.0*	2600.0*	1700.0*	1000.0*
TOT HW Devel (Sum 1-6)	6894.0	23658.0	27571.0	10383.0	4256.0	3100.0	1700.0	1000.0

*32-Bit Finance Assumption.
**Unburdened.

5.4 CUMULATIVE CASH FLOW GRAPH



5.5 BURP FINANCIAL STATEMENT

A copy of the Aurora Pro Forma Financial Statement (from the BURP analysis) is provided on the next page.

11-NOV-83

AURORA PHASE 0

PRODUCT

STATEMENT OF OPERATIONS

$ THOUSANDS

	FY83	FY84	FY85	FY86	FY87	FY88	FY89	FY90	FY91
NO. OF UNITS	0	0	2,095	14,950	39,000	64,750	36,500	36,000	0
MLP/UNIT	0	0	35,638	32,725	31,637	30,298	21,894	14,363	0
TRANSFER COST/UNIT	0	0	13,384	9,505	8,484	7,835	5,520	3,617	0
SALES AT MLP	$0	$0	$74,661	$489,232	$1,233,837	$1,961,820	$799,148	$517,079	$0
UPLIFT	0	0	4,330 5.8%	28,375 5.8%	71,563	113,786	46,351	29,991	0
GROSS EQUIPMENT SALES	0	0	78,991	517,607	1,305,399	2,075,605	845,499	547,070	0
ALLOWANCES	0	0	2,314 3%	15,166 3%	38,249	60,816	24,774	16,029	0
QUANTITY DISCOUNTS	0	0	14,634 20%	95,889 20%	241,832	384,517	156,633	101,347	0
NET EQUIPMENT SALES (2% MLP)	0	0	62,043 83	406,551 83	1,025,318	1,630,272	664,092	429,693	0
SERVICE REVENUE	0	0	825 1.3% NORT	7,945 2%	31,749 3%	77,390	120,736	142,886	88,892
OTHER INCOME	0	0	0	0	0	0	0	0	0
NET OPERATING REVENUE	0	0	62,868	414,497	1,057,067	1,707,662	784,828	572,579	88,892
TRANSFER COST	0	0	28,039	142,102	330,864	507,344	201,466	130,198 1340	0
CORP MFG. CHARGE	2,947	4,396	3,148 ✓	12,197	26,658	42,387	17,266	11,172 #2.9	0
FA&T INV. PROVISION	0	0	0	0	0	0	0	0	0
FA&T COST	0	0	1,493	9,785	24,677	39,236	15,983	10,342	0 101.5
OTHER COS	0	0	0	0	0	0	0	0	0
SERVICE EXPENSE	0	0	665	5,482	21,675	52,429	81,182	95,859	52,745 310.9
HARDWARE WARRANTY	0	0	1,816	2,539	6,522	9,769	5,194	5,111	0 30.9
SOFTWARE WARRANTY	0	0	0	0	0	0	0	0	0
TOTAL COS	2,947	4,396	35,162	172,105	410,396	651,165	321,091	252,682	52,745
GROSS MARGIN	(2,947)	(4,396)	27,706	242,392	646,672	1,056,497	463,737	319,897	36,148
PL MKT/ADM/ADV	0	0	0	0	0	0	0	0	0
PL DIRECT SELLING	0	0	0	0	0	0	0	0	0
PL BAD DEBT	0	0	186	1,220	3,076	4,891	1,992	1,289 12.7	0
PL ENGINEERING	0	0	0	0	0	0	0	0	0
CORP SELLING	0	0	8,872	58,137	146,621	233,129	94,965	61,446 603.1	0
CORP MKT/ADV	0	0	4,963	32,524	82,025	130,422	53,127	34,375 337.5	0
CORP ENGINEERING	7,088	23,960	28,215	12,431	8,602	9,767	7,414	1,000 98.5	0
CORP MFG. PROJECTS	0	0	310	2,033	5,127	8,151	3,320	2,148	0 21
ADMIN G&A EXPENSE	0	0	2,012	13,264	33,826	54,645	25,115	18,323	0 147.2
OTHER <INC> EXP (EX INT)	0	0	0	0	0	0	0	0	0
TOTAL EXPENSES	7,088	23,960	44,559	119,608	279,277	441,005	185,934	118,582	0
OPERATING PROFIT	(10,035)	(28,356)	(16,852)	122,784	367,395	615,492	277,803	201,316	36,148
TAXES	(3,813)	(10,775)	(6,404)	46,658	139,610	233,887	105,565	76,500	13,736
OPERATING PROFIT AFTER TAXES	(6,222)	(17,581)	(10,449)	76,126	227,785	381,605	172,238	124,816	22,411

11-NOV-83

AURORA PHASE 0
=========
CASH FLOW
=========
$ THOUSANDS

	FY83	FY84	FY85	FY86	FY87	FY88	FY89	FY90	FY91
OP PROFIT AFTER TAX	($6,222)	($17,581)	($10,449)	$76,126	$227,785	$381,605	$172,238	$124,816	$22,411
PLUS: DEPRECIATION PP&E	404	1,219	2,500	2,493	1,706	1,150	883	11	0
MINUS: A/R INCREASE	0	0	15,717	87,907	160,643	162,649	(230,709)	(53,062)	(120,922)
MINUS: INVENTORY INCREASE	0	0	60,523	39,540	50,567	(94,978)	(19,040)	(33,801)	(2,810)
MINUS: PP & E INCREASE	1,617	2,563	5,567	565	54	0	0	0	0
PLUS: OP. LIAB. INCREASE	0	0	0	0	0	0	0	0	0
PLUS: BUYBACK	0	0	0	0	0	0	0	0	0
EQUALS: NET CASH FLOW	(7,434)	(18,925)	(89,756)	(49,393)	18,227	315,085	422,870	211,690	146,143

NPV @ 40% HURDLE = $ 64730 K
IRR = 61.8 %

MARKUP (LIFETIME) = 3.8 TIMES
MAX. NEG. CASH FLOW = $-165508 K
5-YEAR COST-OF-OWNERSHIP = $41167

DEVEL. PERIOD TO FRS = 11 QTRS (FRS = Q4 FY85)
CASH PAYBACK FROM FRS = 10 QTRS (PAYBACK = Q2 FY88)
BMC % MLP = 0.3 %

5.6 SENSITIVITY ANALYSIS

Sensitivity analyses were performed on the major variables that could determine the financial performance of Aurora. Information gained from these sensitivities may be useful in focusing on elements which would minimize product risks and maximize life cycle profitability.

Transfer Cost — Product profitability was more sensitive to changes in transfer cost than any other element. Increased transfer cost is a two-edged sword: in a competitive environment, it reduces margins while also increasing the cost of carrying inventory. A 10% increase in transfer cost reduces gross margin from $2.79B to $2.65B or only 5%, but decreases profitability as measured by NPV from $64.7M to $43.6M, or 32.6%

Price/Volume — Aurora profitability would be hard hit if a price decrease of 10% increased volumes by 20%. Net present value falls by $11.6M, to $56.4M. Similarly, a price increase of 10% resulting in 50% fewer shipments decreases NPV to $24.4M, a decline of 55%.

Shipments — A 10% decrease in shipments reduces net present value by 15.6%, or $10.1M, and gross margin by 9.9%, or $276.4M. Changes in expected volume are exceeded in importance only by transfer cost and pricing in terms of impact on profitability.

Inventory — Changes in inventory requirements impact cash flow and profitability. A 20% increase in inventory increases the corporation's cash requirements associated with Aurora by $29.5M in FY87, or 19.6%. In addition, it reduces net present value by approximately 9.7%.

FRS 1 & 2 Qtr Slips — A one quarter slip in FRS (from Q3 FY85) would be expected to reduce first year ships by 32% and shipments thereafter by 10% annually. The financial results include a 16.5% decrease in NPV (from $65M to $54M) and a small reduction in IRR (61.8% to 59.5%). A two quarter slip would result in no FY85 shipments, a 20% reduction in units shipped thereafter, and a consequent 34% drop in NPV to $42.5M. In either case, Aurora remains financially viable.

Mid-Life Repricing	Although the Aurora Base Case BURP assumes a constant MLP throughout the product life cycle, a mid-life repricing might reasonably be expected. A 15% price cut on Day 1 of FY88 impacting all Aurora Systems $ Boxes (not boards) yields an IRR of 55.7%, and NPV of $43.6M, and lifetime NOR and Gross Margin of $4,323M and $2,439M, respectively. No incremental units were assumed. The 15% price decrease reduces FY89 gross margins by only 5% compared to FY86 because of expected manufacturing cost reductions.
Manufacuring Base Case	An analysis was performed using the base case shipment forecast of Aurora manufacturing management. A 53% decrease in Systems shipments reduced IRR by 25.1%, but the product still cleared the 40% hurdle rate at 46.3%. Lifetime gross margin declined to $1,443M from $2,785M.
Corporate & Mfg Asset Factors	A BURP analysis using corporate asset factors, which allocate non-specific product costs based on system family, yielded an IRR of 43.9%

CHAPTER 6 REFERENCE DOCUMENTS

DOCUMENT	REVISION	DATE PUBLISHED	ISSUED BY
VAX SYSTEMS DEVELOPMENT			
AURORA Product/Market Requirements	1.0	22 Nov 83	Jan Tuttle
AURORA Alternatives/Feasibility Study			Pauline Nist/ Brian Allison
AURORA System Specificaton		17 Nov 83	Brian Allison
AURORA System Functional Specs			
AURORA Systems	1.0		Brian Allison
AURORA Central Processor Module (ACP)	1.1	15 Nov 83	Dennis Hayes
AURORA Console Specification	2.0	11 Nov 83	Jerry Stark
AURORA Memory Extension (AME)			TBD
AURORA I/O Modules (AIO/AIE	1.0		Dick Binder Don Dossa
AURORA Control Panel			TBD
AURORA Pedestal Mechanical			Charlie Barker
AURORA Pedestal Power System			Charlie Barker
AURORA Project Plan		Nov 83	Pauline Nist
MicroVAX Specification			Dileep Bhandarkar
BI Specification	2.0		Frank Bomba
BI Architecture	1.1		Bob Chen
BI Interface Chip Specification	1.3		Rick Gillette
BI Clock Driver	2.0		Frank Bomba
BI Clock Receiver	2.0		Frank Bomba
BI Physical Interconnect	1.3		Bob Willard
BCI3 Chip Specification			Flavio Rose
AURORA Program PERT		Nov 83	Pauline Nist/ Peg Wesley

DOCUMENT	REVISION	DATE PUBLISHED	ISSUED BY
AURORA Financial Analysis -- Phase 0		16 Nov 83	John Coombs
Diagnostic Engineering Project Plan for the AURORA System	1.0	3 Nov 83	Roger Andersen
VAX Systems LRP			Ken Nisbet/ Joe Menard
VAX Component Revenue Sources		30 Sept 83	Carl Gottleib
SEMICONDUCTOR ENGINEERING GROUP			
Microvax 32000 Product Update		Oct 83	Randy Spears
32-Bit Supermicro Product Analysis		16 August	Randy Spears
STORAGE SYSTEMS ENGINEERING GROUP			
Electronic Memories World-Wide Business Forecast--FY83 - FY88		1 April 83	Durant/Herman/Haley/ Cullen
MAYA Business Plan -- Phase 0		Oct 82	Larry Tashbook
MSCP Protocol	1.2		Ed Gardner
DISTRIBUTED SYSTEMS ENGINEERING GROUP			
BI Combo Business Plan		8 Sept 83	Lloyd Atkinson
BI Combo Product Requirements		29 July 83	Lloyd Atkinson
Ethernet Lance Chip Spec	1.0		Mike Carrafiello
NI MOP Spec	3.0		Ken Chapman
ULTRIX BASE PRODUCT ENGINEERING GROUP			
VAX UNIX Market Requriements Document	Rev. 2.0	11 July 83	Bernie Toth
MicroULTRIX V1.0 Product Requirements Document		24 Oct 83	Bill Doll
ULTRIX/MicroULTRIX Business Plan	1.0	24 Oct 83	Bill Doll

DOCUMENT	REVISION	DATE PUBLISHED	ISSUED BY
VMS ENGINEERING GROUP			
VMS/MIDNITE Version 1 Business Plan		August 82	Dick Angel
VMS/MIDNITE Version 1 Product Requirements	0	August 82	Dick Angel
VMS MIDNITE Version 1 Market Requirements	0	August 82	Dick Angel
VAX WORKSTATION PROGRAM			
VAXstation 300 (AGATE) Business Plan	1.0	19 July 83	John Stefanowicz
Workstation competition	--	1 June 83	John Stefanowicz
WS32 Product Requirements Document	.2	17 Oct	Ron Setera
ARTIFICIAL INTELLIGENCE TECHNOLOGY CENTER			
VAX-11 LISP Version 1.0 Phase 0/1 Document		10 May 83	Norma Abel/ Bob Abramson
MicroVAX PROGRAM OFFICE			
MicroVAX Product Family and their Related Mass Storage Requirements		4 May 83	Kaj Larsen
The MicroVAX Product Family in a DEC Distributed Environment		29 June 83	Kaj Larsen
MicroVAX Business Plan--Preliminary		1 Nov 83	MicroVAX Program Team

DOCUMENT	REVISION	DATE PUBLISHED	ISSUED BY
SALEM VOLUME MANUFACTURING			
AURORA Manufacturing Impact Statement -- Phase 0	1.0	31 Oct 83	Peg Wesley
CUSTOMER SERVICES SUPPORT ENGINEERING			
AURORA Customer Services Impact Statement		Nov 83	Ted Gent
Reliability Predictions for AURORA Components		3 Nov 83	Bill Peters
INTERNATIONAL PRODUCTS GROUP			
Guidelines for the Design of International Products		August 1983	John Atkins/ Frank Feigin
International Power Cables and Connectors Technical Bulletin		August 1983	Frank Feigin
MARKET GROUPS			
Commercial OEM Low-End VAX Product Requirements			Len Slosek
COMDEX Feedback		12 May 83	Len Slosek
European View of MicroVAX		June 83	Marc Zavadil
BI Processor Strategy		14 Sept 83	Rich Lewan/ Chris Reed
OEM BI Product Forecasts		20 Oct 83	Tim Mackey
MicroVAX Board Forecasts		25 Oct 83	Tim Mackey
New Products/Markets Expected: Image Processing		15 Sept 83	Tom Austin

DEC Standards

DEC standards which relate to Aurora systems.

002	AC Power Wiring and Safety
003	Hardware Manuals
030	Module Manufacturing (must be updated for BI modules)
032	VAX SRM (must be updated for MicroVAX)
038	System Evaluation
041	Customer Installability
042	Hardware Installation Manuals for Customer Installability
051	Coded Character Set
052	RS-232/V.28 Interface (the KDZ does not conform)
060	National and International Hardware Product Standards
102	Environmental Standards
103	FCC Labeling
104	Acoustic Noise
106	In-house Acceptance Procedures
111	Terminal Synchronization
116	Workmanship Standards
119	Product Safety
122	A.C. Power Lines
123	Power Control Bus
126	Packaged Systems Documentation
139	Reliability Prediction
158	Unibus Interface Specification
176	Printed-wiring Board Acceptance Criteria
178	Marking Standard
186	Signal Integrity

CHAPTER 7 BUSINESS PLAN HISTORY/CHANGES

7 BUSINESS PLAN HISTORY/CHANGES

For the initial plan and each subsequent revision, complete this form. The objective is to enable readers to quickly understand how the plan has been revised over time.

Dev. Phase	Rev. Date	Goals/ Description	Prod. Announcement	FRS	Phase Completion Dates						Avg. MLP/TC	Unit Ships Ext./Int.	%Gross Margin & NOR	IRR %	NPV @ 40 %	Total Development Budget		
					0	1	2	3	4	5						Eng.	Mfg.	Svce.

digital

uVAX Monthly Product Update

Like progress itself, the LSI group won't stand still. In 1984, we will produce more semiconductor designs then all previous years combined.

For this reason, we've decided to produce a monthly product bulletin that will help keep you in tune with the current products being developed and how they progress, along with questions and answers to important topics that affect us all.

The uVax Chip

The Digital uVAX32000 CPU chip will soon be widely acclaimed as one of the best performing low cost 32-bit microprocessor in the industry. And, there are efforts being made to extend its performance by adding a floating point unit, along with a variety of state-of-the-art peripherals chips and development tools, making this a well rounded product line.

uVax32000, October Status

The uVax32000 CPU chip logic and circuit design are 100% complete, and all sections of the device have been simulated using RSIM. As far as layout is concerned, there are fewer than 1000 unique transistors not yet laid out.

The preliminary data sheet for the uVAX32000 is now complete and can be obtained from the uVAX product manager. Send mail to SNICKR::SPEARS or call DTN-225-5175.

Product Schedules

The following is a chart showing the status of the uVAX32000 and uVax Chip family.

LSI CHIP PRODUCT SCHEDULES

PRODUCT	1st PASS PG	2nd PASS PG	LIMITED RELEASE	PRODUCTION RELEASE	COMMENTS
uVAX CPU	JAN 84	APR 84	AUG 84	TBD	
uVAX FPU	NOV 83	APR 84	AUG 84	TBD	
uVAX VDMA	Q2 FY85	Q3 FY85	Q4 FY85	TBD	
uVAX MEMC	Q2 FY85	Q3 FY85	Q4 FY85	TBD	
uVAX VIC	TBD	TBD	TBD	TBD	TBD AFTER RISK EVAL

APPENDIX B

VAX MARKET SHARE

The market share goals for our full spectrum of VAX products is predicated on the market definition specified in the Market Analysis section. In summary, this VAX market is defined as:

- Worldwide shipments of less than $1.6M computer systems (if-sold value).
- U.S. vendors only (foreign vendors to be added later).
- Excludes service and aftermarket add-ons.
- Processors must have at least 24-bits addressing/ data-path/ALU, except for significant 16-bit competitors. (Tandem and HP)

The market share goals were set by examining the size of this market and establishing an aggressive, yet realistic, goal for capturing a share of this market consistent with our financial objectives. Figure 5-8 illustrates the market shares for MicroVAX and VAX system products, including software.

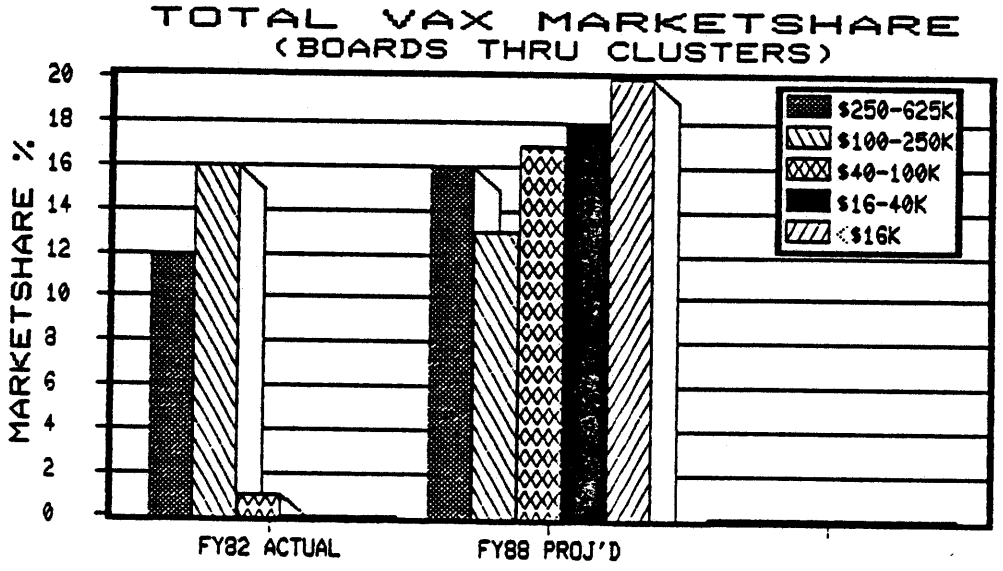


Figure 5-8

The following charts illustrate in more detail the composition of our $16K-$625K VAX system revenues. A similar analysis of MicroVAX and VAXstation revenues, as well as greater than $625K revenues, is currently underway.

VAX REVENUE OBJECTIVE

$16K - $625K SYSTEMS ONLY

32-Bit Systems Market ($B)	Fiscal Years						CAGR
	82	84	86	88	90	92	%
$16K-$625K Systems	7.2	13	21	31	44	56	23%

VAX Revenue Goals ($M)	(act)					
	82	84	86	88	90	92
$250-625K $	463	638	1155	1876	2495	3500
Market Share	12%	11%	13%	16%	16%	18%
$100-250K $	375	667	752	993	1195	1450
Market Share	16%	17%	13%	13%	12%	12%
$40-100K $	2	293	567	1002	1715	2350
Market Share	1%	17%	15%	17%	21%	22%
$16-40K $	0	63	400	940	1820	2800
Market Share	0%	8%	18%	18%	20%	22%
Total $16K-625K $	840	1661	2874	4766	7225	10100
Market Share VAX ($16K-625K only)	12%	13%	14%	15%	17%	18%
IBM	41%					
HP	7%					
Prime	4%					
Tandem	3%					
PE	2%					
SEL	2%					
DG	2%					
Other	27%					

Note: $100-250K market share decreases because 750-level uniprocessor revenues will be replaced largely by Scorpio VAXcluster and Scorpio-MP sales, many of which appear in the $40-100K priceband.

VAX Revenue Composition

Figure 5-9 illustrates the changing composition of the VAX business which is evolving from a high-end business (11/780) to a balance of low-, medium-, and high-end businesses.

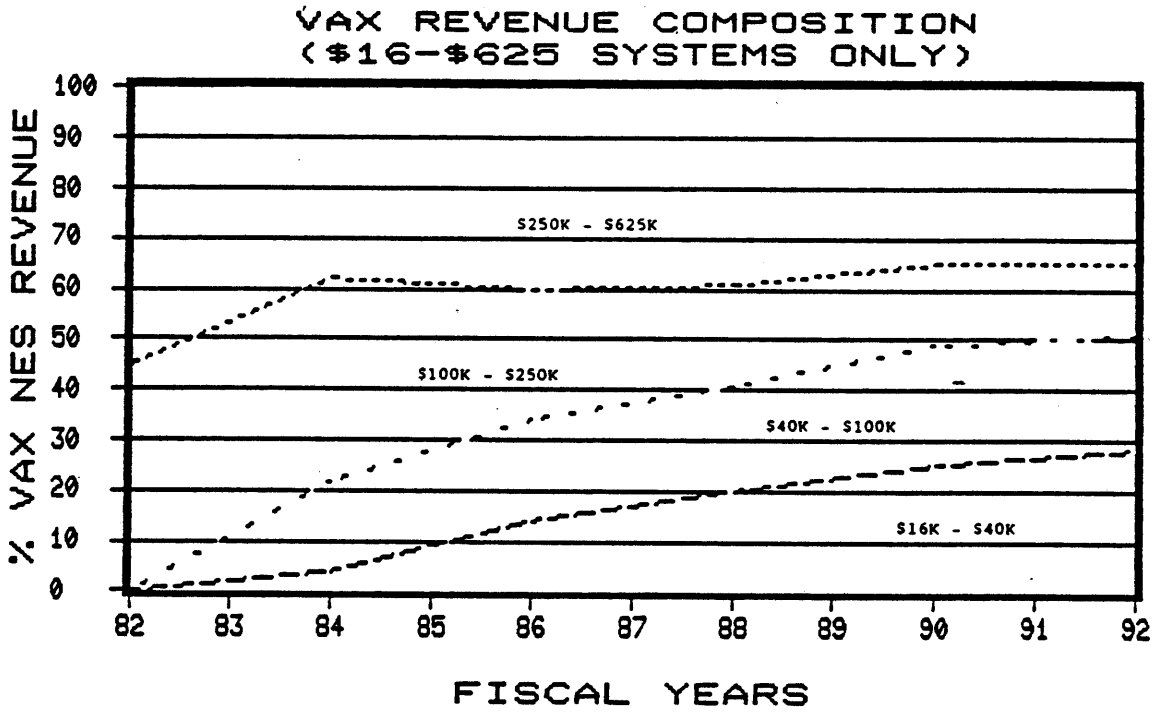


Figure 5-9

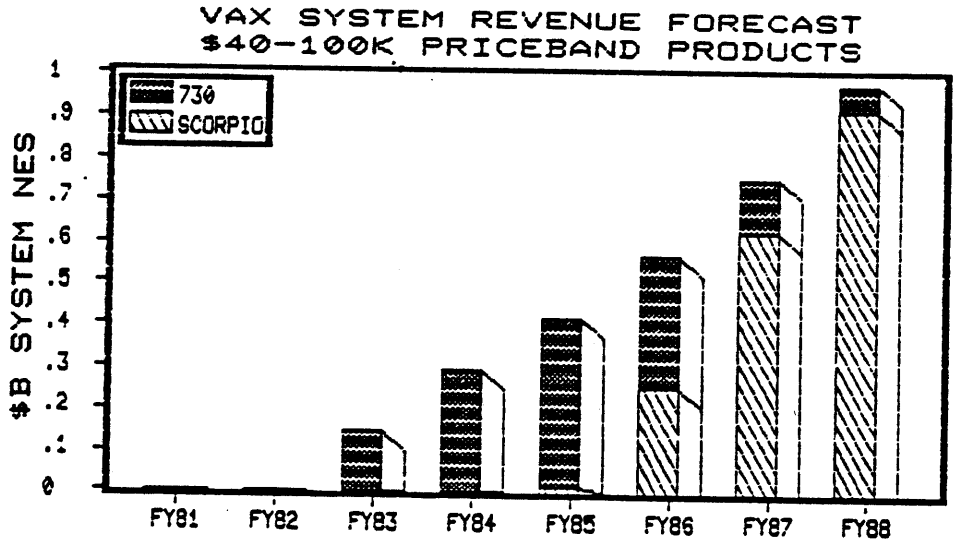


Figure 5-12

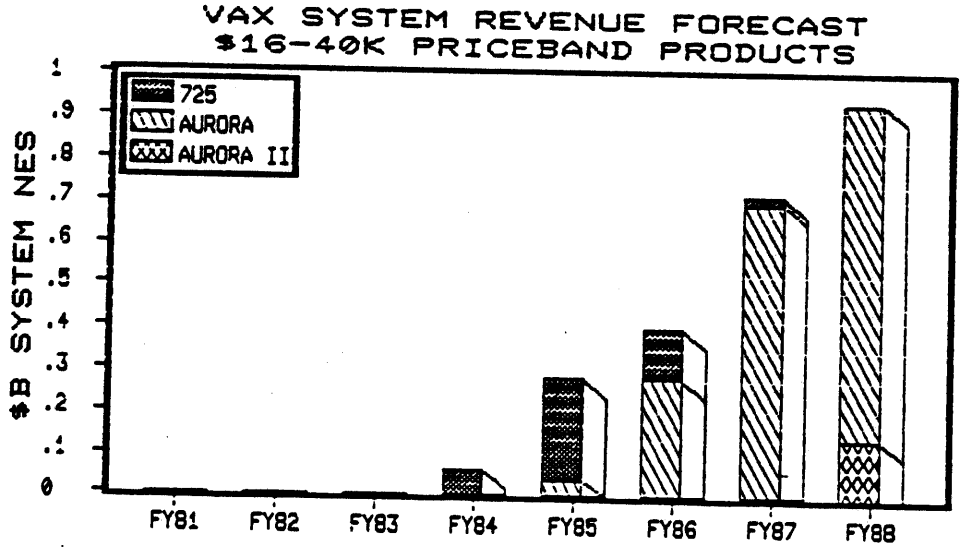


Figure 5-13

Assumptions

- Overall
  - Units include both systems and boxes
  - $ are $M NES which included discounts, allowances, and all add-on business on CPU invoice. This excludes service and all loose (separately invoiced) add-on business.
  - $ are stated in year of expenditure ($ in 85 are FY'85 dollars)
  - Market continues steady recovery from 82 downturn. No significant future downturns are forecast.
  - Revenue forecasts assume potential changes in ordering techniques (separate invoicing of disks for VAXcluster orders do not affect how we measure system revenue).

- System-Specific

SYSTEM	$ NES/UNIT RANGE	PRICE CHANGES	REPLACED BY	OTHER
780	294-269	NIL	SUPERSTAR	
782 Upgrade	180	Reduction (83/84)	SUPERSTAR	
SUPERSTAR	275	NIL	VENUS, NAUT	780 Pricing
750	100	<-5%	SCORPIO, NAUT	
730	55-45	-20% (83)	SCORPIO	
LCN	30	<-5% (85)	BI-uVAX	Q1 Aztec
VENUS	378-540	NIL	NAUT, SUPERVAX	Increasingly large config
NAUTILUS	245-260	NIL	SUPERVAX, NAUT II	
SCORPIO	45-54	<-5% (87)	SCORPIO II, BI-uVAX II	
BI-uVAX	25	<-10% (87)	SCORPIO II, BI-uVAX II	

These products will be aggressively priced, and will provi our salesforce with competitive products to sell again firms such as Apollo, HP and Three Rivers. This product wi move VAX/VMS into an important new market segment - t Single-User Dedicated Application Market.

Integrated High-Performance Workstations

We will upgrade the Integrated Medium-Performance Workstati to 780 level performance using the MicroVAX leaving pri about the same. This product will counter the expected pri cutting by our competition in the 730-750 power workstat: market by providing 780 levels of performance.

OEM Workstations

These products are intended to help VAX Workstati proliferate throughout the market with additional "Val Added" functionality. The VS100 and VS300 will be offered traditional rack-mount packages at very aggressive prices.

PRODUCT POSITIONING

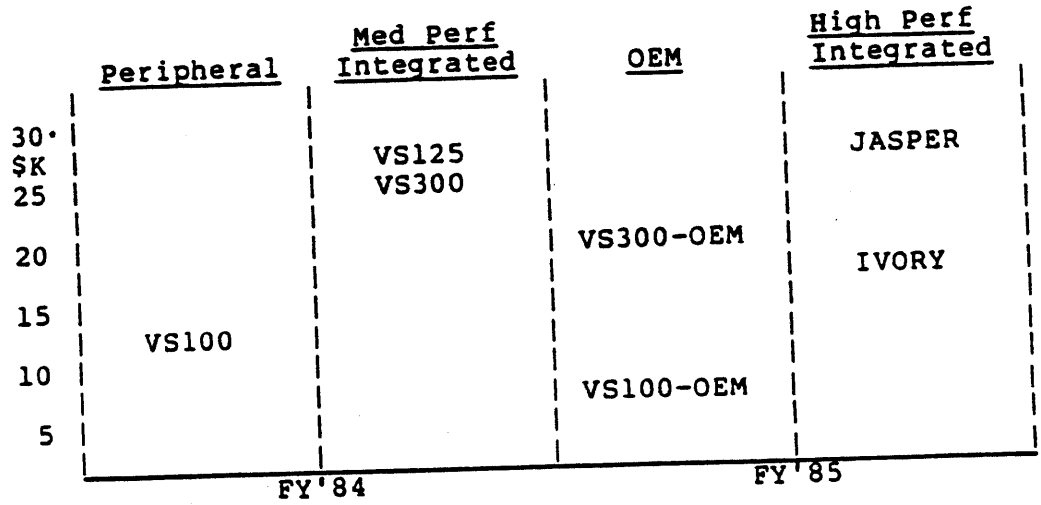


Figure 5-6

Product Descriptions

See Appendix F: VAXstation Product Summaries.

SOFTWARE SYSTEMS GROUP

LRP SOFTWARE CHART -- 32-BIT LANGUAGES AND TOOLS

FY'84		FY'85		FY'86	
DEC	BEST COMPETITOR	DEC	BEST COMPETITOR	DEC	BEST COMPETITOR
VAX LANGUAGES -languages-specific features -performance	IBM (4300)	VAX LANGUAGES -VIA integration -Tools integration	IBM (S38), UNIX	VAX LANGUAGES -New FIPs validation (as appropriate)	UNIX, Japan, Inc.
VAX TOOLS -code and module management	UNIX (PWB)	VAX TOOLS -smart editors -program generators	IBM (S38), UNIX	VAX TOOLS -high level program support environment	UNIX, Japan, Inc.
VAX TERMINAL/GRAPHICS -VAXstation VI Software -Intern'l Std. Graphics	Apollo	VAX TERMINAL/GRAPHICS -Graphics Human Interface	IBM	VAX TERMINAL/GRAPHICS -Generic Graphics Applications	IBM

OPERATING SYSTEMS

VMS -HSC/CI support -Lock Manager -Ethernet	IBM (S38)	VMS, MicroVMS -CI Clusters -High availability -Data Integrity -Security features	IBM (S38)	VMS, MicroVMS -PC-VAX -NI Personal VAX clusters	IBM, Japan, Inc.
SEABOARD -O/S to run on Seahorse	UNIX	SEABOARD -O/S to run on Seahorse	UNIX	SEABOARD -O/S to run on Seahorse	UNIX

APPENDIX C

MARKET SIZING OVERVIEW

Goals

- Establish a single shipment forecast and revenue plan for all MicroVAX products
- Measure results against this plan over time

Philosophy

- The market for 32-bit Supermicro-computers will develop independently of Digital's participation
- Digital's participation is a response to a market opportunity; Digital can only influence the distribution of market share

Methodology

- Identify an industry accepted market definition, "Computer products priced between $1-40K
- Develop a model to forecast the most likely total available market size
- Segment the available market by price band, application, product type, distribution channel and word length
- Estimate Digital market share, shipment forecast and revenue plan

MARKET SIZING CONCLUSIONS

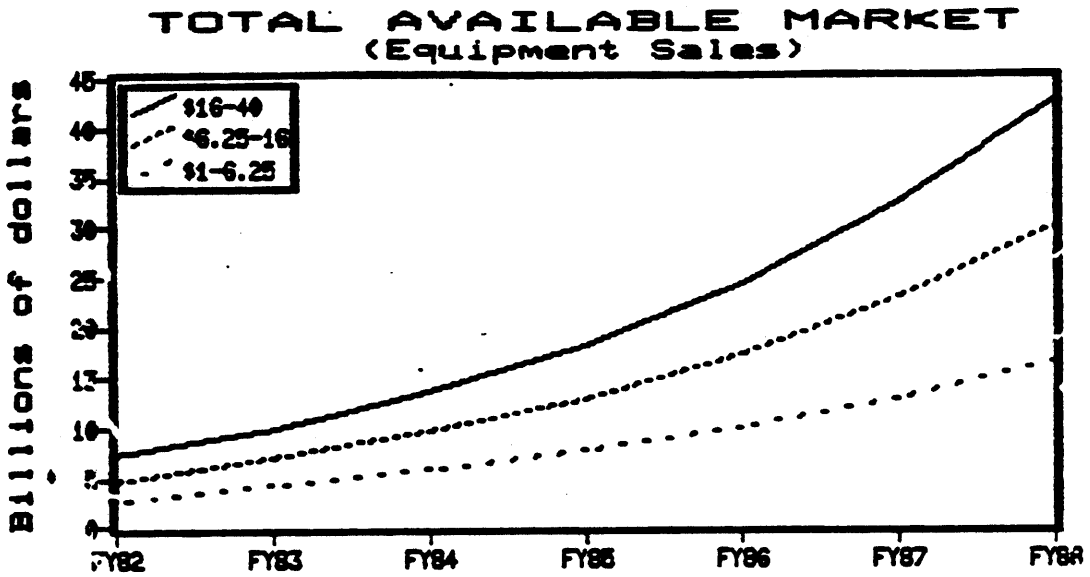
General

- The available market for computer equipment priced between $1K and $40K will triple in size by FY88
- The low end market will increase from 1/4 to about 1/2 of the total computer market by FY88
- Office and Technical applications account for more than 80% of the $1-40K market
- The 32-bit segment will grow from 10% to about 50% of the low end segment by FY88; the 16-bit segment will continue to grow through FY88
- The highest 32-bit penetration will occur in the $6.25-40K price band and in the direct and OEM channels
- Desktop products account for over 60% of the low end market opportunity

Specific

- The target market for MicroVAX products is defined as those customers desiring 32-bit desktop and system products, selling between $6.25 and $40K, with office and technical applications and distributed through the direct and OEM channels. This target market represents 15-20% of the total available low end market.

MicroVAX Program Office



Revenue ($B)

Price Band	FY84	FY85	FY86	FY87	FY88
$1-6.25	$ 6.0	$ 7.8	$10.1	$13.0	$16.8
6.25-16	3.8	5.3	7.4	10.1	13.5
16-40	4.0	5.3	6.9	9.5	12.8
	$13.8	$18.4	$24.4	$32.6	$43.1

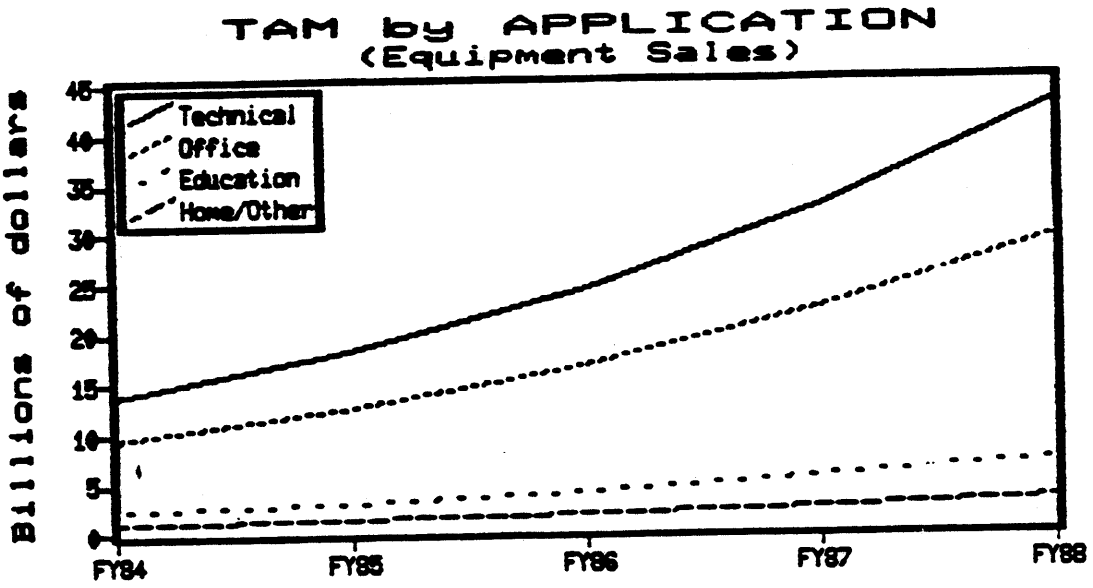
Units (K)

$1-6.25	2274	3034	4033	5235	6676
6.25-16	400	530	740	1000	1350
16-40	156	212	268	380	518
	2830	3776	5041	6615	8544

Comments

- The available market for computer equipment priced between $1K and $40K will triple in size by FY88.
- Distribution of revenue by price band is roughly uniform. Distribution of unit shipments by price band is heavily weighted towards the lowest price band.
- Revenue and unit growth is greatest in the $6.25-16K price band.

MicroVAX Program Office



Revenue ($B)

Application	FY84	FY85	FY86	FY87	FY88
Technical	$ 4.2	$ 5.7	$ 7.5	$10.2	$13.6
Office	7.2	9.5	12.6	16.9	22.3
Education	1.3	1.7	2.3	3.0	3.9
Home/Other	1.1	1.5	2.0	2.5	3.3
	$13.8	$18.4	$24.4	$32.6	$43.1

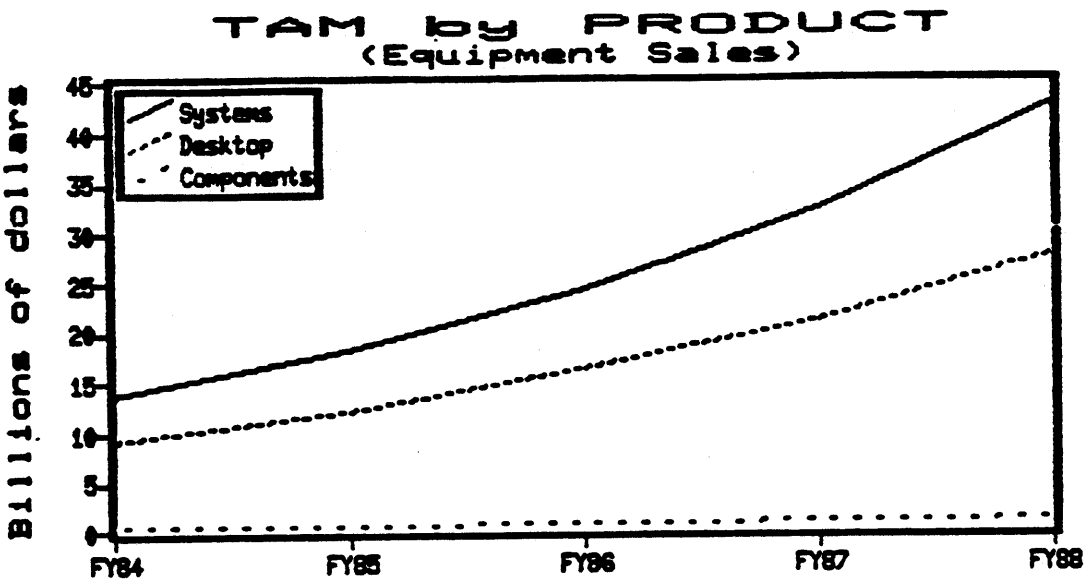
Units (K)

Technical	603	795	1068	1414	1840
Office	1534	2025	2704	3548	4581
Education	355	474	629	821	1056
Home/Other	338	482	640	832	1067
	2830	3776	5041	6615	8544

Comments

- Office and Technical applications account for more than 80% of the $1-40K market.
- All application segments are growing at approximately the same rate.

MicroVAX Program Office



Revenue ($B)

Product	FY84	FY85	FY86	FY87	FY88
Systems	$ 4.5	$ 6.1	$ 7.8	$11.1	$15.1
Desktop	8.7	11.6	15.7	20.4	26.6
Components	.6	.7	.9	1.1	1.4
	$13.8	$18.4	$24.4	$32.6	$43.1

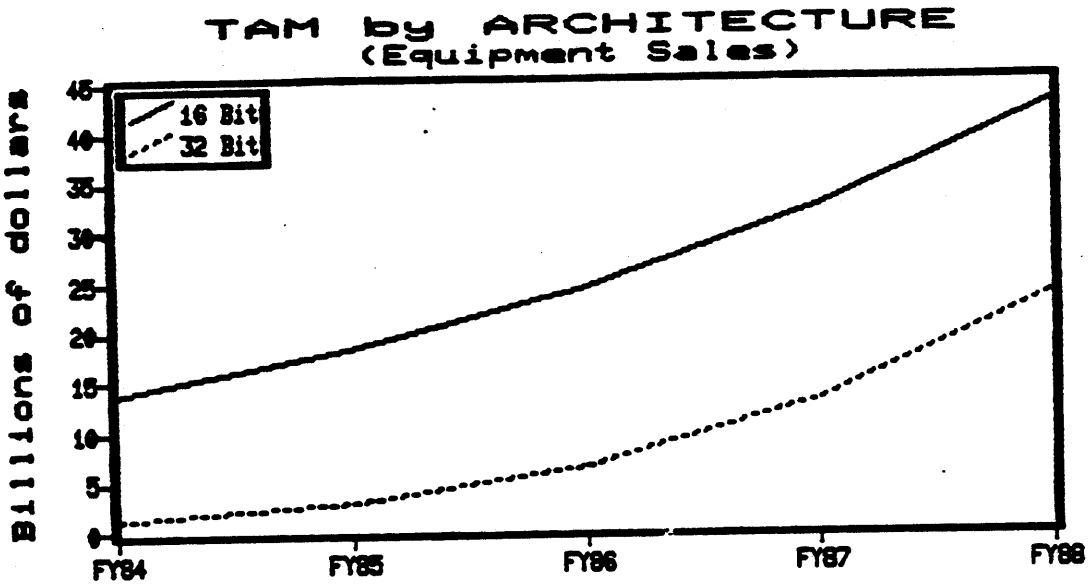
Units (K)

Systems	270	364	474	676	910
Desktop	2406	3218	4294	5584	7152
Components	154	194	273	355	482
	2830	3776	5041	6615	8544

Comments

- Desktop products account for over 60% of the low end market opportunity.
- System and Desktop products grow at approximately the same rate (no clear "winner").
- Components remain relatively insignificant.

MicroVAX Program Office



Revenue ($B)

Architecture	FY84	FY85	FY86	FY87	FY88
16-Bit	$12.4	$15.4	$17.8	$19.4	$21.1
32-Bit	1.4	3.0	6.6	13.2	22.0
	$13.8	$18.4	$24.4	$32.6	$43.1

Units (K)

16-Bit	2741	3552	4440	5174	5703
32-Bit	89	224	601	1441	2841
	2830	3776	5041	6615	8544

Comments

- The low end 32-bit market will show explosive growth through FY88. However, the 16-bit market will also continue to grow through FY88.
- The highest 32-bit market penetration will occur in the $6.25-40K price bands and in the direct and OEM channel.

APPENDIX D

MicroVAX Program Office

PRODUCT FORECASTING METHODOLOGY

DECISION TREE MODEL
- SUMMARY -

- Size and segment the market by number of users/ interfaces, (human and machine)

- Select a range of alternative scenarios for market evolution. Assign a probability of occurrence to each possible scenario. Structure a probability tree to develop a weighted average forecast.

- Vary the assumptions to test alternative outcomes.

DECISION TREE MODEL

- o Size and Segment the market by number of users/ interfaces

Actual computer shipments by US manufacturers, and non-US manufacturers serving the US marketplace were provided by Joe Menard, VAX BPM. His database is developed using International Data Corp's, (IDC), census sheets. This information segments the computer market into pricebands from $1K to >$625K. The segmentation is based on the average system value at initial purchase; includes software and peripherals sold with the CPU.

The unit shipments for FY81-FY83 were converted to the number of users or interfaces, based on an average number of users per priceband.

PRICEBAND	AVERAGE NUMBER OF USERS
$1-6.25K	1
6.25-16	2
16-40	4
40-100	8
100-250	16
250-625	32
>625	96

The estimated number of computer users is the basis for the market projections. The rationale for this approach was to analyze the available market as objectively as possible. The number of users/interfaces is a finite number in any given year. The computer solution to these users is varied, but the number of users remains constant.

Ex. 100 users/interfaces could be satisfied with one VAX 11/780 solution or 100 PRO-350's.

- o Structure Probability (Decision) Tree

Using the calculated number of users for FY83 as the starting point, a decision tree approach was utilized to model a weighted average five year forecast for the computer market. The forecast is segmented by priceband, total units and dollars, 32-bit units and dollars, and non-32 bit units and dollars. This analytical tool allows the decision maker to develop alternative outcomes for each decision. Each scenario is weighted by a probability of occurrence, the sum equalling 100%. This technique was used to reflect the wide variety of computer solutions a user can select for its needs.

The model specifically analyzes three alternative solution paths for the user/interface.

Moderate Product Mix Path

Relatively even mix of high end (>$40K) solutions and low end (<$40K)

Ex. 50% of 100 users select one VAX 11/780
25% select 25 PRO-350's
25% select 6 MPDP-11's (avg. #users/system = 4)

Total users = 100
High end units = 1
Low end units = 31

Total units = 32

Low End Multi-user path

Majority of users are satisfied with the cost/performance characteristics of the low end; and desire multi-user solutions.

Ex. 70% of 100 users select a low end product
65% of these are multi-user (MPDP-11)
35% are single users (PRO-350)
the remaining 30% demand a high end product (VAX 11/750)

Total users = 100
High end units = 1
Low end units = 35

Total units = 36

Low End Single-user path

Majority of users select a low end product; and desire more single user solutions.

Ex. 70% of 100 users select a low end product
65% of these are single-user
35% are multi-user
the remaining 30% demand a high end product

Total users = 100
High end units = 1
Low end units = 52

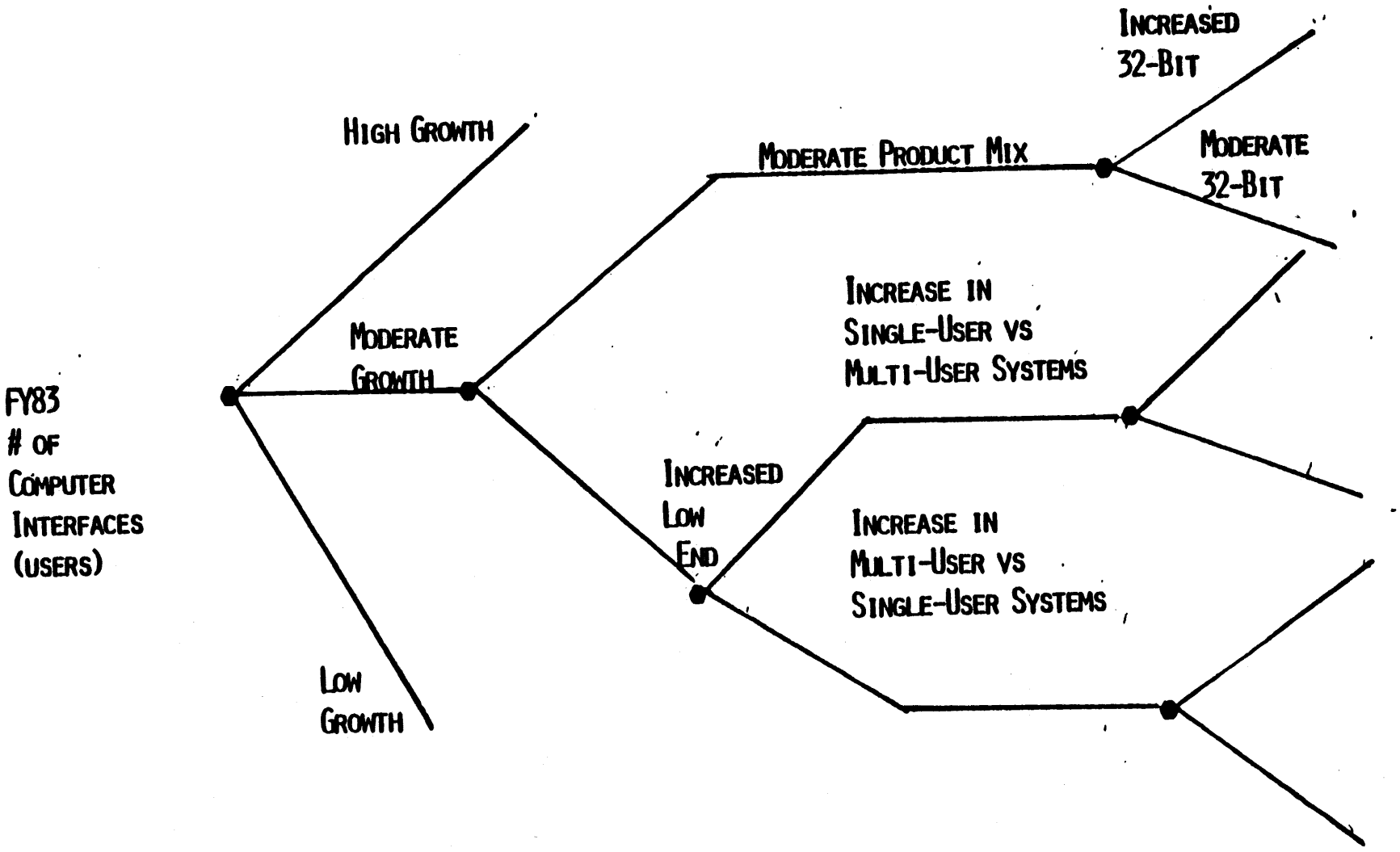
Total units = 53

Once the product mix is determined, the decision concerning 16 vs. 32 bit is modeled. The basis for the split between architecture is an understanding of the mix today and estimates of 32-bit future penetration. Penetration estimates were formulated from inputs from VAX BPM and Product Management. The MicroVAX Program Office has contracted with IDC to specifically analyze the 32-bit low end market. The published data will be incorporated into the model's assumptions.

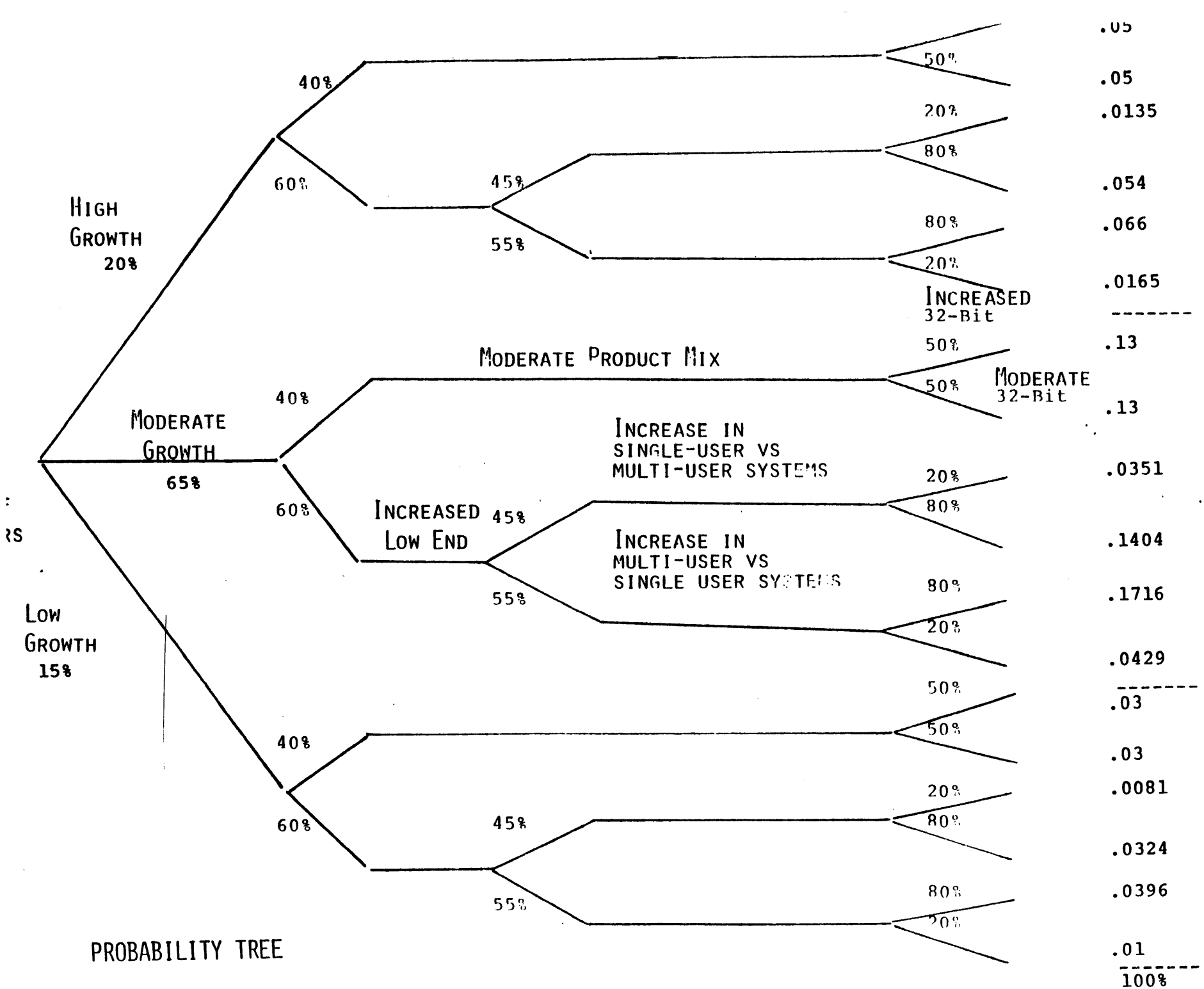
The following chart details the final assumptions used to forecast the low end market. The % fiqures refer to the % of users. For simplicity, only three years are illustrated. The decision model is also shown with the assigned probabilities of each solution path

MICROVAX PROGRAM OFFICE
MARKET SIZING MODEL

PROBABILITY TREE



● DECISION POINTS



PROBABILITY TREE

DECISION POINTS

Decision point	Decision	Assumptions			
1	growth forecast for the number of users	High path :	35% growth		
		Moderate :	22%		
		Low :	15%		
			FY83	FY85	FY87
2	product mix (% of users demanding low end solutions)	Moderate Path:	55%	62%	70%
		Increased Low:	55%	64%	72%
3	single-user vs multi-user low end solution (% of users)	Single-user path:	FY83	FY85	FY87
		1-6.25K :	62%	66%	67%
		6.25-16 :	19	19	20
		16-40 :	18	15	13
		Multi-user path:			
		1.-6.25 :	62%	52%	44%
		6.25-16 :	20	24	29
		16-40 :	18	21	26
4	32-bit penetration (penetration %)	Moderate Penetration :	FY83	FY85	FY87
		1-6.25 :	-	4%	26%
		6.25-16 :	-	15	45
		16-40 :	10	31	55
		Increased Penetration :			
		1-6.25 :	-	5%	26%
		6.25-16 :	-	20	45
		16-40 :	10	35	55

This methodology results in a forecast of the total available market by priceband. (Appendix 1). The forecast was compared to market research conducted by external firms. Infocorp's forecast of the low end market was used for comparison as they follow a similar priceband segmentation as the model.

TOTAL AVAILABLE MARKET BY PRICEBAND

- UNITS -

		CY84	CY85	CY86	CY87
$1-6.25K	Infocorp	3555	4567	5212	5760
	Model	2750	3700	4960	6575
	%	23%	19%	5%	14%
$6.25-16	Infocorp	540	635	720	775
	Model	465	660	921	1260
	%	14%	4%	28%	62%
$16-40	Infocorp	210	240	330	350
	Model	190	255	345	475
	%	10%	6%	5%	36%

The comparison shows the model to be fairly consistent, within 20% of external forecasts, at least for the first 3 years.

MARKET SEGMENTATION

The total available market was further segmented by product type, application, architecture and channel. The segmentation analysis creates a multi-dimensional view of the low end computer market. Each dimension can be compared with external market data for reasonableness in addition to providing a method to understand the growth potential of each segment.

Using market information from Dataquest, Infocorp, Digital BPM plans, and VAX BPM, the market was segmented by priceband and application.

TAM BY APPLICATION AND BY PRICEBAND
- Inputs -

$1-6.25	Technical	17%
	Office	54
	Education	14
	Home/Other	15
		100%
$6.25-16	Technical	34%
	Office	55
	Education	7
	Home/Other	4
		100%
$16-40	Technical	48%
	Office	45
	Education	5
	Home/Other	2
		100%

Technical : Industrial, scientific, manufacturing, laboratory applications

Office : Small business, F1350, word processing applications

Education : School systems, Universities, student use

Home/Other: Home use, Small EDP applications

The application by priceband segmentation was further segmented by product type. This information was compared to both internal and external market research.

TOTAL AVAILABLE MARKET BY PRODUCT

- UNITS -

		FY84	FY85	FY86	FY87
Systems	IDC	208	318	412	563
	Model	270	364	374	676
	%	29%	14%	15%	20%
Desktop	IDC	2975	4106	5341	6812
	Model	2406	3218	4294	5584
	%	19%	22%	20%	18%
Components	OEM Group	136	182	246	340
	Model	154	194	273	355
	%	13%	7%	11%	7%

Systems : Multi-user computers

Desktop : Single-user personal computers and workstations

Components : Board and box products

Segmentation by architecture is forecasted by the decision tree model based on assumed penetration rates for 32-bit products in the low end.

Segmentation by channel refers to the distribution methods, by application, for the low end computer marketplace. Infocorp and Digital BPM plans were used to develop distribution parameters for each application.

Technical	Direct	50%
	OEM	15%
	Reseller	35%
Office	Direct	50%
	OEM	5%
	Reseller	45%
Education	Direct	60%
	OEM	-
	Reseller	40%
Home/Other	Direct	-
	OEM	-
	Reseller	100%
Total Market	Direct	47%
	OEM	7%
	Reseller	46%

Direct : Customer purchases computer product directly from vendor's salesforece

OEM : Customer purchases computer product from an OEM that has added value in terms of peripherals or software

Reseller : Customer purchases computer product from vendor store or retailer store

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APPENDIX E

******

BACKPLANE INTERCONNECT (BI) BUS

****

BI MECHANICAL REQUIREMENTS

* CROSS-PRODUCT COMPATIBILITY ("UNIBUS OF THE FUTURE")

* 6 SLOTS PER CARD CAGE

* NO CABLES OFF MODULES - I/O ON BACKPLANE SIDE

* 7 VOLTAGE CHANNELS

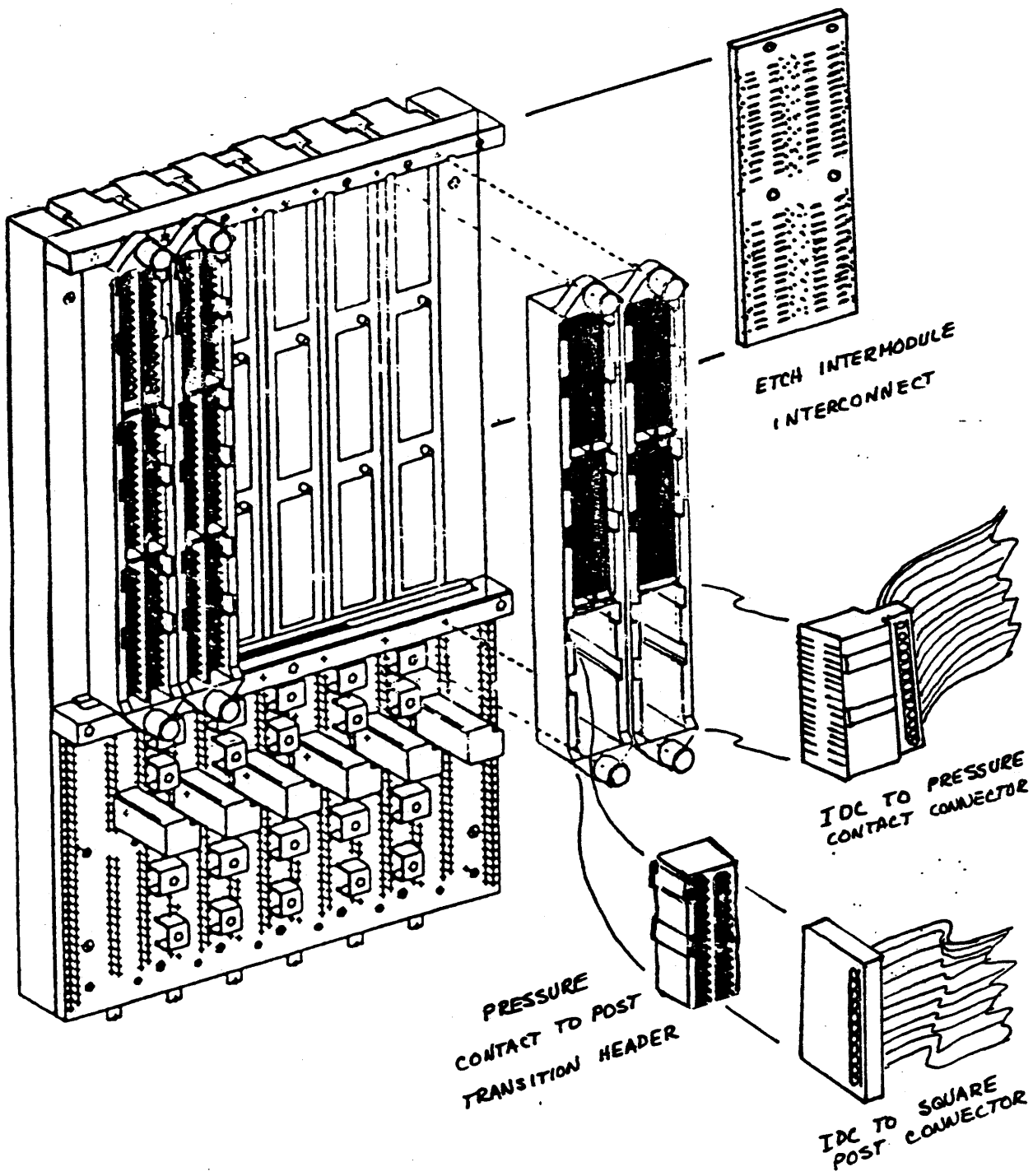
* NO CONFIGURATION CONSTRAINTS - ANY BI MODULE IN ANY SLOT

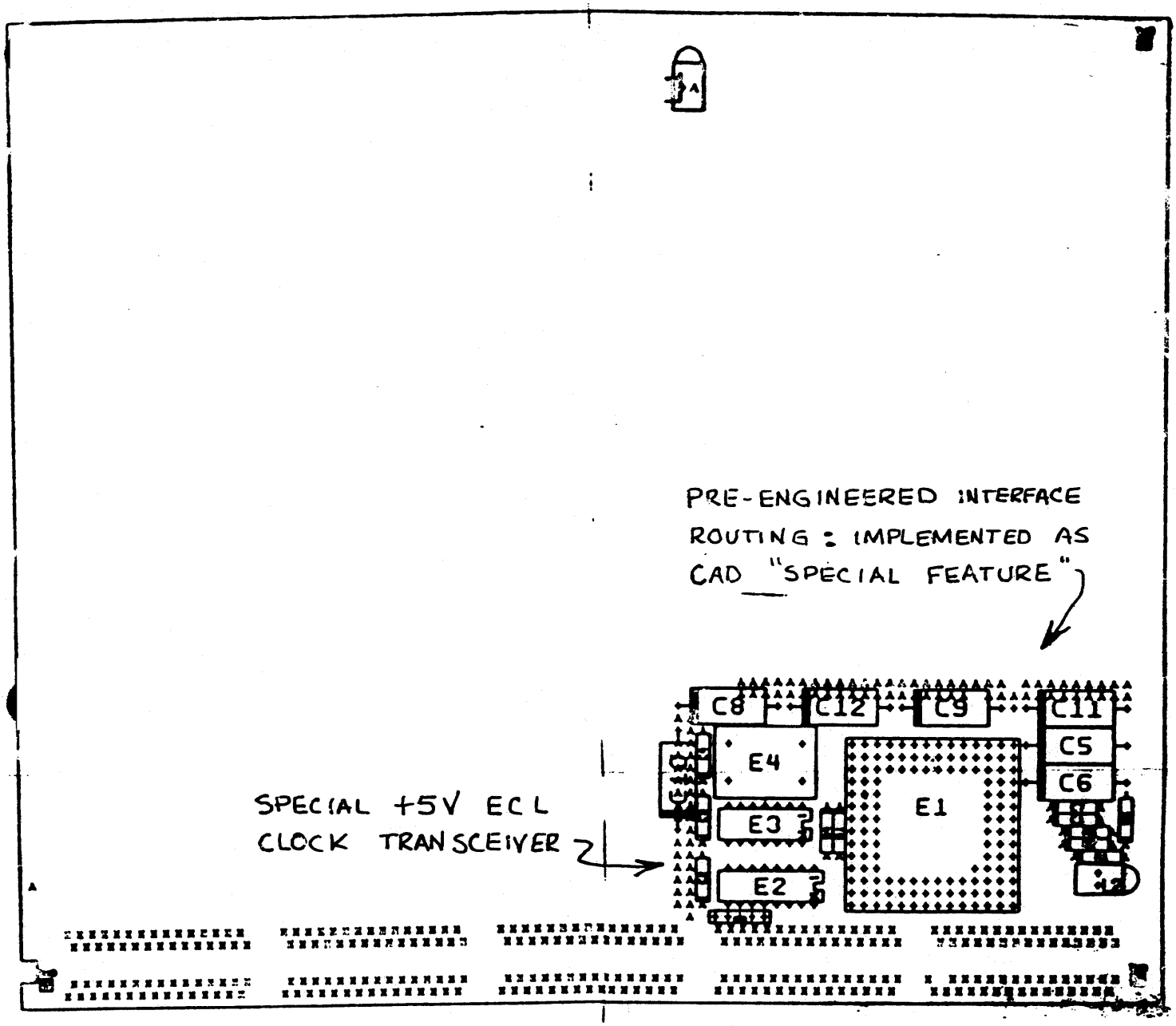
* 50 WATTS DISSIPATION PER MODULE

* PRE-ENGINEERED MODULE TO BUS INTERFACE CIRCUITRY

* USER FRIENDLY: CUSTOMER INSTALLABLE/MAINTAINABLE

BI BACKPLANE ASSEMBLY AND I/O COMPONENTS





PRE-ENGINEERED BI INTERFACE CHIP SET

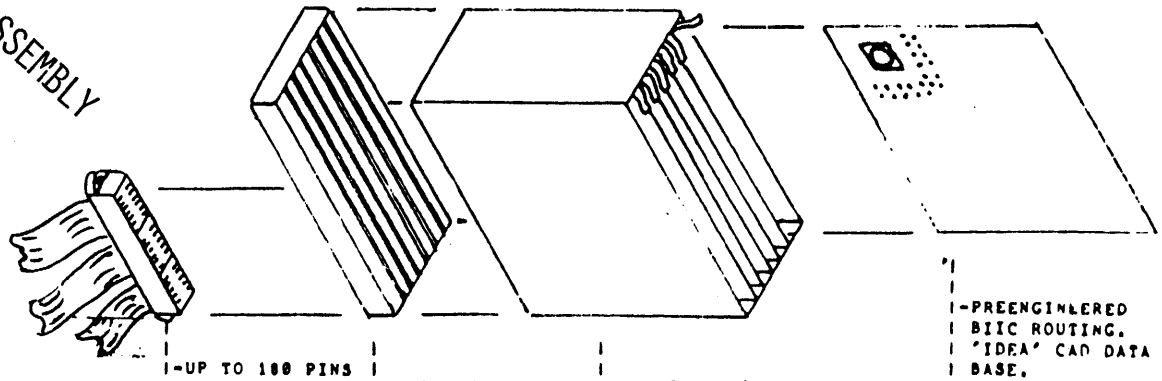
BI CARDCAGE BUILDING BLOCKS

BI BACKPLANE ASSEMBLY

BI CARDCAGE

BI MODULE

I/O CONNECTOR ASSEMBLY

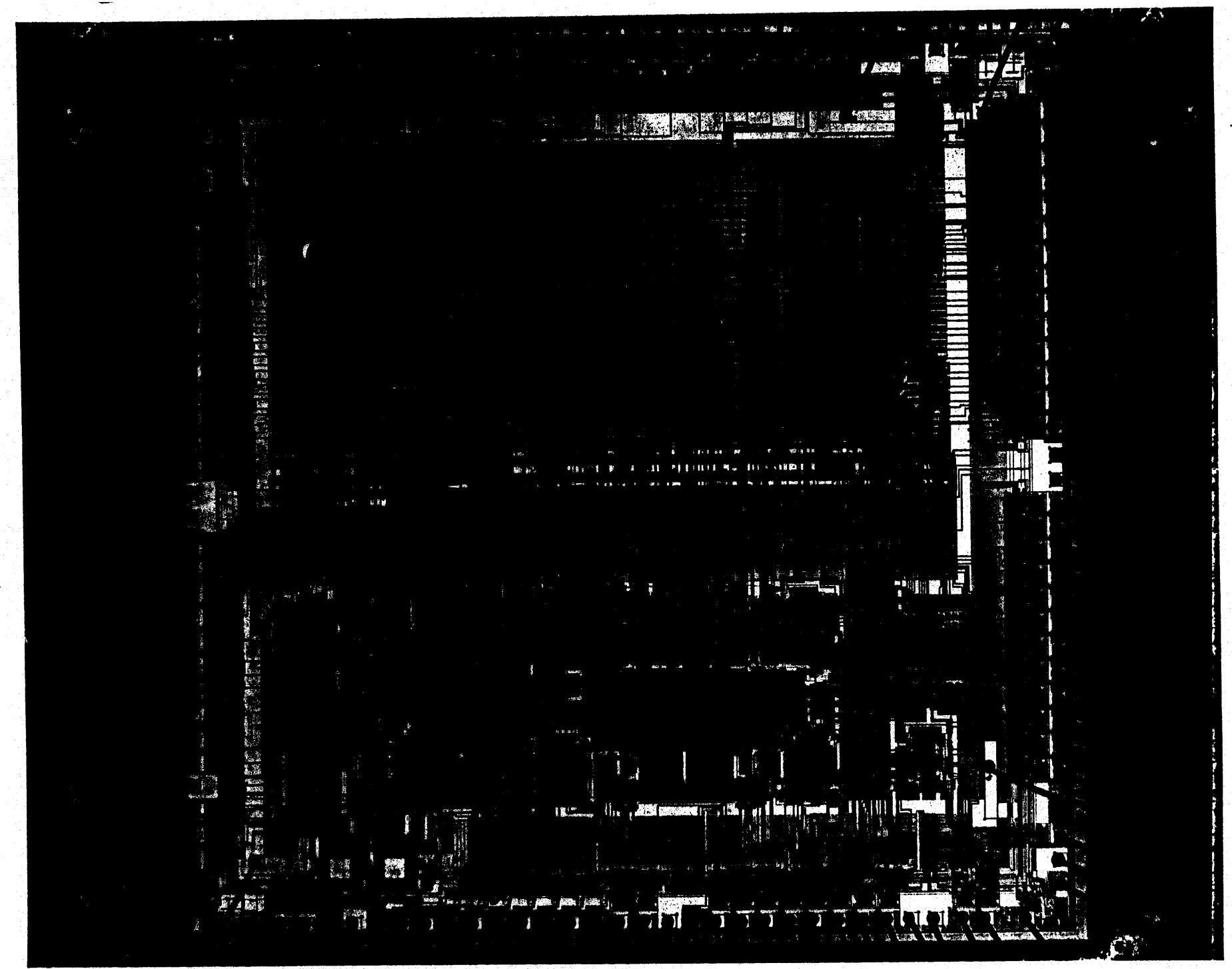


- UP TO 180 PINS
- .025 SQ. GOLD PLATED POST FOR IDC CONNECTORS
- 6 FIELDS OF 30 PINS EACH
- PRECONFIGURED OPTION CABLE SET.
- ATTACHES TO B/P SUBASS'Y WITH 2 SCREWS.
- KEYED FOR POLARITY
- SELF-ALIGNING PRESSURE CONTACT TO 60 POST PIN TRANSITION HEADER
- FUTURE
  - *IDC TO PRESSURE CONTACT HEADER
  - *INTERMODULE ETCH BOARD

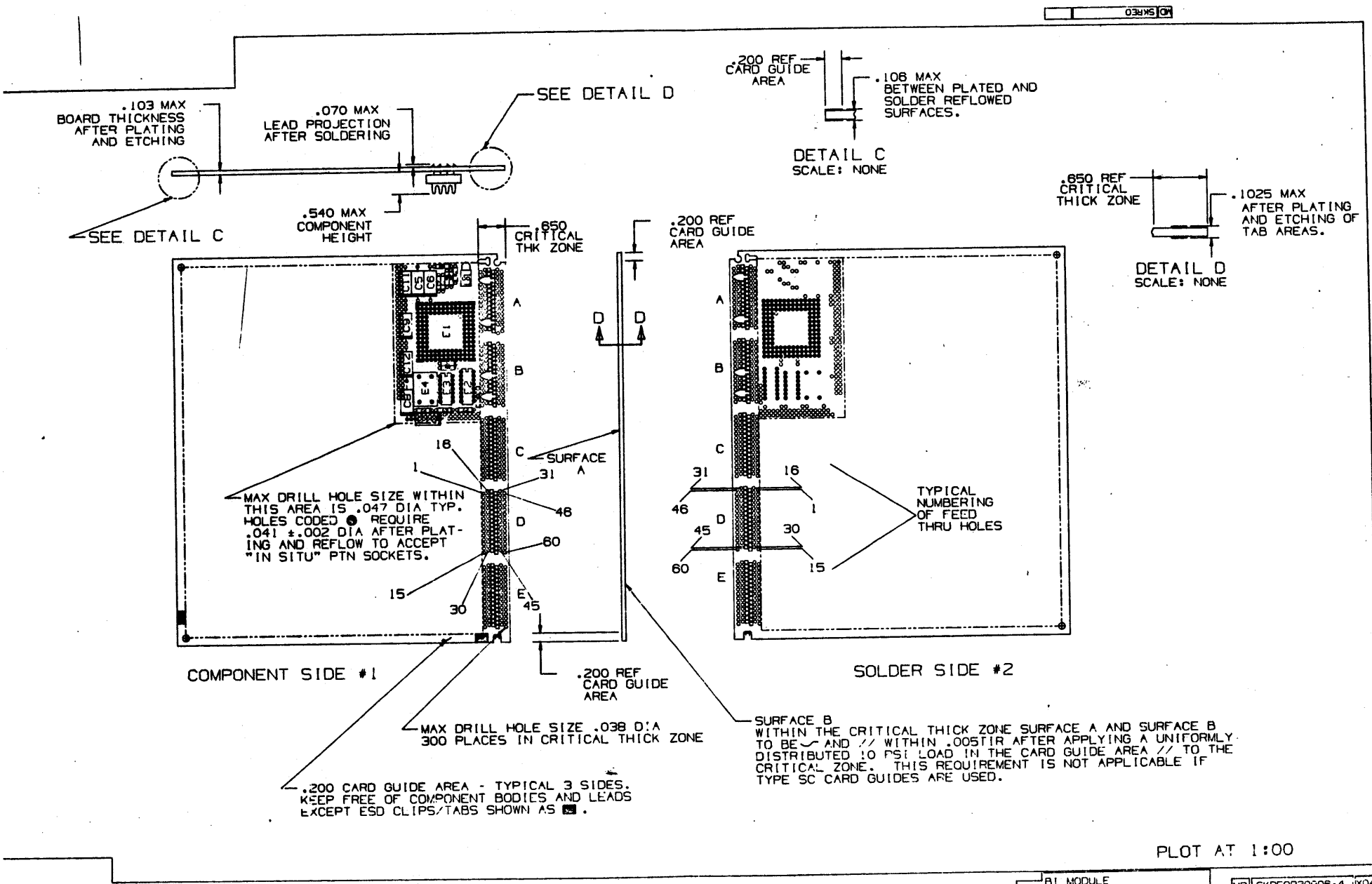
- ETCH B/P
- 6 SLOTS
- 180 CONTACTS I/O PER SLOT; USER CONFIGURED
- 7 VOLTAGE CHANNELS
- SUBASSEMBLY ATTACHES TO CAGE W/4 SCREWS
- TOP OR SIDE ENTRY

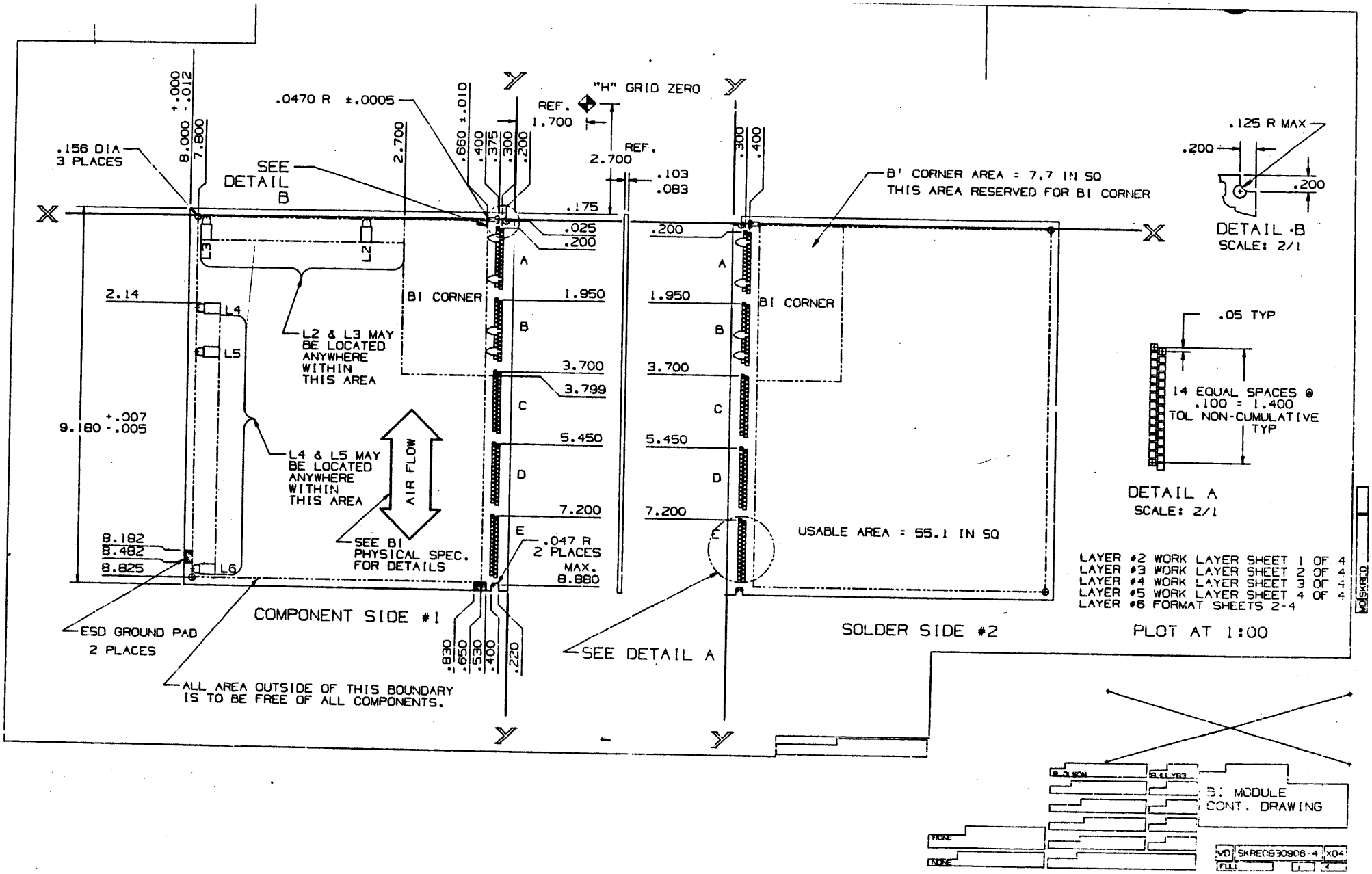
- 6 SLOT CARD GUIDE
- PREENGINEERED AIRFLOW MGMT.
- REMOTE CONNECTOR CAM ACTUATOR
- "STANDARD" SYS. ATTACHMENT PTS. 4 PLACES EACH SIDE
- 0.8 in. MODULE CENTERS

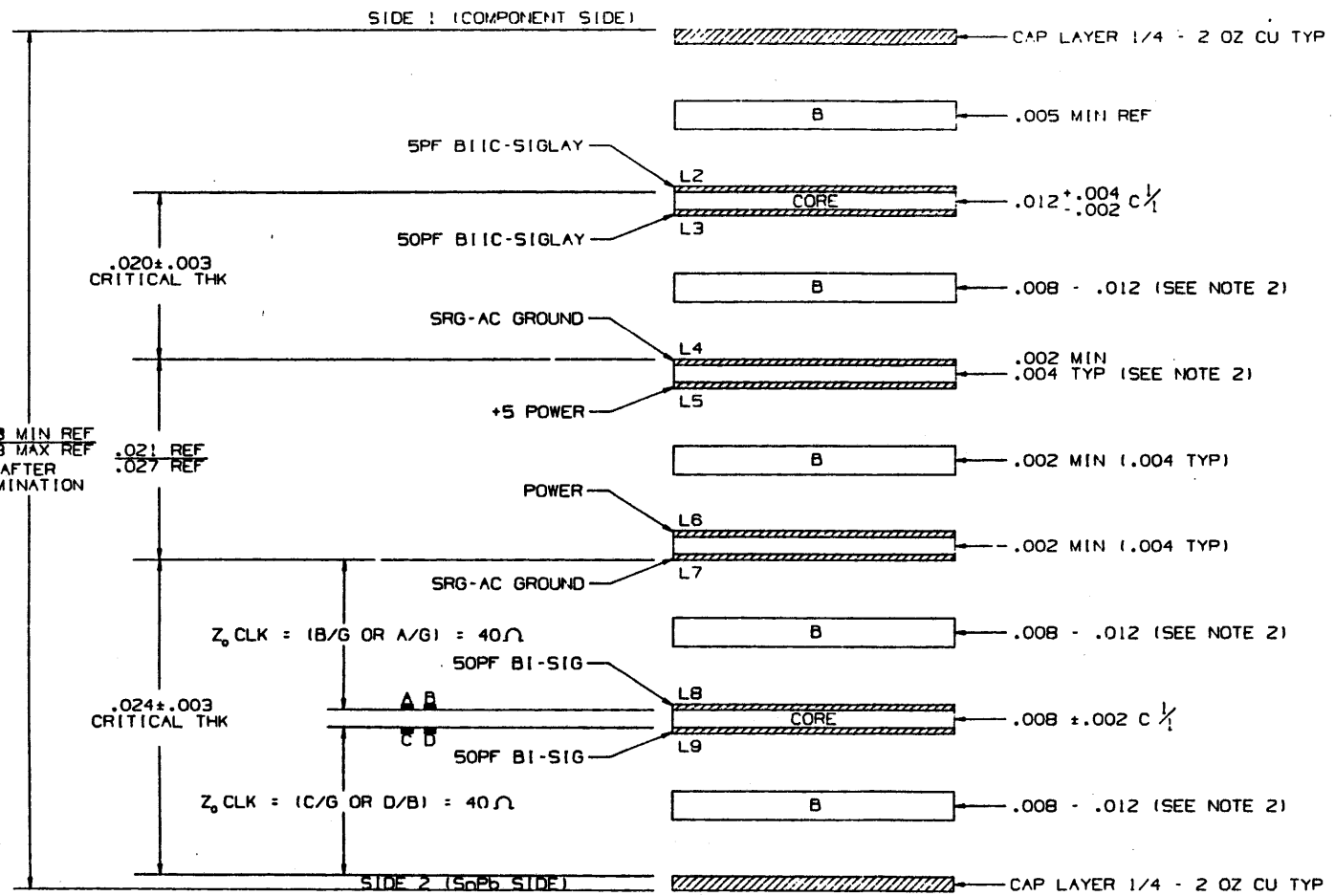
- PREENGINEERED BIIC ROUTING. 'IDEA' CAD DATA BASE.
- 8.0x9.18 MODULE SIZE
- .093 THICK
- UP TO 4 SIGNAL LAYERS
- 4 POWER AND GND LAYERS
- UP TO 50 WATTS PER MODULE
- ZMOS BIIC CHIP
- ECL CLOCK TRANSCEIVER
- SELF TEST ANNUNCIATOR LEDS



BIIC CHIP


.103 MAX
BOARD THICKNESS
AFTER PLATING
AND ETCHING
.070 MAX
LEAD PROJECTION
AFTER SOLDERING
SEE DETAIL D
SEE DETAIL C
.540 MAX
COMPONENT
HEIGHT
.650
CRITICAL
THK ZONE
.200 REF
CARD GUIDE
AREA
.106 MAX
BETWEEN PLATED AND
SOLDER REFLOWED
SURFACES.
DETAIL C
SCALE: NONE
.650 REF
CRITICAL
THICK ZONE
.1025 MAX
AFTER PLATING
AND ETCHING OF
TAB AREAS.
DETAIL D
SCALE: NONE
A
B
C
D
E
D D
SURFACE
A
MAX DRILL HOLE SIZE WITHIN
THIS AREA IS .047 DIA TYP.
HOLES CODED ● REQUIRE
.041 ±.002 DIA AFTER PLAT-
ING AND REFLOW TO ACCEPT
"IN SITU" PTN SOCKETS.
1
16
31
46
60
15
30
45
TYPICAL
NUMBERING
OF FEED
THRU HOLES
COMPONENT SIDE #1
SOLDER SIDE #2
.200 REF
CARD GUIDE
AREA
MAX DRILL HOLE SIZE .038 DIA
300 PLACES IN CRITICAL THICK ZONE
SURFACE B
WITHIN THE CRITICAL THICK ZONE SURFACE A AND SURFACE B
TO BE ⌒ AND // WITHIN .005TIR AFTER APPLYING A UNIFORMLY
DISTRIBUTED 10 PSI LOAD IN THE CARD GUIDE AREA // TO THE
CRITICAL ZONE. THIS REQUIREMENT IS NOT APPLICABLE IF
TYPE SC CARD GUIDES ARE USED.
.200 CARD GUIDE AREA - TYPICAL 3 SIDES.
KEEP FREE OF COMPONENT BODIES AND LEADS
EXCEPT ESD CLIPS/TABS SHOWN AS ■.
PLOT AT 1:00
BI MODULE
CONT. DRAWING
MD SKREO930906-4 Y04


.156 DIA
3 PLACES
SEE
DETAIL
B
.0470 R ±.0005
"H" GRID ZERO
REF.
1.700
REF.
2.700
.103
.083
.175
.025
.200
B' CORNER AREA = 7.7 IN SQ
THIS AREA RESERVED FOR B1 CORNER
B1 CORNER
L2 & L3 MAY
BE LOCATED
ANYWHERE
WITHIN
THIS AREA
L4 & L5 MAY
BE LOCATED
ANYWHERE
WITHIN
THIS AREA
AIR FLOW
SEE B1
PHYSICAL SPEC.
FOR DETAILS
.047 R
2 PLACES
MAX.
8.880
USABLE AREA = 55.1 IN SQ
COMPONENT SIDE #1
SOLDER SIDE #2
SEE DETAIL A
ESD GROUND PAD
2 PLACES
ALL AREA OUTSIDE OF THIS BOUNDARY
IS TO BE FREE OF ALL COMPONENTS.
.125 R MAX
DETAIL B
SCALE: 2/1
.05 TYP
14 EQUAL SPACES @
.100 = 1.400
TOL NON-CUMULATIVE
TYP
DETAIL A
SCALE: 2/1
LAYER #2 WORK LAYER SHEET 1 OF 4
LAYER #3 WORK LAYER SHEET 2 OF 4
LAYER #4 WORK LAYER SHEET 3 OF 4
LAYER #5 WORK LAYER SHEET 4 OF 4
LAYER #6 FORMAT SHEETS 2-4
PLOT AT 1:00
B1 MODULE
CONT. DRAWING



SECTION D-D
SCALE: NONE

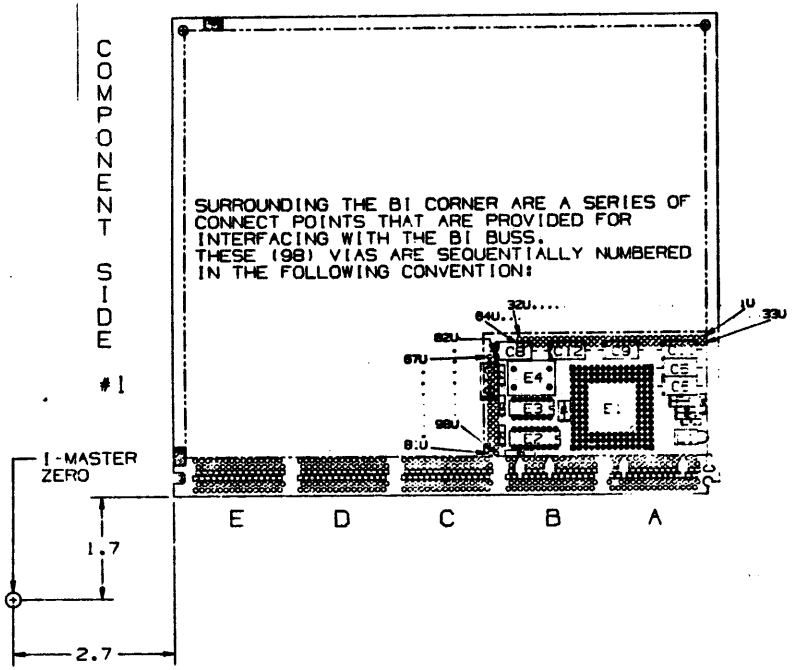
NOTES:

1. INSULATION LAYERS DESIGNATED "CORE" MUST BE COPPER CLAD AND LAMINATED BY UL APPROVED MATERIAL SUPPLIERS.
2. INSULATION LAYERS DESIGNATED "B" OR UNMARKED MAY USE CORE AND PREPREG INTERCHANGABLY.
3. MAX WARP AND TWIST AFTER STRESS RELIEF (IF ANY) TO BE .87 MILS PER LINEAR INCH.
4. TO BECOME A OS FOR THIS MSL TYPE, VENDOR MUST SUBMIT TO DIGITAL A SPECIFICALLY TOLERANCED LAYUP WHICH WILL BE MUTUALLY AGREED/ADHERED TO.
5. FINISHED BOARD THICKNESS MEASURED AFTER PLATING AND ETCHING TO BE .102 MAX WHEN MEASURED BETWEEN SIDE 1-SIDE 2 Au PLATED TABS; .093±10% EVERYWHERE ELSE.

PLOT AT 1.00

BI INTERFACE TABLE

THE FOLLOWING IS A TABLE WHICH DESIGNATES THE BI CORNER CONNECT POINTS FOR INTERFACING WITH THE BI BUSS.



THESE CONNECT POINTS MAY BE CONSIDERED AS EITHER VIAS OR CONNECT POINTS WHERE PADS COULD BE PROVIDED AT THE APPROPRIATE SIGNAL LAYER FOR DIRECT CONNECT WITHOUT A VIA PROVIDED. ALL CONNECT POINTS ARE ON A .100" GRID IN ROWS .100" APART. THE LOCATIONS ON THE MODULE OF THESE INDIVIDUAL POINTS MAY BE CALCULATED (COUNTING BY .100") USING THE X-Y GRID LOCATIONS OF 1U AND 65U REFERENCED FROM "1" MASTER ZERO ORIGIN

1U IS X=11.600, Y=4.300
65U IS X= 8.000, Y=4.000

EXAMPLE:

? GRID LOCATION OF 86U

ANS.= X= 65U (X) + .100 = 8.100"
Y= 65U (Y) - .400 = 3.600"

SIGNAL TO PIN NUMBER TABLE

MODULE CONNECT POINTS	SIGNAL NAME	ROUTED FROM	SIGNAL LAYER #
1U	+MB	CONN A-35	8
2U	PASSTHRU	CONN A-37	8
3U	PASSTHRU	CONN A-39	8
4U	PASSTHRU	CONN A-41	8
5U	BCI STPASS L	LED RES #6	9
6U	BCI SCI L	BIIC, H-2	9
7U	BCI D30 H	BIIC, J-2	2
8U	BCI D28 H	BIIC, K-2	2
9U	BCI D31 H	BIIC, K-1	3
10U	BCI D24 H	BIIC, M-2	8
11U	BCI D25 H	BIIC, N-1	3
12U	BCI D26 H	BIIC, M-1	2
13U	BCI D20 H	BIIC, P-2	3
14U	N/C (E1-N2)	BIIC, N-2	2
15U	BCI D22 H	BIIC, N-3	2
16U	BCI D18 H	BIIC, N-4	2
17U	BCI D15 H	BIIC, N-5	2
18U	BCI D12 H	BIIC, N-6	2
19U	BCI D09 H	BIIC, N-7	2
20U	BCI D06 H	BIIC, P-9	3
21U	BCI D13 H	BIIC, M-8	9
22U	BCI D05 H	BIIC, N-9	2
23U	BCI D01 H	BIIC, N-10	2
24U	N/C OPEN VIA	••••••••	•
25U	BCI D04 H	BIIC, M-9	8
26U	BCI 10 H	BIIC, M-12	8
27U	BCI CLE H	BIIC, M-13	9
28U	BCI RAK L	BIIC, L-13	9
29U	BCI I3 H	BIIC, N-11	2
30U	BCI EV0 L	BIIC, K-13	9
31U	BCI EV3 L	BIIC, K-14	9
32U	BCI AC LO L	BIIC, N-13	2
33U	PASSTHRU	CONN A-32	8
34U	+MB	CONN A-51	8
35U	PASSTHRU	CONN A-52	8
36U	PASSTHRU	CONN A-54	8
37U	BI SPARE L	CONN A-56	8
38U	BCI SC2 L	BIIC, H-1	2
39U	BCI SEL L	BIIC, H-3	9
40U	BCI SC0 L	BIIC, J-1	9
41U	BCI D29 H	BIIC, L-1	3
42U	BCI D27 H	BIIC, L-2	2
43U	BCI D23 H	BIIC, M-3	9
44U	BCI D21 H	BIIC, M-4	8
45U	BCI D17 H	BIIC, M-5	9
46U	BCI D19 H	BIIC, P-3	3
47U	BCI D16 H	BIIC, P-4	3
48U	BCI D14 H	BIIC, P-5	3
49U	BCI D11 H	BIIC, P-6	3

SIGNAL TO PIN NUMBER TABLE CONT.

MODULE CONNECT POINTS	SIGNAL NAME	ROUTED FROM	SIGNAL LAYER #
50U	BCI D10 H	BIIC, P-7	3
51U	BCI D07 H	BIIC, P-8	3
52U	BCI D08 H	BIIC, N-8	2
53U	-5.2V	••••••••	•
54U	OPEN VIA	••••••••	•
55U	BCI D03 H	BIIC, P-10	3
56U	BCI D02 H	BIIC, P-11	3
57U	N/C (E1-B13)	BIIC, B-13	9
58U	BCI EV2 L	BIIC, J-12	9
59U	BCI NXT L	BIIC, M-14	9
60U	BCI EV1 L	BIIC, L-14	9
61U	BCI D00 H	BIIC, P-12	2
62U	BCI I1 H	BIIC, N-12	2
63U	BCI I2 H	BIIC, P-13	2
64U	BCI P0 H	BIIC, N-14	3
65U	BCI DC LO L	BIIC, J-14	9
66U	GND	••••••••	•
67U	BCI INT5 L	BIIC, F-14	3
68U	BCI INT4 L	BIIC, E-14	3
69U	BCI RQI L	BIIC, D-14	3
70U	BI BAD L	CONN B-51	8
71U	BCI INT6 L	BIIC, G-12	9
72U	BCI SDE L	BIIC, H-14	9
73U	BCI INT7 L	BIIC, G-13	9
74U	N/C -2.00V	••••••••	•
75U	BCI PHASE L	CLK REC-PIN#8	3
76U	BCI TIME H	CLK REC-PIN#1	9
77U	BCI TIME L	CLK REC-PIN#15	3
78U	BCI PHASE H	CLK REC-PIN#10	3
79U	BI ID3 H	RES, SIP-PIN#2	9
80U	BI ID1 H	RES, SIP-PIN#4	9
81U	OPEN VIA	••••••••	•
82U	BCI EV4 L	BIIC, J-13	9
83U	BCI RS1 L	BIIC, E-13	3
84U	BCI MAB L	BIIC, F-13	3
85U	+12.0V	CONN B-50	8
86U	BI STF L	CONN B-36	8
87U	-12.0V	CONN B-37	8
88U	5 Mhz TTL H	CLK DRV-PIN#6	3
89U	10 Mhz TTL H	CLK DRV-PIN#5	3
90U	20 Mhz TTL H	CLK DRV-PIN#4	3
91U	BCI MDE L	BIIC, G-14	9
92U	BCI RQ0 L	BIIC, F-12	9
93U	BCI RS0 L	BIIC, C-14	9
94U	BI RESET L	CONN B-54	8
95U	N/C (E2-14)	CLK REC-PIN#14	3
96U	N/C (E2-13)	CLK REC-PIN#13	3
97U	BI ID2 H	RES, SIP-PIN#3	9
98U	BI ID0 H	RES, SIP-PIN#5	9

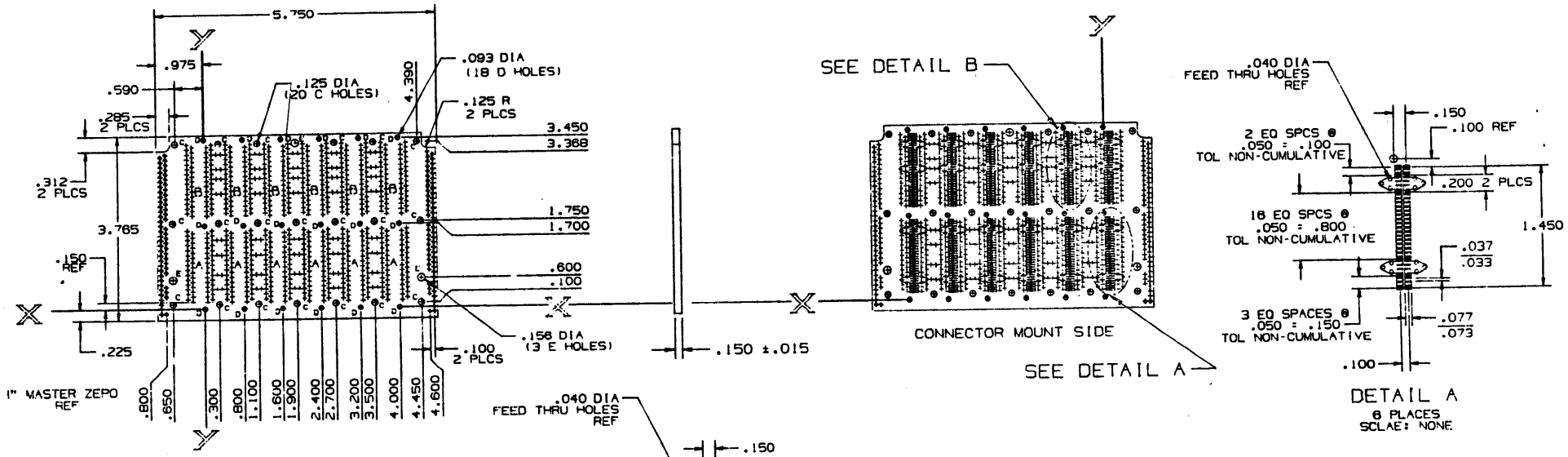
PLOT AT 1:00

JIM STAPLES
REVISION 00 01JUL83
01 12JUL83

BI MODULE CONT. DRAWING

FULL 4 4

MD SKREC0830906-4 X04


5.750
.975
.590
.285
2 PLCS
.125 DIA
(20 C HOLES)
.093 DIA
(18 D HOLES)
.125 R
2 PLCS
4.390
3.450
3.388
1.750
1.700
.600
.100
.312
2 PLCS
3.765
.150
REF
.225
.156 DIA
(3 E HOLES)
.100
2 PLCS
1" MASTER ZEPO
REF
.800
.650
.300
.800
1.100
1.600
1.900
2.400
2.700
3.200
3.500
4.000
4.450
4.600
TERMINATOR & BUS BAR SIDE
.150 ±.015
SEE DETAIL B
CONNECTOR MOUNT SIDE
SEE DETAIL A
.040 DIA
FEED THRU HOLES
REF
.150
.100 REF
2 EQ SPCS @
.050 = .100
TOL NON-CUMULATIVE
.200 2 PLCS
18 EQ SPCS @
.050 = .800
TOL NON-CUMULATIVE
1.450
.037
.033
3 EQ SPACES @
.050 = .150
TOL NON-CUMULATIVE
.077
.073
.100
DETAIL A
6 PLACES
SCLAE: NONE
.040 DIA
FEED THRU HOLES
REF
.150
.100 REF
2 EQ SPCS @
.050 = .100
TOL NON-CUMULATIVE
.200 2 PLCS
6 EQ SPCS @
.050 = .300
TOL NON-CUMULATIVE
1.450
.037
.033
13 EQ SPCS @
.050 = .650
TOL NON-CUMULATIVE
.077
.073
.100
DETAIL B
6 PLACES
SCLAE: NONE
BACKPLANE, BI
MECH. SPEC.