TECHNICAL MANUAL

AM-600/T

MAGNETIC TAPE FORMATTER INTERFACE

DWM-00607-00
REV. A00

alpha micro

FIRST EDITION

May 1984   E.N. 01700

REVISIONS INCORPORATED	
REVISION	DATE

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CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual provides operating and maintenance instructions for the AM-600/T
Magnetic Tape Transport Formatter Interface circuit board manufactured by
Alpha Microsystems located in Irvine, California.   Circuit board
description, operating and usage instructions, programming, theory of
operation, and maintenance instructions are included to provide the user
with the information necessary to use this circuit board to its full
capability.

1.2 CIRCUIT BOARD DESCRIPTION

The AM-600/T circuit board provides a general purpose, single board
interface capability between the Alpha Micro bus and the industry standard
1/2 inch magnetic tape formatter. The main features of the AM-600/T are as
follows:

*   Fully compatible with all Alpha Micro CPU boards (except AM-1000)

*   Full DMA data transfer capability

*   Interrupt capability provided

*   Interfaces up to two formatters (eight transports total)

*   Controls both seven and nine track tape transports

*   Controls transports with densities of up to 3200 bytes per inch
     and tape velocities up to 37.5 ips

*   Easy cabling interface via two 50-conductor flat ribbon cables

*   Software control over virtually all standard formatter
     modes and operation

A simplified block diagram of the AM-600/T is shown in Figure 1-1. For a
complete detailed description of circuit board operation, see Chapter 4 of
this manual.
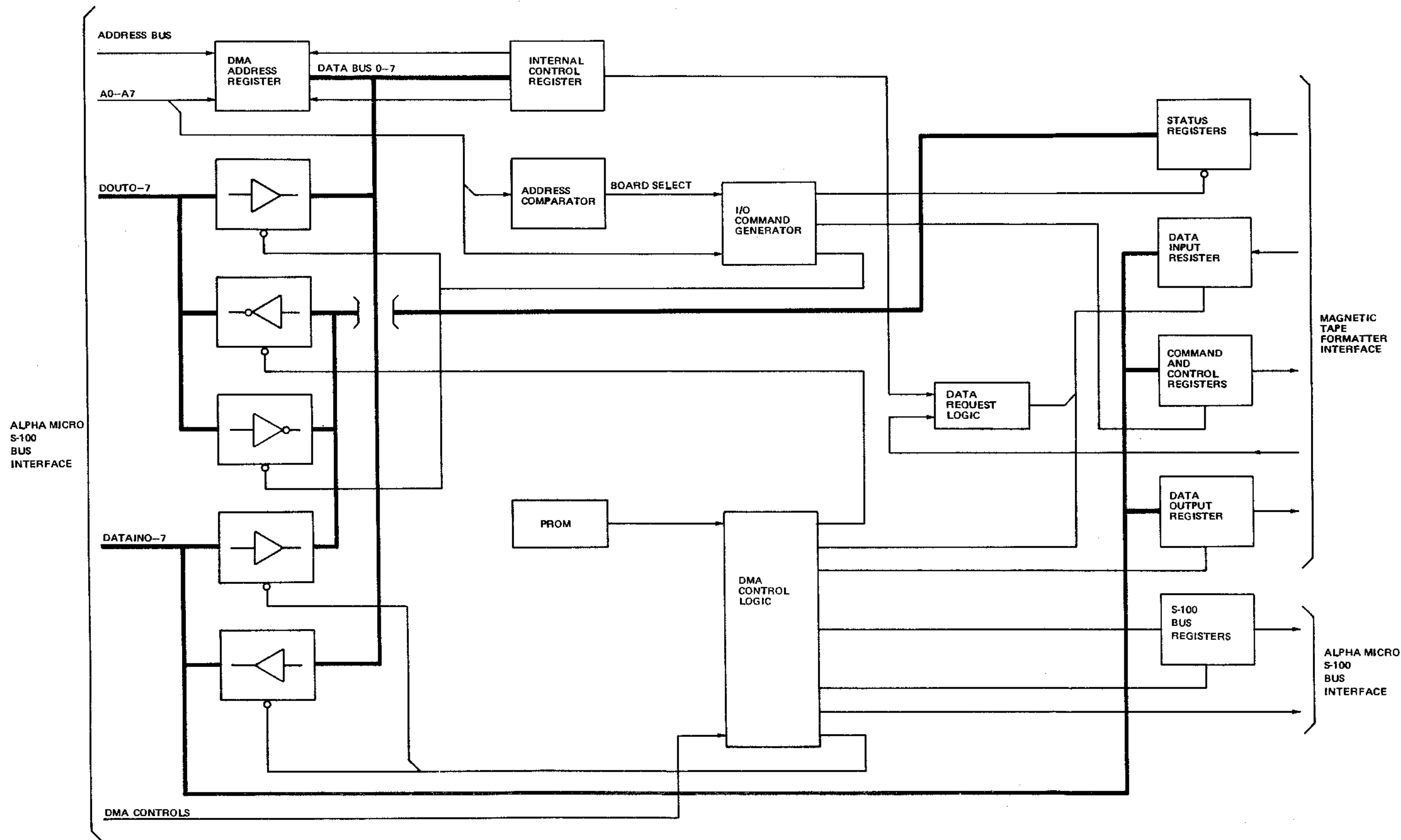
FIGURE 1-1.

AM-600/T Simplified Block Diagram

1.3 APPLICATION

The AM-600/T is fully compatible with the standard Alpha Micro bus-based systems. Jumpers on the circuit board that provide for user selection are described in Chapter 2. The AM-600/T formatter interface directly controls both seven and nine track tape transports with 1/2 inch tape.

CHAPTER 2

OPERATING DATA

2.1 INTRODUCTION

This chapter contains information on the use of the AM-600/T Magnetic Tape
Transport Formatter Interface circuit board. Capabilities, specifications,
interface wiring, and user option descriptions are provided for the
successful integration of the board into the user's system.

2.2 CAPABILITIES AND SPECIFICATIONS

The AM-600/T circuit board provides general purpose, single board interface
capability between the Alpha Micro bus and the industry standard 1/2 inch
magnetic tape formatter. A maximum of two formatters can be used with each
AM-600/T for a total of eight tape transports. Specifications for the
AM-600/T circuit board are contained in Table 2-1.

TABLE 2-1. AM-600/T Specifications

PARAMETER	SPECIFICATION
Interface	Alpha Micro bus for CPU, a maximum of eight tape transports through two formatter units.
Interrupts	Multiple level interrupt capability, user selected.
Tape Format	Controls both 7 and 9 track tape formats.
Tape Density	Controls transports with densities of up to 1600 bytes/inch.
Tape Speed	Controls transports with tape velocities up to 37.5 inches/sec.
Data Transfer	Full DMA data transfer capability of data blocks up to 65K bytes.
Board Control	Software control over virtually all standard formatter modes and operations.
Cables	Two 50-conductor flat ribbon cables interface with formatter unit.
Circuit Board	Standard 9" x 10" with 100 pin connector to interface with CPU bus system.
Power	+8 V @ 2.1 Amps
Environmental	Temperature 10 to 30 degrees (Centigrade) Humidity 10% - 80% (non-condensing)

2.3 INTERFACE DESCRIPTION AND WIRING

The AM-600/T circuit board provides interface capability between the standard Alpha Micro bus and magnetic tape transport formatter units.

2.3.1 Alpha Micro Bus Interface

The AM-600/T circuit board is fully compatible with all Alpha Micro bus-oriented systems. The board and its associated tape transports are addressed through the address lines, and data is transferred through the standard data in and data out lines. The board is compatible with both the 8-bit bus configuration and also the 16-bit CPU configuration. See Paragraph 2.3.4 for selection of the various available user options.

Only DMA data transfers are accommodated for maximum data transfer rates. The Alpha Micro bus connections are made via the bottom edge connector and are listed in Table 2-2. See Chapter 4 for complete descriptions of all interface signals.

TABLE 2-2. Alpha Micro Bus Interface Signals (Sheet 1 of 6)

SIGNAL	NAME	J1 PIN NO.
+8	8 Volts	1
$\overline{VI0}$	Vectored Interrupt 0	4
$\overline{VI1}$	Vectored Interrupt 1	5
$\overline{VI2}$	Vectored Interrupt 2	6
$\overline{VI3}$	Vectored Interrupt 3	7
$\overline{VI4}$	Vectored Interrupt 4	8
$\overline{VI5}$	Vectored Interrupt 5	9
$\overline{VI6}$	Vectored Interrupt 6	10
$\overline{VI7}$	Vectored Interrupt 7	11
A18	Address 18	15
A16	Address 16	16
A17	Address 17	17
$\overline{STATDSB}$	Status Bus Disable. A low indicates a 16-bit transfer; a high indicates an Address bus transfer.	18
$\overline{C}$/CDSB	Command/Control Bus Disable	19

Table 2-2. Alpha Micro Bus Interface Signals (Sheet 2 of 6)

SIGNAL	NAME	J1 PIN NO.
GND	Ground	20
$\overline{\text{ADDDSB}}$	Address Bus Disable	22
$\overline{\text{DODSB}}$	Data Bus Disable	23
02	Phase 2 Clock	24
$\overline{\text{STVAL}}$	Status Valid	25
PHLDA	DMA Acknowledge Line	26
PWAIT	CPU Wait	27
A5	Address 5	29
A4	Address 4	30
A3	Address 3	31
A15	Address 15	32
A12	Address 12	33
A9	Address 9	34
DO1	Bits 0-7	35
DO0	Data Out Bus	36
A10	Address 10	37

Table 2-2.   Alpha Micro Bus Interface Signals (Sheet 3 of 6)

SIGNAL	NAME	J1 PIN NO.
DO4	Data Out Bus	38
DO5	Data Out Bus	39
DO6	Data Out Bus	40
DATAIN2	Data In Bus	41
DATAIN3	Data In Bus	42
DATAIN7	Data In Bus	43
$\overline{SM1}$	Bus Master OP Code Fetch	44
SOUT	I/O Output Cycle	45
SINP	I/O Input Cycle	46
SMEMR	Memory Read Cycle	47
$\overline{SWLTA}$	Halt Acknowledge	48
GND	Ground	50
+8	+8 Volts	51
$\overline{DMA0}$	Direct Memory Access	55
$\overline{DMA1}$	Direct Memory Access	56

Table 2-2. Alpha Micro Bus Interface Signals (Sheet 4 of 6)

SIGNAL	NAME	J1 PIN NO.
DMA2	Direct Memory Access	57
SXTRQ	16-bit Request	58
A19	Address 19	59
A20	Address 20	61
A21	Address 21	62
A22	Address 22	63
A23	Address 23	64
ADVAL	Optional signal which indicates that the upper byte address information is on the data bus.	65
WRDIS	Prevents write execution	66
DMARCVD	DMA Received	69
GND	Ground	70
PRDY	Ready	72
PHOLD	DMA Request Line	74

Table 2-2. Alpha Micro Bus Interface Signals (Sheet 5 of 6)

SIGNAL	NAME	J1 PIN NO.
PSYNC	Processor Sync, Start of Bus Cycle.	76
$\overline{\text{PWR}}$	Write Strobe	77
PDBIN	Data Bus Input Command	78
A0	Address 0	79
A1	Address 1	80
A2	Address 2	81
A6	Address 6	82
A7	Address 7	83
A8	Address 8	84
A13	Address 13	85
A14	Address 14	86
A11	Address 11	87
DO2	Data Out Bus	88

Table 2-2. Alpha Micro Bus Interface Signals (Sheet 6 of 6)

SIGNAL	NAME	J1 PIN NO.
DO3	Data Out Bus	89
DO7	Data Out Bus	90
DATAIN4	Data In Bus	91
DATAIN5	Data In Bus	92
DATAIN6	Data In Bus	93
DATAIN1	Data In Bus	94
DATAIN0	Data In Bus	95
$\overline{\text{SINTA}}$	Interrupt Acknowledge	96
$\overline{\text{SWO}}$	Bus Master Output Cycle	97
GND	Ground	100

2.3.2 Tape Transport Formatter Interface

The tape transport formatter circuit board interfaces with a maximum of eight tape transports through two formatter units.   Interface signal connections are made through J2 and J3 on the top edge of the circuit board and are listed in Table 2-3. See Chapter 4 for a complete description of interface signals.

TABLE 2-3. Tape Transport Formatter Interface Signals

J2				J3			
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	G	26	$\overline{W3}$	1	RP	26	$\overline{NRZI}$
2	$\overline{FBY}$	27	G	2	$\overline{R0}$	27	G
3	G	28	$\overline{W6}$	3	$\overline{R1}$	28	$\overline{RDY}$
4	$\overline{LWD}$	29	G	4	$\overline{LP}$	29	G
5	G	30	$\overline{W2}$	5	G	30	$\overline{RWD}$
6	$\overline{W4}$	31	G	6	$\overline{R4}$	31	G
7	G	32	$\overline{W5}$	7	G	32	$\overline{FPT}$
8	$\overline{GO}$	33	G	8	$\overline{R7}$	33	G
9	G	34	$\overline{WRT}$	9	G	34	$\overline{RSTR}$
10	$\overline{W0}$	35		10	$\overline{R6}$	35	G
11	G	36		11	G	36	$\overline{WSTR}$
12	$\overline{W1}$	37	G	12	$\overline{HER}$	37	G
13		38	$\overline{EDIT}$	13	G	38	$\overline{DBY}$
14	$\overline{SGL}$	39	G	14	$\overline{FMK}$	39	
15		40	$\overline{ERASE}$	15	G	40	$\overline{SPEED}$
16		41	G	16	$\overline{CCG}$	41	
17	G	42	$\overline{WFM}$	17	G	42	$\overline{CER}$
18	$\overline{REV}$	43		18	$\overline{FEN}$	43	G
19	G	44		19	G	44	$\overline{ONL}$
20	$\overline{REW}$	45	$\overline{PAR}$	20	$\overline{R5}$	45	
21		46		21	G	46	$\overline{TAD}$
22	$\overline{WP}$	47	G	22	$\overline{EOT}$	47	
23	G	48	$\overline{R2}$	23	G	48	$\overline{FAD}$
24	$\overline{W7}$	49	G	24	$\overline{OFL}$	49	
25	G	50	$\overline{R3}$	25	$\overline{7TK}$	50	$\overline{DEN}$

G = Ground

2.3.3 Wiring and Connections

For formatters with flat cable interface, the connections are straight forward since no pin translations are required. The maximum overall cable length is 20 feet. If two formatters are daisy-chained together, terminating resistors should be left only in the formatter at the end of the chain.

Formatters with a 100 pin PC edge connection require an adapter board (DWB-00601-00) to connect the flat cable to the edge connector. One adapter board is required for each formatter unit, and the formatters can be daisy-chained as described in the previous paragraph. The adapter board is shown in Figure 2-1, and the wire list is given in Table 2-4.

100 PIN VIKING CONNECTER
(^V450/1JKC5)

HOLES USED TO SECURE
BOARD TO FORMATTER

| A01 | J1 (100 PIN EDGE CONN) | A50 |
| B01 | | B50 |

VIEWED FROM
COMPONENT SIDE

49 | J2   50 PIN 3M | 1
50 | | 2

49 | J3   50 PIN 3M | 1
50 | | 2

49 | J4   50 PIN 3M | 1
50 | | 2

49 | J5   50 PIN 3M | 1
50 | | 2

3M 3433-2002
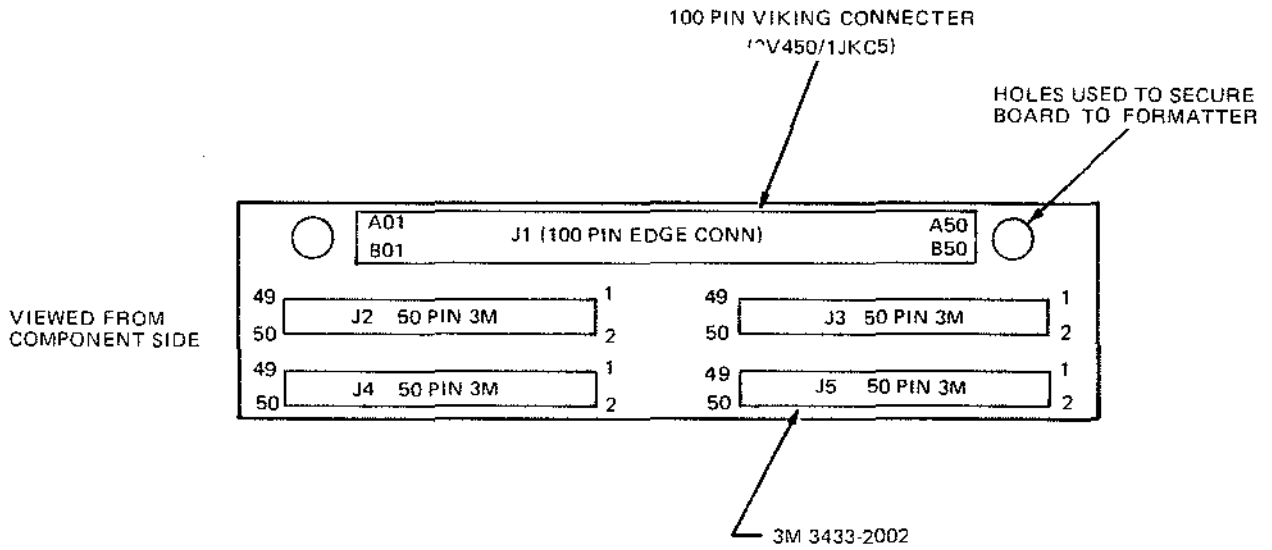
J2, J4: ALL ODD PINS EXCEPT 1, 3, 45 ARE TIED TO GROUND.
J3, J5: ALL ODD PINS ARE TIED TO GROUND EXCEPT PIN 25
J1: THE FOLLOWING PINS ARE TIED TO GROUND:
    A02, B02, A05, B05, A09, B09, A11, B11, A14, B14, A17, B17, A20, B20, A23, B23
    A26, B26, A29, B29, A32, A35, A39, B38, A41, B41

FIGURE 2-1.   Adapter for 100 Pin Edge Connector to Flat Cables

TABLE 2-4. Adapter Wire List (sheet 1 of 2)

SIGNAL NAME	FROM	TO	TO
$\overline{TAD0}$	J1-A01	J2-46	J4-46
$\overline{FAD}$	J1-B01	J3-48	J5-48
$\overline{GO}$	J1-A03	J2-8	J4-8
$\overline{TAD1}$	J1-B03	J3-46	J5-46
$\overline{WRT}$	J1-A04	J2-34	J4-34
$\overline{REV}$	J1-B04	J2-18	J4-18
$\overline{EDIT}$	J1-A06	J2-38	J4-38
$\overline{WFM}$	J1-B06	J2-42	J4-42
$\overline{THR1}$	J1-A07	J2-44	J4-44
$\overline{ERASE}$	J1-B07	J2-40	J4-40
$\overline{DEN}$	J1-A09	J3-50	J5-50
$\overline{THR2}$	J1-B09	J2-36	J4-36
N/C	J1-A10	N/C	N/C
$\overline{PAR}$	J1-B10	J2-45	J4-45
$\overline{OFL}$	J1-A12	J3-24	J5-24
$\overline{REW}$	J1-B12	J2-20	J4-20
$\overline{FEN}$	J1-A13	J3-18	J5-18
$\overline{LWD}$	J1-B13	J2-4	J4-4
$\overline{WP}$	J1-A15	J2-22	J4-22
N/C	J1-B15	N/C	N/C
$\overline{W1}$	J1-A16	J2-12	J4-12
$\overline{W0}$	J1-B16	J2-10	J4-10
$\overline{W3}$	J1-A18	J2-26	J4-26
$\overline{W2}$	J1-B18	J2-30	J4-30
$\overline{W3}$	J1-A18	J2-26	J4-26
$\overline{W4}$	J1-B19	J2-6	J4-6
$\overline{W7}$	J1-A21	J2-24	J4-24
$\overline{W6}$	J1-B21	J2-28	J4-28
$\overline{DBY}$	J1-A22	J3-38	J5-38

Table 2-4. Adapter Wire List (Sheet 2 of 2)

SIGNAL NAME	FROM	TO	TO
$\overline{FBY}$	J1-B22	J2-2	J4-2
$\overline{HER}$	J1-A24	J3-12	J5-12
$\overline{CCG}$	J1-B24	J3-16	J5-16
$\overline{FMK}$	J1-A25	J3-14	J5-14
$\overline{CER}$	J1-B25	J3-42	J5-42
$\overline{ONL}$	J1-A27	J3-44	J5-44
$\overline{RDY}$	J1-B27	J3-28	J5-28
$\overline{FPT}$	J1-A28	J3-32	J5-32
$\overline{RWD}$	J1-B28	J3-30	J5-30
$\overline{EOT}$	J1-A30	J3-22	J5-22
$\overline{LP}$	J1-B30	J3-4	J5-4
$\overline{NRZI}$	J1-A31	J3-26	J5-26
N/C	J1-B31	N/C	N/C
$\overline{SGL}$	J1-A33	J2-14	J4-14
$\overline{7TK}$	J1-B33	J3-25	J5-25
$\overline{WSTR}$	J1-A34	J3-36	J5-36
$\overline{SPEED}$	J1-B34	J3-40	J5-40
$\overline{RP}$	J1-A36	J3-1	J5-1
$\overline{RSTR}$	J1-B36	J3-34	J5-34
$\overline{R1}$	J1-A37	J3-3	J5-3
$\overline{R0}$	J1-B37	J3-2	J5-2
$\overline{R3}$	J1-A39	J2-50	J4-50
$\overline{R2}$	J1-B39	J2-48	J4-48
$\overline{R5}$	J1-A40	J3-20	J5-20
$\overline{R4}$	J1-B40	J3-6	J5-6
$\overline{R7}$	J1-A42	J3-8	J5-8
$\overline{R6}$	J1-B42	J3-10	J5-10
$\overline{LOL}$	N/C	J2-16	J4-16

2.3.4 User Options

The AM-600/T circuit board accommodates several options that are selected by the user for specific requirements. These options are for addressing, interrupts, DMA selections, CPU type, memory addressing, and tape formatter options. The following sections describe these jumper options in detail.

2.3.4.1 Addressing

The standard I/O address block for the AM-600/T is A3 through A7 and is etched on the printed circuit board. If a different address block is desired, cut the appropriate etch on the component side of the board and jumper the board for the desired address (see Figure 2-2).

MPC/NO MPC

CPU Compatibility
Jumpers

I/O Address
Selection

Vectored Interrupts
and DMA Selection
Jumpers
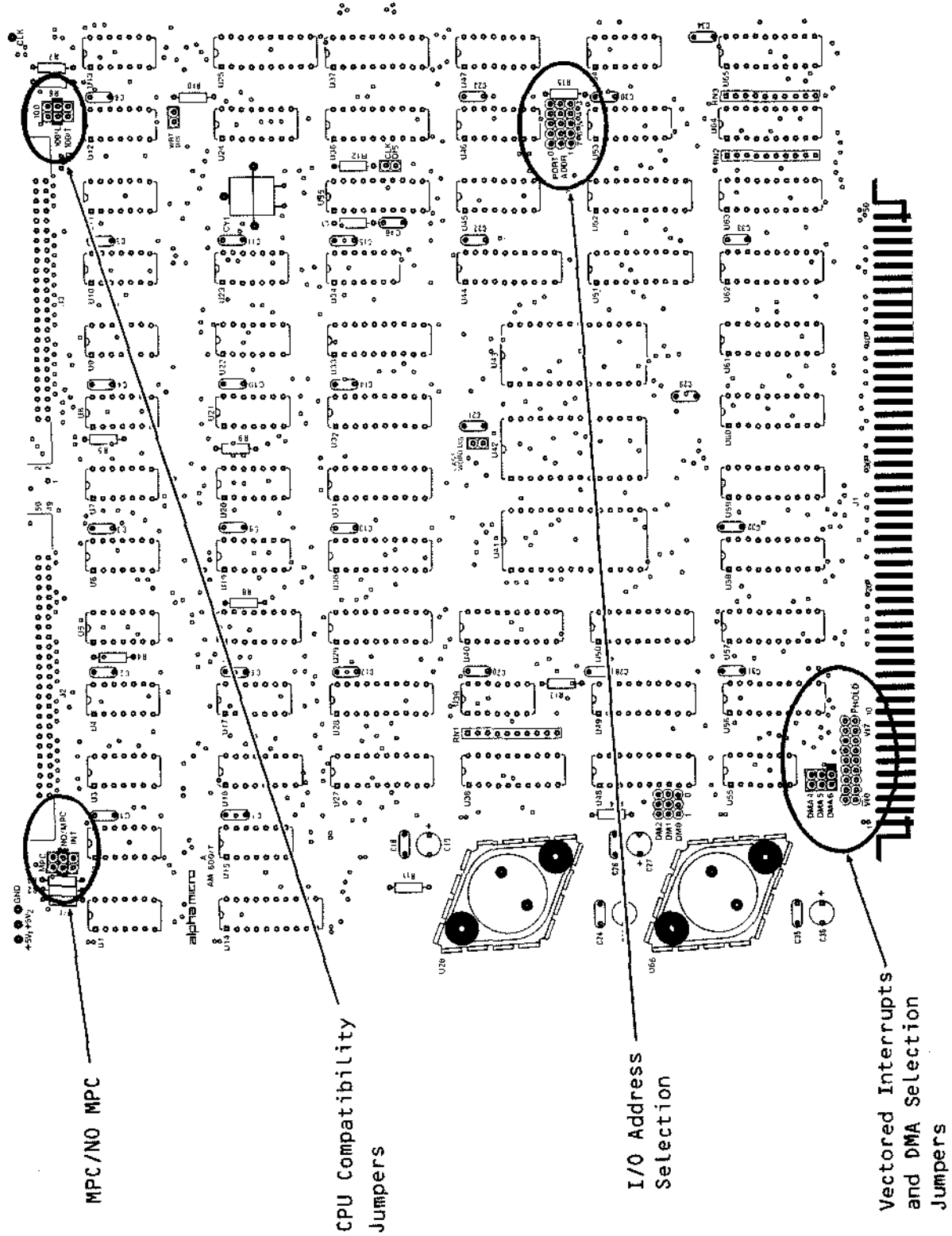
FIGURE 2-2. Jumper Options

2.3.5 Interrupts

The interrupt signal from the AM-600/T ($\overline{\text{INTR}}$) can be jumpered to any of the vectored interrupt lines $\overline{\text{VI0}}$- VI7. The standard configuration is with no jumpers connected. If required, the jumpers are located in the lower left section of the board as shown in Figure 2-2.

2.3.6 DMA Options

Two modes of DMA operation are possible with the AM-600/T. The first mode releases the bus to the CPU after every read or write cycle. With this mode of operation, the AM-600/T must re-acquire control of the bus as each byte of data is ready for transmission. This is the recommended mode for magnetic tape drives.

The second mode of operation retains control of the bus until the entire command has been completed. Therefore, if a large block of data were to be read from memory and stored on the tape, all the data would be transferred without the CPU regaining control of the bus. This mode should only be used when the data transfer speed is high enough such that re-acquiring the bus in between data byte transfers results in insufficient data transfer rates. This mode of operation can be selected under software control. See Chapter 3.

2.3.7 CPU Compatibility

The AM-600/T is compatible with the Alpha Micro AM-100 CPU, Alpha Micro AM-100/T and AM-100/L 16-bit CPUs. Some of these boards may require jumper modifications or etch cuts for purposes of compatability. The following paragraphs describes these modifications on a board by board basis.

2.3.7.1 AM-100 CPU Compatibility

To provide AM-600/T compatibility with the Alpha Micro AM-100 CPU, jumpers must be installed in both the AM-600/T and the AM-100 board No. 2.

On the AM-600/T board install the following jumpers as required. (Refer to Figure 2-2.)

Set DMA level 5. This may be accomplished by cutting the etch at DMA 6 (used for AM-100/T and AM-100/L systems) then jumpering the board for DMA 5.

NO/MPC is the standard setting and should not require modification.

CPU jumper should be set for AM-100.

The following jumpers are required on the AM-100 Circuit Board No. 2 for system compatiblity. Refer to the AM-100 Technical Manual, DWM-00100-00, for further information.

    a. DMAGRANT5 jumper.
    b. DMA Request 5 jumper (VI5).

2.3.7.2 AM-100/T CPU Compatibility.

Verify the following jumper settings. (Refer to Figure 2-2.)

DMA level 6 has been assigned to the AM-600/T interface. The board is etch strapped for this assignment and should require no modification.

NO/MPC is the standard setting and should require no modification. However, if your system should contain an AM-700 board in combination with the AM-100/T, this jumper should be set to the MPC position. For further jumper information regarding the AM-700 board refer to the AM-700 Installation Instructions, PDI-00700-00.

Set the CPU selection jumper to AM-100/T.

2.3.7.3 AM-100/L CPU Compatibility

No AM-600/T jumper modifications are required with the AM-100/L CPU, although you may wish to verify these settings. (Refer to Figure 2-2.)

DMA level 6. This is the standard setting as it comes from Alpha Micro.

NO/MPC is the standard setting.

CPU jumper should be configured for the AM-100/L.

CHAPTER 3

PROGRAMMING

3.1 INTRODUCTION

This chapter describes the programming requirements for the AM-600/T circuit board.   I/O ports and data transfer and controls are described for integration into the user's system.

3.2 I/O PORTS

Eight I/O ports are required by the AM-600/T circuit board as shown in Table 3-1 through 3-7. The I/O port address is jumper selectable by a series of jumpers as described in Chapter 2 of this manual. The standard I/O address range is: A3-A7. Table 3-1 summarizes the functions of each I/O port.

The function of each of the I/O registers is as follows:

1. <u>External Control Register.</u> Selects address and controls for selected tape transport. See Table 3-2 for a description of control bits.

2. <u>Transport Status Register.</u> Indicates mode and status of selected tape transport. See Table 3-3 for a description of status bits.

3. <u>Formatter Command Register.</u> Selects tape mode and motion to the selected transport. See Table 3-4 for a description of control bits.

4. <u>Formatter Status Register.</u> Indicates status of formatter. See Table 3-5 for a description of status bits.

5. <u>Internal Control Register.</u> Contains enables and DMA register instructions. See Table 3-6 for a description of control bits.

6. <u>Formatter Command Summary.</u> See Table 3-8 for a description of various legal commands.

7. <u>DMA Address Register/Word Count Register.</u> A 24 bit DMA controller is contained in the DMA logic and may be programmed as outlined in the following paragraph.

The command for all 8-bit bytes may be set up by loading bits 5-7 of the internal control register. After the command has been set up, the appropriate byte may be clocked by an output to either I/O port A4 (low byte), A5 (middle byte), or A6 (high byte). After all parameters of the DMA controller have been set up, the DMA controller must be enabled (command = 111) before performing any DMA operation (READ or WRITE from mag tape). After completing a READ block command, the DMA Word Count Registers may be read to determine the data block size. See Table 3-7 for a summary of DMA controller instructions. See Chapter 4 for detailed specifications of the DMA address generator circuit.

TABLE 3-1. I/O Port Definitions

I/O PORT*	INPUT	OUTPUT	COMMENTS
X0	Transport Status	EXT Control Register	See Tables 3-2, 3-3
X1	Formatter Status	Formatter Command Register	See Tables 3-4, 3-5
X2	--	--	Not used
X3	Not Used	INT Control Register	See Table 3-6
X4	DMA Register Low Byte (A0-A7)	DMA Register Low Byte (A0-A7)	See Chapter 4
X5	DMA Register Middle Byte (A8-A15)	DMA Register Middle Byte (A8-A15)	See Chapter 4
X6	DMA Register High Byte (A16-A23)	Data Register High Byte (A16-A23)	See Chapter 4
X7	--	--	Not used.

* I/O port address is jumper selectable to any even block of I/O addresses. :A0-:A7 is the standard I/O address range.

TABLE 3-2. External Control Register (Output Function)

BIT	FUNCTION	COMMENTS
0	Transport Address 0	Binary address for up to four
1	Transport Address 1	transports.
2	Formatter Address 1	Selects one of two formatters.
3	Read Threshold 1	Specifies high threshold for read after write operation.
4	Read Threshold 2	Specifies an extra low threshold level for the real electronics in the tape drive.
5	Low Density Select	Selects lower data transfer packing density.
6	Not Used	
7	Not Used	

TABLE 3-3. Transport Status Register (Input Function)

BIT	FUNCTION	COMMENTS
0	7 Track	Indicates transport is in 7 track mode.
1	NRZI Mode	Indicates transport is in NRZI mode.
2	End of Tape	Indicates end of tape has been detected during the previous command.
3	Load Point	Indicates load point on tape.
4	File Protect	Indicates file protect status.
5	Rewinding	Indicates transport is rewinding.
6	On-Line	Indicates transport is on line.
7	Ready	Indicates transport ready status.

TABLE 3-4. Formatter Command Register (Output Function)

BIT	FUNCTION	COMMENTS
0	Reverse	Determines direction of tape motion.
1	Write	Specifies write mode when asserted.
2	Write File Mark	File mark written on tape, or in read mode, this bit is set to skip to the next block.
3	Edit	Edit mode of operation.
4	Erase	Selects erase mode.
5	Rewind Pulse	Setting and then resetting this bit causes the selected transport to rewind to load point.
6	Off-Line Pulse	Setting and then resetting this bit causes the selected transport to go off-line and into local mode.
7	Go Pulse	Setting and then resetting this bit, while holding the other bits stable, will initiate a command to the formatter. See Command Summary in Table 3-8.

TABLE 3-5. Formatter Status Register (Input Function)

BIT	FUNCTION	COMMENTS
0	Done	Indicates that the pre-programmed byte count has been satisfied by the appropriate command.
1	Hard Error	Indicates detection of uncorrectable read error. This bit must be ignored if filemark is detected (bit 2).
2	Filemark	Indicates detection of a tape filemark.
3	PE Tape	Indicates the presence of a phase encoded tape, if transport is in phase encoded mode. (Not latched on interface).
4	Data Request	Indicates interface is ready for additional READ or WRITE byte operations.
5	Lost Data	Indicates data lost during either a READ or WRITE command.
6	Interrupt	Indicates that an interrupt has been generated by the AM-600/T. This bit is only valid after a GO command has been issued.
7	Formatter Busy	Indicates that formatter is processing a command.

TABLE 3-6.   Internal Control Register (Output Function)

BIT	FUNCTION	COMMENTS
0	Not Used	
1	HOG	This bit is used to select the DMA mode of operation. See Chapter 3.3.
2	Internal MPC Control	If the MPC shorting block is positioned to internal, this bit allows software control of the MPC jumpers. 0 = No MPC 1 = MPC
3	Interface Enable	Enables interface logic and formatter logic.
4	Interrupt Enable	Enables interrupt logic.
5 6 7	I0 I1 I2	DMA Register instructions. See detailed description of command codes contained in Table 3-7. Before issuing any READ or WRITE command to the formatter, the DMA registers must be enabled (111 code). See paragraph 4.3.1.2 for control mode description.

TABLE 3-7. DMA Register Instructions

I_2	I_1	I_0	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D_0-D_7
L	L	L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	D_0-D_2→CR	INPUT
L	L	H	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CR→D_0-D_2 (Note 1)
L	H	L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WC→D
L	H	H	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	AC→D
H	L	L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WCR→WC	HOLD	AR→AC	HOLD	Z
						1	HOLD	ZERO→WC	HOLD	AR→AC	HOLD	Z
H	L	H	5	LOAD ADDRESS	LOAD	0, 1, 2, 3	HOLD	HOLD	D→AR	D→AC	HOLD	INPUT
H	H	L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D→WR	D→WC	HOLD	HOLD	HOLD	INPUT
						1	D→WR	ZERO→WC	HOLD	HOLD	HOLD	INPUT
H	H	H	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
						2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

CR = Control Reg.   WCR = Word Count Reg.   L = LOW
AR = Address Reg.   WC = Word Counter   H = HIGH
AC = Address Counter   D = Data   Z = High Impedance

Note 1:
Data Bits D_3-D_7 are high during this instruction.

TABLE 3-8. Formatter Command Summary

COMMAND TYPE*	DESCRIPTION	COMMAND BITS					COMMENTS
		REV	WRITE	WFM	EDIT	ERASE	
Write	Write Data Block	0	1	0	X	0	Length of data block programmed in DMA registers.
Write	Write Filemark	0	1	1	0	0	Write filemark on tape.
Write	Erase 3.75"	0	1	1	0	1	
Write	Erase Programmed	0	1	0	0	1	Length of erase function programmed in DMA registers.
Read	Read Data Block	X	0	0	X	0	Data block size may be determined by reading the byte count registers within the DMA controller. To control the maximum size block to be read, the Word Count Register should be programmed with the maximum number of bytes to be transferred plus one. Writing to Memory will cease when the WCR=WCH+1. The total block size will be contained in the WC. A software timer function should be provided to guard against attempting to read blank tapes.
Skip	Skip Data Block	X	0	0	1	1	
Skip	Skip File	X	0	1	0	0	
Misc.	Formatter Reset						These commands do not cause formatter to go busy.
Misc.	Rewind						
Misc.	Off Line						

*Read and Write commands are initiated by pulsing the GO bit (see Table 3-4).

3.3   DMA DATA TRANSFER

DMA data transfer is initiated by signal (DRQ) from the control logic indicating that it is ready for more data, or has received data from the drive. If no other DMA controller in the system has control of the bus, a DMA service request is generated by the controller and transmitted to the CPU via one of the prioritized DMA request lines. The DMA controller will then wait until the DMA arbitration signals are received from the CPU indicating bus mastership for the controller.

Upon receiving the DMA arbitration signals, the DMA controller places the DMA address register contents on the system address bus and begins either a READ or WRITE sequence to the mag tape drive, depending upon Bit 1 of the Formatter Command Register.

Two modes of DMA operation are possible with the AM-600/T. The first mode releases the bus to the CPU after every read or write cycle. With this mode of operation, the AM-600/T must re-acquire control of the bus as each byte of data is ready for transmission and is the recommended mode for magnetic tape drives.

The second mode of operation retains control of the bus until the entire command has been completed. Therefore, if a large block of data were to be read from memory and stored on the tape, all the data would be transferred without the CPU regaining control of the bus. This mode should only be used when the data transfer speed is high enough such that re-acquiring the bus in between data byte transfers results in insufficient data transfer rates. This mode of operation is selected by Bit 1 of the Internal Control Register. See Table 3-6.

3.4 INTERRUPT OPERATION

Interrupt operation is enabled by Bit 4 of the Internal Control Register. If enabled, an interrupt will be generated after completion of a READ or WRITE command when the tape begins to decelerate. The interrupt flip-flop will be reset by a GO command to the formatter.

CHAPTER 4

FUNCTIONAL THEORY OF OPERATIONS

4.1 INTRODUCTION

The AM-600/T Magnetic Tape Transport Formatter Interface circuit board
contains the integrated circuit elements necessary for the data processing
functions described in Chapters 1, 2, and 3 of this manual. This Chapter
describes the functional theory of operation of the circuit board and also
provides information for each of the integrated circuit elements.

4.2 CIRCUIT BOARD OPERATION

This circuit board provides control and interface capability between the
Alpha Micro S-100 bus and an industry standard 1/2" Magnetic Tape Transport
Formatter.   The functional block diagram of the circuit board is shown in
Figure 4-1, and the circuit board schematic is contained in Appendix B of
this manual. Table 4-1 contains a list of the signals used in this circuit
board with descriptions of their functions. Reference Table 2-2 for a list
of bus interface signals. For formatter interface signals see Table 4-2.
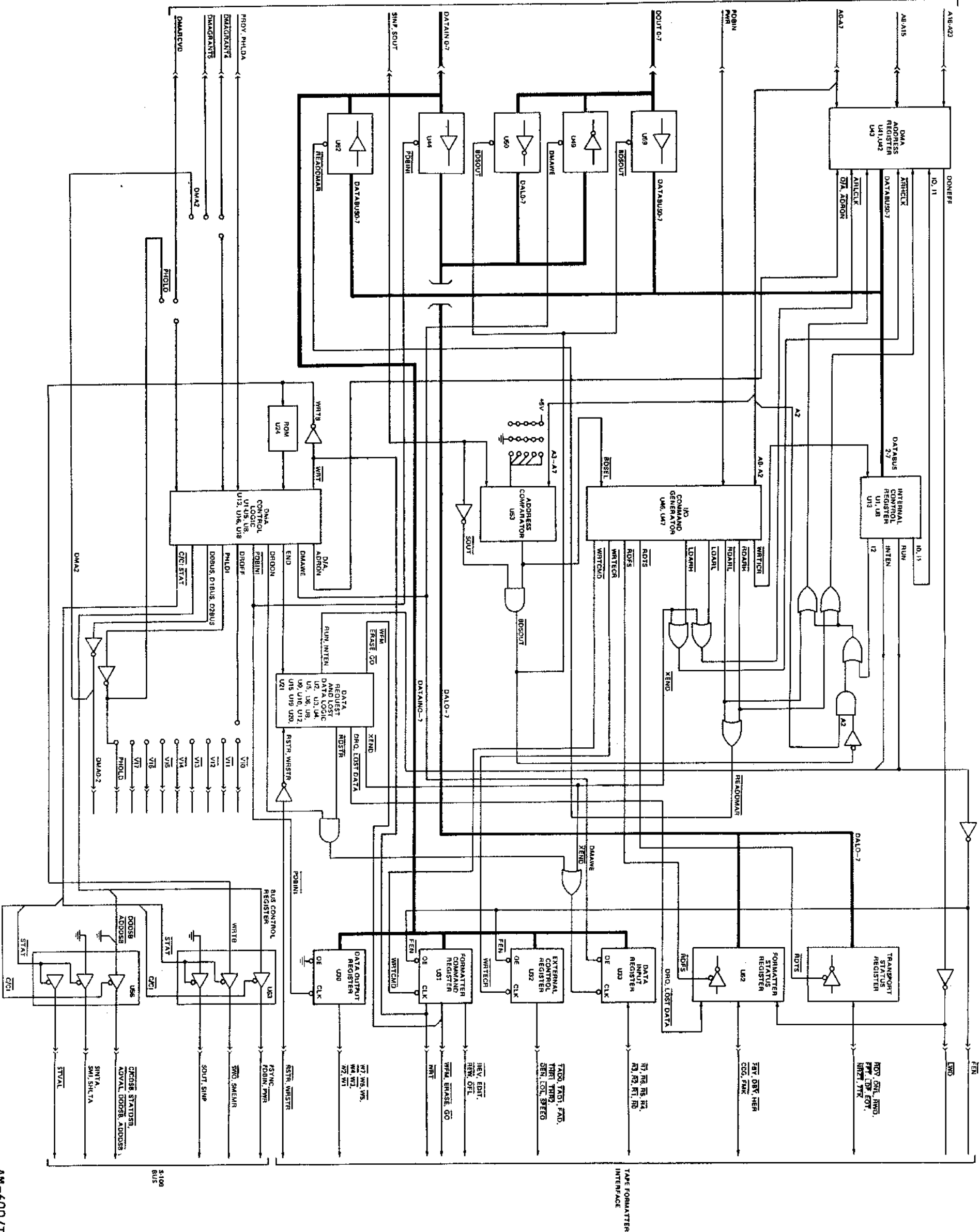
FIGURE 4-1. AM-600/T Functional Block Diagram   Page 4-3

TABLE 4-1. AM-600/T Signal List (sheet 1 of 9)

SIGNAL	NAME	FUNCTION
$\overline{ADRON}$	Address Register Output Enable	Places address data from DMA address register onto Data Bus
$\overline{ARHCLK}$	Address Register High Byte Clock	Clock input to the counters and registers in the DMA address registers for the upper eight bits of address data.
$\overline{ARMCLK}$	Address Register Middle Byte Clock	Clock input to the counters and registers in the DMA address register for the middle eight bits of address data.
$\overline{ARLCLK}$	Address Register Low Byte Clock	Clock input to the counters and registers in the DMA address register for the lower eight bits of address data.
$\overline{BDSEL}$	Board Select	Output of board address comparator. Asserted when Alpha Micro I/O address matches I/O address wired in jumpers.
$\overline{BDSOUT}$	Board Select Output Cycle	Asserted when AM-600/T is addressed and an output cycle is selected (BDSEL SOUT).

TABLE 4-1. AM-600/T Signal List (sheet 2 of 9)

SIGNAL	NAME	FUNCTION
B02	Buffered Phase 2 CLock	Buffered phase 2 clock from phase 2 on Alpha Micro Bus.
$\overline{CCG}$	Check Character Gate	Input from formatter set true when the read information being transmitted to the AM-600/T is a CRC character or a longitudinal redundancy check character.
C/CI $\overline{C/CI}$	Controller Command	Disables the processor address and data bus drivers while enabling the DMA controller command drivers. Sets D/A at 02 leading edge.
D/A $\overline{D/A}$	DMA Address Enable	Places address data from DMA address register onto Data Bus (optional for 8-bit format).
$\overline{DBY}$	Data Busy	Input from formatter when the transport tape is up to speed.
DAWE	DMA Write Enable	Generated during a write cycle to gate data onto the data bus and ensure its validity before, during, and after PWR.
DONE	Done	Asserted when the DMA register reaches its terminal count.

TABLE 4-1. AM-600/T Signal List (sheet 3 of 9)

SIGNAL	NAME	FUNCTION
DONECLK	Done Clock	Clock input to combine with DONE to set DONEFF.
DONEFF $\overline{\text{DONEFF}}$	Done Signal	Signifies the completion of the DMA data transfer.
DRQ $\overline{\text{DRQ}}$	Data Request	Initiates a DMA cycle indicating that the controller requires DMA service.
$\overline{\text{DRQCLK}}$	Data Request Clock	Clocks the Data Request flip-flop.
DRQFF $\overline{\text{DRQFF}}$	Data Request Signal	Generated from DRQ to directly generate PHOLD.
DRQON	Data Request On	Generated from DRQ to enable tape read logic.
END $\overline{\text{END}}$	End	Generated by the sequencer to terminate the entire DMA cycle.
$\overline{\text{ERASE}}$	Erase	Output to formatter. When asserted with WRT, executes a write command no data.

TABLE 4-1. AM-600/T Signal List (sheet 4 of 9)

SIGNAL	NAME	FUNCTION
$\overline{FEN}$	Formatter Enable	Output to tape transport generated from RUN. Enables formatters. When false, causes formatters to revert to quiescent state.
$\overline{GO}$	Initiate Command	Output to formatter to initiate any command specified by the command lines.
INIT INTEN	Initialize Interrupt Enable	Circuit board reset signal generated by PRESET from Alpha Micro bus. Enables the INTR flip-flop.
INTR	Interrupt	Provides jumper output to vectored interrupt lines VI0-VI7 (not used).
I0, I1, I2	Instruction Codes	Instruction code inputs to the DMA Address Register.
L	AM-100/L	Activated when the AM-100/L CPU is selected.
LDARH	Load DMA Register High Byte	Generates a clock to load data bits 16-24 into the high byte of DMA Address Register.
LDARM	Load DMA Register Middle Byte.	Generates a clock to load data bits 8-15 into the middle byte of DMA Address Register.

TABLE 4-1. AM-600/T Signal List (sheet 5 of 9)

SIGNAL	NAME	FUNCTION
LDARL	Load DMA Register Low Byte.	Generates a clock to load data bits 0-7 into the low byte DMA address generator.
LOSTDATA $\overline{\text{LOSTDATA}}$	Lost Data Error	Set when a Read data request is generated with DRQ still set or if a a Write data request is generated with prior DMA cycle still in progress.
$\overline{\text{LWD}}$	Last Word of Data	Output to Tape Transport generated from DONEFF.
MBUS	My Bus	Enables the AM-600/T to take control of system busses.
MPC	Memory Partition Controller	Indicates presence of a Memory Partition Controller
$\overline{\text{NRZI}}$	NRZI	Input from formatter indicating transport configuration.
OB02	On-board two-phase clock	Select for the two phase on-board clock
PDBINI $\overline{\text{PDBINI}}$	Data Bus In	Used to generate PDBIN output to Alpha Micro Bus when gated by the Bus Control Register.

TABLE 4-1. AM-600/T Signal List (sheet 6 of 9)

SIGNAL	NAME	FUNCTION
PSYNCI $\overline{\text{PSYNCI}}$	Processor Sync	Used to generate PSYNC output to Alpha Micro Bus when gated by the Bus Control Register.
PWRI	Write Strobe	Used to generate PWR on Alpha Micro Bus when gated by WRDIS and Bus Control Register.
$\overline{\text{RDARH}}$	Read DMA Address Register High Byte.	Provides instruction input (I2) to upper byte DMA address register.
$\overline{\text{RDARL}}$	Read DMA Address Register Low Byte.	Provides instruction input (I2) to lower byte DMA address register.
$\overline{\text{RDFS}}$	Read Formatter Status	Gates the contents of the Formatter Status Register onto the DATIN0-7 bus.
$\overline{\text{RDSTR}}$	Tape Read Strobe	Enabled by DRQON to clock tape read
$\overline{\text{RDTS}}$	Read Transport Status	Gates the contents of the Transport Status Register onto the DATIN0-7 bus.
RDYCLK	Ready Clock	Clock signal jumpered to B02 for standard S-100 bus or B02 for Alpha Micro bus.
$\overline{\text{RDARL}}$	Read Address Register Low Byte	Read input to the counters and registers in the DMA address register for the upper eight bits of address data.

TABLE 4-1. AM-600/T Signal List (sheet 7 of 9)

SIGNAL	NAME	FUNCTION
RDARM	Read Address Register Middle Byte 3	Read input to the counters and registers in the DMA address register for the middle eight bits of address data.
RDARH	Read Address Register High Byte	Read input to the counters and registers in the DMA address register for the lower eight bits of address data.
READDMAR	Read DMA Address Register	Generated by RDARH or RDARL to gate DATABUS0-7 to DATAIN0-7.
ROMCLK	ROM Clock	Clocks the data from the ROM into the ROM output data register.
RSTR	Read Strobe	Input from formatter to sample data lines, one pulse for each character of read information.
RUN	Run	Output of internal control register from DATABUS bit 3 to generate Formatter Enable (FE) output and enable external control register and formatter command register.
S SR	AM-100 CPU Select	Used to select the AM-100 CPU

TABLE 4-1.   AM-600/T Signal List (sheet 8 of 9)

SIGNAL	NAME	FUNCTION
$\overline{\text{SOUT}}$	Activate Output Cycle	Bus input to indicate that the current bus cycle is a bus master output to an I/O address.
STAT $\overline{\text{STAT}}$	Status	Controls processor status drivers and DMA controller status drivers.
WAIT	Wait	Suppresses update clocks to the sequencer to halt operation.
$\overline{\text{WFM}}$	Write File Mark	Formatter output to write a filemark on the tape.
$\overline{\text{WRT}}$	Write to Formatter	Controls data transfer between AM-600/T and Formatter. WRT=0 Read From Formatter, WRT=1 Write To Formatter.
WRTB	Write to Bus	Enables the ROM and generates SMEMR and SWO to the Alpha Micro bus when gated by the Bus Control Register.

TABLE 4-1. AM-600/T Signal List (sheet 9 of 9)

SIGNAL	NAME	FUNCTION
$\overline{\text{WRTCMD}}$	Write to Formatter Command Register	Clock signal from I/O Command Register to load data from DATAIN bus to Formatter Command Register.
$\overline{\text{WRTECR}}$	Write to External Control Register	Clock signal from I/O Command Register to load data from DATAIN bus to Formatter Command Register.
$\overline{\text{WRTICR}}$	Write to Internal Control	Clock signal from the I/O command generator to load data from the DATABUS to the Internal Control Register.
WSTR	Write Strobe	Input from formatter. Pulses each time a data character is written onto tape.
$\overline{\text{XEND}}$	Extra End Pulse	Generated from END or from DMA control logic to clock the Data Input Register and DMA Address Register.

TABLE 4-2. AM-600/T Magnetic Tape Interface Signals (sheet 1 of 7)

MNEMONIC	NAME	AM-600 IN/OUT	LEVEL or PULSE	CONNECTOR PIN	FUNCTION
C̄C̄Ḡ	Check character Gate (NRZI Mode Only) Only)	In Gnd	Level J3-15	J3-16	Set true by the NRZI formatter when the read information being transmitted to the AM-600 is a cyclic redundancy check character (CRCC) or a longitudinal redundancy check character (LRCC). CCG= false for data characters.
C̄Ē̄R̄	Corrected Error (PE Mode Only)	In	Pulse Gnd	J3-42 J3-43	When true indicates that a single track dropout has been detected and the formatter is performing an error correction.
D̄B̄Ȳ	Data Busy	In	Level Gnd	J3-38 J3-37	True when tape is up to speed, has traversed the BBG, and the formatter is about to write data or look for a read signal on the tape. Remains true until data transfer and the post record delay is completed. Goes false when tape starts deceleration.
D̄Ē̄N̄	Density Select (7 track NRZI only)	Out	Level Gnd	J3-50 J3-49	Selects the lower of two possible data packing densities.
Ē̄D̄Ī̄T̄	Edit	Out	Level Gnd	J2-38 J2-37	When asserted with WRT, the selected transport operates in the Edit mode.

TABLE 4-2. AM-600/T Magnetic Tape Interface Signals (sheet 2 of 7)

MNEMONIC	NAME	AM-600 IN/OUT	LEVEL or PULSE	CONNECTOR PIN	FUNCTION
$\overline{EOT}$	End of Tape	In	Level Gnd	J3-22 J3-21	Status signal asserted when EOT marker is detected in the forward direction and remains until EOT marker is detected in the reverse direction.
$\overline{ERASE}$	Erase	Out	Level Gnd	J2-40 J2-39	When asserted with WRT, executes a write command with no data. A length of tape specified by LWD is erased.
$\overline{FAD}$	Formatter Address	Out	Level Gnd	J3-48 J3-47	
$\overline{FBY}$	Formatter Busy	In	Level Gnd	J2-2 J2-1	When asserted, inhibits further commands to the formatter.
$\overline{FEN}$	Formatter Enable	Out	Level J3-17	J3-18	Enables formatters. When false, causes formatters to revert to a quiescent state.
$\overline{FMK}$	File Mark	In	Pulse Gnd	J3-14 J3-13	Pulsed when a filemark is detected on the tape during a read operation or during a write file mark operation in a read after write transport.
$\overline{FPT}$	File Protect	In	Level Gnd	J3-32 J3-31	Status signal asserted when a reel of tape without a write-enable ring is mounted on the transport supply reel.

TABLE 4-2. AM-600/T Magnetic Tape Interface Signals (sheet 3 of 7)

MNEMONIC	NAME	AM-600 IN/OUT	LEVEL or PULSE	CONNECTOR PIN	FUNCTION
$\overline{GO}$	Initiate Command	Out	Pulse Gnd	J2-8 J2-7	Initiates any command specified by the command lines.
$\overline{HER}$	Hard Error	In	Pulse Gnd	J3-12 J3-11	Indicates a read error.
$\overline{LP}$	Load Point	In	Level Gnd	J3-4	Status signal asserted when the load point marker is under the photosensor and the transport is not rewinding.
$\overline{LWD}$	Last Word	Out	Level Gnd	J2-4 J2-3	When asserted during a write or erase command, indicates that the next character to be strobed into the formatter is the last character of the record.
$\overline{NRZI/PE}$	NRZI/PE	In	Level Gnd	J3-26	Indicates configuration of transport.
$\overline{OFL}$	Offline Command	Out	Pulse Gnd	J3-24 J3-23	Commands the selected transport to go off line without causing the formatter to go busy.
$\overline{OML}$	Online	In	Level Gnd	J3-44 J3-43	Status signal asserted when tape transport is on line (transport under remote control).

TABLE 4-2. AM-600/T Magnetic Tape Interface Signals (sheet 4 of 7)

MNEMONIC	NAME	AM-600 IN/OUT	LEVEL or PULSE	CONNECTOR PIN	FUNCTION
$\overline{PAR}$	Parity Select	Out	Level Gnd	J2-45	Controls parity mode for write or read data transfer. True=even (BCD) parity mode, false=odd (binary) parity mode.
$\overline{RDY}$	Ready	In	Level Gnd	J3-28 J3-27	Status signal indicating that the transport is ready to receive a remote command.
$\overline{REV}$	Reverse/Forward	Out	Level Gnd	J2-18 J2-17	When asserted, initiates reverse tape motion, false initiates forward tape motion.
$\overline{REW}$	Rewind	Out	Pulse Gnd	J2-20 J2-19	Causes the selected on line transport to rewind to load point.
$\overline{RP}$	Read Data Parity	In	Level Gnd	J3-1	Parity line for Read Data. Parity is either even or odd as selected by PAR signal.
$\overline{RSTR}$	Read Strobe	In	Pulse Gnd	J3-34 J3-33	Samples Read Data lines. One pulse for each character of read information (R0-R7, RP).
$\overline{RWD}$	Rewinding	In	Level	J3-30 J3-29	Indicates rewinding status of selected transport.

TABLE 4-2. AM-600/T Magnetic Tape Interface Signals (sheet 5 of 7)

MNEMONIC	NAME	AM-600 IN/OUT	LEVEL or PULSE	CONNECTOR PIN	FUNCTION
$\overline{R0}$	Read Data Lines	In	Level	J3-2	Transmits read data from tape transport formatter.
			Gnd		
$\overline{R1}$			Level	J3-3	
			Gnd		
$\overline{R2}$			Level	J2-48	
			Gnd	J2-47	
$\overline{R3}$			Level	J2-50	
			Gnd	J2-49	
$\overline{R4}$			Level	J3-6	
			Gnd	J3-5	
$\overline{R5}$			Level	J3-20	
			Gnd	J3-19	
$\overline{R6}$			Level	J3-10	
			Gnd	J3-9	
$\overline{R7}$			Level	J3-8	
			Gnd	J3-7	
$\overline{SGL}$				J2-14	

TABLE 4-2. AM-600/T Magnetic Tape Interface Signals (sheet 6 of 7)

MNEMONIC	NAME	AM-600 IN/OUT	LEVEL or PULSE	CONNECTOR PIN	FUNCTION
$\overline{TAD0}$ $\overline{TAD1}$	Transport Address	Out	Level		Determines which of four transports are selected by the formatter.
$\overline{WFM}$	Write File Mark	Out	Level Gnd	J2-42 J2-41	When asserted, writes a filemark on the tape.
$\overline{WP}$	Write Data Parity			J2-22	Parity line for write data. Parity is either even or odd as selected by PAR signal.
$\overline{WRT}$	Write/Read Command	Out	Level Gnd	J2-34 J2-33	True commands write action, false commands read action.
$\overline{WSTR}$	Write Strobe	In	Pulse Gnd	J3-36 J3-35	Pulses each time a data character is written onto tape.

TABLE 4-2. AM-600/T Magnetic Tape Interface Signals (sheet 7 of 7)

MNEMONIC	NAME	AM-600 IN/OUT	LEVEL or PULSE	CONNECTOR PIN	FUNCTION
$\overline{W0}$	Write Data Lines	Out	Level	J2-10	Transmits write data to the tape transport formatter.
			Gnd	J2-9	
$\overline{W1}$		Out	Level	J2-12	
			Gnd	J2-11	
$\overline{W2}$		Out	Level	J2-30	
			Gnd	J2-29	
$\overline{W3}$		Out	Level	J2-26	
			Gnd	J2-25	
$\overline{W4}$		Out	Level	J2-6	
			Gnd	J2-5	
$\overline{W5}$		Out	Level	J2-32	
			Gnd	J2-30	
$\overline{W6}$		Out	Level	J2-28	
			Gnd	J2-27	
$\overline{W7}$		Out	Level	J2-24	
			Gnd	J2-23	
$\overline{7TK}$	7 Track/9 Track	In	Level	J3-25	

4.2.1 Alpha Micro Bus Interface

The AM-600/T circuit board interfaces with the Alpha Micro S-100 bus for
programmed I/O operations between the AM-600/T and CPU.   The Alpha Micro
S-100 bus interface consists of I/O port decoding and command generation,
DATAIN bus interface, and DATAOUT bus interface.

4.2.1.1 I/O Port Decoding and Command Generation

This circuitry consists of a 6-bit address comparator and two of 1 of 8
decoders to generate the load commands and read commands to the various
ports contained on the board. These ports were defined in detail in Chapter
3 of this manual.

I/O address "A0" is etched into the PC board as the standard base I/O
address for the board.

4.2.1.2 Datain Bus Interface

The DATAIN bus serves three basic functions:

    1. It provides an output path for data to be read under program
        control from each input port on the board.   The transport and
        formatter status registers attach directly to the bus and are
        enabled by read commands from the I/O port decoder.   The DMA
        address registers operate through a tri-state buffer in a similar
        manner.

2. It provides an input path for data from memory to be written into
    the DATA Output Register under DMA control. This is accomplished
    by enabling the DATAIN0-7 receivers with $\overline{\text{PDBINI}}$ and using the
    trailing edge of the same signal to strobe the incoming data into
    the output data register.

3. It provides a path for address information for use with the
    optional memory partition controller (AM-700). This is
    accomplished by optionally gating the middle byte DMA address
    controller chip onto the DATAIN bus. The address information from
    the chip is gated onto the DATAIN bus by a signal $\overline{\text{ADRON}}$ from the
    DMA sequence controller circuitry. This signal occurs one bus
    cycle before PSYNCI is generated.

4.2.1.3 DATAOUT Bus Interface

The DATAOUT bus serves three basic functions:

1. It provides an input path for data to be written under program
    control to each output port on the board. Non-inverting receivers
    transmit the data to both DMA address registers and the Internal
    Control Register. Inverting receivers transmit the data to the
    External Control Register and Formatter Command Register. Load
    pulses from the I/O port decoder store the data into the selected
    register.

2. It provides an output path for data to memory from the Input Data
    Register. Data is transferred under DMA control with the DATAOUT
    bus drivers being enabled by $\overline{\text{DMAWE}}$ from the DMA sequence
    controller. New input data is strobed into the Input Data Register
    under two conditions:

a. At the end of the DMA transfer cycle.

b. Upon receipt of an $\overline{\text{RSTR}}$ pulse from the formatter if no DMA
    cycle is in progress.

3. It provides a path for address information when used with the
    optional memory partition controller (AM-700). This is
    accomplished by optionally gating the upper byte DMA address
    controller chips onto the DATAOUT bus. The address information
    from the chip is gated onto the DATAOUT bus in the same manner as
    the middle byte described in the previous section.

4.2.2 Magnetic Tape Formatter Interface

The AM-600/T connects to the magnetic tape formatter through two 50-pin flat
cables as described in Chapter 2. Data, commands, and status signals pass
through the registers shown on the right side at Figure 4-1. The data
exchange and timing is described in the following paragraphs.

4.2.2.1 Data Request Logic

Data Request logic (DRQ) is basically a request for a DMA cycle to begin.
This happens whenever data is to be read from the formatter or supplied to
the formatter.

1. Read from formatter ($\overline{\text{WRT}}$=0).
    Data transmitted from the formatter is strobed into the Input Data
    Register by RDSTR (trailing edge). If WFM and ERASE are both
    false, RDSTR trailing edge also generates DRQ which initiates a DMA
    request cycle. After the DMA cycle is in progress, DRQ is reset by
    PSYNCI and is then ready for more data.

2. Write to formatter ($\overline{WRT}$=1).

   After a Write Data command, the first byte of data must be loaded
   into the Output Data Register. This is accomplished by setting DRQ
   on the trailing edge of the Write Data Command (GO-WRT). As each
   byte is read by the formatter, $\overline{WSTR}$ is sent back, acknowledging
   the receipt of the data. The trailing edge of $\overline{WSTR}$ is then used
   to generate subsequent DRQs. This continues until the last byte to
   be sent to the formatter is in the Output Data Reegister, at which
   time DONEFF prevents any more DRQs from being generated and
   transmits $\overline{LWD}$ (last word of data) to the formatter. As with the
   READ cycle, after the DMA cycle is in progress, DRQ is reset by
   PSYNCI in anticipation of the next cycle.

4.2.2.2 Interrupt Logic

Interrupt is generated under only one condition. Interrupt Enable must be
set. When INTEN is set an interrupt will be generated when the tape begins
to decelerate after a tape movement command. The interrupt is reset by
reading the formatter status register. Interrupts are not normally used by
the CPU in the present AM-600/T configuration.

4.2.2.3 Lost Data Detector

Depending upon formatter data rates and CPU DMA handshaking overhead, it is
possible that data requests by the formatter may not be serviced in time.
The lost data detector attempts to detect this fault condition. The
conditions detected are as follows:

1. READ

   If a data request is generated by the formatter with DRQ still set
   from a prior request, the LOST DATA bit will be set.

2. WRITE

If a data request is generated by the formatter with a prior DMA cycle still in progress, the LOST DATA bit will be set.

The LOST DATA bit is reset upon issuing any command to the formatter.

4.2.2.4 Miscellaneous Latches

Three signals from the formatter are latched by the interface and processed after the present command has been executed. These signals are:

1. End of Tape Mark Detected.

2. Hard Error Detected.

3. File Mark Detected.

These latches are all reset upon issuing any command to the formatter.

4.2.3 DMA Sequence Control

The DMA control circuitry provides compatibility with all standard Alpha Micro CPU boards as summarized below.

4.2.3.1 Standard Alpha Micro bus Exchange Timing (AM-100/T, AM-100/L Systems)

Timing and sequence of the exchange cycle between the AM-600/T and the Alpha Micro bus is shown in Figure 4-2 and described in the following paragraphs.
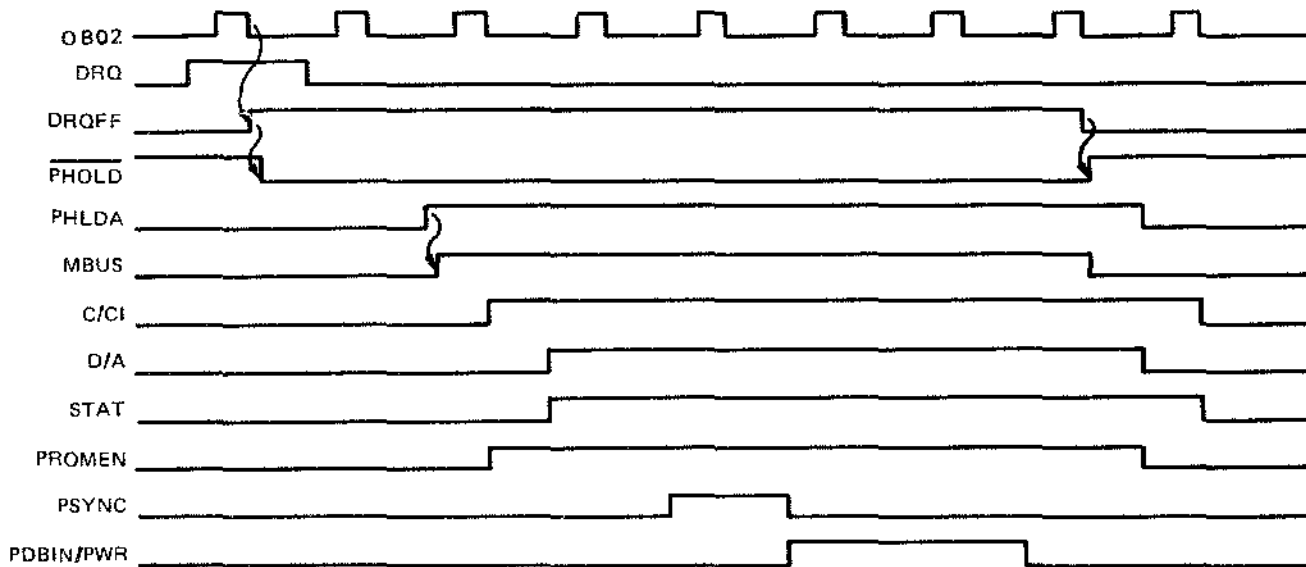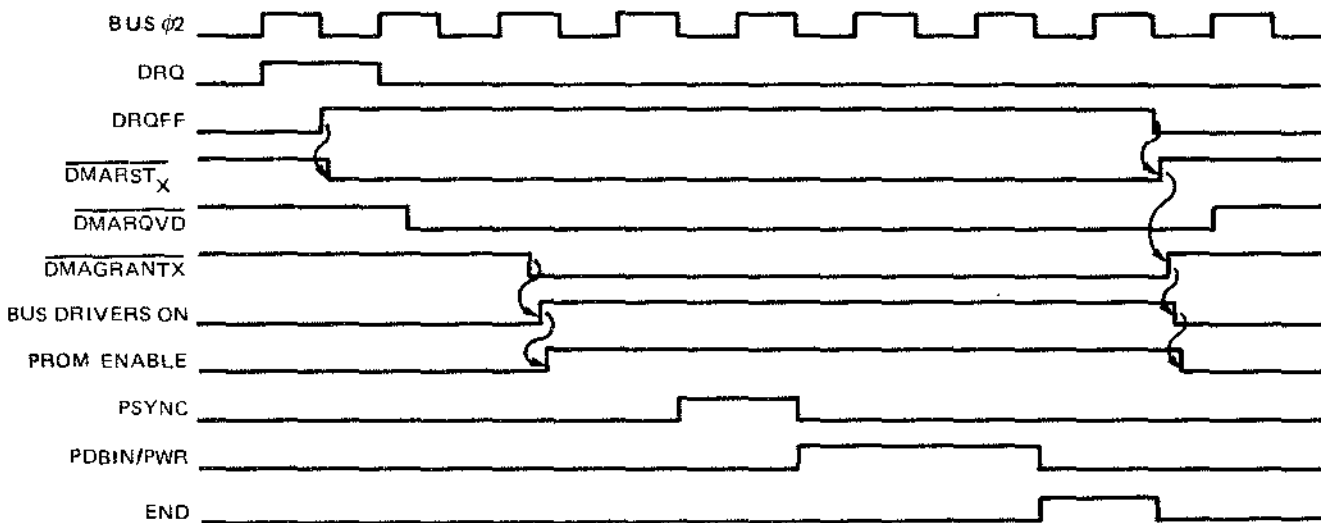
FIGURE 4-2. Standard Alpha Micro Bus DMA Timing

A DMA cycle is initiated by DRQ indicating that the controller requires DMA
service. This signal is strobed by the trailing edge of an on-board
free-running 3 MHz clock (OB02) to generate DRQFF which directly generates
PHOLD.   Note that DRQ is gated through only when PHOLD   is not asserted to
prevent any race conflicts in the bus arbitration logic.

PHOLD   signals the processor that a potential bus master desires control of
the bus. The processor responds to PHOLD by issuing PHLDA indicating   that
the processor is relinquishing control of the bus.

The time interval between $\overline{\text{PHOLD}}$ and PHLDA assertions is the arbitration time for DMA controllers to establish which one will gain control of the bus. During this time, each requestor tries to put his assigned priority on the bus (DMA0-2) and checks to see if a higher priority is present. If so, interfering lower order assertions are removed. At PHLDA leading edge time, the mbus flip-flop is strobed, with the highest priority DMA requester's MBUS flip-flop being set to indicate bus control.

The priority of each DMA controller is set by three jumpers on each board. These jumpers represent the octal code for the DMA priority assigned to each board.

If MBUS is set, the DMA controller begins its takeover of the system busses. Signal C/CI is set at 0B02 trailing edge and is used to disable the processor address and data bus drivers while enabling the DMA controller command drivers. C/CI also sets D/A at 0B02 leading edge time. Signal D/A is used to disable the processor command drivers and also $\overline{\text{STAT}}$ at 0B02 leading edge time. $\overline{\text{STAT}}$ is used to disable the processor status drivers while enabling the DMA controller status drivers.

After the DMA controller has transferred the required data, it will relinquish control of the bus as follows:

1. DRQFF is reset by END on 0B02 trailing edge time. This indicates that the last data transfer for this DMA cycle has just taken place.

2. $\overline{\text{PHOLD}}$ is released, signaling the processor that the DMA cycle is complete.

3. D/A is reset by $\overline{\text{PHOLD}}$ at 0B02 leading edge time, thereby enabling the processor command drivers and disabling the sequencer.

4. C/CI and $\overline{STAT}$ are reset at 0B02 trailing edge time. This effectively disables the remaining DMA controller drivers and enables all remaining processor drivers.

5. As soon as PHLDA is dropped by the processor, the bus exchange is complete.

4.2.3.2 AM-100 Compatible Bus Exchange Timing

Timing and sequence of the exchange between the AM-600/T and the Alpha Micro AM-100 8-bit bus is shown in Figure 4-3 and described in the following paragraphs.

FIGURE 4-3. AM-100 Compatible Control DMA Timing

A DMA cycle is initiated by DRQ indicating that the controller requires DMA service.   This signal is strobed by bus 02 trailing edge to generate DRQFF

which is used to signal the processor for service. The DMA request is routed to one of eight DMA priority lines ($\overline{\text{VIO- 7}}$) via a jumper on the board. This determines the priority for each DMA controller. Once the processor receives a DMA request, it issues DMARCVD indicating that no DMA controller may subsequently generate another DMA request. The standard DMA level for the AM-600/T is VI6. This can be changed by an etch cut and jumper on the board. See Figure 2-2.

One cycle after DMARCVD, a corresponding $\overline{\text{DMAGRANT}}$x signal will be issued by the processor. This signal must be received by the DMA controller via a jumper on the board. This jumper must correspond to the jumper described in the above paragraph. See Figure 2-2.

$\overline{\text{DMAGRANT}}$x tristates the processor bus drivers and is used by the DMA controller to force C/CI, D/A and $\overline{\text{STAT}}$ to enable all DMA controller bus drivers and enable the PROM driven sequencer.

After the DMA controller has transferred the required data, it will relinquish control of the bus as follows:

1. DRQFF is reset by END at 02 trailing edge time. This indicates that the last data transfer for this DMA cycle has just taken place.

2. The DMA request to the processor ($\overline{\text{VIO- 7}}$) is removed. Upon receiving this, the processor immediately removes $\overline{\text{DMAGRANT}}$x and regains control of the bus.

4.2.3.3 Data Transfer Sequence

The data transfer timing is primarily controlled by a PROM driven sequencer. After the DMA controller has become bus master, the sequencer is enabled by D/A.   The sequencer will thus start at address :00 for a READ cycle or address :10 for a WRITE cycle.

The PROM address is incremented by the stored data in the PROM itself. Therefore, every time the register is clocked, new data is clocked out of the PROM and the PROM address is incremented to get the data ready for the next cycle.   The register is clocked by the trailing edge of the clock (either OB02 or bus 02, depending upon which processor the AM-600/T is to accommodate).

PSYNC is generated at address :01 or :11. The next clock pulse results in either PDBIN or $\overline{PWR}$ being generated. Subsequent clock pulses may be inhibited by the PRDY detect logic, thereby allowing slower data transfer to take place under control of PRDY.

After the data transfer has taken place, END is generated by the sequencer and is used to terminate the entire DMA cycle.

DMAWE is generated by sequencer during a WRITE cycle and is used to gate data onto the data bus to insure its validity before, during, and after PWR.

$\overline{ADRON}$ is also generated by the sequencer during a Read or Write cycle and is used in an optional configuration to multiplex the upper address bytes onto the data bus for use with the AM-700 Memory Partition Controller.

4.2.3.4 Processor Ready Detect Logic

PRDY is strobed at by the trailing edge of STVAL and latched. At this time, WAIT is set which suppresses the next update clock to the sequencer, thus introducing a WAIT state into the data transfer. As long as PRDY is false, the sequencer will not be clocked, thereby remaining in its original state.

4.2.4 DMA Address Generator/Byte Count Circuitry

The heart of the DMA address generator/byte counter is the AMD 2940 integrated circuit. A complete description of this IC is contained in Paragraph 4.3.1.

Three of these circuits are used in cascade to form a 24-bit address register and 24-bit byte counter. Under normal operation, the internal address, and the byte counter is loaded with the number of bytes to be transferred.

During each DMA write cycle, the address register drivers are enabled by signal D/A from the DMA sequence controller. At the end of each DMA transfer, the address register is incremented by END and the byte counter is decremented.

When the byte counter reaches zero, the DONEFF is set which signifies the completion of the transfer.

For a DMA read cycle, the address register operation is identical. However, the byte counter is set to zero initially and incremented each time the address register is incremented. Therefore, upon completion of the read command, the contents of the byte counter represent the block size of the data just read from tape.

Optionally, the upper address byte drivers can be multiplexed onto the DATA bus and used with the AM-700 Memory Partition Controller. In this configuration, $\overline{\text{ADRON}}$ from the DMA sequence controller enables the drivers just prior to the DMA sequence controller issuing a PSYNCI. This option is enabled by the MPC jumper on the AM-600/T. It must be used only in an AM-100/T based system with an AM-700 present.

4.2.5 Test Jumper Blocks and Test Points

Three test shorting block jumpers are provided on the board to facilitate initial testing and debug:

1. Clock Disable: Inserting this shorting block disables the on-board
   3 MHz clock. This is useful for initial testing in manufacturing
   using IN-CIRCUIT testing techniques.

2. Write Disable: Inserting this jumper prevents the AM-600/T from
   issuing any write strobes to memory during DMA transfers. This
   jumper is useful when debugging boards which malfunction by
   erroneously overwriting portions of the operating system.

3. Last Word Disable: Inserting this jumper suppresses the DONE
   signal, thereby allowing DMA transfers of infinite size, making it
   easier to examine DMA related timing signals.

In addition, test points are provided at the top of the board.

1. + 5 V
   Two +5 volt test points are provided to enable easy checks of the
   on-board regulators.

2. CLK

A clock test point is provided to allow easy examination of the on-board clock. If the CPU select jumper is set to "100", a 2 MHz bus clock signal should be present. If the CPU select jumper is set to "100T" or "100L" a 3 MHz clock signal should be present.

4.3 CIRCUIT MODULE DESCRIPTION

This section describes the operation of the individual circuit modules contained on the AM-600/T circuit board. Description of the control logic and interface modules are accompanied by logic and connection diagrams.

4.3.1 DMA Address Generator

(U41, U42, U43)

This device is a high-speed, eight-bit wide direct memory access address generator slice that can be cascaded to form larger addresses. Device connections are shown in Figure 4-4.

Logic Symbol   Connection Diagram
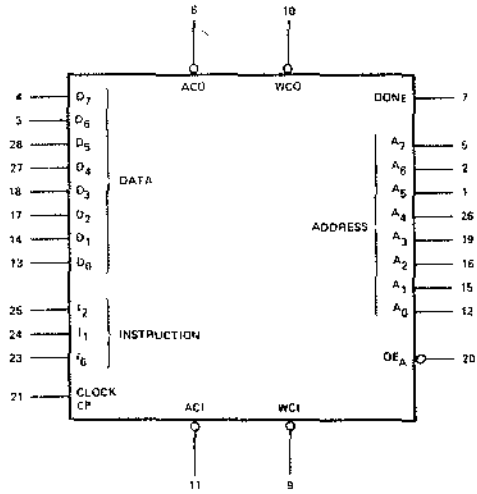
Top View
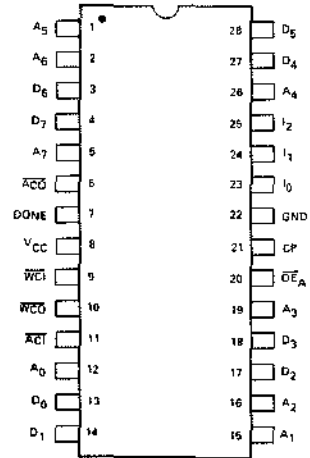
FIGURE 4-4.   DMA Address Generator Connections

The primary function of the device is to generate sequential memory addresses for use in the sequential transfer of data to or from a memory. It also maintains a data word count and generates a DONE signal when a programmable terminal count has been reached. The device is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential memory locations.

The device can be programmed to increment or decrement the memory address in any of four control modes and executes eight different instructions. The initial address and word count are saved internally so that they can be restored later in order to repeat the data transfer operation.

4.3.1.1 Architecture

As shown in Figure 4-5, the device consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- Three-state address output buffers with external output enable control.
- An instruction decoder.

Control Register.   Under instruction control, the Control Register can be loaded from the bidirectional DATA lines D0-D7. Control Register bits 0 and 1 determine the Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 4-5 defines the Control Register format and Figure 4-6 provides Control Register Format definitions.
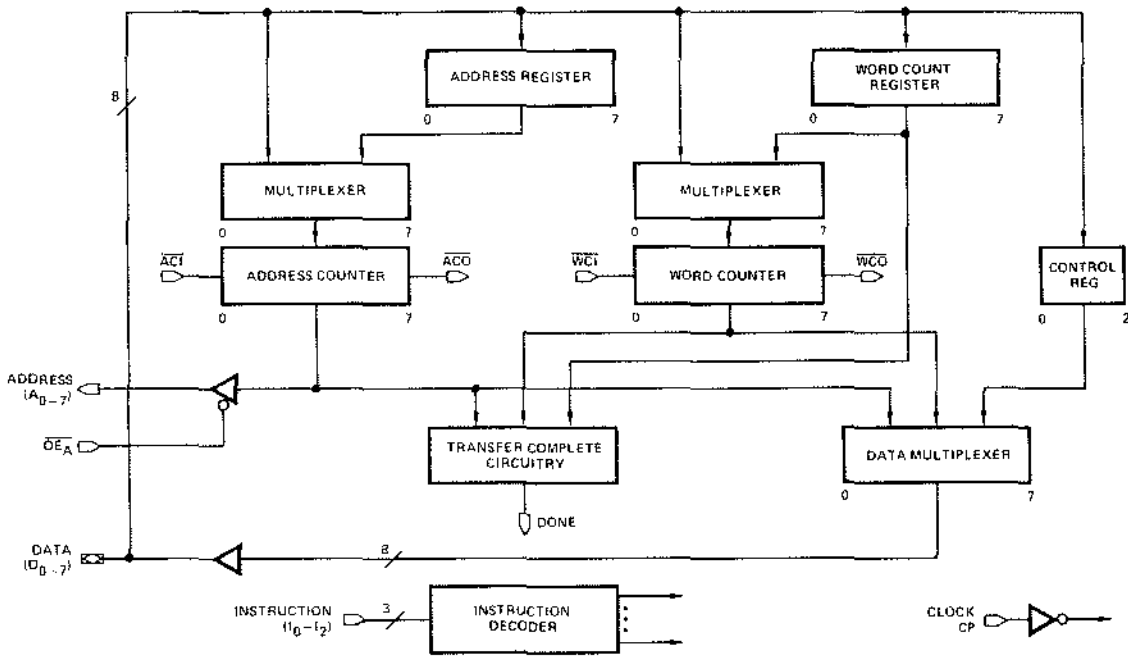
FIGURE 4-5. DMA Address Generator Block Diagram

Control Register

CR$_2$	CR$_1$	CR$_0$

CR$_1$	CR$_0$	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Hold	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

CR$_2$	Address Counter
L	Increment
H	Decrement

H = HIGH
L = LOW

FIGURE 4-6. Control Register Format

Address Counter. The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry input $(\overline{ACI})$ and Address Carry Output $(\overline{ACO})$ allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from DATA inputs, D0-D7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP. The Address Counter output can be enabled onto the three-state ADDRESS outputs A0-A7 under control of the Output Enable input, OEA.

Address Register. The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D0-D7.

Word Counter and Word Count Register. The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, decrements in Control Mode 0, and is disabled in Control Mode 2. The LOAD WORD COUNT instruction simulataneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry. The Transfer Complete Circuitry is a combinational loggic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is an open-collector output.

Data Multiplexer. The Data Multiplexer is an eight-bit wide, 3-input multiplexer which allows the Address Counter, Word Counter, and Control Register to be read at the DATA lines, D0-D7. The Data Multiplexer and three-state Data output buffers are instruction controlled.

Address Output Buffers.   The three-state Address Output Buffers allows
the Address Counter output to be enabled onto the ADDRESS Lines, A0-A7,
under external control.   When the Output Enable input, $\overline{OEA}$, is LOW, the
Address output buffers are enabled; when OEA is high, the ADDRESS lines are
in the sink 24mA output current over the commercial operating range.

Instruction Decoder.   The Instruction Decoder generates required internal
control signals as a function of the INSTRUCTION inputs, I0-I2 and Control
Register bits 0 and 1.

Clock.   The CLOCK input, CP is used to clock the Address Register,
Address Counter, Word Count Register, Word Counter, and Control Register,
all on the LOW to HIGH transition of the CP signal.

4.3.1.2 Control Modes

Control Mode 0 - Word Count Equals One Mode.   In this mode, the number of
data words to be transferred is initially loaded into the Word Counter and
Word Count Register.   When the Word Counter is enabled and the Word Counter
Carry-in, WCI, is LOW, the Word Counter decrements on the LOW to HIGH
transition of the CLOCK input, CP. The DONE signal is generated during the
last word transfer; i.e., when the Word Counter equals one.

Control Mode 1 - Word Count Compare Mode. Initially, the number of data
words to be transferred is loaded into the Word Count Register and the Word
Counter is cleared. When the Word Counter is enabled and the WCI input is
LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK
input, CP. In this mode, the Word Counter always indicates the number of
data words that have been transferred. The Transfer Complete Circuitry
compares the Word Counter with the Word Count Register and generates the
DONE signal during the last word transfer; i.e., when the Word Counter plus
one equals the Word Count Register.

Control Mode 2 - Address Compare Mode. In this mode, only an initial and final memory address need to be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the ACI input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer; i.e., when the Address Counter equals the Word Counter.

Control Mode 3 - Word Counter Carry Out Mode. For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

4.3.1.3 Instructions

The instruction set consists of eight instructions. Six instructions load and read the Address Counter, Word Counter and Control Register; one instruction enables the Address and Word counters; and one instruction reinitializes the Address and Word Counters. The function of the REINITIALIZE COUNTERS, LOAD WORD COUNT, and ENABLE COUNTERS instructions varies with the Control Mode being utilized. Table 4-3 defines the instructions as a function of instruction inputs I0-I2 and the four Control Modes.

TABLE 4-3. DMA Register Instructions

I_2 I_1 I_0	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D_0-D_7
L L L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	D_0-$D_2 \rightarrow$ CR	INPUT
L L H	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CR $\rightarrow D_0$-D_2 (Note 1)
L H L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WC $\rightarrow$ D
L H H	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	AC $\rightarrow$ D
H L L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WCR $\rightarrow$ WC	HOLD	AR $\rightarrow$ AC	HOLD	Z
				1	HOLD	ZERO $\rightarrow$ WC	HOLD	AR $\rightarrow$ AC	HOLD	Z
H L H	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D $\rightarrow$ AR	D $\rightarrow$ AC	HOLD	INPUT
H H L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D $\rightarrow$ WR	D $\rightarrow$ WC	HOLD	HOLD	HOLD	INPUT
				1	D $\rightarrow$ WR	ZERO $\rightarrow$ WC	HOLD	HOLD	HOLD	INPUT
H H H	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
				2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

CR = Control Reg.   WCR = Word Count Reg.   L = LOW
AR = Address Reg.   WC = Word Counter   H = HIGH
AC = Address Counter   D = Data   Z = High Impedance

Note 1:
Data Bits D_3-D_7 are high during this instruction.

WRITE CONTROL REGISTER. The WRITE CONTROL REGISTER instruction writes DATA input D0-D2 into the Control Register; DATA inputs D3-D7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register outputs to DATA lines, D0-D2. DATA lines D3-D7 are in the HIGH state during this instruction.

WORD COUNTER. The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter outputs to DATA Lines DO-D7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs DO-D7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs DO-D7 are written into the Word Count Register and the Word Counter is cleared.

READ ADDRESS COUNTER. The READ ADDRESS COUNTER instruction gates the Address Counter outputs to DATA Lines DO-D7, and the LOAD ADDRESS instruction writes DATA inputs DO-D7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

REINITIALIZE COUNTERS. The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA Lines.

4.3.2 Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear

(U1, U5, U8, U13)

For logic and connections, see Figure 4-7.
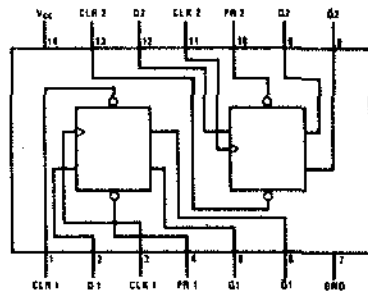
TRUTH TABLE

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	Q̄0

Notes. ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse

Q0 = the level of Q before the indicated input conditions were established.

TOGGLE Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

FIGURE 4-7. Dual D Flip-Flop Connections

4.3.3 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

(U16, U18)

For device logic and connections, see Figure 4-8.

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	Q̄0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	Q̄0
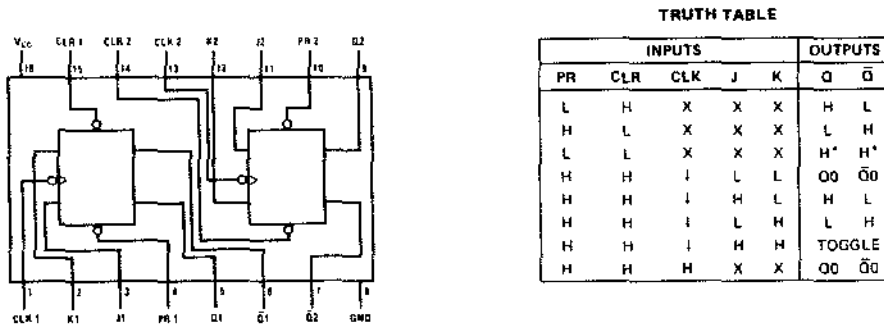
Notes.   Q0 = the level of Q before the indicated input conditions were established.
         TOGGLE. Each output changes to the complement of its previous level on each active transition of the clock.
         *This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

FIGURE 4-8.   J-K Flip-Flop Connections

4.3.4 Decoder

(U46,U47)

These are Schottky-clamped circuits designed for memory-decoding or data-routing applications requiring very short propagation delay times. This DIP decodes one of eight lines based on the conditions at the three binary select inputs and the three enable inputs. For logic and connections, see Figure 4-9.

Connection Diagram
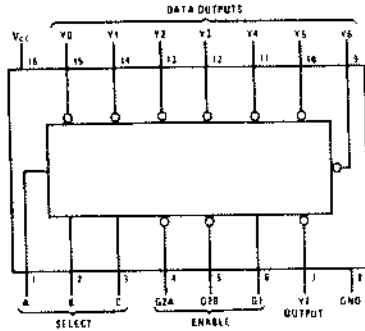
Truth Table

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Logic Diagram
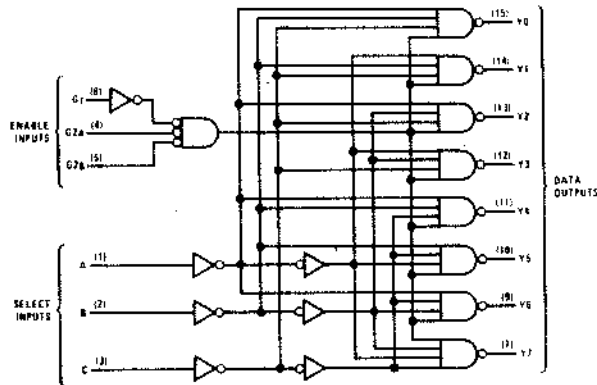
FIGURE 4-9. Decoder Connections

4.3.5 Inverting Octal Bus Driver

(U14, U29, U37, U44, U49, U50, U51, U52, U64)
These buffers provide the drive capability for tri-state bus requirements
and are inverting. For logic and connections, see Figure 4-10.
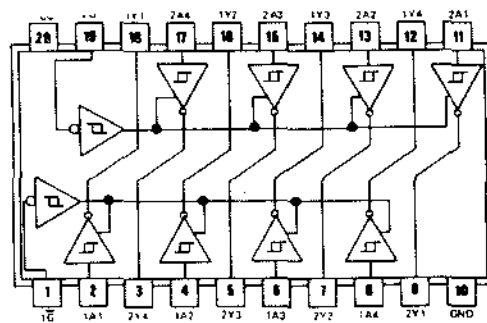
FIGURE 4-10. Inverting Bus Driver Connections

4.3.6 Noninverting Octal Bus Driver

(U25, U27, U28, U56, U57, U58, U59, U60,U61, U62, U63, U65)
These buffers provide the drive capability for tri-state bus requirements
and are noninverting. For logic and connections, see Figure 4-11.
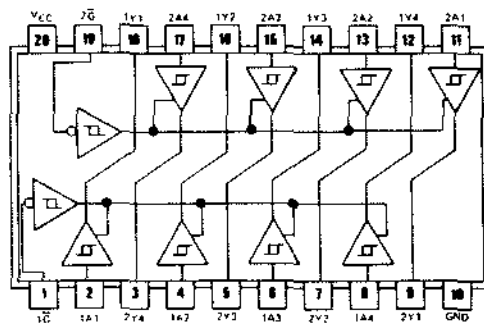
FIGURE 4-11. Non-Inverting Bus Driver Connections

4.3.7 Octal D Register With Reset

(U40, U36)

This register consists of positive-edge-triggered D-type flip-flops with a direct clear input. Information at the D inputs is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. For device connections and logic, see Figure 4-12.

Connection Diagram
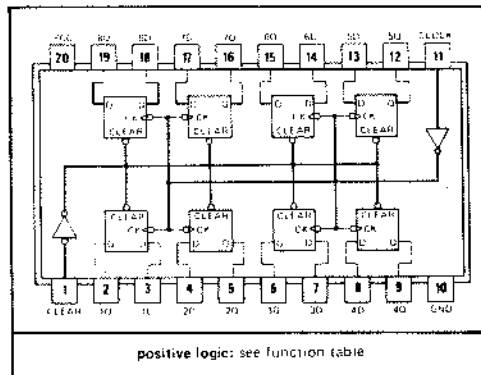
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

positive logic: see function table

Logic Diagram
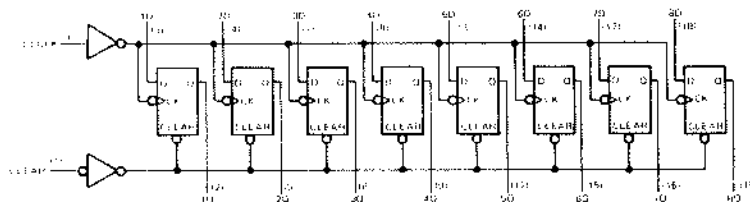
FIGURE 4-12. Octal D Register Connections

DWM-00607-00 REV A00

4.3.8 Set-Reset Latches

(U45)

These latches provide temporary storage of binary information between processing components. When either one of the data inputs is at a low logic level, the output follows the level of the R input. When both data inputs are high, the output remains latched in its previous state. When both inputs are low, the output goes high. However, this high level may not persist when either one of the data inputs returns to the high state. For logic connections, see Figure 4-13.

Logic and Connections
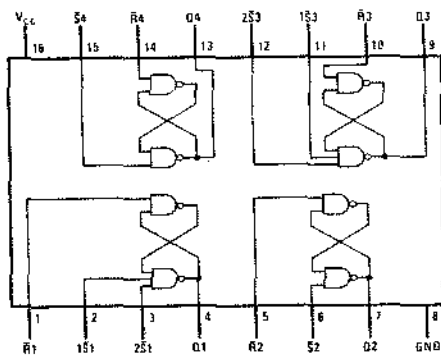
Truth Table

INPUTS		OUTPUT
S1	$\overline{R}$	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H*

H = High Level
L = Low Level
Q_0 = The level of Q before the indicated input conditions were established.
* This output level is pseudo stable that is, it may not persist when the S and R inputs return to their inactive (high) level.
† For latches with double $\overline{S}$ inputs:
    H = both $\overline{S}$ inputs high
    L = one or both $\overline{S}$ inputs low

FIGURE 4-13. Octal D Register Connections

4.3.9 Bipolar PROM

(U24)

This PROM is organized in the 32 word by eight bit configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.   If the enable input is raised to a high level, all eight outputs go to the OFF level or high impedance state. This device produces tri-state outputs. For logic and connections, see Figure 4-14.

Block Diagram

Connection Diagram

Vcc = Pin 16
GND = Pin 8

Note: Pin 1 is marked for orientation.

Logic Symbol
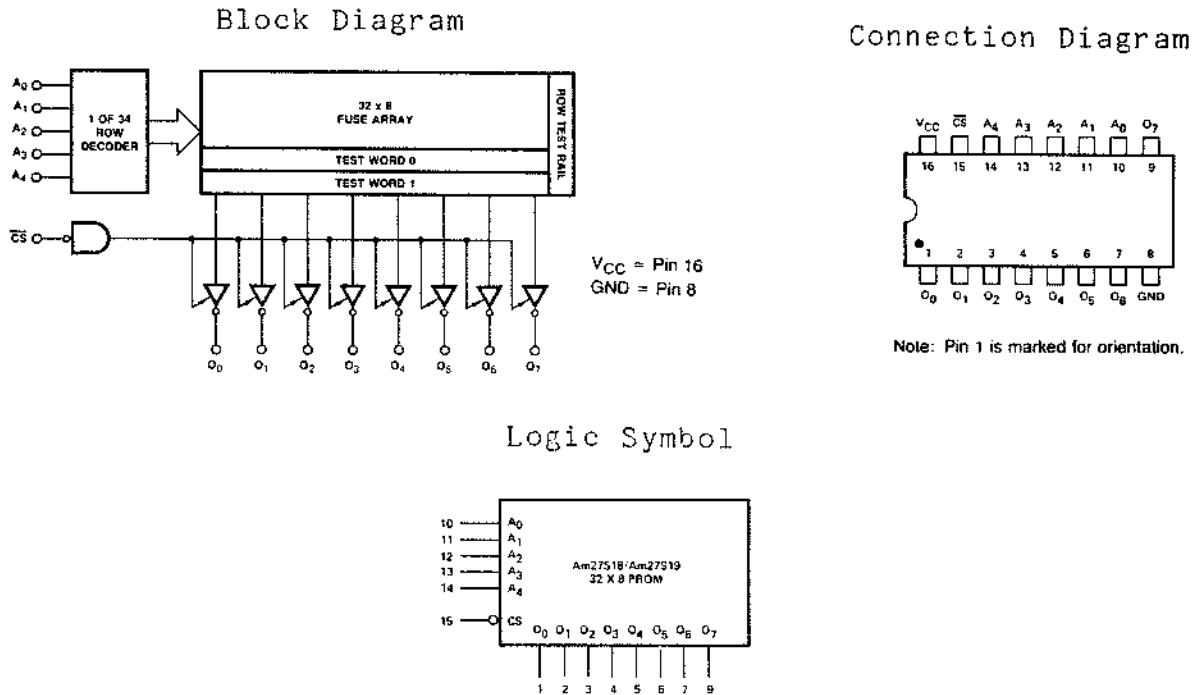
FIGURE 4-14.   Bipolar PROM Connections

4.3.10 Tri-State D Flip-Flops

(U31, U32, U33,)

These 8-bit registers contain D-Type flip-flops with totem-pole tri-state outputs capable of driving highly capacitive or low impedance loads. When the output control is taken to a high logic level, the outputs go into the high impedance state. When a low logic level is applied to the output control, data at the D inputs are loaded into their respective flip-flops on the next positive-going transition of the clock. For logic and connections, see Figure 4-15.
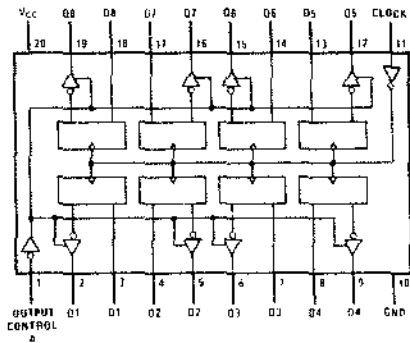
Connection Diagram   Logic Diagram
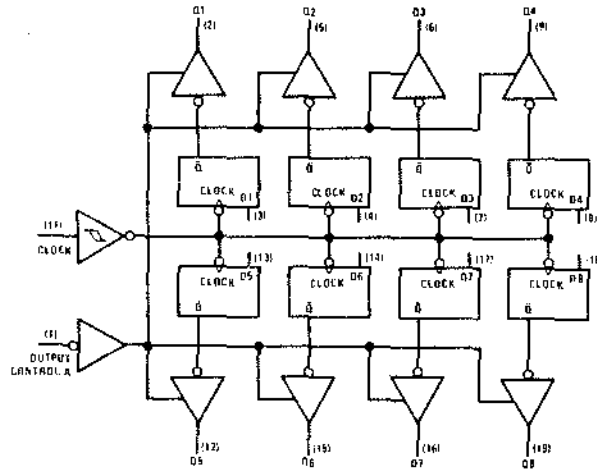
Truth Table

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	↓	X	Q0
H	X	X	Z

FIGURE 4-15. Tri-State D Flip-Flop Connections

4.3.11 Bus Comparator

(U53)

This device compares two binary words of two to six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are TTL inputs, whereas inputs of the second word are high impedance receivers driven by a terminated data bus. The output has a latch that is strobe controlled. The transfer of information to the output occurs when the

STROBE input goes from a logical 1 to a logical 0 state. Inputs may be changed while the STROBE is at the logical 1 level, without affecting the state of the output. Logic and connections are shown in Figure 4-16.

Logic Diagram

Connection Diagram

Truth Table

CONDITION	STROBE	OUTPUT	
		DM71/8131	DM71/8136
T B 1 ≠ B	H	Q_{n-1} *	Q_{n-1} *
T · B	L	L	H
T ≠ B	L	H	L

*Latched in previous state
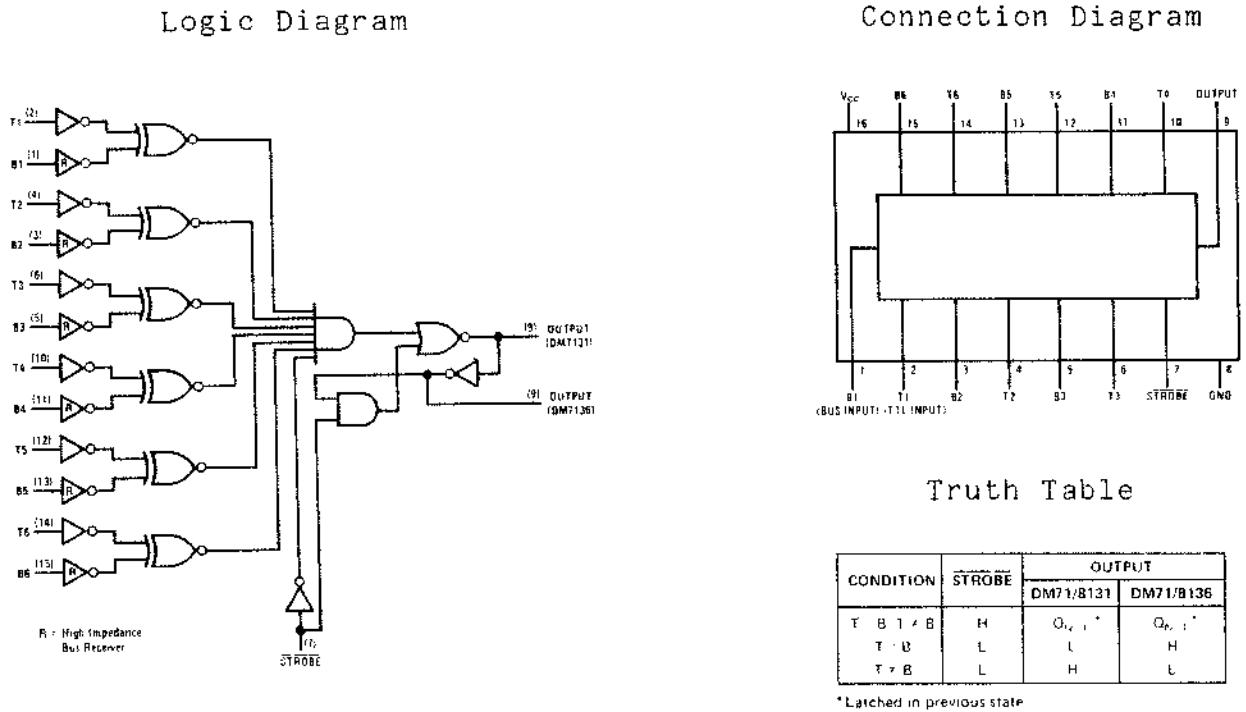
FIGURE 4-16. Bus Comparator Connections

4.3.12 Four-Phase Clock Generator

(U35)

This device consists of an oscillator, divide-by-four counter, a second divide-by-four counter with gating to generate four clock pulses, high level (12-volt) output drivers, low level (5-volt) complementary output drivers, and a D-type flip-flop controlled by an external signal and the 03 clock. For logic and connections, reference Figure 4-17.
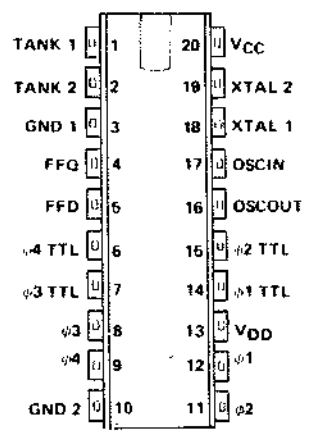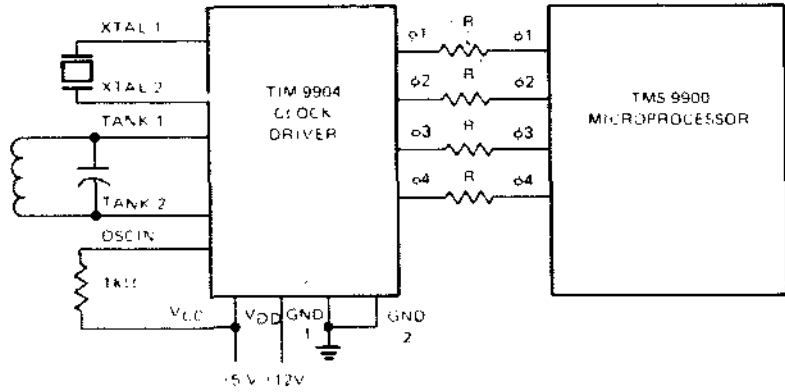
FIGURE 4-17. Four-Phase Clock Logic and Connections

CHAPTER 5

MAINTENANCE AND TROUBLESHOOTING

5.1 INTRODUCTION

The AM-600/T circuit board performs to full capability with a minimum of
maintenance.   This chapter describes maintenance and troubleshooting
procedures and the procedure for handling warranty returns.

5.2 CIRCUIT BOARD CHECKOUT

The AM-600/T circuit board was fully tested before it   left   Alpha
Microsystems and will operate satisfactorily in the system if the hardware
and software requirements of Chapters Two and Three of this manual are met.
Should a problem arisee after the circuit card has been in operation, use the
following procedures to identify and locate the fault:

1. Check all cabling for proper seating of connectors.

2. Check the circuit board for proper seating in the slot.

3. Check jumper options to ensure correctness of application.

4. Check all power connections for proper seating in the slot.

5. Verify that the fault is in the AM-600/T and not either in the system or in the peripherals. This can best be accomplished with substitution of a known good circuit board.

6. Contact the Alpha Micro Technical Services Group for information on diagnotic test availability.

5.3 WARRANTY PROCEDURES

This circuit board is covered by warranty issued by Alpha Microsystems Inc., Irvine, California. Complete details of the warranty are included with the circuit board. Should a problem arise with this circuit board, call your dealer or the Alpha Micro Technical Services Group for information.

CHAPTER 6

COMPONENT CROSS REFERENCE LIST

Component Cross Reference List (sheet 1 of 2)

REF. DESIG.	MFR. TYPE NO.	PAR. NO.	REF. DESIG.	MFR. TYPE NO.	PAR. NO.
U1	74LS74	4.3.2	U13	74LS74	4.3.2
U2	74LS00		U14	74LS240	4.3.5
U3	74LS32		U15	74LS08	
U4	74LS08		U16	74LS112	4.3.3
U5	74KS740	4.3.2	U17	7438	
U6	74LS10		U18	74LS112	4.3.3
U7	SPARE		U19	74LS32	
U8	74LS74	4.3.2	U20	74LS08	
U9	4LS00		U21	74LS32	
U10	74LS32		U22	314E221331	
U11	74LS08		U23	314E221331	
U12	4LS00		U24	DWB0060202	4.3.9

Component Cross Reference List (sheet 2 of 2)

REF. DESIG.	MFR. TYPE NO.	PAR. NO.	REF. DESIG.	MFR. TYPE NO.	PAR. NO.
U25	74LS244	4.3.6	U51	74LS240	4.3.5
U26			U52	74LS240	4.3.5
U27	74LS244	4.3.6	U53	8131N/A+	4.3.11
U28	74LS244	4.3.6	U54	74LS10	
U29	74LS240	4.3.5	U55	7416	
U30	74LS373		U56	74LS32	4.3.6
U31	74LS374	4.3.10	U57	74LS244	4.3.6
U32	74LS374	4.3.10	U58	74LS244	4.3.6
U33	74LS374	4.3.10	U59	74LS244	4.3.6
U34	74LS02		U60	74LS244	4.3.6
U35	9904ANL	4.3.12	U61	74LS244	4.3.6
U36	74LS273	4.3.7	U62	74LS24	4.3.6
U37	74LS240	4.3.5	U63	74LS24	4.3.6
U38	SPARE		U64	74LS240	4.3.5
U39	74LS32		U65	74LS24	4.3.6
U40	74L273	4.3.7			
U41	2940	4.3.1			
U42	2940	4.3.1			
U43	2940	4.3.1			
U44	74LS240	4.3.5			
U45	74LS279	4.3.8			
U46	74LS138				
U47	74LS138				
U48	DWB0060501				
U49	74LS240	4.3.5			
U50	74LS240	4.3.5			

APPENDIX A

PARTS LIST

```
......ASSEMBLY....................        ..............COMPONENT.........................  ASSY.
NUMBER    DESCRIPTION                REC# NUMBER   DESCRIPTION                         BIN#   QUANTITY
```

DWB0060700 ASSY MAG TAPE INTERFACE AM-600/T   A04 01274

REC#	NUMBER	DESCRIPTION	ASSY. BIN#	QUANTITY
00001	DWF0060700	PCB DETAIL AM-600/T		1.000
00002	CNF0000211	HEADER,MALE,50PIN,R/A,4 WALL,BOX		2.000
00003	CNS0001600	SOCKET 16 PIN DIP		1.000
00004	CNS0002000	SOCKET 20 PIN DIP		2.000
00005	CNS0002800	SOCKET 28 PIN DIP		3.000
00006	CPN0047001	CAPACITOR, 47PF,10%,200V,CERAMIC		1.000
00007	CPN0047401	CAPACITOR, .47UF,20%, 50V,CERAMIC		30.000
00008	CPP0015601	CAPACITOR 15 UF 20V		4.000
00009	DWB0001102	CAP/RES NET 100 PF, 220 OHM, 10 PIN		3.000
00010	DWB0060202	CONTROL PROM, 16 BIT COMP AM-600		1.000
00011	DWB0060501	ASSY DMA BUS ARBITRATOR S-100 BUS		1.000
00012	CRY0000600	CRYSTAL, 12 MHZ		1.000
00013	CNF0003800	HEADER MALE, 6PIN,DBL ROW,STR,.1"C.		3.000
00014	CNF0003302	HEADER MALE, 2PIN,SGL ROW,STR,.1"C.		3.000
00015	CNA0000600	CONN RECEPTACLE SHORTING 2CONT BLK		3.000
00016	HDM0001200	THERMAL GREASE	F/S	0.000
00017	HDM0002100	HEAT SINK 1.4 WI .5 HT 1.880L		2.000
00018	HDS5000106	SCREW, 6-32 X .375 TRUSS HD,PHIL,SS	F/S	4.000
00019	HDN1000006	NUT HEX 6-32 KEP INT/EXT CAD STL	F/S	4.000
00020	HDW1000406	NYLON SHOULDER WASHER #6	F/S	4.000
00021	ICL0032300	IC REGULATOR +5V TO-3		2.000
00022	IC17413801	IC DECODER 3 TO 8 LINE		2.000
00023	IC17424401	IC OCTAL BUS DRIVER NONINVERT		12.000
00024	IC17424001	IC OCTAL BUS DRIVER INVERTING		9.000
00025	IC10813100	IC COMPARATOR 6 BIT		1.000
00026	IC10747401	IC DUAL D FLIPFLOP		4.000
00027	IC10740801	IC QUAD 2 INPUT AND GATE		5.000
00028	IC10743201	IC QUAD 2 INPUT OR GATE		4.000
00029	IC17437401	IC OCTAL D FLIPFLOP, TRI-STATE		3.000
00030	IC17427301	IC OCTAL D REGISTER W/RESET		2.000
00031	IC10740001	IC QUAD 2 INPUT NAND GATE		3.000
00032	IC10741001	IC TRIPLE 3 INPUT NAND GATE		2.000
00033	IC17411201	IC DUAL J-K NEGATIVE FLIPFLOP		2.000
00034	IC17427901	IC QUAD S-R LATCHES		1.000
00035	IC10741600	IC HEX INVERTER /DRIVER OC		1.000
00036	IC17437301	IC OCTAL D FLIPFLOP, TRI-STATE		1.000
00037	IC10743800	IC QUAD 2 INPUT NAND DRIVER OC		1.000
00038	ICS0294000	IC DMA ADDRESS GENERATOR		3.000
00039	ICS0990400	IC, CLOCK GEN, 4 PHASE		1.000
00040	RS20010300	RESISTOR 10 K 1/4W 5% CAR		10.000
00041	RS20010200	RESISTOR 1 K 1/4W 5% CAR		3.000
00042	RS20047100	RESISTOR 470 OHM 1/4W 5% CAR		2.000
00043	RSN0000300	RES.NETWK,14PIN,DIP,24RES, 220/330		2.000
00044	IND0000600	INDUCTOR, 3.3 UH		1.000
00045	CBW0002420	WIRE,BUS,24AWG,SINGLE STRAND,TYP.S		0.000
00046	IC10740201	IC QUAD 2 INPUT NOR GATE		1.000
00047	DWL0060700	SCHEMATIC MAG TAPE I/F AM-600/T		0.000
00048	LBL0001828	LABEL, PCB SERIAL I.D. AM-600/T		1.000

APPENDIX B

SCHEMATICS

8 7 6 5 4 3 2 1

LTR	DATE	DESCRIPTION	
AP1		ENGINEERING RELEASE	
A00		RELEASE PER ENG1336	
A01	7/18/78	INCORP PER EN-0223	
A02	11-11-81	INCORP PER EN-0515	
A03	9-13-93	REVISE PER ECO 1206	
A04		REVISE PER ENO1274	

J1

+7.5V 1
+7.5V 51

+5V1 TP
U66 7805 TO3
+5V1

15µf 20V C36   .47 C35

15µf 20V C27   .47 C26   .47-15 PLCS
C1,2,3,4,5,6,7,8,9,10,11,12,13,14,15

+5V2 TP
U26 7805 TO3
+5V2

15µf 20V C25   .47 C24

15µf 20V C19   .47 C18   .47-11 PLCS
C20,21,22,23,28,29,30,31,32,33,34

GND TP

GND 20
GND 50
GND 70
GND 100

SPARES

LS08   LS00   LS240   7438   LS32
LS00   LS08
LS10   LS240   LS02   LS240   7416   LS240
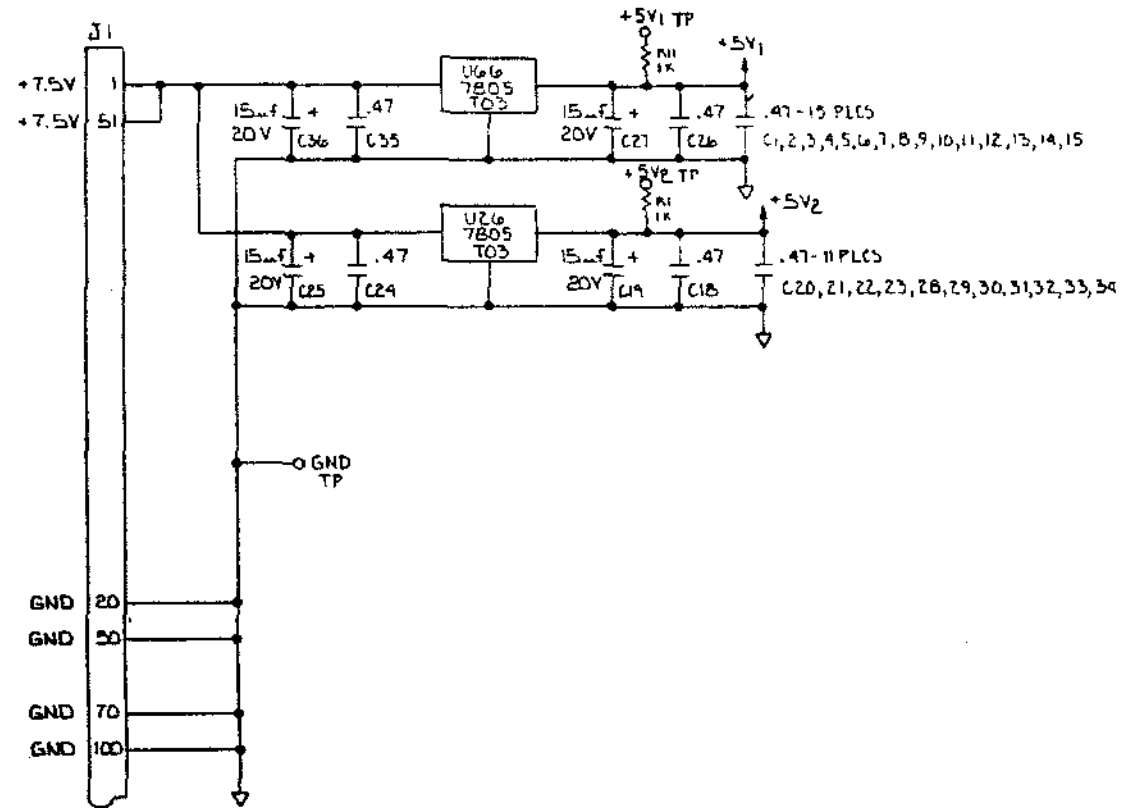
VOLTAGE AND GROUND CHART
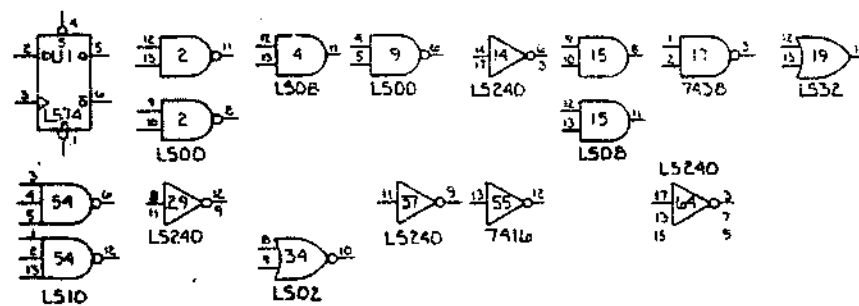
REFERENCE DESIGNATIONS					
LAST USED	NOT USED
C36	C17
CY1	
R15	
PN3	
U66	
L1	

+5V1	+5V2		GND	IC REFERENCE DESIGNATIONS
14			7	U39,55,59
16			8	U45,46,47,53
20			10	U38,40,44,48,49,50,51,52, 56,57,58,59,60,61,62,63,64,65
8			22	U41,42,43
	14		7	U1,2,3,4,5,6,7,8,9,10,11,12,13,15,17,19,20,21,22,23,34
	16		8	U16,18,24
	20		10	U14,27,28,29,30,31,32,33,35,36,37,25
	8		22	U41,42,43

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES ARE IN OHMS ±5% 1/4 WATT.
2. CAPACITOR VALUES ARE IN MICROFARADS ±20% 50 VOLTS
3. J2 GROUND PINS: ALL ODD PINS, EXCEPT PIN 45.
4. J3 GROUND PINS: ALL ODD PINS, EXCEPT PINS 1,3 AND 25.
5. THE FIRST DIGIT OF ALL ZONE REFERENCES IS THE SHEET NO.
EXAMPLE: (3C5) = SHEET 3 ZONE C5.

alpha micro

TITLE SCHEMATIC, MAG TAPE INTERFACE, AM-600/T

D   DWG NO   DWL-00607 00   A-4

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