TECHNICAL MANUAL FOR

AM-200

FLOPPY DISK CONTROLLER CIRCUIT BOARD

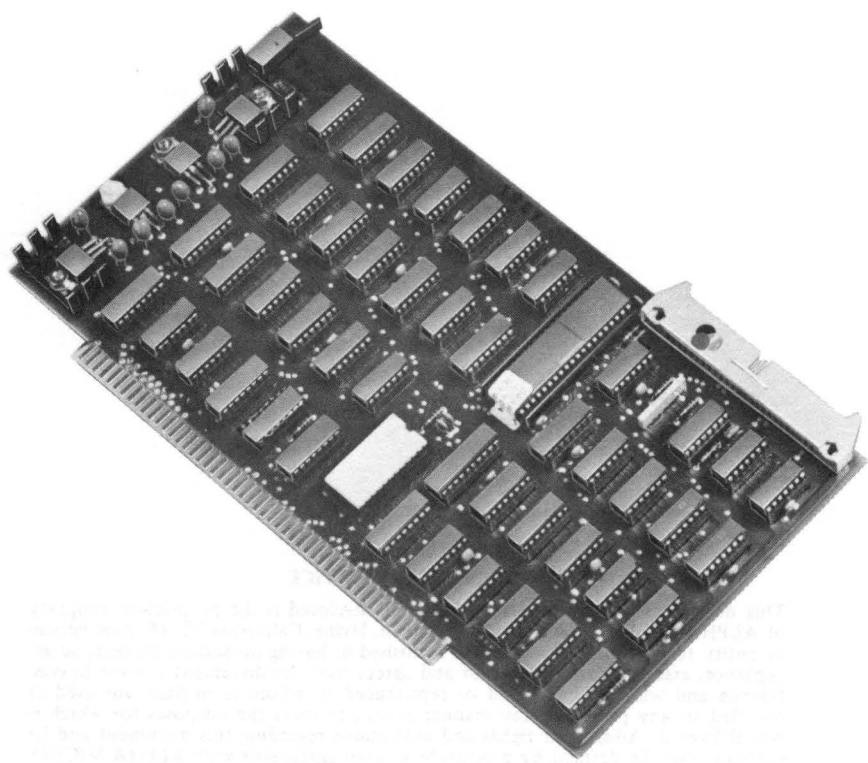
DWM–00200–00

alpha micro

TECHNICAL MANUAL FOR

AM-200

FLOPPY DISK CONTROLLER CIRCUIT BOARD



Manufactured By

ALPHA MICROSYSTEMS
17881 SKY PARK NORTH
IRVINE, CALIFORNIA 92714

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont.)

LIST OF TABLES

USER COMMENTS

TECHNICAL PUBLICATIONS FILE REFERENCE

FROM: NAME _____

_____

ADDRESS _____

CITY _____

STATE _____ ZIP _____

NOTE: Use this form to communicate any errors, suggested changes, or general comments about this document.

If necessary, call us at:

(714) 957-6076

DOCUMENT: TITLE/NUMBER/REVISION _____

_____

COMMENTS:

FOLD, STAPLE & MAIL

STAPLE

STAPLE

FOLD

FOLD

PLACE
STAMP
HERE

CUT ALONG LINE

17881 Sky Park North
Irvine, California
92714

ATTN: EDUCATIONAL SERVICES DIVISION

FOLD

FOLD

SECTION 1
GENERAL DESCRIPTION

1.0 INTRODUCTION.

This manual provides operating and maintenance instructions for the AM-200 Floppy Disk Controller Circuit Board manufactured by Alpha Microsystems located in Irvine, California. Circuit board description, operating and usage instructions, programming, theory of operation, and maintenance instructions are included to provide the user with the information necessary to utilize this circuit board to its full capability.

1.1 CIRCUIT BOARD DESCRIPTION.

The AM-200 Floppy Disk Controller circuit board is an S-100 bus compatible DMA floppy disk controller based on the Western Digital FD 1771 control DIP. It provides full or partial sector reading from the drive and has multiple drive control and multi-level interrupt capabilities. An 8K PROM is contained on the board to provide a bootstrap load program for the floppy disk subsystem.

A simplified block diagram of the circuit board is shown in Figure 1-1. For a complete detailed description of circuit board operation, see Section 4 of this manual.

1.2 APPLICATION.

This circuit board provides the data processing necessary for control and operation of most popular single density floppy disk drives in an S-100 bus system. The AM-200 requires separate clock and data inputs and provides outputs for step-direction drives. See Section 2 of this manual for wiring instructions and system interface information.

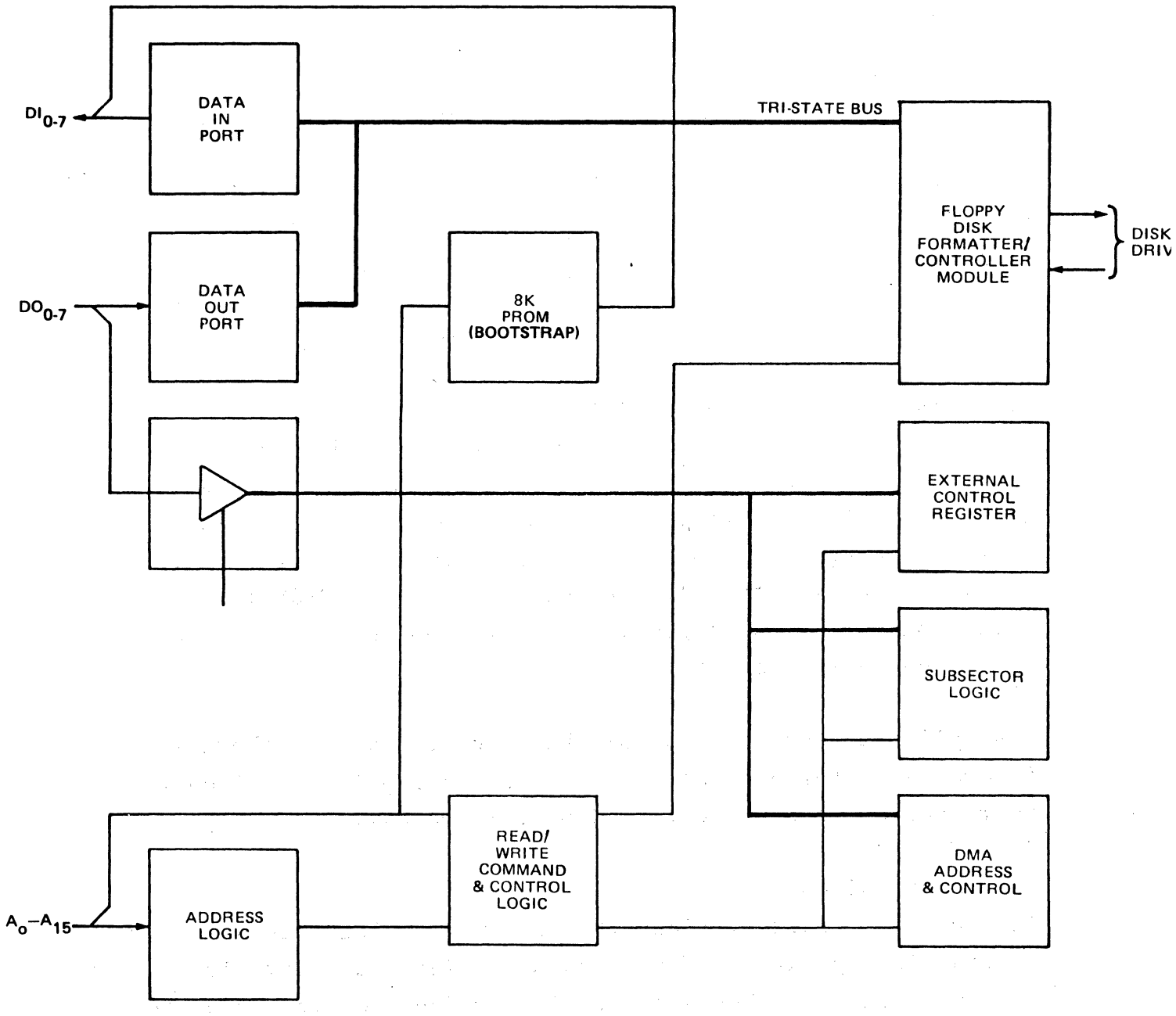


Figure 1-1. AM-200 Simplified Block Diagram

SECTION 2
OPERATING DATA

2.0 INTRODUCTION.

This section contains information on the use of the AM-200 Floppy Disk Controller Board. Capabilities, specifications, interface wiring and user option descriptions are provided for the successful integration of the board into the user's system.

2.1 CAPABILITIES AND SPECIFICATIONS.

This circuit board operates from the standard S-100 bus structure and provides interface capability to most popular single density floppy disk drives. It is a DMA device for transfer of data between a floppy disk drive and system memory under CPU control. Specifications for the AM-200 circuit board are contained in Table 2-1.

Table 2-1. AM-200 Specifications

Parameter	Specifications
Interface	S-100 Bus for CPU, a maximum of four floppy disk drives with separate clock and data inputs and with step-direction head positioning.
Bootstrap Program	Eight by 1024 bit PROM which contains bootstrap program.
Interrupts	Multiple level interrupt capability - user selected.
DMA Access	Multiple level direct memory access - user selected.
Data Transfer	Full DMA transfer of data between floppy drive and system memories.
Sector Read	Full or partial sector read from floppy drive.
Circuit Board	Standard 5" x 10" with 100 pin connector.

2.2 INTERFACE DESCRIPTION AND WIRING.

The AM-200 Floppy Disk Controller provides interface capability between the standard S-100 bus and floppy disk drives.

2.2.1 S-100 BUS INTERFACE.

The AM-200 circuit board is fully S-100 bus compatible. The board and its associated floppy disk drives are addressed through the address lines and data is transferred through the standard data in and data out lines. The S-100 bus connections are made via the bottom edge connector and are described in Table 2-2.

2.2.2 FLOPPY DRIVE INTERFACE.

The AM-200 Floppy Disk controller accommodates a maximum of four floppy disk drives. Most of the popular drives are compatible if they provide outputs of separate clock and data and require step-direction head control. All floppy disk drive interface signals are described in Table 2-3.

Table 2-2. S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
$\overline{\text{ADDSBL}}$	Address Disable	22	AM-200 output to disconnect CPU address lines from S-100 bus.
A0	Address 0	79	16 Bits of S-100 Addressing.
A1	Address 1	80	
A2	Address 2	81	
A3	Address 3	31	
A4	Address 4	30	
A5	Address 5	29	
A6	Address 6	82	

Table 2-2 (Cont.). S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
A7	Address 7	83	16 Bits of S-100 Addressing.
A8	Address 8	84	
A9	Address 9	34	
A10	Address 10	37	
A11	Address 11	87	
A12	Address 12	33	
A13	Address 13	85	
A14	Address 14	86	
A15	Address 15	32	
$\overline{\text{CCDSBL}}$	Control Disable	19	AM-200 output to disconnect CPU control lines from S-100 bus.
DATAIN 0	Input Data Bit 0	95	Data Input Port. Bus Master Input From Slaves.
DATAIN 1	Input Data Bit 1	94	
DATAIN 2	Input Data Bit 2	41	
DATAIN 3	Input Data Bit 3	42	
DATAIN 4	Input Data Bit 4	91	
DATAIN 5	Input Data Bit 5	92	
DATAIN 6	Input Data Bit 6	93	
DATAIN 7	Input Data Bit 7	43	
DATAOUT 0	Output Data Bit 0	36	Data Output Port. Bus Master Output To Slaves.
DATAOUT 1	Output Data Bit 1	35	
DATAOUT 2	Output Data Bit 2	88	
DATAOUT 3	Output Data Bit 3	89	
DATAOUT 4	Output Data Bit 4	38	
DATAOUT 5	Output Data Bit 5	39	
DATAOUT 6	Output Data Bit 6	40	
DATAOUT 7	Output Data Bit 7	90	

Table 2-2 (Cont.). S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
$\overline{\text{DMAGRANT}}$ 0	Direct Memory Access Grant 0	63	Input from CPU indicating bus control has been relinquished to one of 8 DMA controllers. Any one of 8 is selectable by jumper on AM-200 board. Normal level is 6 for floppy controller.
$\overline{\text{DMAGRANT}}$ 1	Direct Memory Access Grant 1	62	
$\overline{\text{DMAGRANT}}$ 2	Direct Memory Access Grant 2	61	
$\overline{\text{DMAGRANT}}$ 3	Direct Memory Access Grant 3	60	
$\overline{\text{DMAGRANT}}$ 4	Direct Memory Access Grant 4	59	
$\overline{\text{DMAGRANT}}$ 5	Direct Memory Access Grant 5	58	
$\overline{\text{DMAGRANT}}$ 6	Direct Memory Access Grant 6	57	
$\overline{\text{DMAGRANT}}$ 7	Direct Memory Access Grant 7	56	
$\overline{\text{DMARCVD}}$	DMA Received	64	DMA acknowledge signal from CPU, jumper selectable on AM-200 board. Signal indicates DMAGRANT is coming the next cycle.
$\overline{\text{DODSBL}}$	Data Out Disable	23	AM-200 output to disconnect CPU data lines from S-100 bus.
PDBIN	Data Bus In	78	Read enable. Used by bus master to request addressed slave to place data on input port.

Table 2-2 (Cont.). S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
PHLDA	Halt Acknowledge	26	AM-200 input, jumper selectable. Indicates that the CPU has halted and its output lines are disconnected from the bus.
$\overline{\text{PHOLD}}$	CPU Halt	74	Halts the CPU for Direct Memory Access control (Jumper Selectable).
$\overline{\text{PINT}}$	Interrupt Request	73	($\overline{\text{INTREQ}}$) Jumper selectable interrupt request output.
PINTE	Interrupt Enable	28	(INTE) AM-200 output to hold Interrupt Enable bus signal low during DMA.
PRDY	Ready	72	AM-200 I/O signal to allow extensions of bus timing.
PSYNC	Sync	76	Indicates the beginning of each bus transfer cycle.
PWAIT	Wait	27	Acknowledges that the CPU has stopped.
$\overline{\text{PWR}}$	Write Strobe	77	Write strobe. Generated by bus masters as write command to slaves.
$\overline{\text{RESET}}$	Reset	75	AM-200 Reset input.

Table 2-2 (Cont.). S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
SHLTA	Halt	48	(HLTA) AM-200 output to hold Halt acknowledge bus signal low during DMA.
SINP	I/O Input Cycle	46	AM-200 I/O signal indicating I/O input operation.
SINTA	Interrupt Acknowledge	96	(INTA) AM-200 output to hold SINTA bus signal low during DMA.
SMEMR	Memory Read Cycle	47	AM-200 I/O signal indicating memory read operation.
SMI	Memory Instruction Fetch Cycle	44	AM-200 output to hold SMI bus signal low during DMA.
SOUT	I/O Output Cycle	45	AM-200 I/O signal indicating I/O output operation.
SSTACK	Stack Operation	98	AM-200 output to hold SSTACK bus signal low during DMA.
STDSBL	Status Disable	18	AM-200 output to disconnect CPU status lines from S-100 bus.
$\overline{\text{SWO}}$	Write Cycle	97	AM-200 I/O signal indicating output operation.

Table 2-2 (Cont.). S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
$\overline{VI0}$ $\overline{VI1}$ $\overline{VI2}$ $\overline{VI3}$ $\overline{VI4}$ $\overline{VI5}$ $\overline{VI6}$ $\overline{VI7}$	Interrupt 0 Interrupt 1 Interrupt 2 Interrupt 3 Interrupt 4 Interrupt 5 Interrupt 6 Interrupt 7	4 5 6 7 8 9 10 11	Jumper selected Interrupts. Used for both interrupt requests and DMA requests. Normal configuration: VI6 used for DMA request.
Ø2	Phase 2 clock	24	Phase 2 clock from cpu.
+8VDC	+8VDC	1,51	+8V power.
+16VDC	+16VDC	2,52	+16 power.
GND	Ground	50, 100	System Ground

Table 2-3. AM-200 Floppy Disk Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
$\overline{DS1L}$	Drive Select 1 Left Rtn	26 25	Low level output loads and selects Head 0 (The left-side head) of drive 1.
$\overline{DS1R}$	Drive Select 1 Right Rtn	28 27	Low level output loads and selects Head 1 (the right-side head) of drive 1.
$\overline{DS2L}$	Drive Select 2 Left Rtn	18 17	Low level output loads and selects Head 0 (the left-side head) of drive 2.

Table 2-3 (Cont.) AM-200 Floppy Disk Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
$\overline{\text{DS2R}}$	Drive Select 2 Right Rtn	4 3	Low level output loads and selects Head 1 (the right-side head) of drive 2.
$\overline{\text{INDEX}}$	Disk Index 0 Rtn	20 19	AM-200 input. One ms negative going pulse occurs for each revolution of the selected disk.
$\overline{\text{INDEX 1}}$	Disk Index 1 Rtn	8 7	AM-200 input. Optional index pulse. (No connection in AM-200).
$\overline{\text{INWARDS}}$	Direction Select Rtn	34 33	AM-200 output. Defines direction of motion of the head positioner when the step line is pulsed. Low = inward (higher track number). High = outward (lower track number - away from center).
$\overline{\text{READ DATA}}$	Disk Output Data Rtn	46 45	AM-200 input. Data output of selected head. Each flux transition = 200 ns pulse active low. (No connection in AM-200.)
$\overline{\text{READY}}$	Ready 0 Rtn	22 21	AM-200 input. A low level indicates that a diskette is loaded in selected drive and is within 90% of its operating speed.

Table 2-3 (Cont.). AM-200 Floppy Disk Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
$\overline{\text{READY 1}}$	Ready 1 Rtn	6 5	AM-200 input. Optional ready signal. (No connection in AM-200.)
$\overline{\text{REMOTE}}$ $\overline{\text{EJECT 0}}$	Remote Eject 0 Rtn	14 13	Low level ejects diskette in selected drive. (No connection in AM-200.)
$\overline{\text{REMOTE}}$ $\overline{\text{EJECT 1}}$	Remote Eject 1 Rtn	32 31	Optional remote eject signal. (Jumper pad in AM-200.)
$\overline{\text{RESTORE}}$	Restore Head to 00 Rtn	12 11	Low level causes low speed repositioning of the heads to track 00. (No connection in AM-200.)
$\overline{\text{SEEK}}$ $\overline{\text{COMPLETE}}$	Seek Operation Complete Rtn	10 9	AM-200 input. Low level indicates that a seek or restore operation has been completed.
$\overline{\text{SEPCLOCK}}$	Separated Clock Rtn	50 49	AM-200 input. Separated data from read data.
$\overline{\text{SEPDATA}}$	Separated Data Rtn	48 47	AM-200 input. Separated data from read data.
$\overline{\text{SPINDLE}}$ $\overline{\text{MOTOR}}$ $\overline{\text{ENABLE}}$	Spindle Motor Enable Rtn	24 23	Low level energizes the spindle motor. (No connection in AM-200.)

Table 2-3 (Cont.). AM-200 Floppy Disk Interface Signals List

MNEMONIC	NAME	PIN	DESCRIPTION
$\overline{\text{SPINDLE}}$ $\overline{\text{POSITION}}$ $\overline{\text{PULSES}}$	Spindle Position Pulses Rtn	16 15	Jumper pad in AM-200
$\overline{\text{STEP}}$	Step Pulses Rtn	36 35	AM-200 output. Low level of one pulse for each track crossed by the head for a seek to a new address.
$\overline{\text{TRACK 0}}$	Track 0 Rtn	42 41	AM-200 input. Low level indicates heads are positioned over track 0.
$\overline{\text{WD}}$	Write Data Rtn	38 37	AM-200 output. Write data to disk. Write current changes polarity for each positive to negative transition on this line.
$\overline{\text{WG}}$	Write Gate Rtn	40 39	AM-200 output. Low level turns on write current.
$\overline{\text{WP}}$	Write Protect Rtn	44 43	AM-200 input. Low level indicates that the selected disk is write protected.
$\overline{\text{WRITE}}$ $\overline{\text{PROTECT 1}}$	Write Protect 1 Rtn	30 29	Optional write protect line. (Jumper pad in AM-200.)

2.2.3 WIRING AND CONNECTIONS.

When the AM-200 circuit board is received, it is ready for use. No adjustment or calibration is required for operation. The hardware requirements for use are described in this section and the software requirements are described in Section 3.

First ensure that the proper power wiring is available and the correct voltages are connected to the various pins as shown on sheet 1 of the schematic. All power connections are made through the bottom edge connector.

All connections to the S-100 bus are made through the bottom edge connector (Table 2-2) and connections to the floppy disk drive are made through the top edge connector (Table 2-3). Ensure that these connections are correct before plugging the AM-200 circuit board into the system.

2.2.3.1 AM-200 WITH PERSCI DRIVE.

When using the PERSCI drive and the IMS chassis, the fifty conductor cable must be positioned as shown in Figure 2-1. The edge connector for the AM-200 circuit board is connected so that the cable comes forward and back over the board to the rear of the computer chassis and connects to the PERSCI drive as shown.

NOTE

Be sure to perform the wiring modifications to the PERSCI drive as shown in Figure 2-2 before turning on system.

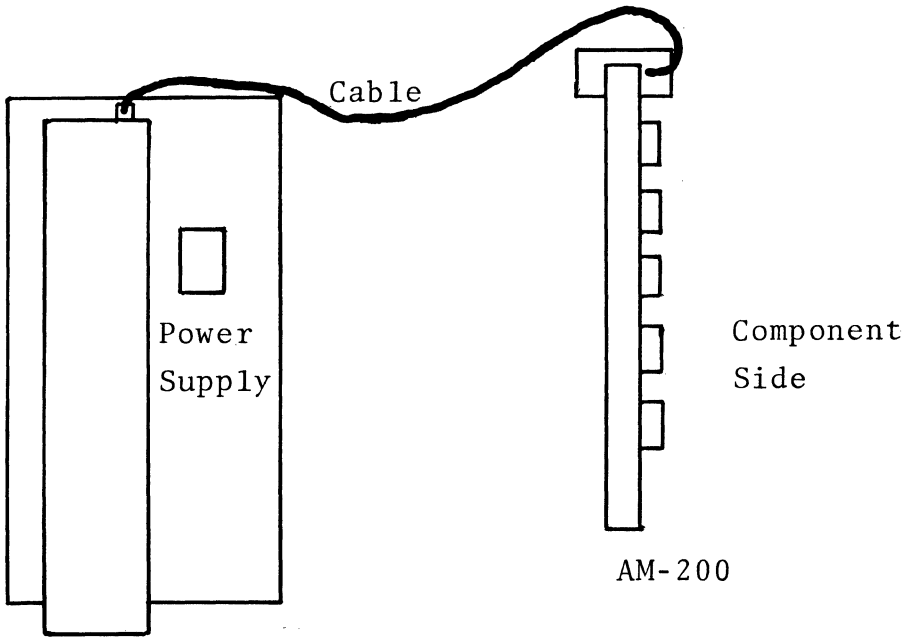


Figure 2-1. AM-200 Cabling to PERSCI Disk Drive

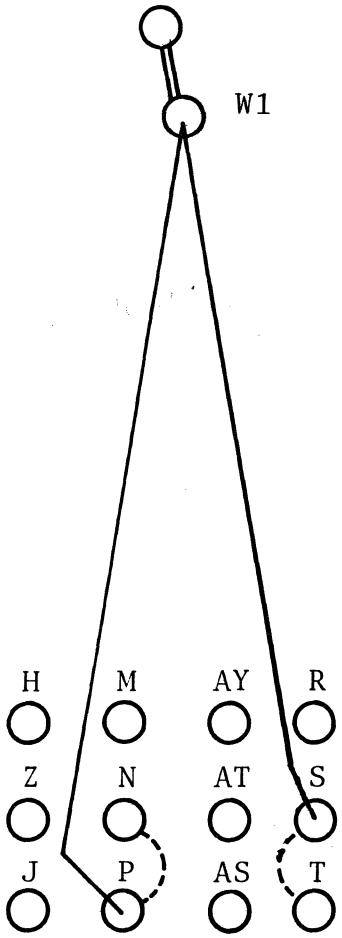
CAUTION

When installing cable at AM-200 end, make sure that pin 1 of the cable is nearest the edge of the circuit card. This is reversed from the standard marking on the flat cable connector on the board.

On the PC board near the rear of the PerSci drive, find the pattern as shown.

1. Remove N-P (shown dotted)
2. Remove S-T (shown dotted)
3. Add W1-P
4. Add W1-S

This modification must be made for each drive used.



When using more than one PerSci the following modification must be made on the 2nd dual drive.

Header U11

1. Remove 4-11 (shown dotted)
2. Remove 2-13 (shown dotted)
3. Add 4-9
4. Add 2-14
5. Remove resistor pack on first drive.

Header U11
Second dual drive only

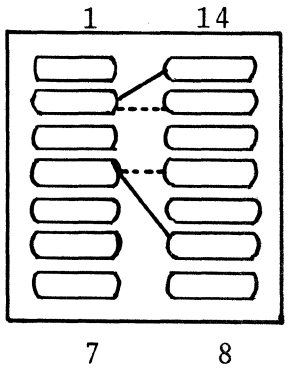


Figure 2-2. PERSCI Dual Disk Drive Wiring Modifications

2.2.3.2 AM-200 WITH WANGCO/ORBIS DRIVE.

When the AM-200 Floppy Disk Controller is used with Wangco/Orbis disk systems, the following modifications to the AM-200 are required. Use this procedure for modifications to Revision A and B boards.

Modification Procedure. Specific modification procedures are as follows:

1. Locate and cut the following traces as shown in Figure 2-3.

    a. On component side between U9 and U10, just opposite pin #2 of U10.
    b. On solder side between U12(1771) and U25. This is a very short, vertical trace just adjacent to pins 5 and 6 of U25.

2. Again on the solder side, add the following wires referring to the attached diagram.

    a. W1 from TG43 to J2-2. TG43 is just opposite pin 5 of U12(1771) and J2-2 is nearest to the right edge of the PC board and the lower of the two pins.
    b. W2 from HLD to J2-30. HLD is just opposite U12-7 and J2-30 is just above U15-1.
    c. W3 from R5-2 to J2-16. R5-2 is the eyelet just above the "R5" symbol engraved on the PC board and J2-16 is just above U16-1.
    d. W4 from U10-2 to WD STEP. U10-2 is between U9 and U10 and is the hole closest to U10-2 and WD STEP is just adjacent to U12-27.

3. Perlod PROMS will not function with the Wangco system so you must order specific PROMS from Alpha Micro.

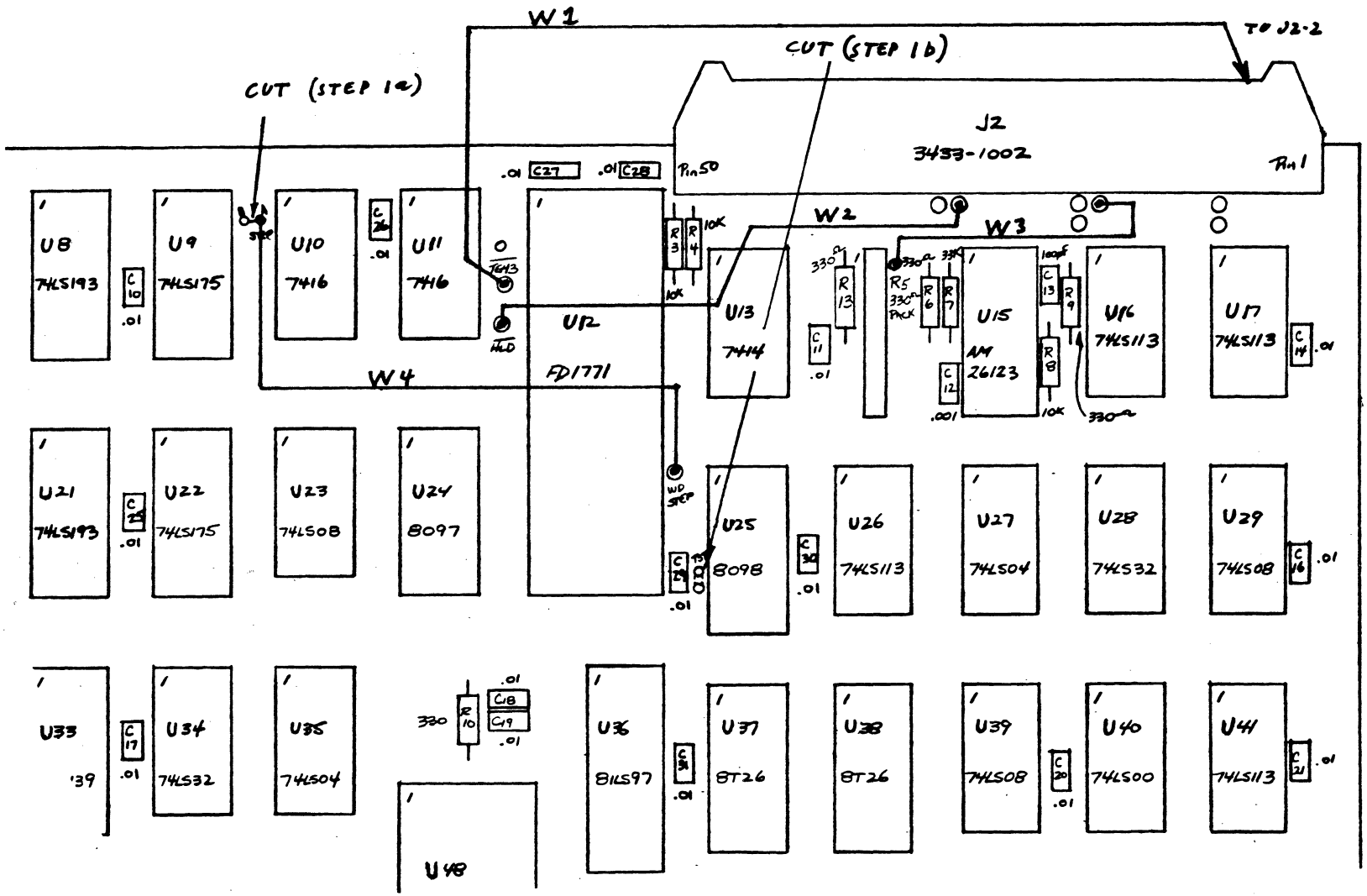


Figure 2-3. AM-200 Circuit Board Layout

4. Due to differences between the Persci and the Wangco disk drives, an adapter board is supplied mounted in the disk drive cabinet. A cable must be connected between the connector marked "INTERFACE" and the AM-200. A Wangco system disk should also be included.

2.3 USER OPTIONS.

Several features on the AM-200 circuit board can be jumper selected at the user's option. If these jumpers are desired, they must be inserted in the circuit board before it is installed in the system.

2.3.1 ADDRESS CODE.

Circuit board addressing can be selected at the user's option for any address block on the address lines A3-A7. Address line A2 must be a zero to generate floppy controller enable (CE) and the first four addresses operate disk controller module registers (see paragraph 4.2.1.2). Connect jumper wires on header U46 to +5V and ground to assign the desired address block. The standard I/O address is: F0.

2.3.2 INTERRUPT LINES.

Interrupt compatibility for any S-100 bus system is provided with jumpers to PINT or any of the vectored interrupt lines VI0-VI7. Attach the jumper wire from the pad connected to pin 2 of U44 to the desired interrupt line (schematic sheet 9).

2.3.3 DMA REQUEST LINES.

DMA request capability for any S-100 bus system is provided with jumpers to PHOLD or any of the vectored interrupt lines VI0-VI7. Attach the jumper wire from the pad connected to pin 4 of U44 to the desired DMA request line (schematic sheet 10). A jumper to VI6 is standard.

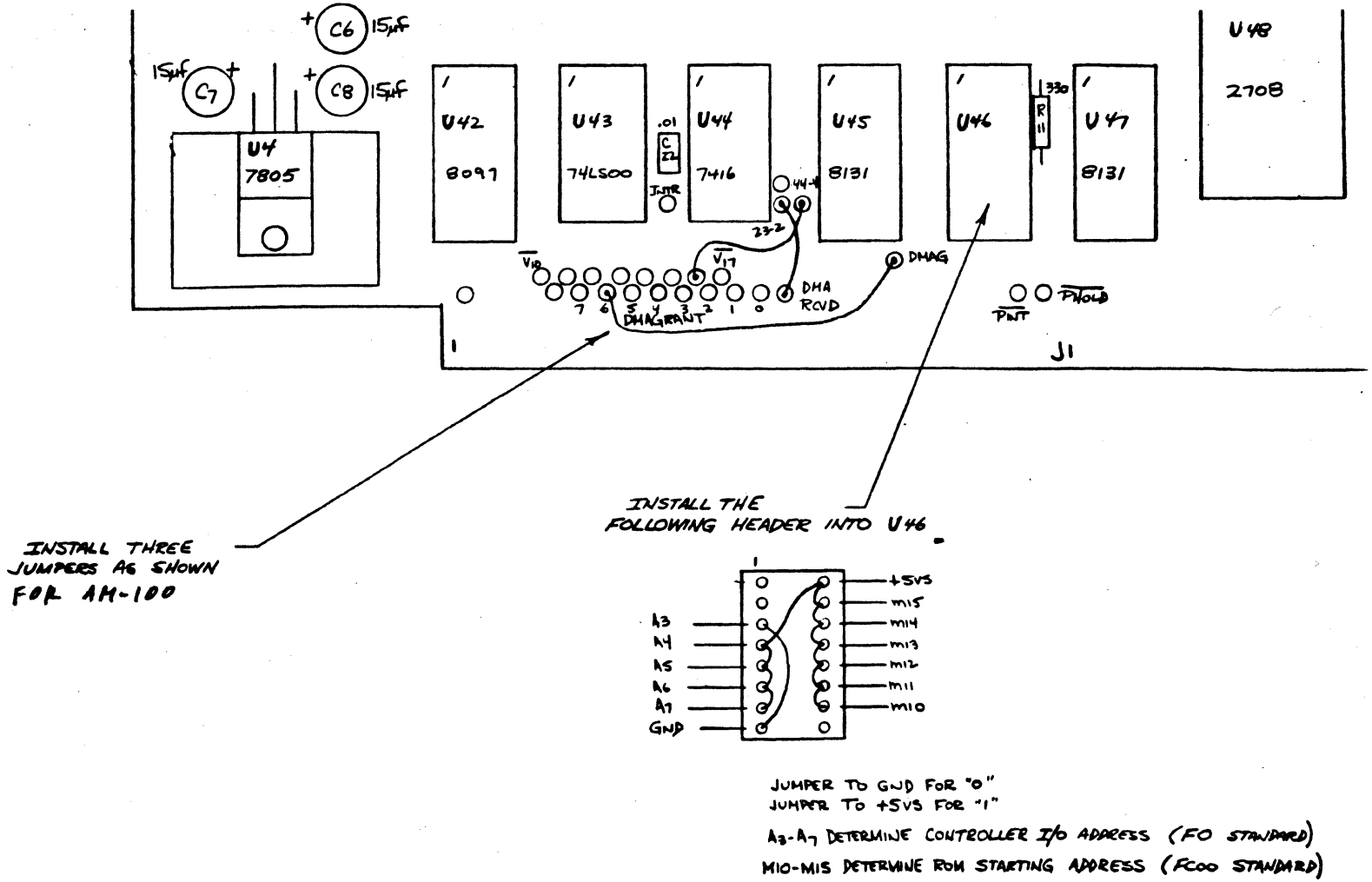


Figure 2-4. Jumpers For Use With AM-100 System

2.3.4 DMA RECEIVED.

DMA Received (DMARCVD) signal from the S-100 Bus must be jumper selected for proper CPU response to the AM-200 circuit board. Install the three jumpers as shown in Figure 2-4 and schematic sheets 8 and 10.

2.3.5 DMA GRANT LINES.

DMA Grant response from the S-100 bus must be jumper selected to provide CPU response to the AM-200 circuit board. Attach the jumper from the pad connected to pin 6 of U25 to the desired DMA Grant line (schematic sheet 8) which is normally DMAGRANT 6.

2.3.6 PHANTOM FEATURE.

A phantom feature can be used with the AM-200 Floppy Disk Controller. This feature is supported in operating system software release 3.0 and later and will not work if a Video Display Module (VDM) is being used for the software program Dystat because the system memory overlaps the VDM memory (see Alpha Micro Operating System AMOS Manual). Also, the memory board must support the phantom feature.

2.3.6.1 APPLICATION.

Modification procedure to the AM-200 circuit board for the phantom feature cover two different configurations. Check the configuration level at your circuit board by the revision designation located on the component side of the board in the lower left quadrant just under the AM-200.

NOTE

For AM-200 circuit boards of Rev. B02 and later, use modification procedures in paragraph 2.3.6.2. For circuit boards earlier than Rev. B02, use modification procedures in paragraph 2.3.6.3.

2.3.6.2 MODIFICATION PROCEDURE FOR BOARDS OF REV. B02 AND LATER.

To provide the phantom feature for boards of Rev. B02 and later, jumper pins 1 and 2 of the address header U46. To remove the phantom feature, remove the jumper.

2.3.6.3 MODIFICATION PROCEDURE FOR BOARDS EARLIER THAN REV. B02.

Use the following procedure to modify AM-200 circuit boards earlier than rev. B02 to add the phantom feature.

NOTE

The primary 48K-64K memory in the system must have phantom option. If in doubt, contact the manufacturer.

1. Cut etch U35-8 to U40-10 at feedthru near U40-10 on back.

2. Jumper.
   a. U22-10 to J1-67
   b. U22-11 to U23-13
   c. U35-8 to U23-12
   d. U40-10 to U23-11

3. Enable phantom on 48K-64K board in the primary bank only, remove jumper from all other.

4. If you do not have a PERLOD REV. D bootstrap PROM in your floppy controller, order specific PROMS from Alpha Micro.

5. PHANTOM will not work with VER. 2.0 and earlier software or AMSLOD REV. B or PERLOD REV. B. and earlier IPL (Indentured Parts List) PROMs.

6. The latest revision of the AM-100 IPL PROM currently in use is PERLOD REV. D which is released on diskettes starting with release 3.1* This IPL PROM now loads either AMS or IBM format, automatically deciding which format the diskette is in.

* Software supplied with Alpha Micro AM-100 systems.

2.3.7 8080 AND CPM SYSTEM MODIFICATION.

When the AM-200 Floppy Disk Controller is used with 8080 systems, DMA jumpers must be as shown in Figure 2-5 (instead of Figure 2-4 for AM-100 systems). In addition, the following modifications to the AM-200 are required.

2.3.7.1 APPLICATION.

This procedure is applicable to AM-200 Floppy Disk Controller Revisions A and B. Note the differences in the procedure for Revision A as compared to the procedure for Revision B.

2.3.7.2 MODIFICATION PROCEDURE.

Use the following procedure to modify AM-200 circuit boards when used with 8080 systems.

1. First determine if you have a REV. A or B board. If the board is a REV. B, skip step 2 and proceed with step 3.

2. If you have a REV. A board, the following jumper changes are required. All wiring changes will be to the solder side of the board.

   a. Cut short trace between U39-4 and U39-5.
   b. Cut other trace going to U39-4.
   c. Cut etch between U53-7 and U53-5.
   d. Jumper free end of trace just cut, to U39-3. See Figure 2-4.
   e. Run a jumper wire from U39-4 to U29-10.

3. Remove jumper wires in lower right corner of board and rewire according to the drawing in Figure 2-5.

4. Remove AM-100 IPL PROM and install the 8080 IPL PROM.

5. No jumper changes are needed on DIP header at U46.

6. The normal 8080 IPL PROM runs at FC00h. So when operating CP/M, examine FC00h and run. CP/M should come up with a sign-on message.

7. A special 8080 IPL PROM is available to run at F000h. If this is used, changes must be made to the DIP header at U46.

8. The console I/O ports are set up for use with the 3P+S and are the same as the AM-100 system. Ports and status bits are as follows:

Control port	:	00h
Data port	:	01h
RDA	:	02h
TBE	:	01h

status bits are all positive true.

9. To improve the reliability of 8080 systems using AM-200 and CP/M, install a 1000 ohm 1/4 watt resistor as follows:

   a. Locate U43 pins 9 and 14. Connect the 1000 ohm resistor between these two pins. U43 should be a 74LS00, near the lower left hand corner of the board.
   b. This modification will not affect normal operation with the AM-100.

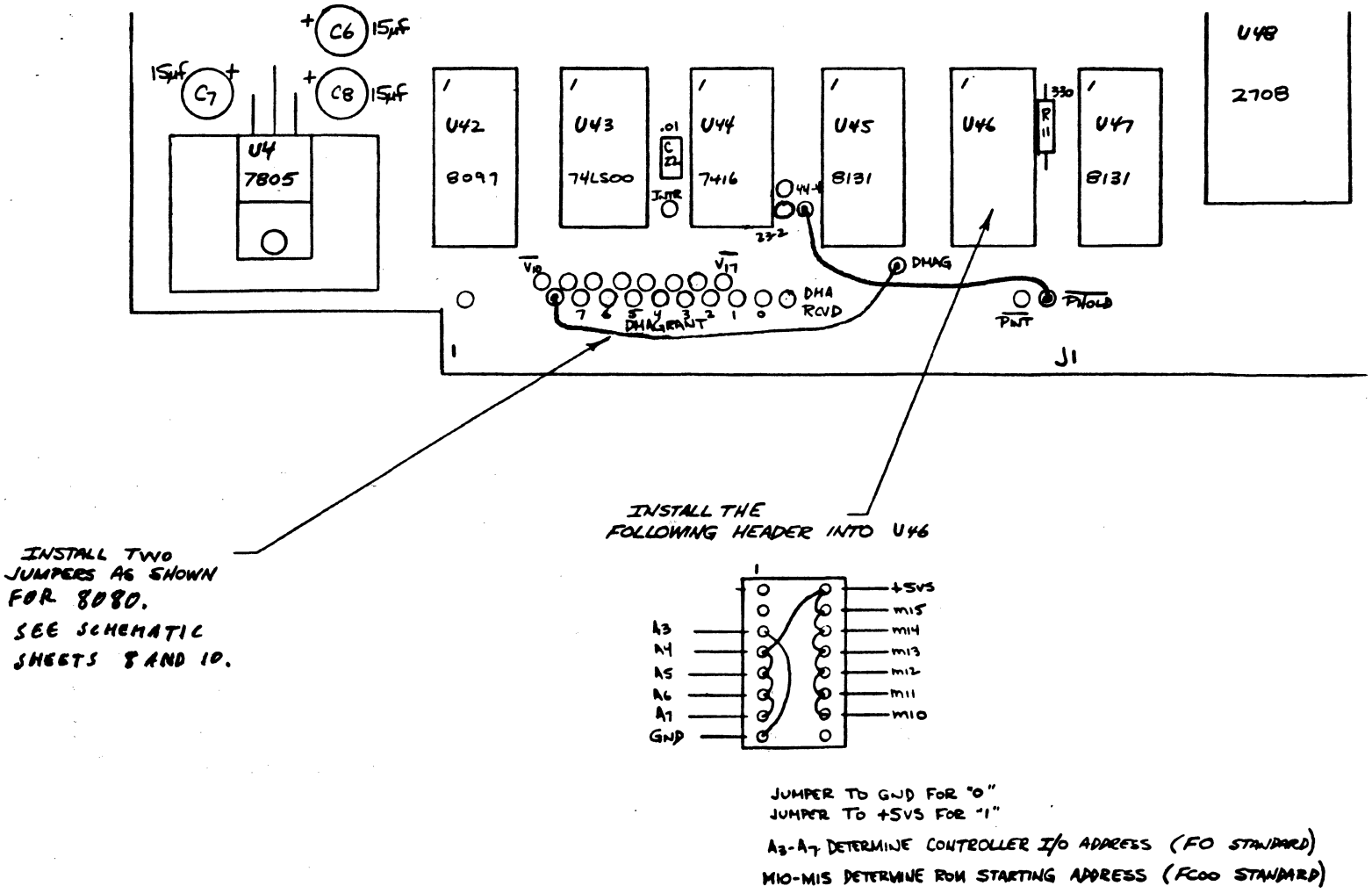


Figure 2-5. Jumpers For Use With 8080 System

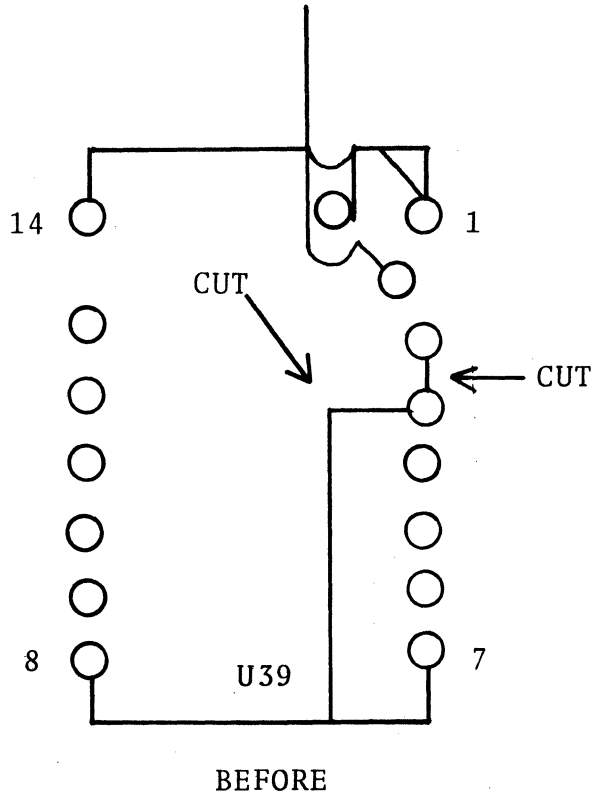


Figure 2-6. AM-200 8080 Modification Etch Cuts "A" Level Only.

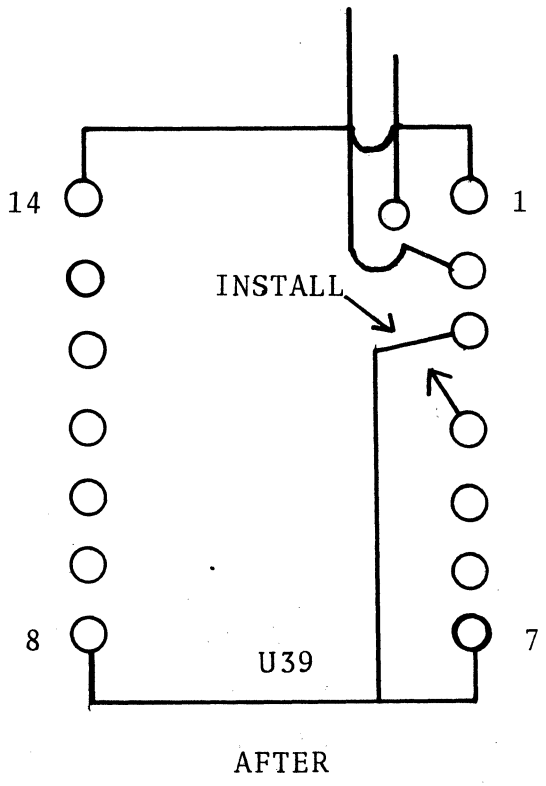


Figure 2-7. AM-200 8080 Modification Wire Additions "A" Level Only.

SECTION 3
PROGRAMMING

3.0 INTRODUCTION.

This section describes the programming requirements for the AM-200 circuit board. Circuit board addressing, bootstrap loader, external control register, and disk format modification are described for complete system compatibility.

3.1 ADDRESSING.

The AM-200 and its associated disk drives are addressed through the S-100 bus address lines. The circuit board address is jumper selectable by the plug-in header U46 from address lines A3-A7. Address lines A0 and A1 select the desired register in the disk controller module and A2 must be a zero to generate floppy controller enable (CE) signal.

Registers internal to the floppy disk controller module must be loaded with the proper control data for disk operation. These registers are loaded from the data access lines for read and write operations under control of address lines A0 and A1. See paragraph 4.2.1.1 for a complete description of these registers. Table 3-1 defines the I/O ports contained in the Floppy Controller.

3.2 EXTERNAL CONTROL REGISTER.

The external control register must be loaded with control data to select the desired operation. To load the control register, address the card with bits A3-A7 and set A0=0, A1=1 and A2=1. The control register accepts control information from the CPU as shown in Table 3-2.

Table 3-1. I/O Port Definitions

I/O Port Address*	Input	Output	Comments
F0	Status Register	Command Register	See Paragraph 4.2.1.2
F1	Track Register	Track Register	See Paragraph 4.2.1.2
F2	Sector Register	Sector Register	See Paragraph 4.2.1.2
F3	Data Register	Data Register	See Paragraph 4.2.1.2
F4	-----	Registers Low Byte**	-----
F5	-----	Registers High Byte**	-----
F6	External Status Register	External Control Register	See Table 3-2

*The base I/O Port address (shown as F0) is jumper selectable to any block of eight I/O addresses.

**Either DMA Address Register or Byte Count Register. See External Control Register, bit 7.

Table 3-2. External Control Register Data

Bit	Function
0	Select Drive 0
1	Select Drive 1
2	Select Drive 2
3	Select Drive 3
4	Sets stepping rate instead of disk controller (PerSci only)
5	Enables interrupts (used as phantom).
6	Controls disk read or write: 1 = WRITE TO FLOPPY, 0 = READ FROM FLOPPY
7	Selects DMA address register (Bit 7=0) or Subsector Register (Bit 7=1).

See Table 3-3 and paragraph 4.2.1.2 for programming registers internal to the disk controller module (U12).

Table 3-3. External Status Register Data

Bit	Input Function
4	Subsector count register $\neq$ 0
7	Seek complete

3.3 BOOTSTRAP LOADER.

The 8K PROM on the AM-200 circuit board contains the bootstrap loader program for system initialization. The base address for boot load is jumper selected by address header U46 (FC00 for PerSci and Wangco). To load the program, set this address on lines A10-A15 and sequence through the address block with address bits A0-A9.

SECTION 4
FUNCTIONAL THEORY OF OPERATION

4.0 INTRODUCTION.

The AM-200 floppy disk controller board contains integrated circuit elements for the necessary data processing for the performance of functions as described in Sections 1, 2 and 3 of this manual. This section describes the functional theory of operation of the circuit board and also provides information for each of the integrated circuit elements.

4.1 CIRCUIT BOARD OPERATION.

This circuit board provides floppy disk control and interface capability that interfaces with the system S-100 bus to the CPU. An 8K PROM contains a bootstrap program for system startup.

The functional block diagram is shown in Figure 4-1 and the circuit board schematic is contained in Section 6 of this manual. Table 4-1 contains a list of the signals used in this circuit board with definitions of their functions.

For S-100 Bus Interface Signals see Table 2-2. For Floppy Disk Interface Signals see Table 2-3. For Floppy Formatter/Controller Signal descriptions see Table 4-2.

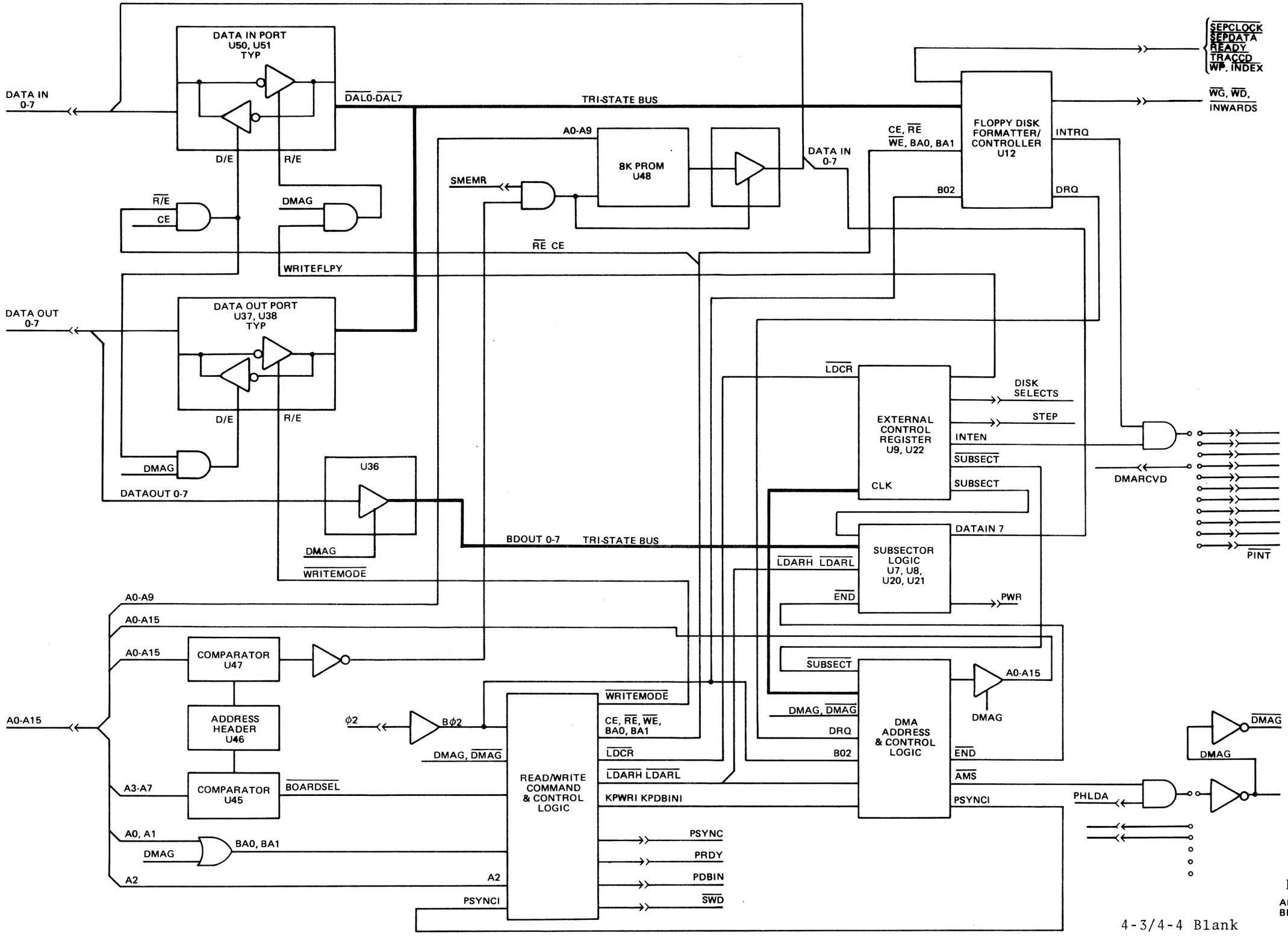


Figure 4-1
AM-200 FUNCTIONAL
BLOCK DIAGRAM

Table 4-1. AM-200 Circuit Board Signal List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	FUNCTION
AO-A15	Address Bit 0-Address Bit 15	3, 5, 6	S-100 Bus Address Lines.
$\overline{AMS}$	Activate Memories	10	Generates jumper selected DMA request to bus master.
BA0, BA1	Buffered Address 0 & 1	6	Sets decoder to generate address load commands.
BDOUT0-BDOUT7	Buffered Data Out Bits 0-7	2	Buffered CPU output data.
$\overline{BOARDSEL}$	Board Select	5	Output of board address comparator. Asserted when S-100 I/O Address matches I/O address wired in header.
CE, $\overline{CE}$	Chip Enable	8	Enables Floppy Disk Formatter/Controller, Data Ports, and conditionally sets PRDY.
$\overline{CE1}$	Chip Enable 1	8	True when the board has been addressed ($\overline{BOARDSEL}$) and $\overline{A2}$ is high. Used to make $\overline{CE}$.
$\overline{DAL0}$-$\overline{DAL7}$	Data Access Lines	7, 9	Eight bit bi-directional bus used for transfer of data, control and status information.

Table 4-1 (Cont.). AM-200 Circuit Board Signal List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	FUNCTION
DATAIN0-DATAIN7	Input Data Bits 0-7	4, 6, 7	Bus Master input data Port.
DATAOUT0-DATAOUT7	Output Data Bits 0-7	2	Bus Master output data Port.
DMAG, $\overline{\text{DMAG}}$	DMA Grant	8	Jumper selectable from S-100 $\overline{\text{DMAGRANT}}$ lines. Sets DMA priority level for AM-200. Level must match VIx level used to request DMA.
$\overline{\text{DS2FF}}$	Read From Floppy	11	Generates Read Enable signal and sets PWRI flip-flop.
$\overline{\text{END}}$	End	10	Controls DMA address register and subsector register. Stops sequencing when high.
INTEN, $\overline{\text{INTEN}}$	Interrupt Enable	2	External control register bit 5 output to enable S-100 interrupts.
JPDBINI	Data Bus Inset	11	Sets Data Bus in flip-flop(J).
KPDBINI	Data Bus Inset	11	Resets Data Bus In flip-flop (K).
KPWRI	PWRI Reset	11	Resets PWRI flip-flop (K)
$\overline{\text{LDARH}}$	Load Address Register High	8	Loads higher 8 bits of sub-sector address register and DMA address register.

Table 4-1 (Cont.). AM-200 Circuit Board Signal List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	FUNCTION
$\overline{\text{LDARL}}$	Load Address Register Low	8	Loads lower 8 bits of sub-sector address register and DMA address register.
$\overline{\text{LDCR}}$	Load Control Register	8	Provides clock input to load external control register from DATAOUT 0-7 lines.
MR, $\overline{\text{MR}}$	Master Reset	2	Resets circuit card.
M10-M15	Address lines	5	Jumper selected output from address header to comparator for PROM selection.
PDBIN	Data Bus In	11	Read strobe.
$\overline{\text{PDBINI}}$	Data Bus In Inverted	11	Inverted read strobe.
PSYNCI	PSYNC Internal	10	Generates PSYNC output through gate (DMAG) and begins bus cycle.
$\overline{\text{PWR}}$	Write Strobe	4	0 = Bus Master is writing.
PWRI	PWR Internal	11	Generates write strobe (PWR) when subsector is non-zero.
$\overline{\text{RDCR}}$	Read Control Register	8	Gates DATAIN 4 and 7 when External Control register is to be read by CPU.

Table 4-1 (Cont.). AM-200 Circuit Board Signal List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	FUNCTION
RE, $\overline{RE}$	Read Enable	8	Initiates a read mode in the Disk Controller DIP, enables the Data In Port with an active CS, and sets PRDY to the S-100 bus.
STEP, $\overline{STEP}$	Disk Head Step	2	Controller output pulses for stepping of disk read/write head.
SUBSECT $\overline{SUBSECT}$	Selects Subsector Register	2	Selects either of two 16 bit registers for addressing by the CPU. 0=DMA Address Register, 1=Subsector Count Register.
$\overline{SWO}$	Write Output Status	11	Output indicating Bus Master is in Write Mode.
$\overline{WE}$	Write Enable	8	Sets the Data Access Lines to the write mode with an active CS to the Disk controller DIP.
WRITEFLPY $\overline{WRITEFLPY}$	Write to Floppy	2	Mode control for DMA logic to either read from or write to floppy disk.
$\overline{WRITE}$ $\overline{MODE}$	Write Mode	8	Sets Receiver Enables in Data Out Port when in Write Mode. Generated from SWO at DMAG.

4.1.1 ADDRESSING.

Address data is received from the S-100 bus on lines A0-A15. The address lines provide one input to comparators U45 and U47. The other inputs come from address header U46, which generates address codes from jumpers on an address block permitting user selection of the circuit board I/O address. The address coding jumper wires are connected to either +5V or ground to generate the selected address. Signal $\overline{\text{BOARDSEL}}$ is asserted when the input address from the address lines compare with the address of the card. This generates Chip Enable (CE) signals in the command and control logic.

The board I/O address is contained on address lines A0-A7 (normally F0). The first four addresses (A0-A1) are contained on the disk controller module U12. Address line A2 must be a 0 to enable CE generation and lines A3-A7 generate $\overline{\text{BOARDSEL}}$ through comparator U45 and header U46.

Addressing for the 8K PROM (U48) is handled by comparator U47 and Header U46. The base address of the PROM is jumper selectable and is normally configured for address FC00 for Per-Sci drives.

4.1.2 BOOTSTRAP PROM.

The 8K PROM (U48) contains the bootstrap program for floppy disk operation. The base address is selected by U46 which enables PROM operation with receipt of Memory Read Status (SMEMR) signal from the S-100 bus. Address lines A0-A9 then sequence through the memory and load the contents of the PROM into the system CPU, through gated drivers, U49 and U53 to DATAIN 0-7 lines.

4.1.3 EXTERNAL CONTROL REGISTER.

The external control register (U9 and U22) must be loaded with data for the AM-200 to execute the desired functions. The external control register consists of eight D flip-flops connected to data lines BDOUT0-BDOUT7. The clock input is Load Control Register (LDCR) signal generated from Buffered Address Bits BA0 and BA1 through decoder U33 (BA0=0, BA1=1). The decoders are enabled by $\overline{\text{PWR}}$, $\overline{\text{A2}}$ and $\overline{\text{BOARDSEL}}$.

The functions loaded into the register with their corresponding bit locations are as follows:

Bit	Mnemonic	Function
0	DS1L	Select Drive 0
1	DS1R	Select Drive 1
2	DS2L	Select Drive 2
3	DS2R	Select Drive 3
4	STEP	Controls stepping rate instead of Disk Controller (PerSci only)
5	INTEN	Enables Interrupts
6	WRITEFLPY	Controls Disk read or write
7	SUBSECT	Selects DMA address Register (Bit 7=0) or subsector count register (Bit 7=1).

For a control register loading operation to take place, the circuit card must be addressed with address lines A2=1, A1=1, A0=0, and BOARDSEL. The PWR signal through U34 generates $\overline{\text{LDCR}}$ which loads the register.

4.1.4 SUBSECTOR REGISTER LOGIC.

Subsector logic consists of a 16-bit up/down counter with control logic. The counter is wired to count down only from its preset state.

This register is loaded before each read command to the floppy drive with one less than the number of bytes to be read from the desired sector. Loading is accomplished by setting bit 7 of the control register to a 1. Combinations of Address lines A0 and A1 generate load commands $\overline{\text{LDARL}}$ and $\overline{\text{LDARH}}$ from the command logic decoder. The settings are A0=0, A1=0 for the lower byte $\overline{\text{LDARL}}$ and A0=1, A1=0 for the upper byte LDARH.

The subsector register is decremented after each byte is transferred from the disk into memory or vice versa. When the register underflows, no more write pulses are transferred. The Borrow output of U21 then sets Bit 7 (DATAIN7) indicating the end of the subsector.

4.1.5 DMA ADDRESS AND CONTROL.

This 16-bit register consists of up/down counters U5, U6, U18, and U19 that are wired to always count up from its preset state. Loading and operation is similar to the subsector register except that the DMA address register operates on the opposite state of control register bit 7 (bit 7=0).

The DMA register is loaded with the initial memory address from BDOUT lines for data transfer to or from the floppy disk. The register is incremented by the $\overline{\text{END}}$ signal after each byte of data is transferred. The register output is wired to the 16 address lines A0-A15.

4.1.6 FLOPPY DISK FORMATTER/CONTROLLER.

The floppy disk formatter/controller module consists of a Western Digital FD1771 module that interfaces the AM-200 with the floppy disk drive. Control and data logic support module operation and provide complete S-100 bus system interface.

The module data lines are connected to tri-state bus lines DAL0-DAL7 for data transfer of both read and write cycles.

Chip select (CE), read or write enable, clock etc. are supplied by the AM-200 logic. Separate data and clock and floppy disk control signals interface directly with the module.

For a complete description of the module and its operation, see paragraph 4.2.1.

4.1.7 DISK READ AND WRITE SEQUENCE.

DMA transfer is initiated by a Data Request signal (DRQ) from the floppy Disk Controller module indicating that it is ready for more data from memory or has received more data from the disk. If $\overline{\text{DMARCVD}}$ is high, DRQ sets the AMS flip-flop and generates an interrupt on the selected line indicating a DMA request. The $\overline{\text{DMARCVD}}$ signal notifies all other DMA controllers on the bus that a DMA exchange is in process so they will not issue a DMA request. The AM-200 then waits until a DMA Grant (DMAG) signal is received from the CPU.

When the DMAG signal is received, it sets flip-flop U16 pin 5 which sets DMA flip-flop U16 pin 8. This generates a pulse that sets PSYNCI flip-flop and generates the PSYNC output to the CPU. At the same time, the DMA register output is placed on address lines A0-A15 indicating the current memory address of data transfer. A data transfer cycle begins for either disk read or write depending on the state of bit 6 of the control register. When a byte of data is transferred, $\overline{\text{END}}$ signal increments the DMA address register, decrements the subsector register and resets the DMA and AMS flip-flops. The AM-200 then waits for another DRQ and $\overline{\text{DMAGRANTx}}$ to repeat the cycle.

When the subsector register decrements past zero, it underflows and sets DATAIN7 indicating the end of a subsector block of data. This sequence is illustrated in Figure 4-2.

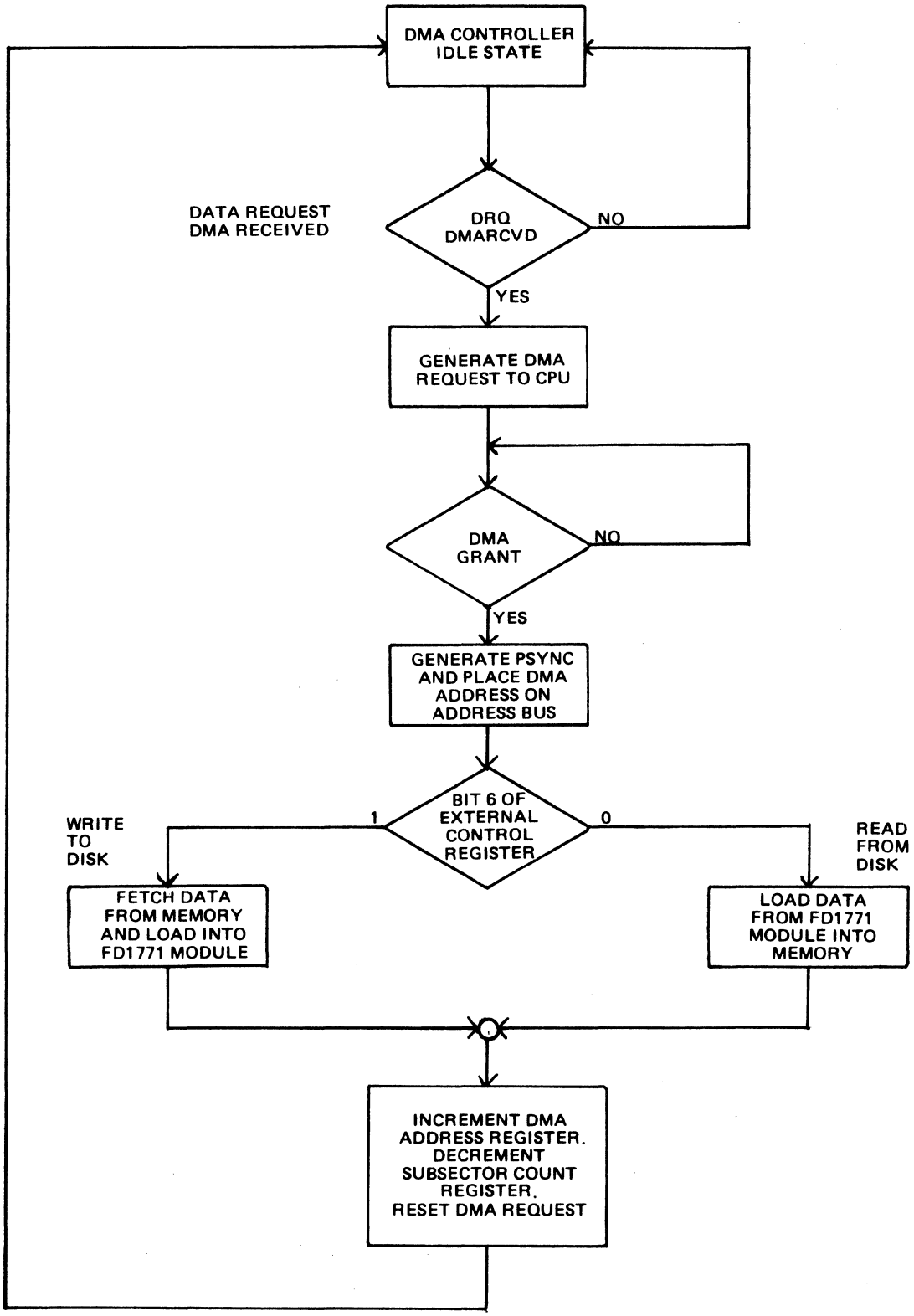


Figure 4-2. Disk Read and Write Sequence Flow Diagram

4.2 CIRCUIT MODULE DESCRIPTION.

This section describes the operation of the individual circuit packages (DIPS) contained on the AM-200 circuit board. Most of the data processing is handled by the Floppy Disk Formatter/ Controller module so it is described in detail. The control logic and interface modules are also described with logic and connection diagrams for each one.

4.2.1 FLOPPY DISK FORMATTER/CONTROLLER DESCRIPTION (U12).

This device performs the function of interfacing a processor to a flexible (Floppy) diskette drive. It provides the data accessing controls and the bidirectional transfer of information between the processor's memory and the magnetically stored data on the diskette. The diskette data is stored in a data entry format compatible with the IBM 3740 specification (other formats may be used providing more data storage). In this format all information is recorded on tracks (radial paths) in sectors (arc sections) defined by a programmed header. Module pin connections are shown in Figure 4-3 and signals are described in Table 4-2.

The device handles single density frequency modulated (FM) data. Each data cell is defined by clock pulses. A pulse recorded between clock pulses identifies the presence of a logic 1 bit; the absence of this pulse is interpreted as a logic 0 bit. The Address Marks for Index, ID, and Data are identified by a particular pattern not repeated in the remainder of the ID field or Data field. This is accomplished by reading patterns that are recorded with missing clock bits (logic 0) as shown below:

Index Address Mark	Data	1 1 1 1 1 1 0 0	=FC
	Clock	1 1 0 1 0 1 1 1	=D7
ID Address Mark	Data	1 1 1 1 1 1 0 1	=FE
	Clock	1 1 0 0 0 1 1 1	=C7

Data Address Mark	Data	1 1 1 1 1 0 1 1	=FB
	Clock	1 1 0 0 0 1 1 1	=C7
Deleted	Data	1 1 1 1 1 0 0 0	=F8
Data Address Mark	Clock	1 1 0 0 0 1 1 1	=C7

These patterns are used as synchronization codes by the device when reading data and are recorded by the formatting command, Write Track, when the device is presented with data F7 through FE.

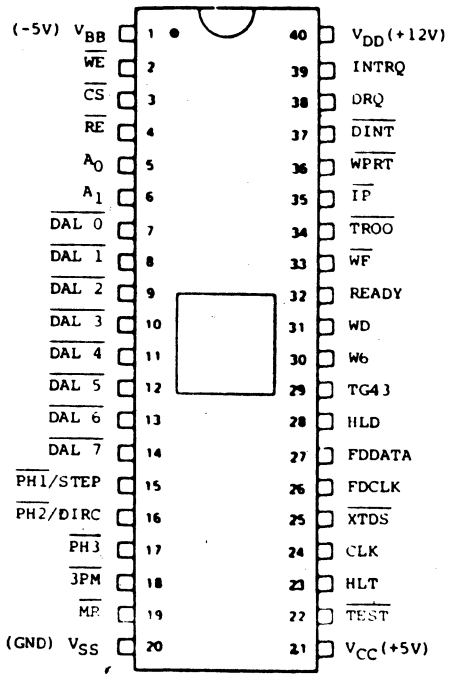


Figure 4-3. Floppy Disk Formatter/Controller Pin Connections

Table 4-2. Floppy Disk Formatter/Controller Signal List

SIGNAL	PIN	FUNCTION
VBB	1	-5V power input
WE WRITE ENABLE	2	Sets the DAL in the write mode with an active $\overline{CS}$ (Chip Select) signal.
CS CHIP SELECT	3	Active low selects the module and enables CPU communication with the device.
RE READ ENABLE	4	Initiates the Read mode to search for a track and sector code in the ID field equal to that in the track and sector registers.
A_0 REGISTER ADDRESS 0	5	Register address line 0 for accessing the active registers with $\overline{CS}$, $\overline{RE}$ and $\overline{WE}$. See Table 4-3.
A_1 REGISTER ADDRESS 1	6	Register address line 1 for accessing the active registers with $\overline{CS}$, $\overline{RE}$ and $\overline{WE}$. See Table 4-3.
DAL0-DAL7 DATA ACCESS LINES	7-14	Data Access Lines Bits 0-7.
PH1/STEP PHASE 1/STEP	15	Phase 1 output for 3 phase stepping motors or stepping rate for step-direction motors.

Table 4-2 (Cont.). Floppy Disk Formatter/Controller Signal List

SIGNAL	PIN	FUNCTION
PH2/DIRC PHASE 2/	16	Phase 2 output for 3 phase stepping motors or level to determine direction for step-direction motors. 0=step in 1=step out.
PH3 PHASE 3	17	Phase 3 output for 3 phase stepping motors.
3PM 3 PHASE MOTOR	18	Selects type of motor interface 1 = 3 Phase, 0=step-direction.
MR MASTER RESET	19	Master Reset clears the command register and initiates a restore (seek track 00) command.
(GND) VSS	20	Ground
VCC	21	+5V power input
TEST	22	For testing only.
HLT HELD LOAD TIMING	23	Input to enable a read or write operation. Input is sampled after a 10 ms internal delay and may be wired high if 10 ms is sufficient time.
CLK	24	System Ø2 clock
XTDS EXTERNAL DATA SEPARATION	25	Selects data separation 0 = External 1 = Internal.

Table 4-2 (Cont.). Floppy Disk Formatter/Controller Signal List

SIGNAL	PIN	FUNCTION
FDCLK SEPARATED CLOCK	26	Separated clock input after data and clock have been separated from raw data from disk.
FDDATA SEPARATED DATA	27	Separated Data input after data and clock have been separated from raw data from disk.
HLD HEAD LOAD	28	Output to cause the storage element to be placed in close proximity to the Read/Write head.
TG43 LOW CURRENT	29	Output to lower the write current when writing on the inner tracks.
WG WRITE GATE	30	Write Gate output to floppy disk drive.
WD WRITE DATA	31	Write Data output to floppy disk drive.
READY	32	Input indicating that the disk is loaded, rotating and the front door is closed.
WF FILE INOPERABLE	33	Input
TR00 TRACK ZERO	34	Indicates that the Read/Write head is over track zero.

Table 4-2 (Cont.). Floppy Disk Formatter/Controller Signal List

SIGNAL	PIN	FUNCTION
IP INDEX PULSE	35	Input signal to indicate when the index mark is encountered - once per revolution of the disk.
WPRT WRITE PROTECT	36	Active low input that prevents execution of a write command.
DINT DISK INITIALIZATION	37	Active low input that prevents a write track command to disable rewriting of a format over previously formatted disk.
DRQ DATA REQUEST	38	Output that indicates readiness to transfer a byte of data during read or write operations.
INTRQ INTERRUPT REQUEST	39	Output that indicates completion of an operation either successfully or terminated by a fault.
VDD	40	+12V power input.

Table 4-3. AM-200 Register Addresses

A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	Status Rgstr	Command Rgstr
0	1	Track Rgstr	Track Rgstr
1	0	Sector Rgstr	Sector Rgstr
1	1	Data Rgstr	Data Rgstr

4.2.1.1 ORGANIZATION.

The Floppy Disk Formatter block diagram is illustrated in Figure 4-4. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register. This 8-bit register assembles serial data from the Read Data input (FDDATA) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register. This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register. This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR). This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can

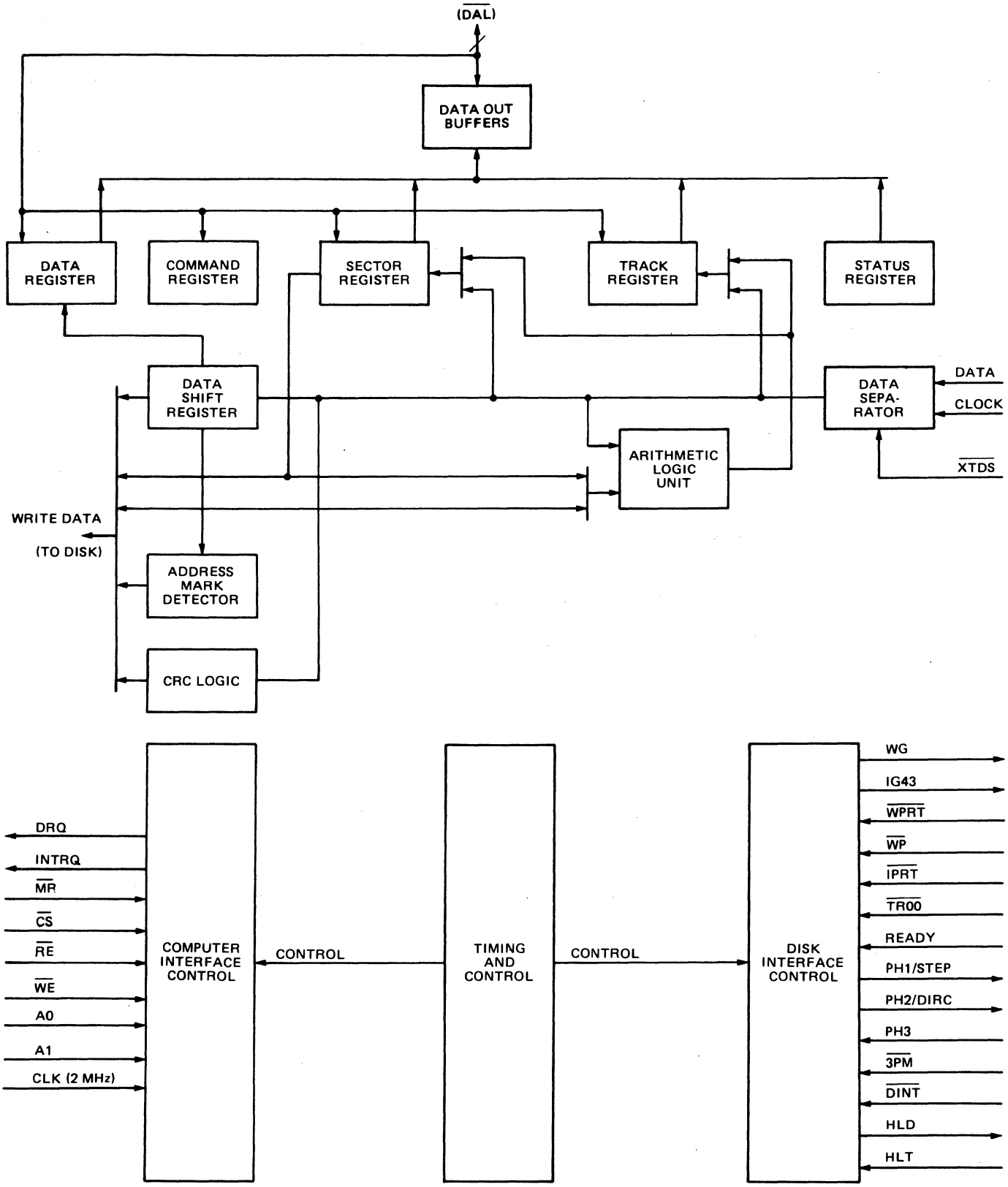


Figure 4-4. Floppy Disk Formatter/Controller Module Block Diagram

be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR). This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR). This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic. This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU). The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

AM Detector. The Address Mark detector is used to detect ID, Data, and index address marks during Read and Write operations.

Timing and Control. All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from a 2.0 MHz external crystal clock.

4.2.1.2 PROCESSOR INTERFACE.

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the device. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The least-significant address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ (RE)	WRITE (WE)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the device and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readput, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

4.2.1.3 FLOPPY DISK INTERFACE.

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. A 2.0 MHz ± 1% square wave clock is required at the CLK input for internal control timing, (may be 1.0 MHz for mini floppy.)

Head Positioning. Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 4-4) can be applied to a Three Phase Motor or a Step-Direction Motor through the device interface. When the 3PM input is connected to ground the device operates with a three-phase motor control interface, with one active low signal per phase on the three output signals PH1, PH2 and PH3. The stepping sequence, when stepping in, is Phases 1-2-3-1,

and when stepping out, Phases 1-3-2-1. Phase 1 is active low after Master Reset. Note: PH3 needs an inverter if used.

Table 4-4. Stepping Rates

r1	r0	1771-01 CLK=2MHZ TEST=1	1771-01 CLK=1MHZ TEST=1	1771 or-01 CLK=2MHZ TEST=0	1771 or-01 CLK=1MHZ TEST=0
0	0	6ms	12ms	APPROX.	APPROX.
U	1	6ms	12ms	400us	800us
1	0	10ms	20ms		
1	1	20ms	40ms		

The Step-Direction Motor Control Interface is activated by leaving input 3PM open or connecting it to +5V. The Phase 1 pin PH1 becomes a Step pulse of 4 microseconds duration. The Phase 2 pin PH2 becomes a direction control with a high level on this pin indicating a Step In, and a low level indicating a Step Out. The Direction output is valid a minimum of 24 microseconds prior to the activation of the Step pulse.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is preset.

The Head Load (HDL) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify Operation, or a Seek or Step operation with the head load bit, h, a logic one remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HDL signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input after 10 msec. A low high state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded before stepping to the destination track on the disk whenever the h bit is a logic one.

Disk Read Operation. The 2.0 MHz external clock provided to the device is internally divided by 4 to form the 500 KHz clock rate for data transfer. When reading data from a diskette this divider is synchronized to transitions of the Read Data (FDDATA) input. When a transition does not occur on the 500 KHz clock active state, the clock divider circuit injects a clock to maintain a continuous 500 KHz data clock. The 500 KHz data clock is further divided by 2 internally to separate the clock and information bits. The divider is phased to the information by the detection of the address mark.

In the internal data read and separation mode the Read Data input should be a pulse for every Flux Transition. This signal can be derived from the amplified, differentiated, and sliced Read Head signal, or by the output of a flip-flop toggling on the Read Data pulses. This input is sampled by the 2 MHz clock to detect transitions.

The chip can also operate on externally separated data, as supplied by methods such as Phase Lock loop, One Shots, or variable frequency oscillators. This is accomplished by grounding the External Data Separator ($\overline{\text{XTDS}}$) INPUT. When the Read Data input makes a low-to-high transition, the information input to the FDDATA line is clocked into the Data Shift Register. The assembled 8 bit data from the Data Shift Register are then transferred to the Data Register.

The normal sector length for Read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read and Write commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands respectively by setting a logic o in Bit 3 of the command word. The sector length indicator specifies the number of 16 byte groups or 16 x N, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

Disk Write Operation. After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 usec duration. This signal may be used to externally toggle a flip-flop to control the direction of Write Current flow.

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the device before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the device terminated the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the $\overline{\text{Write Gate}}$ output becomes inactive. Tie $\overline{\text{WF}}$ high if not used.

Whenever a Read or Write command is received the device samples the READY input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the READY input.

4.2.1.4 COMMAND DESCRIPTION.

The Floppy Disk Formatter/Controller accepts and executes eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in table 4-5. Flags for all four types are summarized in Table 4-6.

Table 4-5. Command Summary

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	s
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

Table 4-6. Flag Summary

TYPE I

h = Head Load Flag (Bit 3)
- h=1, Load head at beginning
- h=0, Do not load head at beginning

V = Verify flag (Bit 2)
- V=1, Verify on last track
- V=0, No verify

r1r0 = Stepping motor rate (Bits 1-0)
- Refer to Table 1 for rate summary

u = Update flag (Bit 4)
- u=1, Update Track register
- u=0, No update

TYPE II

m = Multiple Record flag (Bit 4)
- m =0, Single Record
- m =1, Multiple Records

b = Block length flag (Bit 3)
- b =1, IBM format (128 to 1024 bytes)
- b =0, Non-IBM format (16 to 4096 bytes)

a_1a_0 =Data Address Mark (Bits 1-0)
- a_1a_0 =00, FB (Data Mark)
- a_1a_0 =01, FA (User defined)
- a_1a_0 =10, F9 (User defined)
- a_1a_0 =11, F8 (Deleted Data Mark)

TYPE III

s =Synchronize flag (Bit 0)
- $\overline{s}$=0, Synchronize to AM
- $\overline{s}$=1, Do Not Synchronize to AM

TYPE IV

I_i =Interrupt Condition flags (Bits 3-0)
- I_0=1, Not Ready to Ready Transition
- I_1=1, Ready to Not Ready Transition
- I_2=1, Index Pulse
- I_3=1, Immedate interrupt

E =Enable HLD and 10 msec Delay
- E=1, Enable HLD, HLT and 10 msec Delay
- E=0, Head is assumed Engaged and there is no 10 msec Delay.

4.2.1.5 TYPE I COMMANDS.

The Type 1 Commands include the RESTORE, SEEK STEP, STEP-IN, AND STEP-OUT commands. Flow diagrams are contained in Figure 4-5. Each of the Type 1 Commands contain a rate field (r0r1), which determines the stepping motor rate as defined in Table 4-4.

The type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command HLD (output is made active). If h=0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the device receives a command that specifically disengages the head. If the device does not receive any commands after three revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type 1 Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed, if V=0, no verification is performed.

During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the BUSY status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, the Seek Error status bit (Status bit 4) is set and the BUSY status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after two revolutions of the disk, the device terminates the operation and sends an interrupt (INTRQ).

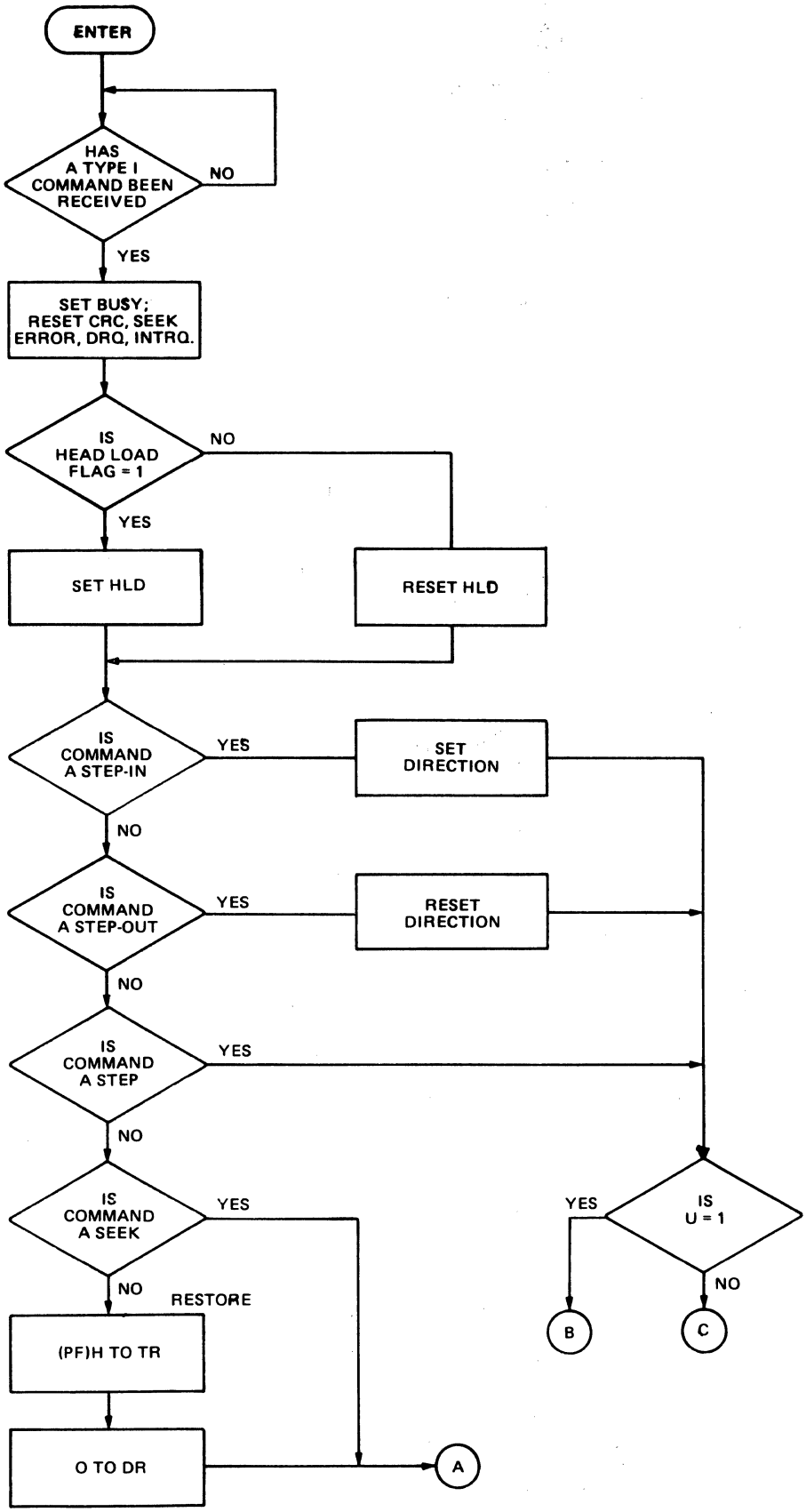


Figure 4-5. Type I Command Flow (Sh 1 of 3)

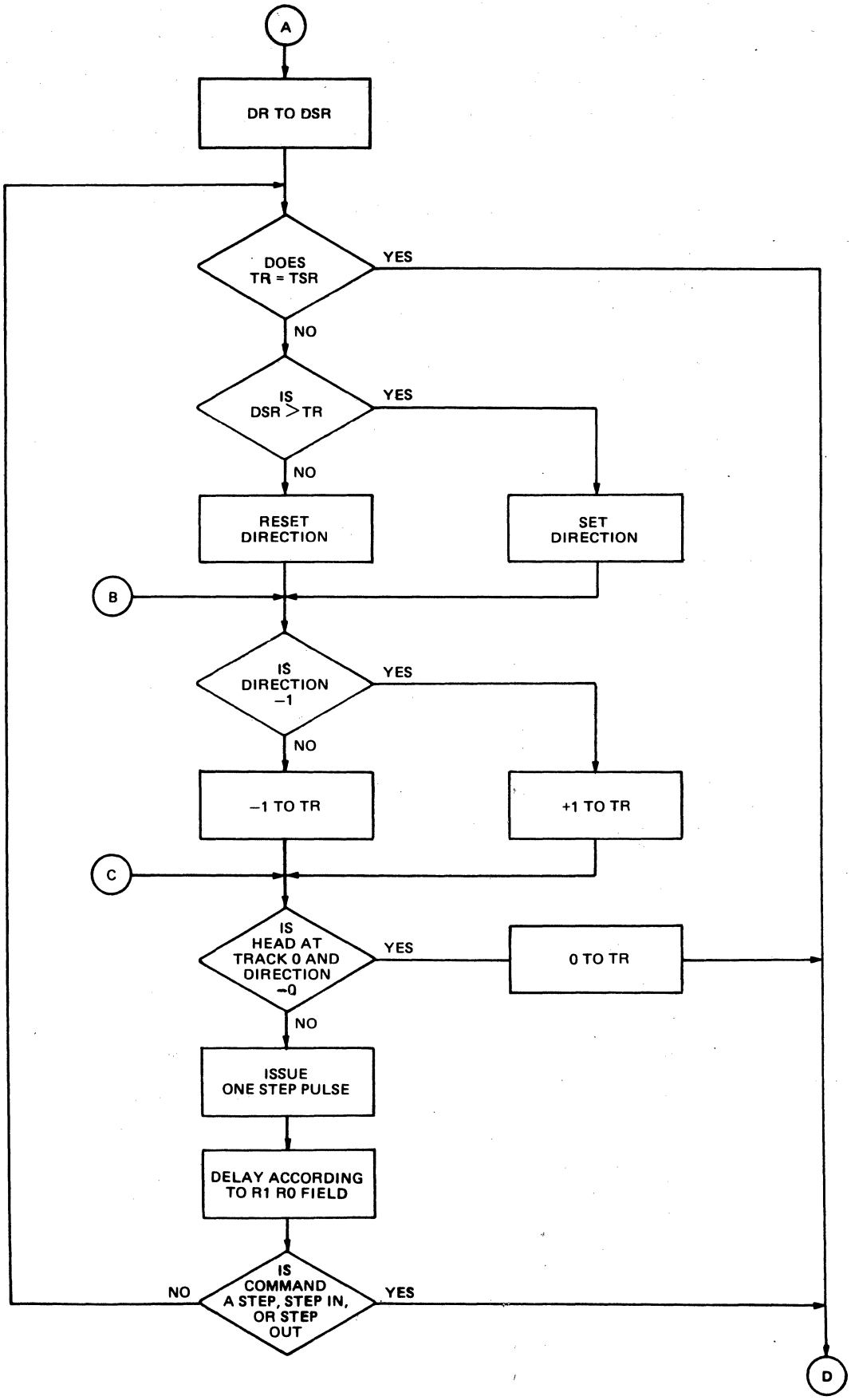


Figure 4-5. Type I Command Flow (Sh 2 of 3)

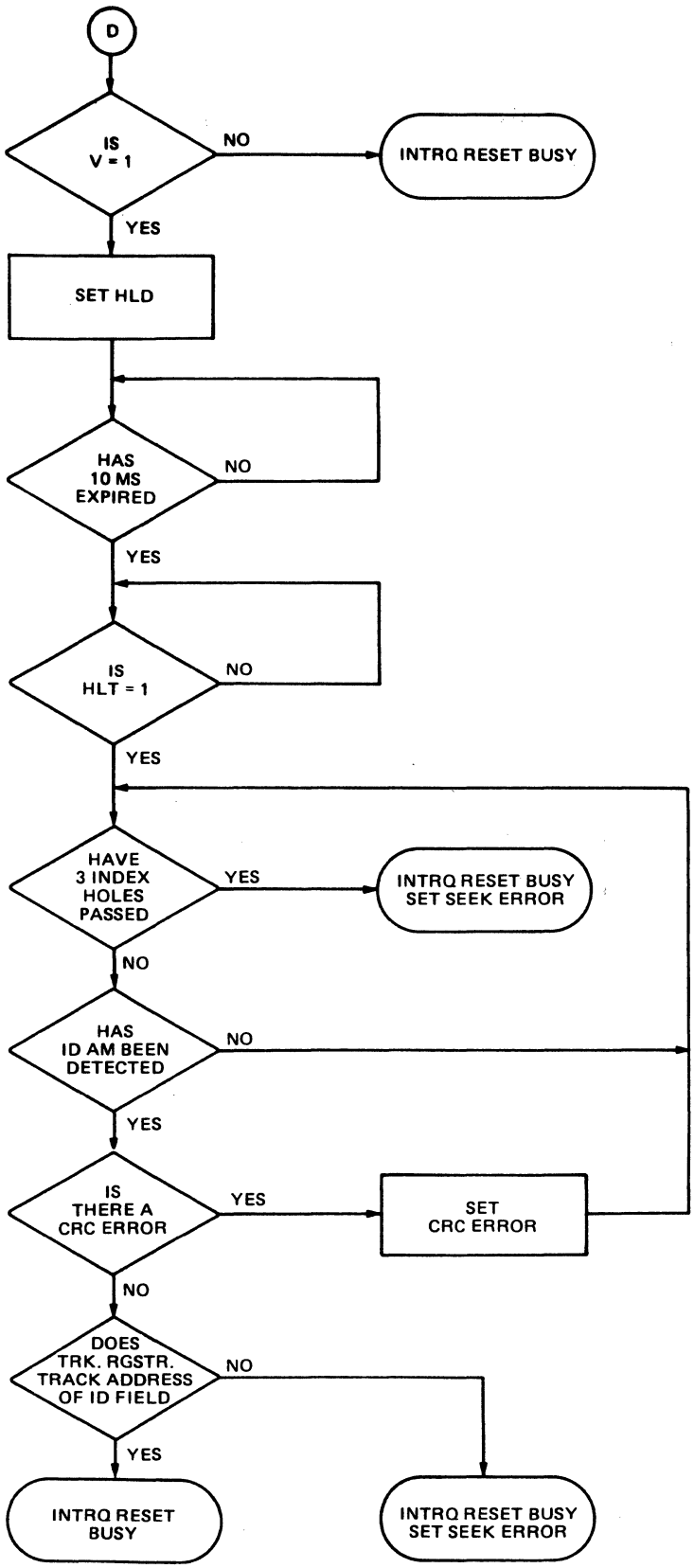


Figure 4-5. Type I Command Flow (Sh 3 of 3)

The STEP, STEP-IN, and STEP-OUT commands contain an UPDATE flag (U). When U=1, the track register is updated by one for each step. When U=o, the track register is not updated.

Restore (Seek Track 0). Upon receipt of this command the Track 00 ($\overline{TROO}$) input is sampled. If $\overline{TROO}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TROO}$ is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r1r0r field are issued until the $\overline{TROO}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{TROO}$ input does not go active low after 255 stepping pulses, the device terminates operation, interrupts, and sets the Seek error status bit. Note that the RESTORE command is executed when MR goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

Seek. This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The device will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step. Upon receipt of this command, the device issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit

allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-In. Upon receipt of this command, the device issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r1 r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-Out. Upon receipt of this command, the device issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

4.2.1.6 TYPE II COMMANDS.

The Type II Commands include the Read Sector(s) and Write Sector(s) commands. Flow diagrams are shown in Figure 4-6. Prior to loading the type II command into the COMMAND REGISTER, the computer must load the Sector Register with the desired sector number. Upon receipt of the type II command, the busy status Bit is set. If the E flag =1 (this is the normal case) HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and Data Field format are shown below:

GAP	ID AM	TRACK NUMBER	ZEROS	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD									DATA FIELD			

IDAM = ID Address Mark – DATA=$(FE)_{16}$ CLK = $(C7)_{16}$
Data AM = Data Address Mark – DATA=(F8, F9, FA, or FB), CLK = $(C7)_{16}$

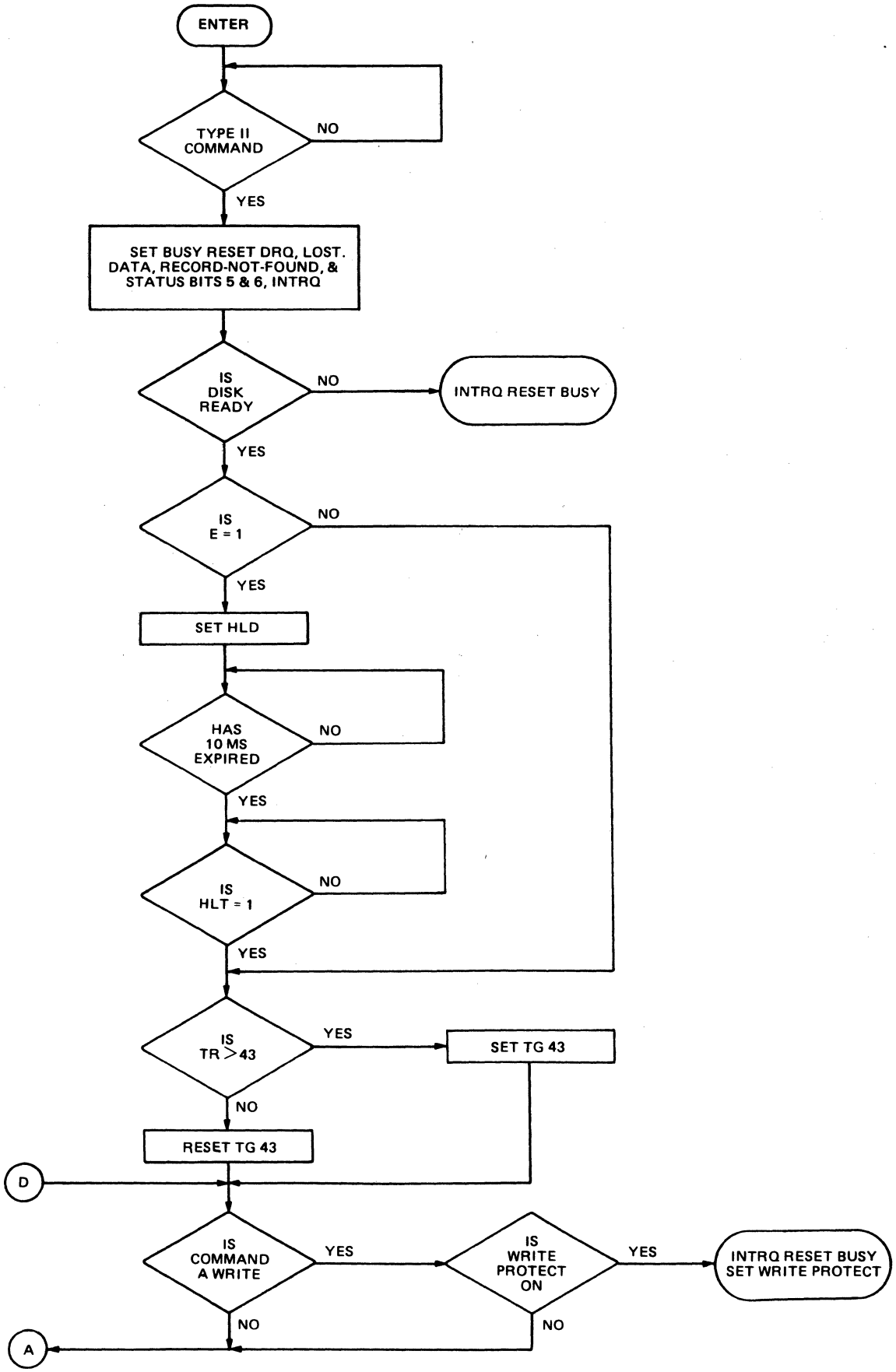


Figure 4-6. Type II Command Flow (Sh 1 of 4)

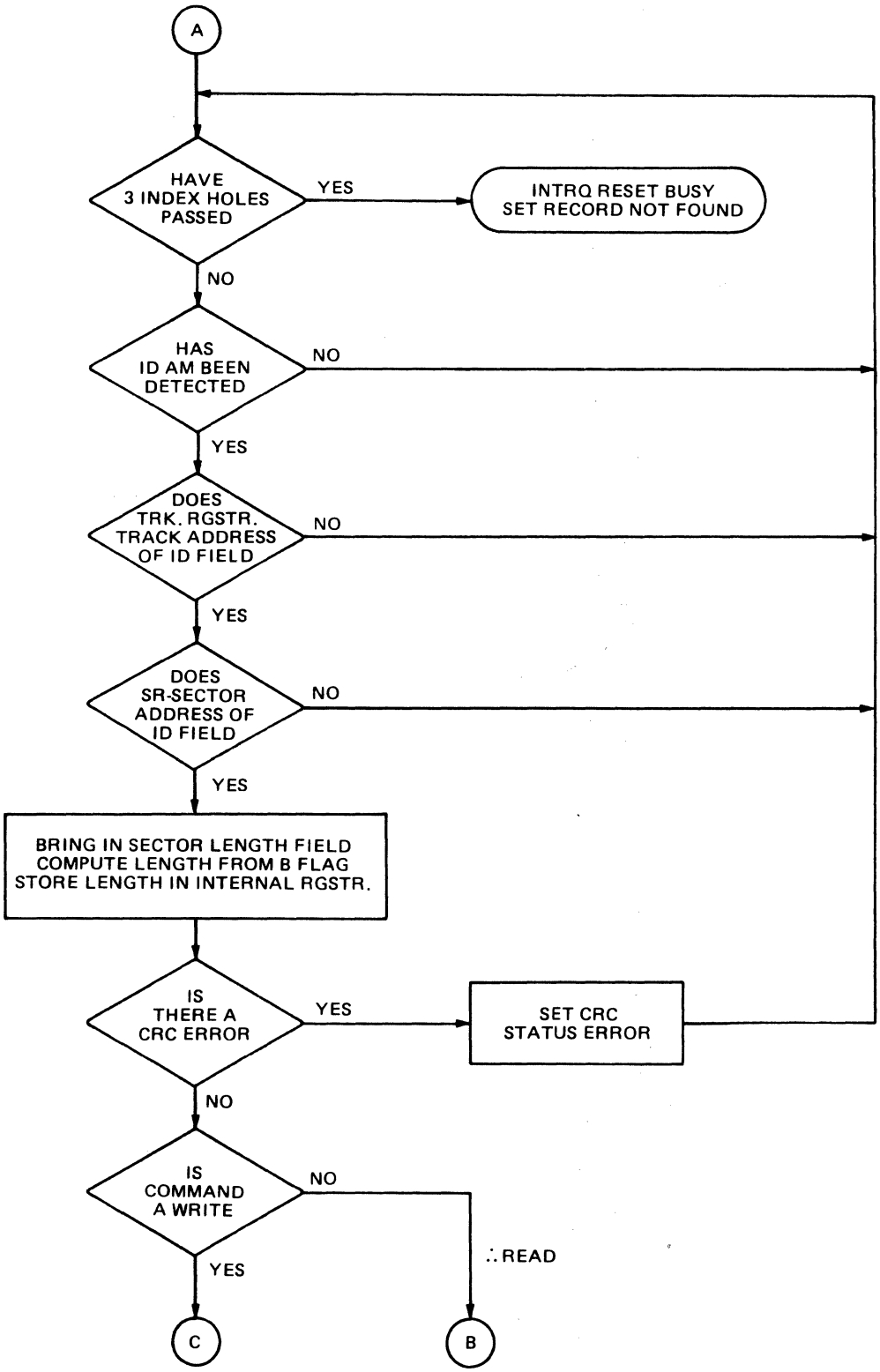


Figure 4-6. Type II Command Flow (Sh 2 of 4)

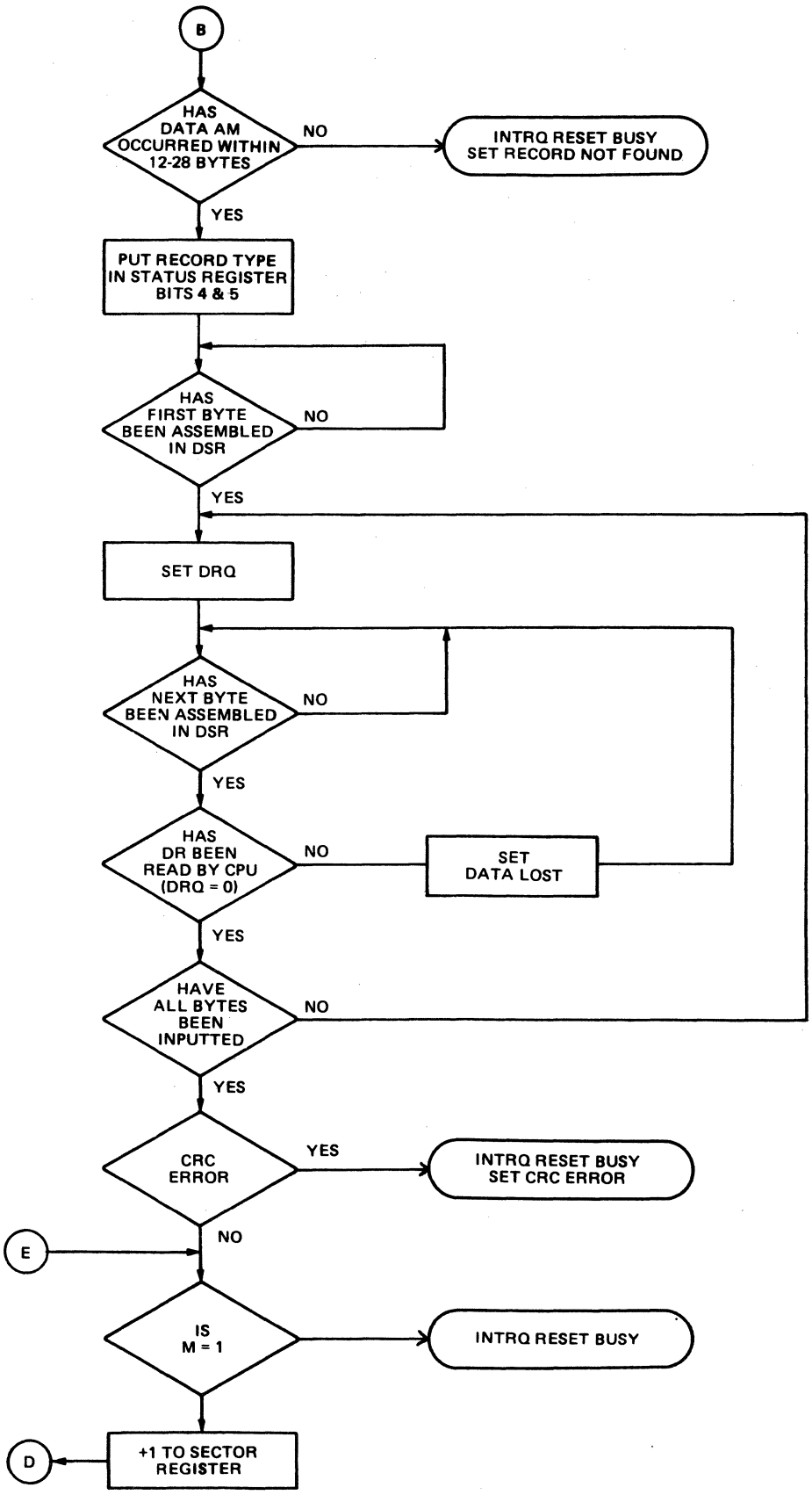


Figure 4-6. Type II Command Flow (Sh 3 of 4)

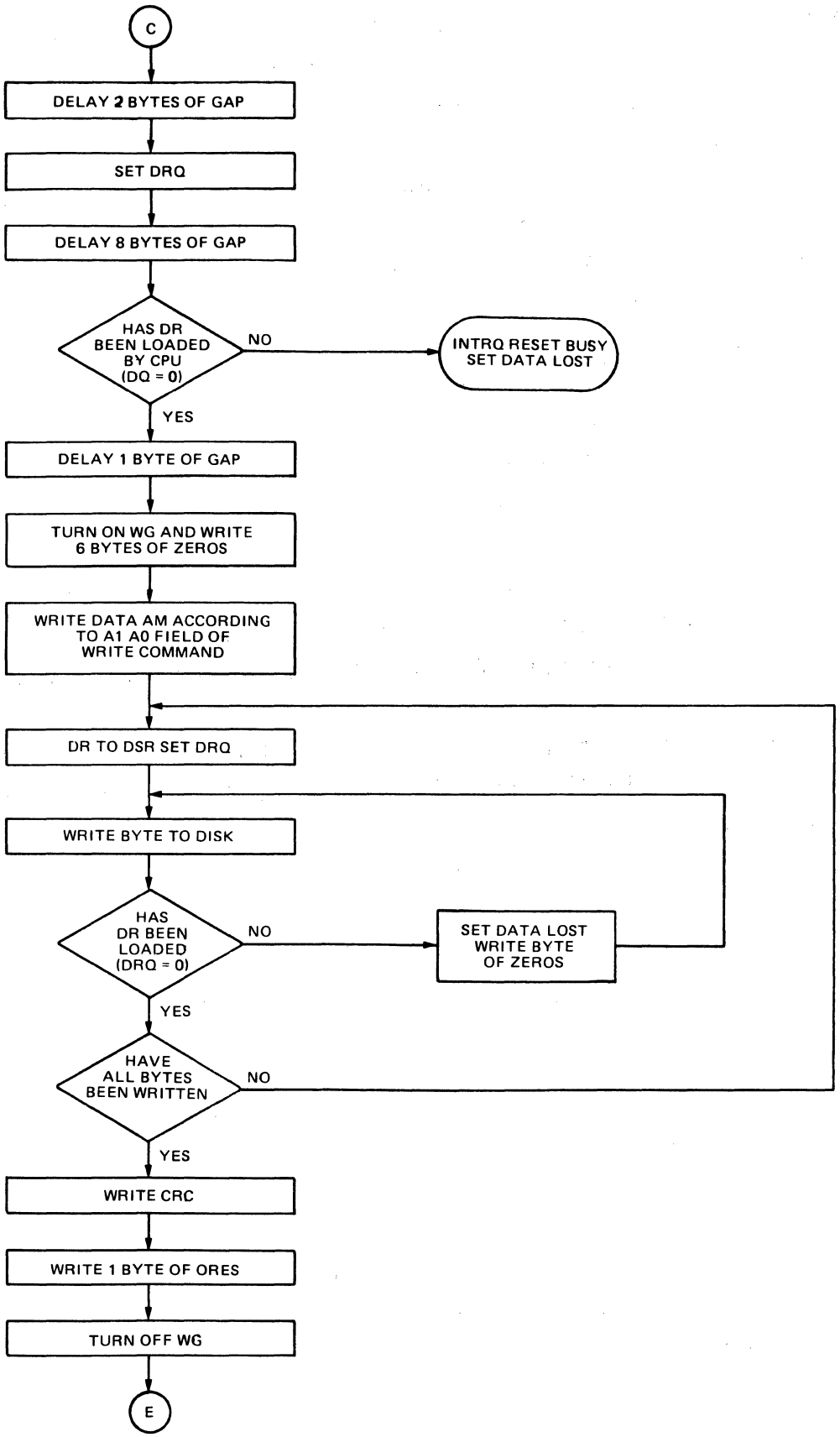


Figure 4-6. Type II Command Flow (Sh 4 of 4)

When an ID field is located on the disk, the device compares the Track Number of the ID field with the Track register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The device must find an ID field with a Track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where n-0,1,2,3.

For b=1

Sector Length Field (hex)	Number of bytes in sector (decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:

For b=0

Sector Length Field (hex)	Number of bytes in sector (decimal)
01	16
02	32
03	48
04	64
.	.
.	.
.	.
FF	4080
00	4096

Each of the type II commands also contain a (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m=o a single sector is read or written and an interrupt is generated at the completion of the command. If m=1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The device will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force interrupt command is loaded into the command register, which terminated the command and generates an interrupt.

Read Command. Upon receipt of the Read command, the head is loaded, the BUSY status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct field; if not, the Record Not Found status bit is set and the operation is terminated. When the

first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below:

Status Bit 5	Status Bit 6	Data AM (HEX)
0	0	FB
0	1	FA
1	0	F9
1	1	F8

Write Command. Upon receipt of the Write command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The device counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a^1a^0 field of the command as shown below:

a1	a0	DATA MARK (HEX)	CLOCK MARK (HEX)
0	0	FB	C7-
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

The device then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.

4.2.1.7 TYPE III COMMANDS.

Type III Commands include Read Address, Read Track, and Write Track. Flow diagrams are shown in Figure 4-7.

Read Address. Upon receipt of the Read Address command, the head is loaded and the BUSY Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	ZEROS	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the device checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the BUSY Status is reset.

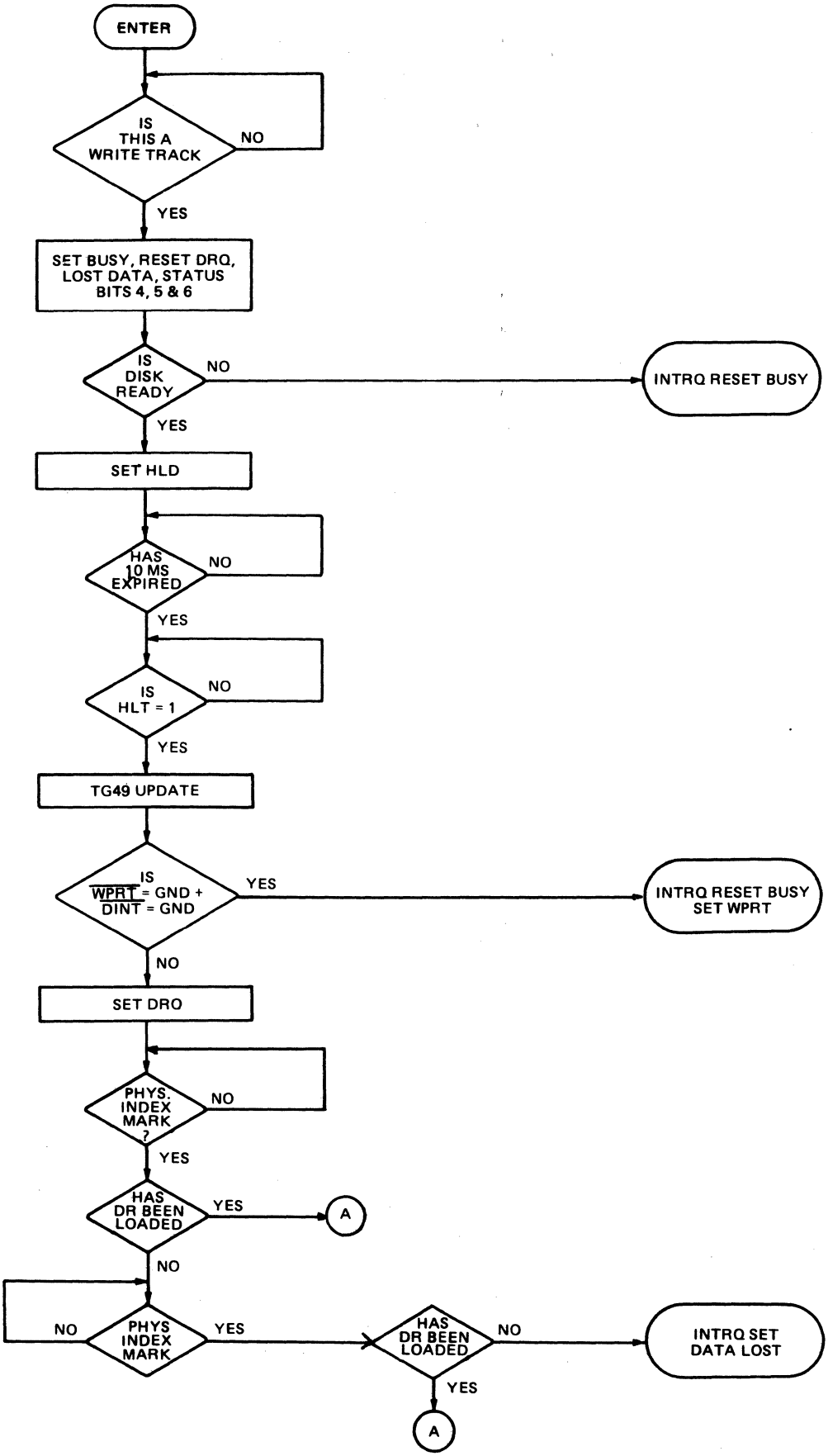


Figure 4-7. Type III Command Flow (Sh 1 of 2)

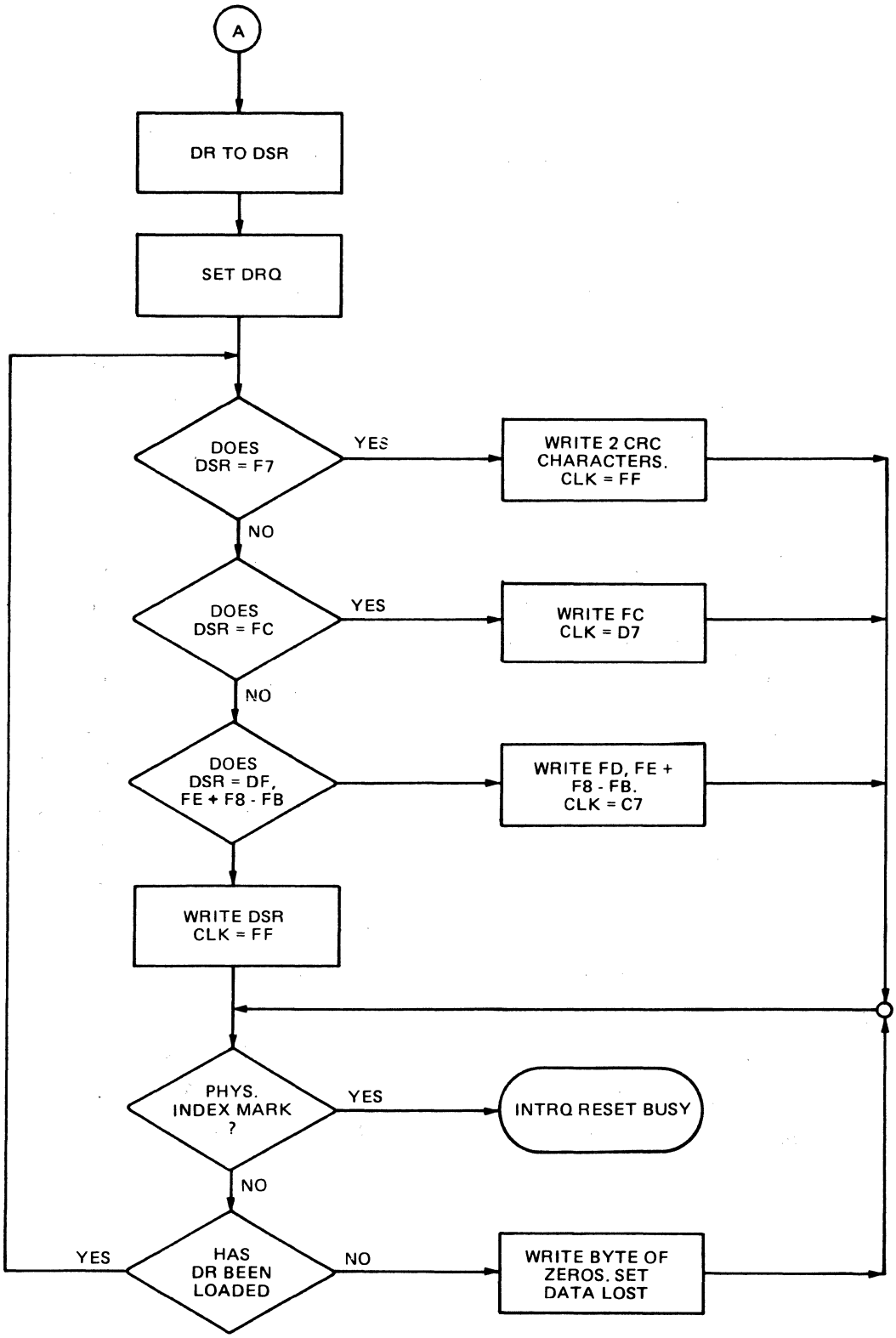


Figure 4-7. Type III Command Flow (Sh 2 of 2)

Read Track. Upon receipt of the Read Track command, the head is loaded and the BUSY Status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit 0 (S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

Write Track. Upon receipt of the Write Track command, the head is loaded and the BUSY Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the Table 4-7 below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.

Table 4-7. Control Bytes for Initialization

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Char.	FF
F8	Data Addr. Mark	C7
F9	Data Addr. Mark	C7
FA	Data Addr. Mark	C7
FB	Data Addr. Mark	C7
FC	Index Addr. Mark	D7
FD	Spare	
FE	ID Addr. Mark	C7

The Write Track command will not execute if the $\overline{\text{DINT}}$ input is grounded; instead if the Write Protect Status bit is set and the interrupt is activated. Note that one F7 pattern generates 2 CRC characters.

4.2.1.8 TYPE IV COMMANDS.

Force Interrupt. This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt (Note: After the interrupt occurs, user must load force interrupt with I_0-I_3 = 0 to clear out INTRQ)

NOTE: If I_0-I_3 = 0, there is no interrupt generated but the current command is terminated and busy is reset.

4.2.1.9 STATUS DESCRIPTION.

Upon receipt of any command, except the Force interrupt command, the BUSY Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the BUSY status bit is reset, and the rest of the status bits are unchanged. If the Force interrupt command is received when there is not a current command under execution, the BUSY Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)

7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4-8. Descriptions of the various bits are contained in Tables 4-9 and 4-10.

Table 4-8. Status Register Summary

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

Table 4-9. Status Bits for Type I Commands

BIT NAME	MEANING
S7 Not Ready	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the READY input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2 Track 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
SO BUSY	When set command is in progress. When reset no command is in progress.

Table 4-10. Status Bits for Type II and III Commands

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the READY input and 'ored' with MR. The TYPE II and III Commands will not execute unless the drive is ready.
S6 RECORD TYPE/ WRITE PROTECT	On read Record: It indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.

Table 4-10 (Cont.). Status Bits for Type II and III Commands

BIT NAME	MEANING
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
SO BUSY	When set, command is under execution. When reset, no command is under execution.

4.2.1.10 FORMATTING THE DISK.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the device raises the data request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a clock mark of $(FF)_{16}$. However, if the device detects a data pattern on F7 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by a F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128, 256, 512, or 1024 bytes, or may be formatted in non-IBM 3740 with sectors length of 16 to 4096 bytes in 16 byte increments.

IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes/sector. The next section deals with the IBM 3740 format with 128 bytes/sector and the following section details non-IBM formats.

IBM 3740 Formats - 128 Bytes/Sector. Shown in Figure 4-8, is the IBM format with 128 bytes/sector. In order to format this format, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	40	00 or FF
	6	00
	1	FC (Index Mark)
	26	00 or FF
*	6	00
	1	FE (ID Address Mark)
	1	Track Number (0 thru 4C)
	1	00
	1	Sector Number (1 thru 1A)
	1	00
	1	F7 (2 CRC's written)
	11	00 or FF
	6	00
	1	FB (Data Address Mark)
	128	Data (IBM uses E5)
	1	F7 (2 CRC's written)
	27	00 or FF
	247**	00 or FF

* Write bracketed field 26 times

** Continue writing until module interrupts out. Approx. 247 bytes.

Non-IBM Formats. Non IBM Formats are very similar to the IBM formats except a different algorithum is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Type II commands with b flag equal to zero. Note that F7 thru FE must not appear in the sector length byte of the ID field.

In formatting the device, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field) must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The device does not require the index address mark (i.e., DATA = FC,CLK = D7) and need not be present.

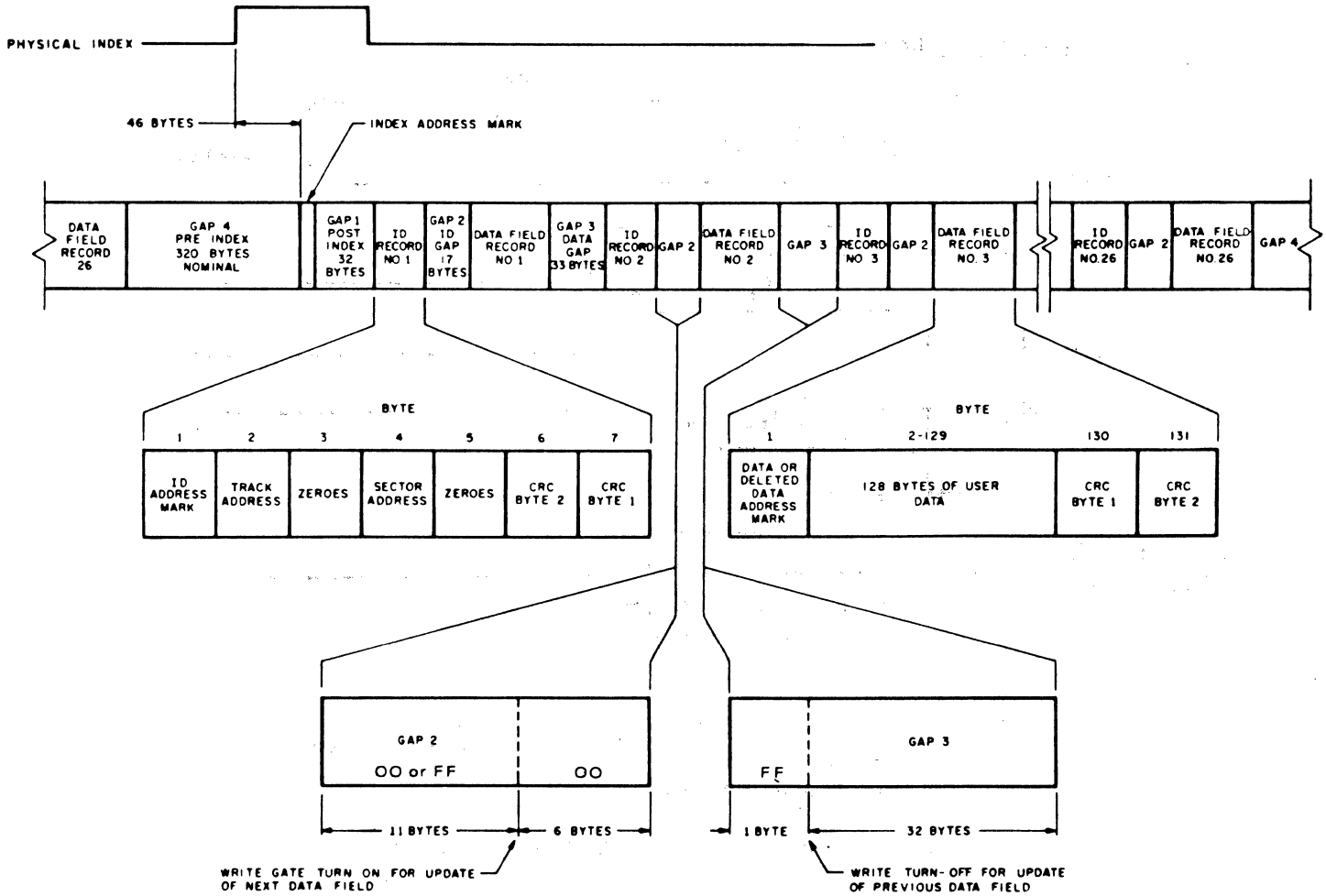


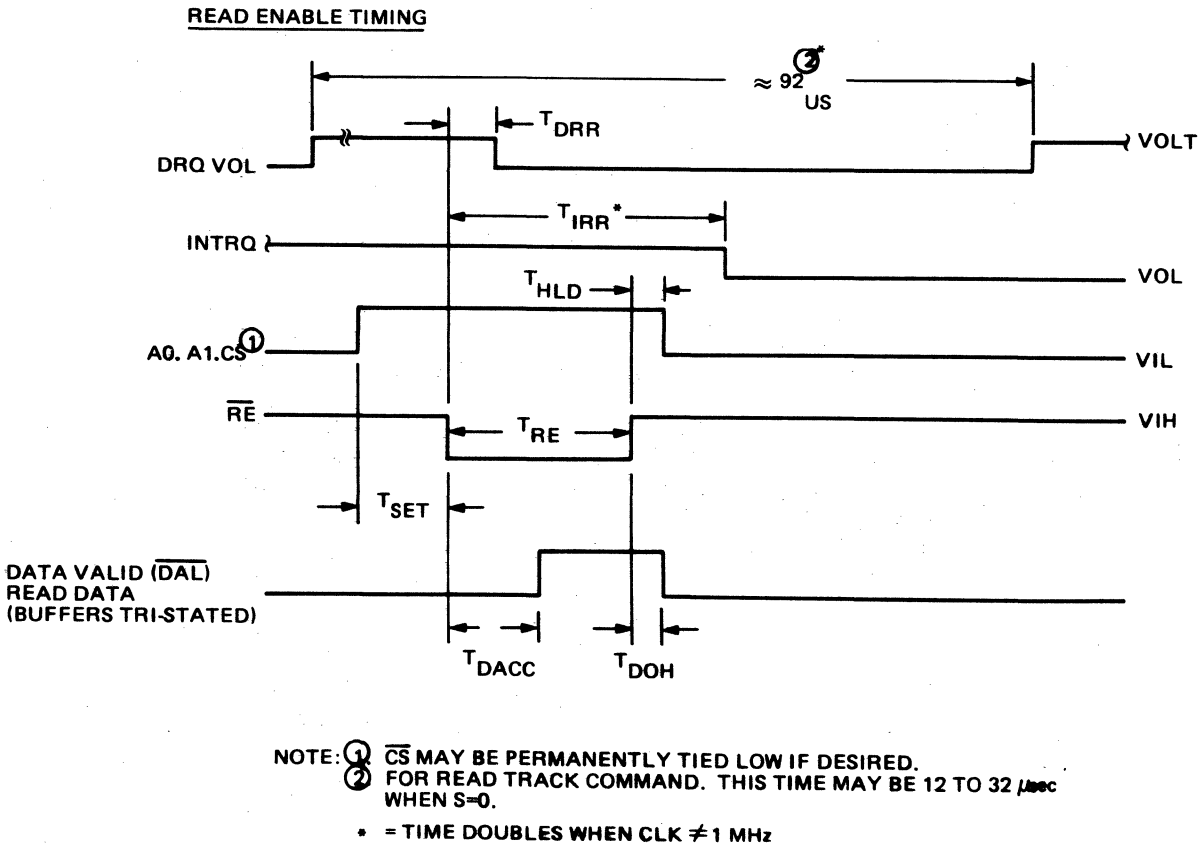
Figure 4-8. Track Format

4.2.1.11 TIMING CHARACTERISTICS.

Timing diagrams with their associated tables of values for the various disk operations are shown in Figures 4-9 through 4-14. In all cases, T_A = 0°C, to 70°C, V_{DD} = +12V ±.6V, V_{BB} = -5 ±.25V, V_{SS} = OV, V_{CC} = +5 ±.25V.

Timings are given for 2MHZ clock. For those timings noted, values will double when chip is operated at 1MHZ. Use 1MHZ when using mini-floppy.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	500			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$			150	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L= 25 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 25 pf

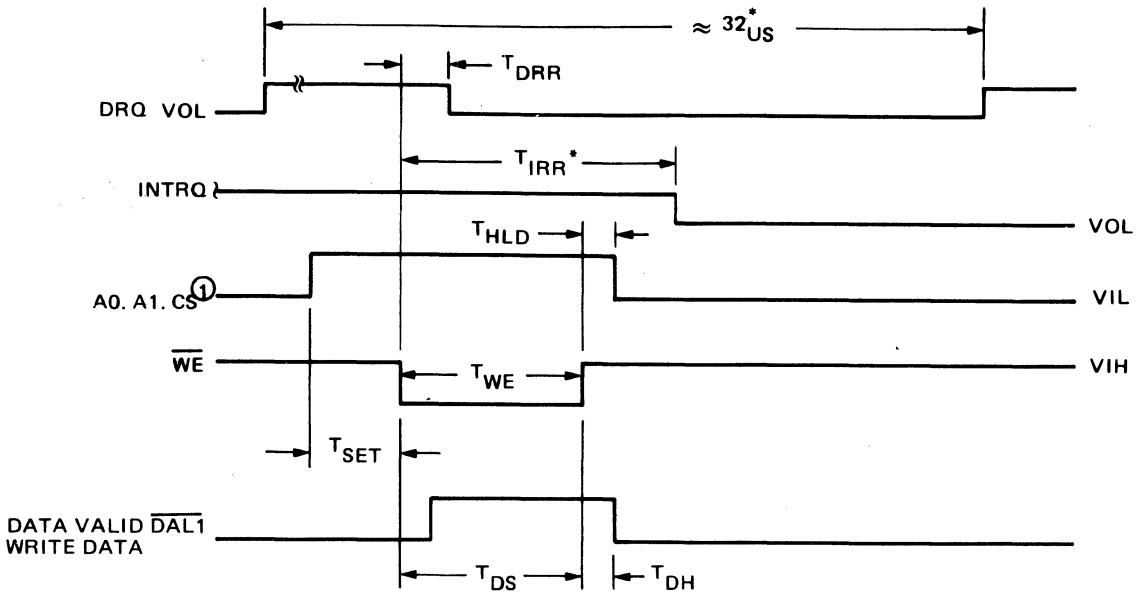


NOTE: ① $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
② FOR READ TRACK COMMAND. THIS TIME MAY BE 12 TO 32 μsec WHEN S=0.
* = TIME DOUBLES WHEN CLK ≠ 1 MHz

Figure 4-9. Read Operations Timing

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$			150	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	150			nsec	

WRITE ENABLE TIMING



NOTE: ① $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. WHEN WRITING DATA INTO SECTOR, TRACK, OR DATA REGISTER, USER CANNOT READ THIS REGISTER UNTIL AT LEAST 8 μSEC AFTER THE RISING EDGE OF $\overline{WE}$ WHEN WRITING INTO THE COMMAND REGISTER. STATUS IS NOT VALID UNTIL SOME 12 μSEC LATER. THESE TIMES ARE DOUBLED WHEN CLK = 1 MHZ.

* = TIME DOUBLES WHEN CLK = 1 MHZ

Figure 4-10. Write Operations Timing

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TPWX	Pulse Width Rd Data & Rd Clock	150		350	nsec	
TCX	Clock Cycle Ext	2500			nsec	
TDEX	Data to Clock	500			nsec	
TDDX	Data to Data Cycle	2500			nsec	

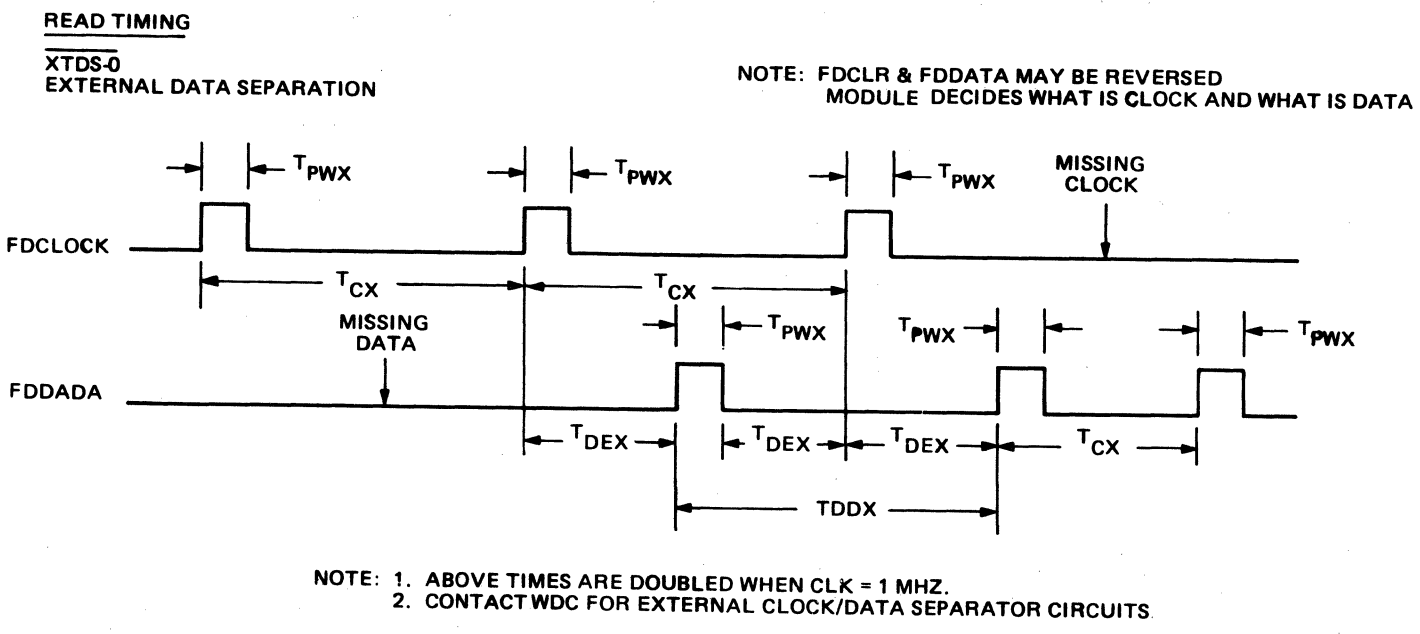
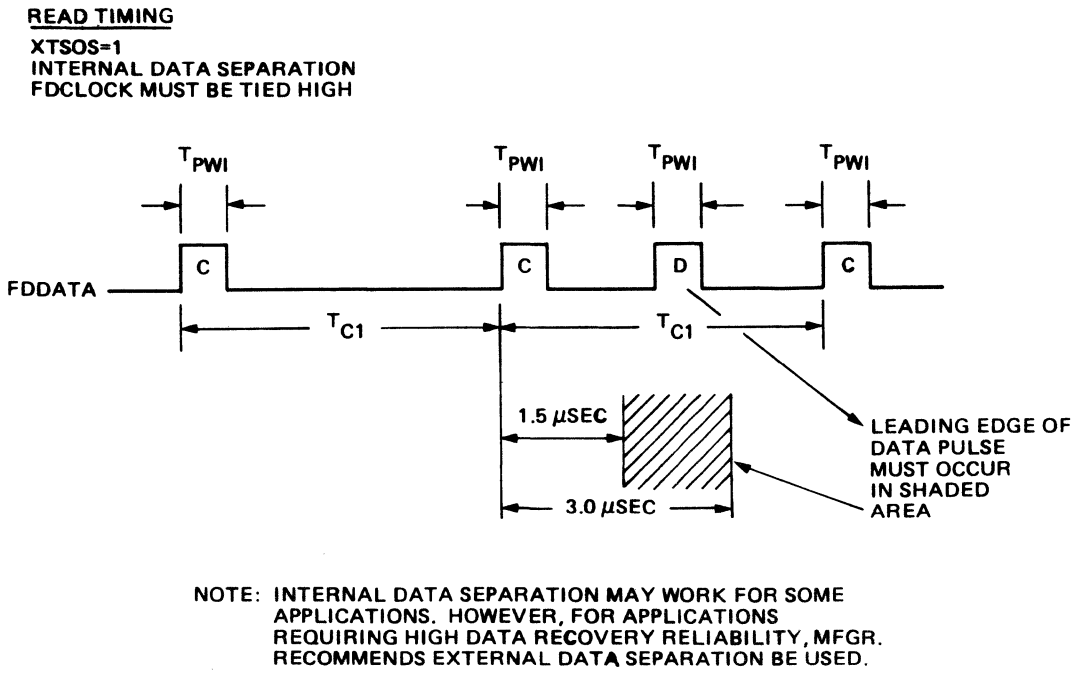


Figure 4-11. External Data Separation Timing ($\overline{XTDS}$=0)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TPWI	Pulse Width Data & Clock	150		1000	nsec	
TCI	Clock Cycle Internal	3500		5000	nsec	



NOTE: INTERNAL DATA SEPARATION MAY WORK FOR SOME APPLICATIONS. HOWEVER, FOR APPLICATIONS REQUIRING HIGH DATA RECOVERY RELIABILITY, MFGR. RECOMMENDS EXTERNAL DATA SEPARATION BE USED.

Figure 4-12. Internal Data Separation Timing ($\overline{\text{XTDS}}$=1)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TWGD	Write Gate to Data		1200		nsec	300 nsec ± CLK tolerance
TPWW	Pulse Width Write Data	500		600	nsec	
TCDW	Clock to Data		2000		nsec	±0.5%± CLK tolerance
TCW	Clock Cycle Write		4000		nsec	±0.5%± CLK tolerance
TWGH	Write Gate Hold to Data	0		100	nsec	

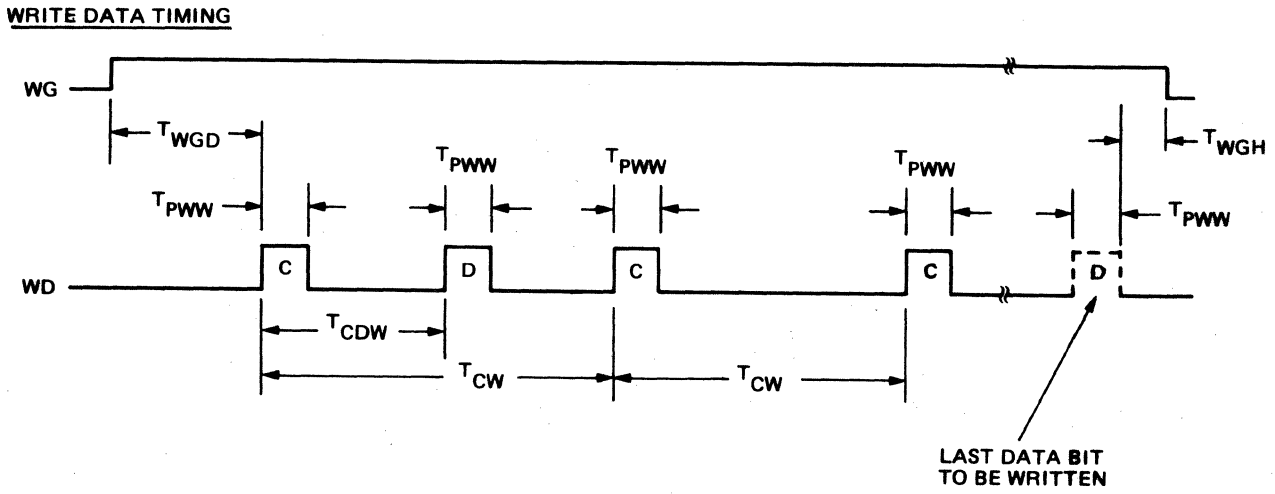


Figure 4-13. Write Data Timing

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TCD_1	Clock Duty	175			nsec	2MHZ ± 1% See Note
TCD_2	Clock Duty	210			nsec	
TSTP	Step Pulse Output	3800		4200	nsec	
TDIR	Dir Setup to Step	24			usec	These times doubled when CLK = 1 MHZ
TMR	Master Reset Pulse Width	10			usec	
TIP	Index Pulse Width	10			usec	
TWF	Write Fault Pulse Width	10			usec	

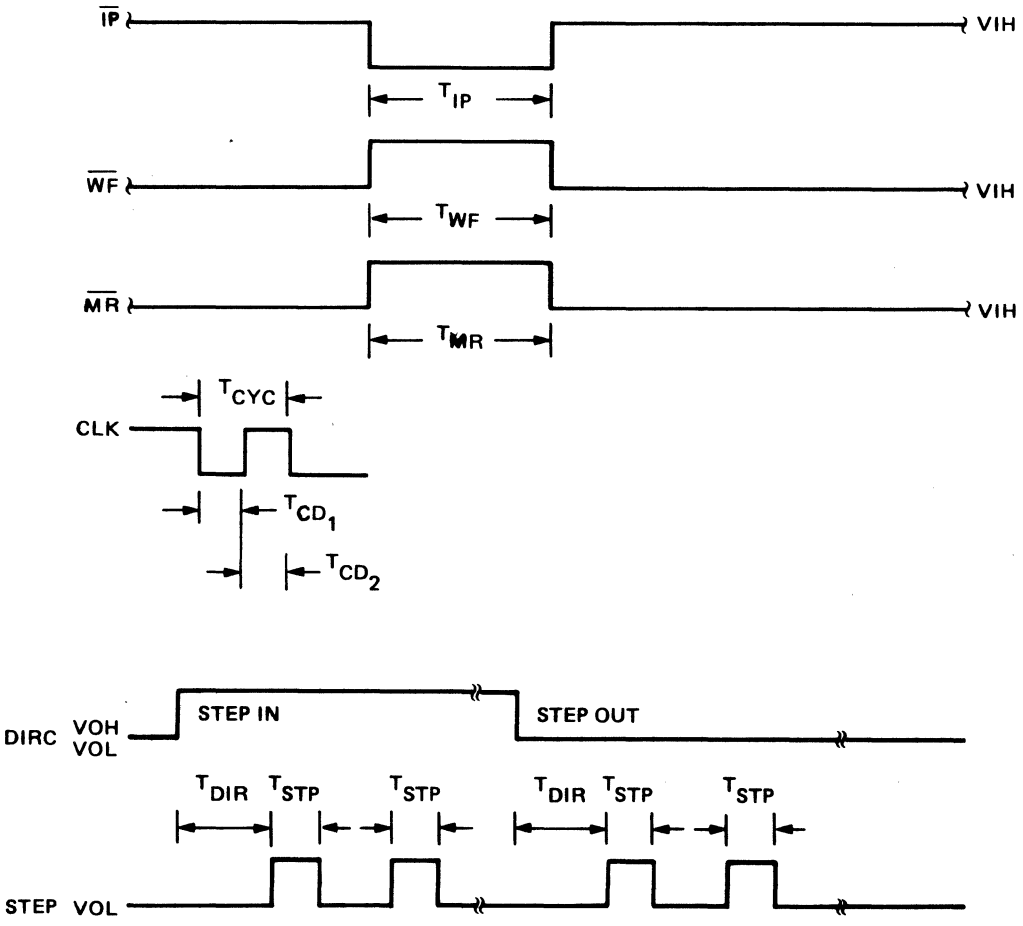


Figure 4-14. Miscellaneous Timing

4.2.2 SYNCHRONOUS UP/DOWN COUNTER WITH DUAL CLOCK (U5, U6, U7, U8, U18, U19, U20, U21).

This device is a synchronous 4-bit binary up/down counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs, while the load input is low. The output changes independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level, independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by

feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

External connections are shown in Figure 4-15, the logic diagram is shown in Figure 4-16, and timing is shown in Figure 4-17.

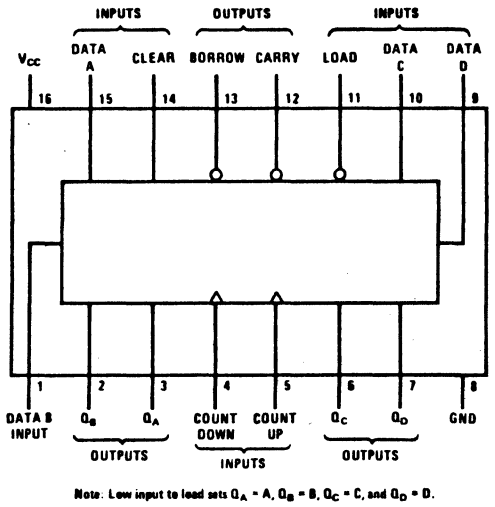


Figure 4-15. Synchronous Up/Down Counter Connections

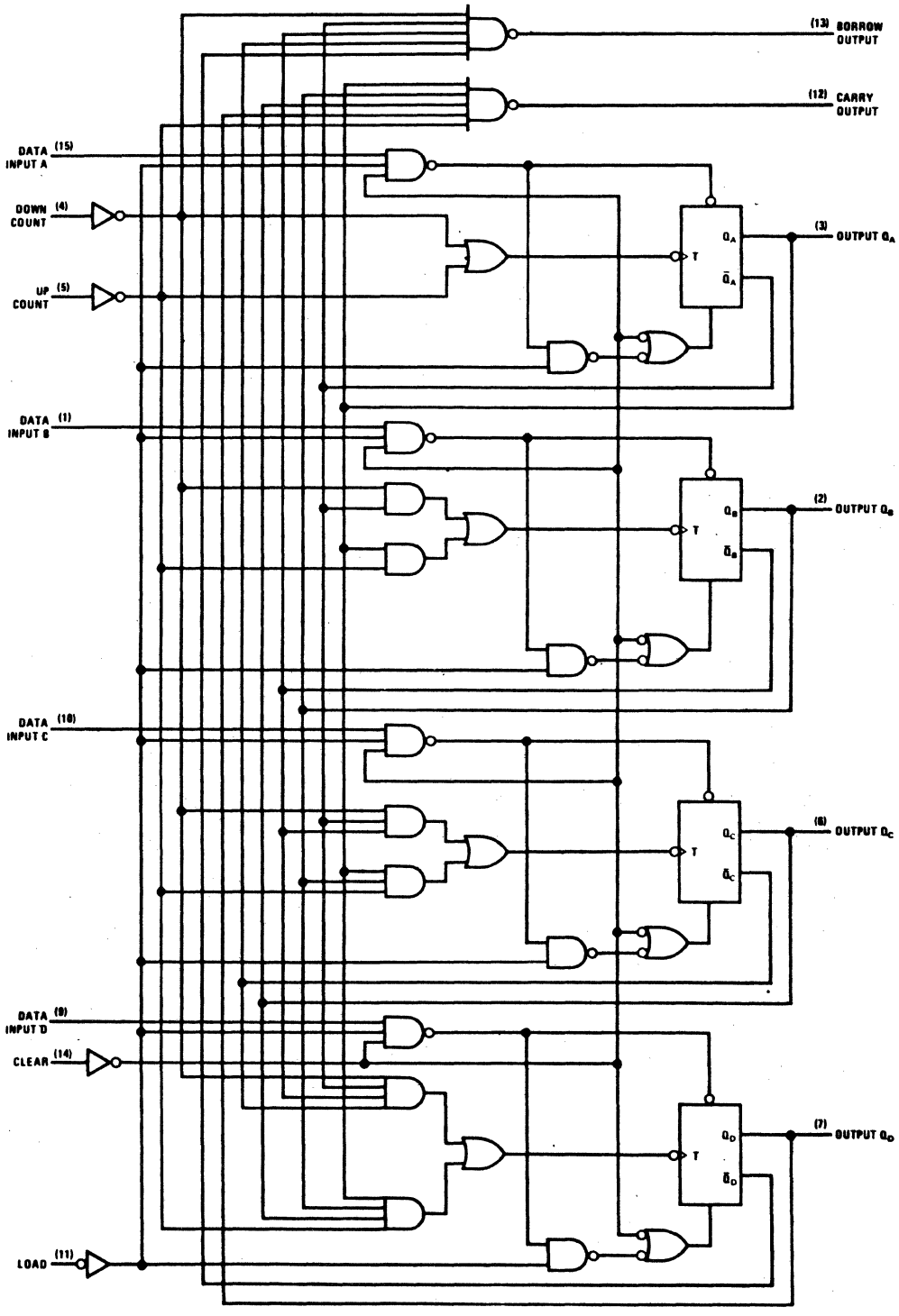
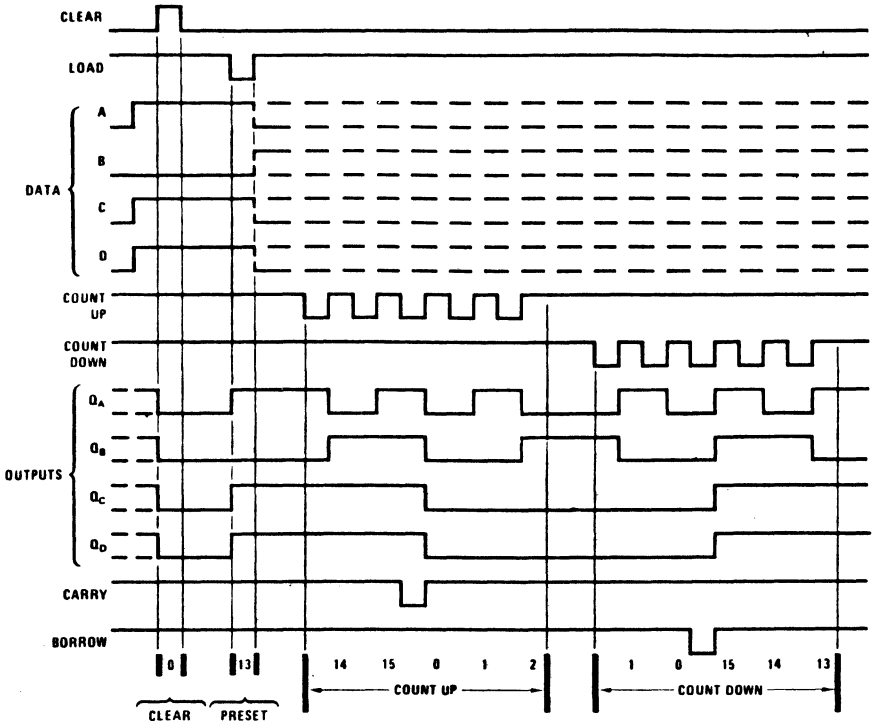


Figure 4-16. Synchronous Up/Down Counter Logic Diagram



Sequence:

(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Notes:

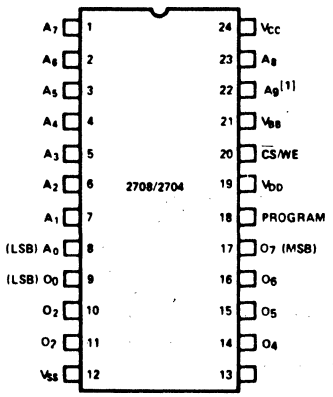
(A) Clear overrides load, data, and count inputs.
(B) When counting up, count-down input must be high; when counting down, count-up input must be high.

Figure 4-17. Synchronous Up/Down Counter Timing Diagram

4.2.3 8K UV ERASABLE PROM (U48).

This device is a 1K x 8 (8192) bit ultraviolet light erasable and electrically reprogrammable EPROM. The outputs are three-state, allowing direct interface with common system bus structures. Device connections are shown in Figure 4-18 and timing is shown in Figure 4-19.

PIN CONFIGURATION

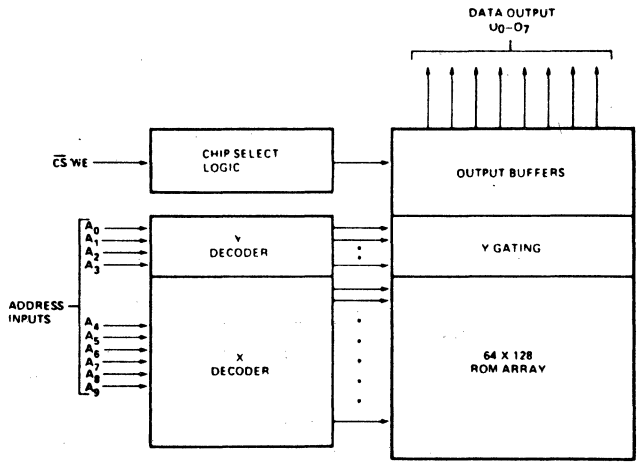


NOTE 1: PIN 22 MUST BE CONNECTED TO V_{SS} FOR THE 2704.

PIN NAMES

A_0 A_9	ADDRESS INPUTS
O_1 O_8	DATA OUTPUTS/INPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

BLOCK DIAGRAM



PIN CONNECTION DURING READ OR PROGRAM

	PIN NUMBER							
MODE	DATA I/O 9-11, 13-17	ADDRESS INPUTS 1-8, 22, 23	V_{SS} 12	PROGRAM 18	V_{DD} 19	$\overline{CS}$/WE 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	V_{IH}	-5	+5
PROGRAM	D_{IN}	A_{IN}	GND	PULSED 26V	+12	V_{IHW}	-5	+5

Figure 4-18. 8K UV Erasable PROM Connections

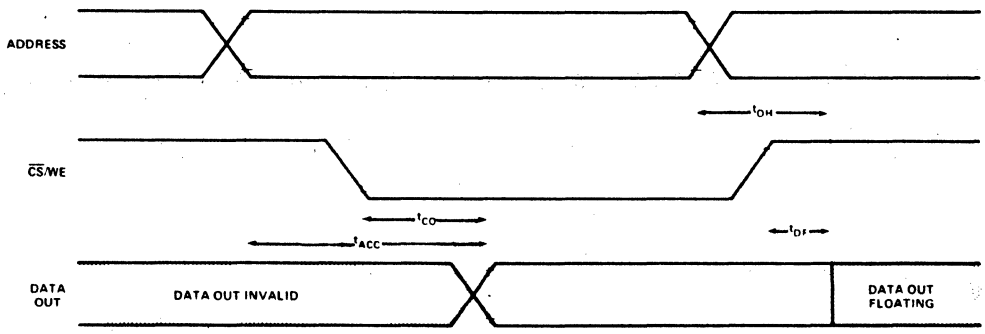


Figure 4-19. 8K UV Erasable PROM Timing

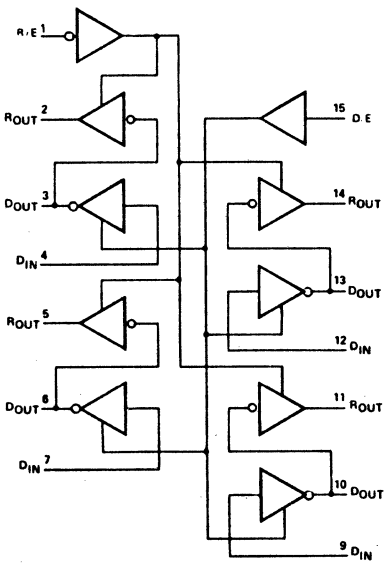
Erasure Characteristics. The erasure characteristics of this device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000A range. Data show that constant exposure to room level fluorescent lighting could erase the typical device in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If this device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available which should be placed over the window to prevent unintentional erasure.

4.2.4 TRI-STATE QUAD BUS TRANSCEIVER (U37, U38, U50, U51). This device consists of four pairs of tri-state logic elements configured as quad bus drivers/receivers along with separate buffered receiver enable and driver enable lines. Both the driver and receiver gates have tri-state outputs and low current PNP inputs.

A logic 1 on the Data Enable (E/E) input allows input data to be transferred to the outputs of the drivers while a logic 0 forces the outputs to a high impedance state and disables the PNP resulting in negligible input load current. The receiver gates are enabled by a logic 0 on the Receiver Enable (R/E) pin and provide 16 in a current sink capability. A logic 1 forces the receiver outputs to a high impedance state and disables the PNP inputs.

Logic and connections are shown in Figure 4-20.

Logic Diagram



VCC = (16)
GND = (8)
( ) = Denotes Pin Numbers

Connection Diagram

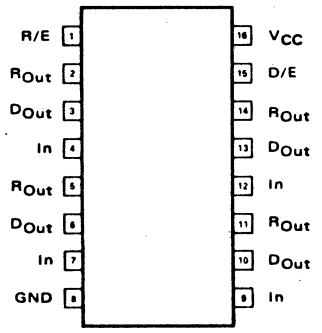
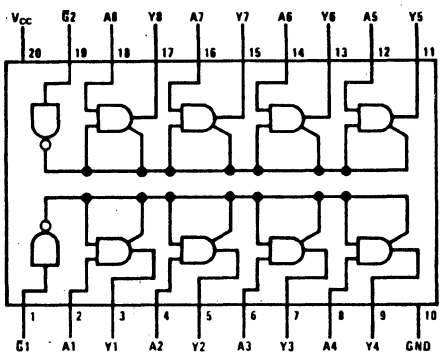


Figure 4-20. Tri-State Bus Transceiver Connections

4.2.5 TRI-STATE OCTAL BUFFERS (U36).

This device provides six, two-input buffers in each package. One of the two inputs is used as a control line to gate the output into a high impedance state, while the other passes the data through the buffer. The outputs are placed in the tri-state condition by applying a high logic level to the control pins. Logic and connections are shown in Figure 4-21.

Logic Diagram



Truth Table

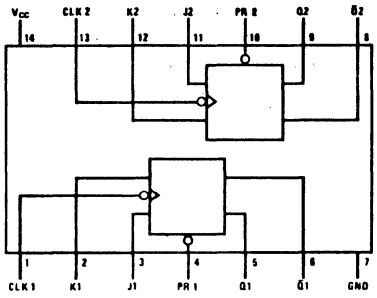
INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

Figure 4-21. Tri-State Octal Buffer Connections

4.2.6 DUAL J-K NEGATIVE-EDGE TRIGGERRED FLIP-FLOPS WITH PRESET (U16, U17, U26, U41).

The J-K Flip-Flop logic and connections are shown in Figure 4-22.

Connection Diagram



Truth Table

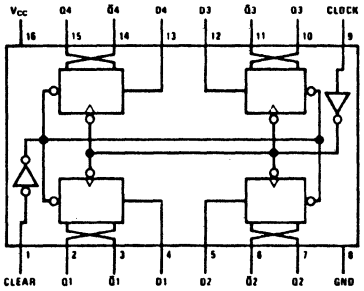
INPUTS				OUTPUTS	
PR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

Figure 4-22. J-K Flip-Flop Connections

4.2.7 QUAD D FLIP-FLOPS WITH CLEAR (U9, U22).

These are positive-edge triggered flip-flops with a direct clear input and complementary outputs. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. Logic and connections are shown in Figure 4-23.

Connection Diagram



Logic Diagram

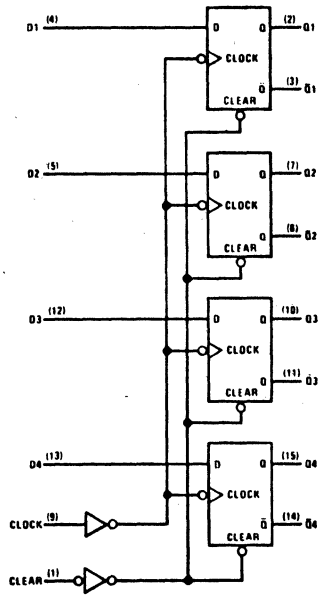
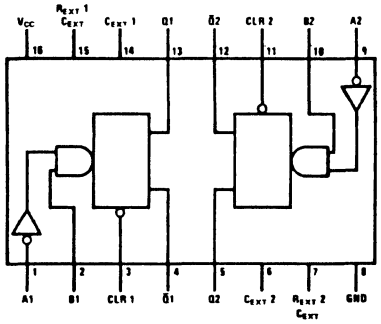


Figure 4-23. Quad D Flip-Flop Connections

4.2.8 DUAL RETRIGGERABLE ONE-SHOTS WITH CLEAR (U15).
One-shot logic and connections are shown in Figure 4-24.



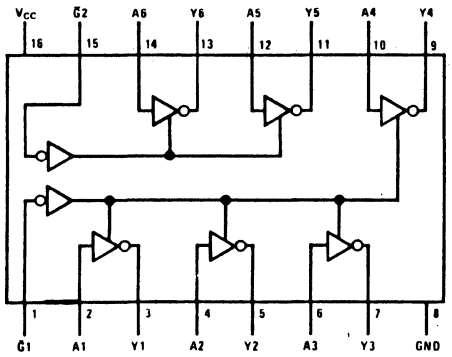
INPUTS			OUTPUTS	
A	B	CLR	Q	$\bar{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎎
↓	H	H	⎍	⎎
X	X	L	L	H

Notes: ⎍ = one high-level pulse, ⎎ = one low-level pulse.
To use the internal timing resistor of 54121/74121, connect R_{INT} to V_{CC}.
An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} (positive).
For accurate repeatable pulse widths, connect an external resistor between R_{EXT}/C_{EXT} and V_{CC} with R_{INT} open-circuited.
To obtain variable pulse widths, connect external variable resistance between R_{INT} or R_{EXT}/C_{EXT} and V_{CC}.

Figure 4-24. One Shot Connections

4.2.9 HEX TRI-STATE BUFFERS (U25).
These devices provide six, two-input buffers in each package. One of the two inputs to each buffer is used as a control line to gate the output onto the high-impedance state, while the other input passes the data through the buffer. The outputs are placed in the tri-state condition by applying a high logic level to the control pins. Logic and connections are shown in Figure 4-25.

Logic and Connection Diagram



Truth Table

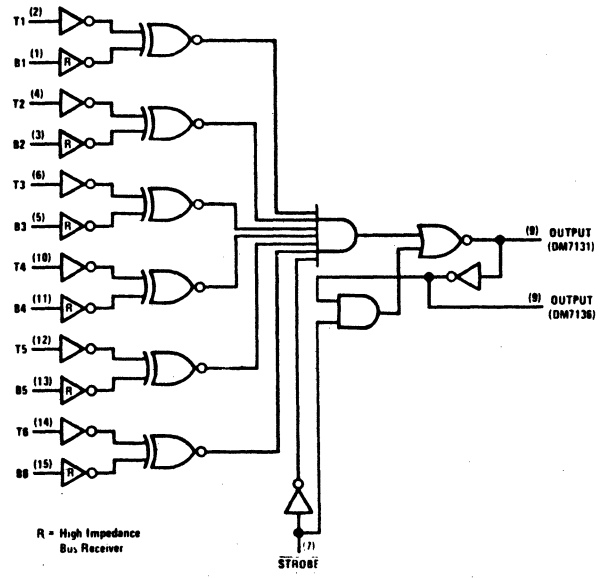
INPUTS		OUTPUT
$\bar{G}$	A	Y
H	X	Hi-Z
L	H	L
L	L	H

Figure 4-25. Hex Tri-State Buffer Connections

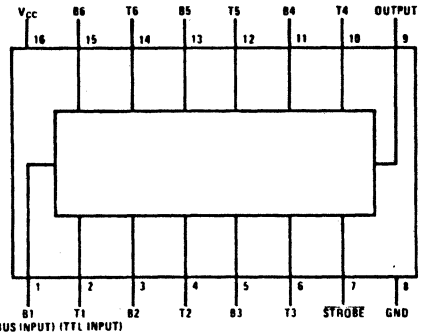
4.2.10 BUS COMPARATOR (U45, U47).

This device compares two binary words of two to six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are TTL inputs, whereas inputs of the second word are high impedance receivers driven by a terminated data bus. The output has a latch that is strobe controlled. The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logical 1 to a logical 0 state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logical 1 level, without affecting the state of the output. Logic and connections are shown in Figure 4-26.

Logic Diagram



Connection Diagram



Truth Table

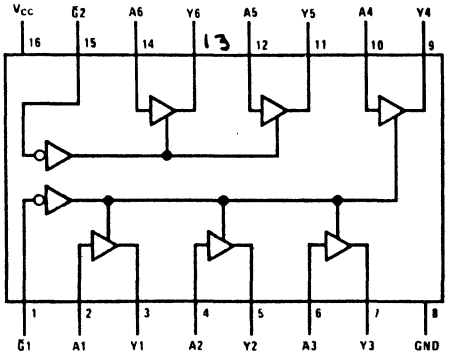
CONDITION	$\overline{\text{STROBE}}$	OUTPUT	
		DM71/8131	DM71/8136
T = B, T ≠ B	H	Q_{N-1}*	Q_{N-1}*
T = B	L	L	H
T ≠ B	L	H	L

*Latched in previous state

Figure 4-26. Bus Comparator Connections

4.2.11 TRI-STATE BUFFERS (U24, U30, U31, U42, U49, U53, U54). These devices provide six, two-input buffers in each package. One of the two inputs to each buffer is used as a control line to gate the output onto the high-impedance state, while the other input passes the data through the buffers. The outputs are placed in the tri-state condition by applying a high logic level to the control pins. Logic and connections are shown in Figure 4-27.

Logic and Connection Diagram



Truth Table

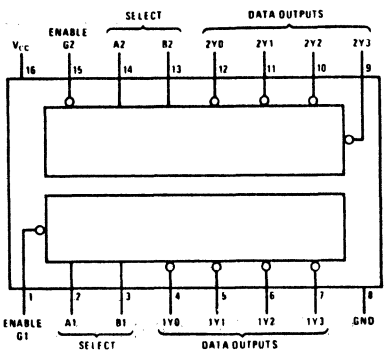
INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Hi-Z
L	H	H
L	L	L

Figure 4-27. Tri-State Buffer Connections

4.2.12 DECODER/DEMULTIPLEXER (U33).

These Schottky-clamped circuits are designed to be used in high performance memory decoding or data routing applications requiring very short propagation delay times. This device contains two separate two-line to four-line decoders in one package. The active-low enable input can be used as a data line in demultiplexing applications. The device features fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high performance Schottky diodes to suppress line ringing. Logic and connections are shown in Figure 4-28.

Connection Diagram



Logic Diagram

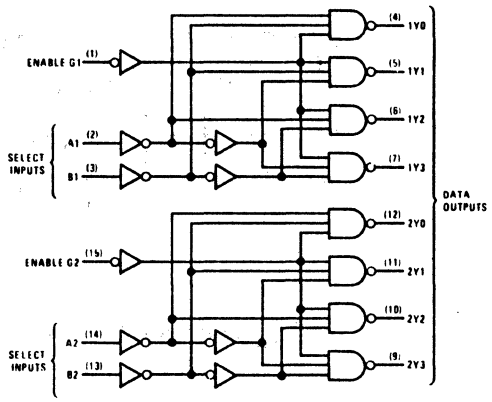


Figure 4-28. Decoder/Demultiplexer Connections

SECTION 5
MAINTENANCE AND TROUBLESHOOTING

5.0 INTRODUCTION.

The AM-200 circuit board performs to full capability with a minimum of maintenance. This section describes maintenance and troubleshooting procedures and procedures for handling warranty returns.

5.1 CIRCUIT BOARD CHECKOUT.

The AM-200 circuit board was fully tested before it left Alpha Micro and will operate satisfactorily in your system if the hardware and software requirements of Sections Two and Three of this manual are met. Should a problem arise after the circuit card has been in operation, use the following procedures to identify and locate the fault.

1. Check all cabling for proper seating of connectors.

2. Check the circuit board for proper seating in the slot.

3. Check all power connections for correct voltages.

4. Check all jumper options to ensure correctness for your application.

5. Verify that the fault is in the AM-200 and not either in the system or in the peripherals. This can best be accomplished with substitution of a known good circuit board if available. If spare circuit boards are not available, the procedures in paragraph 5.2 will help locate the fault.

5.2 TROUBLESHOOTING PROCEDURES.

Several units of the system must operate together with the AM-200 so it may be difficult to determine if the fault is in the AM-200 board, CPU, memory boards, or disk drive. Substitute known good units wherever possible to localize the fault to one of these units.

When it is certain that the AM-200 board is faulty, determine if the entire circuit board has failed or if parts are still operating.

5.2.1 COMPLETE AM-200 FAILURE.

If the CPU seems to be functioning and the disk drive is turned on and seems to be operating but the AM-200 will not boot load, read or write, perform the following checks first:

1. Check the power supply voltages as shown on sheet 1 of the schematic.

2. Check the Ø2 clock input at J1 pin 24.

3. Check the S-100 bus input control signals as described in Table 2-2. Verify that other circuit boards on the same S-100 bus are operating satisfactorily.

5.2.2 PARTIAL FAILURE.

If the circuit board is failing in only part of its operational capabilities, use the following procedures to locate the fault.

If the AM-200 does not boot load but operates the disk drive, perform the following checks:

1. Check pin 20 of the 8K PROM (U48). This should be low to enable the PROM and to enable the output drivers

(schematic sheet 6). If this is faulty, trace back through U40 and U35 to address comparator U47.

2. If the PROM enable is correct, check the address lines to the PROM for a valid address. If all PROM inputs are correct, the PROM DIP is probably faulty.

If the AM-200 boot loads but does not operate the disk drive properly, perform the following checks:

1. Check the addressing comparator output $\overline{\text{BOARDSEL}}$ at pin 9 of U45 (schematic sheet 5). Pin 9 should be low when the board is addressed.

2. Check the DMA Grant signals jumper selected from the S-100 bus (schematic sheet 8). These signals enable the operation of most of the logic on the board.

3. Check the enable inputs to the disk controller DIP U12 (schematic sheet 9). Particularly $\overline{\text{WE}}$, $\overline{\text{RE}}$, and $\overline{\text{CE}}$. Signal $\overline{\text{CE}}$ must be low for DIP operation and $\overline{\text{WE}}$ and $\overline{\text{RE}}$ for write and read operations.

4. Check the data and clock inputs from the disk drive and their control signals. Disk drive signals are described in Table 2-3 and timing diagrams for disk operation are contained in Figures 4-8 through 4-13.

5. If the disk drive operates but data will not transfer correctly, check the DMA address register (schematic sheet 3) and the subsector counter logic (schematic sheet 4). Operation of this logic is described in Section 4.1.4 and 4.1.5.

6. If the AM-200 will perform some commands but not others, check the external control register logic (schematic sheet 2). Ensure that the CPU is sending the desired command and then check the corresponding output of the control register (U22). Data and operation of the control register is described in paragraph 4.1.3.

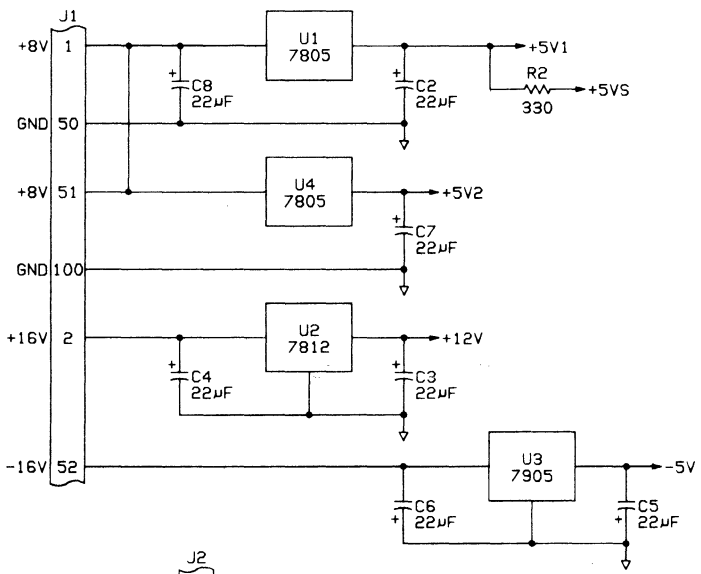
5.3 WARRANTY PROCEDURES.

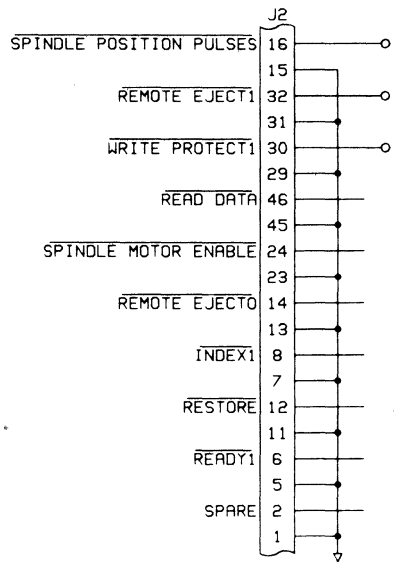
This circuit board is covered by warranty issued by Alpha Micro-Systems, Irvine, California. Complete details of the warranty are included with the circuit board. Should a problem arise with this circuit board, call your dealer or the Alpha Micro International Support Services Administrator for information.

SECTION 6
SCHEMATIC AND PARTS LIST

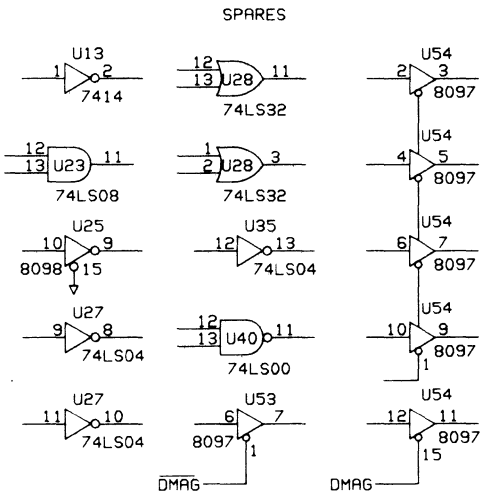
APPR	DATE	EN NO.	DESCRIPTION	LEVEL	
				IS	WAS
	11-30-78	00016	PHANTOM MOD	B02	B00
	12-6-78	00018	SHUGART REL	B03	B02

POWER





SPARES



TABULATION	
DASH#	VARIATION
-01	PERSCI COMPATABLE
-02	WANGGO/SHUBART COMP

2. CAPACITORS ARE IN MICROFARADS.
1. RESISTORS ARE IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED

ALPHA MICRO SYSTEMS
IRVINE, CA 92714

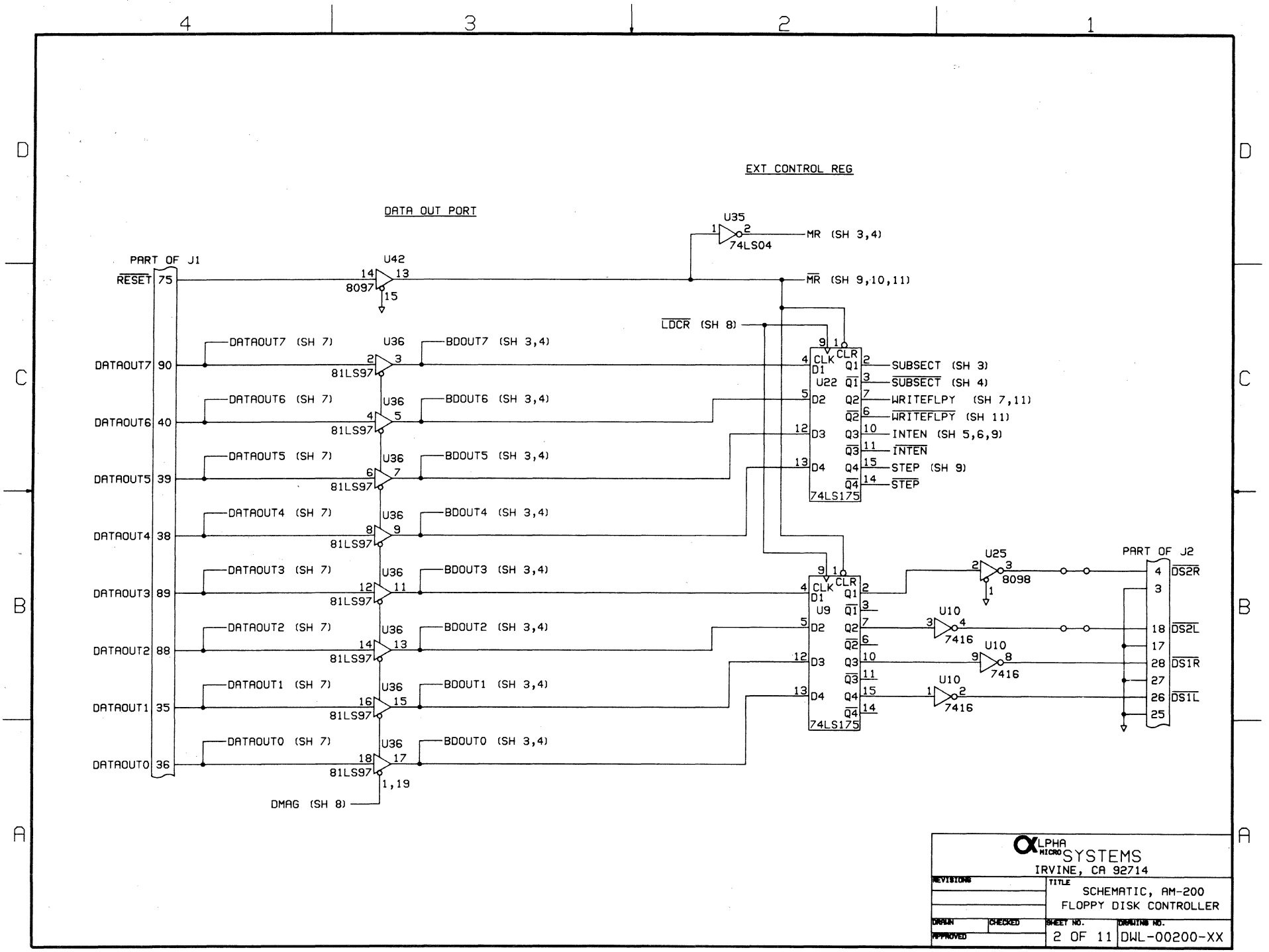
REVISIONS B03 9JAN79

TITLE SCHEMATIC, AM-200 FLOPPY DISK CONTROLLER

DRAWN | CHECKED | APPROVED D WILCOX

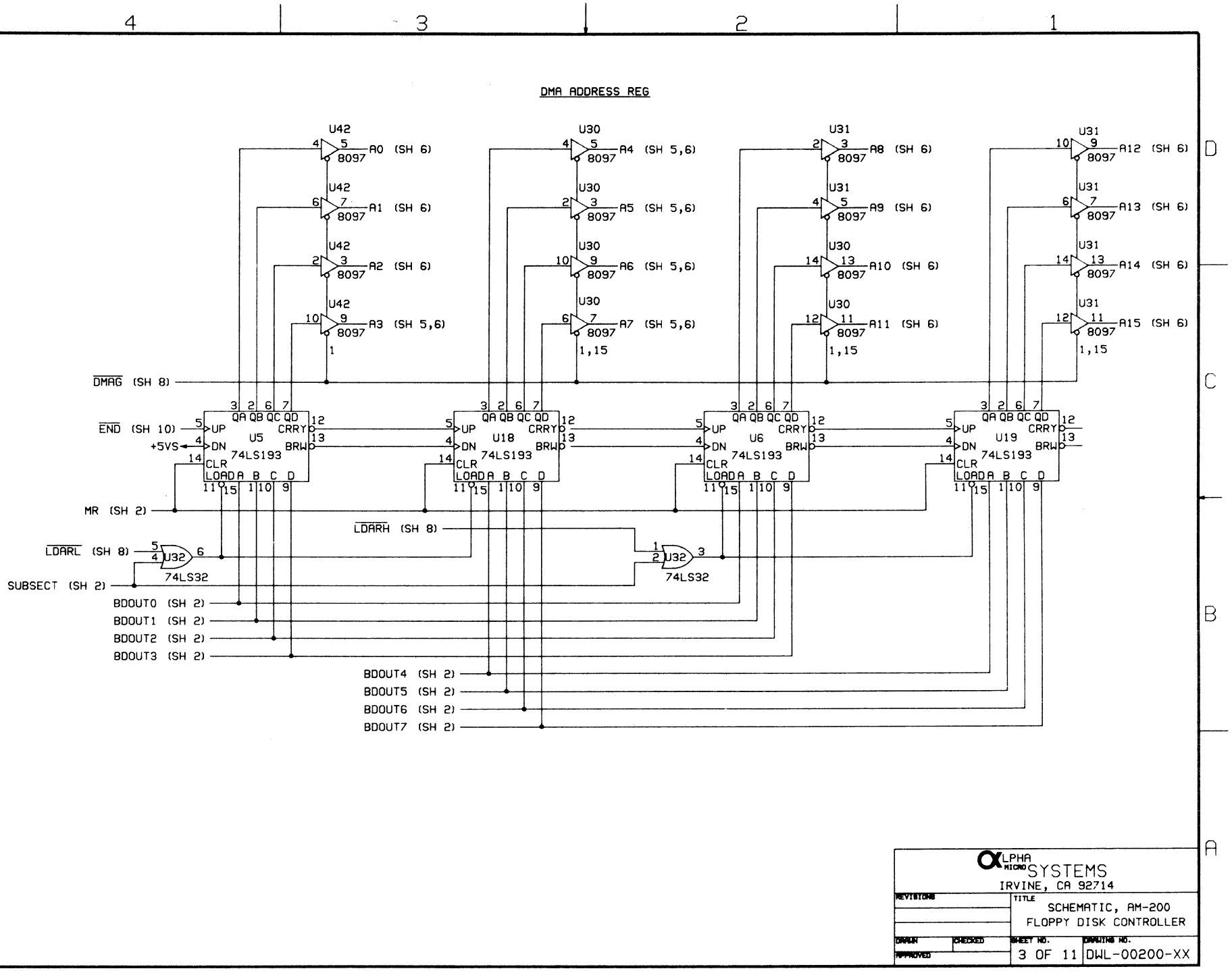
SHEET NO. 1 OF 11

DRAWING NO. DWL-00200-XX



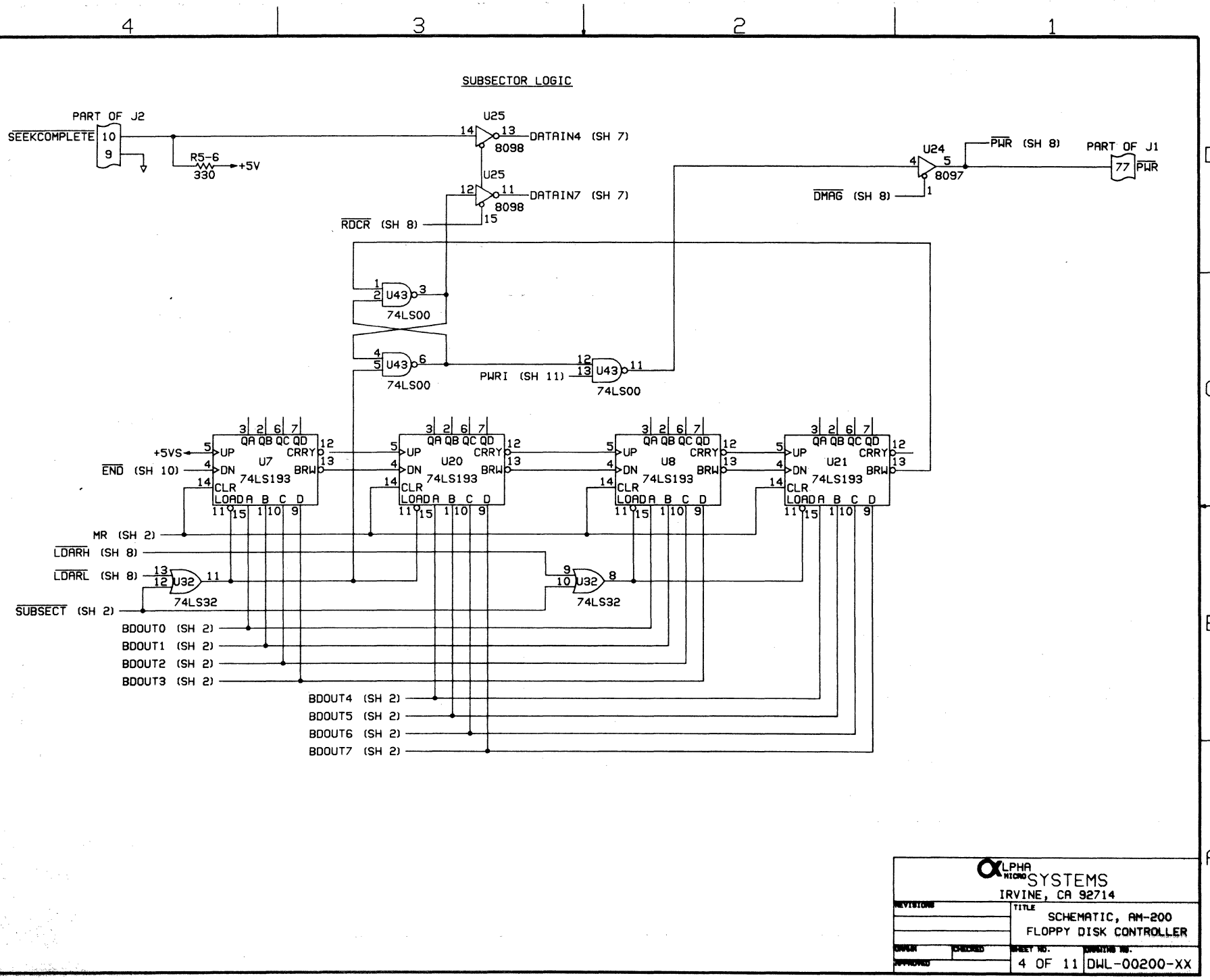
ALPHA MICRO SYSTEMS
IRVINE, CA 92714

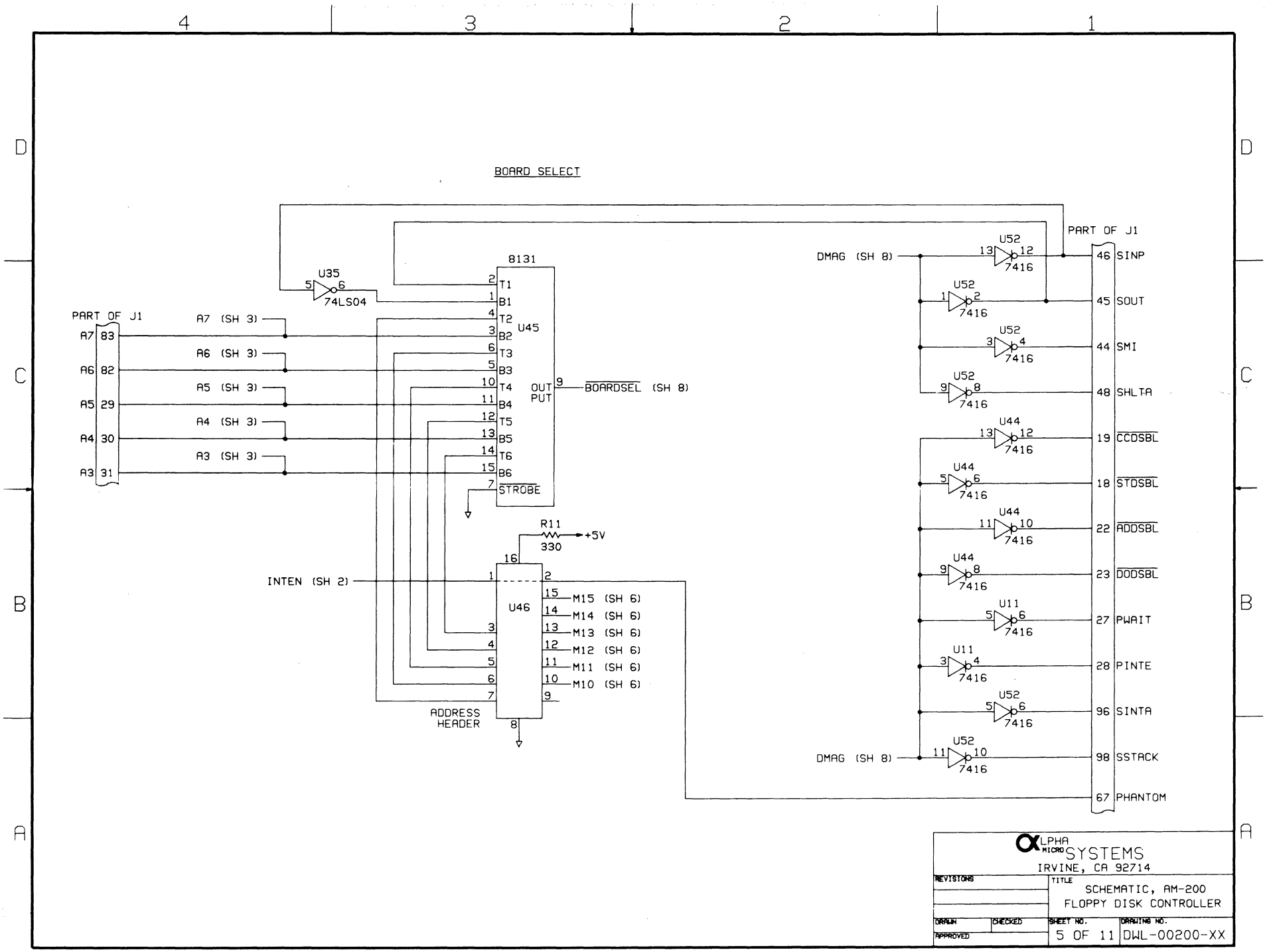
REVISIONS	TITLE	
	SCHEMATIC, AM-200 FLOPPY DISK CONTROLLER	
DRAWN / CHECKED / APPROVED	SHEET NO.	DRAWING NO.
	2 OF 11	DWL-00200-XX

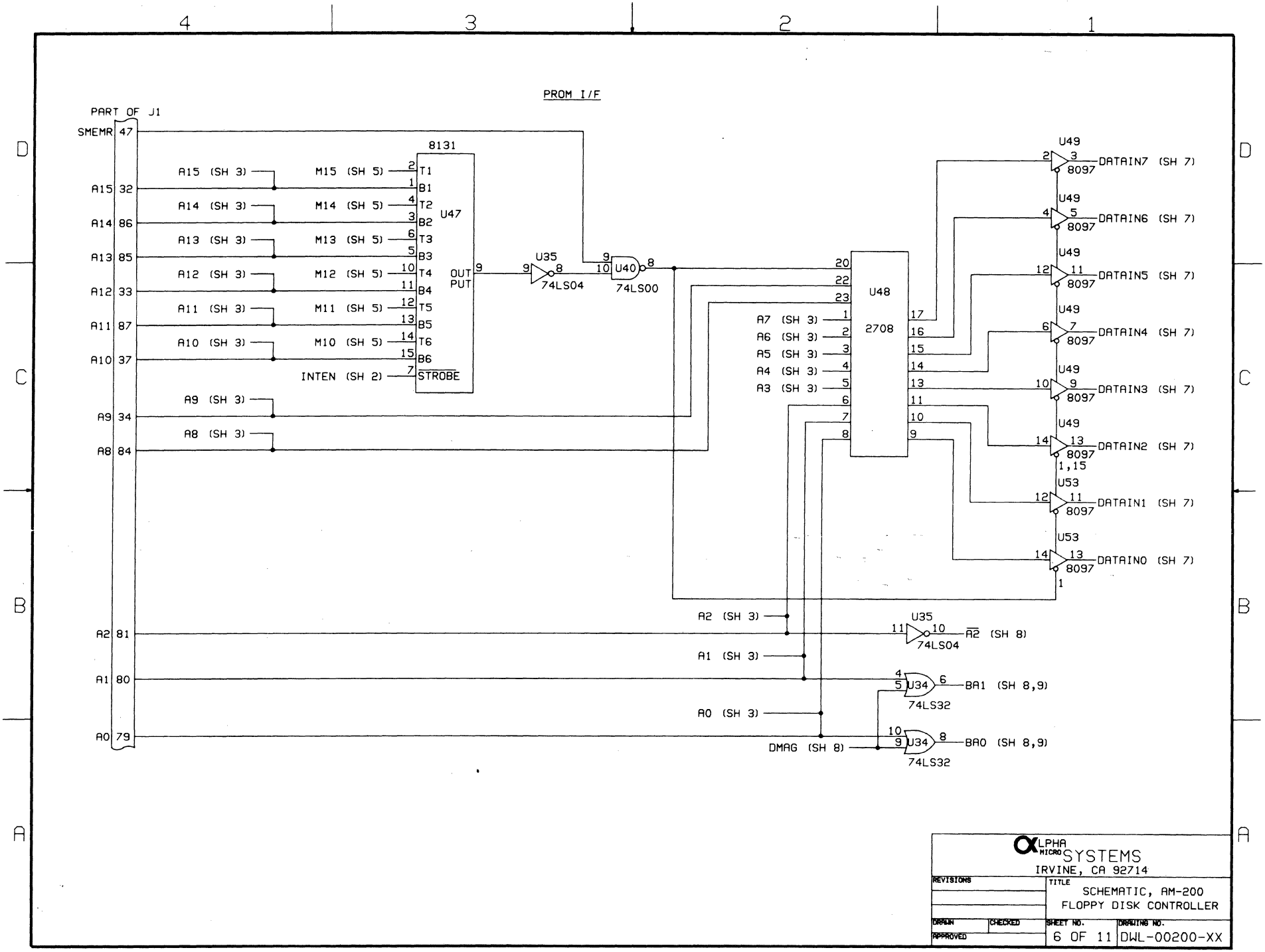


ALPHA MICRO SYSTEMS
IRVINE, CA 92714

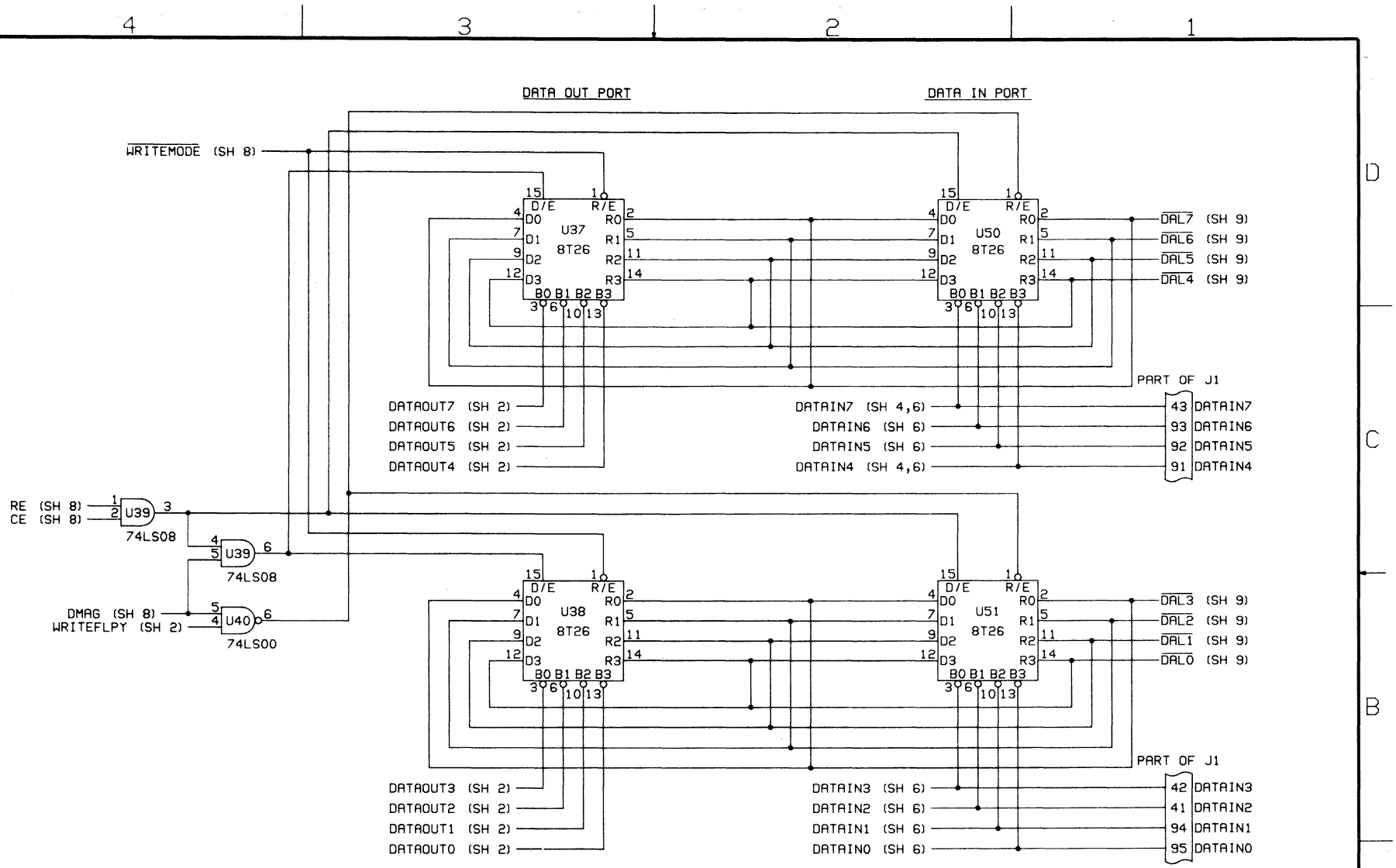
REVISIONS	TITLE	
	SCHEMATIC, AM-200 FLOPPY DISK CONTROLLER	
DRAWN / CHECKED / APPROVED	SHEET NO.	DRAWING NO.
	3 OF 11	DWL-00200-XX


SUBSECTOR LOGIC
PART OF J2
SEEKCOMPLETE
R5-6
330
+5V
U25
8098
DATAIN4 (SH 7)
DATAIN7 (SH 7)
RDCR (SH 8)
U24
8097
PWR (SH 8)
PART OF J1
77 PWR
DMAG (SH 8)
U43
74LS00
PWRI (SH 11)
+5VS
END (SH 10)
U7
U20
U8
U21
74LS193
MR (SH 2)
LDARH (SH 8)
LDARL (SH 8)
U32
74LS32
SUBSECT (SH 2)
BDOUT0 (SH 2)
BDOUT1 (SH 2)
BDOUT2 (SH 2)
BDOUT3 (SH 2)
BDOUT4 (SH 2)
BDOUT5 (SH 2)
BDOUT6 (SH 2)
BDOUT7 (SH 2)
ALPHA MICRO SYSTEMS
IRVINE, CA 92714
REVISIONS
TITLE
SCHEMATIC, AM-200
FLOPPY DISK CONTROLLER
DRAWN
CHECKED
APPROVED
SHEET NO.
4 OF 11
DRAWING NO.
DWL-00200-XX


BOARD SELECT
PART OF J1
A7 83
A6 82
A5 29
A4 30
A3 31
A7 (SH 3)
A6 (SH 3)
A5 (SH 3)
A4 (SH 3)
A3 (SH 3)
U35
74LS04
8131
U45
T1
B1
T2
B2
T3
B3
T4
B4
T5
B5
T6
B6
STROBE
OUTPUT
BOARDSEL (SH 8)
R11
330
+5V
INTEN (SH 2)
U46
M15 (SH 6)
M14 (SH 6)
M13 (SH 6)
M12 (SH 6)
M11 (SH 6)
M10 (SH 6)
ADDRESS HEADER
PART OF J1
DMAG (SH 8)
U52
7416
U44
7416
U11
7416
46 SINP
45 SOUT
44 SMI
48 SHLTA
19 CCDSBL
18 STDSBL
22 ADDSBL
23 DODSBL
27 PWAIT
28 PINTE
96 SINTA
98 SSTACK
67 PHANTOM
ALPHA MICRO SYSTEMS
IRVINE, CA 92714
REVISIONS
TITLE
SCHEMATIC, AM-200
FLOPPY DISK CONTROLLER
DRAWN
CHECKED
APPROVED
SHEET NO.
5 OF 11
DRAWING NO.
DWL-00200-XX

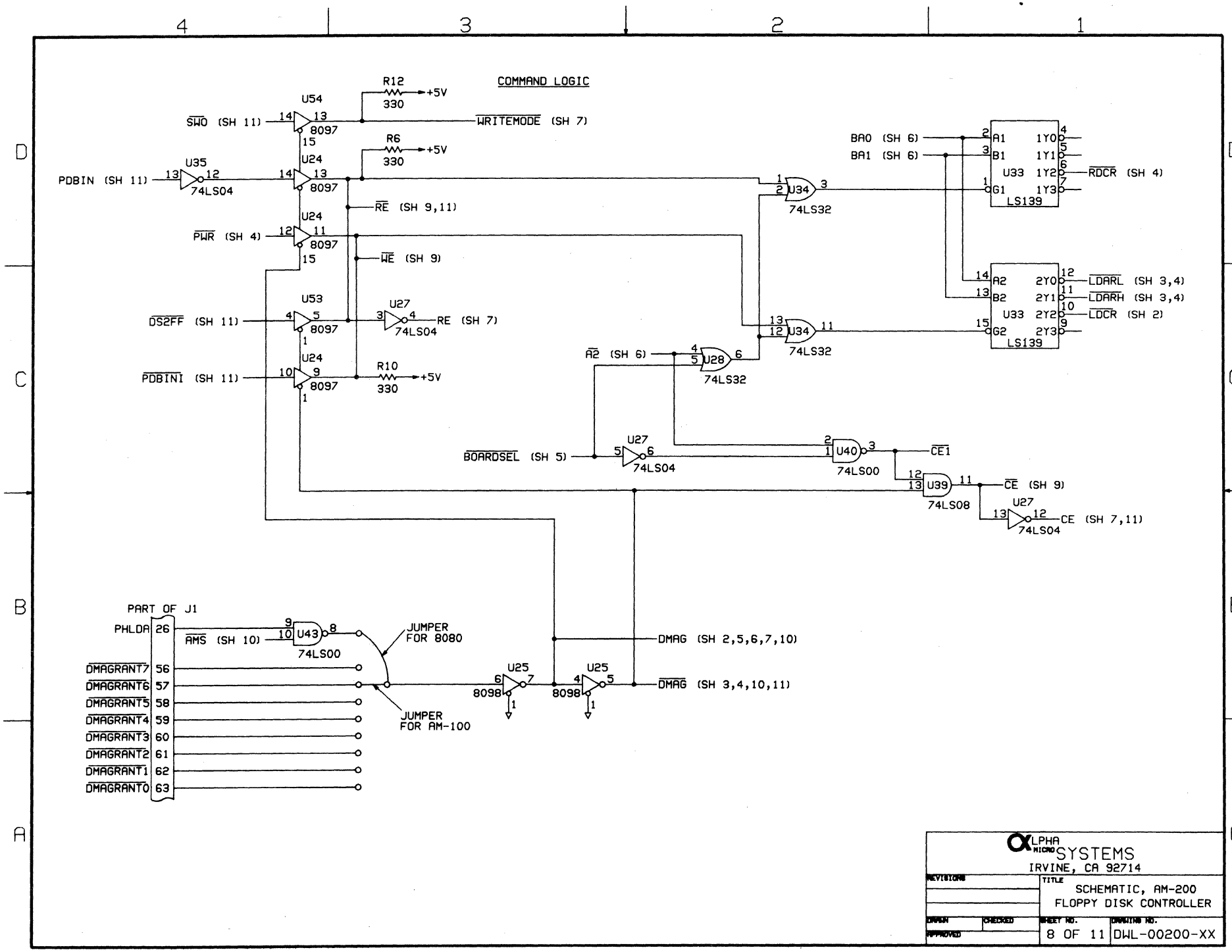


ALPHA MICRO SYSTEMS IRVINE, CA 92714	
REVISIONS	TITLE SCHEMATIC, AM-200 FLOPPY DISK CONTROLLER
DRAWN / CHECKED / APPROVED	SHEET NO. 6 OF 11
	DRAWING NO. DWL-00200-XX



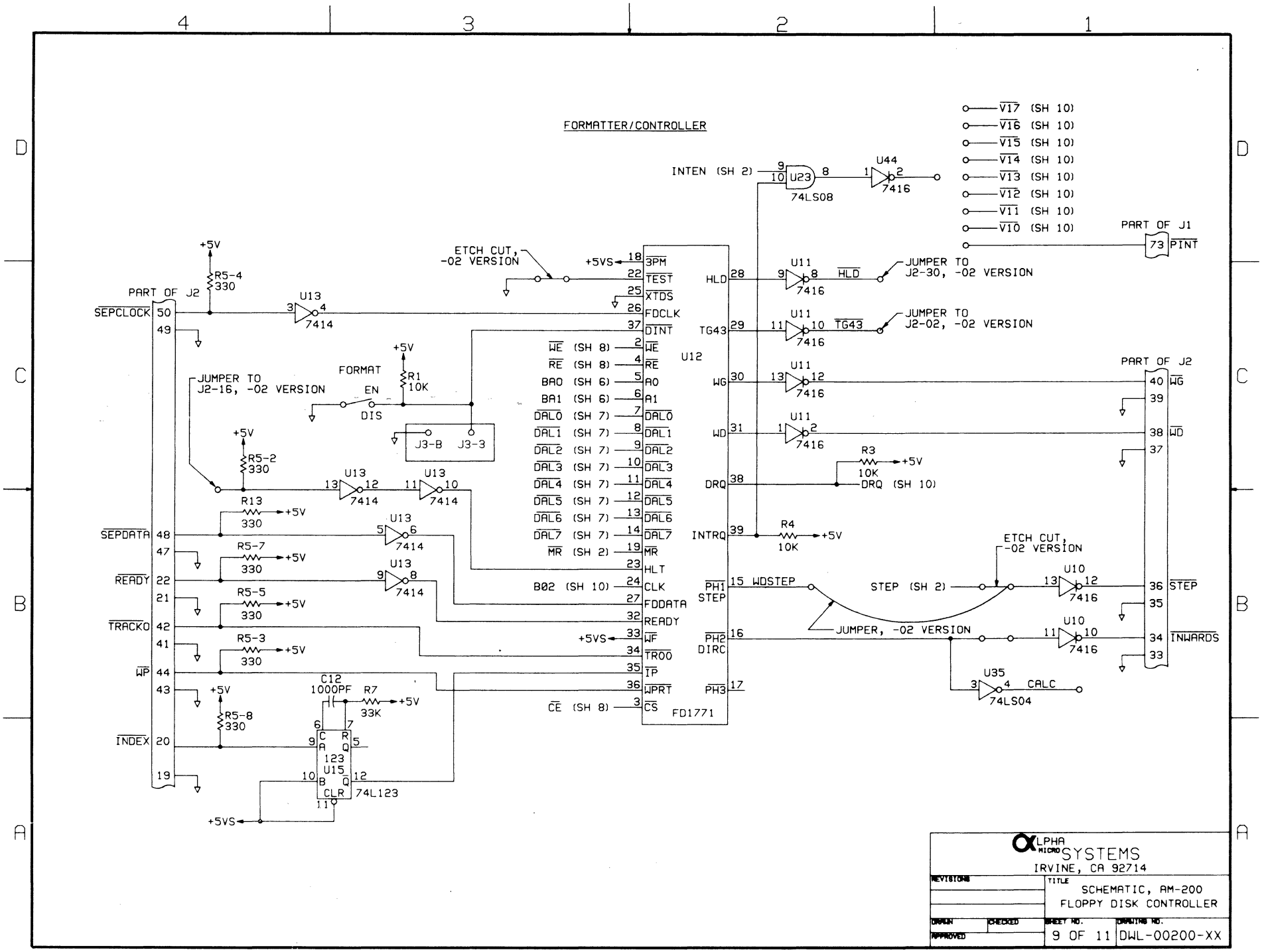
ALPHA MICRO SYSTEMS
IRVINE, CA 92714

REVISIONS	TITLE	
	SCHEMATIC, AM-200 FLOPPY DISK CONTROLLER	
DRAWN / CHECKED / APPROVED	SHEET NO.	DRAWING NO.
	7 OF 11	DWL-00200-XX

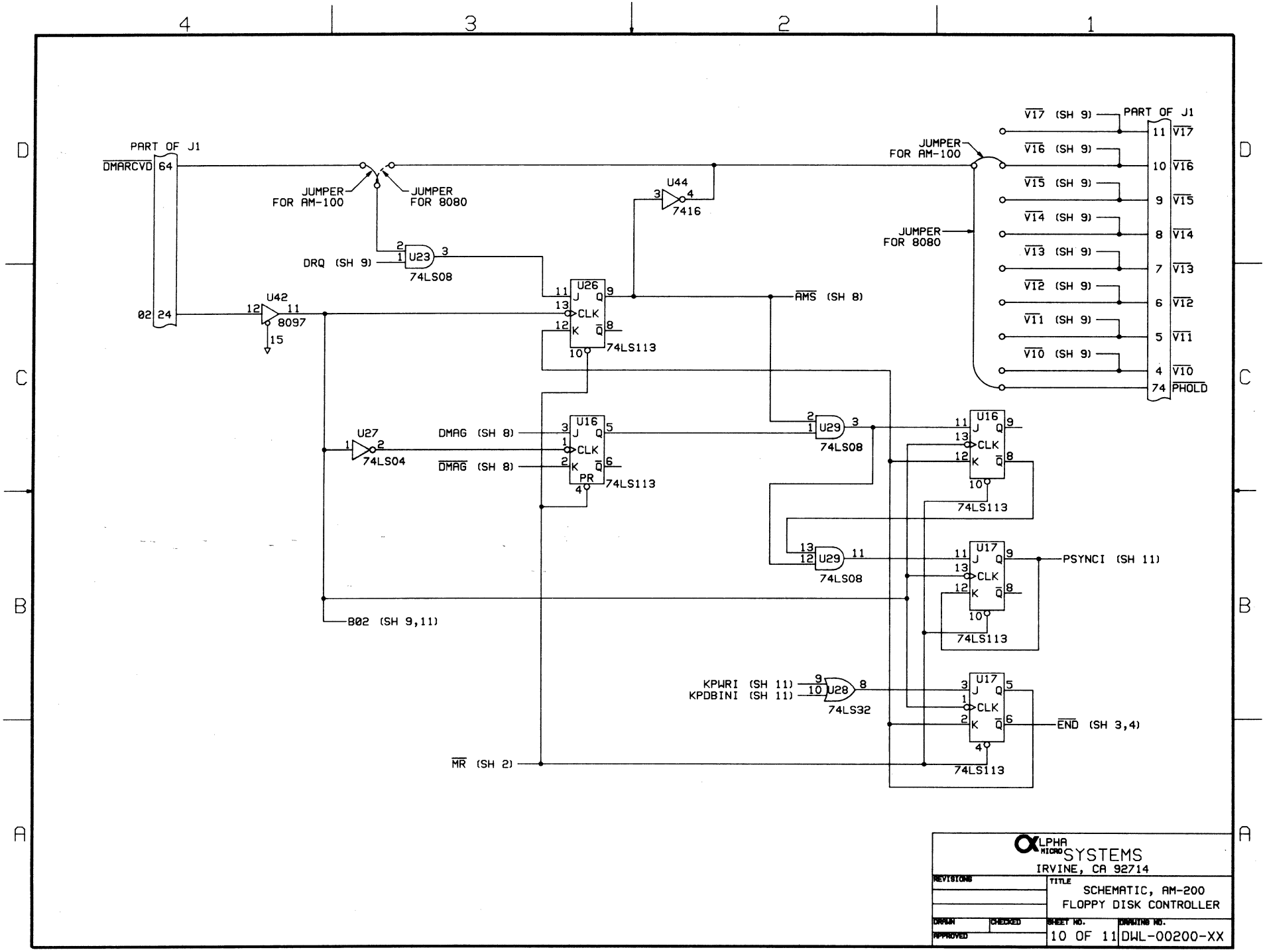


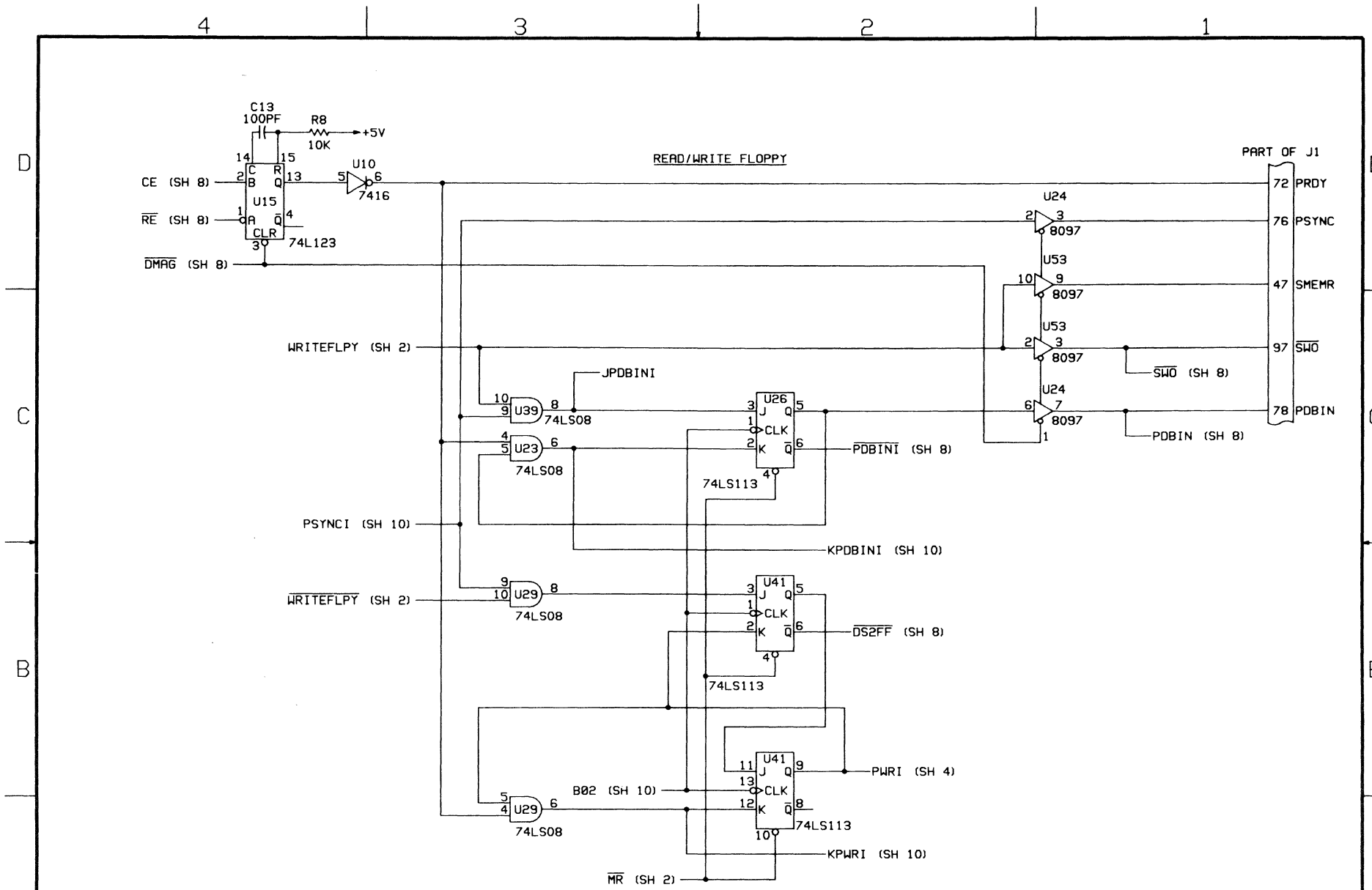
ALPHA MICRO SYSTEMS
IRVINE, CA 92714

REVISIONS	TITLE	
	SCHEMATIC, AM-200 FLOPPY DISK CONTROLLER	
DRAWN / CHECKED / APPROVED	SHEET NO.	DRAWING NO.
	8 OF 11	DWL-00200-XX



ALPHA MICRO SYSTEMS IRVINE, CA 92714		
REVISIONS	TITLE: SCHEMATIC, AM-200 FLOPPY DISK CONTROLLER	
DRAWN / CHECKED / APPROVED	SHEET NO. 9 OF 11	DRAWING NO. DWL-00200-XX


PART OF J1
DMARCVD 64
02 24
JUMPER FOR AM-100
JUMPER FOR 8080
DRQ (SH 9)
U23
74LS08
U42
8097
U44
7416
U26
74LS113
AMS (SH 8)
JUMPER FOR AM-100
JUMPER FOR 8080
V17 (SH 9)
V16 (SH 9)
V15 (SH 9)
V14 (SH 9)
V13 (SH 9)
V12 (SH 9)
V11 (SH 9)
V10 (SH 9)
PART OF J1
11 V17
10 V16
9 V15
8 V14
7 V13
6 V12
5 V11
4 V10
74 PHOLD
U27
74LS04
DMAG (SH 8)
DMAG (SH 8)
U16
74LS113
U29
74LS08
U16
74LS113
U29
74LS08
U17
74LS113
PSYNCI (SH 11)
B02 (SH 9,11)
KPWRI (SH 11)
KPDBINI (SH 11)
U28
74LS32
U17
74LS113
END (SH 3,4)
MR (SH 2)
ALPHA MICRO SYSTEMS
IRVINE, CA 92714
REVISIONS
TITLE
SCHEMATIC, AM-200
FLOPPY DISK CONTROLLER
DRAWN
CHECKED
APPROVED
SHEET NO.
10 OF 11
DRAWING NO.
DWL-00200-XX



ALPHA MICRO SYSTEMS
IRVINE, CA 92714

REVISIONS	TITLE
	SCHEMATIC, AM-200 FLOPPY DISK CONTROLLER
DRAWN / CHECKED / APPROVED	SHEET NO. 11 OF 11
	DRAWING NO. DWL-00200-XX

BILL # PDB-00200-01 Retail price $ 0.00

REV.A00 Whsle price $ 0.00

01/04/79 Net price $ 0.00

Description DISK FLOPPY PERSCI AM-200

	PART NUMBER	DESCRIPTION	QTY
1	DWB-00200-01	DISK FLOPPY PERSCI COMPATIBLE	1
2	DWB-00206-00	PROGRAMMING BOOT PROMS PERLOD	1
3	DWS-00200-00	SPEC FLOPPY DISK AM-200	1
4	DWB-00103-01	HEADER OPTION AM-100	1
5	LBL-00002-00	LABEL WARRANTY VOID	1
6	LBL-00003-00	LABEL AMOS COPYRIGHT	6

COST = $ 0.00

BILL # DWB-00200-02 Retail price $ 0.00

REV.B03 Whsle price $ 0.00

01/04/79 Net price $ 0.00

Description DISK FLOPPY WANGCO COMPATIBLE

	PART NUMBER	DESCRIPTION	QTY
1	DWF-00200-00	DISK CONTROLLER FLOPPY AM-200	1
2	CNF-00002-01	CONN HEADER 50 PIN	1
3	CNS-00040-00	SOCKET 40 PIN DIP	1
4	CNS-00020-00	SOCKET 20 PIN DIP	1
5	CNS-00016-00	SOCKET 16 PIN DIP	28
6	CNS-00014-00	SOCKET 14 PIN DIP	19
7	HDM-00000-00	HEATSINK SMALL	2
8	ICL-07805-00	IC REGULATOR +5V	2
9	ICL-07812-00	IC REGULATOR +12V	1
10	ICL-07905-00	IC REGULATOR -5V	1
11	CPP-00156-01	CAPACITOR 15 UF 20V	8
12	CPN-00103-01	CAPACITOR .01 UF	22
13	CPN-00101-01	CAPACITOR 100 PF	1
14	CPN-00102-01	CAPACITOR 1000 PF	1
15	SWT-00001-00	SWITCH TOGGLE	1
16	RSN-00002-00	R-PACK SIP 330 OHM	1
17	RS2-00331-00	RESISTOR 330 OHM 1/4W 5% CAR	7
18	RS2-00103-00	RESISTOR 10 K 1/4W 5% CAR	4
19	RS2-00333-00	RESISTOR 33 K 1/4W 5% CAR	1
20	ICS-01771-00	IC FLOPPY CONTROLLER SINGLE DEN	1
21	IC1-74193-01	IC COUNTER 4 BIT BINARY	8
22	IC1-74175-01	IC QUAD D FLIPFLOP	2
23	IC1-07416-00	IC HEX INVERTER /DRIVER OC	4
24	IC1-07414-00	IC HEX INVERTER W/HYSTERESIS	1
25	IC1-26123-00	IC DUAL ONE SHOT	1
26	IC1-74113-01	IC DUAL J-K FLIPFLOP	4
27	IC1-07408-01	IC QUAD 2 INPUT AND GATE	3
28	IC1-74367-00	IC HEX BUFFER	7
29	IC1-74368-00	IC HEX INVERTING BUFFER	1
30	IC1-07404-01	IC HEX INVERTER	2
31	IC1-07432-01	IC QUAD 2 INPUT OR GATE	3
32	IC1-74139-01	IC DECODER 2 TO 4 LINE DUAL	1
33	IC1-08197-01	IC BUFFER OCTAL	1
34	IC1-08T26-00	IC QUAD INVERTING BUFFER	4
35	IC1-07400-01	IC QUAD 2 INPUT NAND GATE	2
36	IC1-08131-00	IC COMPARATOR 6 BIT	2
37	CNH-00016-00	IC HEADER 16 PIN	1
38	HDS-00632-01	SCREW 6-32 X .250	3
39	HDN-00632-01	NUT HEX 6-32	3
40	HDW-00632-01	WASHER LOCK 6-32	3
41	HDS-00632-03	SCREW 6-32 X .750 NYL	1
42	HDN-00632-02	NUT HEX 6-32 NYL	1
43	DWB-00201-01	HEADER ADDRESS AM-200	1

Alpha Microsystems
17881 Sky Park North
Irvine, California 92714