

# Xcell journal

THE AUTHORITATIVE JOURNAL FOR PROGRAMMABLE LOGIC USERS

## Low Cost Solutions for High Performance Results

### NEW PRODUCTS

Spartan-3 FPGAs  
Open New Markets  
and Applications

RocketPHY Delivers  
10 Gbps SONET  
Performance in CMOS

### SOFTWARE

ISE 5.2i Supports  
Spartan-3 FPGAs Now

Precision Synthesis Tool for  
Next-Generation Designs

### APPLICATIONS

Scaleable SPI-4.2  
"Lite" Solution for  
Spartan-3 FPGAs

Software-Compiled System  
Design Methodology

### TECHNOLOGY

Adaptive I/O Solution  
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# Welcome to Our Programmable World

Ralph Waldo Emerson said it best: *Do not go where the path may lead. Go instead where there is no path and leave a trail.*

Here at Xilinx, we do not follow the trends of business and technology – we set them.

Take, for example, our new family of Spartan™-3 Platform FPGAs – the first reprogrammable logic devices to be manufactured with the state-of-the-art 90 nm process technology. Because 90 nm device geometries enable more transistors in a smaller area, Xilinx has reduced die size with this new generation of Platform FPGAs by as much as 80 percent – and increased density to as many as 5 million system gates with as many as 1,200 user I/Os. Perhaps most important of all, Spartan-3 FPGAs are priced to replace ASICs in high-volume production. Now the FPGA you use to prototype your design can be the FPGA you use in the manufacture of your design.

We are also pleased to announce in this edition of *XJ* the RocketPHY family of 10 Gbps CMOS Physical Layer (PHY) transceivers. Designed on a standard 0.15 μm CMOS process, RocketPHY devices are the first Xilinx family of Physical Layer OC-192 SONET-compliant transceivers optimized for a wide range of 10 Gbps optical interconnect applications. This technology is also used in our new Virtex-II Pro™ X FPGAs.

Many of you may be reading *Xcell Journal* for the first time at Programmable World 2003. Welcome to our world. It's growing bigger, faster, and better every day. A subscription to *XJ* is free for the asking (see URL below). We hope you enjoy and gain valuable knowledge from this edition. Much of what we publish is brand new to the world. In our Fall 2003 issue, we will show you what may very well be the beginning of the end of all fixed logic design. But if you just can't wait for the latest news and information on programmable logic and systems, visit *Xcell Online* ([www.xilinx.com/publications/xcellonline](http://www.xilinx.com/publications/xcellonline)), where you'll find frequent reports on what's happening in the world of programmable logic.

Tom Durkin  
Managing Editor

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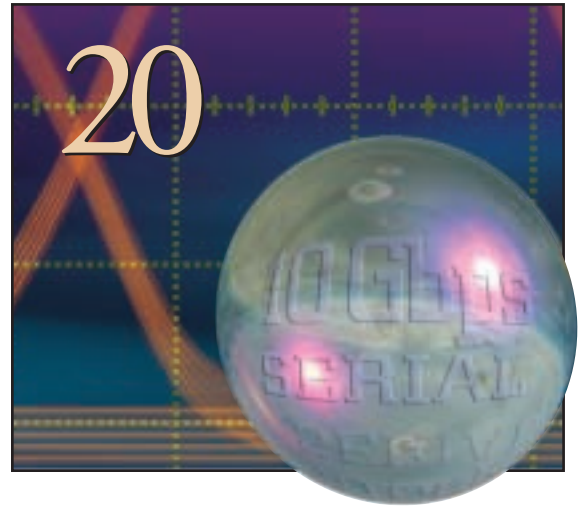
## New Spartan-3 FPGAs Are Cost-Optimized for Design and Production

The new Xilinx Spartan-3 FPGA family offers up to 5 million system gates with the lowest cost per gate and lowest cost per I/O compared to any other programmable logic alternative. Why use a gate array or standard cell ASIC when you can get a low-cost, high-density, and faster time-to-market solution with Spartan-3 FPGAs?

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Check out *Xcell Online* ([www.xilinx.com/publications/xcellonline/](http://www.xilinx.com/publications/xcellonline/)) for these late-breaking *Xcell Online Web Xclusives* and more:

- Xilinx 300 nm and 90 nm Process Technologies: Why This Is Important to Designers.
- Is Your FPGA Design Secure? It Is with Xilinx — and Here's How It Works.
- PCI Express Advanced Switching: Solve Your PCI Implementation Problems.
- Why The Boeing Company Chose Virtex-II Pro Platform FPGAs for Image Processing.



## New RocketPHY Transceiver Family Debuts at 10 Gbps

A new family of 10 Gbps serial I/O transceivers dramatically cuts costs in light-speed applications. These transceivers make it possible to create unique optical connectivity designs.



## NSPICE Bridges Simulation Gap

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## Get the EasyPath Solution

The Virtex-II and the Virtex-II Pro EasyPath solutions are a cost-effective alternative to ASIC conversion — saving you money while significantly decreasing your time to market.

58



## How to Design a 3DES Security Microcontroller

Using IP cores and a pre-integrated IP platform, engineers at SoC Solutions built a custom microcontroller platform in less than two weeks.

69



## Platform Delivers Fast, Flexible AC Servomotor-Control Designs

New digital motor-control applications exceed the capabilities of conventional solutions.

82



## Xilinx FPGA Blasted into Orbit

A radiation-hardened Xilinx FPGA gives the Australian FedSat satellite powerful reconfigurable computing capabilities.

86

# Xcell journal

View from the Top .....	6
New Spartan-3 FPGAs Are Cost-Optimized .....	7
Spartan-3 Family Opens New Applications .....	10
ISE 5.2i Delivers Head Start to Spartan-3 Designers .....	14
Spartan-3 FPGAs Add SPI-4.2 "Lite" Core .....	16
New RocketPHY Transceiver Family — 10 Gbps .....	20
Accelerate Your Multi-Gigabit Serial Design .....	24
High-Speed Serial Interface Design .....	28
Kit for Cadence Tools Speeds RocketIO Designs .....	30
Software-Compiled System Design .....	32
Tarari and Celoxica — Fast Algorithm Acceleration .....	38
Next-Generation FPGA Synthesis .....	44
NSPICE Bridges Simulation Gap .....	46
Optimize Pin Assignments Early .....	49
Got the BGA Blues? .....	52
Reduce Resistor Counts and Lower Costs .....	56
Get the EasyPath Solution .....	58
Xilinx Chips Fight Drunk Driving .....	63
FPGAs Are the Brains Behind "Smart" Cars .....	64
How to Design a 3DES Security Microcontroller .....	69
How to Use Free Software in Embedded Designs .....	74
Xilinx Delivers HyperTransport Lite Reference Design .....	79
Low-Cost IP Connectivity Lets Diverse Systems Communicate .....	80
Platform Delivers Fast, Flexible AC Servomotor Designs .....	82
Xilinx FPGA Blasted into Orbit .....	86
MyXPA Helps You Get the Most from the XPA Program .....	90
Xilinx Events and Tradeshow .....	91
Fuzzy Logic .....	93
Xilinx Partner Yellow Pages .....	94
Spartan-3 Data Sheet .....	102
Reference Pages .....	106

# Move Over, von Neumann



by Wim Roelandts  
CEO, Xilinx, Inc.

Extraordinary advances in programmable logic technologies are making it possible for FPGAs to offer unique new ways to build advanced designs that were previously impossible. In fact,

many traditional design components are becoming obsolete as FPGAs become faster and less expensive. The standard microprocessor is no longer the only way – or the best way – to develop high-performance, low-cost computers.

Programmable logic devices are dramatically changing the way computers are designed. Instead of using a single CPU that executes instructions serially (the von Neumann approach), with programmable logic you can easily run multiple tasks in parallel and achieve an impressive increase in performance while drastically reducing costs. The benefits are too overwhelming to ignore, and programmable logic is the key. The von Neumann architecture is already 50 years old – it's clearly time for a change.

A Xilinx customer, Wincom Systems, will soon introduce a new Web server that can handle the work of 50 to 300 conventional microprocessor-based servers each costing \$5,000 or more – and it costs approximately \$2,500. It does all this without relying on microprocessors, and the server fits in a box the size of a DVD player. This remarkable improvement in cost and performance is being realized in a variety of other new designs that will soon come to market.

Because FPGAs can easily handle massive numbers of calculations in parallel, they are far faster than conventional DSPs or microprocessors in many applications.

Programmable logic devices performing many operations in parallel are replacing microprocessors by providing much higher performance at far lower cost. Here's one example.



Programmable logic has always been far less expensive to develop than ASICs. Now the device costs have been dramatically reduced as well. For example, an FPGA that cost \$1,000 in 1996 costs less than \$10 today – and today's device offers far more features at a much higher speed. In addition, the introduction of 90 nm technology will position our costs to be lowered once again. Next year, our largest FPGA will have approximately 20 million gates, compared to 20,000 in 1993.

## Conclusion

Programmable logic devices can do much more than just replace conventional components. You can create designs that are far more profitable and far more powerful than alternative solutions. Your business depends on getting new designs to market ahead of your competition – designs that provide maximum value, at minimal costs. Programmable logic delivers what you need, today. And it just keeps getting better. ❧

# New Spartan-3 FPGAs Are Cost-Optimized for Design and Production

The new Xilinx Spartan-3 FPGA family offers up to 5 million system gates with the lowest cost per gate and lowest cost per I/O compared to any other programmable logic alternative. Why use a gate array or standard cell ASIC when you can get a low-cost, high-density, and faster time-to-market solution with Spartan-3 FPGAs?

by Rob Schreck  
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Today's design engineers deal with a dilemma every time they start a new logic development project. They want to develop a product fast and get it to market first – but they also must meet demands to lower costs. Many times, engineers have turned to ASIC solutions to meet their cost objectives, but that often means high NRE costs and long development times. Using ASICs also often means running the risks of:

- Missing the market window
- Losing out to competition
- Design problems
- Design changes
- Skyrocketing NRE costs.



Xilinx offers you a better solution with the new class of Spartan™-3 Platform FPGAs. Built on four generations of proven Spartan success in high-volume consumer and automotive applications, this new family of Platform FPGAs delivers unprecedented density, field reprogrammable functionality, and competitive price points. You also get a platform with the density, scalability, and features to tackle tough connectivity, DSP, and embedded design problems.

With Spartan-3 FPGAs, you can develop logic for many new consumer, networking, and automotive applications, including blade servers, low-cost routers, and medical imaging. You can get those products to market fast, because you manufacture the system with the same FPGA you use to develop and prototype the design.

#### Driving Down FPGA Costs

Design engineers have been looking for an alternative to long ASIC development cycles and high ASIC NRE costs. To support an industry requirement that has grown to over \$20 billion, Xilinx set the goal of low cost, unprecedented density range, and high capability for the Spartan-3 family of FPGAs so they could be used both for prototyping and for production of high-volume products. To meet that aggressive target, Xilinx developed this Platform FPGA architecture with a small die size, a wide logic density range, and sufficient I/Os to support the mid-range of gate array and standard cell logic designs. In addition, Xilinx included the features most needed for today's designs:

- Up to 1.8 Mb of block RAM can be used for large FIFOs and data storage.
- Abundant distributed RAM, implemented from logic cells, can be used for small FIFOs, shift registers, and constant coefficients. This combination of block RAM and distributed RAM provides a unique flexibility found only in Xilinx FPGAs.

- Digital clock managers (DCMs) and pre-engineered clock networks facilitate the design of high-speed systems.
- High-speed multipliers are embedded for DSP applications, such as adaptive filters and forward error correction.
- Programmable SelectIO™-Ultra supports 23 I/O standards and provides a low-cost bridge from one I/O standard to another.



Figure 1 - Staggered pad technology

- XCITE digitally controlled impedance technology supports increased signal integrity for both single-ended and differential I/Os.

The result is a cost-optimized FPGA fabric that is, nevertheless, flexible, scalable, and able to provide the capability to support many designs.

#### Process Leadership in 90 nm

Xilinx integrated a large logic density range with all of the above features – and then took another giant step to drive down cost using a new 90 nm process technology. The Spartan-3 FPGA family is the first programmable logic built with this process technology, which leads to die sizes 50% to 80% smaller than any competing solution.

Xilinx also uses 300 mm wafer technology to deliver the efficiency and capacity needed to produce high-volume Spartan-3

FPGAs. These 300 mm wafers deliver almost 2.5 times the number of die compared to the mature 200 mm wafers, but at a fraction of the cost per die. We also implemented a dual wafer fabrication strategy, using world-class foundries at both IBM and UMC to reduce production risks and increase capacity.

Our process technology leadership makes Xilinx the world's lowest-cost, lowest-risk FPGA provider. The Xilinx investment in design optimization, 90 nm manufacturing technology, and 300 mm wafer production delivers price points for Spartan-3 FPGAs at under \$20 for a 1M-gate FPGA and under \$100 for a 4M-gate FPGA.

#### Delivering More I/Os in Smaller Die

Spartan-3 FPGAs offer a remarkably small die for the number of logic gates using 90 nm process technology. Naturally, with a smaller die comes a smaller perimeter for the necessary number of I/O pads. This could be a problem for an application that demands a high I/O count.

However, by using staggered pad technology (Figure 1), Xilinx is able to deliver two rows of I/Os on each edge of the die versus one row found in all other FPGAs and ASIC alternatives. You get more I/Os in a smaller die, resulting in a low cost per I/O and low cost per gate for Spartan-3 FPGAs.

#### Spartan-3 FPGAs: The Complete Design Platform

Spartan-3 Platform FPGAs offer a complete solution of logic, memory, and I/Os – along with features such as multipliers – to provide a rich fabric to support connectivity, DSP, and embedded design applications (Figure 2).

#### Spartan-3 Connectivity Solution

Many design problems revolve around getting data on and off the FPGA. The best way to ease these connectivity problems is a robust I/O solution. All Spartan-3 I/O pins





Figure 2 - Spartan-3 Platform FPGA

support the Xilinx SelectIO™-Ultra functionality, dramatically increasing design flexibility. Each user I/O pin can support any of the 23 electrical interface standards. With the abundant I/Os in the Spartan-3 FPGA family, you get the lowest cost per parallel interconnect available in the industry.

The differential I/O standards assist you in achieving higher performance, lower power consumption, and lower pin count. These standards are supported by soft IP building blocks for important new interface protocols, such as PCI 32/33 and PCI 64/33, RapidIO™, POS PHY Level 4, Flexbus 4, SPI-4, and HyperTransport™.

To further simplify the design process and reduce costs, the Spartan-3 FPGAs support XCITE digitally controlled impedance technology for both single-ended and differential I/O standards. XCITE technology provides I/O impedance matching that adapts to changes in supply voltage and temperature. XCITE technology reduces board cost by eliminating the need for most external termination resistors. What's more, XCITE technology increases signal integrity.

**Low-Cost Points for High-Performance DSP**  
The abundant RAM resources – along with 18X18 multipliers – give Spartan-3 FPGAs a



Figure 3 - ISE 5.2i design suite

significant DSP capability that can deliver up to 330 billion MACs/second. This economical and robust performance makes Spartan-3 devices a cost-effective solution for low-cost applications, such as digital communications, video and imaging, and industrial control.

In addition, the partnership between Xilinx and The MathWorks offers a simple, familiar design flow with MATLAB™/Simulink™ software to design the DSP functions.

#### Industry's Lowest Cost Soft Processor Solution

The high feature set of the Spartan-3 FPGA family provides a low-cost platform for embedding the Xilinx MicroBlaze™ soft

processor. When you combine the MicroBlaze processor and available peripherals with Spartan-3 logic, memory, and I/Os, you can develop a custom embedded design for your specific requirements. You increase on-chip integration, reduce board cost, and minimize the risk of vendors choosing to make obsolete a specific microcontroller.

#### Xilinx Complete Development Support

Spartan-3 FPGAs also come fully supported in the current Xilinx ISE 5.2i software design suite (Figure 3). ISE 5.2i is the most prevalent design methodology in the industry, with more than 150,000 installed users. ISE includes a full spectrum of easy-to-use productivity options that can be inserted to fit in almost any existing corporate logic design methodology. Xilinx ISE tools increase your productivity, which in turn slash design times by as much as 50% when compared to ASIC methodologies.

For design verification, the Xilinx ChipScope™ Pro debugging environment delivers unmatched power to uncover critical bottlenecks and optimize your design.

For engineers using the MicroBlaze processor to develop a field programmable controller, Xilinx offers a complete hardware and software solution with the Xilinx Embedded Design Kit (EDK). Software tools similar to those used for IBM PowerPC™ designs are available to:

- Configure peripherals
- Develop protocols
- Integrate the logic.

Then you can verify your design in the system at speed in the Spartan-3 FPGA. It's an easy solution for today's complex designs.

#### Conclusion

The Xilinx Spartan-3 FPGA offers the lowest cost FPGA in the industry, as well as a true low-cost design platform for many applications. You get the density and features you need for a wide range of designs, plus a development environment to get you through the design cycle and into production quickly. To learn more about the Spartan-3 family, visit [www.xilinx.com/spartan3/](http://www.xilinx.com/spartan3/).

# Spartan-3 Family Opens New Markets and Applications

Spartan-3 FPGAs invade traditional ASIC markets with competitive price points and value-added reprogrammability.

by Robert Bielby  
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Nineteen years ago, Xilinx introduced the field programmable gate array, or FPGA. The concept was simple: by building a gate array based upon SRAM technology, you could develop a chip directly on your desktop, doing away with the high non-recurring engineering costs associated with custom ASICs. The benefits of this technology were immediate and obvious – instant turnaround time and infinite reprogrammability. The idea of a “foundry on the desktop” caught on over time as designers began to rely on FPGAs for product development and limited production deployment.

However, because of the inherent silicon overhead cost for reprogrammability (easily more than 20:1 for an FPGA vs. ASIC), FPGAs were not considered cost-effective for higher volume applications.



In 1998, Xilinx forever changed the playing field with the introduction of the Spartan™ FPGA family. Based on the highly successful XC4000 FPGA architecture, the Spartan FPGA family heralded a new era in programmable logic by delivering products at price points previously not considered possible in the industry. Through streamlined packaging, speed grades, test, and process technology, Xilinx achieved significant cost reductions. These reductions opened a wide range of new markets and applications that could reap the time-to-market benefits and flexibility of programmable logic.

Since the introduction of the first Spartan family, Xilinx has maintained an unabated trend of delivering successively improved Spartan families almost yearly. Each new family offered significant cost and performance benefits over the previous families. Additionally, each family provided additional, new features leading to an even greater reduction in bill of materials costs.

The extent of the cost reductions cannot be overstated: The Spartan-II, the third-generation Spartan family, featured the 100,000-gate XC2S100 family member for just \$10. This represents a 100:1 reduction in cost over the equivalent density device that was introduced just five years earlier.

The Spartan-II FPGA not only delivers a lower cost per gate than its predecessor, it also includes embedded features, such as logic level translators, embedded memory blocks, and integrated phase locked loops, all at the \$10 price point. Thus, it's no surprise that more than 45 million units of the Spartan-II series family have been shipped since its introduction.

Equally as impressive is the range and types of applications where Spartan FPGAs are used in production. Applications such as PC add-in cards, children's digital cam-

eras, CD players, DVD players, personal computers, set-top boxes, personal video recorders, plasma displays, MP3 players, home theater, home audio, karaoke machines, and a host of other applications too extensive to list here. It's almost safe to say that if you can think of an application, there's a very good chance that it contains a Spartan FPGA.

The effect of a low-cost FPGA hasn't gone unnoticed on the Xilinx bottom line: Today more than 13% of Xilinx revenue is generated in nontraditional consumer applications.



With the recent introduction of the Spartan-3 family, Xilinx continues to build on the momentum established six years ago – delivering FPGAs at price points that are unmatched in the industry. Based on a 90 nm SRAM technology and manufactured on 300 mm wafers, the Spartan-3 family enjoys the industry's most advanced process technology. This technology allows the Spartan-3 family to maintain an inarguable price/performance advantage over not only competitors' FPGAs but also ASICs.

The Spartan-3 family also represents a significant breakthrough both in density range and I/O pin count when compared to previous the Spartan families. With a 100:1 range in density spanning from 50,000 gates to 5,000,000 gates and an I/O count

of up to 1,120 user I/Os, the Spartan-3 FPGA family opens up the world of programmability to an even greater suite of applications than ever before.

### Driving New Markets

With such a wide density range and pin count, the Spartan-3 family can compete with the majority of ASIC design starts. In effect, in the future, it's going to be harder to figure out where you won't find Spartan-3 FPGAs than where you will find Spartan-3 FPGAs. Although this comment may be

somewhat fanciful, the list of markets and applications in those markets that are a perfect match for the new, low cost Spartan-3 family is quite broad:

### Automotive

The newest innovations in automobiles today are not centered on improved fuel efficiency or improved performance, but instead are focused on improving the driver and passengers' driving experience and safety. This emerging new technology is called telematics.

Telematics represents the greatest innovation in the automotive industry since perhaps the introduction of the car itself. Imagine what would be possible if all of your personal information appliances and entertainment devices could communicate and share information with one another in a single environment. In such a scenario, your cell phone could communicate directly to your PDA, which would allow you to review your email, download a MP3 audio track, and play it on the car stereo while you checked your stock portfolio and looked for the best route to go to work. Multifunction telematics is both possible and available in high-end cars today.

The challenges to optimal telematics, however, are many, because the emergence of new standards, technologies, and short development cycles complicate product

development and deployment. Cost-effective, flexible solutions such as those made possible by Spartan-3 devices will enable you to stay current in this rapidly growing and evolving market.

### Medical

The latest breakthroughs in telemedicine leverage advances in networking and broadband technologies to provide local care by a remote physician or a team of dispersed specialists.

New programs, such as Telestroke, have been developed to support medical doctors who practice medicine in small rural communities or in community hospitals where there are no local specialists in stroke treatment. The Telestroke program is a system to connect medical staffs who work at emergency rooms of small hospitals with stroke specialists by using videoconference systems, ISDN, and desktop computers. These two parties examine the patient simultaneously, test the extent of the stroke, investigate scanned films of the patient's internal organs, and determine the types of strokes that the patient may have suffered. The system enables stroke specialists to tell doctors in the emergency room what appropriate medication to prescribe and what operations to perform. The cost sensitivities of this technology, which combine a wide range of complex technologies, are again well addressed by Spartan-3 FPGAs.

### Digital Video

The digital television set market is poised to enter a period of sustained growth. Various regional digital broadcasting standards have been established in most countries – ATSC high definition in the U.S. and South Korea, ISDB in Japan, and DVB in most of the rest of the world. More countries continue to roll out digital television services every month. And there is more to come. In the U.S., high-definition cable signals are being offered by an increasing number of cable service providers in an increasing number of markets.

Meanwhile, digital terrestrial broadcasts are expected to begin in Japan this year. The deployment of digital video services will



drive the long-awaited consumer demand for digital television sets. The image processing requirements demand both a cost-effective yet high-performance digital signal processing technology such as that offered by Spartan-3 devices.

### Home Networking

The connected home market – consisting of home networking equipment, software, residential gateways, home control, and automation products – is estimated to be \$9.2 billion worldwide by 2006. The current growth of the connected home market has been spurred over the past year by a surge in popularity of wireless networking technology and basic home routers to enable broadband and resource sharing, including file and printer sharing.

Multiple other factors will continue to fuel this growth, including the need for network security. Home routers and residential gateways will need “firewall” protection for always-on connections. Additionally, the release of Windows™ XP, the first true “home network friendly” operating system from Microsoft, has greatly simplified the task of interconnecting and sharing resources. The next wave in home networking will be the broad-based sharing of video and audio – adding new complexities and challenges but also benefits to the consumer. Localized media centers with global sharing will drive new solution models that will again greatly benefit from the programmability and flexibility of Spartan-3 FPGAs.

These examples are but a small sampling of the many exciting new markets and applications for Spartan-3.

### eSP Simplifies System Design

Two years ago, Xilinx introduced the industry's first Web portal dedicated to accelerating product development for a wide range of markets and applications. With a focus on providing solutions and tutorials primarily targeting new and emerging standards and protocols, the aptly named eSP (emerging standards and protocols) Web portal has proved to be an effective industry resource validated by more than seven million visits to date.

The eSP portal covers a wide range of markets and applications, including:

- Both consumer and professional digital video technologies
- Wireless networking
- Home networking
- Automotive telematics
- Metro access networking technologies.

With the introduction of the Spartan-3 family, Xilinx has expanded the breadth of the eSP portal to highlight and provide solutions and tutorials on the new markets and applications now addressed by this revolutionary new FPGA family. To learn more about the new Spartan-3 markets, applications, and solutions, visit the eSP portal at [www.xilinx.com/esp/](http://www.xilinx.com/esp/). ❧

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## Online innovation

Whether you're designing next-generation consumer, digital video, automotive, industrial, or even broadband applications, the eSP web portal can help make your innovation a reality. Featuring everything from technology tutorials, market overviews, and system block diagrams to reference boards, IP cores and more, this is the ultimate resource for all your design solutions.

SPARTAN-3



## The power of 3

The high-performance, low-cost Spartan-3 platform FPGA features a range of density options from 50,000 to 5 million gates, as well as the lowest I/O and gate costs available. This makes it the ideal device for a wide variety of applications. Now, our eSP web portal gives you access to a complete suite of Spartan-3 silicon, software, and IP solutions optimized for your design.

For more information, visit us at [www.xilinx.com/esp/s3](http://www.xilinx.com/esp/s3).



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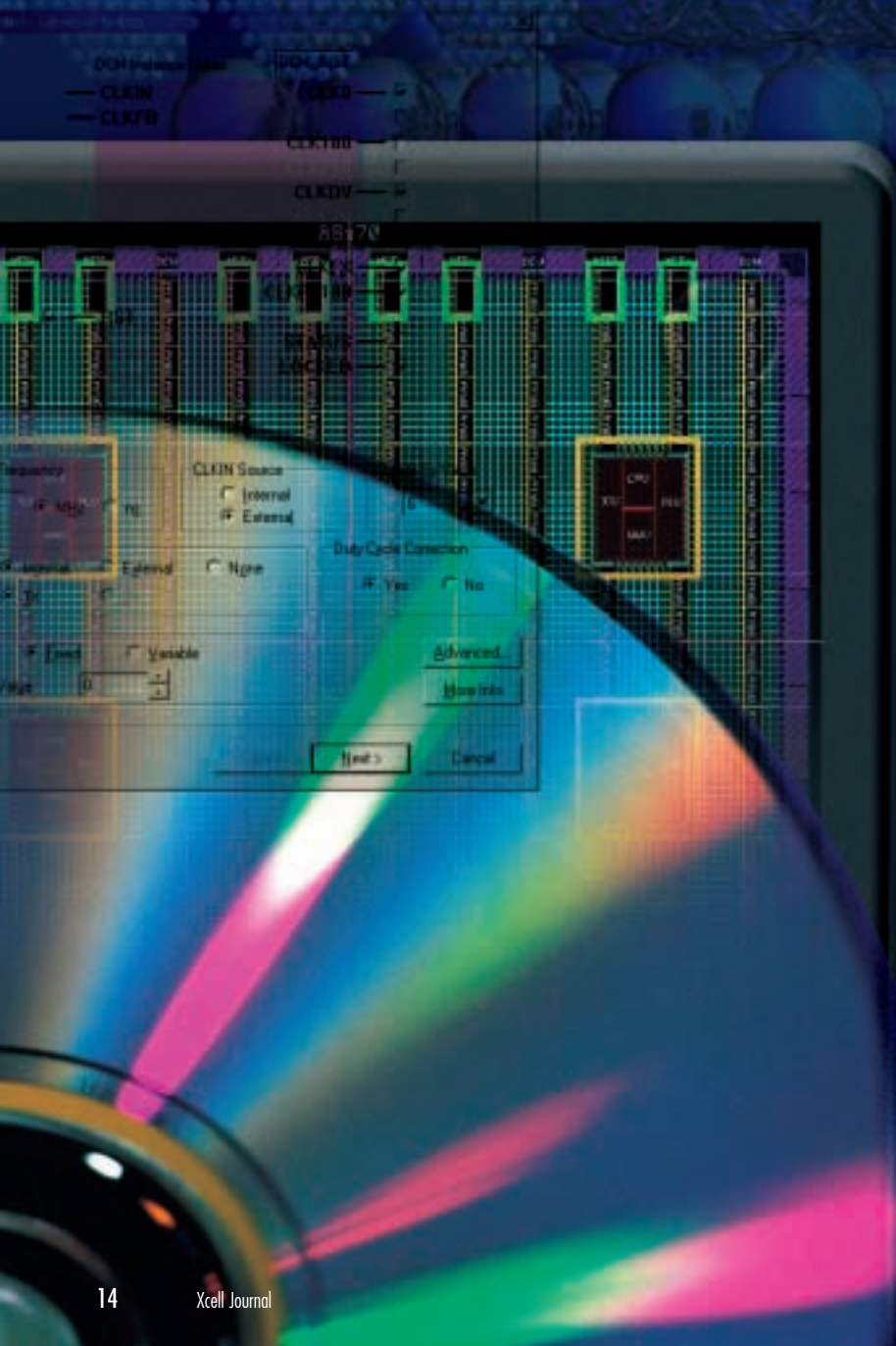
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# ISE 5.2i Delivers Head Start to Spartan-3 Designers

Xilinx ISE 5.2i design and development software allows you to take full advantage of the features of the newly released Xilinx Spartan-3 family of FPGAs.



by Lee Hansen  
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Why wait for critical software design support of the latest FPGA family when Xilinx ISE 5.2i design software already supports the new, low-cost Spartan™-3 FPGAs right now? You can hit the ground running with the newest and best-in-class FPGAs and development tools – including third-party software support.

Spartan-3 FPGAs are based on the pioneering Virtex™-II Platform FPGA architecture introduced in late 2000. Virtex-II FPGAs exploded beyond the supposed limits of what a programmable logic device could do. Since then, the Xilinx ISE design environment has kept pace with the technology to make full use of the Platform FPGA architecture, including tight partner tool integration.

## Leverage the Architectural Advantage

Spartan-3 FPGAs are ready to use with Synplicity™ and Mentor Graphics Exemplar synthesis support now. That means all of the internal logic structures can be put to maximum use in your Spartan-3 design today – not six months to a year from now, which is the usual timeline when a new architecture is released.

The ISE 5.2i toolset and synthesis partners support inferencing of internal logic structures. This allows the synthesis tools to make maximum performance choices for your design during implementation, and makes it easier to code, debug, and read HDL source code.

Spartan-3 devices also contain the “active interconnect” routing pioneered in Virtex-II FPGAs. The active interconnect technology, with its buffered routing, allows more logic structures to be reached with minimum impact on signal delay time. Because timing delay is minimized, even for long signal routes, you also see less impact to timing during the re-place-and-route phase. With active interconnect technology, more signal paths stay in time spec than with traditional architectures.

ISE 5.2i offers architecture wizard support for the Spartan-3 DCMs (digital clock managers), as shown in Figure 1. The architecture wizard lets you program the advanced clock features of the Spartan-3 DCMs through an easy-to-use



design wizard. Just set the appropriate attributes in the dialog box, and fully editable VHDL or Verilog™ code is written into your HDL source, saving valuable design time. This HDL source is “correct by construction” without requiring you to understand every nuance of the device architecture.

The full range of I/O options for Spartan-3 FPGAs are completely supported in ISE, including differential routing, which gives you the maximum in system I/O protocol choices. Xilinx XCITE digital internal resistor I/O termination is fully supported in ISE, greatly reducing the number of external resistors on your board and freeing up valuable PCB real estate for essential devices.

## Productivity Options

A full spectrum of ISE design productivity options is available to optimize your Spartan-3 design. Incremental design technology slashes design recompile times by limiting the re-implementation phase to only the design modules that need to change. The rest of the design is frozen and intact, preserving previous performance results.

Now included at no extra cost in ISE 5.2i is a modular design capability delivering a divide-and-conquer, team-based approach to high-density design. Teams of engineers can complete their modules in parallel,

focusing on individual module performance rather than overall design completion. Modular design functionality speeds the design flow through to faster completion.

Although incremental design and modular design have similar capabilities, the incremental design approach provides a simple design flow and faster runtimes when all modules are available. On the other hand, the modular design option provides individual independence inside a team environment and can be used when you need the flexibility for design modules to arrive at different times.

The area mapping capabilities of ISE Floorplanner and PACE enable quick and easy logic grouping, leading to better timing results and faster design performance. RPMs (relationally placed macros) allow design teams to save floorplanned HDL designs for later design reuse. RPMs let managers best utilize their HDL resources and deliver repeatable, guaranteed design performance.

## Conclusion

With ISE 5.2i and Spartan-3 FPGAs, you now have at your fingertips the lowest cost FPGA design options available today. ISE 5.2i extends these advantages by adding the design edge that delivers more productivity and lower design costs, all in a package that's built on proven Xilinx architectural design advantages. ✖

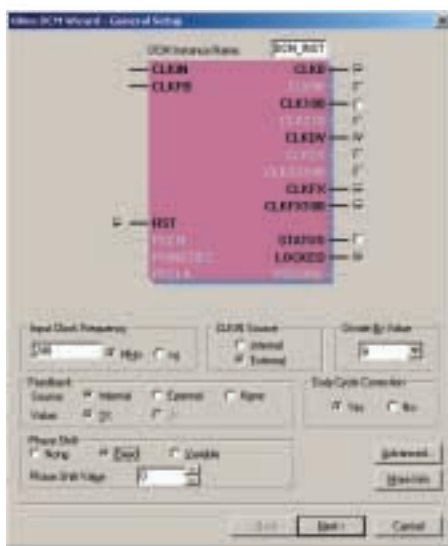


Figure 1 - ISE 5.2i DCM architecture wizard

# Spartan-3 FPGAs Add SPI-4.2 "Lite" Core to Slash Design Costs

The SPI-4.2 "Lite" solution for Spartan-3 FPGAs delivers 2.5 Gbps but remains compliant with the SPI-4.2 10 Gbps specification to deliver a low-cost, high-end solution perfect for existing MAN/LAN networks.

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Finding creative ways to keep costs low has become a mandate for designers of advanced systems. This is especially true in the telecommunications space, where the demand for ultra-fast 10 Gbps infrastructure performance is still in the formative stages. Therefore, providing 10 Gbps levels of performance is not a market or product priority at this time.

Instead, metro access and WAN/LAN equipment providers are focused on building and servicing the more mainstream 2.5 Gbps infrastructure as a way to ride out the current economic doldrums. Their priorities have shifted from features and performance to cost and risk avoidance.

Given these market conditions, designers of Ethernet, Packet-Over-SONET, and ATM applications have demonstrated a keen interest in low-cost solutions for interconnecting PHY devices and traffic management components such as network processors and ASSPs using the SPI-4.2 interconnect standard.

Xilinx is responding to this interest with a pre-engineered, drop-in SPI-4.2 "Lite" intellectual property (IP) core that can be implemented on its low-cost Spartan-3 devices. The core is fully compliant with the 10 Gbps (OC-192) OIF-SPI4-02.0 specification while operating at a reduced line rate of 2.5 Gbps (OC-48). This article provides an overview of the benefits of the solution and the details of the SPI-4.2 Lite core.

## **Spartan-3 FPGAs and SPI-4.2 Lite**

The sweet spot for new telecommunications equipment over the next 12 to 18 months will be products running at 2.5 Gbps. Because POS-PHY Level 3 (SPI-3) is targeted to 2.5-Gbps OC-48 applica-



tions, one way to meet this demand is to build SPI-3 compliant interfaces inside these products.

However, a powerful alternative to building a SPI-3 interface is to build an interface using the SPI-4.2 Lite solution hosted on a Spartan-3 FPGA. This approach achieves 2.5 Gbps line rates while still adhering to the OIF SPI-4.2 10 Gbps specification. Furthermore, the PCB design is simplified because this solution delivers better flow control than the SPI-3 standard and uses fewer pins.

Hosting the SPI-4.2 Lite IP core on a Spartan-3 allows gigabit network providers to meet the demand for 2.5 Gbps performance at the lowest possible cost – while also putting their designers in a great position for the transition to 10 Gbps data rates. Because the core runs at a line rate of 2.5 Gbps, compared to 10 Gbps for the full-rate core, it can be successfully hosted on a low-cost Spartan-3 device that delivers the requisite performance to achieve the lower line rate.

The SPI-4.2 Lite solution is a great starting point for network equipment providers that will scale their products to 10 Gbps data rates when the market moves in that direction. Because the SPI-4.2 Lite solution running at 2.5 Gbps is functionally compliant with the OIF SPI-4.2 10 Gbps specification, the internal interface, the functional testing, and the back-end application logic can all be reused. In the line card design, as shown in Figure 2, IP reuse is straightforward. Only the size of the SPI core will change. This significantly reduces the development time associated with building equipment targeted at a 10 Gbps-dominated marketplace.

### SPI-4.2 Lite Core Overview

The SPI-4.2 Lite core is delivered as independent source (Tx) and sink (Rx) cores. A block diagram of the SPI4.2 Lite IP core and its interfaces is shown in Figure 3. It is a drop-in replacement for the Xilinx full-rate SPI-4.2 IP core – the signals and functionality of both the full-rate and Lite SPI4.2 core are identical.

### SPI4.2 Lite Core Specifications:

- Performance: 200 Mbps on SPI-4.2
- Supported families: Virtex™-II, Spartan-3
- Slices Required: 1,450
- SelectRAM™ blocks: 6
- Global clock buffers: 3
- Digital clock managers: 2.

The source and sink cores provide data storage implemented with FIFOs using dual-port SelectRAM blocks that support independent read/write clock domains. These FIFOs allow the storage of up to 512 data words. The design optimizations developed for the full-rate SPI-4.2 source core are also implemented in the Lite release. This includes the unique ability of the Xilinx SPI-4.2 solution to maximize bandwidth utilization by not inserting filler idle cycles on the SPI-4.2 interface. Under normal operating conditions, back-to-back packets are separated by a

single combined EOP/SOP control word.

You can request the insertion of idle cycles or training patterns regardless of the source FIFO status. By allowing the insertion of idle bus cycles in response to user requests, flow control latency is greatly reduced. In addition, the SPI-4.2 Lite core is able to transfer contiguous data bursts across the SPI-4.2 interface. The source FIFO will refrain from transmitting data until an entire burst has been written into the FIFO. Once a burst has been written into the FIFO, the data will be transferred across the SPI-4.2 interface without interruption until the entire burst has been transmitted.

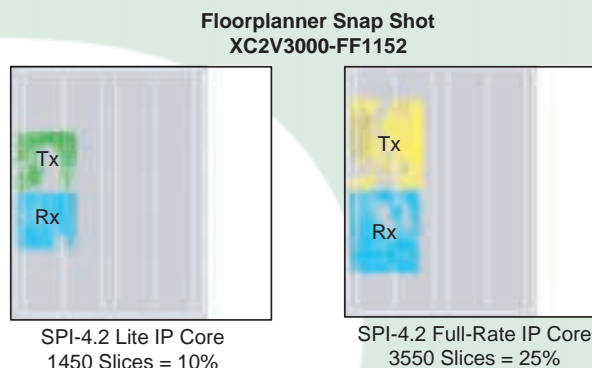


Figure 1 - Lite core requires 15% fewer slices.

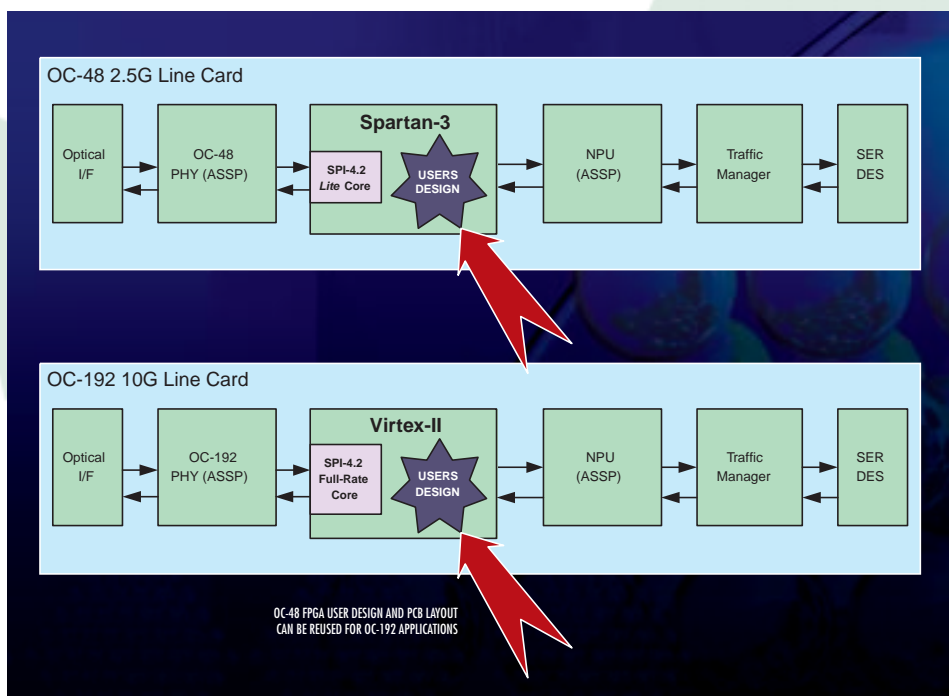


Figure 2 - SPI-4.2 Lite and full-rate design reuse example for OC-48 and OC-192 line cards

## SPI-4.2 Lite Interfaces

The SPI-4.2 Lite core has four primary interfaces:

1. User interface
2. SPI-4.2 interface
3. Status interface
4. Calendar interface, as shown in Figure 3.

The core also has a set of static configuration signals that are used for in-circuit customization of the core. The SPI-4.2 core's interface supports up to 200 Mbps (100 MHz LVDS DDR I/O) for an aggregate bandwidth of 2.5 Gbps. Like the full-rate SPI-4.2 IP core, the FIFO status path operates at a quarter of the data rate and its electrical interface can be user-configured to be either LVTTL or LVDS.

In order to support the widest range of applications, the SPI-4.2 Lite core offers you a choice of either a 32-bit or 64-bit user interface. The user interface operates at up to 150 MHz for both the 32-bit and 64-bit core configurations. With the 64-bit interface at frequencies greater than 100 MHz, the user interface can operate at a higher bandwidth than the SPI-4.2 interface. You can transmit and receive data from two FIFOs implemented in dual-port SelectRAM blocks that each support independent read/write clock domains.

This interface is designed with standard FIFO handshaking signals to simplify the user's logic. For additional flexibility, the source FIFO status channel interface comes in two configurations: the addressable interface and the transparent interface. The addressable calendar can be programmed to indicate the order and frequency of the channel's status on the user interface, enabling a polling implementation. The transparent calendar has a 2-bit interface for all channel configurations and is updated in the order that it is received by the sink interface, allowing minimal latency in the flow control implementation.

## Quick Start to Implementation

Two Xilinx implementation documents are provided with the core: the SPI-4.2 Design Example Guide and the SPI-4.2 Quick Start

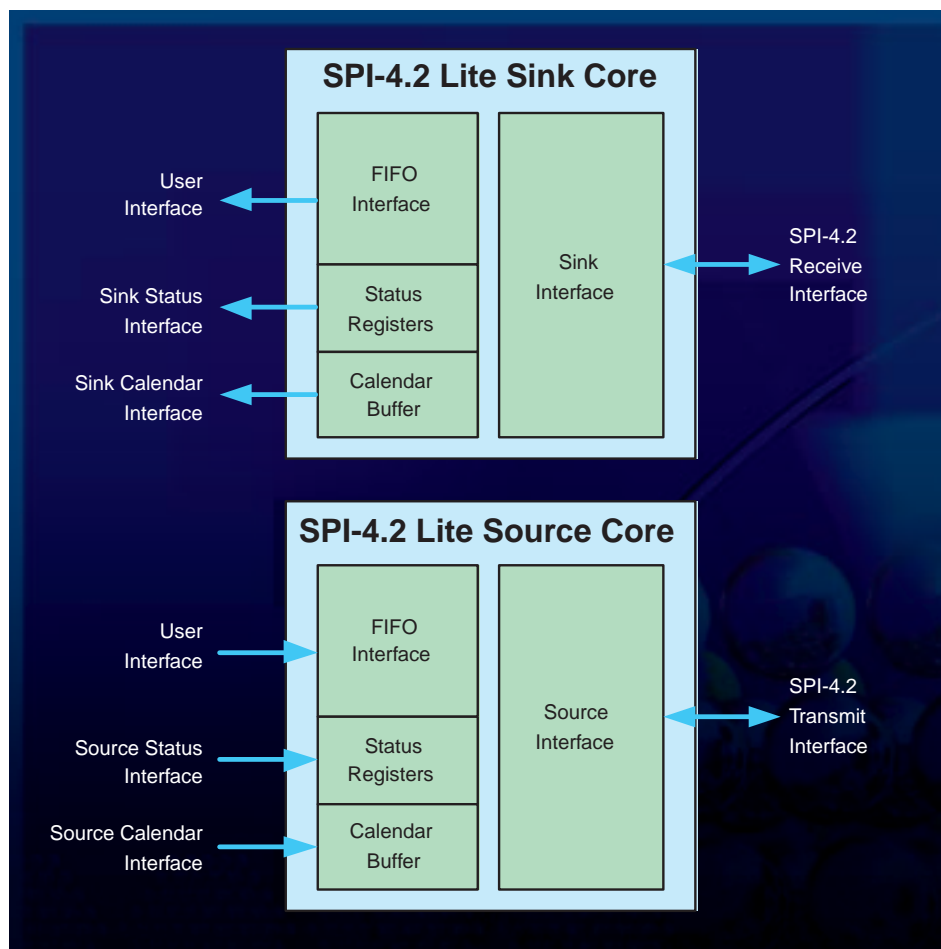


Figure 3 - Block diagram of SPI-4.2 Lite and full-rate core

Guide. These documents help you quickly integrate the SPI-4.2 core into your design.

The SPI-4.2 Design Example Guide provides RTL code (along with a user's guide) that enables you to simulate the core immediately with automatically generated SPI-4.2 packet data. This illustrates how to connect to each of the core's interfaces. The provided code is also synthesizable so you can run it through Xilinx implementation tools. This allows you to instantly view the layout of the core in the Floorplanner, simulate the core with back-annotated timing information, and quickly evaluate performance compliance.

The SPI-4.2 Quick Start Guide contains the information necessary for you to modify the core to meet your design requirements. It walks you through the process of selecting the correct designs and netlists, customizing the timing and constraints necessary for their particular application, and running the automated implementation scripts.

## Conclusion

The compact SPI-4.2 Lite core combined with the low-cost Spartan-3 architecture provides a powerful SPI-4.2 interconnect solution that helps telecommunications and networking infrastructure providers respond to the pressure to deliver low-cost solutions in today's marketplace. The SPI-4.2 Lite core is packaged with the full-rate core and is offered at \$18,000 (USD). Customers with an in-maintenance license for the full-rate core are entitled to receive the new SPI-4.2 Lite core as an update.

For more information, or to evaluate the new SPI-4.2 Lite core, please contact your Xilinx sales representative. ❧

## References

- [1] PMC-Sierra, Inc., POS-PHY™ Level-4, A Saturn Packet and Cell Interface Specification for OC-192 SONET/SDH and 10Gb/s Ethernet Applications. Issue 5: June 2000.
- [2] OIF-SPI4-02.0 System Packet Interface Level-4 (SPI-4) Phase 2: OC-192 System Interface for Physical and Link Layer Devices.

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# New RocketPHY Transceiver Family Debuts at 10 Gbps

A new family of 10 Gbps serial I/O transceivers dramatically cuts costs in light-speed applications. These transceivers make it possible to create unique optical connectivity designs.

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On May 5, 2003, Xilinx unveiled another key first in the programmable logic industry – the RocketPHY family of 10 Gbps CMOS Physical Layer (PHY) transceivers. Designed for a wide range of applications and markets including MAN, WAN, LAN, and SAN, the RocketPHY family represents the next milestone in our commitment to supporting the imminent transition to serial signaling technologies.

The Xilinx serial I/O technologies, named the “Serial Tsunami Initiative,” are causing a virtual tidal wave of new standards to emerge, bringing you the significant benefits of lower cost, lower power consumption, reduced electromagnetic emissions, and simplified PCB design.

## The Serial Tsunami Initiative

Five years ago, it was clear that the traditional approach to scaling I/O performance was reaching its limitations; industry stan-

dards such as PCI halted its traditional approach of scaling bandwidth by doubling both bus width and frequency with the introduction of the 64-bit, 133 MHz PCI-X node. PCB layout constraints restricted PCI-X to a bus width of 64 bits while standard single-ended signaling technologies capped out at 133 MHz. With the introduction of PCI Express, the industry signaled the end of the parallel I/O era – serial signaling technologies are now becoming mainstream.

Xilinx has responded by delivering innovative solutions that address these industry-wide transitions. In 1999, Xilinx led the charge with the introduction of the Virtex™ FPGA family. The Virtex family introduced SelectIO™ technology, an industry first, to support multiple I/O signaling standards that were programmable on a pin-by-pin basis. The Virtex family provided direct support for a wide range of new high-performance I/O signaling technologies, including GTL, STTL, HSTL, and BTL. These standards were rapidly gaining market acceptance in chip-to-chip interfacing, memory interfacing, and back-

planes, as the performance limitations of LVTTTL signaling became too great.

The benefits of the SelectIO solution were clear – high-performance signaling technologies integrated on an FPGA platform that allowed for direct communication with the higher speed I/O interfaces. With SelectIO technology, you could simplify bridging between standards, eliminate external transceivers, improve cost, and reduce board area, all the while delivering higher performance I/O signaling.

Xilinx expanded upon the vision of providing integrated support for high-speed I/O signaling in subsequent FPGA families with the introduction of the Virtex-II and the more recent Virtex-II Pro™ families. The Virtex-II family opened up the reach of high-speed I/O signaling through the integration of LVDS I/Os capable of operations up to 622 MHz using a source-synchronous clocking topology. In conjunction with RocketIO™ technology, the Virtex-II Pro family extended the I/O signaling capabilities to 3.125 Gbps using CML-based differential serial signaling technologies with integrated clock recovery.

## Introducing RocketPHY Transceivers

The latest in our comprehensive portfolio of high-speed serial I/O solutions is the RocketPHY family of Physical Layer transceivers. Designed on a standard 0.15  $\mu\text{m}$  CMOS process, RocketPHY devices are the first Xilinx family of Physical Layer transceivers that support SONET-compliant jitter and are optimized for a wide range of 10 Gbps optical interconnect applications.

The RocketPHY family of low-cost, low-power CMOS transceivers consists of three family members that support multi-rate operation from 9.9532 Gbps to 10.709 Gbps; they include a serializer/deserializer (SERDES), an integrated clock multiplication unit (CMU), and clock/data recovery (CDR) circuitry. The parallel interface of the RocketPHY family is directly compliant with Xilinx Virtex-II Pro FPGAs and other industry framers and media access controllers (MACs), through XSBI and SFI-4, 16-bit differential LVDS interfaces.

### RocketPHY Features

RocketPHY devices offer:

- Multi-rate 9.9532 Gbps to 10.709 Gbps integrated CMOS transceiver (MUX/DeMUX, CDR, CMU)
- SONET OC-192/SDH STM-64/Telcordia compliant
  - 9.9532 Gbps SONET data rate
  - 155.52 MHz or 622.08 MHz reference clock
  - Exceeds OC-192 jitter generation, jitter transfer, and jitter tolerance specifications, as shown in Figure 1
- SONET FEC support
  - 10.709 Gbps data rate (G.709)
  - 167.33 MHz or 669.325 MHz reference clock
- IEEE 802.3ae 10 Gigabit Ethernet Standard (Base R, W) compliant
  - 10.3125 Gbps data rate
  - 161.13 MHz or 644.53 MHz reference clock

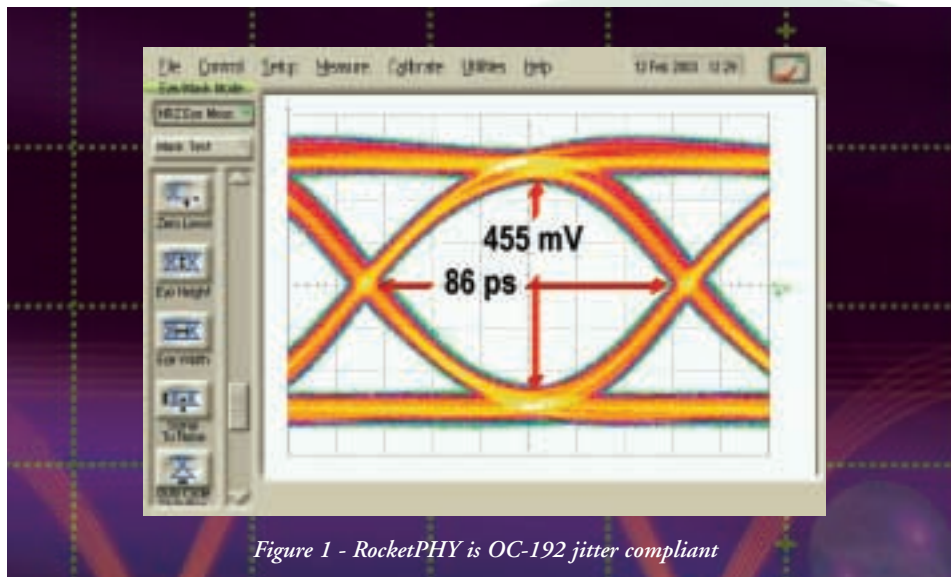


Figure 1 - RocketPHY is OC-192 jitter compliant

- 16-bit LVDS parallel interface compliant to OIF SFI-4 and IEEE 802.3ae XSBI (3.3V supply)
- Differential CML driver for PMD interface
- FIFO to de-couple transmission clock
- Multi-rate 10 GHz transmit clock output
- Parallel interface bit order swapping
- Serial data polarity inversion (on transmit)
- Three transmitter reference clock modes with clean-up PLL
  - TX reference clock
  - RX recovered clock (line timing)
  - TX parallel input clock
- Line and diagnostic loopback modes
- On-chip CML and LVDS termination
- Seamless interfacing to Virtex FPGA families and ASSPs via Versatile Parallel Interface
  - Back clocking mode (622 MHz or 311 MHz)
  - Forward clocking mode (622 MHz or 311 MHz)
- Transmitter/receiver lock detection
- 17 mm x 17 mm, 256-ball, fine-pitch, plastic BGA package
- CMOS manufacturing process
- Power supplies: 1.8V and 3.3V
  - 1.5W typical power consumption.

RocketPHY Family Member	Supported Standards	Target Applications	Parallel Interface
RocketPHY 10G Ultra MSATM	SONET OC-192 SDH STM-64 G.709 10Gbps Ethernet 10Gb Fibre Channel	MSA Modules XFP Modules	XSBI SFI 4
RocketPHY 10G SONET/SDH	OC-192 SDH STM-64	SONET/SDH-based transmission systems, ADMs	SFI 4
RocketPHY 10GbE/FC	10Gbps Ethernet 10Gb Fibre Channel	Transmission equipment, NICs, test equipment, edge routers, storage, area networks	XSBI

Table 1 - RocketPHY family overview

## Applications

Each of the three RocketPHY devices is optimized for specific applications as shown in Table 1. A basic application block diagram is shown in Figure 2.

### SONET OC-192 and SDH STM-64

In SONET/SDH operation, the transceiver connects to the SONET/SDH framer via the parallel 16-bit LVDS interface. It receives and transmits SONET-framed 16-bit words at a rate of 622.08 Mbps. The 16-bit words are converted from/to a serial bitstream at 9.9532 Gbps. An LVPECL reference clock of either 155.52 MHz or 622.08 MHz may be used (see Figure 3).

### Optical Transport Network Operations (SONET + FEC)

In Optical Transport Network (OTN) operation for OC-192 applications, the transceiver connects to the SONET/SDH framer via the parallel 16-bit LVDS interface. It receives and transmits SONET-framed 16-bit words at 669.325 Mbps. The 16-bit words are converted to a serial bitstream at 10.709 Gbps. An LVPECL reference clock of either 167.33 MHz or 669.325 MHz may be used (see Figure 4).

### 10 Gigabit Ethernet –

#### 10G Base-R and 10G Base-W Ethernet

In 10G Base-R operation, the transceiver forms the PMA (Physical Medium Attachment), which is located below the PCS (Physical Coding Sublayer). It receives and transmits 64B/66B encoded data in 16-bit words at 644.53 Mbps. The serial data rate is 10.3125 Gbps. An LVPECL reference clock of either 161.13 MHz or 644.53 MHz may be used. No frame detection or alignment occurs.

In 10G Base-W operation, the transceiver forms the PMA, which is located below the WIS (WAN Interface Sublayer). It receives and transmits 64B/66B-encoded and SONET scrambled data in SONET-framed 16-bit words at a rate of 622.08 Mbps. The operation is the same as that described for SONET (see Figure 5).

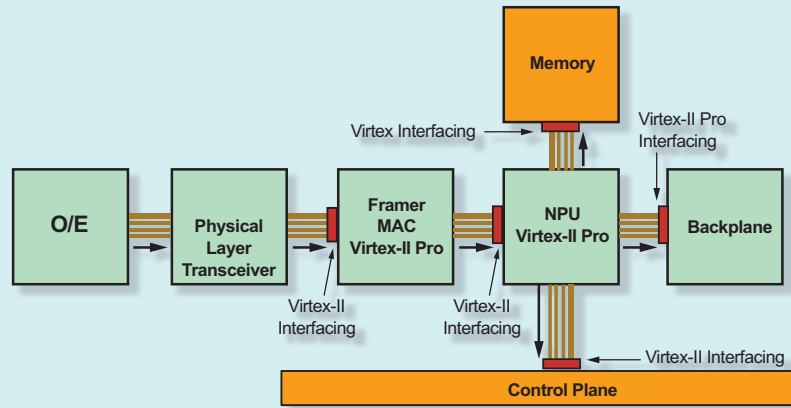


Figure 2 - Basic RocketPHY application block diagram

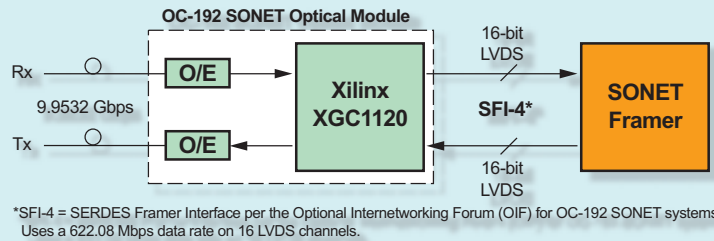


Figure 3 - SONET OC-192 and SDH STM-64 Application

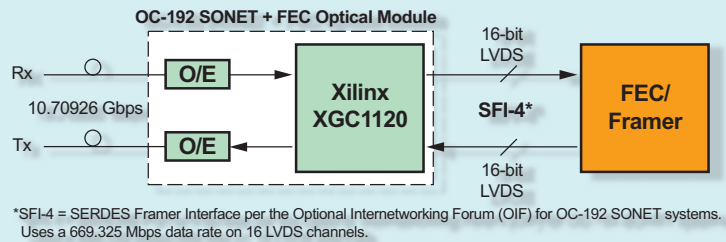


Figure 4 - Optical Transport Network Operations (SONET + FEC) Applications

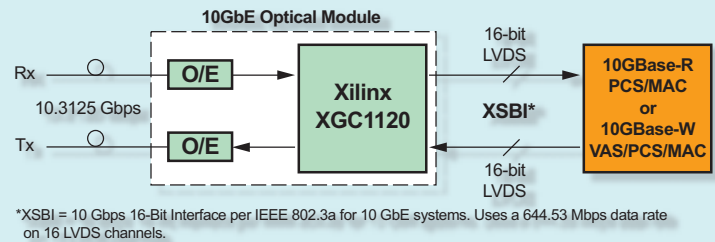


Figure 5 - 10 Gigabit Ethernet: 10G Base-R and 10G Base-W Ethernet applications

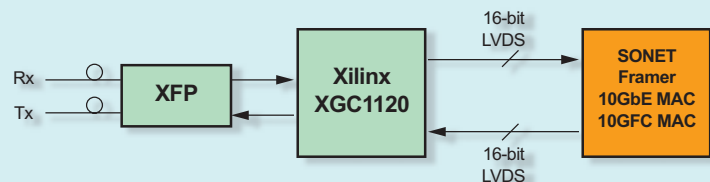


Figure 6 - XFP and MSA module applications

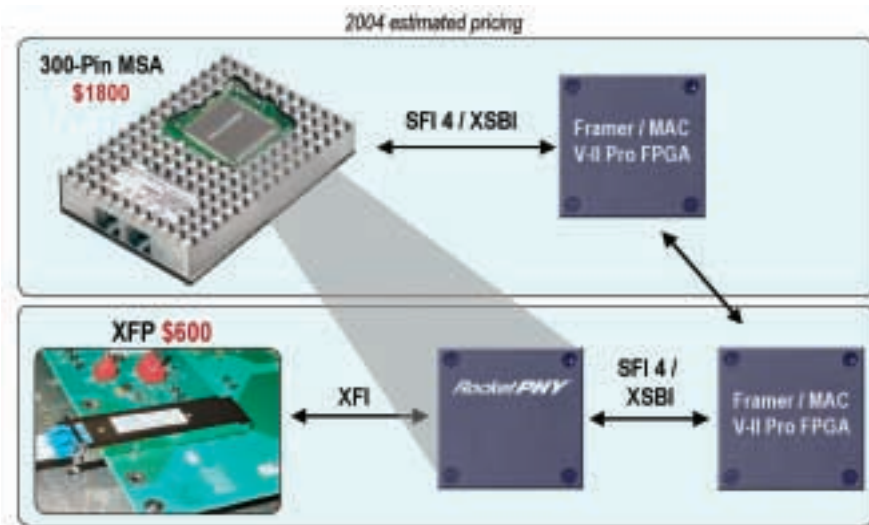


Figure 7 - 300 MSA vs. XFP cost comparison

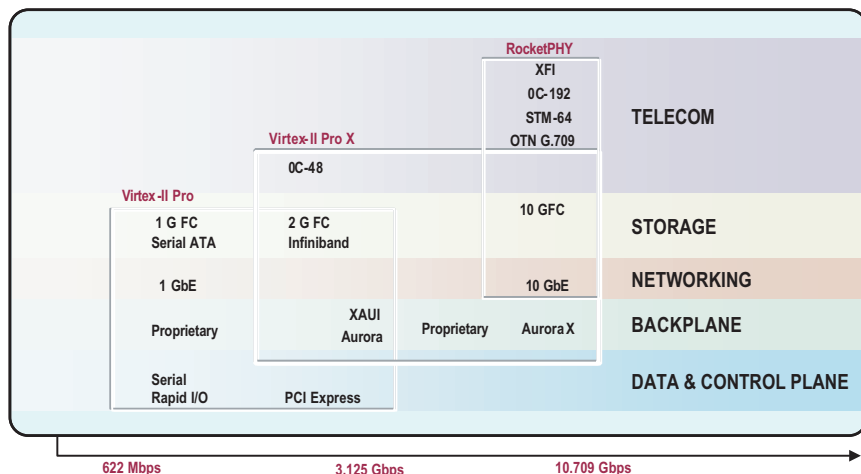


Figure 8 - Seamless serial solutions from 622 Mbps to 10 Gbps

### 10G Fibre Channel and Proprietary Designs

The RocketPHY transceivers support proprietary applications with serial data rates ranging from 9.6 Gbps to 10.709 Gbps, in addition to emerging standards such as 10G Fibre Channel. The transmit reference clock can be either R/16 or R/64 where R is the serial data rate.

### XFP – The Future of 10 Gbps Optical Networking

One of the latest innovations occurring in the optical module market is the transition from the relatively large, costly, 300-pin, multi-source agreement (MSA) optical modules to a new, lower-cost, smaller form-factor optical transceiver named “XFP” for 10 Gbps Form-Factor Pluggable.

The XFP standard promises to offer half the size, one-third the cost, and one-fifth the power requirements; it will serve to further fuel the 10 Gbps optical revolution, as seen in Figure 6. XFP not only defines the dimensions of the optical module itself, but also a standard signaling interface called XFI, ensuring interoperability with industry-standard Physical Layer transceivers. The RocketPHY family is compatible with both XFP and MSA optical modules standards (see Figure 7).

### Virtex-II Pro X – RocketPHY Technology Built-in

Xilinx will also introduce the new Virtex-II Pro X architecture in May 2003, with integrated 10 Gbps RocketIO SERDES support. The Virtex-II Pro X SERDES

provides continuous serial signaling support from 2 Gbps through 10 Gbps with an enhanced Physical Coding Sublayer (PCS) and CMU supplying extended support for telecom-based applications, including those requiring OC-48 SONET jitter compliance. Combined with the new RocketPHY family, Xilinx offers the broadest range of serial solutions addressing the various connectivity hierarchies for a wide range of markets and applications (see Figure 8).

### Conclusion

Over the past five years, it has become evident that core logic performance has far exceeded the capabilities of traditional LVTTTL signaling technologies. Furthermore, the approach to scaling I/O bandwidth by simultaneously increasing frequency and bus width has also reached its limitations, principally because of both cost and technical feasibility.

Through the introduction of innovative products such as the Virtex FPGA family and its subsequent generations, Xilinx has been able to provide solutions that address the ever-changing landscape of I/O signaling and interfacing. The more recent trend in the industry, serial signaling, has not gone unnoticed; with the introduction of Virtex-II Pro and Virtex-II Pro X FPGAs, Xilinx has demonstrated technical and market leadership in delivering seamless solutions for serial signaling applications ranging from 622 Mbps to 10 Gbps.

Now, with the introduction of the RocketPHY family of Physical Layer transceivers, Xilinx is further expanding its range and breadth of serial solutions by delivering the FPGA industry’s first 10 Gbps, OC-192 SONET-compliant transceiver optimized for multi-market optical transceiver applications. With this line up, Xilinx is delivering a suite of serial solutions that are unparalleled in the industry.

For additional product details, see [www.xilinx.com/phy/](http://www.xilinx.com/phy/).

For applications, block diagrams, demonstration boards, intellectual property, and other solutions for RocketPHY applications, see [www.xilinx.com/espl/](http://www.xilinx.com/espl/). ❧

# Accelerate Your Multi-Gigabit Serial Design

The Xilinx "Adaptive I/O" solution enables rapid prototyping, enhanced diagnostic testing, and in-system performance optimization for high-speed serial I/O designs.

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The shift to high-speed serial I/O technology has enabled designers to push the performance of systems well beyond that of traditional parallel bus-based architectures. Multi-gigabit serial links are capable of transmitting data at substantially greater speeds, with significantly lower power, and with a fraction of the pins required for system-synchronous (common clock) or source-synchronous (clock forwarding) schemes.

However, with all the advantages of serial I/O technology, you must address a number of new design challenges when integrating high-speed serial links into your design. Board design, for example, becomes a more involved issue when dealing with signal integrity and transmission line effects of multi-gigabit serial signals. In addition, standards compliance and interoperability testing require new characterization techniques and additional resources during the development process.

The Xilinx "Adaptive I/O" solution for the Virtex-II Pro™ family of Platform FPGAs gives you the power and flexibility to meet these serial I/O design challenges head-on. Leveraging the combination of the RocketIO™ multi-gigabit transceivers (MGTs) and the IBM PowerPC™ 405 embedded processor core, the Adaptive I/O solution gives you the performance and system-level management functions you need to accelerate the development of your high-speed serial design.

The solution is delivered in the form of three pre-engineered reference designs that can be easily integrated into your existing design environment to provide rapid prototyping ability, enhanced characterization and diagnostic testing, and in-system performance optimization of your high-speed serial links. Although the reference designs take advantage of the integrated processor in the Virtex-II Pro device, no PowerPC or C-programming expertise is required to use the Adaptive I/O solution.



## Multi-Gigabit Signal Integrity

Designing with multi-gigabit serial I/O technology requires greater attention to issues that affect signal integrity, such as attenuation, noise, and reflections. At multi-gigabit frequencies, board traces behave like transmission lines, introducing the need for a more detailed understanding of the signal topologies and characteristics of the transmission medium. Jitter effects, dielectric losses, and impedance matching issues must all be carefully considered to ensure reliable data transfer across a serial link at the intended baud rate.

Serial I/O technology provides benefits at various levels within a system, enabling the creation of high-speed links from chip to chip, board to board, and box to box. Clearly, signal topologies and even the transmission medium can vary significantly depending on the type of application. The complexity of the design challenge and level of signal integrity analysis required will also vary accordingly. For example, transmitting over several feet of coaxial cable presents different challenges than transmitting over a few inches of FR4 laminate board.

Consider the example of a serial backplane (Figure 1) in which the distance a signal must travel can change substantially depending on which slot a board is plugged into. The signal attenuation and deterministic jitter imposed on the longer backplane trace will be greater than on the shorter trace. In scenarios such as this, it is often desirable to modify or “tune” the drive characteristics of the MGT transmitter to match the characteristics of a particular signal path, ensuring the highest possible signal quality and reliable recovery of the data at the receiver end.

## Solving the Backplane Dilemma

The RocketIO MGTs in Virtex-II Pro devices include many advanced features to simplify the development of serial I/O-based systems. The MGT blocks are composed of two distinct sub-blocks (Figure 2): the physical media attachment (PMA) block and the physical coding sub-layer (PCS) block. The PMA is responsible for the serialization and deserialization (SERDES) of the data stream as well as the actual physical interface for the

MGT transmitter and receiver. The PCS interfaces with the FPGA fabric and manages encode/decode functions, clock synchronization, clock correction, and channel bonding operations.

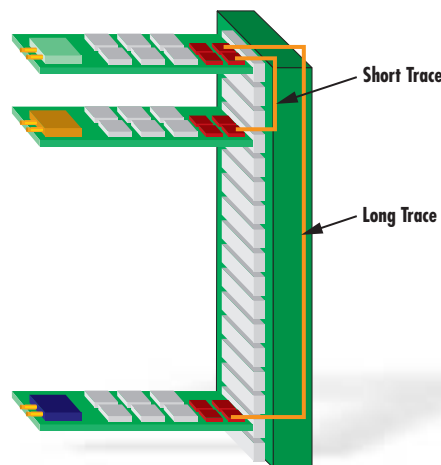


Figure 1 - The backplane distance dilemma

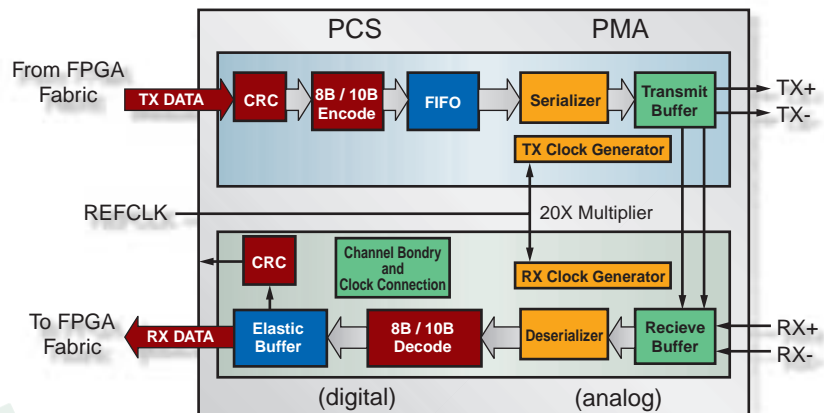


Figure 2 - RocketIO multi-gigabit transceiver

Among the list of other common SERDES functions, there are two programmable features contained within the MGT blocks to optimize transmission over a wide variety of signal topologies and transmission media:

- Programmable differential swing control
- Programmable pre-emphasis.

## Programmable Differential Swing Control

Virtex-II Pro MGTs have five levels of programmable differential swing control selec-

table through the RocketIO primitive attribute `TX_DIFF_CTRL`. The peak-to-peak swing at the output of the MGT transmitter can be varied from approximately 400 mV to 800 mV (800 mV to 1600 mV peak-to-peak differential) in increments of 100 mV. Adjusting the swing control level gives you the flexibility to meet the requirements of a wide range of serial I/O standards and ensures interoperability with many other devices over a variety of signal lengths and topologies.

## Programmable Pre-Emphasis

High-speed serial signals experience significant attenuation (signal loss) due to the “skin effect” and dielectric losses of the transmission medium, particularly over longer distances. Pre-emphasis is a technique whereby the highest-frequency components of the serial signal are boosted to compensate for

these losses, significantly extending the distance the signal can be reliably transmitted over a given type of conductor.

Virtex-II Pro MGTs have four levels of programmable pre-emphasis (from 10% to 33%) selectable through the RocketIO primitive attribute `TX_PREEMPHASIS`. At maximum pre-emphasis, RocketIO MGTs are capable of transmitting a 3.125 Gbps serial signal error-free over more than 40” of standard FR4 printed circuit board material (Figure 3).

The Adaptive I/O solution solves the backplane dilemma by giving you the abil-

ity to dynamically adjust the programmable swing control and pre-emphasis levels of the MGTs in response to changing signal topologies, while leaving the rest of the FPGA design unchanged. For example, referring again to Figure 1, the Virtex-II Pro MGT transmitter can be automatically configured to have different swing control and pre-emphasis settings in response to the changing trace length associated with each slot location.

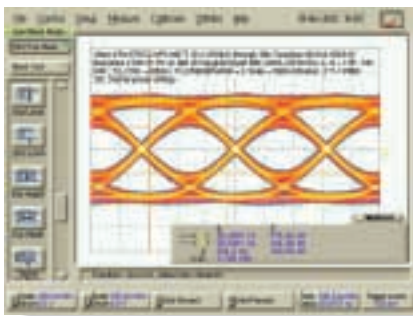


Figure 3 - 3.125 Gbps over 44" of FR4 with 33% pre-emphasis

Application Note XAPP660 ([www.xilinx.com/xapp/xapp660.pdf](http://www.xilinx.com/xapp/xapp660.pdf)), with complete reference design files, provides you with an entirely self-contained solution for dynamic configuration of the MGT swing control and pre-emphasis attributes (Figure 4). The PowerPC 405 core is used to perform reconfiguration of the MGT attributes via the internal configuration access port (ICAP), an interface similar to SelectMAP, which allows the FPGA configuration logic to be accessed over general interconnects inside the device.

After power-up and initial configuration with a base FPGA design, the PowerPC processor reads a 4-bit slot ID register to determine the swing control and pre-emphasis settings that should be assigned to each MGT for the given signal topology. The PowerPC core then modifies the MGT attributes by managing a partial reconfiguration of select configuration bits over the ICAP interface, leaving the rest of the FPGA design unchanged.

The slot ID can be a static code delivered from the backplane or a dynamic value driven by internal logic or another device.

The MGT attribute settings for each slot ID value are predefined with simple modifications to a "C" file array structure. The end result is that the MGTs can adapt to up to 16 different signal topologies automatically and provide optimal signal transmission without the need for separate bitstreams. The use of the PowerPC 405 core to manage the MGT attribute modifications results in a very resource-efficient design. The total solution consumes only 67 slices (about 2% of an XC2VP4 device), and can thus be easily integrated into almost any Virtex-II Pro design.

### Enhanced Characterization and Diagnostic Testing

In addition to managing the signal integrity aspects of multi-gigabit serial I/O design, significant time and resources can be spent on standards compliance, interoperability testing, and general characterization of the serial links during the development process. Furthermore, multi-gigahertz oscilloscopes, bit-error rate test (BERT) modules, and other required test equipment can quickly consume a good portion of your program budget.

The Adaptive I/O solution again offers a pre-engineered solution for simplifying the development and reducing the overall cost of MGT-based designs. Application Note XAPP661 ([www.xilinx.com/xapp/xapp661.pdf](http://www.xilinx.com/xapp/xapp661.pdf)), with associated reference design files, describes the Xilinx bit-error rate test (XBERT) module for enhanced characterization and diagnostic testing (Figure 5). The XBERT module includes a pattern generator capable of generating eight different pseudo-random bit sequence (PRBS) patterns as defined by ITU-T (International Telecommunication Union-Standardization Sector) Recommendation 0.150. It also includes a built-in error detector and frame/bit-error counters for tracking the total number of transmitted frames and total number of associated bit-errors.

The XBERT module is controlled and monitored by the PowerPC core over the processor local bus (PLB) interface. In addition, the PowerPC core reads the status of the frame and bit-error counters and then transmits this information to the

PLB-attached universal asynchronous receiver transmitter (UART). Using a standard serial cable connection to a PC, the UART can communicate with a simple PC terminal program such as Hilgraeve Inc.'s HyperTerminal, giving you the ability to control the bit-error rate testing from your keyboard and see the test results continuously updated on your PC screen.

Using the results from the XBERT module, a practical bit-error rate (for example,  $<10^{-12}$ ) can be calculated for your multi-gigabit serial links. And, because the XBERT is a soft implementation built from FPGA logic resources, it can be used for characterization or diagnostic testing and then removed from the final design. The XAPP661 reference design solution gives you the ability to perform sophisticated bit-error rate testing more efficiently and at a fraction of the cost of other solutions.

### Putting It All Together

The XAPP660 reference design provides the ability to automatically adapt the MGT transmitter attributes to meet changing signal topologies or other system requirements. And XAPP661 enables enhanced characterization or diagnostic testing of serial links with an interactive user interface.

However, the Adaptive I/O solution takes things one step further. Application Note XAPP662 ([www.xilinx.com/xapp/xapp662.pdf](http://www.xilinx.com/xapp/xapp662.pdf)) combines the XBERT characterization module of XAPP661 with the MGT partial reconfiguration capability of XAPP660 to provide a complete MGT development platform for real-time performance optimization, adaptive system calibration, and field diagnostic testing.

The XAPP662 reference design adds an ICAP controller interface to the internal PLB of the system described in XAPP661, adding the ability to modify the MGT differential swing control and pre-emphasis settings during characterization and diagnostic testing (Figure 6). Using a standard intellectual property interface (IPIF) module available from Xilinx, the ICAP controller module is easily integrated into the PLB-based system.

With this solution, you have the power to perform an iterative loop, alternating

between MGT attribute changes and bit-error rate testing through a command line interface on your desktop PC. The end result is a complete solution for real-time performance optimization and reliability

testing of your MGT serial links.

Portions of the XAPP662 reference design can also be easily integrated into your final design. The IPIF-to-ICAP interface module, for example, can be used in

any PLB- or OPB- (on-chip peripheral bus) based system to provide MGT attribute reconfiguration under control of the PowerPC core. This can be a preferred solution to XAPP660 for systems that already incorporate a PLB or OPB bus structure. In addition, any in-system communication link can interface to the on-chip UART, introducing the possibility of remote system upgrade or field diagnostic testing.

### Managing the Product Life Cycle

Together, the three components of the Xilinx Adaptive I/O technology provide you with solutions to help you manage your high-speed serial systems in all phases of the product life cycle. In the development phase, the ability to perform real-time performance optimization with interactive control over MGT attributes and the XBERT module provides you with rapid prototyping and efficient characterization.

In your fielded production design, the MGT partial reconfiguration controller of XAPP660 or XAPP662 gives you the power to automatically adapt your MGT transmitter characteristics in response to different signal topologies or changing system environments on the fly. This ensures that every link is optimized for performance and minimum bit-error rate without the need for multiple bitstreams or external components.

Lastly, the Adaptive I/O solution gives you the ability to perform in-field system calibration or diagnostic testing to ensure your end product is maintained for maximum reliability and performance.

### Conclusion

The Xilinx Adaptive I/O solution enables rapid prototyping, enhanced characterization, and in-system performance optimization of your multi-gigabit serial I/O designs. The combination of RocketIO MGTs and the IBM PowerPC 405 core provides you with a complete platform for developing, optimizing, and delivering world-class, high-speed serial solutions.

To learn more about the three reference designs that make up the Adaptive I/O solution, visit [www.xilinx.com/search/vsearch.htm](http://www.xilinx.com/search/vsearch.htm). ❏

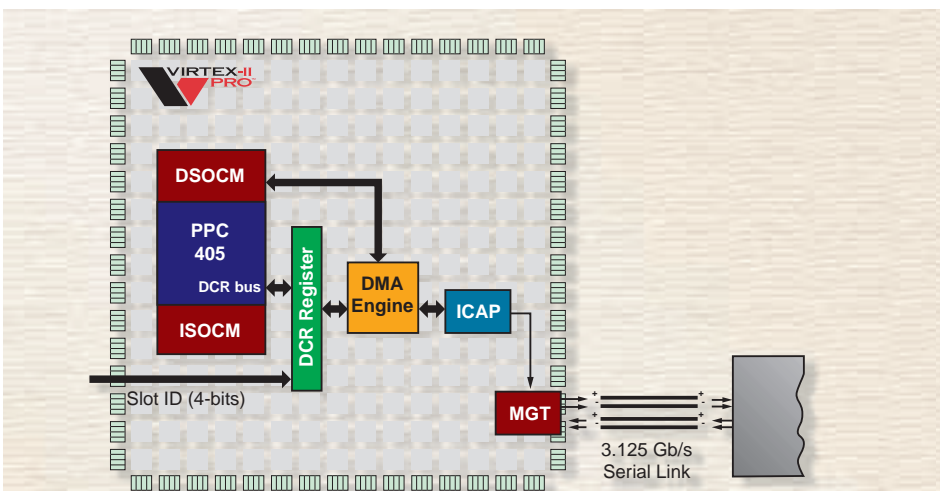


Figure 4 - Dynamic reconfiguration of MGT differential swing control and pre-emphasis attributes

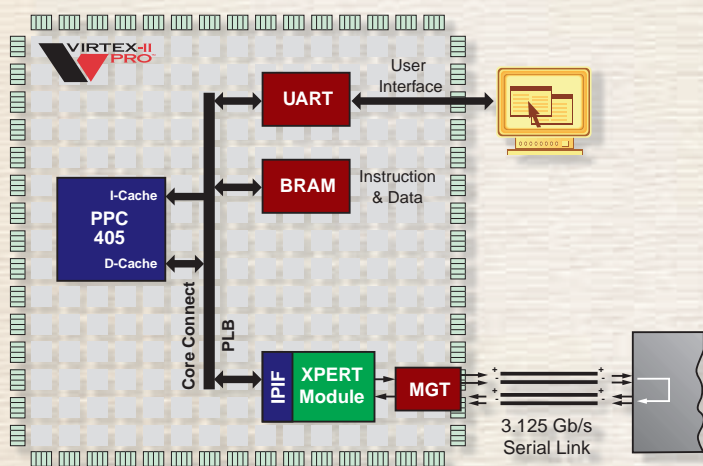


Figure 5 - XBERT module for enhanced characterization and diagnostic testing

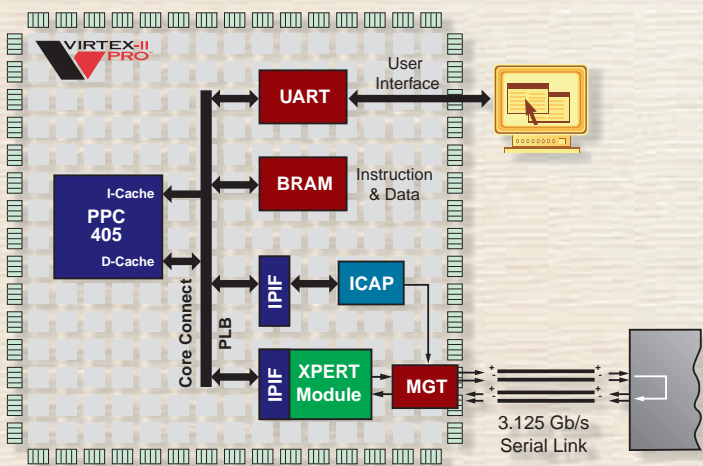


Figure 6 - Complete platform for real-time optimization of MGT serial links

# High-Speed Serial Interface Design: Learn Fast, Finish Faster

Xilinx Global Services provides you with the skills, courses, and information needed to meet the design challenges of FPGA programmable systems that interface embedded processors with multi-gigabit serial transceivers.

by Bill Okubo  
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With the tremendous increase in connectivity bandwidth requirements, our industry is experiencing a rapid move away from parallel interface architectures toward high-speed multi-gigabit serial standards.

Serial interfaces will ultimately be deployed in nearly every electronic product imaginable – including chip-to-chip interfacing, backplane connectivity, system boards, and box-to-box communications. Serial interfaces reduce system costs, simplify system design, and provide scalability to meet new bandwidth requirements. These emerging technologies sometimes require special knowledge in order to create high-speed serial I/O solutions – skills and experience that may be new to traditional programmable logic designers.

Service organizations play an increasingly important role in providing the knowledge about programmable systems needed to solve high-performance architectural challenges.

To ensure the success of design teams, while keeping overall cost down, Xilinx Global Services offers a complete portfolio of services for the Virtex-II Pro™ FPGA family. Xilinx Education Services, Xilinx Design Services (XDS), and support.xilinx.com all provide the experience and skills to help you successfully develop high-speed serial solutions and embedded systems, as well as FPGA logic design.

## Designing with RocketIO Transceivers

High-speed serial I/O channels can replace parallel buses in many systems and will result in lower overall costs – if designed correctly. These channels can significantly reduce board space and simplify board design while freeing I/O resources for other applications. To teach you how to create these high-speed serial designs efficiently, Xilinx provides training designed to reduce significantly the rigors of getting up to speed on this new technology.



Designing with RocketIO Multi-Gigabit Transceivers is a two-day course that teaches how to fully utilize RocketIO™ transceivers in Xilinx Virtex-II Pro FPGAs. By mastering the details of high-speed serial designs, you learn to develop fast and efficient serial interfaces that will operate flawlessly. In addition to classroom instruction, more than half of this class is taught in the lab, where you learn how to efficiently synthesize, implement, and debug designs.

Designing with RocketIO Multi-Gigabit Transceivers teaches you the skills necessary to:

- Fully utilize the ports and attributes of RocketIO transceivers
- Effectively use advanced RocketIO features such as CRC, channel bonding, clock correction, comma detection, 8b/10b encoding, programmable termination, and pre-emphasis
- Use the Architecture Wizard to instantiate RocketIO primitives in designs
- Achieve compatibility with high-speed I/O standards using RocketIO
- Recognize and understand the data streams of popular communications standards such as Gigabit Ethernet and PCI Express.

### **Xilinx Design Services Has RocketIO Expertise**

Designers who work with Virtex-II Pro FPGAs need to know with certainty that the RocketIO multi-gigabit transceivers (MGTs) will perform according to their specific requirements. To allow the measurement design parameters such as bit-error rate, latency, and resynchronization time, and physical-layer characterization involves the building and reuse of embedded hardware and software systems on Virtex-II Pro FPGAs. XDS has experience with and access to various Xilinx characterization boards to carry out such measurements.

Experience with partial reconfiguration of RocketIO MGTs is also important when you're designing Virtex-II Pro FPGAs. For example, electrical transmission characteristics commonly vary from serial link to serial link depending on the



distance of the link. Partial reconfiguration offers you a way to avoid storing multiple bitstreams on a system, allowing each system's RocketIO configuration to be personalized using either on-board switches or software control. Partial reconfiguration can also be used to switch a RocketIO channel from one physical standard to another without any service disruption on the unaffected channels.

In addition to providing partial reconfiguration under software control, XDS has embedded software expertise to help you deliver fully integrated and dynamically configurable systems. XDS can help you develop the high-level communications protocol for FPGA programmable logic and embedded software.

### **Web-Based Tech Tips**

A comprehensive support resource is essential to fast design cycles and first-time success for a new serial I/O design. Available 24/7, [support.xilinx.com](http://support.xilinx.com) has online information on the latest downloads, techXclusives, and other recent support-related news. MySupport.xilinx.com can be personalized so that you see only the information related to the devices that

you use, such as data sheet updates for Virtex-II Pro FPGAs.

Tech Tips for RocketIO is a new support tool that includes information such as:

- RocketIO FAQ
- Documentation about RocketIO
- Top Answers for RocketIO.

### **Conclusion**

Before you start your next high-speed serial design, save yourself time and effort by taking advantage of the skills and experience offered by Xilinx Global Services. Learn more about the services available for RocketIO MGTs at: [www.support.xilinx.com/support/gsd](http://www.support.xilinx.com/support/gsd).

The course description for Designing with RocketIO MGTs is available at: [www.support.xilinx.com/support/training/abstracts/rocketio.htm](http://www.support.xilinx.com/support/training/abstracts/rocketio.htm).

For information about the serial I/O expertise of Xilinx Design Services, see: [www.support.xilinx.com/xds](http://www.support.xilinx.com/xds).

RocketIO Tech Tips are available on [support.xilinx.com](http://support.xilinx.com) at: [www.support.xilinx.com/xlnx/xil\\_tt\\_home.jsp](http://www.support.xilinx.com/xlnx/xil_tt_home.jsp). ❧

# Kit for Cadence SPECCTRAQuest Tools Speeds RocketIO Designs

Instead of taking weeks, you can now create and verify gigahertz-speed serial links on PCBs in days.



by Xcell Staff

More than 500 designers and engineers have downloaded the Xilinx RocketIO™ Design Kit for Cadence Design Systems' SPECCTRAQuest™ design and analysis environment for high-speed digital systems. Customers have clearly been pleased with the kit's results in shortening time-to-market and reducing costs.

The design kit helps reduce the time needed to implement Virtex-II Pro™ RocketIO transceivers because it takes advantage of concurrent design efficiencies using technologies that address silicon, package, and board design.

The kit acts as an electronic blueprint that enables you to create, implement,

and verify gigahertz-speed serial links quickly. Operating within the Cadence SPECCTRAQuest Signal Integrity Expert environment, the kit is a proven approach for characterizing the interactions between the Xilinx Platform FPGA and the rest of the system.

The design kit is the result of an alliance between Xilinx and Cadence to help you exploit the capacity and performance of the Xilinx Virtex-II Pro FPGA family. "Our customers' ability to quickly design-in the Virtex-II Pro Rocket IO technology is critical," said Rich Sevcik, senior vice president and general manager of FPGA products at Xilinx. "By working with Cadence, we can minimize the design-in time for our mutual customers."

## Unique Features

The RocketIO Design Kit for SPECCTRAQuest allows you to develop optimal constraints for PCB systems. The constraints drive the PCB floorplanning, routing, and verification process. The RocketIO Design Kit for SPECCTRAQuest includes:

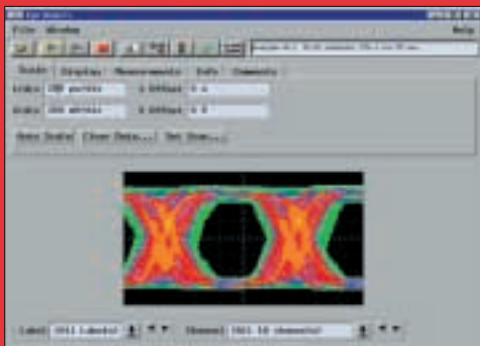
- Ready-to-simulate system-level topologies for typical use of the device on the board/system
- Verified I/O buffer models
- Large package model
- Test-bench and correlation data
- Connector models for backplane applications
- Device-specific scripts and tools to evaluate simulation results
- Instructional video describing how to get started with the design kit.

## Price and Availability

The RocketIO Design Kit for SPECCTRAQuest is provided free to Xilinx customers who have signed the appropriate non-disclosure agreement. More information is available at [www.support.xilinx.com/](http://www.support.xilinx.com/). The Cadence SPECCTRAQuest Signal Integrity Expert product starts at a U.S. list price of \$24,200 for a one-year license. For pricing outside of North America, contact your local Cadence office or distributor. More information regarding other Serial Tsunami design resources is available at [www.xilinx.com/serialsolution](http://www.xilinx.com/serialsolution). ❧

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*Eye displays in a logic analyzer can show voltage and time data from multiple channels simultaneously, helping you spot sub-nanosecond problems in much less time than conventional methods.*

It's a never-ending cycle: Every new generation of processors and buses means a new need for speed—in your customers and in you. As edge rates go sub-nanosecond and schedules get shorter, signal integrity problems get tougher just when you need to solve them faster and with fewer compromises. Perhaps we can help.

Working with designers around the world, we've seen scope probe loading lead many people down a wrong road. Probe impedance varies with frequency, so it can cause errors in bias, amplitude, offset, rise time and propagation delay. The circuit may even stop or start whenever you connect the probe.

You can reduce or eliminate these problems with an active probe, which provides high resistance, low capacitive loading, a flat response—and a more accurate view of what's really happening in your circuit. Sharing tips like this is just one of the ways Agilent can help you find the causes of signal integrity problems now and design them out next time.

**There's more where this came from at [www.agilent.com/find/moresi](http://www.agilent.com/find/moresi), where you can download application notes about probing, normalization, de-embedding and more, order a CD-ROM, and attend a series of FREE signal integrity eSeminars.**

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# Software-Compiled System Design Optimizes Xilinx Programmable Systems

Celoxica and Xilinx have partnered to fine-tune software-compiled system design for the benefit of designers using Virtex-II Pro and MicroBlaze programmable systems.

We cannot solve our problems with the same thinking we used when we created them.

– Albert Einstein

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Okay, so none of us will claim to be Einstein, but programmable system design might be the next development challenge we face.

With the advent of the Xilinx Virtex-II Pro™ Platform FPGA and the MicroBlaze™ soft processor, we now have access to unrivalled levels of product flexibility and performance. This technology – for the first time – enables us to partition and re-partition systems between hardware and software at any time during the development cycle. We can even re-partition the hardware and software mix after the product has gone to market. This complete reprogrammability means the system can be optimized over and over again.

But for design teams looking to use this powerful technology, system design can be a challenge. Exploring whether a design is even feasible can cost many months of time, effort, and expense, let alone finding the optimal design. And if system verification does not begin right from the start, projects can miss their specifications or take too long to get to market – reducing your ability to compete, your business credibility, and your all-important bottom line. It's a design headache you don't need.



## Meeting the Design Challenge

A remedy for this headache is the synergy of software-compiled system design and programmable systems technology. Software-compiled system design is a methodology that provides a seamless bridge between hardware and software (Figure 1). It enables the system partition, verification, and hardware/software co-design to be driven directly from the system specification. Software-compiled system design was specifically developed for programmable systems and provides an efficient, cost-effective, and quality driven co-design solution.

## Software-Compiled System Design

At the heart of software-compiled system design is the principle of providing a direct link between the programmable platform and the originally defined system functionality. This provides the necessary system verification flow and offers confidence to the designer who wants to fully explore the design space – pushing the envelope of design innovation and product differentiation.

The methodology also deploys novel technology that permits more informed and flexible hardware/software partitioning. This enables tradeoff analysis, partition and re-partition at any stage in the design, and by using higher level languages (HLLs) for both hardware and software design, the methodology allows the system specification to be written in a form that both teams can immediately use, without costly and time-consuming rewrites.

## So Prove It

To demonstrate the capabilities of software-compiled system design, Celoxica and Xilinx partnered to undertake the co-design of a JPEG 2000 codec (compressor/decompressor) for implementation in a Virtex-II Pro FPGA. In particular, we wanted to address the design challenge of system partitioning, co-verification, and the easy integration of hardware and software.

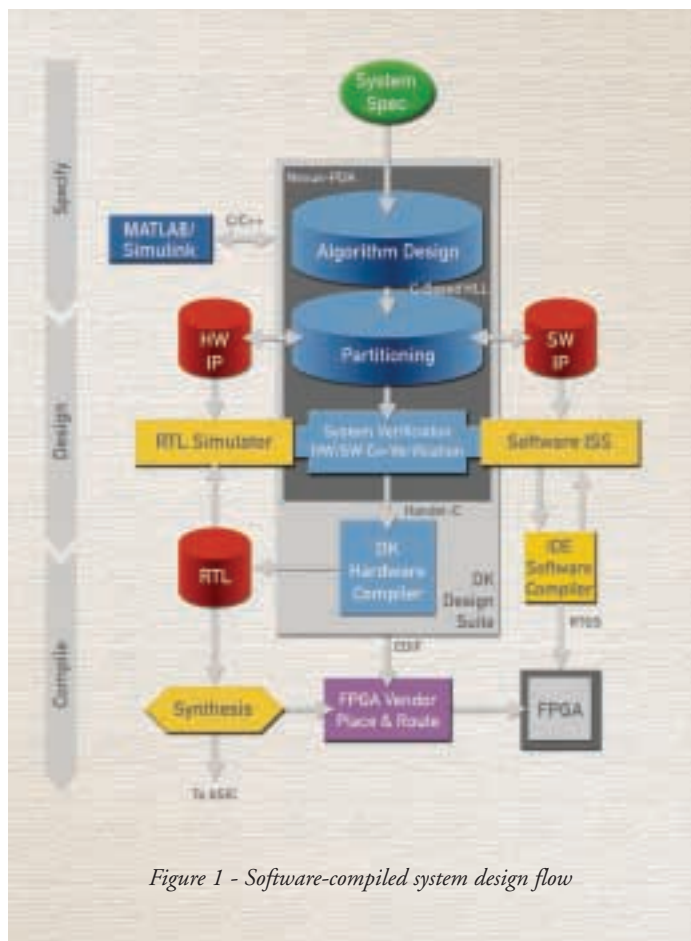


Figure 1 - Software-compiled system design flow

JPEG 2000 is a standards-based image coding system that uses state-of-the-art compression techniques based on wavelet technology (Figure 2). Its architecture lends itself to a range of uses from consumer electronics, such as digital cameras, to medical imaging, remote sensing, surveillance systems, and scanners.

## Project Specifications

- Maximize overall system performance
- Innovate and differentiate from the competition
- Demonstrate an efficient and effective co-design environment
- Use software specification as a starting point for system design
- Improve communication between hardware and software design teams
- Simplify partitioning and migration of code between software and hardware for better overall Quality of Design (QoD)

- Demonstrate a complete system verification flow
- Deliver competitive Quality of Results (QoR)
- Exceed time-to-market expectations
- Support design re-use strategies
- Maximize current EDA and IP investments.

## Project Plan

- Phase 1: Profile and verify
- Phase 2: Partition and verify
- Phase 3: Design and verify
- Phase 4: Implement and verify

## Tools

- Celoxica Nexus PDK
- Celoxica DK Design Suite
- Wind River Xilinx Edition toolset
- Xilinx ISE 5.1i

## Phase 1: Profile and Verify

A multitude of applications can benefit from hardware acceleration and product flexibility. To demonstrate this, we selected JPEG 2000; our starting point for the design was the C specification code.

To drive our system verification flow, we ran the specification code through an appropriate target – in this instance the IBM PowerPC™ 405 GP. From this we simulated and verified the functionality of our system and established a test bench that remained constant and consistent throughout the design.

We then began code profiling to establish where our program spent its time and determine which functions called other functions during execution. We found profiling was useful, as it quickly identified the functions in a program that were processor hungry or compute intensive. That made them possible candidates for offload into the FPGA fabric. However, the profiling does not analyze dataflow between hardware and software, nor burst

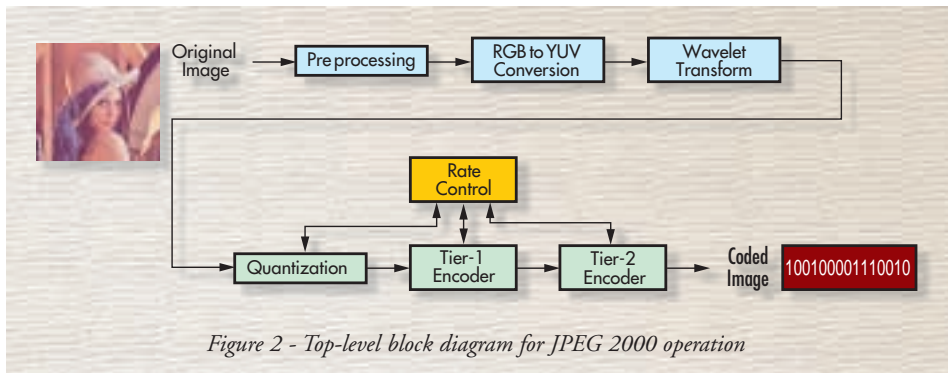


Figure 2 - Top-level block diagram for JPEG 2000 operation

length or frequency, so designer intervention is mandatory to understand the dynamics of our hardware/software interaction.

Using Wind River's WindView™ visualization and diagnostic tool, we determined that the DWT (discrete wavelet transform) and Tier 1 encoder were the processor-intensive functions, consuming 87% of processing time (Figure 3). We selected them for further scrutiny and tradeoff analysis.

### Phase 2: Partition and Verify

Validating the system partition against the requirements of the design specification is cardinal in programmable system design. Typically the system designer maps a system-level architecture into specific hardware and software components, making direct reference to the project specification and factors such as component availability, cost, and technical feasibility.

The consequences of the system partition cascade through the design flow to physical implementation and final system performance is greatly dependent upon partitioning decisions. It makes little sense to invest time, money, and effort optimizing and refining an incorrect partition – it is inherently sub-optimal.

Uniquely, software-compiled system design provides the designer with a flexible partitioning capability that permits partition and re-partition at any stage in the design process. Moreover, it is linked to a verification flow that enables the

designer to confidently explore and innovate in the design space, analyzing hardware/software tradeoffs, and identifying the optimal system partition for the best QoD.

Facilitating this is the data streaming manager (DSM), a portable co-design API (Figure 4) supplied with Celoxica's DK Design Suite. Developed specifically for programmable system partitioning and

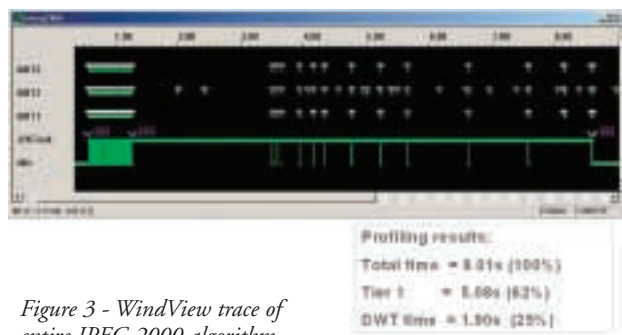


Figure 3 - WindView trace of entire JPEG 2000 algorithm

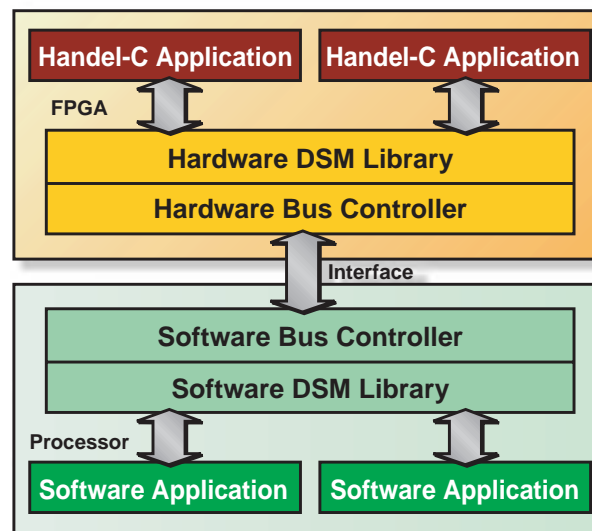


Figure 4 - DSM portable codesign API

hardware/software integration, the DSM allows the designer to iteratively explore, test, and verify multiple partition alternatives. The designer can quickly create and easily move ports that are used to send data between the software and hardware by using the API standard (Figures 5 and 6). As each option is explored, the designer can verify the partitioning with the software used as a test bench throughout the project.

In our project, the DSM validated the profiling information determined in Phase 1 of our design flow. It helped analyze the data flow and the burst length and frequency between our hardware and software, and fine-tuned the partition to meet the project's criteria. Moreover, the DSM's inherent portability meant the design could be repartitioned at any stage in the design flow, redefining the system architecture and easily accommodating late specification changes.

### Phase 3: Design and Verify

With the optimal partition determined and verified, we began the design optimization phase of our project. Software-compiled system design makes use of HLLs for both hardware and software design. HLLs allow the system specification to be written in a form that both the hardware and software teams can immediately use – without costly and time-consuming rewrites. Additionally, HLLs simplify the migration of code between hardware and software. Because there is a common language base and common level of abstraction between the hardware and software, there is improved communication and shared understanding between the development teams.

As we did in our partitioning phase, we used the DSM throughout the design optimization phase. The DSM provided a functionally accurate simulation environment that allowed our hardware and software to interact – keeping them connected throughout design optimization (Figure 7).

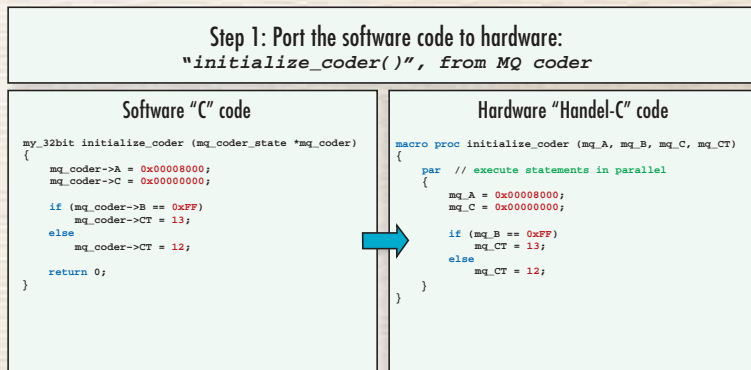


Figure 5 - Porting software to hardware

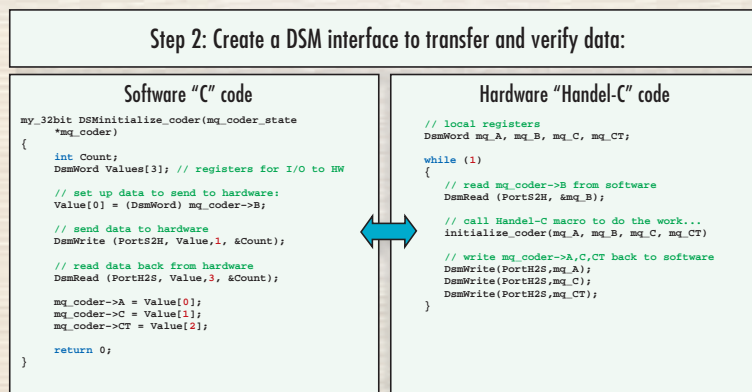


Figure 6 - Setting up the DSM interface to test and verify partition alternatives



Figure 7 - Functionally accurate simulation environment

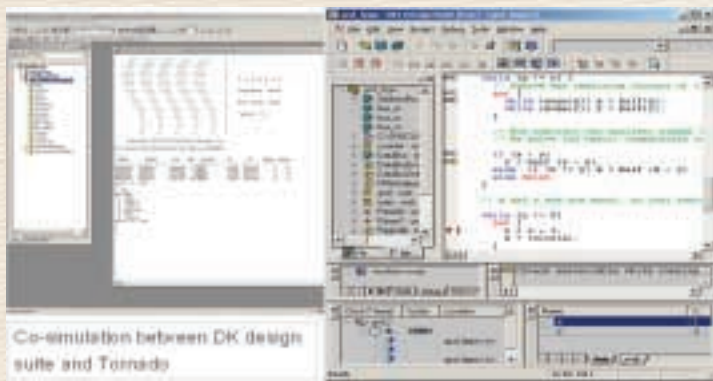


Figure 8 - Co-simulation between Celoxica's DK Design Suite and Wind River's Tornado visualization and debugging environment

The software was run as a native executable on the PPC 405 GP, and the hardware was run using the simulation and debugging capability of Celoxica's DK Design Suite. We used a utility program to monitor the data passing between the applications to assist with debugging. Because all of the API functions were provided, this allowed complete system development to begin – without the development platform being available. Once we got it working, the application was easily transferred to the target platform for final testing. Co-simulation between hardware and software was made possible by connecting DK with the Tornado™ environment from Wind River (Figure 8).

As our system specification was described in ANSI-C, we progressed our design in ANSI-C and used hardware language extensions defined in Handel-C to describe our hardware. These hardware extensions enable, for example, efficient control over area, timing, clocks, RAMs, ROMs, and interfaces.

Combining multiple DSM calls, we made optimizations to the software. And we applied hardware optimization techniques, such as increasing parallelism, replacing for() loops with while() loops, pipelining, and syntax duplication.

### Specification Change

At this stage in the design, a specification change was introduced. A novel lifting algorithm was developed that performs a two-dimensional DWT and thus provides faster processing time. The algorithm was readily available as a HDL IP block, and we decided, with respect to design time and maximizing IP investment, to integrate the IP into the design as a black box. The integration was simplified by using the interface declaration available in Handel-C for connecting third-party IP into a software-compiled system design flow (Figure 9).

### Phase 4: Implement and Verify

Implementation to the target platform was simplified by using the platform abstraction layer (PAL). The PAL shields designers from

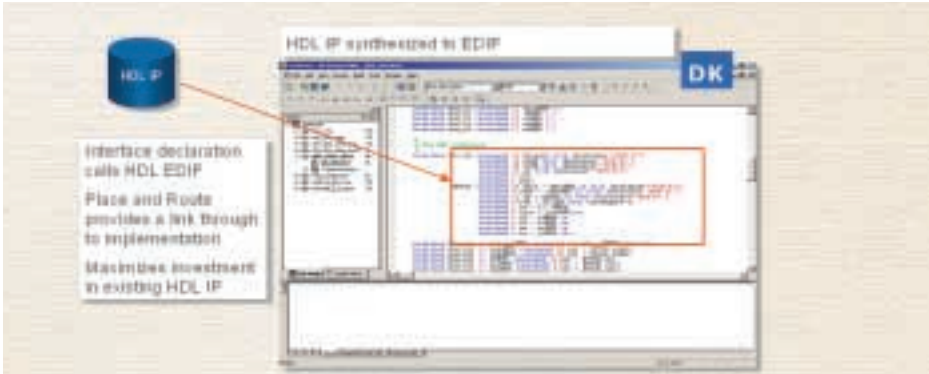


Figure 9 - Interface declaration “black-boxed” HDL IP into a software-compiled system design flow

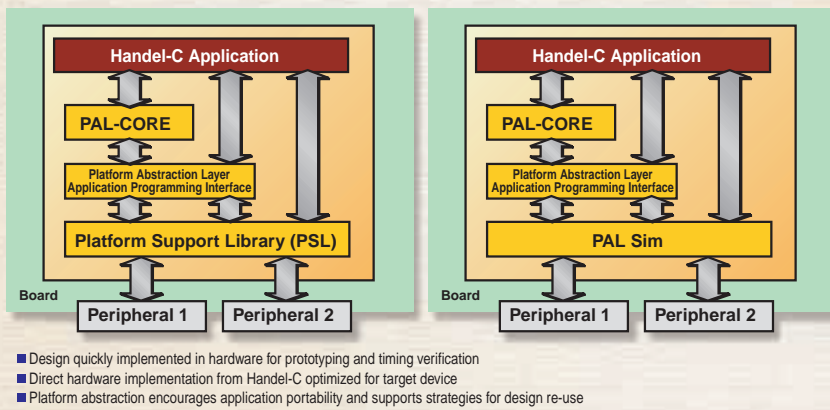


Figure 10 - PAL block diagram

Figure 11 - Virtex-II Pro prototyping platform ▶



Figure 12 - Virtex-II Pro ML300 evaluation platform ▼



low-level hardware interfaces, easing the integration of FPGAs with physical resources. This is done by developing a library of low-level interfaces to specific platform resources, such as I/O or memory. This library, called the platform support library (PSL), is then accessed by the hardware application on the FPGA using a simple and consistent application programming interface – the PAL API (Figure 10).

The target platform was a Wind River SBC405GP (single board computer reference design) with a Proteus FPGA daughter card, effectively a Virtex-II Pro prototyping platform (Figure 11). This development environment supported timing simulation, emulation, and block optimization, and it was used prior to final implementation in a Virtex-II Pro ML300 Evaluation Platform (Figure 12).

Object code was compiled into the PPC405GP under Wind River’s VxWorks™ RTOS, with the hardware implementation using the direct EDIF output generated by Celoxica’s DK Design Suite. This EDIF netlist was optimized for the Virtex-II Pro Platform FPGA (Figure 13), ensuring maximum efficiency for best QoR. Optionally, the DK Design Suite can also output RTL-level VHDL or Verilog, pre-optimized for traditional synthesis tool flows (Figure 14).

## Results

The results (Tables 1 and 2) from the Celoxica DK Design Suite were compared to the handcrafted VHDL authored by a JPEG 2000 domain expert. Handel-C’s systematic and ANSI-C-like approach to the problem led to substantial savings in design time. An expert Handel-C engineer with no prior knowledge of the JPEG 2000 standard was able to get the algorithm to a working hardware implementation in less than half the time it took to code the VHDL.

The other key success we had was that the design was easily able to meet the system timing constraints. The results provide clear validation that design abstraction leads to increased designer productivity without necessarily compromising performance or area.

**Conclusion**

Software-compiled system design is a proven methodology for programmable system co-design. It provides a solution for system partitioning, co-verification, and hardware/software integration across a spectrum of design styles and applications.

For use by all members of your design team, from the system architect to the verification engineer, software-compiled system design enables code sharing between hardware, firmware, and software designers from system specification through to implementation.

The Celoxica DK Design Suite is a fully featured development toolset that enables a complete implementation of a software-compiled system design. It is interoperable with popular third-party tools and languages and provides fast co-simulation between C/C++, Handel-C, HDLs, instruction set simulators (ISSs), and modeling languages such as Open SystemC™ and MATLAB™.

Software-compiled system design methodology offers you compelling benefits, and it is an efficient and effective design strategy for Xilinx programmable systems. ❌

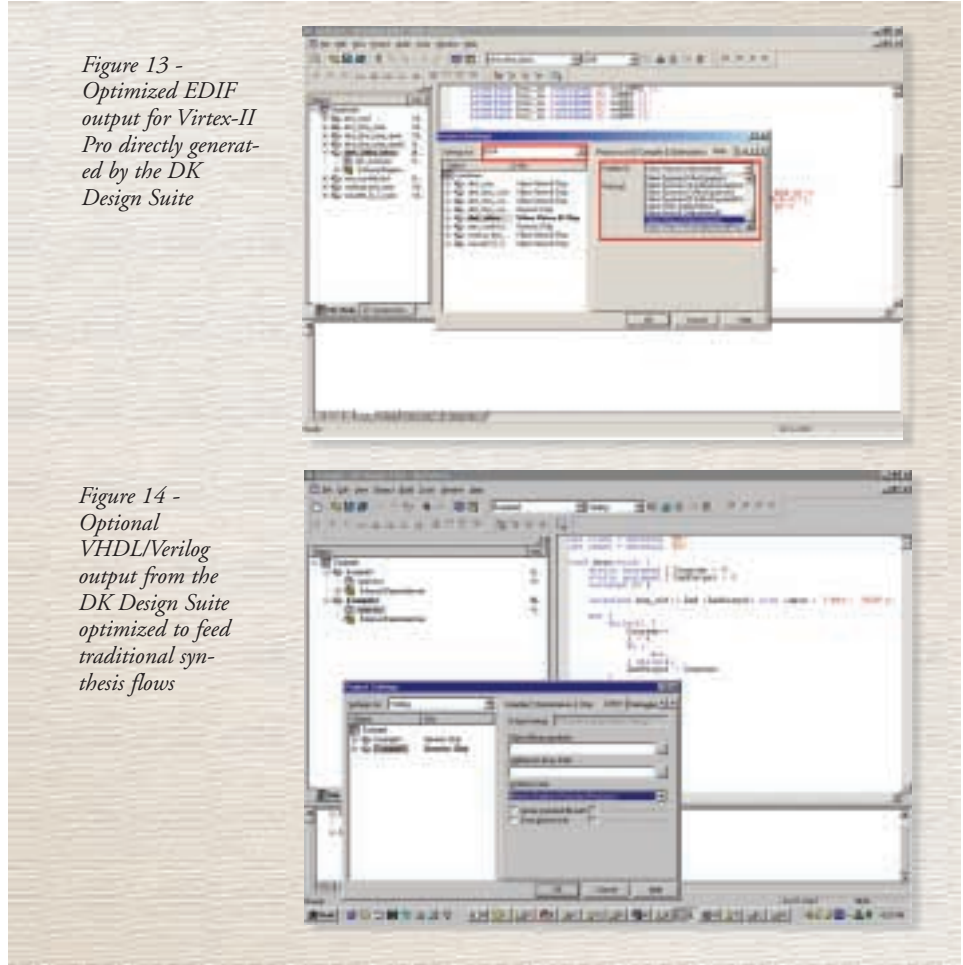


Figure 13 - Optimized EDIF output for Virtex-II Pro directly generated by the DK Design Suite

Figure 14 - Optional VHDL/Verilog output from the DK Design Suite optimized to feed traditional synthesis flows

Celoxica 1st pass		2nd pass	Final	HDL	Observations
Slices	646	546	758	800	Comparable
Device utilization	6%	5%	7%	7%	
Speed (MHz)	110	130	151	128	HC faster
Lines of code	386	386	395	435	
Design time (days)	6	7 (6+1)	7 (6+1)	20*	HC quicker
*Lena used as testbench throughout, input bit width 12, max 1k image				*Doesn't include partitioning spec. development	
					Expert vs. Novice

Table 1 - Rapid Handel-C (HC) implementation for area efficiency

Celoxica 1st pass		Celoxica Final	HDL	Observations
Slices	1.347	1.999	620	HDL smaller
Device utilization	12%	18%	6%	
Speed (MHz)	89.5	115.5	76	HC faster
Lines of code	310	330	800	
Design time (days)	10	12 (10+2)	30*	HC quicker
Average cycles per code block	108	108	67.5	
Processing time (per code block ms)	1.206	0.939	0.888	HDL faster
Simulation time for Lena JPEG	5 mins	5 mins	Hours	Expert vs. Novice

Table 2 - Rapid Handel-C implementation for performance optimization

\*Doesn't include partitioning spec. development

# Tarari and Celoxica Deliver Fast and Easy Algorithm Acceleration

Hardware acceleration speeds the entire design cycle, and the combination of Tarari's Content Processing Platform and Celoxica's DK Design Suite makes it fast and painless.

by Dale Riley  
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Traditional methods of porting algorithms for hardware acceleration usually require many steps that are both difficult and time-consuming. The algorithms must be ported to a hardware language, simulated by themselves, and then prototyped on FPGAs.

During this prototype stage, the FPGA must also connect to the software environment. The complete task often requires a team of hardware engineers well-versed in FPGA development, another hardware engineer to develop the platform, and a software engineer to write the interfaces from software to hardware. In addition, software developers must wait for the hardware to be completed and tested before integration.

Software developers can get a head start on developing and debugging software using the Tarari Content Processing Platform™ (CPP) and the Celoxica DK Design Suite to co-simulate the algorithm and quickly convert new or existing C code to hardware for significant acceleration. Celoxica's C-to-gates technology eliminates the language conversion step. Tarari's CPP eliminates the need to understand the complexities of interconnects and software interfaces, enabling developers to concentrate on performance rather than functionality.

## Tarari Content Processing Platform

The concept of hardware acceleration is a simple one: Create a piece of hardware dedicated to completing tasks much faster than software or general-purpose hardware. The reality of creating that piece of dedicated hardware, however, is much more complex.

Consider just a PCI interface. It has a bus with several possible configurations, such as 32- or 64-bit buses, or 33- or 66-MHz clocks. During operation there are many states and conditions to keep track of and control. Even SDRAM has somewhat complex controls. You could buy each of these elements of the design, but then you would have to create interfaces and control mechanisms between them and tie them all together.

All of this work has been completed with the Tarari CPP.

Figure 1 shows a block diagram of the Tarari CPP that includes:

- A half-length PCI-compliant card
- 32- or 64-bit bus width operating at 33- or 66-MHz bus speeds
- 256 MB of DDR SDRAM for high-capacity global storage
- LEDs for status and debug

- 4 MB of ZBT SSRAM for high-speed, low-latency local storage
- A 2M-gate XCV2000 Virtex™-II Platform FPGA performing as the content processing controller (CPC) that:
  - Provides all connectivity between the PCI Bus, DDR SDRAM, and content processing engines (CPEs)
  - Dynamically reconfigures FPGAs
  - Hosts core content processing logic
  - Has maximum total data throughput of 4 GBps
  - Supports bus-master direct-memory-access (DMA) mode.
- Two independent content processing engines (CPE) each consisting of:
  - A 1M-gate XC2V1000 Virtex-II Platform FPGA
  - Independent busses for fast algorithmic processing and continuous operation during reconfiguration
  - Dynamic reconfigurability, allowing upgrades via software.

The Tarari CPP is a fully developed PCI card with three Virtex-II FPGAs. The three

Xilinx FPGAs are located under the fan/heat sink/shroud assembly as shown in Figure 2. This placement ensures that the components don't overheat. The FPGAs require external cooling because they are pushed to their performance limits in terms of clock speed and there is little to no airflow to cool them.

All data flow and control logic is implemented on the CPC. Using DMA technology, the CPC can act as a PCI bus master, allowing data transfer between the host system memory and the onboard DDR SDRAM. The bandwidth of the DDR SDRAM is approximately four times the bandwidth of the PCI or CPE buses. This high bandwidth allows the CPC to multiplex accesses to the memory and makes it appear that multiple devices are simultaneously accessing the memory. Finally, the CPC controls programming of the CPEs for fast reconfigurability.

The Tarari CPP contains the entire support infrastructure needed to deploy a PCI solution, allowing you to focus on algorithm development rather than on hardware implementation details. Another key advantage is time to market; using the Tarari CPP allows you to skip the work involved in designing the PCI infrastructure and bypass all of the manufacturing steps as well. The card is

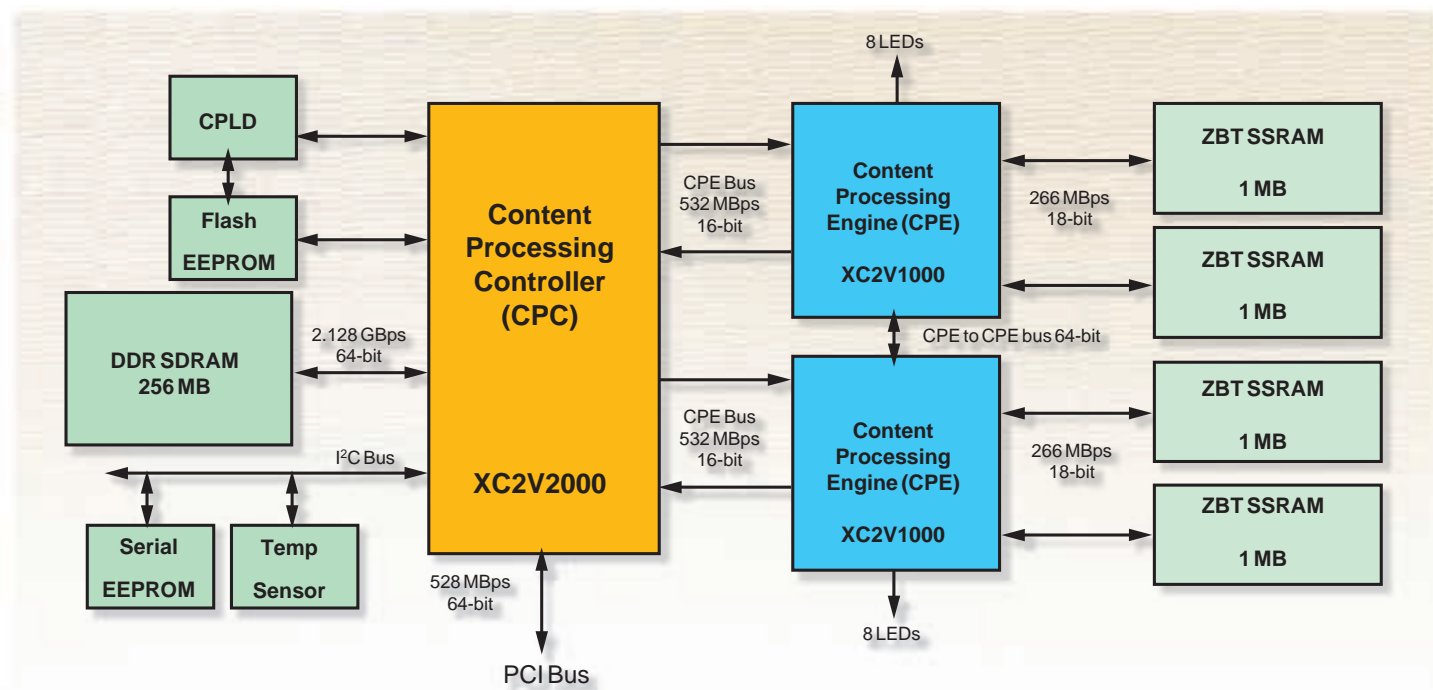


Figure 1 - Tarari Content Processing Platform block diagram



Figure 2 - Tarari PCI card with three Xilinx Virtex-II FPGAs located underneath heat sink/fan shroud

delivered to you ready for production deployment. Your algorithm firmware can be downloaded to the card at runtime, and no hardware customization is required. Plug it in and start accelerating.

### Development Flow

The first step is to select an algorithm for hardware acceleration. Selection is usually done using profiling tools that identify software bottlenecks. The next step is to determine memory usage, dataflow, and suitability of the identified code sections that will be implemented in an FPGA. The following step is to estimate the size, speed, and performance metrics at each stage of the design cycle. With so many parameters to consider, designers increasingly rely upon hardware/software co-design, co-simulation, and prototyping as essential elements of the development flow.

The Tarari CPP is built on the development framework shown in Figure 3 to meet these needs. The flow emphasizes rapid development with a common C-based language for both hardware and software components. This allows maximum experimentation and exploration of the design space for better quality of design.

Using this framework, you can:

- Create system models directly from the

original software application and verify the functionality and characteristics of a system.

- Quickly identify and extract critical portions of the algorithms as candidates for hardware implementation.
- Make informed partitioning decisions for optimum use of hardware resources and verify performance and functionality in simulation.
- Perform cycle-accurate hardware simulations.
- Directly implement C-based hardware designs onto the Tarari CPP.

This approach reduces the time it takes to design accelerated applications, thus lowering cost, improving time to market, and minimizing risks.

### Applications

The best candidate algorithms for hardware acceleration with Tarari's CPP board fit one or more of the following criteria:

- High operation-per-byte ratio
- Benefits from running multiple instantiations (parallel processing, multi-threading)
- Capable of being pipelined

- Takes advantage of wide data widths
- CPU execution time far exceeding data transfer time over PCI.

Where these criteria are met, there has been considerable success with FPGA solutions for the following applications:

- Security/encryption – RSA, DES/3-DES, SHA, MD5, AES/Rijndael
- Streaming applications – video processing, pattern matching/filtering, compression/decompression
- Vector engines.

Candidate products and applications incorporating these basic hardware blocks include:

- Network security
- Media streaming
- XML/Web services accelerations
- Image processing
- High-performance computing applications.

### Algorithm Example

The GZIP (GNU zip) algorithm is a commonly used utility that compresses and decompresses data files using the “Deflate” and other patent-free algorithms at [www.gzip.org](http://www.gzip.org). The key feature of GZIP decompression is that it operates on a 1-bit wide stream of data, requiring that all operations reading from the input data stream are performed sequentially. Although GZIP decompression fulfills a limited number of the algorithm selection criteria described above, the results demonstrate that the general technique of offloading a CPU and exploiting algorithm parallelism can improve system performance.

### Porting GZIP C Source Code to Handel-C

To reduce the time required to implement the GZIP decompression, GNU C source code was used for the example. The majority of the algorithm was used with little or no modification to provide an immediate basis for prototyping and a controlled test framework in which to enhance and optimize the



algorithm. Making use of Handel-C's simple support for parallelism via the `par{}` construct is an example.

The process for porting the GZIP algorithm to hardware was to write the code for one "module" of the system at a time in Handel-C. Note that the modules correspond to algorithmic stages in the decompression algorithm, as shown in Table 1, rather than more traditional hardware blocks.

maximum performance. Consequently, for this improved performance, a simple interface eliminated the double clock constraint by using pipelined access to the block RAM.

### LZ77 Decompressor

The main component in the hardware implementation is the "sliding window," which is 32 KB in size with byte-wide access. The sliding window is built using

the pipelined block RAM access macros mentioned above. Copy operations resulting from a length/distance pair are performed using a pipelined loop as shown in the code in Figure 4, which reads from one port of the sliding window block RAM and writes back to the other port. This results in fast operation by processing one byte every clock cycle once the pipeline is full.

### Simulation Testing of GZIP Modules

A significant advantage of developing a GZIP decompression algorithm in Handel-C is that the simulator can be used to test the functionality of the design before implementation. These simulations are performed rapidly – a model of the entire GZIP decompression algorithm can simulate 100 KB of compressed data in 25 seconds or less on a Pentium™ III 850 MHz system. During development of each GZIP module in Handel-C, we conducted simulations to verify their operation. The software GZIP source code was modified to produce test harnesses implemented as C functions called directly from the Handel-C code.

### Data Throughput

Given the maximum clock rate of the design to be 133 MHz – verified by using the Xilinx ISE 5.1i timing analyzer – the data throughput of the GZIP decompression algorithm was calculated from simula-

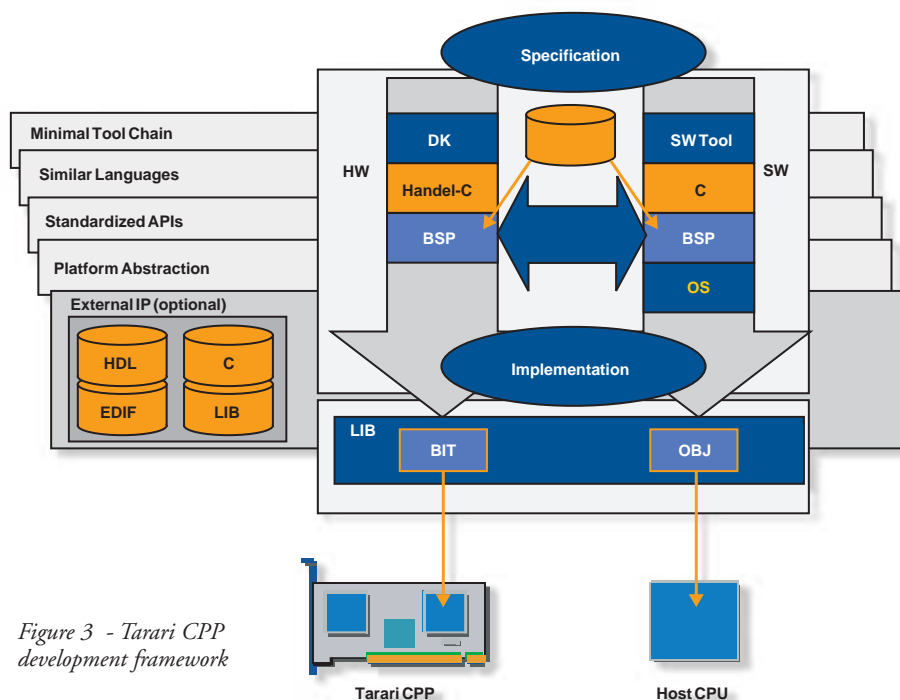


Figure 3 - Tarari CPP development framework

### Optimized Block Memory Accesses

The Handel-C language supports the use of block RAM by adding the specification with `{block=1}` after a RAM declaration. This specification results in using block memory to build the RAM and generating a RAM clock at double the algorithm clock rate, which is used to implement single-cycle access to the block RAM. This process provides a quick route to hardware prototype for the design.

However, using the single-cycle block RAM access limits the algorithm clock rate to half of the RAM clock rate. Some portions of the GZIP decompression algorithm are sequential in nature, so a high clock rate is desirable to achieve

```

void Decompress(...)
{
...
while(1) par
{ //1 byte per cycle once pipe is full
...
ReadWindowAddr(CopyPos); // Pipe Stage 1 - Set address
ReadWindowData(TempData); // Pipe Stage 2 - Read
WriteWindow(CurrentPos,TempData); // Pipe Stage 3 - Write
...
}
...
}

```

Figure 4 - Example of pipelined loop code for Handel-C for LZ77 sliding window

tion results in terms of the number of clock cycles required to decompress given files.

Table 2 shows the theoretical peak and maximum sustained decompressed data output rate from the GZIP decompression algorithm. The actual data output rate depends on the level of compression – highly compressed files result in a higher rate.

In comparison, software GZIP has a peak data output rate of approximately 25 MBps on an average Pentium III-based system.

### Implementation

The Handel-C GZIP decompression algorithm was synthesized directly to EDIF using the compiler. Xilinx ISE 5.1i tools were used to place-and-route the circuitry and to configure the Xilinx FPGAs on the Tarari CPP. A board-support package (BSP) of function calls is provided in the Tarari Content Processor Development Kit. The BSP provides a layer of abstraction that shields users from “low-level detail” and is used during both simulation and implementation of the design.

The final implementation size was 40% of one Virtex-II 1000 Platform FPGA with speed exceeding the 133 MHz required for maximum DDR data access on the Tarari CPP card.

GZIP Decompression Rate (Mbytes/s)	
Theoretical peak	130
Maximum sustained	116

Table 2 - Performance results for GZIP decompression

Module	Function
1 Main	Detects the type of a compressed data block, and calls the appropriate modules to decompress it. Coordinates operation of all other modules in the application.
2 Optimized block memory access	Provides a simple interface for pipelined access to block RAM on Xilinx FPGAs. Required to achieve high clock rates. Used to provide RAMs for Huffman tables and LZ77 sliding window.
3 Bitstream reader	Reads a variable number of bits from the input bitstream.
4 Builder for tree description Huffman decoder	For dynamic compressed blocks. Uses the tree description generated from the input bitstream to build a Huffman decoder table for the tree descriptions for the main Huffman decoders.
5 Tree description Huffman decoder	For dynamic compressed blocks. Decodes the Huffman codes from the input bitstream, generating tree descriptions for the “literal/length” and “distance” Huffman decoders.
6 Builder for “literal/length” Huffman decoder	Uses the tree description generated from the input bitstream or the static bit-length codes to build a Huffman decoder table for the “literal/length” Huffman decoder.
7 Builder for “distance” Huffman decoder	Uses the tree description generated from the input bitstream or the static bit-length codes to build a Huffman decoder table for the “distance” Huffman decoder.
8 “Literal/length” and “distance” Huffman decoders	Decodes the Huffman codes from the input bitstream, generating “literal” values and “length/distance” pairs.
9 LZ77 decompress	Uses the LZ77 algorithm on the stream of “literal” values and length/distance pairs to reconstruct the original uncompressed data.

Table 1 - Modules and descriptions for Handel-C GZIP decompression algorithm

### Conclusion

Application acceleration is simplified using the combination of the Tarari CPP and the Celoxica DK Design Suite. Together they provide the ability to deliver hardware acceleration products with much lower NRE costs than traditional methods and with a quicker time to market.

The GZIP decompression algorithm was used to demonstrate the platform’s ability to deliver significant acceleration and an overall performance improvement for applications. The Celoxica DK Design Suite allowed interactive simulation and debugging of the GZIP decompression algorithm. Interactive simulation delivers both rapid proof of concept and the completion of development in only two months. The Celoxica DK Design Suite – along with the other design tools, examples, and documentation from Celoxica – enable you to quickly develop and deploy highly accelerated products.

You could continue to optimize performance for a specific algorithm or, more important, incorporate additional algorithms to deliver even higher application performance benefits. Systems deployed at customer sites with Tarari CPPs can take advantage of these enhancements due to the built-in reconfiguration capabilities of the Virtex-II FPGAs, resulting in an overall lower cost of ownership.

To find out more about hardware acceleration using the Tarari Content Processor Development Kit, visit [www.tarari.com/products-cpdk.html](http://www.tarari.com/products-cpdk.html). To discuss how your applications can be accelerated, contact Tarari at [sales@tarari.com](mailto:sales@tarari.com). **Σ**

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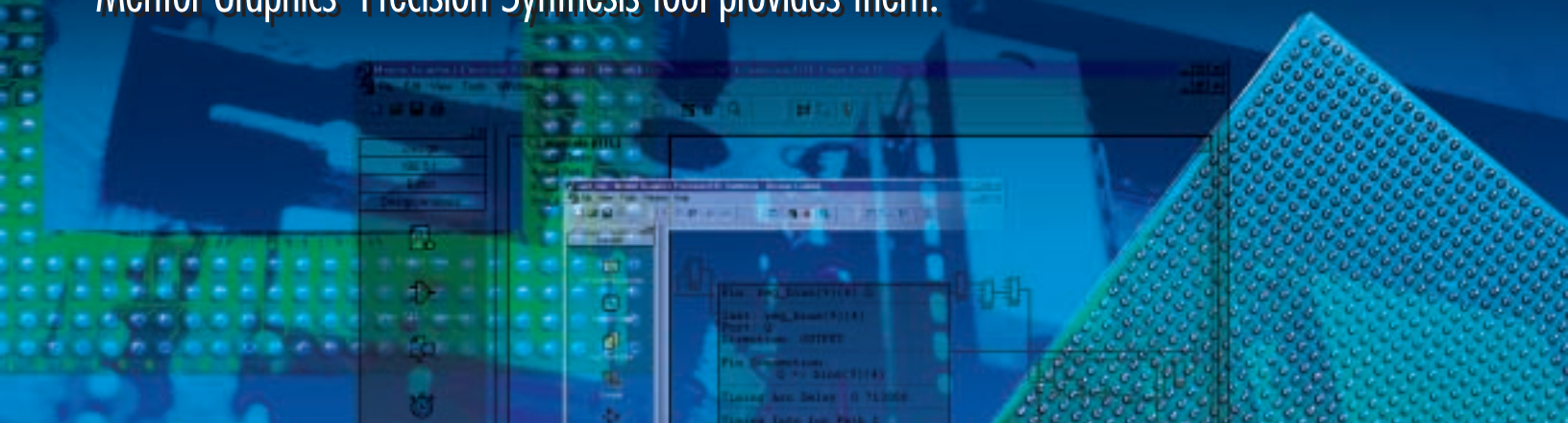


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# Next-Generation FPGA Synthesis Requires ASIC-Level Capabilities

The same breakthroughs that make FPGAs competitive with ASICs also impose design and verification challenges that require advanced methodologies and debug capabilities. Mentor Graphics' Precision Synthesis tool provides them.



by Tom Hill  
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In the fast-moving world of programmable logic, EDA vendors face the persistent challenge of creating design tools and methodologies to keep pace with the increasing complexity and capacity of silicon.

ASICs have historically provided a cost-effective solution for the electronics industry; this technology is responsible for considerable growth and innovation. The popularity of ASIC technology has provided the driving force in the EDA industry and dictated the direction for software development. ASIC development is, however, moving beyond the reach of many mainstream designers due to high upfront (NRE) charges and a longer time-to-market. FPGAs are filling this void and will become the dominant approach for designers and the new driving force in the EDA industry.

## FPGA Growth

FPGA design methodology has many advantages. You control the entire design and layout processes. Design cycle times are faster, photo-mask costs are non-existent, and there are no minimum order restrictions. On the other hand, the low performance, comparatively smaller gate densities, and high unit costs of FPGAs have historically relegated them to small, low-volume designs. ASICs claimed the remainder of the market.

Xilinx is overcoming these market barriers by developing reconfigurable, system-level FPGAs such as the Virtex-II Pro™ Platform FPGA, which integrates embedded microprocessor cores, memory, and hard and soft macros. These features provide you with the benefits of reduced system-development times, improved power consumption, increased volume, and expanded board space, as well as the flexibility to make changes right up to production time. These dramatic technological

breakthroughs, however, add design and verification challenges and require new methodologies and debug capabilities.

For designers to take full advantage of FPGA technology, the supporting software tools must be capable of solving designers' toughest challenges. Mentor Graphics introduced its Precision™ Synthesis platform to solve this new set of problems.

## Precision Synthesis Concepts

Three major considerations drove the development of the Precision Synthesis platform's architecture:

1. Intuitive user interaction
2. Excellent Quality of Results (QoR)
3. Advanced analysis.

## Intuitive Use

When you interact with an EDA product, the tool should add speed and reliability to the development, analysis, and debug of a design. Although the tool must drive the

design process, it must also be capable of adapting to each user's design style. The Precision Synthesis platform was constructed with this in mind. You see only the tasks and data that are relevant to a particular point in the design process. Extraneous data is hidden until needed. Selective visibility allows you to concentrate on the task at hand and provides an intuitive approach to synthesis (Figure 1).

The Precision Synthesis platform also offers push-button synthesis flow without compromising results or flexibility. This ease-of-use feature was achieved by replacing user-configured synthesis options with automated configuration. Optimization algorithms configure options based on an analysis of a design against its constraints, thus eliminating the need to specify effort levels or optimization "goals."

Intuitive use can be enhanced by utilizing industry standards and knowledge whenever possible. We adopted, for example, the Synopsys Design Constraint (SDC) format for defining timing constraints. As many ASIC designs are now completed in FPGAs, the SDC format eases the migration of designs between the two design environments.

### Excellent Quality of Results

The Precision Synthesis tool includes a suite of unique algorithms called Architecture Signature Extraction (ASE) optimization that automatically focuses specific optimizations on those areas of the design that are most likely to hinder overall performance, such as finite state machines (FSM), cross-hierarchical paths, or paths with excessive combinational logic. The ASE technology uses an automated, heuristic approach to deliver smaller and faster designs without iterative manual user intervention.

The Precision Synthesis platform's ASE technology takes full advantage of Xilinx device features by providing the smallest design that meets your target frequency. This saves you time by reducing design iterations, and money by helping you fit into smaller devices or lower speed grades in the process.

### Advanced Analysis

FPGA devices are now being used to implement highly complex designs for a

wide range of applications. The complexity of large systems results from the detailed timing and clocking requirements being designed into these devices. This timing complexity can lead to excessive design iterations or even undetected timing problems affecting printed-circuit-board debug.

To solve these new timing issues and guarantee a reliable design, the Precision Synthesis platform includes a timing engine and design analysis capabilities. Its PreciseTime™ timing engine provides a completely interactive, standalone timing analysis environment designed to handle the most complicated clocking schemes with speed and accuracy. The PreciseTime engine's capabilities extend beyond timing analysis to include:

- Reports of internal clocks, including clock propagation information through simple gates, dividers, and DCMs
- Reports of missing constraints that prevent comprehensive timing analysis
- Reports of timing paths that cross asynchronous clock domains (These reports help you verify clock isolation or the existence of metastable safe synchronization logic.)
- Powerful schematic viewing with schematic-fragment-generation capabilities and multiple critical-path viewing (Figure 2).

First-time success on your printed circuit board requires a fully and accurately constrained design during synthesis; PreciseTime was designed to do just that.

### Next-Generation FPGA Synthesis

The FPGA synthesis domain is rapidly expanding beyond the RTL space to encompass the architectural and physical realms. This expansion will produce significant gains in both designer productivity and chip performance. Designers will require tools with powerful algorithms for

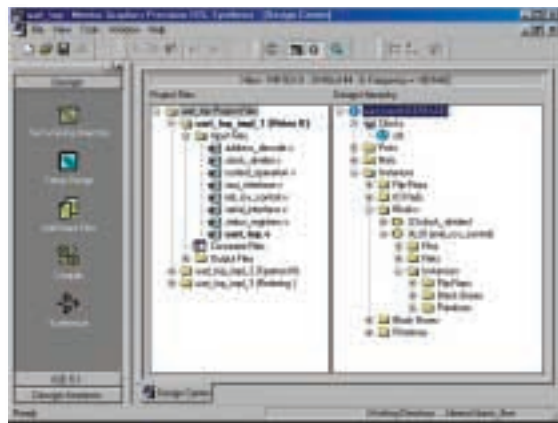


Figure 1 - Precision Synthesis Design Center

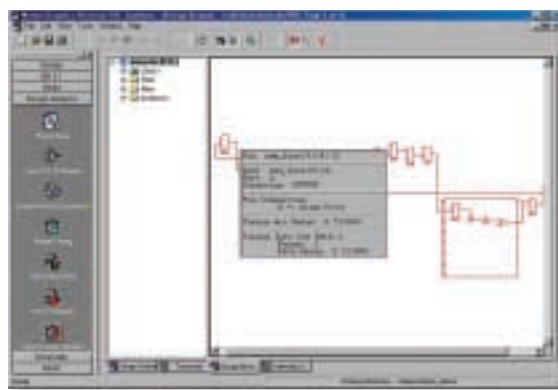


Figure 2 - Critical path schematic

optimization at each level of abstraction. They will benefit from a seamless methodology that allows easy migration throughout each phase of the design.

The Precision Synthesis product designation represents a synthesis technology platform that encompasses a family of synthesis products created by Mentor Graphics to address high-end FPGA design issues from different levels of abstraction.

Built to keep pace with the ever-changing programmable logic world, the Precision Synthesis platform is a choice worth considering for next-generation FPGA implementations. By incorporating an intuitive user interface, excellent QoR, and unparalleled accuracy, it can handle the toughest FPGA designs.

Mentor Graphics is committed to provide you with the latest set of EDA tools to enable electronic design innovation. For more information about the Precision Synthesis platform or Mentor Graphics' complete FPGA-design product family, visit [www.mentor.com/fpgal](http://www.mentor.com/fpgal). ☒

# NSPICE Bridges Simulation Gap

A next-generation, mixed-domain SPICE tool with directly integrated S-parameter data capability provides the most accurate simulation of combined silicon and system behavior.

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Streamlining the simulation of entire complex system environments – from chip, to package, to board, to connector, to backplane, and back again to chip – has become one of the most urgent needs of designers today. The problem becomes even more challenging because the supply chain for multi-gigabit serial I/O connectivity requires tighter integration among many different parties: chip and board designers, system integrators, and backplane and connector suppliers.

Internet applications for data, audio, video, and graphics have spawned a myriad of competing standards to relieve the serial I/O bottleneck, including 10 Gigabit XAUI, InfiniBand™ and PCI Express™.

The only effective way to address the design, simulation, and integration of multi-gigabit serial I/Os on multiport networks is to bridge the circuit simulation gap between chips and systems. NSPICE, a next-generation SPICE (Simulation Program with Integrated Circuit Emphasis) tool developed by Apache, co-simulates nonlinear SPICE models for the transmitter and receiver circuitry. Together with linear scattering parameters (S-parameters) for connectors and backplanes, NSPICE bridges the simulation for chip-to-chip and other complex topologies.

### Limitations of S-Parameter Lumped RLC

At high frequencies, the S-parameter is the most accurate form of broadband frequency representation for such off-chip, passive networks as packages, boards, and backplanes. S-parameters are preferred over other frequency domain parameters (Y and Z, for example) primarily because S-parameters range between the values of 0 and 1, and they are well behaved across a broad frequency range. In addition, S-parameters are the easiest parameters to measure using a vector network analyzer. By matching the signal impedance without reflection and saving the results to a standard file, you can directly access S-parameter data for simulation.

However, most existing SPICE tools still require you to model S-parameter data from backplanes, boards, and transmission lines into lumped RLC (resistance, inductance, and capacitance) “black box” models, or SPICE subcircuits. This timeworn lumped RLC approach is necessitated by the inability of existing time-domain SPICE tools to take in the frequency-domain S-parameter data directly.

There are two main problems with this approach. First, lumped models do not accurately represent distributed frequency-dependent effects, particularly in the high

end of this prolonged process, it is likely that the system will be inaccurate and restricted to a limited frequency range because the poles/zeros will have to be reduced and approximated.

### Benefits of S-Parameter Integrated NSPICE

As shown in Figure 1, integrating S-parameter data directly into a mixed-domain, high-capacity SPICE tool offers a faster and more accurate alternative to lumped approaches. NSPICE is fully compatible with HSPICE (an analog circuit simulator marketed by Synopsys). It per-

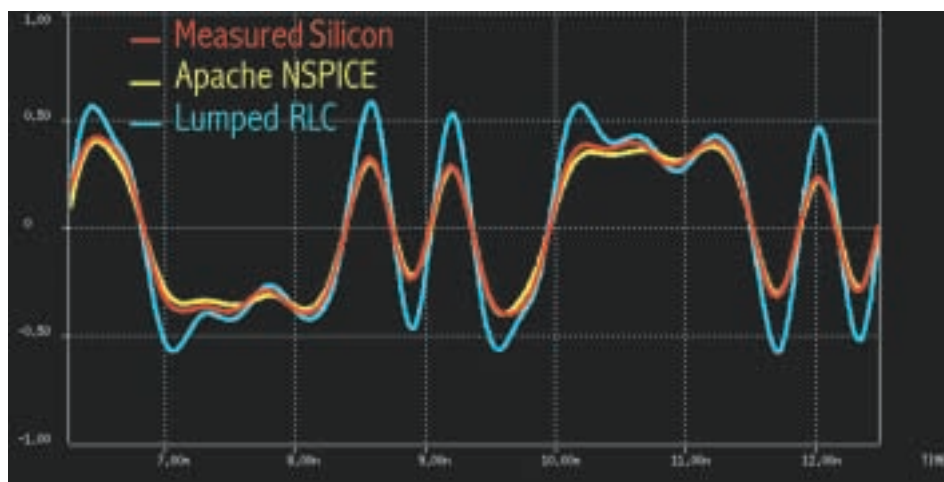


Figure 1 - Comparison of S-parameter lumped RLC approach with S-parameter integrated in NSPICE

frequency range. Second, the model generation process can result in a massive quantity of elements, taxing both you and the SPICE tool.

To illustrate the modeling complexity, let's examine a simple two-port passive linear network that has four S-parameters: reflection at both ports, as well as forward and backward transmission. Correspondingly, a four-port network contains 16 S-parameters. A passive structure such as an FR-4 backplane can possess hundreds of poles/zeros across a broad frequency range. Using the lumped approach, you must generate models by fitting and optimizing each pole/zero combination from S-parameter data. This process can result in hundreds of thousands of elements in large multiport networks. The lumped model development time alone can take up to several weeks, not counting the SPICE simulation time and resulting convergence issues. And at the

forms mixed-domain simulation with direct S-parameter data, generating accurate eye diagram patterns and output waveforms. NSPICE co-simulates the nonlinear SPICE models for the transmitter and receiver circuitry together with linear S-parameters for connectors and backplanes, thereby bridging the simulation for chip-to-chip and other complex topologies.

Figure 2 depicts a typical application: a 3.125 Gbps SERDES system consisting of a transmitter with PLLs (phase locked loops, represented by a SPICE netlist), connectors, backplanes, linecards (represented with S-parameter models), cables (represented with transmission-line models), and a receiver (represented by a SPICE netlist). The entire system requires simulating more than 10,000 devices, on top of hundreds of thousands of RLC parasitics.

As shown in Figure 3, the total turn time using NSPICE, from reading in S-

parameters to generating eye diagrams, is at least 10 times faster than lumped model generation and simulation approaches, which can consume several weeks. For smaller circuits that are less than a few thousand elements, the turn time in NSPICE for an eye diagram can be shrunk down to only a few minutes.

Until recently, some connector, backplane, and board suppliers provided only fitted lumped models to their customers, because that was the only way to simulate the effects in SPICE. Unfortunately,

accuracy has already been lost in the fitting process, so customers are now requesting vendors to provide the S-parameter data directly. NSPICE can simulate the system using whatever models are available for each component, in any combination of lumped models, transmission models, and S-parameters.

NSPICE is written in C++ and employs hierarchical algorithms offering improved performance, memory efficiency, and better convergence using advanced matrix solver technology. The product is fully

compatible with HSPICE and SPICE models and netlists. NSPICE also supports pseudo-random bit stream (PRBS) generation and eye diagrams.

### Working with NSPICE

To illustrate the typical usage of NSPICE, assume that a channel simulation configuration has the following components: encrypted models from the IP vendor for the transmitter and receiver, S-parameter models for the backplane, and lumped models for the connectors and packages from the manufacturer. After constructing a SPICE netlist that represents your channel configuration, you can run transient time-domain simulation on the entire system using NSPICE – without translating the S-parameter models – and generate eye diagrams directly from the simulation results. In addition, NSPICE supports advanced analysis, such as frequency modulation, to simulate the on-chip PLL response together with off-chip resonance effects, thereby enhancing the accuracy of the PLL simulation.

The Xilinx flagship Virtex™-II Platform FPGA demands simulation that accurately correlates the RocketIO™ serial transceiver behavior and performance with actual silicon. By modeling serial backplane, chip-to-chip, and other topologies with direct S-parameter data, NSPICE provides the most accurate simulation of silicon behavior.

### Conclusion

Adapting to the ever-increasing demands of networking bandwidth requires the use of technology that seamlessly bridges the time-domain and frequency-domain aspects of large systems. A true, mixed-domain SPICE, integrated with actual S-parameter data, benefits the entire supply chain for multi-gigabit serial connectivity by providing the most accurate prediction of silicon and system behavior. Predicting behavior accurately ensures significant system cost savings, easier integration, and, most important, accurate and consistent operation across a broadband frequency range.

To learn more about NSPICE, visit [www.apache-da.com](http://www.apache-da.com) or contact [info@apache-da.com](mailto:info@apache-da.com). ❧

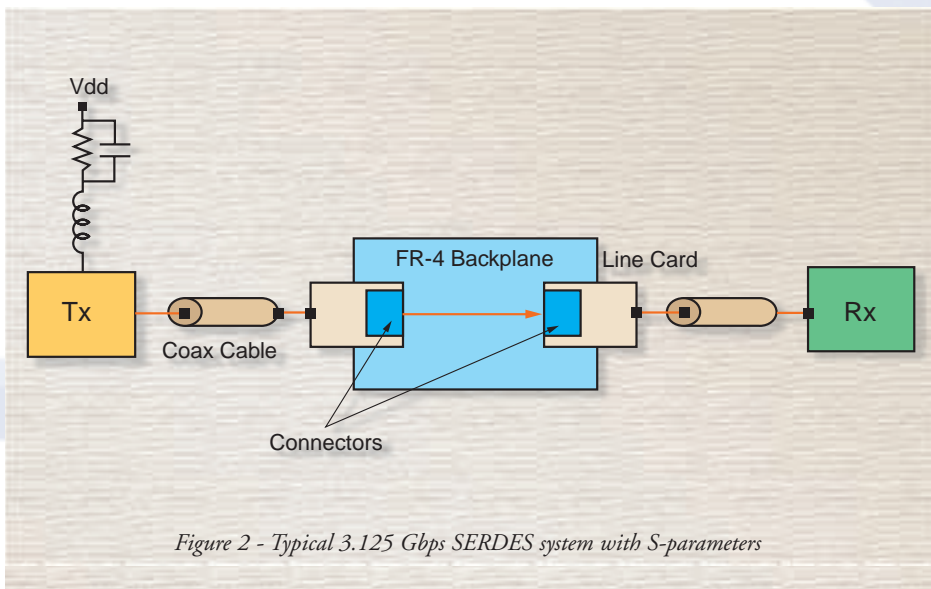


Figure 2 - Typical 3.125 Gbps SERDES system with S-parameters

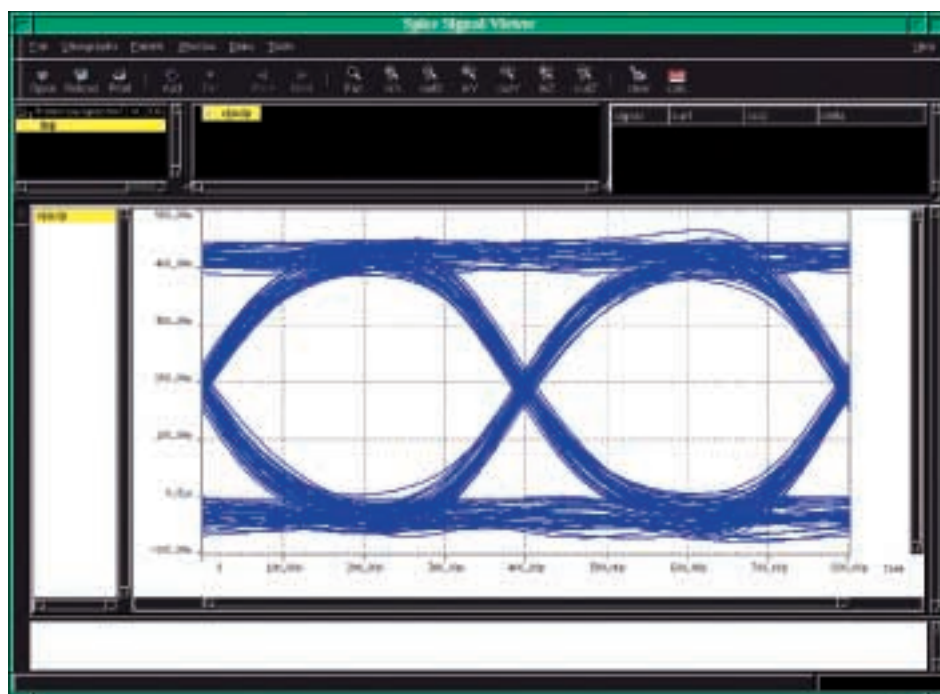


Figure 3 - Turn time using NSPICE, from reading in S-parameters to generating eye diagrams



# Optimize Pin Assignments Early

By minimizing wire crossing and printed circuit board route complexity, DesignF/X pin assignment software reduces routing layers and enables your systems to run faster and come to market sooner.

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According to the International Technology Roadmap for Assembly and Packaging, sponsored by International SEMATECH, the package pin count for high-performance ICs is expected to reach 4,009 by year 2007. With densities of this magnitude, proper pin assignment is essential to maximize the component, board, system performance, and to deliver products on time and on budget. Xilinx's Serial Tsunami Initiative addresses density-related problems from the FPGA component perspective, but you also need the right board-level EDA tools. Most of today's EDA board-level tools focus solely on schematic and layout issues. In doing so, they fail to address many of the complex problems – such as board performance, cost, and schedule slippage – that are created by sub-optimal pin assignment.

In addition to enhancing performance by reducing routing layers, automating pin assignments at the front end of the design process gives you more time for signal integrity analysis, functional simulation, and even system packaging activity. The end result is higher quality products with significant reductions in design time, engineering costs, and product manufacturing costs.

The DesignF/X™ automated design and optimization tool from PAI (Product Acceleration Inc.) helps you analyze and optimize the component pin assignments very early in the product development cycle – during concept development, device selection, early component architecture and placement, and early FPGA device floorplanning. The DesignF/X tool helps shorten development time and time-to-market, improves the performance of the finished product, and reduces the costs of development and of the finished product as well.

### DesignF/X Benefits

The DesignF/X tool suite enhances product feasibility, reduces engineering time and costs, and improves operational metrics.

### Product Feasibility

Often, high-density PCB routing challenges are solved through thinner traces combined with extremely small, blind, or buried vias and increased PCB layers. These solutions, however, can result in significantly degraded system performance and forced operation at lower system clock speeds. In some cases, the degradation is so bad it results in the loss of market relevance for a product.

With the DesignF/X tools, these issues are avoided through earlier, smarter, and faster analysis and optimization of pin assignments on critical system components. In turn, this enables fundamental product viability and increases the odds of market success.

### Engineering Costs and Timelines

Engineering costs are driven by individual task lengths, inter-task relationships,

## DESIGNF/X VALUE CALCULATOR

### Example - Board Design Using FPGA

	Current	With DF/X	Fully loaded labor rate	Benefits	
	Time required	Time required		Time savings	Cost savings
	Worker weeks	Worker weeks	\$/ hour	Worker weeks	Dollars
<b>Product Design</b>					
Architecture & delivery	6.0	5.0	\$ 80.0	1.0	\$ 3,200
Simulation closure	6.0	4.0	\$ 80.0	2.0	\$ 6,400
FPGA design flow iterations	3.0	0.0	\$ 80.0	3.0	\$ 9,600
<b>PCB Layout</b>					
Component placement	2.0	0.4	\$ 80.0	1.6	\$ 5,120
Optimization setup	0.0	0.2	\$ 80.0	(0.2)	\$ (640)
Board layout	8.0	7.0	\$ 80.0	1.0	\$ 3,200
<b>Totals</b>	<b>25.0</b>	<b>16.6</b>		<b>8.4</b>	<b>\$ 26,880</b>

Key Metrics	
Avg designs per engineer per yr =	3.0
Dollar savings per design =	\$ 26,880
Total savings per month =	\$ 6,720
Total savings per year =	\$ 80,640
Margin improvement per design =	33.7%
Time improvement per design =	33.6%

Figure 1 - Analysis of cost saving using DesignF/X tool suite

and labor costs. The use of FPGAs clearly implies a desire to control engineering costs. However, traditional approaches require the FPGA designer to interact with and wait for task completion by a systems hardware designer and a PCB layout engineer. Only then can the FPGA designer analyze and optimize pin assignments, using a manual and iterative process. These delays and iterations affect the direct cost of the activities, creating unnecessary task dependencies, forcing extensive change management overhead, and impacting the overall project momentum.

The DesignF/X tool suite employs intelligent algorithms to create an accurate impact analysis and optimize pin assignment early, before you spend time creating symbols, schematics, and developing the PCB layout. Consequently, the FPGA designer handles board-level issues regarding pin assignment directly, without the task and process delay imposed by traditional processes. The result is an immediate improvement in project engineering costs and timelines.

### Operational Metrics

Apart from the costs of R&D, other key operational metrics that determine product success are the cost of production and time-to-market.

The choice of an FPGA-based design approach implies that time-to-market is a key operational metric for the success of your project. However, poor pin assignment can result in PCBs that are more expensive to manufacture, with up to a 10% cost increase with each additional board layer. In addition, increased PCB layer counts may result in longer order cycles and a narrow supply base. This becomes extremely important when layer counts rise above 24, and critical at more than 40 layers, at which point the PCB itself represents a significant portion of the overall system cost.

By avoiding increased order cycles and extended development cycles, DesignF/X tools help you gain significant time-to-market advantages. By helping to reduce the complexity of the PCB and its layer count, the DesignF/X software lets you

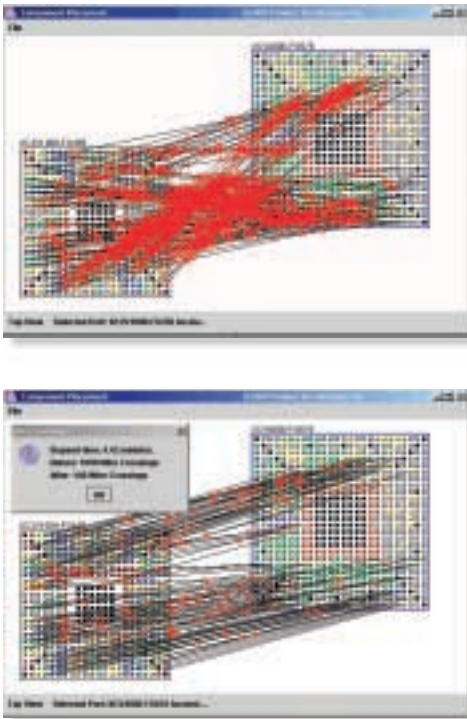


Figure 2 - Before and after DesignF/X wire-crossing reduction

reduce recurring product costs, improve order cycles, and expand the pool of available suppliers.

Figure 1 compares the cost of designing a product with – and without – the DesignF/X package. In this example, the DesignF/X tool suite enables an organization to reduce costs by nearly \$27,000 per design and shorten product design cycle time from 25 weeks to just over 16 weeks. This reflects a greater than 33% improvement in margin per design and a savings of more than eight worker-weeks. By using DesignF/X tools early in the design process, you can help avoid costly iterations due to improper pin assignments and reduce the time of your FPGA design flow iterations to nearly zero.

### Design Flow Using DesignF/X

Begin by importing your component information or creating it rapidly from your datasheet or ASCII pin file. You then specify the connectivity between the target FPGA and other major components, as well as their approximate placement. This process includes a definition of pin/signal mobility and basic constraint information.

The DesignF/X software then performs

a “situation analysis” based on various combinations of component connectivity and placement, resulting in optimized pin assignments. The optimization is performed in terms of the board itself and of the system as a whole, with special attention paid to detecting and reducing wire crossing. Figure 2 illustrates the effectiveness of DesignF/X detection and reduction of wire crossing.

Once you are satisfied with the results, you can create output files consisting of optimized component pin assignments and related reports. These individual component pin assignments can then be used as pin assignment constraints for the internal design of those components.

Original pin assignments can be written in the Xilinx PAD file format. The DesignF/X program outputs the optimized pin assignments in the corresponding format, enabling DesignF/X software to fit seamlessly into your FPGA design flow with minimal disruption to existing processes.

Future releases of the DesignF/X tool suite will support bidirectional data exchange with Xilinx PACE software to create pin and area constraints. In this

case, an NGD file is used as input to PACE. Any additional FPGA pin and area constraints can then be developed using PACE and saved for use in the Xilinx place-and-route flow.

Figure 3 illustrates how DesignF/X-generated pin assignment constraints can be used easily in an FPGA design flow.

### Conclusion

Unlike other EDA board-level design tools – which focus on schematic and layout issues – the DesignF/X suite from PAI provides you with what you need to reduce design time and costs through pre-layout pin optimization. With an intuitive user interface, Java-based design, powerful algorithms, and accurate analysis capabilities, DesignF/X software enhances the quality, performance, and cycle-time parameters of board design projects. The PAI product suite is designed to coexist within existing methodologies – protecting your investment in tools, skills, and processes. For more information about DesignF/X and PAI’s software solutions, visit [www.prodacc.com](http://www.prodacc.com) or email [sales@prodacc.com](mailto:sales@prodacc.com). ❧

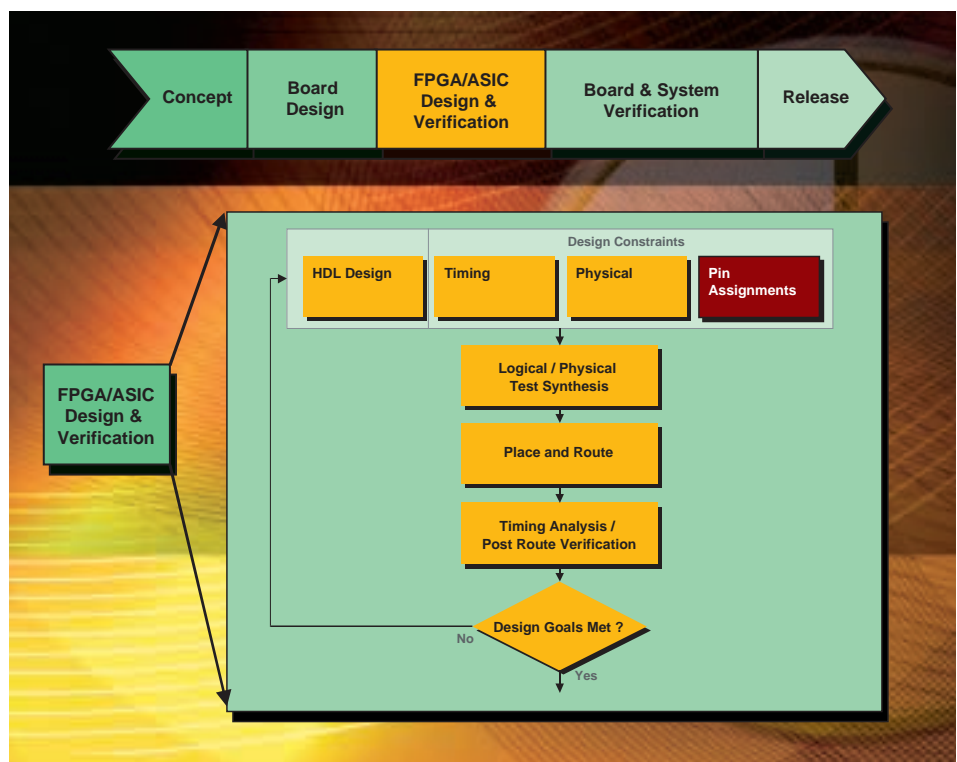


Figure 3 - Typical board/system design flow

# Got the BGA Blues?

Learn how to obtain visibility into the pins of a ball grid array package using Boundary Scan and the Universal Scan debugging tool.



by Rick Folea  
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 Rcreations, Inc.  
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The first prototype of a board populated with BGAs returns from assembly. You attach the Xilinx download cable, apply power, attempt to download test data, and you get – nothing. Debugging is easy when you have access to signal pins – but this board has BGAs, so you can't probe the pins effectively. You wish you could:

- Monitor how mode-select pins are set
- Check continuity across BGA solder connections
- See if the oscillator is connected to the part
- Check the [DIN/DONE/CCLK](#) line continuity
- See if the data/address or other signals are active or connected to the part.

It would be wonderful if you could peel the chip open. But you can't. There are, however, more sophisticated ways to access BGA pins. This article introduces Universal Scan™ – a new tool that takes advantage of IEEE 1149.1 Boundary Scan, commonly known as JTAG, a feature already built into every Xilinx device. It provides visibility and control over the pins under that BGA – or any JTAG device – quickly, easily, and inexpensively.

### JTAG Background – The Basics

You are probably already familiar with the JTAG interface – TCK, TDI, TDO, and TMS – and how JTAG is used to configure Xilinx devices. You may not be as familiar with Boundary Scan, another powerful test technology.

### Boundary Scan Overview

Understanding and using Boundary Scan requires only three basic pieces of information:

- **How the scan chain is connected** – Where does Boundary Scan reside inside your Xilinx device?
- **How the scan cells are connected** – How does Boundary Scan interface with your signals?

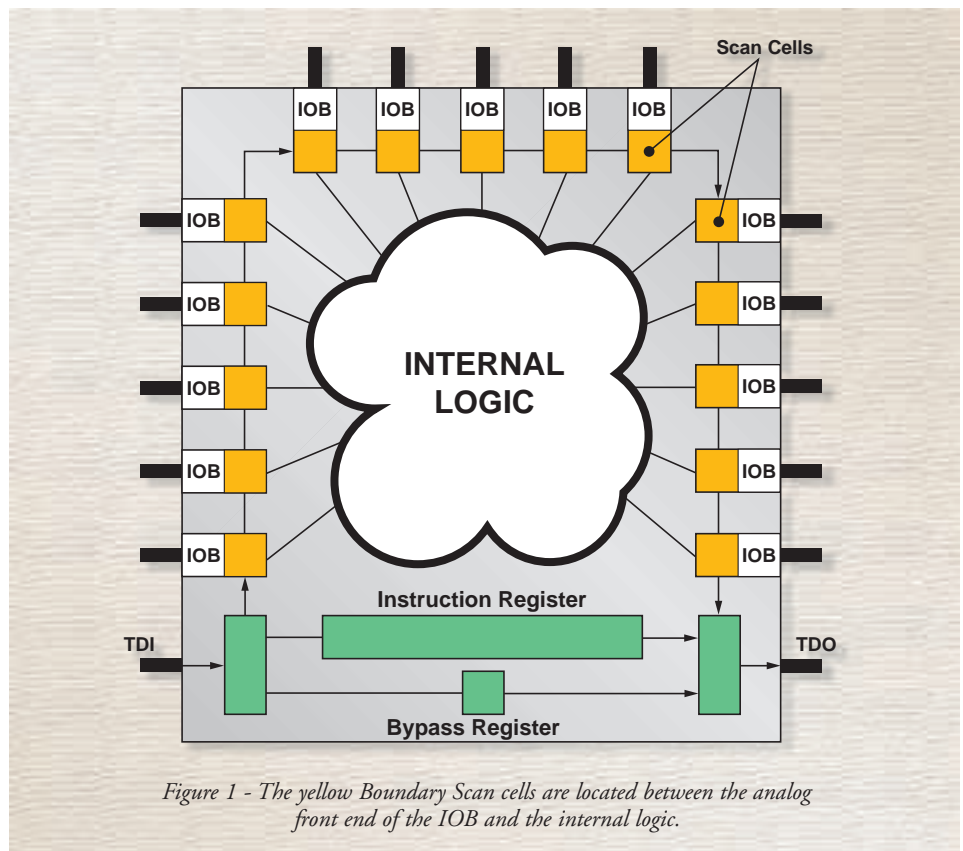


Figure 1 - The yellow Boundary Scan cells are located between the analog front end of the IOB and the internal logic.

- **Boundary Scan operational modes** – What are they and how do they affect the scan cells and the information you can access?

### The Scan Chain

At the most fundamental level, Boundary Scan is illustrated in Figure 1. Logic occupies the interior of the device. Pins occupy the perimeter, or boundary. The interconnects between each pin and the internal logic pass through the Boundary Scan logic blocks (yellow in Figure 1). Boundary Scan blocks are on the logic side of the IOB (input/output block). They are normally transparent to the operation of the device; signals flow unimpeded through them.

Each of these blocks is connected around the boundary of the part to form a giant shift register (the boundary register). When in Boundary Scan mode, TDI is connected to one end of the shift register, and TDO is connected to the other end. TCK and TMS are used to shift data in and out of this giant shift register.

TDI and TDO can be connected to numerous registers (such as those used to

configure the part). Two of the registers are shown in Figure 1: the instruction register and the bypass register.

To use Boundary Scan, you simply shift an instruction into the instruction register and then shift data in/out of the associated data register.

The bypass register is used to skip over a part in a scan chain. Skipping parts of the scan chain allows you to bypass the boundary register and exit in a single TCK cycle.

Scan logic in each of the scan cells consists of a group of registers that captures the state of signals entering and exiting the device, and a group of registers that can drive these same signals. The operation of these cells depends on the Boundary Scan mode.

Manufacturers may define many Boundary Scan modes for a given device, but only the three required by the IEEE 1149.1 standard are necessary for successful debugging. These modes are: **SAMPLE/PRELOAD**, **EXTEST**, and **BYPASS**.

### SAMPLE PRELOAD

In the **SAMPLE/PRELOAD** mode of Boundary Scan, the logic inside the yellow

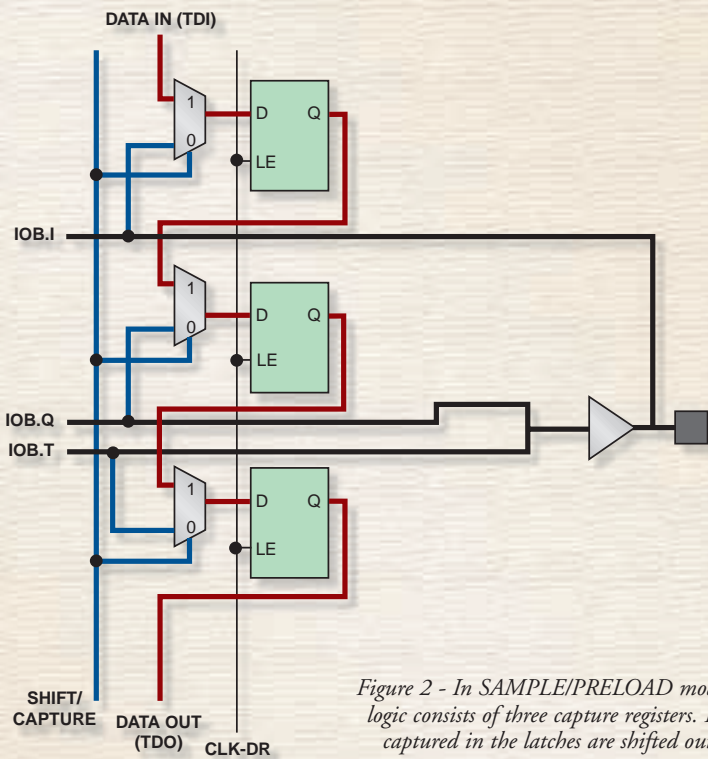


Figure 2 - In SAMPLE/PRELOAD mode, the scan logic consists of three capture registers. I/O signals captured in the latches are shifted out serially.

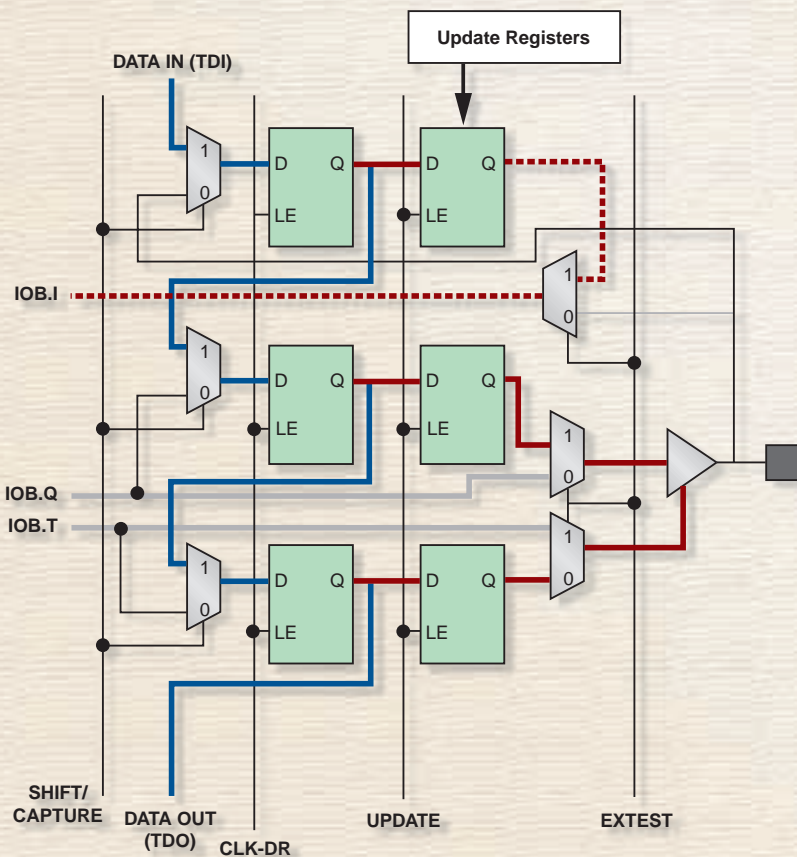


Figure 3 - In EXTEST mode, normal signal flow is interrupted and data that had been shifted into the update registers by the test engineer is applied to the signals.

blocks of Figure 1 is represented in greater detail in Figure 2.

One capture register is dedicated to each signal typically associated with an I/O buffer (INPUT, OUTPUT, TRISTATE). On a command set by the test engineer, these registers, or scan cells, capture the state of all three signals (or however many there are for the pin). Once data is captured, it is shifted out (the red path in Figure 3), and the state of the pin is displayed. Data can be captured at any time. It is asynchronous with signals flowing in and out of the device. The capture process does not interfere with the circuit's operation.

### EXTEST

When a part is in EXTEST mode, data that the test engineer wants to apply to the OUTPUT, TRISTATE – and in some cases, INPUT – signals is shifted into the scan chain. Although the capture registers from SAMPLE/PRELOAD still capture the states of the signals flowing through the device, they never go anywhere. The signals are cut off from their normal function and the data shifted into the update registers is applied to the signals, as shown in Figure 3. Captured data is shifted out as update data is shifted in.

### BYPASS

We have already touched on BYPASS. In this mode, the Boundary Scan chain is bypassed and all TDI data flows through the part in one TCK cycle.

### Applying Boundary Scan to Access Pins

Using the JTAG state machine to implement Boundary Scan can be tedious. But the new Universal Scan debug tool from Ricerations Inc. automates much of the work. You simply drop virtual parts on the screen, connect the JTAG signals to the parallel port, and hit the SCAN button. Instantly, the activity of every pin under the BGA (or around any JTAG part) appears on your PC display.

Each of the red or black dots in Figure 4 represents a pin. Red represents a logic High; black a logic Low. Blue is a pin that can't be scanned (power, ground, and such).

If a pin is toggling, that means there is signal activity on that pin. Typically, this is all we want to know when we use an oscilloscope to debug – whether the pin is high, low, or toggling. The Universal Scan tool is an activity indicator. You instantly see – in real time – if the mode select pins are set correctly, if the oscillator is connected, if the data bus or address bus is active, and so on.

Universal Scan software does not require netlists, test executives, test fixtures, or other board-test peripherals. You don't have to maintain a parts library, because the Universal Scan program doesn't need it. You simply supply the BSDL files, which are freely available from vendor websites, and the Universal Scan tool builds a virtual part on the fly. All that is required is a JTAG-enabled part; packaging doesn't matter.

A valuable aspect of Boundary Scan testing is that, while in **SAMPLE/PRELOAD** mode, you can monitor all the pins while your circuit is running at full speed without any impact on the system. **SAMPLE/PRELOAD** mode is completely transparent to the system. How often have you touched an oscilloscope probe to a pin only to create probe loading that changes the circuit's operation, especially with new high-speed circuits? Boundary Scan does not have that problem – it is completely unobtrusive.

Because watching pins blink on the screen can be tedious, the Universal Scan screen display offers virtual indicators (LEDs) that you connect to the pins to organize those aspects of the circuit's activity that interest you. It also has virtual switches that allow you to manually drive a pin to a known state.

To perform a continuity test between two devices, put one device into **EXTEST** mode and toggle the virtual switches connected to the output buffers. The LEDs connected to the other device's input buffers will show the result. Performing a continuity test this way is quick, easy, and does not require touching the board.

To monitor results on an oscilloscope,

you can drive signals from the BGA to a connector. This gives total visibility and control over every scan-enabled pin on the part. You are only limited by your imagination.

Because Boundary Scan is independent of internal activity, the part does not have to be configured for this testing. You can take the board right off the factory floor and start testing it before the VHDL/Verilog/firmware is ready.

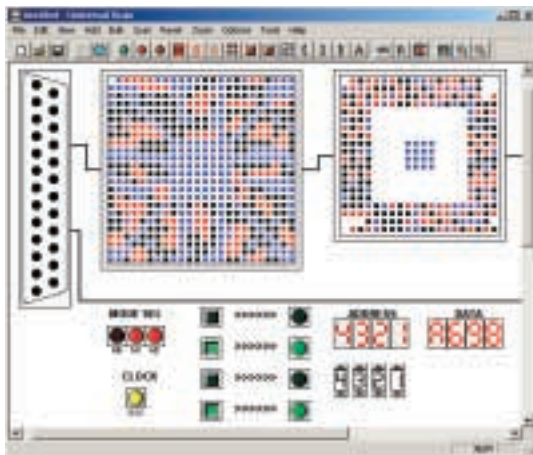


Figure 4 - Virtual switches and LEDs help organize and control the pin information.


### Conclusion

Using Boundary Scans to probe otherwise inaccessible pins under a BGA is an easy, three-step process with the Universal Scan tool:

1. Drag and drop the parts under test on the PC screen.
2. Connect the JTAG chain to the parallel port.
3. Hit the Scan button.

Instantly you can monitor the activity of every JTAG-enabled BGA pin (or around any scan-enabled device) on your PC display.

You don't need test fixtures, netlists, or test executives. The devices don't have to be configured. You can start testing the board right off the factory floor before the firmware is complete.

You'll find information on the Universal Scan toolset on the [www.xilinx.com](http://www.xilinx.com) website by following this click chain: *Products/System Resources/Configuration Solutions/Third-Party Tools/Universal Scan*. Or you can go directly to [www.UniversalScan.com](http://www.UniversalScan.com). 

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# Reduce Resistor Counts and Lower Costs

The background of the page features a close-up, slightly blurred photograph of two resistors on a printed circuit board. The resistors are cylindrical with orange and black color bands. They are connected to thin copper traces on the board. The lighting is dramatic, with a strong blue and cyan color cast, creating a sense of depth and focus on the components.

Second-generation XCITE technology provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os for Virtex-II Pro Platform FPGAs.

by Rob Schreck  
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Today's high-performance chips with fast signal rates require termination to prevent signal reflections and to maintain signal integrity. Historically, engineers have used external termination resistors. However, with advanced packaging technologies and availability of hundreds of I/Os, external termination resistors are no longer viable, especially for ball grid array packages.

To solve this problem, Xilinx pioneered adaptive on-chip termination with XCITE (Xilinx Controlled Impedance Technology) in Virtex™-II Platform FPGAs. XCITE dynamically eliminates drive strength variation due to process, temperature, and voltage fluctuations. XCITE uses two external high-precision resistors per I/O bank to incorporate equivalent input and output impedance internally for hundreds of I/O pins. Not only is the cost of the resistors saved (and the additional manufacturing costs that accrue with them), but with fewer printed circuit board respins the cost of developing PC boards also decreases, as illustrated in Figure 1.





Figure 1 - Reduced component count with XCITE

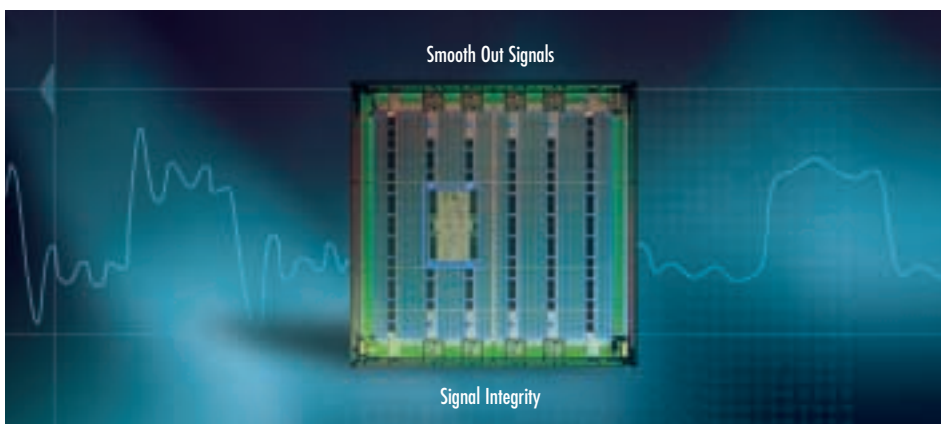


Figure 2 - Increased signal integrity with XCITE

### Increase Signal Integrity

With XCITE, you can eliminate hundreds of external resistors and increase the signal integrity of your boards for single-ended connectivity solutions such as low-voltage complementary metal-oxide semiconductors (LVCMOS). With higher performance I/O becoming more pervasive, you need this capability not only in single-ended connectivity, but in differential signals as well.

Now, Xilinx offers second-generation XCITE technology in the Virtex-II Pro™ Platform FPGA family, extending to popular connectivity standards like low-voltage differential signaling (LVDS), as shown in Figure 2.

### Second Generation XCITE technology


Second-generation XCITE for Virtex-II Pro FPGAs provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os.

XCITE can be used on any I/O block in any bank, thus offering absolute flexi-

bility and independent operability on each I/O bank. When applied to inputs, XCITE provides controlled impedance input parallel termination.

When applied to outputs, XCITE provides controlled impedance series as well as parallel termination. Each of the eight Virtex-II Pro I/O banks supports XCITE, controlled by just two external reference resistors per bank.

### Conclusion

As shown in Table 1, Virtex-II Pro Platform FPGAs offer second-generation XCITE technology that gives you increased signal integrity for both single-ended and differential signaling. Using XCITE technology allows you to dramatically reduce the number of resistors to lower your component costs. The increased signal integrity of each Virtex-II Pro Platform FPGA design reduces the risk of board re-design, delivering even more cost reduction. Simplify your designs and lower your costs with Virtex-II Pro FPGAs with XCITE. For more information, go to [www.xilinx.com/xcite](http://www.xilinx.com/xcite). 

Second-Generation Technology	Proved in the field and used extensively by customers means you can rest assured about its functionality – another Xilinx innovation for lowering risk, improving design efficiency, and maximizing performance.
Lower Costs	By using XCITE, you need fewer resistors, fewer PCB traces, and less board real estate – all resulting in lower PCB costs.
Absolute I/O Flexibility	Use any termination on any I/O bank. Non-XCITE technology alternatives deliver limited functionality with compromising banking restrictions. XCITE input buffers support full and half impedance.
Support for Popular Standards	Wide support for many I/O standards, including LVDS, LVDS6T, LVCMOS, LVTTL, SSTL, HSTL, GTL, and GTLP.
Maximum I/O Bandwidth	With less ringing and reflections, you can maximize your I/O bandwidth.
Immune to Temperature and Voltage Changes	Temperature and voltage variations lead to significant impedance mismatches. XCITE provides complete immunity by dynamically adjusting on-chip termination with digitally controlled impedance at all temperatures and voltages.
Eliminates Stub Reflection	XCITE technology improves discrete termination techniques by eliminating the distance between the package pin and resistor.
Increased System Reliability	With fewer components on board, XCITE delivers higher reliability.

Table 1 - XCITE benefits for Virtex-II Pro Platform FPGAs

# Get the EasyPath Solution

The Virtex-II and the Virtex-II Pro EasyPath solutions are a cost-effective alternative to ASIC conversion — saving you money while significantly decreasing your time to market.

by Frank Toth  
Marketing Manager, Advanced Products  
Xilinx, Inc.  
[frank.toth@xilinx.com](mailto:frank.toth@xilinx.com)

Once a working prototype is developed, designers using high-density FPGAs need a risk-free method of reducing the cost of components used in their end-market products and systems. The traditional ASIC approach is expensive and error prone. The designer typically relies on an ASIC conversion methodology provided by either the FPGA or the ASIC supplier. These methods are supported by a wide range of claims for conversion accuracy and performance. Typically, 30 to 40 weeks is required to accomplish such a conversion for mass production.

Xilinx attacks this problem head-on with our introduction of the Virtex-II EasyPath™ series solutions, including a Virtex-II Pro™ version, as the newest member of the Virtex™-II family of Platform FPGAs. The EasyPath solution slashes the conversion time to 10 to 12 weeks (Figure 1), and delivers a 30% to 80% cost reduction without risk and without additional investment of engineering time or other resources.

#### **Traditional Conversion: Trial and Error**

Conventional conversions require direct time and expense for the services of the ASIC manufacturer for fabrication masks and test programs, and for the engineer-

ing cost of verification and simulation. When the completed system is transferred into production, further system engineering time and expense are needed to requalify the final production system with this new ASIC.

As systems become faster, timing and clocking budgets are tighter, and any slight change in critical paths brought about by ASIC conversion can cause timing mismatches and race conditions. All of these factors introduce substantial risk of delay and escalating cost.

### Risk-Free, Quick, and Easy

The Virtex-II and Virtex-II Pro EasyPath FPGAs emerge from the conversion process ready for full production without any need for a requalification or proof of performance that would normally be required of new ASIC silicon. EasyPath silicon is identical to the FPGA prototype, with the logic and routing resources used by the customer design completely tested for functionality and performance at speed.

### Streamlined Process

Once the design is settled and the qualification completed, you can simply submit four design files (Figure 2), which are standard outputs from any Virtex-II and Virtex-II Pro design.

The EasyPath product is tested for performance and functionality using the same techniques as those applied to the prototype FPGA. Designers order the same speed grade, package, and density as they did for the original FPGA. Typical lead times for production quantities range in weeks rather than months – from the engineering confirmation of the design submittal to full production silicon (thousands of units).

There is no need for the customary first article testing and no risk of the delays that result from multiple spins of ASIC silicon.

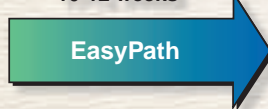
### Test Coverage

The manufacturing test of EasyPath silicon is based on a foundation of proven FPGA test techniques that assure complete testing of the customer design.

Typical ASIC testing relies on the completeness of vectors generated by the cus-

### EasyPath Conversion

10-12 weeks



### Custom ASIC Conversion

30-40 weeks

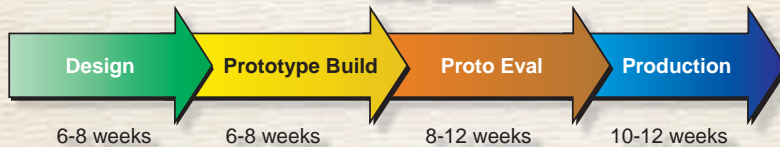


Figure 1 - EasyPath conversion time compared to custom ASIC conversion.

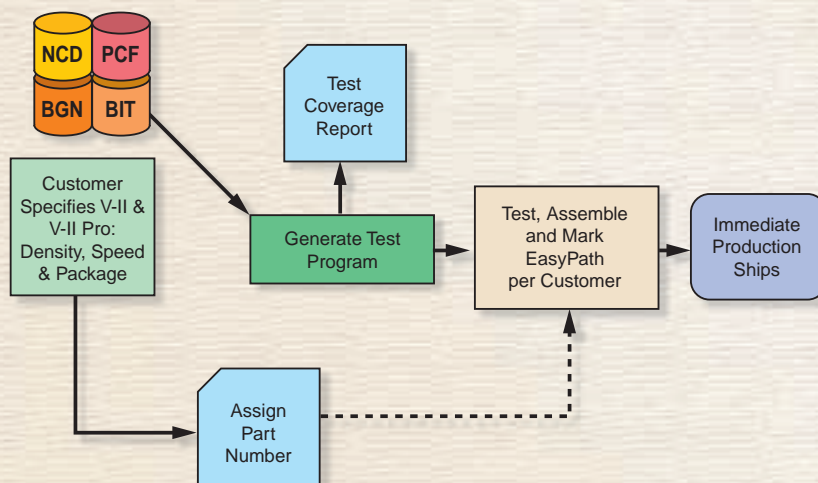


Figure 2 - EasyPath flow

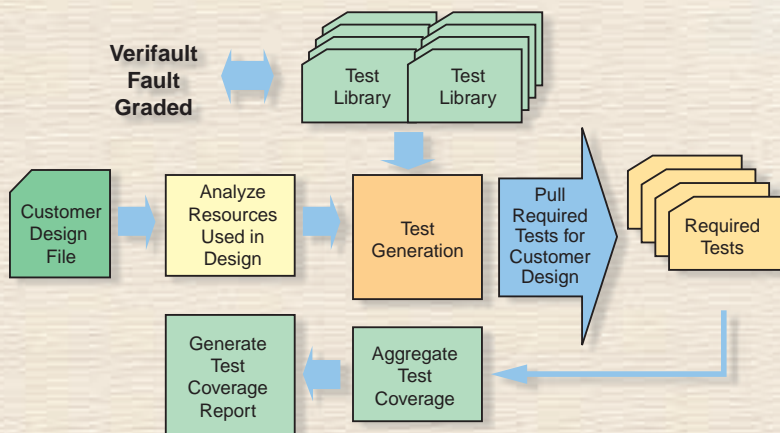


Figure 3 - EasyPath test program

tomor or the ASIC supplier. The ASIC supplier works in conjunction with the designer to cover all the possible test cases with vectors to assure correct operation.

In contrast to this approach, EasyPath testing is based on instrumenting and testing all of the resources used by the cus-

tomor design, as well as testing critical structures at speed. Using multiple bit-stream loads, each resource is instrumented using a library of Verifault™ verified test designs (Figure 3).

The resources used in the EasyPath design are matched against this proven test

library, with each routing resource tested using “source” and “load” techniques (Figure 4). The “source” provides the stimulus, and the “load” evaluates the response.

The EasyPath solution takes advantage of some of the unique architectural features of the Virtex-II and Virtex-II Pro FPGAs.

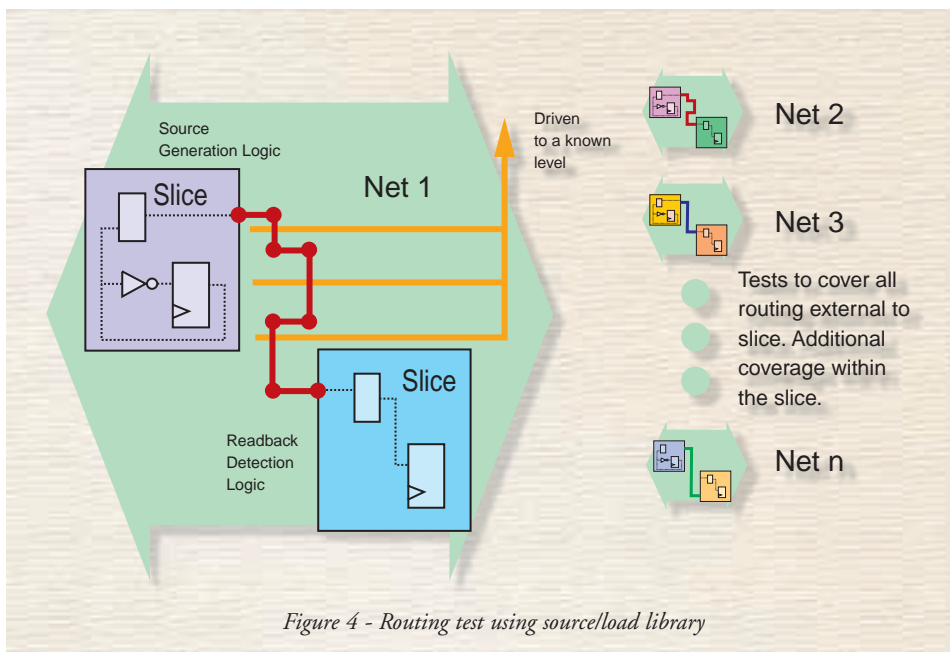


Figure 4 - Routing test using source/load library

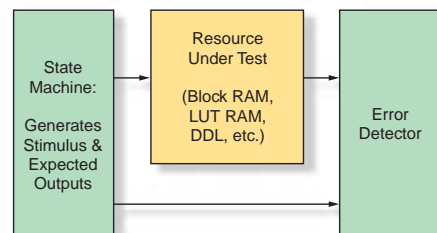


Figure 5 - FPGA testing using self tests

When testing routing, for example, you can allow unused routing resources to be tied to a known state to test for shorts.

As for complicated circuitry such as block RAMs and multipliers, we use multiple bit-streams to instantiate built-in self-test (BIST) structures (Figure 5) designed to thoroughly test these complex circuits.

Error detectors (Figure 6) check for the correct operation of each circuit. Critical resources within the device are speed tested using standard FPGA techniques to guarantee the device operates at the desired speed grade.

### Conclusion

The Virtex-II and Virtex-II Pro EasyPath solutions eliminate your risk, and give you complete control over the expense of converting to a lower cost solution for advanced systems. Now you can reduce total system cost without the need for additional engineering resources. You won't have to requalify the system for new silicon, or worry about the cost and delay of ASIC silicon respins. You can confidently predict the crossover point for realizing the cost savings of the conversion.

In light of current market pressures and tight inventory management, a conventional ASIC will not always be the optimum cost reduction solution. The Xilinx Virtex-II Pro EasyPath solution provides you with a risk-free, rapid, and easily implemented cost reduction alternative. Check it out at [www.xilinx.com/easypath/](http://www.xilinx.com/easypath/).

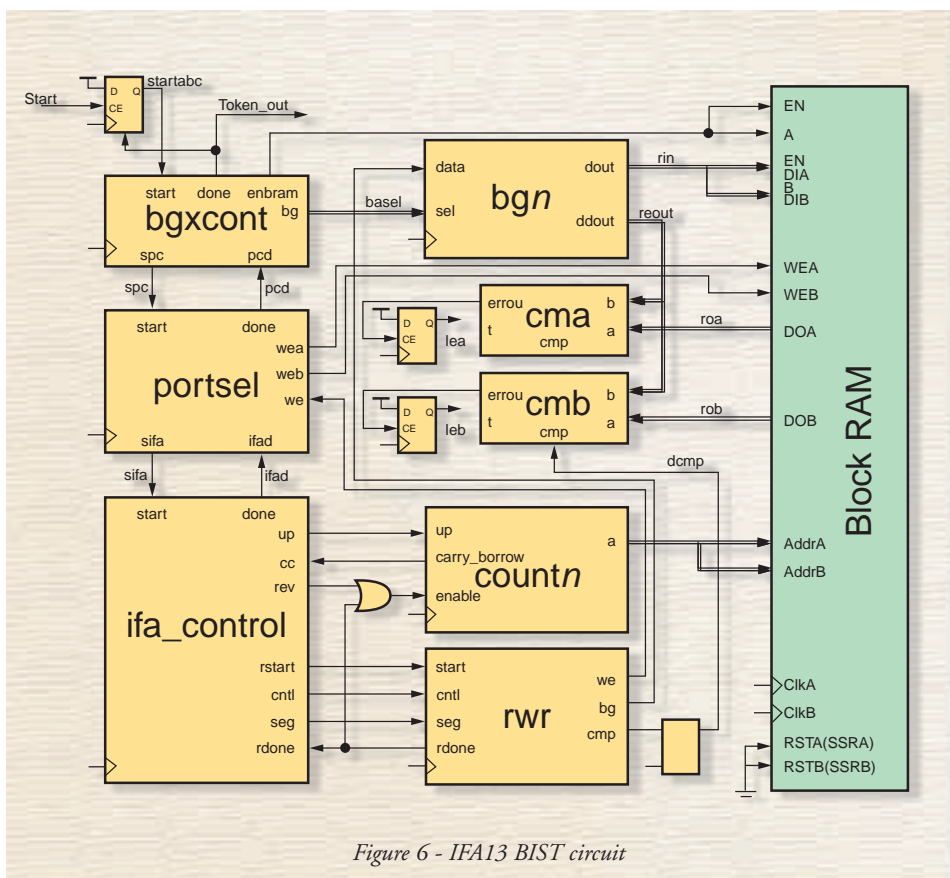
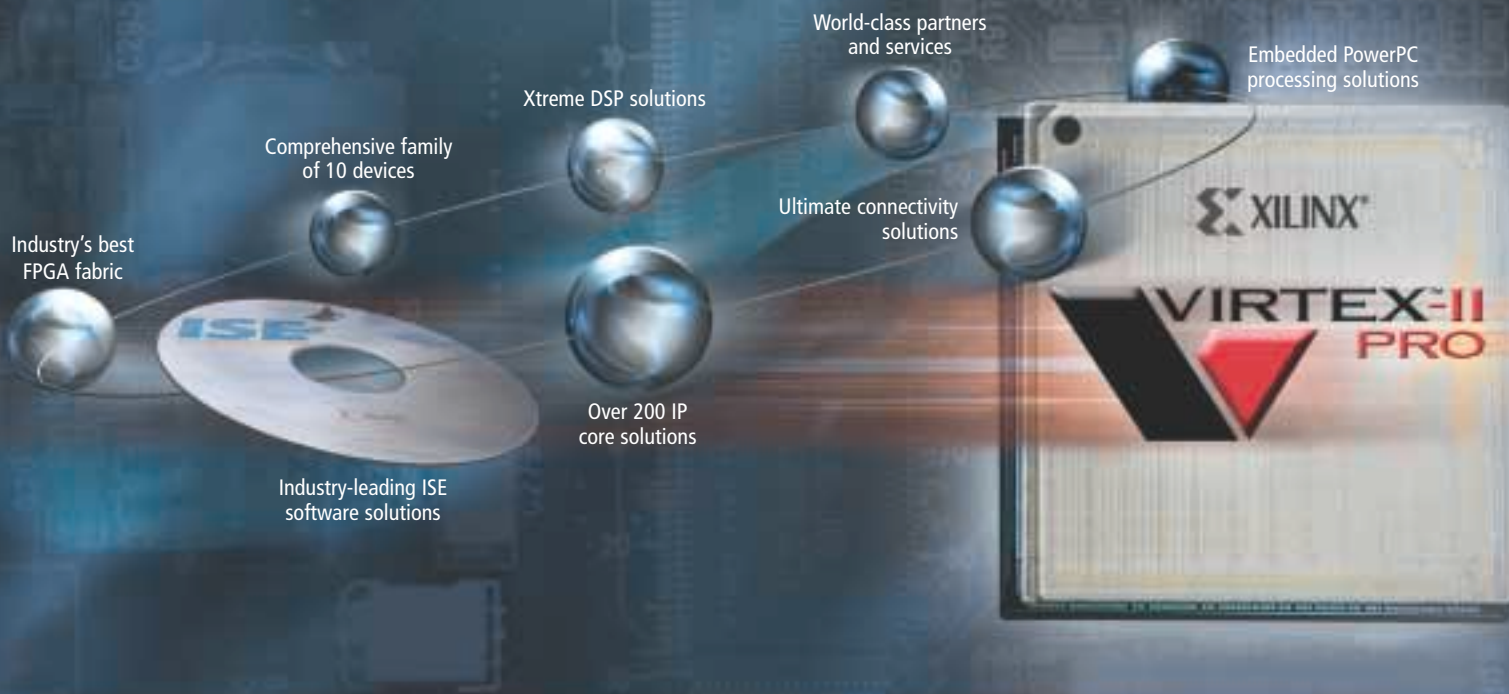


Figure 6 - IFA13 BIST circuit

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# Xilinx Chips Fight Drunk Driving

Low-cost high-performance Xilinx technology powers development of inexpensive alcohol breath testers for drivers and law enforcement.

by Xcell Staff

Late last year, Canadian-based Alcohol Countermeasure System (ACS) introduced the Elan™ personal breath tester, which measures an individual's blood alcohol concentration. Developed in collaboration with Xilinx, the Elan tester demonstrates the creative potential for new mass market products that exploit low-cost, low power-consuming FPGAs.

The Elan tester analyzes and displays blood alcohol (%BAC) test results on a 3-digit LCD display within 10 seconds, yet it's not much bigger than a cigarette lighter and costs just \$49 USD.

## Stopping Repeat Offenders

ACS and Xilinx have also developed a high-end, voice-recognition alcohol breath tester that will help law enforcement manage repeat offenders. Available today in beta form, the ACS WR3 ignition interlock device locks the auto ignition until the driver passes a sobriety analysis by breathing and humming into the mouthpiece.

What makes this new technology unique is the voice recognition feature – enabled by Xilinx chips – which makes it impossible for the offender to cheat and activate the vehicle with the breath of another individual.



Figure 1 - The Elan alcohol breath tester from ACS.

## Xilinx FPGAs Key Component

“Xilinx low-cost programmable chips provided the technology we required to produce the most advanced alcohol breath testers on the market today,” said Nigel Correia, operations manager at Alcohol Countermeasure Systems. “We needed leading-edge technology combined with low power and low cost, and Xilinx delivered.”

ACS partners with North American and European law enforcement agencies in the deployment of its technology. The Elan alcohol breath tester is available to the public and can be ordered directly from ACS online at [www.acs-corp.com](http://www.acs-corp.com). ❧

# FPGAs Are the Brains Behind "Smart" Cars

Digital signal processing with Virtex-II Pro FPGAs from Xilinx enables a wide range of sophisticated electronics designed to make driving safer.





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According to a study carried out by Visteon Corporation, safety is the number one concern of vehicle customers. It's at the heart of the consumer priority hierarchy (Figure 1).

Increasingly, equipment designers are turning to programmable technology to make cars – and driving – safer. Far beyond the more familiar tire and braking technology, side impact protection, and airbags, today's "driver assistance" systems have evolved from the physical to the electronic domain. The latest electronics-rich vehicles use sensors to continuously evaluate surroundings, display relevant information, and in some instances, even take control of the vehicle.

### Safer, More Efficient – and More Comfortable

Driver assistance systems can offer basic safety features, such as adding infrared (IR) cameras to improve visibility, but the more advanced equipment can warn the driver of potentially dangerous situations. Using a wider array of sensors, these electronic systems enable the vehicle to be aware of surrounding traffic, lane direction, and potential collisions. The ultimate aim is to enable the vehicle to react automatically – whether this involves giving the driver information or assisting with car control – so that occupants are kept safe.

For example, some of the latest trucks are equipped with video cameras that capture images of the lane ahead. If the vehicle changes lanes without using indicators – a sign, perhaps, that the driver is fatigued – an alert is sounded through the cabin loudspeakers.

Driver assistance can also make drivers more comfortable by automating routine actions. Conventional cruise control, for

example, has now evolved into adaptive cruise control (ACC), which automatically controls the throttle. ACC brakes to match the speed of the vehicle in front and keep a safe distance from it. If the vehicle ahead accelerates or changes lanes, ACC returns to the pre-set speed of the cruise control.

output control signals, each under the control of its own processor (a Xilinx MicroBlaze™ 32-bit soft processor, for example, or even an embedded IBM PowerPC™ in a Virtex-II Pro™ FPGA, Figure 2).

The high-speed section is dedicated to the real-time processing of video coming

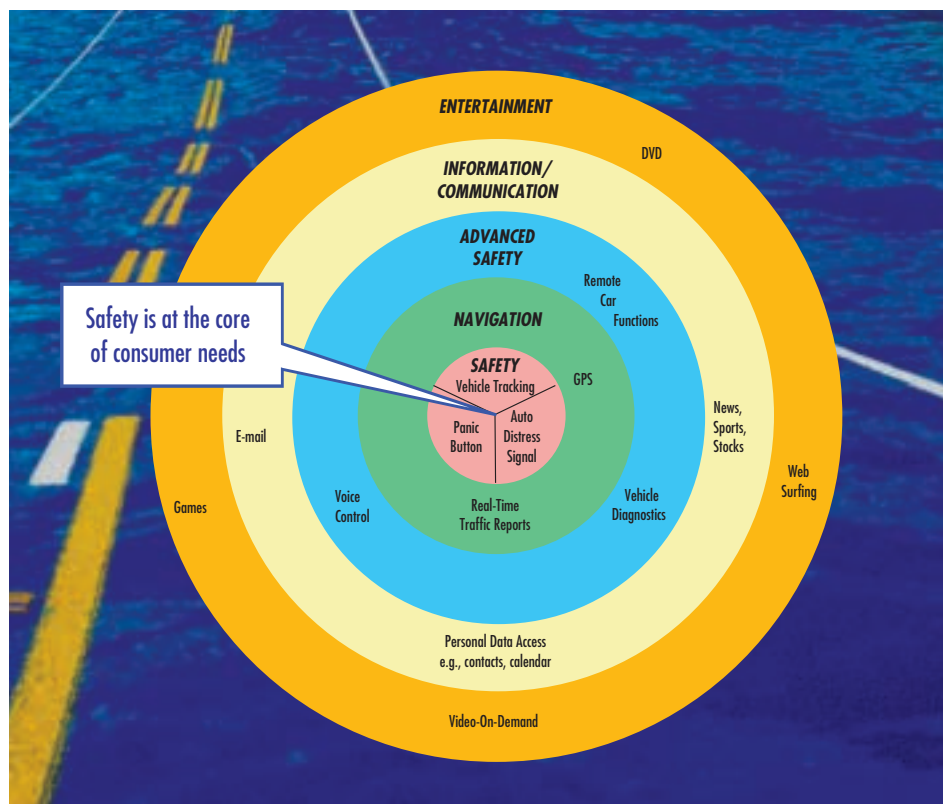


Figure 1 - Hierarchy of consumer needs (courtesy Visteon Corporation)

Other new developments may also serve to make traffic more efficient. The "electronic tow bar," for example, will enable truck convoys in which the lead vehicle is driven manually and the following trucks are driven automatically. In addition to taking some of the burden from drivers, the distance between trucks can be greatly reduced because the electronic driving device reacts faster than a human. Not only does this save valuable road space, but by traveling in the slipstream of the vehicle in front it saves fuel as well.

### Xilinx FPGAs in Driver Assistance Systems

A driver assistance system is partitioned into very high-speed input processing and relatively low-speed sensor inputs and

from the cameras mounted at the front of the vehicle. Given the critical nature of the application – crash avoidance, emergency procedures, and alerts – real-time processing is absolutely essential. Typically, two or more cameras will be used to capture a stereo image, thus enabling calculation of image depth (directly related to real distances from objects) in the FPGA. This information, combined with radar and laser measurements, plus the information collected from gyros and wheel sensors to detect motion, yields a very accurate map of the vehicle's surroundings and its path.

Capturing and processing this information in real time requires the use of math-intensive digital signal processing (DSP) algorithms. Software processing cannot

meet these performance requirements, and it often takes several conventional DSP processors to perform such high-speed tasks. Frequently, even ASSP (application-specific standard product) video processors cannot match the extremely high-speed DSP performance of Xilinx FPGAs, also known as XtremeDSP™ processing.

In addition, using fully flexible FPGAs rather than off-the-shelf video components enables equipment manufacturers to

easily develop the unique, optimized edge detection, image depth, and enhancement algorithms that will differentiate system performance from the competition.

After processing the video, the decision tree mechanisms can be partitioned between hardware (for speed-critical algorithms such as sudden object avoidance) and processor software (for sounding alerts such as lane drift warnings). Partitioning speed-critical processes into

FPGA hardware also enables testing at real-time rates, something that is impossible to do in software.

### XtremeDSP – Real-Time Image Processing

So why can Xilinx FPGAs offer faster video processing than conventional DSPs? The fundamental reason has to do with the FPGA architecture's inherent ability to process data in parallel. In contrast, a DSP processor takes in successive instructions and data, and processes them in a serial fashion.

In addition, the latest Virtex-II Pro family of devices from Xilinx also has an array of embedded, high-performance multiplier blocks to increase image-processing power even further. This enables the FPGA to be configured as a large array of multiply-accumulate (MAC) engines performing multiple operations concurrently (in a single clock cycle) as opposed to multiple cycles through the single or few MAC engines available in conventional DSPs (Figure 3).

Another advantage of Xilinx FPGAs is that you can size the array precisely to suit the calculation requirements, which is ideal for performing calculations on

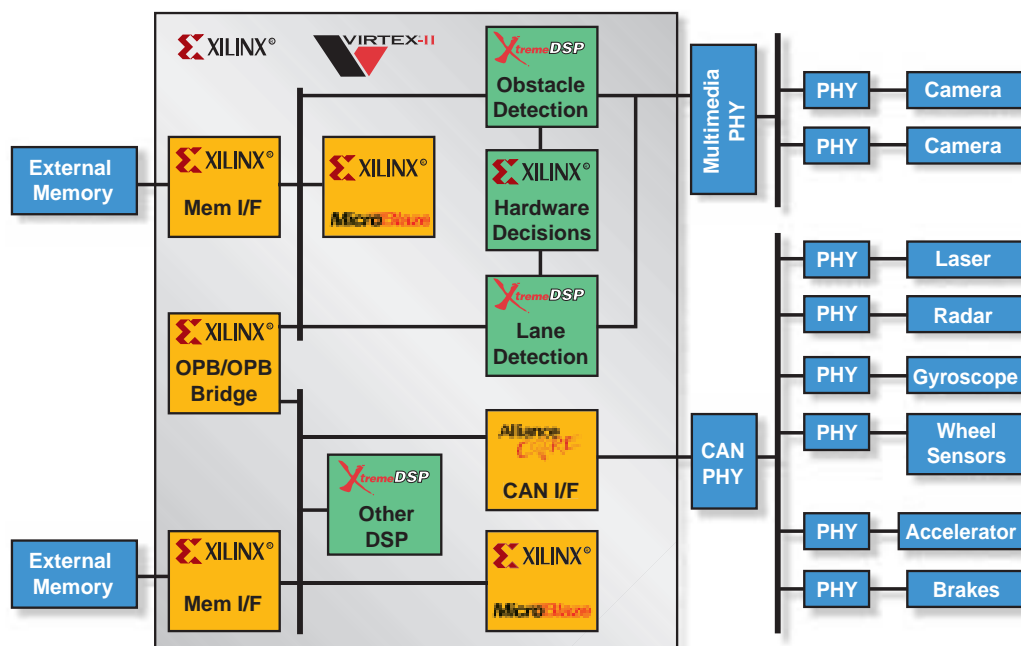


Figure 2 - Concept of FPGA in ACC driver assistance system, with pre-verified Controller Area Network (CAN) interface core

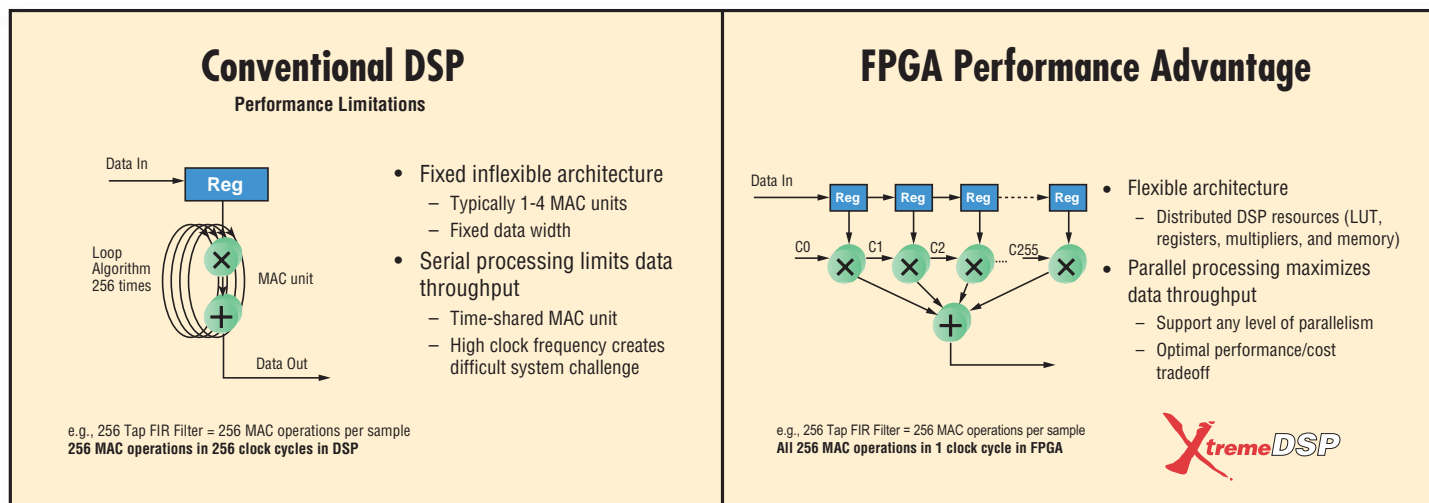


Figure 3 - Xilinx FPGAs offer unrivaled DSP performance.

images. Calculations can be performed on clusters of pixels, such as discrete cosine transform (DCT) macroblocks, concurrently with other blocks in the picture instead of having to scan the entire picture sequentially. And because processing can now be done in real time, less memory is needed for buffering pixel values when using FPGAs.

In addition to real-time performance, the reprogrammability of Xilinx FPGAs also offers superb system flexibility, enabling algorithm upgrades even after deployment. This is important, as current driver support systems are still in the early stages of research and development. As edge- and object-detection algorithms improve over time, hardware upgrades can be accomplished in a matter of minutes and with no board redesign.

### Bridging Automotive Networks

Today, multiple network technologies have emerged that cover various functions and features in the car. These technologies range from multimedia networks, such as media oriented systems transport (MOST) in the cockpit, to car control networks like FlexRay™ automotive control systems. As vehicles evolve into a truly networked arena, equipment manufacturers must determine which standard will be the most successful or offer the greatest advantage over other network protocols.

However, one of the real benefits of using an FPGA rather than an ASSP is that it allows you to produce designs that precisely match interfaces and peripherals to the system requirements – particularly useful when trying to interface with protocols in the early stages of development. When you're trying to get a product to market quickly, a chipset or ASIC (application specific integrated circuit) re-spin is both costly and time-consuming.

With an FPGA, if the specification of a network protocol changes during a standard's early days, all it takes to support the latest revision is a relatively simple redesign in software and a download of the new hardware configuration. You can even do it over a wide area network using Xilinx IRL™ (Internet Reconfigurable Logic) technology, which means the hardware can

be revised during maintenance without costly recalls or extra manpower.

### IQ Solutions for Automotive Applications

To address the needs of automotive electronics equipment designers, Xilinx has created a new range of devices with an extended industrial temperature range option. Called the "IQ" range (Table 1), it comprises current Xilinx industrial grade (I) FPGAs and CPLDs qualified to a new extended temperature grade (Q).

The first products qualified to operate at the new temperature grade are Spartan™-XL 3.3V FPGAs ranging from 5K gates to 30K gates, and the 36 and 72 macrocell XC9500XL 3.3V CPLDs. In the coming months, the IQ family will be expanded to include FPGA devices up to 300K gates, and CPLDs up to 512 macrocells in density (Table 2).

### Conclusion

The new wave of driver assistance systems requires high-performance image processing without sacrificing flexibility, especially during early stages of research and development of object detection and automotive network technologies. The use of Xilinx FPGAs at the heart of such systems offers the industry's best DSP performance, unrivaled support for network connectivity standards, and gives system architects a fully flexible design platform with which to work. Working in real time, these systems provide emergency driver alerts, assist car control, and significantly increase safety. ❧

Temperature Grade/Range °C			
Product	C	I	Q
FPGA	T <sub>J</sub> = 0 to +85	T <sub>J</sub> = -40 to +100	T <sub>J</sub> = -40 to +125
CPLD	T <sub>A</sub> = 0 to +70	T <sub>A</sub> = -40 to +85	T <sub>A</sub> = -40 to +125

Table 1 - Temperatures supported by Xilinx products

Xilinx IQ Solutions Silicon Selector			
Product Family	Packages	Voltage	Density Range
XC9500XL CPLDs	VQ44, VQ64, TQ100	3.3V	36 - 72 Macrocells
CoolRunner XPLA3 CPLD	VQ44, VQ100, TQ144, PQ208	3.3V	32 - 512 Macrocells
CoolRunner-II CPLD	VQ44, VQ100, TQ144, PQ208	1.8V	32 - 512 Macrocells
Spartan-XL FPGA	VQ100, TQ144, PQ208, BG256	3.3V	5K - 40K Gates
Spartan-II FPGA	TQ144, PQ208, FG256,	2.5V	15K - 200K Gates
Spartan-IIe FGPA	TQ144, PQ208, FT256, FG456	1.8V	50K - 300K Gates

Table 2 - Xilinx IQ solutions silicon for automotive applications

Further Information	
<a href="http://www.xilinx.com/esp/technologies/consumer/automotive.htm">www.xilinx.com/esp/technologies/consumer/automotive.htm</a>	Xilinx Emerging Standards and Protocols (eSP)
<a href="http://www.xilinx.com/automotive">www.xilinx.com/automotive</a>	Xilinx Automotive Products – The IQ Range
<a href="http://www.xilinx.com/dsp">www.xilinx.com/dsp</a>	Xilinx DSP Central
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# The Right Features... The Right Fit

The Memec Design Virtex-II Pro™ Development Kit provides an extremely versatile, cost-effective means to design and verify applications based on the Xilinx® Virtex-II Pro™ FPGA family. With the Kit, designers can explore the embedded PowerPC™ and multi-gigabit serial transceivers included in Virtex-II Pro.

## The Kit Features:

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- Four Rocket I/O™ Multi-Gigabit Transceivers that support 3.125 Gbps per port
  - 8 M x 32 SDRAM
- P160 expansion slot for 110 user I/O
- Interface to SystemACE™ module
- Configuration through JTAG and ISP PROMs

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# How to Design a 3DES Security Microcontroller

Using IP cores and a pre-integrated IP platform, engineers at SoC Solutions built a custom microcontroller platform in less than two weeks.

Alliance



by James Bruister  
President  
SoC Solutions, LLC  
[jbruister@socsolutions.com](mailto:jbruister@socsolutions.com)

Today's seemingly limitless access to information has also brought forth a need to secure personal and corporate information from unauthorized access and to protect privacy. This need for secure data not only applies to securing wired and wireless communications, but is also important in applications where access control, data integrity, confidentiality, and authentication are required. For this reason, cryptography will find its way into a host of common devices, including bank ATMs, kiosks, information portals, video surveillance equipment, building access controls, and the like.

The problem of securing data is a complex one, and applications requiring cryptographic processing are varied. Many devices need 3DES (Triple Data Encryption Standard) hardware acceleration, because software implementations are simply too slow. In addition, most designs require a combination of features not readily available in off-the-shelf components.

To implement a custom interface or protocol that meets the product's specific functional requirement, you must either develop with FPGAs or spin an ASIC. In both cases, the most common approach is to first code the design in a hardware description language such as Verilog or VHDL, and then synthesize the design to the targeted silicon, such as a Xilinx Virtex™ FPGA.

In this article, we will describe how we built a secure microcontroller platform using our PiP-EC02 Embedded Controller IP platform with the addition of our 3DES core.

### A Better Approach

At SoC Solutions, we believe the best approach to implementing these secure designs is to start with an IP platform, or IP reference design, which we define as a pre-developed, pre-integrated Verilog or VHDL design. Also known as soft designs or soft cores, these can be targeted to FPGA devices.

### 3DES Secure Data

#### Encryption/Decryption Application

Many applications, such as online private information transfers, require that data files or streamed information be secured by encrypting the payload data. 3DES is considered to be very secure because it can use three separate keys to encrypt data.

Our secure microcontroller implements a smart device that stores 3DES-encrypted data in memory; it then decrypts the data before storing it back to memory. This is useful where data is provided as medium to large data files (or streams) and where the microprocessor has limited bandwidth to do the math-intensive encryption (or decryption) while simultaneously processing other tasks or applications.

The 3DES core uses a three-key concatenated DES algorithm to provide 192 bits of security. Keys can be stored in memory or input through a software application, which is run on the secure microcontroller's microprocessor core. The microprocessor controls data movement to and from memory. It also sets up the 3DES engine. Extra microprocessor bandwidth is available for additional application software. We used a 32-bit microprocessor, although a Xilinx MicroBlaze™ core could also be used in our secure microprocessor design. Figure 1 is a flow diagram of an encryption/decryption microcontroller device.

stored result. In a typical application, a communications port such as Ethernet, PCI, USB, or a simple COM port would be used as a data I/O port.

The design includes a direct memory access engine to read and write data from/to the 3DES core to internal FPGA SRAM or external memory. Also included are an internal SRAM controller, an interrupt controller, timers, UARTS, and an external bus interface.

The process of encrypting or decrypting a file is simple. The microprocessor fills memory from data acquired either under software control or through a

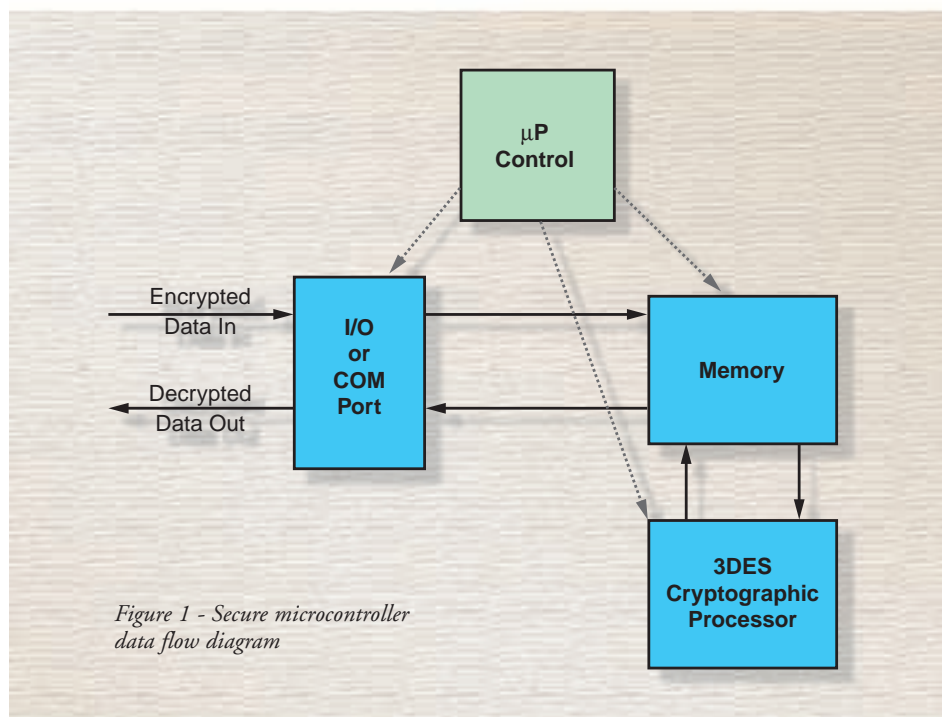


Figure 1 - Secure microcontroller data flow diagram

### Reference Design

The two main hardware components of the reference design are the microprocessor core chip and a platform FPGA, such as a Xilinx Spartan™ or Virtex device. All of the functions (excluding the microprocessor) are implemented in the FPGA using SoC Solutions' IP platforms and soft cores.

The secure microcontroller reference design provides the basis, or starting point, for the custom design. This implementation uses the microprocessor to load memory, control the start of encryption/decryption, and then verify the

COM port. The microprocessor then sets up the DMA engine with a source address, destination address, and a block length. The processor writes a start bit to the DMA engine and then "lets 'er rip." The DMA engine reads a sub-block from the source address, sends it to the 3DES core for processing, and then writes the processed sub-block results to the destination address.

Timers can be used to poll the DMA engine `dma_done` flag to know when the operation is complete. The interrupt controller can also be used to signal the end of the 3DES operation.

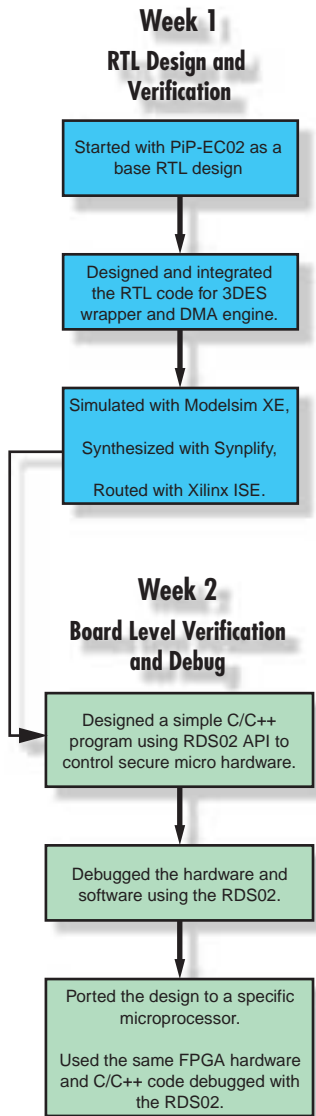


Figure 2 - Secure microcontroller development flow

### Co-Development is the Key

We developed our secure microcontroller in less than two weeks. Figure 2 shows the development method we used.

#### Week 1

To get the design started quickly, we used the SoC Solutions PiP-EC02 pre-integrated embedded controller platform. The PiP-EC02 contained the needed microprocessor subsystem, which included an advanced high-performance bus (AHB) and ARM™ peripheral bus (APB) on-chip, interrupt controller, two timers, internal SRAM controller, 16550 UART, AHB arbiter, and external memory controller

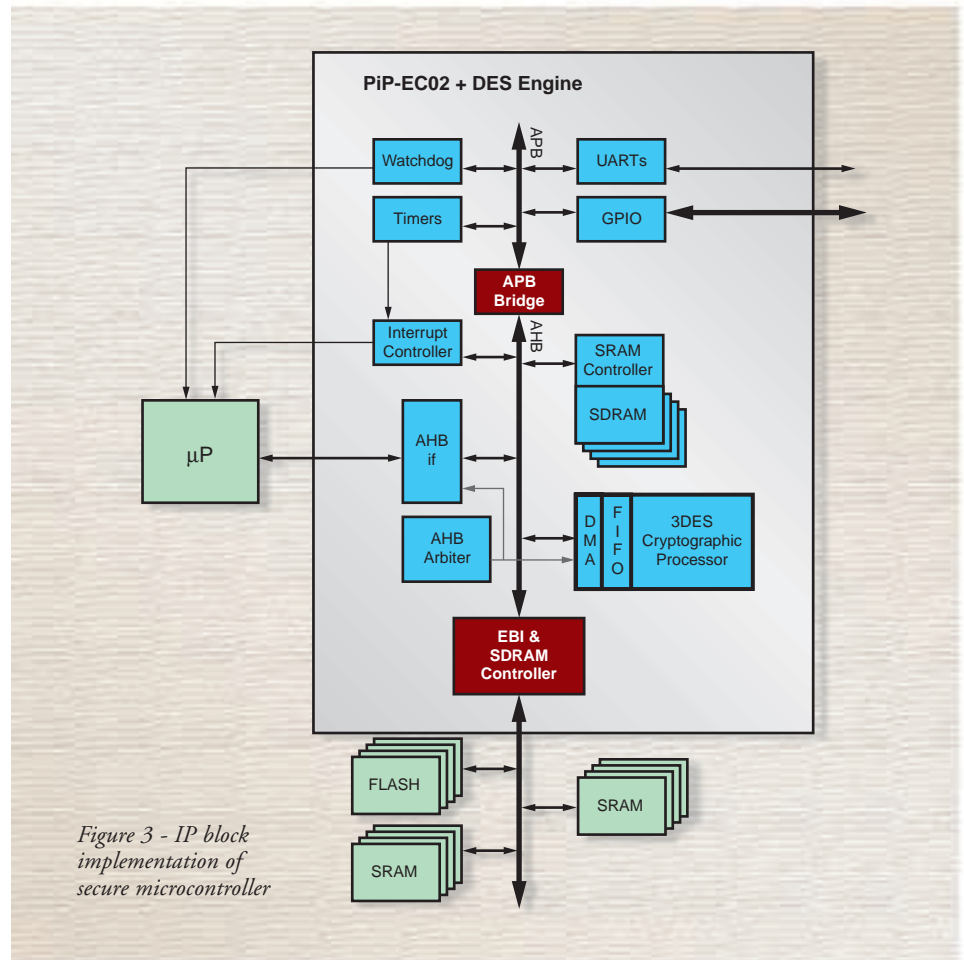


Figure 3 - IP block implementation of secure microcontroller

(EBI). The IP block implementation is shown in Figure 3.

Next, we designed an interface for the 3DES core to the AHB. We selected the AHB to enable fast DMA for 3DES processing. The 3DES interface and wrapper consisted of a combination of a custom DMA controller, input FIFO (16x32), output FIFO (16x32), and the 3DES core. The PiP-EC02 provided the AHB arbiter template. Using the arbiter template to make the DMA connection to the system bus was a very simple design process.

The complete design was then simulated using a Mentor Graphics Modelsim XE (Xilinx Edition) simulator supplied by Xilinx. The PiP-EC02 provided the AHB functional model (BFM), as well as all the test fixtures we needed to test the microprocessor subsystem. We wrote a simple test bench to load memory, start the DMA engine, and then check the encrypted (or decrypted) results that were stored back into memory.

#### Week 2

Now we were ready to try our design in real hardware. To debug our secure microcontroller, we chose the SoC RDS02 Rapid Development System – illustrated in Figure 4 – which allowed us to use Microsoft Visual Studio™ tools to quickly make software changes and debug the hardware on the fly. We used the Xilinx ChipScope™ integrated logic analyzer (ILA) to debug the actual design on the Virtex-E development board, shown in Figure 5. All of these tools were run on the same computer. Stepping through code and triggering the ILA was very easy.

Using the RDS02 proved to be an ideal way to debug, because we tried many, many software iterations. Each iteration took only seconds to recompile and re-run. By comparison, the same software iteration would have been far more time-consuming if we had used typical microprocessor development tools. It would have taken up to five minutes to

reload the system flash memory using the JTAG port.

Once we were satisfied our secure microcontroller hardware was solid and the software was debugged, it was time to port the design to a microprocessor. In our example, we ported the design to an ARM7™ board called the “Brain Board,” shown in Figure 6.

Here again, we took advantage of the PiP-EC02. The PiP-EC02 package provided the boot code and software drivers we needed for the UART, memory controllers, timers, and interrupt controller. As for software, all we had to do was add C/C++ code developed on the RDS02 – and modify the RDS02 API function calls to call ARM7 load and store functions. To do this, we used software-defined macros to retarget the API function calls – nothing much to it.

The hardware port was also just a matter of a simple edit to the AHB microprocessor interface and a Verilog, Synplicity, and Xilinx recompile.

We then retested the secure microcontroller design on the Brain Board running ARM code, and we were done – a prototype in less than two weeks.

#### Secure Microcontroller Features

- PiP-EC02 embedded controller platform
- AHB, SRAM controller, interrupt controller, UART, timers, AHB – APB bridge, external bus interface, general purpose I/O
- 3DES cryptographic processor core
- DES – DMA controller

#### Conclusion

3DES security is just the kind of value-add our customers are turning to as a way of differentiating their products from the competition. By using a co-development approach instead of coding the design first and then synthesizing it, we were able to design in security in less than two weeks.

For more information on SoC Solutions, visit [www.xilinx.com/products/logiccore/alliancesoc/soc.htm](http://www.xilinx.com/products/logiccore/alliancesoc/soc.htm) or contact [sales@socsolutions.com](mailto:sales@socsolutions.com). ❧

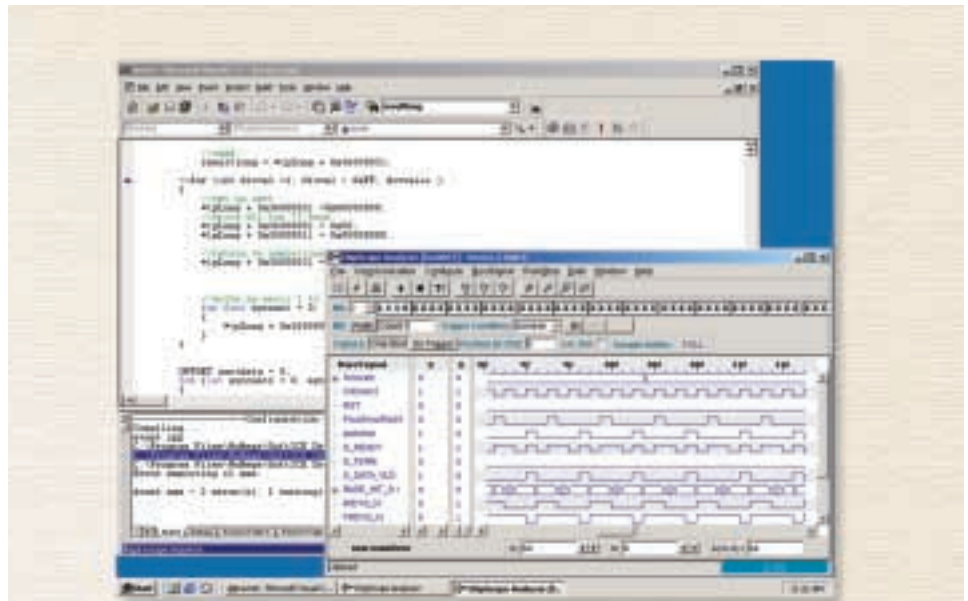


Figure 4 - SoC RDS02 Rapid Development System

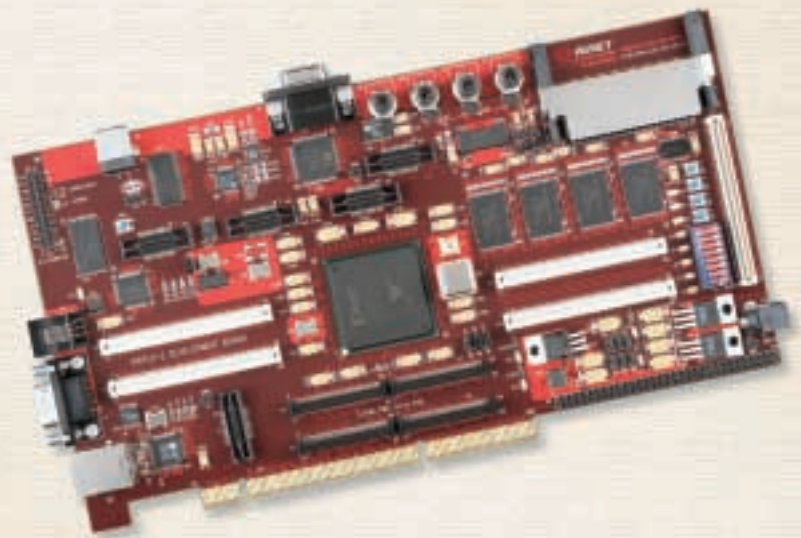


Figure 5 - Virtex-E development board by Avnet

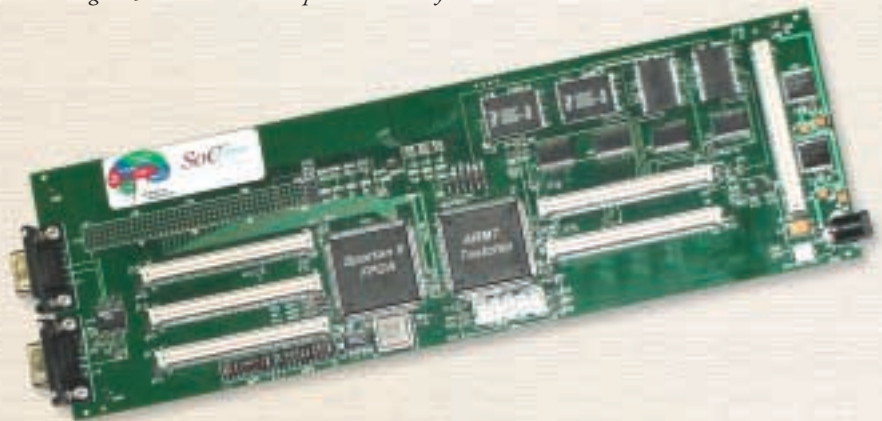


Figure 6 - SoC Solutions' "Brain Board"



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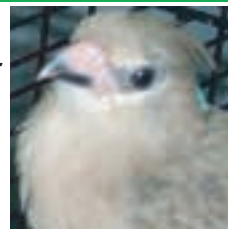
**Mr. Freaky Says:**  
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**Mr. Lazy Says:**

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# How to Use Free Software in FPGA Embedded Designs

Looking to bring the Free Software/Open Source Software movement into the realm of hardware design, Andrey Filippov built a low-cost, high-performance network camera using a Spartan-IIe FPGA and free WebPACK development software from Xilinx.

by Andrey Filippov, Ph.D.  
President  
Elphel, Inc.  
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Just recently, Gordon Moore “renewed” his law for another decade, predicting that the density of integrated circuits will continue to double every 18 months. At this daunting pace, how is it possible to keep up with the ever-growing challenges of electronics design? One answer is to effectively reuse what others have done before, so you can focus on the really new issues.

The growing number of successful adoptions of the Free Software and Open Source Software (FS/OSS) development models has proved the effective reuse of software in applications development.

Xilinx programmable logic devices represent a “frontier” between the hardware and the software worlds. They offer a unique opportunity to apply FS/OSS solutions to hardware design.

I strongly believe that the potential for successful applications of the FS/OSS models to hardware design is even higher than for software itself – you can always make a profit by selling the actual hardware. In this article I’ll show how this approach helped me to create a high-speed, high-resolution network camera (a class of cameras that do not need additional computers to serve digital images and video over the LAN or the Internet).

## Background

I had my first experience with GNU/Linux less than two years ago when I realized I would have to program the network cameras I designed around the ETRAX100LX processor. The processor, made by Axis Communications AB, was optimized for running GNU/Linux. Having the experience of designing many microprocessor-based systems that were mostly programmed in assembly languages, I was really amazed that in just a couple of weeks my camera was able to serve JPEG images over a LAN using HTTP protocol. It was possible to control acquisition and view images using any standard web browser.

That Model 303 camera combined software from multiple sources – GNU/Linux itself, specific code for the ETRAX platform, and many, many others. I just had to add specific drivers for my hardware and modify some of the existent programs. What impressed me the most was the ease of navigation in big, third-party software systems where I could find just the right place to insert small patches of code to modify functionality.

Being primarily an electronics designer, I started to think it was possible to make similar productivity enhancements to the hardware/FPGA part of the camera system.

### Design Goals

Starting the design of a new camera – Model 313, shown in Figure 1 – I had the following goals in mind:

- **A high-performance, simple network camera** that fully supports the frame rate/resolution of megapixel CMOS sensors. That means 15 fps at 1280x1024 resolution (or proportionally, 60 fps at 640x512 resolution, for example).
- **Use a reconfigurable FPGA** for image acquisition/processing/compression – as opposed to two specialized ASIC chips and one-time-only programmable devices (as was used in the model 303 camera). That goal came from the following requirements to:

- **Simplify the product development.** I estimated if that if I were to com-

pletely troubleshoot a one-time programmable FPGA by simulation, it would be too difficult and time consuming. On the other hand, the Xilinx Spartan™-IIE XS300E chip was five times higher (in gate count) than the biggest anti-fuse FPGA I was able to design. Having the option to switch between simulation and actual hardware testing proved to be much more efficient.

- **Make the system flexible with upgradeable “hardware” algorithms** in the same way as it is done with software – this would significantly increase the lifespan of the product.
- **Increase the number of possible product applications** by providing a customizable development platform.
- **Use free, downloadable development tools** so you could customize my product without spending thousands of dollars on software.

### Selecting the Right FPGA

When I started to think about the new camera design, my only FPGA experience was with anti-fuse devices of up to 60K gates. So, I was open to consider different FPGAs that matched my design goals. (At that point, I was not even sure it was possible.)

Soon I came upon a good candidate. It was the largest (at that time) member of the Xilinx Spartan-IIE family – a 300K-gate XS300E.

To find out if the XS300E was capable of handling JPEG compression of 1.3 megapixel images at 15 fps, I “window-shopped” for commercial IPs that performed similar tasks. I was able to find some device utilization specs that indicated that I would have enough room to implement all the functions I needed: frame buffer SDRAM control, image fixed pattern noise elimination, color space conversion, and CPU interfacing.

I did not use that IP, however, because it would prevent me from having an open source design. So, I just used the IP specs as a temporary substitute for my own lack of expertise in Xilinx devices.

Knowing that my project was doable in terms of hardware, I downloaded for free WebPACK™ 4.2i software from the Xilinx website to try it out. I wanted to see if there was anything else I was not aware of, at the moment, that would prevent me from following my plan.

To get some initial experience with both Xilinx devices and software, I read Xilinx Application Note XAPP610 and decided to try an 8x8 DCT core (needed for JPEG compression). The application note provided Verilog sources, which allowed me to synthesize, map, and place-and-route the design – but I had problems trying to simulate the design.

It turned out that the “lite” version of a third-party simulator bundled for free with the WebPACK software had limitations on design complexity. The most obvious problem was the 500-line limit on the source code. The XAPP610 DCT implementation alone was bigger, but I was able to try simulation by removing comment lines and combining multiple lines into one.

The “lite” simulator did run, but that workaround trick would not work for my complete project, so I had to forget about that simulator and use something different.

All the rest of the WebPACK software worked just fine for me. Eventually, I was able to utilize more than 98% of the chip’s resources to meet all of my timing constraints.

### System Architecture

Now that I knew I could fit my design to a Spartan-IIE, I switched to the schematic and PCB design. The Model 313 camera consists of two boards, shown in Figure 2. The small board has just the CMOS image sensor and closely related circuitry.

The main board consists of a 1.48 by 3.50 inch, four-layer PCB that has the following principal components:

- **32-bit, 100 MHz processor** (ETRAX100LX, Axis Communications) running a



Figure 1 - Model 313 Elphel network camera



Figure 2 - Main PCB of Model 313 camera

GNU/Linux operating system. The processor has multiple embedded peripherals, including a network MAC.

- **10/100 Mb Ethernet PHY** (BCM2521A4KPT, Broadcom).
- **16 MB (4Mx32) SDRAM** system memory (MT48LC4M32LFFC-8, Micron).
- **8MB (4Mx16) flash memory** (MT28F640J3FS-12, Micron) used to store GNU/Linux, applications, Web pages, configuration files, as well as bitstreams for the FPGA configuration.
- **Spartan-IIE, 300K-gate, reconfigurable FPGA** (Xilinx XC2S300E-6FT256) used to control image acquisition, processing, frame storage in SDRAM, image compression, and transfer to the system memory using the processor DMA channel. The FPGA is configured using JTAG pins connected to the general-purpose parallel port of the processor.

- **Image memory, 16 MB (8Mx16) SDRAM** (MT48LC8M16LFFF-8, Micron) connected directly to the FPGA so that accesses do not interfere with the system bus. This memory is dedicated to the image frame buffer that is used to store both the uncompressed image data as well as calculated coefficients for the on-

the-fly FPN (fixed pattern noise) elimination (subtraction of the background frame and multiplying each pixel by its reverse sensitivity).

- **3-PLL programmable clock generator** (CY22393FC, Cypress). This part provides fixed frequencies that have to be available during system startup (20 MHz processor PLL input and 25 MHz for the network PHY). It also generates two programmable clocks that add extra flexibility for FPGA operation (in other words, it is possible to compare simulation results with the actual maximal operation frequency for any particular module).

- **IEEE 802.3af compliant power over LAN** uses an isolated DC-DC converter to supply 3.3V from the input 48 VDC. An additional converter provides 1.8V to the Spartan core.

### FPGA Code

Most of the system functionality is implemented in the Xilinx Spartan-IIE FPGA. The code is written in Verilog HDL and is available for download at my Elphel website under the GNU/GPL (general public license) license. It is designed around a four-channel SDRAM controller that uses embedded block RAM modules as “ping-pong” buffers to provide quasi-simultaneous block access for the following data sources and receivers:

- Image data from the sensor, either processed or raw, one- or two-bytes per pixel, arranged as 256 (128) pixel lines
- Calibration data to the FPN elimination module prepared by software in advance, 128x16-bit blocks
- Data to the JPEG compressor, arranged as square blocks of 16x16 bytes

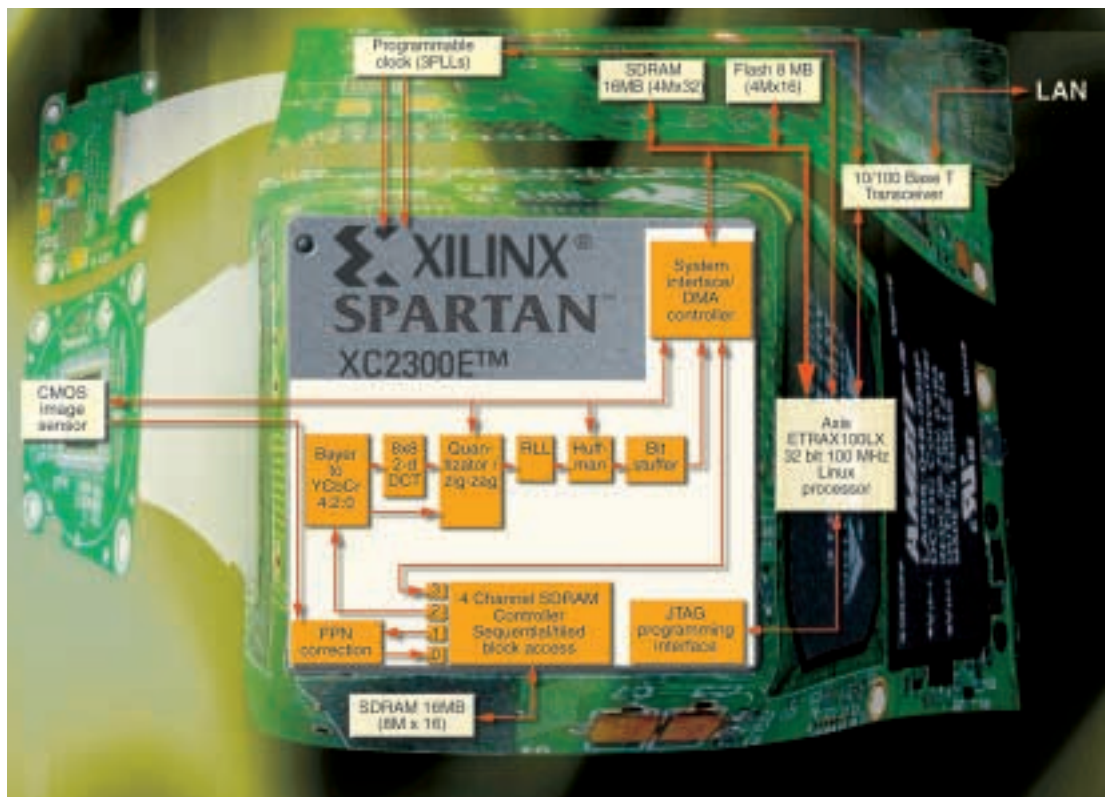


Figure 3 - The importance of the JPEG encoder in the Spartan-IIE dwarfs the other components on the PCB.

- CPU access to the SDRAM (normally used to read raw sensor data and write back the calibration data for the FPN elimination).

The JPEG encoder uses two-thirds of the FPGA resources, as shown in Figure 3. The encoder consists of the chain of the processing modules, some of which use block RAM for data buffering and table storage:

- Bayer-to-YCbCr converter
- 8x8 DCT based on the Xilinx XAP610, modified to provide block-asynchronous operation and to increase dynamic range
- Quantizator and zigzag encoder
- RLL encoder
- Huffman encoder
- Bit stuffer.

The output data is transferred to the system memory using the CPU DMA channel.

## Results

Since the Elphel Model 313 reconfigurable, high-resolution network camera was first described in the LinuxDevices online magazine Dec. 3, 2002 (and Dec. 4, in Slashdot), many of the inquiries I received have been about its open nature as a user-customizable platform.

There are four possible kinds of customization of the camera. Three of them are inherited from the previous Model 303 camera and are related to the open software:

1. Modification of the user interface with Web design tools
2. Addition of new applications (or modification of existent ones) that can be downloaded to the camera
3. Modification of the kernel (Linux) to add new drivers.

However, only the use of the Xilinx reconfigurable FPGA – supported by the free-for-download ISE WebPACK development tools – made it possible to increase the camera performance nearly 100 times. This hardware/software customization turned out to be the most powerful of the four possible types of customization:

4. Modification of the “heart” of the camera – the Spartan-IIIE XS300E FPGA.

As of now, the camera has only a baseline JPEG compression algorithm implemented in the FPGA, which can serve still JPEG images and Apple Quicktime movies that are made of a sequence of the JPEG-encoded frames.

By adding new software to the camera processor and HDL code to the FPGA, you can use the camera for experiments with advanced image/video compression algorithms – such as 2000JPEG for better size/quality still images or MPEG (-1, 2, 4) for video. Additionally, you could program the camera processor and FPGA for motion detection, pattern recognition, particle discrimination — or whatever else you may think of.

## Conclusion

So how did the FS/OSS approach help me to create the Elphel Model 313 camera? Maybe it did not cut my FPGA development time in the same proportion as it did for the software development – the area where it is really mature. But the overall FS/OSS co-design technique really worked:

- I used free Xilinx 2-d DCT implementation that utilized about 30% of the chip resources. It did not meet exactly the requirements of my design – but this is where the advantage of free code is obvious: I could modify the code in a way I liked. With closed proprietary IPs you can't do this.

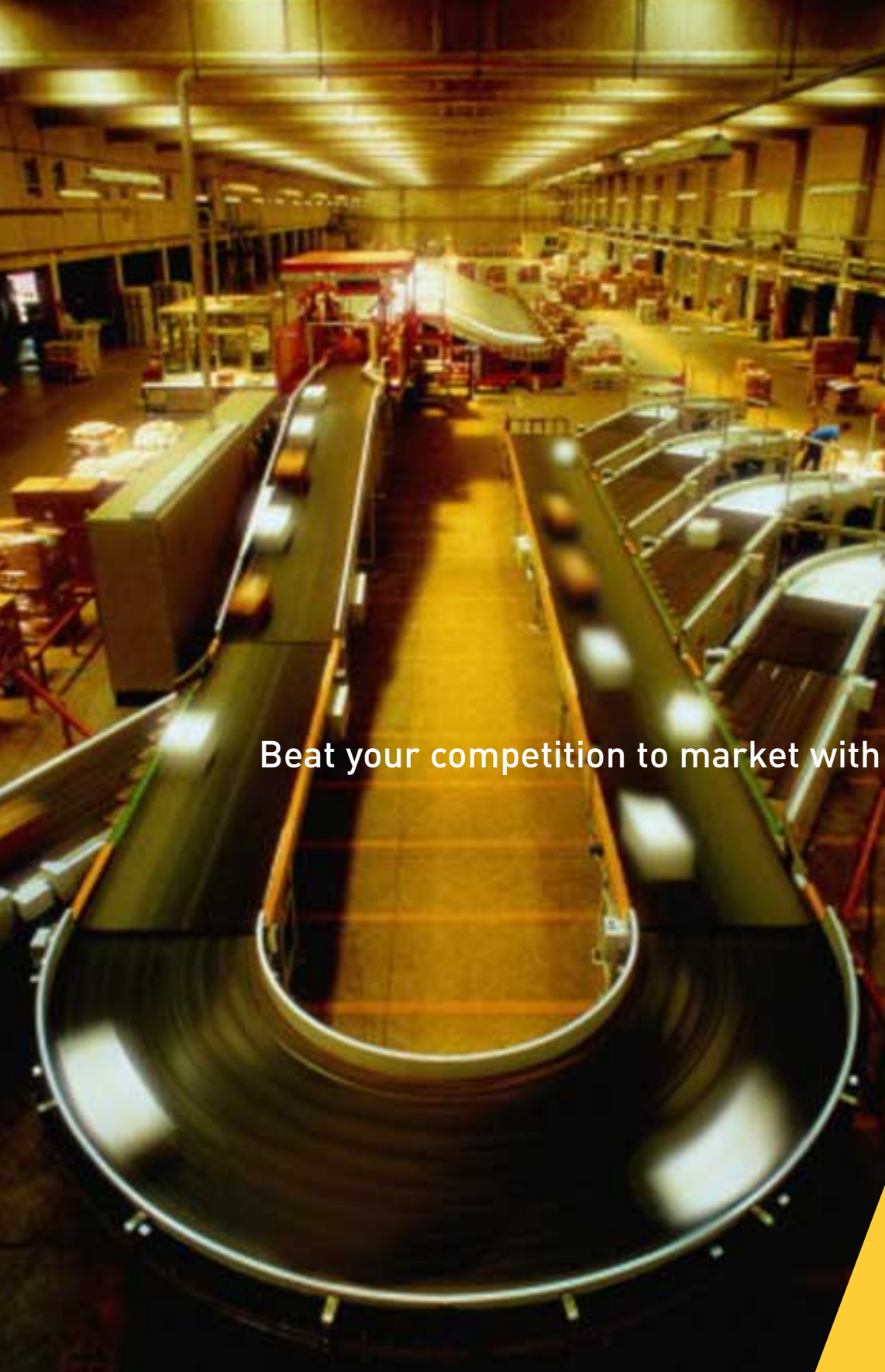
- The resultant product has unique features that I was desperately looking for as a customer. I wanted a camera I could modify to fit my needs. In many cases, the required modifications I wanted were really minor – but still impossible in a proprietary camera.

On several occasions I was asked, “Isn't that scary to open your design? What if somebody will use it and get all the money?”

- First of all, the license used for the Elphel products (GNU/GPL) is not exactly the same as the public domain. Any company that wants to manufacture cameras based on Elphel designs will have to play by the same rules – the GPL legal protection is no weaker than that of closed source proprietary licenses.
- It is actually impossible to steal this kind of an open design. Even if someone in some far-away country (where there are no copyright laws and GPL is not enforceable) manufactured a derivative closed product, it would lack the critical feature of Elphel cameras – their custom reconfigurability with Spartan FPGAs.
- Elphel has more cameras under development, and I would consider wider availability of the products based on the Model 313 design as free promotional material for my company. ❌

### URLs for more information:

- [www.xilinx.com/spartan2e/](http://www.xilinx.com/spartan2e/) – Spartan-IIIE FPGA family
- [www.xilinx.com/ise/webpack5/](http://www.xilinx.com/ise/webpack5/) – latest free ISE WebPACK software
- [www.xilinx.com/xapp/xapp610.pdf](http://www.xilinx.com/xapp/xapp610.pdf) – Application Note XAPP610 “Video Decompression Using IDCT”
- [www.elphel.com](http://www.elphel.com) – schematics and software for Model 303 and 313 network cameras
- [developer.axis.com/products/etrax100lx/](http://developer.axis.com/products/etrax100lx/) – Axis ETRAX 100LX platform
- [www.fsf.org](http://www.fsf.org) – Free Software Foundation
- [www.opensource.org](http://www.opensource.org) – Open Source™ Initiative
- [www.linuxdevices.com](http://www.linuxdevices.com) – previous articles on network cameras.



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# Xilinx Delivers HyperTransport Lite Reference Design

Xilinx Virtex-II Platform FPGAs and Broadcom's MIPS-based processors enable rapid development of gigabit Internet protocol products.

XILINX  
REFERENCE DESIGN  
Alliance Program  
**BROADCOM**

by Xcell Staff

A new minimal HyperTransport™ (HT-Lite) reference design for Xilinx Virtex™-II Platform FPGAs enables rapid development of designs using Broadcom™ MIPS™-based processors. The Virtex-II FPGA leverages Xilinx flexible SelectIO™-Ultra technology and Broadcom's minimal HyperTransport IP to create a bridge between processors and ASSPs.

This reference design underscores the companies' commitment to a technology relationship aimed at providing interoperable interfaces for use in communications, networking, and consumer applications. The HT-Lite reference design is one of several efforts resulting from Broadcom's membership in the Xilinx Reference Design Alliance Program.

"Collaboration between companies like Broadcom and Xilinx – both Hyper-

Transport Technology Consortium members – ensures that the HyperTransport technology will continue to satisfy the ever-increasing need for bandwidth," said Gabriel Sartori, president of the consortium. "The reference design demonstrates how HyperTransport technology enables next-generation networks by providing a universal connection that reduces the number of buses within a system, provides a high-performance link for embedded applications, and enables highly scalable multi-processing systems."

"By combining the highly flexible Xilinx Virtex-II FPGA solution with our MIPS-based processors, OEMs can easily add additional features with minimal impact to their design schedules," said Krishna Anne, strategic marketing manager of Broadcom's Broadband Processor Business Unit.

**Collaboration between companies like Broadcom and Xilinx – both HyperTransport Technology Consortium members – ensures that the HyperTransport technology will continue to satisfy the ever-increasing need for bandwidth.**

The HT-Lite reference design is used as a slave interface to end an HT chain supporting an 8-bit link width at a design speed of 400 MHz DDR (800 Mbps per I/O). The HT-Lite core uses fewer than 1,900 slices in a Virtex-II FPGA.

The HT-Lite reference design is available now free of charge. Documentation and instructions for downloading the reference design can be found at [www.xilinx.com/xapp/xapp639.pdf](http://www.xilinx.com/xapp/xapp639.pdf). Customers in need of a full-featured HyperTransport solution can use the full HT core, also available now at [www.xilinx.com/ipcenter/](http://www.xilinx.com/ipcenter/). **Σ**

# Low-Cost IP Connectivity Lets Diverse Systems Communicate

The proliferation of interface and communication standards from industry to industry has made it difficult to get systems talking to each other. A configurable low-cost board solves the problem.

by Grant Stockton  
President & CEO  
Technovare Systems, Inc.  
[grant@technovare.com](mailto:grant@technovare.com)

Tough economic conditions and cost sensitivity are making it difficult for designers of commercial and industrial equipment to provide the one feature customers request most – network connectivity. Network connectivity and the ability to manage systems from a Web interface are highly valued. But implementing them has remained elusive because companies do not want to design them in as a standard feature during an economic downturn.

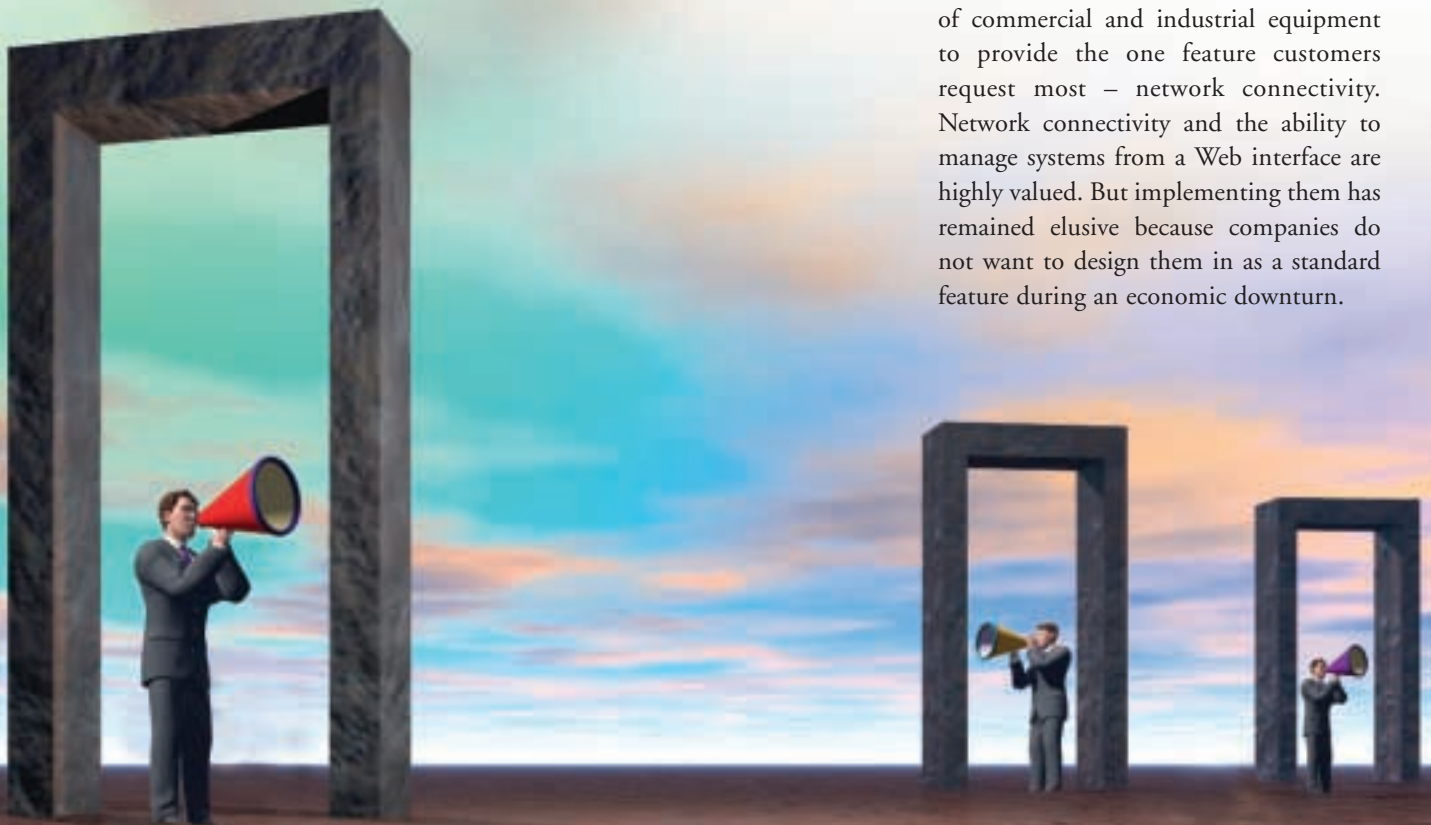






Figure 1 - NEP board TSINET100BT32C

Technovare's Network Enabled Processor™ (NEP) board shown in Figure 1 provides an off-the-shelf solution to this dilemma by letting system designers integrate networking into their feature set quickly and without the expense of an additional design cycle.

The NEP board integrates an embedded Web server that performs all of the processing and services required for network connectivity such as TCP/IP, SNMP, HTTP, Telnet, and FTP. A key enabling feature of the NEP board is a user-definable interface implemented by a Xilinx Spartan™ FPGA.

The Spartan FPGA's flexibility and configurability allows host systems to communicate with the NEP board using any digital format, protocol, or standard.

Standard interfaces such as RS-232 and RS-485 are available on all versions of the NEP board. Once TCP/IP processing has taken place, data can be sent out over a standard network connection consisting of a single 10/100 BaseT Ethernet port.

Cores for many parallel and serial interfaces such as I<sup>2</sup>C, SDLC, EPP, USB, and CAN are available and can be integrated on request.

In addition to providing you with a network-connectivity solution, the NEP board is also a generic processing platform that can offload your host system of computing overhead and even run an entire embedded application. Equipped with Motorola's 5272 Coldfire™ 32-bit RISC processor, Wind River Systems' VxWorks™ RTOS, 4 Mbytes of SDRAM, and 16 MB of flash RAM, the NEP board is a formidable processing platform for many embedded applications. Its primary features are shown in Table 1.

### Solving Problems for Diverse Applications

Most commercial and industrial applications have developed their own set of standards, protocols, and communication interfaces based upon their own unique requirements.

CAN is widely used in the industrial-automation market, for example, and two-wire communication is widely used in building-automation applications. The convergence of industry-specific communications protocols such as these with IP-based Ethernet has created a large number of nodes in which translation from one network to another is required.

- Programmable interface implemented by Spartan FPGA
- 10/100 BaseT Ethernet interface
- Dual UART interfaces for RS-232 and RS-485 to support serial data transmission, translation, and control
- USB1.1 interface transmits up to 12 Mbps serial data
- 4 MB SDRAM, 16 MB flash memory
- 32-bit Motorola ColdFire™ microprocessor
- VxWorks™ real-time operating system with embedded TCP/IP stack
- Remote configuration and in-circuit firmware update capability
- PC/104 form factor.

Table 1 - NEP board features

The NEP board is ideal for these applications. It provides pre-configured communications interfaces for many standard protocols as well as the ability to create custom interfaces for ones that do not already exist. Its interface translation capability between UART and 10/100 BaseT Ethernet permits easy integration into existing computer and control systems.

As systems mature and more features are

added, you will find the communication protocol that you employ most frequently is often not sufficient to handle the system's bandwidth requirements. To address this problem, the NEP board incorporates a high-speed Ethernet connection. Systems that are now communicating over low-speed interfaces such as RS-232 can easily migrate to IP-based Ethernet.

The NEP board's unique user-defined interface allows applications to take full advantage of 10/100 BaseT Ethernet data rates by allowing parallel and high-speed serial connectivity to the host system.

Just as every industry has its own communications protocol, every system usually has its own user interface. The proliferation of interfaces generally requires user-interface software on the host computer that communicates with the system via RS-232, USB, or some other standard interface. Any other host computer wanting to communicate with the system must first be loaded with the interface software and be directly connected to the system.

This problem is alleviated with the NEP board's embedded Web server. Any host computer with a Web browser can log into the system from any location on the entire Internet – with proper authorization – and have access to the user interface that runs on the NEP board.

Equipped with a 32-bit RISC processor, 4 MB of SDRAM, and 16 MB of flash memory, the NEP board's Web server can serve sophisticated Web pages consisting of HTML-based pages and Java script. For systems that require more memory space, a PCMCIA expansion card will be available shortly.

### Conclusion

The NEP board delivers a user-friendly, Web-based interface that creates network connectivity to everyday existing systems. The board's affordable price – about \$150 for 1,000-unit orders – lets system designers integrate their applications into existing and future systems without affecting cost or product delivery schedules. For more information, visit Technovare's website at [www.technovare.com](http://www.technovare.com). ❧

# Platform Delivers Fast, Flexible AC Servomotor-Control Designs

New digital motor-control applications exceed the capabilities of conventional solutions. International Rectifier's Accelerator platform solves this problem and reduces development time by eliminating programming, coding, debugging, and code maintenance.

by Jasbinder Bhoot  
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Digital signal processors (DSPs) and microcontrollers have traditionally been used for digital motor-control applications in both low-performance AC inverter drives and high-performance servo drives. But a new generation of applications is pushing their performance limits.

Motor control requires both torque and speed control. Torque control is

achieved by regulating the motor current. It requires high-performance computation in the range of tens of microseconds. Speed control, on the other hand, requires relatively moderate computation speeds, typically in the range of hundreds of microseconds.

Both functions are usually implemented by a DSP or microcontroller. A motion-control ASIC is sometimes added to complete high-performance functions such as the PWM (pulse-width modulation) waveform generator, encoder signal interface, and so forth.

Many demanding servomotor applications such as high-speed factory automation systems and fly-by-wire/drive-by-wire vehicle control systems require higher levels of timing performance than ever before.

DSPs and microcontrollers can no longer keep pace with the new generation of applications that require not just higher performance but more flexibility as well – without increasing cost and resources. International Rectifier Inc. provides an answer in its Accelerator™ Motor Control Design Platform. The Accelerator platform leverages low-cost Spartan™ FPGA technology to provide a re-configurable signal-processing architecture that uses soft peripherals. It achieves unmatched motor-control performance with feedback-control-loop bandwidths of up to 5 KHz.

## New Challenges in Motor Control

A class of new motor-control applications that require both high performance and the flexibility to support a variety of motor-

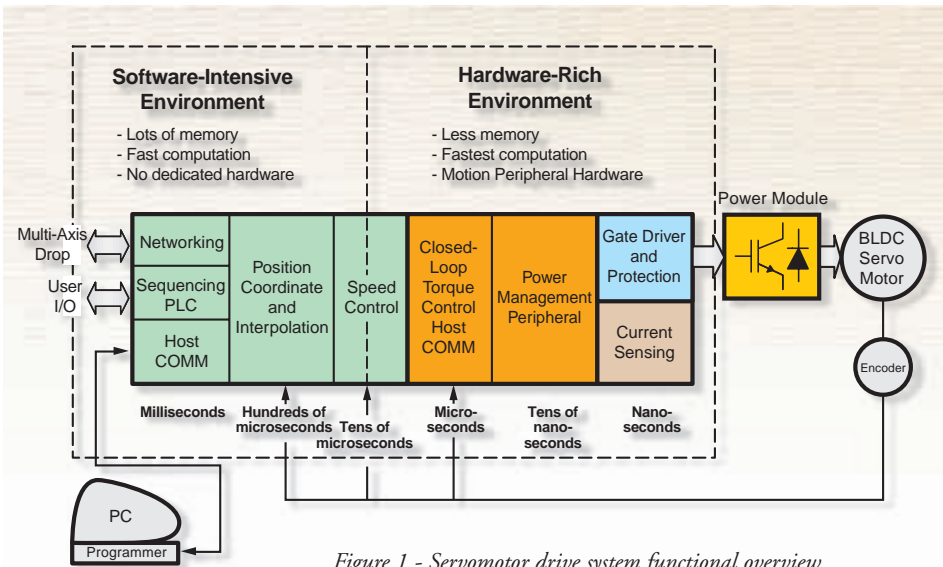


Figure 1 - Servomotor drive system functional overview

feedback scenarios cannot be served economically by off-the-shelf DSPs and microcontrollers. These devices have three inherent limitations:

1. Traditional DSPs and microcontrollers used fixed hardware logic to implement motion peripherals and communication ports. This limits your ability to adapt the design to different types of feedback devices and peripherals.
2. High-end servomotors require significant computation power for torque control. A single DSP or microcontroller cannot always meet performance requirements. Multiple DSPs or microcontrollers are needed, often with an ASIC to perform the motion-control tasks. This not only adds cost but also introduces complex functional partitioning.
3. DSPs and microcontrollers require a high level of support to maintain the torque algorithms. Although the maintenance task is easier if the algorithms are written in a high-level language such as C, they are typically written in assembly language.

### Typical Servo-Drive Control Architecture

In a typical digital closed-loop servo control system, functions are divided into subtasks that operate at different update rates depending on the available bandwidth and processing priority. For example, certain tasks need to be implemented in real-time while others

may be delayed. Or there may be tasks that are one-time driven events. Each task is controlled by a multitasking operating system that is closely coupled with a DSP's or microcontroller's interrupt structure.

Figure 1 shows a functional overview of a typical servo-drive system. The computational requirements can be divided into two segments:

1. A hardware-rich environment for tasks that require very fast computation
2. A software-intensive environment for tasks in which performance is less critical; software implementation, however, requires additional memory bandwidth and programming effort.

Functions that are far from the machine side and closer to the host communication (or a man-machine interface) require much slower processing. These tasks are usually very complex and require a large amount of memory. Torque control, for example, can be implemented using a simple step function, but position coordination and interpolation require many more control parameters and therefore require more memory.

Motor control is made even more complex by a chain-reaction phenomenon. Torque control requires higher performance than speed control, for example, but the impact on system requirements does not stop there. The integral of torque is speed and the integral of speed is position. Due to this chain reaction, each parameter requires a different processing speed. A real-time operating system is needed to satisfy these various processing speeds.

### Standalone DSPs Can't Cut It!

In order to meet the challenges, most standalone motion-control DSPs must increase memory resources for programming and data. Even this may not solve the problem because software solutions for logic peripherals are difficult to implement without sacrificing performance.

Stated in numerical terms, the torque-control loop computation update rate for

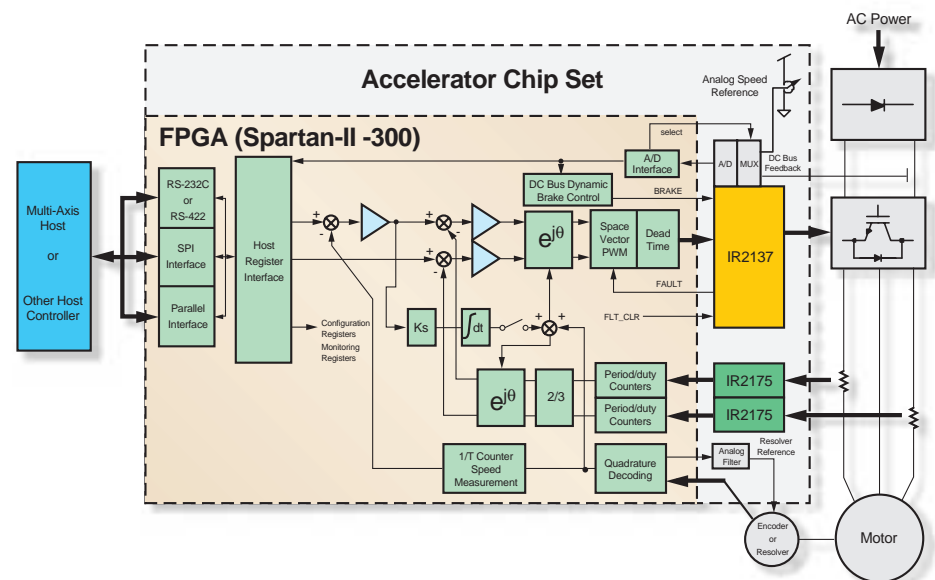


Figure 2 - Accelerator block diagram



Figure 3 - The Accelerator motor-control platform

a servo drive must be in the 25-microsecond range to achieve 4-KHz torque bandwidth. There are also a wide range of emerging motion functions that require very specific programming, fast computation, and unique digital logic. Unique logic of this type includes dead time compensation, monitoring the temperature of the power devices, accurate motor-phase voltage-feedback sensing, current sensing, and motor-machine parameters. These functions require speeds in the nanosecond range.

Implementing motion functions in an ASIC plus a DSP also presents a challenge because it requires functional partitioning. All closed-control functions (including torque control, speed control, and positioning) are

implemented in the DSP or microcontroller. Motion-peripheral functions are implemented in a dedicated ASIC.

Dividing tasks between two ICs is necessary because torque control demands a much faster computation update rate and it becomes extremely difficult to perform torque control and the other control functions. Therefore, the traditional approach of using a DSP or microcontroller – with or without an ASIC – is rapidly approaching the point of being unable to satisfy performance demand, faster development time, and easy, low-cost software maintenance.

### The Accelerator Platform

International Rectifier's Accelerator platform is a complete reconfigurable motor-drive-control design platform. Based on the Xilinx Spartan FPGA family, it provides the flexibility needed for many motion peripheral types as well as the high bandwidth needed for torque control. Flexibility is achieved by providing various object-code sets, which are used to reprogram the FPGA as needed.

Figure 2 shows a block diagram of the Accelerator system. All necessary control algorithms are implemented in the Spartan-II FPGA, including the logic for

the communication protocol. The programmable nature of the FPGA I/O allows direct interfacing to International Rectifier's high-voltage ICs, the IR2137 and the IR2175, which control and sense electrical power to the motor.

### FPGA Technology Makes the Difference

Spartan-II FPGAs deliver the performance that allows critical control functions to be implemented in hardware rather than software. By implementing these parameters in hardware, latency and execution time do not vary: The solution is inherently fast and deterministic. The FPGA-based solution provides computation speed of the current-control function well below 5 microseconds, which in turn enables high PWM carrier frequency update. The FPGA also allows the torque-control loop response to reach 5 KHz at the -3 dB point. This high-bandwidth torque control loop provides low harmonic current ripple. Interfacing with recently introduced low-inductance servomotors such as linear motors becomes much easier.

### Customizable Motion-Peripheral Logic

Servo applications require many different types of interface circuits to accommodate a variety of sensors and feedback devices.

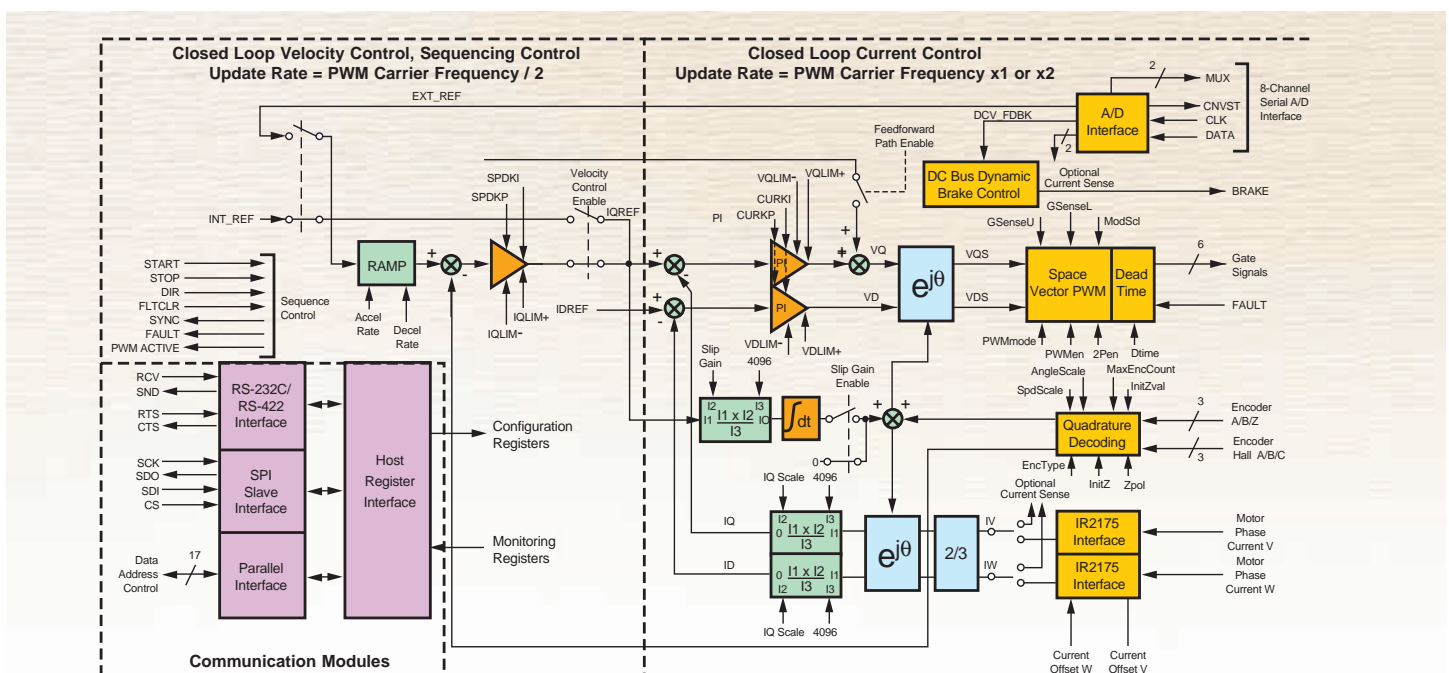


Figure 4 - Detailed control function block diagram

Motor-position sensors may be either an encoder or resolver, for example, depending on the specific application requirements. There are many different types of encoders, such as incremental, absolute, sine, cosine, or serial-data types. Each requires very different logic to implement. By leveraging the programmable nature of the FPGA, Accelerator can support multiple types of feedback devices without changing the physical hardware.

### Accelerator Platform – Hardware Construction

The Accelerator platform is pictured in Figure 3. It is rated to handle up to 1.5-KW output with a 300% overload for 1 second. Its continuous power rating is 230V/7Arms. Position feedback is implemented using an incremental encoder interface with an index marker pulse. Accelerator can support either 115 V or 230 V AC single- or three-phase inputs. The system is also equipped with a variety of protection circuits ranging from over-current protection, short-current protection, and over-temperature protection as well as over-voltage protection.

The Accelerator platform integrates the latest chipsets from International Rectifier – the IR2137 and the IR2175. The IR2137 is a monolithic 600-V high-voltage gate driver with built-in over-current protection. The IR2175 is a monolithic 600-V current-sensing IC in a SO8 package. These two high-voltage ICs teamed with the Xilinx Spartan-II FPGA device simplify the complicated design task of analog and power electronics circuits such as gate drivers, protection, and current-sensing functions.

### System Design Flow and Configuration

The Accelerator platform comes with all the hardware and software needed to design a complete high-performance motor-control system. It supports an encoder-based servo amplifier, resolver-based servo amplifier, and a sensorless control algorithm. Each of these products can be licensed from International Rectifier.

You can configure the control structure, tune the regulator control loop, and choose various communication protocols without rigorous programming effort. Figure 4 shows

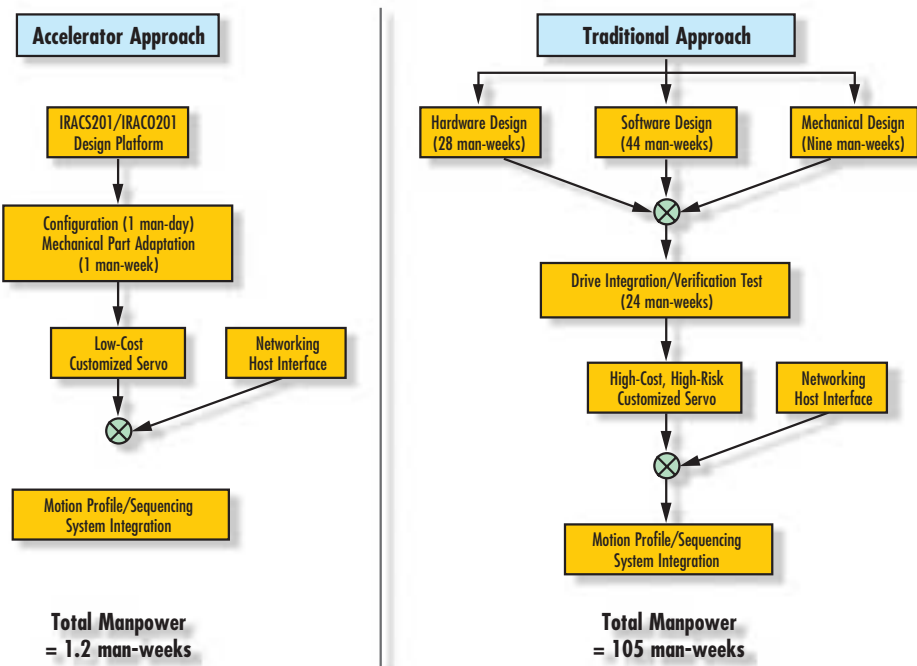


Figure 5 - Servo-drive design process comparison

a block diagram illustrating configuration capability. Configuration switches are located at each control section. An induction machine, for example, can be configured by enabling the slip-gain block and adjusting ID and IQ current feedback scaling gains.

The Accelerator platform includes a toolbox for designing control algorithms using graphically connected control blocks. The toolbox contains the Control Block Library, which is a complete set of control primitives available in Simulink™. It can be expanded when needed to create unique peripheral blocks. The Accelerator platform also uses a unique Matlab™-to-Verilog Porter (MVP) tool, where the Verilog code is generated, synthesized, and directly downloaded into the Xilinx Spartan-II FPGA to configure functionality. This method relieves you of considerable manual translation or re-hosting effort.

Accelerator comes with a Verilog library that contains servo-specific, parameterized, fully tested motion-peripheral circuit modules. A current-sensing interface module, encoder-feedback module, and PWM waveform generator are examples of unique motion peripheral modules.

Figure 5 shows the impact of the Accelerator platform on the resources needed to develop a servo-drive system in compari-

son to the traditional DSP-based approach.

The Accelerator system significantly reduces the development time of a servo design by eliminating programming, coding, debugging, and code maintenance.

### Conclusion

The Accelerator platform provides a low-cost solution for servomotor drive designs and still maintains the levels required for today's high-performance, permanent-magnet, and induction machine control systems. The platform is based on a Xilinx FPGA device that allows flexibility for customized functions without compromising the time-critical machine control functions.

Low cost is achieved in two ways:

- DSP functions are implemented in parallel using FPGA devices. This approach removes the need for using multiple standalone DSPs.
- A proven, flexible hardware architecture allows rapid development of complete systems, which drastically reduces the resources required for rapid system development.

The Accelerator platform is available today directly from International Rectifier. Additional details can be found at [www.irf.com](http://www.irf.com). ❧

# Xilinx FPGA Blasted into Orbit

A radiation-hardened Xilinx FPGA gives the Australian FedSat satellite powerful reconfigurable computing capabilities.

by Peter Bergsman  
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On the morning of December 14, 2002, the ground shook at the Yoshinobu Launch Range at the Tanegashima Space Centre, on the island of Tanegashima in southern Japan. The 170-foot H-IIA rocket streaked aloft, carrying with it a Xilinx XQR4062XL, part of the XC4000XL series FPGA. This radiation-hardened FPGA is the core of the high-performance computing (HPC-I) payload incorporated in the Australian scientific mission satellite FedSat (Figure 1). The spacecraft was developed by the Cooperative Research Centre for Satellite Systems (CRCSS) in Australia. The HPC-I payload (Figure 2) was developed for CRCSS at the Queensland University of Technology.

FPGAs have flown in space before, but HPC-I is the first intentional use by CRCSS of reconfigurable computing technology (RCT) in the standard operation of a spaceborne computing system.

*Source: National Space  
Development Agency  
of Japan (NASDA)*

According to Anwar Dawood, CRCSS principal research scientist and program leader, “Traditional fixed computer hardware is designed to perform a diverse range of functions. This results in an efficient processing for some tasks and a slow processing for other tasks, especially the recursive and intensive computing jobs.” Furthermore, fixed computer hardware is inflexible and unable to adopt changes when newly created functions are required, he added.

Dawood pointed out that RCT offers the promising alternative of flexible hardware, which can be reconfigured – either by remote command or dynamically through its own internal operations – to specialize its function to an arbitrary range of demanding applications.

The Xilinx-based HPC-1 is the prototype with which Dawood and his team expect to establish the viability of RCT in spaceborne computing – including the tolerance of the hardware to the intense radiation of outer space.

### Second-Generation HPC-II

Dawood and the HPC team are now developing a second-generation HPC-II, which is built around the increased capacity and capability of a Xilinx FPGA. This second-generation project will emphasize critical space applications and onboard real-time data processing.

Dawood has initiated several application projects to exploit the efficiencies of space-based RCT, including:

- Disaster Detection and Monitoring System (DDMS) uses HPC technology for real-time or near-real-time image processing for detecting and monitoring natural disasters, such as forest fires and volcanic plumes.
- Satellite-Based Broadband Services (SBBS) utilizes HPC technology to provide multimedia communications, Internet access, and education services to both urban and rural areas.

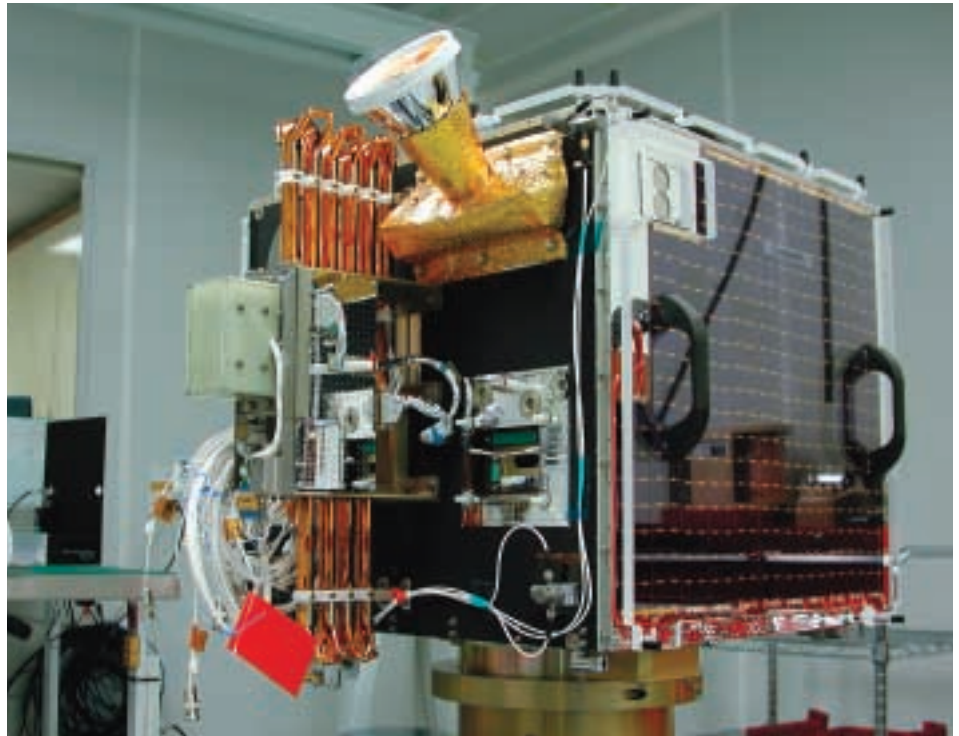


Figure 1 - FedSat spacecraft prior to launch (courtesy FedSat Project Team)

- Satellite Autonomous Navigation System (SANS) deploys HPC technology in conjunction with advanced GPS for onboard orbit determination for autonomous navigation.

### Fail-Safe Design

Avoiding catastrophic satellite failure is an equally compelling motive for remote reconfiguration. Entire satellite constellations have been lost through tiny failures in computing circuitry.



Figure 2 - HPC-1 payload (courtesy FedSat Project Team)

The reconfigurability of Xilinx FPGAs enables satellites to be rewired without having to be retrieved. This raises the promise of adaptable spacecraft that could be reconfigured remotely to work around problems – or even be able to repair themselves. Retired spacecraft might also be reconfigured for new purposes.

An example of a catastrophic satellite loss was described by Mark Long in a February 5 article for e-inSITE ([www.e-insite.net](http://www.e-insite.net)). In 1998, Hughes Space and Communications announced that electrical shorts were the most likely cause of a string of failures involving the spacecraft control processors (SCPs) onboard its 601 flight models. The SCPs controlled the satellites’ critical functions, including propulsion for attitude control, solar wing positioning, and antenna pointing.

Investigators finally traced the problem to a tin-plated latching relay that served as an on/off switch within the SCPs. Under certain combined conditions, the switch was shorted out by a tiny, crystalline growth less than the width of a human hair.

If the satellite operators had the ability to reconfigure their SCP systems on the fly, they might have found a way around the electrical shorts that led to the untimely demise of their satellite constellation.

### Radiation-Hardened

In the same article, Long pointed out another potential application for radiation-hardened Xilinx products in the onboard signal processing systems of advanced, next-generation satellite computer platforms.

Later this year, Hughes will launch the first of its Spaceway satellite platforms. These platforms will feature onboard processors

developed by TRW. The TRW processors have been designed to provide high-speed, onboard processing capabilities that will allow signals to pass directly between small aperture terminals without requiring the intervention of a gateway terminal.

The potent combination of onboard digital signal processing, packet switching, and spot-beam technologies is expected to enable single-hop connectivity throughout each of the system's many beam coverage areas.

Similar technology is also expected to fly on two Astrolink satellites being constructed by Liberty Media.

### Conclusion

The technology being developed by Xilinx for space-based applications promises to further enhance the capabilities of next-generation satellites to act as broadband routers in the sky.

For more information on Xilinx radiation-hardened FPGAs, visit [www.xilinx.com/products/military/radhardv.htm](http://www.xilinx.com/products/military/radhardv.htm).

To learn more about CRCSS, high-performance computing, and the FedSat satellite, go to [www.crcss.bee.qut.edu.au/comp.shtml](http://www.crcss.bee.qut.edu.au/comp.shtml) and [www.crcss.csiro.au](http://www.crcss.csiro.au). ❧

## Radiation-Tolerant FPGAs in Space

Space is a hostile environment. Streams of high-energy particles constantly bombard any exposed object. The Earth's atmosphere provides a strong, protective barrier that absorbs most of this radiation. Satellites, however, are located well outside this protective shield, and their electronic circuitry is especially vulnerable to damage that might lead to catastrophic failure.

According to Howard Bogrow, marketing manager for the Xilinx Aerospace and Defense Products Division, high-energy particles can cause a secondary reaction in untreated silicon-based chips that can cause their circuits to latch up. To address this problem, the XQR4000XL devices utilize a 0.35 micron epitaxial CMOS process that provides latch-up immunity, high total-ionizing dose (TID) tolerance, and low probability of single event upsets (SEUs) induced by natural radiation in satellite and other space environments.

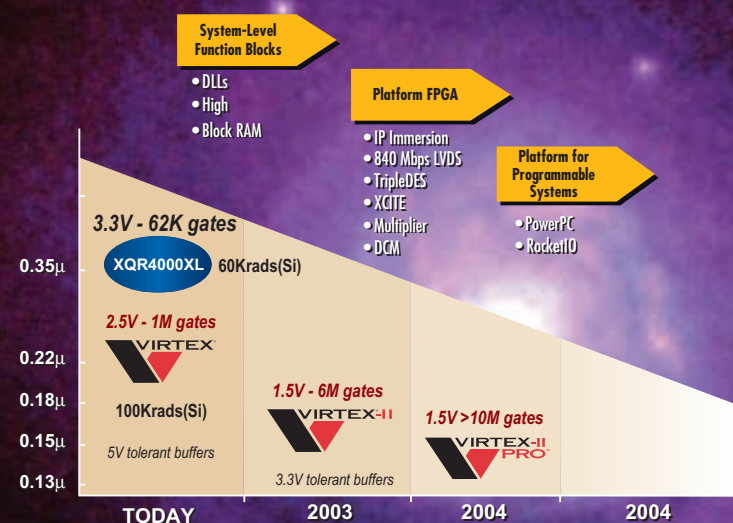


Figure 3 - Roadmap for radiation-tolerant FPGAs

Xilinx is currently shipping radiation-hardened versions of two device families:

- 4000XL with up to 130,000 gates, certified radiation tolerant to 60 Krad
- Virtex™ FPGAs with up to one million gates, certified to 100 Krad.

Later this year, a radiation tolerant line of QPro™ Virtex-II series FPGAs with up to six million gates will be released (Figure 3).

To determine the radiation tolerance of the company's products, Xilinx conducts extensive testing of their TID ([www.xilinx.com/prs\\_rls/radhard.html](http://www.xilinx.com/prs_rls/radhard.html)) and SEU characteristics ([www.support.xilinx.com/support/techxclusives/1000-techX35.htm](http://www.support.xilinx.com/support/techxclusives/1000-techX35.htm)).



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by Bill Okubo  
Solutions Marketing Group, Global Services  
Xilinx, Inc.  
bill.okubo@xilinx.com

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Figure 1 - MyXPA status display

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By making it easy to monitor the number of training credits purchased and compare them to credits used, MyXPA helps you proactively manage the renewal process and determine the proper level of participation in the XPA Program for next year.

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Xilinx participates in numerous trade shows and events throughout the year. These gatherings are excellent opportunities to meet our world-class silicon and software experts, ask questions, see demonstrations of new products and technologies, network with peers, and share success stories with Xilinx products. For more information and the most up-to-date schedule, visit [www.xilinx.com/events/](http://www.xilinx.com/events/).

## Worldwide Events Schedule

June 2-3	PCI-SIG Developers Conference	San Jose, CA
June 2-4	40th Design Automation Conference	Anaheim, CA
June 20	Programmable World Korea	Seoul, Korea
June 24	Programmable World Japan	Tokyo, Japan
July 21-25	Nuclear and Space Radiation Effects Conference	Monterey, CA
August 12	Programmable World China	Shanghai, China
August 14	Programmable World Taiwan	Hsinchu, Taiwan
September 9-11	Military and Aerospace Programmable Logic Devices (MAPLD) International Conference	Washington, D.C.
September 15-18	Intel Developer Forum	San Jose, CA
September 16-17	Embedded Systems Conference	Boston, MA

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# FUZZY LOGIC

In the Spring 2003 issue of *Xcell Journal*, we asked our readers to find nine “diamonds” on the pages of the magazine. The task was to note the page number where each diamond was found, add up the page numbers of each diamond, and send the sum to us with a good clean joke. The top five winners with the correct number and a joke (that we could print) would each win a HandSpring™ Visor Pro™ PDA.

For the record, the nine page numbers were 14, 17, 36, 45, 52, 61, 66, 96, and 110. The correct sum was 497.

And the winners are:

### Paul Newton

A guy gets shipwrecked. When he wakes up, he’s on a beach. The sand is purple.

He can’t believe it.

The sky is purple. He walks around a bit and sees that there is purple grass, purple birds, and purple fruit on the purple trees.

He’s shocked when he finds that his skin is starting to turn purple too ...

“Oh no!” he cries, “I think I’ve been marooned!”

### Mohammad Al-Taban

After explaining to a student with various lessons and examples, that:

$$\lim_{x \rightarrow 8} \frac{1}{x-8} = \infty$$

I tried to check if she really understood that, so I gave her a different example.

This was the result:

$$\lim_{x \rightarrow 5} \frac{1}{x-5} = \infty$$



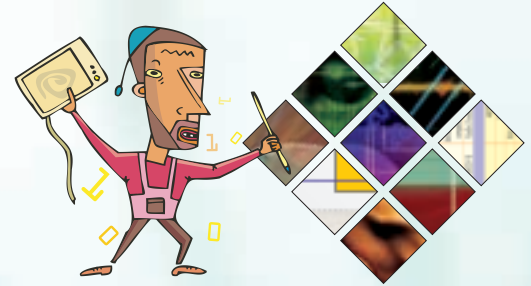
### David Kutz

Three engineering students were gathered together discussing the possible designers of the human body.

One said, “It was a mechanical engineer. Just look at all the joints.”

Another said, “No, it was an electrical engineer. The nervous system has many thousands of electrical connections.”

The last one said, “Actually it was a civil engineer. Who else would run a toxic waste pipeline through a recreational area?”



### Scott Campbell

Three engineers and three IRS agents are traveling by train to a conference. At the station, the three IRS agents each buy tickets and watch as the three engineers buy only a single ticket.

“How are three people going to travel on only one ticket?” asks an agent. “Watch and you’ll see,” answers an engineer.

They all board the train.

The IRS agents take their respective seats, but all three engineers cram into a restroom and close the door behind them.

Shortly after the train departed, the conductor comes around collecting tickets. He knocks on the restroom door and says, “Ticket, please.”

The door opens just a crack and a single arm emerges with a ticket in hand. The conductor takes it and moves on.

The agents saw this and agreed it was quite a clever idea. So after the conference, they decide to copy the engineers on the return trip and save some money.

When they get to the station, they buy a single ticket for the return trip. To their astonishment, the engineers do not buy a ticket at all.

“How are you going to travel without a ticket?” says one perplexed IRS agent.

“Watch and you will see,” answers an engineer. When they board the train, the three agents cram into a restroom and the three engineers cram into another one nearby.

The train departs. Shortly afterward, one of the engineers leaves his restroom and walks over to the restroom where the IRS agents are hiding.

He knocks on the door and says, “Ticket, please.”

### Keith Dellinger

How can you tell introverted engineers from extroverted engineers?

Introverted engineers look at their own shoes. Extroverted engineers look at your shoes.



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RTL Linter technology for Virtex-II series  
FPGAs (SpyGlass®)

### **Cadence Design Systems**

[www.cadence.com/feature/fpga\\_design.html](http://www.cadence.com/feature/fpga_design.html)

Virtex-II Pro MGT support for high-speed  
PCB design (SPECCTRAQuest®); NCSim  
family for FPGA design simulation; SPW  
for DSP data path development on FPGAs

### **Celoxica**

[www.celoxica.com](http://www.celoxica.com)

C-level design creation, compilation, and  
verification for Virtex-II and Virtex-II Pro  
FPGAs

### **Endeavor**

[www.endeav.com](http://www.endeav.com)

Co-verification for Virtex-II Pro  
(CoSimple™)

### **EVE**

[www.eve-team.com](http://www.eve-team.com)

RTL-level Simulator Accelerator (ZEBU)

### **Forte Design**

[www.fortedes.com](http://www.fortedes.com)

HLL compiler to RTL (Cynlib Tool Suite);  
timing specification and analysis tool  
(TimingDesigner)

### **Future Design Automation**

[www.future-da.com](http://www.future-da.com)

ANSI-C algorithms to RTL models  
(SystemCenter)

### **Hierarchical Design Inc. (HDI)**

[www.hierdesign.com](http://www.hierdesign.com)

Hierarchical floorplanning and analysis  
software for Virtex-II series FPGAs

### **Mentor Graphics**

[www.mentor.com](http://www.mentor.com)

Virtex-II Pro MGT support for high-speed  
PCB design (HyperLynx™, ICX™,  
Tau™); complete FPGA design flow using  
the ModelSim® family of simulators and  
Leonardo-Spectrum™/Precision® synthesis;  
Seamless® co-verification support for  
Virtex-II Pro

### **Novilit**

[www.novilit.com](http://www.novilit.com)

Design partitioning using ISE EDK  
(AnyWare) for Virtex-II series FPGAs

### **Product Acceleration Inc.**

[www.prodacc.com](http://www.prodacc.com)

FPGA symbol generation  
(LiveComponent™) and automated pin  
assignment optimization and PCB layer  
count control (DesignF/X)

### **Simucad**

[www.simucad.com](http://www.simucad.com)

Verilog Simulator for FPGAs (Silos)

### **Synopsys**

[www.synopsys.com](http://www.synopsys.com)

Virtex-II Pro multigigabit transceiver  
support for high-speed PCB design  
(HSPICE®); FPGA Compiler II™ RTL  
synthesis for Virtex series FPGAs;  
VCS™(MX)/Scirocco™(MX) simulators;  
Formality® formal verification, LEDA®  
RTL linter, and PrimeTime™ static  
timing analysis; high-level design using  
CoCentric™ System C Compiler and  
CoCentric System Studio

### **Synplicity**

[www.synplicity.com](http://www.synplicity.com)

RTL synthesis (Synplify®), debugger  
technology (Identify®), and physical  
synthesis (Amplify®) for all Xilinx FPGAs

### **Translogic**

[www.translogiccorp.com](http://www.translogiccorp.com)

FPGA symbol generation for fast PCB  
design iterations (FPGA Connector™)  
for Virtex-II series FPGAs

### **Verplex**

[www.verplex.com](http://www.verplex.com)

Formal verification technology for Virtex-II  
series FPGAs (Conformal™ LEC)

## Xilinx AllianceCORE Third-Party IP Providers and Products

### Alcatel Technology Licensing Group

[www.ind.alcatel.com/emacl/](http://www.ind.alcatel.com/emacl/)  
Ethernet media access controller cores  
United States

### Amphion Semiconductor Ltd.

[www.amphion.com](http://www.amphion.com)  
DSP, wireless communications, and multimedia cores  
United States

### Barco-Silex

[www.barco-silex.com](http://www.barco-silex.com)  
DSP cores, with a specialization in image-audio applications  
Belgium

### CAST, Inc.

[www.cast-inc.com](http://www.cast-inc.com)  
General purpose IP for processors, peripherals, multimedia, networking, encryption, serial communications, and bus interfaces  
United States

### Crossbow Technologies, Inc.

[www.crossbowip.com](http://www.crossbowip.com)  
System Interconnect IP for on-chip and chip-to-chip multiprocessing  
United States

### Deltatec S.A.

[www.deltatec.be/](http://www.deltatec.be/)  
IP and services for digital imaging, DSP, multimedia, PCI, and datacom  
Belgium

### Derivation Systems, Inc.

[www.derivation.com](http://www.derivation.com)  
IP cores for high-assurance hardware/software applications and embedded systems products; 32-bit Java processor core  
United States

### Digital Communications Technologies, Ltd.

[www.dctl.com](http://www.dctl.com)  
Embedded JAVA solutions  
United Kingdom

### Digital Core Design

[www.dcd.pl/](http://www.dcd.pl/)  
Microprocessor, microcontroller, floating point, and serial communication controller cores  
Poland

### Dolphin Integration

[www.dolphin.fr/](http://www.dolphin.fr/)  
Bus interface, processor, peripheral, and DSP cores; EDA software  
France

### Duma Video, Inc.

[www.dumavideo.com](http://www.dumavideo.com)  
Digital video, AES/EBU audio, MPEG and DCT cores; real-time MPEG-2 HD and SD compression  
United States

### elinfochips Pvt. Ltd.

[www.elinfochips.com](http://www.elinfochips.com)  
PCI, USB, 80186, multimedia, and wireless cores  
United States

### Eureka Technology

[www.eurekatech.com](http://www.eurekatech.com)  
Cores for SoC designs based on PCI and supporting PowerPC™, ARM, MIPS, ARC, and SH2/SH4 processors  
United States

### GV & Associates, Inc.

[www.gvassociates.com](http://www.gvassociates.com)  
Boards and expertise in DSP, processor, software, analog, and RF design  
United States

### iCoding Technology, Inc.

[www.icoding.com](http://www.icoding.com)  
Turbo Code-related error correction products including system design  
United States

### Intrinsyc, Inc.

[www.intrinsyc.com](http://www.intrinsyc.com)  
Single board embedded computers (FPGA + external processor); peripheral IP  
United Kingdom

### Loarant Corporation

[www.loarant.com](http://www.loarant.com)  
Proprietary 16-bit RISC CPU; embedded system design  
United States

### MEET Ltd.

[www.meet-electronics.com](http://www.meet-electronics.com)  
IP cores dedicated to industrial servomotor control  
Switzerland

### Memec Core

[www.memecore.com](http://www.memecore.com)  
Peripheral, bus interfaces, encryption, and communications cores  
United States

### ModelWare, Inc.

[www.modelware.com](http://www.modelware.com)  
Datacom/telecom cores including ATM, HDLC, POS, IMA, UTOPIA, and bridges  
United States

### NewLogic GmbH

[www.newlogic.at/](http://www.newlogic.at/)  
Cores for wireless applications including Bluetooth and 802.11  
Austria

### Paxonet Communications

[www.paxonet.com](http://www.paxonet.com)  
Solutions for interworking metro networking technologies to SONET  
United States

### Perigee, LLC

[www.perigeellc.com](http://www.perigeellc.com)  
DSP and image processing cores; embedded firmware, GUI, and application software development  
United States

### RealFast Operating Systems AB

[www.realfast.se/](http://www.realfast.se/)  
Real-time systems and RTOS; operating system cores  
Sweden

### SOC Solutions, L.L.C.

[www.socsolutions.com](http://www.socsolutions.com)  
Embedded uP and software; networking, wireless, audio, GPS, and handheld; peripheral cores  
United States

**SysOnChip, Inc.**

[www.syonchip.co.kr/](http://www.syonchip.co.kr/)

IP and products for CDMA Cellular/PCS/WLL modem, FEC, and Bluetooth  
Republic of South Korea

**Telecom Italia Lab S.p.A.**

[www.idosoc.com/soc/viplibrary/main.jsp?screen=viplibrary](http://www.idosoc.com/soc/viplibrary/main.jsp?screen=viplibrary)

Cores for ATM, optical networking, and switched digital video broadcast equipment  
Italy

**Tensilica, Inc.**

[www.tensilica.com](http://www.tensilica.com)

Configurable processors cores and development tools  
United States

**TurboConcept**

[www.turboconcept.com](http://www.turboconcept.com)

Turbo Code forward error correction solutions  
France

**Virtual IP Group**

[www.virtualipgroup.com](http://www.virtualipgroup.com)

Cores for microcontrollers, telecommunication, datacom, PC peripherals, and bus interface standards  
United States

**Wipro, Ltd.**

[www.wipro.com](http://www.wipro.com)

IP building blocks for technologies like IEEE 1394, USB, Bluetooth, and IEEE 802.11  
United States

**Xylon d.o.o.**

[www.logicbricks.com](http://www.logicbricks.com)

Human-machine interfaces and industrial communication controllers  
Croatia

**Zuken, Inc.**

[www.zuken.co.jp/soc/](http://www.zuken.co.jp/soc/)

PCI2.2, 10/100 Ethernet, and gigabit Ethernet cores  
Japan

## Reference Design Partners

The Xilinx Reference Design Alliance Program builds partnerships with industry-leading semiconductor manufacturers to develop reference designs for accelerating our customer's product and system time to market. The goal is to build a library of high-quality, multicomponent system-level reference designs in the areas of networking, communications, image and video processing, DSP, and emerging technologies and markets.

**Agere Systems**

[www.agere.com](http://www.agere.com)

**AMCC**

[www.amcc.com](http://www.amcc.com)

**Analog Devices**

[www.analog.com](http://www.analog.com)

**Bay Microsystems**

[www.baymicrosystems.com](http://www.baymicrosystems.com)

**BitBlitz Communications**

[www.bitblitz.com](http://www.bitblitz.com)

**Broadcom Corp.**

[www.broadcom.com](http://www.broadcom.com)

**Centillum**

[www.centillum.com](http://www.centillum.com)

**Congigine Corporation**

[www.cognigine.com](http://www.cognigine.com)

**Cypress Semiconductor**

[www.cypress.com](http://www.cypress.com)

**IBM Microelectronics**

[www.ibm.com/us/](http://www.ibm.com/us/)

**IDT**

[www.idt.com](http://www.idt.com)

**Ignis Optics**

[www.ignis-optics.com](http://www.ignis-optics.com)

**Infineon Technologies AG**

[www.infineontechnologies.com](http://www.infineontechnologies.com)

**Intel Corporation**

[developer.intel.com/design/network/](http://developer.intel.com/design/network/)

**Intrinsity**

[www.intrinsity.com/home.htm](http://www.intrinsity.com/home.htm)

**Micron Technology**

[www.micron.com](http://www.micron.com)

**Motorola**

[www.motorola.com](http://www.motorola.com)

**Octasic Semiconductor**

[www.octasic.com](http://www.octasic.com)

**PMC-Sierra Inc.**

[www.pmc-sierra.com/index.html](http://www.pmc-sierra.com/index.html)

**SiberCore Technologies**

[www.sibercore.com](http://www.sibercore.com)

**Teracross**

[www.teracross.com/~web/](http://www.teracross.com/~web/)

**Texas Instruments**

[www.ti.com](http://www.ti.com)

**TransSwitch Corporation**

[www.transwitch.com/index\\_flash.jsp](http://www.transwitch.com/index_flash.jsp)

**Velio Communications, Inc.**

[www.velio.com](http://www.velio.com)

**Vitesse**

[www.vitesse.com](http://www.vitesse.com)

**West Bay Semiconductor Inc.**

[www.westbaysemi.com](http://www.westbaysemi.com)

**ZettaCom**

[www.zettacom.com](http://www.zettacom.com)

**Xanoptix**

[www.xanoptix.com](http://www.xanoptix.com)



## XPERTS Partners

### 3T BV

[www.3T.nl](http://www.3T.nl)

Design services; measurement instruments; fail-safe controlling; medical equipment, communication, and computer peripherals

### Accent S.r.l.

[www.Accent.it/](http://www.Accent.it/)

Complex FPGAs; SoCs; PowerPCs; IP-platforms; software, PCB, and IC foundry services, from concept to silicon

### ADI Engineering

[www.adiengineering.com](http://www.adiengineering.com)

Reference designs; custom designs; design services focused on Intel IXA and XScale

### Advanced Electronic Designs, Inc.

[www.aedbozeman.com](http://www.aedbozeman.com)

Design services and manufacturing support; hardware and software design for embedded systems

### Advanced Principles Group, Inc.

[www.advancedprinciples.com](http://www.advancedprinciples.com)

Design services and consulting; software algorithm acceleration and application-specific computing systems

### Alpha Data

[www.alpha-data.com](http://www.alpha-data.com)

PCI/PMC/CPCI FPGA boards; embedded applications using HDL or System Generator methodologies

### AMIRIX Systems Inc.

[www.amirix.com](http://www.amirix.com)

Design services for electronic product realization; high-performance digital boards; programmable logic; embedded software

### Andraka Consulting Group, Inc.

[www.andraka.com](http://www.andraka.com)

Exclusively FPGAs for DSP since 1994; applications include radar, sonar, digital communications, imaging, and video

### Array Electronics

[www.array-electronics.de/](http://www.array-electronics.de/)

SoC/FPGA/PCB designs in telecom, industrial, and DSPs; concepts; verification; prototypes; cores

### Avnet Design Services

[www.ads.avnet.com](http://www.ads.avnet.com)

Embedded processing FPGA design services; Virtex-II Pro; high-speed SERDES; IP Core integration; timing closure; RLD RAM; RapidIO™

### Baranti Group Inc.

[www.baranti.com](http://www.baranti.com)

Award-winning design/manufacturing firm; expertise in digital video, FPGAs

### Barco Silex

[www.barco-silex.com](http://www.barco-silex.com)

Total solutions consisting of IP, FPGA, and board design

### Benchmark Electronics Inc.

[www.bench.com](http://www.bench.com)

EMS/JDM team; product design, support, introduction, and launch into volume production

### Birger Engineering, Inc.

[www.birger.com](http://www.birger.com)

Development of algorithms, electronics, and systems for digital imaging

### BitSim AB

[www.bitsim.com](http://www.bitsim.com)

Design services; DSP, video, 3G, and WLAN designs; high-speed prototyping boards

### Bottom Line Technologies Inc.

[www.bltninc.com](http://www.bltninc.com)

FPGA, product, and system design services; networking; data communications; telecommunications; video; PCI; signal processing; military; aerospace

### CES Design Services @ Siemens Program and System Engineering

[www.ces-designservices.com](http://www.ces-designservices.com)

Platform-oriented SoC/FPGA/PCB and firmware design in telecom, industrial, and video processing; customized solutions; concept; verification; prototypes

### CG-CoreEl Programmable Solutions P. Ltd.

[www.cg-coreel.com](http://www.cg-coreel.com)

Design services; telecom, networking, and Processor IP and designs; turnkey FPGA; RTL design/validation

### Chess iT/Embedded

[www.chess.nl/](http://www.chess.nl/)

Embedded hardware and software design of products and services at the chip, board, and system level

### Colorado Electronic Product Design, Inc.

[www.cepdinc.com](http://www.cepdinc.com)

Designing embedded systems with FPGAs for DSP; interfaces for medical, consumer, aerospace, and military

### Comit Systems, Inc.

[www.comit.com](http://www.comit.com)

High-end FPGA/SoC design services, including the integration of customer-developed and third-party IP

### ControlNet India Pvt Ltd.

[www.controlnetindia.com](http://www.controlnetindia.com)

ASIC/SoC Analog/RF FPGA design services; IP development; domains: Ethernet, IEEE1394, USB, security, PCI, WLAN, Infiniband

### Convergent Design LLC

[www.convergent-design.com](http://www.convergent-design.com)

Audio/video design for professional/consumer products

### DATA Respons ASA

[www.datarespons.com](http://www.datarespons.com)

Professional design and development services for embedded hardware/software solutions; FPGA/digital hardware application specialists

### Deltatec International Inc.

[www.deltatec.be/](http://www.deltatec.be/)

Design services; digital imaging applications; broadcast video, image processing and image synthesis

### Digicom Answers Pty Ltd.

[www.fpga.com.au/](http://www.fpga.com.au/)

Design services; experienced FPGA resources; design-on-demand; pre-design advice; reviews and problem solving

### Digital Design Corporation (DDC)

[www.digidescorp.com](http://www.digidescorp.com)

Design services and products; image processing; video; communications; DSP; audio; automotive; controls; interfaces

**Dillon Engineering, Inc.**

[www.dilloneng.com](http://www.dilloneng.com)

Design services; FPGA-based DSP algorithms; high-bandwidth, real-time digital signal and image processing applications

**DRS Tactical Systems West Inc. (formally Catalina Research)**

[www.catalinaresearch.com](http://www.catalinaresearch.com)

Design services; FPGAs for DSP, including the manufacturer of Virtex reconfigurable computing boards

**Eden Networks, Inc.**

[www.edennetworks.com](http://www.edennetworks.com)

Turnkey design services; telecom and networking designs (Ethernet, SONET, ATM, VoIP)

**Edgewood Technologies, LLC**

[www.edgewoodtechnologies.com](http://www.edgewoodtechnologies.com)

Design services; FPGAs for telecom, DSP, embedded processors

**Enea Data AB**

[www.enea.se/](http://www.enea.se/)

Telecommunication, data communication, DSP, RTOS, automotive, defense, high-reliability, and consumer electronics design

**Enterpoint Ltd.**

[www.enterpoint.co.uk/](http://www.enterpoint.co.uk/)

Design services; development boards; video, telecommunications, military, and high-speed design

**ESD Inc.**

[www.esdnet.com](http://www.esdnet.com)

Design services; FPGAs for embedded systems, software/hardware design, PCB layout

**Evatronix S.A.**

[www.evatronix.pl/](http://www.evatronix.pl/)

Design services; FPGA design (Virtex, Virtex-E, Spartan-II); embedded systems; SoCs and SoPCs designs

**Evermore Systems Inc.**

[www.evermoresystems.com](http://www.evermoresystems.com)

Design services; FPGA designs for communications, audio/video, wireless, and home networking

**ExaLinx**

[www.exalinx.com](http://www.exalinx.com)

Design services; ASIC emulation for high-speed communications and wireless applications; reference designs

**Fidus Systems Inc.**

[www.fidus.ca/](http://www.fidus.ca/)

Design services; FPGAs; communications; video; DSP; interface conversions; ASIC verification; hardware; PCB layout; software; SI/EMC

**First Principles Technology, Inc.**

[www.fptek.com](http://www.fptek.com)

Design/assembly/test services; FPGA + PCB + DSP/processor + system; imaging; video; test; satellite telecom; control

**Flexibilis Oy**

[www.flexibilis.com](http://www.flexibilis.com)

IP development; FPGA design services; Linux device drivers

**Flextronics Design**

[www.flextronics.com/design/](http://www.flextronics.com/design/)

Complete product design and development services for high-speed communications; reconfigurable computing; imaging; audio/video; military

**GDA Technologies, Inc.**

[www.gdatech.com](http://www.gdatech.com)

A leading services company focused on designing systems, SoC, ASIC, FPGA, and IP

**HCL Technologies**

[www.hcltech.com](http://www.hcltech.com)

High-speed board, ASIC, and FPGA design and verification services in avionics, medical, networking/telecom, consumer electronics

**Helion Technology Limited**

[www.heliontech.com](http://www.heliontech.com)

Design services and IP for FPGA with a focus on data security, wireless, and DSP

**IDERS Inc.**

[www.iders.ca/](http://www.iders.ca/)

Contract electronic engineering and EMS resource, providing complete product cycles ranging from specifications to production

**Image Technology Laboratory Corporation**

[www.gazogiken.co.jp/](http://www.gazogiken.co.jp/)

Design services; FPGAs for image processing; design tools: EDK, System Generator, and Forge

**INITEC AG**

[www.initec.ch/](http://www.initec.ch/)

Design services for system design; FPGA applications in telecommunication systems and medical electronics

**Innovative Computer Technology**

[ictconn.com](http://ictconn.com)

Digital, analog, Xilinx FPGA, and software design solutions for customers in a wide variety of industries throughout the United States

**iWave Systems Technologies Private Ltd.**

[www.iwavesystems.com](http://www.iwavesystems.com)

Embedded hardware and software design; board design; FPGA and ASIC development services

**Liewenthal Electronics Ltd.**

[www.liewenthal.ee/](http://www.liewenthal.ee/)

Embedded systems design services; development of software and hardware including Virtex and Spartan FPGAs

**Logic Product Development**

[www.logicpd.com](http://www.logicpd.com)

Full-service product development, including industrial design, mechanical, electrical, and software engineering

**M&M Consulting**

[hellman@mmcons.com](mailto:hellman@mmcons.com)

Design services; imaging; video, audio designs; high-density ASIC emulation

**Memondo Graphics**

[www.memondo.com](http://www.memondo.com)

Implementation of digital signal processing, communications, and image processing solutions and algorithms over Xilinx FPGAs

**Mikrokrets AS**

[www.mikrokrets.no/](http://www.mikrokrets.no/)

FPGA development comprising telecommunication, network communications, and embedded systems; PCB development

**Millogic Ltd.**

[www.millogic.com](http://www.millogic.com)

Design services and synthesizable cores; expertise in PCI, video, imaging, DSP, compression, ASIC verification, communications

**Milstar Inc.**

[www.Milstar.co.il/](http://www.Milstar.co.il/)

Design services and manufacturers (industrial and military specs); DSP; communication; video; audio; high-speed boards

**Misarc srl - Agrate**

[www.misarc.com](http://www.misarc.com)

Design services and manufacturers; telecommunications, SoC development, and test equipment boards using FPGA solutions

**Multi Video Designs**

[www.mvd-fpga.com](http://www.mvd-fpga.com)

Design services; DSP for video, telecommunications; SoC with Virtex-II/Pro and Spartan (PowerPC/MicroBlaze™); Xilinx training

**Multiple Access Communications Ltd.**

[www.macltd.com](http://www.macltd.com)

Design services; products and consultancy; DSP for wireless communications

**Nallatech**

[www.nallatech.com](http://www.nallatech.com)

Embedded reconfigurable computers for high-performance applications in DSP, imaging, and defense; Xilinx Diamond XPERTS

**NetQuest Corporation**

[www.netquestcorp.com](http://www.netquestcorp.com)

Turnkey engineering design and production services in advanced high-speed embedded communications

**North Pole Engineering Inc.**

[www.northpoleengineering.com](http://www.northpoleengineering.com)

Hardware and software design services for FPGA, ASIC, and embedded systems

**Northwest Logic**

[www.nwlogic.com](http://www.nwlogic.com)

PCI, PCI-X, and SDRAM controller IP; high-end FPGA design services

**NovTech Engineering**

[www.novtech.com](http://www.novtech.com)

Board-level and IP cores; turnkey design services; imaging; communication; PCI cores; encryption

**NUVATION**

[www.nuvation.com](http://www.nuvation.com)

Design services; imaging and communications for defense/security, medical, consumer, and datacom/telecom markets

**Plextek Ltd.**

[www.plextek.com](http://www.plextek.com)

Design services; FPGA, DSP, radio, microwave, and microprocessor technologies for defense and communications

**POLAR-Design**

[www.polar-design.de/](http://www.polar-design.de/)

High-end FPGA design for telecom, networking, and DSP applications

**Polybus Systems Corporation**

[www.polybus.com](http://www.polybus.com)

Test patterns; customizable in-system FPGA test patterns; design services; networking and communications

**Presco, Inc.**

[www.prescoinc.com](http://www.prescoinc.com)

Twenty-five years of experience in custom electronics design/manufacturing for high-performance image processing, data communications, inkjet

**Productivity Engineering GmbH**

[www.pe-gmbh.com](http://www.pe-gmbh.com)

Design services; PCI design; microprocessor cores; obsolete component replacements; ASIC prototyping

**Programall Technologies Inc.**

[www.ProgramallTechnologies.com](http://www.ProgramallTechnologies.com)

Design services; embedded systems targeting Virtex, Spartan, Virtex-II, and Virtex-II Pro FPGAs

**R&D Consulting**

972-9-7673074

FPGA development; video; imaging; graphics; DSP; communications

**Rapid Prototypes, Inc.**

[www.FPGA.com](http://www.FPGA.com)

Design services; high-performance reconfigurable FPGA applications requiring maximum speed or density using physical design principles

**RDLABS**

[www.rdlabs.com](http://www.rdlabs.com)

FPGA/ASIC design; wireless communications; 802.11b/a IP cores; Matlab, Sysgen, ModelSim; instruments HP1661A, HP8594E, HP54520A

**RightHand Technologies, Inc.**

[www.righthandtech.com](http://www.righthandtech.com)

Design services; Virtex-II Pro FPGAs, boards, and software for video gaming, storage, medical, wireless

**Rising Edge Technology Inc.**

[www.risingedgetech.com](http://www.risingedgetech.com)

Complete design solutions from the ground up; FPGA interface designs

**Riverside Machines Ltd.**

[www.riverside-machines.com](http://www.riverside-machines.com)

Design services and project management; DSP, wireless, network, and processor development; Verilog, VHDL, SystemC, Specman

**Roke Manor Research**

[www.roke.co.uk/](http://www.roke.co.uk/)

Design services; IP, ATM, DSP, imaging, radar, and control solutions for FPGAs

**Roman-Jones, Inc.**

[www.roman-jones.com](http://www.roman-jones.com)

Design services; FPGAs for embedded microprocessors; PCI; DSP; low-cost 8051 softcore

**Sapphire Computers, Inc.**

[drudolf@voyager.net](mailto:drudolf@voyager.net)

Engineering design consulting; high-speed digital and FPGA design

**Siemens AG, Electronic Design House**

[www.eda-services.com](http://www.eda-services.com)

Design services; system-on-chip; ASICs; FPGAs; IPs; DSPs; boards; EMC; embedded software; prototypes

**Silicon & Software Systems Ltd. (S3)**

[www.s3group.com](http://www.s3group.com)

World-class electronics design company uniquely combining IC, FPGA, software, and hardware design expertise

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### 1.8V CORE VOLTAGE CPLD COMPETITIVE CHART

Manufacturer	Xilinx	Lattice		Altera
Device Family	CoolRunner-II	ispMACH4000C	ispMACH4000Z	None
Standby Current	12 µA	1,800 µA	20 µA	N/A
Internal Performance	500 MHz	400 MHz	265 MHz	N/A
Clock Divider/Doubler	YES/YES	NO/NO	NO/NO	N/A
Max Density (Macrocells)	512	512	128	N/A
I/O Standards Support	LVTTTL, LVCMOS, HSTL, SSTL	LVTTTL, LVCMOS	LVTTTL, LVCMOS	N/A
I/O Banks (max)	4	2	2	N/A



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## Introduction

The 1.2V Spartan™-3 family of Field Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The eight-member family offers densities ranging from 50,000 to five million system gates, as shown in [Table 1](#).

The Spartan-3 family builds on the success of the earlier Spartan-II family by increasing the amount of logic resources, the capacity of internal RAM, the total number of I/Os, and the overall level of performance as well as by improving clock management functions. Numerous enhancements derive from state-of-the-art Virtex™-II technology. These Spartan-3 enhancements, combined with advanced process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3 FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

The Spartan-3 family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

## Features

- Very low cost, high-performance logic solution for high-volume, consumer-oriented applications
- Densities as high as 74K logic cells
- 325 MHz system clock rate
- Three separate power supplies for the core (1.2V), I/Os (1.2V to 3.3V), and special functions (2.5V)
- SelectIO™ signaling
  - Up to 784 I/O pins
  - 622 Mbps data transfer rate per I/O
  - Seventeen single-ended signal standards
  - Six differential signal standards including LVDS
  - Termination by Digitally Controlled Impedance
  - Signal swing ranging from 1.14V to 3.45V
  - Double Data Rate (DDR) support
- Logic resources
  - Abundant, flexible logic cells with registers
  - Wide multiplexers
  - Fast look-ahead carry logic
  - Dedicated 18 x 18 multipliers
  - JTAG logic compatible with IEEE 1149.1/1532 standards
- SelectRAM™ hierarchical memory
  - Up to 1,872 Kb of total block RAM
  - Up to 520 Kb of total distributed RAM
- Digital Clock Manager (up to four DCMs)
  - Clock skew elimination
  - Frequency synthesis
  - High-resolution phase shifting
- Eight global clock lines and abundant routing
- Fully supported by Xilinx ISE development system
  - Synthesis, mapping, placement and routing

Table 1 – Summary of Spartan-3 FPGA Attributes

Device	System Gates	Logic Cells	CLB Array (One CLB = Four Slices)			Distributed RAM (bits <sup>1</sup> )	Block RAM (bits <sup>1</sup> )	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs						
XC3S50	50K	1,728	16	12	192	12K	0	0	0	124	56
XC3S200	200K	4,320	24	20	480	30K	216K	12	4	173	76
XC3S400	400K	8,064	32	28	896	56K	288K	16	4	264	116
XC3S1000	1M	17,280	48	40	1,920	120K	432K	24	4	391	175
XC3S1500	1.5M	29,952	64	52	3,328	208K	576K	32	4	487	221
XC3S2000	2M	46,080	80	64	5,120	320K	720K	40	4	565	270
XC3S4000	4M	62,208	96	72	6,912	432K	1,728K	96	4	712	312
XC3S5000	5M	74,880	104	80	8,320	520K	1,872K	104	4	784	344

**Notes:**

<sup>1</sup>By convention, one Kb is equivalent to 1,024 bits.

## Architectural Overview

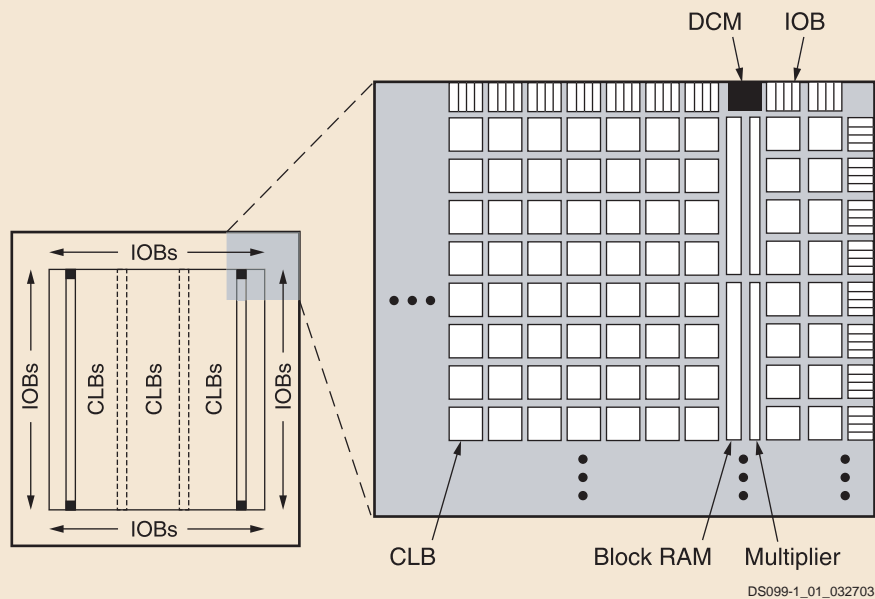
The Spartan-3 family architecture consists of five fundamental programmable functional elements:

- Configurable Logic Blocks (CLBs) contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Input/Output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus three-state operation. Twenty-three different signal standards, including six high-performance differential standards, are available as shown in [Table 2](#). Double Data Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.
- Block RAM provides data storage in the form of 18 Kb dual-port blocks.
- Multiplier blocks accept two 18-bit binary numbers as inputs and calculate the product.

- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.

These elements are organized as shown in [Figure 1](#). A ring of IOBs surrounds a regular array of CLBs. Those devices ranging from the XC3S200 to the XC3S2000 have two columns of block RAM embedded in the array. The XC3S4000 and XC3S5000 devices have four RAM columns. Each column is made up of several 18 Kb RAM blocks; each block is associated with a dedicated multiplier. The DCMs are positioned at the ends of the outer block RAM columns, making up a total of four. The XC3S50, the lowest cost member of the family, has neither block RAM, nor dedicated multipliers, nor DCMs.

The Spartan-3 family features a rich network of traces and switches that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



### Notes:

1. The two additional block RAM columns of the XC3S4000 and XC3S5000 devices are shown with dashed lines. The XC3S50 device does not have any block RAM, multipliers, or DCMs.

Figure 1 – Spartan-3 Family Architecture

## Configuration

Spartan-3 FPGAs are programmed by loading configuration data into robust static memory cells that collectively control all functional elements and routing resources. Before powering on the FPGA, configuration data is stored externally in a PROM or some other nonvolatile medium either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes: Master Parallel, Slave Parallel, Master Serial, Slave Serial and Boundary Scan (JTAG). The Master and Slave Parallel modes use an 8-bit wide SelectMAP™ Port.

The recommended memory for storing the configuration data is the low-cost Xilinx Platform Flash PROM family, which includes XCF00S PROMs for serial configuration and XCF00P PROMs for parallel configuration.

## I/O Capabilities

The SelectIO feature of Spartan-3 devices supports 17 single-ended standards and six differential standards as listed in [Table 2](#). [Table 3](#) shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Table 2 – Signal Standards Supported by the Spartan-3 Family

Standard Category	Description	V <sub>CCO</sub> (V)	Class	Symbol
<b>Single-Ended</b>				
GTL	Gunning Transceiver Logic	N/A	Terminated	GTL
			Plus	GTL <sub>P</sub>
HSTL	High-Speed Transceiver Logic	1.5	I	HSTL_I
			III	HSTL_III
		1.8	I	HSTL_I_18
			II	HSTL_II_18
LVCMOS	Low-Voltage CMOS	1.2	N/A	LVCMOS12
		1.5	N/A	LVCMOS15
		1.8	N/A	LVCMOS18
		2.5	N/A	LVCMOS25
		3.3	N/A	LVCMOS33
LVTTL	Low-Voltage Transistor/Transistor Logic	3.3	N/A	LVTTL
PCI	Peripheral Component Interconnect	3.0	33 MHz	PCI33_3
SSTL	Stub Series Terminated Logic	1.8	N/A	SSTL18_I
		2.5	I	SSTL2_I
			II	SSTL2_II
<b>Differential</b>				
LDT	Lightning Data Transport (HyperTransport™)	2.5	N/A	LDT_25
LVDS	Low-Voltage Differential Signaling		Standard	LVDS_25
			Bus	BLVDS_25
			Extended Mode	LVDSEXT_25
		Ultra	ULVDS_25	
RSDS	Reduced-Swing Differential Signaling	2.5	N/A	RSDS_25



Table 3 – Spartan-3 User I/O Chart

Device	Available User I/Os and Differential (Diff) I/O Pairs															
	VQ100		TQ144		PQ208		FT256		FG456		FG676		FG900		FG1156	
	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XC3S50	63	TBD	97	46	124	56	-	-	-	-	-	-	-	-	-	-
XC3S200	63	TBD	97	46	141	62	173	76	-	-	-	-	-	-	-	-
XC3S400	-	-	-	-	141	62	173	76	264	116	-	-	-	-	-	-
XC3S1000	-	-	-	-	-	-	173	76	333	149	391	175	-	-	-	-
XC3S1500	-	-	-	-	-	-	-	-	333	149	487	221	-	-	-	-
XC3S2000	-	-	-	-	-	-	-	-	-	-	489	221	565	270	-	-
XC3S4000	-	-	-	-	-	-	-	-	-	-	-	-	633	300	712	312
XC3S5000	-	-	-	-	-	-	-	-	-	-	-	-	633	300	784	344

**Notes:**

1. All device options listed in a given package column are pin-compatible.

## Product Ordering and Availability

Table 4 shows all valid device ordering combinations of device density, speed grade, package, and temperature

range parameters for the Spartan-3 family as well as the availability status of those combinations.

Table 4 – Spartan-3 Device Availability

Device	Package Type:	VQFP	TQFP	PQFP	FTBGA	FBGA			
	No. of Pins:	100	144	208	256	456	676	900	1156
	Code:	VQ100	TQ144	PQ208	FT256	FG456	FG676	FG900	FG1156
	Speed Grade								
XC3S50	Commercial devices offered in the -4 and -5 speed grades; industrial devices offered in the -4 speed grade.	(C, I)	(C, I)	(C, I)	-	-	-	-	-
XC3S200		(C, I)	(C, I)	(C, I)	(C, I)	-	-	-	-
XC3S400		-	-	(C, I)	(C, I)	(C, I)	-	-	-
XC3S1000		-	-	-	(C, I)	(C, I)	(C, I)	-	-
XC3S1500		-	-	-	-	(C, I)	(C, I)	-	-
XC3S2000		-	-	-	-	-	(C, I)	(C, I)	-
XC3S4000		-	-	-	-	-	-	(C, I)	(C, I)
XC3S5000		-	-	-	-	-	-	(C, I)	(C, I)

**Notes:**

1. C = Commercial:  $T_j = 0^\circ$  to  $+85^\circ$  C; I = Industrial:  $T_j = -40^\circ$  C to  $+100^\circ$  C.
2. Parentheses indicate that a given product is not yet released. Contact sales for availability information.







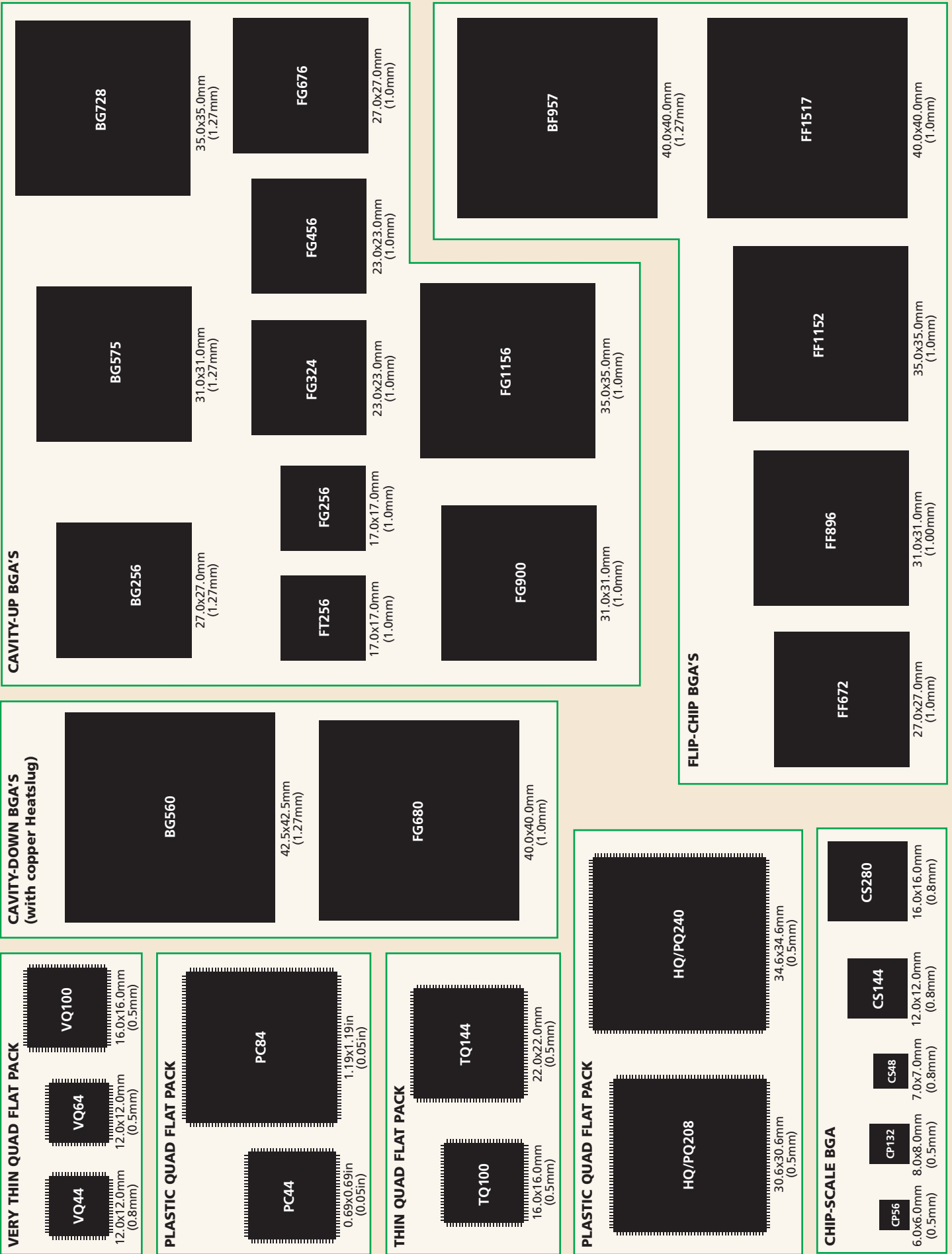
# Xilinx IQ Solutions



Part Number	Speed	Package	Voltage	Description
<b>XC9500XL CPLD</b>				
XC9536XL	10 ns/100 MHz	VQ44, VQ64	3.3V	36 Macrocells (800 Gates), ISP, JTAG, Bus Hold & I/P Hysteresis
XC9572XL	10 ns/100 MHz	VQ64, TQ100	3.3V	72 Macrocells (1,600 Gates), ISP, JTAG, Bus Hold & I/P Hysteresis
<b>CoolRunner XPLA3</b>				
XCR3032XL	10 ns/100 MHz	VQ44	3.3V	32 Macrocells (800 Gates), Low Power, Slew Rate Control, ISP & JTAG
XCR3064XL	10 ns/100 MHz	VQ44, VQ100	3.3V	64 Macrocells (1,600 Gates), Low Power, Slew Rate Control, ISP & JTAG
XCR3128XL	10 ns/100 MHz	VQ100, TQ144	3.3V	128 Macrocells (3,200 Gates), Low Power, Slew Rate Control, ISP & JTAG
XCR3256XL	10 ns/100 MHz	TQ144, PQ208	3.3V	256 Macrocells (6,400 Gates), Low Power, Slew Rate Control, ISP & JTAG
XCR3384XL	10 ns/100 MHz	PQ208	3.3V	384 Macrocells (9,600 Gates), Low Power, Slew Rate Control, ISP & JTAG
XCR3512XL	10 ns/100 MHz	PQ208	3.3V	512 Macrocells (12,800 Gates), Low Power, Slew Rate Control, ISP & JTAG
<b>CoolRunner-II</b>				
XC2C32	6 ns/145 MHz	VQ44	1.8V	32 Macrocells (800 Gates), 6 I/O Standards, Slew Rate Control, Clock Doubler, Bus Hold, I/P Hysteresis. Ultra low power.
XC2C64	7.5 ns/127 MHz	VQ44, VQ100	1.8V	64 Macrocells (1,600 Gates), 6 I/O Standards, Slew Rate Control, Clock Doubler, Bus Hold, I/P Hysteresis. Ultra low power.
XC2C128	7.5 ns/127 MHz	VQ44, VQ100	1.8V	128 Macrocells (3,200 Gates), 9 I/O Standards, Slew Rate Control, Clock Doubler, Clcok Divider, CoolClock, DataGate, Bus Hold, I/P Hysteresis. Ultra low power.
XC2C256	7.5 ns/127 MHz	VQ100, TQ144	1.8V	256 Macrocells (6,400 Gates), 9 I/O Standards, Slew Rate Control, Clock Doubler, Clcok Divider, CoolClock, DataGate, Bus Hold, I/P Hysteresis. Ultra low power.
XC2C384	10 ns/100 MHz	TQ144, PQ208	1.8V	384 Macrocells (9,600 Gates), 9 I/O Standards, Slew Rate Control, Clock Doubler, Clcok Divider, CoolClock, DataGate, Bus Hold, I/P Hysteresis. Ultra low power.
XC2C512	10 ns/100 MHz	PQ208	1.8V	512 Macrocells (12,800 Gates), 9 I/O Standards, Slew Rate Control, Clock Doubler, Clcok Divider, CoolClock, DataGate, Bus Hold, I/P Hysteresis. Ultra low power.

Part Number	Speed Grade	Package	Voltage	Description
<b>Spartan-XL</b>				
XCS05XL	-4	VQ100	3.3V	Low cost FPGA with power down pin, 5V tol I/O, 5,000 Gate, 238 logic cells, 100 CLBs.
XCS10XL	-4	VQ100	3.3V	Low cost FPGA with power down pin, 5V tol I/O, 10,000 Gate, 466 logic cells, 196 CLBs.
XCS20XL	-4	TQ144, PQ208	3.3V	Low cost FPGA with power down pin, 5V tol I/O, 20,000 Gate, 950 logic cells, 400 CLBs.
XCS30XL	-4	TQ144, PQ208	3.3V	Low cost FPGA with power down pin, 5V tol I/O, 30,000 Gate, 1,368 logic cells, 576 CLBs.
XCS40XL	-4	PQ208, BG256	3.3V	Low cost FPGA with power down pin, 5V tol I/O, 40,000 Gate, 1,862 logic cells, 784 CLBs.
<b>Spartan-II</b>				
XC2S15	-5	TQ144	2.5V	High volume FPGA, on-chip RAM, 16 I/O standards, 15,000 Gate, 432 logic cells, 96 CLBs, 4 block RAM blocks, 4 DLLs.
XC2S30	-5	TQ144, PQ208	2.5V	High volume FPGA, on-chip RAM, 16 I/O standards, 30,000 Gate, 972 logic cells, 216 CLBs, 6 block RAM blocks, 4 DLLs.
XC2S50	-5	TQ144, PQ208, FG256	2.5V	High volume FPGA, on-chip RAM, 16 I/O standards, 50,000 Gate, 1,728 logic cells, 384 CLBs, 8 block RAM blocks, 4 DLLs.
XC2S100	-5	TQ144, PQ208, FG256	2.5V	High volume FPGA, on-chip RAM, 16 I/O standards, 100,000 Gate, 2,700 logic cells, 600 CLBs, 10 block RAM blocks, 4 DLLs.
XC2S150	-5	PQ208, FG256	2.5V	High volume FPGA, on-chip RAM, 16 I/O standards, 150,000 Gate, 3,888 logic cells, 864 CLBs, 12 block RAM blocks, 4 DLLs.
XC2S200	-5	PQ208, FG456	2.5V	High volume FPGA, on-chip RAM, 16 I/O standards, 200,000 Gate, 5,292 logic cells, 1,176 CLBs, 14 block RAM blocks, 4 DLLs.
<b>Spartan-IIIE</b>				
XC2S50E	-6	TQ144, PQ208, FT256	1.8V	High volume FPGA, on-chip RAM, 19 I/O standards, 50,000 Gate, 1,728 logic cells, 384 CLBs, 8 block RAM blocks, 4 DLLs.
XC2S100E	-6	TQ144, PQ208, FT256	1.8V	High volume FPGA, on-chip RAM, 19 I/O standards, 100,000 Gate, 2,700 logic cells, 600 CLBs, 10 block RAM blocks, 4 DLLs.
XC2S150E	-6	PQ208, FT256	1.8V	High volume FPGA, on-chip RAM, 19 I/O standards, 150,000 Gate, 3,888 logic cells, 864 CLBs, 12 block RAM blocks, 4 DLLs.
XC2S200E	-6	PQ208, FT256	1.8V	High volume FPGA, on-chip RAM, 19 I/O standards, 200,000 Gate, 5,292 logic cells, 1,176 CLBs, 14 block RAM blocks, 4 DLLs.
XC2S300E	-6	PQ208, FG456	1.8V	High volume FPGA, on-chip RAM, 19 I/O standards, 300,000 Gate, 6,912 logic cells, 1,536 CLBs, 16 block RAM blocks, 4 DLLs.
XC2S400E	-6	FT256, FG456, FG676	1.8V	High volume FPGA, on-chip RAM, 19 I/O standards, 400,000 Gate, 10,800 logic cells, 2,400 CLBs, 40 block RAM blocks, 4 DLLs.
XC2S600E	-6	FG456, FG676	1.8V	High volume FPGA, on-chip RAM, 19 I/O standards, 600,000 Gate, 10,800 logic cells, 3,456 CLBs, 72block RAM blocks, 4DLLs.









# Xilinx Software

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Devices	Virtex™ Series	<b>Virtex-E:</b> V50E – V300E <b>Virtex-II:</b> 2V40 – 2V250 <b>Virtex-II Pro:</b> 2VP2	<b>Virtex:</b> V50 – V300 <b>Virtex-E:</b> V50E – V300E <b>Virtex-II:</b> 2V40 – 2V250 <b>Virtex-II Pro:</b> 2VP2	ALL	ALL
	Spartan™ Series	<b>Spartan-II/IIE:</b> ALL (except XC2S400E and XC2S600E) <b>Spartan-3:</b> 3S50	<b>Spartan-II/IIE:</b> ALL <b>Spartan-3:</b> 3S50 and 3S200	<b>Spartan-II/IIE:</b> ALL <b>Spartan-3:</b> ALL	<b>Spartan-II/IIE:</b> ALL <b>Spartan-3:</b> ALL
	CoolRunner™ XPLA3 / CoolRunner-II XC9500™ Series	ALL ALL	ALL ALL	ALL ALL	ALL ALL
Services	Educational Services	Yes	Yes	Yes	Yes
	Design Services	Sold as an Option	Sold as an Option	Sold as an Option	Sold as an Option
Design Entry	Support Services	Web Only	Yes	Yes	Yes
	Schematic Editor	Yes	Yes	PC Only	No
	HDL Editor	Yes	Yes	Yes	Yes
	State Diagram Editor	Yes	Yes	PC Only	No
	CORE Generator System	No	Yes	Yes	Yes
	PACE (Pinout and Area Constraint Editor)	Yes	Yes	Yes	Yes
	Architecture Wizards	Yes	Yes	Yes	Yes
	DCM – Digital Clock Management MGT – Multi-Gigabit Transceivers				
	3rd Party RTL Checker Support	Yes	Yes	Yes	Yes
	Xilinx System Generator for DSP	No	Sold as an Option	Sold as an Option	Sold as an Option
Embedded System Design	GNU Embedded Tools GCC – GNU Compiler GDB – GNU Software Debugger	No	Yes (Available with optional EDK)	Yes (Available with optional EDK)	Yes (Available with optional EDK)
	WindRiver Xilinx Edition Development Tools Diab C/C++ Compiler SingleStep Debugger visionPROBE II target connection	No	Sold as an Option	Sold as an Option	Sold as an Option
Synthesis	Xilinx Synthesis Technology (XST)	Yes	Yes	Yes	No
	Synplicity Synplify/Pro	Integrated Interface	Integrated Interface	Integrated Interface (PC Only)	Integrated Interface (PC Only)
	Synplicity Amplify Physical Synthesis Support	Yes	Yes	Yes	Yes
	Leonardo Spectrum	Integrated Interface	Integrated Interface	Integrated Interface	Integrated Interface
	Synopsys FPGA Compiler II	EDIF Interface	EDIF Interface	EDIF Interface	EDIF Interface
	ABEL	CPLD	CPLD	CPLD (PC Only)	No
Implementation	FloorPlanner	Yes	Yes	Yes	Yes
	Constraints Editor	Yes	Yes	Yes	Yes
	Timing Driven Place & Route	Yes	Yes	Yes	Yes
	Modular Design	Yes	Yes	Yes	Yes
	Timing Improvement Wizard	Yes	Yes	Yes	Yes
	iMPACT	Yes	Yes	Yes	Yes
Programming	System ACE Configuration Manager	Yes	Yes	Yes	Yes
Board Level Integration	IBIS Models	Yes	Yes	Yes	Yes
	STAMP Models	Yes	Yes	Yes	Yes
	LMG SmartModels	Yes	Yes	Yes	Yes
	HSPICE Models*	Yes	Yes	Yes	Yes
Verification	HDL Benchertm	Yes	Yes	PC Only	No
	ModelSim® Xilinx Edition (MXE II)	ModelSim XE II Starter**	ModelSim XE II Starter**	ModelSim XE II Starter**	ModelSim XE II Starter**
	Static Timing Analyzer	Yes	Yes	Yes	Yes
	ChipScope Pro	No	Sold as an Option	Sold as an Option	Sold as an Option
	FPGA Editor with Probe	No	Yes	Yes	Yes
	ChipViewer	Yes	Yes	Yes	Yes
	XPower (Power Analysis)	Yes	Yes	Yes	Yes
	3rd Party Equivalency Checking Support	Yes	Yes	Yes	Yes
	SMARTModels for PPC and Rocket I/O	No	Yes	Yes	Yes
	3rd Party Simulator Support	Yes	Yes	Yes	Yes
Platforms		PC (MS Windows 2000/MS Windows XP)	PC Only (MS Windows 2000/MS Windows XP)	PC (MS Windows 2000/MS Windows XP/Sun Solaris, Linux)	PC (MS Windows 2000/MS Windows XP/Sun Solaris, Linux)
IP/CORE	For more information on the complete list of Xilinx IP products, visit the Xilinx IP Center at <a href="http://www.xilinx.com/ipcenter">http://www.xilinx.com/ipcenter</a>				

\* HSPICE Models available at the Xilinx Design Tools Center at [www.xilinx.com/ise](http://www.xilinx.com/ise). \*\* MXE II supports the simulation of designs up to 1 million system gates and is sold as an option.

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# Xilinx Global Services

## Xilinx Global Services

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[http://support.xilinx.com/support/gsd/xpa\\_program.htm](http://support.xilinx.com/support/gsd/xpa_program.htm)

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Part Number	Product Description	Duration	Availability
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		<b>hours</b>	
FPGA13000-5-ILT	Fundamentals of FPGA Design	8	Now
FPGA23000-5-ILT	Designing for Performance	16	Now
FPGA33000-5-ILT	Advanced FPGA Implementation	16	Now
LANG11000-5-ILT	Introduction to VHDL	24	Now
LANG21000-5-ILT	Advanced VHDL	16	Now
LANG12000-5-ILT	Introduction to Verilog	24	Now
PCI8000-4-ILT	PCI CORE Basics	8	Now
PCI28000-4-ILT	Designing a PCI System	16	Now
ASIC25000-5-ILT	Designing for Performance for the ASIC User	24	Now
DSP2000-3-ILT	DSP Implementation Techniques for Xilinx FPGAs	24	Now
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RIO22000-5-ILT	Designing with RocketIO MGT	16	Now
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EMBD-21000-5-ILT	Embedded Systems Development	16	Now
<b>Platinum Technical Service</b>			
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SC-PLAT-SITE-150	Platinum Technical Service site license for 101-150 customers	N/A	Now
<b>Titanium Technical Service</b>			
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PS-TEC-SERV-JP	Titanium Technical Service (minimum 8 hours) Japan	N/A	Now
<b>Design Services</b>			
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<b>Xilinx Productivity Advantage</b>			
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DS-XPA25K	Custom XPA for \$10,0001 – \$25,000	N/A	Now
DS-XPA	Custom XPA for \$25,001 – \$100,000	N/A	Now
DS-XPA-10K-INT	Custom XPA (International) for \$0 – \$10,000	N/A	Now
DS-XPA-25K-INT	Custom XPA (International) for \$10,0001 – \$25,000	N/A	Now
DS-XPA-INT	Custom XPA (International) for \$25,001 – \$100,000	N/A	Now
DS-ISE-ALI-XPA	XPA Seat, ISE Alliance	N/A	Now
DS-ISE-FND-XPA	XPA Seat, ISE Foundation	N/A	Now
<b>Promotion Packages</b>			
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