Signetics

Logic Products

74LS1801
Bit Stream Manager

Encoder/Decoder
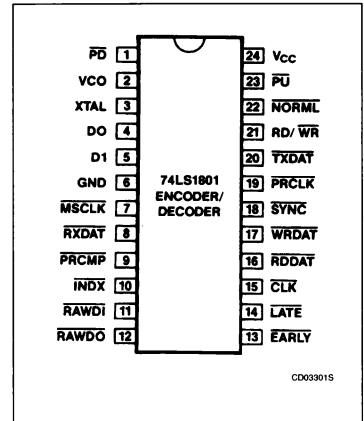*Product Specification*

DESCRIPTION
The 74LS1801 Encoder/Decoder (Figure 1) supports disk drive and data communications devices that require fast and reliable data separation capabilities. Although ideally suited for use with the 74LS1802 Serializer/Deserializer, the 74LS1801 is a flexible device which can be implemented in a variety of design applications.

Encoding is possible in FM, MFM, or Differential Manchester formats, making the 74LS1801 invaluable in designs requiring single density disk recording, double density disk recording, or in data communications applications. Included on-chip is a phase-comparator which can be bypassed; this feature is particularly useful in applications that use a complete external phase lock loop.
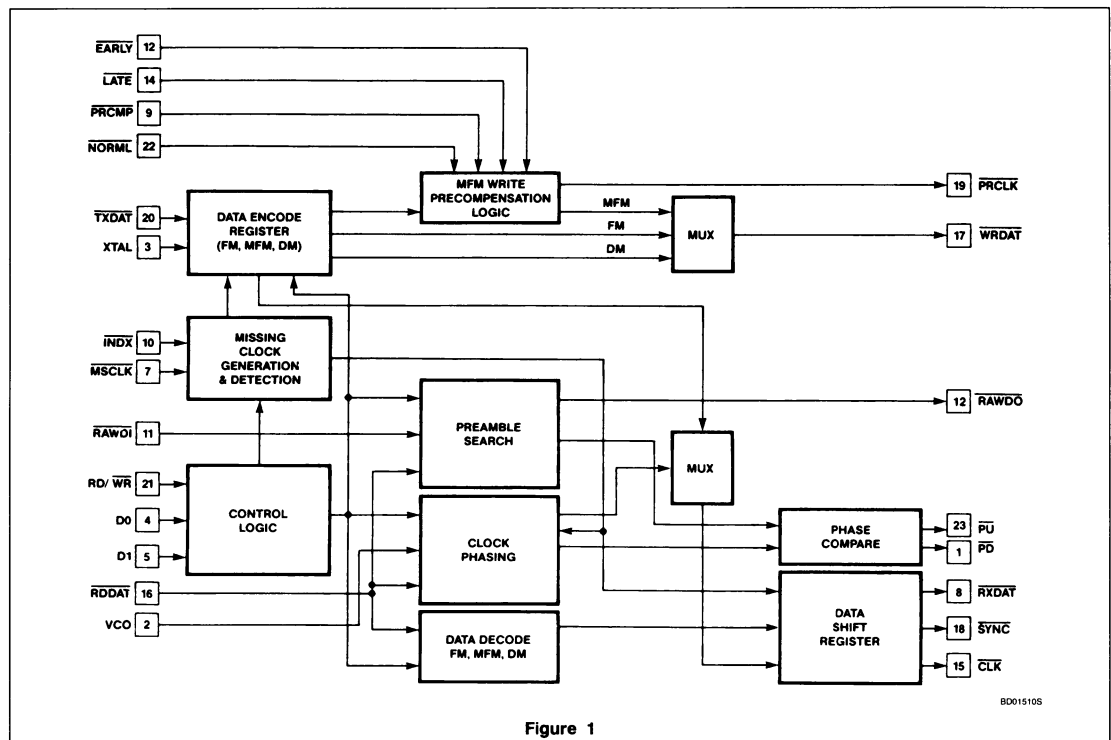
FEATURES
- **Data rates up to 10MHz**
- **FM, MFM, and Differential Manchester encoding/decoding**
- **Precompensation in MFM write mode**
- **Built-in phase comparator**
- **Single 5V power supply**
- **Selectable encoding violation generation/detection formats**

PIN CONFIGURATION

Pin	Signal		Pin	Signal
1	$\overline{PD}$		24	Vcc
2	VCO		23	$\overline{PU}$
3	XTAL		22	$\overline{NORML}$
4	DO		21	RD/$\overline{WR}$
5	D1		20	$\overline{TXDAT}$
6	GND		19	$\overline{PRCLK}$
7	$\overline{MSCLK}$		18	$\overline{SYNC}$
8	$\overline{RXDAT}$		17	$\overline{WRDAT}$
9	$\overline{PRCMP}$		16	$\overline{RDDAT}$
10	$\overline{INDX}$		15	$\overline{CLK}$
11	$\overline{RAWDi}$		14	$\overline{LATE}$
12	$\overline{RAWDO}$		13	$\overline{EARLY}$

74LS1801 ENCODER/DECODER

CD03301S

BLOCK DIAGRAM

Figure 1

BD01510S

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PIN CONFIGURATION

```
                 PD  [1]        24]  VCC
                 VCO [2]        23]  PU
                 XTAL[3]        22]  NORML
                 DO  [4]        21]  RD/WR
                 D1  [5]        20]  TXDAT
                 GND [6]  74LS1801   19]  PRCLK
                 MSCLK[7] ENCODER/   18]  SYNC
                 RXDAT[8]  DECODER   17]  WRDAT
                 PRCMP[9]        16]  RDDAT
                 INDX[10]        15]  CLK
                 RAWDi[11]       14]  LATE
                 RAWDO[12]       13]  EARLY
```

PIN NO.	IDENTIFIER	DESCRIPTION
10	INDX	INDeX – an input that designates the missing clock pattern to be generated during the write mode; in the read mode, determines which data/clock pattern must be recognized as an address mark (Table 2, 3).
11	RAWDI	RAW Data In – a shaped data pulse derived from RAWDO. RAWDO is normally tied directly to RAWDI.
12	RAWDO	RAW Data Out – a shaped data pulse derived from RDDAT that can be processed through an external phase lock loop. RAWDO is normally tied directly to RAWDI.
13	EARLY	Modifies clock rate with respect to crystal reference when early precompensation is desired.
14	LATE	Modifies clock rate with respect to crystal reference when late pre-compensation is desired.
15	CLK	CLocK – Clock input equal to the frequency of NRZ data.
16	RDDAT	ReaD DATa – an input of encoded serial data (MFM, FM, or Differential Manchester) that is to be converted to NRZ data.
17	WRDAT	WRite DATa – an output of encoded serial data (FM, MFM, or Differential Manchester) derived from NRZ data.
18	SYNC	SYNChronization output – when active low, indicates recognition of valid encoding violation in the RDDAT.
19	PRCLK	PRecompensation CLocK – an output used to excite an external delay line.
20	TXDAT	Transmit Data – an input of NRZ data that is to be encoded to FM, MFM, or Differential Manchester data.
21	RD/WR	ReaD/WRite – an input designating mode of operation: when high, a read is indicated; when low, a write is indicated.
22	NORML	NORMaL – a clock input that is used when no precompensation is desired.
23	PU	Pump Up – an output from the phase comparator that indicates the frequency of an external VCO is too low as compared to RDDAT.
24	VCC	Supply voltage.

PIN NO.	IDENTIFIER	DESCRIPTION
1	PD	Pump Down – an output from the phase comparator that indicates the frequency of an external VCO is too high as compared to RDDAT.
2	VCO	Voltage Controlled Oscillator – an input used as a phase reference for the encoded read data (RDDAT).
3	XTAL	An input used to synchronize the 74LS1801 during write mode; the crystal frequency is twice the serial data rate.
4	D0	Mode Select – inputs designating the format (FM, MFM, Differential Manchester) of serial I/O data that is to be encoded or decoded.
5	D1	
6	GND	Ground.
7	MSCLK	MiSsing CLocK – missing clock bits are generated/detected in the data stream, depending upon the state of this input (Table 2, 3).
8	RXDAT	Receive DATa – an output consisting of NRZ data decoded from MFM, FM, or Differential Manchester data.
9	PRCMP	PReCoMP – an input that allows precompensation of MFM encoded data.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
Hermetic DIP	N74LS1801I
Plastic DIP	N74LS1801N

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FUNCTIONAL OPERATION

The 74LS1801 Encoder/Decoder serves to translate data between disk drive or data communications devices and the 74LS1802 Serializer/Deserializer (or comparable device). Information entering or leaving the Serializer/Deserializer interface is in the form of standard NRZ data and can be encoded to (or decoded from) one of three popular formats:

- Frequency Modulation (FM) — single density disk recordings.
- Modified Frequency Modulation (MFM) — double density disk recordings.
- Differential Manchester — data communications applications.

Read/Write and Format Control

The operational mode of the 74LS1801 is dictated by the RD/$\overline{\text{WR}}$ input: when low, a write (encode) is indicated; when high, a read (decode) is designated. In either mode, the format of data being decoded or encoded is controlled by the states of D0 and D1 inputs as shown below:

Table 1. Format Control

D0	D1	RESULTING FORMAT
L	L	MFM
H	L	FM
L	H	Differential Manchester

Following are discussions of the encoding and decoding functions of the 74LS1801, and the timing requirements necessary for accurate data transmittal.

Encoding Logic

When in the encode mode, NRZ data is input via the $\overline{\text{TXDAT}}$ input and, after about a three bit delay, is output on $\overline{\text{WRDAT}}$. As described, output format is dependent on the states of D0 and D1. Address marks are distinguished from data by deleting clock pulses within the character.

These "missing clocks" are generated within the byte following a preamble of either all 0's (MFM and FM format) or all 1's (Differential Manchester format). As described in Table 2, clocks are eliminated according to inputs $\overline{\text{INDX}}$, $\overline{\text{MSCLK}}$, and the specified encoding format.

When encoding data in the MFM format, $\overline{\text{MSCLK}}$ may be enabled during preamble generation and up to the beginning of an address mark. $\overline{\text{MSCLK}}$ can then be disabled during the byte following an address mark, or before the final bit of a four bit series in which the first two bits are 0's (e.g., before the final 0 in 0010). In applications utilizing consecutive A1 characters (such as in the case of floppy disk soft-sectored formats), $\overline{\text{MSCLK}}$

Table 2. Missing Clocks

$\overline{\text{MSCLK}}$	$\overline{\text{INDX}}$	FORMAT	RESULTING CLOCK PATTERN Bit Cell Numbers:							
			0	1	2	3	4	5	6	7
L	H	FM			V	V	V			
L	L	FM			V		V			
L	H	Differential Manchester	V	V		V	V			
L	L	Differential Manchester	V	V			V			
L	X	MFM	2nd of 3 clocks missing							

NOTES:
X = Don't care
V = Missing Clock

Table 3. Address Mark Identification Requirements in Decode Mode

$\overline{\text{MSCLK}}$	$\overline{\text{INDX}}$	CONDITIONS FOR ACTIVE $\overline{\text{SYNC}}$ OUTPUT
H	X	First "1" bit after preamble
L	H	A1$_{16}$ with missing clocks
L	L	Any byte with missing clocks

would remain active until the beginning of the byte following the A1 series.

The 74LS1801 also provides pre-compensation capabilities when encoding data in the MFM format. Activating the $\overline{\text{PRCMP}}$ signal (low) synchronizes output data according to a clock input provided on one of three inputs: $\overline{\text{EARLY}}$ – a clock shifted early in time, $\overline{\text{LATE}}$ – a clock shifted late in time, or $\overline{\text{NORML}}$ – a clock provided when no precompensation is needed. These inputs are supplied by an external delay line which, in turn, is excited by the $\overline{\text{PRCLK}}$ output (see Typical System Configuration, Figure 2.)

When encoding in FM or Differential Manchester formats, missing clocks are only generated in the first byte following a preamble of zeroes. The most significant bit of this byte must be a "1"; for example, address marks F8, FB, FC, or FE. $\overline{\text{MSCLK}}$ may be enabled up to the beginning of an address mark; once an address mark has been transmitted, it is not necessary to disable $\overline{\text{MSCLK}}$.

Decoding Logic

In the decode mode, data (MFM, FM, or Differential Manchester) is input via the $\overline{\text{RDDAT}}$ input and, after an eleven bit delay, is output as NRZ data on $\overline{\text{RXDAT}}$. As described above, input format is defined by the states of D0 and D1. In the MFM format, a minimum preamble length of 34 bits is required to allow for phase synchronization and location of an address mark; when in FM or Differential Manchester mode, a minimum length of 18 bits is required. After a preamble has been recognized, the 74LS1801 searches for an address mark. When an address mark is identified, the $\overline{\text{SYNC}}$ output becomes active low, and alerts the 74LS1802 of incoming data. Rules for positive address mark identifi-

cation are described below and summarized in Table 3.

When $\overline{\text{MSCLK}}$ is inactive, $\overline{\text{SYNC}}$ is activated on the first "1" data bit following a preamble of zeroes (MFM and FM) or 1's (Differential Manchester). Data is contained in the byte following this bit.

If $\overline{\text{MSCLK}}$ is active, the byte following a preamble of all zeroes is checked for the required missing clocks (Table 3) and if detected, $\overline{\text{SYNC}}$ is activated.

PHASE LOCK LOOP AND DATA SEPARATION LOGIC

Data/clock separation logic requires a clock pulse that is synchronous with read data ($\overline{\text{RDDAT}}$); to create this signal, the 74LS1801 employs a Phase Lock Loop. In its simplest form, the PLL consists of an internal phase comparator, an external low pass filter and an external voltage controlled oscillator (VCO). Output from the VCO is continuously fed back to the phase compare circuit and contrasted with data read from the disk or communications device ($\overline{\text{RDDAT}}$). A difference in phase is represented as one of two quantized output pulses: Pump Up indicates VCO frequency is too low, whereas Pump Down indicates that the VCO frequency is too high. The resulting output ($\overline{\text{PU}}$ or $\overline{\text{PD}}$) is then processed by a low-pass filter which outputs a DC voltage proportional to the phase deviation. Accordingly, the VCO frequency is precisely serviced to the rate at which data was recorded. The 74LS1801 provides the capability to bypass internal phase compare logic; a typical application of this feature would be in designs implementing a complete external PLL.
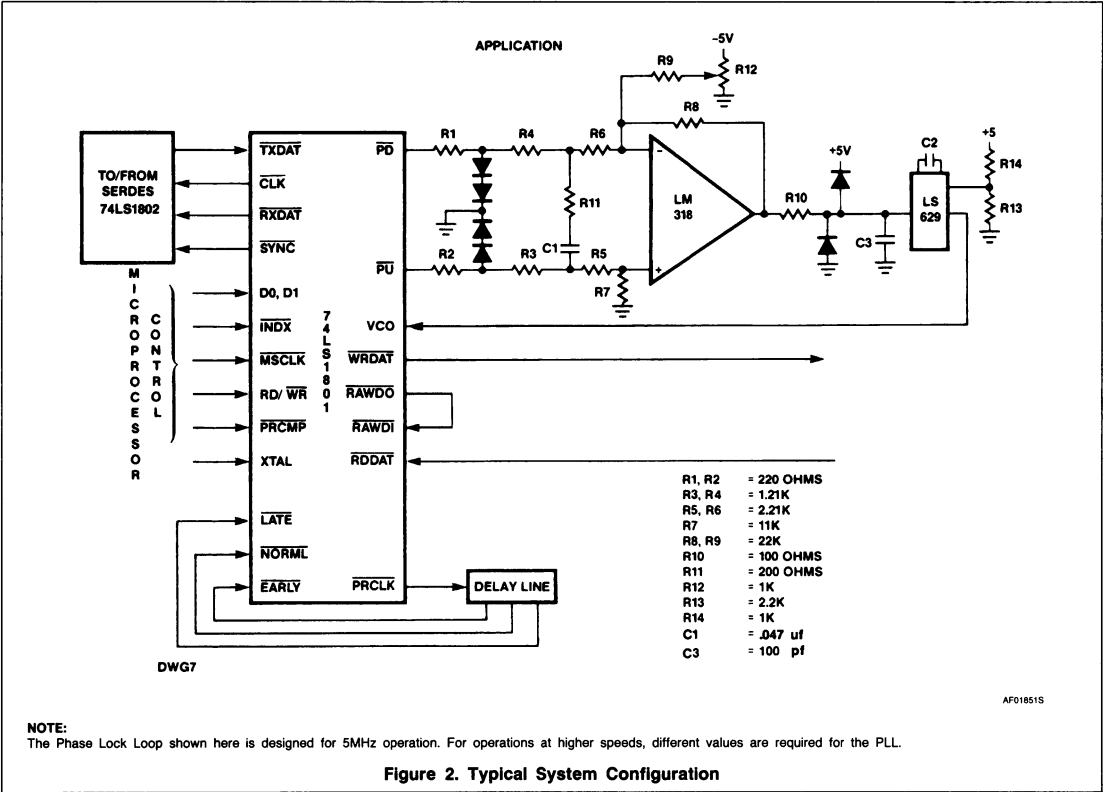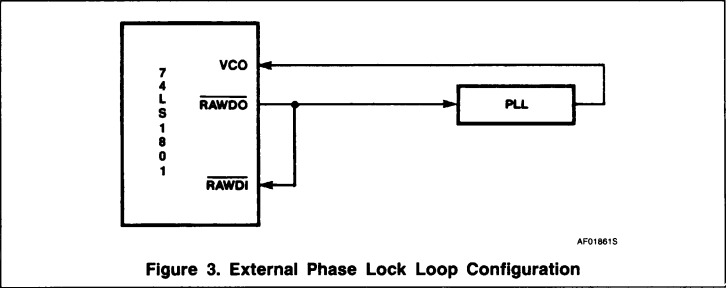
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APPLICATION

R1, R2 = 220 OHMS
R3, R4 = 1.21K
R5, R6 = 2.21K
R7 = 11K
R8, R9 = 22K
R10 = 100 OHMS
R11 = 200 OHMS
R12 = 1K
R13 = 2.2K
R14 = 1K
C1 = .047 uf
C3 = 100 pf

DWG7

AF01851S

NOTE:
The Phase Lock Loop shown here is designed for 5MHz operation. For operations at higher speeds, different values are required for the PLL.

Figure 2. Typical System Configuration
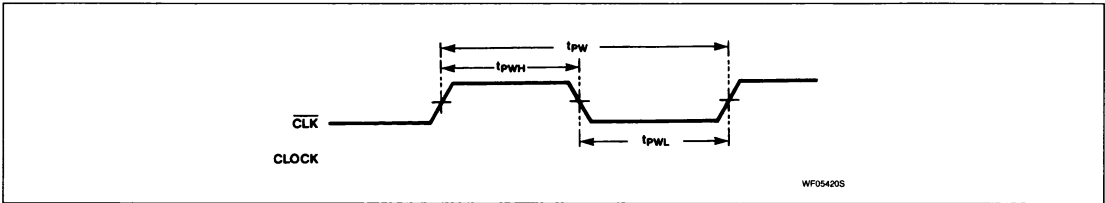
Figure 3 illustrates this application and is discussed below.

RAW Data Out is a shaped data pulse derived directly from $\overline{RDDAT}$. In MFM and FM modes, output is generated from the falling edge of $\overline{RDDAT}$: in Differential Manchester mode, output is generated from both rising and falling edges. RAW Data In is a shaped data pulse derived from $\overline{RAWDO}$ and is used in internal data separation logic. The falling edge of $\overline{RAWDI}$ must be in phase with the falling edge of the VCO. $\overline{RAWDI}$ is normally tied directly to $\overline{RAWDO}$.

AF01861S

Figure 3. External Phase Lock Loop Configuration

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CLOCK CYCLE

WF05420S

READ CYCLE

WF05430S

OTHER TIMING

WF05440S
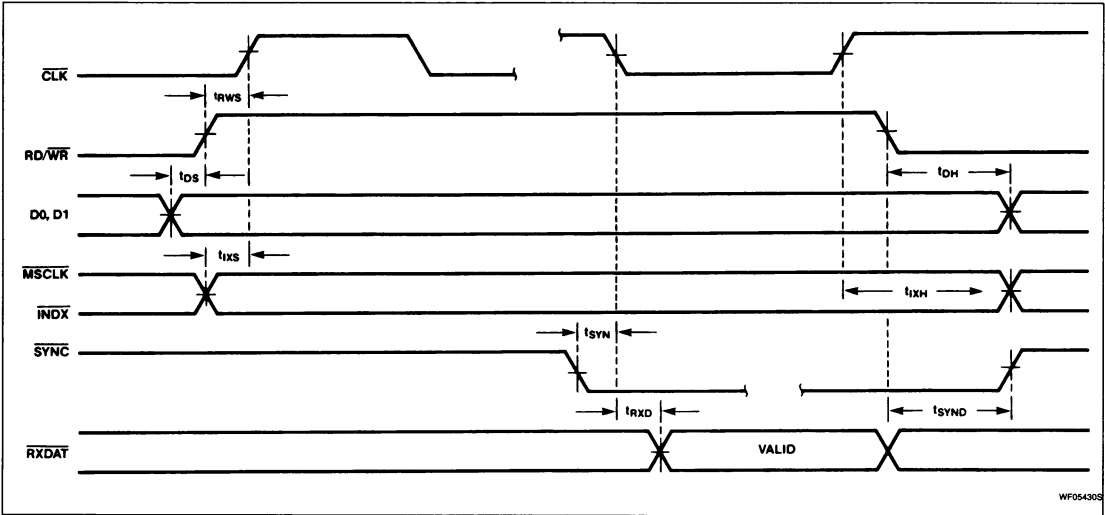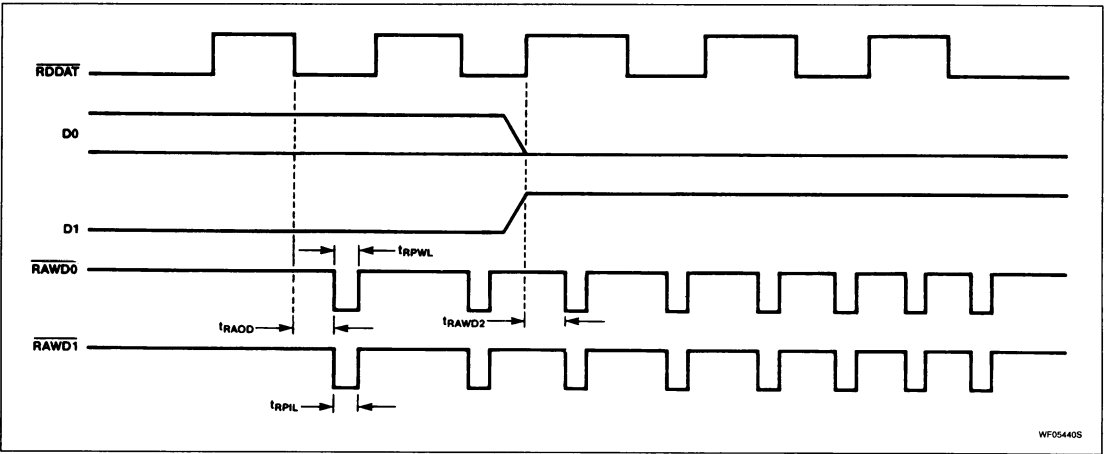
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WRITE CYCLE TIMING

WF05450S
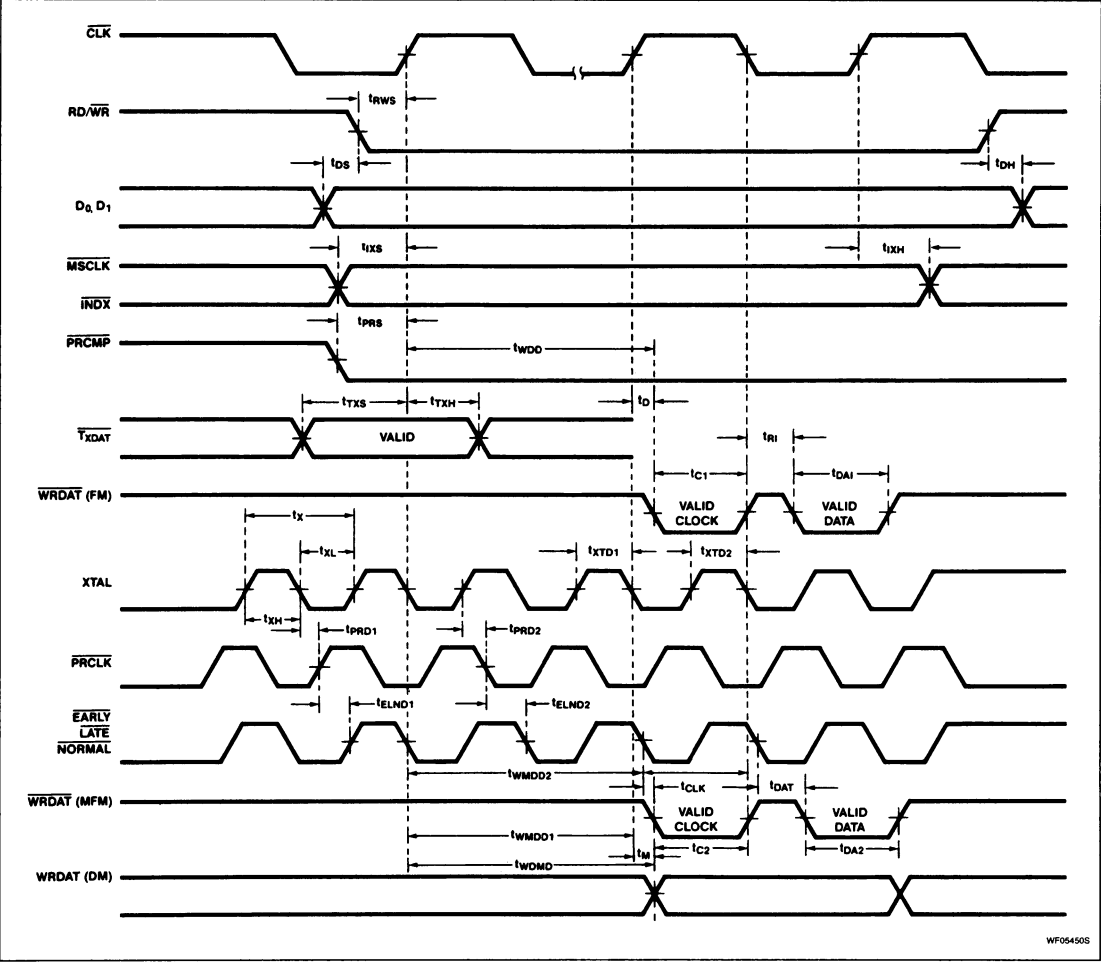
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ABSOLUTE MAXIMUM RATINGS

PIN	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V
All other pins	Logic input pins	5.5	V

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V \pm 5\%$; TA = 0°C to +70°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT	COMMENTS
			Min	Typ	Max		
V_{TH}	Input threshold voltage		0.8		2.0	V	
V_{CD}	Input clamp diode voltage	$I_N = -18mA$			-1.2	V	
I_{IL}	Input low current	$V_{IN} = 0.4V$			-20	μA	
I_{IH}	Input high current	$V_{IN} = 2.7V$			20	μA	
I_I	Max input high current	$V_{IN} = 5.5V$			100	μA	
V_{OL}	Output voltage low	$I_{OL} = 8mA$ $I_{OL} = 20mA$			0.5 0.5	V V	Pins 8, 12, 15, 17, 18, 19 Pins 1, 23
V_{OH}	Output voltage high	$V_{CC} = 4.5V$ $I_{OH} = 400\mu A$ $I_{OH} = 1mA$	2.5 2.5			V V	Pins 8, 12, 15, 17, 18, 19 Pins 1, 23
I_{OS}	Output short circuit current	$V_{OUT} = 0$ $V_{OUT} = 1$	-15 -15		-100 -100	mA mA	Pins 8, 12, 15, 17, 18, 19 Pins 1, 23
I_{CC}	Supply current				184	mA	

AC ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION	LIMITS (in ns)		
		Min	Typ	Max
t_{PW}	$\overline{CLK}$ pulse width	100		
t_{PWL}	$\overline{CLK}$ low time	50		
t_{PWH}	$\overline{CLK}$ high time	50		
t_X	XTAL cycle time	50		
t_{XH}	XTAL high time	25		
t_{XL}	XTAL low time	25		
t_{RWS}	RD/$\overline{WR}$ set-up to ↑$\overline{CLK}$	0		
t_{DS}	D0, D1 set-up to RD/$\overline{WR}$	0		
t_{IXS}	$\overline{MSCLK}$, $\overline{INDX}$ set-up to ↑$\overline{CLK}$		35.2	
t_{SYN}	↓$\overline{SYNC}$ to ↓$\overline{CLK}$	2		
t_{RXD}	↓$\overline{CLK}$ to $\overline{RXDAT}$ valid			4
t_{DH}	RD/$\overline{WR}$ to D0, D1 hold	0		
t_{SYND}	RD/$\overline{WR}$ to $\overline{SYNC}$ inactive delay			36.4
t_{RAOD}	↓$\overline{RDDAT}$ to ↓$\overline{RAWDO}$ delay		29.2	
t_{RPIL}	$\overline{RAWDI}$ pulse width	20*		
t_{RPWL}	$\overline{RAWDO}$ pulse width			40*
t_{WDMD}	$\overline{TXDAT}$ to $\overline{WRDAT}$ (DM)			$t_{PW} + 41.2$
t_M	↑$\overline{CLK}$ to $\overline{WRDAT}$ delay		41.2	
t_{RAWD2}	↑$\overline{RDDAT}$ to ↓$\overline{RAWDO}$ delay		32.2	

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AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	DESCRIPTION	LIMITS (in ns)		
		Min	Typ	Max
t_{DA2}	DATA bit duration		23.0	
t_{IXH}	$\uparrow$CLK to $\overline{MSCLK}$, $\overline{INDX}$ hold		14.8	
t_{PRS}	$\overline{PRCMP}$ set-up to $\uparrow\overline{CLK}$			0
t_{TXS}	$\overline{TXDAT}$ set-up to $\uparrow\overline{CLK}$		85.2	
t_{TXH}	$\overline{TXDAT}$ hold time		14.8	
t_{WDD}	$\overline{TXDAT}$ to $\overline{WRDAT}$ clock delay (FM data)		t_{PW} + 36.3	
t_D	$\uparrow\overline{CLK}$ to clock delay (FM data)		36.3	
t_{C1}	Clock bit duration (FM)		19.0	
t_{R1}	Clock & data bit separation		31.0	
t_{DA1}	Data bit duration (FM)		19.0	
t_{XTD1}	$\uparrow$XTAL to $\uparrow\overline{CLK}$ delay		35.2	
t_{XTD2}	$\uparrow$XTAL to $\downarrow\overline{CLK}$ delay		32.2	
t_{PRD1}	$\downarrow$XTAL to $\uparrow\overline{PRCLK}$ delay		26.3	
t_{PRD2}	$\uparrow$XTAL to $\downarrow\overline{PRCLK}$ delay		28.3	
t_{ELND1}	$\uparrow\overline{PRCLK}$ to $\overline{Early}$, $\overline{Late}$, $\overline{Normal}$ rising edge	$\frac{1}{2}$ t_{PW}		$\frac{1}{4}$ t_{PW}
t_{ELND2}	$\downarrow\overline{PRCLK}$ to $\overline{Early}$, $\overline{Late}$, $\overline{Normal}$ falling edge	$\frac{1}{4}$ t_{PW}		0
t_{WMDD2}	$\overline{TXDAT}$ to $\overline{WRDAT}$ data delay (MFM)			3.5 x t_{PW}
t_{WMDD1}	$\overline{TXDAT}$ to $\overline{WRDAT}$ clock delay (MFM)			3.0 x t_{PW}
t_{CLK}	$\overline{Early}$, $\overline{Late}$, $\overline{Normal}$ falling edge to clock bit delay (MFM)		12.1	
t_{C2}	Clock bit duration (MFM)		23.0	
t_{DAT}	$\overline{Early}$, $\overline{Late}$, $\overline{Normal}$ falling edge to data bit delay (MFM)		12.1	

*Tabular entries with an asterisk are parameters that are guaranteed at the values listed; these values were determined either by system bench testing or by Signetics' characterization procedures. All other tabular entries are taken directly from simulation results run at range of operational frequencies; these values are not tested or guaranteed.

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