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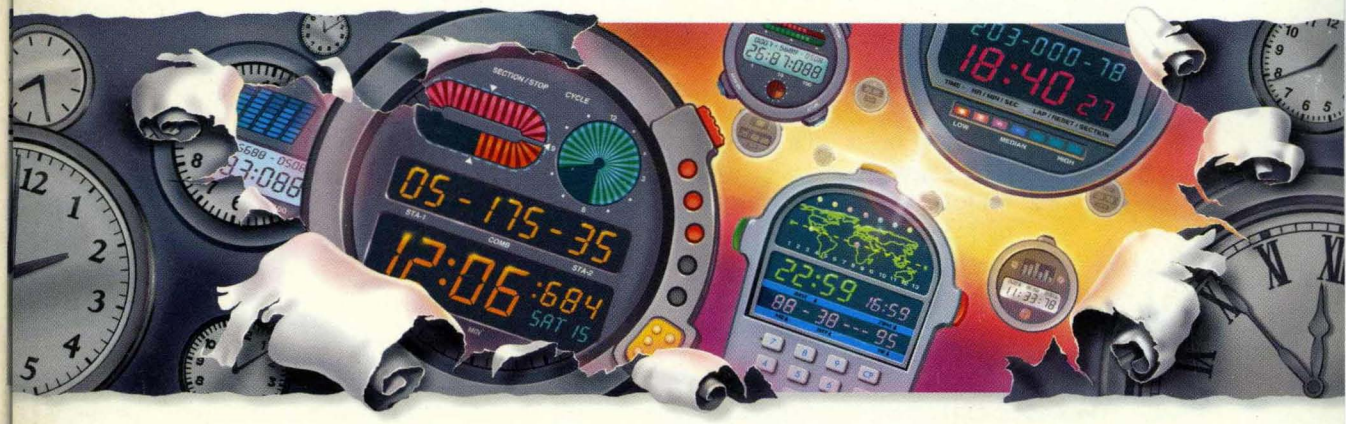
TIMING SOLUTIONS



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- *Low Voltage, Low Skew Fanout Buffers*
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TIMING SOLUTIONS

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Timing Solutions

This brochure contains device information on Motorola's family of timing solution products. The brochure includes datasheets on both PLL and fanout buffer based products both at 5.0V and 3.3V V_{CC}'s. The timing solutions family will continue to grow rapidly. For datasheets designated "Advance Information" or "Product Preview", as well as new products, please contact your Motorola representative.

Printed in U.S.A.

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* = Represents information that has not appeared in previous issues of this publication.

Italics represent documents that have been revised since the last issue of this publication.

MOTOROLA'S LOW SKEW CLOCK DRIVERS

Part Number	Output Level	Max Out–to–Out Skew (ns) (Note 1.)	Max Output Freq. (MHz)	Number of Q Outputs	Q' Outputs	Package Types	Other Features
MC74F803	TTL	1.0	35		4	14 DIP/SOIC	TTL Inputs
MC74F1803	TTL	2.0	35		4	14 DIP/SOIC	TTL Inputs
MC10/100H640	TTL	0.5	33 & 66	6	2	28 PLCC	PECL or TTL Inputs (Note 2.)
MC10/100H641	TTL	0.5	65	9		28 PLCC	PECL Inputs (Note 2.)
MC10/100H642	TTL	0.5	33 & 66	8		28 PLCC	PECL or TTL Inputs (Note 2.)
MC10/100H643	TTL	0.5	65	9		28 PLCC	ECL Inputs
MC10/100H644	TTL	0.5	33 & 66	4	2	20 PLCC	PECL or TTL Inputs (Note 2.)
MC10/100H645	TTL	0.65	66	9		28 PLCC	TTL Inputs
MC10/100H646	TTL	0.5	100	8		28 PLCC	PECL or TTL Inputs (Note 2.)
MC88913	CMOS	1.0	55	4	2	14 DIP/SOIC	
MC88914	CMOS	1.0	55	4	2	14 DIP/SOIC	Pwr-On & Ext Resets
MC88915	CMOS	0.5	55, 70	7	1	28 PLCC	Phase-Locked Loop
MC88915T	CMOS	0.5	133, 160	7	1	28 PLCC	Phase-Locked Loop
MC88916	CMOS	0.5	20, 40, 80	5	1	20 SOIC	Phase-Locked Loop
MC88920	CMOS	0.5	12.5, 25, 50	5	1	20 SOIC	Phase-Locked Loop
MC88921	CMOS	0.5	80	2	1	20 SOIC	Phase-Locked Loop
MC88PL117	CMOS	0.35	133, 160	16		52 PLCC	Phase-Locked Loop
MC88LV915T	LVCMOS	0.5	100	7	1	28 PLCC	3.3V PLL
MC88LV926	LVCMOS	0.5	66	4	1	20 SOIC	3.3V PLL
MPC903/904/905	LVCMOS	0.4	66	6		16 SOIC	3.3V Osc/Buffer
MPC911	HSTL	0.05	200	9		28 PLCC	3.3V Fanout Buffer
MPC930/931	LVCMOS	0.3	125	5		32 TQFP	3.3V PLL
MPC932	LVCMOS	0.35	120	7		32 TQFP	3.3V PLL
MPC940	LVCMOS	0.25	200	18		32 TQFP	1:18 Fanout Buffer
MPC941	LVCMOS	0.25	200	27		52 TQFP	1:27 Fanout Buffer
MPC946	LVCMOS	0.35	150	10		32 TQFP	3.3V ÷1,÷2 Outputs
MPC947	LVCMOS	0.5	100	9		32 TQFP	3.3V Fanout Buffer
MPC948	LVCMOS	0.35	150	12		32 TQFP	3.3V Fanout Buffer
MPC949	LVCMOS	0.35	150	15		52 TQFP	3.3V ÷1,÷2 Outputs
MPC950/951	LVCMOS	0.35	200	9		32 TQFP	3.3V PLL
MPC952	LVCMOS	0.35	180	11		32 TQFP	3.3V PLL
MPC970/971	LVCMOS	0.35	250	13		52 TQFP	3.3V PLL
MPC972/973	LVCMOS	0.35	180	14		52 TQFP	3.3V PLL
MPC974	LVCMOS	0.35	125	15		52 TQFP	3.3V PLL
MPC980	LVCMOS	0.5	66	10		52 TQFP	3.3V Dual PLL
MPC990/991	LVECL/LVPECL	0.1	400	diff 14/pairs		52 TQFP	3.3V PLL
MPC992	LVECL/LVPECL	0.1	100	diff 7/pairs		32 TQFP	3.3V PLL
MPC9108	CMOS	N/A	50	1		8 SOIC	5V Clock Gen
MC10/100EL11	ECL	0.02	1000	diff 2/pairs		8 SOIC	PECL/ECL Inputs (Note 2.)
MC10/100EL15	ECL	0.05	600	diff 4/pairs		16 SOIC	MUXed Test CLK Input
MC10/100E111	ECL	0.05	600	diff 9/pairs		28 PLCC	PECL/ECL Inputs (Note 2.)
MC10/100E211	ECL	0.075	1000	diff 6/pairs		28 PLCC	Indiv. Sync Enable
MC100EP111	LVECL	0.035	1500	diff 10/pairs		32 TQFP	1:10 Fanout Buffer
MC100EP221	LVECL	0.050	1500	diff 20/pairs		52TQFP	1:20 Fanout Buffer
MC100LVEL/EL13	LVECL	0.05	600	diff 6/pairs		20 SOIC	3.3V Dual 1:3 Fanout
MC100LVEL/EL14	LVECL	0.05	600	diff 10/pairs		20 SOIC	3.3V 1:5 Fanout
MC100LVE111	LVECL	0.05	600	diff 9/pairs		28 PLCC	3.3V PECL/ECL
MC100LVE/E210	LVECL	0.05	600	diff 9/pairs		28 PLCC	3.3V Dual 1:4,1:5 Fanout
MC100LVE222	LVECL	0.05	600	diff 15/pairs		52 TQFP	3.3V Dual 1:15,÷1, ÷2 Fanout
MC100LVE/E310	LVECL	0.05	600	diff 8/pairs		28 PLCC	3.3V 2:8 Fanout
MC12429	LVPECL		400	diff 1/pair		28 PLCC	Clock Generator
MC12430	LVPECL		800	diff 1/pair		28 PLCC	Clock Generator
MC12439	LVPECL		800	diff 1/pair		28 PLCC	Clock Generator

1. Within device skew.
2. PECL = Positive ECL (ECL levels referenced to +5.0V).

AN1091
Application Note

Low Skew Clock Drivers and Their System Design Considerations

Prepared by
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This application note addresses various system design issues to help ensure that Motorola's low skew clock drivers are used effectively in a system environment.

Low Skew Clock Drivers and Their System Design Considerations

ABSTRACT

Several varieties of clock drivers with 1ns or less skew from output-to-output are available from Motorola. Microprocessor-based systems are now running at 33MHz and beyond, and system clock distribution at these frequencies mandate the use of low skew clock drivers. Unfortunately, just plugging a high performance clock driver into a system does not guarantee trouble free operation. Only careful board layout and consideration of system noise issues can guarantee reliable clock distribution. This application note addresses these system design issues to help ensure that Motorola's low skew clock drivers are used effectively in a system environment.

INTRODUCTION

With frequencies regularly reaching 33MHz and approaching 40-50MHz in today's CISC and RISC microprocessor systems, well controlled and precise clock signals are required to maintain a synchronous system. Many microprocessors also require input clock duty cycles very close to 50%. These stringent timing requirements mandate the use of specially designed, low skew clock distribution circuits or 'clock drivers.' However, just plugging one of these parts into your board does not ensure a trouble free system. Careful system and board design techniques must be used in conjunction with a low skew clock driver to meet system timing requirements and provide clean clock signals.

Why are Low Skew Clock Drivers Necessary

An MPU system designer wants to utilize as much of a clock cycle as possible without adding unnecessary timing guardbands. Propagation delays of peripheral logic do not scale with frequency. Therefore, as the clock period decreases, the system designer has less time but the same logic delays to accomplish the function. How can he get more time? A viable option is to use a special clock source that minimizes clock 'uncertainty.'

A simple example illustrates this concept. At 33MHz, T_{cycle} = 30ns. An FCT240A, for example, has a High-Low uncertainty of the min/max spread of t_{PLH} to t_{PHL} of approximately 3.3ns. If 1.7ns of pin-to-pin skew due to the actual part and PCB trace delays is also considered, then only 25ns of the clock period is still available. The worst case t_P of clock-to-data valid on the 88200 M-Bus is 12ns, which leaves only 13ns to accomplish additional functions. In this case 17% of a cycle is required for clock distribution or clock 'uncertainty,' which is an unacceptable penalty from a system designer's point of view. At 50MHz this penalty becomes 25%. A maximum of 10% of the period allotted for clock distribution is an acceptable standard.

If multiple levels of clock distribution (one clock driver's output feeding the inputs of several other clock drivers) are necessary due to large clock fan-outs, the additional part-to-part skew variations add even more to the clock uncertainty. Standard logic has always been specified with a large (and conservative) delta between the minimum and maximum propagation delays. This delta creates the excessive amount of clock 'uncertainty' which the system designer has been forced to design into his system, even though it is not realistic. When system frequencies were below 16MHz this large clock penalty could be tolerated, but as the above example points out, not anymore. A clock driver's specs *guarantee* this min/max delta to be a specific, small value. To reduce the clock overhead to manageable levels, a clock driver with minimal variation (<5%) from a 50% duty cycle and guaranteed low output-to-output and part-to-part skew must be used.

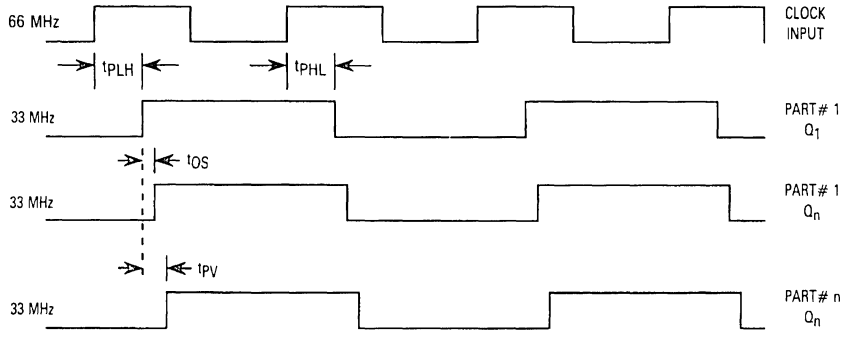
DEFINITIONS

A typical clock driver has a single input which is usually driven by a crystal oscillator. The clock driver can have any number of outputs which have a certain frequency relationship to the clock input. Clock driver skew is typically defined by three different specs. These specs are graphically illustrated in Figure 1.

The first spec, t_{OS}, measures the difference between the fastest and slowest propagation delays (any transition) between the outputs of a single part. This number must be 1ns or less for high-end systems.

The second, t_{PS}, measures the difference between the high-to-low and low-to-high transition for a single output (pin). This spec defines how close to a 50% duty cycle the outputs of the clock driver will be. For example, if this spec is 1ns (±0.5ns), at 33MHz the output duty cycle is 50% ±3.5%. A clock driver which only buffers the crystal input, creating a 1:1 input to output frequency relationship, can be a problem if a very tight tolerance to a 50% duty cycle is required. In this situation the output duty cycle is directly dependent on the input duty cycle, which is not well controlled in most crystal oscillators. The clock driver's outputs switching at half the input frequency (÷2) is a common relationship, which means that the outputs switch on only one edge of the oscillator, eliminating the output's dependence on the duty cycle of the input (crystal oscillator frequency is very stable).

The third spec, t_{PV}, measures the maximum propagation delay delta between any given pin on any part. This spec defines the part to part variation between any clock driver (of the same device type) which is ever shipped. This number reflects the process variation inherent in any technology. For CMOS, this spec is usually 3ns or less. High performance ECL technologies can bring this number down into the 1-2ns range. Another way to minimize the part-to-part variation is to use a phase-locked loop clock driver, which are just now becoming available.



Notes: 1) t_{PS} measures $|t_{PLH}-t_{PHL}|$ for any single output on a part.
2) t_{OS} measures the maximum difference between any t_{PHL} or t_{PLH} between any output on a single part.
3) t_{PV} measures the maximum difference between any t_{PHL} or t_{PLH} between any output on any part.

Figure 1. Timing Diagram Depicting Clock Skew Specs Within One Part and Between Any Two Parts

An important consideration when designing a clock driver into a system is that the skew specs described above are usually specified at a fixed, lumped capacitive load. In a real system environment the clock lines usually have various loads distributed over several inches of PCB trace which can contribute additional delay and sometimes act like transmission lines, so the system designer must use careful board layout techniques to minimize the total system skew. In other words, just plugging a low skew clock driver into a board will not solve all your timing problems.

DESIGN CONSIDERATIONS

Figure 2 is a scale replication of a section of an actual 88000 RISC system board layout. The section shown in the figure includes the MC88100 MPU and the MC88200 CMMU devices and the MC88914 CMOS clock driver. The only PCB traces shown are the clock output traces from the MC88914 to the various loads. For this clock driver the output-to-output skew (t_{OS}) is guaranteed to be less than 1ns at any given temperature, supply voltage, and fixed load up to 50 pF.

In calculating the total system skew, the difference in clock PCB trace length and loading must be taken into account. For an unloaded PCB trace, the signal delay per unit length, t_{PD}, is dependent only on the dielectric constant, e_r. of the board material. The characteristic impedance, Z_O, of the line is dependent upon e_r and the geometry of the trace. These relationships are depicted in Figure 3 for a microstrip line.1 The formulas for t_{PD} and Z_O are slightly different for other types of strip lines, but for simplicity's sake all calculations in this article will assume a microstrip line.

The equations in Figure 3 are valid only for an unloaded trace; loading down a line will increase its delay and lower its impedance. The signal propagation delay (t_{PD}') and characteristic impedance (Z_O') due to a loaded trace are calculated by the following formulas:

$$t_{PD}' = t_{PD}\sqrt{1 + \frac{C_d}{C_O}}$$

$$Z_O' = \frac{Z_O}{\sqrt{1 + \frac{C_d}{C_O}}}$$

C_d is the distributed load capacitance per unit length, which is the total input capacitance of the receiving devices divided by the length of the trace. C_O is the intrinsic capacitance of the trace, which is defined as:

$$C_O = \frac{t_{PD}}{Z_O}$$

Assuming typical microstrip dimensions and characteristics as w = 0.01 in, t = 0.002in, h = 0.012in, and e_r = 4.7, the equations of Figure 3 yield Z_O = 69.4Ω and t_{PD} = 0.144ns/in C_O is then calculated as 2.075pF/in. If it is assumed that an MC88100 or 88200 clock input load is 15pF, and that two of these loads, in addition to a 7pF FAST TTL load, are distributed along a 9.6in clock trace,

$$C_d = (2 \times 15 + 7)\text{pF}/9.6\text{in} = \text{pF/in}.$$

The loaded trace propagation delay and characteristic impedance are then calculated as

$$t_{PD}' = 0.243\text{ns/in and } Z_O' = 41\Omega.$$

Looking at trace C in Figure 2, the two MC88200's are approximately 3 inches apart. Using the calculated value of t_{PD}', the clock signal skew due to the trace is about 0.7ns. Since these two devices are on the same trace, this is the total clock skew between these devices. Upon careful inspection of all the clock traces, it can be seen that clock signal skew was accounted for and minimized on this board layout. The longest

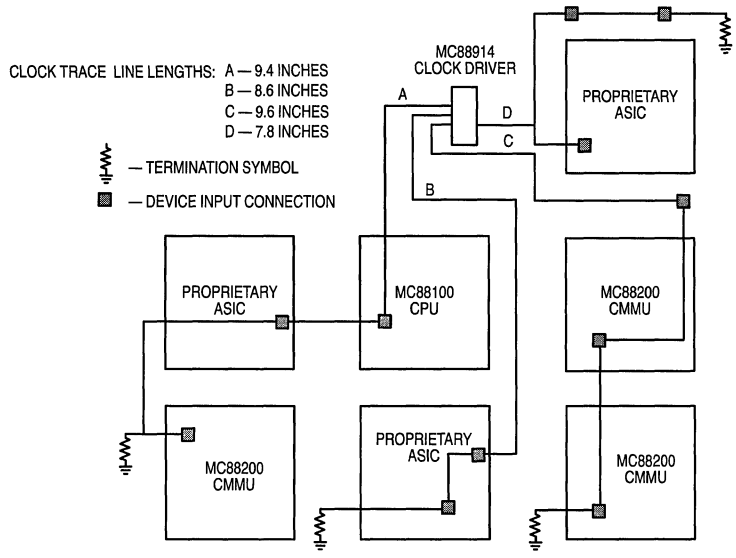
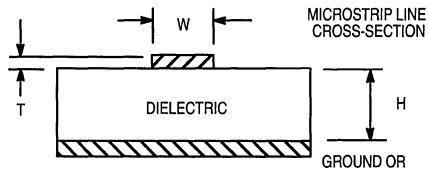


Figure 2. Scale Representation of an Actual 88000 System PCB Layout
(Only sections of the board related to the clock driver outputs are shown.)

distance between any 88K devices on a single clock trace is about 4.5 inches, which translates to approximately 1.1ns of skew. The two 88K devices farthest away from the clock driver (traces a and c), are located at almost exactly the same distance along their respective traces, making the clock skew between them the 1ns guaranteed from output to output of the clock driver. This means that the worst case clock skew between any two devices on this board is approximately 2.1ns, which at 33MHz is 7% of the period. Without careful attention to matching the clock traces on the board, this number could easily exceed 3ns and the 10% cut-off point, even if a low skew clock driver is used.



$$Z_O = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

$$t_{pd} = 1.017\sqrt{0.475\ e_r + 0.67}\ \text{ns/ft}$$

WHERE:
e_r = Relative Dielectric Constant of the Board Material
w, h, t = Dimensions Indicated in a Microstrip Diagram

Figure 3. Formulas for the Characteristic Impedance and Propagation Delay of a Microstrip Line (Ref 1)

CLOCK SIGNAL TERMINATIONS

Transmission line effects occur when a large mismatch is present between the characteristic impedance of the line and the input or output impedances of the receiving or driving device. The basic guidelines used to determine if a PCB trace needs to be examined for transmission line effects is that if the smaller of the driving device's rise or fall time is less than three times the propagation delay of a switching wave through a trace, the transmission line effects will be present.[2] This relationship can be stated in equation form as:[3]

$$3 \times t_{PD}' \times \text{trace length} \leq t_{RISE} \text{ or } t_{FALL}$$

For the MC88914 CMOS clock driver described in this article, rise and fall times are typically 1.5ns or less (from 20% to 80% of V_{CC}). Analyzing the clock trace characteristics presented earlier for transmission line effects, 3 x 0.243ns/in x trace length ≤1ns (1ns is used as 'fastest' rise or fall time). Therefore the trace length must be less than 1.5 inches for the transmission line effects to be masked by the rise and fall times.

Figure 4 shows the clock signal waveform seen at the receiver end of an unterminated 0.5 inch trace and an unterminated 9 inch trace. These results were obtained using SPICE simulations. which may not be exact, but are adequate to predict trends and for comparison purposes. The 9 inch trace, which is well beyond the 1.5 inch limit where transmission line effects come into play, exhibits unacceptable switching characteristics caused by reflections going back and forth on the trace. Even the 0.5 inch line exhibits substantial overshoot and undershoot. Any unterminated line will exhibit some overshoot and undershoot at these edge rates.

Clock lines shorter than 1-1.5 inches are unrealistic on a practical board layout, therefore it is recommended that CMOS clock lines be terminated if the driver has 1-2ns edge rates. Termination, which is used to more closely match the line to the load or source impedances, has been a fact of life in the ECL world for many years (reference 1 is an excellent source for transmission line theory and practice in ECL systems), but CMOS and TTL devices have only recently reached the speeds and edge rates which require termination. CMOS outputs further complicate the issue by driving from rail to rail (5 V), with slew rates exceeding those of high performance ECL devices.

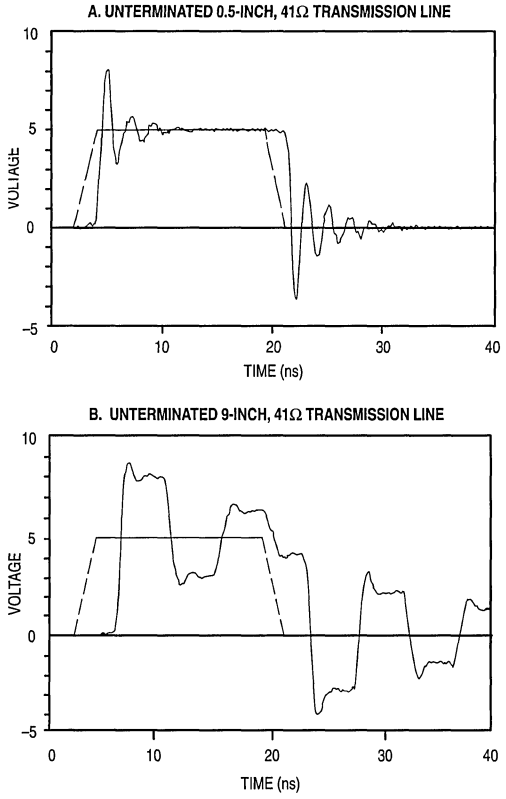


Figure 4. SPICE Simulation Results of 'Short' and 'Long' Transmission Lines. Simulations Were Run with Typical Parameters @ 25°C and V_{CC} = 5.0V

Since clock lines are only driven from a single location, they lend themselves to termination more easily than bus lines which are commonly driven from multiple locations. Termination of bus lines with multiple drivers is a complicated manner which will not be addressed in this article. The most common types of termination in digital systems are shown in Figure 5. Since no single termination scheme is optimal in all cases, the tradeoffs involving the use of each will be discussed, and recommendations specific to clock drivers will be made. Reference 2 is a comprehensive and practical treatment of transmission line theory and analysis of CMOS signals, and is recommended reading for those who want to gain a better understanding of transmission lines. Figure 6 shows SPICE simulated waveforms of the different termination schemes to be discussed. The driving device in the simulations was the MC88914 output buffer; in all simulations it drove a 9 inch 41Ω transmission line. The simulations were run using typical model parameters at 25°C and V_{CC} = 5V.

Series termination, depicted in Figure 5b, is recommended if the load is lumped at the end of the trace and the output impedance of the driving device is less than the loaded characteristic impedance of the trace, or when a minimum number of components is required. The main problem with series termination occurs when the driving device has different output impedance values in the low and high states, which is a problem in TTL and some CMOS devices. A well designed CMOS clock driver should have nearly equal output impedances in the high and low states, avoiding this problem. An additional advantage is that series termination does not create a DC current path, thus the V_{OL} and V_{OH} levels are not degraded. The SPICE generated waveforms of series termination in Figure 6a show that series termination effectively masks the transmission line effects exhibited in Figure 4. If each clock output is driving only one device, series termination would be recommended, but this is not a realistic case in most systems, so series termination is not generally recommended for termination of clock lines.

Parallel termination utilizes a single resistor tied to ground or V_{CC} whose value is equal to the characteristic impedance of the line. Its major disadvantage is the DC current path it creates when the driver is in the high state (if the resistor is tied to ground). This causes excessive power dissipation and V_{OH} level degradation. Since a clock driver output is always switching, the DC current draw argument loses some credibility at higher frequencies because the AC switching current becomes a major component of the overall current. Therefore the main consideration in parallel termination is how much V_{OH} degradation can be tolerated by the receiving devices. Figure 6b demonstrates that this termination technique is effective in minimizing the switching noise, but Thevenin termination has some advantages over parallel termination.

Thevenin termination utilizes one resistor tied to ground and a second tied to V_{CC}. An important consideration when using this type of termination is choosing the resistor values to avoid settling of the voltage between the high and low logic levels of the receiving device.2 TTL designers commonly use a 220/330 resistor value ratio, but CMOS is a little tricky because the switch point is at $V_{CC}/2$. With a 1:1 resistor ratio a failure at the driver output would cause the line to settle at 2.5V, causing system debug problems and also potential damage to the receiving devices.

In Thevenin termination, the parallel equivalent value of the two resistors should be equal to the characteristic impedance of the line. A DC path does exist in both the high and low states, but it is not as bad as parallel termination because the resistance in the Thevenin DC path is at least 2 times greater.

Figure 6c shows the termination waveforms, which exhibit characteristics similar to parallel termination, but with less V_{OH} degradation. The only real advantage of parallel over Thevenin is less resistors (1/2 as many) and less space taken up on the board by the resistors. If this is not a factor, Thevenin termination is recommended over parallel.

AC termination, shown in Figure 5e, normally utilizes a resistor and capacitor in series to ground. The capacitor blocks DC current flow, but allows the AC signal to flow to ground during switching. The RC time constant of the resistor and capacitor must be greater than twice the loaded line delay. AC termination is recommended because of its low power dissipation and also because of the availability of the resistor and capacitor in single-in-line packages (SIP). A pullup resistor to V_{CC} is sometimes added to set the DC level at a certain point because of the failure condition described in regards to Thevenin termination. As discussed earlier, the argument of lower DC current is less convincing at high frequencies. The AC terminated waveform walks out slightly toward the end of a high-to-low or low-to-high transition as seen in Figure 6d, making it slightly less desirable than Thevenin termination.

Thevenin and AC termination are the two recommended termination schemes for clock lines, but it depends on what frequency the clock is running at when making a decision between these types of termination. Although hard data is not provided to back this statement up, it is a safe assumption that at frequencies of 25 MHz and below AC is the best choice. If the system frequency could reach 40 MHz and beyond, Thevenin becomes the better choice.

ADDITIONAL CONSIDERATIONS WHEN TERMINATING CLOCK LINES

The results presented might imply that terminating the clock lines will completely solve noise problems, but termination can cause secondary problems with some logic devices. Termination acts to reduce the noise seen at the receiver, but that noise actually is seen as additional current and noise at the output of the driving device. If the internal and input logic on the source device is not sufficiently decoupled on chip from the high current outputs, internal threshold problems can occur. This phenomenon is commonly known as 'dynamic threshold.' It is usually evidenced by glitches appearing on the outputs of a fast, high current drive logic device as it switches high or low. This is most severe on 'ACT' devices which have high current and high slew rate CMOS outputs along with TTL inputs which have low noise immunity. This problem can be minimized by decoupling the internal ground and V_{CC} supplies on-chip and in the package. This decoupling is accomplished by having separate 'quiet' ground and V_{CC} pads on chip which supply the input circuitry's ground and V_{CC} references. These pads are then tied to extra 'quiet' ground and 'quiet' V_{CC} pins on the package, or to special 'split leads' which resemble a tuning fork and utilize the leadframe inductance to accomplish the decoupling. When choosing a clock source, make sure that the part has one of these decoupling schemes.

References

1. Blood, William R., *MECL System Design Handbook*, Motorola Inc., 1983.
2. Application Note AN1051, *Transmission Line Effects in PCB Applications*, Motorola Inc., 1990.
3. *Motorola FACT Data Book* DL138, Motorola Inc., 1990.

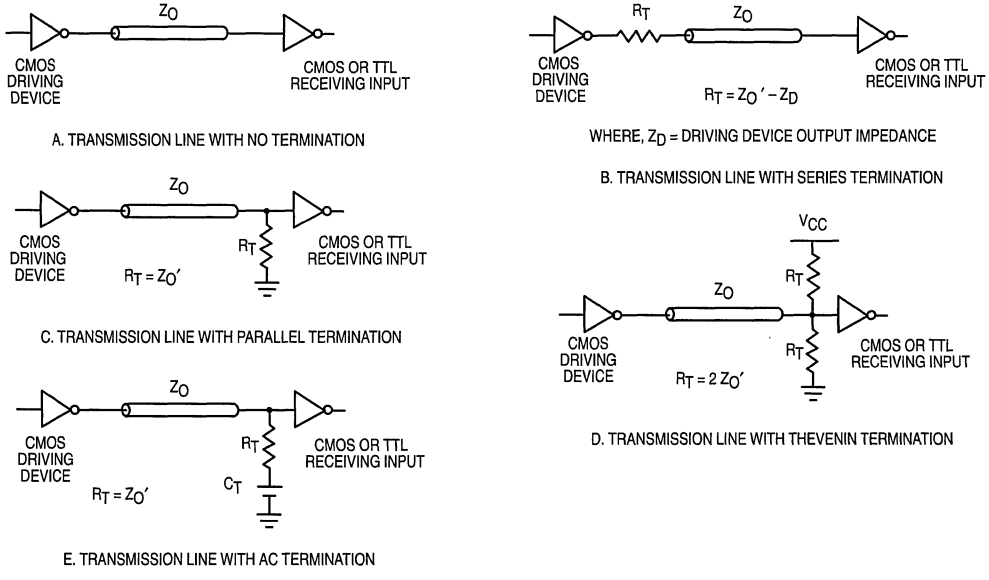


Figure 5. Schematic Representation of Common Termination Techniques

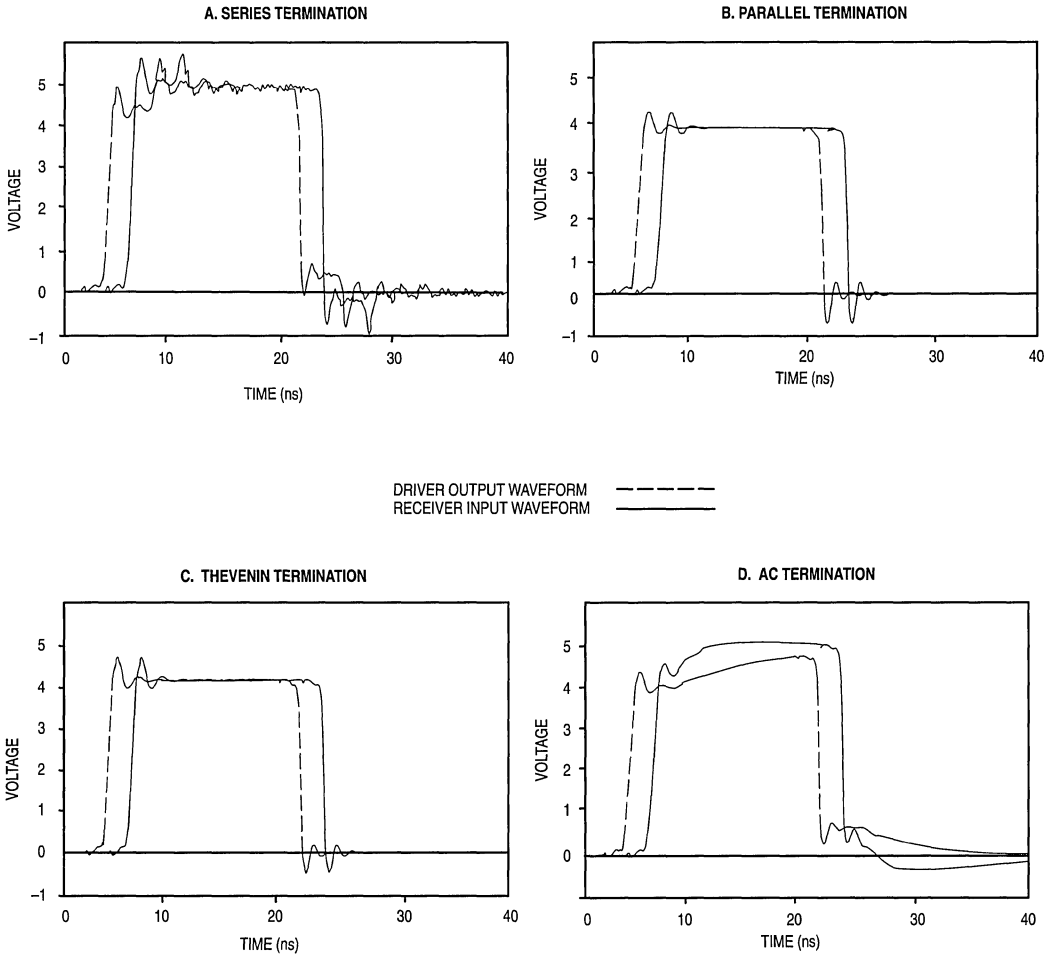


Figure 6. SPICE Simulation Results for Various Terminations of a 9-Inch 41Ω Transmission Line. Simulations Were Run with Typical Model Parameters @ 25°C and V_{CC} = 5.0V

AN1405
Application Note

ECL Clock Distribution Techniques

Prepared by
Todd Pearson
ECL Applications Engineering

This application note provides information on system design using ECL logic technologies for reducing system clock skew over the alternative CMOS and TTL technologies.

ECL Clock Distribution Techniques

INTRODUCTION

The ever increasing performance requirements of today's systems has placed an even greater emphasis on the design of low skew clock generation and distribution networks. Clock skew, the difference in time between "simultaneous" clock transitions within a system, is a major component of the constraints which form the upper bound for the system clock frequency. Reductions in system clock skew allow designers to increase the performance of their designs without having to resort to more complicated architectures or more costly, faster logic. ECL logic technologies offer a number of advantages for reducing system clock skew over the alternative CMOS and TTL technologies.

SKEW DEFINITIONS

The skew introduced by logic devices can be divided into three parts: duty cycle skew, output-to-output skew and part-to-part skew. Depending on the specific application, each of the three components can be of equal or overriding importance.

Duty Cycle Skew

The duty cycle skew is a measure of the difference between the T_{PLH} and T_{PHL} propagation delays (Figure 1). Because differences in T_{PLH} and T_{PHL} will result in pulse width distortion the duty cycle skew is sometimes referred to as pulse skew. Duty cycle skew is important in applications where timing operations occur on both edges or when the duty cycle of the clock signal is critical. The later is a common requirement when driving the clock inputs of advanced microprocessors.

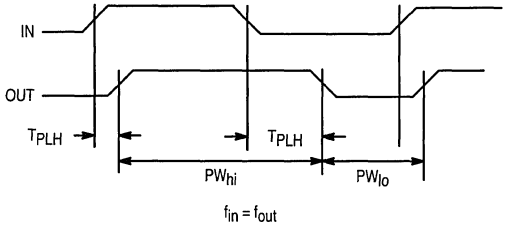


Figure 1. Duty Cycle Skew

Output-to-Output Skew

Output-to-output skew is defined as the difference between the propagation delays of all the outputs of a device. A key constraint on this measurement is the requirement that the output transitions are identical, therefore if the skew between all edges produced by a device is important the output-to-output skew would need to be added to the duty cycle skew to get the total system skew. Typically the output-to-output skew will be smaller than the duty cycle skew for TTL and CMOS devices. Because of the near zero duty cycle skew of a differential ECL device the output-to-output skew will generally be larger. The output-to-output skew is important in systems where either a single device can provide all of the necessary clocks or for the first level device of a nested clock distribution tree. In these two situations the only parameter of importance will be the relative position of each output with respect to the other outputs on that die. Since these outputs will all see the same environmental and process conditions the skew will be significantly less than the propagation delay windows specified in the standard device data sheet.

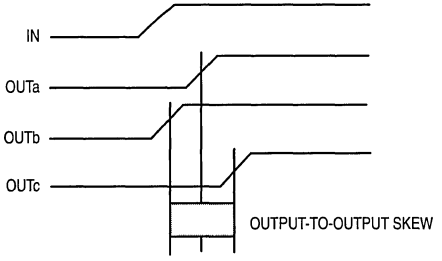


Figure 2. Output-to-Output Skew

Part-to-Part Skew

The part-to-part skew specification is by far the most difficult performance aspect of a device to minimize. Because the part-to-part skew is dependent on both process variations and variations in the environment the resultant specification is significantly larger than for the other two components of skew. Many times a vendor will provide subsets of part-to-part skew specifications based on non-varying environmental conditions. Care should be taken in reading data sheets to fully understand the conditions under which the specified limits are guaranteed. If the part-to-part skew is specified and is different than the specified propagation delay window for the device one can be assured there are constraints on the part-to-part skew specification.

Power supply and temperature variations are major contributors to variations in propagation delays of silicon devices. Constraints on these two parameters are commonly seen in part-to-part skew specifications. Although there are situations where the power supply variations could be ignored, it is difficult for this author to perceive of a realistic system whose devices are all under identical thermal conditions. Hot spots on boards or cabinets, interruption in air flow and variations in IC density of a board all lead to thermal gradients within a system. These thermal gradients will guarantee that devices in various parts of the system are under different junction temperature conditions. Although it is unlikely that a

designer will need the entire commercial temperature range, a portion of this range will need to be considered. Therefore, a part-to-part skew specified for a single temperature is of little use, especially if the temperature coefficient of the propagation delay is relatively large.

For designs whose clock distribution networks lie on a single board which utilizes power and ground planes an assumption of non-varying power supplies would be a valid assumption and a specification limit for a single power supply would be valuable. If, however, various pieces of the total distribution tree will be on different boards within a system there is a very real possibility that each device will see different power supply levels. In this case a specification limit for a fixed V_{CC} will be inadequate for the design of the system. Ideally the data sheets for clock distribution devices should include information which will allow designers to tailor the skew specifications of the device to their application environment.

SYSTEM ADVANTAGES OF ECL

Skew Reductions

ECL devices provide superior performance in all three areas of skew over their TTL or CMOS competitors. A skew reducing mechanism common to all skew parameters is the faster propagation delays of ECL devices. Since, to some extent, all skew represent a percentage of the typical delays faster delays will usually mean smaller skews. ECL devices, especially clock distribution devices, can be operated in either single-ended or differential modes. To minimize the skew of these devices the differential mode of operation should be used, however even in the single-ended mode the skew performance will be significantly better than for CMOS or TTL drivers.

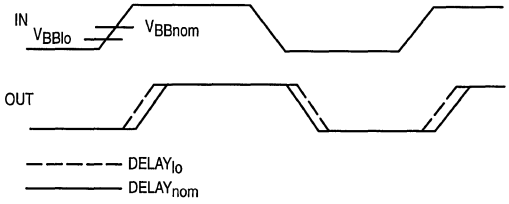


Figure 3. V_{BB} Induced Duty Cycle Skew

ECL output buffers inherently show very little difference between T_{PLH} and T_{PHL} delays. What differences one does see are due mainly to switching reference levels which are not ideally centered in the input swing (see Figure 3). For worst case switching reference levels the pulse skew of an ECL device will still be less than 300ps. If the ECL device is used differentially the variation in the switching reference will not impact the duty cycle skew as it is not used. In this case the pulse skew will be less than 50ps and can generally be ignored in all but the highest performance designs. The problem of generating clocks which are capable of meeting the duty cycle requirements of the most advanced microprocessors, would be a trivial task if differential ECL compatible clock inputs were used. TTL and CMOS clock drivers on the other hand have inherent differences between the T_{PLH} and T_{PHL} delays in addition to the problems with non-centered switching thresholds. In devices specifically designed to minimize this parameter it generally cannot be guaranteed to anything less than 1ns.

The major contributors to output-to-output skew is IC layout and package choice. Differences in internal paths and paths through the package generally can be minimized regardless of the silicon technology utilized at the die level, therefore ECL devices offer less of an advantage in this area than for other skew parameters. CMOS and TTL output performance is tied closely to the power supply levels and the stability of the power busses within the chip. Clock distribution trees by definition always switch simultaneously, thus creating significant disturbances on the internal power busses. To alleviate this problem multiple power and ground pins are utilized on TTL and CMOS clock distribution devices. However even with this strategy TTL and CMOS clock distribution devices are limited to 500ps – 700ps output-to-output skew guarantees. With differential ECL outputs very little if any noise is generated and coupled onto the internal power supplies. This coupled with the faster propagation delays of the output buffers produces output-to-output skews on ECL clock chips as low as 50ps.

Two aspects of ECL clock devices will lead to significantly smaller part-to-part skews than their CMOS and TTL competitors: faster propagation delays and delay insensitivity to environmental variations. Variations in propagation delays with process are typically going to be based on a percentage of the typical delay of the device. Assuming this percentage is going to be approximately equivalent between ECL, TTL and CMOS processes, the faster the device the smaller the delay variations. Because state-of-the-art ECL devices are at least 5 times faster than TTL and CMOS devices, the expected delay variation would be one fifth those of CMOS and TTL devices without even considering environmental dependencies.

The propagation delays of an ECL device are insensitive to variations in power supply while CMOS and TTL device propagation delays vary significantly with changes in this parameter. Across temperature the percentage variation for all technologies is comparable, however, again the faster propagation delays of ECL will reduce the magnitude of the variation. Figure 4 on the following page represents normalized propagation delay versus temperature and power supply for the three technologies.

Low Impedance Line Driving

The clock requirements of today's systems necessitate an almost exclusive use of controlled impedance interconnect. In the past this requirement was unique to the performance levels associated with ECL technologies, and in fact precluded its use in all but the highest performance systems. However the high performance CMOS and TTL clock distribution chips now require care in the design and layout of PC boards to optimize their performance, with this criteria established the migration from these technologies to ECL is simplified. In fact, the difficulties involved in designing with these "slower" technologies in a controlled impedance environment may even enhance the potential of using ECL devices as they are ideally suited to the task.

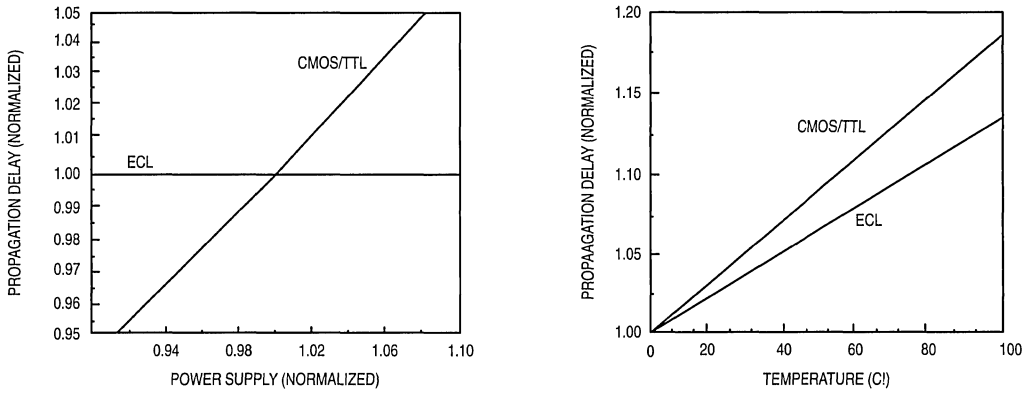


Figure 4. T_{PD} vs Environmental Condition Comparison

The low impedance outputs and high impedance inputs of an ECL device are ideal for driving 50Ω to 130Ω controlled impedance transmission lines. The specified driving impedance of ECL is 50Ω, however this value is used only for convenience sake due to the 50Ω impedance of most commonly used measurement equipment. Utilizing higher impedance lines will reduce the power dissipated by the termination resistors and thus should be considered in power sensitive designs. The major drawback of higher impedance lines (delays more dependent on capacitive loading) may not be an issue in the point to point interconnect scheme generally used in low skew clock distribution designs.

Differential Interconnect

The device skew minimization aspects of differential ECL have already been discussed however there are other system level advantages that should be mentioned. Whenever clock lines are distributed over long distances the losses in the line and the variations in power supply upset the ideal relationship between input voltages and switching thresholds. Because differential interconnect "carries" the switching threshold information from the source to the load the relationship between the two is less likely to be changed. In addition for long lines the smaller swings of an ECL device produce much lower levels of cross-talk between adjacent lines and minimizes EMI radiation from the PC board.

There is a cost associated with fully differential ECL, more pins for equivalent functions and more interconnect to be laid on a typically already crowded PC board. The first issue is really a non-issue for clock distribution devices. The output-to-output and duty cycle skew are very much dependent on quiet internal power supplies. Therefore the pins sacrificed for the complimentary outputs would otherwise have to be used as power supply pins, thus functionality is actually gained for an equivalent pin count as the inversion function is also available on a differential device. The presence of the inverted signal could be invaluable for a design which clocks both off the positive and negative edges. Figure 5 shows a method of obtaining very low skew (<50ps) 180° shifted two phase clocks.

It is true that differential interconnect requires more signals to be routed on the PC board. Fortunately with the wide data and address buses of today's designs the clock lines represent a small fraction of the total interconnect. The final choice as to whether or not to use differential interconnect lies in the level of skew performance necessary for the design. It should be noted that although single-ended ECL provides less attractive skew performance than differential ECL, it does provide significantly better performance than equivalent CMOS and TTL functions.

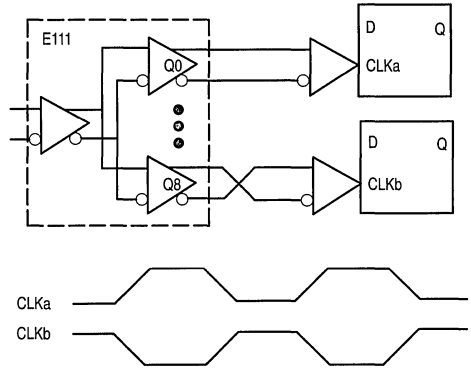


Figure 5. 180° Shifted Two Phase Clocks

USING ECL WITH POSITIVE SUPPLIES

It is hard to argue with the clock distribution advantages of ECL presented thus far, but it may be argued that except for all ECL designs it is too costly to include ECL devices in the distribution tree. This claim is based on the assumption that at least two extra power supplies are required; the negative V_{EE} supply and the negative V_{TT} termination voltage. Fortunately both these assumptions are false. PECL (Positive ECL) is an acronym which describes using ECL devices with a positive

rather than negative power supply. It is important to understand that all ECL devices are also PECL devices. By using ECL devices as PECL devices on a +5 volt supply and incorporating termination techniques which do not require a separate termination voltage (series termination, thevenin equivalent) ECL can be incorporated in a CMOS or TTL design with no added cost.

The reason for the choice of negative power supplies as standard for ECL is due to the fact that all of the output levels and internal switching bias levels are referenced to the V_{CC} rail. It is generally easier to keep the grounds quieter and equal potential throughout a system than it is with a power supply. Because the DC parameters are referenced to the V_{CC} rail any disturbances or voltage drops seen on V_{CC} will translate 1:1 to the output and internal reference levels. For this reason when communicating with PECL between two boards it is recommended that only differential interconnect be used. By using differential interconnect V_{CC} variations within the specified range will not in any way affect the performance of the device.

Finally mentioning ECL to a CMOS designer invariably conjures up visions of space heaters as their perception of ECL is high power. Although it is true that the static power of ECL is higher than for CMOS the dynamic power differences between the technologies narrows as the frequency increases. As can be seen in Figure 6 at frequencies as low as 20MHz the per gate power of ECL is actually less than for CMOS. Since clock distribution devices are never static it does not make sense to compare the power dissipation of the two technologies in a static environment.

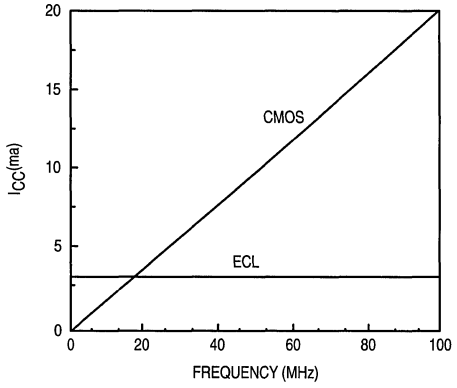


Figure 6. ICC/Gate vs Frequency Comparison

MIXED SIGNAL CLOCK DISTRIBUTION

ECL Clock Distribution Networks

Clock distribution in a ECL system is a relatively trivial matter. Figure 7 illustrates a two level clock distribution tree which produces nine differential ECL clocks on six different cards. The ECLinPS E211 device gives the flexibility of disabling each of the cards individually. In addition the synchronous registered enables will disable the device only when the clock is already in the LOW state, thus avoiding the problem of generating runt pulses when an asynchronous disable is used. The device also provides a muxed clock input for incorporating a high speed system clock and a lower speed test or scan clock within the same distribution tree. The ECLinPS E111 device is used to receive the signals from the backplane and distribute it on the card. The worst case skew between all 54 clocks in this situation would be 275ps assuming that all the loads and signal traces are equalized.

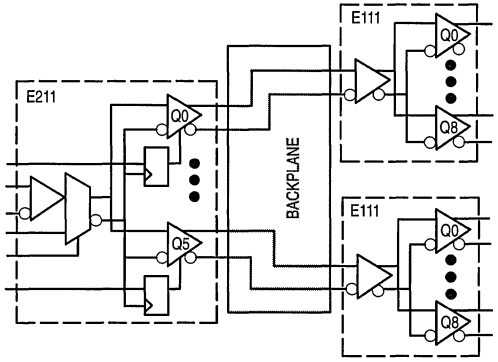


Figure 7. ECL Clock Distribution Tree

Mixed Technology Distribution Networks

Building clock networks in TTL and CMOS systems can be a little more complicated as there are more alternatives available. For simple one level distribution trees fanout devices like the MECL 10H645 1:9 TTL to TTL fanout tree can be used. However as the number of levels of fanout increases the addition of ECL devices in an other wise TTL or CMOS system becomes attractive. In Figure 8 on the next page an E111 device is combined with a MECL H641 device to produce 81 TTL level clocks. Analyzing the skew between the 81 clocks yields a worst case skew, allowing for the full temperature and V_{CC} range variation, of 1.25ns. Under ideal situations, no variation in temperature or V_{CC} supply, the skew would be only 750ps. When compared with distribution trees utilizing only TTL or CMOS technologies these numbers represent ≈50% improvement, more if the environmental conditions vary to any degree. For a 50MHz clock the total skew between the 81 TTL clocks is less than 6.5% of the clock period, thus providing the designer extra margin for layout induced skew to meet the overall skew budget of the design.

Many designers have already realized the benefits of ECL clock distribution trees and thus are implementing them in their designs. Furthermore where they have the capability, i.e. ASICs, they are building their VLSI circuits with ECL compatible clock inputs. Unfortunately other standard VLSI circuits such as microprocessors, microprocessor support chips and memory still cling to TTL or CMOS clock inputs. As a result many systems need both ECL and TTL clocks within the same system. Unlike the situation outlined in Figure 8 the ECL levels are not merely intermediate signals but rather are

driving the clock inputs of the logic. As a result the ECL edges need to be matched with the TTL edges as pictured in Figure 9.

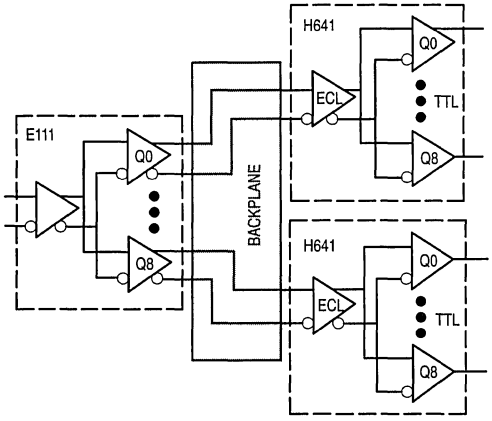


Figure 8. ECL to TTL Clock Distribution

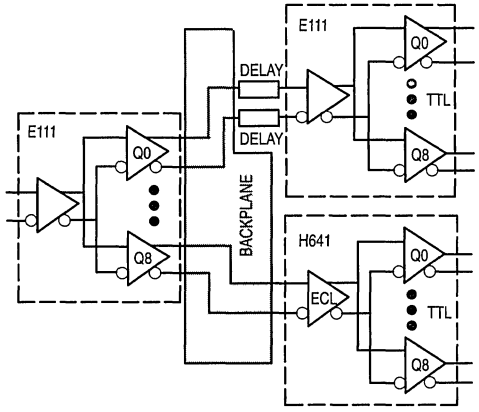


Figure 9. Mixed ECL and TTL Distribution

An ECL clock driver will be significantly faster than a TTL or CMOS equivalent function. Therefore to de-skew the ECL and TTL signals of Figure 9 a delay needs to be added to the input of the ECL device. Because a dynamic delay adjust would not lend itself to most production machines a static delay would be used. The value of the delay element would be a best guess estimate of the differences in the two propagation delays. It is highly unlikely that the temperature coefficients of the propagation delays of the ECL devices, TTL devices and delay devices would be equal. Although these problems will add skew to the system, the resultant total skew of the distribution network will be less than if no ECL chips were used.

PLL Based Clock Drivers

A potential solution for the problem outlined in Figure 9 is in the use of phase locked loop based clock distribution chips. Because these devices feedback an output and lock it to a reference clock input the delay differences between the various technology output buffers will be eliminated. One might believe that with all of the euphoria surrounding the performance of PLL based clock distribution devices that the need for any ECL in the distribution tree will be eliminated. However when analyzed further the opposite appears to be the case.

For a single board design with a one level distribution system there obviously is no need for ECL. When, however, a multiple board system is required where nested levels of devices are needed ECL once again becomes useful. One major aspect of part-to-part skew for PLL based clock chips often overlooked is the dependence on the skew of the various reference clocks being locked to. As can be seen in Figure 10 the specified part-to-part skew of the device would necessarily need to be added to the reference clock skew to get the overall skew of the clock tree. From the arguments presented earlier this skew will be minimized if the reference clock is distributed in ECL. It has not been shown as of yet where a PLL based ECL clock distribution chip can provide the skew performance of the simple fanout buffer. From a system standpoint the buffer type circuits are much easier to design with and thus given equivalent performance would represent the best alternative. The extra features provided by PLL based chips could all be realized if they were used in only the final stage of the distribution tree.

The MPC973 is a PLL based clock driver which features differential PECL reference clock inputs. When combined with the very low skew MC10E111 fanout buffer, very low skew clock trees can be realized for multiprocessor MPP designs. There will be a family of devices featuring various technology compatible inputs and outputs to allow for the building of precisely aligned clock trees based on either ECL, TTL, CMOS or differential GTL (or a mixture of all four) compatible levels.

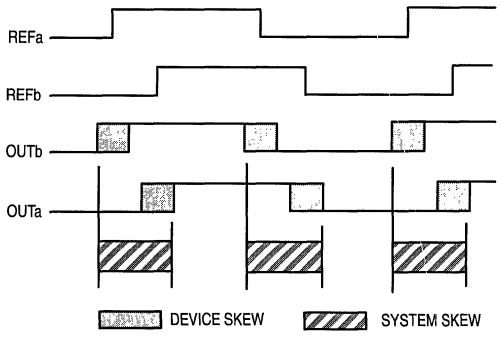


Figure 10. System Skew For PLL Clock Distribution

Conclusion

The best way to maximize the performance of any synchronous system is to spend the entire clock period performing value added operations. Obviously any portion of the clock period spent idle due to clock skew limits the potential performance of the system. Using ECL technology devices in clock distribution networks will minimize all aspects of skew and thus maximize the performance of a system. Unfortunately the VLSI world is not yet ECL clock based so that the benefits of a totally ECL based distribution tree cannot be realized for many systems. However there are methods of incorporating ECL into the intermediate levels of the tree to significantly reduce the overall skew. In addition the system designers can utilize their new found knowledge to incorporate ECL compatible clocks on those VLSI chips of which they have control while at the same time pressuring other VLSI vendors in doing the same so that future designs can enjoy fully the advantages of distributing clocks with ECL.

AN1406
Application Note

Designing With PECL (ECL at +5.0V)

Prepared by
Cleon Petty
Todd Pearson
ECL Applications Engineering

This application note provides detailed information on designing with Positive Emitter Coupled Logic (PECL) devices.

MOTOROLA

Designing With PECL (ECL at +5.0V)
The High Speed Solution for the CMOS/TTL Designer

Introduction

PECL, or Positive Emitter Coupled Logic, is nothing more than standard ECL devices run off of a positive power supply. Because ECL, and therefore PECL, has long been the "black magic" of the logic world many misconceptions and falsehoods have arisen concerning its use. However, many system problems which are difficult to address with TTL or CMOS technologies are ideally suited to the strengths of ECL. By breaking through the wall of misinformation concerning the use of ECL, the TTL and CMOS designers can arm themselves with a powerful weapon to attack the most difficult of high speed problems.

It has long been accepted that ECL devices provide the ultimate in logic speed; it is equally well known that the price for this speed is a greater need for attention to detail in the design and layout of the system PC boards. Because this requirement stems only from the speed performance aspect of ECL devices, as the speed performance of any logic technology increases these same requirements will hold. As can be seen in Table 1 the current state-of-the-art TTL and CMOS logic families have attained performance levels which require controlled impedance interconnect for even relatively short distances between source and load. As a result system designers who are using state-of-the-art TTL or CMOS logic are already forced to deal with the special requirements of high speed logic; thus it is a relatively small step to extend their thinking from a TTL and CMOS bias to include ECL devices where their special characteristics will simplify the design task.

Table 1. Relative Logic Speeds

Logic Family	Typical Output Rise/Fall	Maximum Open Line Length (L_{max})*
10KH	1.0ns	3"
ECLinPS	400ps	1"
FAST	2.0ns	6"
FACT	1.5ns	4"

* Approximate for stripline interconnect ($L_{max} = T_r/2T_{pd}$)

System Advantages of ECL

The most obvious area to incorporate ECL into an otherwise CMOS/TTL design would be for a subsystem which requires very fast data or signal processing. Although this is the most obvious it may also be the least common. Because of the need for translation between ECL and CMOS/TTL technologies the performance gain must be greater than the overhead required to translate back and forth between technologies. With typical delays of six to seven nanoseconds for translating between technologies, a significant portion of the logic would need to be realized using ECL for the overall system performance to improve. However, for very high speed subsystem requirements ECL may very well provide the best system solution.

Transmission Line Driving

Many of the inherent features of an ECL device make it ideal for driving long, controlled impedance lines. The low impedance of the open emitter outputs and high input impedance of any standard ECL device make it ideally suited for driving controlled impedance lines. Although designed to drive 50Ω lines an ECL device is equally adept at driving lines of impedances of up to 130Ω without significant changes in the AC characteristics of the device. Although some of the newer CMOS/TTL families have the ability to drive 50Ω lines many require special driver circuits to supply the necessary currents to drive low impedance transmission interconnect. In addition the large output swings and relatively fast output slew rates of today's high performance CMOS/TTL devices exacerbate the problems of crosstalk and EMI radiation. The problems of crosstalk and EMI radiation, along with common mode noise and signal amplitude losses, can be alleviated to a great degree with the use of differential interconnect. Because of their architectures, neither CMOS nor TTL devices are capable of differential communication. The differential amplifier input structure and complimentary outputs of ECL devices make them perfectly suited for differential applications. As a result, for systems requiring signal transmission between several boards, across relatively large distances, ECL devices provide the CMOS/TTL designer a means of ensuring reliable transmission while minimizing EMI radiation and crosstalk.

Figure 1 shows a typical application in which the long line driving, high bandwidth capabilities of ECL can be utilized. The majority of the data processing is done on wide bit width words with a clock cycle commensurate with the bandwidth capabilities of CMOS and TTL logic. The parallel data is then serialized into a high bandwidth data stream, a bandwidth which requires ECL technologies, for transmission across a long line to another box or machine. The signal is received differentially and converted back to relatively low speed parallel data where it can be processed further in CMOS/TTL logic. By taking advantage of the bandwidth and line driving capabilities of ECL the system minimizes the number of lines required for interconnecting the subsystems without sacrificing the overall performance. Furthermore by taking advantage of PECL this application can be realized with a single five volt power supply. The configuration of Figure 1 illustrates a situation where the mixing of logic technologies can produce a design which maximizes the overall performance while managing power dissipation and minimizing cost.

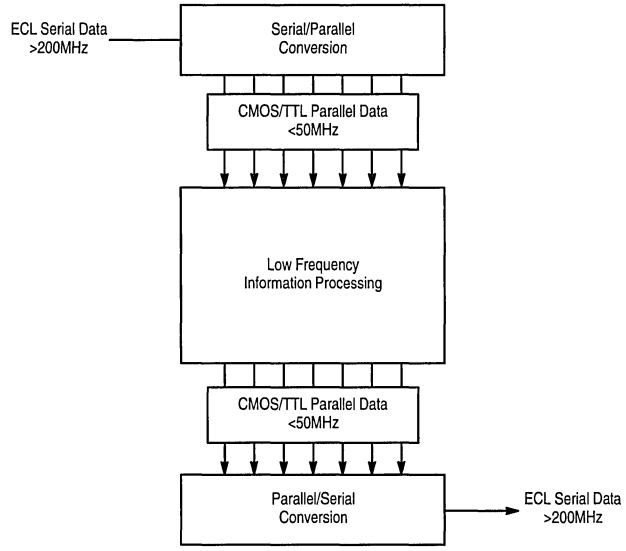


Figure 1. Typical Use of ECL's High Bandwidth, Line Driving Capabilities

Clock Distribution

Perhaps the most attractive area for ECL in CMOS/ TTL designs is in clock distribution. The ever increasing performance capabilities of today's designs has placed an even greater emphasis on the design of low skew clock generation and distribution networks. Clock skew, the difference in time between "simultaneous" clock transitions throughout an entire system, is a major component of the constraints which form the upper bound for the system clock frequency. Reductions in system clock skew allow designers to increase the performance of their designs without having to resort to more complicated architectures or costly, faster logic. ECL logic has the capability of significantly reducing the clock skew of a system over an equivalent design utilizing CMOS or TTL technologies.

The skew introduced by a logic device can be broken up into three areas; the part-to-part skew, the within-part skew and the rise-to-fall skew. The part-to-part skew is defined as the differences in propagation delays between any two devices while the within-device skew is the difference between the propagation delays of similar paths for a single device. The final portion of the device skew is the rise-to-fall skew or simply the differences in propagation delay between a rising input and a failing input on the same gate. The within-device skew and the rise-to-fall skew combine with delay variations due to environmental conditions and processing to comprise the part-to-part skew. The part-to-part skew is defined by the propagation delay window described in the device data sheets.

Careful attention to die layout and package choice will minimize within-device skew. Although this minimization is independent of technology, there are other characteristics of ECL which will further reduce the skew of a device. Unlike their CMOS/TTL counterparts, ECL devices are relatively insensitive to variations in supply voltage and temperature. Propagation delay variations with environmental conditions must be accounted for in the specification windows of a device. As a result because of ECLs AC stability the delay windows for a device will inherently be smaller than similar CMOS or TTL functions.

The virtues of differential interconnect in line driving have already been addressed, however the benefits of differential interconnect are even more pronounced in clock distribution. The propagation delay of a signal through a device is intimately tied to the switching threshold of that device. Any deviations of the threshold from the center of the input voltage swing will increase or decrease the delay of the signal through the device. This difference will manifest itself as rise-to-fall skew in the device. The threshold levels for both CMOS and TTL devices are a function of processing, layout, temperature and other factors which are beyond the control of the system level designer. Because of the variability of these switching references, specification limits must be relaxed to guarantee acceptable manufacturing yields. The level of relaxation of these specifications increases with increasing logic depth. As the depth of the logic within a device increases the input signal will switch against an increasing number of reference levels; each encounter will add skew when the reference level is not perfectly centered. These relaxed timing windows add directly to the overall system skew. Differential ECL, both internal and external to the die, alleviates this threshold sensitivity as a DC switching reference is no longer required. Without the need for a switching reference the delay windows, and thus system skew, can be significantly reduced while maintaining acceptable manufacturing yields.

What does this mean to the CMOS/TTL designer? It means that CMOS/TTL designers can build their clock generation card and backplane clock distribution using ECL. Designers will not only realize the benefits of driving long lines with ECL but will also be able to realize clock distribution networks with skew specs unheard of in the CMOS/TTL world. Many

specialized functions for clock distribution are available from Motorola (MC10/100E111, MC10/100E211, MC10/100EL11). Care must be taken that all of the skew gained using ECL for clock distribution is not lost in the process of translating into CMOS/TTL levels. To alleviate this problem the MC10/100H646 can be used to translate and fanout a differential ECL input signal into TTL levels. In this way all of the fanout on the backplane can be done in ECL while the fanout on each card can be done in the CMOS/TTL levels necessary to drive the logic.

Figure 2 illustrates the use of specialized fanout buffers to design a CMOS/TTL clock distribution network with minimal skew. With 50ps output-to-output skew of the MC10/100E111 and 1ns part-to-part skew available on the MC10/100H646 or MC10/100H641, a total of 72 or 81 TTL clocks, respectively, can be generated with a worst case skew between all outputs of only 1.05ns. A similar distribution tree using octal CMOS or TTL buffers would result in worst case skews of more than 6ns. This 5ns improvement in skew equates to about 50% of the up/down time of a 50MHz clock cycle. It is not difficult to imagine situations where an extra 50% of time to perform necessary operations would be either beneficial or even a life saver. For more information about using ECL for clock distribution, refer to application note AN1405/D – ECL Clock Distribution Techniques.

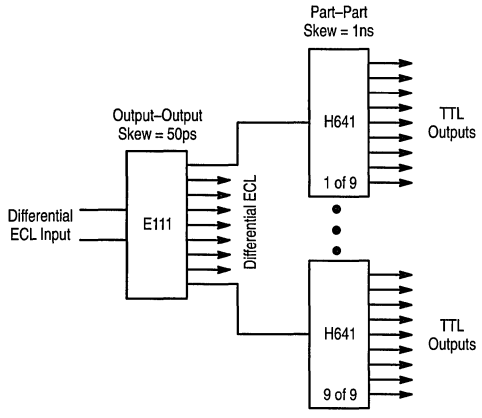


Figure 2. Low Skew Clock Fanout Tree

PECL versus ECL

Nobody will argue that the benefits presented thus far are not attractive, however the argument will be made that the benefits are not enough to justify the requirements of including ECL devices in a predominantly CMOS/TTL design. After all the inclusion of ECL requires two additional negative voltage supplies; V_{EE} and the terminating voltage V_{TT}. Fortunately this is where the advantages of PECL come into play. By using ECL devices on a positive five volt CMOS/TTL power supply and using specialized termination techniques ECL logic can be incorporated into CMOS/TTL designs without the need for additional power supplies. What about power dissipation you ask, although it is true that in a DC state ECL will typically dissipate more power than a CMOS/TTL counterpart, in applications which operate continually at frequency, i.e.. clock distribution, the disparity between ECL and CMOS/TTL power dissipation is reduced. The power dissipation of an ECL device remains constant with frequency while the power of a CMOS/TTL device will increase with frequency. As frequencies approach 50MHz the difference between the power dissipation of a CMOS or TTL gate and an ECL gate will be minimal. 50MHz clock speeds are becoming fairly common in CMOS/TTL based designs as today's high performance MPUs are fast approaching these speeds. In addition, because ECL output swings are significantly less than those of CMOS and TTL the power dissipated in the load will be significantly less under continuous AC conditions.

It is clear that PECL can be a powerful design tool for CMOS/TTL designers, but where can one get these PECL devices. Perhaps the most confusing aspect of PECL is the misconception that a PECL device is a special adaptation of an ECL device. In reality *every* ECL device is also a PECL device; there is nothing magical about the negative voltage supply used for ECL devices. The only real requirement of the power supplies is that the potential difference described in the device data sheets appears across the upper and lower power supply rails (V_{CC} and V_{EE} respectively). A potential stumbling block arises in the specified V_{EE} levels for the various ECL families. The 10H and 100K families specify parametric values for potential differences between V_{CC} and V_{EE} of 4.94V to 5.46V and 4.2V to 4.8V respectively; this poses a problem for the CMOS/TTL designer who works with a typical V_{CC} of 5.0V ±5%. However, because both of these ECL standards are voltage compensated both families will operate perfectly fine and meet all of the performance specifications when operated on standard CMOS/TTL power supplies. In fact, Motorola is extending the V_{EE} specification ranges of many of their ECL families to be compatible with standard CMOS/TTL power supplies. Unfortunately earlier ECL families such as MECL 10K™ are not voltage compensated and therefore any reduction in the potential difference between the two supplies will result in an increase in the V_{OL} level, and thus a decreased noise margin. For the typical CMOS/TTL power supplies a 10K device will experience an ≈50mV increase in the V_{OL} level. Designers should analyze whether this loss of noise margin could jeopardize their designs before implementing PECL formatted 10K using 5.0V ± 5% power supplies.

The traditional choice of a negative power supply for ECL is the result of the upper supply rail being used as the reference for the I/0 and internal switching bias levels of the technology. Since these critical parameters are referenced to the upper rail any noise on this rail will couple 1:1 onto them; the result will be reduced noise margins in the design. Because, in general, it is a simpler task to keep a ground rail relatively noise free, it is beneficial to use the ground rail as this reference. However when careful attention is paid to the power supply design, PECL can be used to optimize system performance. Once again the use of differential PECL will simplify the designer's task as the noise margins of the system will be doubled and any noise riding on the upper V_{CC} rail will appear as common mode noise; common mode noise will be rejected by the differential receiver.

MECL to PECL DC Level Conversion

Although using ECL on positive power supplies is feasible, as with any high speed design there are areas in which special attention should be placed. When using ECL devices with positive supplies the input output voltage levels need to be translated. This translation is a relatively simple task. Since these levels are referenced off of the most positive rail, V_{CC}, the following equation can be used to calculate the various specified DC levels for a PECL device:

PECL Level = V_{CCNEW} – ISpecification LevelI

As an example, the V_{OHMAX} level for a 10H device operating with a V_{CC} of 5.0V at 25°C would be as follows:

PECL Level = 5.0V – I–0.81VI
PECL Level = (5.0 – 0.81)V = 4.19V

The same procedure can be followed to calculate all of the DC levels, including V_{BB} for any ECL device. Table 2 at the bottom of the page outlines the various PECL levels for a V_{CC} of 5.0V for both the 10H and 100K ECL standards. As mentioned earlier any changes in V_{CC} will show up 1:1 on the output DC levels. Therefore any tolerance values for V_{CC} can be transferred to the device I/0 levels by simply adding or subtracting the V_{CC} tolerance values from those values provided in Table 2.

PECL Termination Schemes

PECL outputs can be terminated in all of the same ways standard ECL, this would be expected since an ECL and a PECL device are one in the same. Figure 3 illustrates the various output termination schemes utilized in typical ECL systems. For best performance the open line technique in Figure 3 would not be used except for very short interconnect between devices; the definition of short can be found in the various design guides for the different ECL families. In general for the fastest performance and the ability to drive distributive loads the parallel termination techniques are the best choice. However occasions may arise where a long uncontrolled or variable impedance line may need to be driven; in this case the series termination technique would be appropriate. For a more thorough discourse on when and where to use the various termination techniques the reader is referred to the MECL System Design Handbook (HB205/D) and the design guide in the ECLinPS Databook (DL140/D). The parallel termination scheme of Figure 3 requires an extra V_{TT} power supply for the impedance matching load resistor. In a system which is built mainly in CMOS/TTL this extra power supply requirement may prohibit the use of this technique. The other schemes of Figure 3 use only the existing positive supply and ground and thus may be more attractive for the CMOS/ TTL based machine.

Parallel Termination Schemes

Because the techniques using an extra V_{TT} power supply consume significantly less power, as the number of PECL devices incorporated in the design increases the more attractive the V_{TT} supply termination scheme becomes. Typically ECL is specified driving 50Ω into a –2.0V, therefore for PECL with a V_{CC} supply different than ground the V_{TT} terminating voltage will be V_{CC} – 2.0V. Ideally the V_{TT} supply would track 1:1 with V_{CC}, however in theory this scenario is highly unlikely. To ensure proper operation of a PECL device within the system the tolerances of the V_{TT} and the V_{CC} supplies should be considered. Assume for instance that the nominal case is for a 50Ω load (R_t) into a +3.0V supply; for a 10H compatible device with a V_{OHmax} of –0.81V and a realistic V_{OLmin} of –1 .85V the following can be derived:

$I_{OHmax} = (V_{OHmax} - V_{TT})/R_t$
$I_{OHmax} = (\{5.0 - 0.81\} - 3.0)/50 = 23.8mA$
$I_{OLmin} = (V_{OLmin} - V_{TT})/R_t$
$I_{OLmin} = (\{5.0 - 0.81\} - 3.0)/50 = 3.0mA$

If +5% supplies are assumed a V_{CC} of V_{CCnom} –5% and a V_{TT} of V_{TTnom} +5% will represent the worst case. Under these conditions, the following output currents will result:

$I_{OHmax} = (\{4.75 - 0.81\} - 3.15)/50 = 15.8mA$
$I_{OLmin} = (\{4.75 - 1.85\} - 3.15)/50 = 0mA$

Using the other extremes for the supply voltages yields:

$I_{OHmax} = 31.8mA$
$I_{OLmin} = 11mA$

Table 2. ECL/PECL DC Level Conversion for V_{CC} = 5.0V

	10E Characteristics						100E Characteristics		
	0°C		25°C		85°C		0 to 85°C		
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
V_{OH}	–1.02/3.98	–0.84/4.16	–0.98/4.02	–0.81/4.19	–0.92/4.08	–0.735/4.265	–1.025/3.975	–0.880/4.120	V
V_{OL}	–1.95/3.05	–1.63/3.37	–1.95/3.05	–1.63/3.37	–1.95/3.05	–1.600/3.400	–1.810/3.190	–1.620/3.380	V
V_{OHA}	—	—	—	—	—	—	—	–1.610/3.390	V
V_{OLA}	—	—	—	—	—	—	–1.035/3.965	—	V
V_{IH}	–1.17/3.83	–0.84/4.16	–1.13/3.87	–0.81/4.19	–1.07/3.93	–0.735/4.265	–1.165/3.835	–0.880/4.120	V
V_{IL}	–1.95/3.05	–1.48/3.52	–1.95/3.05	–1.48/3.52	–1.95/3.05	–1.450/3.550	–1.810/3.190	–1.475/3.525	V
V_{BB}	–1.38/3.62	–1.27/3.73	–1.35/3.65	–1.25/3.75	–1.31/3.69	–1.190/3.810	–1.380/3.620	–1.260/3.740	V

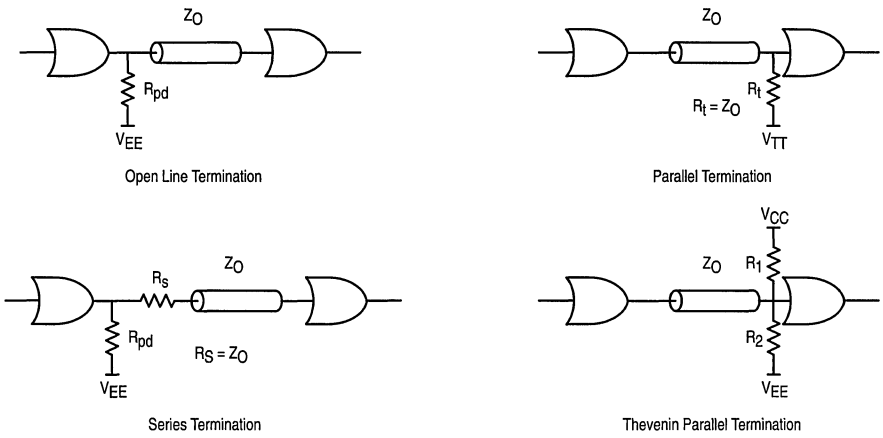


Figure 3. Termination Techniques for ECL/PECL Devices

The changes in the I_{OH} currents will affect the DC V_{OH} levels by ≈±40mV at the two extremes. However in the vast majority of cases the DC levels for ECL devices are well centered in their specification windows, thus this variation will simply move the level within the valid specification window and no loss of worst case noise margin will be seen. The I_{OL} situation on the other hand does pose a potential AC problem. In the worst case situation the output emitter follower could move into the cutoff state. The output emitter followers of ECL devices are designed to be in the conducting "on" state at all times. If cutoff, the delay of the device will be increased due to the extra time required to pull the output emitter follower out of the cutoff state. Again this situation will arise only under a number of simultaneous worst case situations and therefore is highly unlikely to occur, but because of the potential it should not be overlooked.

Thevenin Equivalent Termination Schemes

The Thevenin equivalent parallel termination technique of Figure 3 is likely the most attractive scheme for the CMOS/TTL designer who is using a small amount of ECL. As mentioned earlier this technique will consume more power, however the absence of an additional power supply will more than compensate for the extra power consumption. In addition, this extra power is consumed entirely in the external resistors and thus will not affect the reliability of the IC. As is the case with standard parallel termination, the tolerances of the V_{TT} and V_{CC} supplies should be addressed in the design phase. The following equations provide a means of determining the two resistor values and the resulting equivalent V_{TT} terminating voltage.

$$R1 = R2\ (\{V_{CC} - V_{TT}\}/\{V_{TT} - V_{EE}\})$$
$$R2 = Z_O\ (\{V_{CC} - V_{EE}\}/\{V_{CC} - V_{TT}\})$$
$$V_{TT} = V_{CC}\ (R2/\{R1 + R2\})$$

For the typical setup:

V_{CC} = 5.0V; V_{EE} = GND; V_{TT} = 3.0V; and Z_O = 50Ω

R2 = 50 ({5 – 0}/{5–3}) = 125Ω
R1 = 125 ({5–3}/{3–0}) = 83.3Ω

checking for V_{TT}

V_{TT} = 5 (125/{125 – 83.3}) = 3.0V

Because of the resistor divider network used to generate V_{TT} the variation in V will be intimately tied to the variation in V_{CC}. Differentiating the equation for V_{TT} with respect to V_{CC} yields:

$$dV_{TT}/dV_{CC} = R2/(R1 + R2)\ dV_{CC}$$

Again for the nominal case this equation reduces to:

$$\Delta V_{TT} = 0.6\ \Delta V_{CC}$$

So that for ΔV_{CC} = ±5% = ±0.25V, ΔV_{TT} = ±0.15V.

As mentioned previously the real potential for problems will be if the V_{OL} level can potentially put the output emitter follower into cutoff. Because of the relationship between the V_{CC} and V_{TT} levels the only situation which could present a problem will be for the lowest value of V_{CC}. Applying the equation for I_{OLmin} under this condition yields:

$$I_{OLmin} = (\{V_{OLmin} - V_{TT}\}/R_t$$
$$I_{OLmin} = (\{4.75 - 1.85\} - 2.85)/50 = 1.0mA$$

From this analysis it appears that there is no potential for the output emitter follower to be cutoff. This would suggest that the Thevenin equivalent termination scheme is actually a better design to compensate for changes in V_{CC} due to the fact that these changes will affect V_{TT}, although not 1:1 as would be ideal, in the same way. To make the design even more immune to potential output emitter follower cutoff the designer can design for nominal operation for the worst case situation. Since the designer has the flexibility of choosing the V_{TT} level via the selection of the R1 and R2 resistors the following procedure can be followed.

Let V_{CC} = 4.75V and V_{TT} = V_{CC} – 2.0V = 2.75V
Therefore:

R2 = 119Ω and R1 = 86Ω thus:
I_{OHmax} = 23mA and I_{OLmin} = 3.0mA

Plugging in these values for the equations at the other extreme for V_{CC} = 5.25V yields:

V_{TT} = 3.05V, I_{OHmax} = 28mA and I_{OLmin} = 5.2mA

Although the output currents are slightly higher than nominal, the potential for performance degradation is much less and the results of any degradation present will be significantly less dramatic than would be the case when the output emitter follower is cutoff. Again in most cases the component manufactures will provide devices with typical output levels; typical levels significantly reduces any chance of problems. However it is important that the system designer is aware of where any potential problems may come from so they can be dealt with during the initial design.

Differential ECL Termination

Differential ECL outputs can be terminated using two different strategies. The first strategy is to simply treat the complimentary outputs as independent lines and terminate them as previously discussed. For simple interconnect between devices on a single board or short distances across the backplane this is the most common method used. For interconnect across larger distances or where a controlled impedance backplane is not available the differential outputs can be distributed via twisted pair of ribbon cable (use of ribbon cable assumes every other wire is a ground so that a characteristics impedance will arise). Figure 4 illustrates common termination techniques for twisted pair/ribbon cable applications. Notice that Thevenin equivalent termination techniques can be extended to twisted pair and ribbon cable applications as pictured in Figure 4. However for twisted pair/ribbon cable applications the standard termination technique picture in Figure 4 is somewhat simpler and also does not require a separate termination voltage supply. If however the Thevenin techniques are necessary for a particular application the following equations can be used:

$R1 + R2 = Z_O/2$
$R3 = R1\ (V_{TT} - V_{EE})/(V_{OH} + V_{OL} - 2V_{TT})$
$V_{TT} = (R3\{V_{OH} + V_{OL}\} + R1\{V_{EE}\})/(R1 + 2R3)$

where V_{OH}, V_{OL}, V_{EE} and V_{TT} are PECL voltage levels.

Plugging in the various values for V_{CC} will show that the V_{TT} tracks with V_{CC} at a rate of approximately 0.7:1. Although this rate is approaching ideal it would still behoove the system designer to ensure there are no potential situations where the output emitter follower could become cutoff. The calculations are similar to those performed previously and will not be repeated.

Noise and Power Supply Distribution

Since ECL devices are top rail referenced it is imperative that the V_{CC} rail be kept as noise free and variation free as possible. To minimize the V_{CC} noise of a system liberal bypassing techniques should be employed. Placing a bypass capacitor of 0.01μF to 0.1μF on the V_{CC} pin of every device will help to ensure a noise free V_{CC} supply. In addition when using PECL in a system populated heavily with CMOS and TTL logic the two power supply planes should be isolated as much as possible. This technique will help to keep the large current spike noise typically seen in CMOS and TTL drivers from coupling into the ECL devices. The ideal situation would be multiple power planes; two dedicated to the PECL V_{CC} and ground and the other two to the CMOS/TTL V_{CC} and ground. However if these extra planes are not feasible due to board cost or board thickness constraints common planes with divided subplanes can be used (Figure 5). In either case the planes or sub planes should be connected to the system power via separate paths. Use of separate pins of the board connectors is one example of connecting to the system supplies.

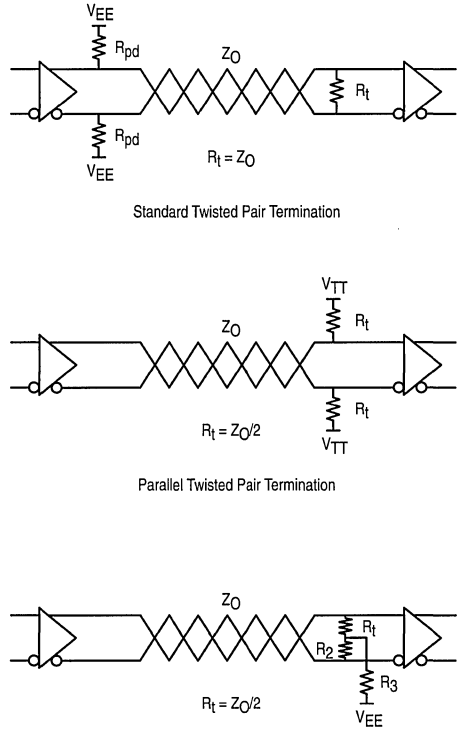


Figure 4. Twisted Pair Termination Techniques

For single supply translators or dual supply translators which share common power pins the package pins should be connected to the ECL V_{CC} and ground planes to ensure the noise introduced to the part through the power plane is minimal. For translating devices with separate TTL and ECL

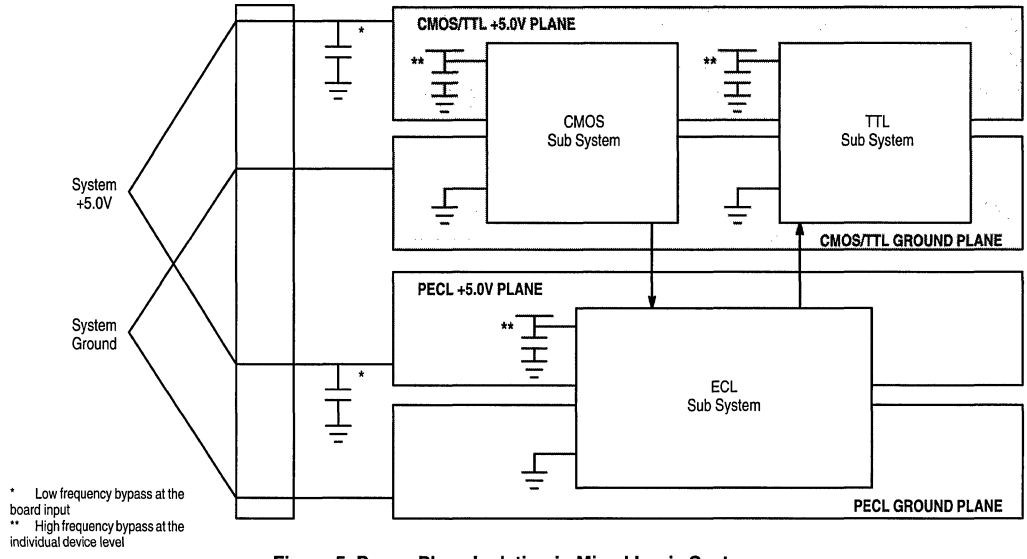


Figure 5. Power Plane Isolation in Mixed Logic Systems

power supply pins, the pins should be tied to the appropriate power planes.

Another concern is the interconnect between two cards with separate connections to the V_{CC} supply. If the two boards are at the opposite extremes of the V_{CC} tolerance, with the driver being at the higher limit and the receiver at the lower limit, there is potential for soft saturation of the receiver input. Soft saturation will manifest itself as degradation in AC performance. Although this scenario is unlikely, again the potential should be examined. For situations where this potential exists there are devices available which are less susceptible to the saturation problem. This variation in V_{CC} between boards will also lead to variations in the input switching references. This variation will lead to switching references which are not ideally centered in the input swing and cause rise/fall skew within the receiving device. Obviously the later skew problem can be eliminated by employing differential interconnect between boards.

When using PECL to drive signals across a backplane, situations may arise where the driver and the receiver are on different power supplies. A potential problem exists if the receiver is powered down independent of the driver. Figure 6 (on the following page) represents a generic driver/receiver pair. From Figure 6, one can see if the receiver is powered down and presents a path to ground through its V_{CC} pin while the driver is still powered at +5.0V the base/collector junction of the input transistor of the receiver will be forward biased and conduct current. Although the collector load resistor will limit the current in the situation of Figure 6, the current may still be enough to damage the junction or exceed the current handling capability of the base electrode metal stripe. Either of these situations could lead to degradation of the reliability of the devices. Because different devices have different ESD protection schemes, and input architectures, the extent of the potential problem will vary from device to device.

Another issue that arises in driving backplanes is situations where the input signals to the receiver are lost and present an open input condition. Many differential input devices will become unstable in this situation, however, most of the newer designs, and some of the older designs, incorporate internal clamp circuitry to guarantee stable outputs under open input conditions. All of the ECLinPS (except for the E111), ECLinPS Lite, and H600 devices, along with the MC10125, 10H125 and 10114 will maintain stable outputs under open input conditions.

Conclusion

The use of ECL logic has always been surrounded by clouds of misinformation; none of those clouds have been thicker than the one concerning PECL. By breaking through this cloud of misinformation the traditional CMOS/TTL designers can approach system problems armed with a complete set of tools. For areas within their designs which require very high speed, the driving of long, low impedance lines or the distribution of very low skew clocks, designers can take advantage of the built in features of ECL. By incorporating this ECL logic using PECL methodologies this inclusion need not require the addition of more power supplies to unnecessarily drive up the cost of their systems. By following the simple guidelines presented here CMOS/TTL designers can truly optimize their designs by utilizing ECL logic in areas in which they are ideally suited. Thus bringing to market products which offer the ultimate in performance at the lowest possible cost.

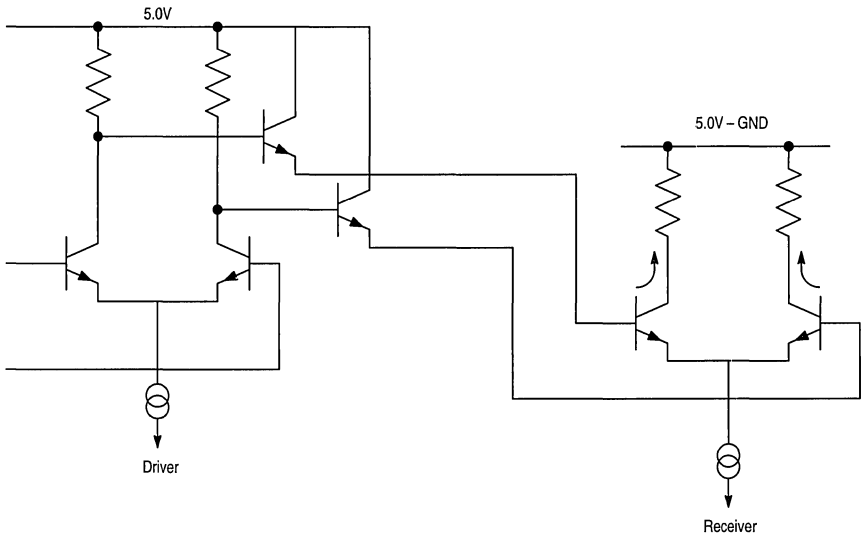


Figure 6. Generic Driver/Receiver Pair

AN1545
Application Note

Thermal Data for MPC Clock Drivers

Prepared by
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Applications Engineering

This application note provides general information on thermal and related reliability issues with respect to the MPC family of clock driver products. In addition, methods are presented to estimate power dissipation and junction temperatures for the MPC product family.

MOTOROLA

Thermal Data for MPC Clock Drivers

Package Choice

The Motorola Timing Solutions products are offered in a variety of surface mount plastic packages. These packages include the 16 and 20 lead SOIC, 20 and 28 lead PLCC and the 32 and 52 lead TQFP packages. The bulk of the newer products are being introduced in the SOIC and TQFP packages with the PLCC being used for the older mature products.

The surface mount plastic packages were selected as the optimum combination of performance, physical size and thermal handling in a low cost standard package. While more exotic packages exist to improve the thermal and electrical performance the cost of these are prohibitive for many applications.

Long Term Failure Mechanisms in Plastic Packages

When analyzing a design for its long term reliability it is important that the dominant failure mechanisms are well understood. Although today's plastic packages are as reliable as ceramic packages under most environmental conditions, as the junction temperature increases a failure mode unique to plastic packages becomes a significant factor in the long term reliability of the device.

Modern plastic package assembly utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. Because plastic packages use injection molding the bond wires used must be extremely ductile to keep from breaking or being pulled from the bond pad during the injection process. Gold wire has far better ductility than aluminum wire and therefore is used in the process of plastic packaging. Aluminum is the metal used in the majority of low cost digital IC processes for transistor and bond wire interconnect. As the temperature of the silicon (junction temperature) increases an intermetallic forms between the gold and aluminum interface. This intermetallic formation results in a significant increase in the impedance of the wire bond and can lead to performance failure of the affected pin. With this relationship between intermetallic formation and junction temperature established, it is incumbent on the designer to ensure that the junction temperature for which a device will operate is consistent with the long term reliability goals of the system.

Reliability studies were performed at elevated ambient temperatures (125°C) from which an arrhenius equation relating junction temperature to bond failure was established. The application of the equation yields Table 1. This table relates the junction temperature of a device in a plastic package to the continuous operating time before 0.1% bond failure (1 failure per 1000 bonds). Note that this equation only holds for continuous elevated junction temperature levels, as the curve is quite steep if a system cycles through a temperature range but spends a relatively short amount of time at the extreme the numbers provided in this table will grossly underestimate the lifetime of the device based solely on the worst case junction temperature seen.

Table 1. Package Junction Temperatures

Junction Temperature (°C)	Time (Hours)	Time (Years)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.1
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

The Motorola Timing solutions products are designed with chip power levels that permit acceptable reliability levels, in most systems, under conventional 500lfpm (2.5m/s) airflow. However because of their flexibility and programmability there may be some situations where special thermal considerations may be required.

Thermal Management

In any system design proper thermal management is essential to establish the appropriate trade–off between performance, density, reliability and cost. In particular the designer should be aware of the reliability implication of continuously operating semiconductor devices at high junction temperatures.

The increasing popularity of plastic, small outline surface mount packages is putting a greater emphasis on the need for better thermal management of a system. This is due to the fact that the newer SMD packages generally require less board space than their first generation brethren. Thus designs incorporating the latest generation SMD packaging technologies have a higher thermal density. To optimize the thermal management of a system it is imperative that the user understand all of the variables which contribute to the junction temperature of the device.

The variables involved in determining the junction temperature of a device are both supplier and user defined. The supplier, through lead frame design, mold compounds, die size and die attach can positively impact the thermal resistance and thus, the junction temperature of a device. Motorola continually experiments with new package designs and assembly techniques in an attempt to further enhance the thermal performance of its products.

It can be argued that the user has the greatest control of the variables which commonly impact the thermal performance of a device. Ambient temperature, air flow and related cooling techniques are the obvious user controlled variables, however PCB substrate material, layout density, amount of exposed copper and weight of copper used in the power planes can all have significant impacts on the thermal performance of a system.

PCB substrates all have different thermal characteristics, these characteristics should be considered when exploring the PCB alternatives. Users should also account for the different power dissipation of the different devices in their systems and space them accordingly. In this way the heat

load is spread across a larger area and "hot spots" do not appear in the layout. Copper interconnect and power planes act as heat radiators, therefore significant thermal dissipation can be achieved by paying special attention to the copper elements of a PCB. The thermal resistance of copper (package leadframes are made from copper) is significantly lower than that of the epoxy used for the body of plastic packages. As a result the dominant mode of heat flow out of a package is through the leads. By employing techniques at the board level to enhance the transfer of this heat from the package leads to the PCB one can reduce the effective thermal resistance of the plastic package. Copper interconnect traces on the top layer of the PCB are excellent radiators for transferring heat to the ambient air, especially if these traces are exposed to even moderate air flow. In addition using thick copper power planes not only reduces the electrical resistance but also enhances their thermal carrying capabilities. The power planes can be thermally enhanced further by employing special edge connectors which draw the heat from the planes and again dissipate it into the ambient. Finally, the use of thermal conductive epoxies between the underneath of a device and thermal vias to a power plane can accelerate the transfer of heat from the device to the PCB where once again it can more easily be passed to the ambient.

The advent of small outline SMD packaging and the industry push towards smaller, denser designs makes it incumbent on the designer to provide for the removal of thermal energy from the system. Users should be aware that they control many of the variables which impact the junction temperatures and, thus, to some extent, the long term reliability of their designs.

Calculating Junction Temperature

Since the reliability of a device is directly related to junction temperature and that temperature cannot be measured directly there needs to be a means of calculating the approximate junction temperature from measurable parameters. There are two equations which can be used:

$$T_J = T_A + PD\Theta_{JA} \text{ or } T_J = T_C + PD\Theta_{JC}$$

where:

T_J = Junction Temperature
T_A = Ambient Temperature (°C)
T_C = Case Temperature (°C)
PD = Internal Power Dissipation of the Device (W)
Θ_{JA} = Avg Pkg Thermal Resistance (Junction – Ambient)
Θ_{JC} = Avg Pkg Thermal Resistance (Junction – Case)

The Θ_{JC} numbers are determined by submerging a device in a liquid bath and measuring the temperature rise of the bath, it therefore represents an average case temperature. The difficulty in using this method arises in the determination of the case temperature in an actual system The case temperature is a function of the location on the package at which the temperature is measured. Therefore, to use the Θ_{JC} method the case temperature would have to be measured at several different points and averaged to represent the T_C of the device. This in practice could prove difficult and relatively inaccurate. To alleviate this problem manufacturers will sometimes provide a Θ_{Jref} value for a package. This number represents the thermal resistance between the die and a specific spot on the package (usually the top dead center). This measure of thermal resistance typically has a much wider standard deviation than the standard resistance parameters and therefore is sometimes avoided, however it is the most easily measured parameter from which junction temperatures can be calculated.

The Θ_{JA} method of estimating junction temperature is the most widely used. To use this method one need only measure the ambient air temperature in the vicinity of the device in question and calculate the internal power dissipation of that device. The total power dissipation in a device is made up of two parts; the static power and the dynamic power. The two components can be calculated separately and then added together. Another source of power is the termination power as clock drivers are generally used to drive terminated transmission lines. For an ECL output this can be significant however for CMOS outputs the termination load current is pulled through very little voltage (the output HIGH and LOW voltages are very near the rail) so that most of the power is dissipated in the actual load. With this in mind we will address calculating power for ECL and CMOS/BiCMOS separately.

Because clock drivers generally drive transmission lines we will not assume any lumped capacitive load at the outputs. Lumped capacitive loads on outputs add significantly to the power dissipated on chip, when however the capacitive loads are at the the end of transmission lines they are buffered from the driving device and thus do not add to the power dissipation above that attributed to driving the transmission line. Note that for the purpose of power dissipation calculations it is not equivalent to calculate the distributed capacitance of a transmission line and treat it as a lumped load at the output of the device. This technique will significantly overestimate the calculated power of a device.

Calculating Power Dissipation in CMOS/BiCMOS Devices

The total power dissipated in a device can be represented as follows:

$$P_D = I_{CC}(static)*V_{CC} + I_{CC}(dynamic)*V_{CC} + n(I_{OH}*(V_{CC} - V_{OH}) + I_{OL}*(V_{OL}))/2$$

In general rather than using dynamic I_{CC} numbers the dynamic power is calculated using power dissipation capacitance numbers (C_{PD}). Using C_{PD} numbers the above equation becomes:

$$P_D = I_{CC}(static)*V_{CC} + C_{PD}*V_{CC}^2*f + n(I_{OH}*(V_{CC} - V_{OH}) + I_{OL}*(V_{OL}))/2$$

As mentioned previously since the output logic levels are very nearly rail to rail, the third part of the above equation can be ignored. Note that although this assumption may be true for series terminated lines it may not be true for parallel termination where the relatively large DC currents will drive the output voltage levels away from the rails. If we assume series termination then the equation reduces to the following:

$$P_D = I_{CC}(static)*V_{CC} + C_{PD}*V_{CC}^2*f$$

The dynamic dissipation may be a function of the number of outputs switching, if this is the case a CPD number may be provided for each output buffer. In this case the equation would expand to:

$P_D = I_{CC}(static)*V_{CC} + C_{PD}(internal)*V_{CC}^2*f + C_{PD}(output)*V_{CC}^2*f*n$

where n = number of outputs at the given frequency f.

Finally for a CMOS device the $I_{CC}(static) = 0$ and for a BiCMOS device which utilizes ECL gates internal the $C_{PD}(internal) = 0$ so that the equations reduce to:

CMOS $P_D = C_{PD}(internal)*V_{CC}^2*f + C_{PD}(output)*V_{CC}^2*f*n$

BiCMOS $P_D = I_{CC}(static)*V_{CC} + C_{PD}(output)*V_{CC}^2*f*n$

Calculating Power Dissipation in ECL Devices

Starting from the same basic equation:

$P_D = I_{CC}(static)*V_{CC} + I_{CC}(dynamic)*V_{CC} + n(I_{OH}*(V_{CC} - V_{OH}) + I_{OL}*(V_{CC} - V_{OL}))/2$

For ECL devices the the static current is equal to the dynamic current (I_{CC} is independent of frequency) therefore the equation reduces to:

$P_D = I_{CC}*V_{CC} + n(I_{OH}*(V_{CC} - V_{OH}) + I_{OL}*(V_{CC} - V_{OL}))/2$

The above equation assumes a 50% duty cycle on a single ended output and thus takes the average of the high state and low state power dissipation. For differential outputs it is simpler to calculate the power per output pairs. Since the pairs are always in complementary states the output power for the pair is simply the addition of the low state and high state power consumption. The only time one will see a difference between a single ended and differential output calculation is under worst case conditions. For say an 18 single ended output device the worst case condition would be for all 18 to be in the worst case logic state for power dissipation purposes. For a device on the other hand with 9 pairs of complimentary outputs (18 total) only 9 of the outputs can be in the worst case condition at a time so that the worst case power dissipation of a complimentary output device will be less than a device with an equivalent number of single ended outputs.

The only issue left is determining I_{OL} and I_{OH}. These values are a function of the termination technique and the pull down voltage used. The currents are easily calculated based on the V_{OH}/V_{OL} levels the pull down resistance and the pull down voltage used. For a standard termination of 50Ω to a voltage of 2.0V below V_{CC}:

$I_{OH} = (V_{CC} - 0.98) - (V_{CC} - 2.0)/50 = 20.4mA$

$I_{OL} = (V_{CC} - 1.7) - (V_{CC} - 2.0)/50 = 6.0mA$

Thermal Resistance of Plastic Packages

With the power estimates calculated the Θ_{JA} of the appropriate package is the only required parameter left to estimate the junction temperature of a device. The Θ_{JA} number for a package is expressed in °C per Watt (°C/W) and is used to determine the temperature elevation of the die (junction) over the external ambient temperature. Standard lab measurements of this parameter for the various timing solution packages are provided in the graphs of Figure 1 through Figure 3.

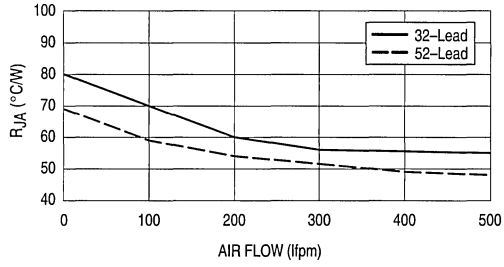


Figure 1. Thermal Resistance of the TQFP Packages

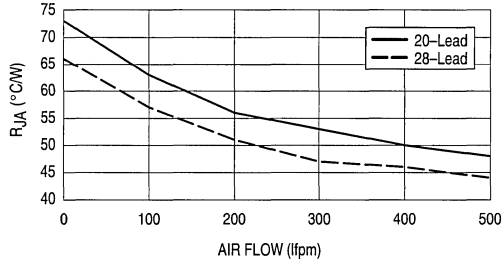


Figure 2. Thermal Resistance of the PLCC Packages

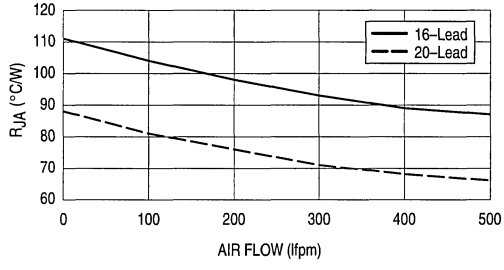


Figure 3. Thermal Resistance of the SOIC Packages

Junction Temperature Calculation Example

As an example the junction temperature of the MPC951 will be calculated. The static I_{CC} of the MPC951 is 95mA and the C_{PD} per output is 25pf. From these numbers the following results:

$P_D = 95mA*3.3V + 3.3V*3.3V*25pf*f*n = 315mW + 2.72e{-}10*f*n$

Assume we will configure all 9 outputs to the same frequency, the curve in Figure 4 shows the power dissipation vs frequency for the MPC951.

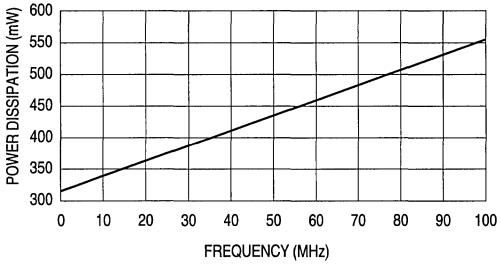


Figure 4. MPC951 Junction Temperature Calculation

Assume that one is building a design with all nine outputs operating at 66MHz. From the graph this corresponds to a power dissipation of 470mW. The MPC951 is packaged in the 32lead TQFP; from the Θ_{JA} chart (assume zero air flow) the thermal resistance of the package is 97°C/W. Plugging these into the T_J equation yields the following:

$T_J = T_A + 80°C/W*0.470W = T_A + 38°C.$

For a worst case ambient temperature of 70°C the resulting junction temperature would be 108°C. From the MTBF table this would correspond to a lifetime of greater than nine years, a lifetime which is well within the requirements of most systems. If however the user needed a little higher performance of 100MHz on the outputs the T_J would be:

$T_J = T_A + 80°C/W*0.555W = T_A + 44°C$

Under these conditions the worst case junction temperature would be 114°C and the worst case lifetime would be approaching 4 years. This may not be a satisfactory lifetime and the user would have to do some thermal management to reduce the junction temperature. Obvious enhancements would be providing airflow or perhaps reducing the maximum ambient specifications. If airflow was added (200lfpm) the junction temperature would reduce to:

$T_J = T_A + 60°C/W * 0.555W = T_A + 33°C$

This drops the junction temperature down into the same range as the 66MHz output case.

The second example will use an ECL output device; the MC100LVE111. The device has 9 differential output pairs and an I_{CC} of 65mA. Assume that the outputs are terminated 50Ω to 2.0V below V_{CC}.

$P_D = 65mA*3.3V + 9((0.98*1.02/50)+(1.7*0.3/50)) =$
$215mW + 270mW = 485mW$

The MC100LVE111 is packaged in the 28lead PLCC; from the Θ_{JA} tables the Θ_{JA} at 500lfpm is 45°C/W. This yield the following approximate junction temperature:

$T_J = T_A + 45°C/W*0.485W = T_A + 22°C$

For a maximum ambient of 70°C the LVE111 exhibits more than satisfactory long term reliability for most systems under standard operating conditions.

Note in both cases the most efficient way to lower the junction temperature is to reduce the ambient temperature of the system. Unit changes in ambient temperature result in unit changes in junction temperature no other parameter is this tightly coupled to junction temperature.

Limitations to Junction Temperature Calculations

The use of the previously described technique for estimating junction temperatures is intimately tied to the measured values of the Θ_{JA} of the package. Since this parameter is a function of not only the package, but also the test fixture the results may not be applicable for every environmental condition. As mentioned previously the Θ_{JA} of a package in a system could be somewhat higher or lower depending on the thermal design of the board.

In addition the reliability numbers derived for the intermetallic formation assumes constant usage at the specific conditions. In the real world devices will not be exposed to worst case conditions continuously but rather will cycle between the worst case and a lower junction temperature. The MTBF table does not take into account this cycling so that simply calculating the worst case junction temperature and applying it to the table directly will significantly underestimate the long term reliability of the device. Because reliability and environmental conditions are statistical in nature it is important that statistical analysis be applied to any long term reliability studies done on the clock driver products.

Low Skew Fanout Buffers

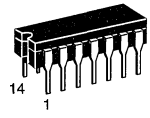
Clock Driver Quad D-Type Flip-Flop
With Matched Propagation Delays

MC74F803

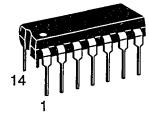
CLOCK DRIVER QUAD D-TYPE FLIP-FLOP WITH MATCHED PROPAGATION DELAYS

The MC74F803 is a high-speed, low-power, quad D-type flip-flop featuring separate D-type inputs, and inverting outputs with closely matched propagation delays. With a buffered clock (CP) input that is common to all flip-flops, the F803 is useful in high-frequency systems as a clock driver, providing multiple outputs that are synchronous. Because of the matched propagation delays, the duty cycles of the output waveforms in a clock driver application are symmetrical within 1.0 to 1.5 nanoseconds.

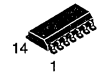
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Matched Outputs for Synchronous Clock Driver Applications
- Outputs Guaranteed for Simultaneous Switching



J SUFFIX
CERAMIC
CASE 632-08

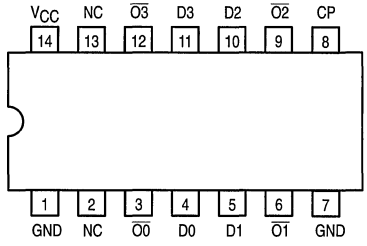


N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-03

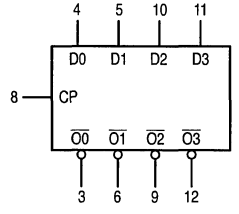
Pinout: 14-Lead Plastic (Top View)



GUARANTEED OPERATION RANGES

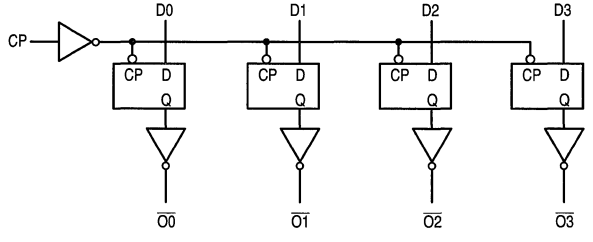
Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High	—	—	–20	mA
I_{OL}	Output Current — Low	—	—	24	mA

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PINS 1 AND 7
NC = PINS 2 AND 13

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The F803 consists of four positive edge-triggered flip-flops with individual D-type inputs and inverting outputs. The buffered clock is common to all flip-flops and the following specifications allow for outputs switching simultaneously. The four flip-flops store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. The maximum frequency of the clock input is 70 megahertz, and the LOW-to-HIGH and HIGH-to-LOW propagation delays of the $\overline{O}_1$ output vary by, at most, 1 nanosecond. Therefore, the device is ideal for use as a divide-by-two driver for high-frequency clock signals that require symmetrical duty cycles. The difference between the LOW-to-HIGH and HIGH-to-LOW propagation delays for the $\overline{O}_0$, $\overline{O}_2$, and $\overline{O}_3$ outputs vary by at most 1.5 nanoseconds. These outputs are very useful as clock drivers for circuits with less stringent requirements. In addition, the output-to-output skew is a maximum of 1.5 nanoseconds. Finally, the I_{OH} specification at 2.5 volts is guaranteed to be at least – 20 milliamps. If their inputs are identical, multiple outputs can be tied together and the I_{OH} is commensurately increased.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions*	
V_{IH}	Input HIGH Voltage	2.0	—	—	V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage	—	—	0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage	—	—	– 1.2	V	I_{IN} = –18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	2.5	—	—	V	I_{OH} = –20 mA	V_{CC} = 4.5 V
V_{OL}	Output LOW Voltage	—	0.35	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
		—	—	20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
I_{IH}	Input HIGH Current	—	—	100		V_{IN} = 7.0 V	V_{CC} = MAX
I_{IL}	Input LOW Current	—	—	–0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)	–60	—	–150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current	—	—	70	mA	V_{CC} = MAX	

* Normal test conditions for this device are all four outputs switching simultaneously. Two outputs of the 74F803 can be tied together and the I_{OH} doubles.

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%, see Note 1)

Symbol	Parameter	C_L = 50 pF Min	Max	C_L = 100 pF Min	Max	Unit
f_{max}	Maximum Clock Frequency	70	—	50	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{On}$	3.0	7.5	3.0	10	ns
t_{Pv}	Propagation Delay CP to $\overline{On}$ Variation (see Note 3)	—	3.0	—	4.0	ns
t_{ps} $\overline{O}_1$	Propagation Delay Skew $\|t_{PLH}$ Actual – t_{PHL} Actual$\|$ for $\overline{O}_1$ Only	—	1.0	—	2.0	ns
t_{ps} $\overline{O}_0$, $\overline{O}_2$, $\overline{O}_3$	Propagation Delay Skew $\|t_{PLH}$ Actual – t_{PHL} Actual$\|$ for $\overline{O}_0$, $\overline{O}_2$, $\overline{O}_3$	—	1.5	—	2.0	ns
t_{os}	Output to Output Skew (see Note 2) $\|t_p$ $\overline{On}$ – t_p $\overline{Om}\|$	—	1.5	—	2.5	ns
t_{rise}, t_{fall} $\overline{O}_1$	Rise/Fall Time for $\overline{O}_1$ (0.8 to 2.0 V)	—	3.0	—	4.0	ns
t_{rise}, t_{fall} $\overline{O}_0$, $\overline{O}_2$, $\overline{O}_3$	Rise/Fall Time for $\overline{O}_0$, $\overline{O}_2$, $\overline{O}_3$ (0.8 to 2.0 V)	—	3.5	—	4.5	ns

1. The test conditions used are all four outputs switching simultaneously. The AC characteristics described above (except for $\overline{O}_1$) are also guaranteed when two outputs are tied together.
2. Where t_p $\overline{On}$ and t_p $\overline{Om}$ are the actual propagation delays (any combination of high or low) for two separate outputs from a given high transition of CP.
3. For a given set of conditions (i.e., capacitive load, temperature, V_{CC}, and number of outputs switching simultaneously) the variation from device to device is guaranteed to be less than or equal to the maximum.

AC OPERATING REQUIREMENTS (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%)

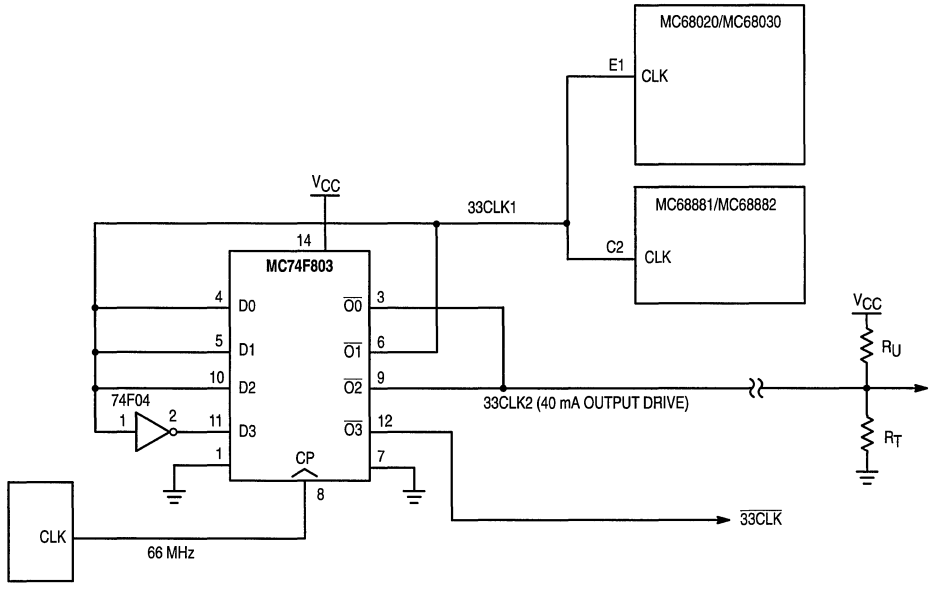
Symbol	Parameter	C_L = 50 pF		C_L = 100 pF		Unit
		Min	Max	Min	Max	
$t_{s(H)}$ $t_{s(L)}$	Setup Time, HIGH or LOW D_n to CP	3.0 3.0	— —	4.0 4.0	— —	ns
t_f	$t_p + t_s$ (see Note)	—	9.0	—	12	ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW D_n to CP	2.0 2.0	— —	2.0 2.0	— —	ns
$t_{w(H)}$ $t_{w(L)}$	CP Pulse Width HIGH or LOW	7.0 6.0	— —	8.0 8.0	— —	ns

The combination of the setup time (t_s) requirement and maximum propagation delay (t_p) are guaranteed to be within this limit for all conditions.

APPLICATION NOTE

The closely matched outputs of the MC74F803 provide an ideal interface for the clock input of Motorola's high-frequency microprocessors.

74F803 INTERFACE AS CLOCK TO MC68020 SYSTEM



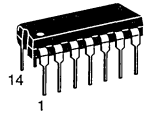
Clock Driver Quad D-Type Flip-Flop
With Matched Propagation Delays

MC74F1803

CLOCK DRIVER QUAD D–TYPE FLIP–FLOP WITH MATCHED PROPAGATION DELAYS

The MC74F1803 is a high–speed, low–power, quad D–type flip–flop featuring separate D–type inputs and inverting outputs with closely matched propagation delays. With a buffered clock (CP) input that is common to all flip–flops, the MC74F1803 is useful in high–frequency systems as a clock driver, providing multiple outputs that are synchronous. Because of the matched propagation delays, the duty cycles of the output waveforms in a clock driver application are symmetrical within 2.0 nanoseconds.

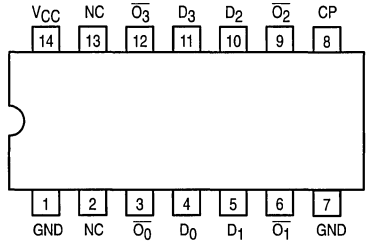
- Edge–Triggered D–Type Inputs
- Buffered Positive Edge–Triggered Clock
- Matched Outputs for Synchronous Clock Driver Applications
- Outputs Guaranteed for Simultaneous Switching



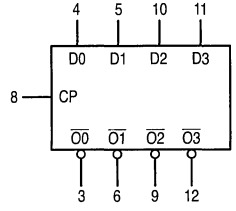
N SUFFIX
PLASTIC
CASE 646–06

D SUFFIX
SOIC
CASE 751A–03

Pinout: 14–Lead Plastic (Top View)

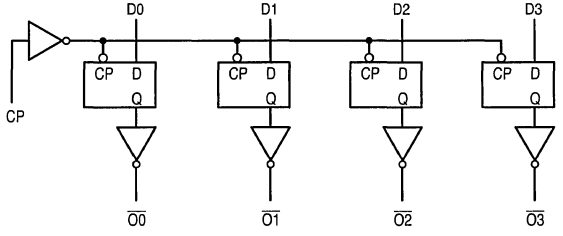


LOGIC SYMBOL



VCC = PIN 14
GND = PINS 1 AND 7
NC = PINS 2 AND 13

LOGIC DIAGRAM



VCC = Pin 14; GND = Pins 1,7; NC = Pins 2, 13

NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays

FUNCTIONAL DESCRIPTION

The MC74F1803 consists of four positive edge–triggered flip–flops with individual D–type inputs and inverting outputs. The buffered clock is common to all flip–flops and the following specifications allow for outputs switching simultaneously. The four flip–flops store the state of their individual D inputs that meet the setup and hold time requirements on the LOW–to–HIGH Clock (CP) transition. The maximum frequency of the clock input is 70 megahertz and the LOW–to–HIGH and HIGH–to–LOW propagation delays of the $\overline{On}$ output vary by at most, 2.0 nanoseconds. Therefore, the device is ideal for use as a divide–by–two driver for high–frequency clock signals that require symmetrical duty cycles. In addition, the output–to–output skew is a maximum of 2.0 nanoseconds. Finally, the I_{OH} specification at 2.5 volts is guaranteed to be at least –20 milli–amps. If their inputs are identical, multiple outputs can be tied together and the I_{OH} is commensurately increased.

GUARANTEED OPERATION RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High	—	—	–20	mA
I_{OL}	Output Current — Low	—	—	24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions [1,2]	
V_{IH}	Input HIGH Voltage		2.0	–	–	V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage		–	–	0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage		–	–	–1.2	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage A_n Outputs	74	2.5	–	–	V	I_{OH} = –20 mA	V_{CC} =4.5 V
V_{OL}	Output LOW Voltage A_n Outputs	74	–	0.35	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current		–	–	20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
			–	–	100	µA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current		–	–	–0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current [3]		–60	–	–150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current		–	–	70	mA	V_{CC} = MAX	

3. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
4. Normal test conditions for this device are all four outputs switching simultaneously. Two outputs of the MC74F1803 can be tied together and the I_{OH} doubles.
5. Not more than one output should be shorted at a time, nor for more than 1 second.

AC OPERATING REQUIREMENTS (T_A = 0°C to +70°C: V_{CC} = +5.0 V ±10%: RL = 500 Ω)

Symbol	Parameter	C_L = 50 pF Min	Max	Unit
t_s(H) t_s(L)	Setup Time, HIGH or LOW: D_n to CP	3.0 3.0	– –	ns
t_f	$t_p + t_s$ [1]	–	9.0	ns
t_h(H) t_h(L)	Hold Time, HIGH or LOW: D_n to CP	2.0 2.0	– –	ns
t_w(H) t_w(L)	Cp Pulse Width HIGH or LOW	7.0 6.0	– –	ns

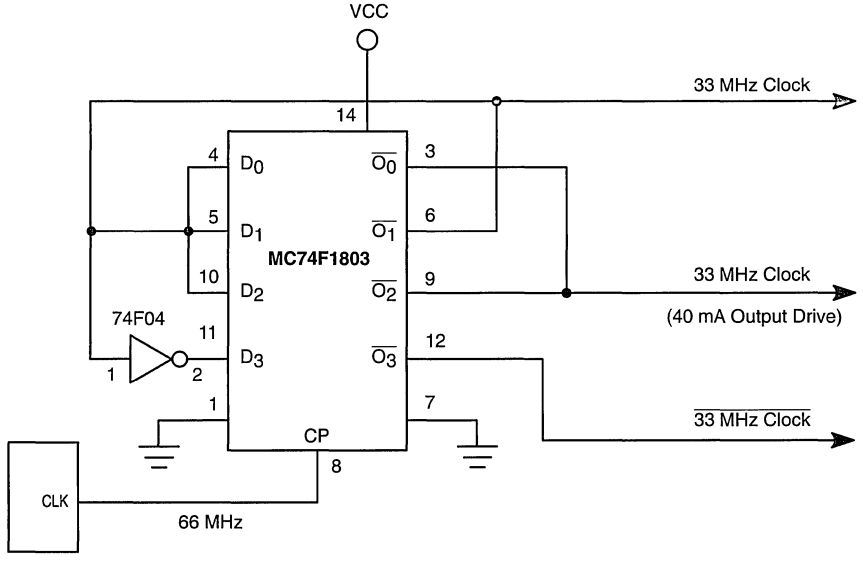
1. The combination of the setup time (t_s) requirement and maximum propagation delay (t_p) are guaranteed to be within this limit for all conditions.

AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C: V_{CC} = +5.0 V ±10%: RL = 500 Ω) [1]

Symbol	Parameter	C_L = 50 pF		Unit
		Min	Max	
f_{max}	Maximum Clock Frequency	70	–	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O_n}$	3.0	7.5	ns
t_{Pv}	Propagation Delay CP to $\overline{O_n}$ Variation	–	3.0	ns
t_{ps} $\overline{O_0}$, $\overline{O_1}$, $\overline{O_2}$, $\overline{O_3}$,	Propagation Delay Skew $\lvert t_{PLH}$ Actual – t_{PHL} Actuall for $\overline{O_0}$, $\overline{O_1}$, $\overline{O_2}$, $\overline{O_3}$	–	2.0	ns
t_{os}	Output to Output Skew [2] $\lvert t_p \overline{O_n} - t_p \overline{O_m} \rvert$	–	2.0	ns
t_{rise}, t_{fall} $\overline{O_1}$,	Rise/Fall Time for $\overline{O_1}$ (0.8 to 2.0 V)	–	3.0	ns
t_{rise}, t_{fall} $\overline{O_0}$, $\overline{O_2}$, $\overline{O_3}$,	Rise/Fall Time for $\overline{O_1}$, $\overline{O_2}$, $\overline{O_3}$, (0.8 to 2.0 V)	–	3.5	ns

1. The test conditions used are all four outputs switching simultaneously. The AC characteristics described above are also guaranteed when two outputs are tied together.
2. Where $t_p \overline{O_n}$ and $t_p \overline{O_m}$ are the actual propagation delays (any combination of high or low) for two separate outputs from a given high transition of CP.
3. For a given set of conditions (i.e., capacitive load, temperature, V_{CC}, and number of outputs switching simultaneously) the variation from device to device is guaranteed to be less than or equal to the maximum.

TYPICAL MC74F1803 APPLICATION



Low Skew CMOS Clock Driver

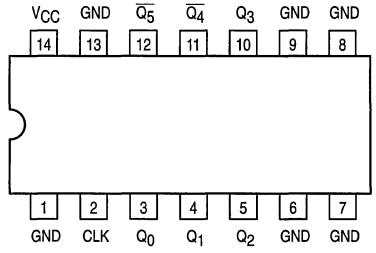
MC88913

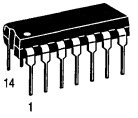
LOW SKEW CMOS CLOCK DRIVER

The MC88913 is a high–speed, low power, hex divide–by–two D–type flip–flop with two inverting and four non–inverting outputs that have closely matched propagation delays. With a TTL compatible buffered clock input that is common to all flip–flops, the MC88913 is ideal for use in high–frequency systems as a clock driver, providing multiple outputs that are synchronous.

- Minimum Clock Input f_{MAX} of 110MHz
- TTL Compatible Positive Edge–Triggered Clock
- Matched Outputs for Synchronous Applications
- Outputs Source/Sink 24mA
- Part–to–Part Skew of Less Than 4.0ns
- Guaranteed Rise and Fall Times for a Given Capacitive Load

Pinout: 14–Lead Plastic (Top View)





N SUFFIX
PLASTIC PACKAGE
CASE 646–06

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03

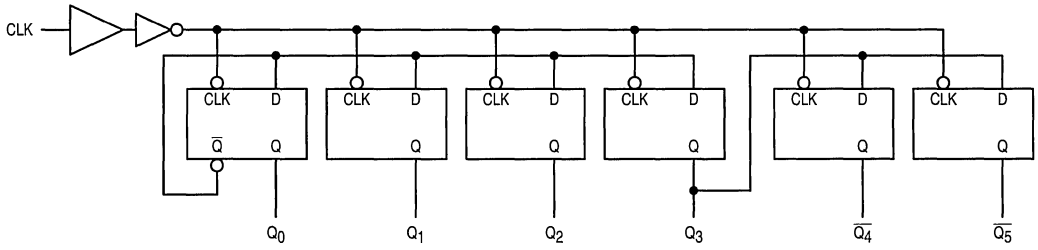
MAXIMUM RATINGS*

Symbol	Parameter	Value	Units
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
P_D	Power Dissipation in Still Air Plastic Package** SOIC Package**	750 500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1mm from Case for 10s (Plastic or SOIC Package)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

** Derating: Plastic Package: –10mW/°C from 65°C to 125°C
SOIC Package: –7.0mW/°C from 65°C to 125°C

LOGIC DIAGRAM



NOTE: This diagram is provided only for understanding of logic operation and should **not** be used to estimate propagation delays

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature	–40	+85	°C
t_r, t_f	Input Rise and Fall Time V_{in} from 0.8 to 2.0V V_{meas} from 0.8 to 2.0V	0 0	10 8.0	ns/V

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter		Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	µA	$V_{IN} = V_{CC}$ or GND V_{CC} = 5.5V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	µA	$V_{IN} = V_{CC}$ or GND V_{CC} = 5.5V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input	1.5	mA	$V_{IN} = V_{CC}$ –2.1V V_{CC} = 5.5V, T_A = Worst Case

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC} (V)	T_A = 25°C, C_L = 50 pF		T_A = –40 to +85°C, C_L = 50 pF		Unit
			Min	Max	Min	Max	
t_W	CLK Pulse Width (HIGH to LOW)	5.0	3.0		3.0		ns

CAPACITANCE

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	30	pF	V_{CC} = 5.0V

DC CHARACTERISTICS

Symbol	Parameter	V_{CC}	T_A = +25°C	T_A = −40 to +85°C		Unit	Conditions
			Typ	Guaranteed Max			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = −50μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −24mA −24mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = 24mA 24mA
I_{IN}	Maximum Input	5.5		±0.1	±0.1	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} −2.1V
I_{OLD}	Minimum Dynamic Output Current**	5.5			75	mA	V_{OLD} = 1.65V
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85V

* All outputs loaded; thresholds on inputs associated with output under test.
** Maximum test duration 20ms, one output at a time.

AC CHARACTERISTICS (V_{CC} = 5.0V ±10%)

Symbol	Parameter	V_{CC} (V)	T_A = 25°C, C_L = 50 pF		T_A = −40 to +85°C, C_L = 50 pF		Unit
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency (50% Duty Cycle)	5.0	110		110		MHz
t_{PLH}, t_{PHL}	Propagation Delay CLK to Q_n, $\overline{Q_n}$	5.0	4.0	10.5	4.0	11.5	ns
t_{PV}	Propagation Delay Variation CLK to Q_0, Q_1, Q_2 (see Note 1)	5.0		4.0		5.0	ns
	Propagation Delay Variation CLK to All Outputs (see Note 1)	5.0		4.5		5.5	ns
t_{PS}	Propagation Delay Skew (Q_0, Q_1, Q_2) $\lvert t_{PHL}$ Actual − t_{PLH} Actual$\rvert$	5.0		1.0		1.0	ns
	Propagation Delay Skew (All Outputs) $\lvert t_{PHL}$ Actual − t_{PLH} Actual$\rvert$	5.0		1.5		1.5	ns
t_{OS}	Output–to–Output Skew (Q_0, Q_1, Q_2) $\lvert t_p\ Q_n - t_p\ Q_m \rvert$ (see Note 2)	5.0		1.0		1.0	ns
	Output–to–Output Skew (All Outputs) $\lvert t_p\ Q_n - t_p\ Q_m \rvert$ (see Note 2)	5.0		1.5		1.5	ns
t_{rise} t_{fall}	Rise/Fall Time for Q_0, Q_1, Q_2 (0.2 x V_{CC} to 0.8 x V_{CC})	5.0		3.0		4.0	ns
	Rise/Fall Time for All Outputs (0.2 x V_{CC} to 0.8 x V_{CC})	5.0		3.5		4.5	ns

1. For a given set of conditions (i.e., capacitive load, temperature and V_{CC}) the variation from device to device is guaranteed to be less than or equal to the maximum.
2. Where $t_p\ Q_n$ and $t_p\ Q_m$ are the actual propagation delays (any combination of HIGH or LOW) for any two separate outputs from a given high transition of CLK.

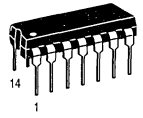
Low Skew CMOS Clock Driver With Reset

MC88914

LOW SKEW CMOS CLOCK DRIVER WITH RESET

The MC88914 is a high–speed, low power, hex divide–by–two D–type flip–flop with matched propagation delays, an internal power–on–reset, and external synchronous reset. With TTL compatible buffered clock and external reset inputs that are common to all flip–flops, the MC88914 is ideal for use in high–frequency systems as a clock driver, providing multiple outputs that are synchronous.

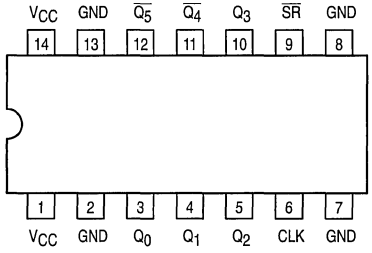
- Power–on–Reset and External Synchronous Reset
- TTL Compatible Positive Edge–Triggered Clock
- Matched Outputs for Synchronous Applications
- Outputs Source/Sink 24mA
- Part–to–Part Skew of Less Than 3.0ns
- Guaranteed Rise and Fall Times for a Given Capacitive Load



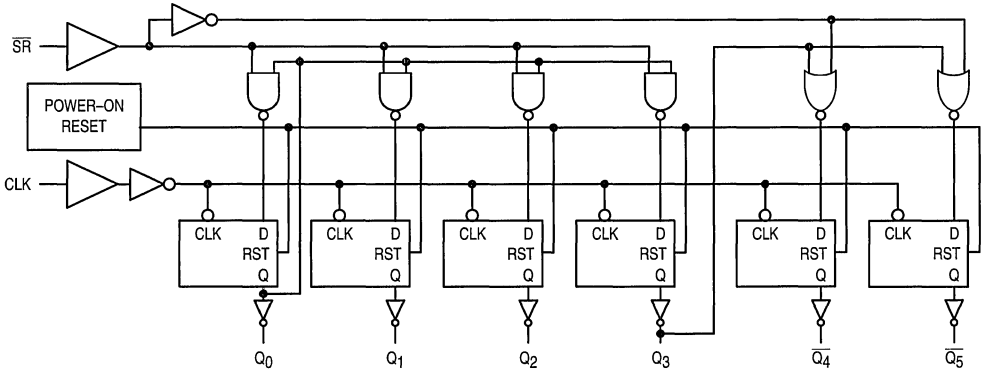
N SUFFIX
PLASTIC PACKAGE
CASE 646–06

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03

Pinout: 14–Lead Plastic (Top View)



LOGIC DIAGRAM



NOTE: This diagram is provided only for understanding of logic operation and should **not** be used to estimate propagation delays

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter		Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input	1.5	mA	$V_{IN} = V_{CC} - 2.1V$ $V_{CC} = 5.5V$, T_A = Worst Case

DC CHARACTERISTICS

Symbol	Parameter	V_{CC}	$T_A = +25°C$	$T_A = -40$ to $+85°C$		Unit	Conditions
			Typ	Guaranteed Max			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	$I_{OUT} = -50\mu A$
		4.5 5.5		3.86 4.86	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24mA$ $-24mA$
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	$I_{OUT} = 50\mu A$
		4.5 5.5		0.36 0.36	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = 24mA$ $24mA$
I_{IN}	Maximum Input	5.5		±0.1	±0.1	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic Output Current**	5.5			75	mA	$V_{OLD} = 1.65V$
I_{OHD}		5.5			−75	mA	$V_{OHD} = 3.85V$

* All outputs loaded; thresholds on inputs associated with output under test.

** Maximum test duration 20ms, one output at a time.

AC CHARACTERISTICS (V_{CC} = 5.0V ±10%)

Symbol	Parameter	V_{CC} (V)	T_A = 25°C, C_L = 50 pF		T_A = –40 to +85°C, C_L = 50 pF		Unit
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency (50% Duty Cycle)	5.0	110		110		MHz
t_{PLH}, t_{PHL}	Propagation Delay CLK to Q_n, $\overline{Q_n}$	5.0	4.0	9.0	4.0	11	ns
t_{PV}	Propagation Delay Variation CLK to Q_n, $\overline{Q_n}$ (see Note 1)	5.0		3.0		3.0	ns
t_{PS}	Propagation Delay Skew (Q_n, $\overline{Q_n}$) $\lvert t_{PHL}$ Actual – t_{PLH} Actual$\rvert$	5.0		1.0		1.0	ns
t_{OS}	Output–to–Output Skew (Q_n, $\overline{Q_n}$) $\lvert t_p\ Q_n - t_p\ Q_m \rvert$ (see Note 2)	5.0		1.0		1.0	ns
t_{rise} t_{fall}	Rise/Fall Time for Q_n, $\overline{Q_n}$ (0.2 x V_{CC} to 0.8 x V_{CC})	5.0		3.0		4.0	ns

1. For a given set of conditions (i.e., capacitive load, temperature and V_{CC}) the variation from device to device is guaranteed to be less than or equal to the maximum.
2. Where $t_p\ Q_n$ and $t_p\ Q_m$ are the actual propagation delays (any combination of HIGH or LOW) for any two separate outputs from a given high transition of CLK.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC} (V)	T_A = 25°C, C_L = 50 pF		T_A = –40 to +85°C, C_L = 50 pF		Unit
			Min	Max	Min	Max	
t_W	CLK Pulse Width (HIGH to LOW)	5.0	3.0		3.0		ns
t_{SU}	Minimum Setup Time, HIGH or LOW SRB to Clock	5.0	3.5		3.5		ns
t_{HD}	Minimum Hold Time, HIGH or LOW SRB to Clock	5.0	1.0		1.0		ns

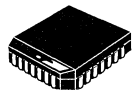
CAPACITANCE

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	30	pF	V_{CC} = 5.0V

68030/040 PECL-TTL Clock Driver

MC10H640
MC100H640

68030/040 PECL–TTL CLOCK DRIVER



FN SUFFIX
PLASTIC PACKAGE
CASE 776–02

The MC10H/100H640 generates the necessary clocks for the 68030, 68040 and similar microprocessors. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part–to–part skew, within–part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (ECL referenced to +5.0V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50MHz and beyond, the inherent superiority of ECL (particularly differential ECL) as a means of clock signal distribution becomes increasingly evident. The H640 also uses differential PECL internally to achieve its superior skew characteristic.

The H640 includes divide–by–two and divide–by–four stages, both to achieve the necessary duty cycle skew and to generate MPU clocks as required. A typical 50MHz processor application would use an input clock running at 100MHz, thus obtaining output clocks at 50MHz and 25MHz (see Logic Symbol).

The 10H version is compatible with MECL 10H™ ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0V).

- Generates Clocks for 68030/040
- Meets 030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and PECL Power/Ground Pins
- Asynchronous Reset
- Single +5.0V Supply

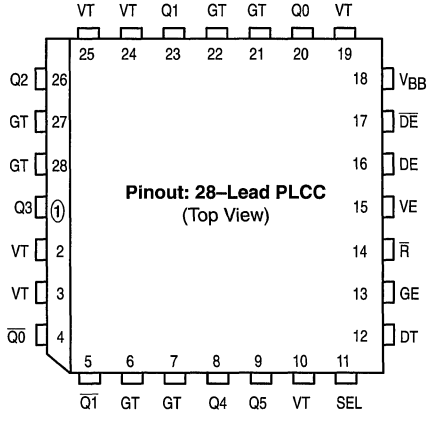
Function

Reset (R): LOW on RESET forces all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

Power–Up: The device is designed to have the POS edges of the ÷2 and ÷4 outputs synchronized at power up.

Select (SEL): LOW selects the ECL input source (DE/$\overline{DE}$). HIGH selects the TTL input source (DT).

The H640 also contains circuitry to force a stable state of the ECL input differential pair, should both sides be left open. In this case, the DE side of the input is pulled LOW, and $\overline{DE}$ goes HIGH.

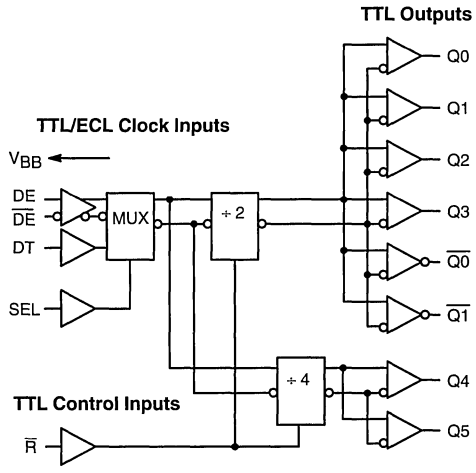


Pinout: 28–Lead PLCC
(Top View)

PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0 V)
VT	TTL V_{CC} (+5.0 V)
VE	ECL V_{CC} (+5.0 V)
GE	ECL Ground (0 V)
DE, $\overline{DE}$	ECL Signal Input (positive ECL)
V_{BB}	V_{BB} Reference Output
DT	TTL Signal Input
Qn, $\overline{Qn}$	Signal Outputs (TTL)
SEL	Input Select (TTL)
$\overline{R}$	Reset (TTL)

LOGIC DIAGRAM



AC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
t_{PLH}	Propagation Delay ECL D to Output	Q0–Q3	4.9	5.9	4.9	5.9	5.2	6.2	ns	CL = 25pF
t_{PLH}	Propagation Delay TTL D to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	CL = 25pF
tskwd*	Within–Device Skew			0.5		0.5		0.5	ns	CL = 25pF
t_{PLH}	Propagation Delay ECL D to Output	$\overline{Q0}$, $\overline{Q1}$	4.9	5.9	4.9	5.9	5.2	6.2	ns	CL = 25pF
t_{PLH}	Propagation Delay TTL D to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	CL = 25pF
t_{PLH}	Propagation Delay ECL D to Output	Q4, Q5	4.9	5.9	4.9	5.9	5.2	6.2	ns	CL = 25pF
t_{PLH}	Propagation Delay TTL D to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	CL = 25pF
t_{PD}	Propagation Delay R to Output	All Outputs	4.3	6.3	4.3	6.3	5.0	7.0	ns	CL = 25pF
t_R t_F	Output Rise/Fall Time 0.8 V – 2.0 V	All Outputs		2.5 2.5		2.5 2.5		2.5 2.5	ns	CL = 25pF
f_{max}	Maximum Input Frequency		135		135		135		MHz	CL = 25pF
t_{pw}	Minimum Pulse Width		1.50		1.50		1.50		ns	
t_{rr}	Reset Recovery Time		1.25		1.25		1.25		ns	

* Within–Device Skew defined as identical transitions on similar paths through a device.

V_{CC} and CLOAD RANGES TO MEET DUTY CYCLE REQUIREMENTS ($0°C \le T_A \le 85°C$ Output Duty Cycle Measured Relative to 1.5V)

Symbol	Characteristic		Min	Nom	Max	Unit	Condition
	Range of V_{CC} and CL to meet minimum pulse width (HIGH or LOW) = 11.5 ns at $f_{out} \le 40$ MHz	V_{CC} CL	4.75 10	5.0	5.25 50	V pF	Q0–Q3 $\overline{Q0}$–$\overline{Q1}$
	Range of V_{CC} and CL to meet minimum pulse width (HIGH or LOW) = 9.5 ns at $40 < f_{out} \le 50$ MHz	V_{CC} CL	4.875 15	5.0	5.125 27	V pF	Q0–Q3

DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
I_{EE}	Power Supply Current	ECL		57		57		57	mA	VE Pin
I_{CCH}		TTL		30		30		30	mA	Total all VT pins
I_{CCL}				30		30		30	mA	

TTL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7V V_{IN} = 7.0V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

10H PECL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

		0°C		25°C		85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current		225		175		175	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5			
V_{IH}*	Input HIGH Voltage	3.83	4.16	3.87	4.19	3.94	4.28	V	VE = 5.0V
V_{IL}*	Input LOW Voltage	3.05	3.52	3.05	3.52	3.05	3.555		
V_{BB}*	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	

*NOTE: PECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for V_{CC} = 5.0V.

100H PECL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

		0°C		25°C		85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current		225		175		175	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5			
V_{IH}*	Input HIGH Voltage	3.835	4.12	3.835	4.12	3.835	4.12	V	VE = 5.0V
V_{IL}*	Input LOW Voltage	3.19	3.525	3.19	3.525	3.19	3.525		
V_{BB}*	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	

*NOTE: PECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for V_{CC} = 5.0V.

10/100H640
DUTY CYCLE CONTROL

To maintain a duty cycle of ±5% at 50MHz, limit the load capacitance and/or power supply variation as shown in Figures 1 and 2. For a ±2.5% duty cycle limit, see Figures 3 and 4. Figures 5 and 6 show duty cycle variation with temperature. Figure 7 shows typical TPD versus load. Figure 8 shows reset recovery time. Figure 9 shows output states after power up.

Best duty cycle control is obtained with a single µP load and minimum line length.

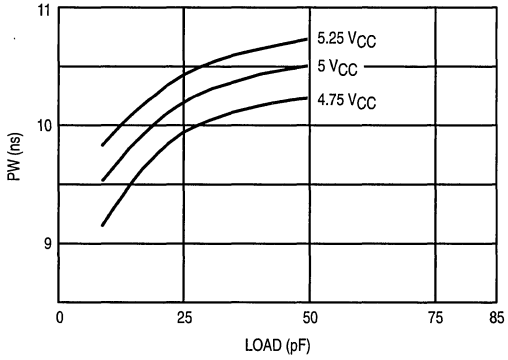


Figure 1. Positive Pulse Width at 25°C Ambient and 50 MHz Out

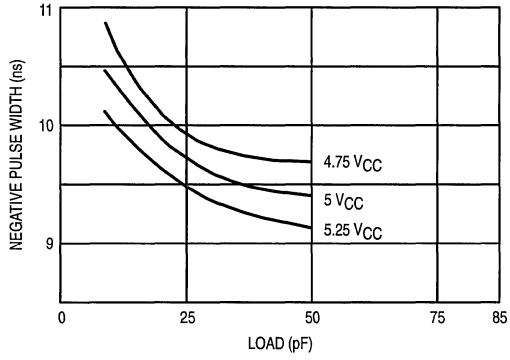


Figure 2. Negative Pulse Width @ 50 MHz Out and 25°C Ambient

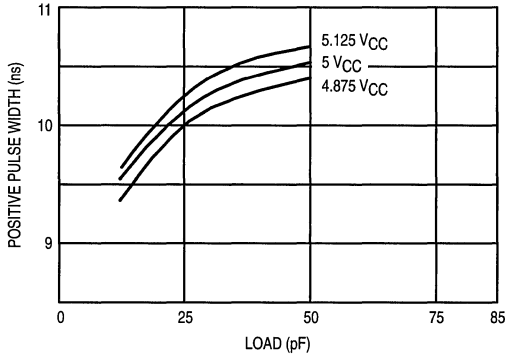


Figure 3. Positive Pulse Width at 25°C Ambient at 50 MHz Out

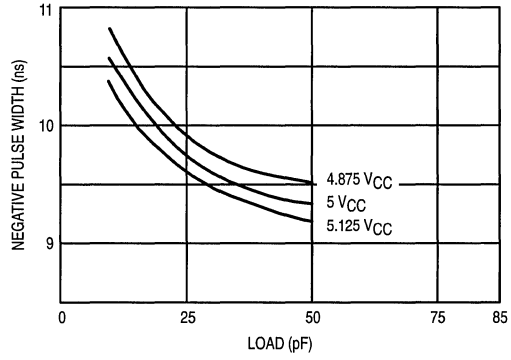


Figure 4. Negative Pulse Width @ 50 MHz Out and 25°C Ambient

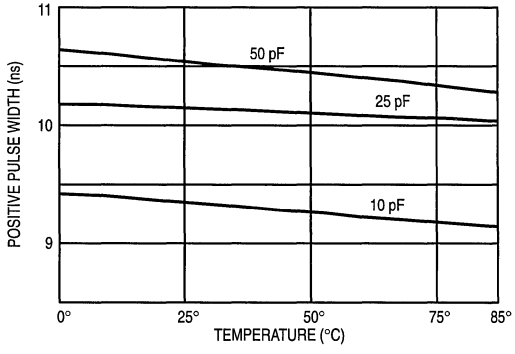


Figure 5. Temperature versus Positive Pulse Width for 100H640 at 50 MHz and +5.0 V V_{CC}

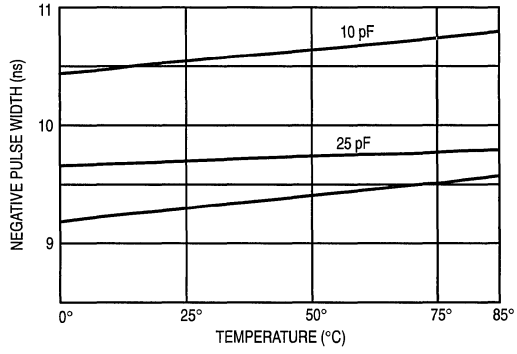


Figure 6. Temperature versus Negative Pulse Width for MC100H640 @ 50 MHz and +5.0 V V_{CC}

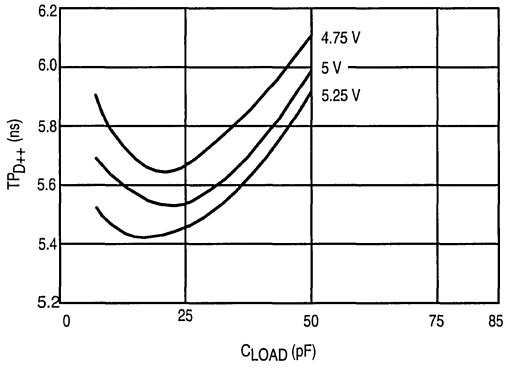


Figure 7. TP versus Load Typical at T_A = 25°C

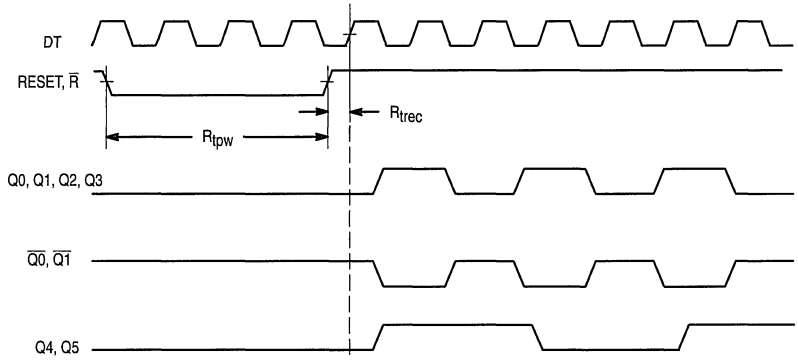
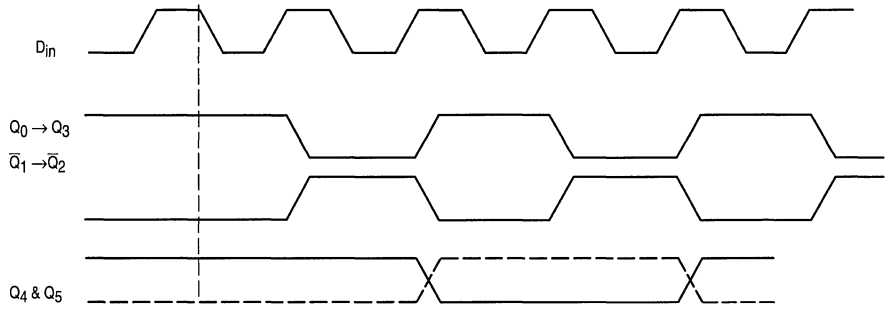


Figure 8. MC10H/100H640 Clock Phase and Reset Recovery Time After Reset Pulse



AFTER POWER UP
OUTPUTS Q_4 & Q_5 WILL SYN WITH POSITIVE EDGES OF D_{in} & $Q_0 \rightarrow Q_3$ & NEGATIVE EDGES OF $\overline{Q}_0$ & $\overline{Q}_1$

Figure 9. Output Timing Diagram

Single Supply PECL-TTL 1:9 Clock Distribution Chip

MC10H641
MC100H641

SINGLE SUPPLY PECL–TTL 1:9 CLOCK DISTRIBUTION CHIP

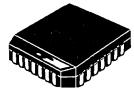
The MC10H/100H641 is a single supply, low skew translating 1:9 clock driver. Devices in the Motorola H600 translator series utilize the 28–lead PLCC for optimal power pinning, signal flow through and electrical performance.

The device features a 24mA TTL output stage, with AC performance specified into a 50pF load capacitance. A latch is provided on–chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pulldown) the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW. Both the LEN and $\overline{EN}$ pins are positive ECL inputs.

The V_{BB} output is provided in case the user wants to drive the device with a single–ended input. For single–ended use the V_{BB} should be connected to the $\overline{D}$ input and bypassed with a 0.01μF capacitor.

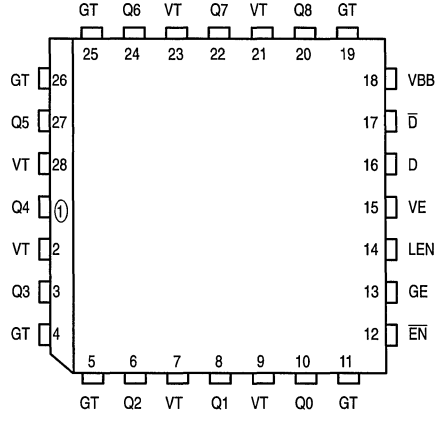
The 10H version of the H641 is compatible with positive MECL 10H™ logic levels. The 100H version is compatible with positive 100K levels.

- PECL–TTL Version of Popular ECLinPS E111
- Low Skew
- Guaranteed Skew Spec
- Latched Input
- Differential ECL Internal Design
- V_{BB} Output for Single–Ended Use
- Single +5V Supply
- Logic Enable
- Extra Power and Ground Supplies
- Separate ECL and TTL Supply Pins



FN SUFFIX
PLASTIC PACKAGE
CASE 776–02

Pinout: 28–Lead PLCC (Top View)



PIN NAMES

Pins	Function
GT, VT	TTL GND, TTL V_{CC}
GE, VE	ECL GND, ECL V_{CC}
D, $\overline{D}$	Signal Input (Positive ECL)
V_{BB}	V_{BB} Reference Output (Positive ECL)
Q0–Q8	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (Positive ECL)
LEN	Latch Enable Input (Positive ECL)

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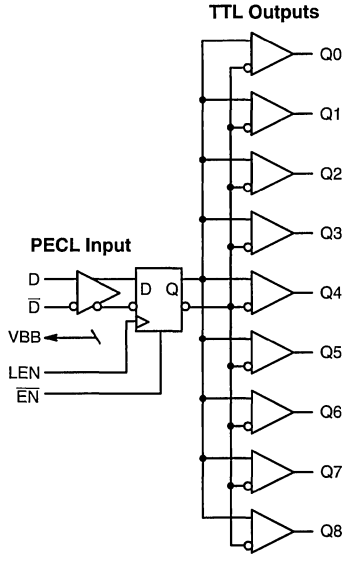
LOGIC DIAGRAM



DC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C			T_A = + 25°C			T_A = + 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	Power Supply Current PECL		24	30		24	30		24	30	mA	
I_{CCH}	TTL		24	30		24	30		24	30	mA	
I_{CCL}			27	35		27	35		27	35	mA	

TTL DC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.5		2.5		2.5		V	I_{OH} = –15mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

10H PECL DC CHARACTERISTICS

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input HIGH Current		225		175		175	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	3.83	4.16	3.87	4.19	3.94	4.28	V	VE = 5.0V[1]
V_{IL}	Input LOW Voltage	3.05	3.52	3.05	3.52	3.05	3.55	V	VE = 5.0V[1]
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	VE = 5.0V[1]

1. PECL V_{IH}, V_{IL}, and V_{BB} are referenced to VE and will vary 1:1 with the power supply. The levels shown are for VE = 5.0V.

100H PECL DC CHARACTERISTICS

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input HIGH Curren		225		175		175	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	3.835	4.120	3.835	4.120	3.835	4.120	V	VE = 5.0V[1]
V_{IL}	Input LOW Voltage	3.190	3.525	3.190	3.525	3.190	3.525	V	VE = 5.0V[1]
V_{BB}	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	VE = 5.0V[1]

1. PECL V_{IH}, V_{IL}, and V_{BB} are referenced to VE and will vary 1:1 with the power supply. The levels shown are for VE = 5.0V.

AC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic	T_J = 0°C			T_J = + 25°C			T_J = + 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay D to Q	5.00 5.36	5.50 5.86	6.00 6.36	4.86 5.27	5.36 5.77	5.86 6.27	5.08 5.43	5.58 5.93	6.08 6.43	ns	CL = 50 pF[1]
t_{skew}	Device Skew Part–to–Part Single V_{CC} Output–to–Output			 1000 750 350			 1000 750 350			 1000 750 350	ps	 CL = 50pF[2] CL = 50 pF[3] CL = 50 pF[4]
t_{PLH} t_{PHL}	Propagation Delay LEN to Q	4.9		6.9	4.9		6.9	5.0		7.0	ns	CL = 50 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{EN}$ to Q	5.0		7.0	4.9		6.9	5.0		7.0	ns	CL = 50 pF
t_r t_f	Output Rise/Fall 0.8V to 2.0V			1.7 1.6			1.7 1.6			1.7 1.6	ns	CL = 50 pF
f_{MAX}	Max Input Frequency	65			65			65			MHz	CL = 50 pF[5]
t_{REC}	Recovery Time $\overline{EN}$	1.25			1.25			1.25			ns	
t_S	Setup Time	0.75	0.50		0.75	0.50		0.75	0.50		ns	
t_H	Hold Time	0.75	0.50		0.75	0.50		0.75	0.50		ns	

1. Propagation delay measurement guaranteed for junction temperatures. Measurements performed at 50MHz input frequency.
2. Skew window guaranteed for a single temperature across a $V_{CC} = V_T = V_E$ of 4.75V to 5.25V (See Application Note in this datasheet).
3. Skew window guaranteed for a single temperature and single $V_{CC} = V_T = V_E$
4. Output–to–output skew is specified for identical transitions through the device.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.

DETERMINING SKEW FOR A SPECIFIC APPLICATION

The H641 has been designed to meet the needs of very low skew clock distribution applications. In order to optimize the device for this application special considerations are necessary in the determining of the part–to–part skew specification limits. Older standard logic devices are specified with relatively slack limits so that the device can be guaranteed over a wide range of potential environmental conditions. This range of conditions represented all of the potential applications in which the device could be used. The result was a specification limit that in the vast majority of cases was extremely conservative and thus did not allow for an optimum system design. For non–critical skew designs this practice is acceptable, however as the clock speeds of systems increase overly conservative specification limits can kill a design.

The following will discuss how users can use the information provided in this data sheet to tailor a part–to–part skew specification limit to their application. The skew determination process may appear somewhat tedious and time consuming, however if the utmost in performance is required this procedure is necessary. For applications which do not require this level of skew performance a generic part–to–part skew limit of 2.5ns can be used. This limit is good for the entire ambient temperature range, the guaranteed V_{CC} (V_T, V_E) range and the guaranteed operating frequency range.

Temperature Dependence

A unique characteristic of the H641 data sheet is that the AC parameters are specified for a junction temperature rather than the usual ambient temperature. Because very few designs will actually utilize the entire commercial temperature range of a device a tighter propagation delay window can be established given the smaller temperature range. Because the junction temperature and not the ambient temperature is what affects the performance of the device the parameter limits are specified for junction temperature. In addition the relationship between the ambient and junction temperature will vary depending on the frequency, load and board environment of the application. Since these factors are all under the control of the user it is impossible to provide specification limits for every possible application. Therefore a baseline specification was established for specific junction temperatures and the information that follows will allow these to be tailored to specific applications.

Since the junction temperature of a device is difficult to measure directly, the first requirement is to be able to "translate" from ambient to junction temperatures. The standard method of doing this is to use the power dissipation of the device and the thermal resistance of the package. For a TTL output device the power dissipation will be a function of the load capacitance and the frequency of the output. The total power dissipation of a device can be described by the following equation:

$$P_D \text{ (watts)} = I_{CC} \text{ (no load)} * V_{CC} + V_S * V_{CC} * f * C_L * \# \text{ Outputs}$$

where:

V_S= Output Voltage Swing = 3V
f = Output Frequency
C_L = Load Capacitance
$I_{CC} = I_{EE} + I_{CCH}$

Figure 1 plots the I_{CC} versus Frequency of the H641 with no load capacitance on the output. Using this graph and the information specific to the application a user can determine the power dissipation of the H641.

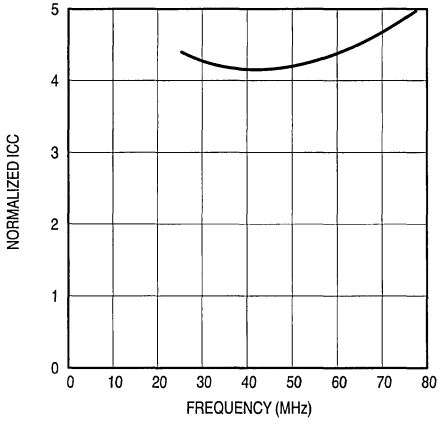


Figure 1. I_{CC} versus f (No Load)

Figure 2 illustrates the thermal resistance (in °C/W) for the 28–lead PLCC under various air flow conditions. By reading the thermal resistance from the graph and multiplying by the power dissipation calculated above the junction temperature increase above ambient of the device can be calculated.

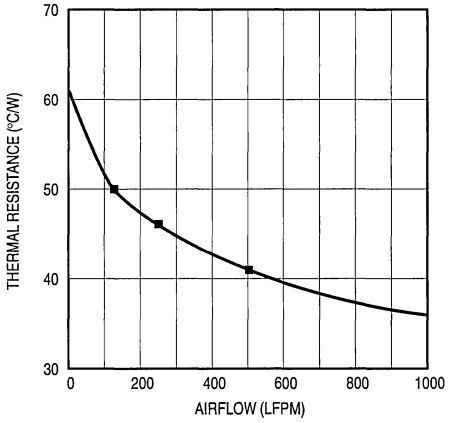


Figure 2. $\varnothing_{JA}$ versus Air Flow

Finally taking this value for junction temperature and applying it to Figure 3 allows the user to determine the propagation delay for the device in question. A more common use would be to establish an ambient temperature range for the H641's in the system and utilize the above methodology to determine the potential increased skew of the distribution network. Note that for this information if the T_{PD} versus Temperature curve were linear the calculations would not be required. If the curve were linear over all temperatures a simple temperature coefficient could be provided.

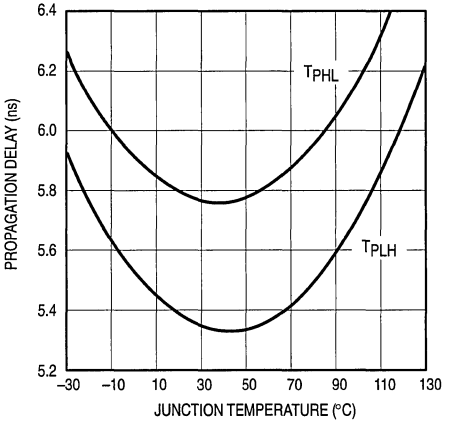


Figure 3. T_{PD} versus Junction Temperature

V_{CC} Dependence

TTL and CMOS devices show a significant propagation delay dependence with V_{CC}. Therefore the V_{CC} variation in a system will have a direct impact on the total skew of the clock distribution network. When calculating the skew between two devices on a single board it is very likely an assumption of identical V_{CC}'s can be made. In this case the number provided in the data sheet for part–to–part skew would be overly conservative. By using Figure 4 the skew given in the data sheet can be reduced to represent a smaller or zero variation in V_{CC}. The delay variation due to the specified V_{CC} variation is ≈270ps. Therefore, the 1ns window on the data sheet can be reduced by 270ps if the devices in question will always experience the same V_{CC}. The distribution of the propagation delay ranges given in the data sheet is actually a composite of three distributions whose means are separated by the fixed difference in propagation delay at the typical, minimum and maximum V_{CC}.

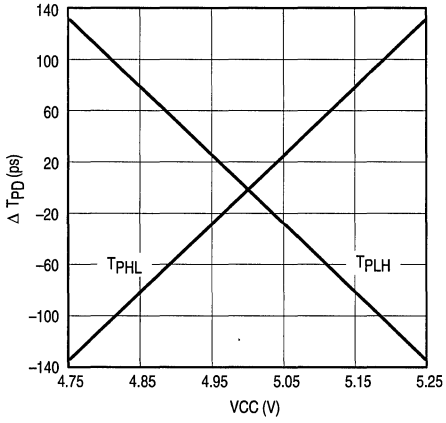


Figure 4. ΔT_{PD} versus V_{CC}

Capacitive Load Dependence

As with V_{CC} the propagation delay of a TTL output is intimately tied to variation in the load capacitance. The skew specifications given in the data sheet, of course, assume equal loading on all of the outputs. However situations could arise where this is an impossibility and it may be necessary to estimate the skew added by asymmetric loading. In addition the propagation delay numbers are provided only for 50pF loads, thus necessitating a method of determining the propagation delay for alternative loads.

Figure 5 shows the relationship between the two propagation delays with respect to the capacitive load on the output. Utilizing this graph and the 50pF limits the specification of the H641 can be mapped into a spec for either a different value load or asymmetric loads.

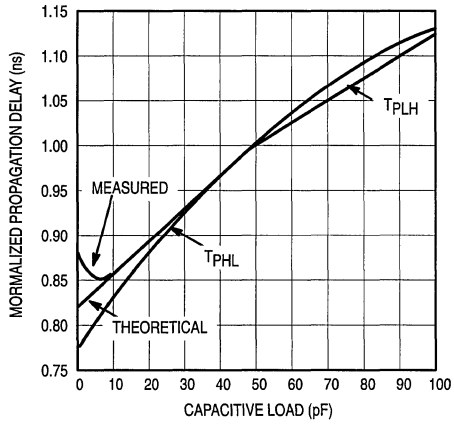


Figure 5. T_{PD} versus Load

Rise/Fall Skew Determination

The rise–to–fall skew is defined as simply the difference between the T_{PLH} and the T_{PHL} propagation delays. This skew for the H641 is dependent on the V_{CC} applied to the device. Notice from Figure 4 the opposite relationship of T_{PD} versus V_{CC} between T_{PLH} and T_{PHL}. Because of this the rise–to–fall skew will vary depending on V_{CC}. Since in all likelihood it will be impossible to establish the exact value for V_{CC}, the expected variation range for V_{CC} should be used. If this variation will be the ±5% shown in the data sheet the rise–to–fall skew could be established by simply subtracting the fastest T_{PLH} from the slowest T_{PHL}; this exercise yields 1.41ns. If a tighter V_{CC} range can be realized Figure 4 can be used to establish the rise–to–fall skew.

Specification Limit Determination Example

The situation pictured in Figure 6 will be analyzed as an example. The central clock is distributed to two different cards; on one card a single H641 is used to distribute the clock while on the second card two H641's are required to supply the needed clocks. The data sheet as well as the graphical information of this section will be used to calculate the skew between H641a and H641b as well as the skew between all three of the devices. Only the T_{PLH} will be analyzed, the T_{PHL} numbers can be found using the same technique. The following assumptions will be used:

- All outputs will be loaded with 50pF
- All outputs will toggle at 30MHz
- The V_{CC} variation between the two boards is ±3%
- The temperature variation between the three devices is ±15°C around an ambient of 45°C.
- 500LFPM air flow

The first task is to calculate the junction temperature for the devices under these conditions. Using the power equation yields:

$$P_D = I_{CC}\text{ (no load)} * V_{CC} + V_{CC} * V_S * f * C_L * \#\text{ outputs}$$
$$= 1.8 * 48mA * 5V + 5V * 3V * 30MHz * 50pF * 9$$
$$= 432mW + 203mW = 635mW$$

Using the thermal resistance graph of Figure 2 yields a thermal resistance of 41°C/W which yields a junction temperature of 71°C with a range of 56°C to 86°C. Using the T_{PD} versus Temperature curve of Figure 3 yields a propagation delay of 5.42ns and a variation of 0.19ns.

Since the design will not experience the full ±5% V_{CC} variation of the data sheet the 1ns window provided will be unnecessarily conservative. Using the curve of Figure 4 shows a delay variation due to a ±3% V_{CC} variation of ±0.075ns. Therefore the 1ns window can be reduced to 1ns – (0.27ns – 0.15ns) = 0.88ns. Since H641a and H641b are on the same board we will assume that they will always be at the same V_{CC}; therefore the propagation delay window will only be 1ns – 0.27ns = 0.73ns.

Putting all of this information together leads to a skew between all devices of

0.19ns + 0.88ns
(temperature + supply, and inherent device),

while the skew between devices A and B will be only

0.19ns + 0.73ns
(temperature + inherent device only).

In both cases, the propagation delays will be centered around 5.42ns, resulting in the following t_{PLH} windows:

T_{PLH} = 4.92ns – 5.99ns; 1.07ns window (all devices)
T_{PLH} = 5.00ns – 5.92ns; 0.92ns window (devices a & b)

Of course the output–to–output skew will be as shown in the data sheet since all outputs are equally loaded.

This process may seem cumbersome, however the delay windows, and thus skew, obtained are significantly better than the conservative worst case limits provided at the beginning of this note. For very high performance designs, this extra information and effort can mean the difference between going ahead with prototypes or spending valuable engineering time searching for alternative approaches.

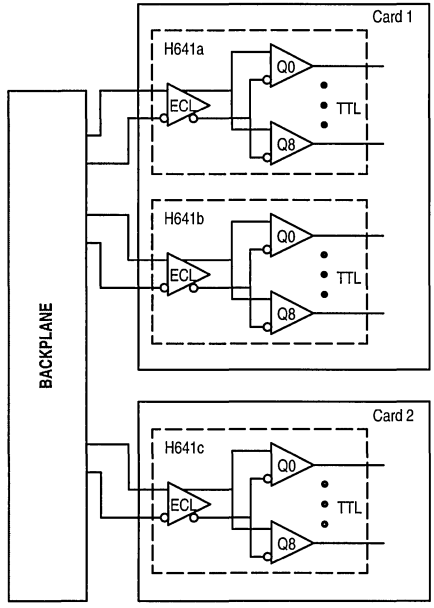


Figure 6. Example Application

68030/040 PECL-TTL Clock Driver

MC10H642
MC100H642

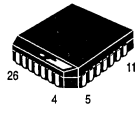
68030/040
PECL–TTL CLOCK
DRIVER

The MC10H/100H642 generates the necessary clocks for the 68030, 68040 and similar microprocessors. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part–to–part skew, within–part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (ECL referenced to +5.0V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50MHz and beyond, the inherent superiority of ECL (particularly differential ECL) as a means of clock signal distribution becomes increasingly evident. The H642 also uses differential PECL internally to achieve its superior skew characteristic.

The H642 includes divide–by–two and divide–by–four stages, both to achieve the necessary duty cycle skew and to generate MPU clocks as required. A typical 50MHz processor application would use an input clock running at 100MHz, thus obtaining output clocks at 50MHz and 25MHz (see Logic Diagram).

The 10H version is compatible with MECL 10H™ ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0V).



FN SUFFIX
PLASTIC PACKAGE
CASE 776–02

- Generates Clocks for 68030/040
- Meets 030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and PECL Power/Ground Pins
- Asynchronous Reset
- Single +5.0V Supply

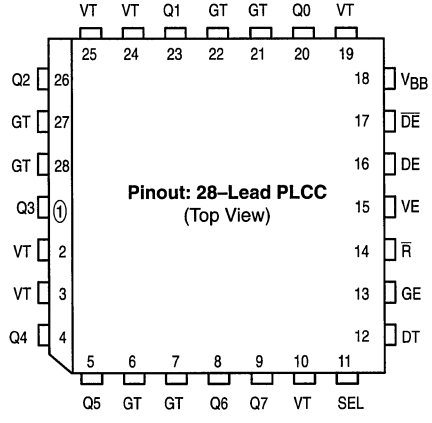
Function

Reset(R): LOW on RESET forces all Q outputs LOW.

Select(SEL): LOW selects the ECL input source (DE/$\overline{DE}$).
HIGH selects the TTL input source (DT).

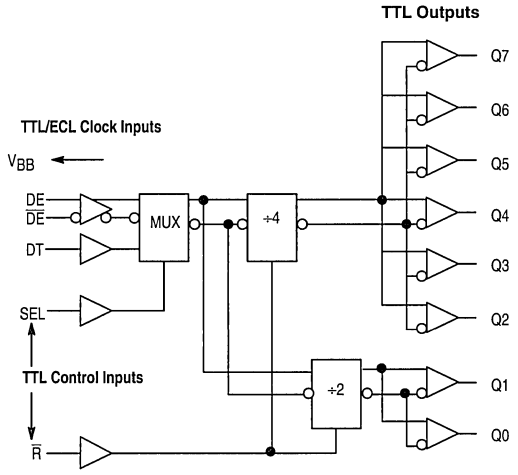
The H642 also contains circuitry to force a stable input state of the ECL differential input pair, should both sides be left open. In this Case, the DE side of the input is pulled LOW, and $\overline{DE}$ goes HIGH.

Power Up: The device is designed to have positive edges of the ÷2 and ÷4 outputs synchronized at Power Up.



MOTOROLA

LOGIC DIAGRAM



PIN NAMES

Pin	Symbol	Description	Pin	Symbol	Description
1	Q3	Signal Output (TTL)**	15	VE	ECL V_{CC} (+5.0V)
2	VT	TTL V_{CC} (+5.0V)	16	DE	ECL Signal Input (Non–Inverting)
3	VT	TTL V_{CC} (+5.0V)	17	$\overline{DE}$	ECL Signal Input (Inverting)
4	Q4	Signal Output (TTL)**	18	V_{BB}	V_{BB} Reference Output
5	Q5	Signal Output (TTL)**	19	VT	TTL V_{CC} (+5.0V)
6	GT	TTL Ground (0V)	20	Q0	Signal Output (TTL)*
7	GT	TTL Ground (0V)	21	GT	TTL Ground (0V)
8	Q6	Signal Output (TTL)**	22	GT	TTL Ground (0V)
9	Q7	Signal Output (TTL)**	23	Q1	Signal Output (TTL)*
10	VT	TTL V_{CC} (+5.0V)	24	VT	TTL V_{CC} (+5.0V)
11	SEL	Input Select (TTL)	25	VT	TTL V_{CC} (+5.0V)
12	DT	TTL Signal Input	26	Q2	Signal Output (TTL)**
13	GE	ECL Ground (0V)	27	GT	TTL Ground (0V)
14	R	Reset (TTL)	28	GT	TTL Ground (0V)

*Divide by 2
**Divide by 4

AC CHARACTERISTICS (V_T = V_E = 5.0V ±5%)

Symbol	Characteristic		T_A = 0°C Min	T_A = 0°C Max	T_A = 25°C Min	T_A = 25°C Max	T_A = 85°C Min	T_A = 85°C Max	Unit	Condition
t_{PLH}	Propagation Delay D to Output	Q2–Q7 C ECL	4.70	5.70	4.75	5.75	4.60	5.60	ns	CL = 25pF
		C TTL	4.70	5.70	4.75	5.75	4.50	5.50		
tskpp	Part–to–Part Skew			1.0		1.0		1.0	ns	
tskwd*	Within–Device Skew			0.5		0.5		0.5	ns	
t_{PLH}	Propagation Delay D to Output	Q0, Q1 C ECL	4.30	5.30	4.50	5.50	4.25	5.25	ns	CL = 25pF
		C TTL	4.30	5.30	4.50	5.50	4.25	5.25		
tskpp	Part–to–Part Skew	All Outputs		2.0		2.0		2.0	ns	CL = 25pF
tskwd	Within–Device Skew			1.0		1.0		1.0	ns	CL = 25pF
t_{PD}	Propagation Delay R to Output	All Outputs	4.3	6.3	4.0	6.0	4.5	6.5	ns	CL = 25pF
t_R	Output Rise/Fall Time	All		2.5		2.5		2.5	ns	CL = 25pF
t_F	0.8 V to 2.0 V	Outputs		2.5		2.5		2.5		
f_{MAX}**	Maximum Input Frequency		100		100		100		MHz	CL = 25pF
RPW	Reset Pulse Width		1.5		1.5		1.5		ns	
RRT	Reset Recovery Time		1.25		1.25		1.25		ns	

* Within–Device Skew defined as identical transactions on similar paths through a device.
** NOTE: MAX Frequency is 135MHz.

10H PECL CHARACTERISTICS (V_T = V_E = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C Min	T_A = 0°C Max	T_A = 25°C Min	T_A = 25°C Max	T_A = 85°C Min	T_A = 85°C Max	Unit	Condition
I_{IH}	Input HIGH Current		225		175		175	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5			
	* NOTE								
V_{IH}	Input HIGH Voltage	3.83	4.16	3.87	4.19	3.94	4.28	V	V_{EE} = 5.0V
V_{IL}	Input LOW Voltage	3.05	3.52	3.05	3.52	3.05	3.555		
	* NOTE								
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	

100H PECL CHARACTERISTICS (V_T = V_E = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C Min	T_A = 0°C Max	T_A = 25°C Min	T_A = 25°C Max	T_A = 85°C Min	T_A = 85°C Max	Unit	Condition
I_{IH}	Input HIGH Current		225		175		175	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5			
	* NOTE								
V_{IH}	Input HIGH Voltage	3.835	4.120	3.835	4.120	3.835	4.120	V	V_{EE} = 5.0V
V_{IL}	Input LOW Voltage	3.190	3.525	3.190	3.525	3.190	3.525		
	* NOTE								
V_{BB}	Output Reference Voltage	3.620	3.740	3.620	3.740	3.620	3.740	V	

*NOTE: PECL LEVELS are referenced to V_{CC} and will vary 1:1 with the power supply. The VALUES shown are for V_{CC} = 5.0V.

10H/100H DC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic		T_A = 0°C Min	T_A = 0°C Max	T_A = 25°C Min	T_A = 25°C Max	T_A = 85°C Min	T_A = 85°C Max	Unit	Condition
I_{EE}	Power Supply Current	PECL		57		57		57	mA	VE Pin
I_{CCH}		TTL		30		30		30	mA	Total All VT Pins
I_{CCL}				30		30		30	mA	

10H/100H TTL DC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic	T_A = 0°C Min	T_A = 0°C Max	T_A = 25°C Min	T_A = 25°C Max	T_A = 85°C Min	T_A = 85°C Max	Unit	Condition
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7V V_{IN} = 7.0V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

10/100H642
DUTY CYCLE CONTROL

To maintain a duty cycle of ±5% at 50 MHz, limit the load capacitance and/or power supply variation as shown in Figures 1 and 2. For a ±2.5% duty cycle limit, see Figures 3 and 4. Figures 5 and 6 show duty cycle variation with temperature. Figure 7 shows typical TPD versus load. Figure 8 shows reset recovery time. Figure 9 shows output states after power up.

Best duty cycle control is obtained with a single µP load and minimum line length.

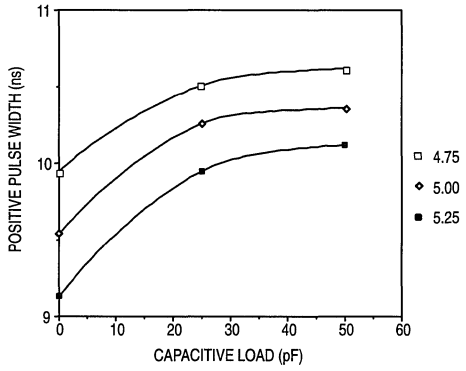


Figure 1. MC10H642 Positive PW versus Load @ ±5% V_{CC}, T_A = 25°C

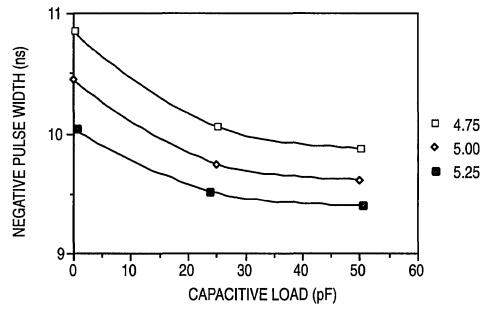


Figure 2. MC10H642 Negative PW versus Load @ ±5% V_{CC}, T_A = 25°C

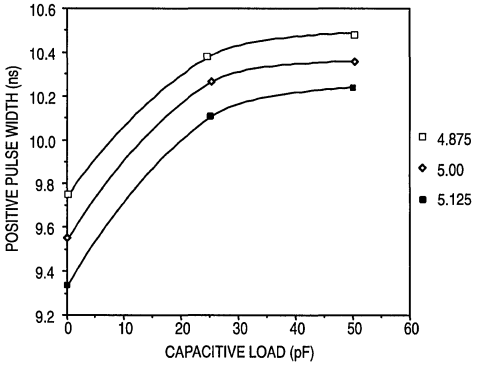


Figure 3. MC10H642 Positive PW versus Load @ ±2.5% V_{CC}, T_A = 25°C

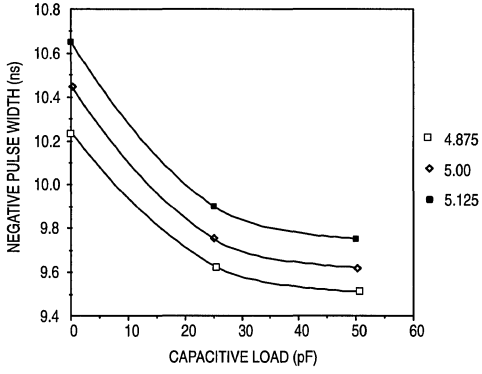


Figure 4. MC10H642 Negative PW versus Load @ ±2.5% V_{CC}, T_A = 25°C

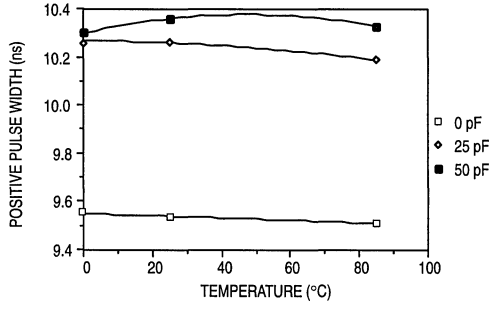


Figure 5. MC10H642 Positive PW versus Temperature, V_{CC} = 5.0V

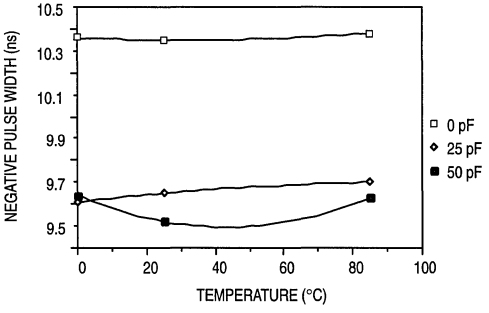


Figure 6. MC10H642 Negative PW versus Temperature, V_{CC} = 5.0V

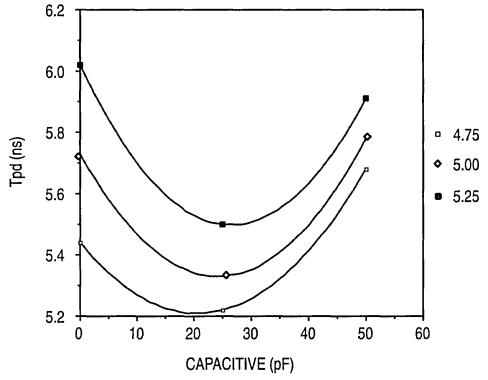


Figure 7. MC10H642 + Tpd versus Load, V_{CC} ±5%, T_A = 25°C (Overshoot at 50 MHz with no load makes graph non linear)

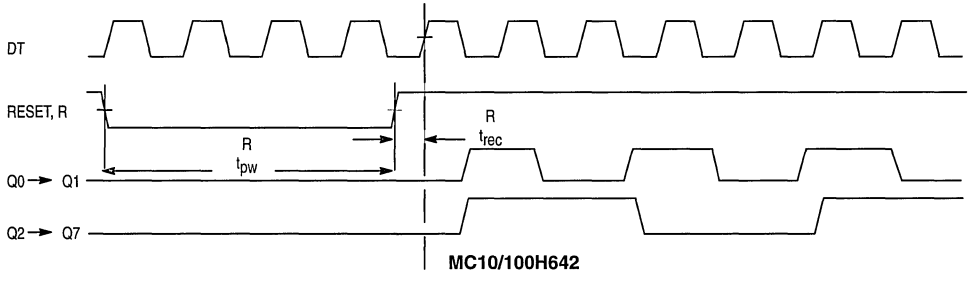


Figure 8. Clock Phase and Reset Recovery Time After Reset Pulse

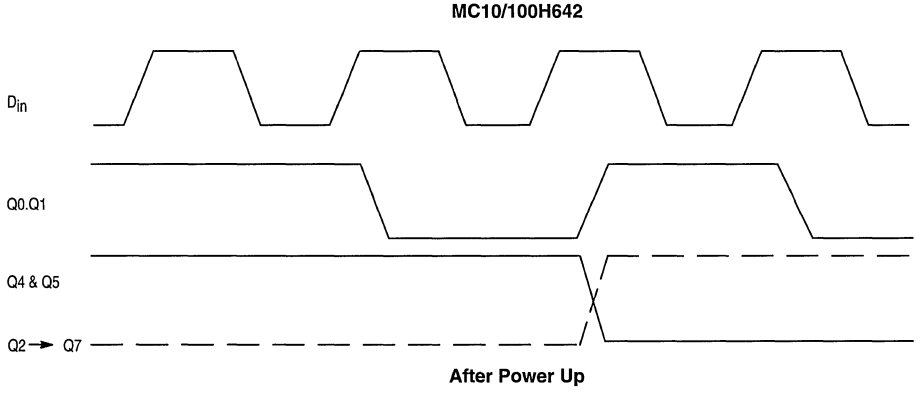
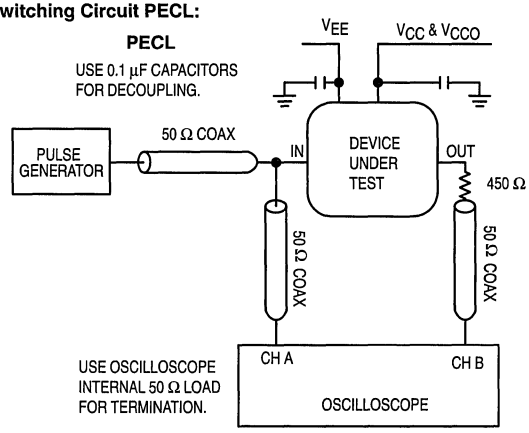


Figure 9. Outputs Q2 → Q7 will Synchronize with Pos Edges of D_{in} & Q0 → Q1

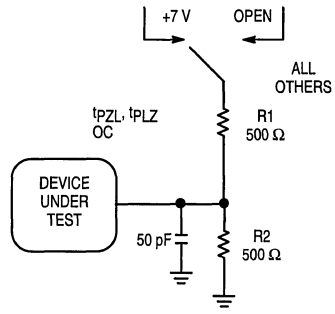
SWITCHING CIRCUIT AND WAVEFORMS

Switching Circuit PECL:

PECL

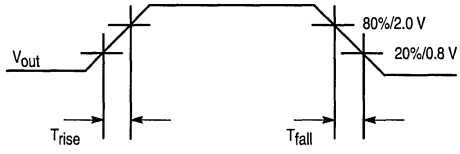


TTL



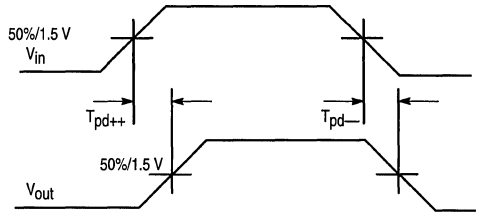
WAVEFORMS: Rise and Fall Times

PECL/TTL



Propagation Delay — Single Ended

PECL/TTL



Dual Supply ECL-TTL 1:8 Clock Driver

MC10H643
MC100H643

DUAL SUPPLY
ECL–TTL 1:8
CLOCK DRIVER

The MC10H/100H643 is a dual supply, low skew translating 1:8 clock driver. Devices in the Motorola H600 translator series utilize the 28–lead PLCC for optimal power pinning, signal flow through and electrical performance. The dual–supply H643 is similar to the H641, which is a single–supply 1:9 version of the same function.

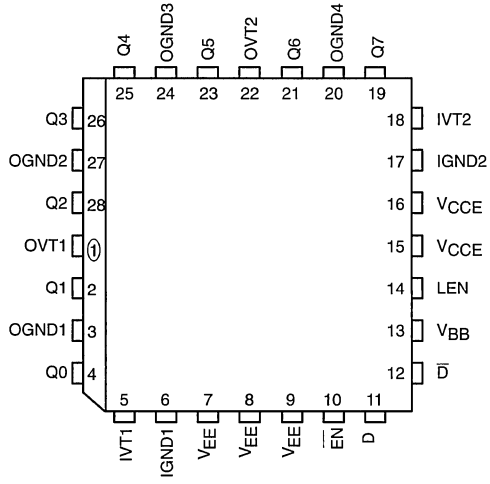
The device features a 48mA TTL output stage, with AC performance specified into a 50pF load capacitance. A Latch is provided on–chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pulldowns) the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW.

The 10H version is compatible with MECL 10H™ ECL logic levels. The 100H version is compatible with 100K levels.

- ECL/TTL Version of Popular ECLinPS™ E111
- Low Skew Within Device 0.5ns
- Guaranteed Skew Spec Part–to–Part 1.0ns
- Latch
- Differential Internal Design
- V_{BB} Output
- Dual Supply
- Reset/Enable
- Multiple TTL and ECL Power/Ground Pins

FN SUFFIX
PLASTIC PACKAGE
CASE 776–02

Pinout: 28–Lead PLCC (Top View)



PIN NAMES

PIN	FUNCTION
OGND	TTL Output Ground (0V)
OVT	TTL Output V_{CC} (+5.0V)
IGND	Internal TTL GND (0V)
IVT	Internal TTL V_{CC} (+5.0V)
V_{EE}	ECL V_{EE} (–5.2/–4.5V)
V_{CCE}	ECL Ground (0V)
D, $\overline{D}$	Signal Input (ECL)
V_{BB}	V_{BB} Reference Output
Q0–Q7	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (ECL)
LEN	Latch Enable Input (ECL)

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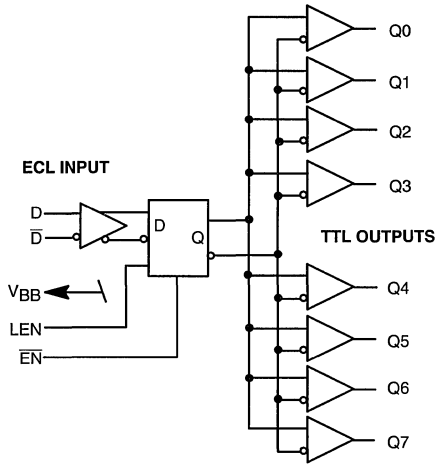
LOGIC DIAGRAM



DC CHARACTERISTICS (IVT = OVT = 5.0V ±5%; V_{EE} = –5.2V ±5% (10H Version); V_{EE} = –4.5V ±0.3V (100H Version))

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{EE}	Power Supply Current	ECL	–	42	–	42	–	42	mA	V_{EE} Pins
I_{CCL}		TTL	–	106	–	106	–	106	mA	Total all OVT
I_{CCH}			–	95	–	95	–	95	mA	and IVT pins

AC CHARACTERISTICS (IVT = OVT = 5.0V ±5%; V_{EE} = –5.2V ±10% (10H); –4.5V ±0.3V (100H); V_{CCE} = GND)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
t_{PLH}	Propagation Delay to Output								
	D	4.0	5.0	4.1	5.1	4.4	5.4		
	LEN	3.5	5.5	3.5	5.5	3.9	5.9	ns	CL = 50pF
	$\overline{EN}$	3.5	5.5	3.5	5.5	3.9	5.9		
t_{SKEW}	Within–Device Skew	–	0.5	–	0.5		0.5	ns	Note 1
t_W	Pulse Width Out HIGH or LOW @ f_{out} = 50MHz	9.0	11.0	9.0	11.0	9.0	11.0	ns	CL = 50pF Note 2
t_S	Setup Time D	0.75	–	0.75	–	0.75	–	ns	
t_H	Hold Time D	0.75	–	0.75	–	0.75	–	ns	
t_{RR}	Recovery Time								
	LEN	1.25	–	1.25	–	1.25	–	ns	
	$\overline{EN}$	1.25	–	1.25	–	1.25	–		
t_{PW}	Minimum Pulse Width								
	LEN	1.5	–	1.5	–	1.5	–	ns	
	$\overline{EN}$	1.5	–	1.5	–	1.5	–		
t_r t_f	Rise / Fall Times 0.8 V – 2.0 V	–	1.2	–	1.2	–	1.2	ns	CL = 50pF

1. Within–Device skew defined as identical transitions on similar paths through a device.
2. Pulse width is defined relative to 1.5V measurement points on the ouput waveform.

TRUTH TABLE

D	LEN	$\overline{EN}$	Q
L	L	L	L
H	L	L	H
X	H	L	Q_O
X	X	H	L

DC CHARACTERISTICS (IVT = OVT = 5.0V ±5%; V_{EE} = –5.2V ±5% (10H Version); V_{EE} = –4.5V ±0.3V (100H Version))

		0°C		25°C		85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	2.5 2.0	– –	2.5 2.0	– –	2.5 2.0	– –	V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage	–	0.5	–	0.5	–	0.5	V	I_{OH} = 48mA
IOS	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

10H DC CHARACTERISTICS (IVT = OVT = 5.0V ±5%; V_{EE} = –5.2V ±5% (10H Version); V_{EE} = –4.5V ±0.3V (100H Version))

		0°C		25°C		85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	– 0.5	225 –	– 0.5	175 –	– 0.5	175 –	µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1170 –1950	–840 –1480	–1130 –1950	–810 –1480	–1070 –1950	–735 –1450	mV	
V_{BB}	Output Reference Voltage	–1380	–1270	–1350	–1250	–1310	–1190	mV	

100H DC CHARACTERISTICS (IVT = OVT = 5.0V ±5%; V_{EE} = –5.2V ±5% (10H); V_{EE} = –4.5V ±0.3V (100H))

		0°C		25°C		85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	– 0.5	225 –	– 0.5	175 –	– 0.5	175 –	µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	mV	
V_{BB}	Output Reference Voltage	–1380	–1260	–1380	–1260	–1380	–1260	mV	

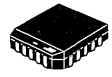
68030/040 PECL-TTL Clock Driver

MC10H644
MC100H644

68030/040 PECL–TTL CLOCK DRIVER

The MC10H/100H644 generates the necessary clocks for the 68030, 68040 and similar microprocessors. The device is functionally equivalent to the H640, but with fewer outputs in a smaller outline 20–lead PLCC package. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part–to–part skew, within–part skew and also duty cycle skew.

- Generates Clocks for 68030/040
- Meets 68030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and ECL Power/Ground Pins
- Within Device Skew on Similar Paths is 0.5 ns
- Asynchronous Reset
- Single +5.0V Supply



FN SUFFIX
PLASTIC PACKAGE
CASE 775–02

The user has a choice of using either TTL or PECL (ECL referenced to +5.0V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50MHz and beyond, the inherent superiority of ECL (particularly differential ECL) as a means of clock signal distribution becomes increasingly evident. The H644 also uses differential ECL internally to achieve its superior skew characteristic.

The H644 includes divide–by–two and divide–by–four stages, both to achieve the necessary duty cycle and skew to generate MPU clocks as required. A typical 50MHz processor application would use an input clock running at 100MHz, thus obtaining output clocks at 50MHz and 25MHz (see Logic Symbol).

The 10H version is compatible with MECL 10H™ ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0V).

Function

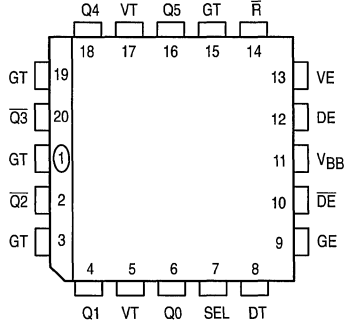
Reset (R): LOW on RESET forces all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

Synchronized Outputs: The device is designed to have the POS edges of the ÷2 and ÷4 outputs synchronized.

Select (SEL): LOW selects the ECL input source (DE/$\overline{DE}$). HIGH selects the TTL input source (DT).

The H644 also contains circuitry to force a stable state of the ECL input differential pair, should both sides be left open. In this case, the DE side of the input is pulled LOW, and $\overline{DE}$ goes HIGH.

Pinout: 20–Lead PLCC (Top View)

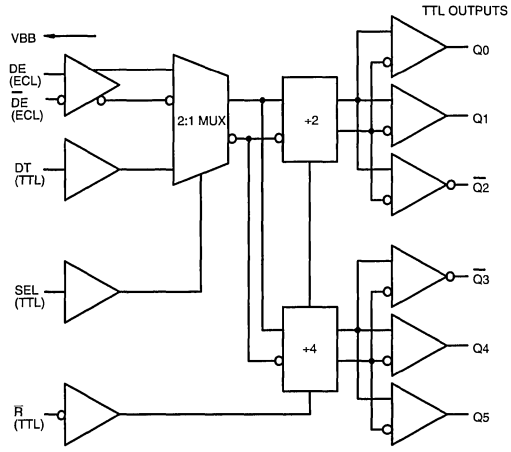


MECL 10H is a trademark of Motorola, Inc.

PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0V)
VT	TTL V_{CC} (+5.0V)
VE	ECL V_{CC} (+5.0V)
GE	ECL Ground (0V)
DE, $\overline{DE}$	ECL Signal Input (positive ECL)
V_{BB}	V_{BB} Reference Output
DT	TTL Signal Input
Qn, $\overline{Qn}$	Signal Outputs (TTL)
SEL	Input Select (TTL)
$\overline{R}$	Reset (TTL)

LOGIC DIAGRAM



AC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
t_{PLH}	Propagation Delay ECL D to Output	All Outputs	5.8	6.8	5.7	6.7	6.1	7.1	ns	CL = 50pF
t_{PLH}	Propagation Delay TTL D to Output		5.7	6.7	5.7	6.7	6.0	7.0	ns	CL = 50pF
t_{skwd}*	Within–Device Skew	Q0, 1, 4, 5	–	0.5	–	0.5	–	0.5	ns	CL = 50pF
t_{skwd}*	Within–Device Skew	$\overline{Q2}$, $\overline{Q3}$	–	0.5	–	0.5	–	0.5	ns	CL = 50pF
t_{skwd}*	Within–Device Skew	All Outputs	–	1.5	–	1.5	–	1.5	ns	CL = 50pF
t_{skp-p}*	Part–to–Part Skew	Q0, 1, 4, 5	–	1.0	–	1.0	–	1.0	ns	CL = 50pF
t_{PD}	Propagation Delay R to Output	All Outputs	4.3	7.3	4.3	7.3	4.5	7.5	ns	CL = 50pF
t_R t_F	Output Rise/Fall Time 0.8V – 2.0V	All Outputs	–	1.6	–	1.6	–	1.6	ns	CL = 50pF
f_{max}	Maximum Input Frequency		135	–	135	–	135	–	MHz	CL = 50pF
TW	Minimum Pulse Width Reset		1.5	–	1.5	–	1.5	–	ns	
t_{rr}	Reset Recovery Time		1.25	–	1.25	–	1.25	–	ns	
T_{PW}	Pulse Width Out High or Low @ f_{in} = 100 MHz and CL = 50 pf	Q0, 1	9.5	10.5	9.5	10.5	9.5	10.5	ns	CL = 50pf Relative 1.5V
TS	Setup Time SEL to DE, DT		2.0	–	2.0	–	2.0	–	ns	
TH	Hold Time SEL to DE, DT		2.0	–	2.0	–	2.0	–	ns	

* Skews are specified for Identical Edges

DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{EE}	Power Supply Current	ECL		65		65		65	mA	VE Pin
I_{CC}		TTL		85		85		85	mA	Total all V_T pins

TTL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0 mA I_{OH} = –24 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V

10H PECL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	µA	
V_{IH}* V_{IL}*	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.55	V	VE = 5.0 V
V_{BB}*	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	VE = 5.0 V

100H PECL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	µA	
V_{IH}* V_{IL}*	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	VE = 5.0 V
V_{BB}*	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	VE = 5.0 V

* NOTE: PECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for V_{CC} = 5.0 V. Only corresponds to ECL Clock Inputs.

1:9 TTL Clock Driver

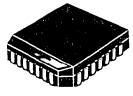
MC10H645

1:9 TTL CLOCK DRIVER

The MC10H645 is a single supply, low skew, TTL I/O 1:9 Clock Driver. Devices in the Motorola H600 clock driver family utiize the 28–lead PLCC for optimal power and signal pin placement.

The device features a 24mA TTL ouput stage with AC performance specified into a 50pF load capacitance. A 2:1 input mux is provided on chip to allow for distributing both system and diagnostic clock signals or designing clock redundancy into a system. With the SEL input held LOW the DO input will be selected, while the D1 input is selected when the SEL input is forced HIGH.

- Low Skew Typically 0.65ns Within Device
- Guaranteed Skew Spec 1.25ns Part–to–Part
- Input Clock Muxing
- Differential ECL Internal Design
- Single Supply
- Extra TTL and ECL Power/Ground Pins

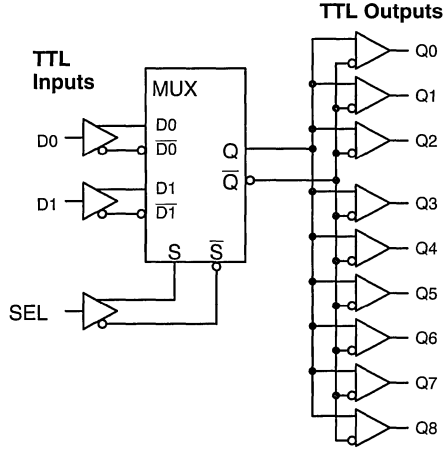


FN SUFFIX
PLASTIC PACKAGE
CASE 776–02

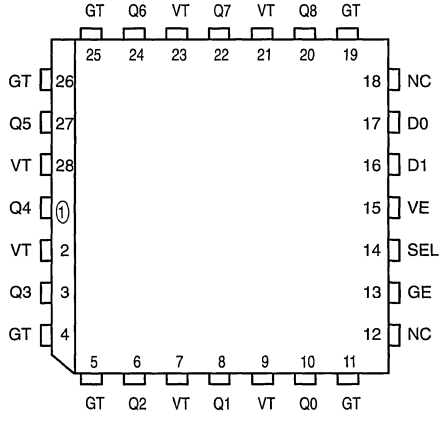
PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0V)
VT	TTL V_{CC} (+5.0V)
VE	ECL V_{CC} (+5.0V)
GE	ECL Ground (0V)
Dn	TTL Signal Input
Q0 – Q8	TTL Signal Outputs
SEL	TTL Mux Select

LOGIC DIAGRAM



Pinout: 28–Lead PLCC (Top View)



PIN DESCRIPTIONS

Pin	Symbol	Description	Pin	Symbol	Description
1	Q4	Signal Output (TTL)	15	VE	ECL V_{CC} (+5.0V)
2	VT	TTL V_{CC} (+5.0V)	16	D1	Signal Input (TTL)
3	Q3	Signal Output (TTL)	17	D0	Signal Input (TTL)
4	GT	TTL Ground (0V)	18	NC	No Connection
5	GT	TTL Ground (0V)	19	GT	TTL Ground (0V)
6	Q2	Signal Output (TTL)	20	Q8	Signal Output (TTL)
7	VT	TTL V_{CC} (+5.0V)	21	VT	TTL V_{CC} (+5.0V)
8	Q1	Signal Output (TTL)	22	Q7	Signal Output (TTL)
9	VT	TTL V_{CC} (+5.0V)	23	VT	TTL V_{CC} (+5.0V)
10	Q0	Signal Output (TTL)	24	Q6	Signal Output (TTL)
11	GT	TTL Ground (0V)	25	GT	TTL Ground (0V)
12	NC	No Connection	26	GT	TTL Ground (0V)
13	GE	ECL Ground	27	Q5	Signal Output (TTL)
14	SEL	Select Input (TTL)	28	VT	TTL V_{CC} (+5.0V)

ABSOLUTE RATINGS (Do not exceed)

Symbol	Characteristic	Value	Unit
VE (ECL)	Power Supply Voltage	–0.5 to +7.0	V
VT (TTL)	Power Supply Voltage	–0.5 to +7.0	V
VI (TTL)	Input Voltage	–0.5 to +7.0	V
V_{out}	Disabled 3–State Output	0.0 to V_T	V
T_{stg}	Storage Temperature	–65 to 150	°C
T_{amb}	Operating Temperature	0.0 to +85	°C

TRUTH TABLE

D0	D1	SEL	Q
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

DC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
I_{EE}	Power Supply Current	ECL		30		30		30	mA	VE Pin
I_{CCH}		TTL		30		30		30	mA	Total all VT pins
I_{CCL}				35		35		35	mA	
V_{OH}	Output HIGH Voltage		2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage			0.5		0.5		0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current		–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

TTL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0 mA I_{OH} = –24 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V

AC CHARACTERISTICS (VT = VE = 5.0V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_0 to Output Only	Q0–Q8	4.8	5.8	4.8	5.8	5.2	6.2	ns	CL = 50pF
t_{PLH}	Propagation Delay D_1 to Output		4.8	5.8	4.8	5.8	5.2	6.2	ns	
t_{PHL}	Propagation Delay D_0 to Output D_1 to Output		 4.8 4.8	 5.8 5.8	 4.8 4.8	 5.8 5.8	 5.2 5.2	 6.2 6.2	ns	
t_{skpp}	Part–to–Part Skew D_0 to Output Only			1.0		1.0		1.0	ns	
t_{skwd}*	Within–Device Skew D_0 to Output Only			0.65		0.65		0.65	ns	
t_{PLH}	Propagation Delay SEL to Q	Q0–Q8	4.5	6.5	5.0	7.0	5.2	7.2	ns	CL = 50pF
t_r t_f	Output Rise/Fall Time 0.8V to 2.0V	Q0–Q8	0.5 0.5	2.5 2.5	0.5 0.5	2.5 2.5	0.5 0.5	2.5 2.5	ns	CL = 50pF
t_S	Setup Time SEL to D		 1.0		 1.0		 1.0		ns	

* Within–Device Skew defined as identical transitions on similar paths through a device.

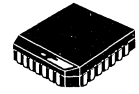
DUTY CYCLE SPECIFICATIONS (0°C ≤ TA ≤ 85°C; Duty Cycle Measured Relative to 1.5V)

Symbol	Characteristic		Min	Nom	Max	Unit	Condition
PW	Range of V_{CC} and CL to Meet Min Pulse Width (HIGH or LOW) at f_{out} ≤50MHz	V_{CC} CL PW	4.875 10.0 9.0	5.0	5.125 50.0 11.0	V pF ns	All Outputs

PECL/TTL-TTL 1:8 Clock Distribution Chip

MC10H646
MC100H646

PENTIUM MICROPROCESSOR PECL/TTL–TTL CLOCK DRIVER



FN SUFFIX
PLASTIC PACKAGE
CASE 776–02

The MC10H/100H646 is a single supply, low skew translating 1:8 clock driver. Devices in the Motorola H600 translator series utilize the 28–lead PLCC for optimal power pinning, signal flow through and electrical performance. The single supply H646 is similar to the H643, which is a dual supply 1:8 version of the same function.

- PECL/TTL–TTL Version of Popular ECLinPS™ E111
- Low Skew
- Guaranteed Skew Spec
- Tri–State Enable
- Differential Internal Design
- V_{BB} Output
- Single Supply
- Extra TTL and ECL Power/Ground Pins
- Matched High and Low Output Impedance
- Meets Specifications Required to Drive the Pentium™ Microprocessor

The H646 was designed specifically to drive series terminated transmission lines. Special techniques were used to match the HIGH and LOW output impedances to about 7ohms. This simplifies the choice of the termination resistor for series terminated applications. To match the HIGH and LOW output impedances, it was necessary to remove the standard I_{OS} limiting resistor. As a result, the user should take care in preventing an output short to ground as the part will be permanently damaged.

The H646 device meets all of the requirements for driving the 60 and 66MHz Pentium Microprocessor. The device has no PLL components, which greatly simplifies its implementation into a digital design. The eight copies of the clock allows for point–to–point clock distribution to simplify board layout and optimize signal integrity.

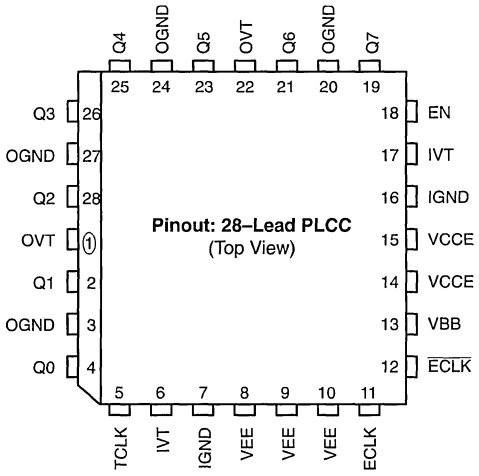
The H646 provides differential PECL inputs for picking up LOW skew PECL clocks from the backplane and distributing it to TTL loads on a daughter board. When used in conjunction with the MC10/100E111, very low skew, very wide clock trees can be designed. In addition, a TTL level clock input is provided for flexibility. Note that only one of the inputs can be used on a single chip. For correct operation, the unused input pins should be left open.

The Output Enable pin forces the outputs into a high impedance state when a logic 0 is applied.

The output buffers of the H646 can drive two series terminated, 50Ω transmission lines each. This capability allows the H646 to drive up to 16 different point–to–point clock loads. Refer to the Applications section for a more detailed discussion in this area.

The 10H version is compatible with MECL 10H™ ECL logic levels. The 100H version is compatible with 100K levels.

MECL 10H and ECLinPS are trademarks of Motorola, Inc. Pentium is a trademark of Intel Corporation.



PIN NAMES

PIN	FUNCTION
OGND	TTL Output Ground (0V)
OVT	TTL Output V_{CC} (+5.0V)
IGND	Internal TTL GND (0V)
IVT	Internal TTL V_{CC} (+5.0V)
V_{EE}	ECL V_{EE} (0V)
V_{CCE}	ECL Ground (5.0V)
ECLK, $\overline{ECLK}$	Differential Signal Input (PECL)
V_{BB}	V_{BB} Reference Output
Q0–Q7	Signal Outputs (TTL)
EN	Tri–State Enable Input (TTL)

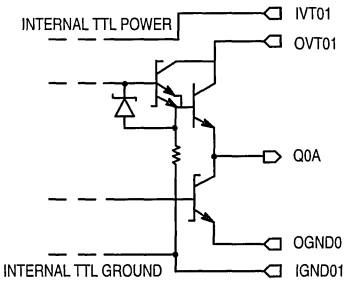
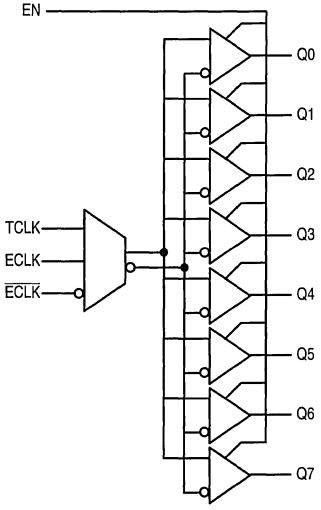


Figure 1. Output Structure

LOGIC DIAGRAM



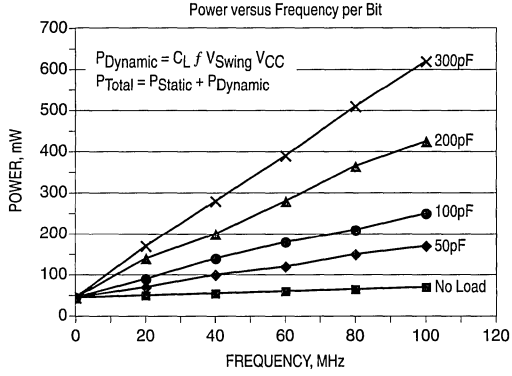


Figure 2. Power versus Frequency (Typical)

TRUTH TABLE

TCLK	ECLK	$\overline{ECLK}$	EN	Q
GND	L	H	H	L
GND	H	L	H	H
H	GND	GND	H	H
L	GND	GND	H	L
X	X	X	L	Z

L = Low Voltage Level; H = High Voltage Level; Z = Tristate

DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.6	– –	2.6	– –	2.6	– –	V	I_{OH} = 24mA
V_{OL}	Output LOW Voltage	–	0.5	–	0.5	–	0.5	V	I_{OL} = 48mA
IOS	Output Short Circuit Current	–	–	–	–	–	–	mA	See Note 1

1. The outputs must not be shorted to ground, as this will result in permanent damage to the device. The high drive outputs of this device do not include a limiting IOS resistor.

TTL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0 mA I_{OH} = –24 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V

10H PECL DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			225			175			175	µA	
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA	
V_{IH}	Input HIGH Voltage	3.83		4.16	3.87		4.19	3.94		4.28	V	IVT = IVO = VCCE = 5.0V (1)
V_{IL}	Input LOW Voltage	3.05		3.52	3.05		3.52	3.05		3.555	V	IVT = IVO = VCCE = 5.0V (1)
V_{BB}	Output Reference Voltage	3.62		3.73	3.65		3.75	3.69		3.81	V	IVT = IVO = VCCE = 5.0V (1)

100H PECL DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			225			175			175	µA	
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA	
V_{IH}	Input HIGH Voltage	3.835		4.12	3.835		4.12	3.835		3.835	V	IVT = IVO = VCCE = 5.0V (1)
V_{IL}	Input LOW Voltage	3.19		3.525	3.19		3.525	3.19		3.525	V	IVT = IVO = VCCE = 5.0V (1)
V_{BB}	Output Reference Voltage	3.62		3.74	3.62		3.74	3.62		3.74	V	IVT = IVO = VCCE = 5.0V (1)

1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to VCCE and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = VCCE = 5.0V

DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic	0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
I_{CCL}	Power Supply Current		185		166	185		185	mA	Total all OVT, IVT, and VCCE pins
I_{CCH}			175		154	175		175	mA	
I_{CCZ}			210			210		210		

AC CHARACTERISTICS (IVT = OVT = VCCE = 5.0V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	ECLK to Q TCLK to Q	4.8 5.1	5.8 6.4	5.0 5.3	6.0 6.4	5.6 5.7	6.6 7.0	ns	
t_{PHL}	Propagation Delay	ECLK to Q TCLK to Q	4.4 4.7	5.4 6.0	4.4 4.8	5.4 5.9	4.8 5.2	5.8 6.5	ns	
$t_{SK(O)}$	Output Skew	Q0, Q3, Q4, Q7 Q1, Q2, Q5 Q0–Q7		350 350 500		350 350 500		350 350 500	ps	Note 1, 6
$t_{SK(PR)}$	Process Skew	ECLK to Q TCLK to Q		1.0 1.3		1.0 1.1		1.0 1.3	ns	Note 2, 6
$t_{SK(P)}$	Pulse Skew	$\Delta t_{PLH} - t_{PHL}$		1.0		1.0		1.0	ns	
t_r, t_f	Rise/Fall Time		0.3	1.5	0.3	1.5	0.3	1.5	ns	
t_{PW}	Output Pulse Width	66MHz @ 2.0V 66MHz @ 0.8V 60MHz @ 2.0V 60MHz @ 0.8V	5.5 5.5 6.0 6.0		5.5 5.5 6.0 6.0		5.5 5.5 6.0 6.0		ns	Note 3, 6
$t_{Stability}$	Clock Stability			±75		±75		±75	ps	Note 4, 6
F_{MAX}	Maximum Input Frequency			80		80		80	MHz	Note 5, 6

1. Output skew defined for identical output transitions.
2. Process skew is valid for V_{CC} = 5.0V ±5%.
3. Parameters guaranteed by $t_{SK(P)}$ and t_r, t_f specification limits.
4. Clock stability is the period variation between two successive rising edges.
5. For series terminated lines. See Applications section for F_{MAX} enhancement techniques.
6. All AC specifications tested driving 50Ω series terminated transmission lines at 80MHz.

1:2 Differential Fanout Buffer

MC10EL11
MC100EL11

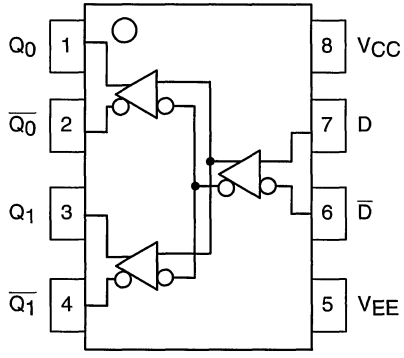
The MC10EL/100EL11 is a differential 1:2 fanout buffer. The device is functionally similar to the E111 device but with higher performance capabilities. Having within-device skews and output transition times significantly improved over the E111, the EL11 is ideally suited for those applications which require the ultimate in AC performance.

The differential inputs of the EL11 employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open (pulled to V_{EE}) the Q outputs will go LOW.

- 265ps Propagation Delay
- 5ps Skew Between Outputs
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D	Data Inputs
Q0, Q1	Data Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current 10EL 100EL		 26 26	 31 31		 26 26	 31 31		 26 26	 31 31		 26 30	 31 36	mA
V_{EE}	Power Supply Voltage 10EL 100EL	 –4.75 –4.20	 –5.2 –4.5	 –5.5 –5.5	 –4.75 –4.20	 –5.2 –4.5	 –5.5 –5.5	 –4.75 –4.20	 –5.2 –4.5	 –5.5 –5.5	 –4.75 –4.20	 –5.2 –4.5	 –5.5 –5.5	V
I_{IH}	Input HIGH Current			150			150			150			150	µA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

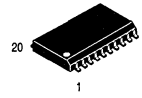
		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
t_{PLH} t_{PHL}	Propagation Delay to Output	135	260	385	185	260	335	190	265	340	215	290	365	ps
t_{SKEW}	Within-Device Skew[1] Duty Cycle Skew[2]		5 5			5 5	20 20		5 5	20 20		5 5	20 20	ps
V_{PP}	Minimum Input Swing[3]	150			150			150			150			mV
V_{CMR}	Common Mode Range[4]	–0.4		See[4]	–0.4		See[4]	–0.4		See[4]	–0.4		See[4]	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

1. Within-device skew defined as identical transitions on similar paths through a device.
2. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
3. Minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.
4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 2.5V.

Dual 1:3 Fanout Buffer

For information on the MC100EL13, please refer to the MC100LVEL13 datasheet on page 94 in the Low Voltage, Low Skew Fanout Buffer Section of this book.

MC100EL13

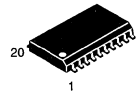


DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04

1:5 Clock Distribution Chip

MC100EL14

For information on the MC100EL14, please refer to the MC100LVEL14 datasheet on page 96 in the Low Voltage, Low Skew Fanout Buffer Section of this book.



DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-04

1:4 Clock Distribution Chip

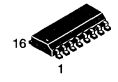
MC10EL15
MC100EL15

The MC10EL/100EL15 is a low skew 1:4 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. If a single-ended input is to be used the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01μF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EL15 under single-ended input conditions, as a result this pin can only source/sink up to 0.5mA of current.

The EL15 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

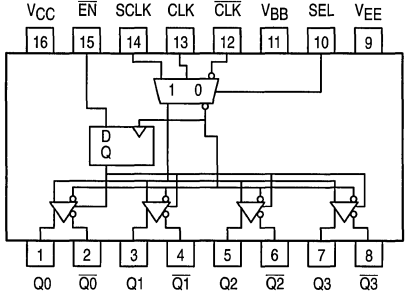
The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

- 50ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK	Diff Clock Inputs
SCLK	Scan Clock Input
$\overline{EN}$	Sync Enable
SEL	Clock Select Input
V_{BB}	Reference Output
Q_{0-3}	Diff Clock Outputs

FUNCTION TABLE

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK or SCLK

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V)	0 to –6.0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
V_{EE}	Operating Range[1,2]	–5.7 to –4.2	V

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2. Parametric values specified at: 100EL Series: –4.20V to –5.50V
   10EL Series: –4.94V to –5.50V

10EL SERIES
DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1])

		–40°C		0°C		25°C		85°C		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
V_{OH}	Output HIGH Voltage	–1080	–890	–1020	–840	–980	–810	–910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1650	–1950	–1630	–1950	–1630	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1230	–890	–1170	–840	–1130	–810	–1060	–720	mV
V_{IL}	Input LOW Voltge	–1950	–1500	–1950	–1480	–1950	–1480	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	µA

1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

100EL SERIES
DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1])

		–40°C			0°C to 85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	–1085	–1005	–880	–1025	–955	–880	mV	V_{IN} = V_{IH}(max)
V_{OL}	Output LOW Voltage	–1830	–1695	–1555	–1810	–1705	–1620	mV	or V_{IL}(min)
V_{OHA}	Output HIGH Voltage	–1095	—	—	–1035	—	—	mV	V_{IN} = V_{IH}(max)
V_{OLA}	Output LOW Voltage	—	—	–1555	—	—	–1610	mV	or V_{IL}(min)
V_{IH}	Input HIGH Voltage	–1165	—	–880	–1165	—	–880	mV	
V_{IL}	Input LOW Voltge	–1810	—	–1475	–1810	—	–1475	mV	
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	µA	V_{IN} = V_{IL}(max)

1. This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

AC/DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current 10EL 100EL		25 25	35 35		25 25	35 35		25 25	35 35		25 25	35 38	mA
V_{BB}	Output Reference Voltage 10EL 100EL	–1.43 –1.38		–1.30 –1.26	–1.38 –1.38		–1.27 –1.26	–1.35 –1.38		–1.25 –1.26	–1.31 –1.38		–1.19 –1.26	V
I_{IH}	Input High Current			150			150			150			150	µA
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	 460 410 410		 660 710 710	 470 420 420		 610 720 720	 470 420 420		 610 720 720	 500 450 470		 700 750 750	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew[1]			200 50			200 50			200 50			200 50	ps
t_S	Setup Time $\overline{EN}$	150			150			150			150			ps
t_H	HoldTime $\overline{EN}$	400			400			400			400			ps
V_{PP}	Minimum Input Swing CLK[2]	250			250			250			250			mV
V_{CMR}	Common Mode Range CLK[3]	–2.0		–0.4	–2.0		–0.4	–2.0		–0.4	–2.0		–0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)				325		575	325		575	325		575	ps

1. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
2. Minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.
3. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 2.5V.

1:9 Differential Clock Driver

MC10E111
MC100E111

1:9 DIFFERENTIAL CLOCK DRIVER

The MC10E/100E111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. It accepts one signal input, which can be either differential or else single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs. An enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

- Low Skew
- Guarateed Skew Spec
- Differential Design
- V_{BB} Output
- Enable
- Extended 100E V_{EE} Range of –4.2 to –5.46V
- 75kΩ Input Pulldown Resistors

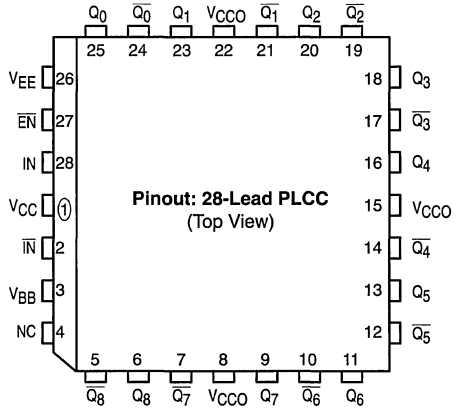
The device is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within-device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same V_{CCO}) as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

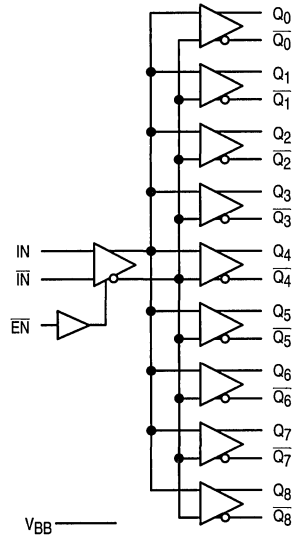
PIN NAMES

Pin	Function
IN, $\overline{IN}$	Differential Input Pair
$\overline{EN}$	Enable
Q_0, $\overline{Q_0}$–Q_8, $\overline{Q_8}$	Differential Outputs
V_{BB}	V_{BB} Output



Pinout: 28-Lead PLCC
(Top View)

LOGIC SYMBOL



DC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit	Cond
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{BB}	Output Reference Voltage 10E	–1.43		–1.30	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19	V	
	100E	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26		
I_{IH}	Input HIGH Current			150			150			150			150	µA	
I_{EE}	Power Supply Current 10E		48	60		48	60		48	60		48	60	mA	
	100E		48	60		48	60		48	60		55	69		
V_{PP}(DC)	Input Sensitivity	50			50			50			50			mV	1
V_{CMR}	Commom Mode Range	–1.6		–0.4	–1.6		–0.4	–1.6		–0.4	–1.6		–0.4	V	2

1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit	Cond
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (Diff)	380		680	460		560	480		580	510		610	ps	1
	IN (SE)	280		780	410		610	430		630	460		660		2
	Enable	400		900	450		850	450		850	450		850		3
	Disable	400		900	450		850	450		850	450		850		3
t_S	Setup Time $\overline{EN}$ to IN	250	0		200	0		200	0		200	0		ps	5
t_H	Hold Time IN to $\overline{EN}$	50	–200		0	–200		0	–200		0	–200		ps	6
t_R	Release Time $\overline{EN}$ to IN	350	100		300	100		300	100		300	100		ps	7
t_{skew}	Within-Device Skew		25	75		25	50		25	50		25	50	ps	4
V_{PP}(AC)	Minimum Input Swing	250			250			250			250			mV	8
t_r, t_f	Rise/Fall Time	250	450	650	275	375	600	275	375	600	275	375	600	ps	

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
3. Enable is defined as the propagation delay from the 50% point of a **negative** transition on $\overline{EN}$ to the 50% point of a **positive** transition on Q (or a negative transition on $\overline{Q}$). Disable is defined as the propagation delay from the 50% point of a **positive** transition on $\overline{EN}$ to the 50% point of a **negative** transition on Q (or a positive transition on $\overline{Q}$).
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. The setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition (see Figure 1).
6. The hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or a positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition (see Figure 2).
7. The release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E111 as a differential input as low as 50 mV will still produce full ECL levels at the output.

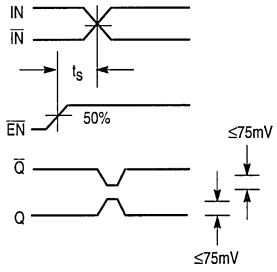


Figure 1. Setup Time

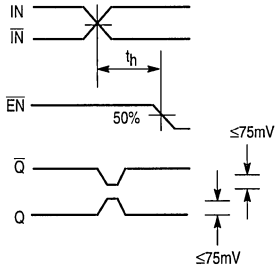


Figure 2. Hold Time

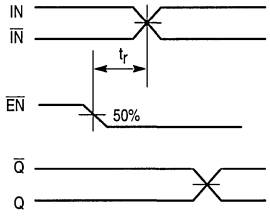


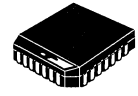
Figure 3. Release Time

Low Voltage Dual 1:4, 1:5 Differential Fanout Buffer
ECL/PECL Compatible

For information on the MC100E210, please refer to the MC100LVE210 datasheet on page 102 in the Low Voltage, Low Skew Fanout Buffer Section of this book.

MC100E210

LOW VOLTAGE
DUAL 1:4, 1:5 DIFFERENTIAL
FANOUT BUFFER

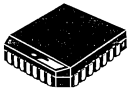


FN SUFFIX
PLASTIC PACKAGE
CASE 776–02

1:6 Differential Clock Distribution Chip

MC10E211
MC100E211

1:6 DIFFERENTIAL CLOCK DISTRIBUTION CHIP



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

The MC10E/100E211 is a low skew 1:6 fanout device designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal (PECL is an acronym for Positive ECL, PECL levels are ECL levels referenced to +5V rather than ground). If a single-ended input is to be used the V_{BB} pin should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01μF capacitor. The V_{BB} supply is designed to act as the switching reference for the input of the E211 under single-ended input conditions, as a result this pin can only source/sink up to 0.5mA of current.

- Guaranteed Low Skew Specification
- Synchronous Enabling/Disabling
- Multiplexed Clock Inputs
- V_{BB} Output for Single-Ended Use
- Internal 75kΩ Input Pulldown Resistors
- Common and Individual Enable/Disable Control
- High Bandwidth Output Transistors
- Extended 100E V_{EE} Range of –4.2V to –5.46V

The E211 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open in which case it will be pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

Both a common enable and individual output enables are provided. When asserted the positive output will go LOW on the next negative transition of the CLK (or SCLK) input. The enabling function is synchronous so that the outputs will only be enabled/disabled when the outputs are already in the LOW state. In this way the problem of runt pulse generation during the disable operation is avoided. Note that the internal flip flop is clocked on the falling edge of the input clock edge, therefore all associated specifications are referenced to the negative edge of the CLK input.

The output transitions of the E211 are faster than the standard ECLinPS™ edge rates. This feature provides a means of distributing higher frequency signals than capable with the E111 device. Because of these edge rates and the tight skew limits guaranteed in the specification, there are certain termination guidelines which must be followed. For more details on the recommended termination schemes please refer to the applications information section of this data sheet.

FUNCTION TABLE

CLK	SCLK	SEL	$\overline{ENx}$	Q
H/L	X	L	L	CLK
X	H/L	H	L	SCLK
Z*	Z*	X	H	L

* Z = Negative transition of CLK or SCLK

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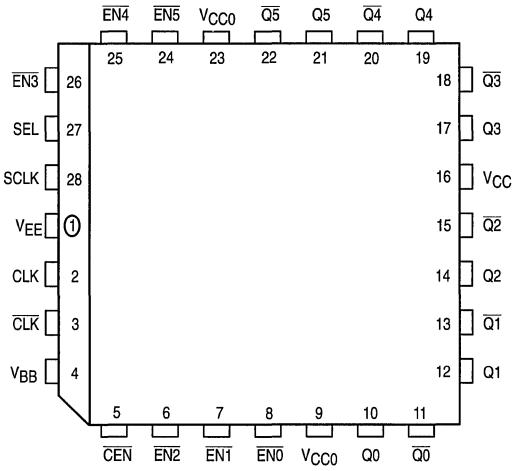
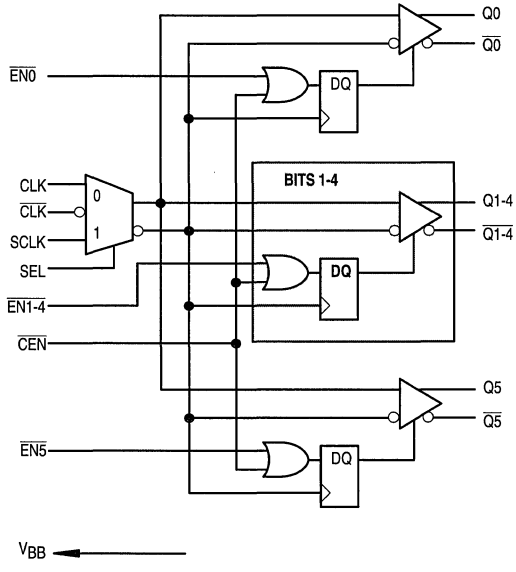


Pinout: 28-Lead PLCC (Top View)



Logic Diagram

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Characteristic	Symbol	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Output Reference Voltage	V_{BB}										V	
10E		–1.38		–1.27	–1.35		–1.25	–1.31		–1.19		
100E		–1.38		–1.26	–1.38		–1.26	–1.38		–1.26		
Input High Current	I_{IH}			150			150			150	µA	
Power Supply Current	I_{EE}										mA	
10E			119	160		119	160		119	160		
100E			119	160		119	160		137	164		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Characteristic	Symbol	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Propagation Delay to Output	t_{PLH}										ps	
CLK to Q (Diff)	t_{PHL}	795	930	1065	805	940	1075	825	960	1095		
CLK to Q (SE)		745	930	1115	755	940	1125	775	960	1145		
SCLK to Q		650	900	1085	650	910	1095	650	930	1115		
SEL to Q		745	970	1195	755	980	1205	775	1000	1225		
Disable Time	t_{PHL}										ps	
CLK or SCLK to Q			600	800		600	800		600	800		2
Part–to–Part Skew	t_{skew}										ps	
CLK (Diff) to Q				270			270			270		
CLK (SE), SCLK to Q				370			370			370		
Within-Device Skew			50	75		50	75			75		1
Setup Time	t_s										ps	
$\overline{EN}$x to CLK		200	–100		200	–100		200	–100			
$\overline{CEN}$ to CLK		200	0		200	0		200	0			2
Hold Time	t_h										ps	
CLK to $\overline{EN}$x, $\overline{CEN}$		900	600		900	160		900	600			2
Minimum Input Swing (CLK)	V_{PP}	0.25		1.0	0.25		1.0	0.25		1.0	V	3
Com. Mode Range (CLK)	V_{CMR}	–0.4		Note	–0.4		Note	–0.4		Note	V	4
Rise/Fall Times	t_r										ps	
20 – 80%	t_f	150		400	150		400	150		400		

1. Within-Device skew is defined for identical transitions on similar paths through a device.
2. Setup, Hold and Disable times are all relative to a falling edge on CLK or SCLK.
3. Minimum input swing for which AC parameters are guaranteed. Full DC ECL output swings will be generated with only 50mV input swings.
4. The range in which the high level of the input swing must fall while meeting the V_{PP} spec. The lower end of the range is V_{EE} dependent and can be calculated as V_{EE} + 2.4V.

APPLICATIONS INFORMATION

General Description

The MC10E/100E211 is a 1:6 fanout tree designed explicitly for low skew high speed clock distribution. The device was targeted to work in conjunction with the E111 device to provide another level of flexibility in the design and implementation of clock distribution trees. The individual synchronous enable controls and multiplexed clock inputs make the device ideal as the first level distribution unit in a distribution tree. The device provides the ability to distribute a lower speed scan or test clock along with the high speed system clock to ease the design of system diagnostics and self test procedures. The individual enables could be used to allow for the disabling of individual cards on a backplane in fault tolerant designs.

Because of lower fanout and larger skews the E211 will not likely be used as an alternative to the E111 for the bulk of the clock fanout generation. Figure 1 shows a typical application combining the two devices to take advantage of the strengths of each.

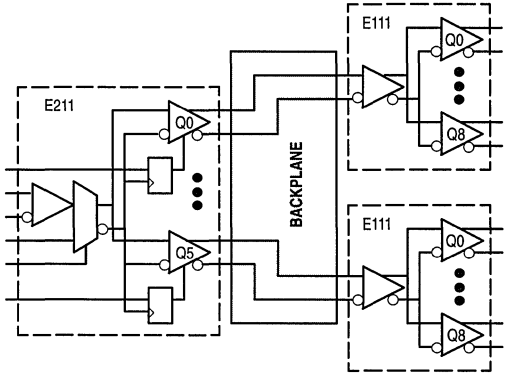


Figure 1. Standard E211 Application

Using the E211 in PECL Designs

The E211 device can be utilized very effectively in designs utilizing only a +5V power supply. Since the internal switching reference levels are biased off of the V_{CC} supply the input thresholds for the single-ended inputs will vary with V_{CC}. As a result the single-ended inputs should be driven by a device on the same board as the E211. Driving these inputs across a backplane where significant differences between the V_{CC}'s of the transmitter and receiver can occur can lead to AC performance and/or significant noise margin degradations. Because the differential I/O does not use a switching reference, and due to the CMR range of the E211, even under worst case V_{CC} situations between cards there will be no AC performance or noise margin loss for the differential CLK inputs.

For situations where TTL clocks are required the E211 can be interfaced with the H641 or H643 ECL to TTL Clock Distribution Chips from Motorola. The H641 is a single supply 1:9 PECL to TTL device while the H643 is a 1:8 dual supply standard ECL to TTL device. By combining the superior skew performance of the E211, or E111, with the low skew translating capabilities of the H641 and H643 very low skew TTL clock distribution networks can be realized.

Handling Open Inputs and Outputs

All of the input pins of the E211 have a 50kΩ to 75kΩ pulldown resistor to pull the input to V_{EE} when left open. This feature can cause a problem if the differential clock inputs are left open as the input gate current source transistor will become saturated. Under these conditions the outputs of the CLK input buffer will go to an undefined state. It is recommended, if possible,that the SCLK input should be selected any time the differential CLK inputs are allowed to float. The SCLK buffer, under open input conditions, will maintain a defined output state and thus the Q outputs of the device will be in a defined state (Q = LOW). Note that if all of the inputs are left open the differential CLK input will be selected and the state of the Q outputs will be undefined.

With the simultaneous switching characteristics and the tight skew specifications of the E211 the handling of the unused outputs becomes critical. To minimize the noise generated on the die all outputs should be terminated in pairs, ie. both the true and compliment outputs should be terminated even if only one of the outputs will be used in the system. With both complimentary pairs terminated the current in the V_{CC} pins will remain essentially constant and thus inductance induced voltage glitches on V_{CC} will not occur. V_{CC} glitches will result in distorted output waveforms and degradations in the skew performance of the device.

The package parasitics of the 28-lead PLCC cause the signals on a given pin to be influenced by signals on adjacent pins. The E211 is characterized and tested with all of the outputs switching, therefore the numbers in the data book are guaranteed only for this situation. If all of the outputs of the E211 are not needed and there is a desire to save power the unused output pairs can be left unterminated. Unterminated outputs can influence the propagation delay on adjacent pins by 15ps - 20ps. Therefore under these conditions this 15ps - 20ps needs to be added to the overall skew of the device. Pins which are separated by a package corner are not considered adjacent pins in the context of propagation delay influence. Therefore as long as all of the outputs on a single side of the package are terminated the specification limits in the data sheet will apply.

APPLICATIONS INFORMATION

Differential versus Single-Ended Use

As can be seen from the data sheet, to minimize the skew of the E211 the device must be used in the differential mode. In the single-ended mode the propagation delays are dependent on the relative position of the V_{BB} switching reference. Any V_{BB} offset from the center of the input swing will add delay to either the T_{PLH} or T_{PHL} and subtract delay from the other. This increase and decrease in delay will lead to an increase in the duty cycle skew and thus part-to-part skew. The within-device skew will be independent of the V_{BB} and therefore will be the same regardless of whether the device is driven differentially or single-endedly.

For applications where part-to-part skew or duty cycle skew are not important the advantages of single-ended clock distribution may lead to its use. Using single-ended interconnect will reduce the number of signal traces to be routed, but remember that all of the complimentary outputs still need to be terminated therefore there will be no reduction in the termination components required. To use the E211 with a single-ended input the arrangement pictured in Figure 2b should be used. If the input to the differential CLK inputs are AC coupled as pictured in Figure 2a the dependence on a centered V_{BB} reference is removed. The situation pictured will ensure that the input is centered around the bias set by the V_{BB}. As a result when AC coupled the AC specification limits for a differential input can be used. For more information on AC coupling please refer to the interfacing section of the design guide in the ECLinPS data book.

Using the Enable Pins

Both the common enable ($\overline{CEN}$) and the individual enables ($\overline{ENx}$) are synchronous to the CLK or SCLK input depending on which is selected. The active low signals are clocked into the enable flip flops on the negative edges of the E211 clock inputs. In this way the devices will only be disabled when the outputs are already in the LOW state. The internal propagation delays are such that the delay to the output through the distribution buffers is less than that through the enable flip flops. This will ensure that the disabling of the device will not slice any time off the clock pulse. On initial power up the enable flip flops will randomly attain a stable state, therefore precautions should be taken on initial power up to ensure the E211 is in the desired state.

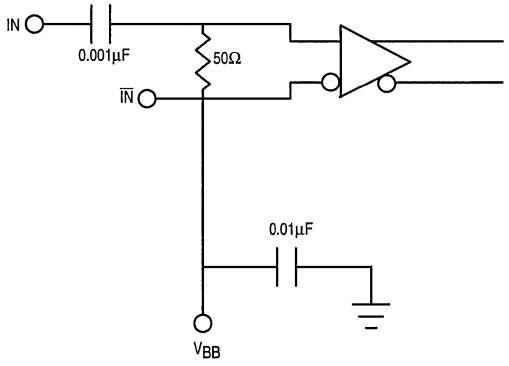


Figure 2a. AC Coupled Input

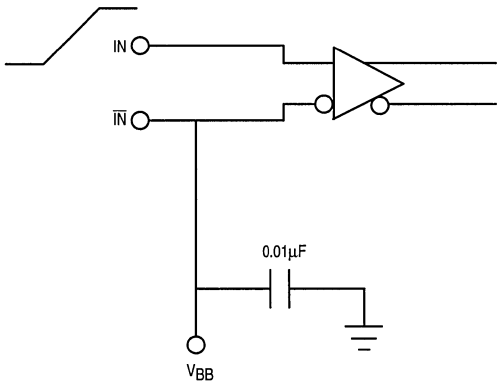


Figure 2b. Single-Ended Input

Product Preview

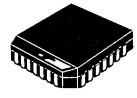
Low Voltage 2:8 Differential Fanout Buffer

ECL/PECL Compatible

For information on the MC100E310, please refer to the MC100LVE310 datasheet on page 110 in the Low Voltage, Low Skew Fanout Buffer Section of this book.

MC100E310

LOW VOLTAGE
2:8 DIFFERENTIAL
FANOUT BUFFER



FN SUFFIX
PLASTIC PACKAGE
CASE 776–02

Low Voltage, Low Skew Fanout Buffers

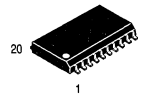
Dual 1:3 Fanout Buffer

MC100LVEL13
MC100EL13

The MC100LVEL13 is a dual, fully differential 1:3 fanout buffer. The MC100EL13 is pin and functionally equivalent to the MC100LVEL13 but is specified for operation at the standard 100E ECL voltage supply. The Low Output–Output Skew of the device makes it ideal for distributing two different frequency synchronous signals.

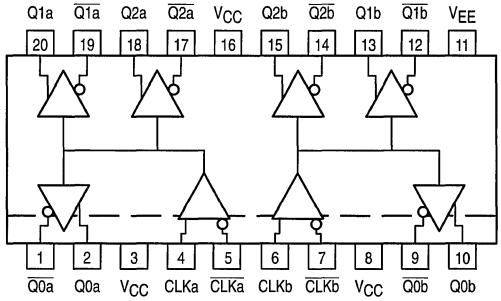
The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to V_{EE}, The $\overline{D}$ input will bias around $V_{CC}/2$ and the Q output will go LOW.

- Differential Inputs and Outputs
- 20–Lead SOIC Packaging
- 500ps Typical Propagation Delays
- 50ps Output–Output Skews
- Supports Both Standard and Low Voltage 100K ECL
- >2000V ESD Protection



DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04

Logic Diagram and Pinout: 20–Lead SOIC (Top View)



PIN NAMES

Pins	Function
Qna, $\overline{Qna}$	Differential Clock Outputs
Qnb, $\overline{Qnb}$	Differential Clock Outputs
CLKn, $\overline{CLKn}$	Differential Clock Inputs

MC100LVEL13
DC CHARACTERISTICS (V_{EE} = –3.0V to –3.8V; V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		30	38		30	38		30	38		32	40	mA
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{INL}	Input LOW Current Dn $\overline{Dn}$	0.5 –300			0.5 –300			0.5 –300			0.5 –300			µA

MC100LVEL13
AC CHARACTERISTICS (V_{EE} = –3.0V to –3.8V; V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay CLK→Q/$\overline{Q}$	410		600	420		610	430		620	450		640	ps
$t_{sk(O)}$	Output–Output Skew Any Qa→Qa, Any Qb→Qb Any Qa→Any Qb			50 75			50 75			50 75			50 75	ps
$t_{sk(DC)}$	Duty Cycle Skew $\lvert t_{PLH} - t_{PHL} \rvert$			50			50			50			50	ps
V_{PP}	Minimum Input Swing[1]	150		1000	150		1000	150		1000	150		1000	mV
V_{CMR}	Common Mode Range[2] V_{PP} < 500mV V_{PP} ≥ 500mV	 –2.0 –1.8		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	230		500	ps

1. Minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR}(min) will be fixed at 3.3V – $\lvert V_{CMR}(min) \rvert$.

MC100EL13
DC CHARACTERISTICS (V_{EE} = –4.2V to –5.5V; V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		30	38		30	38		30	38		32	40	mA
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{INL}	Input LOW Current Dn $\overline{Dn}$	0.5 –300			0.5 –300			0.5 –300			0.5 –300			µA

MC100EL13
AC CHARACTERISTICS (V_{EE} = –4.2V to –5.5V; V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay CLK→Q/$\overline{Q}$	410		600	420		610	430		620	450		640	ps
$t_{sk(O)}$	Output–Output Skew Any Qa→Qa, Any Qb→Qb Any Qa→Any Qb			50 75			50 75			50 75			50 75	ps
$t_{sk(DC)}$	Duty Cycle Skew $\lvert t_{PLH} - t_{PHL} \rvert$			50			50			50			50	ps
V_{PP}	Minimum Input Swing[1]	150		1000	150		1000	150		1000	150		1000	mV
V_{CMR}	Common Mode Range[2] V_{PP} < 500mV V_{PP} ≥ 500mV	 –3.2 –3.0		 –0.4 –0.4	 –3.3 –3.1		 –0.4 –0.4	 –3.3 –3.1		 –0.4 –0.4	 –3.3 –3.1		 –0.4 –0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	230		500	ps

1. Minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –4.5V. Note for PECL operation, the V_{CMR}(min) will be fixed at 5.0V – $\lvert V_{CMR}(min) \rvert$.

1:5 Clock Distribution Chip

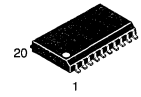
MC100LVEL14
MC100EL14

The MC100LVEL/100EL14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The LVEL14 is functionally and pin compatible with the EL14 but is designed to operate in ECL or PECL mode for a voltage supply range of –3.0V to –3.8V (or 3.0V to 3.8V). If a single-ended input is to be used the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the LVEL14 under single-ended input conditions, as a result this pin can only source/sink up to 0.5mA of current.

The LVEL14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

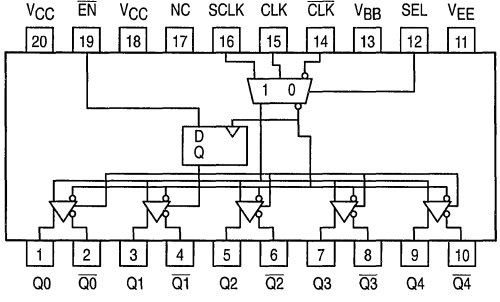
The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

- 50ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- 75kΩ Internal Input Pulldown Resistors
- >2000V ESD Protection
- V_{EE} Range of –3.0V to –5.5V



DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK	Diff Clock Inputs
SCLK	Scan Clock Input
$\overline{EN}$	Sync Enable
SEL	Clock Select Input
V_{BB}	Reference Output
$Q_{0–4}$	Diff Clock Outputs

FUNCTION TABLE

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK or SCLK

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V)	0 to –6.0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
V_{EE}	Operating Range[1,2]	–5.7 to –4.2	V

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2. Parametric values specified at: 100EL Series: –4.20V to –5.50V
   10EL Series: –4.94V to –5.50V

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1])

		–40°C			0°C to 85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	–1085	–1005	–880	–1025	–955	–880	mV	V_{IN} = V_{IH}(max)
V_{OL}	Output LOW Voltage	–1830	–1695	–1555	–1810	–1705	–1620	mV	or V_{IL}(min)
V_{OHA}	Output HIGH Voltage	–1095	—	—	–1035	—	—	mV	V_{IN} = V_{IH}(max)
V_{OLA}	Output LOW Voltage	—	—	–1555	—	—	–1610	mV	or V_{IL}(min)
V_{IH}	Input HIGH Voltage	–1165	—	–880	–1165	—	–880	mV	
V_{IL}	Input LOW Voltage	–1810	—	–1475	–1810	—	–1475	mV	
I_{IL}	Input LOW Current $\overline{CLK}$ Others	–300 0.5	—	—	–300 0.5	—	—	µA	V_{IN} = V_{IL}(max)

1. This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –3.0V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

MC100LVEL14 AC/DC CHARACTERISTICS (V_{EE} = –3.8V to –3.0V; V_{CC} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current 100LVEL 100EL		32 32	40 40		32 32	40 40		32 32	40 40		34 34	42 42	mA
V_{BB}	Output Ref 100LVEL Voltage 100EL	–1.43 –1.38		–1.30 –1.26	–1.38 –1.38		–1.27 –1.26	–1.35 –1.38		–1.25 –1.26	–1.31 –1.38		–1.19 –1.26	V
I_{IH}	Input High Current			150			150			150			150	µA
t_{PLH} t_{PHL}	Prop CLK to Q (Diff) Delay CLK to Q (SE) SCLK to Q	520 470 470		720 770 770	550 500 500		750 800 800	580 530 530	680 680 680	780 830 830	630 580 580		830 880 880	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew[1]			200 50			200 50			200 50			200 50	ps
t_S	Setup Time $\overline{EN}$	0			0			0			0			ps
t_H	Hold Time $\overline{EN}$	0			0			0			0			ps
V_{PP}	Minimum Input Swing CLK	150			150			150			150			mV
V_{CMR}	Common Mode Range[2] V_{PP} < 500mV V_{PP} ≥ 500mV	–2.0 –1.8		–0.4 –0.4	–2.1 –1.9		–0.4 –0.4	–2.1 –1.9		–0.4 –0.4	–2.1 –1.9		–0.4 –0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	230		500	ps

1. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR}(min) will be fixed at 3.3V – |V_{CMR}(min)|.

MC100EL14 AC/DC CHARACTERISTICS (V_{EE} = –4.2V to –5.5V; V_{CC} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current 100LVEL 100EL		32 32	40 40		32 32	40 40		32 32	40 40		34 34	42 42	mA
V_{BB}	Output Ref 100LVEL Voltage 100EL	–1.43 –1.38		–1.30 –1.26	–1.38 –1.38		–1.27 –1.26	–1.35 –1.38		–1.25 –1.26	–1.31 –1.38		–1.19 –1.26	V
I_{IH}	Input High Current			150			150			150			150	µA
t_{PLH} t_{PHL}	Prop CLK to Q (Diff) Delay CLK to Q (SE) SCLK to Q	520 470 470		720 770 770	550 500 500		750 800 800	580 530 530	680 680 680	780 830 830	630 580 580		830 880 880	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew[1]			200 50			200 50			200 50			200 50	ps
t_S	Setup Time $\overline{EN}$	0			0			0			0			ps
t_H	Hold Time $\overline{EN}$	0			0			0			0			ps
V_{PP}	Minimum Input Swing CLK	150			150			150			150			mV
V_{CMR}	Common Mode Range[2] V_{PP} < 500mV V_{PP} ≥ 500mV	–3.2 –3.0		–0.4 –0.4	–3.3 –3.1		–0.4 –0.4	–3.3 –3.1		–0.4 –0.4	–3.3 –3.1		–0.4 –0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	230		500	ps

1. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –4.5V. Note for PECL operation, the V_{CMR}(min) will be fixed at 5.0V – |V_{CMR}(min)|.

Low-Voltage 1:9 Differential ECL/PECL Clock Driver

MC100LVE111

LOW-VOLTAGE 1:9 DIFFERENTIAL ECL/PECL CLOCK DRIVER

The MC100LVE111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. The MC100LVE111's function and performance are similar to the popular MC100E111, with the added feature of low voltage operation. It accepts one signal input, which can be either differential or single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs.

- 200ps Part-to-Part Skew
- 50ps Output-to-Output Skew
- Differential Design
- V_{BB} Output
- Voltage and Temperature Compensated Outputs
- Low Voltage V_{EE} Range of –3.0 to –3.8V
- 75kΩ Input Pulldown Resistors

FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

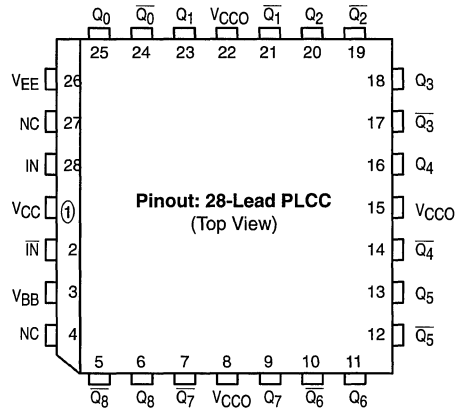
The LVE111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

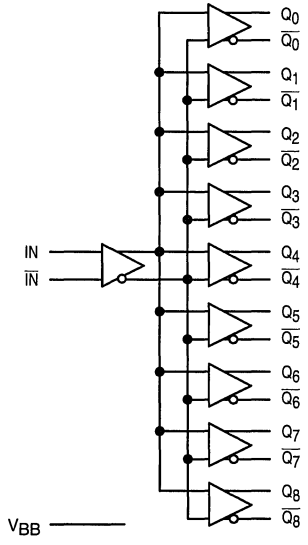
The MC100LVE111, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE111 to be used for high performance clock distribution in +3.3V systems. Designers can take advantage of the LVE111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For systems incorporating GTL, parallel termination offers the lowest power by taking advantage of the 1.2V supply as a terminating voltage. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

PIN NAMES

Pins	Function
IN, $\overline{IN}$	Differential Input Pair
Q_0, $\overline{Q_0}$–Q_8, $\overline{Q_8}$	Differential Outputs
V_{BB}	V_{BB} Output



LOGIC SYMBOL



ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–3.0		–3.8	–3.0		–3.8	–3.0		–3.8	–3.0		–3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current		55	66		55	66		55	66		65	78	mA

PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	V
V_{OL}	Output LOW Voltage[1]	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	V
V_{IH}	Input HIGH Voltage[1]	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage[1]	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{BB}	Output Reference Voltage[1]	1.92		2.04	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{CC}	Power Supply Voltage	3.0		3.8	3.0		3.8	3.0		3.8	3.0		3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current		55	66		55	66		55	66		65	78	mA

1. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single-ended)	 400 350		 650 700	 435 385		 625 675	 440 390		 630 680	 445 395		 635 685	ps	 Note 1 Note 2
t_{skew}	Within-Device Skew Part-to-Part Skew (Diff)			50 250			50 200			50 200			50 200	ps	Note 3
V_{PP}	Minimum Input Swing	500			500			500			500			mV	Note 4
V_{CMR}	Common Mode Range	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	V	Note 5
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
3. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E111 as a differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

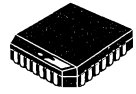
Low Voltage Dual 1:4, 1:5 Differential Fanout Buffer
ECL/PECL Compatible

MC100LVE210
MC100E210

LOW VOLTAGE
DUAL 1:4, 1:5 DIFFERENTIAL
FANOUT BUFFER

The MC100LVE210 is a low voltage, low skew dual differential ECL fanout buffer designed with clock distribution in mind. The device features two fanout buffers, a 1:4 and a 1:5 buffer, on a single chip. The device features fully differential clock paths to minimize both device and system skew. The dual buffer allows for the fanout of two signals through a single chip, thus reducing the skew between the two fundamental signals from a part–to–part skew down to an output–to–output skew. This capability reduces the skew by a factor of 4 as compared to using two LVE111's to accomplish the same task. The MC100LVE210 works from a –3.3V supply while the MC100E210 provides identical function and performance from a standard –4.5V 100E voltage supply.

- Dual Differential Fanout Buffers
- 200ps Part–to–Part Skew
- 50ps Typical Output–to–Output Skew
- Low Voltage ECL/PECL Compatible
- 28–lead PLCC Packaging

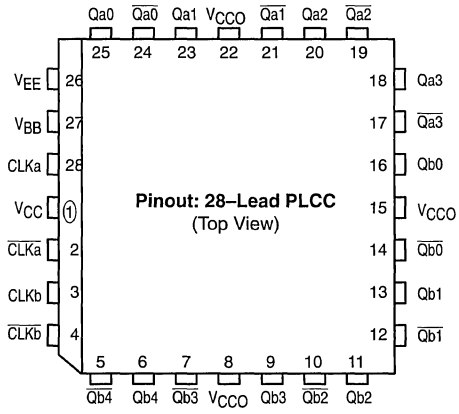


FN SUFFIX
PLASTIC PACKAGE
CASE 776–02

For applications which require a single–ended input, the V_{BB} reference voltage is supplied. For single–ended input applications the V_{BB} reference should be connected to the CLK input and bypassed to ground via a 0.01µf capacitor. The input signal is then driven into the CLK input.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used it is necessary to terminate at least the output pairs adjacent to the output pair being used in order to maintain minimum skew. Failure to follow this guideline will result in small degradations of propagation delay (on the order of 10–20ps) of the outputs being used, while not catastrophic to most designs this will result in an increase in skew. Note that the package corners isolate outputs from one another such that the guideline expressed above holds only for outputs on the same side of the package.

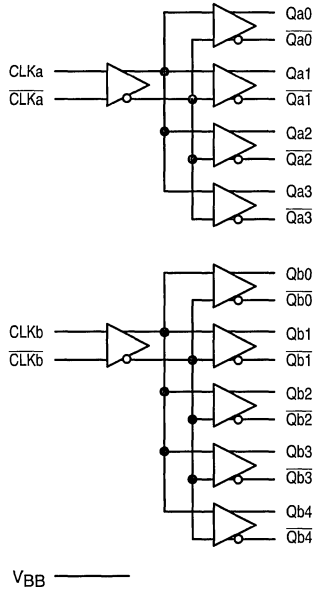
The MC100LVE210, as with most ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE210 to be used for high performance clock distribution in +3.3V systems. Designers can take advantage of the LVE210's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line terminations are typically used as they require no additional power supplies, if parallel termination is desired a terminating voltage of V_{CC}–2.0V will need to be provided. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.



PIN NAMES

Pins	Function
CLKa, CLKb	Differential Input Pairs
Qa0:4, Qb0:3	Differential Outputs
V_{BB}	V_{BB} Output

LOGIC SYMBOL



MC100LVE210
ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.085	–1.005	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.830	–1.695	–1.555	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–3.0		–3.8	–3.0		–3.8	–3.0		–3.8	–3.0		–3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current			55			55			55			65	mA

MC100LVE210
PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	2.215	2.295	2.42	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	V
V_{OL}	Output LOW Voltage[1]	1.47	1.605	1.745	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	V
V_{IH}	Input HIGH Voltage[1]	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage[1]	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{BB}	Output Reference Voltage[1]	1.92		2.04	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{CC}	Power Supply Voltage	3.0		3.8	3.0		3.8	3.0		3.8	3.0		3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current			55			55			55			65	mA

1. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

MC100LVE210
AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended)	 475 400		 675 700	 475 400		 675 700	 500 450		 700 750	 500 450		 700 750	ps	 Note 1 Note 2
t_{skew}	Within–Device Skew Qa→Qb Qa→Qa,Qb→Qb Part–to–Part Skew (Diff)		50 50	75 75 200		50 30	75 50 200		50 30	75 50 200		50 30	75 50 200	ps	Note 3
V_{PP}	Minimum Input Swing	500			500			500			500			mV	Note 4
V_{CMR}	Common Mode Range	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	V	Note 5
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
3. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the LVE210 as a differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

MC100E210
ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.085	–1.005	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.830	–1.695	–1.555	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–5.25		–4.2	–5.25		–4.2	–5.25		–4.2	–5.25		–4.2	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current			55			55			55			65	mA

MC100E210
PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	3.915	3.995	4.12	3.975	4.045	4.12	3.975	4.045	4.12	3.975	4.045	4.12	V
V_{OL}	Output LOW Voltage[1]	3.170	3.305	3.445	3.19	3.295	3.38	3.19	3.295	3.38	3.19	3.295	3.38	V
V_{IH}	Input HIGH Voltage[1]	3.835		4.12	3.835		4.12	3.835		4.12	3.835		4.12	V
V_{IL}	Input LOW Voltage[1]	3.190		3.525	3.190		3.525	3.190		3.525	3.190		3.525	V
V_{BB}	Output Reference Voltage[1]	3.62		3.74	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{CC}	Power Supply Voltage	4.75		5.25	4.75		5.25	4.75		5.25	4.75		5.25	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current			55			55			55			65	mA

1. These values are for V_{CC} = 5.0V. Level Specifications will vary 1:1 with V_{CC}.

MC100E210
AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended)	 475 400		 675 700	 475 400		 675 700	 500 450		 700 750	 500 450		 700 750	ps	 Note 1 Note 2
t_{skew}	Within–Device Skew Qa→Qb Qa→Qa,Qb→Qb Part–to–Part Skew (Diff)		50 50	75 75 200		50 30	75 50 200		50 30	75 50 200		50 30	75 50 200	ps	Note 3
V_{PP}	Minimum Input Swing	500			500			500			500			mV	Note 4
V_{CMR}	Common Mode Range	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	V	Note 5
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
3. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E210 as a differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

Low Voltage 1:15 Differential ÷1/÷2 ECL/PECL Clock Driver

MC100LVE222

LOW VOLTAGE 1:15 DIFFERENTIAL ÷1/÷2 ECL/PECL CLOCK DRIVER

The MC100LVE222 is a low voltage, low skew 1:15 differential ÷1/÷2 ECL fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The LVE222 can be used as a simple fanout buffer or outputs can be configured to provide half frequency outputs. The combination of 1x and 1/2x frequencies is flexible providing for a myriad of combinations. All timing differences between the 1x and 1/2x signals are compensated for internal to the chip so that the output–to–output skew is identical regardless of what output frequencies are selected.

- Fifteen Differential Outputs
- 200ps Part–to–Part Skew
- 50ps Output–to–Output Skew
- Selectable 1x or 1/2x Frequency Outputs
- Extended Power Supply Range of –3.0V to –5.25V (+3.0V to +5.25V)
- 52–Lead TQFP Packaging
- ESD > 2000V

FA SUFFIX
TQFP PACKAGE
CASE 848D–03

The fsel and CLK_Sel input pins are asynchronous control signals. As a result, changing these inputs could cause indeterminent excursions on the outputs immediately following the changes on the inputs.

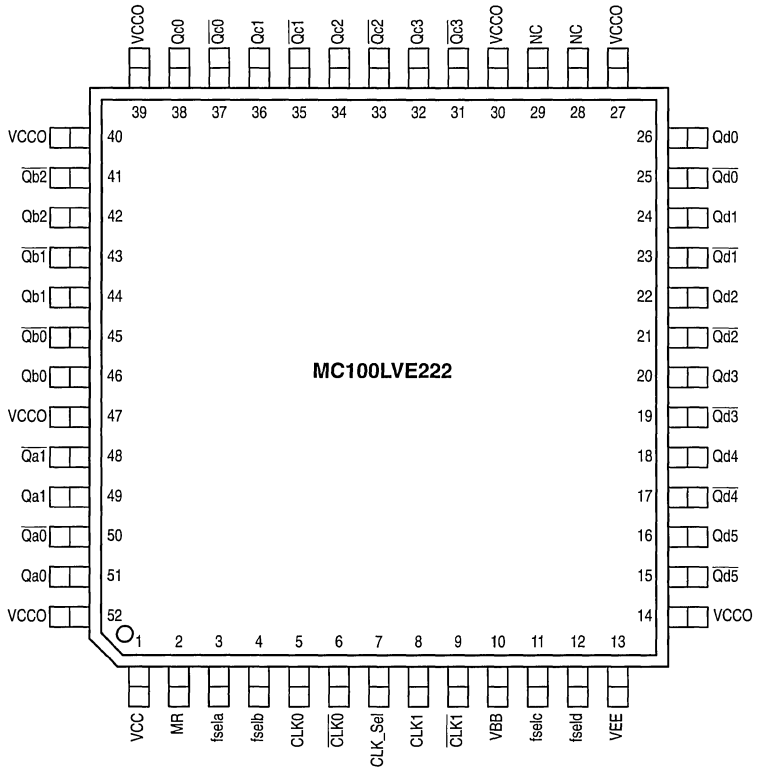
For applications which require a single–ended input, the V_{BB} reference voltage is supplied. For single–ended input applications the V_{BB} reference should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µf capacitor. The input signal is then driven into the CLK input.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications all fifteen differential pairs will be used and therefore terminated. In the case where fewer than fifteen pairs are used it is necessary to terminate at least the output pairs adjacent to the output pair being used in order to maintain minimum skew. Failure to follow this guideline will result in small degradations of propagation delay (on the order of 10–20ps) of the outputs being used, while not catastrophic to most designs this will result in an increase in skew. Note that the package corners isolate outputs from one another such that the guideline expressed above holds only for outputs on the same side of the package.

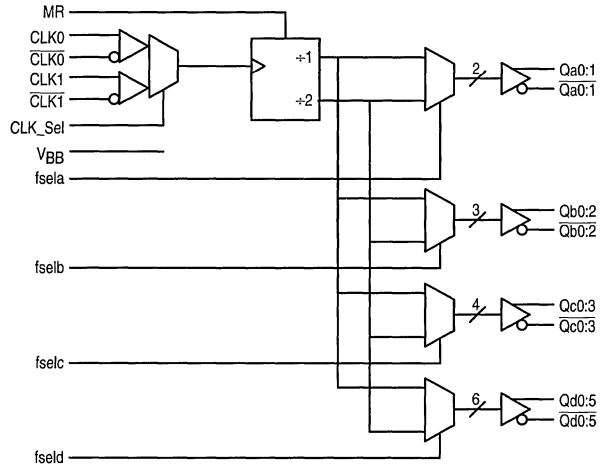
The MC100LVE222, as with most ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE222 to be used for high performance clock distribution in +3.3V systems. Designers can take advantage of the LVE222's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line, terminations are typically used as they require no additional power supplies, if parallel termination is desired a terminating voltage of V_{CC}–2.0V will need to be provided. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

The MC100LVE222 is packaged in the 52–lead TQFP package. For a 3.3V supply this package provides the optimum performance and minimizes board space requirements. The LVE222 will operate from a standard 100E –4.5V supply or a 5.0V PECL supply. The 52–lead TQFP utilizes a 10x10mm body with a lead pitch of 0.65mm.

Pinout: 52–Lead TQFP (Top View)



LOGIC SYMBOL



FUNCTION TABLE

Input	Function	
	0	1
MR	Active	Reset
CLK_Sel	CLK0	CLK1
fseln	÷1	÷2

ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.085	–1.005	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.830	–1.695	–1.555	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–3.0		–5.25	–3.0		–5.25	–3.0		–5.25	–3.0		–5.25	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input $\overline{CLK0}$, $\overline{CLK1}$ LOW Current Others	–300 0.5			–300 0.5			–300 0.5			–300 0.5			µA
I_{EE}	Power Supply Current		122	136		122	136		122	136		125	139	mA

PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	2.215	2.295	2.420	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	V
V_{OL}	Output LOW Voltage[1]	1.470	1.605	1.745	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	V
V_{IH}	Input HIGH Voltage[1]	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage[1]	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{BB}	Output Reference Voltage[1]	1.92		2.04	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{CC}	Power Supply Voltage	3.0		5.25	3.0		5.25	3.0		5.25	3.0		5.25	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input $\overline{CLK0}$, $\overline{CLK1}$ LOW Current Others	–300 0.5			–300 0.5			–300 0.5			–300 0.5			µA
I_{EE}	Power Supply Current		122	136		122	136		122	136		125	139	mA

1. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

ECL AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

		–40°C			0°C			25°C			70°C				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended) MR	 1040 990 1100	 1140 1140 1250	 1240 1290 1400	 1060 1010 1130	 1160 1160 1280	 1260 1310 1430	 1080 1030 1170	 1180 1180 1320	 1280 1330 1470	 1120 1070 1220	 1220 1220 1370	 1320 1370 1520	ps	 Note 1. Note 2.
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)			50 200			50 200			50 200			50 200	ps	Note 3.
V_{PP}	Minimum Input Swing	400			400			400			400			mV	Note 4.
V_{CMR}	Common Mode Range V_{PP} < 500mV V_{PP} ≥ 500mV	 V_{EE} +1.3 V_{EE} +1.6	 	 –0.4 –0.4	 V_{EE} +1.2 V_{EE} +1.5	 	 –0.4 –0.4	 V_{EE} +1.2 V_{EE} +1.5	 	 –0.4 –0.4	 V_{EE} +1.2 V_{EE} +1.5	 	 –0.4 –0.4	V	Note 5.
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
3. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the LVE222. A differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

PECL AC CHARACTERISTICS (V_{EE} = GND; V_{CC} = V_{CCO} = V_{CC} (min) to V_{CC} (max))

		–40°C			0°C			25°C			70°C				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended) MR	 1040 990 1100	 1140 1140 1250	 1240 1290 1400	 1060 1010 1130	 1160 1160 1280	 1260 1310 1430	 1080 1030 1170	 1180 1180 1320	 1280 1330 1470	 1120 1070 1220	 1220 1220 1370	 1320 1370 1520	ps	 Note 1. Note 2.
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)			50 200			50 200			50 200			50 200	ps	Note 3.
V_{PP}	Minimum Input Swing	400			400			400			400			mV	Note 4.
V_{CMR}	Common Mode Range V_{PP} < 500mV V_{PP} ≥ 500mV	 1.3 1.6	 	 V_{CC} –0.4 V_{CC} –0.4	 1.2 1.5	 	 V_{CC} –0.4 V_{CC} –0.4	 1.2 1.5	 	 V_{CC} –0.4 V_{CC} –0.4	 1.2 1.5	 	 V_{CC} –0.4 V_{CC} –0.4	V	Note 5.
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
3. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the LVE222. A differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

Low Voltage 2:8 Differential Fanout Buffer
ECL/PECL Compatible

MC100LVE310
MC100E310

LOW VOLTAGE
2:8 DIFFERENTIAL
FANOUT BUFFER

The MC100LVE310 is a low voltage, low skew 2:8 differential ECL fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The LVE310 offers two selectable clock inputs to allow for redundant or test clocks to be incorporated into the system clock trees. The MC100E310 is pin compatible to the National 100310 device. The MC100LVE310 works from a –3.3V supply while the MC100E310 provides identical function and performance from a standard –4.5V 100E voltage supply.

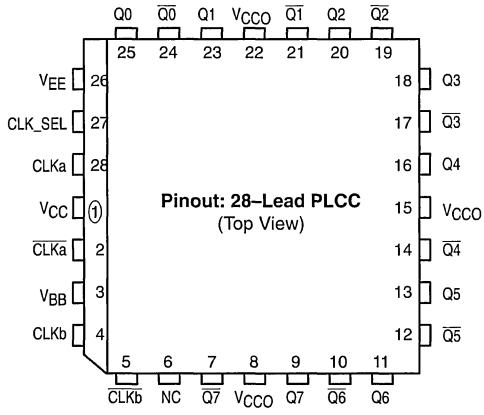
- Dual Differential Fanout Buffers
- 200ps Part–to–Part Skew
- 50ps Output–to–Output Skew
- Low Voltage ECL/PECL Compatible
- 28–lead PLCC Packaging

FN SUFFIX
PLASTIC PACKAGE
CASE 776–02

For applications which require a single–ended input, the V_{BB} reference voltage is supplied. For single–ended input applications the V_{BB} reference should be connected to the CLK input and bypassed to ground via a 0.01µf capacitor. The input signal is then driven into the CLK input.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used it is necessary to terminate at least the output pairs adjacent to the output pair being used in order to maintain minimum skew. Failure to follow this guideline will result in small degradations of propagation delay (on the order of 10–20ps) of the outputs being used, while not catastrophic to most designs this will result in an increase in skew. Note that the package corners isolate outputs from one another such that the guideline expressed above holds only for outputs on the same side of the package.

The MC100LVE310, as with most ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE310 to be used for high performance clock distribution in +3.3V systems. Designers can take advantage of the LVE310's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line terminations are typically used as they require no additional power supplies, if parallel termination is desired a terminating voltage of V_{CC}–2.0V will need to be provided. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

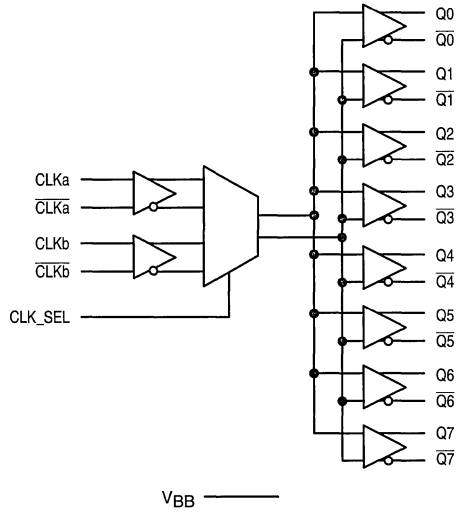


PIN NAMES

Pins	Function
CLKa, CLKb	Differential Input Pairs
Q0:7	Differential Outputs
V_{BB}	V_{BB} Output
CLK_SEL	Input Clock Select

CLK_SEL	Input Clock
0	CLKa Selected
1	CLKb Selected

LOGIC SYMBOL



MC100LVE310
ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.085	–1.005	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.830	–1.695	–1.555	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–3.0		–3.8	–3.0		–3.8	–3.0		–3.8	–3.0		–3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current		55	60		55	60		55	60		65	70	mA

MC100LVE310
PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	2.215	2.295	2.42	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	V
V_{OL}	Output LOW Voltage[1]	1.47	1.605	1.745	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	V
V_{IH}	Input HIGH Voltage[1]	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage[1]	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{BB}	Output Reference Voltage[1]	1.92		2.04	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{CC}	Power Supply Voltage	3.0		3.8	3.0		3.8	3.0		3.8	3.0		3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current		55	60		55	60		55	60		65	70	mA

1. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

MC100LVE310
AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended)	 525 500		 725 750	 550 525		 750 775	 550 550		 750 800	 575 600		 775 850	ps	 Note 1 Note 2
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)			75 250			75 200			50 200			50 200	ps	Note 3
V_{PP}	Minimum Input Swing	500			500			500			500			mV	Note 4
V_{CMR}	Common Mode Range	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	V	Note 5
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
3. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the LVE310 as a differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

MC100E310
ECL DC CHARACTERISTICS

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	–1.085	–1.005	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.830	–1.695	–1.555	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–5.25		–4.2	–5.25		–4.2	–5.25		–4.2	–5.25		–4.2	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current		55	60		55	60		55	60		65	70	mA

MC100E310
PECL DC CHARACTERISTICS

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage[1]	3.915	3.995	4.12	3.975	4.045	4.12	3.975	4.045	4.12	3.975	4.045	4.12	V
V_{OL}	Output LOW Voltage[1]	3.170	3.305	3.445	3.19	3.295	3.38	3.19	3.295	3.38	3.19	3.295	3.38	V
V_{IH}	Input HIGH Voltage[1]	3.835		4.12	3.835		4.12	3.835		4.12	3.835		4.12	V
V_{IL}	Input LOW Voltage[1]	3.190		3.525	3.190		3.525	3.190		3.525	3.190		3.525	V
V_{BB}	Output Reference Voltage[1]	3.62		3.74	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{CC}	Power Supply Voltage	4.75		5.25	4.75		5.25	4.75		5.25	4.75		5.25	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current		55	60		55	60		55	60		65	70	mA

1. These values are for V_{CC} = 5.0V. Level Specifications will vary 1:1 with V_{CC}.

MC100E310
AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

		–40°C			0°C			25°C			85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended)	 525 500		 725 750	 550 525		 750 775	 550 550		 750 800	 575 600		 775 850	ps	 Note 1 Note 2
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)			75 250			75 200			50 200			50 200	ps	Note 3
V_{PP}	Minimum Input Swing	500			500			500			500			mV	Note 4
V_{CMR}	Common Mode Range	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	V	note 5
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
3. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E310 as a differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

Product Preview

Low-Voltage 1:10 Differential ECL/PECL Clock Driver

MC100EP111

LOW–VOLTAGE 1:10 DIFFERENTIAL ECL/PECL CLOCK DRIVER

The MC100EP111 is a low skew 1–to–10 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The input signals can be either differential or single–ended if the V_{BB} output is used. The selected signal is fanned out to 10 identical differential outputs.

- 100ps Part–to–Part Skew
- 35ps Output–to–Output Skew
- Differential Design
- V_{BB} Output
- Voltage and Temperature Compensated Outputs
- Low Voltage V_{EE} Range of –2.375 to –3.8V
- 75kΩ Input Pulldown Resistors

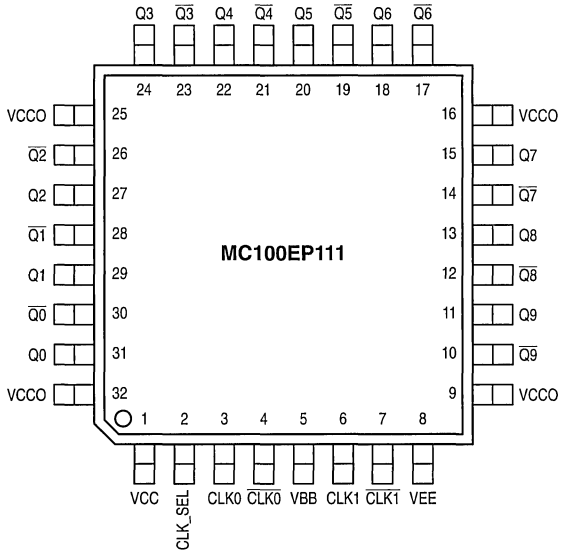
FA SUFFIX
32–LEAD TQFP PACKAGE
CASE 873A–02

The EP111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate–to–gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100EP111, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the EP111 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

Pinout: 32–Lead TQFP
(Top View)



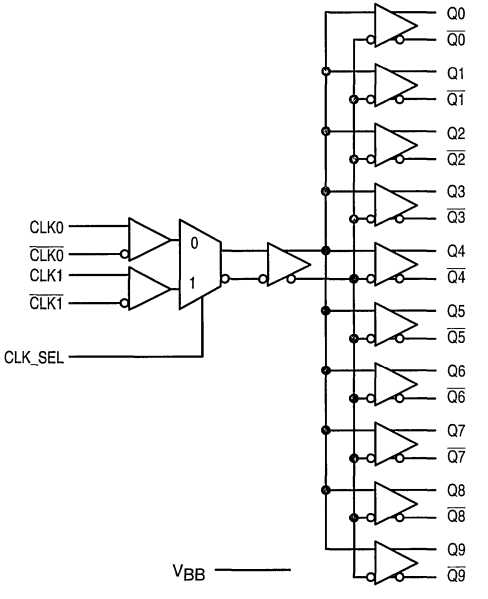
PIN NAMES

Pins	Function
CLKn, $\overline{\text{CLKn}}$	Differential Input Pairs
Q0:9, $\overline{\text{Q0:9}}$	Differential Outputs
CLK_SEL	Active Clock Select Input
VBB	V_{BB} Output

FUNCTION

CLK_SEL	Active Input
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

LOGIC SYMBOL



ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–2.375		–3.8	–2.375		–3.8	–2.375		–3.8	–2.375		–3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current													mA

PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (1.)	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	V
V_{OL}	Output LOW Voltage (1.)	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	V
V_{IH}	Input HIGH Voltage (1.)	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage (1.)	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{BB}	Output Reference Voltage (Note 1.)	1.92		2.04	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{CC}	Power Supply Voltage	2.375		3.8	2.375		3.8	2.375		3.8	2.375		3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current													mA

1. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended)								 400 400					ps	
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)		 35 100			 35 100			 35 100			 35 100		ps	
f_{max}	Maximum Input Frequency		1.5			1.5			1.5			1.5		GHz	
V_{PP}	Minimum Input Swing	500			500			500			500			mV	
V_{CMR}	Common Mode Range													V	
t_r/t_f	Output Rise/Fall Time		200			200			200			200		ps	20%–80%

Product Preview

Low-Voltage 1:20 Differential ECL/PECL Clock Driver

MC100EP221

LOW–VOLTAGE 1:20 DIFFERENTIAL ECL/PECL CLOCK DRIVER

The MC100EP221 is a low skew 1–to–20 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The input signals can be either differential or single–ended if the V_{BB} output is used. The selected signal is fanned out to 20 identical differential outputs.

- 150ps Part–to–Part Skew
- 50ps Output–to–Output Skew
- Differential Design
- V_{BB} Output
- Voltage and Temperature Compensated Outputs
- Low Voltage V_{EE} Range of –2.375 to –3.8V
- 75kΩ Input Pulldown Resistors

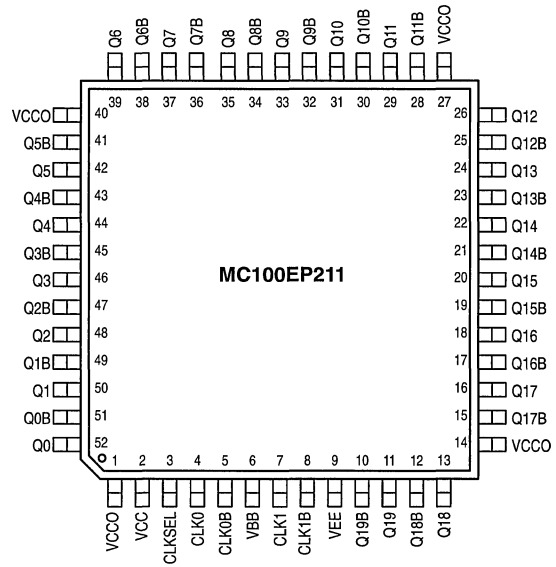
FA SUFFIX
52–LEAD TQFP PACKAGE
CASE 848D–03

The EP221 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate–to–gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100EP221, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the EP221 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP221's performance to distribute low skew clocks across the backplane. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

Pinout: 52–Lead TQFP
(Top View)



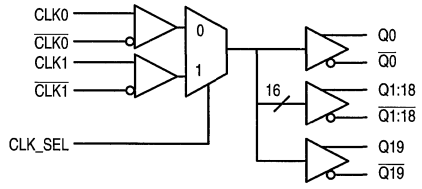
PIN NAMES

Pins	Function
CLKn, $\overline{\text{CLKn}}$	Differential Input Pairs
Q0:19, $\overline{\text{Q0:19}}$	Differential Outputs
CLK_SEL	Active Clock Select Input
VBB	V_{BB} Output

FUNCTION

CLK_SEL	Active Input
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

LOGIC SYMBOL



ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–2.375		–3.8	–2.375		–3.8	–2.375		–3.8	–2.375		–3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current													mA

PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (1.)	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	V
V_{OL}	Output LOW Voltage (1.)	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	V
V_{IH}	Input HIGH Voltage (1.)	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage (1.)	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{BB}	Output Reference Voltage (Note 1.)	1.92		2.04	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{CC}	Power Supply Voltage	2.375		3.8	2.375		3.8	2.375		3.8	2.375		3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{EE}	Power Supply Current													mA

1. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended)								 500 500					ps	
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)		 50 150			 50 150			 50 150			 50 150		ps	
f_{max}	Maximum Input Frequency		1.5			1.5			1.5			1.5		GHz	
V_{PP}	Minimum Input Swing	500			500			500			500			mV	
V_{CMR}	Common Mode Range													V	
t_r/t_f	Output Rise/Fall Time		200			200			200			200		ps	20%–80%

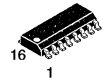
1:6 PCI Clock Generator/ Fanout Buffer

MPC903
MPC904
MPC905

1:6 PCI CLOCK GENERATOR/ FANOUT BUFFER

The MPC903, MPC904 and MPC905 are six output clock generation devices targeted to provide the clocks required in a 3.3V or 5.0V PCI environment. The device operates from a 3.3V supply and can interface to either a TTL input or an external crystal. The inputs to the device can be driven with 5.0V when the V_{CC} is at 3.3V. The outputs of the MPC903/904/905 meet all of the specifications of the PCI standard. The three devices are identical except in the function of the Output Enables.

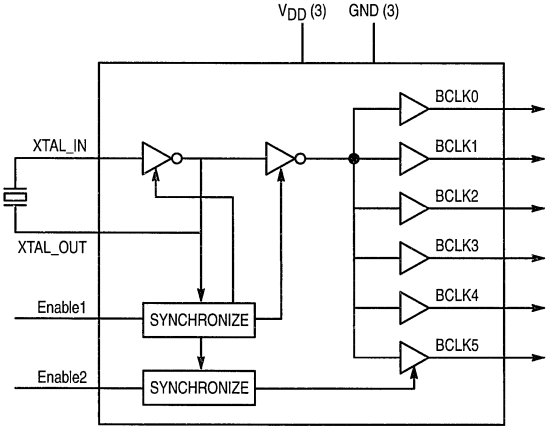
- Six Low Skew Outputs
- Synchronous Output Enables for Power Management
- Low Voltage Operation
- XTAL Oscillator Interface
- 16-Lead SOIC Package
- 5.0V Tolerant Enable Inputs



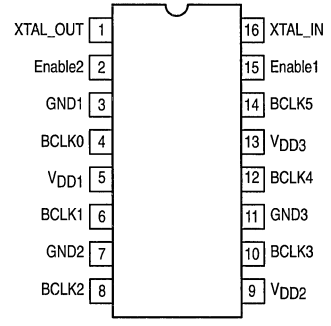
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05

The MPC903/904/905 device is targeted for PCI bus or processor bus environments with up to 12 clock loads. Each of the six outputs on the MPC903/904/905 can drive two series terminated 50Ω transmission lines. This capability effectively makes the MPC903/904/905 a 1:12 fanout buffer.

The MPC903 offers two synchronous enable inputs to allow users flexibility in developing power management features for their designs. Both enable signals are active HIGH inputs. A logic '0' on the Enable1 input will pull all of the outputs into the logic '0' state and shut down the internal oscillator for a zero power sleep state. A logic '0' on the Enable2 input will disable only the BCLK5 output. The Enable2 input can be used to disable any high power device for system power savings during periods of inactivity. Both enable inputs are synchronized internal to the chip so that the output disabling will happen only when the outputs are already LOW. This feature guarantees no runt pulses will be generated during enabling and disabling. Note that when the MPC903 is re-enabled via the Enable1 pin, the user must allow for the oscillator to regain stability. Thus, the re-enabling of the chip cannot occur instantaneously. The MPC904 and MPC905 Enable functions are slightly different than the 903 and are outlined in the function tables on the following page.



Pinout: 16-Lead Plastic Package (Top View)



MOTOROLA

FUNCTION TABLE

		Outputs 0 to 4			Output 5			OSC (On/Off)		
ENABLE1	ENABLE2	MPC903	MPC904	MPC905	MPC903	MPC904	MPC905	MPC903	MPC904	MPC905
0	0	Low	Low	Low	Low	Low	Low	OFF	OFF	ON
0	1	Low	Low	Low	Low	Toggling	Toggling	OFF	ON	ON
1	0	Toggling	Toggling	Toggling	Low	Low	Low	ON	ON	ON
1	1	Toggling	Toggling	Toggling	Toggling	Toggling	Toggling	ON	ON	ON

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	–0.5	4.6	V
V_{IN}	Input Voltage	–0.5	V_{CC} + 0.5	V
T_{oper}	Operating Temperature Range	0	+70	°C
T_{stg}	Storage Temperature Range	–65	+150	°C
T_{sol}	Soldering Temperature Range (10 Sec)		+260	°C
T_j	Junction Temperature Range		+125	°C
P(E1=1)	Power Dissipation		TBD	mW
P(E1=0)	Power Dissipation		40	µW
ESD	Static Discharge Voltage	2000		V
I_{Latch}	Latch Up Current	50		mA

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Temperature Range	0	70	°C
V_{DD}	Positive Supply Voltage (Functional Range)	3.0	3.6	V
t_{DC}in	T_{high} (at XTAL_IN Input) T_{low} (at XTAL_IN Input)	0.44T[1] 0.44T[1]	0.56T[1] 0.56T[1]	T = Period

1. When using External Source for reference, requirement to meet PCI clock duty cycle requirement on the output.

DC CHARACTERISTICS (T_A = 0–70°C; V_{DD} = 3.3V ±0.3V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	High Level Input Voltage		2.0		5.5[2]	V	
V_{IL}	Low Level Input Voltage				0.8	V	
V_{OH}	High Level Output Voltage		2.4			V	I_{OH} = –36mA[1]
V_{OL}	Low Level Output Voltage				0.4	V	I_{OL} = 36mA[1]
I_{IH}	Input High Current				2.5[2]	µA	
I_{IL}	Input Low Current				2.5	µA	
I_{CC}	Power Supply Current	DC 33MHz 66MHz		20 37 78	 45 95	µA mA mA	
C_{IN}	Input Capacitance	XTAL_IN Others			9.0 4.5	pF	

1. The MPC903/904/905 outputs can drive series terminated or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info).
2. XTAL_IN input will sink up to 10mA when driven to 5.5V. There are no reliability concerns associated with the condition. Note that the Enable1 input must be a logic HIGH. Do not take the Enable1 input to a logic LOW with >V_{CC} volts on the XTAL_IN input.

AC CHARACTERISTICS (T_A = 0–70°C; V_{DD} = 3.3V ±0.3V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Operating Frequency	Using External Crystal Using External Clock Source	TBD DC		50 100	MHz	
t_{pw}	Output Pulse Width	HIGH (Above 2.0V) LOW (Below 0.8V) HIGH (Above 2.0V) LOW (Below 0.8V)	0.40T[1] 0.40T[1] 0.45T[2] 0.45T[2]		0.60T[1] 0.60T[1] 0.55T[2] 0.55T[2]		T = Periods
t_{per}	Output Period		T – 400ps				T = Desired Period
t_{os}	Output-to-Output Skew	Rising Edges Falling Edges			400 500	ps	
t_r, t_f	Rise/Fall Times (Slew Rate)		1		4	V/ns	Series Terminated Transmission Lines
t_{EN}	Enable Time	Enable1 Enable2			5 4	ms Cycles	
t_{DIS}	Disable Time	Enable1 Enable2			4 4	Cycles	
A_{osc}	XTAL_IN to XTAL_OUT Oscillator Gain		6			db	
Phase	Loop Phase Shift Modulo 360° +		30			Degrees	

1. Assuming input duty cycle specs from Recommended Operationg Conditions table are met.
2. Assuming external crystal or 50% duty cycle external reference is used.

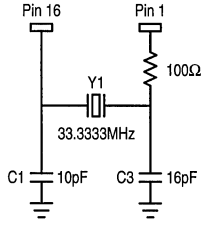


Figure 3. Crystal Oscillator Interface
(Fundamental)

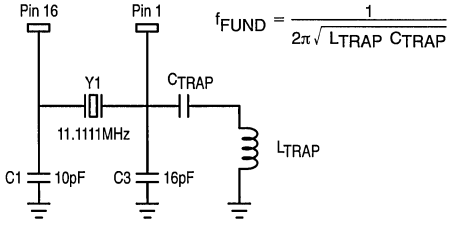


Figure 4. Crystal Oscillator Interface
(3rd Overtone)

Table 1. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Parallel Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100µW
Aging	5ppm/Yr (First 3 Years)

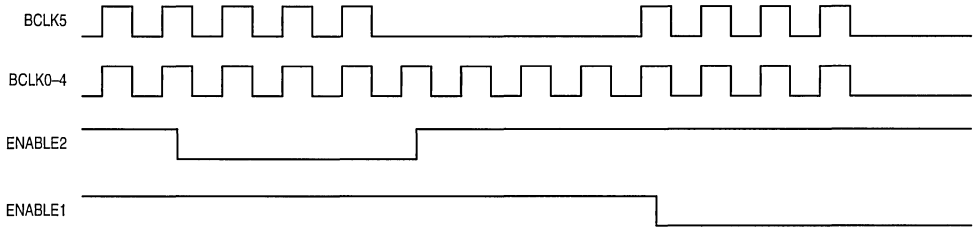


Figure 5. Enable Timing Diagram

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC903/904/905 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC903/904/905 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC903/904/905 clock driver is effectively doubled due to its capability to drive multiple lines.

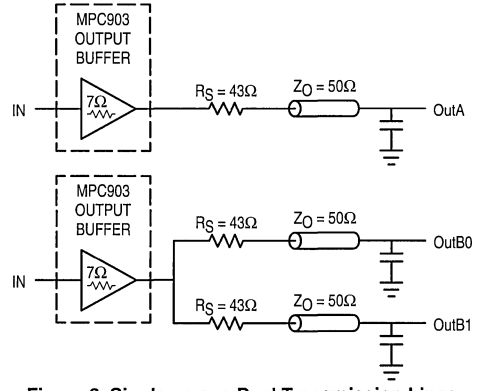


Figure 6. Single versus Dual Transmission Lines

The waveform plots of Figure 7 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC903/904/905 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line

driving need not be used exclusively to maintain the tight output–to–output skew of the MPC903. The output waveform in Figure 7 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

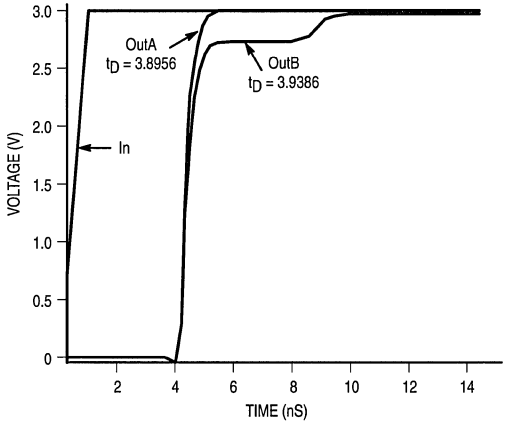
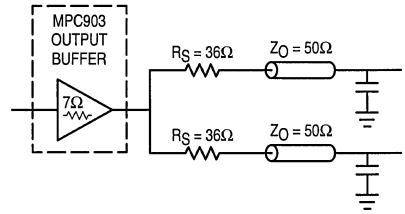


Figure 7. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

Figure 8. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

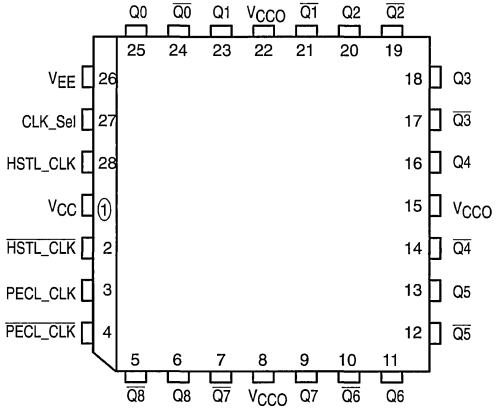
Low-Voltage 1:9 Differential ECL/HSTL to HSTL Clock Driver

The MPC9111 is a low skew 1–to–9 differential HSTL compatible output fanout buffer. The device is functionally equivalent to the MC100LVE111 device. The device accepts either LVPECL or HSTL compatible input levels and provides 9 low skew differential HSTL compatible outputs. The device operates from a single 3.3V V_{CC} supply.

- 800ps Part–to–Part Skew
- 250ps Output–to–Output Skew
- Open Emitter HSTL Compatible Outputs
- Differential Design
- 28–Lead PLCC
- 3.3V V_{CC}

The MPC911 HSTL outputs are not realized in the conventional manner. To minimize part–to–part and output–to–output skew the HSTL compatible output levels are generated with an open emitter architecture. The outputs are pulled down with 50Ω to ground rather than the typical 50Ω to V_{DDQ} pullup of a "standard" HSTL output. Because the HSTL outputs are pulled to ground the MPC911 does not utilize the V_{DDQ} supply of the HSTL standard. The output levels are derived from V_{CC}, an internal regulator minimizes the output level variation with V_{CC} variations.

Pinout: 28-Lead PLCC (Top View)



MPC911

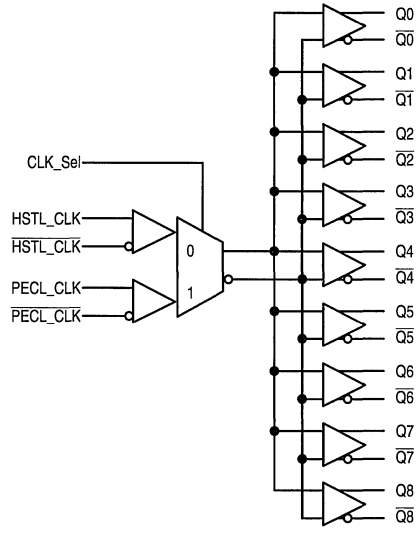
LOW-VOLTAGE 1:9 DIFFERENTIAL ECL/HSTL TO HSTL CLOCK DRIVER

FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

PIN NAMES

Pins	Function
HSTL_CLK, $\overline{\text{HSTL\_CLK}}$	Differential HSTL Input
PECL_CLK, $\overline{\text{PECL\_CLK}}$	Differential PECL Input
Q0–Q8, $\overline{\text{Q0}}$–$\overline{\text{Q8}}$	Differential Outputs

LOGIC SYMBOL



HSTL DC CHARACTERISTICS

Symbol	Characteristic	0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	0.9			0.9			0.9			V
V_{OL}	Output LOW Voltage			0.5			0.5			0.5	V
V_{IH}	Input HIGH Voltage	V_{ref} + 0.10		1.9	V_{ref} + 0.10		1.9	V_{ref} + 0.10		1.9	V
V_{IL}	Input LOW Voltage	–0.3		V_{ref} – 0.10	–0.3		V_{ref} – 0.10	–0.3		V_{ref} – 0.10	V
V_X	Input Crossover Volt	0.68		0.9	0.68		0.9	0.68		0.9	V
V_{ref}	Input Reference Volt	0.68		0.9	0.68	0.75	0.9	0.68		0.9	

LV PECL DC CHARACTERISTICS

Symbol	Characteristic	0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage[1]	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage[1]	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{CC}	Power Supply Voltage	3.0		3.6	3.0		3.6	3.0		3.6	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{CC}	Power Supply Current			100			100			110	mA

1. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

AC CHARACTERISTICS

Symbol	Characteristic	0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output HSTL IN (differential) PECL	1.4 1.3	2.0 1.9	2.3 2.0	1.6 1.4	1.9 1.9	2.4 2.1	1.8 1.5	2.3 2.0	2.6 2.3	ns	Note 1
t_{skew}	Within-Device Skew Part-to-Part Skew (Diff)			250 900			250 800			250 800	ps	Note 2
V_{PP}	Minimum Input Swing PECL_CLK	600			600			600			mV	Note 3
V_{CMR}	Common Mode Range PECL_CLK	V_{CC} –1.5		V_{CC} –0.8	V_{CC} –1.5		V_{CC} –0.8	V_{CC} –1.5		V_{CC} –0.8	V	Note 4
t_r/t_f	Output Rise/Fall Time	500 600	800 1200	1200 1800	500 600	800 1200	1200 1800	500 600	800 1200	1200 1800	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
3. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the MPC911 as a differential input as low as 50 mV will still produce full HSTL levels at the output.
4. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

Product Preview

Low Voltage 1:18 Clock Distribution Chip

MPC940

LOW VOLTAGE 1:18 CLOCK DISTRIBUTION CHIP

The MPC940 is a 1:18 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or an LVTTL/LVCMOS compatible input. The 18 outputs are LVCMOS or LVTTL compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output–to–output skews of 175ps, the MPC940 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product with a larger number of outputs, please consult the MPC941 data sheet.

- LVPECL or LVCMOS/LVTTL Clock Input
- 175ps Maximum Targeted Output–to–Output Skew
- Drives Up to 36 Independent Clock Lines
- Maximum Output Frequency of 250MHz
- High Impedance Output Enable
- 32–Lead TQFP Packaging
- 3.3V or 2.5V V_{CC} Supply Voltage

FA SUFFIX
32–LEAD TQFP PACKAGE
CASE 873A–02

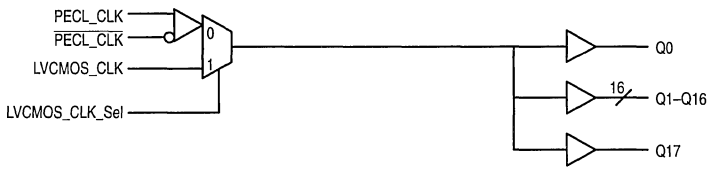
With a low output impedance, in both the HIGH and LOW logic states, the output buffers of the MPC940 are ideal for driving series terminated transmission lines. More specifically, each of the 18 MPC940 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC940 has an effective fanout of 1:36 in applications where each line drives a single load. With this level of fanout, the MPC940 provides enough copies of low skew clocks for most high performance synchronous systems.

The differential LVPECL inputs of the MPC940 allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS/LVTTL input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the TTL level clock input.

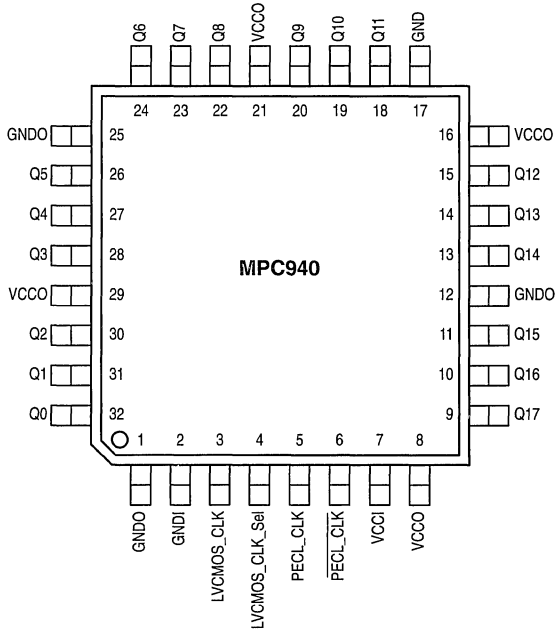
The MPC940 is fully 3.3V and 2.5V compatible. The 32–lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

LOGIC DIAGRAM



Pinout: 32–Lead TQFP (Top View)



FUNCTION TABLE

LVCMOS_CLK_Sel	Input
0	PECL_CLK
1	LVCMOS_CLK

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%, or 2.5V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	PECL_CLK Other				V	
V_{IL}	Input LOW Voltage	PECL_CLK Other				V	
V_{PP}	Peak–to–Peak Input Voltage	PECL_CLK				mV	
V_{CMR}	Common Mode Range	PECL_CLK				V	
V_{OH}	Output HIGH Voltage					V	Note 1.
V_{OL}	Output LOW Voltage					V	Note 1.
I_{IN}	Input Current					µA	
C_{IN}	Input Capacitance					pF	
C_{pd}	Power Dissipation Capacitance					pF	
I_{CC}	Maximum Quiescent Supply Current					mA	

1. The MPC940 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%, or 2.5V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency			250		MHz	Note 1.
t_{pd}	Propagation Delay	PECL_CLK to Q TTL_CLK to Q		3.0 3.0		ns	Note 1.
$t_{sk(o)}$	Output–to–Output Skew				175	ps	Note 1.
$t_{sk(pr)}$	Part–to–Part Skew	PECL_CLK to Q TTL_CLK to Q		550 550		ps	Note 2.
t_{pwo}	Output Pulse Width			$t_{CYCLE}/2$ ±500		ps	Note 1., Measured at $V_{CC}/2$
t_r, t_f	Output Rise/Fall Time		0.20		1.0	ns	0.8V to 2.0V

1. Driving 50Ω transmission lines
2. Part–to–part skew at a given temperature and voltage

Product Preview

Low Voltage 1:27 Clock Distribution Chip

MPC941

LOW VOLTAGE 1:27 CLOCK DISTRIBUTION CHIP

The MPC941 is a 1:27 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or an LVTTL/LVCMOS compatible input. The 27 outputs are LVCMOS or LVTTL compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output–to–output skews of 250ps, the MPC941 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product with a smaller number of outputs, please consult the MPC940 data sheet.

- LVPECL or LVCMOS/LVTTL Clock Input
- 250ps Maximum Targeted Output–to–Output Skew
- Drives Up to 54 Independent Clock Lines
- Maximum Output Frequency of 250MHz
- High Impedance Output Enable
- 52–Lead TQFP Packaging
- 3.3V V_{CC} Supply Voltage

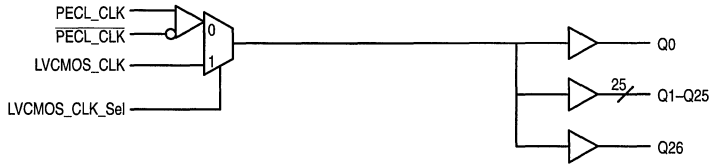
FA SUFFIX
52–LEAD TQFP PACKAGE
CASE 848D–03

With a low output impedance, in both the HIGH and LOW logic states, the output buffers of the MPC941 are ideal for driving series terminated transmission lines. More specifically, each of the 27 MPC941 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC941 has an effective fanout of 1:54 in applications where each line drives a single load. With this level of fanout, the MPC941 provides enough copies of low skew clocks for most high performance synchronous systems.

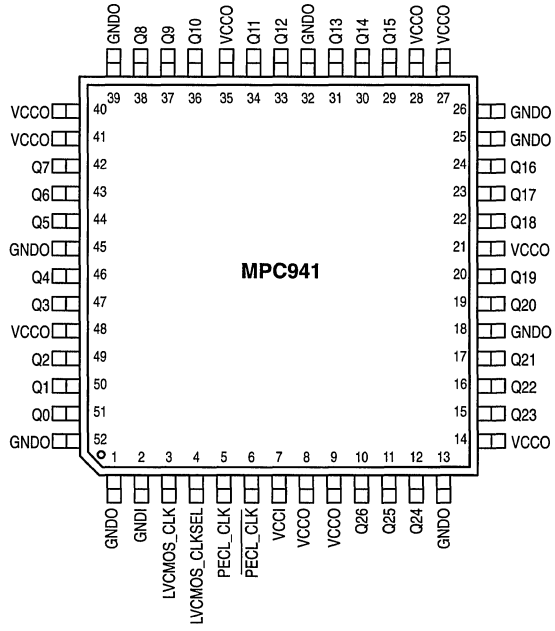
The differential LVPECL inputs of the MPC941 allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS/LVTTL input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the TTL level clock input.

The MPC941 is fully 3.3V compatible. The 52–lead TQFP package was chosen to optimize performance, board space and cost of the device. The 52–lead TQFP has a 10x10mm body size with a conservative 0.65mm pin spacing.

LOGIC DIAGRAM



Pinout: 52–Lead TQFP (Top View)



FUNCTION TABLE

LVCMOS_CLK_Sel	Input
0	PECL_CLK
1	LVCMOS_CLK

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	PECL_CLK Other				V	
V_{IL}	Input LOW Voltage	PECL_CLK Other				V	
V_{PP}	Peak–to–Peak Input Voltage	PECL_CLK				mV	
V_{CMR}	Common Mode Range	PECL_CLK				V	
V_{OH}	Output HIGH Voltage					V	Note 1.
V_{OL}	Output LOW Voltage					V	Note 1.
I_{IN}	Input Current					µA	
C_{IN}	Input Capacitance					pF	
C_{pd}	Power Dissipation Capacitance					pF	
I_{CC}	Maximum Quiescent Supply Current					mA	

1. The MPC941 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency			250		MHz	Note 1.
t_{pd}	Propagation Delay	PECL_CLK to Q TTL_CLK to Q		3.0 3.0		ns	Note 1.
$t_{sk(o)}$	Output–to–Output Skew			250		ps	Note 1.
$t_{sk(pr)}$	Part–to–Part Skew	PECL_CLK to Q TTL_CLK to Q		650 650		ps	Note 2.
t_{pwo}	Output Pulse Width			$t_{CYCLE}/2$ ±500		ps	Note 1., Measured at $V_{CC}/2$
t_r, t_f	Output Rise/Fall Time		0.20		1.0	ns	0.8V to 2.0V

2. Driving 50Ω transmission lines.
3. Part–to–part skew at a given temperature and voltage.

Low Voltage 1:10 CMOS Clock Driver

MPC946

LOW VOLTAGE 1:10 CMOS CLOCK DRIVER

FA SUFFIX
TQFP PACKAGE
CASE 873A–02

The MPC946 is a low voltage CMOS, 10 output clock buffer. The 10 outputs can be configured into a standard fanout buffer or into 1X and 1/2X combinations. The ten outputs were designed and optimized to drive 50Ω series or parallel terminated transmission lines. With output to output skews of 350ps the MPC946 is an ideal clock distribution chip for synchronous systems which need a tight level of skew from a large number of outputs. For a similar product with more outputs consult the MPC949 data sheet.

- Clock Distribution for Pentium™ Systems with PCI
- 2 Selectable LVCMOS/LVTTL Clock Inputs
- 350ps Output to Output Skew
- Drives up to 20 Independent Clock Lines
- Maximum Input/Output Frequency of 150MHz
- Tristatable Outputs
- 32–Lead TQFP Packaging
- 3.3V VCC Supply

With an output impedance of approximately 7Ω, in both the HIGH and the LOW logic states, the output buffers of the MPC946 are ideal for driving series terminated transmission lines. More specifically each of the 10 MPC946 outputs can drive two series terminated transmission lines. With this capability, the MPC946 has an effective fanout of 1:20 in applications using point–to–point distribution schemes.

The MPC946 has the capability of generating 1X and 1/2X signals from a 1X source. The design is fully static, the signals are generated and retimed inside the chip to ensure minimal skew between the 1X and 1/2X signals. The device features selectability to allow the user to select the ratio of 1X outputs to 1/2X outputs.

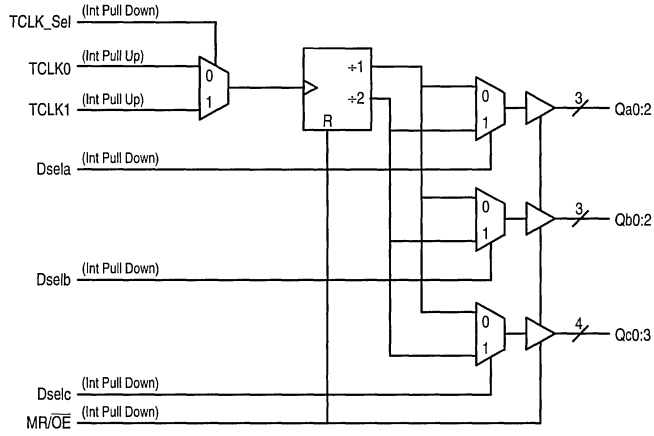
Two independent LVCMOS/LVTTL compatible clock inputs are available. Designers can take advantage of this feature to provide redundant clock sources or the addition of a test clock into the system design. With the TCLK_Sel input pulled HIGH the TCLK1 input is selected.

All of the control inputs are LVCMOS/LVTTL compatible. The Dsel pins choose between 1X and 1/2X outputs. A LOW on the Dsel pins will select the 1X output. The MR/Tristate input will reset the internal flip flops and tristate the outputs when it is forced HIGH.

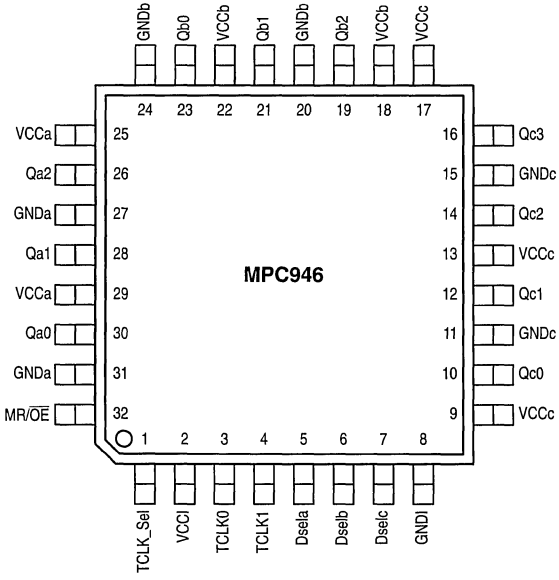
The MPC946 is fully 3.3V compatible. The 32–lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

Pentium is a trademark of Intel Corporation.

LOGIC DIAGRAM



Pinout: 32–Lead TQFP (Top View)



FUNCTION TABLES

TCLK_Sel	Input
0	TCLK0
1	TCLK1
Dselx	**Outputs**
0	1x
1	1/2x
MR/$\overline{OE}$	**Outputs**
0	Enabled
1	Hi–Z

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current (CMOS Inputs)		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.5			V	I_{OH} = –20mA[1]
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 20mA[1]
I_{IN}	Input Current			±120	µA	Note 2.
I_{CC}	Maximum Quiescent Supply Current		70	85	mA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output

1. The MPC946 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
2. I_{IN} current is a result of internal pull–up/pull–down resistors.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency	150			MHz	Note 1.
t_{PLH}, t_{PHL}	Propagation Delay TCLK to Q	5.0 4.5	8.0 7.5	12.0 11.5	ns	Note 1., 3.
$t_{sk(o)}$	Output–to–Output Skew Same Frequency Outputs Different Frequency Outputs Same Frequency Outputs Different Frequency Outputs			 350 350 350 450	ps	Note 1., 3. F_{max} < 100MHz F_{max} < 100MHz F_{max} > 100MHz F_{max} > 100MHz
$t_{sk(pr)}$	Part–to–Part Skew		2.0	4.5	ns	Note 2.
t_{PZL}, t_{PZH}	Output Enable Time		3	11	ns	Note 3.
t_{PLZ}, t_{PHZ}	Output Disable Time		3	11	ns	Note 3.
t_r, t_f	Output Rise/Fall Time	0.1	0.5	1.0	ns	0.8V to 2.0V, Note 3.

1. Driving 50Ω transmission lines.
2. Part–to–part skew at a given temperature and voltage.
3. Termination is 50Ω to V_{CC}/2.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC946 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC946 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 1 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC946 clock driver is effectively doubled due to its capability to drive multiple lines.

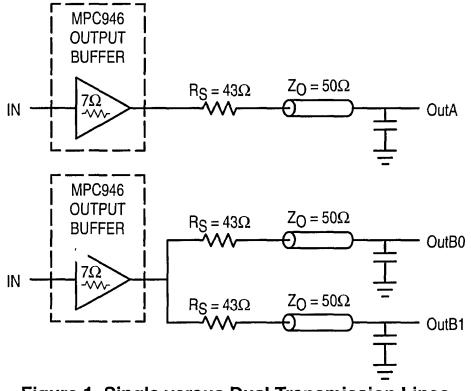


Figure 1. Single versus Dual Transmission Lines

The waveform plots of Figure 2 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC946 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC946. The output waveform in Figure 2 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

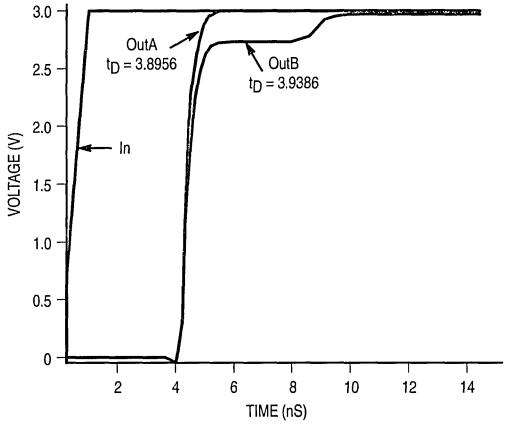
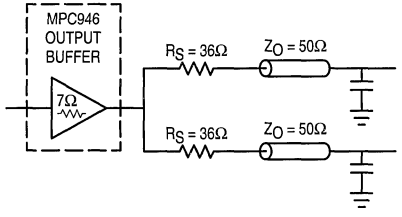


Figure 2. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 3 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

Figure 3. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Low Voltage 1:9 Clock Distribution Chip

MPC947

LOW VOLTAGE 1:9 CLOCK DISTRIBUTION CHIP

FA SUFFIX
32–LEAD TQFP PACKAGE
CASE 873A–02

The MPC947 is a 1:9 low voltage clock distribution chip. The device features the capability to select between two LVTTL compatible inputs and fans the signal out to 9 LVCMOS or LVTTL compatible outputs. These 9 outputs were designed and optimized to drive 50Ω series terminated transmission lines. With output–to–output skews of 500ps, the MPC947 is ideal as a clock distribution chip for synchronous systems which need a tight level of skew at a relatively low cost. For a similar product targeted at a higher price/performance point, consult the MPC948 data sheet.

- Clock Distribution for PowerPC™ 620 L2 Cache
- 2 Selectable LVCMOS/LVTTL Clock Inputs
- 500ps Maximum Output–to–Output Skew
- Drives Up to 18 Independent Clock Lines
- Maximum Output Frequency of 110MHz
- Synchronous Output Enable
- Tristatable Outputs
- 32–Lead TQFP Packaging
- 3.3V V_{CC} Supply Voltage

With an output impedance of approximately 7Ω, in both the HIGH and LOW logic states, the output buffers of the MPC947 are ideal for driving series terminated transmission lines. More specifically, each of the 9 MPC947 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC947 has an effective fanout of 1:18 in applications using point–to–point distribution schemes. With this level of fanout, the MPC947 provides enough copies of low skew clocks for high performance synchronous systems, including use as a clock distribution chip for the L2 cache of a PowerPC 620 based system.

Two independent LVCMOS/LVTTL compatible clock inputs are available. Designers can take advantage of this feature to provide redundant clock sources or the addition of a test clock into the system design. With the select input pulled HIGH, the TTL_CLK1 input will be selected.

All of the control inputs are LVCMOS/LVTTL compatible. The MPC947 provides a synchronous output enable control to allow for starting and stopping of the output clocks. A logic high on the Sync_OE pin will enable all of the outputs. Because this control is synchronized to the input clock, potential output glitching or runt pulse generation is eliminated. In addition, for board level test, the outputs can be tristated via the tristate control pin. A logic LOW applied to the $\overline{\text{Tristate}}$ input will force all of the outputs into high impedance. Note that all of the MPC947 inputs have internal pullup resistors.

The MPC947 is fully 3.3V compatible. The 32–lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

PowerPC is a trademark of International Business Machines Corporation.

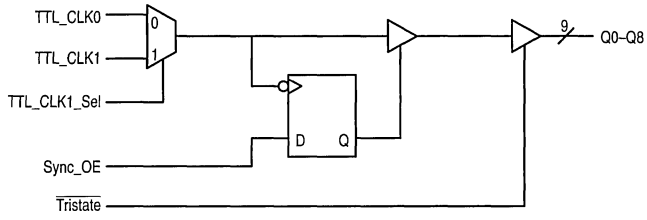


Figure 1. Logic Diagram

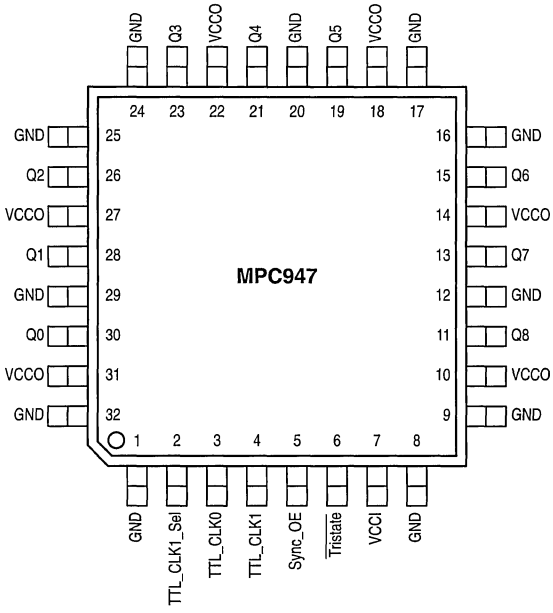


Figure 2. 32–Lead Pinout (Top View)

FUNCTION TABLES

TTL_CLK1_Sel	Input
0	TTL_CLK0
1	TTL_CLK1

Sync_OE	Outputs
0	Disabled
1	Enabled

$\overline{\text{Tristate}}$	Outputs
0	Tristate
1	Enabled

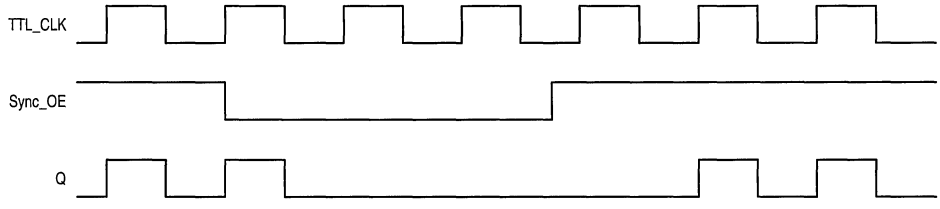


Figure 3. Sync_OE Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current (CMOS Inputs)		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.5			V	I_{OH} = –20mA (Note 1.)
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 20mA (Note 1.)
I_{IN}	Input Current			–100	µA	Note 2.
I_{CC}	Maximum Quiescent Supply Current		21	28	mA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output

1. The MPC947 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).
2. I_{IN} current is a result of internal pull–up resistors.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency	110			MHz	Note 3.
t_{pd}	Propagation Delay TCLK to Q	4.75		9.25	ns	Note 3.
$t_{sk(o)}$	Output–to–Output Skew			500	ps	Note 3.
$t_{sk(pr)}$	Part–to–Part Skew			2.0	ns	Notes 3., 4.
t_{pwo}	Output Pulse Width	$t_{CYCLE}/2$ – 800		$t_{CYCLE}/2$ + 800	ps	Note 3., Measured at $V_{CC}/2$
t_s	Setup Time Sync_OE to Input Clk	0.0			ns	Notes 3., 5.
t_h	Hold Time Input Clk to Sync_OE	1.0			ns	Notes 3., 5.
t_{PZL}, t_{PZH}	Output Enable Time			11	ns	
t_{PLZ}, t_{PHZ}	Output Disable Time			11	ns	
t_r, t_f	Output Rise/Fall Time	0.2		1.0	ns	0.8V to 2.0V

3. Driving 50Ω terminated to $V_{CC}/2$.
4. Part–to–part skew at a given temperature and voltage.
5. Setup and Hold times are relative to the falling edge of the input clock.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC947 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC947 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC947 clock driver is effectively doubled due to its capability to drive multiple lines.

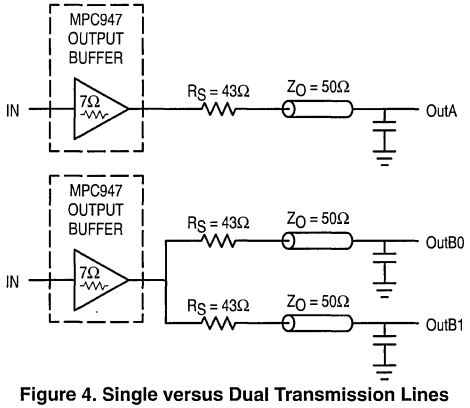


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC947 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC947. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

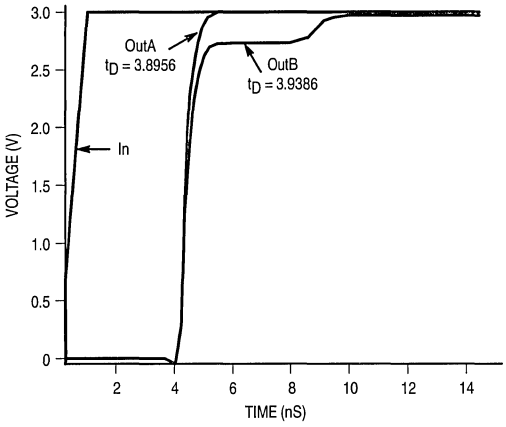
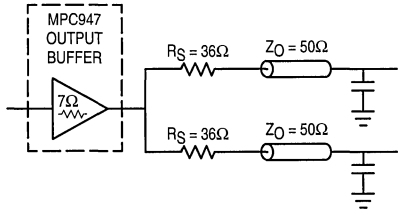


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Low Voltage 1:12 Clock Distribution Chip

MPC948

LOW VOLTAGE 1:12 CLOCK DISTRIBUTION CHIP

The MPC948 is a 1:12 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or a LVTTL compatible input. The 12 outputs are LVCMOS or LVTTL compatible and feature the drive strength to drive 50Ω series terminated transmission lines. With output–to–output skews of 350ps, the MPC948 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product targeted at a lower price/performance point, please consult the MPC947 data sheet.

- Clock Distribution for PowerPC™ 620 L2 Cache
- LVPECL or LVCMOS/LVTTL Clock Input
- 350ps Maximum Output–to–Output Skew
- Drives Up to 24 Independent Clock Lines
- Maximum Output Frequency of 150MHz
- Synchronous Output Enable
- Tristatable Outputs
- 32–Lead TQFP Packaging
- 3.3V V_{CC} Supply Voltage

FA SUFFIX
32–LEAD TQFP PACKAGE
CASE 873A–02

With an output impedance of approximately 7Ω, in both the HIGH and LOW logic states, the output buffers of the MPC948 are ideal for driving series terminated transmission lines. More specifically, each of the 12 MPC948 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC948 has an effective fanout of 1:24 in applications where each line drives a single load. With this level of fanout, the MPC948 provides enough copies of low skew clocks for high performance synchronous systems, including use as a clock distribution chip for the L2 cache of a PowerPC 620 based system.

The differential LVPECL inputs of the MPC948 allow the device to interface directly with a LVPECL fanout buffer like the MC100LVE111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS/LVTTL input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the TTL_CLK_Sel pin will select the TTL level clock input.

All of the control inputs are LVCMOS/LVTTL compatible. The MPC948 provides a synchronous output enable control to allow for starting and stopping of the output clocks. A logic high on the Sync_OE pin will enable all of the outputs. Because this control is synchronized to the input clock, potential output glitching or runt pulse generation is eliminated. In addition, for board level test, the outputs can be tristated via the tristate control pin. A logic LOW applied to the $\overline{\text{Tristate}}$ input will force all of the outputs into high impedance. Note that all of the MPC948 inputs have internal pullup resistors.

The MPC948 is fully 3.3V compatible. The 32–lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

PowerPC is a trademark of International Business Machines Corporation.

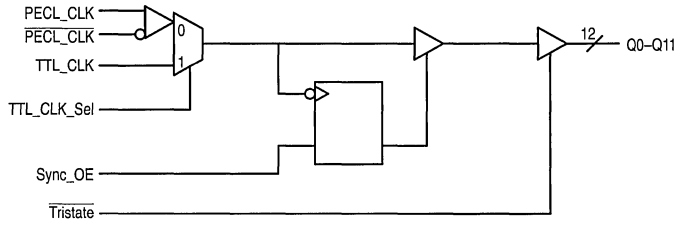


Figure 1. Logic Diagram

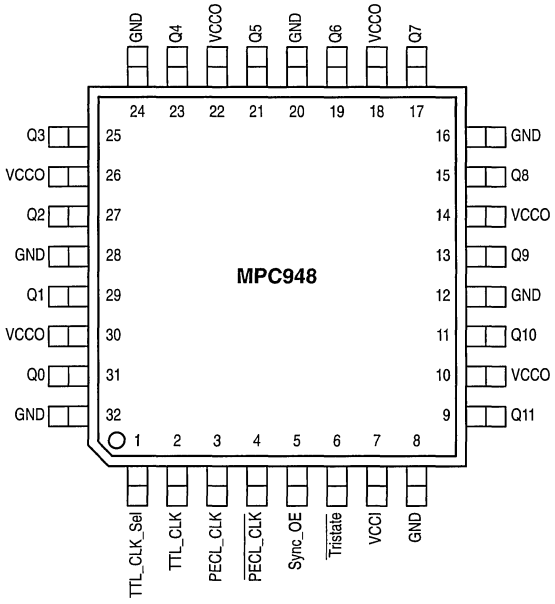


Figure 2. 32–Lead Pinout (Top View)

FUNCTION TABLES

TTL_CLK_Sel	Input
0	PECL_CLK
1	TTL_CLK

Sync_OE	Outputs
0	Disabled
1	Enabled

$\overline{\text{Tristate}}$	Outputs
0	Tristate
1	Enabled

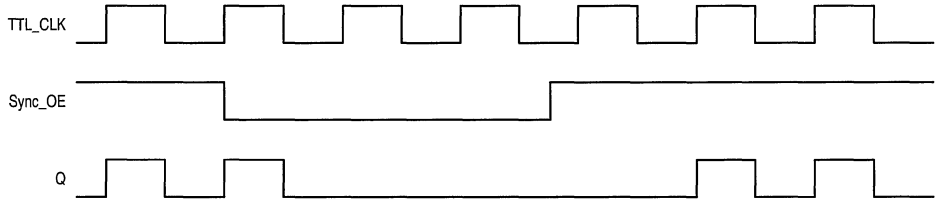


Figure 3. Sync_OE Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	PECL_CLK Other	2.135 2.0		2.42 3.60	V	Single Ended Spec
V_{IL}	Input LOW Voltage	PECL_CLK Other	1.49		1.825 0.8	V	Single Ended Spec
V_{PP}	Peak–to–Peak Input Voltage	PECL_CLK	300		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC} – 2.0		V_{CC} – 0.6	V	Note NO TAG
V_{OH}	Output HIGH Voltage		2.5			V	I_{OH} = –20mA (Note NO TAG)
V_{OL}	Output LOW Voltage				0.4	V	I_{OL} = 20mA (Note NO TAG)
I_{IN}	Input Current				±100	µA	Note NO TAG
C_{IN}	Input Capacitance				4	pF	
C_{pd}	Power Dissipation Capacitance			25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current			22	30	mA	

1. V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
2. The MPC948 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull–up resistors which affect input current, $\overline{\text{PECL\_CLK}}$ has a pull–down resistor.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency		150			MHz	Note NO TAG
t_{pd}	Propagation Delay	PECL_CLK to Q TTL_CLK to Q	4.0 4.4		8.0 8.9	ns	Note NO TAG
$t_{sk(o)}$	Output–to–Output Skew				350	ps	Note NO TAG
$t_{sk(pr)}$	Part–to–Part Skew	PECL_CLK to Q TTL_CLK to Q			1.5 2.0	ns	Notes NO TAG, NO TAG
t_{pwo}	Output Pulse Width		$t_{CYCLE}/2$– 800		$t_{CYCLE}/2$+ 800	ps	Notes NO TAG, NO TAG Measured at $V_{CC}/2$
t_s	Setup Time	Sync_OE to PECL_CLK Sync_OE to TTL_CLK	1.0 0.0			ns	Notes NO TAG, NO TAG
t_h	Hold Time	PECL_CLK to Sync_OE TTL_CLK to Sync_OE	0.0 1.0			ns	Notes NO TAG, NO TAG
t_{PZL},t_{PZH}	Output Enable Time		3		11	ns	
t_{PLZ},t_{PHZ}	Output Disable Time		3		11	ns	
t_r, t_f	Output Rise/Fall Time		0.20		1.0	ns	0.8V to 2.0V

4. Driving 50Ω transmission lines
5. Part–to–part skew at a given temperature and voltage
6. Assumes 50% input duty cycle.
7. Setup and Hold times are relative to the falling edge of the input clock

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC948 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC948 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. NO TAG illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC948 clock driver is effectively doubled due to its capability to drive multiple lines.

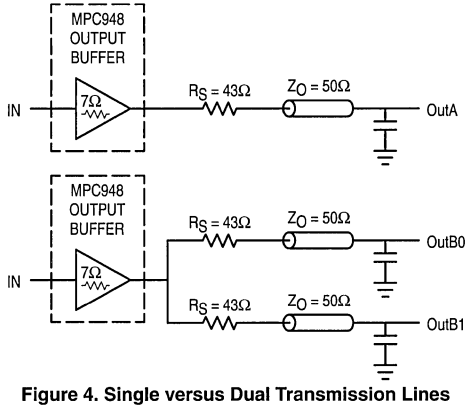


Figure 4. Single versus Dual Transmission Lines

The waveform plots of NO TAG show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC948 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC948. The output waveform in NO TAG shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

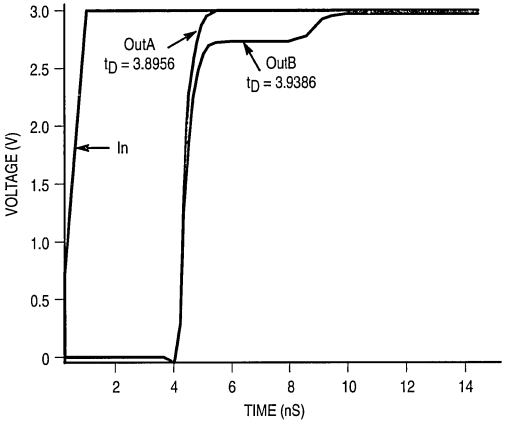
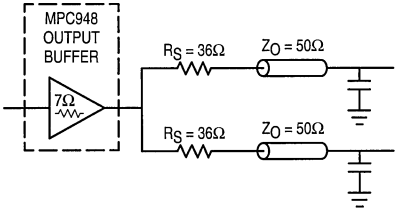


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in NO TAG should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Low Voltage 1:15 PECL to CMOS Clock Driver

MPC949

LOW VOLTAGE 1:15 PECL TO CMOS CLOCK DRIVER

FA SUFFIX
52–LEAD TQFP PACKAGE
CASE 848D–03

The MPC949 is a low voltage CMOS, 15 output clock buffer. The 15 outputs can be configured into a standard fanout buffer or into 1X and 1/2X combinations. The device features a low voltage PECL input, in addition to its LVCMOS/LVTTL inputs, to allow it to be incorporated into larger clock trees which utilize low skew PECL devices (see the MC100LVE111 data sheet) in the lower branches of the tree. The fifteen outputs were designed and optimized to drive 50Ω series or parallel terminated transmission lines. With output to output skews of 300ps the MPC949 is an ideal clock distribution chip for synchronous systems which need a tight level of skew from a large number of outputs. For a similar product with a smaller fanout and package consult the MPC946 data sheet.

- Clock Distribution for Pentium™ Systems with PCI
- Low Voltage PECL Clock Input
- 2 Selectable LVCMOS/LVTTL Clock Inputs
- 350ps Maximum Output to Output Skew
- Drives up to 30 Independent Clock Lines
- Maximum Output Frequency of 150MHz
- High Impedance Output Enable
- 52–Lead TQFP Packaging
- 3.3V V_{CC} Supply

With an output impedance of approximately 7Ω, in both the HIGH and the LOW logic states, the output buffers of the MPC949 are ideal for driving series terminated transmission lines. More specifically each of the 15 MPC949 outputs can drive two series terminated transmission lines. With this capability, the MPC949 has an effective fanout of 1:30 in applications using point–to–point distribution schemes.

The MPC949 has the capability of generating 1X and 1/2X signals from a 1X source. The design is fully static, the signals are generated and retimed inside the chip to ensure minimal skew between the 1X and 1/2X signals. The device features selectability to allow the user to select the ratio of 1X outputs to 1/2X outputs.

Two independent LVCMOS/LVTTL compatible clock inputs are available. Designers can take advantage of this feature to provide redundant clock sources or the addition of a test clock into the system design. With the TCLK_Sel input pulled HIGH the TCLK1 input is selected. The PCLK_Sel input will select the PECL input clock when driven HIGH.

All of the control inputs are LVCMOS/LVTTL compatible. The Dsel pins choose between 1X and 1/2X outputs. A LOW on the Dsel pins will select the 1X output. The MR/$\overline{OE}$ input will reset the internal flip flops and tristate the outputs when it is forced HIGH.

The MPC949 is fully 3.3V compatible. The 52 lead TQFP package was chosen to optimize performance, board space and cost of the device. The 52–lead TQFP has a 10x10mm body size with a 0.65mm pin spacing.

Pentium is a trademark of Intel Corporation.

Figure 1. Logic Diagram

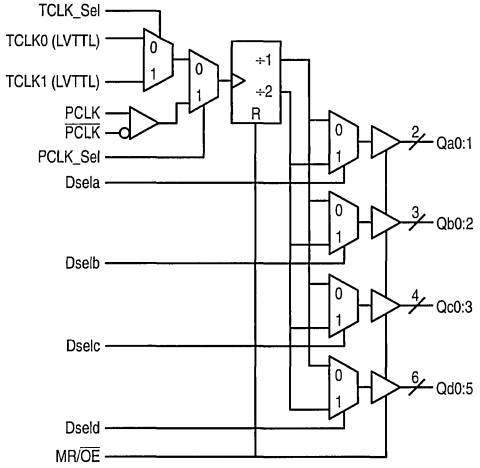
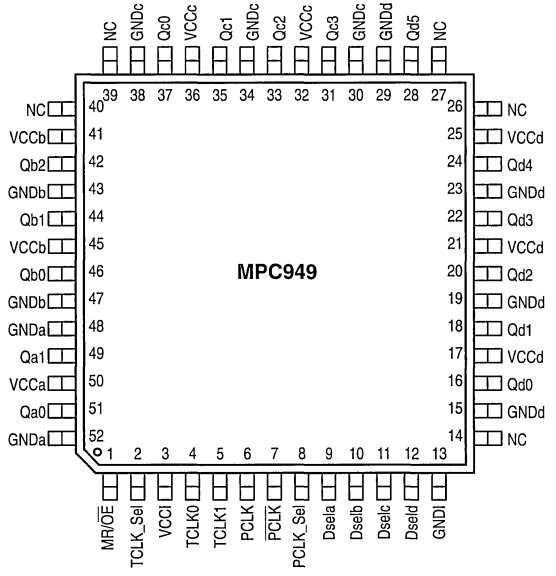


Figure 2. 52–Lead Pinout (Top View)



FUNCTION TABLE

Input	0	1
TCLK_Sel	TCLK0	TCLK1
PCLK_Sel	TCLKn	PCLK
Dseln	÷1	÷2
MR/$\overline{OE}$	Enabled	Hi–Z

PIN DESCRIPTION

Pin Name	Function
TCLK_Sel (Int Pulldown)	Select pin to choose TCKL0 or TCLK1
TCLK0:1 (Int Pullup)	LVCMOS/LVTTL clock inputs
PCLK (Int Pulldown)	True PECL clock input
$\overline{PCLK}$ (Int Pullup)	Compliment PECL clock input
Dseln (Int Pulldown)	1x or 1/2x input divide select pins
MR/$\overline{OE}$ (Int Pulldown)	Internal reset and output tristate control pin
PCLK_Sel (Int Pulldown)	Select Pin to choose TCLK or PCLK

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current	TBD	TBD	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	(Except PECL_CLK)	2.0		3.60	V	
V_{IL}	Input LOW Voltage	(Except PECL_CLK)			0.8	V	
V_{PP}	Peak–to–Peak Input Voltage	PECL_CLK	300		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC} – 2.0		V_{CC} – 0.6	V	Note 1.
V_{OH}	Output HIGH Voltage		2.5			V	I_{OH} = –20mA (Note 2.)
V_{OL}	Output LOW Voltage				0.4	V	I_{OL} = 20mA (Note 2.)
I_{IN}	Input Current				±120	µA	Note 3.
C_{IN}	Input Capacitance				4	pF	
C_{pd}	Power Dissipation Capacitance			25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current			70	85	mA	

1. V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
2. The MPC949 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull–up/pull–down resistors which affect input current.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency		150			MHz	Note 4.
t_{PLH}	Propagation Delay	PECL_CLK to Q TTL_CLK to Q	4.0 4.2	6.5 7.5	9.0 10.6	ns	Note 4.
t_{PHL}	Propagation Delay	PECL_CLK to Q TTL_CLK to Q	3.8 4.0	6.2 7.2	8.6 10.5	ns	Note 4.
$t_{sk(o)}$	Output–to–Output Skew			300	350	ps	Note 4.
$t_{sk(pr)}$	Part–to–Part Skew	PECL_CLK to Q TTL_CLK to Q		1.5 2.0	2.75 4.0	ns	Note 5.
t_{PZL},t_{PZH}	Output Enable Time			3	11	ns	Note 4.
t_{PLZ},t_{PHZ}	Output Disable Time			3	11	ns	Note 4.
t_r, t_f	Output Rise/Fall Time		0.10		1.0	ns	0.8V to 2.0V

4. Driving 50Ω transmission lines terminated to $V_{CC}/2$.
5. Part–to–part skew at a given temperature and voltage.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC949 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC949 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC949 clock driver is effectively doubled due to its capability to drive multiple lines.

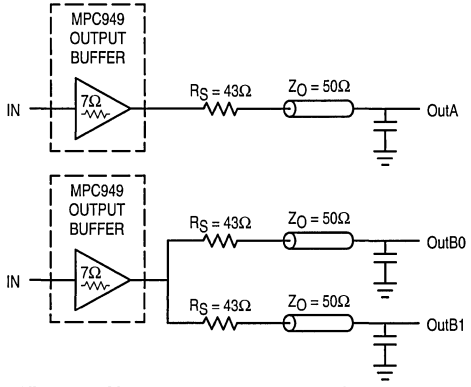


Figure 3. Single versus Dual Transmission Lines

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC949 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC949. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

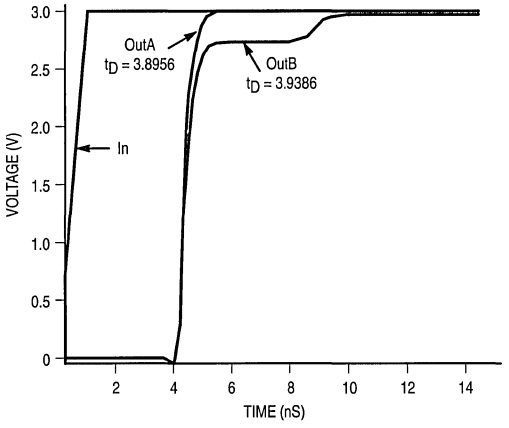
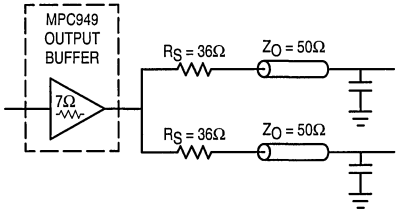


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

Figure 5. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

PC Clock Generators

Advance Information

Multiple Output Clock Synthesizer

MPC9108

MULTIPLE OUTPUT CLOCK SYNTHESIZER

The MPC9108 is a multiple CMOS output clock synthesizer targeted for disk drive applications. The device interfaces to a 20MHz crystal as its frequency source. From this source the device provides a buffered copy of the 20MHz clock as well as synthesized 40MHz and 50MHz output clocks.

- Fully Integrated PLL
- Fully Integrated Crystal Oscillator
- Low cost, low jitter design
- Low cost 8–lead SOIC packaging

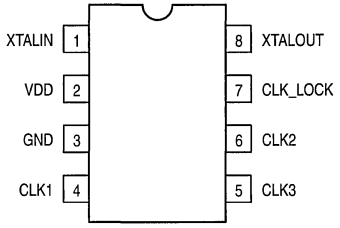
In addition to the output clock frequencies, the MPC9108 also offers a lock indicator output. When the internal PLL achieves phase and frequency lock the CLK_LOCK signal will go HIGH. The pin will remain HIGH unless the PLL loses lock due to input clock or power supply disturbances.

The XTALIN pin (pin 1) can be over–driven with a standard 5V CMOS signal. When an externally generated reference is used the XTALOUT pin should be left open.

The MPC9108 operates from a 5.0V supply across the commercial temperature range of 0°C to 70°C. The 8–lead SOIC package is used to optimize board space efficiency as well as minimizing cost.

D SUFFIX
PLASTIC SOIC
CASE 751–03

Pinout: 8–Lead SOIC
(Top View)

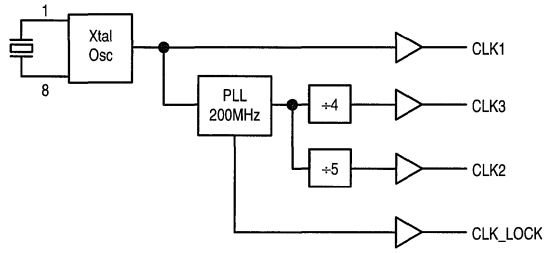


Pin Descriptions

Pin Name	Pin Number	I/O	Function
XTALIN	1	I	20MHz Crystal Connection, External Reference Point
VDD	2	–	+5V Power Supply
GND	3	–	Ground
CLK1	4	O	20MHz Output, Buffer Xtal Output
CLK2	5	O	50MHz Output, PLL Controlled
CLK3	6	O	40MHz Output, PLL Controlled
CLK_LOCK	7	O	HIGH When PLL is Locked
XTALOUT	8	O	Crystal Oscillator Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{IN}	Input Voltage	–0.5 to +7.0	V
T_A	Operating Temperature Range (In Free-Air)	0 to +70	°C
T_A	Ambient Temperature Range (Under Bias)	–55 to +125	°C
T_{STG}	Storage Temperature Range	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

DC CHARACTERISTICS ($0°C < T_A < 70°C$; $V_{DD} = 5V \pm 10\%$; Unless Otherwise Stated)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IL}	Input Low Voltage			0.8	V	$V_{DD} = 5V$
V_{IH}	Input High Voltage	2.0			V	$V_{DD} = 5V$
I_{IL}	Input Low Current			–5	µA	$V_{IN} = 0.5V$
I_{IH}	Input High Current			5	µA	$V_{IN} = V_{DD}$
V_{OL}	Output Low Voltage CLKn			0.4	V	$I_{OL} = 4mA$
V_{OL}	Output Low Voltage CLK_LOCK			0.4	V	$I_{OL} = 10mA$
V_{OH}	Output High Voltage	$0.8V_{DD}$			V	$I_{OH} = –30mA$
I_{DD}	Supply Current		25	40	mA	No Load; Note 1.
F_D	Output Frequency Change Over Supply & Temp		0.002	0.01	%	With Respect to Typ Freq
I_{SC}	Short Circuit Current	25	40		mA	Each Output Clock
C_I	Input Capacitance			10	pF	Except X1, X2
C_L	Xtal Load Capacitance		20		pF	Pins X1, X2

1. All clocks operating at highest frequencies.

AC CHARACTERISTICS ($0°C < T_A < 70°C$; $V_{DD} = 5V \pm 10\%$; Unless Otherwise Stated)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
t_{ICr}	Input Clock Rise Time				20	ns	
t_{ICf}	Input Clock Fall Time				20	ns	
t_r	Output Rise Time	0.8 to 2.0V		1.0	2.0	ns	30pf Load
t_r	Rise Time	20% to 80% V_{DD}		2.0	4.0	ns	30pf Load
t_f	Output Fall Time	2.0 to 0.8V		1.0	2.0	ns	30pf Load
t_f	Fall Time	20% to 80% V_{DD}		2.0	4.0	ns	30pf Load
d_t	Duty Cycle	Pins 4, 6, 5	45/55	48/52	55/45	%	30pf Load
f_i	Input Frequency			20		MHz	
t_{jab}	Jitter Absolute	Pins 4, 6, 5	–500		500	ps	
t_{lock}	Output Lock Time		0.02	3.0	4.0	ms	

PLL Clock Drivers

Low Skew CMOS PLL Clock Driver

MC88915

The MC88915 Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance PC's and workstations.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the MC88915 to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88915's can lock onto a single reference clock, which is ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 7).

Five "Q" outputs (QO–Q4) are provided with less than 500 ps skew between their rising edges. The $\overline{Q5}$ output is inverted (180° phase shift) from the "Q" outputs. The 2X_Q output runs at twice the "Q" output frequency, while the Q/2 runs at 1/2 the "Q" frequency.

The VCO is designed to run optimally between 20 MHz and the 2X_Q Fmax specification. The wiring diagrams in Figure 5 detail the different feedback configurations which create specific input/output frequency relationships. Possible frequency ratios of the "Q" outputs to the SYNC input are 2:1, 1:1, and 1:2.

The FREQ_SEL pin provides one bit programmable divide–by in the feedback path of the PLL. It selects between divide–by–1 and divide–by–2 of the VCO before its signal reaches the internal clock distribution section of the chip (see the block diagram on page 2). In most applications FREQ_SEL should be held high (÷1). If a low frequency reference clock input is used, holding FREQ_SEL low (÷2) will allow the VCO to run in its optimal range (>20 MHz).

In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88915 in a static "test mode". In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board–level testing (see detailed description on page 11).

A lock indicator output (LOCK) will go high when the loop is in steady–state phase and frequency lock. The LOCK output will go low if phase–lock is lost or when the PLL_EN pin is low. Under certain conditions the lock output may remain low, even though the part is phase–locked. Therefore the LOCK output signal should not be used to drive any active circuitry; it should be used for passive monitoring or evaluation purposes only.

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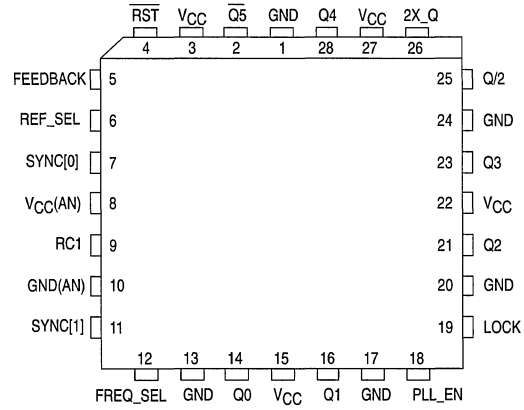
Features

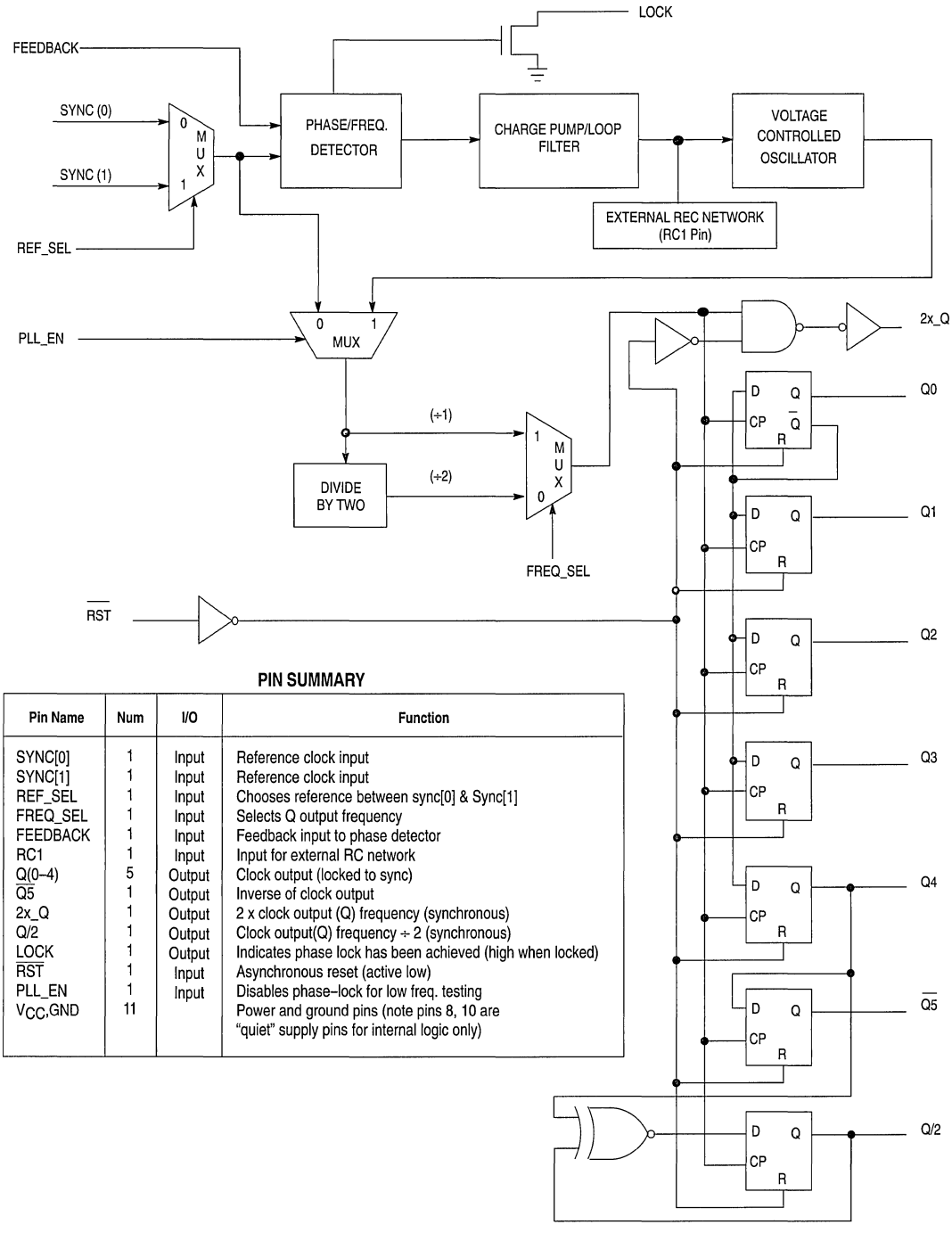
- Five Outputs (QO–Q4) with Output–Output Skew < 500 ps each being phase and frequency locked to the SYNC input
- The phase variation from part–to–part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t_{PD} specification, which defines the part–to–part skew)
- Input/Output phase–locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5MHz – 2X_Q FMAX spec
- Additional outputs available at 2X and +2 the system "Q" frequency. Also a $\overline{Q}$ (180° phase shift) output available
- All outputs have ±36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL–level compatible
- Test Mode pin (PLL_EN) provided for low frequency testing. Two selectable CLOCK inputs for test or redundancy purposes



28–Lead Pinout (Top View)

FN SUFFIX
PLASTIC PLCC
CASE 776–02

ORDERING INFORMATION
MC88915FN55 PLCC
MC88915FN70 PLCC



MC88915 Block Diagram

PIN SUMMARY

Pin Name	Num	I/O	Function
SYNC[0]	1	Input	Reference clock input
SYNC[1]	1	Input	Reference clock input
REF_SEL	1	Input	Chooses reference between sync[0] & Sync[1]
FREQ_SEL	1	Input	Selects Q output frequency
FEEDBACK	1	Input	Feedback input to phase detector
RC1	1	Input	Input for external RC network
Q(0–4)	5	Output	Clock output (locked to sync)
$\overline{Q5}$	1	Output	Inverse of clock output
2x_Q	1	Output	2 x clock output (Q) frequency (synchronous)
Q/2	1	Output	Clock output(Q) frequency ÷ 2 (synchronous)
LOCK	1	Output	Indicates phase lock has been achieved (high when locked)
$\overline{RST}$	1	Input	Asynchronous reset (active low)
PLL_EN	1	Input	Disables phase-lock for low freq. testing
V_{CC},GND	11		Power and ground pins (note pins 8, 10 are "quiet" supply pins for internal logic only)

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND; T_A =0° C to + 70° C, V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA [1]	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 36 mA [1]	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	±1.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} – 2.1 V	5.25	1.5 [2]	mA
I_{OLD}	Minimum Dynamic Output Current [3]	V_{OLD} = 1.0V Max	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85 V Max	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA

1. I_{OL} and I_{OH} are 12mA and –12mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0ms, one output loaded at a time.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1	Power Dissipation @ 33MHz with 50Ω Thevenin Termination	15 mW/Output 120 mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2	Power Dissipation @ 33MHz with 50Ω Parallel Termination to GND	37.5 mW/Output 300 mW/Device	mW	V_{CC} = 5.0 V T = 25° C

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Min		Max	Unit
t_{RISE}, t_{FALL}	Maximum Rise and Fall times, (SYNC Inputs: From 0.8V – 2.0V)	–		3.0	ns
t_{CYCLE}	Input Clock Period (SYNC Inputs)	FN55	FN70	200 [1]	ns
		36	28.5		
Duty Cycle	Input Duty Cycle (SYNC Inputs)	50% ±25%			

1. Information in Fig. 5 and in the "General AC Specification Notes", Note #3 describes this specification and its actual limits depending on the application.

FREQUENCY SPECIFICATIONS (T_A =0° C to + 70° C, V_{CC} = 5.0V ±5%, C_L = 50pF)

Symbol	Parameter	Guaranteed Minimum		Unit
		MC88915FN55	MC88915FN70	
f_{max} [1]	Maximum Operating Frequency (2X_Q Output)	55	70	MHz
	Maximum Operating Frequency (Q0–Q4,$\overline{Q5}$ Output)	27.5	35	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase–locked condition, and all outputs loaded at 50 pF.

AC ELECTRICAL CHARACTERISTICS (T_A =0° C to +70° C, V_{CC} = 5.0V ±5%, C_L = 50pF)

Symbol	Parameter	Min	Max	Unit
t_{RISE}, t_{FALL} (Outputs)	Rise and Fall Times, all Outputs Into a 50 pF, 500 Ω Load (Between 0.2V_{CC} and 0.8V_{CC})	1.0	2.5	ns
t_{RISE}, t_{FALL} [3] (2X_Q Output)	Rise and Fall Time, 2X_Q Output Into a 20 pF Load With Termination specified in note 2 (Between 0.8 V and 2.0 V)	0.5	1.6	ns
$t_{Pulse\ Width}$ [3] (Q0,Q1,Q3,Q4, $\overline{Q5}$,Q/2)	Output Pulse Width (Q0, Q1, Q3, Q4, $\overline{Q5}$, Q/2 @V_{CC}/2)	0.5t_{CYCLE} – 0.5	0.5t_{CYCLE} + 0.5	ns
		t_{CYCLE} = 1/Freq. at which the "Q" Outputs are running		
$t_{Pulse\ Width}$ [3] (Q2 only)	Output Pulse Width (Q2 Output @ V_{CC}/2)	0.5t_{CYCLE} – 0.6	0.5t_{CYCLE} + 0.6	
$t_{Pulse\ Width}$ [3] (2X_Q Output)	Output Pulse Width (2X_Q Output @ 1.5 V) (See AC Note 2)	0.5t_{CYCLE} – 0.5	0.5t_{CYCLE} + 0.5	ns
$t_{Pulse\ Width}$ [3] (2X_Q Output)	Output Pulse Width (2X_Q Output @ V_{CC}/2)	0.5t_{CYCLE} – 1.0	0.5t_{CYCLE} + 1.0	ns
t_{PD} [3] (Sync–Feedback)	SYNC input to feedback delay (meas. @ SYNC0 or 1 and FEEDBACK input pins) (See General AC Specification note 4 and Fig. 2 for explanation)	(470kΩ From RC1 to An.V_{CC}) –1.05 (470kΩ From RC1 to An.GND) +1.25	–0.50 +3.25	ns
t_{SKEWr} [1,3] (Rising)	Output–to–Output Skew Between Outputs Q0 – Q4, Q/2 (Rising Edges Only)	–	500	ps
t_{SKEWf} [1,3] (Falling)	Output–to–Output Skew Between Outputs Q0 – Q4 (Falling Edges Only)	–	750	ps
$t_{SKEWall}$ [1,3]	Output–to–Output Skew Between Outputs 2X_Q, Q/2, Q0 – Q4 Rising, $\overline{Q5}$ Falling	–	750	ps
t_{LOCK}	Time Required to acquire [2] Phase–Lock from time SYNC Input Signal is Received.	1	10	ms
t_{PHL} (Reset – Q)	Propagation Delay, RST to Any Output (High–Low)	1.5	13.5	ns

1. Under equally loaded conditions, C_L ≤50pF (±2pF), and at a fixed temperature and voltage.
2. With V_{CC} fully powered–on and an output properly connected to the FEEDBACK pin. t_{LOCK} Max. is with C1 = 0.1µF, t_{LOCK} Min is with C1 = 0.01µF.
3. These specifications are not tested, they are guaranteed by statistical characterization. See General AC Specification note 1.

RESET TIMING REQUIREMENTS [1]

Symbol	Parameter	Minimum	Unit
t_{REC}, $\overline{RST}$ to SYNC	Reset Recovery Time rising $\overline{RST}$ edge to falling SYNC edge	9.0	ns
t_W, $\overline{RST}$ LOW	Minimum Pulse Width, $\overline{RST}$ input LOW	5.0	ns

1. These reset specs are valid only when PLL_EN is LOW and the part is in Test mode (not in phase–lock)

General AC Specification Notes

1. Several specifications can only be measured when the MC88915 is in phase–locked operation. It is not possible to have the part in phase–lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88915 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area. Response Surface Modeling (RSM) techniques were used to relate IC performance to the CMOS transistor properties over operation voltage and temperature. IC Performance to each specification and fab variation were used in conjunction with Yield Surface Modeling™ (YSM ™) methodology to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way all units passing the ATE test will meet or exceed the non–tested specifications limits.

2. These two specs ($t_{RISE/FALL}$ and t_{PULSE} Width 2X_Q output) guarantee that the MC88915 meets the 25 MHz 68040 P–Clock input specification (at 50 MHz). For these two specs to be guaranteed by Motorola, the termination scheme shown below in Figure 1 must be used.

3. The wiring Diagrams and written explanations in Figure 5 demonstrate the input and output frequency relationships for three possible feedback configurations. The allowable SYNC input range for each case is also indicated. There are two allowable SYNC frequency ranges, depending whether FREQ_SEL is high or low. Although not shown, it is possible to feed back the $\overline{Q5}$ output, thus creating a 180° phase shift between the SYNC input and the "Q" outputs. Table 1 below summarizes the allowable SYNC frequency range for each possible configuration.

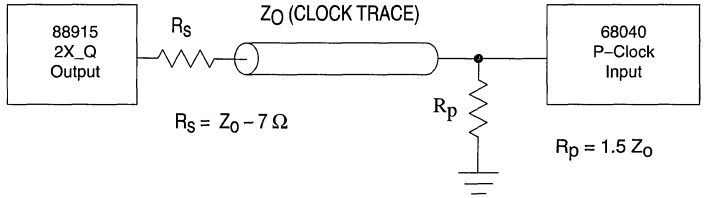
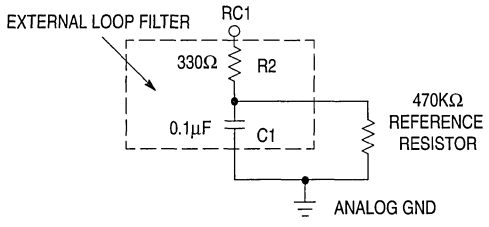


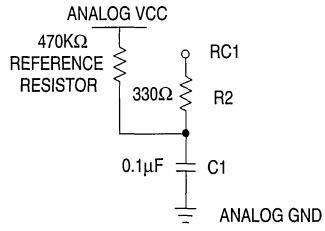
Figure 1. MC68040 P–Clock Input Termination Scheme

FREQ_SEL Level	Feedback Output	Allowable SYNC Input Frequency Range (MHZ)	Corresponding VCO Frequency Range	Phase Relationships of the "Q" Outputs to Rising SYNC Edge
HIGH	Q/2	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
HIGH	Any "Q" (Q0–Q4)	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	0°
HIGH	$\overline{Q5}$	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	180°
HIGH	2X_Q	20 to (2X_Q FMAX Spec)	20 to (2X_Q FMAX Spec)	0°
LOW	Q/2	2.5 to (2X_Q FMAX Spec)/8	20 to (2X_Q FMAX Spec)	0°
LOW	Any "Q" (Q0–Q4)	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
LOW	$\overline{Q5}$	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAXSpec)	180°
LOW	2X_Q	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAXSpec)	0°

Table 1. Allowable SYNC Input Frequency Ranges for Different Feedback Configurations.

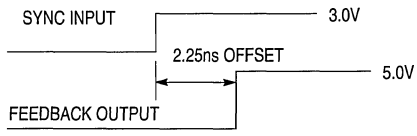
4. A 1 MΩ resistor tied to either Analog V_{CC} or Analog GND as shown in Figure 2 is required to ensure no jitter is present on the MC88915 outputs. This technique causes a phase offset between the SYNC input and the output connected to the FEEDBACK input, measured at the input pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14 lots described in note 1 while the part was in phase–locked operation. The actual measurements were made with a 10 MHz SYNC input (1.0 ns edge rate from 0.8 V – 2.0 V) with the Q/2 output fed back. The phase measurements were made at 1.5 V. The Q/2 output was terminated at the FEEDBACK input with 100Ω to V_{CC} and 100 Ω to ground.





With the 470KΩ resistor tied in this fashion, the t_{PD} specification measured at the input pins is:

$t_{PD} = 2.25ns \pm 1.0ns$



With the 470KΩ resistor tied in this fashion, the t_{PD} specification measured at the input pins is:

$t_{PD} = -0.775ns \pm 0.275ns$

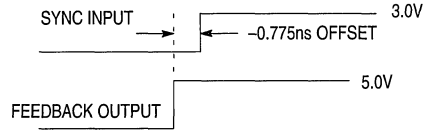


Figure 2. Depiction of the Fixed SYNC to Feedback Offset (tPD) Which is Present When a 470KΩ Resistor is Tied to VCC or Ground

5. The t_{SKEWr} specification guarantees that the rising edges of outputs Q/2, Q0, Q1, Q2, Q3, and Q4 will always fall within a 500ps window within one part. However, if the relative position of each output within this window is not specified, the 500 ps window must be added to each side of the tPD specification limits to calculate the total part–to–part skew. For this reason the absolute distribution of these outputs are provided in table 2. When taking the skew data, Q0 was used as a reference, so all measurements are relative to this output. The information in Table 2 is derived from measurements taken from the 14 process lots described in Note 1, over the temperature and voltage range.

Output	– (ps)	+ (ps)
Q0	0	0
Q1	–72	40
Q2	–44	276
Q3	–40	255
Q4	–274	–34
Q/2	–16	250
2X_Q	–633	–35

Table 2. Relative Positions of Outputs Q/2, Q0–Q4, 2X_Q, Within the 500ps t_{SKEWr} Spec Window

6. Calculation of Total Output–to–Skew between multiple parts (Part–to–Part skew)

   By combining the t_{PD} specification and the information in Note 5, the worst case output–to–output skew between multiple 88915's connected in parallel can be calculated. This calculation assumes that all parts have a common SYNC input clock with equal delay of that input signal to each part. This skew value is valid at the 88915 output pins only (equally loaded), it does not include PCB trace delays due to varying loads.

   With a 1MΩ resistor tied to analog V_{CC} as shown in note 4, the t_{PD} spec. limits between SYNC and the Q/2 output (connected to the FEEDBACK pin) are –1.05ns and –0.5ns. To calculate the skew of any given output between two or more parts, the absolute value of the distribution of that output given in table 2 must be subtracted and added to the lower and upper t_{PD} spec limits respectively. For output Q2, [276 – (–44)] = 320ps is the absolute value of the distribution. Therefore [–1.05ns – 0.32ns] = –1.37ns is the lower t_{PD} limit, and [–0.5ns + 0.32ns] = –0.18ns is the upper limit. Therefore the worst case skew of output Q2 between any number of parts is |(–1.37) – (–0.18)| = 1.19ns. Q2 has the worst case skew distribution of any output, so 1.2ns is the absolute worst case output–to–output skew between multiple parts.

7. Note 4 explains that the t_{PD} specification was measured and is guaranteed for the configuration of the Q/2 output connected to the FEEDBACK pin and the SYNC input running at 10MHz. The fixed offset (t_{PD}) as described above has some dependence on the input frequency and at what frequency the VCO is running. The graphs of Figure 3 demonstrate this dependence.

   The data presented in Figure 3 is from devices representing process extremes, and the measurements were also taken at the voltage extremes (V_{CC} = 5.25V and 4.75V). Therefore the data in Figure 3 is a realistic representation of the variation of t_{PD}.

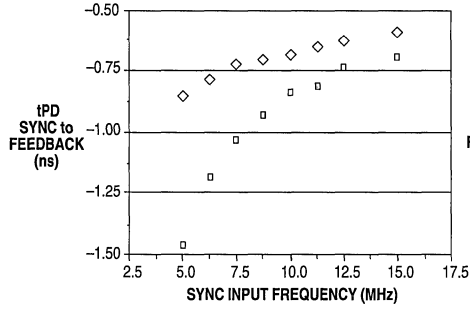


Figure 3a.

t_{PD} versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1MΩ Resistor Tied to Analog V_{CC})

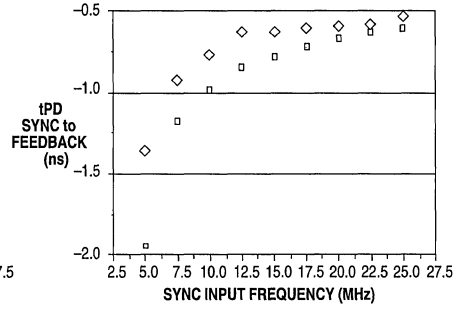


Figure 3b.

t_{PD} versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1MΩ Resistor Tied to Analog V_{CC})

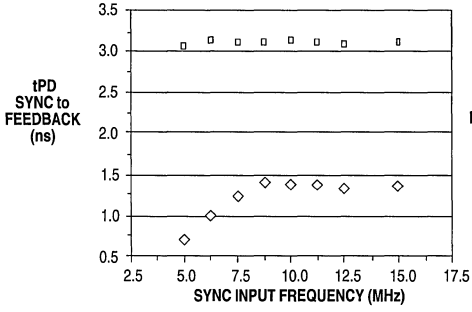


Figure 3c.

t_{PD} versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1MΩ Resistor Tied to Analog GND)

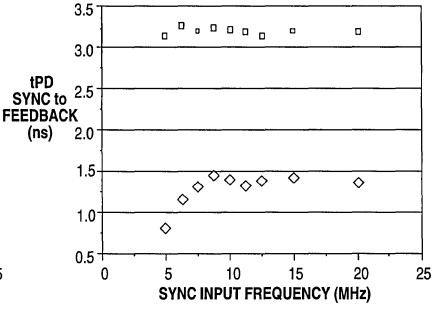


Figure 3d.

t_{PD} versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1MΩ Resistor Tied to Analog GND)

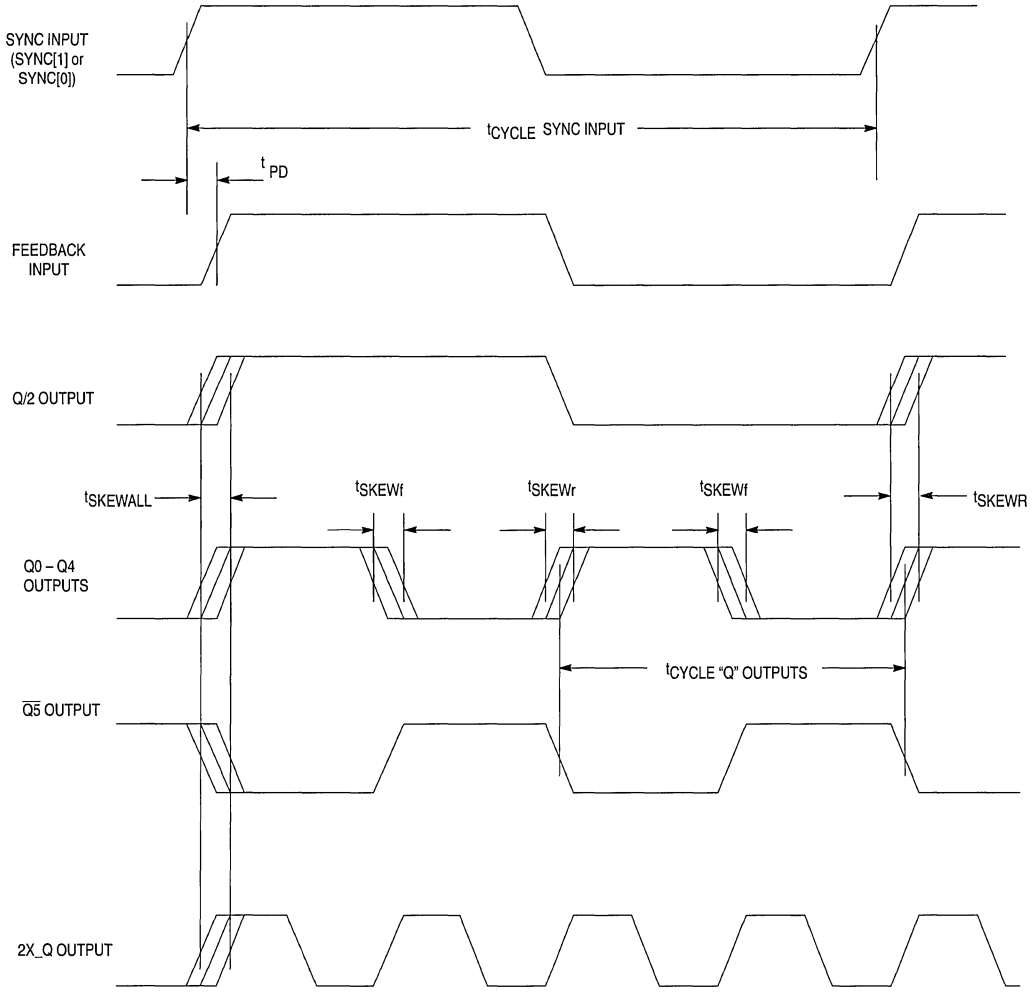
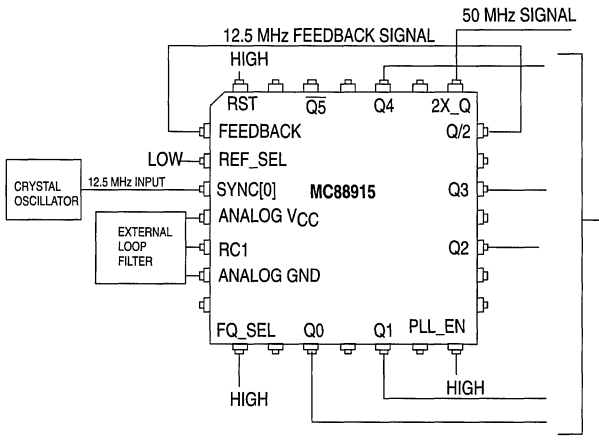


Figure 4. Output / Input Switching Waveforms and Timing Diagrams

(These waveforms represent the hook–up configuration of Figure 5a on page 164)

Timing Notes:

- The MC88915 aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
- All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges.All skews are specified as 'windows', not as a ± deviation around a center point.
- If a "Q" output is connected to the FEEDBACK input (this situation is not shown), the "Q" output frequency would match the SYNC input frequency, the 2X_Q output would run at twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency.



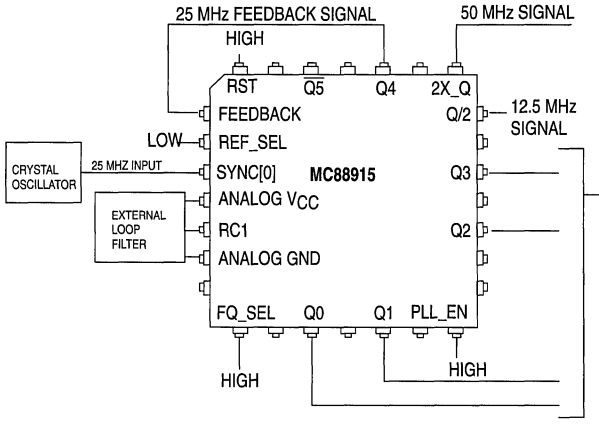
1:2 Input to "Q" Output Frequency Relationship

In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The "Q" outputs (Q0–Q4, $\overline{Q5}$) will always run at 2X the Q/2 frequency, and the 2X_Q output will run at 4X the Q/2 frequency.

Allowable Input Frequency Range:

5MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL HIGH)
2.5MHz to (2X_Q FMAX Spec)/8 (for FREQ_SEL LOW)

Figure 5a. Wiring Diagram and Frequency Relationships With Q/2 Output Feed Back



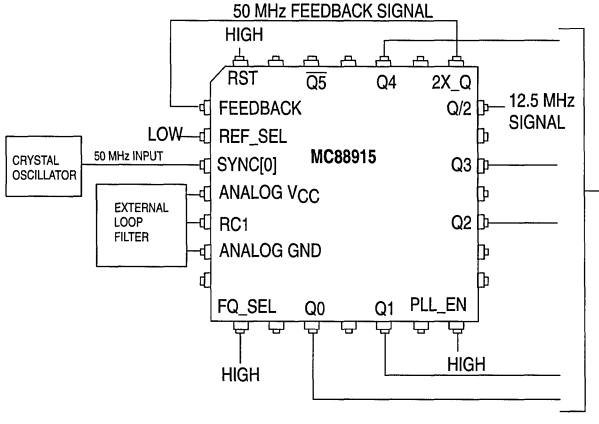
1:1 Input to "Q" Output Frequency Relationship

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the "Q" frequency, and the 2X_Q output will run at 2X the "Q" frequency.

Allowable Input Frequency Range:

10MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL HIGH)
5MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL LOW)

Figure 5b. Wiring Diagram and Frequency Relationships With Q4 Output Feed Back



2:1 Input to "Q" Output Frequency Relationship

In this application, the 2X_Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2X_Q and SYNC, thus the 2X_Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2X_Q frequency, and the "Q" outputs will run at 1/2 the 2X_Q frequency.

Allowable Input Frequency Range:

20MHz to (2X_Q FMAX Spec) (for FREQ_SEL HIGH)
10MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL LOW)

Figure 5c. Wiring Diagram and Frequency Relationships with 2X_Q Output Feed Back

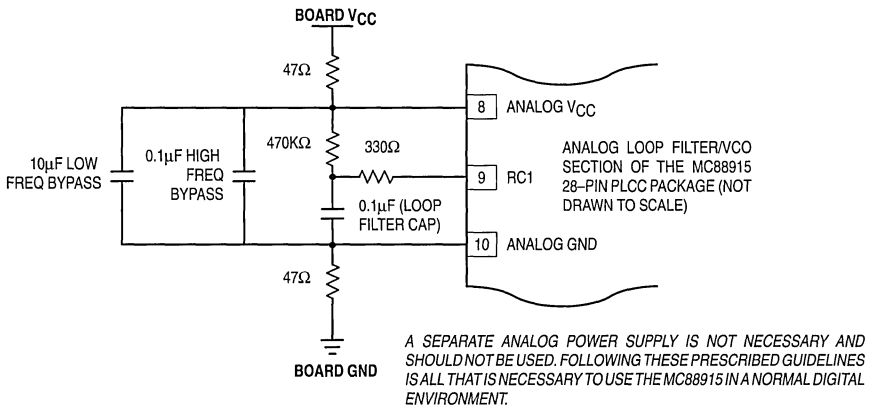


Figure 6. Recommended Loop Filter and Analog Isolation Scheme for the MC88915

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 6 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88915's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100pS phase deviation on the 88915 outputs. A 250mV step deviation on V_{CC} using the recommended filter values should cause no more than a 250pS phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step should cause no more than a 100pS phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88915's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 6 is to give the 88915 additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (470K and 330Ω). The loop filter capacitor (0.1μF) can be a ceramic chip capacitior, the same as a standard bypass capacitor.

1d. The 470K reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 470K resistor provides the correct amount of current injection into the charge pump (2–3μA). If the VCO is running below 40MHz, a 1MΩ reference resistor should be used (instead of 470K).

2. In addition to the bypass capacitors used in the analog filter of Figure 6, there should be a 0.1μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88915 outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88915 package as possible.

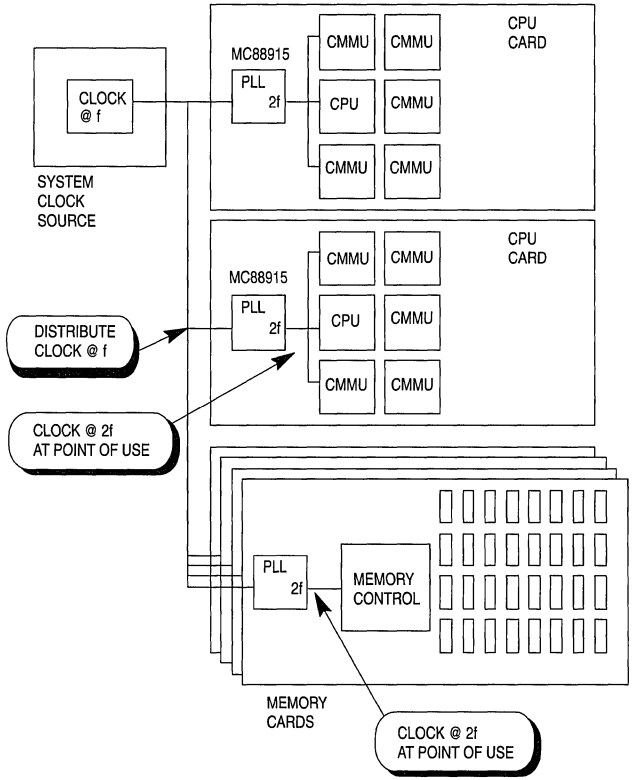


Figure 7. Representation of a Potential Multi–Processing Application Utilizing the MC88915 for Frequency Multiplication and Low Board–to–Board Skew

MC88915 System Level Testing Functionality

When the PLL_EN pin is low, the VCO is disabled and the 88915 is in low frequency "test mode". In test mode (with FREQ_SEL high), the 2X_Q output is inverted from the selected SYNC input, and the "Q" outputs are divide–by–2 (negative edge triggered) of the SYNC input, and the Q/2 output is divide–by–4. With FREQ_SEL low the 2X_Q output is divide–by–2 of the SYNC, the "Q" outputs divide–by–4, and the Q/2 output divide–by–8. These relationships can be seen on the block diagram. A recommended test configuration would be to use SYNC0 as the test clock input, and tie PLL_EN and REF_SEL together and connect them to the test select logic. When these inputs are low, the 88915 is in test mode and the SYNC0 input is selected.

This functionality is needed since most board–level testers run at 1 MHz or below, and the 88915 cannot lock onto that low of an input frequency. In the test mode described above, any frequency test signal can be used.

Low Skew CMOS PLL Clock Drivers, 3-State

55, 70, 100, 133 and 160MHz Versions

MC88915TFN55
MC88915TFN70
MC88915TFN100
MC88915TFN133
MC88915TFN160

LOW SKEW CMOS PLL CLOCK DRIVER

The MC88915T Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance PC's and workstations. For a 3.3V version, see the MC88LV915T data sheet.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the MC88915T to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88915's can lock onto a single reference clock, which is ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 7).

Five "Q" outputs (Q0–Q4) are provided with less than 500 ps skew between their rising edges. The $\overline{Q5}$ output is inverted (180° phase shift) from the "Q" outputs. The 2X_Q output runs at twice the "Q" output frequency, while the Q/2 runs at 1/2 the "Q" frequency.

The VCO is designed to run optimally between 20 MHz and the 2X_Q F_{max} specification. The wiring diagrams in Figure 5 detail the different feedback configurations which create specific input/output frequency relationships. Possible frequency ratios of the "Q" outputs to the SYNC input are 2:1, 1:1, and 1:2.

The FREQ_SEL pin provides one bit programmable divide–by in the feedback path of the PLL. It selects between divide–by–1 and divide–by–2 of the VCO before its signal reaches the internal clock distribution section of the chip (see the block diagram on page 2). In most applications FREQ_SEL should be held high (÷1). If a low frequency reference clock input is used, holding FREQ_SEL low (÷2) will allow the VCO to run in its optimal range (>20MHz and >40MHz for the TFN133 version).

In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88915 in a static "test mode". In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board–level testing (see detailed description on page 11).

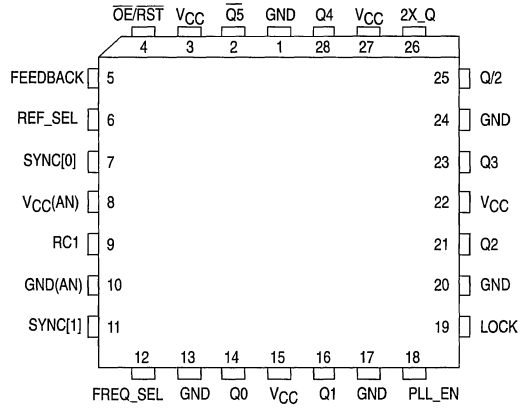
Pulling the $\overline{OE}/\overline{RST}$ pin low puts the clock outputs 2X_Q, Q0–Q4, $\overline{Q5}$ and Q/2 into a high impedance state (3–state). After the $\overline{OE}/\overline{RST}$ pin goes back high Q0–Q4, $\overline{Q5}$ and Q/2 will be reset in the low state, with 2X_Q being the inverse of the selected SYNC input. Assuming PLL_EN is low, the outputs will remain reset until the 88915 sees a SYNC input pulse.

A lock indicator output (LOCK) will go high when the loop is in steady–state phase and frequency lock. The LOCK output will go low if phase–lock is lost or when the PLL_EN pin is low. The LOCK output will go high no later than 10ms after the 88915 sees a SYNC signal and full 5V V_{CC}.

Features

- Five Outputs (Q0–Q4) with Output–Output Skew < 500 ps each being phase and frequency locked to the SYNC input
- The phase variation from part–to–part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t_{PD} specification, which defines the part–to–part skew)
- Input/Output phase–locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5MHz – 2X_Q FMAX spec. (10MHz – 2X_Q FMAX for the TFN133 version)
- Additional outputs available at 2X and +2 the system "Q" frequency. Also a $\overline{Q}$ (180° phase shift) output available
- All outputs have ±36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL–level compatible. ±88mA I_{OL}/I_{OH} specifications guarantee 50Ω transmission line switching on the incident edge
- Test Mode pin (PLL_EN) provided for low frequency testing. Two selectable CLOCK inputs for test or redundancy purposes. All outputs can go into high impedance (3–state) for board test purposes
- Lock Indicator (LOCK) accuracy indicates a phase–locked state

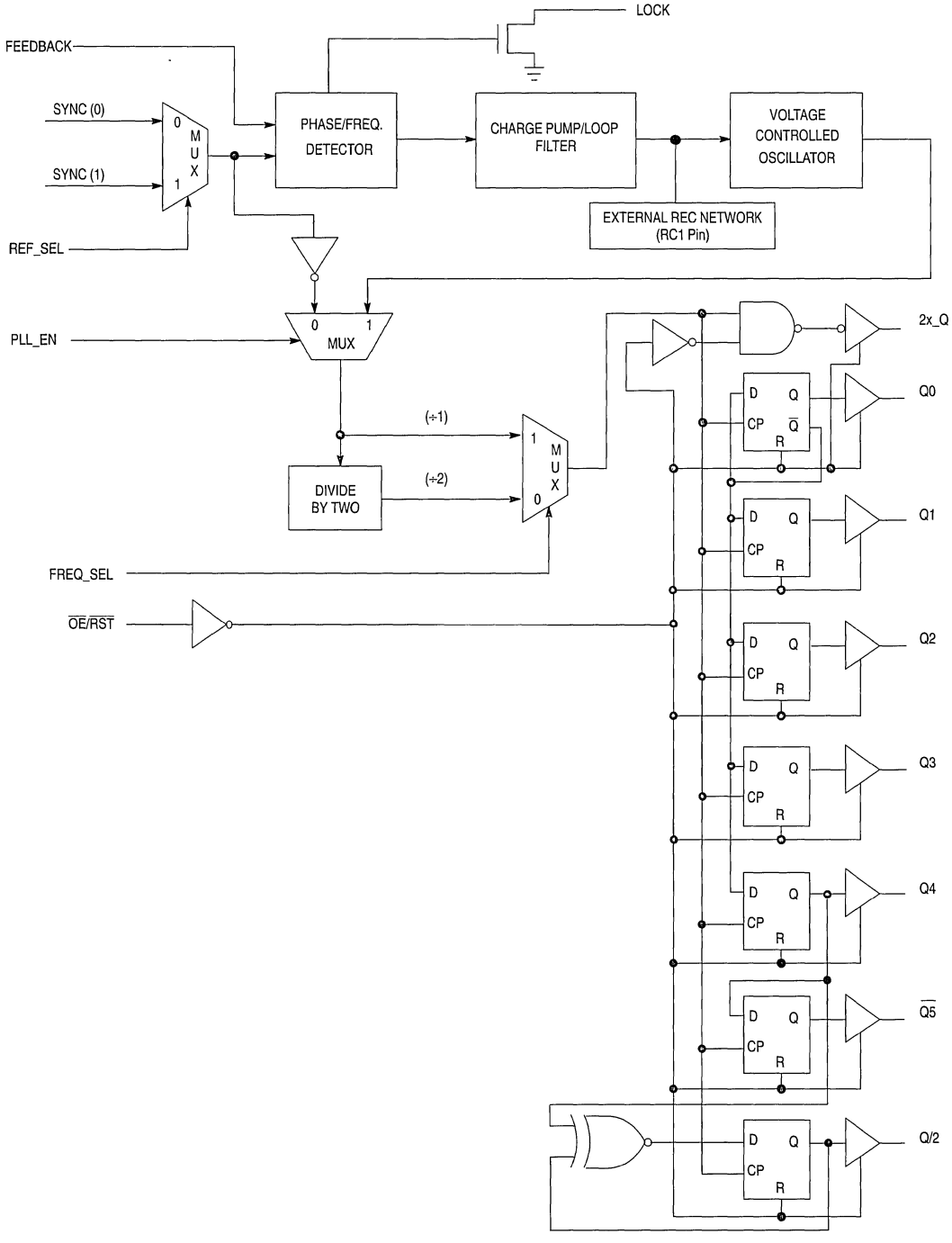
Pinout: 28–Lead PLCC (Top View)



FN SUFFIX
PLASTIC PLCC
CASE 776–02

PIN SUMMARY

Pin Name	Num	I/O	Function
SYNC[0]	1	Input	Reference clock input
SYNC[1]	1	Input	Reference clock input
REF_SEL	1	Input	Chooses reference between sync[0] & Sync[1]
FREQ_SEL	1	Input	Doubles VCO Internal Frequency (low)
FEEDBACK	1	Input	Feedback input to phase detector
RC1	1	Input	Input for external RC network
Q(0–4)	5	Output	Clock output (locked to sync)
$\overline{Q5}$	1	Output	Inverse of clock output
2x_Q	1	Output	2 x clock output (Q) frequency (synchronous)
Q/2	1	Output	Clock output(Q) frequency ÷ 2 (synchronous)
LOCK	1	Output	Indicates phase lock has been achieved (high when locked)
$\overline{OE/RST}$	1	Input	Output Enable/Asynchronous reset (active low)
PLL_EN	1	Input	Disables phase–lock for low freq. testing
V_{CC},GND	11		Power and ground pins (note pins 8, 10 are "analog" supply pins for internal PLL only)



MC88915T Block Diagram (All Versions)

MC88915TFN55 and MC88915TFN70

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum		Maximum	Unit
		TFN70	TFN55		
$t_{RISE/FALL}$,SYNC Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	—	—	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period SYNC Inputs	28.5 [1]	36.0 [1]	200 [2]	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% ±25%			

1. These t_{CYCLE} minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
2. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ_SEL is high or low.

DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to GND) T_A =–40° C to +85° C for 55MHz Version; T_A =0° C to +70° C for 70MHz Version; V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA [1]	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 36 mA [1]	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	±1.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} – 2.1 V	5.25	2.0 [2]	mA
I_{OLD}	Minimum Dynamic Output Current [3]	V_{OLD} = 1.0V Max	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85V Min	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3–State Leakage Current	V_I = V_{IH} or V_{IL};V_O = V_{CC} or GND	5.25	±50 [4]	µA

1. I_{OL} and I_{OH} are 12mA and –12mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0ms, one output loaded at a time.
4. Specification value for I_{OZ} is preliminary, will be finalized upon 'MC' status.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1	Power Dissipation @ 50MHz with 50Ω Thevenin Termination	23mW/Output 184mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2	Power Dissipation @ 50MHz with 50Ω Parallel Termination to GND	57mW/Output 456mW/Device	mW	V_{CC} = 5.0 V T = 25° C

NOTE: PD_1 and PD_2 mW/Output numbers are for a 'Q' output.

FREQUENCY SPECIFICATIONS (T_A =–40° C to +85° C, V_{CC} = 5.0 V ±5%)

Symbol	Parameter	Guaranteed Minimum		Unit
		TFN70	TFN55	
f_{max} [1]	Maximum Operating Frequency (2X_Q Output)	70	55	MHz
	Maximum Operating Frequency (Q0–Q4,$\overline{Q5}$ Output)	35	27.5	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase–locked condition, and all outputs loaded with 50Ω terminated to V_{CC}/2.

MC88915TFN55 and MC88915TFN70 (continued)

AC CHARACTERISTICS (T_A =–40° C to +85° C, V_{CC} = 5.0V ±5%, Load = 50Ω Terminated to V_{CC}/2)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2V_{CC} and 0.8V_{CC})	1.0	2.5	ns	Into a 50Ω Load Terminated to V_{CC}/2
$t_{RISE/FALL}$ [1] 2X_Q Output	Rise/Fall Time Into a 20pF Load, With Termination Specified in Note 2	0.5	1.6	ns	t_{RISE}: 0.8V – 2.0V t_{FALL}: 2.0V – 0.8V
$t_{PULSE\ WIDTH}$ [1] (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ V_{CC}/2	0.5t_{CYCLE} – 0.5 [2]	0.5t_{CYCLE} + 0.5 [2]	ns	Into a 50Ω Load Terminated to V_{CC}/2
$t_{PULSE\ WIDTH}$ [1] (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5V 66MHz 50MHz 40MHz	0.5t_{CYCLE} – 0.5 [2] 0.5t_{CYCLE} – 1.0 0.5t_{CYCLE} – 1.5	0.5t_{CYCLE} + 0.5 [2] 0.5t_{CYCLE} + 1.0 0.5t_{CYCLE} + 1.5	ns	Must Use Termination Specified in Note 2
$t_{PULSE\ WIDTH}$ [1] (2X_Q Output)	Output Pulse Width: 2X_Q @ V_{CC}/2 50–65MHz 40–49MHz 66–70MHz	0.5t_{CYCLE} – 1.0 [2] 0.5t_{CYCLE} – 1.5 0.5t_{CYCLE} – 0.5	0.5t_{CYCLE} + 1.0 [2] 0.5t_{CYCLE} + 1.5 0.5t_{CYCLE} + 0.5	ns	Into a 50Ω Load Terminated to V_{CC}/2
t_{PD} [1,3] SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1MΩ from RC1 to An V_{CC}) –1.05 (With 1MΩ from RC1 to An GND) +1.25	–0.40 +3.25	ns	See Note 4 and Figure 2 for Detailed Explanation
t_{SKEWr} [1,4] (Rising) See Note 5	Output–to–Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V_{CC}/2
t_{SKEWf} [1,4] (Falling)	Output–to–Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V_{CC}/2
$t_{SKEWall}$ [1,4]	Output–to–Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to V_{CC}/2
t_{LOCK} [5]	Time Required to Acquire Phase–Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL} [6]	Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
t_{PHZ},t_{PLZ} [6]	Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. These specifications are not tested, they are guaranteed by statistcal characterization. See AC specification Note 1.
2. T_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
3. The T_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With V_{CC} fully powered–on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1µF, t_{LOCK} minimum is with C1 = 0.01µF.
6. The t_{PZL}, t_{PHZ}, t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

MC88915TFN100

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$,SYNC Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	—	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period SYNC Inputs	20.0 [1]	200 [2]	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% ±25%		

1. These t_{CYCLE} minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
2. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ_SEL is high or low.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) T_A =–40° C to +85° C, V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA [1]	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 36 mA [1]	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	±1.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} – 2.1 V	5.25	2.0 [2]	mA
I_{OLD}	Minimum Dynamic Output Current [3]	V_{OLD} = 1.0V Max	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85V Min	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3–State Leakage Current	V_I = V_{IH} or V_{IL};V_O = V_{CC} or GND	5.25	±50 [4]	µA

1. I_{OL} and I_{OH} are 12mA and –12mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0ms, one output loaded at a time.
4. Specification value for I_{OZ} is preliminary, will be finalized upon 'MC' status.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1	Power Dissipation @ 50MHz with 50Ω Thevenin Termination	23mW/Output 184mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2	Power Dissipation @ 50MHz with 50Ω Parallel Termination to GND	57mW/Output 456mW/Device	mW	V_{CC} = 5.0 V T = 25° C

NOTE: PD_1 and PD_2 mW/Output numbers are for a 'Q' output.

FREQUENCY SPECIFICATIONS (T_A =–40° C to +85° C, V_{CC} = 5.0 V ±5%)

Symbol	Parameter	Guaranteed Minimum TFN100	Unit
f_{max} [1]	Maximum Operating Frequency (2X_Q Output)	100	MHz
	Maximum Operating Frequency (Q0–Q4,$\overline{Q5}$ Output)	50	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase–locked condition, and all outputs loaded with 50Ω terminated to V_{CC}/2.

MC88915TFN100 (continued)

AC CHARACTERISTICS (T_A =–40° C to +85° C, V_{CC} = 5.0V ±5%, Load = 50Ω Terminated to V_{CC}/2)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2V_{CC} and 0.8V_{CC})	1.0	2.5	ns	Into a 50Ω Load Terminated to V_{CC}/2
$t_{RISE/FALL}$ [1] 2X_Q Output	Rise/Fall Time Into a 20pF Load, With Termination Specified in Note [2]	0.5	1.6	ns	t_{RISE}: 0.8V – 2.0V t_{FALL}: 2.0V – 0.8V
$t_{PULSE\ WIDTH}$ [1] (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ V_{CC}/2	0.5t_{CYCLE} – 0.5 [2]	0.5t_{CYCLE} + 0.5 [2]	ns	Into a 50Ω Load Terminated to V_{CC}/2
$t_{PULSE\ WIDTH}$ [1] (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5V	0.5t_{CYCLE} – 0.5 [2]	0.5t_{CYCLE} + 0.5 [2]	ns	Must Use Termination Specified in Note **2**
$t_{PULSE\ WIDTH}$ [1] (2X_Q Output)	Output Pulse Width: 2X_Q @ V_{CC}/2 40–49MHz 50–65MHz 66–100MHz	0.5t_{CYCLE} – 1.5 [2] 0.5t_{CYCLE} – 1.0 0.5t_{CYCLE} – 0.5	0.5t_{CYCLE} + 1.5 [2] 0.5t_{CYCLE} + 1.0 0.5t_{CYCLE} + 0.5	ns	Into a 50Ω Load Terminated to V_{CC}/2
t_{PD} [1,3] SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1MΩ from RC1 to An V_{CC}) –1.05 (With 1MΩ from RC1 to An GND) +1.25	 –0.30 +3.25	ns	See Note **4** and Figure 2 for Detailed Explanation
t_{SKEWr} [1,4] (Rising) See Note [5]	Output–to–Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V_{CC}/2
t_{SKEWf} [1,4] (Falling)	Output–to–Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V_{CC}/2
$t_{SKEWall}$ [1,4]	Output–to–Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to V_{CC}/2
t_{LOCK} [5]	Time Required to Acquire Phase–Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL} [6]	Output Enable Time $\overline{OE/RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
t_{PHZ},t_{PLZ} [6]	Output Disable Time $\overline{OE/RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. These specifications are not tested, they are guaranteed by statistcal characterization. See AC specification Note 1.
2. T_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
3. The T_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With V_{CC} fully powered–on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1µF, t_{LOCK} minimum is with C1 = 0.01µF.
6. The t_{PZL}, t_{PHZ}, t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

MC88915TFN133

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$, SYNC Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	—	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period SYNC Inputs	15.0 [1]	100 [2]	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% ±25%		

1. These t_{CYCLE} minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
2. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ_SEL is high or low.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) T_A =–40° C to +85° C, V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA [1]	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 36 mA [1]	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	±1.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} – 2.1 V	5.25	2.0 [2]	mA
I_{OLD}	Minimum Dynamic Output Current [3]	V_{OLD} = 1.0V Max	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85V Min	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3–State Leakage Current	V_I = V_{IH} or V_{IL};V_O = V_{CC} or GND	5.25	±50 [4]	µA

1. I_{OL} and I_{OH} are 12mA and –12mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0ms, one output loaded at a time.
4. Specification value for I_{OZ} is preliminary, will be finalized upon 'MC' status.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1	Power Dissipation @ 50MHz with 50Ω Thevenin Termination	23mW/Output 184mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2	Power Dissipation @ 50MHz with 50Ω Parallel Termination to GND	57mW/Output 456mW/Device	mW	V_{CC} = 5.0 V T = 25° C

NOTE: PD_1 and PD_2 mW/Output numbers are for a 'Q' output.

FREQUENCY SPECIFICATIONS (T_A =–40° C to +85° C, V_{CC} = 5.0 V ±5%)

Symbol	Parameter	Guaranteed Minimum TFN133	Unit
f_{max} [1]	Maximum Operating Frequency (2X_Q Output)	133	MHz
	Maximum Operating Frequency (Q0–Q4,$\overline{Q5}$ Output)	66	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase–locked condition, and all outputs loaded with 50Ω terminated to V_{CC}/2.

MC88915TFN133 (continued)

AC CHARACTERISTICS (T_A =–40° C to +85° C, V_{CC} = 5.0V ±5%, Load = 50Ω Terminated to $V_{CC}/2$)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2V_{CC} and 0.8V_{CC})	1.0	2.5	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
$t_{RISE/FALL}$ [1] 2X_Q Output	Rise/Fall Time Into a 20pF Load, With Termination Specified in Note 2	0.5	1.6	ns	t_{RISE}: 0.8V – 2.0V t_{FALL}: 2.0V – 0.8V
$t_{PULSE\ WIDTH}$ [1] (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}/2$	0.5t_{CYCLE} – 0.5 [2]	0.5t_{CYCLE} + 0.5 [2]	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
$t_{PULSE\ WIDTH}$ [1] (2X_Q Output)	Output Pulse Width: 66–133MHz 2X_Q @ 1.5V 40–65MHz	0.5t_{CYCLE} – 0.5 [2] 0.5t_{CYCLE} – 0.9	0.5t_{CYCLE} + 0.5 [2] 0.5t_{CYCLE} + 0.9	ns	Must Use Termination Specified in Note 2
$t_{PULSE\ WIDTH}$ [1] (2X_Q Output)	Output Pulse Width: 66–133MHz 2X_Q @ $V_{CC}/2$ 40–65MHz	0.5t_{CYCLE} – 0.5 [2] 0.5t_{CYCLE} – 0.9	0.5t_{CYCLE} + 0.5 [2] 0.5t_{CYCLE} + 0.9	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
t_{PD} [1,3] SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1MΩ from RC1 to An V_{CC})		ns	See Note 4 and Figure 2 for Detailed Explanation
		–1.05	–0.25		
		(With 1MΩ from RC1 to An GND)			
		+1.25	+3.25		
t_{SKEWr} [1,4] (Rising) See Note 5	Output–to–Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
t_{SKEWf} [1,4] (Falling)	Output–to–Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
$t_{SKEWall}$ [1,4]	Output–to–Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
t_{LOCK} [5]	Time Required to Acquire Phase–Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL} [6]	Output Enable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
t_{PHZ},t_{PLZ} [6]	Output Disable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. These specifications are not tested, they are guaranteed by statistcal characterization. See AC specification Note 1.
2. T_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
3. The T_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With V_{CC} fully powered–on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1µF, t_{LOCK} minimum is with C1 = 0.01µF.
6. The t_{PZL}, t_{PHZ}, t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

MC88915TFN160

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$,SYNC Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	—	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period SYNC Inputs	12.5	100	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% ±25%		

1. These t_{CYCLE} minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
2. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ_SEL is high or low.

DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to GND) T_A =0° C to +70° C, V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA [1]	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 36 mA [1]	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	±1.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} – 2.1 V	5.25	2.0 [2]	mA
I_{OLD}	Minimum Dynamic Output Current [3]	V_{OLD} = 1.0V Max	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85V Min	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3–State Leakage Current	V_I = V_{IH} or V_{IL};V_O = V_{CC} or GND	5.25	±50 [4]	µA

1. I_{OL} and I_{OH} are 12mA and –12mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0ms, one output loaded at a time.
4. Specification value for I_{OZ} is preliminary, will be finalized upon 'MC' status.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1	Power Dissipation @ 50MHz with 50Ω Thevenin Termination	15mW/Output 120mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2	Power Dissipation @ 50MHz with 50Ω Parallel Termination to GND	57mW/Output 456mW/Device	mW	V_{CC} = 5.0 V T = 25° C

NOTE: PD_1 and PD_2 mW/Output numbers are for a 'Q' output.

FREQUENCY SPECIFICATIONS (T_A =0° C to +70° C, V_{CC} = 5.0 V ±5%)

Symbol	Parameter	Guaranteed Minimum TFN160	Unit
f_{max} [1]	Maximum Operating Frequency (2X_Q Output)	160	MHz
	Maximum Operating Frequency (Q0–Q4,$\overline{Q5}$ Output)	80	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase–locked condition, and all outputs loaded with 50Ω terminated to V_{CC}/2.

MC88915TFN160 (continued)

AC CHARACTERISTICS (T_A =0° C to +70° C, V_{CC} = 5.0V ±5%, Load = 50Ω Terminated to $V_{CC}/2$)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2V_{CC} and 0.8V_{CC})	1.0	2.5	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
$t_{RISE/FALL}$ 2X_Q Output	Rise/Fall Time	0.5	1.6	ns	t_{RISE}: 0.8V – 2.0V t_{FALL}: 2.0V – 0.8V
$t_{PULSE\ WIDTH}$ (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}/2$	$0.5t_{CYCLE} - 0.5$ [2]	$0.5t_{CYCLE} + 0.5$ [2]	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
$t_{PULSE\ WIDTH}$ (2X_Q Output)	Output Pulse Width: 2X_Q @ V_{CC} 80MHz 100MHz 133MHz 160MHz	$0.5t_{CYCLE} - 0.7$ $0.5t_{CYCLE} - 0.5$ $0.5t_{CYCLE} - 0.5$ TBD	$0.5t_{CYCLE} + 0.7$ $0.5t_{CYCLE} + 0.5$ $0.5t_{CYCLE} + 0.5$ TBD	ns	
t_{PD}[1] SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1MΩ from RC1 to An V_{CC})		ns	See Note **2** and Figure 2 for Detailed Explanation
	133MHz 160MHz	–1.05 –0.9	–0.25 –0.10		
t_{CYCLE} (2x_Q Output)	Cycle–to–Cycle Variation 133MHz 160MHz	$t_{CYCLE} - 300ps$ $t_{CYCLE} - 300ps$	$t_{CYCLE} + 300ps$ $t_{CYCLE} + 300ps$		
t_{SKEWr}[3] (Rising) See Note **4**	Output–to–Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
t_{SKEWf}[3] (Falling)	Output–to–Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
$t_{SKEWall}$[3]	Output–to–Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
t_{LOCK}[4]	Time Required to Acquire Phase–Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL}[5]	Output Enable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
t_{PHZ},t_{PLZ}[5]	Output Disable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. T_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
2. The T_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
3. Under equally loaded conditions and at a fixed temperature and voltage.
4. With V_{CC} fully powered–on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1µF, t_{LOCK} minimum is with C1 = 0.01µF.
5. The t_{PZL}, t_{PHZ}, t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

Applications Information for All Versions

General AC Specification Notes

1. Several specifications can only be measured when the MC88915TFN55, 70 and 100 are in phase–locked operation. It is not possible to have the part in phase–lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88915TFN55, 70 and 100 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area, to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way all units passing the ATE test will meet or exceed the non–tested specifications limits.
2. These two specs ($t_{RISE/FALL}$ and t_{PULSE} Width 2X_Q output) guarantee that the MC88915T meets the 40MHz and 33MHz MC68040 P–Clock input specification (at 80MHz and 66MHz, respectively). For these two specs to be guaranteed by Motorola, the termination scheme shown below in Figure 1 must be used.
3. The wiring Diagrams and explanations in Figure 5 demonstrate the input and output frequency relationships for three possible feedback configurations. The allowable SYNC input range for each case is also indicated. There are two allowable SYNC frequency ranges, depending whether FREQ_SEL is high or low. Although not shown, it is possible to feed back the $\overline{Q5}$ output, thus creating a 180° phase shift between the SYNC input and the "Q" outputs. Table 1 below summarizes the allowable SYNC frequency range for each possible configuration.

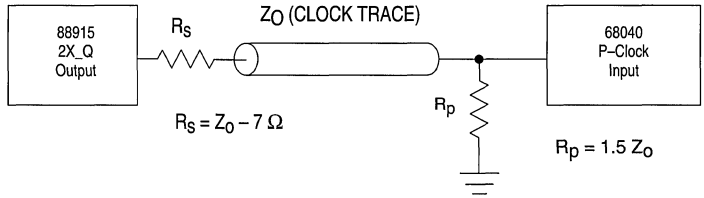
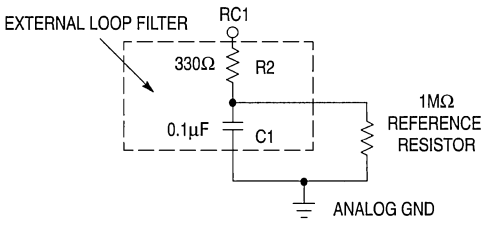


Figure 1. MC68040 P–Clock Input Termination Scheme

FREQ_SEL Level	Feedback Output	Allowable SYNC Input Frequency Range (MHZ)	Corresponding VCO Frequency Range	Phase Relationships of the "Q" Outputs to Rising SYNC Edge
HIGH	Q/2	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
HIGH	Any "Q" (Q0–Q4)	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	0°
HIGH	$\overline{Q5}$	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	180°
HIGH	2X_Q	20 to (2X_Q FMAX Spec)	20 to (2X_Q FMAX Spec)	0°
LOW	Q/2	2.5 to (2X_Q FMAX Spec)/8	20 to (2X_Q FMAX Spec)	0°
LOW	Any "Q" (Q0–Q4)	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
LOW	$\overline{Q5}$	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAXSpec)	180°
LOW	2X_Q	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAXSpec)	0°

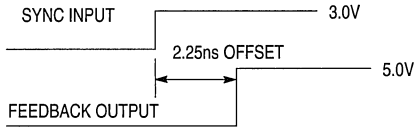
Table 1. Allowable SYNC Input Frequency Ranges for Different Feedback Configurations.

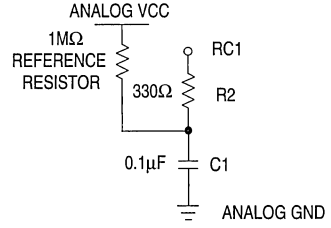
4. A 1MΩ resistor tied to either Analog V_{CC} or Analog GND as shown in Figure 2 is required to ensure no jitter is present on the MC88915T outputs. This technique causes a phase offset between the SYNC input and the output connected to the FEEDBACK input, measured at the input pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14 lots described in note 1 while the part was in phase–locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V – 2.0V) with the Q/2 output fed back. The phase measurements were made at 1.5V. The Q/2 output was terminated at the FEEDBACK input with 100Ω to V_{CC} and 100Ω to ground.



With the 1MΩ resistor tied in this fashion, the t_{PD} specification measured at the input pins is:

t_{PD} = 2.25ns ± 1.0ns





With the 1MΩ resistor tied in this fashion, the t_{PD} specification measured at the input pins is:

t_{PD} = −0.775ns ± 0.275ns

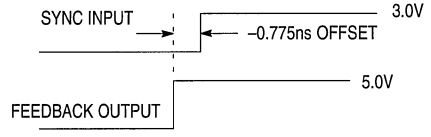


Figure 2. Depiction of the Fixed SYNC to Feedback Offset (tPD) Which is Present When a 1MΩ Resistor is Tied to VCC or Ground

5. The t_{SKEWr} specification guarantees that the rising edges of outputs Q/2, Q0, Q1, Q2, Q3, and Q4 will always fall within a 500ps window within one part. However, if the relative position of each output within this window is not specified, the 500 ps window must be added to each side of the tPD specification limits to calculate the total part–to–part skew. For this reason the absolute distribution of these outputs are provided in table 2. When taking the skew data, Q0 was used as a reference, so all measurements are relative to this output. The information in Table 2 is derived from measurements taken from the 14 process lots described in Note 1, over the temperature and voltage range.

Output	– (ps)	+ (ps)
Q0	0	0
Q1	–72	40
Q2	–44	276
Q3	–40	255
Q4	–274	–34
Q/2	–16	250
2X_Q	–633	–35

Table 2. Relative Positions of Outputs Q/2, Q0–Q4, 2X_Q, Within the 500ps t_{SKEWr} Spec Window

6. **Calculation of Total Output–to–Skew between multiple parts (Part–to–Part skew)**

   By combining the t_{PD} specification and the information in Note 5, the worst case output–to–output skew between multiple 88915's connected in parallel can be calculated. This calculation assumes that all parts have a common SYNC input clock with equal delay of that input signal to each part. This skew value is valid at the 88915 output pins only (equally loaded), it does not include PCB trace delays due to varying loads.

   With a 1MΩ resistor tied to analog V_{CC} as shown in note 4, the t_{PD} spec. limits between SYNC and the Q/2 output (connected to the FEEDBACK pin) are –1.05ns and –0.5ns. To calculate the skew of any given output between two or more parts, the absolute value of the distribution of that output given in table 2 must be subtracted and added to the lower and upper t_{PD} spec limits respectively. For output Q2, [276 – (–44)] = 320ps is the absolute value of the distribution. Therefore [–1.05ns – 0.32ns] = –1.37ns is the lower t_{PD} limit, and [–0.5ns + 0.32ns] = –0.18ns is the upper limit. Therefore the worst case skew of output Q2 between any number of parts is |(–1.37) – (–0.18)| = 1.19ns. Q2 has the worst case skew distribution of any output, so 1.2ns is the absolute worst case output–to–output skew between multiple parts.

7. Note 4 explains that the t_{PD} specification was measured and is guaranteed for the configuration of the Q/2 output connected to the FEEDBACK pin and the SYNC input running at 10MHz. The fixed offset (t_{PD}) as described above has some dependence on the input frequency and at what frequency the VCO is running. The graphs of Figure 3 demonstrate this dependence.

   The data presented in Figure 3 is from devices representing process extremes, and the measurements were also taken at the voltage extremes (V_{CC} = 5.25V and 4.75V). Therefore the data in Figure 3 is a realistic representation of the variation of t_{PD}.

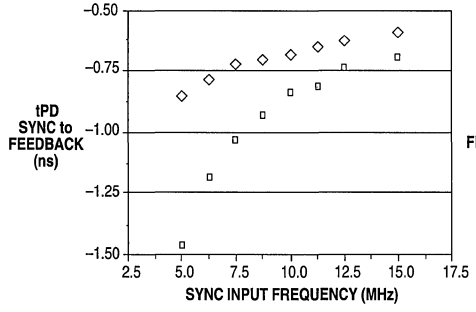


Figure 3a.

t_{PD} versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1MΩ Resistor Tied to Analog VCC)

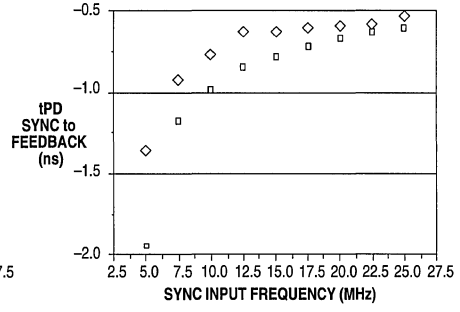


Figure 3b.

t_{PD} versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1MΩ Resistor Tied to Analog V_{CC})

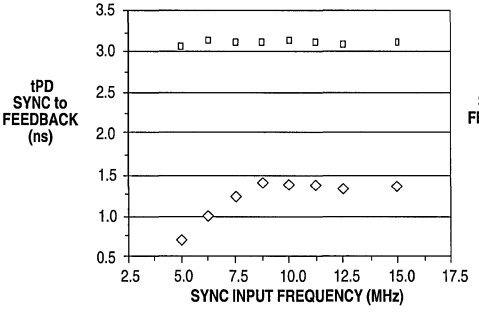


Figure 3c.

t_{PD} versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1MΩ Resistor Tied to Analog GND)

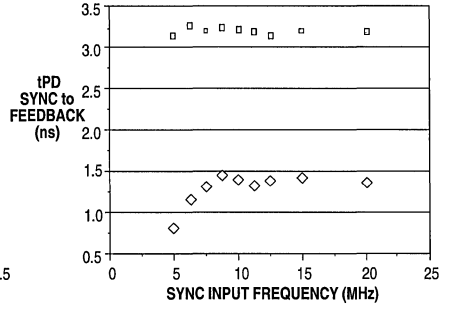


Figure 3d.

t_{PD} versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1MΩ Resistor Tied to Analog GND)

8. The lock indicator pin (LOCK) will reliably indicate a phase–locked condition at SYNC input frequencies down to 10MHz. At frequencies below 10MHz, the frequency of correction pulses going into the phase detector form the SYNC and FEEDBACK pins may not be sufficient to allow the lock indicator circuitry to accurately predict a phase–locked conditition. The MC88915T is guaranteed to provide stable phase–locked operation down to the appropriate minimum input frequency given in Table 1, even though the LOCK pin may be LOW at frequencies below 10MHZ. The exact minimum frequency where the lock indicator functionality can be guaranteed will be available when the MC88915T reaches 'MC' status.

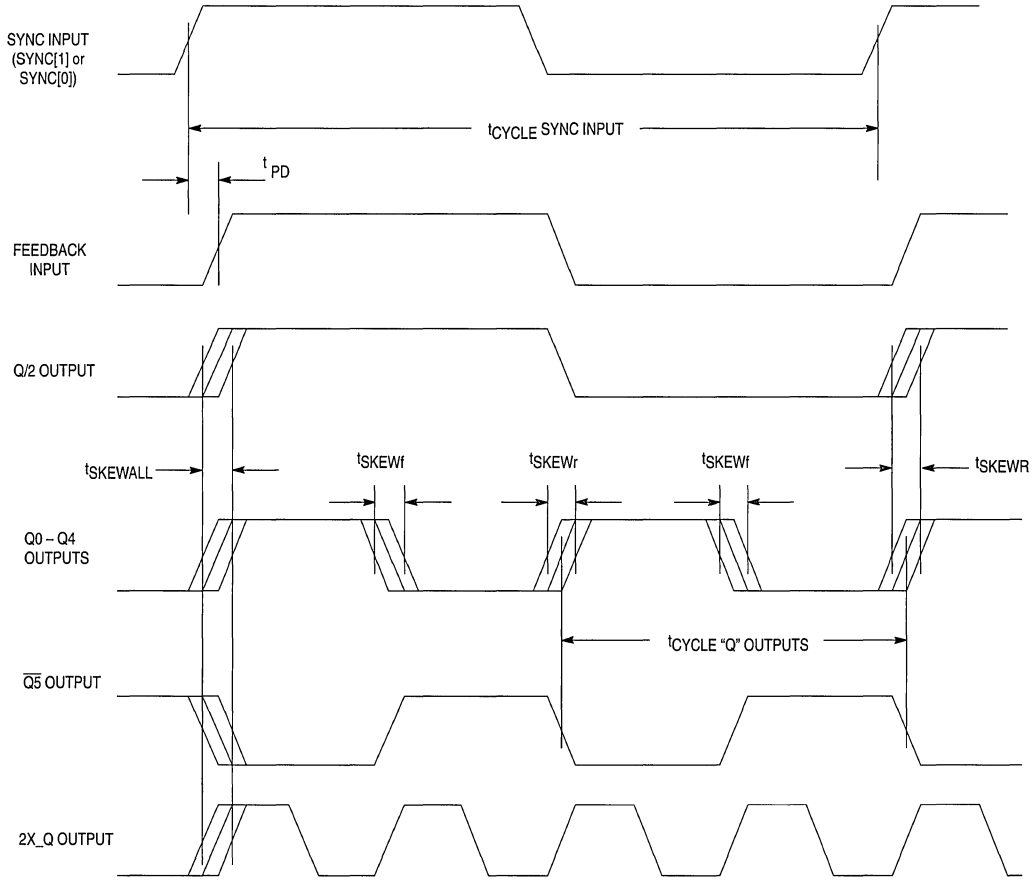
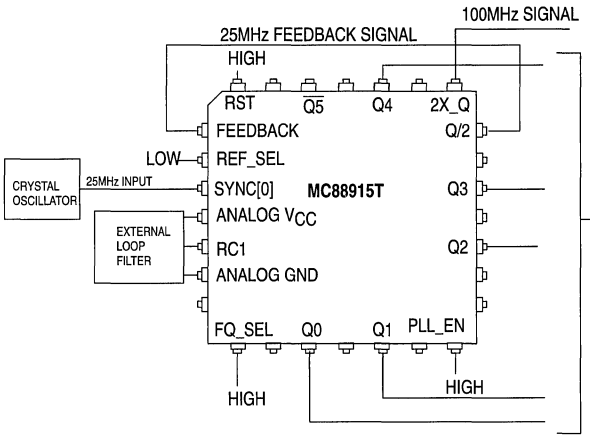


Figure 4. Output/Input Switching Waveforms and Timing Diagrams

(These waveforms represent the hook–up configuration of Figure 5a on page 182)

Timing Notes:

- The MC88915T aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
- All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges.All skews are specified as 'windows', not as a ± deviation around a center point.
- If a "Q" output is connected to the FEEDBACK input (this situation is not shown), the "Q" output frequency would match the SYNC input frequency, the 2X_Q output would run at twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency.



1:2 Input to "Q" Output Frequency Relationship

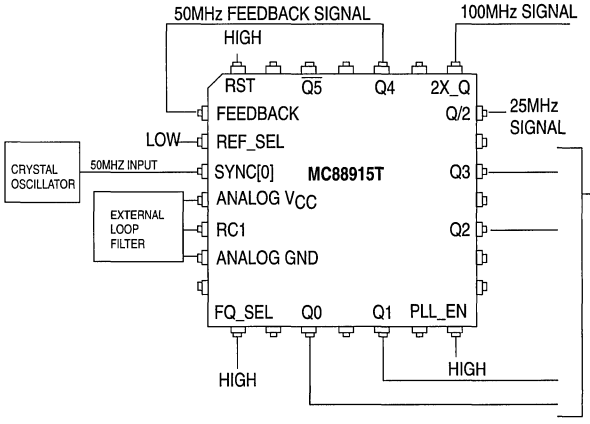
In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The "Q" outputs (Q0–Q4, $\overline{Q5}$) will always run at 2X the Q/2 frequency, and the 2X_Q output will run at 4X the Q/2 frequency.

Allowable Input Frequency Range:

5MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL HIGH)
2.5MHz to (2X_Q FMAX Spec)/8 (for FREQ_SEL LOW)

Note: If the $\overline{OE}/\overline{RST}$ input is active, a pull–up or pull–down resistor isn't necessary at the FEEDBACK pin so it won't when the fed back output goes into 3–state.

Figure 5a. Wiring Diagram and Frequency Relationships With Q/2 Output Feed Back



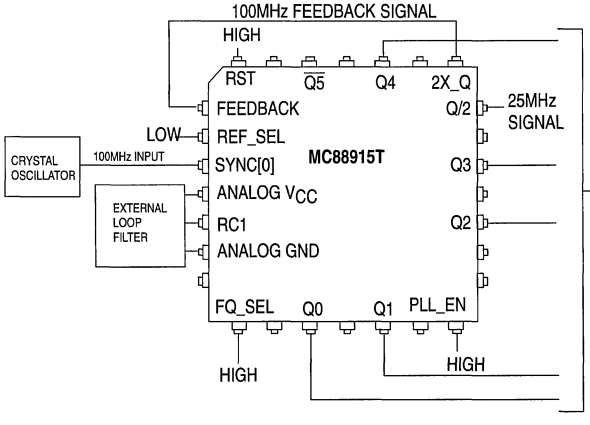
1:1 Input to "Q" Output Frequency Relationship

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the "Q" frequency, and the 2X_Q output will run at 2X the "Q" frequency.

Allowable Input Frequency Range:

10MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL HIGH)
5MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL LOW)

Figure 5b. Wiring Diagram and Frequency Relationships With Q4 Output Feed Back



2:1 Input to "Q" Output Frequency Relationship

In this application, the 2X_Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2X_Q and SYNC, thus the 2X_Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2X_Q frequency, and the "Q" outputs will run at 1/2 the 2X_Q frequency.

Allowable Input Frequency Range:

20MHz to (2X_Q FMAX Spec) (for FREQ_SEL HIGH)
10MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL LOW)

Figure 5c. Wiring Diagram and Frequency Relationships with 2X_Q Output Feed Back

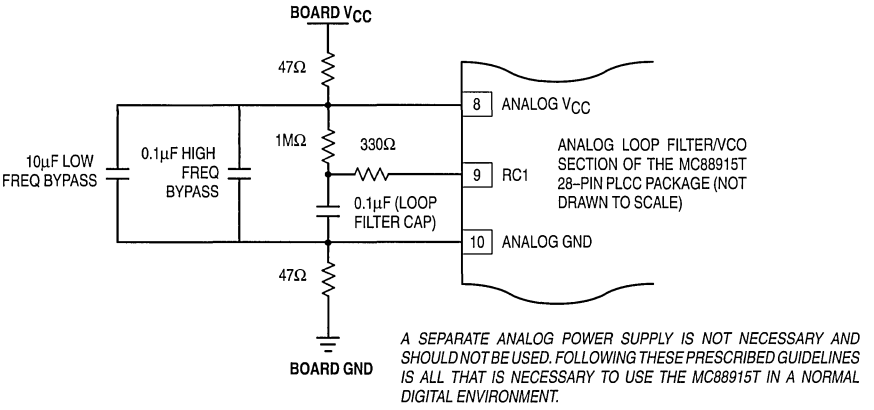


Figure 6. Recommended Loop Filter and Analog Isolation Scheme for the MC88915T

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 6 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88915T's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100pS phase deviation on the 88915T outputs. A 250mV step deviation on V_{CC} using the recommended filter values should cause no more than a 250pS phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step should cause no more than a 100pS phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88915T's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 6 is to give the 88915T additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (1MΩ and 330Ω). The loop filter capacitor (0.1μF) can be a ceramic chip capacitior, the same as a standard bypass capacitor.

1d. The 1M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 1MΩ resistor provides the correct amount of current injection into the charge pump (2–3μA). For the TFN55, 70 or 100, if the VCO is running below 40MHz, a 1.5MΩ reference resistor should be used (instead of 1MΩ).

2. In addition to the bypass capacitors used in the analog filter of Figure 6, there should be a 0.1μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88915T outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88915T package as possible.

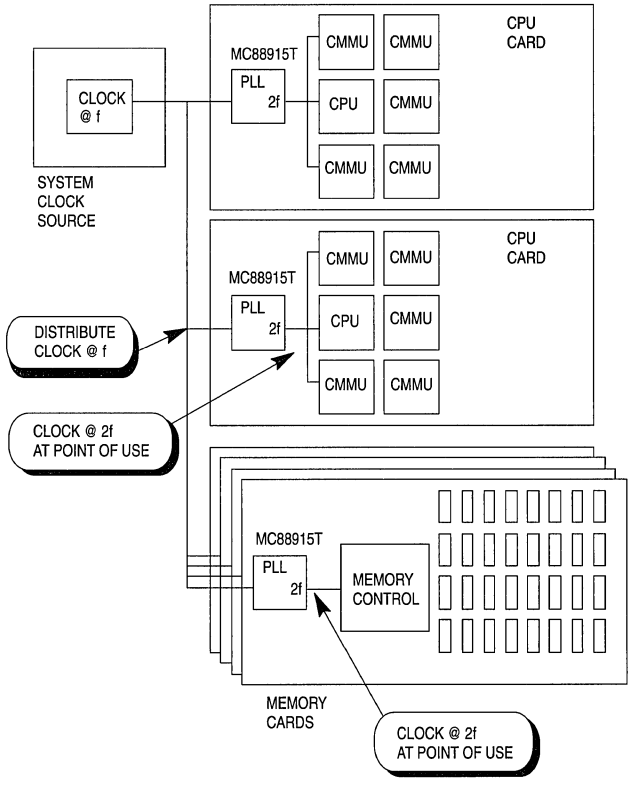


Figure 7. Representation of a Potential Multi–Processing Application Utilizing the MC88915T for Frequency Multiplication and Low Board–to–Board Skew

MC88915T System Level Testing Functionality

3–state functionality has been added to the 100MHz version of the MC88915T to ease system board testing. Bringing the $\overline{OE}/\overline{RST}$ pin low will put all outputs (except for LOCK) into the high impedance state. As long as the PLL_EN pin is low, the Q0–Q4, Q5, and the Q/2 outputs will remain reset in the low state after the $\overline{OE}/\overline{RST}$ until a falling SYNC edge is seen. The 2X_Q output will be the inverse of the SYNC signal in this mode. If the 3–state functionality will be used, a pull–up or pull–down resistor must be tied to the FEEDBACK input pin to prevent it from floating when the fedback output goes into high impedance.

With the PLL_EN pin low the selected SYNC signal is gated directly into the internal clock distribution network, bypassing and disabling the VCO. In this mode the outputs are directly driven by the SYNC input (per the block diagram). This mode can also be used for low frequency board testing.

Note: If the outputs are put into 3–state during normal PLL operation, the loop will be broken and phase–lock will be lost. It will take a maximum of 10mS (tLOCK spec) to regain phase–lock after the $\overline{OE}/\overline{RST}$ pin goes back high.

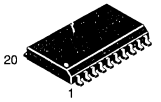
Low Skew CMOS PLL Clock Driver With Processor Reset

MC88916

LOW SKEW CMOS PLL CLOCK DRIVER WITH PROCESSOR RESET

The MC88916 Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for CISC microprocessor or single processor RISC systems. The $\overline{RST\_IN}/\overline{RST\_OUT}$(LOCK) pins provide a processor reset function designed specifically for the MC68/EC/LC030/040 microprocessor family. The 88916 comes in two speed grades: 70 and 80MHz. These frequencies correspond to the 2X_Q maximum output frequency. The two grades should be ordered as the MC88916DW70 and MC88916DW80, respectively.

- Provides Performance Required to Drive 68030 Microprocessor Family as well as the 33 and 40MHz 68040 Microprocessors
- Three Outputs (Q0–Q2) With Output–Output Skew <500ps and Six Outputs Total (Q0–Q2, $\overline{Q3}$, 2X_Q,) With <1ns Skew Each Being Phase and Frequency Locked to the SYNC Input
- The Phase Variation From Part–to–Part Between SYNC and the 'Q' Outputs Is Less Than 600ps (Derived From the T_{PD} Specification, Which Defines the Part–to–Part Skew)
- SYNC Input Frequency Range From 5MHZ to 2X_Q $F_{Max}/4$
- Additional Outputs Available at 2X and ÷2 the System 'Q' Frequency. Also a $\overline{Q}$ (180° Phase Shift) Output Available.
- All Outputs Have ±36mA Drive (Equal High and Low) CMOS Levels. Can Drive Either CMOS or TTL Inputs. All Inputs Are TTL–Level Compatible
- Test Mode Pin (PLL_EN) Provided for Low Frequency Testing



DW SUFFIX
SOIC PACKAGE
CASE 751D–04

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple locations on a board. The PLL also allows the MC88916 to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency.

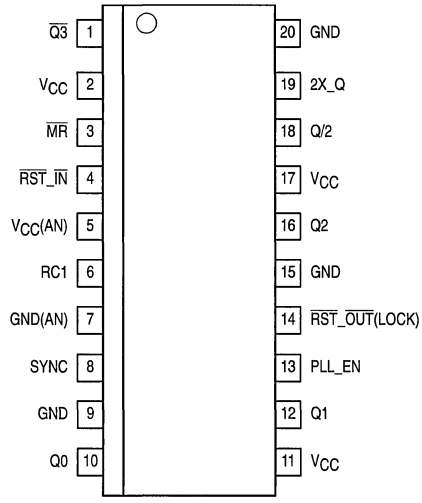
Three 'Q' outputs (Q0–Q2) are provided with less than 500ps skew between their rising edges. The $\overline{Q3}$ output is inverted (180° phase shift) from the 'Q' outputs. A 2X_Q output runs at twice the 'Q' output frequency. The 2X_Q output does not meet the stringent duty cycle requirement of the 20 and 25Mhz 68040 microprocessor PCLK input. The 88920 has been designed specifically to provide the 68040 PCLK and BCLK inputs for the low frequency 68040 microprocessor. 68040 designers should refer to the 88920 data sheet for more details. For the 33 and 40MHz 68040, the 2X_Q output will meet the duty cycle requirements of the PCLK input. The Q/2 output runs at 1/2 the 'Q' frequency. This output is fed back internally, providing a fixed 2X multiplication from the 'Q' outputs to the SYNC input. Since the feedback is done internally (no external feedback pin is provided) the input/output frequency relationships are fixed.

In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88916 in a static 'test mode'. In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment.

The $\overline{RST\_OUT}$(LOCK) pin doubles as a phase–lock indicator. When the $\overline{RST\_IN}$ pin is held high, the open drain $\overline{RST\_OUT}$ pin will be pulled actively low until phase–lock is achieved. When phase–lock occurs, the $\overline{RST\_OUT}$(LOCK) is released and a pull–up resistor will pull the signal high. To give a processor reset signal, the $\overline{RST\_IN}$ pin is toggled low, and the $\overline{RST\_OUT}$(LOCK) pin will stay low for 1024 cycles of the 'Q' output frequency after the RST_IN pin is brought back high.

Description of the $\overline{RST\_IN}/\overline{RST\_OUT}$(LOCK) Functionality

The $\overline{RST\_IN}$ and $\overline{RST\_OUT}$(LOCK) pins provide a 68030/040 processor reset function, with the $\overline{RST\_OUT}$ pin also acting as a lock indicator. If the $\overline{RST\_IN}$ pin is held high during system power–up, the $\overline{RST\_OUT}$ pin will be in the low state until steady state phase/frequency lock to the input reference is achieved. 1024 'Q' output cycles after phase–lock is achieved the $\overline{RST\_OUT}$(LOCK) pin will go into a high impedance state, allowing it to be pulled high by an external pull–up resistor (see the AC/DC specs for the characteristics of the $\overline{RST\_OUT}$(LOCK) pin). If the $\overline{RST\_IN}$ pin is held low during power–up, the $\overline{RST\_OUT}$(LOCK) pin will remain low.



Pinout: 20–Lead Wide SOIC Package (Top View)

Description of the RST_IN/RST_OUT(LOCK) Functionality (continued)

After the system start–up is complete and the 88916 is phase–locked to the SYNC input signal (RST_OUT high), the processor reset functionality can be utilized. When the RST_IN pin is toggled low (min. pulse width=10nS), RST_OUT(LOCK) will go to the low state and remain there for 1024 cycles of the 'Q' output frequency (512 SYNC cycles). During the time in which the RST_OUT(LOCK) is actively pulled low, all the 88916 clock outputs will continue operating correctly and in a locked condition to the SYNC input (clock signals to the 68030/040 family of processors must continue while the processor is in reset). A propagation delay after the 1024th cycle RST_OUT(LOCK) goes back to the high impedance state to be pulled high by the resistor.

Power Supply Ramp Rate Restriction for Correct 68030 Processor Reset Operation During System Start–up

Because the RST_OUT(LOCK) pin is an indicator of phase–lock to the reference source, some constraints must be placed on the power supply ramp rate to make sure the RST_OUT(LOCK) signal holds the processor in reset during system start–up (power–up). With the recommended loop filter values (see Figure 7) the lock time is approximately 10ms. The phase–lock loop will begin attempting to lock to a reference source (if it is present) when VCC reaches 2V. If the V_{CC} ramp rate is significantly slower than 10ms, then the PLL could lock to the reference source, causing RST_OUT(LOCK) to go high before the 88916 and 68030 processor is fully powered up, violating the processor reset specification. Therefore, if it is necessary for the RST_IN pin to be held high during power–up, the V_{CC} ramp rate must be less than 10mS for proper 68030/040 reset operation.

This ramp rate restriction can be ignored if the RST_IN pin can be held low during system start–up (which holds RST_OUT low). The RST_OUT(LOCK) pin will then be pulled back high 1024 cycles after the RST_IN pin goes high.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0V
PD_1	Power Dissipation at 33MHz With 50Ω Thevenin Termination	15mW/Output 90mW/Device	mW	V_{CC} = 5.0V T = 25°C
PD_2	Power Dissipation at 33MHz With 50Ω Parallel Termination to GND	37.5mW/Output 225mW/Device	mW	V_{CC} = 5.0V T = 25°C

MAXIMUM RATINGS*

Symbol	Parameter	Limits	Unit
V_{CC}, AV_{CC}	DC Supply Voltage Referenced to GND	–0.5 to 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, Per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, Per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current Per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	5.0 ±10%	V
V_{in}	DC Input Voltage	0 to V_{CC}	V
V_{out}	DC Output Voltage	0 to V_{CC}	V
T_A	Ambient Operating Temperature	–40 to 85	°C
ESD	Static Discharge Voltage	> 1500	V

DC CHARACTERISTICS (T_A = –40°C to +85°C; V_{CC} = 5.0V ± 5%)

Symbol	Parameter	V_{CC}	Guaranteed Limits	Unit	Condition
V_{IH}	Minimum High Level Input Voltage	4.75 5.25	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{IL}	Minimum Low Level Input Voltage	4.75 5.25	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{OH}	Minimum High Level Output Voltage	4.75 5.25	4.01 4.51	V	V_{IN} = V_{IH} or V_{IL} I_{OH} –36mA –36mA
V_{OL}	Minimum Low Level Output Voltage	4.75 5.25	0.44 0.44	V	V_{IN} = V_{IH} or V_{IL} I_{OH} +36mA[1] +36mA
I_{IN}	Maximum Input Leakage Current	5.25	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.25	2.0 [2]	mA	V_I = V_{CC} – 2.1V
I_{OLD}	Minimum Dynamic[3] Output Current	5.25	88	mA	V_{OLD} = 1.0V Max
I_{OHD}		5.25	–88	mA	V_{OHD} = 3.85 Min
I_{CC}	Maximum Quiescent Supply Current	5.25	750	µA	V_I = V_{CC}, GND

1. I_{OL} is +12mA for the $\overline{RST\_OUT}$ output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration 2.0ms, one output loaded at a time.

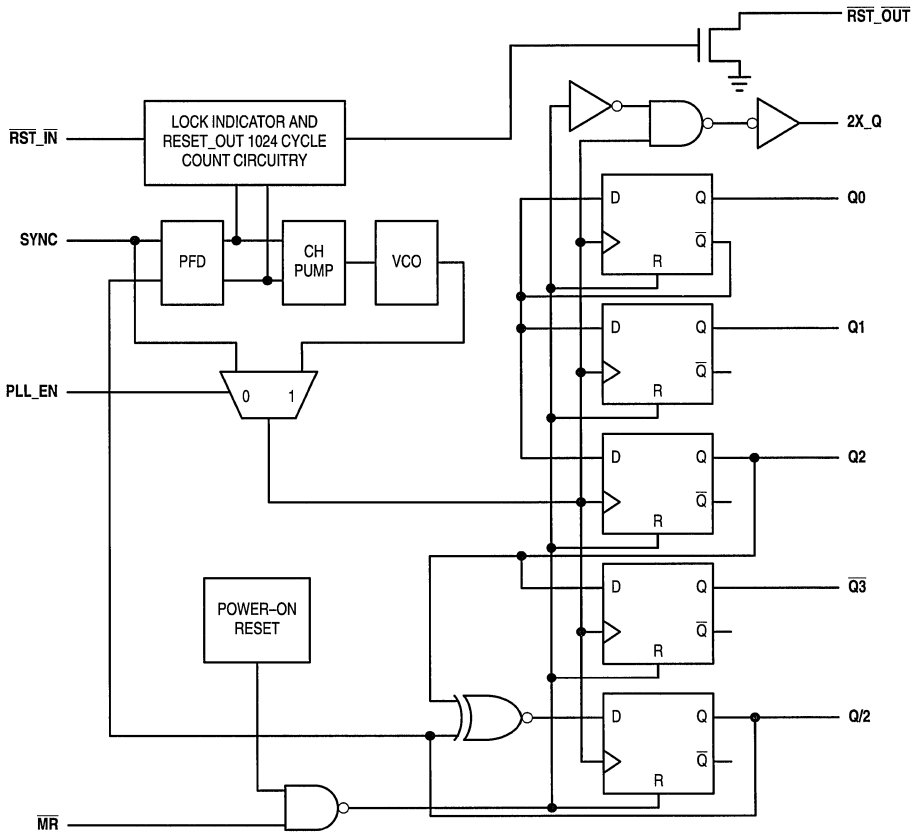


Figure 1. MC88916 Logic Block Diagram

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum		Maximum	Unit
$t_{RISE/FALL}$ SYNC Input	Rise/Fall Time, SYNC Input From 0.8V to 2.0V	—		5.0	ns
t_{CYCLE},	Input Clock Period	'DW70	'DW80		
SYNC Input	SYNC Input	57	50	200	ns
Duty Cycle	Duty Cycle, SYNC Input	50% ± 25%			

FREQUENCY SPECIFICATIONS (T_A = –40°C to +85°C; V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Guaranteed Minimum		Unit
		MC88916DW70	MC88916DW80	
Fmax (2X_Q)	Maximum Operating Frequency, 2X_Q Output	70	80	MHz
Fmax ('Q')	Maximum Operating Frequency, Q0–Q2, $\overline{Q3}$ Outputs	35	40	MHz

1. Maximum Operating Frequency is guaranteed with the 88916 in a phase–locked condition, and all outputs loaded at 50Ω terminated to $V_{CC}/2$.

AC CHARACTERISTICS (T_A = –40°C to +85°C; V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Mimimum	Maximum	Unit	Condition
$t_{RISE/FALL}$[1] All Outputs	Rise/Fall Time, All Outputs into a 50Ω Load	0.3	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{RISE/FALL}$[1] 2X_Q Output	Rise/Fall Time into a 20pF Load, With Termination Specified in AppNote 3	0.5	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{pulse\ width(a)}$[1] (Q0, Q1, Q2, $\overline{Q3}$)	Output Pulse Width Q0, Q1, Q2, $\overline{Q3}$ at $V_{CC}/2$	$0.5t_{cycle}$ – 0.5	$0.5t_{cycle}$ + 0.5	ns	50Ω Load Terminated to $V_{CC}/2$ (See App Note 3)
$t_{pulse\ width(b)}$[1] (2X_Q Output)	Output Pulse Width 2X_Q at $V_{CC}/2$ 40–49MHz 50–65MHz 66–80MHz	$0.5t_{cycle}$ – 1.5[5] $0.5t_{cycle}$ – 1.0[5] $0.5t_{cycle}$ – 0.5	$0.5t_{cycle}$ + 1.5[5] $0.5t_{cycle}$ + 1.0[5] $0.5t_{cycle}$ + 0.5	ns	50Ω Load Terminated to $V_{CC}/2$ (See App Note 3)
t_{PD}[1,4] SYNC – Q/2	SYNC Input to Q/2 Output Delay (Measured at SYNC and Q/2 Pins)	–0.75	–0.15	ns	With 1MΩ From RC1 to An V_{CC} (See Application Note 2)
		+1.25[7]	+3.25[7]	ns	With 1MΩ From RC1 to An GND (See Application Note 2)
t_{SKEWr}[1,2] (Rising)	Output–to–Output Skew Between Outputs Q0–Q2, Q/2 (Rising Edge Only)	—	500	ps	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
t_{SKEWf}[1,2] (Falling)	Output–to–Output Skew Between Outputs Q0–Q2 (Falling Edge Only)	—	1.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
$t_{SKEWall}$[1,2]	Output–to–Output Skew 2X_Q, Q/2, Q0–Q2 Rising $\overline{Q3}$ Falling	—	1.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
t_{LOCK}[3]	Phase–Lock Acquisition Time, All Outputs to SYNC Input	1	10	ms	
t_{PHL} $\overline{MR}$ – Q	Propagation Delay, $\overline{MR}$ to Any Output (High–Low)	1.5	13.5	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
t_{REC}, $\overline{MR}$ to SYNC[6]	Reset Recovery Time rising $\overline{MR}$ edge to falling SYNC edge	9	—	ns	
t_W, $\overline{MR}$ LOW[6]	Minimum Pulse Width, $\overline{MR}$ input Low	5	—	ns	
t_W, $\overline{RST\_IN}$ LOW	Minimum Pulse Width, $\overline{RST\_IN}$ Low	10	—	ns	When in Phase–Lock
t_{PZL}	Output Enable Time $\overline{RST\_IN}$ Low to $\overline{RST\_OUT}$ Low	1.5	16.5	ns	See Application Note 5
t_{PLZ}	Output Enable Time $\overline{RST\_IN}$ High to $\overline{RST\_OUT}$ High Z	1016 'Q' Cycles (508 Q/2 Cycles)	1024 'Q' Cycles (512 Q/2 Cycles)	ns	See Application Note 5

1. These specifications are not tested, they are guaranteed by statistical characterization. See Application Note 1 for a discussion of this methodology.
2. Under equally loaded conditions and at a fixed temperature and voltage.
3. With V_{CC} fully powered–on: t_{CLOCK} Max is with C1 = 0.1μF; t_{LOCK} Min is with C1 = 0.01μF.
4. See Application Note 4 for the distribution in time of each output referenced to SYNC.
5. Limits do not meet requirements of the 68040 microprocessor. Refer to the 88920 for a low frequency 68040 clock driver.
6. Specification is valid only when the PLL_EN pin is low.
7. This is a typical specification only, worst case guarantees are not provided.

Application Notes

1. Several specifications can only be measured when the MC88916 is in phase–locked operation. It is not possible to have the part in phase–lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88916 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area. IC performance to each specification and fab variation were used to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way, all units passing the ATE test will meet or exceed the non–tested specifications limits.
2. A 1MΩ resistor tied to either Analog V_{CC} or Analog GND, as shown in Figure 2, is required to ensure no jitter is present on the MC88916 outputs. This technique causes a phase offset between the SYNC input and the Q0 output, measured at the pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14 lots described in note 1 while the part was in phase–locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V to 2.0V). The phase measurements were made at 1.5V. See Figure 2 for a graphical description.
3. The pulse width spec for the Q and 2Q_X outputs is referenced to a $V_{CC}/2$ threshold. To translate this down to a 1.5V reference with the same pulse width tolerance, the termination scheme pictured in Figure 3 must be used. This termination scheme is required to drive the PCLK input of the 68040 microprocessor with the 88916 outputs.
4. The t_{PD} spec (SYNC to Q/2) guarantees how close the Q/2 output will be locked to the reference input connected to the SYNC input (including temperature and voltage variation). This also tells what the skew from the Q/2 output on one part connected to a given reference input, to the Q/2 output on one or more parts connected to that reference input (assuming equal delay from the reference input to the SYNC input of each part). Therefore the t_{PD} spec is equivalent to a part–to–part specification. However, to correctly predict the skew from a given output on one part to any other output on one or more other parts, the distribution of each output in relation to the SYNC input must be known. This distribution for the MC88916 is provided in Table 1.

TABLE 1. Distribution of Each Output versus SYNC

Output	–(ps)	+(ps)
2X_Q	TBD	TBD
Q0	TBD	TBD
Q1	TBD	TBD
Q2	TBD	TBD
$\overline{Q3}$	TBD	TBD
Q/2	TBD	TBD

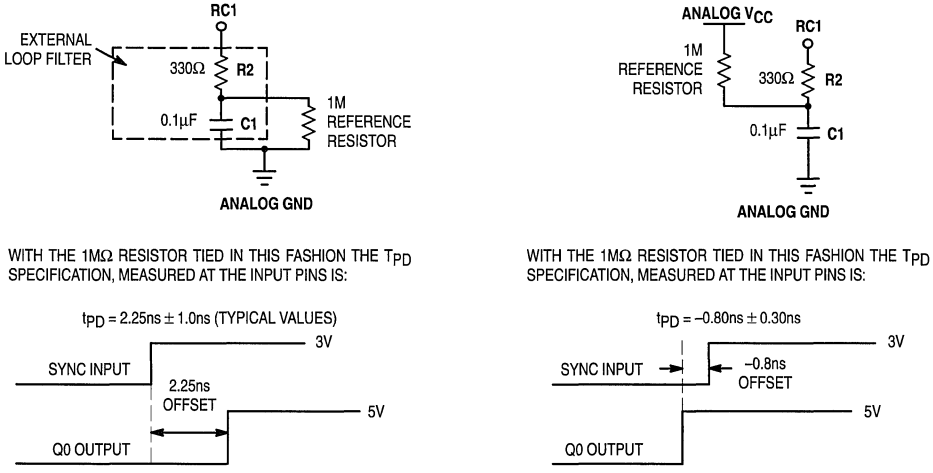


Figure 2. Depiction of the Fixed SYNC to Q0 Offset (t_{PD}) Which Is Present When a 1MΩ Resistor Is Tied to V_{CC} or Ground

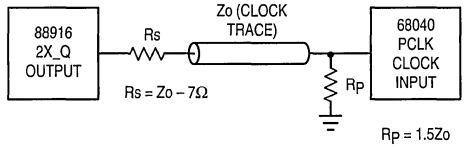


Figure 3. MC68040 PCLK Input Termination Scheme

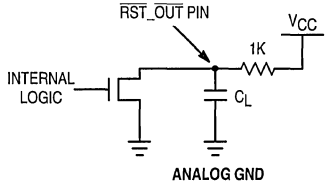


Figure 4. RST_OUT Test Circuit

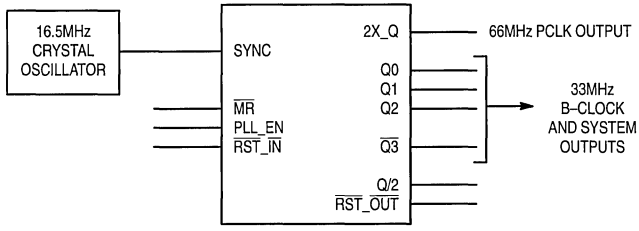


Figure 5. Logical Representation of the MC88916 With Input/Output Frequency Relationships

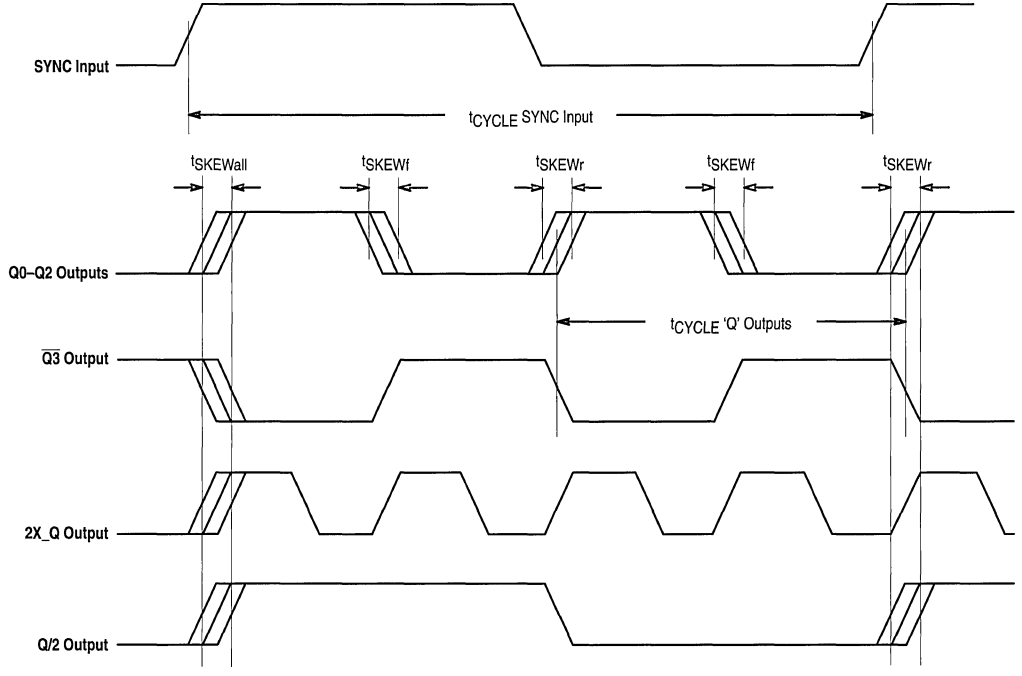


Figure 6. Output/Input Switching Waveforms and Timing Relationships

Timing Notes

1. The MC88916 aligns rising edges of the outputs and the SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges. All skews are specified as 'windows', not as a ± deviation around a center point.

The t_{PD} spec includes the full temperature range from 0°C to 70°C and the full V_{CC} range from 4.75V to 5.25V. If the ΔT and ΔV_{CC} in a given system are less than the specification limits, the t_{PD} spec window will be reduced. The t_{PD} window for a given ΔT and ΔV_{CC} is given by the following regression formula:

TBD

5. The $\overline{RST}\_\overline{OUT}$ pin is an open drain N–Channel output. Therefore an external pull–up resistor must be provide to pull up the $\overline{RST}\_\overline{OUT}$ pin when it goes into the high impedance state (after the MC88916 is phase–locked to the reference input with $\overline{RST}\_\overline{IN}$ held high or 1024 'Q' cycles after the $\overline{RST}\_\overline{IN}$ pin goes high when the part is locked). In the t_{PLZ} and t_{PZL} specifications, a 1KΩ resistor is used as a pull–up as shown in Figure 4.

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 7 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will make the 88916 PLL insensitive to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100ps phase deviation on the 88916 outputs. A 250mV step deviation on V_{CC} using the recommended filter values will cause no more than a 250ps phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step will cause no more than a 100ps phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88916's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 7 is to give the 88916 additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (1M and 330Ω). The loop filter capacitor (0.1uF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 1M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 1M resistor provides the correct amount of current injection into the charge pump (2–3μA). If the VCO is running below 40MHz, a 1.5MΩ reference resistor should be used.

2. In addition to the bypass capacitors used in the analog filter of Figure 7, there should be a 0.1μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88916 outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88916 package as possible.

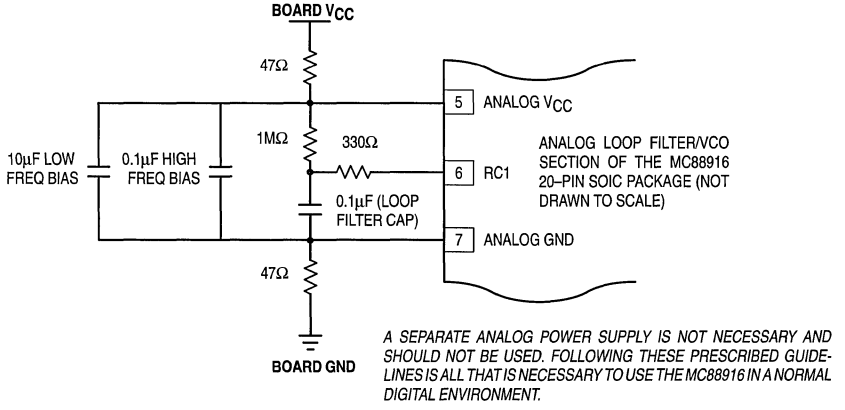


Figure 7. Recommended Loop Filter and Analog Isolation Scheme for the MC88916

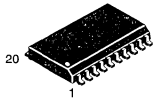
Low Skew CMOS PLL Clock Driver
With Power-Down/Power-Up Feature

MC88920

LOW SKEW CMOS PLL CLOCK DRIVER With Power–Down/ Power–Up Feature

The MC88920 Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for CISC microprocessor or single processor RISC systems. The $\overline{RST}$_IN/$\overline{RST}$_$\overline{OUT}$(LOCK) pins provide a processor reset function designed specifically for the MC68/EC/LC030/040 microprocessor family.

The PLL allows the the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple locations on a board. The PLL also allows the MC88920 to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency.



DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04

- 2X_Q Output Meets All Requirements of the 20 and 25MHz 68040 Microprocessor PCLK Input Specifications
- Three Outputs (Q0–Q2) With Output–Output Skew <500ps and Six Outputs Total (Q0–Q2, $\overline{Q3}$, 2X_Q,) With <1ns Skew Each Being Phase and Frequency Locked to the SYNC Input
- The Phase Variation From Part–to–Part Between SYNC and the 'Q' Outputs Is Less Than 600ps (Derived From the T_{PD} Specification, Which Defines the Part–to–Part Skew)
- SYNC Input Frequency Range From 5MHZ to 2X_Q F_{Max}/4
- Additional Outputs Available at 2X and ÷2 the System 'Q' Frequency. Also a $\overline{Q}$ (180° Phase Shift) Output Available.
- All Outputs Have ±36mA Drive (Equal High and Low) CMOS Levels. Can Drive Either CMOS or TTL Inputs. All Inputs Are TTL–Level Compatible
- Test Mode Pin (PLL_EN) Provided for Low Frequency Testing
- Special Power–Down Mode With 2X_Q, Q0, and Q1 Being Reset (With $\overline{MR}$), and Other Outputs Remain Running. 2X_Q, Q0 and Q1 Are Guaranteed to Be in Lock 3 Clock Cycles After $\overline{MR}$ Is Negated

Three 'Q' outputs (Q0–Q2) are provided with less than 500ps skew between their rising edges. The $\overline{Q3}$ output is inverted (180° phase shift) from the 'Q' outputs. A 2X_Q output runs at twice the 'Q' output frequency. The 2X_Q output is ideal for 68040 systems which require a 2X processor clock input, and it meets the tight duty cycle spec of the 20 and 25MHz 68040. The Q/2 output runs at 1/2 the 'Q' frequency. This output is fed back internally, providing a fixed 2X multiplication from the 'Q' outputs to the SYNC input. Since the feedback is done internally (no external feedback pin is provided) the input/output frequency relationships are fixed.

In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88920 in a static 'test mode'. In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment.

The $\overline{RST}$_$\overline{OUT}$(LOCK) pin doubles as a phase–lock indicator. When the $\overline{RST}$_IN pin is held high, the open drain $\overline{RST}$_$\overline{OUT}$ pin will be pulled actively low until phase–lock is achieved. When phase–lock occurs, the $\overline{RST}$_$\overline{OUT}$(LOCK) is released and a pull–up resistor will pull the signal high. To give a processor reset signal, the $\overline{RST}$_IN pin is toggled low, and the $\overline{RST}$_$\overline{OUT}$(LOCK) pin will stay low for 1024 cycles of the 'Q' output frequency after the RST_IN pin is brought back high.

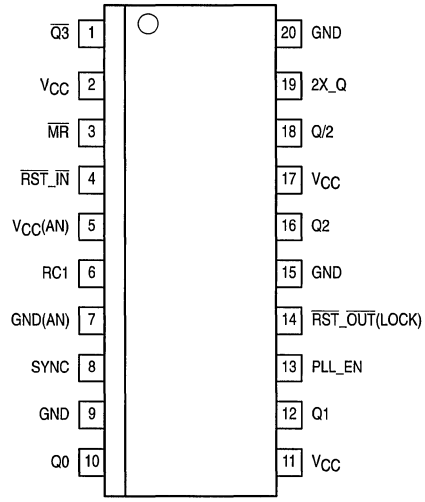
Description of the $\overline{RST}$_IN/$\overline{RST}$_$\overline{OUT}$(LOCK) Functionality

The $\overline{RST}$_IN and $\overline{RST}$_$\overline{OUT}$(LOCK) pins provide a 68030/040 processor reset function, with the $\overline{RST}$_$\overline{OUT}$ pin also acting as a lock indicator. If the $\overline{RST}$_IN pin is held high during system power–up, the $\overline{RST}$_$\overline{OUT}$ pin will be in the low state until steady state phase/frequency lock to the input reference is achieved. 1024 'Q' output cycles after phase–lock is achieved the $\overline{RST}$_$\overline{OUT}$(LOCK) pin will go into a high impedance state, allowing it to be pulled high by an external pull–up resistor (see the AC/DC specs for the characteristics of the $\overline{RST}$_$\overline{OUT}$(LOCK) pin). If the $\overline{RST}$_IN pin is held low during power–up, the $\overline{RST}$_$\overline{OUT}$(LOCK) pin will remain low.

Power–Down Mode Functionality

The MC88920 has a special feature designed in to allow the processor clock inputs to be reset for total processor power–down, and then to return to phase–locked operation very quickly when the processor is powered–up again.

The $\overline{MR}$ pin resets outputs 2X_Q, Q0 and Q1 only leaving the other outputs operational for other system activity. When $\overline{MR}$ is negated, all outputs will be operating normally within 3 clock cycles.



Pinout: 20–Lead Wide SOIC Package (Top View)

Description of the $\overline{RST\_IN}$/$\overline{RST\_OUT}$(LOCK) Functionality (continued)

After the system start–up is complete and the 88920 is phase–locked to the SYNC input signal ($\overline{RST\_OUT}$ high), the processor reset functionality can be utilized. When the $\overline{RST\_IN}$ pin is toggled low (min. pulse width=10nS), $\overline{RST\_OUT}$(LOCK) will go to the low state and remain there for 1024 cycles of the 'Q' output frequency (512 SYNC cycles). During the time in which the $\overline{RST\_OUT}$(LOCK) is actively pulled low, all the 88920 clock outputs will continue operating correctly and in a locked condition to the SYNC input (clock signals to the 68030/040 family of processors must continue while the processor is in reset). A propagation delay after the 1024th cycle $\overline{RST\_OUT}$(LOCK) goes back to the high impedance state to be pulled high by the resistor.

Power Supply Ramp Rate Restriction for Correct 030/040 Processor Reset Operation During System Start–up

Because the $\overline{RST\_OUT}$(LOCK) pin is an indicator of phase–lock to the reference source, some constraints must be placed on the power supply ramp rate to make sure the $\overline{RST\_OUT}$(LOCK) signal holds the processor in reset during system start–up (power–up). With the recommended loop filter values (see Figure 7) the lock time is approximately 10ms. The phase–lock loop will begin attempting to lock to a reference source (if it is present) when VCC reaches 2V. If the V_{CC} ramp rate is significantly slower than 10ms, then the PLL could lock to the reference source, causing $\overline{RST\_OUT}$(LOCK) to go high before the 88920 and '030/040 processor is fully powered up, violating the processor reset specification. Therefore, if it is necessary for the $\overline{RST\_IN}$ pin to be held high during power–up, the V_{CC} ramp rate must be less than 10mS for proper '030/040 reset operation.

This ramp rate restriction can be ignored if the $\overline{RST\_IN}$ pin can be held low during system start–up (which holds $\overline{RST\_OUT}$ low). The $\overline{RST\_OUT}$(LOCK) pin will then be pulled back high 1024 cycles after the $\overline{RST\_IN}$ pin goes high.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0V
PD_1	Power Dissipation at 33MHz With 50Ω Thevenin Termination	15mW/Output 90mW/Device	mW	V_{CC} = 5.0V T = 25°C
PD_2	Power Dissipation at 33MHz With 50Ω Parallel Termination to GND	37.5mW/Output 225mW/Device	mW	V_{CC} = 5.0V T = 25°C

MAXIMUM RATINGS*

Symbol	Parameter	Limits	Unit
V_{CC}, AV_{CC}	DC Supply Voltage Referenced to GND	–0.5 to 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, Per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, Per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current Per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	5.0 ±10%	V
V_{in}	DC Input Voltage	0 to V_{CC}	V
V_{out}	DC Output Voltage	0 to V_{CC}	V
T_A	Ambient Operating Temperature	0 to 70	°C
ESD	Static Discharge Voltage	> 1500	V

DC CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5.0V ± 5%)

Symbol	Parameter	V_{CC}	Guaranteed Limits	Unit	Condition
V_{IH}	Minimum High Level Input Voltage	4.75 5.25	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{IL}	Minimum Low Level Input Voltage	4.75 5.25	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{OH}	Minimum High Level Output Voltage	4.75 5.25	4.01 4.51	V	V_{IN} = V_{IH} or V_{IL} I_{OH} –36mA –36mA
V_{OL}	Minimum Low Level Output Voltage	4.75 5.25	0.44 0.44	V	V_{IN} = V_{IH} or V_{IL} I_{OH} +36mA[1] +36mA
I_{IN}	Maximum Input Leakage Current	5.25	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.25	2.0 [2]	mA	V_I = V_{CC} – 2.1V
I_{OLD}	Minimum Dynamic[3] Output Current	5.25	88	mA	V_{OLD} = 1.0V Max
I_{OHD}		5.25	–88	mA	V_{OHD} = 3.85 Min
I_{CC}	Maximum Quiescent Supply Current	5.25	750	µA	V_I = V_{CC}, GND

1. I_{OL} is +12mA for the $\overline{RST\_OUT}$ output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration 2.0ms, one output loaded at a time.

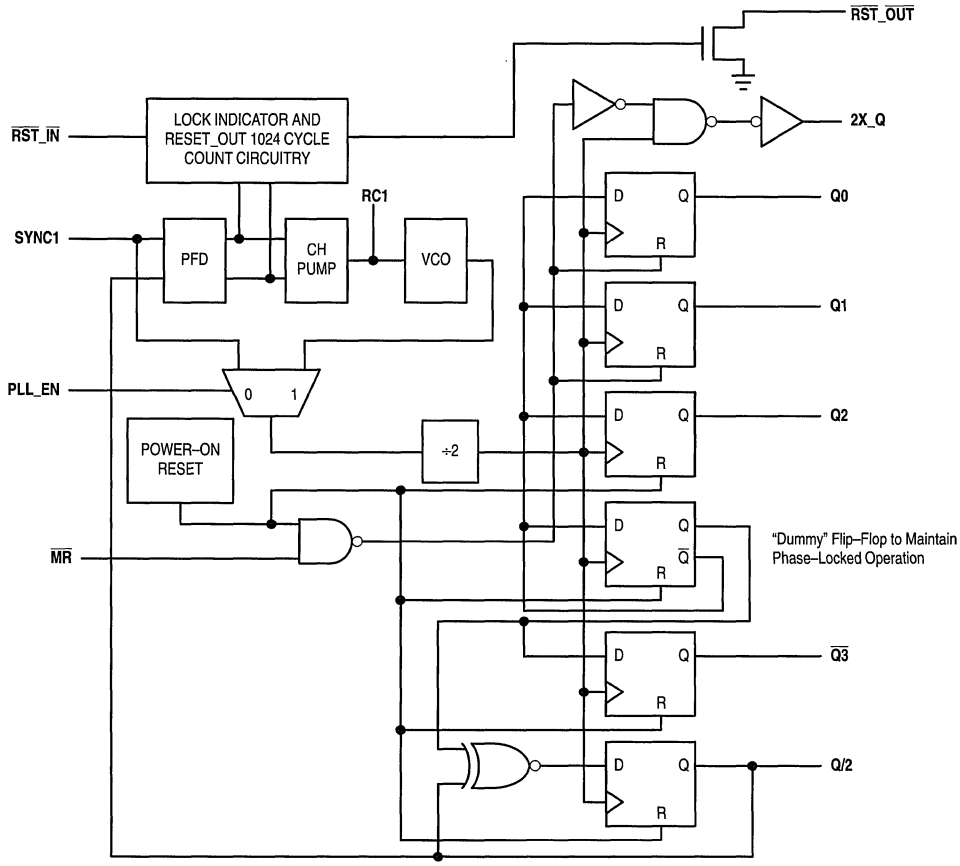


Figure 1. MC88920 Logic Block Diagram

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$ SYNC Input	Rise/Fall Time, SYNC Input From 0.8V to 2.0V	—	5.0	ns
t_{CYCLE}, SYNC Input	Input Clock Period SYNC Input	$\frac{1}{f_{2X\_Q}/4}$	200	ns
Duty Cycle	Duty Cycle, SYNC Input	50% ± 25%		

FREQUENCY SPECIFICATIONS (T_A = 0°C to 70°C; V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Guaranteed Minimum	Unit
Fmax (2X_Q)	Maximum Operating Frequency, 2X_Q Output	50	MHz
Fmax ('Q')	Maximum Operating Frequency, Q0–Q2, $\overline{Q3}$ Outputs	25	MHz

1. Maximum Operating Frequency is guaranteed with the 88920 in a phase–locked condition, and all outputs loaded at 50pF.

AC CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Mimimum	Maximum	Unit	Condition
$t_{RISE/FALL}$[1] All Outputs	Rise/Fall Time, All Outputs into 50Ω Load	0.3	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{RISE/FALL}$[1] 2X_Q Output	Rise/Fall Time into a 20pF Load, With Termination Specified in AppNote 3	0.5	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{pulse\ width(a)}$[1] (Q0, Q1, Q2, $\overline{Q3}$)	Output Pulse Width Q0, Q1, Q2, $\overline{Q3}$ at $V_{CC}/2$	$0.5t_{cycle}$ – 0.5[5]	$0.5t_{cycle}$ + 0.5[5]	ns	50Ω Load Terminated to $V_{CC}/2$ (See Application Note 3)
$t_{pulse\ width(b)}$[1] (2X_Q Output)	Output Pulse Width 2X_Q at $V_{CC}/2$	$0.5t_{cycle}$ – 0.5[5]	$0.5t_{cycle}$ + 0.5[5]	ns	50Ω Load Terminated to $V_{CC}/2$ (See Application Note 3)
t_{PD}[1,4] SYNC – Q/2	SYNC Input to Q/2 Output Delay (Measured at SYNC and Q/2 Pins)	–0.75	–0.15	ns	With 1MΩ From RC1 to An V_{CC} (See Application Note 2)
		+1.25[7]	+3.25[7]	ns	With 1MΩ From RC1 to An GND (See Application Note 2)
t_{SKEWr}[1,2] (Rising)	Output–to–Output Skew Between Outputs Q0–Q2, Q/2 (Rising Edge Only)	—	500	ps	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
t_{SKEWf}[1,2] (Falling)	Output–to–Output Skew Between Outputs Q0–Q2 (Falling Edge Only)	—	1.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
$t_{SKEWall}$[1,2]	Output–to–Output Skew 2X_Q, Q/2, Q0–Q2 Rising $\overline{Q3}$ Falling	—	1.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
t_{LOCK}[3]	Phase–Lock Acquisition Time, All Outputs to SYNC Input	1	10	ms	
t_{PHL} $\overline{MR}$ – Q	Propagation Delay, $\overline{MR}$ to Any Output (High–Low)	1.5	13.5	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
t_{REC}, $\overline{MR}$ to SYNC[6]	Reset Recovery Time rising $\overline{MR}$ edge to falling SYNC edge	9	—	ns	
t_{REC}, $\overline{MR}$ to Normal Operation	Recovery Time for Outputs 2X_Q, Q0, Q1 to Return to Normal PLL Operation	—	3 Clock Cycles (Q Frequency)	ns	
t_W, $\overline{MR}$ LOW[6]	Minimum Pulse Width, $\overline{MR}$ input Low	5	—	ns	
t_W, $\overline{RST\_IN}$ LOW	Minimum Pulse Width, $\overline{RST\_IN}$ Low	10	—	ns	When in Phase–Lock
t_{PZL}	Output Enable Time $\overline{RST\_IN}$ Low to $\overline{RST\_OUT}$ Low	1.5	16.5	ns	See Application Note 5
t_{PLZ}	Output Enable Time $\overline{RST\_IN}$ High to $\overline{RST\_OUT}$ High Z	1016 'Q' Cycles (508 Q/2 Cycles)	1024 'Q' Cycles (512 Q/2 Cycles)	ns	See Application Note 5

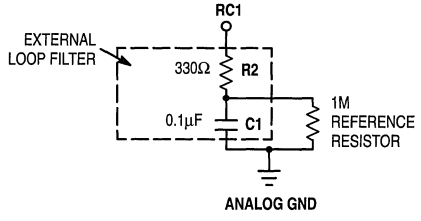
1. These specifications are not tested, they are guaranteed by statistical characterization. See Application Note 1 for a discussion of this methodology.
2. Under equally loaded conditions and at a fixed temperature and voltage.
3. With V_{CC} fully powered–on: t_{CLOCK} Max is with C1 = 0.1µF; t_{LOCK} Min is with C1 = 0.01µF.
4. See Application Note 4 for the distribution in time of each output referenced to SYNC.
5. Refer to Application Note 3 to translate signals to a 1.5V threshold.
6. Specification is valid only when the PLL_EN pin is low.
7. This is a typical specification only, worst case guarantees are not provided.

Application Notes

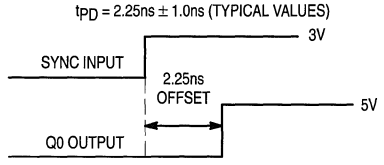
1. Several specifications can only be measured when the MC88920 is in phase–locked operation. It is not possible to have the part in phase–lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88920 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area. IC performance to each specification and fab variation were used to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way, all units passing the ATE test will meet or exceed the non–tested specifications limits.
2. A 1MΩ resistor tied to either Analog V_{CC} or Analog GND, as shown in Figure 2, is required to ensure no jitter is present on the MC88920 outputs. This technique causes a phase offset between the SYNC input and the Q0 output, measured at the pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14 lots described in note 1 while the part was in phase–locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V to 2.0V). The phase measurements were made at 1.5V. See Figure 2 for a graphical description.
3. Two specs ($t_{RISE/FALL}$ and t_{PULSE} Width 2X_Q output, see AC Specifications) guarantee that the MC88920 meets the 20MHz and 25MHz 68040 P–Clock input specification (at 40MHz and 50MHz). For these two specs to be guaranteed by Motorola, the termination scheme shown in Figure 3 must be used. For applications which require 1.5V thresholds, but do not require a tight duty cycle the R_P resistor can be ignored.
4. The t_{PD} spec (SYNC to Q/2) guarantees how close the Q/2 output will be locked to the reference input connected to the SYNC input (including temperature and voltage variation). This also tells what the skew from the Q/2 output on one part connected to a given reference input, to the Q/2 output on one or more parts connected to that reference input (assuming equal delay from the referenceinput to the SYNC input of each part). Therefore the t_{PD} spec is equivalent to a part–to–part specification. However, to correctly predict the skew from a given output on one part to any other output on one or more other parts, the distribution of each output in relation to the SYNC input must be known. This distribution for the MC88920 is provided in Table 1.

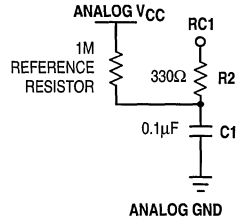
TABLE 1. Distribution of Each Output versus SYNC

Output	–(ps)	+(ps)
2X_Q	TBD	TBD
Q0	TBD	TBD
Q1	TBD	TBD
Q2	TBD	TBD
$\overline{Q3}$	TBD	TBD
Q/2	TBD	TBD



WITH THE 1MΩ RESISTOR TIED IN THIS FASHION THE T_{PD} SPECIFICATION, MEASURED AT THE INPUT PINS IS:





WITH THE 1MΩ RESISTOR TIED IN THIS FASHION THE T_{PD} SPECIFICATION, MEASURED AT THE INPUT PINS IS:

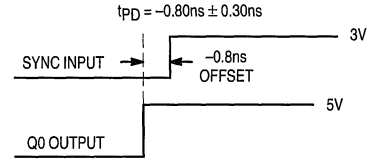


Figure 2. Depiction of the Fixed SYNC to Q0 Offset (t_{PD}) Which Is Present When a 1MΩ Resistor Is Tied to V_{CC} or Ground

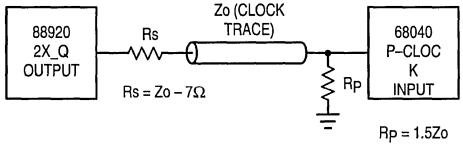


Figure 3. MC68040 P–Clock Input Termination Scheme

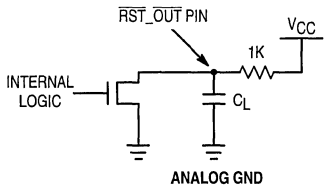


Figure 4. RST_OUT Test Circuit

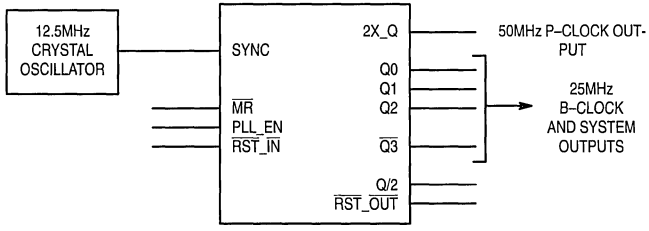


Figure 5. Logical Representation of the MC88920 With Input/Output Frequency Relationships

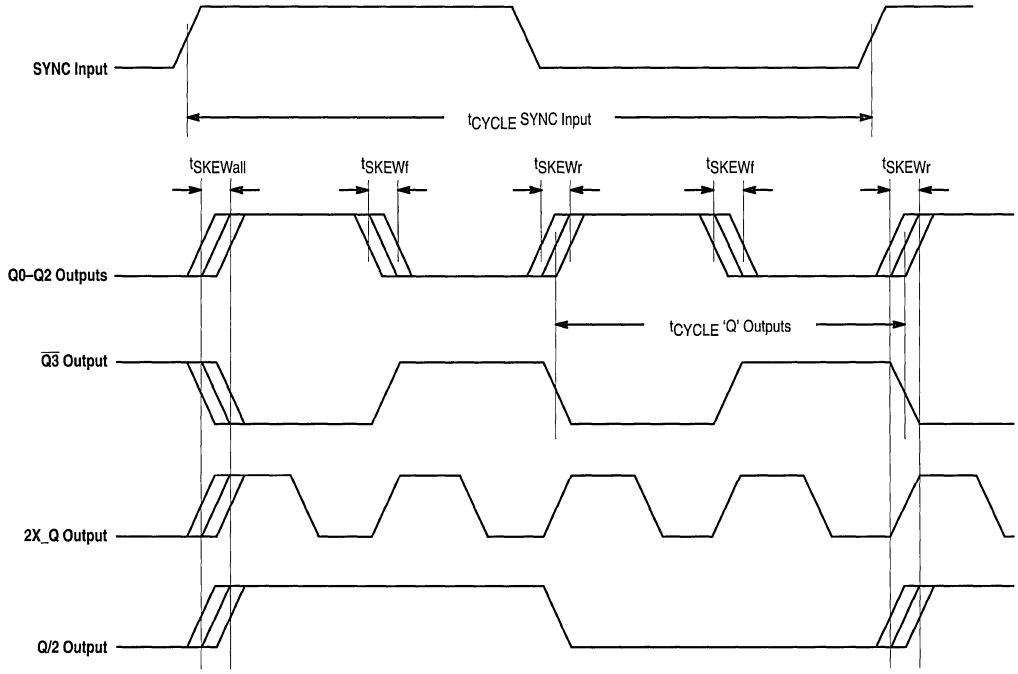


Figure 6. Output/Input Switching Waveforms and Timing Relationships

Timing Notes

1. The MC88920 aligns rising edges of the outputs and the SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges. All skews are specified as 'windows', not as a ± deviation around a center point.

The t_{PD} spec includes the full temperature range from 0°C to 70°C and the full V_{CC} range from 4.75V to 5.25V. If the ΔT and ΔV_{CC} is a given system are less than the specification limits, the t_{PD} spec window will be reduced. The t_{PD} window for a given ΔT and ΔV_{CC} is given by the following regression formula:

TBD

5. The $\overline{RST}\_\overline{OUT}$ pin is an open drain N–Channel output. Therefore an external pull–up resistor must be provide to pull up the $\overline{RST}\_\overline{OUT}$ pin when it goes into the high impedance state (after the MC88920 is phase–locked to the reference input with $\overline{RST}\_\overline{IN}$ held high or 1024 'Q' cycles after the $\overline{RST}\_\overline{IN}$ pin goes high when the part is locked). In the t_{PLZ} and t_{PZL} specifications, a 1KΩ resistor is used as a pull–up as shown in Figure 4.

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 7 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will make the 88920 PLL insensitive to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100ps phase deviation on the 88920 outputs. A 250mV step deviation on V_{CC} using the recommended filter values will cause no more than a 250ps phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step will cause no more than a 100ps phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88920's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 7 is to give the 88920 additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (1M and 330Ω). The loop filter capacitor (0.1uF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 1M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 1M resistor provides the correct amount of current injection into the charge pump (2–3μA).

2. In addition to the bypass capacitors used in the analog filter of Figure 7, there should be a 0.1μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88920 outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88920 package as possible.

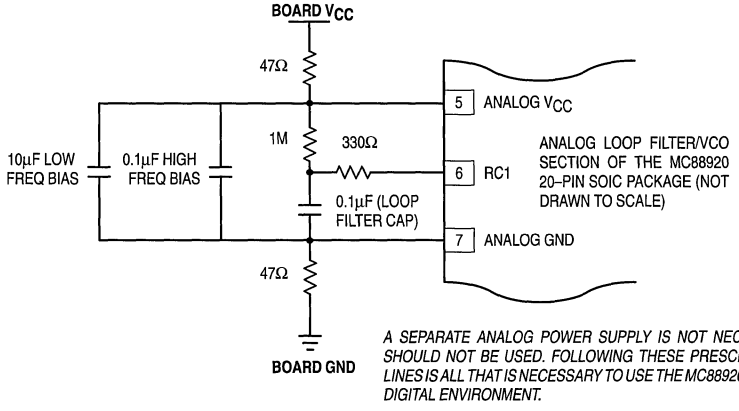


Figure 7. Recommended Loop Filter and Analog Isolation Scheme for the MC88920

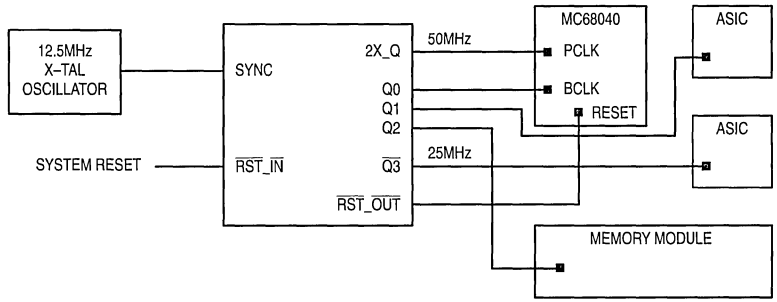


Figure 8. Typical MC88920/MC68040 System Configuration

Low Skew CMOS PLL Clock Driver
With Power-Down/Power-Up Feature

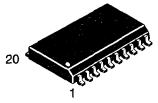
MC88921

LOW SKEW CMOS PLL CLOCK DRIVER With Power–Down/ Power–Up Feature

The MC88921 Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for CISC microprocessor or single processor RISC systems.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple locations on a board. The PLL also allows the MC88921 to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency.

- 2X_Q Output Meets All Requirements of the 20, 25 and 33MHz 68040 Microprocessor PCLK Input Specifications
- 60 and 66MHz Output to Drive the Pentium™ Microprocessor
- Four Outputs (Q0–Q3) With Output–Output Skew <500ps and Six Outputs Total (Q0–Q3, 2X_Q) With <1ns Skew Each Being Phase and Frequency Locked to the SYNC Input
- The Phase Variation From Part–to–Part Between SYNC and the 'Q' Outputs Is Less Than 600ps (Derived From the T_{PD} Specification, Which Defines the Part–to–Part Skew)
- SYNC Input Frequency Range From 5MHZ to 2X_Q $F_{Max}/4$
- Additional Outputs Available at 2X the System 'Q' Frequency
- All Outputs Have ±36mA Drive (Equal High and Low) CMOS Levels. Can Drive Either CMOS or TTL Inputs. All Inputs Are TTL–Level Compatible
- Test Mode Pin (PLL_EN) Provided for Low Frequency Testing
- Special Power–Down Mode With 2X_Q, Q0, and Q1 Being Reset (With $\overline{MR}$), and Other Outputs Remain Running. 2X_Q, Q0 and Q1 Are Guaranteed to Be in Lock 3 Clock Cycles After $\overline{MR}$ Is Negated



DW SUFFIX
SOIC PACKAGE
CASE 751D–04

Four 'Q' outputs (Q0–Q3) are provided with less than 500ps skew between their rising edges. A 2X_Q output runs at twice the 'Q' output frequency. The 2X_Q output is ideal for 68040 systems which require a 2X processor clock input. The 2X_Q output meets the tight duty cycle spec of the 20, 25 and 33MHz 68040. The 66MHz 2X_Q output can also be used for driving the clock input of the Pentium Microprocessor while providing multiple 33MHz outputs to drive the support and bus logic. The FBSEL pin allows the user to internally feedback either the Q or the Q/2 frequency providing a 1x or 2x multiplication factor of the reference input.

In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88921 in a static 'test mode'. In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment.

A lock indicator output (LOCK) will go HIGH when the loop is in steady state phase and frequency lock. The output will go LOW if phase–lock is lost or when the PLL_EN pin is LOW. The lock output will go HIGH no later than 10ms after the 88921 sees a sync signal and full 5.0V V_{CC}.

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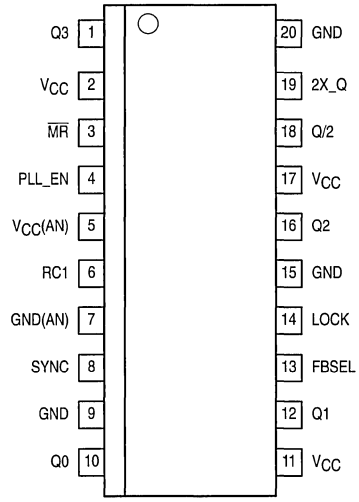
Power–Down Mode Functionality

The MC88921 has a special feature designed in to allow the processor clock inputs to be reset for total processor power–down, and then to return to phase–locked operation very quickly when the processor is powered–up again.

The $\overline{MR}$ pin resets outputs 2X_Q, Q0 and Q1 only leaving the other outputs operational for other system activity. When $\overline{MR}$ is negated, all outputs will be operating normally within 3 clock cycles.



Pinout: 20–Lead Wide SOIC Package (Top View)

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0V
PD_1	Power Dissipation at 33MHz With 50Ω Thevenin Termination	15mW/Output 90mW/Device	mW	V_{CC} = 5.0V T = 25°C
PD_2	Power Dissipation at 33MHz With 50Ω Parallel Termination to GND	37.5mW/Output 225mW/Device	mW	V_{CC} = 5.0V T = 25°C

MAXIMUM RATINGS*

Symbol	Parameter	Limits	Unit
V_{CC}, AV_{CC}	DC Supply Voltage Referenced to GND	–0.5 to 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, Per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, Per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current Per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	5.0 ±10%	V
V_{in}	DC Input Voltage	0 to V_{CC}	V
V_{out}	DC Output Voltage	0 to V_{CC}	V
T_A	Ambient Operating Temperature	0 to 70	°C
ESD	Static Discharge Voltage	> 1500	V

DC CHARACTERISTICS (T_A = –40°C to 85°C; V_{CC} = 5.0V ± 5%)

Symbol	Parameter	V_{CC}	Guaranteed Limits	Unit	Condition
V_{IH}	Minimum High Level Input Voltage	4.75 5.25	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{IL}	Minimum Low Level Input Voltage	4.75 5.25	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{OH}	Minimum High Level Output Voltage	4.75 5.25	4.01 4.51	V	V_{IN} = V_{IH} or V_{IL} I_{OH} –36mA –36mA
V_{OL}	Minimum Low Level Output Voltage	4.75 5.25	0.44 0.44	V	V_{IN} = V_{IH} or V_{IL} I_{OH} +36mA[1] +36mA
I_{IN}	Maximum Input Leakage Current	5.25	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.25	2.0 [2]	mA	V_I = V_{CC} – 2.1V
I_{OLD}	Minimum Dynamic[3] Output Current	5.25	88	mA	V_{OLD} = 1.0V Max
I_{OHD}		5.25	–88	mA	V_{OHD} = 3.85 Min
I_{CC}	Maximum Quiescent Supply Current	5.25	750	µA	V_I = V_{CC}, GND

1. I_{OL} is +12mA for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration 2.0ms, one output loaded at a time.

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$ SYNC Input	Rise/Fall Time, SYNC Input From 0.8V to 2.0V	—	5.0	ns
t_{CYCLE}, SYNC Input	Input Clock Period SYNC Input	$\frac{1}{f_{2X\_Q/4}}$	200	ns
Duty Cycle	Duty Cycle, SYNC Input	50% ± 25%		

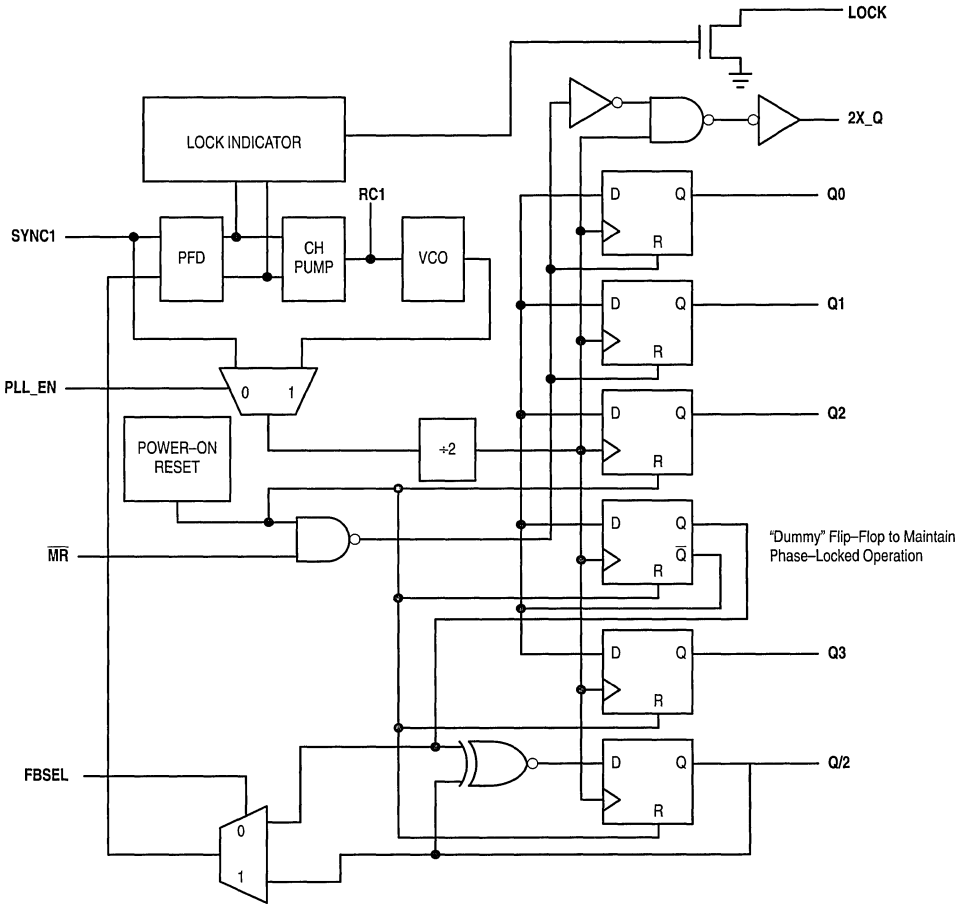


Figure 1. MC88921 Logic Block Diagram

FREQUENCY SPECIFICATIONS (T_A = –40°C to 85°C; V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Guaranteed Minimum	Unit
Fmax (2X_Q)	Maximum Operating Frequency, 2X_Q Output	66	MHz
Fmax ('Q')	Maximum Operating Frequency, Q0–Q3 Outputs	33	MHz

1. Maximum Operating Frequency is guaranteed with the 88921 in a phase–locked condition, and all outputs loaded at 50pF.

AC CHARACTERISTICS (T_A = –40°C to 85°C; V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Minimum	Maximum	Unit	Condition
$t_{RISE/FALL}$[1] All Outputs	Rise/Fall Time, All Outputs into 50Ω Load	0.3	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{RISE/FALL}$[1] 2X_Q Output	Rise/Fall Time into a 20pF Load, With Termination Specified in AppNote 3	0.5	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{pulse\ width(a)}$[1] (Q0, Q1, Q2, Q3)	Output Pulse Width Q0, Q1, Q2, Q3 at $V_{CC}/2$	$0.5t_{cycle} - 0.5$[5]	$0.5t_{cycle} + 0.5$[5]	ns	50Ω Load Terminated to $V_{CC}/2$ (See Application Note 3)
$t_{pulse\ width(b)}$[1] (2X_Q Output)	Output Pulse Width 2X_Q at $V_{CC}/2$	$0.5t_{cycle} - 0.5$[5]	$0.5t_{cycle} + 0.5$[5]	ns	50Ω Load Terminated to $V_{CC}/2$ (See Application Note 3)
t_{PD}[1,4] SYNC – Q/2	SYNC Input to Q Output Delay (Measured at SYNC and Q/2 Pins)	–0.75	–0.15	ns	With 1MΩ From RC1 to An V_{CC} (See Application Note 2)
		+1.25 [7]	+3.25 [7]	ns	With 1MΩ From RC1 to An GND (See Application Note 2)
t_{SKEWr}[1,2] (Rising)	Output–to–Output Skew Between Outputs Q0–Q3 (Rising Edge Only)	—	500	ps	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
t_{SKEWf}[1,2] (Falling)	Output–to–Output Skew Between Outputs Q0–Q3 (Falling Edge Only)	—	1.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
$t_{SKEWall}$[1,2]	Output–to–Output Skew 2X_Q, Q0–Q3 Rising	—	1.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
t_{LOCK}[3]	Phase–Lock Acquisition Time, All Outputs to SYNC Input	1	10	ms	
t_{PHL} $\overline{MR}$ – Q	Propagation Delay, $\overline{MR}$ to Any Output (High–Low)	1.5	13.5	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
t_{REC}, $\overline{MR}$ to SYNC[6]	Reset Recovery Time rising $\overline{MR}$ edge to falling SYNC edge	9	—	ns	
t_{REC}, $\overline{MR}$ to Normal Operation	Recovery Time for Outputs 2X_Q, Q0, Q1 to Return to Normal PLL Operation	—	3 Clock Cycles (Q Frequency)	ns	
t_W, $\overline{MR}$ LOW[6]	Minimum Pulse Width, $\overline{MR}$ input Low	5	—	ns	

1. These specifications are not tested, they are guaranteed by statistical characterization. See Application Note 1 for a discussion of this methodology.
2. Under equally loaded conditions and at a fixed temperature and voltage.
3. With V_{CC} fully powered–on: t_{CLOCK} Max is with C1 = 0.1μF; t_{LOCK} Min is with C1 = 0.01μF.
4. See Application Note 4 for the distribution in time of each output referenced to SYNC.
5. Refer to Application Note 3 to translate signals to a 1.5V threshold.
6. Specification is valid only when the PLL_EN pin is low.
7. This is a typical specification only, worst case guarantees are not provided.

Application Notes

1. Several specifications can only be measured when the MC88921 is in phase–locked operation. It is not possible to have the part in phase–lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88921 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area.

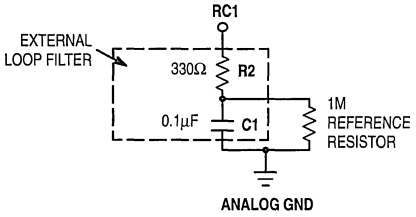
2. A 1MΩ resistor tied to either Analog V_{CC} or Analog GND, as shown in Figure 2, is required to ensure no jitter is present on the MC88921 outputs. This technique causes a phase offset between the SYNC input and the Q0 output, measured at the pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14 lots described in note 1 while the part was in phase–locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V to 2.0V). The phase measurements were made at 1.5V. See Figure 2 for a graphical description.

3. Two specs ($t_{RISE/FALL}$ and t_{PULSE} Width 2X_Q output, see AC Specifications) guarantee that the MC88921 meets the 20MHz, 25MHz and 33MHz 68040 P–Clock input specification (at 40MHz, 50MHz, and 66MHz). For these two specs to be guaranteed by Motorola, the termination scheme shown in Figure 3 must be used. For applications which require 1.5V thresholds, but do not require a tight duty cycle the R_P resistor can be ignored.

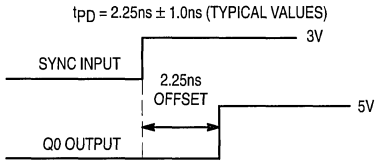
4. The t_{PD} spec (SYNC to Q/2) guarantees how close the Q/2 output will be locked to the reference input connected to the SYNC input (including temperature and voltage variation). This also tells what the skew from the Q/2 output on one part connected to a given reference input, to the Q/2 output on one or more parts connected to that reference input (assuming equal delay from the reference input to the SYNC input of each part). Therefore the t_{PD} spec is equivalent to a part–to–part specification. However, to correctly predict the skew from a given output on one part to any other output on one or more other parts, the distribution of each output in relation to the SYNC input must be known. This distribution for the MC88921 is provided in Table 1.

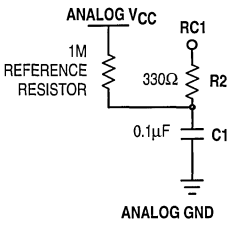
TABLE 1. Distribution of Each Output versus SYNC

Output	–(ps)	+(ps)
2X_Q	TBD	TBD
Q0	TBD	TBD
Q1	TBD	TBD
Q2	TBD	TBD
Q3	TBD	TBD
Q/2	TBD	TBD



WITH THE 1MΩ RESISTOR TIED IN THIS FASHION THE T_{PD} SPECIFICATION, MEASURED AT THE INPUT PINS IS:





WITH THE 1MΩ RESISTOR TIED IN THIS FASHION THE T_{PD} SPECIFICATION, MEASURED AT THE INPUT PINS IS:

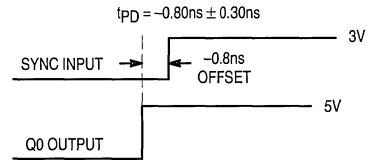


Figure 2. Depiction of the Fixed SYNC to Q0 Offset (t_{PD}) Which Is Present When a 1MΩ Resistor Is Tied to V_{CC} or Ground

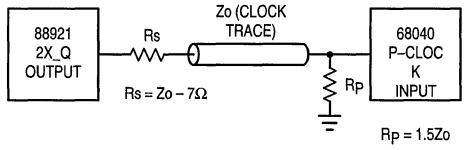


Figure 3. MC68040 P–Clock Input Termination Scheme

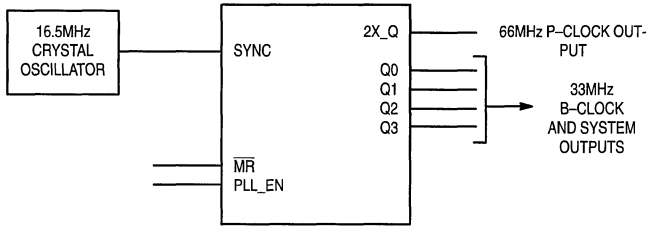


Figure 4. Logical Representation of the MC88921 With Input/Output Frequency Relationships

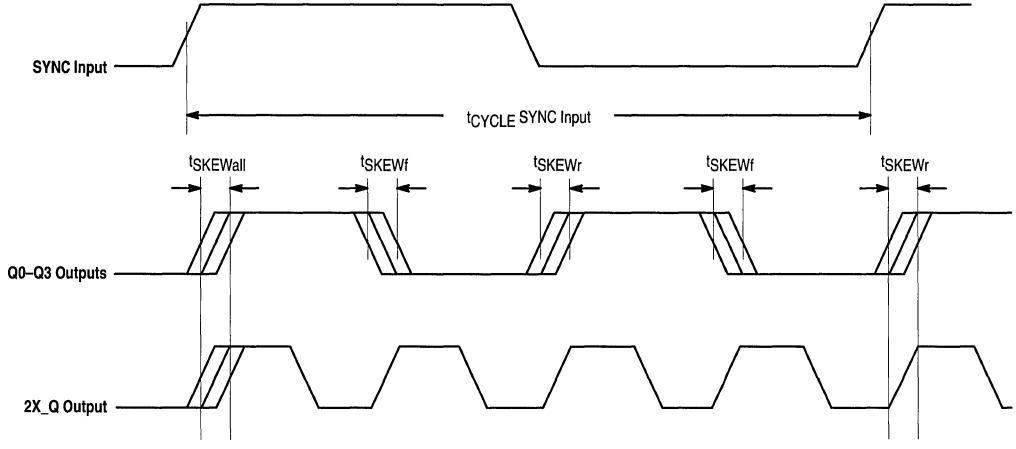


Figure 5. Output/Input Switching Waveforms and Timing Relationships

Timing Notes

1. The MC88921 aligns rising edges of the outputs and the SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges. All skews are specified as 'windows', not as a ± deviation around a center point.

The t_{PD} spec includes the full temperature range from 0°C to 70°C and the full V_{CC} range from 4.75V to 5.25V. If the ΔT and ΔV_{CC} is a given system are less than the specification limits, the t_{PD} spec window will be reduced.

The t_{PD} window for a given ΔT and ΔV_{CC} is given by the following regression formula:

TBD

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 7 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will make the 88921 PLL insensitive to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100ps phase deviation on the 88921 outputs. A 250mV step deviation on V_{CC} using the recommended filter values will cause no more than a 250ps phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step will cause no more than a 100ps phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88921's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 7 is to give the 88921 additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (1M and 330Ω). The loop filter capacitor (0.1uF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 1M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 1M resistor provides the correct amount of current injection into the charge pump (2–3μA).

2. In addition to the bypass capacitors used in the analog filter of Figure 7, there should be a 0.1μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88921 outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88921 package as possible.

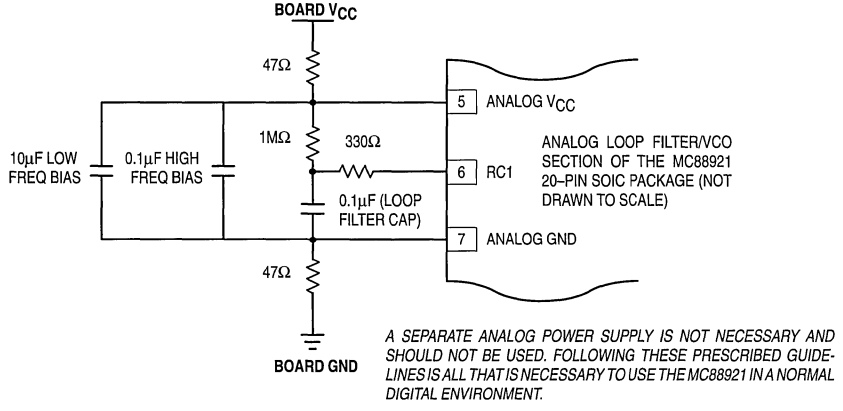


Figure 6. Recommended Loop Filter and Analog Isolation Scheme for the MC88921

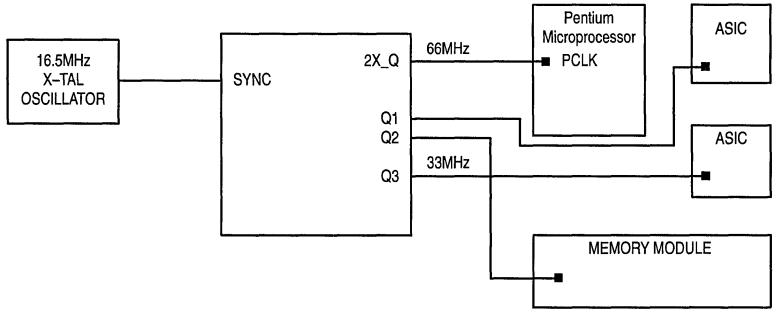


Figure 7. Typical MC88921/Pentium Microprocessor System Configuration

Not Recommended for New Designs

CMOS PLL Clock Driver

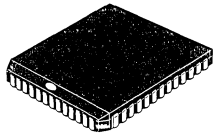
Programmable Frequency, Low Skew, High Fan-Out

MC88PL117

CMOS PLL CLOCK DRIVER

The MC88PL117 utilizes proven phase–locked loop clock driver technology to create a large fan–out, multiple frequency and phase, low skew clock driver. The 88PL117 provides the clock frequencies necessary to drive systems using the PowerPC™ 601 microprocessor and the Pentium™ microprocessor (see applications section for details). A total of 14 high current, matched impedance outputs are available in 8 programmable output frequency and phase configurations. Output frequencies are referenced to a system frequency, Q, and are available at 2X, 1X, and 1/2X the Q frequency. Four programmable input frequency multiplication ratios can be programmed to provide outputs at 1X, 2X, and 4X the system frequency Q. Details on the programmable configurations can be found in the applications section of this data sheet.

- Clock Driver for PowerPC 601 and Pentium Microprocessors
- 14 programmable outputs
- Maximum output–to–output skew of 500ps for a single frequency
- Maximum output–to–output skew of 500ps for multiple frequencies
- f_{MAX} of 2X_Q = 120MHz
- One output with programmable phase capability
- ±36mA DC current outputs drive 50Ω transmission lines
- A lock indicator output (LOCK) goes high when steady–state phase–lock is achieved
- OE/$\overline{MR}$ 3–state control
- Dedicated feedback output
- Two selectable clock inputs
- PLL enable pin for testability
- Dynamic Switch Between SYNC Inputs



FN SUFFIX
52–LEAD PLASTIC LEADLESS
CHIP CARRIER (PLCC)
CASE 778–02

One output (QFEED) is dedicated for feedback. It is located physically close to the FEEDBACK input pin to minimize the feedback line length. External delay (increased wire length) or logic can be inserted in the feedback path if necessary. Proper termination of the feedback line is necessary for any line length over one inch.

One output is provided with up to eight selectable 1/8 or 1/4 period (45° or 90°) delay increments. Three control pins, Ø2, Ø1 and Ø0, program the eight increments; the increment/phase shift positions are shown in Table 3. in the applications section.

All outputs can be 3–stated (high impedance) during board–level testing with the OE/$\overline{MR}$ pin; the QFEED and LOCK outputs will not be 3–stated, which allows the 88PL117 to remain in a phase–locked condition. Correct phase and frequency coherency will be guaranteed one to two cycles after bringing the OE/$\overline{MR}$ pin high. The PLL_EN pin disables the PLL and gates the SYNC input signal directly into the internal clock distribution network to provide low frequency testability. Two selectable SYNC inputs (SYNC0 and SYNC1) are provided for clock redundancy or ease of testability. The device is guaranteed to lock to the new SYNC input when the REF_SEL input is switched dynamically.

A phase–lock indicator output (LOCK) stays low when the part is out of lock (start–up, etc.) and goes high when steady–state phase–lock is achieved. The lock indicator circuitry works reliably for VCO frequencies down to 55MHz. For VCO frequencies less than 55MHz, no guarantees are offered for the lock indicator output.

The MC88PL117 VCO is capable of operating at frequencies higher than the output divider and feedback structures are able to follow. When the VCO is in the mode described above, it is referred to as "runaway" and the device will not lock. The condition usually occurs at power–up. To avoid runaway, it is recommended that the device be fully powered before a sync signal is applied.

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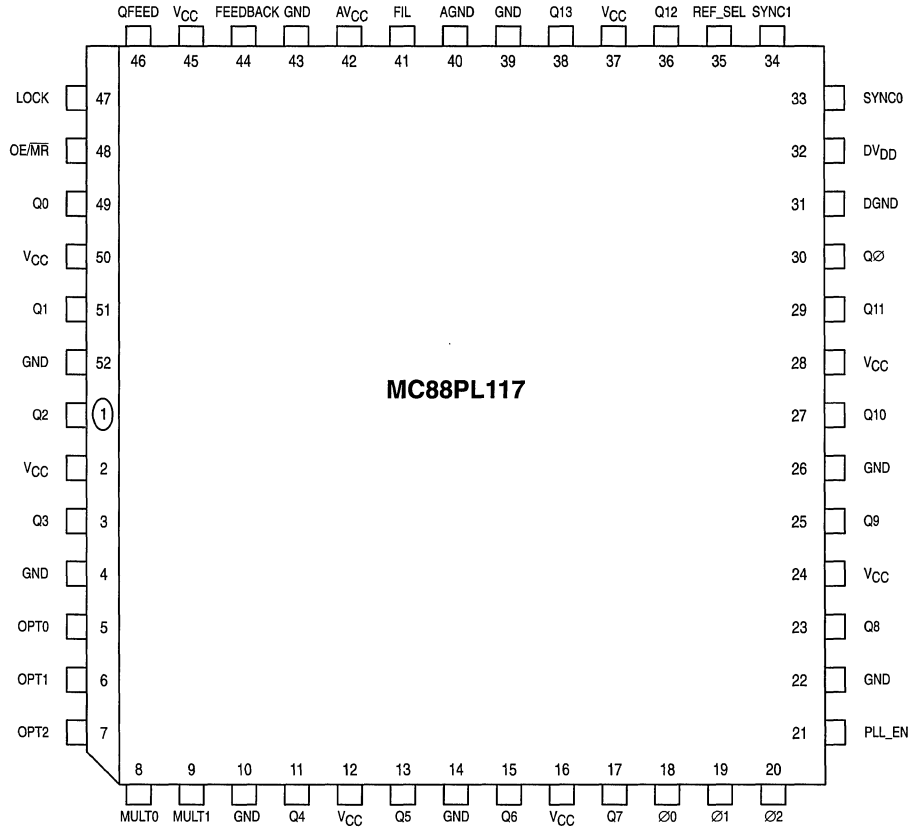
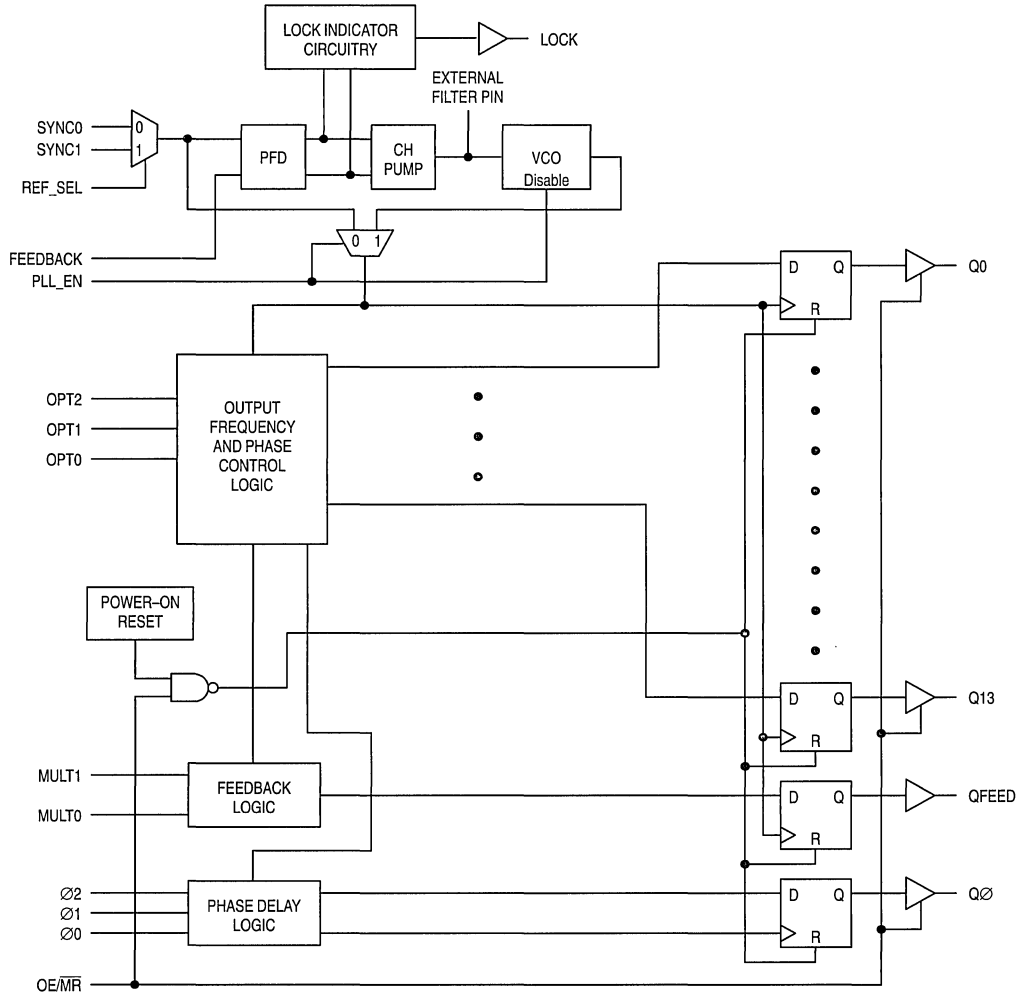


Pinout: 52–Lead PLCC (Top View)



MC88PL117 Block Diagram (Logical Representation)

Explanation of Programmable Frequency Configurations

The MC88PL117 has six different output frequency configurations. Figures 1 to 6 graphically depict these output configurations. There are also three feedback frequency options, which yields a total of 18 unique input–to–output frequency configurations. All configurations use 'Q' as the system frequency frame of reference. Therefore all output and feedback frequencies are referenced as a multiple of Q. Figures 1 to 6 also indicate the input levels of OPT0, OPT1, and OPT2 for each of the eight output configurations. The input levels of MULT0 and MULT1 are varied in these figures to represent the different feedback (multiplication) frequencies. The frequency of the phase shift output, QØ, is also indicated in the figures. Tables 1. and 2. lists all 18 input/output frequency configurations. Table 3. gives the QØ phase shift increments.

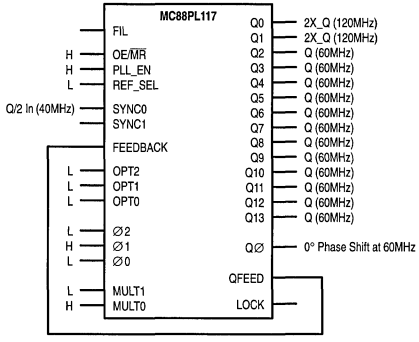


Figure 1. Output Frequency Configuration 1
(OPT0 = L, OPT1 = L, OPT2 = L
Q/2 Input Frequency, MULT0 = H, MULT1 = L)

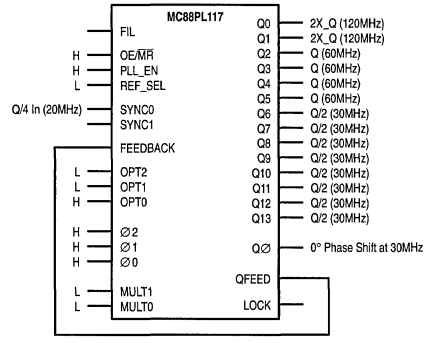


Figure 2. Output Frequency Configuration 2
(OPT0 = H, OPT1 = L, OPT2 = L
Q/4 Input Frequency, MULT0 = L, MULT1 = L)

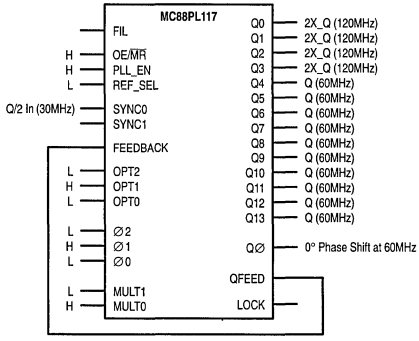


Figure 3. Output Frequency Configuration 3
(OPT0 = L, OPT1 = H, OPT2 = L
Q/2 Input Frequency, MULT0 = H, MULT1 = L)

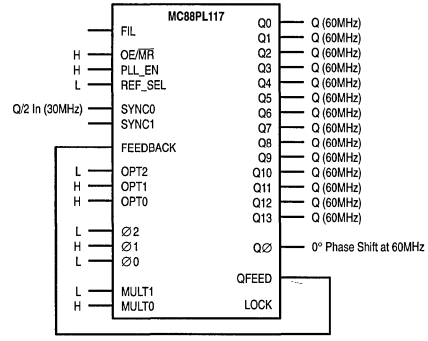


Figure 4. Output Frequency Configuration 4
(OPT0 = H, OPT1 = H, OPT2 = L
Q/2 Input Frequency, MULT0 = H, MULT1 = L)

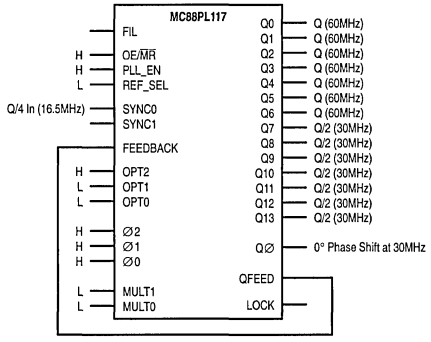


Figure 5. Output Frequency Configuration 5
(OPT0 = L, OPT1 = L, OPT2 = H
Q/4 Input Frequency, MULT0 = L, MULT1 = L)

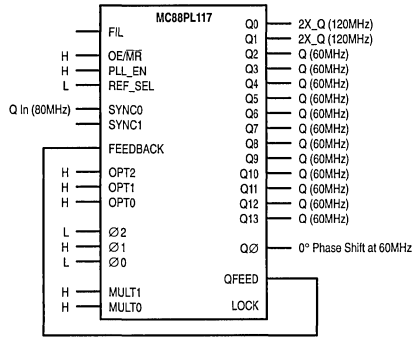


Figure 6. Output Frequency Configuration 6
(OPT0 = H, OPT1 = H, OPT2 = H
Q Input Frequency, MULT0 = H, MULT1 = H)

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) T_A =0° C to + 70° C, V_{CC} = 5.0 V ±5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA [1]	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 36 mA [1]	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	±1.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} – 2.1 V	5.25	2.0 [2]	mA
I_{OLD}	Minimum Dynamic Output Current [3]	V_{OLD} = 1.0V Max	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85V Min	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3–State Leakage Current	V_I = V_{IH} or V_{IL};V_O = V_{CC} or GND	5.25	±50 [4]	µA

1. I_{OL} and I_{OH} are 12mA and –12mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0ms, one output loaded at a time.
4. Specification value for I_{OZ} is preliminary, will be finalized upon 'MC' status.

PRELIMINARY AC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Target Specifications Min	Target Specifications Max	Unit	Condition
t_{skewr}	Output–to–Output Skew (Same Frequency, Coincident Rising Edges)		500	ps	50Ω Load[2]
$t_{skewrall}$	Output–to–Output Skew (Any Frequency, Coincident Rising Edges, Q0–Q13, QFEED)		500	ps	50Ω Load[2]
t_{skewp}	Part–to–Part Skew[1]		1.0	ns	50Ω Load[2]
t_r/t_f	Output Rise/Fall Time (0.8 to 2.0V)	0.15	1.0	ns	50Ω Load[2]
t_{PULSE}	Output Pulse Width, All Outputs[2] (Measured at $V_{CC}/2$)	$0.5t_{CYCLE} - 0.5$	$0.5t_{CYCLE} + 0.5$	ns	50Ω Load[2]
t_{pd}	SYNC Input to FEEDBACK Delay f_{SYNC}=15MHz	–200	400	ps	Feedback=Q,Q/2
	f_{SYNC}=20MHz	–200	400		
	f_{SYNC}=25MHz	–100	500		
	f_{SYNC}=30MHz	0	600		
	f_{SYNC}=15MHz	–50	550		Feedback=Q/4
$Jitter_{CC}$	Cycle–to–Cycle Jitter (Clock Period Stability)		±250	ps	
f_{MAX}	Maximum Output Frequency for 2X_Q Outputs	8	120	MHz	50Ω Load[2]
f_{MAX}	Maximum Output Frequency for Q Outputs	4	60	MHz	50Ω Load[2]
f_{MAX}	Maximum Output Frequency for Q/2 Outputs	2	30	MHz	50Ω Load[2]
$t_{skew\varnothing}$	Phase Accuracy of Q∅ versus Q or Q/2	Phase Offset – 750	Phase Offset + 250	ps	

1. This assumes that each device is running off of the same clock source with zero skew between clock source signals. A small amount of negative offset may be present between SYNC and FEEDBACK (t_{PD} Spec).
2. 50Ω load terminated to $V_{CC}/2$.

TABLE 1. PROGRAMMABLE OUTPUT CONFIGURATIONS (Q is system reference frequency)

Output Configuration Number	OPT2	OPT1	OPT0	No of 2X_Q Outputs	No of Q Outputs	No of Q/2 Outputs
1	L	L	L	2	12	0
2	L	L	H	2	4	8
3	L	H	L	4	10	0
4	L	H	H	0	14	0
5	H	L	L	0	7	7
6	H	H	H	2	12	0

TABLE 2. PROGRAMMABLE INPUT FREQUENCY MODES (Multiplication factors)

Input Frequency Mode	MULT1	MULT0	Input Frequency
1	L	L	Q/4
2	L	H	Q/2
3	H	H	Q

TABLE 3. Q∅ PROGRAMMABLE PHASE INCREMENTS FOR Q AND Q/2 OUTPUTS

∅2	∅1	∅0	Q∅ Phase to Q Outputs[1]	Q∅/2 Phase to Q Outputs[2]	∅2	∅1	∅0	Q∅ Phase to Q Outputs[1]	Q∅/2 Phase to Q Outputs[2]
L	L	L	180°	45°	H	L	L	180°	225°
L	L	H	90°	90°	H	L	H	90°	270°
L	H	L	0°	135°	H	H	L	0°	315°
L	H	H	270°	180°	H	H	H	270°	360°

1. Valid for output configurations 1, 3, 4, 6, 8
2. Valid for output configurations 2, 5, 7

Applications Information

Introduction

The 88PL117 provides the necessary clock frequencies for the PowerPC 601 and Pentium Microprocessors. With output frequency capabilities up to 120MHz and the ability to also generate half and quarter frequency clocks the 88PL117 simplifies the system implementation of a PowerPC 601 or Pentium Microprocessor. This section will overview the clock requirements of the PowerPC 601 and Pentium Microprocessors and apply those to the specification limits of the 88PL117 to demonstrate compatibility. Although not exhaustive the intent is to provide a basic set of guidelines on system implementation. For more cost sensitive applications which require fewer clocks the designer should refer to the MC88915TFN133 data sheet for an alternative clock driver suitable for PowerPC 601 or Pentium Microprocessor based designs.

Figures 7 and 8 illustrate two common output configurations of the 88PL117 which will facilitate POWERPC 601 (MPC601) system designs. Figure 7 would prove beneficial for high frequency processor designs where the bus clock would likely run at one fourth the 2X_PCLK input. In this configuration a 2X_Q output of the 88PL117 can drive the 2X_PCLK of the PowerPC 601 processor while a Q and Q/2 output can drive the $\overline{\text{PCLK\_EN}}$ and $\overline{\text{BCLK\_EN}}$ inputs respectively. For designs where the system bus will run at half the frequency of the 2X_PCLK (same frequency as the internal processor clock) a larger number of Q outputs would be required. Figure 8 could be used in this situation with a

2X_Q output driving the 2X_PCLK input and a Q output driving the PCLK_EN. In this implementation the BCLK_EN input of the MPC601 is simply tied LOW.

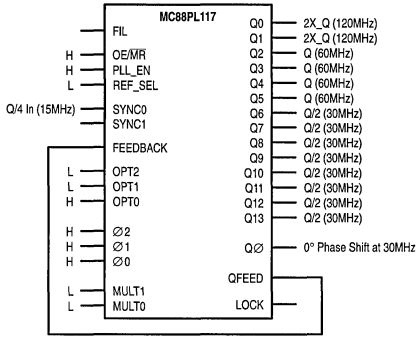


Figure 7. 88PL117 Output Configuration 1 for Driving the MPC601 Microprocessor

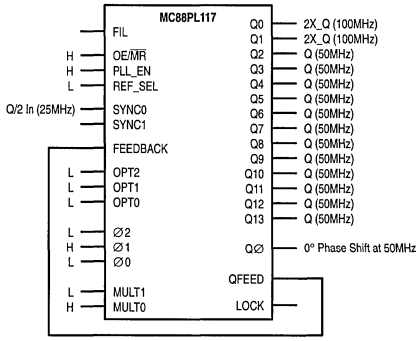


Figure 8. 88PL117 Output Configuration 2 for Driving the MPC601 Microprocessor

Driving the PowerPC 601 Microprocessor

Figures 9 and 10 illustrate the required waveforms for driving the MPC601 processor in both bus clock frequency modes. Figure 10 illustrates the relationship between the 2X_Q, Q and Q/2 outputs of the 88PL117. For the case of the BCLK_EN input being held LOW, the setup and hold specifications for PCLK_EN are automatically satisfied by the internal design of the 88PL117. For the first case pictured in Figure 9, there may be a potential problem: the hold time spec for BCLK_EN rising to 2X_PCLK is 0ns. Because there can be up to ±250ps skew between the 2X_Q and Q/2 outputs of the 88PL117, this hold spec may be violated. This situation can be remedied in one of two ways: first extra PCB etch can be added to the Q/2 output to delay it relative to the 2X_Q output; or secondly, the Q∅ output can be used to drive the BCLK_EN input. The Q∅ output can be phase delayed relative to the 2X_Q output to ensure the hold time requirement of the MPC601 processor will be met.

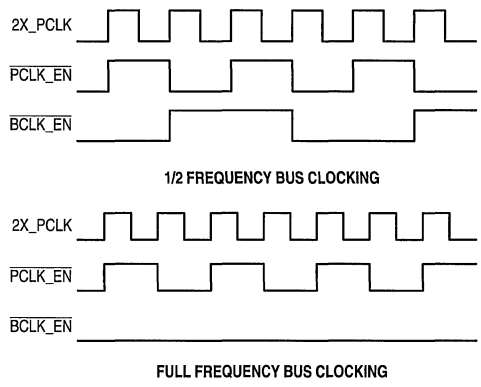


Figure 9. MPC601 Processor Clocking Waveforms

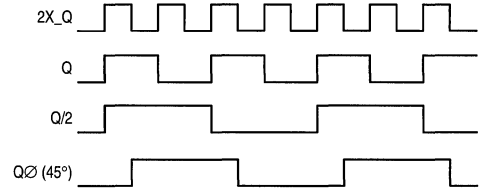


Figure 10. 88PL117 Output Waveforms

The 88PL117 features CMOS level outputs to minimize edge transition time and optimize transmission line driving capability. The MPC601 processor inputs are TTL level compatible inputs and therefore specification limits are calculated from TTL level thresholds. The specification limits of concern are the input duty cycle and input pulse width requirements outlined in the MPC601 specification for the 2X_PCLK input. Figure 11 demonstrates the termination technique required on the 2X_Q output of the 88PL117 to ensure compatibility with the 2X_PCLK input of the MPC601 processor. At 100 or 120MHz, the 2X_Q output threshold must be shifted down to the 1.4V threshold to meet the input pulse width specification limits. The termination scheme in Figure 11 creates a voltage division which essentially translates the CMOS threshold down to a TTL threshold, while at the same time effectively terminating the transmission line. The 88PL117 exhibits a very tight duty cycle specification at CMOS thresholds. Therefore, once translated via the termination scheme of Figure 11, the MPC601 processor input specifications are easily met.

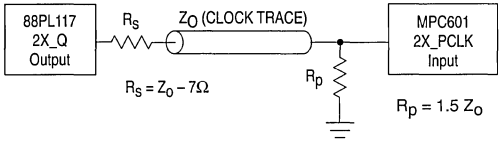


Figure 11. MPC601 2X_PCLK Input Termination Scheme

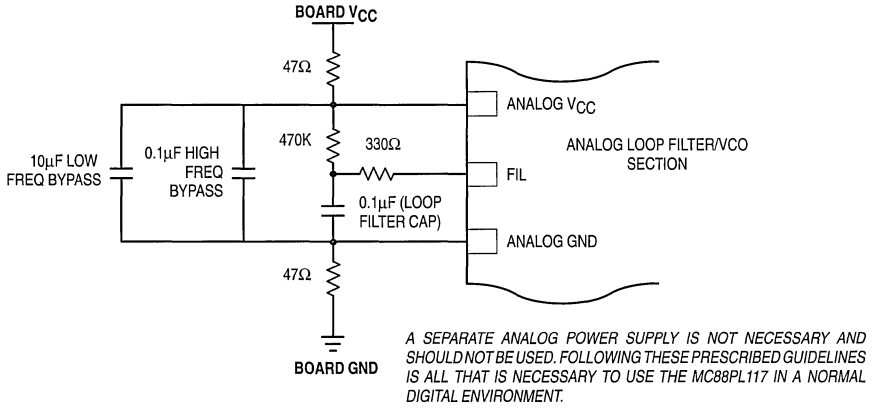


Figure 12. Recommended Loop Filter and Analog Isolation Scheme

Notes Concerning Loop Filter and Board Layout Issues

1 Figure 12 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the FIL pin.

1b The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will minimize the PLL's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100pS phase deviation on the device outputs. A 250mV step deviation on V_{CC} using the recommended filter values should cause no more than a 250pS phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step should cause no more than a 100pS phase deviation. If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 12 is to give the chip additional protection from the power supply and ground plane transients that can occur in a a high frequency, high speed digital system.

1c There are no special requirements set forth for the loop filter resistors (470K and 330Ω). The loop filter capacitor (0.1μF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

2 In addition to the bypass capacitors used in the analog filter of Figure 12, there should be a 0.1μF bypass capacitor between each of the other (digital) nine V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the high current outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the package as possible.

Low Voltage PLL Clock Drivers

Low Voltage Low Skew CMOS PLL Clock Driver, 3-State

MC88LV915T

LOW SKEW CMOS PLL CLOCK DRIVER

The MC88LV915T Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance PC's and workstations.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the MC88LV915T to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88LV915's can lock onto a single reference clock, which is ideal for applications where a central system clock must be distributed synchronously to multiple boards (see Figure 9 on Page 229).

Five "Q" outputs (Q0–Q4) are provided with less than 500 ps skew between their rising edges. The $\overline{Q5}$ output is inverted (180° phase shift) from the "Q" outputs. The 2X_Q output runs at twice the "Q" output frequency, while the Q/2 runs at 1/2 the "Q" frequency.

The VCO is designed to run optimally between 20 MHz and the 2X_Q F_{max} specification. The wiring diagrams in Figure 7 detail the different feedback configurations which create specific input/output frequency relationships. Possible frequency ratios of the "Q" outputs to the SYNC input are 2:1, 1:1, and 1:2.

The FREQ_SEL pin provides one bit programmable divide–by in the feedback path of the PLL. It selects between divide–by–1 and divide–by–2 of the VCO before its signal reaches the internal clock distribution section of the chip (see the block diagram on page 2). In most applications FREQ_SEL should be held high (÷1). If a low frequency reference clock input is used, holding FREQ_SEL low (÷2) will allow the VCO to run in its optimal range (>20MHz).

In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88LV915T in a static "test mode". In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board–level testing (see detailed description on page 11).

Pulling the $\overline{OE}/\overline{RST}$ pin low puts the clock outputs 2X_Q, Q0–Q4, $\overline{Q5}$ and Q/2 into a high impedance state (3–state). After the $\overline{OE}/\overline{RST}$ pin goes back high Q0–Q4, $\overline{Q5}$ and Q/2 will be reset in the low state, with 2X_Q being the inverse of the selected SYNC input. Assuming PLL_EN is low, the outputs will remain reset until the 88LV915 sees a SYNC input pulse.

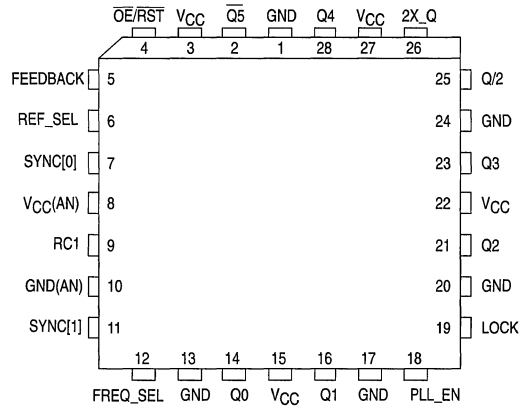
A lock indicator output (LOCK) will go high when the loop is in steady–state phase and frequency lock. The LOCK output will go low if phase–lock is lost or when the PLL_EN pin is low. The LOCK output will go high no later than 10ms after the 88LV915 sees a SYNC signal and full 5V V_{CC}.

Features

- Five Outputs (Q0–Q4) with Output–Output Skew < 500 ps each being phase and frequency locked to the SYNC input
- The phase variation from part–to–part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t_{PD} specification, which defines the part–to–part skew)
- Input/Output phase–locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5MHz – 2X_Q FMAX spec.
- Additional outputs available at 2X and +2 the system "Q" frequency. Also a $\overline{Q}$ (180° phase shift) output available
- All outputs have ±36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL–level compatible. ±88mA I_{OL}/I_{OH} specifications guarantee 50Ω transmission line switching on the incident edge
- Test Mode pin (PLL_EN) provided for low frequency testing. Two selectable CLOCK inputs for test or redundancy purposes. All outputs can go into high impedance (3–state) for board test purposes
- Lock Indicator (LOCK) accuracy indicates a phase–locked state

Yield Surface Modeling and YSM are trademarks of Motorola, Inc.

Pinout: 28–Lead PLCC (Top View)

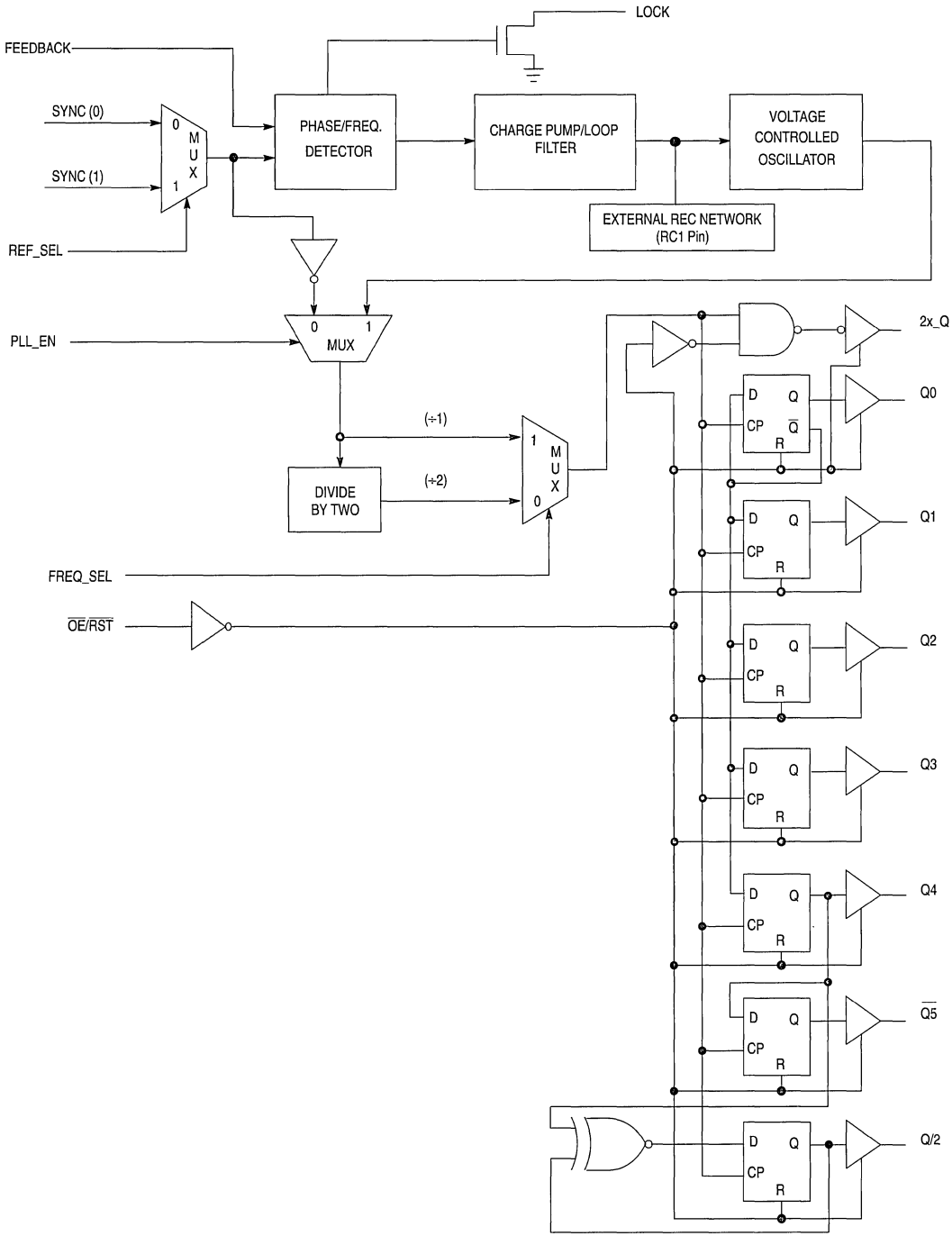


FN SUFFIX
PLASTIC PLCC
CASE 776–02

PIN SUMMARY

Pin Name	Num	I/O	Function
SYNC[0]	1	Input	Reference clock input
SYNC[1]	1	Input	Reference clock input
REF_SEL	1	Input	Chooses reference between sync[0] & Sync[1]
FREQ_SEL	1	Input	Doubles VCO Internal Frequency (low)
FEEDBACK	1	Input	Feedback input to phase detector
RC1	1	Input	Input for external RC network
Q(0–4)	5	Output	Clock output (locked to sync)
$\overline{Q5}$	1	Output	Inverse of clock output
2x_Q	1	Output	2 x clock output (Q) frequency (synchronous)
Q/2	1	Output	Clock output(Q) frequency ÷ 2 (synchronous)
LOCK	1	Output	Indicates phase lock has been achieved (high when locked)
$\overline{OE/RST}$	1	Input	Output Enable/Asynchronous reset (active low)
PLL_EN	1	Input	Disables phase–lock for low freq. testing
V_{CC},GND	11		Power and ground pins (note pins 8, 10 are "analog" supply pins for internal PLL only)

MC88LV915T BLOCK DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Limits	Unit
V_{CC}, AV_{CC}	DC Supply Voltage Referenced to GND	–0.5 to 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, Per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, Per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current Per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	3.3 ±0.3	V
V_{in}	DC Input Voltage	0 to V_{CC}	V
V_{out}	DC Output Voltage	0 to V_{CC}	V
T_A	Ambient Operating Temperature	0 to 70	°C
ESD	Static Discharge Voltage	> 1000	V

DC CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	V_{CC}	Guaranteed Limits	Unit	Condition
V_{IH}	Minimum High Level Input Voltage	3.0 3.3	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{IL}	Minimum Low Level Input Voltage	3.0 3.3	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0 3.3	2.4 2.7	V	V_{IN} = V_{IH} or V_{IL} I_{OH}= –24mA
V_{OL}	Minimum Low Level Output Voltage	3.0 3.3	0.44 0.44	V	V_{IN} = V_{IH} or V_{IL} I_{OH}= 24mA
I_{IN}	Maximum Input Leakage Current	3.6	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	3.6	2.0	mA	V_I = V_{CC} – 2.1V
I_{OLD}	Minimum Dynamic[3] Output Current	3.6	+50	mA	V_{OLD} = 1.25V
I_{OHD}		3.6	–50	mA	V_{OHD} =2.35V
I_{CC}	Maximum Quiescent Supply Current	3.6	TBD	µA	V_I = V_{CC}, GND

1. I_{OL} is +12mA for the $\overline{RST\_OUT}$ output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration 2.0ms, one output loaded at a time.

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$ SYNC Input	Rise/Fall Time, SYNC Input From 0.8V to 2.0V	—	5.0	ns
t_{CYCLE}, SYNC Input	Input Clock Period SYNC Input	$\frac{1}{f_{2X\_Q}/4}$	100	ns
Duty Cycle	Duty Cycle, SYNC Input	50% ± 25%		

FREQUENCY SPECIFICATIONS (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Guaranteed Minimum	Unit
Fmax (2X_Q)	Maximum Operating Frequency, 2X_Q Output	100	MHz
Fmax ('Q')	Maximum Operating Frequency, Q0–Q3 Outputs	50	MHz

NOTE: Maximum Operating Frequency is guaranteed with the 88LV926 in a phase–locked condition.

AC CHARACTERISTICS (T_A =0° C to +70° C, V_{CC} = 3.3V ±0.3V, Load = 50Ω Terminated to $V_{CC}/2$)

Symbol	Parameter		Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.8 to 2.0V)		0.5	2.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
$t_{PULSE\ WIDTH}$ (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}/2$		$0.5t_{CYCLE} - 0.5$ [1]	$0.5t_{CYCLE} + 0.5$ [1]	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
$t_{PULSE\ WIDTH}$ (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5V	40MHz 66MHz 80MHz 100MHz	$0.5t_{CYCLE} - 1.5$ $0.5t_{CYCLE} - 1.0$ $0.5t_{CYCLE} - 1.0$ $0.5t_{CYCLE} - 1.0$	$0.5t_{CYCLE} + 0.5$ $0.5t_{CYCLE} + 0.5$ $0.5t_{CYCLE} + 0.5$ $0.5t_{CYCLE} + 0.5$	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
t_{CYCLE} (2x_Q Output)	Cycle–to–Cycle Variation 2x_Q @ $V_{CC}/2$	40MHz 66MHz 80MHz 100MHz	$t_{CYCLE} - 600ps$ $t_{CYCLE} - 300ps$ $t_{CYCLE} - 300ps$ $t_{CYCLE} - 400ps$	$t_{CYCLE} + 600ps$ $t_{CYCLE} + 300ps$ $t_{CYCLE} + 300ps$ $t_{CYCLE} + 400ps$		
t_{PD} [2] SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)		(With 1MΩ from RC1 to An V_{CC})		ns	
		66MHz 80MHz 100MHz	–1.65 –1.45 –1.25	–1.05 –0.85 –0.65		
t_{SKEWr} [3] (Rising) See Note 4	Output–to–Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)		—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
t_{SKEWf} [3] (Falling)	Output–to–Output Skew Between Outputs Q0–Q4 (Falling Edges Only)		—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
$t_{SKEWall}$ [3]	Output–to–Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling		—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
t_{LOCK} [4]	Time Required to Acquire Phase–Lock From Time SYNC Input Signal is Received		1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL} [5]	Output Enable Time $\overline{OE/RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2		3.0	14	ns	Measured With the PLL_EN Pin Low
t_{PHZ},t_{PLZ} [5]	Output Disable Time $\overline{OE/RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2		3.0	14	ns	Measured With the PLL_EN Pin Low

1. T_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
2. The T_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
3. Under equally loaded conditions and at a fixed temperature and voltage.
4. With V_{CC} fully powered–on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1µF, t_{LOCK} minimum is with C1 = 0.01µF.
5. The t_{PZL}, t_{PHZ}, t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

Applications Information for All Versions

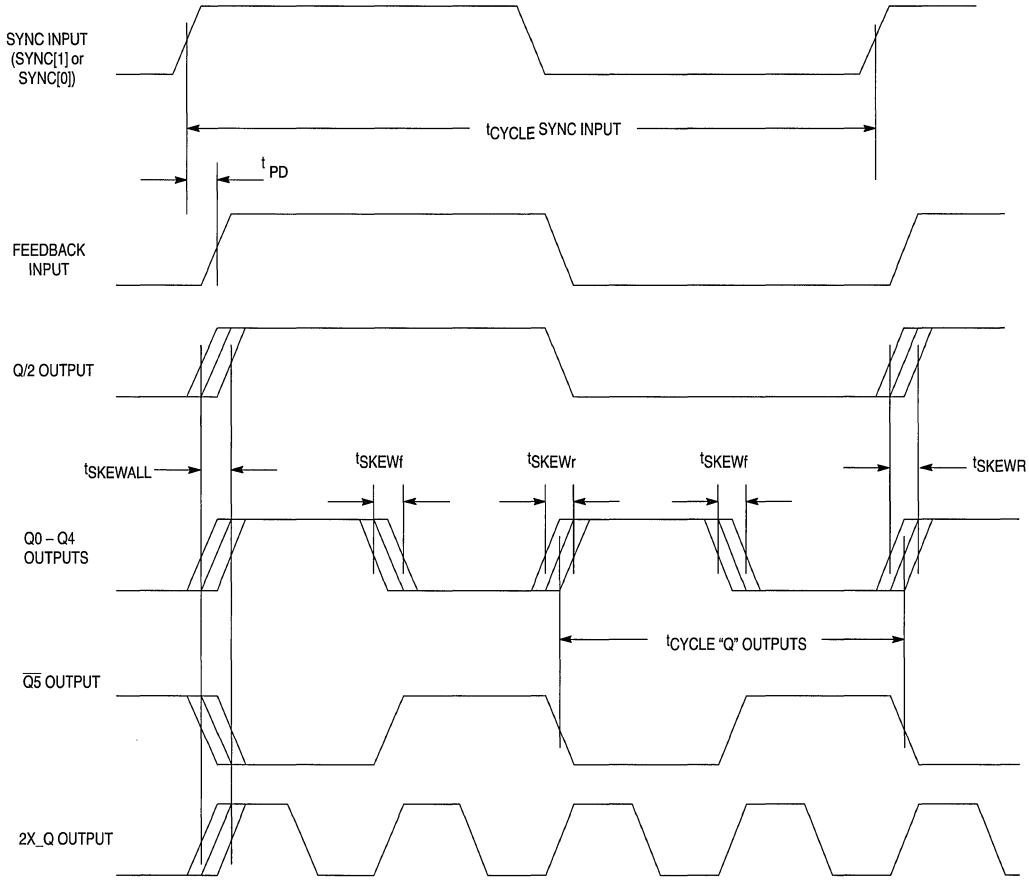
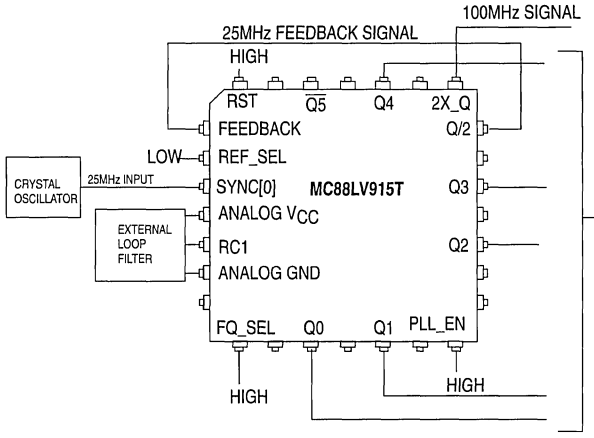


Figure 6. Output/Input Switching Waveforms and Timing Diagrams

(These waveforms represent the hook–up configuration of Figure 7a on page 227)

Timing Notes:

- The MC88LV915T aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
- All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges.All skews are specified as 'windows', not as a ± deviation around a center point.
- If a "Q" output is connected to the FEEDBACK input (this situation is not shown), the "Q" output frequency would match the SYNC input frequency, the 2X_Q output would run at twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency.



1:2 Input to "Q" Output Frequency Relationship

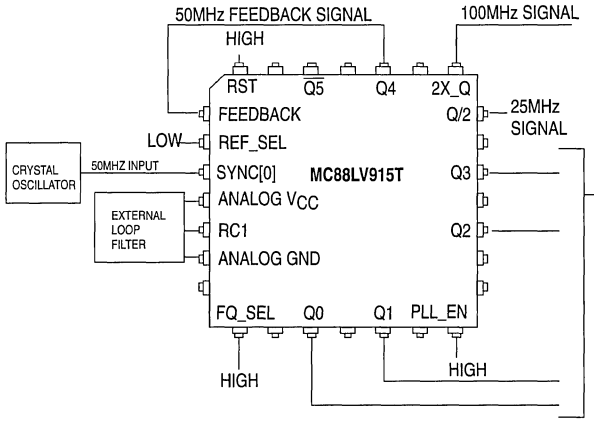
In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The "Q" outputs (Q0–Q4, $\overline{Q5}$) will always run at 2X the Q/2 frequency, and the 2X_Q output will run at 4X the Q/2 frequency.

Allowable Input Frequency Range:

5MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL HIGH)
2.5MHz to (2X_Q FMAX Spec)/8 (for FREQ_SEL LOW)

Note: If the $\overline{OE}/\overline{RST}$ input is active, a pull–up or pull–down resistor isn't necessary at the FEEDBACK pin so it won't when the fed back output goes into 3–state.

Figure 7a. Wiring Diagram and Frequency Relationships With Q/2 Output Feed Back



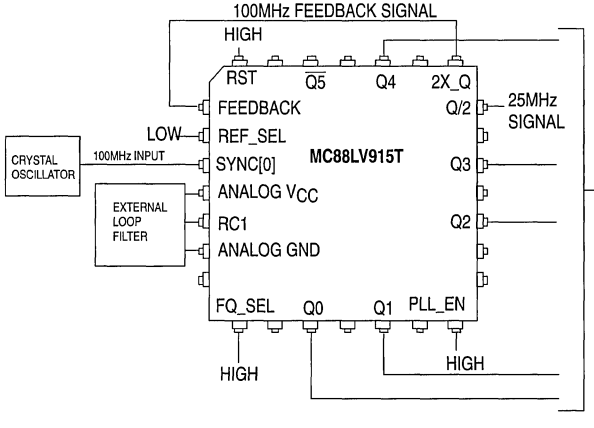
1:1 Input to "Q" Output Frequency Relationship

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the "Q" frequency, and the 2X_Q output will run at 2X the "Q" frequency.

Allowable Input Frequency Range:

10MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL HIGH)
5MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL LOW)

Figure 7b. Wiring Diagram and Frequency Relationships With Q4 Output Feed Back



2:1 Input to "Q" Output Frequency Relationship

In this application, the 2X_Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2X_Q and SYNC, thus the 2X_Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2X_Q frequency, and the "Q" outputs will run at 1/2 the 2X_Q frequency.

Allowable Input Frequency Range:

20MHz to (2X_Q FMAX Spec) (for FREQ_SEL HIGH)
10MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL LOW)

Figure 7c. Wiring Diagram and Frequency Relationships with 2X_Q Output Feed Back

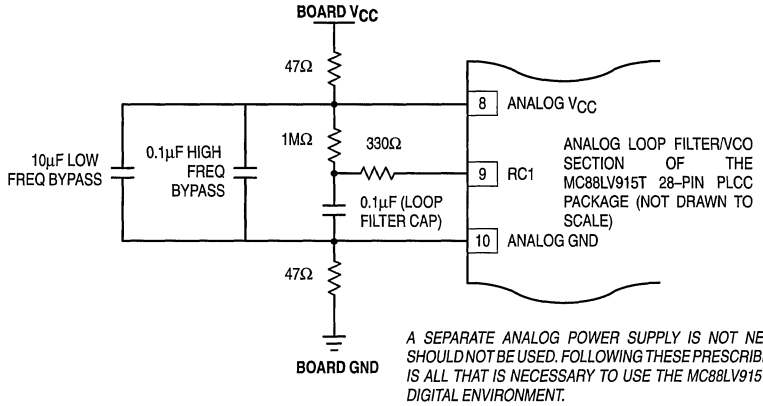


Figure 8. Recommended Loop Filter and Analog Isolation Scheme for the MC88LV915T

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 8 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88LV915T's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100pS phase deviation on the 88LV915T outputs. A 250mV step deviation on V_{CC} using the recommended filter values should cause no more than a 250pS phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step should cause no more than a 100pS phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88LV915T's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 8 is to give the 88LV915T additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (1MΩ and 330Ω). The loop filter capacitor (0.1μF) can be a ceramic chip capacitior, the same as a standard bypass capacitor.

1d. The 1M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 1MΩ resistor provides the correct amount of current injection into the charge pump (2–3μA). For the TFN55, 70 or 100, if the VCO is running below 40MHz, a 1.5MΩ reference resistor should be used (instead of 1MΩ).

2. In addition to the bypass capacitors used in the analog filter of Figure 8, there should be a 0.1μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88LV915T outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88LV915T package as possible.

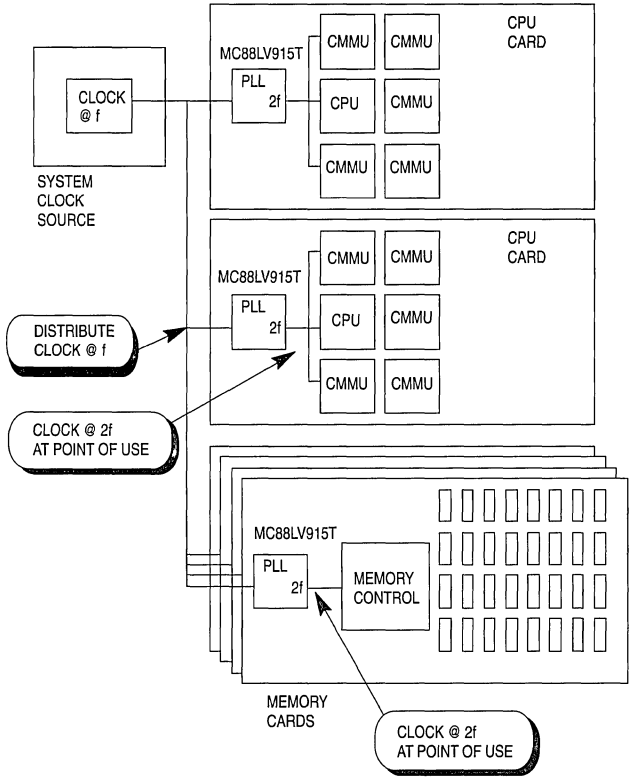


Figure 9. Representation of a Potential Multi–Processing Application Utilizing the MC88LV915T for Frequency Multiplication and Low Board–to–Board Skew

MC88LV915T System Level Testing Functionality

3–state functionality has been added to the 100MHz version of the MC88LV915T to ease system board testing. Bringing the $\overline{OE}/\overline{RST}$ pin low will put all outputs (except for LOCK) into the high impedance state. As long as the PLL_EN pin is low, the Q0–Q4, Q5, and the Q/2 outputs will remain reset in the low state after the $\overline{OE}/\overline{RST}$ until a falling SYNC edge is seen. The 2X_Q output will be the inverse of the SYNC signal in this mode. If the 3–state functionality will be used, a pull–up or pull–down resistor must be tied to the FEEDBACK input pin to prevent it from floating when the fedback output goes into high impedance.

With the PLL_EN pin low the selected SYNC signal is gated directly into the internal clock distribution network, bypassing and disabling the VCO. In this mode the outputs are directly driven by the SYNC input (per the block diagram). This mode can also be used for low frequency board testing.

Note: If the outputs are put into 3–state during normal PLL operation, the loop will be broken and phase–lock will be lost. It will take a maximum of 10mS (tLOCK spec) to regain phase–lock after the $\overline{OE}/\overline{RST}$ pin goes back high.

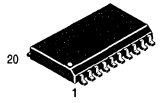
Low Skew CMOS PLL 68060 Clock Driver

MC88LV926

LOW SKEW CMOS PLL 68060 CLOCK DRIVER

The MC88LV926 Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for CISC microprocessor or single processor RISC systems. The $\overline{\text{RST\_IN}}$/$\overline{\text{RST\_OUT}}$(LOCK) pins provide a processor reset function designed specifically for the MC68/EC/LC030/040/060 microprocessor family. To support the 68060 processor, the 88LV926 operates from a 3.3V as well as a 5.0V supply.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple locations on a board. The PLL also allows the MC88LV926 to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency.



DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04

- 2X_Q Output Meets All Requirements of the 50 and 66MHz 68060 Microprocessor PCLK Input Specifications
- Low Voltage 3.3V V_{CC}
- Three Outputs (Q0–Q2) With Output–Output Skew <500ps
- $\overline{\text{CLKEN}}$ Output for Half Speed Bus Applications
- The Phase Variation From Part–to–Part Between SYNC and the 'Q' Outputs Is Less Than 600ps (Derived From the T_{PD} Specification, Which Defines the Part–to–Part Skew)
- SYNC Input Frequency Range From 5MHZ to 2X_Q $F_{Max}/4$
- All Outputs Have ±36mA Drive (Equal High and Low) CMOS Levels
- Can Drive Either CMOS or TTL Inputs. All Inputs Are TTL–Level Compatible
- Test Mode Pin (PLL_EN) Provided for Low Frequency Testing

Three 'Q' outputs (Q0–Q2) are provided with less than 500ps skew between their rising edges. A 2X_Q output runs at twice the 'Q' output frequency. The 2X_Q output is ideal for 68060 systems which require a 2X processor clock input, and it meets the tight duty cycle spec of the 50 and 66MHz 68060. The QCLKEN output is designed to drive the $\overline{\text{CLKEN}}$ input of the 68060 when the bus logic runs at half of the microprocessor clock rate. The QCLKEN output is skewed relative to the 2X_Q output to ensure that $\overline{\text{CLKEN}}$ setup and hold times of the 68060 are satisfied. A Q/2 frequency is fed back internally, providing a fixed 2X multiplication from the 'Q' outputs to the SYNC input. Since the feedback is done internally (no external feedback pin is provided) the input/output frequency relationships are fixed. The $\overline{\text{Q3}}$ output provides an inverted clock output to allow flexibility in the clock tree design.

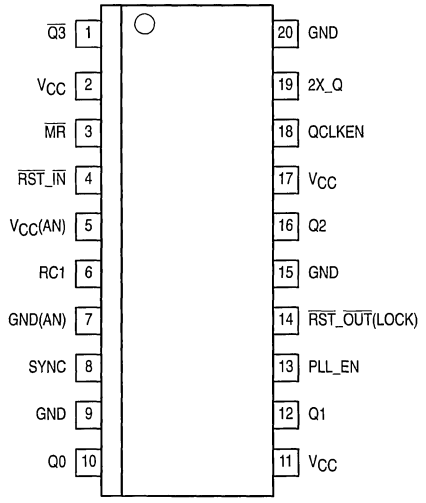
In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88LV926 in a static 'test mode'. In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment.

The $\overline{\text{RST\_OUT}}$(LOCK) pin doubles as a phase–lock indicator. When the $\overline{\text{RST\_IN}}$ pin is held high, the open drain $\overline{\text{RST\_OUT}}$ pin will be pulled actively low until phase–lock is achieved. When phase–lock occurs, the $\overline{\text{RST\_OUT}}$(LOCK) is released and a pull–up resistor will pull the signal high. To give a processor reset signal, the $\overline{\text{RST\_IN}}$ pin is toggled low, and the $\overline{\text{RST\_OUT}}$(LOCK) pin will stay low for 1024 cycles of the 'Q' output frequency after the RST_IN pin is brought back high.

Description of the $\overline{\text{RST\_IN}}$/$\overline{\text{RST\_OUT}}$(LOCK) Functionality

The $\overline{\text{RST\_IN}}$ and $\overline{\text{RST\_OUT}}$(LOCK) pins provide a 68030/040/060 processor reset function, with the $\overline{\text{RST\_OUT}}$ pin also acting as a lock indicator. If the $\overline{\text{RST\_IN}}$ pin is held high during system power–up, the $\overline{\text{RST\_OUT}}$ pin will be in the low state until steady state phase/frequency lock to the input reference is achieved. 1024 'Q' output cycles after phase–lock is achieved the $\overline{\text{RST\_OUT}}$(LOCK) pin will go into a high impedance state, allowing it to be pulled high by an external pull–up resistor (see the AC/DC specs for the characteristics of the $\overline{\text{RST\_OUT}}$(LOCK) pin). If the $\overline{\text{RST\_IN}}$ pin is held low during power–up, the $\overline{\text{RST\_OUT}}$(LOCK) pin will remain low.

Pinout: 20–Lead Wide SOIC Package (Top View)



Description of the RST_IN/RST_OUT(LOCK) Functionality (continued)

After the system start–up is complete and the 88LV926 is phase–locked to the SYNC input signal (RST_OUT high), the processor reset functionality can be utilized. When the RST_IN pin is toggled low (min. pulse width=10nS), RST_OUT(LOCK) will go to the low state and remain there for 1024 cycles of the 'Q' output frequency (512 SYNC cycles). During the time in which the RST_OUT(LOCK) is actively pulled low, all the 88LV926 clock outputs will continue operating correctly and in a locked condition to the SYNC input (clock signals to the 68030/040/060 family of processors must continue while the processor is in reset). A propagation delay after the 1024th cycle RST_OUT(LOCK) goes back to the high impedance state to be pulled high by the resistor.

Power Supply Ramp Rate Restriction for Correct 030/040 Processor Reset Operation During System Start–up

Because the RST_OUT(LOCK) pin is an indicator of phase–lock to the reference source, some constraints must be placed on the power supply ramp rate to make sure the RST_OUT(LOCK) signal holds the processor in reset during system start–up (power–up). With the recommended loop filter values (see Figure 6.) the lock time is approximately 10ms. The phase–lock loop will begin attempting to lock to a reference source (if it is present) when VCC reaches 2V. If the V_{CC} ramp rate is significantly slower than 10ms, then the PLL could lock to the reference source, causing RST_OUT(LOCK) to go high before the 88LV926 and '030/040 processor is fully powered up, violating the processor reset specification. Therefore, if it is necessary for the RST_IN pin to be held high during power–up, the V_{CC} ramp rate must be less than 10mS for proper 68030/040/060 reset operation.

This ramp rate restriction can be ignored if the RST_IN pin can be held low during system start–up (which holds RST_OUT low). The RST_OUT(LOCK) pin will then be pulled back high 1024 cycles after the RST_IN pin goes high.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5*	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40*	pF	V_{CC} = 5.0V
PD_1	Power Dissipation at 33MHz With 50Ω Thevenin Termination	15mW/Output* 90mW/Device	mW	V_{CC} = 5.0V T = 25°C
PD_2	Power Dissipation at 33MHz With 50Ω Parallel Termination to GND	37.5mW/Output* 225mW/Device	mW	V_{CC} = 5.0V T = 25°C

* Value at V_{CC} = 3.3V TBD.

MAXIMUM RATINGS*

Symbol	Parameter	Limits	Unit
V_{CC}, AV_{CC}	DC Supply Voltage Referenced to GND	–0.5 to 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, Per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, Per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current Per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	3.3 ±0.3	V
V_{in}	DC Input Voltage	0 to V_{CC}	V
V_{out}	DC Output Voltage	0 to V_{CC}	V
T_A	Ambient Operating Temperature	0 to 70	°C
ESD	Static Discharge Voltage	> 1500	V

DC CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V)[4]

Symbol	Parameter	V_{CC}	Guaranteed Limits	Unit	Condition
V_{IH}	Minimum High Level Input Voltage	3.0 3.3	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{IL}	Minimum Low Level Input Voltage	3.0 3.3	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0 3.3	2.2 2.5	V	V_{IN} = V_{IH} or V_{IL} I_{OH} –36mA –36mA
V_{OL}	Minimum Low Level Output Voltage	3.0 3.3	0.55 0.55	V	V_{IN} = V_{IH} or V_{IL} I_{OH} +36mA[1] +36mA
I_{IN}	Maximum Input Leakage Current	3.3	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	3.3	2.0[2]	mA	V_I = V_{CC} – 2.1V
I_{OLD}	Minimum Dynamic[3] Output Current	3.3	88	mA	V_{OLD} = 1.0V Max
I_{OHD}		3.3	–88	mA	V_{OHD} = 3.85 Min
I_{CC}	Maximum Quiescent Supply Current	3.3	750	µA	V_I = V_{CC}, GND

1. I_{OL} is +12mA for the $\overline{RST\_OUT}$ output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration 2.0ms, one output loaded at a time.
4. The MC88LV926 can also be operated from a 5.0V supply. V_{OH} output levels will vary 1:1 with V_{CC}, input levels and current specs will be unchanged.

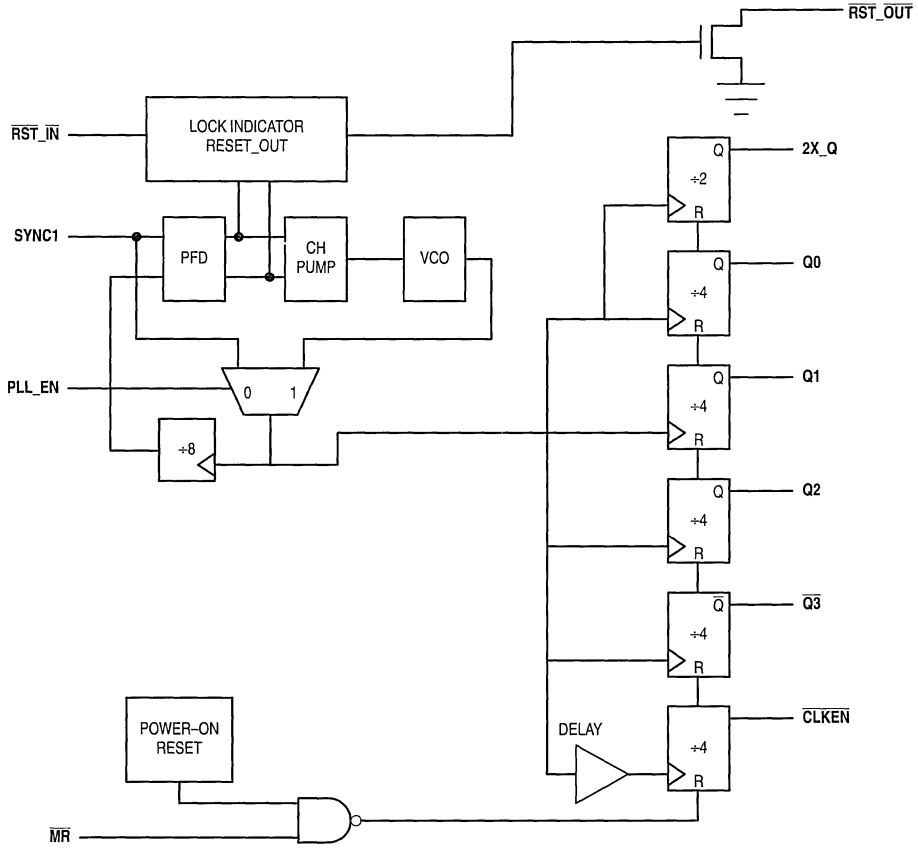


Figure 1. MC88LV926 Logic Block Diagram

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$ SYNC Input	Rise/Fall Time, SYNC Input From 0.8V to 2.0V	—	5.0	ns
t_{CYCLE}, SYNC Input	Input Clock Period SYNC Input	$\frac{1}{f_{2X\_Q/4}}$	200	ns
Duty Cycle	Duty Cycle, SYNC Input	50% ± 25%		

FREQUENCY SPECIFICATIONS (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V or 5.0V ±5%)

Symbol	Parameter	Guaranteed Minimum	Unit
Fmax (2X_Q)	Maximum Operating Frequency, 2X_Q Output	66	MHz
Fmax ('Q')	Maximum Operating Frequency, Q0–Q3 Outputs	33	MHz

Maximum Operating Frequency is guaranteed with the 88LV926 in a phase–locked condition.

AC CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V or 5.0V ±5%)

Symbol	Parameter	Mimimum	Maximum	Unit	Condition
$t_{RISE/FALL}$[1] All Outputs	Rise/Fall Time, into 50Ω Load	0.3	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{RISE/FALL}$[1] 2X_Q Output	Rise/Fall Time into a 50Ω Load	0.5	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{pulse\ width(a)}$[1] (Q0, Q1, Q2, $\overline{Q3}$)	Output Pulse Width Q0, Q1, Q2, Q3 at 1.65V	$0.5t_{cycle}$ – 0.5	$0.5t_{cycle}$ + 0.5	ns	50Ω Load Terminated to $V_{CC}/2$ (See Application Note 3)
$t_{pulse\ width(b)}$[1] (2X_Q Output)	Output Pulse Width 2X_Q at 1.65V	$0.5t_{cycle}$ – 0.5	$0.5t_{cycle}$ + 0.5	ns	50Ω Load Terminated to $V_{CC}/2$ (See Application Note 3)
t_{SKEWr}[1,2] (Rising)	Output–to–Output Skew Between Outputs Q0–Q2 (Rising Edge Only)	—	500	ps	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 5.)
t_{SKEWf}[1,2] (Falling)	Output–to–Output Skew Between Outputs Q0–Q2 (Falling Edge Only)	—	1.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 5.)
$t_{SKEWall}$[1,2]	Output–to–Output Skew 2X_Q, Q0–Q2, $\overline{Q3}$	—	750	ps	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 5.)
t_{SKEW} QCLKEN	Output–to–Output Skew $\overline{QCLKEN}$ to 2X_Q 2X_Q = 50MHz 2X_Q = 66MHz	9.7[6] 7.0[6]	—	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 5.)
t_{LOCK}[3]	Phase–Lock Acquisition Time, All Outputs to SYNC Input	1	10	ms	
t_{PHL} $\overline{MR}$ – Q	Propagation Delay, $\overline{MR}$ to Any Output (High–Low)	1.5	13.5	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
t_{REC}, $\overline{MR}$ to SYNC[5]	Reset Recovery Time rising $\overline{MR}$ edge to falling SYNC edge	9	—	ns	
t_W, $\overline{MR}$ LOW[5]	Minimum Pulse Width, $\overline{MR}$ input Low	5	—	ns	
t_W, $\overline{RST\_IN}$ LOW	Minimum Pulse Width, $\overline{RST\_IN}$ Low	10	—	ns	When in Phase–Lock
t_{PZL}	Output Enable Time $\overline{RST\_IN}$ Low to $\overline{RST\_OUT}$ Low	1.5	16.5	ns	See Application Note 5
t_{PLZ}	Output Enable Time $\overline{RST\_IN}$ High to $\overline{RST\_OUT}$ High Z	1016 'Q' Cycles (508 Q/2 Cycles)	1024 'Q' Cycles (512 Q/2 Cycles)	ns	See Application Note 5

1. These specifications are not tested, they are guaranteed by statistical characterization. See Application Note 1 for a discussion of this methodology.
2. Under equally loaded conditions and at a fixed temperature and voltage.
3. With V_{CC} fully powered–on: t_{CLOCK} Max is with C1 = 0.1µF; t_{LOCK} Min is with C1 = 0.01µF.
4. See Application Note 4 for the distribution in time of each output referenced to SYNC.
5. Specification is valid only when the PLL_EN pin is low.
6. Guaranteed that $\overline{QCLKEN}$ will meet the setup and hold time requirement of the 68060.

Application Notes

1. Several specifications can only be measured when the MC88LV926 is in phase–locked operation. It is not possible to have the part in phase–lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88LV926 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area. Response Surface Modeling (RSM) techniques were used to relate IC performance to the CMOS transistor properties over operation voltage and temperature. IC performance to each specification and fab variation were used in conjunction with Yield Surface Modeling™ (YSM™) methodology to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way, all units passing the ATE test will meet or exceed the non–tested specifications limits.
2. A 470KΩ resistor tied to either Analog V_{CC} or Analog GND, as shown in Figure 2., is required to ensure no jitter is present on the MC88LV926 outputs. This technique causes a phase offset between the SYNC input and the Q0 output, measured at the pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14 lots described in note 1 while the part was in phase–locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V to 2.0V). The phase measurements were made at 1.5V. See Figure 2. for a graphical description.
3. Two specs ($t_{RISE/FALL}$ and t_{PULSE} Width 2X_Q output, see AC Specifications) guarantee that the MC88LV926 meets the 33MHz and 66MHz 68060 P–Clock input specification.

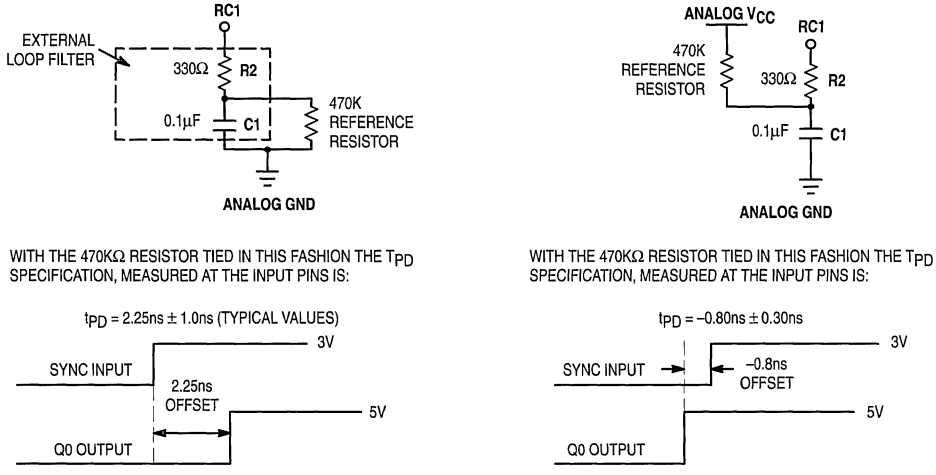


Figure 2. Depiction of the Fixed SYNC to Q0 Offset (t_{PD}) Which Is Present When a 470KΩ Resistor Is Tied to V_{CC} or Ground

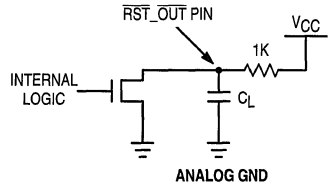


Figure 3. RST_OUT Test Circuit

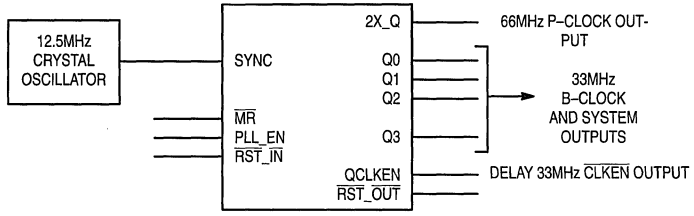


Figure 4. Logical Representation of the MC88LV926 With Input/Output Frequency Relationships

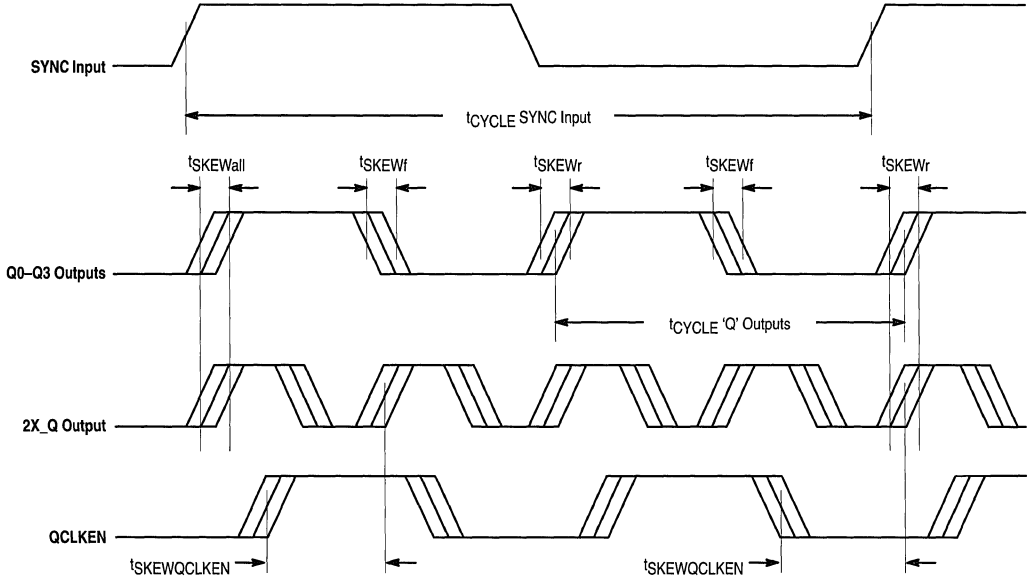


Figure 5. Output/Input Switching Waveforms and Timing Relationships

Timing Notes

1. The MC88LV926 aligns rising edges of the outputs and the SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges. All skews are specified as 'windows', not as a ± deviation around a center point.

The t_{PD} spec includes the full temperature range from 0°C to 70°C and the full V_{CC} range from 3.0V to 3.3V. If the ΔT and ΔV_{CC} is a given system are less than the specification limits, the t_{PD} spec window will be reduced. The t_{PD} window for a given ΔT and ΔV_{CC} is given by the following regression formula:

TBD

5. The $\overline{RST}\_\overline{OUT}$ pin is an open drain N–Channel output. Therefore an external pull–up resistor must be provide to pull up the $\overline{RST}\_\overline{OUT}$ pin when it goes into the high impedance state (after the MC88LV926 is phase–locked to the reference input with $\overline{RST}\_\overline{IN}$ held high or 1024 'Q' cycles after the $\overline{RST}\_\overline{IN}$ pin goes high when the part is locked). In the t_{PLZ} and t_{PZL} specifications, a 1KΩ resistor is used as a pull–up as shown in Figure 3.

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 6. shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will make the 88LV926 PLL insensitive to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100ps phase deviation on the 88LV926 outputs. A 250mV step deviation on V_{CC} using the recommended filter values will cause no more than a 250ps phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step will cause no more than a 100ps phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88LV926's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 6. is to give the 88LV926 additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (470K and 330Ω). The loop filter capacitor (0.1uF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 470K reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 470K resistor provides the correct amount of current injection into the charge pump (2–3μA). If the VCO is running below 40MHz, a 1MΩ reference resistor should be used (instead of 470K).

2. In addition to the bypass capacitors used in the analog filter of Figure 6., there should be a 0.1μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88LV926 outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88LV926 package as possible.

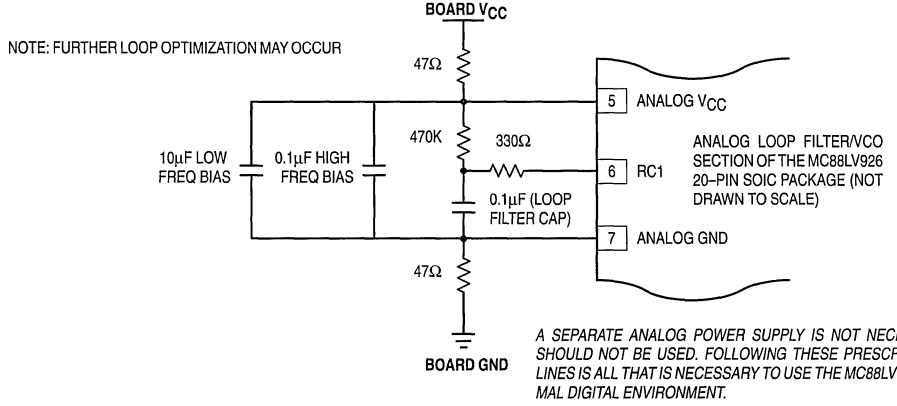


Figure 6. Recommended Loop Filter and Analog Isolation Scheme for the MC88LV926

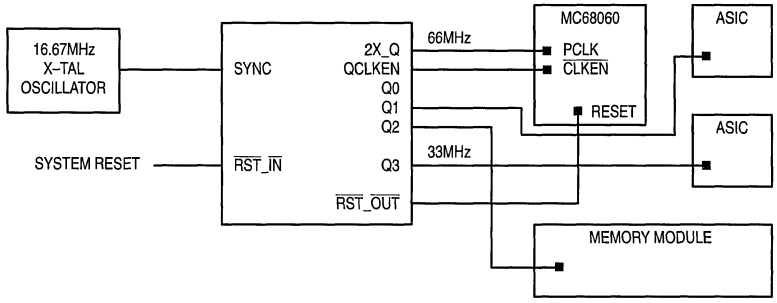


Figure 7. Typical MC88LV926/MC68060 System Configuration

Low Voltage PLL Clock Driver

MPC930
MPC931

LOW VOLTAGE
PLL CLOCK DRIVER

The MPC930/931 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock applications. With output frequencies of up to 150MHz and output skews of 300ps the MPC930/931 is ideal for the most demanding clock distribution designs. The device employs a fully differential PLL design to minimize cycle to cycle and long term jitter. This parameter is of significant importance when the clock driver is providing the reference clock for PLL's on board todays microprocessors and ASiC's. The device offers 6 low skew outputs, and a choice between internal or external feedback. The feedback option adds to the flexibility of the device, providing numerous input to output frequency relationships.

- On–Board Crystal Oscillator (MPC930)
- Differential LVPECL Reference Input (MPC931)
- Fully Integrated PLL
- Output Shut Down Mode
- Output Frequency up to 150MHz
- Compatible with PowerPC™ and Intel Microprocessors
- 32–Lead TQFP Packaging
- Power Down Mode
- ±100ps Typical Cycle–to–Cycle Jitter

FA SUFFIX
32–LEAD TQFP PACKAGE
CASE 873A–02

The MPC930 and MPC931 are very similar in basic functionality, but there are some minor differences. The MPC931 has been optimized for use as a zero delay buffer. In addition to tighter specification limits on the phase offset of the device, a higher speed VCO has been used on the MPC931. The MPC930, on the other hand, is more optimized for use as a clock generator. When choosing between the 930 and 931, pay special attention to the differences in the AC parameters of each device.

The MPC930/931 offers two power saving features for power conscious portable or "green" designs. The power down pin will seemlessly reduce all of the clock rates by one half so that the system will run at half the potential clock rate to extend battery life. The POWER_DN pin is synchronized internally to the slowest output clock rate. This allows the transition in and out of the power–down mode to be output glitch free. In addition, the shut down control pins will turn off various combinations of clock outputs while leaving a subset active to allow for total processor shut down while maintaining system monitors to "wake up" the system when signaled. During shut down, the PLL will remain locked, if internal feedback is used, so that wake up time will be minimized. The shut down and power down pins can be combined for the ultimate in power savings. The Shut_Dn pins are synchronized to the clock internal to the chip to eliminate the possibility of generating runt pulses.

The MPC930/931 devices offer a great deal of flexibility in what is used as the PLL reference. The MPC930 offers an integrated crystal oscillator that allows for an inexpensive crystal to be used as the frequency reference. For more information on the crystal oscillator please refer to the applications section of this data sheet. In those applications where the 930/931 will be used to regenerate clocks from an existing source or as a zero delay buffer, alternative reference clock inputs are provided. Both devices offer an LVCMOS input that can be used as the PLL reference. In addition the MPC931 replaces the crystal oscillator inputs with a differential PECL reference clock input that allows the device to be used in mixed technology clock distribution trees.

An internal feedback divide by 8 of the VCO frequency is compared with the input reference provided by the on–board crystal oscillator when the internal feedback is selected. The on–board crystal oscillator requires no external components other than a series resonant crystal (see Applications Information section for more on crystals). The internal VCO is running at 8x the input reference clock. The outputs can be configured to run at 4x, 2x, 1.25x or 0.66x the input reference frequency. If the external feedback is selected, one of the MPC931's outputs must be connected to the Ext_FB pin. Using the external feedback, numerous input/output frequency relationships can be developed.

The MPC930/931 is fully 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive terminated 50Ω transmission lines. For series terminated applications, each output can drive two 50Ω transmission lines, effectively increasing the fanout to 1:12. The device is packaged in a 32–lead TQFP package to provide the optimum combination of board density and cost.

PowerPC is a trademark of International Business Machines Corporation. Pentium is a trademark of Intel Corporation.

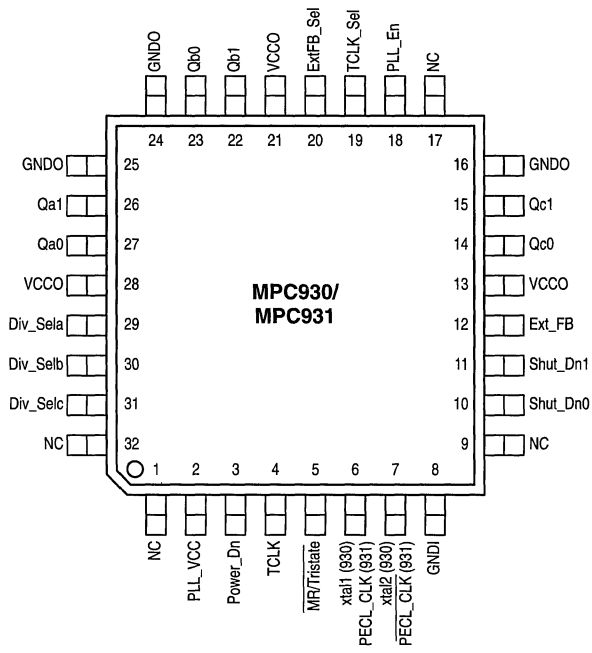


Figure 1. 32–Lead Pinout (Top View)

FUNCTION TABLES

TCLK_Sel	Reference
0	xtal (PECL_CLK)
1	TCLK

PLL_En	PLL Status
0	Test Mode
1	PLL Enabled

ExtFB_Sel	Reference
0	Int. ÷8
1	Ext_FB

Power_Dn	PLL Status
0	VCO/1
1	VCO/2

Div_Sela,b,c	Qa	Qb	Qc
0	÷2	÷2	÷4
1	÷4	÷4	÷6

$\overline{\text{MR}}$/Tristate	PLL Status
0	Disabled
1	Enabled

Shut_Dn1	Shut_Dn0	Div_Seln
0	0	Qb & Qc Low, Qa Toggle
0	1	Qa & Qb Low, Qc Toggle
1	0	Qb Low, Qa & Qc Toggle
1	1	All Toggle

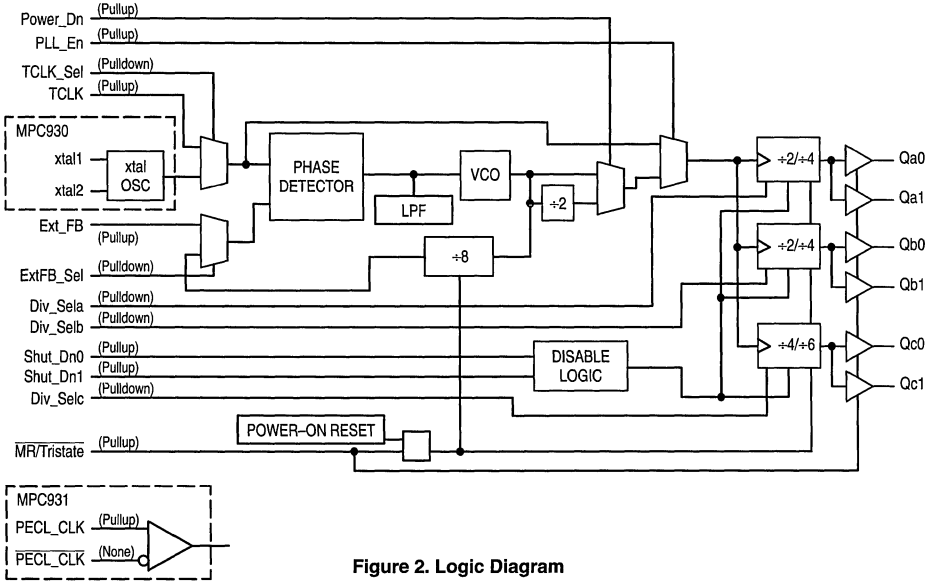


Figure 2. Logic Diagram

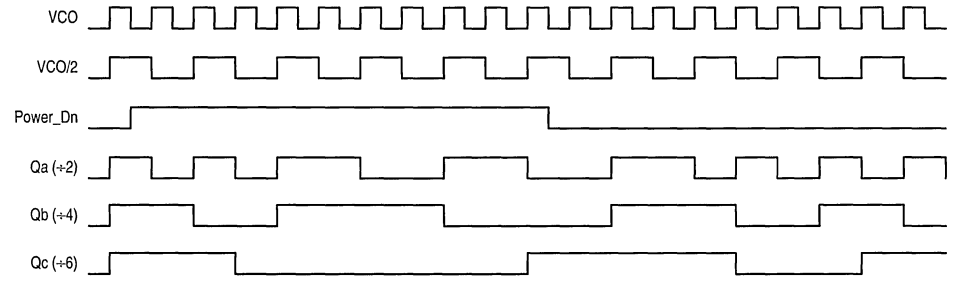


Figure 3. Power_Dn Timing Diagram

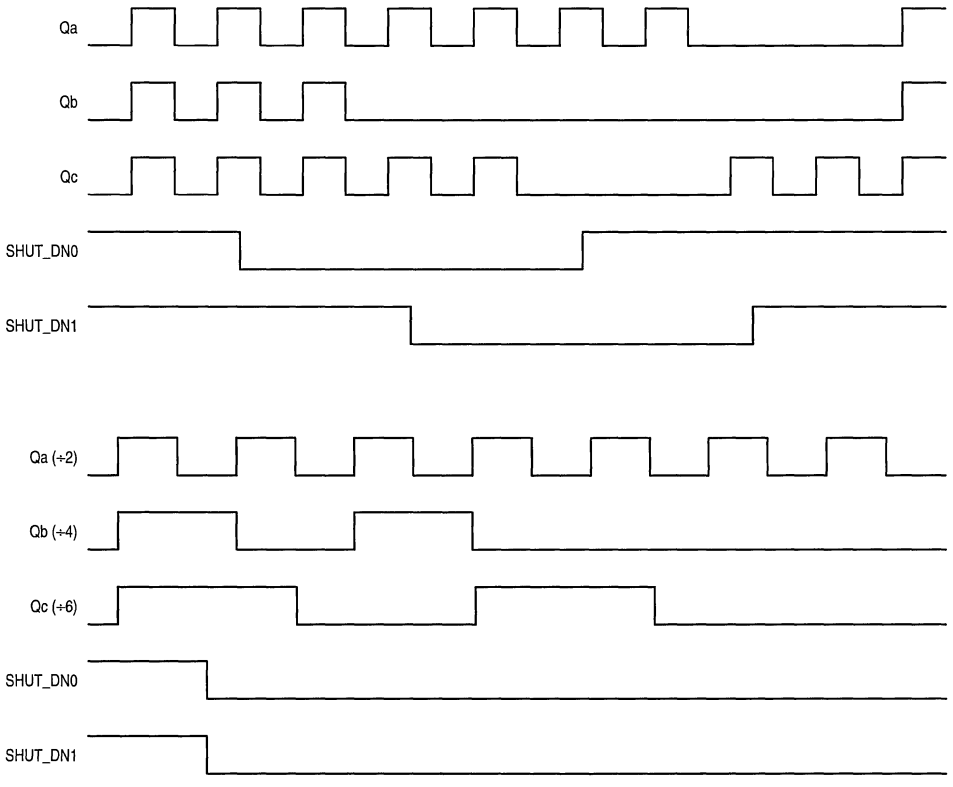


Figure 4. Shut_Dn Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	10	Note 1.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

1. Maximum input reference frequency is limited by the VCO lock range and the feedback divider.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20mA (Note 2.)
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20mA (Note 2.)
I_{IN}	Input Current			±120	µA	Note 3.
I_{CC}	Maximum Core Supply Current		65	85	mA	
I_{CCPLL}	Maximum PLL Supply Current		15	20	mA	
C_{IN}				4	pF	
C_{pd}			25		pF	Per Output

2. The MPC930/931 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull–up/pull–down resistors which affect input current.

MPC930 AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{xtal}	Crystal Oscillator Frequency Range	10		20	MHz	Note 5., Note 7.
f_{ref}	Input Reference Frequency	Note 7.		Note 7.	MHz	Ref = TCLK
t_{os}	Output–to–Output Skew Same Frequency (Note 4.) Diff Frequency Same Frequency Diff Frequency		200 300 300 450	300 400 400 600	ps	$f_{max} \leq$ 100MHz $f_{max} \leq$ 100MHz f_{max} > 100MHz f_{max} > 100MHz
f_{VCO}	VCO Lock Range Power_Dn = 0 Power_Dn = 1	100 50		280 140	MHz	
f_{max}	Maximum Output Frequency Qa, Qb (÷2) Qa, Qb, Qc (÷4) Qc (÷6)			140 80 47	MHz	Note 4.
t_{pd}	TCLK to EXT_FB Delay	–600	–100	400	ps	f_{ref} = 50MHz, FB = ÷4
t_{pw}	Output Duty Cycle (Note 4.)	$t_{CYCLE}/2$ –750	$t_{CYCLE}/2$ ±500	$t_{CYCLE}/2$ +750	ps	
t_r, t_f	Output Rise/Fall Time (Note 4.)	0.1		1.0	ns	0.8 to 2.0V
t_{PLZ}, t_{PHZ}	Output Disable Time	2.0		8.0	ns	50Ω to $V_{CC}/2$
t_{PZL}	Output Enable Time	2.0		10	ns	50Ω to $V_{CC}/2$
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)		±100		ps	Note 6.
t_{lock}	Maximum PLL Lock Time			10	ms	

4. Measured with 50Ω to $V_{CC}/2$ termination.
5. See Applications Info section for more Crystal specifications.
6. See Applications Info section for more jitter information.
7. Input reference frequency is bounded by VCO lock range and feedback divide selection.

MPC931 AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency	Note 11.		Note 11.	MHz	
t_{os}	Output–to–Output Skew Same Frequency (Note 8.) Diff Frequency Same Frequency Diff Frequency		200 300 300 450	300 400 400 600	ps	$f_{max} \leq$ 100MHz $f_{max} \leq$ 100MHz f_{max} > 100MHz f_{max} > 100MHz
f_{VCO}	VCO Lock Range Power_Dn = 0 Power_Dn = 1	200 100		480 240	MHz	
f_{max}	Maximum Output Frequency Qa, Qb (÷2) Qa, Qb, Qc (÷4) Qc (÷6)			150 120 80	MHz	Note 9.
t_{pd}	Reference to EXT_FB Average Delay TCLK PECL_CLK	–150 –400	0 –250	+150 –100	ps	f_{ref} = 50MHz; FB = ÷8; Note 12.
t_{pw}	Output Duty Cycle (Note 8.)	$t_{CYCLE}/2$ –750	$t_{CYCLE}/2$ ±500	$t_{CYCLE}/2$ +750	ps	
t_r, t_f	Output Rise/Fall Time (Note 8.)	0.1		1.0	ns	0.8 to 2.0V
t_{PLZ}, t_{PHZ}	Output Disable Time	2.0		8.0	ns	50Ω to $V_{CC}/2$
t_{PZL}	Output Enable Time	2.0		10	ns	50Ω to $V_{CC}/2$
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)		±100		ps	Note 10.
t_{lock}	Maximum PLL Lock Time			10	ms	

8. Measured with 50Ω to $V_{CC}/2$ termination.
9. f_{max} limited by skew spec. Outputs will generate valid CMOS signals up to 180MHz.
10. See Applications Info section for more jitter information.
11. Input reference frequency is bounded by VCO lock range and feedback divide selection.
12. t_{pd} is specified for 50MHz input reference, the window will shrink/grow proportionally from the minimum limit with shorter/linger reference periods. The t_{pd} does not include jitter.

APPLICATIONS INFORMATION

Programming the MPC930/931

The MPC930/931 clock driver outputs can be configured into several frequency relationships, in addition the external feedback option allows for a great deal of flexibility in establishing unique input to output frequency relationships. The output dividers for the three output groups allows the user to configure the outputs into 1:1, 2:1, 3:1, 3:2 and 3:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 3:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's at VCO/4 and the Qc's at VCO/6. These settings will provide output frequencies with a 3:2:1 relationship.

The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The VCO lock range can be found in the specification tables. The feedback frequency and the Power_Dn pin can be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 25 and 180MHz the MPC930/931 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. Table 2 shows the multiplication factors between the inputs and outputs when the internal feedback option is used. For external feedback Table 1 can be used to determine the multiplication factor, there are too many potential combinations to tabularize the external feedback condition. Figure 5 through Figure 10 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

Table 1. Programmable Output Frequency Relationships (Power_Dn = '0')

INPUTS			OUTPUTS		
Div_Sela	Div_Selb	Div_Selc	Qa	Qb	Qc
0	0	0	VCO/2	VCO/2	VCO/4
0	0	1	VCO/2	VCO/2	VCO/6
0	1	0	VCO/2	VCO/4	VCO/4
0	1	1	VCO/2	VCO/4	VCO/6
1	0	0	VCO/4	VCO/2	VCO/4
1	0	1	VCO/4	VCO/2	VCO/6
1	1	0	VCO/4	VCO/4	VCO/4
1	1	1	VCO/4	VCO/4	VCO/6

Table 2. Input Reference/Output Frequency Relationships (Internal Feedback Only)

INPUTS			OUTPUTS					
			Qa		Qb		Qc	
Div_Sela	Div_Selb	Div_Selc	Power_Dn=0	Power_Dn=1	Power_Dn=0	Power_Dn=1	Power_Dn=0	Power_Dn=1
0	0	0	4x	2x	4x	2x	2x	x
0	0	1	4x	2x	4x	2x	4/3x	2/3x
0	1	0	4x	2x	2x	x	2x	x
0	1	1	4x	2x	2x	x	4/3x	2/3x
1	0	0	2x	x	4x	2x	2x	x
1	0	1	2x	x	4x	2x	4/3x	2/3x
1	1	0	2x	x	2x	x	2x	x
1	1	1	2x	x	2x	x	4/3x	2/3x

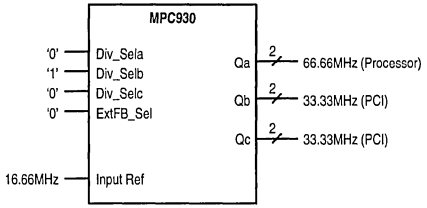


Figure 5. Dual Frequency Configuration

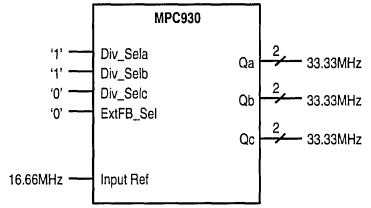


Figure 6. Single Frequency Configuration

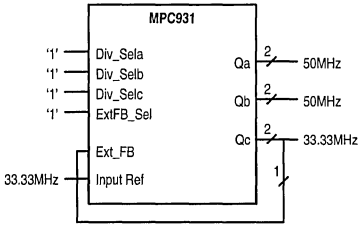


Figure 7. "Zero" Delay Fractional Multiplier

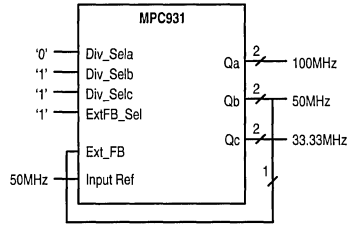


Figure 8. "Zero" Delay Fractional Divider

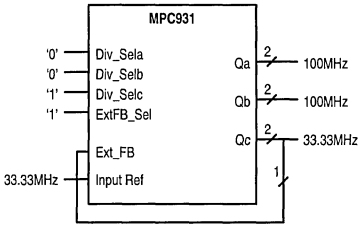


Figure 9. "Zero" Delay Multiply by 3 (50% Duty Cycle)

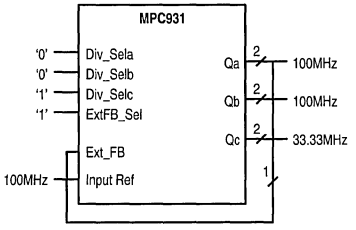


Figure 10. "Zero" Delay Divide by 3 (50% Duty Cycle)

Using the MPC930/931 as a Zero Delay Buffer

The external feedback option of the MPC930/931 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The Tpd of the device is specified in the specification tables. For zero delay buffer applications, the MPC931 is recommended over the MPC930. The MPC931 has been optimized and specified specifically for use as a zero delay buffer.

When used as a zero delay buffer the MPC930/931 will likely be in a nested clock tree application. For these applications the MPC931 offers a LVPECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The MPC931 then can lock onto the LVPECL reference and translate with near zero delay to low skew LVCMOS outputs. Clock trees implemented in this fashion will show significantly tighter skews than trees developed from CMOS fanout buffers.

To minimize part–to–part skew the external feedback option again should be used. The PLL in the MPC931 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only ±150ps, thus for multiple devices under identical configurations the part–to–part skew will be around 850ps (300ps for Tpd variation plus 300ps

output–to–output skew plus 250ps jitter). For devices that are configured differently the differences between the nominal delays must also be accounted for.

When using the MPC931 as a zero delay buffer there is more information which can help minimize the overall timing uncertainty. To fully minimize the specified uncertainty, it is crucial that the relative position of the outputs be known. It is recommended that if all of the outputs are going to be used that the Qc0 output be used as the feedback reference. The Qc0 output lies in the middle of the other outputs with respect to output skew. Therefore it can be assumed that the output to output skew of the device is ±150ps with respect to output Qc0.

There will be some cases where only a subset of the outputs of the MPC931 are required. There is significantly tighter skew performance between outputs on a common bank (i.e., Qa0 to Qa1). The skews between these common bank outputs are outlined in the table below. In general the skews between outputs on a given bank is about a third of the skew between all banks, reducing the skew to a value of 100ps.

Table 3. Within–Bank Skews

Outputs	Relative Skews
Qa0 → Qa1	+35ps, ±50ps
Qb0 → Qb1	–30ps, ±50ps
Qc0 → Qc1	20ps, ±50ps

Jitter Performance of the MPC930/931

With the clock rates of today's digital systems continuing to increase more emphasis is being placed on clock distribution design and management. Among the issues being addressed is system clock jitter and how that affects the overall system timing budget. The MPC930/931 was designed to minimize clock jitter by employing a differential bipolar PLL as well as incorporating numerous power and ground pins in the design. The following few paragraphs will outline the jitter performance of the MPC930/931, illustrate the measurement limitations and provide guidelines to minimize the jitter of the device.

The most commonly specified jitter parameter is cycle–to–cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MPC930/931. As a result different methods are used which approximate cycle–to–cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. If this is not the case the measurement inaccuracy will add significantly to the measured jitter. The oscilloscope cannot collect adjacent pulses, rather it collects data from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce jitter values somewhat larger than if consecutive cycles were measured, therefore, this measurement will represent an upper bound of cycle–to–cycle jitter. Most likely, this is a conservative estimate of the cycle–to–cycle jitter.

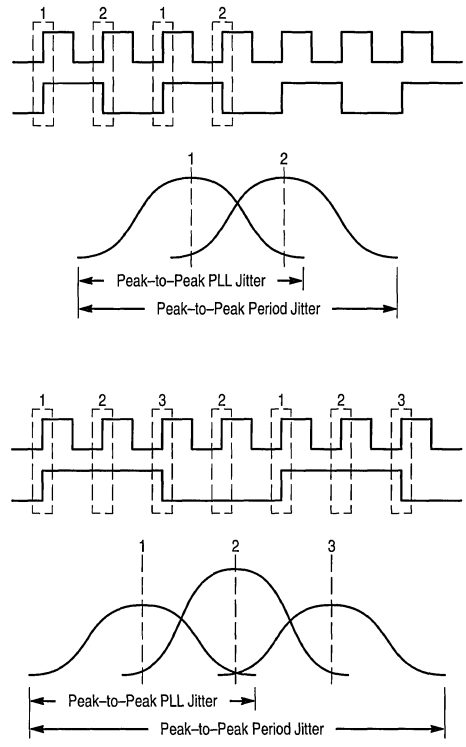
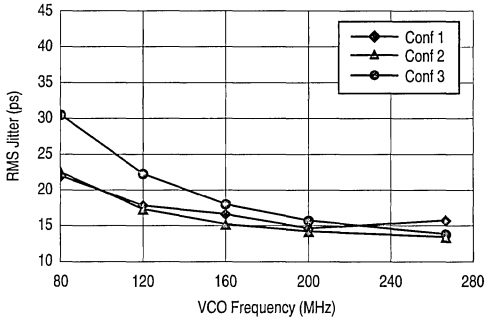


Figure 11. PLL Jitter and Edge Displacement

There are two sources of jitter in a PLL based clock driver, the commonly known random jitter of the PLL and the less intuitive jitter caused by synchronous, different frequency outputs switching. For the case where all of the outputs are switching at the same frequency the total jitter is exactly equal to the PLL jitter. In a device, like the MPC930/931, where a number of the outputs can be switching synchronously but at different frequencies a "multi–modal" jitter distribution can be seen on the highest frequency outputs. Because the output being monitored is affected by the activity on the other outputs it is important to consider what is happening on those other outputs. From Figure 11, one can see for each rising edge on the higher frequency signal the activity on the lower frequency signal is not constant. The activity on the other outputs tends to alter the internal thresholds of the device such that the placement of the edge being monitored is displaced in time. Because the signals are synchronous the relationship is periodic and the resulting jitter is a compilation of the PLL jitter superimposed on the displaced edges. When histograms are plotted the jitter looks like a "multi–modal" distribution as pictured in Figure 11 on page 246. Depending on the size of the PLL jitter and the relative displacement of the edges the "multi–modal" distribution will appear truly "multi–modal" or simply like a "fat" Gaussian distribution. Again note that in the

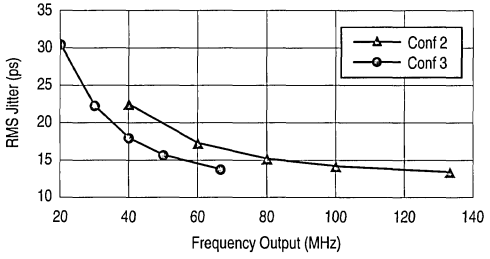
case where all the outputs are switching at the same frequency there is no edge displacement and the jitter is reduced to that of the PLL.

Figure 12 graphically represents the PLL jitter of the MPC930/931. The data was taken for several different output configurations. Because of the relatively few outputs on the MPC930/931, the multimodal distribution is of a second order affect on the 930/931 and can be ignored. As one can see in the figure the PLL jitter is much less dependent on output configuration than on internal VCO frequency. However, for a given VCO frequency, a lower output frequency produces more jitter.



Conf 1 = Qa=÷2, Qb=Qc=÷4
Conf 2 = Qa=÷2, Qb=Qc=Shut Down
Conf 3 = Qa=÷4, Qb=Qc=Shut Down

Figure 12. RMS Jitter versus VCO Frequency
(Qa0 Output)



Conf 2 = Qa=÷2, Qb=Qc=Shut Down
Conf 3 = Qa=÷4, Qb=Qc=Shut Down

Figure 13. RMS Jitter versus Output Frequency
(Qa0 Output)

Finally from the data there are some general guidelines that, if followed, will minimize the output jitter of the device. First and foremost always configure the device such that the VCO runs as fast as possible. This is by far the most critical parameter in minimizing jitter. Second keep the reference frequency as high as possible. More frequent updates at the phase detector will help to reduce jitter. Note that if there is a tradeoff between higher reference frequencies and higher VCO frequency always chose the higher VCO frequency to minimize jitter. The third guideline is to try to shut down outputs that are unused. Minimizing the number of switching outputs will minimize output jitter.

Power Supply Filtering

The MPC930/931 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC930/931 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MPC930/931.

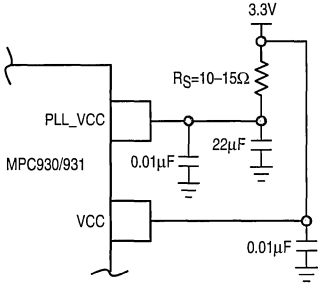


Figure 14. Power Supply Filter

Figure 14 illustrates a typical power supply filter scheme. The MPC930/931 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_VCC pin of the MPC930/931. From the data sheet the I_{PLL_VCC} current (the current sourced through the PLL_VCC pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 14 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC930/931 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the Power Management Features of the MPC930/931

The MPC930/931 clock driver offers two different features that designers can take advantage of for managing power dissipation in their designs. The first feature allows the user to turn off outputs which drive portions of the system which may go idle in a sleep mode. The Shut_Dn pins allow for three different combinations of output shut down schemes. The schemes are summarized in the function tables in the data sheet. The MPC930/931 synchronizes the shut down signals internal to the chip and applies them in a manner which eliminates the possibility of creating runt pulse on the outputs. The device waits for the output to go into the "LOW" state prior to disabling. When the outputs are re–enabled the device waits and re–enables the output such that the transition is synchronous and in the proper phase relationship to the outputs which remained active.

The Power_Dn pin offers another means of implementing power management schemes into a design. To use this feature the device must be set up in its normal operating mode with the Power_Dn pin "LOW", in addition the user must use the internal feedback option. If the external feedback option were used the output frequency reduction would change the feedback frequency and the PLL will lose lock. When the Power_Dn pin is driven "HIGH" the MPC930/931 synchronizes the signal to the internal clock and then seemlessly reduces the frequency of the outputs by one half. The Power_Dn signal is synchronized to the slowest internal VCO clock. It waits until both VCO clocks are in the "LOW" state and then switches from the nominal speed VCO clock to the half speed VCO clock. This will in turn cause the current output pulse to stretch to reflect the reduction in output frequency. When the Power_Dn pin is brought back "LOW" the device will again wait until both of the VCO clocks are "LOW" and then switch to the nominal VCO clock. This will cause the current output pulses, and all successive pulses, to shrink to match the higher output frequency. Both the power up and power down features are illustrated in the timing diagrams of in this data sheet.

Timing diagrams for both of the power management features are shown in Figure 3 and Figure 4 on page 241.

Using the On–Board Crystal Oscillator

The MPC930 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC930/931 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

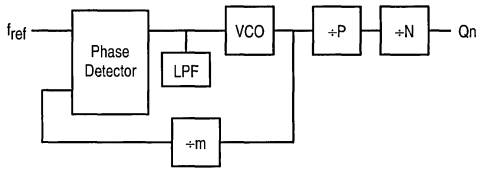
The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC930 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implement–ations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 4. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω Max
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

The MPC930 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal. To determine the crystal required to produce the desired output frequency for an application which utilizes internal feedback the block diagram of Figure 15 should be used. The P and the M values for the MPC930/931 are also included in Figure 15. The M values can be found in the configuration tables included in this applications section.



$$f_{ref} = \frac{f_{VCO}}{m}, \quad f_{VCO} = fQn \cdot N \cdot P$$

$$\therefore f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

m = 8
P = 1 (Power_Dn='0'), 2 (Power_Dn='1')

Figure 15. PLL Block Diagram

For the MPC930 clock driver, the following will provide an example of how to determine the crystal frequency required for a given design.

Given:

Qa = 66.6MHz
Qb = 33.3MHz
Qc = 22.2MHz
Power_Dn = '0'

$$f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

From Table 4

fQc = VCO/6 then N = 6

From Figure 15

m = 8 and P = 1

$$f_{ref} = \frac{22.22 \cdot 6 \cdot 1}{8} = 16.66MHz$$

Driving Transmission Lines

The MPC930/931 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC930/931 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 16 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC930/931 clock driver is effectively doubled due to its capability to drive multiple lines.

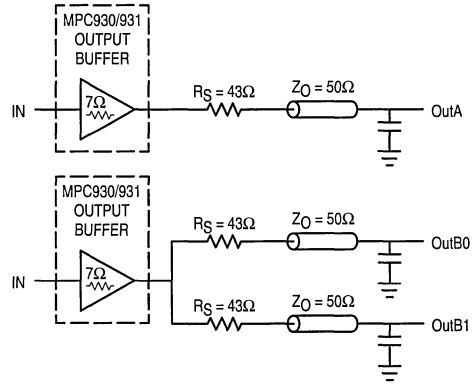


Figure 16. Single versus Dual Transmission Lines

The waveform plots of Figure 17 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC930/931 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC930/931. The output waveform in Figure 17 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS \left(Zo / (Rs + Ro + Zo) \right)$$

Zo = 50Ω || 50Ω
Rs = 43Ω || 43Ω
Ro = 7Ω

$$VL = 3.0 \, (25 / (21.5 + 7 + 25) = 3.0 \, (25 / 53.5)$$
$$= 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

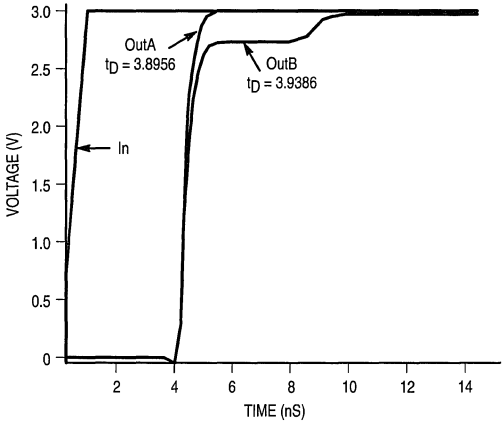
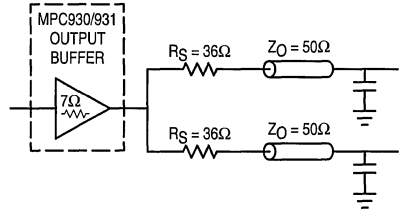


Figure 17. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 18 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

Figure 18. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Advance Information

Low Voltage PLL Clock Driver

MPC932

LOW VOLTAGE PLL CLOCK DRIVER

FA SUFFIX
TQFP PACKAGE
CASE 873A-02

The MPC932 is a 3.3V compatible PLL based clock driver device targetted for zero delay applications. The device provides 6 outputs for driving clock loads plus a single dedicated PLL feedback clock output. The dedicated feedback output gives the user six choices of input multiplcation factors: x1, x1.25, x1.5, x2, x2.5 and x3.

- 6 Low Skew Clock Outputs
- 1 Dedicated PLL Feedback Output
- Individual Output Enable Control
- Fully Integrated PLL
- Output Frequency Up TO 120MHz
- 32–lead TQFP Packaging
- 3.3V VCC
- ±100ps Cycle–Cycle Jitter

The MPC932 provides individual output enable control. The enables are synchronized to the internal clock such that upon assertion the shut down signals will hold the clocks LOW without generating a runt pulse on the outputs. The shut down pins provide a means of powering down certain portions of a system or a means of disabling outputs when the full compliment are not required for a specific design. The shut down pins will disable the outputs when driven LOW. A common shut down pin is provided to disable all of the outputs (except the feedback output) with a single control signal.

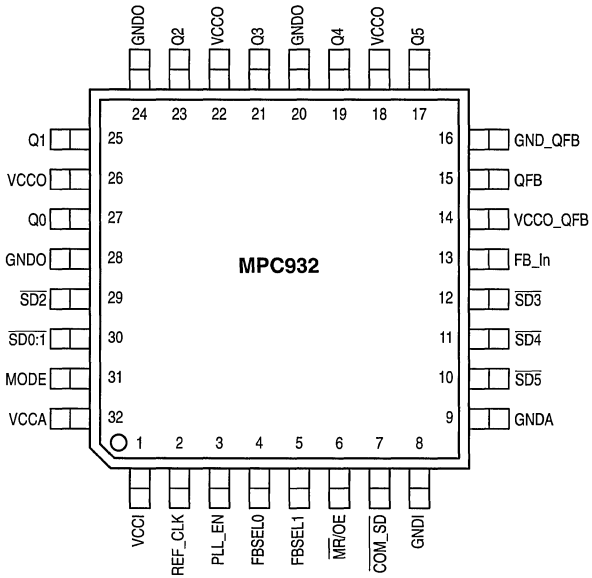
Two feedback select pins are provided to select the multiplication factor of the PLL. The MPC932 provides six multiplication factors: x1, x1.25, x1.5, x2, x2.5 and x3. In the x1.25 and x2.5 modes, the QFB output will not provide a 50% duty cycle. The phase detector of the MPC932 only monitors rising edges of its feedback signals, thus for this function a 50% duty cycle is not required. As the QFB signal can also be used to drive other clocks in a system it is important the user understand that the duty cycle will not be 50%. In the x1 and x1.5 modes the QFB output will produce 50% duty cycle signals.

The MPC932 provides two pins for use in system test and debug operations. The $\overline{MR}$/OE input will force all of the outputs into a high impedance state to allow for back driving the outputs during system test. In addition the PLL_EN pin allows the user to bypass the PLL and drive the outputs directly through the Ref_CLK input. Note the Ref_CLK signal will be routed through the dividers so that it will take several transitions on the Ref_CLK input to create a transition on the outputs.

The MPC932 is fully 3.3V compatible and requires no external loop filter components. All of the inputs are LVCMOS/LVTTL compatible and the outputs produce rail–to–rail 3.3V swings. For series terminated applications each output can drive two series terminated 50Ω transmission lines. For parallel terminated lines the device can drive terminations of 50Ω into VCC/2. The device is packaged in a 32–lead TQFP package to provide the optimum combination of performance, board density and cost.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Pinout: 32-Lead TQFP Package (Top View)



FUNCTION TABLES

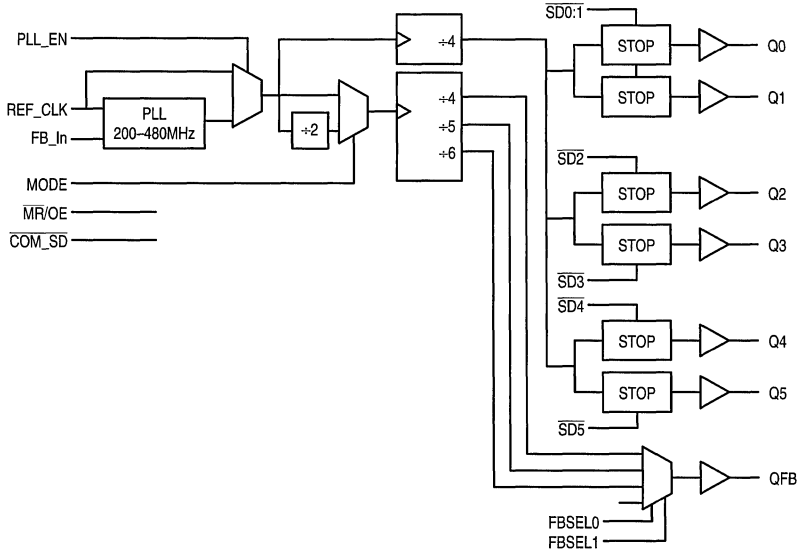
SDn, COM_SD	Qn
0	Held LOW
1	Enabled

PLL_En	PLL Status
0	Test Mode
1	PLL Enabled

MR/OE	PLL Status
0	Disabled
1	Enabled

MODE	FBSEL1	FBSEL0	Qn	QFB
0	0	0	VCO/4	VCO/8
0	0	1	VCO/4	VCO/10
0	1	0	VCO/4	VCO/12
0	1	1	NA	NA
1	0	0	VCO/4	VCO/4
1	0	1	VCO/4	VCO/5
1	1	0	VCO/4	VCO/6
1	1	1	NA	NA

LOGIC DIAGRAM



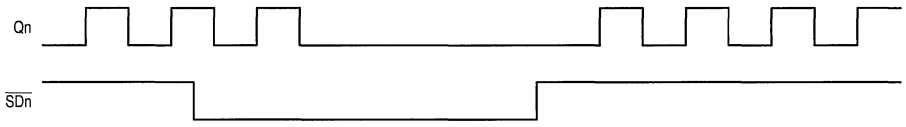


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 1.	Note 1.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

1. Maximum and Maximum input reference frequency is limited by the VCO lock range and the feedback divider.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20mA (Note 2.)
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20mA (Note 2.)
I_{IN}	Input Current			±120	µA	Note 3.
I_{CC}	Maximum Core Supply Current			100	mA	
I_{CCPLL}	Maximum PLL Supply Current		15	20	mA	
C_{IN}				4	pF	
C_{pd}			25		pF	Per Output

2. The MPC932 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull–up/pull–down resistors which affect input current.

MPC932 AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency	Note 6.		Note 6.	MHz	
t_{os}	Output-to-Output Skew		200	300	ps	Note 4.
f_{VCO}	VCO Lock Range	200		480	MHz	
f_{max}	Maximum Output Frequency (÷4) (÷5) (÷6)			120 96 80	MHz	
t_{pd}	Reference to EXT_FB Average Delay TCLK PECL_CLK	X – 150	X	X + 150	ps	f_{ref} = 50MHz; Note 7.
t_{pw}	Output Duty Cycle (Note 4.)	$t_{CYCLE}/2$ –750	$t_{CYCLE}/2$ ±500	$t_{CYCLE}/2$ +750	ps	
t_r, t_f	Output Rise/Fall Time (Note 4.)	0.1		1.0	ns	0.8 to 2.0V
t_{PLZ}, t_{PHZ}	Output Disable Time	2.0		8.0	ns	50Ω to $V_{CC}/2$
t_{PZL}	Output Enable Time	2.0		10	ns	50Ω to $V_{CC}/2$
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)		±100		ps	Note 5.
t_{lock}	Maximum PLL Lock Time			10	ms	

4. Measured with 50Ω to $V_{CC}/2$ termination.
5. See Applications Info section for more jitter information.
6. Input reference frequency is bounded by VCO lock range and feedback divide selection.
7. t_{pd} measurement uses the averaging feature of the oscilliscope to remove the jitter component.

APPLICATIONS INFORMATION

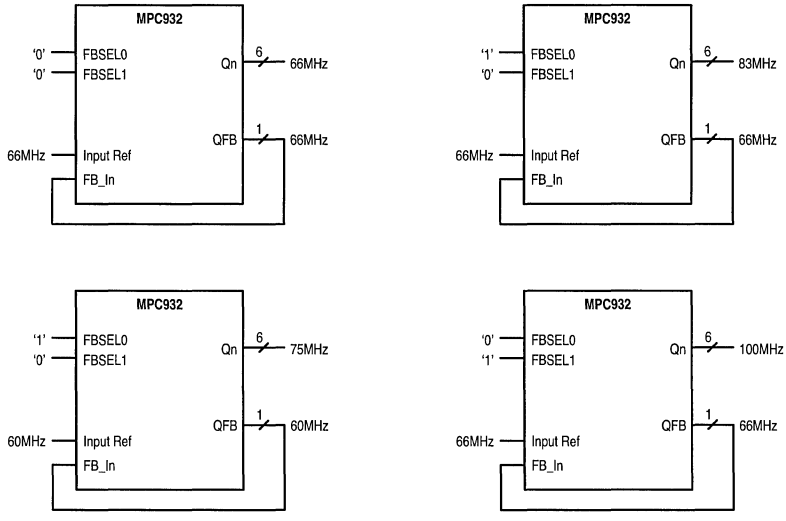
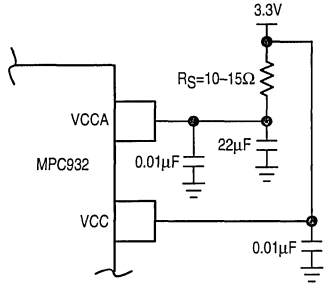


Figure 2. MPC932 Potential Configurations
(Mode = 1)

Power Supply Filtering

The MPC932 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC932 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC932.



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Although the MPC932 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC932 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC932 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 16 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC932 clock driver is effectively doubled due to its capability to drive multiple lines.

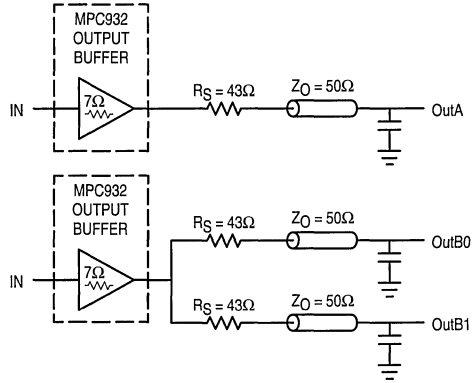


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 17 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC932 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC932. The output waveform in Figure 17 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel

combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / (Rs + Ro + Zo))$$

$Zo = 50\Omega \parallel 50\Omega$
$Rs = 43\Omega \parallel 43\Omega$
$Ro = 7\Omega$

$$VL = 3.0 (25 / (21.5 + 7 + 25) = 3.0 (25 / 53.5)$$
$$= 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

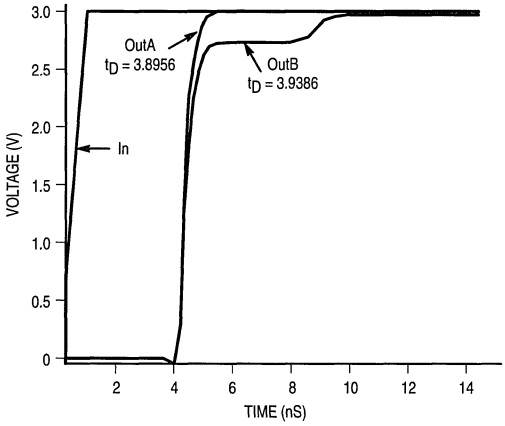
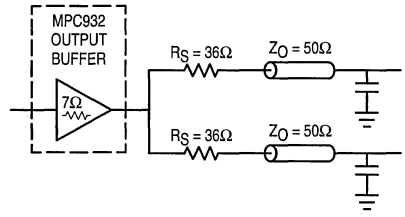


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 18 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Low Voltage PLL Clock Driver

MPC950
MPC951

LOW VOLTAGE
PLL CLOCK DRIVER

The MPC950/951 are 3.3V compatible, PLL based clock driver devices targeted for high performance clock tree designs. With output frequencies of up to 180MHz and output skews of 375ps the MPC950 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle–to–cycle and long term jitter. This parameter is of significant importance when the clock driver is providing the reference clock for PLL's on board today's microprocessors and ASiC's. The devices offer 9 low skew outputs, the outputs are configurable to support the clocking needs of the various high performance microprocessors.

- Fully Integrated PLL
- Oscillator or Crystal Reference Input
- Output Frequency up to 180MHz
- Outputs Disable in High Impedance
- Compatible with PowerPC™, Intel and High Performance RISC Microprocessors
- TQFP Packaging
- Output Frequency Configurable
- ±100ps Typical Cycle–to–Cycle Jitter

FA SUFFIX
32–LEAD TQFP PACKAGE
CASE 873A–02

Two selectable feedback division ratios are available on the MPC950 to provide input reference clock flexibility. The FBSEL pin will choose between a divide by 8 or a divide by 16 of the VCO frequency to be compared with the input reference to the MPC950. The internal VCO is running at either 2x or 4x the high speed output, depending on configuration, so that the input reference will be either one half, one fourth or one eighth the high speed output.

The MPC951 replaces the crystal oscillator and internal feedback of the MPC950 with a differential PECL reference input and an external feedback input. These features allow for the MPC951 to be used as a zero delay, low skew fanout buffer. In addition, the external feedback allows for a wider variety of input–to–output frequency relationships. The MPC951 REF_SEL pin allows for the selection of an alternate LVCMOS input clock to be used as a test clock or to provide the reference for the PLL from an LVCMOS source.

The MPC950 provides an external test clock input for scan clock distribution or system diagnostics. In addition the REF_SEL pin allows the user to select between a crystal input to an on–board oscillator for the reference or to chose a TTL level oscillator input directly. The on–board crystal oscillator requires no external components beyond a series resonant crystal.

Both the MPC950 and MPC951 are fully 3.3V compatible and require no external loop filter components. All inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive terminated 50Ω transmission lines. Select inputs do not have internal pull–up/pull–down resistors and thus must be set externally. If the PECL_CLK inputs are not used, they can be left open. For series terminated 50Ω lines, each of the MPC950/951 outputs can drive two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7mm 32–lead TQFP package to provide the optimum combination of board density and performance.

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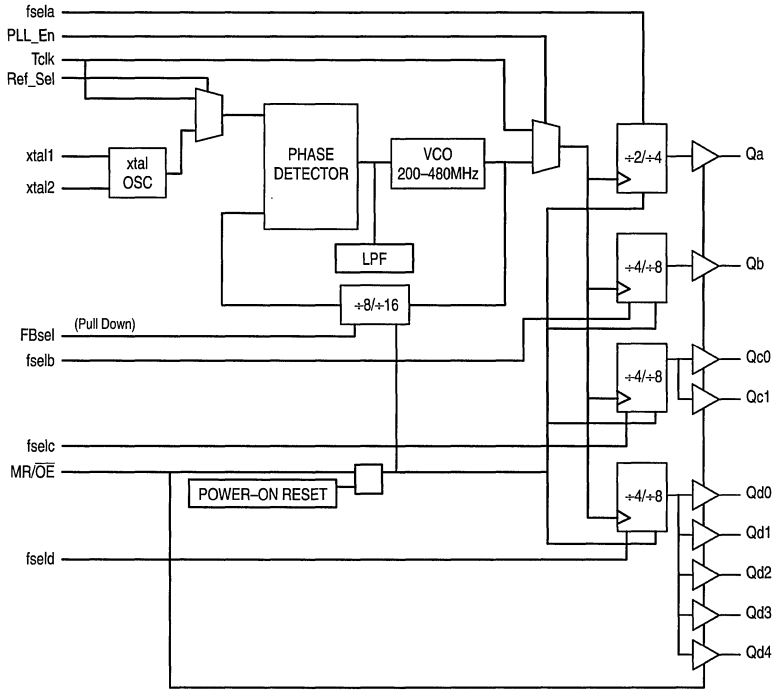
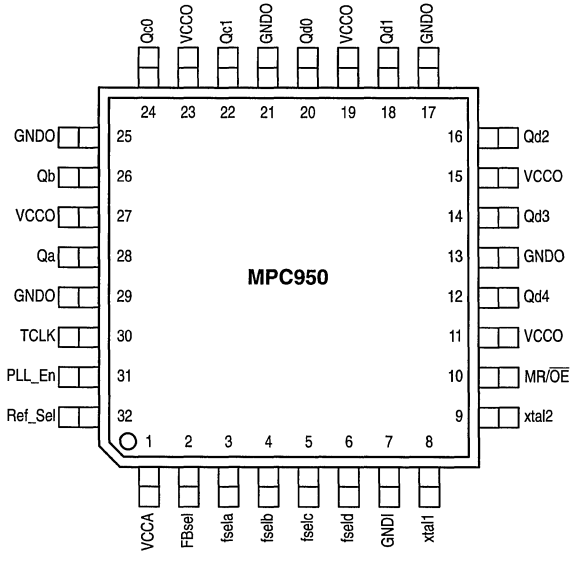
MPC950 LOGIC DIAGRAM





FUNCTION TABLES

Ref_Sel	Function
1	TCLK
0	XTAL_OSC

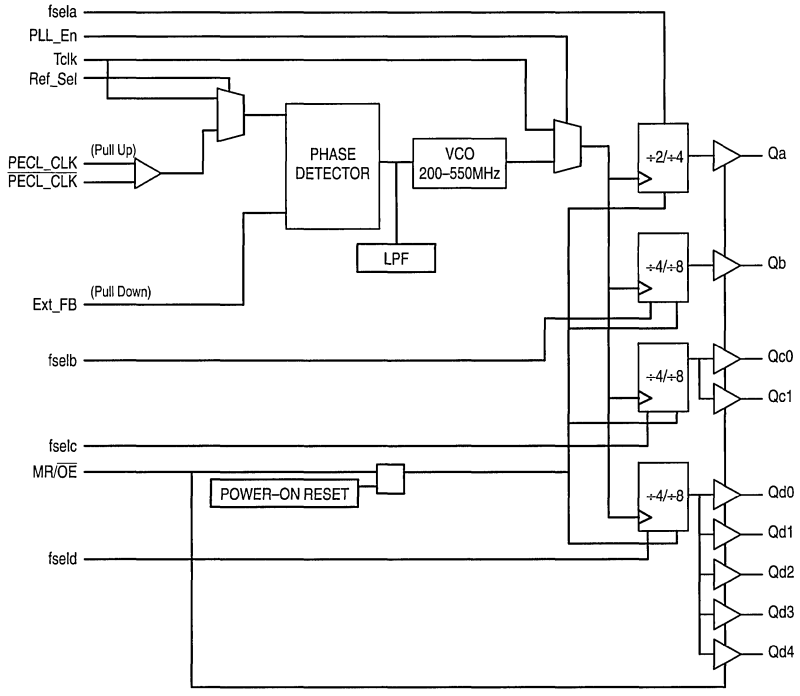
PLL_En	Function
1	PLL Enabled
0	PLL Bypass

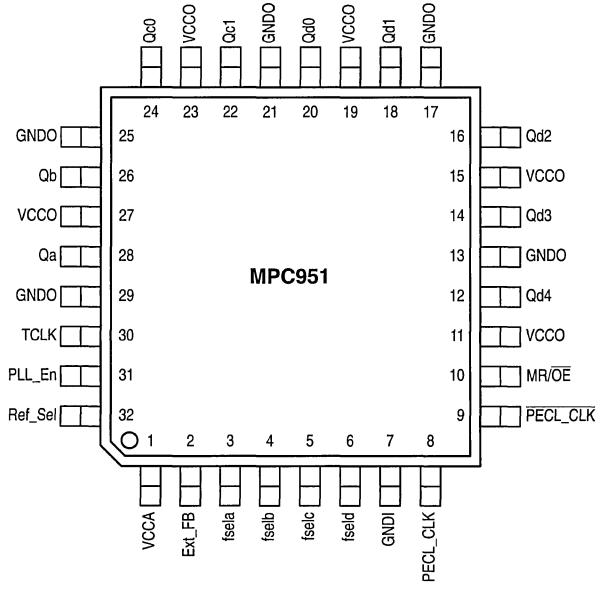
FBsel	Function
1	÷8
0	÷16

MR/$\overline{OE}$	Function
1	Outputs Disabled
0	Outputs Enabled

fseln	Function
1	Qa = ÷4; Qb:d = ÷8
0	Qa = ÷2; Qb:d = ÷4

MPC951 LOGIC DIAGRAM





FUNCTION TABLES

Ref_Sel	Function
1	TCLK
0	PECL_CLK

PLL_En	Function
1	PLL Enabled
0	PLL Bypass

MR/OE	Function
1	Outputs Disabled
0	Outputs Enabled

fseln	Function
1	Qa = ÷4; Qb:d = ÷8
0	Qa = ÷2; Qb:d = ÷4

FUNCTION TABLE – MPC950/951

INPUTS				OUTPUTS				TOTALS		
fsela	fselb	fselc	fseld	Qa(1)	Qb(1)	Qc(2)	Qd(5)	Total 2x	Total x	Total x/2
0	0	0	0	2x	x	x	x	1	8	0
0	0	0	1	2x	x	x	x/2	1	3	5
0	0	1	0	2x	x	x/2	x	1	6	2
0	0	1	1	2x	x	x/2	x/2	1	1	7
0	1	0	0	2x	x/2	x	x	1	7	1
0	1	0	1	2x	x/2	x	x/2	1	2	6
0	1	1	0	2x	x/2	x/2	x	1	3	5
0	1	1	1	2x	x/2	x/2	x/2	1	0	8
1	0	0	0	x	x	x	x	0	9	0
1	0	0	1	x	x	x	x/2	0	4	5
1	0	1	0	x	x	x/2	x	0	7	2
1	0	1	1	x	x	x/2	x/2	0	2	7
1	1	0	0	x	x/2	x	x	0	8	1
1	1	0	1	x	x/2	x	x/2	0	3	6
1	1	1	0	x	x/2	x/2	x	0	6	3
1	1	1	1	x	x/2	x/2	x/2	0	1	8

NOTE: x = $f_{VCO}/4$; 200MHz < f_{VCO} < 480MHz.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	LVCMOS Inputs	2.0		3.6	V	
V_{IL}	Input LOW Voltage	LVCMOS Inputs			0.8	V	
V_{PP}	Peak–to–Peak Input Voltage	PECL_CLK	300		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC}–2.0		V_{CC}–0.6	mV	Note 1.
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH} = –40mA, Note 2.
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 40mA, Note 2.
I_{IN}	Input Current				±120	µA	
C_{IN}	Input Capacitance				4	pF	
C_{pd}	Power Dissipation Capacitance			25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current			90	115	mA	All VCC Pins
I_{CCPLL}	Maximum PLL Supply Current			15	20	mA	VCCA Pin Only

1. V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
2. The MPC950/951 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 1.	Note 1.	MHz	
f_{Xtal}	Crystal Oscillator Frequency	10	25	MHz	Note 2.
f_{refDC}	Reference Input Duty Cycle	25	75	%	

1. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider for the TCLK or PECL_CLK inputs.
2. See Applications Info section for more crystal information.

AC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time		0.10		1.0	ns	0.8 to 2.0V
t_{pw}	Output Duty Cycle		$t_{CYCLE}/2-1000$		$t_{CYCLE}/2+1000$	ps	
$t_{sk(O)}$	Output–to–Output Skews	Same Frequencies		200	375	ps	
		Different Frequencies Qa_{fmax} < 150MHz Qa_{fmax} > 150MHz		325	 500 750		
f_{VCO}	PLL VCO Lock Range	Feedback = VCO/4 Feedback = VCO/8 Feedback = VCO/16	200 200 200		480 480 480	MHz	MPC951 MPC950 or 951 MPC950
f_{max}	Maximum Output Frequency	Qa (÷2) Qa/Qb (÷4) Qb (÷8)			180 120 60	MHz	
t_{pd}	Input to Ext_FB Delay (Note 1.)	TCLK PECL_CLK	50 –950	250 –770	400 –600	ps	f_{ref} = 50MHz Feedback=VCO/8
$t_{PLZ,HZ}$	Output Disable Time				7	ns	
t_{PZL}	Output Enable Time				6	ns	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)			±100		ps	Note 2.
t_{lock}	Maximum PLL Lock Time				10	ms	

1. The specification is guaranteed for the MPC951 only. The t_{pd} window is specified for a 50Mhz input reference clock. The window will enlarge/reduce proportionally from the minimum limits with an increase/decrease of the input reference clock period.
2. See Applications Info section for more jitter information.

APPLICATIONS INFORMATION

Programming the MPC950/951

The MPC950/951 clock driver outputs can be configured into several frequency relationships, in addition the external feedback option of the MPC951 allows for a great deal of flexibility in establishing unique input to output frequency relationships. The output dividers for the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 4:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's and Qc's at VCO/4 and the Qd's at VCO/8. These settings will provide output frequencies with a 4:2:1 relationship.

The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 25 and 180MHz the MPC950/951 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. Table 2 shows the multiplication factors between the inputs and outputs for the MPC950. For external feedback (MPC951) Table 1 can be used to determine the multiplication factor, there are too many potential combinations to tabularize the external feedback condition. Figure 1 through Figure 6 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

Using the MPC951 as a Zero Delay Buffer

The external feedback option of the MPC951 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The input reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

When used as a zero delay buffer the MPC951 will likely be in a nested clock tree application. For these applications the MPC951 offers a LVPECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The MPC951 then can lock onto the LVPECL reference and translate with near zero delay to low skew LVCMOS outputs. Clock trees implemented in this fashion will show significantly tighter skews than trees developed from CMOS fanout buffers.

To minimize part–to–part skew the external feedback option again should be used. The PLL in the MPC951 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only ±200ps, thus for multiple devices under identical configurations the part–to–part skew will be around 1000ps (350ps for Tpd variation plus 350ps output–to–output skew plus 300ps for I/O jitter). By running the devices at the highest possible input reference, this part–to– part skew can be minimized. Higher input reference frequencies will minimize both I/O jitter and t_{pd} variations.

Table 1. Programmable Output Frequency Relationships

INPUTS				OUTPUTS			
fsela	fselb	fselc	fseld	Qa	Qb	Qc	Qd
0	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/2	VCO/4	VCO/4	VCO/8
0	0	1	0	VCO/2	VCO/4	VCO/8	VCO/4
0	0	1	1	VCO/2	VCO/4	VCO/8	VCO/8
0	1	0	0	VCO/2	VCO/8	VCO/4	VCO/4
0	1	0	1	VCO/2	VCO/8	VCO/4	VCO/8
0	1	1	0	VCO/2	VCO/8	VCO/8	VCO/4
0	1	1	1	VCO/2	VCO/8	VCO/8	VCO/8
1	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4
1	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8
1	0	1	0	VCO/4	VCO/4	VCO/8	VCO/4
1	0	1	1	VCO/4	VCO/4	VCO/8	VCO/8
1	1	0	0	VCO/4	VCO/8	VCO/4	VCO/4
1	1	0	1	VCO/4	VCO/8	VCO/4	VCO/8
1	1	1	0	VCO/4	VCO/8	VCO/8	VCO/4
1	1	1	1	VCO/4	VCO/8	VCO/8	VCO/8

Table 2. Input Reference versus Output Frequency Relationships (MPC950 Only)

					FB_Sel = '1'				FB_Sel = '0'			
Config	fsela	fselb	fselc	fseld	Qa	Qb	Qc	Qd	Qa	Qb	Qc	Qd
1	0	0	0	0	4x	2x	2x	2x	8x	4x	4x	4x
2	0	0	0	1	4x	2x	2x	x	8x	4x	4x	2x
3	0	0	1	0	4x	2x	x	2x	8x	4x	2x	4x
4	0	0	1	1	4x	2x	x	x	8x	4x	2x	2x
5	0	1	0	0	4x	x	2x	2x	8x	2x	4x	4x
6	0	1	0	1	4x	x	2x	x	8x	2x	4x	2x
7	0	1	1	0	4x	x	x	2x	8x	2x	2x	4x
8	0	1	1	1	4x	x	x	x	8x	2x	2x	2x
9	1	0	0	0	2x	2x	2x	2x	4x	4x	4x	4x
10	1	0	0	1	2x	2x	2x	x	4x	4x	4x	2x
11	1	0	1	0	2x	2x	x	2x	4x	4x	2x	4x
12	1	0	1	1	2x	2x	x	x	4x	4x	2x	2x
13	1	1	0	0	2x	x	2x	2x	4x	2x	4x	4x
14	1	1	0	1	2x	x	2x	x	4x	2x	4x	2x
15	1	1	1	0	2x	x	x	2x	4x	2x	2x	4x
16	1	1	1	1	2x	x	x	x	4x	2x	2x	2x

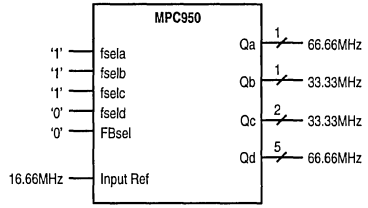


Figure 1. Dual Frequency Configuration

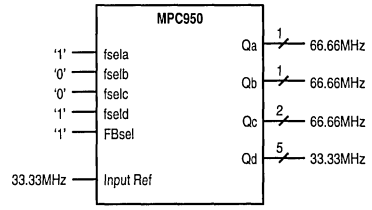


Figure 2. Dual Frequency Configuration

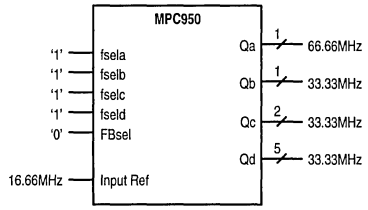


Figure 3. Dual Frequency Configuration

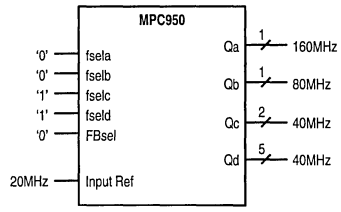


Figure 4. Triple Frequency Configuration

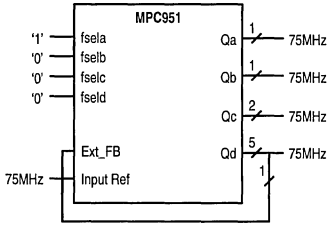


Figure 5. "Zero" Delay Buffer

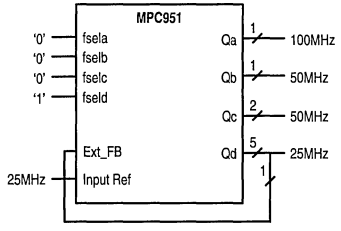


Figure 6. "Zero" Delay Frequency Multiplier

Jitter Performance of the MPC950/951

With the clock rates of today's digital systems continuing to increase more emphasis is being placed on clock distribution design and management. Among the issues being addressed is system clock jitter and how that affects the overall system timing budget. The MPC950/951 was designed to minimize clock jitter by employing a differential bipolar PLL as well as incorporating numerous power and ground pins in the design. The following few paragraphs will outline the jitter performance of the MPC950/951, illustrate the measurement limitations and provide guidelines to minimize the jitter of the device.

The most commonly specified jitter parameter is cycle–to–cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MPC950/951. As a result different methods are used which approximate cycle–to–cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. If this is not the case the measurement inaccuracy will add significantly to the measured jitter. The oscilloscope cannot collect adjacent pulses, rather it collects data from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce jitter values somewhat larger than if consecutive cycles were measured, therefore, this measurement will represent an upper bound of cycle–to–cycle jitter. Most likely, this is a conservative estimate of the cycle–to–cycle jitter.

There are two sources of jitter in a PLL based clock driver, the commonly known random jitter of the PLL and the less intuitive jitter caused by synchronous, different frequency outputs switching. For the case where all of the outputs are

switching at the same frequency the total jitter is exactly equal to the PLL jitter. In a device, like the MPC950/951, where a number of the outputs can be switching synchronously but at different frequencies a "multi–modal" jitter distribution can be seen on the highest frequency outputs. Because the output being monitored is affected by the activity on the other outputs it is important to consider what is happening on those other outputs. From Figure 9, one can see for each rising edge on the higher frequency signal the activity on the lower frequency signal is not constant. The activity on the other outputs tends to alter the internal thresholds of the device such that the placement of the edge being monitored is displaced in time. Because the signals are synchronous the relationship is periodic and the resulting jitter is a compilation of the PLL jitter superimposed on the displaced edges. When histograms are plotted the jitter looks like a "multi–modal" distribution as pictured in Figure 9. Depending on the size of the PLL jitter and the relative displacement of the edges the "multi–modal" distribution will appear truly "multi–modal" or simply like a "fat" Gaussian distribution. Again note that in the case where all the outputs are switching at the same frequency there is no edge displacement and the jitter is reduced to that of the PLL.

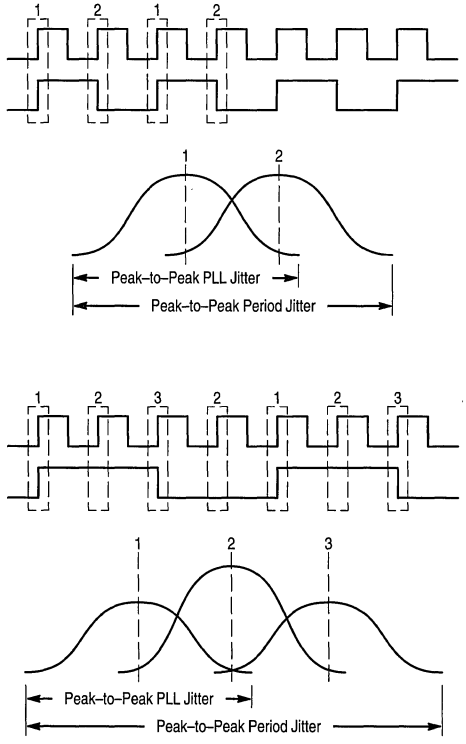
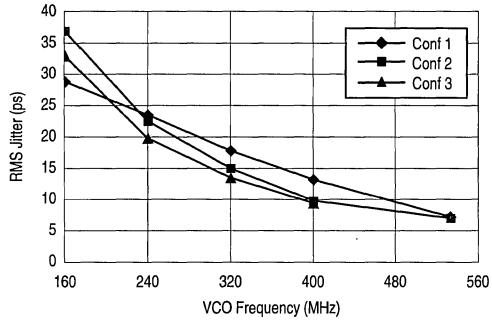


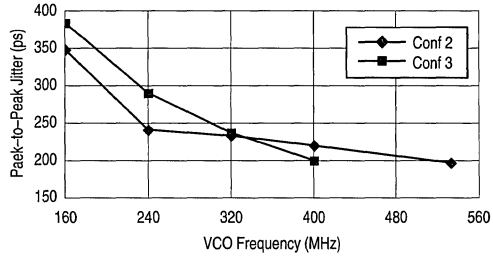
Figure 7. PLL Jitter and Edge Displacement

Figure 10 graphically represents the PLL jitter of the MPC950/951. The data was taken for several different output configurations. By triggering on the lowest frequency output the PLL jitter can be measured for configurations in which outputs are switching at different frequencies. As one can see in the figure the PLL jitter is much less dependent on output configuration than on internal VCO frequency.



Conf 1 = All Outputs at the Same Frequency
Conf 2 = 4 Outputs at X, 5 Outputs at X/2
Conf 3 = 1 Output at X, 8 Outputs at X/4

Figure 8. RMS PLL Jitter versus VCO Frequency



Conf 2 = 4 Outputs at X, 5 Outputs at X/2
Conf 3 = 1 Output at X, 8 Outputs at X/4

Figure 9. Peak–to–Peak Period Jitter versus VCO Frequency

Two different configurations were chosen to look at the period displacement caused by the switching outputs. Configuration 3 is considered worst case as the "trimodal" distribution (as pictured in Figure 9) represents the largest spread between distribution peaks. Configuration 2 is considered a typical configuration with half the outputs at a high frequency and the remaining outputs at one half the high frequency. For these cases the peak–to–peak numbers are reported in Figure 11 as the sigma numbers are useless because the distributions are not Gaussian. For situations where the outputs are synchronous and switching at different frequencies the measurement technique described here is insufficient to use for establishing guaranteed limits. Other techniques are currently being investigated to identify a more accurate and repeatable measurement so that guaranteed

limits can be provided. The data generated does give a good indication of the general performance, a performance that in most cases is well within the requirements of today's microprocessors.

Finally from the data there are some general guidelines that, if followed, will minimize the output jitter of the device. First and foremost always configure the device such that the VCO runs as fast as possible. This is by far the most critical parameter in minimizing jitter. Second keep the reference frequency as high as possible. More frequent updates at the phase detector will help to reduce jitter. Note that if there is a tradeoff between higher reference frequencies and higher VCO frequency always chose the higher VCO frequency to minimize jitter. The third guideline may be the most difficult, and in some cases impossible, to follow. Try to minimize the number of different frequencies sourced from a single chip. The fixed edge displacement associated with the switching noise in most cases nearly doubles the "effective" jitter of a high speed output.

Power Supply Filtering

The MPC950/951 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC950/951 provides separate power supplies for the output buffers (VCCO) and the phase–locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC950/951.

Figure 10 illustrates a typical power supply filter scheme. The MPC950/951 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC950/951. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 10 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

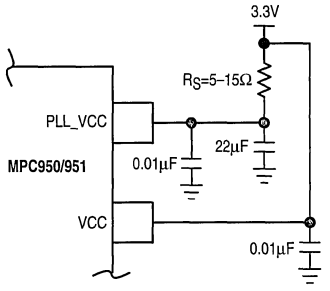


Figure 10. Power Supply Filter

Although the MPC950/951 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the On–Board Crystal Oscillator

The MPC950/951 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC950/951 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

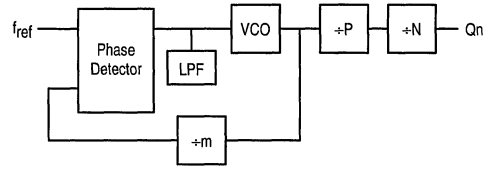
The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC950/951 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 3. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150ppm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω Max
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

The MPC950/951 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal. To determine the crystal required to produce the desired output frequency for an application which utilizes internal feedback the block diagram of Figure 11 should be used. The P and the M values for the MPC950/951 are also included in Figure 11. The M values can be found in the configuration tables included in this applications section.



$$f_{ref} = \frac{f_{VCO}}{m}, \quad f_{VCO} = fQn \cdot N \cdot P$$

$$\therefore f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

m = 8 (FBsel = '1'), 16(FBsel = '0')
P = 1

Figure 11. PLL Block Diagram

For the MPC950/951 clock driver, the following will provide an example of how to determine the crystal frequency required for a given design.

Given:

Qa = 160MHz
Qb = 80MHz
Qc = 40MHz
Qd = 40MHz
FBSel = '0'

$$f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

From Table 3

fQd = VCO/8 then N = 8 OR fQa = VCO/2 then N = 2

From Figure 11

m = 16 and P = 1

$$f_{ref} = \frac{40 \cdot 8 \cdot 1}{16} = 20MHz \text{ OR } \frac{160 \cdot 2 \cdot 1}{16} = 20MHz$$

Driving Transmission Lines

The MPC950/951 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can

be driven by each output of the MPC950/951 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 12 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC950/951 clock driver is effectively doubled due to its capability to drive multiple lines.

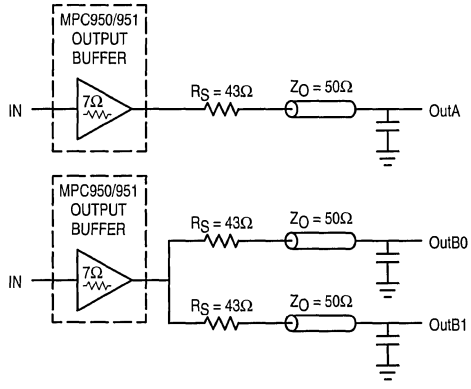


Figure 12. Single versus Dual Transmission Lines

The waveform plots of Figure 13 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC950/951 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC950/951. The output waveform in Figure 13 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / (Rs + Ro + Zo))$$

$Zo = 50\Omega \parallel 50\Omega$
$Rs = 43\Omega \parallel 43\Omega$
$Ro = 7\Omega$

$$VL = 3.0 (25 / (21.5 + 7 + 25) = 3.0 (25 / 53.5)$$
$$= 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

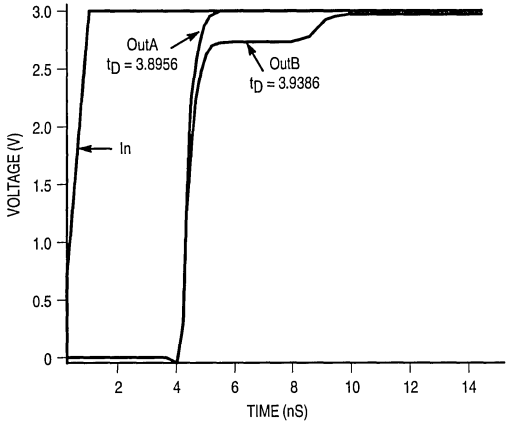
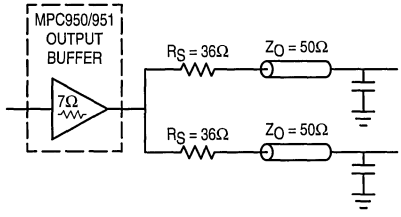


Figure 13. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 14 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

Figure 14. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Low Voltage PLL Clock Driver

MPC952

LOW VOLTAGE PLL CLOCK DRIVER

FA SUFFIX
TQFP PACKAGE
CASE 873A-02

The MPC952 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree applications. The device features a fully integrated PLL with no external components required. With output frequencies of up to 180MHz and eleven low skew outputs the MPC952 is well suited for high performance designs. The device employs a fully differential PLL design to optimize jitter and noise rejection performance. Jitter is an increasingly important parameter as more microprocessors and ASiC's are employing on chip PLL clock distribution.

- Fully Integrated PLL
- Output Frequency up to 180MHz
- High Impedance Disabled Outputs
- Compatible with PowerPC™, Intel and High Performance RISC Microprocessors
- Output Frequency Configurable
- TQFP Packaging
- ±100ps Cycle–to–Cycle Jitter

The MPC952 features three banks of individually configurable outputs. The banks contain 5 outputs, 4 outputs and 2 outputs. The internal divide circuitry allows for output frequency ratios of 1:1, 2:1, 3:1 and 3:2:1. The output frequency relationship is controlled by the fsel frequency control pins. The fsel pins as well as the other inputs are LVCMOS/LVTTL compatible inputs.

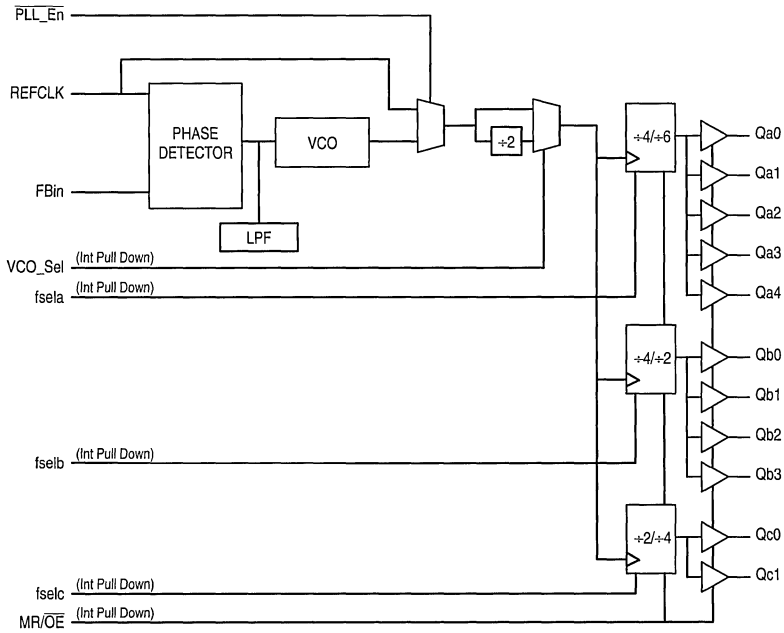
The MPC952 uses external feedback to the PLL. This features allows for the use of the device as a "zero delay" buffer. Any of the eleven outputs can be used as the feedback to the PLL. The VCO_Sel pin allows for the choice of two VCO ranges to optimize PLL stability and jitter performance. The MR/$\overline{OE}$ pin allows the user to force the outputs into high impedance for board level test.

For system debug the PLL of the MPC952 can be bypassed. When forced to a logic HIGH, the PLLEN input will route the signal on the RefClk input around the PLL directly to the internal dividers. Because the signal is routed through the dividers, it may take several transitions of the RefClk to affect a transition on the outputs. This features allows a designer to single step the design for debug purposes.

The outputs of the MPC952 are LVCMOS outputs. The outputs are optimally designed to drive terminated transmission lines. For applications using series terminated transmission lines each MPC952 output can drive two lines. This capability provides an effective fanout of 22, more than enough clocks for most clock tree designs. For more information on driving transmission lines consult the applications section of this data sheet.

PowerPC is a trademark of International Business Machines Corporation. Pentium is a trademark of Intel Corporation.

Figure 1. MPC952 Logic Diagram



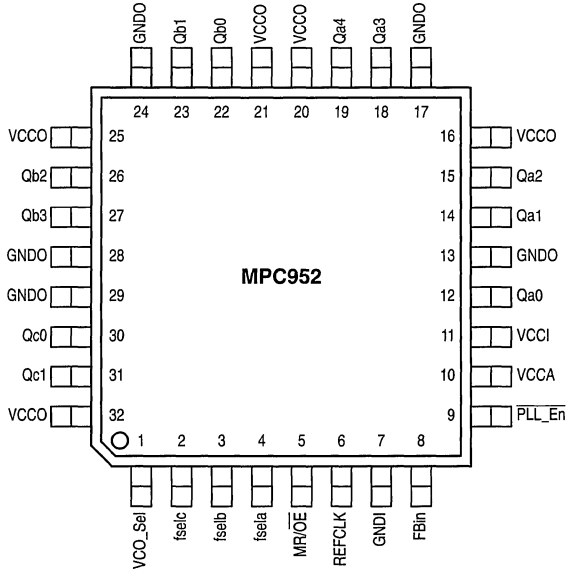


Figure 2. 32–Lead Pinout (Top View)

FUNCTION TABLES

fsela	Qan	fselb	Qbn	fselc	Qcn
0	÷4	0	÷4	0	÷2
1	÷6	1	÷2	1	÷4

Control Pin	Logic '0'	Logic '1'
VCO_Sel	fVCO	fVCO/2
MR/$\overline{OE}$	Output Enable	High Z
$\overline{PLL\_En}$	Enable PLL	Disable PLL

Pin Name	Description
VCCA	PLL Power Supply
VCCO	Output Buffer Power Supply
VCCI	Internal Core Logic Power Supply
GNDI	Internal Ground
GNDO	Output Buffer Ground

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20mA (Note 1.)
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20mA (Note 1.)
I_{IN}	Input Current			±120	µA	Note 2.
C_{IN}	Input Capacitance		2.7	4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	
I_{CC}	Maximum Quiescent Supply Current			160	mA	Total ICC Static Current
I_{CCA}	PLL Supply Current		15	20	mA	

1. The MPC952 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pull–up, pull–down resistors which affect input current.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 3.	Note 3.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

3. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time (Note 4.)		0.10		1.0	ns	0.8 to 2.0V
t_{pw}	Output Pulse Width (Note 4.)		$t_{CYCLE}/2$ –750	$t_{CYCLE}/2$ ±500	$t_{CYCLE}/2$ +750	ps	
t_{os}	Output-to-Output Skew (Note 4.)	Excluding Qa0 All Outputs All Outputs			350 450 550	ps	Same Frequencies Same Frequencies Different Frequencies
f_{VCO}	PLL VCO Lock Range	Feedback = VCO/4 Feedback = VCO/6 Feedback = VCO/8 Feedback = VCO/12	200 200 200 200		480 480 480 480	MHz	VCO_Sel = 0 VCO_Sel = 0 VCO_Sel = 0 VCO_Sel = 0
f_{max}	Maximum Output Frequency	Qc,Qb (÷2) Qa,Qb,Qc (÷4) Qa (÷6)	180 120 80			MHz	(Note 4.)
t_{pd}	REFCLK to FBIN Delay		–200	0	200	ps	Notes 4., 5.
t_{PLZ}, t_{PHZ}	Output Disable Time		2		8	ns	50Ω to $V_{CC}/2$
t_{PZL}, t_{PLH}	Output Enable Time		2		10	ns	50Ω to $V_{CC}/2$
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)			±100		ps	
t_{lock}	Maximum PLL Lock Time				10	ms	

4. 50Ω to $V_{CC}/2$.
5. t_{pd} is specified for 50MHz input ref, the window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC952 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

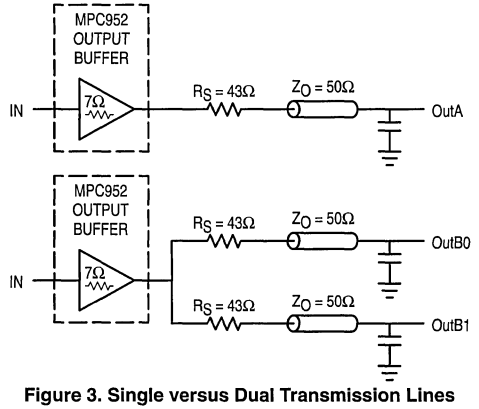


Figure 3. Single versus Dual Transmission Lines

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC952 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC952 clock driver is effectively doubled due to its capability to drive multiple lines.

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC952 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC952. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS (Zo / Rs + Ro +Zo) = 3.0 (25/53.5) = 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

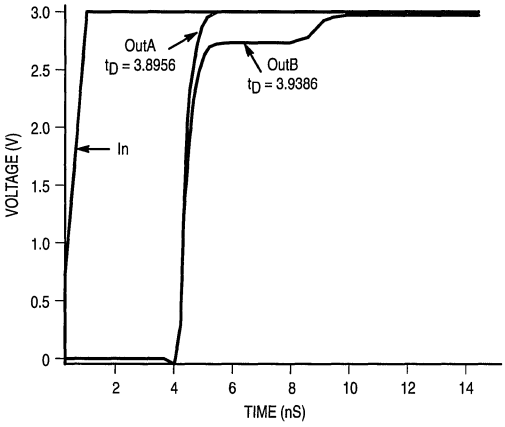
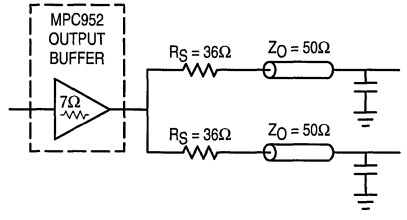


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



7Ω + 36Ω || 36Ω = 50Ω || 50Ω
25Ω = 25Ω

Figure 5. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Power Supply Filtering

The MPC952 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC952 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC952.

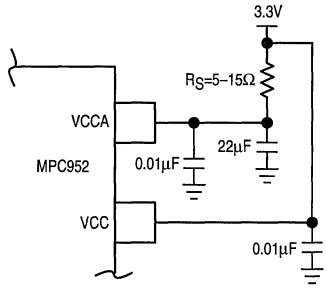


Figure 6. Power Supply Filter

Figure 6 illustrates a typical power supply filter scheme. The MPC952 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC952. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 6 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC952 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Not Recommended for New Designs
See MPC972 or MPC974

Low Voltage PLL Clock Driver

MPC970

LOW VOLTAGE
PLL CLOCK DRIVER

The MPC970 is a 3.3V compatible, PLL based clock driver devices targeted for high performance RISC or CISC processor based systems.

- Fully Integrated PLL
- Output Frequency Up to 250MHz
- Compatible with PowerPC™ and Pentium™ Processors
- Output Frequency Configuration
- On–Board Crystal Oscillator
- 52–Lead TQFP Packaging
- ±50ps Typical Cycle–to–Cycle Jitter

FA SUFFIX
52–LEAD TQFP PACKAGE
CASE 848D–03

The MPC970 was designed specifically to drive today's PowerPC 601 and Pentium processors while providing the necessary performance to address higher frequency PowerPC 601 as well as PowerPC 603 and PowerPC 604 applications. The 2x_PCLK output can toggle at up to 250MHz while the remaining outputs can be configured to drive the other system clocks for MPC 601 based systems. As the processor based clock speeds increase the processor bus will likely run at one third or even one fourth the processor clock. The MPC970 supports the necessary waveforms to drive the BCLKEN input signal of the MPC 601 when the processor bus is running at a lower frequency than the processor. The MPC970 uses an advanced PLL design which minimizes the jitter generated on the outputs. The jitter specification is well within the requirements of the Pentium processor and meets the stringent preliminary specifications of the PowerPC 603 and PowerPC 604 processors. The application section of this data sheet deals in more detail with driving PowerPC and Pentium processor based systems.

The external feedback option of the MPC970 provides for a near zero delay between the reference clock input and the outputs of the device. This feature is required in applications where a master clock is being picked up off the backplane and regenerated and distributed on a daughter card. The advanced PLL of the MPC970 eliminates the dead zone of the phase detector and minimizes the jitter of the PLL so that the phase error variation is held to a minimum. This phase error uncertainty makes up a major portion of the part–to–part skew of the device.

For single clock driver applications the MPC970 provides an internal oscillator and internal feedback to simplify board layout and minimize system cost. By using the on–board crystal oscillator the MPC970 acts as both the clock generator and distribution chip. The external component is a relatively inexpensive crystal rather than a more expensive oscillator. Since in single board applications the delay between the input reference and the outputs is inconsequential an internal feedback option is offered. The internal feedback simplifies board design in that the system designer need not worry about noise being coupled into the feedback line due to board parasitics and layout. The internal feedback is a fixed divide by 32 of the VCO. This divide ratio ensures that the input crystals will be ≤20MHz, thus keeping the crystal costs down and ensuring availability from multiple vendors.

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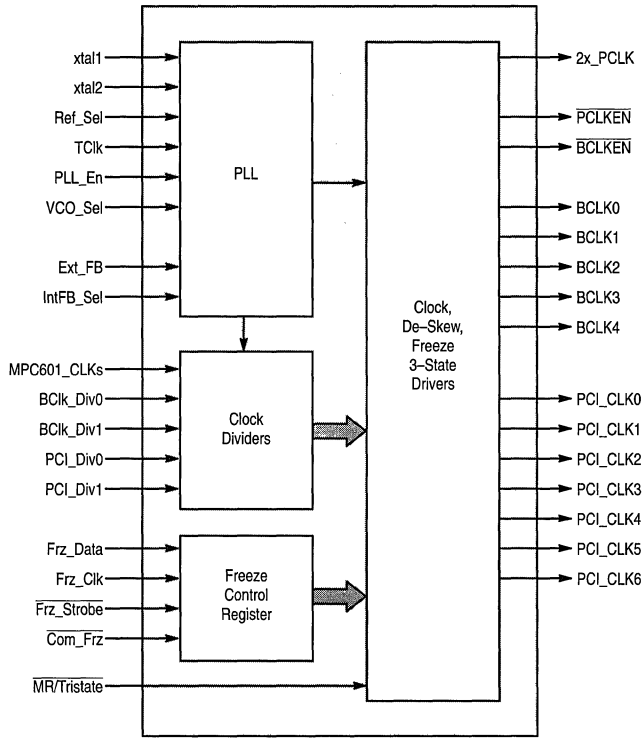


Figure 1. Enable/Disable Scheme

The MPC970 offers a very flexible output enable/disable scheme. This enable/disable scheme helps facilitate system debug as well as provide unique opportunities for system power down schemes to meet the requirements of "green" class machines. The MPC970 allows for the enabling of each output independently via a serial input port or a common enable/disable of all outputs simultaneously via a parallel control pin. When disabled or "frozen" the outputs will be locked in the "LOW" state, however the internal state machines will continue to run. Therefore when "unfrozen" the outputs will activate synchronous and in phase with those outputs which were not frozen. The freezing and unfreezing of outputs occurs only when they are already in the "LOW" state, thus the possibility of runt pulse generation is eliminated. A power–on reset will ensure that upon power up all of the outputs will be active.

For IC and board level testing a $\overline{\text{MR/Tristate}}$ input is provided. When pulled "LOW" all outputs will tristate and all internal flip flops will be reset. In addition the internal PLL can be bypassed and the fanout dividers and output buffers can be driven directly by the TClk input pin. Note that in this mode it will take a number of input clock pulses to cause output transitions as the TClk is fed through the internal dividers.

The MPC970 is fully 3.3V (3.6V for PowerPC 601 designs) compatible and requires no external loop filter components. All inputs accept LVCMOS/LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive 50Ω transmission lines. For series terminated lines each MPC970 output can drive two 50Ω lines in parallel thus effectively doubling the fanout of the device.

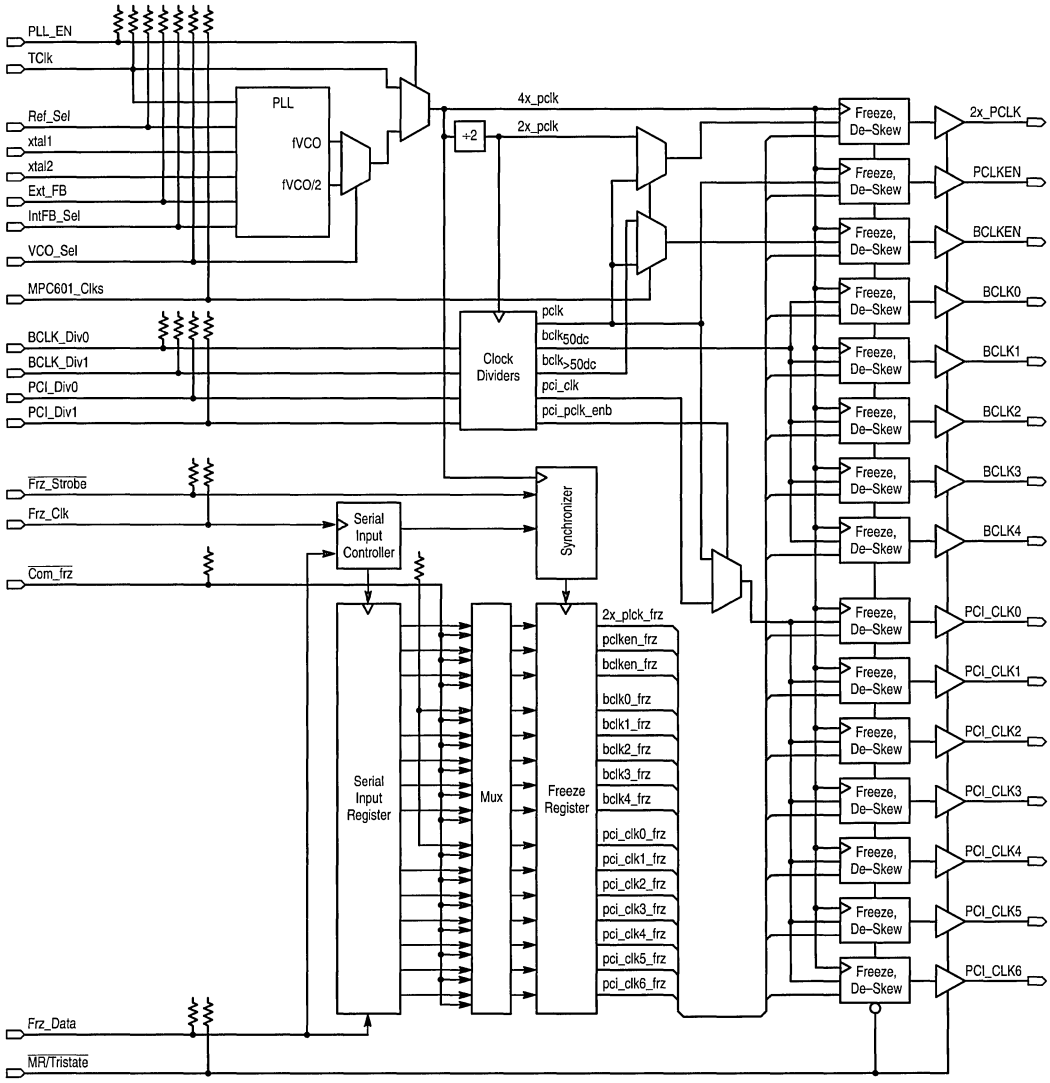


Figure 2. Simplified Block Diagram

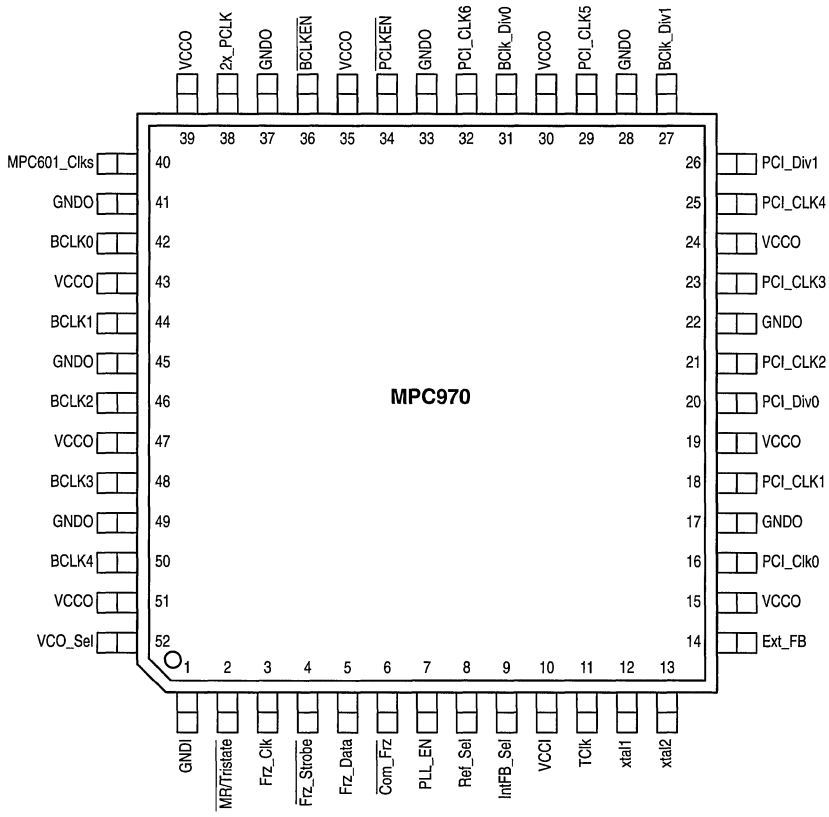


Figure 3. 52–Lead Pinout (Top View)

FUNCTION TABLE 1

MPC601_Clks	2x_PCLK	PCLKEN	BCLKEN	BCLK	PCI_CLK
0	VCO/4	VCO/4	VCO/4	X	X
1	VCO/2	VCO/4	BCLK*	X	X

* Output is purposely delayed vs 2x_PCLK output.

FUNCTION TABLE 2

PCI_Div1	PCI_Div0	PCI_CLK	BCLK_Div1	BCLK_Div0	BCLK
0	0	BLCK	0	0	PCLKEN
0	1	BCLK/2	0	1	PCLKEN/2
1	0	BCLK/3	1	0	PCLKEN/3
1	1	PCLKEN	1	1	PCLKEN/4

FUNCTION TABLE 3

Control Pin	Logic '0'	Logic '1'
VCO_Sel	fVCO/2	fVCO
Ref_Sel	TCLK	Crystal Osc
PLL_En	Bypass PLL	Enable PLL
IntFB_Sel	Ext Feedback	Int Feedback

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic		Min	Max	Unit	Condition
V_{CC}	Power Supply Voltage		3.0	3.8	V	
I_{CC}	Quiescent Power Supply			250	mA	
V_{IL}	Input Voltage LOW	LVCMOS Inputs		$0.3V_{DD}$	V	
V_{IH}	Input Voltage HIGH	LVCMOS Inputs	$0.7V_{DD}$		V	
I_{IH}	Input Current HIGH	LVCMOS Inputs		–100	µA	$V_{IN} = V_{CC}$
I_{IL}	Input Current LOW		–200		µA	V_{IN} = GND
V_{OH}	Output Voltage HIGH		V_{DD}–0.2		V	I_{OH} = –20mA (Note 1.)
V_{OL}	Output Voltage LOW			0.2	V	I_{OL} = 20mA (Note 1.)
I_{OZ}	Tristate Output Leakage Current		–10	10	µA	$V_{OH} = V_{CC}$ or GND
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance				pF	
C_{OUT}	Output Capacitance			8	pF	

1. The MPC970 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	10	Note 2.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

2. Maximum input reference is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{Xtal}	Crystal Oscillator Frequency	10		25	MHz	Note 3.
F_{out}	Maximum 2x_PCLK Output Frequency			200	MHz	Note 4.
t_{DC}	Output Duty Cycle (Notes 4., 5.)	45 35		55 65	%	F_{out} < 200MHz F_{out} ≥ 200MHz
$V_{OH}AC$	AC Output HIGH Voltage	2.4 2.2			V	F_{out} < 200MHz F_{out} ≥ 200MHz
$V_{OL}AC$	AC Output LOW Voltage			0.4 0.6	V	F_{out} < 200MHz F_{out} ≥ 200MHz
t_{pw}	2x_PCLK Pulse Width (Notes 4., 5.)	1.75	2.27		ns	F_{out} = 200MHz
t_{per}	Minimum Clock Out Period	4.85	4.91		ns	F_{out} = 200MHz
f_{VCO}	VCO Lock Range	200		700	MHz	
t_{jitter}	Output Jitter (Notes 4., 5.)		±50 110 76	±100 190 210	ps	PLL Jitter 2x_P Period Variation Period Variation (Other)
t_{skew}	Output–to–Output Skew (Notes 4., 5.) 2x_PCLCK, PCLKEN, BCLKEN, BCLK 2x_PCLK, PCLKEN, BCLK PCI_CLK BCLK All			 550 550 450 550 800	ps	 MPC601_Clks = '0' MPC601_Clks = '1'
t_{delay}	Propagation Delay 2x_PCLK to BCLKEN	100		850	ps	MPC601_Clks = '1'
t_r, t_f	Output Rise/Fall Time (Notes 4., 5.)	0.15		1.5	ns	0.8 to 2.0V
t_{lock}	PLL Lock Time			10	ms	
t_{PZL}	Output Enable Time $\overline{MR}$/Tristate to Outputs			8	ns	
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{MR}$/Tristate to Outputs			10	ns	
f_{MAX}	Maximum Frz_Clk Frequency			20	MHz	
t_s	Setup Time Frz_Data to Frz_Clk $\overline{Com\_Frz}$ to $\overline{Frz\_Strobe}$	8 5				
t_h	Hold Time Frz_Clk to Frz_Data $\overline{Frz\_Strobe}$ to $\overline{Com\_Frz}$	8 5				

3. See Applications Info section for more crystal information.
4. Drive 50Ω transmission lines.
5. Measured at 1.4V.

DETAILED PIN DESCRIPTIONS

The following gives a brief description of the functionality of the MPC970 I/O. Unless explicitly stated all inputs are LVCMOS/LVTTL compatible with internal pull up resistors. All outputs are LVCMOS level outputs which are capable of driving two series terminated 50Ω transmission lines on the incident edge.

xtal1, xtal2

For the MPC970 the xtal1 and xtal2 pins represent the external crystal connections to the internal oscillator. The crystal oscillator is completely self contained, there are no external components required. The oscillator is specified to function for crystals of up to 50MHz. Exact crystal specifications are outlined in the applications section.

VCO_Sel

The VCO_Sel pin allows the user to further divide the internal VCO frequency for the generation of lower frequencies at the outputs. The VCO_Sel pin should be used to set the VCO into its most optimum range. Refer to the applications section for more details on the VCO frequency range. A logic '1' on the VCO_Sel pin will bypass the internal ÷2.

TClk

The TClk input serves a dual purpose; it can be used as either a reference clock input for the PLL from an external frequency source or it can be used as a board level test clock in the PLL bypass mode.

PLL_En

The PLL_En pin allows the TClk input to be routed around the PLL for system test and debug. When pulled low the MPC970 will be placed in the test mode. Note that the TClk input will be routed through the divider chain. For instance in the PowerPC 601 microprocessor clock generation mode the TClk input will toggle twice for each toggle on the 2x_PCLK output. Depending on the states of the frequency divider select pins this ratio may be higher.

Frz_Data

Frz_Data is the serial data input for the output freeze function of the device. Refer to the applications section for more information on the freeze functionality.

Frz_Clk

Frz_Clk is the serial freeze logic clock input. Refer to the applications section for more information on the freeze functionality.

$\overline{\text{Frz\_Strobe}}$

The $\overline{\text{Frz\_Strobe}}$ input is used to freeze or unfreeze all of the outputs simultaneously. Refer to the applications section for more information on the freeze functionality.

$\overline{\text{Com\_Frz}}$

The $\overline{\text{Com\_Frz}}$ input allows the user to enable/disable all of the outputs with the control of a single pin. The action will take place upon a high to low transition of the $\overline{\text{Frz\_Strobe}}$ input.

BClk_Div0:1

The BClk_Div inputs are used to program the VCO divide ratio for the BCLK outputs. These inputs also set the divide ratio of the BCLKEN output to be equal in frequency to the BCLK outputs when the device is in the MPC601_Clks mode. The BClk_Div inputs set the frequency as follows:

BClk_Div1	BClk_Div0	BCLK Frequency
0	0	PCLKEN
0	1	PCLKEN/2
1	0	PCLKEN/3
1	1	PCLKEN/4

In most applications these inputs will be strapped to the appropriate power rails.

PCI_Div0:1

The PCI_Div inputs set the division ratio for the PCI_CLKs. The PCI_CLKs are set relative to the BCLK or the PCLKEN output such that you can upgrade the processor bus and maintain the PCI bus frequency in the currently defined ≤ 33MHz range. The PCI_Div inputs set the PCI_CLKs as follows:

PCI_Div1	PCI_Div0	PCI_CLK Frequency
0	0	BCLK
0	1	BCLK/2
1	0	BCLK/3
1	1	PCLKEN

In a typical application these inputs will be strapped to the appropriate power rail.

MPC601_Clks

The MPC601_Clks input will configure the outputs to drive the PowerPC 601 microprocessor when pulled HIGH or left open. When pulled LOW it will configure the 2xPCLK, PCLKEN and BCLKEN all into a VCO/4 mode. In this mode the MPC970 will have three more outputs available to drive clock loads on the processor bus for PowerPC 603, PowerPC 604 or Pentium microprocessor based systems.

Ext_FB

The Ext_FB pin is an input to the phase detector of the PLL which is tied to an external feedback output. Typically this feedback will be one of the lowest frequency outputs of the MPC970.

IntFB_Sel

The IntFB_Sel input selects whether the internal feedback signal or an external feedback signal is routed to the phase detector of the PLL. The default mode, pulled HIGH via the internal pull up resistor, is to select the internal feedback.

$\overline{\text{MR/Tristate}}$

The $\overline{\text{MR/Tristate}}$ input when pulled LOW will reset all of the internal flip flops and also tristate all of the clock outputs. This input is used primarily for IC and board level test.

Ref_Sel

The Ref_Sel input allows the user to choose between two sources for the PLL reference frequency. For the MPC970, LOW on Ref_Sel will choose the LVCMOS TCLK input. For the MPC970, a HIGH on Ref_Sel will choose the crystal oscillator input.

2x_PCLK

In general the outputs are named based on the implementation in a PowerPC 601 microprocessor based system. In the MPC601_Clk mode the 2x_PCLK will run at half the internal VCO frequency. With a maximum internal VCO frequency of 1000MHz this output could theoretically toggle at 500MHz, in practice however the output can toggle only as fast as 300MHz. This frequency will be required on future enhancements to the MPC 601 microprocessor. When the MPC970 is taken out of the MPC601_Clk mode the 2xPCLK will run at a VCO/4 frequency. This divide ratio will place this output frequency in the present and future processor bus speeds of the PowerPC 603, PowerPC 604 and Pentium microprocessors. The 2x_PCLK output is a 50% duty cycle LVCMOS output.

PCLKEN

The PCLKEN output is designed to drive the PCLKEN input of the PowerPC 601 microprocessor when the MPC970 is in the MPC601_Clk mode. The PCLKEN output frequency is one half that of the 2x_PCLK output, a divide by four of the internal VCO. The PCLKEN output runs at the same frequency regardless of the state of the frequency divide controls. The toggle frequency of this output is well placed for driving the PowerPC 603, PowerPC 604 and Pentium processor buses. The PCLKEN output is a 50% duty cycle LVCMOS output.

BCLKEN

The BCLKEN output is designed to drive the BCLKEN input of the PowerPC 601 microprocessor when the MPC970 is in the MPC601_Clks mode. The BCLKEN toggles at the same frequency as the BCLK outputs as described earlier. However when the BCLKEN output is a divide by three or a divide by four of the PCLKEN output the duty cycle is 66/33 and 75/25 respectively per the requirement of the MPC 601 processor. In addition to meet the HOLD time spec for the BCLKEN input of the MPC 601 the BCLKEN output of the MPC970 lags the 2xPCLK output by no less than 100ps. When the MPC970 is not in the MPC601_Clks mode the BCLKEN output is set at a fixed divide by four from the internal VCO. In addition in this mode the BCLKEN output does NOT lag the other outputs, but rather is synchronous within the Output–to–Output skew spec of the device.

BCLK0:4

The BCLK outputs are designed to drive the clock loads on the processor bus of either the PowerPC or Pentium microprocessors. The most common practice in "non MPC 601" applications will be to place these outputs in the PCLKEN/1 mode and combine them with the above outputs to drive all of the loads on the processor bus. The division ratios do allow for the swap of these outputs with the PCI_CLK outputs if more clocks are needed to drive the processor bus. For PowerPC 601 microprocessor based systems the division ratios allow the processor internal speeds to be increased while maintaining reasonable speeds for the L2 cache and the PCI bridge chip. The BCLK outputs are 50% duty cycle LVCMOS outputs.

PCI_Clk0:6

As the name would suggest the PCI_CLK outputs are designed to drive the PCI bus clock loads in a typical microprocessor based system. The division ratios allow for these outputs to remain in the ≤ 33MHz PCI bus speeds for various common processor bus speeds as well as higher future processor bus speeds. These outputs can also be programmed to run at the processor bus speeds if more processor bus clocks are required. The PCI_CLK outputs are 50% duty cycle LVCMOS outputs.

APPLICATIONS INFORMATION

Programming the MPC970

The MPC970 is very flexible in the programming of the frequency relationships of the various outputs as well as the relationships between the input references and outputs. The purpose of this section is to outline the various relationships. Although not exhaustive the hope is that enough information is supplied to allow the customers to tailor the I/O relationships for their specific applications.

The VCO used in the MPC970 is a differential ring oscillator. The VCO exhibits a very wide frequency range to allow for a great deal of flexibility to the end user. Special design techniques were used in the overall PLL design to keep the relatively high gain of the VCO from significantly impacting the jitter of the PLL.

Table 1 tabulates the various output frequencies for the different modes defined by the division select input pins. In this table the VCO_Sel pin is high so that the ÷2 prescaler is bypassed. Note that the ÷32 feedback is always fed directly from the VCO and is thus unaffected by the level on the VCO_Sel input. Table 1 shows each of the output frequencies as a function of the VCO frequency. The two VCO ranges can be used to plug in values to get the actual frequencies. When the internal feedback option is used the multiplication factor of the device will equal 32 divided by the

output divide ratio. If the VCO_Sel pin is "LOW" the multiplication factor will be reduced further by 2. (See "Using the On–Board Crystal Oscillator" section of this datasheet.)

Using the External Feedback Feature of the MPC970/71

In applications where the relationship between the output waveforms and the input waveforms are critical the external feedback option will likely be used. Table 1 and Table 2 are still appropriate for establishing the potential output frequency relationships. The input reference frequency for external feedback applications will be equal to the frequency of the feedback signal. As a result the use of the external feedback yields a number of potential input to output frequency multiplication factors which are not available using the internal feedback. Using the external feedback the device can function as a zero delay buffer and could multiply the input from 4 to as much as 48. In practice however the multiplication factor is limited by the loop dynamics of the PLL. The MPC970 PLL was optimized for an input reference frequency or greater than 10MHz. Frequencies lower than 10MHz will tend to pass through the filter and add jitter to the PLL. In addition the PLL was optimized for feedback divide ratios of between 8 and 64. The user should avoid using the device with feedback divide ratios outside of this range. For the external feedback case the feedback divide ratio will include the ÷2 (if VCO_Sel is LOW) plus the output divider for the feedback output. If, for instance the MPC970 is to be used as a zero delay buffer the VCO_Sel pin should be pulled LOW and all of the outputs should be set in a VCO/4 mode. This would produce a feedback ratio of ÷8. Several potential configurations using the external feedback are pictured in Figure 4 through Figure 7.

The external feedback option of the MPC970 is critical for applications in which more than one clock driver need to be synchronized. The external feedback option ensures that the feed through delay is the same as the feedback delay. This functionality removes propagation delay variation as a factor in the determination of part to part skew. The low jitter PLL used in the MPC970 has a near zero deadband phase detector and very little part to part variability. The result is a very low phase error variability in the product. When coupled with the output to output skew the phase error variability accounts for the part to part skew of the device. From the specification table one sees that the worst case part to part skew of the device is 800ps, assuming that there is zero skew in the multiple reference inputs. For multiple MPC970 applications if the lowest generated output frequency is used as the feedback signal the devices will be guaranteed to be synchronized. For applications where the lowest frequency is not used as the reference or where the internal feedback is used there is no way to guarantee that the multiple devices will be phase synchronized.

Table 1. Programmable Output Frequency Relationships (MPC601_Clks = 'HIGH'; VCO_Sel = 'HIGH')

INPUTS				OUTPUTS				
PCI_Div1	PCI_Div0	BCLK_Div1	BCLK_Div0	2x_PCLK	PCLKEN	BCLKEN*	BCLK	PCI_CLK
0	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/2	VCO/4	VCO/8	VCO/8	VCO/8
0	0	1	0	VCO/2	VCO/4	VCO/12	VCO/12	VCO/12
0	0	1	1	VCO/2	VCO/4	VCO/16	VCO/16	VCO/16
0	1	0	0	VCO/2	VCO/4	VCO/4	VCO/4	VCO/8
0	1	0	1	VCO/2	VCO/4	VCO/8	VCO/8	VCO/16
0	1	1	0	VCO/2	VCO/4	VCO/12	VCO/12	VCO/24
0	1	1	1	VCO/2	VCO/4	VCO/16	VCO/16	VCO/32
1	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4	VCO/12
1	0	0	1	VCO/2	VCO/4	VCO/8	VCO/8	VCO/24
1	0	1	0	VCO/2	VCO/4	VCO/12	VCO/12	VCO/36
1	0	1	1	VCO/2	VCO/4	VCO/16	VCO/16	VCO/48
1	1	0	0	VCO/2	VCO/4	VCO/4	VCO/4	VCO/4
1	1	0	1	VCO/2	VCO/4	VCO/8	VCO/8	VCO/4
1	1	1	0	VCO/2	VCO/4	VCO/12	VCO/12	VCO/4
1	1	1	1	VCO/2	VCO/4	VCO/16	VCO/16	VCO/4

* BCLK_En output is delayed relative to other outputs

Table 2. Programmable Output Frequency Relationships (MPC601_Clks = 'LOW'; VCO_Sel = 'HIGH')

INPUTS				OUTPUTS				
PCI_Div1	**PCI_Div0**	**BCLK_Div1**	**BCLK_Div0**	**2x_PCLK**	**PCLKEN**	**BCLKEN***	**BCLK**	**PCI_CLK**
0	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8	VCO/8
0	0	1	0	VCO/4	VCO/4	VCO/4	VCO/12	VCO/12
0	0	1	1	VCO/4	VCO/4	VCO/4	VCO/16	VCO/16
0	1	0	0	VCO/4	VCO/4	VCO/4	VCO/4	VCO/8
0	1	0	1	VCO/4	VCO/4	VCO/4	VCO/8	VCO/16
0	1	1	0	VCO/4	VCO/4	VCO/4	VCO/12	VCO/24
0	1	1	1	VCO/4	VCO/4	VCO/4	VCO/16	VCO/32
1	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4	VCO/12
1	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8	VCO/24
1	0	1	0	VCO/4	VCO/4	VCO/4	VCO/12	VCO/36
1	0	1	1	VCO/4	VCO/4	VCO/4	VCO/16	VCO/48
1	1	0	0	VCO/4	VCO/4	VCO/4	VCO/4	VCO/4
1	1	0	1	VCO/4	VCO/4	VCO/4	VCO/8	VCO/4
1	1	1	0	VCO/4	VCO/4	VCO/4	VCO/12	VCO/4
1	1	1	1	VCO/4	VCO/4	VCO/4	VCO/16	VCO/4

* BCLK_En output is coincident with other outputs

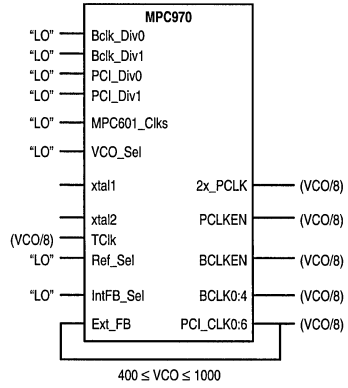


Figure 4. External Feedback Configuration 1

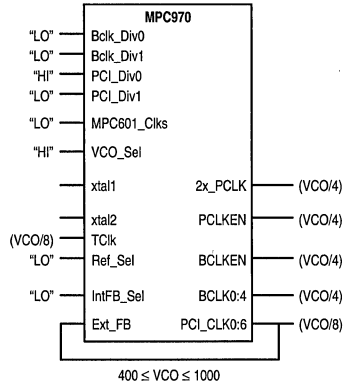


Figure 5. External Feedback Configuration 2

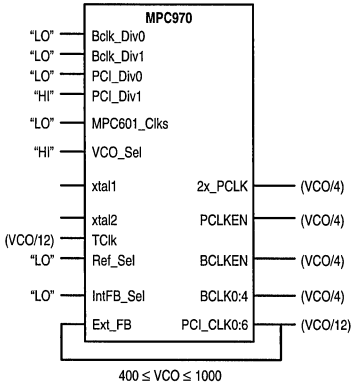


Figure 6. External Feedback Configuration 3

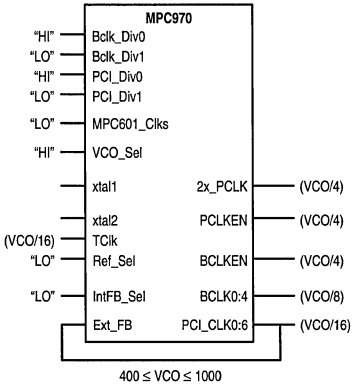


Figure 7. External Feedback Configuration 4

Using the On–Board Crystal Oscillator

The MPC970 features an on–board crystal oscillator to allow for seed clock generaytion as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC970 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required. In addition, with crystals with a higher shunt capacitance, it may be necessary to place a 1k resistor across the two crystal leads.

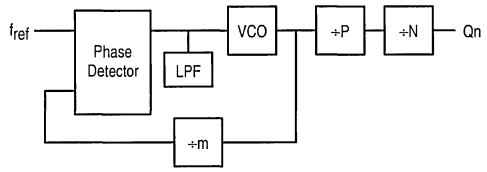
The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC970 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 3. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental at Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100µW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

The MPC970 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal. To determine the crystal required to produce the desired output frequency for an application which utilizes internal feedback the block diagram of Figure 8 should be used. The P and the M values for the MPC970 are also included in Figure 8. The M values can be found in the configuration tables included in this applications section.



$$f_{ref} = \frac{f_{VCO}}{m}, \quad f_{VCO} = fQn \cdot N \cdot P$$

$$\therefore f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

m = 32
P = 1 (VCO_Sel='1'), 2(VCO_Sel='0')

Figure 8. PLL Block Diagram

For the MPC970 clock driver, the following will provide an example of how to determine the crystal frequency required for a given design.

Given:

2x_PCLK = 200MHz
PCLKEN = 100MHz
BCLK = 50MHz
PCI_CLK = 25MHz
VCO_SEL = '1'

$$f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

From Table 3

PCI_CLK = VCO/16 then N = 16
or
PCLKEN = VCO/4 then N = 4

From Figure 8

m = 32 and P = 1

$$f_{ref} = \frac{25 \cdot 16 \cdot 1}{32} = 12.5MHz \text{ or } \frac{100 \cdot 4 \cdot 1}{32} = 12.5MHz$$

Driving Transmission Lines

The MPC970 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel

terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC970 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 9 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC970 clock driver is effectively doubled due to its capability to drive multiple lines.

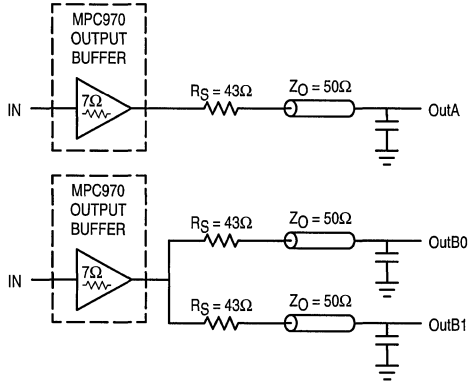


Figure 9. Single versus Dual Transmission Lines

The waveform plots of Figure 10 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC970 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC970. The output waveform in Figure 10 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 11 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

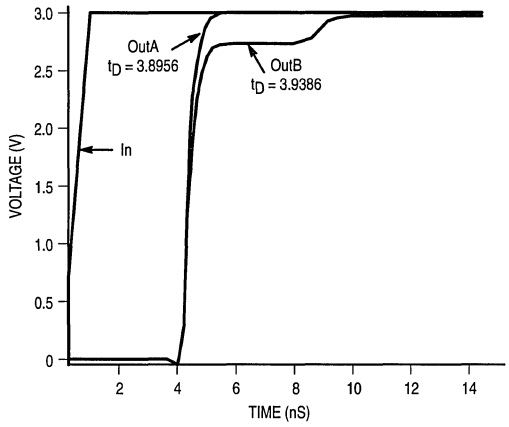
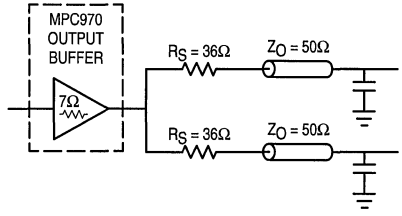


Figure 10. Single versus Dual Waveforms



$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

Figure 11. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Using the Output Freeze Circuitry

With the recent advent of a "green" classification for computers the desire for unique power management among system designers is keen. The individual output enable control of the MPC970 allows designers, under software control, to implement unique power management schemes into their designs. Although useful, individual output control at the expense of one pin per output is too high, therefore a simple serial interface was derived to economize on the control pins.

The freeze control logic provides two mechanisms through which the MPC970 clock outputs may be frozen (stopped in the logic '0' state):

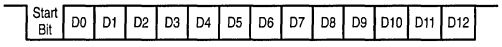
The first freeze mechanism allows serial loading of the 13–bit Serial Input Register, this register contains one programmable freeze enable bit for 13 of the 15 output clocks. The BCLK0 and PCI_CLK0 outputs cannot be frozen with the serial port, this avoids any potential lock up situation

should an error occur in the loading of the Serial Input Register. The user may programmably freeze an output clock by writing logic '0' to the respective freeze enable bit. Likewise, the user may programmably unfreeze an output clock by writing logic '1' to the respective enable bit.

The second freeze mechanism allows all 15 clocks to be frozen simultaneously by placing a logic '0' on the Com_Frz input and then issuing a low going pulse on the Frz_Strobe input. Likewise, all 15 clocks can be simultaneously unfrozen by placing logic '1' on the Com_Frz input and then issuing a low–going pulse on the Frz_Strobe input. Note that all 15 clocks are affected by the Frz_Strobe freeze logic.

The freeze logic will never force a newly–frozen clock to a logic '0' state before the time at which it would normally transition there. The logic simply keeps the frozen clock at logic '0' once it is there. Likewise, the freeze logic will never force a newly–unfrozen clock to a logic '1' state before the time at which it would normally transition there. The logic re–enables the unfrozen clock during the time when the respective clock would normally be in a logic '0' state, eliminating the possibility of 'runt' clock pulses.

The user may write to the Serial Input register through the Frz_Data input by supplying a logic '0' start bit followed serially by 13 NRZ freeze enable bits. After the 13th freeze enable bit the Frz_Data signal must be left in (or returned to) a logic '1' state (Figure 12). The period of each Frz_Data bit equals the period of the free–running Frz_Clk signal. The Frz_Data serial transmission should be timed so the MPC970 can sample each Frz_Data bit with the rising edge of the free–running Frz_Clk signal.



D0 is the control bit for 2x_PCLK
D1 is the control bit for PCLKEN
D2 is the control bit for BCLKEN
D3–D6 are the control bits for BCLK1–BCLK4
D7–D12 are the control bits for PCI_CLK1–PCI_CLK6

Figure 12. Freeze Data Input Protocol

The user can combine the two freeze capabilities to simplify system level implementation. The serial input port can be used to establish the freeze mask to disable the appropriate outputs. The Frz_Strobe input can then be used to unfreeze the outputs without having to serially load an "all unfrozen" freeze mask.

Driving the PowerPC 601 Microprocessor

The MPC601 processor requires three clock inputs from the MPC970 clock driver. A 2x_PCLK input at twice the internal MPC 601 clock rate and the PCLKEN and BCLKEN signals used to mask internal clock edges. The PCLKEN signal always runs at one half the 2x_PCLK signal while the BCLKEN signal can run at 1x, 1/2x, 1/3x or 1/4x the PCLK input signal depending on the speed of the processor bus. When the BCLKEN signal is running at 1/3 or 1/4 the PCLK input the input duty cycle must be 66/33 and 75/25 respectively. In addition, as shown in Figure 13, to satisfy the BCLKEN to 2x_PCLK Hold specification the BCLKEN signal must be at least coincident with the 2x_PCLK edge. To simplify board level implementation it would be desirable that the BCLKEN signal actually lag the 2x_PCLK by a few hundred picoseconds. The MPC970 insures that its BCLKEN output always lags the 2x_PCLK input by at least 300ps.

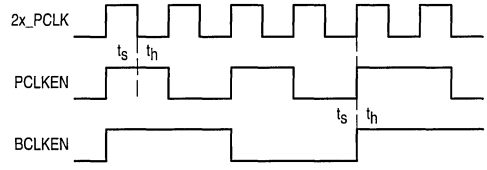


Figure 13. MPC601 Setup and Hold Times

Table 4 illustrates some typical MPC 601 system frequencies which can be realized using the MPC970 clock driver.

Table 4. Common MPC601 System Frequencies

2x_PCLK	PCLK	BCLK	PCI_CLK
240	120	60(1/2x)	30(1/2x)
240	120	40(1/3x)	20(1/2x)
240	120	30(1/4x)	30(1x)
200	100	50(1/2x)	25(1/2x)
200	100	33(1/3x)	33(1x)
200	100	25(1/4x)	25(1x)
160	80	40(1/2x)	20(1/2x)
160	80	20(1/4x)	20(1x)
132	66	66(1x)	33(1/2x)
132	66	33(1/2x)	33(1x)

Driving the PowerPC 603, PowerPC 604 and Pentium Microprocessors

The PowerPC 603, PowerPC 604 and Pentium processors differ from the MPC 601 processor in that the processor input clocks are at the same frequency as the processor bus. A typical system for these processors will include 8 – 16 clock loads on the processor bus. When the MPC970 is taken out of the MPC601_Clk mode there are a total of 8 "non PCI_CLK" outputs which can be run at the processor bus speeds for these microprocessors. Since each output can drive two series terminated transmission lines the MPC970 can support point to point clock distribution for up to 16 loads on the processor bus. In addition there will be 7 PCI_CLK outputs which can drive up to 14 loads on the PCI bus.

If more clock loads are present on the processor bus the PCI_CLKs can be configured to drive processor bus clock loads in addition to the BCLKs or alternatively the clocking roles of the BCLKs and PCI_CLKs can be reversed. Table 3 illustrates some useful frequency combinations for driving PowerPC 603, PowerPC 604 or Pentium microprocessor based systems.

Table Table 5. Common PowerPC 603, PowerPC 604 and Pentium System Frequencies

2x_PCLK	PCLK	BCLK	PCI_CLK
80	80	80(1x)	26(1/3x)
75	75	75(1x)	25(1/3x)
66	66	66(1x)	33(1/2x)
66	66	66(1x)	66(1x)
66	66	33(1/2x)	66(PCLKEN)
60	60	60(1x)	30(1/2x)

Advance Information

Low Voltage PLL Clock Driver

MPC972
MPC973

LOW VOLTAGE
PLL CLOCK DRIVER

FA SUFFIX
52–LEAD TQFP PACKAGE
CASE 848D-03

The MPC972/973 are 3.3V compatible, PLL based clock driver devices targeted for high performance CISC or RISC processor based systems. With output frequencies of up to 150MHz and skews of 350ps the MPC972/973 are ideally suited for the most demanding synchronous systems. The devices offer twelve low skew outputs plus a feedback and sync output for added flexibility and ease of system implementation.

- Fully Integrated PLL
- Output Frequency up to 150MHz
- Compatible with PowerPC™ and Pentium™ Microprocessors
- TQFP Packaging
- 3.3V V_{CC}
- ± 100ps Typical Cycle–to–Cycle Jitter

The MPC972/973 features an extensive level of frequency programmability between the 12 outputs as well as the input vs output relationships. Using the select lines output frequency ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 6:1 and 6:5 between outputs can be realized by pulsing low one clock edge prior to the coincident edges of the Qa and Qc outputs. The Sync output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies, this allows for very flexible programming of the input reference vs output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non–binary factor. The Power–On Reset ensures proper programming if the frequency select pins are set at power up. If the fselFB2 pin is held high, it may be necessary to apply a reset after power–up to ensure synchronization between the QFB output and the other outputs. The internal power–on reset is designed to provide this function, but with power–up conditions being system dependent, it is difficult to guarantee. All other conditions of the fsel pins will automatically synchronize during PLL lock acquisition.

The MPC972/973 offers a very flexible output enable/disable scheme. This enable/disable scheme helps facilitate system debug as well as provide unique opportunities for system power down schemes to meet the requirements of "green" class machines. The MPC972 allows for the enabling of each output independently via a serial input port. When disabled or "frozen" the outputs will be locked in the "LOW" state, however the internal state machines will continue to run. Therefore when "unfrozen" the outputs will activate synchronous and in phase with those outputs which were not frozen. The freezing and unfreezing of outputs occurs only when they are already in the "LOW" state, thus the possibility of runt pulse generation is eliminated. A power-on reset will ensure that upon power up all of the outputs will be active. Note that all of the control inputs on the MPC972/973 have internal pull–up resistors.

The MPC972/973 is fully 3.3V compatible and requires no external loop filter components. All inputs accept LVCMOS/LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive 50Ω transmission lines. For series terminated lines each MPC972/973 output can drive two 50Ω lines in parallel thus effectively doubling the fanout of the device.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

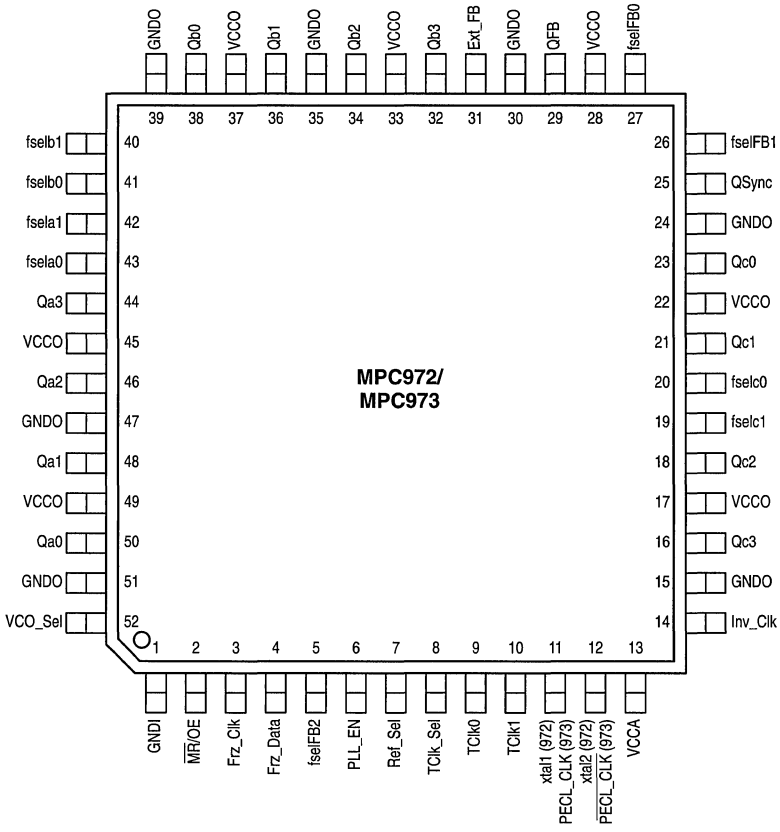


Figure 1. 52–Lead Pinout (Top View)

FUNCTION TABLE 1

fsela1	fsela0	Qa	fselb1	fselb0	Qb	fselc1	fselc0	Qc
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

FUNCTION TABLE 2

fselFB2	fselFB1	fselFB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

FUNCTION TABLE 3

Control Pin	Logic '0'	Logic '1'
VCO_Sel	VCO/2	VCO
Ref_Sel	TCLK	Xtal (PECL)
TCLK_Sel	TCLK0	TCLK1
PLL_En	Bypass PLL	Enable PLL
$\overline{MR}$/OE	Master Reset/Output Hi–Z	Enable Outputs
Inv_Clk	Non–Inverted Qc2, Qc3	Inverted Qc2, Qc3

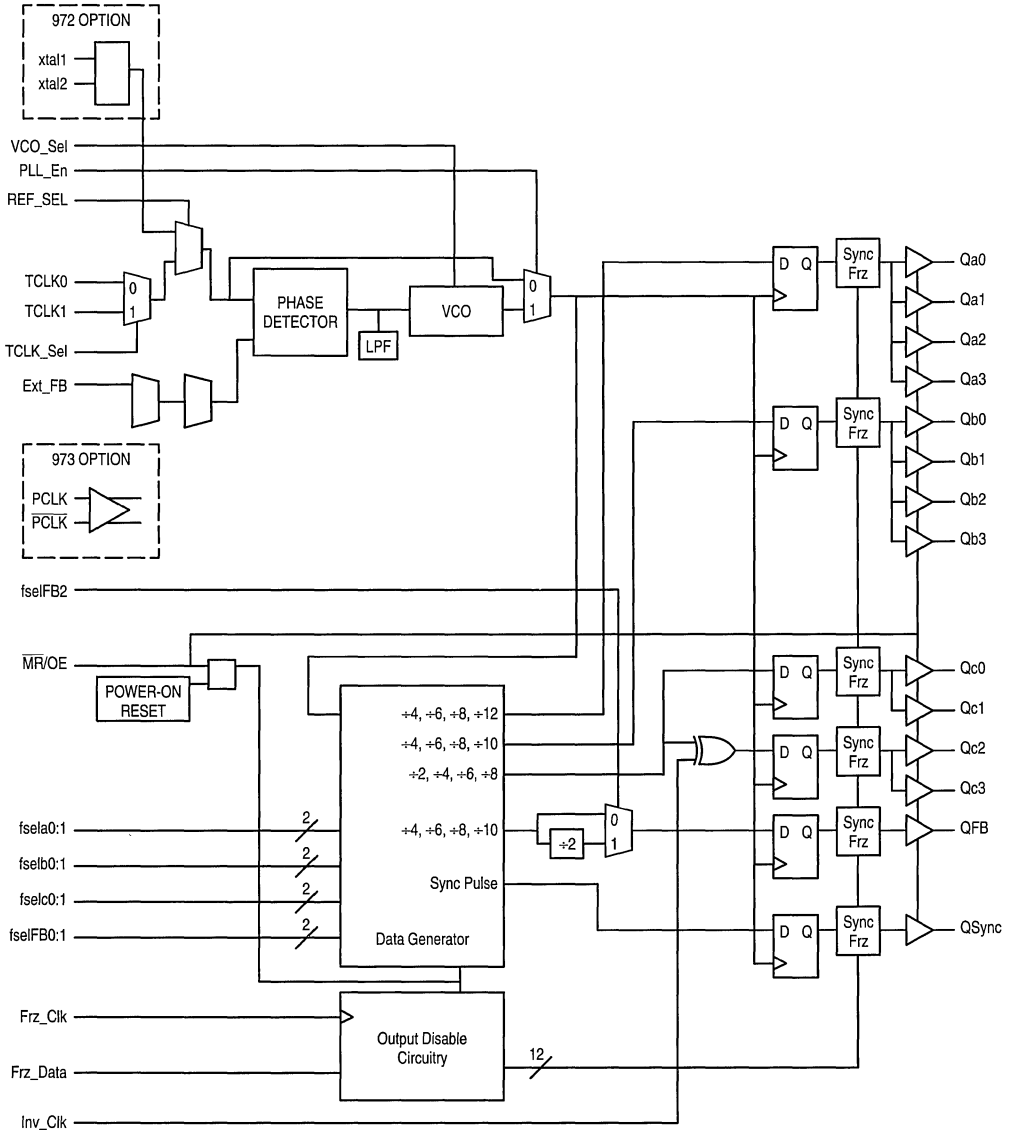


Figure 2. Logic Diagram

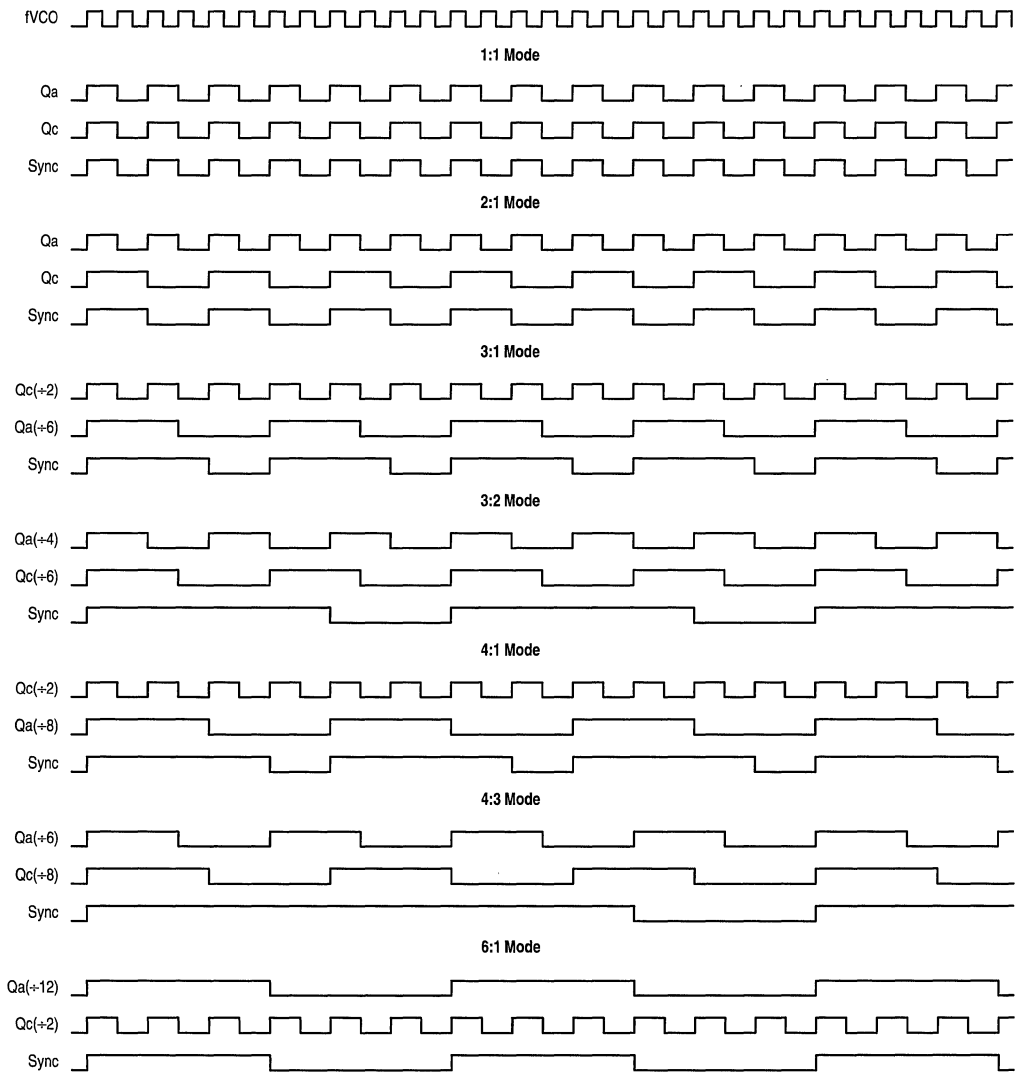


Figure 3. Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current	TBD	TBD	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage	0.8			V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20mA (Note 1.)
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20mA (Note 1.)
I_{IN}	Input Current			±100	µA	Note 2.
I_{CC}	Maximum Quiescent Supply Current			TBD	mA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output

1. The MPC972/973 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pull–up/pull–down resistors which affect input current.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	10	Note 3.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

3. Maximum input reference frequency is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time (Note 4.)	0.15		1.5	ns	0.8 to 2.0V
t_{pw}	Output Duty Cycle (Note 4.)		$t_{CYCLE}/2$ ±500		ps	
t_{Xtal}	Crystal Oscillator Frequency	10		25	MHz	Note 5.
t_{pd}	SYNC to Feedback Propagation Delay	TBD	X_1±150	TBD	ps	Notes 4., 6.; QFB = ÷8
t_{os}	Output-to-Output Skew Same Frequency Different Frequency			350 500	ps	Note 4.
f_{VCO}	VCO Lock Range	200		480	MHz	
f_{max}	Maximum Output Frequency Q (÷2) Q (÷4) Q (÷6) Q (÷8)			150 120 80 60	MHz	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)		±100		ps	
t_{PLZ}, t_{PHZ}	Output Disable Time	2		8	ns	
t_{PZL}, t_{PZH}	Output ENable TIme	2		10	ns	
t_{lock}	Maximum PLL Lock Time			10	ms	
f_{MAX}	Maximum Frz_Clk Frequency			20	MHz	

4. 50Ω transmission line terminated into $V_{CC}/2$.
5. See Applications Info section for more crystal information.
6. t_{pd} is specified for a 50MHz input reference. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

APPLICATIONS INFORMATION

Programming the MPC972/973

The MPC972/973 is the most flexible frequency programming device in the Motorola timing solution portfolio. With three independent banks of four outputs as well as an independent PLL feedback output the total number of possible configurations is too numerous to tabulate. Table 1 tabulates the various selection possibilities for the three banks of outputs. The divide numbers presented in the table represent the divider applied to the output of the VCO for that bank of outputs. To determine the relationship between the three backs the three divide ratios would be compared. For instance if a frequency relationship of 5:3:2 was desired the following selection could be made. The Qb outputs could be set to ÷10, the Qa outputs to ÷6 and the Qc outputs to ÷4. With this output divide selection the desired 5:3:2 relationship would be generated. For situations where the VCO will run at relatively low frequencies the PLL may not be stable for the desired divide ratios. For these circumstances the VCO_Sel pin allows for an extra ÷2 to be added into the clock path. When asserted this pin will maintain the desired output relationships, but will provide an enhanced lock range for the PLL. Once the output frequency relationship is set and the VCO is in its stable range the feedback output would be programmed to match the input reference frequency.

The MPC972/973 offers only an external feedback to the PLL. A separate feedback output is provided to optimize the flexibility of the device. If in the example above the input reference frequency was equal to the lowest output frequency the feedback output would be set in the ÷10 mode. If the input needed to be half the lowest frequency output the fselFB2 input could be asserted to half the feedback frequency. This action multiplies the output frequencies by two relative to the input reference frequency. With 7 unique feedback divide capabilities there is a tremendous amount of flexibility. Again assume the above 5:3:2 relationship is needed with the highest frequency output equal to 100MHz. If one was also constrained because the only reference frequency available was 50MHz the setup in Figure 4 could be used. The MPC972/973 provides the 100, 66 and 40MHz outputs all synthesized from the 50MHz source. With its multitude of divide ratio capabilities the MPC972/973 can generate almost any frequency from a standard, common frequency already present in a design. Figure 5 and Figure 6 illustrate a few more examples of possible MPC972/973 configurations.

The MPC972/973 has one more prgramming feature added to its arsenal. The Inv_Clk input pin when asserted will invert the Qc2 and Qc3 outputs. This inversion will not affect the output–output skew of the device. This inversion allows for the development of 180° phase shifted clocks. This output could also be used as a feedback output to the MPC972/973 or a second PLL device to generate early or late clocks for a specific design. Figure 7 illustrates the use of two MPC972/973's to generate two banks of clocks with one bank divided by 2 and delayed by 180° relative to the first.

Using the MPC973 as a Zero Delay Buffer

The external feedback of the MPC973 clock driver allows for its use as a zero delay buffer (if the TCLK inputs are used the MPC972 can also be used a zero delay buffer). By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The feedback divider affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs. Because the static phase offset is a function of the feedback divisor the Tpd of the MPC973 is a function of the feedback configuration used. The Tpd of the device is specified in the specification tables.

When used as a zero delay buffer the MPC973 will likely be in a nested clock tree application. For these applications the MPC973 offers a LVPECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The MPC973 then can lock onto the LVPECL reference and translate with near zero delay to low skew LVCMOS outputs. Clock trees implemented in this fashion will show significantly tighter skews than trees developed from CMOS fanout buffers.

To minimize part–to–part skew the external feedback option again should be used. The PLL in the MPC973 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only ±150ps, thus for multiple devices under identical configurations the part–to–part skew will be around 650ps (300ps for Tpd variation plus 350ps output–to–output skew). For devices that are configured differently one must account for the differences between the nominal delays of the multiple devices.

SYNC Output Description

In situations where output frequency relationships are not integer multiples of each other there is a need for a signal for system synchronization purposes. The SYNC output of the MPC972/973 is designed to specifically address this need. The MPC972/973 monitors the relationship between the Qa and the Qc banks of outputs. It provides a low going pulse, one period in duration, one period prior to the coincident rising edges of the Qa and Qc outputs. The duration and the placement of the pulse is dependent on the higher of the Qa and Qc output frequencies. The timing diagrams in the data sheet show the various waveforms for the SYNC output. Note that the SYNC output is defined for all possible combinations of the Qa and Qc outputs even though under some relationships the lower frequency clock could be used as a synchronizing signal.

Table 1. Programmable Output Frequency Relationships (VCO_Sel='1')

fsela1	fsela0	Qa	fselb1	fselb0	Qb	fselc1	fselc0	Qc
0	0	VCO/4	0	0	VCO/4	0	0	VCO/2
0	1	VCO/6	0	1	VCO/6	0	1	VCO/4
1	0	VCO/8	1	0	VCO/8	1	0	VCO/6
1	1	VCO/12	1	1	VCO/10	1	1	VCO/8

Table 2. Programmable Output Frequency Relationships (VCO_Sel='1')

fselFB2	fselFB1	fselFB0	QFB
0	0	0	VCO/4
0	0	1	VCO/6
0	1	0	VCO/8
0	1	1	VCO/10
1	0	0	VCO/8
1	0	1	VCO/12
1	1	0	VCO/16
1	1	1	VCO/20

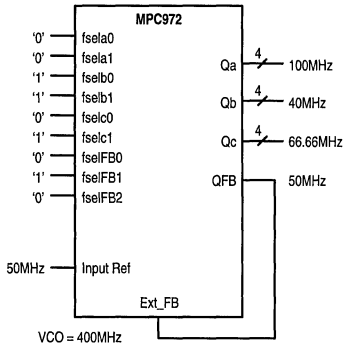


Figure 4. Programming Configuration Example

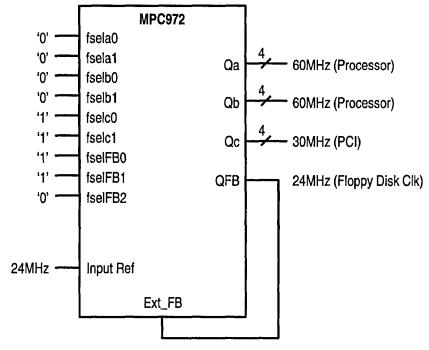


Figure 5. Generating Pentium Clocks from Floppy Clock

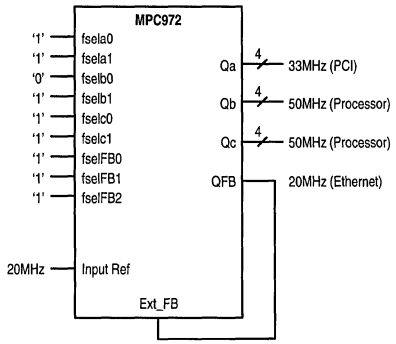


Figure 6. Generating MPC604 Clocks from Ethernet Clocks

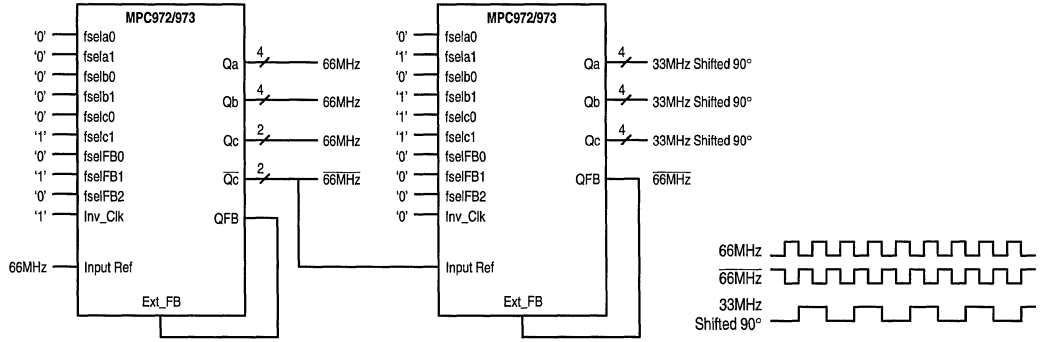


Figure 7. Phase Delay Using Multiple MPC972/973's

Using the On–Board Crystal Oscillator

The MPC972/973 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC972/973 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required. In addition, with crystals with a higher shunt capacitance, it may be necessary to place a 1k resistor across the two crystal leads.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC972/973 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 3. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω Max
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

The MPC972/973 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal.

Power Supply Filtering

The MPC972/973 is a mixed analog/digital product and exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC972/973 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC972/973.

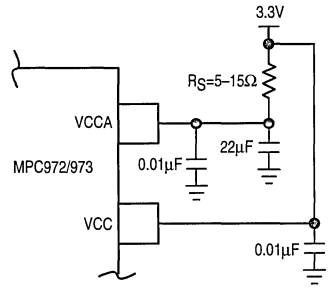


Figure 8. Power Supply Filter

Figure 8 illustrates a typical power supply filter scheme. The MPC972/973 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC972/973. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 8 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC972/973 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be

adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC972/973 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC972/973 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 9 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC972/973 clock driver is effectively doubled due to its capability to drive multiple lines.

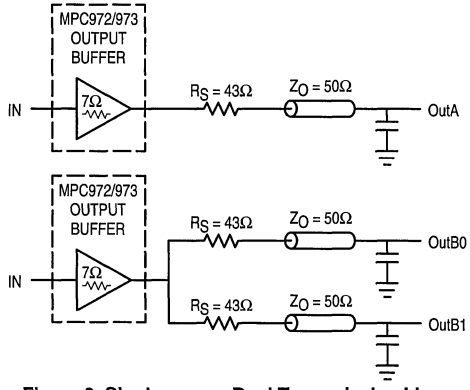


Figure 9. Single versus Dual Transmission Lines

The waveform plots of Figure 10 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC972/973 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC972/973. The output waveform in Figure 10 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 11 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

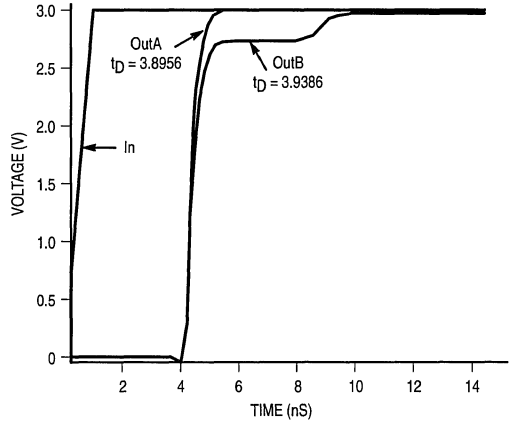
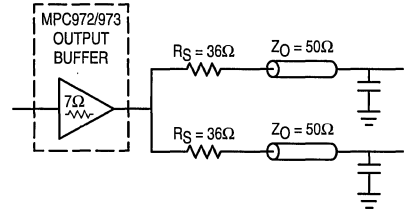


Figure 10. Single versus Dual Waveforms



$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

Figure 11. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Using the Output Freeze Circuitry

With the recent advent of a "green" classification for computers the desire for unique power management among system designers is keen. The individual output enable

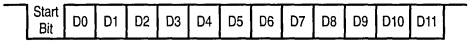
control of the MPC972/973 allows designers, under software control, to implement unique power management schemes into their designs. Although useful, individual output control at the expense of one pin per output is too high, therefore a simple serial interface was derived to economize on the control pins.

The freeze control logic provides a mechanism through which the MPC972 clock outputs may be frozen (stopped in the logic '0' state):

The freeze mechanism allows serial loading of the 12–bit Serial Input Register, this register contains one programmable freeze enable bit for 12 of the 14 output clocks. The Qc0 and QFB outputs cannot be frozen with the serial port, this avoids any potential lock up situation should an error occur in the loading of the Serial Input Register. The user may programmably freeze an output clock by writing logic '0' to the respective freeze enable bit. Likewise, the user may programmably unfreeze an output clock by writing logic '1' to the respective enable bit.

The freeze logic will never force a newly–frozen clock to a logic '0' state before the time at which it would normally transition there. The logic simply keeps the frozen clock at logic '0' once it is there. Likewise, the freeze logic will never force a newly–unfrozen clock to a logic '1' state before the time at which it would normally transition there. The logic re–enables the unfrozen clock during the time when the respective clock would normally be in a logic '0' state, eliminating the possibility of 'runt' clock pulses.

The user may write to the Serial Input register through the Frz_Data input by supplying a logic '0' start bit followed serially by 12 NRZ freeze enable bits. The period of each Frz_Data bit equals the period of the free–running Frz_Clk signal. The Frz_Data serial transmission should be timed so the MPC972 can sample each Frz_Data bit with the rising edge of the free–running Frz_Clk signal.



D0–D3 are the control bits for Qa0–Qa3, respectively
D4–D7 are the control bits for Qb0–Qb3, respectively
D8–D10 are the control bits for Qc1–Qc3, respectively
D11 is the control bit for QSync

Figure 12. Freeze Data Input Protocol

3.3V PLL Clock Driver

MPC974

LOW VOLTAGE PLL CLOCK DRIVER

The MPC974 is a fully integrated PLL based clock generator and clock distribution chip which operates from a 3.3V supply. The MPC974 is ideally suited for high speed, timing critical designs which need a high level of clock fanout. The device features 15 high drive LVCMOS outputs, each output has the capability of driving a 50Ω parallel terminated transmission line or two 50Ω series terminated transmission lines on the incident edge.

- Fully Integrated PLL
- Two Reference Clock Inputs for Redundant Clock Applications
- High Impedance Output Control
- Logic Enable on the Outputs
- 3.3V V_{CC} Supply
- Output Frequency Configurable
- TQFP Packaging
- ±100ps Typical Cycle–to–Cycle Jitter

FA SUFFIX
52–LEAD TQFP PACKAGE
CASE 848D-03

The MPC974 features 3 independent frequency programmable banks of outputs. The frequency programmability offers the capability of establishing output frequency relationships of 1:1, 2:1, 3:1, 3:2 and 3:2:1. In addition, the device features a separate feedback output which allows for a wide variety of input/output frequency multiplication alternatives. The VCO_Sel pin provides an extended VCO lock range for added flexibility and general purpose usage.

The TCLK0 and TCLK1 inputs provide a method for dynamically switching the PLL between two different clock sources. The PLL has been optimized to provide small deviations in output pulse width and well controlled, slow transition back to lock when the inputs are switched between two references that are equal in frequency but out of phase with each other. This feature makes the MPC974 an ideal solution for fault tolerant applications which require redundant clock sources.

All of the control pins are LVTTL/LVCMOS level inputs. The Fsel pins control the VCO divide ratios that are applied to the various output banks and the feedback output. The $\overline{MR}$ input will reset the internal flip flops and place the outputs in high impedance when driven LOW. The OE pin will force all of the outputs except the feedback output LOW to allow for acquiring phase lock prior to providing clocks to the rest of the system. Note that the OE pin is not synchronized to the internal clock. As a result, the initial pulse after de–assertion of the OE pin may be distorted. The PLL_En pin allows the PLL to be bypassed for board level functional test. When bypassed the signal on the selected TCLK will be routed around the PLL and will drive the internal dividers directly.

The MPC974 is packaged in the 52–lead TQFP package to provide optimum electrical performance as well as minimize board space requirements. The device is specified for 3.3V V_{CC}.

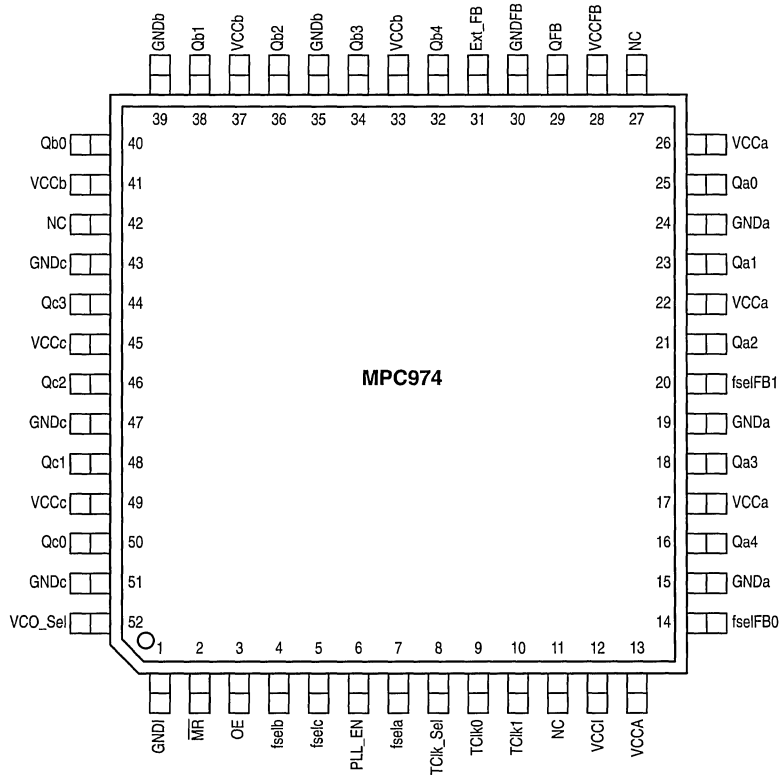


Figure 1. 52–Lead Pinout (Top View)

FUNCTION TABLE 1

fsela	Qa	fselb	Qb	fselc	Qc
0	÷2	0	÷2	0	÷4
1	÷4	1	÷4	1	÷6

FUNCTION TABLE 2

fselFB0	fselFB1	QFB
0	0	÷4
0	1	÷6
1	0	÷8
1	1	÷12

FUNCTION TABLE 3

VCO_Sel	fVCO
0	VCO/2
1	VCO/4

FUNCTION TABLE 4

Control Pin	Logic '0'	Logic '1'
$\overline{MR}$	Master Reset/Output High Z	–
PLL_EN	Bypass PLL	Enable PLL
TClk_Sel	TCLK0	TCLK1
OE	Qa, Qb, Qc Logic LOW	All Outputs Enabled

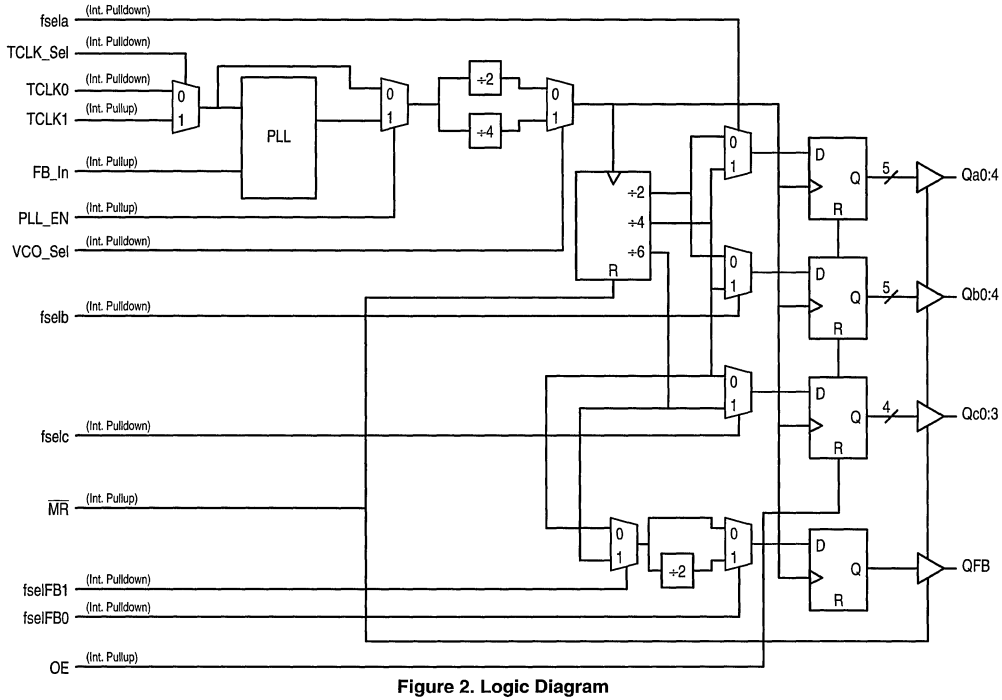


Figure 2. Logic Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	5.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		8	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20mA (Note 1.)
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20mA (Note 1.)
I_{IN}	Input Current			±100	µA	Note 2.
I_{CC}	Maximum Quiescent Supply Current			120	mA	
C_{IN}	Input Capacitance			8	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output

1. The MPC974 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
2. Inputs have either pull–up or pull–down resistors which affect input current.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 3.	Note 3.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

3. Input reference frequency is limited by the divider selection and the VCO lock range.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time (Note 4.)	0.15		1.5	ns	0.8 to 2.0V
t_{pw}	Output Duty Cycle (Note 4.)	$t_{CYCLE}/2$ −800	$t_{CYCLE}/2$ ±500	$t_{CYCLE}/2$ +800	ps	
f_{VCO}	PLL VCO Lock Range fseln, fselFBn = ÷4 to ÷12	200		500	MHz	Note 5.
t_{pd}	SYNC to Feedback Propagation Delay	−250		100	ps	Notes 4., 6.
t_{os}	Output-to-Output Skew			350	ps	Note 4.
f_{max}	Maximum Output Frequency Q (÷2) Q (÷4) Q (÷6)			125 63 42	MHz	VCO_Sel = 0
t_{PZL}	Output Enable Time	2		10	ns	
t_{PLZ}, t_{PHZ}	Output Disable Time	2		10	ns	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)		±100		ps	
t_{lock}	Maximum PLL Lock Time			10	ms	

4. 50Ω transmission lines terminated to $V_{CC}/2$.
5. The PLL will be unstable if the total divide between the VCO and the feedback pin is less < 8. VCO_SEL = '0', fsela or fselb = '0' cannot be used for the PLL feedback signal.
6. t_{pd} is specified for 50MHz input reference. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

APPLICATIONS INFORMATION

Programming the MPC974

The MPC974 clock driver outputs can be configured into several frequency relationships, in addition the external feedback option allows for a great deal of flexibility in establishing unique input–to–output frequency relationships. The output dividers for the four output groups allows the user to configure the outputs into 1:1, 2:1, 3:2 and 3:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Function Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 3:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's and Qc's at VCO/4 and the Qd's at VCO/6. These settings will provide output frequencies with a 3:2:1 relationship.

The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The VCO lock range can be found in the specification tables. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 10 and 125MHz the MPC974 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. The separate PLL feedback output allows for a wide range of output vs input frequency relationships. Function Table 1 can be used to identify the potential relationships available. Figure 3 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

Using the MPC974 as a Zero Delay Buffer

The external feedback option of the MPC974 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is near zero. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The static phase offset is a function of the input reference frequency of the MPC974. The Tpd of the device is specified in the specification tables.

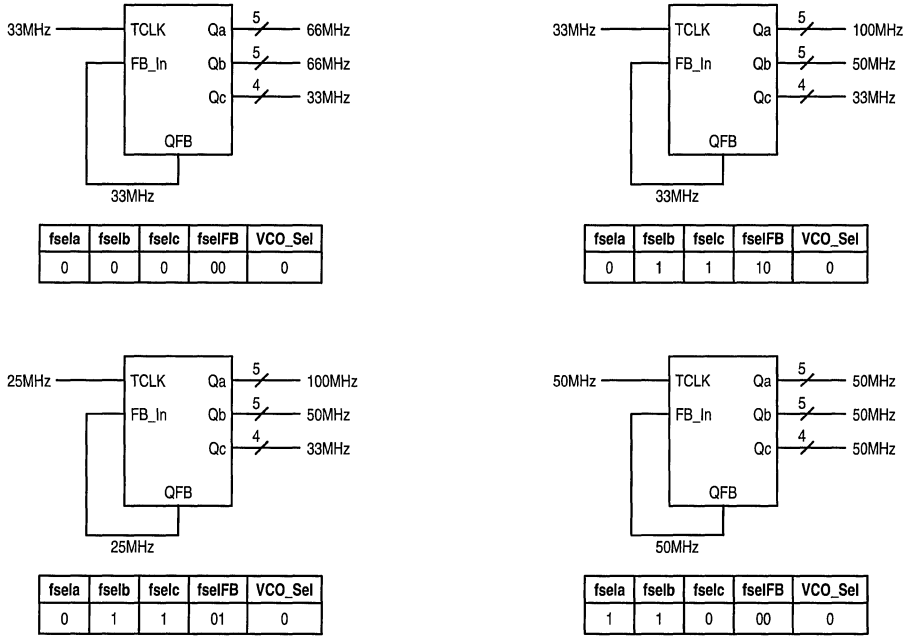


Figure 3. MPC974 Programming Schemes

To minimize part–to–part skew the external feedback option again should be used. The PLL in the MPC974 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only ±150ps, thus for multiple devices under identical configurations the part–to–part skew will be around 850ps (300ps for Tpd variation plus 350ps output–to–output skew plus 200ps for jitter). To minimize this value, the highest possible reference frequencies should be used. Higher reference frequencies will minimize both the t_{pd} parameter as well as the input to output jitter.

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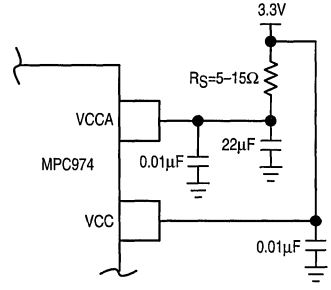

Figure 4. Power Supply Filter

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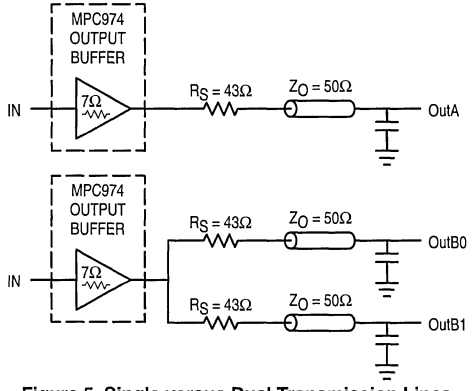

Figure 5. Single versus Dual Transmission Lines

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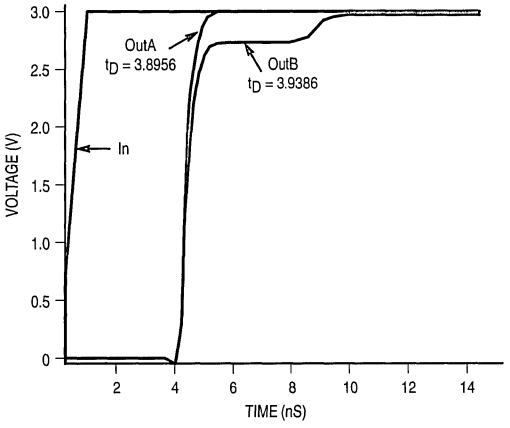


Figure 6. Single versus Dual Waveforms

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 7 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

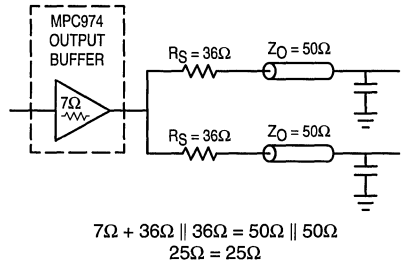


Figure 7. Optimized Dual Line Termination

Dual 3.3V PLL Clock Generator

MPC980

DUAL 3.3V PLL CLOCK GENERATOR

The MPC980 is a 3.3V dual PLL clock generator targeted for high end Pentium™ and PowerPC™ 603/604 personal computers. The MPC980 synthesizes processor as well as PCI clocks from a 14.31818MHz external crystal. In addition the device provides two buffered outputs of the 14.31818MHz crystal as well as a 40MHz SCSI clock, a 24MHz floppy clock and a12MHz keyboard clock. One of the buffered 14.31818MHz outputs can be configured to provide a 16MHz output rather than the second copy of the 14.31818MHz output.

- Provides Processor and System Clocks for Pentium™ Designs
- Provides Processor and System Clocks for PowerPC™ 603/604 Designs
- Two Fully Integrated Phase–Locked Loops
- Cycle–Cycle Jitter of ±150ps
- Operates from 3.3V Supply
- 52–Lead TQFP Packaging

FA SUFFIX
TQFP PACKAGE
CASE 848D–02

The processor clock outputs of the MPC980 can be programmed to provide 50, 60 or 66MHz. Under all processor output frequencies the PCI clock outputs will be equal to one half the processor clock outputs. The PCI outputs will run synchronously to the processor clock outputs. There are a total of ten output clocks which can be split into a group of four and a group of six. Either group can be configured as processor or PCI clocks. Each of the outputs can drive two series terminated transmission lines allowing for the driving of up to twelve independent processor loads and eight PCI clock loads. A pin selectable option is available to delay the PCI clock outputs relative to the processor clocks. The amount of delay is a function of the processor clock frequency and varies from 2ns to 6ns.

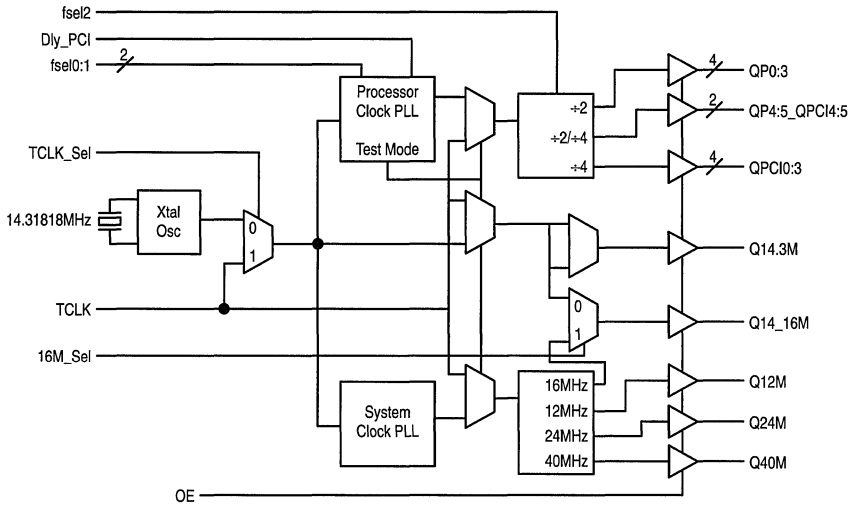
The output jitter of the the PLL at 66MHz output is ±150ps peak to peak, cycle to cycle (the worst case deviation of the clock period is guaranteed to be less than ±150ps). The skews between one processor clock and any other processor clock (or one PCI clock to any other PCI clock) is 350ps (±175ps). The worst case skew between the processor clocks and the PCI clocks is 500ps (±250ps).

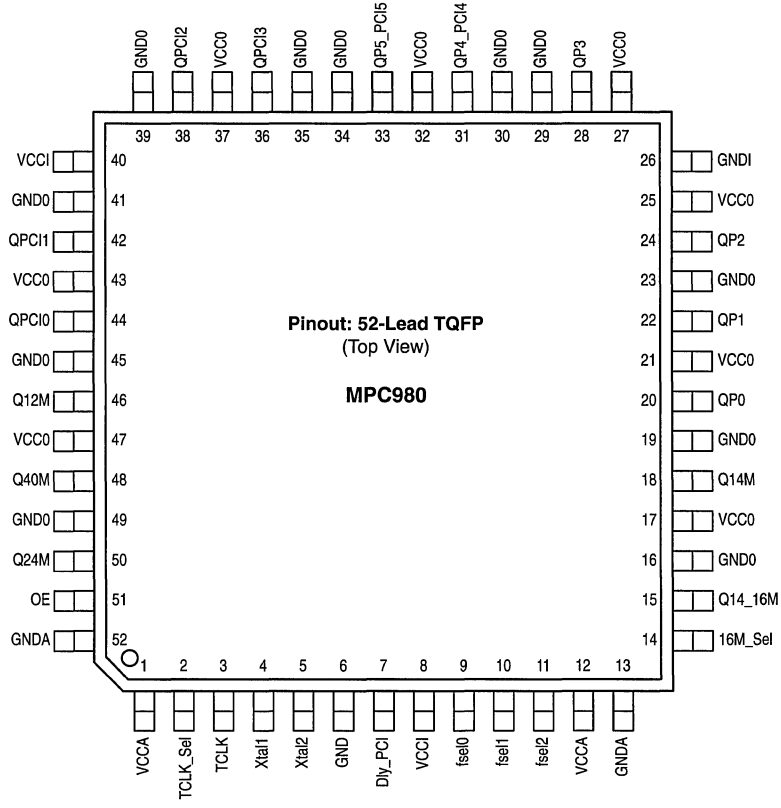
An output enable pin is provided to tristate all of the outputs for board level test. In addition a testing mode is provided to allow for the bypass of the PLL's for board level functional debug.

The product is packaged in a 52–lead TQFP to optimize board space and power supply distribution. The TQFP package occupies a 12mm x 12mm space on the PCB.

Pentium is a trademark of Intel Corporation. PowerPC is a trademark of International Business Machines Corporation.

LOGIC DIAGRAM





Pinout: 52-Lead TQFP
(Top View)

MPC980

FUNCTION TABLE 1

OE	fsel0	fsel1	QP	QPCI	Q14M	Q16M	Q24M	Q12M	Q40M
0	X	X	High Impedance	High Impedance	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z
1	0	0	50MHz	25MHz	14.31818	16	24	12	40
1	0	1	60MHz	30MHz	14.31818	16	24	12	40
1	1	0	66MHz	33MHz	14.31818	16	24	12	40
1	1	1	TCLK/2	TCLK/4	TCLK	TCLK/6	TCLK/4	TCLK/8	TCLK/2

FUNCTION TABLE 2

Dly_PCI	QP/QPCI Relationship
0	Synchronous Processor & PCI Clocks
1	PCI Clocks Lag Processor Clocks

FUNCTION TABLE 3

fsel2	QP/QPCI Output Configuration
0	6 Processor and 4 PCI Clocks
1	4 Processor and 6 PCI Clocks

FUNCTION TABLE 4

TCLK_Sel	PLL Input Reference
0	Crystal Oscillator
1	TCLK

DC CHARACTERISTICS (T_A = 0° to 70°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{CC}	Power Supply Voltage	3.3–5%	3.3	3.3+5%	V	
V_{IL}	Input LOW Voltage			$0.3V_{CC}$	V	
V_{IH}	Input HIGH Voltage	$0.7V_{CC}$		V_{CC}	V	
V_{OH}	Output HIGH Voltage	V_{CC} –0.4			V	–20mA (Note 1.)
V_{OL}	Output LOW Voltage			0.4	V	+20mA (Note 1.)
C_{IN}	Input Capacitance			4.5	pF	
I_{CC}	Quiescent Supply Current			190	mA	

1. Output can drive two series terminated 50Ω transmission lines or a single 50Ω line terminated 50Ω into $V_{CC}/2$.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
f_{Xtal}	Input Crystal Frequency			14.31818		MHz	
f_{max}	Maximum Output Frequency	QP QPCI			66 33	MHz	
t_{dc}	Output Duty Cycle		$t_{CYCLE}/2$ −1000	$t_{CYCLE}/2$ ±500	$t_{CYCLE}/2$ +1000	ps	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)	66/33MHz 60/30MHz 50/25MHz			±150 ±200 ±250	ps	
t_{skew}	Output–to–Output Skew	QP to QP QPCI to QPCI QP to QPCI			350 350 500	ps	Rising Edges Only; Dly_PCI = 0
t_{delay}	Time Delay	QP to QPCI	2	$\frac{1}{4f_{QP}}$	$\frac{1}{4f_{QP}} + 1$	ns	Dly_PCI = 1
t_r, t_f	Output Rise/Fall Time		0.05		0.8	ns	1.0 to 1.8V
t_{LOCK}	PLL Lock Time				10	ms	
t_{PZL}, t_{PZH}	Output Enable Time		3		10	ns	50Ω to $V_{CC}/2$
t_{PLZ}, t_{PHZ}	Output Disable Time		4		11	ns	50Ω to $V_{CC}/2$

APPLICATIONS INFORMATION

Using the On–Board Crystal Oscillator

The MPC980 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC980 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC980 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 4. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental at Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150ppm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω Max
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Low Voltage PLL Clock Driver

MPC990
MPC991

LOW VOLTAGE
PLL CLOCK DRIVER

The MPC990/991 is a 3.3V compatible, PLL based ECL/PECL clock driver. The fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC990/991 makes the device ideal for Workstation, Mainframe Computer and Telecommunication applications. The MPC990 and MPC991 devices are identical except in the interface to the reference clock for the PLL. The MPC990 offers an on–board crystal oscillator as the PLL reference while the MPC991 offers a differential ECL/PECL input for applications which need to lock to an existing clock signal. Both designs offer a secondary single–ended ECL clock for system test capabilities.

- Fully Integrated PLL
- Output Frequency Up to 400MHz
- ECL/PECL Inputs and Outputs
- Operates from a 3.3V Supply
- Output Frequency Configurable
- TQFP Packaging
- ±50ps Cycle–to–Cycle Jitter

FA SUFFIX
52–LEAD TQFP PACKAGE
CASE 848D–03

The MPC990/991 offers three banks of outputs which can each be programmed via the the four fsel pins of the device. There are 16 different output frequency configurations available in the device. The configurations include output ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 4:3:1 and 4:3:2. The programming table in this data sheet illustrates the various programming options. The SYNC output monitors the relationship between the Qa and Qc output banks. The output pulses per the timing diagrams in this data sheet signal the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies (i.e., 3:2 or 4:3 relationships). The Sync_Sel input toggles the Qd outputs between sync signals and extensions to the Qc bank of outputs.

The MPC990/991 provides a separate output for the feedback to the PLL. This allows for the feedback frequency to be programmed independently of the other outputs allowing for unique input vs output frequency relationships. The fselFB inputs provide 6 different feedback frequencies from the QFB differential output pair.

The MPC990/991 features an external differential ECL/PECL feedback to the PLL. This external feedback feature allows for the MPC991's use as a "zero" delay buffer. The propagation delay between the input reference and the output is dependent on the input reference frequency. The selection of higher reference frequencies will provide near zero delay through the device.

The PLL_En, Ref_Sel and the Test_Clk input pins provide a means of bypassing the PLL and driving the output buffers directly. This allows the user to single step a design during system debug. Note that the Test_Clk input is routed through the dividers so that depending on the programming several edges on the Test_Clk input will be needed to get corresponding edge transitions on the outputs. The VCO_Sel input provides a means of recentering the VCO to provide a broader range of VCO frequencies for stable PLL operation.

If the frequency select or the VCO_Sel pins are changed during operation, a master reset signal must be applied to ensure output synchronization and phase–lock. If the VCO is driven beyond its maximum frequency, the VCO can outrun the internal dividers when the VCO_Sel pin is low. This will also prevent the PLL from achieving lock. Again, a master reset signal will need to be applied to allow for phase–lock. The device employs a power–on reset circuit which will ensure output synchronization and PLL lock on initial power–up.

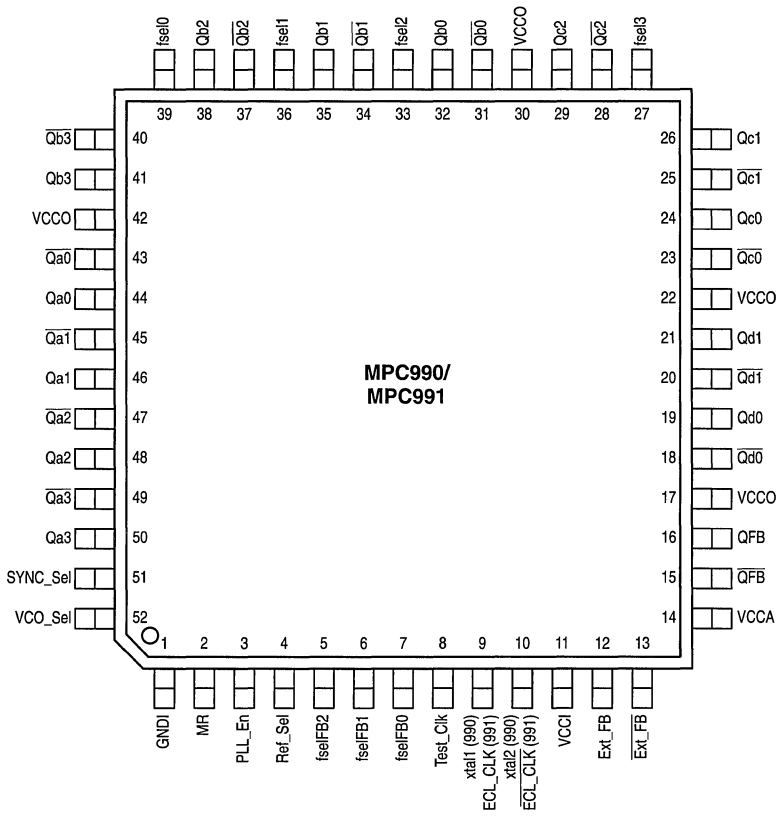


Figure 1. 52–Lead Pinout (Top View)

FUNCTION TABLE 1

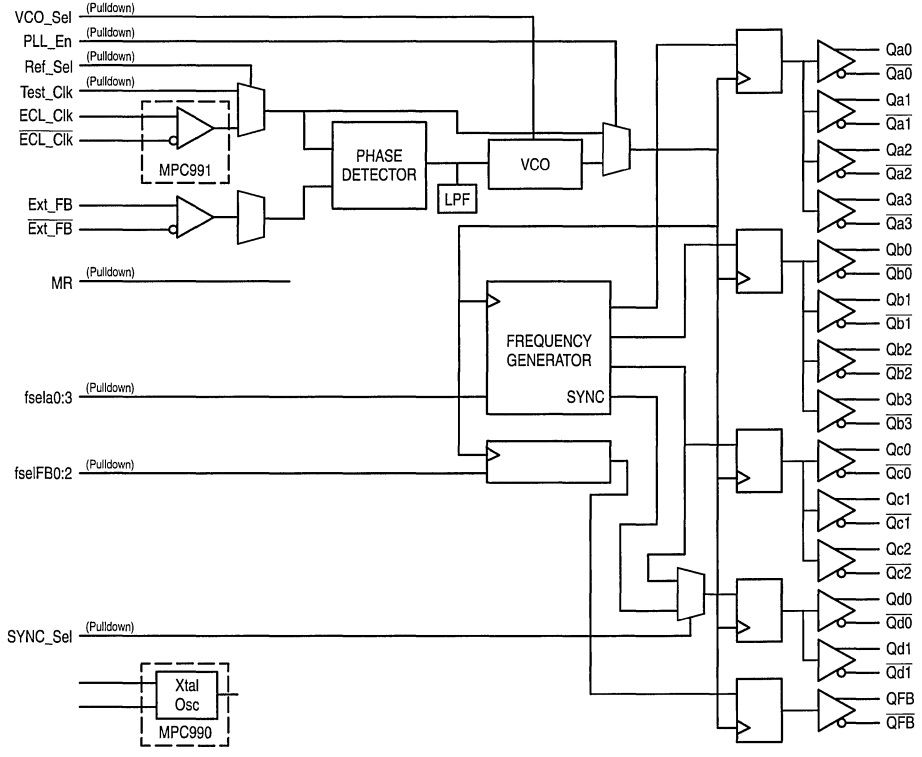
INPUTS				OUTPUTS		
fsel3	**fsel2**	**fsel1**	**fsel0**	**Qa**	**Qb**	**Qc**
0	0	0	0	÷2	÷2	÷2
0	0	0	1	÷2	÷2	÷4
0	0	1	0	÷2	÷4	÷4
0	0	1	1	÷2	÷2	÷6
0	1	0	0	÷2	÷6	÷6
0	1	0	1	÷2	÷4	÷6
0	1	1	0	÷2	÷4	÷8
0	1	1	1	÷2	÷6	÷8
1	0	0	0	÷2	÷2	÷8
1	0	0	1	÷2	÷8	÷8
1	0	1	0	÷4	÷4	÷6
1	0	1	1	÷4	÷6	÷6
1	1	0	0	÷4	÷6	÷8
1	1	0	1	÷6	÷6	÷8
1	1	1	0	÷6	÷8	÷8
1	1	1	1	÷8	÷8	÷8

FUNCTION TABLE 2

fselFB2	fselFB1	fselFB0	QFB
0	0	0	÷2
0	0	1	÷4
0	1	0	÷6
0	1	1	÷8
1	0	0	÷8
1	0	1	÷16
1	1	0	÷24
1	1	1	÷32

FUNCTION TABLE 3

Control Pin	Logic '0'	Logic '1'
PLL_En	Enable PLL	Bypass PLL
VCO_Sel	fVCO	fVCO/2
Ref_Sel	xtal or ECL/PECL	Test_Clk
MR	—	Reset Outputs
SYNC_Sel	SYNC Outputs	Match Qc Outputs



NOTE: ECL_Clk, Ext_FB have internal pulldowns, while $\overline{\text{ECL\_Clk}}$, $\overline{\text{Ext\_FB}}$ have external pullups to ensure stability under open input conditions.

Figure 2. MPC990/991 Logic Diagram

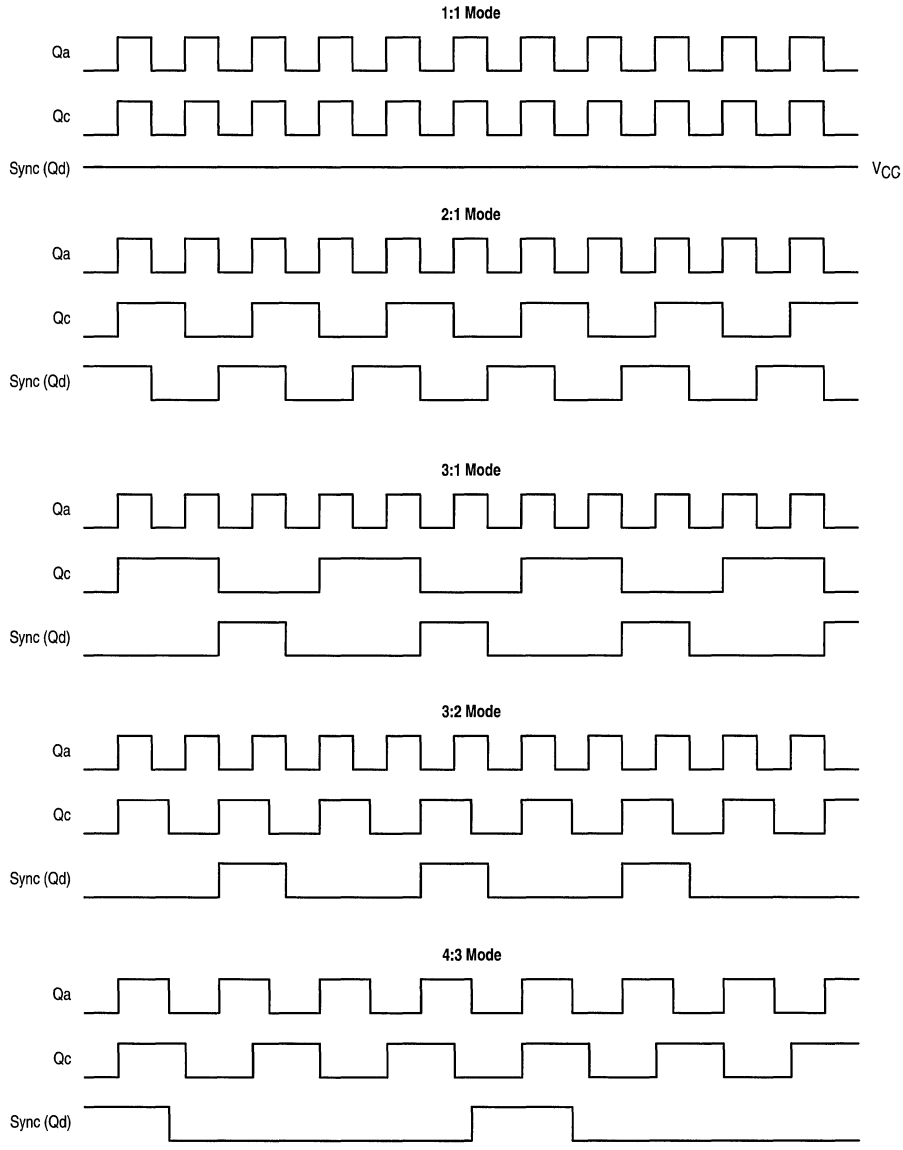


Figure 3. Timing Diagrams

ECL DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCA} = V_{CCI} = V_{CCO} = 0V, GNDI = –3.3V ±5%, Note 1.)

		0°C			25°C			70°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	–1.3		–0.7	–1.3	–1.0	–0.7	–1.3		–0.7	V
V_{OL}	Output LOW Voltage	–2.0		–1.4	–2.0	–1.7	–1.4	–2.0		–1.4	V
V_{IH}	Input HIGH Voltage	–1.1		–0.9	–1.1		–0.9	–1.1		–0.9	V
V_{IL}	Input LOW Voltage	–1.8		–1.5	–1.8		–1.5	–1.8		–1.5	V
V_{PP}	Minimum Input Swing	500			500			500			mV
V_{CMR}	Common Mode Range	V_{CC} –1.3V		V_{CC} –0.5V	V_{CC} –1.3V		V_{CC} –0.5V	V_{CC} –1.3V		V_{CC} –0.5V	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{GNDI}	Power Supply Current		200	240		200	240		200	240	mA

1. Refer to Motorola Application Note AN1545/D "*Thermal Data for MPC Clock Drivers*" for thermal management guidelines.

PECL DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCA} = V_{CCI} = V_{CCO} = 3.3V ±5%, GNDI = 0V, Note 2.)

		0°C			25°C			70°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (Note 3.)	2.0		2.6	2.0	2.3	2.6	2.3		2.6	V
V_{OL}	Output LOW Voltage (Note 3.)	1.3		1.9	1.3	1.6	1.9	1.3		1.9	V
V_{IH}	Input HIGH Voltage (Note 3.)	2.2		2.4	2.2		2.4	2.2		2.4	V
V_{IL}	Input LOW Voltage (Note 3.)	1.5		1.8	1.5		1.8	1.5		1.8	V
V_{PP}	Minimum Input Swing	500			500			500			mV
V_{CMR}	Common Mode Range	V_{CC} –1.3V		V_{CC} –0.5V	V_{CC} –1.3V		V_{CC} –0.5V	V_{CC} –1.3V		V_{CC} –0.5V	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{GNDI}	Power Supply Current		200	240		200	240		200	240	mA

2. Refer to Motorola Application Note AN1545/D "*Thermal Data for MPC Clock Drivers*" for thermal management guidelines.
3. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCA} = V_{CCI} = V_{CCO} = 3.3V ±5%, Termination of 50Ω to V_{CC} – 2.0V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
f_{xtal}	Crystal Oscillator Frequency		10		25	MHz	
t_r, t_f	Output Rise/Fall Time		0.2		1.0	ns	20% to 80%
t_{pw}	Output Duty Cycle		47.5	50	52.5	%	
t_{os}	Output-to-Output Skew	Same Frequency		150	250	ps	
		Different Frequencies		250	350		
f_{VCO}	PLL VCO Lock Range	VCO_Sel = '0'	400		800	MHz	FB ÷8 to ÷32 (Note 4.)
		VCO_Sel = '1'	200		400		FB ÷4 to ÷32
t_{pd}	Ref to Feedback Offset		75	250	425	ps	f_{ref} = 50MHz (Note 5.)
f_{max}	Maximum Output Frequency	Qa,Qb,Qc (÷2)			400	MHz	
		Qa,Qb,Qc (÷4)			200		
		Qa,Qb,Qc (÷6)			133		
		Qa,Qb,Qc (÷8)			100		
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)			±50		ps	
t_{lock}	Maximum PLL Lock Time				10	ms	

4. With VCO_Sel = '0', the PLL will be unstable with a ÷2, ÷4 or ÷6 feedback ratio. With VCO_Sel = '1', the PLL will be unstable with a ÷2 feedback ratio.
5. t_{pd} is specified for 50MHz input reference FB ÷8. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 6.	Note 6.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

6. Maximum and minimum input reference frequencies are limited by the VCO lock range and the feedback divider.

APPLICATIONS INFORMATION

Using the On–Board Crystal Oscillator

The MPC990 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC990 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most of the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC990 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

The MPC990 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal.

Table 5. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental at Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω Max
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MPC990/991 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC990/991 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC990/991.

Figure 4 illustrates a typical power supply filter scheme. The MPC990/991 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter

should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC990/991. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 4 must have a resistance of 5–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC990/991 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

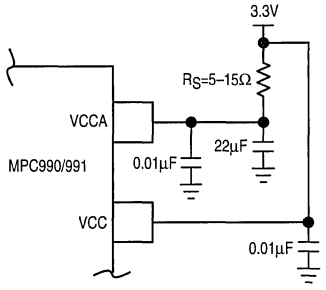


Figure 4. Power Supply Filter

Low Voltage PECL PLL Clock Driver

MPC992

LOW VOLTAGE PLL CLOCK DRIVER

FA SUFFIX
PLASTIC TQFP PACKAGE
CASE 873A-02

The MPC992 is a 3.3V compatible, PLL based PECL clock generator and distributor. The fully differential design ensures optimum skew and PLL jitter performance. The performance of the device makes the MPC992 ideal for workstations, main frame computer, telecommunication and instrumentation applications. The device offers a crystal oscillator or a differential PECL reference clock input to provide flexibility in the reference clock interface. All of the control signals to the MPC992 are LVTTL compatible inputs.

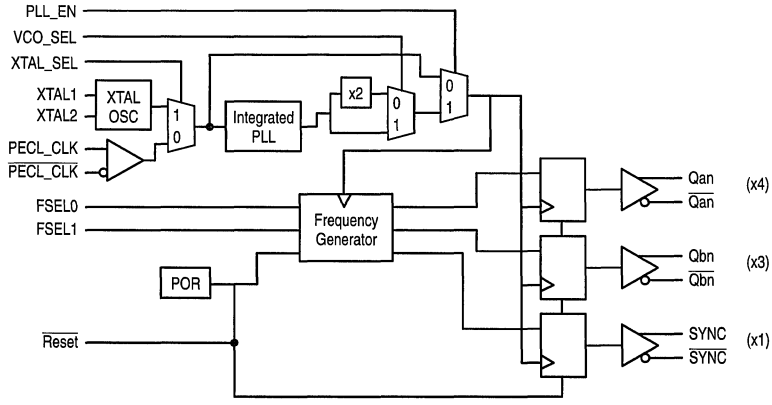
- Fully Integrated PLL
- Output Frequency of up to 400MHz
- PECL Clock Inputs and Outputs
- Operates from a 3.3V V_{CC} Supply
- Output Frequency Configurable
- 32 TQFP Packaging
- ±25ps Cycle–Cycle Jitter

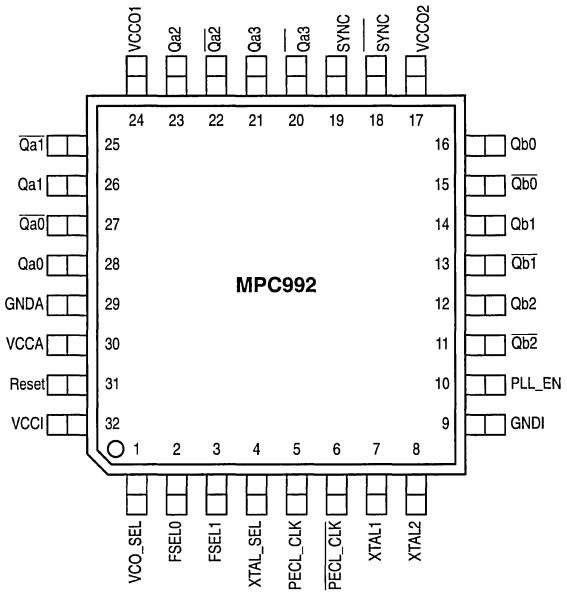
The MPC992 offers two banks of outputs which can be configured into four different relationships. The output banks can be configured into 2:1, 3:1, 3:2 and 5:2 ratios to provide a wide variety of potential frequency outputs. In addition to these two banks of outputs a synchronization output is also offered. The SYNC output will provide information as to the time when the two output banks will transition positively in phase. This information can be important when the odd ratios are used as it provides for a baseline point in the system timing. The SYNC output will pulse high for one Qa clock period, centered on the rising Qa clock edge four edges prior to the Qb synchronous edge. The relationship is illustrated in the timing diagrams in the data sheet.

The MPC992 offers several features to aid in system debug and test. The PECL reference input pins can be interfaced to a test signal and the PLL can be bypassed to allow the designer to drive the MPC992 outputs directly. This allows for single stepping in a system functional debug mode. In addition an overriding reset is provided which will force all of the Q outputs LOW upon assertion.

The MPC992 is packaged in a 32–lead TQFP package to optimize both performance and board density.

MPC992 LOGIC DIAGRAM





FUNCTION TABLE 1

FSEL0	FSEL1	Qa	Qb	Feedback	Ratio
0	0	VCO/4	VCO/6	VCO/24	3:2
0	1	VCO/2	VCO/4	VCO/16	2:1
1	0	VCO/4	VCO/10	VCO/40	5:2
1	1	VCO/2	VCO/6	VCO/24	3:1

INPUT vs OUTPUT FREQUENCY

FSEL0	FSEL1	Qa	Qb	Int Feedback
0	0	6 (f_{ref})	4 (f_{ref})	f_{ref}
0	1	8 (f_{ref})	4 (f_{ref})	f_{ref}
1	0	10 (f_{ref})	4 (f_{ref})	f_{ref}
1	1	12 (f_{ref})	4 (f_{ref})	f_{ref}

FUNCTION TABLE 2

Control Signal	Logic '0'	Logic '1'
Reset	Outputs Enabled	Outputs Disabled
XTAL_SEL	PECL REF	XTAL REF
PLL_EN	Disabled	Enabled
VCO_SEL	High Frequency	Low Frequency

PIN DESCRIPTION

Pin Name	Function
VCO_SEL	VCO range select pin (Int Pullup)
PLL_EN	PLL bypass select pin (Int Pullup)
XTAL_SEL	Input reference source select pin (Int Pullup)
XTAL1:2	Crystal interface pins for the internal oscillator
PECL_CLK	True PECL reference clock input (Int Pulldown)
$\overline{\text{PECL\_CLK}}$	Compliment PECL reference clock input (Int Pullup)
FSELn	Internal divider select pins (Int Pullup)
RESET	Internal flip–flop reset, true outputs go LOW (Int Pulldown)

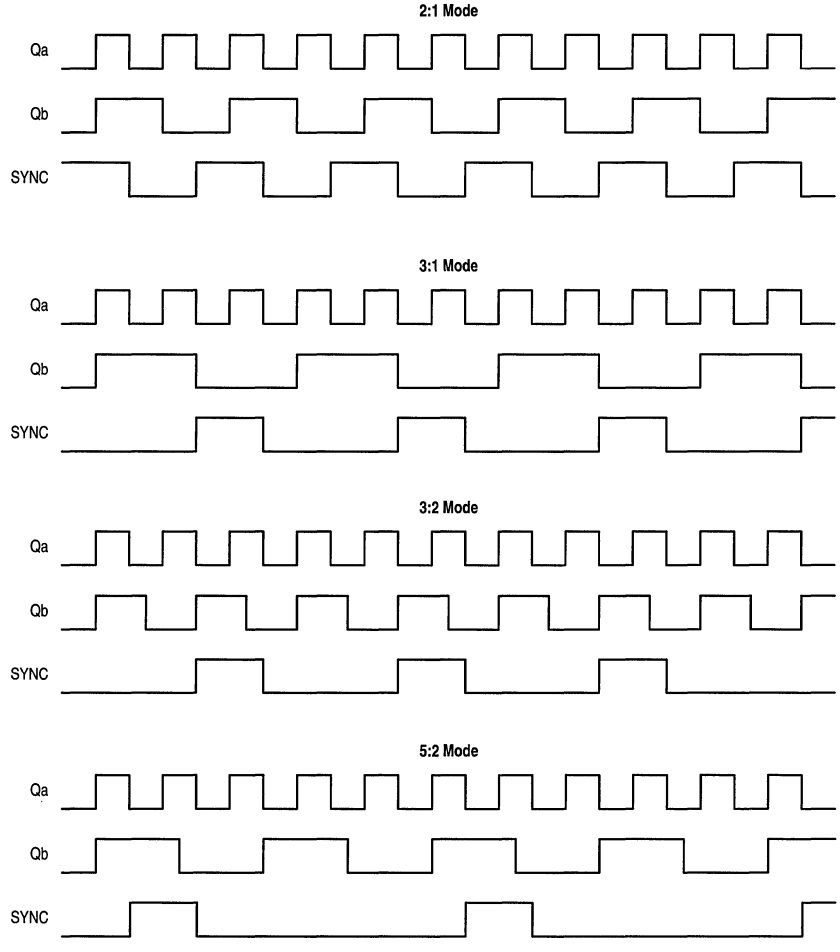


Figure 1. Output Waveforms

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{OUT}	Output Current Continuous Surge		50 100	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	PECL_CLK[1] Other	2.15 2.0		2.4 V_{CC}	V	V_{CC} = 3.3V
V_{IL}	Input LOW Voltage	PECL_CLK[1] Other	1.5 0		1.8 0.8	V	V_{CC} = 3.3V
V_{OH}	Output HIGH Voltage[1]		1.8		2.4	V	V_{CC} = 3.3V
V_{OL}	Output LOW Voltage[1]		1.2		1.7	V	V_{CC} = 3.3V
I_{IN}	Input Current		–120		120	µA	
I_{CCI}	Maximum Quiescent Supply Current			130	150	mA	
I_{CCA}	Maximum PLL Supply Current			15	20	mA	

1. DC levels will vary 1:1 with V_{CC}.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time		200		850	ps	20% to 80%
t_{pw1}	Output Duty Cycle		49		51	%	
t_{pw2}	SYNC Output Duty Cycle		0.95		1.05	%	PCLK Period
f_{ref}	Input Reference Frequency	Xtal FREF	10 Note 2		20 Note 2	MHz	
t_{os}	Output-to-Output Skew	Qa, Qb Qa (–) to SYNC (+)			100 300	ps	
f_{VCO}	PLL VCO Lock Range		200 400		440 750	MHz	VCO_SEL = 1 VCO_SEL = 0
f_{max}	Maximum Output Frequency	Qa (÷2) Qa,Qb (÷4) Qb (÷6) Qb (÷10)			375 187.5 125 75	MHz	Note 1
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)			±25	±50	ps	Note 3
t_{lock}	Maximum PLL Lock Time				10	ms	

1. At 400MHz the output swing will be less than the nominal value.
2. ECLK and XTAL input reference limited by the feedback divide and the guaranteed VCO lock range.
3. Guaranteed by characterization.

APPLICATIONS INFORMATION

Using the On–Board Crystal Oscillator

The MPC992 features an on–board crystal oscillator to allow for seed clock generation as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC992 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design, for optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC992 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically

a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Figure 2 shows an optional series capacitor in the crystal oscillator interface. The on–board oscillator introduces a small phase shift in the overall loop which causes the oscillator to operate at a frequency slightly slower than the specified crystal. The series capacitor is used to compensate the loop and allow the oscillator to function at the specified crystal frequency. If a 100ppm type error is not important, the capacitor can be left off the PCB. For more detailed information, order Motorola Application Note AN1579/D.

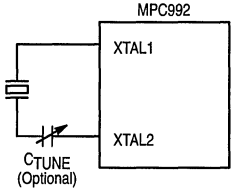


Figure 2. Recommended Crystal Interface

Table 1. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150ppm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω max
Correlation Drive Level	100µW
Aging	5ppm/Yr (First 3 Years)

Power Supply Filtering

The MPC992 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC992 provides separate power supplies for the digital circuitry (V_{CCI}) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC992.

Figure 5 illustrates a typical power supply filter scheme. The MPC992 is most susceptible to noise with spectral content in the 10kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC992. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 5 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

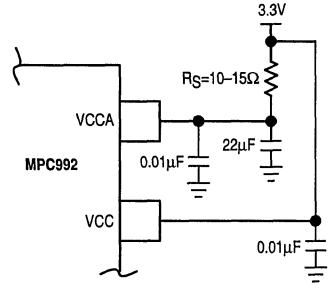


Figure 3. Power Supply Filter

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000µH choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the VCCA pin a low DC resistance inductor is required (less than 15Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MPC992 provides sub–nanosecond output edge rates and thus a good power supply bypassing scheme is a must. The important aspect of the layout for the MPC992 is low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC992 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the

capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

No active signal lines should pass below the crystal interface to the MPC992. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on–board oscillator. In addition, the crystal interface circuitry will be adversely affected by activity on the PECL_CLK inputs. Therefore, it is recommended that the PECL input signals be static when the crystal oscillator circuitry is being used.

Although the MPC992 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Clock Generation Circuits

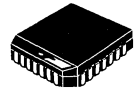
High Frequency Clock Generator

MC12429

HIGH FREQUENCY PLL CLOCK GENERATOR

The MC12429 is a general purpose synthesized clock source targeting applications that require both serial and parallel interfaces. Its internal VCO will operate over a range of frequencies from 400 to 800MHz. The differential PECL output can be configured to be the VCO frequency divided by 2, 4, 8 or 16. With the output configured to divide the VCO frequency by 2, and with a 16.000MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1MHz steps. The PLL loop filter is fully integrated so that no external components are required.

- 25 to 400MHz Differential PECL Outputs
- ±25ps Peak–to–Peak Output Jitter
- Fully Integrated Phase–Locked Loop
- Minimal Frequency Over–Shoot
- Synthesized Architecture
- Serial 3–Wire Interface
- Parallel Interface for Power–Up
- Quartz Crystal Interface
- 28–Lead PLCC Package
- Operates from 3.3V or 5.0V Power Supply



FN SUFFIX
28–LEAD PLCC PACKAGE
CASE 776–02

Functional Description

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 8 before being sent to the phase detector. With a 16MHz crystal, this provides a reference frequency of 2MHz. Although this data sheet illustrates functionality only for a 16MHz crystal, any crystal in the 10–25MHz range can be used.

The VCO within the PLL operates over a range of 400 to 800MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

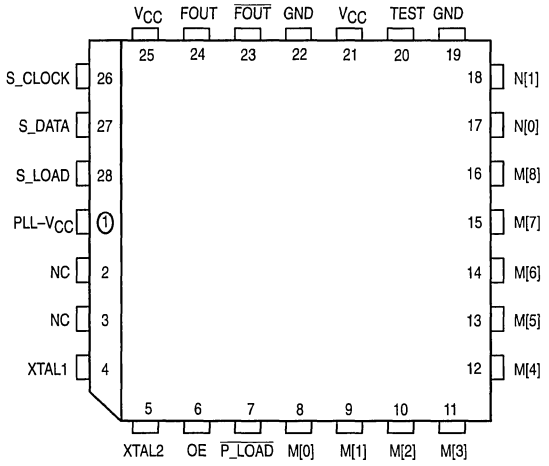
The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider (N divider) is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (2, 4, 8, or 16). This divider extends performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated in 50Ω to V_{CC} – 2.0. The positive reference for the output driver and the internal logic is separated from the power supply for the phase–locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. On the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH–to–LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.



N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	16

Figure 1. 28–Lead (Top View)

PIN DESCRIPTIONS

Pin Name	Function
Inputs	
XTAL1, XTAL2	These pins form an oscillator when connected to an external series–resonant crystal.
S_LOAD (Int. Pulldown)	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH–to–LOW transition of S_LOAD for proper operation.
S_DATA (Int. Pulldown)	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK (Int. Pulldown)	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
$\overline{\text{P\_LOAD}}$ (Int. Pullup)	This pin loads the configuration latches with the contents of the parallel inputs .The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation.
M[8:0] (Int. Pullup)	These pins are used to configure the PLL loop divider. They are sampled on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$. M[8] is the MSB, M[0] is the LSB.
N[1:0] (Int. Pullup)	These pins are used to configure the output divider modulus. They are sampled on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$.
OE (Int. Pullup)	Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation on the F_{OUT} output.
Outputs	
F_{OUT}, $\overline{F_{OUT}}$	These differential positive–referenced ECL signals (PECL) are the output of the synthesizer.
TEST	The function of this output is determined by the serial configuration bits T[2:0].
Power	
V_{CC}	This is the positive supply for the internal logic and the output buffer of the chip, and is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}). Current drain through $V_{CC} \approx$ 85mA.
PLL_V_{CC}	This is the positive supply for the PLL, and should be as noise–free as possible for low–jitter operation. This supply is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}). Current drain through PLL_$V_{CC} \approx$ 15mA.
GND	These pins are the negative supply for the chip and are normally all connected to ground.

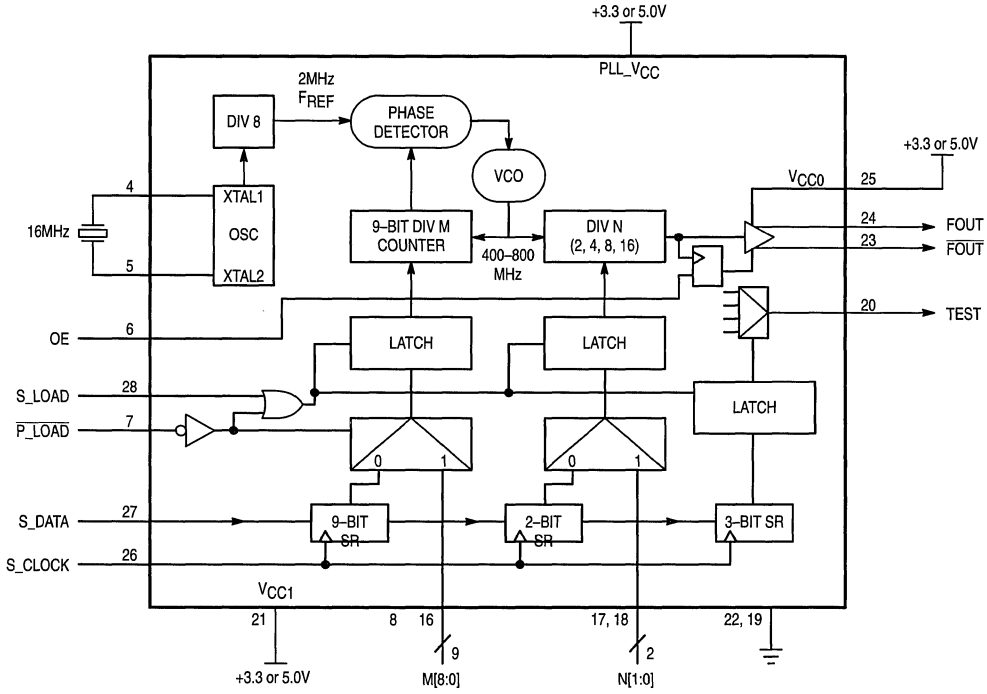


Figure 2. MC12429 Block Diagram

PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = (F_{XTAL} \div 8) \times M \div N \quad (1)$$

Where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$ for a 16MHz input reference.

Assuming that a 16MHz reference frequency is used the above equation reduces to:

$$FOUT = 2 \times M \div N$$

Substituting the four values for N (2, 4, 8, 16) yields:

FOUT = M, FOUT = M ÷ 2,
FOUT = M ÷ 4 and FOUT = M ÷ 8
for 200 < M < 400

The user can identify the proper M and N values for the desired frequency from the above equations. The four output frequency ranges established by N are 200 – 400MHz, 100 – 200MHz, 50 – 100MHz and 25 – 50MHz respectively. From these ranges the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example if an output frequency of 131MHz was desired the following steps would be taken to identify the appropriate M and N values. 131MHz falls within the frequency range set by an N value of 4 so N [1:0] = 01. For N = 4 FOUT = M ÷ 2 and M = 2 x FOUT. Therefore M = 131 x 2 = 262, so M[8:0] = 100000110. Following this same procedure a user can generate any whole frequency desired between 25 and 400MHz. Note that for N > 2 fractional values of FOUT can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies acheivable) will be equal to FXTAL ÷ 8 ÷ N.

For input reference frequencies other than 16MHz the set of appropriate equations can be deduced from equation 1. For computer applications another useful frequency base would be 16.666MHz. From this reference one can generate a family of output frequencies at multiples of the 33.333MHz PCI clock. As an example to generate a 133.333MHz clock

from a 16.666MHz reference the following M and N values would be used:

$$FOUT = 16.666 \div 8 \times M \div N = 2.083333 \times M \div N$$

$$\text{Let } N = 4, \quad M = 133.3333 \div 2.083333 \times 4 = 256$$

The value for M falls within the constraints set for PLL stability, therefore N[1:0] = 01 and M[8:0} = 10000000. If the value for M fell outside of the valid range a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{\text{P\_LOAD}}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{\text{P\_LOAD}}$ signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the $\overline{\text{P\_LOAD}}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data streeam on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 3 illustrates the timing diagram for both a parallel and a serial load of the MC12429 synthesizer.

M[8:0] and N[1:0] are normally specified once at power–up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine–tune the clock as the ability to control the serial interface becomes available. To minimize transients in the frequency domain, the output should be varied in the smallest step size possible. The bandwidth of the PLL is such that frequency stepping in 1MHz steps at the maximum S_CLOCK frequency or less will cause smooth, controlled slewing of the output frequency.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the CMOS output may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1 and T0 control bits are preset to '000' when $\overline{\text{P\_LOAD}}$ is LOW so that the PECL FOUT outputs are as jitter–free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12429 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MC12429 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 4 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 250MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 125MHz as the minimum divide ratio of the N counter is 2. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

T2	T1	T0	**TEST** (Pin 20)
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	FREF
0	1	1	M COUNTER OUT
1	0	0	FOUT
1	0	1	LOW
1	1	0	PLL BYPASS
1	1	1	FOUT/4

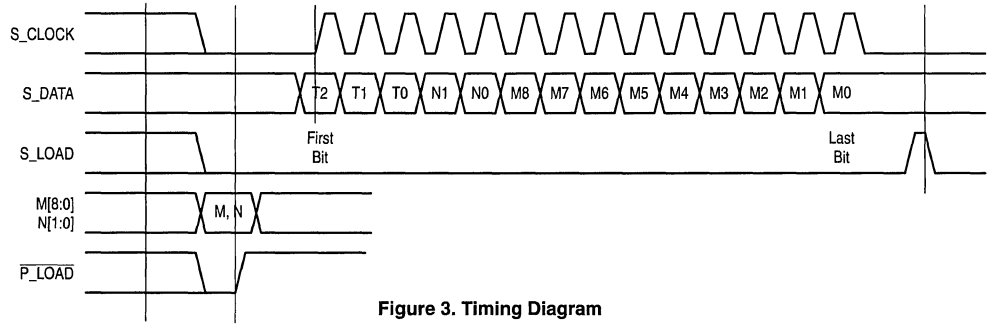
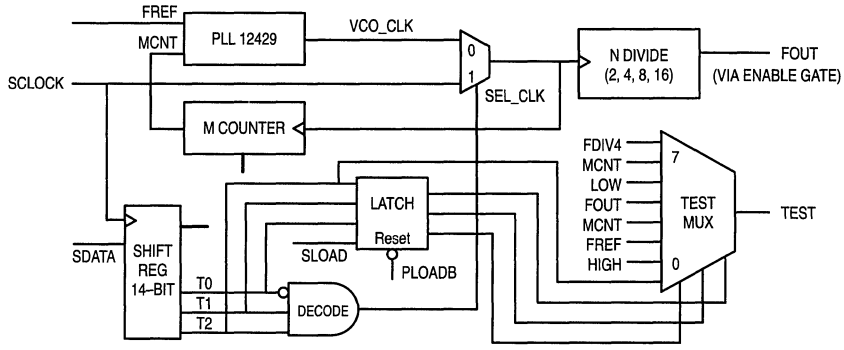


Figure 3. Timing Diagram



- T2=T1=1, T0=0: Test Mode
- SCLOCK is selected, MCNT is on TEST output, SCLOCK DIVIDE BY N is on FOUT pin

PLOADB acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

Figure 4. Serial Test Clock Block Diagram

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V to 5.0V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage		2.0			V	V_{CC} = 3.3 to 5.0V
V_{IL}	Input LOW Voltage				0.8	V	V_{CC} = 3.3 to 5.0V
I_{IN}	Input Current				1.0	mA	
V_{OH}	Output HIGH Voltage	TEST	2.5			V	I_{OH} = –0.8mA
V_{OL}	Output LOW Voltage	TEST			0.4	V	I_{OL} = 0.8mA
V_{OH}	Output HIGH Voltage	FOUT $\overline{FOUT}$	2.17		2.50	V	V_{CC0} = 3.3V (Notes 1., 2.)
V_{OL}	Output LOW Voltage	FOUT $\overline{FOUT}$	1.41		1.76	V	V_{CC0} = 3.3V (Notes 1., 2.)
I_{CC}	Power Supply Current	V_{CC} PLL_V_{CC}		85 15	100 20	mA	

1. Output levels will vary 1:1 with V_{CC0} variation.
2. 50Ω to V_{CC} – 2.0V pulldown.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V to 5.0V ±5%)

Symbol	Characteristic		Min	Max	Unit	Condition
F_{MAXI}	Maximum Input Frequency	S_CLOCK Xtal Oscillator	 10	10 20	MHz	Note 3.
F_{MAXO}	Maximum Output Frequency	VCO (Internal) FOUT	400 25	800 400	MHz	Note 4.
t_{LOCK}	Maximum PLL Lock Time			10	ms	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)			±25	ps	Note 4., See Applications Section
t_s	Setup Time	S_DATA to S_CLOCK S_CLOCK to $\overline{S\_LOAD}$ M, N to $\overline{P\_LOAD}$	20 20 20		ns	
t_h	Hold Time	S_DATA to S_CLOCK M, N to $\overline{P\_LOAD}$	20 20		ns	
tpw_{MIN}	Minimum Pulse Width	$\overline{S\_LOAD}$ $\overline{P\_LOAD}$	50 50		ns	Note 4.
t_r, t_f	Output Rise/Fall	FOUT	300	800	ps	20%–80%, Note 4.

3. 10MHz is the maximum frequency to load the feedback devide registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.
4. 50Ω to V_{CC} – 2.0V pulldown.

APPLICATIONS INFORMATION

Using the On–Board Crystal Oscillator

The MC12429 features a fully integrated on–board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MC12429 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the xtal terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1KΩ.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MC12429 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 1 below specifies the performance requirements of the crystals to be used with the MC12429.

Table 6. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MC12429 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12429 provides separate power supplies for the digital ciruitry (V_{CC}) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MC12429.

Figure 5 illustrates a typical power supply filter scheme. The MC12429 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_VCC pin of the MC12429. From the data sheet the I_{PLL_VCC} current (the current sourced through the PLL_VCC pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 5 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

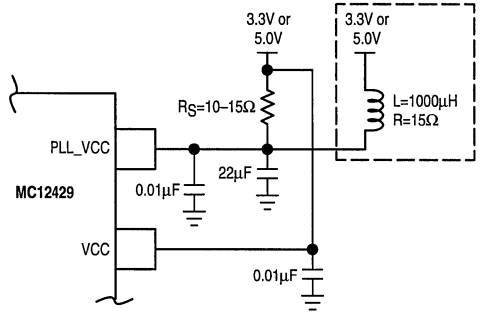


Figure 5. Power Supply Filter

A higher level of attenuation can be acheived by replacing the resistor with an appropriate valued inductor. Figure 5 shows a 1000µH choke, this value choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin a low DC resistance inductor is required (less than 15Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12429 provides sub–nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representaive board layout for the MC12429. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12429 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

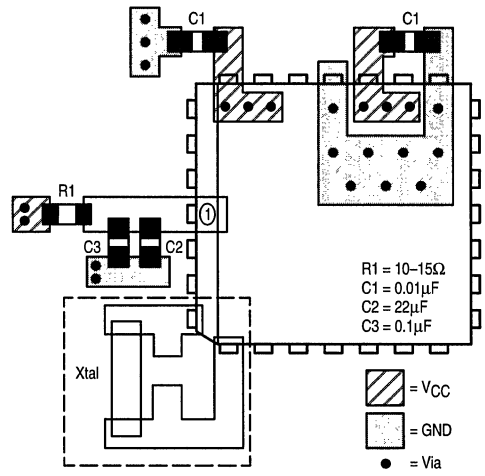


Figure 6. PCB Board Layout for MC12429

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on–board oscillator. Note the provisions for placing a resistor across the crystal oscillator terminals as discussed in the crystal oscillator section of this data sheet.

Although the MC12429 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may

be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Jitter Performance of the MC12429

The MC12429 exhibits long term and cycle–to–cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

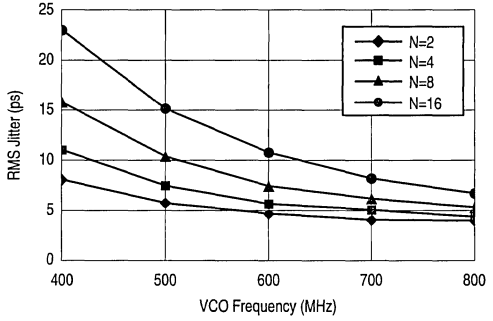


Figure 7. RMS PLL Jitter versus VCO Frequency

Figure 7 illustrates the RMS jitter performance of the MC12429 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data. In addition the data represents long term period jitter, the cycle–to–cycle jitter could not be measured to the level of accuracy required with available test equipment but certainly will be smaller than the long term period jitter.

The most commonly specified jitter parameter is cycle–to–cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MC12429. As a result different methods are used which approximate cycle–to–cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. The oscilloscope cannot collect adjacent pulses, rather it collects pulses from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce period jitter values somewhat larger than if consecutive cycles (cycle–to–cycle jitter) were measured. All of the jitter data reported on the MC12429 was collected in this manner.

Figure 8 shows the jitter as a function of the output frequency. For the 12429 this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ±25ps peak–to–peak long term period jitter. The graph shows that for output frequencies from 87.5 to 400MHz the jitter falls within the ±25ps peak–to–peak specification. The general trend is that as the output frequency is decreased the output edge jitter will increase.

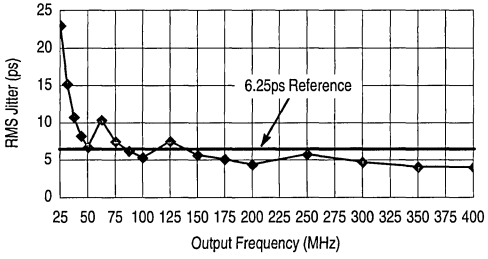


Figure 8. RMS Jitter versus Output Frequency

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

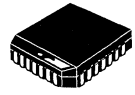
High Frequency Clock Generator

MC12430

HIGH FREQUENCY PLL CLOCK GENERATOR

The MC12430 is a general purpose synthesized clock source targeting applications that require both serial and parallel interfaces. Its internal VCO will operate over a range of frequencies from 400 to 800MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4 or 8. With the output configured to divide the VCO frequency by 2, and with a 16.000MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1MHz steps. The PLL loop filter is fully integrated so that no external components are required.

- 50 to 800MHz Differential PECL Outputs
- ±25ps Peak–to–Peak Output Jitter
- Fully Integrated Phase–Locked Loop
- Minimal Frequency Over–Shoot
- Synthesized Architecture
- Serial 3–Wire Interface
- Parallel Interface for Power–Up
- Quartz Crystal Interface
- 28–Lead PLCC Package
- Operates from 3.3V or 5.0V Power Supply



FN SUFFIX
28–LEAD PLCC PACKAGE
CASE 776–02

FA SUFFIX
32–LEAD TQFP PACKAGE
CASE 873A–02

Functional Description

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 8 before being sent to the phase detector. With a 16MHz crystal, this provides a reference frequency of 2MHz. Although this data sheet illustrates functionality only for a 16MHz crystal, any crystal in the 10–20MHz range can be used.

The VCO within the PLL operates over a range of 400 to 800MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

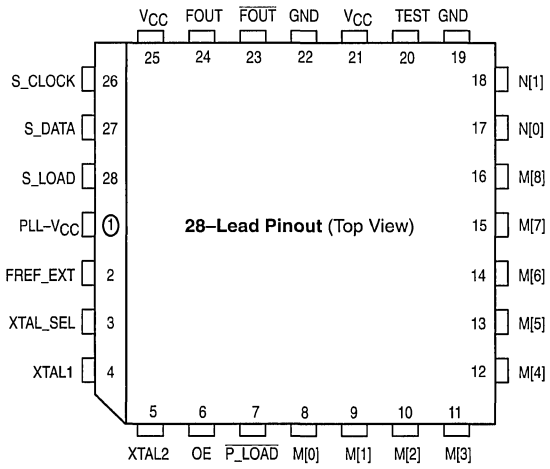
The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider (N divider) is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4 or 8). This divider extends performance of the part while providing a 50% duty cycle.

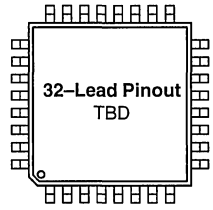
The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated in 50Ω to V_{CC} – 2.0. The positive reference for the output driver and the internal logic is separated from the power supply for the phase–locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. On the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH–to–LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.





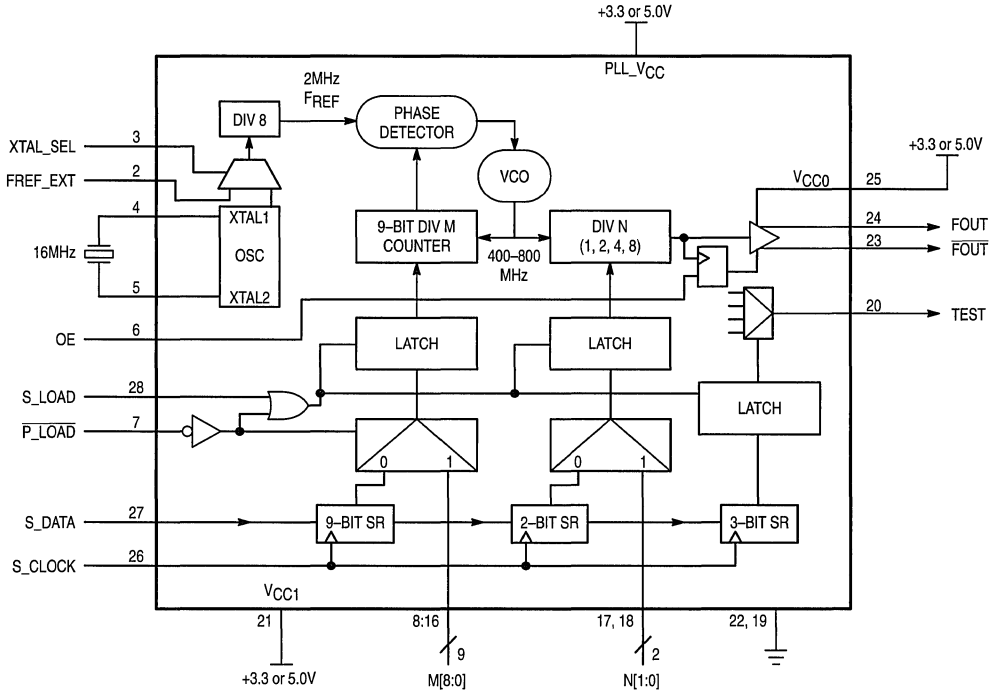
N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	1

Input	0	1
XTAL_SEL	FREF_EXT	XTAL
OE	Disabled	Enabled

PIN DESCRIPTIONS

Pin Name	Function
Inputs	
XTAL1, XTAL2	These pins form an oscillator when connected to an external series–resonant crystal.
S_LOAD (Int. Pulldown)	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH–to–LOW transition of S_LOAD for proper operation.
S_DATA (Int. Pulldown)	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK (Int. Pulldown)	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
$\overline{\text{P\_LOAD}}$ (Int. Pullup)	This pin loads the configuration latches with the contents of the parallel inputs .The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation.
M[8:0] (Int. Pullup)	These pins are used to configure the PLL loop divider. They are sampled on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$. M[8] is the MSB, M[0] is the LSB.
N[1:0] (Int. Pullup)	These pins are used to configure the output divider modulus. They are sampled on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$.
OE (Int. Pullup)	Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation on the F_{OUT} output.
Outputs	
F_{OUT}, $\overline{F_{OUT}}$	These differential positive–referenced ECL signals (PECL) are the output of the synthesizer.
TEST	The function of this output is determined by the serial configuration bits T[2:0]. The output is single–ended ECL.
Power	
V_{CC}	This is the positive supply for the internal logic and the output buffer of the chip, and is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}). Current drain through $V_{CC} \approx$ 85mA.
PLL_V_{CC}	This is the positive supply for the PLL, and should be as noise–free as possible for low–jitter operation. This supply is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}). Current drain through PLL_$V_{CC} \approx$ 15mA.
GND	These pins are the negative supply for the chip and are normally all connected to ground.
Other	
FREF_EXT (Int. Pulldown)	LVCMOS/CMOS input which can be used as the PLL reference.
XTAL_SEL (Int. Pullup)	LVCMOS/CMOS input that selects between the crystal and the FREF_EXT source for the PLL reference signal. A HIGH selects the crystal input.

MC12430 BLOCK DIAGRAM



PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = (F_{XTAL} \div 8) \times M \div N \qquad (1)$$

Where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$ for any input reference.

Assuming that a 16MHz reference frequency is used the above equation reduces to:

$$FOUT = 2 \times M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

FOUT = 2M, FOUT = M,
FOUT = M ÷ 2 and FOUT = M ÷ 4
for 200 < M < 400

The user can identify the proper M and N values for the desired frequency from the above equations. The four output frequency ranges established by N are 400–800MHz, 200–400MHz, 100–200MHz and 50–100MHz respectively. From these ranges the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example if an output frequency of 131MHz was desired the following steps would be taken to identify the appropriate M and N values. 131MHz falls within the frequency range set by an N value of 4 so N [1:0] = 01. For N = 4 FOUT = M ÷ 2 and M = 2 x FOUT. Therefore M = 131 x 2 = 262, so M[8:0] = 100000110. Following this same procedure a user can generate any whole frequency desired between 50 and 800MHz. Note that for N > 2 fractional values of FOUT can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies acheivable) will be equal to FXTAL ÷ 8 ÷ N.

For input reference frequencies other than 16MHz the set of appropriate equations can be deduced from equation 1. For computer applications another useful frequency base would be 16.666MHz. From this reference one can generate a family of output frequencies at multiples of the 33.333MHz PCI clock. As an example to generate a 133.333MHz clock

from a 16.666MHz reference the following M and N values would be used:

$$FOUT = 16.666 \div 8 \times M \div N = 2.083333 \times M \div N$$

$$\text{Let } N = 4, \quad M = 133.3333 \div 2.083333 \times 4 = 256$$

The value for M falls within the constraints set for PLL stability, therefore N[1:0] = 01 and M[8:0} = 10000000. If the value for M fell outside of the valid range a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{\text{P\_LOAD}}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{\text{P\_LOAD}}$ signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the $\overline{\text{P\_LOAD}}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data streeam on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 3 illustrates the timing diagram for both a parallel and a serial load of the MC12430 synthesizer.

M[8:0] and N[1:0] are normally specified once at power–up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine–tune the clock as the ability to control the serial interface becomes available. To minimize transients in the frequency domain, the output should be varied in the smallest step size possible. The bandwidth of the PLL is such that frequency stepping in 1MHz steps at the maximum S_CLOCK frequency or less will cause smooth, controlled slewing of the output frequency.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. The T2, T1 and T0 control bits are preset to '000' when $\overline{\text{P\_LOAD}}$ is LOW so that the PECL FOUT outputs are as jitter–free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12430 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MC12430 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 4 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 250MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 250MHz as the minimum divide ratio of the N counter is 1. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

T2	T1	T0	**TEST** (Pin 20)
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	FREF
0	1	1	M COUNTER OUT
1	0	0	FOUT
1	0	1	LOW
1	1	0	PLL BYPASS
1	1	1	FOUT/4

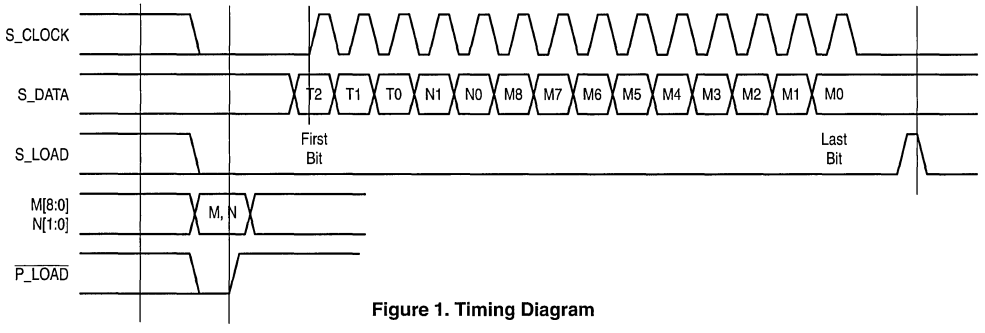
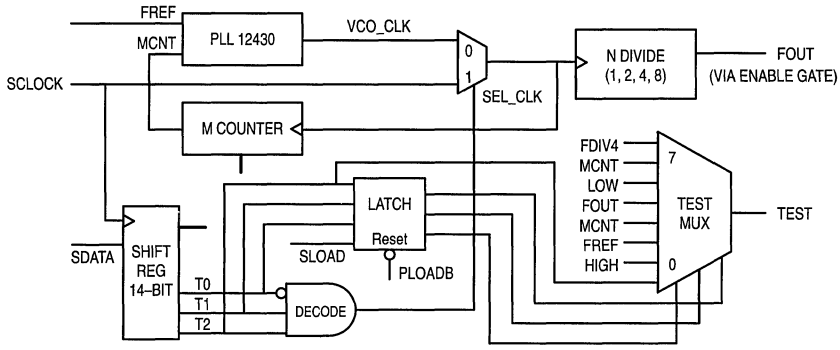


Figure 1. Timing Diagram



- T2=T1=1, T0=0: Test Mode
- SCLOCK is selected, MCNT is on TEST output, SCLOCK DIVIDE BY N is on FOUT pin

PLOADB acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

Figure 2. Serial Test Clock Block Diagram

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V to 5.0V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0			V	V_{CC} = 3.3 to 5.0V
V_{IL}	Input LOW Voltage			0.8	V	V_{CC} = 3.3 to 5.0V
I_{IN}	Input Current			1.0	mA	
V_{OH}	Output HIGH Voltage	2.17		2.50	V	V_{CC0} = 3.3V[1]
V_{OL}	Output LOW Voltage	1.41		1.76	V	V_{CC0} = 3.3V[1]
I_{CC}	Power Supply Current V_{CC} PLL_V_{CC}		85 15	100 20	mA	

1. Output levels will vary 1:1 with V_{CC0} variation.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V to 5.0V ±5%)

Symbol	Characteristic		Min	Max	Unit	Condition
F_{MAXI}	Maximum Input Frequency	S_CLOCK Xtal Oscillator FREF_EXT	 10 10	10 20 Note 3.	MHz	Note 2.
F_{MAXO}	Maximum Output Frequency	VCO (Internal) FOUT	400 50	800 800	MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak) Note 4.			±25 ±65	ps	N = 2, 4, 8; Note 5. N = 1; Note 5.
t_s	Setup Time	S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20 20 20		ns	
t_h	Hold Time	S_DATA to S_CLOCK M, N to P_LOAD	20 20		ns	
tpw_{MIN}	Minimum Pulse Width	S_LOAD P_LOAD	50 50		ns	
t_r, t_f	Output Rise/Fall	FOUT	300	800	ps	20%–80%

2. 10MHz is the maximum frequency to load the feedback devide registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.
3. Maximum frequency on FREF_EXT is a function of the internal M counter limitations. The phase detector can handle up to 100MHz on the input, but the M counter must remain in the valid range of 200 ≤ M ≤ 400. See the programming section on page 334 of this data sheet fore more details.
4. See Applications Information below for additional information.
5. 50Ω to V_{CC} – 2.0V pull–down.

APPLICATIONS INFORMATION

Using the On–Board Crystal Oscillator

The MC12430 features a fully integrated on–board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MC12430 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MC12430 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 1 below specifies the performance requirements of the crystals to be used with the MC12430.

Table 7. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MC12430 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12430 provides separate power supplies for the digital ciruitry (V_{CC}) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MC12430.

Figure 5 illustrates a typical power supply filter scheme. The MC12430 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_VCC pin of the MC12430. From the data sheet the I_{PLL_VCC} current (the current sourced through the PLL_VCC pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 5 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

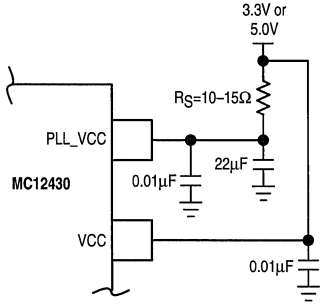


Figure 3. Power Supply Filter

A higher level of attenuation can be acheived by replacing the resistor with an appropriate valued inductor. A 1000µH choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin a low DC resistance inductor is required (less than 15Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12430 provides sub–nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representaive board layout for the MC12430. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12430 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

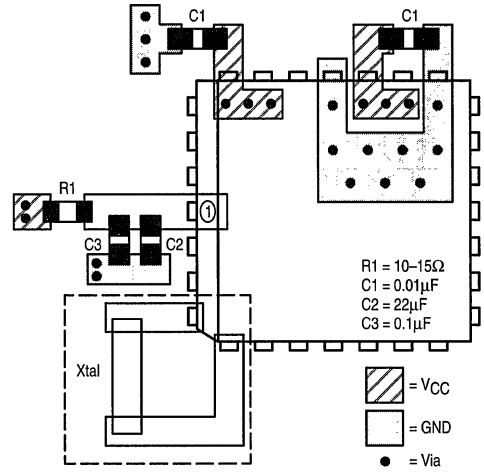


Figure 4. PCB Board Layout for MC12430

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on–board oscillator.

Although the MC12430 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section

should be adequate to eliminate power supply noise related problems in most designs.

Jitter Performance of the MC12430

The MC12430 exhibits long term and cycle–to–cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

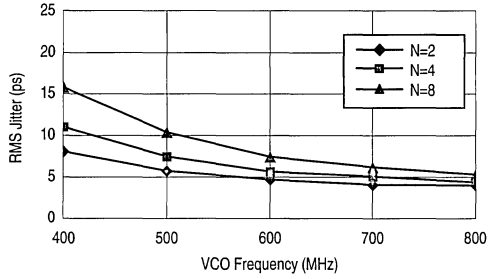


Figure 5. RMS PLL Jitter versus VCO Frequency

Figure 5 illustrates the RMS jitter performance of the MC12430 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data. In addition the data represents long term period jitter, the cycle–to–cycle jitter could not be measured to the level of accuracy required with available test equipment but certainly will be smaller than the long term period jitter.

The most commonly specified jitter parameter is cycle–to–cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MC12430. As a result different methods are used which approximate cycle–to–cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. The oscilloscope cannot collect adjacent pulses, rather it collects pulses from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce period jitter values somewhat larger than if consecutive cycles (cycle–to–cycle jitter) were measured. All of the jitter data reported on the MC12430 was collected in this manner.

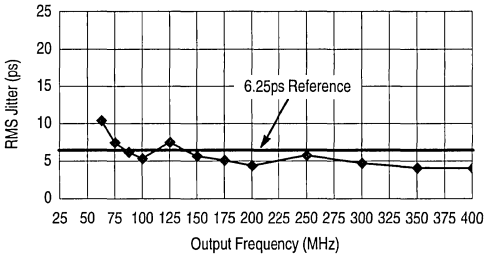


Figure 6. RMS Jitter versus Output Frequency

Figure 6 shows the jitter as a function of the output frequency. For the 12430 this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ±25ps peak–to–peak long term period jitter. The graph shows that for output frequencies from 87.5 to 400MHz the jitter falls within the ±25ps peak–to–peak specification. The general trend is that as the output frequency is decreased the output edge jitter will increase.

The jitter data from Figure 5 and Figure 6 do not include the performance of the 12430 when the output is in the divide by 1 mode. In divide by one mode the output signal is a digitally doubled version of the VCO output. The period of the outputs of the digital doubler is dependent on the duty cycle of the VCO output. Since the VCO output duty cycle cannot be guaranteed to be always 50% the resulting 12430 output in divide by one mode will be bimodal at times. Since a bimodal distribution cannot be acurately represented with an rms value, peak–to–peak values of jitter for the divide by one mode are presented.

Figure 9 shows the peak–to–peak jitter of the 12430 output in divide by one mode as a function of output frequency. Notice that as with the other modes the jitter improves with increasing frequency. The ±65ps shown in the data sheet table represents a conservative value of jitter, especially for the higher vco, and thus output frequencies.

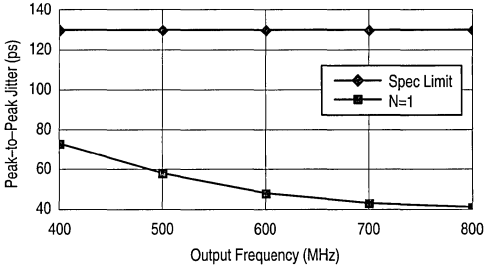


Figure 7. Peak–to–Peak Jitter versus Output Frequency

The jitter data presented should provide users with enough information to determine the effect on their overall

timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

Output Voltage Swing vs Frequency

In the divide by one mode the output rise and fall times will limit the peak to peak output voltage swing. For a 400MHz output the peak to peak swing of the 12430 output will be approximately 700mV. This swing will gradually degrade as the output frequency increases, at 800MHz the output swing will be reduced to approximately 400mV. For a worst case analysis it would be safe to assume that the 12430 output will always generate at least a 400mV output swing. Note that most high speed ECL receivers require only a few hundred millivolt input swings for reliable operation. As a result the output generated by the 12430 will, under all conditions, be sufficient for clocking standard ECL devices. Note that if a larger swing is desired the 12430 could drive a single gate ECLinPS Lite amplifier like the MC100LVEL16. The LVEL16 will speed up the output edge rates and produce a full swing ECL output at 800MHz.

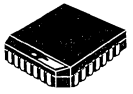
High Frequency Clock Generator

MC12439

HIGH FREQUENCY PLL CLOCK GENERATOR

The MC12439 is a general purpose synthesized clock source targeting applications that require both serial and parallel interfaces. Its internal VCO will operate over a range of frequencies from 400 to 800MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4, or 8. With the output configured to divide the VCO frequency by 1, and with a 16.66MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 16.66MHz steps.

- 50 to 800MHz Differential PECL Outputs
- ±25ps Typical Peak–to–Peak Output Jitter
- Minimal Frequency Over–Shoot
- Synthesized Architecture
- Serial 3–Wire Interface
- Parallel Interface for Power–Up
- Quartz Crystal Interface
- 28–Lead PLCC Package
- Operates from 3.3V or 5.0V Power Supply



FN SUFFIX
28–LEAD PLCC PACKAGE
CASE 776–02

Functional Description

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is sent directly to the phase detector. With a 16.66MHz crystal, this provides a reference frequency of 16.66MHz. Although this data sheet illustrates functionality only for a 16MHz and 16.66MHz crystal, any crystal in the 10–20MHz range can be used. In addition to the crystal, an LVCMOS input can also be used as the PLL reference. The reference is selected via the XTAL_SEL input pin.

The VCO within the PLL operates over a range of 400 to 800MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle.

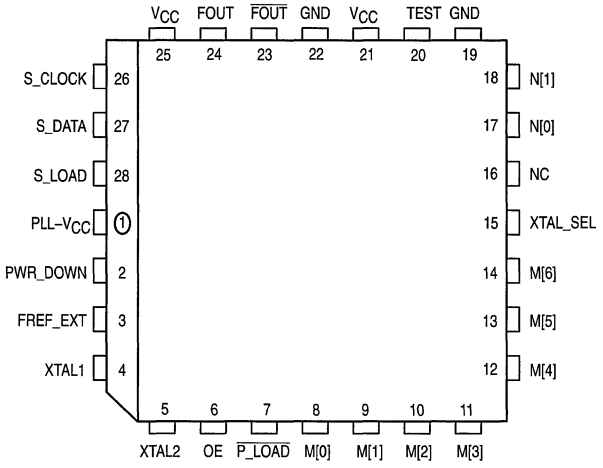
The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated in 50Ω to V_{CC} – 2.0.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. On the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH–to–LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

The PWR_DOWN pin, when asserted, will synchronously divide the FOUT by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de–assertion of the PWR_DOWN pin, the FOUT input will step back up to its programmed frequency in four discrete increments.



N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	1

Input	0	1
PWR_DOWN	FOUT	FOUT/16
XTAL_SEL	FREF_EXT	XTAL
OE	Disabled	Enabled

Figure 1. 28–Lead Pinout (Top View)

PIN DESCRIPTIONS

Pin Name	Type	Function
Inputs		
XTAL1, XTAL2	—	These pins form an oscillator when connected to an external series–resonant crystal.
S_LOAD	Int. Pulldown	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH–to–LOW transition of S_LOAD for proper operation.
S_DATA	Int. Pulldown	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK	Int. Pulldown	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
$\overline{\text{P\_LOAD}}$	Int. Pullup	This pin loads the configuration latches with the contents of the parallel inputs .The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation.
M[6:0]	Int. Pullup	These pins are used to configure the PLL loop divider. They are sampled on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$. M[6] is the MSB, M[0] is the LSB.
N[1:0]	Int. Pullup	These pins are used to configure the output divider modulus. They are sampled on the LOW–to–HIGH transition of $\overline{\text{P\_LOAD}}$.
OE	Int. Pullup	Active HIGH Output Enable.
Outputs		
FOUT, $\overline{\text{FOUT}}$	—	These differential positive–referenced ECL signals (PECL) are the output of the synthesizer.
TEST	—	The function of this output is determined by the serial configuration bits T[2:0].
Power		
V_{CC}	—	This is the positive supply for the chip, and is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}).
PLL_V_{CC}	—	This is the positive supply for the PLL, and should be as noise–free as possible for low–jitter operation. This supply is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}).
GND	—	These pins are the negative supply for the chip and are normally all connected to ground.
Other		
PWR_DOWN	Int. Pulldown	LVCMOS input that forces the FOUT output to synchronously reduce its frequency by a factor of 16.
FREF_EXT	Int. Pulldown	LVCMOS input which can be used as the PLL reference frequency.
XTAL_SEL	Int. Pullup	LVCMOS input that selects between the XTAL and FREF_EXT PLL reference inputs. A HIGH selects the XTAL input.

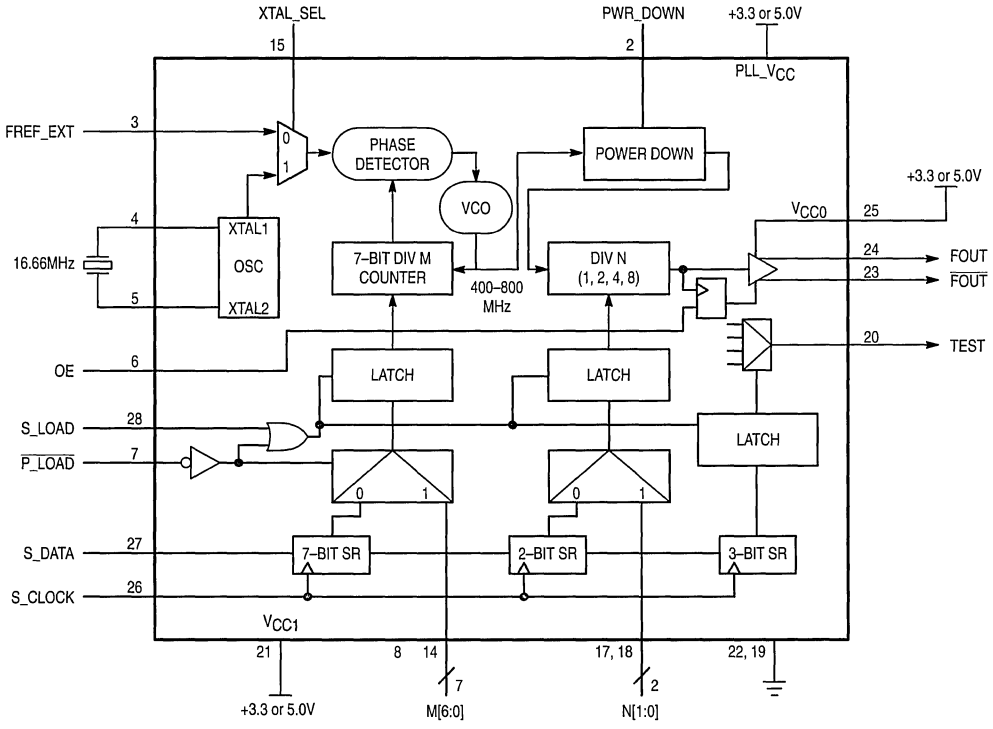


Figure 2. MC12439 Block Diagram

PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = F_{XTAL} \times M \div N \quad (1)$$

Where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $25 \leq M \leq 50$ for a 16MHz input reference.

For input references other than 16MHz, the valid M values can be calculated from the valid VCO range of 400–800MHz.

Assuming that a 16MHz reference frequency is used the above equation reduces to:

$$FOUT = 16 \times M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

FOUT = 16M, FOUT = 8M,
FOUT = 4M and FOUT = 2M
for 25 < M < 50

The user can identify the proper M and N values for the desired frequency from the above equations. The four output frequency ranges established by N are 400–800MHz, 200–400MHz, 100–200MHz and 50–100MHz respectively. From these ranges the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example if an output frequency of 384MHz was desired the following steps would be taken to identify the appropriate M and N values. 384MHz falls within the frequency range set by an N value of 2 so N [1:0] = 00. For N = 2 FOUT = 8M and M = FOUT ÷ 8. Therefore M = 384 ÷ 8 = 48, so M[8:0] = 0110000.

For input reference frequencies other than 16MHz the set of appropriate equations can be deduced from equation 1. For computer applications another useful frequency base would be 16.666MHz. From this reference one can generate a family of output frequencies at multiples of the 33.333MHz PCI clock. As an example to generate a 533.333MHz clock

from a 16.666MHz reference the following M and N values would be used:

FOUT = 16.666 x M ÷ N

Let N = 1, M = 533.333 ÷ 16.666 = 32

The value for M falls within the constraints set for PLL stability (400÷16.666 ≤ M ≤ 800÷16.666; 24 ≤ M ≤ 48), therefore N[1:0] = 11 and M[6:0} = 0100000. If the value for M fell outside of the valid range a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{\text{P\_LOAD}}$ signal such that a LOW to HIGH transition will latch the information present on the M[6:0] and N[1:0] inputs into the M and N counters. When the $\overline{\text{P\_LOAD}}$ signal is LOW the input latches will be transparent and any changes on the M[6:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the $\overline{\text{P\_LOAD}}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data streeam on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. NO TAG illustrates the timing diagram for both a parallel and a serial load of the MC12439 synthesizer.

M[6:0] and N[1:0] are normally specified once at power–up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine–tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the CMOS output may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1 and T0 control bits are preset to '000' when $\overline{\text{P\_LOAD}}$ is LOW so that the PECL FOUT outputs are as jitter–free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12439 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MC12439 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. NO TAG shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 250MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 250MHz as the minimum divide ratio of the N counter is 1. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

T2	T1	T0	**TEST** (Pin 20)
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	FREF
0	1	1	M COUNTER OUT
1	0	0	FOUT
1	0	1	LOW
1	1	0	PLL BYPASS
1	1	1	FOUT/4

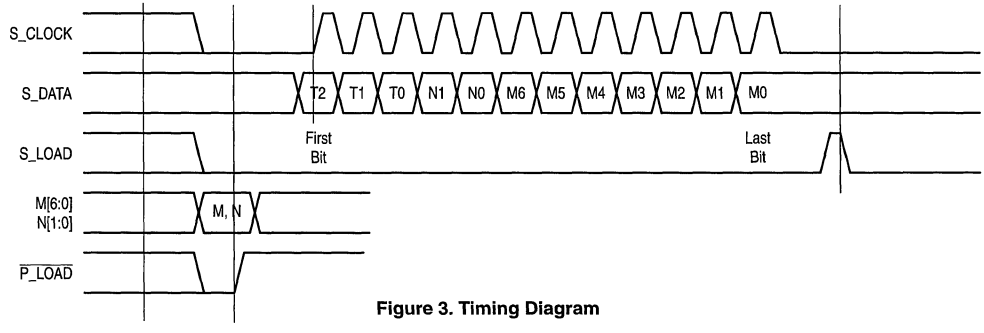
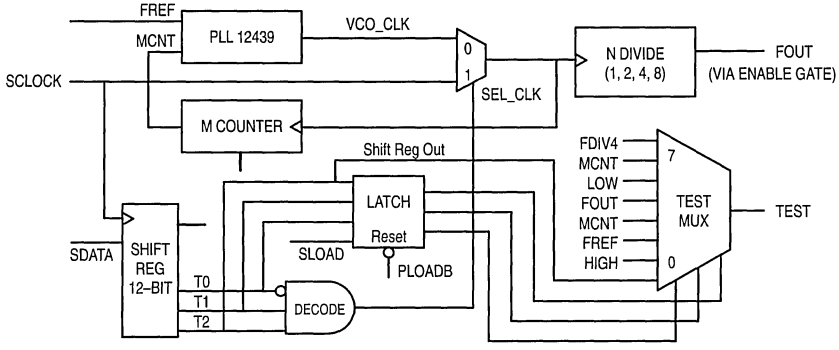


Figure 3. Timing Diagram



- T2=T1=1, T0=0: Test Mode
- SCLOCK is selected, MCNT is on TEST output, SCLOCK DIVIDE BY N is on FOUT pin

PLOADB acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

Figure 4. Serial Test Clock Block Diagram

DC CHARACTERISTICS (T_A = 0 to 70°C; V_{CC} = 3.3 to 5.0V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0			V	V_{CC} = 3.3 to 5.0V
V_{IL}	Input LOW Voltage			0.8	V	V_{CC} = 3.3 to 5.0V
I_{IN}	Input Current			1.0	mA	
I_{OH}	Output HIGH Current (Note 1.) (FOUT/$\overline{FOUT}$ Only)			50	mA	Continuous Current
V_{OH}	Output HIGH Voltage TEST	2.5			V	I_{OH} = –0.8mA, (Note 2.)
V_{OL}	Output LOW Voltage TEST			0.4	V	I_{OL} = 0.8mA, (Note 2.)
V_{OH}	Output HIGH Voltage FOUT / $\overline{FOUT}$	2.27		2.47	V	V_{CC} = 3.3V (Notes 3., 4.)
V_{OL}	Output LOW Voltage FOUT / $\overline{FOUT}$	1.49		1.68	V	V_{CC} = 3.3V (Notes 3., 4.)
I_{CC}	Power Supply Current V_{CC} / PLL_V_{CC}		90 / 15	110 / 20	mA	

1. Maximum I_{OH} spec implies the device can drive 25Ω impedance with the PECL outputs.
2. See Applications Information section for output level versus frequency information.
3. Output levels will vary 1:1 with V_{CC} variation.
4. 50Ω to V_{CC} – 2.0V pulldown.

AC CHARACTERISTICS (T_A = 0 to 70°C; V_{CC} = 3.3 to 5.0V ±5%)

Symbol	Characteristic		Min	Max	Unit	Condition
F_{MAXI}	Maximum Input Frequency	S_CLOCK Xtal Oscillator FREF_EXT	 10 10	10 20 Note 5.	MHz	
F_{MAXO}	Maximum Output Frequency	VCO (Internal) FOUT	400 50	900 800	MHz	
t_{LOCK}	Maximum PLL Lock Time		1	10	ms	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak) (Note 6.)			±25 ±65	ps	N = 2,4,8; Note 7. N = 1; Note 7.
t_s	Setup Time	S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to $\overline{P\_LOAD}$	20 20 20		ns	
t_h	Hold Time	S_DATA to S_CLOCK M, N to $\overline{P\_LOAD}$	20 20		ns	
tpw_{MIN}	Minimum Pulse Width	S_LOAD $\overline{P\_LOAD}$	50 50		ns	Note 7.
t_r, t_f	Output Rise/Fall Time		300	800	ps	Note 7.

5. Maximum frequency on FREF_EXT is a function of the internal M counter limitations. The phase detector can handle up to 100MHz on the input, but the M counter must remain in the valid range of 25 ≤ M ≤ 50. See the programming section in this data sheet for more details.
6. See Applications Information section for additional information.
7. 50Ω to V_{CC} – 2.0V pulldown.

APPLICATIONS INFORMATION

Using the On–Board Crystal Oscillator

The MC12439 features a fully integrated on–board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MC12439 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MC12439 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 1 below specifies the performance requirements of the crystals to be used with the MC12439.

Table 1. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MC12439 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12439 provides separate power supplies for the digital ciruitry (V_{CC}) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MC12439.

Figure 5 illustrates a typical power supply filter scheme. The MC12439 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_VCC pin of the MC12439. From the data sheet the I_{PLL_VCC} current (the current sourced through the PLL_VCC pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 5 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

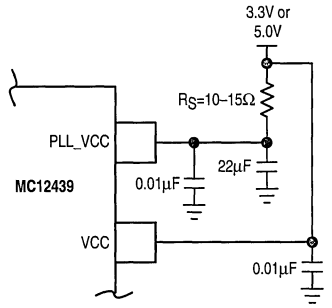


Figure 5. Power Supply Filter

A higher level of attenuation can be acheived by replacing the resistor with an appropriate valued inductor. A 1000μH choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin a low DC resistance inductor is required (less than 15Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12439 provides sub–nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representaive board layout for the MC12439. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12439 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

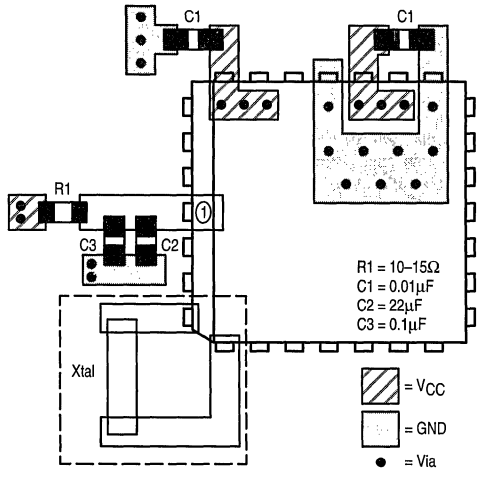


Figure 6. PCB Board Layout for MC12439

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on–board oscillator.

Although the MC12439 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Jitter Performance of the MC12439

The MC12439 exhibits long term and cycle–to–cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

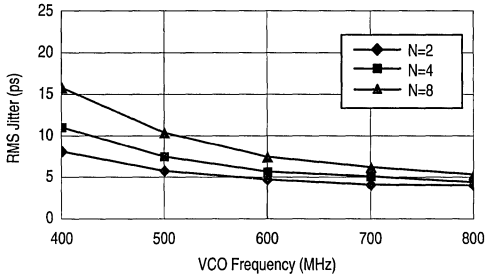


Figure 7. RMS PLL Jitter versus VCO Frequency

Figure 7 illustrates the RMS jitter performance of the MC12439 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data. In addition the data represents long term period jitter, the cycle–to–cycle jitter could not be measured to the level of accuracy required with available test equipment but certainly will be smaller than the long term period jitter.

The most commonly specified jitter parameter is cycle–to–cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MC12439. As a result different methods are used which approximate cycle–to–cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. The oscilloscope cannot collect adjacent pulses, rather it collects pulses from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce period jitter values somewhat larger than if consecutive cycles (cycle–to–cycle jitter) were measured. All of the jitter data reported on the MC12439 was collected in this manner.

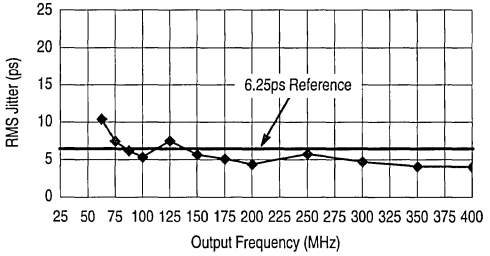


Figure 8. RMS Jitter versus Output Frequency

Figure 8 shows the jitter as a function of the output frequency. For the 12439 this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ±25ps peak–to–peak long term period jitter. The graph shows that for output frequencies from 87.5 to 400MHz the jitter falls within the ±25ps peak–to–peak specification. The general trend is that as the output frequency is decreased the output edge jitter will increase.

The jitter data from Figure 7 and Figure 8 do not include the performance of the 12439 when the output is in the divide by 1 mode. In divide by one mode the output signal is a digitally doubled version of the VCO output. The period of the outputs of the digital doubler is dependent on the duty cycle of the VCO output. Since the VCO output duty cycle cannot be guaranteed to be always 50% the resulting 12439 output in divide by one mode will be bimodal at times. Since a bimodal distribution cannot be acurately represented with an rms value, peak–to–peak values of jitter for the divide by one mode are presented.

Figure 9 shows the peak–to–peak jitter of the 12439 output in divide by one mode as a function of output frequency. Notice that as with the other modes the jitter improves with increasing frequency. The ±65ps shown in the data sheet table represents a conservative value of jitter, especially for the higher vco, and thus output frequencies.

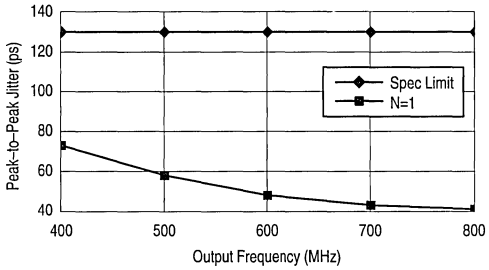


Figure 9. Peak–to–Peak Jitter versus Output Frequency

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

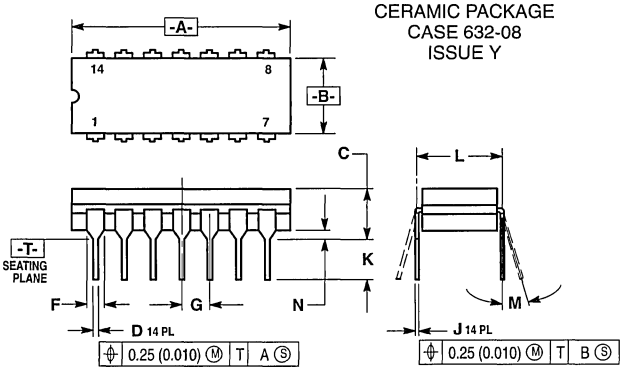
Output Voltage Swing vs Frequency

In the divide by one mode the output rise and fall times will limit the peak to peak output voltage swing. For a 400MHz output the peak to peak swing of the 12439 output will be approximately 700mV. This swing will gradually degrade as the output frequency increases, at 800MHz the output swing will be reduced to approximately 500mV. For a worst case analysis it would be safe to assume that the 12439 output will always generate at least a 400mV output swing. Note that most high speed ECL receivers require only a few hundred millivolt input swings for reliable operation. As a result the output generated by the 12439 will, under all conditions, be sufficient for clocking standard ECL devices. Note that if a larger swing is desired the 12439 could drive a single gate ECLinPS Lite amplifier like the MC100LVEL16. The LVEL16 will speed up the output edge rates and produce a full swing ECL output at 800MHz.

Case Outlines

Case Outlines

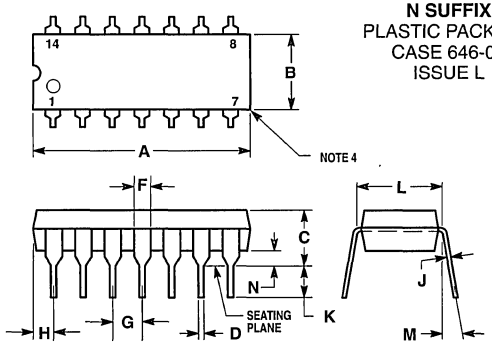
J SUFFIX
CERAMIC PACKAGE
CASE 632-08
ISSUE Y



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 632-01 THRU -07 OBSOLETE, NEW STANDARD 632-08.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.1	0.020	0.040

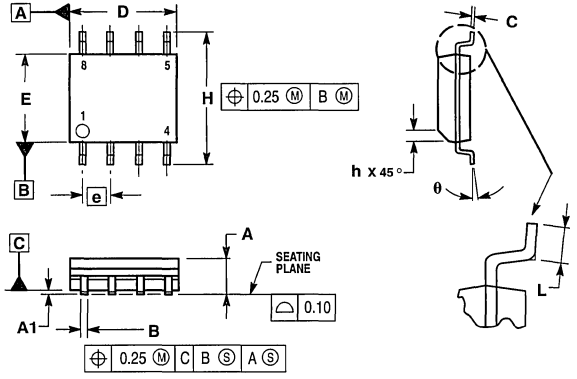
N SUFFIX
PLASTIC PACKAGE
CASE 646-06
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.
5. 646-05 OBSOLETE, NEW STANDARD 646-06.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

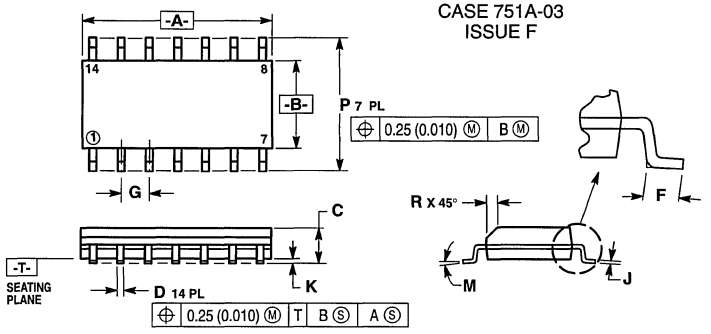
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

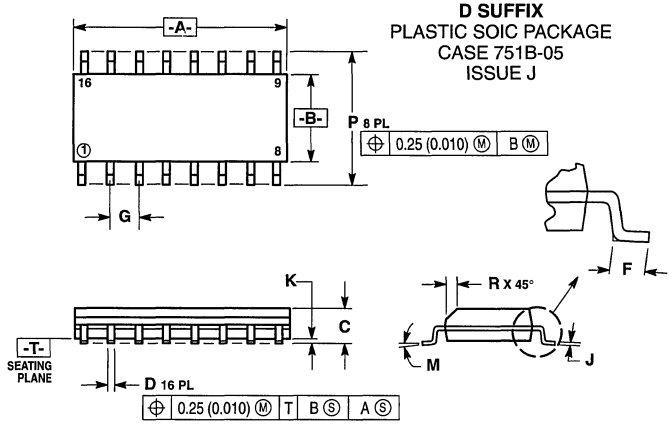
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A-03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

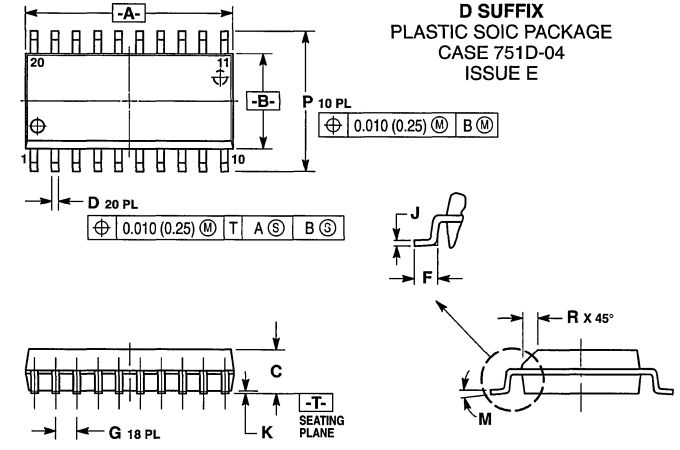
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

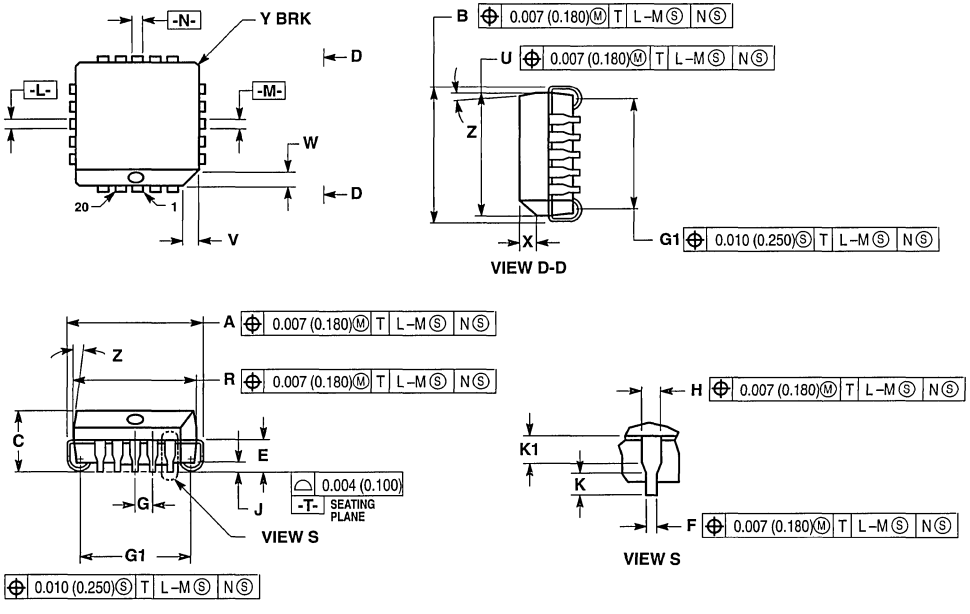
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

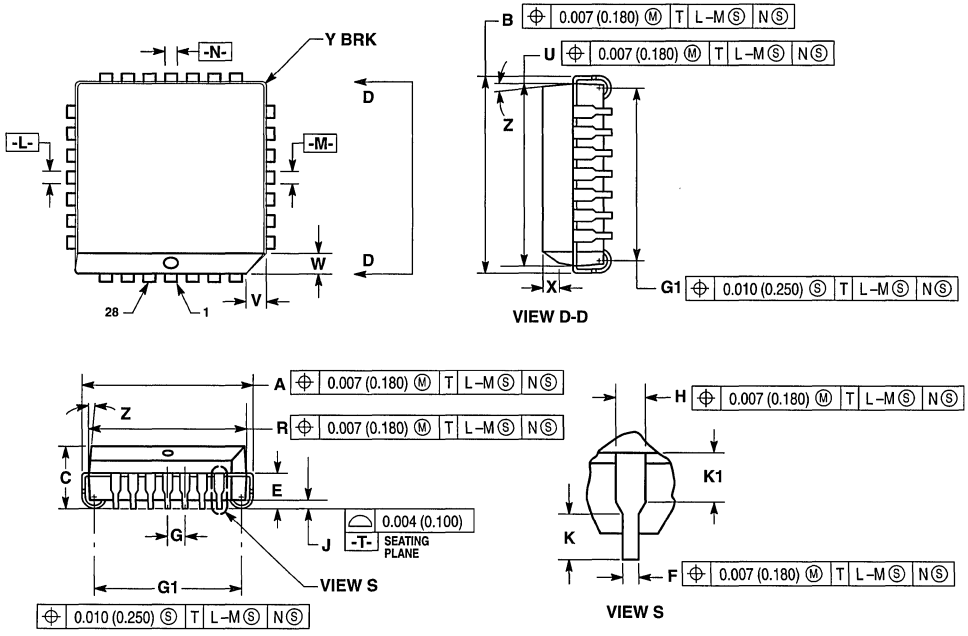
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

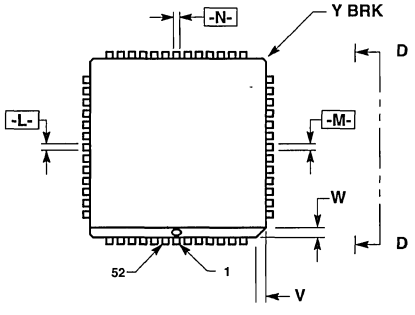
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE D

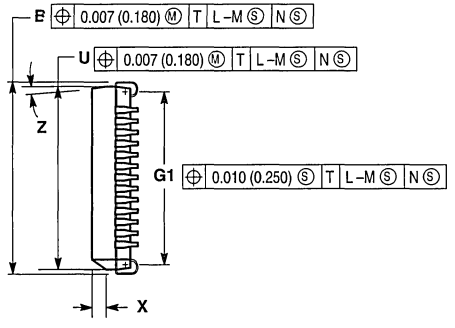


NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

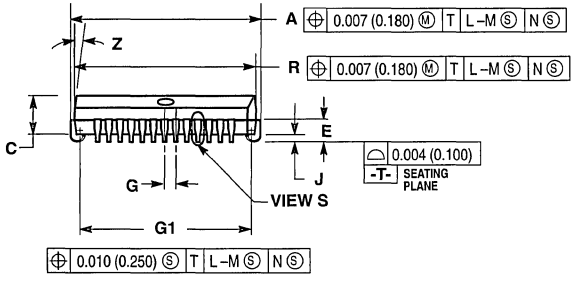
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

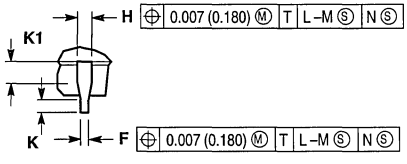
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 778-02
ISSUE C





VIEW D-D



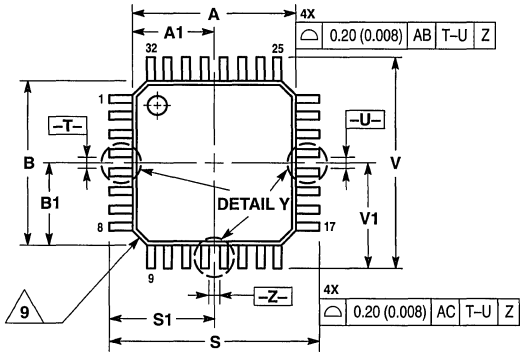


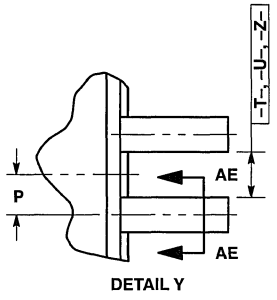
VIEW S

NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

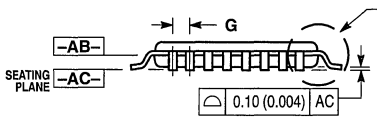
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0 81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0 040	—	1.02	—

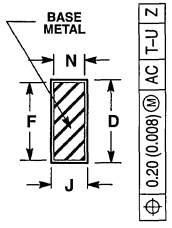
FA SUFFIX
TQFP PACKAGE
CASE 873A-02
ISSUE A



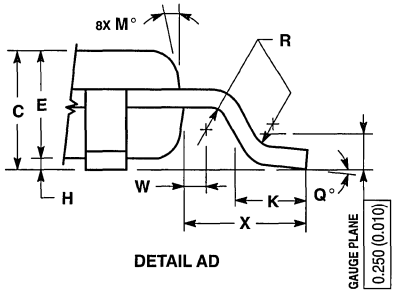


DETAIL Y





SECTION AE–AE

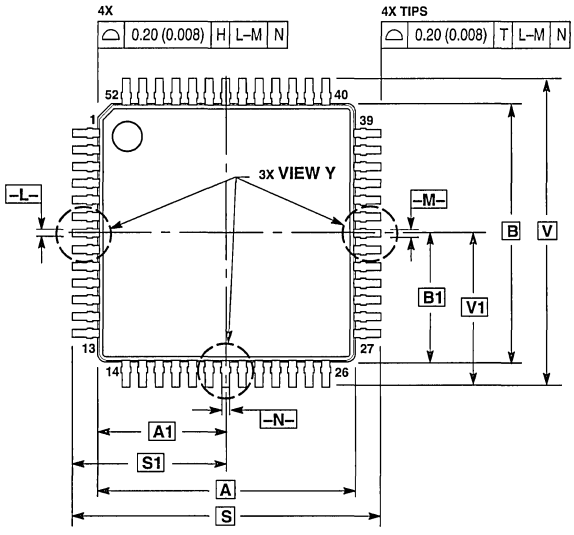


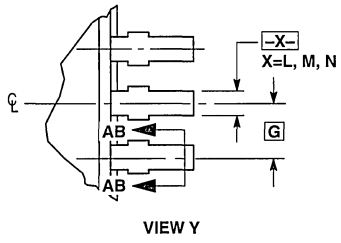
DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

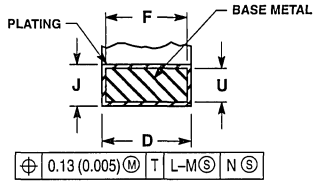
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

FA SUFFIX
TQFP PACKAGE
CASE 848D–03
ISSUE C

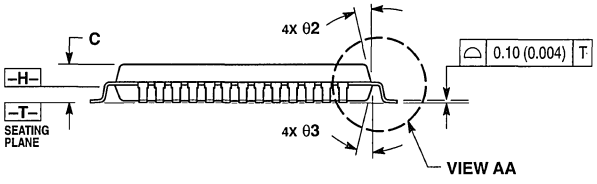




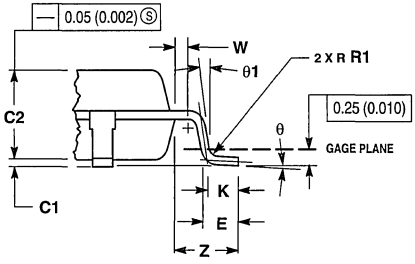
VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE



VIEW AA



VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	5°	13°	5°	13°

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