MOTOROLA

DL128/D
REV 6

Analog/Interface ICs

Device Data

Vol. I

MOTOROLA

ANALOG/INTERFACE ICs DEVICE DATA

Q4/96
DL128
REV 6

VOL. I

What's Different

New Additions

CHAPTER 3

LM2575
MC78BC00
MC78FC00
MC78LC00
MC33154
MC33264
MC33341
MC33347
MC33348
MC33363A
MC33364
MC33368
MC33463
MC33464
MC33465
MC33466
MC34065, MC33065
MC34165, MC33165
MC44604
MC44605

CHAPTER 7

MC1413
MC34156
SN75175

CHAPTER 8

MC13109
MC13110
MC13111
MC13144
MC13159

CHAPTER 9

MC13022
MC13029A
MC13081X
MC13022A
MC13280AY, MC13281A/B
MC13282A
MC13283
MC44007
MC44030/35
MC44306
MC44353
MC44354
MC44355
MC44461
MC44462
MC44463

CHAPTER 10

MC33143
MC33193
MC33197A
MC33293
MCCF33093
MCCF33094
MCCF33095

Deletes

LM307
LM248
MC1411
MC1412
MC1472
MC1748C
MC3361C
MC3371A
MC3372A
MC3430
MC3486
MC3487
MC13001X/07X
MC13017
MC13024
MC33292
MC33344
MC34050
MC34051
MC44301
MC44302
MC44303
MCT1413
SN75173

New Product Literature (Referenced)

AN454A
AN829
AN921
AN932
AN1044
AN1315
AN1539
AN1544
AN1548
AN1575

Not Recommended For New Designs

AM26LS31
AM26LS32
MC26S10
MC3373
MC3448A
MC3450
MC3453
MC3467
MC3481
MC3485
ULN2068
TDA1185A

3 Ways To Receive
Motorola Semiconductor Technical Information

Literature Distribution Centers

Printed literature can be obtained from the Literature Distribution Centers upon request. For those items that incur a cost, the U.S. Literature Distribution Center will accept Master Card and Visa.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center,
3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

Mfax is a trademark of Motorola, Inc.

Mfax™ – Touch–Tone Fax

Mfax offers access to over 30,000 Motorola documents for faxing to customers worldwide. With menus and voice instruction, customers can request the documents needed, using their own touch–tone telephones from any location, 7 days a week and 24 hours a day. A number of features are offered within the Mfax system, including: product data sheets, application notes, engineering bulletins, article reprints, selector guides, Literature Order Forms, Technical Training Information, and HOT DOCS (4–digit code identifiers for currently referenced promotional or advertising material).

A fax of complete, easy–to–use instructions can be obtained by a first–time phone call into the system, entering your FAX number, and then pressing 1.

How to reach us:

Mfax: RMFAX0@email.sps.mot.com – TOUCH–TONE (602) 244–6609
or via the http://Design–NET.com home page, select the Mfax Icon.

Motorola SPS World Marketing Internet Server

Motorola SPS's Electronic Data Delivery organization has set up a World Wide Web Server to deliver Motorola SPS's technical data to the global Internet community. Technical data such as the complete Master Selection Guide along with the OEM North American price book are available on the Internet server with full search capabilities. Other data on the server includes abstracts of data books, application notes, selector guides, and textbooks. All have easy text search capability. Ordering literature from the Literature Distribution Center is available on–line. Other features of Motorola SPS's Internet server include: the availability of a searchable press release database, technical training information with on–line registration capabilities, complete on–line access to the Mfax system for ordering faxes, an on–line technical support form to send technical questions and receive answers through email, information on product groups, full search capabilities of device models, a listing of the domestic and international sales offices, and direct links to other Motorola world wide web servers. For more information on Motorola SPS's Internet server you can request **BR1307/D** from Mfax or LDC.

How to reach us:

After accessing the Internet, use the following URL:
http://Design–NET.com

MOTOROLA

DL128/D
REV 6

Analog ICs

Device Data

Vol. I

This publication presents technical information for the broad line of Analog and Interface Integrated Circuit products. Complete device specifications are provided in the form of **Data Sheets** which are categorized by product type into ten chapters for easy reference. **Selector Guides** by product family are provided in the beginning of each chapter to enable quick comparisons of performance characteristics. A **Cross Reference** chapter lists Motorola nearest replacement and functional equivalent part numbers for other industry products.

One chapter is devoted showing all of the **Tape and Reel Options**. All **Packaging Information**, including surface mount packages, is provided in another chapter.

Additionally, chapters are provided with information on **Quality and Reliability Assurance** program concepts, high–reliability processing, and abstracts of available **Applications and Product Literature**.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

Series J
First Printing

Printed in U.S.A.

Data Classification

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

Advance Information

This heading on a data sheet indicates that the device is in sampling, pre–production, or first production stages. The disclaimer at the bottom of the first page reads: "This document contains information on a new product. Specifications and information herein are subject to change without notice."

Fully Released

A fully released data sheet contains neither a classification heading nor a disclaimer at the bottom of the first page. This document contains information on a product in full production. Guaranteed limits will not be changed without written notice to your local Motorola Semiconductor Sales Office.

Alphanumeric Index and Cross References

In Brief . . .

Motorola Analog and Interface Integrated Circuits cover a much broader range of products than the traditional op amps/regulators/consumer–image associated with Analog suppliers. Analog circuit technology currently influences the design and architecture of equipment for all major markets. As with other integrated circuit technologies, Analog circuit design techniques and processes have been continually refined and updated to meet the needs of these diversified markets.

Operational amplifiers have utilized JFET inputs for improved performance, plus innovative design and trimming concepts have evolved for improved high performance and precision characteristics. In analog power ICs, basic voltage regulators have been refined to include higher current and voltage levels, low dropout regulators, and more precise three–terminal fixed and adjustable voltages. The power area continues to expand into switching regulators, power supply control and supervisory circuits, motor controllers, and battery charging controllers.

Analog designs also offer a wide array of line drivers, receivers and transceivers for many of the EIA, European, IEEE and IBM interface standards. Peripheral drivers for a variety of devices are also offered. In addition to these key interface functions, hard disk drive read channel circuits, 10BASE–T and Ethernet circuits are also available.

In Data Conversion, a high performance video speed flash converter is available, as well as a variety of CMOS and Sigma–Delta converters. Analog circuit technology has also provided precision low–voltage references for use in Data Conversion and other low temperature drift applications.

A host of special purpose analog devices have also been developed. These circuits find applications in telecommunications, radio, television, automotive, RF communications, and data transmission. These products have reduced the cost of RF communications, and have provided capabilities in telecommunications which make the telephone line convenient for both voice and data communications. Analog developments have also reduced the many discrete components formerly required for consumer functions to a few IC packages and have made significant contributions to the rapidly growing market for electronics in automotive applications.

The table of contents provides a perspective of the many markets served by Analog/Interface ICs and of Motorola's involvement in these areas.

1

Alphanumeric Index

Device Number	Function	Page
AM26LS30	Dual Differential/Quad Single–Ended Line Drivers	7–13
AM26LS31#	Quad Line Driver with NAND Enabled Three–State Outputs	7–24
AM26LS32#	Quad EIA–422/423 Line Receiver with Three–State Outputs	7–24
CA3059	Zero Voltage Switches	4–14
CA3146	General Purpose Transistor Array	9–28
LF347, B	JFET Input Operational Amplifiers	2–11
LF351	JFET Input Operational Amplifiers	2–11
LF353	JFET Input Operational Amplifiers	2–11
LF411C	Low Offset, Low Drift JFET Input Operational Amplifiers	2–13
LF412C	Low Offset, Low Drift JFET Input Operational Amplifiers	2–13
LF441C	Low Power JFET Input Operational Amplifiers	2–17
LF442C	Low Power JFET Input Operational Amplifiers	2–17
LF444C	Low Power JFET Input Operational Amplifiers	2–17
LM11C, CL	Precision Operational Amplifiers	2–24
LM201A	Operational Amplifiers	2–30
LM211	Highly Flexible Voltage Comparator	2–39
LM224	Quad Low Power Operational Amplifiers	2–45
LM239, A	Quad Single Supply Comparators	2–52
LM258	Dual Low Power Operational Amplifiers	2–62
LM285	Micropower Voltage Reference Diodes	5–4
LM293	Low Offset Voltage Dual Comparators	2–68
LM301A	Operational Amplifiers	2–30
LM308A	Precision Operational Amplifier	2–34
LM311	Highly Flexible Voltage Comparator	2–39
LM317	Three–Terminal Adjustable Output Positive Voltage Regulator	3–45
LM317L	Three–Terminal Adjustable Output Voltage Regulator	3–53
LM317M	Three–Terminal Adjustable Output Positive Voltage Regulator	3–61
LM323, A	Positive Voltage Regulators	3–69
LM324, A	Quad Low Power Operational Amplifiers	2–45
LM337	Three–Terminal Adjustable Output Negative Voltage Regulator	3–75
LM337M	Three–Terminal Adjustable Output Negative Voltage Regulator	3–82
LM339, A	Quad Single Supply Comparators	2–52
LM340, A Series	Three–Terminal Positive Voltage Regulators	3–89
LM348	Differential Input Operational Amplifier	2–56
LM350	Three–Terminal Adjustable Output Positive Voltage Regulator	3–105
LM358	Dual Low Power Operational Amplifier	2–62
LM385, B	Micropower Voltage Reference Diodes	5–4
LM393, A	Low Offset Voltage Dual Comparators	2–68
LM833	Dual Low Noise, Audio Amplifier	2–73
LM2575	Easy Switcher 1.0 A Step–Down Voltage Regulator	3–113
LM2900	Quad Single Supply Operational Amplifier	2–113
LM2901, V	Quad Single Supply Comparator	2–52
LM2902, V	Quad Low Power Operational Amplifier	2–45
LM2903, V	Low Offset Voltage Dual Comparator	2–68
LM2904, V	Dual Low Power Operational Amplifier	2–62
LM2931	Low Dropout Voltage Regulator	3–136
LM2935	Low Dropout Dual Regulator	3–146
LM3900	Quad Single Supply Operational Amplifier	2–113
LP2950	Micropower Voltage Regulator	3–150
LP2951	Micropower Voltage Regulator	3–150
MC1350	Monolithic IF Amplifier	9–30
MC1374	TV Modulator Circuit	9–34
MC1377	Color TV RGB to PAL/NTSC Encoder	9–42
MC1378	Color TV Composite Video Overlay Synchronizer	9–58
MC1391	TV Horizontal Processor	9–62
MC1403, B	Low Voltage Reference	5–9
MC1404	Voltage References Family	5–13
MC1413, B	High Voltage, High Current Darlington Transistor Arrays	7–30
MC1416, B	High Voltage, High Current Darlington Transistor Arrays	7–30
MC1436, C	High Voltage, Internally Compensated Operational Amplifiers	2–79
MC1455, B	Timing Circuit	11–6
MC1458, C	Internally Compensated, High Performance Dual Operational Amplifiers	2–84
MC1488	Quad Line Driver	7–33
MC14C88B	Quad Low Power Line Driver	7–44
MC14C89B, AB	Quad Low Power Line Receiver	7–50
MC1489, A	Quad Line Receivers	7–39
MC1490	RF/IF Audio Amplifier	2–92
MC1494	Linear Four–Quadrant Multiplier	11–14
MC1495	Wideband Linear Four–Quadrant Multiplier	11–28
MC1496	Balanced Modulatosr/Demodulators	8–45
MC1723C	Voltage Regulator	3–162
MC1741C	Internally Compensated, High Performance Operational Amplifier	2–99
MC1776C	Micropower Programmable Operational Amplifier	2–104
MC2833	Low Power FM Transmitter System	8–55
MC3301	Quad Single Supply Operational Amplifier	2–113
MC3302	Quad Single Supply Comparators	2–52
MC3303	Quad Low Power Operational Amplifier	2–123
MC3334	High Energy Ignition Circuit	10–15
MC3335	Low Power Dual Conversion FM Receiver	8–62
MC3340	Electronic Attenuator	9–66
MC3346	General Purpose Transistor Array One Differentially Connected Pair and Three Isolated Transistor Arrays	9–69
MC3356	Wideband FSK Receiver	8–66
MC3357	Low Power FM IF	8–72
MC3358	Dual, Low Power Operational Amplifier	2–137
MC3359	Dual, Low Power Operational Amplifier	8–76
MC3362	Low Power Dual Conversion FM Receiver	8–82
MC3363	Low Power Dual Conversion FM Receiver	8–89
MC3371	Low Power Narrowband FM IF	8–97
MC3372	Low Power Narrowband FM IF	8–97
MC3373#	Remote Control Wideband Amplifier with Detector	9–72
MC3374	Low Voltage FM Narrowband Receiver	8–114
MC3392	Low Side Protected Switch	10–19
MC3399	Automotive Half–Amp High–Side Switch	10–28
MC3403	Quad Low Power Operational Amplifier	2–123

* = See Communications Device Data (DL136).
# = Not recommended for new designs.

Alphanumeric Index (continued)

Device Number	Function	Page
MC3405	Dual Operational Amplifier and Dual Comparator	2–129
MC3418	Continuously Variable Slope Delta Modulator/Demodulator	*
MC3419–IL	Telephone Line–Feed Circuit	*
MC3423	Overvoltage Crowbar Sensing Circuit	3–168
MC3425	Power Supply Supervisory/Over and Undervoltage Protection Circuit	3–174
MC3448A#	Bidirectional Instrumentation Bus (GPIB) Transceiver	7–58
MC3450#	Quad MTTL Compatible Line Receivers	7–64
MC3453#	MTTL Compatible Quad Line Driver	7–71
MC3456	Dual Timing Circuit	11–43
MC3458	Dual, Low Power Operational Amplifier	2–137
MC3467#	Triple Wideband Preamplifier with Electronic Gain Control (EGC)	7–76
MC3476	Low Cost Programmable Operational Amplifier	2–144
MC3479	Stepper Motor Driver	4–19
MC3481#	Quad Single–Ended Line Driver	7–81
MC3485#	Quad Single–Ended Line Driver	7–81
MC3488A	Dual EIA–423/EIA–232D Line Driver	7–86
MC3518	Continuously Variable Slope Delta Modulator/Demodulator	*
MC4558AC, C	Dual Wide Bandwidth Operational Amplifiers	2–149
MC4741C	Differential Input Operational Amplifier	2–156
MC7800 Series	Three–Terminal Positive Voltage Regulators	3–182
MC78L00, A Series	Three–Terminal Low Current Positive Voltage Regulators	3–197
MC78M00 Series	Three–Terminal Medium Current Positive Voltage Regulators	3–204
MC78T00 Series	Three–Ampere Positive Voltage Regulators	3–213
MC78BC00	Micropower Voltage Regulator	3–222
MC78FC00	Micropower Voltage Regulator	3–223
MC78LC00	Micropower Voltage Regulator	3–224
MC7900 Series	Three–Terminal Negative Voltage Regulators	3–225
MC79L00, A Series	Three–Terminal Low Currect Negative Voltage Regulators	3–235
MC79M00 Series	Three–Terminal Negative Voltage Regulators	3–240
MC10319	High Speed 8–Bit Analog–to–Digital Flash Converter	6–6
MC13020	Motorola C–QUAM AM Stereo Decoder	9–66
MC13022	Advanced Medium Voltage AM Stereo Decoder	9–81
MC13022A	Advanced Medium Voltage AM Stereo Decoder	9–86
MC13025	Electronically Tuned Radio Front End	9–91
MC13027	AMAX Stereo Chipset	9–94
MC13028A	Advanced Wide Voltage IF and C–QUAM AM Stereo Decoder	9–119
MC13029A	Advanced Wide Voltage IF and C–QUAM AM Stereo Decoder with FM Amplifier and AM/FM Internal Switch	9–137
MC13030	Dual Conversion AM Receiver	9–156
MC13055	Wideband FSK Receiver	8–121
MC13060	Mini–Watt Audio Output	9–171
MC13077	Advanced PAL/NTSC Encoder	9–175
MC13081X	Multimode Color Monitor Horizontal, Vertical and Video Combination Processor	9–187
MC13109	Universal Cordless Telephone Subsystem IC	8–128
MC13110	Universal Cordless Telephone Subsystem IC with Scrambler	8–154
MC13111	Universal Cordless Telephone Subsystem IC	8–185
MC13122	AMAX Stereo Chipset	9–94
MC13135	FM Communications Receiver	8–214
MC13136	FM Communications Receiver	8–214
MC13141	Low Power DC–1.8 GHz LNA and Mixer	8–226
MC13142	Low Power DC–1.8 GHz LNA, Mixer and VCO	8–235
MC13143	Ultra Low Power DC–2.4 GHz Linear Mixer	8–245
MC13144	VHF – 2.0 GHz Low Noise Amplifier with Programmable Bias	8–252
MC13150	Narrowband FM Coilless Detector IF Subsystem	8–258
MC13155	Wideband FM IF System	8–275
MC13156	Wideband FM IF System	8–290
MC13158	Wideband FM IF Subsystem	8–308
MC13159	Wideband FM IF Amplifier	8–330
MC13173	Infrared Integrated Transceiver System	8–336
MC13175	UHF FM/AM Transmitter	8–353
MC13176	UHF FM/AM Transmitter	8–353
MC13280AY	80/100 MHz Video Processor	9–205
MC13281A, B	80/100 MHz Video Processor	9–205
MC13282A	100 MHz Video Processor with OSD Interface	9–215
MC13283	130 MHz Video Processor with OSD Interface	9–226
MC26S10#	Quad Open–Collector Bus Transceiver	7–55
MC33023	High Speed Single–Ended PWM Controller	3–392
MC33025	High Speed Double–Ended PWM Controller	3–408
MC33030	DC Servo Motor Controller/Driver	4–27
MC33033	Brushless DC Motor Controller	4–41
MC33035	Brushless DC Motor Controller	4–64
MC33039	Closed–Loop Brushless Motor Adapter	4–87
MC33060A	Precision Switchmode Pulse Width Modulator Control Circuit	3–425
MC33063A	DC–to–DC Converter Control Circuit	3–437
MC33064	Undervoltage Sensing Circuit	3–446
MC33065	High Performance Dual Channel Current Mode Controller	3–451
MC33065–H, L	High Performance Dual Channel Current Mode Controllers	3–465
MC33066	High Performance Resonant Mode Controller	3–478
MC33067	High Performance Resonant Mode Controller	3–486
MC33071, A	High Slew Rate, Wide Bandwidth, Single Supply Operational Amplifiers	2–272
MC33072, A	High Slew Rate, Wide Bandwidth, Single Supply Operational Amplifiers	2–272
MC33074, A	High Slew Rate, Wide Bandwidth, Single Supply Operational Amplifiers	2–272
MC33076	Dual High Output Current, Low Power, Low Noise Bipolar Op Amp	2–161
MC33077	Dual, Low Noise Operational Amplifier	2–169
MC33078	Dual/Quad Low Noise Operational Amplifier	2–180
MC33079	Dual/Quad Low Noise Operational Amplifier	2–180
MC33091A	High Side TMOS Driver	10–31
MC33092	Alternator Voltage Regulator	10–45
MC33095	Integral Alternator Regulator	10–134
MC33102	Sleep–Mode Two–State, Micropower Operational Amplifier	2–189
MC33110	Low Voltage Compander	*
MC33111	Low Voltage Compander with Mute and Feedthrough	*
MC33120	Subscriber Loop Interface Circuit	*
MC33121	Low Voltage Subscriber Loop Interface Circuit	*
MC33128	Power Management Controller	3–244

* = See Communications Device Data (DL136).
# = Not recommended for new designs.

Alphanumeric Index (continued)

Device Number	Function	Page
MC33129	High Performance Current Mode Controller	3–499
MC33143	Dual High–Side Switch	10–45
MC33151	High Speed Dual MOSFET Driver	3–514
MC33152	High Speed Dual MOSFET Driver	3–522
MC33153	Single IGBT Gate Driver	3–251
MC33154	Single IGBT Gate Driver	3–262
MC33160	Microprocessor Voltage Regulator and Supervisory Circuit	3–530
MC33161	Universal Voltage Monitors	3–537
MC33163	Power Switching Regulator	3–550
MC33164	Micropower Undervoltage Sensing Circuit	3–564
MC33165	Power Switching Regulator	3–570
MC33166	Power Switching Regulator	3–584
MC33167	Power Switching Regulator	3–598
MC33169	GaAs Power Amplifier Support IC	3–263
MC33171	Low Power, Single Supply Operational Amplifier	2–201
MC33172	Low Power, Single Supply Operational Amplifier	2–201
MC33174	Low Power, Single Supply Operational Amplifier	2–201
MC33178	High Output Current, Low Power, Low Noise Bipolar Op Amp	2–208
MC33179	High Output Current, Low Power, Low Noise Bipolar Op Amp	2–208
MC33181	Low Power, High Slew Rate, Wide Bandwidth, JFET Input Op Amp	2–299
MC33182	Low Power, High Slew Rate, Wide Bandwidth, JFET Input Op Amp	2–299
MC33184	Low Power, High Slew Rate, Wide Bandwidth, JFET Input Op Amp	2–299
MC33192	Mi–Bus Interface Stepper Motor Controller	10–60
MC33193	Automotive Direction Indicator	10–71
MC33197A	Automotive Wash Wiper Timer	10–78
MC33199	Automotive ISO 9141 Serial Link Driver	10–83
MC33201	Rail–to–Rail Operational Amplifier	2–218
MC33202	Rail–to–Rail Operational Amplifier	2–218
MC33204	Rail–to–Rail Operational Amplifier	2–218
MC33206	Rail–to–Rail Operational Amplifier with Enable Feature	2–227
MC33207	Rail–to–Rail Operational Amplifier with Enable Feature	2–227
MC33218A	Voice Switched Speakerphone with Microprocessor Interface	*
MC33219A	Voice Switched Speakerphone	*
MC33261	Power Factor Controller	3–812
MC33262	Power Factor Controller	3–823
MC33264	Micropower Voltage Regulators with On/Off Control	3–273
MC33267	Low Dropout Regulator	3–280
MC33269 Series	Low Dropout Positive Voltage Regulator	3–285
MC33272A	Single Supply, High Slew Rate Low Input Offset Voltage, Bipolar Op Amp	2–237
MC33274A	Single Supply, High Slew Rate Low Input Offset Voltage, Bipolar Op Amp	2–237
MC33282	Low Input Offset, High Slew Rate, Wide Bandwidth, JFET Input Op Amp	2–246
MC33284	Low Input Offset, High Slew Rate, Wide Bandwidth, JFET Input Op Amp	2–246
MC33293A	Quad Low Side Switch	10–94
MC33298	Octal Output Driver	10–109
MC33304	Low Voltage Rail–to–Rail, Sleepmode Operational Amplifier	2–254
MC33340	Battery Fast Charge Controller	3–290
MC33341	Power Supply/Battery Charger Regulation Control Circuit	3–301
MC33345	Lithium Battery Protection Circuit for One to Four Cell Battery Packs	3–316
MC33346	Lithium Battery Protection Circuit for Three or Four Cell Battery Packs	3–328
MC33347	Lithium Battery Protection Circuit for One or Two Cell Battery Packs	3–329
MC33348	Lithium Battery Protection Circuit for One Cell Battery Packs	3–339
MC33362	High Voltage Switching Regulator	3–348
MC33363	High Voltage Switching Regulator	3–359
MC33363A	High Voltage Switching Regulator	3–370
MC33364	Critical Conduction SMPS Controller	3–371
MC33368	High Voltage GreenLine™ Power Factor Controller	3–372
MC33463	Variable Frequency Micropower DC–to–DC Converter	3–384
MC33464	Micropower Undervoltage Sensing Circuits	3–386
MC33465	Micropower Undervoltage Sensing Circuits with Output Delay	3–388
MC33466	Fixed Frequency PWM Micropower DC–to–DC Converter	3–390
MC34001, B	JFET Input Operational Amplifier	2–265
MC34002, B	JFET Input Operational Amplifier	2–265
MC34004, B	JFET Input Operational Amplifier	2–265
MC34010	Electronic Telephone Circuit	*
MC34011A	Electronic Telephone Circuit	*
MC34012	Telephone Tone Ringer	*
MC34014	Telephone Speech Network with Dialer Interface	*
MC34016	Cordless Universal Telephone Interface	*
MC34017	Telephone Tone Ringer	*
MC34018	Voice Switched Speakerphone Circuit	*
MC34023	High Speed Single–Ended PWM Controller	3–392
MC34025	High Speed Double–Ended PWM Controller	3–408
MC34055	IEEE 802.3 10BASE–T Transceiver	7–90
MC34058	Hex EIA–485 Transceiver with Three–State Outputs	7–105
MC34059	Hex EIA–485 Transceiver with Three–State Outputs	7–105
MC34060A	Precision Switchmode Pulse Width Modulator Control Circuit	3–425
MC34063A	DC–to–DC Converter Control Circuit	3–437
MC34064	Undervoltage Sensing Circuit	3–446
MC34065	High Performance Dual Channel Current Mode Controller	3–451
MC34065–H, L	High Performance Dual Channel Current Mode Controllers	3–465
MC34066	High Performance Resonant Mode Controller	3–478
MC34067	High Performance Resonant Mode Controller	3–486
MC34071, A	High Slew Rate, Wide Bandwidth, Single–Supply Operational Amplifier	2–272
MC34072, A	High Slew Rate, Wide Bandwidth, Single–Supply Operational Amplifier	2–272
MC34074, A	High Slew Rate, Wide Bandwidth, Single–Supply Operational Amplifier	2–272
MC34080	High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifier	2–288
MC34081	High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifier	2–288
MC34082	High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifier	2–288

* = See Communications Device Data (DL136).
# = Not recommended for new designs.

Alphanumeric Index (continued)

Device Number	Function	Page
MC34083	High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifier	2–288
MC34084	High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifier	2–288
MC34085	High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifier	2–288
MC34114	Telephone Speech Network with Dialer Interface	*
MC34115	Continuously Variable Slope Delta Modulator/Demodulator	*
MC34117	Telephone Tone Ringer	*
MC34118	Voice Switched Speakerphone Circuit	*
MC34119	Low Power Audio Amplifier	9–227
MC34129	High Performance Current Mode Controller	3–499
MC34151	High Speed Dual MOSFET Driver	3–514
MC34152	High Speed Dual MOSFET Driver	3–522
MC34156	28–Channel Inkjet Driver	7–116
MC34160	Microprocessor Voltage Regulator and Supervisory Circuit	3–530
MC34161	Universal Voltage Monitor	3–537
MC34163	Power Switching Regulator	3–550
MC34164	Micropower Undervoltage Sensing Circuit	3–564
MC34165	Power Switching Regulator	3–570
MC34166	Power Switching Regulator	3–584
MC34167	Power Switching Regulator	3–598
MC34181	Low Power, High Slew Rate, Wide Bandwidth, JFET Input Op Amp	2–299
MC34182	Low Power, High Slew Rate, Wide Bandwidth, JFET Input Op Amp	2–299
MC34184	Low Power, High Slew Rate, Wide Bandwidth, JFET Input Op Amp	2–299
MC34216A	Programmable Telephone Line Interface Circuit with Loudspeaker Amplifier	*
MC34250	5.0 V, 200 M–Bit/Sec PR–IV Hard Disk Drive Read Channel	7–118
MC34261	Power Factor Controller	3–612
MC34262	Power Factor Controller	3–623
MC34268	SCSI–2 Active Terminator Regulator	3–638
MC34270	Liquid Crystal Display and Backlight Integrated Circuit	3–641
MC34271	Liquid Crystal Display and Backlight Integrated Circuit	3–641
MC44002	Chroma 4 Multistandard Video Processor	9–236
MC44007	Chroma 4 Multistandard Video Processor	9–236
MC44011	Bus Controlled Multistandard Video Processor	9–275
MC44030	Multistandard Video Signal Processor with Integrated Delay Line	9–324
MC44035	Multistandard Video Signal Processor with Integrated Delay Line	9–324
MC44144	Subcarrier Phase–Locked Loop	9–326
MC44145	Pixel Clock Generator/Sync Separator	9–331
MC44353	PLL Tuned UHF Audio/Video Modulator ICs for PAL, SECAM and NTSC TV Systems	9–338
MC44354	PLL Tuned UHF Audio/Video Modulator ICs for PAL, SECAM and NTSC TV Systems	9–338
MC44355	PLL Tuned UHF Audio/Video Modulator ICs for PAL, SECAM and NTSC TV Systems	9–338
MC44461	Picture–in–Picture (PIP) Controller	9–341
MC44462	Y–C Picture–in–Picture (PIP) Controller	9–354
MC44463	Picture–in–Picture (PIP) Controller	9–360
MC44602	HIgh Performance Current Mode Controller	3–651
MC44603	Mixed Frequency Mode GreenLine PWM Controller	3–667
MC44604	High Safety Standby Ladder Mode GreenLine PWM Controller	3–689
MC44605	High Safety Latched Mode GreenLine PWM Controller for (Multi) Synchronized Applications	3–690
MC44817, B	PLL Tuning Circuit with 3–Wire Bus	9–367
MC44818	PLL Tuning Circuit with I2C Bus	9–374
MC44824, 25	PLL Tuning Circuit with I2C Bus	9–381
MC44826	PLL Tuning Circuit with I2C Bus	9–388
MC44827	PLL Tuning Circuit with 3–Wire Bus	9–395
MC44828	PLL Tuning Circuit with I2C Bus	9–396
MC44829	PLL Tuning Circuit with I2C Bus	9–397
MC44864	PLL Tuning Circuit with 1.3 GHz Prescaler and D/A Converters for Automatic Tuner Alignment	9–405
MC68160	Enhanced Ethernet Transceiver	7–120
MC75172B	Quad EIA–485 Line Driver with Three–State Output	7–146
MC75174B	Quad EIA–485 Line Driver with Three–State Output	7–146
MC79076	Electronic Ignition Control Chip	10–131
MCC3334	High Energy Ignition Circuit	10–15
MCCF3334	High Energy Ignition Circuit	10–15
MCCF33093	Ignition Control Flip–Chip	10–132
MCCF33094	Ignition Control Flip–Chip	10–133
MCCF33095	Integral Alternator Regulator	10–134
MCCF79076	electronic Ignition Control Chip	10–131
MCT1458, C	Internally Compensated, High Performance Dual Operational Amplifier	2–89
MCT4558C	Dual Wide Bandwidth Operational Amplifier	2–153
SAA1042	Stepper Motor Driver	4–92
SG3525A	Pulse Width Modulator Control Circuit	3–691
SG3526	Pulse Width Modulator Control Circuit	3–697
SG3527A	Pulse Width Modulator Control Circuit	3–691
SN75175	Quad EIA–485 Line Receiver	7–157
TCA0372	Dual Power Operational Amplifier	2–308
TCA3385	Telephone Ring Signal Converter	*
TCA3388	Telephone Speech Network	*
TCA5600	Universal Microprocessor Power Supply/Controller	3–705
TCF5600	Universal Microprocessor Power Supply/Controller	3–705
TCF6000	Peripheral Clamping Array	10–144
TDA1085C	Universal Motor Speed Controller	4–97
TDA1185A#	Triac Phase Angle Controller	4–107
TL062	Low Power JFET Input Operational Amplifier	2–312
TL064	Low Power JFET Input Operational Amplifier	2–312
TL071C, AC	Low Noise JFET Input Operational Amplifier	2–319
TL072C, AC	Low Noise JFET Input Operational Amplifier	2–319
TL074C, AC	Low Noise JFET Input Operational Amplifier	2–319
TL081C, AC	JFET Input Operational Amplifier	2–325
TL082C, AC	JFET Input Operational Amplifier	2–325
TL084C, AC	JFET Input Operational Amplifier	2–325
TL431, A, B Series	Programmable Precision References	5–18
TL494	Switchmode Pulse Width Modulation Control Circuit	3–716
TL594	Precision Switchmode Pulse Width Modulation Control Circuit	3–726

* = See Communications Device Data (DL136).
# = Not recommended for new designs.

Alphanumeric Index (continued)

Device Number	Function	Page
TL780 Series	Three–Terminal Positive Fixed Voltage Regulator	3–736
UAA1016B	Zero Voltage Controller	4–116
UAA1041b	Automotive Direction Indicator	10–148
UAA2016	Zero Voltage Switch Power Controller	4–122
UC2842A	High Performance Current Mode Controller	3–742
UC2842B	High Performance Current Mode Controller	3–755
UC2843A	High Performance Current Mode Controller	3–742
UC2843B	High Performance Current Mode Controller	3–755
UC2844	High Performance Current Mode Controller	3–769
UC2844B	High Performance Current Mode Controller	3–782
UC2845	High Performance Current Mode Controller	3–769
UC2845B	High Performance Current Mode Controller	3–782
UC3842A	High Performance Current Mode Controller	3–742
UC3842B	High Performance Current Mode Controller	3–755
UC3843A	High Performance Current Mode Controller	3–742
UC3843B	High Performance Current Mode Controller	3–755
UC3844	High Performance Current Mode Controller	3–769
UC3844B	High Performance Current Mode Controller	3–782
UC3845	High Performance Current Mode Controller	3–769
UC3845B	High Performance Current Mode Controller	3–782
UC3844B	High Performance Current Mode Controller	3–782
UC3845	High Performance Current Mode Controller	3–769
UC3845B	High Performance Current Mode Controller	3–782
ULN2068#	Quad 1.5 A Sinking High Current Switch	7–162
ULN2803	Octal High Voltage, High Current Darlington Transistor Array	7–166
ULN2804	Octal High Voltage, High Current Darlington Transistor Array	7–166
µA78S40	Universal Switching Regulator Subsystem	3–796

* = See Communications Device Data (DL136).
# = Not recommended for new designs.

Cross References

The following table represents a cross reference guide for all Analog devices that are manufactured by Motorola. Where the Motorola part number differs from the industry part number, the Motorola device is a "form, fit and function" replacement for the industry part number. However, some differences in characteristics and/or specifications may exist.

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
75175	SN75175	
9636AT	MC3488AP	
9640PC	MC26S10P#	
9667PC	MC1413P	
9668PC	MC1416P	
AD589J		LM385Z–1.2
AD589K		LM385Z–1.2
AD589L		LM385Z–1.2
AD589M		LM385BZ–1.2
AM201AD		LM201AN
AM201D		LM201AN
AM26LS30P	AM26LS30PC	
AM26LS31CJ	AM26LS31PC#	
AM26LS31CN	AM26LS31PC#	
AM26LS32ACJ	AM26LS32D#	
AM26LS32ACN	AM26LS32PC#	
AM26LS32PC	AM26LS32PC#	
AM723PC	MC1723CP	
AN5150		MC34129P
CA081AE		TL081ACP
CA081E		TL081CP
CA082AE		TL082ACP
CA082E		TL082CP
CA084AE		TL084ACN
CA084E		TL084CN
CA1391E	MC1391P	
CA1458S	MC1458CP1	
CA239AE	LM239AN	
CA239E	LM239N	
CA3026		CA3054
CA3045F		MC3346P
CA3046	MC3346P	
CA3054	CA3054	
CA3058		CA3059
CA3059	CA3059	
CA3079	CA3079	
CA3086F		MC3346P
CA3136A		MC3346P
CA3146		MC3346P
CA339AE	LM339AN	
CA339E	LM339N	
CA723CE	MC1723CP	
CA741CS	MC1741CP1	
CS2842AD	UC2842BD1	
CS2843AD	UC2843BD1	
CS2844D	UC2844BD1	
CS2845D	UC2845BD1	
CS3842AD	UC3842BD1	
CS3843AD	UC3843BD1	
CS3844D	UC3844BD1	
CS3845D	UC3845BD1	
DM8822N		MC1489AP
DS1233M		MC34064P–5
DS1488N	MC1488P	
DS1489AN	MC1489AP	
DS1489N	MC1489P	
DS26LS32N	AM26LS32P#	
DS26S10CN	MC26S10P#	
DS3650N	MC3450P#	
DS8834N		MC8T26AP
DS8835N		MC8T26AP
DS9636ACN	MC3488AP1	
ICL741CLNPA		MC1741CP1
ICL741CLNTY		MC1741CP1
ICL8008CPA		LM301AN
ICL8008CTY		LM301AN
ICL8017CTW		LM301AN
ICL8017MTW		LM301AN
ICL8069CCZR		LM385BZ–1.2
ICL8069DCZR		LM385BZ–1.2
IP33063N	MC33063AP1	
IP34060AN	MC34060AP	
IP34063N	MC34063AP1	
IP3525AN	SG3525AN	
IP3526N	SG3526N	
IP3527AN	SG3527AN	
LM240LAZ–18		MC78L18ACP
LM240LAZ–24		MC78L24ACP
LM240LAZ–5.0		MC78L05ACP
LM240LAZ–6.0		MC78L05ACP
LM240LAZ–8.0		MC78L08ACP
LM249N		MC4741CP
LM2575	LM2575	
LM258D	LM258D	
LM258M	LM258D	
LM258N	LM258N	
LM285Z–1.2	LM285Z–1.2	
LM285Z–2.5	LM285Z–2.5	
LM2901D	LM2901D	
LM2901M	LM2901D	
LM2901N	LM2901N	
LM2902D	LM2902D	

= Not recommended for new designs.

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
IP494ACJ		TL594IN
IP494ACN		TL594CN
IR3M03A		MC34063AP1
IR3M03AN		MC34063AD
ITT3710		MC1391P
ITT656	MC1413P	
L144AP		LM324N
L203	MC1413P	
L387		MC33267T
LF347BN	LF347BN	
LF347N	LF347N	
LF351BN		MC34001BP
LF351N	LF351N	
LF353AN	MC34002AP	
LF353BN	MC34002BP	
LF353D	LF353D	
LF353N	LF353N	
LF411CD	LF411CD	
LF412CD	LF412CD	
LF441CD	LF441CD	
LF441CN	LF441CN	
LF442CD	LF442CD	
LF442CN	LF442CN	
LF444CD	LF444CD	
LF444CN	LF444CN	
LM11CLN	LM11CLN	
LM11CN	LM11CN	
LM139N	MC1391P	
LM1489AN	MC1489AP	
LM1489N	MC1489P	
LM1496N	MC1496P	
LM1496M	MC1496D	
LM1889		MC1374P
LM1981		MC13020P
LM201AD	LM201AD	
LM201AN	LM201AN	
LM201AP		LM201AN
LM211D	LM211D	
LM211M	LM211D	
LM224D	LM224D	
LM224M	LM224D	
LM224N	LM224N	
LM239AN	LM239AN	
LM239D	LM239D	
LM239M	LM239D	
LM239N	LM239N	
LM240LAZ–12		MC78L12ACP
LM240LAZ–15		MC78L15ACP
LM2902M	LM2902D	
LM2902N	LM2902N	
LM2903D	LM2903D	
LM2903M	LM2903D	

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
LM2903N	LM2903N	
LM2903P	LM2903N	
LM2904M	LM2904D	
LM2904N	LM2904N	
LM2905N		MC1455P1
LM2931AD–5.0	LM2931AD–5.0	
LM2931AT–5.0	LM2931AT–5.0	
LM2931AZ–5.0	LM2931AZ–5.0	
LM2931CD	LM2931CD	
LM2931CM	LM2931CD	
LM2931CT	LM2931CT	
LM2931D–5.0	LM2931D–5.0	
LM2931D	LM2931D–5.0	
LM2931T–5.0	LM2931T–5.0	
LM2931Z–5.0	LM2931Z–5.0	
LM2935T	LM2935T	
LM293D	LM293D	
LM301AD	LM301AD	
LM301AM	LM301AD	
LM301AN	LM301AN	
LM301AP		LM301AN
LM3045		MC3346P
LM3046N	MC3346P	
LM3054	CA3054	
LM308AD	LM308AD	
LM308AN	LM308AN	
LM308P		MC3356P
LM311D	LM311D	
LM311M	LM311D	
LM311N	LM311N	
LM311P	LM311N	
LM3146A		MC3346P
LM3146		MC3346P
LM317KC	LM317T	
LM317KD		LM317T
LM317LD	LM317LD	
LM317LZ	LM317LZ	
LM317MP		LM317MT
LM317P		LM317T
LM317T	LM317T	
LM3189		MC3356P
LM320LZ–12		MC79L12ACP
LM320LZ–15		MC79L15ACP
LM320LZ–5.0		MC79L05ACP
LM320MP–12		MC7912CT
LM320MP–15		MC7915CT
LM320MP–18		MC7918CT
LM320MP–24		MC7924CT
LM340LAZ–5.0		MC78L05ACP
LM340LAZ–8.0		MC78L08ACP
LM340T–12	LM340T–12	
LM340T–15	LM340T–15	

= Not recommended for new designs.

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
LM320MP–5.0		MC7905CT
LM320MP–5.2		MC7905.2CT
LM320MP–6.0		MC7906CT
LM320MP–8.0		MC7908CT
LM320T–12		MC7912CT
LM320T–15		MC7915CT
LM320T–5.0		MC7905CT
LM320T–5.2		MC7905.2CT
LM322N		MC1455P1
LM323AT	LM323AT	
LM323T	LM323T	
LM324AD	LM324AD	
LM324AN	LM324AN	
LM324D	LM324D	
LM324M	LM324D	
LM324N	LM324N	
LM337MP		LM337MT
LM337MT	LM337MT	
LM337T	LM337T	
LM339AD	LM339AD	
LM339AM	LM339AD	
LM339AN	LM339AN	
LM339D	LM339D	
LM339N	LM339N	
LM339P		LM339N
LM340AT–12	LM340AT–12	
LM340AT–15	LM340AT–15	
LM340AT–5.0	LM340AT–5.0	
LM340KC–12	LM340T–12	
LM340KC–15	LM340T–15	
LM340LAZ–12		MC78L12ACP
LM340LAZ–18		MC78L18ACP
LM340LAZ–24		MC78L24ACP
LM340T–18	LM340T–18	
LM340T–24	LM340T–24	
LM340T–5.0	LM340T–5.0	
LM340T–6.0	LM340T–6.0	
LM340T–8.0	LM340T–8.0	
LM341P–12		MC78M12CT
LM341P–15		MC78M15CT
LM341P–18		MC78M18CT
LM341P–24		MC78M24CT
LM341P–5.0		MC78M05CT
LM341P–6.0		MC78M06CT
LM341P–8.0		MC78M08CT
LM342P–12		MC78M12CT
LM342P–15		MC78M15CT
LM342P–18		MC78M18CT
LM342P–24		MC78M24CT
LM342P–5.0		MC78M05CT
LM342P–6.0		MC78M06CT
LM342P–8.0		MC78M08CT

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
LM348D	LM348D	
LM348M	LM348D	
LM349N		MC4741CP
LM350T	LM350T	
LM358AN		LM358N
LM358D	LM358D	
LM358N	LM358N	
LM363AN		MC3450P#
LM363N		MC3450P#
LM385BZ–1.2	LM385BZ–1.2	
LM385BZ–2.5	LM385BZ–2.5	
LM385D–1.2	LM385D–1.2	
LM385D–2.5	LM385D–2.5	
LM385M–1.2	LM385D–1.2	
LM385M–2.5	LM385D–2.5	
LM385Z–1.2	LM385Z–1.2	
LM385Z–2.5	LM385Z–2.5	
LM386N		MC34119P
LM3905N		MC1455P1
LM393AN	LM393AN	
LM393D	LM393D	
LM393JG		LM393N
LM393M	LM393D	
LM393N	LM393N	
LM431ACZ	TL431ACLP	
LM431ACM	TL431ACD	
LM4250CN		MC1776CP1
LM555CN	MC1455P1	
LM556CN	MC3456P	
LM703LN		MC1350P
LM723CN	MC1723CP	
LM741EN		MC1741CP1
LM7805CT	MC7805CT	
LM7812CT	MC7812CT	
LM7815CT	MC7815CT	
LM78L05ACZ	MC78L05ACP	
LM78L05CZ	MC78L05CP	
LM78L08ACZ	MC78L08ACP	
LM78L08CZ	MC78L08CP	
LM78L12ACZ	MC78L12ACP	
LM78L12CZ	MC78L12CP	
LM78L15ACZ	MC78L15ACP	
LM78L15CZ	MC78L15CP	
LM78L18ACZ	MC78L18ACP	
LM78L18CZ	MC78L18CP	
LM78L24ACZ	MC78L24ACP	
LM78L24CZ	MC78L24CP	
LM78M05CP		MC78M05CT
LM78M06CP		MC78M06CT
LM78M12CP		MC78M12CT
LM78M15CP		MC78M15CT
LM7905CT	MC7905CT	

= Not recommended for new designs.

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
LM7912CT	MC7912CT	
LM7915CT	MC7915CT	
LM79L05ACZ	MC79L05ACP	
LM79L12ACZ	MC79L12ACP	
LM79L15ACZ	MC78L15ACP	
LM79M05CP		MC79M05CT
LM79M12CP		MC79M12CT
LM79M15CP		MC79M15CT
LM833D	LM833D	
LM833N	LM833N	
LM833P	LM833N	
LM837N		MC33079P
LMC6482D		MC33202D
LMC6482P		MC33202P
LMC6484D		MC33204D
LMC6484P		MC33204P
LP2950CZ-3.0	LP2950CZ-3.0	
LP2950CZ-3.3	LP2950CZ-3.3	
LP2950CZ-5.0	LP2950CZ-5.0	
LP2950ACZ-3.0	LP2950ACZ-3.0	
LP2950ACZ-3.3	LP2950ACZ-3.3	
LP2950ACZ-5.0	LP2950ACZ-5.0	
LP2951CM	LP2951CD	
LP2951ACM	LP2951ACD	
LP2951CM-3.0	LP2951CD-3.0	
LP2951CM-3.3	LP2951CD-3.3	
LP2951ACM-3.0	LP2951ACD-3.0	
LP2951ACM-3.3	LP2951ACD-3.3	
LP2951CN	LP2951CN	
LP2951ACN	LP2951ACN	
LP2951CN-3.0	LP2951CN-3.0	
LP2951CN-3.3	LP2951CN-3.3	
LP2951ACN-3.0	LP2951ACN-3.0	
LP2951ACN-3.3	LP2951ACN-3.3	
LT1083		MC34268DT
LT1431CZ	TL431BCLP	
LTC699CN8		MC34064D-5
LTC699IN8		MC33064D-5
MAX809LCPA		MC34064P-5
MB3759	TL494CN	
N5558V	MC1458P1	
N5723A		MC1723CP
N5741A		MC1741CP1
N5741V	MC1741CP1	
N8T26AB	MC8T26AP	
N8T26AN	MC8T26AP	
N8T26B	MC8T26AP	
N8T26N	MC8T26AP	
N8T97B	MC8T97P	
N8T97N	MC8T97P	
N8T98B	MC8T98P	
N8T98N	MC8T98P	

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
NE550A		MC1723CP
NE555D	MC1455D	
NE555V	MC1455P1	
NE556D	NE556D	
NE5561N		MC34060AP
NE5234D		MC33204D
NE5234P		MC33204P
OP-01P		MC1436P1
RC1458DN	MC1458P1	
RC4136DP		MC3403P
RC4136N		MC3403P
RC4558DN	MC4558CP1	
RC4558P	MC4558CP1	
RC723DB	MC1723CP	
RC741DN	MC1741CP1	
RE5VL47A	MC34164P-5	
RH5RE30AA-T1	MC78LC30HT1	
RH5RE33AA-T1	MC78LC33HT1	
RH5RE40AA-T1	MC78LC40HT1	
RH5RE50AA-T1	MC78LC50HT1	
RN5RG30AA-TR	MC78BC30NTR	
RN5RG33AA-TR	MC78BC33NTR	
RN5RG40AA-TR	MC78BC40NTR	
RN5RG50AA-TR	MC78BC50NTR	
RH5RH301A-T1	MC33466H-30JT1	
RH5RH302B-T1	MC33466H-30LT1	
RH5RH331A-T1	MC33466H-33JT1	
RH5RH332B-T1	MC33466H-33LT1	
RH5RH501A-T1	MC33466H-50JT1	
RH5RH502B-T1	MC33466H-50LT1	
RH5RI301B-T1	MC33463H-30KT1	
RH5RI302B-T1	MC33463H-30LT1	
RH5RI331B-T1	MC33463H-33KT1	
RH5RI332B-T1	MC33463H-33LT1	
RH5RI501B-T1	MC33463H-50KT1	
RH5RI502B-T1	MC33463H-50LT1	
RH5RL30AA-T1	MC78FC30HT1	
RH5RL33AA-T1	MC78FC33HT1	
RH5RL40AA-T1	MC78FC40HT1	
RH5RL50AA-T1	MC78FC50HT1	
RH5VT09AA-T1	MC33464H-09AT1	
RH5VT20AA-T1	MC33464H-20AT1	
RH5VT27AA-T1	MC33464H-27AT1	
RH5VT30AA-T1	MC33464H-30AT1	
RH5VT45AA-T1	MC33464H-45AT1	
RH5VT09CA-T1	MC33464H-09CT1	
RH5VT20CA-T1	MC33464H-20CT1	
RH5VT27CA-T1	MC33464H-27CT1	
RH5VT30CA-T1	MC33464H-30CT1	
RH5VT45CA-T1	MC33464H-45CT1	
RN5RL30AA-TR	MC78FC30NTR	
RN5RL33AA-TR	MC78FC33NTR	

= Not recommended for new designs.

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
RN5RL40AA–TR	MC78FC40NTR	
RN5RL50AA–TR	MC78FC50NTR	
RN5VD09AA–TR	MC33465N–09ATR	
RN5VD20AA–TR	MC33465N–20ATR	
RN5VD27AA–TR	MC33465N–27ATR	
RN5VD30AA–TR	MC33465N–30ATR	
RN5VD45AA–TR	MC33465N–45ATR	
RN5VD09CA–TR	MC33465N–09CTR	
RN5VD20CA–TR	MC33465N–20CTR	
RN5VD27CA–TR	MC33465N–27CTR	
RN5VD30CA–TR	MC33465N–30CTR	
RN5VD45CA–TR	MC33465N–45CTR	
RN5VT09AA–TR	MC33464N–09ATR	
RN5VT20AA–TR	MC33464N–20ATR	
RN5VT27AA–T4	MC33464N–27ATR	
RN5VT30AA–TR	MC33464N–30ATR	
RN5VT45AA–TR	MC33464N–45ATR	
RN5VT09CA–TR	MC33464N–09CTR	
RN5VT20CA–TR	MC33464N–20CTR	
RN5VT27CA–TR	MC33464N–27CTR	
RN5VT30CA–TR	MC33464N–30CTR	
RN5VT45CA–TR	MC33464N–45CTR	
S–80743AN		MC34164P–3
SA555N	MC1455BP1	
SAA1042		SAA1042V
SG1458M	MC1458P1	
SG1496N	MC1496P	
SG1596J	MC1496BP	
SG201AM	LM201AN	
SG201AN		LM201AN
SG201M	LM201AN	
SG201N		LM201AN
SG224N	LM224N	
SG300N		MC1723CP
SG301AM	LM301AN	
SG301AN		LM301AN
SG308AM	LM308AN	
SG3118AM		LM308AN
SG311M	LM311N	
SG317P	LM317T	
SG317R		LM317T
SG324N	LM324N	
SG337P	LM337T	
SG337R		LM337T
SG3423M		MC3423P1
SG3525AN	SG3525AN	
SG3526N	SG3526N	
SG3527AN	SG3527AN	
SG3561	MC34261P	
SG4250CM		MC1776CP1
SG555CM	MC1455P1	
SG556CN	MC3456P	

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
SG723CN	MC1723CP	
SG741CM	MC1741CP1	
SG777CN		LM308AN
SG7805ACP	MC7805ACT	
SG7805ACR		MC7805ACT
SG7805ACT		MC7805ACT
SG7805CP	MC7805CT	
SG7806ACP	MC7806ACT	
SG7806ACR		MC7806ACT
SG7806ACT		MC7806ACT
SG7806CP	MC7806CT	
SG7806CR		MC7806CT
SG7808ACP	MC7808ACT	
SG7808ACT		MC7808ACT
SG7808CP	MC7808CT	
SG7808CR		MC7808CT
SG7812ACP	MC7812ACT	
SG7812ACR		MC7812ACT
SG7812ACT		MC7812ACT
SG7812CP	MC7812CT	
SG7812CR		MC7812CT
SG7815ACP	MC7815ACT	
SG7815ACR		MC7815ACT
SG7815ACT		MC7815ACT
SG7815CP	MC7815CT	
SG7815CR		MC7815CT
SG7815CT		MC7815CT
SG7818ACP	MC7818ACT	
SG7818ACR		MC7818ACT
SG7818ACT		MC7818ACT
SG7818CP	MC7818CT	
SG7818CR		MC7818CT
SG7824ACP	MC7824ACT	
SG7824ACR		MC7824ACT
SG7824ACT		MC7824ACT
SG7824CP	MC7824CT	
SG7824CR		MC7824CT
SG7905.2CP	MC7905.2CT	
SG7905.2CR		MC7905.2CT
SG7905.2CT		MC7905.2CT
SG7905ACP	MC7905ACT	
SG7905ACR		MC7905ACT
SG7905ACT		MC7905ACT
SG7905CP	MC7905CT	
SG7905CR		MC7905CT
SG7905CT		MC7905CT
SG7908CP	MC7908CT	
SG7908CR		MC7908CT
SG7908CT		MC7908CT
SG7912ACP	MC7912ACT	
SG7912ACR		MC7912ACT
SG7912ACT		MC7912ACT

= Not recommended for new designs.

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
SG7912CP	MC7912CT	
SG7912CR		MC7912CT
SG7912CT		MC7912CT
SG79015ACP	MC7915ACT	
SG7915ACR		MC7915ACT
SG7915ACT		MC7915ACT
SG7915CP	MC7915CT	
SG7915CR		MC7915CT
SG7915CT		MC7915CT
SG7918CP	MC7918CT	
SN75LBC086		MC34055DW
SN75121N		MC3481/5P#
SN75126N		MC3481/5P#
SN75150N		MC1488P
SN75154N		MC1489P
SN75174N	MC75174BP	
SN75175N	SN75175N	
SN75188N	MC1488P	
SN75189AN	MC1489AP	
SN75189N	MC1489P	
SN75468N	MC1413P	
SN76591P	MC1391P	
SN76600P	MC1350P	
SSS201AP	LM201AN	
SSS301AP	LM301AN	
TA7504P	MC1741CP1	
TA7506P	LM301AN	
TA75071P		MC34001P
TA75072P		MC34002P
TA75074F		MC34004P
TA75339F	LM339D	
TA75339P	LM339N	
TA75358CF	LM358D	
TA75358CP	LM358N	
TA75393F	LM393D	
TA75393P	LM393N	
TA75458F	MC1458D	
TA75458P	MC1458CP1	
TA75558P	MC4558CP1	
TA7555F	MC1455D	
TA7555P	MC1455P1	
TA75902F	LM324D	
TA76494P		TL494IN
TA78005AP	MC7805CT	
TA78006AP	MC7806CT	
TA78008AP	MC7808CT	
TA78012AP	MC7812CT	
TA78015AP	MC7815CT	
TA78018AP	MC7818CT	
TA78024AP	MC7824CT	
TA78L005AP		MC78L05ACP
TA78L005P		MC78L05CP

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
TA78L008AP		MC78L08ACP
TA78L008P		MC78L08CP
TA78L012AP		MC78L12ACP
TA78L012P		MC78L12CP
TA78L015AP		MC78L15ACP
TA78L015P		MC78L15CP
TA78L018AP		MC78L18ACP
TA78L018P		MC78L18CP
TA78L024AP		MC78L24ACP
TA78L024P		MC78L24CP
TA78M05P	MC78M05CT	
TA78M06P	MC78M06CT	
TA78M08P	MC78M08CT	
TA78M12P	MC78M12CT	
TA78M18P	MC78M18CT	
TA78M20P	MC78M20CT	
TA78M24P	MC78M24CT	
TA79005P	MC7905CT	
TA79006P	MC7906CT	
TA79008P	MC7908CT	
TA79012P	MC7912CT	
TA79015P	MC7915CT	
TA79018P	MC7918CT	
TA79024P	MC7924CT	
TA79L005P		MC79L05CP
TA79L012P		MC79L12P
TA79L015P		MC79L15P
TA79L018P		MC79L18P
TA79L024P		MC79L24P
TB920		MC1391P
TBA920S		MC1391P
TCF5600	TCF5600	
TD62003P/AP	MC1413P	
TD62479P	MC1374P	
TDA1085C	TDA1085C	
TDA1085		TDA1085C
TDA1185A	TDA1185A#	
TDA4817		MC34261P
TDC1018		MC10324P
TDC1048		MC10319P
TK115	MC33264	
TL022CP		LM358N
TL044CJ		LM324N
TL062ACP	TL062ACP	
TL062CD	TL062CD	
TL062CP	TL062CP	
TL062VP	TL062VP	
TL064ACD	TL064ACD	
TL064ACN	TL064ACN	
TL064CD	TL064CD	
TL064CN	TL064CN	
TL064VN	TL064VN	

= Not recommended for new designs.

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
TL071ACD	TL071ACD	
TL071ACP	TL071ACP	
TL071CD	TL071CD	
TL071CP	TL071CP	
TL072ACD	TL072ACD	
TL072ACP	TL072ACP	
TL072CD	TL072CD	
TL072CP	TL072CP	
TL074ACN	TL074ACN	
TL074CN	TL074CN	
TL081ACD	TL081ACD	
TL081ACP	TL081ACP	
TL081CD	TL081CD	
TL081CP	TL081CP	
TL082ACP	TL082ACP	
TL082CD	TL082CD	
TL082CP	TL082CP	
TL084ACN	TL084ACN	
TL084CN	TL084CN	
TL431CD	TL431CD	
TL431CLP	TL431CLP	
TL431CP	TL431CP	
TL431ILP	TL431ILP	
TL431IP	TL431IP	
TL494CN	TL494CN	
TL494IN	TL494IN	
TL497CN		MC34063AP1
TL594CN	TL594CN	
TL594IN	TL594IN	
TL780–05CKC	TL780–05CKC	
TL780–12CKC	TL780–12CKC	
TL780–15CKC	TL780–15CKC	
TL7805ACKC	MC7805ACT	
TLC2272D		MC33202D
TLC2272P		MC33202P
TLC2274D		MC33204D
TLC2274P		MC33204P
µA1391PC	MC1391P	
µA1458CP	MC1458CP1	
µA1458CTC	MC1458CP1	
µA1458P	MC1458P1	
µA1458TC	MC1458P1	
µA2240PC		MC1455P1
µA301AT	LM301AN	
µA3026HM		CA3054
µA3045		MC3346P
µA3046DC	MC3346P	
µA3054DC	CA3054	
µA311T	LM311N	
µA317UC	LM317T	
µA3303P	MC3303P	
µA3403P	MC3403P	

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
µA4136PC		MC4741CP
µA431AWC	TL431CP	
µA4558TC	MC4558CP1	
µA494PC	TL494CN	
µA555TC	MC1455P1	
µA556PC	MC3456P	
µA723CN	MC1723CP	
µA723PC	MC1723CP	
µA741CP	MC1741CP1	
µA742DC		CA3059
µA757DC		MC1350P
µA757DM		MC1350P
µA775PC	LM339N	
µA776TC	MC1776CP1	
µA7805CKC	MC7805CT	
µA7805UC	MC7805CT	
µA7805UV	MC7805BT	
µA7806CKC	MC7806CT	
µA7806UC	MC7806CT	
µA7806UV	MC7806BT	
µA7808CKC	MC7808CT	
µA7808UC	MC7808CT	
µA7808UV	MC7808BT	
µA7812CKC	MC7812CT	
µA7812UC	MC7812CT	
µA7812UV	MC7812BT	
µA7815CKC	MC7815CT	
µA7815UC	MC7815CT	
µA7815UV	MC7815BT	
µA7818CKC	MC7818CT	
µA7818UC	MC7818CT	
µA7818UV	MC7818BT	
µA7824CKC	MC7824CT	
µA7824UC	MC7824CT	
µA7824UV	MC7824BT	
µA78GU1C		LM317T
µA78GUC		LM317T
µA78L05ACLP	MC78L05ACP	
µA78L05AWC		MC78L05ACP
µA78L05CLP	MC78L05CP	
µA78L05WC		MC78L05CP
µA78L08ACLP	MC78L08ACP	
µA78L08AWC		MC78L08ACP
µA78L08CLP	MC78L08CP	
µA78L12ACLP	MC78L12ACP	
µA78L12AWC		MC78L12ACP
µA78L12CLP	MC78L12CP	
µA78L12WC		MC78L12CP
µA78L15ACLP	MC78L15ACP	
µA78L15AWC		MC78L15ACP
µA78L15CLP	MC78L15CP	
µA78L15WC		MC78L15CP

= Not recommended for new designs.

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
µA78L18AWC		MC78L18ACP
µA78L24AWC	MC78L24ACP	
µA78M05CKC	MC78M05CT	
µA78M05CKD		MC78M05CT
µA78M05UC	MC78M05CT	
µA78M06CKC	MC78M06CT	
µA78M06CKD		MC78M06CT
µA78M06UC	MC78M06CT	
µA78M08CKC	MC78M08CT	
µA78M08CKD		MC78M08CT
µA78M08UC	MC78M08CT	
µA78M12CKC	MC78M12CT	
µA78M12CKD		MC78M12CT
µA78M12UC	MC78M12CT	
µA78M15CKC	MC78M15CT	
µA78M15CKD		MC78M15CT
µA78M15UC	MC78M15CT	
µA78M18UC	MC78M18CT	
µA78M20CKC	MC78M20CT	
µA78M20CKD		MC78M20CT
µA78M20UC	MC78M20CT	
µA78M24CKC	MC78M24CT	
µA78M24CKD		MC78M24CT
µA78M24UC	MC78M24CT	
µA78MGT2C		LM317T
µA78MGU1C		LM317T
µA78MGUC		LM317MT
µA78S40PC	µA78S40PC	
µA78S40PV	µA78S40PV	
µA7905.2CKC	MC7905.2CT	
µA7905CKC	MC7905CT	
µA7905UC	MC7905CT	
µA7906CKC	MC7906CT	
µA7906UC	MC7906CT	
µA7908CKC	MC7908CT	
µA7912CKC	MC7912CT	
µA7912UC	MC7912CT	
µA7915CKC	MC7915CT	
µA7915UC	MC7915CT	
µA7918CKC	MC7918CT	
µA7918UC	MC7918CT	
µA7924CKC	MC7924CT	
µA7924UC	MC7924CT	
µA798TC	MC3458P1	
µA79L05AWC	MC79L05ACP	
µA79L05WC	MC79L05CP	
µA79L12AWC	MC79L12ACP	
µA79L12WC	MC79L12CP	
µA79L15AWC	MC79L15ACP	
µA79L15WC	MC79L15CP	
µA79M05AUC	MC79M05CT	
µA79M05CKC	MC79M05CT	

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
µA79M06AUC		MC79M06CT
µA79M06CKC		MC79M06CT
µA79M06UC		MC79M06CT
µA79M08AUC		MC79M08CT
µA79M08CKC		MC79M08CT
µA79M08UC		MC79M08CT
µA79M12AUC	MC79M12CT	
µA79M12CKC	MC79M12CT	
µA79M18AUC		MC79M18CT
µA79M18UC		MC79M18CT
µA79M24AUC		MC79M24CT
µA79M24CKC		MC79M24CT
µA79M24UC		MC79M24CT
µA9636ATC	MC3488AP1	
UAA1016B	UAA1016B	
UC2823DW		MC33023DW
UC2823N		MC33023P
UC2823Q		MC33023FN
UC2825DW		MC33025DW
UC2825N		MC33025P
UC2825Q		MC33025FN
UC2842AD	UC2842AD	
UC2842AN	UC2842AN	
UC2842BD	UC2842BD	
UC2842BN	UC2842BN	
UC2842D	UC2842AD	
UC2842N	UC2842AN	
UC2843AD	UC2843AD	
UC2843AN	UC2843AN	
UC2843BD	UC2843BD	
UC2843BN	UC2843BN	
UC2843D	UC2843AD	
UC2843N	UC2843AN	
UC2844BD	UC2844BD	
UC2844BN	UC2844BN	
UC2844D	UC2844D	
UC2844N	UC2844N	
UC2845BD	UC2845BD	
UC2845BN	UC2845BN	
UC2845D	UC2845D	
UC2845N	UC2845N	
UC317T	LM317T	
UC337T	LM337T	
UC3525AN	SG3525AN	
UC3526N	SG3526N	
UC3527AN	SG3527AN	
UC3823DW		MC34023DW
UC3823N		MC34023P
UC3823Q		MC34023FN
UC3825DW		MC34025DW
UC3825N		MC34025P
UC3825Q		MC34025FN

= Not recommended for new designs.

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
UC3842AD	UC3842AD	
UC3842AN	UC3842AN	
UC3842BD	UC3842BD	
UC3842BN	UC3842BN	
UC3842D	UC3842AD	
UC3842N	UC3842AN	
UC3843AD	UC3843AD	
UC3843AN	UC3843AN	
UC3843BD	UC3843BD	
UC3843BN	UC3843BN	
UC3843D	UC3843AD	
UC3843N	UC3843AN	
UC3844BD	UC3844BD	
UC3844BN	UC3844BN	
UC3844D	UC3844D	
UC3844N	UC3844N	
UC3845BD	UC3845BD	
UC3845BN	UC3845BN	
UC3845D	UC3845D	

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
UC3845N	UC3845N	
UC494ACN		TL594CN
UC494CN		TL494CN
UCN5816A	MC34142FN	
ULN2003A	MC1413	
ULN2004A	MC1416	
ULN2068BB	ULN2068B#	
ULN2068NE	ULN2068B#	
ULN2151H	MC1741CP1	
ULN2151M		MC1741CP1
ULN2803A	ULN2803A	
ULN2804A	ULN2804A	
ULN8126A	SG3526N	
ULS2151M		MC1741CP1
ULX8161M		MC34060AP
UPD6950C		MC10319P
UVC3101		MC10319P
XR082CP	TL082CP	
XR084CP	TL084CN	

= Not recommended for new designs.

Amplifiers and Comparators

In Brief . . .

For over two decades, Motorola has continually refined and updated integrated circuit technologies, analog circuit design techniques and processes in response to the needs of the marketplace. The enhanced performance of newer operational amplifiers and comparators has come through innovative application of these technologies, designs and processes. Some early designs are still available but are giving way to the new, higher performance operational amplifier and comparator circuits. Motorola has pioneered in JFET inputs, low temperature coefficient input stages, Miller loop compensation, all NPN output stages, dual–doublet frequency compensation and analog "in–the–package" trimming of resistors to produce superior high performance operational amplifiers and comparators, operating in many cases from a single supply with low input offset, low noise, low power, high output swing, high slew rate and high gain–bandwidth product at reasonable cost to the customer.

Present day operational amplifiers and comparators find applications in all market segments including motor controls, instrumentation, aerospace, automotive, telecommunications, medical, and consumer products.

Operational Amplifiers

2

Motorola offers a broad line of bipolar operational amplifiers to meet a wide range of applications. From low–cost industry–standard types to high precision circuits, the span encompasses a large range of performance capabilities. These Analog integrated circuits are available as single, dual and quad monolithic devices in a variety of temperature ranges and package styles. Most devices may be obtained in unencapsulated "chip" form as well. For price and delivery information on chips, please contact your Motorola Sales Representative or Distributor.

Table 1. Single Operational Amplifiers

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
Noncompensated											
Commercial Temperature Range (0°C to +70°C)											
LM301A	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	N/626, D/751
LM308A	7.0	0.5	5.0	1.0	80	1.0	0.3	±3.0	±18	Precision	N/626, D/751
Industrial Temperature Range (–25°C to +85°C)											
LM201A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	N/626, D/751
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF351	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626, D/751
LF411C	200 pA	2.0	10	100 pA	25	8.0	25	+5.0	±22	JFET Input, Low Offset, Low Drift	N/626, D/751
LF441C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power, JFET Input	N/626, D/751
LM11C	100 pA	0.6	2.0	10 pA	250	1.0	0.3	±3.0	±20	Precision	N/626
LM11CL	200 pA	5.0	3.0	25 pA	50	1.0	0.3	±3.0	±20	Precision	N/626
MC1436, C	0.04	10	12	10	70	1.0	2.0	±15	±34	High Voltage	P1/626, D/751
MC1741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	P1/626, D/751
MC1776C	0.003	6.0	15	3.0	100	1.0	0.2	±1.2	±18	μPower, Programmable	P1/626, D/751
MC3476	0.05	6.0	15	25	50	1.0	0.2	±1.5	±18	Low Cost, μPower, Programmable	P1/626
MC34001	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
MC34001B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, D/751
MC34071	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/626, D/751
MC34071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, D/751
MC34080B	200 pA	1.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626, D/751
MC34081B	200 pA	1.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, D/751
MC34181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/626
TL071AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, D/751
TL071C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, D/751
TL081AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, D/751
TL081C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
Automotive Temperature Range (–40°C to +85°C)											
MC33071	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/626, D/751
MC33071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, D/751
MC33171	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/626, D/751
MC33181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/626, D/751
Extended Automotive Temperature Range (–40°C to +105°C)											
MC33201	250 nA	9.0	2.0	100	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail	P/626, D/751
Military Temperature Range (–55°C to +125°C)											
MC33201	400 nA	9.0	2.0	200	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail	P/626, D/751

Table 2. Dual Operational Amplifiers

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF353	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626, D/751
LF412C	200 pA	3.0	10	100 pA	25	4.0	13	+5.0	±18	JFET Input, Low Offset, Low Drift	N/626, D/751
LF442C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power, JFET Input	N/626
LM358	0.25	6.0	7.0	50	25	1.0	0.6	±1.5 +3.0	±18 +36	Single Supply, Low Power Consumption	N/626, D/751
LM833	1.0	5.0	2.0	200	31.6	15	7.0	+2.5	±18	Low Noise, Audio	N/626, D/751
MC/MCT1458	0.5	6.0	10	200	20	1.1	0.8	±3.0	±18	Dual MC1741	P1/626, D/751
MC1458C	0.7	10	10	300	20	1.1	0.8	±3.0	±18	General Purpose	P1/626, D/751
MC3458	0.5	10	7.0	50	20	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies, Single Supply, Low Crossover Distortion	P1/626, D/751
MC4558AC	0.5	5.0	10	200	50	2.8	1.6	±3.0	±22	High Frequency	P1/626
MC/MCT4558C	0.5	6.0	10	200	20	2.8	1.6	±3.0	±18	High Frequency	P1/626, D/751
MC34002	100 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
MC34002B	100 pA	5.0	10	70 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
MC34072	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/626, D/751
MC34072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, D/751
MC34082	200 pA	3.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/626
MC34083B	200 pA	3.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626
MC34182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/626, D/751
TL062AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	P/626, D/751
TL062C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	P/626, D/751
TL072AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, D/751
TL072C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, D/751
TL082AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, D/751
TL082C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
Industrial Temperature Range (−25°C to +85°C)											
LM258	0.15	5.0	10	30	50	1.0	0.6	±1.5 +3.0	±18 +36	Split or Single Supply Op Amp	N/626, D/751
Automotive Temperature Range (−40°C to +85°C)											
MC3358	5.0	8.0	10	75	20	1.0	0.6	±1.5 +3.0	±18 +36	Split or Single Supply	P1/626
MC33072	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/626, D/751
MC33072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, D/751
MC33076	0.5	4.0	2.0	70	25	7.4	2.6	±2.0	±18	High Output Current	P1/626, P2/648C, D/751
MC33077	1.0	1.0	2.0	180	150	37	11	±2.5	±18	Low Noise	P/626, D/751
MC33078	750 nA	2.0	2.0	150	31.6	16	7.0	±5.0	±18	Low Noise	N/626, D/751
MC33102											P/626, D/751
(Awake)	600 nA	3.0	1.0	60	25	4.6	1.7	±2.5	±18	Sleep–Mode™	
(Sleep)	60 nA	3.0	1.0	6.0	15	0.3	0.1	±2.5	±18	Micropower	
MC33172	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/626, D/751
MC33178	0.5	3.0	2.0	50	50	5.0	2.0	±2.0	±18	High Output Current	P/626, D/751
MC33182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/626, D/751
MC33272A	650 nA	1.0	0.56	25 nA	31.6	5.5	11.5	±1.5	±18	High Performance	P/626, D/751
MC33282	100 pA	200 μV	5.0	50 pA	50	30	12	±2.5	±18	Low Input, Offset JFET	P/626, D/751
TL062V	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	P/626, D/751

Table 2. Dual Operational Amplifiers (continued)

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{VOL} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
Extended Automotive Temperature Range (−40°C to +105°C)											
MC33202 MC33206	250 nA	11	2.0	100	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail Rail–to–Rail with Enable	P/626, D/751 P/646, D/751A
LM2904	0.25	10	7.0	50	100 typ	1.0	0.6	±1.5 +3.0	±13 +26	Split or Single Supply	N/626, D/751
Extended Automotive Temperature Range (−40°C to +125°C)											
TCA0372	500 nA	15	20	50	30	1.1	1.4	+5.0	+36	Power Op Amp, Single Supply	DP2/648, DW/751G
LM2904V	0.25	13	7.0	50	100 typ	1.0	0.6	±1.5 +3.0	±13 +26	Split or Single Supply	N/626, D/751
Military Temperature Range (−55°C to +125°C)											
MC33202	400 pA	11	2.0	200 pA	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail	P/626, D/751

Table 3. Quad Operational Amplifiers

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{VOL} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF347	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/646
LF347B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	N/646
LF444C	100 pA	10	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power, JFET Input	N/646, D/751A
LM324, A	0.25	6.0	7.0	50	25	1.0	0.6	±1.5 +3.0	±16 +32	Low Power Consumption	N/646, D/751A
LM348 LM3900	0.2	6.0	–	50	25	1.0	0.5	±3.0 +3.0	±18 +36	Quad MC1741	D/751A
MC3403	0.5	10	7.0	50	20	1.0	0.6	±1.5 +3.0	±18 +36	No Crossover Distortion	P/646, D/751A
MC4741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	Quad MC1741	P/646, D/751A
MC34004	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	P/646
MC34004B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/646
MC34074	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/646, D/751A
MC34074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/646, D/751A
MC34084	200 pA	12	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/646, DW/751G
MC34085B	200 pA	12	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/646, DW/751G
MC34184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/646, D/751A
TL064AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	N/646, D/751A
TL064C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	N/646, D/751A
TL074AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	N/646
TL074C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	N/646
TL084AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	N/646
TL084C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	N/646
Industrial Temperature Range (−25°C to +85°C)											
LM224, A	0.15	5.0	7.0	30	50	1.0	0.6	±1.5 +3.0	±16 +32	Split Supplies or Single Supply	N/646, D/751A
Automotive Temperature Range (−40°C to +85°C)											
MC3301/ LM2900	0.3	–	–	–	1.0	4.0	0.6	±2.0 +4.0	±15 +28	Norton Input	P/646 N/646
MC3303	0.5	8.0	10	75	20	1.0	0.6	±1.5 +3.0	±18 +36	Differential General Purpose	P/646, D/751A

Table 3. Quad Operational Amplifiers (continued)

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
MC33074	0.5	4.5	10	75	25	4.5	10	+3.0	+44	High Performance, Single Supply	P/646, D/751A
MC33074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	High Performance	P/646, D/751A
MC33079	750 nA	2.5	2.0	150	31.6	9.0	7.0	±5.0	±18	Low Noise	N/646, D/751A
MC33174	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/646, D/751A
MC33179	0.5	3.0	2.0	50	50	5.0	2.0	±2.0	±18	High Output Current	P/646, D/751A
MC33184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/646, D/751A
MC33274A	650 nA	1.0	0.56	25 nA	31.6	5.5	11.5	±1.5	±18	High Performance	P/646, D/751A
MC33284	100 pA	2.0	5.0	50 pA	50	30	12	±2.5	±18	Low Input, Offset JFET	P/646, D/751A
TL064V	200 pA	9.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	N/646, D/751A
Extended Automotive Temperature Range (−40°C to +105°C)											
MC33204	250 nA	13	2.0	100	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail	P/646, D/751A
MC33207					50	2.2		±0.9	±6.0	Rail–to–Rail with Enable	P/648, D/751B
MC33304					25	3.0		+1.8	+12	Sleepmode, Rail–to–Rail	P/646, D/751A
LM2902	0.5	10	–	50	15	1.0	0.6	±1.5 +3.0	±13 +26	Differential Low Power	N/646, D/751A
Extended Automotive Temperature Range (−40°C to +125°C)											
LM2902V	0.5	13	–	50	15	1.0	0.6	±1.5 +3.0	±13 +26	Differential Low Power	N/646, D/751A
Military Temperature Range (−55°C to +125°C)											
MC33204	400 pA	13	2.0	200 pA	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail	P/646, D/751A

High Frequency Amplifiers

A variety of high frequency circuits with features ranging from low cost simplicity to multifunction versatility marks Motorola's line of integrated amplifiers. Devices described here are intended for industrial and communications applications. For devices especially dedicated to consumer products, i.e., TV and entertainment radio. (See the Consumer Electronics Circuits section.)

AGC Amplifiers

MC1490/MC1350 Family Wideband General Purpose Amplifiers

The MC1490 and MC1350 family are basic building blocks – AGC (Automatic Gain Controlled) RF/Video Amplifiers. These parts are recommended for applications up through 70 MHz. The best high frequency performance may be obtained by using the physically smaller SOIC version (shorter leads) – MC1350D. There are currently no other RF ICs like these, because other manufacturers have dropped their copies. Applications include variable gain video and instrumentation amplifiers, IF (Intermediate Frequency) amplifiers for radio and TV receivers, and transmitter power output control. Many uses will be found in medical instrumentation, remote monitoring, video/graphics processing, and a variety of communications equipment. The family of parts using the same basic die (identical circuit with slightly different test parameters) is listed in the following table.

Table 4. High Frequency Amplifier Specifications

Operating Temperature Range		A_V (dB)	Bandwidth @ MHz	V_{CC}/V_{EE} (Vdc)		Suffix/ Package
−40° to +85°C	0° to +70°C	Typical		Minimum	Maximum	
–	MC1350	50	45	+6.0	+18	P/626, D/751
MC1490	–	50 45 35	10 60 100			P/626

Miscellaneous Amplifiers

2

Motorola provides several Bipolar and CMOS special purpose amplifiers which fill specific needs. These devices range from low power CMOS programmable amplifiers and comparators to variable–gain bipolar power amplifiers.

MC3405
Dual Operational Amplifier and Dual Voltage Comparator

This device contains two Differential Input Operational Amplifiers and two Comparators; each set capable of single supply operation. This operational amplifier–comparator circuit will find its applications as a general purpose product for automotive circuits and as an industrial "building block."

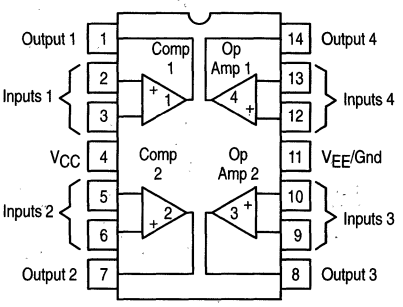


Table 5. Bipolar

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (nA) Max	A_{vol} (V/mV) Min	Response (μs) Typ	Supply Voltage		Suffix/ Package
						Single	Dual	
MC3405	0.5	10	50	20	1.3	3.0 to 36	±1.5 to ±18	P/646

MC14573
Quad Programmable Operational Amplifier

MC14575
Dual Programmable Operational Amplifier and Dual Programmable Comparator

MC14576B/MC14577B
Dual Video Amplifiers

Table 6. CMOS

Function	Quantity Per Package	Single Supply Voltage Range	Dual Supply Voltage Range	Frequency Range	Device	Suffix/ Package
Operational Amplifiers	4	3.0 to 15 V	±1.5 to ±7.5 V	DC to 1.0 MHz	MC14573	P/648, D/751B
Operational Amplifiers and Comparators	2 and 2	3.0 to 15 V	±1.5 to ±7.5 V	DC to 1.0 MHz	MC14575	P/648, D/751B
Video Amplifiers	2	5.0 to 12 V(1)	±2.5 to ±6.0 V(2)	Up to 10 MHz	MC14576C MC14577C	P/626, F/904

(1) 5.0 to 10 V for surface mount package.
(2) ±2.5 to ±5.0 V for surface mount package.

Comparators

Table 7. Single Comparators

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (μA) Max	A_V (V/V) Typ	I_O (mA) Min	Response Time (ns)	Supply Voltage (V)	Description	Temperature Range (°C)	Suffix/ Package
Bipolar										
LM211	0.1	3.0	0.01	200 k	8.0	200	+15, –15	With strobe, will operate from single supply	–25 to +85	D/751
LM311	0.25	7.5	0.05						0 to +70	N/626, D/751
CMOS										
MC14578	1.0 pA	50	–	–	1.1	–	3.5 to 14	Requires only 10 μA from single–ended supply	–30 to +70	P/648, D/751B

Table 8. Dual Comparators

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (μA) Max	A_V (V/V) Typ	I_O (mA) Min	Response Time (ns)	Supply Voltage (V)	Description	Temperature Range (°C)	Suffix/ Package
Bipolar										
LM293	0.25	5.0	0.05	200 k	6.0	1300	±1.5 to ±18	Designed for single or split	–25 to +85	N/626,
LM393		5.0				1300	or	supply operation, input	0 to +70	D/751
LM393A		2.0				1300	3.0 to 36	common mode includes	0 to +70	
LM2903		7.0				1500		ground (negative supply)	–40 to +105	
LM2903V		7.0				1500			–40 to +125	
MC3405	0.5	10	0.05	200 k	6.0	1300	±1.5 to ±7.5 or 3.0 to 15	This device contains 2 op amps and 2 comparators in a single package	0 to +70	P/646
CMOS										
MC14575	0.001	30	0.0001	2.0 k	3.0	1000	±1.5 to ±7.5 or 3.0 to 15	This device contains 2 op amps and 2 comparators in a single package	–40 to +85	P/648, D/751B

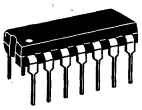
Table 9. Quad Comparators

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (μA) Max	A_V (V/V) Typ	I_O (mA) Min	Response Time (ns)	Supply Voltage (V)	Description	Temperature Range (°C)	Suffix/ Package
Bipolar										
LM239	0.25	5.0	0.05	200 k	6.0	1300	±1.5 to ±18	Designed for single or split	–25 to +85	N/646,
LM239A		2.0		200 k			or	supply operation, input	–25 to +85	D/751A
LM339		5.0		200 k			3.0 to 36	common mode includes	0 to +70	
LM339A		2.0		200 k				ground (negative supply)	0 to +70	
LM2901		7.0		100 k					–40 to +85	
LM2901V		7.0		100 k					–40 to +125	
MC3302	0.5	20	0.5	100 k					–40 to +85	P/646
MC3431	40	10	1.0 Typ	1.2 k	16	33	+5.0, –5.0	High speed comparator/ sense amplifier	0 to +70	P/648
MC3432		6.0				40				
MC3433		10				40				
CMOS										
MC14574	0.001	30	0.0001	2.0 k	3.0	1000	±1.5 to ±7.5 or 3.0 to 15	Externally programmable power dissipation with 1 or 2 resistors	–40 to +85	P/648, D/751B

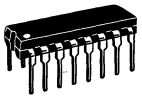
Amplifiers and Comparators Package Overview

2

CASE 626
N, P, P1 SUFFIX



CASE 646
N, P SUFFIX



CASE 648, 648C
DP2, P, P2 SUFFIX

CASE 751
D SUFFIX

CASE 751A
D SUFFIX

CASE 751B
D SUFFIX

CASE 751G
DW SUFFIX

CASE 904
F SUFFIX

Device Listing and Related Literature

Amplifiers

Amplifiers

Comparators

ADDENDUM

RELATED APPLICATION NOTES

App Note	Title	Related Device
AN587	Analysis and Design of the Op Amp Current Source	**MC1741C**

LF347, B
LF351
LF353

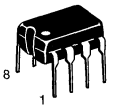
JFET Input Operational Amplifiers

These low cost JFET input operational amplifiers combine two state–of–the–art analog technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The JFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin–compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices.

- Input Offset Voltage of 5.0 mV Max (LF347B)
- Low Input Bias Current: 50 pA
- Low Input Noise Voltage: 16 nV/$\sqrt{Hz}$
- Wide Gain Bandwidth: 4.0 MHz
- High Slew Rate: 13V/μs
- Low Supply Current: 1.8 mA per Amplifier
- High Input Impedance: 10^{12} Ω
- High Common Mode and Supply Voltage Rejection Ratios: 100 dB

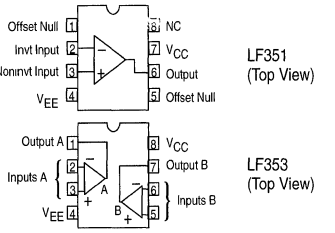
FAMILY OF JFET OPERATIONAL AMPLIFIERS

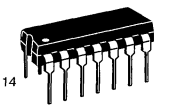


N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

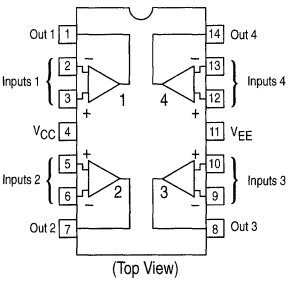
PIN CONNECTIONS





N SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+18 −18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Power Dissipation at T_A = +25°C Derate above T_A =+25°C	P_D $1/\theta_{JA}$	900 10	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J	115	°C
Storage Temperature Range	T_{stg}	− 65 to +150	°C

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is limited to the negative power supply.
2. Any amplifier output can be shorted to ground indefinitely. However, if more than one amplifier output is shorted simultaneously, maximum junction temperature rating may be exceeded.

ORDERING INFORMATION

Device	Function	Operating Temperature Range	Package
LF351D LF351N	Single Single	T_A = 0° to +70°C	SO–8 Plastic DIP
LF353D LF353N	Dual Dual		SO–8 Plastic DIP
LF347BN LF347N	Quad Quad		Plastic DIP Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	LF347B			LF347, LF351, LF353			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ k, V_{CM} = 0) T_A = +25°C 0°C ≤ T_A ≤ +70°C	V_{IO}	 – –	 1.0 –	 5.0 8.0	 – –	 5.0 –	 10 13	mV
Avg. Temperature Coefficient of Input Offset Voltage $R_S \le 10$ k, 0°C ≤ T_A ≤ +70°C	$\Delta V_{IO}/\Delta T$	 –	 10	 –	 –	 10	 –	µV/°C
Input Offset Current (V_{CM} = 0, Note 3) T_A = +25°C 0°C ≤ T_A ≤ +70°C	I_{IO}	 – –	 25 –	 100 4.0	 – –	 25 –	 100 4.0	 pA nA
Input Bias Current (V_{CM} = 0, Note 3) T_A = +25°C 0°C ≤ T_A ≤ +70°C	I_{IB}	 – –	 50 –	 200 8.0	 – –	 50 –	 200 8.0	 pA nA
Input Resistance	r_i	–	10^{12}	–	–	10^{12}	–	Ω
Common Mode Input Voltage Range	V_{ICR}	±11	+15 –12	–	±11	+15 –12	–	V
Large–Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k) T_A = +25°C 0°C ≤ T_A ≤ +70°C	A_{VOL}	 50 25	 100 –	 – –	 25 15	 100 –	 – –	V/mV
Output Voltage Swing (R_L = 10 k)	V_O	±12	±14	–	±12	±14	–	V
Common Mode Rejection ($R_S \le 10$ k)	CMR	80	100	–	70	100	–	dB
Supply Voltage Rejection ($R_S \le 10$ k)	PSRR	80	100	–	70	100	–	dB
Supply Current LF347 LF351 LF353	I_D	 – – –	 7.2 – –	 11 – –	 – – –	 7.2 1.8 3.6	 11 3.4 6.5	mA
Short Circuit Current	I_{SC}	–	25	–	–	25	–	mA
Slew Rate (A_V = +1)	SR	–	13	–	–	13	–	V/µs
Gain–Bandwidth Product	BWp	–	4.0	–	–	4.0	–	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1000 Hz)	e_n	–	24	–	–	24	–	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1000 Hz)	i_n	–	0.01	–	–	0.01	–	$pA/\sqrt{Hz}$
Channel Separation (LF347, LF353) 1.0 Hz ≤ f ≤ 20 kHz (Input Referred)	–	–	–120	–	–	–120	–	dB

For Typical Characteristic Performance Curves, refer to MC34001, 34002, 34004 data sheet.

NOTE: 3. Input bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature. To maintain junction temperatures as close to ambient as is possible, pulse techniques are utilized during test.

LF411C
LF412C

Low Offset, Low Drift JFET Input Operational Amplifiers

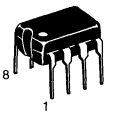
SINGLE/DUAL JFET OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

Through innovative design concepts and precision matching this monolithic high speed JFET input operational amplifier family offers very low input offset voltage as well as low temperature coefficient of input offset voltage. The amplifier requires less than 3.4 mA per amplifier of supply current yet exhibits greater than 2.7 MHz of gain bandwidth product and more than 8.0 V/μs slew rate. Through the use of JFET inputs the amplifier has very low input bias currents and low input offset currents. The amplifier utilizes industry standard pinouts which afford the user the opportunity to directly upgrade circuit performance without the need for redesign.

The LF411C and LF412C are available in the industry standard plastic 8–pin DIP and SO–8 surface mount packages, and specified over the commercial temperature range.

- Low Input Offset Voltage: 2.0 mV Max (Single)
  3.0 mV Max (Dual)
- Low T.C. of Input Offset Voltage: 10 μV/°C
- Low Input Offset Current: 20 pA
- Low Input Bias Current: 60 pA
- Low Input Noise Voltage: 18 nV/$\sqrt{Hz}$
- Low Input Noise Current: 0.01 pA/$\sqrt{Hz}$
- Low Total Harmonic Distortion: 0.05%
- Low Supply Current: 2.5 mA
- High Input Resistance: 10^{12} Ω
- Wide Gain Bandwidth: 8.0 MHz
- High Slew Rate: 25 V/μs (Typ)
- Fast Settling Time: 1.6 μs (to within 0.01%)
- Internally Compensated

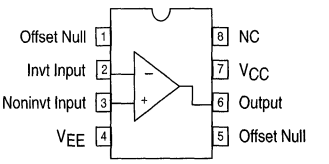


N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

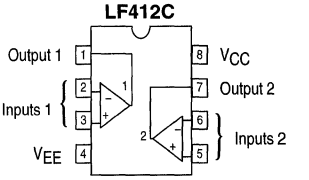
PIN CONNECTIONS

LF411C



(Single, Top View)

LF412C



(Dual, Top View)

ORDERING INFORMATION

Device	Function	Operating Temperature Range	Package
LF411CD	Single	T_A = 0° to +70°C	SO–8
LF411CN			Plastic DIP
LF412CD	Dual		SO–8
LF412CN			Plastic DIP

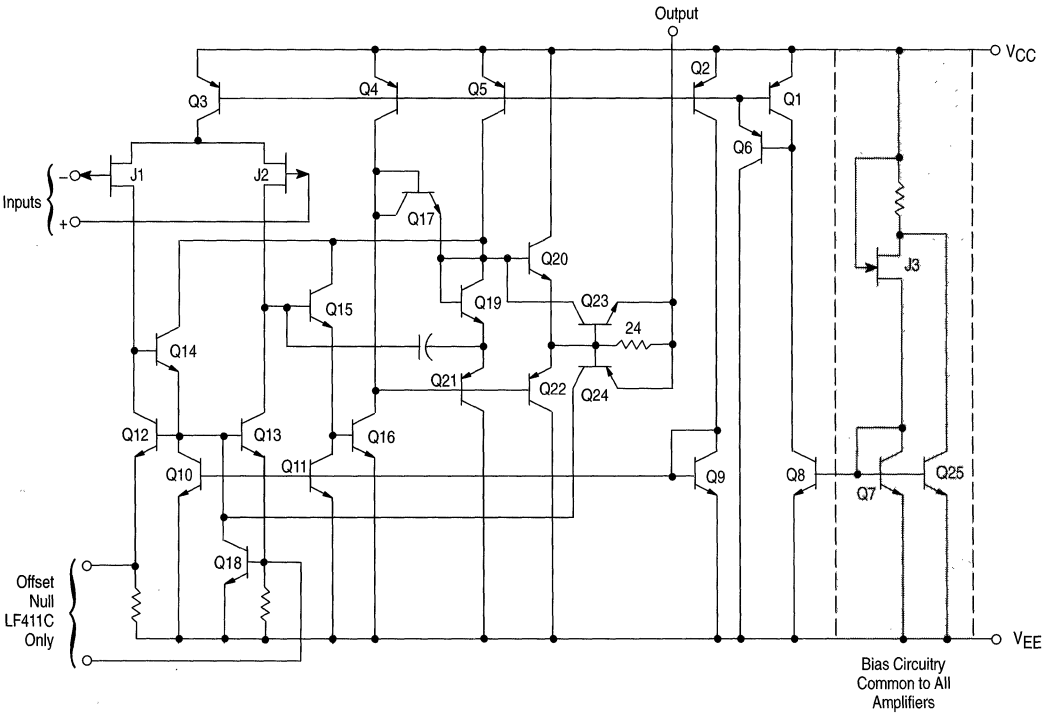
2

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply Voltages		V_{CC}, $\|V_{EE}\|$	+18	V
Input Differential Voltage Range (Note 1)		V_{IDR}	±30	V
Input Voltage Range (Note 1)		V_{IR}	±15	V
Output Short Circuit Duration (Note 2)		t_{SC}	Indefinite	sec
Maximum Junction Temperature		T_J	+150	°C
Operating Ambient Temperature Range		T_A	0 to 70	°C
Thermal Resistance (Junction–to–Ambient)	LF411CN/412CN LF411CD/412CD	$R\theta_{JA}$	100 180	°C/W
Storage Temperature		T_{stg}	–60 to +150	°C
Maximum Power Dissipation		P_D	(Note 2)	mW

NOTES: 1. Input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

Representative Schematic Diagram
(Each Amplifier)



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 0° to 70°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 k Ω, V_{CM} = 0 V, V_O = 0 V)	$\lvert V_{IO}\rvert$				mV
LF411		–	0.5	2.0	
LF412		–	1.0	3.0	
Average Temperature Coefficient of Input Offset Voltage (R_S = 10 k Ω, V_{CM} = 0 V, V_O = 0 V)	$\Delta V_{IO}\,\Delta T$	–	10	–	μV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				
LF411 T_A = 25°C		–	20	100	pA
T_A = 0° to 70°C		–	–	2.0	nA
LF412 T_A = 25°C		–	25	100	pA
T_A = 0° to 70°C		–	–	2.0	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				
LF411 T_A = 25°C		–	0.6	200	pA
T_A = 0° to 70°C		–	–	4.0	nA
LF412 T_A = 25°C		–	0.5	200	pA
T_A = 0° to 70°C		–	–	4.0	nA
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k Ω)	A_{VOL}				V/mV
LF411 T_A = 25°C		25	80	–	
T_A = 0° to 70°C		15	–	–	
LF412 T_A = 25°C		25	150	–	
T_A = 0° to 70°C		15	–	–	
Output Voltage Swing (V_{ID} = ±1.0 V, R_L = 10 kΩ)					V
LF411	V_O +	+12	+13.9	–	
	V_O −	–	−14.7	−12	
LF412	V_O +	+12	+14.0	–	
	V_O −	–	−14.0	−12	
Common Mode Input Voltage Range (V_O = 0 V)	V_{ICR}				V
LF411		+11	+14	−11	
		–	−14	–	
LF412		+11	+15	−11	
		–	−12	–	
Common Mode Rejection (V_{CM} = ±11 V, R_S ≤ 10 k Ω)	CMR				dB
LF411		70	90	–	
LF412		70	100	–	
Power Supply Rejection (Note 3) (V_{CC} V_{EE} = +15 V, −15 V to +5.0 V, −5.0 V)	PSR				dB
LF411		70	86	–	
LF412		70	100	–	
Power Supply Current (V_O = 0 V)	I_D				mA
LF411		–	2.5	3.4	
LF412		–	2.8	6.8	

NOTE: 3. Measured with V_{CC} and V_{EE} simultaneously varied.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 k Ω, A_V = +1.0)	SR				V/μs
LF411		8.0	25	–	
LF412		8.0	13	–	
Gain Bandwidth Product	GBW				MHz
LF411		2.7	8.0	–	
LF412		2.7	4.0	–	
Channel Separation (f = 1.0 Hz to 20 kHz, LF412)	CS	–	−120	–	dB
Differential Input Resistance (V_{CM} = 0 V)	R_{in}	–	10^{12}	–	kΩ
Equivalent Input Voltage Noise (R_S = 100 Ω, f = 1.0 kHz)	e_n				nV/√Hz
LF411		–	30	–	
LF412		–	25	–	
Equivalent Input Noise Current (f = 1.0 kHz)	i_n				pA/√Hz
LF411		–	0.01	–	
LF412		–	0.01	–	

LF441C
LF442C
LF444C

LOW POWER JFET INPUT OPERATIONAL AMPLIFIERS

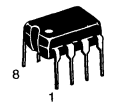
SEMICONDUCTOR TECHNICAL DATA

Low Power JFET Input Operational Amplifiers

These JFET input operational amplifiers are designed for low power applications. They feature high input impedance, low input bias current and low input offset current. Advanced design techniques allow for higher slew rates, gain bandwidth products and output swing. The LF441C device provides for the external null adjustment of input offset voltage.

These devices are specified over the commercial temperature range. All are available in plastic dual in–line and SOIC packages.

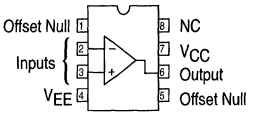
- Low Supply Current: 200 μA/Amplifier
- Low Input Bias Current: 5.0 pA
- High Gain Bandwidth: 2.0 MHz
- High Slew Rate: 6.0 V/μs
- High Input Impedance: 10^{12} Ω
- Large Output Voltage Swing: ±14 V
- Output Short Circuit Protection



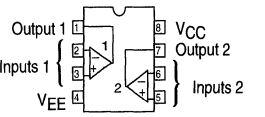
N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

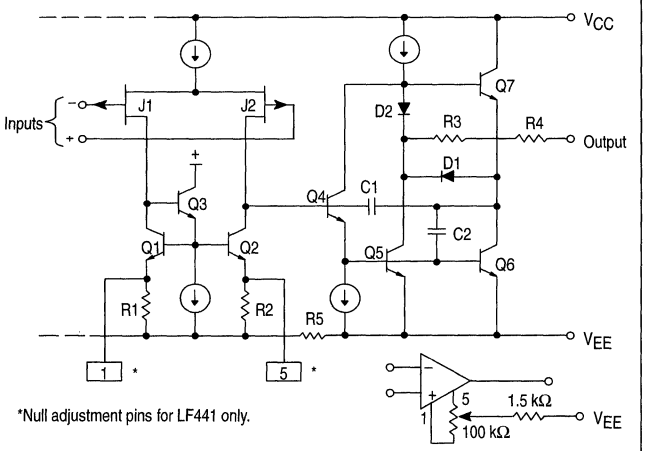


(Single, Top View)



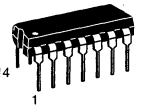
(Dual, Top View)

Representative Schematic Diagram
(Each Amplifier)

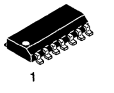


*Null adjustment pins for LF441 only.

LF441C input offset voltage null adjust circuit

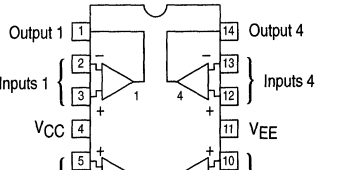


N SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Quad, Top View)

ORDERING INFORMATION

Device	Function	Operating Temperature Range	Package
LF441CD LF441CN	Single	T_A = 0° to +70°C	SO–8 Plastic DIP
LF442CD LF442CN	Dual		SO–8 Plastic DIP
LF444CD LF444CN	Quad		SO–14 Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	±30	V
Input Voltage Range (Notes 1 and 2)	V_{IR}	±15	V
Output Short Circuit Duration (Note 3)	t_{SC}	Indefinite	sec
Operating Junction Temperature (Note 3)	T_J	+150	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C

NOTES: 1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. The magnitude of the input voltage must never exceed the magnitude of the supply or 15 V, whichever is less.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 0° to 70°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 kΩ, V_O = 0 V)	V_{IO}				mV
Single: T_A = +25°C		–	3.0	5.0	
T_A = 0° to +70°C		–	–	7.5	
Dual: T_A = +25°C		–	3.0	5.0	
T_A = 0° to +70°C		–	–	7.5	
Quad: T_A = +25°C		–	3.0	10	
T_A = 0° to +70°C		–	–	12	
Average Temperature Coefficient of Offset Voltage (R_S = 10 kΩ, V_O = 0 V)	$\Delta V_{IO}/\Delta T$	–	10	–	µV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				
T_A = +25°C		–	0.5	50	pA
T_A = 0° to +70°C		–	–	1.5	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				
T_A = +25°C		–	3.0	100	pA
T_A = 0° to +70°C		–	–	3.0	nA
Common Mode Input Voltage Range (T_A = +25°C)	V_{ICR}	– –11	+14.5 –12	+11 –	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 10 kΩ)	A_{VOL}				V/mV
T_A = +25°C		25	60	–	
T_A = 0° to +70°C		15	–	–	
Output Voltage Swing (R_L = 10 kΩ)	V_O + V_O –	+12 –	+14 –14	– –12	V
Common Mode Rejection (R_S ≤ 10 kΩ, V_{CM} = V_{ICR}, V_O = 0 V)	CMR	70	86	–	dB
Power Supply Rejection (R_S = 100 Ω, V_{CM} = 0 V, V_O = 0 V)	PSR	70	84	–	dB
Power Supply Current (No Load, V_O = 0 V)	I_D				µA
Single		–	200	250	
Dual		–	400	500	
Quad		–	800	1000	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 kΩ, C_L = 10 pF, A_V = +1.0)	SR	0.6	6.0	–	V/ μs
Settling Time To within 10 mV (A_V = −1.0, R_L = 10 kΩ, V_O = 0 V to +10 V) To within 1.0 mV	t_s	– –	1.6 2.2	– –	μs
Gain Bandwidth Product (f = 200 kHz)	GBW	0.6	2.0	–	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n	–	47	–	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz)	i_n	–	0.01	–	pA/√Hz
Input Resistance	R_i	–	10^{12}	–	Ω
Channel Separation (f = 1.0 Hz to 20 kHz)	CS	–	120	–	dB

Figure 1. Maximum Power Dissipation versus Temperature for Package Variations

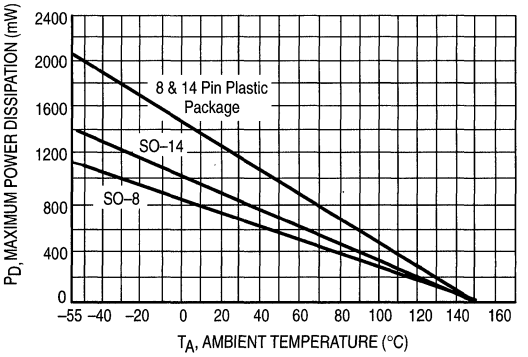


Figure 2. Input Bias Current versus Input Common Mode Voltage

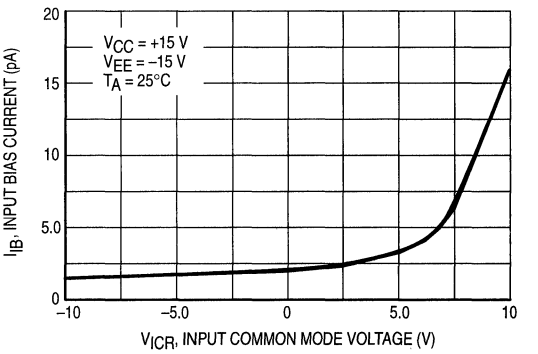


Figure 3. Input Bias Current versus Temperature

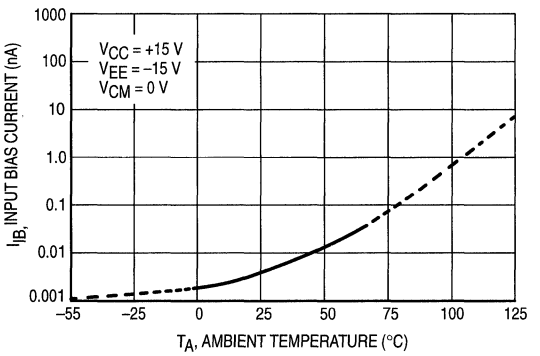
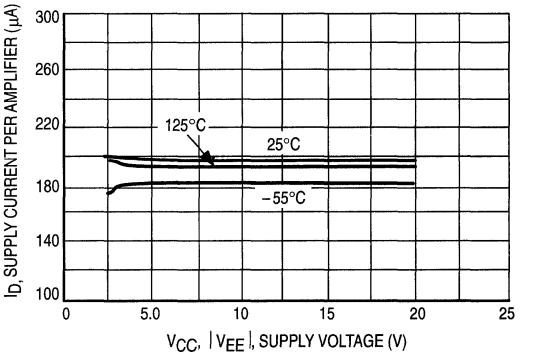


Figure 4. Supply Current versus Supply Voltage



2

Figure 5. Positive Input Common Mode Voltage Range versus Positive Supply Voltage

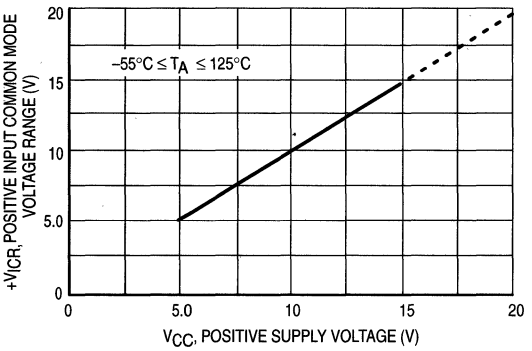


Figure 6. Negative Input Common Mode Voltage Range versus Negative Supply Voltage

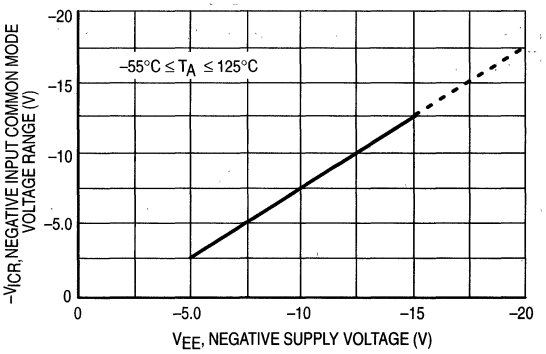


Figure 7. Output Voltage versus Output Source Current

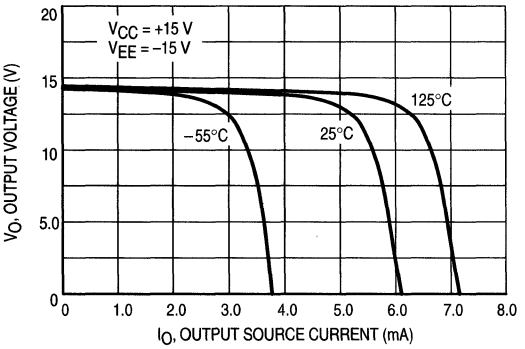


Figure 8. Output Voltage versus Output Sink Current

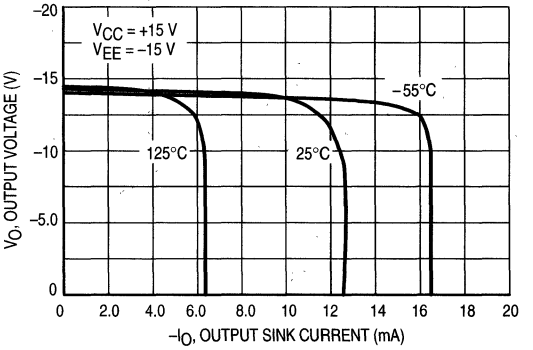


Figure 9. Output Voltage Swing versus Supply Voltage

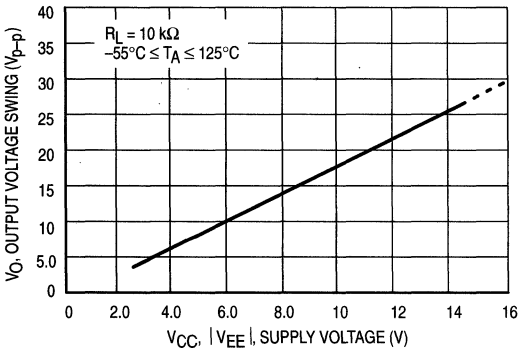


Figure 10. Output Voltage Swing versus Load Resistance

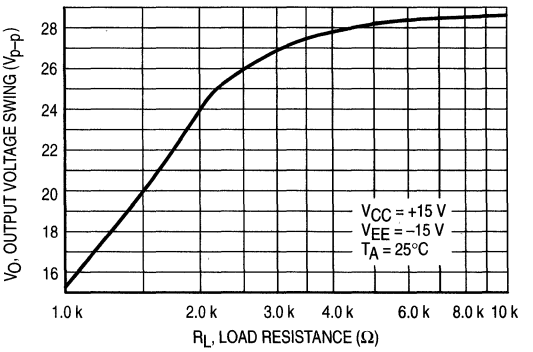


Figure 11. Normalized Gain Bandwidth Product versus Temperature

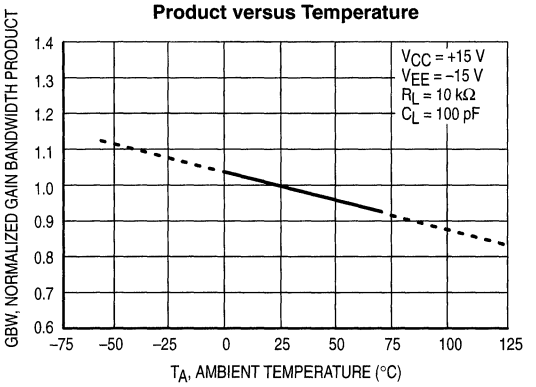


Figure 12. Open Loop Voltage Gain and Phase versus Frequency

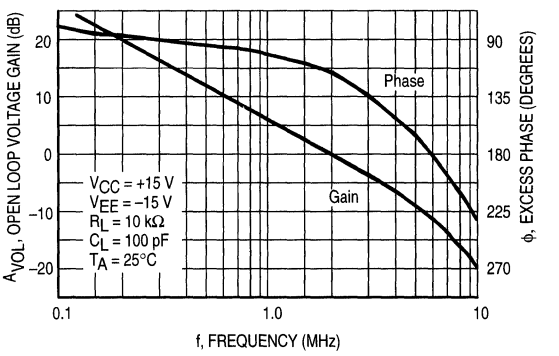


Figure 13. Slew Rate versus Temperature

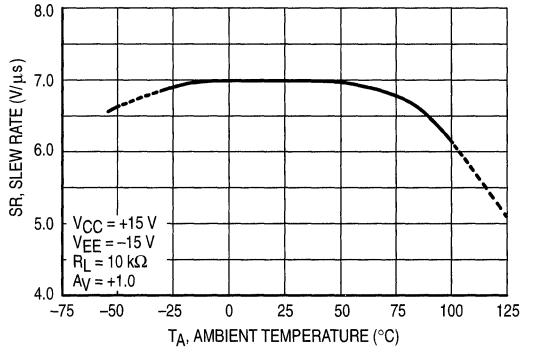


Figure 14. Total Output Distortion versus Frequency

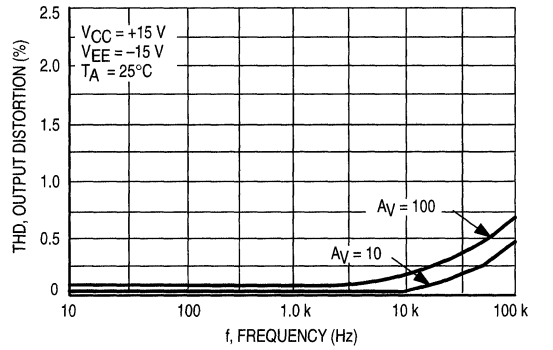


Figure 15. Output Voltage Swing versus Frequency

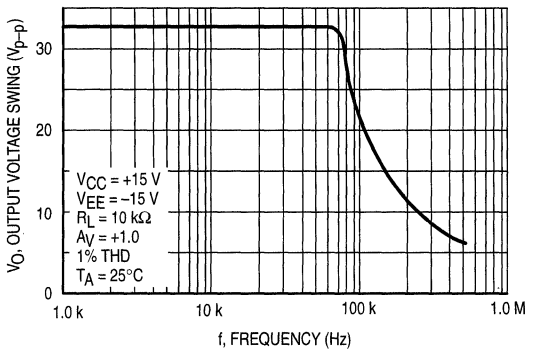
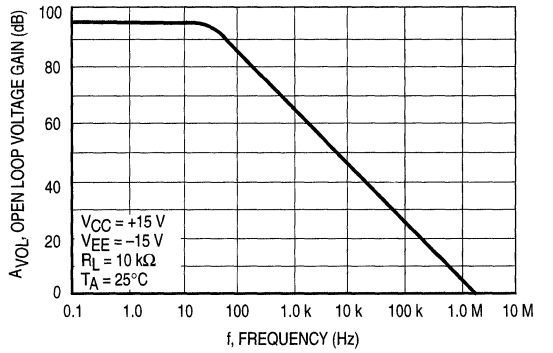


Figure 16. Open Loop Voltage Gain versus Frequency



2

Figure 17. Common Mode Rejection versus Frequency

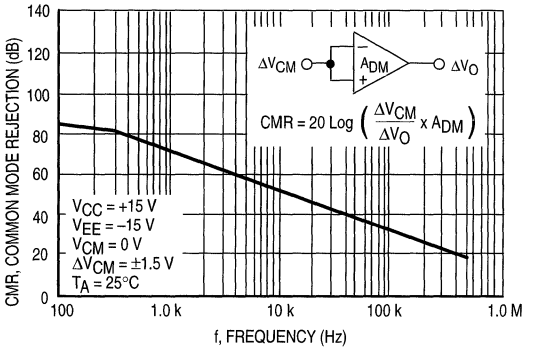


Figure 18. Power Supply Rejection versus Frequency

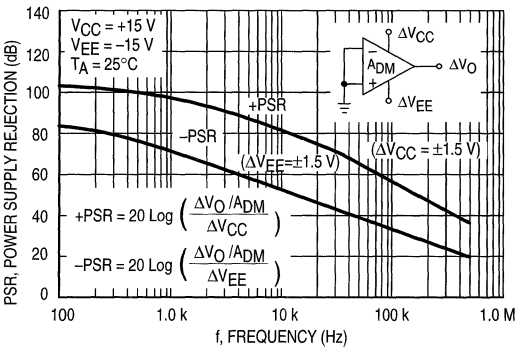


Figure 19. Input Noise Voltage versus Frequency

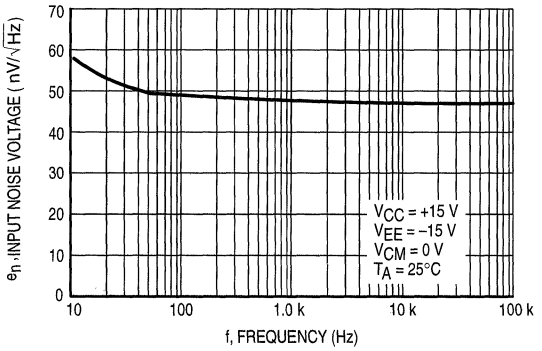


Figure 20. Open Loop Voltage Gain versus Supply Voltage

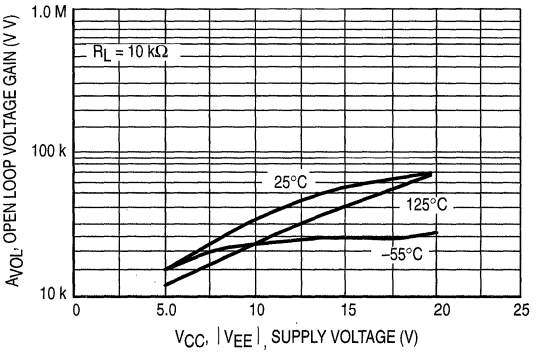


Figure 21. Output Impedance versus Frequency

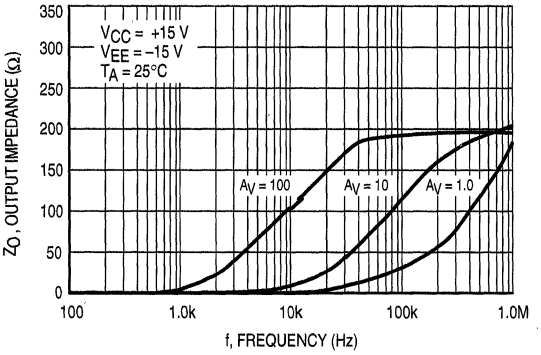
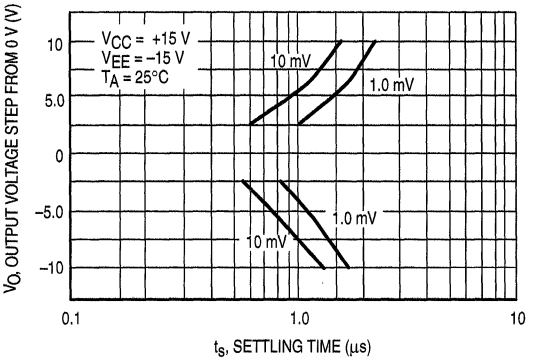


Figure 22. Inverter Settling Time



SMALL SIGNAL RESPONSE

Figure 23. Inverting

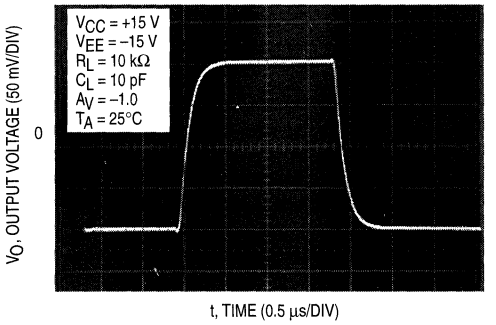
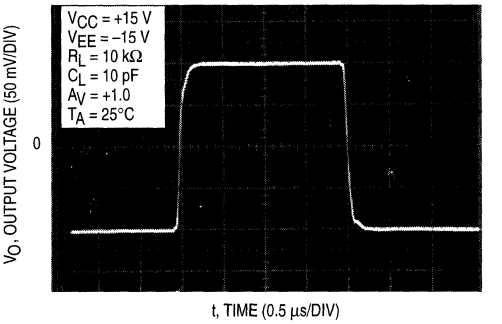


Figure 24. Noninverting



LARGE SIGNAL RESPONSE

Figure 25. Inverting

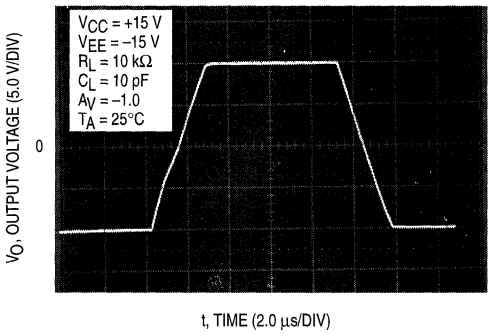
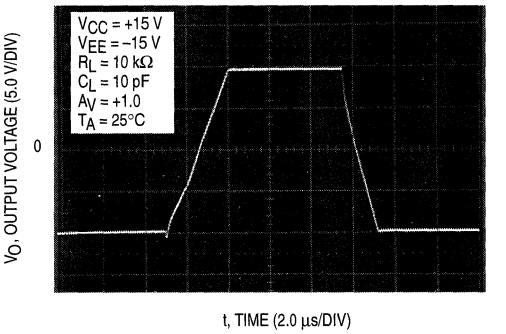


Figure 26. Noninverting



LM11C, CL

Precision Operational Amplifiers

PRECISION OPERATIONAL AMPLIFIERS

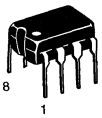
SEMICONDUCTOR TECHNICAL DATA

The LM11C is a precision, low drift operational amplifier providing the best features of existing FET and Bipolar op amps. Implementation of super gain transistors allows reduction of input bias currents by an order of magnitude over earlier devices such as the LM308A. Offset voltage and drift have also been reduced. Although bandwidth and slew rate are not as great as FET devices, input offset voltage, drift and bias current are inherently lower, particularly over temperature. Power consumption is also much lower, eliminating warm–up stabilization time in critical applications.

Offset balancing is provided, with the range determined by an external low resistance potentiometer. Compensation is provided internally, but external compensation can be added for improved stability when driving capacitive loads.

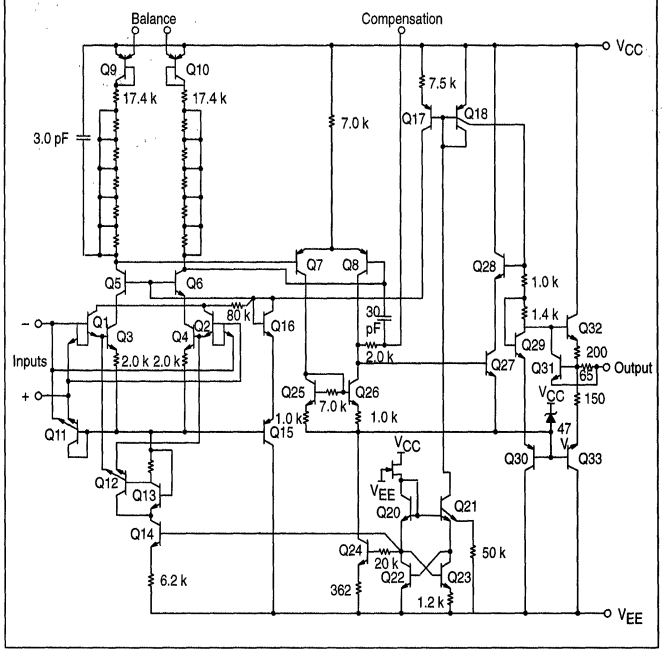
The precision characteristics of the LM11C make this device ideal for applications such as charge integrators, analog memories, electrometers, active filters, light meters and logarithmic amplifiers.

- Low Input Offset Voltage: 100 μV
- Low Input Bias Current: 17 pA
- Low Input Offset Current: 0.5 pA
- Low Input Offset Voltage Drift: 1.0 μV/°C
- Long–Term Stability: 10 μV/year
- High Common Mode Rejection: 130 dB

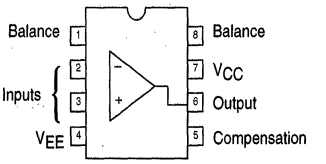


N SUFFIX
PLASTIC PACKAGE
CASE 626

Representative Schematic Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM11CN,CLN	T_A = 0° to +70°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} to V_{EE}	40	Vdc
Differential Input Current (Note 1)	I_{ID}	±10	mA
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	
Power Dissipation (Note 3)	P_D	500	mW
Operating Junction Temperature	T_J	85	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted [Note 4].)

Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	–	0.2	0.6	–	0.5	5.0	mV
T_{low} to T_{high}		–	–	0.8	–	–	6.0	
Input Offset Current	I_{IO}	–	1.0	10	–	4.0	25	pA
T_{low} to T_{high}		–	–	20	–	–	50	
Input Bias Current	I_{IB}	–	17	100	–	17	200	pA
T_{low} to T_{high}		–	–	150	–	–	300	
Input Resistance	r_i	–	10^{11}	–	–	10^{11}	–	Ω
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	–	2.0	5.0	–	3.0	–	µV/°C
T_{low} to T_{high}								
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$	–	10	–	–	50	–	fA/°C
T_{low} to T_{high}								
Input Bias Current Drift	$\Delta I_{IB}/\Delta T$	–	0.8	3.0	–	1.4	–	pA/°C
T_{low} to T_{high}								
Large Signal Voltage Gain	A_{VOL}							V/mV
V_S = ±15 V, V_{out} = ±12 V, I_{out} = ±2.0 mA		100	300	–	25	300	–	
T_{low} to T_{high} (Note 5)		50	–	–	15	–	–	
V_S = ±15 V, V_{out} = ±12 V, I_{out} = ±0.5 mA		250	1200	–	50	800	–	
T_{low} to T_{high}		100	–	–	30	–	–	
Common Mode Rejection	CMR							dB
V_S = ±15 V, –13 V ≤ V_{CM} ≤ 14 V		110	130	–	96	110	–	
V_S = ±15 V, –12.5 V ≤ V_{CM} ≤ 14 V, T_{low} to T_{high}		100	–	–	90	–	–	
Power Supply Rejection	PSR							dB
±2.5 V ≤ V_S ≤ ±20 V		100	118	–	84	100	–	
T_{low} to T_{high}		96	–	–	80	–	–	
Power Supply Current	I_D	–	0.3	0.8	–	0.3	0.8	mA
T_{low} to T_{high}		–	–	1.0	–	–	1.0	
Output Short Circuit Current	I_{SC}	–	±10	–	–	±10	–	mA
T_J = 150°C, Output Shorted to Ground								

NOTES: 1. The inputs are shunted by back–to–back diodes for over–voltage protection. Excessive current will flow if the input differential voltage is in excess of 1.0 V if no limiting resistance is used. Additionally, a 2.0 kΩ resistance in each input is suggested to prevent possible latch–up initiated by supply reversals.

2. The output is current limited when shorted to ground or any voltages less than the supplies. Continuous overloads will require package dissipation to be considered and heatsinking should be provided when necessary.

3. Devices must be derated based on package thermal resistance (see package outline dimensions).

4. These specifications apply for V_{EE} +2.0 V ≤ V_{CM} ≤ V_{CC} –1.0 V (V_{EE} +2.5 V ≤ V_{CM} ≤ V_{CC} –1.0 V for T_{low} to T_{high}) and ±2.5 V ≤ V_S ≤ ±20 V T_{low} to T_{high}: 0°C ≤ T_J ≤ +70°C for LM11C and LM11C.

5. V_{out} = ±11.5 V, all other conditions unchanged.

2

Figure 1. Input Bias Current versus Case Temperature

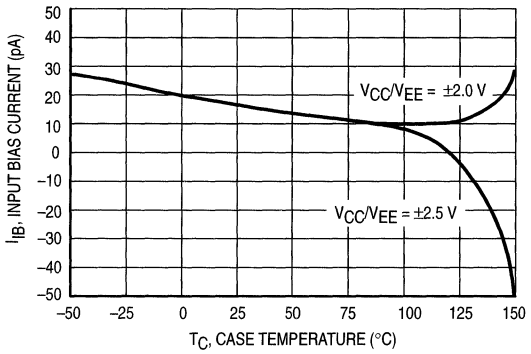


Figure 2. Input Offset Current versus Case Temperature

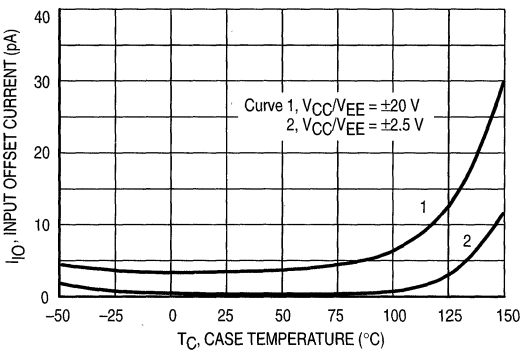


Figure 3. Temperature Coefficient of Input Offset Voltage versus Input Offset Voltage

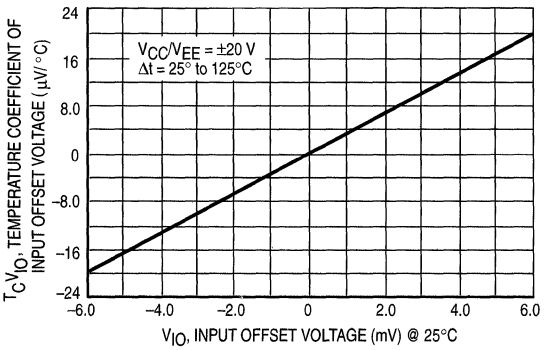


Figure 4. Spectral Noise Density

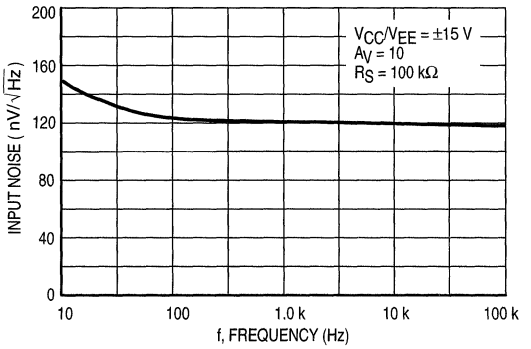


Figure 5. Common Mode Limits versus Temperature

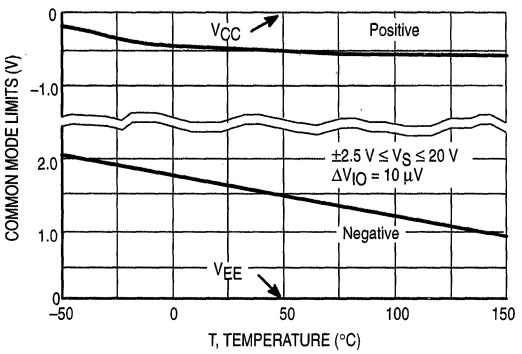


Figure 6. Common Mode Rejection and Slew Limit versus Frequency

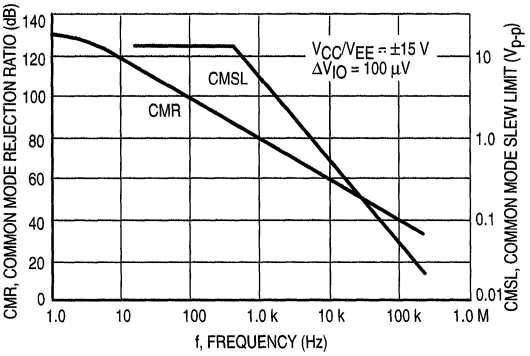


Figure 7. Open Loop Voltage Gain versus Supply Voltage

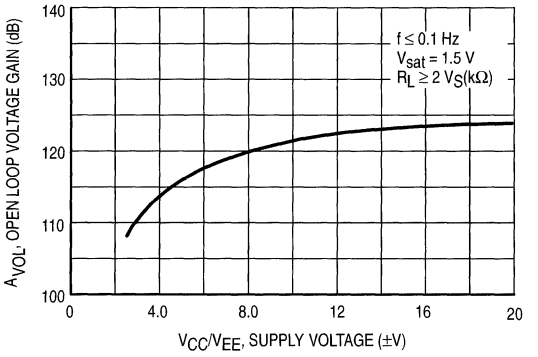


Figure 8. Output Saturation versus Load Current

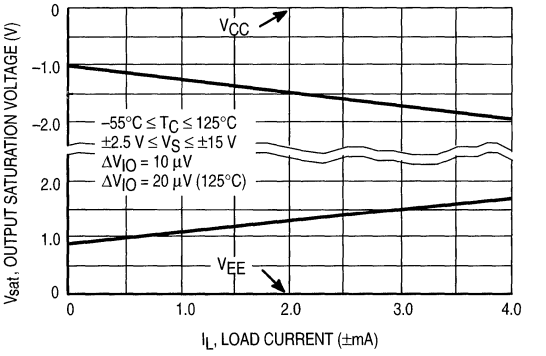


Figure 9. Power Supply Rejection Ratio versus Frequency

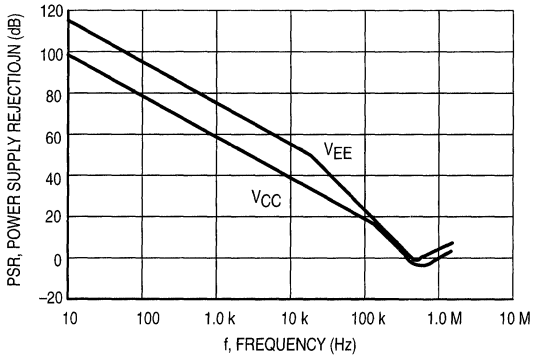


Figure 10. Supply Current versus Supply Voltage

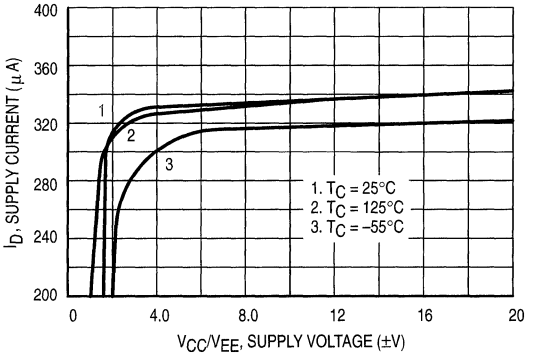


Figure 11. Open Loop Voltage Gain and Phase versus Frequency

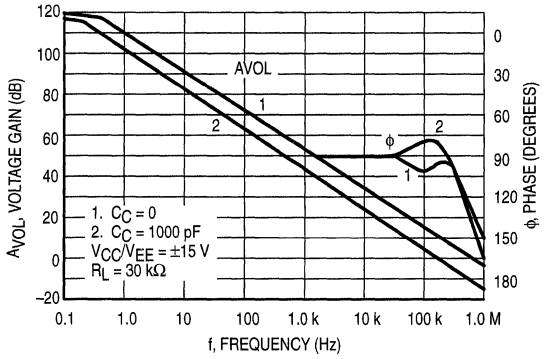
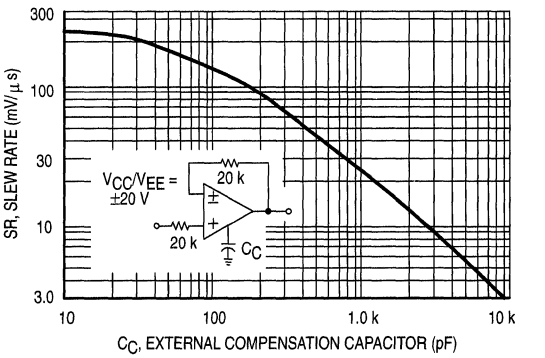
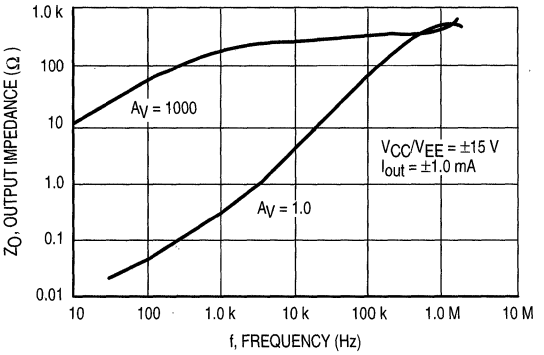


Figure 12. Slew Rate versus External Compensation Capacitor



2

Figure 13. Closed Loop Output Impedance versus Frequency



APPLICATIONS INFORMATION

Due to the extremely low input bias currents of this device, it may be tempting to remove the bias current compensation resistor normally associated with a summing amplifier configuration. Direct connection of the inputs to a low impedance source or ground should be avoided when supply voltages greater than approximately 3.0 V are used. The potential problem involves reversal of one supply which can cause excessive current to flow in the second supply. Possible destruction of the IC could result if the second supply is not current limited to approximately 100 mA or if bypass capacitors greater than 1.0 μF are used in the supply bus.

Disconnecting one supply will generally cause reversal due to loading of the other supply within the IC and in external circuitry. Although the problem can usually be avoided by placing clamp diodes across the power supplies of each printed circuit board, a careful design will include sufficient resistance in the input leads to limit the current to 10 mA if the input leads are pulled to either supply by internal currents. This precaution is not limited only to the LM11C.

The LM11C is capable of resolving picoampere level signals. Leakage currents external to the IC can severely impair the performance of the device. It is important that high quality insulating materials such as teflon be employed. Proper cleaning to remove fluxes and other residues from printed circuit boards, sockets and the device package are necessary to minimize surface leakage.

When operating in high humidity environments or temperatures near 0°C, a surface coating is suggested to set up a moisture barrier.

Leakage effects on printed circuit boards can be reduced by encircling the inputs (both sides of pc board) with a conductive guard ring connected to a low impedance potential nearly the same as that of the inputs.

Guard ring electrical connections for common operational amplifier configurations are illustrated in Figure 14. Electrostatic shielding is suggested in high impedance circuits.

Error voltages in external circuitry can be generated by thermocouple effects. Dissimilar metals along with temperature gradients can set up an error voltage ranging in the hundreds of microvolts. Some of the best thermocouples are junctions of dissimilar metals made up of IC package pins and printed circuit boards. Problems can be avoided by keeping low level circuitry away from heat generating elements.

The LM11C is internally compensated, but external compensation can be added to improve stability, particularly when driving capacitive loads.

Figure 14. Guard Ring Electrical Connections for Common Amplifier Configurations

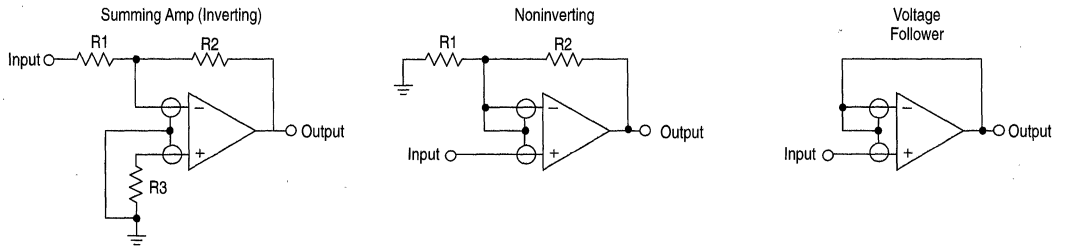
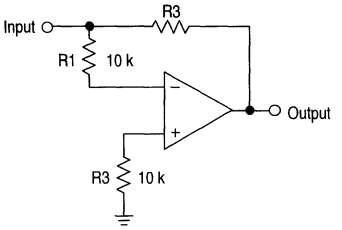
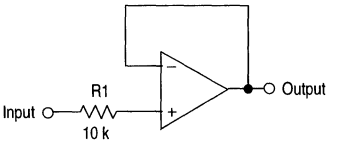


Figure 15. Input Protection for Summing (Inverting) Amplifier



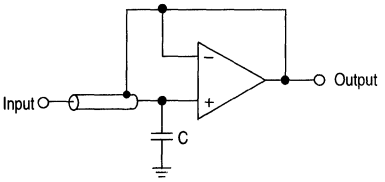
Current is limited by R1 in the event the input is connected to a low impedance source outside the common mode range of the device. Current is controlled by R2 if one supply reverses. R1 and R2 do not affect normal operation.

Figure 16. Input Protection for a Voltage Follower

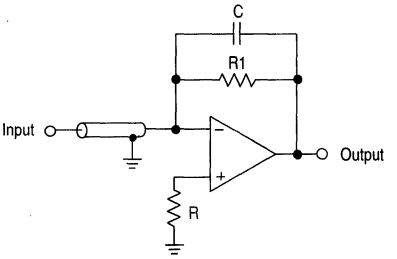


Input current is limited by R1 when the input exceeds supply voltage, power supply is turned off, or output is shorted.

Figure 17. Cable Bootstrapping and Input Shields

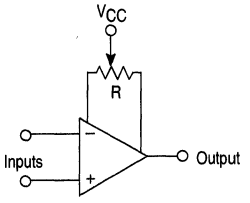


An input shield bootstrapped in a voltage follower reduces input capacitance, leakage, and spurious voltages from cable flexing. A small capacitor from the input to ground will prevent any instability.



In a summing amplifier the input is at virtual ground. Therefore the shield can be grounded. A small feedback capacitor will insure stability.

Figure 18. Adjusting Input Offset Voltage with Balance Potentiometer



Minimum Adjustment Range (mV)	R (Ω)
±0.4	1.0 k
±1.0	3.0 k
±2.0	10 k
±5.0	100 k

Input offset voltage adjustment range is a function of the Balance Potentiometer Resistance as indicated by the table above. The potentiometer is connected between the two "Balance" pins.

LM301A
LM201A

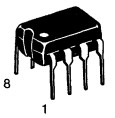
OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

Operational Amplifiers

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation, summing amplifier slew rates to 10 V/μs can be obtained.

- Low Input Offset Current: 20 nA Maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short Circuit Protection
- Guaranteed Drift Characteristics



N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Figure 1. Standard Compensation and Offset Balancing Circuit

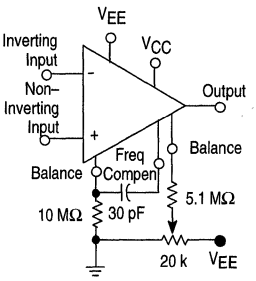
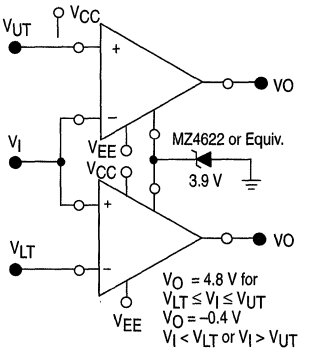
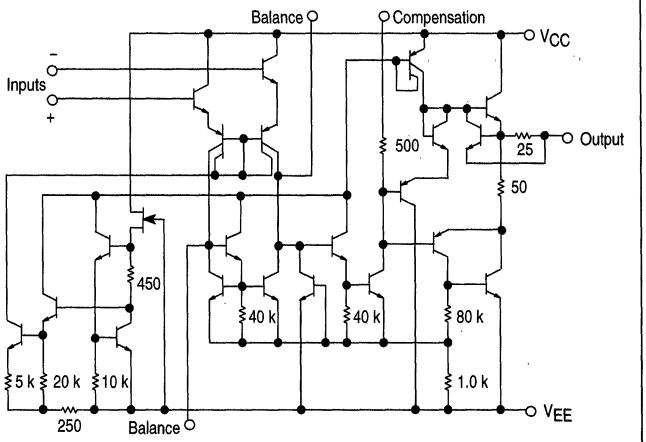


Figure 2. Double-Ended Limit Detector

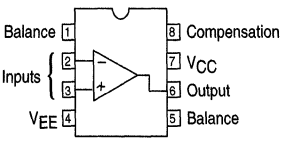


(Pins Not Shown Are Not Connected)

Figure 3. Representative Circuit Schematic



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM301AD LM301AN	T_A = 0° to +70°C	SO–8 Plastic DIP
LM201AD LM201AN	T_A = –25° to +85°C	SO–8 Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		LM201A	LM301A	
Power Supply Voltage	V_{CC}, V_{EE}	±22	±18	Vdc
Input Differential Voltage	V_{ID}	±30		V
Input Common Mode Range (Note 1)	V_{ICR}	±15		V
Output Short Circuit Duration	t_{SC}	Continuous		
Power Dissipation (Package Limitation) Plastic Dual-In-Line Package (LM201A/ Derate above T_A = +25°C 301A)	P_D	 625 5.0	 625 5.0	 mW mW/°C
Operating Ambient Temperature Range	T_A	–25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150		°C

NOTE: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the LM201A, and from ±5.0 V to ±15 V for the LM301A.

Characteristic	Symbol	LM201A			LM301A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 50 kΩ)	V_{IO}	–	0.7	2.0	–	2.0	7.5	mV
Input Offset Current	I_{IO}	–	1.5	10	–	3.0	50	nA
Input Bias Current	I_{IB}	–	30	75	–	70	250	nA
Input Resistance	r_i	1.5	4.0	–	0.5	2.0	–	MΩ
Supply Current V_{CC}/V_{EE} = ±20 V V_{CC}/V_{EE} = ±15 V	I_{CC},I_{EE}	 – –	 1.8 –	 3.0 –	 – –	 – 1.8	 – 3.0	mA
Large Signal Voltage Gain (V_{CC}/V_{EE} = ±15 V, V_O = ±10 V, R_L > 2.0 kΩ)	A_V	50	160	–	25	160	–	V/mV
The following specifications apply over the operating temperature range.								
Input Offset Voltage (R_S ≤ 50 kΩ)	V_{IO}	–	–	3.0	–	–	10	mV
Input Offset Current	I_{IO}	–	–	20	–	–	70	nA
Avg Temperature Coefficient of Input Offset Voltage T_A(min) ≤ T_A ≤ T_A (max)	$\Delta V_{IO}/\Delta T$	–	3.0	15	–	6.0	30	μV/°C
Avg Temperature Coefficient of Input Offset Current +25°C ≤ T_A ≤ T_A (max) T_A(min) ≤ T_A ≤ 25°C	$\Delta I_{IO}/\Delta T$	 – –	 0.01 0.02	 0.1 0.2	 – –	 0.01 0.02	 0.3 0.6	nA/°C
Input Bias Current	I_{IB}	–	–	100	–	–	300	nA
Large Signal Voltage Gain (V_{CC}/V_{EE} = ±15 V, V_O = ±10V, R_L > 2.0 kΩ)	A_{VOL}	25	–	–	15	–	–	V/mV
Input Voltage Range V_{CC}/V_{EE} = ±20 V V_{CC}/V_{EE} = ±15 V	V_{ICR}	 –15 –	 – –	 +15 –	 – –12	 – –	 – +12	V
Common Mode Rejection (R_S ≤ 50 kΩ)	CMR	80	96	–	70	90	–	dB
Supply Voltage Rejection (R_S ≤ 50 kΩ)	PSR	80	96	–	70	96	–	dB
Output Voltage Swing (V_{CC}/V_{EE} = ±15 V, R_L = ±10 kΩ, R_L > 2.0 kΩ)	V_O	±12 ±10	±14 ±13	– –	±12 ±10	±14 ±13	– –	V
Supply Currents (T_A = T_A(max), V_{CC}/V_{EE} = ±20 V)	I_{CC},I_{EE}	–	1.2	2.5	–	–	–	mA

2

Figure 4. Minimum Input Voltage Range

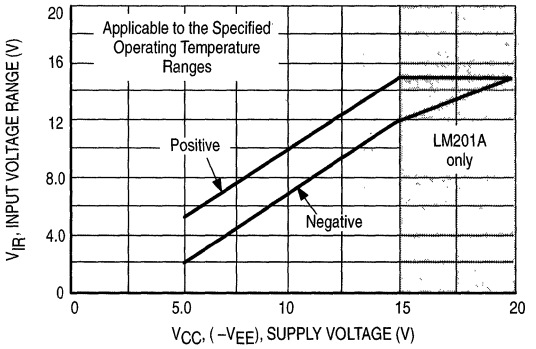


Figure 5. Minimum Output Voltage Swing

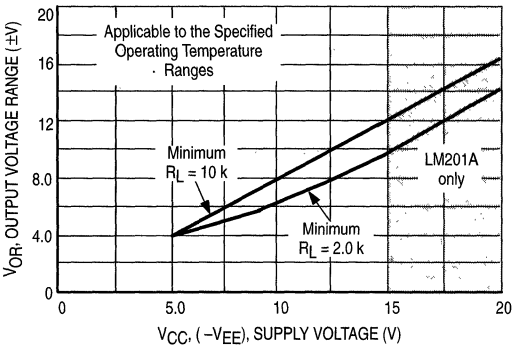


Figure 6. Minimum Voltage Gain

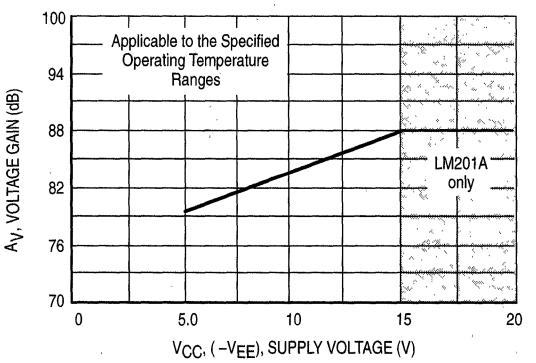


Figure 7. Typical Supply Currents

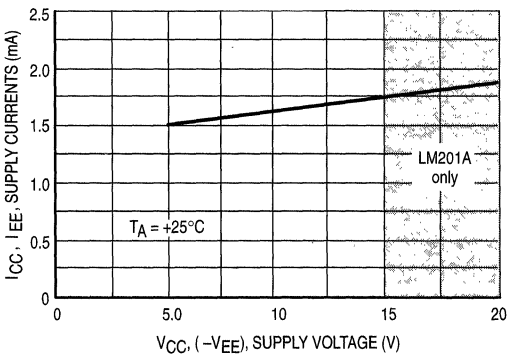


Figure 8. Open Loop Frequency Response

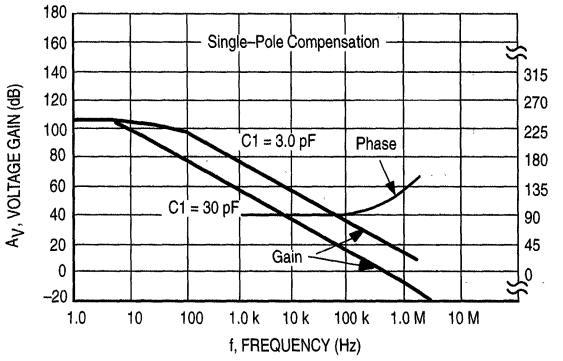


Figure 9. Large Signal Frequency Response

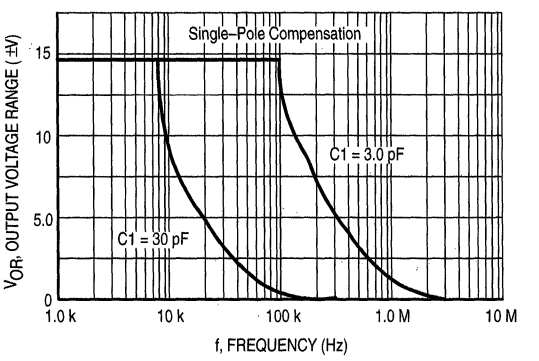


Figure 10. Voltage Follower Pulse Response

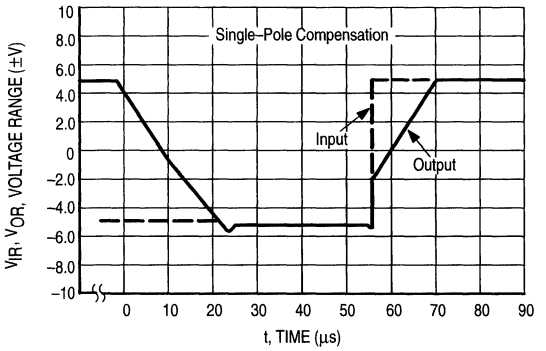


Figure 11. Open Loop Frequency Response

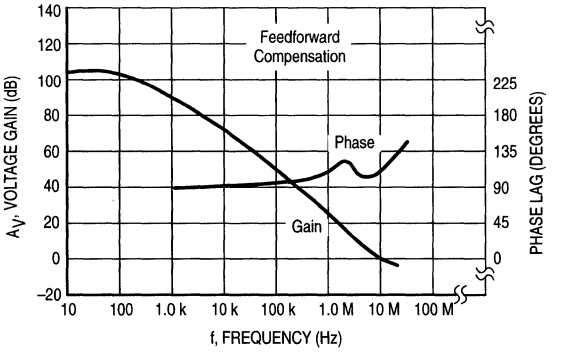


Figure 12. Large Signal Frequency Response

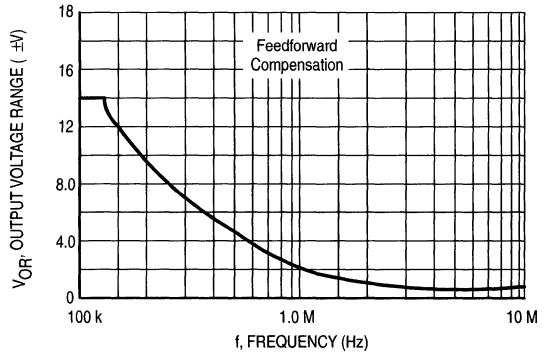


Figure 13. Inverter Pulse Response

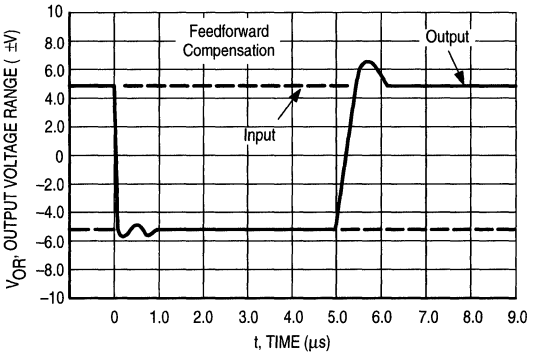


Figure 14. Single–Pole Compensation

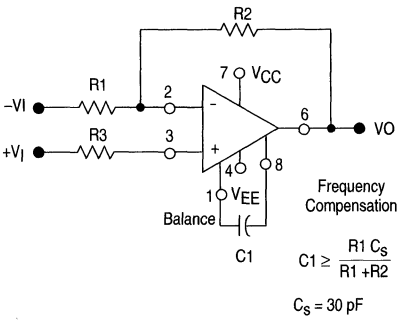
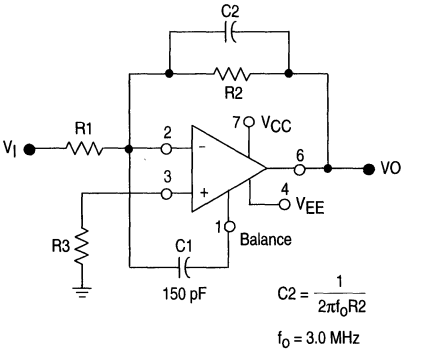


Figure 15. Feedforward Compensation



LM308A

Precision Operational Amplifier

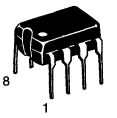
SUPER GAIN OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

The LM308A operational amplifier provides high input impedance, low input offset and temperature drift, and low noise. These characteristics are made possible by use of a special Super Beta processing technology. This amplifier is particularly useful for applications where high accuracy and low drift performance are essential. In addition high speed performance may be improved by employing feedforward compensation techniques to maximize slew rate without compromising other performance criteria.

The LM308A offers extremely low input offset voltage and drift specifications allowing usage in even the most critical applications without external offset nulling.

- Operation from a Wide Range of Power Supply Voltages
- Low Input Bias and Offset Currents
- Low Input Offset Voltage and Guaranteed Offset Voltage Drift Performance
- High Input Impedance

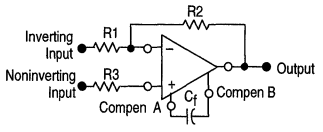


N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

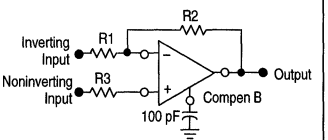
Frequency Compensation

Standard Compensation

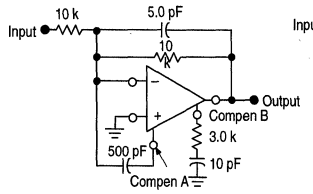


$$C_f \geq 30 \left(\frac{1}{1 + \frac{R2}{R1}}\right)$$

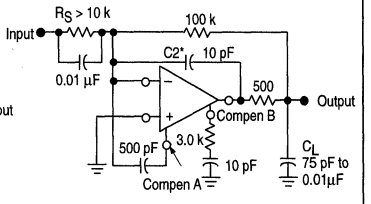
Modified Compensation



Standard Feedforward Compensation

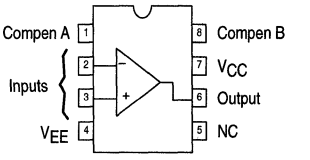


Feedforward Compensations for Decoupling Load Capacitance



$$*C2 > \frac{5 \times 10^5}{R2}\ pF$$

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM308AN LM308AD	T_A = 0° to +70°C	Plastic DIP SO–8

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±18	Vdc
Input Voltage (See Note 1)	V_I	±15	V
Input Differential Current (See Note 2)	I_{ID}	±10	mA
Output Short Circuit Duration	t_{SC}	Indefinite	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	+150	°C

NOTES: 1. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
2. The inputs are shunted with back–to–back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs, unless some limiting resistance is used.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted these specifications apply for supply voltages of +5.0 V ≤ V_{CC} ≤ +15 V and –5.0 V ≥ V_{EE} ≥ –15 V, T_A = +25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	–	0.3	0.5	mV
Input Offset Current	I_{IO}	–	0.2	1.0	nA
Input Bias Current	I_{IB}	–	1.5	7.0	nA
Input Resistance	r_i	10	40	–	MΩ
Power Supply Currents (V_{CC} = +15 V, V_{EE} = –15 V)	I_{CC}, I_{EE}	–	±0.3	±0.8	mA
Large Signal Voltage Gain (V_{CC} = +15 V, V_{EE} = –15 V, V_O = ±10 V, R_L ≥ 10 kΩ)	A_{VOL}	80	300	–	V/mV
The following specifications apply over the operating temperature range.					
Input Offset Voltage	V_{IO}	–	–	0.73	mV
Input Offset Current	I_{IO}	–	–	1.5	nA
Average Temperature Coefficient of Input Offset Voltage T_A (min) ≤ T_A ≤ T_A (max)	$\Delta V_{IO}/\Delta T$	–	1.0	5.0	µV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	–	2.0	10	pA/°C
Input Bias Current	I_{IB}	–	–	10	nA
Large Signal Voltage Gain (V_{CC} +15 V, V_{EE} = –15 V, V_O = ±10 V, R_L ≥ 10 kΩ)	A_{VOL}	60	–	–	V/mV
Input Voltage Range (V_{CC} = +15 V, V_{EE} = –15 V)	V_{ICR}	±14	–	–	V
Common Mode Rejection (R_S ≤ 50 kΩ)	CMR	96	110	–	dB
Supply Voltage Rejection (R_S ≤ 50 kΩ)	PSR	96	110	–	dB
Output Voltage Range (V_{CC} = +15 V, V_{EE} = –15 V, R_L = 10 kΩ)	V_{OR}	±13	±14	–	V

2

Figure 1. Input Bias and Input Offset Currents

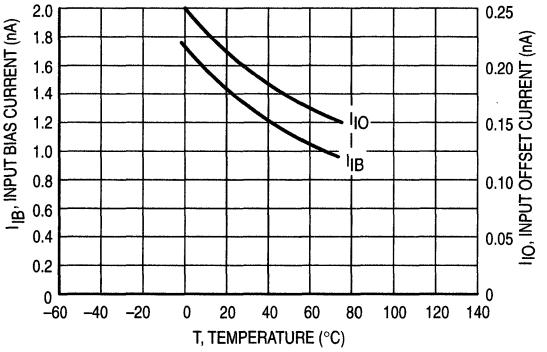


Figure 2. Maximum Equivalent Input Offset Voltage Error versus Input Resistance

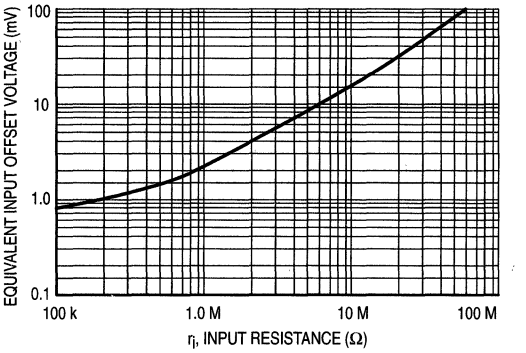


Figure 3. Voltage Gain versus Supply Voltages

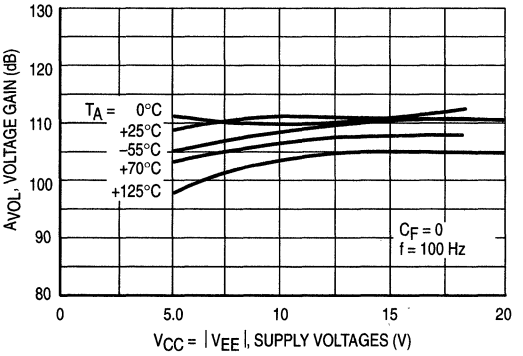


Figure 4. Power Supply Currents versus Power Supply Voltages

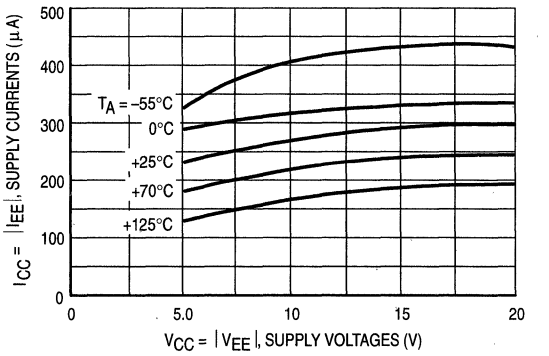


Figure 5. Open Loop Frequency Response

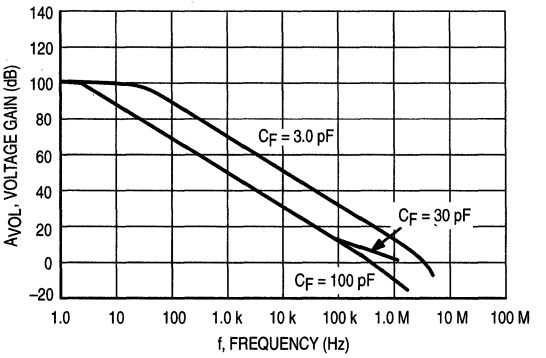
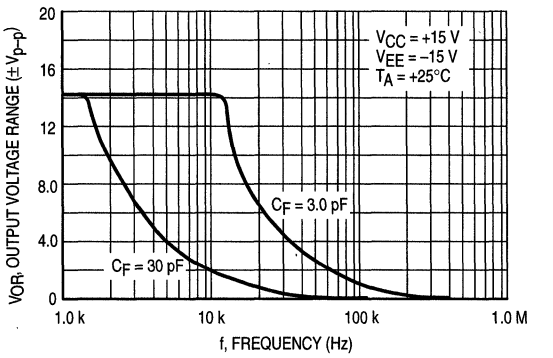


Figure 6. Large Signal Frequency Response



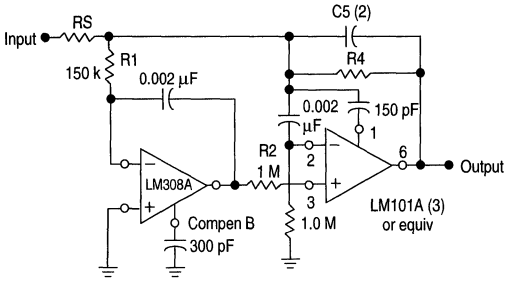
SUGGESTED DESIGN APPLICATIONS

INPUT GUARDING

Special care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the LM308A amplifier. Boards must be thoroughly cleaned with alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at +125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. The guard, which is a conductive ring surrounding the inputs, is connected to a low–impedance point that is at approximately the same voltage as the inputs. Leakage currents from high voltage pins are then absorbed by the guard.

Figure 7. Fast (1) Summing Amplifier with Low Input Current

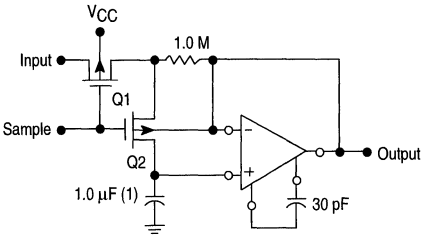


(1) Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/µs

(2) $C5 = \frac{6 \times 10^{-8}}{R1}$

(3) In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

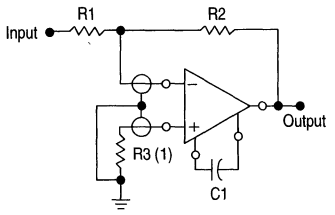
Figure 8. Sample and Hold



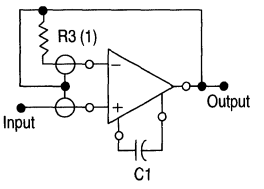
(1) Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

Figure 9. Connection of Input Guards

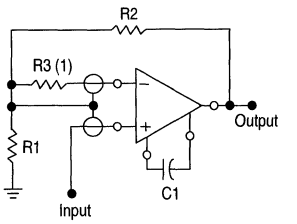
Inverting Amplifier



Follower



Noninverting Amplifier

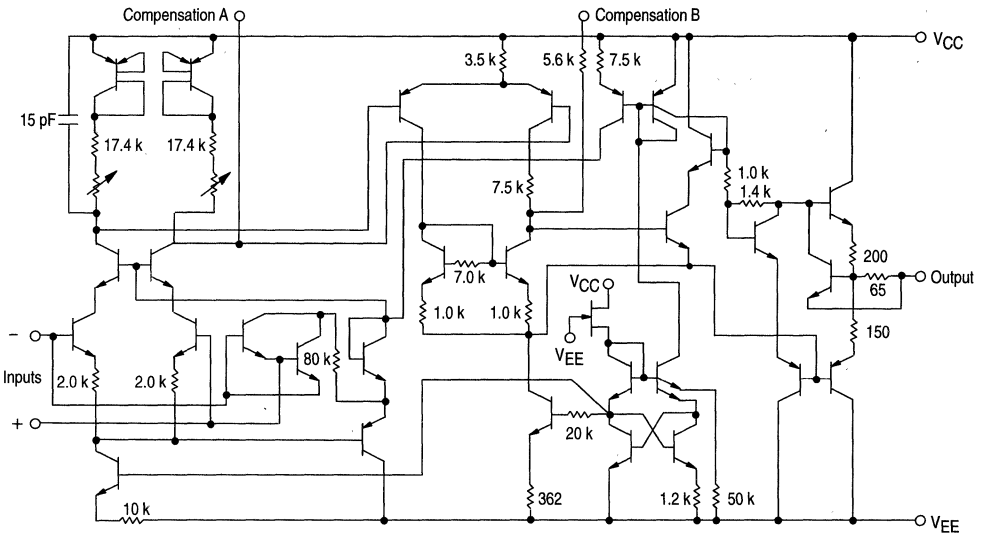


(1) Used to compensate for large source resistances.

Note: $\frac{R1\ R2}{R1 + R2}$ must be an impedance.

2

Representative Circuit Schematic



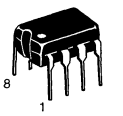
LM311
LM211

Highly Flexible Voltage Comparators

The ability to operate from a single power supply of 5.0 V to 30 V or ±15 V split supplies, as commonly used with operational amplifiers, makes the LM211/LM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the V_{CC} or the V_{EE} supply. This flexibility makes it possible to drive DTL, RTL, TTL, or MOS logic. The output can also switch voltages to 50 V at currents to 50 mA. Thus the LM211/LM311 can be used to drive relays, lamps or solenoids.

HIGH PERFORMANCE VOLTAGE COMPARATORS

SEMICONDUCTOR TECHNICAL DATA

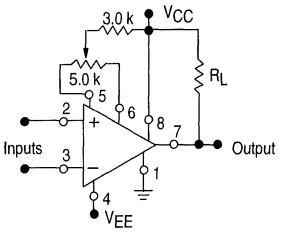


N SUFFIX
PLASTIC PACKAGE
CASE 626

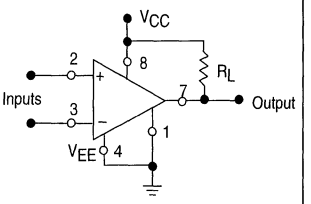
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Typical Comparator Design Configurations

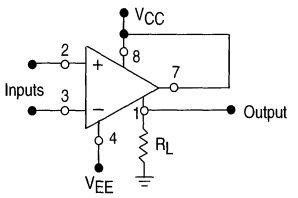
Split Power Supply with Offset Balance



Single Supply

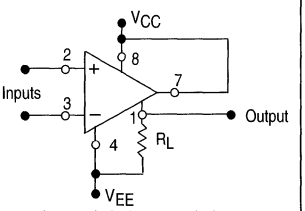


Ground–Referred Load



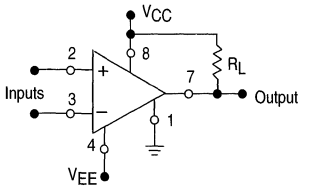
Input polarity is reversed when Gnd pin is used as an output.

Load Referred to Negative Supply

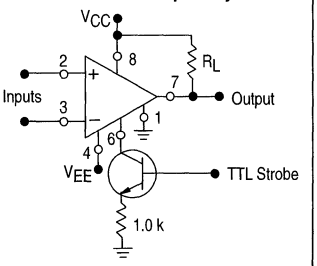


Input polarity is reversed when Gnd pin is used as an output.

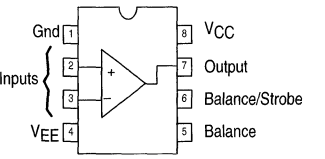
Load Referred to Positive Supply



Strobe Capability



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM211D	T_A = 25° to +85°C	SO–8
LM311D LM311N	T_A = 0° to +70°C	SO–8 Plastic DIP

2

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM211	LM311	Unit
Total Supply Voltage	V_{CC} + $\|V_{EE}\|$	36	36	Vdc
Output to Negative Supply Voltage	V_O –V_{EE}	50	40	Vdc
Ground to Negative Supply Voltage	V_{EE}	30	30	Vdc
Input Differential Voltage	V_{ID}	±30	±30	Vdc
Input Voltage (Note 2)	V_{in}	±15	±15	Vdc
Voltage at Strobe Pin	–	V_{CC} to V_{CC}–5	V_{CC} to V_{CC}–5	Vdc
Power Dissipation and Thermal Characteristics Plastic DIP Derate Above T_A = +25°C	 P_D $1/\theta_{JA}$	 625 5.0		 mW mW/°C
Operating Ambient Temperature Range	T_A	–25 to +85	0 to +70	°C
Operating Junction Temperature	$T_{J(max)}$	+150	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted [Note 1].)

Characteristic	Symbol	LM211			LM311			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 3) $R_S \leq$ 50 kΩ, T_A = +25°C $R_S \leq$ 50 kΩ, $T_{low} \leq T_A \leq T_{high}$*	V_{IO}	 – –	 0.7 –	 3.0 4.0	 – –	 2.0 –	 7.5 10	mV
Input Offset Current (Note 3) T_A = +25°C $T_{low} \leq T_A \leq T_{high}$*	I_{IO}	– –	1.7 –	10 20	– –	1.7 –	50 70	nA
Input Bias Current T_A = +25°C $T_{low} \leq T_A \leq T_{high}$*	I_{IB}	– –	45 –	100 150	– –	45 –	250 300	nA
Voltage Gain	A_V	40	200	–	40	200	–	V/mV
Response Time (Note 4)		–	200	–	–	200	–	ns
Saturation Voltage $V_{ID} \leq$ –5.0 mV, I_O = 50 mA, T_A = 25°C $V_{ID} \leq$–10 mV, I_O = 50 mA, T_A = 25°C $V_{CC} \geq$ 4.5 V, V_{EE} = 0, $T_{low} \leq T_A \leq T_{high}$* $V_{ID} \leq$6.0 mV, $I_{sink} \leq$ 8.0 mA $V_{ID} \leq$10 mV, $I_{sink} \leq$ 8.0 mA	V_{OL}	 – – – –	 0.75 – 0.23 –	 1.5 – 0.4 –	 – – – –	 – 0.75 – 0.23	 – 1.5 – 0.4	V
Strobe "On" Current (Note 5)	I_S	–	3.0	–	–	3.0	–	mA
Output Leakage Current $V_{ID} \geq$ 5.0 mV, V_O= 35 V, T_A = 25°C, I_{strobe}= 3.0 mA $V_{ID} \geq$ 10 mV, V_O= 35 V, T_A = 25°C, I_{strobe}= 3.0 mA $V_{ID} \geq$ 5.0 mV, V_O= 35 V, $T_{low} \leq T_A \leq T_{high}$*		 – – –	 0.2 – 0.1	 10 – 0.5	 – – –	 – 0.2 –	 – 50 –	 nA nA µA
Input Voltage Range ($T_{low} \leq T_A \leq T_{high}$*)	V_{ICR}	–14.5	–14.7 to 13.8	+13.0	–14.5	–14.7 to 13.8	+13.0	V
Positive Supply Current	I_{CC}	–	+2.4	+6.0	–	+2.4	+7.5	mA
Negative Supply Current	I_{EE}	–	–1.3	–5.0	–	–1.3	–5.0	mA

* T_{low} = –25°C for LM211 = 0°C for LM311 T_{high} = +85°C for LM211 = +70°C for LM311

NOTES: 1. Offset voltage, offset current and bias current specifications apply for a supply voltage range from a single 5.0 V supply up to ±15 V supplies.
2. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.
4. The response time specified is for a 100 mV input step with 5.0 mV overdrive.
5. Do not short the strobe pin to ground; it should be current driven at 3.0 mA to 5.0 mA.

Figure 1. Circuit Schematic

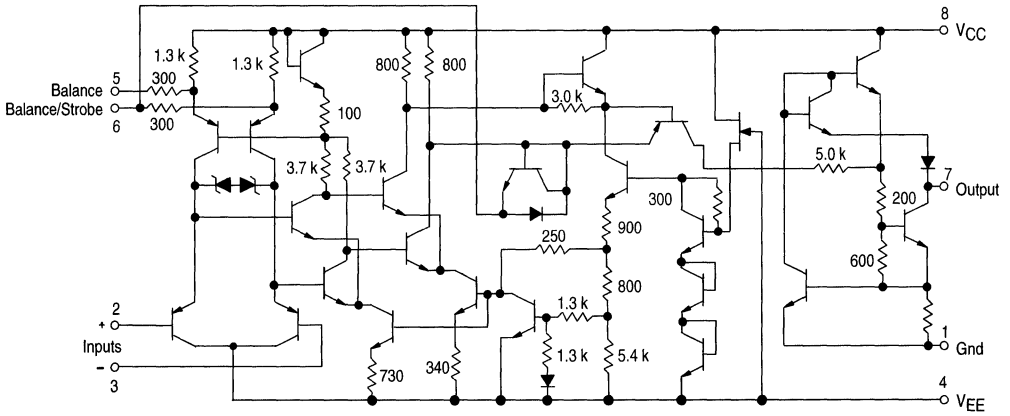


Figure 2. Input Bias Current versus Temperature

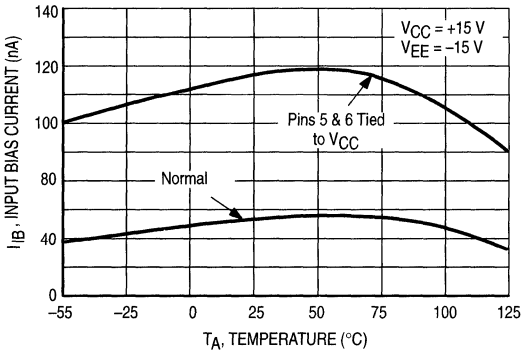


Figure 3. Input Offset Current versus Temperature

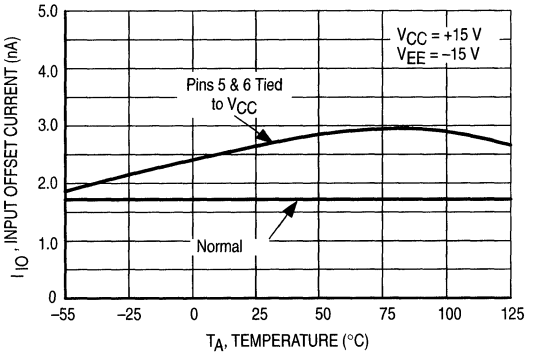


Figure 4. Input Bias Current versus Differential Input Voltage

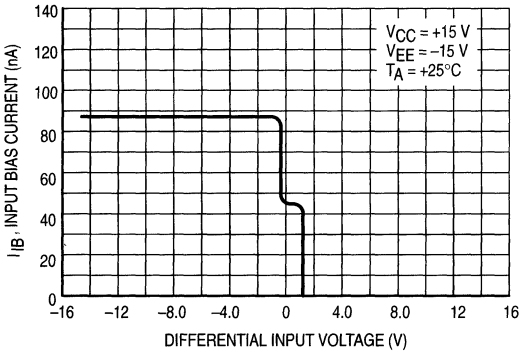
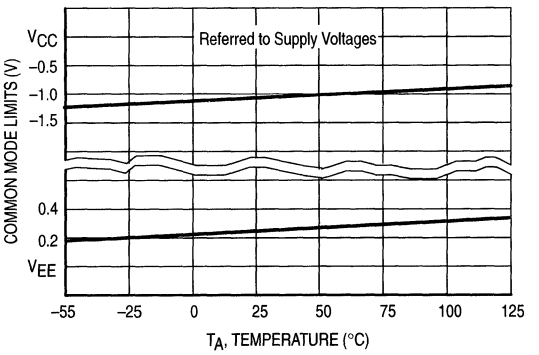


Figure 5. Common Mode Limits versus Temperature



2

Figure 6. Response Time for Various Input Overdrives

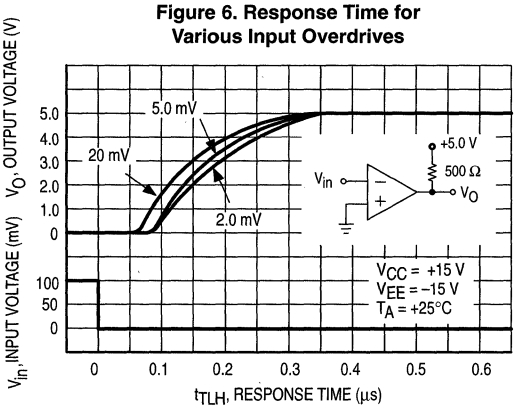


Figure 7. Response Time for Various Input Overdrives

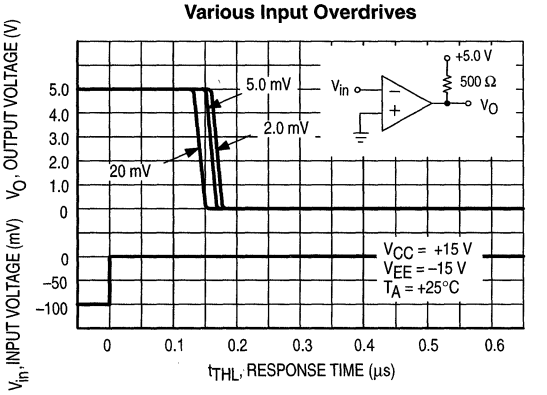


Figure 8. Response Time for Various Input Overdrives

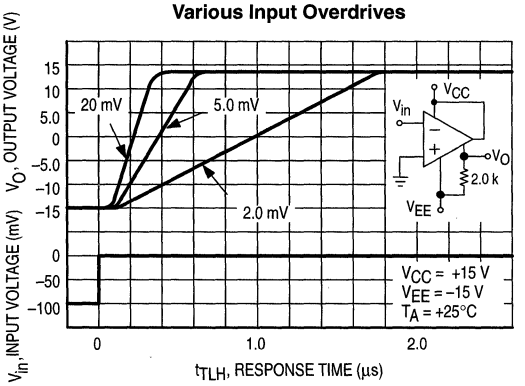


Figure 9. Response Time for Various Input Overdrives

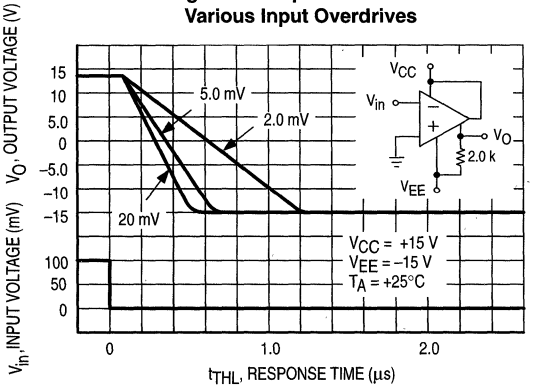


Figure 10. Output Short Circuit Current Characteristics and Power Dissipation

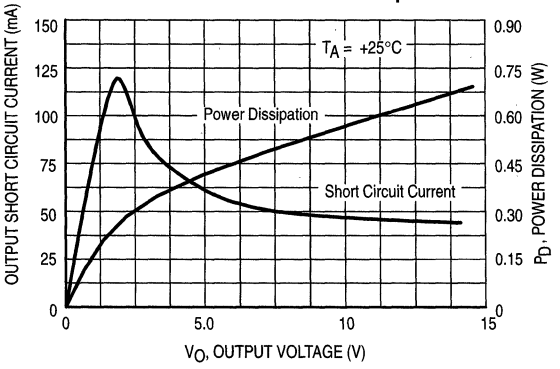


Figure 11. Output Saturation Voltage versus Output Current

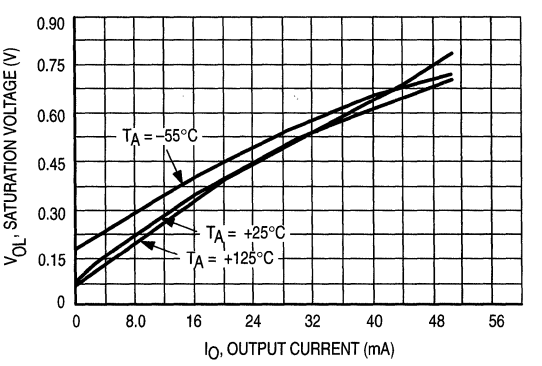


Figure 12. Output Leakage Current versus Temperature

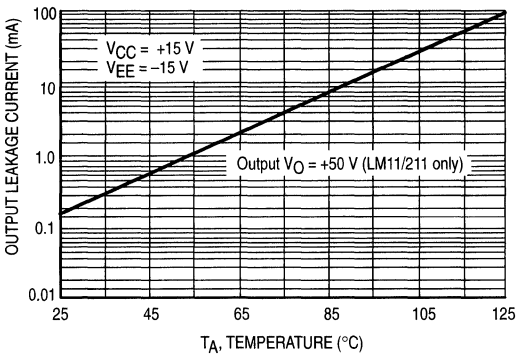


Figure 13. Power Supply Current versus Supply Voltage

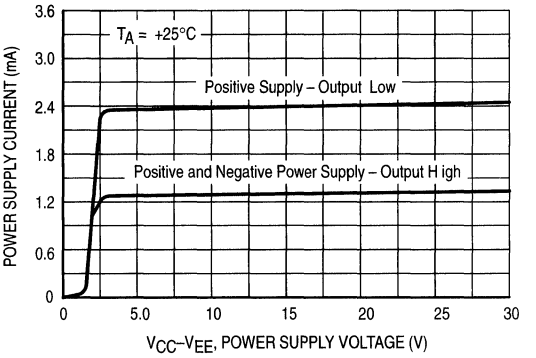
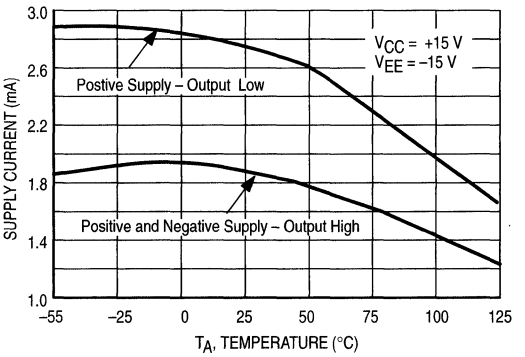


Figure 14. Power Supply Current versus Temperature



APPLICATIONS INFORMATION

Figure 15. Improved Method of Adding Hysteresis Without Applying Positive Feedback to the Inputs

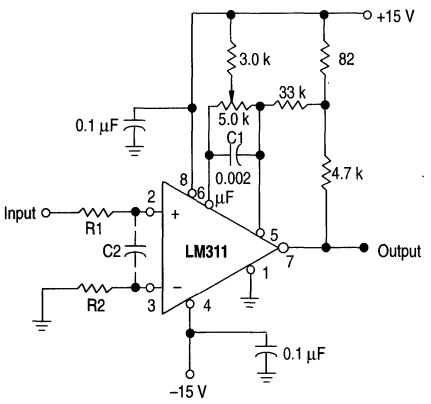
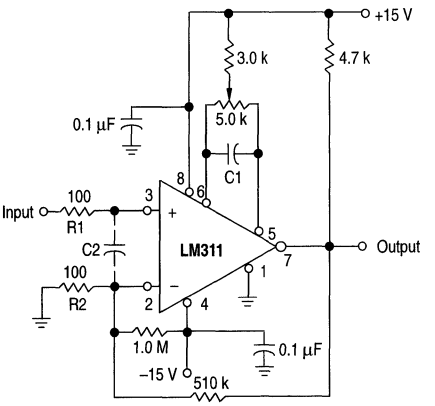


Figure 16. Conventional Technique for Adding Hysteresis



TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

2

When a high speed comparator such as the LM211 is used with high speed input signals and low source impedances, the output response will normally be fast and stable, providing the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (Pins 2 and 3) and also away from Pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1.0 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing–point. This is due to the high gain and wide bandwidth of comparators like the LM211 series. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 15.

The trim pins (Pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim–pot, they should be shorted together. If they are connected to a trim–pot, a 0.01 μF capacitor (C1) between Pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if Pin 5 is used for positive feedback as in Figure 15. For the fastest response time, tie both balance pins to V_{CC}.

Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor (C2) is connected directly across the input pins. When the signal source is applied through a resistive network, R1, it is usually advantageous to choose R2 of the same value, both for DC and for dynamic (AC) considerations. Carbon, tin–oxide, and metal–film resistors have all been used with good results in comparator input circuitry, but inductive wirewound resistors should be avoided.

When comparator circuits use input resistors (e.g., summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words, there should be a very short lead length or printed–circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R1 = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to dampen. Twisting these input leads tightly is the best alternative to placing resistors close to the comparator.

Since feedback to almost any pin of a comparator can result in oscillation, the printed–circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM211 circuitry (e.g., one side of a double layer printed circuit board). Ground, positive supply or negative supply foil should extend between the output and the inputs to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides to guard against capacitive coupling from any fast high–level signals (such as the output). If Pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim–pot, the trim–pot should be located no more than a few inches away from the LM211, and a 0.01 μF capacitor should be installed across Pins 5 and 6. If this capacitor cannot be used, a shielding printed–circuit foil may be advisable between Pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM211.

A standard procedure is to add hysteresis to a comparator to prevent oscillation, and to avoid excessive noise on the output. In the circuit of Figure 16, the feedback resistor of 510 kΩ from the output to the positive input will cause about 3.0 mV of hysteresis. However, if R2 is larger than 100 Ω, such as 50 kΩ, it would not be practical to simply increase the value of the positive feedback resistor proportionally above 510 kΩ to maintain the same amount of hysteresis.

When both inputs of the LM211 are connected to active signals, or if a high–impedance signal is driving the positive input of the LM211 so that positive feedback would be disruptive, the circuit of Figure 15 is ideal. The positive feedback is applied to Pin 5 (one of the offset adjustment pins). This will be sufficient to cause 1.0 mV to 2.0 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive–feedback signal across the 82 Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at Pin 5, so this feedback does not add to the offset voltage of the comparator. As much as 8.0 mV of offset voltage can be trimmed out, using the 5.0 kΩ pot and 3.0 kΩ resistor as shown.

Figure 17. Zero–Crossing Detector Driving CMOS Logic

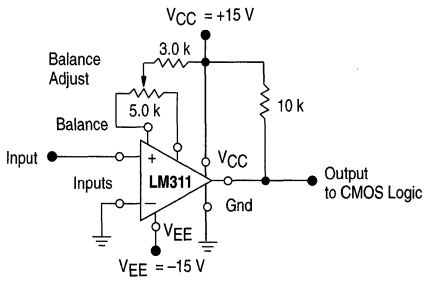
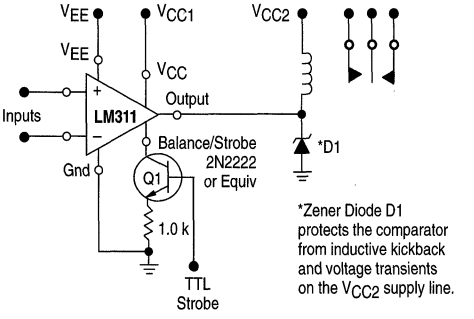


Figure 18. Relay Driver with Strobe Capability



LM324, LM324A, LM224, LM2902, LM2902V

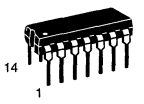
Quad Low Power Operational Amplifiers

The LM324 series are low–cost, quad operational amplifiers with true differential inputs. They have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 32 V with quiescent currents about one–fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

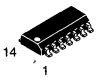
- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents: 100 nA Maximum (LM324A)
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Operation

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

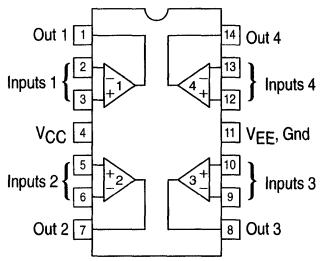


N SUFFIX
PLASTIC PACKAGE
CASE 646
(LM224, LM324, LM2902 Only)



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM224 LM324, LM324A	LM2902, LM2902V	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	 26 ±13	Vdc
Input Differential Voltage Range (See Note 1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range	V_{ICR}	–0.3 to 32	–0.3 to 26	Vdc
Output Short Circuit Duration	t_{SC}	Continuous		
Junction Temperature	T_J	150		°C
Storage Temperature Range	T_{stg}	–65 to +150		°C
Operating Ambient Temperature Range	T_A	–25 to +85 0 to +70	–40 to +105 –40 to +125	°C

NOTE: 1. Split Power Supplies.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM2902D	T_A = –40° to +105°C	SO–14
LM2902N		Plastic DIP
LM2902VD	T_A = –40° to +125°C	SO–14
LM2902VN		Plastic DIP
LM224D	T_A = –25° to +85°C	SO–14
LM224N		Plastic DIP
LM324AD	T_A = 0° to +70°C	SO–14
LM324AN		Plastic DIP
LM324D		SO–14
LM324N		Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	LM224			LM324A			LM324			LM2902			LM2902V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}																mV
V_{CC} = 5.0 V to 30 V (26 V for LM2902, V), V_{ICR} = 0 V to V_{CC} −1.7 V, V_O = 1.4 V, R_S = 0 Ω																	
T_A = 25°C		–	2.0	5.0	–	2.0	3.0	–	2.0	7.0	–	2.0	7.0	–	2.0	7.0	
T_A = T_{high}(1)		–	–	7.0	–	–	5.0	–	–	9.0	–	–	10	–	–	13	
T_A = T_{low}(1)		–	–	7.0	–	–	5.0	–	–	9.0	–	–	10	–	–	10	
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low}(1)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	30	–	7.0	–	–	7.0	–	–	7.0	–	µV/°C
Input Offset Current	I_{IO}	–	3.0	30	–	5.0	30	–	5.0	50	–	5.0	50	–	5.0	50	nA
T_A = T_{high} to T_{low}(1)		–	–	100	–	–	75	–	–	150	–	–	200	–	–	200	
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low}(1)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	300	–	10	–	–	10	–	–	10	–	pA/°C
Input Bias Current	I_{IB}	–	–90	–150	–	–45	–100	–	–90	–250	–	–90	–250	–	–90	–250	nA
T_A = T_{high} to T_{low}(1)		–	–	–300	–	–	–200	–	–	–500	–	–	–500	–	–	–500	
Input Common Mode Voltage Range(2)	V_{ICR}																V
V_{CC} = 30 V (26 V for LM2902, V)		0	–	28.3	0	–	28.3	0	–	28.3	0	–	24.3	0	–	24.3	
V_{CC} = 30 V (26 V for LM2902, V), T_A = T_{high} to T_{low}		0	–	28	0	–	28	0	–	28	0	–	24	0	–	24	
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open Loop Voltage Gain	A_{VOL}																V/mV
R_L = 2.0 kΩ, V_{CC} = 15 V, for Large V_O Swing, T_A = T_{high} to T_{low}(1)		50	100	–	25	100	–	25	100	–	25	100	–	25	100	–	
		25	–	–	15	–	–	15	–	–	15	–	–	15	–	–	
Channel Separation 10 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	–	–120	–	–	–120	–	–	–120	–	–	–120	–	–	–120	–	dB
Common Mode Rejection, R_S ≤ 10 kΩ	CMR	70	85	–	65	70	–	65	70	–	50	70	–	50	70	–	dB
Power Supply Rejection	PSR	65	100	–	65	100	–	65	100	–	50	100	–	50	100	–	dB
Output Voltage−High Limit (T_A = T_{high} to T_{low})(1)	V_{OH}																V
V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C		3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	
V_{CC} = 30 V (26 V for LM2902, V), R_L = 2.0 kΩ		26	–	–	26	–	–	26	–	–	22	–	–	22	–	–	
V_{CC} = 30 V (26 V for LM2902, V), R_L = 10 kΩ		27	28	–	27	28	–	27	28	–	23	24	–	23	24	–	

NOTES: 1. T_{low} = −25°C for LM224 = 0°C for LM324, A = −40°C for LM2902 = −40°C for LM2902V
T_{high} = +85°C for LM224 = +70°C for LM324, A = +105°C for LM2902 = +125°C for LM2902V

2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} −1.7 V.

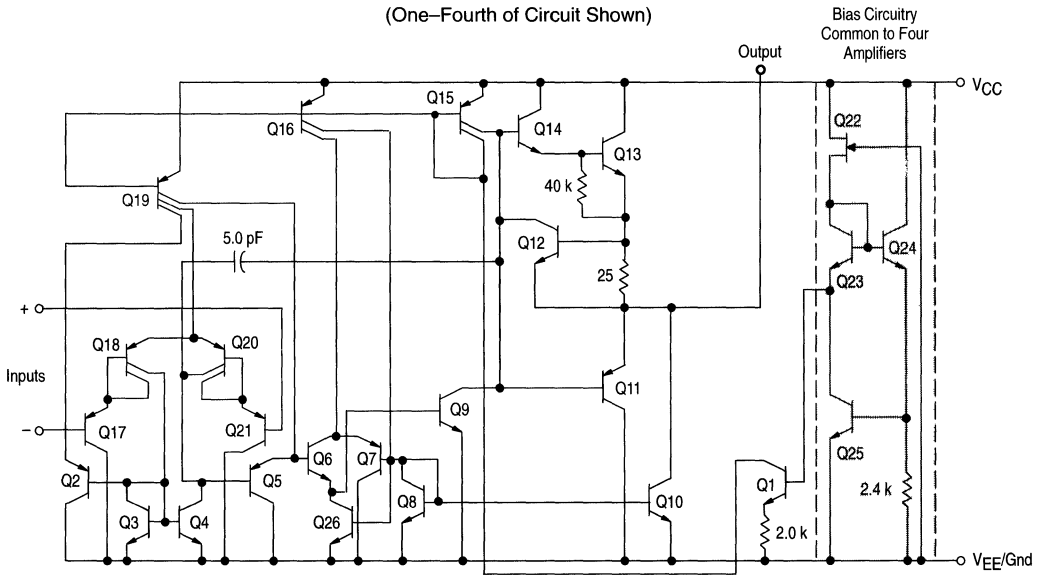
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	LM224			LM324A			LM324			LM2902			LM2902V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage – Low Limit, V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low}(1)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	20	–	5.0	100	–	5.0	100	mV
Output Source Current (V_{ID} = +1.0 V, V_{CC} = 15 V)	I_{O+}																mA
T_A = 25°C		20	40	–	20	40	–	20	40	–	20	40	–	20	40	–	
T_A = T_{high} to T_{low}(1)		10	20	–	10	20	–	10	20	–	10	20	–	10	20	–	
Output Sink Current	I_{O-}																mA
(V_{ID} = –1.0 V, V_{CC} = 15 V) T_A = 25°C		10	20	–	10	20	–	10	20	–	10	20	–	10	20	–	
T_A = T_{high} to T_{low}(1)		5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	
(V_{ID} = –1.0 V, V_O = 200 mV, T_A = 25°C)		12	50	–	12	50	–	12	50	–	–	–	–	–	–	–	µA
Output Short Circuit to Ground(3)	I_{SC}	–	40	60	–	40	60	–	40	60	–	40	60	–	40	60	mA
Power Supply Current (T_A = T_{high} to T_{low})(1)	I_{CC}																mA
V_{CC} = 30 V (26 V for LM2902, V), V_O = 0 V, R_L = ∞		–	–	3.0	–	1.4	3.0	–	–	3.0	–	–	3.0	–	–	3.0	
V_{CC} = 5.0 V, V_O = 0 V, R_L = ∞		–	–	1.2	–	0.7	1.2	–	–	1.2	–	–	1.2	–	–	1.2	

NOTES: 1. T_{low} = –25°C for LM224 T_{high} = +85°C for LM224
= 0°C for LM324, A = +70°C for LM324, A
= –40°C for LM2902 = +105°C for LM2902
= –40°C for LM2902V = +125°C for LM2902V

2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} –1.7 V.

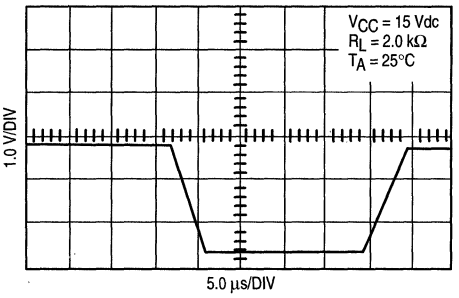
Representative Circuit Diagram
(One–Fourth of Circuit Shown)



CIRCUIT DESCRIPTION

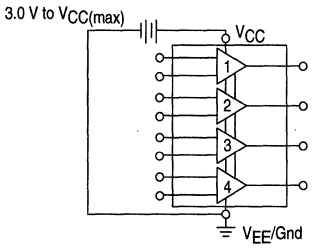
The LM324 series is made using four internally compensated, two–stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single–ended converter. The second stage consists of a standard current source load amplifier stage.

Large Signal Voltage Follower Response



Each amplifier is biased from an internal–voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Single Supply



Split Supplies

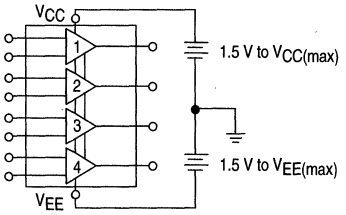


Figure 1. Input Voltage Range

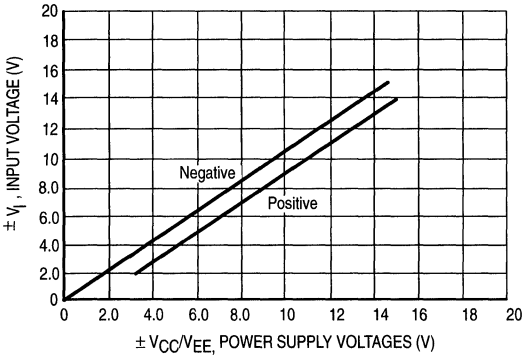


Figure 2. Open Loop Frequency

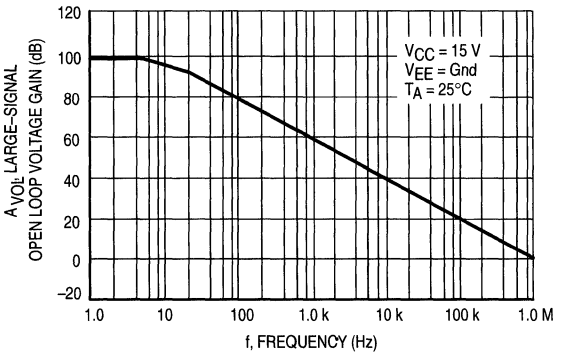


Figure 3. Large–Signal Frequency Response

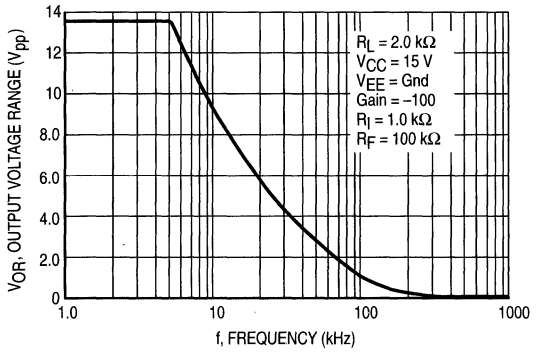


Figure 4. Small–Signal Voltage Follower Pulse Response (Noninverting)

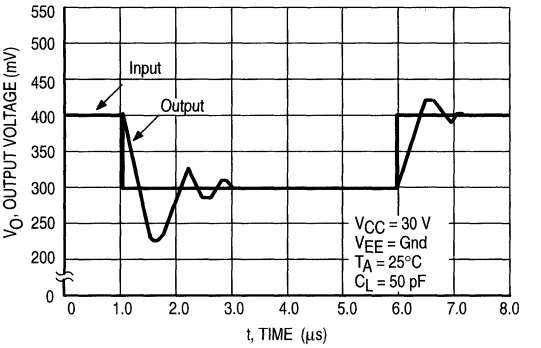


Figure 5. Power Supply Current versus Power Supply Voltage

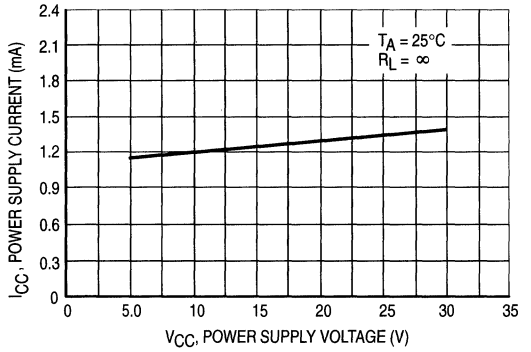
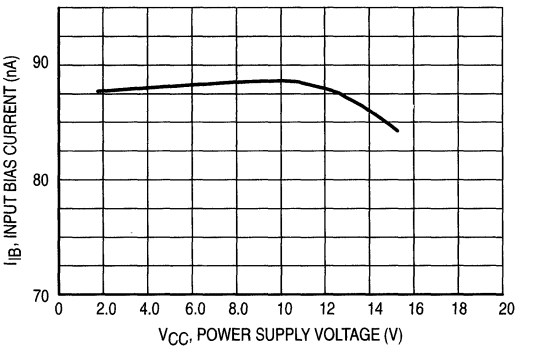
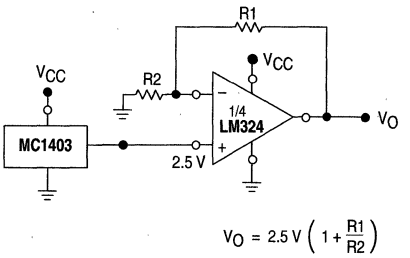


Figure 6. Input Bias Current versus Power Supply Voltage



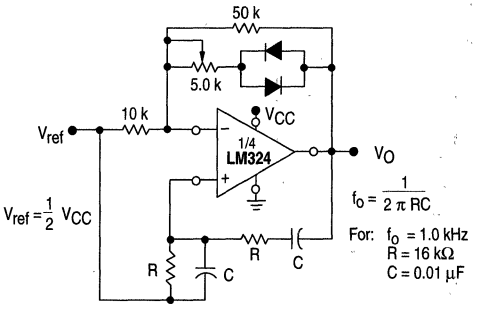
2

Figure 7. Voltage Reference



$$V_O = 2.5\,V\left(1 + \frac{R1}{R2}\right)$$

Figure 8. Wien Bridge Oscillator

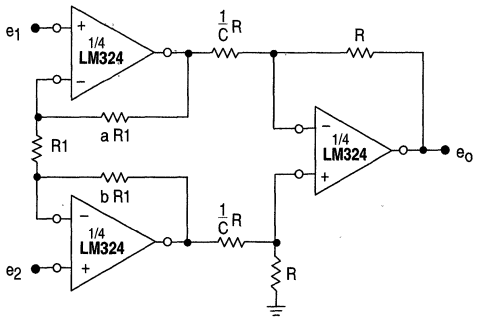


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2\pi RC}$$

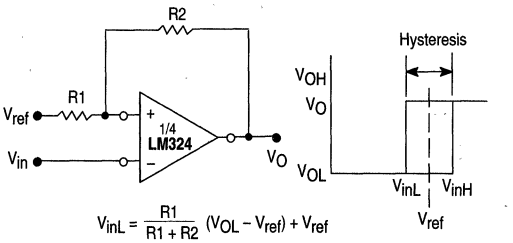
For: f_o = 1.0 kHz
R = 16 kΩ
C = 0.01 μF

Figure 9. High Impedance Differential Amplifier



$$e_o = C(1 + a + b)(e_2 - e_1)$$

Figure 10. Comparator with Hysteresis

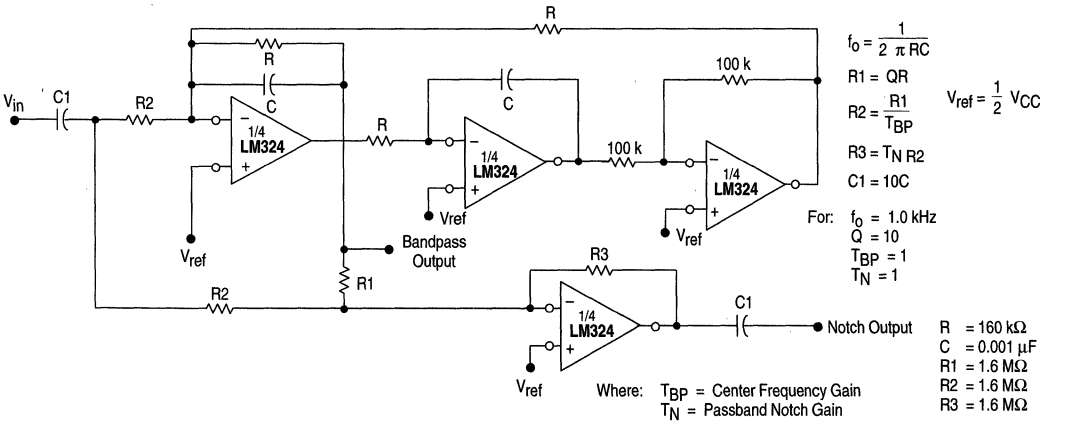


$$V_{inL} = \frac{R1}{R1 + R2}(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2}(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

Figure 11. Bi–Quad Filter



$$f_o = \frac{1}{2\pi RC}$$

R1 = QR

$$R2 = \frac{R1}{T_{BP}}$$

R3 = T_N R2

C1 = 10C

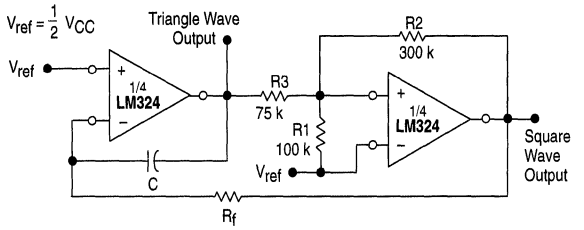
$$V_{ref} = \frac{1}{2} V_{CC}$$

For: f_o = 1.0 kHz
Q = 10
T_{BP} = 1
T_N = 1

R = 160 kΩ
C = 0.001 μF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

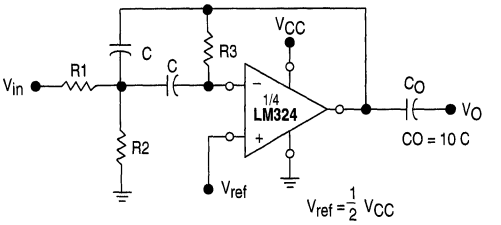
Where: T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

Figure 12. Function Generator



$$f = \frac{R1 + R_C}{4\,C R_f\,R1} \quad \text{if} \quad R3 = \frac{R2\,R1}{R2 + R1}$$

Figure 13. Multiple Feedback Bandpass Filter



Given: f_o = center frequency
$A(f_o)$ = gain at center frequency

Choose value f_o, C

Then: $R3 = \frac{Q}{\pi f_o C}$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier, $\frac{Q_o f_o}{BW} < 0.1$

where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

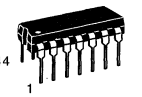
2

Quad Single Supply Comparators

LM339, LM339A, LM239, LM239A, LM2901, M2901V, MC3302

These comparators are designed for use in level detection, low–level sensing and memory applications in consumer automotive and industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: ±5.0 nA (Typ)
- Low Input Offset Voltage: ±1.0 mV (Typ) LM139A Series
- Input Common Mode Voltage Range to Gnd
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible
- ESD Clamps on the Inputs Increase Reliability without Affecting Device Operation



N, P SUFFIX
PLASTIC PACKAGE
CASE 646

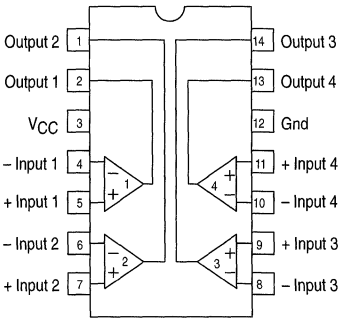
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage LM239, A/LM339A/LM2901, V MC3302	V_{CC}	 +36 or ±18 +30 or ±15	Vdc
Input Differential Voltage Range LM239, A/LM339A/LM2901, V MC3302	V_{IDR}	 36 30	Vdc
Input Common Mode Voltage Range	V_{ICMR}	–0.3 to V_{CC}	Vdc
Output Short Circuit to Ground (Note 1)	I_{SC}	Continuous	
Power Dissipation @ T_A = 25°C Plastic Package Derate above 25°C	P_D	 1.0 8.0	 W mW/°C
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range LM239, A MC3302 LM2901 LM2901V LM339, A	T_A	 –25 to +85 –40 to +85 –40 to +105 –40 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

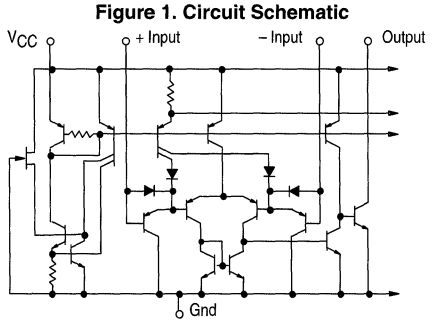
NOTE: 1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}. Output short circuits to V_{CC} can cause excessive heating and eventual destruction.

PIN CONNECTIONS



(Top View)

Figure 1. Circuit Schematic



NOTE: Diagram shown is for 1 comparator.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM239D,AD LM239N,AN	T_A = 25° to +85°C	SO–14 Plastic DIP
LM339D, AD LM339N, AN	T_A = 0° to +70°C	SO–14 Plastic DIP
LM2901D LM2901N	T_A = –40° to +105°C	SO–14 Plastic DIP
LM2901VD LM2901VN	T_A = –40° to +125°C	SO–14 Plastic DIP
MC3302P	T_A = –40° to +85°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = +25°C, unless otherwise noted)

Characteristic	Symbol	LM239A/339A			LM239/339			LM2901/2901V			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	–	±1.0	±2.0	–	±2.0	±5.0	–	±2.0	±7.0	–	±3.0	±20	mVdc
Input Bias Current (Notes 4, 5) (Output in Analog Range)	I_{IB}	–	25	250	–	25	250	–	25	250	–	25	500	nA
Input Offset Current (Note 4)	I_{IO}	–	±5.0	±50	–	±5.0	±50	–	±5.0	±50	–	±3.0	±100	nA
Input Common Mode Voltage Range	V_{ICMR}	0	–	V_{CC} –1.5	0	–	V_{CC} –1.5	0	–	V_{CC} –1.5	0	–	V_{CC} –1.5	V
Supply Current R_L = ∞ (For All Comparators) R_L = ∞, V_{CC} = 30 Vdc	I_{CC}	 – –	 0.8 1.0	 2.0 2.5	 – –	 0.8 1.0	 2.0 2.5	 – –	 0.8 1.0	 2.0 2.5	 – –	 0.8 1.0	 2.0 2.5	mA
Voltage Gain R_L ≥ 15 kΩ, V_{CC} = 15 Vdc	A_{VOL}	50	200	–	50	200	–	25	100	–	25	100	–	V/mV
Large Signal Response Time V_I = TTL Logic Swing, V_{ref} = 1.4 Vdc, V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	–	–	300	–	–	300	–	–	300	–	–	300	–	ns
Response Time (Note 6) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	–	–	1.3	–	–	1.3	–	–	1.3	–	–	1.3	–	µs
Output Sink Current V_I (–) ≥ +1.0 Vdc, V_I(+) = 0, V_O ≤ 1.5 Vdc	I_{Sink}	6.0	16	–	6.0	16	–	6.0	16	–	6.0	16	–	mA
Saturation Voltage V_I(–) ≥ +1.0 Vdc, V_I(+) = 0, I_{sink} ≤ 4.0 mA	V_{sat}	–	130	400	–	130	400	–	130	400	–	130	500	mV
Output Leakage Current V_I(+) ≥ +1.0 Vdc, V_I(–) = 0, V_O = +5.0 Vdc	I_{OL}	–	0.1	–	–	0.1	–	–	0.1	–	–	0.1	–	nA

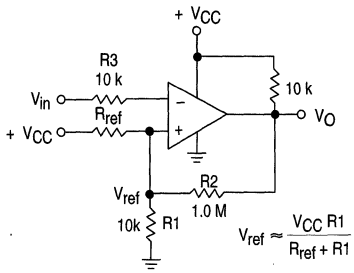
PERFORMANCE CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = T_{low} to T_{high} [Note 3])

Characteristic	Symbol	LM239A/339A			LM239/339			LM2901/2901V			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	–	–	±4.0	–	–	±9.0	–	–	±15	–	–	±40	mVdc
Input Bias Current (Notes 4, 5) (Output in Analog Range)	I_{IB}	–	–	400	–	–	400	–	–	500	–	–	1000	nA
Input Offset Current (Note 4)	I_{IO}	–	–	±150	–	–	±150	–	–	±200	–	–	±300	nA
Input Common Mode Voltage Range	V_{ICMR}	0	–	V_{CC} –2.0	0	–	V_{CC} –2.0	0	–	V_{CC} –2.0	0	–	V_{CC} –2.0	V
Saturation Voltage V_I(–) ≥ +1.0 Vdc, V_I(+) = 0, I_{sink} ≤ 4.0 mA	V_{sat}	–	–	700	–	–	700	–	–	700	–	–	700	mV
Output Leakage Current V_I(+) ≥ +1.0 Vdc, V_I(–) = 0, V_O = 30 Vdc	I_{OL}	–	–	1.0	–	–	1.0	–	–	1.0	–	–	1.0	µA
Differential Input Voltage All V_I ≥ 0 Vdc	V_{ID}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	Vdc

NOTES: 3. (LM239/239A) T_{low} = –25°C, T_{high} = +85°
(LM339/339A) T_{low} = 0°C, T_{high} = +70°C
(MC3302) T_{low} = –40°C, T_{high} = +85°C
(LM2901) T_{low} = –40°C, T_{high} = +105°
(LM2901V) T_{low} = –40°C, T_{high} = +125°C

4. At the output switch point, $V_O \simeq$ 1.4 Vdc, $R_S \leq$ 100 Ω 5.0 Vdc ≤ V_{CC} ≤ 30 Vdc, with the inputs over the full common mode range (0 Vdc to V_{CC} –1.5 Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

Figure 2. Inverting Comparator with Hystersis



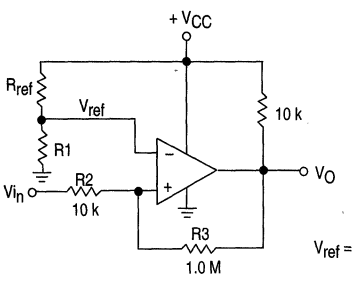
$$V_{ref} \approx \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R3 \simeq R1 \,//\, R_{ref} \,//\, R2$$

$$V_H = \frac{R1 \,//\, R_{ref}}{R1 \,//\, R_{ref} + R2}\ [V_{O(max)} - V_{O(min)}]$$

$$R2 \gg Rref \,//\, R1$$

Figure 3. Noninverting Comparator with Hysteresis



$$V_{ref} = \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R2 \approx R1 \,//\, R_{ref}$$

Amount of Hysteresis V_H

$$V_H = \frac{R2}{R2 + R3}\ [(V_{O(max)} - V_{O(min)}]$$

Typical Characteristics

(V_{CC} = 15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

Figure 4. Normalized Input Offset Voltage

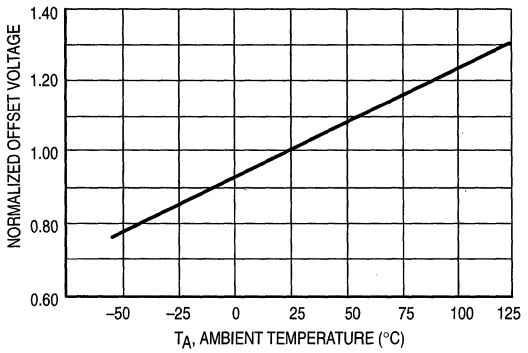


Figure 5. Input Bias Current

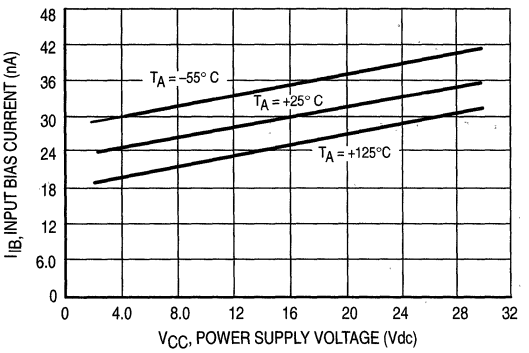


Figure 6. Output Sink Current versus Output Saturation Voltage

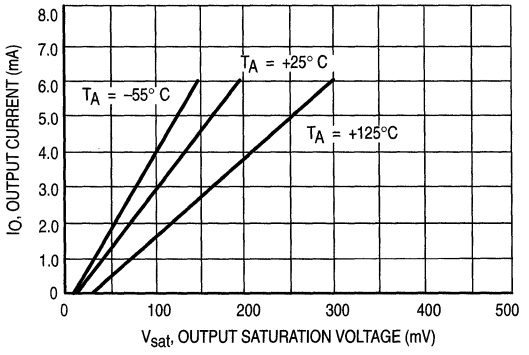
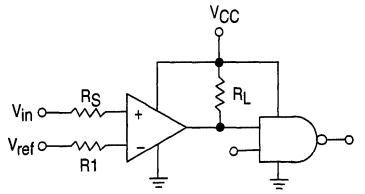


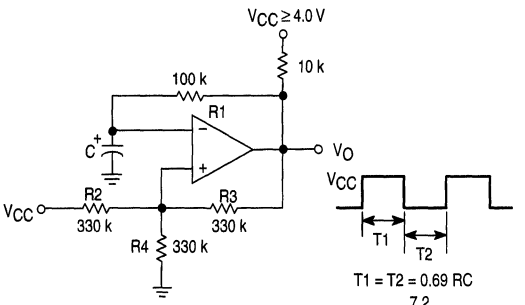
Figure 7. Driving Logic



RS = Source Resistance
R1 ≃ RS

Logic	Device	V_{CC} (V)	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5.0	10

Figure 8. Squarewave Oscillator



T1 = T2 = 0.69 RC

$$f \approx \frac{7.2}{C(\mu F)}$$

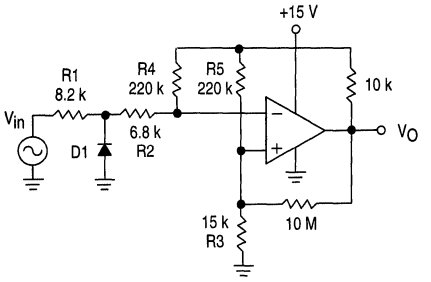
R2 = R3 = R4
R1 ≃ R2 // R3 // R4

APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator's inputs. Voltages more negative than –300 mV should not be used.

Figure 9. Zero Crossing Detector (Single Supply)



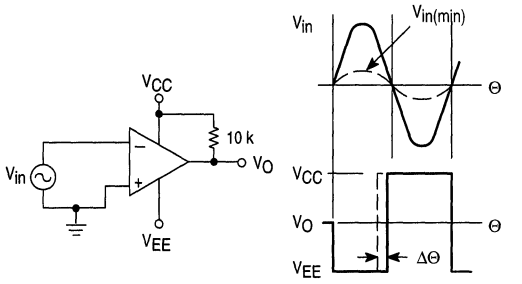
D1 prevents input from going negative by more than 0.6 V.

R1 + R2 = R3

$$R3 \leq \frac{R5}{10}$$ for small error in zero crossing

Figure 10. Zero Crossing Detector (Split Supplies)

$V_{in(min)} \approx 0.4$ V peak for 1% phase distortion (ΔΘ).



LM348

Differential Input Operational Amplifier

DIFFERENTIAL INPUT OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

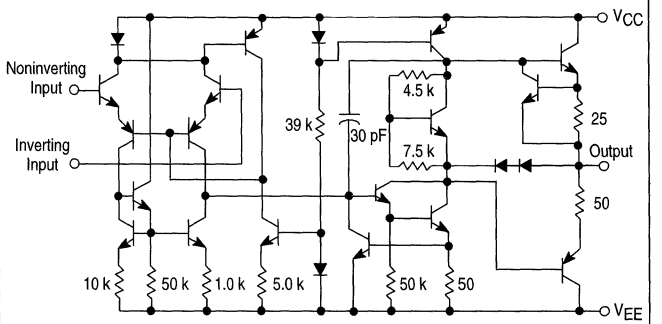
The LM348 is a true quad MC1741. Integrated on a single monolithic chip are four independent, low power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single MC1741. Other features include input offset currents and input bias currents which are much less than the MC1741 industry standard.

The LM348 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

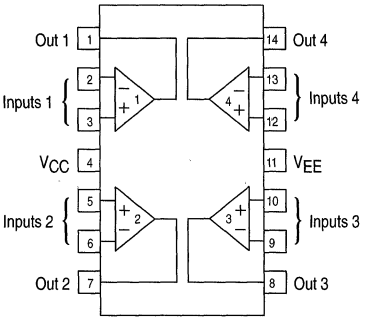
- Each Amplifier is Functionally Equivalent to the MC1741
- Low Input Offset and Input Bias Currents
- Class AB Output Stage Eliminates Crossover Distortion
- Pin Compatible with MC3403 and LM324
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

Representative Schematic Diagram
(1/4 of Circuit Shown)



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM348D	T_A = 0° to +70°C	SO–14

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 −18	Vdc
Input Differential Voltage	V_{ID}	±36	V
Input Common Mode Voltage	V_{ICM}	±18	V
Output Short Circuit Duration	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	–	1.0	6.0	mV
Input Offset Current Input Bias Current	I_{IO} I_{IB}	– –	4.0 30	50 200	nA
Input Resistance	r_i	0.8	2.5	–	MΩ
Common Mode Input Voltage Range	V_{ICR}	±12	–	–	V
Large Signal Voltage Gain ($R_L \geq 2.0$ k, V_O = ±10 V)	A_{VOL}	25	160	–	V/mV
Channel Separation (f = 1.0 Hz to 20 kHz)	–	–	−120	–	dB
Common Mode Rejection ($R_S \leq 10$ k) Supply Voltage Rejection ($R_S \leq 10$ k)	CMR PSR	70 77	90 96	– –	dB
Output Voltage Swing ($R_L \geq 10$ k) ($R_L \geq 2.0$ k)	V_O	 ±12 ±10	 ±13 ±12	 – –	V
Output Short Circuit Current	I_{SC}	–	25	–	mA
Supply Current (All Amplifiers)	I_D	–	2.4	4.5	mA
Small Signal Bandwidth (A_V = 1)	BW	–	1.0	–	MHz
Phase Margin (A_V = 1)	ϕm	–	60	–	Degrees
Slew Rate (A_V = 1)	SR	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = *T_{high} to T_{low}, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	–	7.5	mV
Input Offset Current Input Bias Current	I_{IO} I_{IB}	– –	– –	100 400	nA
Common Mode Input Voltage Range	V_{ICR}	±12	–	–	V
Large Signal Voltage Gain ($R_L \geq 2$ k, V_O = ±10 V)	A_{VOL}	15	–	–	V/mV
Common Mode Rejection ($R_S \leq 10$ k) Supply Voltage Rejection ($R_S \leq 10$ k)	CMR PSR	70 77	90 96	– –	dB
Output Voltage Swing ($R_L \geq 10$ k) ($R_L \geq 2$ k)	V_O	 ±12 ±10	 ±13 ±12	 – –	V

* T_{high} = 70°C. T_{low} = 0°C.

NOTE: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted or the maximum junction temperature will be exceeded.

2

Figure 1. Power Bandwidth (Large Signal Swing versus Frequency)

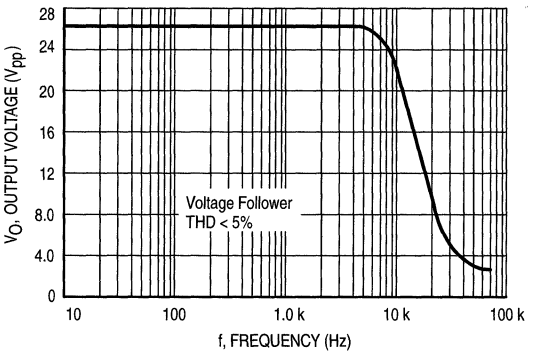


Figure 2. Open Loop Frequency Response

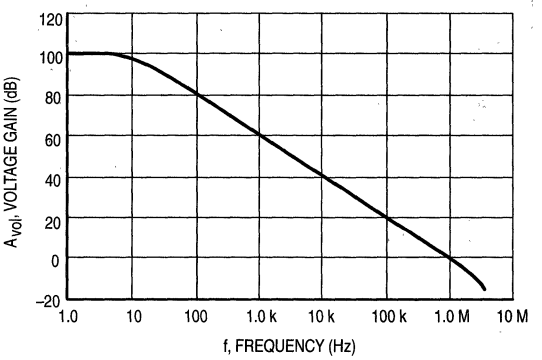


Figure 3. Positive Output Voltage Swing versus Load Resistance

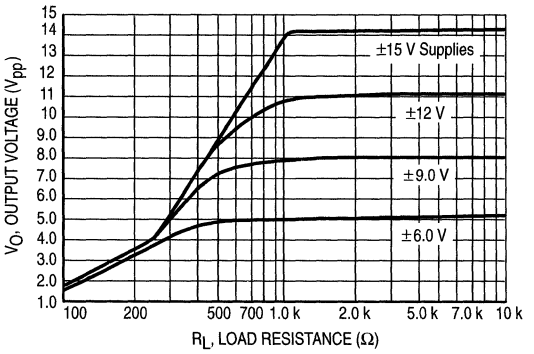


Figure 4. Negative Output Voltage Swing versus Load Resistance

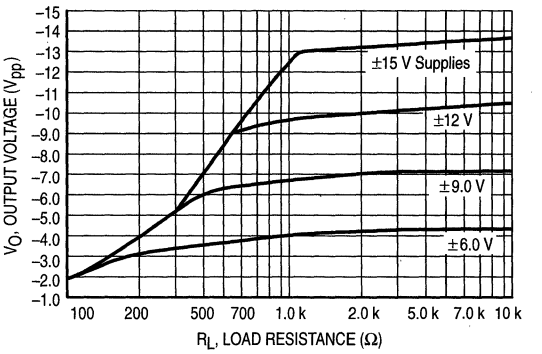


Figure 5. Output Voltage Swing versus Load Resistance (Single Supply Operation)

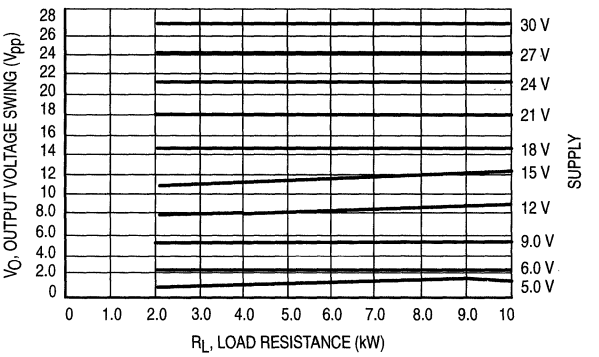


Figure 6. Noninverting Pulse Response

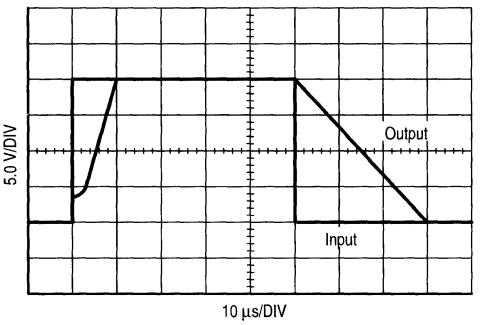
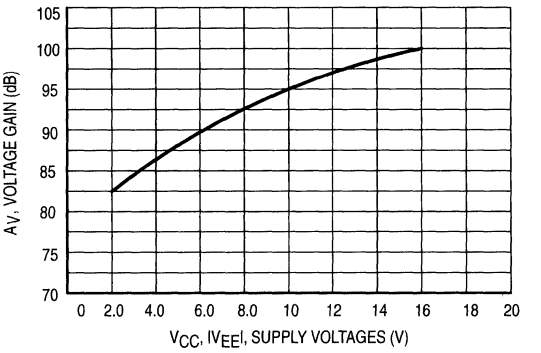
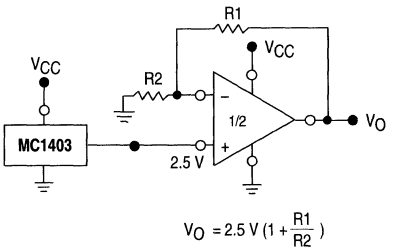


Figure 7. Open Loop Voltage Gain versus Supply Voltage



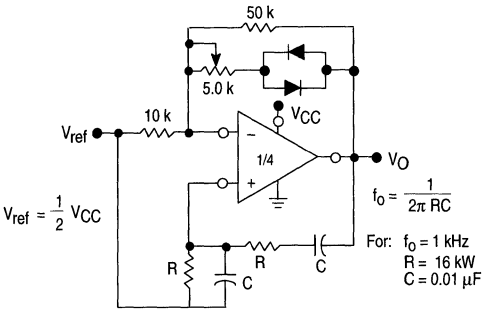
APPLICATIONS INFORMATION

Figure 8. Voltage Reference



$$V_O = 2.5\,V\left(1 + \frac{R1}{R2}\right)$$

Figure 9. Wien Bridge Oscillator

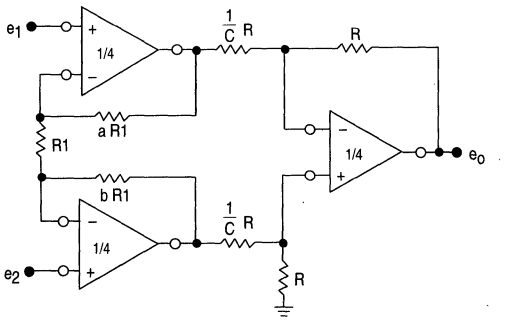


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2\pi RC}$$

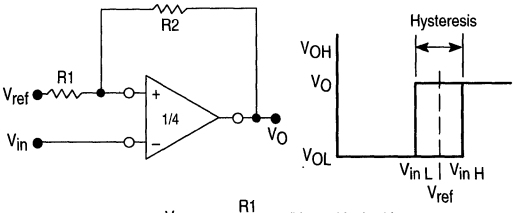
For: f_o = 1 kHz
R = 16 kW
C = 0.01 µF

Figure 10. High Impedance Differential Amplifier



$$e_o = C\,(1 + a + b)\,(e_2 - e_1)$$

Figure 11. Comparator with Hysteresis



$$V_{in\,L} = \frac{R1}{R1 + R2}\,(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{in\,H} = \frac{R1}{R1 + R2}\,(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}\,(V_{OH} - V_{OL})$$

2

Figure 12. High Impedance Instrumentation Buffer/Filter

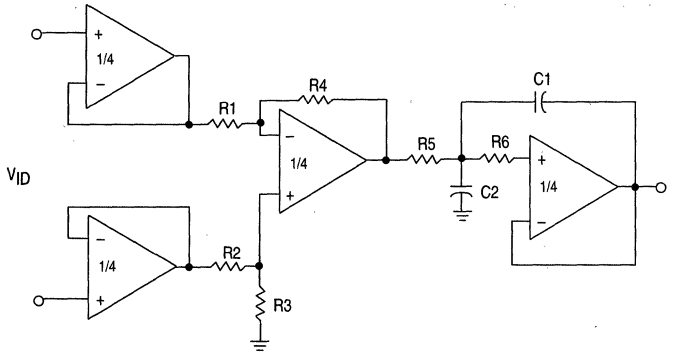


Figure 13. Function Generator

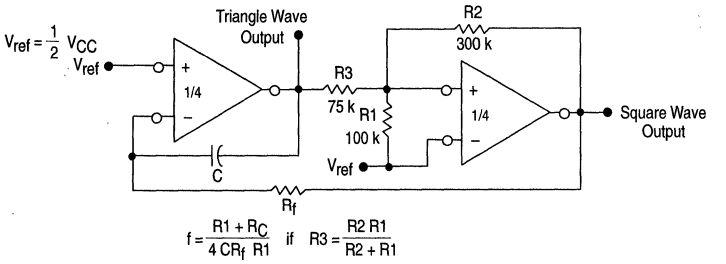


Figure 14. Bi–Quad Filter

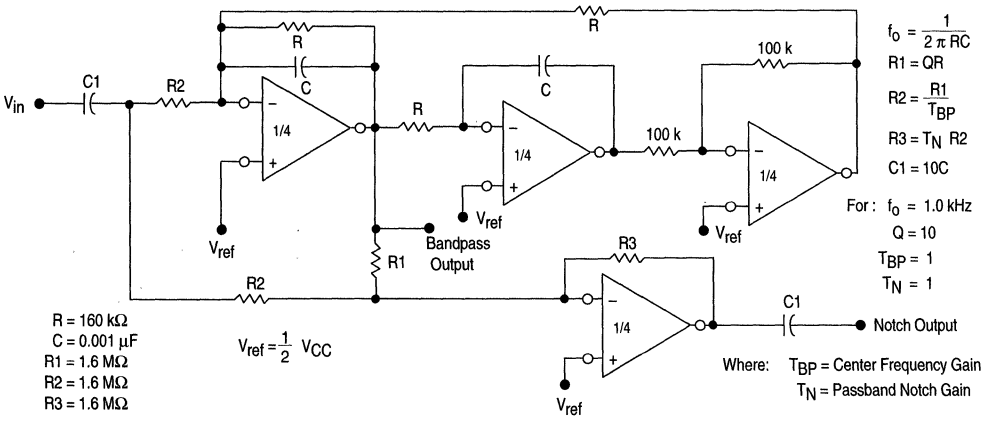
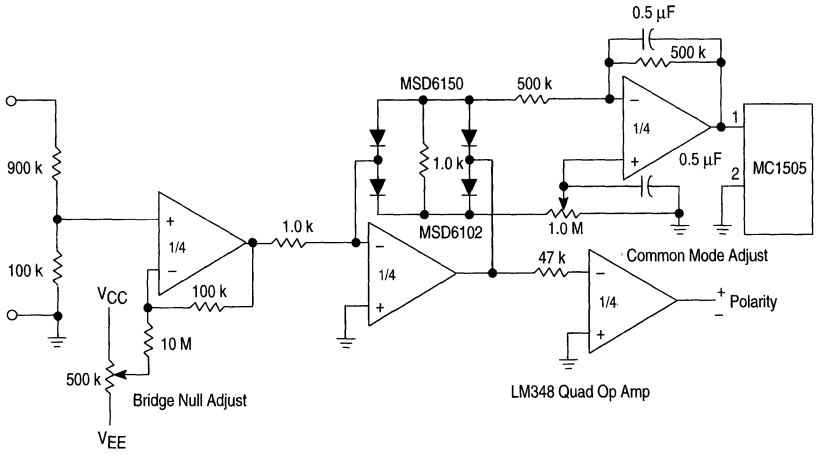


Figure 15. Absolute Value DVM Front End



LM358, LM258, LM2904, LM2904V

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

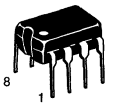
SEMICONDUCTOR TECHNICAL DATA

Dual Low Power Operational Amplifiers

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) single supply or split supply operation and 4) pinouts compatible with the popular MC1558 dual operational amplifier. The LM158 series is equivalent to one–half of an LM124.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 32 V, with quiescent currents about one–fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

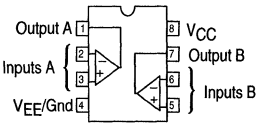
- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- Similar Performance to the Popular MC1558
- ESD Clamps on the Inputs Increase Ruggedness of the Device without Affecting Operation



N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM258 LM358	LM2904 LM2904V	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	 26 ±13	Vdc
Input Differential Voltage Range (Note 1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range (Note 2)	V_{ICR}	–0.3 to 32	–0.3 to 26	Vdc
Output Short Circuit Duration	t_{SC}	Continuous		
Junction Temperature	T_J	150		°C
Storage Temperature Range	T_{stg}	–55 to +125		°C
Operating Ambient Temperature Range LM258 LM358 LM2904 LM2904V	T_A	 –25 to +85 0 to +70 – –	 – – –40 to +105 –40 to +125	°C

NOTES: 1. Split Power Supplies.
2. For Supply Voltages less than 32 V for the LM258/358 and 26 V for the LM2904, the absolute maximum input voltage is equal to the supply voltage.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM2904D	T_A = –40° to +105°C	SO–8
LM2904N		Plastic DIP
LM2904VD	T_A = –40° to +125°C	SO–8
LM2904VN		Plastic DIP
LM258D	T_A = –25° to +85°C	SO–8
LM258N		Plastic DIP
LM358D	T_A = 0° to +70°C	SO–8
LM358N		Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

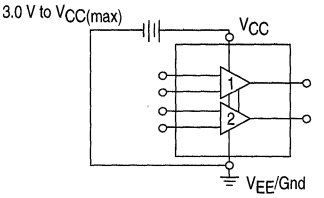
Characteristic	Symbol	LM258			LM358			LM2904			LM2904V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2904, V), V_{IC} = 0 V to V_{CC} −1.7 V, $V_O \cong$ 1.4 V, R_S = 0 Ω	V_{IO}													mV
T_A = 25°C		–	2.0	5.0	–	2.0	7.0	–	2.0	7.0	–	–	–	
T_A = T_{high} (Note 1)		–	–	7.0	–	–	9.0	–	–	10	–	–	13	
T_A = T_{low} (Note 1)		–	–	2.0	–	–	9.0	–	–	10	–	–	10	
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low} (Note 1)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	–	–	7.0	–	–	7.0	–	μV/°C
Input Offset Current	I_{IO}	–	3.0	30	–	5.0	50	–	5.0	50	–	5.0	50	nA
T_A = T_{high} to T_{low} (Note 1)		–	–	100	–	–	150	–	45	200	–	45	200	
Input Bias Current	I_{IB}	–	–45	–150	–	–45	–250	–	–45	–250	–	–45	–250	
T_A = T_{high} to T_{low} (Note 1)		–	–50	–300	–	–50	–500	–	–50	–500	–	–50	–500	
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low} (Note 1)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	–	10	–	pA/°C
Input Common Mode Voltage Range (Note 2), V_{CC} = 30 V (26 V for LM2904, V)	V_{ICR}	0	–	28.3	0	–	28.3	0	–	24.3	0	–	24.3	V
V_{CC} = 30 V (26 V for LM2904, V), T_A = T_{high} to T_{low}		0	–	28	0	–	28	0	–	24	0	–	24	
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open Loop Voltage Gain	A_{VOL}													V/mV
R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing,		50	100	–	25	100	–	25	100	–	25	100	–	
T_A = T_{high} to T_{low} (Note 1)		25	–	–	15	–	–	15	–	–	15	–	–	
Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	–	–120	–	–	–120	–	–	–120	–	–	–120	–	dB
Common Mode Rejection R_S ≤ 10 kΩ	CMR	70	85	–	65	70	–	50	70	–	50	70	–	dB
Power Supply Rejection	PSR	65	100	–	65	100	–	50	100	–	50	100	–	dB
Output Voltage–High Limit (T_A = T_{high} to T_{low}) (Note 1)	V_{OH}													V
V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C		3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	
V_{CC} = 30 V (26 V for LM2904, V), R_L = 2.0 kΩ		26	–	–	26	–	–	22	–	–	22	–	–	
V_{CC} = 30 V (26 V for LM2904, V), R_L = 10 kΩ		27	28	–	27	28	–	23	24	–	23	24	–	
Output Voltage–Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low} (Note 1)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	20	–	5.0	20	mV
Output Source Current V_{ID} = +1.0 V, V_{CC} = 15 V	I_{O+}	20	40	–	20	40	–	20	40	–	20	40	–	mA
Output Sink Current	I_{O-}													
V_{ID} = −1.0 V, V_{CC} = 15 V		10	20	–	10	20	–	10	20	–	10	20	–	mA
V_{ID} = −1.0 V, V_O = 200 mV		12	50	–	12	50	–	–	–	–	–	–	–	μA
Output Short Circuit to Ground (Note 3)	I_{SC}	–	40	60	–	40	60	–	40	60	–	40	60	mA
Power Supply Current (T_A = T_{high} to T_{low}) (Note 1)	I_{CC}													mA
V_{CC} = 30 V (26 V for LM2904, V), V_O = 0 V, R_L = ∞		–	1.5	3.0	–	1.5	3.0	–	1.5	3.0	–	1.5	3.0	
V_{CC} = 5 V, V_O = 0 V, R_L = ∞		–	0.7	1.2	–	0.7	1.2	–	0.7	1.2	–	0.7	1.2	

NOTES: 1. T_{low} = −40°C for LM2904
= −40°C for LM2904V
= −25°C for LM258
= 0°C for LM358
T_{high} = +105°C for LM2904
= +125°C for LM2904V
= +85°C for LM258
= +70°C for LM358

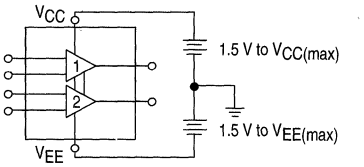
2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} −1.7 V.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

2

Single Supply

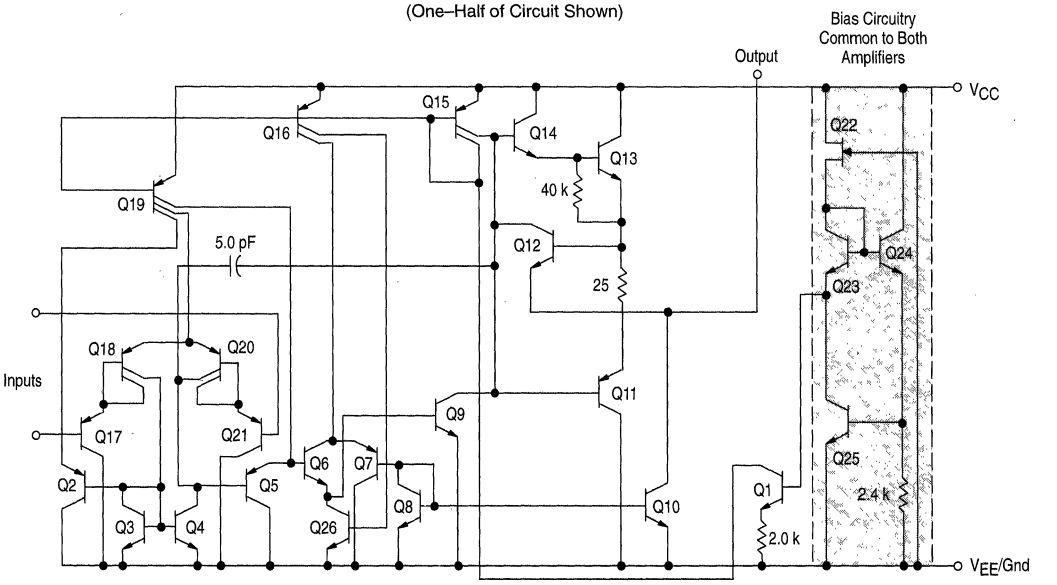


Split Supplies



Representative Schematic Diagram

(One–Half of Circuit Shown)



CIRCUIT DESCRIPTION

The LM258 series is made using two internally compensated, two–stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single–ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal–voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Large Signal Voltage Follower Response

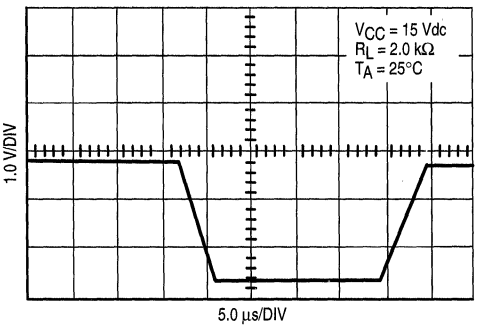


Figure 1. Input Voltage Range

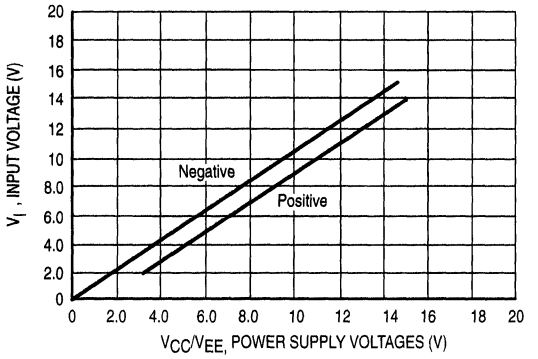


Figure 2. Large–Signal Open Loop Voltage Gain

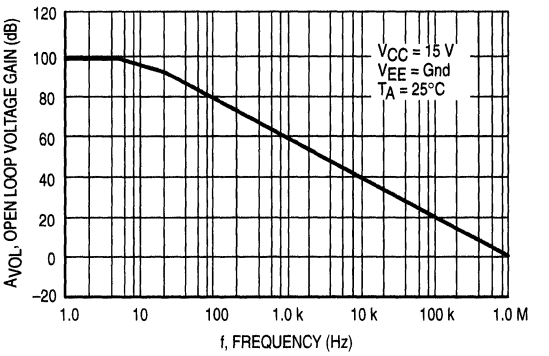


Figure 3. Large–Signal Frequency Response

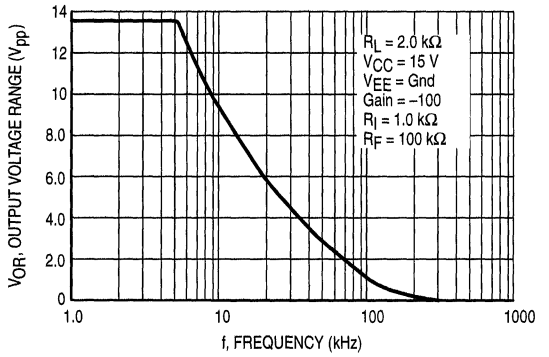


Figure 4. Small Signal Voltage Follower Pulse Response (Noninverting)

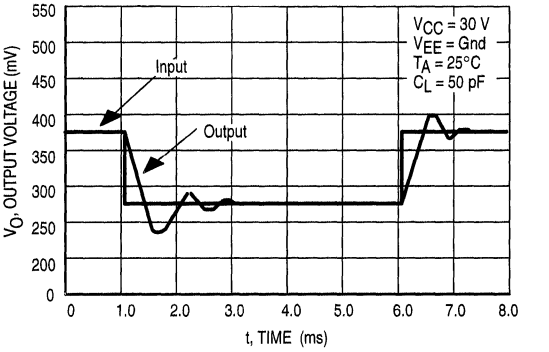


Figure 5. Power Supply Current versus Power Supply Voltage

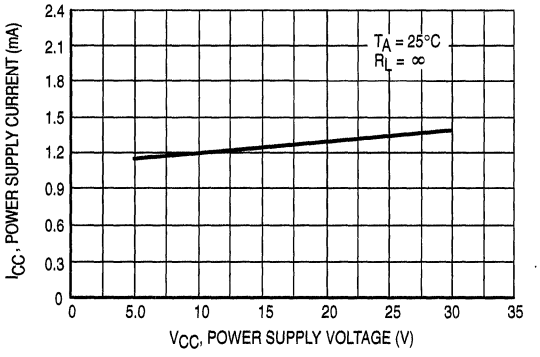
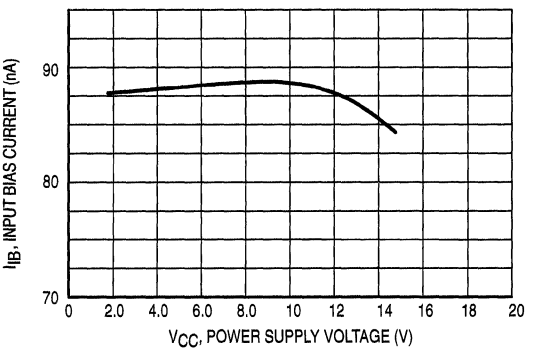
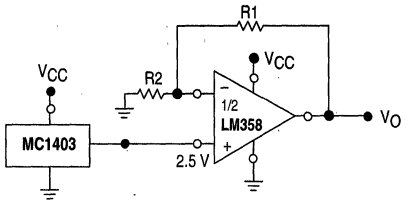


Figure 6. Input Bias Current versus Supply Voltage



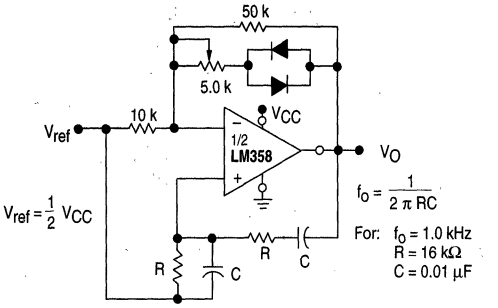
2

Figure 7. Voltage Reference



$$V_O = 2.5\,V\left(1 + \frac{R1}{R2}\right)$$

Figure 8. Wien Bridge Oscillator

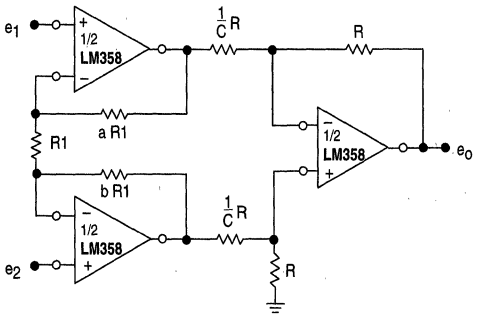


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_O = \frac{1}{2\pi RC}$$

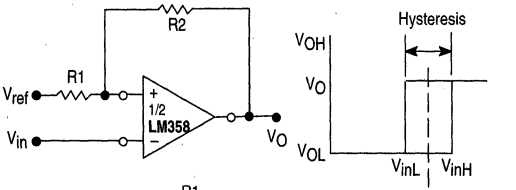
For: f_O = 1.0 kHz
R = 16 kΩ
C = 0.01 µF

Figure 9. High Impedance Differential Amplifier



$$e_o = C\,(1 + a + b)\,(e_2 - e_1)$$

Figure 10. Comparator with Hysteresis

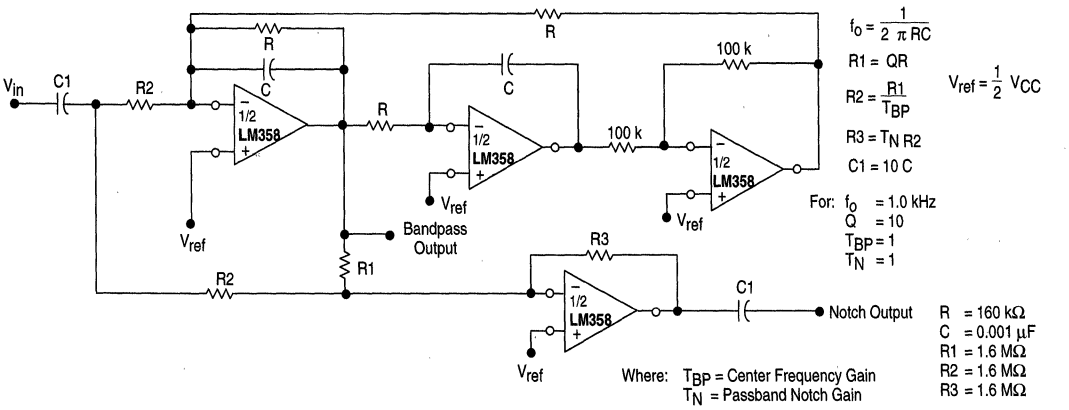


$$V_{inL} = \frac{R1}{R1 + R2}(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2}(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

Figure 11. Bi–Quad Filter



$$f_O = \frac{1}{2\pi RC}$$

R1 = QR

$$R2 = \frac{R1}{T_{BP}}$$

R3 = T_N R2

C1 = 10 C

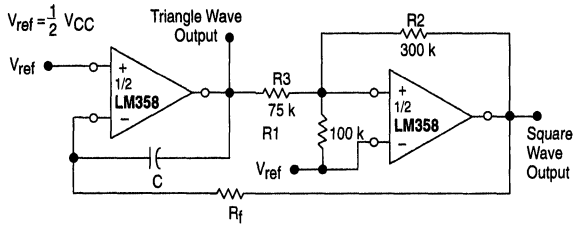
$$V_{ref} = \frac{1}{2} V_{CC}$$

For: f_O = 1.0 kHz
Q = 10
T_{BP} = 1
T_N = 1

R = 160 kΩ
C = 0.001 µF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

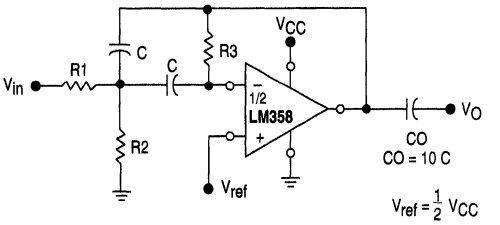
Where: T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

Figure 12. Function Generator



$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if, } R3 = \frac{R2\,R1}{R2 + R1}$$

Figure 13. Multiple Feedback Bandpass Filter



Given: f_o = center frequency
$A(f_o)$ = gain at center frequency

Choose value f_o, C

Then: $R3 = \frac{Q}{\pi f_o C}$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier. $\frac{Q_o f_o}{BW} < 0.1$

Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

LM393, LM393A, LM293, LM2903, LM2903V

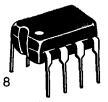
SINGLE SUPPLY, LOW POWER DUAL COMPARATORS

SEMICONDUCTOR TECHNICAL DATA

Low Offset Voltage Dual Comparators

The LM393 series are dual independent precision voltage comparators capable of single or split supply operation. These devices are designed to permit a common mode range–to–ground level with single supply operation. Input offset voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer automotive, and industrial electronics.

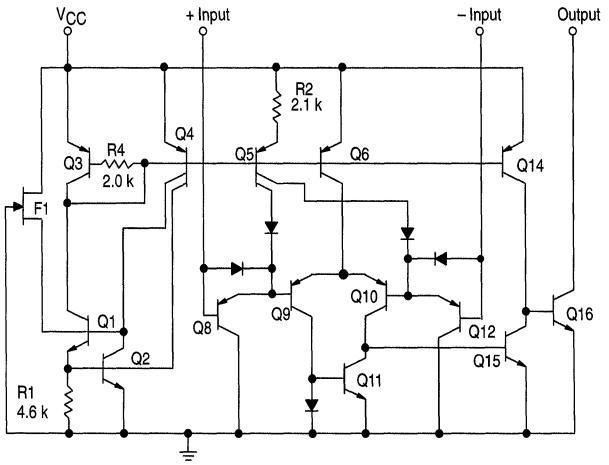
- Wide Single–Supply Range: 2.0 Vdc to 36 Vdc
- Split–Supply Range: ±1.0 Vdc to ±18 Vdc
- Very Low Current Drain Independent of Supply Voltage: 0.4 mA
- Low Input Bias Current: 25 nA
- Low Input Offset Current: 5.0 nA
- Low Input Offset Voltage: 2.0 mV (max) LM393A
  5.0 mV (max) LM293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS, and CMOS Logic Levels
- ESD Clamps on the Inputs Increase the Ruggedness of the Device without Affecting Performance



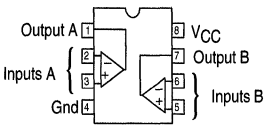
N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Representative Schematic Diagram
(Diagram shown is for 1 comparator)



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM293D	T_A = –25° to +85°C	SO–8
LM393D	T_A = 0° to +70°C	SO–8
LM393AN,N		Plastic DIP
LM2903D	T_A = –40° to +105°C	SO–8
LM2903N		Plastic DIP
LM2903VD	T_A = –40° to +105°C	SO–8
LM2903VN		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	–0.3 to +36	Vdc
Output Short Circuit–to–Ground Output Sink Current (Note 1)	I_{SC} I_{Sink}	Continuous 20	mA
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D $1/R_{\theta JA}$	570 5.7	mW mW/°C
Operating Ambient Temperature Range LM293 LM393, 393A LM2903 LM2903V	T_A	 –25 to +85 0 to +70 –40 to +105 –40 to +125	°C
Maximum Operating Junction Temperature LM393, 393A, 2903, LM2903V LM293	$T_{J(max)}$	 125 150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, $T_{low} \le T_A \le T_{high}$,* unless otherwise noted.)

Characteristic	Symbol	LM393A			Unit
		Min	Typ	Max	
Input Offset Voltage (Note 2) T_A = 25°C $T_{low} \le T_A \le T_{high}$	V_{IO}	 – –	 ±1.0 –	 ±2.0 4.0	mV
Input Offset Current T_A = 25°C $T_{low} \le T_A \le T_{high}$	I_{IO}	 – –	 ±50 –	 ±50 ±150	nA
Input Bias Current (Note 3) T_A = 25°C $T_{low} \le T_A \le T_{high}$	I_{IB}	 – –	 25 –	 250 400	nA
Input Common Mode Voltage Range (Note 4) T_A = 25°C $T_{low} \le T_A \le T_{high}$	V_{ICR}	 0 0	 – –	 V_{CC} –1.5 V_{CC} –2.0	V
Voltage Gain $R_L \ge 15$ kΩ, V_{CC} = 15 Vdc, T_A = 25°C	A_{VOL}	50	200	–	V/mV
Large Signal Response Time V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	–	–	300	–	ns
Response Time (Note 5) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	t_{TLH}	–	1.3	–	µs
Input Differential Voltage (Note 6) All $V_{in} \ge$ Gnd or V– Supply (if used)	V_{ID}	–	–	V_{CC}	V
Output Sink Current $V_{in} \ge$ 1.0 Vdc, V_{in+} = 0 Vdc, $V_O \le$ 1.5 Vdc, T_A = 25°C	I_{Sink}	6.0	16	–	mA
Output Saturation Voltage $V_{in} \ge$ 1.0 Vdc, V_{in+} = 0 Vdc, $I_{Sink} \le$ 4.0 mA, T_A = 25°C $T_{low} \le T_A \le T_{high}$	V_{OL}	 – –	 150 –	 400 700	mV

*T_{low} = 0°C, T_{high} = +70°C for LM393/393A

NOTES: 1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. At output switch point, $V_O \approx$ 1.4 Vdc, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common mode range (0 V to V_{CC} – 1.5 V).
3. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.
4. Input common mode of either input should not be permitted to go more than 0.3 V negative of ground or minus supply. The upper limit of common mode range is V_{CC} –1.5 V.
5. Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.
6. The comparator will exhibit proper output state if one of the inputs becomes greater than V_{CC}, the other input must remain within the common mode range. The low input state must not be less than –0.3 V of ground or minus supply.

2

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, $T_{low} \le T_A \le T_{high}$,* unless otherwise noted.)

Characteristic	Symbol	LM393A			Unit
		Min	Typ	Max	
Output Leakage Current	I_{OL}				μA
V_{in-} = 0 V, $V_{in+} \ge$ 1.0 Vdc, V_O = 5.0 Vdc, T_A = 25°C		–	0.1	–	
V_{in-} = 0 V, $V_{in+} \ge$ 1.0 Vdc, V_O = 30 Vdc, $T_{low} \le T_A \le T_{high}$		–	–	1.0	
Supply Current	I_{CC}				mA
R_L = ∞ Both Comparators, T_A = 25°C		–	0.4	1.0	
R_L = ∞ Both Comparators, V_{CC} = 30 V		–	1.0	2.5	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, $T_{low} \le T_A \le T_{high}$, unless otherwise noted.)

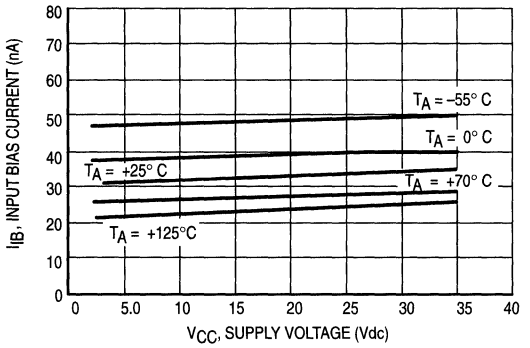
Characteristic	Symbol	LM392, LM393			LM2903, LM2903V			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 2)	V_{IO}							mV
T_A = 25°C		–	±1.0	±5.0	–	±2.0	±7.0	
$T_{low} \le T_A \le T_{high}$		–	–	9.0	–	9.0	15	
Input Offset Current	I_{IO}							nA
T_A = 25°C		–	±5.0	±50	–	±5.0	±50	
$T_{low} \le T_A \le T_{high}$		–	–	±150	–	±50	±200	
Input Bias Current (Note 3)	I_{IB}							nA
T_A = 25°C		–	25	250	–	25	250	
$T_{low} \le T_A \le T_{high}$		–	–	400	–	200	500	
Input Common Mode Voltage Range (Note 3)	V_{ICR}							V
T_A = 25°C		0	–	V_{CC} –1.5	0	–	V_{CC} –1.5	
$T_{low} \le T_A \le T_{high}$		0	–	V_{CC} –2.0	0	–	V_{CC} –2.0	
Voltage Gain	A_{VOL}	50	200	–	25	200	–	V/mV
$R_L \ge$ 15 kΩ, V_{CC} = 15 Vdc, T_A = 25°C								
Large Signal Response Time	–	–	300	–	–	300	–	ns
V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc								
V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C								
Response Time (Note 5)	t_{TLH}	–	1.3	–	–	1.5	–	μs
V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C								
Input Differential Voltage (Note 6)	V_{ID}	–	–	V_{CC}	–	–	V_{CC}	V
All $V_{in} \ge$ Gnd or V– Supply (if used)								
Output Sink Current	I_{Sink}	6.0	16	–	6.0	16	–	mA
$V_{in} \ge$ 1.0 Vdc, V_{in+} = 0 Vdc, $V_O \le$ 1.5 Vdc T_A = 25°C								
Output Saturation Voltage	V_{OL}							mV
$V_{in} \ge$ 1.0 Vdc, V_{in+} = 0, $I_{Sink} \le$ 4.0 mA, T_A = 25°C		–	150	400	–	–	400	
$T_{low} \le T_A \le T_{high}$		–	–	700	–	200	700	
Output Leakage Current	I_{OL}							nA
V_{in-} = 0 V, $V_{in+} \ge$ 1.0 Vdc, V_O = 5.0 Vdc, T_A = 25°C		–	0.1	–	–	0.1	–	
V_{in-} = 0 V, $V_{in+} \ge$ 1.0 Vdc, V_O = 30 Vdc,								
$T_{low} \le T_A \le T_{high}$		–	–	1000	–	–	1000	
Supply Current	I_{CC}							mA
R_L = ∞ Both Comparators, T_A = 25°C		–	0.4	1.0	–	0.4	1.0	
R_L = ∞ Both Comparators, V_{CC} = 30 V		–	–	2.5	–	–	2.5	

*T_{low} = 0°C, T_{high} = +70°C for LM393/393A
LM293 T_{low} = –25°C, T_{high} = +85°C
LM2903 T_{low} = –40°C, T_{high} = +105°C
LM2903V T_{low} = –40°C, T_{high} = +125°C

NOTES: 2. At output switch point, V_O = 1.4 Vdc, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common mode range (0 V to V_{CC} = –1.5 V).
3. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.
5. Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.
6. The comparator will exhibit proper output state if one of the inputs becomes greater than V_{CC}, the other input must remain within the common mode range. The low input state must not be less than –0.3 V of ground or minus supply.

LM293/393,A

Figure 1. Input Bias Current versus Power Supply Voltage



LM2903

Figure 2. Input Bias Current versus Power Supply Voltage

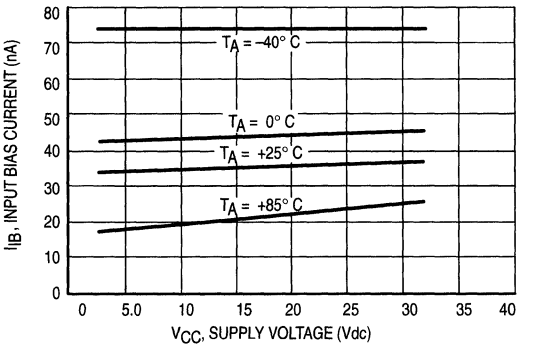


Figure 3. Output Saturation Voltage versus Output Sink Current

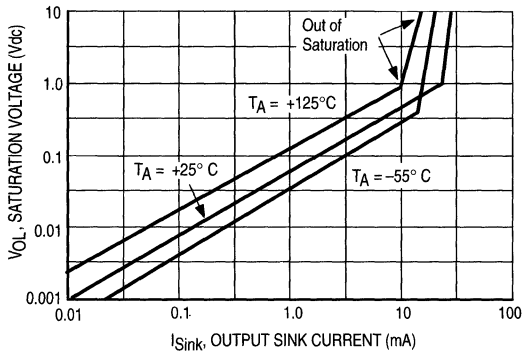


Figure 4. Output Saturation Voltage versus Output Sink Current

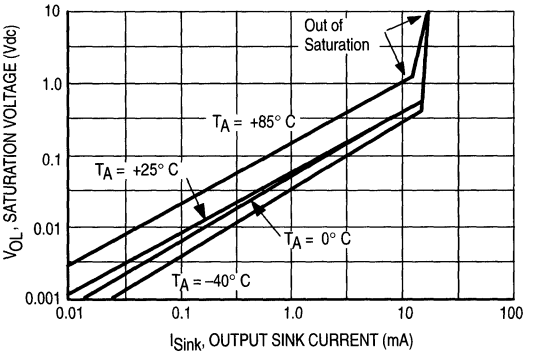


Figure 5. Power Supply Current versus Power Supply Voltage

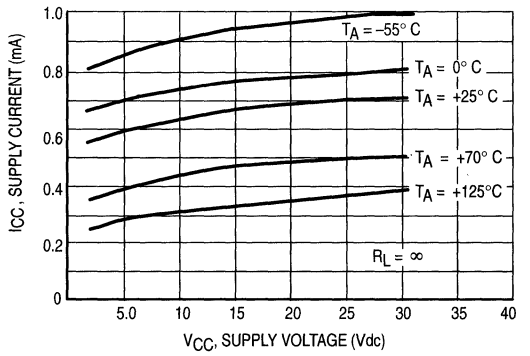
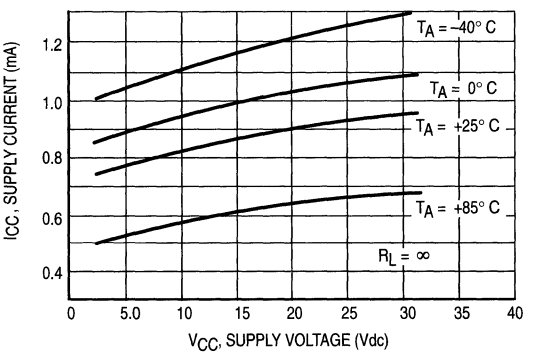


Figure 6. Power Supply Current versus Power Supply Voltage



2

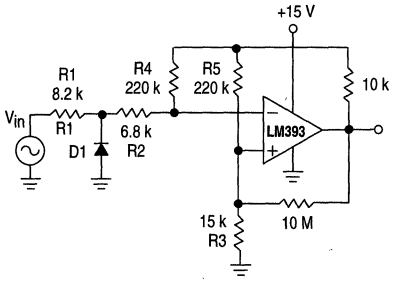
APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation, input resistors < 10 kΩ should be used.

The addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than –0.3 V should not be used.

Figure 7. Zero Crossing Detector (Single Supply)

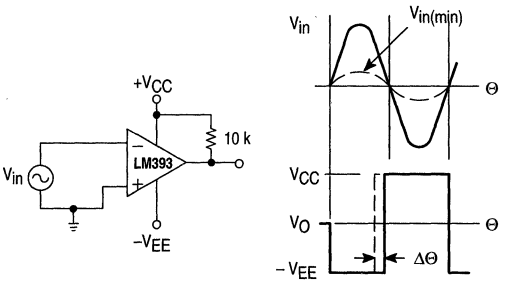


D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10}$$ for small error in zero crossing.

Figure 8. Zero Crossing Detector (Split Supply)



$V_{in(min)} \approx 0.4$ V peak for 1% phase distortion (ΔΘ).

Figure 9. Free–Running Square–Wave Oscillator

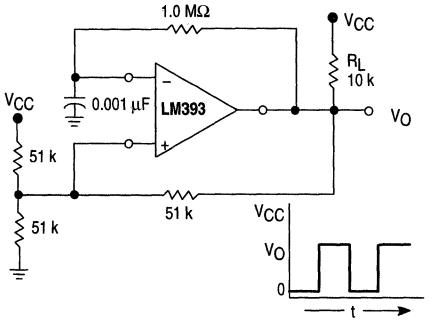
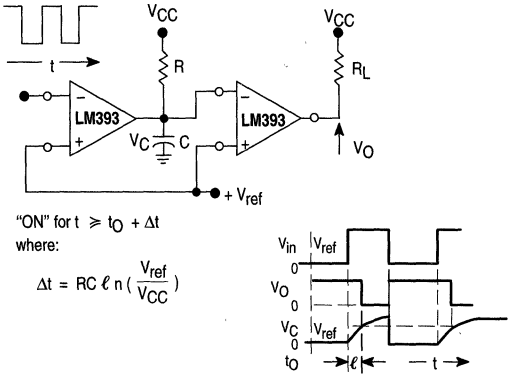


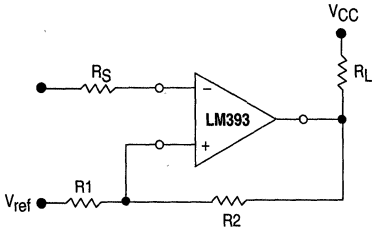
Figure 10. Time Delay Generator



"ON" for $t \geq t_O + \Delta t$
where:

$$\Delta t = RC\,\ell n\left(\frac{V_{ref}}{V_{CC}}\right)$$

Figure 11. Comparator with Hysteresis



$$R_S = R1 \,||\, R2$$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref})\ R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_{O\,Low})\ R1}{R1 + R2}$$

LM833

Dual Low Noise, Audio Amplifier

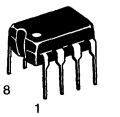
The LM833 is a standard low–cost monolithic dual general–purpose operational amplifier employing Bipolar technology with innovative high–performance concepts for audio systems applications. With high frequency PNP transistors, the LM833 offers low voltage noise (4.5 nV/$\sqrt{Hz}$), 15 MHz gain bandwidth product, 7.0 V/μs slew rate, 0.3 mV input offset voltage with 2.0 μV/°C temperature coefficient of input offset voltage. The LM833 output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The LM833 is specified over the automotive temperature range and is available in the plastic DIP and SO–8 packages (P and D suffixes). For an improved performance dual/quad version, see the MC33079 family.

- Low Voltage Noise: 4.5 nV/$\sqrt{Hz}$
- High Gain Bandwidth Product: 15 MHz
- High Slew Rate: 7.0 V/μs
- Low Input Offset Voltage: 0.3 mV
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Distortion: 0.002%
- Excellent Frequency Stability
- Dual Supply Operation

DUAL OPERATIONAL AMPLIFIER

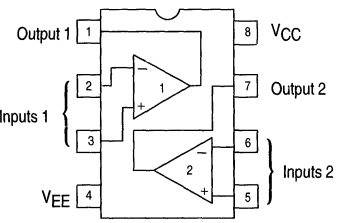
SEMICONDUCTOR TECHNICAL DATA



N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	30	V
Input Voltage Range (Note 1)	V_{IR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation (Notes 2 and 3)	P_D	500	mW

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see power dissipation performance characteristic).
3. Maximum value at $T_A \leq 85°C$.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM833N	$T_A = -40°$ to +85°C	Plastic DIP
LM833D		SO–8

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_O = 0 V)	V_{IO}	–	0.3	5.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	–	2.0	–	μV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}	–	10	200	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}	–	300	1000	nA
Common Mode Input Voltage Range	V_{ICR}	– −12	+14 −14	+12 –	V
Large Signal Voltage Gain (R_L = 2.0 kΩ, V_O = ±10 V	A_{VOL}	90	110	–	dB
Output Voltage Swing: R_L = 2.0 kΩ, V_{ID} = 1.0 V R_L = 2.0 kΩ, V_{ID} = 1.0 V R_L = 10 kΩ, V_{ID} = 1.0 V R_L = 10 kΩ, V_{ID} = 1.0 V	 V_{O+} V_{O-} V_{O+} V_{O-}	 10 – 12 –	 13.7 −14.1 13.9 −14.7	 – −10 – −12	V
Common Mode Rejection (V_{in} = ±12 V)	CMR	80	100	–	dB
Power Supply Rejection (V_S = 15 V to 5.0 V, −15 V to −5.0 V)	PSR	80	115	–	dB
Power Supply Current (V_O = 0 V, Both Amplifiers)	I_D	–	4.0	8.0	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, A_V = +1.0)	S_R	5.0	7.0	–	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	10	15	–	MHz
Unity Gain Frequency (Open Loop)	f_U	–	9.0	–	MHz
Unity Gain Phase Margin (Open Loop)	θ_m	–	60	–	Deg
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n	–	4.5	–	nV/$\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	i_n	–	0.5	–	pA/$\sqrt{Hz}$
Power Bandwidth (V_O = 27 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)	BWP	–	120	–	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	THD	–	0.002	–	%
Channel Separation (f = 20 Hz to 20 kHz)	C_S	–	−120	–	dB

Figure 1. Maximum Power Dissipation versus Temperature

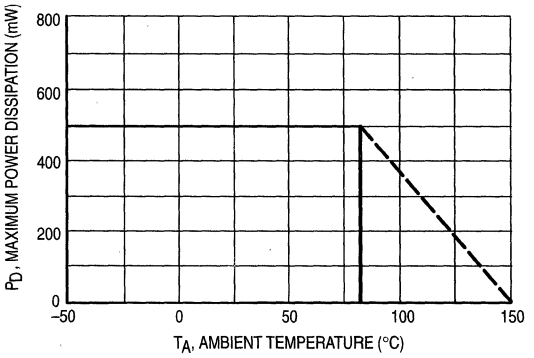


Figure 2. Input Bias Current versus Temperature

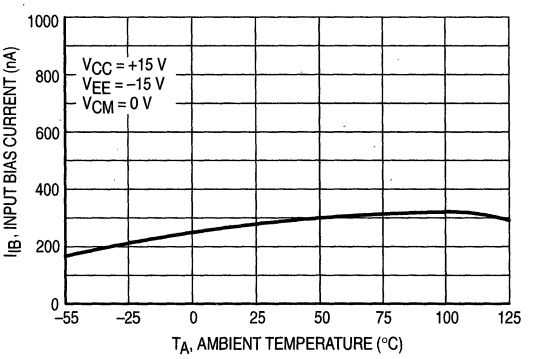


Figure 3. Input Bias Current versus Supply Voltage

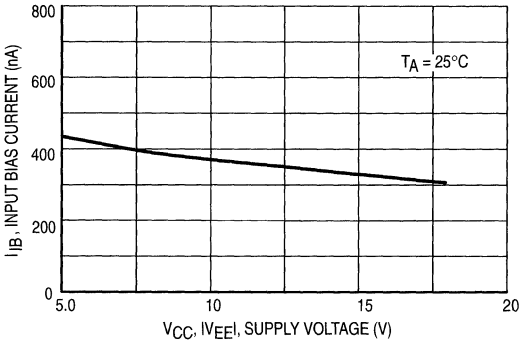


Figure 4. Supply Current versus Supply Voltage

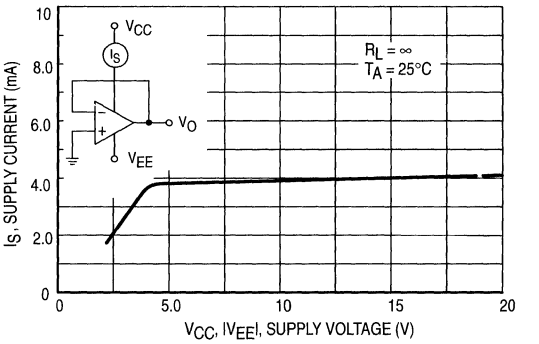


Figure 5. DC Voltage Gain versus Temperature

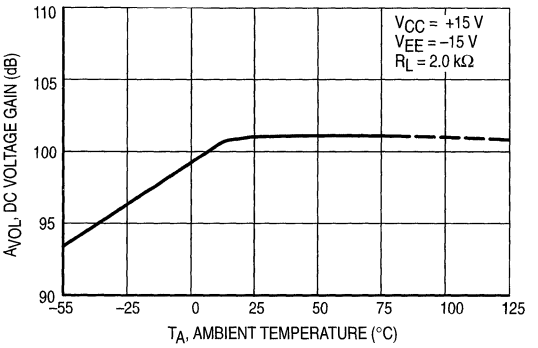


Figure 6. DC Voltage Gain versus Supply Voltage

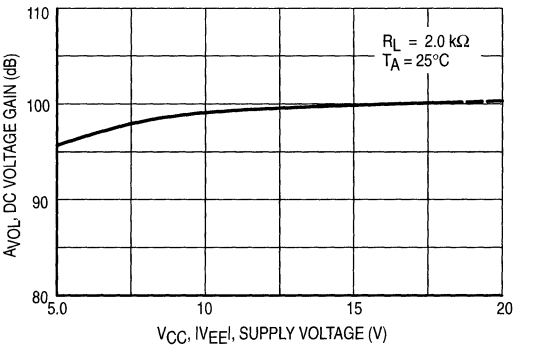


Figure 7. Open Loop Voltage Gain and Phase versus Frequency

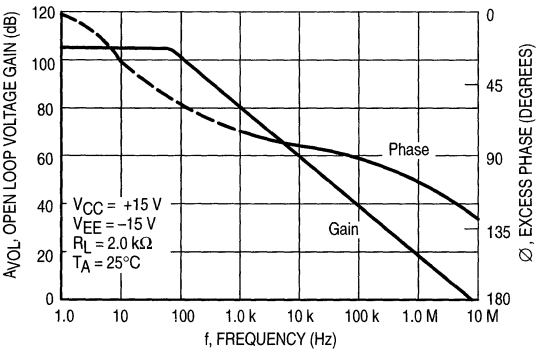
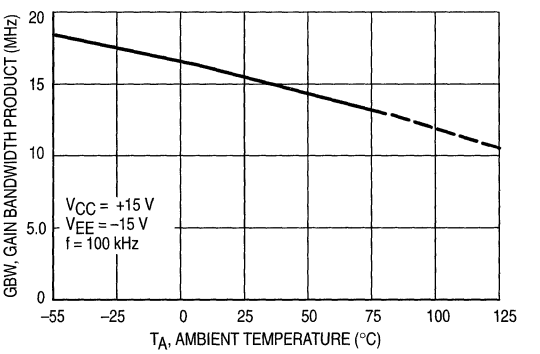


Figure 8. Gain Bandwidth Product versus Temperature



2

Figure 9. Gain Bandwidth Product versus Supply Voltage

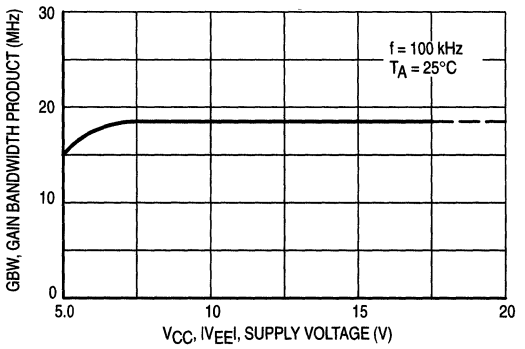


Figure 10. Slew Rate versus Temperature

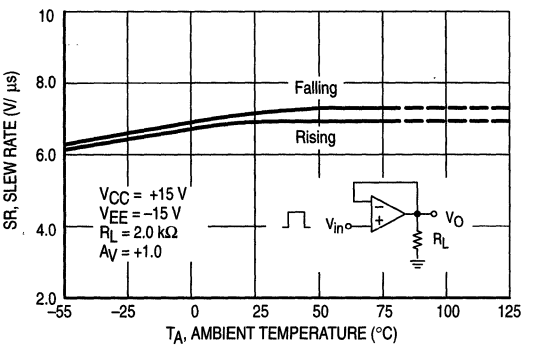


Figure 11. Slew Rate versus Supply Voltage

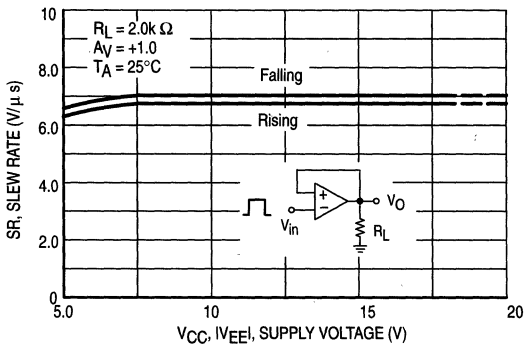


Figure 12. Output Voltage versus Frequency

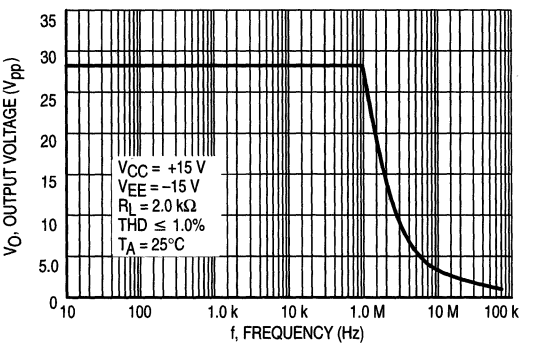


Figure 13. Maximum Output Voltage versus Supply Voltage

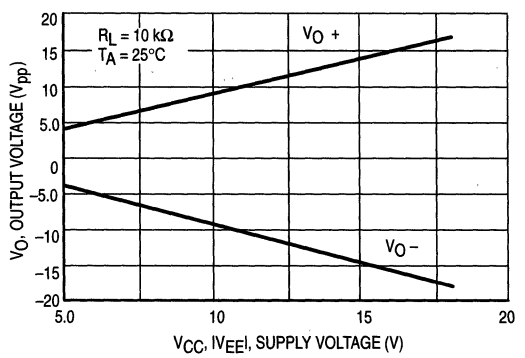


Figure 14. Output Saturation Voltage versus Temperature

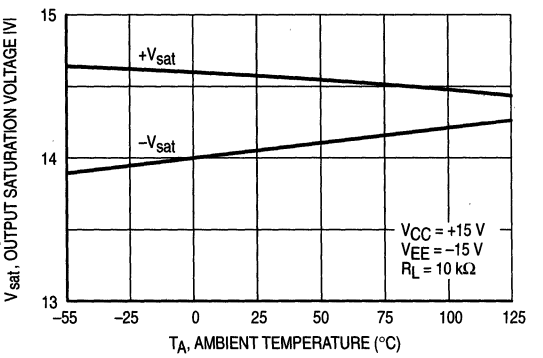


Figure 15. Power Supply Rejection versus Frequency

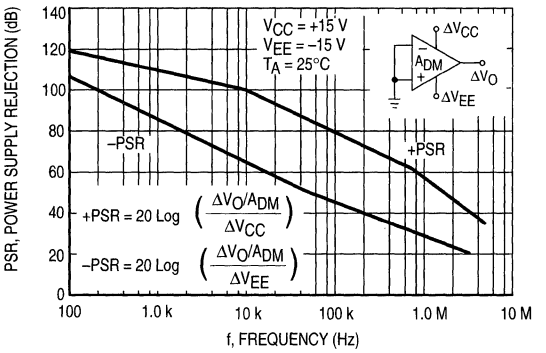


Figure 16. Common Mode Rejection versus Frequency

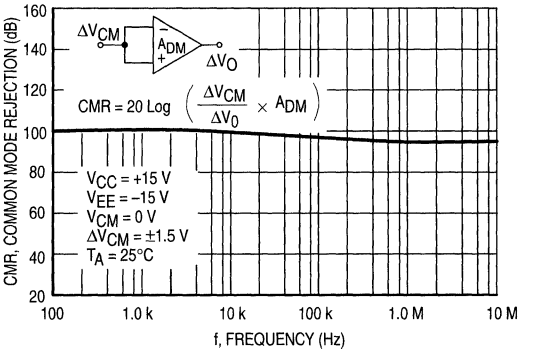


Figure 17. Total Harmonic Distortion versus Frequency

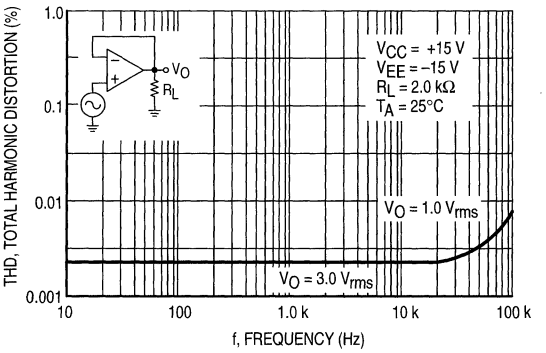


Figure 18. Input Referred Noise Voltage versus Frequency

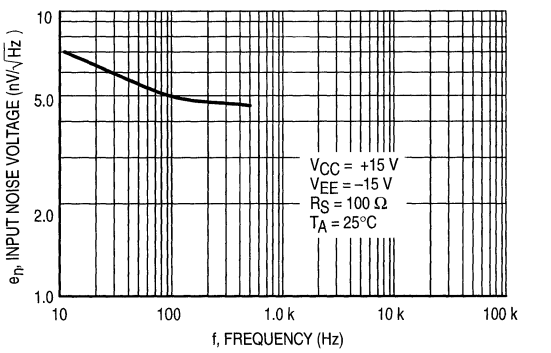


Figure 19. Input Referred Noise Current versus Frequency

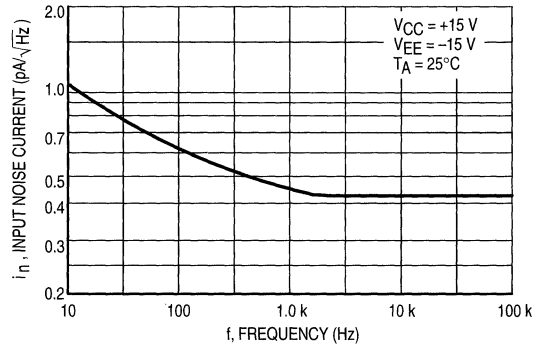
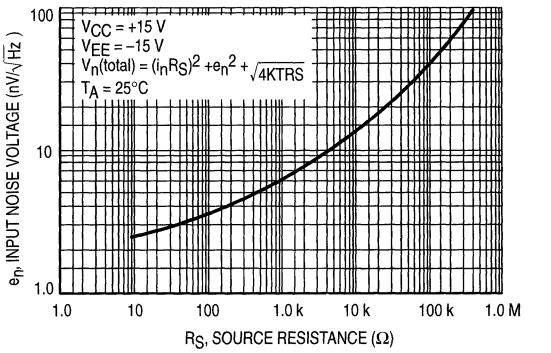


Figure 20. Input Referred Noise Voltage versus Source Resistance



2

Figure 21. Inverting Amplifier

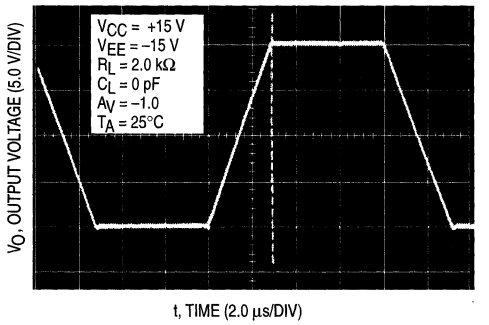


Figure 22. Noninverting Amplifier Slew Rate

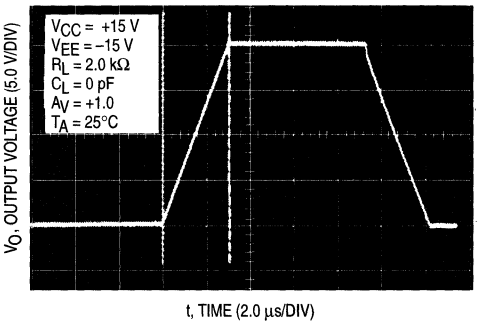
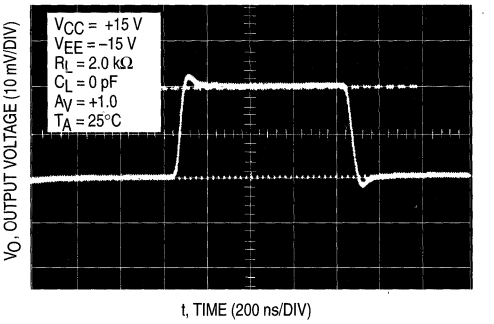


Figure 23. Noninverting Amplifier Overshoot



MC1436, C

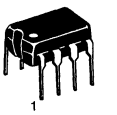
High Voltage, Internally Compensated Operational Amplifiers

The MC1436, C was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Output Voltage Swing:
  ±22 $V_{pk(min)}$ (V_{CC} = +28 V, V_{EE} = −28 V)
- Fast Slew Rate: 2.0 V/μs Typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Overvoltage Protection
- A_{VOL}: 500,000 Typ
- Characteristics Independent of Power Supply Voltages:
  (±5.0 Vdc to ±36 Vdc)

OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Figure 1. Differential Amplifier with ±20 V Common Mode Input Voltage Range

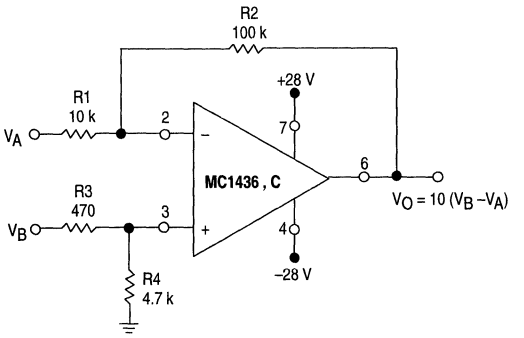
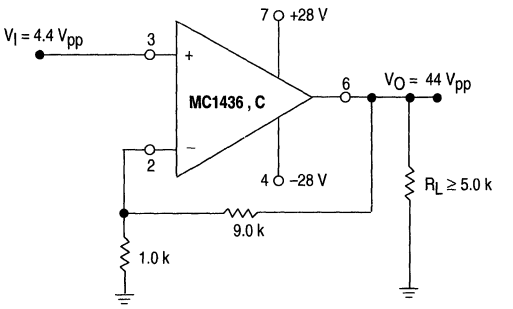
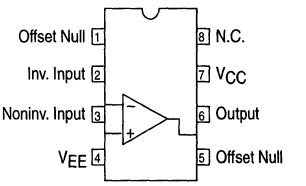


Figure 2. Typical Noninverting X10 Voltage Amplifier



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1436CD,D	T_A = 0° to +70°C	SO–8
MC1436CP1,P1		Plastic DIP

2

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	MC1436	MC1436C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+34 –34	+30 –30	Vdc
Input Differential Voltage Range	V_{IDR}	Note 2		V
Input Common Mode Voltage Range	V_{ICR}	Note 2		V
Output Short Circuit Duration (V_{CC} = V_{EE} = 28 Vdc, V_O = 0)	t_{SC}	5.0		sec
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6		mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70		°C
Storage Temperature Range	T_{stg}	–65 to +150		°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +28 V, V_{EE} = –28 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC1436			MC1436C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_{IB}							nAdc
T_A = +25°C		–	15	40	–	25	90	
T_A = T_{low} to T_{high} (See Note 1)		–	–	55	–	–	–	
Input Offset Current	I_{IO}							nAdc
T_A = +25°C		–	5.0	10	–	10	25	
T_A = +25°C to T_{high}		–	–	14	–	–	–	
T_A = T_{low} to +25°C		–	–	14	–	–	–	
Input Offset Voltage	V_{IO}							mVdc
T_A = +25°C		–	5.0	10	–	5.0	12	
T_A = T_{low} to T_{high}		–	–	14	–	–	–	
Differential Input Impedance (Open loop, f ≤ 5.0 Hz)								MΩ
Parallel Input Resistance	rp	–	10	–	–	10	–	pF
Parallel Input Capacitance	Cp	–	2.0	–	–	2.0	–	
Common Mode Input Impedance (f ≤ 5.0 Hz)	z_{ic}	–	250	–	–	250	–	MΩ
Input Common Mode Voltage Range	V_{ICR}	±22	±25	–	±18	±20	–	Vpk
Equivalent Input Noise Voltage (A_V = 100, R_S = 10 kΩ, f = 1.0 kHz, BW = 1.0 Hz)	e_n	–	50	–	–	50	–	$nV/(Hz)^{1/2}$
Common Mode Rejection (DC)	CMR	70	110	–	50	90	–	dB
Large Signal DC Open Loop Voltage Gain	A_{VOL}							V/V
(V_O = ±10 V, R_L = 100 kΩ) T_A = +25°C		70,000	500,000	–	50,000	500,000	–	
T_A = T_{low} to T_{high}		50,000	–	–	–	–	–	
(V_O = ±10 V, R_L = 10 kΩ, T_A = +25°C)		–	200,000	–	–	200,000	–	
Power Bandwidth (Voltage Follower)	BWp							kHz
(A_V = 1, R_L = 5.0 kΩ, THD ≤ 5%, V_O = 40 V_{pp})		–	23	–	–	23	–	
Unity Gain Crossover Frequency (Open loop)	f_c	–	1.0	–	–	1.0	–	MHz
Phase Margin (Open loop, Unity Gain)	ϕ_m	–	50	–	–	50	–	Degrees
Gain Margin	A_M	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)	SR	–	2.0	–	–	2.0	–	V/μs
Output Impedance (f ≤ 5.0 Hz)	z_O	–	1.0	–	–	1.0	–	kΩ
Short Circuit Output Current	I_{SC}	–	±17	–	–	±19	–	mAdc

NOTES: 1. T_{low} = 0°C for MC1436,C T_{high} = +70°C for MC1436,C
2. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE} +3.0 V.

ELECTRICAL CHARACTERISTICS (V_{CC} = +28 V, V_{EE} = −28 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC1436 Min	MC1436 Typ	MC1436 Max	MC1436C Min	MC1436C Typ	MC1436C Max	Unit
Output Voltage Range (R_L = 5.0 kΩ) V_{CC} = +28 Vdc, V_{EE} = −28 Vdc V_{CC} = +36 Vdc, V_{EE} = −36 Vdc	V_O	 ±20 –	 ±22 –	 – –	 ±20 –	 ±22 –	 – –	V_{pk}
Power Supply Rejection V_{EE} = Constant, $R_S \leq 10$ kΩ V_{CC} = Constant, $R_S \leq 10$ kΩ	 PSR + PSR –	 – –	 35 35	 200 200	 – –	 50 50	 – –	μV/V
Power Supply Current (See Note 2)	I_{CC} I_{EE}	– –	2.6 2.6	5.0 5.0	– –	2.6 2.6	5.0 5.0	mAdc
DC Quiescent Power Consumption (V_O = 0)	P_C	–	146	280	–	146	280	mW

NOTES: 2. V_{CC} = V_{EE} = 5.0 Vdc to 30 Vdc for MC1436
V_{CC} = V_{EE} = 5.0 Vdc to 28 Vdc for MC1436C

Figure 3. Low–Drift Sample and Hold

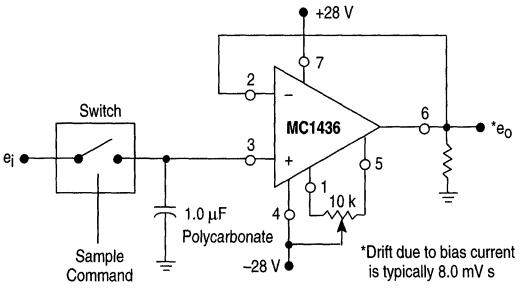


Figure 4. Power Bandwidth

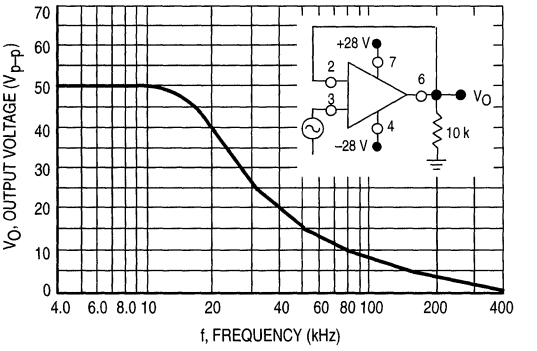


Figure 5. Peak Output Voltage Swing versus Power Supply Voltage

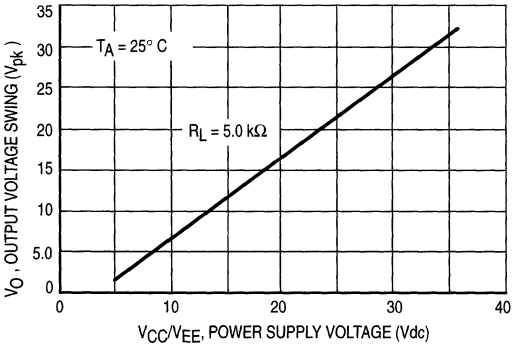
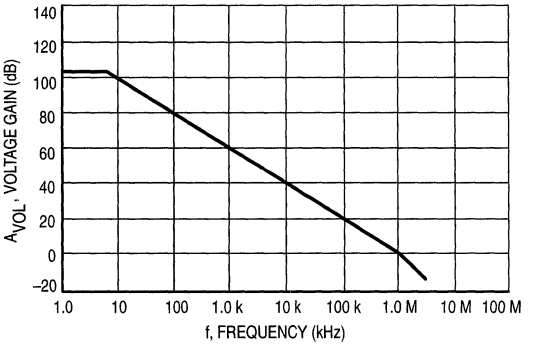


Figure 6. Open Loop Frequency Response



2

Figure 7. Output Short Circuit Current versus Temperature

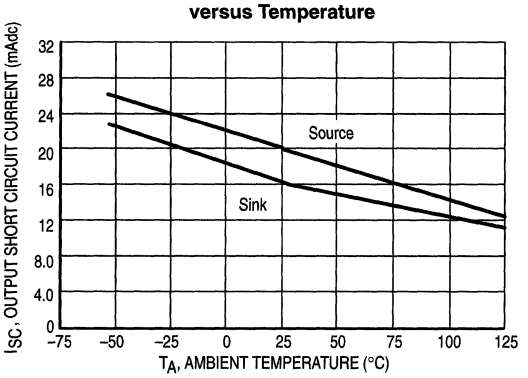


Figure 8. Input Bias Current versus Temperature

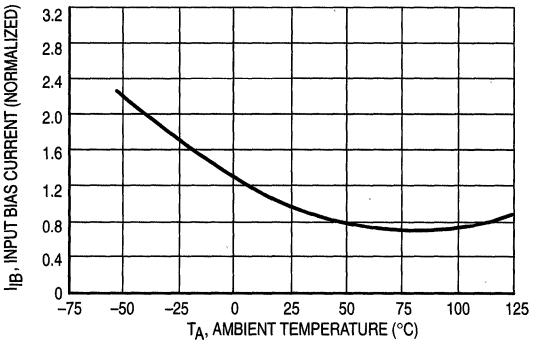
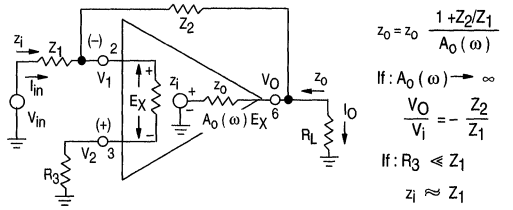


Figure 9. Inverting Feedback Model



$$z_o = z_o \frac{1 + Z_2/Z_1}{A_o(\omega)}$$

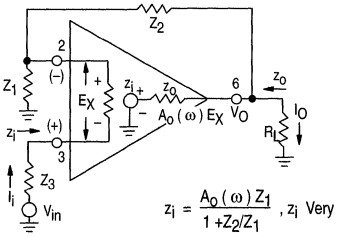
If : $A_o(\omega) \rightarrow \infty$

$$\frac{V_O}{V_i} = -\frac{Z_2}{Z_1}$$

If : $R_3 \ll Z_1$

$z_i \approx Z_1$

Figure 10. Noninverting Feedback Model



$$z_i = \frac{A_o(\omega) Z_1}{1 + Z_2/Z_1}, \; z_i \text{ Very High}$$

$$z_o = z_o \frac{1 + Z_2/Z_1}{A_o(\omega)}$$

$$\frac{V_O}{V_i} = 1 + Z_2/Z_1, \text{ when } A_O(\omega) \rightarrow \infty$$

$Z_o \rightarrow 0$

$A_o(\omega) \rightarrow \infty$

Figure 11. Audio Amplifier

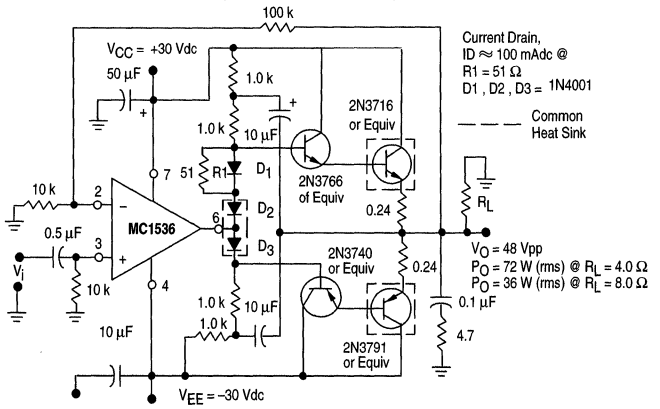


Figure 12. Voltage Controlled Current Source or Transconductance Amplifier with 0 V to 40 V Compliance

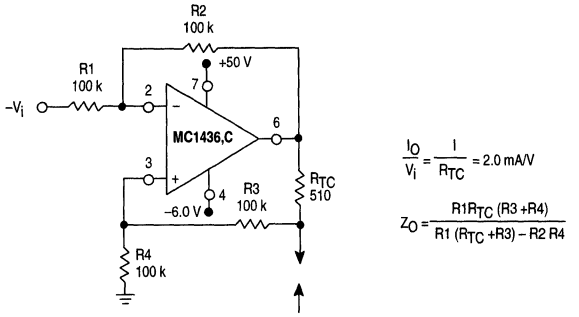


Figure 13. Representative Schematic Diagram

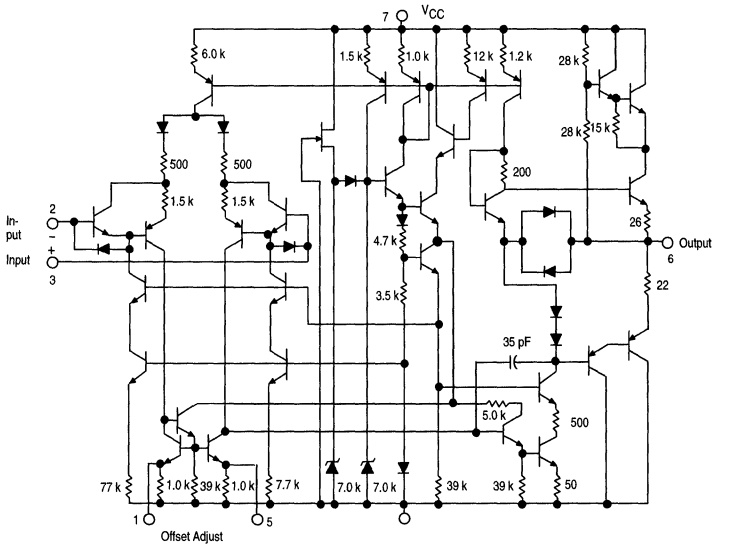
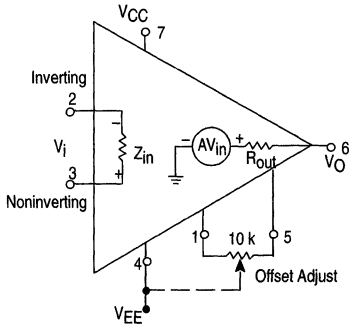


Figure 14. Equivalent Circuit



MC1458, C

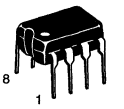
Internally Compensated, High Performance Dual Operational Amplifiers

DUAL OPERATIONAL AMPLIFIERS
(DUAL MC1741)

SEMICONDUCTOR TECHNICAL DATA

The MC1458, C was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short Circuit Protection
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch–Up



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

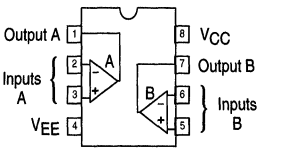
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±30	V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Junction Temperature	T_J	150	°C

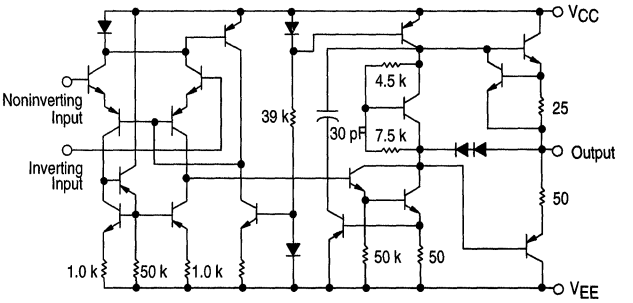
NOTES: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

PIN CONNECTIONS



(Top View)

Representative Schematic Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1458CD, D	T_A = 0° to +70°C	SO–8
MC1458CP1, P1		Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted. (Note 3))

Characteristic	Symbol	MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	–	2.0	6.0	–	2.0	1.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	300	nA
Input Bias Current	I_{IB}	–	80	500	–	80	700	nA
Input Resistance	r_i	0.3	2.0	–	–	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±11	±13	–	V
Large Signal Voltage Gain	A_{VOL}							V/mV
(V_O = ±10 V, R_L = 2.0 k)		20	200	–	–	–	–	
(V_O = ±10 V, R_L = 10 k)		–	–	–	20	200	–	
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection ($R_S \leq 10$ k)	CMR	70	90	–	60	90	–	dB
Supply Voltage Rejection ($R_S \leq 10$ k)	PSR	–	30	150	–	30	–	μV/V
Output Voltage Swing	V_O							V
($R_S \leq 10$ k)		±12	±14	–	±11	±14	–	
($R_S \leq 2.0$ k)		±10	±13	–	±9.0	±13	–	
Output Short Circuit Current	I_{SC}	–	20	–	–	20	–	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.6	–	2.3	8.0	mA
Power Consumption	P_C	–	70	170	–	70	240	mW
Transient Response (Unity Gain)								
(V_I = 20 mV, $R_L \geq 2.0$ kΩ, $C_L \leq 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, $R_L \geq 2.0$ kΩ, $C_L \leq 100$ pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \geq 2.0$ kΩ, $C_L \leq 100$ pF) Slew Rate	SR	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low}, unless otherwise noted. (Note 3))*

Characteristic	Symbol	MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	–	7.5	–	–	12	mV
Input Offset Current (T_A = 0° to +70°C)	I_{IO}	–	–	300	–	–	400	nA
Input Bias Current (T_A = 0° to +70°C)	I_{IB}	–	–	800	–	–	1000	nA
Output Voltage Swing	V_O							V
($R_s \leq 10$ k)		±12	±14	–	–	–	–	
($R_s \leq 2$ k)		±10	±13	–	±9.0	±13	–	
Large Signal Voltage Gain	A_{VOL}							V/mV
(V_O = ±10 V, R_L = 2 k)		15	–	–	–	–	–	
(V_O = ±10 V, R_L = 10 k)		–	–	–	15	–	–	

*T_{low} = 0°C for MC1458, C T_{high} = +70°C for MC1458, C

NOTE: 3. Input pins of an unused amplifier must be grounded for split supply operation or biased at least 3.0 V above V_{EE} for single supply operation.

2

Figure 1. Burst Noise versus Source Resistance

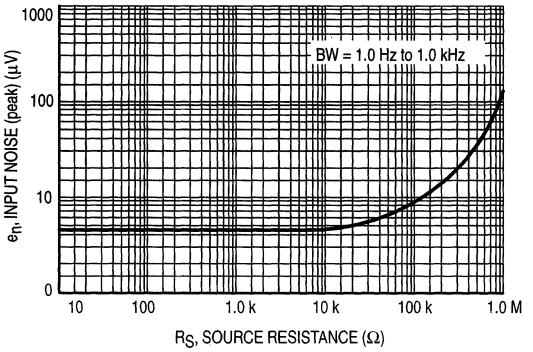


Figure 2. RMS Noise versus Source Resistance

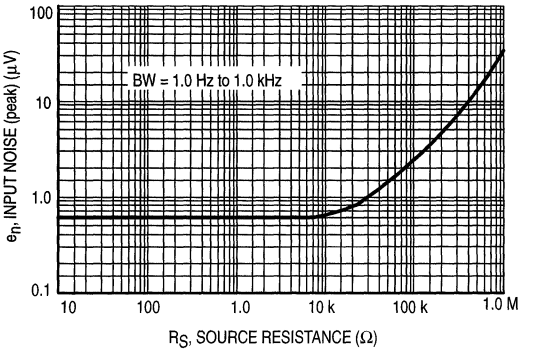


Figure 3. Output Noise versus Source Resistance

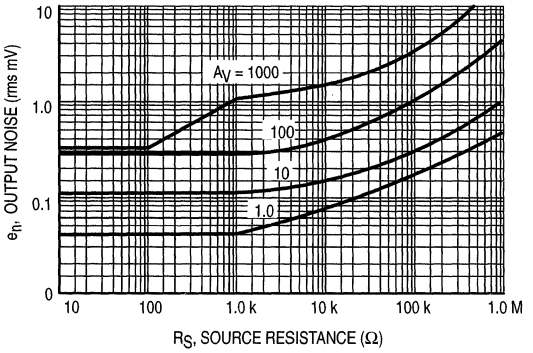


Figure 4. Spectral Noise Density

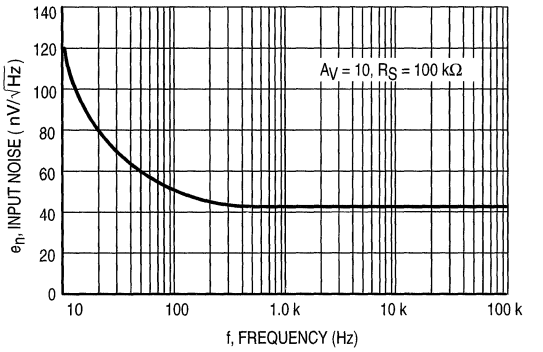
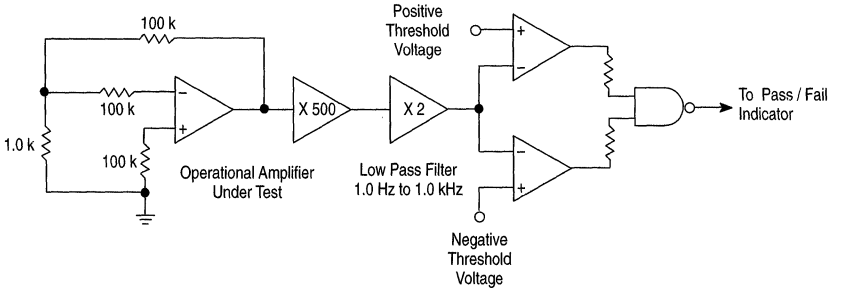


Figure 5. Burst Noise Test Circuit



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 sec and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed loop gain factor of the operational amplifier .

Figure 6. Power Bandwidth (Large Signal Swing versus Frequency)

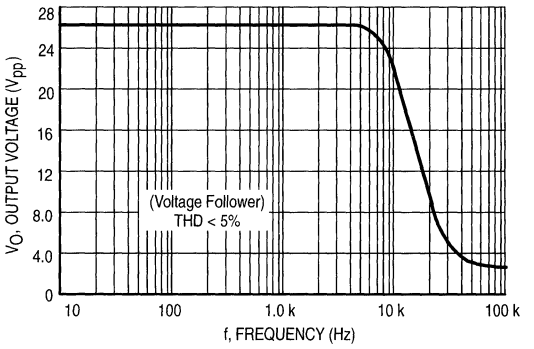


Figure 7. Open Loop Frequency Response

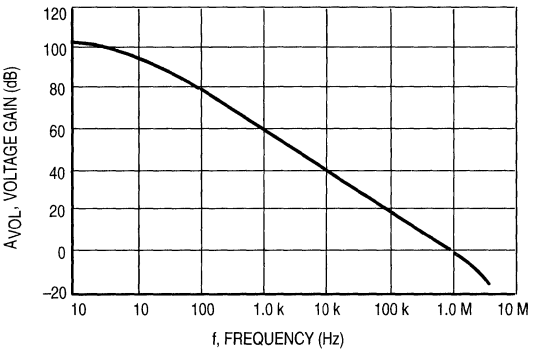


Figure 8. Positive Output Voltage Swing versus Load Resistance

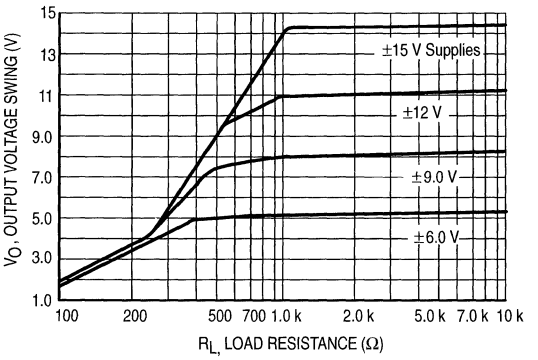


Figure 9. Negative Output Voltage Swing versus Load Resistance

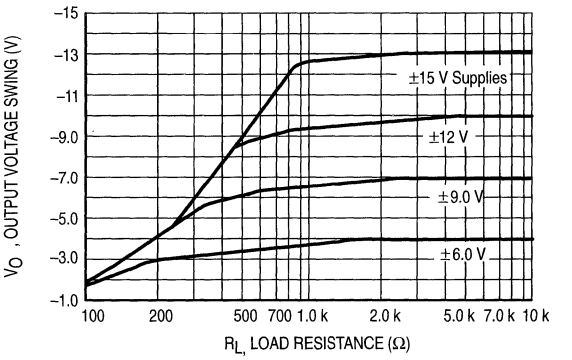


Figure 10. Output Voltage Swing versus Load Resistance (Single Supply Operation)

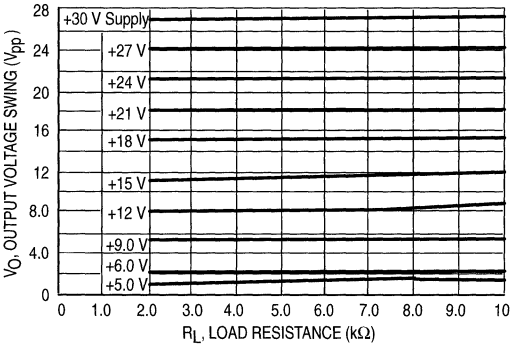
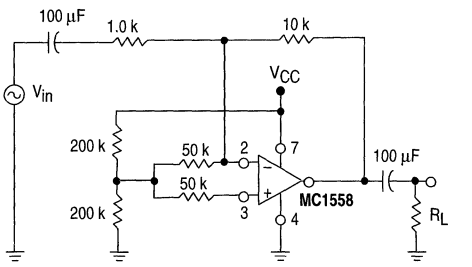


Figure 11. Single Supply Inverting Amplifier



2

Figure 12. Noninverting Pulse Response

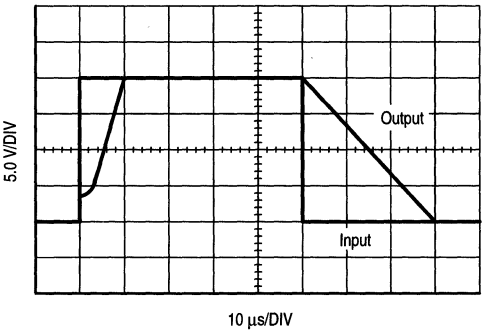


Figure 13. Transient Response Test Circuit

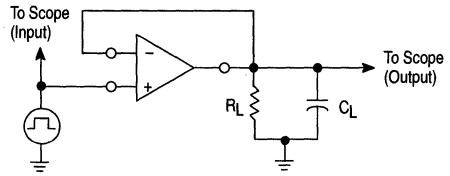


Figure 14. Unused OpAmp

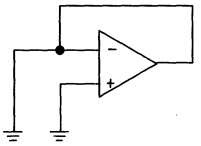
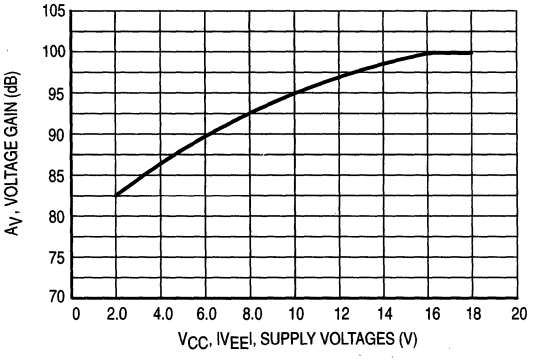


Figure 15. Open Loop Voltage Gain versus Supply Voltage



MOTOROLA

MCT1458, C

Internally Compensated, High Performance Dual Operational Amplifier

The MCT1458, C was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short Circuit Protection
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch–Up

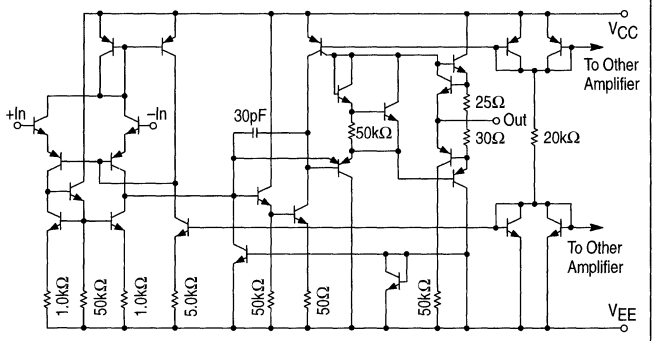
This MCT–prefixed device is intended to be a possible replacement for the similar device with the MC–prefix. Because the MCT device originates from different source material, there may be subtle differences in typical parameter values or characteristic curves. Due to the diversity of potential applications, Motorola can not assure identical performance in all circuits. Motorola recommends that the customer qualify the MCT–prefixed device in each potential application.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±30	V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Junction Temperature	T_J	150	°C

NOTES: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

Representative Schematic Diagram

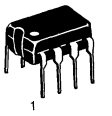


This device contains 46 active transistors.

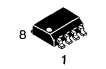
CAUTION: These devices do not have internal ESD protection circuitry and are rated as CLASS 1 devices per the ESD test method in Mil–Std–833D. They should be handled using standard ESD prevention methods to avoid damage to the device.

DUAL OPERATIONAL AMPLIFIER
(DUAL MC1741)

SEMICONDUCTOR TECHNICAL DATA

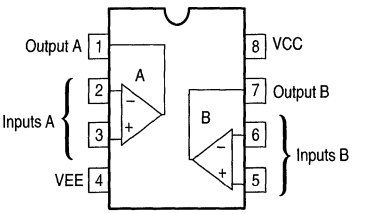


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MCT1458CD, D	T_A = 0° to +70°C	SO–8
MCT1458CP1, P1		Plastic

2

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MCT1458			MCT1458C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	—	2.0	6.0	—	2.0	10	mV
Input Offset Current	I_{IO}	—	20	200	—	20	300	nA
Input Bias Current	I_{IB}	—	80	500	—	80	700	nA
Input Resistance	r_i	0.3	2.0	—	—	2.0	—	MΩ
Input Capacitance	C_i	—	6.0	—	—	6.0	—	pF
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	±11	±13	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k) (V_O = ±10 V, R_L = 10 k)	A_{VOL}	 20 —	 200 —	 — —	 — 20	 — 200	 — —	V/mV
Output Resistance	r_o	—	75	—	—	75	—	Ω
Common Mode Rejection ($R_S \leq 10$ k)	CMR	70	90	—	60	90	—	dB
Supply Voltage Rejection ($R_S \leq 10$ k)	PSR	—	30	150	—	30	—	μV/V
Output Voltage Swing ($R_S \leq 10$ k) ($R_S \leq 2.0$ k)	V_O	 ±12 ±10	 ±14 ±13	 — —	 ±11 ±9.0	 ±14 ±13	 — —	V
Output Short Circuit Current	I_{SC}	—	20	—	—	20	—	mA
Supply Currents (Both Amplifiers)	I_D	—	2.3	5.6	—	2.3	8.0	mA
Power Consumption	P_C	—	70	170	—	70	240	mW
Transient Response (Unity Gain) (V_I = 20 mV, $R_L \geq 2.0$ kΩ, $C_L \leq 100$ pF) Rise Time (V_I = 20 mV, $R_L \geq 2.0$ kΩ, $C_L \leq 100$ pF) Overshoot (V_I = 10 V, $R_L \geq 2.0$ kΩ, $C_L \leq 100$ pF) Slew Rate	 t_{TLH} os SR	 — — —	 0.9 15 0.8	 — — —	 — — —	 0.9 15 0.8	 — — —	 μs % V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low}, unless otherwise noted.)

Characteristic	Symbol	MCT1458			MCT1458C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	—	—	7.5	—	—	12	mV
Input Offset Current (T_A = 0° to +70°C)	I_{IO}	 —	 —	 300	 —	 —	 400	nA
Input Bias Current (T_A = 0° to +70°C)	I_{IB}	 —	 —	 800	 —	 —	 1000	nA
Output Voltage Swing ($R_S \leq 10$ k) ($R_S \leq 2$ k)	V_O	 ±12 ±10	 ±14 ±13	 — —	 — ±9.0	 — ±13	 — —	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2 k) (V_O = ±10 V, R_L = 10 k)	A_{VOL}	 15 —	 — —	 — —	 — 15	 — —	 — —	V/mV

Figure 1. Power Bandwidth (Large Signal Swing versus Frequency)

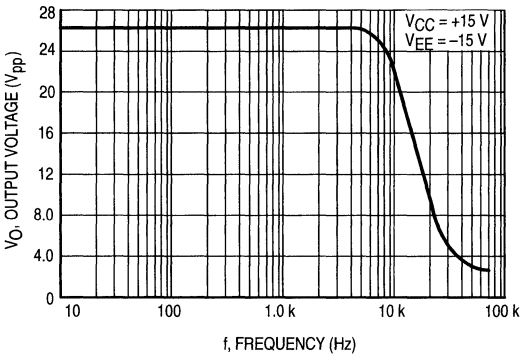


Figure 2. Maximum Output Voltage Swing versus Load Resistance

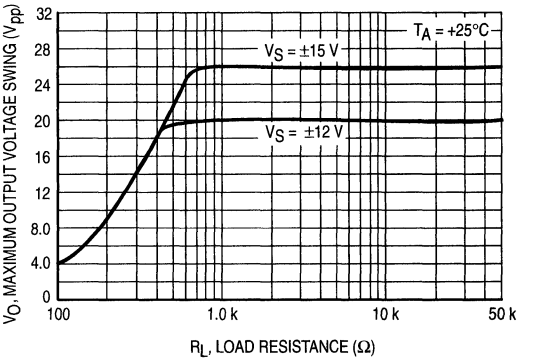


Figure 3. Input Offset Current versus Temperature

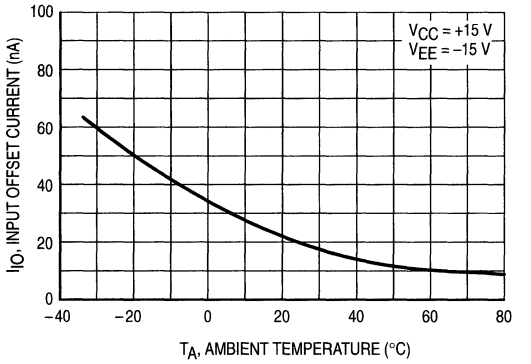


Figure 4. Input Offset Current versus Supply Voltage

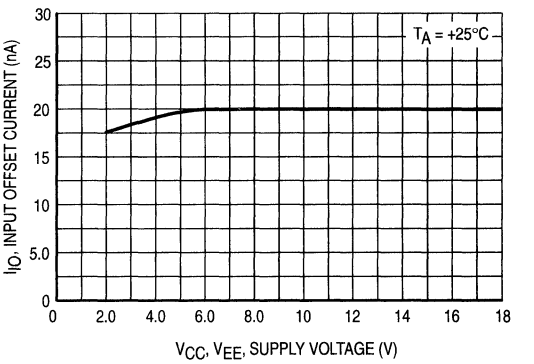


Figure 5. Open Loop Voltage Gain versus Supply Voltage

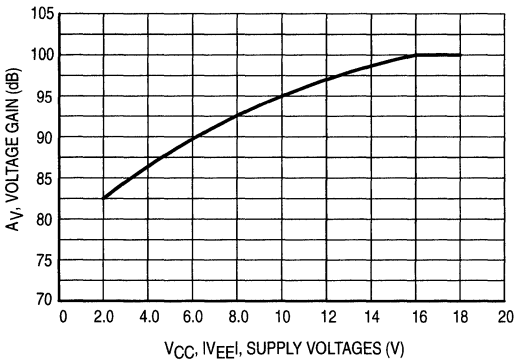
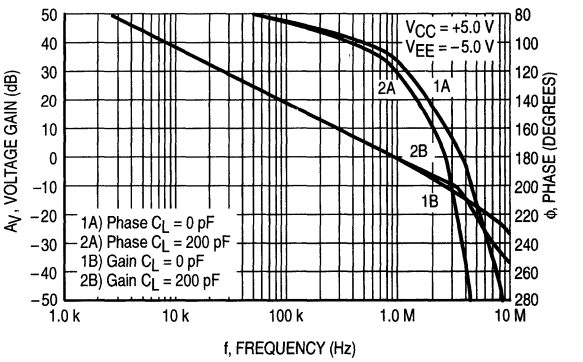


Figure 6. Voltage Gain and Phase versus Frequency



MC1490

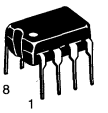
RF/IF/Audio Amplifier

The MC1490 is an integrated circuit featuring wide–range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, –40° to +85°C.

- High Power Gain: 50 dB Typ at 10 MHz
  45 dB Typ at 60 MHz
  35 dB Typ at 100 MHz
- Wide Range AGC: 60 dB Min, DC to 60 MHz
- 6.0 V to 15 V Operation, Single Polarity Supply
- See MC1350D for Surface Mount

WIDEBAND AMPLIFIER WITH AGC

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

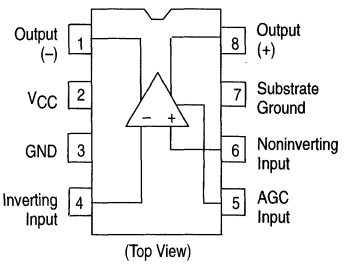
MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
AGC Supply	V_{AGC}	V_{CC}	Vdc
Input Differential Voltage	V_{ID}	5.0	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	+150	°C

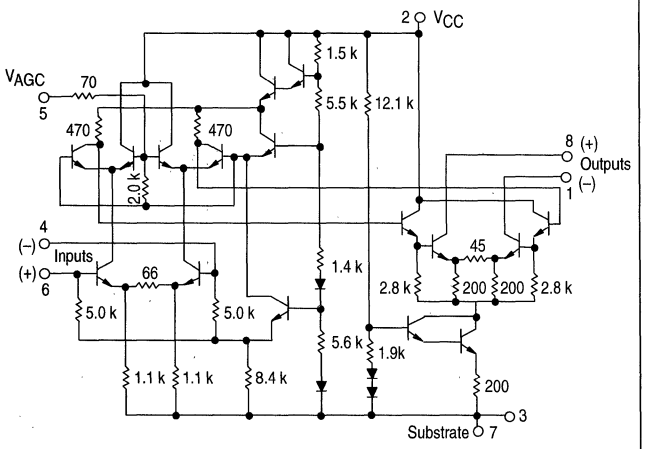
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1490P	T_A = –40° to +85°C	Plastic

PIN CONNECTIONS



Representative Schematic Diagram



Pins 3 and 7 should both be connected to circuit ground.

SCATTERING PARAMETERS
(V_{CC} = +12 Vdc, T_A = +25°C, Z_o = 50 Ω)

Parameter	Symbol	f = MHz Typ 30	f = MHz Typ 60	Unit
Input Reflection Coefficient	$\|S_{11}\|$ $\theta 11$	0.95 –7.3	0.93 –16	– deg
Output Reflection Coefficient	$\|S_{22}\|$ $\theta 22$	0.99 –3.0	0.98 –5.5	– deg
Forward Transmission Coefficient	$\|S_{21}\|$ $\theta 21$	16.8 128	14.7 64.3	– deg
Reverse Transmission Coefficient	S_{12} $\theta 12$	0.00048 84.9	0.00092 79.2	– deg

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, f = 60 MHz, BW = 1.0 MHz, T_A = 25°C)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Power Supply Current Drain	–	I_{CC}	–	–	17	mA
AGC Range (AGC) 5.0 V Min to 7.0 V Max	19	M_{AGC}	–60	–	–	dB
Output Stage Current (Sum of Pins 1 and 8)	–	I_O	4.0	–	7.5	mA
Single–Ended Power Gain R_S = R_L = 50 Ω	19	G_P	40	–	–	dB
Noise Figure R_S = 50 Ohms	19	NF	–	6.0	–	dB
Power Dissipation	–	P_D	–	168	204	mW

Figure 1. Unneutralized Power Gain versus Frequency (Tuned Amplifier, See Figure 19)

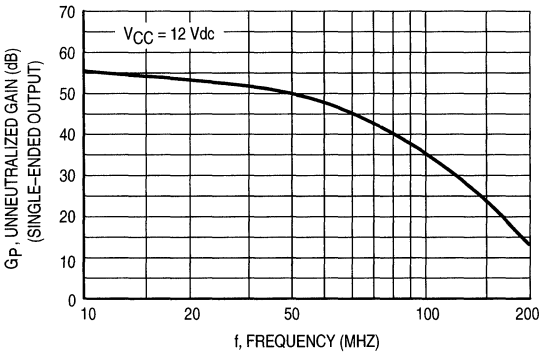


Figure 2. Voltage Gain versus Frequency (Video Amplifier, See Figure 20)

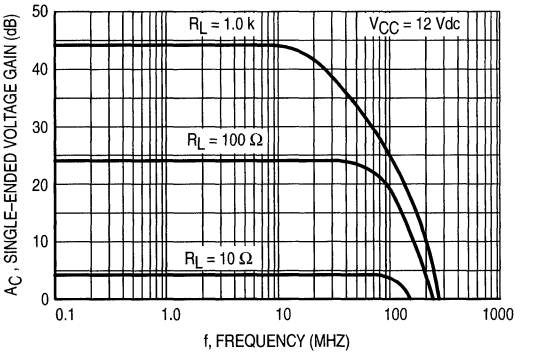


Figure 3. Dynamic Range: Output Voltage versus Input Voltage (Video Amplifier, See Figure 20)

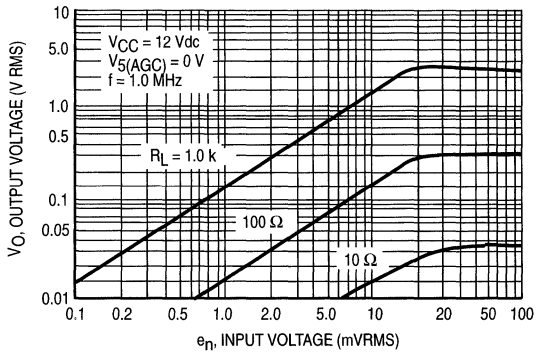
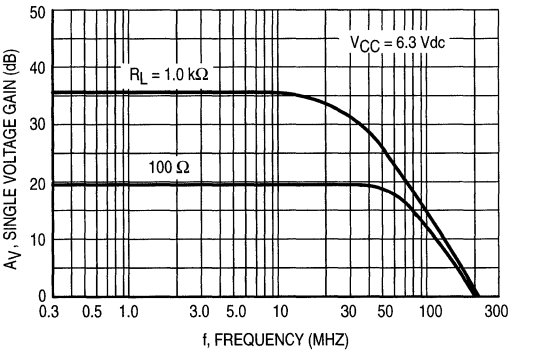


Figure 4. Voltage Gain versus Frequency (Video Amplifier, See Figure 20)



2

Figure 5. Voltage Gain and Supply Current versus Supply Voltage (Video Amplifier, See Figure 20)

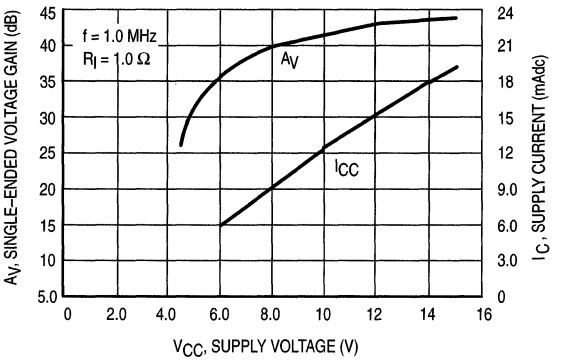


Figure 6. Typical Gain Reduction versus AGC Voltage

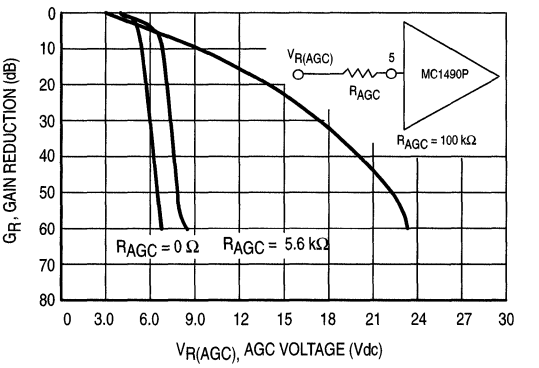


Figure 7. Typical Gain Reduction versus AGC Current

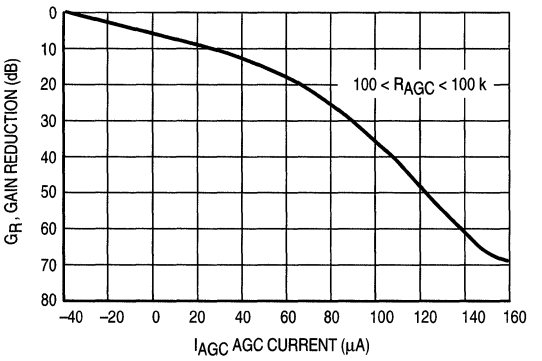


Figure 8. Fixed Tuned Power Gain Reduction versus Temperature (See Test Circuit, Figure 19)

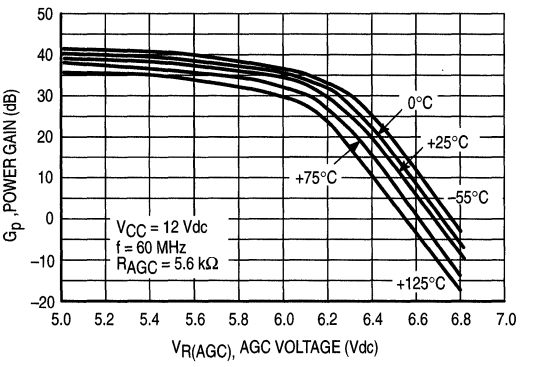


Figure 9. Power Gain versus Supply Voltage (See Test Circuit, Figure 19)

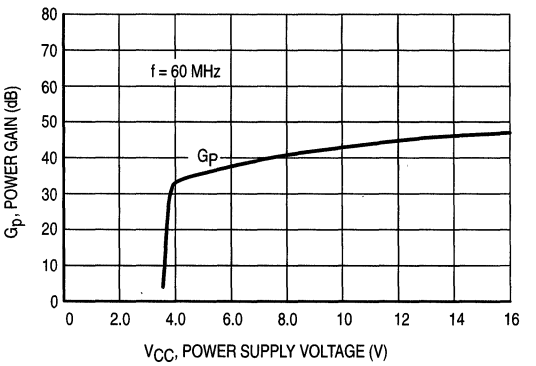


Figure 10. Noise Figure versus Frequency

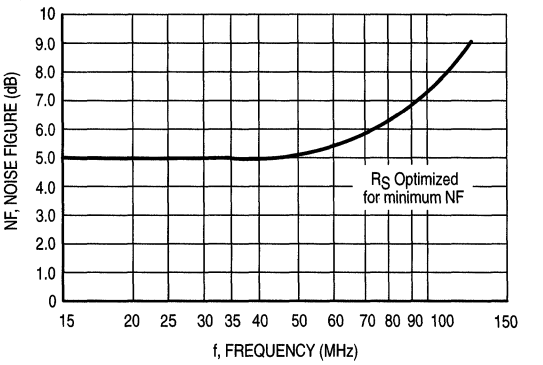


Figure 11. Noise Figure versus Source Resistance

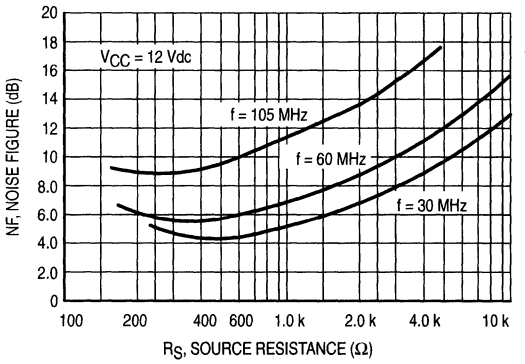


Figure 12. Noise Figure versus AGC Gain Reduction

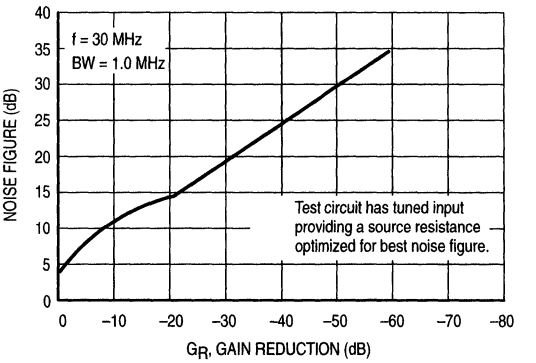


Figure 13. Harmonic Distortion versus AGC Gain Reduction for AM Carrier (For Test Circuit, See Figure 14)

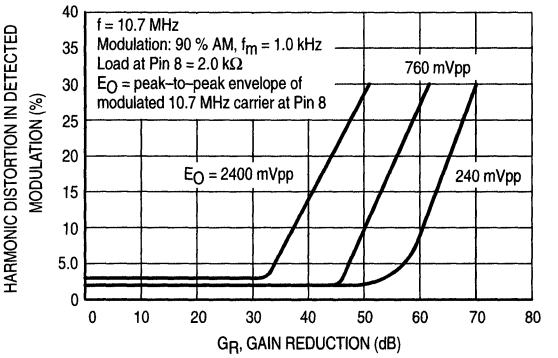
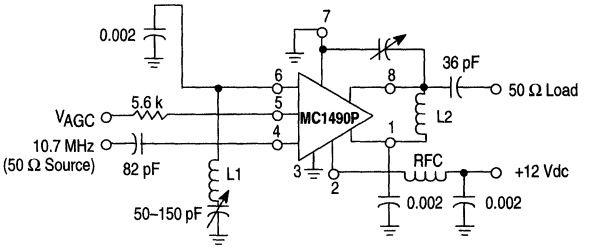


Figure 14. 10.7 MHz Amplifier Gain ≃ 55 dB, BW ≃ 100 kHz



L1 = 24 turns, #22 AWG wire on a T12–44 micro metal Toroid core (–124 pF)

L2 = 20 turns, #22 AWG wire on a T12–44 micro metal Toroid core (–100 pF)

2

Figure 15. S_{11} and S_{22}, Input and Output Reflection Coefficient

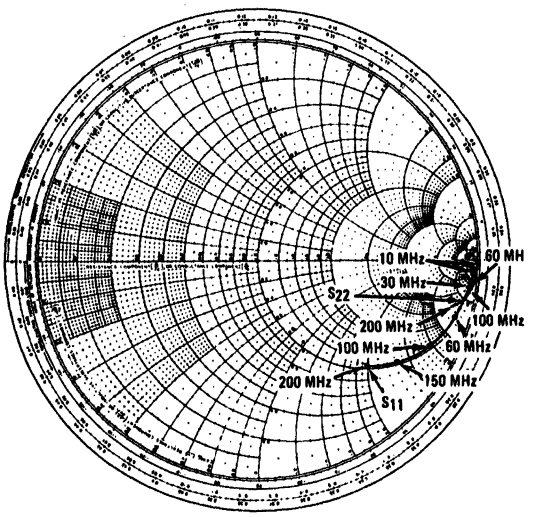


Figure 16. S_{11} and S_{22}, Input and Output Reflection Coefficient

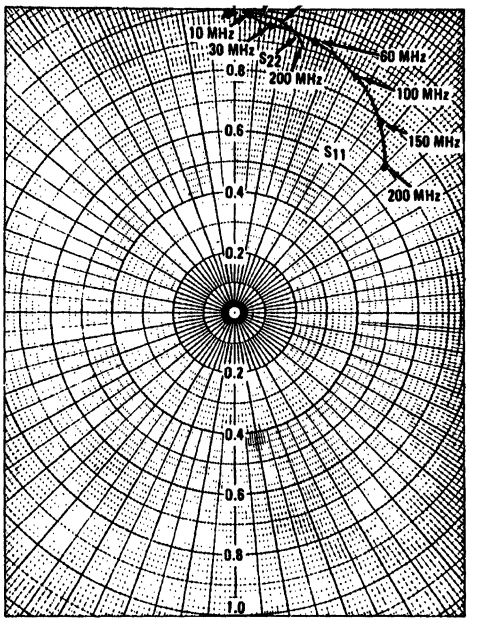


Figure 17. S_{21}, Forward Transmission Coefficient (Gain)

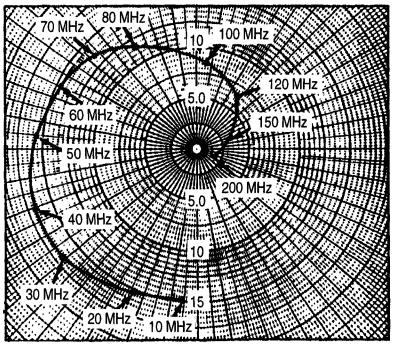


Figure 18. S_{12}, Reverse Transmission Coefficient (Feedback)

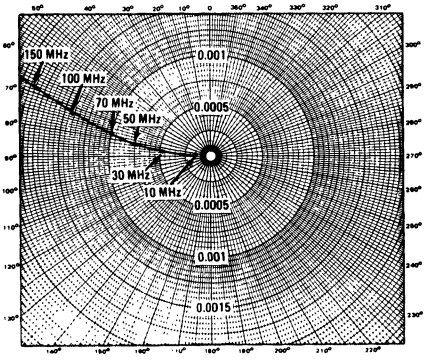
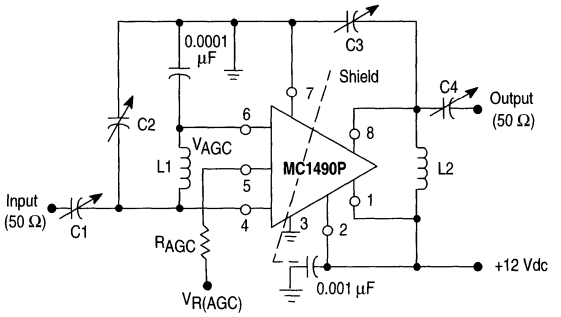


Figure 19. 60 MHz Power Gain Test Circuit



L1 = 7 turns, #20 AWG wire, 5/16″ Dia., 5/8″ long
L2 = 6 turns, #14 AWG wire, 9/16″ Dia., 3/4″ long
C1,C2,C3 = (1–30) pF
C4 = (1–10) pF

Figure 20. Video Amplifier

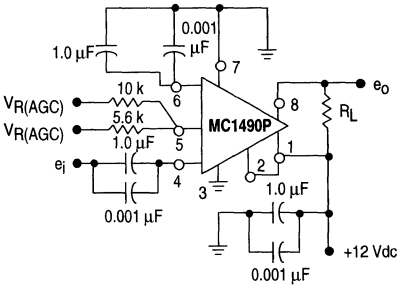
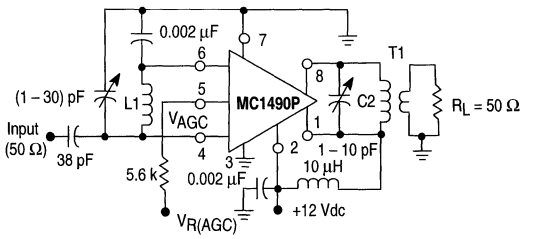
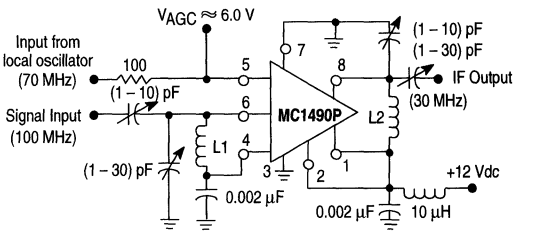


Figure 21. 30 MHz Amplifier (Power Gain = 50 dB, BW ≈ 1.0 MHz)



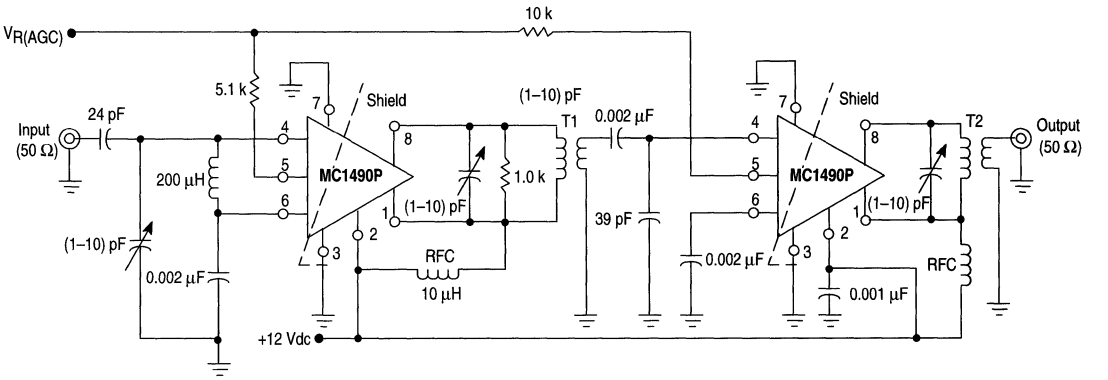
L1 = 12 turns, #22 AWG wire on a Toroid core, (T37–6 micro metal or equiv).
T1: Primary = 17 turns, #20 AWG wire on a Toroid core, (T44–6).
Secondary = 2 turns, #20 AWG wire.

Figure 22. 100 MHz Mixer



L1 = 5 turns, #16 AWG wire, 1/4″, ID Dia., 5/8″ long
L2 = 16 turns, #20 AWG wire on a Toroid core, (T44–6).

Figure 23. Two–Stage 60 MHz IF Amplifier (Power Gain ≈ 80 dB, BW ≈ 1.5 MHz)



T1: Primary Winding = 15 turns, #22 AWG wire, 1/4″ ID Air Core
Secondary Winding = 4 turns, #22 AWG wire,
Coefficient of Coupling ≈ 1.0

T2: Primary Winding = 10 turns, #22 AWG wire, 1/4″ ID Air Core
Secondary Winding = 2 turns, #22 AWG wire,
Coefficient of Coupling ≈ 1.0

2

DESCRIPTION OF SPEECH COMPRESSOR

The amplifier drives the base of a PNP transistor operating common–emitter with a voltage gain of approximately 20. The control R1 varies the quiescent Q point of this transistor so that varying amounts of signal exceed the level V_r. Diode D1 rectifies the positive peaks of Q1's output only when these peaks are greater than $V_r \simeq 7.0$ V. The resulting output is filtered by C_X, R_X.

R_X controls the charging time constant or attack time. C_X is involved in both charge and discharge. R2 (the 150 kΩ and input resistance of the emitter–follower Q2) controls the decay time. Making the decay long and attack short is accomplished by making R_X small and R2 large. (A Darlington emitter–follower may be needed if extremely slow decay times are required.)

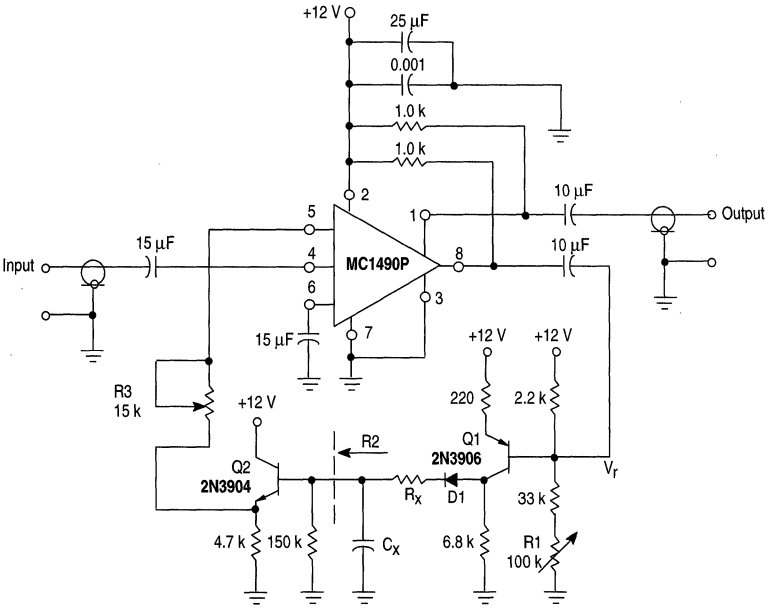
The emitter–follower Q2 drives the AGC Pin 5 of the MC1490P and reduces the gain. R3 controls the slope of signal compression.

Table 1. Distortion versus Frequency

Frequency	Distortion		Distortion	
	10 mV e_i	100 mV e_i	10 mV e_i	100 mV e_i
100 Hz	3.5%	12%	15%	27%
300 Hz	2%	10%	6%	20%
1.0 kHz	1.5%	8%	3%	9%
10 kHz	1.5%	8%	1%	3%
100 kHz	1.5%	8%	1%	3%
	Notes 1 and 2		Notes 3 and 4	

Notes: (1) Decay = 300 ms, Attack = 20 ms
(2) C_X = 7.5 µF, R_X = 0 (Short)
(3) Decay = 20 ms, Attack = 3.0 ms
(4) C_X = 0.68 µF, R_X = 1.5 kΩ

Figure 24. Speech Compressor



MOTOROLA

MC1741C

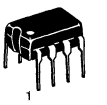
Internally Compensated, High Performance Operational Amplifier

The MC1741C was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short Circuit Protection
- Offset Voltage Null Capability
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

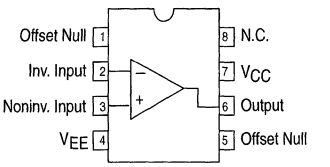
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±18	Vdc
Input Differential Voltage	V_{ID}	±30	V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

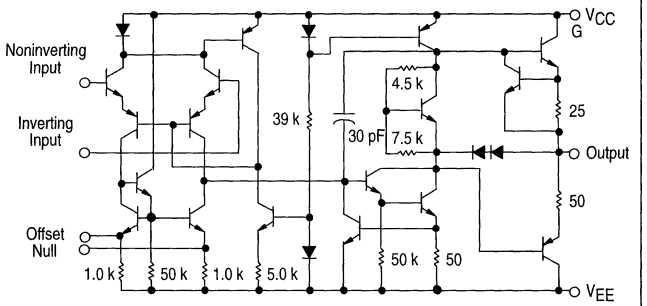
NOTES: 1. For supply voltages less than +15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

PIN CONNECTIONS



(Top View)

Equivalent Circuit Schematic
(1/4 of Circuit Shown)



ORDERING INFORMATION

Device	Alternate	Operating Temperature Range	Package
MC1741CD	–	T_A = 0° to +70°C	SO–8
MC1741CP1	LM741CN µA741TC		Plastic DIP

2

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \geq 2.0$ k)	A_{VOL}	20	200	–	V/mV
Output Resistance	r_o	–	75	–	Ω
Common Mode Rejection ($R_S \leq 10$ k)	CMR	70	90	–	dB
Supply Voltage Rejection ($R_S \leq 10$ k)	PSR	75	–	–	dB
Output Voltage Swing	V_O				V
($R_L \geq 10$ k)		±12	±14	–	
($R_L \geq 2.0$ k)		±10	±13	–	
Output Short Circuit Current	I_{SC}	–	20	–	mA
Supply Current	I_D	–	1.7	2.8	mA
Power Consumption	P_C	–	50	85	mW
Transient Response (Unity Gain, Noninverting)					
(V_I = 20 mV, $R_L \geq$ 2.0 k, $C_L \leq$ 100 pF) Rise Time	t_{TLH}	–	0.3	–	µs
(V_I = 20 mV, $R_L \geq$ 2.0 k, $C_L \leq$ 100 pF) Overshoot	os	–	15	–	%
(V_I = 10 V, $R_L \geq$ 2.0 k, $C_L \leq$ 100 pF) Slew Rate	SR	–	0.5	–	V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, $T_A = T_{low}$ to T_{high}, unless otherwise noted.)*

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	–	7.5	mV
Input Offset Current (T_A = 0° to +70°C)	I_{IO}	–	–	300	nA
Input Bias Current (T_A = 0° to +70°C)	I_{IB}	–	–	800	nA
Supply Voltage Rejection ($R_S \leq 10$ k)	PSR	75	–	–	dB
Output Voltage Swing ($R_L \geq 2.0$ k)	V_O	±10	±13	–	V
Large Signal Voltage Gain ($R_L \geq 2.0$ k, V_O = ±10 V)	A_{VOL}	15	–	–	V/mV

* T_{low} = 0°C T_{high} = 70°C

Figure 1. Burst Noise versus Source Resistance

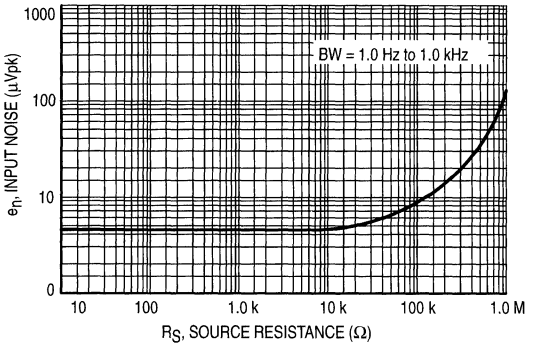


Figure 2. RMS Noise versus Source Resistance

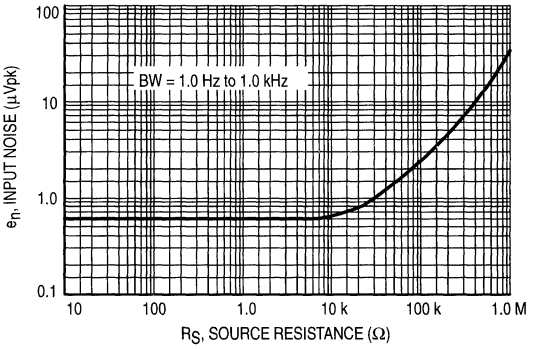


Figure 3. Output Noise versus Source Resistance

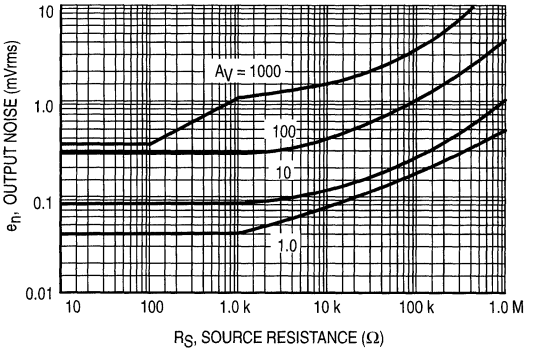


Figure 4. Spectral Noise Density

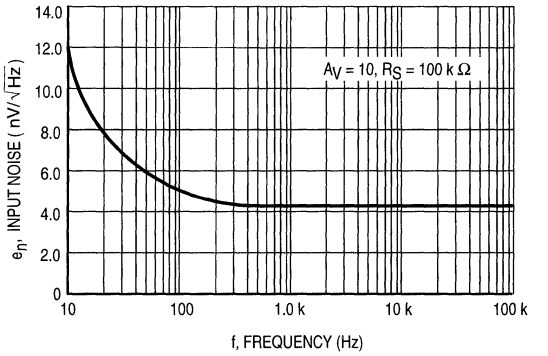
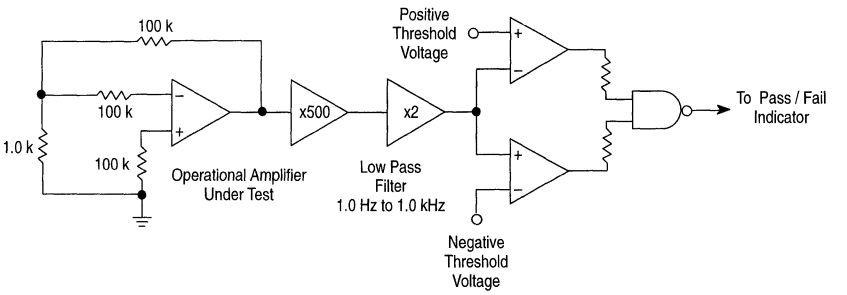


Figure 5. Burst Noise Test Circuit



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 sec and the 20 mV peak limit refers to the operational amplifier input thus eliminating errors in the closed loop gain factor of the operational amplifier.

2

Figure 6. Power Bandwidth (Large Signal Swing versus Frequency)

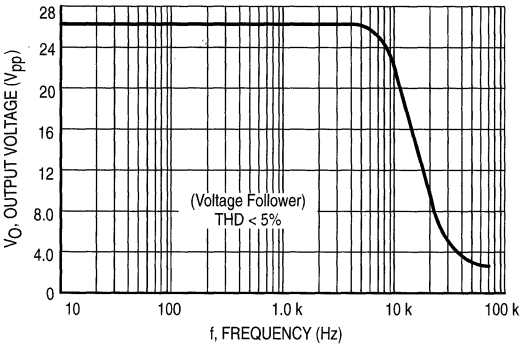


Figure 7. Open Loop Frequency Response

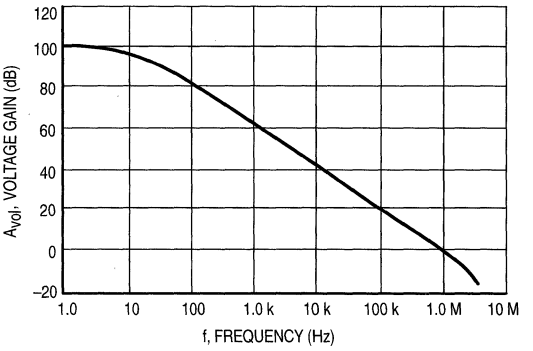


Figure 8. Positive Output Voltage Swing versus Load Resistance

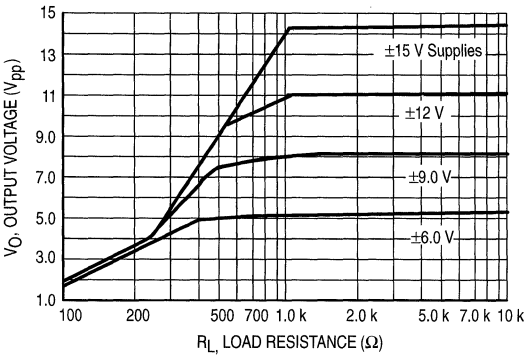


Figure 9. Negative Output Voltage Swing versus Load Resistance

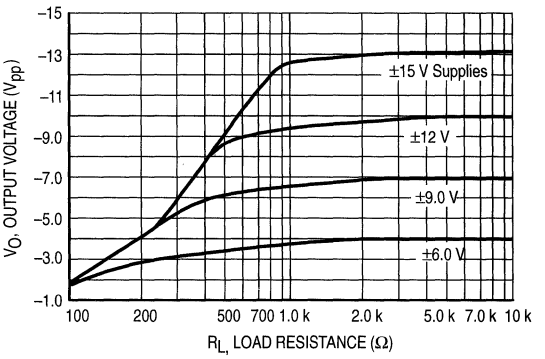


Figure 10. Output Voltage Swing versus Load Resistance (Single Supply Operation)

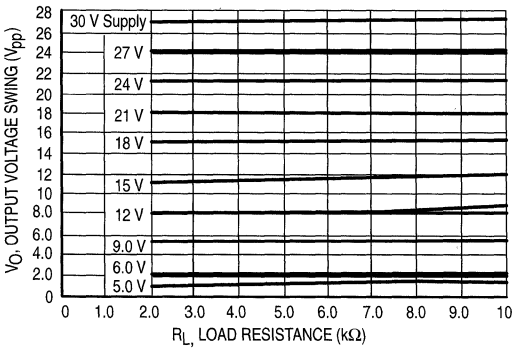


Figure 11. Single Supply Inverting Amplifier

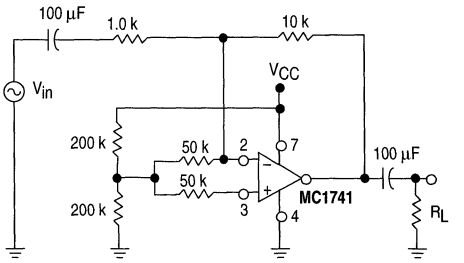


Figure 12. Noninverting Pulse Response

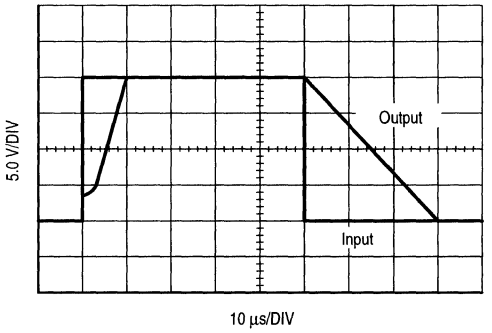


Figure 13. Transient Response Test Circuit

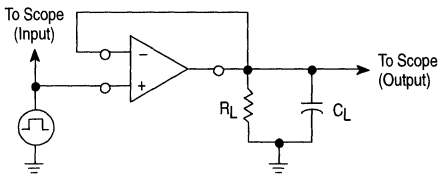
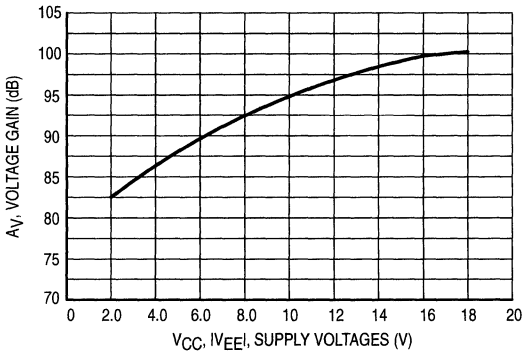


Figure 14. Open Loop Voltage Gain versus Supply Voltage



MC1776C

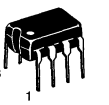
Micropower Programmable Operational Amplifier

This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

- ±1.2 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short Circuit Protection

PROGRAMMABLE OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA



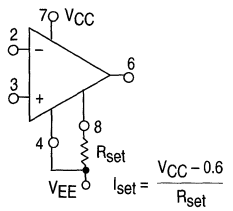
P1 SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Resistive Programming

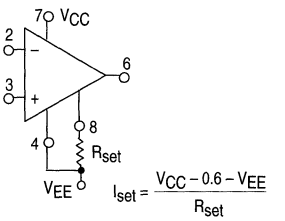
(See Figure 1)

R_{set} to Ground



R_{set} to Negative Supply

(Recommended for supply voltage less than ±6.0 V)

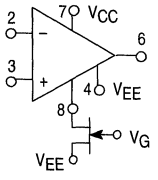


Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 µA	I_{set} = 15 µA
±6.0 V	3.6 MΩ	360 kΩ
±10 V	6.2 MΩ	620 kΩ
±12 V	7.5 MΩ	750 kΩ
±15 V	10 MΩ	1.0 MΩ

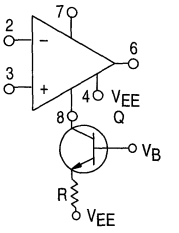
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 µA	I_{set} = 15 µA
±1.5 V	1.6 MΩ	160 kΩ
±3.0 V	3.6 MΩ	360 kΩ
±6.0 V	7.5 MΩ	750 kΩ
±15 V	20 MΩ	2.0 MΩ

Active Programming

FET Current Source

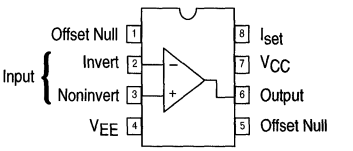


Bipolar Current Source



Pins not shown are not connected.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

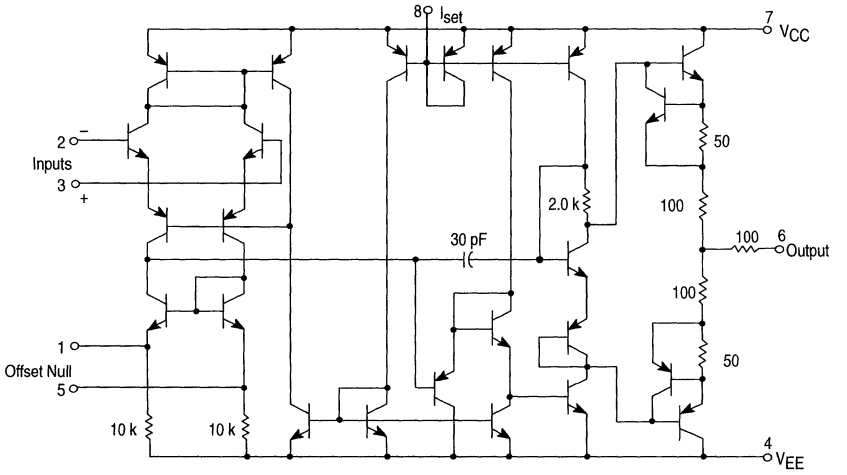
Device	Operating Temperature Range	Package
MC1776CD	T_A = 0° to +70°C	SO–8
MC1776CP1		Plastic DIP

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

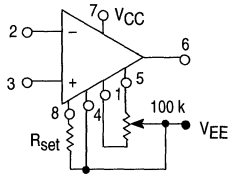
Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC},V_{EE}	±18	Vdc
Differential Input Voltage	V_{ID}	±30	Vdc
Common Mode Input Voltage V_{CC} and $\|V_{EE}\|$ < 15 V V_{CC} and $\|V_{EE}\|$ ≥ 15 V	V_{ICM}	 V_{CC},V_{EE} ±15	Vdc
Offset Null to V_{EE} Voltage	V_{off}–V_{EE}	±0.5	Vdc
Programming Current	I_{set}	500	μA
Programming Voltage (Voltage from I_{set} Terminal to Ground)	V_{set}	(V_{CC} –2.0 V) to V_{CC}	Vdc
Output Short Circuit Duration (Note 1)	t_{SC}	Indefinite	sec
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	150	°C

NOTE 1. May be to ground or either supply voltage. Rating applies up to a case temperature of +125°C or ambient temperature of +70°C and I_{set} ≤ 30 μA.

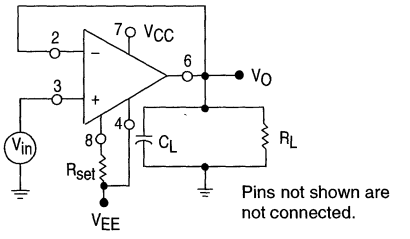
Representative Schematic Diagram



Voltage Offset Null Circuit



Transient Response Test Circuit



2

ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = –3.0 V, I_{set} = 1.5 µA, T_A = +25°C, unless otherwise noted.*)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}				mV
T_A = +25°C		–	2.0	6.0	
$T_{low}^* \leq T_A \leq T_{high}^*$		–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	mV
Input Offset Current	I_{IO}				nA
T_A = +25°C		–	0.7	6.0	
$T_A = T_{high}$		–	–	6.0	
$T_A = T_{low}$		–	–	10	
Input Bias Current	I_{IB}				nA
T_A = +25°C		–	2.0	10	
$T_A = T_{high}$		–	–	10	
$T_A = T_{low}$		–	–	20	
Input Resistance	r_i	–	50	–	MΩ
Input Capacitance	c_i	–	2.0	–	pF
Input Voltage Range	V_{ID}				V
$T_{low} \leq T_A \leq T_{high}$		+1.0	–	–	
Large Signal Voltage Gain	A_{VOL}				V/V
$R_L \geq 75$ kΩ, $V_O = \pm 1.0$ V, T_A = +25°C		25 k	200 k	–	
$R_L \geq 75$ kΩ, $V_O = \pm 1.0$ V, $T_{low} \leq T_A \leq T_{high}$		25 k	–	–	
Output Voltage Swing	V_O				V
$R_L \geq 75$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±2.0	±2.4	–	
Output Resistance	r_o	–	5.0	–	kΩ
Output Short Circuit Current	I_{SC}	–	3.0	–	mA
Common Mode Rejection	CMR				dB
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		70	86	–	
Supply Voltage Rejection Ratio	PSRR				µV/V
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	200	
Supply Current	I_{CC}, I_{EE}				µA
T_A = +25°C		–	13	20	
$T_{low} \leq T_A \leq T_{high}$		–	–	25	
Power Dissipation	P_D				µW
T_A = +25°C		–	78	120	
$T_{low} \leq T_A \leq T_{high}$		–	–	150	
Transient Response (Unity Gain)					
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF					
Rise Time	t_{TLH}	–	3.0	–	µs
Overshoot	os	–	0	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	S_R	–	0.03	–	V/µs

*T_{low} = 0°C T_{high} = +70°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = –3.0 V, I_{set} = 15 μA, T_A = +25°C, unless otherwise noted.*)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}				mV
T_A = +25°C		–	2.0	6.0	
$T_{low}^* \leq T_A \leq T_{high}^*$		–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	mV
Input Offset Current	I_{IO}				nA
T_A = +25°C		–	2.0	25	
$T_A = T_{high}$		–	–	25	
$T_A = T_{low}$		–	–	40	
Input Bias Current	I_{IB}				nA
T_A = +25°C		–	15	50	
$T_A = T_{high}$		–	–	50	
$T_A = T_{low}$		–	–	100	
Input Resistance	r_i	–	5.0	–	MΩ
Input Capacitance	c_i	–	2.0	–	pF
Input Voltage Range	V_{ID}				V
$T_{low} \leq T_A \leq T_{high}$		±1.0	–	–	
Large Signal Voltage Gain	A_{VOL}				V/V
$R_L \geq 5.0$ kΩ, V_O = ±1.0 V, T_A = +25°C		25 k	200 k	–	
$R_L \geq 5.0$ kΩ, V_O = ±1.0 V, $T_{low} \leq T_A \leq T_{high}$		25 k	–	–	
Output Voltage Swing	V_O				V
$R_L \geq 5.0$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±2.0	±2.1	–	
Output Resistance	r_o	–	1.0	–	kΩ
Output Short Circuit Current	I_{SC}	–	5.0	–	mA
Common Mode Rejection	CMR				dB
$R_S \leq$ 10 kΩ, $T_{low} \leq T_A \leq T_{high}$		70	86	–	
Supply Voltage Rejection Ratio	PSRR				μV/V
$R_S \leq$ 10 kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	200	
Supply Current	I_{CC}, I_{EE}				μA
T_A = +25°C		–	130	170	
$T_{low} \leq T_A \leq T_{high}$		–	–	180	
Power Dissipation	P_D				μW
T_A = +25°C		–	780	1020	
$T_{low} \leq T_A \leq T_{high}$		–	–	1080	
Transient Response (Unity Gain)					
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF					
Rise Time	t_{TLH}	–	0.6	–	μs
Overshoot	os	–	5.0	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	S_R	–	0.35	–	V/μs

*T_{low} = 0°C T_{high} = +70°C

2

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, I_{set} = 1.5 µA, T_A = +25°C, unless otherwise noted.*)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}				mV
T_A = +25°C		–	2.0	6.0	
$T_{low}^* \le T_A \le T_{high}^*$		–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	mV
Input Offset Current	I_{IO}				nA
T_A = +25°C		–	0.7	6.0	
$T_A = T_{high}$		–	–	6.0	
$T_A = T_{low}$		–	–	10	
Input Bias Current	I_{IB}				nA
T_A = +25°C		–	2.0	10	
$T_A = T_{high}$		–	–	10	
$T_A = T_{low}$		–	–	20	
Input Resistance	r_i	–	50	–	MΩ
Input Capacitance	c_i	–	2.0	–	pF
Input Voltage Range	V_{ID}				V
$T_{low} \le T_A \le T_{high}$		±10	–	–	
Large Signal Voltage Gain	A_{VOL}				V/V
$R_L \ge 75$ kΩ, V_O = ±10 V, T_A = +25°C		50 k	400 k	–	
$R_L \ge 75$ kΩ, V_O = ±10 V, $T_{low} \le T_A \le T_{high}$		50 k	–	–	
Output Voltage Swing	V_O				V
$R_L \ge 75$ kΩ, T_A = +25°C		±12	±14	–	
$R_L \ge 75$ kΩ, $T_{low} \le T_A \le T_{high}$		±10	–	–	
Output Resistance	r_o	–	5.0	–	kΩ
Output Short Circuit Current	I_{SC}	–	3.0	–	mA
Common Mode Rejection	CMR				dB
$R_S \le$ 10 kΩ, $T_{low} \le T_A \le T_{high}$		70	90	–	
Supply Voltage Rejection Ratio	PSRR				µV/V
$R_S \le$ 10 kΩ, $T_{low} \le T_A \le T_{high}$		–	25	200	
Supply Current	I_{CC}, I_{EE}				µA
T_A = +25°C		–	20	30	
$T_{low} \le T_A \le T_{high}$		–	–	35	
Power Dissipation	P_D				mW
T_A = +25°C		–	780	0.9	
$T_{low} \le T_A \le T_{high}$		–	–	1.05	
Transient Response (Unity Gain)					
V_{in} = 20 mV, $R_L \ge 5.0$ kΩ, C_L = 100 pF					
Rise Time	t_{TLH}	–	1.6	–	µs
Overshoot	os	–	0	–	%
Slew Rate ($R_L \ge 5.0$ kΩ)	S_R	–	0.1	–	V/µs

*T_{low} = 0°C T_{high} = +70°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, I_{set} = 15 μA, T_A = +25°C, unless otherwise noted.*)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}				mV
T_A = +25°C		–	2.0	6.0	
$T_{low}^* \le T_A \le T_{high}^*$		–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	mV
Input Offset Current	I_{IO}				nA
T_A = +25°C		–	2.0	25	
$T_A = T_{high}$		–	–	25	
$T_A = T_{low}$		–	–	40	
Input Bias Current	I_{IB}				nA
T_A = +25°C		–	15	50	
$T_A = T_{high}$		–	–	50	
$T_A = T_{low}$		–	–	100	
Input Resistance	r_i	–	5.0	–	MΩ
Input Capacitance	c_i	–	2.0	–	pF
Input Voltage Range	V_{ID}				V
$T_{low} \le T_A \le T_{high}$		±10	–	–	
Large Signal Voltage Gain	A_{VOL}				V/V
$R_L \ge 5.0$ kΩ, V_O = ±10 V, T_A = +25°C		50 k	400 k	–	
$R_L \ge 75$ kΩ, V_O = ±10 V, $T_{low} \le T_A \le T_{high}$		50 k	–	–	
Output Voltage Swing	V_O				V
$R_L \ge 5.0$ kΩ, T_A = +25°C		±10	±13	–	
$R_L \ge 75$ kΩ, $T_{low} \le T_A \le T_{high}$		±10	–	–	
Output Resistance	r_o	–	1.0	–	kΩ
Output Short Circuit Current	I_{SC}	–	12	–	mA
Common Mode Rejection	CMR				dB
$R_S \le 10$ kΩ, $T_{low} \le T_A \le T_{high}$		70	90	–	
Supply Voltage Rejection Ratio	PSRR				μV/V
$R_S \le 10$ kΩ, $T_{low} \le T_A \le T_{high}$		–	25	200	
Supply Current	I_{CC}, I_{EE}				μA
T_A = +25°C		–	160	190	
$T_{low} \le T_A \le T_{high}$		–	–	200	
Power Dissipation	P_D				μW
T_A = +25°C		–	–	5.7	
$T_{low} \le T_A \le T_{high}$		–	–	6.0	
Transient Response (Unity Gain)					
V_{in} = 20 mV, $R_L \ge 5.0$ kΩ, C_L = 100 pF					
Rise Time	t_{TLH}	–	0.35	–	μs
Overshoot	os	–	10	–	%
Slew Rate ($R_L \ge 5.0$ kΩ)	S_R	–	0.8	–	V/μs

*T_{low} = 0°C T_{high} = +70°C

2

Figure 1. Set Current versus Set Resistor

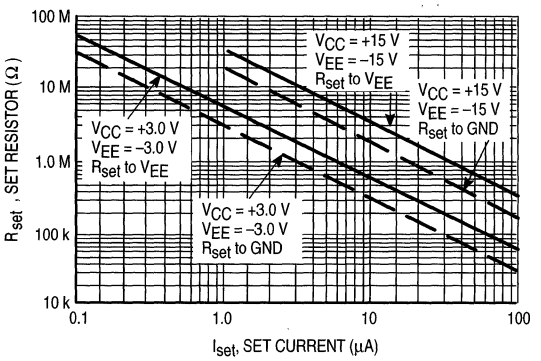


Figure 2. Positive Standby Supply Current versus Set Current

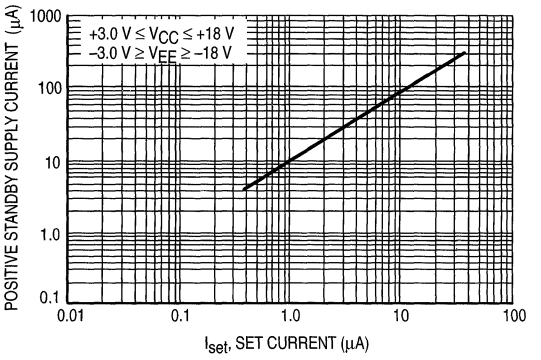


Figure 3. Open Loop Gain versus Set Current

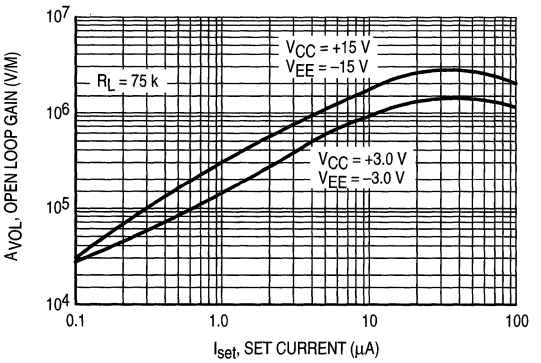


Figure 4. Input Bias Current versus Set Current

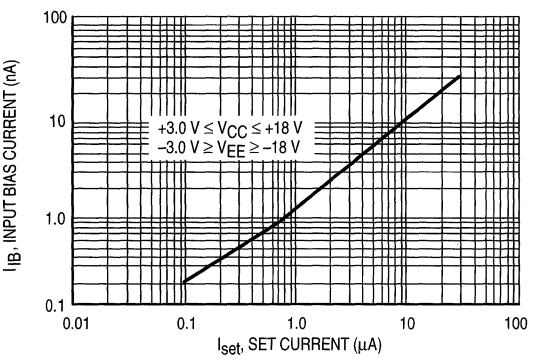


Figure 5. Input Bias Current versus Ambient Temperature

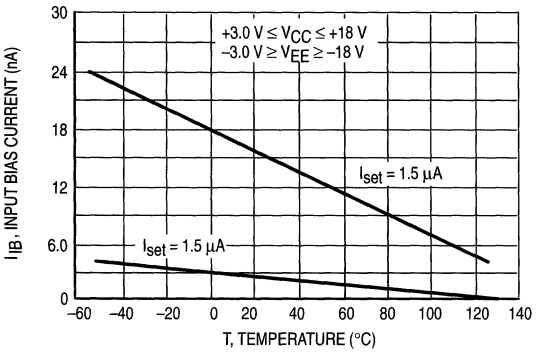


Figure 6. Gain Bandwidth Product versus Set Current

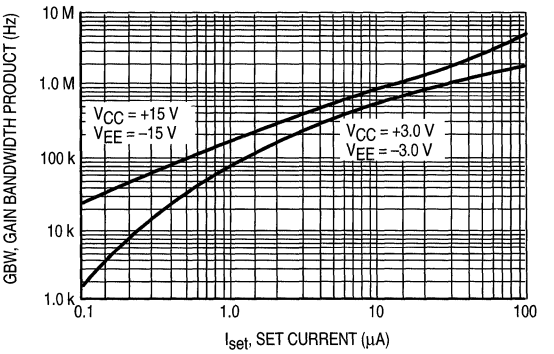


Figure 7. Output Voltage Swing versus Load Resistance

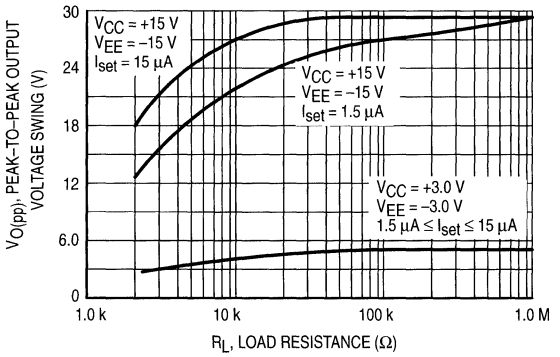


Figure 8. Supply Current versus Ambient Temperature

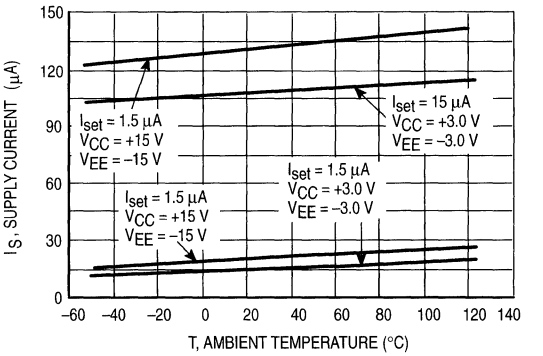


Figure 9. Output Voltage Swing versus Supply Voltage

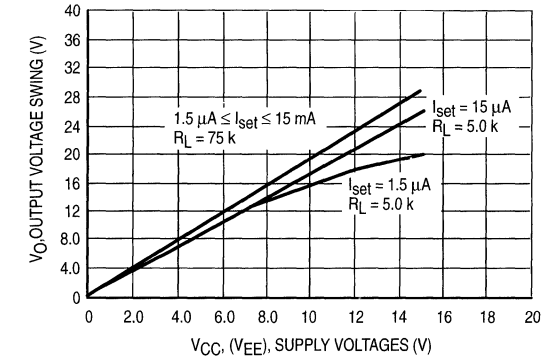


Figure 10. Slew Rate versus Set Current

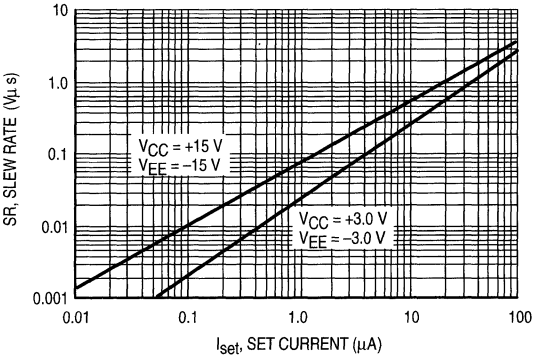


Figure 11. Input Noise Voltage versus Set Current

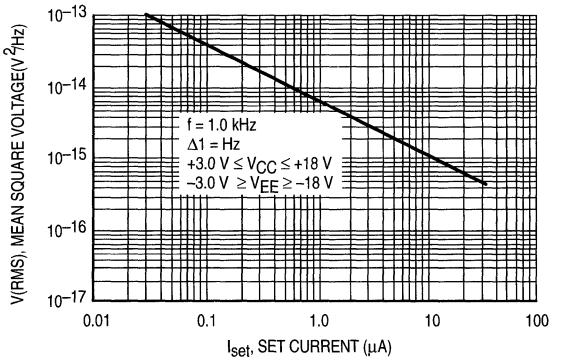
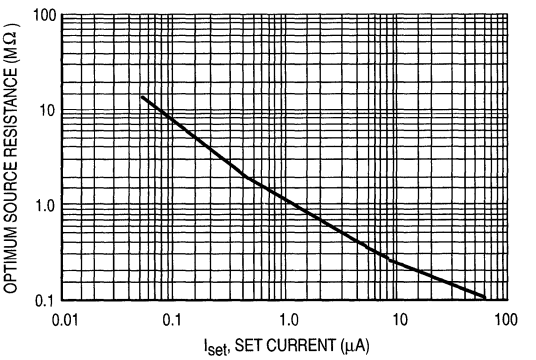
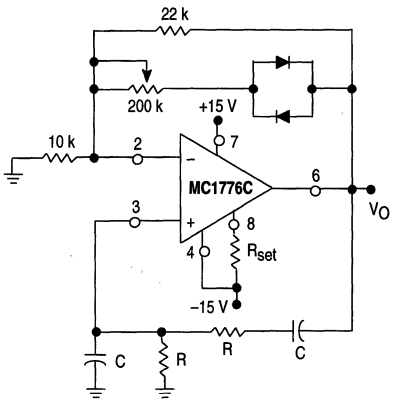


Figure 12. Optimum Source Resistance for Minimum Noise versus Set Current



2

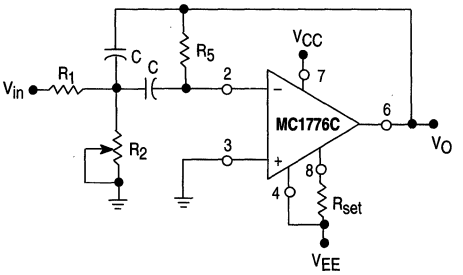
Figure 13. Wien Bridge Oscillator



$$f_O = \frac{1}{2\pi RC} \quad (\text{for } f_O = 1.0 \text{ kHz})$$

R= 16 kΩ
C = 0.01 μF

Figure 14. Multiple Feedback Bandpass Filter



For a given:
fo = center frequency
A (fo) = Gain at center frequency
Q = quality factor

Choose a value for C, then

$$R_5 = \frac{Q}{\pi f_O C}$$

$$R_1 = \frac{R5}{2A\,(f_O)}$$

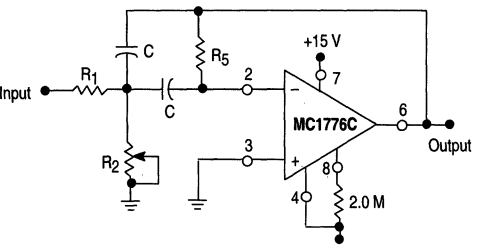
$$R_2 = \frac{R1,R5}{4Q^2\,R1-R5}$$

To obtain less than 10% error from the operational amplifier:

$$\frac{Q_O\, f_O}{GBW} \leq 0.1$$

where f_O and GBW are expressed in Hz. GBW is available from Figure 6 as a function of Set Current, I_{set}.

Figure 15. Multiple Feedback Bandpass Filter (1.0 kHz)



for a 1.0 kHz filter with Q = 10 and A (f_O) = 1

R_1 = 160 k
R_2 = 820
R_5 = 300 k
C = 0.01 μF

Figure 16. Gated Amplifier

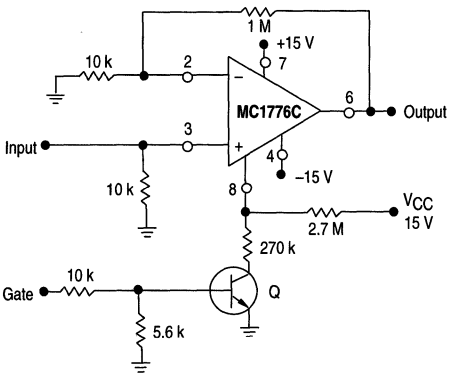
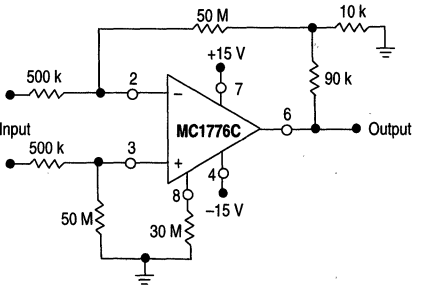


Figure 17. High Input Impedance Amplifier



MC3301, LM2900, LM3900

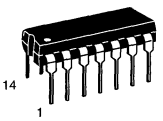
Quad Single Supply Operational Amplifiers

These internally compensated Norton operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each device contains four independent amplifiers – making it ideal for applications such as active filters, multi–channel amplifiers, tachometers, oscillators and other similar usage.

- Single Supply Operation
- Internally Compensated
- Wide Unity Gain Bandwidth: 4.0 MHz Typical
- Low Input Bias Current: 50 nA Typical
- High Open Loop Gain: 1000 V/V Minimum
- Large Output Voltage Swing: (V_{CC} – 1) V_{pp}

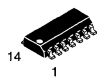
QUAD OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA



N, P SUFFIX
PLASTIC PACKAGE
CASE 646

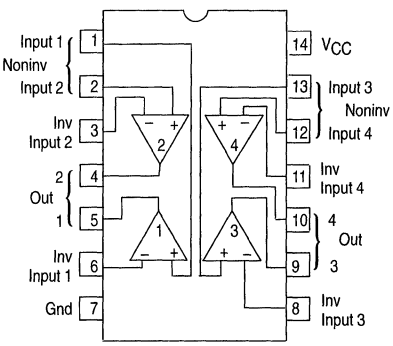
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



MAXIMUM RATINGS

Rating	Symbol	LM2900/ LM3900	MC3301	Unit
Supply Voltage	V_{CC}	+32	+28	V
Input Current (I_{in+} or I_{in-})	I_{in}	5.0		mA
Output Current	I_O	50		mA
Power Dissipation (T_A = +25°C) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	625 5.0		mW mW/°C
Ambient Temperature Range LM2900 LM3900	T_A	 –40 to +85 0 to +70	 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150		°C

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM3900D	T_A = 0° to +70°C	SO–14
LM3900N		Plastic DIP
LM2900N MC3301P	T_A = – 40° to +85°C	

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, R_L = 5.0 kΩ. T_A = +25°C [each amplifier], unless otherwise noted.)

Characteristic	Symbol	LM2900			LM3900			MC3301			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Open Loop Voltage Gain	A_{VOL}										V/mV
f = 100 Hz, R_L = 5.0 k		1.2	2.0	–	1.2	2.0	–	1.2	2.0	–	
$T_A = T_{low}$ to T_{high} (Notes 1, 2)		–	–	–	–	–	–	–	–	–	
Input Resistance (Inverting Input)	r_i	–	1.0	–	–	1.0	–	–	1.0	–	MΩ
Output Resistance	r_o	–	8.0	–	–	8.0	–	–	8.0	–	kΩ
Input Bias Current (Inverting Input)	I_{IB}	–	50	200	–	50	200	–	50	300	nA
$T_A = T_{low}$ to T_{high} (Note 1)		–	–	–	–	–	–	–	–	–	
Slew Rate (C_L = 100 pF, R_L = 2.0 k)	SR										V/μs
Positive Output Swing		–	0.5	–	–	0.5	–	–	0.5	–	
Negative Output Swing		–	20	–	–	20	–	–	20	–	
Unity Gain Bandwidth	BW	–	4.0	–	–	4.0	–	–	4.0	–	MHz
Output Voltage Swing (Note 7)											V
V_{CC} = +15 V, R_L = 2.0 k											
V_{out} High (I_{in}^- = 0, I_{in} += 0)	V_{OH}	13.5	14.2	–	13.5	14.2	–	13.5	14.2	–	
V_{out} Low (I_{in}^- = 10 μA, I_{in} += 0)	V_{OL}	–	0.03	0.2	–	0.03	0.2	–	0.03	0.2	
V_{CC} = Maximum Rating, R_L = ∞											
V_{out} High (I_{in}^- = 0, I_{in} += 0)	V_{OH}	–	29.5	–	–	29.5	–	–	25.5	–	
Output Current											mA
Source	I_{Source}	6.0	10	–	6.0	10	–	5.0	10	5.0	
Sink (Note 3)	I_{Sink}	0.5	0.87	–	0.5	0.87	–	0.5	0.87	0.5	
Low Level Output Current	I_{OL}	–	5.0	–	–	5.0	–	–	5.0	–	
I_{in}^- = 5.0 μA, V_{OL} = 1.0 V											
Supply Current (All Four Amplifiers)											mA
Noninverting Inputs Open	I_{DO}	–	6.9	10	–	6.9	10	–	6.9	10	
Noninverting Inputs Grounded	I_{DG}	–	7.8	14	–	7.8	14	–	7.8	14	
Power Supply Rejection (f = 100 Hz)	PSR	–	55	–	–	55	–	–	55	–	dB
Mirror Gain ($T_A = T_{low}$ to T_{high}; Notes 1, 4)	A_i										μA
I_{in} += 20 μA		0.90	1.0	1.1	0.90	1.0	1.1	0.90	1.0	1.1	
I_{in} += 200 μA		0.90	1.0	1.1	0.90	1.0	1.1	0.90	1.0	1.1	
Δ Mirror Gain ($T_A = T_{low}$ to T_{high}; Notes 1, 4)	ΔA_i	–	2.0	5.0	–	2.0	5.0	–	2.0	5.0	%
20 μA ≤ I_{in} + ≤ 200 μA											
Mirror Current ($T_A = T_{low}$ to T_{high}; Notes 1, 5)		–	10	500	–	10	500	–	10	500	μA
Negative Input Current (Note 6)		–	1.0	–	–	1.0	–	–	1.0	–	mA

NOTES: 1. T_{low} = −40°C for LM2900, MC3301 = 0°C for LM3900 T_{high} = +85°C for LM2900, MC3301 = +70°C for LM3900

2. Open loop voltage gain is defined as voltage gain from the inverting input to the output.
3. Sink current is specified for analog operation. When the device is used as a comparator (non–analog operation) where the inverting input is overdriven, the sink current (low level output current) capability is typically 5.0 mA.
4. This specification indicates the current gain of the current mirror which is used as the noninverting input.
5. Input V_{BE} match between the noninverting and inverting inputs occurs for a mirror current (noninverting input current) of approximately 10 μA.
6. Clamp transistors are included to prevent the input voltages from swinging below ground more than approximately –0.3 V. The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately 1.0 mA. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common mode biasing can be used to prevent negative input voltages.
7. When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.

Figure 1. Open Loop Voltage Gain versus Frequency

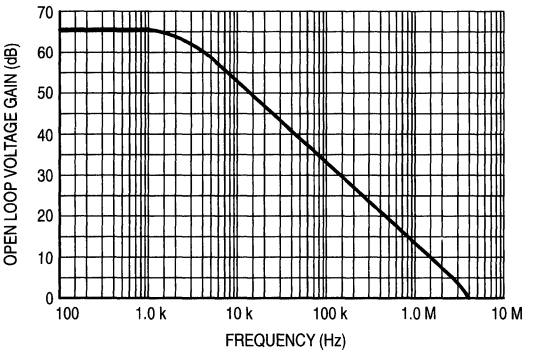


Figure 2. Open Loop Voltage Gain versus Supply Voltage

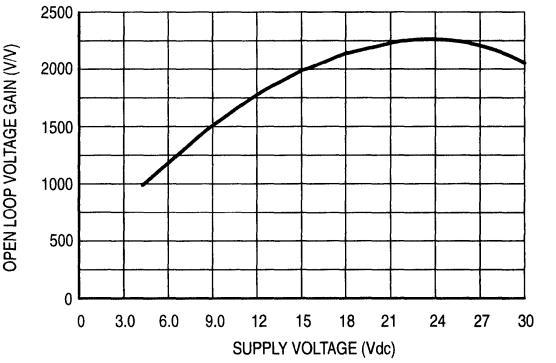


Figure 3. Output Resistance versus Frequency

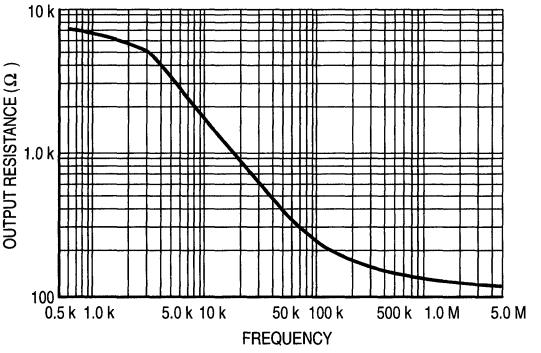


Figure 4. Supply Current versus Supply Voltage

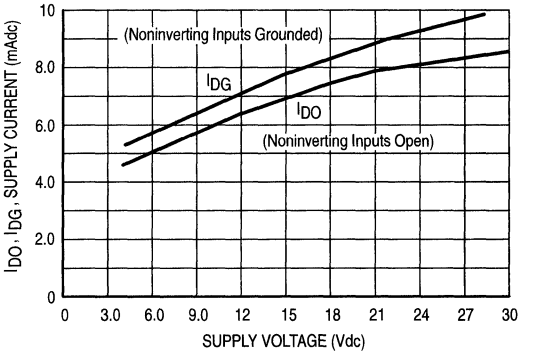


Figure 5. Analog Source Current versus Supply Voltage

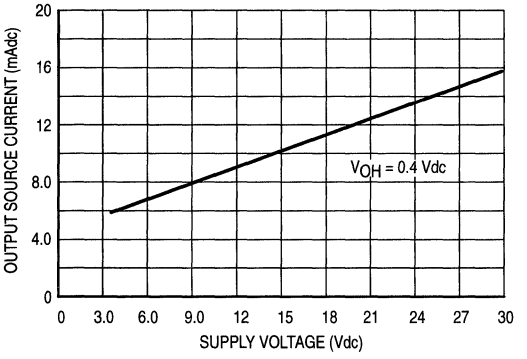
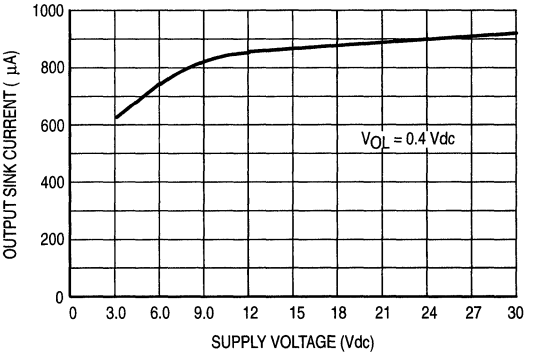


Figure 6. Analog Sink Current versus Supply Voltage



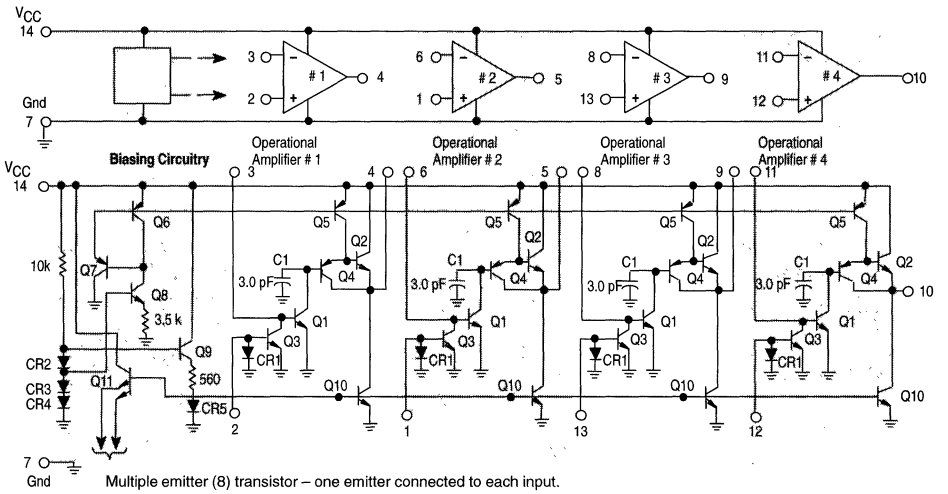
OPERATION AND APPLICATIONS

2

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 7 and 8. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased Class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled analog operation at the output. The sink of the device can be forced to exceed the specified level by keeping the output DC voltage above ≈ 1.0 V resulting in an increase in the distortion appearing at the output. Closed loop stability is maintained by an on–the–chip 3–pF capacitor shown in Figure 10 on the following page. No external compensation is required.

Figure 7. Block Diagram



Multiple emitter (8) transistor – one emitter connected to each input.

A noninverting input obtained by adding a current mirror as shown in Figure 9. Essentially all current which enters the noninverting input, I_{in}^+, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_{in}^+. Since the alpha current gain of Q3 ≈ 1, its collector current is approximately equal to I_{in}^+ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the DC quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

Figure 8. A Basic Gain Stage

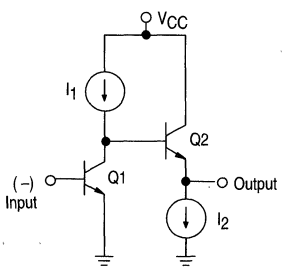
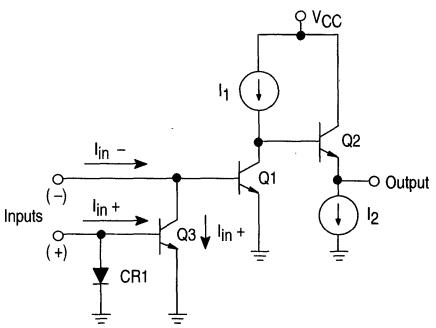


Figure 9. Obtaining A Noninverting Input



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 11. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude V_{BE}/R1 by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R_2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5; thus the current set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 7) provides circuit protection from signals that are negative with respect to ground.

Figure 10. A Basic Operational Amplifier

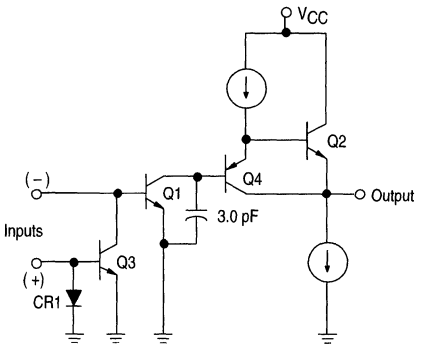
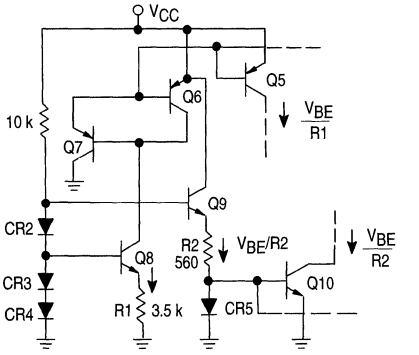


Figure 11. Biasing Circuitry



NORMAL DESIGN PROCEDURE

1. Output Q–Point Biasing
   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing, as shown in Figures 12 and 13. The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 μA to 200 μA range.

   B. V_{CC} Reference Voltage (see Figures 12 and 13)
   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor (R_r) allowing the input current, (I_{in}+) to be within the range of 10 μA to 200 μA.
   Choosing the feedback resistor (R_f) to be equal to $^1/_2$ R_r will now bias the amplifier output DC level to approximately $V_{CC}/2$. This allows the maximum dynamic range of the output voltage.

   C. Reference Voltage other than V_{CC} (see Figure 14)
   The biasing resistor (R_r) may be returned to a voltage(V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_{in} +between 10 μA and 200 μA) the output DC level will be equal to V_r. The expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(A_i)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_i\right) \phi$$

   where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_i is the current mirror gain.

2

Figure 12. Inverting Amplifier

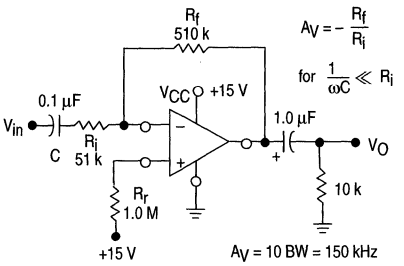
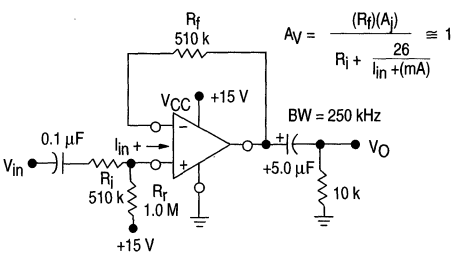


Figure 13. Noninverting Amplifier



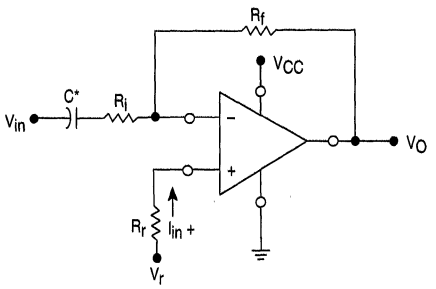
2. Gain Determination
   A. Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the DC bias and the output is normally capacitively coupled to eliminate the DC voltage across the load. Note that when the output is capacitively coupled to the load, the value of I_{sink} becomes a limitation with respect to the load driving capabilities of the device if it is direct coupled. In this configuration, the AC gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_V = \frac{R_f}{R_i}$$

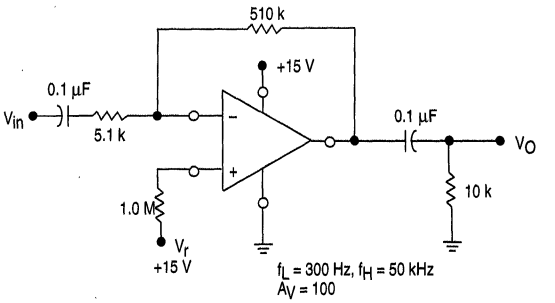
The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 400 kHz with 20 dB of closed loop gain or 40 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

Figure 14. Inverting Amplifier with Arbitrary Reference



*Select for low frequency response.

Figure 15. Inverting Amplifier with A_V = 100 and $V_r = V_{CC}$



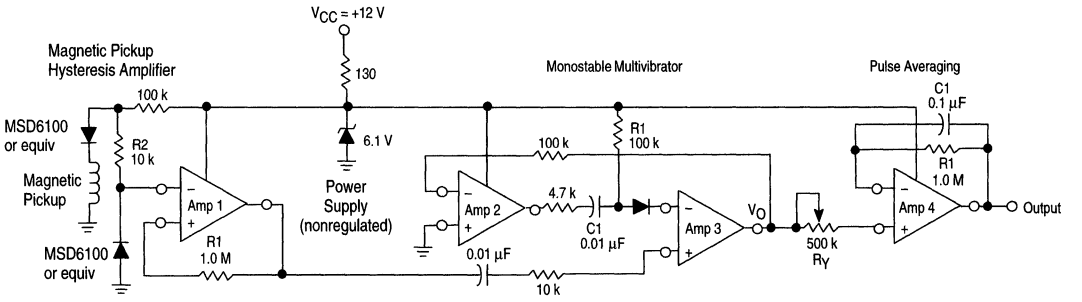
B. Noninverting Amplifier

These devices may be used in the noninverting mode (see Figure 13). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_{in+}}\ \Omega$, where $I_{in+}$is input current in milliamperes. The noninverting AC gain expression is given by:

$$A_V = \frac{(R_f)(A_i)}{R_i + \frac{26}{I_{in+}(mA)}}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the the input resistor is effectively isolated from the feedback loop.

Figure 16. Tachometer Circuit



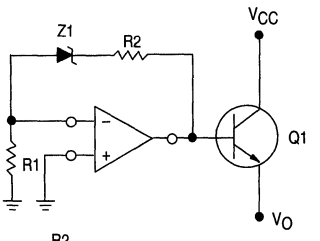
Hysteresis Voltage for Switching

$$V_H = \frac{A_i R2}{R1}(V_{CC} - 1.6)$$

Timing Interval: $t \approx 0.7\ R1\ C1$

$$V_{pp} \cong \frac{(V_O - 0.6) \bullet A_i \bullet t}{R_Y C1}$$

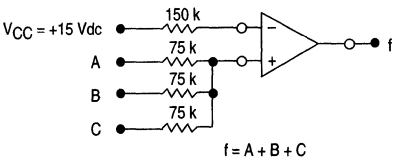
Figure 17. Voltage Regulator



$$V_O = V_{Z1} + 0.6\left(1 + \frac{R2}{R1}\right) - V_{BE\ Q1}$$

Note: For positive T_C zeners R2 and R1 can be selected to give T_C output.

Figure 18. Logic "OR" Gate



2

Figure 19. Logic "NAND" Gate (Large Fan–In)

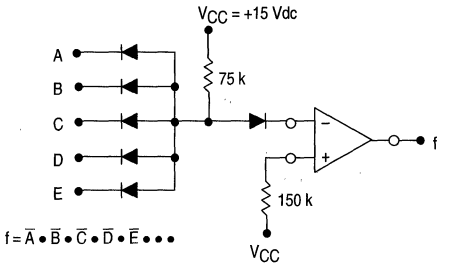


Figure 20. Logic "NOR" Gate

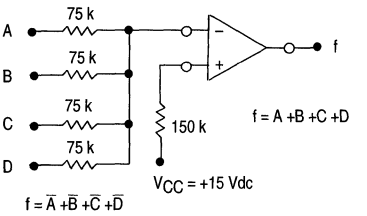


Figure 21. R–S Flip–Flop

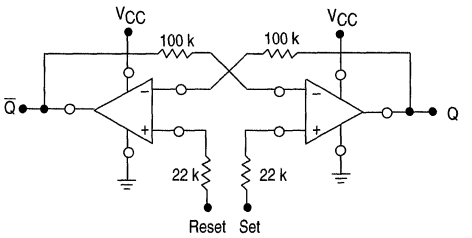


Figure 22. Astable Multivibrator

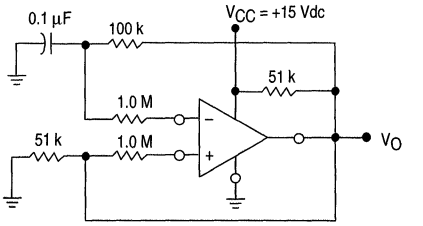


Figure 23. Positive–Edge Differentiator

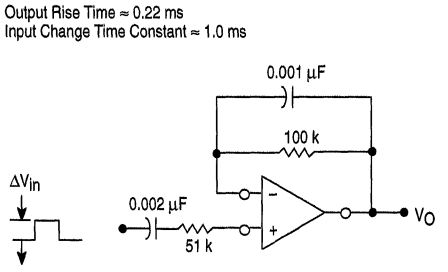


Figure 24. Negative–Edge Differentiator

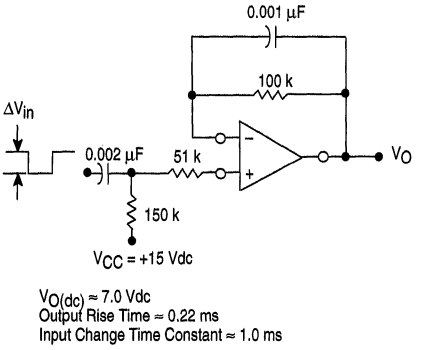


Figure 25. Amplifier and Driver for a 50 Ω Line

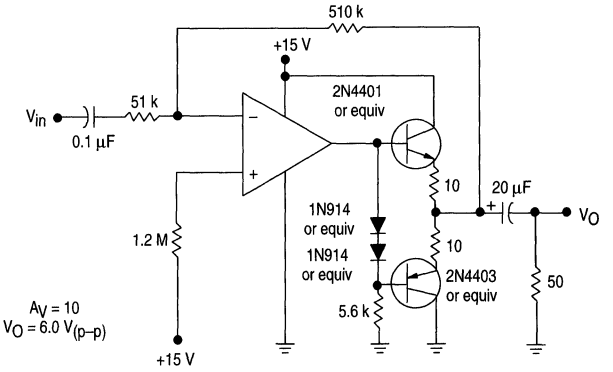


Figure 26. Basic Bandpass and Notch Filter

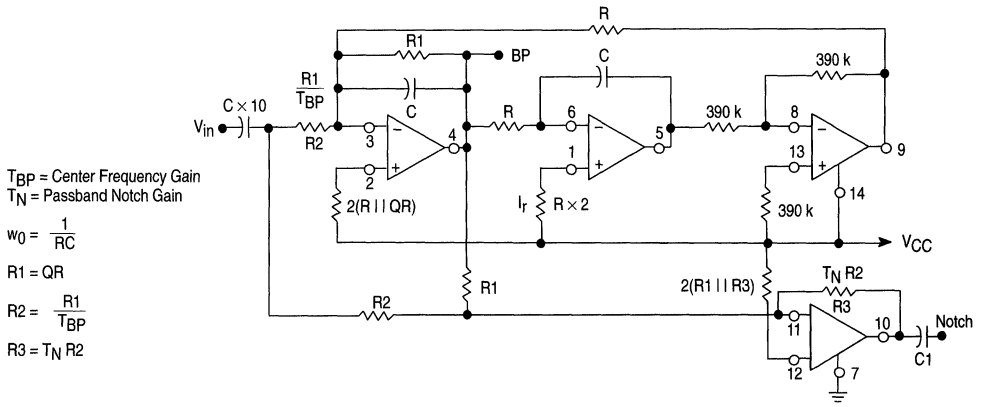
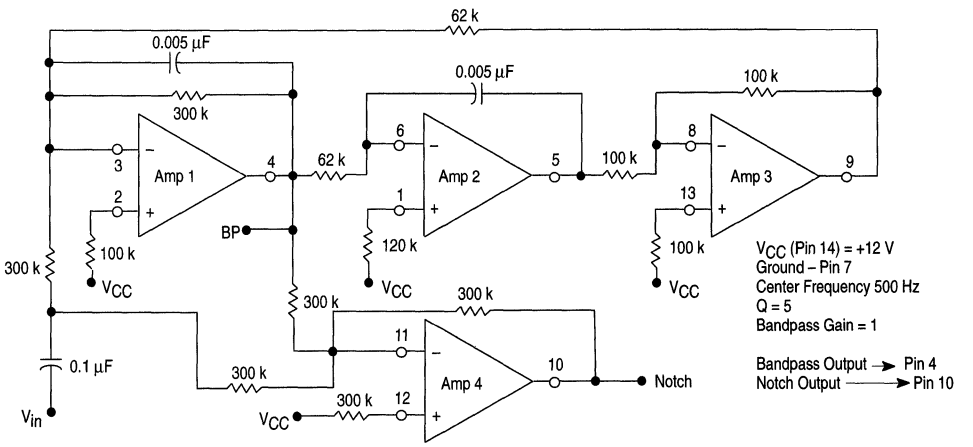
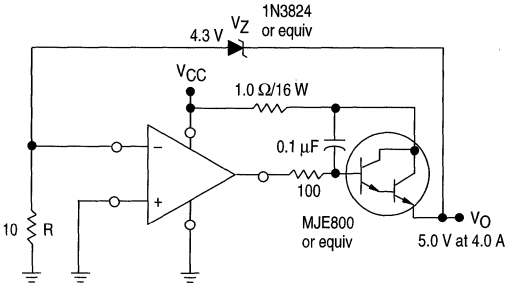


Figure 27. Bandpass and Notch Filter



2

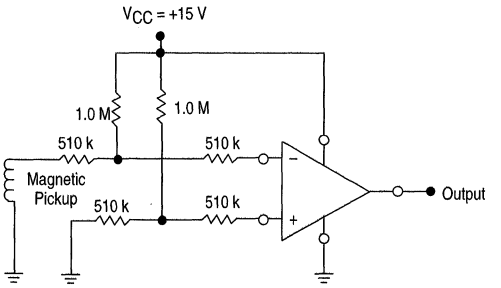
Figure 28. Voltage Regulator

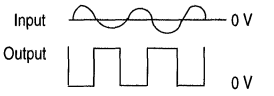


$V_O = V_Z + 0.6$ Vdc

NOTES: 1. R is used to bias the zener.
2. If the zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier (≈2.0 mV/°C), the output is zero–TC. A 7.0 V zener will give approximately zero–TC.

Figure 29. Zero Crossing Detector



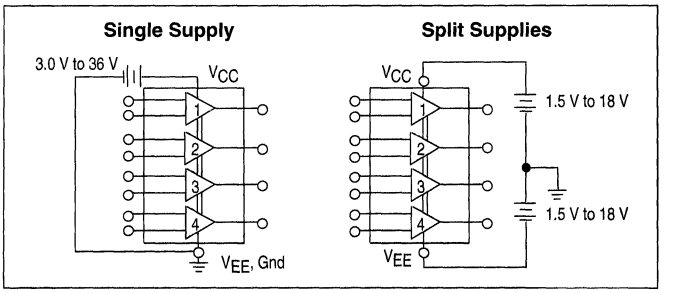


MOTOROLA

Quad Low Power Operational Amplifiers

The MC3403 is a low cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741C. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 36 V with quiescent currents about one third of those associated with the MC1741C (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 36 V
- Split Supply Operation: ±1.5 V to ±18 V
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Similar Performance to Popular MC1741C
- Industry Standard Pinouts
- ESD Diodes Added for Increased Ruggedness



MAXIMUM RATINGS

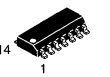
Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 36 ±18	Vdc
Input Differential Voltage Range (Note 1)	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range (Notes 1, 2)	V_{ICR}	±18	Vdc
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Ambient Temperature Range MC3303 MC3403	T_A	 −40 to +85 0 to +70	°C
Junction Temperature	T_J	150	°C

NOTES: 1. Split power supplies.
2. For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

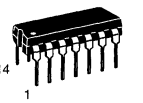
MC3403
MC3303

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

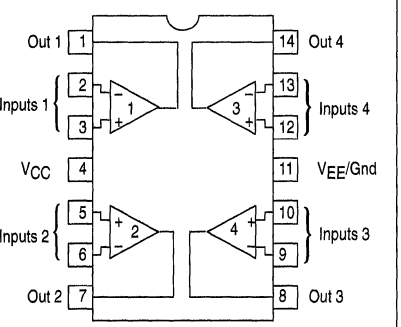


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3303D MC3303P	T_A = −40° to +85°C	SO–14 Plastic DIP
MC3403D MC3403P	T_A = 0° to +70°C	SO–14 Plastic DIP

2

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V for MC3403; V_{CC} = +14 V, V_{EE} = Gnd for MC3303 T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage T_A = T_{high} to T_{low} (Note 1)	V_{IO}	– –	2.0 –	10 12	– –	2.0 –	8.0 10	mV
Input Offset Current T_A = T_{high} to T_{low}	I_{IO}	– –	30 –	50 200	– –	30 –	75 250	nA
Large Signal Open Loop Voltage Gain V_O = ±10 V, R_L = 2.0 kΩ T_A = T_{high} to T_{low}	A_{VOL}	 20 15	 200 –	 – –	 20 15	 200 –	 – –	V/mV
Input Bias Current T_A = T_{high} to T_{low}	I_{IB}	– –	–200 –	–500 –800	– –	–200 –	–500 –1000	nA
Output Impedance f = 20 Hz	z_o	–	75	–	–	75	–	Ω
Input Impedance f = 20 Hz	z_i	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Range R_L = 10 kΩ R_L = 2.0 kΩ R_L = 2.0 kΩ, T_A = T_{high} to T_{low}	V_O	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	 12 10 10	 12.5 12 –	 – – –	V
Input Common Mode Voltage Range	V_{ICR}	+13 V $-V_{EE}$	+13 V $-V_{EE}$	–	+12 V $-V_{EE}$	+12.5 V $-V_{EE}$	–	V
Common Mode Rejection R_S ≤ 10 k Ω	CMR	70	90	–	70	90	–	dB
Power Supply Current (V_O = 0) R_L = ∞	I_{CC}, I_{EE}	–	2.8	7.0	–	2.8	7.0	mA
Individual Output Short–Circuit Current (Note 2)	I_{SC}	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	μV/V
Negative Power Supply Rejection Ratio	PSRR–	–	30	150	–	30	150	μV/V
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low}	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	pA/°C
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	μV/°C
Power Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 20 V(p–p), THD = 5%	BWp	–	9.0	–	–	9.0	–	kHz
Small–Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 50 mV	BW	–	1.0	–	–	1.0	–	MHz
Slew Rate A_V = 1, V_i = –10 V to +10 V	SR	–	0.6	–	–	0.6	–	V/μs
Rise Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	–	0.35	–	–	0.35	–	μs
Fall Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	–	0.35	–	–	0.35	–	μs
Overshoot A_V = 1, R_L = 10 kΩ, V_O = 50 mV	os	–	20	–	–	20	–	%
Phase Margin A_V = 1, R_L = 2.0 kΩ, V_O = 200 pF	ϕm	–	60	–	–	60	–	Degrees
Crossover Distortion (V_{in} = 30 mVpp, V_{out}= 2.0 Vpp, f = 10 kHz)	–	–	1.0	–	–	1.0	–	%

NOTES: 1. T_{high} = +70°C for MC3403, +85°C for MC3303
T_{low} = 0°C for MC3403, –40°C for MC3303
2. Not to exceed maximum package power dissipation.

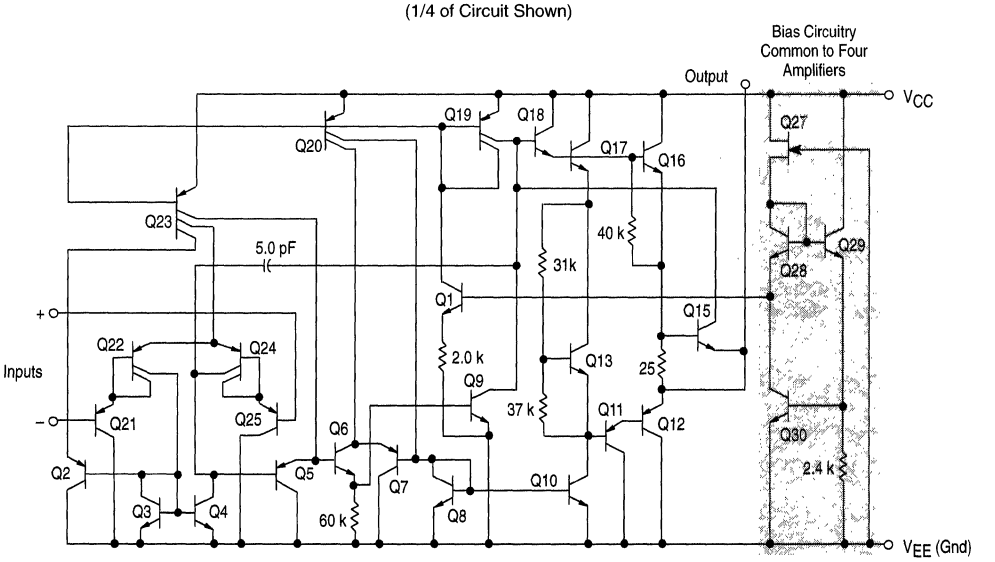
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	10	–	–	10	mV
Input Offset Current	I_{IO}	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	–200	–500	–	–	–500	nA
Large Signal Open Loop Voltage Gain R_L = 2.0 kΩ	A_{VOL}	10	200	–	10	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	μV/V
Output Voltage Range (Note 3) R_L = 10 kΩ, V_{CC} = 5.0 V R_L = 10 kΩ, 5.0 ≤ V_{CC} ≤ 30 V	V_{OR}	 3.3 V_{CC}–2.0	 3.5 V_{CC}–1.7	 – –	 3.3 V_{CC}–2.0	 3.5 V_{CC}–1.7	 – –	Vpp
Power Supply Current	I_{CC}	–	2.5	7.0	–	2.5	7.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	CS	–	–120	–	–	–120	–	dB

NOTES: 3. Output will swing to ground with a 10 kΩ pull down resistor.

Representative Schematic Diagram

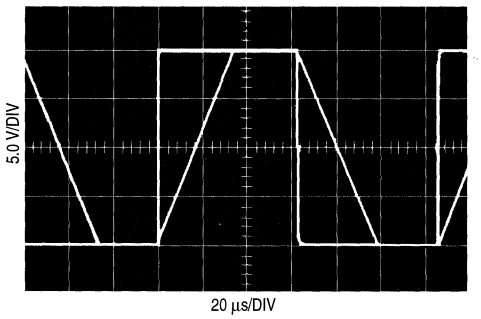
(1/4 of Circuit Shown)



CIRCUIT DESCRIPTION

2

Inverter Pulse Response



The MC3403/3303 is made using four internally compensated, two–stage operational amplifiers. The first stage of each consists of differential input device Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single–ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because Class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient, thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Figure 1. Sine Wave Response

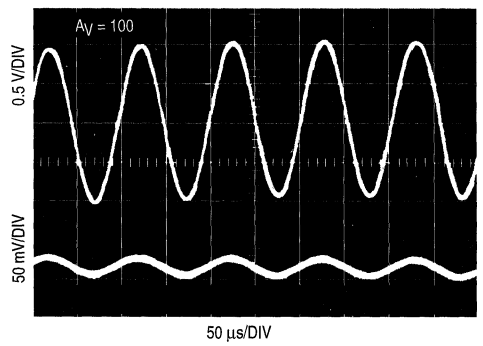


Figure 2. Open Loop Frequency Response

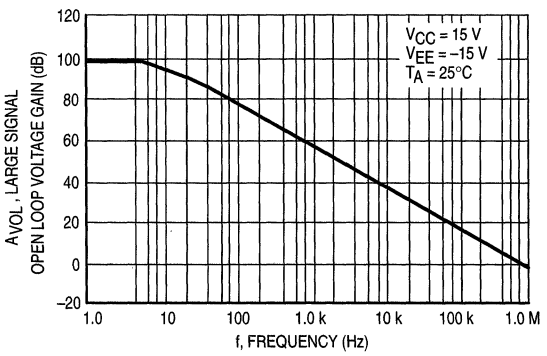


Figure 3. Power Bandwidth

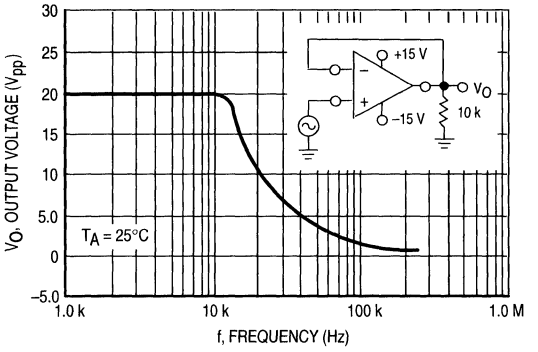


Figure 4. Output Swing versus Supply Voltage

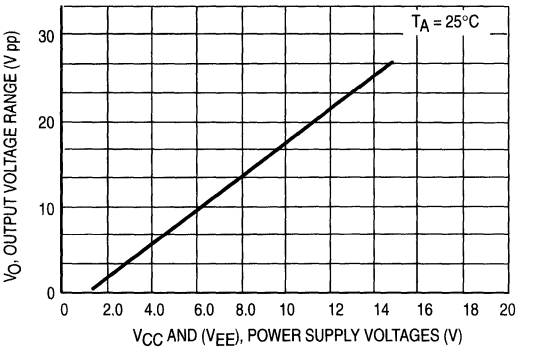


Figure 5. Input Bias Current versus Temperature

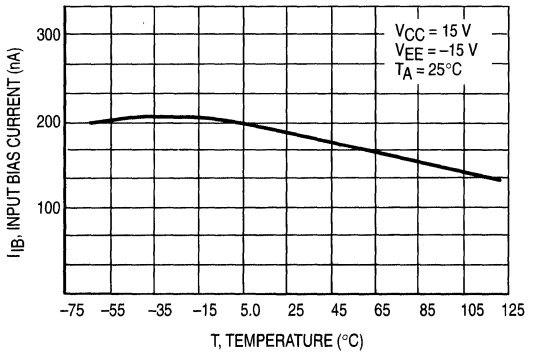


Figure 6. Input Bias Current versus Supply Voltage

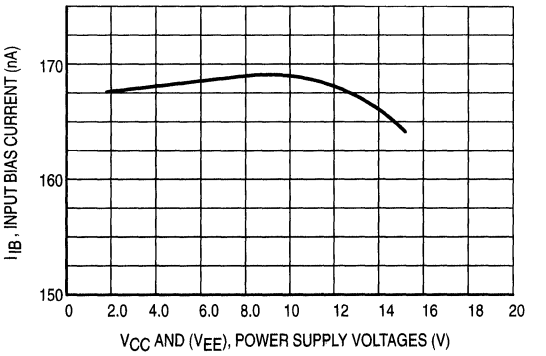


Figure 7. Voltage Reference

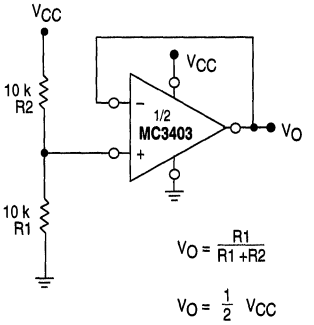
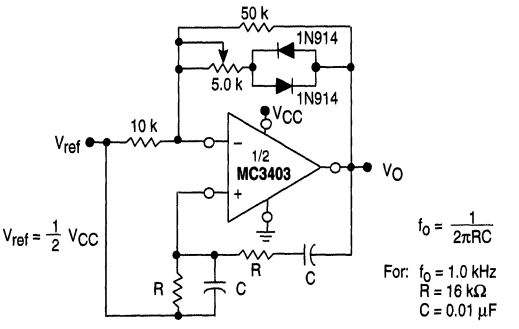


Figure 8. Wien Bridge Oscillator



2

Figure 9. High Impedance Differential Amplifier

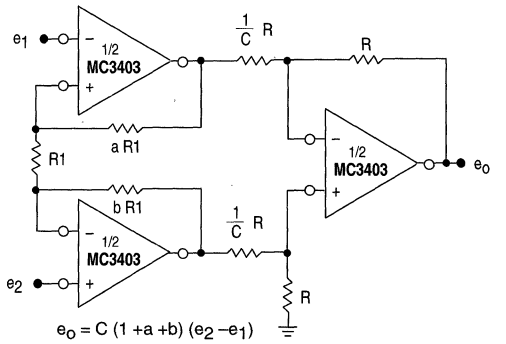


Figure 10. Comparator with Hysteresis

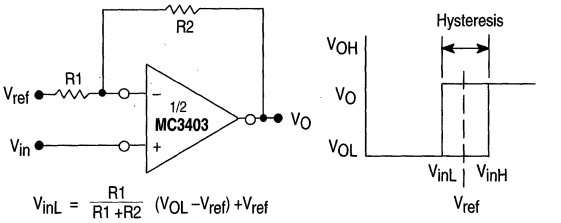
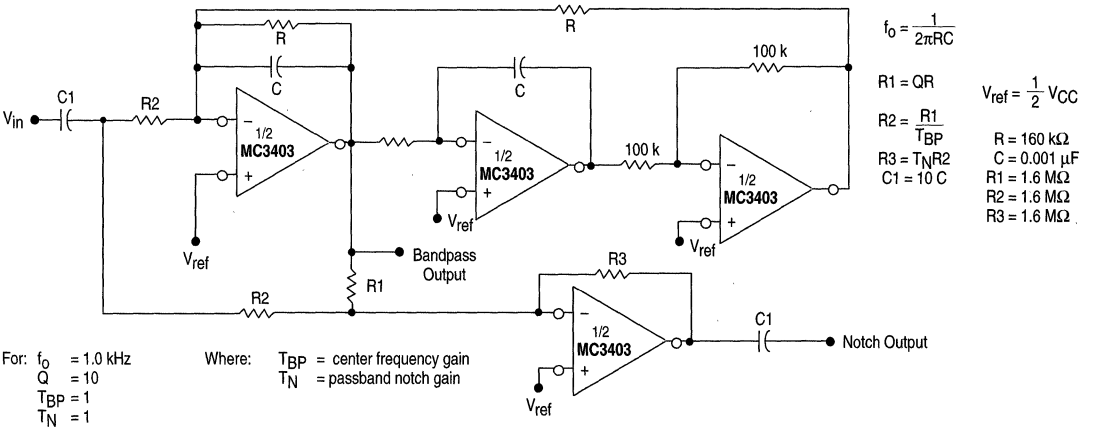


Figure 11. Bi–Quad Filter



For: f_o = 1.0 kHz, Q = 10, T_{BP} = 1, T_N = 1

Where: T_{BP} = center frequency gain, T_N = passband notch gain

Figure 12. Function Generator

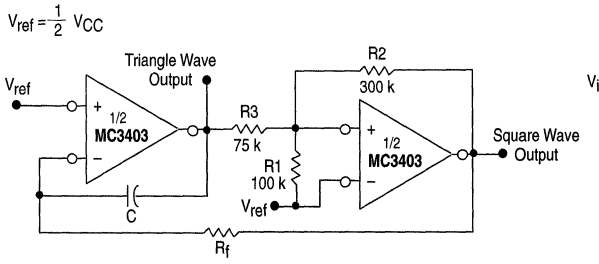
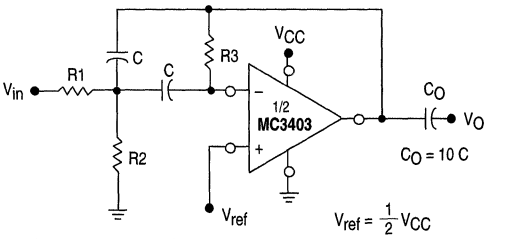


Figure 13. Multiple Feedback Bandpass Filter



Given: f_o = center frequency

$A(f_o)$ = gain at center frequency

Choose value f_o, C

Then: $R3 = \frac{Q}{\pi f_o C}$ $R1 = \frac{R3}{2 A(f_o)}$ $R2 = \frac{R1\,R5}{4Q^2\,R1 - R5}$

For less than 10% error from operational amplifier $\frac{O_o f_o}{BW} < 0.1$ where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MC3405

Dual Operational Amplifier and Dual Comparator

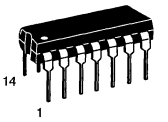
The MC3405 contains two differential–input operational amplifiers and two comparators, each set capable of single supply operation. This operational amplifier–comparator circuit fulfills its applications as a general purpose product for automotive and consumer circuits as well as an industrial building block.

The MC3405 is specified over the commercial operating temperature range of 0° to +70°C.

- Operational Amplifier Equivalent in Performance to MC3403
- Comparator Similar in Performance to LM339
- Single Supply Operation: 3.0 V to 36 V
- Split Supply Operation: ±1.5 V to ±18 V
- Low Supply Current Drain
- Operational Amplifier is Internally Frequency Compensated
- Comparator TTL and CMOS Compatible

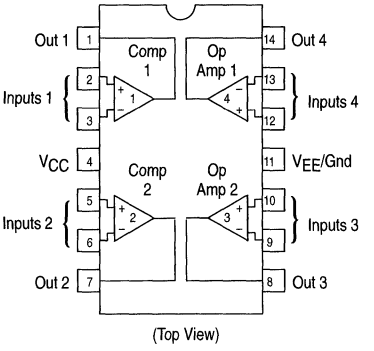
DUAL OPERATIONAL AMPLIFIER / DUAL VOLTAGE COMPARATOR

SEMICONDUCTOR TECHNICAL DATA



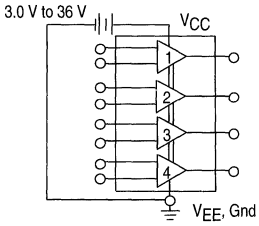
P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS

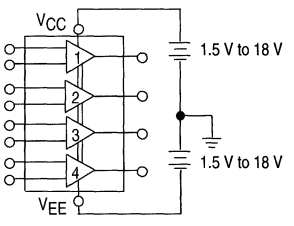


(Top View)

Single Supply



Split Supplies



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3405P	T_A = 0° to +70°C	Plastic DIP

OPERATIONAL AMPLIFIER SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage – Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ±18	Vdc
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	±18	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	Tstg	–55 to +125	°C
Operating Junction Temperature Range	T_J	150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	–	2.0	10	mV
Input Offset Current	I_{IO}	–	30	50	nA
Input Bias Current	I_{IB}	–	–200	–500	nA
Large–Signal, Open Loop Voltage Gain (R_L = 2.0 kΩ)	A_{VOL}	20	200	–	V/mV
Power Supply Rejection	PSR	–	–	150	µV/V
Output Voltage Range (Note 1) (R_L = 10 kΩ, V_{CC} = 5.0 V) (R_L = 10 kΩ, 5.0 V ≤ V_{CC} ≤ 30 V)	V_{OR}	 3.3 V_{CC}–2.0	 3.5 V_{CC}–1.7	 – –	V_{pp}
Power Supply Current (Notes 2 and 3)	I_{CC}	–	2.5	7.0	mA
Channel Separation, f = 1.0 kHz to 20 kHz (Input Referenced)	–	–	–120	–	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (T_A = T_{low} + T_{high}) (Note 4)	V_{IO}	– –	2.0 –	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	µV/°C
Input Offset Current (T_A = T_{low} to T_{high}) (Note 4)	I_{IO}	– –	– –	50 200	nA
Input Bias Current (T_A = T_{low} to T_{high}) (Note 4)	I_{IB}	– –	–200 –	–500 –800	nA
Input Common Mode Voltage Range	V_{ICR}	+13 –V_{EE}	–	–	Vdc
Large Signal, Open Loop Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) (T_A = T_{low} to T_{high}) (Note 4)	A_{VOL}	 20 15	 200 100	 – –	V/mV
Common Mode Rejection	CMR	70	90	–	dB
Power Supply Rejection Ratio	PSRR	–	30	150	µV/V
Output Voltage (R_L = 10 kΩ) (R_L = 2.0 kΩ) (R_L = 2.0 kΩ, T_A = T_{low} to T_{high}) (Note 4)	V_O	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	Vdc
Output Short Circuit Current	I_{SC}	±10	±20	±45	mA
Power Supply Current (Notes 2 and 3)	I_{CC}, I_{EE}	–	2.8	7.0	mA
Phase Margin	ϕm	–	60	–	Degrees
Small–Signal Bandwidth (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	BW	–	1.0	–	MHz

NOTES: 1. Output will swing to ground.
2. Not to exceed maximum package power dissipation.
3. For operational amplifier and comparator.
4. T_{low} = 0°C, T_{high} = +70°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Bandwidth (A_V = 1, R_L = 2.0 kΩ, V_O = 20 V_{pp}, THD = 5%)	BWp	–	9.0	–	kHz
Rise Time/Fall Time	t_{TLH}, t_{THL}	–	0.35	–	µs
Overshoot (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	os	–	20	–	%
Slew Rate	SR	–	0.6	–	V/µs

COMPARATOR SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage – Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ±18	Vdc
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	–0.3 to +36	Vdc
Sink Current	I_{Sink}	20	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	Tstg	–55 to +125	°C
Operating Junction Temperature Range	T_J	150	°C

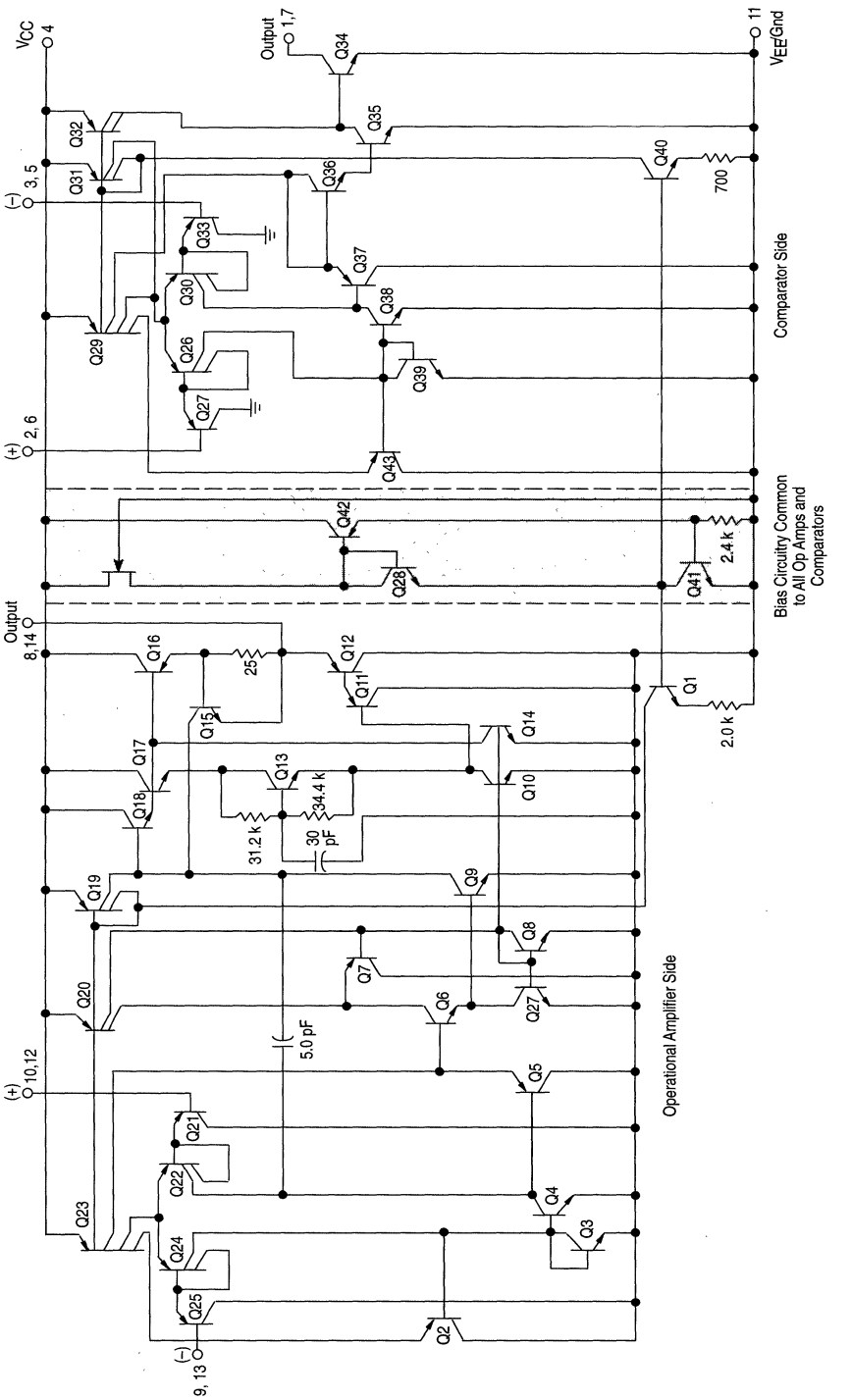
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (T_A = T_{low} to T_{high}) (Notes 1 and 2)	V_{IO}	– –	2.0 –	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	µV/°C
Input Offset Current (T_A = T_{low} to T_{high}) (Note 1)	I_{IO}	– –	50 –	100 200	nA
Input Bias Current (T_A = T_{low} to T_{high}) (Note 1)	I_{IB}	– –	–125 –	–500 –800	nA
Input Common Mode Voltage Range (T_A = T_{low} to T_{high}) (Note 1)	V_{ICR}	0 0	V_{CC} –1.5 V_{CC} –1.7	V_{CC} –1.7 V_{CC} –2.0	Vpp
Input Differential Voltage (All V_{in} ≥ 0 Vdc)	V_{ID}	–	–	36	V
Large–Signal, Open Loop Voltage Gain (R_L = 15 kΩ)	A_{VOL}	–	200	–	V/mV
Output Sink Current (–V_{in} ≥ 1.0 Vdc, +V_{in}= 0, V_O ≤ 1.5 V)	I_{Sink}	6.0	16	–	mA
Low Level Output Voltage (+V_{in}= 0 V, –V_{in}= 1.0 V, I_{Sink} = 4.0 mA) (T_A = T_{low} to T_{high}) (Note 1)	V_{OL}	 – –	 350 –	 500 700	µA
Output Leakage Current (+V_{in} ≥ 1.0 Vdc, –V_{in}= 0, V_O = 5.0 Vdc) (T_A = T_{low} to T_{high}) (Note 1)	I_{OL}	 – –	 0.1 0.1	 1.0 1.0	µA
Large–Signal Response	–	–	300	–	ns
Response Time (Note 3) (V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ)	–	–	1.3	–	µs

NOTES: 1. T_{low} = 0°C, T_{high} = +70°C
2. $V_O \cong$ 1.4 V, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the input common mode range 0 to V_{CC} –1.7 V.
3. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals 300 ns is typical.

2

Representative Schematic Diagram
(1/2 of Circuit Shown)



OPERATIONAL AMPLIFIER SECTION

Figure 1. Sine Wave Response

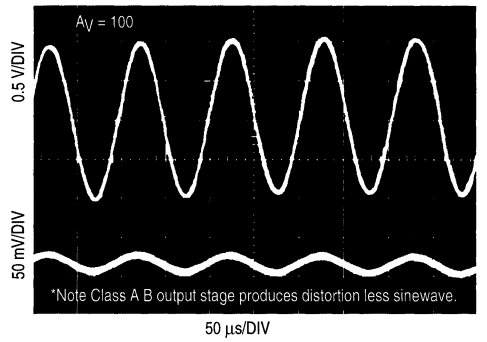


Figure 2. Open Loop Frequency Response

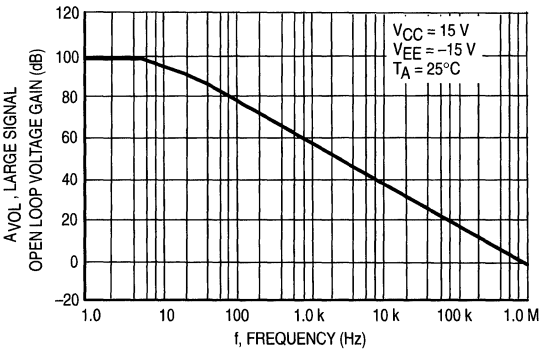


Figure 3. Power Bandwidth

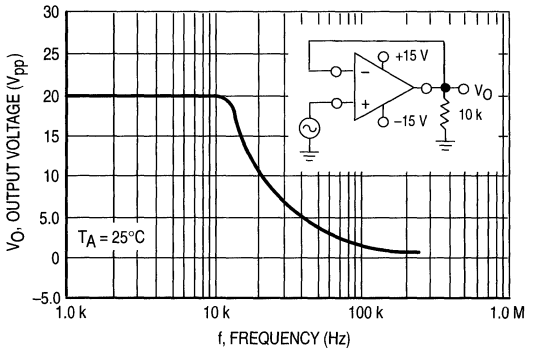


Figure 4. Output Swing versus Supply Voltage

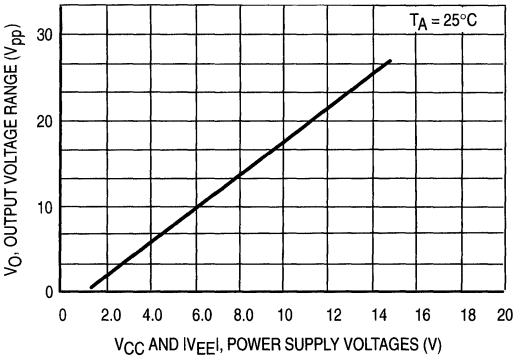


Figure 5. Input Bias Current versus Temperature

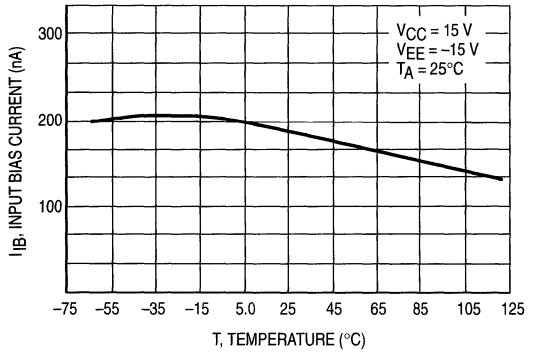
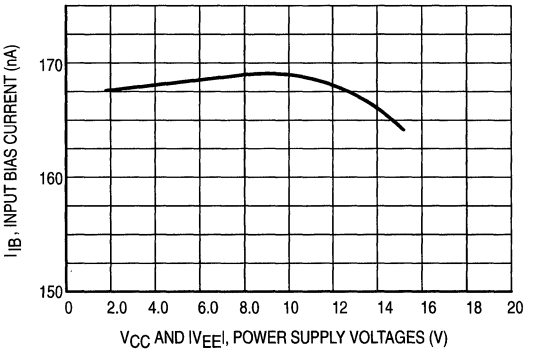


Figure 6. Input Bias Current versus Supply Voltage



COMPARATOR SECTION

2

Figure 7. Normalized Input Offset Voltage

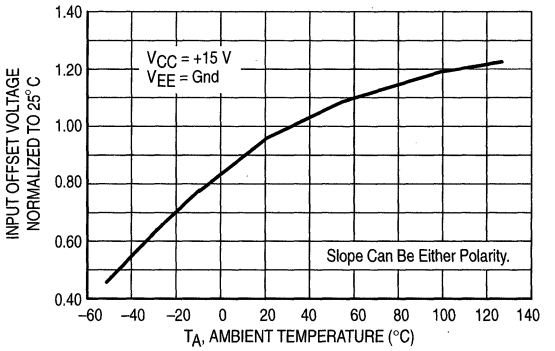


Figure 8. Input Bias Current

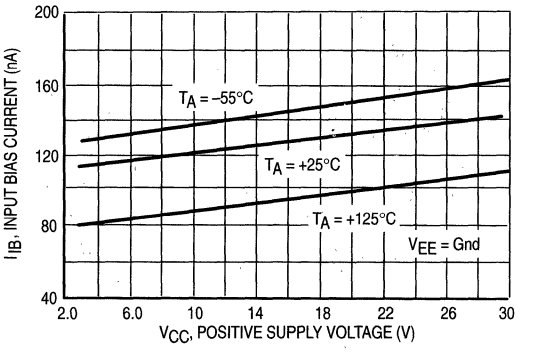


Figure 9. Normalized Input Offset Current

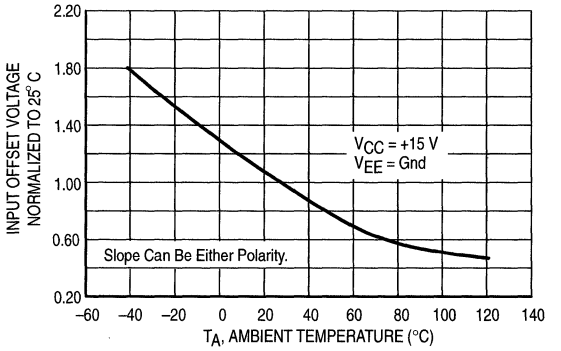


Figure 10. Output Sink Current versus Output Voltage

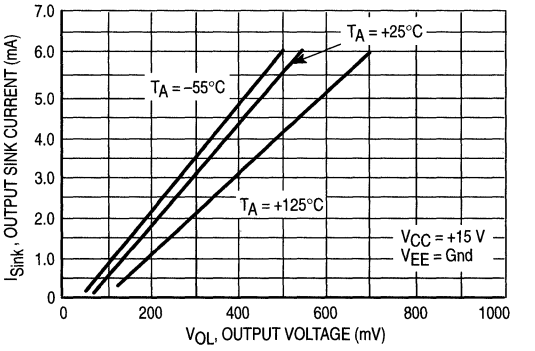
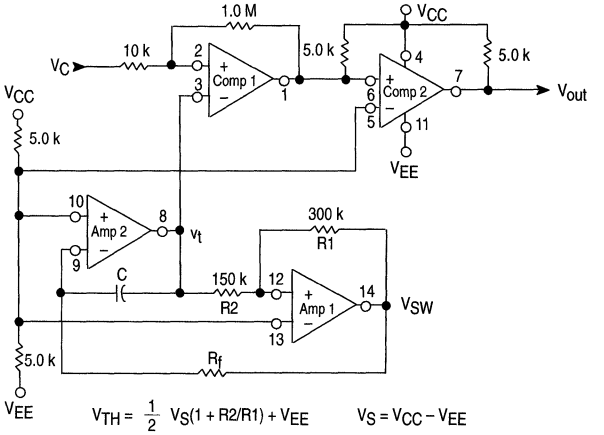


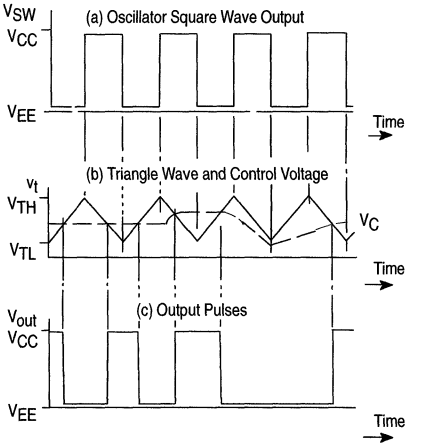
Figure 11. Pulse Width Modulator Schematic and Waveforms



$$V_{TH} = \frac{1}{2} V_S(1 + R2/R1) + V_{EE} \qquad V_S = V_{CC} - V_{EE}$$

$$V_{TL} = \frac{1}{2} V_S(1 - R2/R1) + V_{EE}$$

$$\text{Oscillator Frequency } f = \frac{R1}{4R_fCR2}$$



$$\text{Pulse Width} = \left(\frac{1}{f}\right)\left(\frac{V_C - V_{TL}}{V_{TH} - V_{TL}}\right) \text{ when: } V_{TL} < V_C < V_{TH}$$

$$\text{Duty Cycle in \%} = \left(\frac{V_C - V_{TL}}{V_{TH} - V_{TL}}\right)(100)$$

Figure 12. Window Comparator

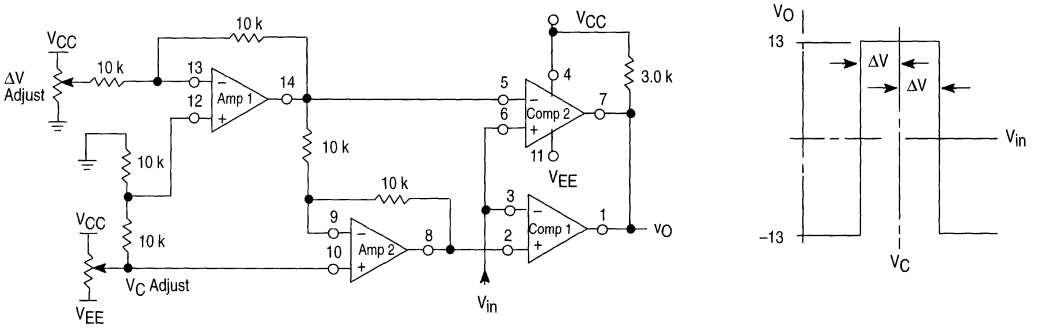
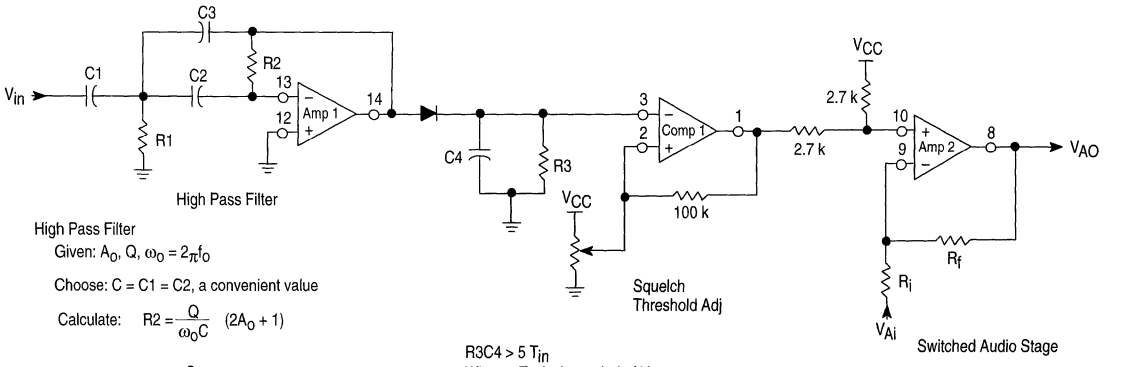


Figure 13. Squelch Circuit for AM or FM



High Pass Filter

Given: A_o, Q, $\omega_o = 2\pi f_o$

Choose: C = C1 = C2, a convenient value

Calculate: $R2 = \frac{Q}{\omega_o C}(2A_o + 1)$

$C3 = \frac{C}{A_o}$

$R1 = \frac{A_o}{Q\omega_o C(2A_o + 1)}$

$R3C4 > 5\,T_{in}$

Where : T_{in} is the period of V_{in}

Q = Quality Factor

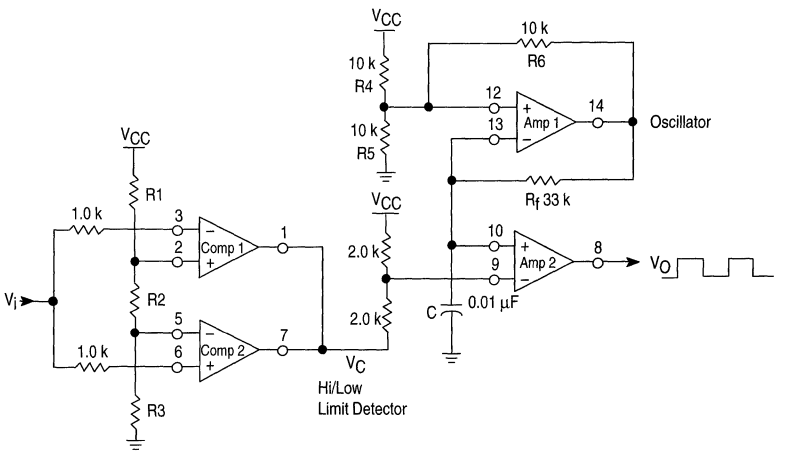
A_o = High Frequency Gain

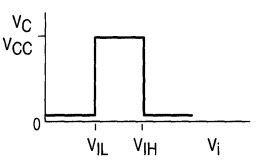
ω_o = Break Frequency

Gain of Audio Stage

$A_{CL} = \frac{R_f}{R_i}$

Figure 14. High/Low Limit Alarm





$V_{IL} = V_{CC}\,\frac{R3}{R1 + R2 + R3}$

$V_{IH} = V_{CC}\,\frac{R2 + R3}{R1 + R2 + R3}$

Oscillator

If R4 = R5 = R6

$f = 0.72/R_fC$

As shown, f = 2.2 kHz

V_O will oscillate if $V_{IH} < V_i$, or $V_{IL} > V_i$

V_O will be low if $V_{IL} < V_i < V_{IH}$

2

Figure 15. Zero Crossing Detector with Temperature Sensor

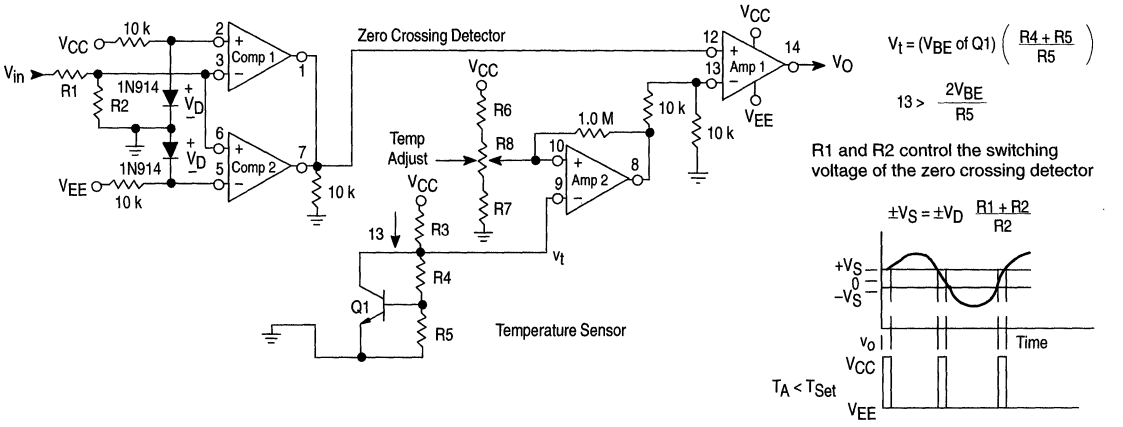
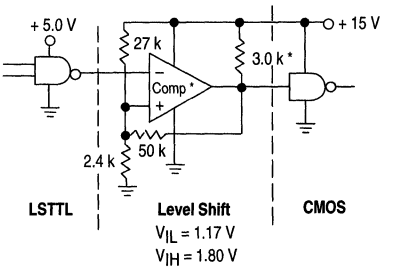
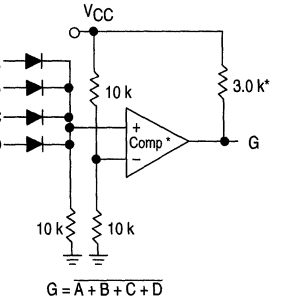


Figure 16. LSTTL to CMOS Interface with Hysteresis



* The same configuration may be used with an op amp if the 3.0 k resistor is removed.

Figure 17. NOR Gate



* The same configuration may be used with an op amp if the 3.0 k resistor is removed.

MC3458
MC3358

Dual, Low Power Operational Amplifiers

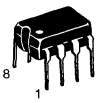
Utilizing the circuit designs perfected for the quad operational amplifiers, these dual operational amplifiers feature: 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, and 3) Single Supply or Split Supply operation.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 36 V with quiescent currents about one–fifth of those associated with the MC1741C (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 36 V
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Class AB Output Stage for Minimum Crossover Distortion
- Single and Split Supply Operations Available
- Similar Performance to the Popular MC1458

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

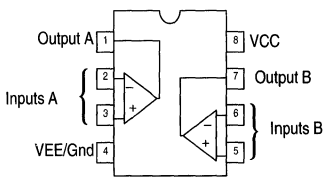
SEMICONDUCTOR TECHNICAL DATA



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 36 ±18	Vdc
Input Differential Voltage Range (1)	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	±15	Vdc
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Operating Ambient Temperature Range MC3458 MC3358	T_A	 0 to +70 –40 to +85	°C

NOTES: 1. Split Power Supplies.
2. For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3358P1	T_A = –40° to +85°C	Plastic DIP
MC3458D	T_A = 0° to +70°C	SO–8
MC3458P1		Plastic DIP

2

ELECTRICAL CHARACTERISTICS (For MC3458, V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)
(For MC3358, V_{CC} = +14 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $T_A = T_{high}$ to T_{low} (Note 1)	V_{IO}	– –	2.0 –	10 12	– –	2.0 –	8.0 10	mV
Input Offset Current $T_A = T_{high}$ to T_{low}	I_{IO}	– –	30 –	50 200	– –	30 –	75 250	nA
Large Signal Open Loop Voltage Gain V_O = ±10 V, R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}	A_{VOL}	 20 15	 200 –	 – –	 20 15	 200 –	 – –	V/mV
Input Bias Current $T_A = T_{high}$ to T_{low}	I_{IB}	– –	–200 –	–500 –800	– –	–200 –	–500 –1000	nA
Output Impedance, f = 20 Hz	z_O	–	75	–	–	75	–	Ω
Input Impedance, f = 20 Hz	z_I	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Range R_L = 10 kΩ R_L = 2.0 kΩ R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}	V_{OR}	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	 12 10 10	 12.5 12 –	 – – –	V
Input Common Mode Voltage Range	V_{ICR}	+13 $-V_{EE}$	+13.5 $-V_{EE}$	–	+13 $-V_{EE}$	+13.5 $-V_{EE}$	–	V
Common Mode Rejection Ratio, $R_S \leq 10$ kΩ	CMR	70	90	–	70	90	–	dB
Power Supply Current (V_O = 0) R_L = ∞	I_{CC}, I_{EE}	–	1.6	3.7	–	1.6	3.7	mA
Individual Output Short Circuit Current (Note 2)	I_{SC}	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	μV/V
Negative Power Supply Rejection Ratio	PSRR–	–	30	150	–	–	–	μV/V
Average Temperature Coefficient of Input Offset Current, $T_A = T_{high}$ to T_{low}	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	pA/°C
Average Temperature Coefficient of Input Offset Current, $T_A = T_{high}$ to T_{low}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	μV/°C
Power Bandwidth A_V = 1, R_L = 2.0 kΩ, V_O = 20 V_{pp}, THD = 5%	BWp	–	9.0	–	–	9.0	–	kHz
Small Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 50 mV	BW	–	1.0	–	–	1.0	–	MHz
Slew Rate A_V = 1, V_I = –10 V to +10 V	SR	–	0.6	–	–	0.6	–	V/μs
Rise Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	–	0.35	–	–	0.35	–	μs
Fall Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{THL}	–	0.35	–	–	0.35	–	μs
Overshoot A_V = 1, R_L = 10 kΩ, V_O = 50 mV	os	–	20	–	–	20	–	%
Phase Margin A_V = 1, R_L = 2.0 kΩ, C_L = 200 pF	ϕm	–	60	–	–	60	–	Degrees
Crossover Distortion (V_{in} = 30 mV_{pp}, V_{out} = 2.0 V_{pp}, f = 10 kHz)	–	–	1.0	–	–	1.0	–	%

NOTES: 1. T_{high} = 70°C for MC3458, 85°C for MC3358
T_{low} = 0°C for MC3458, –40°C for MC3358
2. Not to exceed maximum package power dissipation.

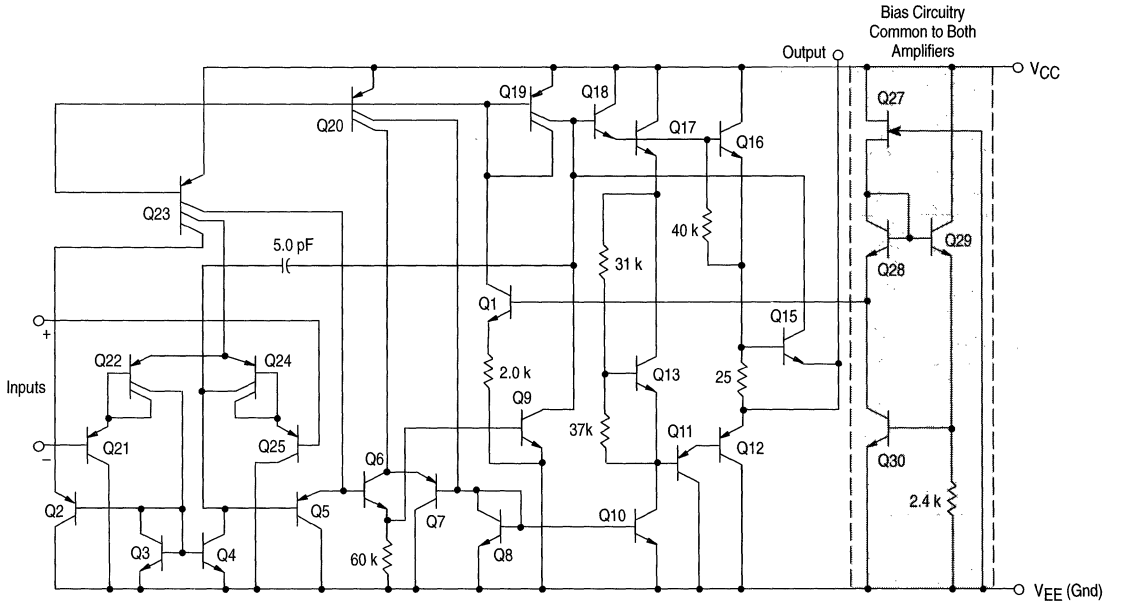
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	mV
Input Offset Current	I_{IO}	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	–200	–500	–	–	–500	nA
Large Signal Open Loop Voltage Gain R_L = 2.0 kΩ,	A_{VOL}	20	200	–	20	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	μV/V
Output Voltage Range (Note 3) R_L = 10 kΩ, V_{CC} = 5.0 V R_L = 10 kΩ, 5.0 V ≤ V_{CC} ≤ 30 V	V_{OR}	 3.3 –	 3.5 V_{CC} –1.7	 – –	 3.3 –	 3.5 V_{CC} –1.7	 – –	V_{pp}
Power Supply Current	I_{CC}	–	2.5	7.0	–	2.5	4.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	CS	–	–120	–	–	–120	–	dB

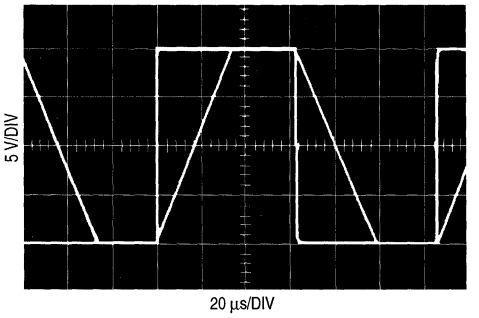
NOTE: 3. Output will swing to ground with a 10 kΩ pull down resistor.

2

Representative Schematic Diagram
(1/2 of Circuit Shown)



Inverter Pulse Response



CIRCUIT DESCRIPTION

The MC3458/3358 is made using two internally compensated, two–stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input Common Mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single–ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because Class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Figure 1. Sine Wave Response

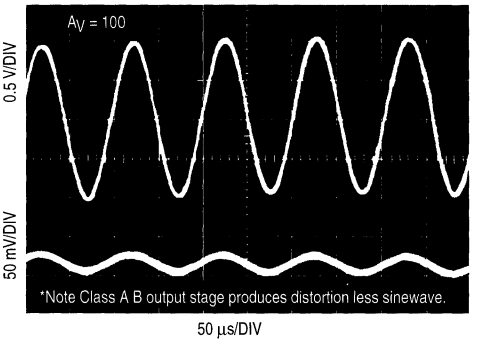


Figure 2. Open Loop Frequency Response

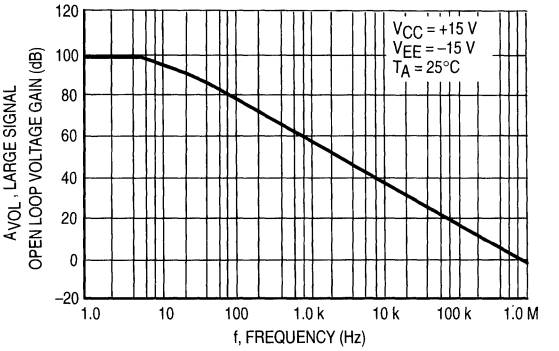


Figure 3. Power Bandwidth

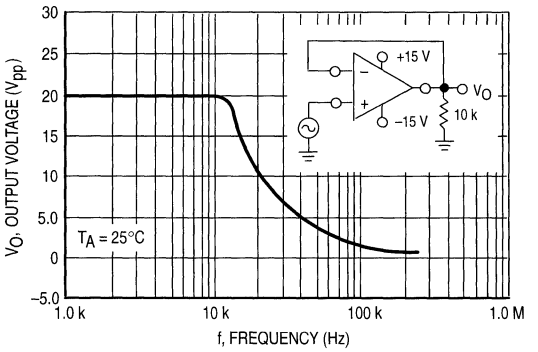


Figure 4. Output Swing versus Supply Voltage

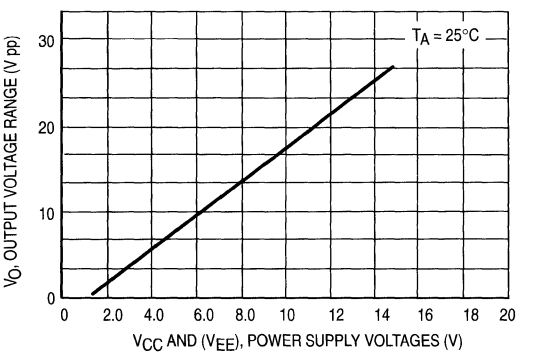


Figure 5. Input Bias Current versus Temperature

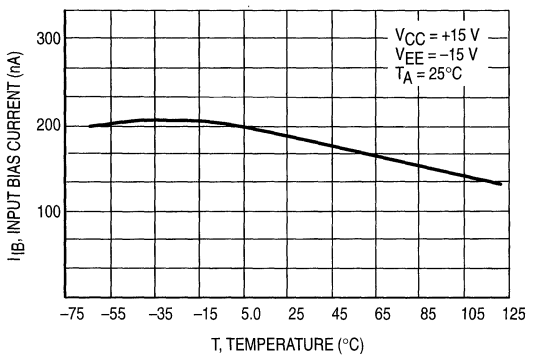
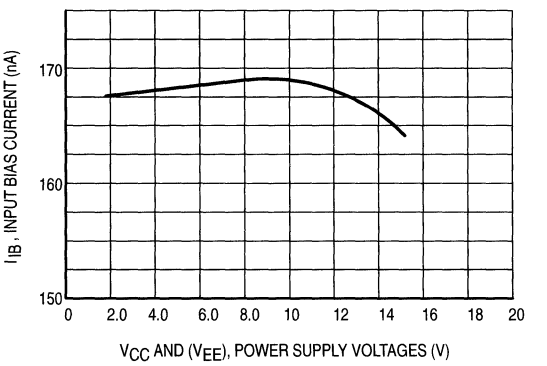


Figure 6. Input Bias Current versus Supply Voltage



2

Figure 7. Voltage Reference

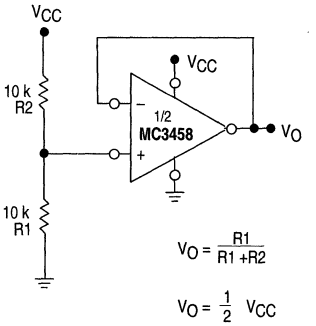


Figure 8. Wien Bridge Oscillator

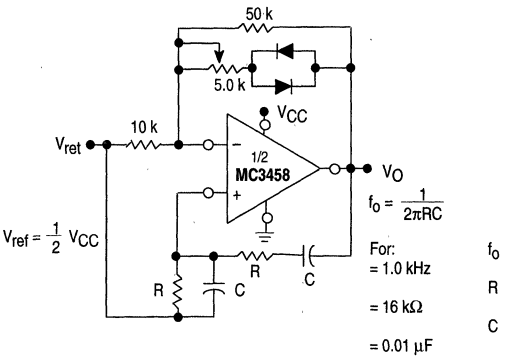


Figure 9. High Impedance Differential Amplifier

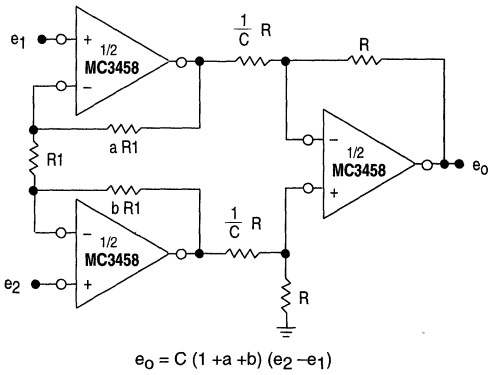


Figure 10. Comparator with Hysteresis

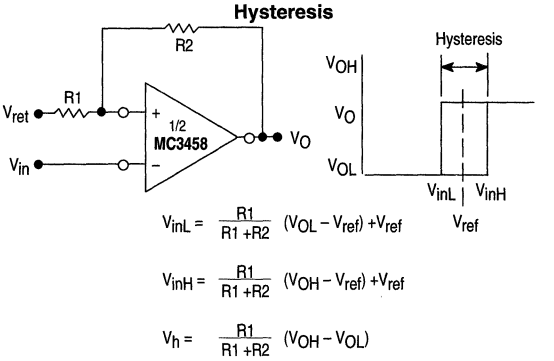


Figure 11. Bi–Quad Filter

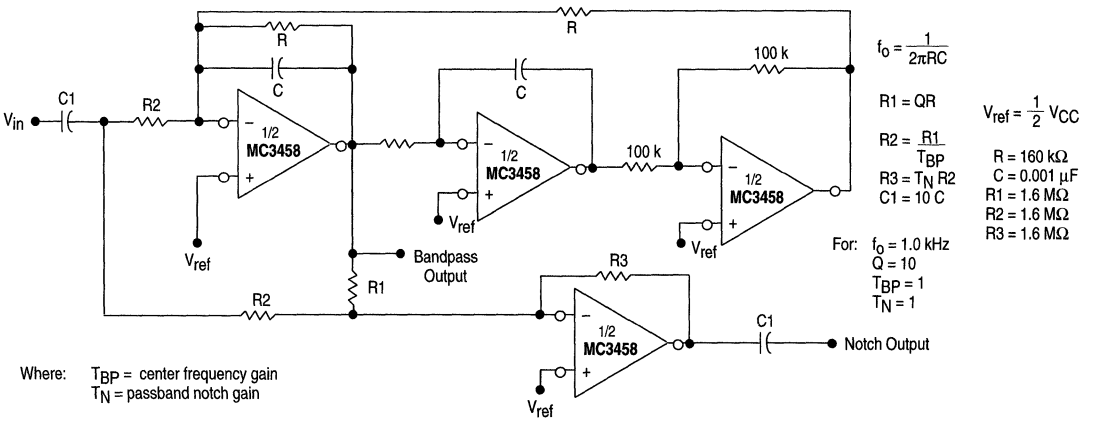
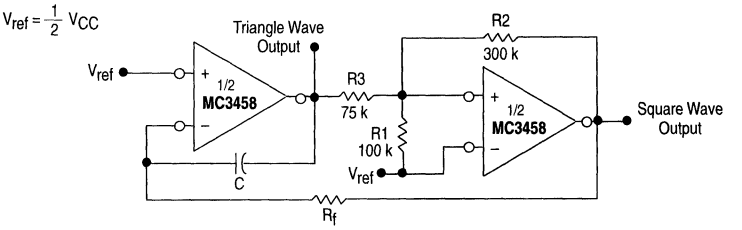
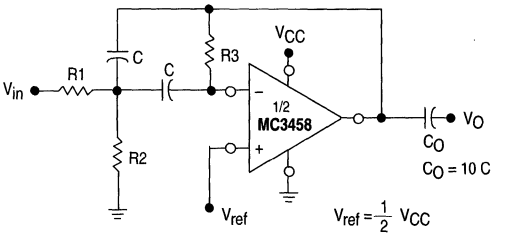


Figure 12. Function Generator



$$f = \frac{R1 + R_C}{4\,C R_f\,R1} \quad \text{if,} \quad R3 = \frac{R2\,R1}{R2 + R1}$$

Figure 13. Multiple Feedback Bandpass Filter



Given: f_0 = center frequency

$A(f_0)$ = gain at center frequency

Choose value f_0, C.

Then: $R3 = \frac{Q}{\pi f_0 C}$ $R1 = \frac{R3}{2\,A(f_0)}$ $R2 = \frac{R1\,R5}{4Q^2\,R1 - R3}$

For less than 10% error from operational amplifier $\frac{Q_0 f_0}{BW} < 0.1$

where, f_0 and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MC3476

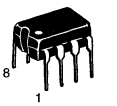
Low Cost Programmable Operational Amplifier

The MC3476 is a low cost selection of the popular industry standard MC1776 programmable operational amplifier. This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

- ±6.0 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short Circuit Protection

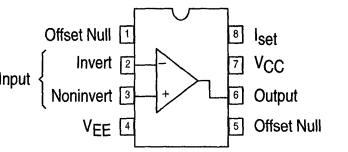
LOW COST PROGRAMMABLE OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

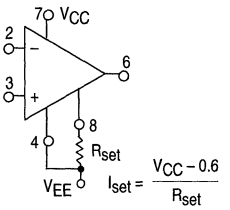
PIN CONNECTIONS



(Top View)

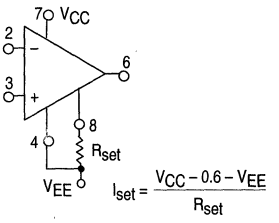
Resistive Programming
(See Figure 1)

R_{set} to Ground



Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 µA	I_{set} = 15 µA
±6.0 V	3.6 MΩ	360 kΩ
±10 V	6.2 MΩ	620 kΩ
±12 V	7.5 MΩ	750 kΩ
±15 V	10 MΩ	1.0 MΩ

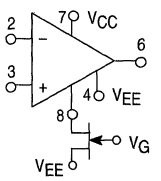
R_{set} to Negative Supply
(Recommended for supply voltage less than ±6.0 V)



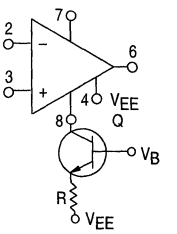
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 µA	I_{set} = 15 µA
+1.5 V	1.6 MΩ	160 kΩ
+3.0 V	3.6 MΩ	360 kΩ
+6.0 V	7.5 MΩ	750 kΩ
+15 V	20 MΩ	2.0 MΩ

Active Programming

FET Current Source



Bipolar Current Source



Pins not shown are not connected.

ORDERING INFORMATION

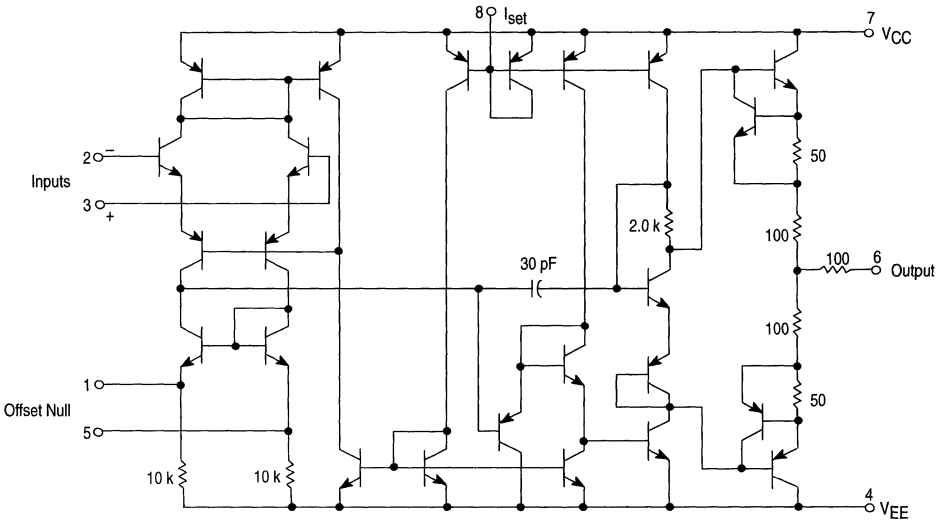
Device	Operating Temperature Range	Package
MC3476P1	T_A = 0° to +70°C	Plastic DIP

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

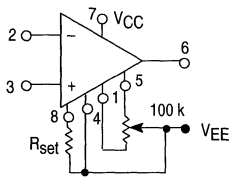
Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Input Differential Voltage Range	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range	V_{ICR}	V_{CC}, V_{EE}	Vdc
Offset Null to V_{EE} Voltage	$V_{off} - V_{EE}$	±0.5	Vdc
Programming Current	I_{set}	200	μA
Programming Voltage (Voltage from I_{set} Terminal to Ground)	V_{set}	(V_{CC} – 0.6 V) to V_{CC}	Vdc
Output Short Circuit Duration (Note 1)	t_{SC}	Indefinite	sec
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	– 55 ot +125	°C
Junction Temperature	T_J	150	°C

NOTES: 1. Short circuit to ground with $I_{set} \leq 15$ μA. Rating applies up to ambient temperature of +70°C.

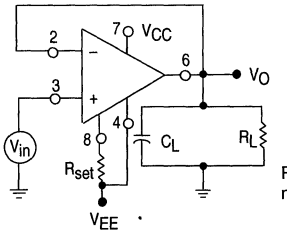
Representative Schematic Diagram



Voltage Offset Null Circuit



Transient Response Test Circuit



Pins not shown are not connected.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = – 15 V, I_{set} = 15 μA, T_A = +25°C, unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset voltage ($R_S \le 10$ kΩ)	V_{IO}				mV
T_A = +25°C		–	2.0	6.0	
0°C ≤ T_A ≤ +70°C		–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	mV
Input Offset Current	I_{IO}				nA
T_A = +25°C		–	20	25	
T_A = +70°C		–	–	25	
T_A = 0°C		–	–	40	
Input Bias Current	I_{IB}				nA
T_A = +25°C		–	15	50	
T_A = +70°C		–	–	50	
T_A = 0°C		–	–	100	
Input Resistance	r_i	–	5.0	–	MΩ
Input Capacitance	C_i	–	2.0	–	pF
Input Common Mode Voltage Gain	V_{ICR}	±10	–	–	V
0°C ≤ T_A ≤ +70°C					
Large Signal Voltage Gain	A_{VOL}				V/V
$R_L \ge 10$ kΩ, V_O = ±10 V, T_A = +25°C		50 k	400 k	–	
$R_L \ge 10$ kΩ, V_O = ±10 V, 0°C ≤ T_A ≤ +70°C		25 k	–	–	
Output Voltage Range	V_{OR}				V
$R_L \ge 10$ kΩ, T_A = +25°C		±12	±13	–	
$R_L \ge 10$ kΩ, 0°C ≤ T_A ≤ +70°C		±12	–	–	
Output Resistance	r_o	–	1.0	–	kΩ
Output Short Circuit Current	I_{SC}	–	12	–	mA
Common Mode Rejection	CMR	70	90	–	dB
$R_S \le 10$ kΩ, 0°C ≤ T_A ≤ +70°C					
Supply Voltage Rejection Ratio	PSRR	–	25	200	μV/V
$R_S \le 10$ kΩ, 0°C ≤ T_A ≤ +70°C					
Supply Current	I_{CC}, I_{EE}				μA
T_A = +25°C		–	160	200	
0°C ≤ T_A ≤ +70°C		–	–	225	
Power Dissipation	P_D				mW
T_A = +25°C		–	4.8	6.0	
0°C ≤ T_A ≤ +70°C		–	–	6.75	
Transient Response (Unity Gain)					
V_{in} = 20 mV, $R_L \ge 10$ kΩ, C_L = 100 pF					
Rise Time	t_{TLH}	–	0.35	–	μs
Overshoot	os	–	10	–	%
Slew Rate ($R_L \ge 10$ kΩ)	SR	–	0.8	–	V/μs

Figure 1. Set Current versus Set Resistor

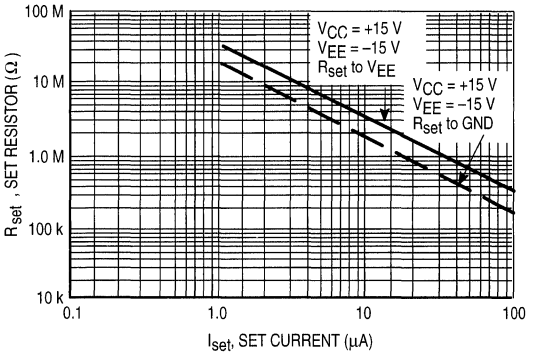


Figure 2. Positive Standby Supply Current versus Set Current

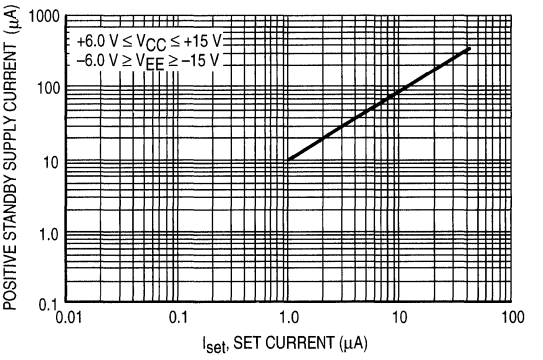


Figure 3. Open Loop versus Set Current

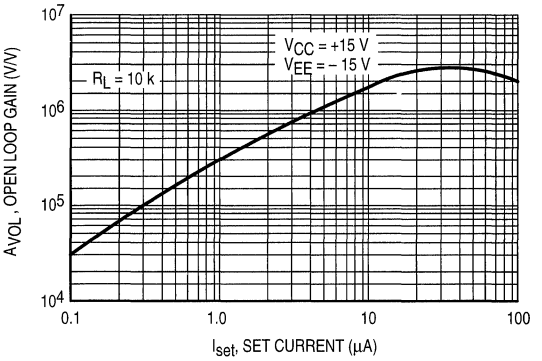


Figure 4. Input Bias Current versus Set Current

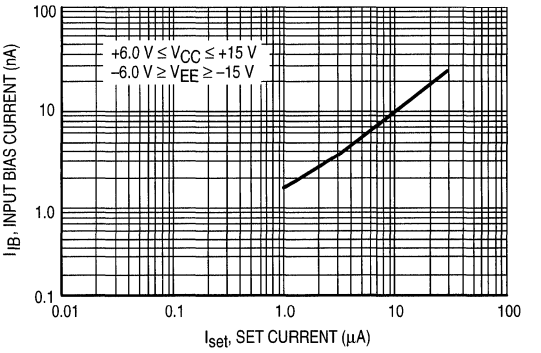


Figure 5. Slew Rate versus Set Current

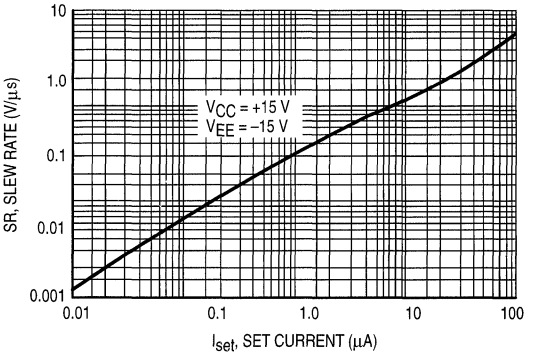
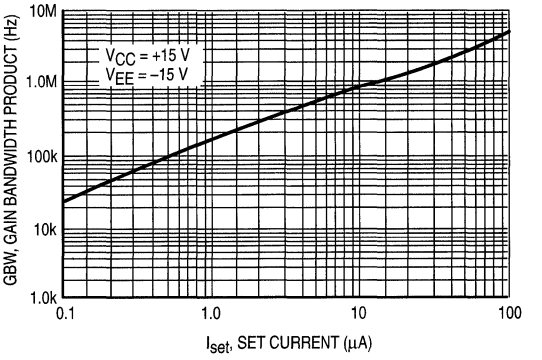


Figure 6. Gain Bandwidth Product versus Set Current



2

Figure 7. Output Voltage Swing versus Load Resistance

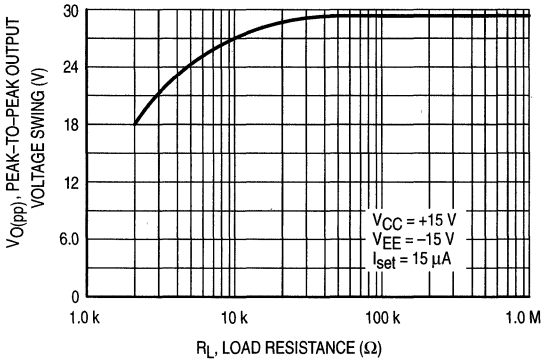
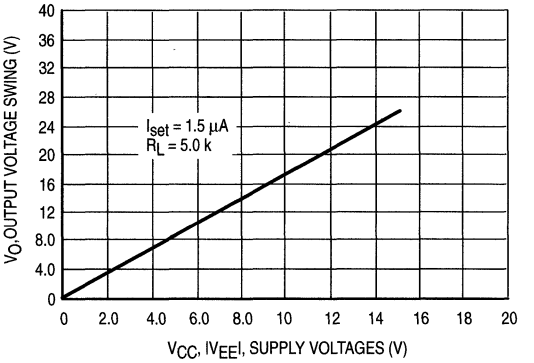


Figure 8. Output Voltage Swing versus Supply Voltage



MOTOROLA

MC4558AC
MC4558C

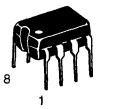
Dual Wide Bandwidth Operational Amplifiers

The MC4558AC, C combine all the outstanding features of the MC1458 and, in addition offer three times the unity gain bandwidth of the industry standard.

- 2.5 MHz Unity Gain Bandwidth Guaranteed (MC4558AC)
- 2.0 MHz Unity Gain Bandwidth Guaranteed (MC4558C)
- Internally Compensated
- Short Circuit Protection
- Gain and Phase Match between Amplifiers
- Low Power Consumption

DUAL WIDE BANDWIDTH OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

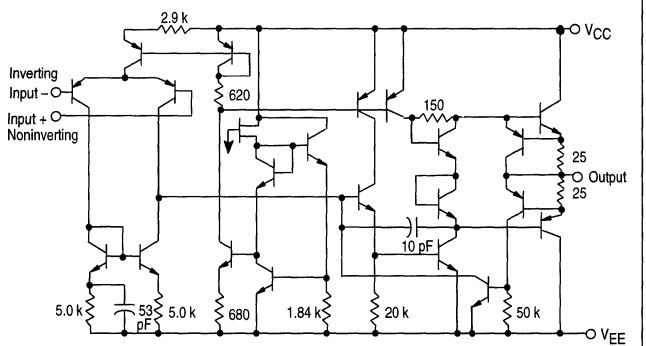
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

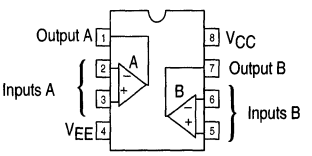
Rating	Symbol	MC4558AC	MC4558C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 –22	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±30		V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous		
Ambient Temperature Range	T_A	0 to +70		°C
Storage Temperature Range	T_{stg}	–55 to +125		°C
Junction Temperature	T_J	150		°C

NOTES: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply.

Representative Schematic Diagram
(1/2 of Circuit Shown)



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC4558CD	T_A = 0° to +70°C	SO–8
MC4558ACP1,CP1		Plastic DIP

2

FREQUENCY CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C)

Characteristic	Symbol	MC4558AC			MC4558C			Unit
		Min	Typ	Max	Min	Typ	Max	
Unity Gain Bandwidth	BW	2.5	2.8	–	2.0	2.8	–	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current (Note 1)	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection ($R_S \le 10$ kΩ)	CMR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \le 10$ kΩ)	PSRR	–	30	150	–	30	150	μV/V
Output Voltage Swing	V_O							V
($R_L \ge 10$ kΩ)		±12	±14	–	±12	±14	–	
($R_L \ge 2.0$ kΩ)		±10	±13	–	±10	±13	–	
Output Short Circuit Current	I_{SC}	10	20	40	10	20	40	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.0	–	2.3	5.6	mA
Power Consumption (Both Amplifiers)	P_C	–	70	150	–	70	170	mW
Transient Response (Unity Gain)								
(V_I = 20 mV, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Slew Rate	SR	1.5	1.6	–	1.0	1.6	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low}, unless otherwise noted. See Note 2.)

Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = T_{high})		–	7.0	200	–	–	–	
(T_A = T_{low})		–	85	500	–	–	–	
(T_A = 0° to +70°C)		–	–	–	–	–	300	
Input Bias Current	I_{IB}							nA
(T_A = T_{high})		–	30	500	–	–	–	
(T_A = T_{low})		–	300	1500	–	–	–	
(T_A = 0° to +70°C)		–	–	–	–	–	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	25	–	–	15	–	–	V/mV
Common Mode Rejection ($R_S \le 10$ kΩ)	CMR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \le 10$ kΩ)	PSRR	–	30	150	–	–	–	μV/V
Output Voltage Swing	V_O							V
($R_L \ge 10$ kΩ)		±12	±14	–	±12	±14	–	
($R_L \ge 2.0$ kΩ)		±10	±13	–	±10	±13	–	
Supply Currents (Both Amplifiers)	I_D							mA
(T_A = T_{high})		–	–	4.5	–	–	5.0	
(T_A = T_{low})		–	–	6.0	–	–	6.7	
Power Consumption (Both Amplifiers)	P_C							mW
(T_A = T_{high})		–	–	135	–	–	150	
(T_A = T_{low})		–	–	180	–	–	200	

NOTES: 1. I_{IB} is out of the amplifier due to PNP input transistors.
2. T_{high} = +70°C, T_{low} = 0°C.

Figure 1. Burst Noise versus Source Resistance

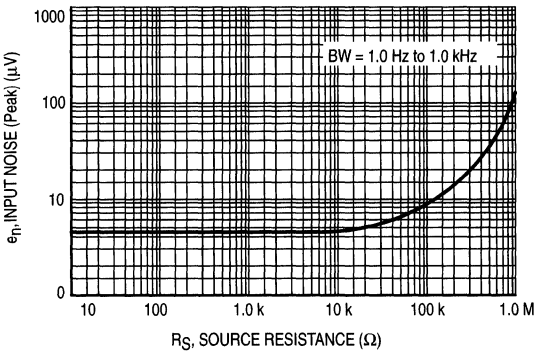


Figure 2. RMS Noise versus Source Resistance

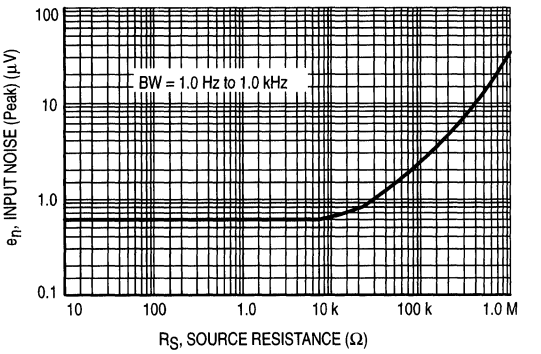


Figure 3. Output Noise versus Source Resistance

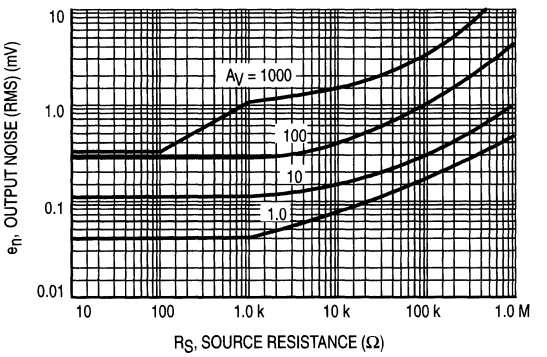


Figure 4. Spectral Noise Density

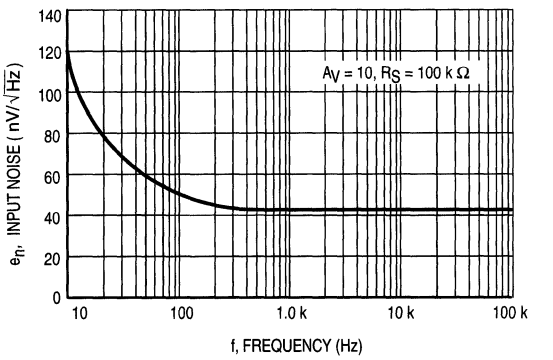
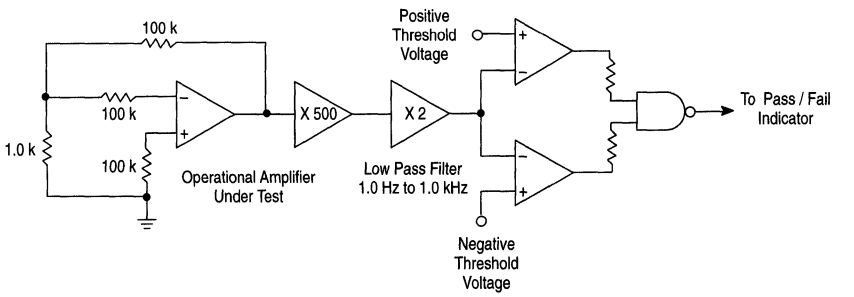


Figure 5. Burst Noise Test Circuit



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 sec and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed loop gain factor of the operational amplifier.

2

Figure 6. Open Loop Frequency Response

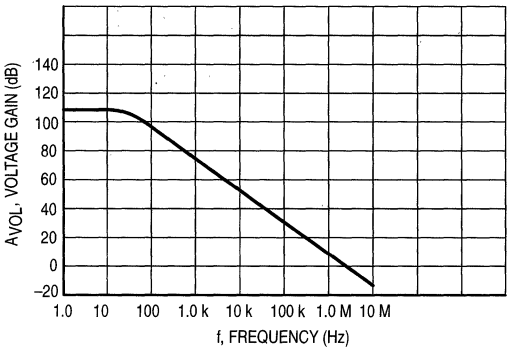


Figure 7. Phase Margin versus Frequency

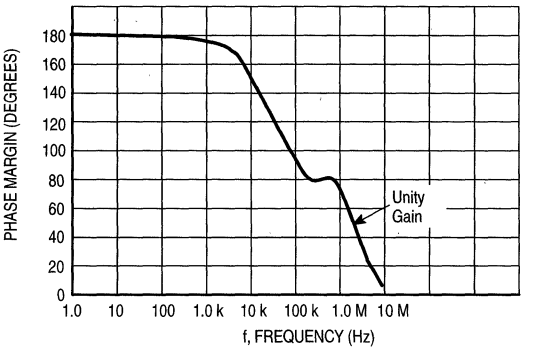


Figure 8. Positive Output Voltage Swing versus Load Resistance

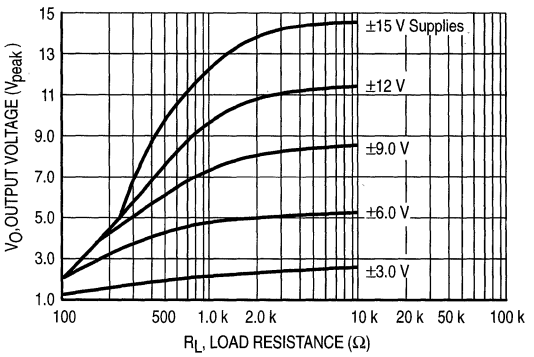


Figure 9. Negative Output Voltage Swing versus Load Resistance

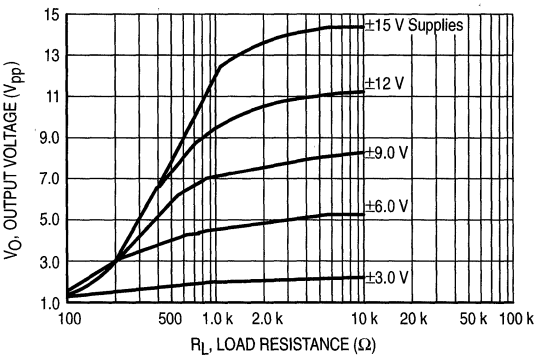


Figure 10. Power Bandwidth (Large Signal Swing versus Frequency)

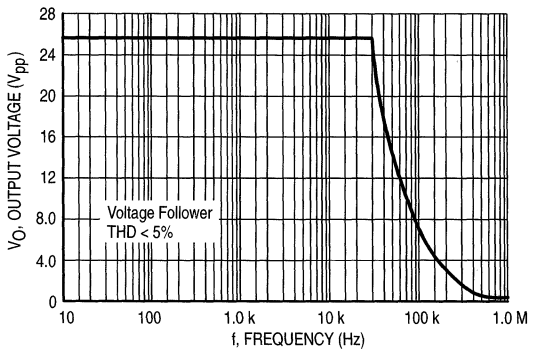
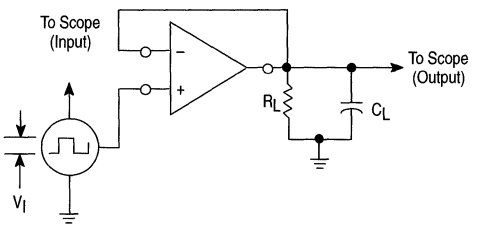


Figure 11. Transient Response Test Circuit



MOTOROLA

MCT4558C

Dual Wide Bandwidth Operational Amplifier

The MCT4558C combines all of the outstanding features of the MC1458 and, in addition, offers three times the unity gain bandwidth of the industry standard.

- 2.0 MHz Unity Gain Bandwidth Guaranteed
- Internally Compensated
- Short Circuit Protection
- Gain and Phase Match Between Amplifiers
- Low Power Consumption

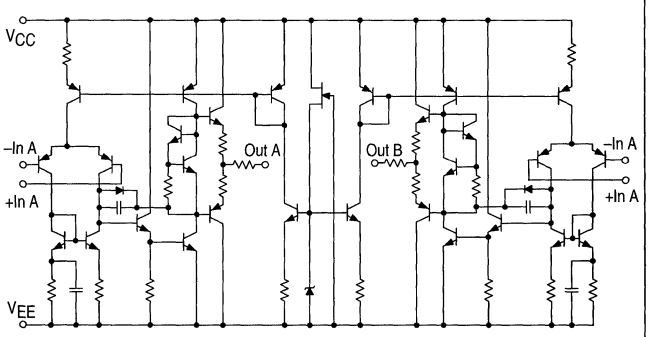
This MCT–prefixed device is intended to be a possible replacement for the similar device with the MC–prefix. Because the MCT device originates from different source material, there may be subtle differences in typical parameter values or characteristic curves. Due to the diversity of potential applications, Motorola can not assure identical performance in all circuits. Motorola recommends that the customer qualify the MCT–prefixed device in each potential application.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±30	V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Junction Temperature	T_J	150	°C

NOTES: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply.

Representative Schematic Diagram



This device contains 29 active transistors.

CAUTION: These devices do not have internal ESD protection circuitry and are rated as CLASS 1 devices per the ESD test method in Mil–Std–833D. They should be handled using standard ESD prevention methods to avoid damage to the device.

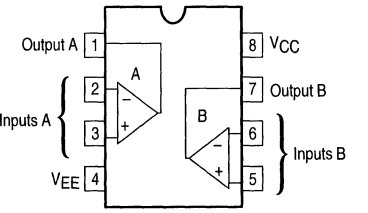
DUAL WIDE BANDWIDTH OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

P1 SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MCT4558CD	T_A = 0° to +70°C	SO–8
MCT4558CPI		Plastic DIP

2

FREQUENCY CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Unity Gain Bandwidth	BW	2.0	2.8	—	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}	—	2.0	6.0	mV
Input Offset Current	I_{IO}	—	20	200	nA
Input Bias Current (Note 1)	I_{IB}	—	80	500	nA
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	20	200	—	V/mV
Common Mode Rejection ($R_S \le 10$ kΩ)	CMR	70	90	—	dB
Supply Voltage Rejection Ratio ($R_S \le 10$ kΩ)	PSRR	—	30	150	μV/V
Output Voltage Swing ($R_L \ge 10$ kΩ) ($R_L \ge 2.0$ kΩ)	V_O	 ±12 ±10	 ±14 ±13	 — —	V
Output Short Circuit Current	I_{SC}	10	20	75	mA
Supply Currents (Both Amplifiers)	I_D	—	4.0	5.6	mA
Power Consumption (Both Amplifiers)	P_C	—	70	170	mW
Transient Response (Unity Gain) (V_I = 20 mV, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Rise Time (V_I = 20 mV, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Overshoot (V_I = 10 V, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Slew Rate	 t_{TLH} os SR	 — — 1.0	 0.3 15 1.8	 — — —	 μs % V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low}, [Note 2] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}	—	—	7.5	mV
Input Offset Current (T_A = 0° to +70°C)	I_{IO}	—	—	300	nA
Input Bias Current (T_A = 0° to +70°C)	I_{IB}	—	—	800	nA
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	15	—	—	V/mV
Output Voltage Swing ($R_L \ge 10$ kΩ) ($R_L \ge 2.0$ kΩ)	V_O	 ±12 ±10	 ±14 ±13	 — —	V
Supply Currents (Both Amplifiers) ($T_A = T_{high}$) ($T_A = T_{low}$)	I_D	 — —	 — —	 5.0 6.7	mA
Power Consumption (Both Amplifiers) ($T_A = T_{high}$) ($T_A = T_{low}$)	P_C	 — —	 — —	 150 200	mW

NOTES: 1. I_{IB} is out of the amplifier due to PNP input transistors.
2. T_{low} = 0°C T_{high} = +70°C

Figure 1. Power Bandwidth (Large Signal Swing versus Frequency)

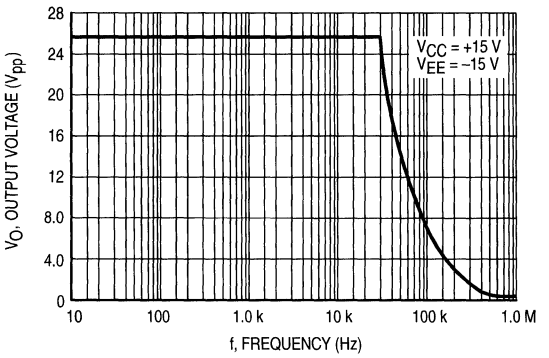


Figure 2. Maximum Output Voltage Swing versus Load Resistance

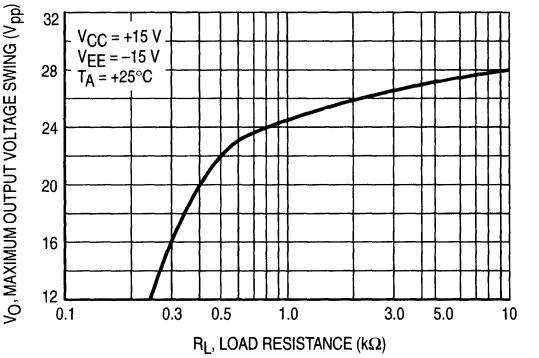


Figure 3. Equivalent Input Noise Voltage versus Frequency

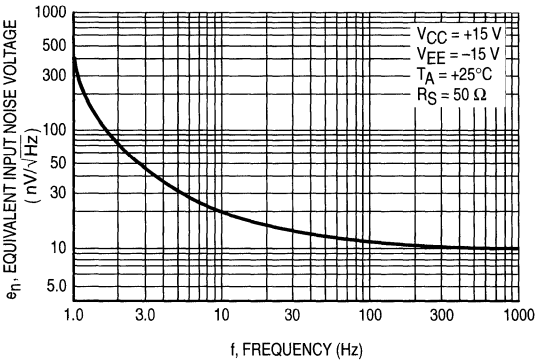


Figure 4. Input Bias Current versus Ambient Temperature

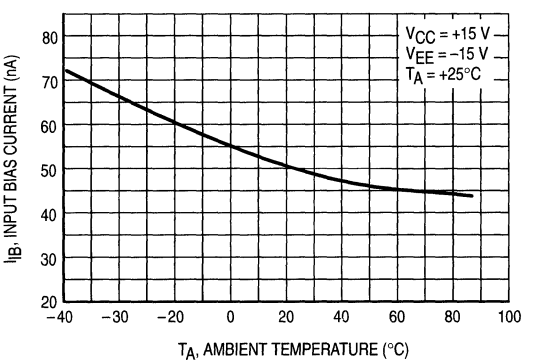


Figure 5. Voltage Gain and Phase versus Frequency

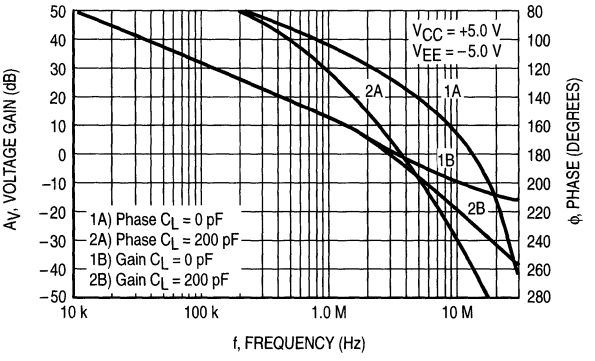
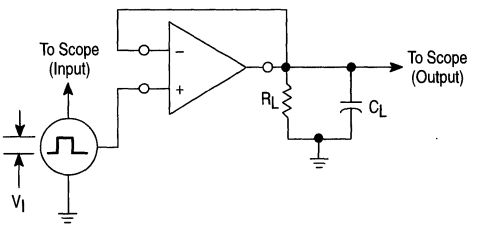


Figure 6. Transient Response Test Circuit



MC4741C

Differential Input Operational Amplifier

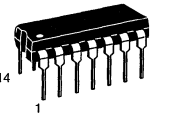
DIFFERENTIAL INPUT OPERATIONAL AMPLIFIER
(QUAD MC1741)

SEMICONDUCTOR TECHNICAL DATA

The MC4741C is a true quad MC1741. Integrated on a single monolithic chip are four independent, low power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance.

The MC4741C can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

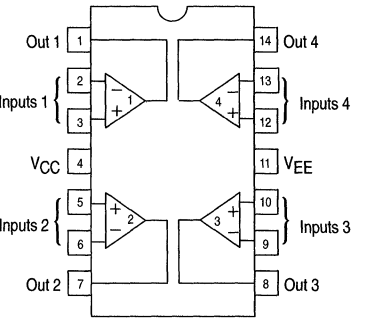
- Each Amplifier is Functionally Equivalent to the MC1741
- Class AB Output Stage Eliminates Crossover Distortion
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)



P SUFFIX
PLASTIC PACKAGE
CASE 646

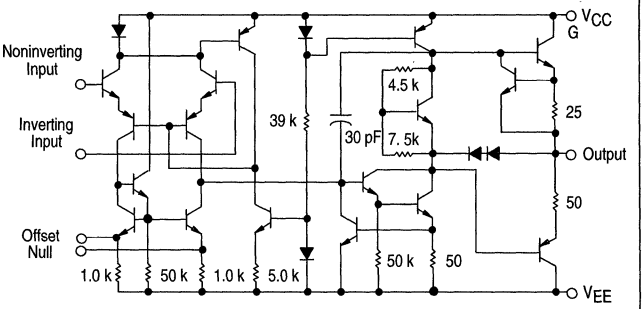
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

Representative Schematic Diagram
(1/4 of Circuit Shown)



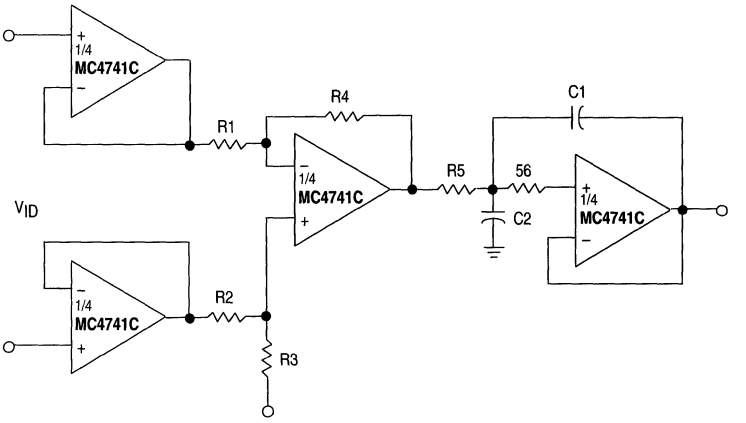
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC4741CD	T_A = 0° to +70°C	SO–14
MC4741CP		Plastic DIP

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 −18	Vdc
Input Differential Voltage	V_{ID}	±36	V
Input Common Mode Voltage	V_{ICM}	±18	V
Output Short Circuit Duration	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Junction Temperature	T_J	150	°C

High Impedance Instrumentation Buffer/Filter



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \geq 2.0$ k)	A_V	20	200	–	V/mV
Output Resistance	r_o	–	75	–	Ω
Common Mode Rejection ($R_S \leq 10$ k)	CMR	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	μV/V
Output Voltage Swing ($R_L \geq 10$ k) ($R_L \geq 2$ k)	V_O	 ±12 ±10	 ±14 ±13	 – –	V
Output Short Circuit Current	I_{SC}	–	20	–	mA
Supply Current – (All Amplifiers)	I_D	–	3.5	7.0	mA
Power Consumption (All Amplifiers)	P_C	–	105	210	mW
Transient Response (Unity Gain – Non–Inverting) (V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Rise Time (V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Overshoot (V_I = 10 V, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Slew Rate	 t_{TLH} os SR	 – – –	 0.3 15 0.5	 – – –	 μs % V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = * T_{high} to T_{low}, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	–	7.5	mV
Input Offset Current (T_A = 0° to + 70°C)	I_{IO}	–	–	300	nA
Input Bias Current (T_A = 0° to + 70°C)	I_{IB}	–	–	800	nA
Large Signal Voltage Gain ($R_L \geq 2$k, V_{OUT} = ±10 V)	A_V	15	–	–	V/mV
Output Voltage Swing ($R_L \geq 2$ k)	V_O	±10	±13	–	V

* T_{high} = 70°C T_{low} = −0°C

Figure 1. Power Bandwidth (Large Signal Swing versus Frequency)

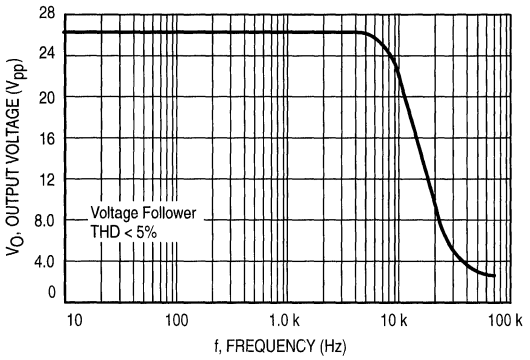


Figure 2. Open Loop Frequency Response

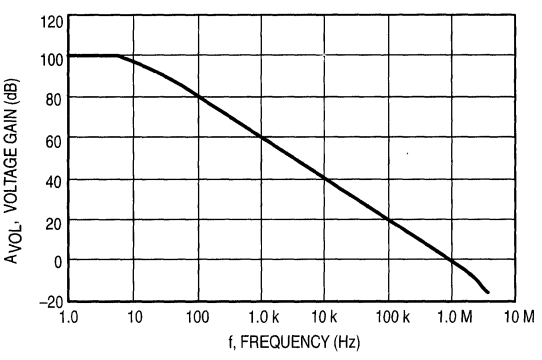


Figure 3. Positive Output Voltage Swing versus Load Resistance

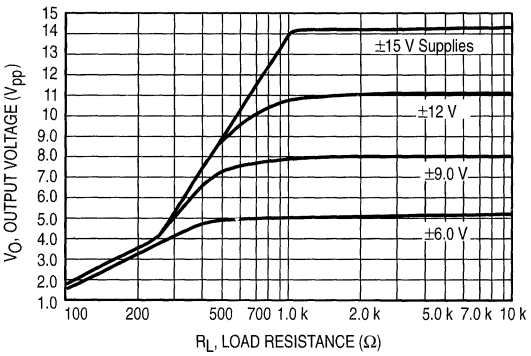


Figure 4. Negative Output Voltage Swing versus Load Resistance

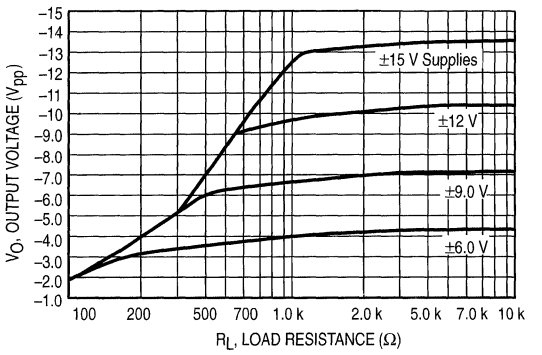


Figure 5. Output Voltage Swing versus Load Resistance (Single Supply Operation)

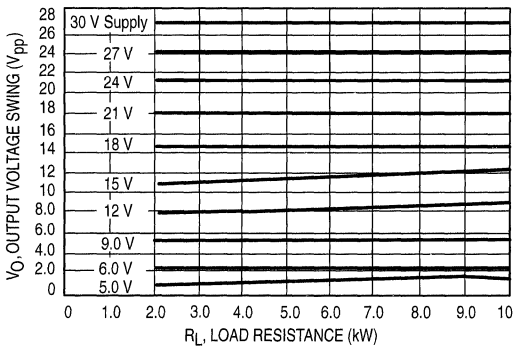
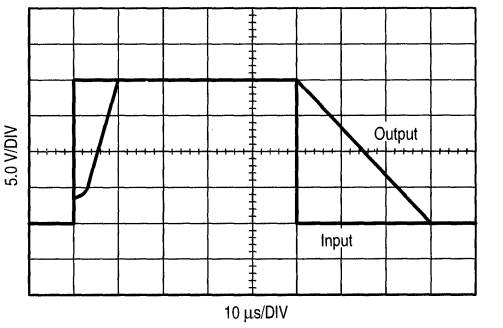


Figure 6. Noninverting Pulse Response



2

Figure 7. Bi–Quad Filter

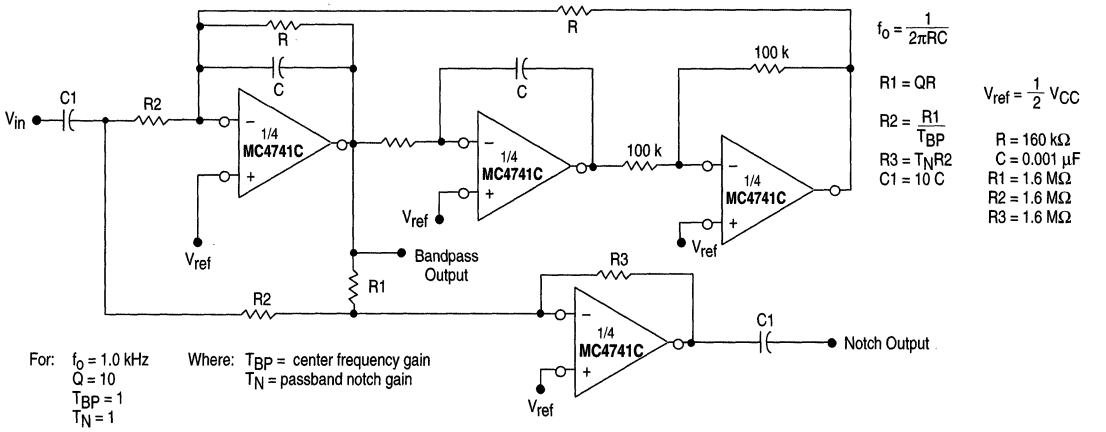


Figure 8. Open Loop Voltage Gain versus Supply Voltage

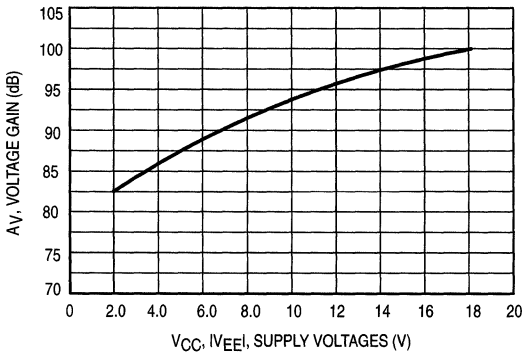


Figure 9. Transient Response Test Circuit

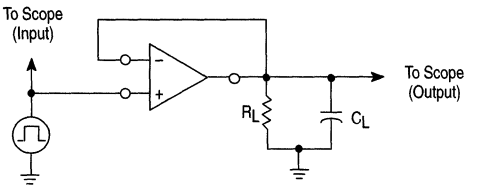
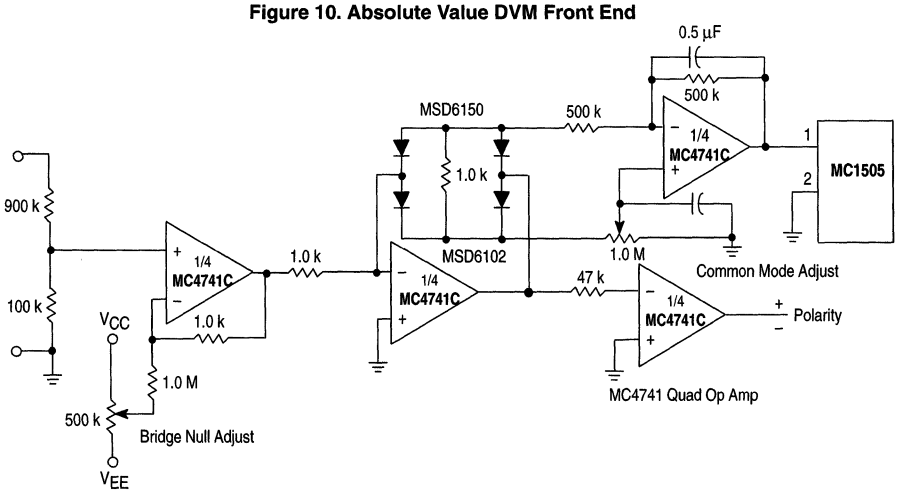


Figure 10. Absolute Value DVM Front End



MC33076

Dual High Output Current, Low Power, Low Noise Bipolar Operational Amplifier

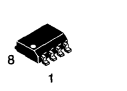
DUAL HIGH OUTPUT CURRENT OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

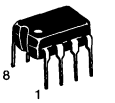
The MC33076 operational amplifier employs bipolar technology with innovative high performance concepts for audio and industrial applications. This device uses high frequency PNP input transistors to improve frequency response. In addition, the amplifier provides high output current drive capability while minimizing the drain current. The all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source and sink AC frequency performance.

The MC33076 is tested over the automotive temperature range and is available in an 8–pin SOIC package (D suffix) and in both the standard 8 pin DIP and 16–pin DIP packages for high power applications.

- 100 Ω Output Drive Capability
- Large Output Voltage Swing
- Low Total Harmonic Distortion
- High Gain Bandwidth: 7.4 MHz
- High Slew Rate: 2.6 V/μs
- Dual Supply Operation: ±2.0 V to ±18 V
- High Output Current: ISC = 250 mA typ
- Similar Performance to MC33178

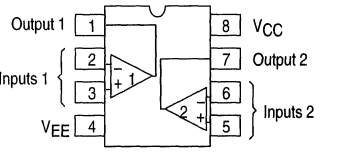


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

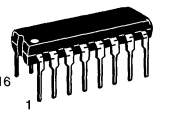


P1 SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS

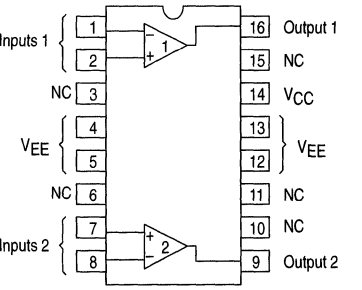


(8 Pin Pkg, Top View)



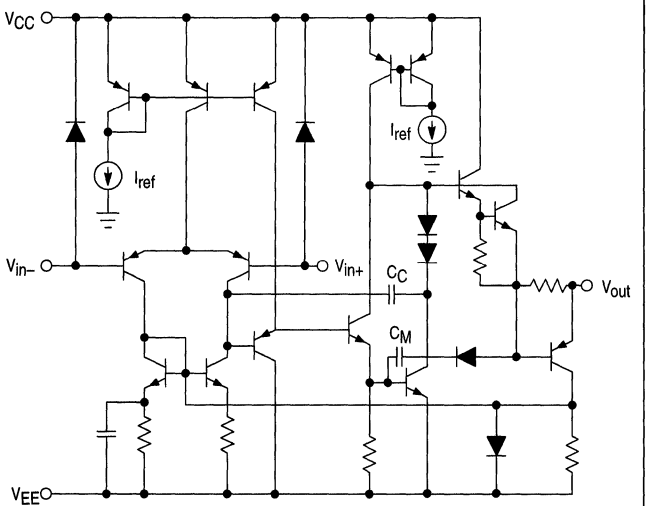
P2 SUFFIX
PLASTIC PACKAGE
CASE 648C
DIP (12+2+2)

PIN CONNECTIONS



(16 Pin Pkg, Top View)

Equivalent Circuit Schematic
(Each Amplifier)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33076D	$T_A = -40°$ to $+85°C$	SO–8
MC33076P1		Plastic DIP
MC33076P2		Power Plastic

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Note 2)	V_{CC} to V_{EE}	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	5.0	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see power dissipation performance characteristic, Figure 1).
See applications section for further information.

DC ELECTRICAL CHARACTERICISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V) (V_S = ±2.5 V to ±15 V) T_A = +25°C T_A = –40° to +85°C	2	$\lvert V_{IO}\rvert$	 — —	 0.5 0.5	 4.0 5.0	mV
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω, V_{CM} = 0 V) T_A = –40° to +85°C		$\Delta V_{IO}/\Delta T$	 —	 2.0	 —	µV/°C
Input Bias Current (V_{CM} = 0 V) T_A = +25°C T_A = –40° to +85°C	3, 4	I_{IB}	 — —	 100 —	 500 600	nA
Input Offset Current (V_{CM} = 0 V) T_A = +25°C T_A = –40° to +85°C		$\lvert I_{IO}\rvert$	 — —	 5.0 —	 70 100	nA
Common Mode Input Voltage Range	5	V_{ICR}	–13	–14 +14	 13	V
Large Signal Voltage Gain (V_O = –10 V to +10 V) (T_A = +25°C) R_L = 100 Ω R_L = 600 Ω (T_A = –40° to +85°C) R_L = 600 Ω	6	A_{VOL}	 25 50 25	 — 200 —	 — — —	kV/V
Output Voltage Swing (V_{ID} = ±1.0 V) (V_{CC} = +15 V, V_{EE} = –15 V) R_L = 100 Ω R_L = 100 Ω R_L = 600 Ω R_L = 600 Ω (V_{CC} = +2.5 V, V_{EE} = –2.5 V) R_L = 100 Ω R_L = 100 Ω	7, 8, 9	 V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-}	 10 — 13 — 1.2 —	 +11.7 –11.7 +13.8 –13.8 +1.66 –1.74	 — –10 — –13 — –1.2	V
Common Mode Rejection (V_{in} = ±13 V)	10	CMR	80	116	—	dB
Power Supply Rejection (V_{CC}/V_{EE} = +15 V/–15 V, +5.0 V/–15 V, +15 V/–5.0 V)	11	PSR	 80	 120	 —	dB

DC ELECTRICAL CHARACTERICISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Output Short Circuit Current (V_{ID} = ±1.0 V Output to Gnd)	12, 13	I_{SC}				mA
(V_{CC} = +15 V, V_{EE} = −15 V)						
Source			190	+250	—	
Sink			—	−280	−215	
(V_{CC} = +2.5 V, V_{EE} = −2.5 V)						
Source			63	+94	—	
Sink			—	−80	−46	
Power Supply Current per Amplifier (V_O = 0 V)	14	I_D				mA
(V_S = ±2.5 V to ±15 V)						
T_A = +25°C			—	2.2	2.8	
T_A = −40° to +85°C			—	—	3.3	

AC ELECTRICAL CHARACTERICISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 100 Ω, C_L = 100 pF, A_V = +1)	15	SR	1.2	2.6	—	V/μs
Gain Bandwidth Product (f = 20 kHz)	16	GBW	4.0	7.4	—	MHz
Unity Gain Frequency (Open Loop) (R_L = 600 Ω, C_L = 0 pF)	—	f_U	—	3.5	—	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	19, 20	A_m	—	15	—	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	19, 20	$\varnothing_m$	—	52	—	Deg
Channel Separation (f = 100 Hz to 20 kHz)	21	CS	—	−120	—	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 600 Ω, THD ≤ 1%)	—	BW_p	—	32	—	kHz
Total Harmonic Distortion (R_L = 600 Ω, V_O = 2.0 V_{pp}, A_V = +1)	22	THD				%
f = 1.0 kHz			—	0.0027	—	
f = 10 kHz			—	0.011	—	
f = 20 kHz			—	0.022	—	
Open Loop Output Impedance (V_O = 0 V, f = 2.5 MHz, A_V = 10)	23	$\|Z_O\|$	—	75	—	Ω
Differential Input Resistance (V_{CM} = 0 V)	—	R_{in}	—	200	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)	—	C_{in}	—	10	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω)	24	e_n				nV/$\sqrt{Hz}$
f = 10 Hz			—	7.5		
f = 1.0 kHz			—	5.0	—	
Equivalent Input Noise Current	—	i_n				pA/$\sqrt{Hz}$
f = 10 Hz			—	0.33	—	
f = 1.0 kHz			—	0.15	—	

2

Figure 1. Maximum Power Dissipation versus Temperature

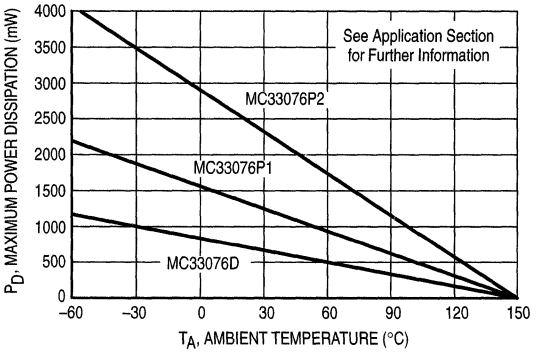


Figure 2. Distribution of Input Offset Voltage

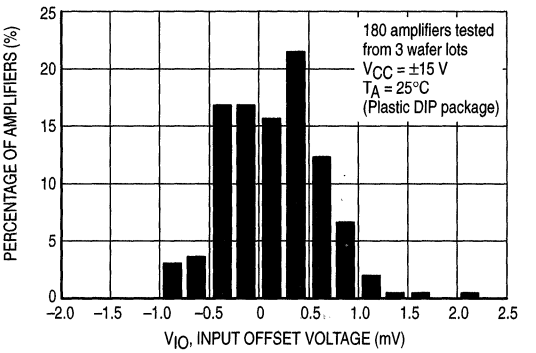


Figure 3. Input Bias Current versus Common Mode Voltage

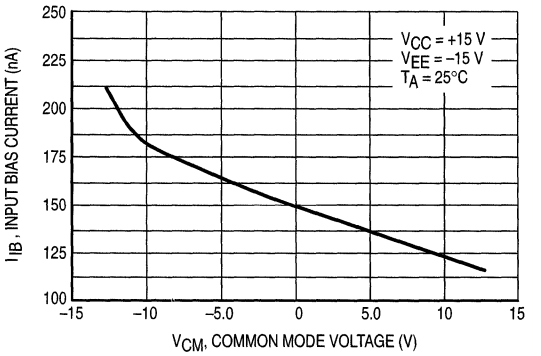


Figure 4. Input Bias Current versus Temperature

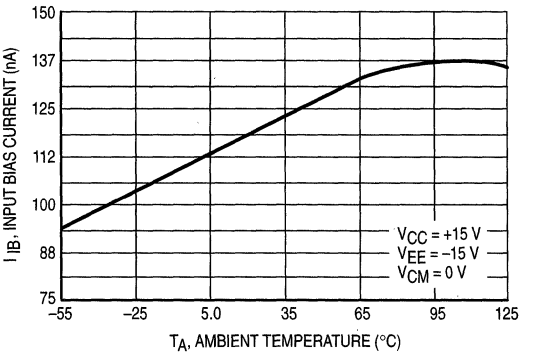


Figure 5. Input Common Mode Voltage Range versus Temperature

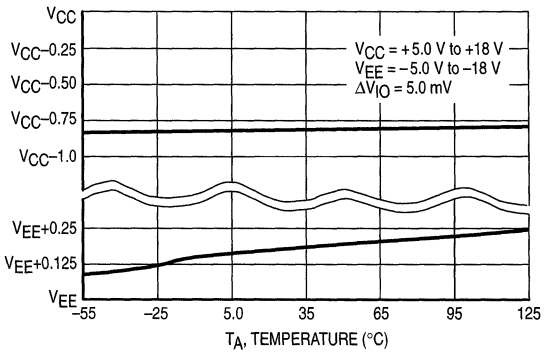


Figure 6. Open Loop Voltage Gain versus Temperature

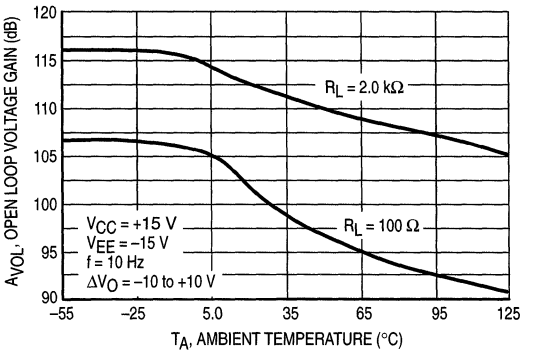


Figure 7. Output Voltage Swing versus Supply Voltage

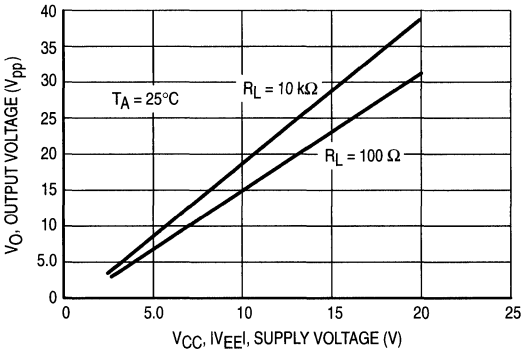


Figure 8. Maximum Peak–to–Peak Output Voltage Swing versus Load Resistance

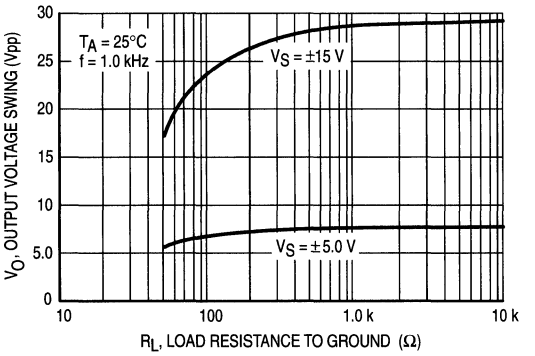


Figure 9. Output Voltage versus Frequency

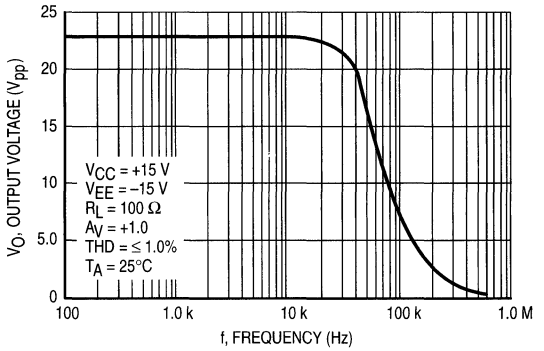


Figure 10. Common Mode Rejection versus Frequency Over Temperature

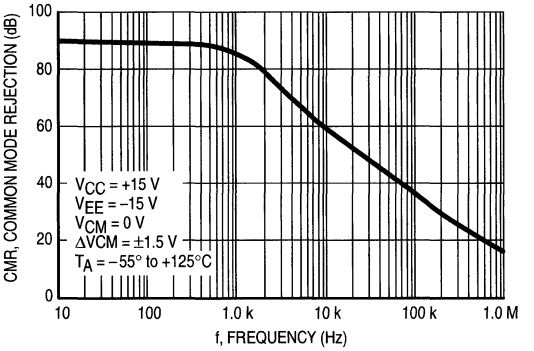


Figure 11. Power Supply Rejection versus Frequency Over Temperature

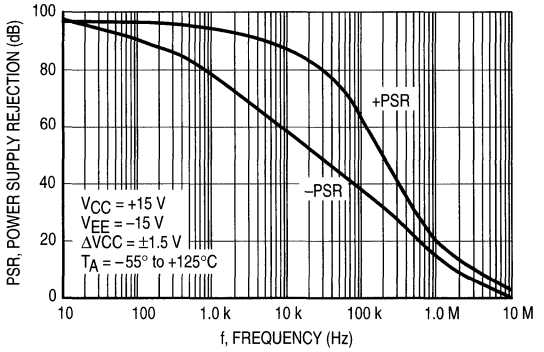
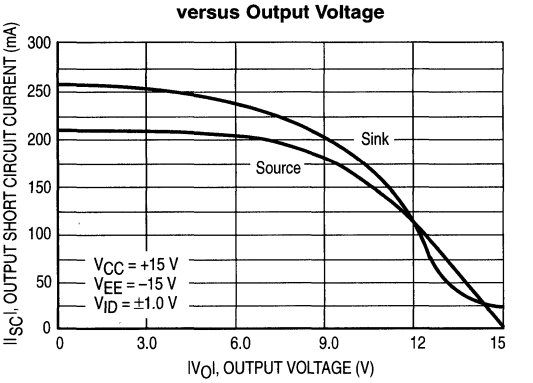


Figure 12. Output Short Circuit Current versus Output Voltage



2

Figure 13. Output Short Circuit Current versus Temperature

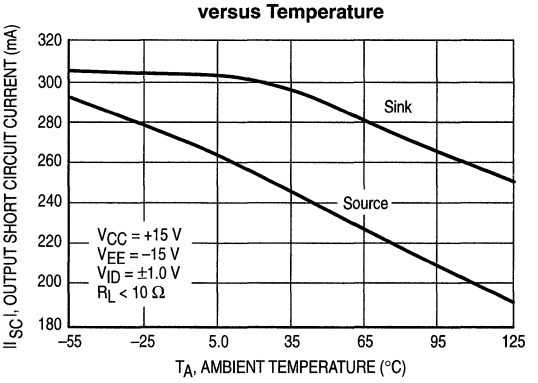


Figure 14. Supply Current versus Supply Voltage with No Load

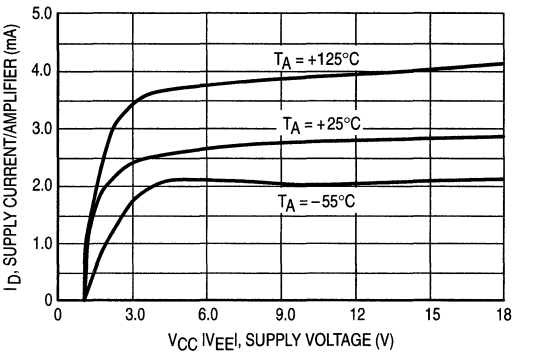


Figure 15. Slew Rate versus Temperature

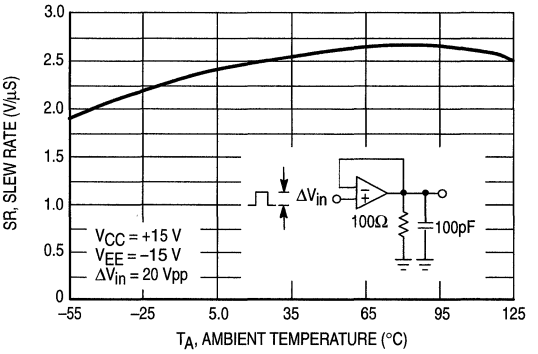


Figure 16. Gain Bandwidth Product versus Temperature

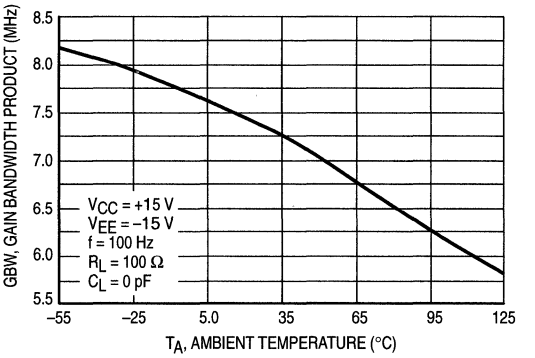


Figure 17. Voltage Gain and Phase versus Frequency

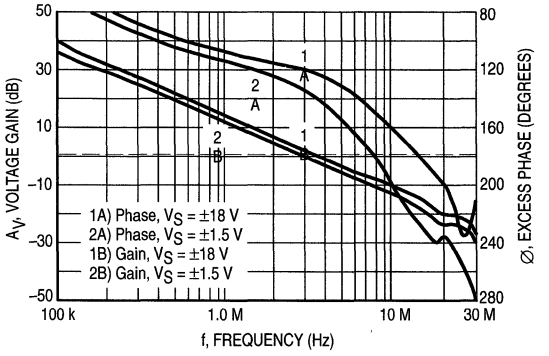


Figure 18. Voltage Gain and Phase versus Frequency

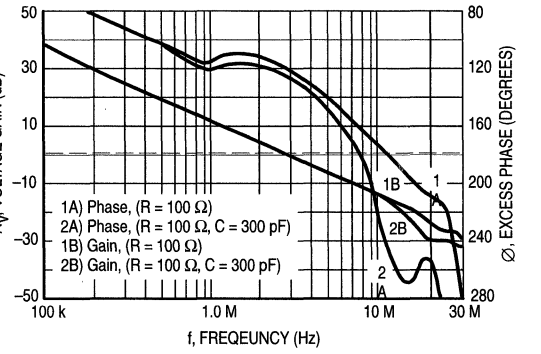


Figure 19. Phase Margin and Gain Margin versus Differential Source Resistance

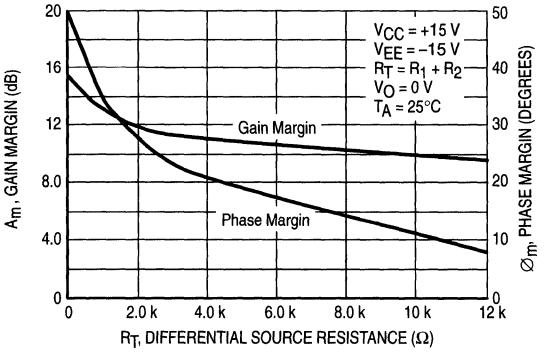


Figure 20. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

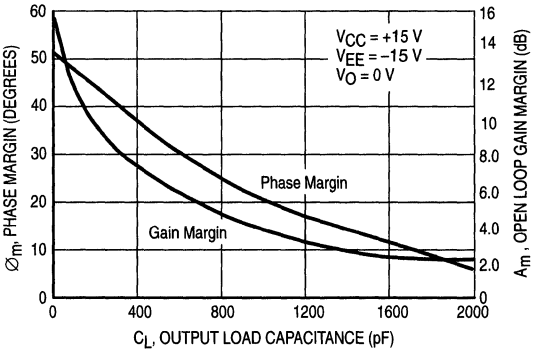


Figure 21. Channel Separation versus Frequency

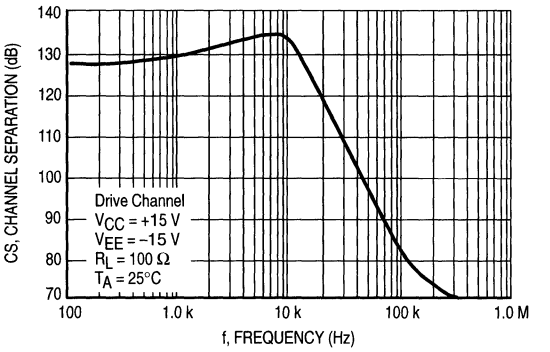


Figure 22. Total Harmonic Distortion versus Frequency

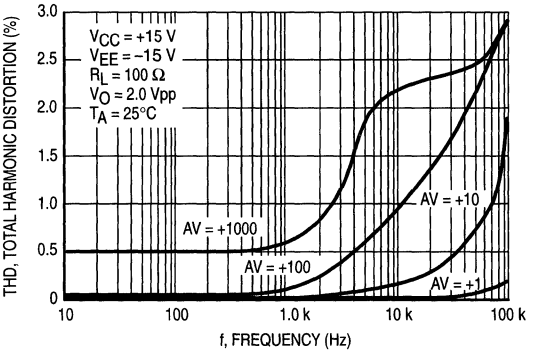


Figure 23. Output Impedance versus Frequency

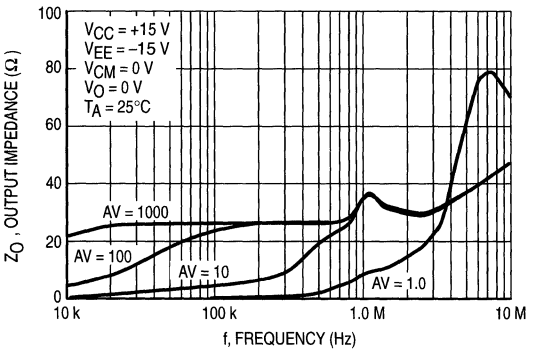


Figure 24. Input Referred Noise Voltage versus Frequency

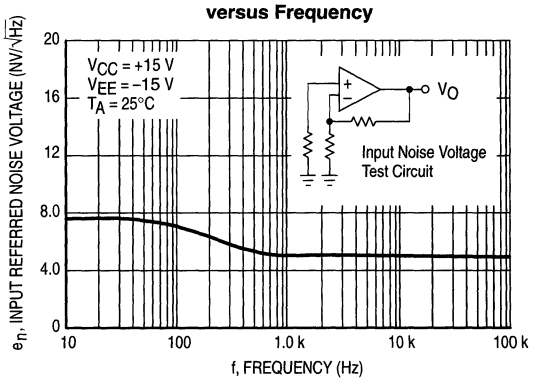


Figure 25. Percent Overshoot versus Load Capacitance

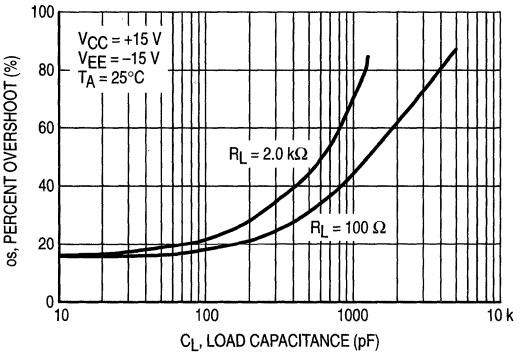
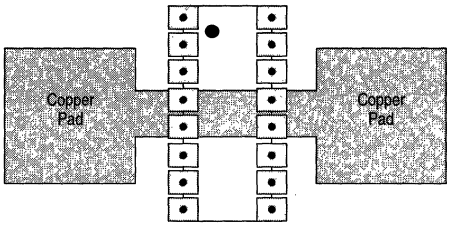


Figure 26. PC Board Heatsink Example



APPLICATIONS INFORMATION

The MC33076 dual operational amplifier is available in the standard 8–pin plastic dual–in–line (DIP) and surface mount packages, and also in a 16–pin batwing power package. To enhance the power dissipation capability of the power package, Pins 4, 5, 12, and 13 are tied together on the leadframe, giving it an ambient thermal resistance of 52°C/W typically, in still air. The junction–to–ambient thermal resistance ($R_{\theta JA}$) can be decreased further by using a copper padb on the printed circuit board (as shown in Figure 26) to draw the heat away from the package. *Care must be taken not to exceed the maximum junction temperature or damage to the device may occur.*

MOTOROLA

MC33077

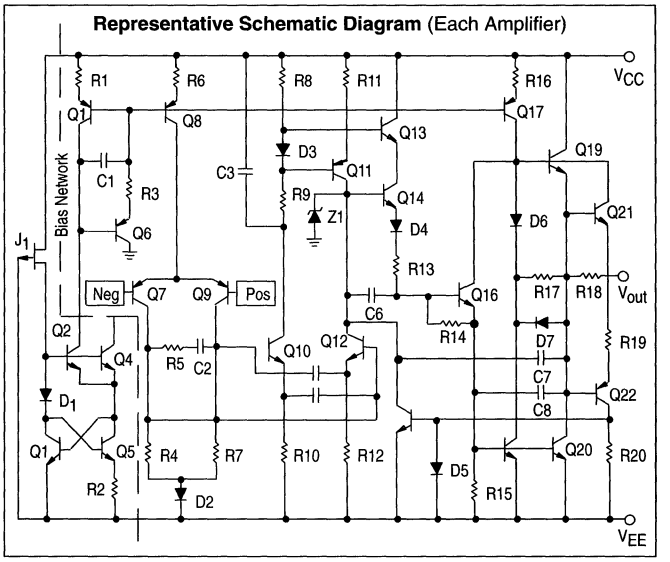
Dual, Low Noise Operational Amplifier

The MC33077 is a precision high quality, high frequency, low noise monolithic dual operational amplifier employing innovative bipolar design techniques. Precision matching coupled with a unique analog resistor trim technique is used to obtain low input offset voltages. Dual–doublet frequency compensation techniques are used to enhance the gain bandwidth product of the amplifier. In addition, the MC33077 offers low input noise voltage, low temperature coefficient of input offset voltage, high slew rate, high AC and DC open loop voltage gain and low supply current drain. The all NPN transistor output stage exhibits no deadband cross–over distortion, large output voltage swing, excellent phase and gain margins, low open loop output impedance and symmetrical source and sink AC frequency performance.

The MC33077 is tested over the automotive temperature range and is available in plastic DIP and SO–8 packages (P and D suffixes).

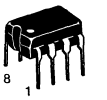
- Low Voltage Noise: 4.4 nV/$\sqrt{Hz}$ @ 1.0 kHz
- Low Input Offset Voltage: 0.2 mV
- Low TC of Input Offset Voltage: 2.0 μV/°C
- High Gain Bandwidth Product: 37 MHz @ 100 kHz
- High AC Voltage Gain: 370 @ 100 kHz
  1850 @ 20 kHz
- Unity Gain Stable: with Capacitance Loads to 500 pF
- High Slew Rate: 11 V/μs
- Low Total Harmonic Distortion: 0.007%
- Large Output Voltage Swing: +14 V to −14.7 V
- High DC Open Loop Voltage Gain: 400 k (112 dB)
- High Common Mode Rejection: 107 dB
- Low Power Supply Drain Current: 3.5 mA
- Dual Supply Operation: ±2.5 V to ±18 V

Representative Schematic Diagram (Each Amplifier)



DUAL, LOW NOISE OPERATIONAL AMPLIFIER

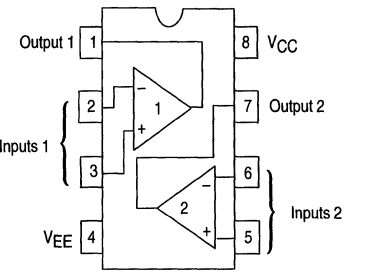
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33077D	$T_A = -40°$ to $+85°C$	SO–8
MC33077P		Plastic DIP

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE} (See Applications Information).
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (See power dissipation performance characteristic, Figure 1).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	$\lvert V_{IO}\rvert$	 — —	 0.13 —	 1.0 1.5	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = –40° to +85°C	$\Delta V_{IO}/\Delta T$	—	2.0	—	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	I_{IB}	 — —	 280 —	 1000 1200	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	I_{IO}	 — —	 15 —	 180 240	nA
Common Mode Input Voltage Range (ΔV_{IO} ,= 5.0 mV, V_O = 0 V)	V_{ICR}	±13.5	±14	—	V
Large Signal Voltage Gain (V_O = ±1.0 V, R_L = 2.0 kΩ) T_A = +25°C T_A = –40° to +85°C	A_{VOL}	 150 k 125 k	 400 k —	 — —	V/V
Output Voltage Swing (V_{ID} = ±1.0 V) R_L = 2.0 kΩ R_L = 2.0 kΩ R_L = 10 kΩ R_L = 10 kΩ	 V_{O+} V_{O-} V_{O+} V_{O-}	 +13.0 — +13.4 —	 +13.6 –14.1 +14.0 –14.7	 — –13.5 — –14.3	V
Common Mode Rejection (V_{in} = ±13 V)	CMR	85	107	—	dB
Power Supply Rejection (Note 3) V_{CC}/V_{EE} = +15 V/ –15 V to +5.0 V/ –5.0 V	PSR	80	90	—	dB
Output Short Circuit Current (V_{ID} = ±1.0 V, Output to Ground) Source Sink	I_{SC}	 +10 –20	 +26 –33	 +60 +60	mA
Power Supply Current (V_O = 0 V, All Amplifiers) T_A = +25°C T_A = –40° to +85°C	I_D	 — —	 3.5 —	 4.5 4.8	mA

NOTE: 3. Measured with V_{CC} and V_{EE} simultaneously varied.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0)	SR	8.0	11	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	25	37	—	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V) f = 100 kHz f = 20 kHz	A_{VO}	 — —	 370 1850	 — —	V/V
Unity Gain Frequency (Open Loop)	f_U	—	7.5	—	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 10 pF)	A_m	—	10	—	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 10 pF)	$\varnothing_m$	—	55	—	Degrees
Channel Separation (f = 20 Hz to 20 kHz, R_L = 2.0 kΩ, V_O = 10 V_{pp})	CS	—	−120	—	dB
Power Bandwidth (V_O = 27_{p-p}, R_L = 2.0 kΩ, THD ≤ 1%)	BW_p	—	200	—	kHz
Distortion (R_L = 2.0 kΩ) A_V = +1.0, f = 20 Hz to 20 kHz V_O = 3.0 V_{rms} A_V = 2000, f = 20 kHz V_O = 2.0 V_{pp} V_O = 10 V_{pp} A_V = 4000, f = 100 kHz V_O = 2.0 V_{pp} V_O = 10 V_{pp}	THD	 — — — — —	 0.007 0.215 0.242 0.3.19 0.316	 — — — — —	%
Open Loop Output Impedance (V_O = 0 V, f = f_U)	$\|Z_O\|$	—	36	—	Ω
Differential Input Resistance (V_{CM} = 0 V)	R_{in}	—	270	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)	C_{in}	—	15	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω) f = 10 Hz f = 1.0 kHz	e_n	 — —	 6.7 4.4	 — —	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz) f = 10 Hz f = 1.0 kHz	i_n	 — —	 1.3 0.6	 — —	pA/√Hz

Figure 1. Maximum Power Dissipation versus Temperature

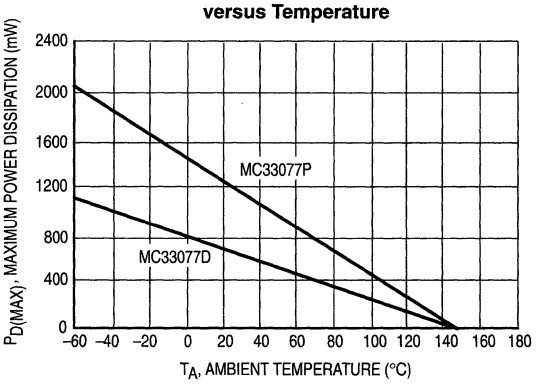
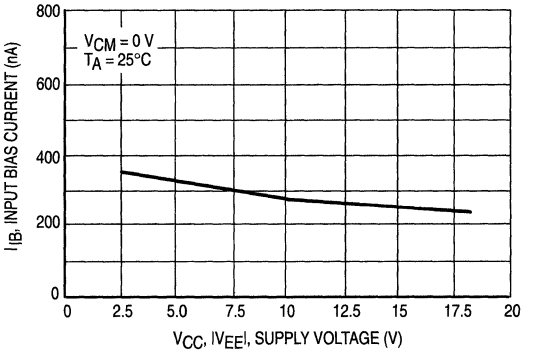


Figure 2. Input Bias Current versus Supply Voltage



2

Figure 3. Input Bias Current versus Temperature

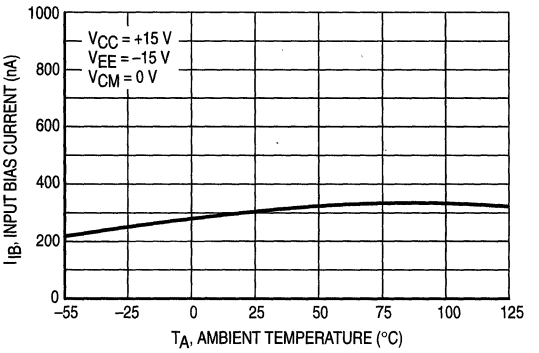


Figure 4. Input Offset Voltage versus Temperature

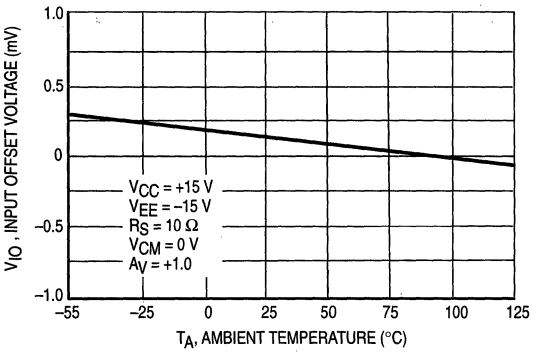


Figure 5. Input Bias Current versus Common Mode Voltage

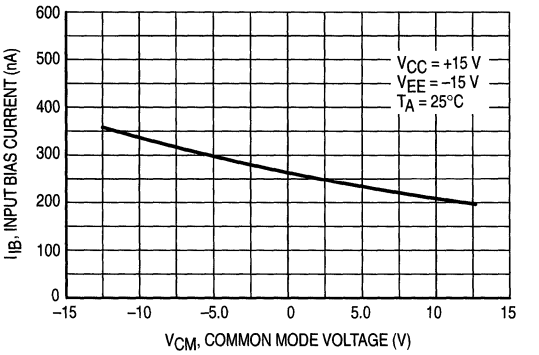


Figure 6. Input Common Mode Voltage Range versus Temperature

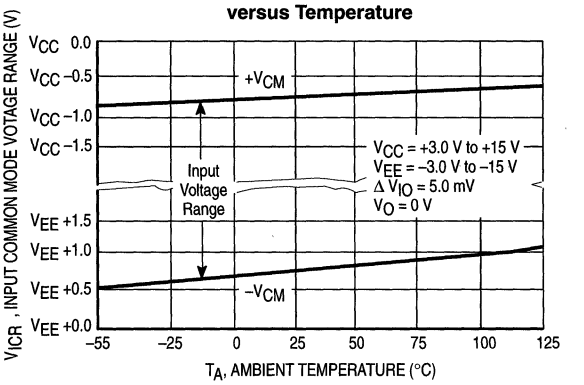


Figure 7. Output Saturation Voltage versus Load Resistance to Ground

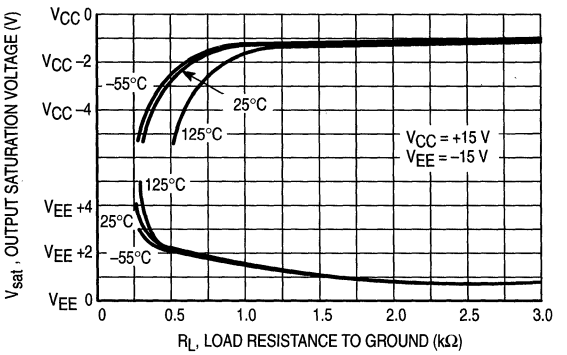


Figure 8. Output Short Circuit Current versus Temperature

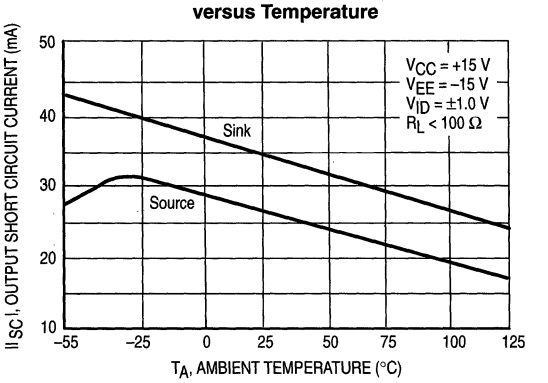


Figure 9. Supply Current versus Temperature

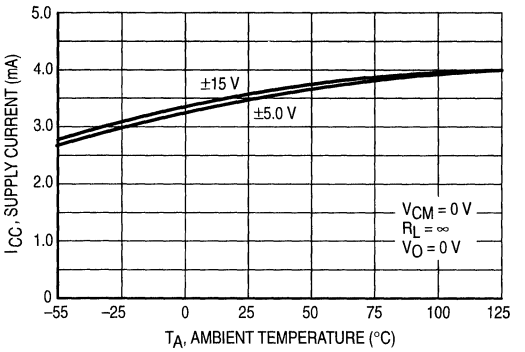


Figure 10. Common Mode Rejection versus Frequency

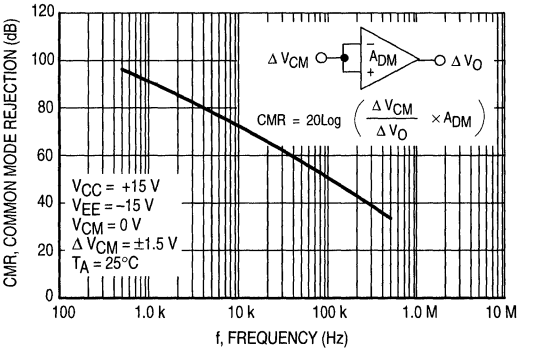


Figure 11. Power Supply Rejection versus Frequency

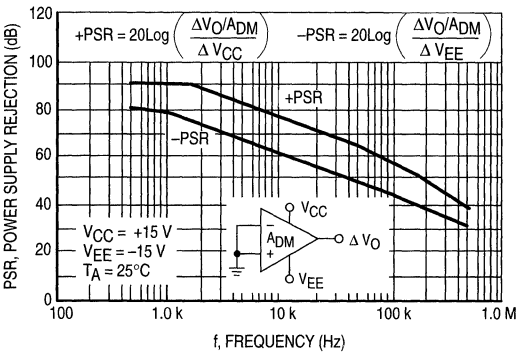


Figure 12. Gain Bandwidth Product versus Supply Voltage

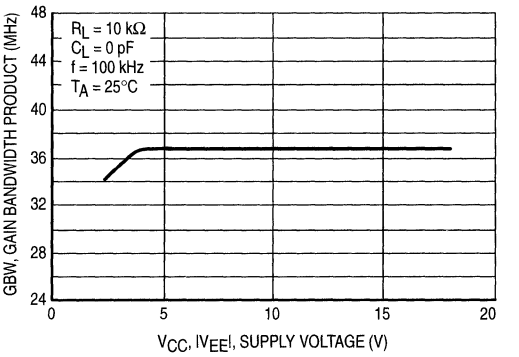


Figure 13. Gain Bandwidth Product versus Temperature

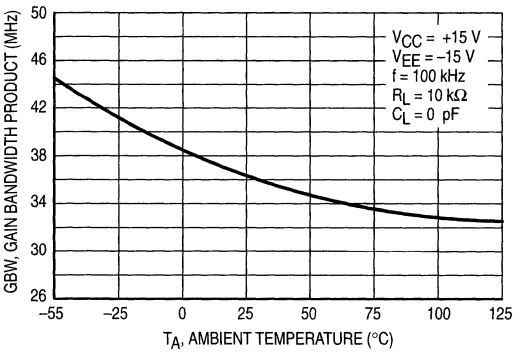
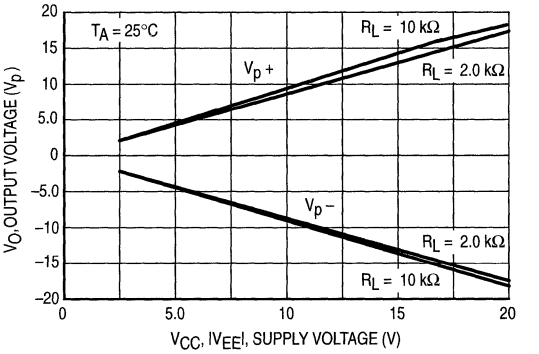


Figure 14. Maximum Output Voltage versus Supply Voltage



2

Figure 15. Output Voltage versus Frequency

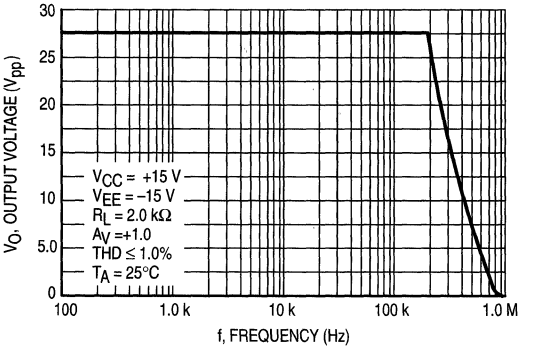


Figure 16. Open Loop Voltage Gain versus Supply Voltage

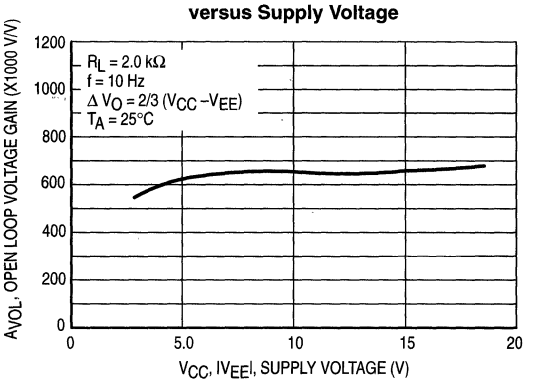


Figure 17. Open Loop Voltage Gain versus Temperature

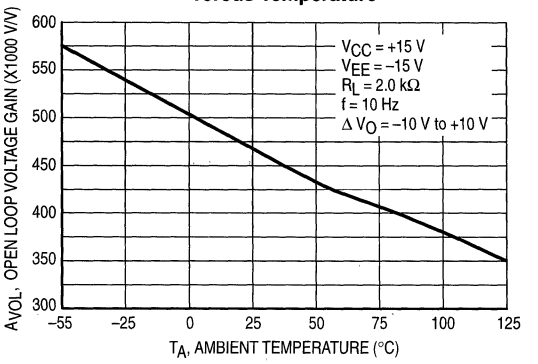


Figure 18. Output Impedance versus Frequency

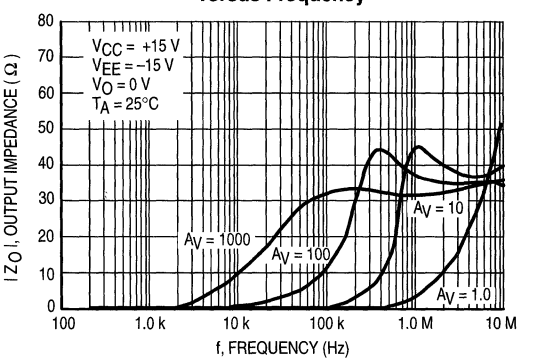


Figure 19. Channel Separation versus Frequency

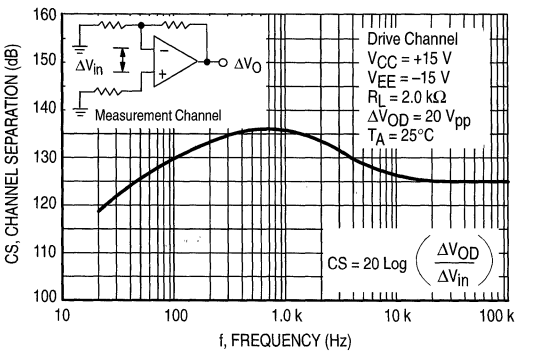


Figure 20. Total Harmonic Distortion versus Frequency

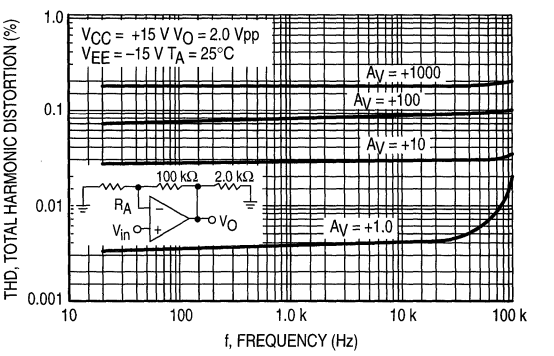


Figure 21. Total Harmonic Distortion versus Frequency

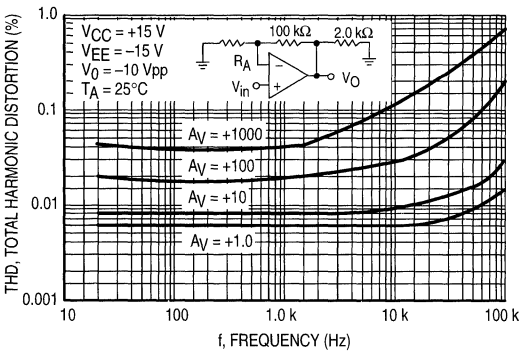


Figure 22. Total Harmonic Distortion versus Output Voltage

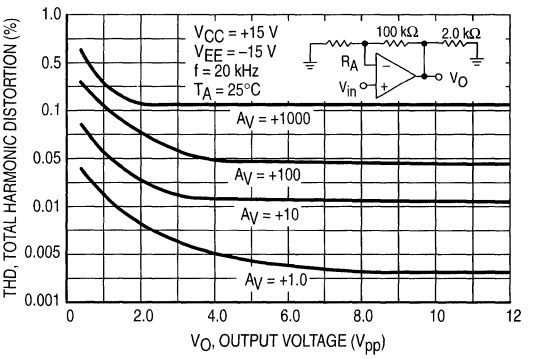


Figure 23. Slew Rate versus Supply Voltage

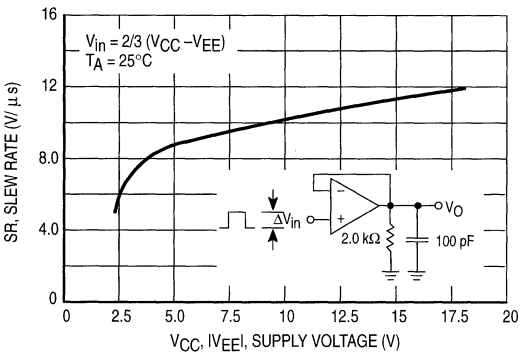


Figure 24. Slew Rate versus Temperature

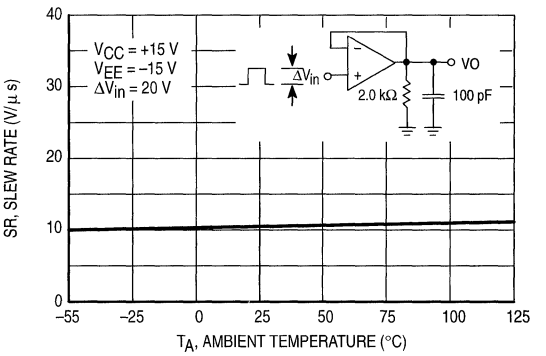


Figure 25. Voltage Gain and Phase versus Frequency

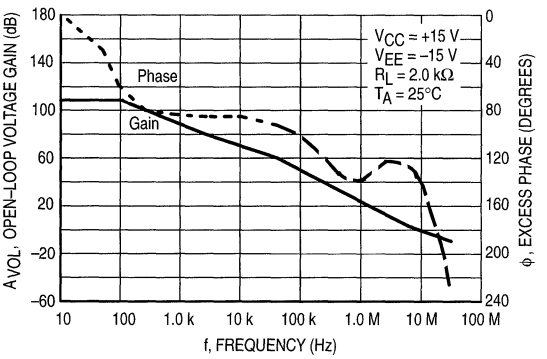
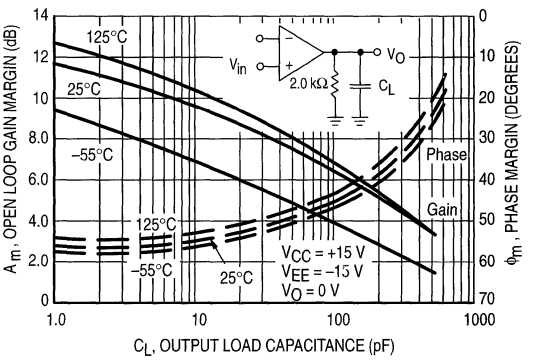


Figure 26. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance



2

Figure 27. Phase Margin versus Output Voltage

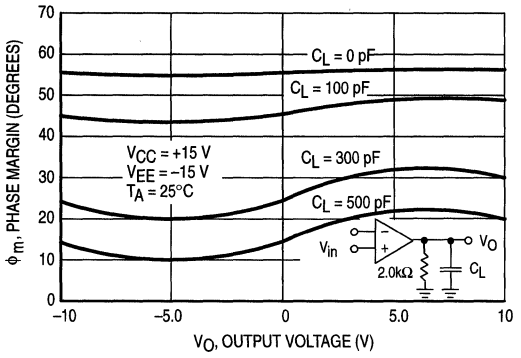


Figure 28. Overshoot versus Output Load Capacitance

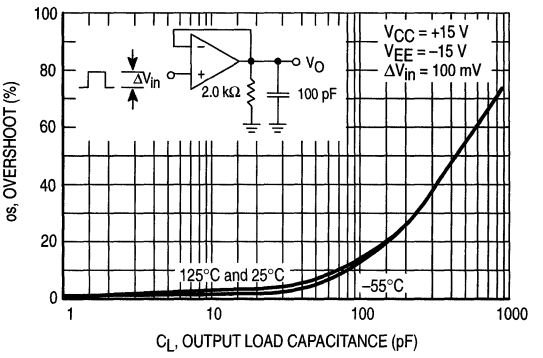


Figure 29. Input Referred Noise Voltage and Current versus Frequency

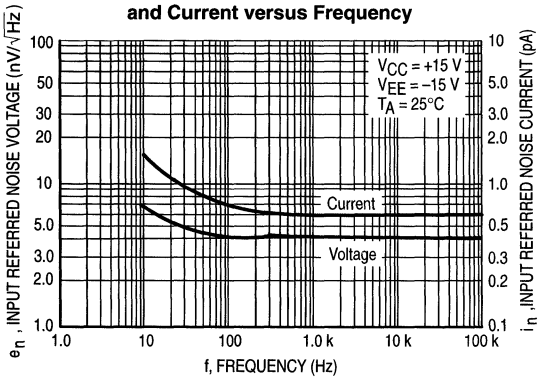


Figure 30. Total Input Referred Noise Voltage versus Source Resistant

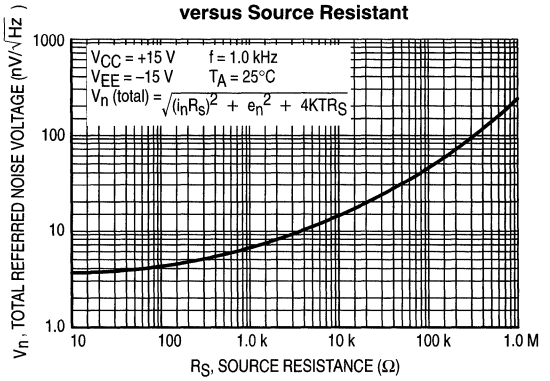


Figure 31. Phase Margin and Gain Margin versus Differential Source Resistance

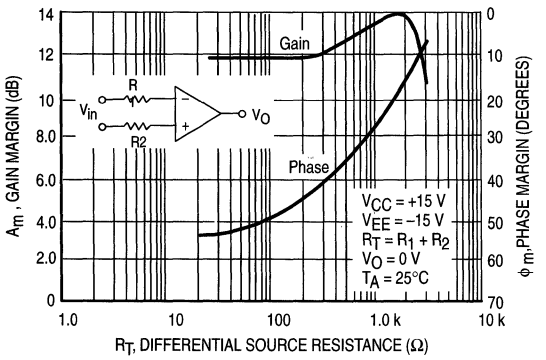


Figure 32. Inverting Amplifer Slew Rate

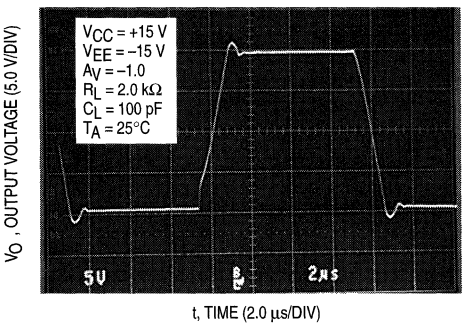


Figure 33. Noninverting Amplifier Slew Rate

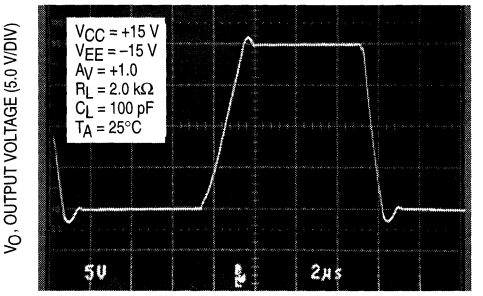


Figure 34. Noninverting Amplifier Overshoot

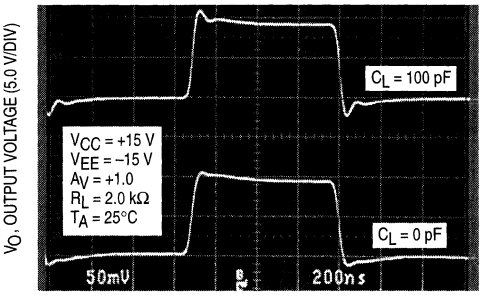
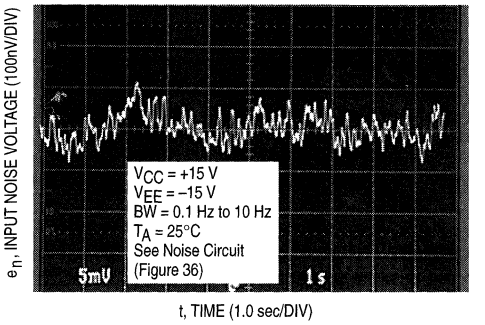


Figure 35. Low Frequency Noise Voltage versus Time



APPLICATIONS INFORMATION

The MC33077 is designed primarily for its low noise, low offset voltage, high gain bandwidth product and large output swing characteristics. Its outstanding high frequency gain/phase performance make it a very attractive amplifier for high quality preamps, instrumentation amps, active filters and other applications requiring precision quality characteristics.

The MC33077 utilizes high frequency lateral PNP input transistors in a low noise bipolar differential stage driving a compensated Miller integration amplifier. Dual–doublet frequency compensation techniques are used to enhance the gain bandwidth product. The output stage uses an all NPN transistor design which provides greater output voltage swing and improved frequency performance over more conventional stages by using both PNP and NPN transistors (Class AB). This combination produces an amplifier with superior characteristics.

Through precision component matching and innovative current mirror design, a lower than normal temperature coefficient of input offset voltage (2.0 μV/°C as opposed to 10 μV/°C), as well as low input offset voltage, is accomplished.

The minimum common mode input range is from 1.5 V below the positive rail (V_{CC}) to 1.5 V above the negative rail (V_{EE}). The inputs will typically common mode to within 1.0 V of both negative and positive rails though degradation in offset voltage and gain will be experienced as the common mode voltage nears either supply rail. In practice, though not recommended, the input voltage may exceed V_{CC} by approximately 30 V and decrease below the V_{EE} by approximately 0.6 V without causing permanent damage to the device. If the input voltage on either or both inputs is less than approximately 0.6 V, excessive current may flow, if not limited, causing permanent damage to the device.

The amplifier will not latch with input source currents up to 20 mA, though in practice, source currents should be limited to 5.0 mA to avoid any parametric damage to the device. If both inputs exceed V_{CC}, the output will be in the high state and phase reversal may occur. No phase reversal will occur if the voltage on one input is within the common mode range and the voltage on the other input exceeds V_{CC}. Phase reversal may occur if the input voltage on either or both inputs is less than 1.0 V above the negative rail. Phase reversal will be experienced if the voltage on either or both inputs is less than V_{EE}.

Through the use of dual–doublet frequency compensation techniques, the gain bandwidth product has been greatly enhanced over other amplifiers using the conventional single pole compensation. The phase and gain error of the amplifier remains low to higher frequencies for fixed amplifier gain configurations.

With the all NPN output stage, there is minimal swing loss to the supply rails, producing superior output swing, no crossover distortion and improved output phase symmetry with output voltage excursions (output phase symmetry being the amplifiers ability to maintain a constant phase relation independent of its output voltage swing). Output phase symmetry degradation in the more conventional PNP and NPN transistor output stage was primarily due to the inherent cut–off frequency mismatch of the PNP and NPN transistors used (typically 10 MHz and 300 MHz, respectively), causing considerable phase change to occur as the output voltage changes. By eliminating the PNP in the output, such phase change has been avoided and a very significant improvement in output phase symmetry as well as output swing has been accomplished.

The output swing improvement is most noticeable when operation is with lower supply voltages (typically 30% with ± 5.0 V supplies). With a 10 k load, the output of the amplifier can typically swing to within 1.0 V of the positive rail (V_{CC}), and to within 0.3 V of the negative rail (V_{EE}), producing a 28.7 V_{pp} signal from ±15 V supplies. Output voltage swing can be further improved by using an output pull–up resistor referenced to the V_{CC}. Where output signals are referenced to the positive supply rail, the pull–up resistor will pull the output to V_{CC} during the positive swing, and during the negative swing, the NPN output transistor collector will pull the output very near V_{EE}. This configuration will produce the maximum attainable output signal from given supply voltages. The value of load resistance used should be much less than any feedback resistance to avoid excess loading and allow easy pull–up of the output.

Output impedance of the amplifier is typically less than 50 Ω at frequencies less than the unity gain crossover frequency (see Figure 18). The amplifier is unity gain stable with output capacitance loads up to 500 pF at full output swing over the –55° to +125°C temperature range. Output phase symmetry is excellent with typically 4°C total phase change over a 20 V output excursion at 25°C with a 2.0 kΩ and 100 pF load. With a 2.0 kΩ resistive load and no capacitance loading, the total phase change is approximately one degree for the same 20 V output excursion. With a 2.0 kΩ and 500 pF load at 125°C, the total phase change is typically only 10°C for a 20 V output excursion (see Figure 27).

As with all amplifiers, care should be exercised to insure that one does not create a pole at the input of the amplifier which is near the closed loop corner frequency. This becomes a greater concern when using high frequency amplifiers since it is very easy to create such a pole with relatively small values of resistance on the inputs. If this does

occur, the amplifier's phase will degrade severely causing the amplifier to become unstable. Effective source resistances, acting in conjunction with the input capacitance of the amplifier, should be kept to a minimum to avoid creating such a pole at the input (see Figure 31). There is minimal effect on stability where the created input pole is much greater than the closed loop corner frequency. Where amplifier stability is affected as a result of a negative feedback resistor in conjunction with the amplifier's input capacitance, creating a pole near the closed loop corner frequency, lead capacitor compensation techniques (lead capacitor in parallel with the feedback resistor) can be employed to improve stability. The feedback resistor and lead capacitor RC time constant should be larger than that of the uncompensated input pole frequency. Having a high resistance connected to the noninverting input of the amplifier can create a like instability problem. Compensation for this condition can be accomplished by adding a lead capacitor in parallel with the noninverting input resistor of such a value as to make the RC time constant larger than the RC time constant of the uncompensated input resistor acting in conjunction with the amplifiers input capacitance.

For optimum frequency performance and stability, careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input output coupling. In order to reduce the input capacitance, the body of resistors connected to the input pins should be physically close to the input pins. This not only minimizes the input pole creation for optimum frequency response, but also minimizes extraneous signal "pickup" at this node. Power supplies should be decoupled with adequate capacitance as close as possible to the device supply pin.

In addition to amplifier stability considerations, input source resistance values should be low to take full advantage of the low noise characteristics of the amplifier. Thermal noise (Johnson Noise) of a resistor is generated by thermally–charged carriers randomly moving within the resistor creating a voltage. The rms thermal noise voltage in a resistor can be calculated from:

$$E_{nr} = \sqrt{4kTR \times BW}$$

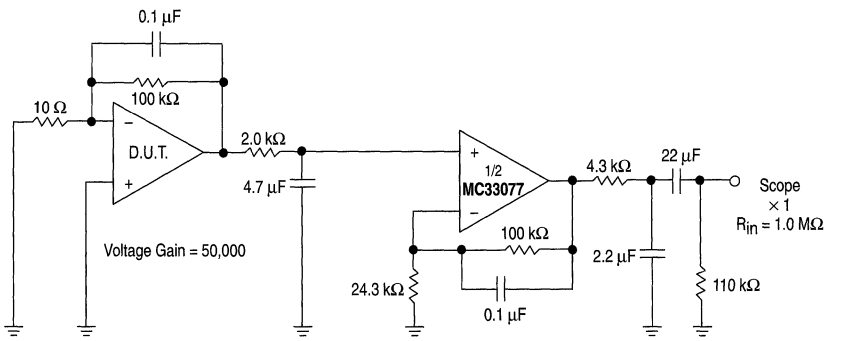
where:

k = Boltzmann's Constant (1.38×10^{-23} joules/k)
T = Kelvin temperature
R = Resistance in ohms
BW = Upper and lower frequency limit in Hertz.

By way of reference, a 1.0 kΩ resistor at 25°C will produce a 4.0 $nV/\sqrt{Hz}$ of rms noise voltage. If this resistor is connected to the input of the amplifier, the noise voltage will be gained–up in accordance to the amplifier's gain configuration. For this reason, the selection of input source resistance for low noise circuit applications warrants serious consideration. The total noise of the amplifier, as referred to its inputs, is typically only 4.4 $nV/\sqrt{Hz}$ at 1.0 kHz.

The output of any one amplifier is current limited and thus protected from a direct short to ground, However, under such conditions, it is important not to allow the amplifier to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the temperature rating.

Figure 36. Voltage Noise Test Circuit (0.1 Hz to 10 Hz_{p-p})



Note: All capacitors are non–polarized.

MC33078
MC33079

Dual/Quad Low Noise Operational Amplifiers

DUAL/QUAD LOW NOISE OPERATIONAL AMPLIFIERS

The MC33078/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input voltage noise with high gain bandwidth product and slew rate. The all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source and sink AC frequency performance.

The MC33078/9 family offers both dual and quad amplifier versions, tested over the automotive temperature range and available in the plastic DIP and SOIC packages (P and D suffixes).

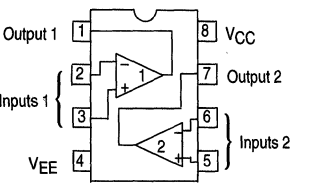
- Dual Supply Operation: ±5.0 V to ±18 V
- Low Voltage Noise: 4.5 nV/$\sqrt{Hz}$
- Low Input Offset Voltage: 0.15 mV
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Total Harmonic Distortion: 0.002%
- High Gain Bandwidth Product: 16 MHz
- High Slew Rate: 7.0 V/μs
- High Open Loop AC Gain: 800 @ 20 kHz
- Excellent Frequency Stability
- Large Output Voltage Swing: +14.1 V/ −14.6 V
- ESD Diodes Provided on the Inputs

DUAL

P SUFFIX
PLASTIC PACKAGE
CASE 626

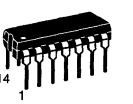
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

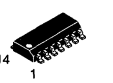


(Dual, Top View)

QUAD

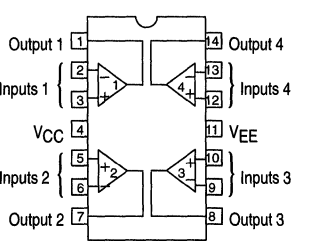


P SUFFIX
PLASTIC PACKAGE
CASE 646



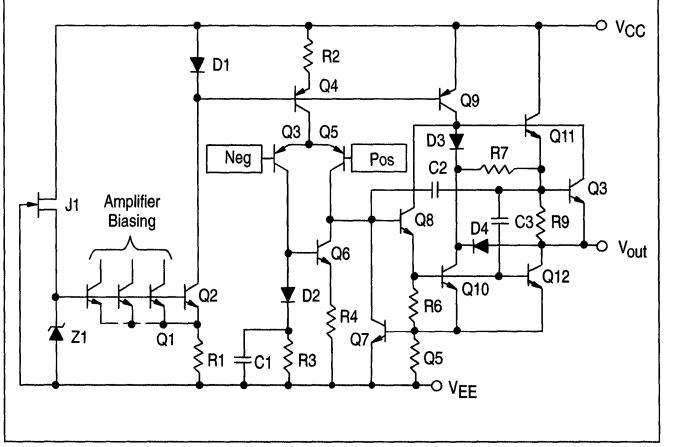
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Quad, Top View)

Representative Schematic Diagram
(Each Amplifier)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33078D MC33078P	T_A = −40° to +85°C	SO–8 Plastic DIP
MC33079D MC33079P		SO–14 Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	$\|V_{IO}\|$				mV
(MC33078) T_A = +25°C		—	0.15	2.0	
T_A = −40° to +85°C		—	—	3.0	
(MC33079) T_A = +25°C		—	0.15	2.5	
T_A = −40° to +85°C		—	—	3.5	
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	—	2.0	—	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				nA
T_A = +25°C		—	300	750	
T_A = −40° to +85°C		—	—	800	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				nA
T_A = +25°C		—	25	150	
T_A = −40° to +85°C		—	—	175	
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	V_{ICR}	±13	±14	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}				dB
T_A = +25°C		90	110	—	
T_A = −40° to +85°C		85	—	—	
Output Voltage Swing (V_{ID} = ±1.0V)					V
R_L = 600 Ω	V_O+	—	+10.7	—	
R_L = 600 Ω	V_O−	—	−11.9	—	
R_L = 2.0 kΩ	V_O+	+13.2	+13.8	—	
R_L = 2.0 kΩ	V_O−	—	−13.7	−13.2	
R_L = 10 kΩ	V_O+	+13.5	+14.1	—	
R_L = 10 kΩ	V_O−	—	−14.6	−14	
Common Mode Rejection (V_{in} = ±13V)	CMR	80	100	—	dB
Power Supply Rejection (Note 3)	PSR	80	105	—	dB
V_{CC}/V_{EE} = +15 V/ −15 V to +5.0 V/ −5.0 V					
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	I_{SC}				mA
Source		+15	+29	—	
Sink		−20	−37	—	
Power Supply Current (V_O = 0 V, All Amplifiers)	I_D				mA
(MC33078) T_A = +25°C		—	4.1	5.0	
T_A = −40° to +85°C		—	—	5.5	
(MC33079) T_A = +25°C		—	8.4	10	
T_A = −40° to +85°C		—	—	11	

NOTE: 3. Measured with V_{CC} and V_{EE} differentially varied simultaneously.

2

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics		Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF A_V = +1.0)		SR	5.0	7.0	—	V/μs
Gain Bandwidth Product (f = 100 kHz)		GBW	10	16	—	MHz
Unity Gain Frequency (Open Loop)		f_U	—	9.0	—	MHz
Gain Margin (R_L = 2.0 kΩ)	C_L = 0 pF C_L = 100 pF	A_m	— —	−11 −6.0	—	dB
Phase Margin (R_L = 2.0 kΩ)	C_L = 0 pF C_L = 100 pF	ϕ_m	— —	55 40	—	Degrees
Channel Separation (f = 20 Hz to 20 kHz)		CS	—	−120	—	dB
Power Bandwidth (V_O = 27 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)		BW_p	—	120	—	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)		THD	—	0.002	—	%
Open Loop Output Impedance (V_O = 0 V, f = 9.0 MHz)		$\|Z_O\|$	—	37	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{IN}	—	175	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{IN}	—	12	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)		e_n	—	4.5	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)		i_n	—	0.5	—	$pA/\sqrt{Hz}$

Figure 1. Maximum Power Dissipation versus Temperature

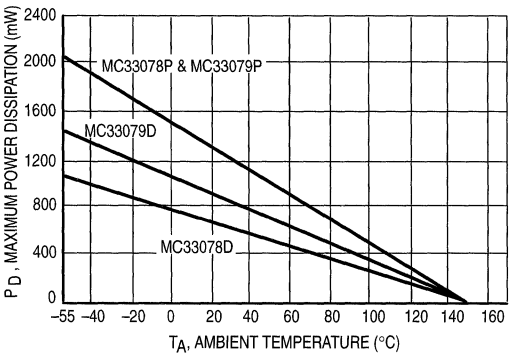


Figure 2. Input Bias Current versus Supply Voltage

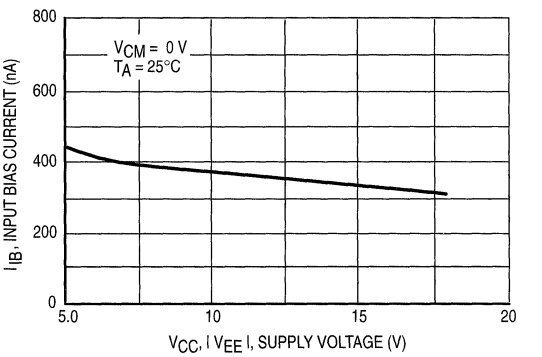


Figure 3. Input Bias Current versus Temperature

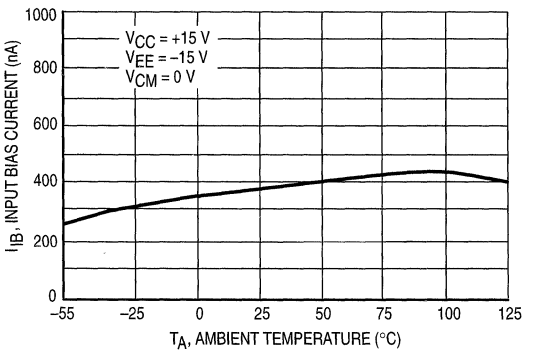


Figure 4. Input Offset Voltage versus Temperature

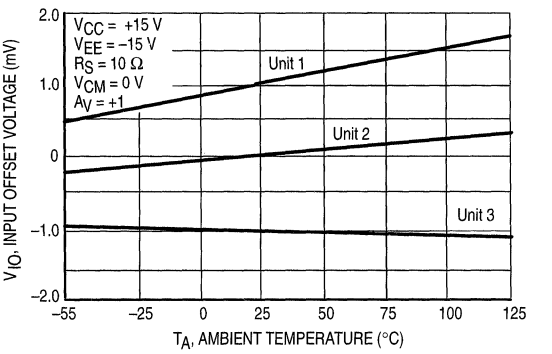


Figure 5. Input Bias Current versus Common Mode Voltage

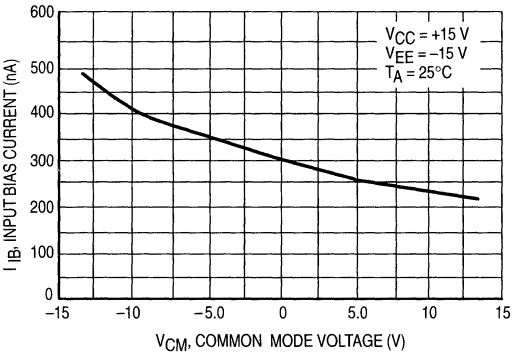


Figure 6. Input Common Mode Voltage Range versus Temperature

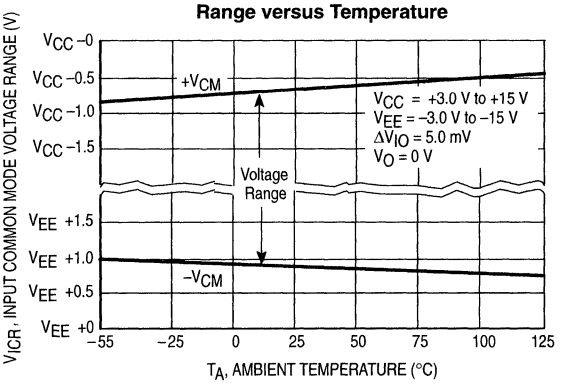


Figure 7. Output Saturation Voltage versus Load Resistance to Ground

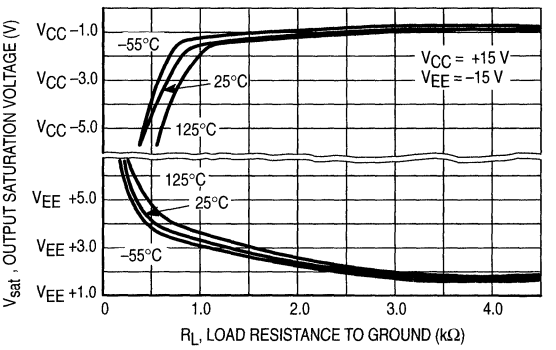


Figure 8. Output Short Circuit Current versus Temperature

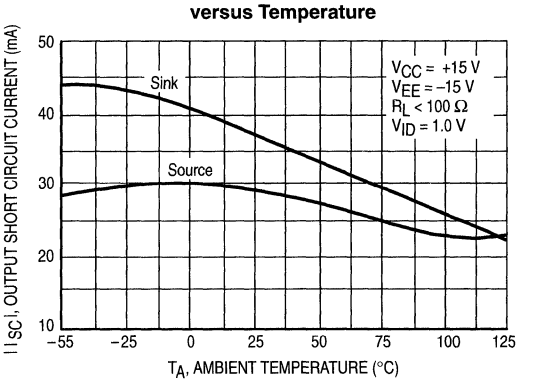


Figure 9. Supply Current versus Temperature

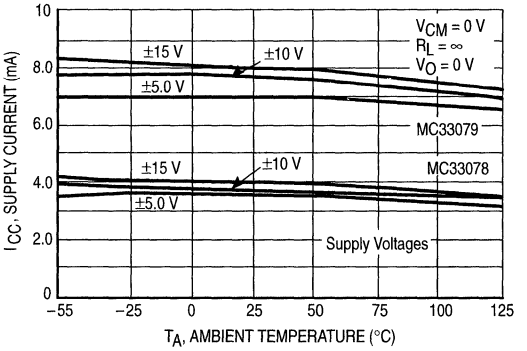
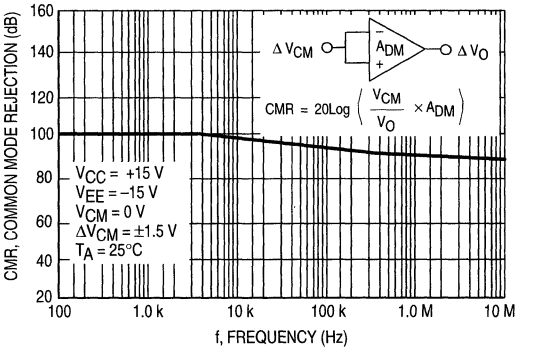


Figure 10. Common Mode Rejection versus Frequency



2

Figure 11. Power Supply Rejection versus Frequency

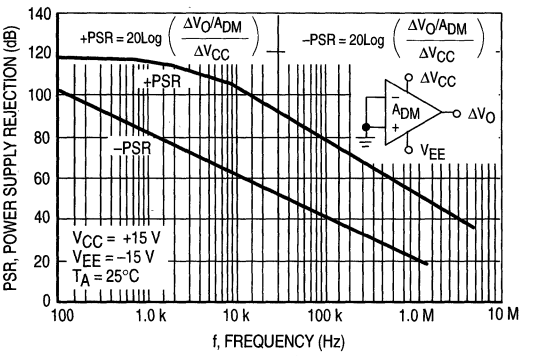


Figure 12. Gain Bandwidth Product versus Supply Voltage

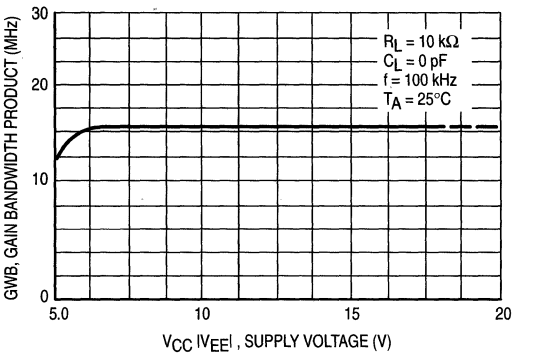


Figure 13. Gain Bandwidth Product versus Temperature

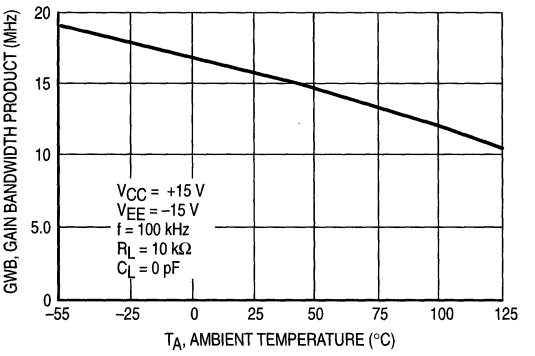


Figure 14. Maximum Output Voltage versus Supply Voltage

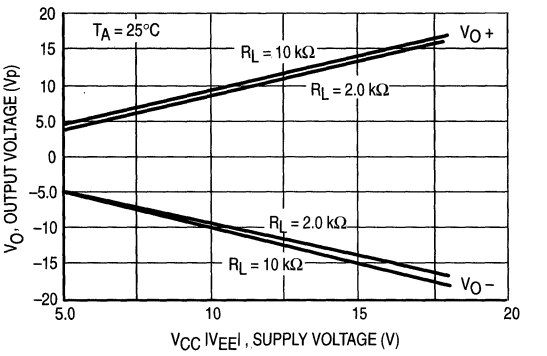


Figure 15. Output Voltage versus Frequency

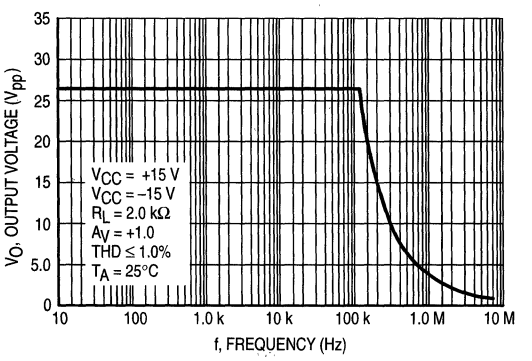


Figure 16. Open Loop Voltage Gain versus Supply Voltage

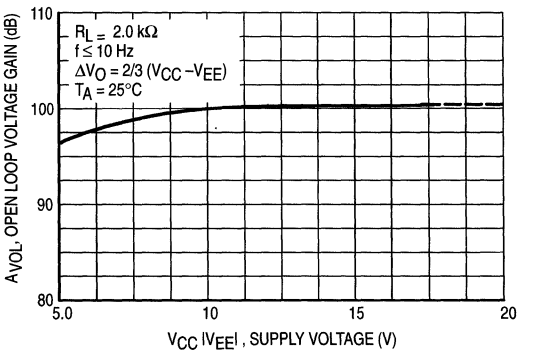


Figure 17. Open Loop Voltage Gain versus Temperature

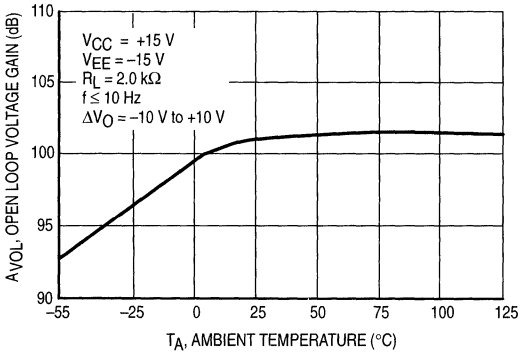


Figure 18. Output Impedance versus Frequency

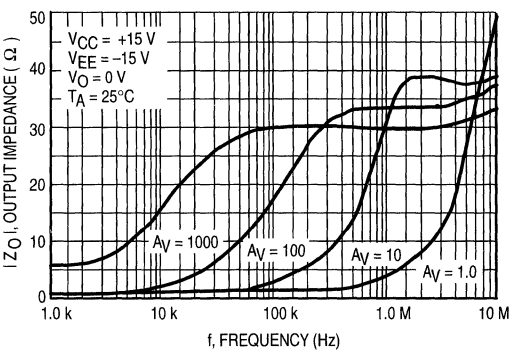


Figure 19. Channel Separation versus Frequency

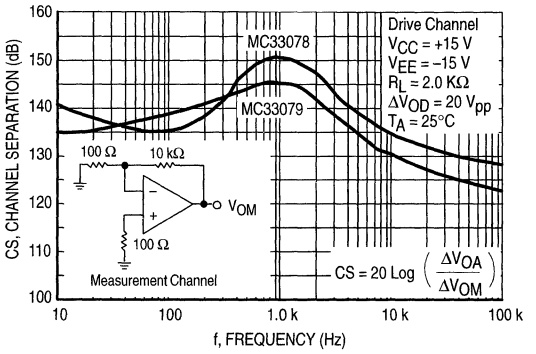


Figure 20. Total Harmonic Distortion versus Frequency

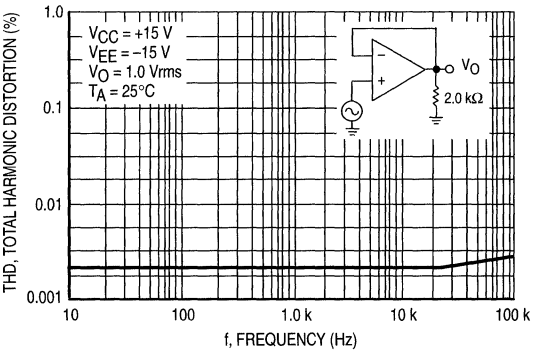


Figure 21. Total Harmonic Distortion versus Output Voltage

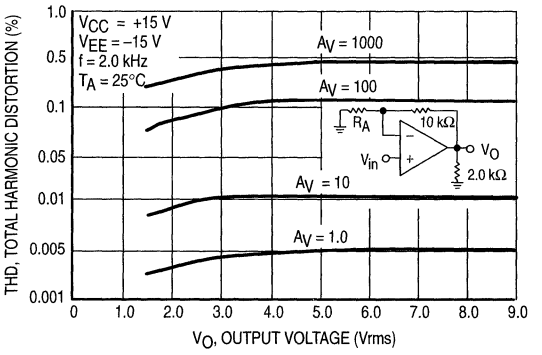
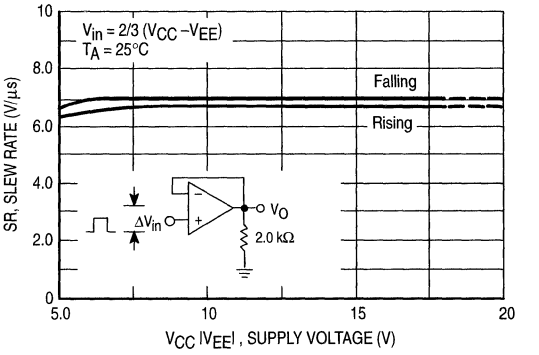


Figure 22. Slew Rate versus Supply Voltage



2

Figure 23. Slew Rate versus Temperature

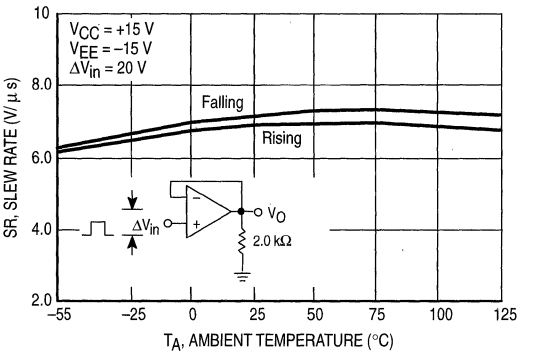


Figure 24. Voltage Gain and Phase versus Frequency

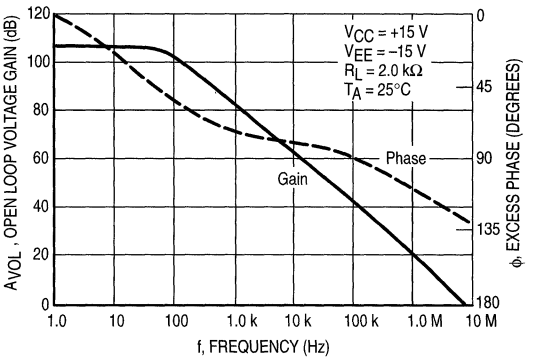


Figure 25. Open Loop Gain Margin and Phase Margin versus Load Capacitance

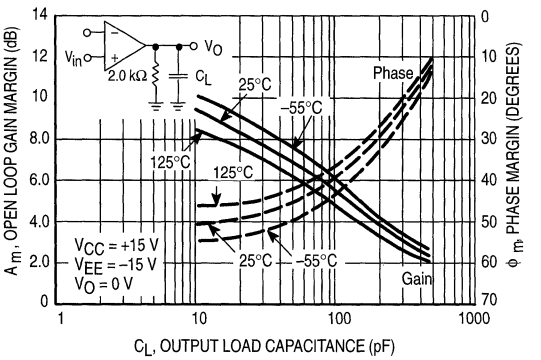


Figure 26. Overshoot versus Output Load Capacitance

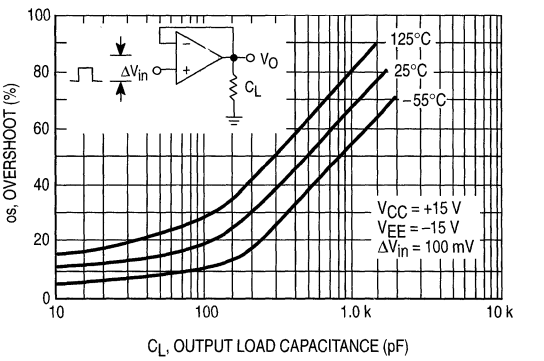


Figure 27. Input Referred Noise Voltage and Current versus Frequency

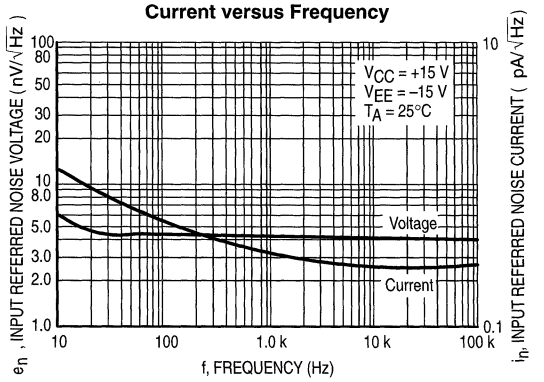


Figure 28. Total Input Referred Noise Voltage versus Source Resistance

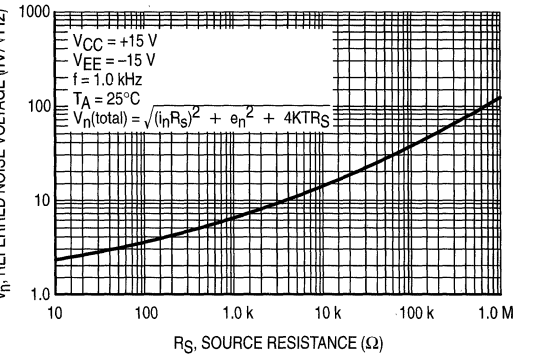


Figure 29. Phase Margin and Gain Margin versus Differential Source Resistance

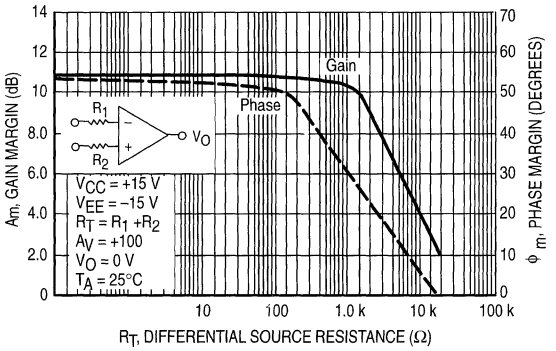


Figure 30. Inverting Amplifier Slew Rate

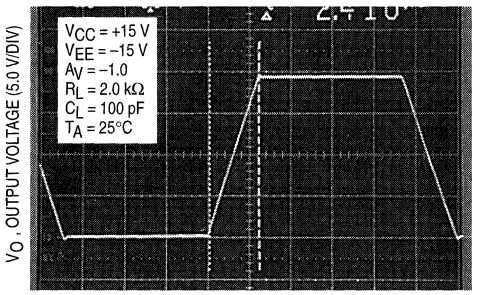


Figure 31. Noninverting Amplifier Slew Rate

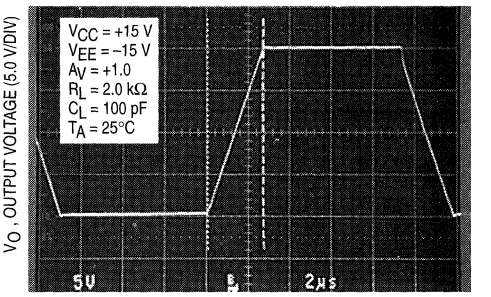


Figure 32. Noninverting Amplifier Overshoot

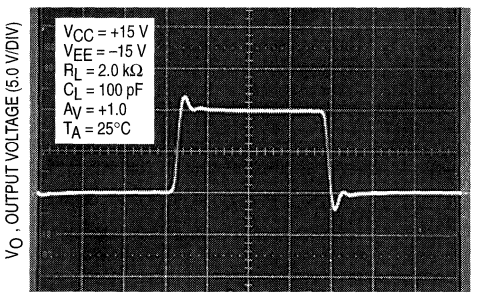
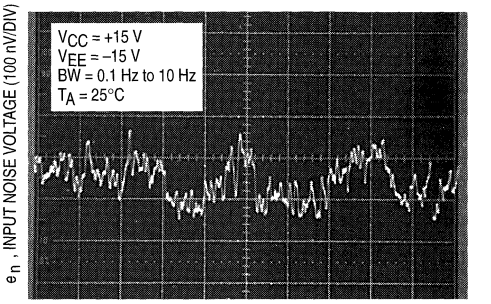
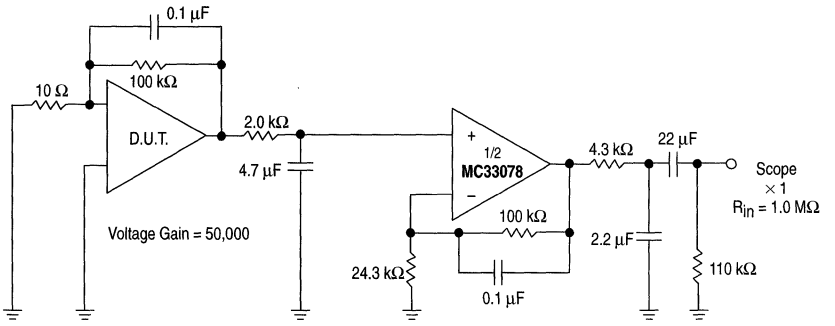


Figure 33. Low Frequency Noise Voltage versus Time



2

Figure 34. Voltage Noise Test Circuit (0.1 Hz to 10 Hz_{p-p})



Note: All capacitors are non–polarized.

MOTOROLA

Sleep-Mode™ Two-State, Micropower Operational Amplifier

The MC33102 dual operational amplifier is an innovative design concept employing Sleep–Mode technology. Sleep–Mode amplifiers have two separate states, a sleepmode and an awakemode. In sleepmode, the amplifier is active and waiting for an input signal. When a signal is applied causing the amplifier to source or sink 160 μA (typically) to the load, it will automatically switch to the awakemode which offers higher slew rate, gain bandwidth, and drive capability.

- Two States: "Sleepmode" (Micropower) and "Awakemode" (High Performance)
- Switches from Sleepmode to Awakemode in 4.0 μs when Output Current Exceeds the Threshold Current (R_L = 600 Ω)
- Independent Sleepmode Function for Each Op Amp
- Standard Pinouts – No Additional Pins or Components Required
- Sleepmode State – Can Be Used in the Low Current Idle State as a Fully Functional Micropower Amplifier
- Automatic Return to Sleepmode when Output Current Drops Below Threshold
- No Deadband/Crossover Distortion; as Low as 1.0 Hz in the Awakemode
- Drop–in Replacement for Many Other Dual Op Amps
- ESD Clamps on Inputs Increase Reliability without Affecting Device Operation

TYPICAL SLEEPMODE/AWAKEMODE PERFORMANCE

Characteristic	Sleepmode (Typical)	Awakemode (Typical)	Unit
Low Current Drain	45	750	μA
Low Input Offset Voltage	0.15	0.15	mV
High Output Current Capability	0.15	50	mA
Low T.C. of Input Offset Voltage	1.0	1.0	μV/°C
High Gain Bandwidth (@ 20 kHz)	0.33	4.6	MHz
High Slew Rate	0.16	1.7	V/μs
Low Noise (@ 1.0 kHz)	28	9.0	nV/√Hz

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range Input Voltage Range	V_{IDR} V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	(Note 2)	sec
Maximum Junction Temperature Storage Temperature	T_J T_{stg}	+150 −65 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (refer to Figure 1).

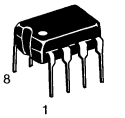
MC33102

DUAL SLEEP–MODE OPERATIONAL AMPLIFIER

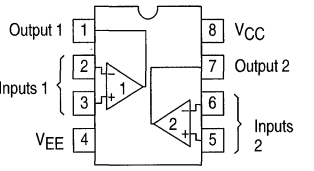
SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

P SUFFIX
PLASTIC PACKAGE
CASE 626



PIN CONNECTIONS



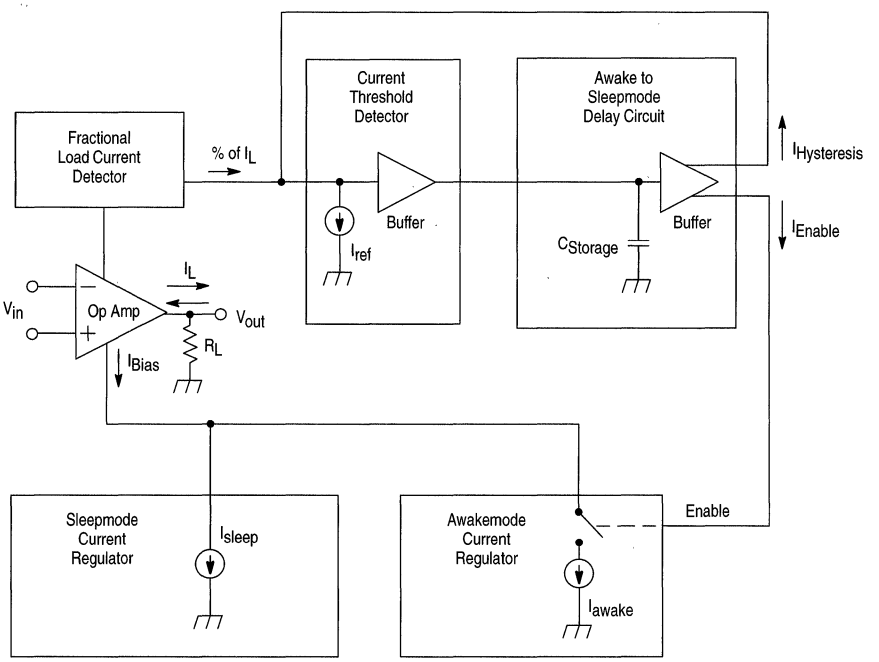
(Dual, Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33102D	T_A = – 40° to +85°C	SO–8
MC33102P		Plastic DIP

2

Simplified Block Diagram



DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	2	$\lvert V_{IO} \rvert$				mV
Sleepmode						
T_A = +25°C			—	0.15	2.0	
T_A = –40° to +85°C			—	—	3.0	
Awakemode						
T_A = +25°C			—	0.15	2.0	
T_A = –40° to +85°C			—	—	3.0	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	3	$\Delta V_{IO}/\Delta T$				µV/°C
T_A = –40° to +85°C (Sleepmode and Awakemode)			—	1.0	—	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	4, 6	I_{IB}				nA
Sleepmode						
T_A = +25°C			—	8.0	50	
T_A = –40° to +85°C			—	—	60	
Awakemode						
T_A = +25°C			—	100	500	
T_A = –40° to +85°C			—	—	600	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	—	$\lvert I_{IO} \rvert$				nA
Sleepmode						
T_A = +25°C			—	0.5	5.0	
T_A = –40° to +85°C			—	—	6.0	
Awakemode						
T_A = +25°C			—	5.0	50	
T_A = –40° to +85°C			—	—	60	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	5	V_{ICR}				V
Sleepmode and Awakemode			–13	–14.8	—	
			—	+14.2	+13	
Large Signal Voltage Gain	7	A_{VOL}				kV/V
Sleepmode (RL = 1.0 MΩ)						
T_A = +25°C			25	200	—	
T_A = –40° to +85°C			15	—	—	
Awakemode (V_O = ±10 V, R_L = 600 Ω)						
T_A = +25°C			50	700	—	
T_A = –40° to +85°C			25	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 10					V
Sleepmode (V_{CC} = +15 V, V_{EE} = –15 V)						
R_L = 1.0 MΩ		V_{O+}	+13.5	+14.2	—	
R_L = 1.0 MΩ		V_{O-}	—	–14.2	–13.5	
Awakemode (V_{CC} = +15 V, V_{EE} = –15 V)						V
R_L = 600 Ω		V_{O+}	+12.5	+13.6	—	
R_L = 600 Ω		V_{O-}	—	–13.6	–12.5	
R_L = 2.0 kΩ		V_{O+}	+13.3	+14	—	
R_L = 2.0 kΩ		V_{O-}	—	–14	–13.3	
Awakemode (V_{CC} = +2.5 V, V_{EE} = –2.5 V)						
R_L = 600 Ω		V_{O+}	+1.1	+1.6	—	
R_L = 600 Ω		V_{O-}	—	–1.6	–1.1	
Common Mode Rejection (V_{CM} = ±13 V)	11	CMR				dB
Sleepmode and Awakemode			80	90	—	
Power Supply Rejection (V_{CC}/V_{EE} = +15 V/–15 V, 5.0 V/–15 V, +15 V/–5.0 V)	12	PSR				dB
Sleepmode and Awakemode			80	100	—	
Output Transition Current	13, 14					μA
Sleepmode to Awakemode (Source/Sink)		$\lvert I_{TH1} \rvert$				
(V_S = ±15 V)			200	160	—	
(V_S = ±2.5 V)			250	200	—	
Awakemode to Sleepmode (Source/Sink)		$\lvert I_{TH2} \rvert$				
(V_S = ±15 V)			—	142	90	
(V_S = ±2.5 V)			—	180	140	
Output Short Circuit Current (Awakemode) (V_{ID} = ±1.0 V, Output to Ground)	15, 16	$\lvert I_{SC} \rvert$				mA
Source			50	110	—	
Sink			50	110	—	
Power Supply Current (per Amplifier) (A_{CL} = 1, V_O = 0V)	17	I_D				μA
Sleepmode (V_S = ±15 V)						
T_A = +25°C			—	45	65	
T_A = –40° to +85°C			—	48	70	
Sleepmode (V_S = ±2.5 V)						
T_A = +25°C			—	38	65	
T_A = –40° to +85°C			—	42	—	
Awakemode (V_S = ±15 V)						
T_A = +25°C			—	750	800	
T_A = –40° to +85°C			—	800	900	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –5.0 V to +5.0 V, C_L = 50 pF, A_V = 1.0)	18	SR				V/μs
Sleepmode (R_L = 1.0 MΩ)			0.10	0.16	—	
Awakemode (R_L = 600 Ω)			1.0	1.7	—	
Gain Bandwidth Product	19	GBW				MHz
Sleepmode (f = 10 kHz)			0.25	0.33	—	
Awakemode (f = 20 kHz)			3.5	4.6	—	
Sleepmode to Awakemode Transition Time	20, 21	t_{tr1}				μs
(A_{CL} = 0.1, V_{in} = 0 V to +5.0 V)						
R_L = 600 Ω			—	4.0	—	
R_L = 10 kΩ			—	15	—	
Awakemode to Sleepmode Transition Time	22	t_{tr2}	—	1.5	—	sec
Unity Gain Frequency (Open Loop)		f_U				kHz
Sleepmode (R_L = 100 kΩ, C_L = 0 pF)			—	200	—	
Awakemode (R_L = 600 Ω, C_L = 0 pF)			—	2500	—	
Gain Margin	23, 25	A_M				dB
Sleepmode (R_L = 100 kΩ, C_L = 0 pF)			—	13	—	
Awakemode (R_L = 600 Ω, C_L = 0 pF)			—	12	—	
Phase Margin	24, 26	$\varnothing_M$				Degrees
Sleepmode (R_L = 100 kΩ, C_L = 0 pF)			—	60	—	
Awakemode (R_L = 600 Ω, C_L = 0 pF)			—	60	—	
Channel Separation (f = 100 Hz to 20 kHz)	29	CS				dB
Sleepmode and Awakemode			—	120	—	
Power Bandwidth (Awakemode)		BW_P				kHz
(V_O = 10 V_{pp}, R_L = 100 kΩ, THD ≤ 1%)			—	20	—	
Total Harmonic Distortion (V_O = 2.0 V_{pp}, A_V = 1.0)	30	THD				%
Awakemode (R_L = 600 Ω)						
f = 1.0 kHz			—	0.005	—	
f = 10 kHz			—	0.016	—	
f = 20 kHz			—	0.031	—	
DC Output Impedance (V_O = 0 V, A_V = 10, I_Q = 10 μA)	31	R_O				Ω
Sleepmode			—	1.0 k	—	
Awakemode			—	96	—	
Differential Input Resistance (V_{CM} = 0 V)		R_{in}				MΩ
Sleepmode			—	1.3	—	
Awakemode			—	0.17	—	
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}				pF
Sleepmode			—	0.4	—	
Awakemode			—	4.0	—	
Equivalent Input Noise Voltage (f = 1.0 kHz, R_S = 100 Ω)	32	e_n				nV/$\sqrt{Hz}$
Sleepmode			—	28	—	
Awakemode			—	9.0	—	
Equivalent Input Noise Current (f = 1.0 kHz)	33	i_n				pA/$\sqrt{Hz}$
Sleepmode			—	0.01	—	
Awakemode			—	0.05	—	

Figure 1. Maximum Power Dissipation versus Temperature

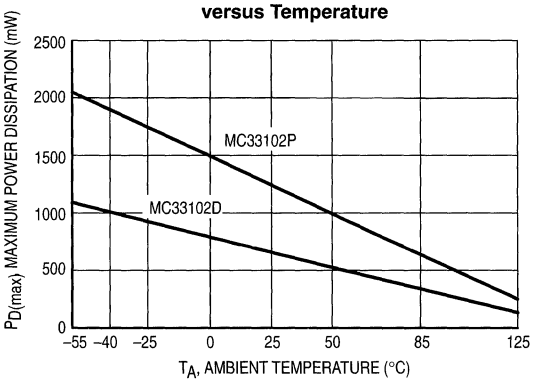


Figure 2. Distribution of Input Offset Voltage (MC33102D Package)

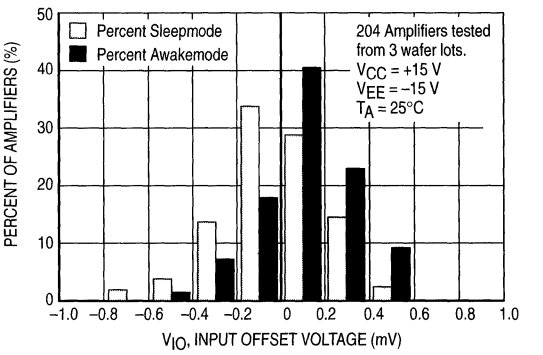


Figure 3. Input Offset Voltage Temperature Coefficient Distribution (MC33102D Package)

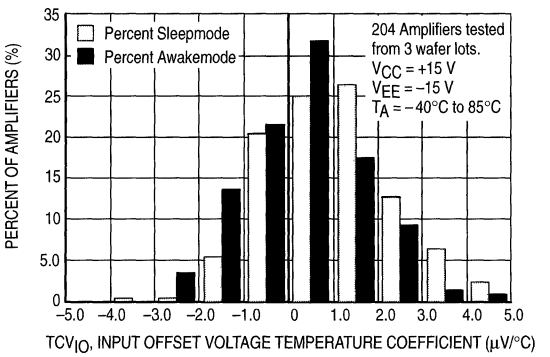


Figure 4. Input Bias Current versus Common Mode Input Voltage

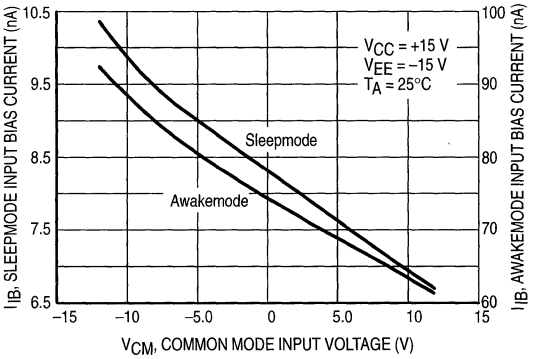


Figure 5. Input Common Mode Voltage Range versus Temperature

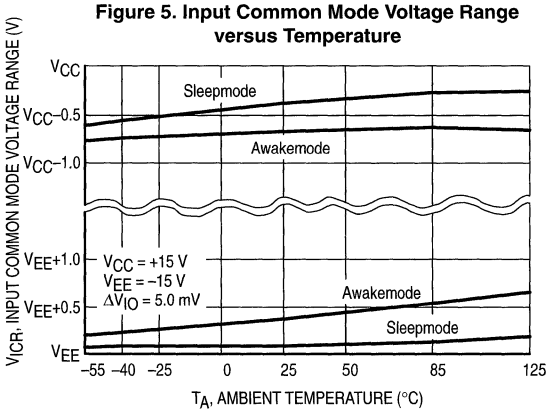
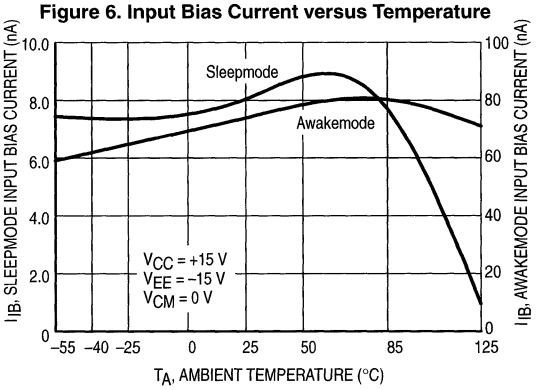


Figure 6. Input Bias Current versus Temperature



2

Figure 7. Open Loop Voltage Gain versus Temperature

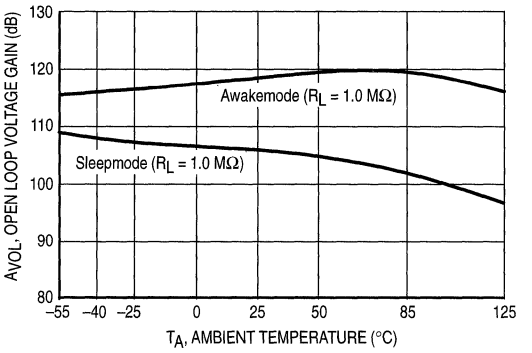


Figure 8. Output Voltage Swing versus Supply Voltage

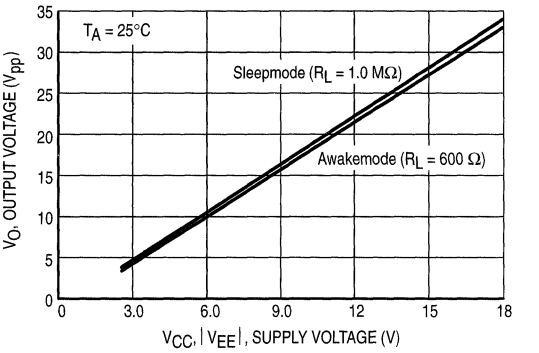


Figure 9. Output Voltage versus Frequency

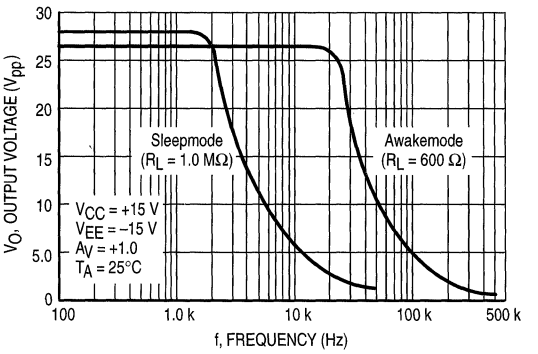


Figure 10. Maximum Peak–to–Peak Output Voltage Swing versus Load Resistance

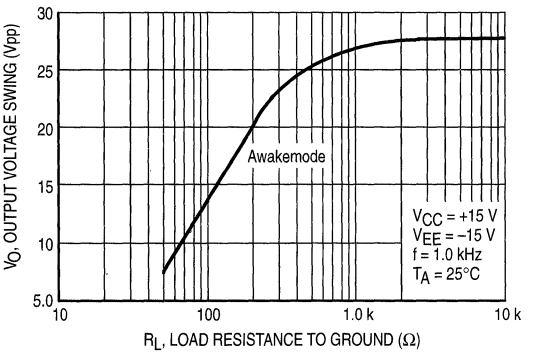


Figure 11. Common Mode Rejection versus Frequency

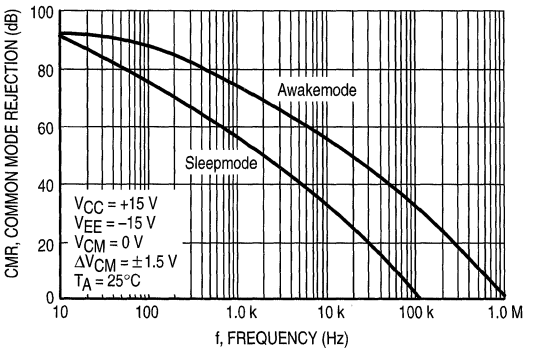


Figure 12. Power Supply Rejection versus Frequency

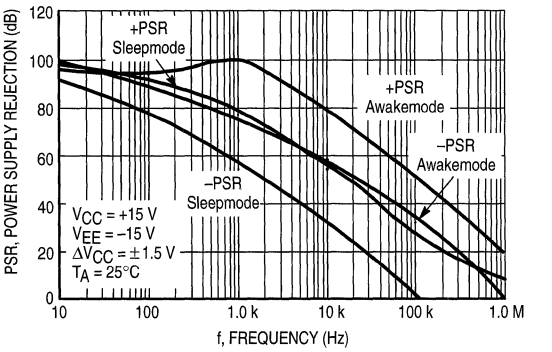


Figure 13. Sleepmode to Awakemode Current Threshold versus Supply Voltage

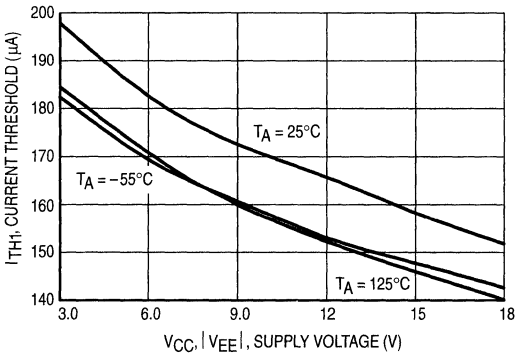


Figure 14. Awakemode to Sleepmode Current Threshold versus Supply Voltage

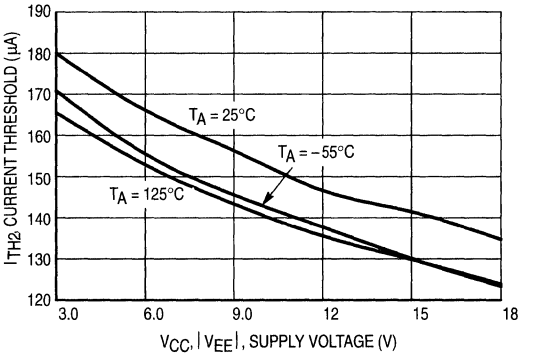


Figure 15. Output Short Circuit Current versus Output Voltage

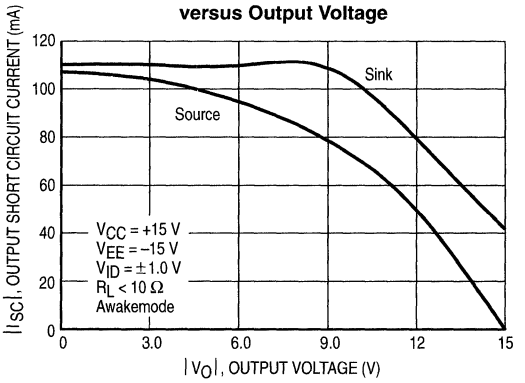


Figure 16. Output Short Circuit Current versus Temperature

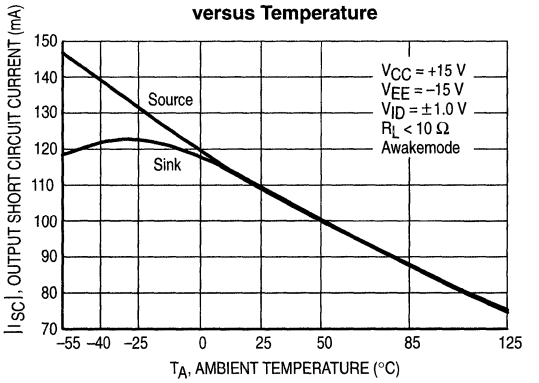


Figure 17. Power Supply Current Per Amplifier versus Temperature

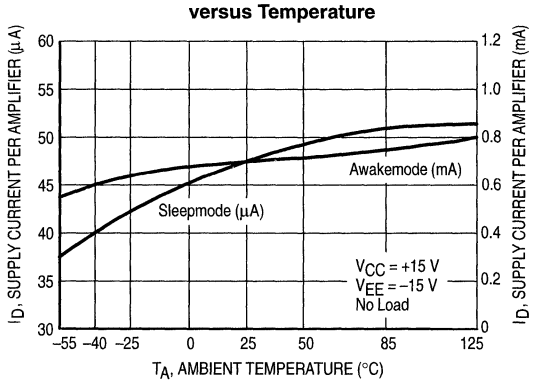
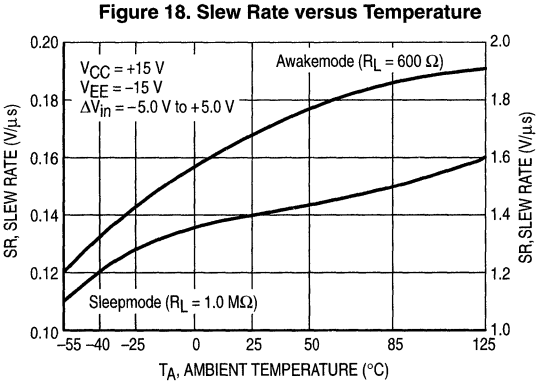


Figure 18. Slew Rate versus Temperature



2

Figure 19. Gain Bandwidth Product versus Temperature

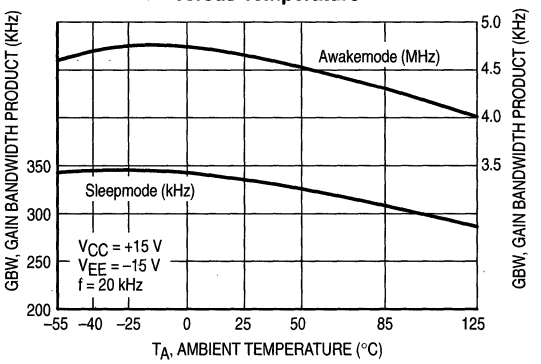


Figure 20. Sleepmode to Awakemode Transition Time

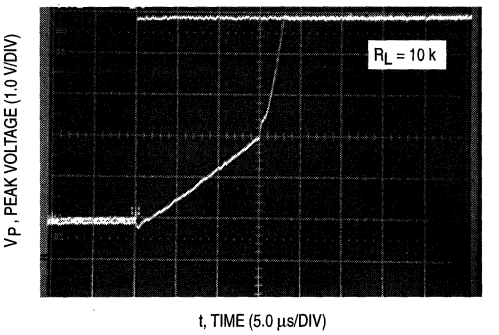


Figure 21. Sleepmode to Awakemode Transition Time

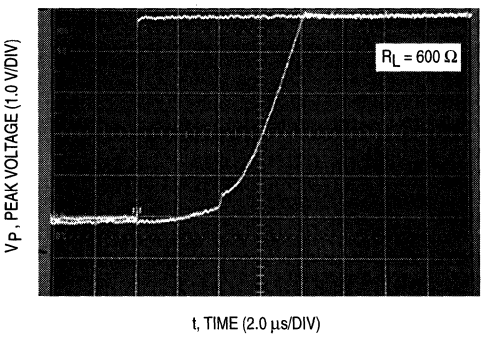


Figure 22. Awakemode to Sleepmode Transition Time versus Supply Voltage

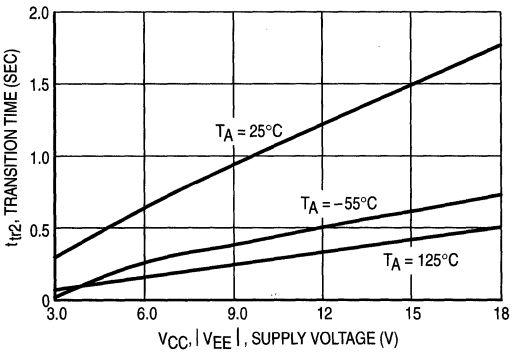


Figure 23. Gain Margin versus Differential Source Resistance

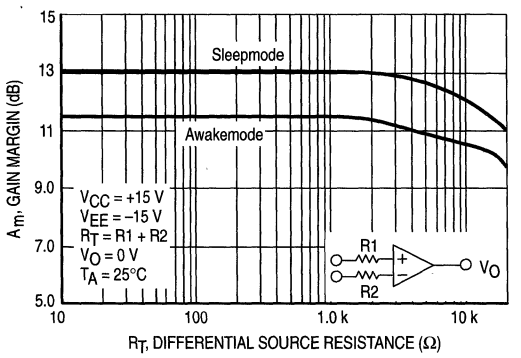


Figure 24. Phase Margin versus Differential Source Resistance

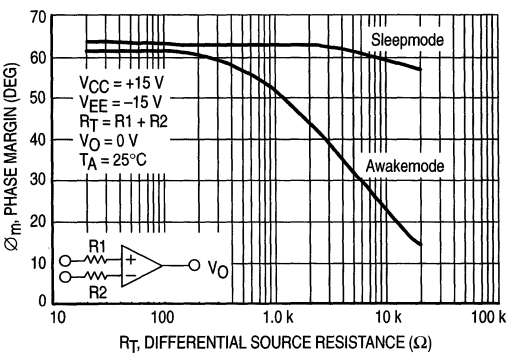


Figure 25. Open Loop Gain Margin versus Output Load Capacitance

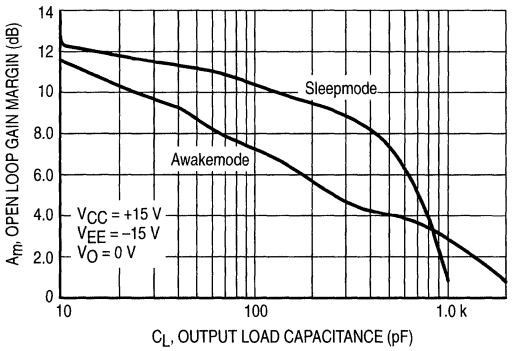


Figure 26. Phase Margin versus Output Load Capacitance

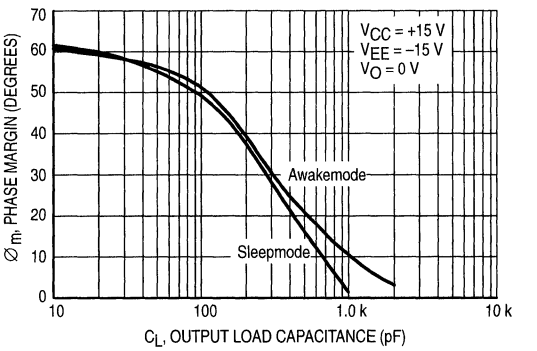


Figure 27. Sleepmode Voltage Gain and Phase versus Frequency

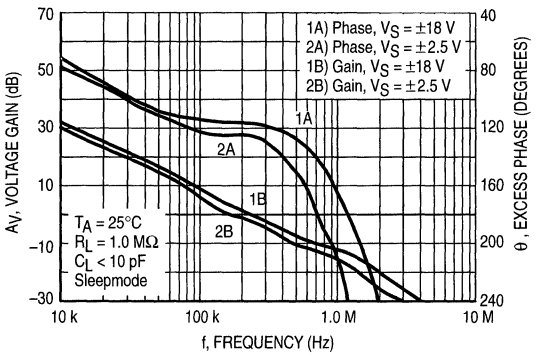


Figure 28. Awakemode Voltage Gain and Phase versus Frequency

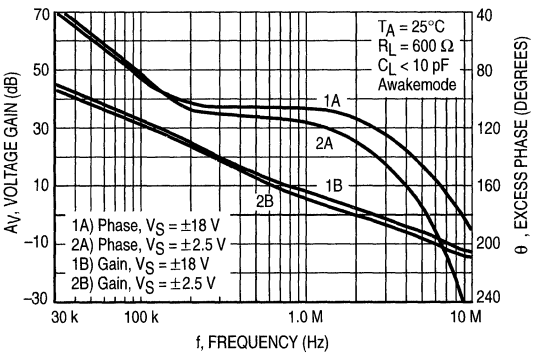


Figure 29. Channel Separation versus Frequency

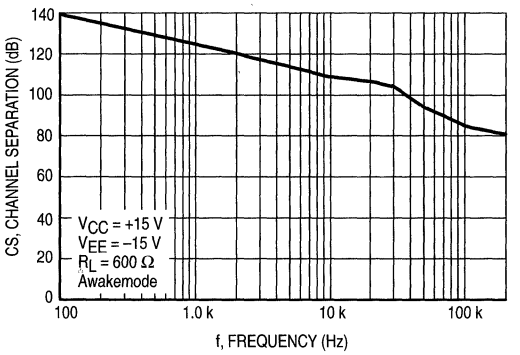
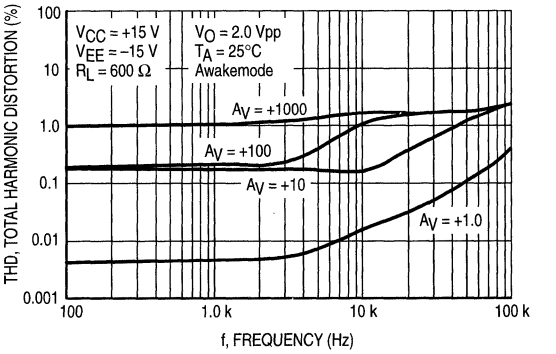


Figure 30. Total Harmonic Distortion versus Frequency



2

Figure 31. Awakemode Output Impedance versus Frequency

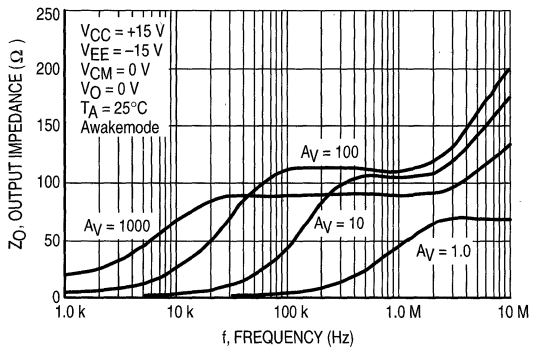


Figure 32. Input Referred Noise Voltage versus Frequency

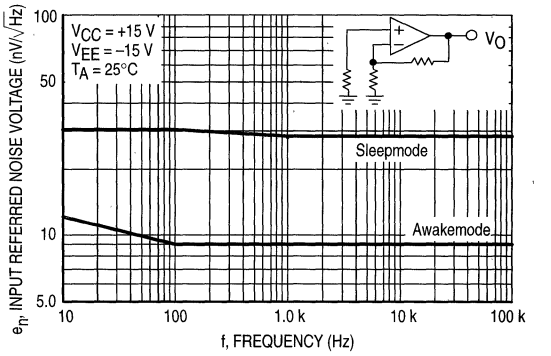


Figure 33. Current Noise versus Frequency

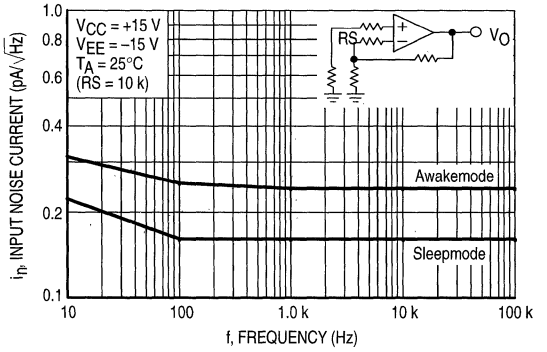


Figure 34. Percent Overshoot versus Load Capacitance

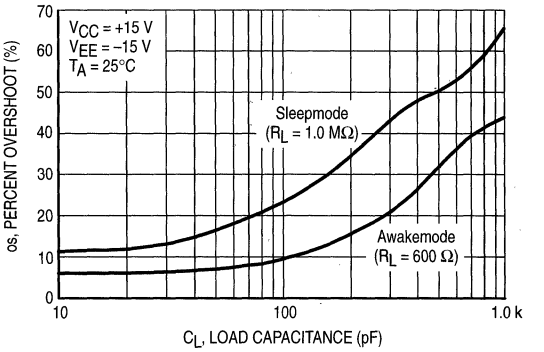


Figure 35. Sleepmode Large Signal Transient Response

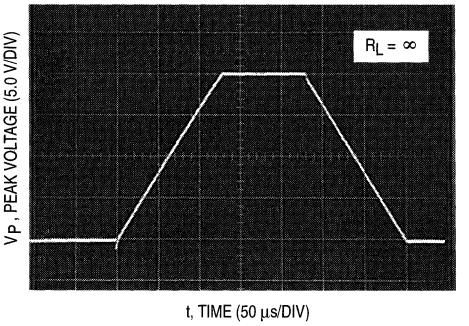


Figure 36. Awakemode Large Signal Transient Response

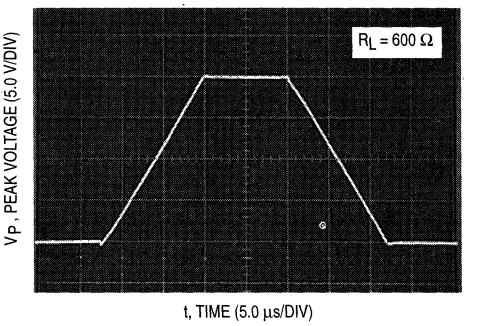


Figure 37. Sleepmode Small Signal Transient Response

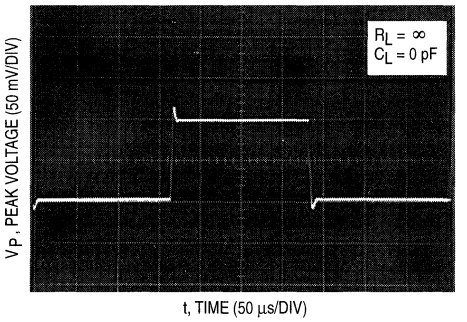
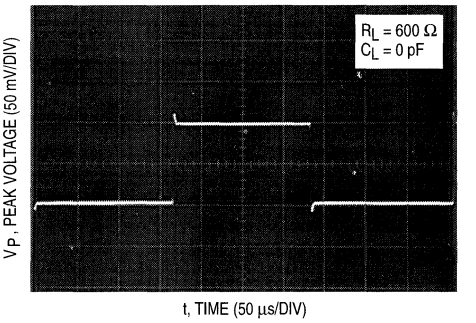


Figure 38. Awakemode Small Signal Transient Response



CIRCUIT INFORMATION

The MC33102 was designed primarily for applications where high performance (which requires higher current drain) is required only part of the time. The two–state feature of this op amp enables it to conserve power during idle times, yet be powered up and ready for an input signal. Possible applications include laptop computers, automotive, cordless phones, baby monitors, and battery operated test equipment. Although most applications will require low power consumption, this device can be used in any application where better efficiency and higher performance is needed.

The Sleep–Mode™ amplifier has two states; a sleepmode and an awakemode. In the sleepmode state, the amplifier is active and functions as a typical micropower op amp. When a signal is applied to the amplifier causing it to source or sink sufficient current (see Figure 13), the amplifier will automatically switch to the awakemode. See Figures 20 and 21 for transition times with 600 Ω and 10 kΩ loads.

The awakemode uses higher drain current to provide a high slew rate, gain bandwidth, and output current capability. In the awakemode, this amplifier can drive 27 Vpp into a 600 Ω load with $V_S = \pm 15$ V.

An internal delay circuit is used to prevent the amplifier from returning to the sleepmode at every zero crossing. This delay circuit also eliminates the crossover distortion commonly found in micropower amplifiers. This amplifier can process frequencies as low as 1.0 Hz without the amplifier returning to sleepmode, depending on the load.

The first stage PNP differential amplifier provides low noise performance in both the sleep and awake modes, and an all NPN output stage provides symmetrical source and sink AC frequency response.

APPLICATIONS INFORMATION

The MC33102 will begin to function at power supply voltages as low as $V_S = \pm 1.0$ V at room temperature. (At this voltage, the output voltage swing will be limited to a few hundred millivolts.) The input voltages must range between V_{CC} and V_{EE} supply voltages as shown in the maximum rating table. Specifically, **allowing the input to go more negative than 0.3 V below V_{EE} may cause product damage.** Also, exceeding the input common mode voltage range on either input may cause phase reversal, even if the inputs are between V_{CC} and V_{EE}.

When power is initially applied, the part may start to operate in the awakemode. This is because of the currents generated due to charging of internal capacitors. When this occurs and the sleepmode state is desired, the user will have to wait approximately 1.5 seconds before the device will switch back to the sleepmode. To prevent this from occurring, ramp the power supplies from 1.0 V to full supply. Notice that the device is more prone to switch into the awakemode when V_{EE} is adjusted than with a similar change in V_{CC}.

The amplifier is designed to switch from sleepmode to awakemode whenever the output current exceeds a preset current threshold (I_{TH}) of approximately 160 µA. As a result, the output switching threshold voltage (V_{ST}) is controlled by the output loading resistance (R_L). This loading can be a load resistor, feedback resistors, or both. Then:

$$V_{ST} = (160\ \mu A) \times R_L$$

Large valued load resistors require a large output voltage to switch, but reduce unwanted transitions to the awakemode. For instance, in cases where the amplifier is connected with a large closed loop gain (A_{CL}), the input offset voltage (V_{IO}) is multiplied by the gain at the output and could produce an output voltage exceeding V_{ST} with no input signal applied.

Small values of R_L allow rapid transition to the awakemode because most of the transition time is consumed slewing in the sleepmode until V_{ST} is reached (see Figures 20, 21). The output switching threshold voltage V_{ST} is higher for larger values of R_L, requiring the amplifier to slew longer in the slower sleepmode state before switching to the awakemode.

The transition time (t_{tr1}) required to switch from sleep to awake mode is:

$$t_{tr1} = t_D = I_{TH} (R_L/SR_{sleepmode})$$

Where: t_D = Amplifier delay (<1.0 μs)
I_{TH} = Output threshold current for more transition (160 μA)
R_L = Load resistance
$SR_{sleepmode}$ = Sleepmode slew rate (0.16 V/μs)

Although typically 160 μA, I_{TH} varies with supply voltage and temperature. In general, any current loading on the output which causes a current greater than I_{TH} to flow will switch the amplifier into the awakemode. This includes transition currents such as those generated by charging load capacitances. In fact, the maximum capacitance that can be driven while attempting to remain in the sleepmode is approximately 1000 pF.

$$C_{L(max)} = I_{TH}/SR_{sleepmode}$$
$$= 160\ \mu A/(0.16\ V/\mu s)$$
$$= 1000\ pF$$

Any electrical noise seen at the output of the MC33102 may also cause the device to transition to the awakemode. To minimize this problem, a resistor may be added in series with the output of the device (inserted as close to the device as possible) to isolate the op amp from both parasitic and load capacitance.

The awakemode to sleepmode transition time is controlled by an internal delay circuit, which is necessary to prevent the amplifier from going to sleep during every zero crossing. This time is a function of supply voltage and temperature as shown in Figure 22.

Gain bandwidth product (GBW) in both modes is an important system design consideration when using a sleepmode amplifier. The amplifier has been designed to obtain the maximum GBW in both modes. "Smooth" AC transitions between modes with no noticeable change in the amplitude of the output voltage waveform will occur as long as the closed loop gains (A_{CL}) in both modes are substantially equal at the frequency of operation. For smooth AC transitions:

$$(A_{CLsleepmode})\ (BW) < GBW_{sleepmode}$$

Where: $A_{CLsleepmode}$ = Closed loop gain in the sleepmode
BW = The required system bandwidth or operating frequency

TESTING INFORMATION

To determine if the MC33102 is in the awakemode or the sleepmode, the power supply currents (I_{D+} and I_{D-}) must be measured. When the magnitude of **either** power supply current exceeds 400 μA, the device is in the awakemode. When the magnitudes of both supply currents are less than 400 μA, the device is in the sleepmode. Since the total supply current is typically ten times higher in the awakemode than the sleepmode, the two states are easily distinguishable.

The measured value of I_{D+} equals the I_D of both devices (for a dual op amp) plus the output source current of device A and the output source current of device B. Similarly, the measured value of I_{D-} is equal to the I_{D-} of both devices plus the output sink current of each device. I_{out} is the sum of the currents caused by both the feedback loop and load resistance. The total I_{out} needs to be subtracted from the measured I_D to obtain the correct I_D of the dual op amp.

An accurate way to measure the awakemode I_{out} current on automatic test equipment is to remove the I_{out} current on both Channel A and B. Then measure the I_D values before the device goes back to the sleepmode state. The transition will take typically 1.5 seconds with ±15 V power supplies.

The large signal sleepmode testing in the characterization was accomplished with a 1.0 MΩ load resistor which ensured the device would remain in sleepmode despite large voltage swings.

MC33171
MC33172
MC33174

Low Power, Single Supply Operational Amplifiers

Quality bipolar fabrication with innovative design concepts are employed for the MC33171/72/74 series of monolithic operational amplifiers. These devices operate at 180 μA per amplifier and offer 1.8 MHz of gain bandwidth product and 2.1 V/μs slew rate without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage includes ground potential (V_{EE}). With a Darlington input stage, these devices exhibit high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

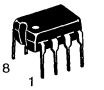
The MC33171/72/74 are specified over the industrial/ automotive temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic as well as the surface mount packages.

- Low Supply Current: 180 μA (Per Amplifier)
- Wide Supply Operating Range: 3.0 V to 44 V or ±1.5 V to ±22 V
- Wide Input Common Mode Range, Including Ground (V_{EE})
- Wide Bandwidth: 1.8 MHz
- High Slew Rate: 2.1 V/μs
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: −14.2 V to +14.2 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 500 pF
- Low Total Harmonic Distortion: 0.03%
- Excellent Phase Margin: 60°C
- Excellent Gain Margin: 15 dB
- Output Short Circuit Protection
- ESD Diodes Provide Input Protection for Dual and Quad

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	MC33171D MC33171P	T_A = −40° to +85°C T_A = −40° to +85°C	SO–8 Plastic DIP
Dual	MC33172D MC33172P	T_A = −40° to +85°C T_A = −40° to +85°C	SO–8 Plastic DIP
Quad	MC33174D MC33174P	T_A = −40° to +85°C T_A = −40° to +85°C	SO–14 Plastic DIP

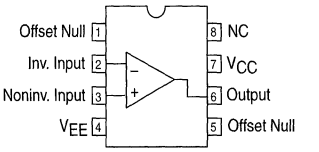
DUAL



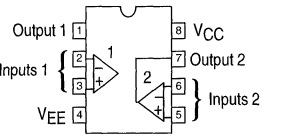
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

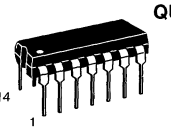


(Single, Top View)

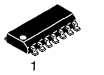


(Top View)

QUAD

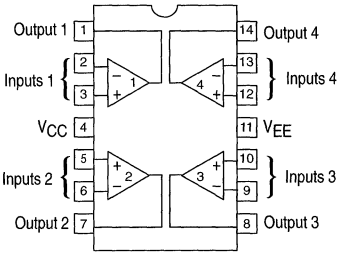


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

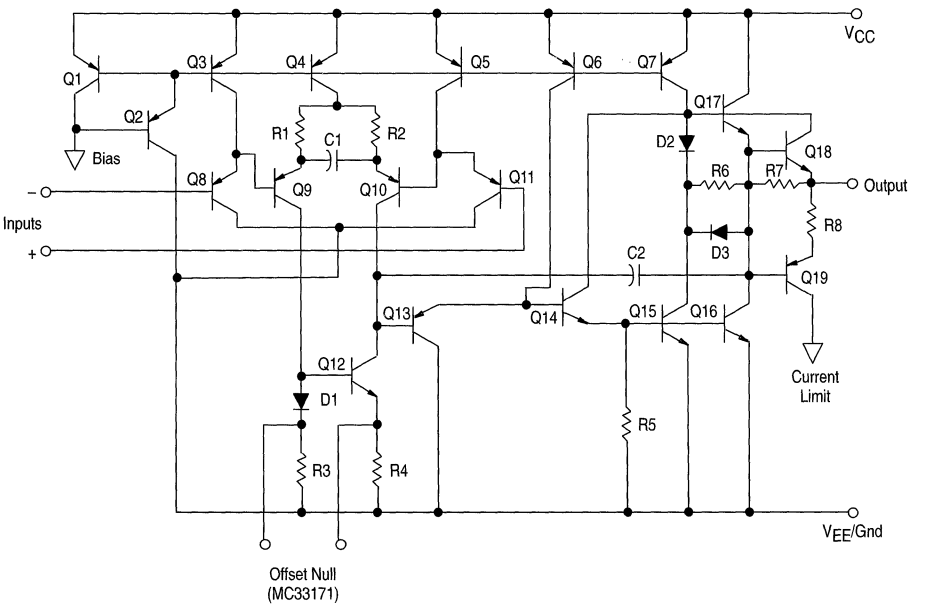
2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	±22	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

Representative Schematic Diagram
(Each Amplifier)



DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} = 0 V)	V_{IO}				mV
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		—	2.0	4.5	
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	2.5	5.0	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}		—	—	6.5	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Bias Current (V_{CM} = 0 V)	I_{IB}				nA
T_A = +25°C		—	20	100	
T_A = T_{low} to T_{high}		—	—	200	
Input Offset Current (V_{CM} = 0 V)	I_{IO}				nA
T_A = +25°C		—	5.0	20	
T_A = T_{low} to T_{high}		—	—	40	
Large Signal Voltage Gain (V_O = ±10 V< R_L = 10 k)	A_{VOL}				V/mV
T_A = +25°C		50	500	—	
T_A = T_{low} to T_{high}		25	—	—	
Output Voltage Swing	V_{OH}				V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 10 k, T_A = +25°C		3.5	4.3	—	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = +25°C		13.6	14.2	—	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = T_{low} to T_{high}		13.3	—	—	
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 10 k, T_A = +25°C	V_{OL}	—	0.05	0.15	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = +25°C		—	−14.2	−13.6	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = T_{low} to T_{high}		—	—	−13.3	
Output Short Circuit (T_A = +25°C)	I_{SC}				mA
Input Overdrive = 1.0 V, Output to Ground					
Source		3.0	5.0	—	
Sink		15	27	—	
Input Common Mode Voltage Range	V_{ICR}				V
T_A = +25°C		V_{EE} to (V_{CC} −1.8)			
T_A = T_{low} to T_{high}		V_{EE} to (V_{CC} −2.2)			
Common Mode Rejection Ratio ($R_S \leq$ 10 k) T_A = +25°C	CMRR	80	90	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω) T_A = +25°C	PSRR	80	100	—	dB
Power Supply Current (Per Amplifier)	I_D				μA
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	180	250	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		—	220	250	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}		—	—	300	

NOTE: 3. T_{low} = −40°C T_{high} = +85°C

2

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 k, C_L = 100 pF) A_V +1 A_V −1	SR	 1.6 —	 2.1 2.1	 — —	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	1.4	1.8	—	MHz
Power Bandwidth A_V = +1.0 R_L = 10 k, V_O = 20 V_{pp}, THD = 5%	BWp	—	35	—	kHz
Phase Margin R_L = 10 k R_L = 10 k, C_L = 100 pF	ϕ_m	 — —	 60 45	 — —	Degrees
Gain Margin R_L = 10 k R_L = 10 k, C_L = 100 pF	A_m	 — —	 15 5.0	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	32	—	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz)	I_n	—	0.2	—	pA/√Hz
Differential Input Resistance V_{cm} = 0 V	R_{in}	—	300	—	MΩ
Input Capacitance	C_i	—	0.8	—	pF
Total Harmonic Distortion A_V = +10, R_L = 10 k, 2.0 $V_{pp} \le V_O \le$ 20 V_{pp}, f = 10 kHz	THD	—	0.03	—	%
Channel Separation (f = 10 kHz)	CS	—	120	—	dB
Open Loop Output Impedance (f = 1.0 MHz)	z_o	—	100	—	Ω

Figure 1. Input Common Mode Voltage Range versus Temperature

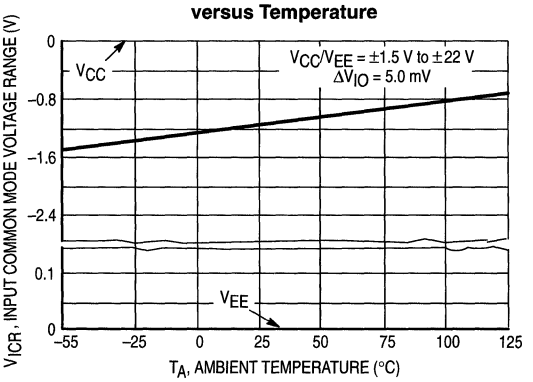


Figure 2. Split Supply Output Saturation versus Load Current

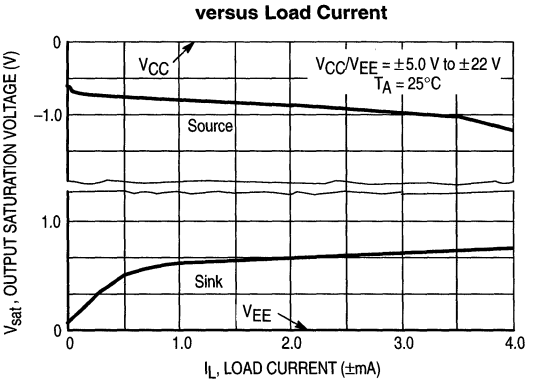


Figure 3. Open Loop Voltage Gain and Phase versus Frequency

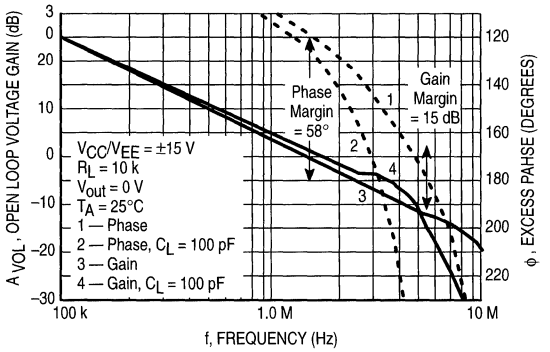


Figure 4. Phase Margin and Percent Overshoot versus Load Capacitance

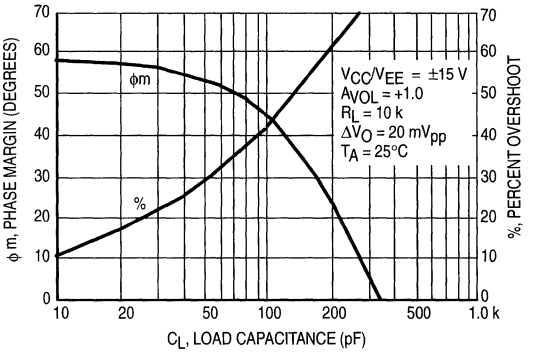


Figure 5. Normalized Gain Bandwidth Product and Slew Rate versus Temperature

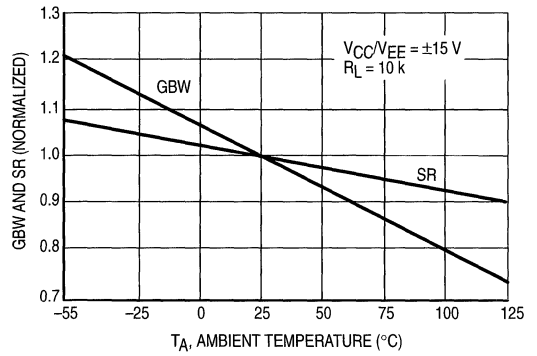


Figure 6. Small and Large Signal Transient Response

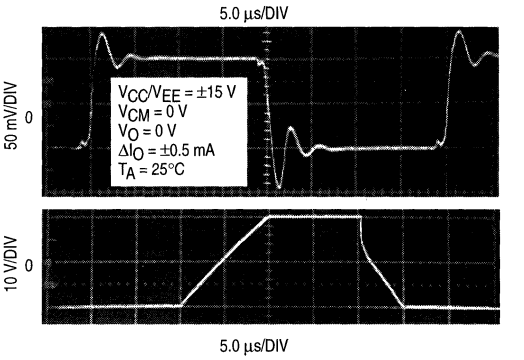


Figure 7. Output Impedance and Frequency

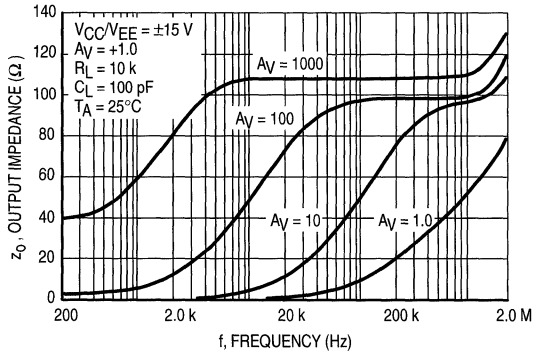
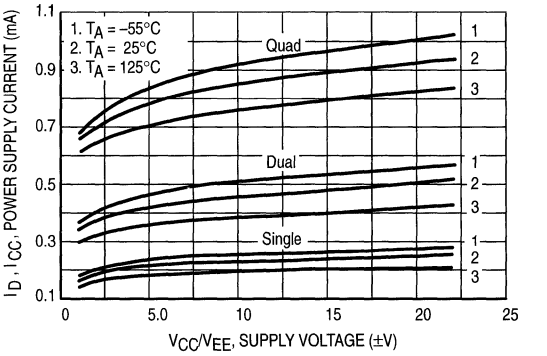


Figure 8. Supply Current versus Supply Voltage



APPLICATIONS INFORMATION – CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC33171/72/74 amplifier family is similar to low power op amp products utilizing JFET input devices, these amplifiers offer additional advantages as a result of the PNP transistor differential inputs and an all NPN transistor output stage.

Because the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{CC} and V_{EE} supply voltages as shown by the maximum rating table. In practice, although *not recommended,* the input voltages can exceed the V_{CC} voltage by approximately 3.0 V and decrease below the V_{EE} voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to 5.0 mA of current from V_{EE} through either inputs' clamping diode without damage or latching, but phase reversal may again occur. If at least one input is within the common mode input voltage range and the other input is within the maximum input voltage range, no phase reversal will occur. If both inputs exceed the upper common mode input voltage limit, the output will be forced to its lowest voltage state.

Since the input capacitance associated with the small geometry input device is substantially lower (0.8 pF) than that of a typical JFET (3.0 pF), the frequency response for a given input source resistance is greatly enhanced. This becomes evident in D–to–A current to voltage conversion applications where the feedback resistance can form a pole with the input capacitance of the op amp. This input pole creates a 2nd Order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 10 kΩ of feedback resistance, the MC33171/72/74 family can typically settle to within 1/2 LSB of 8 bits in 4.2 μs, and within 1/2 LSB of 12 bits in 4.8 μs for a 10 V step. In a standard inverting unity gain fast settling configuration, the symmetrical slew rate is typically ±2.1 V/μs. In the classic noninverting unity gain configuration the typical output positive slew rate is also 2.1 V/μs, and the corresponding negative slew rate will usually exceed the positive slew rate as a function of the fall time of the input waveform.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can typically swing within 0.8 V of the positive rail (V_{CC}) and negative rail (V_{EE}), providing a 28.4 Vpp swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q7, the V_{BE} of the NPN pull–up transistor Q17, and the voltage drop associated with the short circuit resistance, R5. For sink currents less than 0.4 mA, the negative swing is limited by the saturation voltage of the pull–down transistor Q15, and the voltage drop across R4 and R5. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For sink currents (> 0.4 mA), diode D3 clamps the voltage across R4. Thus the negative swing is limited by the saturation voltage of Q15, plus the forward diode drop of D3 ($\approx V_{EE}$ +1.0 V). Therefore an unprecedented peak–to–peak output voltage swing is possible for a given supply voltage as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull–up capability.

Because the PNP output emitter–follower transistor has been eliminated, the MC33171/72/74 family offers a 15 mA minimum current sink capability, typically to an output voltage of (V_{EE} +1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for current switching applications.

In addition, the all NPN transistor output stage is inherently faster than PNP types, contributing to the bipolar amplifier's improved gain bandwidth product. The associated high frequency low output impedance (200 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 400 pF without oscillation in the noninverting unity gain configuration. The 60°C phase margin and 15 dB gain margin, as well as the general gain and phase characteristics, are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The AC characteristics of the MC33171/72/74 family also allow excellent active filter capability, especially for low voltage single supply applications.

Although the single supply specification is defined at 5.0 V, these amplifiers are functional to at least 3.0 V @ 25°C. However slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity, or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

As usual with most high frequency amplifiers, proper lead dress, component placement and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

Figure 9. AC Coupled Noninverting Amplifier with Single +5.0 V Supply

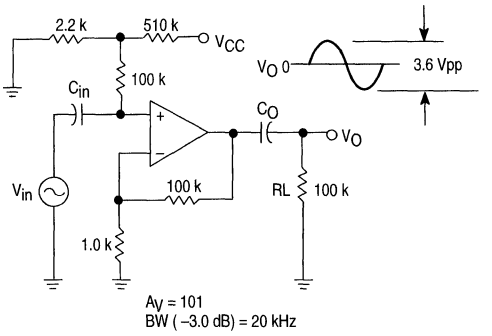


Figure 10. AC Coupled Inverting Amplifier with Single +5.0 V Supply

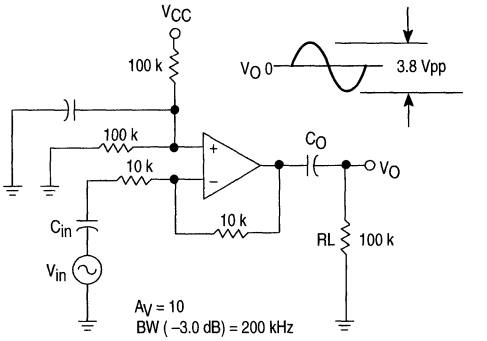


Figure 11. DC Coupled Inverting Amplifier Maximum Output Swing with Single +5.0 V Supply

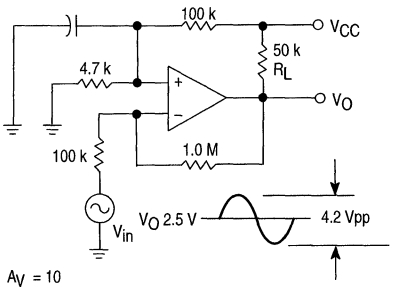
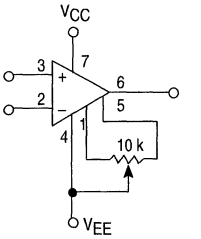


Figure 12. Offset Nulling Circuit



Offset Nulling range is approximately ±80 mV with a 10 k potentiometer, MC33171 only.

Figure 13. Active High–Q Notch Filter

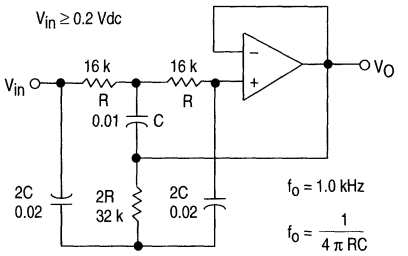
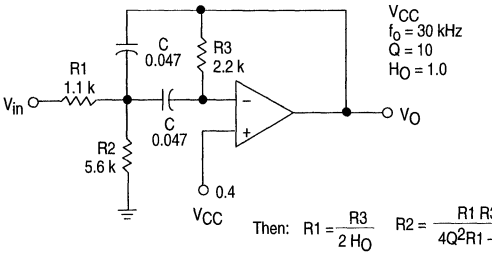


Figure 14. Active Bandpass Filter



Then: $R1 = \frac{R3}{2H_O}$ $R2 = \frac{R1\,R3}{4Q^2R1 - R3}$

Given f_o = center frequency
A_o = Gain at center frequency
Choose Value f_o, Q, A_o, C

$R3 = \frac{Q}{\pi f_o C}$ $\frac{Q_o f_o}{GBW} < 0.1$

For less than 10% error for operational amplifier, where f_o and GBW are expressed in Hz.

2

High Output Current Low Power, Low Noise Bipolar Operational Amplifiers

MC33178
MC33179

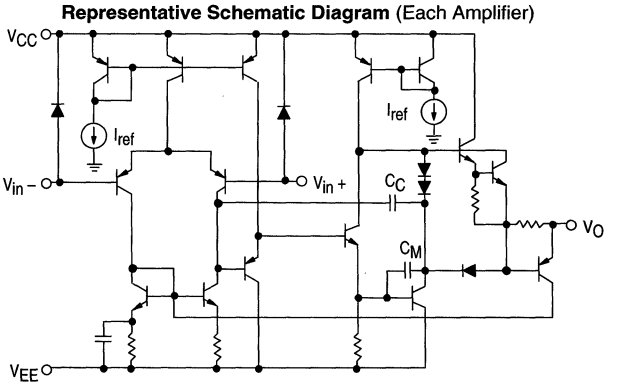
HIGH OUTPUT CURRENT LOW POWER, LOW NOISE OPERATIONAL AMPLIFIERS

The MC33178/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This device family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input offset voltage, noise and distortion. In addition, the amplifier provides high output current drive capability while consuming only 420 μA of drain current per amplifier. The NPN output stage used, exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open–loop high frequency output impedance, symmetrical source and sink AC frequency performance.

The MC33178/9 family offers both dual and quad amplifier versions, tested over the vehicular temperature range, and are available in DIP and SOIC packages.

- 600 Ω Output Drive Capability
- Large Output Voltage Swing
- Low Offset Voltage: 0.15 mV (Mean)
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Total Harmonic Distortion: 0.0024% (@ 1.0 kHz w/600 Ω Load)
- High Gain Bandwidth: 5.0 MHz
- High Slew Rate: 2.0 V/μs
- Dual Supply Operation: ±2.0 V to ±18 V
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Performance

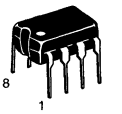
Representative Schematic Diagram (Each Amplifier)



ORDERING INFORMATION

Op Amp Function	Fully Compensated	Operating Temperature Range	Package
Dual	MC33178D MC33178P	T_A = –40° to +85°C	SO–8 Plastic DIP
Quad	MC33179D MC33179P		SO–14 Plastic DIP

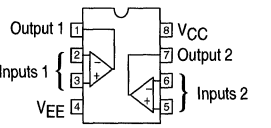
DUAL



P SUFFIX
PLASTIC PACKAGE
CASE 626

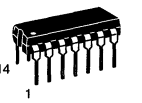
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

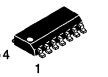


(Top View)

QUAD

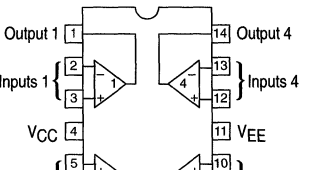


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See power dissipation performance characteristic, Figure 1.)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	2	$\|V_{IO}\|$				mV
(V_{CC} = +2.5 V, V_{EE} = –2.5 V to V_{CC} = +15 V, V_{EE} = –15 V)						
T_A = +25°C			—	0.15	3.0	
T_A = –40° to +85°C			—	—	4.0	
Average Temperature Coefficient of Input Offset Voltage	2	$\Delta V_{IO}/\Delta T$				μV/°C
(R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)						
T_A = –40° to +85°C			—	2.0	—	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	3, 4	I_{IB}				nA
T_A = +25°C			—	100	500	
T_A = –40° to +85°C			—	—	600	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)		$\|I_{IO}\|$				nA
T_A = +25°C			—	5.0	50	
T_A = –40° to +85°C			—	—	60	
Common Mode Input Voltage Range	5	V_{ICR}	–13	–14	—	V
(ΔV_{IO} = 5.0 mV, V_O = 0 V)			—	+14	+13	
Large Signal Voltage Gain (V_O = –10 V to +10 V, R_L = 600 Ω)	6, 7	A_{VOL}				V/V
T_A = +25°C			50 k	200 k	—	
T_A = –40° to +85°C			25 k	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 10					V
(V_{CC} = +15 V, V_{EE} = –15 V)						
R_L = 300 Ω		V_{O+}	—	+12	—	
R_L = 300 Ω		V_{O-}	—	–12	—	
R_L = 600 Ω		V_{O+}	+12	+13.6	—	
R_L = 600 Ω		V_{O-}	—	–13	–12	
R_L = 2.0 kΩ		V_{O+}	+13	+14	—	
R_L = 2.0 kΩ		V_{O-}	—	–13.8	–13	
(V_{CC} = +2.5 V, V_{EE} = –2.5 V)						
R_L = 600 Ω		V_{O+}	1.1	1.6	—	
R_L = 600 Ω		V_{O-}	—	–1.6	–1.1	
Common Mode Rejection (V_{in} = ±13 V)	11	CMR	80	110	—	dB
Power Supply Rejection	12	PSR	80	110	—	dB
V_{CC}/V_{EE} = +15 V/ –15 V, +5.0 V/ –15 V, +15 V/ –5.0 V						
Output Short Circuit Current (V_{ID} = ±1.0 V, Output to Ground)	13, 14	I_{SC}				mA
Source (V_{CC} = 2.5 V to 15 V)			+50	+80	—	
Sink (V_{EE} = –2.5 V to –15 V)			–50	–100	—	
Power Supply Current (V_O = 0 V)	15	I_D				mA
(V_{CC} = 2.5 V, V_{EE} = –2.5 V to V_{CC} = +15 V, V_{EE} = –15 V)						
MC33178 (Dual)						
T_A = +25°C			—	—	1.4	
T_A = –40° to +85°C			—	—	1.6	
MC33179 (Quad)						
T_A = +25°C			—	1.7	2.4	
T_A = –40° to +85°C			—	—	2.6	

2

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0 V)	16, 31	SR	1.2	2.0	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	17	GBW	2.5	5.0	—	MHz
AC Voltage Gain (R_L = 600 Ω, V_O = 0 V, f = 20 kHz)	18, 19	A_{VO}	—	50	—	dB
Unity Gain Frequency (Open–Loop) (R_L = 600 Ω, C_L = 0 pF)		f_U	—	3.0	—	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	20, 22, 23	A_m	—	15	—	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	21, 22, 23	ϕ_m	—	60	—	Degrees
Channel Separation (f = 100 Hz to 20 kHz)	24	CS	—	−120	—	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 600 Ω, THD ≤ 1.0%)		BW_p	—	32	—	kHz
Distortion (R_L = 600 Ω,, V_O = 2.0 V_{pp}, A_V = +1.0 V) (f = 1.0 kHz) (f = 10 kHz) (f = 20 kHz)	25	THD	 — — —	 0.0024 0.014 0.024	 — — —	%
Open Loop Output Impedance (V_O = 0 V, f = 3.0 MHz, A_V = 10 V)	26	$\|Z_O\|$	—	150	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{in}	—	200	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}	—	10	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω,) f = 10 Hz f = 1.0 kHz	27	e_n	 — —	 8.0 7.5	 — —	nV/√Hz
Equivalent Input Noise Current f = 10 Hz f = 1.0 kHz	28	i_n	 — —	 0.33 0.15	 — —	pA/√Hz

Figure 1. Maximum Power Dissipation versus Temperature

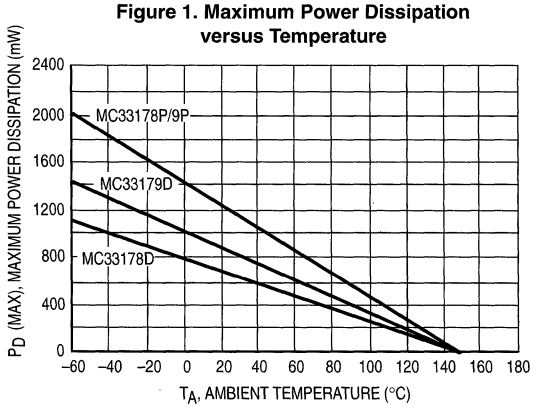


Figure 2. Input Offset Voltage versus Temperature for 3 Typical Units

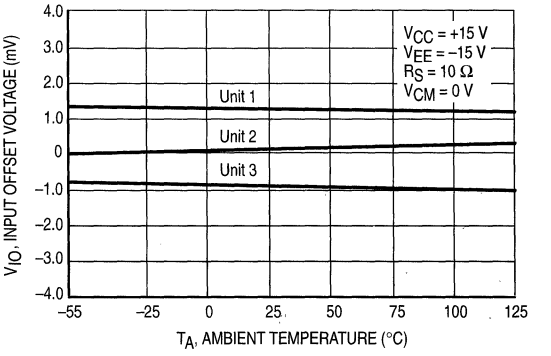


Figure 3. Input Bias Current versus Common Mode Voltage

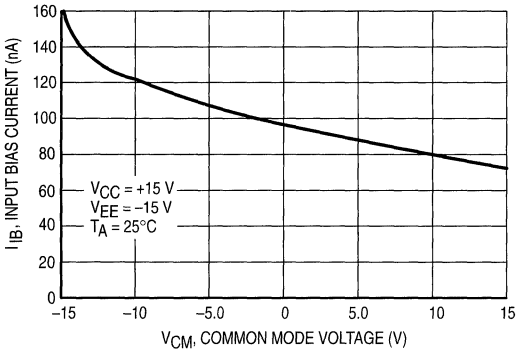


Figure 4. Input Bias Current versus Temperature

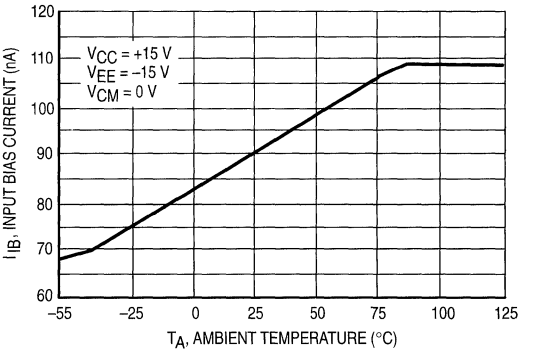


Figure 5. Input Common Mode Voltage Range versus Temperature

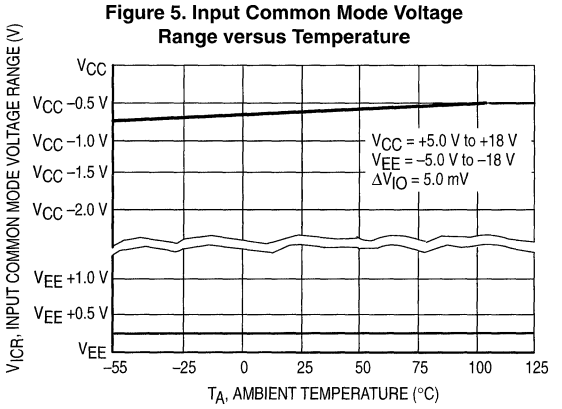


Figure 6. Open Loop Voltage Gain versus Temperature

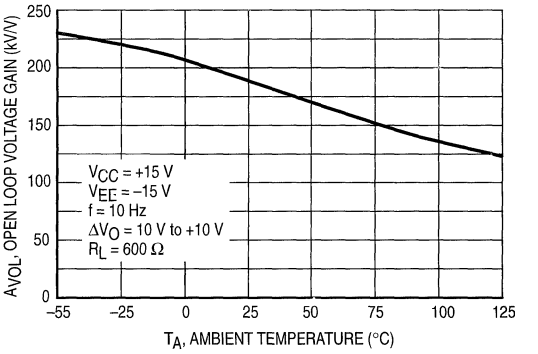


Figure 7. Voltage Gain and Phase versus Frequency

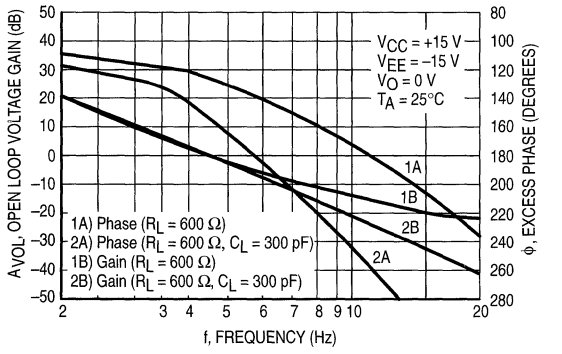
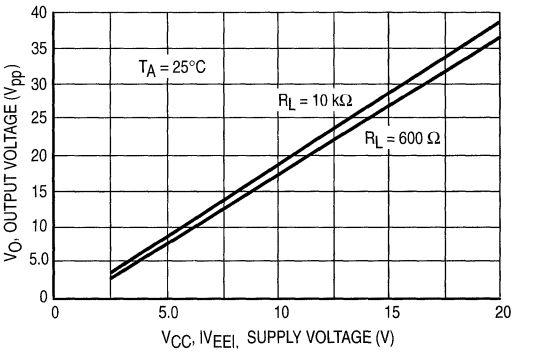


Figure 8. Output Voltage Swing versus Supply Voltage



2

Figure 9. Output Saturation Voltage versus Load Current

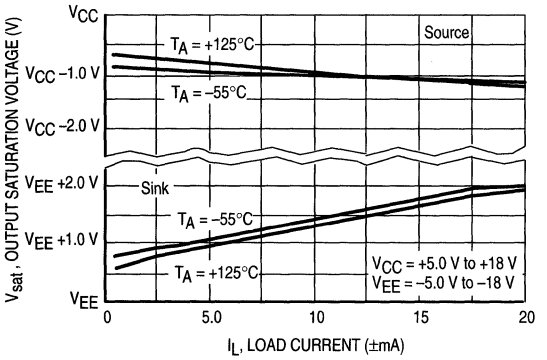


Figure 10. Output Voltage versus Frequency

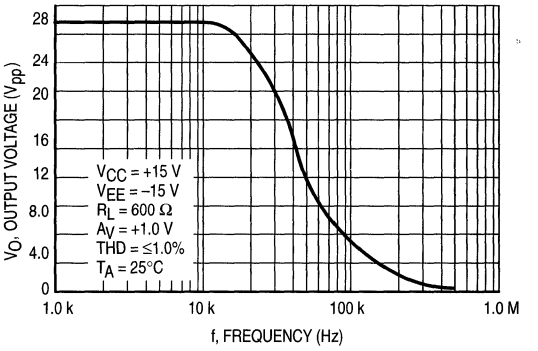


Figure 11. Common Mode Rejection versus Frequency Over Temperature

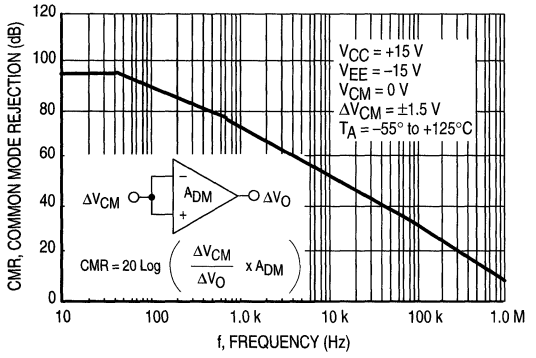


Figure 12. Power Supply Rejection versus Frequency Over Temperature

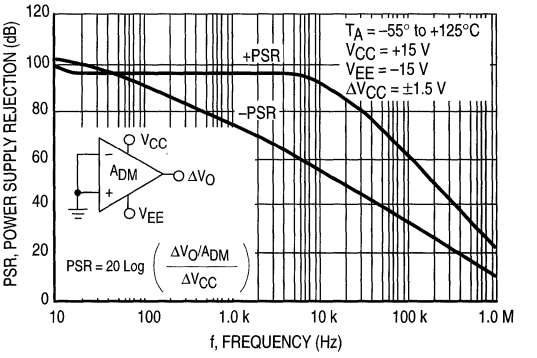


Figure 13. Output Short Circuit Current versus Output Voltage

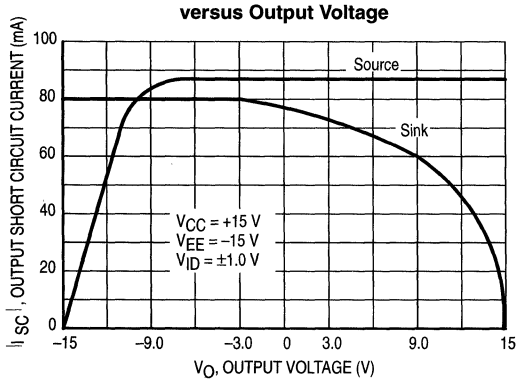


Figure 14. Output Short Circuit Current versus Temperature

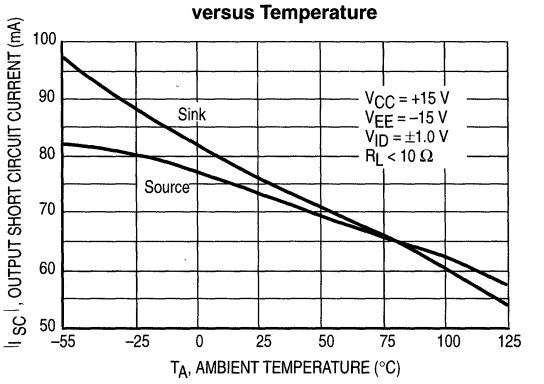


Figure 15. Supply Current versus Supply Voltage with No Load

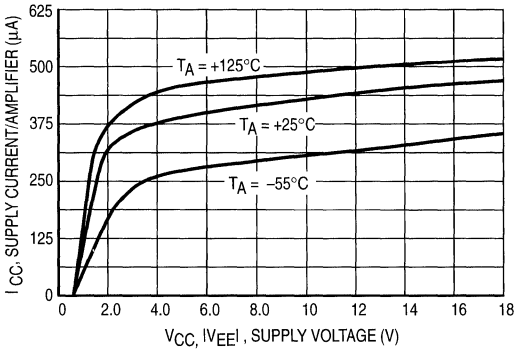


Figure 16. Normalized Slew Rate versus Temperature

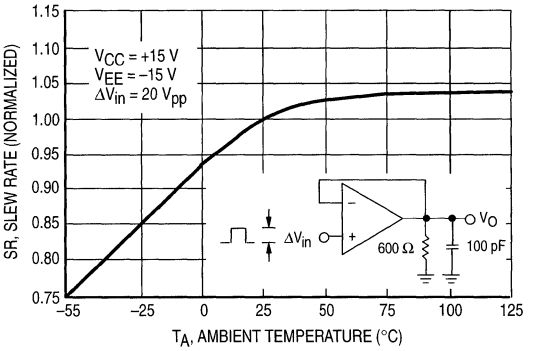


Figure 17. Gain Bandwidth Product versus Temperature

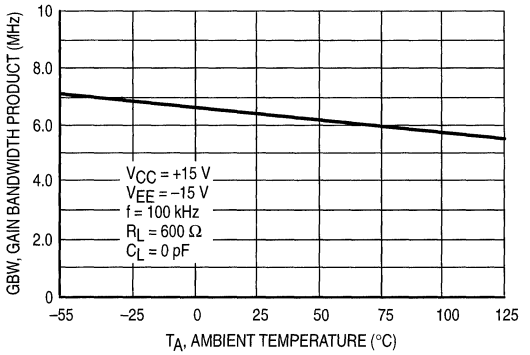


Figure 18. Voltage Gain and Phase versus Frequency

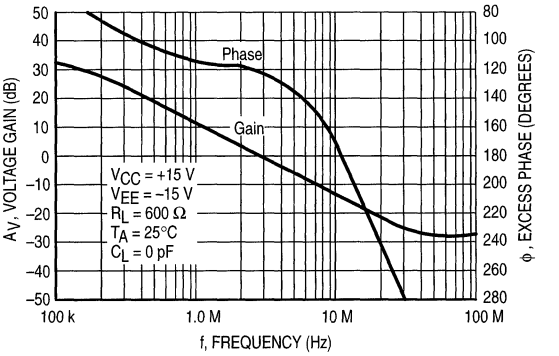


Figure 19. Voltage Gain and Phase versus Frequency

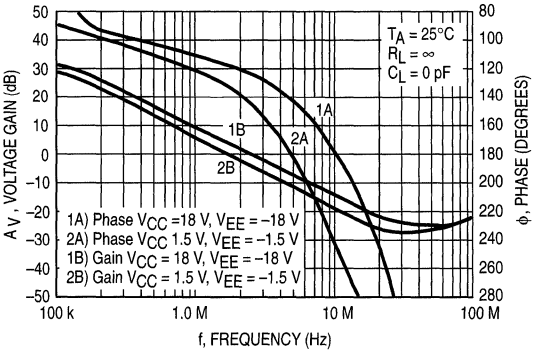
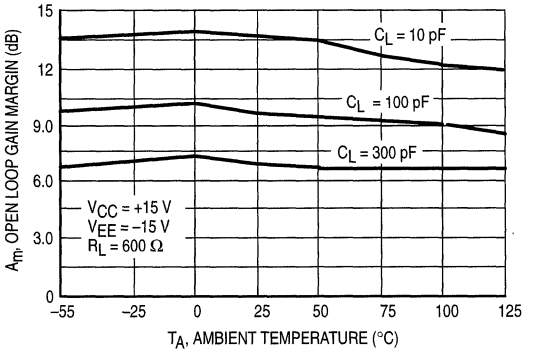


Figure 20. Open Loop Gain Margin versus Temperature



2

Figure 21. Phase Margin versus Temperature

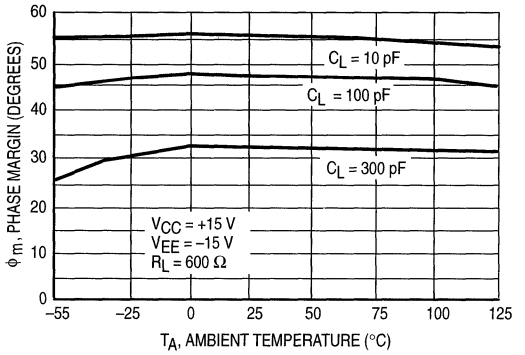


Figure 22. Phase Margin and Gain Margin versus Differential Source Resistance

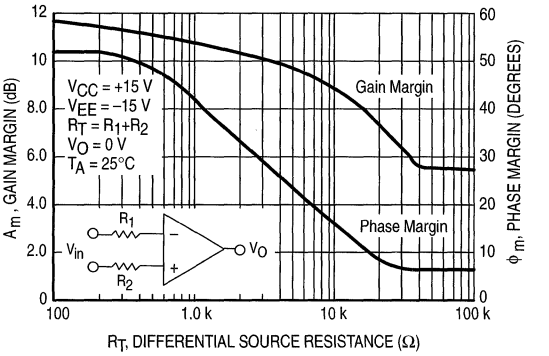


Figure 23. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

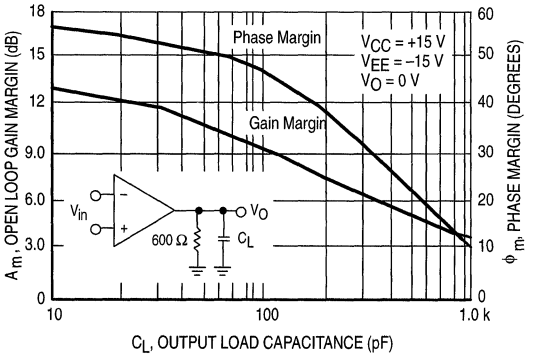


Figure 24. Channel Separation versus Frequency

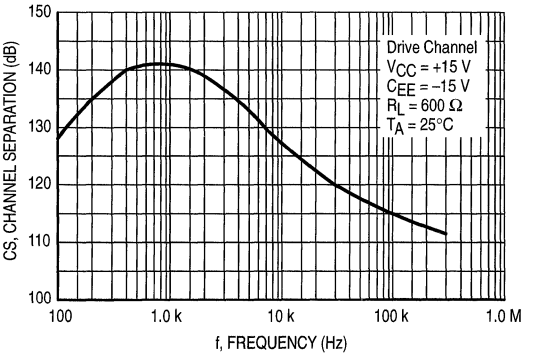


Figure 25. Total Harmonic Distortion versus Frequency

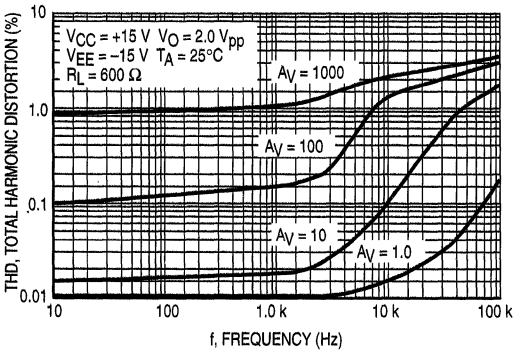


Figure 26. Output Impedance versus Frequency

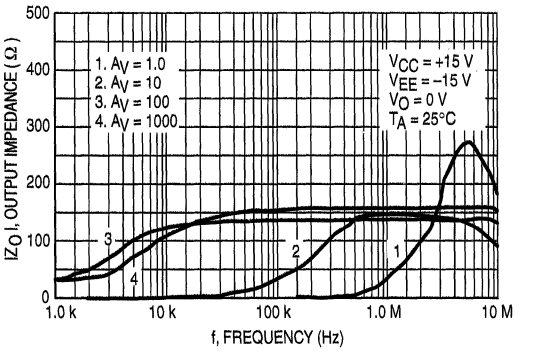


Figure 27. Input Referred Noise Voltage versus Frequency

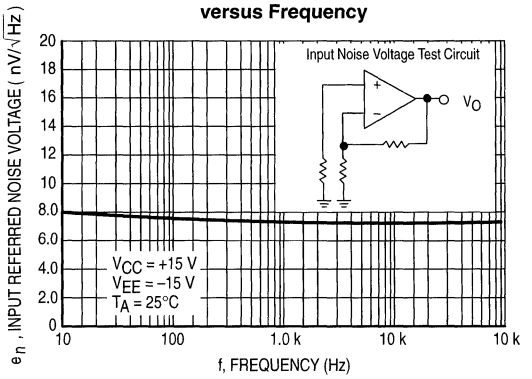


Figure 28. Input Referred Noise Current versus Frequency

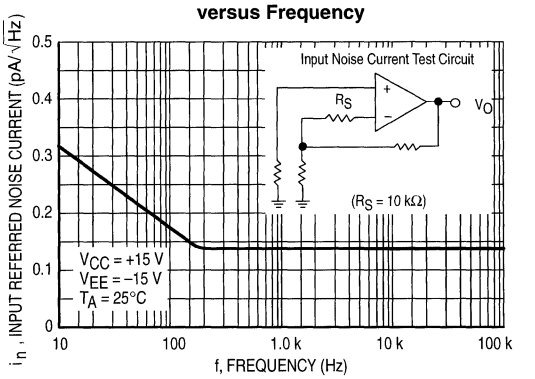


Figure 29. Percent Overshoot versus Load Capacitance

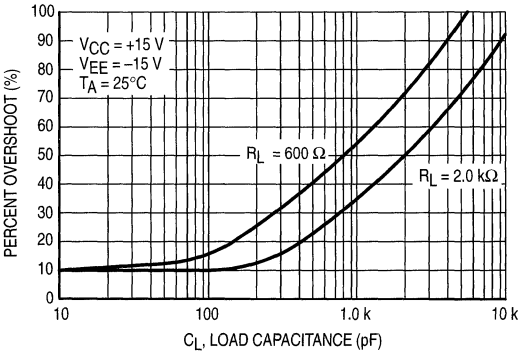


Figure 30. Noninverting Amplifier Slew Rate

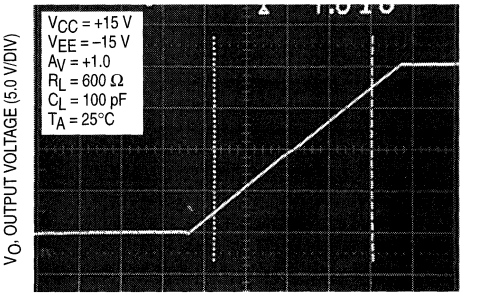


Figure 31. Small Signal Transient Response

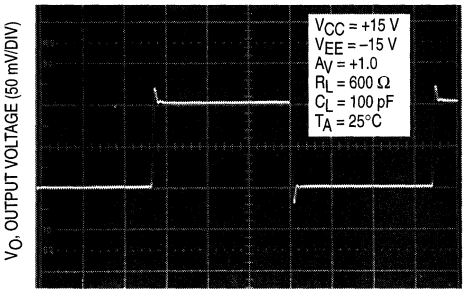
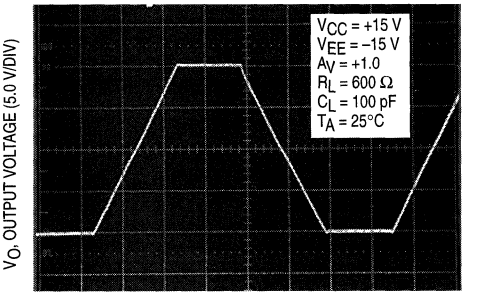
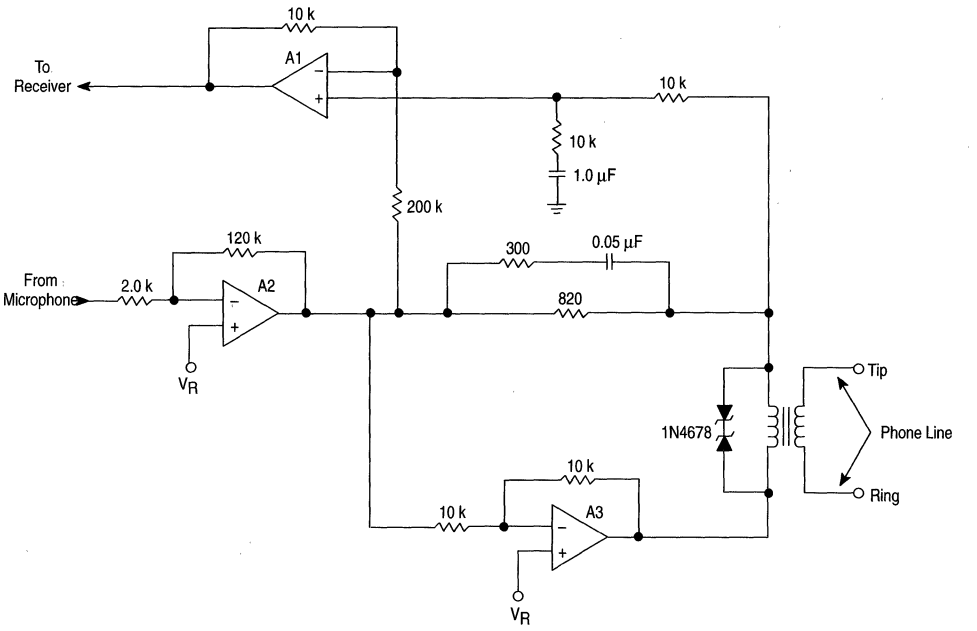


Figure 32. Large Signal Transient Response



2

Figure 33. Telephone Line Interface Circuit



APPLICATION INFORMATION

This unique device uses a boosted output stage to combine a high output current with a drain current lower than similar bipolar input op amps. Its 60° phase margin and 15 dB gain margin ensure stability with up to 1000 pF of load capacitance (see Figure 23). The ability to drive a minimum 600 Ω load makes it particularly suitable for telecom applications. Note that in the sample circuit in Figure 33 both A2 and A3 are driving equivalent loads of approximately 600 Ω.

The low input offset voltage and moderately high slew rate and gain bandwidth product make it attractive for a variety of other applications. For example, although it is not single supply (the common mode input range does not include ground), it is specified at +5.0 V with a typical common mode rejection of 110 dB. This makes it an excellent choice for use with digital circuits. The high common mode rejection, which is stable over temperature, coupled with a low noise figure and low distortion, is an ideal op amp for audio circuits.

The output stage of the op amp is current limited and therefore has a certain amount of protection in the event of a short circuit. However, because of its high current output, it is especially important not to allow the device to exceed the maximum junction temperature, particularly with the MC33179 (quad op amp). Shorting more than one amplifier could easily exceed the junction temperature to the extent of causing permanent damage.

Stability

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole frequency for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supplying decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

Additional stability problems can be caused by high load capacitances and/or a high source resistance. Simple compensation schemes can be used to alleviate these effects.

If a high source of resistance is used (R1 > 1.0 kΩ), a compensation capacitor equal to or greater than the input capacitance of the op amp (10 pF) placed across the feedback resistor (see Figure 34) can be used to neutralize that pole and prevent outer loop oscillation. Since the closed loop transient response will be a function of that capacitance, it is important to choose the optimum value for that capacitor. This can be determined by the following Equation:

$$C_C = (1 + [R1/R2])^2 \times C_L (Z_O/R_2) \quad (1)$$

where: Z_O is the output impedance of the op amp.

For moderately high capacitive loads (500 pF < C_L < 1500 pF) the addition of a compensation resistor on the order of 20 Ω between the output and the feedback loop will help to decrease miller loop oscillation (see Figure 35). For high capacitive loads (C_L > 1500 pF), a combined compensation scheme should be used (see Figure 36). Both the compensation resistor and the compensation capacitor affect the transient response and can be calculated for optimum performance. The value of C_C can be calculated using Equation (1). The Equation to calculate R_C is as follows:

$$R_C = Z_O \times R1/R2 \quad (2)$$

Figure 34. Compensation for High Source Impedance

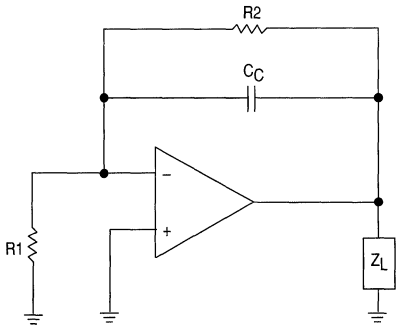


Figure 35. Compensation Circuit for Moderate Capacitive Loads

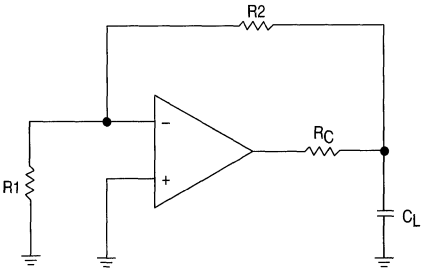
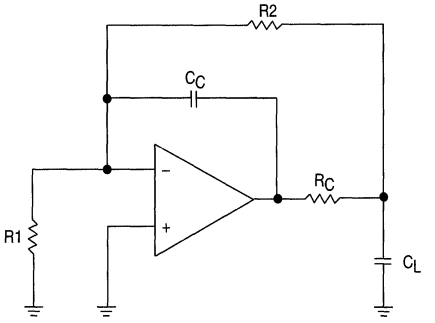


Figure 36. Compensation Circuit for High Capacitive Loads



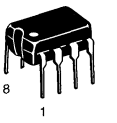
MC33201
MC33202
MC33204

LOW VOLTAGE RAIL–TO–RAIL OPERATIONAL AMPLIFIERS

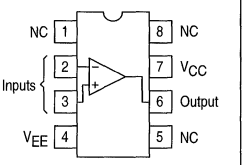
Rail-to-Rail Operational Amplifiers

The MC33201/2/4 family of operational amplifiers provide rail–to–rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail–to–rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (± 0.9 V) yet can operate with a supply of up to +12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

- Low Voltage, Single Supply Operation (+1.8 V and Ground to +12 V and Ground)
- Input Voltage Range Includes both Supply Rails
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over–driven Input Signals
- High Output Current (I_{SC} = 80 mA, Typ)
- Low Supply Current (I_D = 0.9 mA, Typ)
- 600 Ω Output Drive Capability
- Extended Operating Temperature Ranges (–40° to +105°C and –55° to +125°C)
- Typical Gain Bandwidth Product = 2.2 MHz
- Offered in New TSSOP Package Including Standard SOIC and DIP Packages

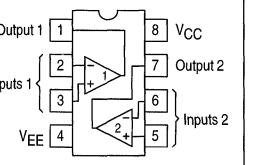


P SUFFIX
PLASTIC PACKAGE
CASE 626

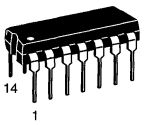


(Single, Top View)

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



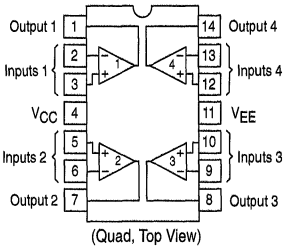
(Dual, Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

DTB SUFFIX
PLASTIC PACKAGE
CASE 948G
(TSSOP–14)



(Quad, Top View)

ORDERING INFORMATION

Operational Amplifier Function	Device	Operating Temperature Range	Package
Single	MC33201D	T_A= –40 ° to +105°C	SO–8
	MC33201P		Plastic DIP
	MC33201VD	T_A = –55 ° to +125°C	SO–8
	MC33201VP		Plastic DIP
Dual	MC33202D	T_A= –40 ° to +105°C	SO–8
	MC33202P		Plastic DIP
	MC33202VD	T_A = –55 ° to +125°C	SO–8
	MC33202VP		Plastic DIP
Quad	MC33204D	T_A= –40 ° to +105°C	SO–14
	MC33204DTB		TSSOP–14
	MC33204P		Plastic DIP
	MC33204VD	T_A = –55 ° to +125°C	SO–14
	MC33204VDTB		TSSOP–14
	MC33204VP		Plastic DIP

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	V_{CC} = 2.0 V	V_{CC} = 3.3 V	V_{CC} = 5.0 V	Unit
Input Offset Voltage V_{IO} (max) MC33201 MC33202 MC33204	 ±8.0 ±10 ±12	 ±8.0 ±10 ±12	 ±6.0 ±8.0 ±10	mV
Output Voltage Swing V_{OH} (R_L = 10 kΩ) V_{OL} (R_L = 10 kΩ)	 1.9 0.10	 3.15 0.15	 4.85 0.15	 V_{min} V_{max}
Power Supply Current per Amplifier (I_D)	 1.125	 1.125	 1.125	mA

Specifications at V_{CC} = 3.3 V are guaranteed by the 2.0 V and 5.0 V tests. V_{EE} = Gnd.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+13	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Common Mode Input Voltage Range (Note 2)	V_{CM}	V_{CC} + 0.5 V to V_{EE} − 0.5 V	V
Output Short Circuit Duration	t_s	(Note 3)	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	− 65 to +150	°C
Maximum Power Dissipation	P_D	(Note 3)	mW

NOTES: 1. The differential input voltage of each amplifier is limited by two internal parallel back–to–back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
2. The input common mode voltage range is limited by internal diodes connected from the inputs to both supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 2)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} 0 V to 0.5 V, V_{CM} 1.0 V to 5.0 V)	3	$\|V_{IO}\|$				mV
MC33201: T_A = + 25°C			–	–	6.0	
T_A = − 40° to +105°C			–	–	9.0	
T_A = − 55° to +125°C			–	–	13	
MC33202: T_A = + 25°C			–	–	8.0	
T_A = − 40° to +105°C			–	–	11	
T_A = − 55° to +125°C			–	–	14	
MC33204: T_A = + 25°C			–	–	10	
T_A = − 40° to +105°C			–	–	13	
T_A = − 55° to +125°C			–	–	17	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω)	4	$\Delta V_{IO}/\Delta T$				μV/°C
T_A = − 40° to +105°C			–	2.0	–	
T_A = − 55° to +125°C			–	2.0	–	
Input Bias Current (V_{CM} = 0 V to 0.5 V, V_{CM} = 1.0 V to 5.0 V)	5, 6	$\|I_{IB}\|$				nA
T_A = + 25°C			–	80	200	
T_A = − 40° to +105°C			–	100	250	
T_A = − 55° to +125°C			–	–	500	
Input Offset Current (V_{CM} = 0 V to 0.5 V, V_{CM} = 1.0 V to 5.0 V)	–	$\|I_{IO}\|$				nA
T_A = + 25°C			–	5.0	50	
T_A = − 40° to +105°C			–	10	100	
T_A = − 55° to +125°C			–	–	200	
Common Mode Input Voltage Range	–	V_{ICR}	V_{EE}	–	V_{CC}	V

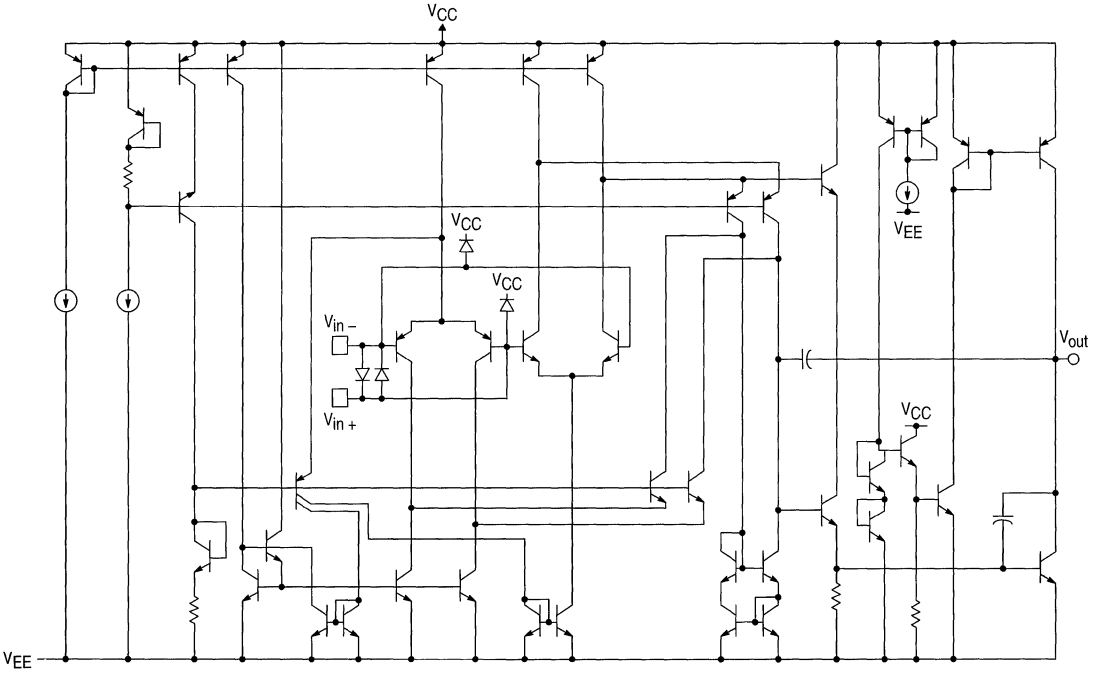
DC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Large Signal Voltage Gain (V_{CC} = + 5.0 V, V_{EE} = – 5.0 V) R_L = 10 kΩ R_L = 600 Ω	7	A_{VOL}	 50 25	 300 250	 – –	kV/V
Output Voltage Swing (V_{ID} = ± 0.2 V) R_L = 10 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 600 Ω	8, 9, 10	 V_{OH} V_{OL} V_{OH} V_{OL}	 4.85 – 4.75 –	 4.95 0.05 4.85 0.15	 – 0.15 – 0.25	V
Common Mode Rejection (V_{in} = 0 V to 5.0 V)	11	CMR	60	90	–	dB
Power Supply Rejection Ratio V_{CC}/V_{EE} = 5.0 V/Gnd to 3.0 V/Gnd	12	PSRR	 500	 25	 –	μV/V
Output Short Circuit Current (Source and Sink)	13, 14	I_{SC}	50	80	–	mA
Power Supply Current per Amplifier (V_O = 0 V) T_A = – 40° to +105°C T_A = – 55° to +125°C	15	I_D	 – –	 0.9 0.9	 1.125 1.125	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_S = ± 2.5 V, V_O = – 2.0 V to + 2.0 V, R_L = 2.0 kΩ, A_V = +1.0)	16, 26	SR	 0.5	 1.0	 –	V/μs
Gain Bandwidth Product (f = 100 kHz)	17	GBW	–	2.2	–	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	20, 21, 22	A_M	–	12	–	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	20, 21, 22	ϕ_M	–	65	–	Deg
Channel Separation (f = 1.0 Hz to 20 kHz, A_V = 100)	23	CS	–	90	–	dB
Power Bandwidth (V_O = 4.0 V_{pp}, R_L = 600 Ω, THD ≤ 1 %)		BW_P	–	28	–	kHz
Total Harmonic Distortion (R_L = 600 Ω, V_O = 1.0 V_{pp}, A_V = 1.0) f = 1.0 kHz f = 10 kHz	24	THD	 – –	 0.002 0.008	 – –	%
Open Loop Output Impedance (V_O = 0 V, f = 2.0 MHz, A_V = 10)		$\lvert Z_O \rvert$	 –	 100	 –	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{in}	–	200	–	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}	–	8.0	–	pF
Equivalent Input Noise Voltage (R_S = 100 Ω) f = 10 Hz f = 1.0 kHz	25	e_n	 – –	 25 20	 – –	$\frac{nV}{\sqrt{Hz}}$
Equivalent Input Noise Current f = 10 Hz f = 1.0 kHz	25	i_n	 – –	 0.8 0.2	 – –	$\frac{pA}{\sqrt{Hz}}$

Figure 1. Circuit Schematic
(Each Amplifier)



This device contains 70 active transistors (each amplifier).

2

Figure 2. Maximum Power Dissipation versus Temperature

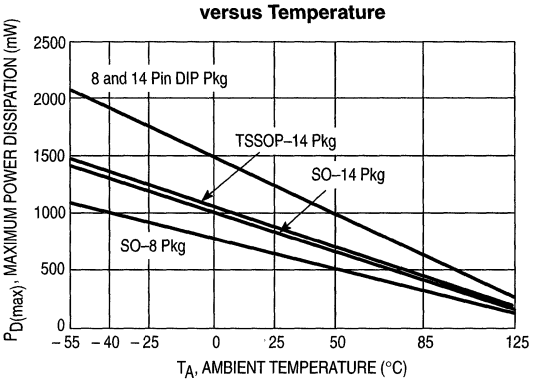


Figure 3. Input Offset Voltage Distribution

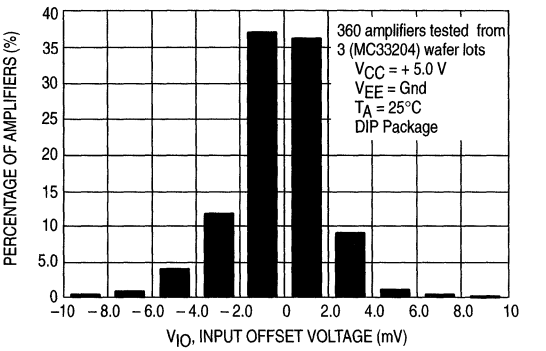


Figure 4. Input Offset Voltage Temperature Coefficient Distribution

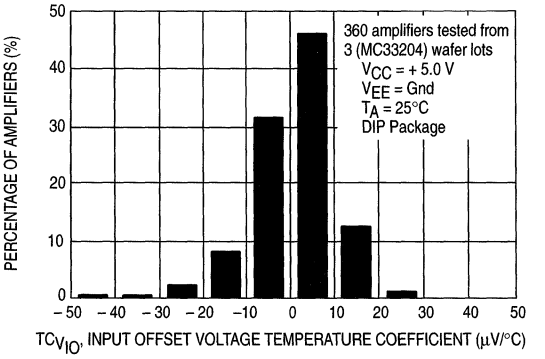


Figure 5. Input Bias Current versus Temperature

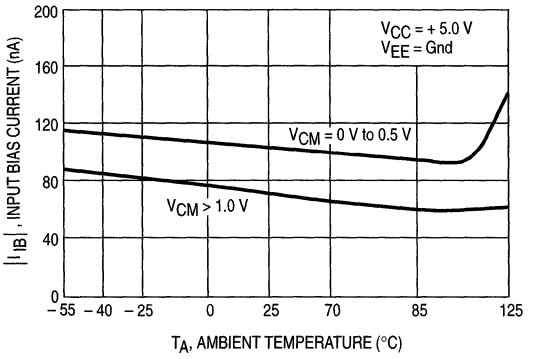


Figure 6. Input Bias Current versus Common Mode Voltage

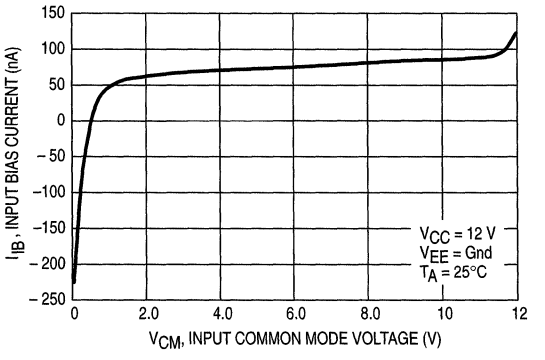


Figure 7. Open Loop Voltage Gain versus Temperature

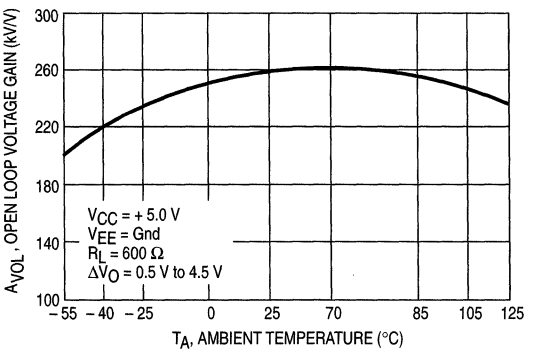


Figure 8. Output Voltage Swing versus Supply Voltage

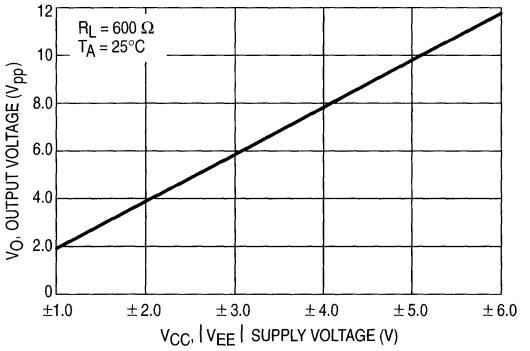


Figure 9. Output Saturation Voltage versus Load Current

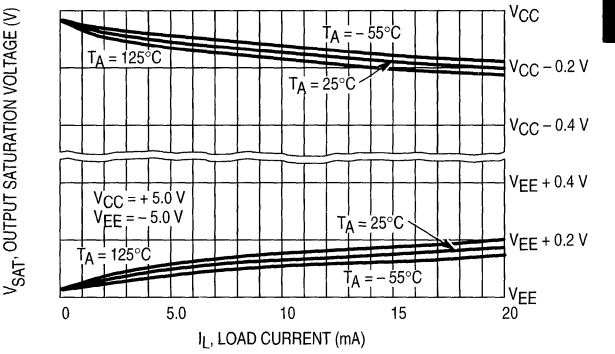


Figure 10. Output Voltage versus Frequency

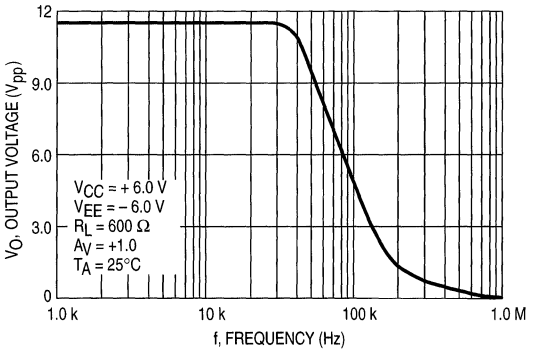


Figure 11. Common Mode Rejection versus Frequency

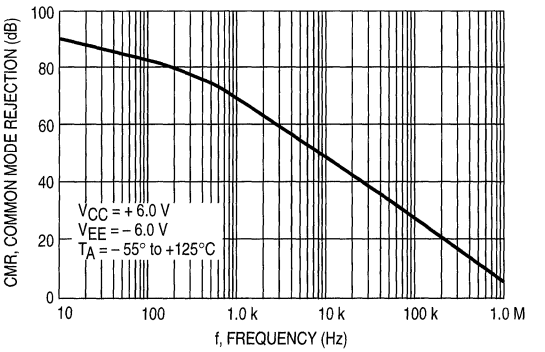


Figure 12. Power Supply Rejection versus Frequency

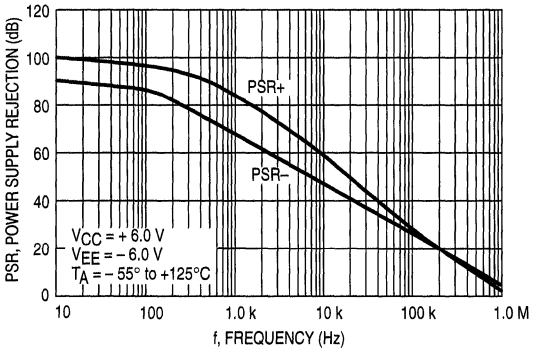
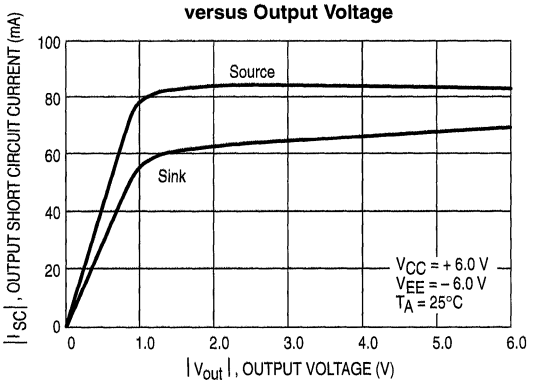


Figure 13. Output Short Circuit Current versus Output Voltage



2

Figure 14. Output Short Circuit Current versus Temperature

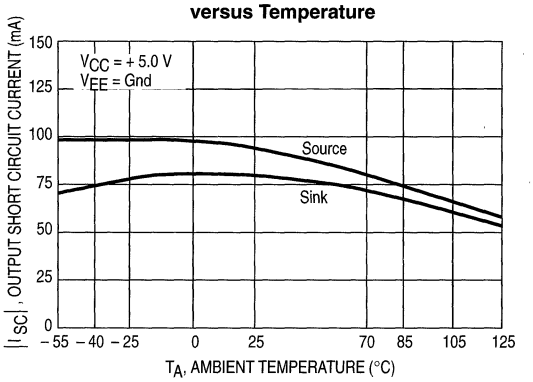


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

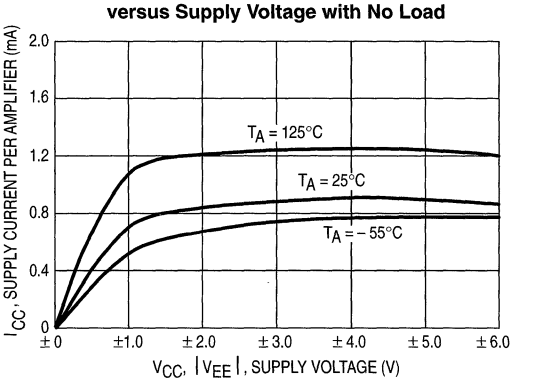


Figure 16. Slew Rate versus Temperature

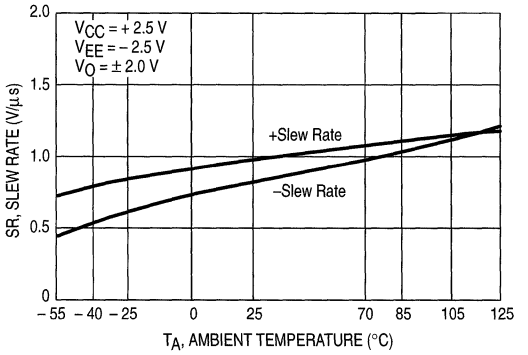


Figure 17. Gain Bandwidth Product versus Temperature

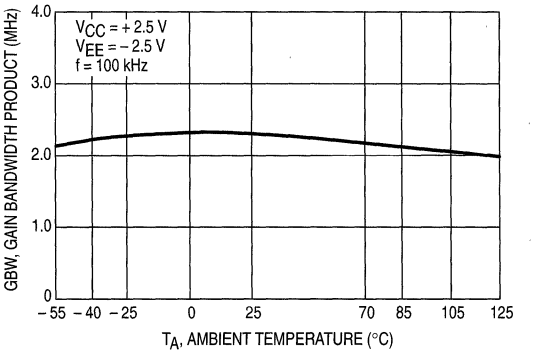


Figure 18. Voltage Gain and Phase versus Frequency

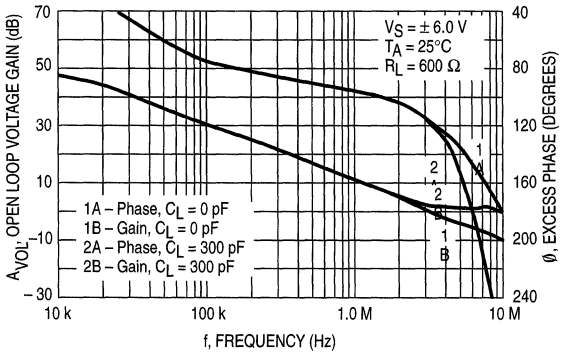


Figure 19. Voltage Gain and Phase versus Frequency

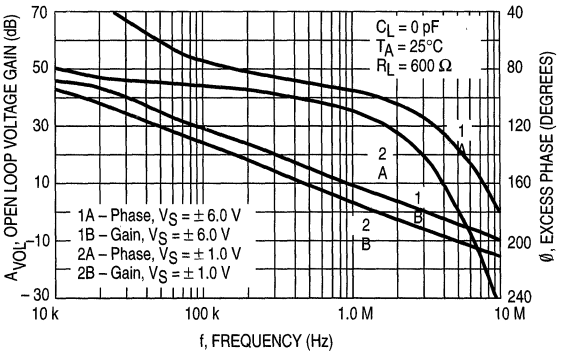


Figure 20. Gain and Phase Margin versus Temperature

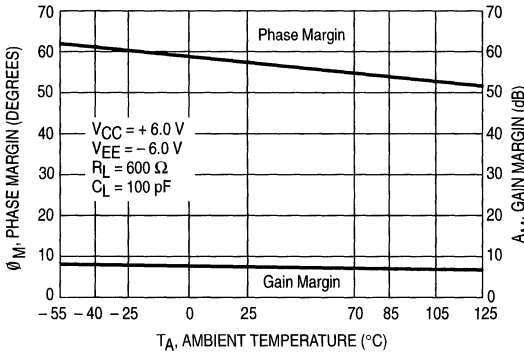


Figure 21. Gain and Phase Margin versus Differential Source Resistance

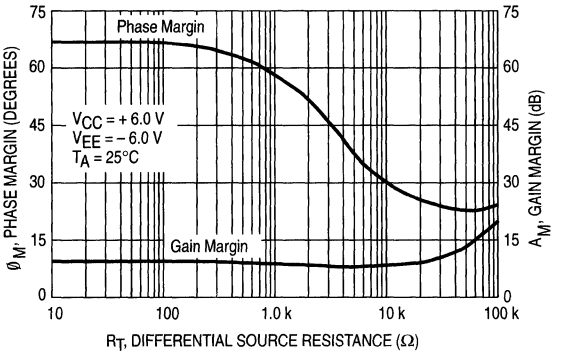


Figure 22. Gain and Phase Margin versus Capacitive Load

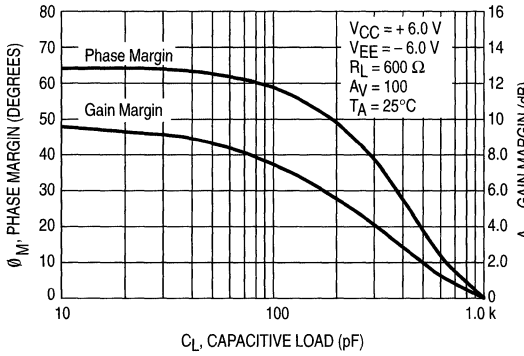


Figure 23. Channel Separation versus Frequency

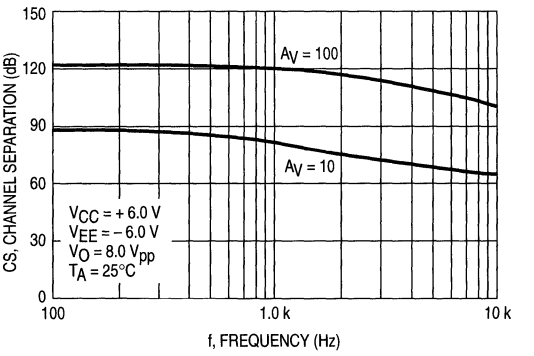


Figure 24. Total Harmonic Distortion versus Frequency

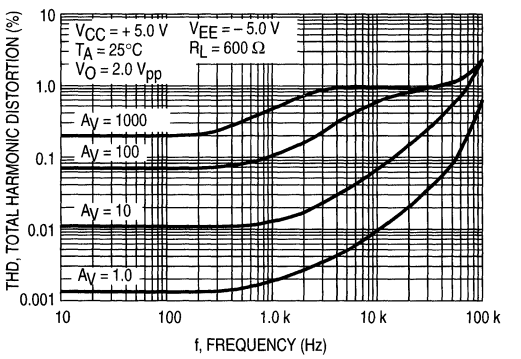
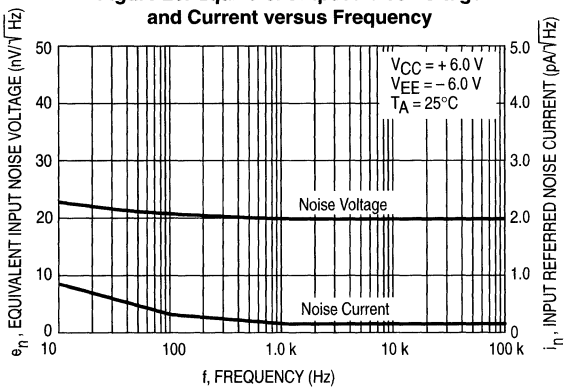


Figure 25. Equivalent Input Noise Voltage and Current versus Frequency



General Information

The MC33201/2/4 family of operational amplifiers are unique in their ability to swing rail–to–rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies. The MC33201/2/4 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

Circuit Information

Rail–to–rail performance is achieved at the input of the amplifiers by using parallel NPN–PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than V_{EE}, the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.

In addition to its rail–to–rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600 Ω loads. Because of this high output current capability, care should be taken not to exceed the 150°C maximum junction temperature.

Figure 26. Noninverting Amplifier Slew Rate

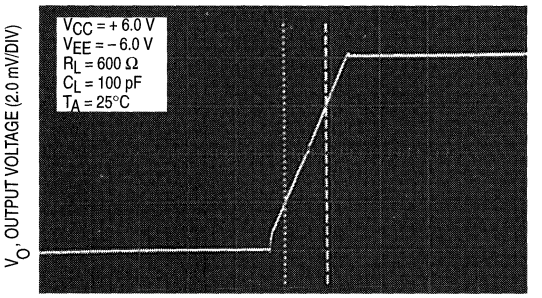


Figure 27. Small Signal Transient Response

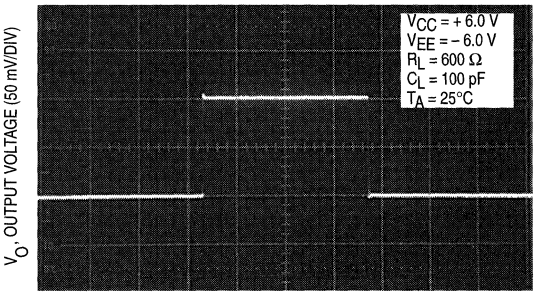
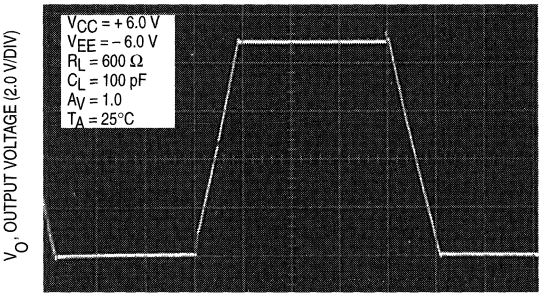


Figure 28. Large Signal Transient Response



MC33206
MC33207

Advance Information

Rail-To-Rail Operational Amplifiers with Enable Feature

LOW VOLTAGE RAIL–TO–RAIL OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

The MC33206/7 family of operational amplifiers provide rail–to–rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs and the output can swing within 50 mV of each rail. This rail–to–rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (±0.9 V) yet can operate with a single supply of up to 12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum.

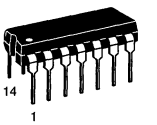
The MC33206/7 has an enable mode that can be controlled externally. The typical supply current in the standby mode is <1.0 μA (V_{Enable} = Gnd). The addition of an enable function makes this amplifier an ideal choice for power sensitive applications, battery powered equipment (instrumentation and monitoring), portable telecommunication, and sample–and–hold applications.

- Standby Mode (I_D ≤1.0 μA, Typ)
- Low Voltage, Single Supply Operation (1.8 V and Ground to 12 V and Ground)
- Rail–to–Rail Input Common Mode Voltage Range
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over–Driven Input Signals
- High Output Current (I_{SC} = 80 mA, Typ)
- Low Supply Current (I_D = 0.9 mA, Typ)
- 600 Ω Output Drive Capability
- Typical Gain Bandwidth Product = 2.2 MHz

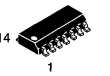
ORDERING INFORMATION

Operational Amplifier Function	Device	Operating Temperature Range	Package
Dual	MC33206D	T_A= –40 ° to +105°C	SO–14
	MC33206P		Plastic DIP
Quad	MC33207D		SO–16
	MC33207P		Plastic DIP

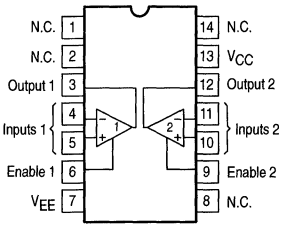
MC33206



P SUFFIX
PLASTIC PACKAGE
CASE 646

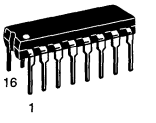


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

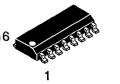


(Dual, Top View)

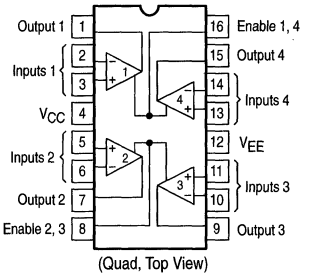
MC33207



P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



(Quad, Top View)

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	13	V
ESD Protection Voltage at any Pin Human Body Model	V_{ESD}	2,000	V
Voltage at any Device Pin	V_{DP}	$V_S \pm 0.5$	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Common Mode Input Voltage Range (Note 2)	V_{CM}	V_{CC} + 0.5 to V_{EE} – 0.5	V
Output Short Circuit Duration (Note 3)	t_s	(Note 3)	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Maximum Power Dissipation	P_D	(Note 3)	mW

NOTES: 1. The differential input voltage of each amplifier is limited by two internal parallel back–to–back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
2. The common–mode input voltage range of each amplifier is limited by diodes connected from the inputs to both power supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
4. ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{Enable} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} 0 to 0.5 V, V_{CM} 1.0 to 5.0 V)	–	V_{IO}				mV
MC33206: T_A = 25°C			–	0.5	8.0	
T_A = –40° to +105°C			–	1.0	11	
MC33207: T_A = 25°C			–	0.5	10	
T_A = –40° to +105°C			–	1.0	13	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω) T_A = –40° to +105°C	–	$\Delta V_{IO}/\Delta T$	–	2.0	–	µV/°C
Input Bias Current (V_{CM} = 0 to 0.5 V, V_{CM} = 1.0 to 5.0 V)	–	$\lvert I_{IB} \rvert$				nA
T_A = 25°C			–	80	200	
T_A = –40° to +105°C			–	100	250	
Input Offset Current (V_{CM} = 0 to 0.5 V, V_{CM} = 1.0 to 5.0 V)	–	$\lvert I_{IO} \rvert$				nA
T_A = 25°C			–	5.0	50	
T_A = –40° to +105°C			–	10	100	
Common Mode Input Voltage Range	–	V_{ICR}	–	V_{CC} + 0.2	V_{CC}	V
			V_{EE}	V_{EE} – 0.2	–	
Large Signal Voltage Gain (V_{CC} = 5.0 V, V_{EE} = –5.0 V)	–	A_{VOL}				kV/V
R_L = 10 kΩ			50	300	–	
R_L = 600 Ω			25	250	–	
Output Voltage Swing (V_{ID} = ±0.2 V)	–					V
R_L = 10 kΩ		V_{OH}	4.85	4.95	–	
R_L = 10 kΩ		V_{OL}	–	0.05	0.15	
R_L = 600 Ω		V_{OH}	4.75	4.85	–	
R_L = 600 Ω		V_{OL}	–	0.15	0.25	
Common Mode Rejection (V_{in} = 0 to 5.0 V)	–	CMR	60	90	–	dB
Power Supply Rejection Ratio	–	PSRR	–	25	500	µV/V
V_{CC}/V_{EE} = 5.0 V/Gnd to 3.0 V/Gnd		PSR	66	92	–	dB
Output Short Circuit Current (Source and Sink)	–	I_{SC}	50	80	–	mA

DC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{Enable} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Power Supply Current (V_O = 2.5 V, T_A = −40° to +105°C, per Amplifier)	–	I_D				
MC33206: V_{Enable} = 5.0 Vdc			–	0.8	1.125	mA
V_{Enable} = Gnd (Standby)			–	0.5	6.0	μA
MC33207: V_{Enable} = 5.0 Vdc			–	1.5	2.25	mA
V_{Enable} = Gnd (Standby)			–	0.5	6.0	μA
Enable Input Voltage (per Amplifier)	–	V_{Enable}				V
Enabled – Amplifier "On"			–	V_{EE} + 1.8	–	
Disabled – Amplifier "Off" (Standby)			–	V_{EE} + 0.3	–	
Enable Input Current (Note 5) (per Amplifier)	–	I_{Enable}				μA
V_{Enable} = 12 V			–	2.5	–	
V_{Enable} = 5.0 V			–	2.2	–	
V_{Enable} = 1.8 V			–	0.8	–	
V_{Enable} = Gnd			–	0	–	

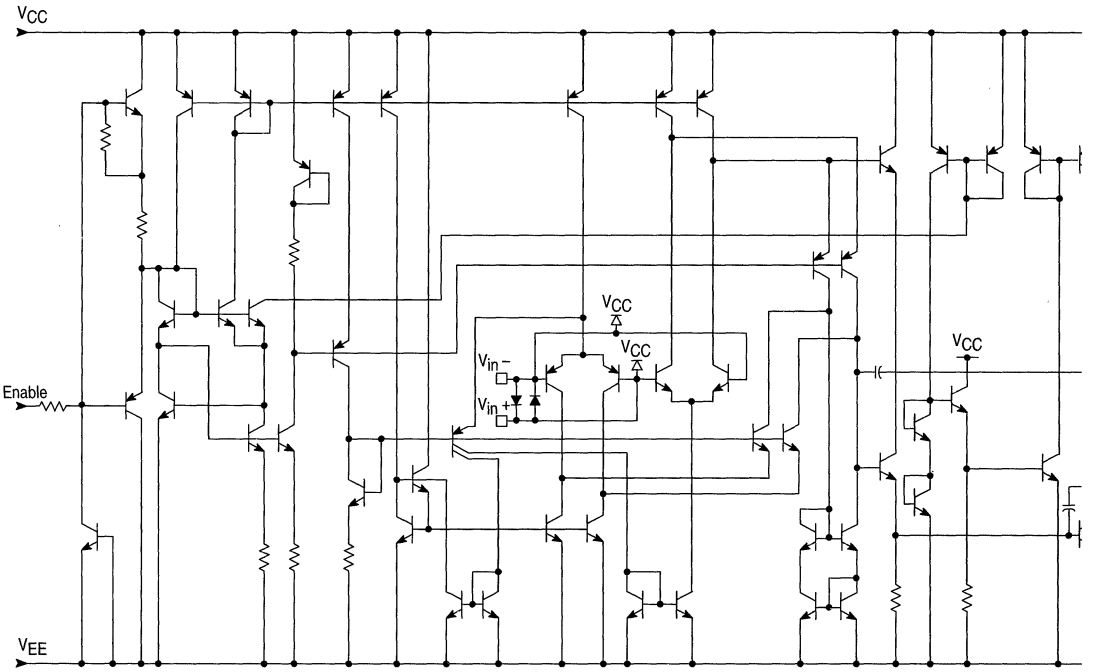
NOTE: 5. External control circuitry must provide for an initial turn–off transient of <10 μA.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{Enable} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_S = ±2.5 V, V_O = −2.0 to +2.0 V, R_L = 2.0 kΩ, A_V = 1.0)	–	SR	0.5	1.0	–	V/μs
Gain Bandwidth Product (f = 100 kHz)	–	GBW	–	2.2	–	MHz
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	–	ϕ_M	–	65	–	Deg
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	–	A_M	–	12	–	dB
Channel Separation (f = 1.0 Hz to 20 kHz, A_V = 100)	–	CS	–	90	–	dB
Power Bandwidth (V_O = 4.0 Vpp, R_L = 600 Ω, THD ≤ 1%)	–	BW_P	–	28	–	kHz
Total Harmonic Distortion (R_L = 600 Ω, V_O = 1.0 Vpp, A_V = 1.0)	–	THD				%
f = 1.0 kHz			–	0.002	–	
f = 10 kHz			–	0.008	–	
Open Loop Output Impedance (V_O = 0 V, f = 2.0 MHz, A_V = 10)	–	$\|Z_O\|$	–	100	–	Ω
Differential Input Resistance (V_{CM} = 0 V)	–	R_{in}	–	200	–	kΩ
Differential Input Capacitance (V_{CM} = 0 V)	–	C_{in}	–	8.0	–	pF
Equivalent Input Noise Voltage (R_S = 100 Ω)	–	e_n				$\frac{nV}{\sqrt{Hz}}$
f = 10 Hz			–	25	–	
f = 1.0 kHz			–	20	–	
Equivalent Input Noise Current	–	i_n				$\frac{pA}{\sqrt{Hz}}$
f = 10 Hz			–	0.8	–	
f = 1.0 kHz			–	0.2	–	
Time Delay for Device to Turn On	–	t_{on}	–	10	–	μs
Time Delay for Device to Turn Off	–	t_{off}	–	2.0	–	μs

2

Figure 1. Circuit Schematic
(Each Amplifier)



This device contains 96 active transistors (each amplifier).

Figure 2. Maximum Power Dissipation versus Temperature

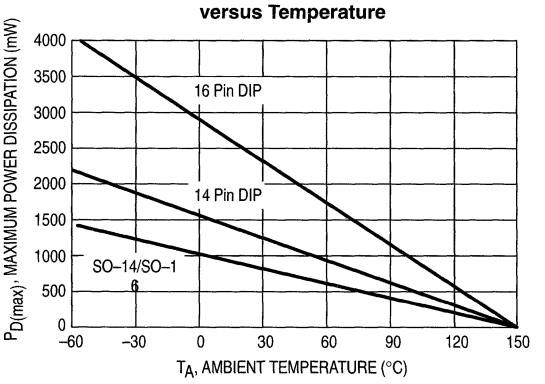


Figure 3. Input Offset Voltage Distribution

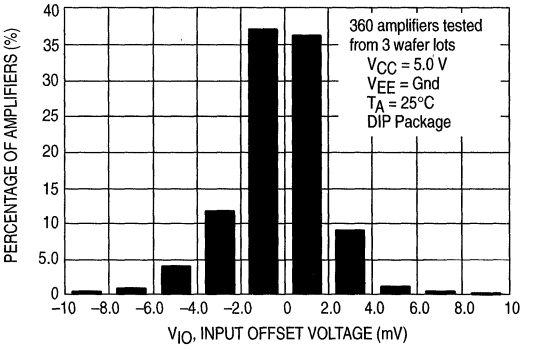


Figure 4. Input Offset Voltage Temperature Coefficient Distribution

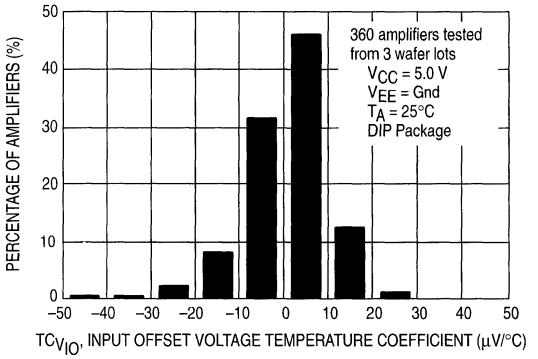


Figure 5. Input Bias Current versus Temperature

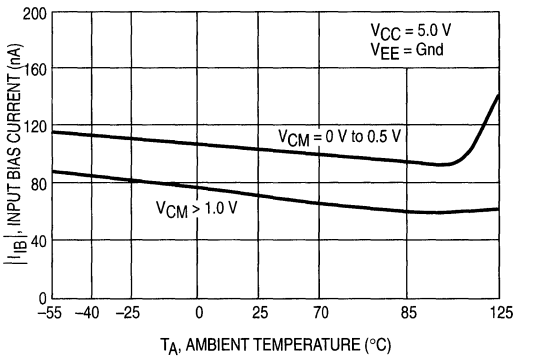


Figure 6. Input Bias Current versus Common Mode Voltage

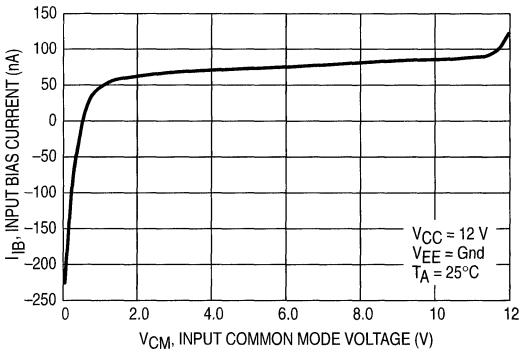


Figure 7. Open Loop Voltage Gain versus Temperature

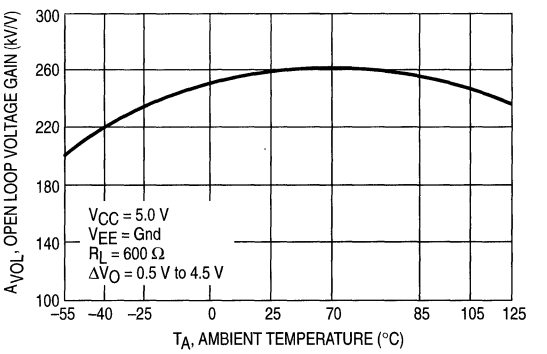


Figure 8. Output Voltage Swing versus Supply Voltage

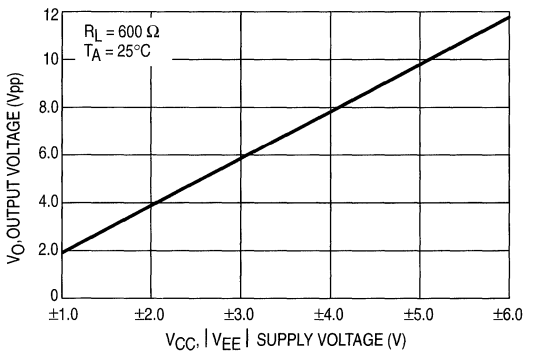
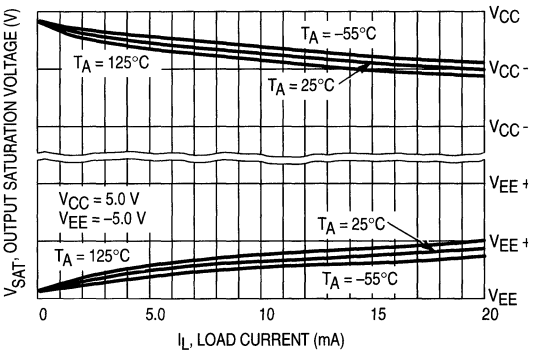


Figure 9. Output Saturation Voltage versus Load Current



2

Figure 10. Output Voltage versus Frequency

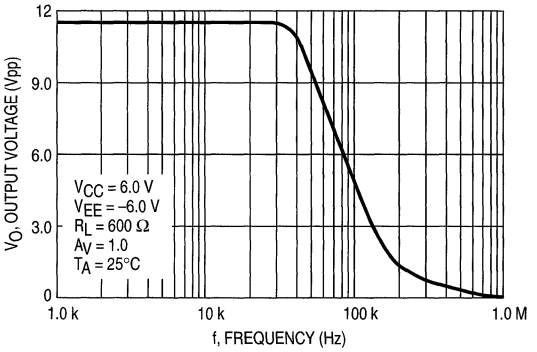


Figure 11. Common Mode Rejection versus Frequency

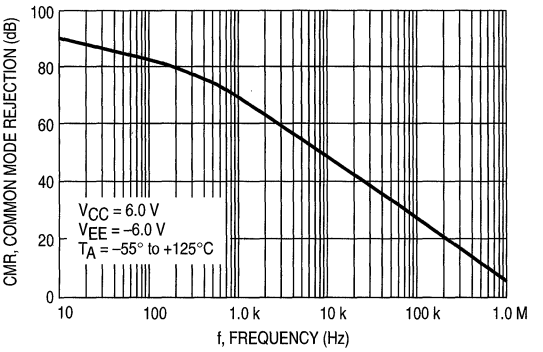


Figure 12. Power Supply Rejection versus Frequency

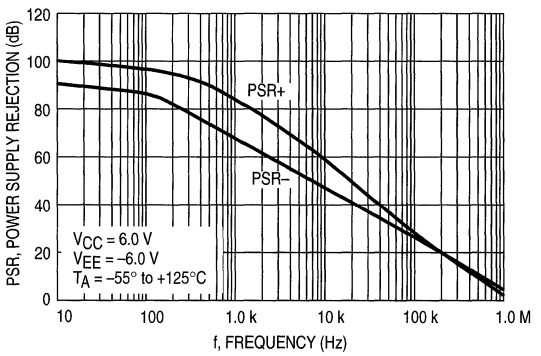


Figure 13. Output Short Circuit Current versus Output Voltage

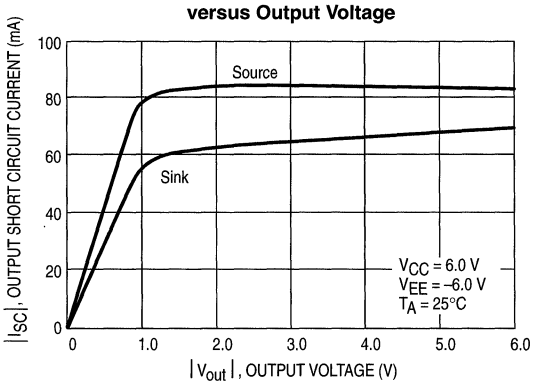


Figure 14. Output Short Circuit Current versus Temperature

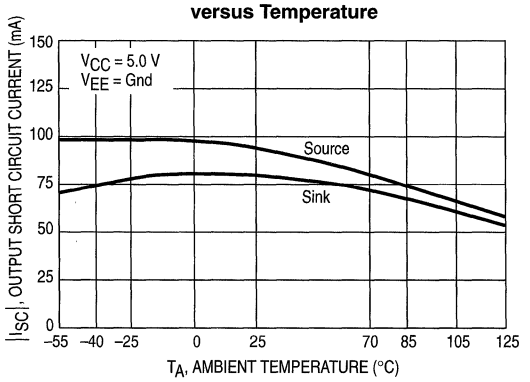


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

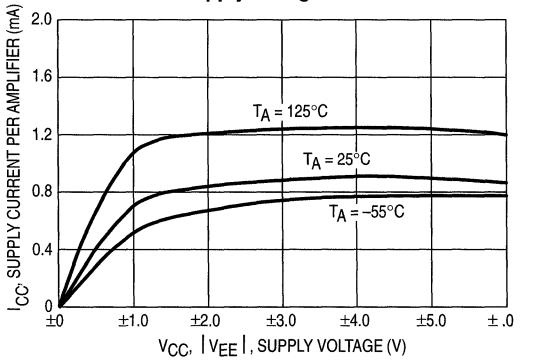


Figure 16. Slew Rate versus Temperature

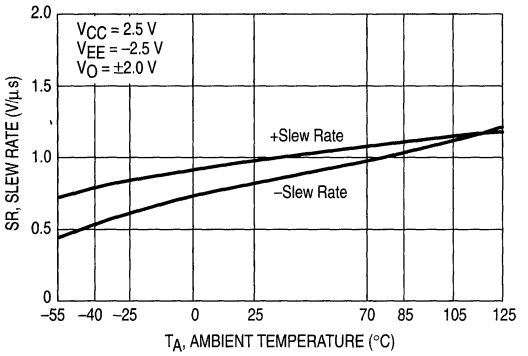


Figure 17. Gain Bandwidth Product versus Temperature

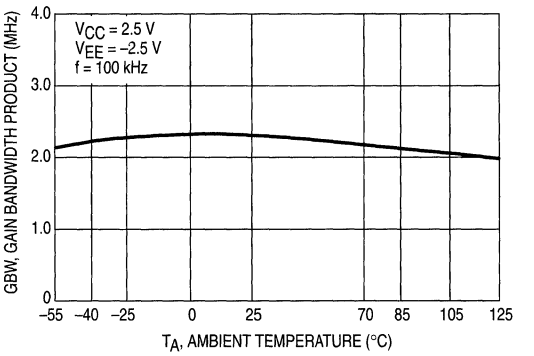


Figure 18. Voltage Gain and Phase versus Frequency

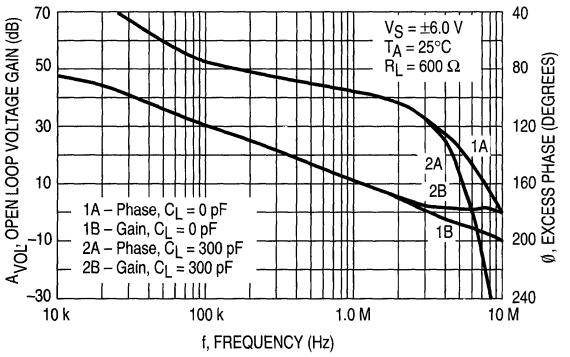


Figure 19. Voltage Gain and Phase versus Frequency

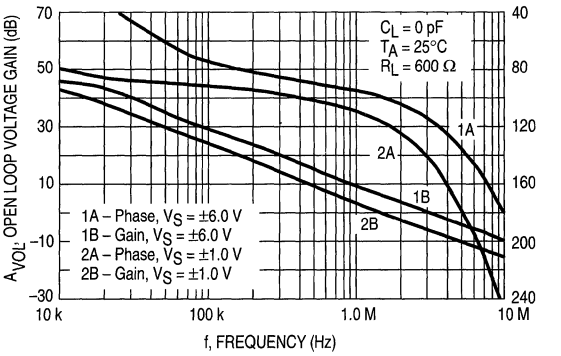


Figure 20. Gain and Phase Margin versus Temperature

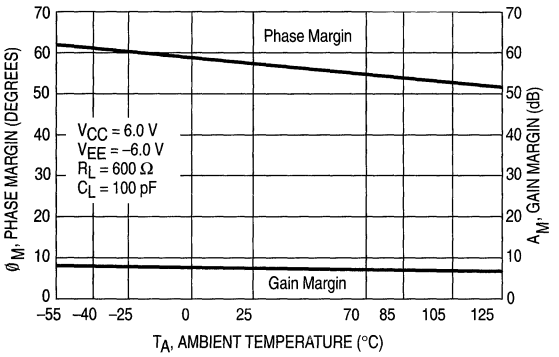
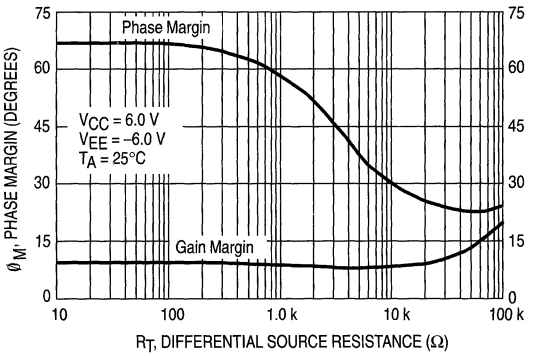


Figure 21. Gain and Phase Margin versus Differential Source Resistance



2

Figure 22. Gain and Phase Margin versus Capacitive Load

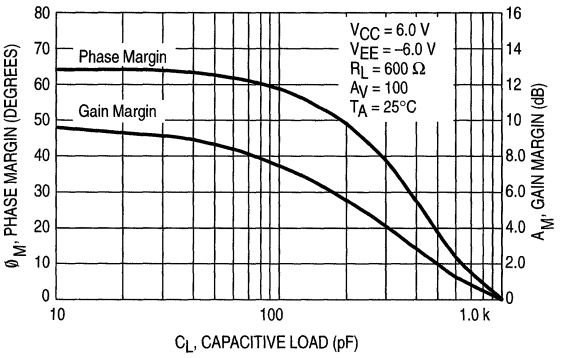


Figure 23. Output Voltage versus Load Resistance

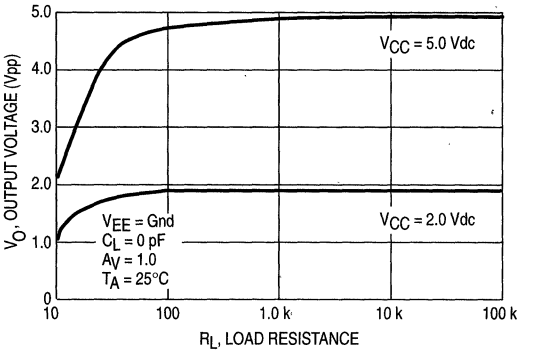


Figure 24. Channel Separation versus Frequency

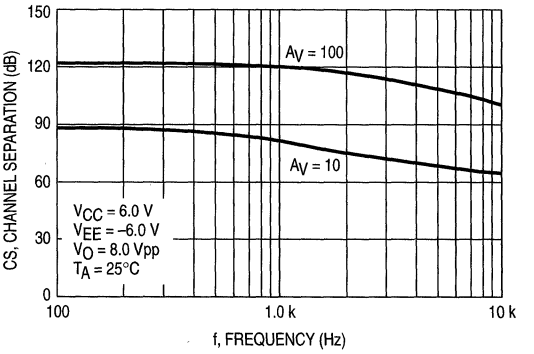


Figure 25. Total Harmonic Distortion versus Frequency

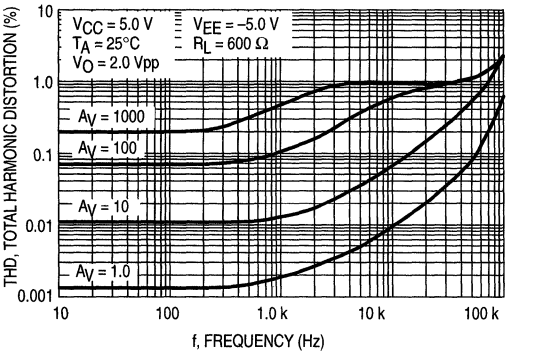
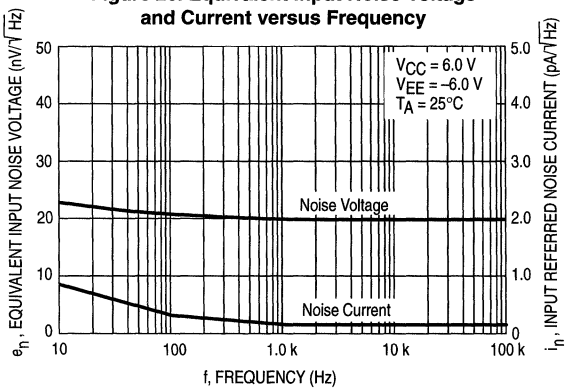


Figure 26. Equivalent Input Noise Voltage and Current versus Frequency



GENERAL INFORMATION

The MC33206/7 family of operational amplifiers are unique in their ability to swing rail–to–rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies. The MC33206/7 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

CIRCUIT INFORMATION

Rail–to–rail performance is achieved at the input of the amplifiers by using parallel NPN–PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than V_{EE}, the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.

In addition to its rail–to–rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600 Ω loads. Because of this high output current capability, care should be taken not to exceed the 150°C maximum junction temperature.

Enable Function

The MC33206/07 enable pins allow the user to externally control the device. (Refer to the Pin Diagram on the first page of this data sheet for enable pin connections.) If the enable pins are pulled low (Gnd) each amplifier (MC33206) and amplifier pair (MC33207) will be disabled. When the enable pins are at a logic high ($V_{Enable} \geq V_{EE} = 1.8$ V) the amplifiers will turn "on". Refer to the data sheet characteristics for the required levels needed to change logical state.

The time to change states (from device "on" to "off" and "off" to "on") is defined as the time delay. The Circuit in Figure 27 is used to measure t_{on} and t_{off}. Typical t_{on} and t_{off} measurements are shown in Figures 28 and 29. When the device is turned off (V_{Enable} = Gnd) an internal regulator is shut off disabling the amplifier.

Figure 27. Test Circuit for t_{on} and t_{off}

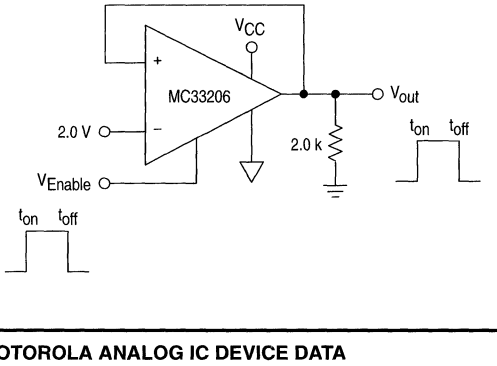
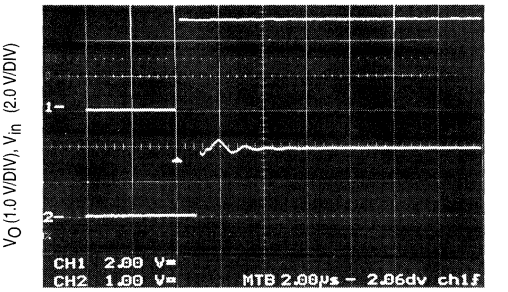
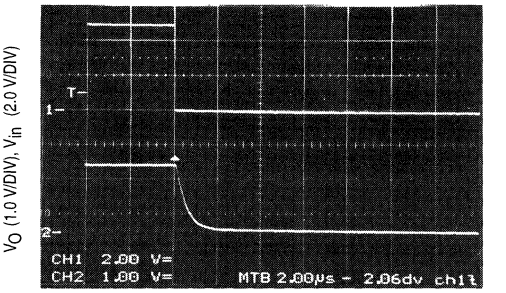


Figure 28. t_{on} Response



t_{on}, TIME (2.0 µs/DIV)

Figure 29. t_{off} Response



t_{off}, TIME (2.0 µs/DIV)

Low Voltage Operation

The MC33206/07 will operate at supply voltages down to 1.8 V and ground. Since this device is a rail–to–rail on both the input and output, one can be assured of continued operation in battery applications when battery voltages drop to low voltage levels. This is called End of Discharge (see Figure 30). Now, the user can select a minimum quantity of batteries best suited for the particular design depending on the type of battery chosen. This will minimize part count in many designs.

Figure 30. Typical Battery Characteristics

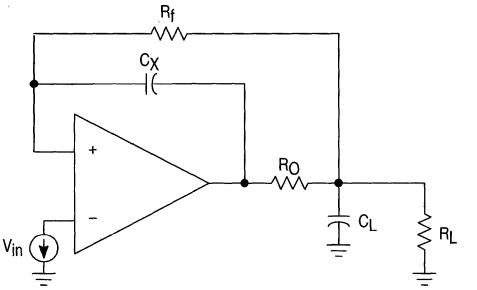
Type	Operating Voltage	End of Discharge
Alkaline	1.5 V	0.9 V
NiCd	1.2 V	1.0 V
NiMh	1.2 V	1.0 V
Silver Oxide	1.6 V	1.3 V
Lithium Ion	3.6 V	2.5 V

Compensating for Output Capacitance

The combination of device output impedance and increasing capacitive loading will cause phase delay (reducing the phase margin) in any amplifier (Figure 22). If the loading is excessive, the resulting response can be circuit oscillation. In other words, an amplifier can become unstable when the phase becomes greater than 180 degrees before the open loop gain drops to unity gain. Figures 18 and 19 show this situation as frequency increases for a given load. The MC33206/7 can typically drive up to 300 pF loads at unity gain without oscillating.

2

Figure 31. Capacitive Loads Compensation



There are several ways to compensate for this phenomena. Adding series resistance to the output is one way, but not an ideal solution. A dc voltage error will occur at the output. A better design solution to compensate for higher capacitive loads would be to use the circuit in Figure 31. This design helps to counteract the loss of phase margin by taking the high frequency output signal and feeding it back into the amplifier inverting input. This technique helps to overcome oscillation due to a highly capacitive load. Keep in mind that compensation will have the affect of lowering the Gain Bandwidth Product (GPW). The values of C_X and R0, are determined experimentally. Typical C_X and C_L will be the same value.

SPICE Model

If a SPICE Macromodel is desired for the MC33206/07, the user can define the characteristics from the following information. Obtain the SPICE Macromodel for the MC33204 Rail–to–Rail Operational Amplifier (device is the same as the MC33207). For the Enable feature of the MC33207, simulate it as a bipolar switch. The Macromodel does not include an input capacitance between the inverting and noninverting inputs. This capacitor is called C_{in}. Add 3.0 to 5.0 pF if stability analysis is required.

Figure 32. Noninverting Amplifier Slew Rate

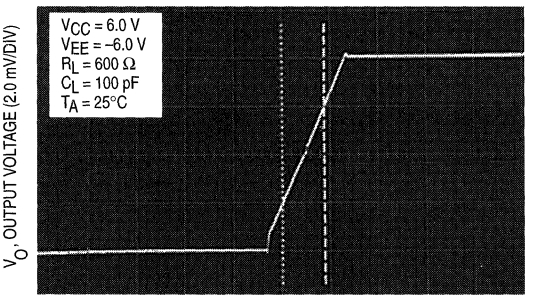


Figure 33. Small Signal Transient Response

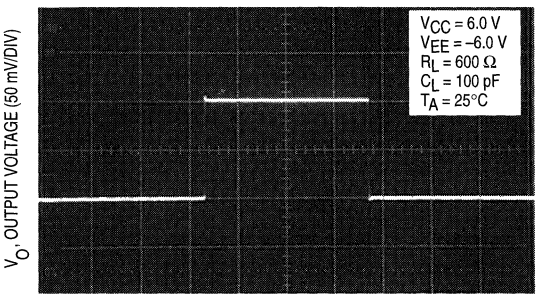
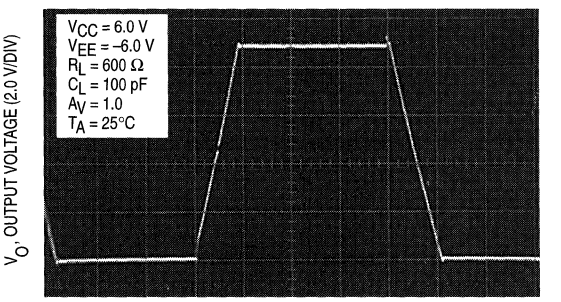


Figure 34. Large Signal Transient Response



MC33272A
MC33274A

HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

Single Supply, High Slew Rate Low Input Offset Voltage, Bipolar Operational Amplifiers

The MC33272/74 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar design concepts. This dual and quad operational amplifier series incorporates Bipolar inputs along with a patented Zip–R–Trim element for input offset voltage reduction. The MC33272/74 series of operational amplifiers exhibits low input offset voltage and high gain bandwidth product. Dual–doublet frequency compensation is used to increase the slew rate while maintaining low input noise characteristics. Its all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, and an excellent phase and gain margin. It also provides a low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

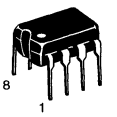
The MC33272/74 series is specified over –40° to +85°C and are available in plastic DIP and SOIC surface mount packages.

- Input Offset Voltage Trimmed to 100 μV (Typ)
- Low Input Bias Current: 300 nA
- Low Input Offset Current: 3.0 nA
- High Input Resistance: 16 MΩ
- Low Noise: 18 nV/$\sqrt{\text{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Product: 24 MHz @ 100 kHz
- High Slew Rate: 10 V/μs
- Power Bandwidth: 160 kHz
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to 500 pF
- Large Output Voltage Swing: +14.1 V/ –14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Single or Split Supply Operation: +3.0 V to +36 V or ±1.5 V to ±18 V
- ESD Diodes Provide Added Protection to the Inputs

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Dual	MC33272AD	T_A = –40° to +85°C	SO–8
	MC33272AP		Plastic DIP
Quad	MC33274AD		SO–14
	MC33274AP		Plastic DIP

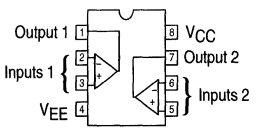
DUAL



P SUFFIX
PLASTIC PACKAGE
CASE 626

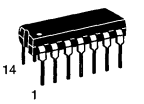
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

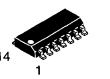


(Top View)

QUAD

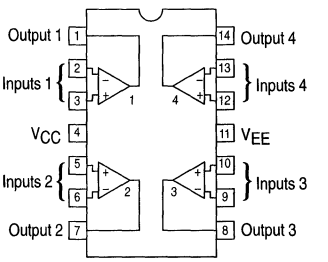


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} to V_{EE}	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

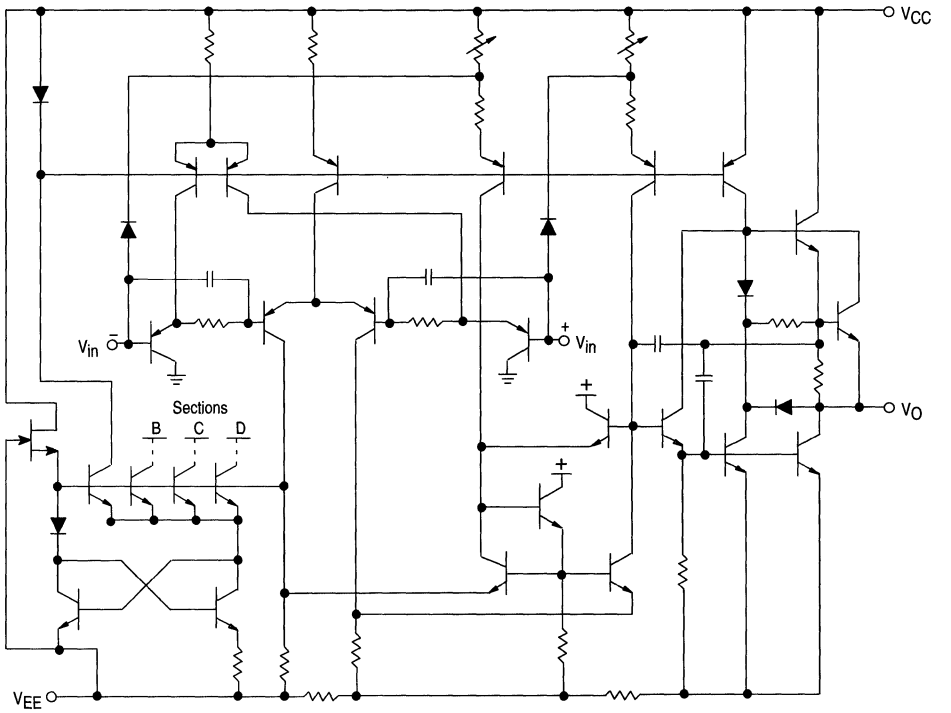
DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	3	$\lvert V_{IO}\rvert$				mV
(V_{CC} = +15 V, V_{EE} = –15 V)						
T_A = +25°C			—	0.1	1.0	
T_A = –40° to +85°C			—	—	1.8	
(V_{CC} = 5.0 V, V_{EE} = 0)						
T_A = +25°C			—	—	2.0	
Average Temperature Coefficient of Input Offset Voltage	3	$\Delta V_{IO}/\Delta T$				μV/°C
R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = –40° to +85°C			—	2.0	—	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	4, 5	I_{IB}				nA
T_A = +25°C			—	300	650	
T_A = –40° to +85°C			—	—	800	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)		$\lvert I_{IO}\rvert$				nA
T_A = +25°C			—	3.0	65	
T_A = –40° to +85°C			—	—	80	
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	6	V_{ICR}	V_{EE} to (V_{CC} –1.8)			V
T_A = +25°C						
Large Signal Voltage Gain (V_O = 0 V to 10 V, R_L = 2.0 kΩ)	7	A_{VOL}				dB
T_A = +25°C			90	100	—	
T_A = –40° to +85°C			86	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 12					V
(V_{CC} = +15 V, V_{EE} = –15 V)						
R_L = 2.0 kΩ		V_O+	13.4	13.9	—	
R_L = 2.0 kΩ		V_O–	—	–13.9	–13.5	
R_L = 10 kΩ		V_O+	13.4	14	—	
R_L = 10 kΩ		V_O–	—	–14.7	–14.1	
(V_{CC} = 5.0 V, V_{EE} = 0 V)	10, 11					
R_L = 2.0 kΩ		V_{OL}	—	—	0.2	
R_L = 2.0 kΩ		V_{OH}	3.7	—	5.0	
Common Mode Rejection (V_{in} = +13.2 V to –15 V)	13	CMR	80	100	—	dB
Power Supply Rejection	14, 15	PSR				dB
V_{CC}/V_{EE} = +15 V/ –15 V, +5.0 V/ –15 V, +15 V/ –5.0 V			80	105	—	
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	16	I_{SC}				mA
Source			+25	+37	—	
Sink			–25	–37	—	
Power Supply Current Per Amplifier (V_O = 0 V)	17	I_{CC}				mA
(V_{CC} = +15 V, V_{EE} = –15 V)						
T_A = +25°C			—	2.15	2.75	
T_A = –40° to +85°C			—	—	3.0	
(V_{CC} = 5.0 V, V_{EE} = 0 V)						
T_A = +25°C			—	—	2.75	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0 V)	18, 33	SR	8.0	10	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	19	GBW	17	24	—	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V, f = 20 kHz)	20, 21, 22	A_{VO}	—	65	—	dB
Unity Gain Frequency (Open Loop)		f_U	—	5.5	—	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 24, 26	A_m	—	12	—	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 25, 26	ϕ_m	—	55	—	Degrees
Channel Separation (f = 20 Hz to 20 kHz)	27	CS	—	−120	—	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)		BW_P	—	160	—	kHz
Total Harmonic Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	28	THD	—	0.003	—	%
Open Loop Output Impedance (V_O = 0 V, f = 6.0 MHz)	29	$\|Z_O\|$	—	35	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{IN}	—	16	—	MΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{IN}	—	3.0	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	30	e_n	—	18	—	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz)	31	i_n	—	0.5	—	pA/√Hz

Figure 1. Equivalent Circuit Schematic (Each Amplifier)



2

Figure 2. Maximum Power Dissipation versus Temperature

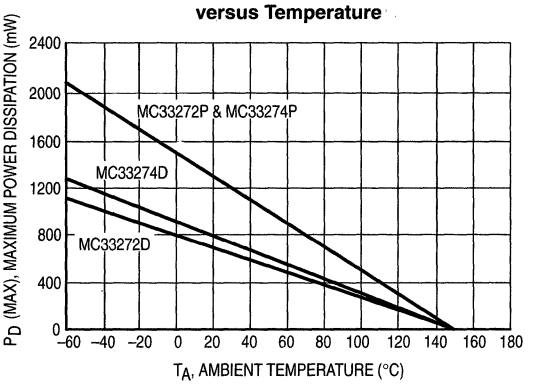


Figure 3. Input Offset Voltage versus Temperature for Typical Units

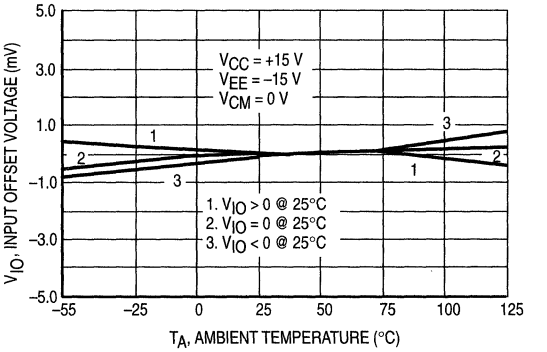


Figure 4. Input Bias Current versus Common Mode Voltage

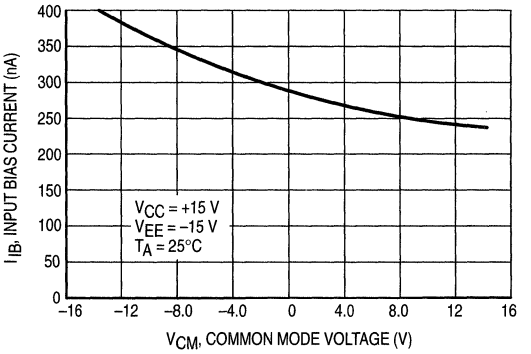


Figure 5. Input Bias Current versus Temperature

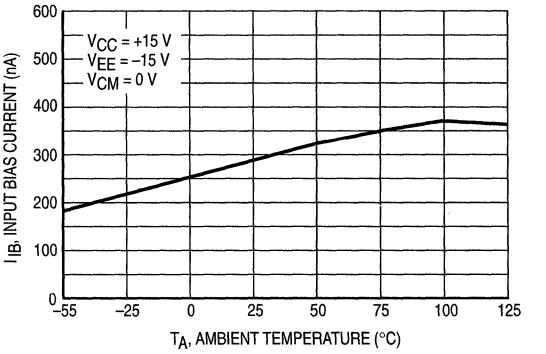


Figure 6. Input Common Mode Voltage Range versus Temperature

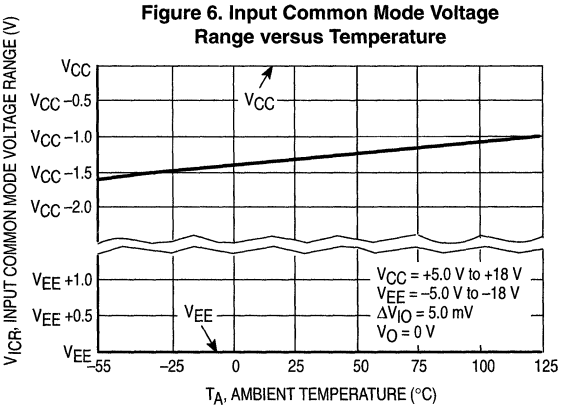


Figure 7. Open Loop Voltage Gain versus Temperature

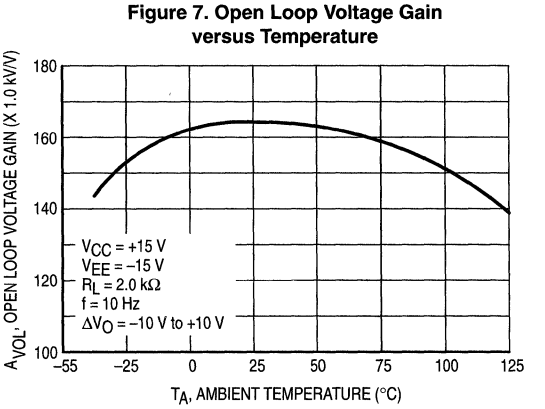


Figure 8. Split Supply Output Voltage Swing versus Supply Voltage

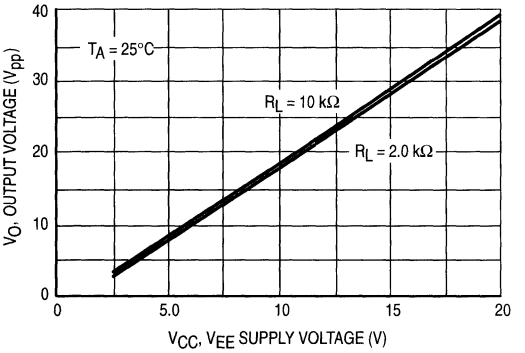


Figure 9. Split Supply Output Saturation Voltage versus Load Current

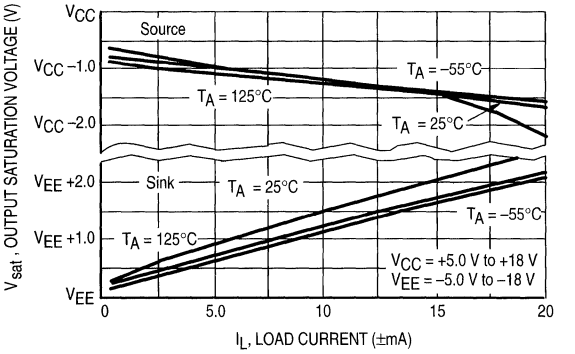


Figure 10. Single Supply Output Saturation Voltage versus Load Resistance to Ground

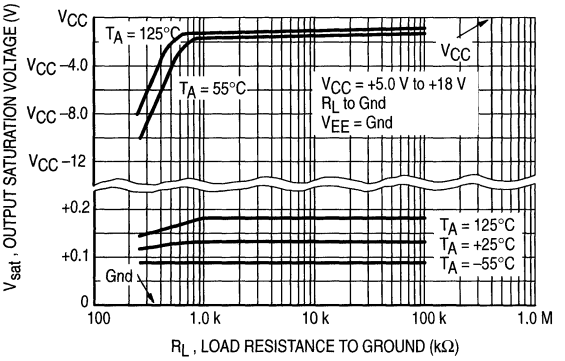


Figure 11. Single Supply Output Saturation Voltage versus Load Resistance to V_{CC}

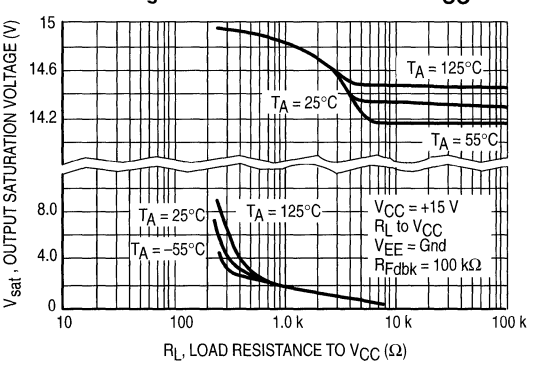


Figure 12. Output Voltage versus Frequency

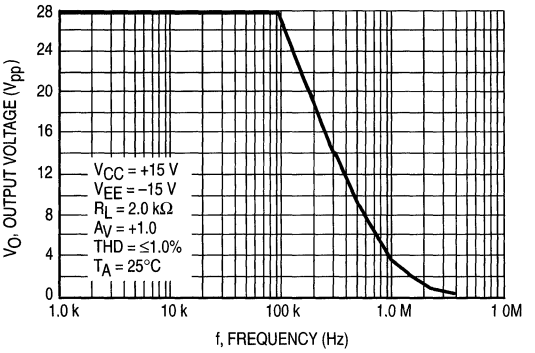
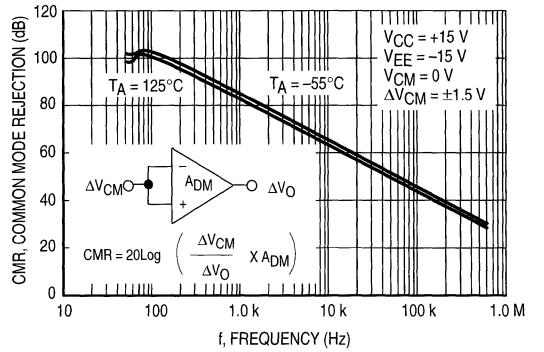


Figure 13. Common Mode Rejection versus Frequency



2

Figure 14. Positive Power Supply Rejection versus Frequency

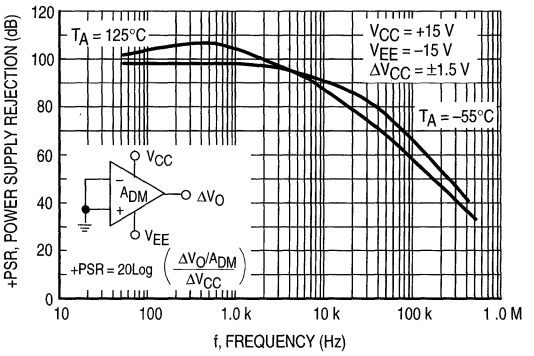


Figure 15. Negative Power Supply Rejection versus Frequency

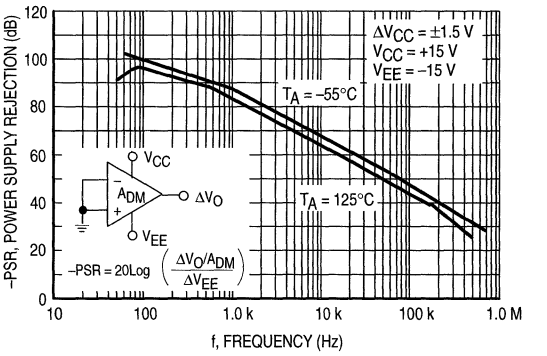


Figure 16. Output Short Circuit Current versus Temperature

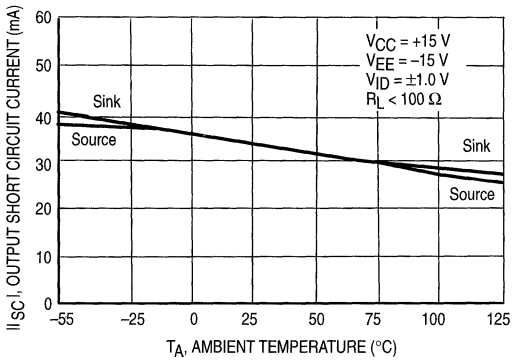


Figure 17. Supply Current versus Supply Voltage

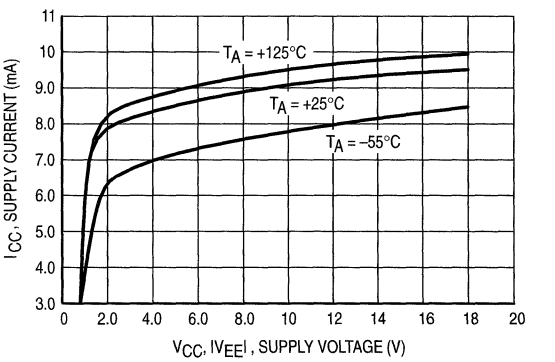


Figure 18. Normalized Slew Rate versus Temperature

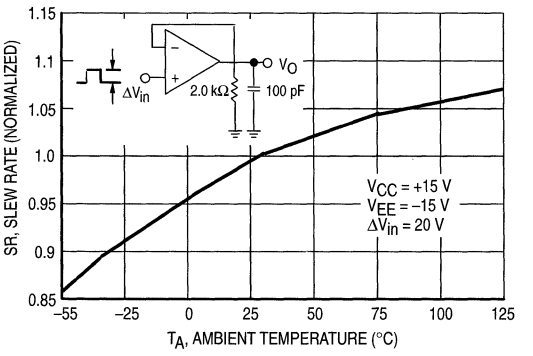


Figure 19. Gain Bandwidth Product versus Temperature

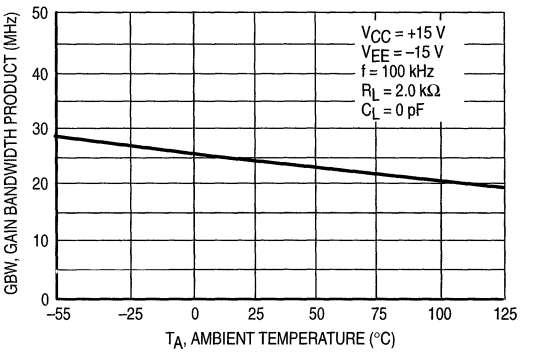


Figure 20. Voltage Gain and Phase versus Frequency

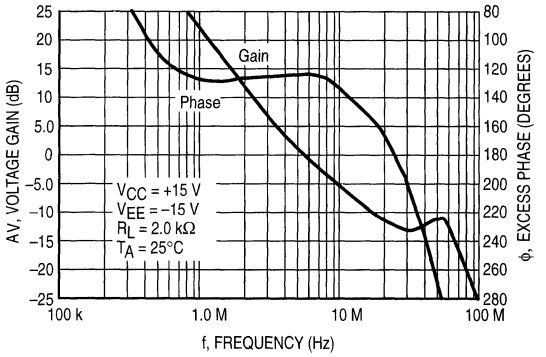


Figure 21. Gain and Phase versus Frequency

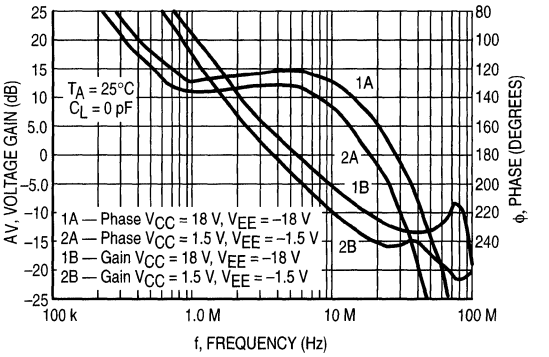


Figure 22. Open Loop Voltage Gain and Phase versus Frequency

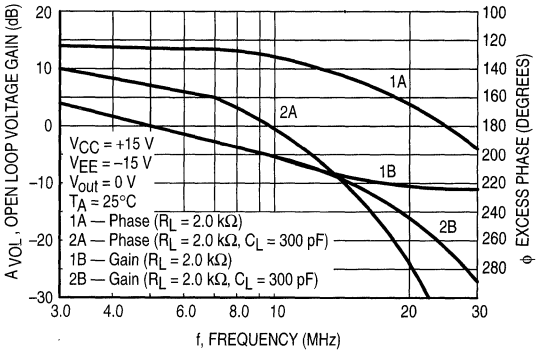


Figure 23. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

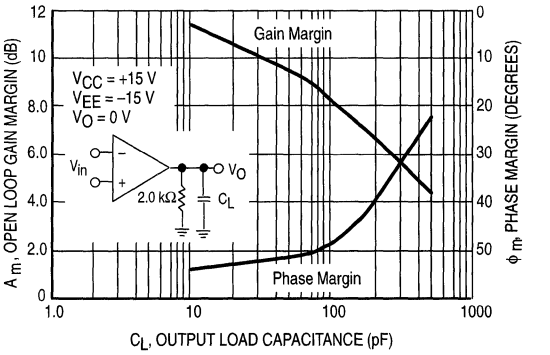


Figure 24. Open Loop Gain Margin versus Temperature

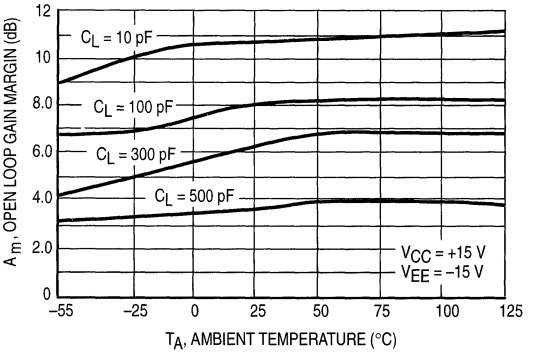
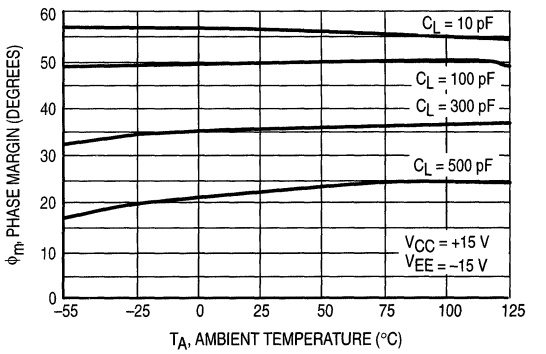


Figure 25. Phase Margin versus Temperature



2

Figure 26. Phase Margin and Gain Margin versus Differential Source Resistance

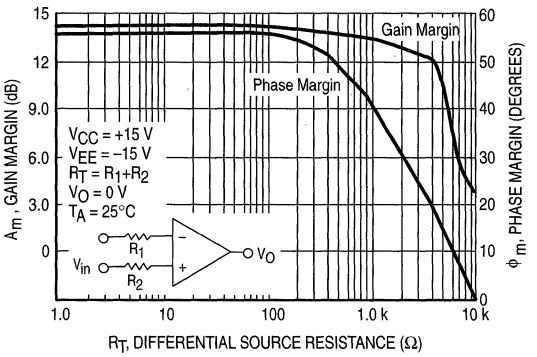


Figure 27. Channel Separation versus Frequency

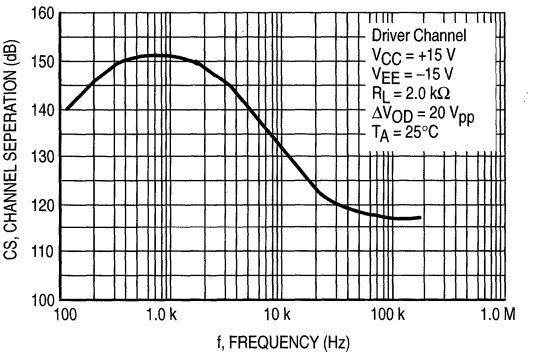


Figure 28. Total Harmonic Distortion versus Frequency

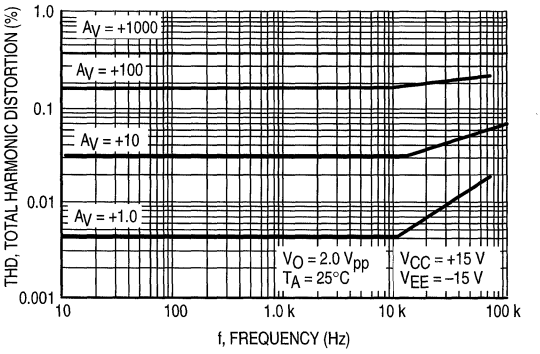


Figure 29. Output Impedance versus Frequency

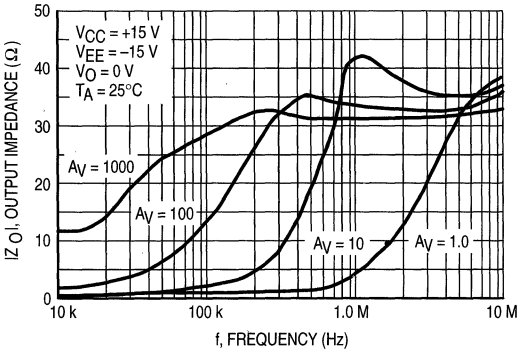


Figure 30. Input Referred Noise Voltage versus Frequency

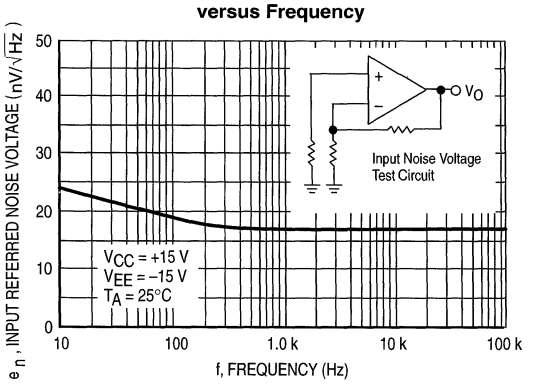


Figure 31. Input Referred Noise Current versus Frequency

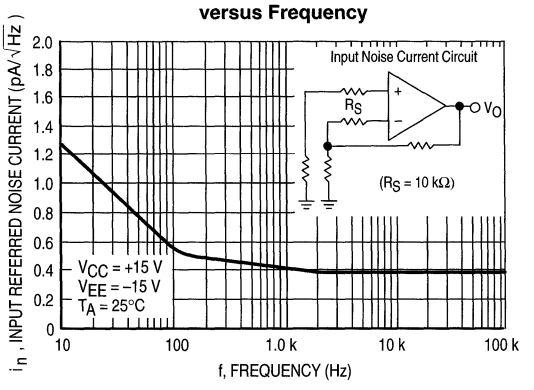


Figure 32. Percent Overshoot versus Load Capacitance

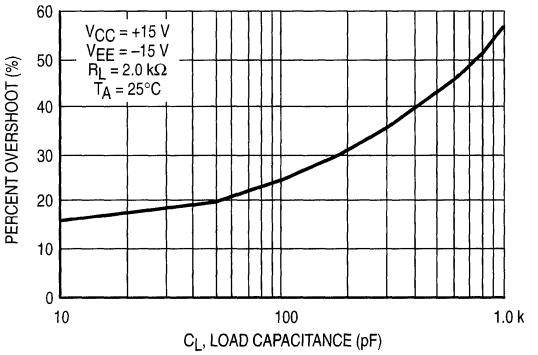


Figure 33. Noninverting Amplifier Slew Rate for the MC33274

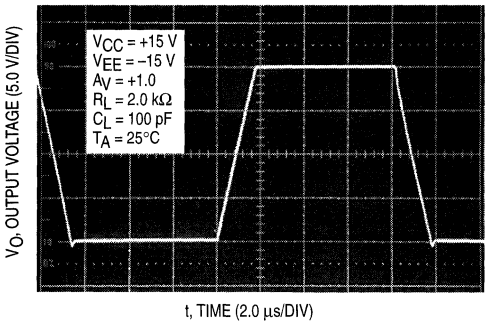


Figure 34. Noninverting Amplifier Overshoot for the MC33274

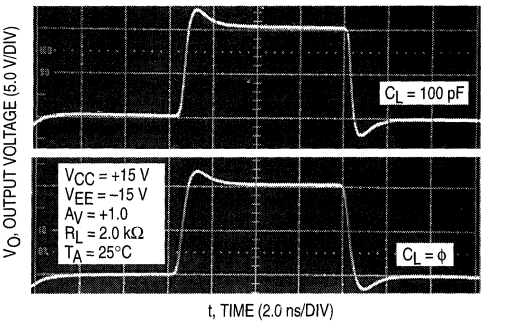


Figure 35. Small Signal Transient Response for MC33274

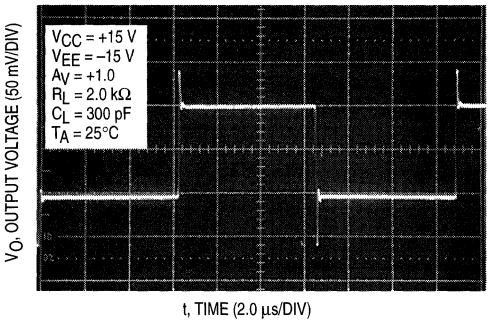
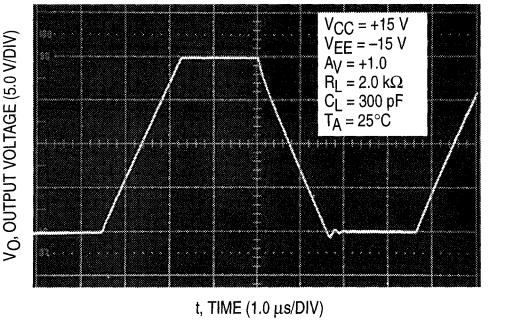


Figure 36. Large Signal Transient Response for MC33274



MC33282
MC33284

HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

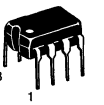
Low Input Offset, High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifiers

The MC33282/284 series of high performance operational amplifiers are quality fabricated with innovative bipolar and JFET design concepts. This dual and quad amplifier series incorporates JFET inputs along with a patented Zip–R–Trim® element for input offset voltage reduction. These devices exhibit low input offset voltage, low input bias current, high gain bandwidth and high slew rate. Dual–doublet frequency compensation is incorporated to produce high quality phase/gain performance. In addition, the MC33282/284 series exhibit low input noise characteristics for JFET input amplifiers. Its all NPN output stage exhibits no deadband crossover distortion and a large output voltage swing. They also provide a low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

The MC33282/284 series are specified over –40° to +85°C and are available in plastic DIP and SOIC surface mount packages.

- Low Input Offset Voltage: Trimmed to 200 μV
- Low Input Bias Current: 30 pA
- Low Input Offset Current: 6.0 pA
- High Input Resistance: 10^{12} Ω
- Low Noise: 18 nV $\sqrt{Hz}$ @ 1.0 kHz
- High Gain Bandwidth Products: 35 MHz @ 100 kHz
- High Slew Rate: 15 V/μs
- Power Bandwidth: 175 kHz
- Unity Gain Stable: w/Capacitance Loads to 300 pF
- Large Output Voltage Swing: +14.1 V/–14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Dual Supply Operation: ±2.5 V to ±18 V (Max)

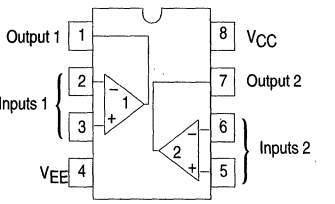
DUAL



P SUFFIX
PLASTIC PACKAGE
CASE 626

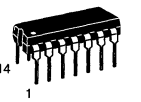
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

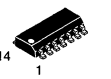


(Top View)

QUAD

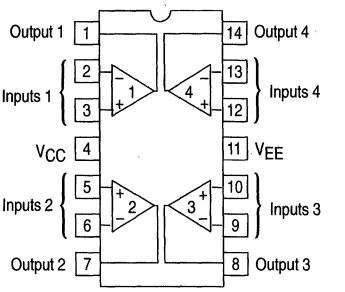


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Dual	MC33282D	T_A = –40° to +85°C	SOP–8
	MC33282P		Plastic DIP
Quad	MC33284D		SO–14
	MC33284P		Plastic DIP

Zip–R–Trim is a registered trademark of Motorola Inc.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	– 60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Figure	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	$\|V_{IO}\|$	3				mV
T_A = +25°C			—	0.2	2.0	
T_A = –40° to +85°C			—	—	4.0	
Average Temperature Coefficient of Input Offset Voltage	$\|\Delta V_{IO}\|/\Delta T$	3				μV/°C
R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = T_{low} to T_{high}			—	15	—	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}	4, 5				
T_A = +25°C			–200	30	200	pA
T_A = –40° to +85°C			–2.0	—	2.0	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}					
T_A = +25°C			–100	6.0	100	pA
T_A = –40° to +85°C			–1.0	—	1.0	nA
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	V_{ICR}	6	–11 —	–12 +14	— +11	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	7				V/mV
T_A = +25°C			50	200	—	
T_A = –40° to +85°C			25	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)		8, 9, 10				V
R_L = 2.0 kΩ	V_O+		13.2	+13.7	—	
R_L = 2.0 kΩ	V_O–		—	–13.9	–13.2	
R_L = 10 kΩ	V_O+		13.7	+14.1	—	
R_L = 10 kΩ	V_O–		—	–14.6	–14.3	
Common Mode Rejection (V_{in} = ±11 V)	CMR	11	70	90	—	dB
Power Supply Rejection	PSR	12				dB
V_{CC}/V_{EE} = +15 V/–15 V, +5.0 V/–15 V, +15 V/–5.0 V			75	100	—	
Output Short Circuit Current (V_{ID} = 1.0 V, output to ground)	I_{SC}	13, 14				mA
Source			15	+21	—	
Sink			—	–27	–15	
Power Supply Current (V_O = 0 V, per amplifier)	I_D	15				mA
T_A = +25°C			—	2.15	2.75	
T_A = –40° to +85°C			—	—	3.0	

2

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Figure	Min	Typ	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0)	SR	16, 28, 29	8.0	15	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	17	20	35	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V, f = 20 kHz)	A_{VO}	18, 21	—	1750	V/V
Unity Gain Frequency (Open Loop)	f_U		—	5.5	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 0 pF)	A_m	19, 20	—	15	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 0 pF)	ϕ_m	19, 20	—	40	Degrees
Channel Separation (f = 20 Hz to 20 kHz)	CS	22	—	–120	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)	BW_P		—	175	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	THD	23	—	0.003	%
Open Loop Output Impedance (V_O = 0 V, f = 9.0 MHz)	$\|Z_O\|$	24	—	37	Ω
Differential Input Resistance (V_{CM} = 0 V)	R_{in}		—	10^{12}	Ω
Differential Input Capacitance (V_{CM} = 0 V)	C_{in}		—	5.0	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n	25	—	18	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz)	i_n		—	0.01	pA/√Hz

Figure 1. Equivalent Circuit Schematic
(Each Amplifier)

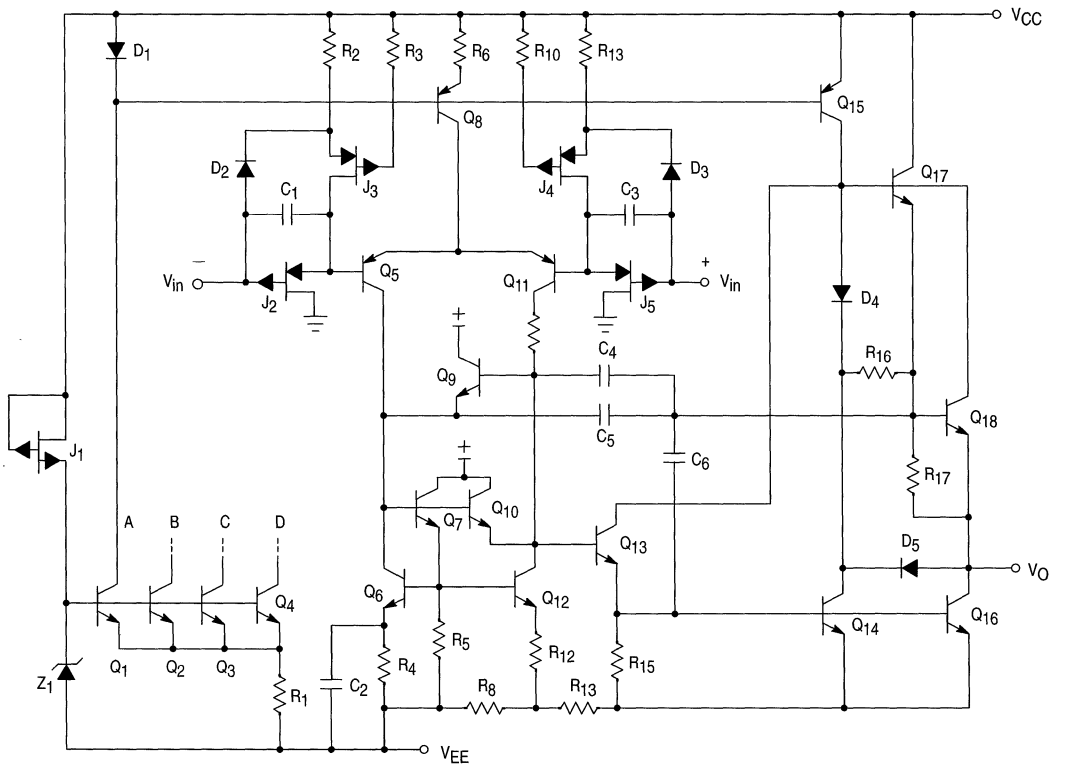


Figure 2. Maximum Power Dissipation versus Temperature

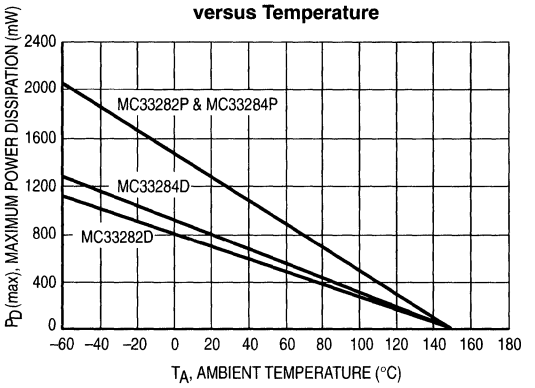


Figure 3. Input Offset Voltage versus Temperature for Typical Units

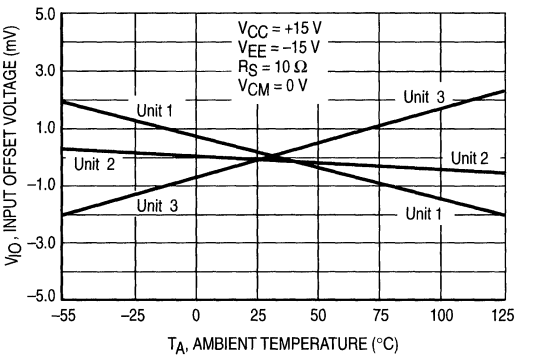


Figure 4. Input Bias Current versus Temperature

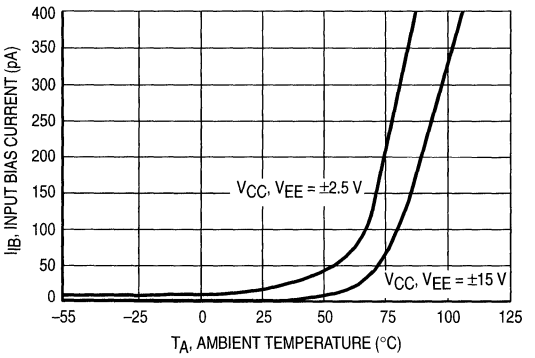


Figure 5. Input Bias Current versus Common Mode Voltage

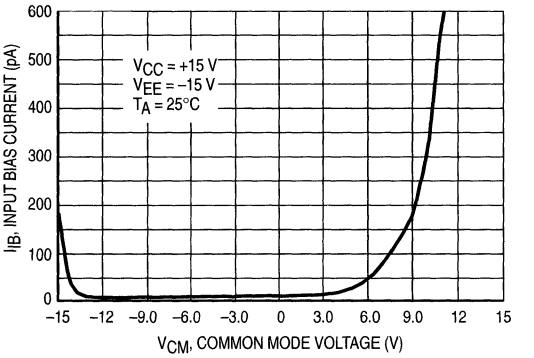


Figure 6. Input Common Mode Voltage Range versus Temperature

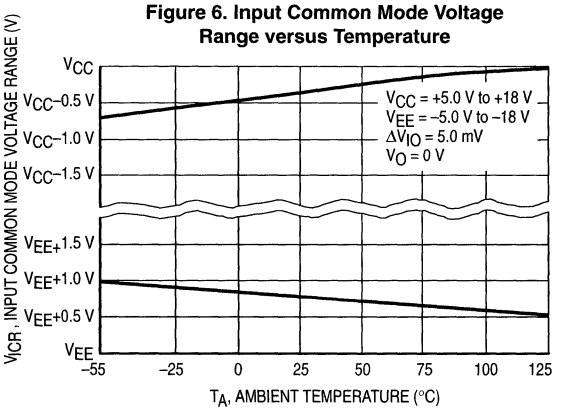
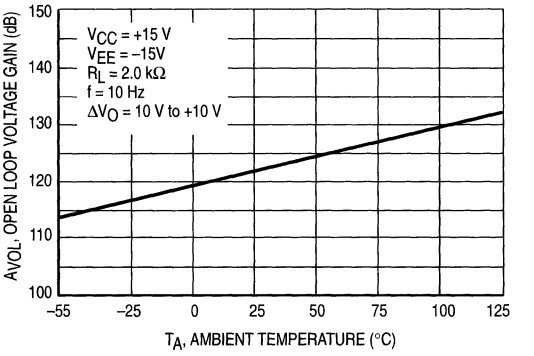


Figure 7. Open Loop Voltage Gain versus Temperature



2

Figure 8. Output Voltage Swing versus Supply Voltage

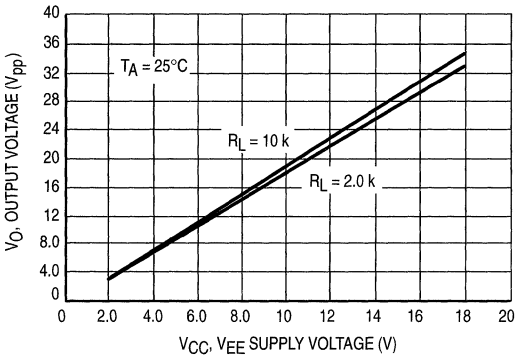


Figure 9. Output Voltage versus Frequency

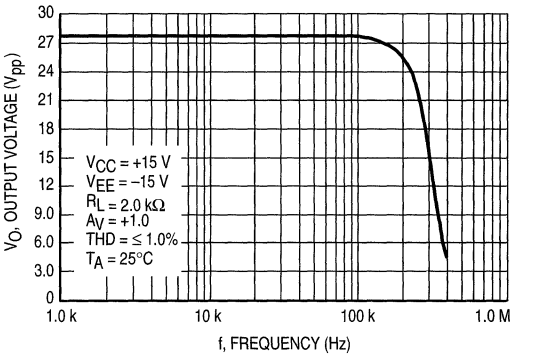


Figure 10. Output Saturation Voltage versus Load Current

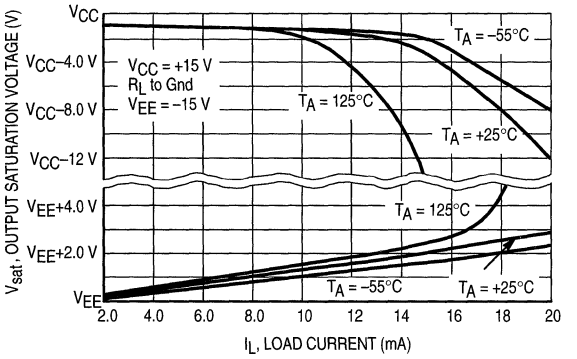


Figure 11. Common Mode Rejection versus Frequency

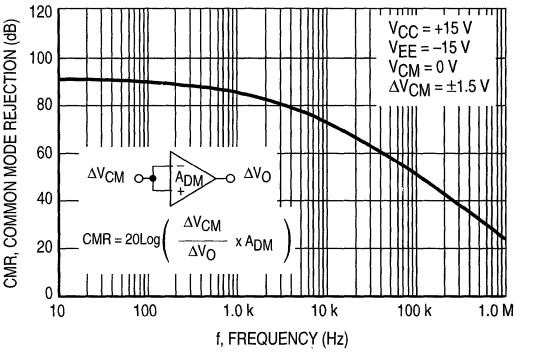


Figure 12. Positive Power Supply Rejection versus Frequency

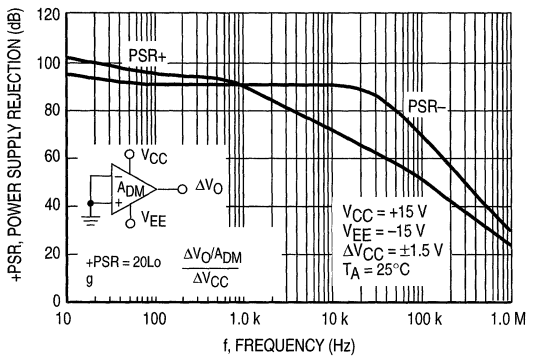


Figure 13. Output Short Circuit Source Current versus Temperature

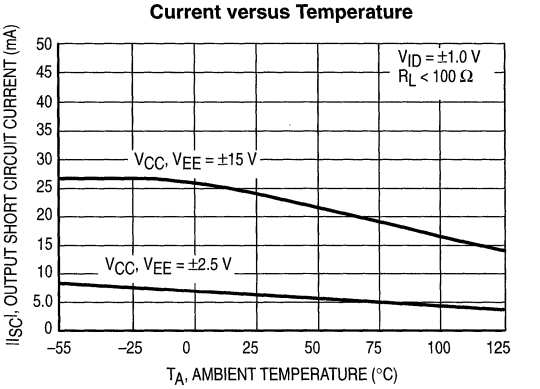


Figure 14. Output Short Circuit Sink Current versus Temperature

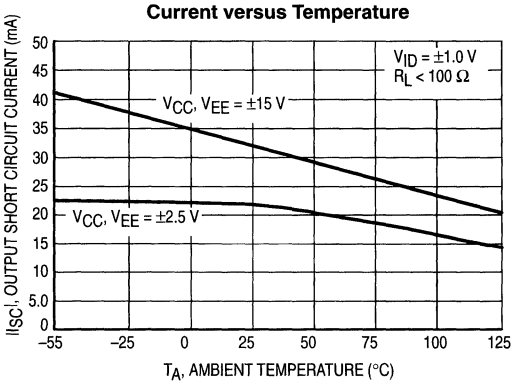


Figure 15. Power Supply Current versus Supply Voltage

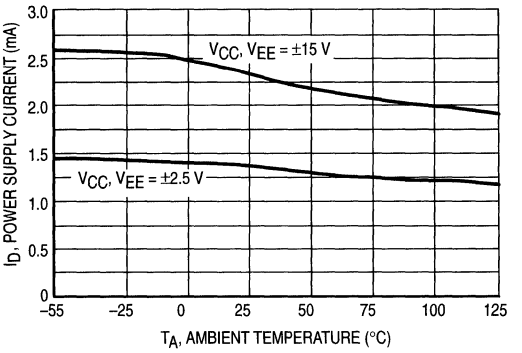


Figure 16. Slew Rate versus Temperature

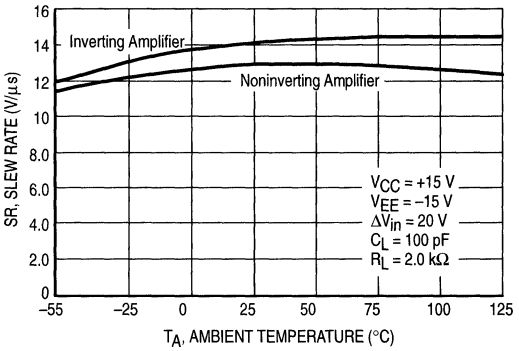


Figure 17. Gain Bandwidth Product versus Temperature

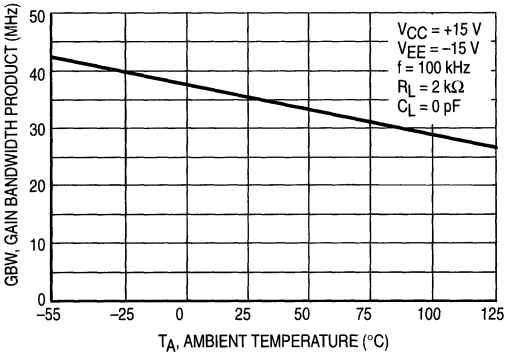


Figure 18. Gain and Phase versus Frequency

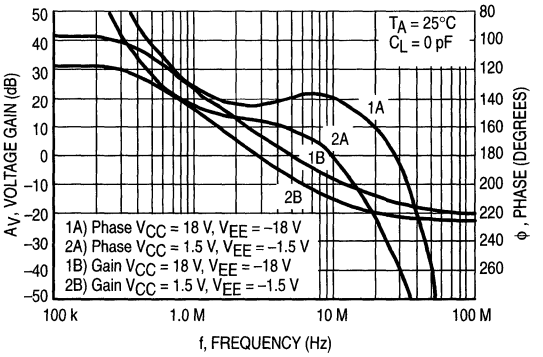
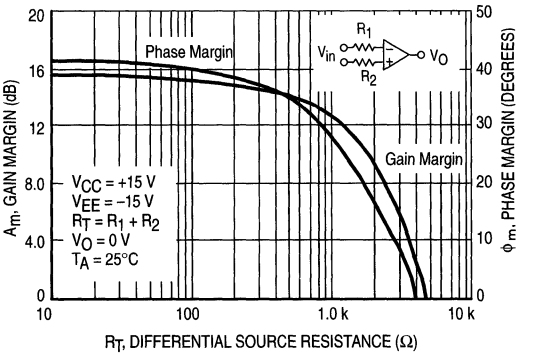


Figure 19. Phase Margin and Gain Margin versus Differential Source Resistance



2

Figure 20. Open Loop Gain and Phase Margin versus Output Load Capacitance

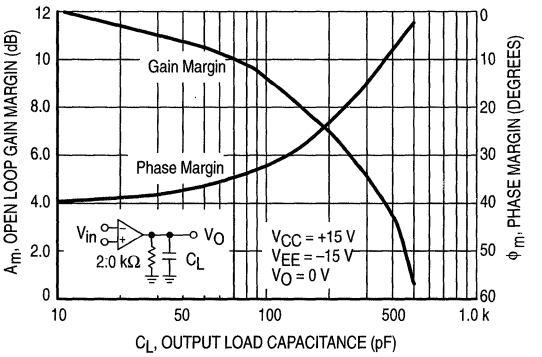


Figure 21. Gain and Phase versus Frequency

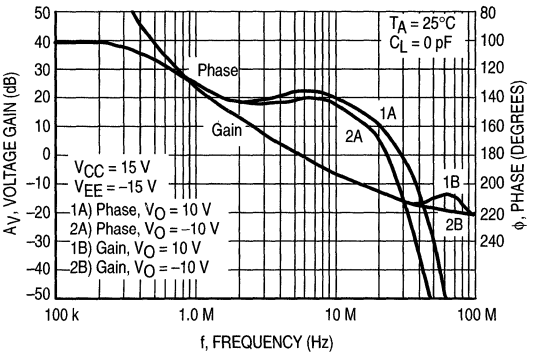


Figure 22. Channel Separation versus Frequency

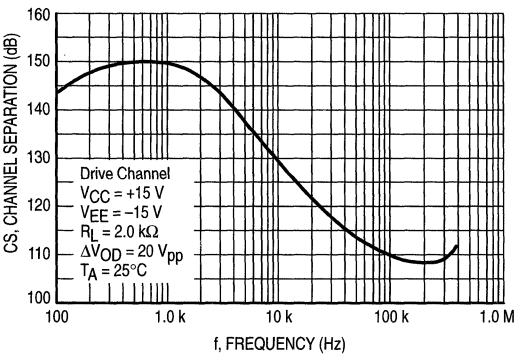


Figure 23. Total Harmonic Distortion versus Frequency

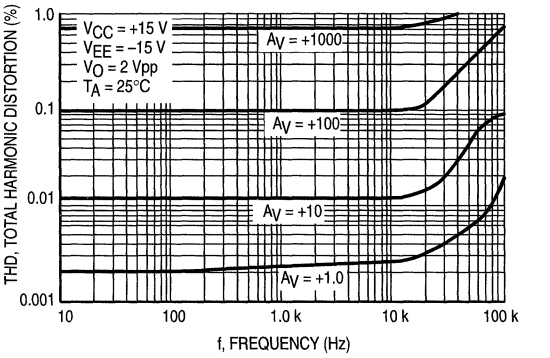


Figure 24. Output Impedance versus Frequency

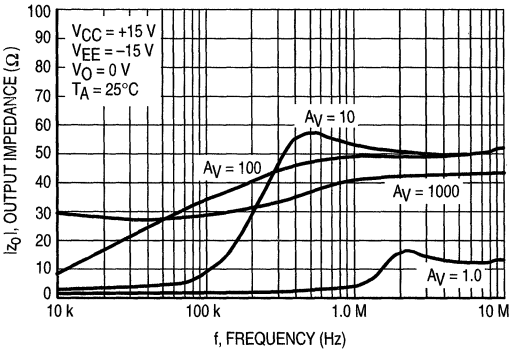


Figure 25. Input Referred Noise Voltage versus Frequency

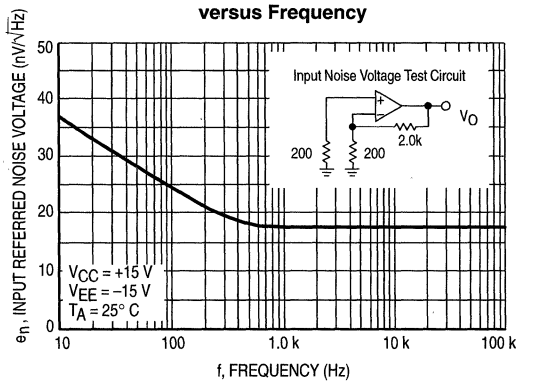


Figure 26. Percent Overshoot versus Load Capacitance

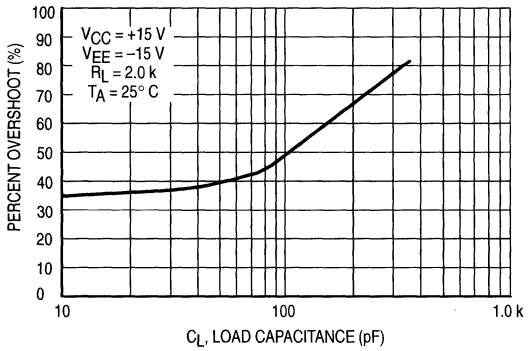


Figure 27. Noninverting Amplifier Overshoot

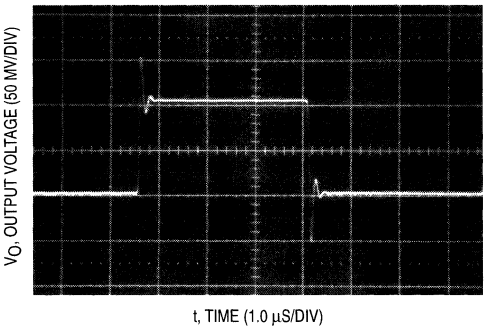


Figure 28. Noninverting Amplifier Slew Rate

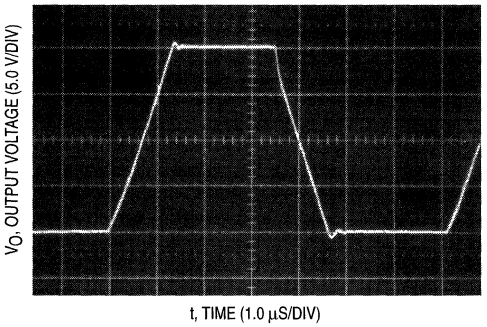
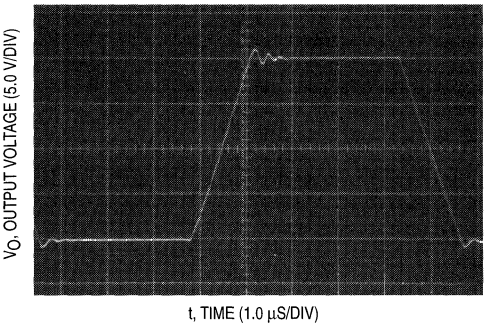


Figure 29. Inverting Amplifier Slew Rate



MC33304

Low Voltage Rail-To-Rail Sleep-Mode™ Operational Amplifier

The MC33304 is a monolithic bipolar operational amplifier. This low voltage rail–to–rail amplifier has both a rail–to–rail input and output stage, with high output current capability. This amplifier also employs Sleep–Mode technology. In sleepmode, the micropower amplifier is active and waiting for an input signal. When a signal is applied, causing the amplifier to source or sink ≥200 μA (typically) to the load, it will automatically switch to the awakemode (supplying up to 70 mA to the load). When the output current drops below 90 μA, the amplifier automatically returns to the sleepmode.

Excellent performance can be achieved as an audio amplifier. This is due to the amplifier's low noise and low distortion. A delay circuit is incorporated to prevent crossover distortion.

- Ideal for Battery Applications
- Full Output Signal (No Distortion) for Battery Applications Down to ±0.9 VDC.
- Single Supply Operation (+1.8 to +12 V)
- Rail–To–Rail Performance on Both the Input and Output
- Output Voltages Swings Typically within 100 mV of Both Rails (R_L = 1.0 mΩ)
- Two States: "Sleepmode" (Micropower, I_D = 110 μA/Amp) and "Awakemode" (High Performance, I_D = 1200 μA/Amp)
- Automatic Return to Sleepmode when Output Current Drops Below Threshold, Allowing a Fully Functional Micropower Amplifier
- Independent Sleepmode Function for Each Amplifier
- No Phase Reversal on the Output for Overdriven Input Signals
- High Output Current (70 mA typically)
- 600 Ω Drive Capability
- Standard Pinouts; No Additional Pins or Components Required
- Drop–In Replacement for Many Other Quad Operational Amplifiers
- Similar to MC33201, MC33202 and MC33204 Family
- The MC33304 Amplifier is Offered in the Plastic DIP or SOIC Package (P and D Suffixes)

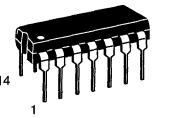
TYPICAL DC ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	V_{CC} = 2.0 V	V_{CC} = 3.3 V	V_{CC} = 5.0 V	Unit
Input Offset Voltage $V_{IO(max)}$ MC33304	±10	±10	±10	mV
Output Voltage Swing V_{OH} (R_L = 600 Ω)	1.85	3.10	4.75	V_{min}
V_{OL} (R_L = 600 Ω)	0.15	0.15	0.15	V_{max}
Power Supply Current per Amplifier (I_D)				
Awakemode	1.625	1.625	1.625	mA
Sleepmode	140	140	140	μA

Specifications are for reference only and not necessarily guaranteed. V_{EE} = Gnd.

RAIL–TO–RAIL SLEEP–MODE OPERATIONAL AMPLIFIER

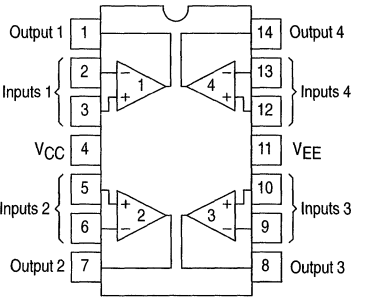
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Quad, Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33304D	T_A = – 40° to +105°C	SO–14
MC33304P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+16	V
ESD Protection Voltage at Any Pin Human Body Model	V_{ESD}	2000	V
Voltage at Any Device Pin (Note 2)	V_{DP}	$V_S \pm 0.5$	V
Input Differential Voltage Range	V_{IDR}	(Notes 1 & 2)	V
Output Short Circuit Duration	t_s	Indefinite (Note 3)	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Maximum Power Dissipation	P_D	(Note 5)	mW

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage Single Supply Split Supplies	V_S	 1.8 ±0.9	 – –	 12 ±6.0	V
Input Voltage Range, Sleepmode and Awakemode	V_{ICR}	V_{EE}	–	V_{CC}	V
Ambient Operating Temperature Range	T_A	–40	–	+105	°C

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} = 0 V, V_O = 0 V) (Note 4) Sleepmode and Awakemode T_A = 25°C T_A = –40° to +105°C	V_{IO}	 –10 –13	 0.7 –	 +10 +13	mV
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V) T_A = –40° to +105°C, Sleepmode and Awakemode	$\Delta V_{IO}/\Delta T$	 –	 2.0	 –	µV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) (Note 4) Awakemode T_A = 25°C T_A = –40° to +105°C	$\lvert I_{IB}\rvert$	 – –	 90 –	 +200 +500	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) (Note 4) Awakemode T_A = 25°C T_A = –40° to +105°C	$\lvert I_{IO}\rvert$	 – –	 3.1 –	 +50 +100	nA
Large Signal Voltage Gain (V_{CC} = +5.0 V, V_{EE} = –5.0 V) Awakemode, R_L = 600 Ω T_A = 25°C T_A = –40° to +105°C	A_{VOL}	 90 85	 116 –	 – –	dB
Power Supply Rejection Ratio, Awakemode	PSRR	65	90	–	dB
Output Short Circuit Current (Awakemode) (V_{ID} = ±0.2 V) Source Sink	I_{SC}	 –200 +50	 –89 +89	 –50 +200	mA
Output Transition Current, Source/Sink Sleepmode to Awakemode, V_{CC} = +1.0 V, V_{EE} = –1.0 V Awakemode to Sleepmode, V_{CC} = +5.0 V, V_{EE} –5.0 V	 $\lvert I_{TH1}\rvert$ $\lvert I_{TH2}\rvert$	 – 90	 – –	 200 –	µA

DC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = +5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage Swing (V_{ID} = ±0.2 V)					V
Sleepmode					
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 1.0 MΩ	V_{OH}	4.90	4.97	–	
V_{CC} = 0 V, V_{EE} = –5.0 V, R_L = 1.0 MΩ	V_{OL}	–	–4.96	–4.90	
V_{CC} = +2.0 V, V_{EE} = 0 V, R_L = 1.0 MΩ	V_{OH}	1.90	1.98	–	
V_{CC} = 0 V, V_{EE} = –2.0 V, R_L = 1.0 MΩ	V_{OL}	–	–1.97	–1.90	
Awakemode					
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 600 Ω	V_{OH}	4.75	4.86	–	
V_{CC} = 0 V, V_{EE} = –5.0 V, R_L = 600 Ω	V_{OL}	–	–4.85	–4.75	
V_{CC} = +2.0 V, V_{EE} = 0 V, R_L = 600 Ω	V_{OH}	1.85	1.91	–	
V_{CC} = 0 V, V_{EE} = –2.0 V, R_L = 600 Ω	V_{OL}	–	–1.90	–1.85	
V_{CC} = +2.5 V, V_{EE} = –2.5 V, R_L = 600 Ω	V_{OH}	–	2.41	–	
V_{CC} = +2.5 V, V_{EE} = –2.5 V, R_L = 600 Ω	V_{OL}	–	–2.40	–	
Common Mode Rejection Ratio	CMRR	60	90	–	dB
Power Supply Current (per Amplifier)	I_D				µA
Sleepmode					
V_{CC} = +2.0 V, V_{EE} = 0 V T_A = +25°C		–	85	–	
V_{CC} = +2.5 V, V_{EE} = –2.5 V T_A = +25°C		–	110	140	
T_A = –40° to +105°C		–	–	150	
V_{CC} = +12 V, V_{EE} = 0 V T_A = +25°C		–	125	–	
Awakemode					
V_{CC} = +2.5 V, V_{EE} = –2.5 V T_A = +25°C		–	1200	1625	
T_A = –40° to +105°C		–	–	1750	
Thermal Resistance	θ_{JA}				°C/W
SOIC		–	145	–	
Plastic DIP		–	75	–	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 V, V_{EE} = –6.0 V, R_L = 600 Ω, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{CC} = +2.5 V, V_{EE} = –2.5 V, A_V = +1.0) (Note 6)	SR				V/µs
Awakemode		0.5	0.89	–	
Gain Bandwidth Product (f = 100 kHz)	GBW				MHz
Awakemode		–	2.2	–	
Gain Margin (C_L = 0 pF)	A_m				dB
Awakemode		–	6.0	–	
Sleepmode (R_L = 1.0 kΩ)		–	9.0	–	
Phase Margin (R_L = 1.0 kΩ, V_O = 0 V, C_L = 0 pF)	ϕ_m				Deg
Awakemode		–	40	–	
Sleepmode		–	60	–	
Sleepmode to Awakemode Transition Time	t_{tr1}				µsec
R_L = 600 Ω		–	4.0	–	
R_L = 10 k		–	12	–	
Awakemode to Sleepmode Transition Time	t_{tr2}	–	1.5	–	sec
Channel Separation (f = 1.0 kHz)	CS				dB
Awakemode		–	100	–	

NOTES: 1. The differential input voltage of each amplifier is limited by two internal diodes. The diodes are connected across the inputs in parallel and opposite to each other. For more differential input voltage range, use current limiting resistors in series with the input pins.
2. The common–mode input voltage range of each amplifier is limited by diodes connected from the inputs to both power supply rails. Therefore, the voltage on either input must not exceed supply rail by more than ±500 mV.
3. Simultaneous short circuits of two or more amplifiers to the positive or negative rail can exceed the power dissipation ratings and cause eventual failure of the device.
4. Rail–to–rail performance is achieved at the input of the amplifier by using parallel NPN–PNP differential stages. When the inputs are near the negative rail (V_{EE} < V_{CM} < 800 mV), the PNP stage is on. When the inputs are above 800 mV (i.e. 800 mV < V_{CM} < V_{CC}), the NPN stage is on. This switching of the input pairs will cause a reversal of input bias current. Slight changes in the input offset voltage will be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.
5. Power dissipation must be considered to ensure maximum junction (T_J) is not exceeded. (See Figure 2)
6. When connected as a voltage follower and used in transient conditions, a current limiting resistor may be needed between the output and the inverting input. This is because of the back to back diodes clamped across the inputs. The value of this resistor should be between 1.0 kΩ and 10 kΩ. If the amplifier does not become slew rate limited and is processing low frequency waveforms, then no resistor would be necessary. (The output could be tied directly to the negative input.)

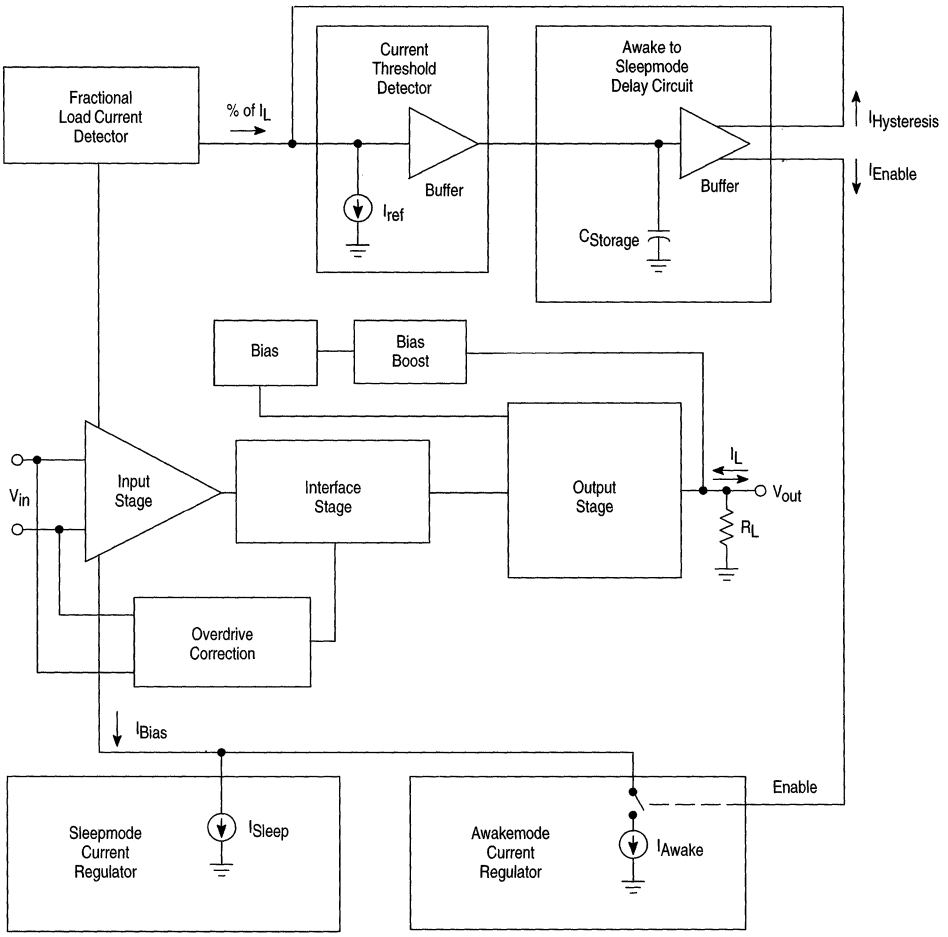
AC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = +6.0 V, V_{EE} = −6.0 V, R_L = 600 Ω, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Bandwidth (V_O = 4.0 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%) Awakemode	BW_p	–	28	–	kHz
Distortion (V_O = 2.0 V_{pp}, A_V = +1.0) Awakemode (f = 10 kHz) Sleepmode (f = 1.0 kHz, R_L = Infinite)	THD	– –	0.009 0.007	– –	%
Open Loop Output Impedance (V_O = 0 V, f = 2.0 MHz, A_V = +10, I_Q = 10 μA) Awakemode Sleepmode	$\|Z_O\|$	– –	100 1000	– –	Ω
Differential Input Impedance (V_{CM} = 0 V) Awakemode Sleepmode	R_{IN}	– –	200 1300	– –	kΩ
Differential Input Capacitance (V_{CM} = 0 V) Awakemode Sleepmode	C_{IN}	– –	8.0 0.4	– –	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz) Awakemode Sleepmode	e_n	– –	15 60	– –	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz) Awakemode Sleepmode	i_n	– –	0.22 0.20	– –	$pA/\sqrt{Hz}$

NOTES: 1. The differential input voltage of each amplifier is limited by two internal diodes. The diodes are connected across the inputs in parallel and opposite to each other. For more differential input voltage range, use current limiting resistors in series with the input pins.
2. The common–mode input voltage range of each amplifier is limited by diodes connected from the inputs to both power supply rails. Therefore, the voltage on either input must not exceed supply rail by more than ±500 mV.
3. Simultaneous short circuits of two or more amplifiers to the positive or negative rail can exceed the power dissipation ratings and cause eventual failure of the device.
4. Rail–to–rail performance is achieved at the input of the amplifier by using parallel NPN–PNP differential stages. When the inputs are near the negative rail (V_{EE} < V_{CM} < 800 mV), the PNP stage is on. When the inputs are above 800 mV (i.e. 800 mV < V_{CM} < V_{CC}), the NPN stage is on. This switching of the input pairs will cause a reversal of input bias current. Slight changes in the input offset voltage will be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.
5. Power dissipation must be considered to ensure maximum junction (T_J) is not exceeded. (See Figure 2)
6. When connected as a voltage follower and used in transient conditions, a current limiting resistor may be needed between the output and the inverting input. This is because of the back to back diodes clamped across the inputs. The value of this resistor should be between 1.0 kΩ and 10 kΩ. If the amplifier does not become slew rate limited and is processing low frequency waveforms, then no resistor would be necessary. (The output could be tied directly to the negative input.)

Figure 1. Equivalent Circuit Block Diagram (Each Amplifier)

2



There are 515 active components for the entire quad device.

DEVICE DESCRIPTION

The MC33304 will begin to function at power supply voltages as low as $V_S = \pm 0.8$ V. The device has the ability to swing rail–to–rail on both the input and the output. Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies. The MC33304 is guaranteed not to latch up or phase reverse over the entire common mode range. However, the output could go into phase reversal state if input voltage is set higher than $+V_{CC}$ or $-V_{EE}$.

When power is initially applied, the part may start to operate in the awakemode. This occurs because of bias currents being generated from the charging of the internal capacitors. When this occurs, the user will have to wait approximately 1.5 seconds before the device will switch back to the sleepmode.

The amplifier is designed to switch from sleepmode to awakemode whenever the output current exceeds a preset current threshold (I_{TH}) of approximately 200 μA. As a result, the output switching threshold voltage (V_{ST}) is controlled by the output loading resistance (R_L). Large valued load resistors require a large output voltage to switch, but reduce unwanted transitions to the awakemode.

Most of the transition time is consumed slewing in the sleepmode until V_{ST} is reached, therefore, small values of R_L allow rapid transition to the awakemode. The output switching threshold voltage (V_{ST}) is higher for the larger values of R_L, requiring the amplifier to slew longer in the slower sleepmode state before switching to the awakemode.

Although typically 200 μA, I_{TH} varies with supply voltage, temperature and the load resistance. Generally, any current loading on the ouput which causes a current greater than I_{TH} to flow will switch the amplifier into the awakemode. This includes transition currents like those generated by charging load capacitances. In fact, the maximum capacitance that can be driven while attempting to remain in the sleepmode is approximately 300 pF.

The awakemode to sleepmode transition time is controlled by an internal delay circuit, which is necessary to prevent the amplifier from going to sleep during every zero crossing of the output waveform. This delay circuit also eliminates the crossover distortion commonly found in micropower amplifiers.

The MC33304 rail–to–rail sleepmode operational amplifier is unique in its ability to swing rail–to–rail on both the input and output using a bipolar design. This offers a low noise and wide common mode input voltage range. Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies.

Rail–to–rail performance is achieved at the input of the amplifiers by using parallel NPN–PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV above V_{EE}, the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents. Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.

In addition to the rail–to–rail performance, the output stage is current boosted to provide enough output current to drive 600 Ω loads. Because of this high current capability, care should be taken not to exceed the 150°C maximum junction temperature specification.

2

Figure 2. Maximum Power Dissipation versus Temperature

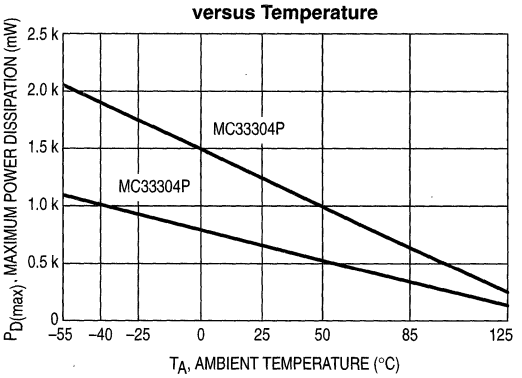


Figure 3. Input Bias Current versus Temperature

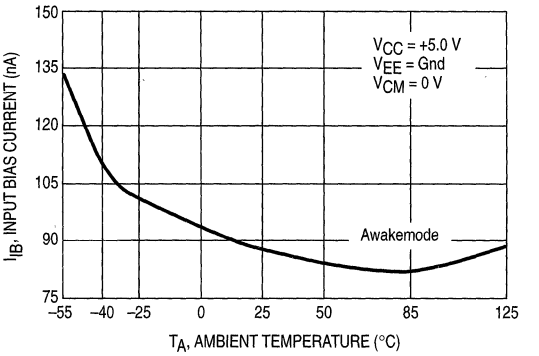


Figure 4. Input Bias Current versus Common Mode Input Voltage

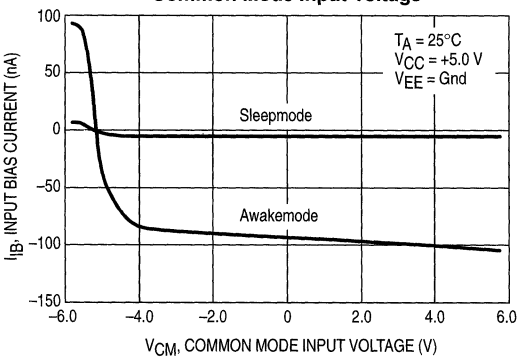


Figure 5. Open Loop Voltage Gain versus Temperature

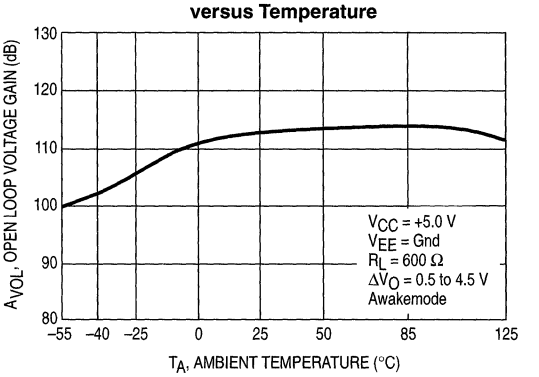


Figure 6. Output Voltage Swing versus Supply Voltage

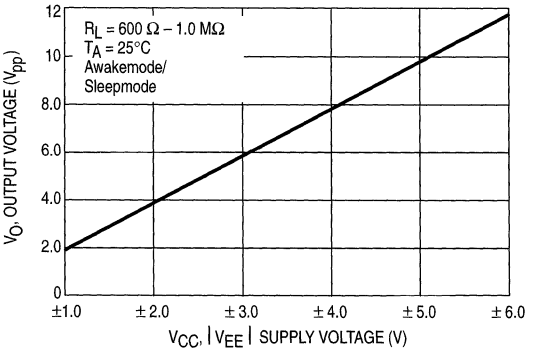


Figure 7. Output Voltage versus Frequency

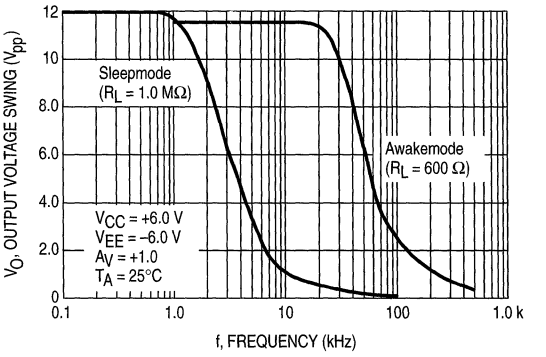


Figure 8. Maximum Peak–to–Peak Output Voltage Swing versus Load Resistance

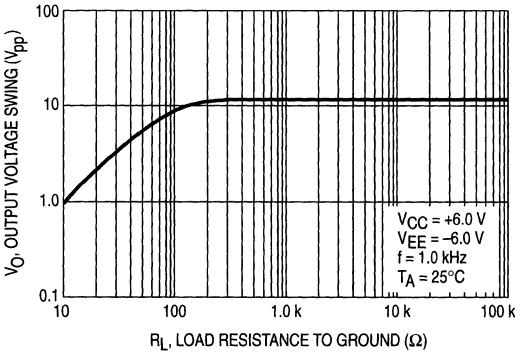


Figure 9. Common Mode Rejection versus Frequency

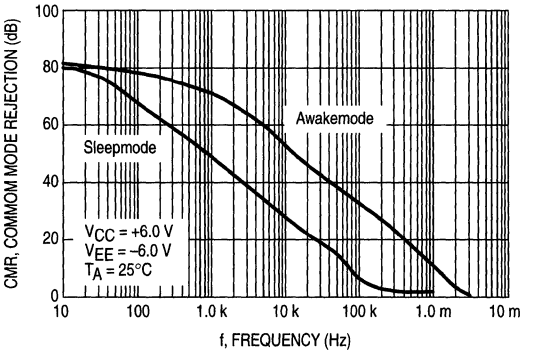


Figure 10. Power Supply Rejection versus Frequency

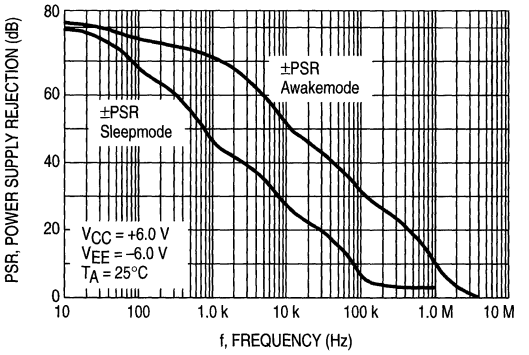


Figure 11. Awakemode to Sleepmode Current Threshold versus Supply Voltage

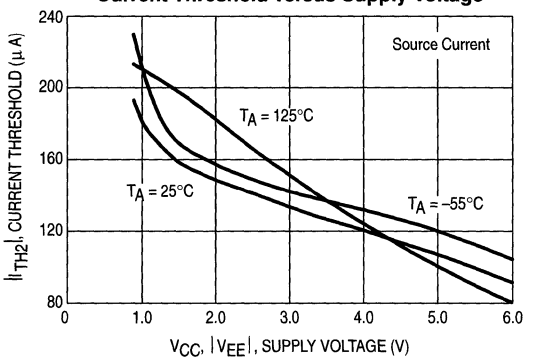


Figure 12. Sleepmode to Awakemode Current Threshold versus Supply Voltage

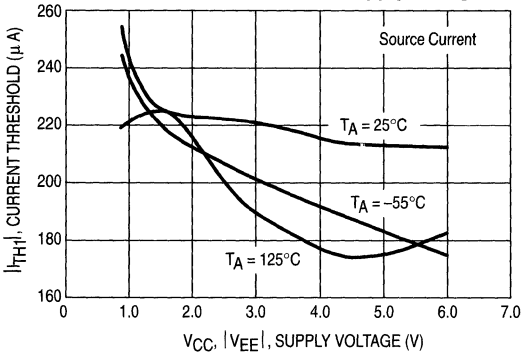
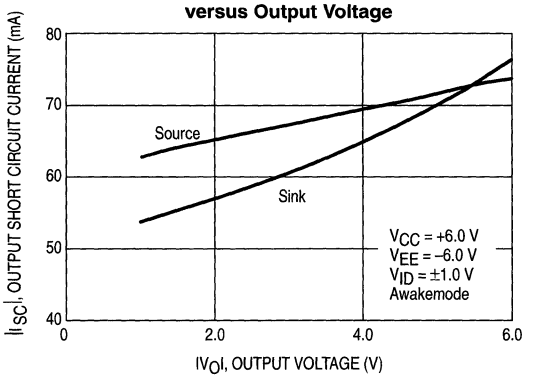


Figure 13. Output Short Circuit Current versus Output Voltage



2

Figure 14. Output Short Circuit Current versus Temperature

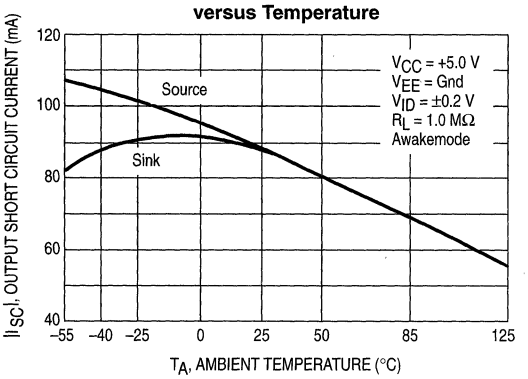


Figure 15. Supply Current versus Supply Voltage with Load

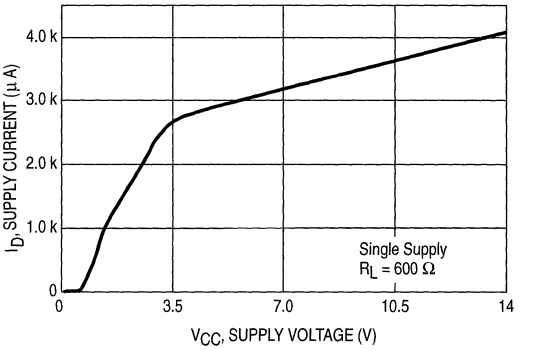


Figure 16. Supply Current versus Supply Voltage

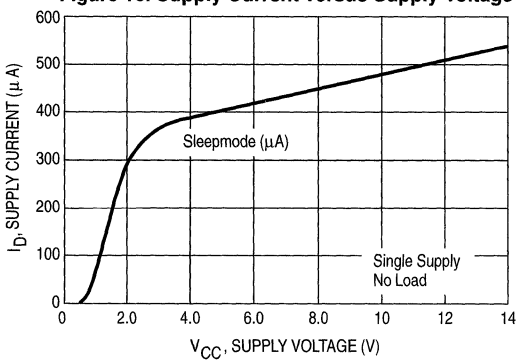


Figure 17. Slew Rate versus Temperature

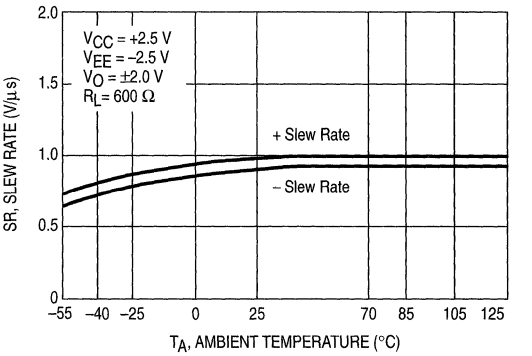


Figure 18. Gain Bandwidth Product versus Temperature

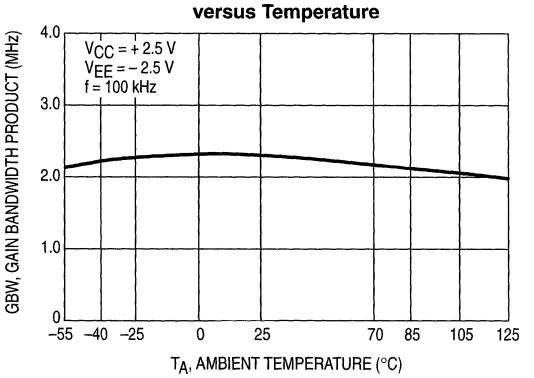


Figure 19. Gain Margin versus Differential Source Resistance

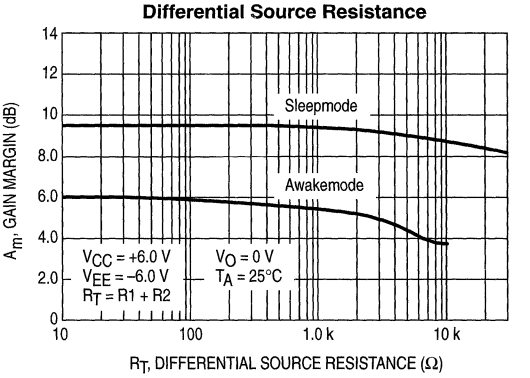


Figure 20. Phase Margin versus Differential Source Resistance

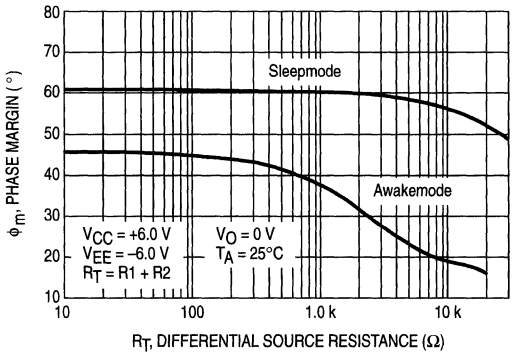


Figure 21. Gain Margin versus Output Load Capacitance

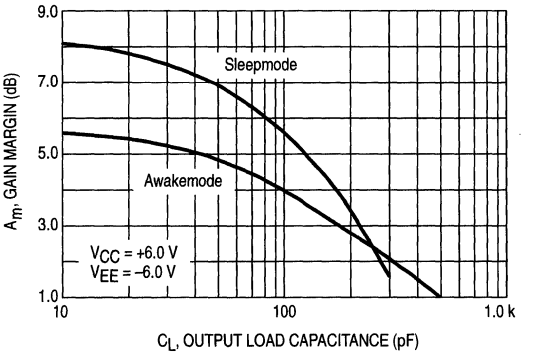


Figure 22. Phase Margin versus Output Load Capacitance

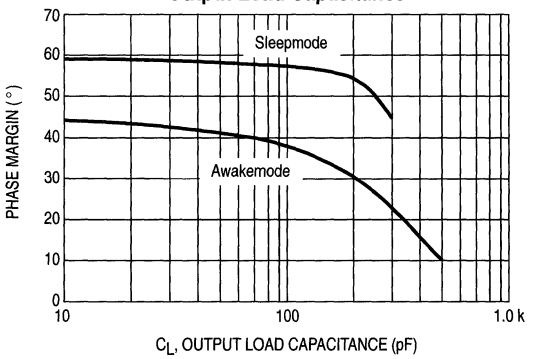


Figure 23. Channel Separation versus Frequency

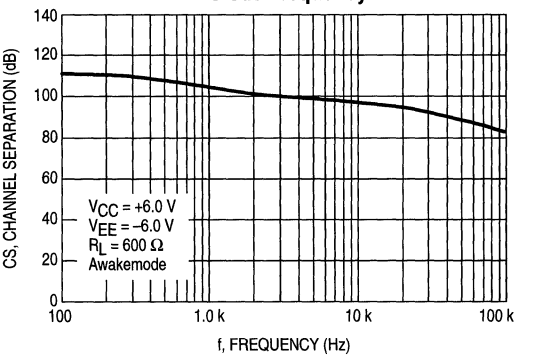


Figure 24. Total Harmonic Distortion versus Frequency

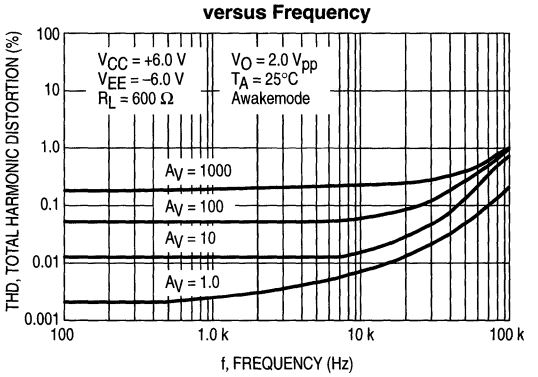
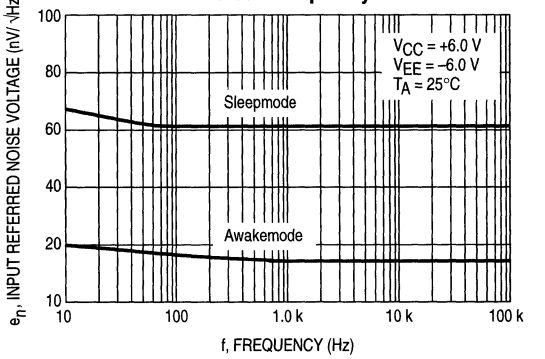


Figure 25. Input Referred Noise Voltage versus Frequency



2

Figure 26. Current Noise versus Frequency

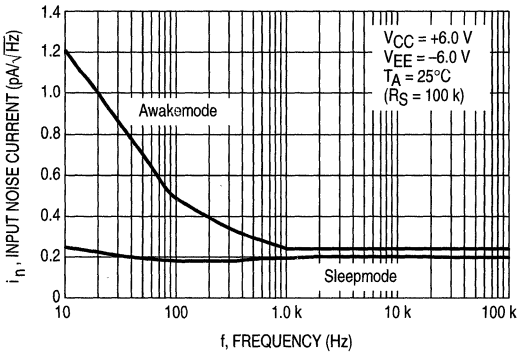
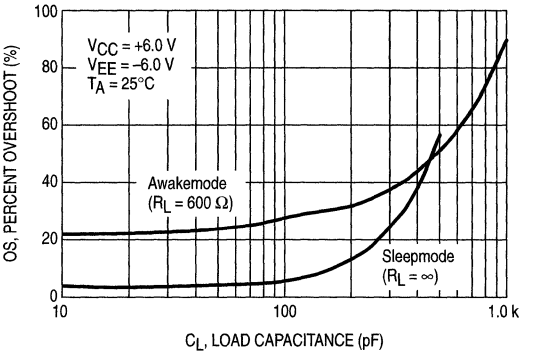


Figure 27. Percent Overshoot versus Load Capacitance



MC34001, B
MC34002, B
MC34004, B

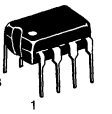
JFET Input Operational Amplifiers

JFET INPUT OPERATIONAL AMPLIFIERS

These low cost JFET input operational amplifiers combine two state–of–the–art analog technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

The Motorola BIFET family offers single, dual and quad operational amplifiers which are pin–compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices. The MC34001/34002/34004 series are specified from 0° to +70°C.

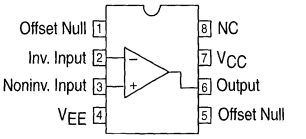
- Input Offset Voltage Options of 5.0 mV and 10 mV Maximum
- Low Input Bias Current: 40 pA
- Low Input Offset Current: 10 pA
- Wide Gain Bandwidth: 4.0 MHz
- High Slew Rate: 13 V/μs
- Low Supply Current: 1.4 mA per Amplifier
- High Input Impedance: $10^{12}\ \Omega$
- High Common Mode and Supply Voltage Rejection Ratios: 100 dB
- Industry Standard Pinouts



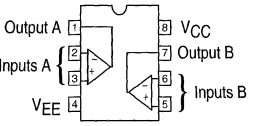
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

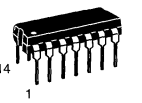
PIN CONNECTIONS



MC34001 (Top View)

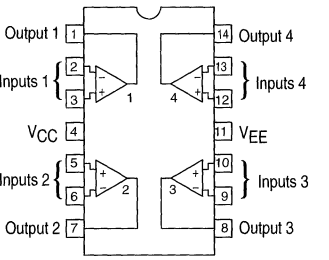


MC34002 (Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



MC34004 (Top View)

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	MC34001BD, D	T_A = 0° to+ 70°C	SO–8
	MC34001BP, P		Plastic DIP
Dual	MC34002BD, D	T_A = 0° to +70°C	SO–8
	MC34002BP, P		Plastic DIP
Quad	MC34004BP, P	T_A = 0° to +70°C	Plastic DIP

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{EE}	±18	V
Differential Input Voltage (Note 1)	V_{ID}	±30	V
Input Voltage Range	V_{IDR}	±16	V
Open Short Circuit Duration	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ k) MC3400XB MC3400X	V_{IO}	 — —	 3.0 5.0	 5.0 10	mV
Average Temperature Coefficient of Input Offset Voltage $R_S \le 10$ k, $T_A = T_{low}$ to T_{high} (Note 2)	$\Delta V_{IO}/\Delta T$	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0) (Note 3) MC3400XB MC3400X	I_{IO}	 — —	 25 25	 100 100	pA
Input Bias Current (V_{CM} = 0) (Note 3) MC3400XB MC3400X	I_{IB}	 — —	 50 50	 200 200	pA
Input Resistance	r_i	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}	±11 —	+15 –12	— —	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k) MC3400XB MC3400X	A_{VOL}	 50 25	 150 100	 — —	V/mV
Output Voltage Swing ($R_L \ge 10$ k) ($R_L \ge 2.0$ k)	V_O	 ±12 ±10	 ±14 ±13	 — —	V
Common Mode Rejection Ratio ($R_S \le 10$ k) MC3400XB MC3400X	CMRR	 80 70	 100 100	 — —	dB
Supply Voltage Rejection Ratio ($R_S \le 10$ k) (Note 4) MC3400XB MC3400X	PSRR	 80 70	 100 100	 — —	dB
Supply Current (Each Amplifier) MC3400XB MC3400X	I_D	 — —	 1.4 1.4	 2.5 2.7	mA
Slew Rate (A_V = 1.0)	SR	—	13	—	V/µs
Gain–Bandwidth Product	GBW	—	4.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1000 Hz)	e_n	—	25	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1000 Hz)	i_n	—	0.01	—	$pA/\sqrt{Hz}$

NOTES: 2. T_{low} = 0°C for MC34001/34001B, MC34002, MC34004/34004B; T_{high} = +70°C for MC34001/34001B, MC34002, MC34004/34004B

3. The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heatsink is recommended if input bias current is to be kept to a minimum.

4. Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 2].)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}				mV
MC3400XB		—	—	7.0	
MC3400X		—	—	13	
Input Offset Current (V_{CM} = 0) (Note 3)	I_{IO}				nA
MC3400XB		—	—	4.0	
MC3400X		—	—	4.0	
Input Bias Current (V_{CM} = 0) (Note 3)	I_{IB}				nA
MC3400XB		—	—	8.0	
MC3400X		—	—	8.0	
Common Mode Input Voltage Range	V_{ICR}	±11	—	—	V
Large Signal (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}				V/mV
MC3400XB		25	—	—	
MC3400X		15	—	—	
Output Voltage Swing	V_O				V
(R ≥ 10 k)		±12	—	—	
(R ≥ 2.0 k)		±10	—	—	
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR				dB
MC3400XB		80	—	—	
MC3400X		70	—	—	
Supply Voltage Rejection Ratio ($R_S \leq 10$ k) (Note 4)	PSRR				dB
MC3400XB		80	—	—	
MC3400X		70	—	—	
Supply Current (Each Amplifier)	I_D				mA
MC3400XB		—	—	2.8	
MC3400X		—	—	3.0	

NOTES: 2. T_{low} = 0°C for MC34001/34001B, MC34002, MC34004/34004B; T_{high} = +70°C for MC34001/34001B, MC34002, MC34004/34004B

3. The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heatsink is recommended if input bias current is to be kept to a minimum.
4. Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

2

Figure 1. Input Bias Current versus Temperature

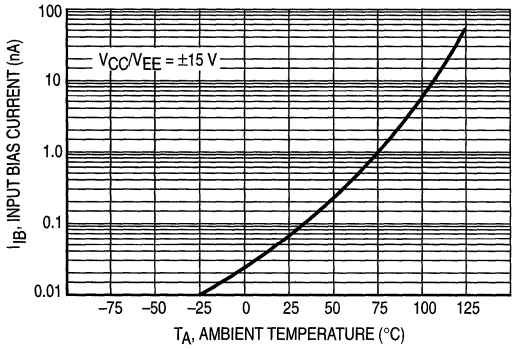


Figure 2. Output Voltage Swing versus Frequency

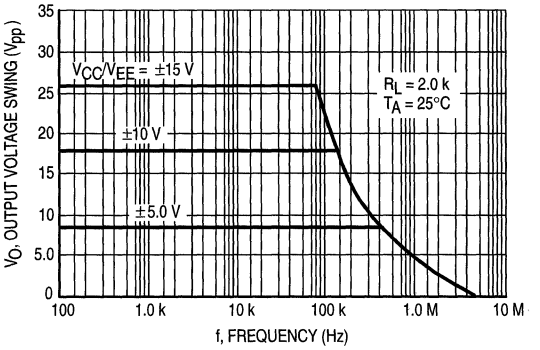


Figure 3. Output Voltage Swing versus Load Resistance

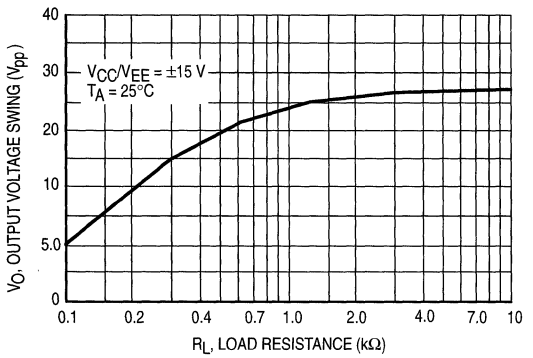


Figure 4. Output Voltage Swing versus Supply Voltage

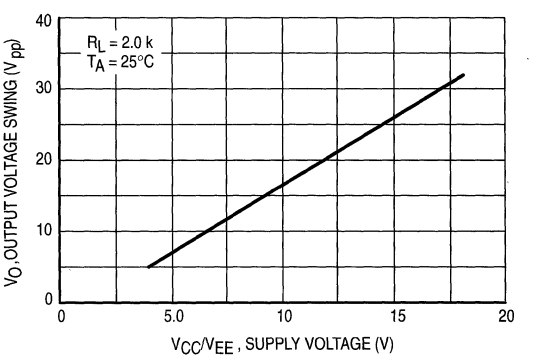


Figure 5. Output Voltage Swing versus Temperature

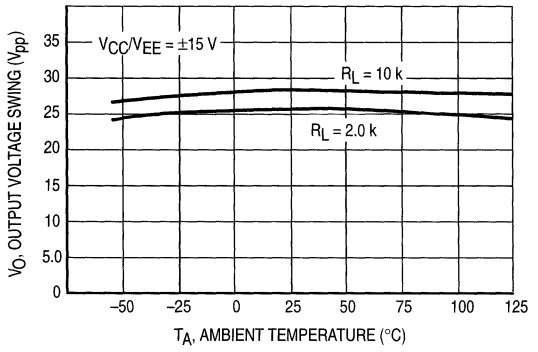


Figure 6. Supply Current per Amplifier versus Temperature

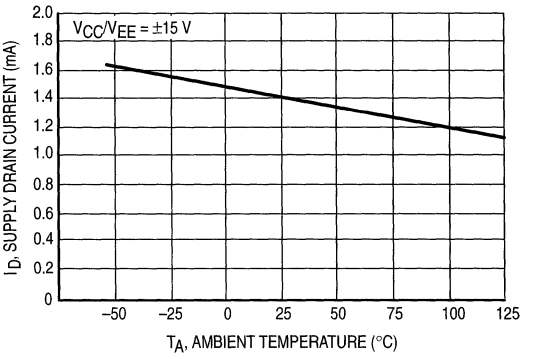


Figure 7. Large–Signal Voltage Gain and Phase Shift versus Frequency

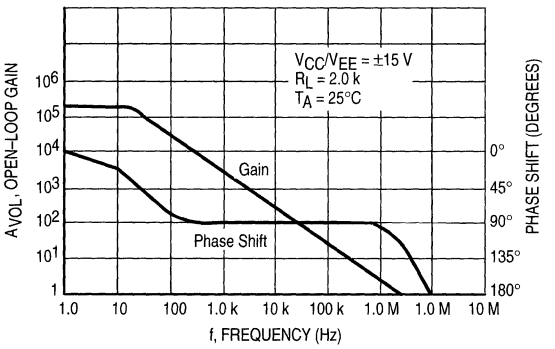


Figure 8. Large–Signal Voltage Gain versus Temperature

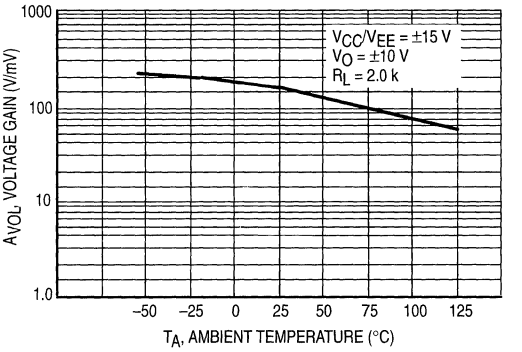


Figure 9. Normalized Slew Rate versus Temperature

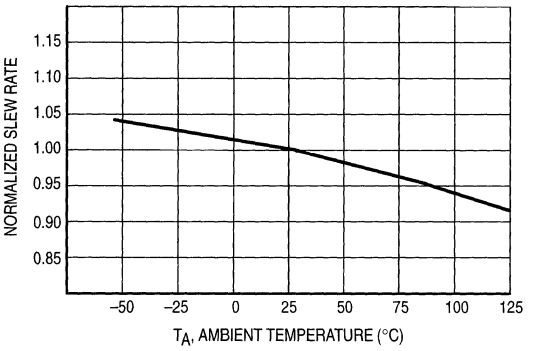


Figure 10. Equivalent Input Noise Voltage versus Frequency

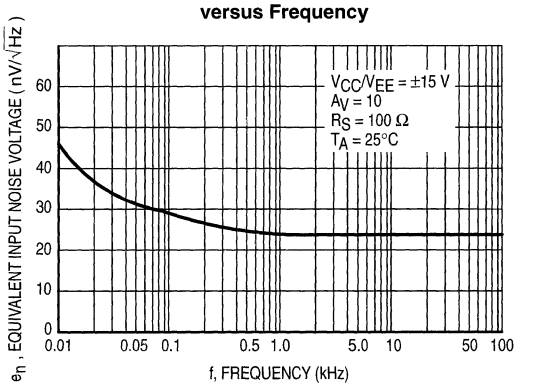
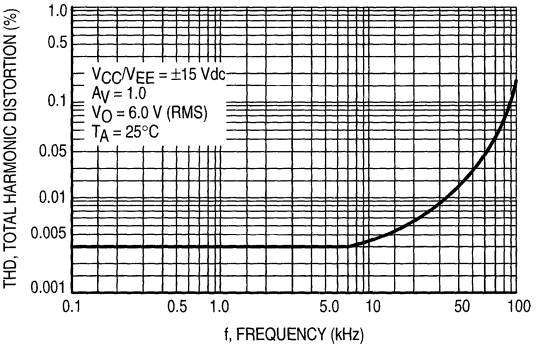


Figure 11. Total Harmonic Distortion versus Frequency



2

Representative Circuit Schematic
(Each Amplifier)

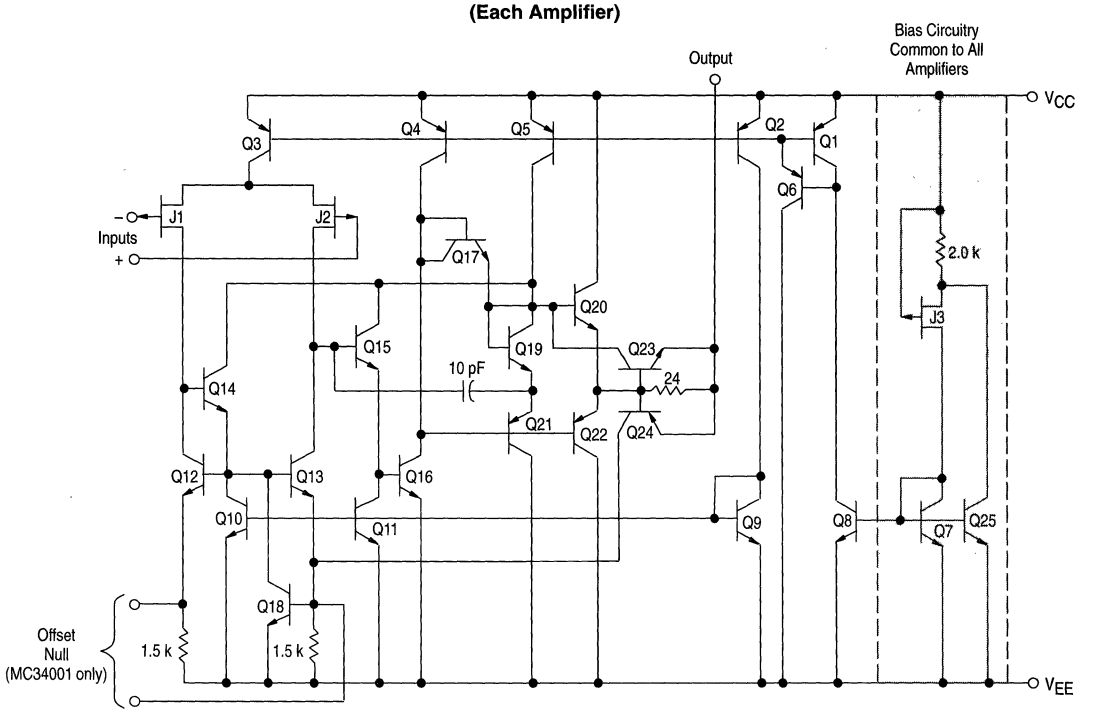
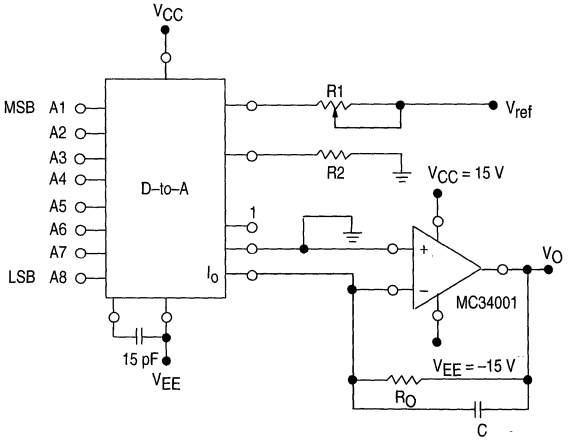


Figure 12. Output Current to Voltage Transformation for a D–to–A Converter



Settling time to within 1/2 LSB is approximately 4.0 μs from the time all bits are switched (C = 68 pF).

The value of C may be selected to minimize overshoot and ringing.

Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Figure 13. Positive Peak Detector

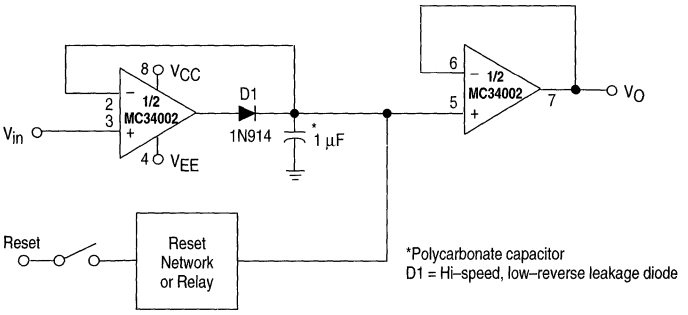
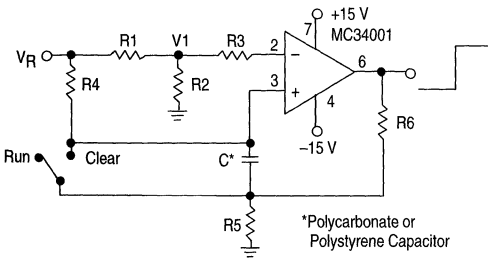


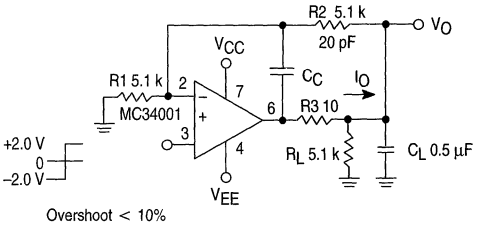
Figure 14. Long Interval RC Timer



Time (t) = R4 Cn ($V_R/V_R–V_I$), $R_3 = R_4$, $R_5 = 0.1\ R_6$
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer
V_R = 10 V C = I.0 µF R3 = R4 = 144 M
R6 = 20 k R5 = 2.0 k R1 = R2 = 1.0 k

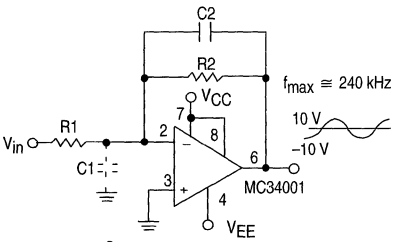
Figure 15. Isolating Large Capacitive Loads



Overshoot < 10%
t_s = 10 µs
When driving large C_L, the V_O slew rate is determined by C_L and $I_{O(max)}$:

$$\frac{\Delta V_O}{\Delta t} = \frac{I_O}{C_L} = \frac{0.02}{0.5}\ \text{V/µs} = 0.04\ \text{V/µs (with } C_L \text{ shown)}$$

Figure 16. Wide BW, Low Noise, Low Drift Amplifier



Power BW: $f_{max} = \frac{S_r}{2\pi V_p} \cong 240\ \text{kHz}$

Parasitic input capacitance (C1 ≅ 3.0 pF plus any additional layout capacitance) interacts with feedback elements and creates undesirable high–frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

MC34071,2,4,A
MC33071,2,4,A

High Slew Rate, Wide Bandwidth, Single Supply Operational Amplifiers

HIGH BANDWIDTH SINGLE SUPPLY OPERATIONAL AMPLIFIERS

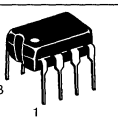
Quality bipolar fabrication with innovative design concepts are employed for the MC33071/72/74, MC34071/72/74 series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/μs slew rate and fast setting time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With A Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33071/72/74, MC34071/72/73 series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic DIP and SOIC surface mount packages.

- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.1%
- Wide Single Supply Operation: 3.0 V to 44 V
- Wide Input Common Mode Voltage Range: Includes Ground (V_{EE})
- Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: −14.7 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 10,000 pF
- Low Total Harmonic Distortion: 0.02%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 12 dB
- Output Short Circuit Protection
- ESD Diodes/Clamps Provide Input Protection for Dual and Quad

ORDERING INFORMATION

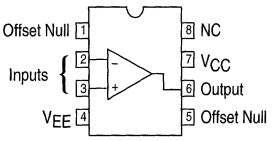
Op Amp Function	Device	Operating Temperature Range	Package
Single	MC34071P, AP MC34071D, AD	T_A = 0° to +70°C	Plastic DIP SO–8
	MC33071P, AP MC33071D, AD	T_A = −40° to +85°C	Plastic DIP SO–8
Dual	MC34072P, AP MC34072D, AD	T_A = 0° to +70°C	Plastic DIP SO–8
	MC33072P, AP MC33072D, AD	T_A = −40° to +85°C	Plastic DIP SO–8
Quad	MC34074P, AP MC34074D, AD	T_A = 0° to +70°C	Plastic DIP SO–14
	MC33074P, AP MC33074D, AD	T_A = −40° to +85°C	Plastic DIP SO–14



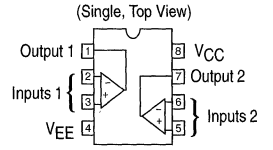
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

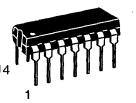
PIN CONNECTIONS



(Single, Top View)



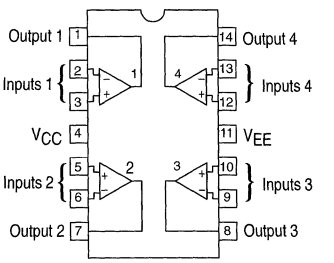
(Dual, Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



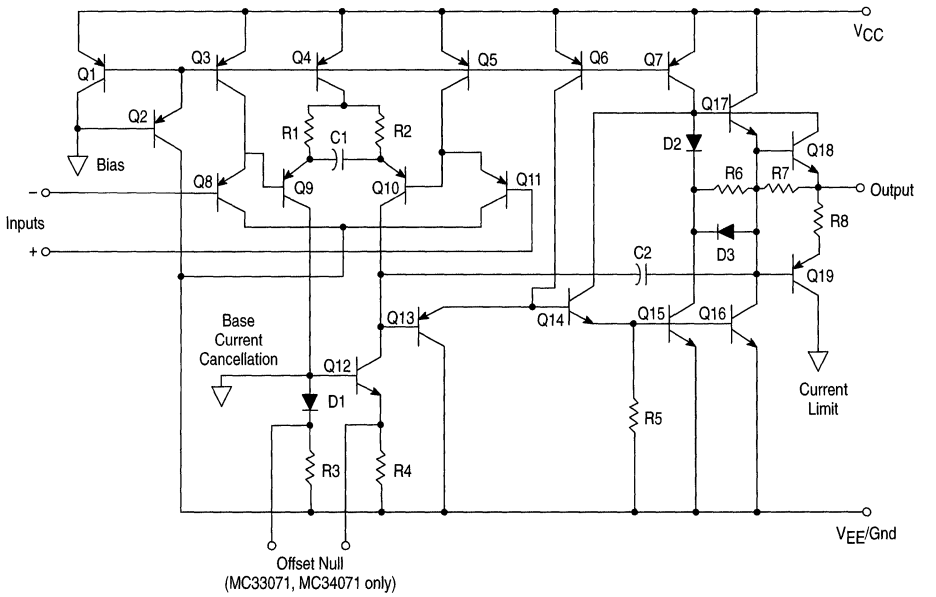
(Quad, Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{EE} to V_{CC})	V_S	+44	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C

NOTES: 1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

Representative Schematic Diagram
(Each Amplifier)



2

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground, unless otherwise noted. See Note 3 for $T_A = T_{low}$ to T_{high})

Characteristics	Symbol	A Suffix Min	A Suffix Typ	A Suffix Max	Non-Suffix Min	Non-Suffix Typ	Non-Suffix Max	Unit
Input Offset Voltage (R_S = 100 Ω, V_{CM} = 0 V, V_O = 0 V)	V_{IO}							mV
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		—	0.5	3.0	—	1.0	5.0	
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	0.5	3.0	—	1.5	5.0	
V_{CC} = +15 V, V_{EE} = −15 V, $T_A = T_{low}$ to T_{high}			—	5.0		—	7.0	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, $T_A = T_{low}$ to T_{high}								
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}							nA
T_A = +25°C		—	100	500	—	100	500	
$T_A = T_{low}$ to T_{high}		—	—	700	—	—	700	
Input Offset Current (V_{CM} = 0 V, V_O = 0V)	I_{IO}							nA
T_A = +25°C		—	6.0	50	—	6.0	75	
$T_A = T_{low}$ to T_{high}		—	—	300	—	—	300	
Input Common Mode Voltage Range	V_{ICR}							V
T_A = +25°C		V_{EE} to (V_{CC} −1.8)			V_{EE} to (V_{CC} −1.8)			
$T_A = T_{low}$ to T_{high}		V_{EE} to (V_{CC} −2.2)			V_{EE} to (V_{CC} −2.2)			
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}							V/mV
T_A = +25°C		50	100	—	25	100	—	
$T_A = T_{low}$ to T_{high}		25	—	—	20	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	V_{OH}							V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C		3.7	4.0	—	3.7	4.0	—	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ, T_A = +25°C		13.6	14	—	13.6	14	—	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kΩ, $T_A = T_{low}$ to T_{high}		13.4	—	—	13.4	—	—	
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C	V_{OL}	—	0.1	0.3	—	0.1	0.3	V
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ, T_A = +25°C		—	−14.7	−14.3	—	−14.7	−14.3	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kΩ, $T_A = T_{low}$ to T_{high}		—	—	−13.5	—	—	−13.5	
Output Short Circuit Current (V_{ID} = 1.0 V, V_O = 0 V, T_A = 25°C)	I_{SC}							mA
Source		10	30	—	10	30	—	
Sink		20	30	—	20	30	—	
Common Mode Rejection	CMR	80	97	—	70	97	—	dB
$R_S \leq$ 10 kΩ, $V_{CM} = V_{ICR}$, T_A = 25°C								
Power Supply Rejection (R_S = 100 Ω)	PSR	80	97	—	70	97	—	dB
V_{CC}/V_{EE} = +16.5 V/−16.5 V to +13.5 V/−13.5 V, T_A = 25°C								
Power Supply Current (Per Amplifier, No Load)	I_D							mA
V_{CC} = +5.0 V, V_{EE} = 0 V, V_O = +2.5 V, T_A = +25°C		—	1.6	2.0	—	1.6	2.0	
V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, T_A = +25°C		—	1.9	2.5	—	1.9	2.5	
V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, $T_A = T_{low}$ to T_{high}		—	—	2.8	—	—	2.8	

NOTES: 3. T_{low} = −40°C for MC33071, 2, 4, /A; = 0°C for MC34071, 2, 4, /A. T_{high} = +85°C for MC33071, 2, 4, /A; = +70°C for MC34071, 2, 4, /A.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground. T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	A Suffix			Non–Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 500 pF) A_V = +1.0 A_V = −1.0	SR	 8.0 —	 10 13	 — —	 8.0 —	 10 13	 — —	V/μs
Setting Time (10 V Step, A_V = −1.0) To 0.1% (+1/2 LSB of 9–Bits) To 0.01% (+1/2 LSB of 12–Bits)	t_s	 — —	 1.1 2.2	 — —	 — —	 1.1 2.2	 — —	μs
Gain Bandwidth Product (f = 100 kHz)	GBW	3.5	4.5	—	3.5	4.5	—	MHz
Power Bandwidth A_V = +1.0, R_L = 2.0 kΩ, V_O = 20 V_{pp}, THD = 5.0%	BW	—	160	—	—	160	—	kHz
Phase margin R_L = 2.0 kΩ R_L = 2.0 kΩ, C_L = 300 pF	f_m	 — —	 60 40	 — —	 — —	 60 40	 — —	Deg
Gain Margin R_L = 2.0 kΩ R_L = 2.0 kΩ, C_L = 300 pF	A_m	 — —	 12 4.0	 — —	 — —	 12 4.0	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	32	—	—	32	—	nV/√Hz
Equivalent Input Noise Current f = 1.0 kHz	i_n	—	0.22	—	—	0.22	—	pA/√Hz
Differential Input Resistance V_{CM} = 0 V	R_{in}	—	150	—	—	150	—	MΩ
Differential Input Capacitance V_{CM} = 0 V	C_{in}	—	2.5	—	—	2.5	—	pF
Total Harmonic Distortion A_V = +10, R_L = 2.0 kΩ, 2.0 $V_{pp} \le V_O \le$ 20 V_{pp}, f = 10 kHz	THD	—	0.02	—	—	0.02	—	%
Channel Separation (f = 10 kHz)	—	—	120	—	—	120	—	dB
Open Loop Output Impedance (f = 1.0 MHz)	$\|Z_O\|$	—	30	—	—	30	—	W

Figure 1. Power Supply Configurations

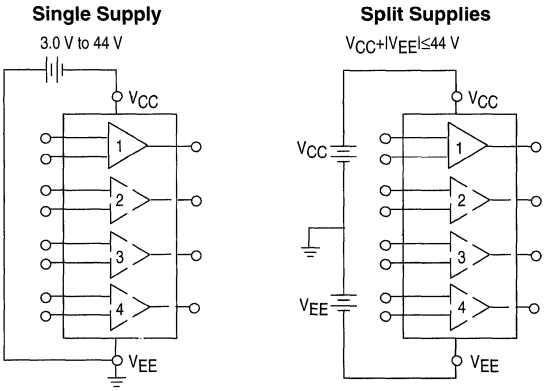
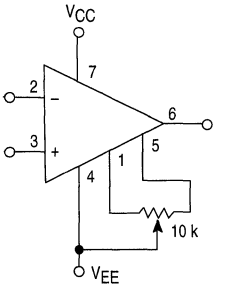


Figure 2. Offset Null Circuit



Offset nulling range is approximately ±80 mV with a 10 k potentiometer (MC33071, MC34071 only).

2

Figure 3. Maximum Power Dissipation versus Temperature for Package Types

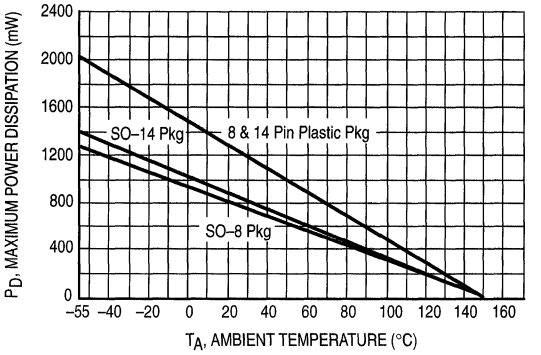


Figure 4. Input Offset Voltage versus Temperature for Representative Units

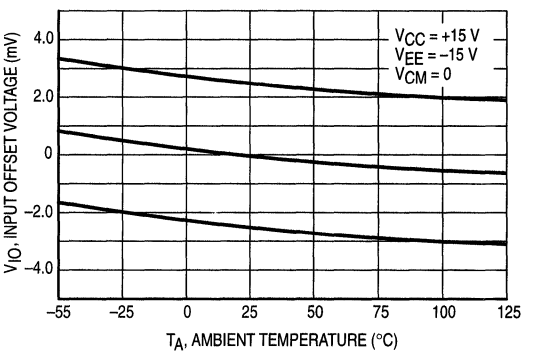


Figure 5. Input Common Mode Voltage Range versus Temperature

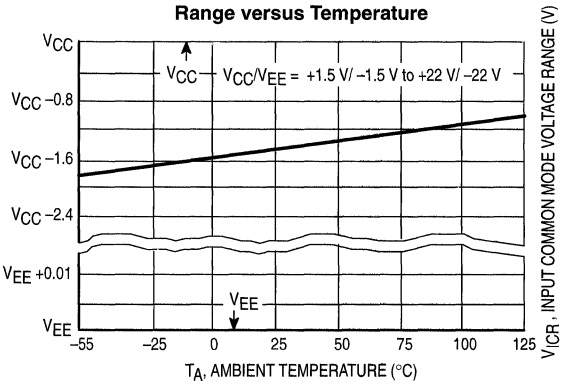


Figure 6. Normalized Input Bias Current versus Temperature

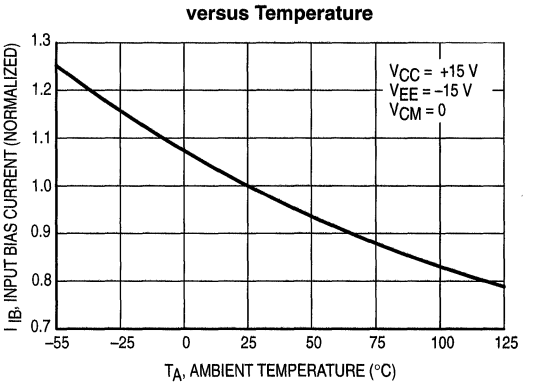


Figure 7. Normalized Input Bias Current versus Input Common Mode Voltage

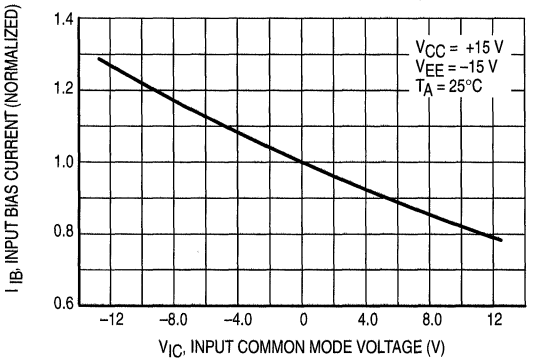


Figure 8. Split Supply Output Voltage Swing versus Supply Voltage

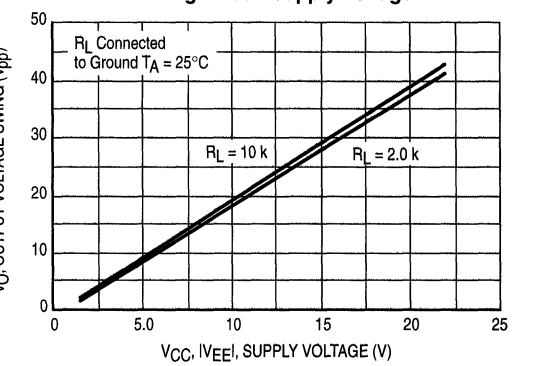


Figure 9. Single Supply Output Saturation versus Load Resistance to V_{CC}

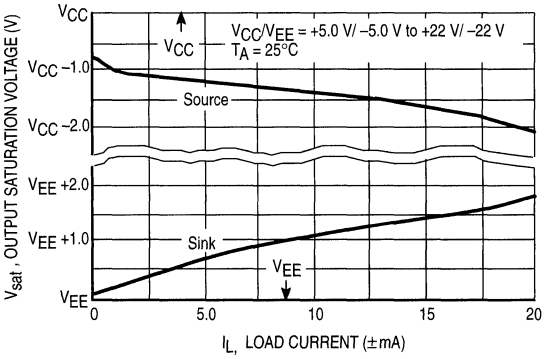


Figure 10. Split Supply Output Saturation versus Load Current

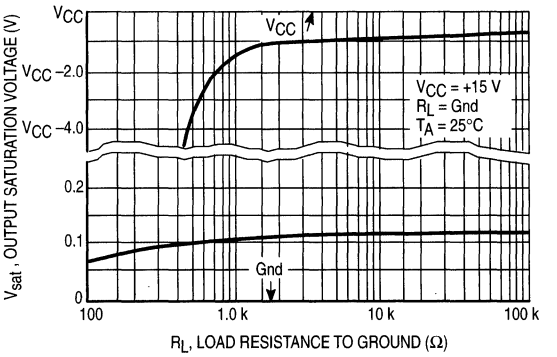


Figure 11. Single Supply Output Saturation versus Load Resistance to Ground

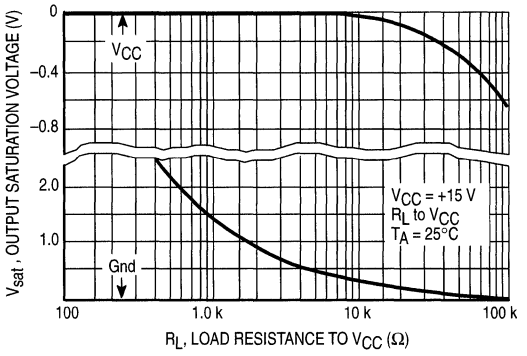


Figure 12. Output Short Circuit Current versus Temperature

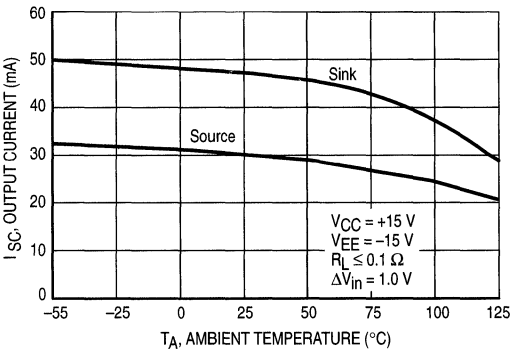


Figure 13. Output Impedance versus Frequency

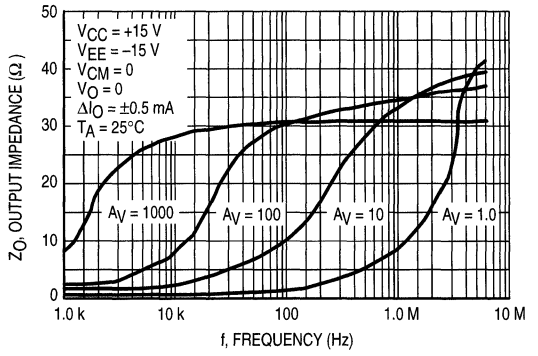
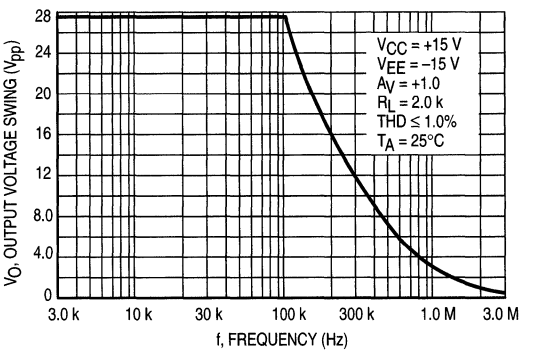


Figure 14. Output Voltage Swing versus Frequency



2

Figure 15. Total Harmonic Distortion versus Frequency

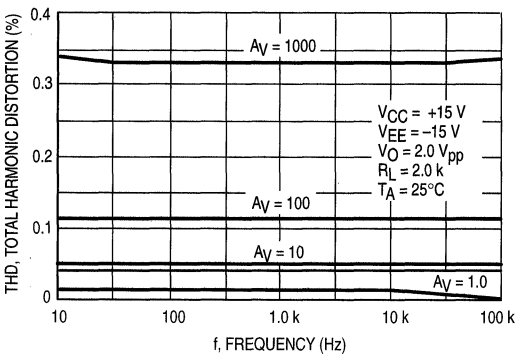


Figure 16. Total Harmonic Distortion versus Output Voltage Swing

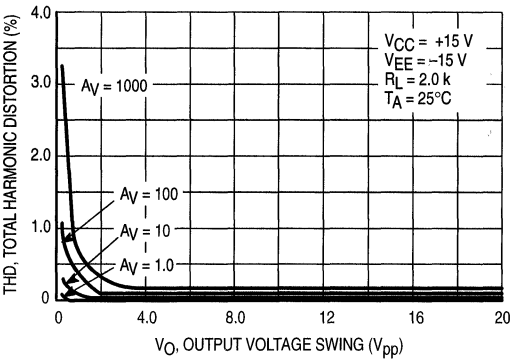


Figure 17. Open Loop Voltage Gain versus Temperature

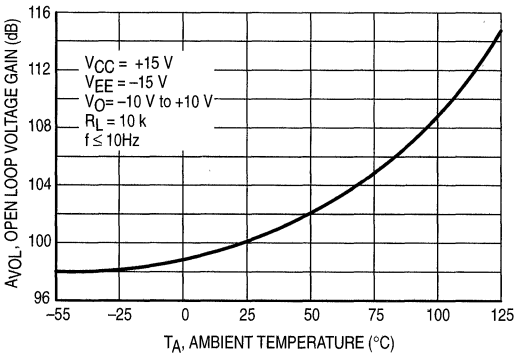


Figure 18. Open Loop Voltage Gain and Phase versus Frequency

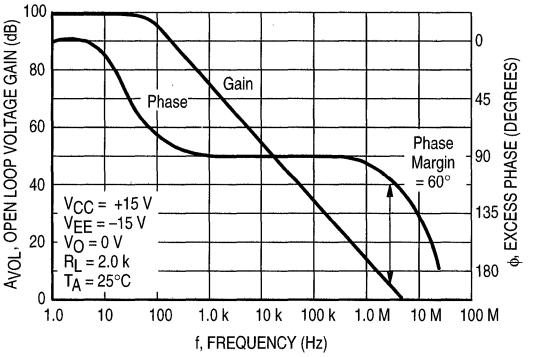


Figure 19. Open Loop Voltage Gain and Phase versus Frequency

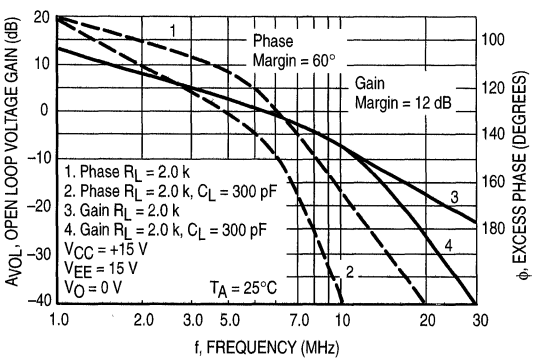


Figure 20. Normalized Gain Bandwidth Product versus Temperature

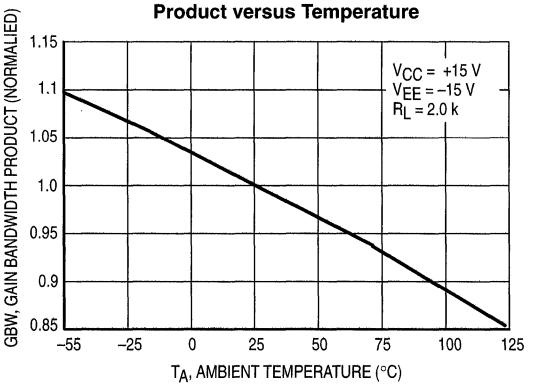


Figure 21. Percent Overshoot versus Load Capacitance

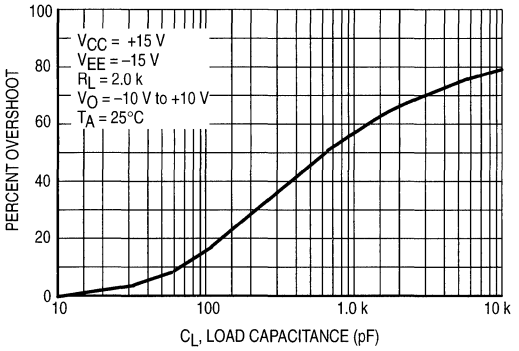


Figure 22. Phase Margin versus Load Capacitance

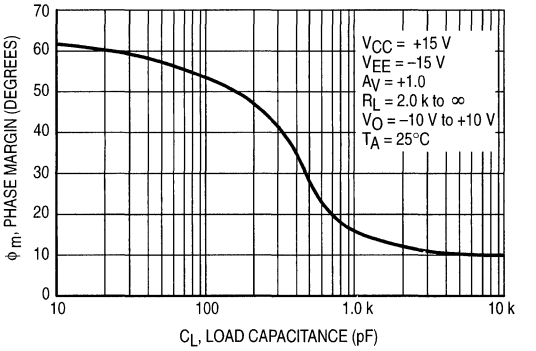


Figure 23. Gain Margin versus Load Capacitance

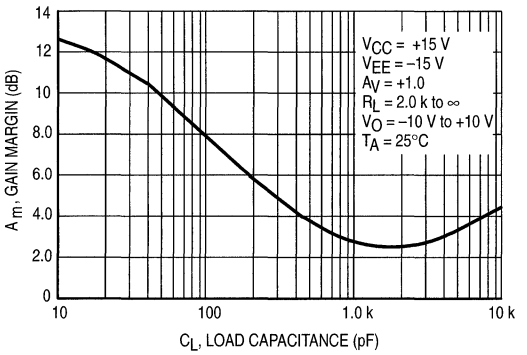


Figure 24. Phase Margin versus Temperature

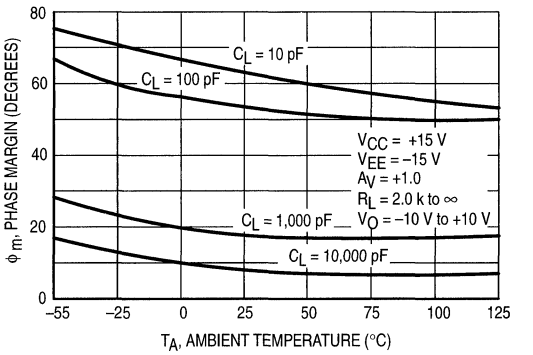


Figure 25. Gain Margin versus Temperature

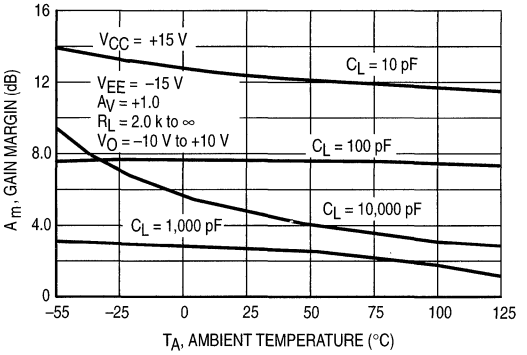
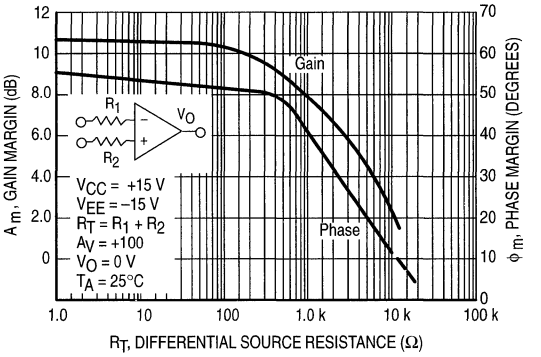


Figure 26. Phase Margin and Gain Margin versus Differential Source Resistance



2

Figure 27. Normalized Slew Rate versus Temperature

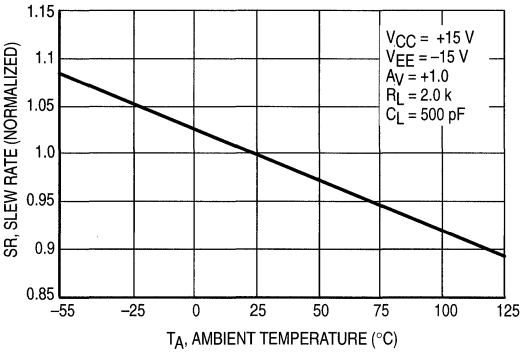


Figure 28. Output Settling Time

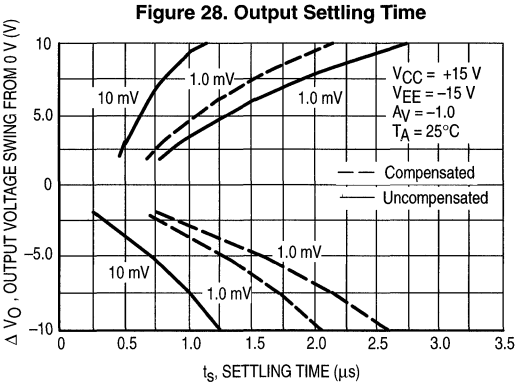


Figure 29. Small Signal Transient Response

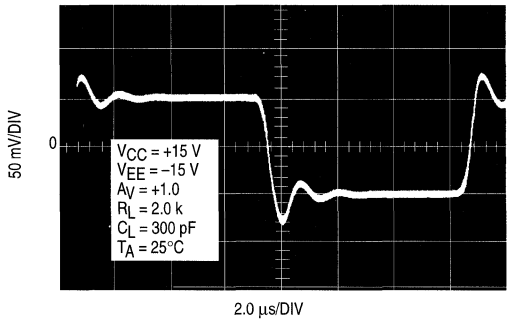


Figure 30. Large Signal Transient Reponse

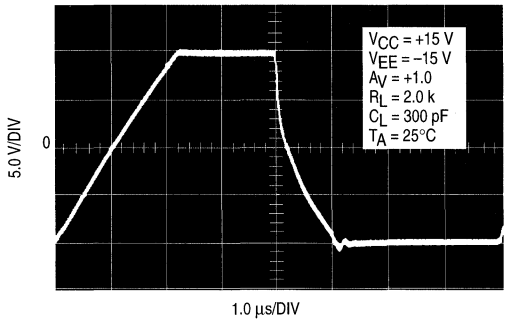


Figure 31. Common Mode Rejection versus Frequency

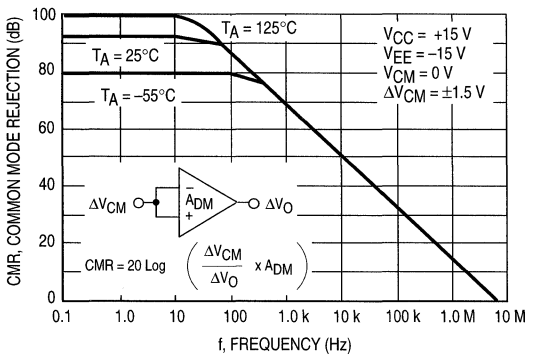


Figure 32. Power Supply Rejection versus Frequency

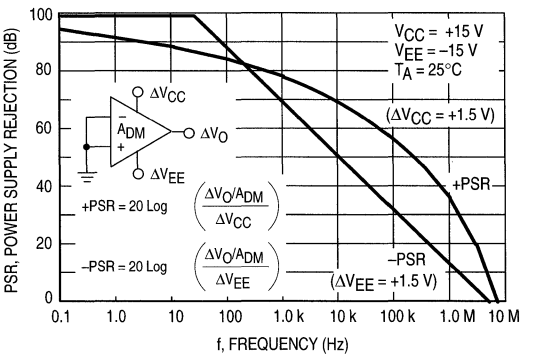


Figure 33. Supply Current versus Supply Voltage

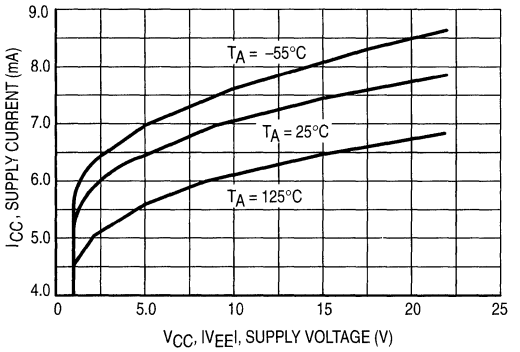


Figure 34. Power Supply Rejection versus Temperature

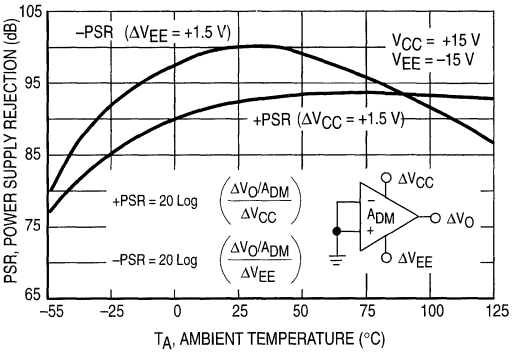


Figure 35. Channel Separation versus Frequency

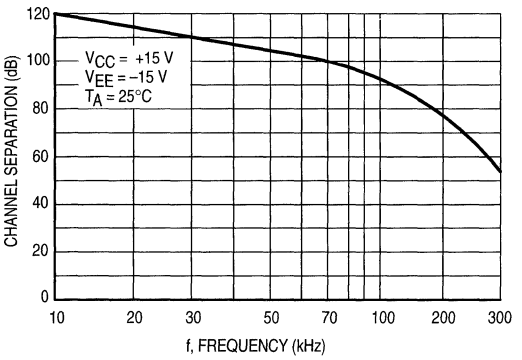
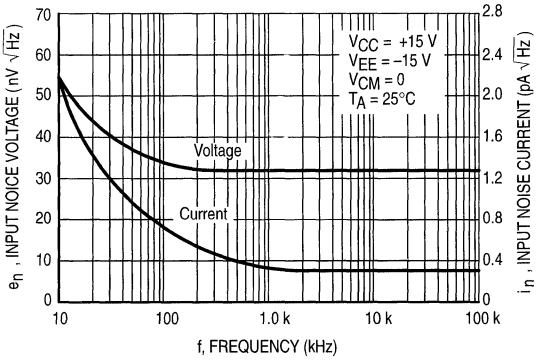


Figure 36. Input Noise versus Frequency



APPLICATIONS INFORMATION
CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC34071 amplifier series are similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{EE} and V_{CC} supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the V_{CC} voltage by approximately 3.0 V and decrease below the V_{EE} voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to approximately 5.0 mA of current from V_{EE} through either inputs clamping diode without damage or latching, although phase reversal may again occur.

If one or both inputs exceed the upper common mode voltage limit, the amplifier output is readily predictable and may be in a low or high state depending on the existing input bias conditions.

Since the input capacitance associated with the small geometry input device is substantially lower (2.5 pF) than the typical JFET input gate capacitance (5.0 pF), better frequency response for a given input source resistance can be achieved using the MC34071 series of amplifiers. This performance feature becomes evident, for example, in fast settling D–to–A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 2.0 kΩ of feedback resistance, the MC34071 series can settle to within 1/2 LSB of 8 bits in 1.0 μs, and within 1/2 LSB of 12–bits in 2.2 μs for a 10 V step. In a inverting unity gain fast settling configuration, the symmetrical slew rate is ±13 V/μs. In the classic noninverting unity gain configuration, the output positive slew rate is +10 V/μs, and the corresponding negative slew rate will exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are superior to that of JFETs, a low untrimmed maximum offset voltage of 3.0 mV prime and 5.0 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low cost precision, high speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can swing within 1.0 V of the positive rail (V_{CC}), and within 0.3 V of the negative rail (V_{EE}), providing a 28.7 V_{pp} swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q_7, and V_{BE} of the NPN pull up transistor Q_{17}, and the voltage drop associated with the short circuit resistance, R_7. The negative swing is limited by the saturation voltage of the pull–down transistor Q_{16}, the voltage drop $I_L R_6$, and the voltage drop associated with resistance R_7, where I_L is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For large valued sink currents (>5.0 mA), diode D3 clamps the voltage across R_6, thus limiting the negative swing to the saturation voltage of Q_{16}, plus the forward diode drop of D3 ($\approx V_{EE}$ +1.0 V). Thus for a given supply voltage, unprecedented peak–to–peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter–follower transistor has been eliminated, the MC34071 series offers a 20 mA minimum current sink capability, typically to an output voltage of (V_{EE} +1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.

In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier's high gain bandwidth product and fast settling capability. The associated high frequency low output impedance (30 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 10,000 pF without oscillation in the unity closed loop gain configuration. The 60° phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the MC34071 series also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specifications is defined at 5.0 V, these amplifiers are functional to 3.0 V @ 25°C although slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input–output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

(Typical Single Supply Applications V_{CC} = 5.0 V)

Figure 37. AC Coupled Noninverting Amplifer

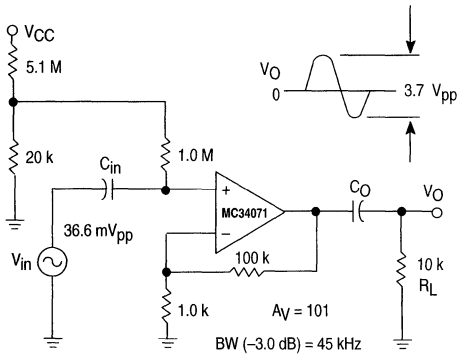


Figure 38. AC Coupled Inverting Amplifier

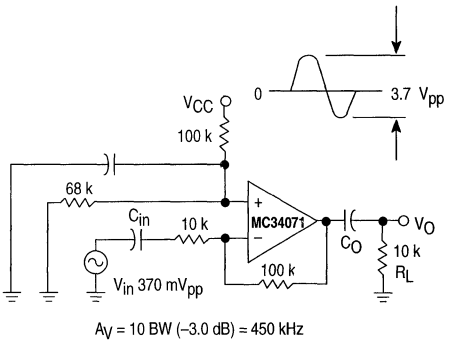


Figure 39. DC Coupled Inverting Amplifer Maximum Output Swing

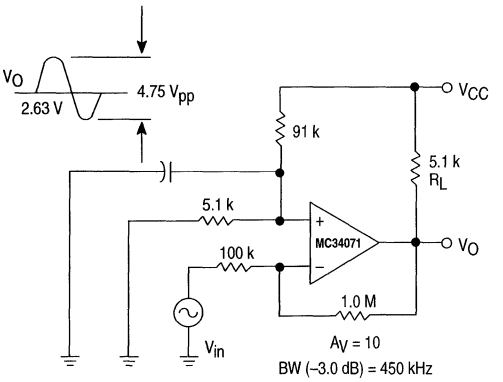


Figure 40. Unity Gain Buffer TTL Driver

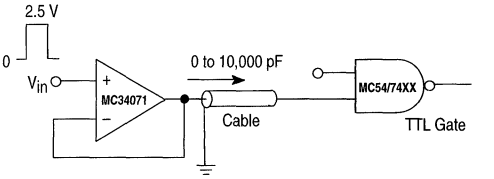


Figure 41. Active High–Q Notch Filter

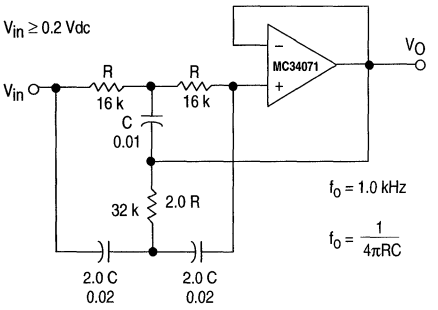
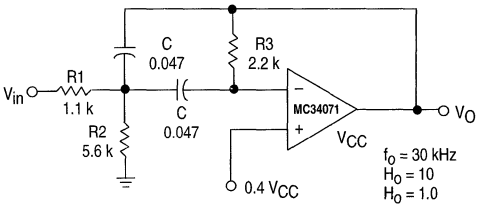


Figure 42. Active Bandpass Filter



Given f_0 = Center Frequency
A_O = Gain at Center Frequency
Choose Value f_0, Q, A_0, C

Then:

$$R3 = \frac{Q}{\pi f_0 C} \qquad R1 = \frac{R3}{2H_0} \qquad R2 = \frac{R1\,R3}{4Q^2R1 - R3}$$

For less than 10% error from operational amplifier $\frac{Q_0 f_0}{GBW} < 0.1$

where f_0 and GBW are expressed in Hz.
GBW = 4.5 MHz Typ.

2

Figure 43. Low Voltage Fast D/A Converter

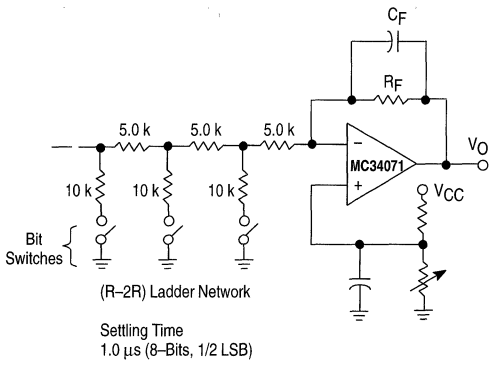


Figure 44. High Speed Low Voltage Comparator

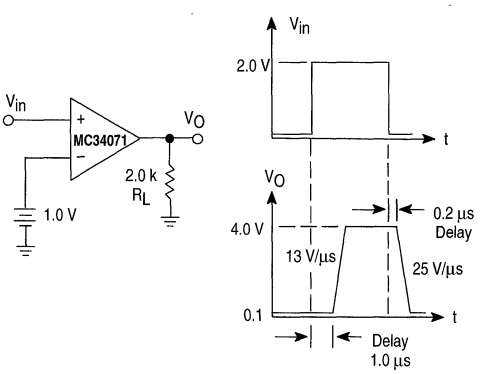


Figure 45. LED Driver

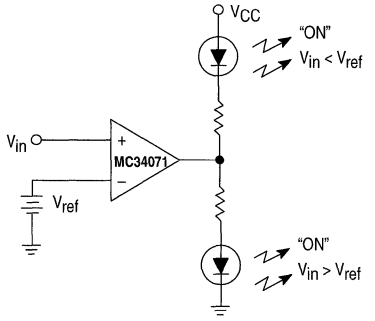


Figure 46. Transistor Driver

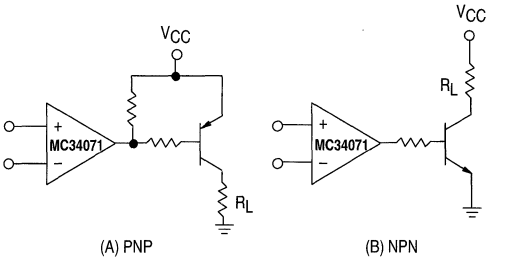


Figure 47. AC/DC Ground Current Monitor

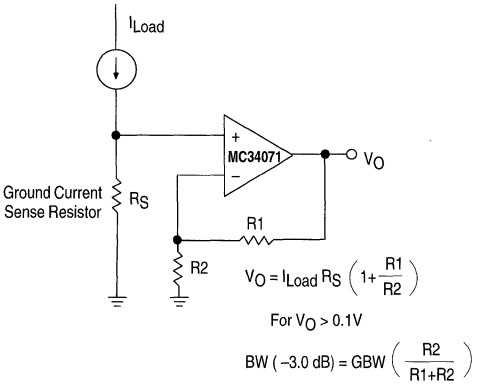


Figure 48. Photovoltaic Cell Amplifier

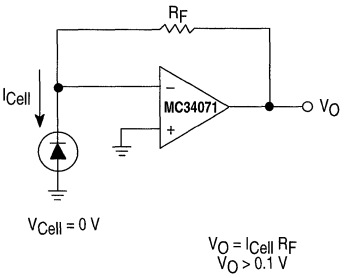
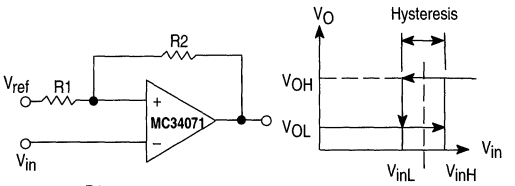


Figure 49. Low Input Voltage Comparator with Hysteresis

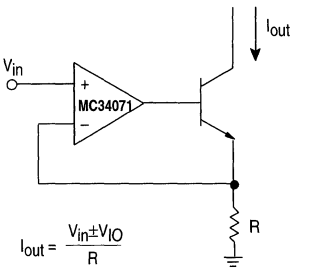


$$V_{inL} = \frac{R1}{R1+R2}(V_{OL}-V_{ref})+V_{ref}$$

$$V_{inH} = \frac{R1}{R1+R2}(V_{OH}-V_{ref})+V_{ref}$$

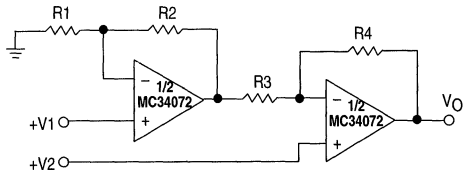
$$V_H = \frac{R1}{R1+R}(V_{OH}-V_{OL})$$

Figure 50. High Compliance Voltage to Sink Current Converter



$$I_{out} = \frac{V_{in} \pm V_{IO}}{R}$$

Figure 51. High Input Impedance Differential Amplifier



$$\frac{R2}{R1} = \frac{R4}{R3} \text{ (Critical to CMRR)}$$

$$V_O = 1\left(+\frac{R4}{R3}\right)\left(V2-V1\,\frac{R4}{R3}\right)$$

For (V2 ≥ V1), V > 0

Figure 52. Bridge Current Amplifier

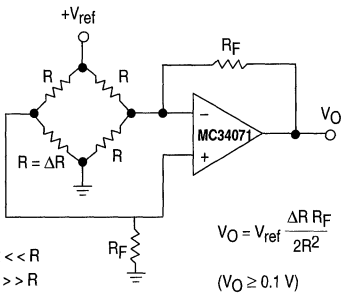


Figure 53. Low Voltage Peak Detector

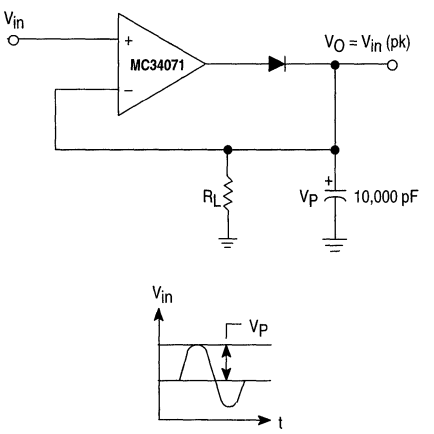
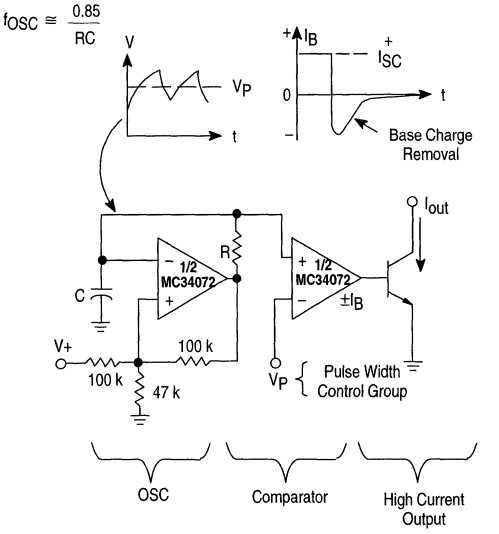


Figure 54. High Frequency Pulse Width Modulation

$$f_{OSC} \cong \frac{0.85}{RC}$$



GENERAL ADDITIONAL APPLICATIONS INFORMATION V_S = ±15.0 V

2

Figure 55. Second Order Low–Pass Active Filter

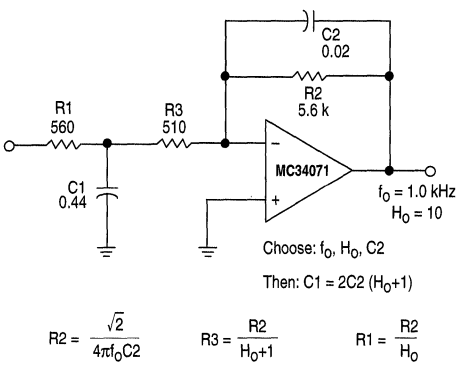


Figure 56. Second Order High–Pass Active Filter

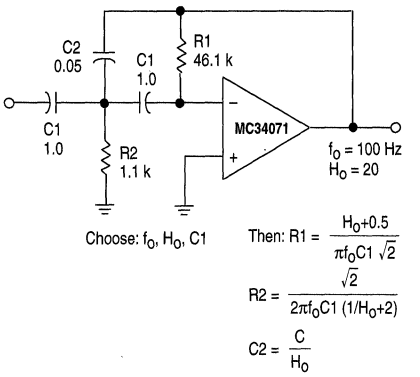


Figure 57. Fast Settling Inverter

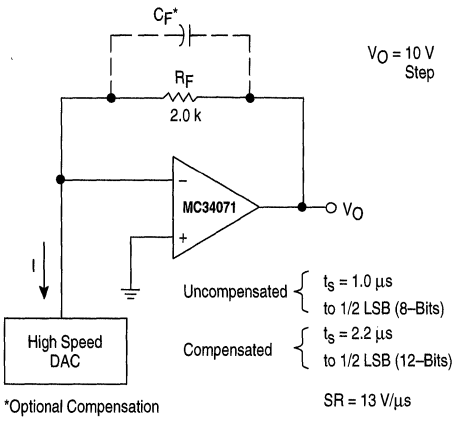


Figure 58. Basic Inverting Amplifier

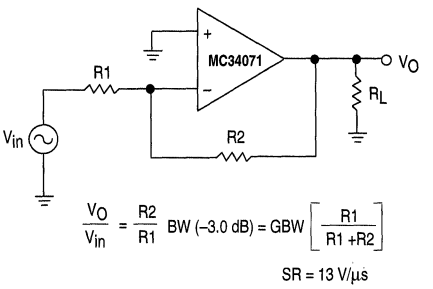


Figure 59. Basic Noninverting Amplifier

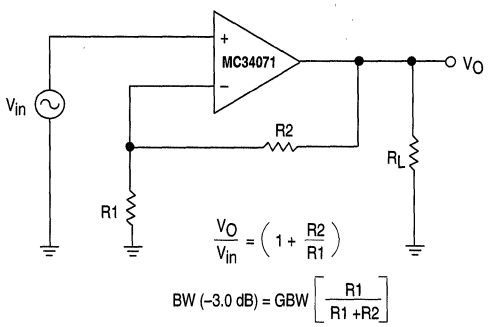


Figure 60. Unity Gain Buffer (A_V = +1.0)

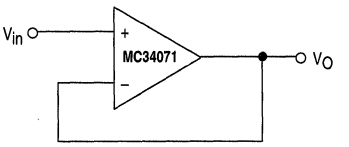


Figure 61. High Impedance Differential Amplifier

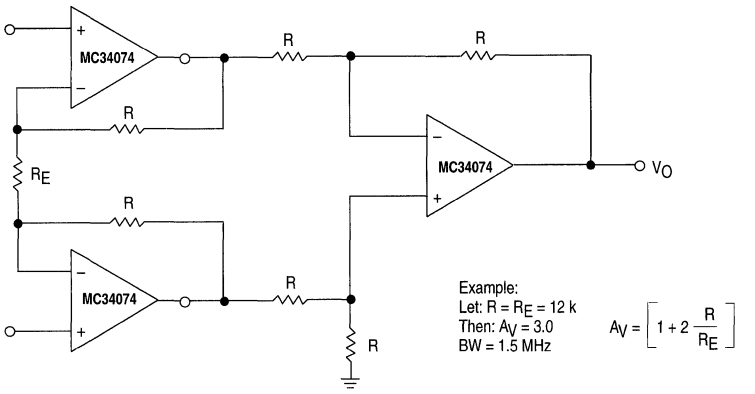
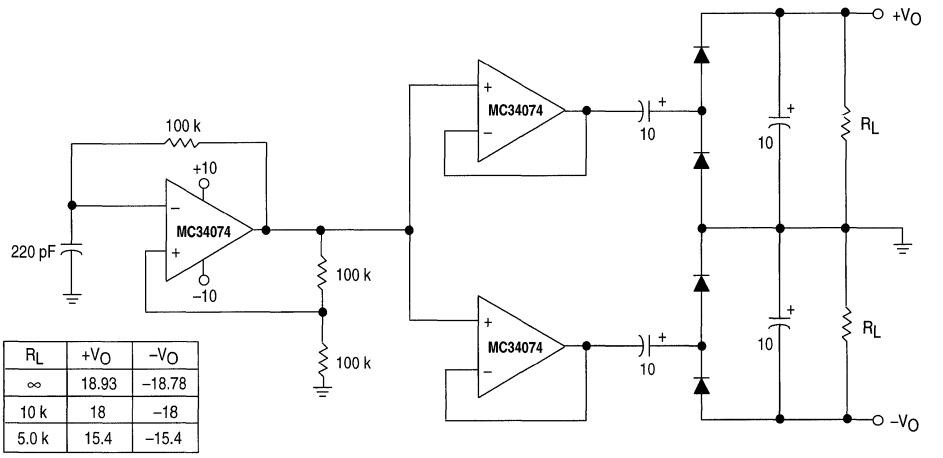


Figure 62. Dual Voltage Doubler



RL	+VO	–VO
∞	18.93	–18.78
10 k	18	–18
5.0 k	15.4	–15.4

2

High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifiers

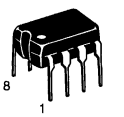
MC34080 thru MC34085

HIGH PERFORMANCE JFET INPUT OPERATIONAL AMPLIFIERS

These devices are a new generation of high speed JFET input monolithic operational amplifiers. Innovative design concepts along with JFET technology provide wide gain bandwidth product and high slew rate. Well–matched JFET input devices and advanced trim techniques ensure low input offset errors and bias currents. The all NPN output stage features large output voltage swing, no deadband crossover distortion, high capacitive drive capability, excellent phase and gain margins, low open loop output impedance, and symmetrical source/sink AC frequency response.

This series of devices is available in fully compensated or decompensated ($A_{VCL} \geq 2$) and is specified over a commercial temperature range. They are pin compatible with existing Industry standard operational amplifiers, and allow the designer to easily upgrade the performance of existing designs.

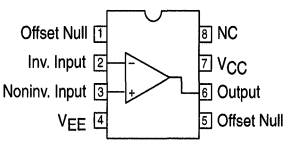
- Wide Gain Bandwidth: 8.0 MHz for Fully Compensated Devices
  16 MHz for Decompensated Devices
- High Slew Rate: 25 V/μs for Fully Compensated Devices
  50 V/μs for Decompensated Devices
- High Input Impedance: $10^{12}\Omega$
- Input Offset Voltage: 0.5 mV Maximum (Single Amplifier)
- Large Output Voltage Swing: −14.7 V to +14 V for
  $V_{CC}/V_{EE} = \pm 15$ V
- Low Open Loop Output Impedance: 30 Ω @ 1.0 MHz
- Low THD Distortion: 0.01%
- Excellent Phase/Gain Margins: 55°/7.6 dB for Fully Compensated Devices



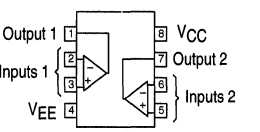
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



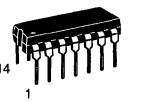
(Single, Top View)



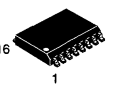
(Dual, Top View)

ORDERING INFORMATION

Op Amp Function	Fully Compensated	$A_{VCL} \geq 2$ Compensated	Operating Temperature Range	Package
Single	MC34081BD	MC34080BD	T_A = 0° to +70°C	SO–8
	MC34081BP	MC34080BP		Plastic DIP
Dual	MC34082P	MC34083BP		Plastic DIP
Quad	MC34084DW	MC34085BDW	T_A = 0° to +70°C	SO–16L
	MC34084P	MC34085BP		Plastic DIP

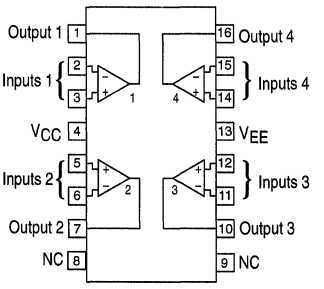


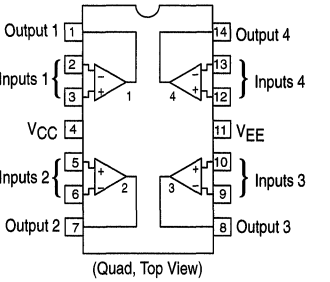
P SUFFIX
PLASTIC PACKAGE
CASE 646



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

PIN CONNECTIONS





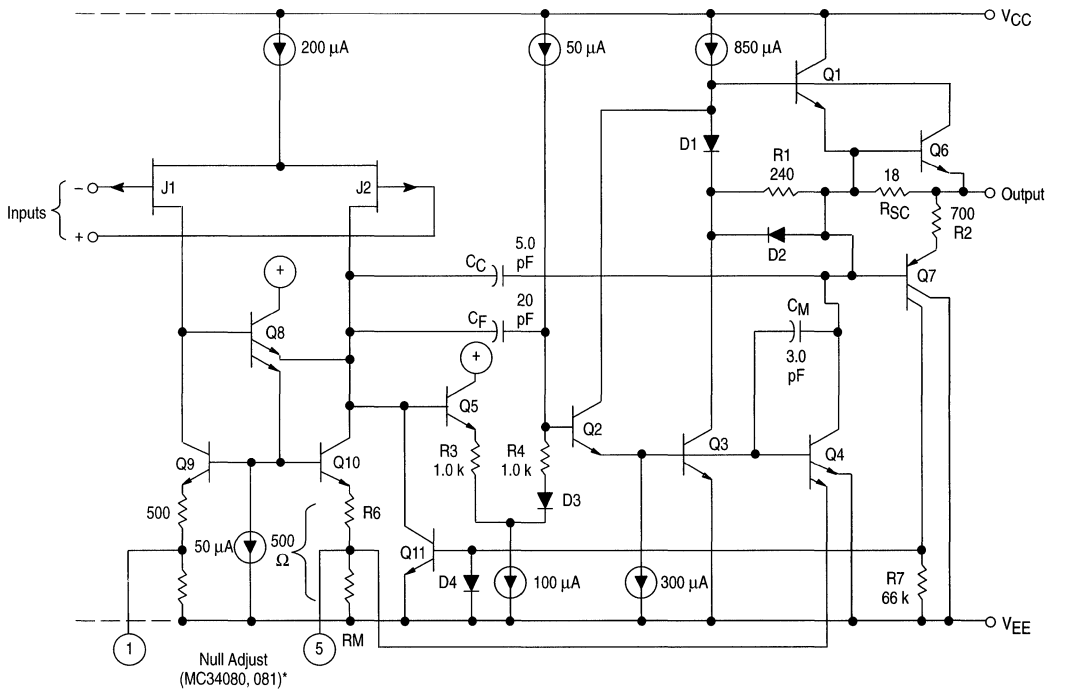
(Quad, Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+44	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	– 65 to +165	°C

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

Representative Schematic Diagram
(Each Amplifier)



*Pins 1 & 5 (MC34080,081) should *not* be directly grounded or connected to V_{CC}.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = – 15 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (Note 4)	V_{IO}				mV
Single					
T_A = +25°C		—	0.5	2.0	
T_A = 0° to +70°C (MC34080B, MC34081B)		—	—	4.0	
Dual					
T_A = +25°C		—	1.0	3.0	
T_A = 0° to +70°C (MC34082, MC34083)		—	—	5.0	
Quad					
T_A = +25°C		—	6.0	12	
T_A = 0° to +70°C (MC34084, MC34085)		—	—	14	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	µV/°C
Input Bias Current (V_{CM} = 0 Note 5)	I_{IB}				nA
T_A = +25°C		—	0.06	0.2	
T_A = 0° to +70°C		—	—	4.0	
Input Offset Current (V_{CM} = 0 Note 5)	I_{IO}				nA
T_A = +25°C		—	0.02	0.1	
T_A = 0° to +70°C		—	—	2.0	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}				V/mV
T_A = +25°C		25	80	—	
T_A = T_{low} to T_{high}		15	—	—	
Output Voltage Swing	V_{OH}				V
R_L = 2.0 k, T_A = +25°C		13.2	13.7	—	
R_L = 10 k, T_A = +25°C		13.4	13.9	—	
R_L = 10 k, T_A = T_{low} to T_{high}		13.4	—	—	
R_L = 2.0 k, T_A = +25°C	V_{OL}	—	–14.1	–13.5	
R_L = 10 k, T_A = +25°C		—	–14.7	–14.1	
R_L = 10 k, T_A = T_{low} to T_{high}		—	—	–14.0	
Output Short Circuit Current (T_A = +25°C)	I_{SC}				mA
Input Overdrive = 1.0 V, Output to Ground					
Source		20	31	—	
Sink		20	28	—	
Input Common Mode Voltage Range	V_{ICR}	(V_{EE} +4.0) to			V
T_A = +25°C		(V_{CC} – 2.0)			
Common Mode Rejection Ratio (R_S ≤ 10 k, T_A = +25°C)	CMRR	70	90	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω, T_A = 25°C)	PSRR	70	86	—	dB
Power Supply Current	I_D				mA
Single					
T_A = +25°C		—	2.5	3.4	
T_A = T_{low} to T_{high}		—	—	4.2	
Dual					
T_A = +25°C		—	4.9	6.0	
T_A = T_{low} to T_{high}		—	—	7.5	
Quad					
T_A = +25°C		—	9.7	11	
T_A = T_{low} to T_{high}		—	—	13	

NOTES: (continued)

3. T_{low} = 0°C for MC34080B, MC34081B, MC34084, MC34085 T_{high} = +70°C for MC34080B, MC34081B, MC34084, MC34085
4. See application information for typical changes in input offset voltage due to solderability and temperature cycling.
5. Limits at T_A = +25°C are guaranteed by high temperature (T_{high}) testing.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = – 15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF)	SR				V/μs
Compensated A_V = +1.0		20	25	—	
A_V = –1.0		—	30	—	
Decompensated A_V = +2.0		35	50	—	
A_V = –1.0		—	50	—	
Settling Time (10 V Step, A_V = –1.0)	t_s				μs
To 0.10% (±1/2 LSB of 9–Bits)		—	0.72	—	
To 0.01% (±1/2 LSB of 12–Bits)		—	1.6	—	
Gain Bandwidth Product (f = 200 kHz)	GBW				MHz
Compensated		6.0	8.0	—	
Decompensated		12	16	—	
Power Bandwidth (R_L = 2.0 k, V_O = 20 V_{pp}, THD = 5.0%)	BWp				kHz
Compensated A_V = +1.0		—	400	—	
Decompensated A_V = – 1.0		—	800	—	
Phase Margin (Compensated)	ϕ_m				Degrees
R_L = 2.0 k		—	55	—	
R_L = 2.0 k, C_L = 100 pF		—	39	—	
Gain Margin (Compensated)	A_m				dB
R_L = 2.0 k		—	7.6	—	
R_L = 2.0 k, C_L = 100 pF		—	4.5	—	
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	30	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	I_n	—	0.01	—	$pA/\sqrt{Hz}$
Input Capacitance	C_i	—	5.0	—	pF
Input Resistance	r_i	—	10^{12}	—	Ω
Total Harmonic Distortion A_V = +10, R_L = 2.0 k, 2.0 ≤ V_O ≤ 20 V_{pp}, f = 10 kHz	THD	—	0.05	—	%
Channel Separation (f = 10 kHz)	—	—	120	—	dB
Open Loop Output Impedance (f = 1.0 MHz)	Z_o	—	35	—	Ω

Figure 1. Input Common Mode Voltage Range versus Temperature

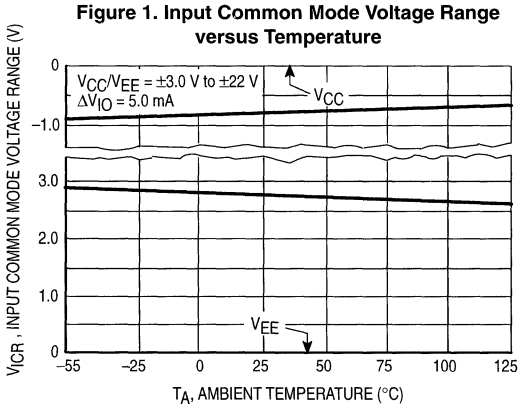
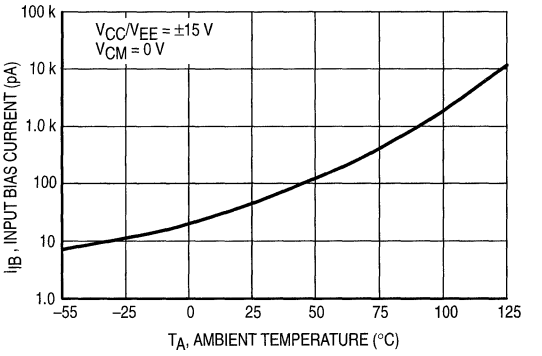


Figure 2. Input Bias Current versus Temperature



2

Figure 3. Input Bias Current versus Input Common Mode Voltage

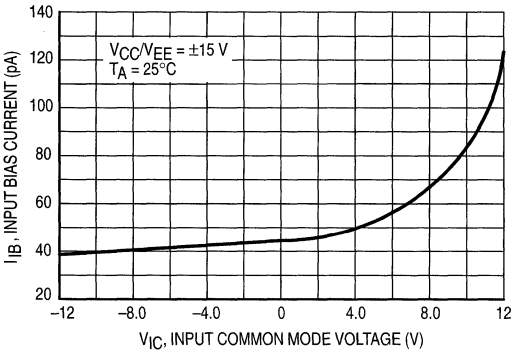


Figure 4. Output Voltage Swing versus Supply Voltage

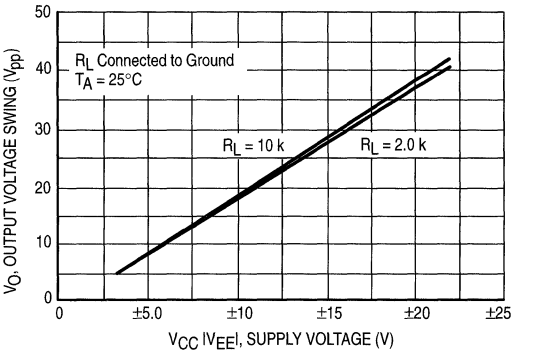


Figure 5. Output Saturation versus Load Current

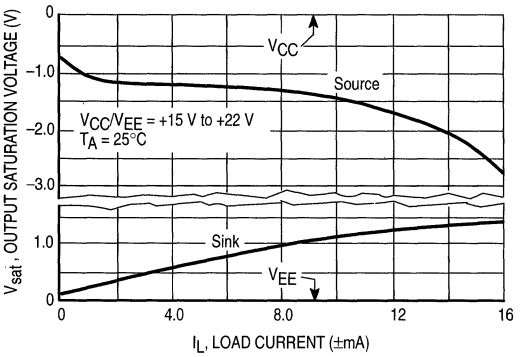


Figure 6. Output Saturation vesus Load Resistance to Ground

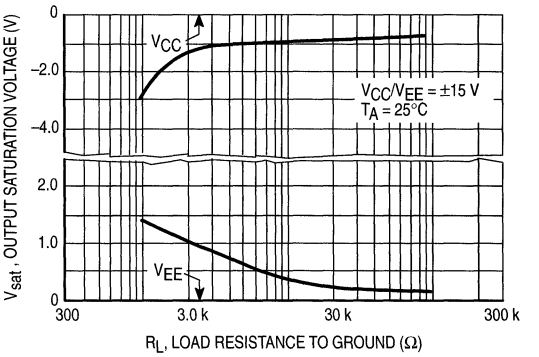


Figure 7. Output Saturation versus Load Resistance to V_{CC}

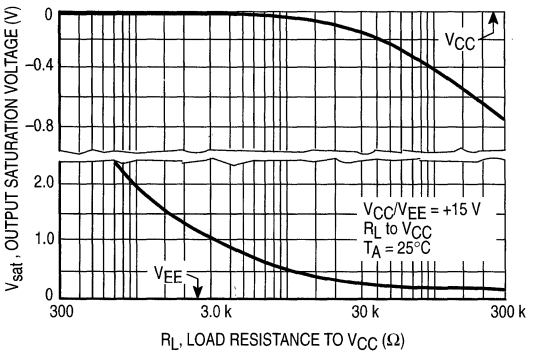


Figure 8. Output Short Circuit Current versus Temperature

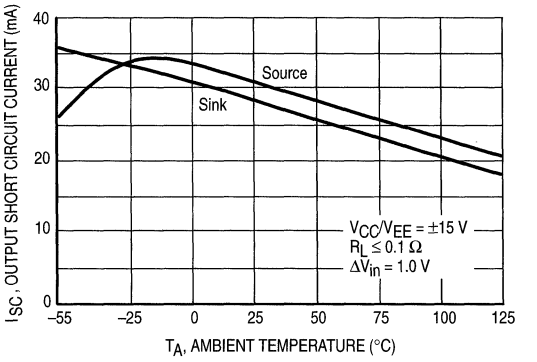


Figure 9. Output Impedance versus Frequency

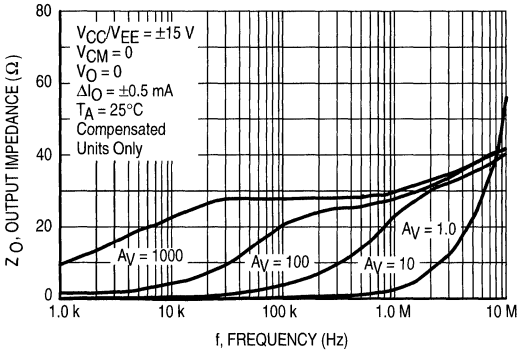


Figure 10. Output Impedance versus Frequency

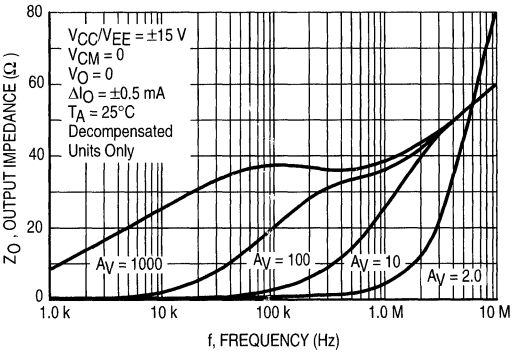


Figure 11. Output Voltage Swing versus Frequency

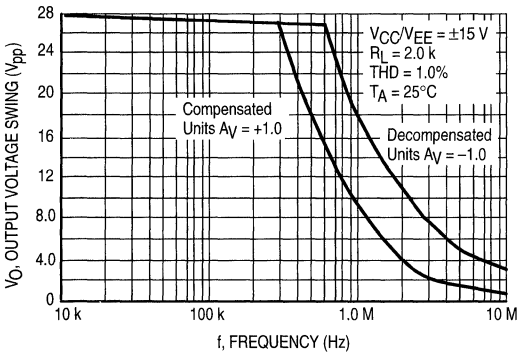


Figure 12. Output Distortion versus Frequency

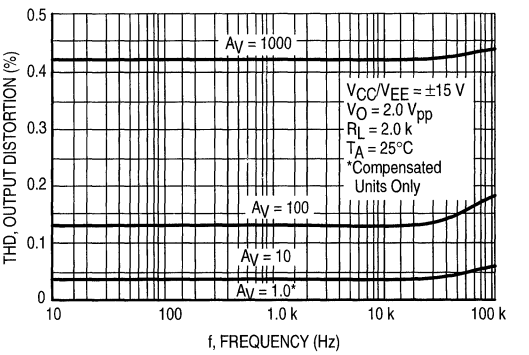
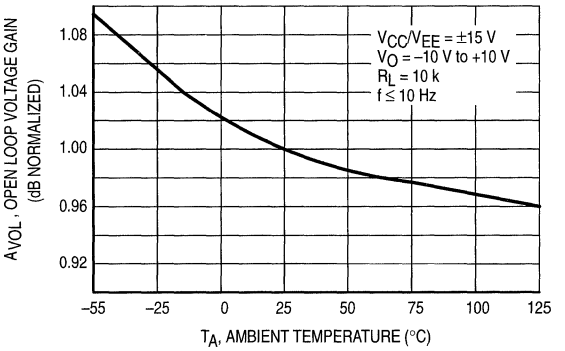


Figure 13. Open Loop Voltage Gain versus Temperature



2

Figure 14. Open Loop Voltage Gain and Phase versus Frequency

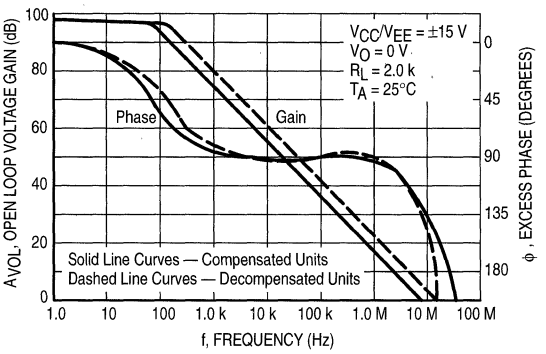


Figure 15. Open Loop Voltage Gain and Phase versus Frequency

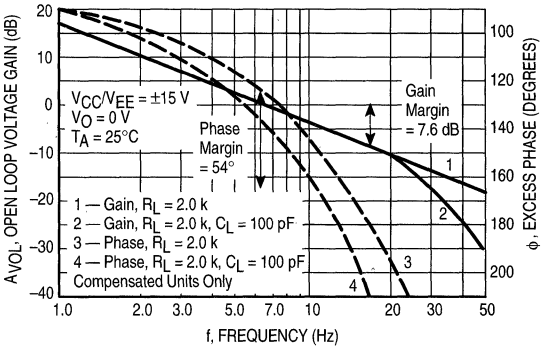


Figure 16. Open Loop Voltage Gain and Phase versus Frequency

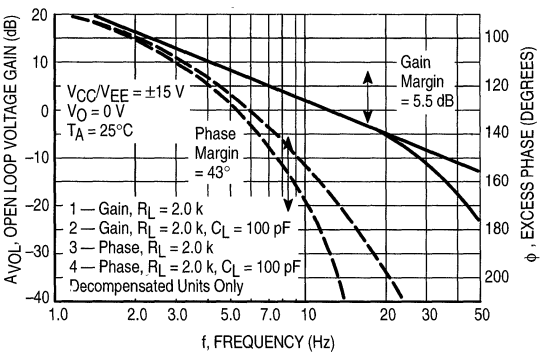


Figure 17. Normalized Gain Bandwidth Product versus Temperature

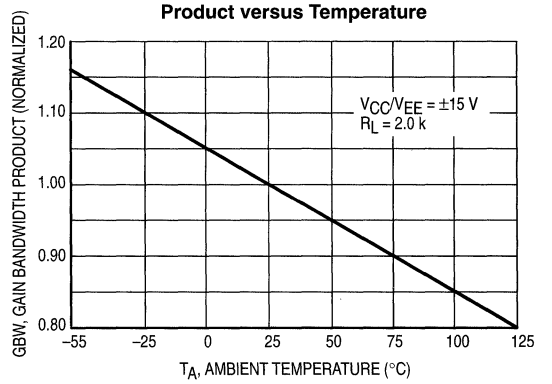


Figure 18. Percent Overshoot versus Load Capacitance

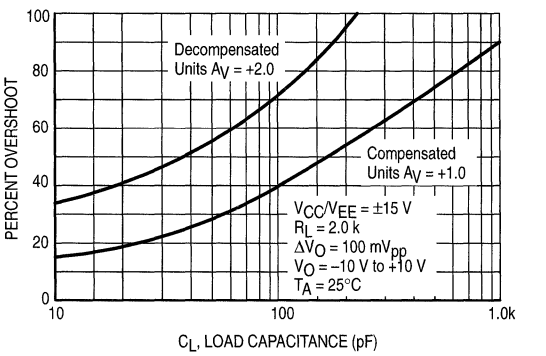


Figure 19. Phase Margin versus Load Capacitance

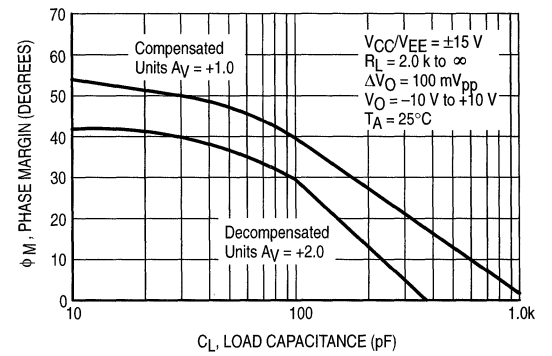


Figure 20. Gain Margin versus Load Capacitance

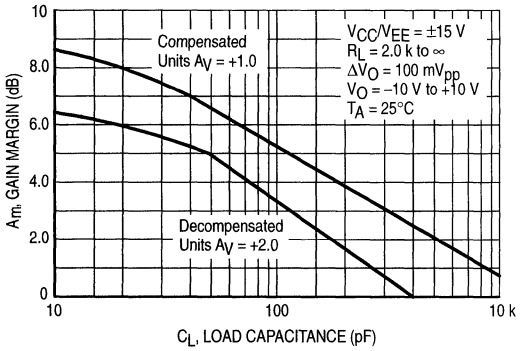


Figure 21. Phase Margin versus Temperature

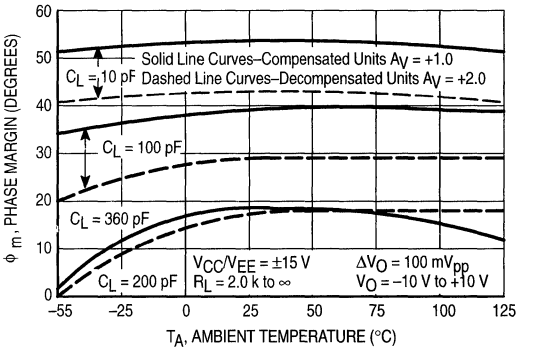


Figure 22. Gain Margin versus Temperature

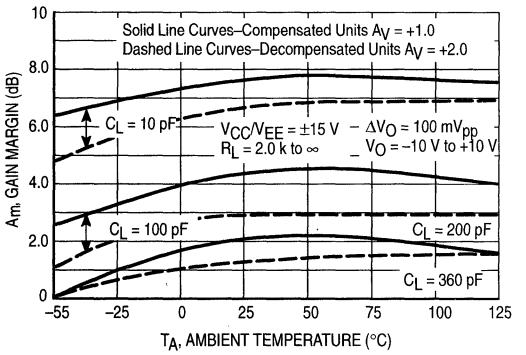
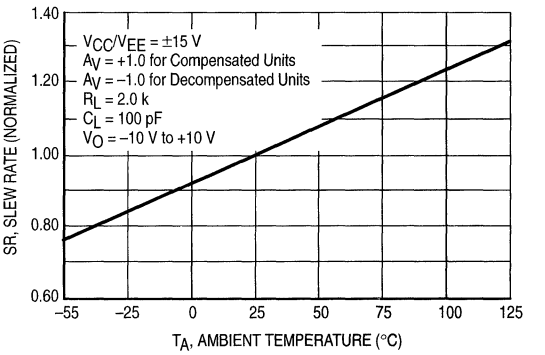


Figure 23. Normalized Slew Rate versus Temperature



2

MC34084 Transient Response

A_V = +1.0, R_L = 2.0 k, V_{CC}/V_{EE} = ±15 V, T_A = 25°C

Figure 24. Small Signal

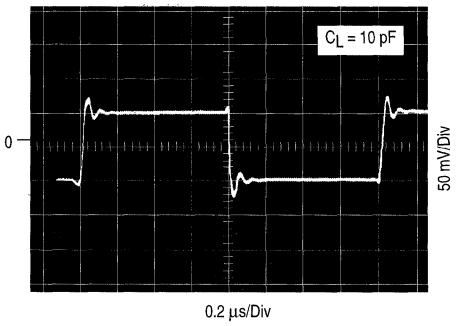
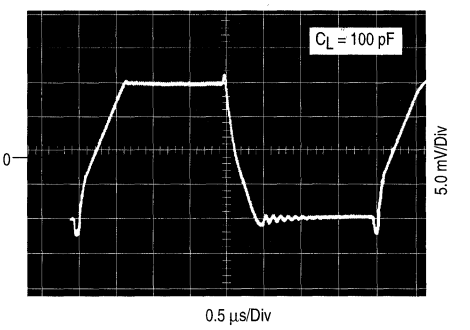


Figure 25. Large Signal



MC34085 Transient Response

A_V = +2.0, R_L = 2.0 k, V_{CC}/V_{EE} = ±15 V, T_A = 25°C

Figure 26. Small Signal

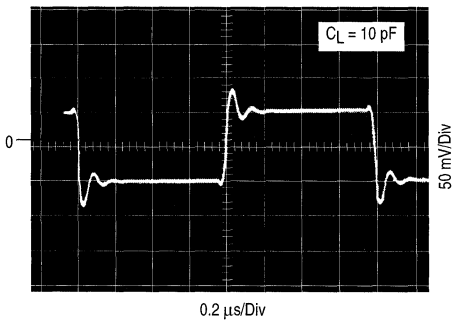


Figure 27. Large Signal

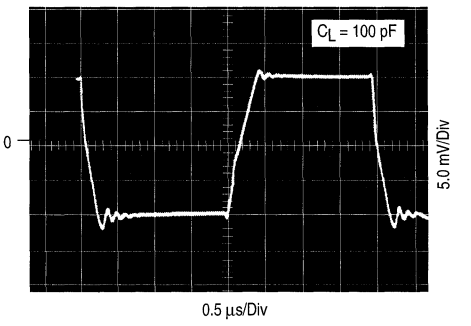


Figure 28. Common Mode Rejection Ratio versus Frequency

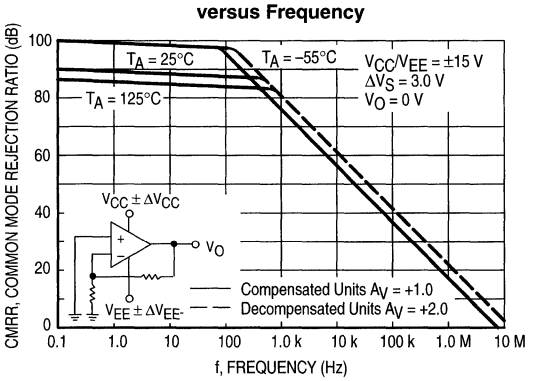


Figure 29. Power Supply Rejection Ratio versus Frequency

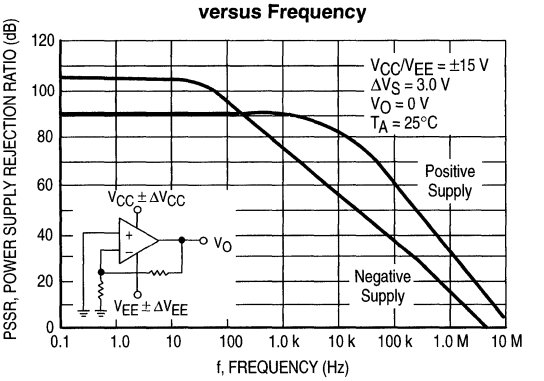


Figure 30. Power Supply Rejection Ratio versus Temperature

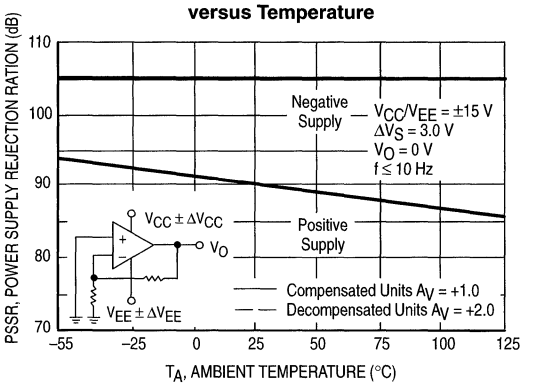


Figure 31. Normalized Supply Current versus Supply Voltage

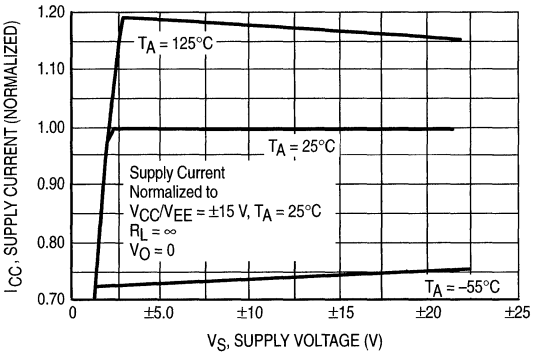


Figure 32. Channel Separation versus Frequency

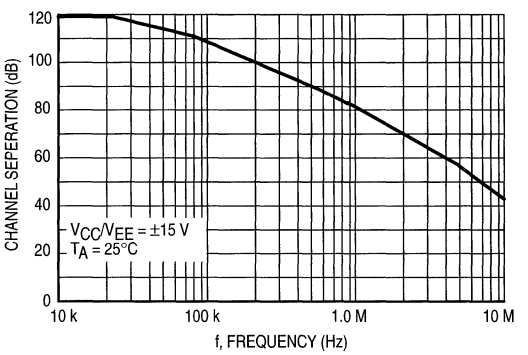
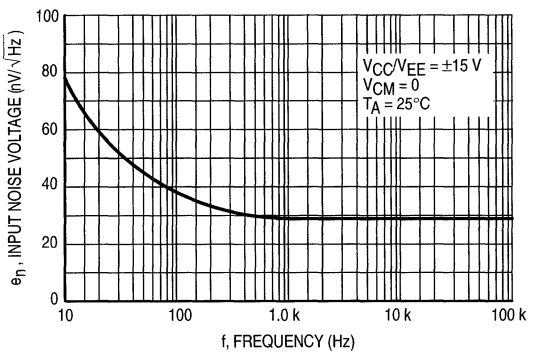


Figure 33. Spectral Noise Density



APPLICATIONS INFORMATION

The bandwidth and slew rate of the MC34080 series is nearly double that of currently available general purpose JFET op–amps. This improvement in AC performance is due to the P–channel JFET differential input stage driving a compensated miller integration amplifier in conjunction with an all NPN output stage.

The all NPN output stage offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. With a 10 k load resistance, the op amp can typically swing within 1.0 V of the positive rail (V_{CC}), and within 0.3 V of the negative rail (V_{EE}), providing a 28.7 p–p swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages. If the load resistance is referenced to V_{CC} instead of ground, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the NPN output transistor will pull the output very near V_{EE} during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull–up capability.

The all NPN transistor output stage is also inherently fast, contributing to the operation amplifier's high gain–bandwidth product and fast settling time. The associated high frequency output impedance is 50 Ω (typical) at 8.0 MHz. This allows driving capacitive loads from 0 pF to 300 pF without oscillations over the military temperature range, and over the full range of output swing. The 55°C phase margin and 7.6 dB gain margin as well as the general gain and phase characteristics are virtually independent of the sink/source output swing conditions. The high frequency characteristics of the MC34080 series is especially useful for active filter applications.

The common mode input range is from 2.0 V below the positive rail (V_{CC}) to 4.0 V above the negative rail (V_{EE}). The amplifier remains active if the inputs are biased at the positive rail. This may be useful for some applications in that single supply operation is possible with a single negative supply. However, a degradation of offset voltage and voltage gain may result.

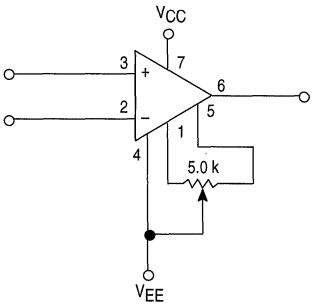
Phase reversal does not occur if either the inverting or noninverting input (or both) exceeds the positive common mode limit. If either input (or both) exceeds the negative common mode limit, the output will be in the high state. The input stage also allows a differential up to ±44 V, provided the maximum input voltage range is not exceeded. The supply voltage operating range is from ±5.0 V to ±22 V.

For optimum frequency performance and stability, careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input–output coupling. In order to reduce the input capacitance, resistors connected to the input pins should be physically close to these pins. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pickup" at this node.

Supply decoupling with adequate capacitance close to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit large impedance changes over temperature.

Primarily due to the JFET inputs of the op amp, the input offset voltage may change due to temperature cycling and board soldering. After 20 temperature cycles (– 55° to 165°C), the typical standard deviation for input offset voltage is 559 μV in the plastic packages. With respect to board soldering (260°C, 10 seconds), the typical standard deviation for input offset voltage is 525 μV in the plastic package. Socketed devices should be used over a minimal temperature range for optimum input offset voltage performance.

Figure 34. Offset Nulling Circuit



MC34181,2,4
MC33181,2,4

Low Power, High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifiers

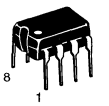
Quality bipolar fabrication with innovative design concepts are employed for the MC33181/2/4, MC34181/2/4 series of monolithic operational amplifiers. This JFET input series of operational amplifiers operates at 210 μA per amplifier and offers 4.0 MHz of gain bandwidth product and 10 V/μs slew rate. Precision matching and an innovative trim technique of the single and dual versions provide low input offset voltages. With a JFET input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33181/2/4, MC34181/2/4 series of devices are specified over the commercial or industrial/vehicular temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic DIP as well as the SOIC surface mount packages.

- Low Supply Current: 210 μA (Per Amplifier)
- Wide Supply Operating Range: ±1.5 V to ±18 V
- Wide Bandwidth: 4.0 MHz
- High Slew Rate: 10 V/μs
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: –14 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 500 pF
- Low Total Harmonic Distortion: 0.04%
- Excellent Phase Margin: 67°
- Excellent Gain Margin: 6.7 dB
- Output Short Circuit Protection
- Offered in New TSSOP Package Including the Standard SOIC and DIP Packages

ORDERING INFORMATION

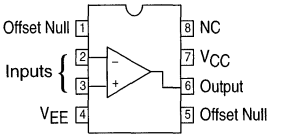
Op Amp Function	Device	Operating Temperature Range	Package
Single	MC34181P MC34181D	T_A = 0° to +70°C	Plastic DIP SO–8
	MC33181P MC33181D	T_A = –40° to +85°C	Plastic DIP SO–8
Dual	MC34182P MC34182D	T_A = 0° to +70°C	Plastic DIP SO–8
	MC33182P MC33182D	T_A = –40° to +85°C	Plastic DIP SO–8
Quad	MC34184P MC34184D MC34184DTB	T_A = 0° to +70°C	Plastic DIP SO–14 TSSOP–14
	MC33184P MC33184D MC33184DTB	T_A = –40° to +85°C	Plastic DIP SO–14 TSSOP–14



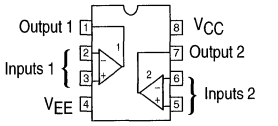
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

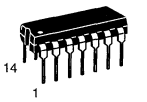
PIN CONNECTIONS



(Single, Top View)



(Dual, Top View)

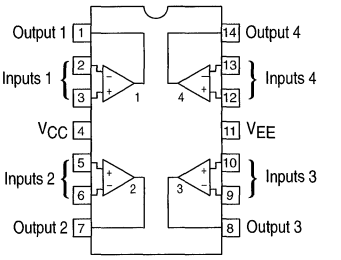


P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

DTB SUFFIX
PLASTIC PACKAGE
CASE 948G
(TSSOP–14)

PIN CONNECTIONS



(Quad, Top View)

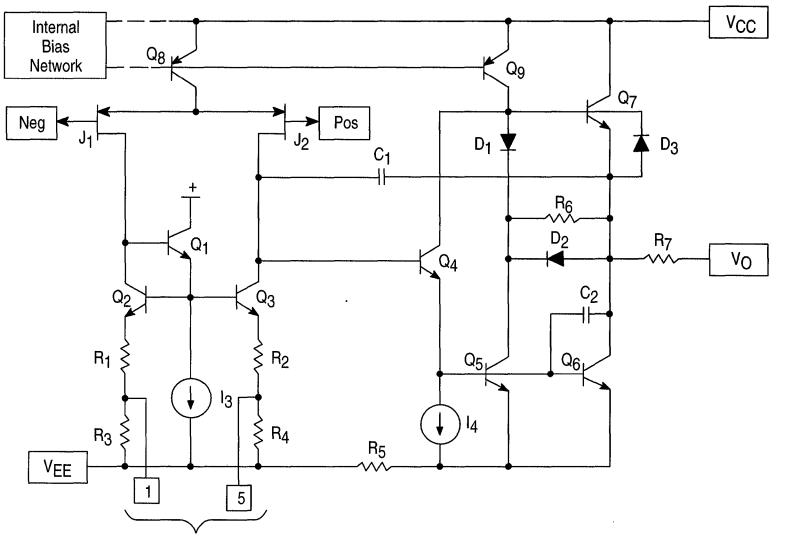
2

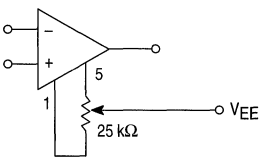
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C

NOTES: 1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

Representative Schematic Diagram
(Each Amplifier)





MC3X181 Input Offset
Voltage Null CIrcuit

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_O = 0 V)	V_{IO}				mV
Single					
T_A = +25°C		—	0.5	2.0	
T_A = 0° to +70°C (MC34181)		—	—	3.0	
T_A = –40° to +85°C (MC33181)		—	—	3.5	
Dual					
T_A = +25°C		—	1.0	3.0	
T_A = 0° to +70°C (MC34182)		—	—	4.0	
T_A = –40° to +85°C (MC33182)		—	—	4.5	
Quad					
T_A = +25°C		—	4.0	10	
T_A = 0° to +70°C (MC34184)		—	—	11	
T_A = –40° to +85°C (MC33184)		—	—	11.5	
Average Temperature Coefficient of V_{IO} (R_S = 50 Ω, V_O = 0V)	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0V)	I_{IO}				nA
T_A = +25°C		—	0.001	0.05	
T_A = 0° to +70°C		—	—	1.0	
T_A = –40° to +85°C		—	—	2.0	
Input Bias Current (V_{CM} = 0 V, V_O = 0V)	I_{IB}				nA
T_A = +25°C		—	0.003	0.1	
T_A = 0° to +70°C		—	—	2.0	
T_A = –40° to +85°C		—	—	4.0	
Input Common Mode Voltage Range	V_{ICR}	(V_{EE} +4.0 V) to (V_{CC} –2.0 V)			V
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V)	A_{VOL}				V/mV
T_A = +25°C		25	60	—	
T_A = T_{low} to T_{high}		15	—	—	
Output Voltage Swing (V_{ID} = 1.0 V, R_L = 10 kΩ)	V_{O+}	+13.5	+14	—	V
T_A = +25°C	V_{O-}	—	–14	–13.5	
Common Mode Rejection (R_S = 50 Ω, V_{CM} = V_{ICR}, V_O = 0 V)	CMR	70	86	—	dB
Power Supply Rejection (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	PSR	70	84	—	dB
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	I_{SC}				mA
Source		3.0	8.0	—	
Sink		8.0	11	—	
Power Supply Current (No Load, V_O = 0 V)	I_D				μA
Single					
T_A = +25°C		—	210	250	
T_A = T_{low} to T_{high}		—	—	250	
Dual					
T_A = +25°C		—	420	500	
T_A = T_{low} to T_{high}		—	—	500	
Quad					
T_A = +25°C		—	840	1000	
T_A = T_{low} to T_{high}		—	—	1000	

2

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 kΩ, C_L = 100 pF) A_V = +1.0 A_V = −1.0	SR	 7.0 —	 10 10	 — —	V/μs
Settling Time (A_V = −1.0, R_L = 10 kΩ, V_O = 0 V to +10 V Step) To Within 0.10% To Within 0.01%	t_s	 — —	 1.1 1.5	 — —	μs
Gain Bandwidth Product (f = 100 kHz)	GBW	3.0	4.0	—	MHz
Power Bandwidth (A_V = +1.0, R_L = 10 kΩ, V_O = 20 V_{pp}, THD = 5.0%)	BW_p	—	120	—	kHz
Phase Margin (−10 V < V_O < +10 V) R_L = 10 kΩ R_L = 10 kΩ, C_L = 100 pF	f_m	 — —	 67 34	 — —	Degrees
Gain Margin (−10 V < V_O < +10 V) R_L = 10 kΩ R_L = 10 kΩ, C_L = 100 pF	A_m	 — —	 6.7 3.4	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	38	—	nV/√Hz
Equivalent Input Noise Current f = 1.0 kHz	i_n	—	0.01	—	pA/√Hz
Differential Input Capacitance	C_i	—	3.0	—	pF
Differential Input Resistance	R_i	—	10^{12}	—	W
Total Harmonic Distortion A_V = 10, R_L = 10 kΩ, 2.0 V_{pp} < V_O < 20 V_{pp}, f = 1.0 kHz	THD	—	0.04	—	%
Channel Separation (R_L = 10 kΩ, −10 V < V_O < +10 V, 0 Hz < f < 10 kHz)	—	—	120	—	dB
Open Loop Output Impedance (f = 1.0 MHz)	$\|Z_o\|$	—	200	—	Ω

Figure 1. Maximum Power Dissipation versus Temperature for Package Variations

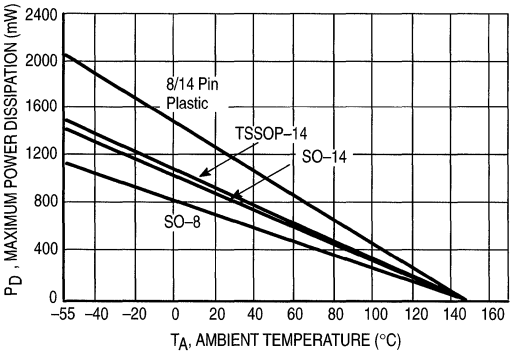


Figure 2. Input Common Mode Voltage Range versus Temperature

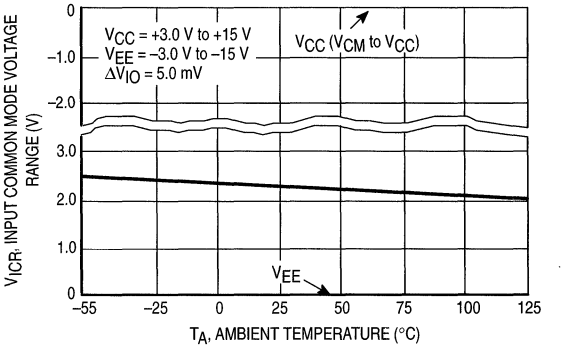


Figure 3. Input Bias Current versus Temperature

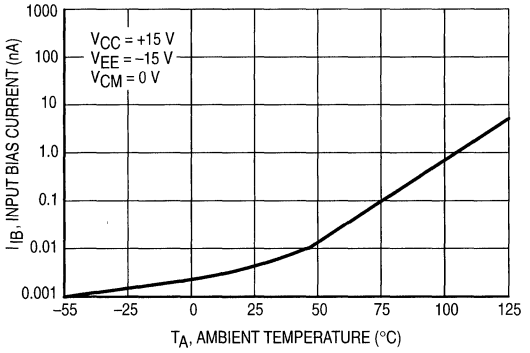


Figure 4. Input Bias Current versus Input Common Mode Voltage

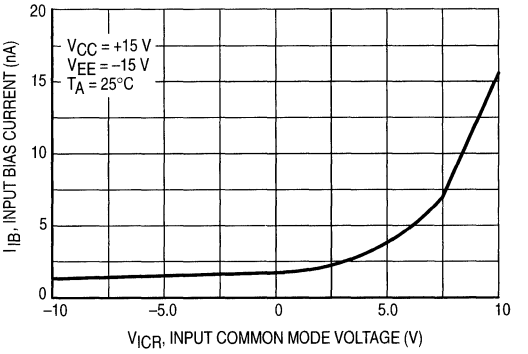


Figure 5. Output Voltage Swing versus Supply Voltage

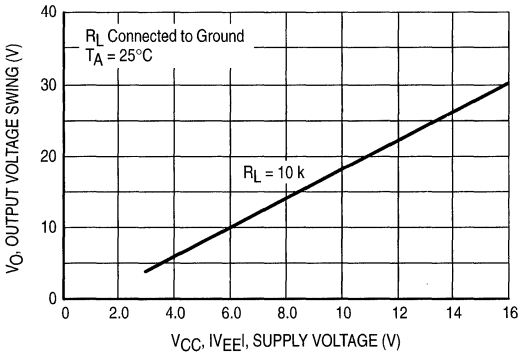


Figure 6. Output Saturation Voltage versus Load Current

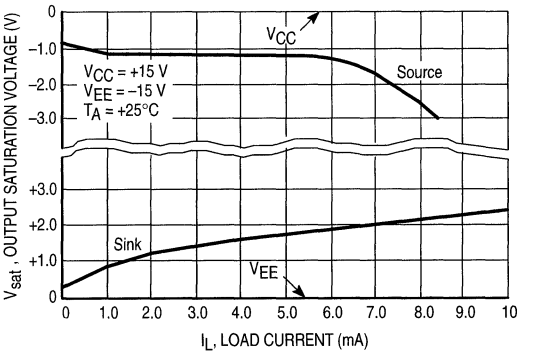


Figure 7. Output Saturation Voltage versus Load Resistance to Ground

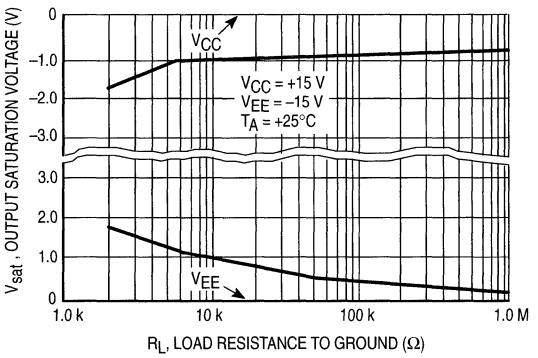
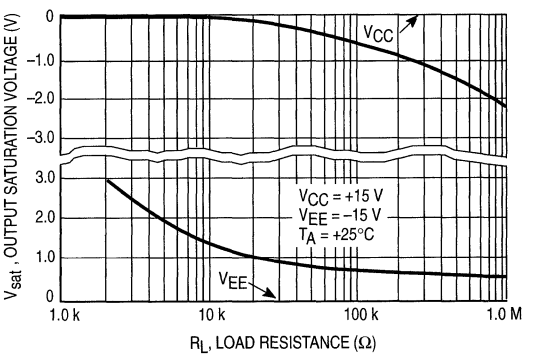


Figure 8. Output Saturation Voltage versus Load Resistance to V_{CC}



2

Figure 9. Output Short Circuit Current versus Temperature

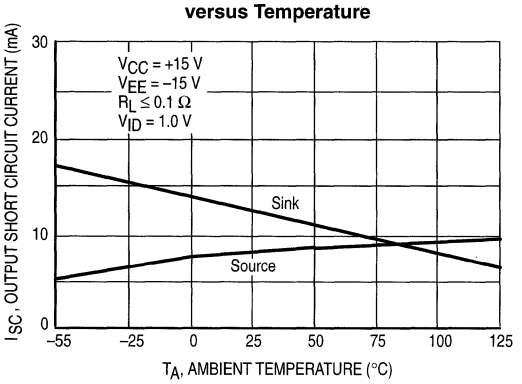


Figure 10. Output Impedance versus Frequency

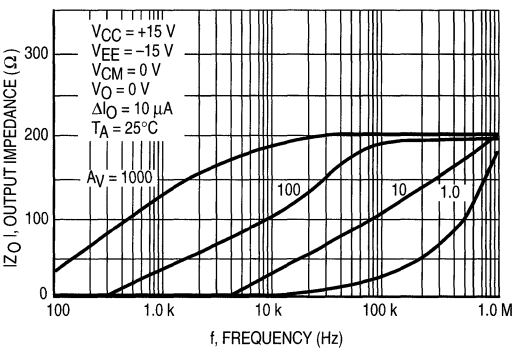


Figure 11. Output Voltage Swing versus Frequency

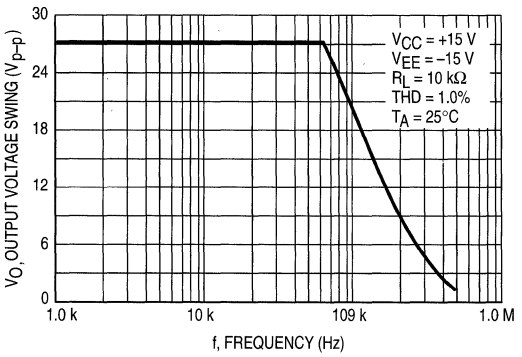


Figure 12. Output Distortion versus Frequency

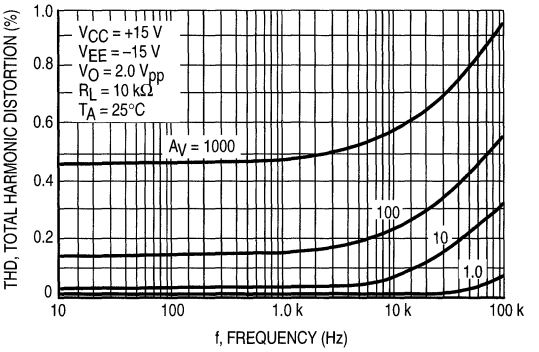


Figure 13. Open Loop Voltage Gain versus Temperature

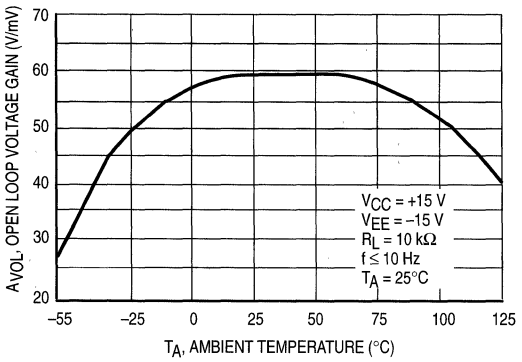


Figure 14. Open Loop Voltage Gain and Phase versus Frequency

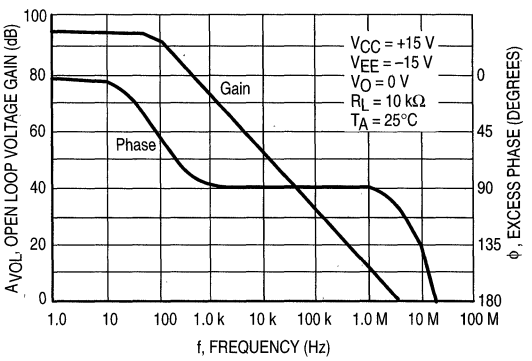


Figure 15. Normalized Gain Bandwidth Product versus Temperature

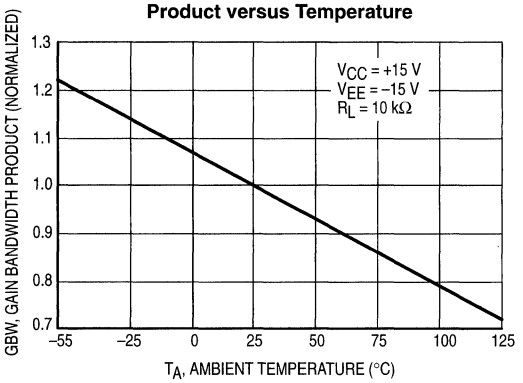


Figure 16. Output Voltage Overshoot versus Load Capacitance

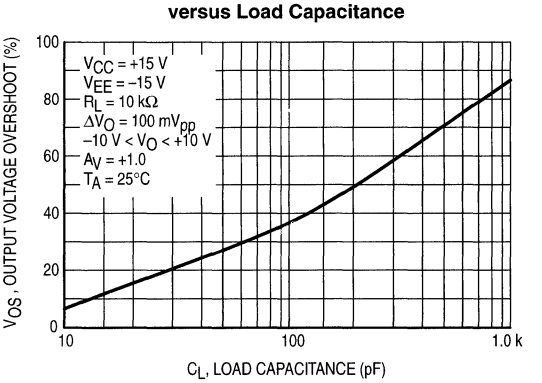


Figure 17. Phase Margin versus Load Capacitance

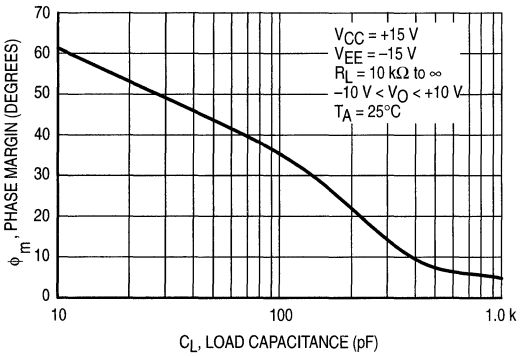


Figure 18. Gain Margin versus Load Capacitance

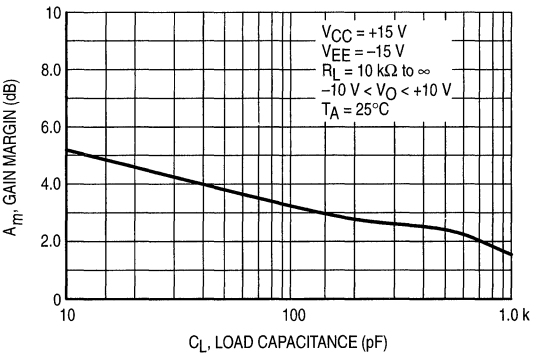


Figure 19. Phase Margin versus Temperature

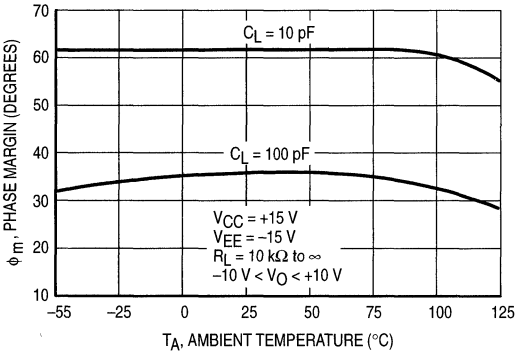
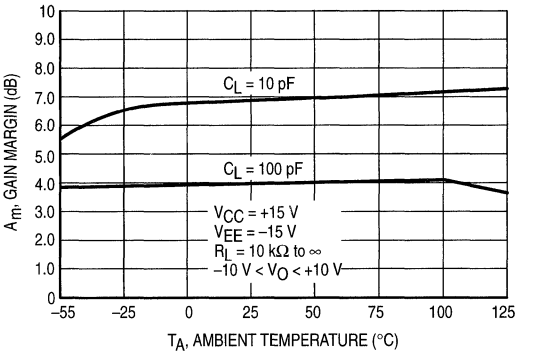


Figure 20. Gain Margin versus Temperature



2

Figure 21. Normalized Slew Rate versus Temperature

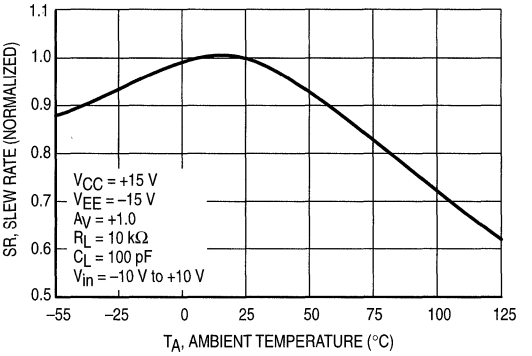


Figure 22. Common Mode Rejection versus Frequency

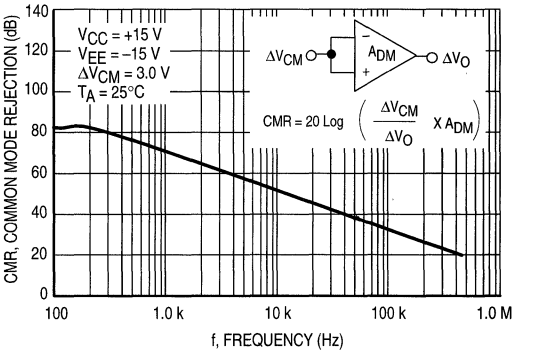


Figure 23. Input Noise Voltage versus Frequency

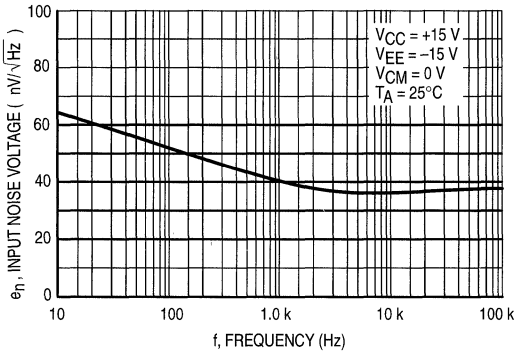


Figure 24. Power Supply Rejection versus Temperature

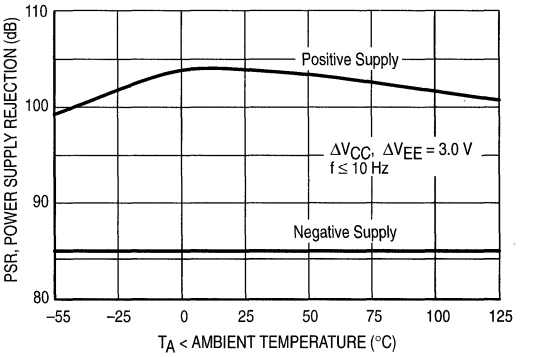


Figure 25. Power Supply Rejection versus Frequency

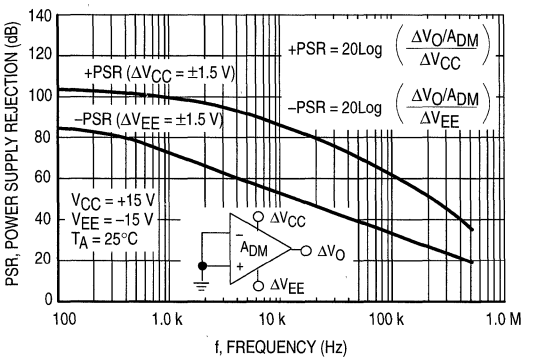


Figure 26. Normalized Supply Current versus Supply Voltage

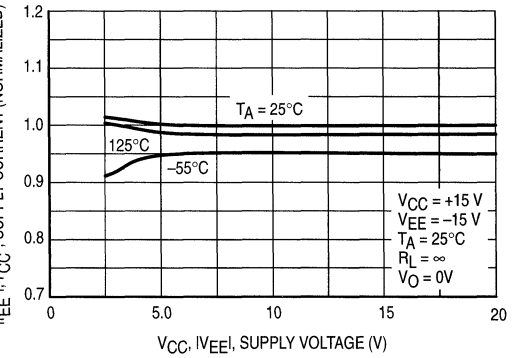


Figure 27. Channel Separation versus Frequency

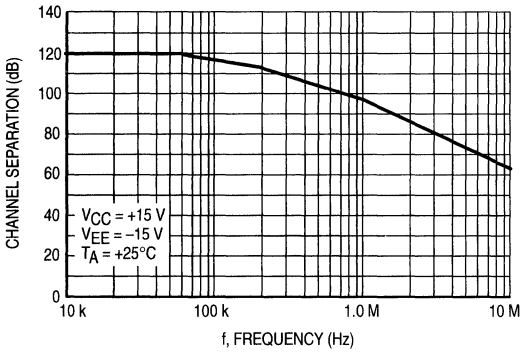


Figure 28. Transient Response

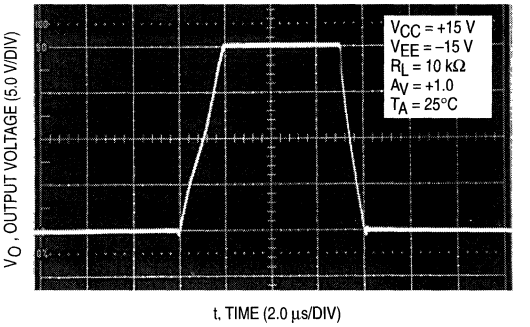
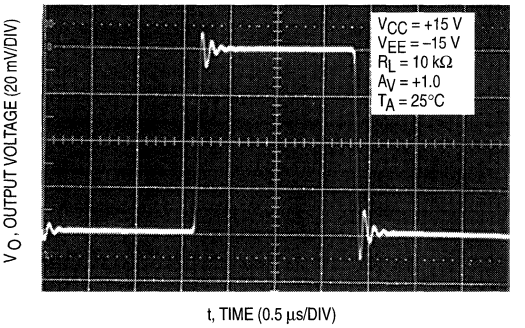


Figure 29. Small Signal Transient Reponse



TCA0372

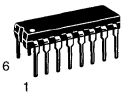
Advance Information

Dual Power Operational Amplifier

The TCA0372 is a monolithic circuit intended for use as a power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. No deadband crossover distortion provides better performance for driving coils.

- Output Current to 1.0 A
- Slew Rate of 1.3 V/μs
- Wide Bandwidth of 1.1 MHz
- Internal Thermal Shutdown
- Single or Split Supply Operation
- Excellent Gain and Phase Margins
- Common Mode Input Includes Ground
- Zero Deadband Crossover Distortion

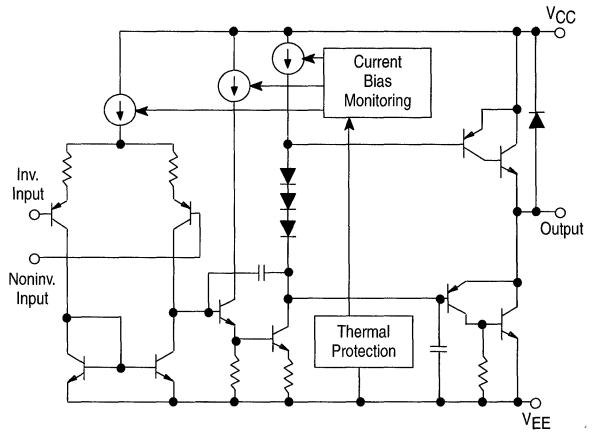
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
SOP (12+2+2)L



DP2 SUFFIX
PLASTIC PACKAGE
CASE 648

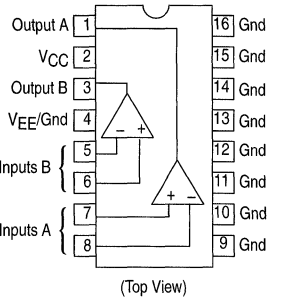
DP1 SUFFIX
PLASTIC PACKAGE
CASE 626

Representative Block Diagram



PIN CONNECTIONS

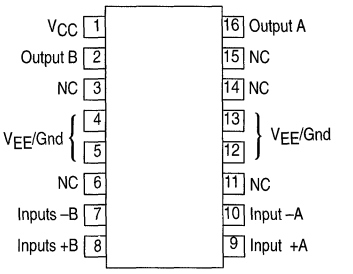
TCA0372DP2



(Top View)

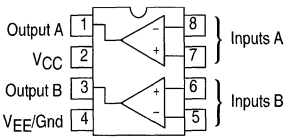
*Pins 4 and 9 to 16 are internally connected.

TCA0372DW



(Top View)

TCA0372DP1



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
TCA0372DW	T_J = –40° to +150°C	SOP (12+2+2) L
TCA0372DP1		Plastic DIP
TCA0372DP2		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	40	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Junction Temperature (Note 2)	T_J	+150	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
DC Output Current	I_O	1.0	A
Peak Output Current (Nonrepetitive)	$I_{(max)}$	1.5	A

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, R_L connected to ground, T_J = –40° to +125°C.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} = 0)	V_{IO}				mV
T_J = +25°C		—	1.0	15	
T_J, T_{low} to T_{high}		—	—	20	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	20	—	µV/°C
Input Bias Current (V_{CM} = 0)	I_{IB}	—	100	500	nA
Input Offset Current (V_{CM} = 0)	I_{IO}	—	10	50	nA
Large Signal Voltage Gain	A_{VOL}	30	100	—	V/mV
V_O = ±10 V, R_L = 2.0 k					
Output Voltage Swing (I_L = 100 mA)	V_{OH}				V
T_J = +25°C		14.0	14.2	—	
T_J = T_{low} to T_{high}		13.9	—	—	
T_J = +25°C	V_{OL}	—	–14.2	–14.0	
T_J = T_{low} to T_{high}		—	—	–13.9	
Output Voltage Swing (I_L = 1.0 A)	V_{OH}				V
V_{CC} = +24 V, V_{EE} = 0 V, T_J = +25°C		22.5	22.7	—	
V_{CC} = +24 V, V_{EE} = 0 V, T_J = T_{low} to T_{high}		22.5	—	—	
V_{CC} = +24 V, V_{EE} = 0 V, T_J = +25°C	V_{OL}	—	1.3	1.5	
V_{CC} = +24 V, V_{EE} = 0 V, T_J = T_{low} to T_{high}		—	—	1.5	
Input Common Mode Voltage Range	V_{ICR}				V
T_J = +25°C		V_{EE} to (V_{CC} –1.0)			
T_J = T_{low} to T_{high}		V_{EE} to (V_{CC} –1.3)			
Common Mode Rejection Ratio (R_S = 10 k)	CMRR	70	90	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω)	PSRR	70	90	—	dB
Power Supply Current	I_D				mA
T_J = +25°C		—	5.0	10	
T_J = T_{low} to T_{high}		—	—	14	

NOTES: 1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, R_L connected to ground, T_J = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 k, C_L = 100 pF)	SR	1.0	1.4	—	V/µs
A_V = –1.0, T_J = T_{low} to T_{high}					
Gain Bandwidth Product (f = 100 kHz, C_L = 100 pF, R_L = 2.0 k)	GBW				MHz
T_J = 25°C		0.9	1.4	—	
T_J = T_{low} to T_{high}		0.7	—	—	
Phase Margin T_J = T_{low} to T_{high}	ϕ_m	—	65	—	Degrees
R_L = 2.0 k, C_L = 100 pF					
Gain Margin	A_m	—	15	—	dB
R_L = 2.0 k, C_L = 100 pF					
Equivalent Input Noise Voltage	e_n	—	22	—	nV/$\sqrt{Hz}$
R_S = 100 Ω, f = 1.0 to 100 kHz					
Total Harmonic Distortion	THD	—	0.02	—	%
A_V = –1.0, R_L = 50 Ω, V_O = 0.5 VRMS, f = 1.0 kHz					

NOTE: In case V_{EE} is disconnected before V_{CC}, a diode between V_{EE} and Ground is recommended to avoid damaging the device.

2

Figure 1. Supply Current versus Suppy Voltage with No Load

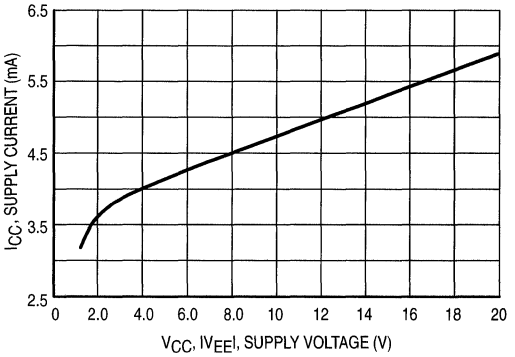


Figure 2. Output Saturation Voltage versus Load Current

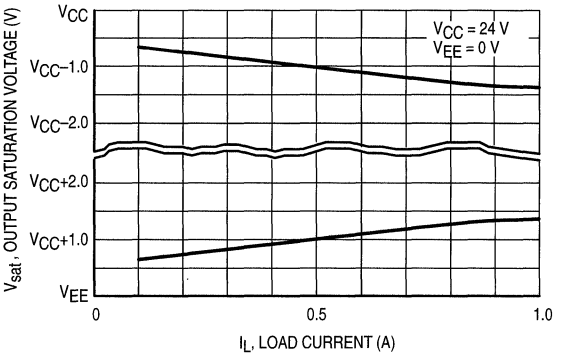


Figure 3. Voltage Gain and Phase versus Frequency

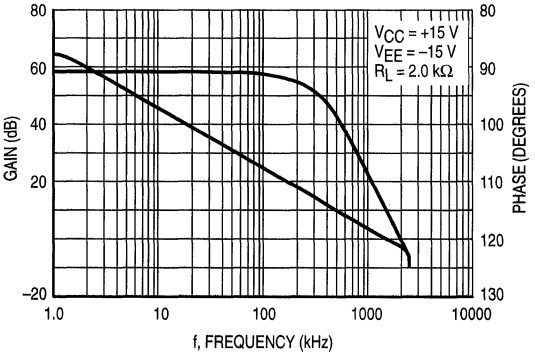


Figure 4. Phase Margin versus Output Load Capacitance

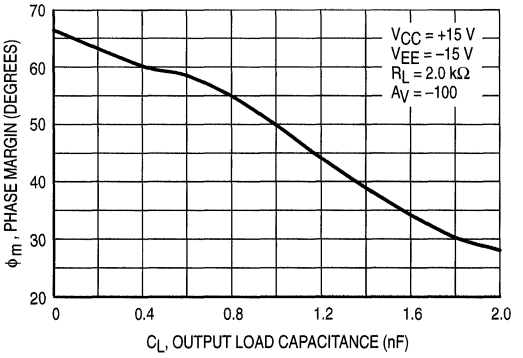


Figure 5. Small Signal Transient Response

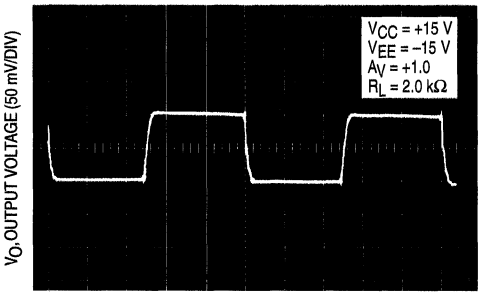


Figure 6. Large Signal Transient Response

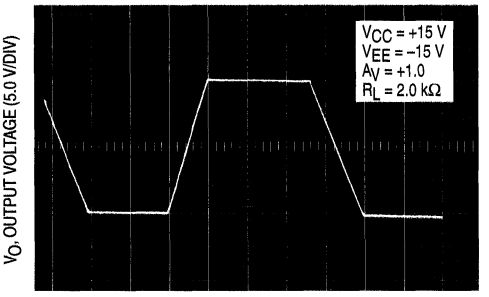


Figure 7. Sine Wave Reponse

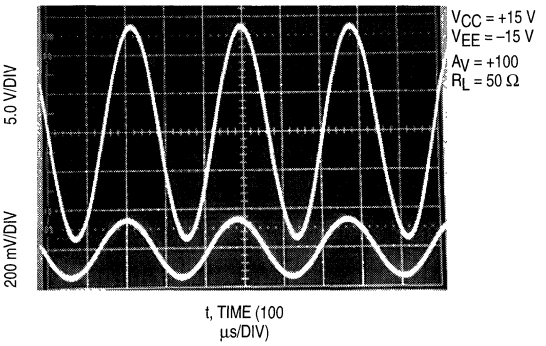
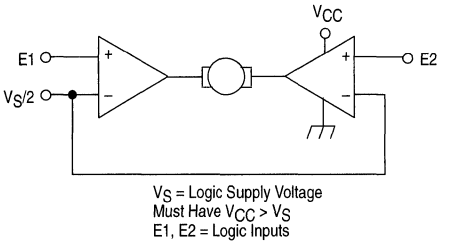
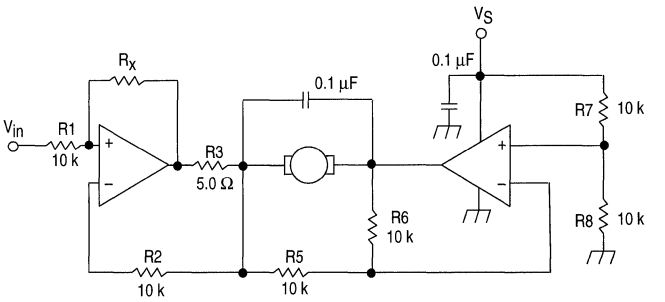


Figure 8. Bidirectional DC Motor Control with Microprocessor–Compatible Inputs



VS = Logic Supply Voltage
Must Have VCC > VS
E1, E2 = Logic Inputs

Figure 9. Bidirectional Speed Control of DC Motors



For circuit stability, ensure that $R_x > \frac{2R3 \cdot R1}{R_M}$ where, R_M = internal resistance of motor.

The voltage available at the terminals of the motor is: $V_M = 2\,(V_1 - \frac{V_S}{2}) + |R_o| \cdot I_M$

where, $|R_o| = \frac{2R3 \cdot R1}{R_x}$ and I_M is the motor current.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(TA)} = \frac{T_{J(max)} - T_A}{R_{\theta JA\ (typ)}}$$

where, $P_{D(TA)}$ = power dissipation allowable at a given operating ambient temperature.

This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum operating junction temperature as listed in the maximum ratings section.

T_A = Maximum desired operating ambient temperature.

$R_{\theta JA(typ)}$ = Typical thermal resistance junction–to–ambient.

TL062
TL064

LOW POWER JFET INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

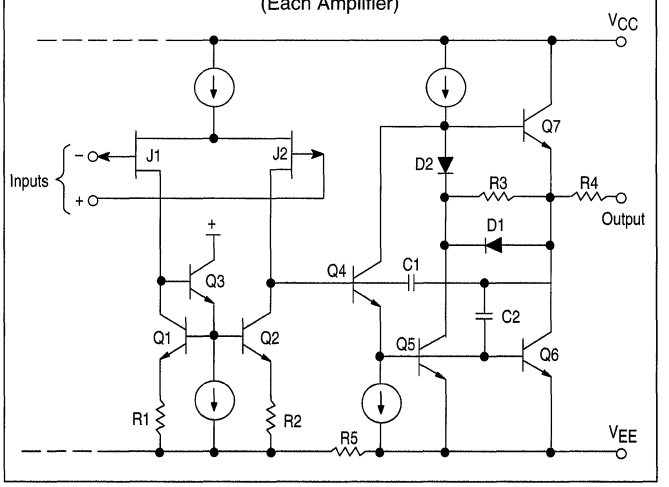
Low Power JFET Input Operational Amplifiers

These JFET input operational amplifiers are designed for low power applications. They feature high input impedance, low input bias current and low input offset current. Advanced design techniques allow for higher slew rates, gain bandwidth products and output swing.

The commercial and vehicular devices are available in Plastic dual in–line and SOIC packages.

- Low Supply Current: 200 μA/Amplifier
- Low Input Bias Current: 5.0 pA
- High Gain Bandwidth: 2.0 MHz
- High Slew Rate: 6.0 V/μs
- High Input Impedance: 10^{12} Ω
- Large Output Voltage Swing: ±14 V
- Output Short Circuit Protection

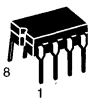
Representative Schematic Diagram
(Each Amplifier)



ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Dual	TL062CD, ACD TL062CP, ACP	T_A = 0° to +70°C	SO–8 Plastic DIP
	TL062VD TL062VP	T_A = –40° to +85°C	SO–8 Plastic DIP
Quad	TL064CD, ACD TL064CN, ACN	T_A = 0° to +70°C	SO–14 Plastic DIP
	TL064VD TL064VN	T_A = –40° to +85°C	SO–14 Plastic DIP

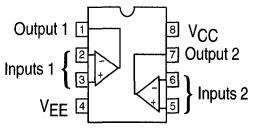
DUAL



P SUFFIX
PLASTIC PACKAGE
CASE 626

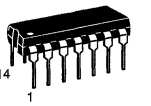
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

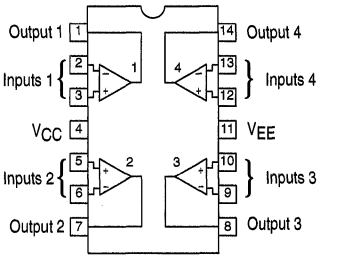
QUAD



N SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	±30	V
Input Voltage Range (Notes 1 and 2)	V_{IR}	±15	V
Output Short Circuit Duration (Note 3)	t_{SC}	Indefinite	sec
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C

NOTES: 1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. The magnitude of the input voltage must never exceed the magnitude of the supply or 15 V, whichever is less.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 1.)

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 0° to +70°C, unless otherwise noted.)

Characteristics	Symbol	TL062AC TL064AC			TL062C TL064C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 50 Ω, V_O = 0V)	V_{IO}							mV
T_A = 25°C		—	3.0	6.0	—	3.0	15	
T_A = 0° to +70°C		—	—	7.5	—	—	20	
Average Temperature Coefficient for Offset Voltage (R_S = 50 Ω, V_O = 0 V)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}							
T_A = 25°C		—	0.5	100	—	0.5	200	pA
T_A = 0° to +70°C		—	—	2.0	—	—	2.0	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}							
T_A = 25°C		—	3.0	200	—	3.0	200	pA
T_A = 0° to +70°C		—	—	2.0	—	—	10	nA
Input Common Mode Voltage Range	V_{ICR}	—	+14.5	+11.5	—	+14.5	+11	V
T_A = 25°C		–11.5	–12.0	—	–11	–12.0	—	
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V)	A_{VOL}							V/mV
T_A = 25°C		4.0	58	—	3.0	58	—	
T_A = 0° to +70°C		4.0	—	—	3.0	—	—	
Output Voltage Swing (R_L = 10 kΩ, V_{ID} = 1.0 V)								V
T_A = 25°C	V_O+	+10	+14	—	+10	+14	—	
	V_O–	—	–14	–10	—	–14	–10	
T_A = 0° to +70°C	V_O+	+10	—	—	+10	—	—	
	V_O–	—	—	–10	—	—	–10	
Common Mode Rejection (R_S = 50 Ω, V_{CM} = V_{ICR} min, V_O = 0 V, T_A = 25°C)	CMR	80	84	—	70	84	—	dB
Power Supply Rejection (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0, T_A = 25°C)	PSR	80	86	—	70	86	—	dB
Power Supply Current (each amplifier) (No Load, V_O = 0 V, T_A = 25°C)	I_D	—	200	250	—	200	250	µA
Total Power Dissipation (each amplifier) (No Load, V_O = 0 V, T_A = 25°C)	P_D	—	6.0	7.5	—	6.0	7.5	mW

2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 4], unless otherwise noted.)

Characteristics	Symbol	TL062V			TL064V			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 50 Ω, V_O = 0V)	V_{IO}							mV
T_A = 25°C		—	3.0	6.0	—	3.0	9.0	
T_A = T_{low} to T_{high}		—	—	9.0	—	—	15	
Average Temperature Coefficient for Offset Voltage	$\Delta V_{IO}/\Delta T$							μV/°C
(R_S = 50 Ω, V_O = 0 V)		—	10	—	—	10	—	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}							
T_A = 25°C		—	5.0	100	—	5.0	100	pA
T_A = T_{low} to T_{high}		—	—	20	—	—	20	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}							
T_A = 25°C		—	30	200	—	30	200	pA
T_A = T_{low} to T_{high}		—	—	50	—	—	50	nA
Input Common Mode Voltage Range (T_A = 25°C)	V_{ICR}	—	+14.5	+11.5	—	+14.5	+11.5	V
		−11.5	−12.0	—	−11.5	−12.0	—	
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V)	A_{VOL}							V/mV
T_A = 25°C		4.0	58	—	4.0	58	—	
T_A = T_{low} to T_{high}		4.0	—	—	4.0	—	—	
Output Voltage Swing (R_L = 10 kΩ, V_{ID} = 1.0 V)								V
T_A = 25°C	V_O+	+10	+14	—	+10	+14	—	
	V_O−	—	−14	−10	—	−14	−10	
T_A = T_{low} to T_{high}	V_O+	+10	—	—	+10	—	—	
	V_O−	—	—	−10	—	—	−10	
Common Mode Rejection	CMR							dB
(R_S = 50 Ω, V_{CM} = V_{ICR} min, V_O = 0, T_A = 25°C)		80	84	—	80	84	—	
Power Supply Rejection	PSR							dB
(R_S = 50 Ω, V_{CM} = 0 V, V_O = 0, T_A = 25°C)		80	86	—	80	86	—	
Power Supply Current (each amplifier)	I_D							μA
(No Load, V_O = 0 V, T_A = 25°C)		—	200	250	—	200	250	
Total Power Dissipation (each amplifier)	P_D							mW
(No Load, V_O = 0 V, T_A = 25°C)		—	6.0	7.5	—	6.0	7.5	

NOTE: 4. T_{low} = −40°C T_{high} = +85°C for TL062,4V

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C, unless otherwise noted.)

Characteristics		Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 kΩ, C_L = 100 pF, A_V = +1.0)		SR	2.0	6.0	—	V/μs
Rise Time (V_{in} = 20 mV, R_L = 10 kΩ, C_L = 100 pF, A_V = +1.0)		t_r	—	0.1	—	μs
Overshoot (V_{in} = 20 mV, R_L = 10 kΩ, C_L = 100 pF, A_V = +1.0)		OS	—	10	—	%
Settling Time		t_S				μs
(V_{CC} = +15 V, V_{EE} = −15 V, A_V = −1.0,	To within 10 mV		—	1.6	—	
R_L = 10 kΩ, V_O = 0 V to +10 V step)	To within 1.0 mV		—	2.2	—	
Gain Bandwidth Product (f = 200 kHz)		GBW	—	2.0	—	MHz
Equivalent Input Noise (R_S = 100 Ω, f = 1.0 kHz)		e_n	—	47	—	nV/$\sqrt{Hz}$
Input Resistance		R_i	—	10^{12}	—	W
Channel Separation (f = 10 kHz)		CS	—	120	—	dB

Figure 1. Maximum Power Dissipation versus Temperature for Package Variations

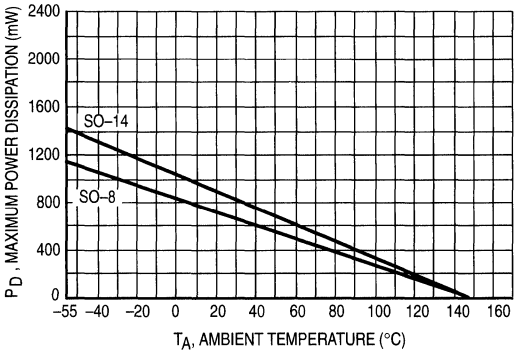


Figure 2. Output Voltage Swing versus Supply Voltage

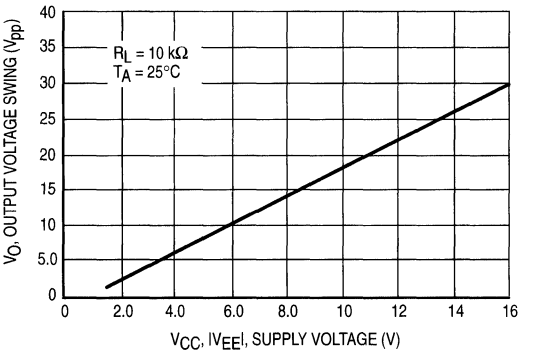


Figure 3. Output Voltage Swing versus Temperature

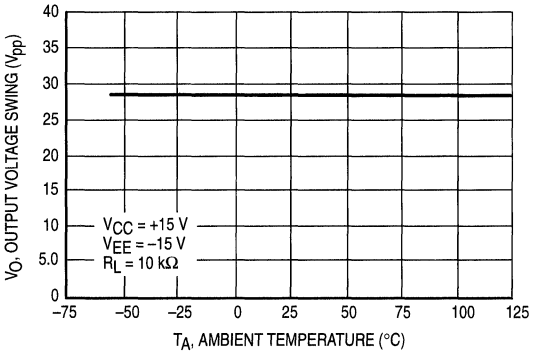


Figure 4. Output Voltage Swing versus Load Resistance

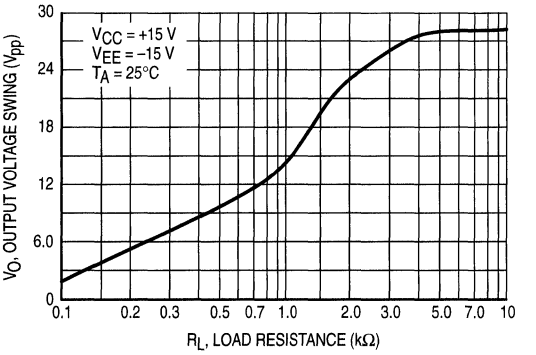


Figure 5. Output Voltage Swing versus Frequency

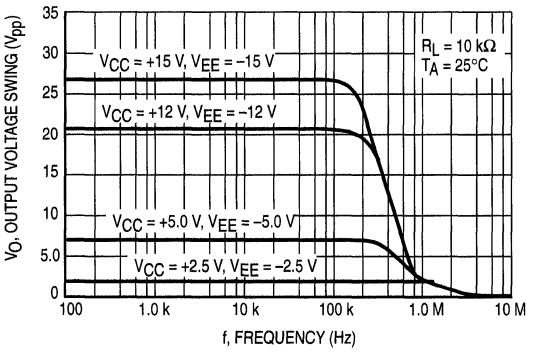
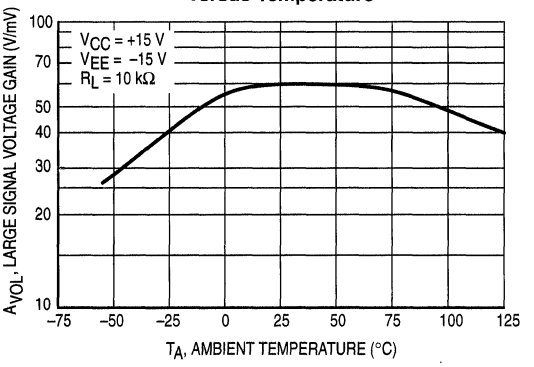


Figure 6. Large Signal Voltage Gain versus Temperature



2

Figure 7. Open Loop Voltage Gain and Phase versus Frequency

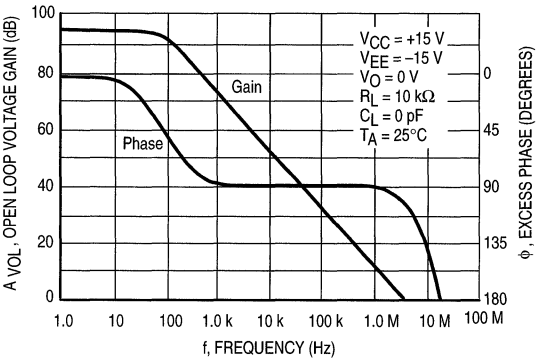


Figure 8. Supply Current per Amplifier versus Supply Voltage

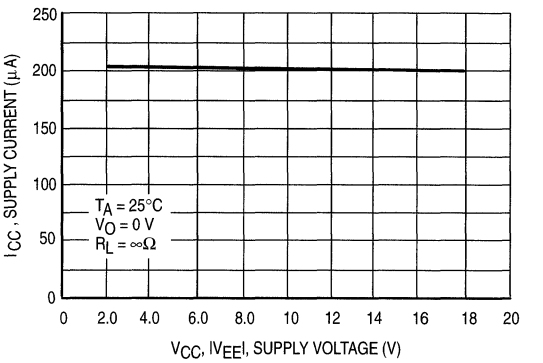


Figure 9. Supply Current per Amplifier versus Temperature

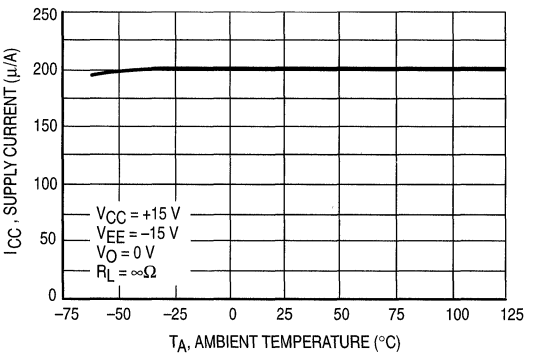


Figure 10. Total Power Dissipation versus Temperature

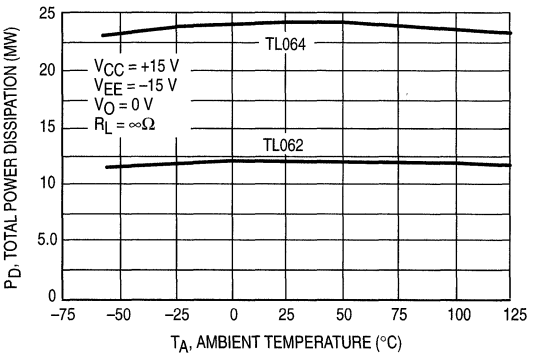


Figure 11. Common Mode Rejection versus Temperature

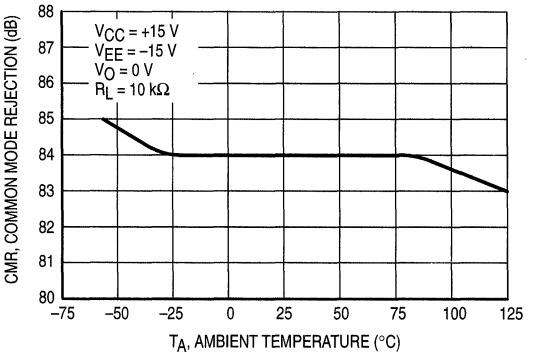


Figure 12. Common Mode Rejection versus Frequency

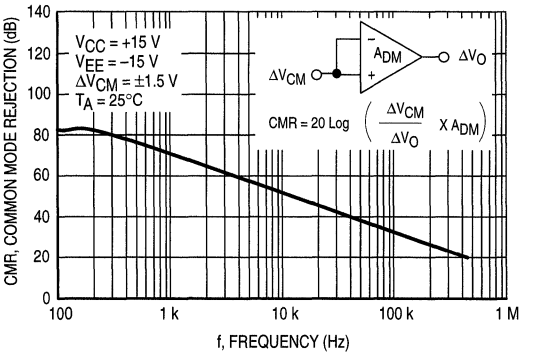


Figure 13. Power Supply Rejection versus Frequency

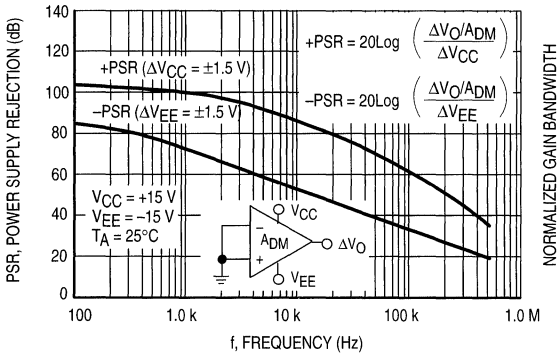


Figure 14. Normalized Gain Bandwidth Product, Slew Rate and Phase Margin versus Temperature

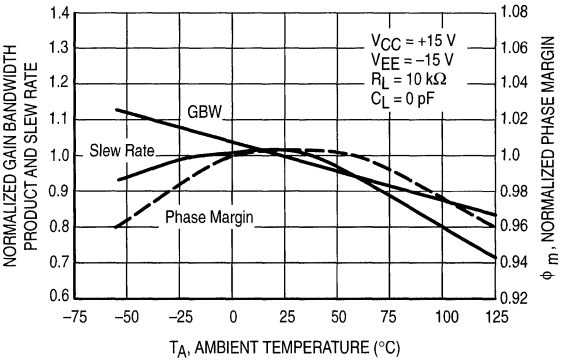


Figure 15. Input Bias Current versus Temperature

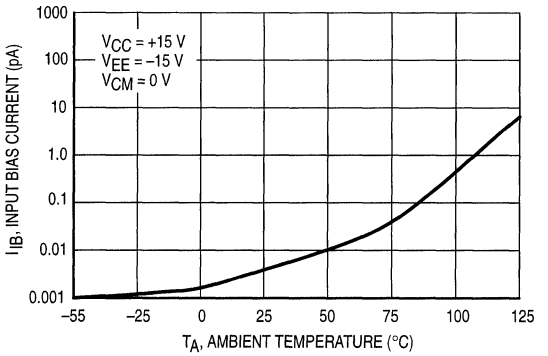


Figure 16. Input Noise Voltage versus Frequency

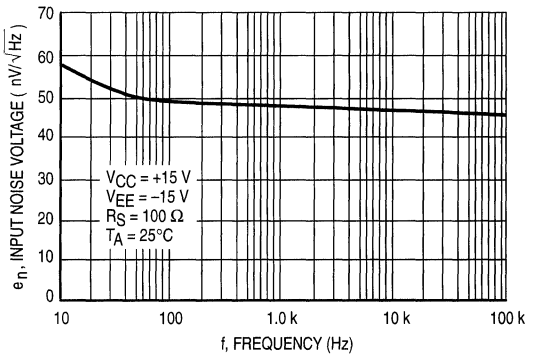


Figure 17. Small Signal Response

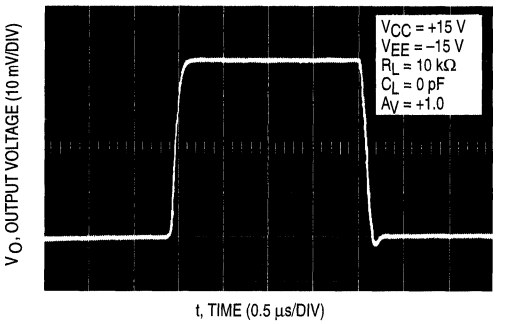
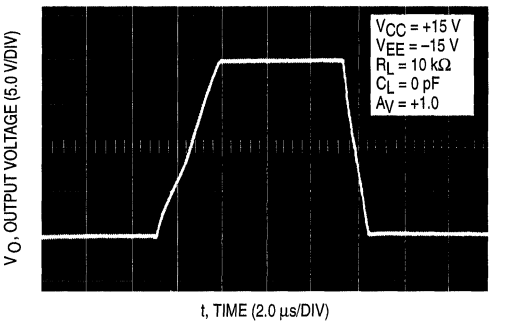


Figure 18. Large Signal Response



2

Figure 19. AC Amplifier

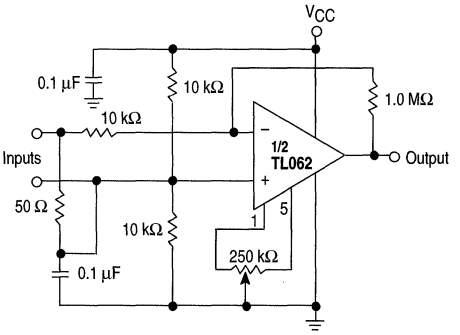


Figure 20. High–Q Notch Filter

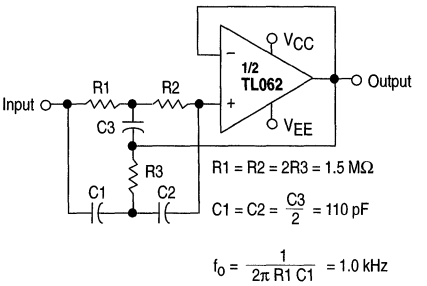


Figure 21. Instrumentation Amplifier

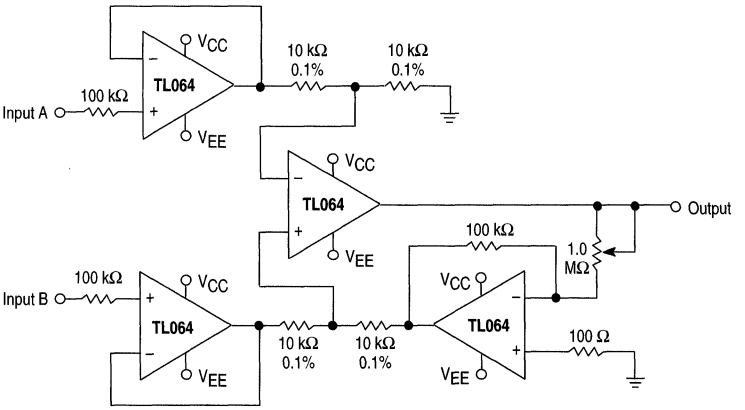


Figure 22. 0.5 Hz Square–Wave Oscillator

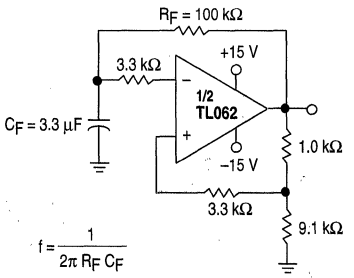
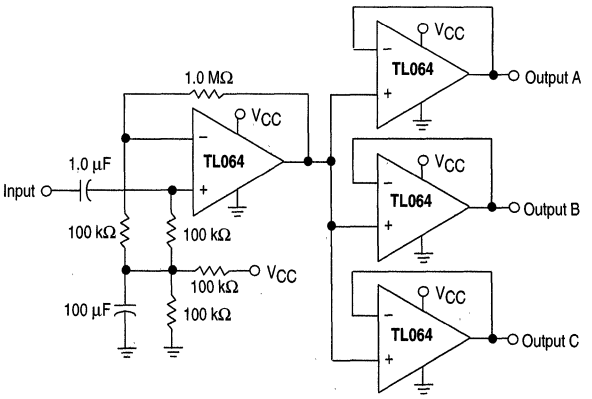


Figure 23. Audio Distribution Amplifier



TL071C,AC
TL072C,AC
TL074C,AC

Low Noise, JFET Input Operational Amplifiers

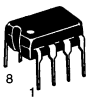
These low noise JFET input operational amplifiers combine two state–of–the–art analog technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input device for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. Moreover, the devices exhibit low noise and low harmonic distortion, making them ideal for use in high fidelity audio amplifier applications.

These devices are available in single, dual and quad operational amplifiers which are pin–compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products.

- Low Input Noise Voltage: 18 nV/$\sqrt{Hz}$ Typ
- Low Harmonic Distortion: 0.01% Typ
- Low Input Bias and Offset Currents
- High Input Impedance: 10^{12} Ω Typ
- High Slew Rate: 13 V/μs Typ
- Wide Gain Bandwidth: 4.0 MHz Typ
- Low Supply Current: 1.4 mA per Amp

LOW NOISE, JFET INPUT OPERATIONAL AMPLIFIERS

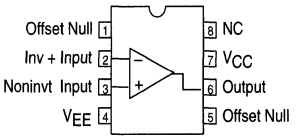
SEMICONDUCTOR TECHNICAL DATA



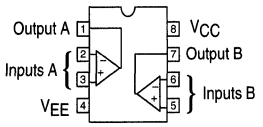
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

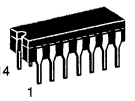
PIN CONNECTIONS



TL071 (Top View)

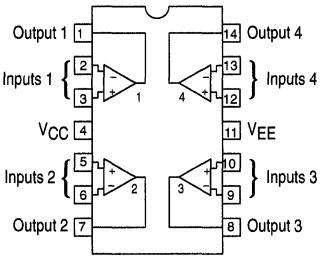


TL072 (Top View)



N SUFFIX
PLASTIC PACKAGE
CASE 646
(TL074 Only)

PIN CONNECTIONS



TL074 (Top View)

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	TL071ACD, CD	T_A = 0° to +70°C	SO–8
	TL071ACP, CP		Plastic DIP
Dual	TL072ACD, CD	T_A = 0° to +70°C	SO–8
	TL072ACP, CP		Plastic DIP
Quad	TL074ACN, CN	T_A = 0° to +70°C	Plastic DIP

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+18 −18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Power Dissipation Plastic Package (N, P) Derate above T_A = +47°C	 P_D $1/\theta_{JA}$	 680 10	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 V, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low} [Note 3])

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ k, V_{CM} = 0) TL071C, TL072C TL074C TL07_AC	V_{IO}	 — — —	 — — —	 13 13 7.5	mV
Input Offset Current (V_{CM} = 0) (Note 4) TL07_C TL07_AC	I_{IO}	 — —	 — —	 2.0 2.0	nA
Input Bias Current (V_{CM} = 0) (Note 4) TL07_C TL07_AC	I_{IB}	 — —	 — —	 7.0 7.0	nA
Large–Signal Voltage Gain (V_O = ±10 V, $R_L \ge 2.0$ k) TL07_C TL07_AC	A_{VOL}	 15 25	 — —	 — —	V/mV
Output Voltage Swing (Peak–to–Peak) ($R_L \ge 10$ k) ($R_L \ge 2.0$ k)	V_O	 24 20	 — —	 — —	V

NOTES: 3. T_{low} = 0°C for TL071C,AC, TL072C,AC, TL074C,AC; T_{high} = +70°C for TL071C,AC, TL072C,AC, TL074C,AC
4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

Figure 1. Unity Gain Voltage Follower

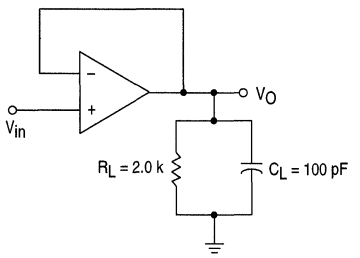
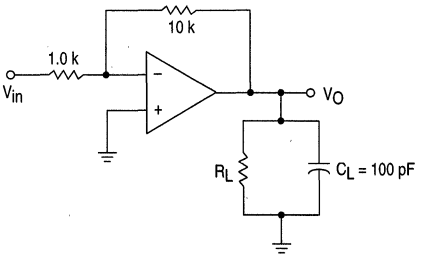


Figure 2. Inverting Gain of 10 Amplifier



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ k, V_{CM} = 0) TL071C, TL072C TL074C TL07_AC	V_{IO}	 — — —	 3.0 3.0 3.0	 10 10 6.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 50 Ω, $T_A = T_{low}$ to T_{high} (Note 3)	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0) (Note 4) TL07_C TL07_AC	I_{IO}	 — —	 5.0 5.0	 50 50	pA
Input Bias Current (V_{CM} = 0) (Note 4) TL07_C TL07_AC	I_{IB}	 — —	 30 30	 200 200	pA
Input Resistance	r_i	—	10^{12}	—	Ω
Common Mode Input Voltage Range TL07_C TL07_AC	V_{ICR}	 ±10 ±11	 +15, –12 +15, –12	 — —	V
Large–Signal Voltage Gain (V_O = ±10 V, $R_L \ge$ 2.0 k) TL07_C TL07_AC	A_{VOL}	 25 50	 150 150	 — —	V/mV
Output Voltage Swing (Peak–to–Peak) (R_L = 10 k)	V_O	24	28	—	V
Common Mode Rejection Ratio ($R_S \le 10$ k) TL07_C TL07_AC	CMRR	 70 80	 100 100	 — —	dB
Supply Voltage Rejection Ratio ($R_S \le 10$ k) TL07_C TL07_AC	PSRR	 70 80	 100 100	 — —	dB
Supply Current (Each Amplifier)	I_D	—	1.4	2.5	mA
Unity Gain Bandwidth	BW	—	4.0	—	MHz
Slew Rate (See Figure 1) V_{in} = 10 V, R_L = 2.0 k, C_L = 100 pF	SR	—	13	—	v/μs
Rise Time (See Figure 1)	t_r	—	0.1	—	μs
Overshoot (V_{in} = 20 mV, R_L = 2.0 k, C_L = 100 pF)	OS	—	10	—	%
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1000 Hz	e_n	—	18	—	nV/$\sqrt{Hz}$
Equivalent Input Noise Current R_S = 100 Ω, f = 1000 Hz	i_n	—	0.01	—	pA/$\sqrt{Hz}$
Total Harmonic Distortion V_O (RMS) = 10 V, $R_S \le$ 1.0 k, $R_L \ge$ 2.0 k, f = 1000 Hz	THD	—	0.01	—	%
Channel Separation A_V = 100	CS	—	120	—	dB

NOTES: 3. T_{low} = 0°C for TL071C,AC, TL072C,AC, TL074C,AC T_{high} = +70°C for TL071C,AC, TL072C,AC, TL074C,AC

4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

2

Figure 3. Input Bias Current versus Temperature

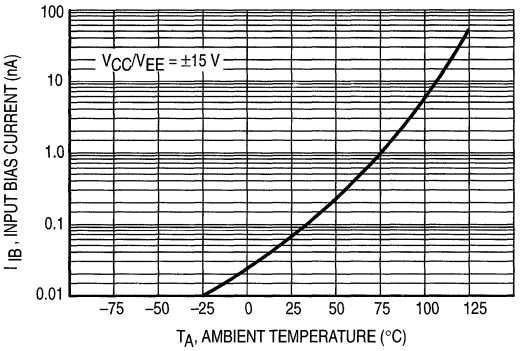


Figure 4. Output Voltage Swing versus Frequency

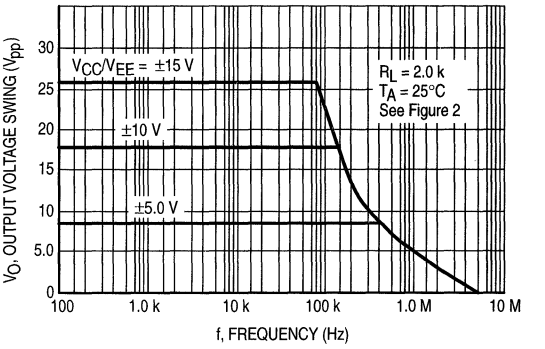


Figure 5. Output Voltage Swing versus Load Resistance

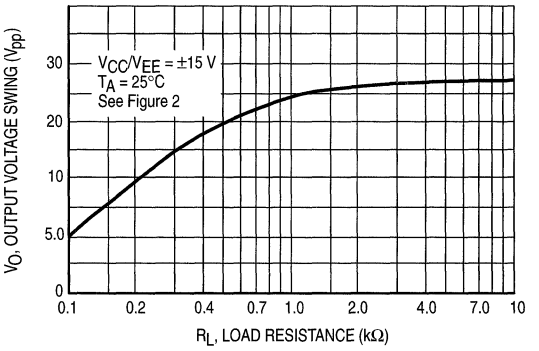


Figure 6. Output Voltage Swing versus Supply Voltage

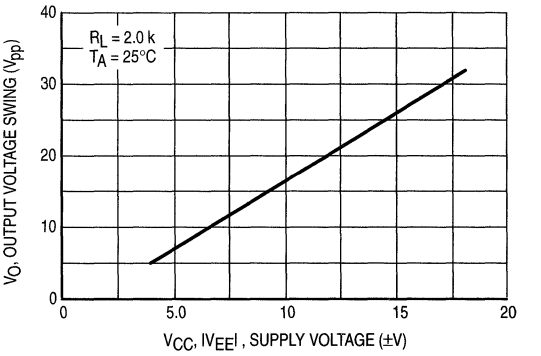


Figure 7. Output Voltage Swing versus Temperature

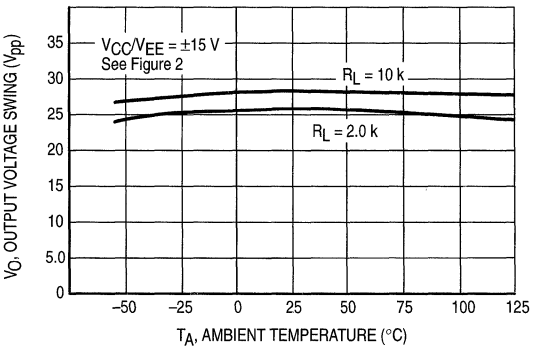


Figure 8. Supply Current per Amplifier versus Temperature

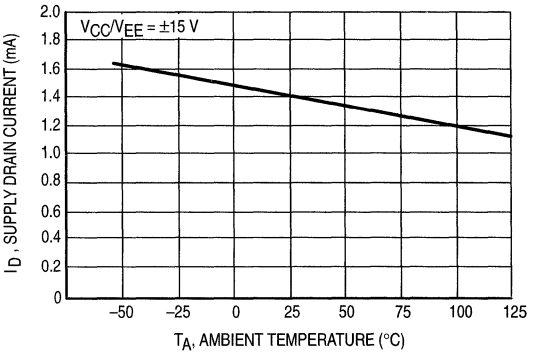


Figure 9. Large Signal Voltage Gain and Phase Shift versus Frequency

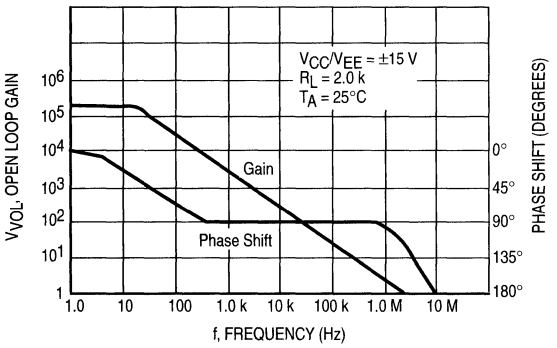


Figure 10. Large Signal Voltage Gain versus Temperature

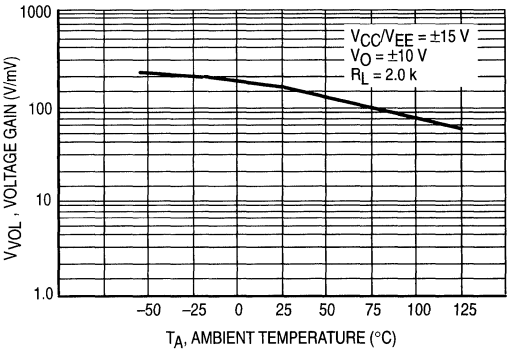


Figure 11. Normalized Slew Rate versus Temperature

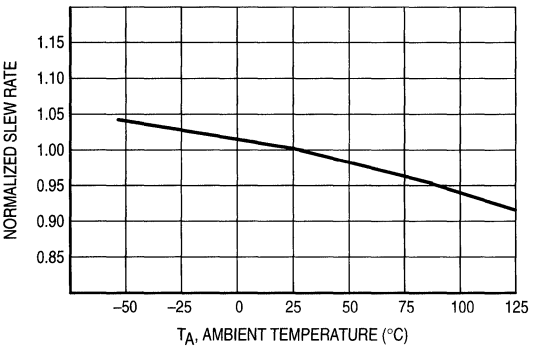


Figure 12. Equivalent Input Noise Voltage versus Frequency

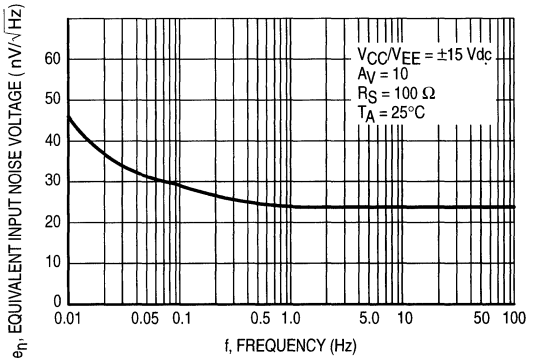
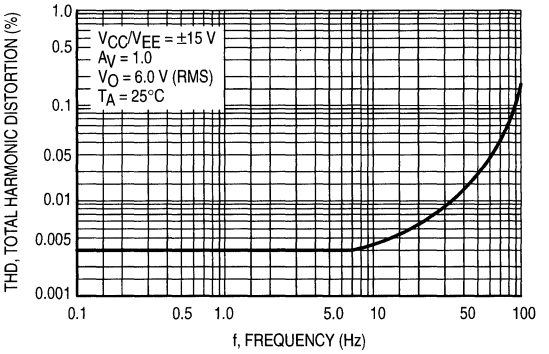


Figure 13. Total Harmonic Distortion versus Frequency



2

Representative Schematic Diagram
(Each Amplifier)

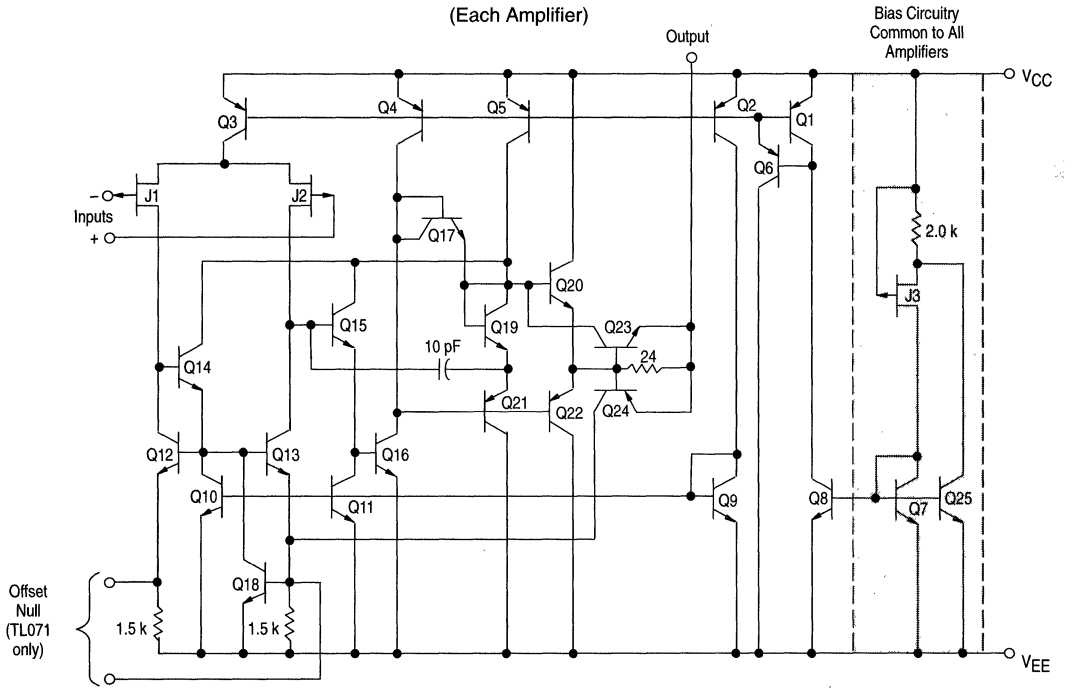


Figure 14. Audio Tone Control Amplifier

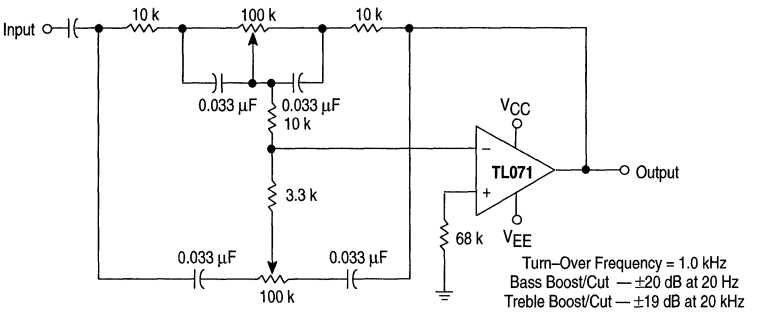
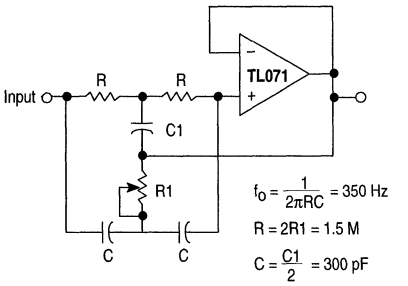


Figure 15. High Q Notch Filter



TL081C,AC
TL082C,AC
TL084C,AC

JFET Input Operational Amplifiers

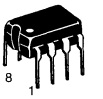
These low–cost JFET input operational amplifiers combine two state–of–the–art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin–compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products.

- Input Offset Voltage Options of 6.0 mV and 15 mV Max
- Low Input Bias Current: 30 pA
- Low Input Offset Current: 5.0 pA
- Wide Gain Bandwidth: 4.0 MHz
- High Slew Rate: 13 V/μs
- Low Supply Current: 1.4 mA per Amplifier
- High Input Impedance: $10^{12}\ \Omega$

JFET INPUT OPERATIONAL AMPLIFIERS

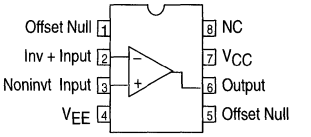
SEMICONDUCTOR TECHNICAL DATA



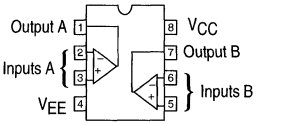
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

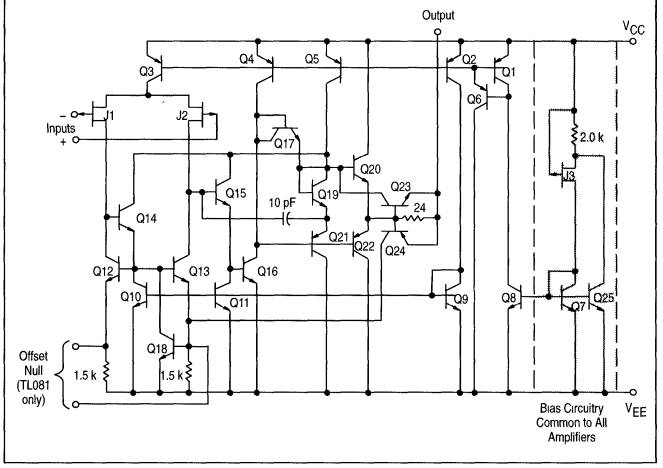


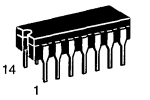
TL081 (Top View)



TL082 (Top View)

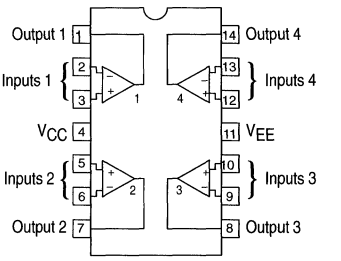
Representative Circuit Schematic (Each Amplifier)





N SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



TL084 (Top View)

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	TL081ACD, CD	T_A = 0° to +70°C	SO–8
	TL081ACP, CP		Plastic DIP
Dual	TL082ACD, CD	T_A = 0° to +70°C	SO–8
	TL082ACP, CP		Plastic DIP
Quad	TL084ACN, CN	T_A = 0° to +70°C	Plastic DIP

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+18 −18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Power Dissipation Plastic Package (N, P) Derate above T_A = +47°C	 P_D $1/\theta_{JA}$	 680 10	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 V, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ k, V_{CM} = 0) TL081C, TL082C TL084C TL08_AC	V_{IO}	 — — —	 — — —	 20 20 7.5	mV
Input Offset Current (V_{CM} = 0) (Note 4) TL08_C TL08_AC	I_{IO}	 — —	 — —	 5.0 3.0	nA
Input Bias Current (V_{CM} = 0) (Note 4) TL08_C TL08_AC	I_{IB}	 — —	 — —	 10 7.0	nA
Large–Signal Voltage Gain (V_O= ±10 V,$R_L \ge 2.0$ k) TL08_C TL08_AC	A_{VOL}	 15 25	 — —	 — —	V/mV
Output Voltage Swing (Peak–to–Peak) ($R_L \ge 10$ k) ($R_L \ge 2.0$ k)	V_O	 24 20	 — —	 — —	V

NOTES: 3. T_{low} = 0°C for TL081AC,C; TL082AC,C; TL084AC,C T_{high} = +70°C for TL081AC; TL082AC,C; TL084AC,C
4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in Junction Temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

Figure 1. Unity Gain Voltage Follower

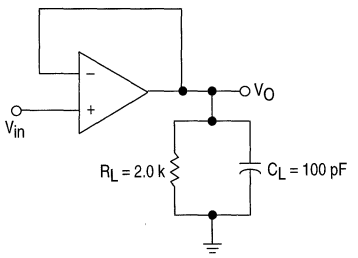
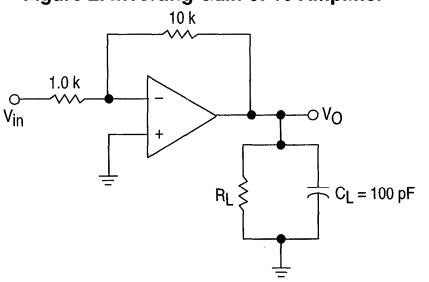


Figure 2. Inverting Gain of 10 Amplifier



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ k, V_{CM} = 0) TL081C, TL082C TL084C TL08_AC	V_{IO}	 — — —	 5.0 5.0 3.0	 15 15 6.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 50 Ω, T_A = T_{low} to T_{high} (Note 3)	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0) (Note 4) TL08_C TL08_AC	I_{IO}	 — —	 5.0 5.0	 200 100	pA
Input Bias Current (V_{CM} = 0) (Note 4) TL08_C TL08_AC	I_{IB}	 — —	 30 30	 400 200	pA
Input Resistance	r_i	—	10^{12}	—	Ω
Common Mode Input Voltage Range TL08_C TL08_AC	V_{ICR}	 ±10 ±11	 +15, −12 +15, −12	 — —	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \geq 2.0$ k) TL08_C TL08_AC	A_{VOL}	 25 50	 150 150	 — —	V/mV
Output Voltage Swing (Peak–to–Peak) (R_L = 10 k)	V_O	24	28	—	V
Common Mode Rejection Ratio ($R_S \leq 10$ k) TL08_C TL08_AC	CMRR	 70 80	 100 100	 — —	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k) TL08_C TL08_AC	PSRR	 70 80	 100 100	 — —	dB
Supply Current (Each Amplifier)	I_D	—	1.4	2.8	mA
Unity Gain Bandwidth	BW	—	4.0	—	MHz
Slew Rate (See Figure 1) V_{in} = 10 V, R_L = 2.0 k, C_L = 100 pF	SR	—	13	—	V/μs
Rise Time (See Figure 1)	t_r	—	0.1	—	μs
Overshoot (V_{in} = 20 mV, R_L = 2.0 k, C_L = 100 pF)	OS	—	10	—	%
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1000 Hz	e_n	—	25	—	$nV/\sqrt{Hz}$
Channel Separation A_V = 100	CS	—	120	—	dB

NOTES: 3. T_{low} = 0°C for TL081AC,C
TL082AC,C
TL084AC,C
T_{high} = +70°C for TL081AC
TL082AC,C
TL084AC,C

4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in Junction Temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

2

Figure 3. Input Bias Current versus Temperature

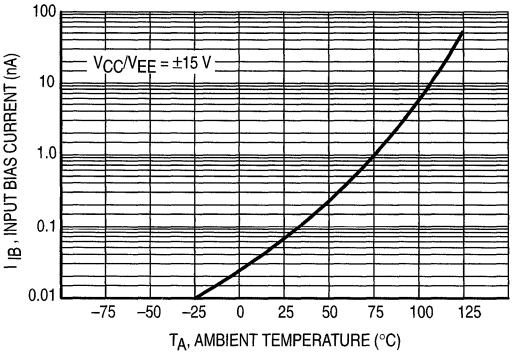


Figure 4. Output Voltage Swing versus Frequency

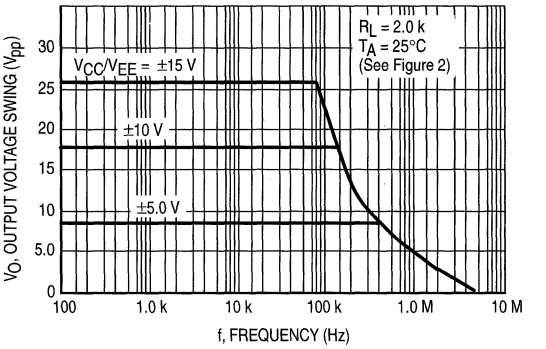


Figure 5. Output Voltage Swing versus Load Resistance

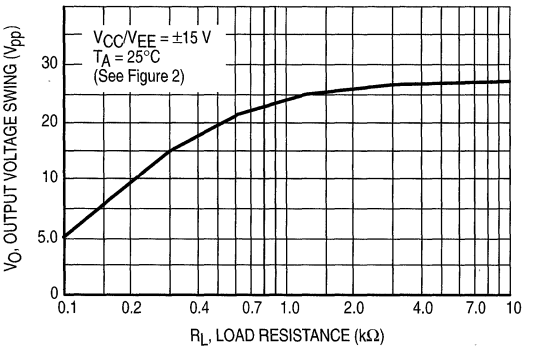


Figure 6. Output Voltage Swing versus Supply Voltage

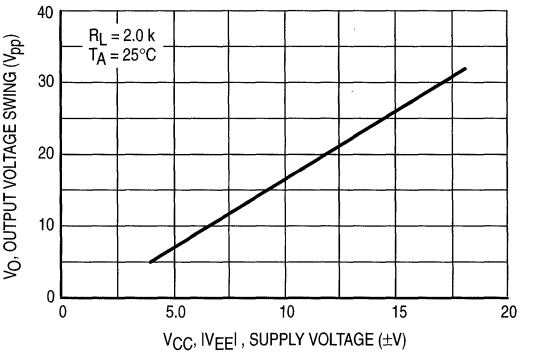


Figure 7. Output Voltage Swing versus Temperature

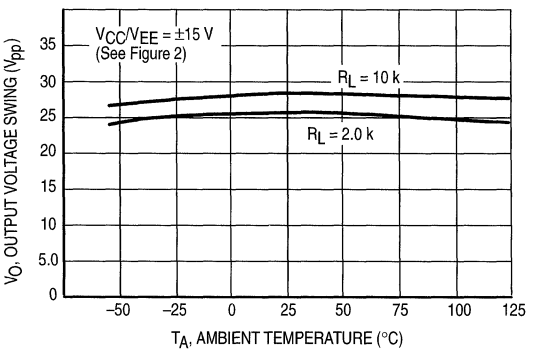


Figure 8. Supply Current per Amplifier versus Temperature

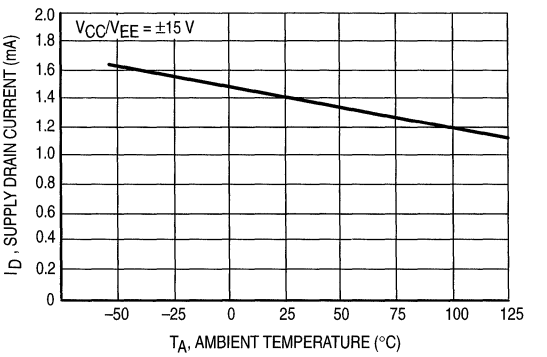


Figure 9. Large Signal Voltage Gain and Phase Shift versus Frequency

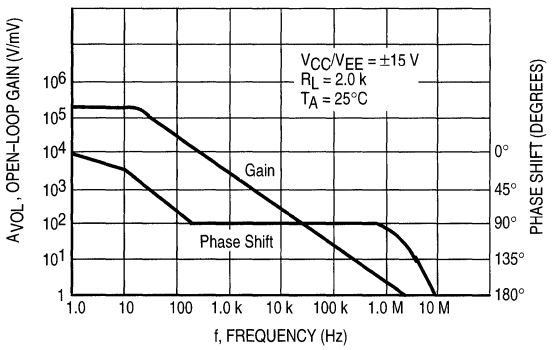


Figure 10. Large Signal Voltage Gain versus Temperature

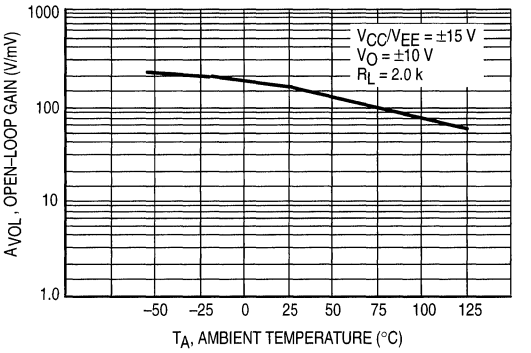


Figure 11. Normalized Slew Rate versus Temperature

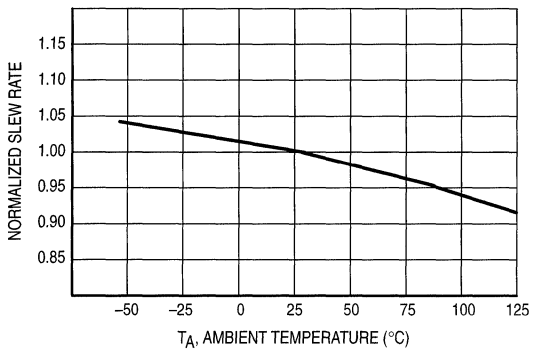


Figure 12. Equivalent Input Noise Voltage versus Frequency

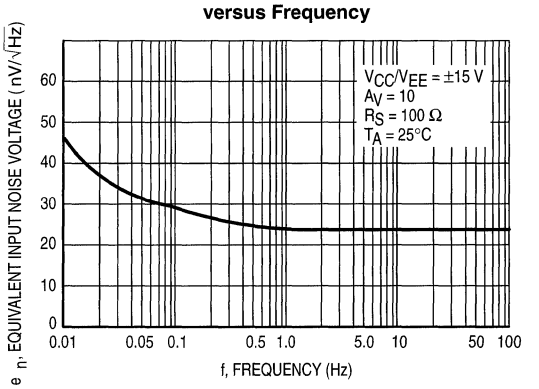
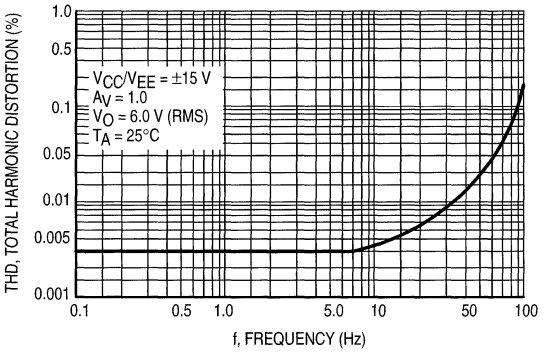


Figure 13. Total Harmonic Distortion versus Frequency



2

Figure 14. Positive Peak Detector

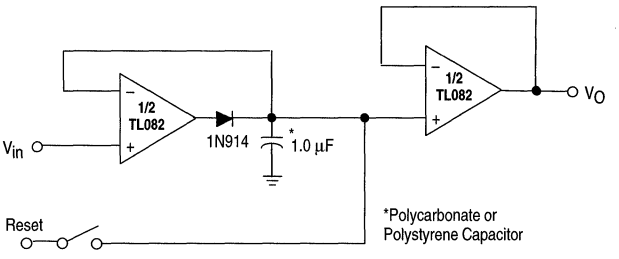
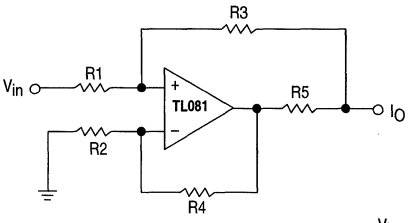
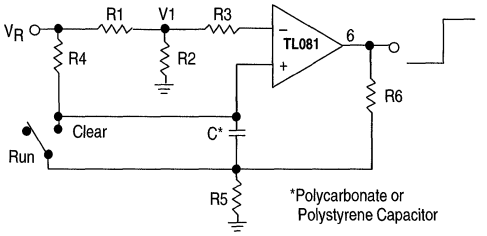


Figure 15. Voltage Controlled Current Source



If R1 through R4 > > R5 then $I_{out} = \frac{V_{in}}{R5}$

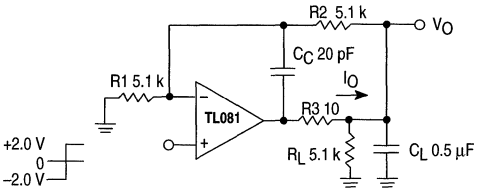
Figure 16. Long Interval RC Timer



Time (t) = R4 Cℓn (V_R/V_R–V_I), $R_3 = R_4$, $R_5 = 0.1\ R_6$
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer
V_R = 10 V C = 1.0 mF R3 = R4 = 144 M
R6 = 20 k R5 = 2.0 k R1 = R2 = 1.0 k

Figure 17. Isolating Large Capacitive Loads



- Overshoot < 10%
- t_S = 10 µs
- When driving large C_L, the V_O slew rate is determined by C_L and $I_{O(max)}$:

$$\frac{\Delta V_O}{\Delta t} = \frac{I_O}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

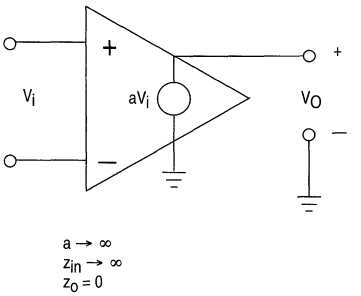
Addendum Operational Amplifier Application Information

2

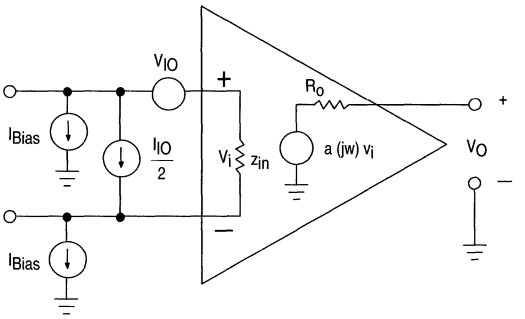
The Ideal Operational Amplifier

An ideal op amp has infinite input impedance, infinite gain, and zero output impedance. Its output is proportional to the differential voltage between the inputs. In reality, slight mismatches between the inputs create an error voltage and current, the input impedance is finite, requiring a small bias current, and gain and operating frequency are limited.

Ideal Op Amp



Equivalent Circuit for Actual Op Amp



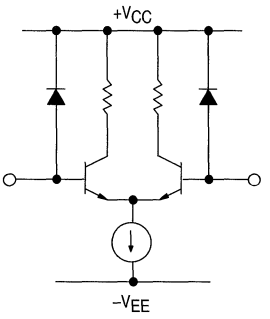
ESD Protection

Newer Motorola devices are equipped with either electrostatic discharge (ESD) diodes or CEO clamps on the inputs to increase their reliability. ESD diodes are connected with the anode attached to the input and the cathode to V_{CC}. During normal operation, the diode should be transparent to the user. However, if the input exceeds V_{CC} by more than a diode drop, the ESD diode will be forward biased and will provide a current path from the input to V_{CC}. Unless the current is limited externally the device could be damaged from overheating.

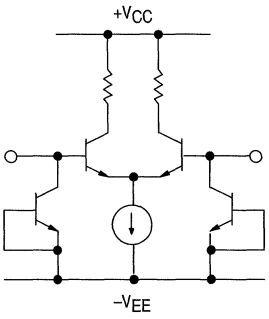
An alternate scheme uses a CEO transistor clamp with the collector connected to the input and the emitter and base connected to V_{EE}. This ESD protection method is totally transparent to the user. Although it is not recommended that the inputs be allowed to exceed V_{CC}, the CEO clamp will not affect device operation. The inputs should never exceed V_{EE}, with or without ESD protection. Single supply op amps are particularly sensitive to damage in a reverse bias condition.

If ESD protection is used on an amplifier, the ESD scheme used will be identified in the data sheet.

ESD Diodes



CEO Clamps

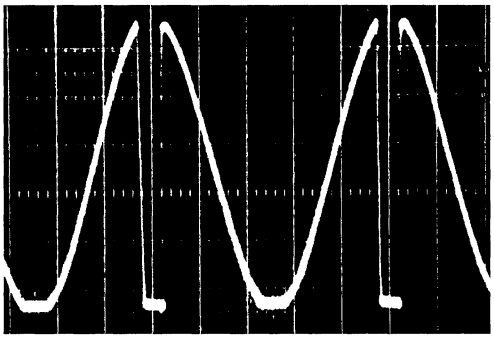


JFET Inputs versus Bipolar Inputs

Although JFET input op amps are generally associated with high speed, there are now bipolar input op amps with comparable slew rates. JFETS do offer higher input impedance and lower input bias current than a typical bipolar input. But for the lowest noise and offset voltage, a bipolar input op amp is a better choice. A bipolar input is also required for true single supply operation. Any op amp can be operated with one supply. But the common mode input voltage range of a single supply op amp includes ground.

Phase Reversal

Most op amp data sheets describe both a maximum input voltage and a minimum common mode input voltage range for the device. The input voltage limit given in the Maximum Ratings Table is considered to be the highest voltage that can be applied without damaging the device. It does not guarantee the device will function normally or within the given electrical specifications. The input common mode voltage range (V_{ICR}), on the other hand, provides the maximum input voltage (for the conditions listed) for normal operation. Exceeding the input common mode range may cause the device to exceed the electrical specifications, latch or go into phase reversal. (As shown in figure at right.)



In a latch condition, the op amp output goes to one of the supply rails, and will remain in that state until the power is removed and reapplied with the error condition corrected. In phase reversal, a normal output low would be seen as an output high, but phase reversal will self correct once the input drops below a certain level. The input voltage required for phase reversal to occur varies, but it is usually seen if the input voltage approaches or exceeds the supply voltage. As you can see in the figure the output is clipping on the negative peaks, and phase reversing on the positive peaks. But as the input drops on the negative going part of the waveform, the output returns the the correct state without powering down the device.

Thermal Considerations

Thermal resistance (θ_{JA}) information is given on most packages in the back of the data book. Low power op amps can handle a short circuit current condition indefinitely. Since some of the higher current drive op amps can deliver a hundred milliamps to an amp in a short circuit condition, extra care is needed to ensure that the maximum junction temperature of the part is not exceeded.

$T_J = T_A + P_D Q_{JA}$

T_J = Junction Temperature (Should not exceed 150°C)

T_A = Ambient Temperature

P_D = Power Dissipation

Q_A = Package Thermal Impedance

Stability and Compensation

Most op amps are internally compensated, enabling them to be used in a unity gain configuration. Uncompensated or decompensated amplifiers have a higher slew rate if no external compensation capacitor is used, but must either be used in a gain of 2 or more or with positive feedback to ensure stable operation. When externally compensating an amplifier, use a capacitor equal or greater than the value recommended in the data sheet. Since the external loop affects the stability of the op amp, the amplifier needs to be evaluated in the circuit and over temperature to determine the minimum amount of compensation required.

Insufficient compensation will cause a high frequency oscillation — higher than the unity gain frequency of the device. This high frequency oscillation is indicative of an instability in the Miller loop, internal to the device. Lower frequency oscillation (below the unity gain frequency of the amplifier) is generally caused by an instability in the outer loop.

The two primary causes of low frequency oscillation are capacitive loading on the output and high differential source resistance. Capacitive loading, which can be either distributed capacitance or an actual load capacitor, can be a problem with as little as 100 pF. Sensitivity to load capacitance varies from op amp to op amp and is not always given in the data sheets. To compensate for capacitive loading, add a small resistor in series with the output. Depending on the load and the external loop, 10 Ω to 100 Ω is generally sufficient (see Figure A). For high capacitive loading, (C_L>1500 pF) a capacitor in the feedback loop may also be necessary (see Figure B).

Keeping the differential source resistance low not only limits the noise generated in the circuit, but avoids stability problems as well. Most op amps are stable with a source resistance of up to 2 kΩ, but will vary from op amp to op amp. The differential source resistance (which includes any feedback resistance) combines with the input capacitance of the op amp to create a low frequency pole. The higher the resistance, the more likely you are to have an oscillation problem. Adding a small capacitor in parallel with the feedback resistor may solve the problem (see Figure C). The capacitor should be greater than the input capacitance of the op amp which is typically about 10 pF.

Figure A. Compensation Circuit for Moderate Capacitive Loads

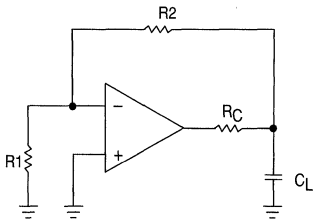


Figure B. Compensation Circuit for High Capacitive Loads

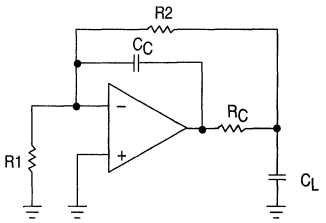
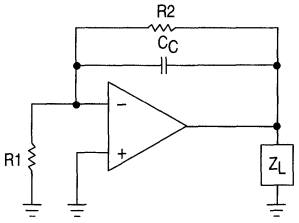


Figure C. Compensation for High Source Impedance



Layout Considerations

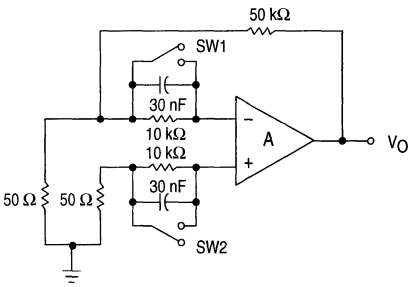
Higher frequency op amps may require special attention to layout. Since most layout problems are not reflected in computer simulations, it is worth it to follow proper layout rules consistently. Some suggestions:

- *Always* bypass the supply pins with at least 0.01 μF to ground, whether or not it is a high frequency application. Some amplifiers have a much lower power supply rejection with respect to the negative supply than to the positive supply due to the internal compensation. A larger bypass capacitor from V_{EE} to ground may be used to prevent high frequency transients from appearing on the output. Generally 10 μF to 20 μF is sufficient.
- Make sure you have a good ground plane.
- Keep AC and DC grounds separate.
- Don't use proto boards or wire wrap for high frequency circuits.
- Use appropriate external components — avoid electrolytics in high frequency paths.
- Keep high frequency paths short (including the leads on discrete components).
- Ground the inputs of unused op amps.

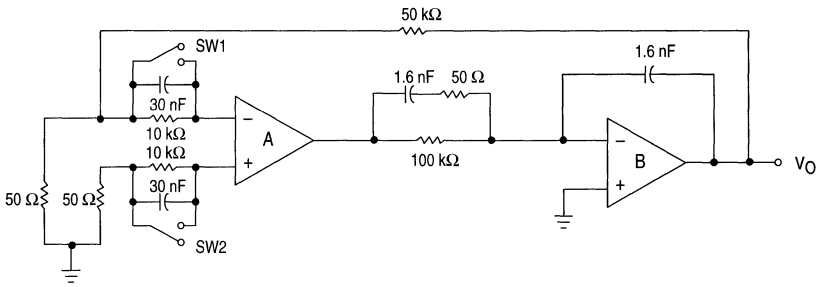
Test Information

The following circuit can be used to test V_{IO}, I_{IO}, and I_{IB}. Op Amp A is the device under test, and Op Amp B is a buffer amplifier which reduces CMRR errors and improves the accuracy of the measurement. The 30 nF capacitors across the 10k Ω source resistors are for stability and may not be needed.

A) Without Buffer Amplifier



B) With Buffer Amplifier



V_{IO} can be measured directly with SW1 and SW2 closed.

To determine I_{IB-}:

- Measure V_{IO} with both switches close,
- Open SW1 only; Measure V_{IO1}

To determine I_{IB+}:

- Close SW1 and open SW2; Measure V_{IO2}

I_{IO} equals the difference between I_{IB+} and I_{IB-}

GLOSSARY

2

Input Offset Voltage (V_{IO}) — The voltage which must be applied between the inputs of an op amp to obtain a zero output voltage. For an ideal op amp, V_{IO} would be zero. Some vendors abbreviate it V_{OS}.

Input Bias Current (I_{IB}) — The current flowing in or out of both inputs of an op amp. JFET input op amps provide the lowest input bias current; typically in the picoamp range. A bipolar input op amp is typically in nanoamps. I_{IB} is highly sensitive to slight process variations and can vary an order of magnitude.

Input Offset Current (I_{IO}) — Ideally, the bias currents on the two inputs are equal. The input offset current is the difference between the two currents when the output is at zero volts. Sometimes abbreviated I_{OS}. This should not be confused with the output short circuit current (I_{SC}).

Input Common Mode Voltage Range (V_{ICR}) — The maximum input voltage range for normal operation within given specifications. Exceeding the input common mode range generally will not damage the inputs if the maximum ratings are not exceeded. However, V_{IO} may not meet the specification given in the data sheet, and phase reversal may occur as the input voltage approaches V_{CC} or V_{EE}. Sometimes abbreviated V_{CM}.

Common Mode Rejection Ratio (CMR or CMRR) — CMRR is defined as the ratio of the common mode gain to the differential mode gain. It is also equal to the ratio of the input common mode voltage to the peak–to–peak change in V_{IO}. Measures the ability of an op amp to reject a signal present at both inputs simultaneously. May be given in dB or volts per volt.

Power Supply Rejection Ratio (PSR or PSRR) — The ratio of the change in V_{IO} to the change in power supply voltage. Measures the immunity of the amplifier to changes in power supply voltage.

Output Short Circuit Current (I_{SC}) — The maximum current an amplifier can deliver into a short circuit. Care must be exercised to ensure the maximum junction temperature of the device is not exceeded to prevent damage to the device.

Supply Current (I_D or I_{CC}) — The operating current required with no load and with the output at zero volts.

Slew Rate (SR) — The rate of change of the output voltage in response to a large amplitude pulse applied to the input. The slew rate determines the power bandwidth of the device.

Gain Bandwidth Product (GBW) — The product of the closed–loop gain times the frequency response at a given frequency. For an op amp with a single pole roll–off, the gain bandwidth product is equal to the unity gain frequency.

Phase Margin (ϕ_M) — 180° minus the phase shift at the unity gain frequency of the device. The phase margin must be positive for unconditionally stable operation. Phase margin (and stability) are affected by the external circuit, particularly the capacitive loading on the output and the differential source resistance on the input.

Channel Separation (CS) — A measurement of the immunity of one op amp to a signal present on another amplifier in a dual or quad.

Power Bandwidth (BWP) — The frequency at which the output starts to clip or distort at maximum peak–to–peak input voltage.

3

Power Supply Circuits

In Brief . . .

In most electronic systems, some form of voltage regulation is required. In the past, the task of voltage regulator design was tediously accomplished with discrete devices, and the results were quite often complex and costly. Today, with bipolar monolithic regulators, this task has been significantly simplified. The designer now has a wide choice of fixed, low V_{Diff} and adjustable type voltage regulators. These devices incorporate many built–in protection features, making them virtually immune to the catastrophic failures encountered in older discrete designs.

The switching power supply continues to increase in popularity and is one of the fastest growing markets in the world of power conversion. They offer the designer several important advantages over linear series–pass regulators. These advantages include significant advancements in the areas of size and weight reduction, improved efficiency, and the ability to perform voltage step–up, step–down, and voltage–inverting functions. Motorola offers a diverse portfolio of full featured switching regulator control circuits which meet the needs of today's modern compact electronic equipment.

Power supplies, MPU/MCU–based systems, industrial controls, computer systems and many other product applications are requiring power supervisory functions which monitor voltages to ensure proper system operation. Motorola offers a wide range of power supervisory circuits that fulfill these needs in a cost effective and efficient manner. MOSFET drivers are also provided to enhance the drive capabilities of first generation switching regulators or systems designed with CMOS/TTL logic devices. These drivers can also be used in dc–to–dc converters, motor controllers or virtually any other application requiring high speed operation of power MOSFETs.

Linear Voltage Regulators

Fixed Output

These low cost monolithic circuits provide positive and/or negative regulation at currents from 100 mA to 3.0 A. They are ideal for on–card regulation employing current limiting and thermal shutdown. Low V_{Diff} devices are offered for battery powered systems.

Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

3

Table 1. Linear Voltage Regulators

Device	V_{out}	25°C Tol. ±%	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out})/°C	Suffix/ Package
Fixed Voltage, 3–Terminal Regulators, 0.1 Amperes								
LM2931*/A–5.0*	5.0	5.0/3.8	40	0.16	0.6	1.0	0.2	D/751, D2T/936, DT, DT–1, T/221A, Z
LP2950C*/AC*	3.0	0.5	30	0.38	0.2/0.1	0.2/0.1	0.04	DT–3.0, Z–3.0
	3.3							DT–3.3, Z–3.3
	5.0							DT–5.0, Z–5.0
MC78LXXC/AC/AB*	5.0, 8.0, 9.0	8.0/4.0	30	1.7	4.0/3.0	1.2	0.2	D/751, P/29
MC78LXXC/AC/AB*	12, 15, 18	8.0/4.0	35	1.7	2.0	1.0	0.2	D/751, P/29
MC78L24C/AC/AB*	24	8.0/4.0	40	1.7	2.0	1.0	0.2	D/751, P/29
MC79L05C/AC/AB*	–5.0	8.0/4.0	30	1.7	4.0/3.0	1.2	0.2	D/751, P/29
MC79LXXC/AC/AB*	–(12, 15, 18)	8.0/4.0	35	1.7	2.0	1.0	0.2	D/751, P/29
MC79L24C/AC/AB*	–24	8.0/4.0	40	1.7	2.0	1.0	0.2	D/751, P/29
MC33160**	5.0	5.0	40	2.0	0.8	1.0	–	P/626
Fixed Voltage, 3–Terminal Regulators, 0.5 Amperes								
MC78MXXB*/C	5.0, 6.0, 8.0, 12	4.0	35	2.0	1.0	2.0	±0.04	DT, DT–1, T/221A
MC78MXXB*/C	15, 18	4.0	35	2.0	1.0	2.0	±0.04	DT, DT–1, T/221A
MC78MXXB*/C	20, 24	4.0	40	2.0	0.25	2.0	±0.04	DT, DT–1, T/221A
MC79MXXB*/C	–(5.0, 8.0, 12, 15)	4.0	35	1.1	1.0	2.0	–0.07 to ±0.04	DT, DT–1, T/221A
MC33267*	5.05	2.0	40	0.58	1.0	1.0	–	D2T/936A, T/314D, TV
Fixed Voltage, 3–Terminal Medium Dropout Regulators, 0.8 Amperes								
MC33269–XX*	3.3, 5.0, 12	1.0	20	1.0	0.3	1.0	–	D/751, DT, T/221A
MC34268	2.85	1.0	15	0.95	0.3	1.0	–	D/751, DT

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C
** T_A = –40° to +85°C

Table 1. Linear Voltage Regulators (continued)

Device	V_{out}	25°C Tol. ±%	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out}) / °C	Suffix/ Package
Fixed Voltage, 3–Terminal Regulators, 1.0 Amperes								
MC78XXB*/C/AC	5.0, 6.0, 8.0, 12, 18	4.0/2.0	35	2.0	2.0/1.0	2.0	–0.06 to –0.22	D2T/936, T/221A
MC7824B*/C/AC	24	4.0/2.0	40	2.0	2.0/1.0	2.0/0.4	0.125	D2T/936, T/221A
MC79XXC/AC	–(5.0, 5.2, 6.0)	4.0/2.0	35	2.0	2.0/1.0	2.0	–0.2	D2T/936, T/221A
MC79XXC/AC	–(8.0, 12, 15, 18)	4.0/2.0	35	2.0	2.0/1.0	2.0/1.25	–0.12 to –0.06	D2T/936, T/221A
MC7924C	–24	4.0	40	2.0	1.0	2.0	–0.04	D2T/936, T/221A
LM340/A–XX	5.0, 6.0, 12, 15, 18	4.0/2.0	35	1.7	1.0/0.2	1.0/0.5	±0.12	T/221A
LM340–24	24	4.0	40	1.7	1.0	1.0	±0.12	T/221S
TL780–XXC	5.0, 12, 15	1.0	35	2.0	0.10	0.5	0.012	KC
Fixed Voltage, 3–Terminal Regulators, 3.0 Amperes								
MC78TXXC/AC	5.0, 8.0, 12	4.0/2.0	35	2.5	0.5	0.6	0.04	T/221A
MC78T15C/AC	15	4.0/2.0	40	2.5	0.5	0.6	0.04	T/221A
LM323/A	5.0	4.0/2.0	20	2.3	0.5/0.3	2.0/1.0	±0.2	T/221A

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C
** T_A = –40° to +85°C

Table 2. Fixed Voltage Medium and Low Dropout Regulators

Device	V_{out}	25°C Tol. ±%	I_O (mA) Max	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out}) / °C	Suffix/ Package
Fixed Voltage, Medium Dropout Regulators									
MC33267*	5.05	2.0	500	40	0.58	1.0	1.0	–	D2T/936A, T/314D, TV
MC34268	2.85	1.0	800	15	0.95	0.3	1.0		D/751, DT
MC33269–XX*	3.3, 5.0, 12			20	1.0				D/751, DT, T/221A
Fixed Voltage, Low Dropout Regulators									
LM2931*/A*	5.0	5.0/3.8	100	37	0.16	1.12	1.0	±2.5	D/751, D2T/936A, DT, DT–1, T/221A, Z
LP2950C*/AC*	3.0	1.0/0.5	100	30	0.38	0.2/0.1	0.2/0.1	0.2	DT–3.0, Z–3.0
	3.3								DT–3.3, Z–3.3
	5.0								DT–5.0, Z–5.0

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C

Table 2. Fixed Voltage Medium and Low Dropout Regulators (continued)

Device	V_{out}	25°C Tol. ±%	I_O (mA) Max	V_{in} Max	$V_{in}-V_{out}$ Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out}) / °C	Suffix/ Package
Fixed Voltage, Low Dropout Regulators									
LP2951C*/AC*	3.0	1.0/0.5	100	28.75	0.38	0.04/0.02	0.04/0.02	±1.0	D–3.0/751, DM–3.0/ 846A, N–3.0/626
	3.3								D–3.3/751, DM–3.3/ 846A, N–3.3/626
	5.0								D/751, DM/846A, N/626
LM2935*	5.0/5.0	5.0/5.0	500/10	60	0.45/0.55	1.0	1.0	–	D2T/936A, T/314D, TH, TV

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C

Adjustable Output

Motorola offers a broad line of adjustable output voltage regulators with a variety of output current capabilities. Adjustable voltage regulators provide users the capability of stocking a single integrated circuit offering a wide range of output voltages for industrial and communications applications. The three–terminal devices require only two external resistors to set the output voltage.

Table 3. Adjustable Output Regulators

Device	V_{out}	I_O (mA) Max	V_{in} Max	$V_{in}-V_{out}$ Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out}) / °C	Suffix/ Package
Adjustable Regulators								
LM317L/B*	2.0–37	100	40	1.9	0.07	1.5	±0.35	D/751, Z
LM2931C*	3.0–24	100	37	0.16	1.12	1.0	±2.5	D/751, D2T/936A, T/314D, TH, TV
LP2951C*/AC*	1.25–29	100	28.75	0.38	0.04/0.02	0.04/0.02	±1.0	D–3.0/751, DM–3.0/ 846A, N–3.0/626
								D–3.3/751, DM–3.3/ 846A, N–3.3/626
								D/751, DM/846A, N/626
MC1723C#	2.0–37	150	38	2.5	0.5	0.2	±0.033	D/751, P/646

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C
\# T_A = 0° to +70°C

Table 3. Adjustable Output Regulators (continued)

Device	V_{out}	I_O (mA) Max	V_{in} Max	$V_{in}-V_{out}$ Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out}) / °C	Suffix/ Package
Adjustable Regulators								
LM317M/B*	1.2–37	500	40	2.1	0.04	0.5	±0.35	DT, DT–1, T/221A
LM337M/B*	–(1.2–37)	500	40	1.9	0.07	1.5	±0.3	T/221A
MC33269*	1.25–19	800	18.75	1.0	0.3	0.5	±0.4	D/751, DT, T/221A
LM317/B*	1.2–37	1500	40	2.25	0.07	1.5	±0.35	D2T/936, T/221A
LM337/B*	–(1.2–37)	1500	40	2.3	0.07	1.5	±0.3	D2T/936, T/221A
LM350/B*	1.2–33	3000	35	2.7	0.07	1.5	±0.5	T/221A

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C
\# T_A = 0° to +70°C

Micropower Voltage Regulators for Portable Applications

80 mA Micropower Voltage Regulator

MC78LC00H, N

T_A = –30° to +80°C, Case 1213, 1212

The MC78LC00 series voltage regulators are specifically designed for use as a power source for video instruments, handheld communication equipment, and battery powered equipment.

The MC78LC00 series features an ultra–low quiescent of 1.1 µA and a high accuracy output voltage. Each device contains a voltage reference, an error amplifier, a driver transistor and resistors for setting the output voltage. These devices are available in either SOT–89, 3 pin, or SOT–23, 5 pin, surface mount packages.

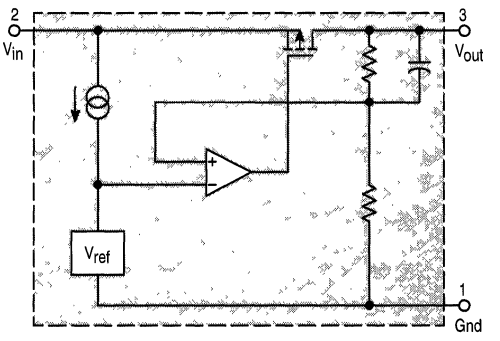
MC78LC00 Series Features:

- Low Quiescent Current of 1.1 µA Typical
- Low Dropout Voltage (30 mV Typical)
- Excellent Line Regulation (0.1%)
- High Accuracy Output Voltage (±2.5%)
- Wide Output Voltage Range (2.0 V to 6.0 V)
- Output Current for Low Power (80 mA Typical)
- Two Surface Mount Packages (SOT–89, 3 Pin, or SOT–23, 5 Pin)

ORDERING INFORMATION

Device	Output Voltage	Operating Temperature Range	Package
MC78LC30HT1	3.0	T_A = –30° to +80°C	SOT–89
MC78LC33HT1	3.3		
MC78LC40HT1	4.0		
MC78LC50HT1	5.0		
MC78LC30NTR	3.0		SOT–23
MC78LC33NTR	3.3		
MC78LC40NTR	4.0		
MC78LC50NTR	5.0		

Other voltages from 2.0 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.



3

120 mA Micropower Voltage Regulator

MC78FC00H

T_A = –30° to +80°C, Case 1213

The MC78FC00 series voltage regulators are specifically designed for use as a power source for video instruments, handheld communication equipment, and battery powered equipment.

The MC78FC00 series voltage regulator ICs feature a high accuracy output voltage and ultra–low quiescent current. Each device contains a voltage reference unit, an error amplifier, a driver transistor, and resistors for setting output voltage, and a current limit circuit. These devices are available in SOT–89 surface mount packages, and allow construction of an efficient, constant voltage power supply circuit.

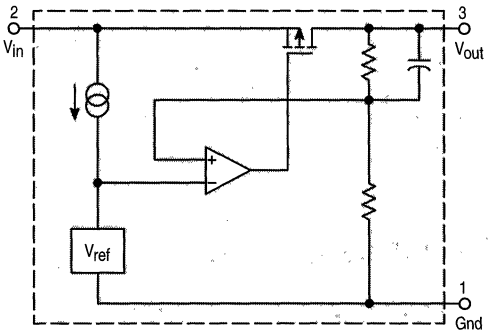
MC78FC00 Series Features:

- Ultra–Low Quiescent Current of 1.1 μA Typical
- Ultra–Low Dropout Voltage (0.5 V Typical)
- Large Output Current (120 mA Typical)
- Excellent Line Regulation (0.1%)
- Wide Operating Voltage Range (2.0 V to 10 V)
- High Accuracy Output Voltage (±2.5%)
- Wide Output Voltage Range (2.0 V to 6.0 V)
- Surface Mount Package (SOT–89)

ORDERING INFORMATION

Device	Output Voltage	Operating Temperature Range	Package
MC78FC30HT1	3.0	T_A = –30° to +80°C	SOT–89
MC78FC33HT1	3.3		
MC78FC40HT1	4.0		
MC78FC50HT1	5.0		

Other voltages from 2.0 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.



Micropower Voltage Regulator for External Power Transistor

MC78BC00N

T_A = –30° to +80°C, Case 1212

The MC78BC00 voltage regulators are specifically designed to be used with an external power transistor to deliver high current with high voltage accuracy and low quiescent current.

The MC78BC00 series are devices suitable for constructing regulators with ultra–low dropout voltage and output current in the range of several tens of mA to hundreds of mA. These devices have a chip enable function, which minimizes the standby mode current drain. Each of these devices contains a voltage reference unit, an error amplifier, a driver transistor and resistors. These devices are available in the SOT–23, 5 pin surface mount packages.

These devices are ideally suited for battery powered equipment, and power sources for hand–held audio instruments, communication equipment and domestic appliances.

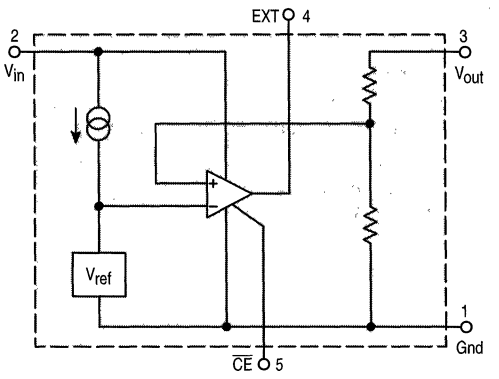
MC78BC00 Series Features:

- Ultra–Low Supply Current (50 μA)
- Standby Mode (0.2 μA)
- Ultra–Low Dropout Voltage (0.1 V with External Transistor and I_O = 100 mA)
- Excellent Line Regulation (Typically 0.1%/V)
- High Accuracy Output Voltage (±2.5%)

ORDERING INFORMATION

Device	Output Voltage	Operating Temperature Range	Package
MC78BC30NTR	3.0	T_A = –30° to +80°C	SOT–23
MC78BC33NTR	3.3		
MC78BC40NTR	4.0		
MC78BC50NTR	5.0		

Other voltages from 2.0 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.



Micropower Voltage Regulators with On/Off Control

MC33264D, DM

T_A = –40° to +85°C, Case 751, 846A

The MC33264 series are micropower low dropout voltage regulators available in SO–8 and Micro–8 surface mount packages and a wide range of output voltages. These devices feature a very low quiescent current (100 μA in the ON mode; 0.1 μA in the OFF mode), and are capable of supplying output currents up to 100 mA. Internal current and thermal limiting protection is provided.

Additionally, the MC33264 has either active HIGH or active LOW control (Pins 2 and 3) that allows a logic level signal to turn–off or turn–on the regulator output.

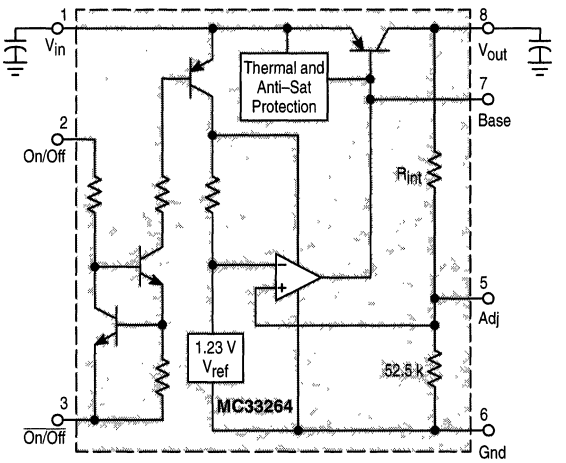
Due to the low input–to–output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC33264 Features:

- Low Quiescent Current (0.3 μA in OFF Mode; 95 μA in ON Mode)
- Low Input–to–Output Voltage Differential of 47 mV at 10 mA, and 131 mV at 50 mA
- Multiple Output Voltages Available
- Extremely Tight Line and Load Regulation
- Stable with Output Capacitance of Only 0.33 μF for 5.0 V, 6.0 V and 4.75 V Output Voltages 0.22 μF for 2.8 V, 3.0 V and 3.3 V Output Voltages
- Internal Current and Thermal Limiting
- Logic Level ON/OFF Control
- Functionally Equivalent to TK115XXMC and LP2980

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33264D–2.8 MC33264D–3.0 MC33264D–3.3 MC33264D–3.8 MC33264D–4.0 MC33264D–4.75 MC33264D–5.0	T_A = –40° to +85°C	SO–8
MC33264DM–2.8 MC33264DM–3.0 MC33264DM–3.3 MC33264DM–3.8 MC33264DM–4.0 MC33264DM–4.75 MC33264DM–5.0		Micro–8



Special Regulators

Voltage Regulator/Supervisory

Table 4. Voltage Regulator/Supervisory

Device	V_{out} (V)		I_O (mA)	V_{in} (V)		Reg_{line} (mV)	Reg_{load} (mV)	T_A (°C)	Suffix/ Package
	Min	Max	Max	Min	Max	Max	Max		
MC33128*	2.9	3.1	35	3.2	7.0	n/a	30	–30 to +60	D/751B
	2.9	3.1	60				40		
	2.9	3.1	20				25		
	–2.65	–2.35	1.0				20		
MC34160	4.75	5.25	100	7.0	40	40	50	0 to +70	P/648C, DW/751G
MC33160								–40 to +85	
MC33267	4.9	5.2	500	6.0	26	50	50	–40 to +105	T/314D, TH, TV
MC33169*	4.7	6.4	–	2.7	9.5	–	–	–40 to +85	DTB/948G
	6.4	7.0							
	–2.35	–2.65							

* These ICs are intended for powering cellular phone GaAs power amplifiers and can be used for other portable applications as well.

Microprocessor Voltage Regulator and Supervisory Circuit

MC34160P, DW

T_A = 0° to +70°C, Case 648C, 751G

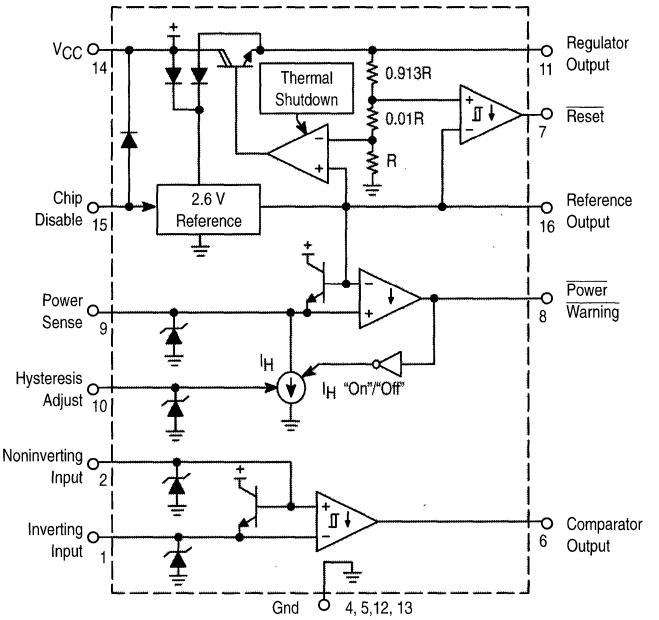
MC33160P, DW

T_A = –40° to +85°C, Case 648C, 751G

The MC34160 series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V, 100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

These devices are contained in a 16 pin dual–in–line heat tab plastic package for improved thermal conduction.



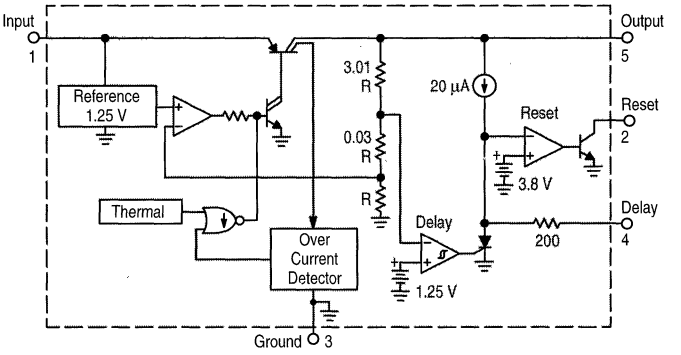
Low Dropout Regulator

MC33267T, TV

T_J = –40° to +105°C, Case 314D, 314B

The MC33267 is a positive fixed 5.0 V regulator that is specifically designed to maintain proper voltage regulation with an extremely low input–to–output voltage differential. This device is capable of supplying output currents in excess of 500 mA and contains internal current limiting and thermal shutdown protection. Also featured is an on–chip power–up reset circuit that is ideally suited for use in microprocessor based systems. Whenever the regulator output voltage is below nominal, the reset output is held low. A programmable time delay is initiated after the regulator has reached its nominal level and upon timeout, the reset output is released.

Due to the low dropout voltage specifications, the MC33267 is ideally suited for use in battery powered industrial and consumer equipment where an extension of useful battery life is desirable. This device is contained in an economical five lead TO–220 type package.



3

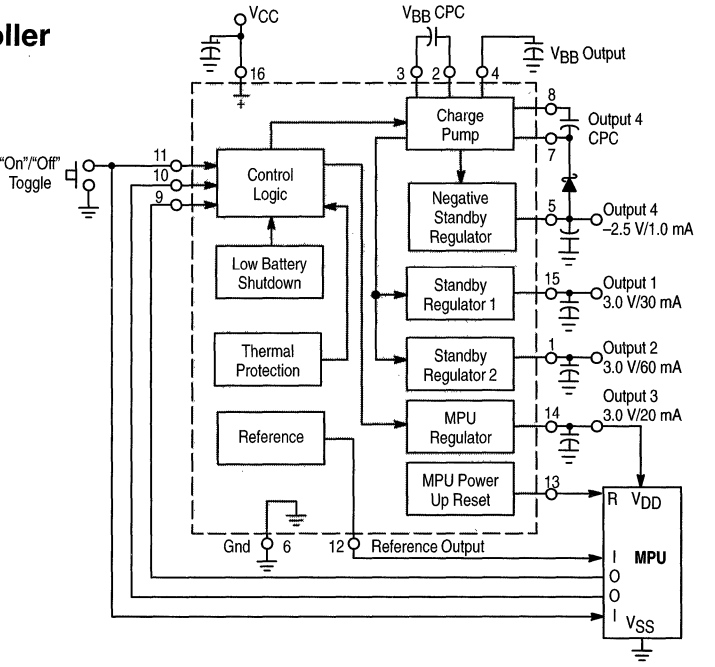
Power Management Controller

MC33128D

T_A = –30° to +60°C, Case 751B

The MC33128 is a power management controller specifically designed for use in battery powered cellular telephone and pager applications. This device contains all of the active functions required to interface the user to the system electronics via a microprocessor. This integrated circuit consists of a low dropout voltage regulator with power–up reset for MPU power, two low dropout voltage regulators for independant powering of analog and digital circuitry, and a negative charge pump voltage regulator for full depletion of gallium arsenide MESFETs.

Also included are protective system shutdown features consisting of a battery latch that is activated upon battery insertion, low battery voltage shutdown, and a thermal over temperature detector. This device is available in a 16–pin narrow body surface mount plastic package.



GaAs Power Amplifier Support IC

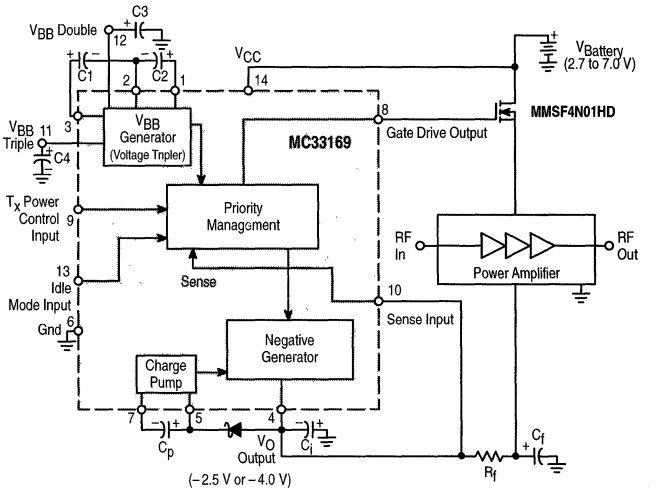
MC33169DTB

T_A = –40° to +85°C, Case 948G

The MC33169 is a support IC for GaAs Power Amplifier Enhanced FETs used in hand portable telephones such as GSM, PCN and DECT. This device provides negative voltages for full depletion of Enhanced MESFETs as well as a priority management system of drain switching, ensuring that the negative voltage is always present before turning "on" the Power Amplifier. Additional features include an idle mode input and a direct drive of the N–Channel drain switch transistor.

This product is available in two versions, –2.5 and –4.0 V. The –4.0 V version is intended for supplying RF modules for GSM and DCS1800 applications, whereas the –2.5 V version is dedicated for DECT and PHS systems.

- Negative Regulated Output for Full Depletion of GaAs MESFETs
- Drain Switch Priority Management Circuit
- CMOS Compatible Inputs
- Idle Mode Input (Standby Mode) for Very Low Current Consumption
- Output Signal Directly Drives N–Channel FET
- Low Startup and Operating Current



SCSI Regulator

Table 5. SCSI Regulator

Device	V_{out} (V)		I_{sink} (mA)	V_{in} (V)		Reg_{line} (%)	Reg_{load} (%)	T_J (°C)	Suffix/ Package
	Min	Max		Min	Max				
MC34268	2.81	2.89	800	3.9	20	0.3	0.5	150	D/751, DT

3

SCSI–2 Active Terminator Regulator

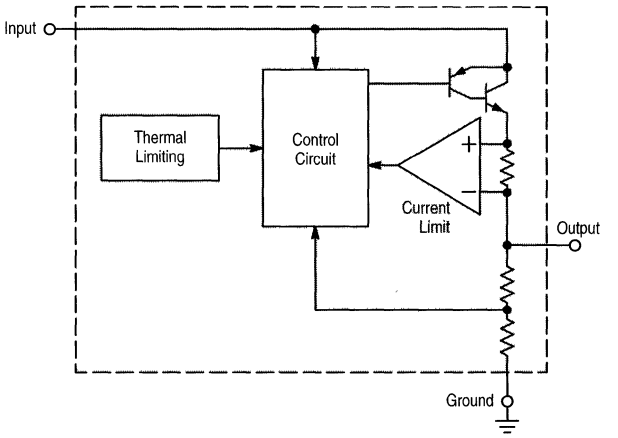
MC34268D, DT

T_J = 0° to +125°C, Case 751, 369A

The MC34268 is a medium current, low dropout positive voltage regulator specifically designed for use in SCSI–2 active termination circuits. This device offers the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum. The regulator consists of a 1.0 V dropout composite PNP/NPN pass transistor, current limiting, and thermal limiting. These devices are packaged in the 8–pin SOP–8 and 3–pin DPAK surface mount power packages.

Applications include active SCSI–2 terminators and post regulation of switching power supplies.

- 2.85 V Output Voltage for SCSI–2 Active Termination
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to 1.4% Tolerance
- No Minimum Load Required
- Space Saving DPAK and SOP–8 Surface Mount Power Packages



Switching Regulator Control Circuits

These devices contain the primary building blocks which are required to implement a variety of switching power supplies. The product offerings fall into three major categories consisting of single–ended and double–ended controllers, plus single–ended ICs with on–chip power switch transistors. These circuits operate in voltage, current or resonant modes and are designed to drive many of the standard switching topologies. The single–ended configurations include buck, boost, flyback and forward converters. The double–ended devices control push–pull, half bridge and full bridge configurations.

3

Table 6. Single–Ended Controllers

These single–ended voltage and current mode controllers are designed for use in buck, boost, flyback, and forward converters. They are cost effective in applications that range from 0.1 to 200 W power output.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
500 (Uncommitted Drive Output)	7.0 to 40	Voltage	5.0 ± 1.5%	200	MC34060A	0 to +70	D/751A
							P/646
					MC33060A	–40 to +85	D/751A
							P/646
1000 (Totem Pole MOSFET Drive Output)	4.2 to 12	Current	1.25 ± 2.0%	300	MC34129	0 to +70	D/751A
							P/646
					MC33129	–40 to +85	D/751A
							P/646
	11.5 to 30		5.0 ± 2.0%	500	UC3842A	0 to +70	D/751A
							N/626
	11 to 30		5.0 ± 1.0%		UC2842A	–25 to +85	D/751A
							N/626
	8.2 to 30		5.0 ± 2.0%		UC3843A	0 to +70	D/751A
							N/626
			5.0 ± 1.0%		UC2843A	–25 to +85	D/751A
							N/626
	11.5 to 30		5.0 ± 2.0%	500 (50% Duty Cycle Limit)	UC3844	0 to +70	D/751A
							N/626
	11 to 30		5.0 ± 1.0%		UC2844	–25 to +85	D/751A
							N/626
	8.2 to 30		5.0 ± 2.0%		UC3845	0 to +70	D/751A
							N/626
			5.0 ± 1.0%		UC2845	–25 to +85	D/751A
							N/626
	11.5 to 30		5.0 ± 2.0%	500 (Improved Oscillator Specifications with Frequency Guaranteed at 250 kHz)	UC3842B	0 to +70	D/751A
							D1/751
							N/626
					UC3842BV	–40 to +105	D/751A
							D1/751
							N/626

Table 6. Single–Ended Controllers (continued)

These single–ended voltage and current mode controllers are designed for use in buck, boost, flyback, and forward converters. They are cost effective in applications that range from 0.1 to 200 W power output.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
1000 (Totem Pole MOSFET Drive Output)	11 to 30	Current	5.0 ± 1.0%	500 (Improved Oscillator Specifications with Frequency Guaranteed at 250 kHz)	UC2842B	–25 to +85	D/751A
							D1/751
							N/626
	8.2 to 30		5.0 ± 2.0%		UC3843B	0 to +70	D/751A
							D1/751
							N/626
					UC3843BV	–40 to +105	D/751A
							D1/751
							N/626
			5.0 ± 1.0%		UC2843B	–25 to +85	D/751A
							D1/751
							N/626
	11.5 to 30		5.0 ± 2.0%	500 (50% Duty Cycle Limit)	UC3844B	0 to +70	D/751A
							D1/751
							N/626
					UC3844BV	–40 to +105	D/751A
							D1/751
							N/626
	11 to 30		5.0 ± 1.0%		UC2844B	–25 to +85	D/751A
							D1/751
							N/626
	8.2 to 30		5.0 ± 2.0%		UC3845B	0 to +70	D/751A
							D1/751
							N/626
					UC3845BV	–40 to +105	D/751A
							D1/751
							N/626
			5.0 ± 1.0%		UC2845B	–25 to +85	D/751A
							D1/751
							N/626
1000 Source 1500 Sink (Split Totem Pole Bipolar Drive Output)	11 to 18		5.0 ± 6.0%		MC44602		P2/648C
2000 (Totem Pole MOSFET Drive Output)	9.2 to 30	Current or Voltage	5.1 ± 1.0%	1000	MC34023	0 to +70	DW/751G
							FN/775
							P/648
					MC33023	–40 to +105	DW/751G
							FN/775
							P/648

Table 7. Single–Ended Controllers with On–Chip Power Switch

These monolithic power switching regulators contain all the active functions required to implement standard dc–to–dc converter configurations with a minimum number of external components.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
1500 (Uncommitted Power Switch)	2.5 to 40	Voltage	1.25 ± 5.2%(1)	100	μA78S40	0 to +70	PC/648
						–40 to +85	PV/648
			1.25 ± 2.0%		MC34063A	0 to +70	D/751
							P1/626
					MC33063A	–40 to +85	D/751
							P1/626
						–40 to +125	D/751
1500 (Uncommitted Power Switch)	3.0 to 65	Voltage	1.25 ± 2.0% and 5.05 ± 3.0%	100	MC34165	0 to +70	P/648C, DW/751G
					MC33165	–40 to +85	
3400 (Uncommitted Power Switch)	2.5 to 40				MC34163	0 to +70	
					MC33163	–40 to +85	
3400(2) (Dedicated Emitter Power Switch)	7.5 to 40		5.05 ± 2.0%	72 ± 12% Internally Fixed	MC34166	0 to +70	D2T/936A, TH, TV, T/314D
					MC33166	–40 to +85	
5500(3) (Dedicated Emitter Power Switch)					MC34167	0 to +70	
					MC33167	–40 to +85	

(1) Tolerance applies over the specified operating temperature range.
(2) Guaranteed minimum, typically 4300 mA.
(3) Guaranteed minimum, typically 6500 mA.

Table 8. Easy Switcher™ Single–Ended Controllers with On–Chip Power Switch

The Easy Switcher™ series is ideally suited for easy, convenient design of a step–down switching regulator (buck converter), with a minimum number of external components.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Oscillator Frequency (kHz)	Output Voltage (V)	Device	T_J (°C)	Suffix/ Package
1000	4.75 to 40	Voltage	52 Fixed Internal	3.3	LM2575T–3.3	–40 to +125	T/314D
	8.0 to 40			5.0	LM2575T–5		
	15 to 40			12	LM2575T–12		
	18 to 40			15	LM2575T–15		
	8.0 to 40			1.23 to 37	LM2575T–Adj		
	4.75 to 40			3.3	LM2575TV–3.3		TV/314B
	8.0 to 40			5.0	LM2575TV–5		
	15 to 40			12	LM2575TV–12		
	18 to 40			15	LM2575TV–15		
	8.0 to 40			1.23 to 37	LM2575TV–Adj		
	4.75 to 40			3.3	LM2575D2T–3.3		D2T/936A
	8.0 to 40			5.0	LM2575D2T–5		
	15 to 40			12	LM2575D2T–12		
	18 to 40			15	LM2575D2T–15		
	8.0 to 40			1.23 to 37	LM2575D2T–Adj		

Table 9. Very High Voltage Single–Ended Controller with On–Chip Power Switch

This monolithic high voltage switching regulator is specifically designed to operate from a rectified ac line voltage source. Included are an on–chip high voltage power switch, active off–line startup circuitry and a full featured PWM controller with fault protection.

Power Switch Maximum Rating		Startup Input Max (V)	Operating Mode	Feedback Threshold (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_J (°C)	Suffix/ Package
V_{DS} (V)	I_{DS} (mA)							
500	2000	250	Voltage	2.6 ± 3.1%	1000	MC33362	–25 to +125	DW/751N, P/648E
700	1000	450				MC33363		
700	1000	450				MC33363A		

Table 10. Double–Ended Controllers

These double–ended voltage, current and resonant mode controllers are designed for use in push–pull, half–bridge, and full–bridge converters. They are cost effective in applications that range from 100 to 2000 watts power output.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
500 (Uncommitted Drive Outputs)	7.0 to 40	Voltage	5.0 ± 5.0%(1)	200	TL494	0 to +70	CN/648
						–25 to +85	IN/648
			5.0 ± 1.5%	300	TL594	0 to +70	CN/648
						–25 to +85	IN/648
± 500 (Totem Pole MOSFET Drive Outputs)	8.0 to 40		5.1 ± 2.0%	400	SG3525A	0 to +70	N/648
					SG3527A		N/648
± 200 (Totem Pole MOSFET Drive Outputs)			5.0 ± 2.0%		SG3526	0 to +125(2)	N/707
±1500 (Totem Pole MOSFET Drive Outputs)	9.6 to 20	Resonant (Zero Current)	5.1 ± 2.0%	1000	MC34066	0 to +70	DW/751G
							P/648
					MC33066	–40 to +85	DW/751G
							P/648
		Resonant (Zero Voltage)		2000	MC34067	0 to +70	DW/751G
							P/648
					MC33067	–40 to +85	DW/751G
							P/648
2000 (Totem Pole MOSFET Drive Outputs)	9.2 to 30	Current or Voltage	5.1 ± 1.0%	1000	MC34025	0 to +70	DW/751G
							FN/775
							P/648
					MC33025	–40 to +105	DW/751G
							FN/775
							P/648

(1) Tolerance applies over the specified operating temperature range.
(2) Junction Temperature Range.

CMOS Micropower DC–to–DC Converters

Variable Frequency Micropower DC–to–DC Converter

MC33463H

T_A = –30° to +80°C, Case 1213

The MC33463 series are micropower switching voltage regulators, specifically designed for handheld and laptop applications, to provide regulated output voltages using a minimum of external parts. A wide choice of output voltages are available. These devices feature a very low quiescent bias current of 4.0 μA typical.

The MC33463H–XXLT1 series features a highly accurate voltage reference, an oscillator, a variable frequency modulation (VFM) controller, a driver transistor (Lx), an error amplifier and feedback resistive divider.

The MC33463H–XXLT1 is identical to the MC33463H–XXKT1, except that a drive pin (EXT) for an external transistor is provided.

Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC33463 Series Features:

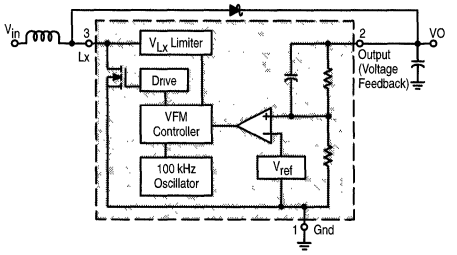
- Low Quiescent Bias Current of 4.0 μA
- High Output Voltage Accuracy of ±2.5%
- Low Startup Voltage of 0.9 V at 1.0 mA
- Surface Mount Package

ORDERING INFORMATION

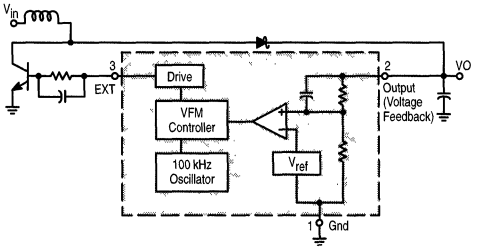
Device	Output Voltage	Type	Operating Temperature Range	Package (Tape/Reel)
MC33463H–30KT1	3.0	Int. Switch	T_A = –30° to +80°C	SOT–89 (Tape)
MC33463H–33KT1	3.3			
MC33463H–50KT1	5.0			
MC33463H–30LT1	3.0	Ext. Switch Drive		SOT–89 (Tape)
MC33463H–33LT1	3.3			
MC33463H–50LT1	5.0			

Other voltages from 2.5 V to 7.5 V, in 0.1 V increments are available upon request. Consult your local Motorola sales office for information.

MC33463H–XXKT1



MC33463H–XXLT1



Fixed Frequency PWM Micropower DC–to–DC Converter

MC33466H

T_A = –30° to +80°C, Case 1213

The MC33466 series are micropower switching voltage regulators, specifically designed for handheld and laptop applications, to provide regulated output voltages using a minimum of external parts. A wide choice of output voltages are available. These devices feature a very low quiescent bias current of 15 μA typical.

The MC33466H–XXJT1 series features a highly accurate voltage reference, an oscillator, a pulse width modulation (PWM) controller, a driver transistor (Lx), an error amplifier and feedback resistive divider.

The MC33466H–XXLT1 is identical to the MC33466H–XXJT1, except that a drive pin (EXT) for an external transistor is provided.

Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC33466 Series Features:

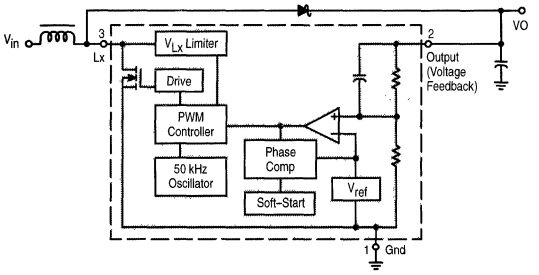
- Low Quiescent Bias Current of 15 μA
- High Output Voltage Accuracy of ±2.5%
- Low Startup Voltage of 0.9 V at 1.0 mA
- Soft–Start = 500 μs
- Surface Mount Package

ORDERING INFORMATION

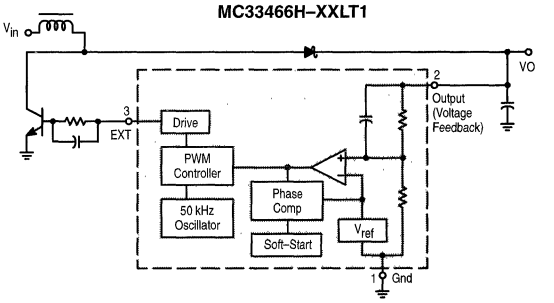
Device	Output Voltage	Type	Operating Temperature Range	Package (Tape/Reel)
MC33466H–30JT1	3.0	Int. Switch	T_A = –30° to +80°C	SOT–89 (Tape)
MC33466H–33JT1	3.3			
MC33466H–50JT1	5.0			
MC33466H–30LT1	3.0	Ext. Switch Drive		SOT–89 (Tape)
MC33466H–33LT1	3.3			
MC33466H–50LT1	5.0			

Other voltages from 2.5 V to 7.5 V, in 0.1 V increments are available upon request. Consult your local Motorola sales office for information.

MC33466H–XXJT1



MC33466H–XXLT1



3

Single–Ended GreenLine™ Controllers

Mixed Frequency Mode GreenLine™ PWM Controller:

Fixed Frequency, Variable Frequency, Standby Mode

MC44603P, DW

T_A = –25° to +85°C, Case 648, 751G

The MC44603 is an enhanced high performance controller that is specifically designed for off–line and dc–to–dc converter applications. This device has the unique ability of automatically changing operating modes if the converter output is overloaded, unloaded, or shorted, offering the designer additional protection for increased system reliability. The MC44603 has several distinguishing features when compared to conventional SMPS controllers. These features consist of a foldback facility for overload protection, a standby mode when the converter output is slightly loaded, a demagnetization detection for reduced switching stresses on transistor and diodes, and a high current totem pole output ideally suited for driving a power MOSFET. It can also be used for driving a bipolar transistor in low power converters (< 150 W). It is optimized to operate in discontinuous mode but can also operate in continuous mode. Its advanced design allows use in current mode or voltage mode control applications.

Current or Voltage Mode Controller

- Operation up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Oscillator with Precise Frequency Control

High Flexibility

- Externally Programmable Reference Current
- Secondary or Primary Sensing
- Synchronization Facility
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis

Safety/Protection Features

- Overvoltage Protection Against Open Current and Open Voltage Loop
- Protection Against Short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft–Start Feature
- Accurate Maximum Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference

GreenLine Controller: Low Power Consumption in Standby Mode

- Low Startup and Operating Current
- Fully Programmable Standby Mode
- Controlled Frequency Reduction in Standby Mode
- Low dV/dT for Low EMI Radiations

High Safety Standby Ladder Mode GreenLine™ PWM Controller

MC44604P

T_A = –25° to +85°C, Case 648

The MC44604 is an enhanced high performance controller that is specifically designed for off–line and dc–to–dc converter applications.

The MC44604 is a modification of the MC44603. The MC44604 offers enhanced safety and reliable power management in its protection features (foldback, overvoltage detection, soft–start, accurate demagnetization detection). Its high current totem pole output is also ideally suited for driving a power MOSFET but can also be used for driving a bipolar transistor in low power converters (< 150 W).

In addition, the MC44604 offers a new efficient way to reduce the standby operating power by means of a patented standby ladder mode operation of the converter significantly reducing the converter consumption in standby mode.

Current or Voltage Mode Controller

- Operation Up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Oscillator with Precise Frequency Control

High Flexibility

- Externally Programmable Reference Current
- Secondary or Primary Sensing
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis

Safety/Protection Features

- Overvoltage Protection Facility Against Open Loop
- Protection Against Short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft–Start Feature
- Accurate Maximum Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference

GreenLine™ Controller:

- Low Startup and Operating Current
- Patented Standby Ladder Mode for Low Standby Losses
- Low dV/dT for Low EMI

High Safety Latched Mode GreenLine™ PWM Controller for (Multi)Synchronized Applications

MC44605P

T_A = –25° to +85°C, Case 648

The MC44605 is a high performance current mode controller that is specifically designed for off–line converters. The MC44605 has several distinguishing features that make it particularly suitable for multisynchronized monitor applications.

The MC44605 synchronization arrangement enables operation from 16 kHz up to 130 kHz. This product was optimized to operate with universal ac mains voltage from 80 V to 280 V, and its high current totem pole output makes it ideally suited for driving a power MOSFET.

The MC44605 protections provide well controlled, safe power management. Safety enhancements detect four different fault conditions and provide protection through a disabling latch.

Current or Voltage Mode Controller

- Current Mode Operation Up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Oscillator with Precise Frequency Control
- Externally Programmable Reference Current
- Secondary or Primary Sensing (Availability of Error Amplifier Output)
- Synchronization Facility
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Output dV/dT for Low EMI
- Low Startup and Operating Current

Safety/Protection Features

- Soft–Start Feature
- Demagnetization (Zero Current Detection) Protection
- Overvoltage Protection Facility Against Open Loop
- EHT Overvoltage Protection (E.H.T.OVP): Protection Against Excessive Amplitude Synchronization Pulses
- Winding Short Circuit Detection (W.S.C.D.)
- Limitation of the Maximum Input Power (M.P.L.): Calculation of Input Power for Overload Protection
- Over Heating Detection (O.H.D.): to Prevent the Power Switch from Excessive Heating

Latched Disabling Mode

- When one of the following faults is detected: EHT overvoltage, Winding Short Circuit (WSCD), excessive input power (M.P.L.), power switch over heating (O.H.D.), a counter is activated
- If the counter is activated for a time that is long enough, the circuit gets definitively disabled. The latch can only be reset by removing and then re–applying power

Very High Voltage Switching Regulator

MC33362DW, P

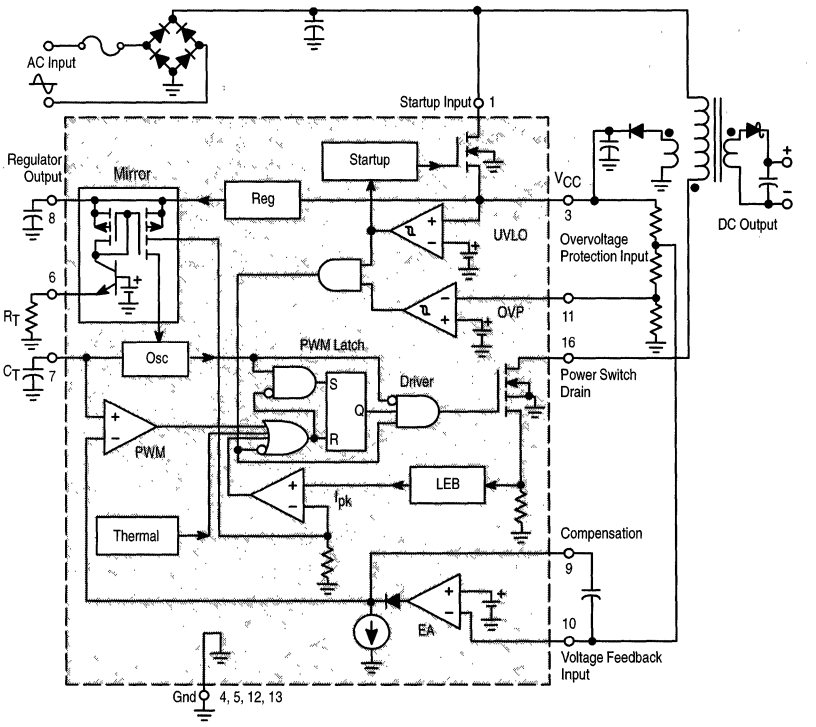
T_J = –25° to +125°C, Case 751N, 658E

3

The MC33362 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 120 VAC line source. This integrated circuit features an on–chip 500 V/2.0 A SenseFET power switch, 250 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16–lead dual–in–line and wide body surface mount packages.

- On–Chip 500 V, 2.0 A SenseFET Power Switch
- Rectified 120 VAC Line Source Operation
- On–Chip 250 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown

20 W Off–Line Converter



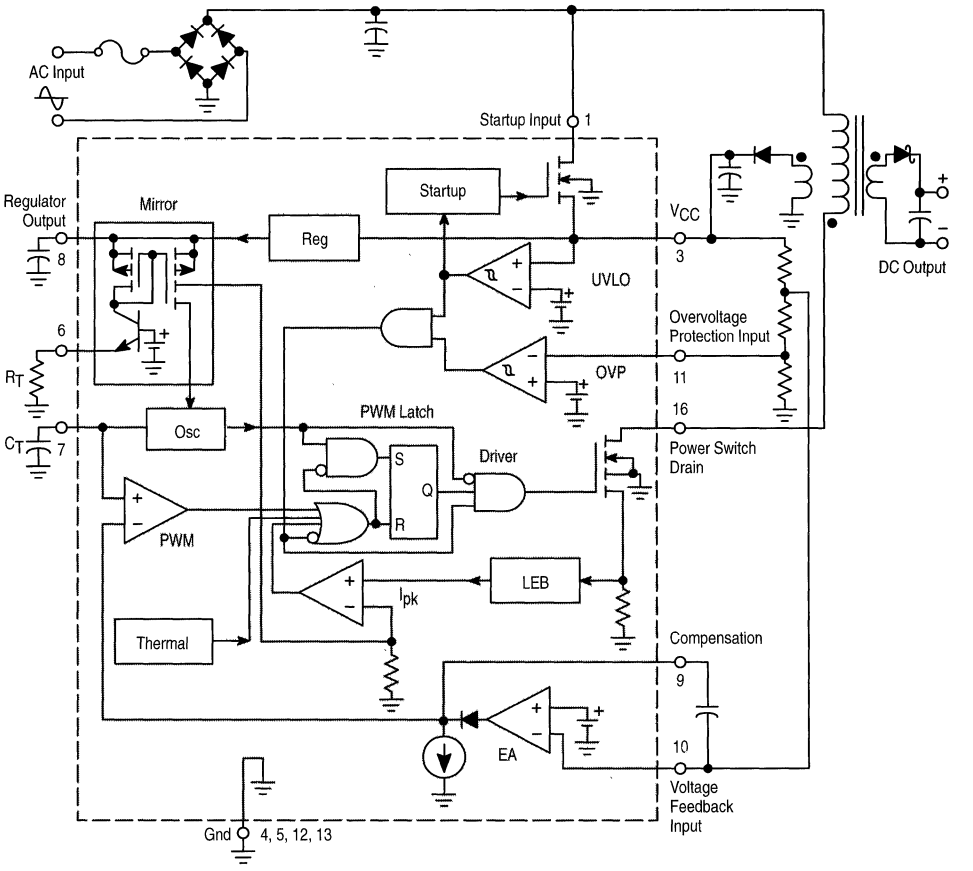
Very High Voltage Switching Regulator

MC33363DW, P, MC33363ADW, P

T_J = –25° to +125°C, Case 751N, 648E

The MC33363 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on–chip 700 V/1.0 A (1.5 A in MC33363A) SenseFET power switch, 450 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16–lead wide body surface mount package.

- On–Chip 700 V, 1.0 A SenseFET Power Switch
- On–Chip 700 V, 1.5 A SenseFET Power Switch in MC33363A
- Rectified 240 Vac Line Source Operation
- On–Chip 450 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown



Critical Conduction SMPS Controller

MC33364D, D1, D2

T_J = –25° to +125°C, Case 751, 751B

3

The MC33364 series are variable frequency SMPS controllers that operate in the critical conduction mode. They are optimized for low power, high density power supplies requiring minimum board area, reduced component count, and low power dissipation. Each narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

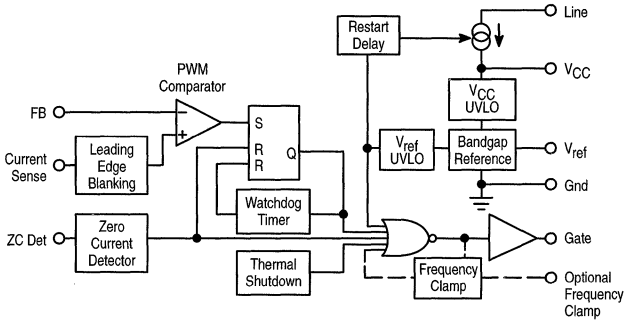
Each MC33364 features an on–board reference, UVLO function, a watchdog timer to initiate output switching, a zero current detector to ensure critical conduction operation, a current sensing comparator, leading edge blanking, and a CMOS driver. Protection features include the ability to shut down switching, and cycle–by–cycle current limiting.

The MC33364D1 is available in a surface mount SO–8 package. It has an internal 144 kHz frequency clamp. For loads which have a low power operating condition, the frequency clamp limits the maximum operating frequency, preventing excessive switching losses and EMI radiation.

The MC33364D2 is available in the SO–8 package without an internal frequency clamp.

The MC33364D is available in the SO–16 package. It has an internal 144 kHz frequency clamp which is pinned out, so that the designer can adjust the clamp frequency by connecting appropriate values of resistance and capacitance.

- Lossless Off–Line Startup
- Leading Edge Blanking for Noise Immunity
- Watchdog Timer to Initiate Switching
- Minimum Number of Support Components
- Shutdown Capability
- Over Temperature Protection
- Optional Frequency Clamp



Special Switching Regulator Controllers

These high performance dual channel controllers are optimized for off–line, ac–to–dc power supplies and dc–to–dc converters in the flyback topology. They also have undervoltage lockout voltages which are optimized for off–line and lower voltage dc–to–dc converters, respectively. Applications include desktop computers, peripherals, televisions, games, and various consumer appliances.

Table 11. Dual Channel Controllers

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
500	4.0	Voltage	1.25 ± 2.0%	700	MC34270	0 to +70	FB/873A
					MC34271		
±1000 (Totem Pole MOSFET Drive Outputs)	11 to 15.5	Current	5.0 ± 2.6%	500	MC34065	0 to +70	DW/751G
							P/648
					MC33065	–40 to +85	DW/751G
							P/648
	11 to 20				MC34065	0 to +70	DW–H/751G
							P–H/648
					MC33065	–40 to +85	DW–H/751G
							P–H/648
	8.4 to 20				MC34065	0 to +70	DW–L/751G
							P–L/648
					MC33065	–40 to +85	DW–L/751G
							P–L/648

Table 12. Universal Microprocessor Power Supply Controllers

A versatile power supply control circuit for microprocessor–based systems, this device is mainly intended for automotive applications and battery powered instruments. The circuit provides a power–on reset delay and a Watchdog feature for orderly microprocessor operation.

Regulated Outputs	Output Current (mA)	V_{CC} (V)		Reference (V)	Key Supervisory Features	Device	T_A (°C)	Package
		Min	Max					
E^2PROM Programmable Output: 24 V (Write Mode) 5.0 V (Read Mode)	150 peak	6.0	35	2.5 ± 3.2%	MPU Reset and Watchdog Circuit	TCF5600 TCA5600	–40 to +85	707

Table 13. Power Factor Controllers

I_O (mA) Max	Minimum Operating Voltage Range (V)	Maximum Startup Voltage (V)	Reference (V)	Features	Device	T_A (°C)	Suffix/ Package
± 500 (Totem Pole MOSFET Drive Outputs)	9.0 to 30	30	2.5 ± 1.4%	Undervoltage Lockout, Internal Startup Timer	MC34261	0 to +70	D/751
							P/626
					MC33261	–40 to +85	D/751
							P/626
				Overvoltage Comparator, Undervoltage Lockout, Internal Startup Timer	MC34262	0 to +85	D/751
							P/626
					MC33262	–40 to +105	D/751
							P/626
1500 (CMOS Totem Pole MOSFET Drive Outputs)	9.0 to 16	500	5.0 ± 1.5%	Off–Line High Voltage Startup Overvoltage Comparator, Undervoltage Lockout, Timer, Low Load Detect	MC33368	–25 to +125	D/751K

Power Factor Controllers

MC34262D, P

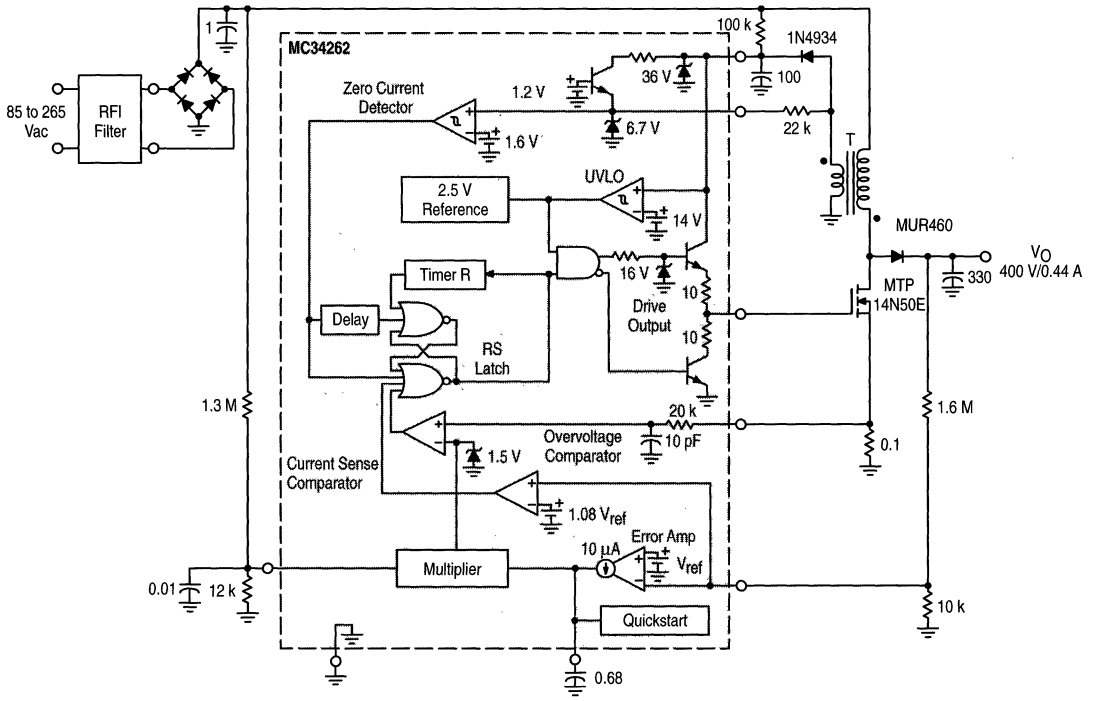
T_A = 0° to +85°C, Case 751, 626

MC33262D, P

T_A = –40° to +105°C, Case 751, 626

The MC34262, MC33262 series are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off–line power converter applications. These integrated circuits feature an internal startup timer for stand alone applications, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, transconductance error amplifier, quickstart circuit for enhanced startup, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of an overvoltage comparator to eliminate runaway output voltage due to load removal, input undervoltage lockout with hysteresis, cycle–by–cycle current limiting, multiplier output clamp that limits maximum peak switch current, an RS latch for single pulse metering, and a drive output high state clamp for MOSFET gate protection. These devices are available in dual–in–line and surface mount plastic packages.



Power Factor Controllers (continued)

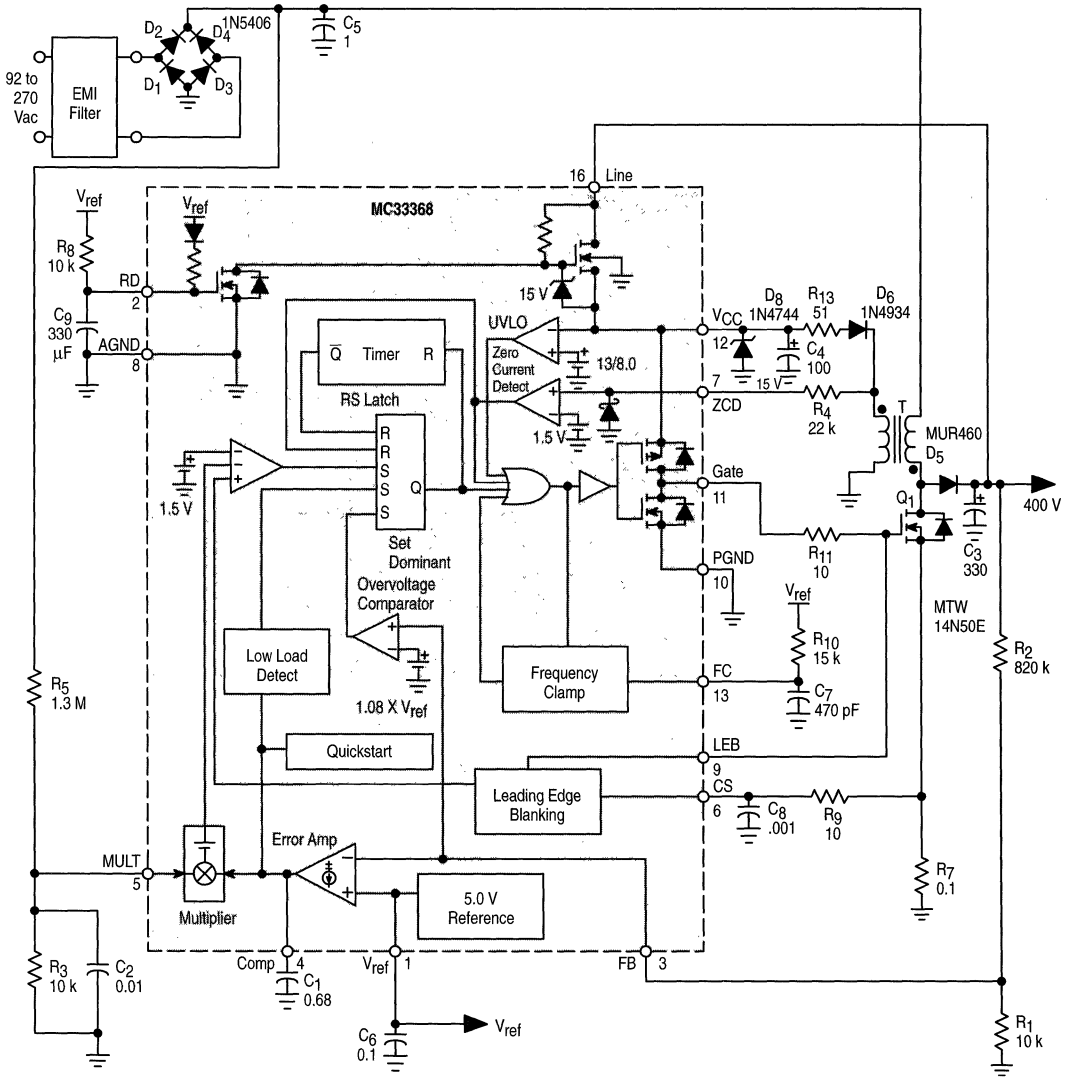
MC33368D

T_J = –25° to +125°C, Case 751K

The MC33368 is an active power factor controller that functions as a boost preconverter in off–line power supply applications. MC33368 is optimized for low power, high density power supplies requiring minimum board area, reduced component count, and low power dissipation. The narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

The MC33368 features a watchdog timer to initiate output switching, a one quadrant multiplier to force the line current to follow the instantaneous line voltage, a zero current detector to ensure critical conduction operation, a transconductance error amplifier, a current sensing comparator, a 5.0 V reference, an undervoltage lockout (UVLO) circuit which monitors the V_{CC} supply voltage, and a CMOS driver for driving MOSFETs. The MC33368 also includes a programmable output switching frequency clamp. Protection features include an output overvoltage comparator to minimize overshoot, a restart delay timer, and cycle–by–cycle current limiting.

- Lossless Off–Line Startup
- Output Overvoltage Comparator
- Leading Edge Blanking (LEB) for Noise Immunity
- Watchdog Timer to Initiate Switching
- Restart Delay Timer



Supervisory Circuits

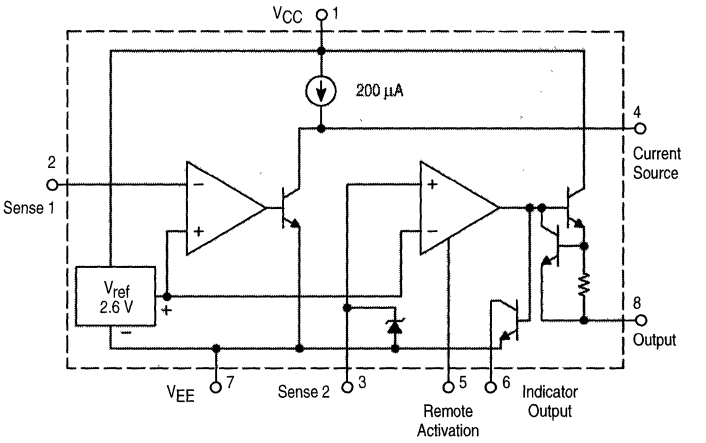
A variety of Power Supervisory Circuits are offered. Overvoltage sensing circuits which drive "Crowbar" SCRs are provided in several configurations from a low cost three–terminal version to 8–pin devices which provide pin–programmable trip voltages or additional features, such as an indicator output drive and remote activation capability. An over/undervoltage protection circuit is also offered.

Overvoltage Crowbar Sensing Circuit

MC3423P1, D

T_A = 0° to +70°C, Case 626, 751

This device can protect sensitive circuitry from power supply transients or regulator failure when used with an external "Crowbar" SCR. The device senses voltage and compares it to an internal 2.6 V reference. Overvoltage trip is adjustable by means of an external resistive voltage divider. A minimum duration before trip is programmable with an external capacitor. Other features include a 300 mA high current output for driving the gate of a "Crowbar" SCR, an open–collector indicator output and remote activation capability.

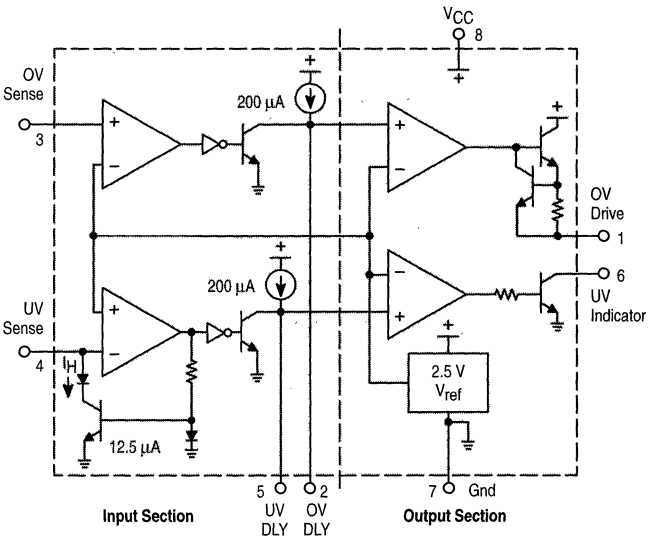


Over/Undervoltage Protection Circuit

MC3425P1

T_A = 0° to +70°C, Case 626

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. This device features dedicated over and undervoltage sensing channels with independently programmable time delays. The overvoltage channel has a high current drive output for use in conjunction with an external SCR "Crowbar" for shutdown. The undervoltage channel input comparator has hysteresis which is externally programmable, and an open–collector output for fault indication.



CMOS Micropower Undervoltage Sensing Circuits

MC33464H, N

T_A = –30° to +80°C, Case 1213, 1212

3

The MC33464 series are micropower undervoltage sensing circuits that are specifically designed for use with battery powered microprocessor based systems, where extended battery life is required. A choice of several threshold voltages from 0.9 V to 4.5 V are available. These devices feature a very low quiescent bias current of 0.8 μA typical.

The MC33464 series features a highly accurate voltage reference, a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation, a choice of output configurations between open drain or complementary MOS, and guaranteed operation below 1.0 V with extremely low standby current. These devices are available in either SOT–89 3–pin or SOT–23 5–pin surface mount packages.

Applications include direct monitoring of the MPU/logic power supply used in portable, appliance, automotive and industrial equipment.

MC33464 Features:

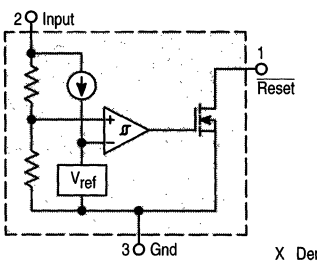
- Extremely Low Standby Current of 0.8 μA at V_{in} = 1.5 V
- Wide Input Voltage Range (0.7 V to 10 V)
- Monitors Power Supply Voltages from 1.1 V to 5.0 V
- High Accuracy Detector Threshold (±2.5%)
- Two $\overline{\text{Reset}}$ Output Types (Open Drain or Complementary Drive)
- Two Surface Mount Packages (SOT–89 or SOT–23 5–Pin)

ORDERING INFORMATION

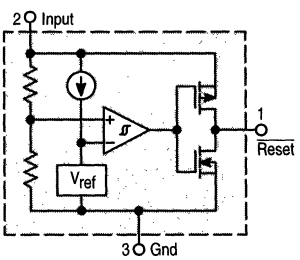
Device	Threshold Voltage	Type	Operating Temperature Range	Package (Qty/Reel)
MC33464H–09AT1	0.9	Open Drain $\overline{\text{Reset}}$	T_A = –30° to +80°C	SOT–89 (1000)
MC33464H–20AT1	2.0			
MC33464H–27AT1	2.7			
MC33464H–30AT1	3.0			
MC33464H–45AT1	4.5			
MC33464H–09CT1	0.9	Compl. MOS $\overline{\text{Reset}}$		
MC33464H–20CT1	2.0			
MC33464H–27CT1	2.7			
MC33464H–30CT1	3.0			
MC33464H–45CT1	4.5			
MC33464N–09ATR	0.9	Open Drain $\overline{\text{Reset}}$		SOT–23 (3000)
MC33464N–20ATR	2.0			
MC33464N–27ATR	2.7			
MC33464N–30ATR	3.0			
MC33464N–45ATR	4.5			
MC33464N–09CTR	0.9	Compl. MOS $\overline{\text{Reset}}$		
MC33464N–20CTR	2.0			
MC33464N–27CTR	2.7			
MC33464N–30CTR	3.0			
MC33464N–45CTR	4.5			

Other voltages from 0.9 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

MC33464X–YYATZ
Open Drain Configuration



MC33464X–YYCTZ
Complementary Drive Configuration



X Denotes Package Type
YY Denotes Threshold Voltage
TZ Denotes Taping Type

CMOS Micropower Undervoltage Sensing Circuits with Output Delay

MC33465N

T_A = –30° to +80°C, Case 1212

The MC33465 series are micropower undervoltage sensing circuits that are specifically designed for use with battery powered microprocessor based systems, where extended battery life is required. A choice of several threshold voltages from 0.9 V to 4.5 V are available. This device features a very low quiescent bias current of 1.0 µA typical.

The MC33465 series features a highly accurate voltage reference, a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation, a choice of output configurations between open drain or complementary MOS, a time delayed output, which can be programmed by the system designer, and guaranteed operation below 1.0 V with extremely low standby current. This device is available in a SOT–23 5–pin surface mount packages.

Applications include direct monitoring of the MPU/logic power supply used in portable, appliance, automotive and industrial equipment.

MC33465 Features:

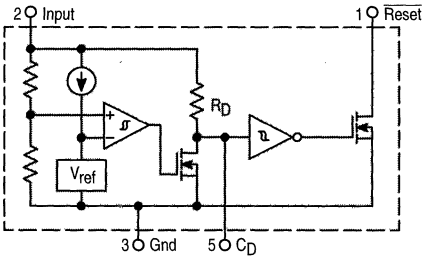
- Extremely Low Standby Current of 1.0 µA at V_{in} = 3.5 V
- Wide Input Voltage Range (0.7 V to 10 V)
- Monitors Power Supply Voltages from 1.1 V to 5.0 V
- High Accuracy Detector Threshold (±2.5%)
- Two $\overline{\text{Reset}}$ Output Types (Open Drain or Complementary Drive)
- Programmable Output Delay by External Capacitor (100 ms typ. with 0.15 µF)
- Surface Mount Package (SOT–23 5–Pin)
- Convenient Tape and Reel (3000 per Reel)

ORDERING INFORMATION

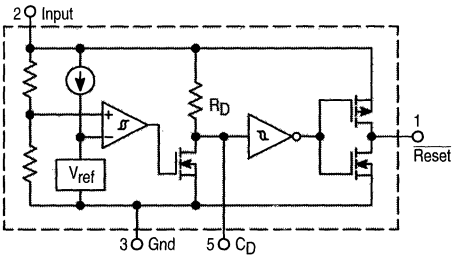
Device	Threshold Voltage	Type	Operating Temperature Range	Package
MC33465N–09ATR	0.9	Open Drain $\overline{\text{Reset}}$	T_A = –30° to +80°C	SOT–23
MC33465N–20ATR	2.0			
MC33465N–27ATR	2.7			
MC33465N–30ATR	3.0			
MC33465N–45ATR	4.5			
MC33465N–09CTR	0.9	Compl. MOS $\overline{\text{Reset}}$		
MC33465N–20CTR	2.0			
MC33465N–27CTR	2.7			
MC33465N–30CTR	3.0			
MC33465N–45CTR	4.5			

Other voltages from 0.9 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

MC33465N–YYATZ
Open Drain Configuration



MC33465N–YYCTZ
Complementary Drive Configuration



YY Denotes Threshold Voltage
TZ Denotes Taping Type

3

Undervoltage Sensing Circuit

MC34064P–5, D–5, DM–5
T_A = 0° to +70°C, Case 29, 751, 846A

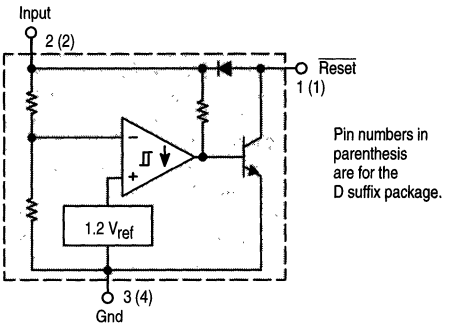
MC33064P–5, D–5, DM–5
T_A = –40° to +85°C, Case 29, 751, 846A

MC34164P–3, P–5, D–3, D–5, DM–3, DM–5
T_A = 0° to +70°C, Case 29, 751, 846A

MC33164P–3, P–5, D–3, D–5, DM–3, DM–5
T_A = –40° to +85°C, Case 29, 751, 846A

The MC34064 and MC34164 are two families of undervoltage sensing circuits specifically designed for use as reset controllers in microprocessor–based systems. They offer the designer an economical solution for low voltage detection with a single external resistor. Both parts feature a trimmed bandgap reference, and a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation.

The two families of undervoltage sensing circuits taken together, cover the needs of the most commonly specified power supplies used in MCU/MPU systems. Key parameter specifications of the MC34164 family were chosen to complement the MC34064 series. The table summarizes critical parameters of both families. The MC34064 fulfills the needs of a 5.0 V ± 5% system and features a tighter hysteresis specification. The MC34164 series covers 5.0 V ± 10% and 3.0 V ± 5% power supplies with significantly lower power consumption, making them ideal for applications where extended battery life is required such as consumer products or hand held equipment.



Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.

The MC34164 is specifically designed for battery powered applications where low bias current (1/25th of the MC34064's) is an important characteristic.

Table 14. Undervoltage Sense/Reset Controller Features

MC34X64 devices are specified to operate from 0° to +70°C, and MC33X64 devices operate from –40° to +85°C.

Device	Standard Power Supply Supported	Typical Threshold Voltage (V)	Typical Hysteresis Voltage (V)	Minimum Output Sink Current (mA)	Power Supply Input Voltage Range (V)	Maximum Quiescent Input Current	Suffix/ Package
MC34064/MC33064	5.0 V ± 5%	4.6	0.02	10	1.0 to 10	500 µA @ V_{in} = 5.0 V	P–5/29
							D–5/751
							DM–5/846A
MC34164/MC33164	5.0 V ± 10%	4.3	0.09	7.0	1.0 to 12	20 µA @ V_{in} = 5.0 V	P–5/29
							D–5/751
							DM–5/846A
MC34164/MC33164	3.0 V ± 5%	2.7	0.06	6.0	1.0 to 12	15 µA @ V_{in} = 3.0 V	P–3/29
							D–3/751
							DM–3/846A

Universal Voltage Monitor

MC34161P, D

T_A = 0° to +70°C, Case 626, 751

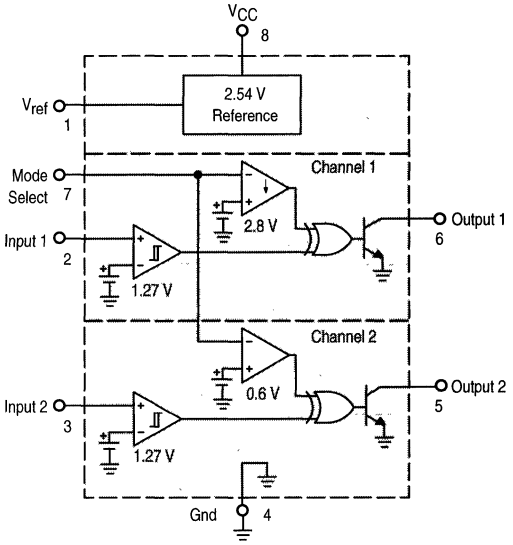
MC33161P, D

T_A = –40° to +85°C, Case 626, 751

The MC34161, MC33161 series are universal voltage monitors intended for use in a wide variety of voltage sensing applications. These devices offer the circuit designer an economical solution for positive and negative voltage detection. The circuit consists of two comparator channels each with hysteresis, a unique Mode Select Input for channel programming, a pinned out 2.54 V reference, and two open collector outputs capable of sinking in excess of 10 mA. Each comparator channel can be configured as either inverting or noninverting by the Mode Select Input. This allows over, under, and window detection of positive and negative voltages. The minimum supply voltage needed for these devices to be fully functional is 2.0 V for positive voltage sensing and 4.0 V for negative voltage sensing.

Applications include direct monitoring of positive and negative voltages used in appliance, automotive, consumer, and industrial equipment.

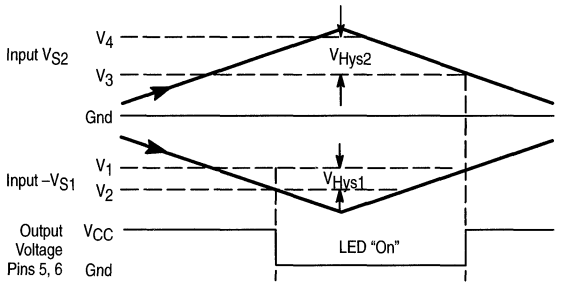
- Unique Mode Select Input Allows Channel Programming
- Over, Under, and Window Voltage Detection
- Positive and Negative Voltage Detection
- Fully Functional at 2.0 V for Positive Voltage Sensing and 4.0 V for Negative Voltage Sensing
- Pinned Out 2.54 V Reference with Current Limit Protection
- Low Standby Current
- Open Collector Outputs for Enhanced Device Flexibility

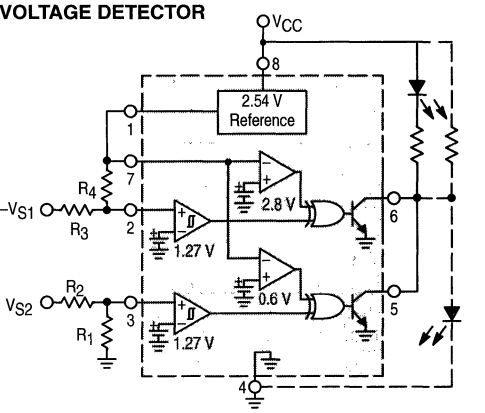


TRUTH TABLE

Mode Select Pin 7	Input 1 Pin 2	Output 1 Pin 6	Input 2 Pin 3	Output 2 Pin 5	Comments
GND	0 1	0 1	0 1	0 1	Channels 1 & 2: Noninverting
V_{ref}	0 1	0 1	0 1	1 0	Channel 1: Noninverting Channel 2: Inverting
V_{CC} (>2.0 V)	0 1	1 0	0 1	1 0	Channels 1 & 2: Inverting

POSITIVE AND NEGATIVE OVERVOLTAGE DETECTOR





Battery Management Circuits

Battery Charger ICs

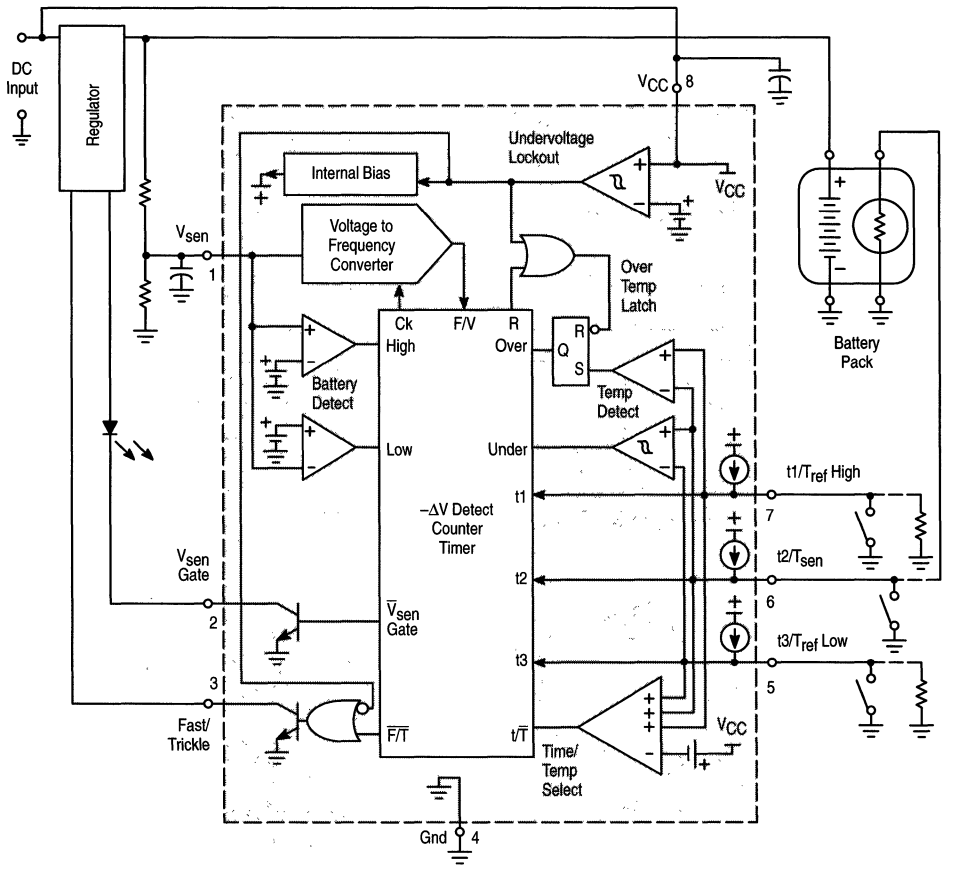
Battery Fast Charge Controller

MC33340P, D

T_A = –25° to +85°C, Case 626, 751

The MC33340 is a monolithic control IC that is specifically designed as a fast charge controller for Nickel Cadmium (NiCd) and Nickel Metal Hydride (NiMH) batteries. This device features negative slope voltage detection as the primary means for fast charge termination. Accurate detection is ensured by an output that momentarily interrupts the charge current for precise voltage sampling. An additional secondary backup termination method can be selected that consists of either a programmable time or temperature limit. Protective features include battery over and undervoltage detection, latched over temperature detection, and power supply input undervoltage lockout with hysteresis. Provisions for entering a rapid test mode are available for enhanced end product testing. This device is available in an economical 8–lead surface mount package.

- Negative Slope Voltage Detection
- Accurate Zero Current Battery Voltage Sensing
- Programmable 1 to 4 Hour Fast Charge Time Limit
- Programmable Over/Under Temperature Detection
- Battery Over and Undervoltage Fast Charge Protection
- Rapid System Test Mode
- Power Supply Input Undervoltage Lockout with Hysteresis
- Operating Voltage Range of 3.0 V to 18 V



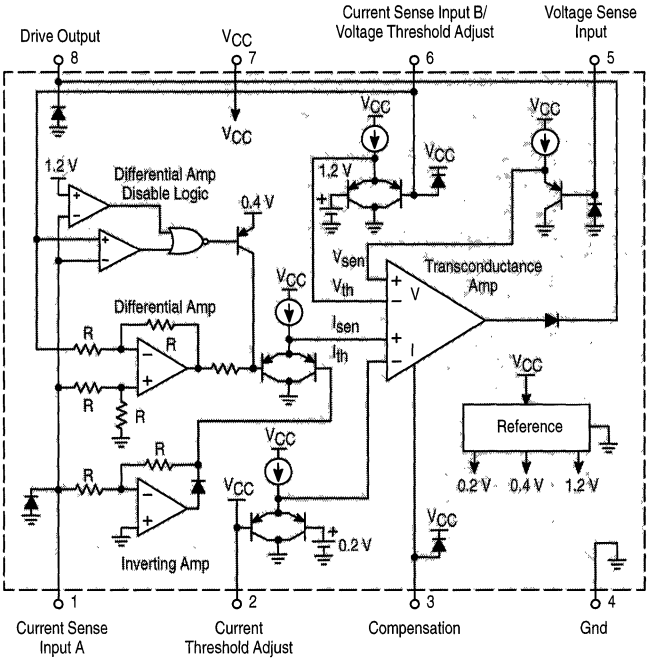
Power Supply Battery Charger Regulation Control Circuit

MC33341P, D

T_A = –40° to +85°C, Case 626, 751

The MC33341 is a monolithic regulation control circuit that is specifically designed to close the voltage and current feedback loops in power supply and battery charger applications. This device features the unique ability to perform source high–side, load high–side, source low–side, and load low–side current sensing, each with either an internally fixed or externally adjustable threshold. The various current sensing modes are accomplished by a means of selectively using the internal differential amplifier, inverting amplifier, or a direct input path. Positive voltage sensing is performed by an internal voltage amplifier. The voltage amplifier threshold is internally fixed and can be externally adjusted in all low–side current sensing applications. An active high drive output is provided to directly interface with economical optoisolators for isolated output power systems. This device is available in 8–lead dual–in–line and surface mount packages.

- Differential Amplifier for High–Side Source and Load Current Sensing
- Inverting Amplifier for Source Return Low–Side Current Sensing
- Noninverting Input Path for Load Low–Side Current Sensing
- Fixed or Adjustable Current Threshold in all Current Sensing Modes
- Positive Voltage Sensing in all Current Sensing Modes
- Fixed Voltage Threshold in all Current Sensing Modes
- Adjustable Voltage Threshold in all Low–Side Current Sensing Modes
- Output Driver Directly Interfaces with Economical Optoisolators
- Operating Voltage Range of 2.3 V to 18 V



Battery Pack ICs

Lithium Battery Protection Circuit for One to Four Cell Battery Packs

MC33345DW, DTB

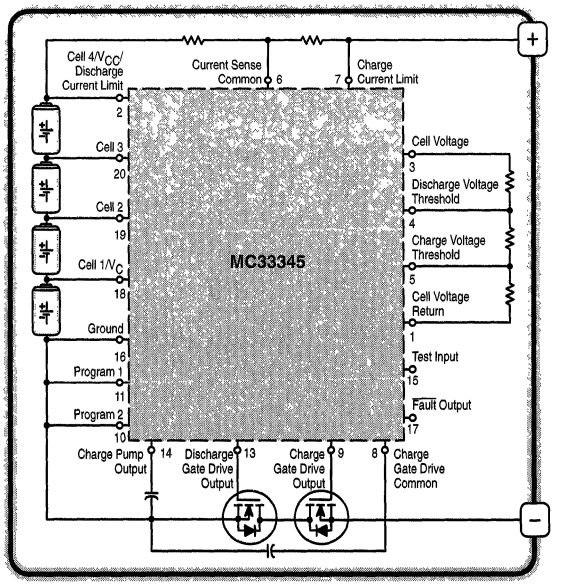
T_A = –25° to +85°C, Case 751D, 948E

3

The MC33345 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one to four cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, cell voltage balancing with on–chip balancing resistors, and a virtually zero current sleepmode state when the cells are discharged. Additional features include an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack, and the programmability for a one to four cell battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. The MC33345 is available in standard and low profile 20 lead surface mount packages.

- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Charge and Discharge Current Limit Detection with Delayed Shutdown
- Cell Voltage Balancing
- On–Chip Balancing Resistors
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Programmable for One, Two, Three or Four Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Four Cell Smart Battery Pack



Lithium Battery Protection Circuit for Three or Four Cell Battery Packs

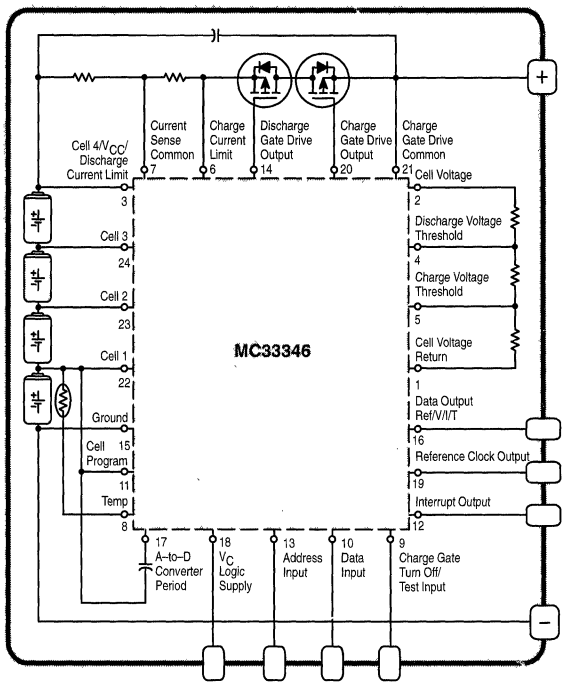
MC33346DW, DTB

T_A = –40° to +85°C, Case 751E, 948H

The MC33346 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of three or four cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, cell voltage balancing with on–chip balancing resistors, and virtually zero current sleepmode state when the cells are discharged. Additional features consists of a six wire microcontroller interface bus that can selectively provide a pulse output that represents the internal reference voltage, cell voltage, cell current and temperature, as well as control the states of four internal balancing and two external MOSFET switches. A microcontroller time reference output is available for gas gauge implementation. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. The MC33346 is available in standard and low profile 24 lead surface mount packages.

- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Delayed Current Shutdown
- Cell Voltage Balancing with On–Chip Resistors
- Six Wire Microcontroller Interface Bus
- Data Output for Reference, Voltage, Current, and Temperature
- Microcontroller Time Reference Output for Gas Gauging
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Programmable for Three or Four Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Four Cell Smart Battery Pack



Battery Pack ICs (continued)

Lithium Battery Protection Circuit for One or Two Cell Battery Packs

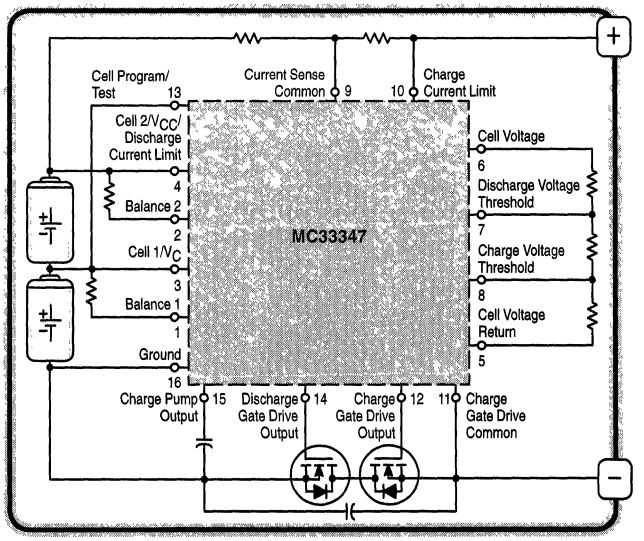
MC33347D, DTB

T_A = –25° to +85°C, Case 751B, 948F

The MC33347 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one or two cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, continuous cell voltage balancing with the choice of on–chip or external balancing resistors, and a virtually zero current sleepmode state when the cells are discharged. Additional features include an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack, and the programmability for one or two cell battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. This MC33347 is avaialble in standard and low profile 16 lead surface mount packages.

- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Charge and Discharge Current Limit Detection with Delayed Shutdown
- Continuous Cell Voltage Balancing
- On–Chip or External Balancing Resistors
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Programmable for One or Two Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Two Cell Smart Battery Pack



Battery Pack ICs (continued)

Lithium Battery Protection Circuit for One Cell Battery Packs

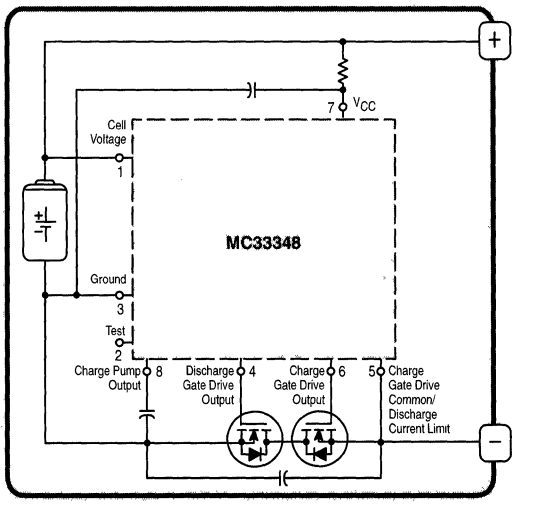
MC33348D, DM

T_A = –25° to +85°C, Case 751, 846A

The MC33348 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one cell rechargeable battery pack. Cell protection features consist of internally trimmed charge and discharge voltage limits, discharge current limit detection with a delayed shutdown, and a virtually zero current sleepmode state when the cell is discharged. An additional feature includes an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. This MC33348 is available in standard and micro 8 lead surface mount packages.

- Internally Trimmed Charge and Discharge Voltage Limits
- Discharge Current Limit Detection with Delayed Shutdown
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Dedicated for One Cell Applications
- Minimum Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical One Cell Smart Battery Pack



ORDERING INFORMATION

Device	Charge Overvoltage Threshold (V)	Charge Overvoltage Hysteresis (mV)	Discharge Undervoltage Threshold (V)	Discharge Current Limit Threshold (mV)	Operating Temperature Range	Package
MC33348D–1	4.20	300	2.25	400	T_A = –25° to +85°C	SO–8
MC33348D–2				200		
MC33348D–3	4.25		2.28	400		
MC33348D–4				200		
MC33348D–5	4.35		2.30	400		
MC33348D–6				200		
MC33348DM–1	4.20		2.25	400		Micro–8
MC33348DM–2				200		
MC33348DM–3	4.25		2.28	400		
MC33348DM–4				200		
MC33348DM–5	4.35		2.30	400		
MC33348DM–6				200		

NOTE: Additional threshold limit options can be made available. Consult your local Motorola sales office for information.

MOSFET/IGBT Drivers

High Speed Dual Drivers

(Inverting)

MC34151P, D

T_A = 0° to +70°C, Case 626, 751

MC33151P, D

T_A = –40° to +85°C, Case 626, 751

(Noninverting)

MC34152P, D

T_A = 0° to +70°C, Case 626, 751

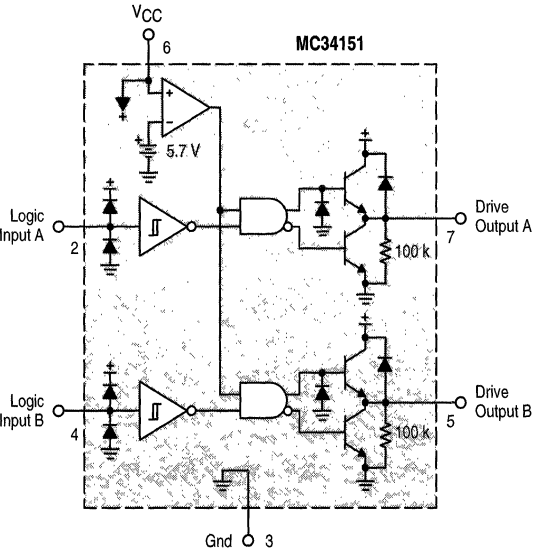
MC33152P, D

T_A = –40° to +85°C, Case 626, 751

These two series of high speed dual MOSFET driver ICs are specifically designed for applications requiring low current digital circuitry to drive large capacitive loads at high slew rates. Both series feature a unique undervoltage lockout function which puts the outputs in a defined low state in an undervoltage condition. In addition, the low "on" state resistance of these bipolar drivers allows significantly higher output currents at lower supply voltages than with competing drivers using CMOS technology.

The MC34151 series is pin–compatible with the MMH0026 and DS0026 dual MOS clock drivers, and can be used as drop–in replacements to upgrade system performance. The MC34152 noninverting series is a mirror image of the inverting MC34151 series.

These devices can enhance the drive capabilities of first generation switching regulators or systems designed with CMOS/TTL logic devices. They can be used in dc–to–dc converters, motor controllers, capacitor charge pump converters, or virtually any other application requiring high speed operation of power MOSFETs.



Single IGBT Driver

MC33153P, D

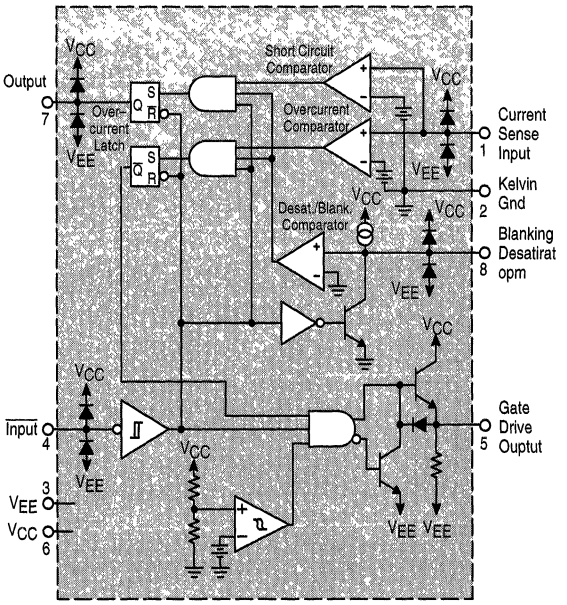
T_A = –40° to +105°C, Case 626, 751

The MC33153 is specifically designed to drive the gate of an IGBT used for ac induction motors. It can be used with discrete IGBTs and IBGT modules up to 100 A.

Typical applications are ac induction motor control, brushless dc motor control, and uninterruptable power supplies.

These devices are available in dual–in–line and surface mount packages and include the following features:

- High Current Output Stage : 1.0 A Source – 2.0 A Sink
- Protection Circuits for Both Conventional and SenseIGBTs
- Current Source for Blanking Timing
- Protection Against Overcurrent and Short Circuit
- Undervoltage Lockout Optimized for IGBT's
- Negative Gate Drive Capability



Single IGBT Gate Driver

MC33154D, P

T_A = –40° to +85°C, Case 626, 751

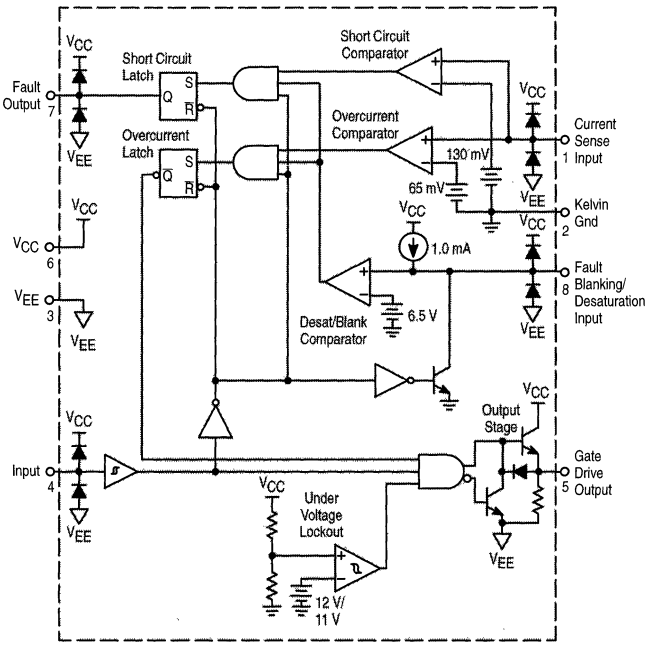
The MC33154 is specifically designed as an IGBT driver for high power applications including ac induction motor control, brushless dc motor control and uninterruptible power supplies.

The MC33154 is similar to the MC33153, except that the output drive is in–phase with the logic input, the output source current drive is four times higher and the supply voltage rating is higher.

Although designed for driving discrete and module IGBTs, this device offers a cost effective solution for driving power MOSFETs and Bipolar Transistors.

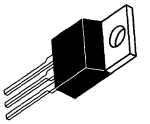
These devices are available in dual–in–line and surface mount packages and include the following features:

- High Current Output Stage: 4.0 A Source/2.0 A Sink
- Protection Circuits for Both Conventional and Sense IGBTs
- Programmable Fault Blanking Time
- Protection against Overcurrent and Short Circuit
- Undervoltage Lockout Optimzed for IGBTs
- Negative Gate Drive Capability
- Cost Effectively Drives Power MOSFETs and Bipolar Transistors

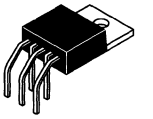


Power Supply Circuits Package Overview

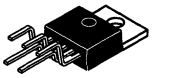
CASE 29
P, Z SUFFIX



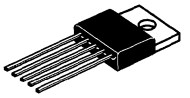
CASE 221A
T, KC SUFFIX



CASE 314A
TH SUFFIX



CASE 314B
TV SUFFIX

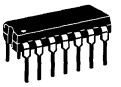


CASE 314D
T SUFFIX

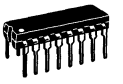
CASE 369
DT–1 SUFFIX

CASE 369A
DT SUFFIX

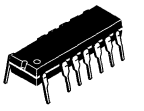
CASE 626
N, P, P1 SUFFIX



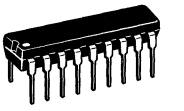
CASE 646
P SUFFIX



CASES 648, 648C
N, P, P2 SUFFIX



CASE 648E
P SUFFIX



CASE 707
N SUFFIX

CASE 751
D, D1, D2 SUFFIX

CASE 751A
D SUFFIX

CASE 751B
D SUFFIX

CASE 751D
DW SUFFIX

CASE 751E
DW SUFFIX

CASE 751G
DW SUFFIX

CASE 751K
D SUFFIX

CASE 751N
DW SUFFIX

CASE 775
FN SUFFIX

CASE 846A
DM SUFFIX

CASE 873A
FB SUFFIX

CASE 936
D2T SUFFIX

CASE 936A
D2T SUFFIX

CASE 948E
DTB SUFFIX

CASE 948F
DTB SUFFIX

CASE 948G
DTB SUFFIX

CASE 948H
DTB SUFFIX

CASE 1212
N SUFFIX

CASE 1213
H SUFFIX

Device Listing and Related Literature

Linear Voltage Regulators

Switching Regulator Control

Switching Regulator Control (continued)

Special Switching Regulator Controllers

Power Factor Correction Controllers

Power Drivers

Power Supervisory

ADDENDUM

RELATED APPLICATION NOTES

3

App Note	Title	Related Device
AN703	Designing Digitally–Controlled Power Supplies	**MC1723C**
AN719	A New Approach to Switching Regulators	**General**
AN1040	Mounting Techniques for Power Semiconductors	**LM317, LM337, MC7800, MC78M00, MC7900, MC79M00**
AN1065	Use of the MC68HC68T1 Real–Time Clock with Multiple Time Bases	**MC34164, MC33164**
AN1315	An Evaluation System Interfacing the MPX2000 Series Pressure Sensors to a Microprocessor	**MC34064, MC33064**
AN920	Theory and Applications of the MC34063 and μA78S40 Switching Regulator Control CIrcuits	**μA78S40**
AN976	A New High Performance Current–Mode Controller Teams Up with Current Sensing Power MOSFETs	**MC34129**
AN983	A Simplified Power Supply Design Using the TL494 Control Circuit	**TL494**
ANE424	50 W Current Mode Controlled Offline Switchmode Power Supply	**UC3842A, UC2842A UC3843A, UC2843A**

LM317

Three-Terminal Adjustable Output Positive Voltage Regulator

THREE–TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SEMICONDUCTOR TECHNICAL DATA

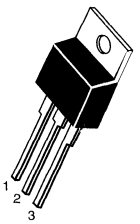
The LM317 is an adjustable 3–terminal positive voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof.

The LM317 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

- Output Current in Excess of 1.5 A
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe–Area Compensation
- Floating Operation for High Voltage Applications
- Available in Surface Mount D^{2}PAK, and Standard 3–Lead Transistor Package
- Eliminates Stocking many Fixed Voltages

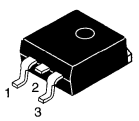
T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface connected to Pin 2.



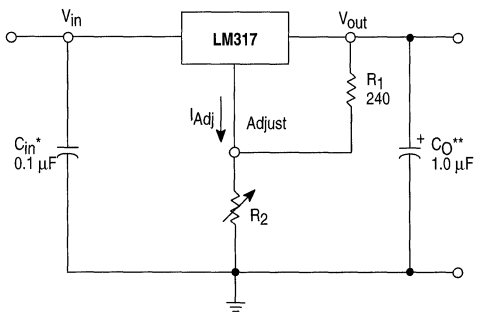
Pin 1. Adjust
2. V_{out}
3. V_{in}

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D^{2}PAK)



Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

Standard Application



* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\ R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM317BD2T	T_J = –40° to +125°C	Surface Mount
LM317BT		Insertion Mount
LM317D2T	T_J = 0° to +125°C	Surface Mount
LM317T		Insertion Mount

3

MAXIMUM RATINGS

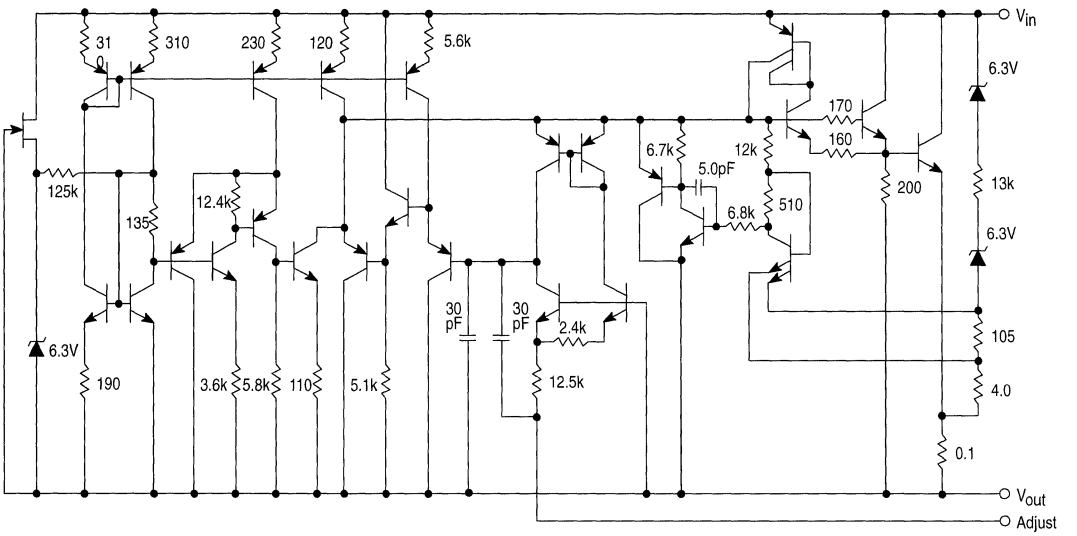
Rating	Symbol	Value	Unit
Input–Output Voltage Differential	$V_I–V_O$	40	Vdc
Power Dissipation			
Case 221A			
T_A = +25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	65	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Case 936 (D^2PAK)			
T_A = +25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	70	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_I–V_O$ = 5.0 V; I_O = 0.5 A for D2T and T packages; $T_J = T_{low}$ to T_{high} [Note 1]; I_{max} and P_{max} [Note 2]; unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3), T_A = +25°C, 3.0 V ≤ $V_I–V_O$ ≤ 40 V	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 3), T_A = +25°C, 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}				
V_O ≤ 5.0 V			–	5.0	25	mV
V_O ≥ 5.0 V			–	0.1	0.5	% V_O
Thermal Regulation, T_A = +25°C (Note 6), 20 ms Pulse		Reg_{therm}	–	0.03	0.07	% V_O/W
Adjustment Pin Current	3	I_{Adj}	–	50	100	µA
Adjustment Pin Current Change, 2.5 V ≤ $V_I–V_O$ ≤ 40 V, 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}	1, 2	ΔI_{Adj}	–	0.2	5.0	µA
Reference Voltage, 3.0 V ≤ $V_I–V_O$ ≤ 40 V, 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}	3	V_{ref}	1.2	1.25	1.3	V
Line Regulation (Note 3), 3.0 V ≤ $V_I–V_O$ ≤ 40 V	1	Reg_{line}	–	0.02	0.07	% V
Load Regulation (Note 3), 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}				
V_O ≤ 5.0 V			–	20	70	mV
V_O ≥ 5.0 V			–	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.7	–	% V_O
Minimum Load Current to Maintain Regulation ($V_I–V_O$ = 40 V)	3	I_{Lmin}	–	3.5	10	mA
Maximum Output Current	3	I_{max}				A
$V_I–V_O$ ≤ 15 V, P_D ≤ P_{max}, T Package			1.5	2.2	–	
$V_I–V_O$ = 40 V, P_D ≤ P_{max}, T_A = +25°C, T Package			0.15	0.4	–	
RMS Noise, % of V_O, T_A = +25°C, 10 Hz ≤ f ≤ 10 kHz		N	–	0.003	–	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 4)	4	RR				dB
Without C_{Adj}			–	65	–	
C_{Adj} = 10 µF			66	80	–	
Long–Term Stability, $T_J = T_{high}$ (Note 5), T_A = +25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case, T Package		$R_{\theta JC}$	–	5.0	–	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C, for LM317T, D2T. T_{low} to T_{high} = –40° to +125°C, for LM317BT, BD2T.
2. I_{max} = 1.5 A, P_{max} = 20 W
3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long–Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Power dissipation within an IC voltage regulator produces a temperature gradient on the die, affecting individual IC components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.

Representative Schematic Diagram



This device contains 29 active transistors.

Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit

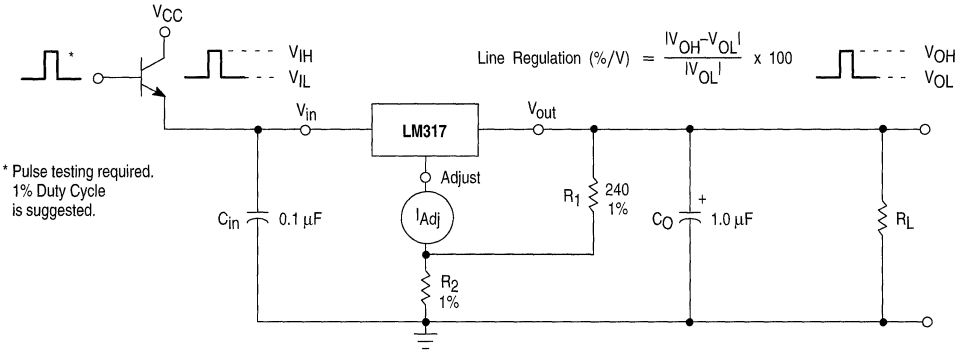
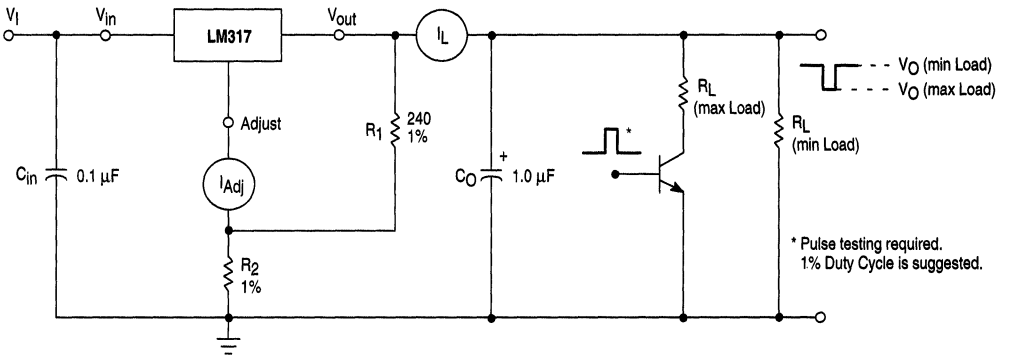


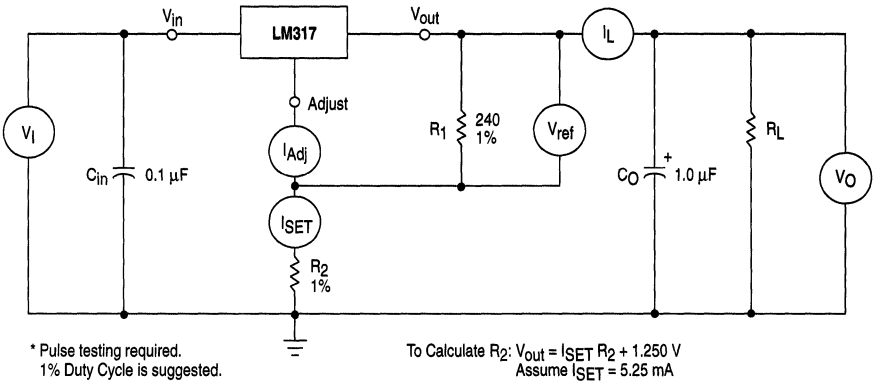
Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit



Load Regulation (mV) = V_O (min Load) – V_O (max Load)

Load Regulation (% V_O) = $\frac{V_O \text{ (min Load)} - V_O \text{ (max Load)}}{V_O \text{ (min Load)}}$ x 100

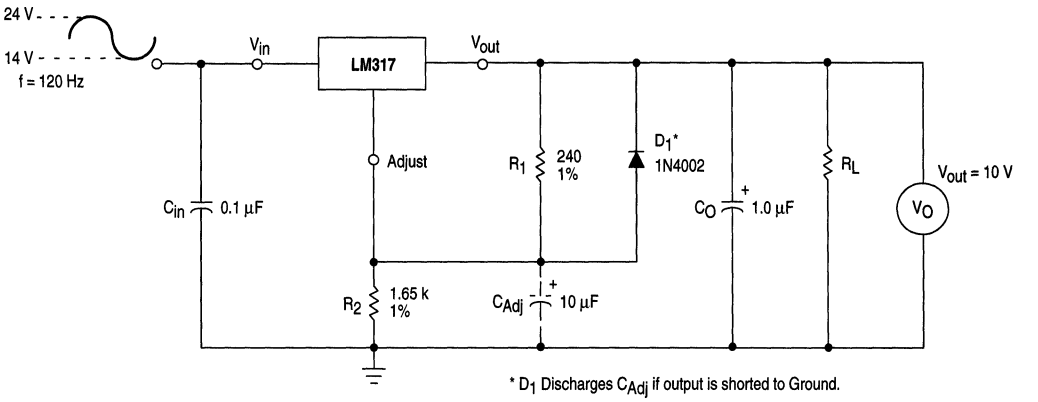
Figure 3. Standard Test Circuit



* Pulse testing required.
1% Duty Cycle is suggested.

To Calculate R_2: $V_{out} = I_{SET} R_2 + 1.250$ V
Assume I_{SET} = 5.25 mA

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if output is shorted to Ground.

Figure 5. Load Regulation

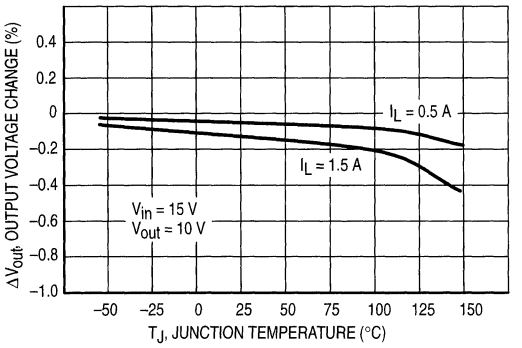


Figure 6. Current Limit

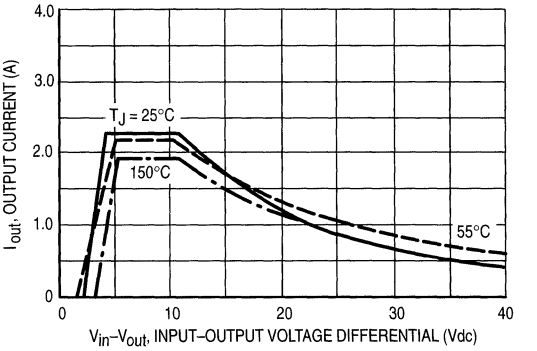


Figure 7. Adjustment Pin Current

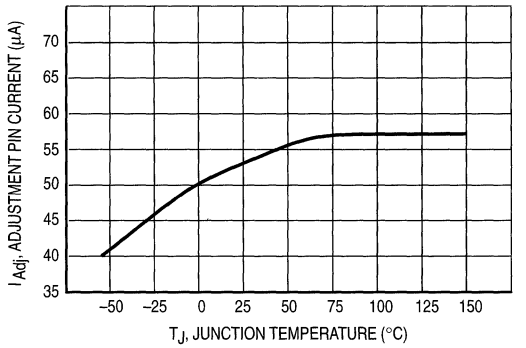


Figure 8. Dropout Voltage

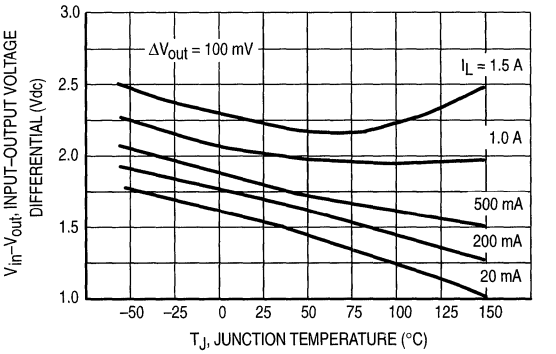


Figure 9. Temperature Stability

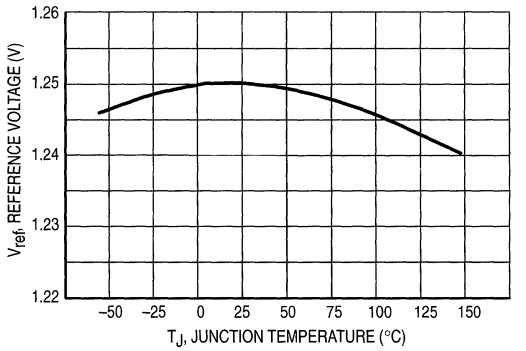


Figure 10. Minimum Operating Current

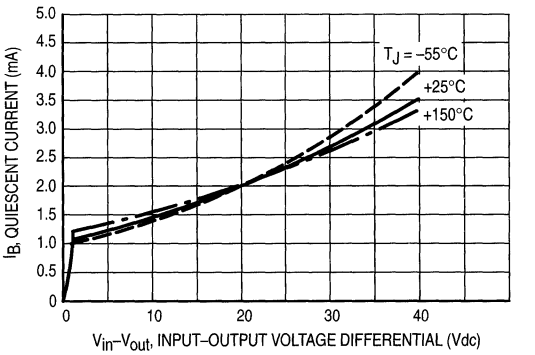


Figure 11. Ripple Rejection versus Output Voltage

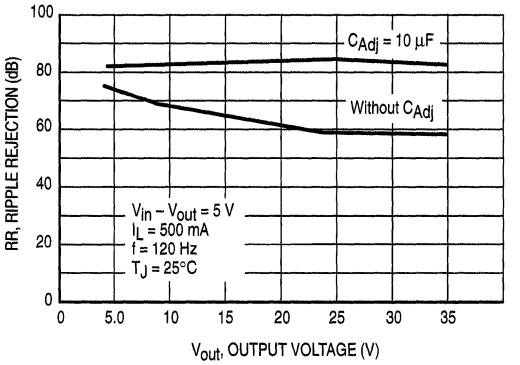


Figure 12. Ripple Rejection versus Output Current

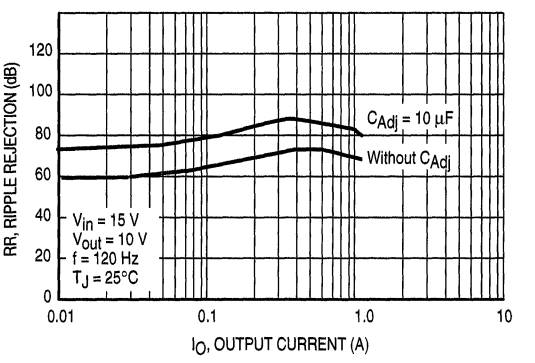


Figure 13. Ripple Rejection versus Frequency

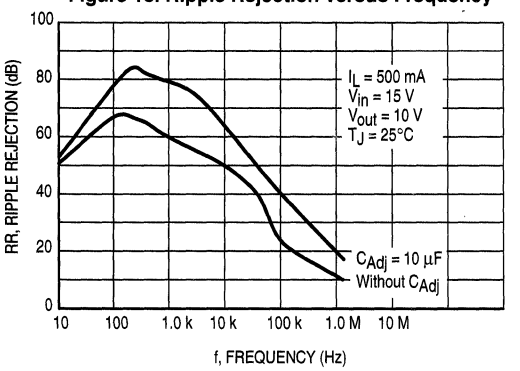


Figure 14. Output Impedance

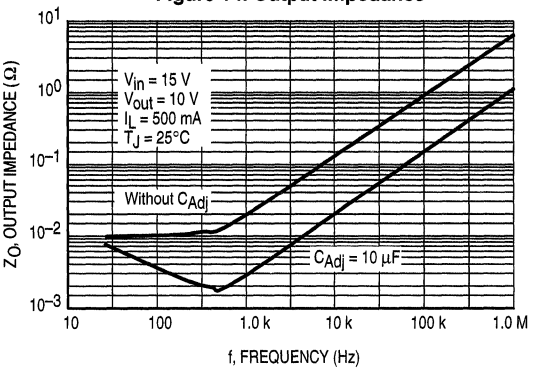


Figure 15. Line Transient Response

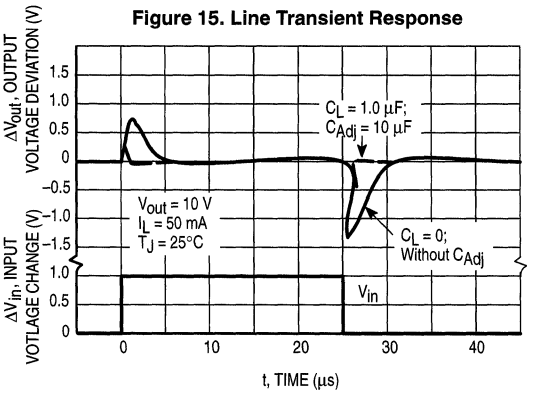
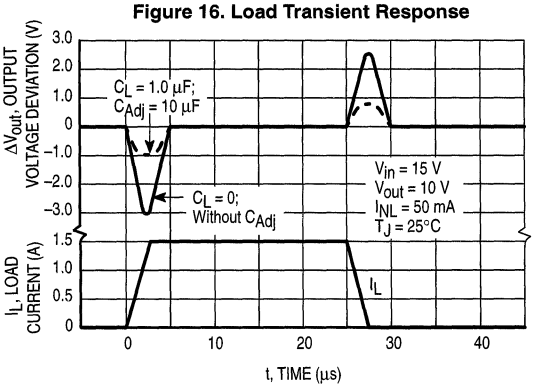


Figure 16. Load Transient Response



APPLICATIONS INFORMATION

Basic Circuit Operation

The LM317 is a 3–terminal floating regulator. In operation, the LM317 develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 to ground.

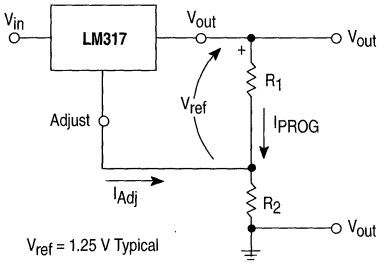
The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}R_2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM317 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



Load Regulation

The LM317 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM317 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 10 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

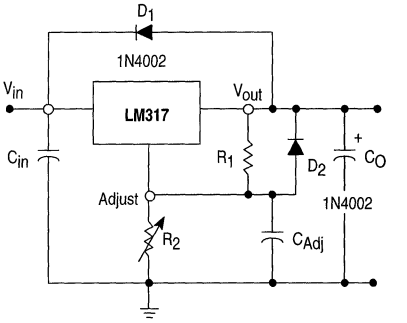


Figure 19. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

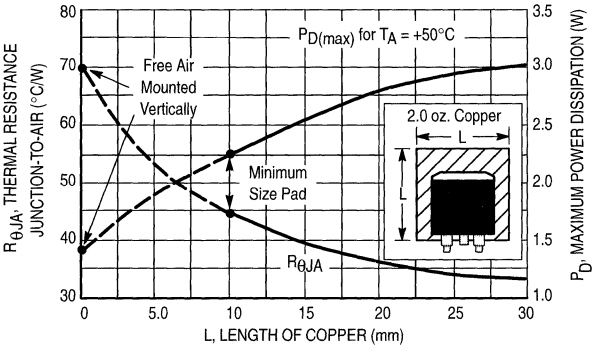


Figure 20. "Laboratory" Power Supply with Adjustable Current Limit and Output Voltage

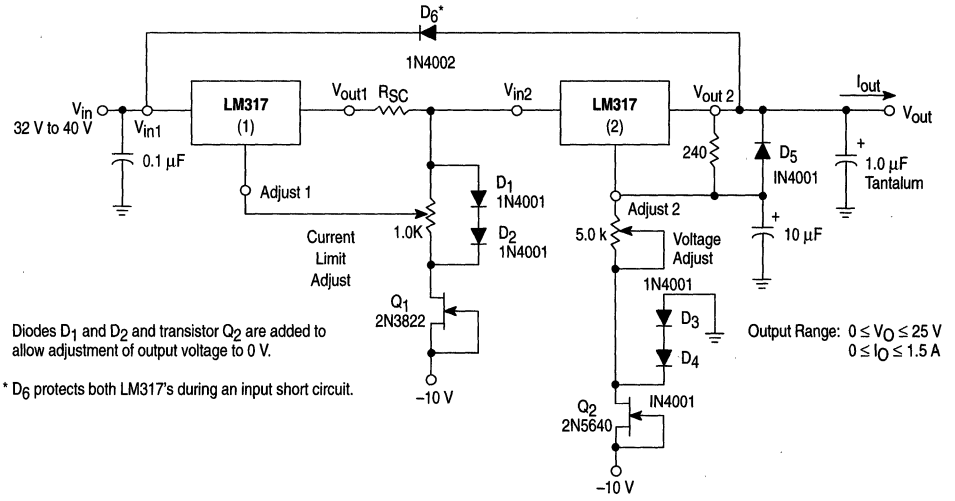
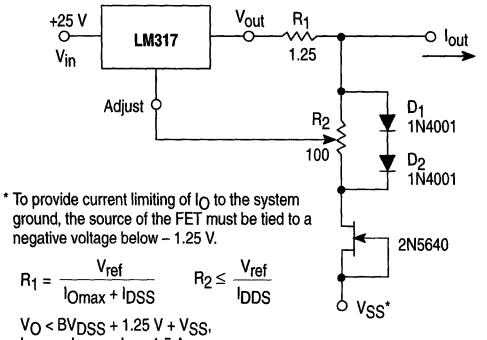


Figure 21. Adjustable Current Limiter

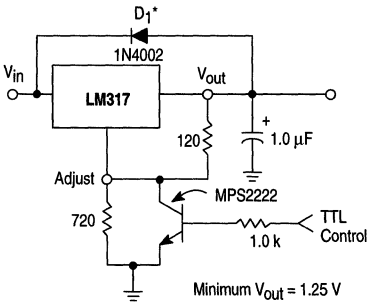


* To provide current limiting of I_O to the system ground, the source of the FET must be tied to a negative voltage below – 1.25 V.

$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}} \qquad R_2 \leq \frac{V_{ref}}{I_{DDS}}$$

$V_O < BV_{DSS} + 1.25\ V + V_{SS}$,
$I_{Lmin} - I_{DSS} < I_O < 1.5\ A$.
As shown $0 < I_O < 1.0\ A$.

Figure 22. 5.0 V Electronic Shutdown Regulator



* D_1 protects the device during an input short circuit.

Figure 23. Slow Turn–On Regulator

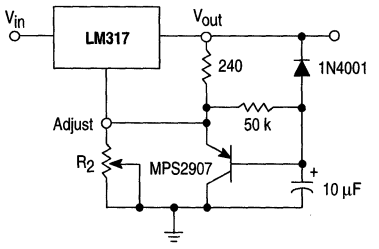
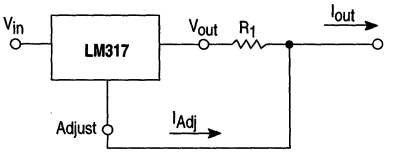


Figure 24. Current Regulator



$$I_{out} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj}$$

$$= \frac{1.25\ V}{R_1}$$

$10\ mA \leq I_{out} \leq 1.5\ A$

LM317L

Three-Terminal Adjustable Output Positive Voltage Regulator

The LM317L is an adjustable 3–terminal positive voltage regulator capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making them essentially blow–out proof.

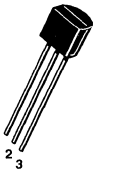
The LM317L serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317L can be used as a precision current regulator.

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3–Lead Transistor Package
- Eliminates Stocking Many Fixed Voltages

LOW CURRENT THREE–TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SEMICONDUCTOR TECHNICAL DATA

Z SUFFIX
PLASTIC PACKAGE
CASE 29



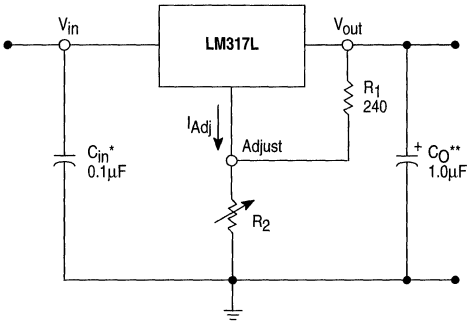
Pin 1. Adjust
2. V_{out}
3. V_{in}

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8*)

Pin 1. V_{in}
2. V_{out}
3. V_{out}
4. Adjust
5. N.C.
6. V_{out}
7. V_{out}
8. N.C.

* SOP–8 is an internally modified SO–8 package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP–8 conforms to all external dimensions of the standard SO–8 package.

Simplified Application



* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM317LD	T_J = 0° to +125°C	SOP–8
LM317LZ		Plastic
LM317LBD	T_J = –40° to +125°C	SOP–8
LM317LBZ		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input–Output Voltage Differential	V_I–V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

3

ELECTRICAL CHARACTERISTICS (V_I–V_O = 5.0 V; I_O = 40 mA; T_J = T_{low} to T_{high} [Note 1]; I_{max} and P_{max} [Note 2]; unless otherwise noted.)

Characteristics	Figure	Symbol	LM317L, LB Min	LM317L, LB Typ	LM317L, LB Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ V_I – V_O ≤ 40 V	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 3), T_A = 25°C 10 mA ≤ I_O ≤ I_{max} – LM317L V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 – –	 5.0 0.1	 25 0.5	 mV % V_O
Adjustment Pin Current	3	I_{Adj}	–	50	100	µA
Adjustment Pin Current Change 2.5 V ≤ V_I – V_O ≤ 40 V, P_D ≤ P_{max} 10 mA ≤ I_O ≤ I_{max} – LM317L	1, 2	ΔI_{Adj}	–	0.2	5.0	µA
Reference Voltage 3.0 V ≤ V_I – V_O ≤ 40 V, P_D ≤ P_{max} 10 mA ≤ I_O ≤ I_{max} – LM317L	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V ≤ V_I – V_O ≤ 40 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max} – LM317L V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 – –	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.7	–	% V_O
Minimum Load Current to Maintain Regulation (V_I – V_O = 40 V)	3	I_{Lmin}	–	3.5	10	mA
Maximum Output Current V_I – V_O ≤ 6.25 V, P_D ≤ P_{max}, Z Package V_I – V_O ≤ 40 V, P_D ≤ P_{max}, T_A = 25°C, Z Package	3	I_{max}	 100 –	 200 20	 – –	mA
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz		N	–	0.003	–	% V_O
Ripple Rejection (Note 4) V_O = 1.2 V, f = 120 Hz C_{Adj} = 10 µF, V_O = 10.0 V	4	RR	 60 –	 80 80	 – –	dB
Long Term Stability, T_J = T_{high} (Note 5) T_A = 25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance, Junction–to–Case Z Package		$R_{\theta JC}$	–	83	–	°C/W
Thermal Resistance, Junction–to–Air Z Package		$R_{\theta JA}$	–	160	–	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C for LM317L –40° to +125°C for LM317LB
2. I_{max} = 100 mA P_{max} = 625 mW
3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long–Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

Representative Schematic Diagram

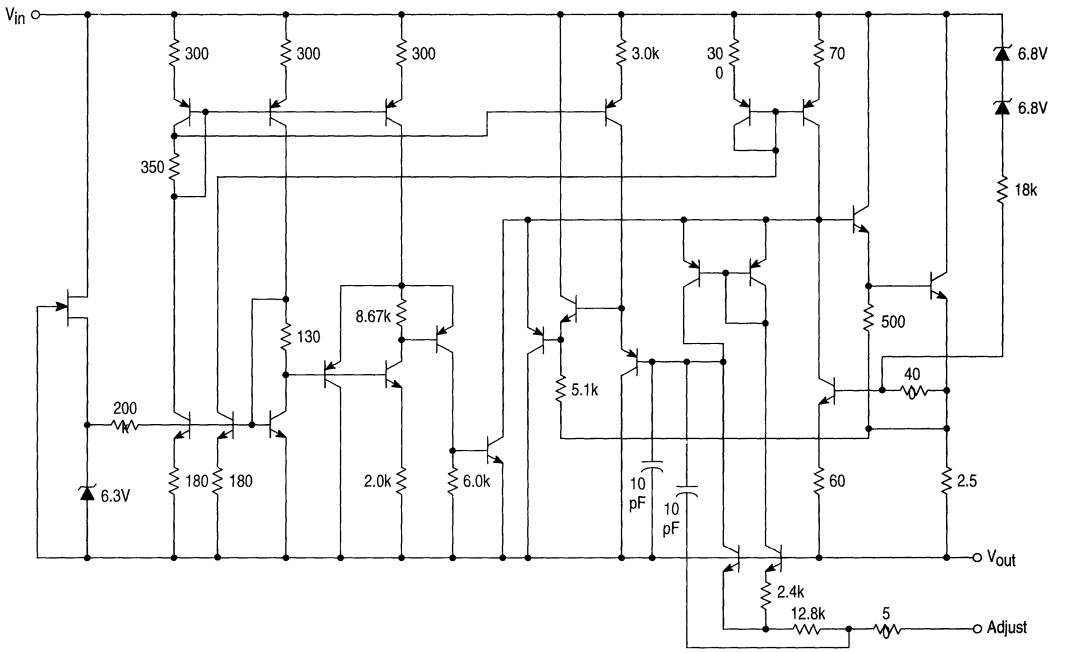


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit

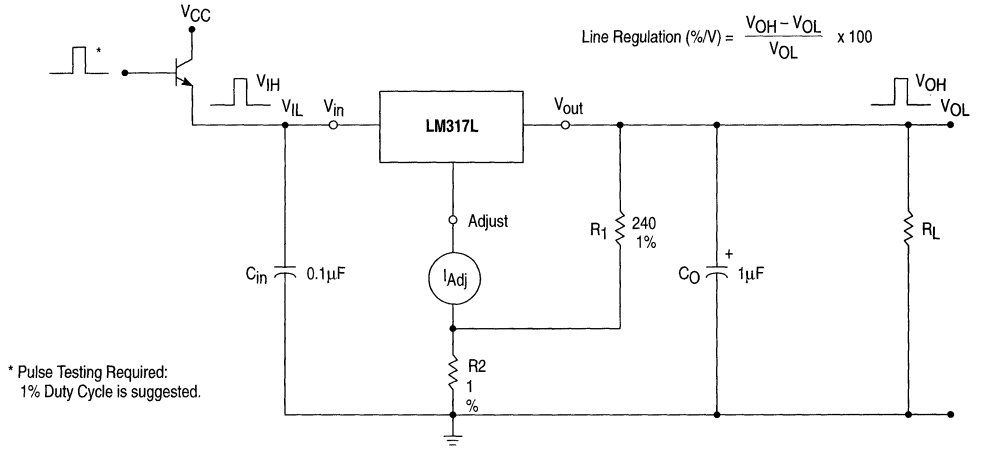
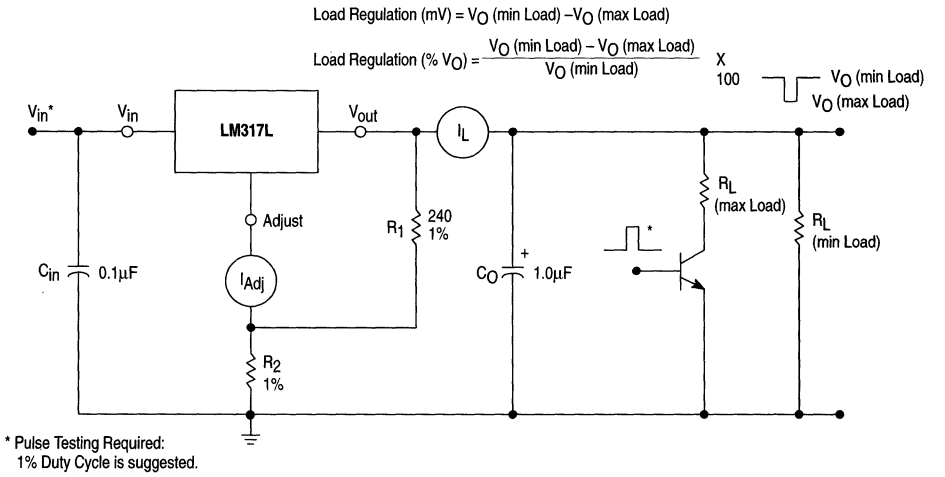
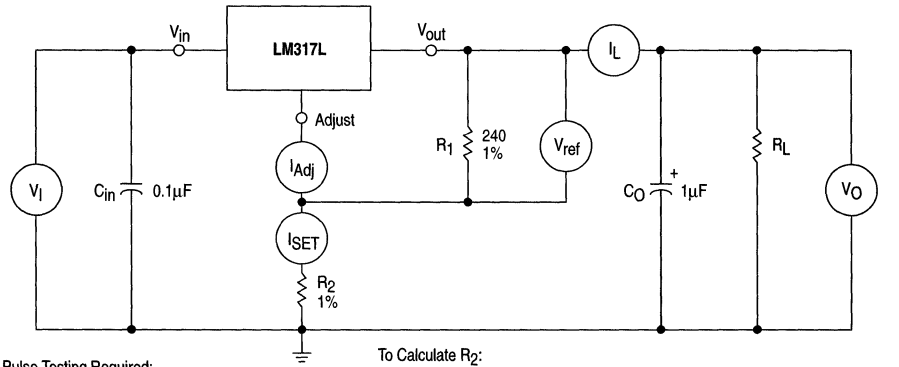


Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit



* Pulse Testing Required:
1% Duty Cycle is suggested.

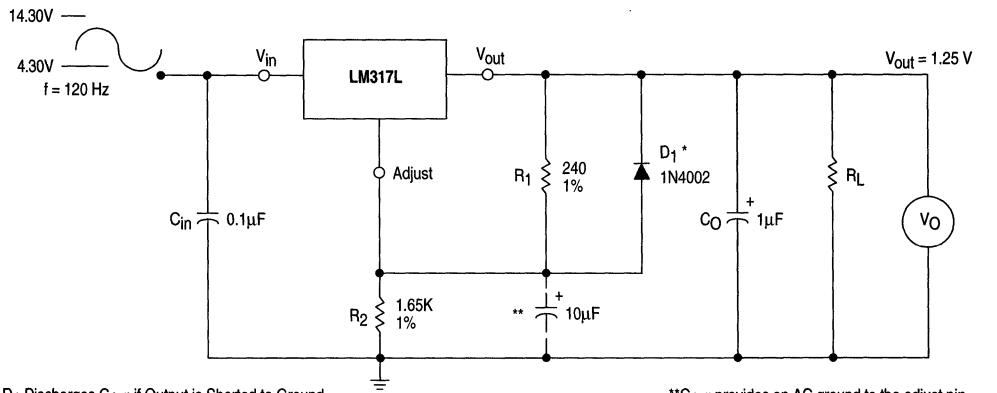
Figure 3. Standard Test Circuit



Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_{out} = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if Output is Shorted to Ground.

**C_{Adj} provides an AC ground to the adjust pin.

Figure 5. Load Regulation

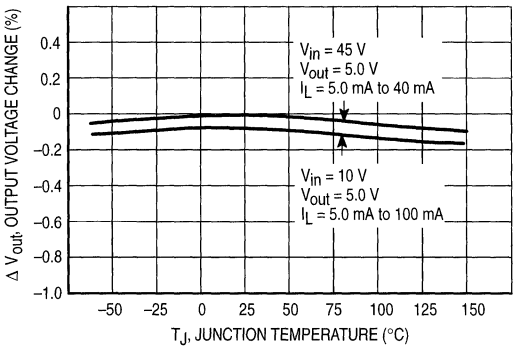


Figure 6. Ripple Rejection

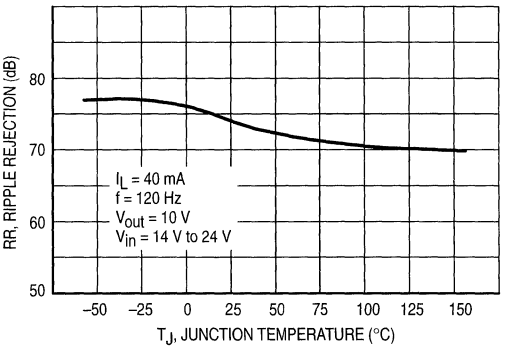


Figure 7. Current Limit

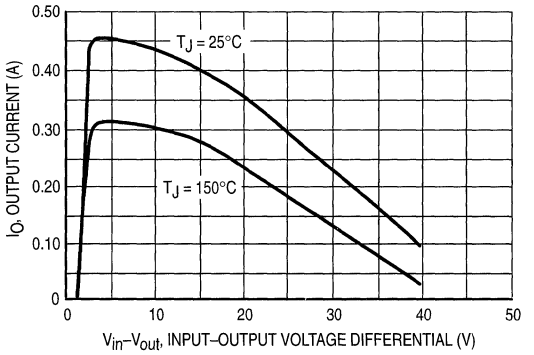


Figure 8. Dropout Voltage

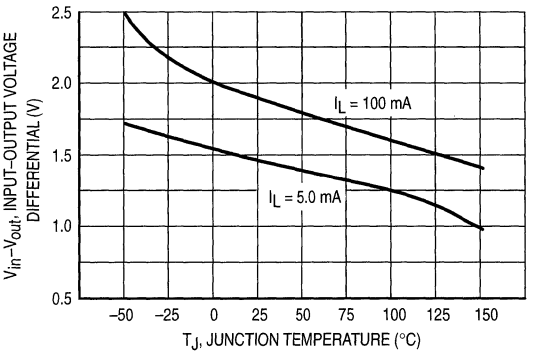


Figure 9. Minimum Operating Current

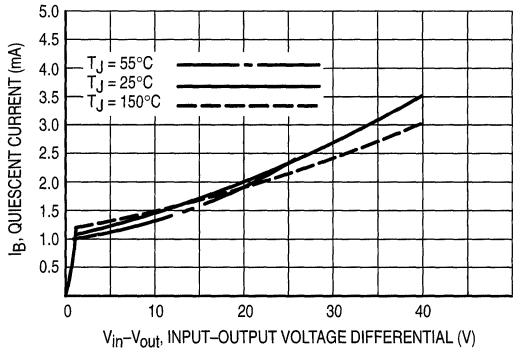


Figure 10. Ripple Rejection versus Frequency

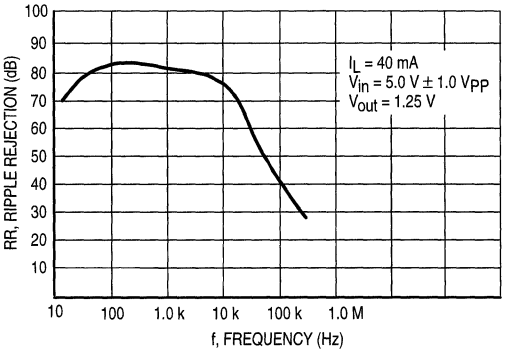


Figure 11. Temperature Stability

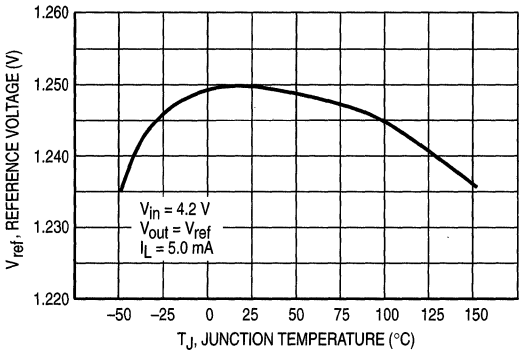


Figure 12. Adjustment Pin Current

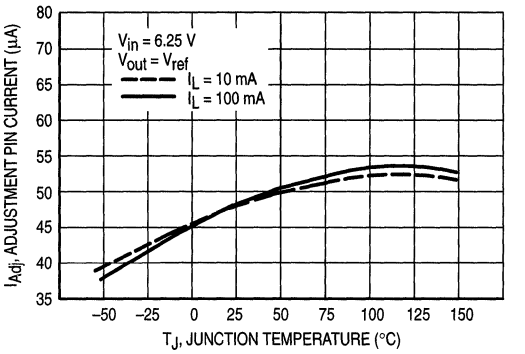


Figure 13. Line Regulation

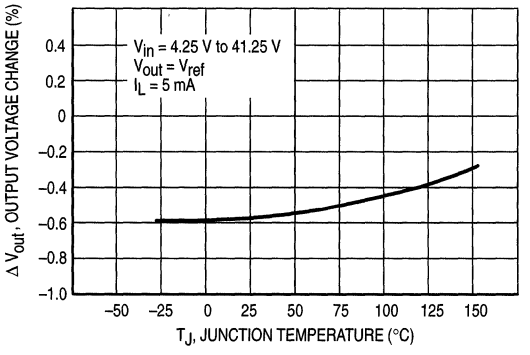


Figure 14. Output Noise

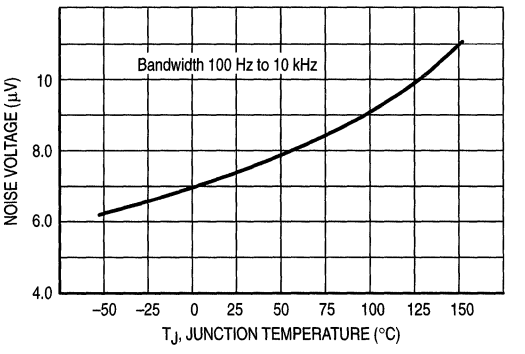


Figure 15. Line Transient Response

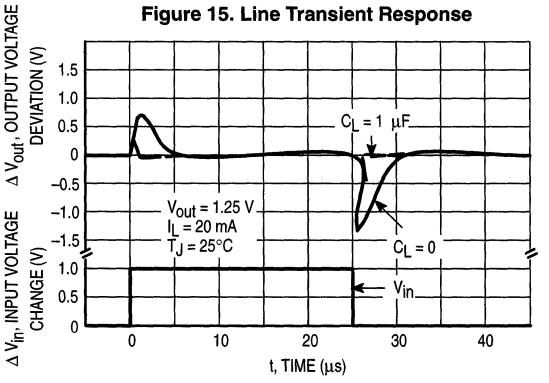
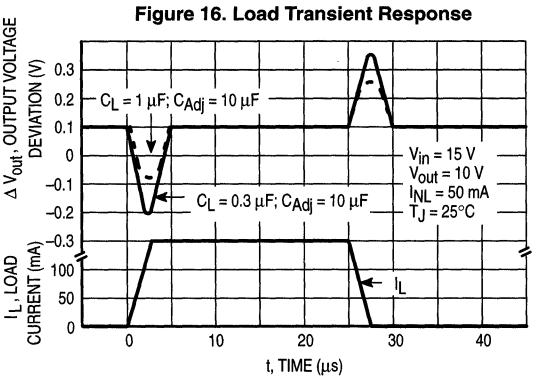


Figure 16. Load Transient Response



APPLICATIONS INFORMATION

Basic Circuit Operation

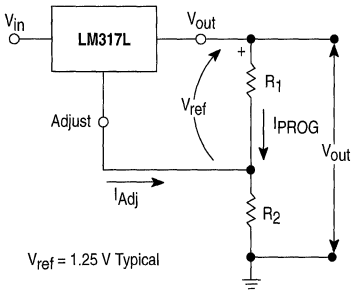
The LM317L is a 3–terminal floating regulator. In operation, the LM317L develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 13), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM317L was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317L is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



Load Regulation

The LM317L is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

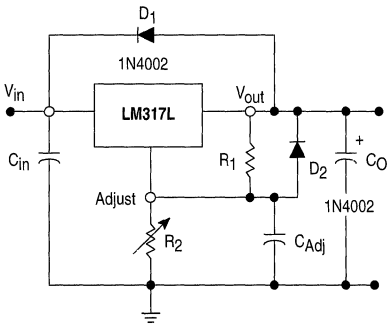
Although the LM317L is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

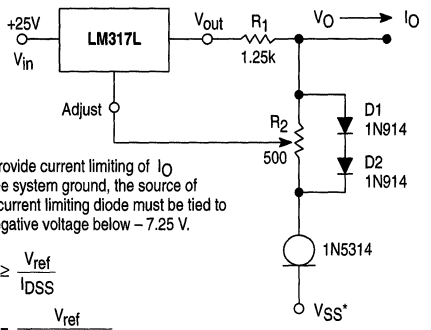
Figure 14 shows the LM317L with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 10 μF, C_{Adj} > 5.0 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes



3

Figure 19. Adjustable Current Limiter



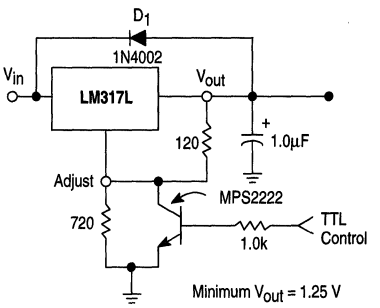
* To provide current limiting of I_O to the system ground, the source of the current limiting diode must be tied to a negative voltage below – 7.25 V.

$$R_2 \geq \frac{V_{ref}}{I_{DSS}}$$

$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

$V_O < P_{OV} + 1.25\ V + V_{SS}$
$I_{Lmin} - I_P < I_O < 100\ mA - I_P$
As shown $O < I_O < 95\ mA$

Figure 20. 5 V Electronic Shutdown Regulator



D_1 protects the device during an input short circuit.

Figure 21. Slow Turn–On Regulator

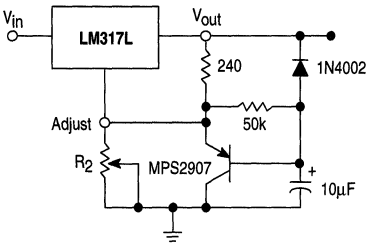
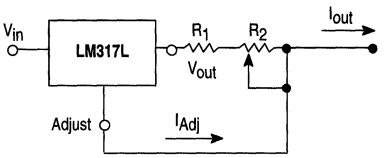


Figure 22. Current Regulator



$$I_{outmax} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj} \cong \frac{1.25\ V}{R_1}$$

$$I_{outmax} = \left(\frac{V_{ref}}{R_1 + R_2}\right) + I_{Adj} \cong \frac{1.25\ V}{R_1 + R_2}$$

$5.0\ mA < I_{out} < 100\ mA$

LM317M

Three-Terminal Adjustable Output Positive Voltage Regulator

MEDIUM CURRENT THREE–TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SEMICONDUCTOR TECHNICAL DATA

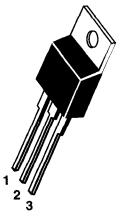
The LM317M is an adjustable three–terminal positive voltage regulator capable of supplying in excess of 500 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof.

The LM317M serves a wide variety of applications including local, on–card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317M can be used as a precision current regulator.

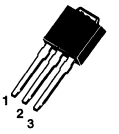
- Output Current in Excess of 500 mA
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Floating Operation for High Voltage Applications
- Eliminates Stocking Many Fixed Voltages

T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface connected to Pin 2



(All 3 Packages)
Pin 1. Adjust
2. V_{out}
3. V_{in}

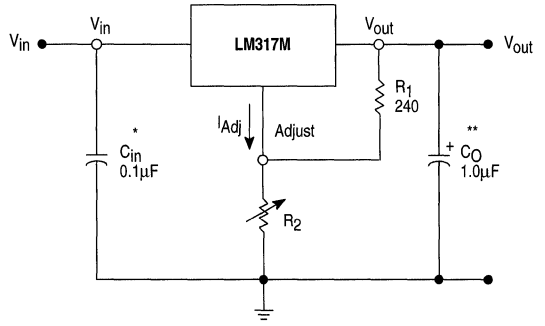


DT–1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)

DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)

Heatsink Surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

Simplified Application



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.
** = C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM317MT	T_J = 0° to +125°C	Plastic Power
LM317MBT#	T_J = –40° to +125°C	Plastic Power
LM317MDT LM317MDT–1	T_J = 0° to 125°C	DPAK

Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input–Output Voltage Differential	V_I–V_O	40	Vdc
Power Dissipation (Package Limitation) (Note 1) Plastic Package, T Suffix T_A = 25°C Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case Plastic Package, DT Suffix T_A = 25°C Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case	 P_D θ_{JA} θ_{JC} P_D θ_{JA} θ_{JC}	 Internally Limited 70 5.0 Internally Limited 92 5.0	 °C/W °C/W °C/W °C/W
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: 1. Figure 23 provides thermal resistance versus pc board pad size.

ELECTRICAL CHARACTERISTICS (V_I–V_O = 5.0 V; I_O = 0.1 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 2) T_A = 25°C, 3.0 V ≤ V_I–V_O ≤ 40 V	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 2) T_A = 25°C, 10 mA ≤ I_O ≤ 0.5 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 – –	 5.0 0.1	 25 0.5	 mV % V_O
Adjustment Pin Current	3	I_{Adj}	–	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ V_I–V_O ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}	1,2	ΔI_{Adj}	–	0.2	5.0	μA
Reference Voltage 3.0 V ≤ V_I–V_O ≤ 40 V, 10 mA ≤ I_O ≤ 0.5 A, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 2) 3.0 V ≤ V_I–V_O ≤ 40 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 2) 10 mA ≤ I_O ≤ 0.5 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 – –	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.7	–	% V_O
Minimum Load Current to Maintain Regulation (V_I–V_O = 40 V)	3	I_{Lmin}	–	3.5	10	mA
Maximum Output Current V_I–V_O ≤ 15 V, P_D ≤ P_{max} V_I–V_O = 40 V, P_D ≤ P_{max}, T_A = 25°C	3	I_{max}	 0.5 0.15	 0.9 0.25	 – –	A
RMS Noise, % of V_O T_A= 25°C, 10 Hz ≤ f ≤ 10 kHz	–	N	–	0.003	–	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 3) Without C_{Adj} C_{Adj} = 10 μF	4	RR	 – 66	 65 80	 – –	dB
Long–Term Stability, T_J = T_{high} (Note 4) T_A= 25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.

NOTES: 1. T_{low} to T_{high} = 0° to +125°C; P_{max} = 7.5 W for LM317M T_{low} to T_{high} = −40° to +125°C; P_{max} = 7.5 W for LM317MB
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
3. C_{Adj}, when used, is connected between the adjustment pin and ground.
4. Since Long–Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

Representative Schematic Diagram

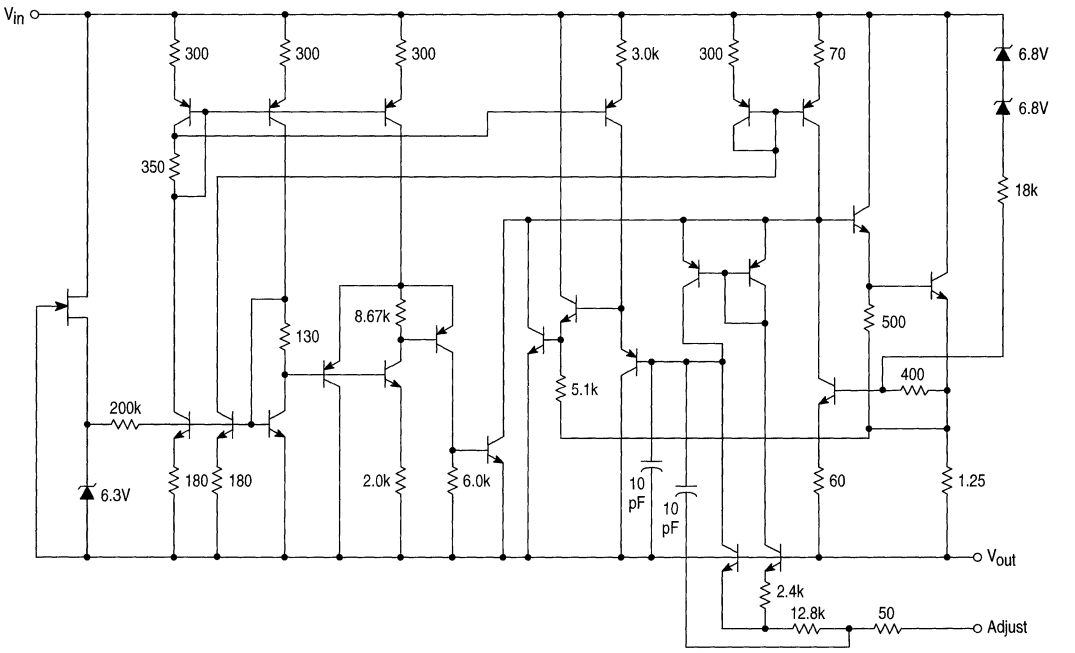


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit

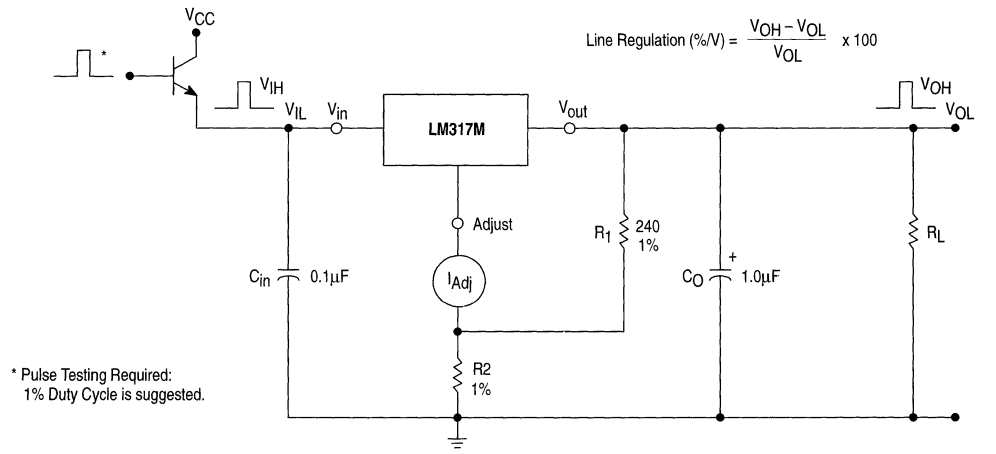
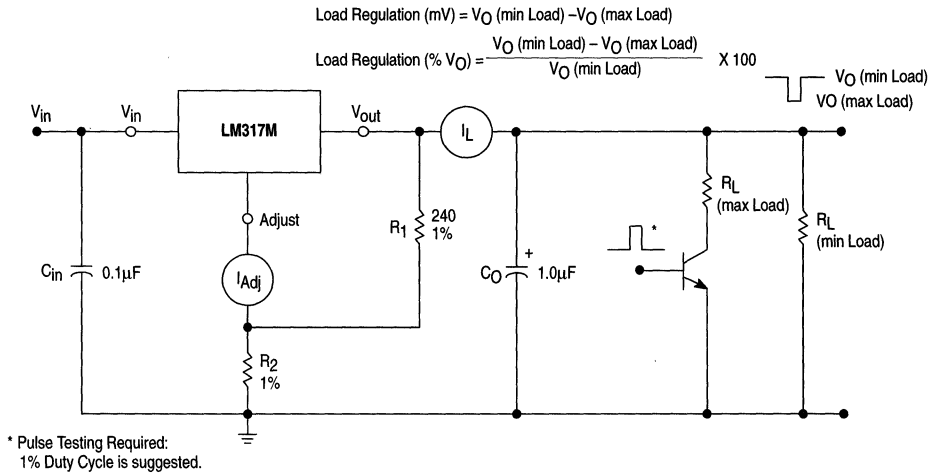
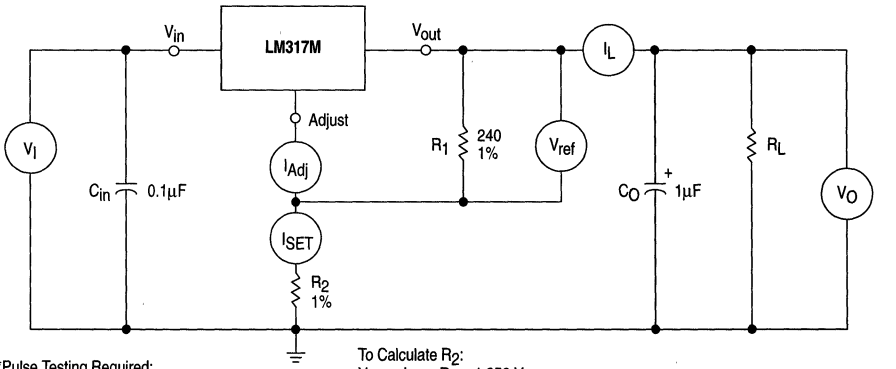


Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit



* Pulse Testing Required:
1% Duty Cycle is suggested.

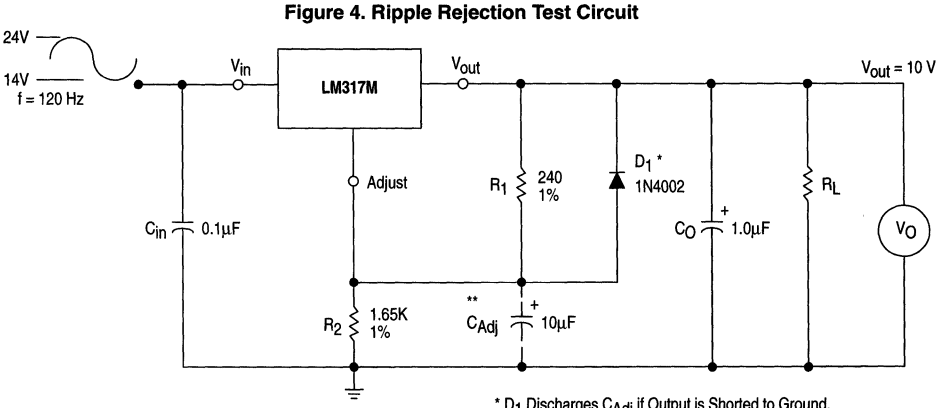
Figure 3. Standard Test Circuit



*Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_{out} = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if Output is Shorted to Ground.
**C_{Adj} provides an AC ground to the adjust pin.

Figure 5. Load Regulation

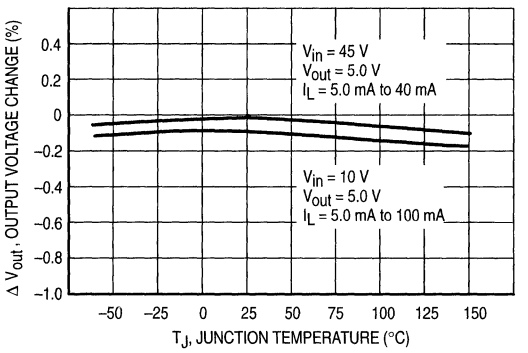


Figure 6. Ripple Rejection

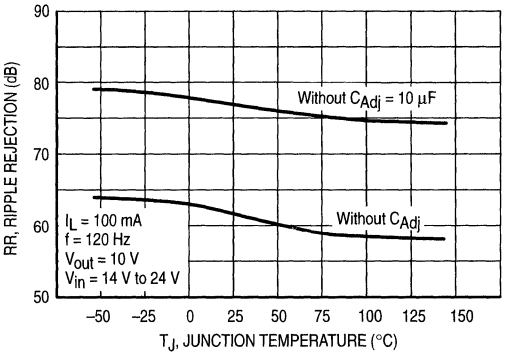


Figure 7. Current Limit

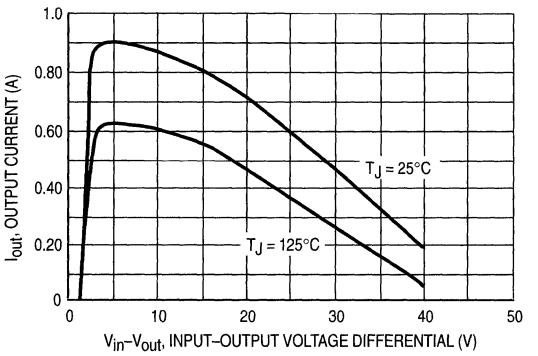


Figure 8. Dropout Voltage

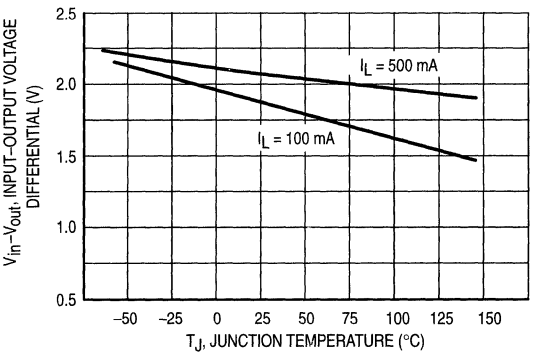


Figure 9. Minimum Operating Current

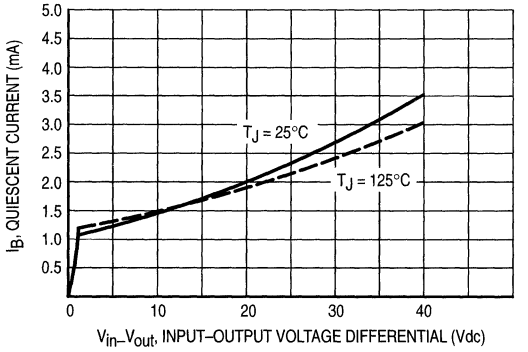


Figure 10. Ripple Rejection versus Frequency

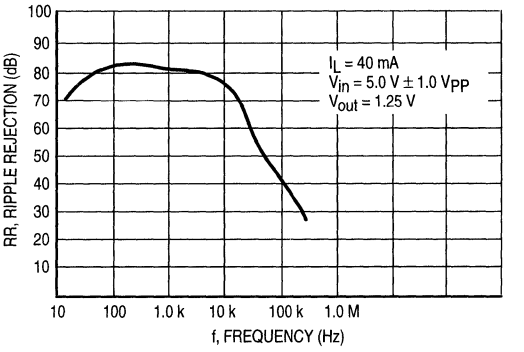


Figure 11. Temperature Stability

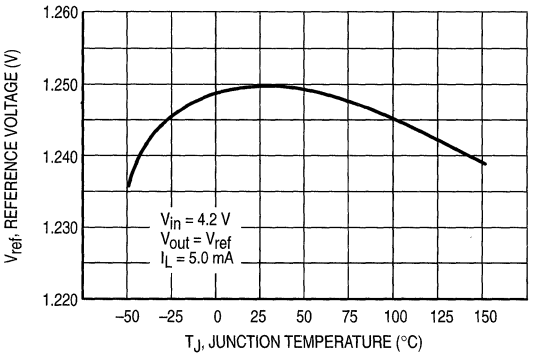


Figure 12. Adjustment Pin Current

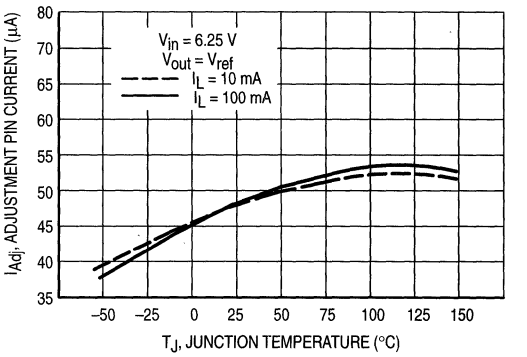


Figure 13. Line Regulation

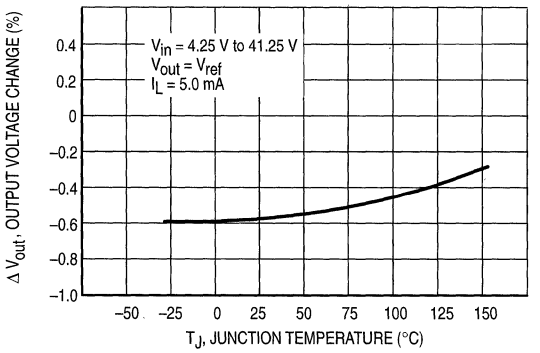


Figure 14. Output Noise

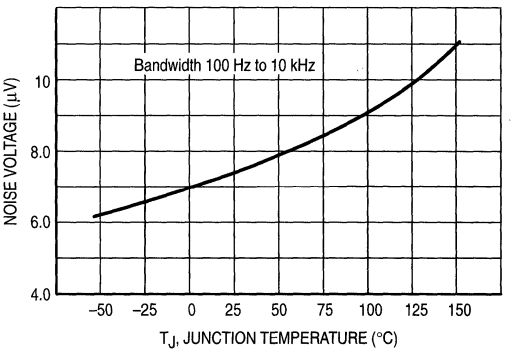


Figure 15. Line Transient Response

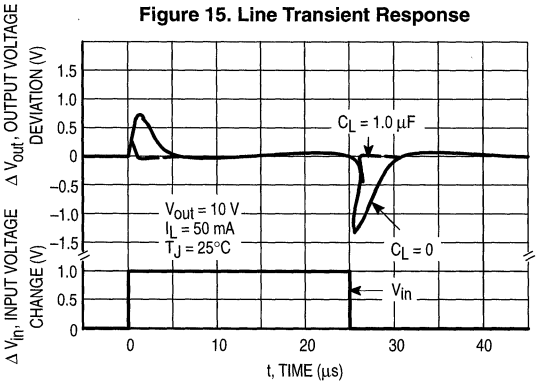
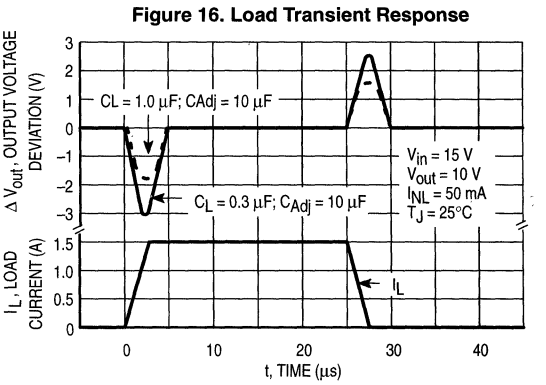


Figure 16. Load Transient Response



APPLICATIONS INFORMATION

Basic Circuit Operation

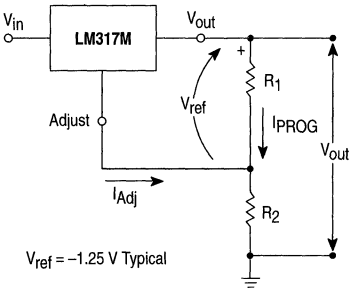
The LM317M is a three–terminal floating regulator. In operation, the LM317M develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}R_2$$

Since the current from the terminal (I_{Adj}) represents an error term in the equation, the LM317M was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317M is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



Load Regulation

The LM317M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317M is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM317M with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 5.0 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

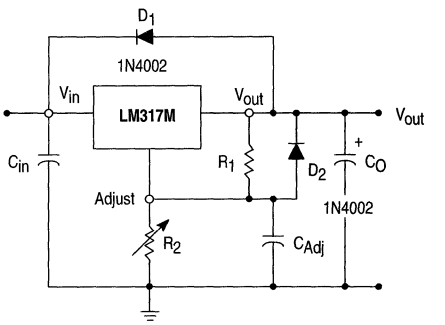
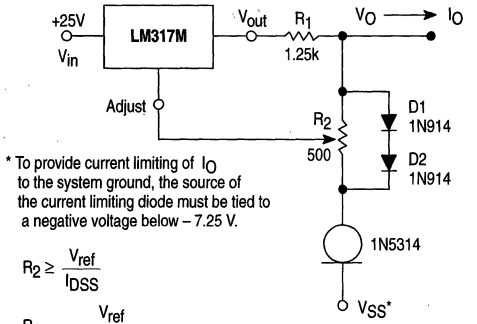


Figure 19. Adjustable Current Limiter



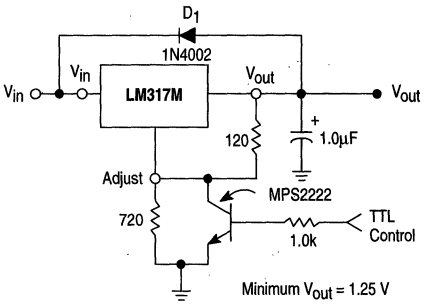
* To provide current limiting of I_O to the system ground, the source of the current limiting diode must be tied to a negative voltage below – 7.25 V.

$$R_2 \geq \frac{V_{ref}}{I_{DSS}}$$

$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

$V_O < P_{OV} + 1.25\ V + V_{SS}$
$I_{Lmin} - I_P < I_O < 500\ mA - I_P$
As shown $O < I_O < 495\ mA$

Figure 20. 5 V Electronic Shutdown Regulator



D_1 protects the device during an input short circuit.

Figure 21. Slow Turn–On Regulator

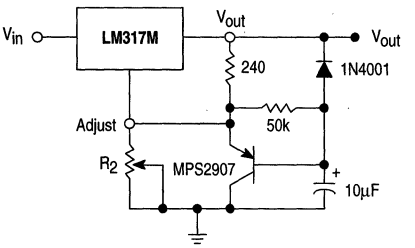
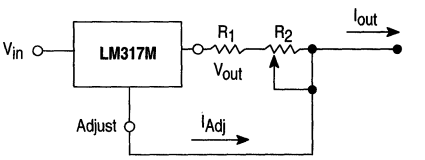


Figure 22. Current Regulator

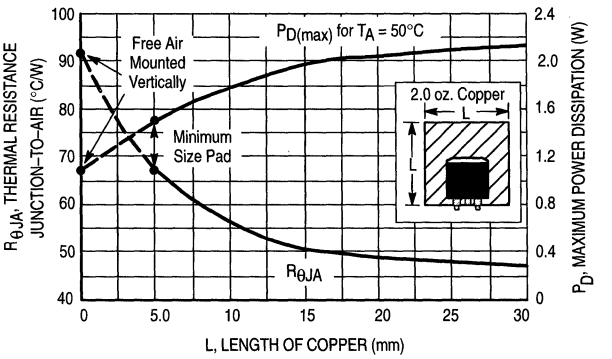


$$I_{outmax} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj} \cong \frac{1.25\ V}{R_1}$$

$$I_{outmax} = \left(\frac{V_{ref}}{R_1 + R_2}\right) + I_{Adj} \cong \frac{1.25\ V}{R_1 + R_2}$$

$5.0\ mA < I_{out} < 100\ mA$

Figure 23. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MOTOROLA

LM323, A

Positive Voltage Regulators

The LM323,A are monolithic integrated circuits which supply a fixed positive 5.0 V output with a load driving capability in excess of 3.0 A. These three–terminal regulators employ internal current limiting, thermal shutdown, and safe–area compensation. The A–suffix is an improved device with superior electrical characteristics and a 2% output voltage tolerance. These regulators are offered with a 0° to +125°C temperature range in a low cost plastic power package.

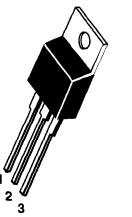
Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. These devices can be used with a series pass transistor to supply up to 15 A at 5.0 V.

- Output Current in Excess of 3.0 A
- Available with 2% Output Voltage Tolerance
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Thermal Regulation and Ripple Rejection Have Specified Limits

3–AMPERE, 5 VOLT POSITIVE VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA

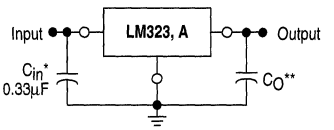
T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Input
2. Ground
3. Output

Heatsink surface is connected to Pin 2.

Simplified Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.5 V above the output voltage even during the low point on the input ripple voltage.

*C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)
**C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Device	Output Voltage Tolerance	Operating Temperature Range	Package
LM323T	4%	T_J = 0° to +125°C	Plastic Power
LM323AT	2%		

MAXIMUM RATINGS

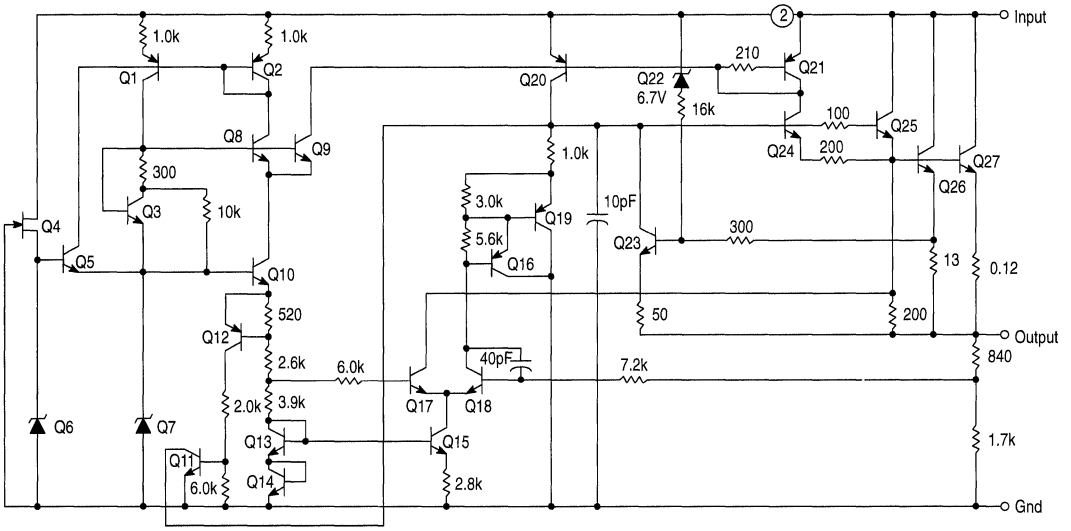
Rating	Symbol	Value	Unit
Input Voltage	V_{in}	20	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Lead Temperature (Soldering, 10 s)	T_{solder}	300	°C

ELECTRICAL CHARACTERISTICS ($T_J = T_{low}$ to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	LM323A			LM323			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C)	V_O	4.9	5.0	5.1	4.8	5.0	5.2	V
Output Voltage (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A, P ≤ P_{max}) (Note 2)	V_O	4.8	5.0	5.2	4.75	5.0	5.25	V
Line Regulation (7.5 V ≤ V_{in} ≤ 15 V, T_J = 25°C) (Note 3)	Reg_{line}	–	1.0	15	–	1.0	25	mV
Load Regulation (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C) (Note 3)	Reg_{load}	–	10	50	–	10	100	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = 25°C)	Reg_{therm}	–	0.001	0.01	–	0.002	0.03	$\%V_O/W$
Quiescent Current (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A)	I_B	–	3.5	10	–	3.5	20	mA
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = 25°C)	V_N	–	40	–	–	40	–	μV_{rms}
Ripple Rejection (8.0 V ≤ V_{in} ≤ 18 V, I_{out} = 2.0A, f = 120 Hz, T_J = 25°C)	RR	66	75	–	62	75	–	dB
Short Circuit Current Limit (V_{in} = 15 V, T_J = 25°C) (V_{in} = 7.5 V, T_J = 25°C)	I_{SC}	– –	4.5 5.5	– –	– –	4.5 5.5	– –	A
Long Term Stability	S	–	–	35	–	–	35	mV
Thermal Resistance, Junction–to–Case (Note 4)	$R_{\Theta JC}$	–	2.0	–	–	2.0	–	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. Although power dissipation is internally limited, specifications apply only for P ≤ P_{max} = 25 W.
3. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1.0 ms and a duty cycle ≤ 5%.
4. Without a heatsink, the thermal resistance ($R_{\Theta JA}$ is 65°C/W). With a heatsink, the effective thermal resistance can approach the specified values of 2.0°C/W, depending on the efficiency of the heatsink.

Representative Schematic Diagram



VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical LM323A to a 20 W input pulse. The variation of the output voltage due to line regulation is labeled À and the thermal regulation component is labeled Á. Figure 2 shows the load and thermal regulation response of a typical LM323A to a 20 W load pulse. The output voltage variation due to load regulation is labeled À and the thermal regulation component is labeled Á.

Figure 1. Line and Thermal Regulation

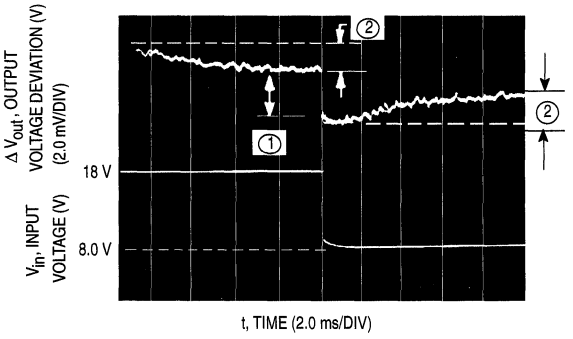


Figure 2. Load and Thermal Regulation

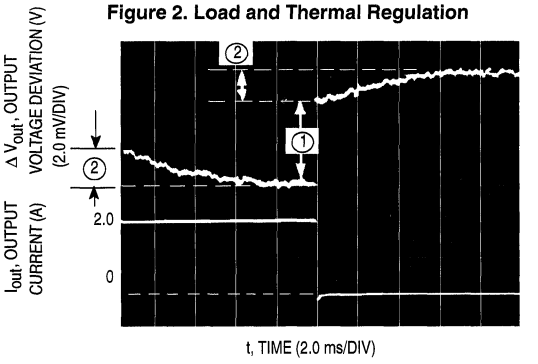


Figure 3. Temperature Stability

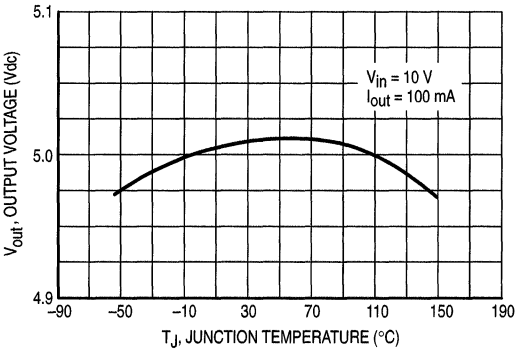


Figure 4. Output Impedance

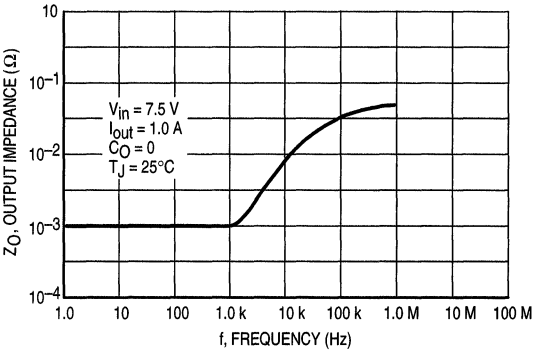


Figure 5. Ripple Rejection versus Frequency

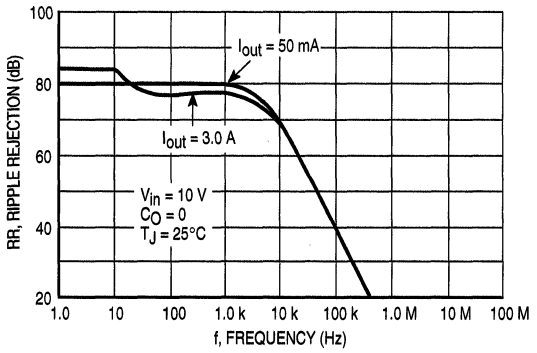


Figure 6. Ripple Rejection versus Output Current

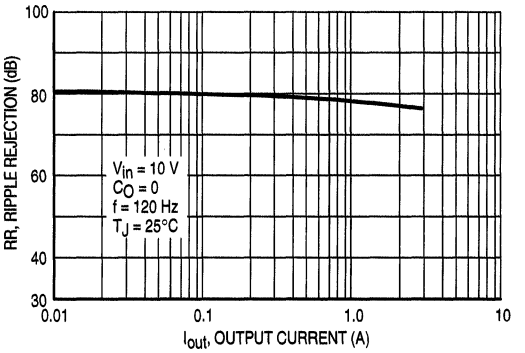


Figure 7. Quiescent Current versus Input Voltage

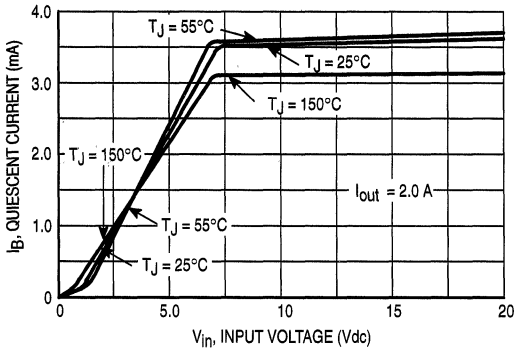


Figure 8. Quiescent Current versus Output Current

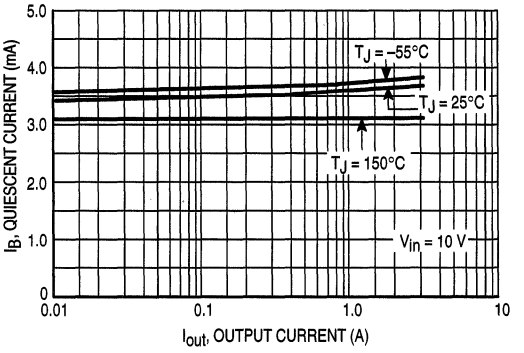


Figure 9. Dropout Voltage

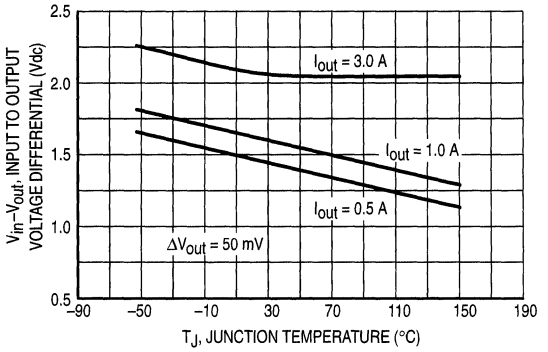


Figure 10. Short Circuit Current

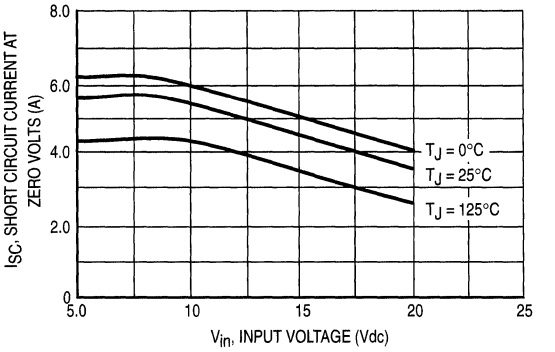


Figure 11. Line Transient Response

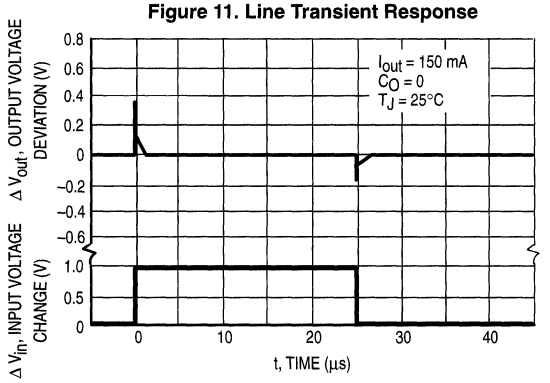
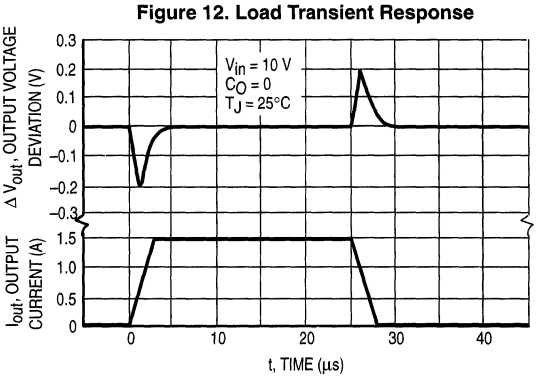


Figure 12. Load Transient Response



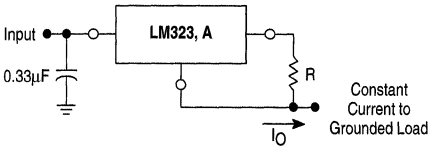
APPLICATIONS INFORMATION

Design Considerations

The LM323,A series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 13. Current Regulator



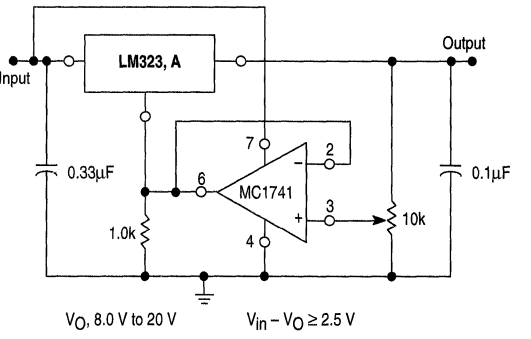
The LM323,A regulator can also be used as a current source when connected as above. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

$\Delta I_B \cong 0.7$ mA over line, load and temperature changes
$I_B \cong 3.5$ mA

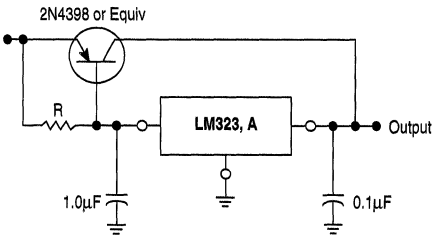
For example, a 2.0 A current source would require R to be a 2.5 Ω, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 V.

Figure 14. Adjustable Output Regulator



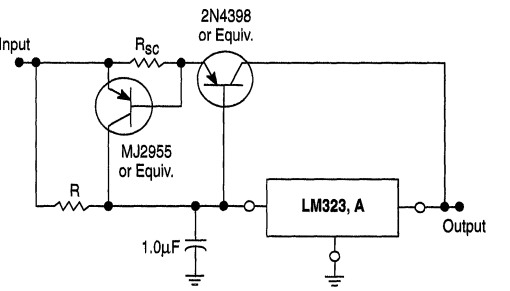
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 V greater than the regulator voltage.

Figure 15. Current Boost Regulator



The LM323, A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 A. Resistor R in conjuction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input–output differential voltage minimum is increased by the V_{BE} of the pass transistor.

Figure 16. Current Boost with Short Circuit Protection



The circuit of Figure 16 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three–terminal regulator. Therefore, an 8.0 A power transistor is specified.

LM337

Three-Terminal Adjustable Output Negative Voltage Regulator

The LM337 is an adjustable 3–terminal negative voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of –1.2 V to –37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof.

The LM337 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM337 can be used as a precision current regulator.

- Output Current in Excess of 1.5 A
- Output Adjustable between –1.2 V and –37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe–Area Compensation
- Floating Operation for High Voltage Applications
- Eliminates Stocking many Fixed Voltages
- Available in Surface Mount D²PAK and Standard 3–Lead Transistor Package

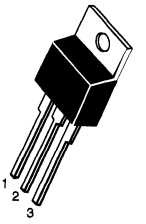
THREE–TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

SEMICONDUCTOR TECHNICAL DATA

3

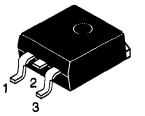
T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface connected to Pin 2.



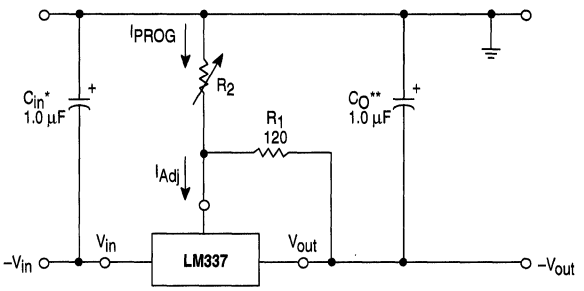
Pin 1. Adjust
2. V_{in}
3. V_{out}

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D²PAK)



Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

Standard Application



*C_{in} is required if regulator is located more than 4 inches from power supply filter. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommended.

**C_O is necessary for stability. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommeded.

$$V_{out} = -1.25\ V\left(1 + \frac{R_2}{R_1}\right)$$

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM337BD2T	$T_J = -40°$ to $+125°C$	Surface Mount
LM337BT		Insertion Mount
LM337D2T	$T_J = 0°$ to $+125°C$	Surface Mount
LM337T		Insertion Mount

MAXIMUM RATINGS

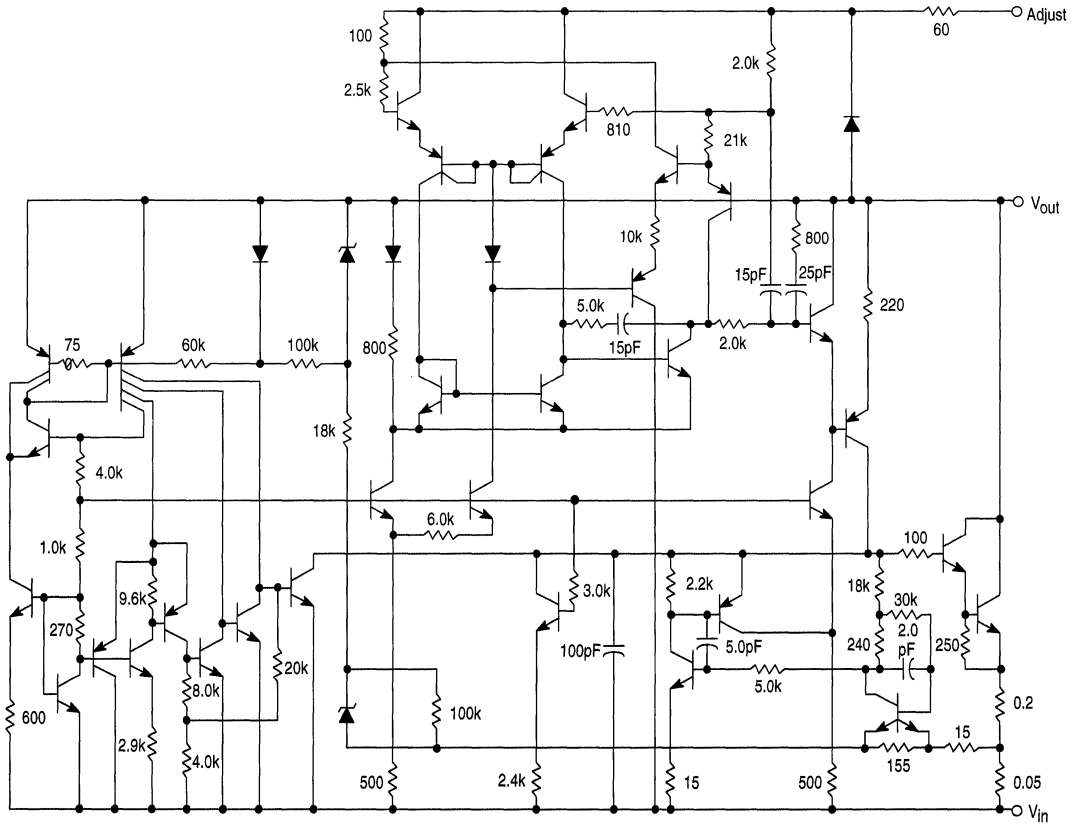
Rating	Symbol	Value	Unit
Input–Output Voltage Differential	$V_I–V_O$	40	Vdc
Power Dissipation			
Case 221A			
T_A = +25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	65	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Case 936 (D^2PAK)			
T_A = +25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	70	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS ($|V_I–V_O|$ = 5.0 V; I_O = 0.5 A for T package; $T_J = T_{low}$ to T_{high} [Note 1]; I_{max} and P_{max} [Note 2].)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3), T_A = +25°C, 3.0 V ≤ $\|V_I–V_O\|$ ≤ 40 V	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 3), T_A = +25°C, 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}				
$\|V_O\|$ ≤ 5.0 V			–	15	50	mV
$\|V_O\|$ ≥ 5.0 V			–	0.3	1.0	% V_O
Thermal Regulation, T_A = +25°C (Note 6), 10 ms Pulse		Reg_{therm}	–	0.003	0.04	% V_O/W
Adjustment Pin Current	3	I_{Adj}	–	65	100	µA
Adjustment Pin Current Change, 2.5 V ≤ $\|V_I–V_O\|$ ≤ 40 V, 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}, T_A = +25°C	1, 2	ΔI_{Adj}	–	2.0	5.0	µA
Reference Voltage, T_A = +25°C, 3.0 V ≤ $\|V_I–V_O\|$ ≤ 40 V, 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}, $T_J = T_{low}$ to T_{high}	3	V_{ref}	−1.213 −1.20	−1.250 −1.25	−1.287 −1.30	V
Line Regulation (Note 3), 3.0 V ≤ $\|V_I–V_O\|$ ≤ 40 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 3), 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}				
$\|V_O\|$ ≤ 5.0 V			–	20	70	mV
$\|V_O\|$ ≥ 5.0 V			–	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.6	–	% V_O
Minimum Load Current to Maintain Regulation	3	I_{Lmin}				mA
($\|V_I–V_O\|$ ≤ 10 V)			–	1.5	6.0	
($\|V_I–V_O\|$ ≤ 40 V)			–	2.5	10	
Maximum Output Current	3	I_{max}				A
$\|V_I–V_O\|$ ≤ 15 V, P_D ≤ P_{max}, T Package			–	1.5	2.2	
$\|V_I–V_O\|$ ≤ 40 V, P_D ≤ P_{max}, T_J = +25°C, T Package			–	0.15	0.4	
RMS Noise, % of V_O, T_A = +25°C, 10 Hz ≤ f ≤ 10 kHz		N	–	0.003	–	% V_O
Ripple Rejection, V_O = −10 V, f = 120 Hz (Note 4)	4	RR				dB
Without C_{Adj}			–	60	–	
C_{Adj} = 10 µF			66	77	–	
Long–Term Stability, $T_J = T_{high}$ (Note 5), T_A = +25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction–to–Case, T Package		$R_{\theta JC}$	–	4.0	–	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C, for LM337T, D2T. T_{low} to T_{high} = −40° to +125°C, for LM337BT, BD2T.
2. I_{max} = 1.5 A, P_{max} = 20 W
3. Load and line regulation are specified at constant junction temperature. Change in V_O because of heating effects is covered under the Thermal Regulation specification. Pulse testing with a low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Power dissipation within an IC voltage regulator produces a temperature gradient on the die, affecting individual IC components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.

Representative Schematic Diagram



This device contains 39 active transistors.

Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit

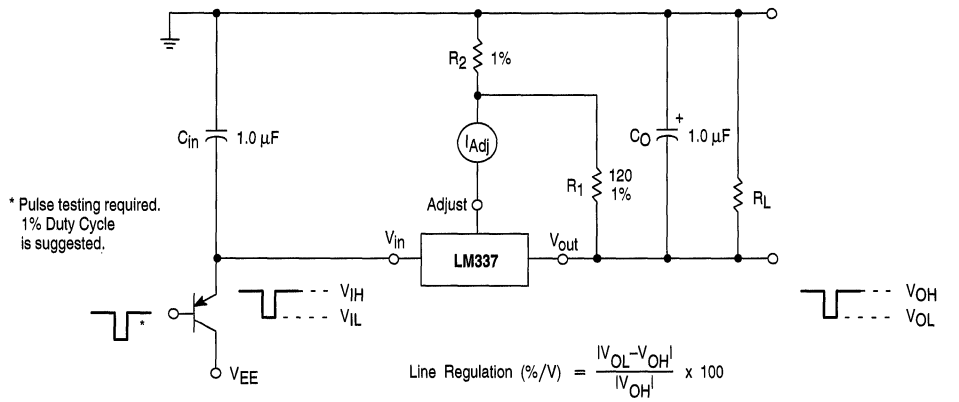
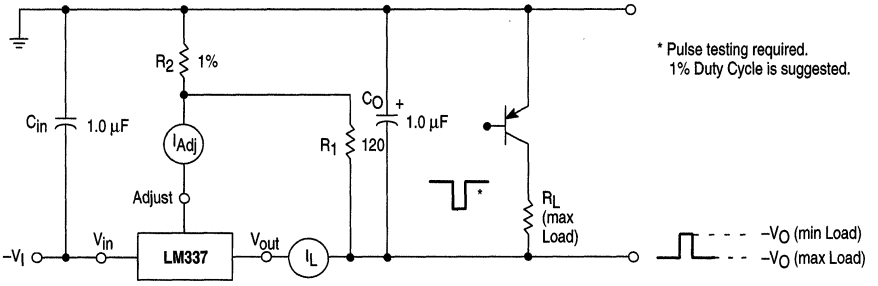


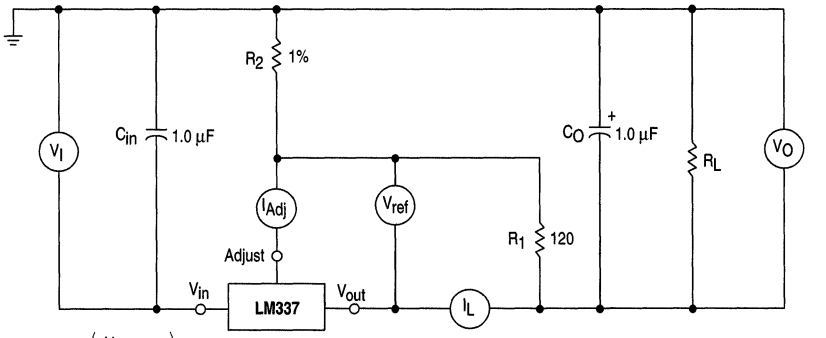
Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit



Load Regulation (mV) = V_O (min Load) – V_O (max Load)

Load Regulation (% V_O) = $\frac{V_O \text{ (min Load)} - V_O \text{ (max Load)}}{V_O \text{ (min Load)}}$ x 100

Figure 3. Standard Test Circuit

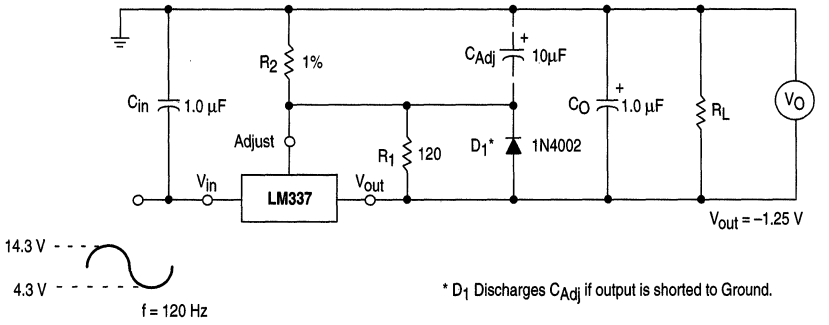


To Calculate R_2: $R_2 = \left(\frac{V_O}{V_{ref}} - 1\right) R_1$

This assumes I_{Adj} is negligible.

* Pulse testing required.
1% Duty Cycle is suggested.

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if output is shorted to Ground.

Figure 5. Load Regulation

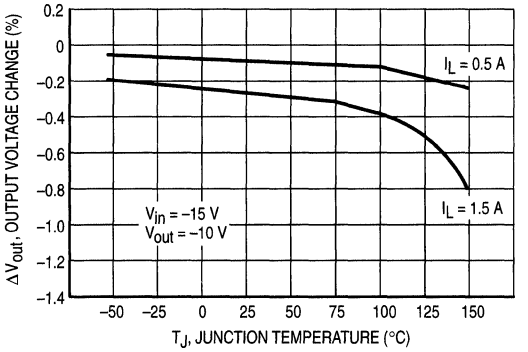


Figure 6. Current Limit

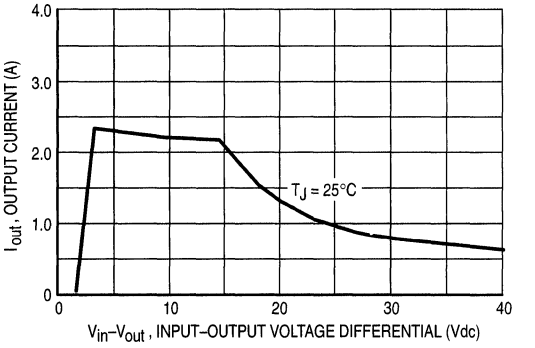


Figure 7. Adjustment Pin Current

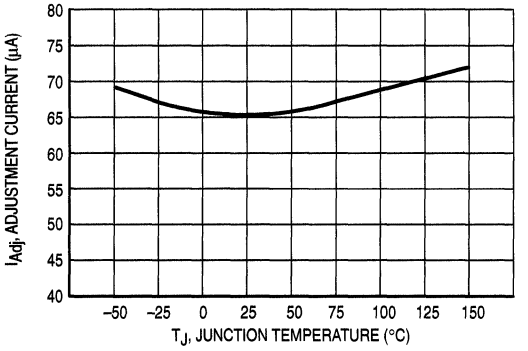


Figure 8. Dropout Voltage

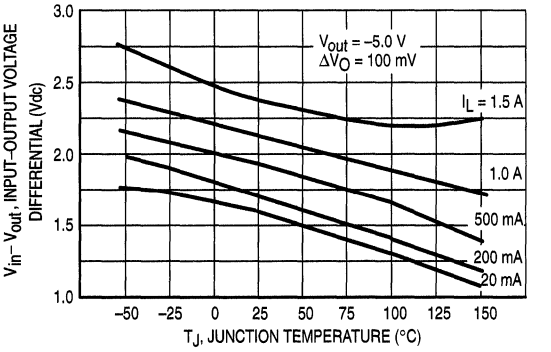


Figure 9. Temperature Stability

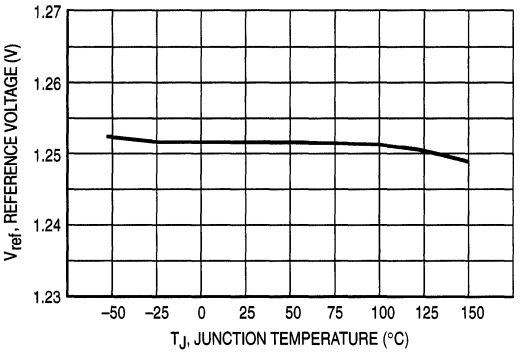


Figure 10. Minimum Operating Current

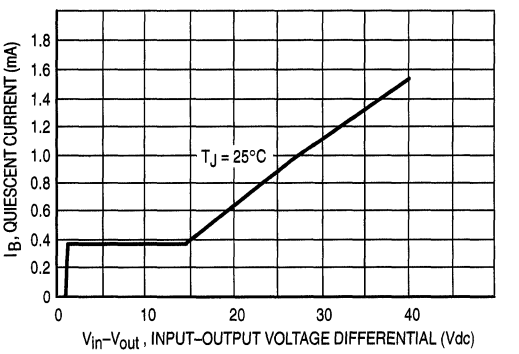


Figure 11. Ripple Rejection versus Output Voltage

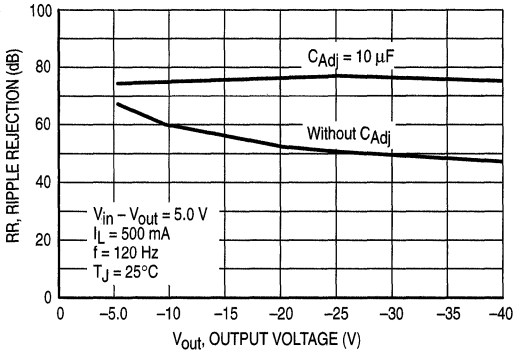


Figure 12. Ripple Rejection versus Output Current

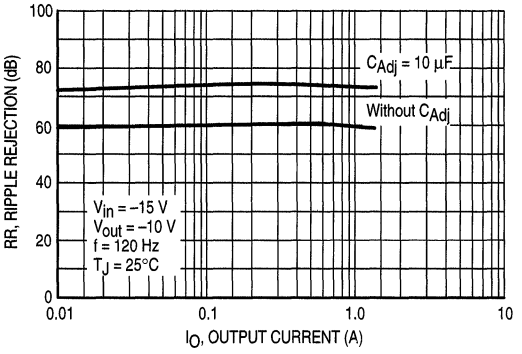


Figure 13. Ripple Rejection versus Frequency

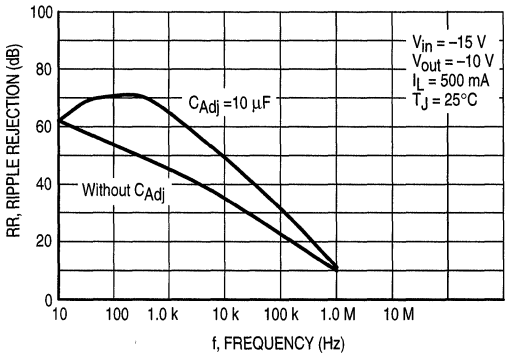


Figure 14. Output Impedance

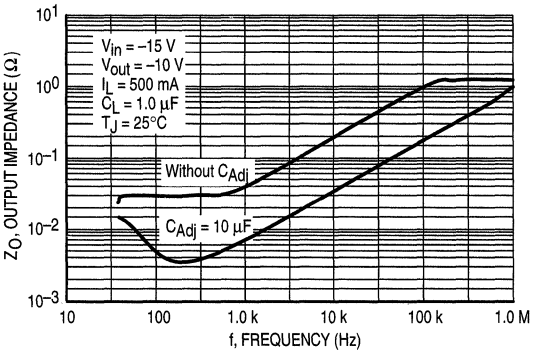


Figure 15. Line Transient Response

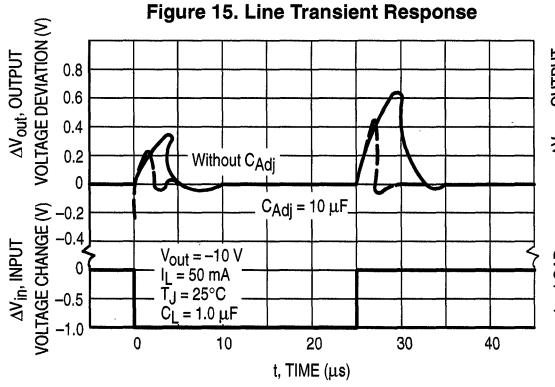
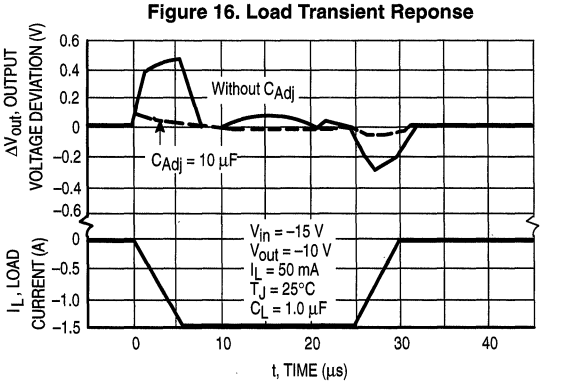


Figure 16. Load Transient Reponse



APPLICATIONS INFORMATION

Basic Circuit Operation

The LM337 is a 3–terminal floating regulator. In operation, the LM337 develops and maintains a nominal –1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 from ground.

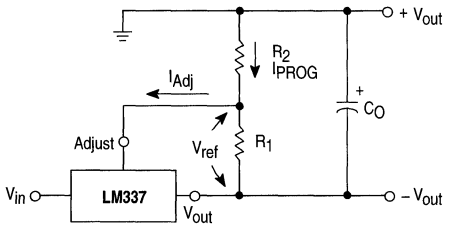
The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

Since the current into the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM337 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM337 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



V_{ref} = –1.25 V Typical

Load Regulation

The LM337 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

An output capacitance (C_O) in the form of a 1.0 μF tantalum or 10 μF aluminum electrolytic capacitor is required for stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM337 with the recommended protection diodes for output voltages in excess of –25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 10 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from the discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

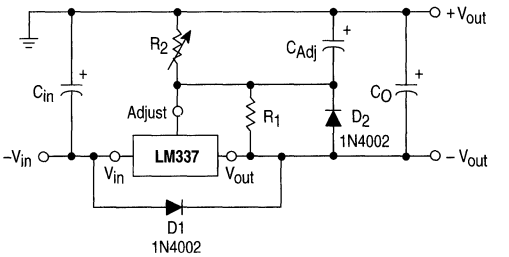
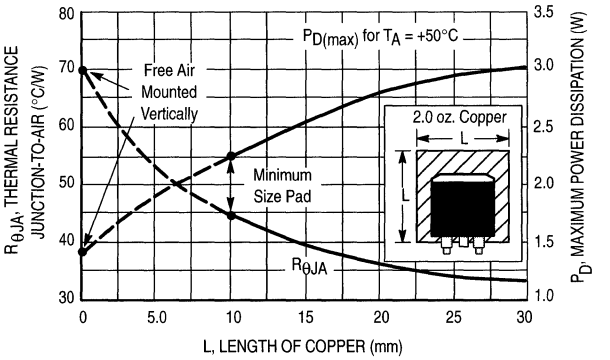


Figure 19. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



LM337M

3

Three-Terminal Adjustable Output Negative Voltage Regulator

The LM337M is an adjustable three–terminal negative voltage regulator capable of supplying in excess of 500 mA over an output voltage range of –1.2 V to –37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof.

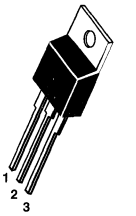
The LM337M serves a wide variety of applications including local, on–card regulation. This device can also be used to make a programmable output regulator or by connecting a fixed resistor between the adjustment and output. The LM337M can be used as a precision current regulator.

- Output Current in Excess of 500 mA
- Output Adjustable Between –1.2 V and –37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3–Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

MEDIUM CURRENT THREE–TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

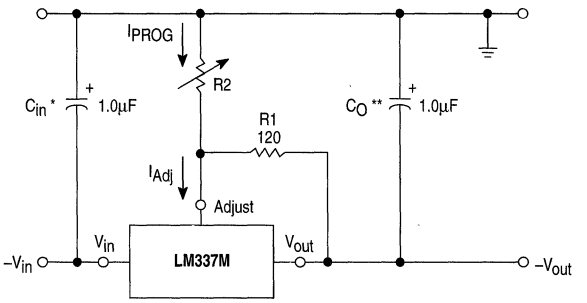
SEMICONDUCTOR TECHNICAL DATA

T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Adjust
2. V_{in}
3. V_{out}

Standard Application



*C_{in} is required if regulator is located more than 4″ from power supply filter. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommended.
**C_O is necessary for stability. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommeded.

$$V_{out} = -1.25\ V\left(1 + \frac{R2}{R1}\right)$$

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM337MT	T_J = 0° to +125°C	Plastic Power

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input–Output Voltage Differential	V_I–V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS ($|V_I - V_O| = 5.0$ V, $I_O = 0.1$; $T_J = T_{low}$ to T_{high} [Note 1], P_{max} per Note 2, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ $\|V_I$–$V_O\|$ ≤ 40 V	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ 0.5 A $\|V_O\|$ ≤ 5.0V $\|V_O\|$ ≥ 5.0V	2	Reg_{load}	 – –	 15 0.3	 15 1.0	 mV %/V_O
Thermal Regulation 10 ms Pulse, T_A = 25°C	–	Reg_{therm}	–	0.03	0.04	% V_O/W
Adjustment Pin Current	3	I_{Adj}	–	65	100	µA
Adjustment Pin Current Change 2.5 V ≤ $\|V_I$–$V_O\|$ ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}, T_A = 25°C	1, 2	ΔI_{Adj}	–	2.0	5.0	µA
Reference Voltage 3.0 V ≤ $\|V_I$–$V_O\|$ ≤ 40 V, 10 mA ≤ I_O ≤ 0.5 A, P_D ≤ P_{max}, T_A = 25°C T_{low} to T_{high}	3	V_{ref}	 –1.213 –1.20	 –1.250 –1.25	 –1.287 –1.30	V
Line Regulation (Note 3) 3.0 V ≤ $\|V_I$–$V_O\|$ ≤ 40 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ 0.5 A $\|V_O\|$ ≤ 5.0 V $\|V_O\|$ ≥ 5.0 V	2	Reg_{load}	 – –	 20 0.3	 70 1.5	mV %/V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.6	–	%/V_O
Minimum Load Current to Maintain Regulation ($\|V_I$–$V_O\|$ ≤ 10 V) ($\|V_I$–$V_O\|$ ≤ 40 V)	3	I_{Lmin}	 – –	 1.5 2.5	 6.0 10	mA
Maximum Output Current $\|V_I$–$V_O\|$ ≤ 15 V, P_D ≤ P_{max} $\|V_I$–$V_O\|$ ≤ 40 V, P_D ≤ P_{max}, T_J = 25°C	3	I_{max}	 0.5 0.1	 0.9 0.25	 – –	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	–	N	–	0.003	–	%/V_O
Ripple Rejection, V_O = –10 V, f = 120 Hz (Note 4) Without C_{Adj} C_{Adj} = 10 µF	4	RR	 – 66	 60 77	 – –	dB
Long Term Stability, $T_J = T_{high}$ (Note 5) T_A = 25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs
Thermal Resistance, Junction–to–Case	–	$R_{\Theta JC}$	–	7.0	–	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. P_{max} = 7.5 W
3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

3

Schematic Diagram

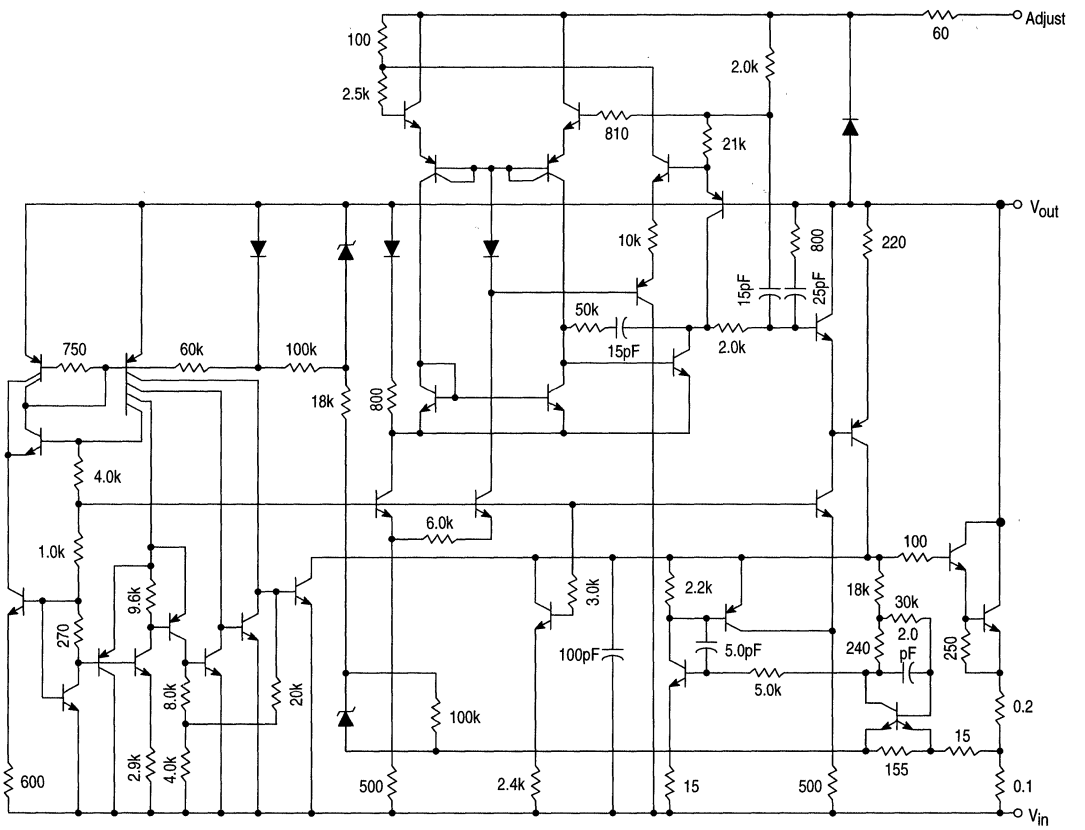


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit

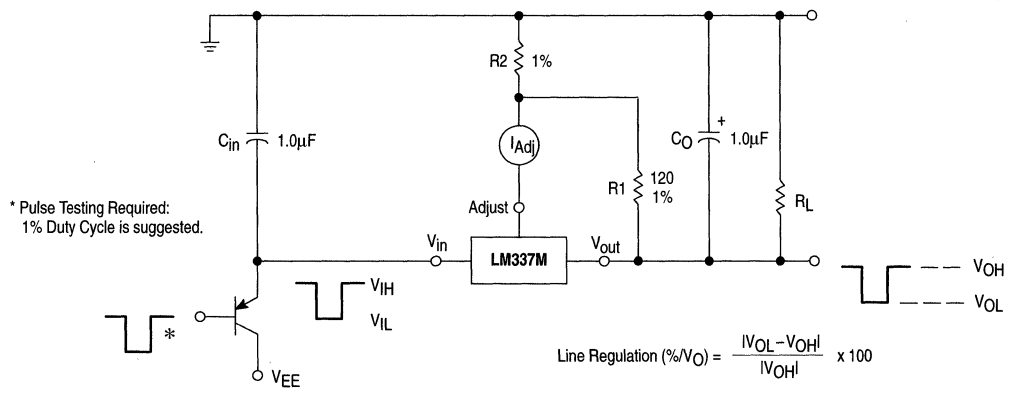
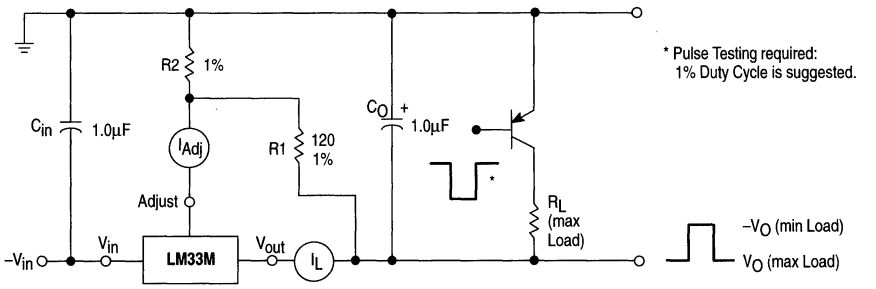


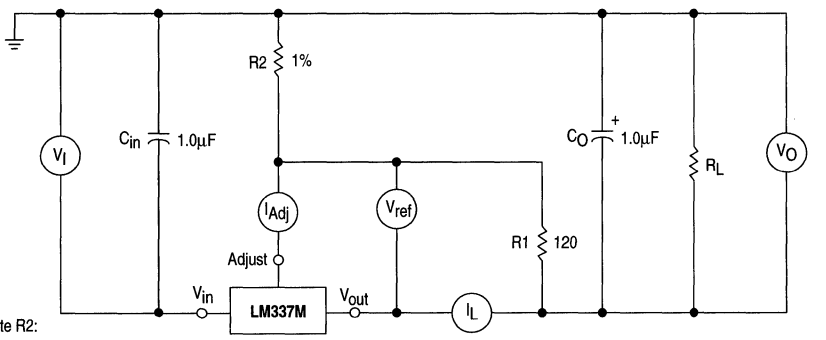
Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit



Load Regulation (mV) = V_O (min Load) – V_O (max Load)

Load Regulation (%/V_O) = $\frac{V_O \text{ (min Load)} - V_O \text{(max Load)}}{V_O \text{ (min Load)}}$ x 100

Figure 3. Standard Test Circuit



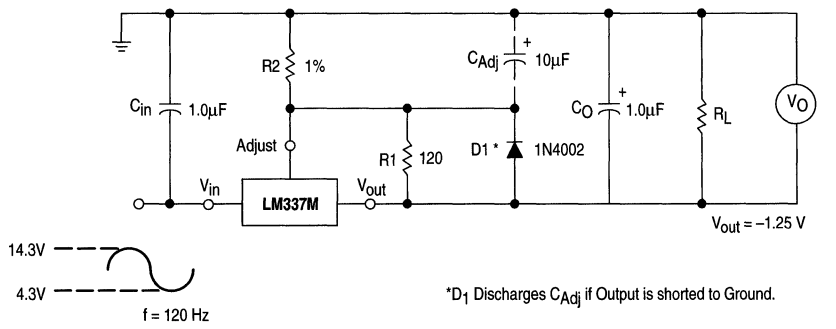
To Calculate R2:

$$R2 = \left(\frac{V_O}{V_{ref}} - 1\right) R_1$$

This assumes I_{Adj} is negligible.

Pulse Testing Required: 1% Duty Cycle is suggested.

Figure 4. Ripple Rejection Test Circuit



*D_1 Discharges C_{Adj} if Output is shorted to Ground.

Figure 5. Load Regulation

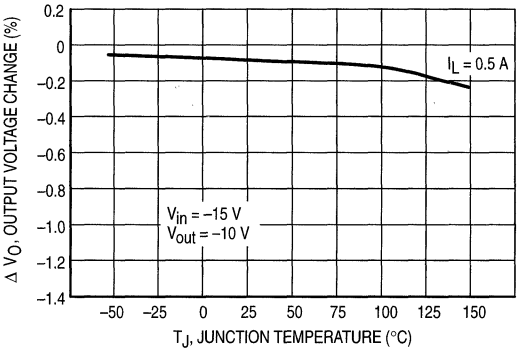


Figure 6. Current Limit

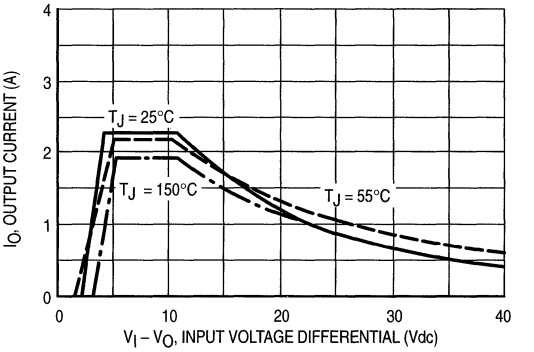


Figure 7. Adjustment Pin Current

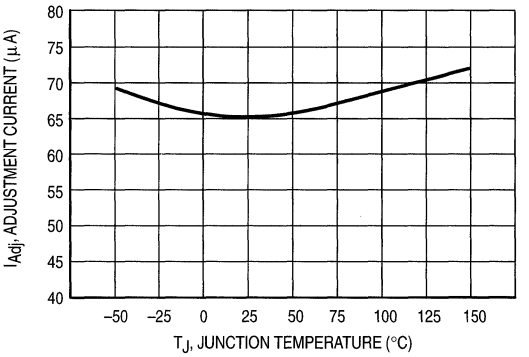


Figure 8. Dropout Voltage

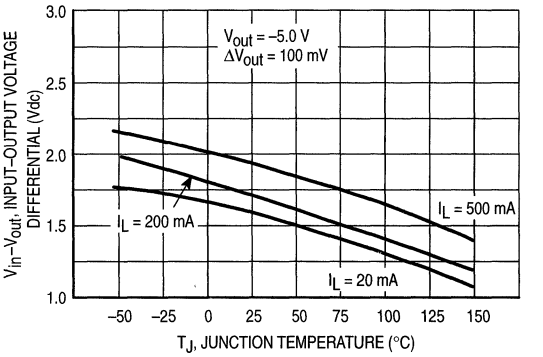


Figure 9. Temperature Stability

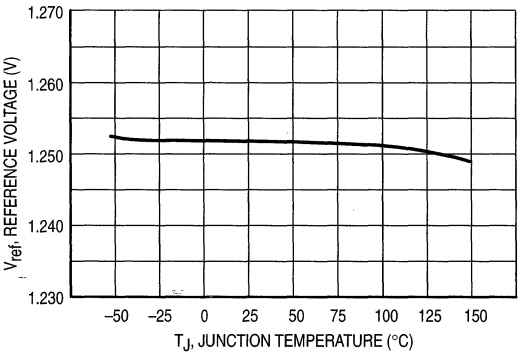


Figure 10. Minimum Operating Current

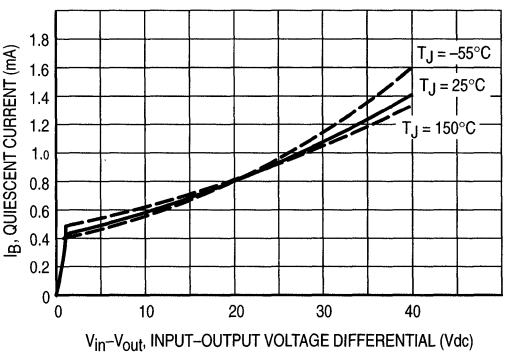


Figure 11. Ripple Rejection versus Output Voltage

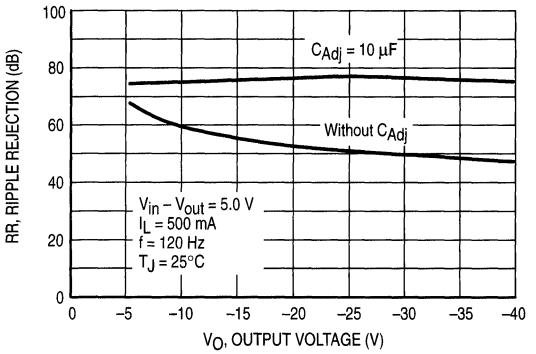


Figure 12. Ripple Rejection versus Output Current

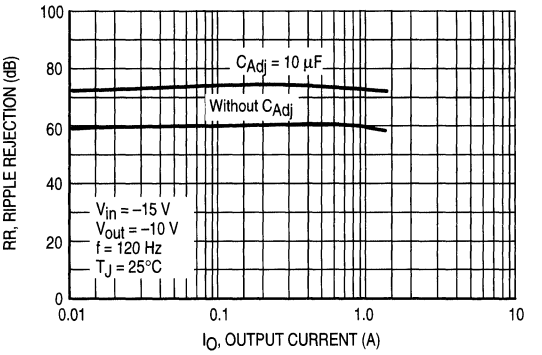


Figure 13. Ripple Rejection versus Frequency

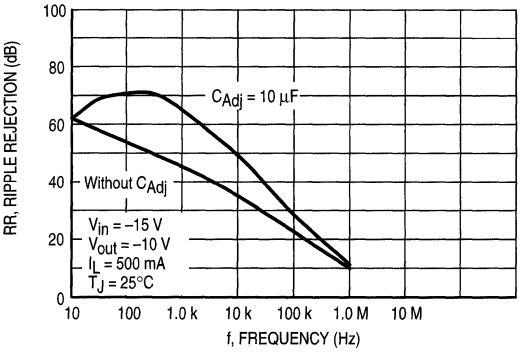


Figure 14. Output Impedance

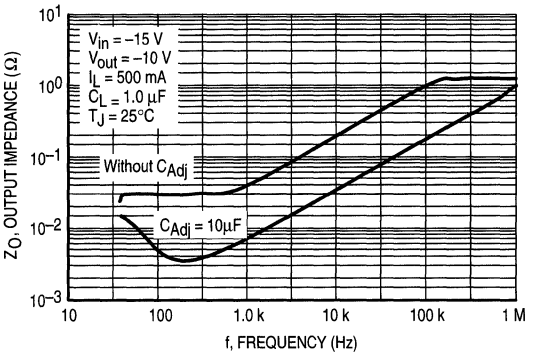


Figure 15. Line Transient Response

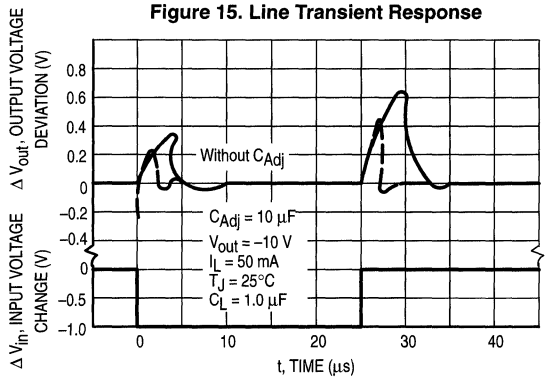
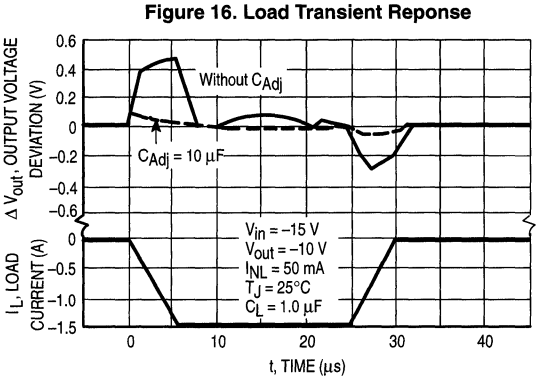


Figure 16. Load Transient Reponse



APPLICATIONS INFORMATION

Basic Circuit Operation

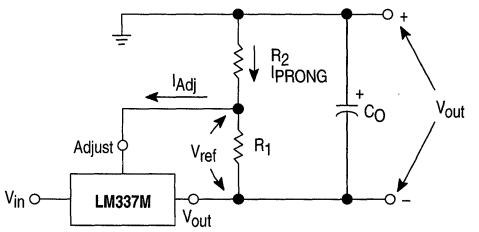
The LM337M is a three–terminal floating regulator. In operation, the LM337M develops and maintains a nominal –1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

Since the current into the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM337M was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM337M is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



V_{ref} = –1.25 V Typically

Load Regulation

The LM337M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

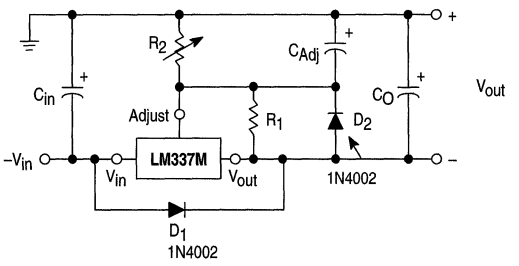
An output capacitance (C_O) in the form of a 1.0 μF tantalum or 10 μF aluminum electrolytic capacitor is required for stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM337M with the recommended protection diodes for output voltages in excess of –25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 10 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes



MOTOROLA

LM340, A Series

3

THREE–TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA

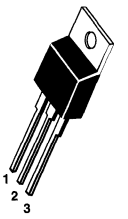
Three-Terminal Positive Fixed Voltage Regulators

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.0 A. These three–terminal regulators employ internal current limiting, thermal shutdown, and safe–area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on A–suffix 5.0, 12 and 15 V device types.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series–pass transistor to boost output current capability at the nominal output voltage.

- Output Current in Excess of 1.0 A
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation

T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Input
2. Ground
3. Output

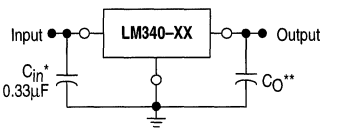
Heatsink surface is connected to Pin 2.

ORDERING INFORMATION

Device	Output Voltage and Tolerance	Operating Temperature Range	Package
LM340T–5.0	5.0 V ± 4%	T_J = 0° to +125°C	Plastic Power
LM340AT–5.0	5.0 V ± 2%		
LM340T–6.0	6.0 V ± 4%		
LM340T–8.0	8.0 V ± 4%		
LM340T–12	12 V ± 4%		
LM340AT–12	12 V ± 2%		
LM340T–15	15 V ± 4%		
LM340AT–15	15 V ± 2%		
LM340T–18	18 V ± 4%		
LM340T–24	24 V ± 4%		

* 2% regulators are available in 5, 12 and 15 V devices.

Simplified Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.7 V above the output voltage even during the low point on the input ripple voltage.

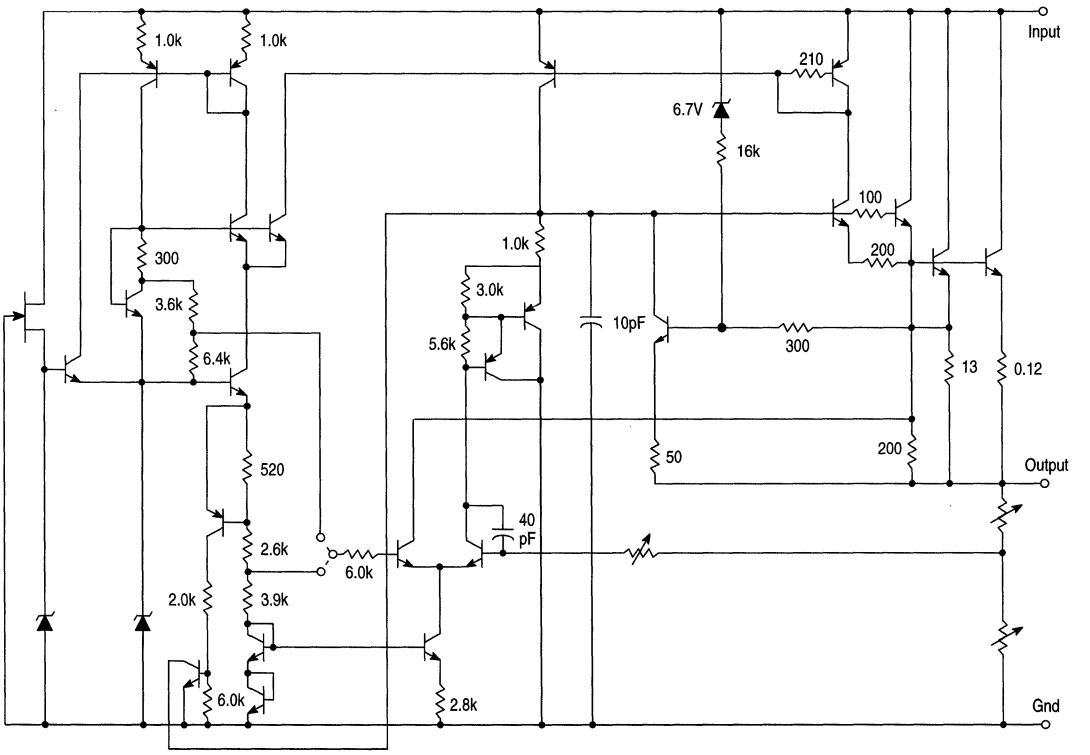
XX these two digits of the type number indicate voltage.
* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O is not needed for stability; however, it does improve transient response. If needed, use a 0.1 μF ceramic disc.

3

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics Plastic Package T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction–to–Air T_C= +25°C Derate above T_C = +75°C (See Figure 1) Thermal Resistance, Junction–to–Case	 P_D $1/\theta_{JA}$ θ_{JA} P_D $1/\theta_{JA}$ θ_{JC}	 Internally Limited 15.4 65 Internally Limited 200 5.0	 W mW/°C °C/W W mW/°C °C/W
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

Representative Schematic Diagram



LM340–5.0

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.8	5.0	5.2	Vdc
Line Regulation (Note 2) 8.0 Vdc to 20 Vdc 7.0 Vdc to 25 Vdc (T_J = +25°C) 8.0 Vdc to 12 Vdc, I_O = 1.0 A 7.3 Vdc to 20 Vdc, I_O = 1.0 A (T_J = +25°C)	Reg_{line}	 – – – –	 – – – –	 50 50 25 50	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 – – –	 – – –	 50 50 25	mV
Output Voltage 7.0 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	4.75	–	5.25	Vdc
Quiescent Current I_O = 1.0 A T_J = +25°C	I_B	 – –	 – 4.0	 8.5 8.0	mA
Quiescent Current Change 7.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V 7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A	ΔI_B	 – – –	 – – –	 1.0 0.5 1.0	mA
Ripple Rejection I_O = 1.0 A (T_J = +25°C)	RR	62	80	–	dB
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	2.0	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	40	–	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±0.6	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		7.3	–	–	Vdc

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

LM340A–5.0

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.9	5.0	5.1	Vdc
Line Regulation	Reg_{line}				mV
7.5 Vdc to 20 Vdc, I_O = 500 mA		–	–	10	
7.3 Vdc to 25 Vdc (T_J = +25°C)		–	3.0	10	
8.0 Vdc to 12 Vdc		–	–	12	
8.0 Vdc to 12 Vdc (T_J = +25°C)		–	–	4.0	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	25	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	25	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	15	
Output Voltage 7.5 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	4.8	–	5.2	Vdc
Quiescent Current	I_B	–	–	6.5	mA
T_J = +25°C		–	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V		–	–	0.5	
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	–	0.8	
7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	0.8	
Ripple Rejection	RR				dB
8.0 ≤ V_{in} ≤ 18 Vdc, f = 120 Hz					
I_O = 500 mA		68	–	–	
I_O = 1.0 A (T_J = +25°C)		68	80	–	
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	2.0	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	40	–	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±0.6	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		7.3	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

LM340–6.0

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	5.75	6.0	6.25	Vdc
Line Regulation	Reg_{line}				mV
9.0 Vdc to 21 Vdc		–	–	60	
8.0 Vdc to 25 Vdc (T_J = +25°C)		–	–	60	
9.0 Vdc to 13 Vdc, I_O = 1.0 A		–	–	30	
8.3 Vdc to 21 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	60	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	60	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	60	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	30	
Output Voltage 8.0 ≤ V_{in} ≤ 21 Vdc, 6.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	5.7	–	6.3	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		–	–	8.5	
T_J = +25°C		–	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 11 V		–	–	0.5	
8.6 ≤ V_{in} ≤ 21 Vdc, I_O = 1.0 A		–	–	1.0	
Ripple Rejection I_O = 1.0 A (T_J = +25°C)	RR	59	78	–	dB
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	1.9	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	45	–	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±0.7	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		8.3	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

LM340–8.0

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	7.7	8.0	8.3	Vdc
Line Regulation	Reg_{line}				mV
11 Vdc to 23 Vdc		–	–	80	
10.5 Vdc to 25 Vdc (T_J = +25°C)		–	–	80	
11 Vdc to 17 Vdc, I_O = 1.0 A		–	–	40	
10.5 Vdc to 23 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	80	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	80	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	80	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	40	
Output Voltage 10.5 ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	7.6	–	8.4	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		–	–	8.5	
T_J = +25°C		–	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
10.5 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 14 V		–	–	0.5	
10.6 ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A		–	–	1.0	
Ripple Rejection I_O = 1.0 A (T_J = +25°C)	RR	56	76	–	dB
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	1.5	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	52	–	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±1.0	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		10.5	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

LM340–12

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	11.5	12	12.5	Vdc
Line Regulation (Note 2) 15 Vdc to 27 Vdc 14.6 Vdc to 30 Vdc (T_J = +25°C) 16 Vdc to 22 Vdc, I_O = 1.0 A 14.6 Vdc to 27 Vdc, I_O = 1.0 A (T_J = +25°C)	Reg_{line}	 – – – –	 – – – –	 120 120 60 120	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 – – –	 – – –	 120 120 60	mV
Output Voltage 14.5 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	11.4	–	12.6	Vdc
Quiescent Current I_O = 1.0 A T_J = +25°C	I_B	 – –	 – 4.0	 8.5 8.0	mA
Quiescent Current Change 14.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V 14.8 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A	ΔI_B	 – – –	 – – –	 1.0 0.5 1.0	mA
Ripple Rejection I_O = 1.0 A (T_J = +25°C)	RR	55	72	–	dB
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	1.1	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	75	–	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±1.5	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		14.6	–	–	Vdc

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM340A–12

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 1.0 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	11.75	12	12.25	Vdc
Line Regulation	Reg_{line}				mV
14.8 Vdc to 27 Vdc, I_O = 500 mA		–	–	18	
14.5 Vdc to 30 Vdc (T_J = +25°C)		–	4.0	18	
16 Vdc to 22 Vdc		–	–	30	
16 Vdc to 22 Vdc (T_J = +25°C)		–	–	9.0	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	60	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	32	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	19	
Output Voltage 14.8 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	11.5	–	12.5	Vdc
Quiescent Current	I_B	–	–	6.5	mA
T_J = +25°C		–	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V		–	–	0.5	
15 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		–	–	0.8	
14.8 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A(T_J = +25°C)		–	–	0.8	
Ripple Rejection	RR				dB
15 ≤ V_{in} ≤ 25 Vdc, f = 120 Hz					
I_O = 500 mA		61	–	–	
I_O = 1.0 A (T_J = +25°C)		61	72	–	
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	1.1	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	75	–	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±1.5	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		14.5	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

LM340–15

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	14.4	15	15.6	Vdc
Line Regulation (Note 2) 18.5 Vdc to 30 Vdc 17.5 Vdc to 30 Vdc (T_J = +25°C) 20 Vdc to 26 Vdc, I_O = 1.0 A 17.7 Vdc to 30 Vdc, I_O = 1.0 A (T_J = +25°C)	Reg_{line}	 – – – –	 – – – –	 150 150 75 150	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 – – –	 – – –	 150 150 75	mV
Output Voltage 17.5 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	14.25	–	15.75	Vdc
Quiescent Current I_O = 1.0 A T_J = +25°C	I_B	 – –	 – 4.0	 8.5 8.0	mA
Quiescent Current Change 17.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V 17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A	ΔI_B	 – – –	 – – –	 1.0 0.5 1.0	mA
Ripple Rejection I_O = 1.0 mA (T_J = +25°C)	RR	54	70	–	dB
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	800	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	90	–	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±1.8	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		17.7	–	–	Vdc

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM340A–15

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1.0 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	14.7	15	15.3	Vdc
Line Regulation	Reg_{line}				mV
17.9 Vdc to 30 Vdc, I_O = 500 mA		–	–	22	
17.5 Vdc to 30 Vdc (T_J = +25°C)		–	4.0	22	
20 Vdc to 26 Vdc, I_O = 1.0 A		–	–	30	
20 Vdc to 26 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	10	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	75	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	12	35	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	21	
Output Voltage 17.9 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	14.4	–	15.6	Vdc
Quiescent Current	I_B	–	–	6.5	mA
T_J = +25°C		–	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V		–	–	0.5	
17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		–	–	0.8	
17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	0.8	
Ripple Rejection	RR				dB
18.5 ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz					
I_O = 500 mA		60	–	–	
I_O = 1.0 A (T_J = +25°C)		60	70	–	
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	800	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	90	–	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±1.8	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		17.5	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

LM340–18

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	17.3	18	18.7	Vdc
Line Regulation 21.5 Vdc to 33 Vdc 21 Vdc to 33 Vdc (T_J = +25°C) 24 Vdc to 30 Vdc, I_O = 1.0 A 21 Vdc to 33 Vdc, I_O = 1.0 A (T_J = +25°C)	Reg_{line}	 – – – –	 – – – –	 180 180 90 180	mV
Load Regulation 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 – – –	 – – –	 180 180 90	mV
Output Voltage 21 ≤ V_{in} ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	17.1	–	18.9	Vdc
Quiescent Current I_O = 1.0 A T_J = +25°C	I_B	 – –	 – 4.0	 8.5 8.0	mA
Quiescent Current Change 21 ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 27 V 21 ≤ V_{in} ≤ 33 Vdc, I_O = 1.0 A	ΔI_B	 – – –	 – – –	 1.0 0.5 1.0	mA
Ripple Rejection I_O = 1.0 mA (T_J = +25°C)	RR	53	69	–	dB
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	500	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	110	–	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±2.3	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		21	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

LM340–24

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	23	24	25	Vdc
Line Regulation	Reg_{line}				mV
28 Vdc to 38 Vdc		–	–	240	
27 Vdc to 38 Vdc (T_J = +25°C)		–	–	240	
30 Vdc to 36 Vdc, I_O = 1.0 A		–	–	120	
27.1 Vdc to 38 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	240	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	240	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	240	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	120	
Output Voltage 27 ≤ V_{in} ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	22.8	–	25.2	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		–	–	8.5	
T_J = +25°C		–	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
27 ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 33 V		–	–	0.5	
27.3 ≤ V_{in} ≤ 38 Vdc, I_O = 1.0 A		–	–	1.0	
Ripple Rejection I_O = 1.0 mA (T_J = +25°C)	RR	50	66	–	dB
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	200	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	170	–	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±3.0	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		27.1	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical LM340AT–5.0 to a 10 W input pulse. The variation of the output voltage due to line regulation is labeled À and the thermal regulation component is labeled Á. Figure 2 shows the load and thermal regulation response of a typical LM340AT–5.0 to a 15 W load pulse. The output voltage variation due to load regulation is labeled À and the thermal regulation component is labeled Á.

Figure 1. Line and Thermal Regulation

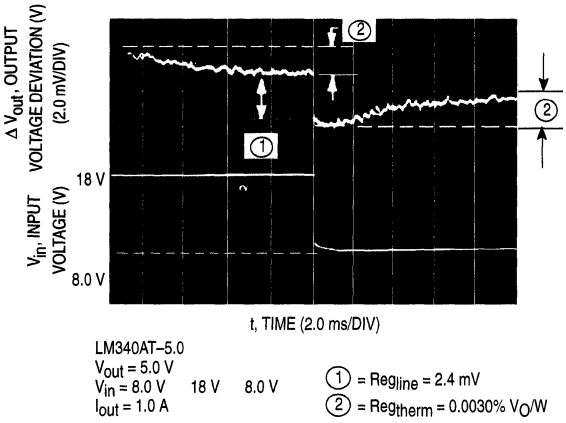


Figure 2. Load and Thermal Regulation

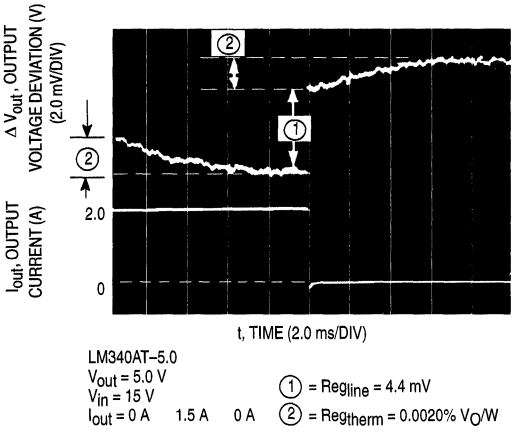


Figure 3. Temperature Stability

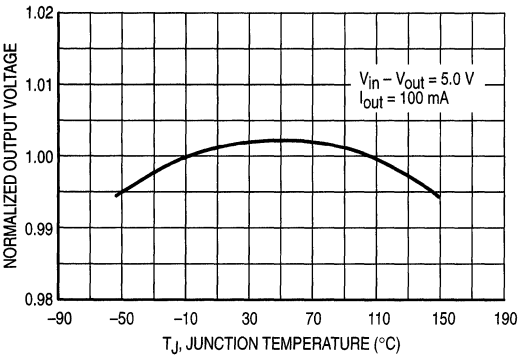
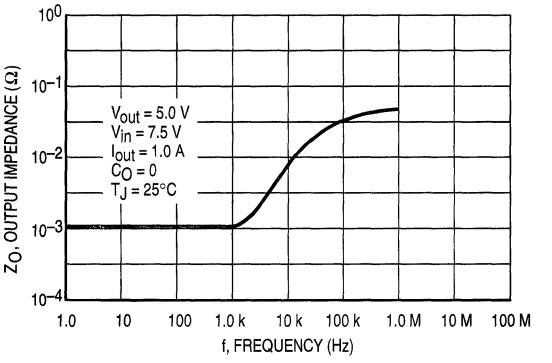


Figure 4. Output Impedance



3

Figure 5. Ripple Rejection versus Frequency

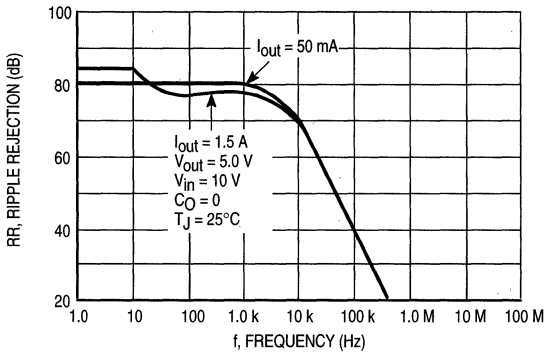


Figure 6. Ripple Rejection versus Output Current

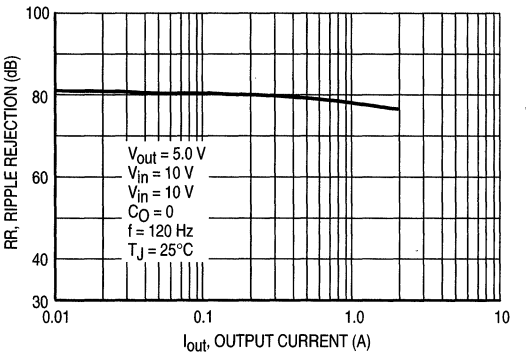


Figure 7. Quiescent Current versus Input Voltage

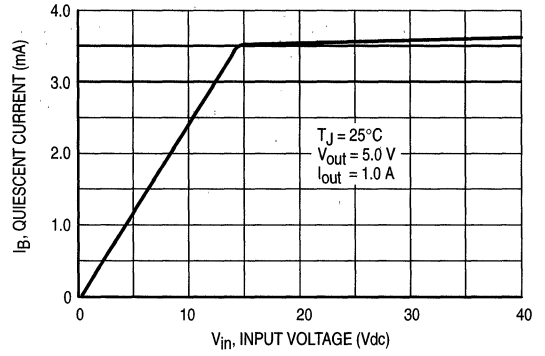


Figure 8. Quiescent Current versus Output Current

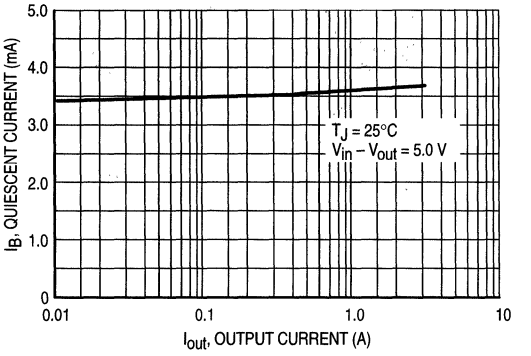


Figure 9. Dropout Voltage

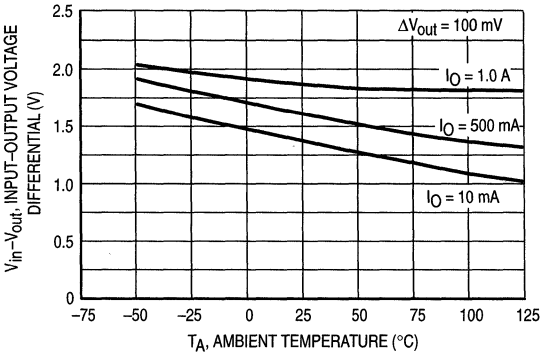


Figure 10. Peak Output Current

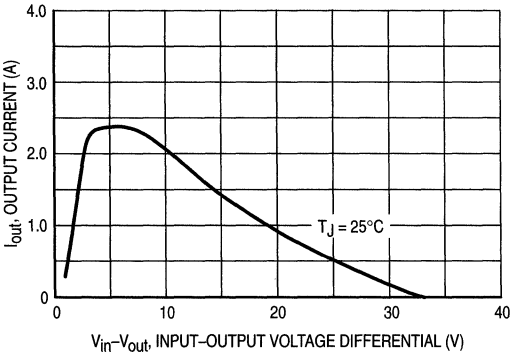


Figure 11. Line Transient Response

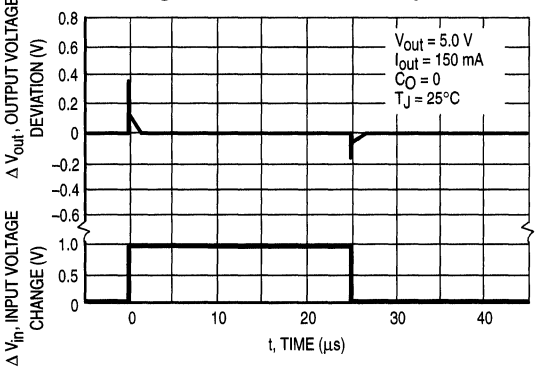


Figure 12. Load Transient Response

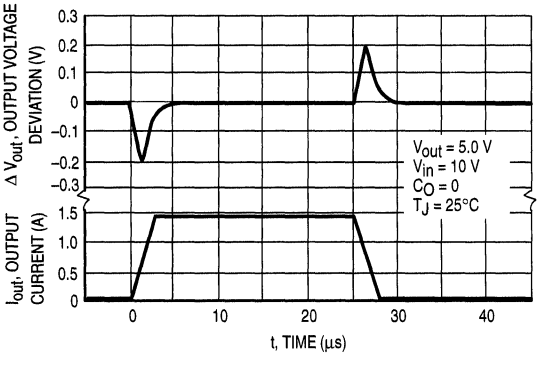
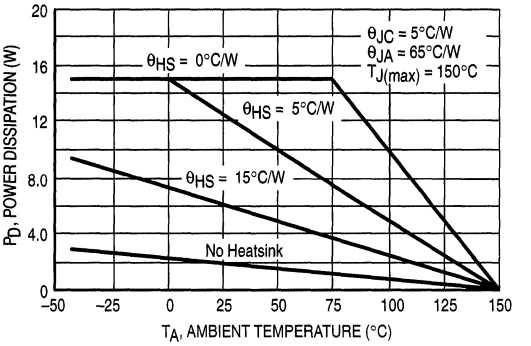


Figure 13. Worst Case Power Dissipation versus Ambient Temperature (Case 221A)



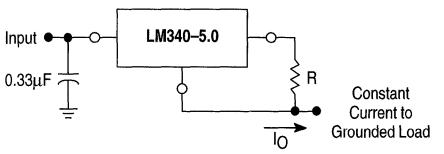
APPLICATIONS INFORMATION

Design Considerations

The LM340, A series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 14. Current Regulator



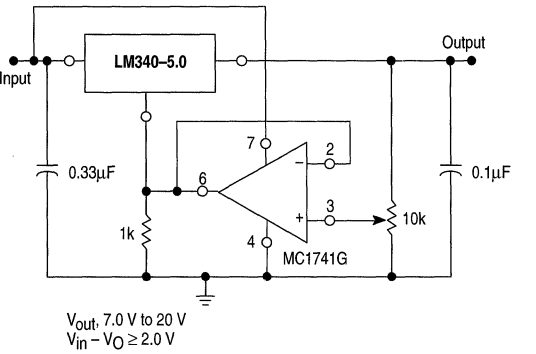
These regulators can also be used as a current source when connected as above. In order to minimize dissipation the LM340–5.0 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

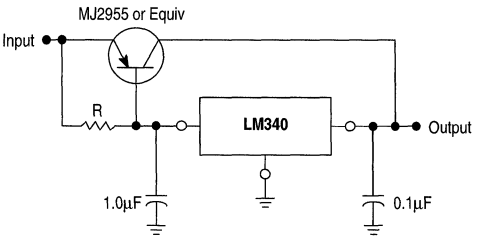
For example, a 1 A current source would require R to be a 5 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 V.

Figure 15. Adjustable Output Regulator



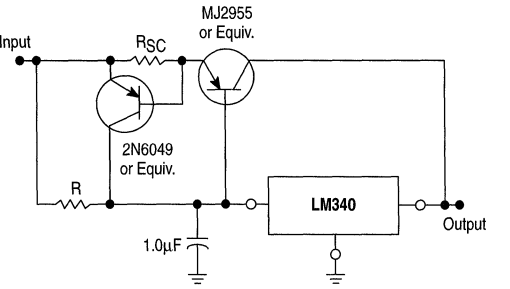
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 V greater than the regulator voltage.

Figure 16. Current Boost Regulator



The LM340, A series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 A. Resistor R in conjuction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input–output differential voltage minimum is increased by V_{BE} of the pass transistor.

Figure 17. Short Circuit Protection



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three–terminal regulator. Therefore, 4.0 A plastic power transistor is specified.

LM350

Three-Terminal Adjustable Output Positive Voltage Regulator

THREE–TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

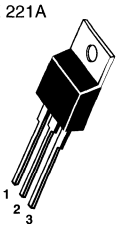
SEMICONDUCTOR TECHNICAL DATA

The LM350 is an adjustable three–terminal positive voltage regulator capable of supplying in excess of 3.0 A over an output voltage range of 1.2 V to 33 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof.

The LM350 serves a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM350 can be used as a precision current regulator.

- Guaranteed 3.0 A Output Current
- Output Adjustable between 1.2 V and 33 V
- Load Regulation Typically 0.1%
- Line Regulation Typically 0.005%/V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3–lead Transistor Package
- Eliminates Stocking Many Fixed Voltages

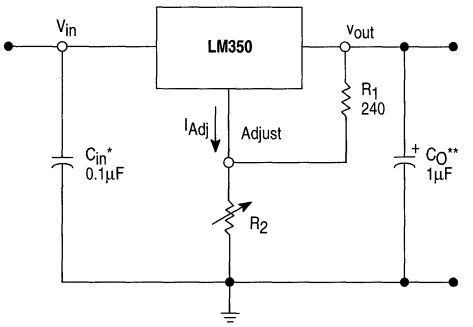
T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Adjust
2. V_{out}
3. V_{in}

Heatsink surface is connected to Pin 2.

Simplified Application



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.
** = C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM350T	T_J = 0° to +125°C	Plastic Power
LM350BT#	T_J = –40° to +125°C	Plastic Power

Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input–Output Voltage Differential	V_I–V_O	35	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Soldering Lead Temperature (10 seconds)	T_{solder}	300	°C

ELECTRICAL CHARACTERISTICS (V_I–V_O = 5.0 V; I_L = 1.5 A; T_J = T_{low} to T_{high}; P_{max} [Note 1], unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 2) T_A = 25°C, 3.0 V ≤ V_I–V_O ≤ 35 V	1	Reg_{line}	–	0.0005	0.03	%/V
Load Regulation (Note 2) T_A = 25°C, 10 mA ≤ I_I ≤ 3.0 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 – –	 5.0 0.1	 25 0.5	 mV % V_O
Thermal Regulation, Pulse = 20 ms, (T_A = +25°C)		Reg_{therm}	–	0.002	–	% V_O/W
Adjustment Pin Current	3	I_{Adj}	–	50	100	µA
Adjustment Pin Current Change 3.0 V ≤ V_I–V_O ≤ 35 V 10 mA ≤ I_L ≤ 3.0 A, P_D ≤ P_{max}	1,2	ΔI_{Adj}	–	0.2	5.0	µA
Reference Voltage 3.0 V ≤ V_I–V_O ≤ 35 V 10 mA ≤ I_O ≤ 3.0 A, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 2) 3.0 V ≤ V_I–V_O ≤ 35 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 2) 10 mA ≤ I_L ≤ 3.0 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 – –	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	1.0	–	% V_O
Minimum Load Current to Maintain Regulation (V_I–V_O = 35 V)	3	I_{Lmin}	–	3.5	10	mA
Maximum Output Current V_I–V_O ≤ 10 V, P_D ≤ P_{max} V_I–V_O = 30 V, P_D ≤ P_{max}, T_A = 25°C	3	I_{max}	 3.0 0.25	 4.5 1.0	 – –	A
RMS Noise, % of V_O T_A= 25°C, 10 Hz ≤ f ≤ 10 kHz		N	–	0.003	–	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 3) Without C_{Adj} C_{Adj} = 10 µF	4	RR	 – 66	 65 80	 – –	dB
Long Term Stability, T_J = T_{high} (Note 4) T_A= 25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance, Junction–to–Case Peak (Note 5) Average (Note 6)		$R_{\theta JC}$	 – –	 2.3 –	 – 1.5	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C; P_{max} = 25 W for LM350T; T_{low} to T_{high} = −40° to +125°C; P_{max} = 25 W for LM350BT
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
3. C_{Adj}, when used, is connected between the adjustment pin and ground.
4. Since Long–Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
5. Thermal Resistance evaluated measuring the hottest temperature on the die using an infrared scanner. This method of evaluation yields very accurate thermal resistance values which are conservative when compared to the other measurement techniques.
6. The average die temperature is used to derive the value of thermal resistance junction to case (average).

Representative Schematic Diagram

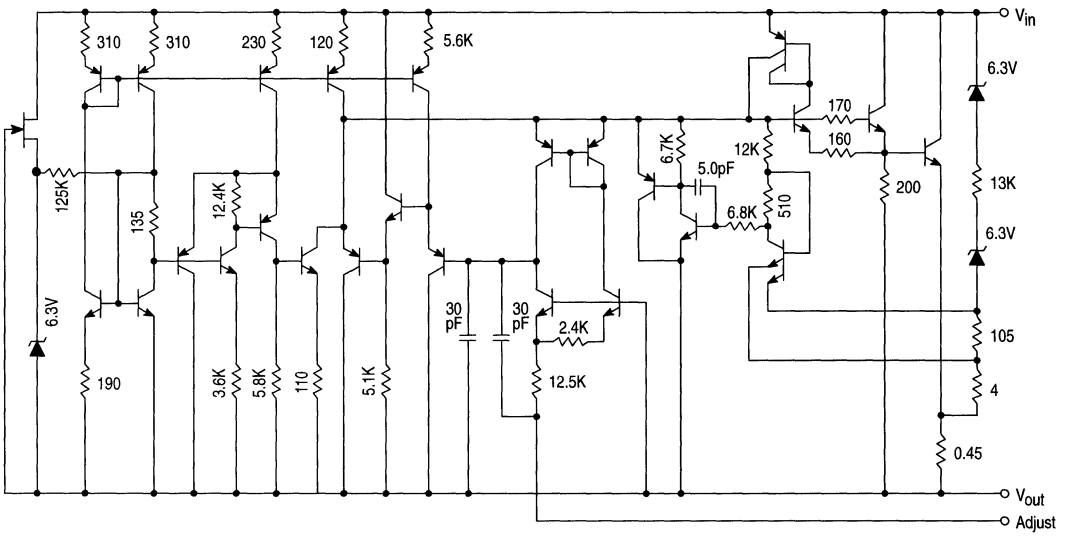


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit

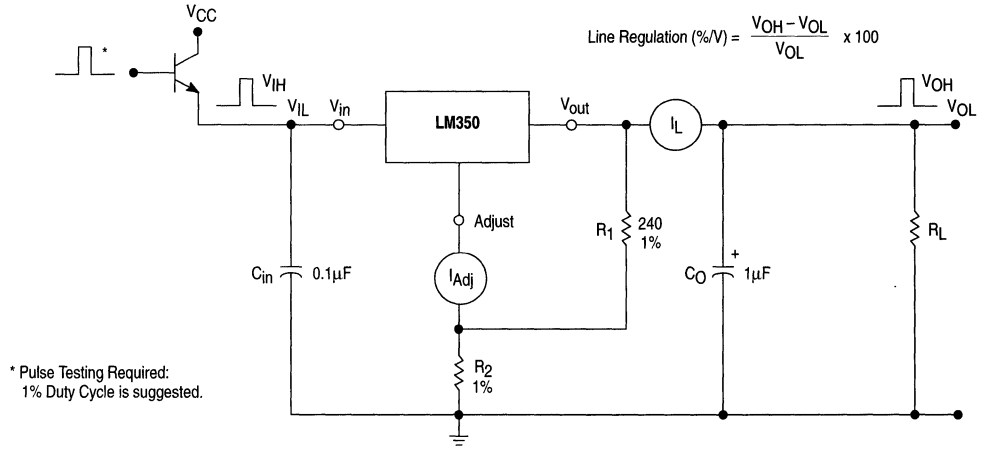
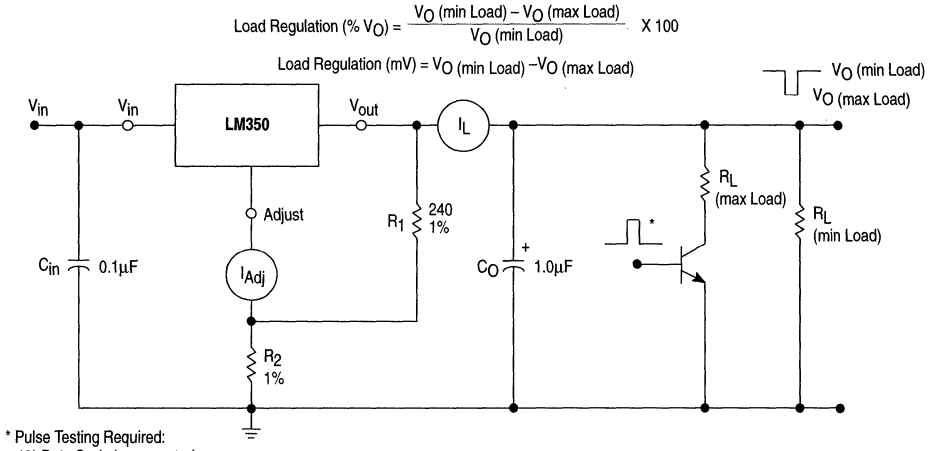


Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit

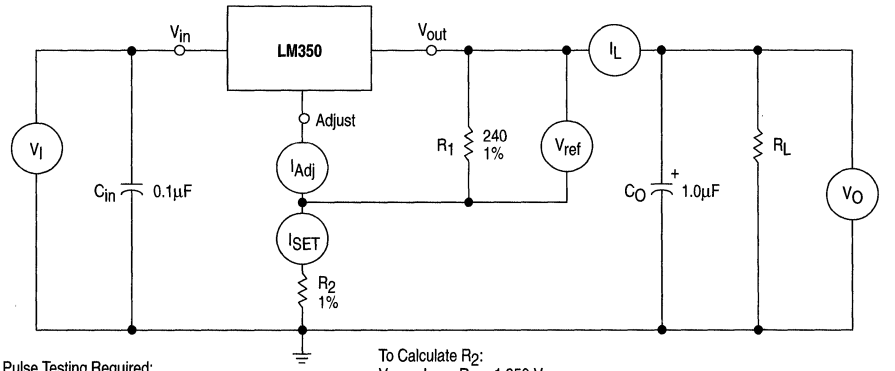
$$\text{Load Regulation (\% } V_O) = \frac{V_O \text{ (min Load)} - V_O \text{ (max Load)}}{V_O \text{ (min Load)}} \times 100$$

$$\text{Load Regulation (mV)} = V_O \text{ (min Load)} - V_O \text{ (max Load)}$$



* Pulse Testing Required:
1% Duty Cycle is suggested.

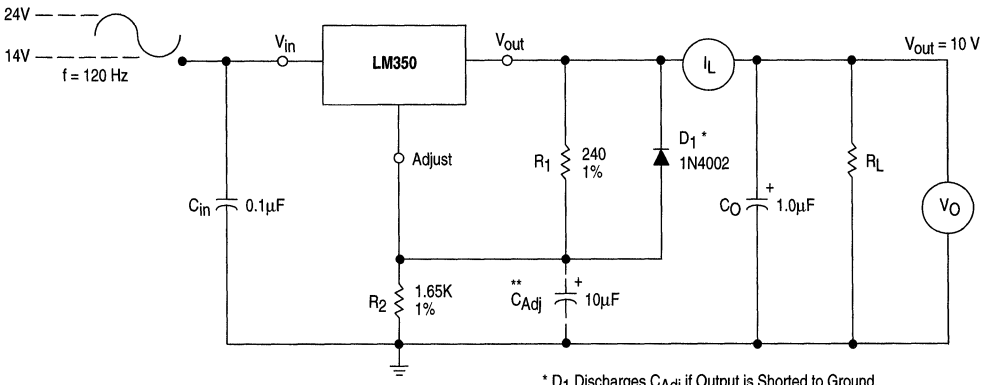
Figure 3. Standard Test Circuit



Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_{out} = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if Output is Shorted to Ground.
**C_{Adj} provides an AC ground to the adjust pin.

Figure 5. Load Regulation

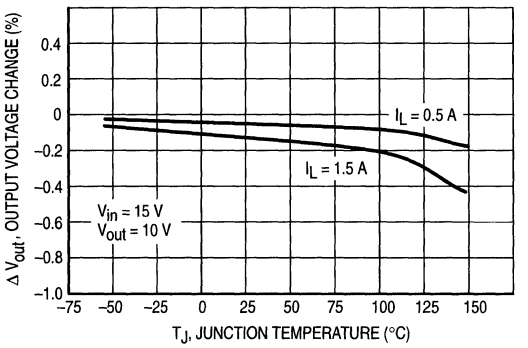


Figure 6. Current Limit

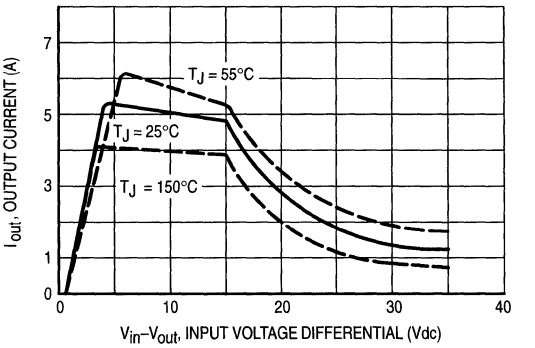


Figure 7. Adjustment Pin Current

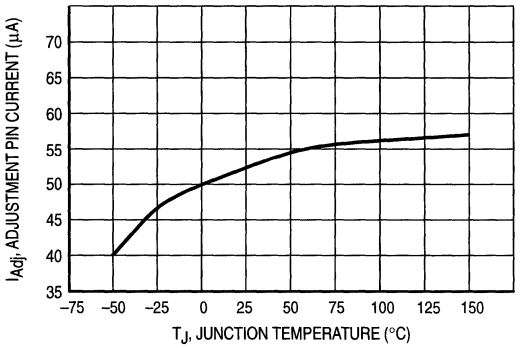


Figure 8. Dropout Voltage

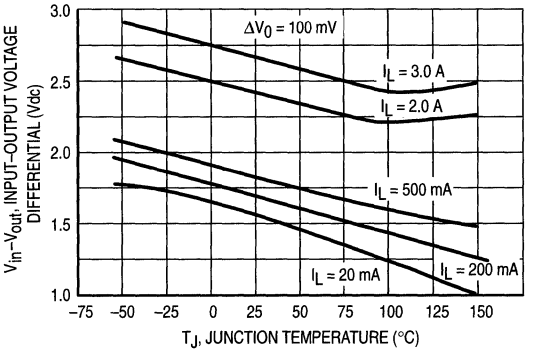


Figure 9. Temperature Stability

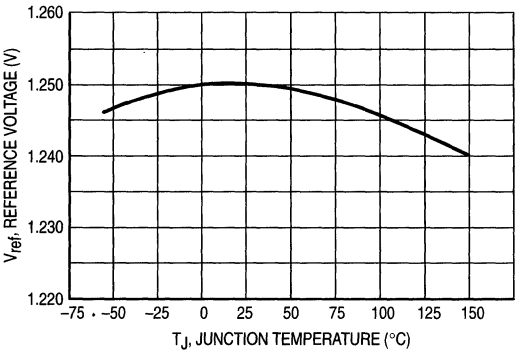
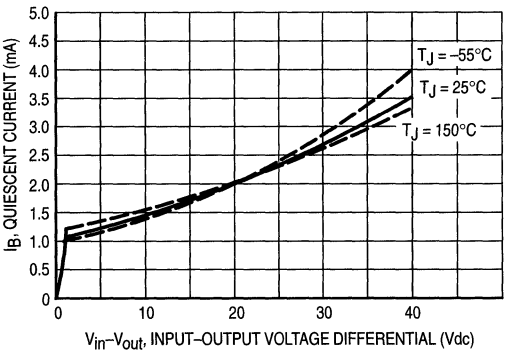


Figure 10. Minimum Operating Current



3

Figure 11. Ripple Rejection versus Output Voltage

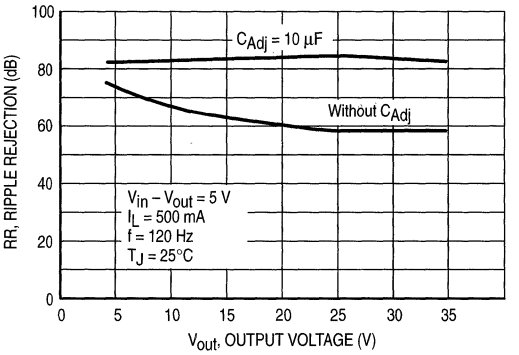


Figure 12. Ripple Rejection versus Output Current

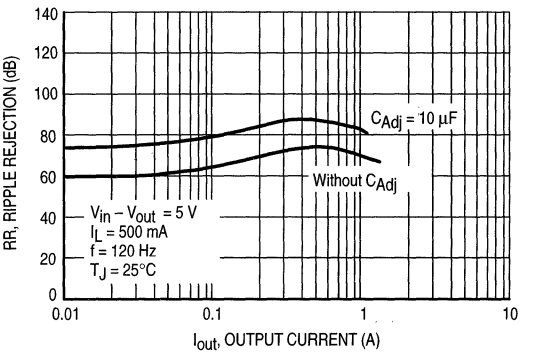


Figure 13. Ripple Rejection versus Frequency

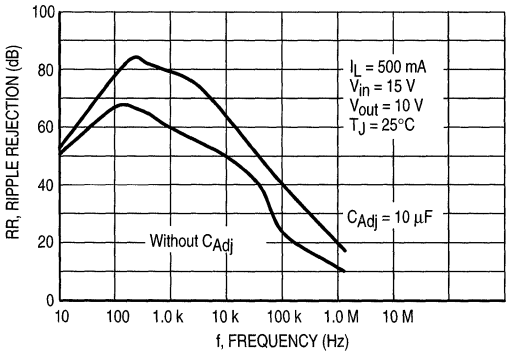


Figure 14. Output Impedance

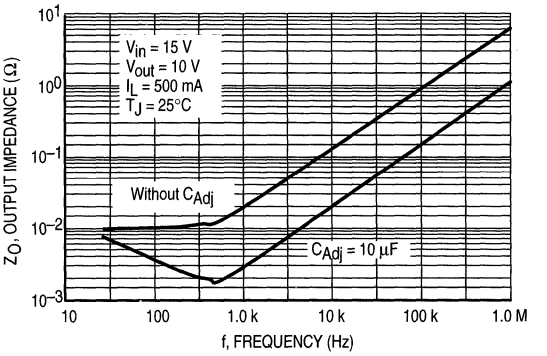


Figure 15. Line Transient Response

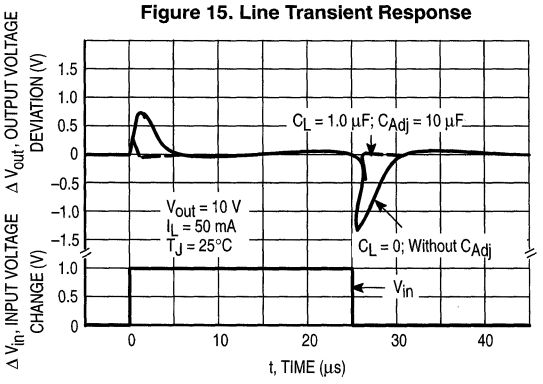
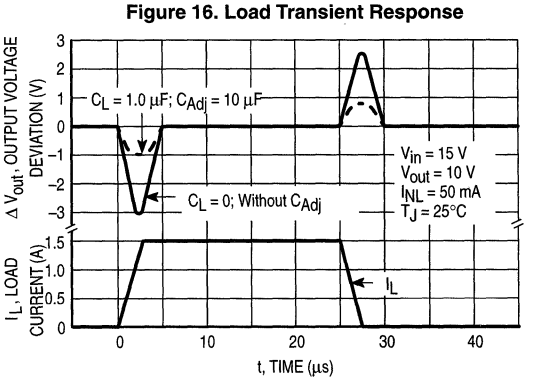


Figure 16. Load Transient Response



APPLICATIONS INFORMATION

Basic Circuit Operation

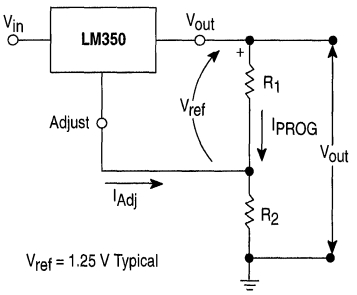
The LM350 is a three–terminal floating regulator. In operation, the LM350 develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

Since the current from the terminal (I_{Adj}) represents an error term in the equation, the LM350 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM350 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



Load Regulation

The LM350 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM350 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator, it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM350 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 10 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

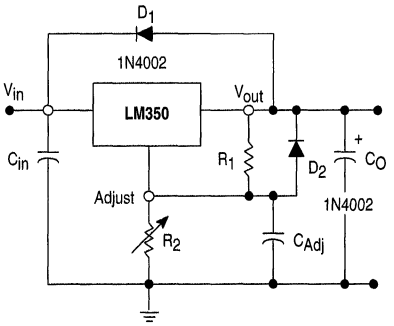
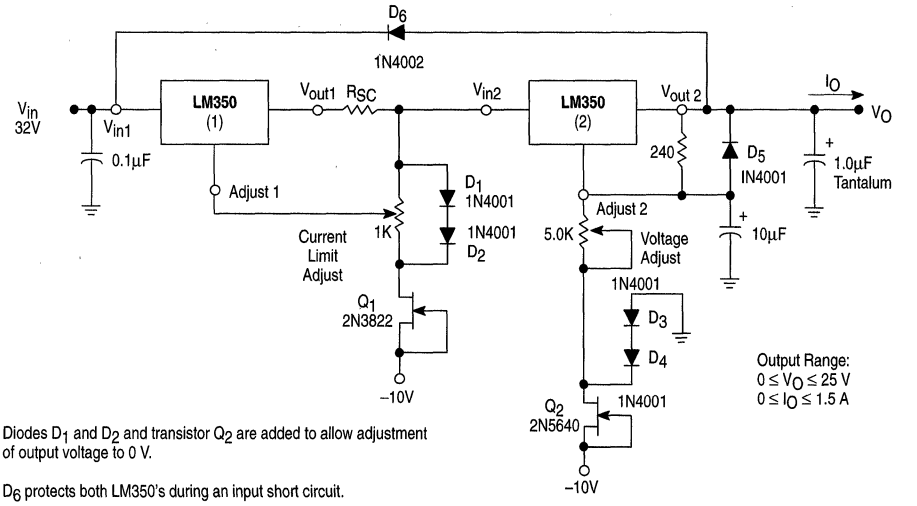


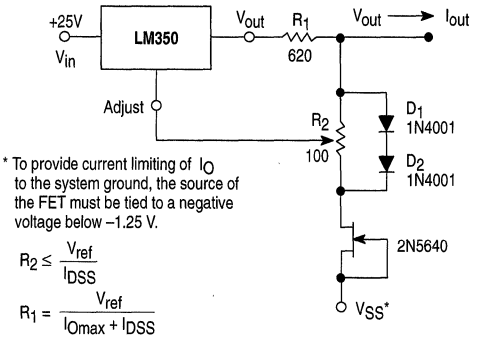
Figure 19. "Laboratory" Power Supply with Adjustable Current Limit and Output Voltage



Diodes D_1 and D_2 and transistor Q_2 are added to allow adjustment of output voltage to 0 V.

D_6 protects both LM350's during an input short circuit.

Figure 20. Adjustable Current Limiter



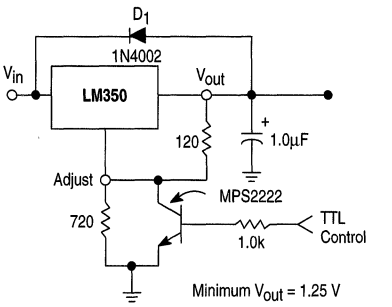
* To provide current limiting of I_O to the system ground, the source of the FET must be tied to a negative voltage below –1.25 V.

$$R_2 \leq \frac{V_{ref}}{I_{DSS}}$$

$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

$V_O < V_{(BR)DSS} + 1.25\ V + V_{SS}$
$I_{Lmin} - I_{DSS} < I_O < 3.0\ A$
As shown $O < I_O < 1.0\ A$

Figure 21. 5.0 V Electronic Shutdown Regulator



D_1 protects the device during an input short circuit.

Figure 22. Slow Turn–On Regulator

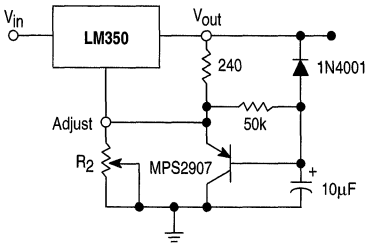
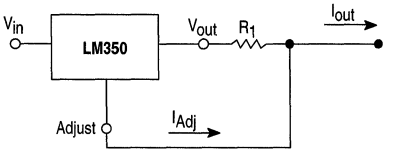


Figure 23. Current Regulator



$$I_{out} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj}$$

$$\cong \frac{1.25\ V}{R_1}$$

$10\ mA \leq I_{out} \leq 3.0\ A$

LM2575

Advance Information

Easy Switcher™ 1.0 A Step-Down Voltage Regulator

EASY SWITCHER™
1.0 A STEP–DOWN
VOLTAGE REGULATOR

SEMICONDUCTOR
TECHNICAL DATA

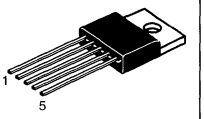
The LM2575 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step–down switching regulator (buck converter). All circuits of this series are capable of driving a 1.0 A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3 V, 5.0 V, 12 V, 15 V, and an adjustable output version.

These regulators were designed to minimize the number of external components to simplify the power supply design. Standard series of inductors optimised for use with the LM2575 are offered by several different inductor manufacturers.

Since the LM2575 converter is a switch–mode power supply, its efficiency is significantly higher in comparison with popular three–terminal linear regulators, especially with higher input voltages. In many cases, the power dissipated by the LM2575 regulator is so low, that no heatsink is required or its size could be reduced dramatically.

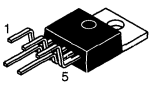
The LM2575 features include a guaranteed ±4% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency (±2% over 0°C to 125°C). External shutdown is included, featuring 80 μA typical standby current. The output switch includes cycle–by–cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

T SUFFIX
PLASTIC PACKAGE
CASE 314D



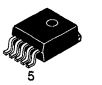
Pin 1. V_{in}
2. Output
3. Ground
4. Feedback
5. $\overline{ON}$/OFF

TV SUFFIX
PLASTIC PACKAGE
CASE 314B



Heatsink surface
connected to Pin 3.

D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^2PAK)



Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3.

Features

- 3.3 V, 5.0 V, 12 V, 15 V, and Adjustable Output Versions
- Adjustable Version Output Voltage Range of 1.23 V to 37 V ±4% Maximum Over Line and Load Conditions
- Guaranteed 1.0 A Output Current
- Wide Input Voltage Range: 4.75 V to 40 V
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- TTL Shutdown Capability, Low Power Standby Mode
- High Efficiency
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection

Applications

- Simple and High–Efficiency Step–Down (Buck) Regulators
- Efficient Pre–Regulator for Linear Regulators
- On–Card Switching Regulators
- Positive to Negative Converters (Buck–Boost)
- Negative Step–Up Converters
- Power Supply for Battery Chargers

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

LM2575–3.3	3.3 V
LM2575–5	5.0 V
LM2575–12	12 V
LM2575–15	15 V
LM2575–Adj	1.23 V to 37 V

ORDERING INFORMATION

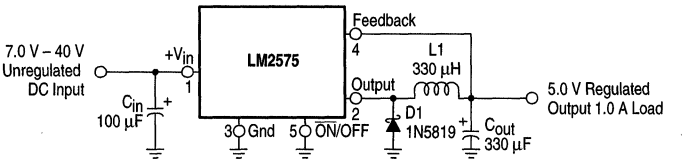
Device	Operating Temperature Range	Package
LM2575T–**	T_J = –40° to +125°C	Straight Lead
LM2575TV–**		Vertical Mount
LM2575D2T–**		Surface Mount

** = Voltage Option, ie. 3.3, 5.0, 12, 15 V and Adjustable Output.

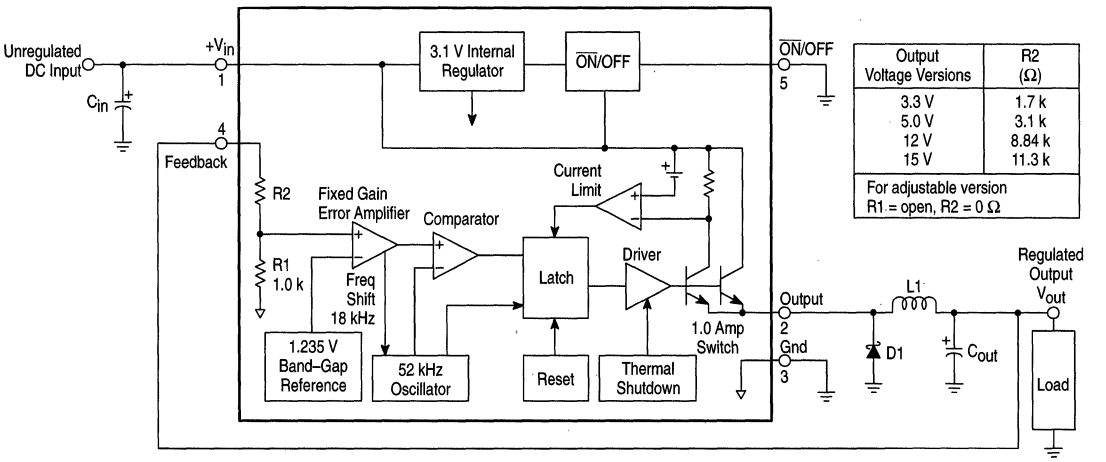
3

Figure 1. Block Diagram and Typical Application

Typical Application (Fixed Output Voltage Versions)



Representative Block Diagram and Typical Application



Output Voltage Versions	R2 (Ω)
3.3 V	1.7 k
5.0 V	3.1 k
12 V	8.84 k
15 V	11.3 k
For adjustable version R1 = open, R2 = 0 Ω	

This device contains 162 active transistors.

ABSOLUTE MAXIMUM RATINGS (Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.)

Rating	Symbol	Value	Unit
Maximum Supply Voltage	V_{in}	45	V
ON/OFF Pin Input Voltage	–	$-0.3 V \le V \le +V_{in}$	V
Output Voltage to Ground (Steady–State)	–	–1.0	V
Power Dissipation			
Case 314B and 314D (TO–220, 5–Lead)	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Case 936A (D^2PAK)	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient (Figure 34)	$R_{\theta JA}$	70	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Storage Temperature Range	T_{stg}	–65 to +150	°C
Minimum ESD Rating (Human Body Model: C = 100 pF, R = 1.5 kΩ)	–	3.0	kV
Lead Temperature (Soldering, 10 s)	–	260	°C
Maximum Junction Temperature	T_J	150	°C

NOTE: ESD data available upon request.

OPERATING RATINGS (Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	–40 to +125	°C
Supply Voltage	V_{in}	40	V

SYSTEM PARAMETERS ([Note 1] Test Circuit Figure 14)

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{in} = 12 V for the 3.3 V, 5.0 V, and Adjustable version, V_{in} = 25 V for the 12 V version, and V_{in} = 30 V for the 15 V version. I_{Load} = 200 mA. For typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
LM2575–3.3 ([Note 1] Test Circuit Figure 14)					
Output Voltage (V_{in} = 12 V, I_{Load} = 0.2 A, T_J = 25°C)	V_{out}	3.234	3.3	3.366	V
Output Voltage (4.75 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A) T_J = 25°C T_J = –40 to +125°C	V_{out}	 3.168 3.135	 3.3 –	 3.432 3.465	V
Efficiency (V_{in} = 12 V, I_{Load} = 1.0 A)	η	–	75	–	%
LM2575–5 ([Note 1] Test Circuit Figure 14)					
Output Voltage (V_{in} = 12 V, I_{Load} = 0.2 A, T_J = 25°C)	V_{out}	4.9	5.0	5.1	V
Output Voltage (8.0 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A) T_J = 25°C T_J = –40 to +125°C	V_{out}	 4.8 4.75	 5.0 –	 5.2 5.25	V
Efficiency (V_{in} = 12 V, I_{Load} = 1.0 A)	η	–	77	–	%
LM2575–12 ([Note 1] Test Circuit Figure 14)					
Output Voltage (V_{in} = 25 V, I_{Load} = 0.2 A, T_J = 25°C)	V_{out}	11.76	12	12.24	V
Output Voltage (15 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A) T_J = 25°C T_J = –40 to +125°C	V_{out}	 11.52 11.4	 12 –	 12.48 12.6	V
Efficiency (V_{in} = 15V, I_{Load} = 1.0 A)	η	–	88	–	%
LM2575–15 ([Note 1] Test Circuit Figure 14)					
Output Voltage (V_{in} = 30 V, I_{Load} = 0.2 A, T_J = 25°C)	V_{out}	14.7	15	15.3	V
Output Voltage (18 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A) T_J = 25°C T_J = –40 to +125°C	V_{out}	 14.4 14.25	 15 –	 15.6 15.75	V
Efficiency (V_{in} = 18 V, I_{Load} = 1.0 A)	η	–	88	–	%
LM2575 ADJUSTABLE VERSION ([Note 1] Test Circuit Figure 14)					
Feedback Voltage (V_{in} = 12 V, I_{Load} = 0.2 A, V_{out} = 5.0 V, T_J = 25°C)	V_{FB}	1.217	1.23	1.243	V
Feedback Voltage (8.0 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A, V_{out} = 5.0 V) T_J = 25°C T_J = –40 to +125°C	V_{FB}	 1.193 1.18	 1.23 –	 1.267 1.28	V
Efficiency (V_{in} = 12 V, I_{Load} = 1.0 A, V_{out} = 5.0 V)	η	–	77	–	%

NOTES: 1. External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2575 is used as shown in the Figure 14 test circuit, system performance will be as shown in system parameters section.

2. Tested junction temperature range for the LM2575: T_{low} = –40°C T_{high} = +125°C

DEVICE PARAMETERS

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{in} = 12 V for the 3.3 V, 5.0 V, and Adjustable version, V_{in} = 25 V for the 12 V version, and V_{in} = 30 V for the 15 V version. I_{Load} = 200 mA. For typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
ALL OUTPUT VOLTAGE VERSIONS					
Feedback Bias Current (V_{out} = 5.0 V [Adjustable Version Only])	I_b				nA
T_J = 25°C		–	25	100	
T_J = –40 to +125°C		–	–	200	
Oscillator Frequency [Note 3]	f_{osc}				kHz
T_J = 25°C		–	52	–	
T_J = 0 to +125°C		47	–	58	
T_J = –40 to +125°C		42	–	63	
Saturation Voltage (I_{out} = 1.0 A [Note 4])	V_{sat}				V
T_J = 25°C		–	1.0	1.2	
T_J = –40 to +125°C		–	–	1.3	
Max Duty Cycle ("on") [Note 5]	DC	94	98	–	%
Current Limit (Peak Current [Notes 4 and 3])	I_{CL}				A
T_J = 25°C		1.7	2.3	3.0	
T_J = –40 to +125°C		1.4	–	3.2	
Output Leakage Current [Notes 6 and 7], T_J = 25°C	I_L				mA
Output = 0 V		–	0.8	2.0	
Output = –1.0 V		–	6.0	20	
Quiescent Current [Note 6]	I_Q				mA
T_J = 25°C		–	5.0	9.0	
T_J = –40 to +125°C		–	–	11	
Standby Quiescent Current ($\overline{ON}$/OFF Pin = 5.0 V ("off"))	I_{stby}				µA
T_J = 25°C		–	80	200	
T_J = –40 to +125°C		–	–	400	
$\overline{ON}$/OFF Pin Logic Input Level (Test Circuit Figure 14)					V
V_{out} = 0 V	V_{IH}				
T_J = 25°C		2.2	1.4	–	
T_J = –40 to +125°C		2.4	–	–	
V_{out} = Nominal Output Voltage	V_{IL}				
T_J = 25°C		–	1.2	1.0	
T_J = –40 to +125°C		–	–	0.8	
$\overline{ON}$/OFF Pin Input Current (Test Circuit Figure 14)					µA
$\overline{ON}$/OFF Pin = 5.0 V ("off"), T_J = 25°C	I_{IH}	–	15	30	
$\overline{ON}$/OFF Pin = 0 V ("on"), T_J = 25°C	I_{IL}	–	0	5.0	

NOTES: 3. The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which causes the regulated output voltage to drop approximately 40% from the nominal output voltage. This self protection feature lowers the average dissipation of the IC by lowering the minimum duty cycle from 5% down to approximately 2%.

4. Output (Pin 2) sourcing current. No diode, inductor or capacitor connected to output pin.

5. Feedback (Pin 4) removed from output and connected to 0 V.

6. Feedback (Pin 4) removed from output and connected to +12 V for the Adjustable, 3.3 V, and 5.0 V versions, and +25 V for the 12 V and 15 V versions, to force the output transistor "off".

7. V_{in} = 40 V.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 14)

Figure 2. Normalized Output Voltage

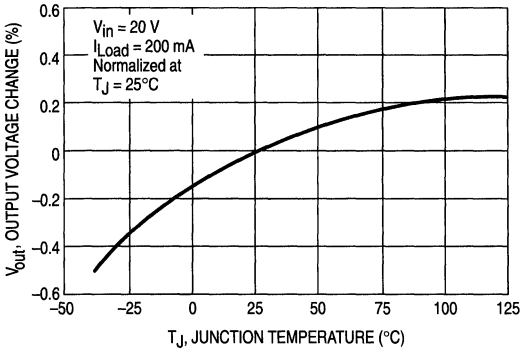


Figure 3. Line Regulation

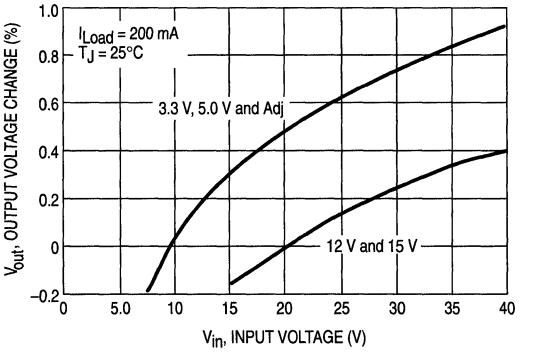


Figure 4. Switch Saturation Voltage

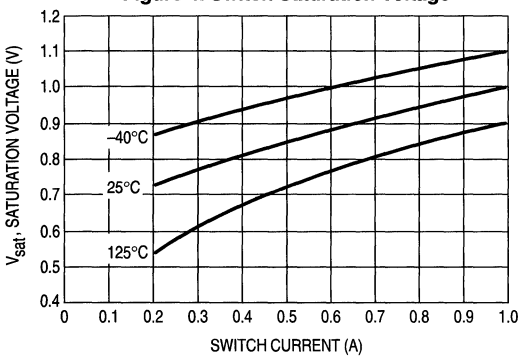


Figure 5. Current Limit

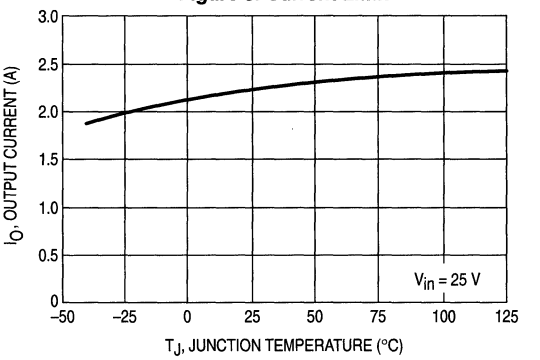


Figure 6. Dropout Voltage

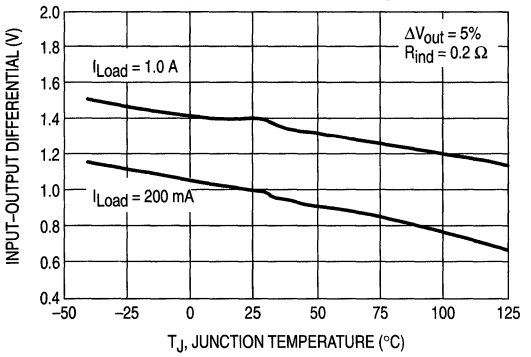
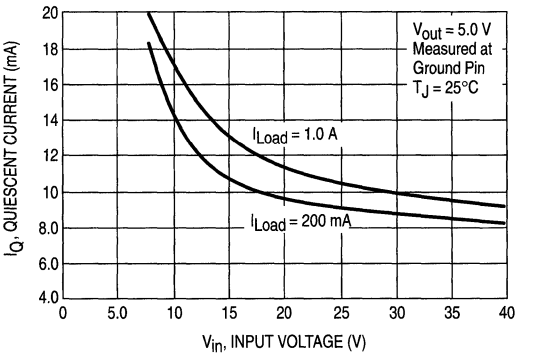


Figure 7. Quiescent Current



3

Figure 8. Standby Quiescent Current

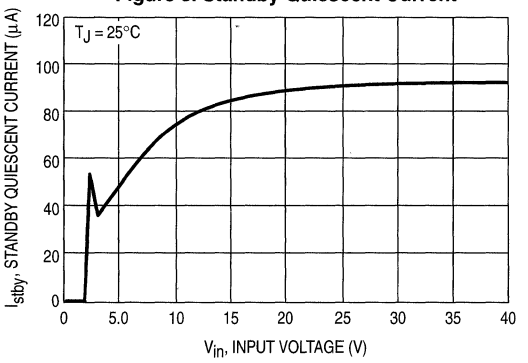


Figure 9. Standby Quiescent Current

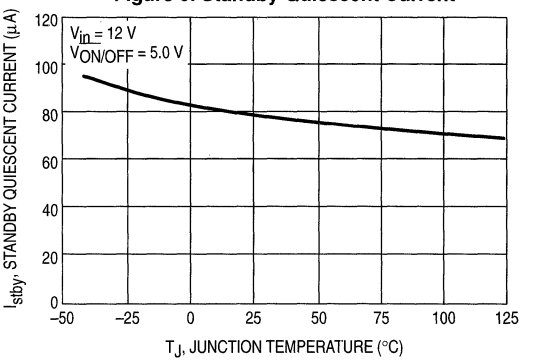


Figure 10. Oscillator Frequency

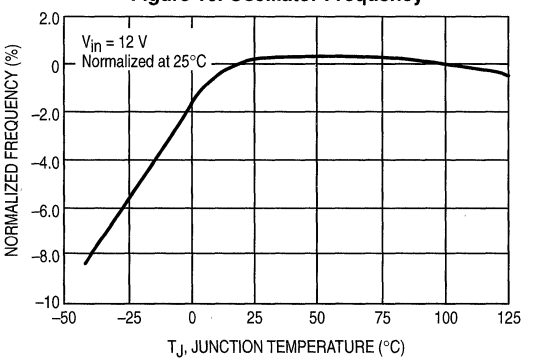


Figure 11. Feedback Pin Current

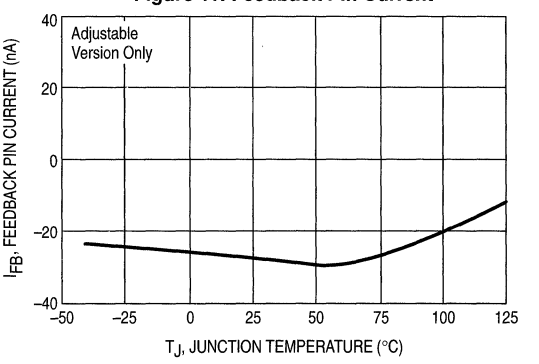


Figure 12. Switching Waveforms

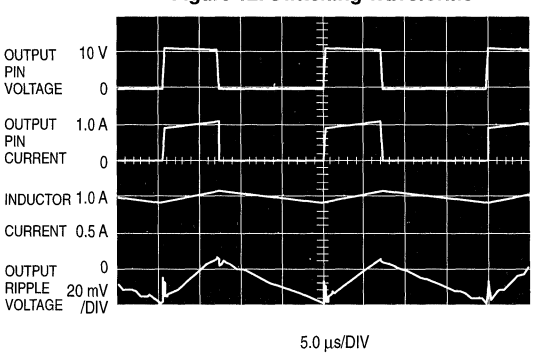


Figure 13. Load Transient Response

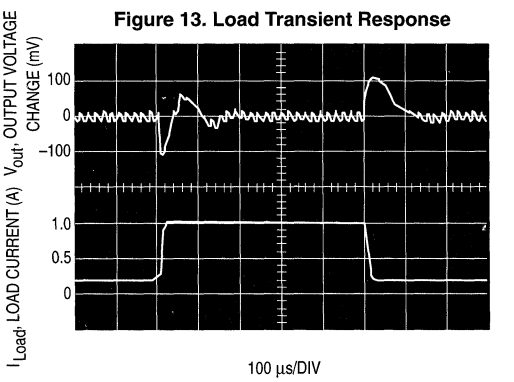
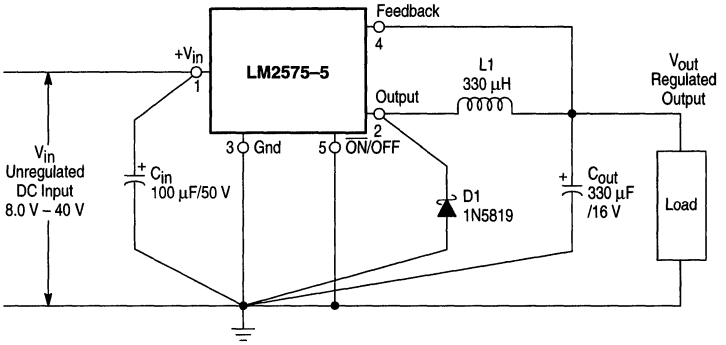


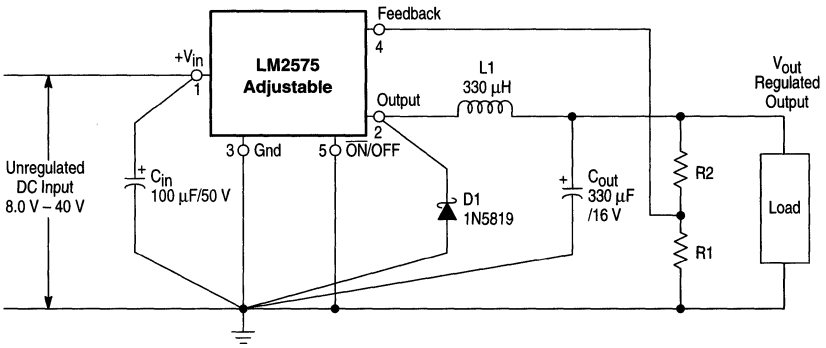
Figure 14. Typical Test Circuit

5.0 Output Voltage Versions



C_{in}	100 µF, 50 V, Aluminium Electrolytic
C_{out}	330 µF, 16 V, Aluminium Electrolytic
D1	Schottky, 1N5819
L1	330 µF, PE–52627 (for 5.0 V in, 3.3 V out, use 100 µH, PE–92108)

Adjustable Output Voltage Versions



$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

$$R2 = R1\left(\frac{V_{out}}{V_{ref}} - 1\right)$$

Where V_{ref} = 1.23 V, R1 between 1.0 kΩ and 5.0 kΩ

PCB LAYOUT GUIDELINES

As in any switching regulator, the layout of the printed circuit board is very important. Rapidly switching currents associated with wiring inductance, stray capacitance and parasitic inductance of the printed circuit board traces can generate voltage transients which can generate electromagnetic interferences (EMI) and affect the desired operation. As indicated in the Figure 14, to minimize inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible. For best results, single–point grounding (as indicated) or ground plane construction should be used.

On the other hand, the PCB area connected to the Pin 2 (emitter of the internal switch) of the LM2575 should be kept to a minimum in order to minimize coupling to sensitive circuitry.

Another sensitive part of the circuit is the feedback. It is important to keep the sensitive feedback wiring short. To assure this, physically locate the programming resistors near to the regulator, when using the adjustable version of the LM2575 regulator.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description (Refer to Figure 1)
1	V_{in}	This pin is the positive input supply for the LM2575 step–down switching regulator. In order to minimize voltage transients and to supply the switching currents needed by the regulator, a suitable input bypass capacitor must be present (C_{in} in Figure 1).
2	Output	This is the emitter of the internal switch. The saturation voltage V_{sat} of this output switch is typically 1.0 V. It should be kept in mind that the PCB area connected to this pin should be kept to a minimum in order to minimize coupling to sensitive circuitry.
3	Gnd	Circuit ground pin. See the information about the printed circuit board layout.
4	Feedback	This pin senses regulated output voltage to complete the feedback loop. The signal is divided by the internal resistor divider network R2, R1 and applied to the non–inverting input of the internal error amplifier. In the Adjustable version of the LM2575 switching regulator this pin is the direct input of the error amplifier and the resistor network R2, R1 is connected externally to allow programming of the output voltage.
5	$\overline{ON}$/OFF	It allows the switching regulator circuit to be shut down using logic level signals, thus dropping the total input supply current to approximately 80 μA. The input threshold voltage is typically 1.4 V. Applying a voltage above this value (up to $+V_{in}$) shuts the regulator off. If the voltage applied to this pin is lower than 1.4 V or if this pin is connected to ground, the regulator will be in the "on" condition.

DESIGN PROCEDURE

Buck Converter Basics

The LM2575 is a "Buck" or Step–Down Converter which is the most elementary forward–mode converter. Its basic schematic can be seen in Figure 15.

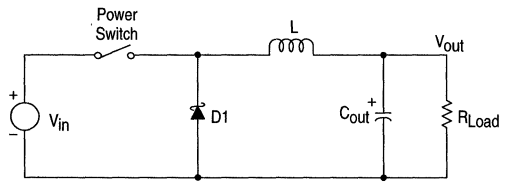
The operation of this regulator topology has two distinct time periods. The first one occurs when the series switch is on, the input voltage is connected to the input of the inductor.

The output of the inductor is the output voltage, and the rectifier (or catch diode) is reverse biased. During this period, since there is a constant voltage source connected across the inductor, the inductor current begins to linearly ramp upwards, as described by the following equation:

$$I_{L(on)} = \frac{(V_{in} - V_{out})\, t_{on}}{L}$$

During this "on" period, energy is stored within the core material in the form of magnetic flux. If the inductor is properly designed, there is sufficient energy stored to carry the requirements of the load during the "off" period.

Figure 15. Basic Buck Converter



The next period is the "off" period of the power switch. When the power switch turns off, the voltage across the inductor reverses its polarity and is clamped at one diode voltage drop below ground by catch dioded. Current now flows through the catch diode thus maintaining the load current loop. This removes the stored energy from the inductor. The inductor current during this time is:

$$I_{L(off)} = \frac{(V_{out} - V_D)\, t_{off}}{L}$$

This period ends when the power switch is once again turned on. Regulation of the converter is accomplished by varying the duty cycle of the power switch. It is possible to describe the duty cycle as follows:

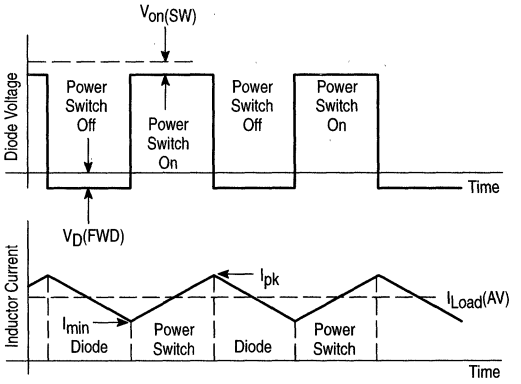
$d = \frac{t_{on}}{T}$, where T is the period of switching.

For the buck converter with ideal components, the duty cycle can also be described as:

$$d = \frac{V_{out}}{V_{in}}$$

Figure 16 shows the buck converter idealized waveforms of the catch diode voltage and the inductor current.

Figure 16. Buck Converter Idealized Waveforms



Procedure (Fixed Output Voltage Version) In order to simplify the switching regulator design, a step–by–step design procedure and example is provided.

Procedure	Example
Given Parameters: V_{out} = Regulated Output Voltage (3.3 V, 5.0 V, 12 V or 15 V) $V_{in(max)}$ = Maximum DC Input Voltage $I_{Load(max)}$ = Maximum Load Current	**Given Parameters:** V_{out} = 5.0 V $V_{in(max)}$ = 20 V $I_{Load(max)}$ = 0.8 A
1. Controller IC Selection According to the required input voltage, output voltage and current, select the appropriate type of the controller IC output voltage version.	**1. Controller IC Selection** According to the required input voltage, output voltage, current polarity and current value, use the LM2575–5 controller IC
2. Input Capacitor Selection (C_{in}) To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin +V_{in} and ground pin Gnd. This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value.	**2. Input Capacitor Selection (C_{in})** A 47 µF, 25 V aluminium electrolytic capacitor located near to the input and ground pins provides sufficient bypassing.
3. Catch Diode Selection (D1) **A.** Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design the diode should have a current rating equal to the maximum current limit of the LM2575 to be able to withstand a continuous output short **B.** The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	**3. Catch Diode Selection (D1)** **A.** For this example the current rating of the diode is 1.0 A. **B.** Use a 30 V 1N5818 Schottky diode, or any of the suggested fast recovery diodes shown in the Table 4.
4. Inductor Selection (L1) **A.** According to the required working conditions, select the correct inductor value using the selection guide from Figures 17 to 21. **B.** From the appropriate inductor selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code. **C.** Select an appropriate inductor from the several different manufacturers part numbers listed in Table 1 or Table 2. When using Table 2 for selecting the right inductor the designer must realize that the inductor current rating must be higher than the maximum peak current flowing through the inductor. This maximum peak current can be calculated as follows: $I_{p(max)} = I_{Load(max)} + \frac{(V_{in} - V_{out})\, t_{on}}{2L}$ where t_{on} is the "on" time of the power switch and $t_{on} = \frac{V_{out}}{V_{in}} \times \frac{1}{f_{osc}}$ For additional information about the inductor, see the inductor section in the "External Components" section of this data sheet.	**4. Inductor Selection (L1)** **A.** Use the inductor selection guide shown in Figures 17 to 21. **B.** From the selection guide, the inductance area intersected by the 20 V line and 0.8 A line is L330. **C.** Inductor value required is 330 µH. From the Table 1 or Table 2, choose an inductor from any of the listed manufacturers.

Procedure (Fixed Output Voltage Version) (continued) In order to simplify the switching regulator design, a step–by–step design procedure and example is provided.

Procedure	Example
5. Output Capacitor Selection (C_{out}) **A.** Since the LM2575 is a forward–mode switching regulator with voltage mode control, its open loop 2–pole–2–zero frequency characteristic has the dominant pole–pair determined by the output capacitor and inductor values. For stable operation and an acceptable ripple voltage, (approximately 1% of the output voltage) a value between 100 μF and 470 μF is recommended. **B.** Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating at least 8V is appropriate, and a 10 V or 16 V rating is recommended.	**5. Output Capacitor Selection (C_{out})** **A.** C_{out} = 100 μF to 470 μF standard aluminium electrolytic. **B.** Capacitor voltage rating = 16 V.

Procedure (Adjustable Output Version: LM2575–Adj)

Procedure	Example
Given Parameters: V_{out} = Regulated Output Voltage $V_{in(max)}$ = Maximum DC Input Voltage $I_{Load(max)}$ = Maximum Load Current	**Given Parameters:** V_{out} = 8.0 V $V_{in(max)}$ = 12 V $I_{Load(max)}$ = 1.0 A
1. Programming Output Voltage To select the right programming resistor R1 and R2 value (see Figure 14) use the following formula: $V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right)$ where V_{ref} = 1.23 V Resistor R1 can be between 1.0 k and 5.0 kΩ. (For best temperature coefficient and stability with time, use 1% metal film resistors). $R2 = R1\left(\frac{V_{out}}{V_{ref}} - 1\right)$	**1. Programming Output Voltage** (selecting R1 and R2) Select R1 and R2: $V_{out} = 1.23\left(1 + \frac{R2}{R1}\right)$ Select R1 = 1.8 kΩ $R2 = R1\left(\frac{V_{out}}{V_{ref}} - 1\right) = 1.8\ k\left(\frac{8.0\ V}{1.23\ V} - 1\right)$ R2 = 9.91 kΩ, choose a 9.88 k metal film resistor.
2. Input Capacitor Selection (C_{in}) To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin +V_{in} and ground pin Gnd This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value. For additional information see input capacitor section in the "External Components" section of this data sheet.	**2. Input Capacitor Selection (C_{in})** A 100 μF aluminium electrolytic capacitor located near the input and ground pin provides sufficient bypassing.
3. Catch Diode Selection (D1) **A.** Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design, the diode should have a current rating equal to the maximum current limit of the LM2575 to be able to withstand a continuous output short. **B.** The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	**3. Catch Diode Selection (D1)** **A.** For this example, a 3.0 A current rating is adequate. **B.** Use a 20 V 1N5820 or MBR320 Schottky diode or any suggested fast recovery diode in the Table 4.

Procedure (Adjustable Output Version: LM2575–Adj) (continued)

Procedure	Example
4. Inductor Selection (L1) **A.** Use the following formula to calculate the inductor Volt x microsecond [V x μs] constant: $E \times T = (V_{in} - V_{out}) \frac{V_{out}}{V_{on}} \times \frac{10^6}{F[Hz]}$ [V x μs] **B.** Match the calculated E x T value with the corresponding number on the vertical axis of the Inductor Value Selection Guide shown in Figure 21. This E x T constant is a measure of the energy handling capability of an inductor and is dependent upon the type of core, the core area, the number of turns, and the duty cycle. **C.** Next step is to identify the inductance region intersected by the E x T value and the maximum load current value on the horizontal axis shown in Figure 21. **D.** From the inductor code, identify the inductor value. Then select an appropriate inductor from the Table 1 or Table 2. The inductor chosen must be rated for a switching frequency of 52 kHz and for a current rating of 1.15 x I_{load}. The inductor current rating can also be determined by calculating the inductor peak current: $I_{p(max)} = I_{Load(max)} + \frac{(V_{in} - V_{out}) t_{on}}{2L}$ where t_{on} is the "on" time of the power switch and $t_{on} = \frac{V_{out}}{V_{in}} \times \frac{1}{f_{osc}}$ For additional information about the inductor, see the inductor section in the "External Components" section of this data sheet.	**4. Inductor Selection (L1)** **A.** Calculate E x T [V x μs] constant: $E \times T = (12 - 8.0) \times \frac{8.0}{12} \times \frac{1000}{52} = 51$ [V x μs] **B.** E x T = 51 [V x μs] **C.** $I_{Load(max)}$ = 1.0 A Inductance Region = L220 **D.** Proper inductor value = 220 μH Choose the inductor from the Table 1 or Table 2.
5. Output Capacitor Selection (C_{out}) **A.** Since the LM2575 is a forward–mode switching regulator with voltage mode control, its open loop 2–pole–2–zero frequency characteristic has the dominant pole–pair determined by the output capacitor and inductor values. For stable operation, the capacitor must satisfy the following requirement: $C_{out} \geq 7.785 \frac{V_{in(max)}}{V_{out} \times L\ [\mu H]}$ [μF] **B.** Capacitor values between 10 μF and 2000 μF will satisfy the loop requirements for stable operation. To achieve an acceptable output ripple voltage and transient response, the output capacitor may need to be several times larger than the above formula yields. **C.** Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating of at least 8V is appropriate, and a 10 V or 16 V rating is recommended.	**5. Output Capacitor Selection (C_{out})** **A.** $C_{out} \geq 7.785 \frac{12}{8.220} = 53$ μF To achieve an acceptable ripple voltage, select C_{out} = 100 μF electrolytic capacitor.

INDUCTOR VALUE SELECTION GUIDE

3

Figure 17. LM2575–3.3

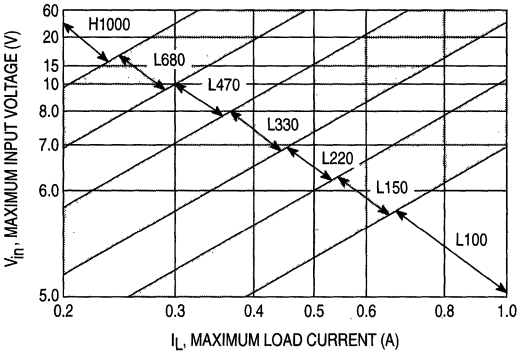


Figure 18. LM2575–5.0

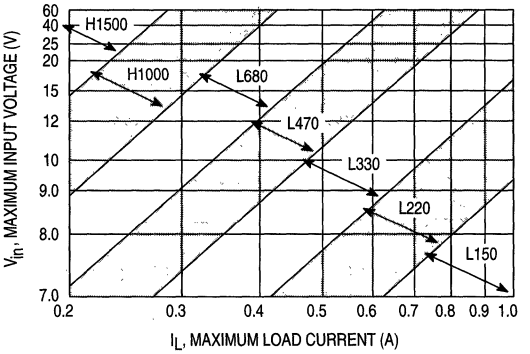


Figure 19. LM2575–12

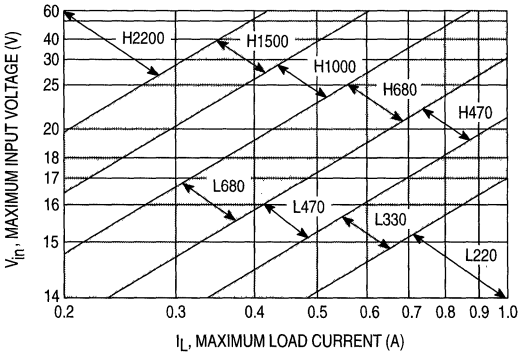


Figure 20. LM2575–15

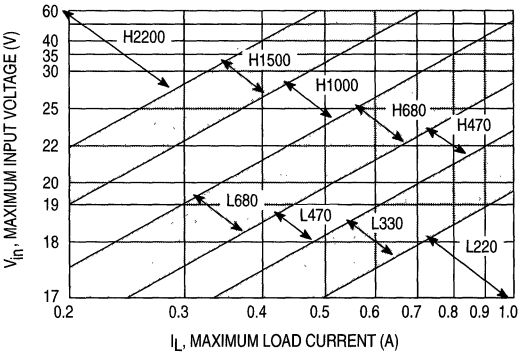
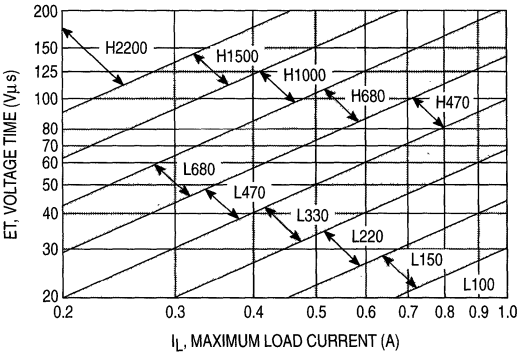


Figure 21. LM2575–Adj



NOTE: This Inductor Value Selection Guide is applicable for continuous mode only.

Table 1. Inductor Selection Guide

Inductor Code	Inductor Value	Pulse Eng	Renco	AIE	Tech 39
L100	100 μH	PE–92108	RL2444	415–0930	77 308 BV
L150	150 μH	PE–53113	RL1954	415–0953	77 358 BV
L220	220 μH	PE–52626	RL1953	415–0922	77 408 BV
L330	330 μH	PE–52627	RL1952	415–0926	77 458 BV
L470	470 μH	PE–53114	RL1951	415–0927	–
L680	680 μH	PE–52629	RL1950	415–0928	77 508 BV
H150	150 μH	PE–53115	RL2445	415–0936	77 368 BV
H220	220 μH	PE–53116	RL2446	430–0636	77 410 BV
H330	330 μH	PE–53117	RL2447	430–0635	77 460 BV
H470	470 μH	PE–53118	RL1961	430–0634	–
H680	680 μH	PE–53119	RL1960	415–0935	77 510 BV
H1000	1000 μH	PE–53120	RL1959	415–0934	77 558 BV
H1500	1500 μH	PE–53121	RL1958	415–0933	–
H2200	2200 μH	PE–53122	RL2448	415–0945	77 610 BV

Table 2. Inductor Selection Guide

Inductance	Current	Schott		Renco		Pulse Engineering		Coilcraft
(μH)	(A)	THT	SMT	THT	SMT	THT	SMT	SMT
68	0.32	67143940	67144310	RL–1284–68–43	RL1500–68	PE–53804	PE–53804–S	DO1608–68
	0.58	67143990	67144360	RL–5470–6	RL1500–68	PE–53812	PE–53812–S	DO3308–683
	0.99	67144070	67144450	RL–5471–5	RL1500–68	PE–53821	PE–53821–S	DO3316–683
	1.78	67144140	67144520	RL–5471–5	–	PE–53830	PE–53830–S	DO5022P–683
100	0.48	67143980	67144350	RL–5470–5	RL1500–100	PE–53811	PE–53811–S	DO3308–104
	0.82	67144060	67144440	RL–5471–4	RL1500–100	PE–53820	PE–53820–S	DO3316–104
	1.47	67144130	67144510	RL–5471–4	–	PE–53829	PE–53829–S	DO5022P–104
150	0.39	–	67144340	RL–5470–4	RL1500–150	PE–53810	PE–53810–S	DO3308–154
	0.66	67144050	67144430	RL–5471–3	RL1500–150	PE–53819	PE–53819–S	DO3316–154
	1.20	67144120	67144500	RL–5471–3	–	PE–53828	PE–53828–S	DO5022P–154
220	0.32	67143960	67144330	RL–5470–3	RL1500–220	PE–53809	PE–53809–S	DO3308–224
	0.55	67144040	67144420	RL–5471–2	RL1500–220	PE–53818	PE–53818–S	DO3316–224
	1.00	67144110	67144490	RL–5471–2	–	PE–53827	PE–53827–S	DO5022P–224
330	0.42	67144030	67144410	RL–5471–1	RL1500–330	PE–53817	PE–53817–S	DO3316–334
	0.80	67144100	67144480	RL–5471–1	–	PE–53826	PE–53826–S	DO5022P–334

NOTE: Table 1 and Table 2 of this Indicator Selection Guide shows some examples of different manufacturer products suitable for design with the LM2575.

Table 3. Example of Several Inductor Manufacturers Phone/Fax Numbers

Pulse Engineering Inc.	Phone Fax	+ 1–619–674–8100 + 1–619–674–8262
Pulse Engineering Inc. Europe	Phone Fax	+ 353 93 24 107 + 353 93 24 459
Renco Electronics Inc.	Phone Fax	+ 1–516–645–5828 + 1–516–586–5562
AIE Magnetics	Phone Fax	+ 1–813–347–2181
Coilcraft Inc.	Phone Fax	+ 1–708–322–2645 + 1–708–639–1469
Coilcraft Inc., Europe	Phone Fax	+ 44 1236 730 595 + 44 1236 730 627
Tech 39	Phone Fax	+ 33 8425 2626 + 33 8425 2610
Schott Corp.	Phone Fax	+ 1–612–475–1173 + 1–612–475–1786

Table 4. Diode Selection Guide gives an overview about both surface–mount and through–hole diodes for an effective design. Device listed in bold are available from Motorola.

	Schottky				**Ultra–Fast Recovery**			
	1.0 A		**3.0 A**		**1.0 A**		**3.0 A**	
V_R	**SMT**	**THT**	**SMT**	**THT**	**SMT**	**THT**	**SMT**	**THT**
20 V	SK12	**1N5817** SR102	SK32 **MBRD320**	**1N5820** **MBR320** SR302				
30 V	**MBRS130LT3** SK13	**1N5818** SR103 11DQ03	SK33 **MBRD330**	**1N5821** **MBR330** SR303 31DQ03	**MURS120T3**	**MUR120** 11DF1 HER102	**MURS320T3**	
40 V	**MBRS140T3** SK14 10BQ040 10MQ040	**1N5819** SR104 11DQ04	**MBRS340T3** **MBRD340** 30WQ04 SK34	**1N5822** **MBR340** SR304 31DQ04	10BF10		**MURD320**	**MUR320** 30WF10 **MUR420**
50 V	**MBRS150** 10BQ050	**MBR150** SR105 11DQ05	**MBRD350** SK35 30WQ05	**MBR350** SR305 11DQ05			31DF1 HER302	

EXTERNAL COMPONENTS

Input Capacitor (C_{in})

The Input Capacitor Should Have a Low ESR

For stable operation of the switch mode converter a low ESR (Equivalent Series Resistance) aluminium or solid tantalum bypass capacitor is needed between the input pin and the ground pin to prevent large voltage transients from appearing at the input. It must be located near the regulator and use short leads. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures. For reliable operation in temperatures below –25°C larger values of the input capacitor may be needed. Also paralleling a ceramic or solid tantalum capacitor will increase the regulator stability at cold temperatures.

RMS Current Rating of C_{in}

The important parameter of the input capacitor is the RMS current rating. Capacitors that are physically large and have large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating. The consequence of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. In order to assure maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be:

$$I_{rms} > 1.2 \times d \times I_{Load}$$

where d is the duty cycle, for a buck regulator

$$d = \frac{t_{on}}{T} = \frac{V_{out}}{V_{in}}$$

and $d = \frac{t_{on}}{T} = \frac{|V_{out}|}{|V_{out}| + V_{in}}$ for a buck–boost regulator.

Output Capacitor (C_{out})

For low output ripple voltage and good stability, low ESR output capacitors are recommended. An output capacitor has two main functions: it filters the output and provides regulator loop stability. The ESR of the output capacitor and the peak–to–peak value of the inductor ripple current are the main factors contributing to the output ripple voltage value.Standard aluminium electrolytics could be adequate for some applications but for quality design low ESR types are recommended.

An aluminium electrolytic capacitor's ESR value is related to many factors such as the capacitance value, the voltage rating, the physical size and the type of construction. In most cases, the higher voltage electrolytic capacitors have lower ESR value. Often capacitors with much higher voltage ratings may be needed to provide low ESR values that are required for low output ripple voltage.

The Output Capacitor Requires an ESR Value That Has an Upper and Lower Limit

As mentioned above, a low ESR value is needed for low output ripple voltage, typically 1% to 2% of the output voltage. But if the selected capacitor's ESR is extremely low (below 0.05 Ω), there is a possibility of an unstable feedback loop, resulting in oscillation at the output. This situation can occur when a tantalum capacitor, that can have a very low ESR, is used as the only output capacitor.

At Low Temperatures, Put in Parallel Aluminium Electrolytic Capacitors with Tantalum Capacitors

Electrolytic capacitors are not recommended for temperatures below –25°C. The ESR rises dramatically at cold temperatures and typically rises 3 times at –25°C and as much as 10 times at –40°C. Solid tantalum capacitors have much better ESR spec at cold temperatures and are recommended for temperatures below –25°C. They can be also used in parallel with aluminium electrolytics. The value of the tantalum capacitor should be about 10% or 20% of the total capacitance. The output capacitor should have at least 50% higher RMS ripple current rating at 52 kHz than the peak–to–peak inductor ripple current.

Catch Diode

Locate the Catch Diode Close to the LM2575

The LM2575 is a step–down buck converter; it requires a fast diode to provide a return path for the inductor current when the switch turns off. This diode must be located close to the LM2575 using short leads and short printed circuit traces to avoid EMI problems.

Use a Schottky or a Soft Switching Ultra–Fast Recovery Diode

Since the rectifier diodes are very significant source of losses within switching power supplies, choosing the rectifier that best fits into the converter design is an important process. Schottky diodes provide the best performance because of their fast switching speed and low forward voltage drop.

They provide the best efficiency especially in low output voltage applications (5.0 V and lower). Another choice could be Fast–Recovery, or Ultra–Fast Recovery diodes. It has to be noted, that some types of these diodes with an abrupt turnoff characteristic may cause instability or EMI troubles.

A fast–recovery diode with soft recovery characteristics can better fulfill a quality, low noise design requirements. Table 4 provides a list of suitable diodes for the LM2575 regulator. Standard 50/60 Hz rectifier diodes such as the 1N4001 series or 1N5400 series are **NOT** suitable.

Inductor

The magnetic components are the cornerstone of all switching power supply designs. The style of the core and the winding technique used in the magnetic component's design has a great influence on the reliability of the overall power supply.

Using an improper or poorly designed inductor can cause high voltage spikes generated by the rate of transitions in current within the switching power supply, and the possibility of core saturation can arise during an abnormal operational mode. Voltage spikes can cause the semiconductors to enter avalanche breakdown and the part can instantly fail if enough energy is applied. It can also cause significant RFI (Radio Frequency Interference) and EMI (Electro–Magnetic Interference) problems.

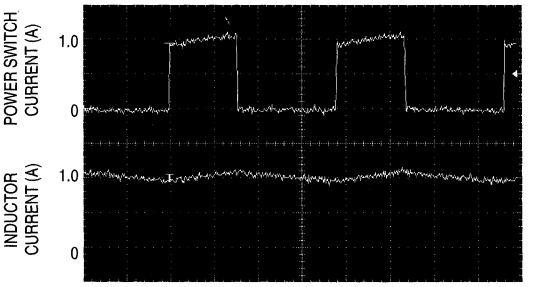
Continuous and Discontinuous Mode of Operation

The LM2575 step–down converter can operate in both the continuous and the discontinuous modes of operation. The regulator works in the continuous mode when loads are relatively heavy, the current flows through the inductor continuously and never falls to zero. Under light load

conditions, the circuit will be forced to the discontinuous mode when inductor current falls to zero for certain period of time (see Figure 22 and Figure 23). Each mode has distinctively different operating characteristics, which can affect the regulator performance and requirements. In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak currents in the switch, inductor and diode, and can have a lower output ripple voltage. On the other hand it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.

To simplify the inductor selection process, an inductor selection guide for the LM2575 regulator was added to this data sheet (Figures 17 through 21). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak–to–peak inductor ripple current to be a certain percentage of the maximum design load current. This percentage is allowed to change as different design load currents are selected. For light loads (less than approximately 200 mA) it may be desirable to operate the regulator in the discontinuous mode, because the inductor value and size can be kept relatively low. Consequently, the percentage of inductor peak–to–peak current increases. This discontinuous mode of operation is perfectly acceptable for this type of switching converter. Any buck regulator will be forced to enter discontinuous mode if the load current is light enough.

Figure 22. Continuous Mode Switching Current Waveforms



HORTIZONTAL TIME BASE: 5.0 µs/DIV

Selecting the Right Inductor Style

Some important considerations when selecting a core type are core material, cost, the output power of the power supply, the physical volume the inductor must fit within, and the amount of EMI (Electro–Magnetic Interference) shielding that the core must provide. The inductor selection guide covers different styles of inductors, such as pot core, E–core, toroid and bobbin core, as well as different core materials such as ferrites and powdered iron from different manufacturers.

For high quality design regulators the toroid core seems to be the best choice. Since the magnetic flux is completely contained within the core, it generates less EMI, reducing noise problems in sensitive circuits. The least expensive is the bobbin core type, which consists of wire wound on a ferrite rod core. This type of inductor generates more EMI due to the fact that its core is open, and the magnetic flux is not completely contained within the core.

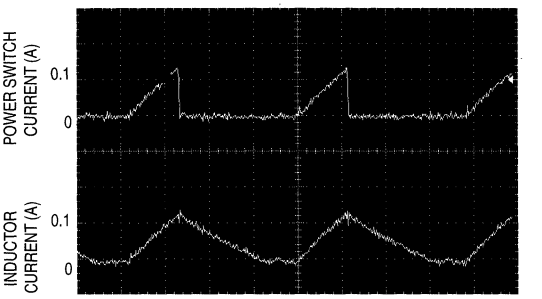
When multiple switching regulators are located on the same printed circuit board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents due to mutual coupling. A toroid, pot core or E–core (closed magnetic structure) should be used in such applications.

Do Not Operate an Inductor Beyond its Maximum Rated Current

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. Core saturation occurs when the flux density is too high and consequently the cross sectional area of the core can no longer support additional lines of magnetic flux.

This causes the permeability of the core to drop, the inductance value decreases rapidly and the inductor begins to look mainly resistive. It has only the dc resistance of the winding. This can cause the switch current to rise very rapidly and force the LM2575 internal switch into cycle–by–cycle current limit, thus reducing the dc output load current. This can also result in overheating of the inductor and/or the LM2575. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.

Figure 23. Discontinuous Mode Switching Current Waveforms



HORTIZONTAL TIME BASE: 5.0 µs/DIV

GENERAL RECOMMENDATIONS

Output Voltage Ripple and Transients

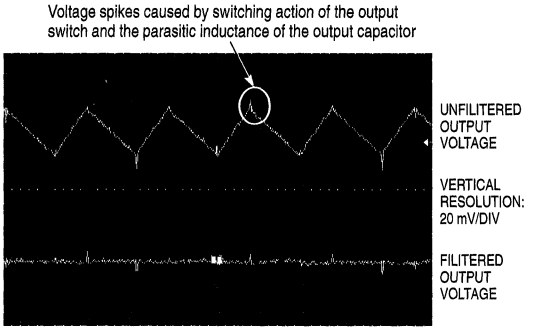
Source of the Output Ripple

Since the LM2575 is a switch mode power supply regulator, its output voltage, if left unfiltered, will contain a sawtooth ripple voltage at the switching frequency. The output ripple voltage value ranges from 0.5% to 3% of the output voltage. It is caused mainly by the inductor sawtooth ripple current multiplied by the ESR of the output capacitor.

Short Voltage Spikes and How to Reduce Them

The regulator output voltage may also contain short voltage spikes at the peaks of the sawtooth waveform (see Figure 24). These voltage spikes are present because of the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. There are some other important factors such as wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all these contribute to the amplitude of these spikes. To minimise these voltage spikes, low inductance capacitors should be used, and their lead lengths must be kept short. The importance of quality printed circuit board layout design should also be highlighted.

Figure 24. Output Ripple Voltage Waveforms



Minimizing the Output Ripple

In order to minimise the output ripple voltage it is possible to enlarge the inductance value of the inductor L1 and/or to use a larger value output capacitor. There is also another way to smooth the output by means of an additional LC filter (20 µH, 100 µF), that can be added to the output (see Figure 33) to further reduce the amount of output ripple and transients. With such a filter it is possible to reduce the output ripple voltage transients 10 times or more. Figure 24 shows the difference between filtered and unfiltered output waveforms of the regulator shown in Figure 33.

The upper waveform is from the normal unfiltered output of the converter, while the lower waveform shows the output ripple voltage filtered by an additional LC filter.

Heatsinking and Thermal Considerations

The Through–Hole Package TO–220

The LM2575 is available in two packages, a 5–pin TO–220(T, TV) and a 5–pin surface mount D^2PAK(D2T). There are many applications that require no heatsink to keep the LM2575 junction temperature within the allowed operating range. The TO–220 package can be used without a heatsink for ambient temperatures up to approximately 50°C (depending on the output voltage and load current). Higher ambient temperatures require some heatsinking, either to the printed circuit (PC) board or an external heatsink.

The Surface Mount Package D^2PAK and its Heatsinking

The other type of package, the surface mount D^2PAK, is designed to be soldered to the copper on the PC board. The copper and the board are the heatsink for this package and the other heat producing components, such as the catch diode and inductor. The PC board copper area that the package is soldered to should be at least 0.4 in^2 (or 100 mm^2) and ideally should have 2 or more square inches (1300 mm^2) of 0.0028 inch copper. Additional increasing of copper area beyond approximately 3.0 in^2 (2000 mm^2) will not improve heat dissipation significantly. If further thermal improvements are needed, double sided or multilayer PC boards with large copper areas should be considered.

Thermal Analysis and Design

The following procedure must be performed to determine whether or not a heatsink will be required. First determine:

1. $P_{D(max)}$ maximum regulator power dissipation in the application.
2. $T_{A(max)}$ maximum ambient temperature in the application.
3. $T_{J(max)}$ maximum allowed junction temperature (125°C for the LM2575). For a conservative design, the maximum junction temperature should not exceed 110°C to assure safe operation. For every additional 10°C temperature rise that the junction must withstand, the estimated operating lifetime of the component is halved.
4. $R_{\theta JC}$ package thermal resistance junction–case.
5. $R_{\theta JA}$ package thermal resistance junction–ambient.

(Refer to Absolute Maximum Ratings in this data sheet or $R_{\theta JC}$ and $R_{\theta JA}$ values).

The following formula is to calculate the total power dissipated by the LM2575:

$$P_D = (V_{in} \times I_Q) + d \times I_{Load} \times V_{sat}$$

where d is the duty cycle and for buck converter

$$d = \frac{t_{on}}{T} = \frac{V_O}{V_{in}},$$

I_Q (quiescent current) and V_{sat} can be found in the LM2575 data sheet,
V_{in} is minimum input voltage applied,
V_O is the regulator output voltage,
I_{Load} is the load current.

The dynamic switching losses during turn–on and turn–off can be neglected if proper type catch diode is used.

Packages Not on a Heatsink (Free–Standing)

For a free–standing application when no heatsink is used, the junction temperature can be determined by the following expression:

$$T_J = (R_{\theta JA})(P_D) + T_A$$

where $(R_{\theta JA})(P_D)$ represents the junction temperature rise caused by the dissipated power and T_A is the maximum ambient temperature.

Packages on a Heatsink

If the actual operating junction temperature is greater than the selected safe operating junction temperature determined in step 3, than a heatsink is required. The junction temperature will be calculated as follows:

$$T_J = P_D (R_{\theta JA} + R_{\theta CS} + R_{\theta SA}) + T_A$$

where $R_{\theta JC}$ is the thermal resistance junction–case,
$R_{\theta CS}$ is the thermal resistance case–heatsink,
$R_{\theta SA}$ is the thermal resistance heatsink–ambient.

If the actual operating temperature is greater than the selected safe operating junction temperature, then a larger heatsink is required.

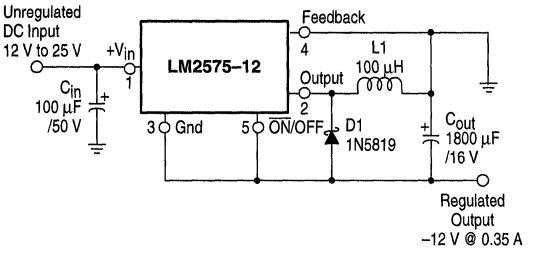
Some Aspects That can Influence Thermal Design

It should be noted that the package thermal resistance and the junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers, such as PC board size, shape, thickness, physical position, location, board temperature, as well as whether the surrounding air is moving or still.

Other factors are trace width, total printed circuit copper area, copper thickness, single– or double–sided, multilayer board, the amount of solder on the board or even colour of the traces.

The size, quantity and spacing of other components on the board can also influence its effectiveness to dissipate the heat.

Figure 25. Inverting Buck–Boost Regulator Using the LM2575–12 Develops –12 V @ 0.35 A



ADDITIONAL APPLICATIONS

Inverting Regulator

An inverting buck–boost regulator using the LM2575–12 is shown in Figure 25. This circuit converts a positive input voltage to a negative output voltage with a common ground by bootstrapping the regulators ground to the negative output voltage. By grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.

In this example the LM2575–12 is used to generate a –12 V output. The maximum input voltage in this case cannot exceed +28 V because the maximum voltage appearing across the regulator is the absolute sum of the input and output voltages and this must be limited to a maximum of 40 V.

This circuit configuration is able to deliver approximately 0.35 A to the output when the input voltage is 12 V or higher. At lighter loads the minimum input voltage required drops to approximately 4.7 V, because the buck–boost regulator topology can produce an output voltage that, in its absolute value, is either greater or less than the input voltage.

Since the switch currents in this buck–boost configuration are higher than in the standard buck converter topology, the available output current is lower.

This type of buck–boost inverting regulator can also require a larger amount of startup input current, even for light loads. This may overload an input power source with a current limit less than 1.5 A.

Such an amount of input startup current is needed for at least 2.0 ms or more. The actual time depends on the output voltage and size of the output capacitor.

Because of the relatively high startup currents required by this inverting regulator topology, the use of a delayed startup or an undervoltage lockout circuit is recommended.

Using a delayed startup arrangement, the input capacitor can charge up to a higher voltage before the switch–mode regulator begins to operate.

The high input current needed for startup is now partially supplied by the input capacitor C_{in}.

Design Recommendations:

The inverting regulator operates in a different manner than the buck converter and so a different design procedure has to be used to select the inductor L1 or the output capacitor C_{out}.

The output capacitor values must be larger than is normally required for buck converter designs. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of µF).

The recommended range of inductor values for the inverting converter design is between 68 µH and 220 µH. To select an inductor with an appropriate current rating, the inductor peak current has to be calculated.

The following formula is used to obtain the peak inductor current:

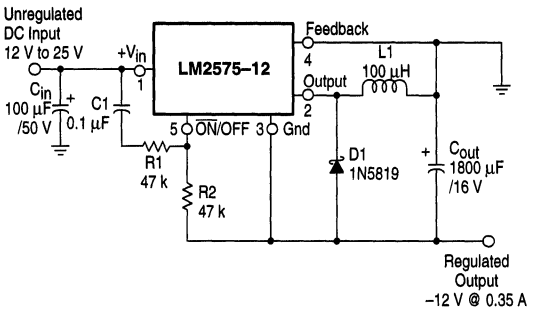
$$I_{peak} \approx \frac{I_{Load}\,(V_{in} + |V_O|)}{V_{in}} + \frac{V_{in} \times t_{on}}{2L_1}$$

where $t_{on} = \dfrac{|V_O|}{V_{in} + |V_O|} \times \dfrac{1}{f_{osc}}$, and f_{osc} = 52 kHz.

Under normal continuous inductor current operating conditions, the worst case occurs when V_{in} is minimal.

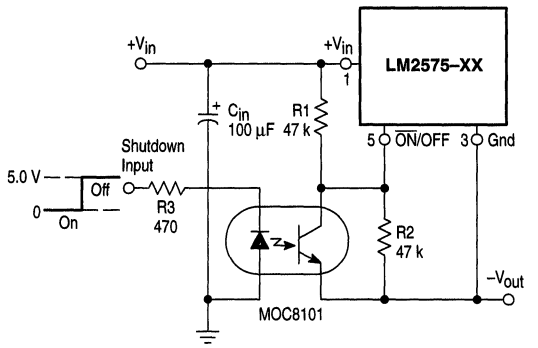
Note that the voltage appearing across the regulator is the absolute sum of the input and output voltage, and must not exceed 40 V.

Figure 26. Inverting Buck–Boost Regulator with Delayed Startup



It has been already mentioned above, that in some situations, the delayed startup or the undervoltage lockout features could be very useful. A delayed startup circuit applied to a buck–boost converter is shown in Figure 26. Figure 31 in the "Undervoltage Lockout" section describes an undervoltage lockout feature for the same converter topology.

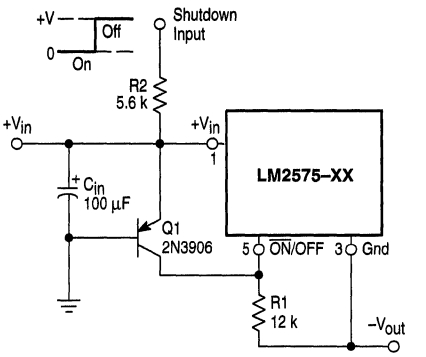
Figure 27. Inverting Buck–Boost Regulator Shut Down Circuit Using an Optocoupler



NOTE: This picture does not show the complete circuit.

With the inverting configuration, the use of the $\overline{ON}$/OFF pin requires some level shifting techniques. This is caused by the fact, that the ground pin of the converter IC is no longer at ground. Now, the $\overline{ON}$/OFF pin threshold voltage (1.4 V approximately) has to be related to the negative output voltage level. There are many different possible shut down methods, two of them are shown in Figures 27 and 28.

Figure 28. Inverting Buck–Boost Regulator Shut Down Circuit Using a PNP Transistor



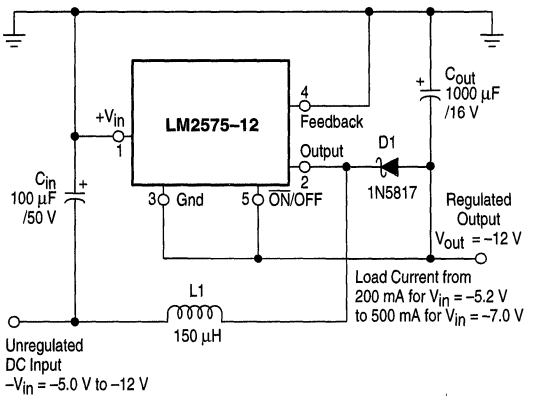
NOTE: This picture does not show the complete circuit.

Negative Boost Regulator

This example is a variation of the buck–boost topology and is called a negative boost regulator. This regulator experiences relatively high switch current, especially at low input voltages. The internal switch current limiting results in lower output load current capability.

The circuit in Figure 29 shows the negative boost configuration. The input voltage in this application ranges from –5.0 V to –12 V and provides a regulated –12 V output. If the input voltage is greater than –12 V, the output will rise above –12 V accordingly, but will not damage the regulator.

Figure 29. Negative Boost Regulator



Design Recommendations:

The same design rules as for the previous inverting buck–boost converter can be applied. The output capacitor C_{out} must be chosen larger than would be required for a standard buck converter. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of μF). The recommended range of inductor values for the negative boost regulator is the same as for inverting converter design.

Another important point is that these negative boost converters cannot provide current limiting load protection in the event of a short in the output so some other means, such as a fuse, may be necessary to provide the load protection.

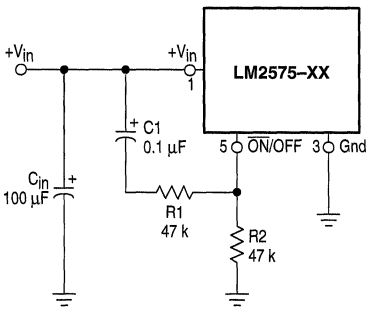
Delayed Startup

There are some applications, like the inverting regulator already mentioned above, which require a higher amount of startup current. In such cases, if the input power source is limited, this delayed startup feature becomes very useful.

To provide a time delay between the time the input voltage is applied and the time when the output voltage comes up, the circuit in Figure 30 can be used. As the input voltage is applied, the capacitor C1 charges up, and the voltage across the resistor R2 falls down. When the voltage on the $\overline{ON}$/OFF pin falls below the threshold value 1.4 V, the regulator starts up. Resistor R1 is included to limit the maximum voltage applied to the $\overline{ON}$/OFF pin, reduces the power supply noise sensitivity, and also limits the capacitor C1 discharge current, but its use is not mandatory.

When a high 50 Hz or 60 Hz (100 Hz or 120 Hz respectively) ripple voltage exists, a long delay time can cause some problems by coupling the ripple into the $\overline{ON}$/OFF pin, the regulator could be switched periodically on and off with the line (or double) frequency.

Figure 30. Delayed Startup Circuitry



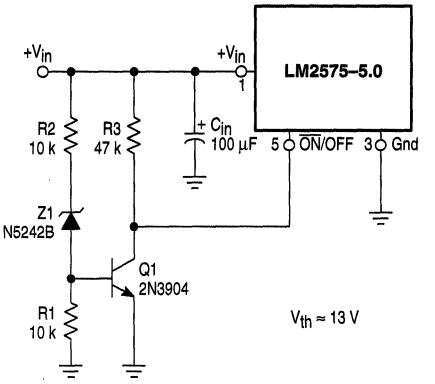
NOTE: This picture does not show the complete circuit.

Undervoltage Lockout

Some applications require the regulator to remain off until the input voltage reaches a certain threshold level. Figure 31 shows an undervoltage lockout circuit applied to a buck regulator. A version of this circuit for buck–boost converter is shown in Figure 32. Resistor R3 pulls the $\overline{ON}$/OFF pin high and keeps the regulator off until the input voltage reaches a predetermined threshold level, which is determined by the following expression:

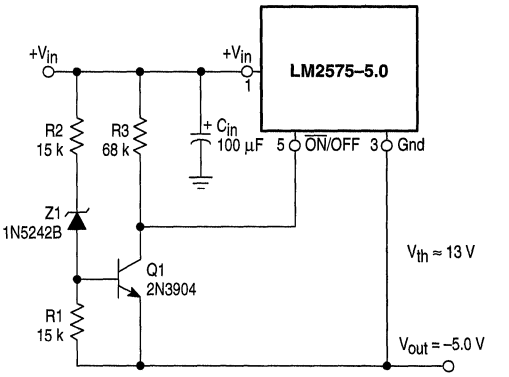
$$V_{th} \approx V_{Z1} + \left(1 + \frac{R2}{R1}\right) V_{BE\,(Q1)}$$

Figure 31. Undervoltage Lockout Circuit for Buck Converter



NOTE: This picture does not show the complete circuit.

Figure 32. Undervoltage Lockout Circuit for Buck–Boost Converter



NOTE: This picture does not show the complete circuit.

Adjustable Output, Low–Ripple Power Supply

A 1.0 A output current capability power supply that features an adjustable output voltage is shown in Figure 33.

This regulator delivers 1.0 A into 1.2 V to 35 V output. The input voltage ranges from roughly 8.0 V to 40 V. In order to achieve a 10 or more times reduction of output ripple, an additional L–C filter is included in this circuit.

Figure 33. Adjustable Power Supply with Low Ripple Voltage

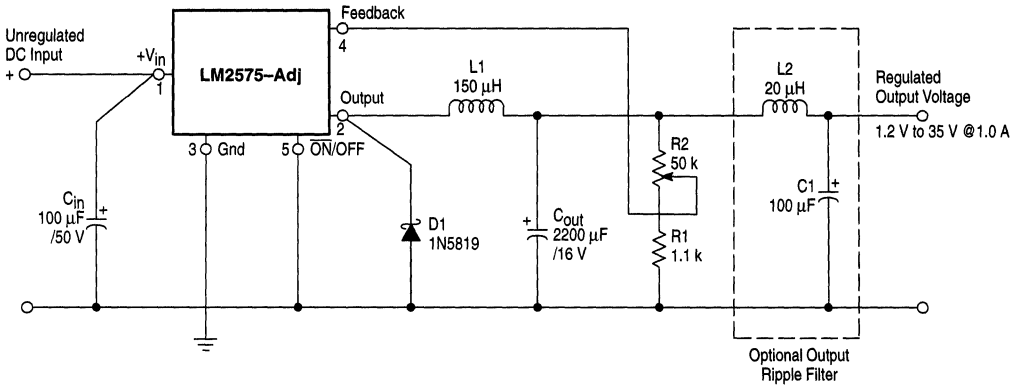
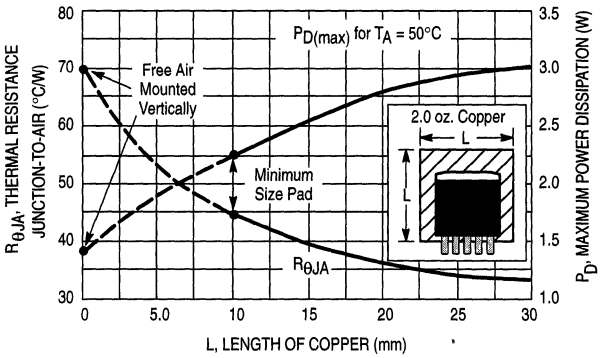
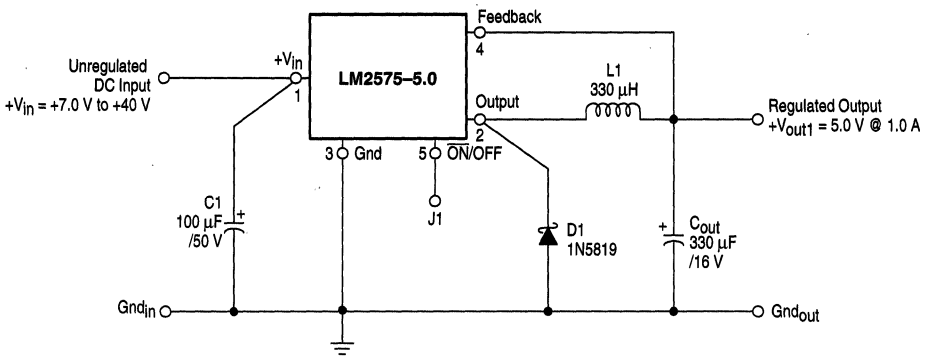


Figure 34. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



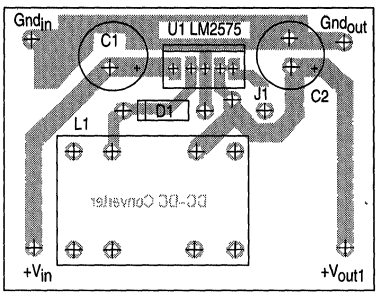
THE LM2575–5.0 STEP–DOWN VOLTAGE REGULATOR WITH 5.0 V @ 1.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH–HOLE PC BOARD LAYOUT

Figure 35. Schematic Diagram of the LM2575–5.0 Step–Down Converter



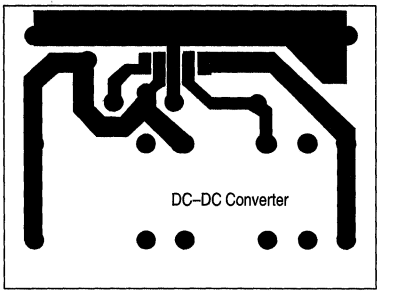
C1 – 100 µF, 50 V, Aluminium Electrolytic
C2 – 330 µF, 16 V, Aluminium Electrolytic
D1 – 1.0 A, 40 V, Schottky Rectifier, 1N5819
L1 – 330 µH, Tech 39: 77 458 BV, Toroid Core, Through–Hole, Pin 3 = Start, Pin 7 = Finish

Figure 36. Printed Circuit Board Component Side



NOTE: Not to scale.

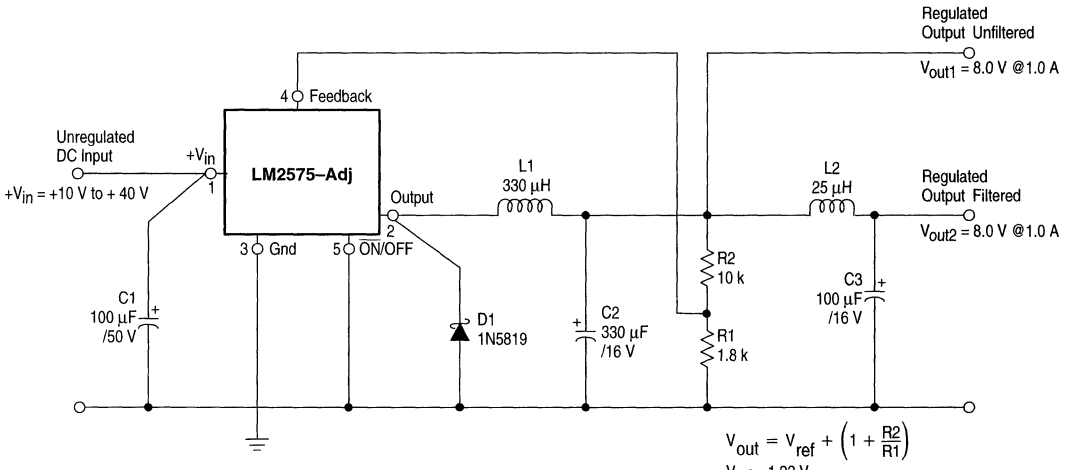
Figure 37. Printed Circuit Board Copper Side



NOTE: Not to scale.

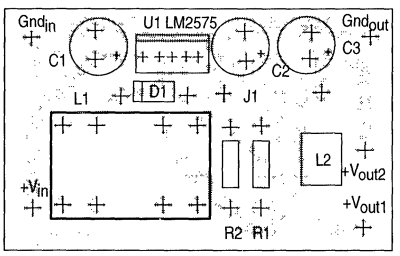
THE LM2575–ADJ STEP–DOWN VOLTAGE REGULATOR WITH 8.0 V @ 1.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH–HOLE PC BOARD LAYOUT

Figure 38. Schematic Diagram of the 8.0 V @ 1.0 V Step–Down Converter Using the LM2575–Adj
(An additional LC filter is included to achieve low output ripple voltage)



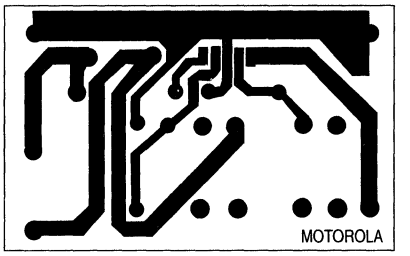
C1 – 100 µF, 50 V, Aluminium Electrolytic
C2 – 330 µF, 16 V, Aluminium Electrolytic
C3 – 100 µF, 16 V, Aluminium Electrolytic
D1 – 1.0 A, 40 V, Schottky Rectifier, 1N5819
L1 – 330 µH, Tech 39: 77 458 BV, Toroid Core, Through–Hole, Pin 3 = Start, Pin 7 = Finish
L2 – 25 µH, TDK: SFT52501, Toroid Core, Through–Hole
R1 – 1.8 k
R2 – 10 k

Figure 39. PC Board Component Side



NOTE: Not to scale.

Figure 40. PC Board Copper Side



NOTE: Not to scale.

References

- National Semiconductor LM2575 Data Sheet and Application Note
- National Semiconductor LM2595 Data Sheet and Application Note
- Marty Brown "Pratical Switching Power Supply Design", Academic Press, Inc., San Diego 1990
- Ray Ridley "High Frequency Magnetics Design", Ridley Engineering, Inc. 1995

LM2931 Series

3

Low Dropout Voltage Regulators

LOW DROPOUT VOLTAGE REGULATORS

The LM2931 series consists of positive fixed and adjustable output voltage regulators that are specifically designed to maintain proper regulation with an extremely low input–to–output voltage differential. These devices are capable of supplying output currents in excess of 100 mA and feature a low bias current of 0.4 mA at 10 mA output.

Designed primarily to survive in the harsh automotive environment, these devices will protect all external load circuitry from input fault conditions caused by reverse battery connection, two battery jump starts, and excessive line transients during load dump. This series also includes internal current limiting, thermal shutdown, and additionally, is able to withstand temporary power–up with mirror–image insertion.

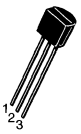
Due to the low dropout voltage and bias current specifications, the LM2931 series is ideally suited for battery powered industrial and consumer equipment where an extension of useful battery life is desirable. The 'C' suffix adjustable output regulators feature an output inhibit pin which is extremely useful in microprocessor–based systems.

- Input–to–Output Voltage Differential of < 0.6 V @ 100 mA
- Output Current in Excess of 100 mA
- Low Bias Current
- 60 V Load Dump Protection
- –50 V Reverse Transient Protection
- Internal Current Limiting with Thermal Shutdown
- Temporary Mirror–Image Protection
- Ideally Suited for Battery Powered Equipment
- Economical 5–Lead TO–220 Package with Two Optional Leadforms
- Available in Surface Mount SOP–8, D^{2}PAK and DPAK Packages

(See Following Page for Ordering Information.)

FIXED OUTPUT VOLTAGE

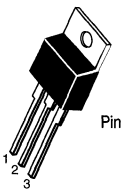
Z SUFFIX
PLASTIC PACKAGE
CASE 29



Pin 1. Output
2. Ground
3. Input

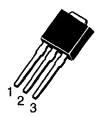
T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface connected to Pin 2.



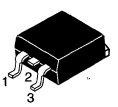
Pin 1. Input
2. Ground
3. Output

DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)



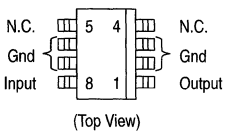
DT–1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D^{2}PAK)



Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

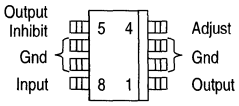
FIXED



(Top View)

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)

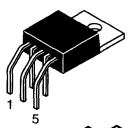
ADJUSTABLE



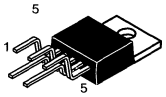
(Top View)

ADJUSTABLE OUTPUT VOLTAGE

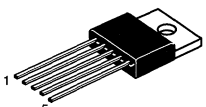
TH SUFFIX
PLASTIC PACKAGE
CASE 314A



TV SUFFIX
PLASTIC PACKAGE
CASE 314B

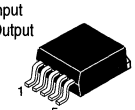


T SUFFIX
PLASTC PACKAGE
CASE 314D



Heatsink surface connected to Pin 3.

Pin 1. Adjust
2. Output Inhibit
3. Ground
4. Input
5. Output



D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^{2}PAK)

Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3.

ORDERING INFORMATION

Device	Output Voltage	Output Tolerance	Case	Package
LM2931AD–5.0	5.0 V	± 3.8%	751	SOP–8 Surface Mount
LM2931ADT–5.0			369A	Surface Mount DPAK
LM2931ADT–1–5.0			369	DPAK
LM2931AD2T–5.0			936	Surface Mount D^2PAK
LM2931AT–5.0			221A	TO–220 Type
LM2931AZ–5.0			29	TO–92 Type
LM2931D–5.0		± 5.0%	751	SOP–8 Surface Mount
LM2931D2T–5.0			936	Surface Mount D^2PAK
LM2931DT–5.0			369A	Surface Mount DPAK
LM2931DT–1–5.0			369	DPAK
LM2931T–5.0			221A	TO–220 Type
LM2931Z–5.0			29	TO–92 Type
LM2931CD	Adjustable		751	SOP–8 Surface Mount
LM2931CD2T			936A	Surface Mount D^2PAK
LM2931CT			314D	5–Pin TO–220 Type
LM2931CTH			314A	5–Pin Horizontal Leadform
LM2931CTV			314B	5–Pin Vertical Leadform

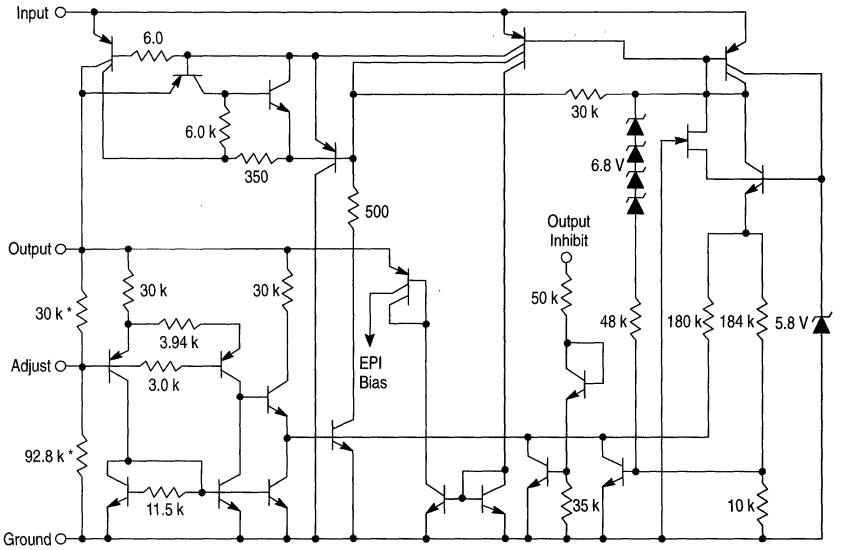
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Continuous	V_I	40	Vdc
Transient Input Voltage ($\tau \leq 100$ ms)	$V_I(\tau)$	60	Vpk
Transient Reverse Polarity Input Voltage 1.0% Duty Cycle, $\tau \leq 100$ ms	$-V_I(\tau)$	–50	Vpk
Power Dissipation			
Case 29 (TO–92 Type)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	178	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	83	°C/W
Case 221A, 314A, 314B and 314D (TO–220 Type)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Case 369 and 369A (DPAK) [Note 1]			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	92	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	6.0	°C/W
Case 751 (SOP–8) [Note 2]			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	160	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	25	°C/W
Case 936 and 936A (D^2PAK) [Note 3]			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	70	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Tested Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. DPAK Junction–to–Ambient Thermal Resistance is for vertical mounting. Refer to Figure 23 for board mounted Thermal Resistance.
2. SOP–8 Junction–to–Ambient Thermal Resistance is for minimum recommended pad size. Refer to Figure 23 for Thermal Resistance variation versus pad size.
3. D^2PAK Junction–to–Ambient Thermal Resistance is for vertical mounting. Refer to Figure 25 for board mounted Thermal Resistance.

3

Representative Schematic Diagram



*Deleted on Adjustable Regulators

This device contains 26 active transistors.

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 10 mA, C_O = 100 µF, $C_{O(ESR)}$ = 0.3 Ω, T_J = 25°C [Note 4].)

Characteristic	Symbol	LM2931–5.0 Min	LM2931–5.0 Typ	LM2931–5.0 Max	LM2931A–5.0 Min	LM2931A–5.0 Typ	LM2931A–5.0 Max	Unit
FIXED OUTPUT								
Output Voltage V_{in} = 14 V, I_O = 10 mA, T_J = 25°C V_{in} = 6.0 V to 26 V, $I_O \leq$ 100 mA, T_J = −40° to +125°C	V_O	 4.75 4.50	 5.0 –	 5.25 5.50	 4.81 4.75	 5.0 –	 5.19 5.25	V
Line Regulation V_{in} = 9.0 V to 16 V V_{in} = 6.0 V to 26 V	Reg_{line}	 – –	 2.0 4.0	 10 30	 – –	 2.0 4.0	 10 30	mV
Load Regulation (I_O = 5.0 mA to 100 mA)	Reg_{load}	–	14	50	–	14	50	mV
Output Impedance I_O = 10 mA, ΔI_O = 1.0 mA, f = 100 Hz to 10 kHz	Z_O	 –	 200	 –	 –	 200	 –	mΩ
Bias Current V_{in} = 14 V, I_O = 100 mA, T_J = 25°C V_{in} = 6.0 V to 26 V, I_O = 10 mA, T_J = −40° to +125°C	I_B	 – –	 5.8 0.4	 30 1.0	 – –	 5.8 0.4	 30 1.0	mA
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	–	700	–	–	700	–	µVrms
Long Term Stability	S	–	20	–	–	20	–	mV/kHR
Ripple Rejection (f = 120 Hz)	RR	60	90	–	60	90	–	dB
Dropout Voltage I_O = 10 mA I_O = 100 mA	V_I–V_O	 – –	 0.015 0.16	 0.2 0.6	 – –	 0.015 0.16	 0.2 0.6	V
Over–Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = −15 V)	$-V_O$	−0.3	0	–	−0.3	0	–	V

NOTE: 4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, V_O = 3.0 V, I_O = 10 mA, R_1 = 27 k, C_O = 100 µF, $C_{O(ESR)}$ = 0.3 Ω, T_J = 25°C [Note 4].)

Characteristic	Symbol	LM2931C			Unit
		Min	Typ	Max	
ADJUSTABLE OUTPUT					
Reference Voltage (Note 5, Figure 18) I_O = 10 mA, T_J = 25°C $I_O \leq$ 100 mA, T_J = −40 to +125°C	V_{ref}	 1.14 1.08	 1.20 –	 1.26 1.32	V
Output Voltage Range	$V_{O\ range}$	3.0 to 24	2.7 to 29.5	–	V
Line Regulation (V_{in} = V_O + 0.6 V to 26 V)	Reg_{line}	–	0.2	1.5	mV/V
Load Regulation (I_O = 5.0 mA to 100 mA)	Reg_{load}	–	0.3	1.0	%/V
Output Impedance I_O = 10 mA, ΔI_O = 1.0 mA, f = 10 Hz to 10 kHz	Z_O	 –	 40	 –	mΩ/V
Bias Current I_O = 100 mA I_O = 10 mA Output Inhibited ($V_{th(OI)}$ = 2.5 V)	I_B	 – – –	 6.0 0.4 0.2	 – 1.0 1.0	mA
Adjustment Pin Current	I_{Adj}	–	0.2	–	µA
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	–	140	–	µVrms/V
Long–Term Stability	S	–	0.4	–	%/kHR
Ripple Rejection (f = 120 Hz)	RR	0.10	0.003	–	%/V
Dropout Voltage I_O = 10 mA I_O = 100 mA	V_I–V_O	 – –	 0.015 0.16	 0.2 0.6	V
Over–Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = −15 V)	$-V_O$	−0.3	0	–	V
Output Inhibit Threshold Voltages Output "On": T_J = 25°C T_J = −40° to +125°C Output "Off": T_J = 25°C T_J = −40° to +125°C	$V_{th(OI)}$	 – – 2.50 3.25	 2.15 – 2.26 –	 1.90 1.20 – –	V
Output Inhibit Threshold Current ($V_{th(OI)}$ = 2.5 V)	$I_{th(OI)}$	–	30	50	µA

NOTES: 4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
5. The reference voltage on the adjustable device is measured from the output to the adjust pin across R_1.

Figure 1. Dropout Voltage versus Output Current

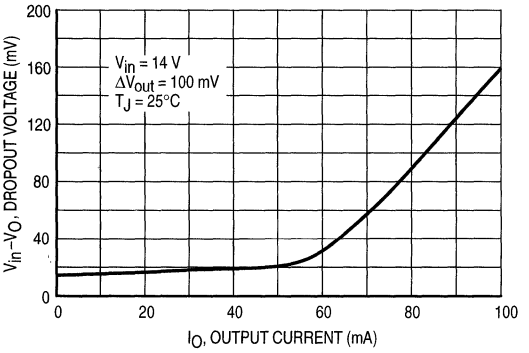


Figure 2. Dropout Voltage versus Junction Temperature

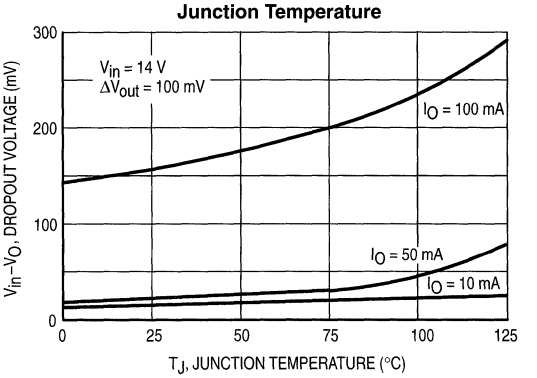


Figure 3. Peak Output Current versus Input Voltage

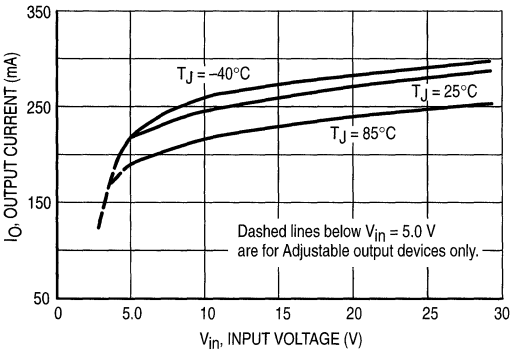


Figure 4. Output Voltage versus Input Voltage

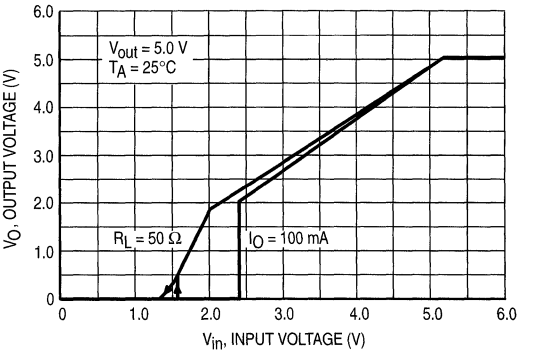


Figure 5. Output Voltage versus Input Voltage

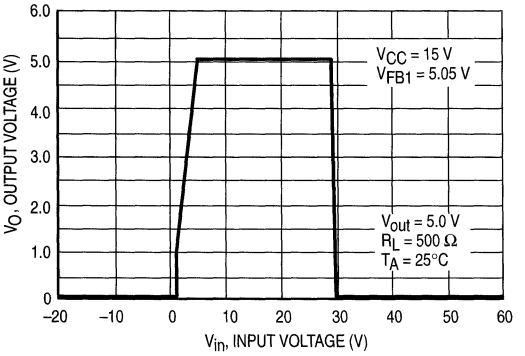


Figure 6. Load Dump Characteristics

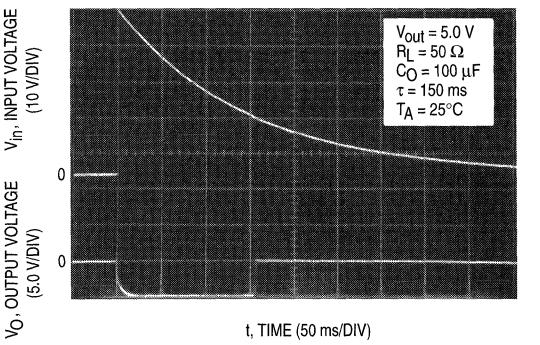


Figure 7. Bias Current versus Input Voltage

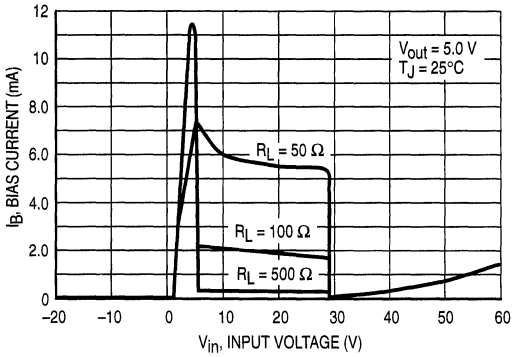


Figure 8. Bias Current versus Output Current

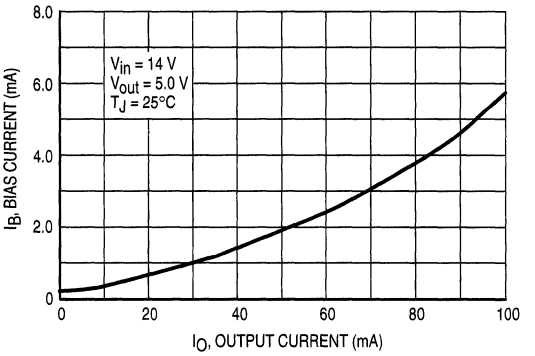


Figure 9. Bias Current versus Junction Temperature

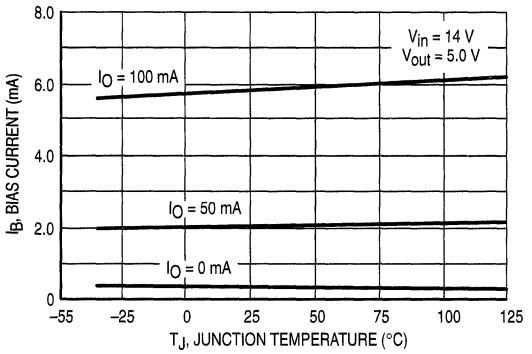


Figure 10. Output Impedance versus Frequency

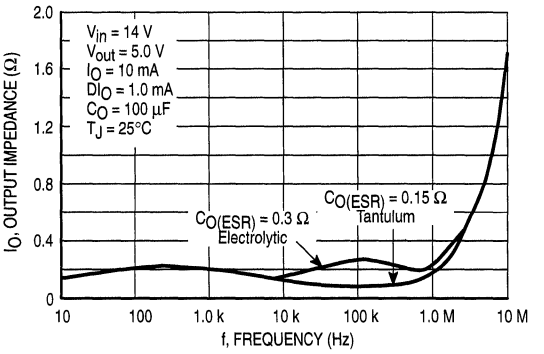


Figure 11. Ripple Rejection versus Frequency

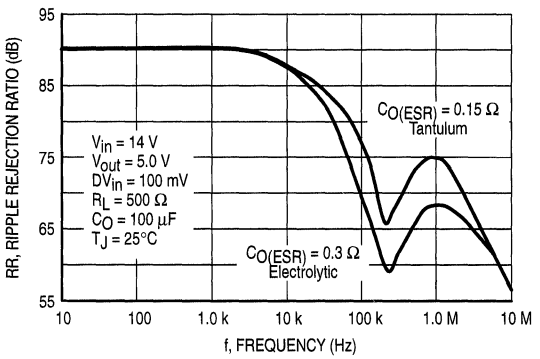


Figure 12. Ripple Rejection versus Output Current

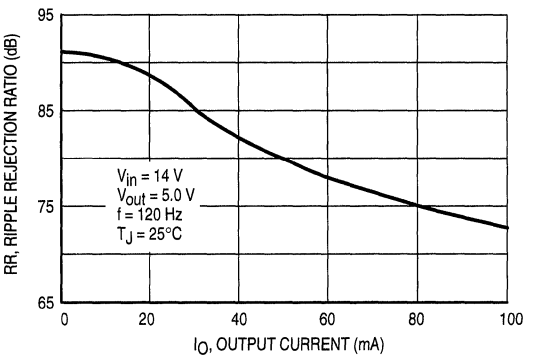


Figure 13. Line Regulation

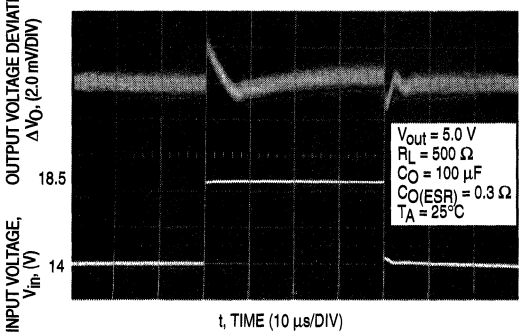


Figure 14. Load Regulation

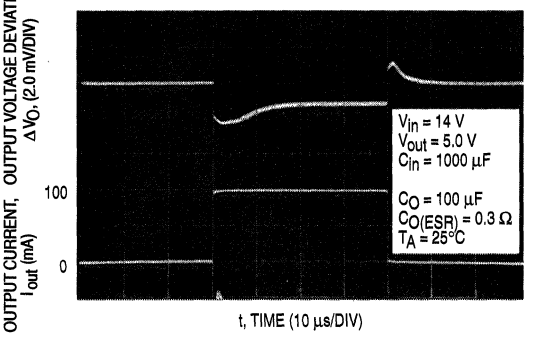


Figure 15. Reference Voltage versus Output Voltage

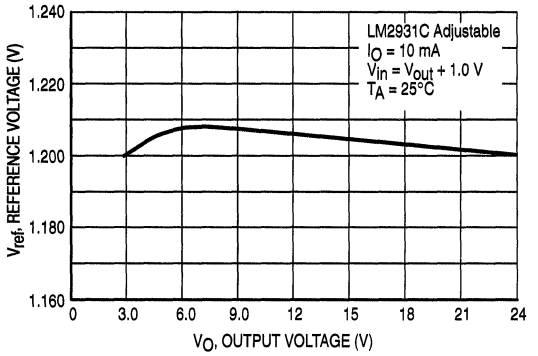
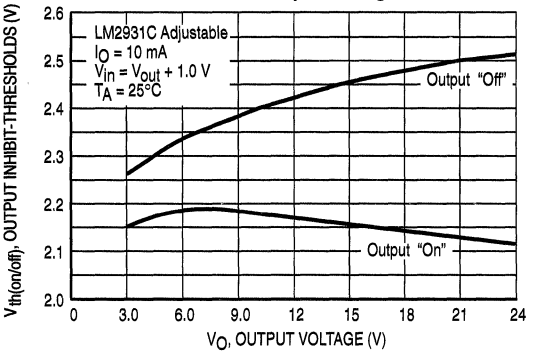


Figure 16. Output Inhibit–Thresholds versus Output Voltage



APPLICATIONS INFORMATION

The LM2931 series regulators are designed with many protection features making them essentially blow–out proof. These features include internal current limiting, thermal shutdown, overvoltage and reverse polarity input protection, and the capability to withstand temporary power–up with mirror–image insertion. Typical application circuits for the fixed and adjustable output device are shown in Figures 17 and 18.

The input bypass capacitor C_{in} is recommended if the regulator is located an appreciable distance (≥ 4″) from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

This regulator series is not internally compensated and thus requires an external output capacitor for stability. The capacitance value required is dependent upon the load current, output voltage for the adjustable regulator, and the type of capacitor selected. The least stable condition is encountered at maximum load current and minimum output voltage. Figure 22 shows that for operation in the "Stable" region, under the conditions specified, the magnitude of the output capacitor impedance $|Z_O|$ must not exceed 0.4 Ω. This limit must be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around −30°C, the capacitance will decrease and the equivalent series resistance (ESR) will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of −40° to +85°C and −55° to +105°C are readily available. Solid tantalum capacitors may be a better choice if small size is a requirement, however, the maximum $|Z_O|$ limit over temperature must be observed.

Note that in the stable region, the output noise voltage is linearly proportional to $|Z_O|$. In effect, C_O dictates the high frequency roll–off point of the circuit. Operation in the area titled "Marginally Stable" will cause the output of the regulator to exhibit random bursts of oscillation that decay in an under–damped fashion. Continuous oscillation occurs when operating in the area titled "Unstable". It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.

Figure 17. Fixed Output Regulator

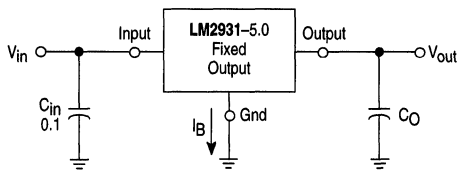
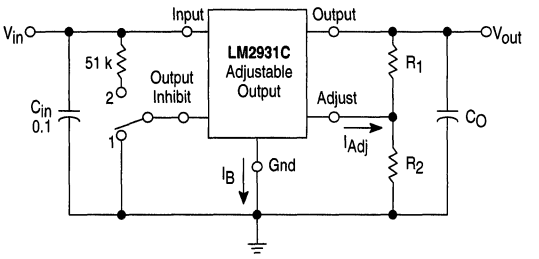


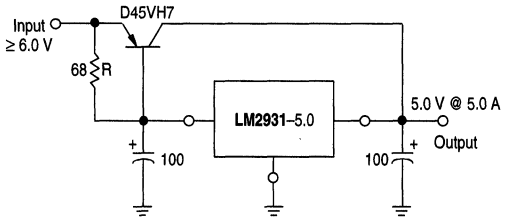
Figure 18. Adjustable Output Regulator



Switch Position 1 = Output "On", 2 = Output "Off"

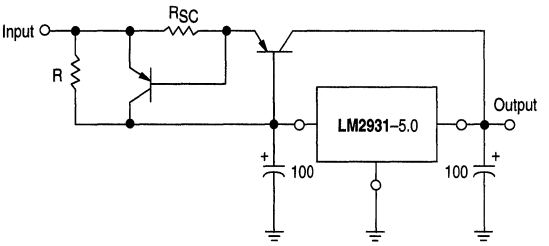
$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2 \qquad 22.5\ k \geq \frac{R_1\,R_2}{R_1 + R_2}$$

Figure 19. (5.0 A) Low Differential Voltage Regulator



The LM2931 series can be current boosted with a PNP transistor. The D45VH7, on a heatsink, will provide an output current of 5.0 A with an input to output voltage differential of approximately 1.0 V. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting. This circuit is not short circuit proof.

Figure 20. Current Boost Regulator with Short Circuit Projection



The circuit of Figure 19 can be modified to provide supply protection against short circuits by adding the current sense resistor R_{SC} and an additional PNP transistor. The current sensing PNP must be capable of handling the short circuit current of the LM2931. Safe operating area of both transistors must be considered under worst case conditions.

Figure 21. Constant Intensity Lamp Flasher

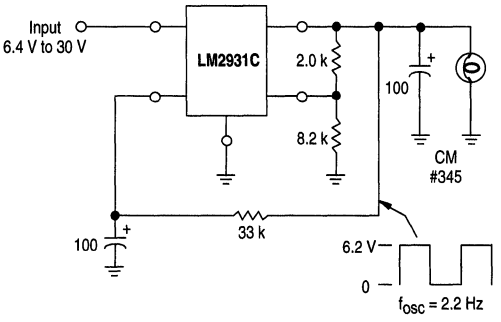


Figure 22. Output Noise Voltage versus Output Capacitor Impedance

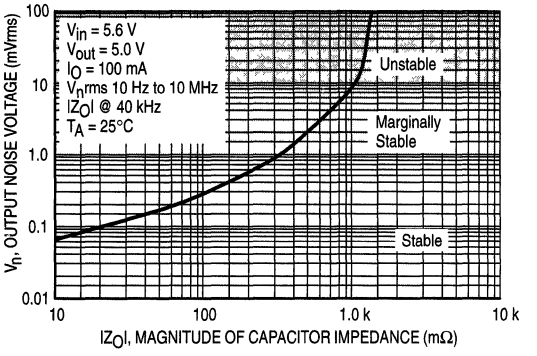


Figure 23. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

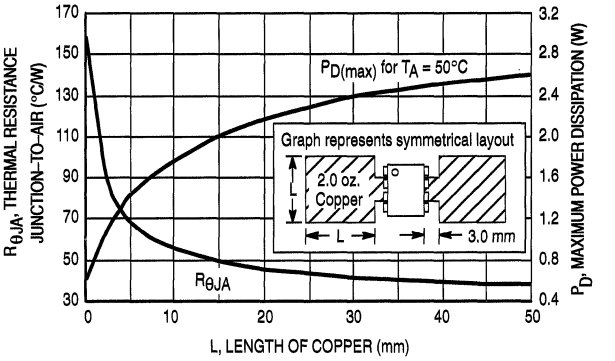


Figure 24. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

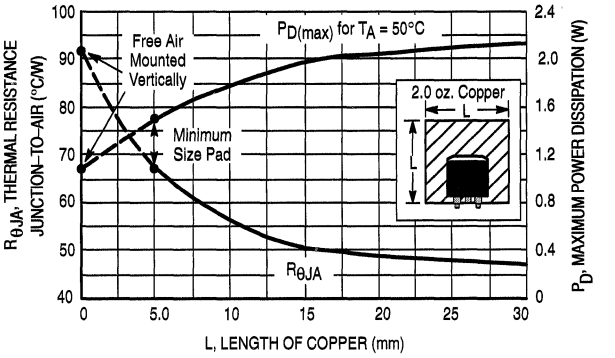
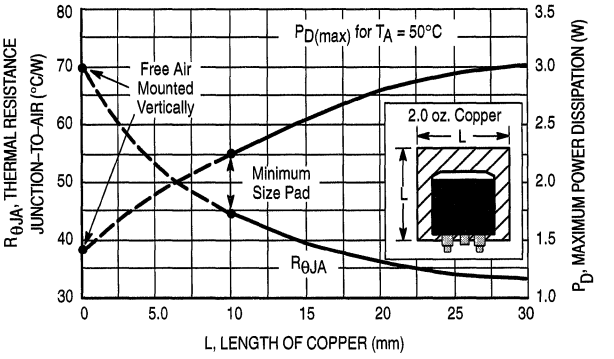


Figure 25. 3–Pin and 5–Pin D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



DEFINITIONS

Dropout Voltage – The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output decreases 100 mV from nominal value at 14 V input, dropout voltage is affected by junction temperature and load current.

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long–Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices electrical characteristics and maximum power dissipation.

LM2935

3

Low Dropout Dual Voltage Regulator

LOW DROPOUT DUAL VOLTAGE REGULATOR

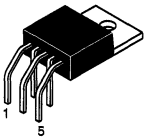
SEMICONDUCTOR TECHNICAL DATA

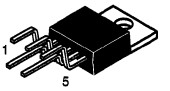
The LM2935 is a dual positive 5.0 V low dropout voltage regulator, designed for standby power systems. The main output is capable of supplying 750 mA for microprocessor power, and can be turned "on" and "off" by the switch/reset input. The other output is dedicated for standby operation of volatile memory, and is capable of supplying up to 10 mA loads. The total device features a low quiescent current of 3.0 mA or less when supplying 10 mA from the standby output.

This part was designed for harsh automotive environments and is therefore immune to many input supply voltage problems such as reverse battery (–12 V), double battery (+24 V), and load dump transients (+60 V).

- Two Regulated 5.0 V Outputs
- Main Output Current in Excess of 750 mA
- On/Off Control of Main Output
- Standby Output Current in Excess of 10 mA
- Low Input/Output Differential of Less than 0.6 V at 500 mA
- Short Circuit Current Limiting
- Internal Thermal Shutdown
- Low Voltage Indicator Output
- Designed for Automotive Environment Including
  - Reverse Battery Protection
  - Double Battery Protection
  - Load Dump Protection
  - Reverse Transient Protection
- Economical 5–Lead TO–220 Package with Two Optional Leadforms
- Also Available in Surface Mount D^2PAK Package

TH SUFFIX
PLASTIC PACKAGE
CASE 314A

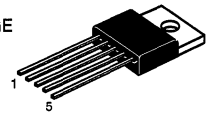




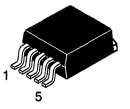
TV SUFFIX
PLASTIC PACKAGE
CASE 314B

Heatsink surface connected to Pin 3.

T SUFFIX
PLASTIC PACKAGE
CASE 314D



Pin 1. Input Voltage/V_{CC}
2. Main Output
3. Ground
4. Switch/Reset
5. Standby/Output



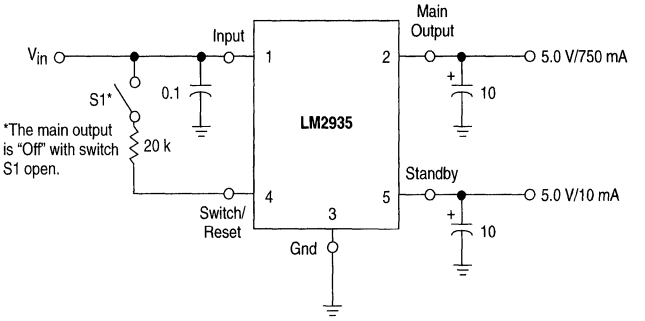
D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^2PAK)

Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM2935D2T	T_J = –40° to +125°C	Surface Mount
LM2935T		Plastic Power
LM2935TH		Horizontal Mount
LM2935TV		Vertical Mount

Typical Application Circuit



An input bypass capacitor is recommended if the regulator is located more than 4″ from the supply input filter. The LM2935 is not internally compensated and thus requires an external output capacitor for stability. A minimum capacitance of 10 μF is recommended. The actual capacitance value is dependent upon load current, temperature, and the capacitor's equivalent series resistance (ESR). The least stable condition is encountered at maximum load current and minimum ambient temperature.

This device contains 29 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Continuous	V_I	60	Vdc
Transient Reverse Polarity Input Voltage 1.0% Duty Cycle, $\tau \leq 100$ ms	$-V_I(\tau)$	−50	Vpk
Switch/Reset Input Current	I_{in}	5.0	mA
Power Dissipation Case 314A, 314B and 314D (TO–220 Type) T_A = 25°C Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case Case 936A (D^2PAK) T_A = 25°C Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case	 P_D $R_{\theta JA}$ $R_{\theta JC}$ P_D $R_{\theta JA}$ $R_{\theta JC}$	 Internally Limited 65 5.0 Internally Limited Per Figure 1 5.0	 W °C/W °C/W W °C/W °C/W
Operating Junction Temperature Range	T_J	−40 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, I_{stby} = 0 mA, C_O = 10 μF, C_{stby} = 10 μF, T_J = 25°C [Note 1].)

Characteristic	Symbol	Min	Typ	Max	Unit
MAIN OUTPUT					
Output Voltage (V_{in} = 6.0 V to 26 V, I_O = 5.0 mA to 500 mA, T_J = −40 to +125°C)	V_O	4.75	5.0	5.25	V
Line Regulation V_{in} = 9.0 V to 16 V, I_O = 5.0 mA V_{in} = 6.0 V to 26 V, I_O = 5.0 mA	Reg_{line}	 – –	 4.0 10	 25 50	mV
Load Regulation (I_O = 5.0 mA to 500 mA)	Reg_{load}	–	10	50	mV
Output Impedance I_O = 500 mAdc and 10 mArms, f = 100 Hz to 10 kHz	Z_O	 –	 200	 –	mΩ
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	–	100	–	μVrms
Long Term Stability	S	–	20	–	mV/kHR

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, I_{stby} = 0 mA, C_O = 10 µF, C_{stby} = 10 µF, T_J = 25°C [Note 1].)

Characteristic	Symbol	Min	Typ	Max	Unit
MAIN OUTPUT (continued)					
Ripple Rejection (f = 120 Hz)	RR	–	66	–	dB
Dropout Voltage I_O = 500 mA I_O = 750 mA	V_I–V_O	 – –	 0.45 0.82	 0.6 –	V
Short Circuit Current Limit	I_{SC}	0.75	1.2	–	A
Over–Voltage Shutdown Threshold	$V_{th(OV)}$	26	31	–	V
SWITCH/RESET					
Output Sink Current (V_{OL} = 1.2 V)	I_{Sink}	–	5.0	–	mA
Output Voltage ($R_{on/off}$ = 20 kΩ) Low State, V_{in} = 4.0 V High State, V_{in} = 14 V	 V_{OL} V_{OH}	 – 4.5	 0.9 5.0	 1.2 6.0	V
Output Pull–Up Resistor, "On"/"Off" (Note 2)	$R_{on/off}$	–	20	30	kΩ
Output Voltage with Reverse Polarity Input (V_{in} = –15 V, R_L = 10 Ω)	$-V_O$	–0.6	0	–	V

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 0 mA, I_{stby} = 10 mA, C_O = 10 µF, C_{stby} = 10 µF, T_J = 25°C [Note 1].)

Characteristic	Symbol	Min	Typ	Max	Unit
STANDBY OUTPUT					
Output Voltage (V_{in} = 6.0 V to 26 V, I_{stby} = 1.0 mA to 10 mA, T_J = –40 to +125°C)	$V_{O(stby)}$	4.75	5.0	5.25	V
Tracking Voltage	V_O–$V_{O(stby)}$	–200	0	200	mV
Line Regulation (V_{in} = 6.0 V to 26 V)	Reg_{line}	–	4.0	50	mV
Load Regulation (I_{stby} = 1.0 mA to 10 mA)	Reg_{load}	–	10	50	mV
Output Impedance $I_{(stby)}$ = 10 mAdc and 1.0 mArms, f = 100 Hz to 10 kHz	$Z_{O(stby)}$	–	1.0	–	Ω
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	–	300	–	µVrms
Long Term Stability	S	–	20	–	mV/kHR
Ripple Rejection (f = 120 Hz)	RR	–	66	–	dB
Dropout Voltage (I_{stby} = 10 mA)	V_I–$V_{O(stby)}$	–	0.55	0.7	V
Short Circuit Current Limit	I_{SC}	25	70	–	mA
Output Voltage with Reverse Polarity Input V_{in} = –15 V, R_L = 510 Ω	$-V_O$	–0.3	0	–	V
Output Voltage with Maximum Positive Input V_{in} = 60 V, R_L = 510 Ω	$V_{O(max)}$	–	5.0	6.0	V
TOTAL DEVICE					
Bias Current I_O = 10 mA, I_{stby} = 0 mA I_O = 500 mA, I_{stby} = 0 mA I_O = 750 mA, I_{stby} = 0 mA Main Output "Off", I_{stby} = 10 mA	I_B	 – – – –	 3.0 40 90 2.0	 – 100 – 3.0	mA

NOTES: 1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. The maximum switch/reset current must not exceed 5.0 mA.

TYPICAL CIRCUIT WAVEFORMS

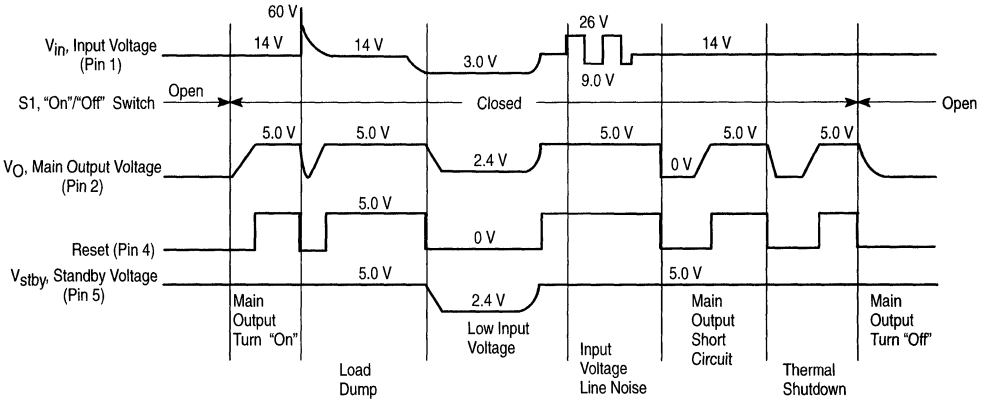
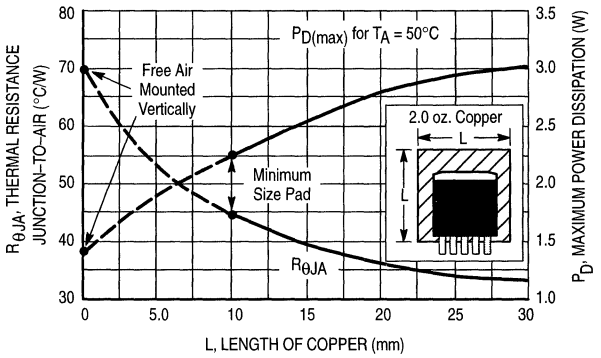


Figure 1. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



LP2950
LP2951

3

Micropower Voltage Regulators

MICROPOWER LOW DROPOUT VOLTAGE REGULATORS

The LP2950 and LP2951 are micropower voltage regulators that are specifically designed to maintain proper regulation with an extremely low input–to–output voltage differential. These devices feature a very low quiescent bias current of 75 μA and are capable of supplying output currents in excess of 100 mA. Internal current and thermal limiting protection is provided.

The LP2951 has three additional features. The first is the $\overline{\text{Error}}$ Output that can be used to signal external circuitry of an out of regulation condition, or as a microprocessor power–on reset. The second feature allows the output voltage to be preset to 5.0 V, 3.3 V or 3.0 V output (depending on the version) or programmed from 1.25 V to 29 V. It consists of a pinned out resistor divider along with direct access to the Error Amplifier feedback input. The third feature is a Shutdown input that allows a logic level signal to turn–off or turn–on the regulator output.

Due to the low input–to–output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable. The LP2950 is available in the three pin case 29 and DPAK packages, and the LP2951 is available in the eight pin dual–in–line, SO–8 and Micro–8 surface mount packages. The 'A' suffix devices feature an initial output voltage tolerance ±0.5%.

LP2950 and LP2951 Features:

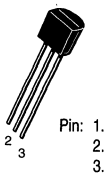
- Low Quiescent Bias Current of 75 μA
- Low Input–to–Output Voltage Differential of 50 mV at 100 μA and 380 mV at 100 mA
- 5.0 V, 3.3 V or 3.0 V ±0.5% Allows Use as a Regulator or Reference
- Extremely Tight Line and Load Regulation
- Requires Only a 1.0 μF Output Capacitor for Stability
- Internal Current and Thermal Limiting

LP2951 Additional Features:

- $\overline{\text{Error}}$ Output Signals an Out of Regulation Condition
- Output Programmable from 1.25 V to 29 V
- Logic Level Shutdown Input

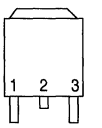
(See Following Page for Ordering Information.)

Z SUFFIX
PLASTIC PACKAGE
CASE 29
(TO–226AA/TO–92)



Pin: 1. Output
2. Ground
3. Input

DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)



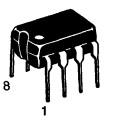
(Top View)

Pin: 1. Input
2. Ground
3. Output

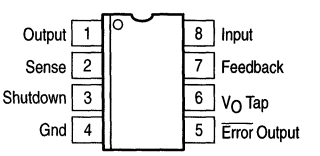
Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

N SUFFIX
PLASTIC PACKAGE
CASE 626



DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)



(Top View)

ORDERING INFORMATION

Device	Type	Operating Temperature Range	Package
LP2950CZ–** LP2950ACZ–**	Fixed Voltage (3.0, 3.3 or 5.0 V)	T_J = –40° to +125°C	TO–92/TO–226AA
LP2950CDT–** LP2950ACDT–**			DPAK
LP2951CD LP2951ACD	Adjustable or 5.0 V Fixed		SO–8
LP2951CD–** LP2951ACD–**	Adjustable or Fixed (3.0, 3.3 V)		
LP2951CN LP2951ACN	Adjustable or 5.0 V Fixed		Plastic
LP2951CN–** LP2951ACN–**	Adjustable or Fixed (3.0, 3.3 V)		
LP2951CDM LP2951ACDM	Adjustable or 5.0 V Fixed		Micro–8
LP2951CDM–** LP2951ACDM–**	Adjustable or Fixed (3.0, 3.3 V)		

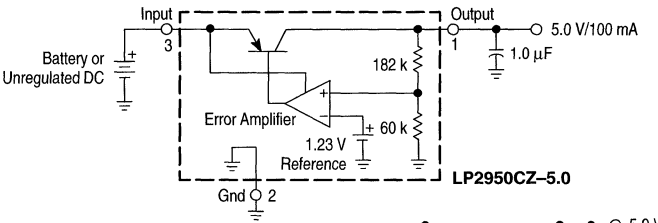
** = Voltage option of 3.0, 3.3 or 5.0 V.

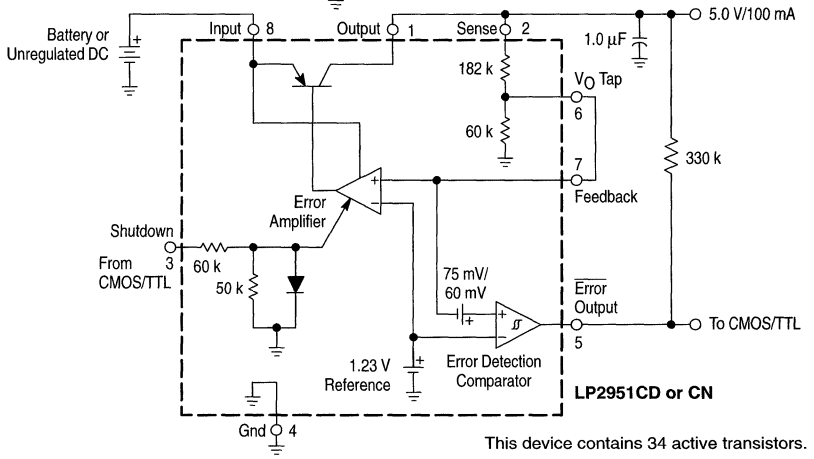
DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

Device No. (±1%)	Device No. (±0.5%)	Nominal Voltage
LP2950CX–5.0	LP2950ACX–5.0	5.0
LP2950CX–3.3	LP2950ACX–3.3	3.3
LP2950CX–3.0	LP2950ACX–3.0	3.0
LP2951CX	LP2951ACX	Adjustable or 5.0
LP2950CX–3.3	LP2951ACX–3.3	Adjustable or 3.3
LP2951CX–3.0	LP2951ACX–3.0	Adjustable or 3.0

X = Package suffix.

Representative Block Diagrams





This device contains 34 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_{CC}	30	Vdc
Power Dissipation and Thermal Characteristics Maximum Power Dissipation	P_D	Internally Limited	W
Case 751(SO–8) D Suffix			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	180	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	45	°C/W
Case 369A (DPAK) DT Suffix [Note 1]			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	92	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	6.0	°C/W
Case 29 (TO–226AA/TO–92) Z Suffix			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	160	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	83	°C/W
Case 626 N Suffix			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	105	°C/W
Case 846A (Micro–8) DM Suffix			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	240	°C/W
Feedback Input Voltage	V_{fb}	–1.5 to +30	Vdc
Shutdown Input Voltage	V_{sd}	–0.3 to +30	Vdc
Error Comparator Output Voltage	V_{err}	–0.3 to +30	Vdc
Operating Junction Temperature	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: 1. The Junction–to–Ambient Thermal Resistance is determined by PC board copper area per Figure 26.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS ($V_{in} = V_O + 1.0$ V, I_O = 100 µA, C_O = 1.0 µF, T_J = 25°C [Note 1], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage, 5.0 V Versions	V_O				V
V_{in} = 6.0 V, I_O = 100 µA, T_J = 25°C					
LP2950C–5.0/LP2951C		4.950	5.000	5.050	
LP2950AC–5.0/LP2951AC		4.975	5.000	5.025	
T_J = –40 to +125°C					
LP2950C–5.0/LP2951C		4.900	–	5.100	
LP2950AC–5.0/LP2951AC		4.940	–	5.060	
V_{in} = 6.0 to 30 V, I_O = 100 µA to 100 mA, T_J = –40 to +125°C					
LP2950C–5.0/LP2951C		4.880	–	5.120	
LP2950AC–5.0/LP2951AC		4.925	–	5.075	
Output Voltage, 3.3 V Versions	V_O				V
V_{in} = 4.3 V, I_O = 100 µA, T_J = 25°C					
LP2950C–3.3/LP2951C–3.3		3.267	3.300	3.333	
LP2950AC–3.3/LP2951AC–3.3		3.284	3.300	3.317	
T_J = –40 to +125°C					
LP2950C–3.3/LP2951C–3.3		3.234	–	3.366	
LP2950AC–3.3/LP2951AC–3.3		3.260	–	3.340	
V_{in} = 4.3 to 30 V, I_O = 100 µA to 100 mA, T_J = –40 to +125°C					
LP2950C–3.3/LP2951C–3.3		3.221	–	3.379	
LP2950AC–3.3/LP2951AC–3.3		3.254	–	3.346	
Output Voltage, 3.0 V Versions	V_O				V
V_{in} = 4.0 V, I_O = 100 µA, T_J = 25°C					
LP2950C–3.0/LP2951C–3.0		2.970	3.000	3.030	
LP2950AC–3.0/LP2951AC–3.0		2.985	3.000	3.015	
T_J = –40 to +125°C					
LP2950C–3.0/LP2951C–3.0		2.940	–	3.060	
LP2950AC–3.0/LP2951AC–3.0		2.964	–	3.036	
V_{in} = 4.0 to 30 V, I_O = 100 µA to 100 mA, T_J = –40 to +125°C					
LP2950C–3.0/LP2951C–3.0		2.928	–	3.072	
LP2950AC–3.0/LP2951AC–3.0		2.958	–	3.042	

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = V_O + 1.0 V, I_O = 100 µA, C_O = 1.0 µF, T_J = 25°C [Note 1], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Line Regulation (V_{in} = $V_{O(nom)}$ +1.0 V to 30 V) [Note 2]	Reg_{line}				%
LP2950C–XX/LP2951C/LP2951C–XX		–	0.08	0.20	
LP2950AC–XX/LP2951AC/LP2951AC–XX		–	0.04	0.10	
Load Regulation (I_O = 100 µA to 100 mA)	Reg_{load}				%
LP2950C–XX/LP2951C/LP2951C–XX		–	0.13	0.20	
LP2950AC–XX/LP2951AC/LP2951AC–XX		–	0.05	0.10	
Dropout Voltage	$V_I - V_O$				mV
I_O = 100 µA		–	30	80	
I_O = 100 mA		–	350	450	
Supply Bias Current	I_{CC}				
I_O = 100 µA		–	93	120	µA
I_O = 100 mA		–	4.0	12	mA
Dropout Supply Bias Current (V_{in} = $V_{O(nom)}$ – 0.5 V, I_O = 100 µA) [Note 2]	$I_{CCdropout}$	–	110	170	µA
Current Limit (V_O Shorted to Ground)	I_{Limit}	–	220	300	mA
Thermal Regulation	$Reg_{thermal}$	–	0.05	0.20	%/W
Output Noise Voltage (10 Hz to 100 kHz) [Note 3]	V_n				µVrms
C_L = 1.0 µF		–	126	–	
C_L = 100 µF		–	56	–	
LP2951A/LP2951AC ONLY					
Reference Voltage (T_J = 25°C)	V_{ref}				V
LP2951C/LP2951C–XX		1.210	1.235	1.260	
LP2951AC/LP2951AC–XX		1.220	1.235	1.250	
Reference Voltage (T_J = –40 to +125°C)	V_{ref}				V
LP2951C/LP2951C–XX		1.200	–	1.270	
LP2951AC/LP2951AC–XX		1.200	–	1.260	
Reference Voltage (T_J = –40 to +125°C)	V_{ref}				V
I_O = 100 µA to 100 mA, V_{in} = 23 to 30 V					
LP2951C/LP2951C–XX		1.185	–	1.285	
LP2951AC/LP2951AC–XX		1.190	–	1.270	
Feedback Pin Bias Current	I_{FB}	–	15	40	nA
ERROR COMPARATOR					
Output Leakage Current (V_{OH} = 30 V)	I_{lkg}	–	0.01	1.0	µA
Output Low Voltage (V_{in} = 4.5 V, I_{OL} = 400 µA)	V_{OL}	–	150	250	mV
Upper Threshold Voltage (V_{in} = 6.0 V)	V_{thu}	40	45	–	mV
Lower Threshold Voltage (V_{in} = 6.0 V)	V_{thl}	–	60	95	mV
Hysteresis (V_{in} = 6.0 V)	V_{hy}	–	15	–	mV
SHUTDOWN INPUT					
Input Logic Voltage	V_{shtdn}				V
Logic "0" (Regulator "On")		0	–	0.7	
Logic "1" (Regulator "Off")		2.0	–	30	
Shutdown Pin Input Current	I_{shtdn}				µA
V_{shtdn} = 2.4 V		–	35	50	
V_{shtdn} = 30 V		–	450	600	
Regulator Output Current in Shutdown Mode (V_{in} = 30 V, V_{shtdn} = 2.0 V, V_O = 0, Pin 6 Connected to Pin 7)	I_{off}	–	3.0	10	µA

NOTES: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. $V_{O(nom)}$ is the part number voltage option.
3. Noise tests on the LP2951 are made with a 0.01 µF capacitor connected across Pins 7 and 1.

DEFINITIONS

Dropout Voltage – The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation – The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current – Current which is used to operate the regulator chip and is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Leakage Current – Current drawn through a bipolar transistor collector–base junction, under a specified collector voltage, when the transistor is "off".

Upper Threshold Voltage – Voltage applied to the comparator input terminal, below the reference voltage which is applied to the other comparator input terminal, which causes the comparator output to change state from a logic "0" to "1".

Lower Threshold Voltage – Voltage applied to the comparator input terminal, below the reference voltage which is applied to the other comparator input terminal, which causes the comparator output to change state from a logic "1" to "0".

Hysteresis – The difference between Lower Threshold voltage and Upper Threshold voltage.

Figure 1. Quiescent Current

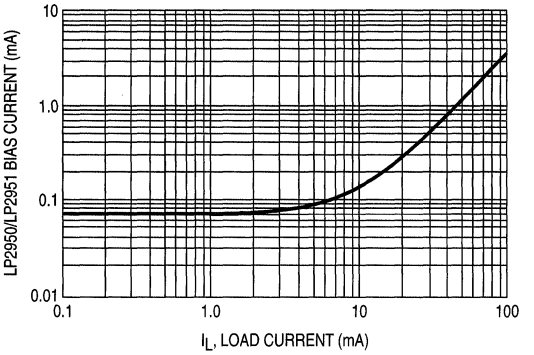


Figure 2. Dropout Characteristics

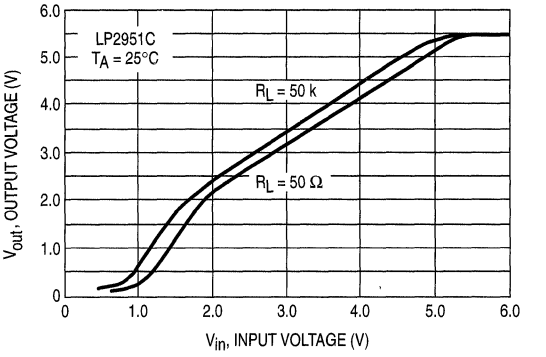


Figure 3. Input Current

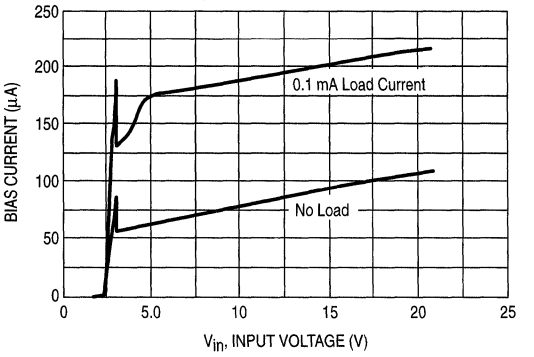


Figure 4. Output Voltage versus Temperature

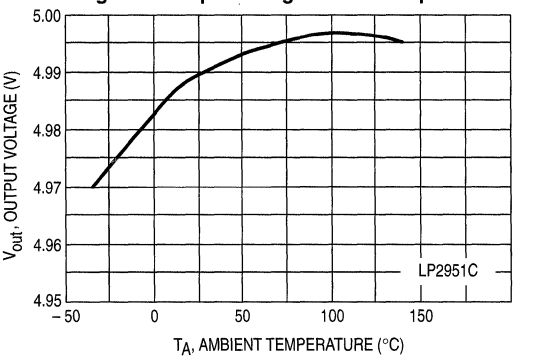


Figure 5. Dropout Voltage versus Output Current

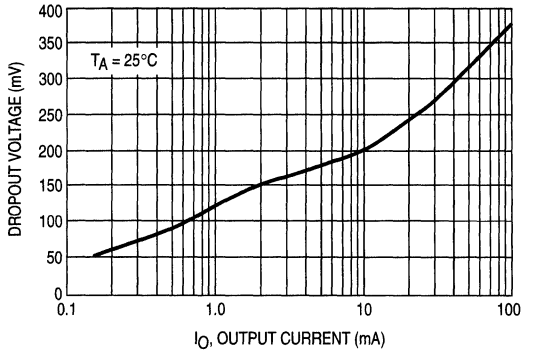


Figure 6. Dropout Voltage versus Temperature

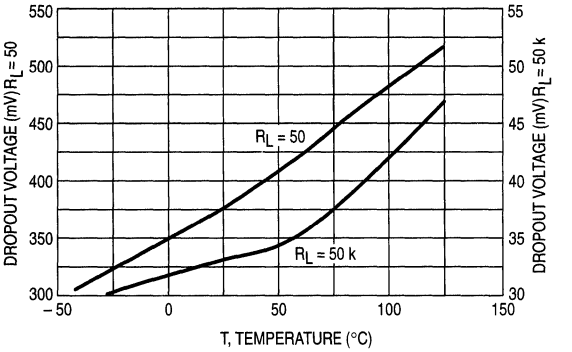


Figure 7. Error Comparator Output

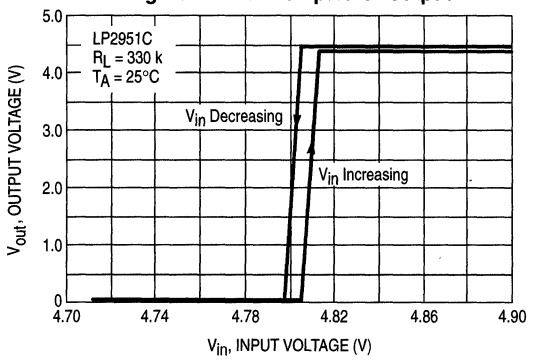


Figure 8. Line Transient Response

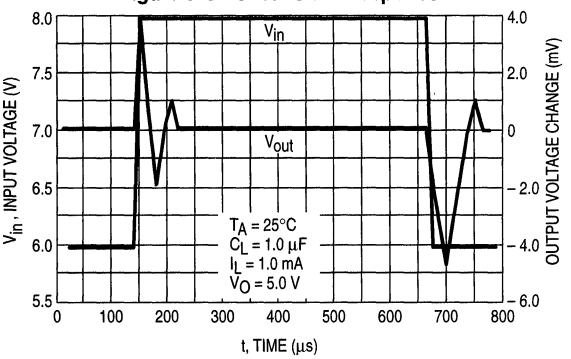


Figure 9. LP2951 Enable Transient

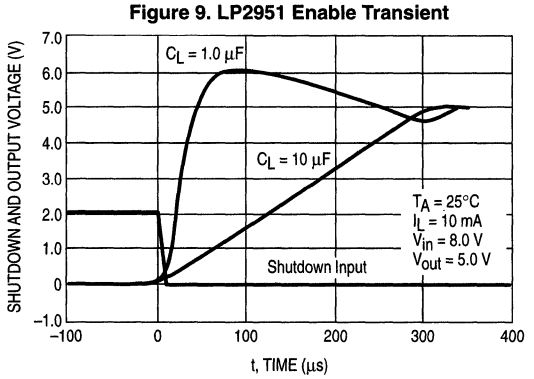


Figure 10. Load Transient Response

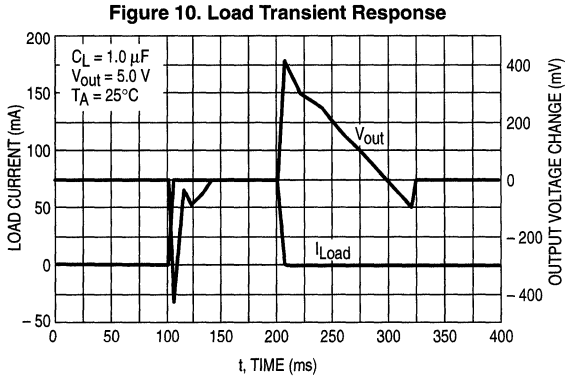


Figure 11. Ripple Rejection

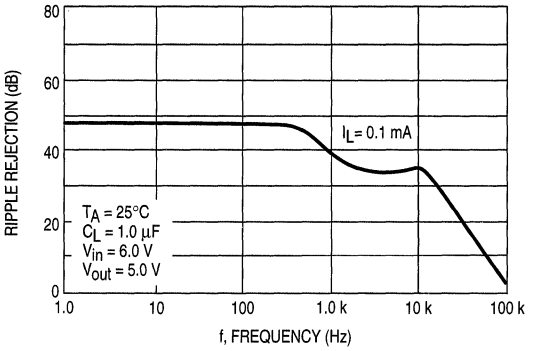


Figure 12. Output Noise

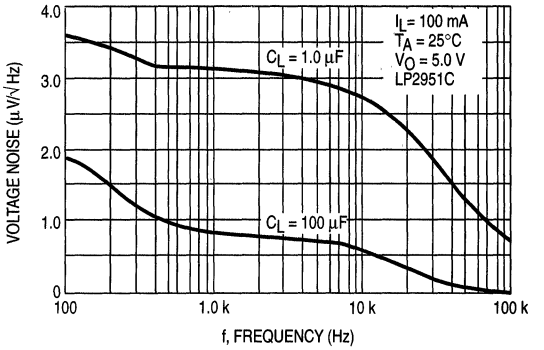


Figure 13. Shutdown Threshold Voltage versus Temperature

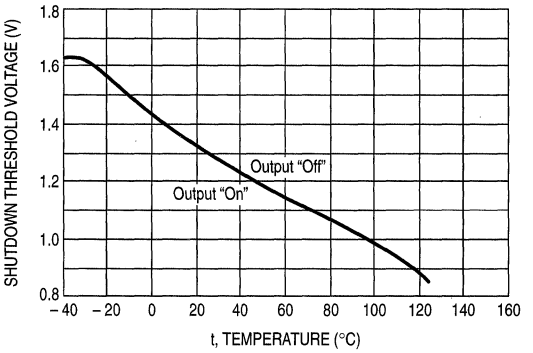
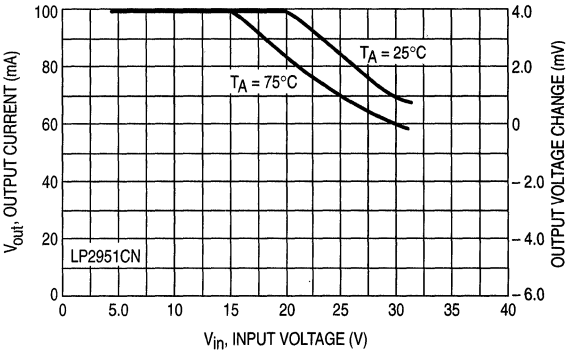


Figure 14. Maximum Rated Output Current



APPLICATIONS INFORMATION

Introduction

The LP2950/LP2951 regulators are designed with internal current limiting and thermal shutdown making them user–friendly. Typical application circuits for the LP2950 and LP2951 are shown in Figures 17 through 25.

These regulators are not internally compensated and thus require a 1.0 μF (or greater) capacitance between the LP2950/LP2951 output terminal and ground for stability. Most types of aluminum, tantalum or multilayer ceramic will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are recommended for operation below 25°C.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.33 μF for currents less than 10 mA, or 0.1 μF for currents below 1.0 mA. Using the 8–pin versions at voltages less than 5.0 V operates the error amplifier at lower values of gain, so that more output capacitance is needed for stability. For the worst case operating condition of a 100 mA load at 1.23 V output (Output Pin 1 connected to the feedback Pin 7) a minimum capacitance of 3.3 μF is recommended.

The LP2950 will remain stable and in regulation when operated with no output load. When setting the output voltage of the LP2951 with external resistors, the resistance values should be chosen to draw a minimum of 1.0 μA.

A bypass capacitor is recommended across the LP2950/LP2951 input to ground if more than 4 inches of wire connects the input to either a battery or power supply filter capacitor.

Input capacitance at the LP2951 Feedback Pin 7 can create a pole, causing instability if high value external resistors are used to set the output voltage. Adding a 100 pF capacitor between the Output Pin 1 and the Feedback Pin 7 and increasing the output filter capacitor to at least 3.3 μF will stabilize the feedback loop.

Error Detection Comparator

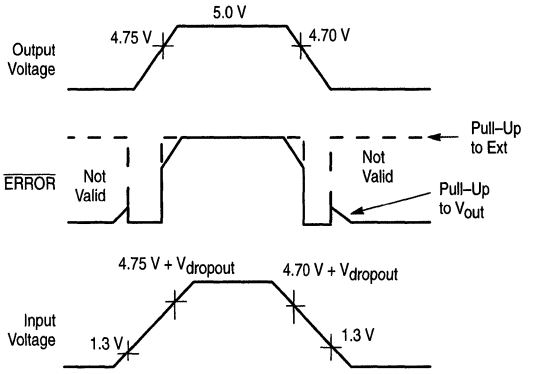
The comparator switches to a positive logic low whenever the LP2951 output voltage falls more than approximately 5.0% out of regulation. This value is the comparator's designed–in offset voltage of 60 mV divided by the 1.235 V internal reference. As shown in the representative block diagram. This trip level remains 5.0% below normal regardless of the value of regulated output voltage. For example, the error flag trip level is 4.75 V for a normal 5.0 V regulated output, or 9.50 V for a 10 V output voltage.

Figure 1 is a timing diagram which shows the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the input voltage to the LP2951 is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3 V input. It goes high when the input reaches about 5.0 V (V_{out} exceeds about 4.75 V). Since the LP2951's dropout voltage is dependent upon the load current (refer to the curve in the Typical Performance Characteristics), the input voltage trip point will vary with load current. The output voltage trip point does not vary with load.

The error comparator output is an open collector which requires an external pull–up resistor. This resistor may be returned to the output or some other voltage within the system. The resistance value should be chosen to be consistent with the 400 μA sink capability of the error comparator. A value between 100 k and 1.0 MΩ is suggested. No pull–up resistance is required if this output is unused.

When operated in the shutdown mode, the error comparator output will go high if it has been pulled up to an external supply. To avoid this invalid response, the error comparator output should be pulled up to V_{out} (see Figure 15).

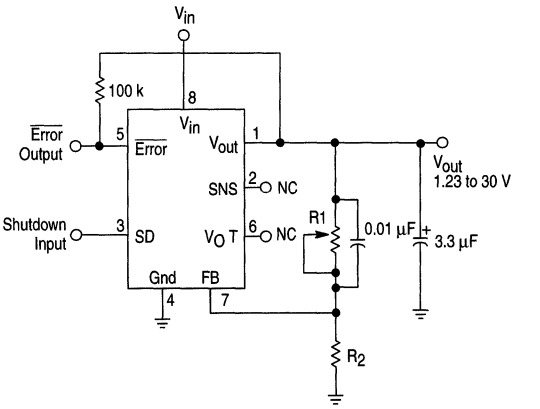
Figure 15. ERROR Output Timing



Programming the Output Voltage (LP2951)

The LP2951CX may be pin–strapped for 5.0 V using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5.0 V tap). Alternatively, it may be programmed for any output voltage between its 1.235 reference voltage and its 30 V maximum rating. An external pair of resistors is required, as shown in Figure 16.

Figure 16. Adjustable Regulator



The complete equation for the output voltage is:

$$V_{out} = V_{ref} (1 + R1/R2) + I_{FB} R1$$

where V_{ref} is the nominal 1.235 V reference voltage and I_{FB} is the feedback pin bias current, nominally −20 nA. The minimum recommended load current of 1.0 μA forces an upper limit of 1.2 MΩ on the value of R2, if the regulator must work with no load. I_{FB} will produce a 2% typical error in V_{out} which may be eliminated at room temperature by adjusting R1. For better accuracy, choosing R2 = 100 k reduces this

error to 0.17% while increasing the resistor program current to 12 μA. Since the LP2951 typically draws 75 μA at no load with Pin 2 open circuited, the extra 12 μA of current drawn is often a worthwhile tradeoff for eliminating the need to set output voltage in test.

Output Noise

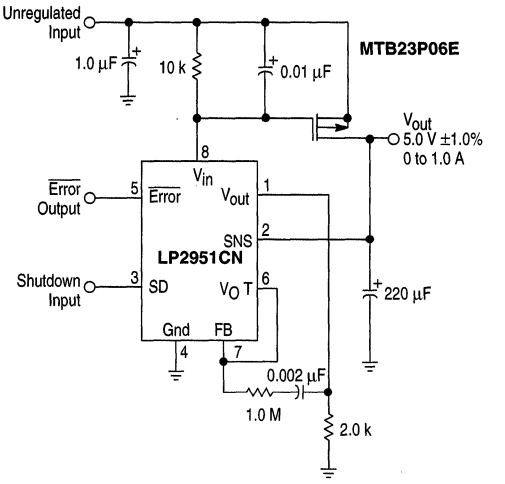
In many applications it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor is the only method for reducing noise on the 3 lead LP2950. However, increasing the capacitor from 1.0 μF to 220 μF only decreases the noise from 430 μV to 160 μVrms for a 100 kHz bandwidth at the 5.0 V output.

Noise can be reduced fourfold by a bypass capacitor across R1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{Bypass} \approx \frac{1}{2\pi R1 \times 200\ Hz}$$

or about 0.01 μF. When doing this, the output capacitor must be increased to 3.3 μF to maintain stability. These changes reduce the output noise from 430 μV to 126 μVrms for a 100 kHz bandwidth at 5.0 V output. With bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

Figure 17. 1.0 A Regulator with 1.2 V Dropout



TYPICAL APPLICATIONS

Figure 18. Lithium Ion Battery Cell Charger

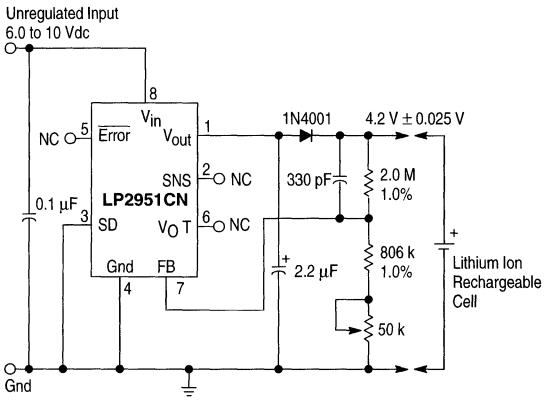


Figure 19. Low Drift Current Sink

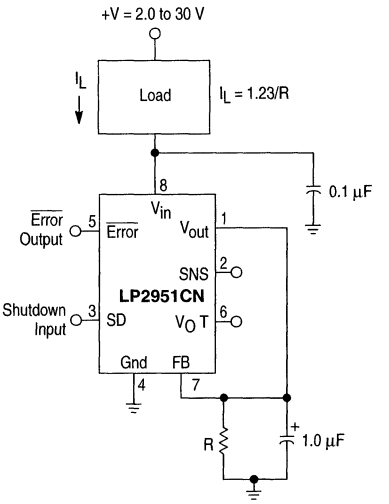
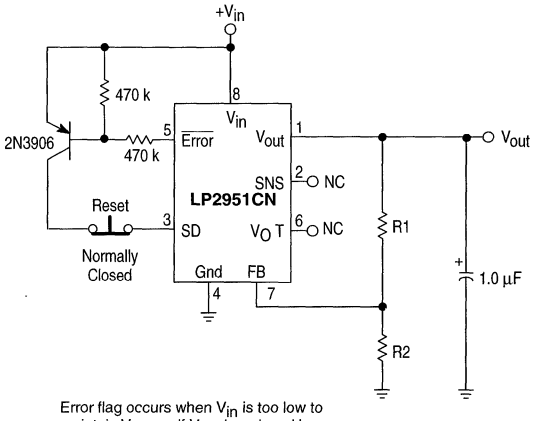


Figure 20. Latch Off When Error Flag Occurs



Error flag occurs when V_{in} is too low to maintain V_{out}, or if V_{out} is reduced by excessive load current.

Figure 21. 5.0 V Regulator with 2.5 V Sleep Function

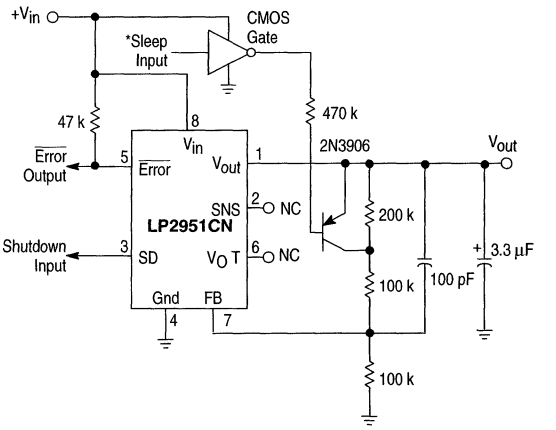
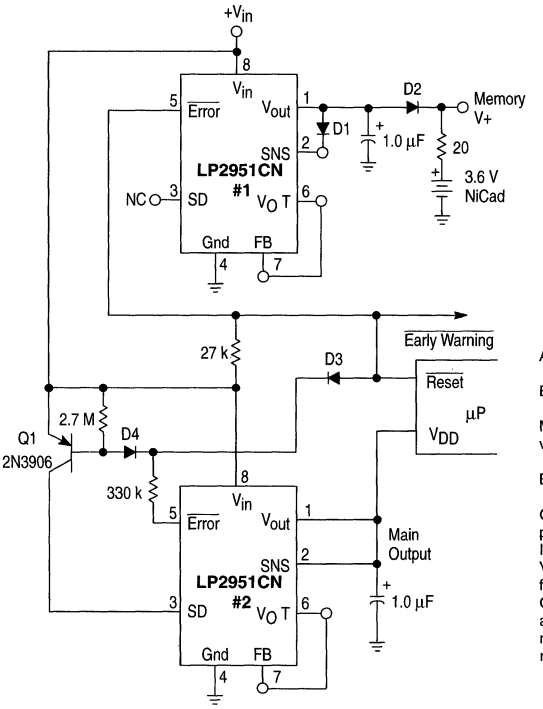


Figure 22. Regulator with Early Warning and Auxiliary Output



All diodes are 1N4148.

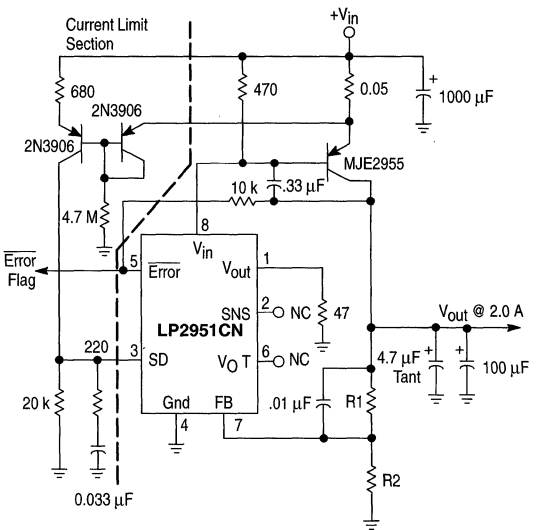
Early Warning flag on low input voltage.

Main output latches off at lower input voltages.

Battery backup on auxiliary output.

Operation: Regulator #1's V_{out} is programmed one diode drop above 5.0 V. Its error flag becomes active when $V_{in} \leq 5.7$ V. When V_{in} drops below 5.3 V, the error flag of regulator #2 becomes active and via Q1 latches the main output "off". When V_{in} again exceeds 5.7 V, regulator #1 is back in regulation and the early warning signal rises, unlatching regulator #2 via D3.

Figure 23. 2.0 A Low Dropout Regulator



$V_{out} = 1.25V\ (1.0 + R1/R2)$

For 5.0 V output, use internal resistors. Wire Pin 6 to 7, and wire Pin 2 to $+V_{out}$ Bus.

Figure 24. Open Circuit Detector for 4.0 to 20 mA Current Loop

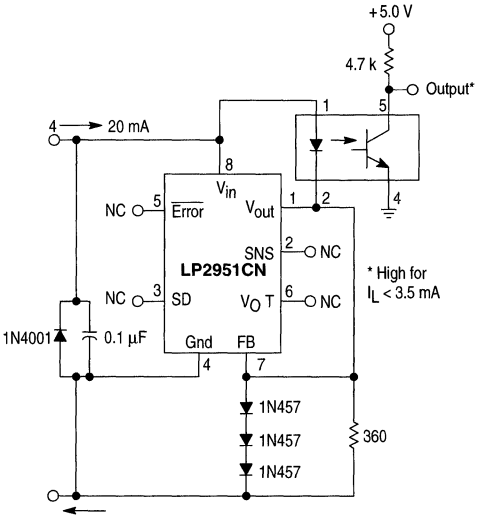


Figure 25. Low Battery Disconnect

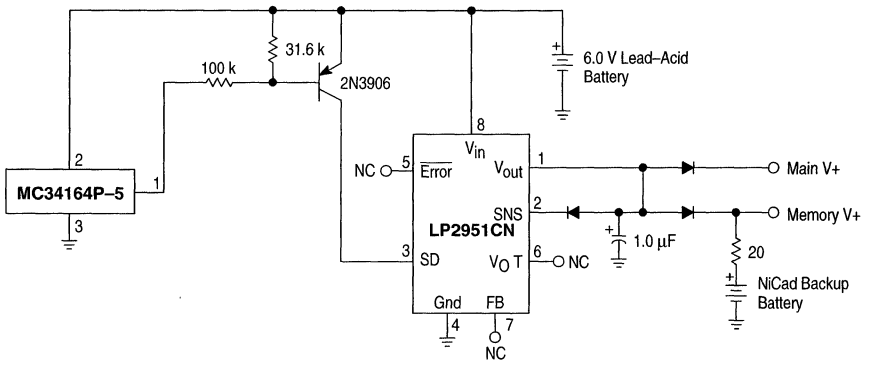
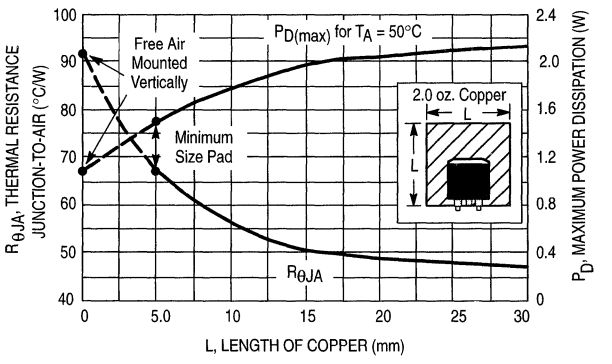


Figure 26. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MC1723C

Voltage Regulator

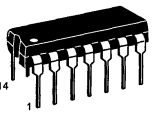
3

The MC1723C is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723C is specified for operation over the commercial temperature range (0° to +70°C).

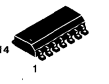
- Output Voltage Adjustable from 2.0 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short Circuit Protection

VOLTAGE REGULATOR

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

Figure 1. Representative Schematic Diagram

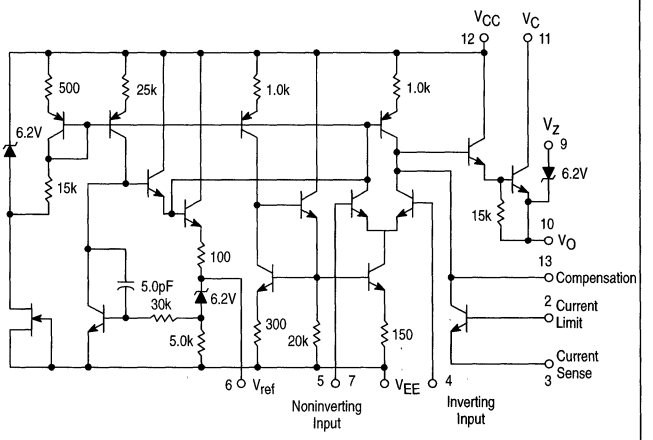
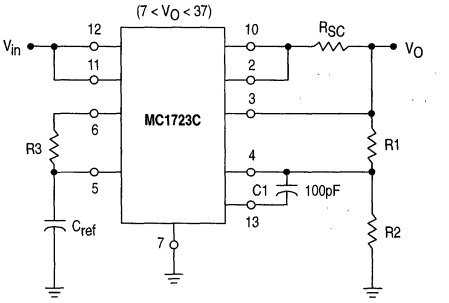


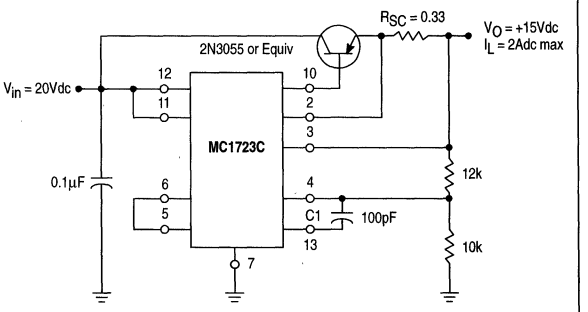
Figure 2. Typical Circuit Connection



$$V_O \cong 7\left(\frac{R1 + R2}{R2}\right) \quad I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}} \text{ at } T_J = +25°C$$

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1 ∥ R2

Figure 3. Typical NPN Current Boost Connection



ORDERING INFORMATION

Device	Alternate	Operating Temperature Range	Package
MC1723CD	–	T_A = 0° to +70°C	SO–14
MC1723CP	LM723CN µA723PC		Plastic DIP

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Pulse Voltage from V_{CC} to V_{EE} (50 ms)	$V_{I(p)}$	50	V_{pk}
Continuous Voltage from V_{CC} to V_{EE}	V_I	40	Vdc
Input–Output Voltage Differential	V_I–V_O	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Current from V_Z	I_Z	25	mA
Voltage Between Noninverting Input and V_{EE}	V_{ie}	8.0	Vdc
Differential Input Voltage	V_{id}	±5.0	Vdc
Power Dissipation and Thermal Characteristics T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction–to–Air	 P_D $1/\theta_{JA}$ θ_{JA}	 1.25 10 100	 W mW/°C °C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{in} 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 2, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Voltage Range	V_I	9.5	–	40	Vdc
Output Voltage Range	V_O	2.0	–	37	Vdc
Input–Output Voltage Differential	V_I–V_O	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_{IB}	–	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz) C_{ref} = 0 C_{ref} = 5.0 µF	V_n	 – –	 20 2.5	 – –	µV(RMS)
Average Temperature Coefficient of Output Voltage (T_{low} < T_A < T_{high})	TCV_O	–	0.003	0.015	%/°C
Line Regulation (T_A = 25°C) { 12 V < V_{in} < 15 V (T_A = 25°C) { 12 V < V_{in} < 40 V (T_{low} < T_A < T_{high}) 12 V < V_{in} < 15 V	Reg_{line}	 – – –	 0.01 0.1 –	 0.1 0.5 0.3	% V_O
Load Regulation (1.0 mA < I_L < 50 mA) T_A = 25°C T_{low} < T_A < T_{high}	Reg_{load}	 – –	 0.03 –	 0.2 0.6	% V_O
Ripple Rejection (f = 50 Hz to 10 kHz) C_{ref} = 0 C_{ref} = 5.0 µF	RR	 – –	 74 86	 – –	dB
Short Circuit Current Limit (R_{SC} = 10 Ω, V_O = 0)	I_{SC}	–	65	–	mAdc
Long Term Stability	$\Delta V_O/\Delta t$	–	0.1	–	%/1000 Hr.

NOTE: T_{low} to T_{high} = 0° to +70°C

Figure 4. Maximum Load Current as a Function of Input–Output Voltage Differential

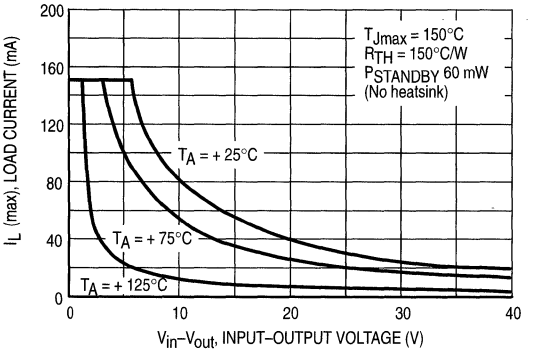


Figure 5. Load Regulation Characteristics Without Current Limiting

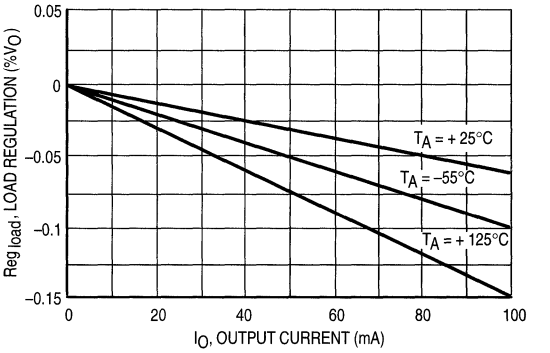


Figure 6. Load Regulation Characteristics With Current Limiting

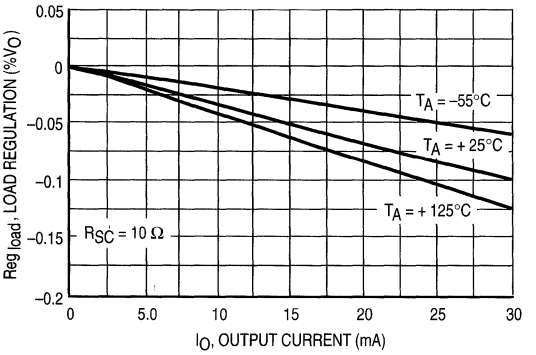


Figure 7. Load Regulation Characteristics With Current Limiting

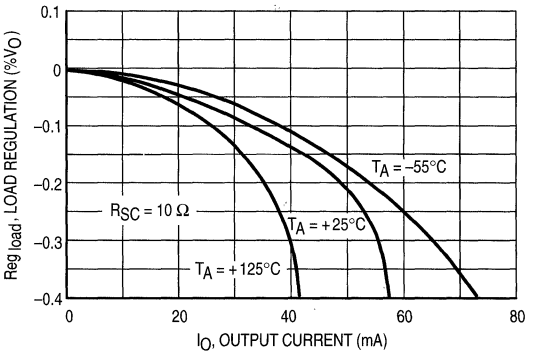


Figure 8. Current Limiting Characteristics

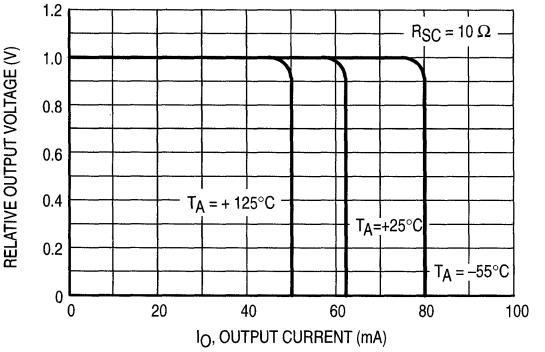


Figure 9. Current Limiting Characteristics as a Function of Junction Temperature

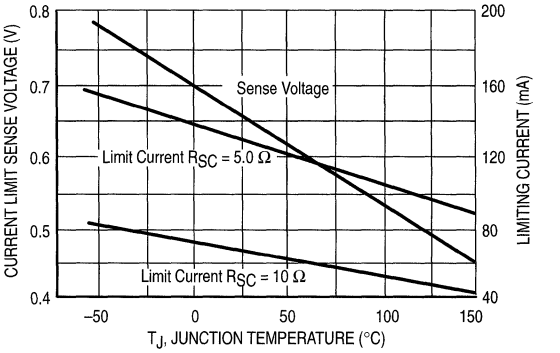


Figure 10. Line Regulation as a Function of Input–Output Voltage Differential

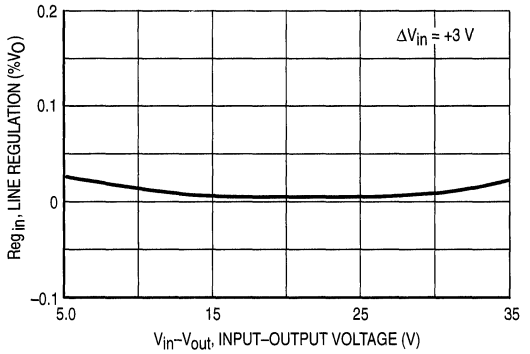


Figure 11. Load Regulation as a Function of Input–Output Voltage Differential

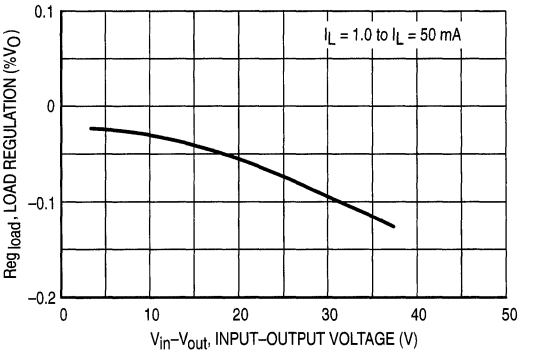


Figure 12. Standby Current Drain as a Function of Input Voltage

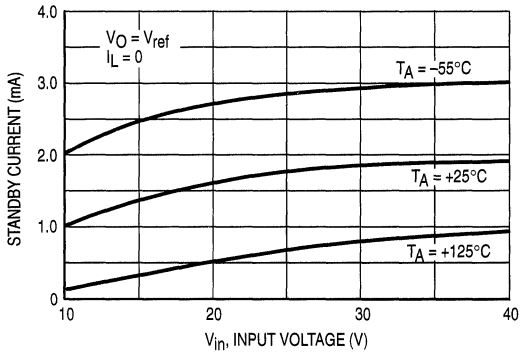


Figure 13. Line Transient Response

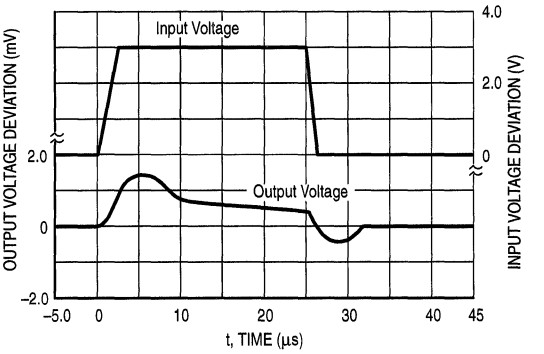


Figure 14. Load Transient Response

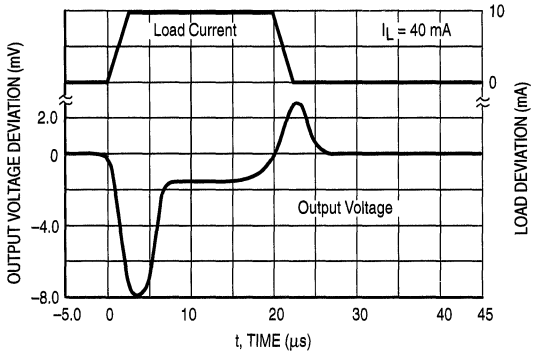


Figure 15. Output Impedance as Function of Frequency

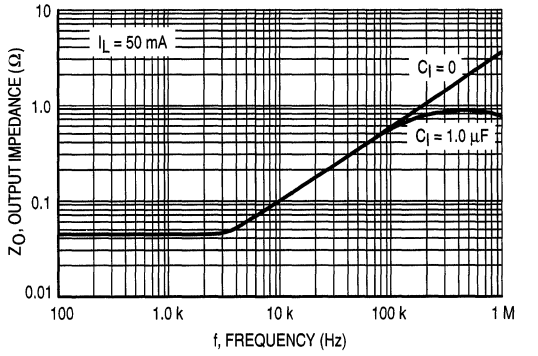
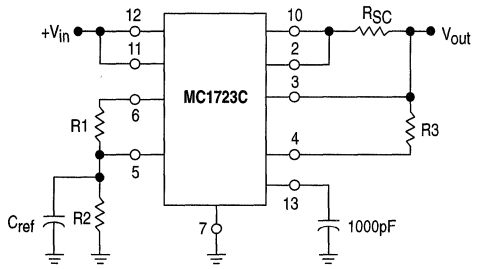


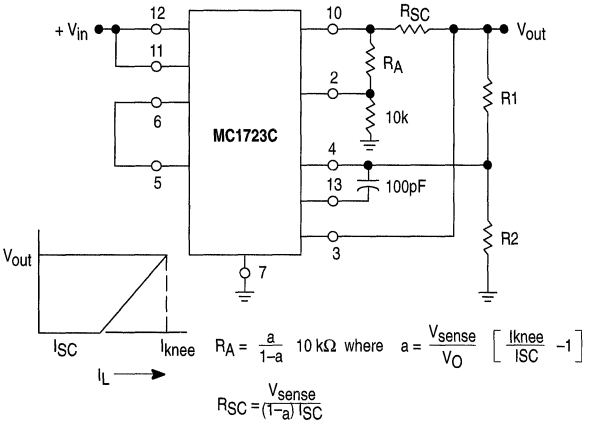
Figure 16. Typical Connection for 2 < V_O < 7



$$V_O \cong 7\left[\frac{R2}{R1+R2}\right] \qquad I_{SC} = \frac{V_{sense}}{R_{SC}} \cong \frac{0.66}{RSC} \quad \text{at } T_J = +25°C$$

For best results 10 k < R1 +R2 < 100 k
For minimum drift R3 = R1 R2

Figure 17. Foldback Connection



$$R_A = \frac{a}{1-a}\ 10\ k\Omega \text{ where } a = \frac{V_{sense}}{V_O}\left[\frac{I_{knee}}{I_{SC}} - 1\right]$$

$$R_{SC} = \frac{V_{sense}}{(1-a)\,I_{SC}}$$

Figure 18. +5.0 V, 1.0 A Switching Regulator

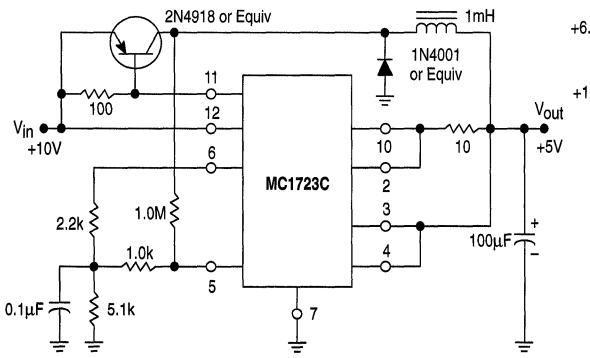


Figure 19. +5.0 V, 1.0 A High Efficiency Regulator

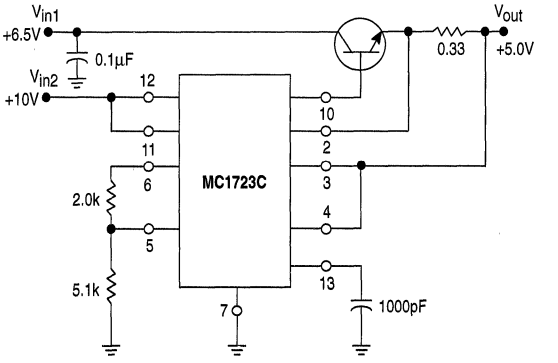


Figure 20. +15 V, 1.0 A Regulator with Remote Sense

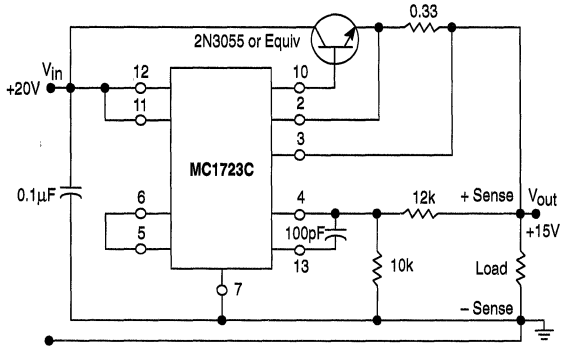


Figure 21. –15 V Negative Regulator

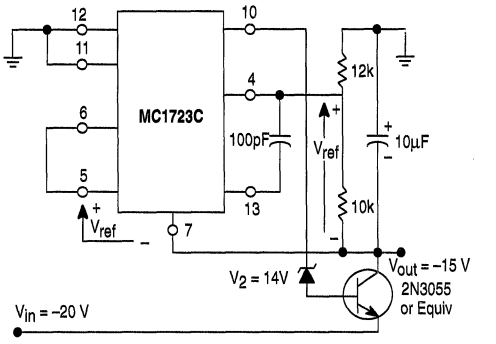
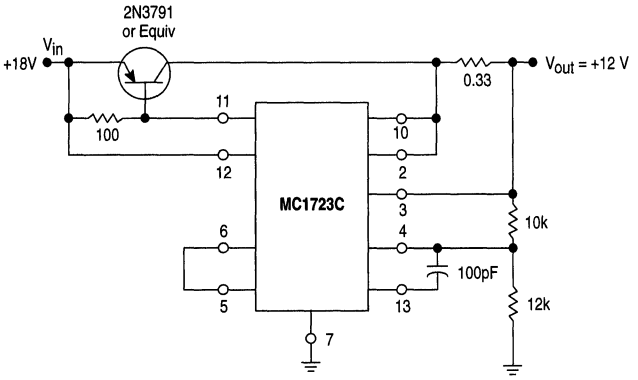


Figure 22. +12V, 1.0 A Regulator
(Using PNP Current Boost)



MC3423

Overvoltage Crowbar Sensing Circuit

3

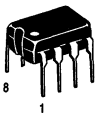
This overvoltage protection circuit (OVP) protects sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. The device senses the overvoltage condition and quickly "crowbars" or short circuits the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

The protection voltage threshold is adjustable and the MC3423 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

The MC3423 is essentially a "two terminal" system, therefore it can be used with either positive or negative supplies.

OVERVOLTAGE SENSING CIRCUIT

SEMICONDUCTOR TECHNICAL DATA



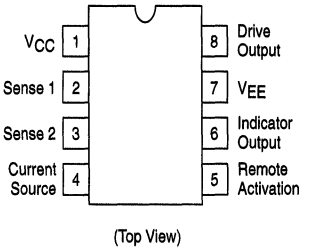
P1 SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)

MAXIMUM RATINGS

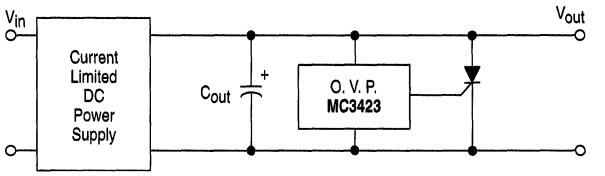
Rating	Symbol	Value	Unit
Differential Power Supply Voltage	$V_{CC}-V_{EE}$	40	Vdc
Sense Voltage (1)	V_{Sense1}	6.5	Vdc
Sense Voltage (2)	V_{Sense2}	6.5	Vdc
Remote Activation Input Voltage	V_{act}	7.0	Vdc
Output Current	I_O	300	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

PIN CONNECTIONS



(Top View)

Simplified Application



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3423D	T_A = 0° to +70°C	SO–8
MC3423P1		Plastic DIP

ELECTRICAL CHARACTERISTICS ($5.0\ V \le V_{CC} - V_{EE} \le 36\ V$, $T_{low} < T_A < T_{high}$, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}–V_{EE}	4.5	–	40	Vdc
Output Voltage (I_O = 100 mA)	V_O	V_{CC}–2.2	V_{CC}–1.8	–	Vdc
Indicator Output Voltage ($I_{O(Ind)}$ = 1.6 mA)	$V_{OL(Ind)}$	–	0.1	0.4	Vdc
Sense Trip Voltage (T_A = 25°C)	V_{Sense1}, V_{Sense2}	2.45	2.6	2.75	Vdc
Temperature Coefficient of V_{Sense1} (Figure 2)	TCV_{S1}	–	0.06	–	%/°C
Remote Activation Input Current (V_{IH} = 2.0 V, $V_{CC} - V_{EE}$ = 5.0 V) (V_{IL} = 0.8 V, $V_{CC} - V_{EE}$ = 5.0 V)	I_{IH} I_{IL}	– –	5.0 –120	40 –180	µA
Source Current	I_{Source}	0.1	0.2	0.3	mA
Output Current Risetime (T_A = 25°C)	t_r	–	400	–	mA/µs
Propagation Delay Time (T_A = 25°C)	t_{pd}	–	0.5	–	µs
Supply Current	I_D	–	6.0	10	mA

NOTES: T_{low} to T_{high} = 0° to +70°C

Figure 1. Representative Block Diagram

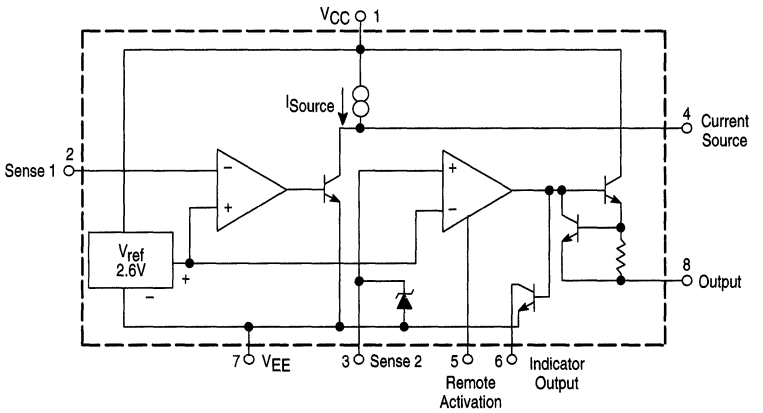
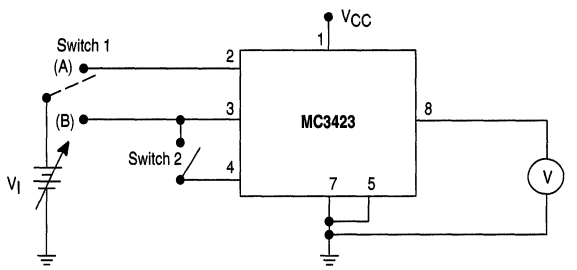


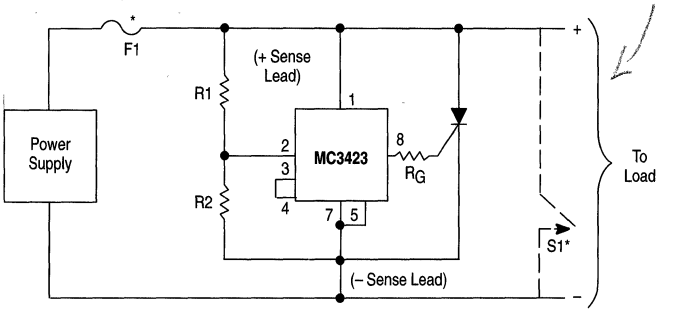
Figure 2. Sense Voltage Test Circuit



	Switch 1	Switch 2
$V_{Sense\ 1}$	Position A	Closed
$V_{Sense\ 2}$	Position B	Open

Ramp V_I until output goes high; this is the V_{Sense} threshold.

Figure 3. Basic Circuit Configuration



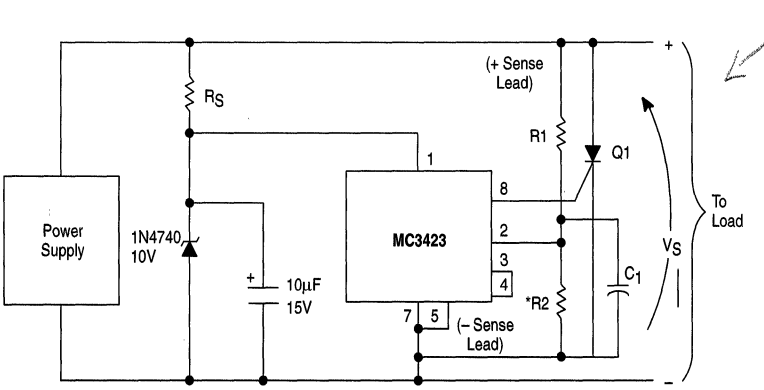
$$V_{trip} = V_{ref}\left(1 + \frac{R1}{R2}\right) \approx 2.6\ V\left(1 + \frac{R1}{R2}\right)$$

$R2 \leq 10\ k\Omega$ for minimum drift

For minimum value of R_G, see Figure 9.

*See text for explanation.

Figure 4. Circuit Configuration for Supply Voltage Above 36 V



$$C_1 > \frac{R_S}{R_1 R_2}\ (R_1 + R_2)\ 10\mu F$$

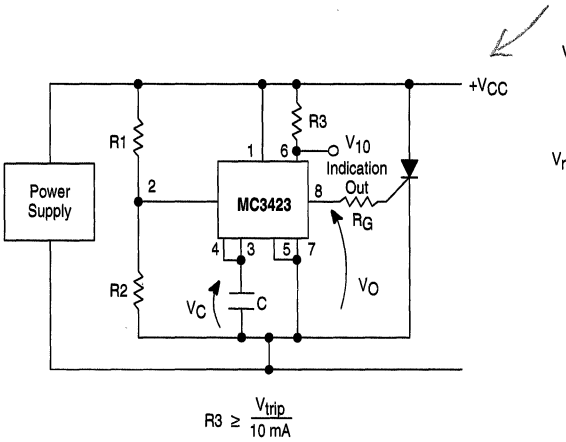
$$R_S = \left(\frac{V_S - 10}{25}\right) k\Omega$$

$$V_{trip} = V_{ref}\left(1 + \frac{R1}{R2}\right) \approx 2.6\ V\left(1 + \frac{R1}{R2}\right)$$

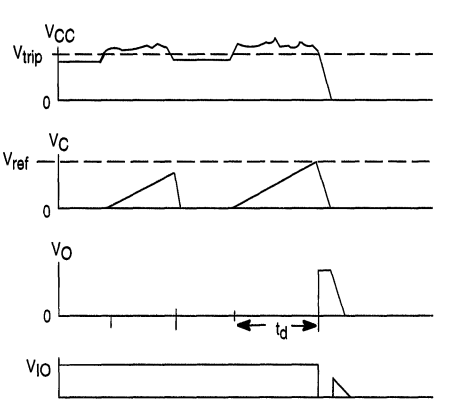
*$R2 \leq 10\ k\Omega$

Q1: $V_S \leq 50$ V; 2N6504 or equivalent
$V_S \leq 100$ V; 2N6505 or equivalent
$V_S \leq 200$ V; 2N6506 or equivalent
$V_S \leq 400$ V; 2N6507 or equivalent
$V_S \leq 600$ V; 2N6508 or equivalent
$V_S \leq 800$ V; 2N6509 or equivalent

Figure 5. Basic Configuration for Programmable Duration of Overvoltage Condition Before Trip



$$R3 \geq \frac{V_{trip}}{10\ mA}$$



$$t_d = \frac{V_{ref}}{I_{source}} \times C \approx [12 \times 10^3]\ C$$

(See Figure 10)

APPLICATION INFORMATION

Basic Circuit Configuration

The basic circuit configuration of the MC3423 OVP is shown in Figure 3 for supply voltages from 4.5 V to 36 V, and in Figure 4 for trip voltages above 36 V. The threshold or trip voltage at which the MC3423 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 3 and 4, or by the graph shown in Figure 8. The minimum value of the gate current limiting resistor, R_G, is given in Figure 9. Using this value of R_G, the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423. If lower output currents are required, R_G can be increased in value. The switch, S1, shown in Figure 3 may be used to reset the crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current–limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

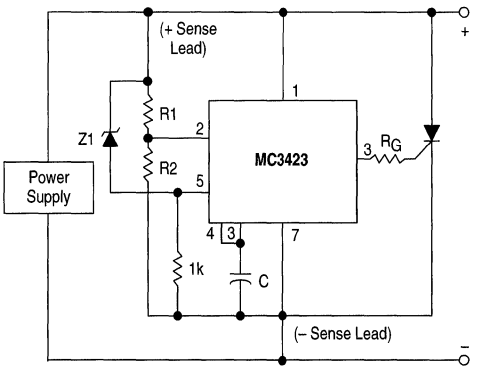
The circuit configurations shown in Figures 3 and 4 will have a typical propogation delay of 1.0 µs. If faster operation is desired, Pin 3 may be connected to Pin 2 with Pin 4 left floating. This will result in decreasing the propogation delay to approximately 0.5 µs at the expense of a slightly increased TC for the trip voltage value.

Configuration for Programmable Minimum Duration of Overvoltage Condition Before Tripping

In many instances, the MC3423 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 5 is used. In this configuration, a capacitor is connected from Pin 3 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 10. The circuit operates in the following manner: When V_{CC} rises above the trip point set by R1 and R2, an internal current source (Pin 4) begins charging the capacitor, C, connected to Pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate ≅ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occur when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 5. In this case, the circuit of Figure 6 can be used. The circuit will operate as previously described for small overvoltages, but will immediately trip if the power supply voltage exceeds V_{Z1} + 1.4 V.

Figure 6. Configuration for Programmable Duration of Overvoltage Condition Before Trip/With Immediate Trip at High Overvoltages



Additional Features

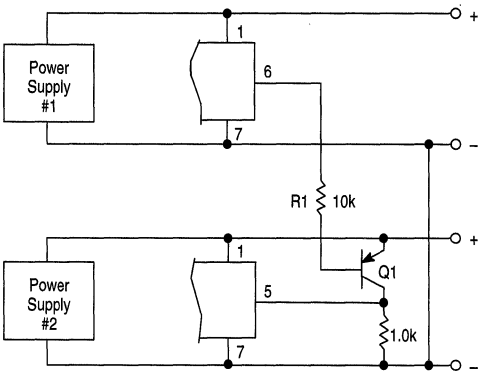
1. Activation Indication Output

An additional output for use as an indicator of OVP activation is provided by the MC3423. This output is an open collector transistor which saturates when the OVP is activated. In addition, it can be used to clock an edge triggered flip–flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

2. Remote Activation Input

Another feature of the MC3423 is its remote activation input, Pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that Pin 5 has an internal pull–up current source. This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423 can be used to activate another MC3423 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 7. In this circuit, the indication output (Pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

Figure 7. Circuit Configuration for Activating One MC3423 from Another



Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

Crowbar SCR Considerations

Referring to Figure 11, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 11A, the supply's input filter caps. This surge current is illustrated in Figure 12, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned–on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities – depending on the severity of the occasion.

Figure 8. R1 versus Trip Voltage

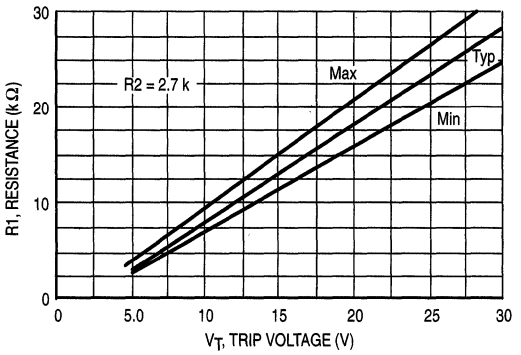


Figure 9. Minimum R_G versus Supply Voltage

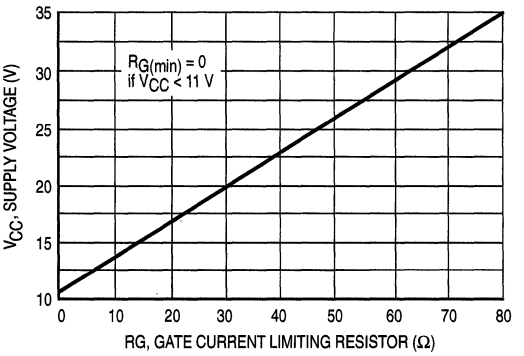


Figure 10. Capacitance versus Minimum Overvoltage Duration

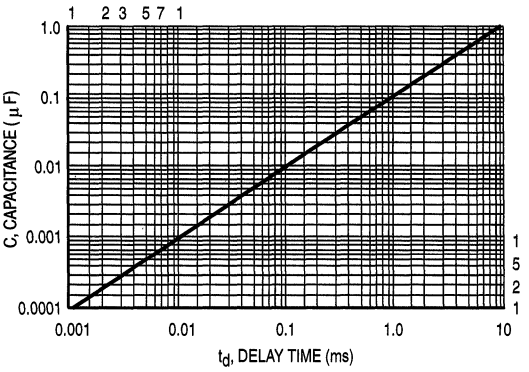


Figure 11. Typical Crowbar OVP Circuit Configurations

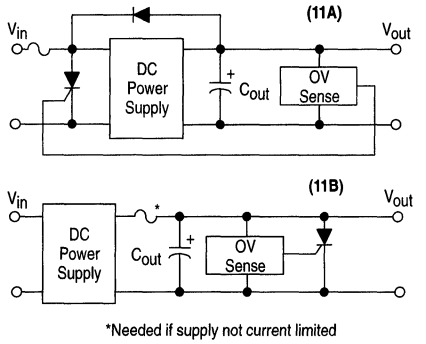


Figure 12. Crowbar SCR Surge Current Waveform

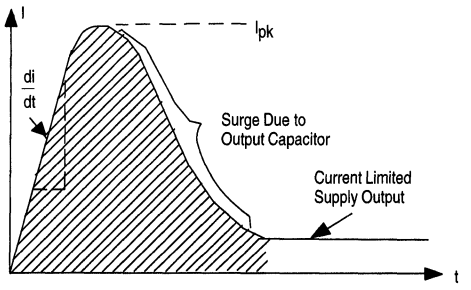
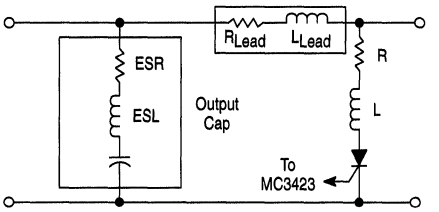


Figure 13. Circuit Elements Affecting SCR Surge and di/dt



The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center–gate–fire SCR has more di/dt capability than a corner–gate–fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast < 1.0 µs rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/µs, assuming a gate current of five times I_{GT} and < 1.0 µs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 13. Of course, this reduces the circuit's ability to rapidly reduce the DC bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance – see Figure 13) to a safe level which is consistent with the systems requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the DC power supply.

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 11A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

Device	I_{RMS}	I_{FSM}	Package
2N6400 Series	16 A	160 A	TO–220 Plastic
2N6504 Series	25 A	160 A	TO–220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N2573 Series	25 A	260 A	Metal TO–3 Type
2N681 Series	25 A	200 A	Metal Stud
MCR3935–1 Series	35 A	350 A	Metal Stud
MCR81–5 Series	80 A	1000 A	Metal Stud

3

Power Supply Supervisory/ Over and Undervoltage Protection Circuit

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. These integrated circuits contain dedicated over and undervoltage sensing channels with independently programmable time delays. The overvoltage channel has a high current Drive Output for use in conjunction with an external SCR Crowbar for shutdown. The undervoltage channel input comparator has hysteresis which is externally programmable, and an open–collector output for fault indication.

- Dedicated Over and Undervoltage Sensing
- Programmable Hysteresis of Undervoltage Comparator
- Internal 2.5 V Reference
- 300 mA Overvoltage Drive Output
- 30 mA Undervoltage Indicator Output
- Programmable Time Delays
- 4.5 V to 40 V Operation

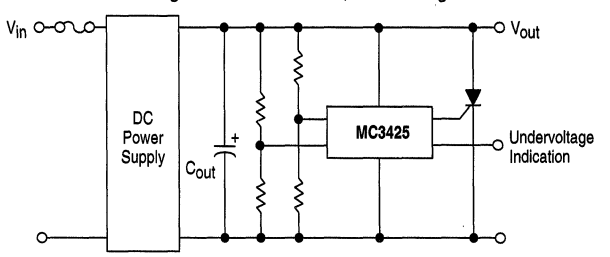
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range (Note 1)	V_{IR}	–0.3 to +40	Vdc
Drive Output Short Circuit Current	$I_{OS(DRV)}$	Internally Limited	mA
Indicator Output Voltage	V_{IND}	0 to 40	Vdc
Indicator Output Sink Current	I_{IND}	30	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$	 1000 80	 mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

NOTE: 1. The input signal voltage should not be allowed to go negative by more than 300 mV or positive by more than 40 V, independent of V_{CC}, without device destruction.

Simplified Application

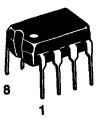
Overvoltage Crowbar Protection, Undervoltage Indication



MC3425

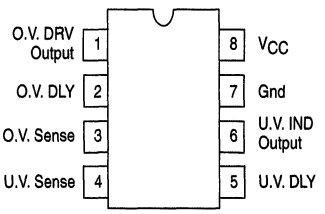
POWER SUPPLY SUPERVISORY/ OVER AND UNDERVOLTAGE PROTECTION CIRCUIT

SEMICONDUCTOR TECHNICAL DATA



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3425P1	T_A = 0° to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS ($4.5\ V \le V_{CC} \le 40\ V$; $T_A = T_{low}$ to T_{high} [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Sense Trip Voltage (Referenced Voltage) V_{CC} = 15 V T_A = 25°C T_{low} to T_{high} (Note 2)	V_{Sense}	 2.4 2.33	 2.5 2.5	 2.6 2.63	Vdc
Line Regulation of V_{Sense} $4.5\ V \le V_{CC} \le 40\ V$; T_J = 25°C	Reg_{line}	–	7.0	15	mV
Power Supply Voltage Operating Range	V_{CC}	4.5	–	40	Vdc
Power Supply Current V_{CC} = 40 V; T_A = 25°C; No Output Loads O.V. Sense (Pin 3) = 0 V; U.V. Sense (Pin 4) = V_{CC}	$I_{CC(off)}$	–	8.5	10	mA
O.V. Sense (Pin 3) = V_{CC}; U.V. Sense (Pin 4) = 0 V	$I_{CC(on)}$	–	16.5	19	mA
INPUT SECTION					
Input Bias Current, O.V. and U.V. Sense	I_{IB}	–	1.0	2.0	µA
Hysteresis Activation Voltage, U.V. Sense V_{CC} = 15 V; T_A = 25°C; I_H = 10% I_H = 90%	$V_{H(act)}$	 – –	 0.6 0.8	 – –	V
Hysteresis Current, U.V. Sense V_{CC} = 15 V; T_A = 25°C; U.V. Sense (Pin 4) = 2.5 V	I_H	9.0	12.5	16	µA
Delay Pin Voltage (I_{DLY} = 0 mA) Low State High State	 $V_{OL(DLY)}$ $V_{OH(DLY)}$	 – V_{CC}–0.5	 0.2 V_{CC}–0.15	 0.5 –	V
Delay Pin Source Current V_{CC} = 15 V; V_{DLY} = 0 V	$I_{DLY(source)}$	140	200	260	µA
Delay Pin Sink Current V_{CC} = 15 V; V_{DLY} = 2.5V	$I_{DLY(sink)}$	1.8	3.0	–	mA
OUTPUT SECTION					
Drive Output Peak Current (T_A = 25°C)	$I_{DRV(peak)}$	200	300	–	mA
Drive Output Voltage I_{DRV} = 100 mA; T_A = 25° C	$V_{OH(DRV)}$	V_{CC}–2.5	V_{CC}–2.0	–	V
Drive Output Leakage Current V_{DRV} = 0 V	$I_{DRV(leak)}$	–	15	200	nA
Drive Output Current Slew Rate (T_A = 25°C)	di/dt	–	2.0	–	A/µs
Drive Output V_{CC} Transient Rejection V_{CC} = 0 V to 15 V at dV/dt = 200 V µs; O.V. Sense (Pin 3) = 0 V; T_A = 25°C	$I_{DRV(trans)}$	–	1.0	–	mA (Peak)
Indicator Output Saturation Voltage I_{IND} = 30 mA; T_A = 25°C	$V_{IND(sat)}$	–	560	800	mV
Indicator Output Leakage Current $V_{OH(IND)}$ = 40 V	$I_{IND(leak)}$	–	25	200	nA
Output Comparator Threshold Voltage (Note 3)	$V_{th(OC)}$	2.33	2.5	2.63	V
Propagation Delay Time (V_{CC} = 15 V; T_A = 25°C) Input to Drive Output or Indicator Output 100 mV Overdrive, C_{DLY} = 0 µF	$t_{PLH(IN/OUT)}$	–	1.7	–	µs
Input to Delay 2.5 V Overdrive (0 V to 5.0 V Step)	$t_{PLH(IN//DLY)}$	–	700	–	ns

NOTES: 2. T_{low} to T_{high} = 0° to +70°C
3. The $V_{th(OC)}$ limits are approximately the V_{Sense} limits over the applicable temperature range.

3

Figure 1. Hysteresis Current versus Hysteresis Activation Voltage

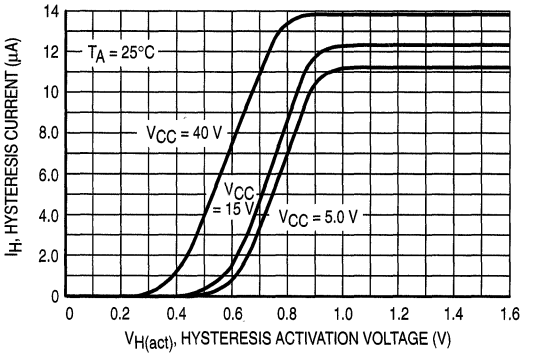


Figure 2. Hysteresis Activation Voltage versus Temperature

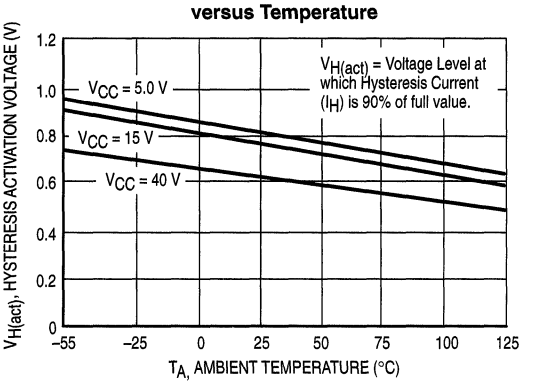


Figure 3. Hysteresis Current versus Temperature

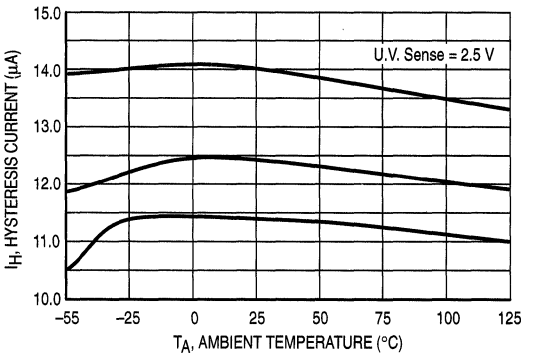


Figure 4. Sense Trip Voltage Change versus Temperature

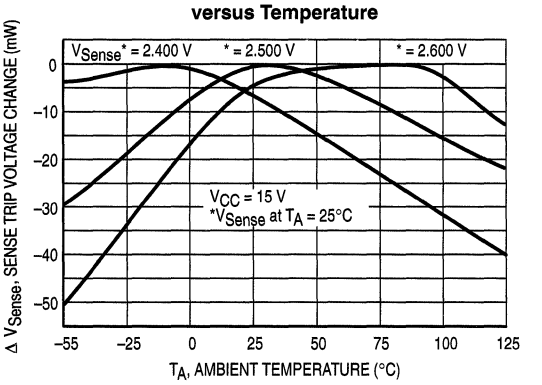


Figure 5. Output Delay Time versus Delay Capacitance

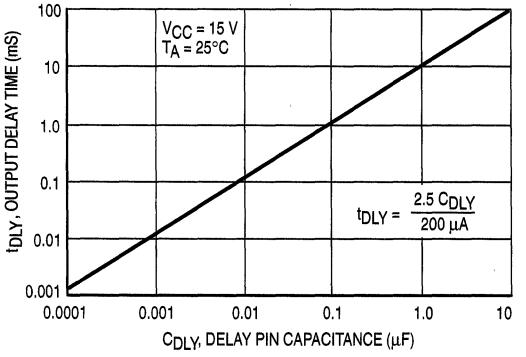


Figure 6. Delay Pin Source Current versus Temperature

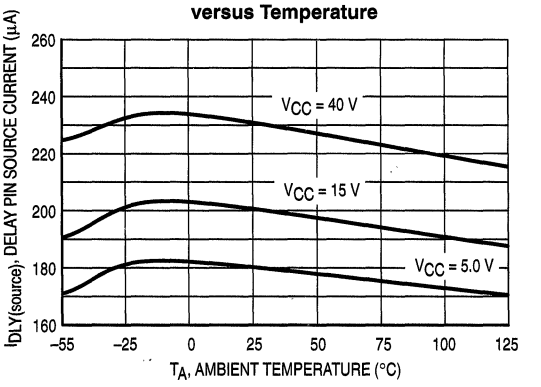


Figure 7. Drive Output Saturation Voltage versus Output Peak Current

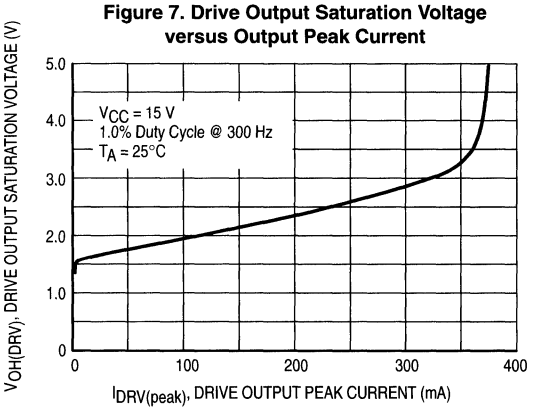


Figure 8. Indicator Output Saturation Voltage versus Output Sink Current

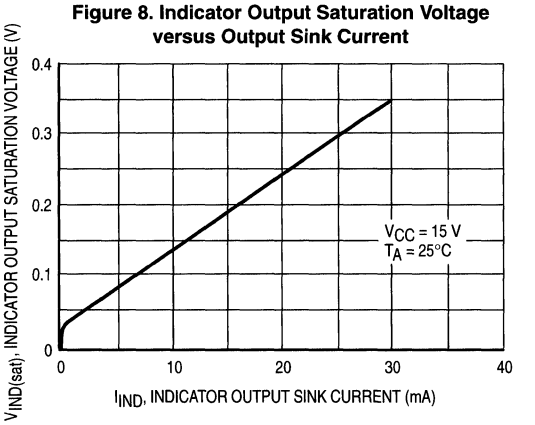


Figure 9. Drive Output Saturation Voltage versus Temperature

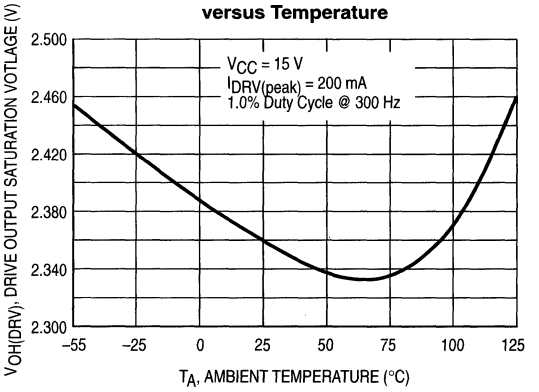
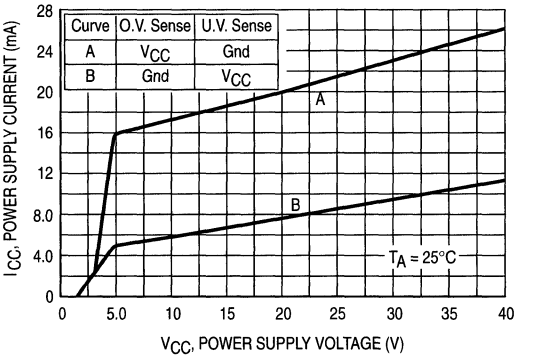


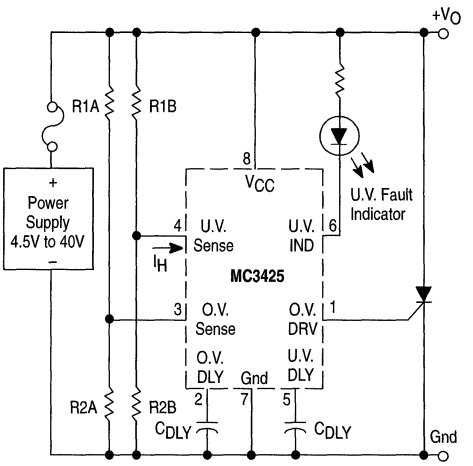
Figure 10. Power Supply Current versus Voltage



APPLICATIONS INFORMATION

3

Figure 11. Overvoltage Protection and Undervoltage Fault Indication with Programmable Delay



$$\text{U.V. Hysteresis} = I_H \left(\frac{R1B\ R2B}{R1B + R2B} \right), V_{O(trip)} - 2.5\ V \left(1 + \frac{R1A}{R2A} \right)$$

$$t_{DLY} = 12500\ C_{DLY}$$

Figure 12. Overvoltage Protection of 5.0 V Supply with Line Loss Detector

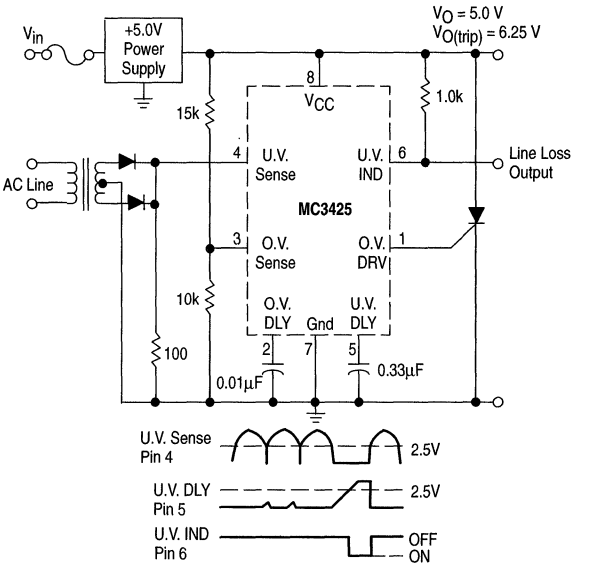


Figure 13. Overvoltage Audio Alarm Circuit

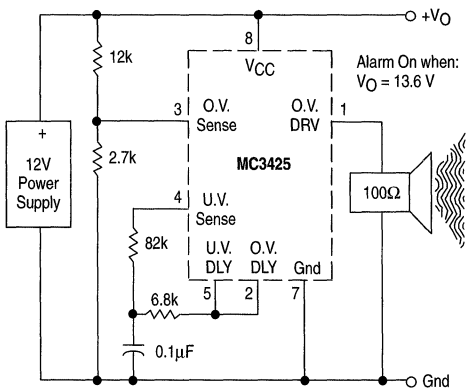
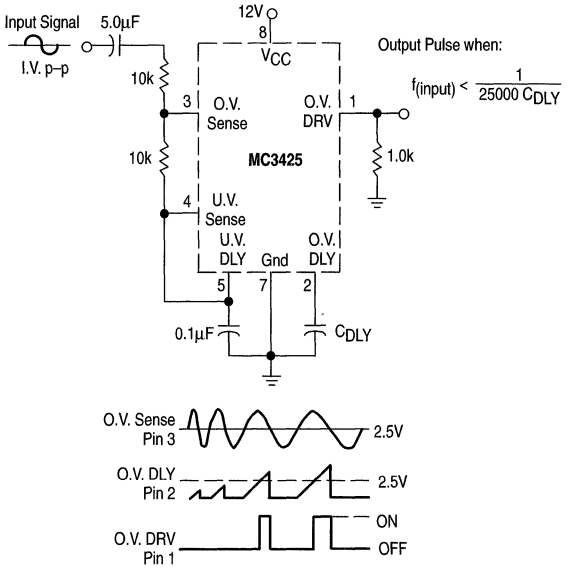


Figure 14. Programmable Frequency Switch



CIRCUIT DESCRIPTION

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. The block diagram is shown below in Figure 15. The Overvoltage (O.V.) and Undervoltage (U.V.) Input Comparators are both referenced to an internal 2.5 V regulator. The U.V. Input Comparator has a feedback activated 12.5 μA current sink (I_H) which is used for programming the input hysteresis voltage (V_H). The source resistance feeding this input (R_H) determines the amount of hysteresis voltage by $V_H = I_H R_H = 12.5 \times 10^{-6} R_H$.

Separate Delay pins (O.V. DLY, U.V. DLY.) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY(source)}$, of typically 200 μA when the noninverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time (t_{DLY}) for the Drive and Indicator outputs. The Delay pins are internally connected to the noninverting inputs of the O.V. and U.V. Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time (t_{DLY}) is based on the constant current source, $I_{DLY(source)}$, charging the external delay capacitor (C_{DLY}) to 2.5 V.

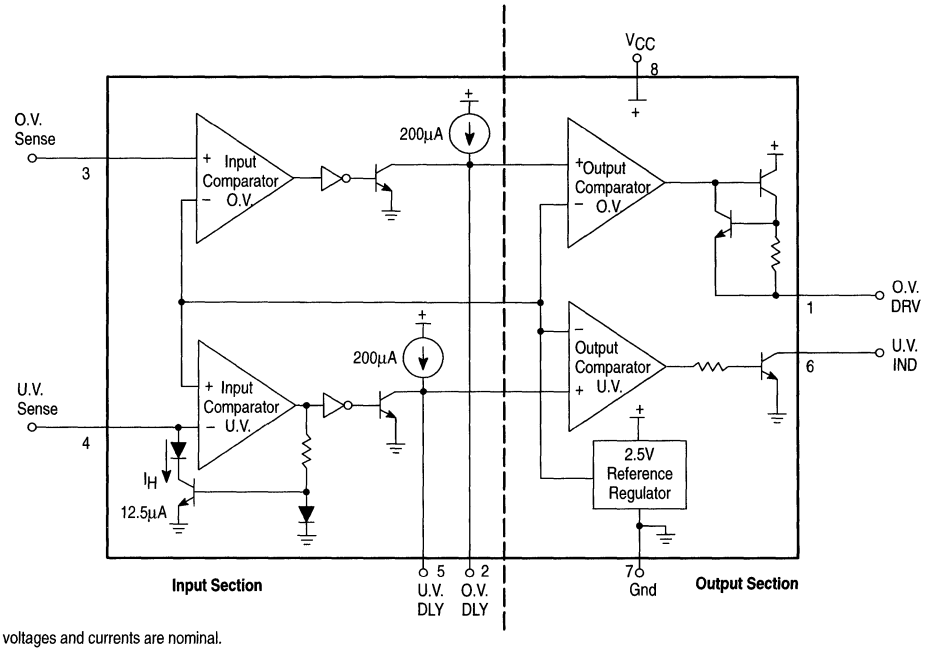
$$t_{DLY} = \frac{V_{ref}\, C_{DLY}}{I_{DLY(source)}} = \frac{2.5\, C_{DLY}}{200\ \mu A} = 12500\, C_{DLY}$$

Figure 5 provides C_{DLY} values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's noninverting input is less than the inverting input. The sink current, $I_{DLY(sink)}$, capability of the Delay pins is ≥ 1.8 mA and is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

The Overvoltage Drive Output is a current–limited emitter–follower capable of sourcing 300 mA at a turn–on slew rate at 2.0 A/μs, ideal for driving "Crowbar" SCR's. The Undervoltage Indicator Output is an open–collector, NPN transistor, capable of sinking 30 mA to provide sufficient drive for LED's, small relays or shut–down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded.

The MC3425 has an internal 2.5 V bandgap reference regulator with an accuracy of ± 4.0% for the basic device.

Figure 15. Representative Block Diagram



Note: All voltages and currents are nominal.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 16, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 16A, the supply's input filter capacitors. This surge current is illustrated in Figure 17, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

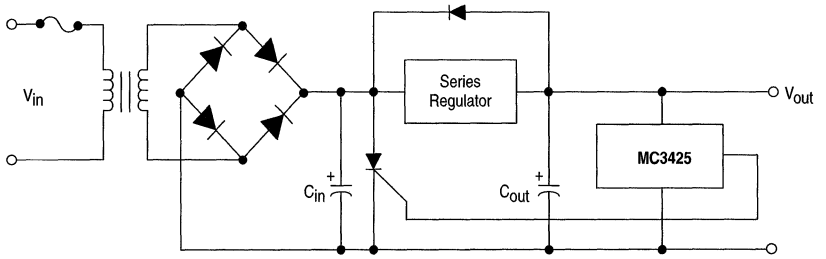
1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned–on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities – depending on the severity of the occasion.

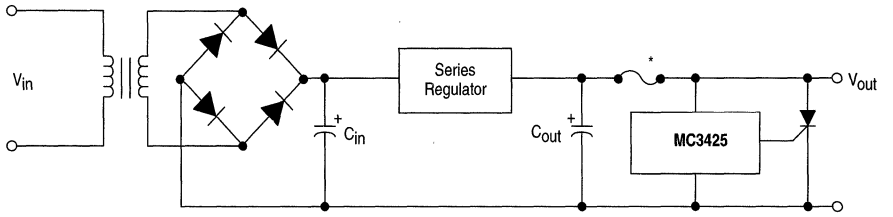
The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center–gate–fire SCR has more di/dt capability than a corner–gate–fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast < 1.0 µs rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/µs, assuming a gate current of five times I_{GT} and < 1.0 µs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 18. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

Figure 16. Typical Crowbar Circuit Configurations

(A) SCR Across Input of Regulator

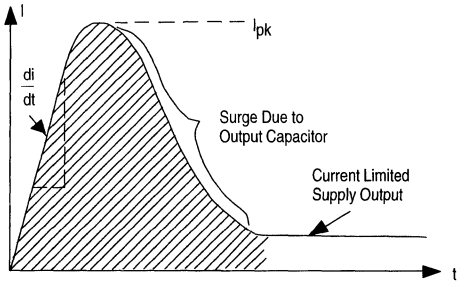


(B) SCR Across Output of Regulator



*Needed if supply is not current limited.

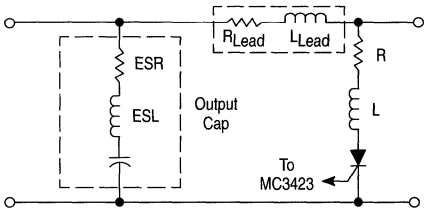
Figure 17. Crowbar SCR Surge Current Waveform



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance – see Figure 18) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the DC power supply.

Figure 18. Circuit Elements Affecting SCR Surge & di/dt



R & L EMPIRICALLY DETERMINED!

UNDERVOLTAGE SENSING

An undervoltage sense circuit with hysteresis may be designed, as shown in Figure 11, using the following equations:

$$R1 = \frac{V_{CCU} - V_{CC1}}{12.5\ \mu A}$$

$$R2 = \frac{2.5\ R1}{V_{CC1} - 2.5}$$

where: V_{CCU} is the designed upper trip point (output indicator goes off)
V_{CC1} is the lower trip point (output indicator goes on)

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 16A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 16B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

Device	I_{RMS}	I_{TSM}
MCR310 Series	10 A	100 A
MCR16 Series	16 A	150 A
MCR25 Series	25 A	300 A
2N6501 Series	25 A	300 A
MCR69 Series	25 A	750 A
MCR264 Series	40 A	400 A
MCR265 Series	55 A	550 A

MC7800 Series

3

Three-Terminal Positive Voltage Regulators

These voltage regulators are monolithic integrated circuits designed as fixed–voltage regulators for a wide variety of applications including local, on–card regulation. These regulators employ internal current limiting, thermal shutdown, and safe–area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 A. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

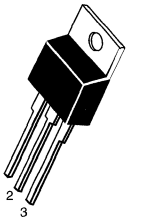
- Output Current in Excess of 1.0 A
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Output Voltage Offered in 2% and 4% Tolerance
- Available in Surface Mount D^2PAK and Standard 3–Lead Transistor Packages

THREE–TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA

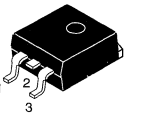
T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface connected to Pin 2.



Pin 1. Input
2. Ground
3. Output

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D^2PAK)



Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

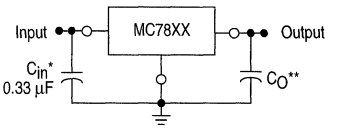
MC7805	5.0 V	MC7812	12 V
MC7806	6.0 V	MC7815	15 V
MC7808	8.0 V	MC7818	18 V
MC7809	9.0 V	MC7824	24 V

ORDERING INFORMATION

Device	Output Voltage Tolerance	Operating Temperature Range	Package
MC78XXACT	2%	T_J = 0° to +125°C	Insertion Mount
MC78XXACD2T			Surface Mount
MC78XXCT	4%		Insertion Mount
MC78XXCD2T			Surface Mount
MC78XXBT		T_J = – 40° to +125°C	Insertion Mount
MC78XXBD2T			Surface Mount

XX indicates nominal voltage.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX, These two digits of the type number indicate nominal voltage.

* C_{in} is required if regulator is located an appreciable distance from power supply filter.

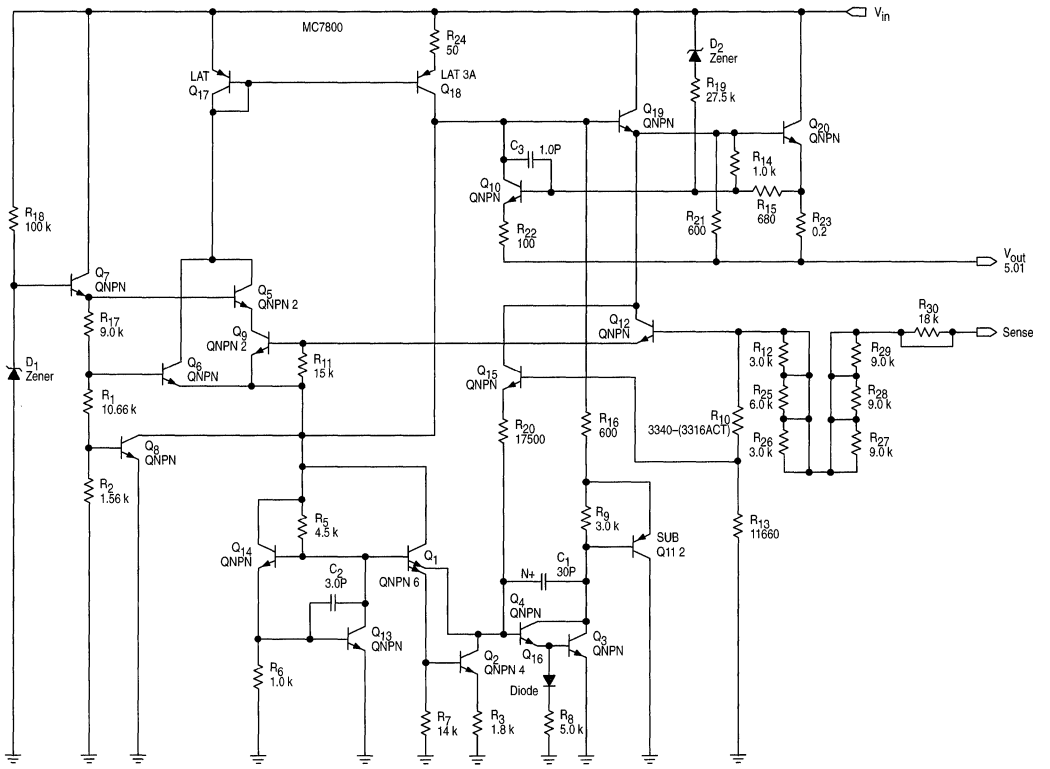
** C_O is not needed for stability; however, it does improve transient response. Values of less than 0.1 µF could cause instability.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 – 18 V) (24 V)	V_I	35 40	Vdc
Power Dissipation Case 221A T_A = 25°C Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case Case 936 (D^2PAK) T_A = 25°C Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case	 P_D $R_{\theta JA}$ $R_{\theta JC}$ P_D $R_{\theta JA}$ $R_{\theta JA}$	 Internally Limited 65 5.0 Internally Limited See Figure 13 5.0	 W °C/W °C/W W °C/W °C/W
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	+150	°C

3

Representative Schematic Diagram



This device contains 22 active transistors.

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7805B			MC7805C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 7.0 Vdc ≤ V_{in} ≤ 20 Vdc 8.0 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	 – 4.75	 – 5.0	 – 5.25	 4.75 –	 5.0 –	 5.25 –	Vdc
Line Regulation, T_J = 25°C (Note 2) 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc	Reg_{line}	 – –	 5.0 1.3	 100 50	 – –	 5.0 1.3	 100 50	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 1.3 0.15	 100 50	 – –	 1.3 0.15	 100 50	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.2	8.0	–	3.2	8.0	mA
Quiescent Current Change 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 – 1.3 0.5	 – – –	 – – –	 1.3 – 0.5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	 –	 68	 –	 –	 68	 –	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	 –	 10	 –	 –	 10	 –	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	 –	 0.2	 –	 –	 0.2	 –	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	−0.3	–	–	−0.3	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7805AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	4.9	5.0	5.1	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 7.5 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	 4.8	 5.0	 5.2	Vdc
Line Regulation (Note 2) 7.5 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.0 Vdc ≤ V_{in} ≤ 12 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, T_J = 25°C 7.3 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = 25°C	Reg_{line}	 – – – –	 5.0 1.3 1.3 4.5	 50 50 25 50	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – –	 1.3 0.8 0.15	 100 100 50	mV
Quiescent Current (T_J = 25°C)	I_B	– –	– 3.2	6.0 6.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 0.8 0.8 0.5	mA

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= −40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7805AC			Unit
		Min	Typ	Max	
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 500 mA	RR	–	68	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	−0.3	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7806B			MC7806C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	5.75	6.0	6.25	5.75	6.0	6.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 8.0 Vdc ≤ V_{in} ≤ 21 Vdc 9.0 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	– 5.7	– 6.0	– 6.3	5.7 –	6.0 –	6.3 –	Vdc
Line Regulation, T_J = 25°C (Note 2) 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 13 Vdc	Reg_{line}	– –	5.5 1.4	120 60	– –	5.5 1.4	120 60	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	– –	1.3 0.2	120 60	– –	1.3 0.2	120 60	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.3	8.0	–	3.3	8.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	– – –	– – –	– 1.3 0.5	– – –	– – –	1.3 – 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz	RR	–	65	–	–	65	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	−0.3	–	–	−0.3	–	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= −40°C for MC78XXB
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7806AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	5.88	6.0	6.12	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 8.6 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	5.76	6.0	6.24	Vdc
Line Regulation (Note 2) 8.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 9.0 Vdc ≤ V_{in} ≤ 13 Vdc 9.0 Vdc ≤ V_{in} ≤ 13 Vdc, T_J = 25°C 8.3 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = 25°C	Reg_{line}	 – – – –	 5.0 1.4 1.4 4.5	 60 60 30 60	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – –	 1.3 0.9 0.2	 100 100 50	mV
Quiescent Current T_J = 25°C	I_B	– –	– 3.3	6.0 6.0	mA
Quiescent Current Change 9.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.6 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 0.8 0.8 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, I_O = 500 mA	RR	 –	 65	 –	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	 –	 10	 –	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	 –	 0.2	 –	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.3	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7808B			MC7808C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	7.7	8.0	8.3	7.7	8.0	8.3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 10.5 Vdc ≤ V_{in} ≤ 23 Vdc 11.5 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	 – 7.6	 – 8.0	 – 8.4	 7.6 –	 8.0 –	 8.4 –	Vdc
Line Regulation, T_J = 25°C, (Note 2) 10.5 Vdc ≤ V_{in} ≤ 25 Vdc 11 Vdc ≤ V_{in} ≤ 17 Vdc	Reg_{line}	 – –	 6.0 1.7	 160 80	 – –	 6.0 1.7	 160 80	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 1.4 .22	 160 80	 – –	 1.4 .22	 160 80	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.3	8.0	–	3.3	8.0	mA

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7808B			MC7808C			Unit
		Min	Typ	Max	Min	Typ	Max	
Quiescent Current Change 10.5 Vdc ≤ V_{in} ≤ 25 Vdc 11.5 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 – 1.0 0.5	 – – –	 – – –	 1.0 – 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	 –	 62	 –	 –	 62	 –	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	 –	 10	 –	 –	 10	 –	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	 –	 0.2	 –	 –	 0.2	 –	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	−0.4	–	–	−0.4	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7808AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	7.84	8.0	8.16	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 10.6 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	 7.7	 8.0	 8.3	Vdc
Line Regulation (Note 2) 10.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 11 Vdc ≤ V_{in} ≤ 17 Vdc 11 Vdc ≤ V_{in} ≤ 17 Vdc, T_J = 25°C 10.4 Vdc ≤ V_{in} ≤ 23 Vdc, T_J = 25°C	Reg_{line}	 – – – –	 6.0 1.7 1.7 5.0	 80 80 40 80	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – –	 1.4 1.0 .22	 100 100 50	mV
Quiescent Current T_J = 25°C	I_B	– –	– 3.3	6.0 6.0	mA
Quiescent Current Change 11 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 10.6 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 0.8 0.8 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	 –	 62	 –	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	 –	 10	 –	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	 –	 0.2	 –	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	−0.4	–	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= −40°C for MC78XXB
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 15 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7809CT Min	MC7809CT Typ	MC7809CT Max	Unit
Output Voltage (T_J = 25°C)	V_O	8.65	9.0	9.35	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 11.5 Vdc ≤ V_{in} ≤ 24 Vdc	V_O	8.55	9.0	9.45	Vdc
Line Regulation, T_J = 25°C (Note 2) 11.5 Vdc ≤ V_{in} ≤ 26 Vdc 11.5 Vdc ≤ V_{in} ≤ 17 Vdc	Reg_{line}	 – –	 6.2 1.8	 50 25	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 1.5 0.3	 50 25	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.4	8.0	mA
Quiescent Current Change 11.5 Vdc ≤ V_{in} ≤ 26 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz	RR	 –	 61	 –	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	 –	 10	 –	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.0	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	 –	 0.2	 –	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.5	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7812B Min	MC7812B Typ	MC7812B Max	MC7812C Min	MC7812C Typ	MC7812C Max	Unit
Output Voltage (T_J = 25°C)	V_O	11.5	12	12.5	11.5	12	12.5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 14.5 Vdc ≤ V_{in} ≤ 27 Vdc 15.5 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	 – 11.4	 – 12	 – 12.6	 11.4 –	 12 –	 12.6 –	Vdc
Line Regulation, T_J = 25°C (Note 2) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc	Reg_{line}	 – –	 7.5 2.2	 240 120	 – –	 7.5 2.2	 240 120	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 1.6 1.0	 240 120	 – –	 1.6 1.0	 240 120	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.4	8.0	–	3.4	8.0	mA
Quiescent Current Change 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 15 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 – 1.0 0.5	 – – –	 – – –	 1.0 – 0.5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz	RR	 –	 60	 –	 –	 60	 –	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	–	2.0	–	Vdc

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7812B			MC7812C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.1	–	–	1.1	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	−0.8	–	–	−0.8	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 10 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7812AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	11.75	12	12.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 14.8 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	11.5	12	12.5	Vdc
Line Regulation (Note 2) 14.8 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 16 Vdc ≤ V_{in} ≤ 22 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc, T_J = 25°C 14.5 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = 25°C	Reg_{line}	 – – – –	 7.5 2.2 2.2 6.0	 120 120 60 120	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – –	 1.6 1.2 1.0	 100 100 50	mV
Quiescent Current T_J = 25°C	I_B	– –	– 3.4	6.0 6.0	mA
Quiescent Current Change 15 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 14.8 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 0.8 0.8 0.5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 500 mA	RR	–	60	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	–	1.1	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	−0.8	–	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= −40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7815B			MC7815C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	14.4	15	15.6	14.4	15	15.6	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 18.5 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	 – 14.25	 – 15	 – 15.75	 14.25 –	 15 –	 15.75 –	Vdc
Line Regulation, T_J = 25°C (Note 2) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc	Reg_{line}	 – –	 8.5 3.0	 300 150	 – –	 8.5 3.0	 300 150	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 1.8 1.2	 300 150	 – –	 1.8 1.2	 300 150	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.5	8.0	–	3.5	8.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 18.5 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 – 1.0 0.5	 – – –	 – – –	 1.0 – 0.5	mA
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz	RR	 –	 58	 –	 –	 58	 –	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	 –	 10	 –	 –	 10	 –	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.2	–	–	1.2	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	 –	 0.2	 –	 –	 0.2	 –	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–1.0	–	–	–1.0	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7815AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	14.7	15	15.3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	 14.4	 15	 15.6	Vdc
Line Regulation (Note 2) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 20 Vdc ≤ V_{in} ≤ 26 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc, T_J = 25°C 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = 25°C	Reg_{line}	 – – – –	 8.5 3.0 3.0 7.0	 150 150 75 150	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – –	 1.8 1.5 1.2	 100 100 50	mV
Quiescent Current T_J = 25°C	I_B	– –	– 3.5	6.0 6.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 0.8 0.8 0.5	mA

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= −40°C for MC78XXB
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7815AC			Unit
		Min	Typ	Max	
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	–	58	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.2	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–1.0	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7818B			MC7818C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	17.3	18	18.7	17.3	18	18.7	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 21 Vdc ≤ V_{in} ≤ 33 Vdc 22 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	– 17.1	– 18	– 18.9	17.1 –	18 –	18.9 –	Vdc
Line Regulation, T_J = 25°C (Note 2) 21 Vdc ≤ V_{in} ≤ 33 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc	Reg_{line}	– –	9.5 3.2	360 180	– –	9.5 3.2	360 180	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	– –	2.0 1.5	360 180	– –	2.0 1.5	360 180	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.5	8.0	–	3.5	8.0	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc 22 Vdc ≤ V_{in} ≤ 33 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	– – –	– – –	– 1.0 0.5	– – –	– – –	1.0 – 0.5	mA
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 33 Vdc, f = 120 Hz	RR	–	57	–	–	57	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_{il} - V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.3	–	–	1.3	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–1.5	–	–	–1.5	–	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 10 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7818AC Min	MC7818AC Typ	MC7818AC Max	Unit
Output Voltage (T_J = 25°C)	V_O	17.64	18	18.36	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 21 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	17.3	18	18.7	Vdc
Line Regulation (Note 2) 21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 24 Vdc ≤ V_{in} ≤ 30 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = 25°C 20.6 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = 25°C	Reg_{line}	 – – – –	 9.5 3.2 3.2 8.0	 180 180 90 180	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – – –	 2.0 1.8 1.5	 100 100 50	mV
Quiescent Current T_J = 25°C	I_B	– –	– 3.5	6.0 6.0	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 21 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – – –	 – – –	 0.8 0.8 0.5	mA
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, I_O = 500 mA	RR	–	57	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	μV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.3	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–1.5	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7824B Min	MC7824B Typ	MC7824B Max	MC7824C Min	MC7824C Typ	MC7824C Max	Unit
Output Voltage (T_J = 25°C)	V_O	23	24	25	23	24	25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 27 Vdc ≤ V_{in} ≤ 38 Vdc 28 Vdc ≤ V_{in} ≤ 38 Vdc	V_O	 – 22.8	 – 24	 – 25.2	 22.8 –	 24 –	 25.2 –	Vdc
Line Regulation, T_J = 25°C (Note 2) 27 Vdc ≤ V_{in} ≤ 38 Vdc 30 Vdc ≤ V_{in} ≤ 36 Vdc	Reg_{line}	 – –	 11.5 3.8	 480 240	 – –	 11.5 3.8	 480 240	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 2.1 1.8	 480 240	 – –	 2.1 1.8	 480 240	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.6	8.0	–	3.6	8.0	mA

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7824B			MC7824C			Unit
		Min	Typ	Max	Min	Typ	Max	
Quiescent Current Change	ΔI_B							mA
27 Vdc ≤ V_{in} ≤ 38 Vdc		–	–	–	–	–	1.0	
28 Vdc ≤ V_{in} ≤ 38 Vdc		–	–	1.0	–	–	–	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	–	–	0.5	
Ripple Rejection	RR							dB
28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz		–	54	–	–	54	–	
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C)	V_n							μV/V_O
10 Hz ≤ f ≤ 100 kHz		–	10	–	–	10	–	
Output Resistance f = 1.0 kHz	r_O	–	1.4	–	–	1.4	–	mΩ
Short Circuit Current Limit (T_A = 25°C)	I_{SC}							A
V_{in} = 35 Vdc		–	0.2	–	–	0.2	–	
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–2.0	–	–	–2.0	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7824AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	23.5	24	24.5	Vdc
Output Voltage	V_O				Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W)		23	24	25	
27.3 Vdc ≤ V_{in} ≤ 38 Vdc					
Line Regulation (Note 2)	Reg_{line}				mV
27 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		–	11.5	240	
30 Vdc ≤ V_{in} ≤ 36 Vdc		–	3.8	240	
30 Vdc ≤ V_{in} ≤ 36 Vdc, T_J = 25°C		–	3.8	120	
26.7 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = 25°C		–	10	240	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		–	2.1	100	
5.0 mA ≤ I_O ≤ 1.0 A		–	2.0	100	
250 mA ≤ I_O ≤ 750 mA		–	1.8	50	
Quiescent Current	I_B	–	–	6.0	mA
T_J = 25°C		–	3.6	6.0	
Quiescent Current Change	ΔI_B				mA
27.3 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		–	–	0.8	
27.3 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = 25°C		–	–	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Ripple Rejection	RR				dB
28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, I_O = 500 mA		–	54	–	
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C)	V_n				μV/V_O
10 Hz ≤ f ≤ 100 kHz		–	10	–	
Output Resistance (f = 1.0 kHz)	r_O	–	1.4	–	mΩ
Short Circuit Current Limit (T_A = 25°C)	I_{SC}				A
V_{in} = 35 Vdc		–	0.2	–	
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–2.0	–	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

3

Figure 1. Peak Output Current as a Function of Input/Output Differential Voltage (MC78XXC, AC, B)

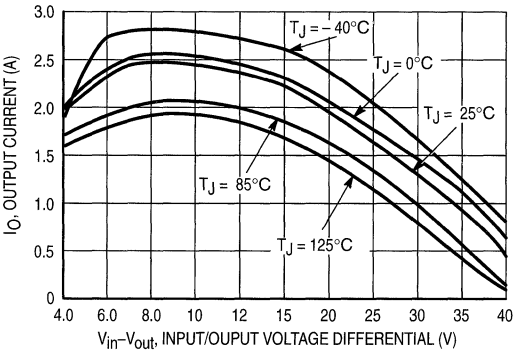


Figure 2. Ripple Rejection as a Function of Output Voltages (MC78XXC, AC)

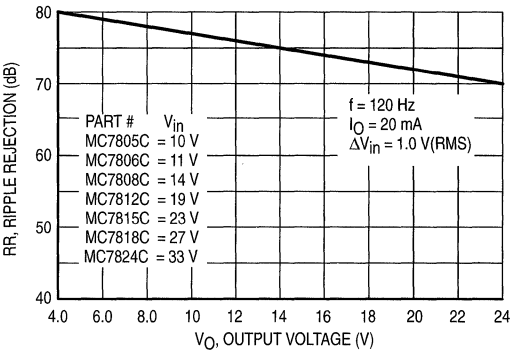


Figure 3. Ripple Rejection as a Function of Frequency (MC78XXC, AC)

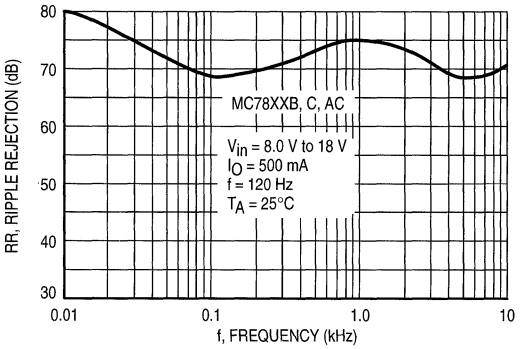


Figure 4. Output Voltage as a Function of Junction Temperature (MC7805C, AC, B)

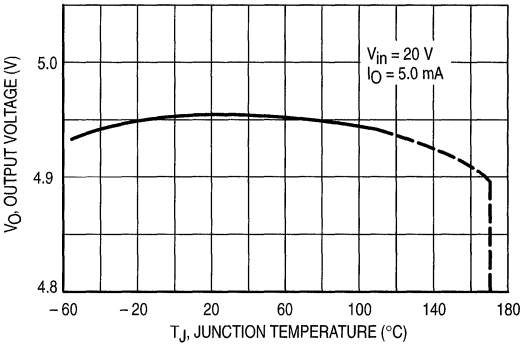


Figure 5. Output Impedance as a Function of Output Voltage (MC78XXC, AC)

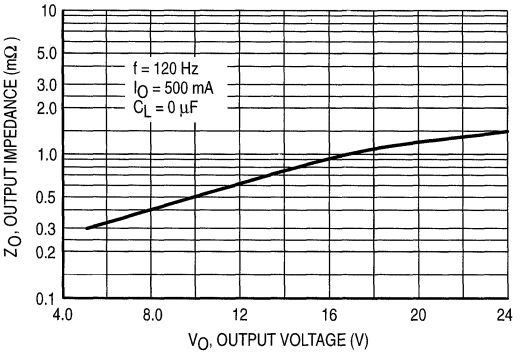
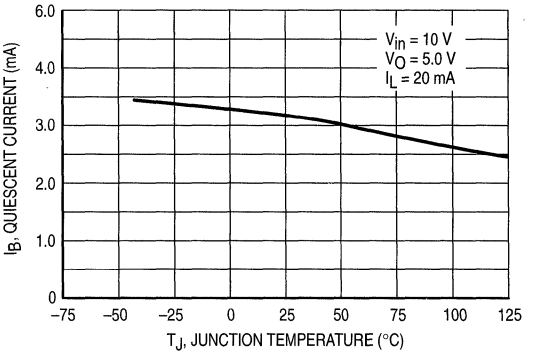


Figure 6. Quiescent Current as a Function of Temperature (MC78XXC, AC, B)



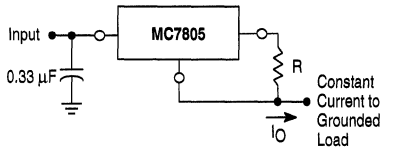
APPLICATIONS INFORMATION

Design Considerations

The MC7800 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 7. Current Regulator



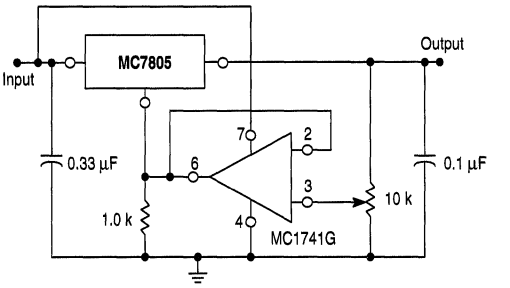
The MC7800 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

$I_B \cong 3.2$ mA over line and load changes.

For example, a 1.0 A current source would require R to be a 5.0 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 V.

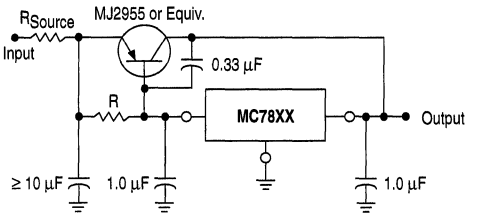
Figure 8. Adjustable Output Regulator



$V_O = 7.0\ V$ to $20\ V$
$V_{IN} = V_O \geq 2.0\ V$

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 V greater than the regulator voltage.

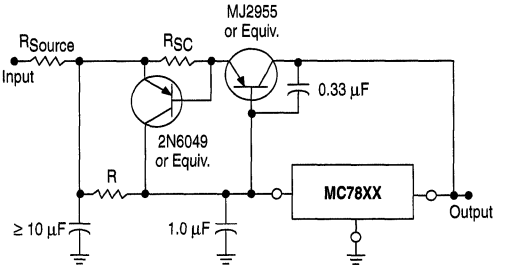
Figure 9. Current Boost Regulator



XX = 2 digits of type number indicating voltage.

The MC7800 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 A. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input/output differential voltage minimum is increased by V_{BE} of the pass transistor.

Figure 10. Short Circuit Protection



XX = 2 digits of type number indicating voltage.

The circuit of Figure 9 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three–terminal regulator. Therefore, a four–ampere plastic power transistor is specified.

Figure 11. Worst Case Power Dissipation versus Ambient Temperature (Case 221A)

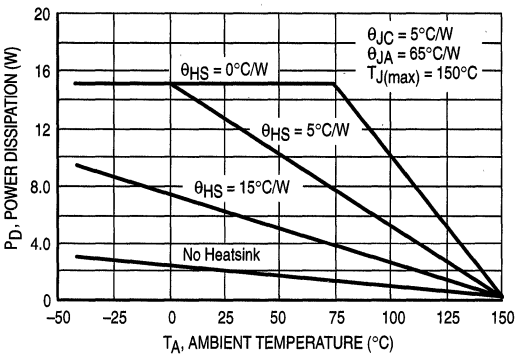


Figure 12. Input Output Differential as a Function of Junction Temperature (MC78XXC, AC, B)

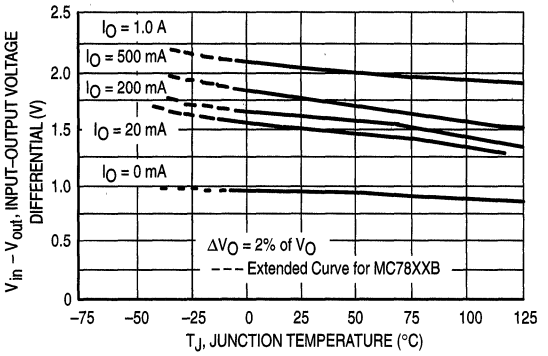
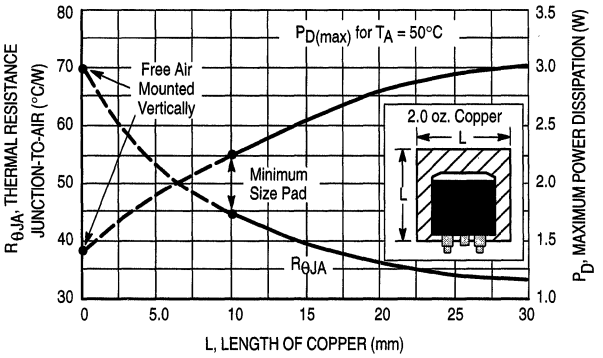


Figure 13. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MOTOROLA

MC78L00, A Series

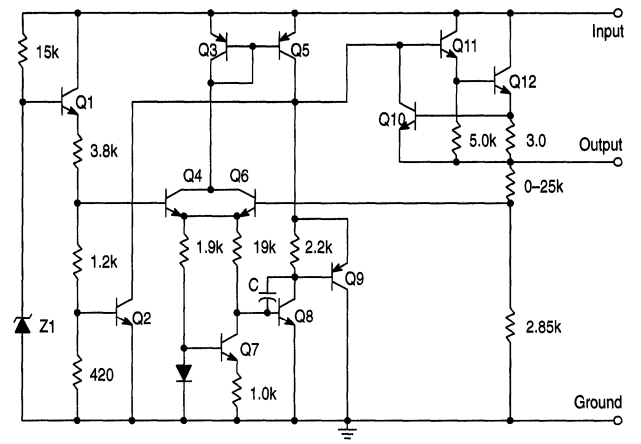
Three-Terminal Low Current Positive Voltage Regulators

The MC78L00, A Series of positive voltage regulators are inexpensive, easy–to–use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode–resistor combination, as output impedance and quiescent current are substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in either ±5% (AC) or ±10% (C) Selections

Representative Schematic Diagram

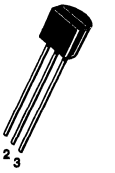


ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC78LXXACD*	T_J = 0° to +125°C	SOP–8
MC78LXXACP		Plastic Power
MC78LXXCP		Plastic Power
MC78LXXABD*	T_J = –40° to +125°C	SOP–8
MC78LXXABP*		Plastic Power

XX indicates nominal voltage
*Available in 5, 8, 9, 12 and 15 V devices.

P SUFFIX
CASE 29



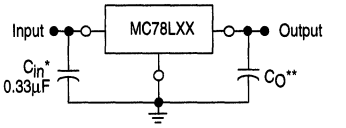
Pin 1. Output
2. GND
3. Input

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)*

Pin 1. V_{out}
2. GND
3. GND
4. NC
5. NC
6. GND
7. GND
8. V_{in}

* SOP–8 is an internally modified SO–8 package. Pins 2, 3, 6, and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP–8 conforms to all external dimensions of the standard SO–8 package.

Standard Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

*C_{in} is required if regulator is located an appreciable distance from power supply filter.
**C_O is not needed for stability; however, it does improve transient response.

DEVICE TYPE/NOMINAL VOLTAGE

10%	5%	Voltage
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L09C	MC78L09AC	9.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

MAXIMUM RATINGS (T_A = +125°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V–8.0 V) (12 V–18 V) (24 V)	V_I	30 35 40	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

3

ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L05AC, AB			MC78L05C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	4.6	5.0	5.4	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 7.0 Vdc ≤ V_I ≤ 20 Vdc 8.0 Vdc ≤ V_I ≤ 20 Vdc	Reg_{line}	 – –	 55 45	 150 100	 – –	 55 45	 200 150	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 11 5.0	 60 30	 – –	 11 5.0	 60 30	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 10 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 4.75 4.75	 – –	 5.25 5.25	 4.5 4.5	 – –	 5.5 5.5	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.8 –	 6.0 5.5	 – –	 3.8 –	 6.0 5.5	mA
Input Bias Current Change (8.0 Vdc ≤ V_I ≤ 20 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	 – –	 – –	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	–	40	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 8.0 Vdc ≤ V_I ≤ 18 V, T_J = +25°C)	RR	41	49	–	40	49	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L08AC, AB			MC78L08C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	7.36	8.0	8.64	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 10.5 Vdc ≤ V_I ≤ 23 Vdc 11 Vdc ≤ V_I ≤ 23 Vdc	Reg_{line}	 – –	 20 12	 175 125	 – –	 20 12	 200 150	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 15 8.0	 80 40	 – –	 15 6.0	 80 40	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 23 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 14 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 7.6 7.6	 – –	 8.4 8.4	 7.2 7.2	 – –	 8.8 8.8	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.0 –	 6.0 5.5	 – –	 3.0 –	 6.0 5.5	mA
Input Bias Current Change (11 Vdc ≤ V_I ≤ 23 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	 – –	 – –	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	60	–	–	52	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 12 V ≤ V_I ≤ 23 V, T_J = +25°C)	RR	37	57	–	36	55	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 15 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, −40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L09AC, AB			MC78L09C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	8.6	9.0	9.4	8.3	9.0	9.7	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 11.5 Vdc ≤ V_I ≤ 24 Vdc 12 Vdc ≤ V_I ≤ 24 Vdc	Reg_{line}	 – –	 20 12	 175 125	 – –	 20 12	 200 150	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 15 8.0	 90 40	 – –	 15 6.0	 90 40	mV
Output Voltage (11.5 Vdc ≤ V_I ≤ 24 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 15 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 8.5 8.5	 – –	 9.5 9.5	 8.1 8.1	 – –	 9.9 9.9	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.0 –	 6.0 5.5	 – –	 3.0 –	 6.0 5.5	mA
Input Bias Current Change (11 Vdc ≤ V_I ≤ 23 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	 – –	 – –	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	60	–	–	52	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 13 V ≤ V_I ≤ 24 V, T_J = +25°C)	RR	37	57	–	36	55	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, −40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L12AC, AB			MC78L12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	11.1	12	12.9	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 14.5 Vdc ≤ V_I ≤ 27 Vdc 16 Vdc ≤ V_I ≤ 27 Vdc	Reg_{line}	 – –	 120 100	 250 200	 – –	 120 100	 250 200	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 20 10	 100 50	 – –	 20 10	 100 50	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 19 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 11.4 11.4	 – –	 12.6 12.6	 10.8 10.8	 – –	 13.2 13.2	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 4.2 –	 6.5 6.0	 – –	 4.2 –	 6.5 6.0	mA
Input Bias Current Change (16 Vdc ≤ V_I ≤ 27 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	 – –	 – –	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	80	–	–	80	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = +25°C)	RR	37	42	–	36	42	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, −40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L15AC, AB			MC78L15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	13.8	15	16.2	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 17.5 Vdc ≤ V_I ≤ 30 Vdc 20 Vdc ≤ V_I ≤ 30 Vdc	Reg_{line}	 – –	 130 110	 300 250	 – –	 130 110	 300 250	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 25 12	 150 75	 – –	 25 12	 150 75	mV
Output Voltage (17.5 Vdc ≤ V_I ≤ 30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 23 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 14.25 14.25	 – –	 15.75 15.75	 13.5 13.5	 – –	 16.5 16.5	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 4.4 –	 6.5 6.0	 – –	 4.4 –	 6.5 6.0	mA
Input Bias Current Change (20 Vdc ≤ V_I ≤ 30 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	 – –	 – –	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	–	90	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = +25°C)	RR	34	39	–	33	39	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L18AC			MC78L18C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	16.6	18	19.4	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 21.4 Vdc ≤ V_I ≤ 33 Vdc 20.7 Vdc ≤ V_I ≤ 33 Vdc 22 Vdc ≤ V_I ≤ 33 Vdc 21 Vdc ≤ V_I ≤ 33 Vdc	Reg_{line}	 – –	 45 35	 325 275	 – –	 32 27	 325 275	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 30 15	 170 85	 – –	 30 15	 170 85	mV
Output Voltage (21.4 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (20.7 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA) (V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 17.1 17.1	 – –	 18.9 18.9	 16.2 16.2 	 – –	 19.8 19.8	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.1 –	 6.5 6.0	 – –	 3.1 –	 6.5 6.0	mA
Input Bias Current Change (22 Vdc ≤ V_I ≤ 33 Vdc) (21 Vdc ≤ V_I ≤ 33 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	 – –	 – –	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	150	–	–	150	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 23 V ≤ V_I ≤ 33 V, T_J = +25°C)	RR	33	48	–	32	46	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L24AC			MC78L24C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23	24	25	22.1	24	25.9	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
27.5 Vdc ≤ V_I ≤ 38 Vdc		–	–	–	–	35	350	
28 Vdc ≤ V_I ≤ 80 Vdc		–	50	300	–	30	300	
27 Vdc ≤ V_I ≤ 38 Vdc		–	60	350	–	–	–	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	40	200	–	40	200	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	20	100	–	20	100	
Output Voltage	V_O							Vdc
(28 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					21.6	–	26.4	
(27 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		22.8	–	25.2				
(28 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA)					21.6	–	26.4	
(27 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA)		22.8	–	25.2				
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.1	6.5	–	3.1	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(28 Vdc ≤ V_I ≤ 38 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.1	–	–	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	200	–	–	200	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 29 V ≤ V_I ≤ 35 V, T_J = +25°C)	RR	31	45	–	30	43	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

3

Figure 1. Dropout Characteristics

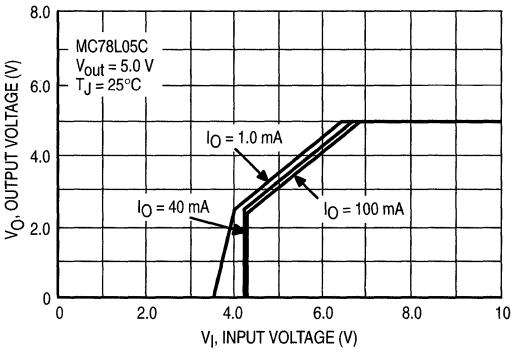


Figure 2. Dropout Voltage versus Junction Temperature

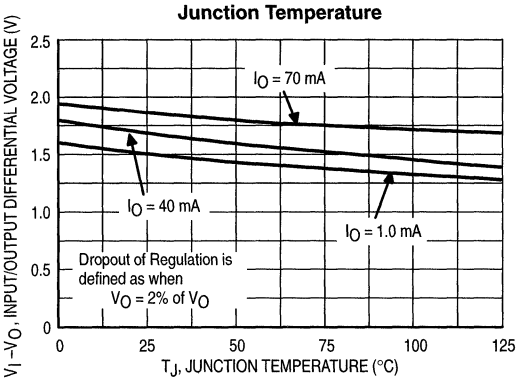


Figure 3. Input Bias Current versus Ambient Temperature

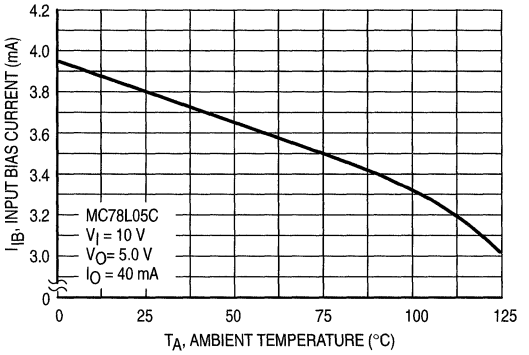


Figure 4. Input Bias Current versus Input Voltage

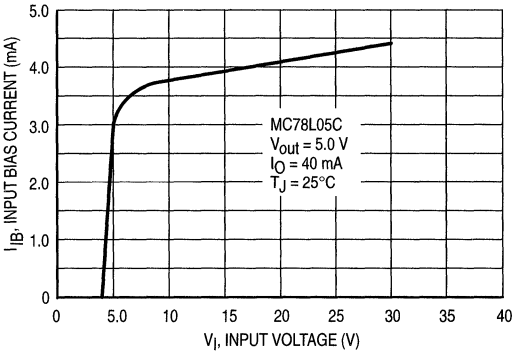


Figure 5. Maximum Average Power Dissipation versus Ambient Temperature – TO–92 Type Package

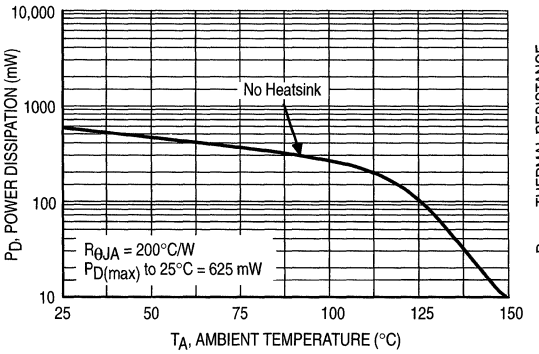
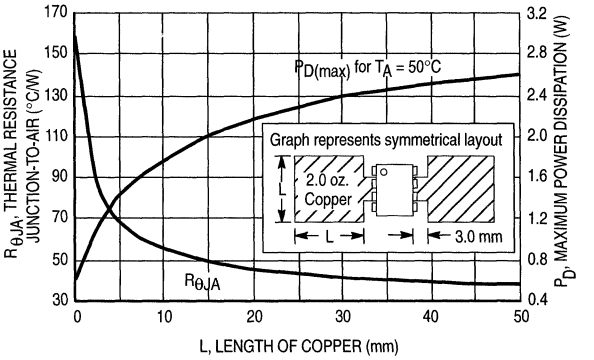


Figure 6. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



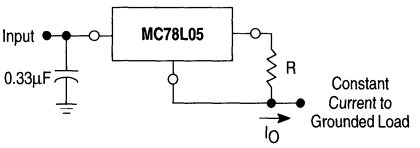
APPLICATIONS INFORMATION

Design Considerations

The MC78L00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short Circuit Protection limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. The input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen.The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Figure 7. Current Regulator



The MC78L00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

I_B = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50 Ω, 1/2 W resistor and the output voltage compliance would be the input voltage less 7 V.

Figure 8. ± 15 V Tracking Voltage Regulator

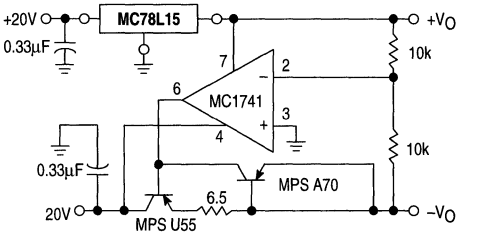
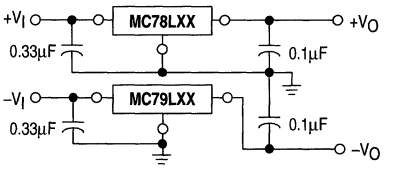


Figure 9. Positive and Negative Regulator



MOTOROLA

MC78M00 Series

3

Three-Terminal Medium Current Positive Voltage Regulators

The MC78M00 Series positive voltage regulators are identical to the popular MC7800 Series devices, except that they are specified for only half the output current. Like the MC7800 devices, the MC78M00 three–terminal regulators are intended for local, on–card voltage regulation.

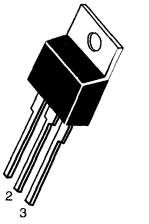
Internal current limiting, thermal shutdown circuitry and safe–area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation

THREE–TERMINAL MEDIUM CURRENT POSITIVE FIXED VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA

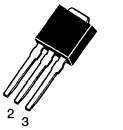
T SUFFIX
PLASTIC PACKAGE
CASE 221A
(TO–220)



Heatsink surface connected to Pin 2.

Pin 1. Input
2. Ground
3. Output

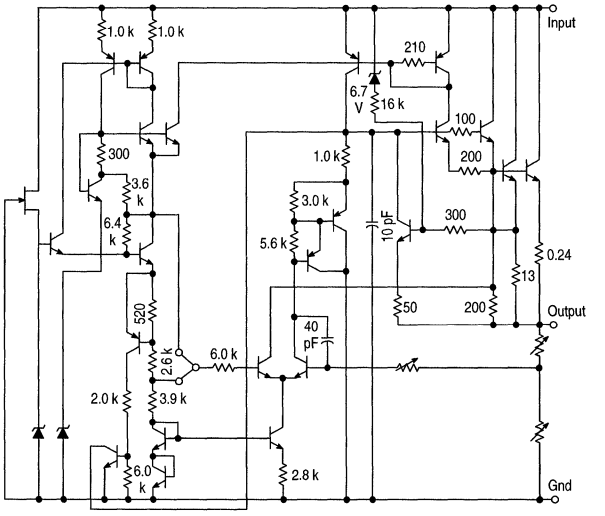
DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)



DT–1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

Representative Schematic Diagram



This device contains 28 active transistors.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC78M05B,C	5.0 V	MC78M09B,C	9.0 V	MC78M18B,C	18 V
MC78M06B,C	6.0 V	MC78M12B,C	12 V	MC78M20B,C	20 V
MC78M08B,C	8.0 V	MC78M15B,C	15 V	MC78M24B,C	24 V

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC78MXXCDT* MC78MXXCDT–1*	T_J = 0° to +125°C	DPAK
MC78MXXCT	T_J = – 40° to +125°C	TO–220
MC78MXXBT#		
MC78MXXBDT#		DPAK

XX Indicates nominal voltage.

* Available in 5, 8, 12 and 15 V devices.

\# Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V–18 V) (20 V–24V)	V_I	35 40	Vdc
Power Dissipation (Package Limitation) Plastic Package, T Suffix T_A = 25°C Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case Plastic Package, DT Suffix T_A = 25°C Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case	 P_D θ_{JA} θ_{JC} P_D θ_{JA} θ_{JC}	 Internally Limited 70 5.0 Internally Limited 92 5.0	 °C/W °C/W °C/W °C/W
Operating Junction Temperature Range	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

MC78M05B,C ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	4.8	5.0	5.2	Vdc
Line Regulation (T_J = 25°C, 7.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	–	3.0	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 20 10	 100 50	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (7.0 Vdc ≤ V_I ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	4.75	–	5.25	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.0	mA
Quiescent Current Change (8.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	μV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V) (I_O = 300 mA, f = 120 Hz, 8.0 ≤ V_I ≤ 18 V, T_J = 25°C)	RR	 62 62	 – 80	 – –	dB
Dropout Voltage (T_J = 25°C)	V_I–V_O	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.2	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M06B,C ELECTRICAL CHARACTERISTICS (V_I = 11 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	5.75	6.0	6.25	Vdc
Line Regulation (T_J = 25°C, 8.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	–	5.0	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 20 10	 120 60	mV
Output Voltage (8.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (8.0 Vdc ≤ V_I ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	5.7	–	6.3	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.0	mA
Quiescent Current Change (9.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	45	–	μV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V) (I_O = 300 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V, T_J = 25°C)	RR	 59 59	 – 80	 – –	dB
Dropout Voltage (T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.2	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M08B,C ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	7.7	8.0	8.3	Vdc
Line Regulation (T_J = 25°C, 10.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	–	6.0	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 160 80	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (10.5 Vdc ≤ V_I ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	7.6	–	8.4	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.0	mA
Quiescent Current Change (10.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	52	–	μV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 11.5 V ≤V_I ≤ 21.5 V) (I_O = 300 mA, f = 120 Hz, 11.5 V ≤V_I ≤ 21.5 V, T_J = 25°C)	RR	 56 56	 – 80	 – –	dB
Dropout Voltage (T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.2	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M09B,C ELECTRICAL CHARACTERISTICS (V_I = 15 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \le$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	8.64	9.0	9.45	Vdc
Line Regulation (T_J = 25°C, 11.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	–	6.0	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 180 90	mV
Output Voltage (11.5 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (11.5 Vdc ≤ V_I ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	8.55	–	9.45	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.0	mA
Quiescent Current Change (11.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	52	–	μV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 12.5 V ≤V_I ≤ 22.5 V) (I_O = 300 mA, f = 120 Hz, 12.5 V ≤V_I ≤ 22.5 V, T_J = 25°C)	RR	 56 56	 – 80	 – –	dB
Dropout Voltage (T_J = 25°C)	V_I–V_O	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.2	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M12B,C ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \le$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	11.5	12	12.5	Vdc
Line Regulation (T_J = 25°C, 14.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA)	Reg_{line}	–	8.0	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 240 120	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	11.4	–	12.6	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	75	–	μV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 15 V ≤V_I ≤ 25 V) (I_O = 300 mA, f = 120 Hz, 15 V ≤V_I ≤ 25 V, T_J = 25°C)	RR	 55 55	 – 80	 – –	dB
Dropout Voltage (T_J = 25°C)	V_I–V_O	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.3	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M15B,C ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation (T_J = 25°C, 17.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA)	Reg_{line}	–	10	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 300 150	mV
Output Voltage (17.5 Vdc ≤ V_I ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	14.25	–	15.75	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.0	mA
Quiescent Current Change (17.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	μV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V) (I_O = 300 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = 25°C)	RR	 54 54	 – 70	 – –	dB
Dropout Voltage (T_J = 25°C)	V_I–V_O	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.3	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M18B,C ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	17.3	18	18.7	Vdc
Line Regulation (T_J = 25°C, 21 Vdc ≤ V_I ≤ 33 Vdc, I_O = 200 mA)	Reg_{line}	–	10	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 30 10	 360 180	mV
Output Voltage (21 Vdc ≤ V_I ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	17.1	–	18.9	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.5	mA
Quiescent Current Change (21 Vdc ≤ V_I ≤ 33 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	100	–	μV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V) (I_O = 300 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V, T_J = 25°C)	RR	 53 53	 – 70	 – –	dB
Dropout Voltage (T_J = 25°C)	V_I–V_O	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.3	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M20B,C ELECTRICAL CHARACTERISTICS (V_I = 29 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \le$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	19.2	20	20.8	Vdc
Line Regulation (T_J = 25°C, 23 Vdc ≤ V_I ≤ 35 Vdc, I_O = 200 mA)	Reg_{line}	–	10	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 30 10	 400 200	mV
Output Voltage (23 Vdc ≤ V_I ≤ 35 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	19	–	21	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.5	mA
Quiescent Current Change (23 Vdc ≤ V_I ≤ 35 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	110	–	μV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V) (I_O = 300 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V, T_J = 25°C)	RR	 52 52	 – 70	 – –	dB
Dropout Voltage (T_J = 25°C)	V_I–V_O	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.5	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M24B,C ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \le$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	23	24	25	Vdc
Line Regulation (T_J = 25°C, 27 Vdc ≤ V_I ≤ 38 Vdc, I_O = 200 mA)	Reg_{line}	–	10	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 30 10	 480 240	mV
Output Voltage (27 Vdc ≤ V_I ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	22.8	–	25.2	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	7.0	mA
Quiescent Current Change (27 Vdc ≤ V_I ≤ 38 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	170	–	μV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V) (I_O = 300 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V, T_J = 25°C)	RR	 50 50	 – 70	 – –	dB
Dropout Voltage (T_J = 25°C)	V_I–V_O	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.5	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

Figure 1. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

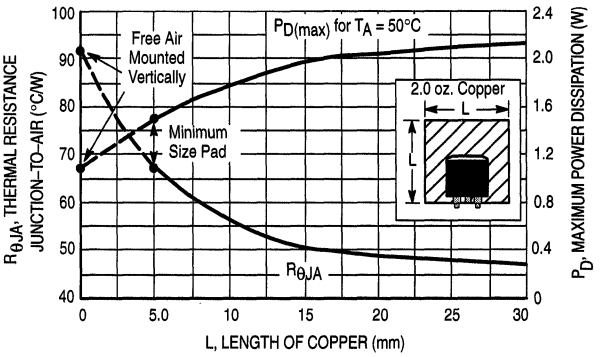


Figure 2. Worst Case Power Dissipation versus Ambient Temperature (TO–220)

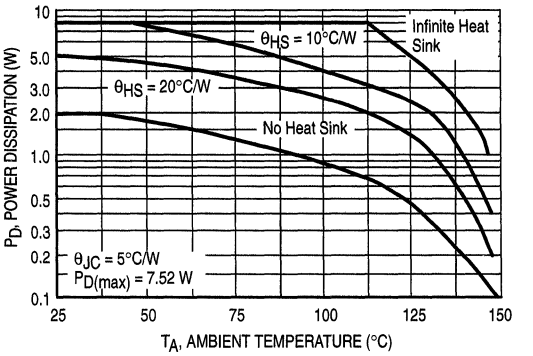


Figure 3. Peak Output Current versus Dropout Voltage

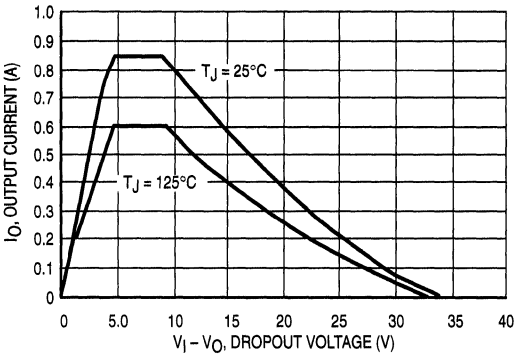


Figure 4. Dropout Voltage versus Junction Temperature

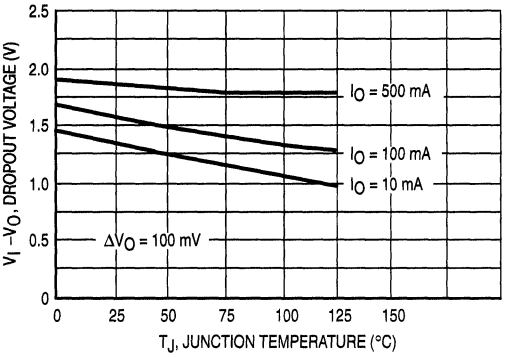


Figure 5. Ripple Rejection versus Frequency

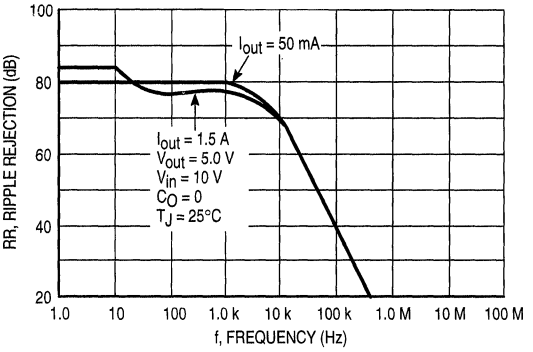


Figure 6. Ripple Rejection versus Output Current

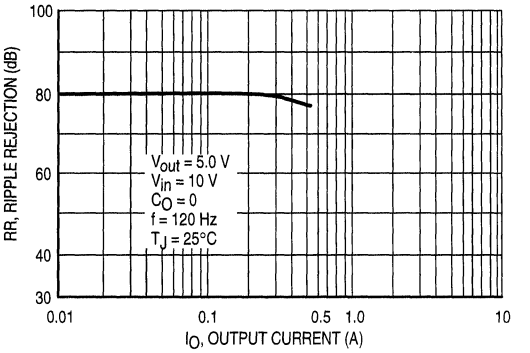


Figure 7. Bias Current versus Input Voltage

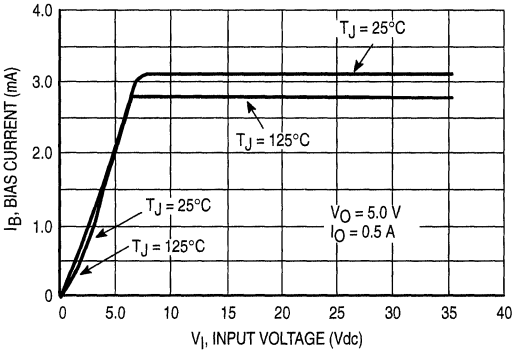
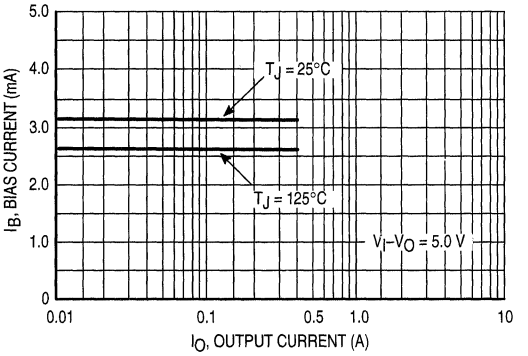


Figure 8. Bias Current versus Output Current



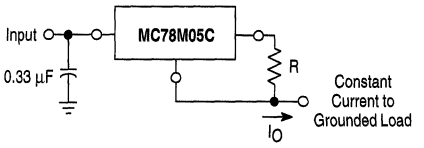
APPLICATIONS INFORMATION

Design Considerations

The MC78M00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 9. Current Regulator



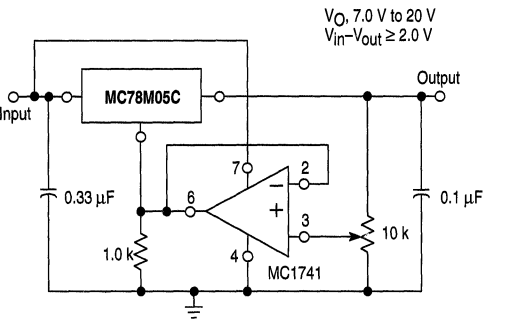
The MC78M00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78M05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_{IB}$$

I_{IB} = 1.5 mA over line and load changes.

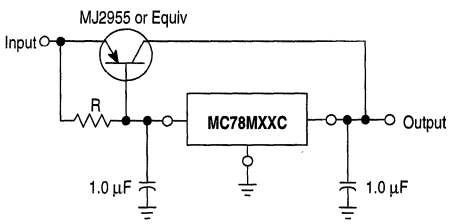
For example, a 500 mA current source would require R to be a 5.0 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7 V.

Figure 10. Adjustable Output Regulator



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 V greater than the regulator voltage.

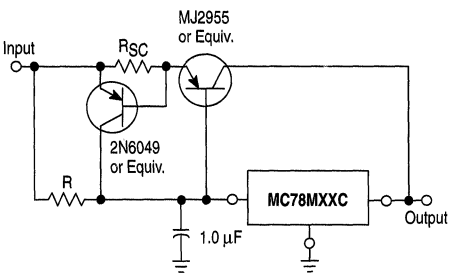
Figure 11. Current Boost Regulator



XX = 2 digits of type number indicating voltage.

The MC78M00 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 A. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input–output differential voltage minimum is increased by V_{BE} of the pass transistor.

Figure 12. Current Boost with Short Circuit Protection



XX = 2 digits of type number indicating voltage.

The circuit of Figure 10 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three–terminal regulator .Therefore, a 4 A plastic power transistor is specified.

MC78T00 Series

Three-Ampere Positive Voltage Regulators

THREE–AMPERE POSITIVE FIXED VOLTAGE REGULATORS

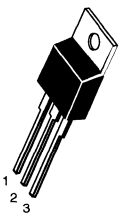
SEMICONDUCTOR TECHNICAL DATA

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 3.0 A. These three–terminal regulators employ internal current limiting, thermal shutdown, and safe–area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on AC–suffix 5.0, 12 and 15 V device types.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series–pass transistor to supply up to 15 A at the nominal output voltage.

- Output Current in Excess of 3.0 A
- Power Dissipation: 25 W
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Thermal Regulation is Specified
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation

T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Input
2. Ground
3. Output

Heatsink surface is connected to Pin 2.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

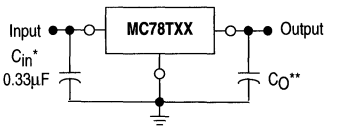
Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 12 V) (15 V)	V_I	35 40	Vdc
Power Dissipation and Thermal Characteristics Plastic Package (Note 1) T_A = +25°C Thermal Resistance, Junction–to–Air T_C = +25°C Thermal Resistance, Junction–to–Case	 P_D $R_{\theta JA}$ P_D $R_{\theta JC}$	 Internally Limited 65 Internally Limited 2.5	 °C/W °C/W
Storage Junction Temperature	T_{stg}	+150	°C
Operating Junction Temperature Range (MC78T00C, AC)	T_J	0 to +125	°C

NOTES: 1. Although power dissipation is internally limited, specifications apply only for $P_O \le P_{max}$, P_{max} = 25 W.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC78T05	5.0 V	MC78T12	12 V
MC78T08	8.0 V	MC78T15	15 V

Simplified Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.2 V above the output voltage even during the low point on the input ripple voltage.

XX these two digits of the type number indicate voltage.

* C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)

** C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Device	V_O Tol.	Operating Temperature Range	Package
MC78TXXCT MC78TXXACT	4% 2%*	T_J = 0° to +125°C	Plastic Power
MC78TXXBT# MC78TXXABT#	4% 2%*	T_J = –40° to +125°C	Plastic Power

XX Indicates nominal voltage.

* 2% regulators available in 5, 12 and 15 V devices.

\# Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC78T05AC			MC78T05C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 7.3 Vdc ≤ V_{in} ≤ 20 Vdc)	V_O	 4.9 4.8	 5.0 5.0	 5.1 5.2	 4.8 4.75	 5.0 5.0	 5.2 5.25	Vdc
Line Regulation (Note 2) (7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, I_O = 3.0 A, T_J = +25°C; 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A)	Reg_{line}	–	3.0	25	–	3.0	25	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 – –	 10 15	 30 80	 – –	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	–	0.001	0.01	–	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 – –	 3.5 4.0	 5.0 6.0	 – –	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A)	ΔI_B	–	0.3	1.0	–	0.3	1.0	mA
Ripple Rejection (8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	62	75	–	62	75	–	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	–	2.2	2.5	–	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	–	10	–	–	10	–	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	2.0	–	–	20	–	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	–	1.5	–	–	1.5	–	A
Peak Output Current (T_J = +25°C)	I_{max}	–	5.0	–	–	5.0	–	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	–	0.2	–	–	0.2	–	mV/°C

NOTES: 1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}, P_{max} = 25 W.
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 13 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, $P_O \le P_{max}$ [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC78T08C			Unit
		Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 10.4 Vdc ≤ V_{in} ≤ 23 Vdc)	V_O	 7.7 7.6	 8.0 8.0	 8.3 8.4	Vdc
Line Regulation (Note 2) (10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C 10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C 11 Vdc ≤ V_{in} ≤ 17 Vdc, I_O = 3.0 A, T_J = +25°C 10.7 Vdc ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A)	Reg_{line}	–	4.0	35	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 – –	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	–	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 – –	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 10.7 Vdc ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A)	ΔI_B	–	0.3	1.0	mA
Ripple Rejection (11 Vdc ≤ V_{in} ≤ 21 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	60	71	–	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	–	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	–	10	–	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	2.0	–	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	–	1.5	–	A
Peak Output Current (T_J = +25°C)	I_{max}	–	5.0	–	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	–	0.3	–	mV/°C

NOTES: 1. Although power dissipation is internally limited, specifications apply only for $P_O \le P_{max}$, P_{max} = 25 W.
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 17 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC78T12AC			MC78T12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A, 5.0 mA ≤ I_O ≤ 2.0 A, 14.5 Vdc ≤ V_{in} ≤ 27 Vdc)	V_O	 11.75 11.5	 12 12	 12.25 12.5	 11.5 11.4	 12 12	 12.5 12.6	Vdc
Line Regulation (Note 2) (14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 16 Vdc ≤ V_{in} ≤ 22 Vdc, I_O = 3.0 A, T_J = +25°C; 14.9 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A)	Reg_{line}	–	6.0	45	–	6.0	45	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 – –	 10 15	 30 80	 – –	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	–	0.001	0.01	–	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 – –	 3.5 4.0	 5.0 6.0	 – –	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 14.9 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A)	ΔI_B	–	0.3	1.0	–	0.3	1.0	mA
Ripple Rejection (15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	57	67	–	57	67	–	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	$V_{in} - V_O$	–	2.2	2.5	–	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	–	10	–	–	10	–	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	2.0	–	–	20	–	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	–	1.5	–	–	1.5	–	A
Peak Output Current (T_J = +25°C)	I_{max}	–	5.0	–	–	5.0	–	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	–	0.5	–	–	0.5	–	mV/°C

NOTES: 1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}, P_{max} = 25 W.
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 20 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC78T15AC			MC78T15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 17.5 Vdc ≤ V_{in} ≤ 30 Vdc)	V_O	 14.7 14.4	 15 15	 15.3 15.6	 14.4 14.25	 15 15	 15.6 15.75	Vdc
Line Regulation (Note 2) (17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 1.0 A, T_J = +25°C; 20 Vdc ≤ V_{in} ≤ 26 Vdc, I_O = 3.0 A, T_J = +25°C; 18 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A)	Reg_{line}	–	7.5	55	–	7.5	55	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 – –	 10 15	 30 80	 – –	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	–	0.001	0.01	–	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 – –	 3.5 4.0	 5.0 6.0	 – –	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 18 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A)	ΔI_B	–	0.3	1.0	–	0.3	1.0	mA
Ripple Rejection (18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	55	65	–	55	65	–	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	–	2.2	2.5	–	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	–	10	–	–	10	–	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	2.0	–	–	20	–	mΩ
Short Circuit Current Limit (V_{in} = 40 Vdc, T_J = +25°C)	I_{SC}	–	1.0	–	–	1.0	–	A
Peak Output Current (T_J = +25°C)	I_{max}	–	5.0	–	–	5.0	–	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	–	0.6	–	–	0.6	–	mV/°C

NOTES: 1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}. P_{max} = 25 W.
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical MC78T05AC to a 20 W input pulse. The variation of the output voltage due to line regulation is labeled and the thermal regulation component is labeled . Figure 2 shows the load and thermal regulation response of a typical MC78T05AC to a 20 W load pulse. The output voltage variation due to load regulation is labeled and the thermal regulation component is labeled .

Figure 1. MC78T05AC Line and Thermal Regulation

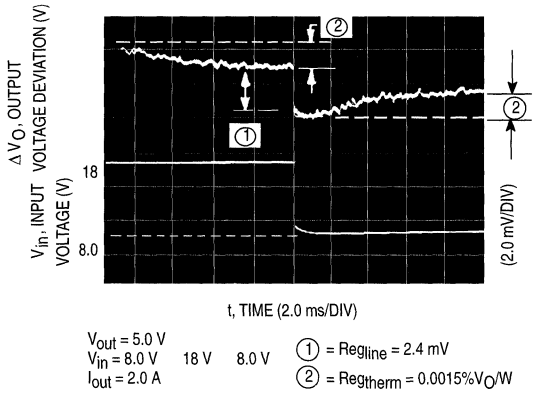
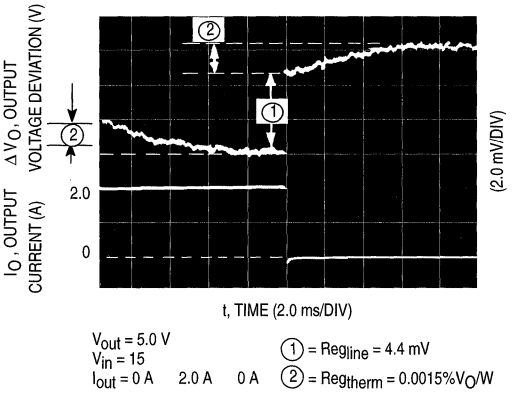


Figure 2. MC78T05AC Load and Thermal Regulation



Representative Schematic Diagram

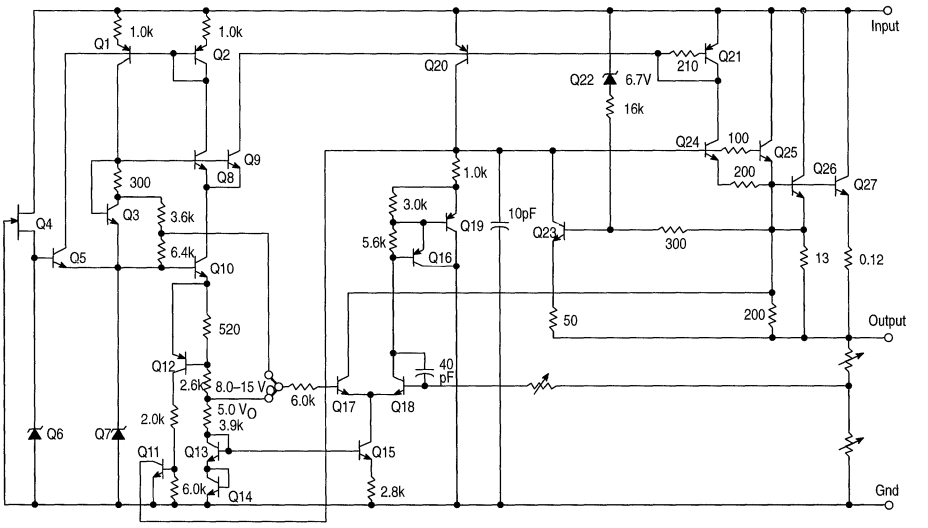


Figure 3. Temperature Stability

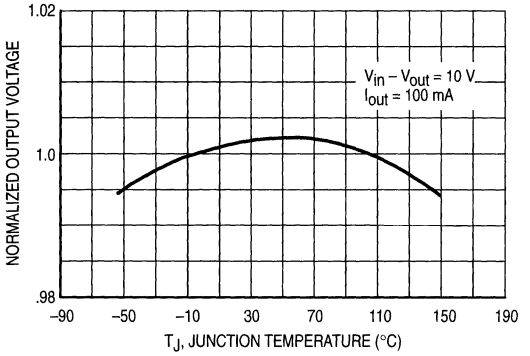


Figure 4. Output Impedance

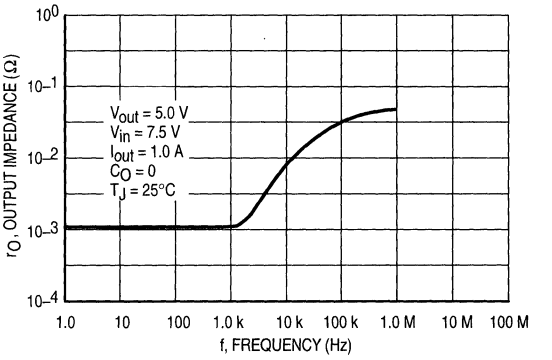


Figure 5. Ripple Rejection versus Frequency

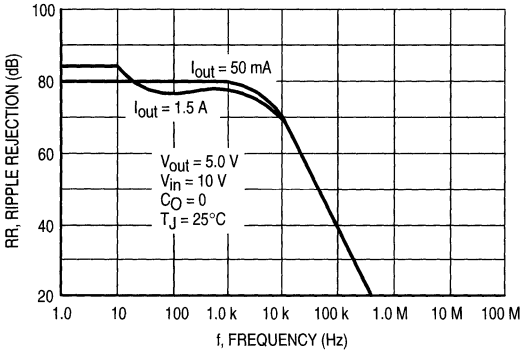


Figure 6. Ripple Rejection versus Output Current

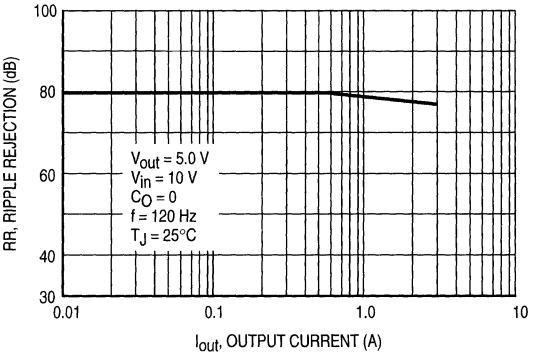


Figure 7. Quiescent Current versus Input Voltage

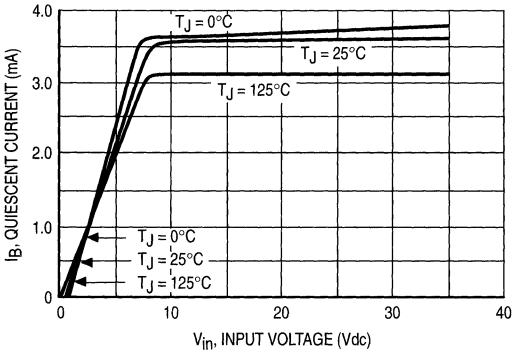
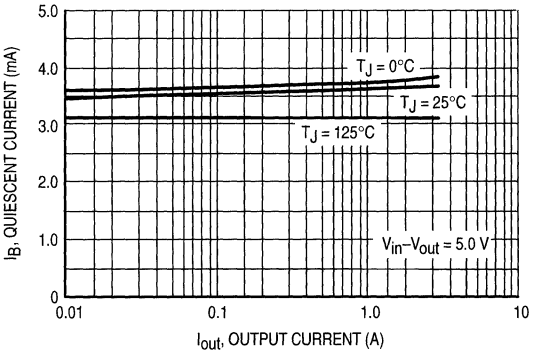


Figure 8. Quiescent Current versus Output Current



3

Figure 9. Dropout Voltage

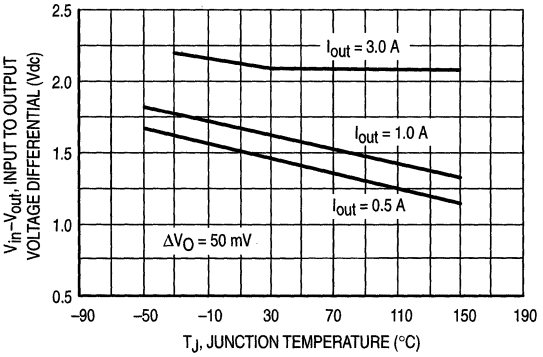


Figure 10. Peak Output Current

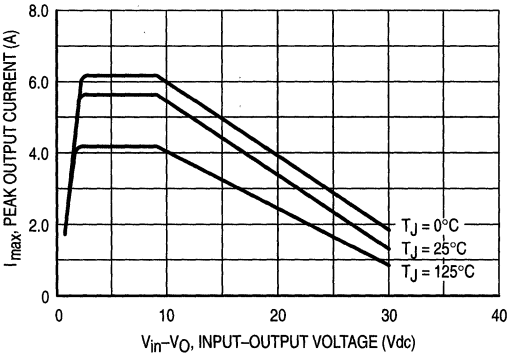


Figure 11. Line Transient Response

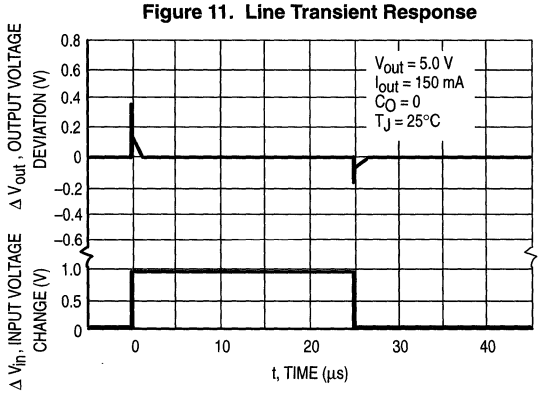


Figure 12. Load Transient Response

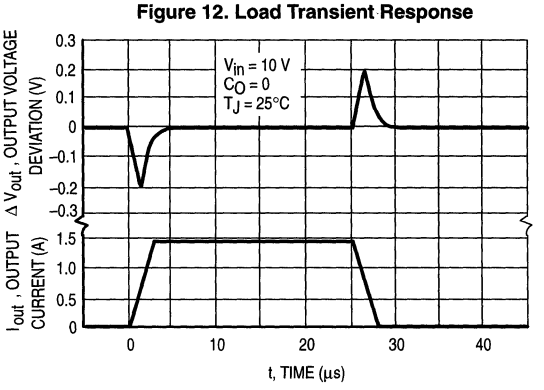
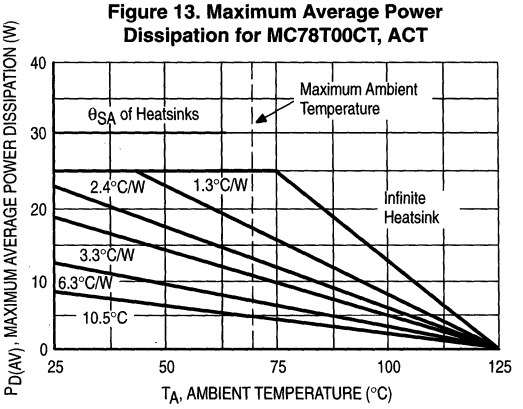


Figure 13. Maximum Average Power Dissipation for MC78T00CT, ACT



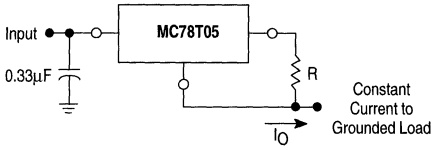
APPLICATIONS INFORMATION

Design Considerations

The MC78T00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 14. Current Regulator



The MC78T05 regulator can also be used as a current source when connected as above. In order to minimize dissipation the MC78T05 is chosen in this application. Resistor R determines the current as follows:

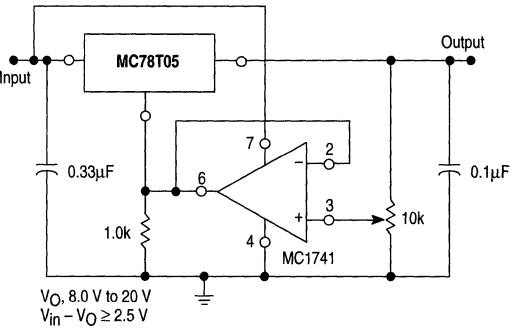
$$I_O = \frac{5.0\ V}{R} + I_B$$

$\Delta I_B \cong 0.7$ mA over line, load and Temperature changes

$I_B \cong 3.5$ mA

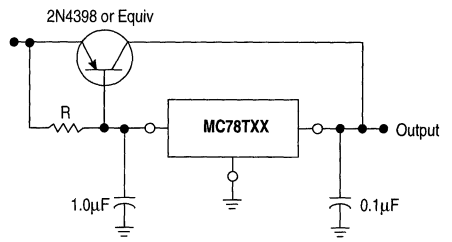
For example, a 2.0 A current source would require R to be a 2.5 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 V.

Figure 15. Adjustable Output Regulator



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 V greater than the regulator voltage.

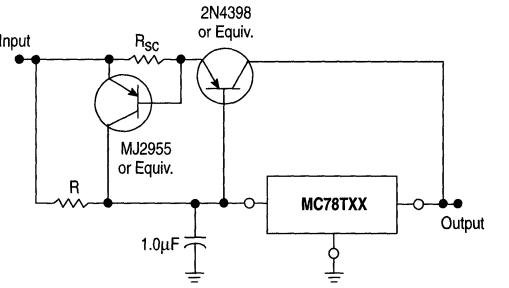
Figure 16. Current Boost Regulator



XX = 2 digits of type number indicating voltage.

The MC78T00 series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 A. Resistor R in conjuction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input–output differential voltage minimum is increased by the V_{BE} of the pass transistor.

Figure 17. Current Boost With Short Circuit Protection



XX = 2 digits of type number indicating voltage.

The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three–terminal regulator. Therefore, an eight–ampere power transistor is specified.

MC78BC00 Series

3

Product Preview

Micropower Voltage Regulator

The MC78BC00 voltage regulators are specifically designed to be used with an external power transistor to deliver high current with high voltage accuracy and low quiescent current.

The MC78BC00 series are devices suitable for constructing regulators with ultra–low dropout voltage and output current in the range of several tens of mA to hundreds of mA. These devices have a chip enable function, which minimizes the standby mode current drain. Each of these devices contains a voltage reference unit, an error amplifier, a driver transistor and resistors. These devices are available in the SOT–23, 5 pin surface mount packages.

These devices are ideally suited for battery powered equipment, and power sources for hand–held audio instruments, communication equipment and domestic appliances.

MC78BC00 Series Features:

- Ultra–Low Supply Current (50 μA)
- Standby Mode (0.2 μA)
- Ultra–Low Dropout Voltage (0.1 V with External Transistor and I_O = 100 mA)
- Excellent Line Regulation (Typically 0.1%/V)
- High Accuracy Output Voltage (±2.5%)

VOLTAGE REGULATOR WITH EXTERNAL POWER TRANSISTOR

SEMICONDUCTOR TECHNICAL DATA

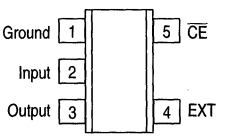
N SUFFIX
PLASTIC PACKAGE
CASE 1212
(SOT–23)

ORDERING INFORMATION

Device	Output Voltage	Operating Temperature Range	Package
MC78BC30NTR	3.0	T_A = –30° to +80°C	SOT–23
MC78BC33NTR	3.3		
MC78BC40NTR	4.0		
MC78BC50NTR	5.0		

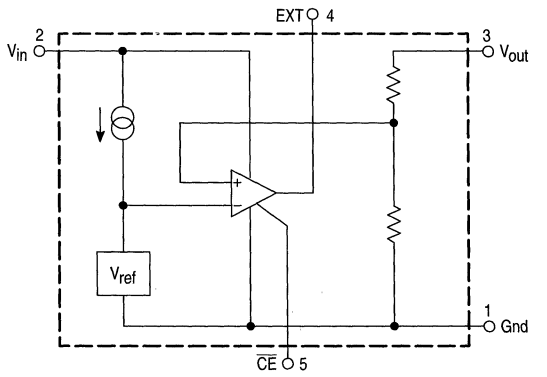
Other voltages from 2.0 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

PIN CONNECTIONS



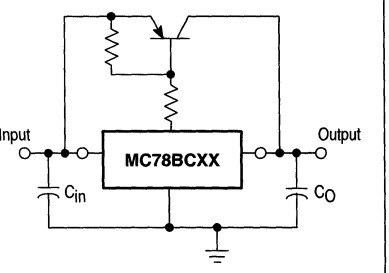
(Top View)

Representative Block Diagram



This device contains 13 active transistors.

Standard Application



MC78FC00 Series

Product Preview

Micropower Voltage Regulator

MICROPOWER ULTRA–LOW QUIESCENT CURRENT VOLTAGE REGULATORS

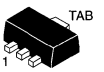
SEMICONDUCTOR TECHNICAL DATA

The MC78FC00 series voltage regulators are specifically designed for use as a power source for video instruments, handheld communication equipment, and battery powered equipment.

The MC78FC00 series voltage regulator ICs feature a high accuracy output voltage and ultra–low quiescent current. Each device contains a voltage reference unit, an error amplifier, a driver transistor, and resistors for setting output voltage, and a current limit circuit. These devices are available in SOT–89 surface mount packages, and allow construction of an efficient, constant voltage power supply circuit.

MC78FC00 Series Features:

- Ultra–Low Quiescent Current of 1.1 μA Typical
- Ultra–Low Dropout Voltage (0.5 V Typical)
- Large Output Current (120 mA Typical)
- Excellent Line Regulation (0.1%)
- Wide Operating Voltage Range (2.0 V to 10 V)
- High Accuracy Output Voltage (±2.5%)
- Wide Output Voltage Range (2.0 V to 6.0 V)
- Surface Mount Package (SOT–89)



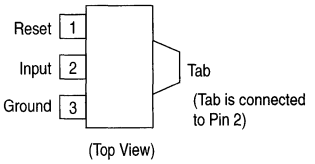
H SUFFIX
PLASTIC PACKAGE
CASE 1213
(SOT–89)

ORDERING INFORMATION

Device	Output Voltage	Operating Temperature Range	Package
MC78FC30HT1	3.0	T_A = –30° to +80°C	SOT–89
MC78FC33HT1	3.3		
MC78FC40HT1	4.0		
MC78FC50HT1	5.0		

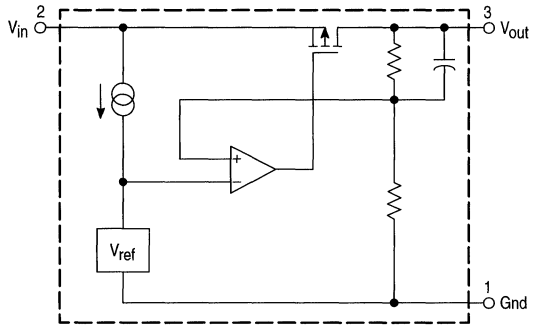
Other voltages from 2.0 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

PIN CONNECTIONS



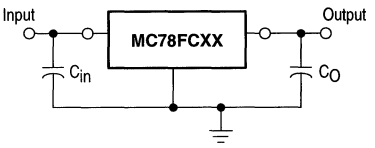
(Top View)

Representative Block Diagram



This device contains 11 active transistors.

Standard Application



3

Product Preview

Micropower Voltage Regulator

The MC78LC00 series voltage regulators are specifically designed for use as a power source for video instruments, handheld communication equipment, and battery powered equipment.

The MC78LC00 series features an ultra–low quiescent of 1.1 µA and a high accuracy output voltage. Each device contains a voltage reference, an error amplifier, a driver transistor and resistors for setting the output voltage. These devices are available in either SOT–89, 3 pin, or SOT–23, 5 pin, surface mount packages.

MC78LC00 Series Features:

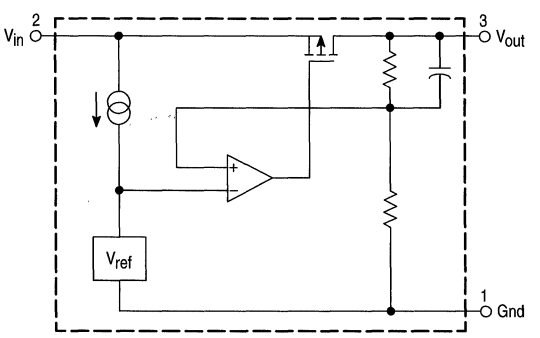
- Low Quiescent Current of 1.1 µA Typical
- Low Dropout Voltage (30 mV Typical)
- Excellent Line Regulation (0.1%)
- High Accuracy Output Voltage (±2.5%)
- Wide Output Voltage Range (2.0 V to 6.0 V)
- Output Current for Low Power (80 mA Typical)
- Two Surface Mount Packages (SOT–89, 3 Pin, or SOT–23, 5 Pin)

ORDERING INFORMATION

Device	Output Voltage	Operating Temperature Range	Package
MC78LC30HT1	3.0	T_A = –30° to +80°C	SOT–89
MC78LC33HT1	3.3		
MC78LC40HT1	4.0		
MC78LC50HT1	5.0		
MC78LC30NTR	3.0		SOT–23
MC78LC33NTR	3.3		
MC78LC40NTR	4.0		
MC78LC50NTR	5.0		

Other voltages from 2.0 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

Representative Block Diagram

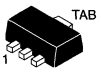


This device contains 8 active transistors.

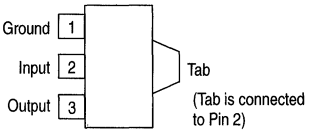
MC78LC00 Series

MICROPOWER ULTRA–LOW QUIESCENT CURRENT VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA

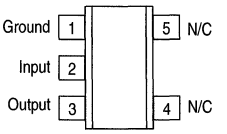


H SUFFIX
PLASTIC PACKAGE
CASE 1213
(SOT–89)



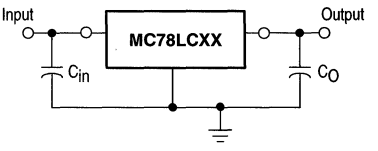
(Top View)

N SUFFIX
PLASTIC PACKAGE
CASE 1212
(SOT–23)



(Top View)

Standard Application



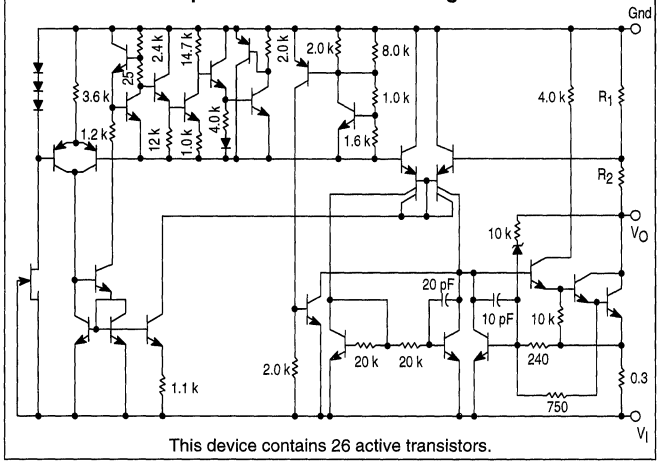
Three-Terminal Negative Voltage Regulators

The MC7900 series of fixed output negative voltage regulators are intended as complements to the popular MC7800 series devices. These negative regulators are available in the same seven–voltage options as the MC7800 devices. In addition, one extra voltage option commonly employed in MECL systems is also available in the negative MC7900 series.

Available in fixed output voltage options from −5.0 V to −24 V, these regulators employ current limiting, thermal shutdown, and safe–area compensation – making them remarkably rugged under most operating conditions. With adequate heatsinking they can deliver output currents in excess of 1.0 A.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Available in 2% Voltage Tolerance (See Ordering Information)

Representative Schematic Diagram



This device contains 26 active transistors.

ORDERING INFORMATION

Device	Output Voltage Tolerance	Operating Temperature Range	Package
MC79XXACD2T	2%	T_J = 0° to +125°C	Surface Mount
MC79XXCD2T	4%		
MC79XXACT	2%		Insertion Mount
MC79XXCT	4%		
MC79XXBD2T	4%	T_J = −40° to +125°C	Surface Mount
MC79XXBT			Insertion Mount

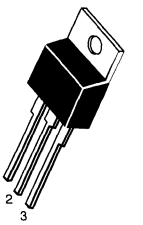
XX indicates nominal voltage.

MC7900 Series

THREE–TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

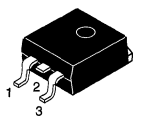
T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface connected to Pin 2.



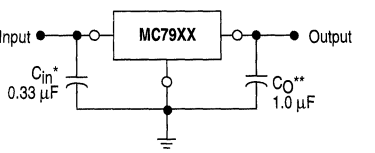
Pin 1. Ground
2. Input
3. Output

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D^2PAK)



Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above more negative even during the high point of the input ripple voltage.

XX, These two digits of the type number indicate nominal voltage.
* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O improve stability and transient response.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7905	5.0 V	MC7912	12 V
MC7905.2	5.2 V	MC7915	15 V
MC7906	6.0 V	MC7918	28 V
MC7908	8.0 V	MC7924	24 V

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (−5.0 V ≥ V_O ≥ −18 V) (24 V)	V_I	−35 −40	Vdc
Power Dissipation Case 221A T_A = +25°C Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case Case 936 (D^2PAK) T_A = +25°C Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case	 P_D θ_{JA} θ_{JC} P_D θ_{JA} θ_{JC}	 Internally Limited 65 5.0 Internally Limited 70 5.0	 W °C/W °C/W W °C/W °C/W
Storage Junction Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W

MC7905C

ELECTRICAL CHARACTERISTICS (V_I = −10 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−4.8	−5.0	−5.2	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) −7.0 Vdc ≥ V_I ≥ −25 Vdc −8.0 Vdc ≥ V_I ≥ −12 Vdc (T_J = +25°C, I_O = 500 mA) −7.0 Vdc ≥ V_I ≥ −25 Vdc −8.0 Vdc ≥ V_I ≥ −12 Vdc	Reg_{line}	 – – – –	 7.0 2.0 35 8.0	 50 25 100 50	mV
Load Regulation, T_J = +25°C (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 11 4.0	 100 50	mV
Output Voltage −7.0 Vdc ≥ V_I ≥ −20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	−4.75	–	−5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change −7.0 Vdc ≥ V_I ≥ −25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I–V_O	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	–	−1.0	–	mV/°C

NOTE: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7905AC

ELECTRICAL CHARACTERISTICS (V_I = −10 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−4.9	−5.0	−5.1	Vdc
Line Regulation (Note 1) −8.0 Vdc ≥ V_I ≥ −12 Vdc; I_O = 1.0 A, T_J = +25°C −8.0 Vdc ≥ V_I ≥ −12 Vdc; I_O = 1.0 A −7.5 Vdc ≥ V_I ≥ −25 Vdc; I_O = 500 mA −7.0 Vdc ≥ V_I ≥ −20 Vdc; I_O = 1.0 A, T_J = +25°C	Reg_{line}	 – – – –	 2.0 7.0 7.0 6.0	 25 50 50 50	mV
Load Regulation (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA 5.0 mA ≤ I_O ≤ 1.0 A	Reg_{load}	 – – –	 11 4.0 9.0	 100 50 100	mV
Output Voltage −7.5 Vdc ≥ V_I ≥ −20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	−4.80	–	−5.20	Vdc
Input Bias Current	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change −7.5 Vdc ≥ V_I ≥ −25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C	ΔI_{IB}	 – – –	 – – –	 1.3 0.5 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	μV
Ripple Rejection (I_O = mA, f = 120 Hz)	RR	–	70	–	dB
Dropout Voltage I_O = 1.0 A. T_J = +25°C	V_I–V_O	 –	 2.0	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 A, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	 –	 −1.0	 –	mV/°C

MC7905.2C

ELECTRICAL CHARACTERISTICS (V_I = −10 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−5.0	−5.2	−5.4	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) −7.2 Vdc ≥ V_I ≥ −25 Vdc −8.0 Vdc ≥ V_I ≥ −12 Vdc (T_J = +25°C, I_O = 500 mA) −7.2 Vdc ≥ V_I ≥ −25 Vdc −8.0 Vdc ≥ V_I ≥ −12 Vdc	Reg_{line}	 – – – –	 8.0 2.2 37 8.5	 52 27 105 52	mV
Load Regulation, T_J = +25°C (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 12 4.5	 105 52	mV
Output Voltage −7.2 Vdc ≥ V_I ≥ −20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	−4.95	–	−5.45	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change −7.2 Vdc ≥ V_I ≥ −25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	42	–	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	68	–	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I–V_O	 –	 2.0	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	 –	 −1.0	 –	mV/°C

NOTE: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7906C

ELECTRICAL CHARACTERISTICS (V_I = −11 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−5.75	−6.0	−6.25	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) −8.0 Vdc ≥ V_I ≥ −25 Vdc −9.0 Vdc ≥ V_I ≥ −13 Vdc (T_J = +25°C, I_O = 500 mA) −8.0 Vdc ≥ V_I ≥ −25 Vdc −9.0 Vdc ≥ V_I ≥ −13 Vdc	Reg_{line}	 – – – –	 9.0 3.0 43 10	 60 30 120 60	mV
Load Regulation, T_J = +25°C (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 13 5.0	 120 60	mV
Output Voltage −8.0 Vdc ≥ V_I ≥ −21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	 −5.7	 –	 −6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change −8.0 Vdc ≥ V_I ≥ −25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	45	–	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I–V_O	 –	 2.0	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 A, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	 –	 −1.0	 –	mV/°C

MC7908C

ELECTRICAL CHARACTERISTICS (V_I = −14 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−7.7	−8.0	−8.3	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) −10.5 Vdc ≥ V_I ≥ −25 Vdc −11 Vdc ≥ V_I ≥ −17 Vdc (T_J = +25°C, I_O = 500 mA) −10.5 Vdc ≥ V_I ≥ −25 Vdc −11 Vdc ≥ V_I ≥ −17 Vdc	Reg_{line}	 – – – –	 12 5.0 50 22	 80 40 160 80	mV
Load Regulation, T_J = +25°C (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 26 9.0	 160 80	mV
Output Voltage −10.5 Vdc ≥ V_I ≥ −23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	 −7.6	 –	 −8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change −10.5 Vdc ≥ V_I ≥ −25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	52	–	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I–V_O	 –	 2.0	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	 –	 −1.0	 –	mV/°C

NOTE: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7912C
ELECTRICAL CHARACTERISTICS (V_I = –19 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–11.5	–12	–12.5	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) –14.5 Vdc ≥ V_I ≥ –30 Vdc –16 Vdc ≥ V_I ≥ –22 Vdc (T_J = +25°C, I_O = 500 mA) –14.5 Vdc ≥ V_I ≥ –30 Vdc –16 Vdc ≥ V_I ≥ –22 Vdc	Reg_{line}	 – – – –	 13 6.0 55 24	 120 60 240 120	mV
Load Regulation, T_J = +25°C (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 46 17	 240 120	mV
Output Voltage –14.5 Vdc ≥ V_I ≥ –27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	 –11.4	 –	 –12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change –14.5 Vdc ≥ V_I ≥ –30 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	75	–	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I–V_O	 –	 2.0	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	 –	 –1.0	 –	mV/°C

MC7912AC
ELECTRICAL CHARACTERISTICS (V_I = –19 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–11.75	–12	–12.25	Vdc
Line Regulation (Note 1) –16 Vdc ≥ V_I ≥ –22 Vdc; I_O = 1.0 A, T_J = +25°C –16 Vdc ≥ V_I ≥ –22 Vdc; I_O = 1.0 A –14.8 Vdc ≥ V_I ≥ –30 Vdc; I_O = 500 mA –14.5 Vdc ≥ V_I ≥ –27 Vdc; I_O = 1.0 A, T_J = +25°C	Reg_{line}	 – – – –	 6.0 24 24 13	 60 120 120 120	mV
Load Regulation (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA 5.0 mA ≤ I_O ≤ 1.0 A	Reg_{load}	 – – –	 46 17 35	 150 75 150	mV
Output Voltage –14.8 Vdc ≥ V_I ≥ –27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	 –11.5	 –	 –12.5	Vdc
Input Bias Current	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change –15 Vdc ≥ V_I ≥ –30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C	ΔI_{IB}	 – – –	 – – –	 0.8 0.5 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	75	–	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I–V_O	 –	 2.0	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 A, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	 –	 –1.0	 –	mV/°C

NOTE: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7915C
ELECTRICAL CHARACTERISTICS (V_I = −23 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−14.4	−15	−15.6	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) −17.5 Vdc ≥ V_I ≥ −30 Vdc −20 Vdc ≥ V_I ≥ −26 Vdc (T_J = +25°C, I_O = 500 mA) −17.5 Vdc ≥ V_I ≥ −30 Vdc −20 Vdc ≥ V_I ≥ −26 Vdc	Reg_{line}	 – – – –	 14 6.0 57 27	 150 75 300 150	mV
Load Regulation, T_J = +25°C (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 68 25	 300 150	mV
Output Voltage −17.5 Vdc ≥ V_I ≥ −30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	−14.25	–	−15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change −17.5 Vdc ≥ V_I ≥ −30 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I–V_O	 –	 2.0	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 A, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	 –	 −1.0	 –	mV/°C

MC7915AC
ELECTRICAL CHARACTERISTICS (V_I = −23 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−14.7	−15	−15.3	Vdc
Line Regulation (Note 1) −20 Vdc ≥ V_I ≥ −26 Vdc, I_O = 1.0 A, T_J = +25°C −20 Vdc ≥ V_I ≥ −26 Vdc, I_O = 1.0 A, −17.9 Vdc ≥ V_I ≥ −30 Vdc, I_O = 500 mA −17.5 Vdc ≥ V_I ≥ −30 Vdc, I_O = 1.0 A, T_J = +25°C	Reg_{line}	 – – – –	 27 57 57 57	 75 150 150 150	mV
Load Regulation (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA 5.0 mA ≤ I_O ≤ 1.0 A	Reg_{load}	 – – –	 68 25 40	 150 75 150	mV
Output Voltage −17.9 Vdc ≥ V_I ≥ −30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	−14.4	–	−15.6	Vdc
Input Bias Current	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change −17.5 Vdc ≥ V_I ≥ −30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C	ΔI_{IB}	 – – –	 – – –	 0.8 0.5 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I–V_O	 –	 2.0	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	 –	 −1.0	 –	mV/°C

NOTE: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7918C
ELECTRICAL CHARACTERISTICS (V_I = −27 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−17.3	−18	−18.7	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) −21 Vdc ≥ V_I ≥ −33 Vdc −24 Vdc ≥ V_I ≥ −30 Vdc (T_J = +25°C, I_O = 500 mA) −21 Vdc ≥ V_I ≥ −33 Vdc −24 Vdc ≥ V_I ≥ −30 Vdc	Reg_{line}	 – – – –	 25 10 90 50	 180 90 360 180	mV
Load Regulation, T_J = +25°C (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 110 55	 360 180	mV
Output Voltage −21 Vdc ≥ V_I ≥ −33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	−17.1	–	−18.9	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	8.0	mA
Input Bias Current Change −21 Vdc ≥ V_I ≥ −33 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	110	–	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I–V_O	 –	 2.0	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	 –	 −1.0	 –	mV/°C

MC7924C
ELECTRICAL CHARACTERISTICS (V_I = −33 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−23	−24	−25	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) −27 Vdc ≥ V_I ≥ −38 Vdc −30 Vdc ≥ V_I ≥ −36 Vdc (T_J = +25°C, I_O = 500 mA) −27 Vdc ≥ V_I ≥ −38 Vdc −30 Vdc ≥ V_I ≥ −36 Vdc	Reg_{line}	 – – – –	 31 14 118 70	 240 120 470 240	mV
Load Regulation, T_J = +25°C (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 150 85	 480 240	mV
Output Voltage −27 Vdc ≥ V_I ≥ −38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	−22.8	–	−25.2	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.6	8.0	mA
Input Bias Current Change −27 Vdc ≥ V_I ≥ −38 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	170	–	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I–V_O	 –	 2.0	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	 –	 −1.0	 –	mV/°C

NOTE: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Figure 1. Worst Case Power Dissipation as a Function of Ambient Temperature

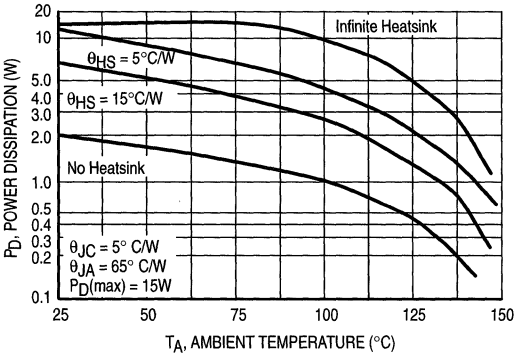


Figure 2. Peak Output Current as a Function of Input–Output Differential Voltage

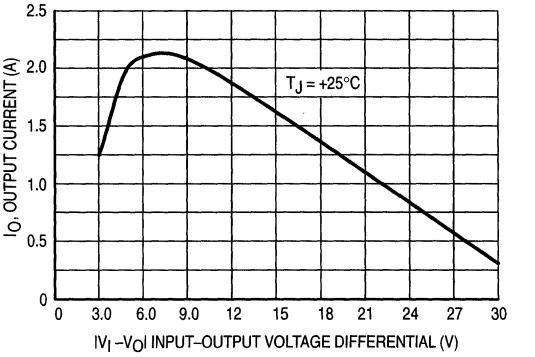


Figure 3. Ripple Rejection as a Function of Frequency

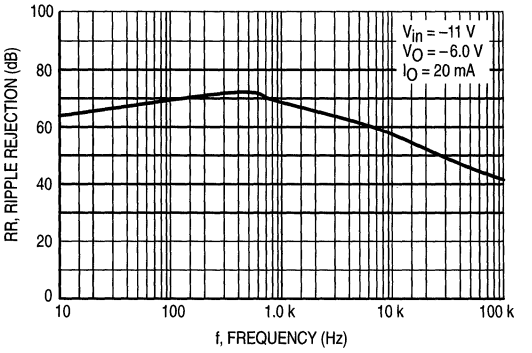


Figure 4. Ripple Rejection as a Function of Output Voltage

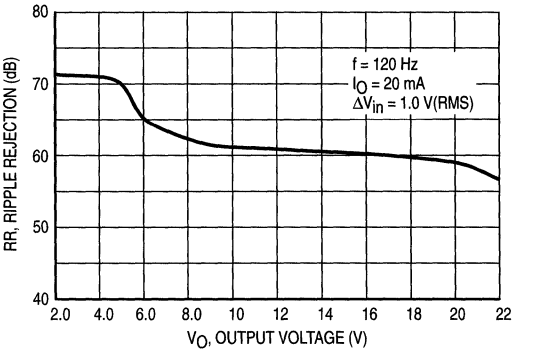


Figure 5. Output Voltage as a Function of Junction Temperature

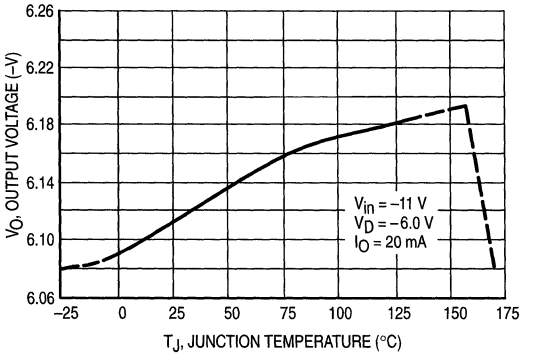
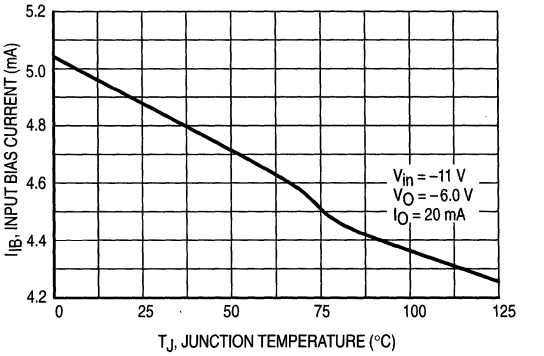


Figure 6. Quiescent Current as a Function of Temperature



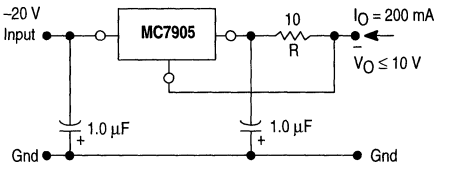
APPLICATIONS INFORMATION

Design Considerations

The MC7900 Series of fixed voltage regulators are designed with Thermal overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The capacitor chosen should have an equivalent series resistance of less than 0.7 Ω. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Figure 7. Current Regulator



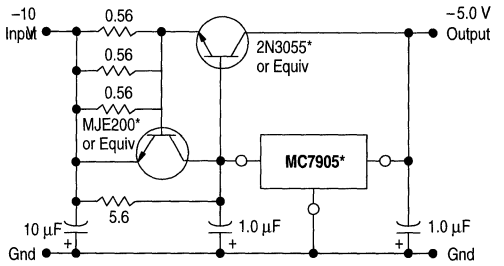
The MC7905, –5.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows.

$$I_O = \frac{5.0\ V}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 5.0 V regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

Figure 8. Current Boost Regulator

(–5.0 V @ 4.0 A, with 5.0 A Current Limiting)

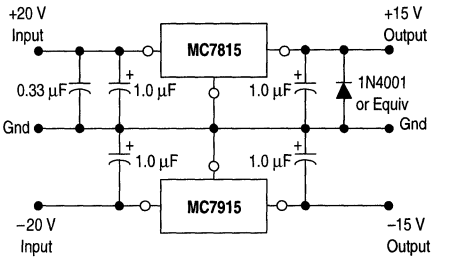


*Mounted on heatsink.

When a boost transistor is used, short circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0.6 V/R_{SC}. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heatsink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

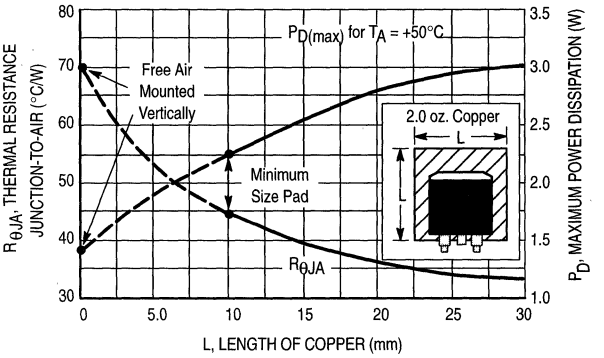
Figure 9. Operational Amplifier Supply

(±15 @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch–up problems whenever the output of the positive regulator (MC7815) is drawn below ground with an output current greater than 200 mA.

Figure 10. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MC79L00, A Series

Three-Terminal Low Current Negative Voltage Regulators

THREE–TERMINAL LOW CURRENT NEGATIVE FIXED VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA

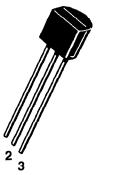
The MC79L00, A Series negative voltage regulators are inexpensive, easy–to–use devices suitable for numerous applications requiring up to100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00 devices are useful for on–card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

- No External Components Required
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

P SUFFIX
PLASTIC PACKAGE
CASE 29

Pin 1. Ground
2. Input
3. Output

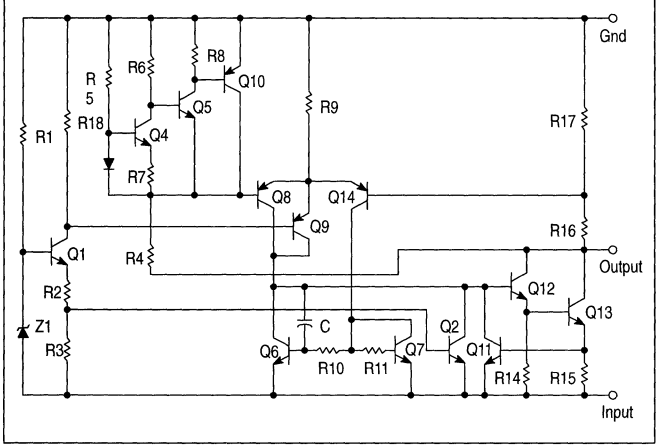


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)*

Pin 1. V_{out}
2. V_{in}
3. V_{in}
4. NC
5. GND
6. V_{in}
7. V_{in}
8. NC

* SOP–8 is an internally modified SO–8 package. Pins 2, 3, 6, and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP–8 conforms to all external dimensions of the standard SO–8 package.

Representative Schematic Diagram



* Automotive temperature range selections are available with special test conditions and additional tests in 5, 12 and 15 V devices. Contact your local Motorola sales office for information.

Device No. ±10%	Device No. 5%	Nominal Voltage
MC79L05C	MC79L05AC	–5.0
MC79L12C	MC79L12AC	–12
MC79L15C	MC79L15AC	–15
MC79L18C	MC79L18AC	–18
MC79L24C	MC79L24AC	–24

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC79LXXACD*	T_J = 0° to +125°C	SOP–8
MC79LXXACP		Plastic Power
MC79LXXCP		Plastic Power
MC79LXXABD*	T_J = –40° to +125°C	SOP–8
MC79LXXABP*		Plastic Power

XX indicates nominal voltage

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (–5 V) (–12, –15, –18 V) (–24 V)	V_I	–30 –35 –40	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	+150	°C

3

ELECTRICAL CHARACTERISTICS (V_I = –10 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J +125°C (for MC79LXXAB), 0°C < T_J < +125°C (for MC79LXXAC)).

Characteristics	Symbol	MC79L05C, AB			MC79L05AC, AB			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–4.6	–5.0	–5.4	–4.8	–5.0	–5.2	Vdc
Input Regulation (T_J = +25°C) –7.0 Vdc ≥ V_I ≥ –20 Vdc –8.0 Vdc ≥ V_I ≥ –20 Vdc	Reg_{line}	 – –	 – –	 200 150	 – –	 – –	 150 100	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 60 30	 – –	 – –	 60 30	mV
Output Voltage –7.0 Vdc ≥ V_I ≥ –20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = –10 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 –4.5 –4.5	 – –	 –5.5 –5.5	 –4.75 –4.75	 – –	 –5.25 –5.25	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.0 5.5	 – –	 – –	 6.0 5.5	mA
Input Bias Current Change –8.0 Vdc ≥ V_I ≥ –20 Vdc 1.0 mA ≤ I_O ≤ 40 mA	I_{IB}	 – –	 – –	 1.5 0.2	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	–	40	–	µV
Ripple Rejection (–8.0 ≥ V_I ≥ –18 Vdc, f = 120 Hz, T_J = +25°C)	RR	40	49	–	41	49	–	dB
Dropout Voltage (I_O = 40 mA, T_J = +25°C)	$\|V_I–V_O\|$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = –19 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J +125°C (for MC79LXXAC), 0°C < T_J < +125°C (for MC79LXXAB)).

Characteristics	Symbol	MC79L12C, AB			MC79L12AC, AB			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–11.1	–12	–12.9	–11.5	–12	–12.5	Vdc
Input Regulation (T_J = +25°C) –14.5 Vdc ≥ V_I ≥ –27 Vdc –16 Vdc ≥ V_I ≥ –27 Vdc	Reg_{line}	 – –	 – –	 250 200	 – –	 – –	 250 200	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 100 50	 – –	 – –	 100 50	mV
Output Voltage –14.5 Vdc ≥ V_I ≥ –27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = –19 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 –10.8 –10.8	 – –	 –13.2 –13.2	 –11.4 –11.4	 – –	 –12.6 –12.6	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.5 6.0	 – –	 – –	 6.5 6.0	mA
Input Bias Current Change –16 Vdc ≥ V_I ≥ –27 Vdc 1.0 mA ≤ I_O ≤ 40 mA	I_{IB}	 – –	 – –	 1.5 0.2	 – –	 – –	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	80	–	–	80	–	µV
Ripple Rejection (–15 ≤ V_I ≤ –25 Vdc, f = 120 Hz, T_J = +25°C)	RR	36	42	–	37	42	–	dB
Dropout Voltage (I_O = 40 mA, T_J = +25°C)	$\|V_I–V_O\|$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = –23 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J +125°C (for MC79LXXAB), 0°C < T_J < +125°C (for MC79LXXAC)).

Characteristics	Symbol	MC79L15C			MC79L15AC, AB			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–13.8	–15	–16.2	–14.4	–15	–15.6	Vdc
Input Regulation (T_J = +25°C) –17.5 Vdc ≥ V_I ≥ –30 Vdc –20 Vdc ≥ V_I ≥ –30 Vdc	Reg_{line}	 – –	 – –	 300 250	 – –	 – –	 300 250	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 150 75	 – –	 – –	 150 75	mV
Output Voltage –17.5 Vdc ≥ V_I ≥ –Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = –23 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 –13.5 –13.5	 – –	 –16.5 –16.5	 –14.25 –14.25	 – –	 –15.75 –15.75	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.5 6.0	 – –	 – –	 6.5 6.0	mA
Input Bias Current Change –20 Vdc ≥ V_I ≥ –30 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – –	 – –	 1.5 0.2	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	–	90	–	µV
Ripple Rejection (–18.5 ≤ V_I ≤ –28.5 Vdc, f = 120 Hz)	RR	33	39	–	34	39	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = –27 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J > +125°C, unless otherwise noted).

Characteristics	Symbol	MC79L18C			MC79L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–16.6	–18	–19.4	–17.3	–18	–18.7	Vdc
Input Regulation (T_J = +25°C) –20.7 Vdc ≥ V_I ≥ –33 Vdc –21.4 Vdc ≥ V_I ≥ –33 Vdc –22 Vdc ≥ V_I ≥ –33 Vdc –21 Vdc ≥ V_I ≥ –33 Vdc	Reg_{line}	 – – – –	 – – – –	 – 325 275 –	 – – – –	 – – – –	 325 – – 275	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 170 85	 – –	 – –	 170 85	mV
Output Voltage –20.7 Vdc ≥ V_I ≥ –33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA –21.4 Vdc ≥ V_I ≥ –33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = –27 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 – –16.2 –16.2	 – – –	 – –19.8 –19.8	 –17.1 – –17.1	 – – –	 –18.9 – –18.9	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.5 6.0	 – –	 – –	 6.5 6.0	mA
Input Bias Current Change –21 Vdc ≥ V_I ≥ –33 Vdc –27 Vdc ≥ V_I ≥ –33 Vdc 1.0 mA ≤ I_O ≤ 40 mA	I_{IB}	 – – –	 – – –	 – 1.5 0.2	 – – –	 – – –	 1.5 – 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	150	–	–	150	–	µV
Ripple Rejection (–23 ≤ V_I ≤ –33 Vdc, f = 120 Hz, T_J = +25°C)	RR	32	46	–	33	48	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = –33 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted).

Characteristics	Symbol	MC79L24C			MC79L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–22.1	–24	–25.9	–23	–24	–25	Vdc
Input Regulation (T_J = +25°C) –27 Vdc ≥ V_I ≥ –38 Vdc –27.5 Vdc ≥ V_I ≥ –38 Vdc –28 Vdc ≥ V_I ≥ –38 Vdc	Reg_{line}	 – – –	 – – –	 – 350 300	 – – –	 – – –	 350 – 300	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 200 100	 – –	 – –	 200 100	mV
Output Voltage –27 Vdc ≥ V_I ≥ –38 V, 1.0 mA ≤ I_O ≤ 40 mA –28 Vdc ≥ V_I ≥ –38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = –33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 – –21.4 –21.4	 – – –	 – –26.4 –26.4	 –22.8 – –22.8	 – – –	 –25.2 – –25.2	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.5 6.0	 – –	 – –	 6.5 6.0	mA
Input Bias Current Change –28 Vdc ≥ V_I ≥ –38 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – –	 – –	 1.5 0.2	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	200	–	–	200	–	µV
Ripple Rejection (–29 ≤ V_I ≤ –35 Vdc, f = 120 Hz, T_J = +25°C)	RR	30	43	–	31	47	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\|V_I–V_O\|$	–	1.7	–	–	1.7	–	Vdc

APPLICATIONS INFORMATION

Design Considerations

The MC79L00, A Series of fixed voltage regulators are designed with Thermal Overload Protections that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire length, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Figure 1. Positive and Negative Regulator

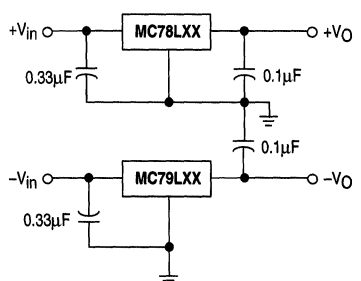
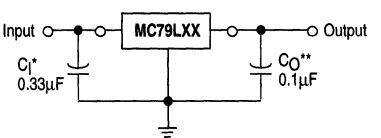


Figure 2. Standard Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the ripple voltage.

* C_I is required if regulator is located an appreciable distance from the power supply filter

** C_O improves stability and transient response.

TYPICAL CHARACTERISTICS

(T_A = +25°C, unless otherwise noted.)

Figure 3. Dropout Characteristics

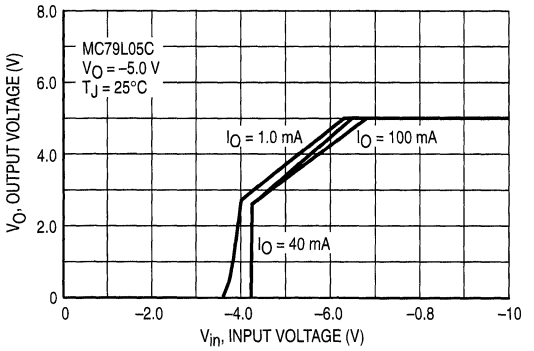


Figure 4. Dropout Voltage versus Junction Temperature

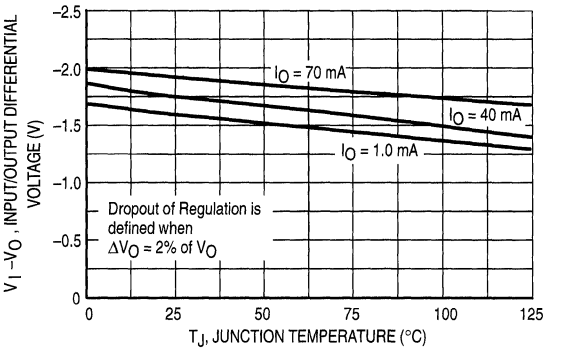


Figure 5. Input Bias Current versus Ambient Temperature

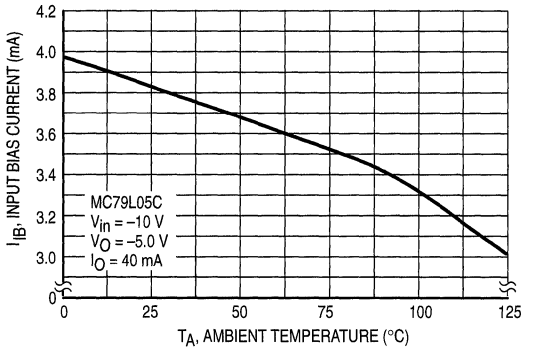


Figure 6. Input Bias Current versus Input Voltage

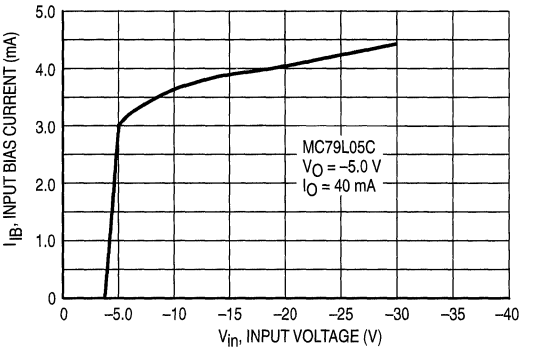


Figure 7. Maximum Average Power Dissipation versus Ambient Temperature (TO–92)

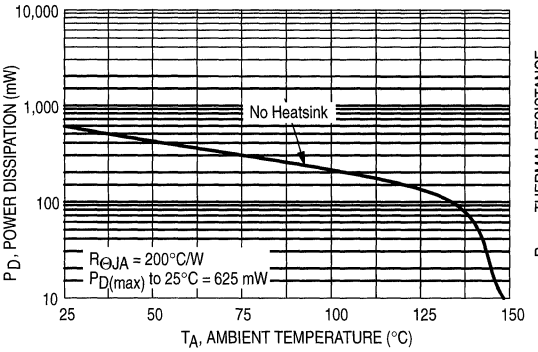
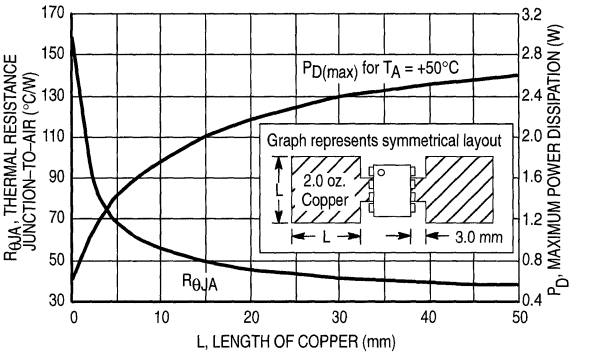


Figure 8. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MC79M00 Series

Three-Terminal Negative Voltage Regulators

The MC79M00 series of fixed output negative voltage regulators are intended as complements to the popular MC78M00 series devices.

Available in fixed output voltage options of –5.0, –8.0, –12 and –15 V, these regulators employ current limiting, thermal shutdown, and safe–area compensation – making them remarkably rugged under most operating conditions. With adequate heatsinking they can deliver output currents in excess of 0.5 A.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Also Available in Surface Mount DPAK (DT) Package

THREE–TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

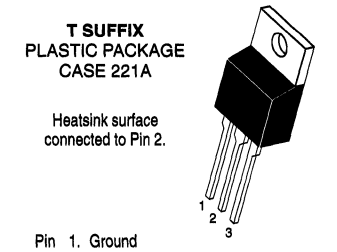
DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC79M05	–5.0 V	MC79M12	–12 V
MC79M08	–8.0 V	MC79M15	–15 V

ORDERING INFORMATION

Device	Output Voltage Tolerance	Operating Temperature Range	Package
MC79MXXBDT, BDT–1	4.0%	T_J = –40° to +125°C	DPAK
MC79MXXBT			Plastic Power
MC79MXXCDT, CDT–1		T_J = 0° to +125°C	DPAK
MC79MXXCT			Plastic Power

XX indicates nominal voltage.

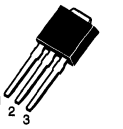


T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface connected to Pin 2.

Pin 1. Ground
2. Input
3. Output

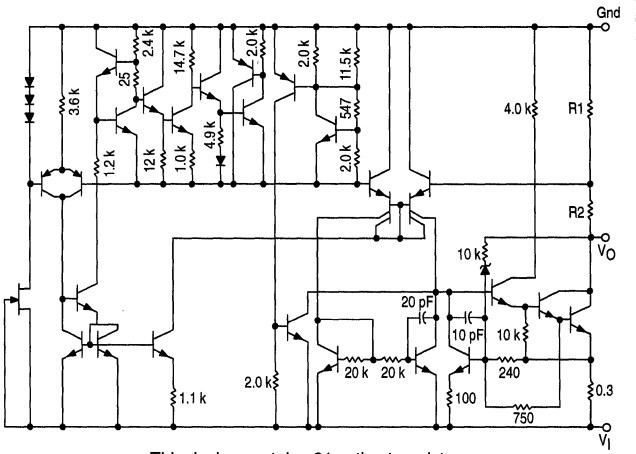
DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)



DT–1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)

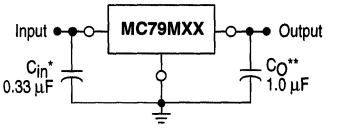
Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

Representative Schematic Diagram



This device contains 31 active transistors.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.1 V more negative even during the high point of the input ripple voltage.

XX, These two digits of the type number indicate nominal voltage.
* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O improve stability and transient response.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	–35	Vdc
Power Dissipation			
Case 221A			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	65	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Case 369 and 369A (DPAK)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	92	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	6.0	°C/W
Storage Junction Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	150	°C

NOTE: ESD data available upon request.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W

MC79M05B, C
ELECTRICAL CHARACTERISTICS (V_I = –10 V, I_O = 350 mA, T_{low} to T_{high} [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	–4.8	–5.0	–5.2	Vdc
Line Regulation, T_J = 25°C (Note 1) –7.0 Vdc ≥ V_I ≥ –25 Vdc –8.0 Vdc ≥ V_I ≥ –18 Vdc	Reg_{line}	 – –	 7.0 2.0	 50 30	mV
Load Regulation, T_J = 25°C (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	–	30	100	mV
Output Voltage –7.0 Vdc ≥ V_I ≥ –25 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	–4.75	–	–5.25	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change –8.0 Vdc ≥ V_I ≥ –25 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = –10 V	ΔI_{IB}	 – –	 – –	 0.4 0.4	mA
Output Noise Voltage, T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz	V_n	–	40	–	μV
Ripple Rejection (f = 120 Hz)	RR	54	66	–	dB
Dropout Voltage I_O = 500 mA, T_J = 25°C	V_I–V_O	–	1.1	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ 125°C	$\Delta V_O/\Delta T$	–	0.2	–	mV/°C

NOTES: 1. Load and line regulation are specified at constant temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
2. B = T_{low} to T_{high}, –40°C < T_J < 125°C
C = T_{low} to T_{high}, 0°C < T_J < 125°C

MC79M08B, C
ELECTRICAL CHARACTERISTICS (V_I = –10 V, I_O = 350 mA, T_{low} to T_{high} [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	–7.7	–8.0	–8.3	Vdc
Line Regulation, T_J = 25°C (Note 1) –7.0 Vdc ≥ V_I ≥ –25 Vdc –8.0 Vdc ≥ V_I ≥ –18 Vdc	Reg_{line}	 – –	 5.0 3.0	 80 50	mV
Load Regulation, T_J = 25°C (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	 –	 30	 100	mV
Output Voltage –7.0 Vdc ≥ V_I ≥ –25 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	 –7.6	 –8.0	 –8.4	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	–	8.0	mA
Input Bias Current Change –8.0 Vdc ≥ V_I ≥ –25 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = –10 V	ΔI_{IB}	 – –	 – –	 0.4 0.4	mA
Output Noise Voltage, T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz	V_n	–	60	–	μV
Ripple Rejection (f = 120 Hz)	RR	54	63	–	dB
Dropout Voltage I_O = 500 mA, T_J = 25°C	V_I–V_O	 –	 1.1	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ 125°C	$\Delta V_O/\Delta T$	 –	 0.4	 –	mV/°C

MC79M12B, C
ELECTRICAL CHARACTERISTICS (V_I = –19 V, I_O = 350 mA, T_{low} to T_{high} [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	–11.5	–12	–12.5	Vdc
Line Regulation, T_J = 25°C (Note 1) –14.5 Vdc ≥ V_I ≥ –30 Vdc –15 Vdc ≥ V_I ≥ –25 Vdc	Reg_{line}	 – –	 5.0 3.0	 80 50	mV
Load Regulation, T_J = 25°C (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	 –	 30	 240	mV
Output Voltage –14.5 Vdc ≥ V_I ≥ –30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	 –11.4	 –	 –12.6	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change –14.5 Vdc ≥ V_I ≥ –30 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = –19 V	ΔI_{IB}	 – –	 – –	 0.4 0.4	mA
Output Noise Voltage, T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz	V_n	–	75	–	μV
Ripple Rejection (f = 120 Hz)	RR	54	60	–	dB
Dropout Voltage I_O = 500 mA, T_J = 25°C	V_I–V_O	 –	 1.1	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ 125°C	$\Delta V_O/\Delta T$	 –	 –0.8	 –	mV/°C

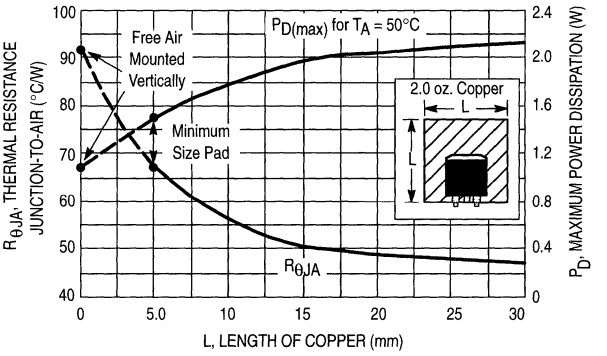
NOTES: 1. Load and line regulation are specified at constant temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
2. B = T_{low} to T_{high}, –40°C < T_J < 125°C
C = T_{low} to T_{high}, 0°C < T_J < 125°C

MC79M15B, C
ELECTRICAL CHARACTERISTICS (V_I = –23 V, I_O = 350 mA, T_{low} to T_{high} [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	–14.4	–15	–15.6	Vdc
Line Regulation, T_J = 25°C (Note 1) –17.5 Vdc ≥ V_I ≥ –30 Vdc –18 Vdc ≥ V_I ≥ –28 Vdc	Reg_{line}	 – –	 5.0 3.0	 80 50	mV
Load Regulation, T_J = 25°C (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	–	30	240	mV
Output Voltage –17.5 Vdc ≥ V_I ≥ –30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	–14.25	–	–15.75	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change –17.5 Vdc ≥ V_I ≥ –30 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = –23 V	ΔI_{IB}	 – –	 – –	 0.4 0.4	mA
Output Noise Voltage, T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz	V_n	–	90	–	μV
Ripple Rejection (f = 120 Hz)	RR	54	60	–	dB
Dropout Voltage I_O = 500 mA, T_J = 25°C	V_I–V_O	–	1.1	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ 125°C	$\Delta V_O/\Delta T$	–	–1.0	–	mV/°C

NOTES: 1. Load and line regulation are specified at constant temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
2. B = T_{low} to T_{high}, –40°C < T_J < 125°C
C = T_{low} to T_{high}, 0°C < T_J < 125°C

Figure 1. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MOTOROLA

MC33128

Power Management Controller

3

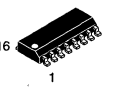
The MC33128 is a power management controller specifically designed for use in battery powered cellular telephone and pager applications. This device contains all of the active functions required to interface the user to the system electronics via a microprocessor. This integrated circuit consists of a low dropout voltage regulator with power–up reset for MPU power, two low dropout voltage regulators for independant powering of analog and digital circuitry, and a negative charge pump voltage regulator for full depletion of gallium arsenide MESFETs.

Also included are protective system shutdown features consisting of a battery latch that is activated upon battery insertion, low battery voltage shutdown, and a thermal over temperature detector. This device is available in a 16–pin narrow body surface mount plastic package.

- Three Positive Regulated Outputs Featuring Low Dropout Voltage
- Negative Regulated Output for Full Depletion of GaAs MESFETs
- MPU Power Up Reset
- Battery Latch
- Low Battery Shutdown
- Pinned–Out Reference for MPU A/D Converter
- Low Start–Up and Operating Current
- Thermal Protection

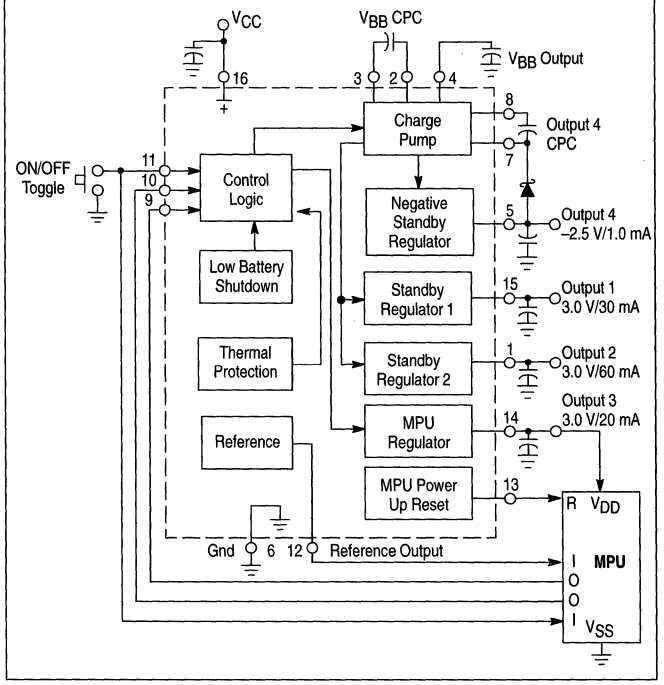
POWER MANAGEMENT CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

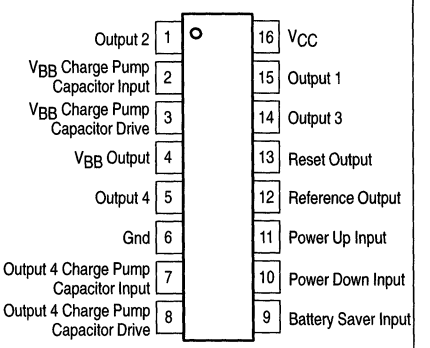


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33128D	T_A = – 30° to +60°C	SO–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage (Pin 16)	V_{CC}	+7.0	V
Input Voltage Range Power Up, Power Down, and Battery Saver Inputs (Pins 11, 10, 9)	V_{in}	−1.0 to V_{CC} + 1.0	V
Charge Pump Capacitor Drive Outputs, Source or Sink Current (Pins 3, 8)	$I_{O(max)}$	30	mA
Schottky Diode Forward Current (Pins 16 to 2, 2 to 4, and 7 to 6)	$I_{F(max)}$	30	mA
Output Source Current (Note 1) Regulator Output 1 (Pin 15) Regulator Output 2 (Pin 1) Regulator Output 3 (Pin 14) Regulator Output 4 (Pin 5) Reference (Pin 12)	I_{Source}	 150 250 50 10 40	mA
Reset Sink Current (Pin 13)	I_{Sink}	5.0	mA
Power Dissipation and Thermal Characteristic D Suffix, Plastic Package Case 751B Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air	 P_D $R_{\varnothing JA}$	 560 180	 mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 1)	T_A	−30 to +60	°C
Storage Temperature	T_{stg}	−60 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V, C_{in} = 33 µF with ESR ≤ 1.6 Ω, C_O = 4.7 µF with ESR ≤ 4.5 Ω, I_{O1} = 30 mA, I_{O2} = 60 mA, I_{O3} = 20 mA, I_{O4} = 1.0 mA, I_{Oref} = 10 mA [Note 2], T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER UP INPUT (Pin 11)					
Low State Input Threshold Voltage	$V_{th(toggle)}$	V_{CC} − 1.5	V_{CC} − 1.2	V_{CC} − 0.8	V
Input Current (V_{in} = V_{O3})	$I_{in(toggle)}$	–	–	120	µA
Internal Pull Up Resistance	$R_{PU(ON/OFF)}$	10	20	30	kΩ
POWER DOWN INPUT (Pin 10)					
High State Input Threshold Voltage (Places IC in Standby Mode)	$V_{th(PDI)}$	1.3	1.5	1.8	V
Input Current (V_{in} = V_{O3})	$I_{in(PDI)}$	–	–	120	µA
BATTERY SAVER INPUT (Pin 9)					
High State Input Threshold Voltage (V_{BB}, V_{O1}, V_{O2}, V_{O4} Activated)	$V_{th(BSI)}$	1.2	1.4	1.7	V
Input Current (V_{in} = V_{O3})	$I_{in(BSI)}$	–	–	120	µA
V_{BB} GENERATOR					
Oscillator Frequency	f_{OSC}	85	95	105	kHz
Oscillator Duty Cycle	DC	35	50	65	%
Charge Pump Capacitor Drive Output Voltage Swing (Pin 3) High State (I_{Source} = 3.0 mA) Low State (I_{Sink} = 3.0 mA)	 V_{OH} V_{OL}	 – –	 V_{CC} − 0.9 0.15	 – –	V
Schottky Diode (Pins 2, 4) Forward Voltage Drop (I_F = 3.0 mA) Reverse Leakage Current (V_{BB} = 7.0 V)	 V_F I_L	 – –	 0.5 0.01	 – –	 V µA
Output Voltage (Pin 4) V_{CC} = 4.5 V V_{CC} = 2.9 V	$V_{O(VBB)}$	 – –	 7.9 4.4	 – –	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. All outputs are fully loaded as stated in the Electrical Characteristics Table above, except for the one under test.

3

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V, C_{in} = 33 µF with ESR ≤ 1.6 Ω, C_O = 4.7 µF with ESR ≤ 4.5 Ω, I_{O1} = 30 mA, I_{O2} = 60 mA, I_{O3} = 20 mA, I_{O4} = 1.0 mA, I_{Oref} = 10 mA [Note 2], T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT 1 (Pin 15)					
Output Voltage (V_{CC} = 3.15 V to 4.5 V, I_{O1} = 30 mA)	Reg_{line1}	2.9	3.0	3.1	V
Load Regulation (I_{O1} = 0 mA to 35 mA)	Reg_{load1}	–	5.0	30	mV
Dropout Voltage (V_{CC} = 2.9 V, I_{O1} = 30 mA)	$V_{in} - V_{O1}$	–	–	0.1	V
Power Supply Rejection Ratio f = 120 Hz f = 100 kHz	PSRR 1	 – –	 70 40	 – –	dB
Turn ON Delay Time (Battery Saver Input to 90% V_{O1} Output)	t_{DLY1}	–	0.2	2.0	ms
REGULATOR OUTPUT 2 (Pin 1)					
Output Voltage (V_{CC} = 3.15 V to 4.5 V, I_{O2} = 60 mA)	Reg	2.9	3.0	3.1	V
Load Regulation (I_{O2} = 0 mA to 60 mA)	Reg_{load2}	–	5.0	40	mV
Dropout Voltage (V_{CC} = 2.9 V, I_{O2} = 60 mA)	$V_{in} - V_{O2}$	–	–	0.11	V
Power Supply Rejection Ratio f = 120 Hz f = 100 kHz	PSRR 2	 – –	 70 40	 – –	dB
Turn ON Delay Time (Battery Saver Input to 90% V_{O2} Output)	t_{DLY2}	–	0.2	2.0	ms
REGULATOR OUTPUT 3 (Pin 14)					
Output Voltage (V_{CC} = 3.15 V to 4.5 V, I_{O3} = 20 mA)	Reg_{line3}	2.9	3.0	3.1	V
Load Regulation (I_{O3} = 0 mA to 20 mA)	Reg_{load3}	–	5.0	25	mV
Dropout Voltage (V_{CC} = 2.9 V, I_{O3} = 20 mA)	$V_{in} - V_{O3}$	–	–	0.1	V
Power Supply Rejection Ratio f = 120 Hz f = 100 kHz	PSRR 3	 – –	 70 40	 – –	dB
Turn ON Delay Time (ON/OFF Toggle Input to 90% V_{O3} Output)	t_{DLY3}	–	0.5	3.0	ms
REGULATOR OUTPUT 4 (Pin 5)					
Output Voltage (V_{CC} = 3.15 V to 4.5 V, I_{O4} = 1.0 mA)	Reg_{line4}	−2.35	−2.5	−2.65	V
Load Regulation (I_{O4} = 0 mA to 1.0 mA)	Reg_{load4}	–	5.0	20	mV
Power Supply Rejection Ratio f = 120 Hz f = 100 kHz	PSRR 4	 – –	 70 40	 – –	dB
Schottky Diode Forward Voltage Drop (Pins 7, 6, I_F = 1.0 mA)	V_F	–	0.5	–	V
Charge Pump Capacitor Drive Output Voltage Swing (Pin 8) High State (I_{Source} = 1.0 mA) Low State (I_{Sink} = 1.0 mA)	 V_{OH} V_{OL}	 – –	 V_{BB} − 0.25 0.15	 – –	V
Turn ON Delay Time (Battery Saver Input to 90% V_{O4} Output)	t_{DLY4}	–	4.0	10	ms
REFERENCE OUTPUT (Pin 12)					
Output Voltage (I_O = 0 mA to 10 mA)	Reg_{load}	1.46	1.5	1.54	V
MPU POWER UP RESET COMPARATOR (Pin 13)					
Threshold Voltage Low State Output (V_{O3} Decreasing) Hysteresis (V_{O3} Increasing)	 $V_{th(low)}$ V_H	 2.5 40	 2.6 60	 2.7 100	V mV
Output Sink Saturation (I_{Sink} = 100 µA, V_{O3} = 2.5 V to 1.0 V)	$V_{CE(sat)}$	–	130	300	mV
Internal Pull–up Resistance	R_{PU}	10	26	40	kΩ
High State Output Voltage (V_{O3} = 2.8 V)	V_{OH}	0.95 V_{O3}	V_{O3}	–	V

NOTE: 2. All outputs are fully loaded as stated in the Electrical Characteristics Table above, except for the one under test.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V, C_{in} = 33 µF with ESR ≤ 1.6 Ω, C_O = 4.7 µF with ESR ≤ 4.5 Ω, I_{O1} = 30 mA, I_{O2} = 60 mA, I_{O3} = 20 mA, I_{O4} = 1.0 mA, I_{Oref} = 10 mA [Note 2], T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
LOW BATTERY SHUTDOWN COMPARATOR (Pin 16)					
Shutdown Threshold Voltage (V_{CC} Decreasing, Pin 10 = Gnd)	$V_{th(LBSC)}$	2.25	2.4	2.55	V
TOTAL DEVICE (Pin 16)					
Power Supply Current (No Load On All Outputs)	I_{CC}				
Operating					
Battery Saver Input High (Pin 9 = 2.0 V)		–	2.6	4.0	mA
Battery Saver Input Low (Pin 9 ≤ 0.8 V)		–	270	330	µA
Standby (After Power Down Input Strobe)		–	8.0	12	µA

NOTE: 2. All outputs are fully loaded as stated in the Electrical Characteristics Table above, except for the one under test.

Figure 1. Dropout Voltage versus Source Current

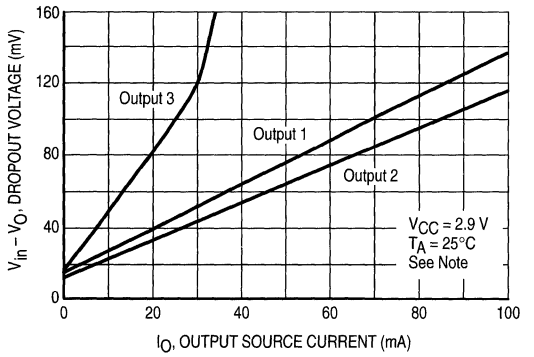


Figure 2. Output 4 Voltage versus Source Current

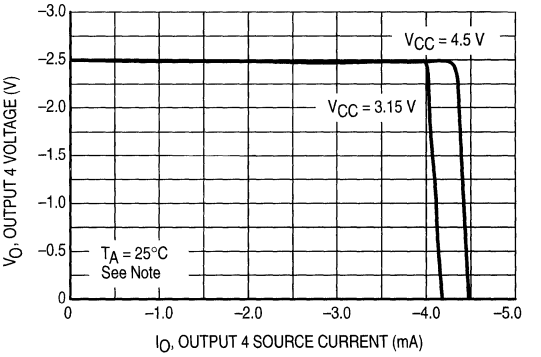


Figure 3. Reference Output Voltage Change versus Source Current

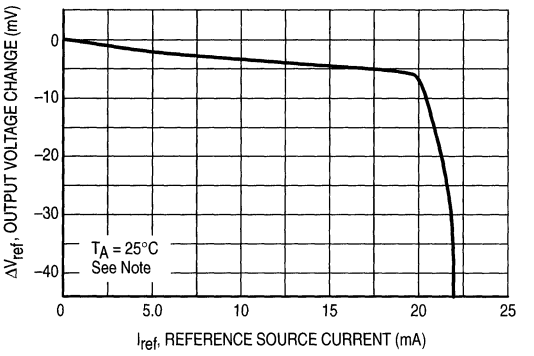
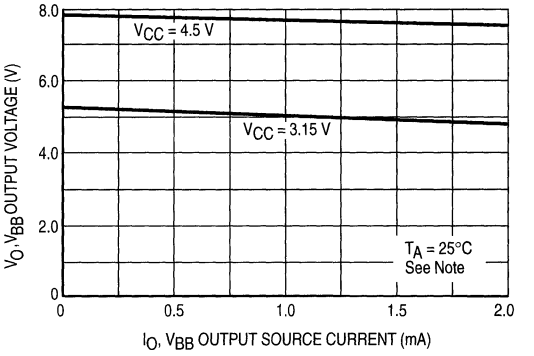


Figure 4. V_{BB} Output Voltage Change versus Source Current



NOTE: All outputs are fully loaded as stated in the Electrical Characteristics Table above, except for the one under test.

OPERATING DESCRIPTION

The MC33128 is a complete power management controller that is designed to interface the user to the system electronics via a microprocessor.

Outputs

Three low dropout voltage regulators are provided at outputs 1, 2 and 3. Outputs 1 and 2 were contemplated for independent powering of the systems analog and digital circuitry. This significantly reduces the possibility of digitally generated noise and spurious signals from coupling into the RF and analog circuits. The low dropout characteristic of Outputs 1 and 2 is achieved by applying a boosted battery voltage, V_{BB}, to their respective driver transistors. This allows the output pass transistors to be driven into saturation when the battery voltage approaches 3.0 V. The V_{BB} Output appears at Pin 4 and can be used to provide gate bias for enhancing external N channel MOSFET switches. Excessive loading of the V_{BB} output will result in an increase in dropout voltage.

Output 4 is derived from a voltage inverting charge pump circuit and is intended to provide the negative gate bias required for full depletion of RF gallium arsenide MESFETs. In personal communication system applications such as cellular telephone, negative gate bias is usually required by the antenna switch and power amplifier circuit blocks with a typical combined current of less than 1.0 mA. Output 4 can supply in excess of 2.0 mA, but there will be an increase in dropout voltage of Outputs 1, 2 and 3.

Outputs 1, 2, 4, V_{BB} Generator and Thermal Protection are all enabled and disabled in unison by the Battery Saver Input, Pin 9. The microprocessor can be programmed to significantly extend the system battery operating time by periodically enabling the receiver circuitry.

Output 3 provides power to the microprocessor, flash EPROM and the system display. These blocks are enabled by the Power Up Input, Pin 11, and disabled by the Power Down Input, Pin 10. By having separate power up and power down inputs, the microprocessor can store any pending information before turning the system and then itself OFF. This allows a controlled or graceful shutdown. Note that the power down request is initiated by pressing the toggle switch while the system is "ON". This action generates a microprocessor non–maskable interrupt that initiates the graceful shutdown.

Battery Voltage Detection

Reverse biasing and eventual failure of the lowest capacity cell in the battery pack can occur if the system is accidentally left on for an extended time period. To prevent this condition the following circuit blocks were incorporated.

A means for low battery detection is accomplished by using the Reference Output, Pin 12, in conjunction with the microprocessor's analog to digital converter input. A microprocessor output (LBO) can be designated to flash a display enunciator when a low battery condition exists. The Reference Output is 1.5 V ±2.7% and is capable of sourcing in excess of 10 mA.

The Power Up Reset Output, Pin 13, is designed to hold the microprocessor reset input low until the voltage at Output 3 rises above 2.66 V. This feature prevents the microprocessor from hanging or writing invalid information into its memory during power up. Notice that the output of the MPU Power Up Reset comparator also drives the base of transistor Q_{PD}. If Output 3 should fall below 2.6 V, due to an overload or a low battery condition, the comparator will drive Q_{PD} "ON", causing its collector to pull high on the Power Down Input, immediately forcing the system into standby mode. Externally pulling down on Pin 13, base of Q_{PD}, will also force the system into standby mode.

A redundant Low Battery Shutdown circuit is included. This circuit directly monitors the battery voltage and also forces the system into standby mode when the battery voltage falls below 2.4 V. To test the functionality of this circuit, the high state signal generated by transistor Q_{PD} must be clamped low, to prevent resetting the ON/OFF Latch. An external short or a pull–down, capable of sinking 2.0 mA at less than 0.8 V, must be connected to Pin 10.

A Battery Latch circuit is designed into the IC to prevent the system from turning on when the batteries are inserted into the finished product. This feature is useful for the end customer as well as the equipment manufacturer. Upon initial application of battery voltage, the lower comparator (0.7 V threshold) forces the Battery Latch into a reset state with its "Q" output low. This in turn triggers a reset of the ON/OFF Latch via the OR gate and also locks out the set signal present at the upper input of the AND gate. As the voltage at Pin 11 rises above (V_{CC} – 1.5 V), the set signal disappears, leaving the state of the ON/OFF Latch unchanged (reset). When the voltage at Pin 11 rises above (V_{CC} –1.0 V), the upper comparator forces the Battery Latch into a set state causing its "Q" output to go high. This allows the AND gate and the ON/OFF Latch to receive a set signal from Pin 11. The initial Battery Latch lockout time is controlled by the internal 20 kΩ resistor and the external 0.1 µF capacitor.

Figure 5. MC33128 Block Diagram

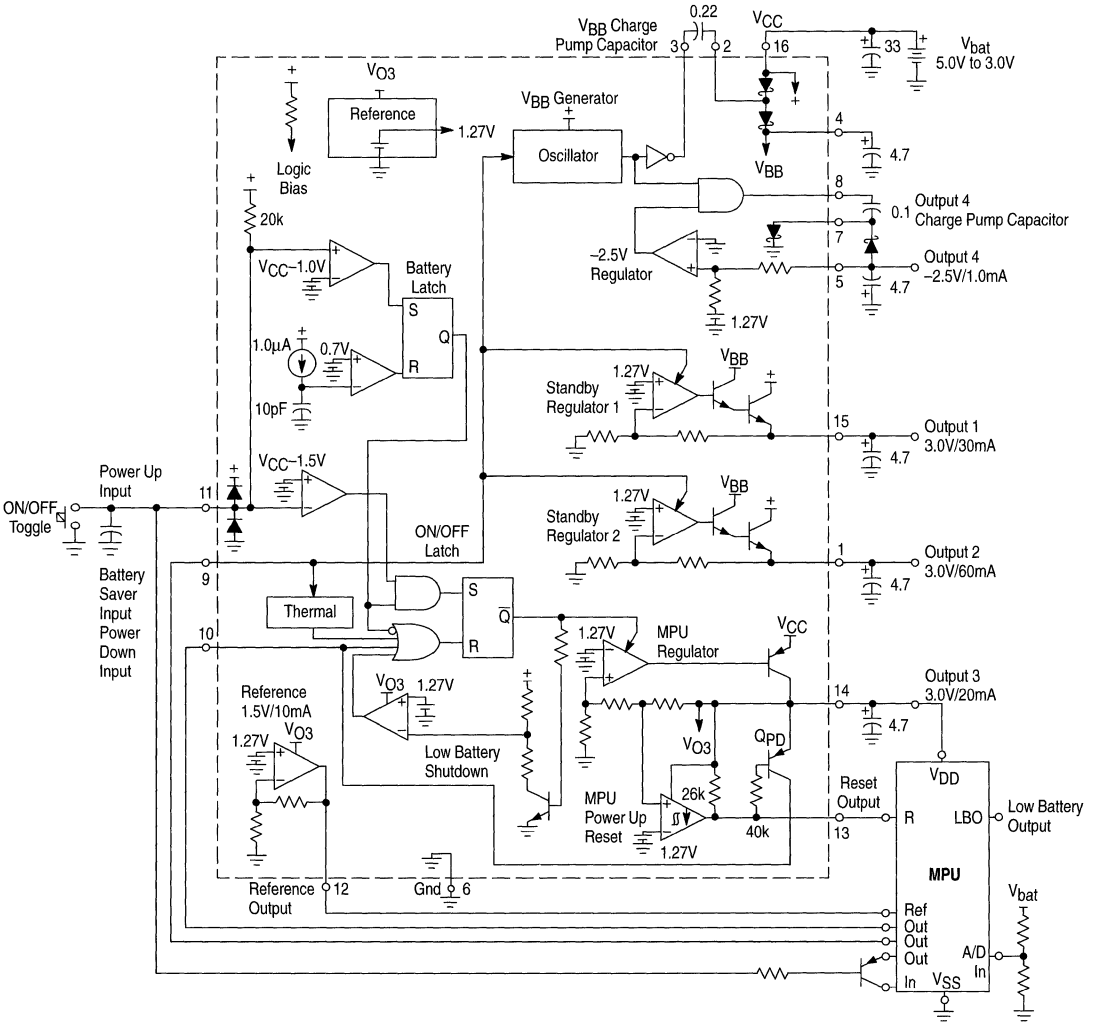
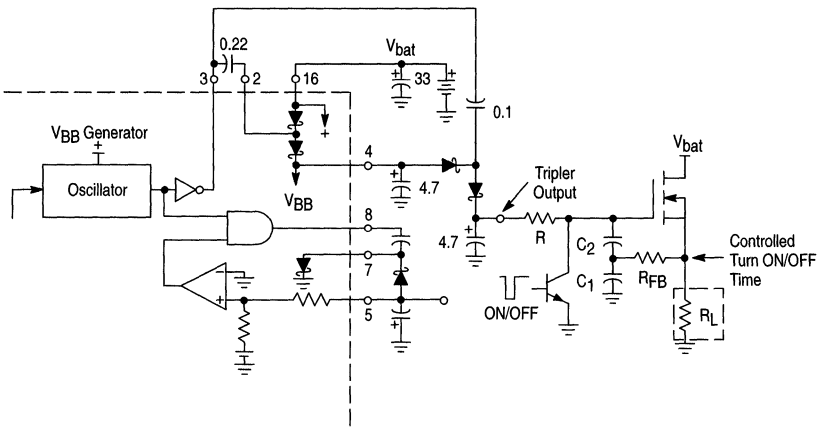


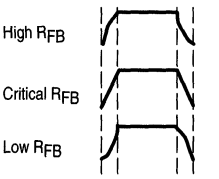
Figure 6. Voltage Tripler and Switch Driver



Tripler Output Voltage

Load Current (mA)	V_{CC} = 3.15 V	V_{CC} = 4.5 V
0	7.96	12.01
0.5	7.48	11.54
1.0	7.24	11.29
1.5	6.99	11.04
2.0	6.62	10.69

Load Turn ON/OFF Time



External Switch

A low threshold N–channel MOSFET can be used to switch the transmitting power amplifier (R_L) ON and OFF. To ensure that all of the available battery voltage appears across the load, the MOSFET must be fully enhanced over the system's required operating voltage range. With the addition of two Schottky diodes and two capacitors, the V_{BB} Generator can be made to function as a voltage tripler. The table in Figure 6 shows the output voltage characteristics of the tripler circuit.

In order to minimize adjacent channel splatter, the RF power amplifier must be turned ON and OFF in a controlled (soft) manner. The applied voltage rise and fall time, as well as the rate of change in rise and fall time, must be tailored to the amplifiers characteristics. The circuit consisting of resistors R, R_{FB}, and capacitors C_1 and C_2 is a simple solution allowing the system designer a means to control the ON and OFF time as well as the waveshape. Feedback resistor R_{FB} controls the waveshape. Capacitors C_1 and C_2 are usually of equal value.

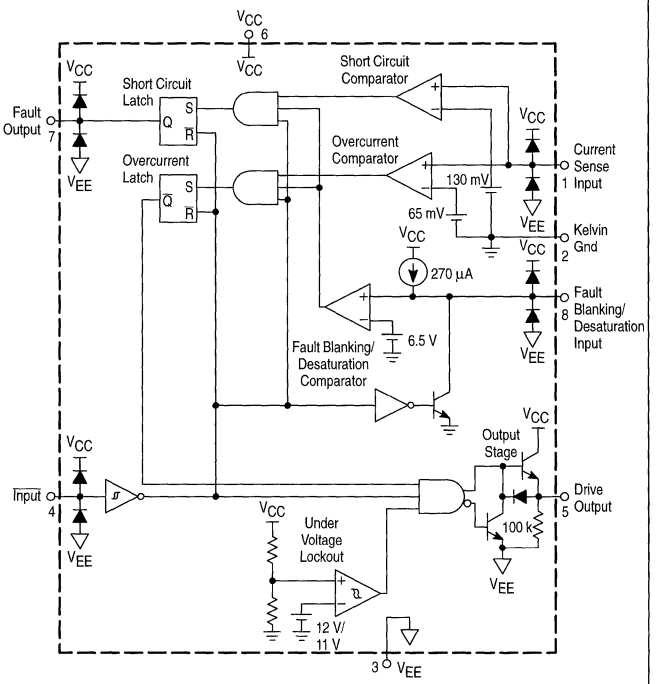
MOTOROLA

Single IGBT Gate Driver

The MC33153 is specifcally designed as an IGBT driver for high power applications that include ac induction motor control, brushless dc motor control and uninterruptable power supplies. Although designed for driving discrete and module IGBTs, this device offers a cost effective solution for driving power MOSFETs and Bipolar Transistors. Device protection features include the choice of desaturation or overcurrent sensing and undervoltage detection. These devices are available in dual–in–line and surface mount packages and include the following features:

- High Current Output Stage: 1.0 A Source/2.0 A Sink
- Protection Circuits for Both Conventional and Sense IGBT's
- Programmable Fault Blanking Time
- Protection against Overcurrent and Short Circuit
- Undervoltage Lockout Optimzed for IGBT's
- Negative Gate Drive Capability
- Cost Effectively Drives Power MOSFETs and Bipolar Transistors

Representative Block Diagram

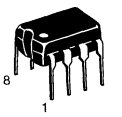


This device contains 133 active transistors.

MC33153

SINGLE IGBT GATE DRIVER

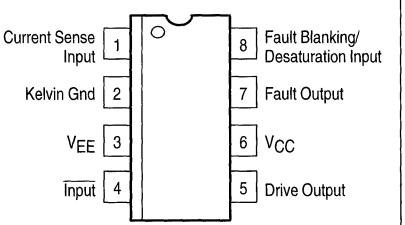
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33153D	T_A = –40° to +105°C	SO–8
MC33153P		DIP–8

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage			V
V_{CC} to V_{EE}	$V_{CC} - V_{EE}$	23	
Kelvin Ground to V_{EE} (Note 1)	$KGnd - V_{EE}$	23	
Logic Input	V_{in}	V_{EE} –0.3 to V_{CC}	V
Current Sense Input	V_S	–0.3 to V_{CC}	V
Blanking/Desaturation Input	V_{BD}	–0.3 to V_{CC}	V
Gate Drive Output	I_O		A
Source Current		1.0	
Sink Current		2.0	
Diode Clamp Current		1.0	
Fault Output	I_{FO}		mA
Source Current		25	
Sink Curent		10	
Power Dissipation and Thermal Characteristics			
D Suffix SO–8 Package, Case 751			
Maximum Power Dissipation @ T_A = 50°C	P_D	0.56	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	180	°C/W
P Suffix DIP–8 Package, Case 626			
Maximum Power Dissipation @ T_A = 50°C	P_D	1.0	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	–40 to +105	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = 0 V, Kelvin Gnd connected to V_{EE}. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUT					
Input Threshold Voltage					V
High State (Logic 1)	V_{IH}	–	2.70	3.2	
Low State (Logic 0)	V_{IL}	1.2	2.30	–	
Input Current					µA
High State (V_{IH} = 3.0 V)	I_{IH}	–	130	500	
Low State (V_{IL} = 1.2 V)	I_{IL}	–	50	100	
DRIVE OUTPUT					
Output Voltage					V
Low State (I_{Sink} = 1.0 A)	V_{OL}	–	2.0	2.5	
High State (I_{Source} = 500 mA)	V_{OH}	12	13.9	–	
Output Pull–Down Resistor	R_{PD}	–	100	200	kΩ
FAULT OUTPUT					
Output voltage					V
Low State (I_{Sink} = 5.0 mA)	V_{FL}	–	0.2	1.0	
High State (I_{Source} = 20 mA)	V_{FH}	12	13.3	–	
SWITCHING CHARACTERISTICS					
Propagation Delay (50% Input to 50% Output C_L = 1.0 nF)					ns
Logic Input to Drive Output Rise	$t_{PLH(in/out)}$	–	80	300	
Logic Input to Drive Output Fall	$t_{PHL(in/out)}$	–	120	300	
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF	t_r	–	17	55	ns
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF	t_f	–	17	55	ns
Propagation Delay					µs
Current Sense Input to Drive Output	$t_{P(OC)}$	–	0.3	1.0	
Fault Blanking/Desaturation Input to Drive Output	$t_{P(FLT)}$	–	0.3	1.0	

NOTE: 1. Kelvin Ground must always be between V_{EE} and V_{CC}.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
T_{low} = –40°C for MC33153 T_{high} = +105°C for MC33153

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V, V_{EE} = 0 V, Kelvin Gnd connected to V_{EE}. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
UVLO					
Startup Voltage	$V_{CC\ start}$	11.3	12	12.6	V
Disable Voltage	$V_{CC\ dis}$	10.4	11	11.7	V
COMPARATORS					
Overcurrent Threshold Voltage (V_{Pin8} > 7.0 V)	V_{SOC}	50	65	80	mV
Short Circuit Threshold Voltage (V_{Pin8} > 7.0 V)	V_{SSC}	100	130	160	mV
Fault Blanking/Desaturation Threshold (V_{Pin1} > 100 mV)	$V_{th(FLT)}$	6.0	6.5	7.0	V
Current Sense Input Current (V_{SI} = 0 V)	I_{SI}	–	–1.4	–10	µA
FAULT BLANKING/DESATURATION INPUT					
Current Source (V_{Pin8} = 0 V, V_{Pin4} = 0 V)	I_{chg}	–200	–270	–300	µA
Discharge Current (V_{Pin8} = 15 V, V_{Pin4} = 5.0 V)	I_{dschg}	1.0	2.5	–	mA
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Standby ($V_{Pin\ 4}$ = V_{CC}, Output Open)		–	7.2	14	
Operating (C_L = 1.0 nF, f = 20 kHz)		–	7.9	20	

NOTE: 1. Kelvin Ground must always be between V_{EE} and V_{CC}.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
T_{low} = –40°C for MC33153 T_{high} = +105°C for MC33153

Figure 1. Input Current versus Input Voltage

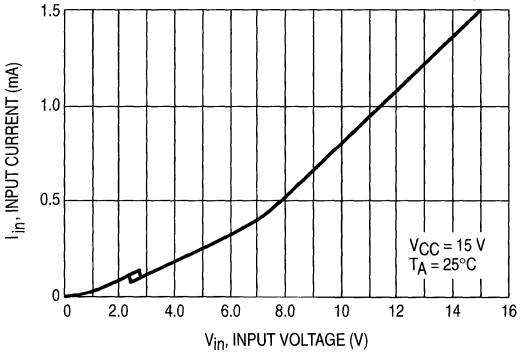


Figure 2. Output Voltage versus Input Voltage

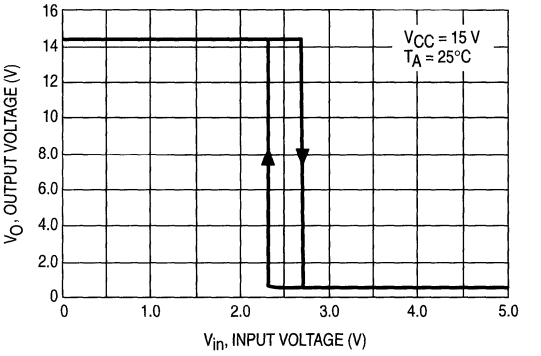


Figure 3. Input Threshold Voltage versus Temperature

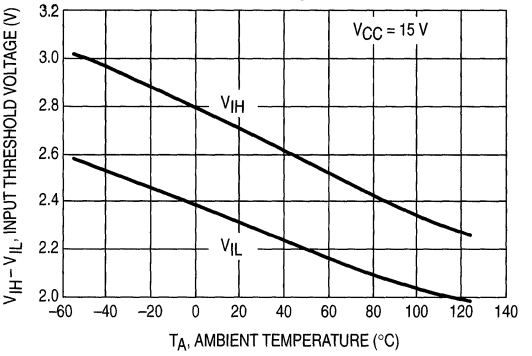


Figure 4. Input Threshold Voltage versus Supply Voltage

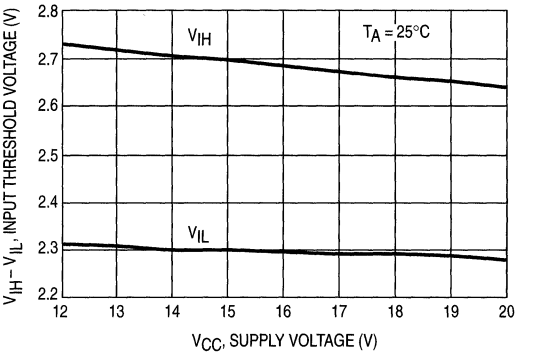


Figure 5. Drive Output Low State Voltage versus Temperature

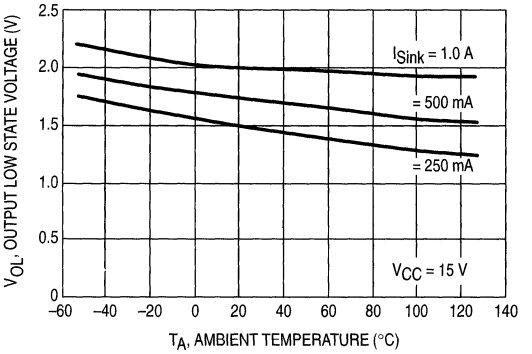


Figure 6. Drive Output Low State Voltage versus Sink Current

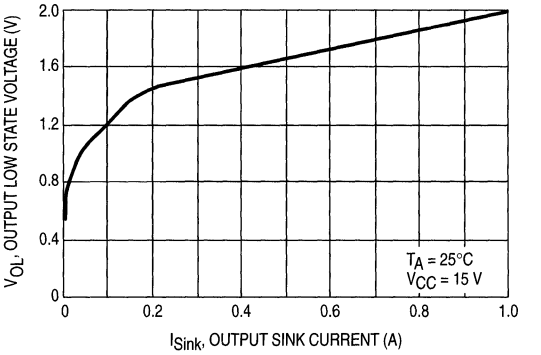


Figure 7. Drive Output High State Voltage versus Temperature

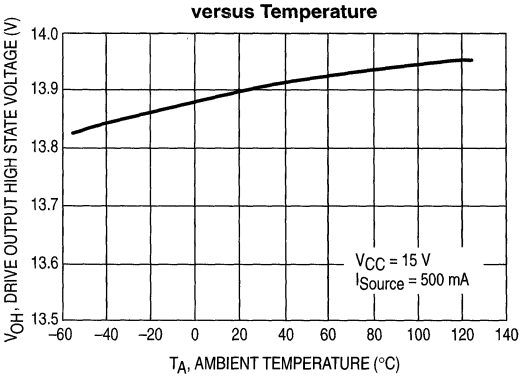


Figure 8. Drive Output High State Voltage versus Source Current

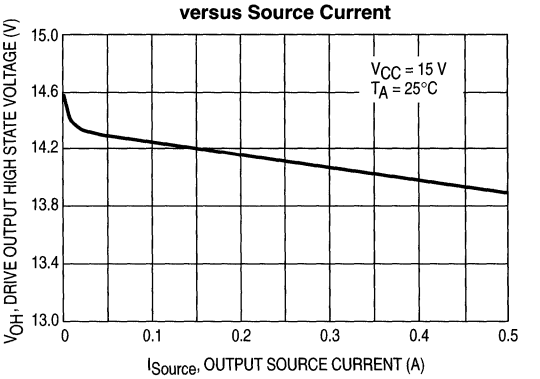


Figure 9. Drive Output Voltage versus Current Sense Input Voltage

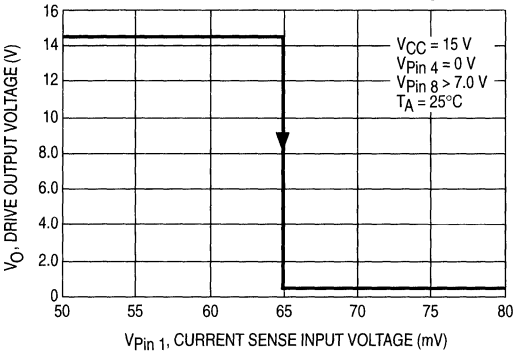


Figure 10. Fault Output Voltage versus Current Sense Input Voltage

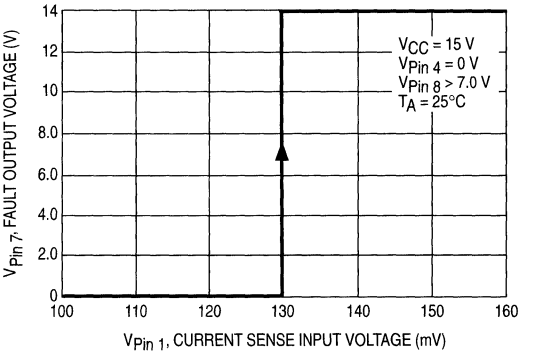


Figure 11. Overcurrent Protection Threshold Voltage versus Temperature

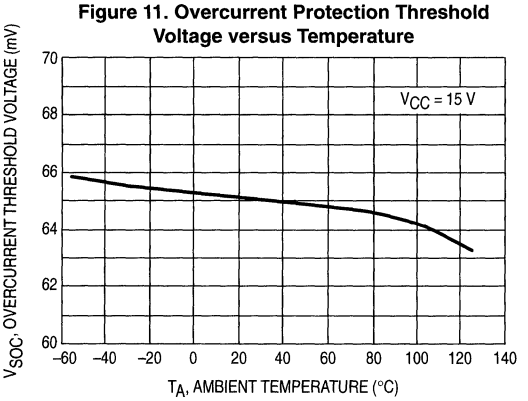


Figure 12. Overcurrent Protection Threshold Voltage versus Supply Voltage

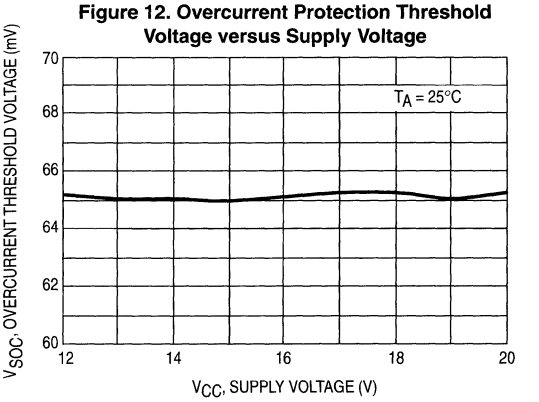


Figure 13. Short Circuit Comparator Threshold Voltage versus Temperature

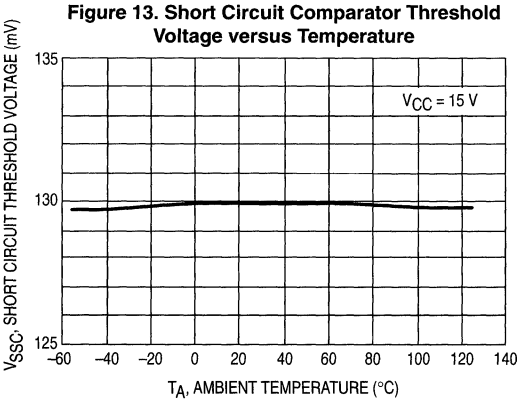


Figure 14. Short Circuit Comparator Threshold Voltage versus Supply Voltage

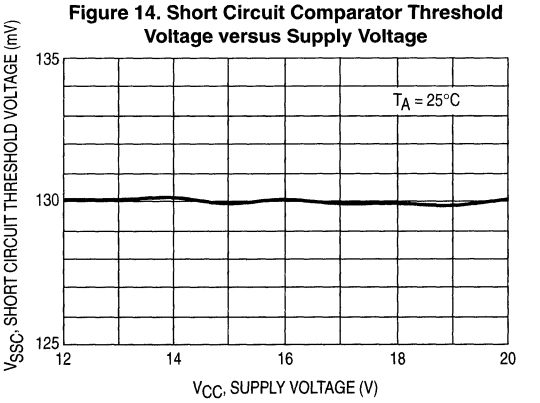


Figure 15. Current Sense Input Current versus Voltage

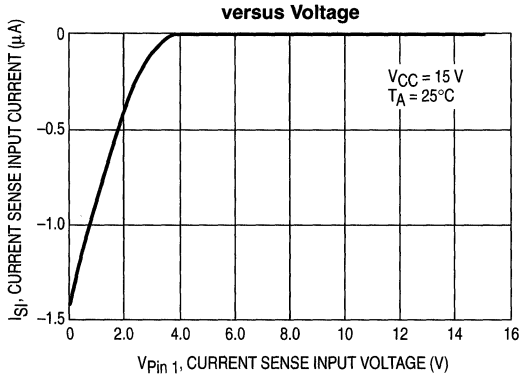


Figure 16. Drive Output Voltage versus Fault Blanking/Desaturation Input Voltage

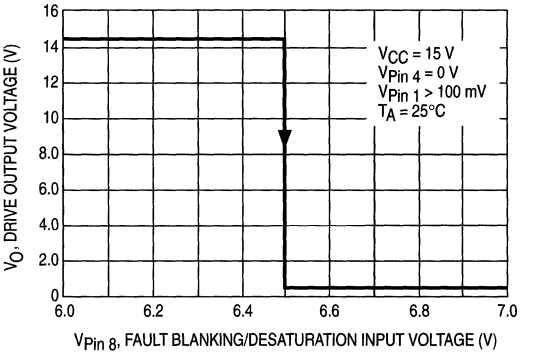


Figure 17. Fault Blanking/Desaturation Comparator Threshold Voltage versus Temperature

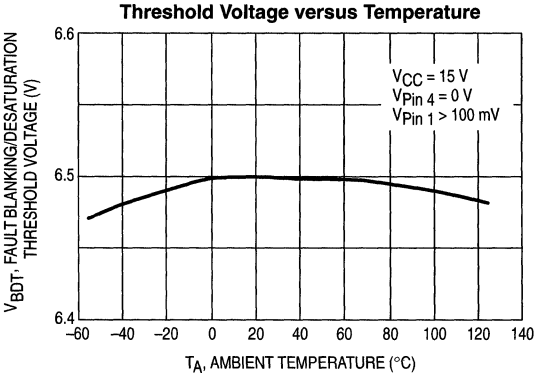


Figure 18. Fault Blanking/Desaturation Comparator Threshold Voltage versus Supply Voltage

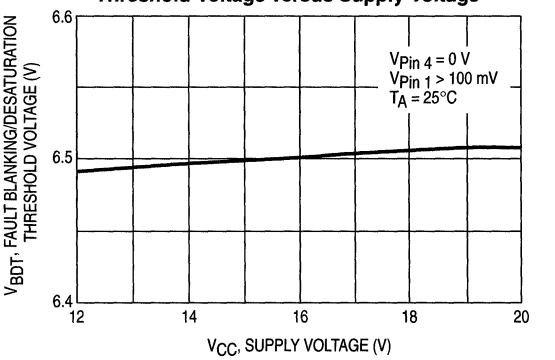


Figure 19. Fault Blanking/Desaturation Current Source versus Temperature

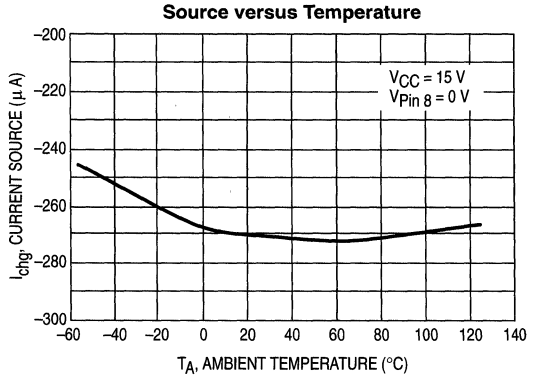


Figure 20. Fault Blanking/Desaturation Current Source versus Supply Voltage

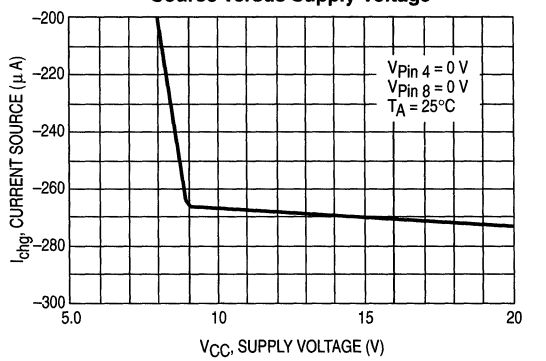


Figure 21. Fault Blanking/Desaturation Current Source versus Input Voltage

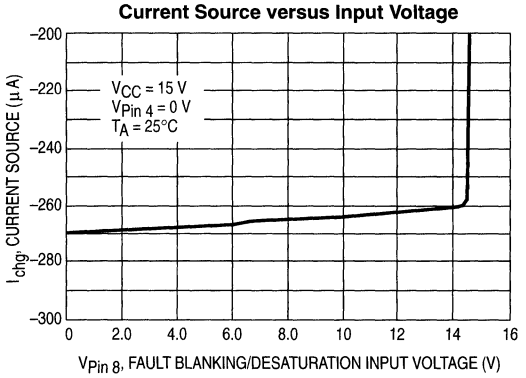


Figure 22. Fault Blanking/Desaturation Discharge Current versus Input Voltage

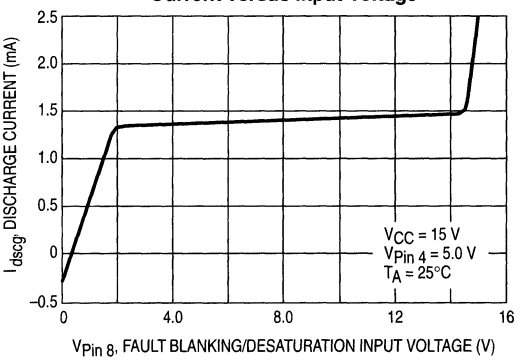


Figure 23. Fault Output Low State Voltage versus Sink Current

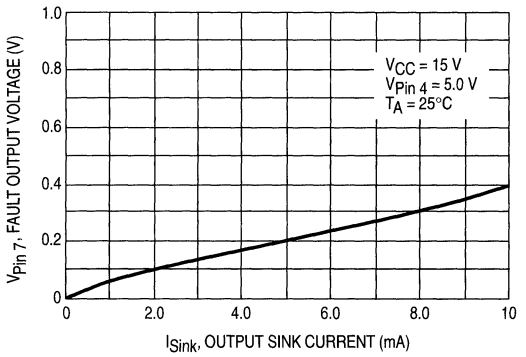


Figure 24. Fault Output High State Voltage versus Source Current

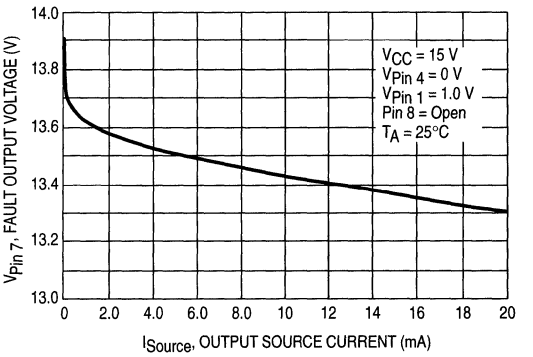


Figure 25. Drive Output Voltage versus Supply Voltage

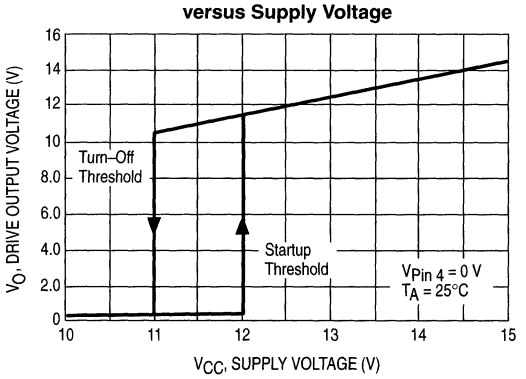


Figure 26. UVLO Thresholds versus Temperature

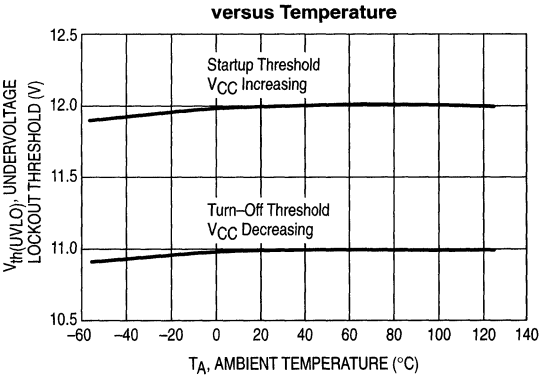


Figure 27. Supply Current versus Supply Voltage

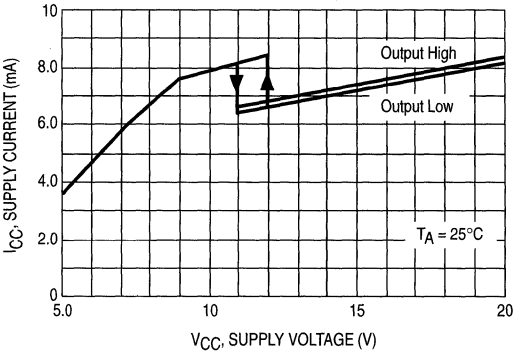


Figure 28. Supply Current versus Temperature

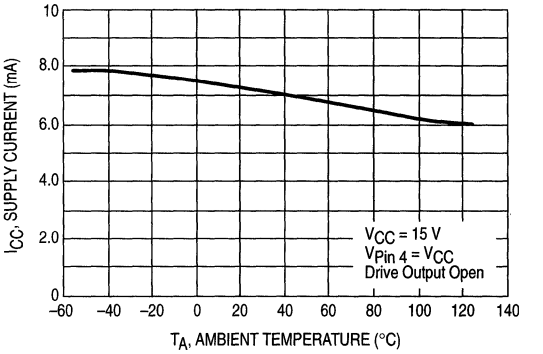
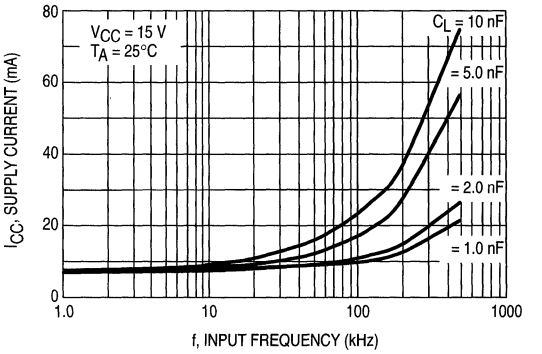


Figure 29. Supply Current versus Input Frequency



OPERATING DESCRIPTION

GATE DRIVE

Controlling Switching Times

The most important design aspect of an IGBT gate drive is optimization of the switching characteristics. The switching characteristics are especially important in motor control applications in which PWM transistors are used in a bridge configuration. In these applications, the gate drive circuit components should be selected to optimize turn–on, turn–off and off–state impedance. A single resistor may be used to control both turn–on and turn–off as shown in Figure 30. However, the resistor value selected must be a compromise in turn–on abruptness and turn–off losses. Using a single resistor is normally suitable only for very low frequency PWM. An optimized gate drive output stage is shown in Figure 31. This circuit allows turn–on and turn–off to be optimized separately. The turn–on resistor, R_{on}, provides control over the IGBT turn–on speed. In motor control circuits, the resistor sets the turn–on di/dt that controls how fast the free–wheel diode is cleared. The interaction of the IGBT and free–wheeling diode determines the turn–on dv/dt. Excessive turn–on dv/dt is a common problem in half–bridge circuits. The turn–off resistor, R_{off}, controls the turn–off speed and ensures that the IGBT remains off under commutation stresses. Turn–off is critical to obtain low switching losses. While IGBTs exhibit a fixed minimum loss due to minority carrier recombination, a slow gate drive will dominate the turn–off losses. This is particularly true for fast IGBTs. It is also possible to turn–off an IGBT too fast. Excessive turn–off speed will result in large overshoot voltages. Normally, the turn–off resistor is a small fraction of the turn–on resistor.

The MC33153 contains a bipolar totem pole output stage that is capable of sourcing 1.0 amp and sinking 2.0 amps peak. This output also contains a pull down resistor to ensure that the IGBT is off whenever there is insufficient V_{CC} to the MC33153.

In a PWM inverter, IGBTs are used in a half–bridge configuration. Thus, at least one device is always off. While the IGBT is in the off–state, it will be subjected to changes in voltage caused by the other devices. This is particularly a problem when the opposite transistor turns on.

When the lower device is turned on, clearing the upper diode, the turn–on dv/dt of the lower device appears across the collector emitter of the upper device. To eliminate shoot–through currents, it is necessary to provide a low sink impedance to the device that is in the off–state. In most applications the turn–off resistor can be made small enough to hold off the device that is under commutation without causing excessively fast turn–off speeds.

Figure 30. Using a Single Gate Resistor

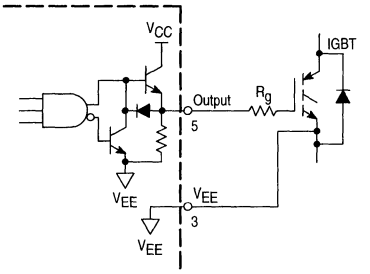
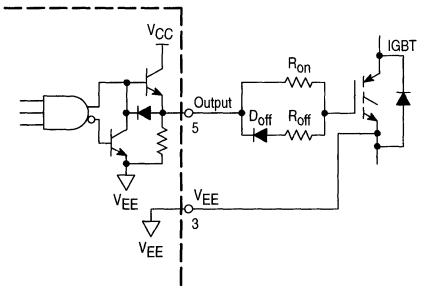


Figure 31. Using Separate Resistors for Turn–On and Turn–Off



A negative bias voltage can be used to drive the IGBT into the off–state. This is a practice carried over from bipolar Darlington drives and is generally not required for IGBTs. However, a negative bias will reduce the possibility of shoot–through. The MC33153 has separate pins for V_{EE} and Kelvin Ground. This permits operation using a +15/–5.0 V supply.

INTERFACING WITH OPTOISOLATORS

Isolated Input

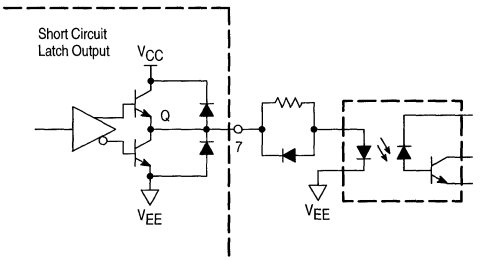
The MC33153 may be used with an optically isolated input. The optoisolator can be used to provide level shifting, and if desired, isolation from ac line voltages. An optoisolator with a very high dv/dt capability should be used, such as the Hewlett Packard HCPL4053. The IGBT gate turn–on resistor should be set large enough to ensure that the opto's dv/dt capability is not exceeded. Like most optoisolators, the HCPL4053 has an active low open–collector output. Thus, when the LED is on, the output will be low. The MC33153 has an inverting input pin to interface directly with an optoisolator using a pull up resistor. The input may also be interfaced directly to 5.0 V CMOS logic or a microcontroller.

Optoisolator Output Fault

The MC33153 has an active high fault output. The fault output may be easily interfaced to an optoisolator. While it is important that all faults are properly reported, it is equally important that no false signals are propagated. Again, a high dv/dt optoisolator should be used.

The LED drive provides a resistor programmable current of 10 to 20 mA when on, and provides a low impedance path when off. An active high output, resistor, and small signal diode provide an excellent LED driver. This circuit is shown in Figure 32.

Figure 32. Output Fault Optoisolator



UNDERVOLTAGE LOCKOUT

It is desirable to protect an IGBT from insufficient gate voltage. IGBTs require 15 V on the gate to achieve the rated on–voltage. At gate voltages below 13 V, the on–voltage increases dramatically, especially at higher currents. At very low gate voltages, below 10 V, the IGBT may operate in the linear region and quickly overheat. Many PWM motor drives use a bootstrap supply for the upper gate drive. The UVLO provides protection for the IGBT in case the bootstrap capacitor discharges.

The MC33153 will typically start up at about 12 V. The UVLO circuit has about 1.0 V of hysteresis and will disable the output if the supply voltage falls below about 11V.

PROTECTION CIRCUITRY

Desaturation Protection

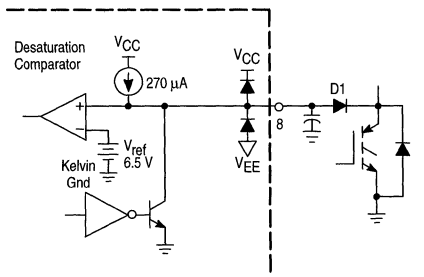
Bipolar Power circuits have commonly used what is known as "Desaturation Detection". This involves monitoring the collector voltage and turning off the device if this voltage rises above a certain limit. A bipolar transistor will only conduct a certain amount of current for a given base drive. When the base is overdriven, the device is in saturation. When the collector current rises above the knee, the device pulls out of saturation. The maximum current the device will conduct in the linear region is a function of the base current and the dc current gain (h_{FE}) of the transistor.

The output characteristics of an IGBT are similar to a Bipolar device. However, the output current is a function of gate voltage instead of current. The maximum current depends on the gate voltage and the device type. IGBTs tend to have a very high transconductance and a much higher current density under a short circuit than a bipolar device. Motor control IGBTs are designed for a lower current density under shorted conditions and a longer short circuit survival time.

The best method for detecting desaturation is the use of a high voltage clamp diode and a comparator. The MC33153 has a Fault Blanking/Desaturation Comparator which senses the collector voltage and provides an output indicating when the device is not fully saturated. Diode D1 is an external high voltage diode with a rated voltage comparable to the power device. When the IGBT is "on" and saturated, D1 will pull down the voltage on the Fault Blanking/Desaturation Input. When the IGBT pulls out of saturation or is "off", the current source will pull up the input and trip the comparator. The comparator threshold is 6.5 V, allowing a maximum on–voltage of about 5.8 V.

A fault exists when the gate input is high and V_{CE} is greater than the maximum allowable $V_{CE(sat)}$. The output of the Desaturation Comparator is ANDed with the gate input signal and fed into the Short Circuit and Overcurrent Latches. The Overcurrent Latch will turn–off the IGBT for the remainder of the cycle when a fault is detected. When input goes high, both latches are reset. The reference voltage is tied to the Kelvin Ground instead of the V_{EE} to make the threshold independent of negative gate bias. Note that for proper operation of the Desaturation Comparator and the Fault Output, the Current Sense Input must be biased above the Overcurrent and Short Circuit Comparator thresholds. This can be accomplished by connecting Pin 1 to V_{CC}.

Figure 33. Desaturation Detection



The MC33153 also features a programmable fault blanking time. During turn–on, the IGBT must clear the opposing free–wheeling diode. The collector voltage will remain high until the diode is cleared. Once the diode has been cleared, the voltage will come down quickly to the $V_{CE(sat)}$ of the device. Following turn–on, there is normally considerable ringing on the collector due to the C_{OSS} capacitance of the IGBTs and the parasitic wiring inductance. The fault signal from the Desaturation Comparator must be blanked sufficiently to allow the diode to be cleared and the ringing to settle out.

The blanking function uses an NPN transistor to clamp the comparator input when the gate input is low. When the input is switched high, the clamp transistor will turn "off", allowing the internal current source to charge the blanking capacitor. The time required for the blanking capacitor to charge up from the on–voltage of the internal NPN transistor to the trip voltage of the comparator is the blanking time.

If a short circuit occurs after the IGBT is turned on and saturated, the delay time will be the time required for the current source to charge up the blanking capacitor from the $V_{CE(sat)}$ level of the IGBT to the trip voltage of the comparator. Fault blanking can be disabled by leaving Pin 8 unconnected.

Sense IGBT Protection

Another approach to protecting the IGBTs is to sense the emitter current using a current shunt or Sense IGBTs. This method has the advantage of being able to use high gain IGBTs which do not have any inherent short circuit capability. Current sense IGBTs work as well as current sense MOSFETs in most circumstances. However, the basic problem of working with very low sense voltages still exists. Sense IGBTs sense current through the channel and are therefore linear with respect to the collector current. Because IGBTs have a very low incremental on–resistance, sense IGBTs behave much like low–on resistance current sense MOSFETs. The output voltage of a properly terminated sense IGBT is very low, normally less than 100 mV.

The sense IGBT approach requires fault blanking to prevent false tripping during turn–on. The sense IGBT also requires that the sense signal is ignored while the gate is low. This is because the mirror output normally produces large transient voltages during both turn–on and turn–off due to the collector to mirror capacitance. With non–sensing types of IGBTs, a low resistance current shunt (5.0 to 50 mΩ) can be used to sense the emitter current. When the output is an actual short circuit, the inductance will be very low. Since the blanking circuit provides a fixed minimum on–time, the peak current under a short circuit can be very high. A short circuit discern function is implemented by the second comparator which has a higher trip voltage. The short circuit signal is latched and appears at the Fault Output. When a short circuit is detected, the IGBT should be turned–off for several milliseconds allowing it to cool down before it is turned back on. The sense circuit is very similar to the desaturation circuit. It is possible to build a combination circuit that provides protection for both Short Circuit capable IGBTs and Sense IGBTs.

APPLICATION INFORMATION

Figure 34 shows a basic IGBT driver application. When driven from an optoisolator, an input pull up resistor is required. This resistor value should be set to bias the output transistor at the desired current. A decoupling capacitor should be placed close to the IC to minimize switching noise.

A bootstrap diode may be used for a floating supply. If the protection features are not required, then both the Fault Blanking/Desaturation and Current Sense Inputs should both be connected to the Kelvin Ground (Pin 2). When used with a single supply, the Kelvin Ground and V_{EE} pins should be connected together. Separate gate resistors are recommended to optimize the turn–on and turn–off drive.

Figure 34. Basic Application

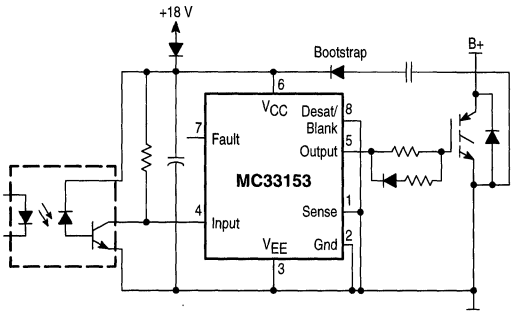
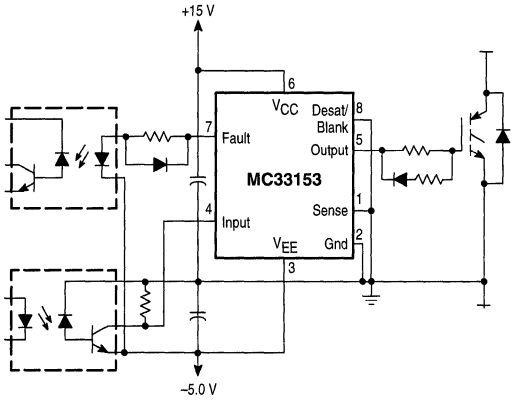


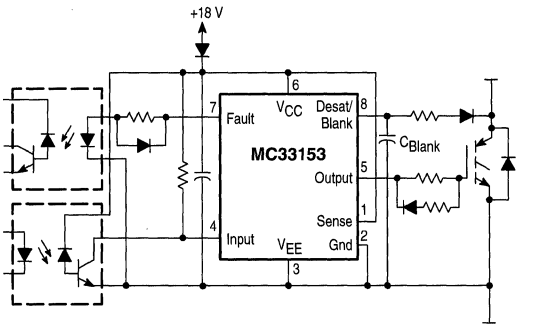
Figure 35. Dual Supply Application



When used in a dual supply application as in Figure 35, the Kelvin Ground should be connected to the emitter of the IGBT. If the protection features are not used, then both the Fault Blanking/Desaturation and the Current Sense Inputs should be connected to Ground. The input optoisolator should always be referenced to V_{EE}.

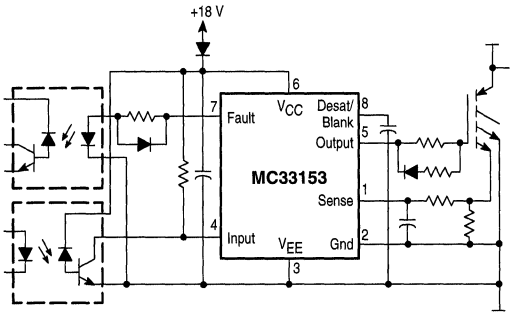
If desaturation protection is desired, a high voltage diode is connected to the Fault Blanking/Desaturation pin. The blanking capacitor should be connected from the Desaturation pin to the V_{EE} pin. If a dual supply is used, the blanking capacitor should be connected to the Kelvin Ground. The Current Sense Input should be tied high because the two comparator outputs are ANDed together. Although the reverse voltage on collector of the IGBT is clamped to the emitter by the free–wheeling diode, there is normally considerable inductance within the package itself. A small resistor in series with the diode can be used to protect the IC from reverse voltage transients.

Figure 36. Desaturation Application



When using sense IGBTs or a sense resistor, the sense voltage is applied to the Current Sense Input. The sense trip voltages are referenced to the Kelvin Ground pin. The sense voltage is very small, typically about 65 mV, and sensitive to noise. Therefore, the sense and ground return conductors should be routed as a differential pair. An RC filter is useful in filtering any high frequency noise. A blanking capacitor is connected from the blanking pin to V_{EE}. The stray capacitance on the blanking pin provides a very small level of blanking if left open. The blanking pin should not be grounded when using current sensing, that would disable the sense. The blanking pin should never be tied high, that would short out the clamp transistor.

Figure 37. Sense IGBT Application



MOTOROLA

MC33154

Product Preview

Single IGBT Gate Driver

3

The MC33154 is specifically designed as an IGBT driver for high power applications including ac induction motor control, brushless dc motor control and uninterruptible power supplies.

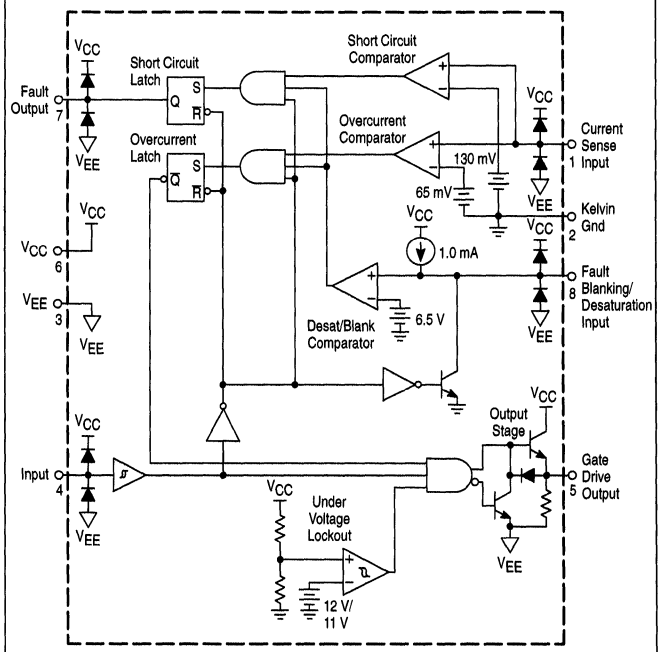
The MC33154 is similar to the MC33153, except that the output drive is in–phase with the logic input, the output source current drive is four times higher and the supply voltage rating is higher.

Although designed for driving discrete and module IGBTs, this device offers a cost effective solution for driving power MOSFETs and Bipolar Transistors.

These devices are available in dual–in–line and surface mount packages and include the following features:

- High Current Output Stage: 4.0 A Source/2.0 A Sink
- Protection Circuits for Both Conventional and Sense IGBTs
- Programmable Fault Blanking Time
- Protection against Overcurrent and Short Circuit
- Undervoltage Lockout Optimzed for IGBTs
- Negative Gate Drive Capability
- Cost Effectively Drives Power MOSFETs and Bipolar Transistors

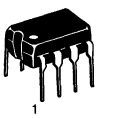
Representative Block Diagram



This device contains 133 active transistors.

SINGLE IGBT GATE DRIVER

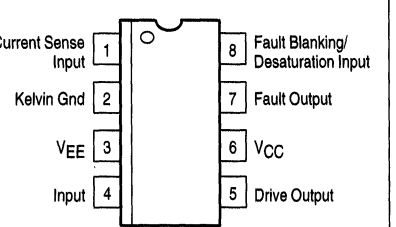
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33154D	T_A = –40° to +85°C	SO–8
MC33154P		DIP–8

MOTOROLA

MC33169

Advance Information

GaAs Power Amplifier Support IC

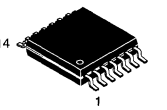
The MC33169 is a support IC for GaAs Power Amplifier Enhanced FETs used in hand portable telephones such as GSM, PCN and DECT. This device provides negative voltages for full depletion of Enhanced MESFETs as well as a priority management system of drain switching, ensuring that the negative voltage is always present before turning "on" the Power Amplifier. Additional features include an idle mode input and a direct drive of the N–Channel drain switch transistor.

This product is available in two versions, –2.5 and –4.0 V. The –4.0 V version is intended for supplying RF modules for GSM and DCS1800 applications, whereas the –2.5 V version is dedicated for DECT and PHS systems.

- Negative Regulated Output for Full Depletion of GaAs MESFETs
- Drain Switch Priority Management Circuit
- CMOS Compatible Inputs
- Idle Mode Input (Standby Mode) for Very Low Current Consumption
- Output Signal Directly Drives N–Channel FET
- Low Startup and Operating Current

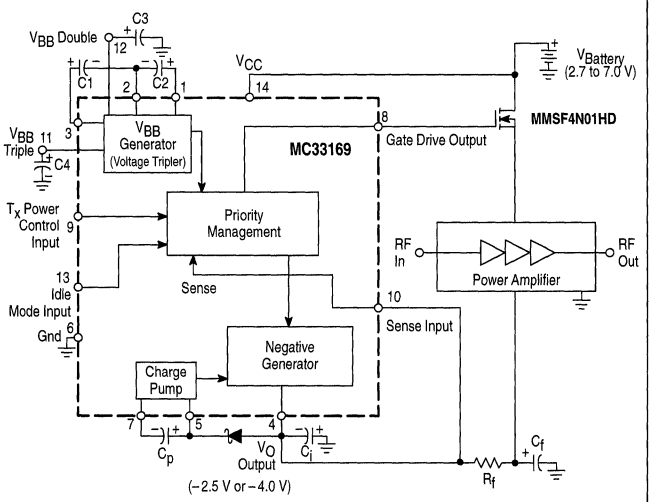
GaAs POWER AMPLIFIER SUPPORT IC

SEMICONDUCTOR TECHNICAL DATA



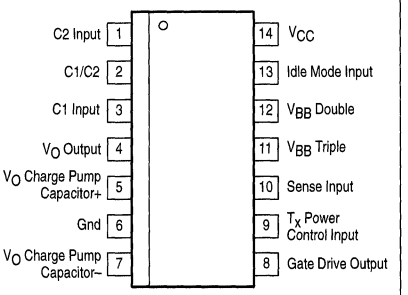
DTB SUFFIX
PLASTIC PACKAGE
CASE 948G
(TSSOP–14)

Simplified Block Diagram



This device contains 148 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33169DTB–4.0	T_A = –40° to +85°C	TSSOP–14
MC33169DTB–2.5		

3

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	14	V_{CC}	9.5	V
T_X Power Control Input	9	VT_X	V_{CC}	V
Idle Mode Input	13	V_i	V_{CC}	V
Sense Input	10	V_{Sense}	–5.0 to 0	V
Negative Generator Output Source Current	4	I_{SS}	20	mA
Charge Pump Capacitor Current	–	I_{max}	60	mA
Diode Forward Current	–	I_{Fmax}	60	mA
Gate Drive Output Current	8	I_{GO}	5.0	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air Operating Junction Temperature	–	 P_D $R_{\theta JA}$ T_J	 417 240 +150	 mW °C/W °C
Operating Ambient Temperature	–	T_A	–40 to +85	°C
Storage Temperature Range	–	T_{stg}	–60 to +150	°C

NOTE: ESD data available upon request.

MC33169–4.0

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.8 V. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
V_{BB} GENERATOR (VOLTAGE TRIPLER)						
Oscillator Frequency	–	f_{osc}	90	100	110	kHz
Oscillator Duty Cycle	–	DC	35	50	65	%
Output Voltage (V_{CC} = 3.0 V, I_O = 3.0 mA) Double Voltage Triple Voltage Triple Voltage (V_{CC} = 7.2 V, I_O = 3.0 mA)	 12 11 11	 V_{BBD} V_{BBT} V_{BBT}	 4.6 6.1 –	 5.0 7.0 11.2	 – – –	V
NEGATIVE GENERATOR OUTPUT						
Output Voltage (I_O = 3.0 mA)	4	V_O	–3.75	–4.0	–4.25	V
Output Voltage Ripple with Filter (R_f = 33 Ω, C_f = 4.7 μF) (I_O = 0 to 5.0 mA)	4	V_r	 –	 2.0	 –	mVpp
PRIORITY MANAGEMENT SECTION						
Idle Mode Input Input Voltage High State (Logic 1) Input Voltage Low State (Logic 0) Input Current High State (Logic 1) Input Current Low State (Logic 0), i.e. Standby Mode	13	 V_{IH} V_{IL} I_{IH} I_{IL}	 2.0 0 10 –	 – – – –	 2.7 0.5 80 1.0	 V V μA μA
T_X Power Control Input Input Voltage Range Input Voltage "Off" State (Zero RF Output Level) Input Voltage "On" State (Maximum RF Output Level) Input Resistance Bandwidth (–3.0 dB)	9	 VT_X $VT_{X(off)}$ $VT_{X(on)}$ R_{in} B	 0 – – – –	 – 0.7 2.7 90 1.0	 3.1 – – – –	 V V V kΩ MHz
Gate Drive Output Voltage (VT_X = 0 V) (VT_X = 3.0 V) Peak Current (Source and Sink) (VT_X = 3.0 V)	8	 V_{GO} I_{GO}	 – V_{CC}+2.7 –	 – – 3.0	 0.5 – –	 V mA
Undervoltage Lockout Voltage on Sense Input (Magnitude)	10	V_{sense}	–3.0	–3.2	–	V

MC33169–4.0

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 4.8 V. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
TOTAL DEVICE POWER CONSUMPTION						
I_{CC} Operating (VT_X = 3.0 V, I_O = 3.0 mA)	–	I_{CC}	–	10	15	mA
I_{CC} Operating	–	I_{CC}				mA
(VT_X = 0 V, I_O = 3.0 mA)			–	12	15	
(VT_X = 0 V, I_O = 0 mA)			–	4.0	5.0	
Standby Mode (Idle Mode Input = 0 V)	–	I_{CC}	–	–	1.0	µA

MC33169–4.0

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
V_{BB} GENERATOR (VOLTAGE TRIPLER)						
Oscillator Frequency	–	f_{osc}	90	100	110	kHz
Oscillator Duty Cycle	–	DC	35	50	65	%
Output Voltage (V_{CC} = 3.0 V, I_O = 3.0 mA)						V
Double Voltage	12	V_{BBD}	4.6	5.0	–	
Triple Voltage	11	V_{BBT}	6.1	7.0	–	
Triple Voltage (V_{CC} = 7.2 V, I_O = 3.0 mA)	11	V_{BBT}	–	11.2	–	
NEGATIVE GENERATOR OUTPUT						
Output Voltage (I_O = 1.0 mA)	4	V_O	−3.75	−4.0	−4.25	V
Output Voltage Ripple with Filter (R_f = 33 Ω, C_f = 4.7 µF) (I_O = 0 to 5.0 mA)	4	V_r	–	2.0	–	mVpp
PRIORITY MANAGEMENT SECTION						
Idle Mode Input	13					
Input Voltage High State (Logic 1)		V_{IH}	2.0	–	2.7	V
Input Voltage Low State (Logic 0)		V_{IL}	0	–	0.5	V
Input Current High State (Logic 1)		I_{IH}	10	–	80	µA
Input Current Low State (Logic 0), i.e. Standby Mode		I_{IL}	–	–	1.0	µA
T_X Power Control Input	9					
Input Voltage Range		VT_X	0	–	3.0	V
Input Voltage "Off" State (Zero RF Output Level)		$VT_{X(off)}$	–	0.7	–	V
Input Voltage "On" State (Maximum RF Output Level)		$VT_{X(on)}$	–	2.7	–	V
Input Resistance		R_{in}	–	90	–	kΩ
Bandwidth (−3.0 dB)		B	–	1.0	–	MHz
Gate Drive Output	8					
Voltage (VT_X = 0 V)		V_{GO}	–	–	0.5	V
(VT_X = 3.0 V)			V_{CC}+2.7	–	–	
Peak Current (Source and Sink) (VT_X = 3.0 V)		I_{GO}	–	3.0	–	mA
Undervoltage Lockout Voltage on Sense Input (Magnitude)	10	V_{sense}	−3.0	−3.2	–	V
TOTAL DEVICE POWER CONSUMPTION						
I_{CC} Operating (VT_X = 3.0 V)	14	I_{CC}				mA
(I_O = 3.0 mA)			–	–	15	
(I_O = 1.0 mA)			–	–	9.0	
I_{CC} Operating (VT_X = 0 V)	14	I_{CC}				mA
(I_O = 3.0 mA)			–	–	13	
(I_O = 1.0 mA)			–	–	9.0	
(I_O = 0 mA)			–	4.5	6.0	
Standby Mode (Idle Mode Input = 0 V)	14	I_{CC}	–	–	1.0	µA

MC33169–2.5

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.8 V. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
V_{BB} GENERATOR (VOLTAGE TRIPLER)						
Oscillator Frequency	–	f_{osc}	90	100	110	kHz
Oscillator Duty Cycle	–	DC	35	50	65	%
Output Voltage (V_{CC} = 3.0 V, I_O = 3.0 mA)						V
Double Voltage	12	V_{BBD}	4.6	5.0	–	
Triple Voltage	11	V_{BBT}	6.1	7.0	–	
Triple Voltage (V_{CC} = 7.2 V, I_O = 3.0 mA)	11	V_{BBT}	–	11.2	–	
NEGATIVE GENERATOR OUTPUT						
Output Voltage	4	V_O				V
(I_O = 3.0 mA)			−2.35	−2.5	−2.65	
(I_O = 5.0 mA, V_{CC} = 6.0 V)			–	−2.5	–	
Output Voltage Ripple with Filter (R_f = 33 Ω, C_f = 4.7 μF)	4	V_r				mVpp
(I_O = 0 to 5.0 mA)			–	2.0	8.0	
PRIORITY MANAGEMENT SECTION						
Idle Mode Input	13					
Input Voltage High State (Logic 1)		V_{IH}	2.0	–	2.7	V
Input Voltage Low State (Logic 0)		V_{IL}	0	–	0.5	V
Input Current High State (Logic 1)		I_{IH}	10	–	80	μA
Input Current Low State (Logic 0), i.e. Standby Mode		I_{IL}	–	–	1.0	μA
T_X Power Control Input	9					
Input Voltage Range		VT_X	0	–	3.0	V
Input Voltage "Off" State (Zero RF Output Level)		$VT_{X(off)}$	–	0.7	–	V
Input Voltage "On" State (Maximum RF Output Level)		$VT_{X(on)}$	–	2.7	–	V
Input Resistance		R_{in}	–	90	–	kΩ
Bandwidth (–3.0 dB)		B	–	1.0	–	MHz
Gate Drive Output	8					
Voltage (VT_X = 0 V)		V_{GO}	–	–	0.5	V
(VT_X = 3.0 V)			V_{CC}+2.7	–	–	
Peak Current (VT_X = 3.0 V)		I_{GO}	–	3.0	–	mA
Undervoltage Lockout Voltage on Sense Input (Magnitude)	10	V_{sense}	–2.0	–2.3	–	V
TOTAL DEVICE POWER CONSUMPTION						
I_{CC} Operating (VT_X = 3.0 V, I_O = 3.0 mA)	14	I_{CC}	–	14	17	mA
I_{CC} Operating	14	I_{CC}				mA
(VT_X = 0 V, I_O = 3.0 mA)			–	13.5	16	
(VT_X = 0 V, I_O = 0 mA)			–	4.5	6.0	
Standby Mode (Idle Mode Input = 0 V)	14	I_{CC}	–	–	1.0	μA

PRIORITY MANAGEMENT TRUTH TABLE

Control Inputs		Outputs	
Idle Mode	T_X Power Control	V_O	Gate Drive
0	0	Off	0.5 V max
1	0	–2.5 or –4.0 V	0.5 V max
0	1	Off	0.5 V max
1	1	–2.5 or –4.0 V	V_{CC} + 2.7 V min

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	C2 Input	This is the positive pin for the charge pump capacitor in the voltage doubler.
2	C1/C2	This is the negative pin for the charge pump capacitors.
3	C1 Input	This is the positive pin for the charge pump capacitor in the voltage tripler.
4	V_O Output	It delivers a regulated negative voltage of –4.0 V or –2.5 V depending on the product version. It can source an output current in excess of 5.0 mA.
5	V_O Charge Pump Capacitor +	This is the positive pin for the capacitor in the inverting charge pump.
6	Gnd	This pin is Ground for both signal and power circuitry.
7	V_O Charge Pump Capacitor –	This is the negative pin for the capacitor in the inverting charge pump.
8	Gate Drive Output	This is the output of the gate amplifier which directly drives the gate of an N–Channel MOSFET. It can sink and source peak currents up to 3.0 mA.
9	T_X Power Control Input	The input signal applied on this pin controls the N–Channel switching MOSFET in follower mode and therefore, linearly controls the RF output voltage.
10	Sense Input Pin	It senses the negative voltage directly on the Power Amplifier. It is also the input pin of an internal Undervoltage Lockout circuit which blocks the switching of the N–Channel MOSFET if the sensed voltage is more positive than –3.0 V (–4.0 V version) or –2.0 V (–2.5 V version).
11	V_{BB} Triple	This is the positive pin of the output filter capacitor in the voltage tripler. The triple voltage at that pin is used internally to supply the inverting charge pump and the gate amplifier.
12	V_{BB} Double	This is the positive pin of the output filter capacitor in the voltage doubler.
13	Idle Mode Input	This pin is used to set the circuit in Low Power Consumption Standby mode. It is CMOS compatible, i.e. a voltage lower than 0.5 V applied on this pin makes the device go into Standby mode in which the current consumption is lower than 1.0 µA. The MC33169 is then awakened by a voltage higher than 2.0 V applied on that pin.
14	V_{CC}	This is the supply input pin for the MC33169, V_{CC} voltage ranges from 2.7 V to 7.2 V.

Figure 1. MC33169 Representative Block Diagram

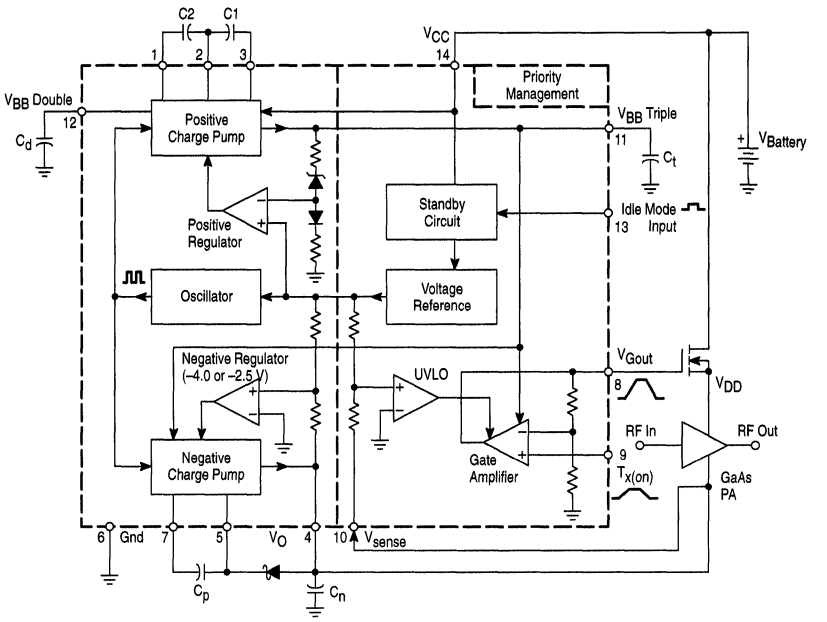


Figure 2. Operating Current versus Temperature

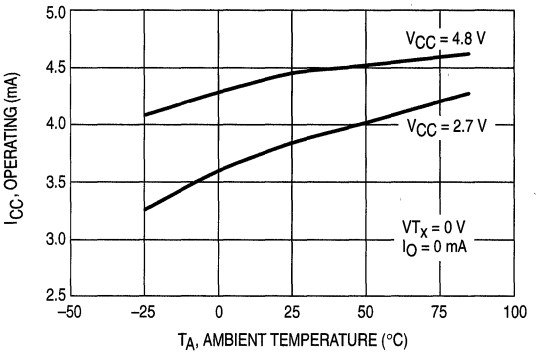


Figure 3. Operating Current versus Temperature

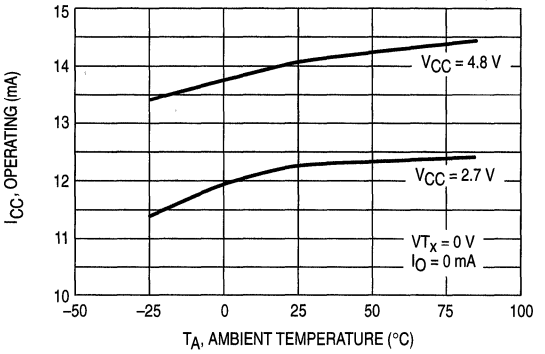


Figure 4. Operating Current versus Temperature

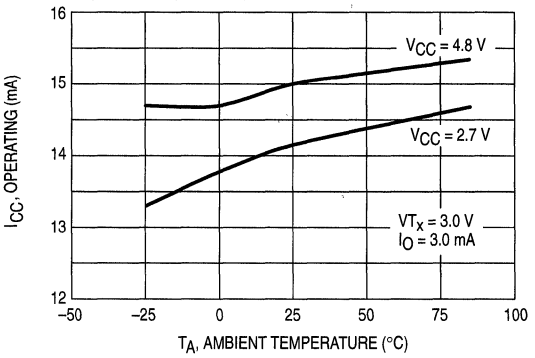


Figure 5. Operating Current versus Temperature

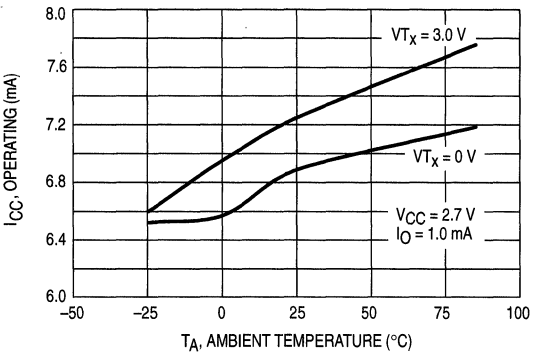


Figure 6. Output Voltage versus Temperature

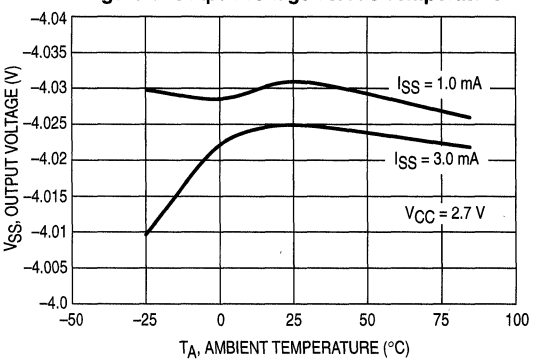


Figure 7. Output Voltage versus Temperature

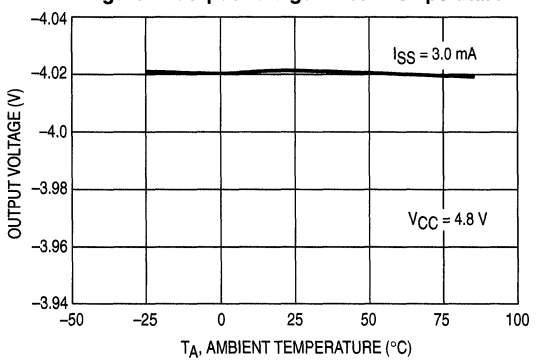


Figure 8. Output Voltage versus Load Current

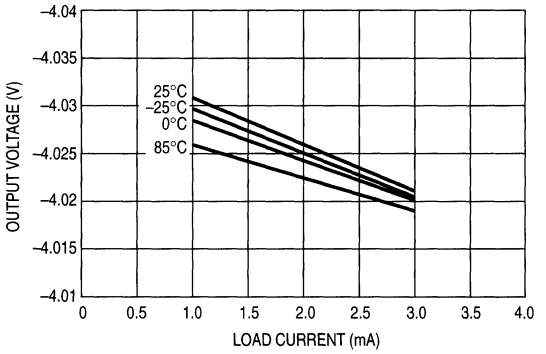
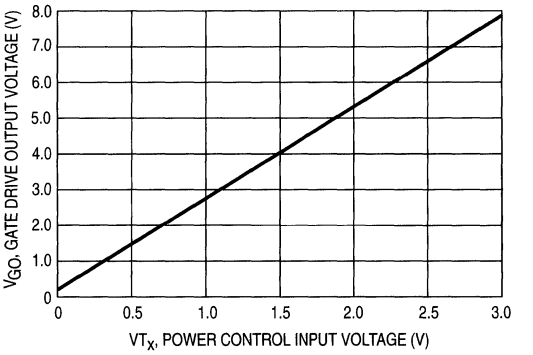


Figure 9. VT_X Control Voltage versus Gate Drive Output Voltage



3

OPERATING DESCRIPTION

The MC33169 is a power amplifier support IC that is designed to properly switch "on" or "off" a MESFET Power Amplifier either manually or by microprocessor. Controlling the power drain of the RF Amplifier extends operating battery life in many portable systems.

Outputs

The IC is designed to provide a −4.0 V or −2.5 V bias to the gate of the RF Amplifier MESFET devices prior to application of a positive battery voltage to the drain. The negative output voltage can provide up to 5.0 mA of current. The positive voltage control requires an external N−Channel logic level MOSFET, connected as a source follower. The Gate Drive Output, Pin 8, can source or sink 3.0 mA to the external MOSFET. The low drive current slows the MOSFET switching speed, thereby minimizing voltage glitches on the V_{CC} line which could cause disturbances to other circuitry.

Inputs

A Sense Input, Pin 10, protects the Power Amplifier load by monitoring the level of the negative output voltage. If the negative voltage magnitude falls below a preset level, 3.2 V typical for the −4.0 V version or 2.3 V for the −2.5 V version, an undervoltage lockout circuit disables the external MOSFET gate drive.

The T_X Power Control Input controls the N−Channel external switching MOSFET in source follower mode, which allows linear control of the RF Output voltage level.

The Idle mode input is CMOS compatible, allowing the RF Amplifier to be placed in a standby mode, drawing less than 1.0 μA from the power source.

3

Figure 10. Class 4 GSM with a Two–Stage Integrated Power Amplifier (I.P.A.)

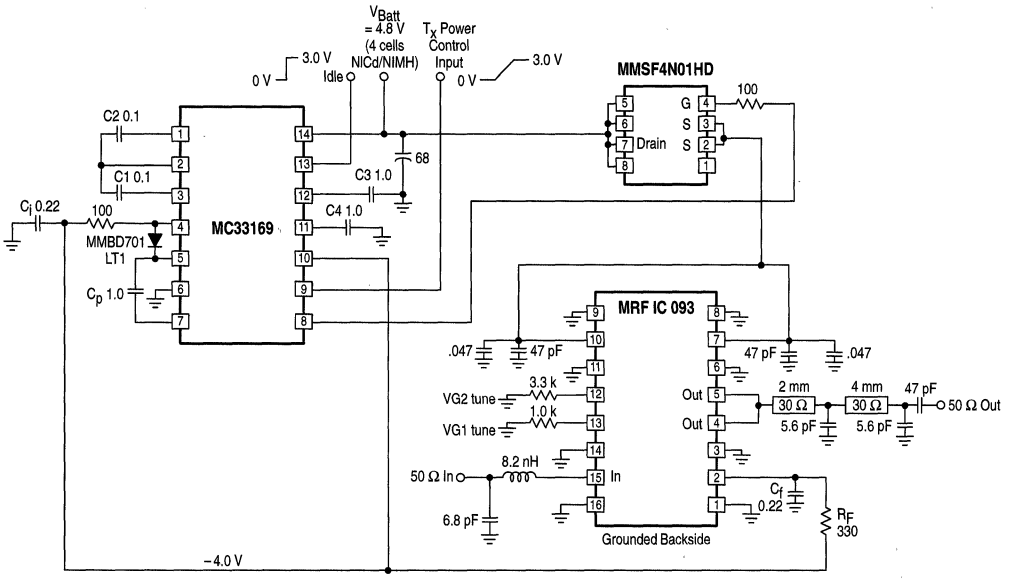
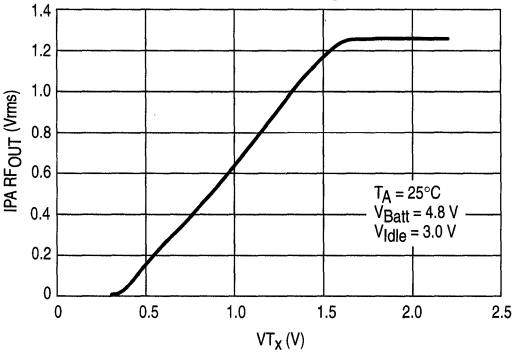


Figure 11. Transfer Characteristic for Gate Drive Output



V_{Batt} = 4.8 V
P_{in} = 10 dBm
V_{Idle} = 3.0 V

V_{ramp}: 40 Hz sinusoidal voltage set for 95% AM depth on RF

Peak output power: 34.6 dBm

CURVES RELATED TO APPLICATION GSM CLASS 4

Figure 12. RF Output Voltage (40 Hz/95% AM) and VT_X Driving Voltage

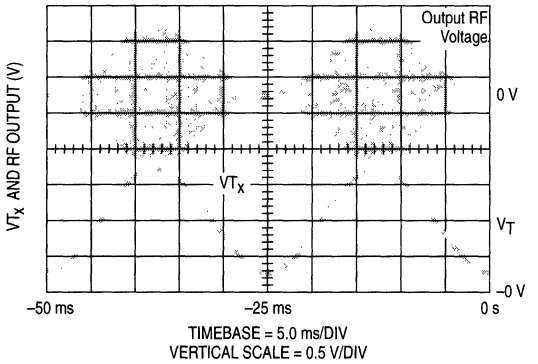


Figure 13. Idle, PA Drain, RF Output and V_O Voltages During a Burst Period

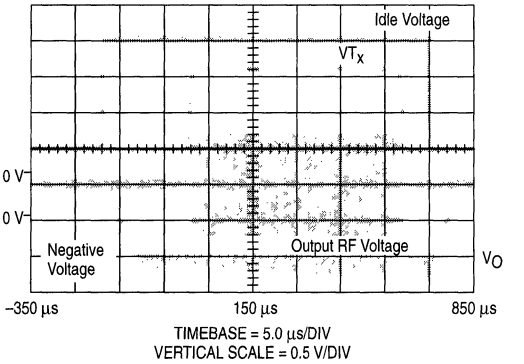


Figure 14. RF Output Voltage, PA Drain Voltage and VT_X Driving Voltage, During Fall Time

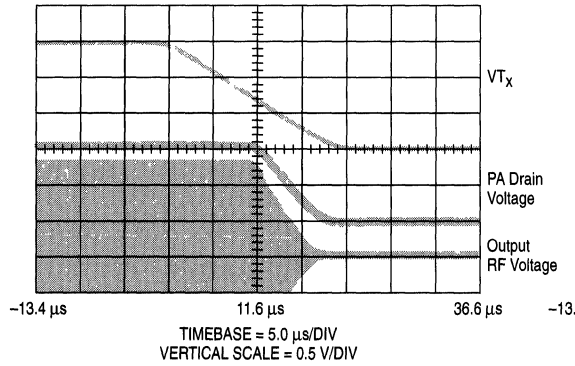


Figure 15. RF Output Voltage, PA Drain Voltage and VT_X Driving Voltage, During Rise Time

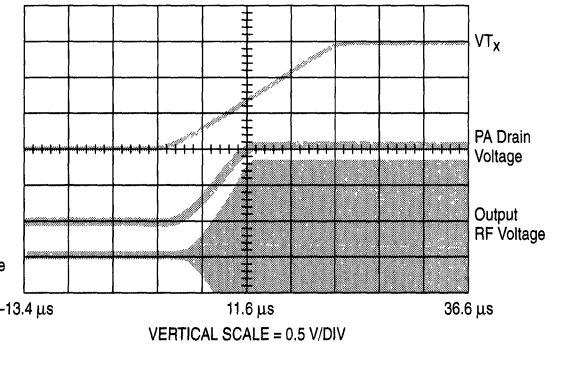


Figure 16. AMPS version with MRFIC0913, Integrated Power Amplifier (I.P.A.)

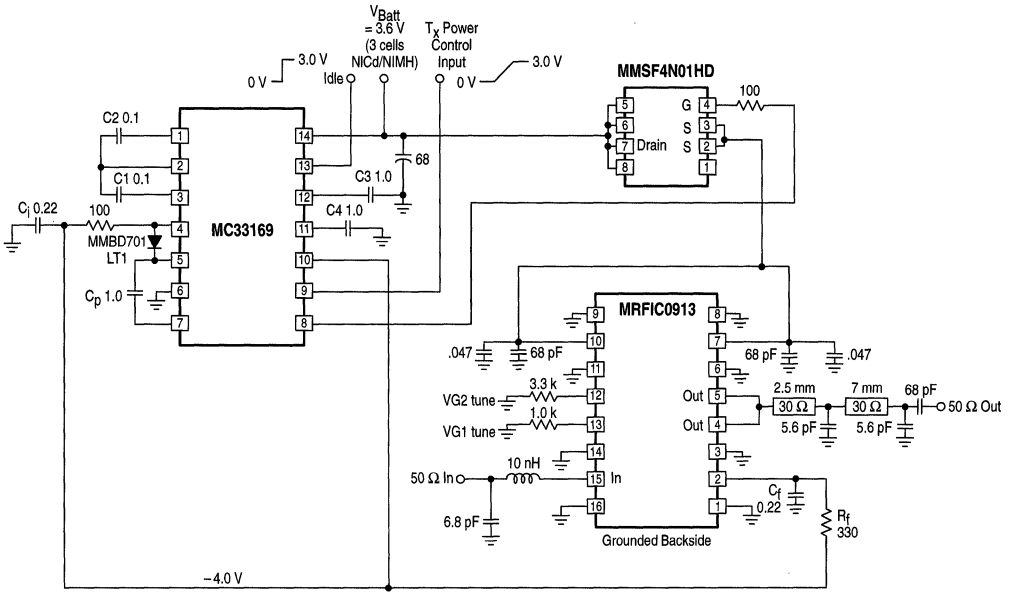
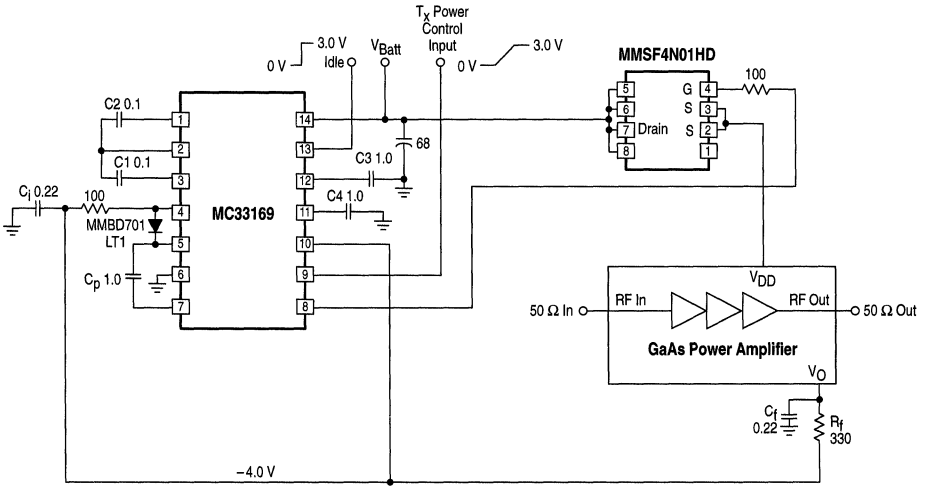


Figure 17. MC33169 with GaAs RF Power Amplifier



MOTOROLA

MC33264

3

Advance Information

Micropower Voltage Regulators with On/Off Control

LOW DROPOUT MICROPOWER VOLTAGE REGULATORS WITH ON/OFF CONTROL

SEMICONDUCTOR TECHNICAL DATA

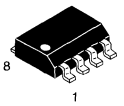
The MC33264 series are micropower low dropout voltage regulators available in SO–8 and Micro–8 surface mount packages and a wide range of output voltages. These devices feature a very low quiescent current (100 μA in the ON mode; 0.1 μA in the OFF mode), and are capable of supplying output currents up to 100 mA. Internal current and thermal limiting protection is provided.

Additionally, the MC33264 has either active HIGH or active LOW control (Pins 2 and 3) that allows a logic level signal to turn–off or turn–on the regulator output.

Due to the low input–to–output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC33264 Features:

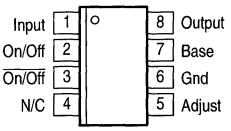
- Low Quiescent Current (0.3 μA in OFF Mode; 95 μA in ON Mode)
- Low Input–to–Output Voltage Differential of 47 mV at 10 mA, and 131 mV at 50 mA
- Multiple Output Voltages Available
- Extremely Tight Line and Load Regulation
- Stable with Output Capacitance of Only
  0.33 μF for 5.0 V, 6.0 V and 4.75 V Output Voltages
  0.22 μF for 2.8 V, 3.0 V and 3.3 V Output Voltages
- Internal Current and Thermal Limiting
- Logic Level ON/OFF Control
- Functionally Equivalent to TK115XXMC and LP2980



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

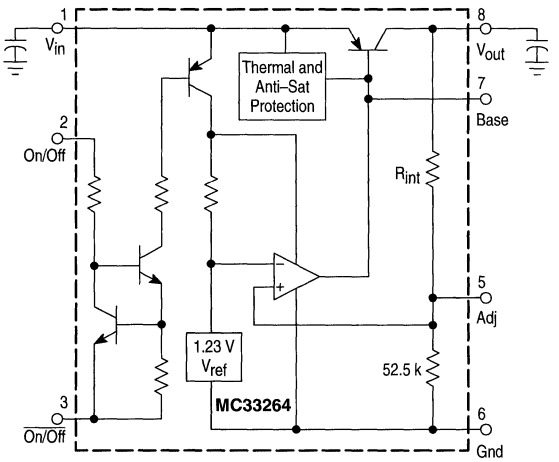
DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)

PIN CONNECTIONS



(Top View)

Representative Block Diagram



This device contains 37 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33264D–2.8 MC33264D–3.0 MC33264D–3.3 MC33264D–3.8 MC33264D–4.0 MC33264D–4.75 MC33264D–5.0	T_A = – 40° to +85°C	SO–8
MC33264DM–2.8 MC33264DM–3.0 MC33264DM–3.3 MC33264DM–3.8 MC33264DM–4.0 MC33264DM–4.75 MC33264DM–5.0		Micro–8

3

MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_{CC}	13	Vdc
Power Dissipation and Thermal Characteristics Maximum Power Dissipation Case 751 (SO–8) D Suffix Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case Case 846A (Micro–8) DM Suffix Thermal Resistance, Junction–to–Ambient	 P_D $R_{\theta JA}$ $R_{\theta JC}$ $R_{\theta JA}$	 Internally Limited 180 45 240	 W °C/W °C/W °C/W
Output Current	I_O	100	mA
Maximum Adjustable Output Voltage	V_O	1.15 x V_{nom}	Vdc
Operating Junction Temperature	T_J	125	°C
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{in} = 6.0 V, I_O = 10 mA, C_O = 1.0 µF, T_J = 25°C (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0 mA)	V_O				V
2.8 Suffix (V_{CC} = 3.8 V)		2.74	2.8	2.86	
3.0 Suffix (V_{CC} = 4.0 V)		2.96	3.0	3.04	
3.3 Suffix (V_{CC} = 4.3 V)		3.23	3.3	3.37	
3.8 Suffix (V_{CC} = 4.8 V)		3.72	3.8	3.88	
4.0 Suffix (V_{CC} = 5.0 V)		3.92	4.0	4.08	
4.75 Suffix (V_{CC} = 5.75 V)		4.66	4.75	4.85	
5.0 Suffix (V_{CC} = 6.0 V)		4.9	5.0	5.1	
V_{in} = (V_O + 1.0) V to 12 V, I_O < 60 mA, T_A= –40° to +85°C					
2.8 Suffix		2.7	–	2.9	
3.0 Suffix		2.9	–	3.1	
3.3 Suffix		3.18	–	3.42	
3.8 Suffix		3.67	–	3.93	
4.0 Suffix		3.86	–	4.14	
4.75 Suffix		4.58	–	4.92	
5.0 Suffix		4.83	–	5.17	
Line Regulation (V_{in} = [V_O + 1.0] V to 12 V, I_O = 60 mA) All Suffixes	Reg_{line}	–	2.0	10	mV
Load Regulation (V_{in} = [V_O + 1.0], I_O = 0 mA to 60 mA) All Suffixes	Reg_{load}	–	16	25	mV
Dropout Voltage	$V_I - V_O$				mV
I_O = 10 mA		–	47	90	
I_O = 50 mA		–	131	200	
I_O = 60 mA		–	147	230	
Quiescent Current	I_Q				µA
ON Mode (V_{in} = [V_O + 1.0] V, I_O = 0 mA)		–	95	150	
OFF Mode		–	0.3	2.0	
ON Mode (V_{in} = [V_O – 0.5] V, I_O = 0 mA) [Note2]		–	540	900	
Ripple Rejection (V_{in} peak–to–peak = [V_O + 1.5] to [V_O + 5.5] V at f = 1.0 kHz)	–	55	65	–	dB
Output Voltage Temperature Coefficient	TC	–	±120	–	ppm/°C
Current Limit (V_{in} = [V_O + 1.0], V_O Shorted)	I_{Limit}	100	150	–	mA
Output Noise Voltage (10 Hz to 100 kHz) (Note 3)	V_n				µVrms
C_L = 1.0 µF		–	110	–	
C_L = 100 µF		–	46	–	

NOTES: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. Quiescent current is measured where the PNP pass transistor is in saturation. V_{CE} = –0.5 V guarantees this condition.
3. Noise tests on the MC33264 are made with a 0.01 µF capacitor connected across Pins 8 and 5.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 6.0 V, I_O = 10 mA, C_O = 1.0 µF, T_J = 25°C (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON/OFF INPUTS					
On/Off Input (Pin 3 Tied to Ground)	$V_{On/Off}$				V
Logic "1" (Regulator ON)		2.4	–	V_{in}	
Logic "0" (Regulator OFF)		0	–	0.5	
$\overline{On/Off}$ Input (Pin 2 Tied to V_{in})					
Logic "0" (Regulator ON)		0	–	V_{in} – 2.4	
Logic "1" (Regulator OFF)		V_{in} – 0.2	–	V_{in}	
On/Off Pin Input Current (Pin 3 Tied to Ground)	$I_{On/Off}$				µA
$V_{On/Off}$= 2.4 V		–	1.9	–	
$\overline{On/Off}$ Pin Input Current (Pin 2 Tied to V_{in})					
$V_{On/Off} = V_{in}$ – 2.4 V		–	12	–	

NOTES: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. Quiescent current is measured where the PNP pass transistor is in saturation. V_{CE} = –0.5 V guarantees this condition.
3. Noise tests on the MC33264 are made with a 0.01 µF capacitor connected across Pins 8 and 5.

DEFINITIONS

Dropout Voltage – The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation – The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current – Current which is used to operate the regulator chip and is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Figure 1. Quiescent Current versus Load Current

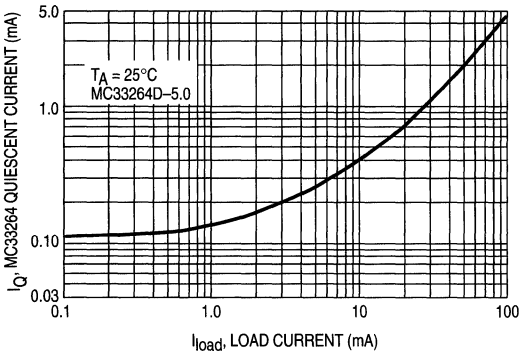


Figure 2. Dropout Voltage versus Input Voltage

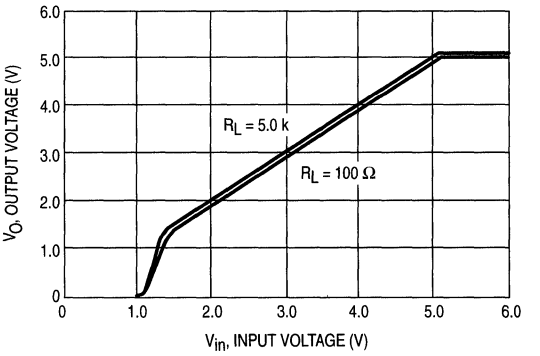


Figure 3. Input Current versus Input Voltage

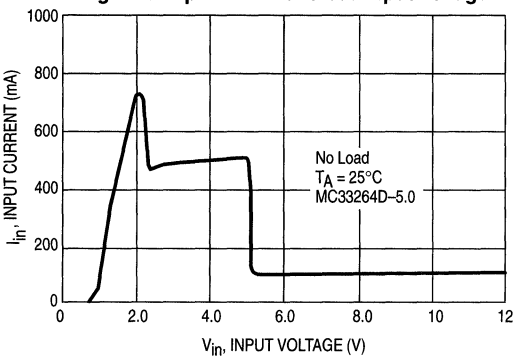


Figure 4. Output Voltage versus Temperature

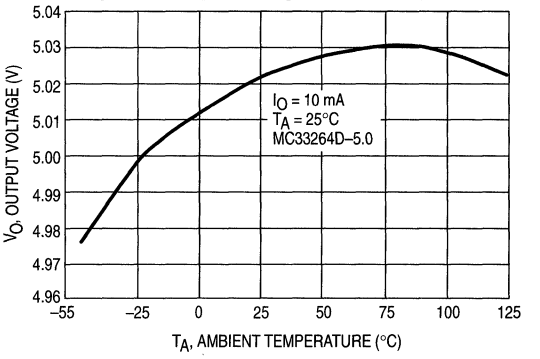


Figure 5. Dropout Voltage versus Output Current

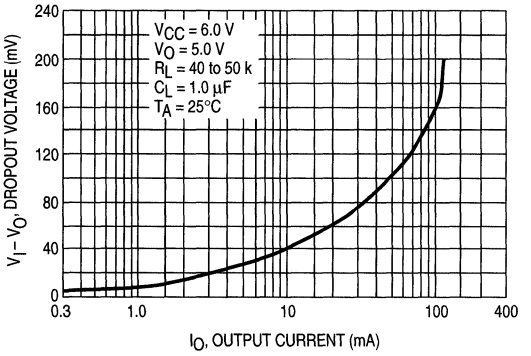
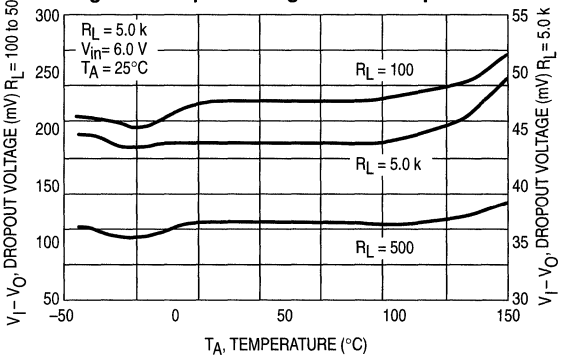


Figure 6. Dropout Voltage versus Temperature



APPLICATION INFORMATION

Introduction

The MC33264 regulators are designed with internal current limiting and thermal shutdown making them user–friendly. These regulators require only 0.33 µF (or greater) capacitance between the output terminal and ground for stability for 2.8 V, 3.0 V, and 3.3 V output voltage options. Output voltage options of 5.0 V, 6.0 V and 4.75 V require only 0.22 µF for stability. The output capacitor must be mounted as close to the MC33264 as possible. If the output capacitor must be mounted further than two centimeters away from the MC33264, then a larger value of output capacitor may be required for stability. A value of 0.68 µF or larger is recommended. Most types of aluminum, tantalum or multilayer ceramic will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are recommended for operation below 25°C.

A bypass capacitor is recommended across the MC33264 input to ground if more than 4.0 inches of wire connects the input to either a battery or power supply filter capacitor.

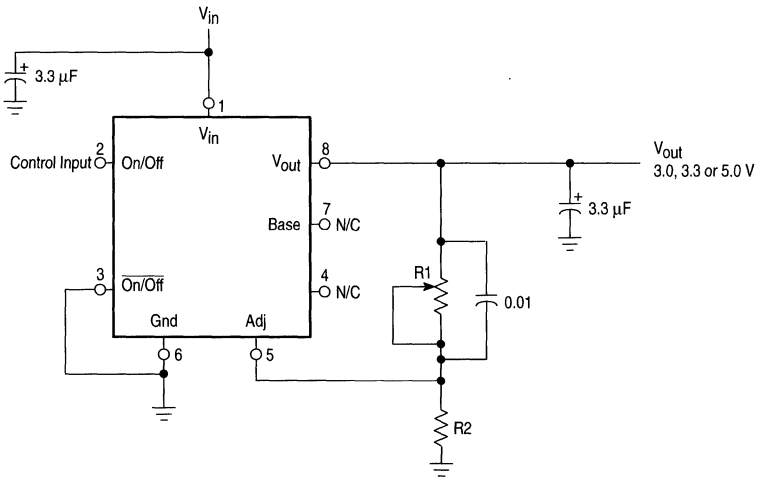
On/Off Control

On/Off control of the regulator may be accomplished in either of two ways. Pin 3 may be tied to circuit ground and a positive logic control applied to Pin 2. The regulator will be turned on by a positive (>2.4 V) level, typically 5.0 V with respect to ground, sourcing a typical current of 6.0 µA. The regulator will turn off if the control input is a logic "0" (<0.5 V). Alternatively, Pin 2 may be tied to the regulator input voltage and a negative logic control applied to Pin 3. The regulator will be turned on when the control voltage is less than V_{in} – 2.4 V, sinking a typical current of 18 µA when V_{in} = 6.0 V. The regulator is off when the control input is open or greater than V_{in} – 0.2 V.

Programming The Output Voltage

The MC33264 output voltage is automatically set using its internal voltage divider. Alternatively, it may be programmed within a typical ±15% range of its preset output voltage. An external pair of resistors is required, as shown in Figure 7.

Figure 7. Regulator Output Voltage Trim



The complete equation for the output voltage is:

$$V_{out} = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{FB}\ R1$$

where V_{ref} is the nominal 1.235 V reference voltage and I_{FB} is the feedback pin bias current, nominally –20 nA. The minimum recommended load current of 1.0 µA forces an upper limit of 1.2 MΩ on the value of R2, if the regulator must work with no load. I_{FB} will produce a 2% typical error in V_{out} which may be eliminated at room temperature by adjusting R1. For better accuracy, choosing R2 = 100 K reduces this error to 0.17% while increasing the resistor program current to 12 µA.

Output Noise

In many applications it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor is the only method for reducing noise.

Noise can be reduced fourfold by a bypass capacitor across R1, since it reduces the high frequency gain from 4 to unity for the MC33264D–5.0. Pick

$$C_{BYPASS} = \frac{1}{2\pi\ R1\ x\ 200\ Hz}$$

or about 0.01 µF. When doing this, the output capacitor must be increased to 3.3 µF to maintain stability. These changes reduce the output noise from 430 µV to 100 Vrms for a 100 kHz bandwidth for the 5.0 V output device. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

TYPICAL APPLICATIONS

Figure 8. Lithium Ion Battery Cell Charger

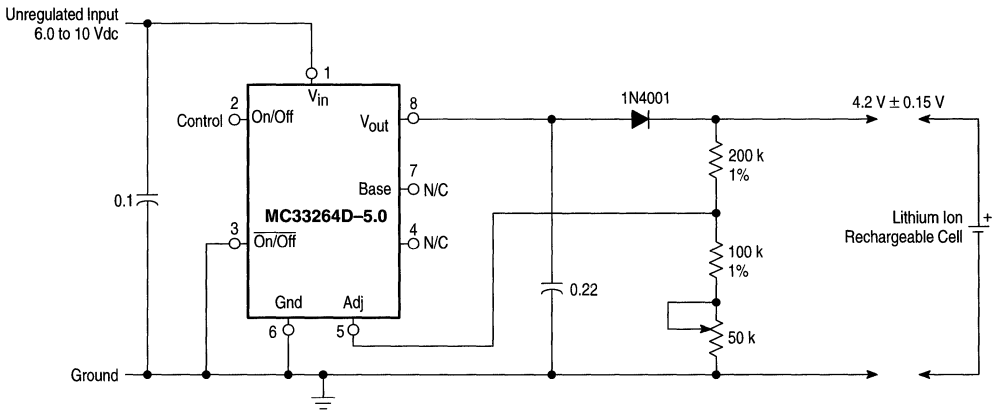


Figure 9. Low Drift Current Source

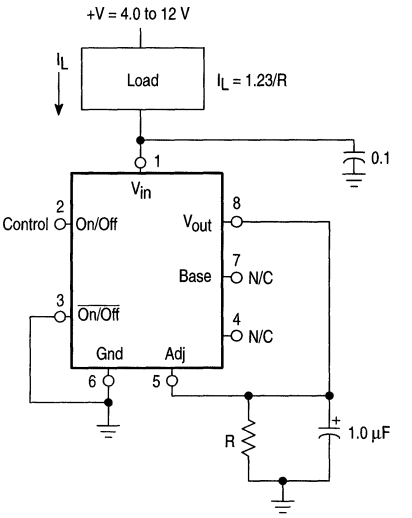


Figure 10. 2.0 Ampere Low Dropout Regulator

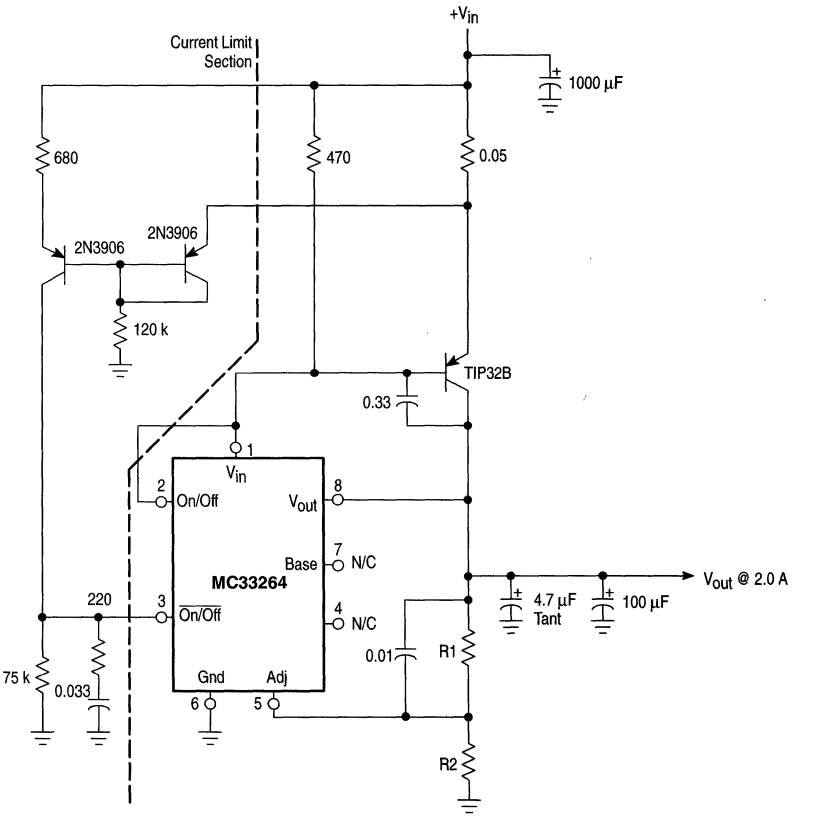


Figure 11. Low Battery Disconnect

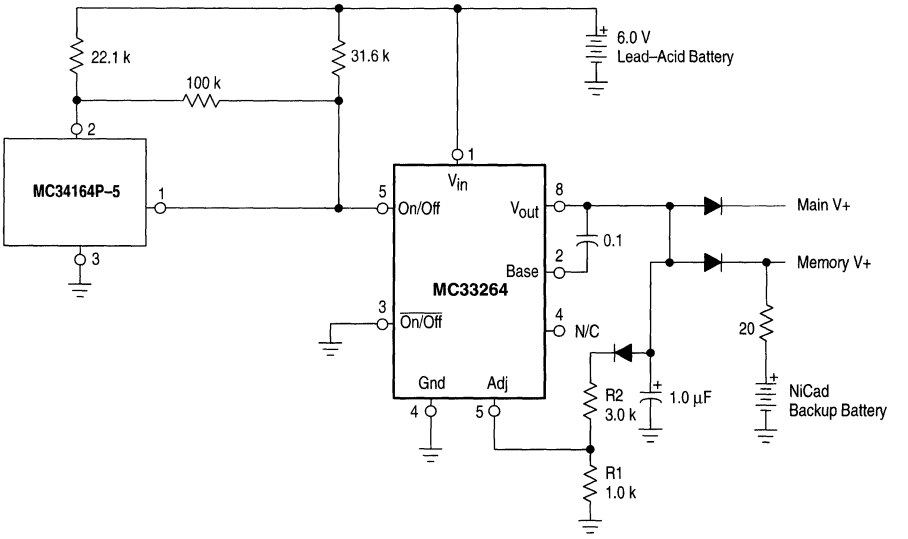
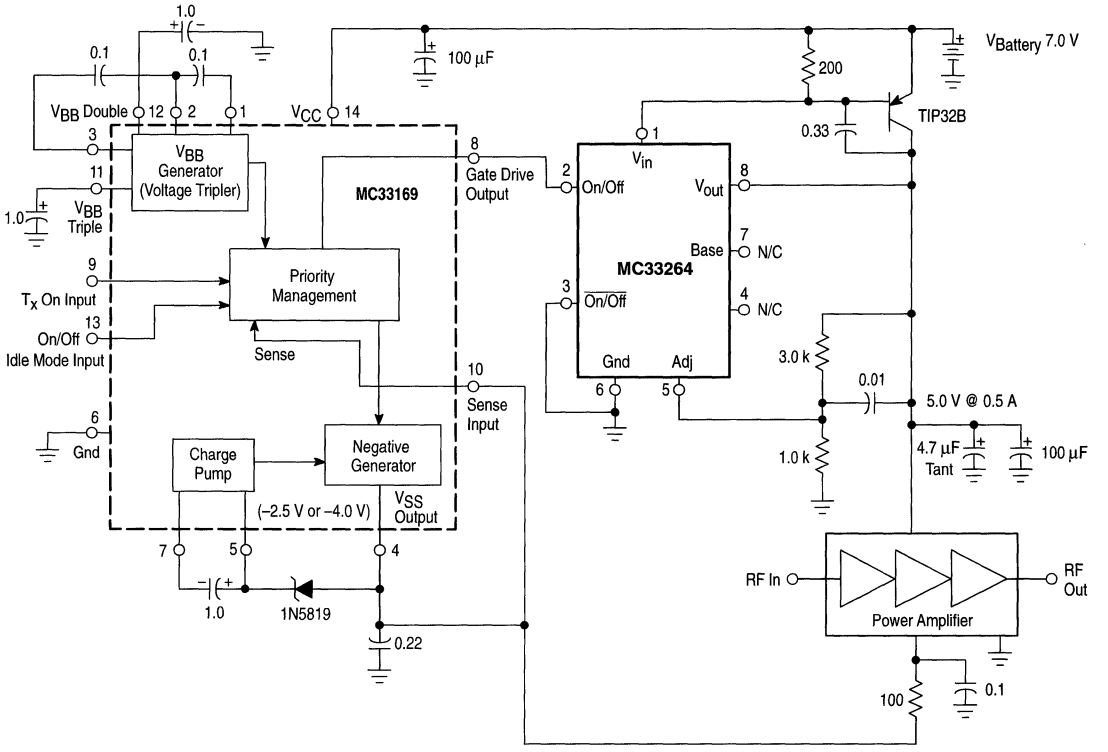


Figure 12. RF Amplifier Supply



MC33267

Low Dropout Regulator

3

The MC33267 is a positive fixed 5.0 V regulator that is specifically designed to maintain proper voltage regulation with an extremely low input–to–output voltage differential. This device is capable of supplying output currents in excess of 500 mA and contains internal current limiting and thermal shutdown protection. Also featured is an on–chip power–up reset circuit that is ideally suited for use in microprocessor based systems. Whenever the regulator output voltage is below nominal, the reset output is held low. A programmable time delay is initiated after the regulator has reached its nominal level and upon timeout, the reset output is released.

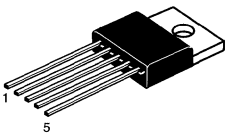
Due to the low dropout voltage specifications, the MC33267 is ideally suited for use in battery powered industrial and consumer equipment where an extension of useful battery life is desirable. This device is contained in an economical five lead TO–220 type package.

- Low Input–to–Output Voltage Differential
- Output Current in Excess of 500 mA
- On–Chip Power–Up Reset Circuit with Programmable Delay
- Internal Current Limiting with Thermal Shutdown
- Economical Five Lead TO–220 Type Packages

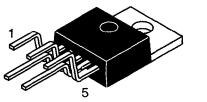
LOW DROPOUT REGULATOR with POWER–UP RESET

SEMICONDUCTOR TECHNICAL DATA

Pin 1. V_{CC} Input
2. Reset
3. Ground
4. Delay
5. Output

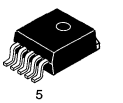


T SUFFIX
PLASTIC PACKAGE
CASE 314D



TV SUFFIX
PLASTIC PACKAGE
CASE 314B

Heatsink surface connected to Pin 3.



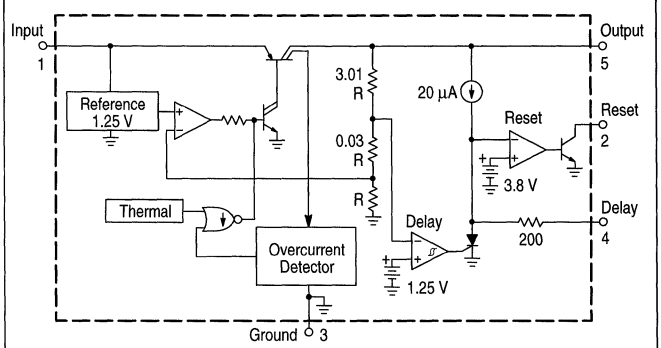
D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^2PAK)

Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3.

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC33267T	T_J = –40 ° to +125°C	Plastic Power
MC33267TV		Plastic Power
MC33267D2T	T_J = –40 ° to +105°C	Surface Mount

Representative Block Diagram



This device contains 37 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range	V_{in}	– 20 to + 40	Vdc
Delay Voltage Range	V_{DLYR}	– 0.3 to V_O	V
Delay Sink Current	$I_{DLY(sink)}$	25	mA
Reset Voltage Range	V_{RR}	– 0.3 to +15	V
Reset Sink Current	$I_{R(sink)}$	50	mA
Power Dissipation			
Case 314B and 314D (TO–220 Type)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	4.0	°C/W
Case 936A (D^2PAK) [Note 1]			
T_A = 90°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	70	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

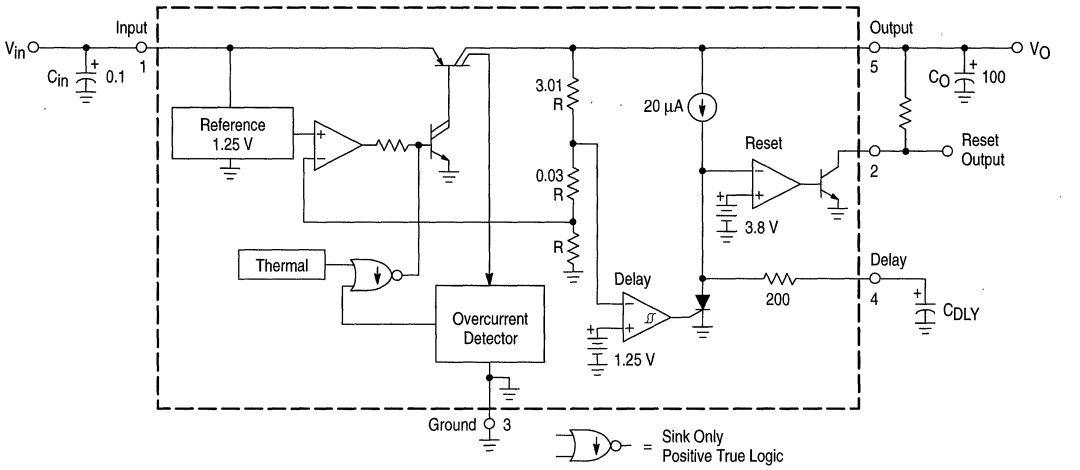
NOTE: 1. D^2PAK Junction–to–Ambient Thermal Resistance is for vertical mounting. Refer to Figure 7 for board mounted thermal resistance.

ELECTRICAL CHARACTERISTICS (V_{in} = 14.4 V, I_O = 5.0 mA, C_O = 100 µF, $C_{O(ESR)} \leq 0.3\ \Omega$, T_J = 25°C (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 5.0 mA to 500 mA, V_{in} = 6.0 V to 28 V)	V_O				V
T_J = 25°C		4.95	5.05	5.15	
T_J = – 40° to +125°C		4.9	–	5.2	
Line Regulation (V_{in} = 6.0 V to 26 V)	Reg_{line}	–	3.0	50	mV
Load Regulation (I_O = 5.0 mA to 500 mA)	Reg_{load}	–	1.0	50	mV
Bias Current	I_B				mA
I_O = 0 mA		–	12	20	
I_O = 150 mA		–	22	40	
I_O = 500 mA		–	100	200	
I_O = 500 mA, V_{in} = 6.2 V		–	120	300	
Ripple Rejection (f = 120 Hz, V_{in} = 7.0 V to 17 V, I_O = 350 mA, C_O = 100 µF)	RR	60	80	–	dB
Dropout Voltage (I_O = 500 mA)	$V_{in} - V_O$	–	0.58	0.8	V
Delay Comparator Threshold (V_O Decreasing)	$V_{th(DLY)}$	4.8	V_O – 0.15	V_O – 0.08	V
Delay Pin Source Current	$I_{DLY(source)}$	12	20	28	µA
Reset Comparator Threshold	$V_{th(R)}$	3.6	3.8	4.0	V
Reset Sink Saturation (I_{sink} = 10 mA)	$V_{CE(sat)}$	–	0.2	0.8	V
Reset Off–State Leakage (V_{CE} = 5.0 V)	$I_{R(leak)}$	–	0.3	10	µA

NOTE: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Typical Application Circuit



APPLICATION CIRCUIT INFORMATION

The MC33267 is a low dropout, positive fixed 5.0 V, 500 mA regulator. Protection features include output current limiting and thermal shutdown. System protection consists of an on–chip power–up microprocessor reset circuit.

A typical applications circuit is shown in Figure 1. The input bypass capacitor (C_{in}) is recommended if the regulator is located an appreciable distance (≥ 4″) from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

These regulators are not internally compensated and thus require an external output capacitor (C_O) for stability. The recommended capacitance is 100 µF with an equivalent series resistance (ESR) of less than 0.3 Ω. A minimum capacitance of 33 µF with a maximum ESR of 3.0 Ω can be used in applications where space is a premium, however, these limits must be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around – 30°C, the capacitance will decrease and the ESR will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of – 40°C to + 85°C and – 55°C to +105°C are readily available. It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.

Figure 2 shows the reset circuit timing relationship. Note that whenever the regulator's output is less than 4.9 V, the delay capacitor (C_{DLY}) is immediately discharged, and the reset output is held in a low state. As the regulator's output voltage increases beyond 4.97 V, the delay comparator will allow the 20 µA current source to charge C_{DLY}. The reset output will go to a high state when C_{DLY} crosses the 3.8 V threshold of the reset comparator. The reset delay time is controlled by the value selected for C_{DLY}. The required system reset time is governed by the microprocessor and usually a reset signal which lasts several machine cycles is sufficient.

Figure 2. Timing Waveforms

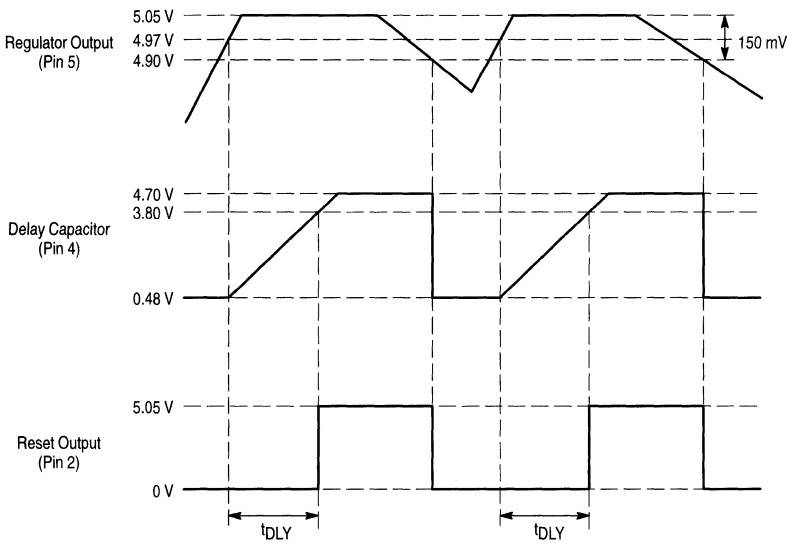


Figure 3. Reset Output versus Input Voltage

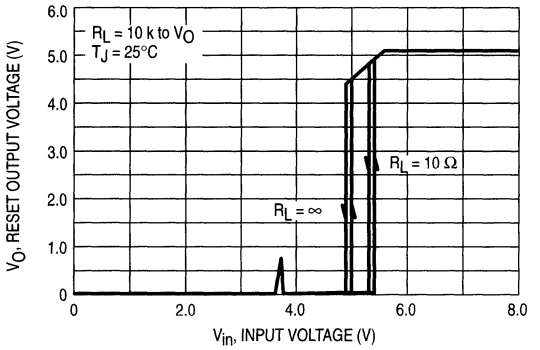


Figure 4. Output Voltage versus Input Voltage

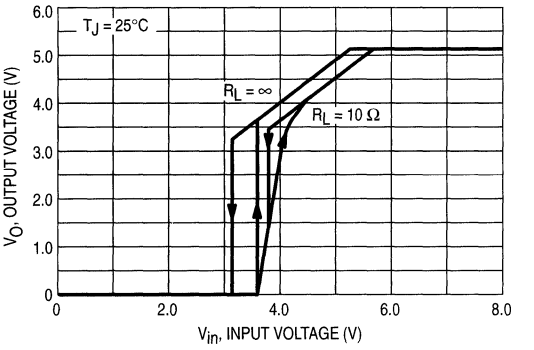


Figure 5. Reset Output versus Input Voltage

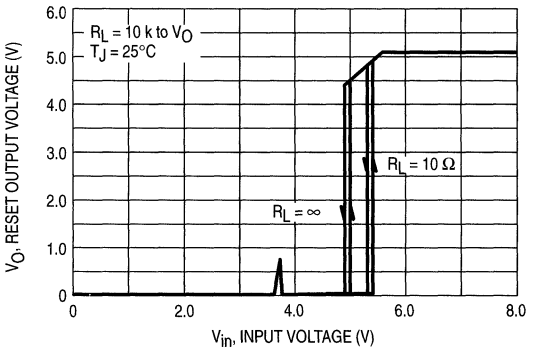


Figure 6. Output Voltage versus Input Voltage

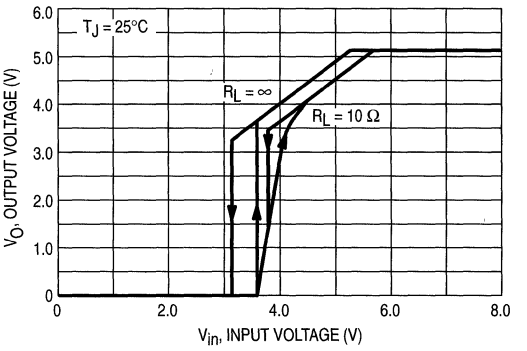
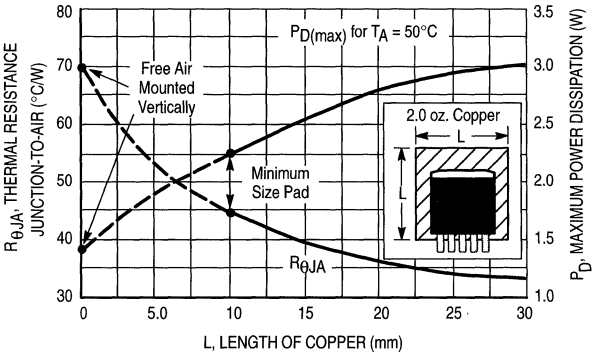


Figure 7. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MOTOROLA

MC33269

Advance Information

Low Dropout Positive Fixed and Adjustable Voltage Regulators

800 mA LOW DROPOUT THREE–TERMINAL VOLTAGE REGULATORS

3

The MC33269 series are low dropout, medium current, fixed and adjustable, positive voltage regulators specifically designed for use in low input voltage applications. These devices offer the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum.

The regulator consists of a 1.0 V dropout composite PNP–NPN pass transistor, current limiting, and thermal shutdown.

- 3.3 V, 5.0 V, 12 V and Adjustable Versions
- Space Saving DPAK and SOP–8 Power Package
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to 1.0% Tolerance
- No Minimum Load Requirement for Fixed Voltage Output Devices

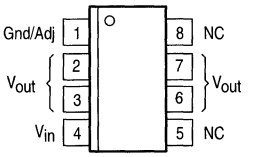
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33269D	$T_J = -40°$ to $+125°C$	SOP–8
MC33269DT		DPAK
MC33269T		Insertion Mount
MC33269D–3.3		SOP–8
MC33269DT–3.3		DPAK
MC33269T–3.3		Insertion Mount
MC33269D–5.0		SOP–8
MC33269DT–5.0		DPAK
MC33269T–5.0		Insertion Mount
MC33269D–12		SOP–8
MC33269DT–12		DPAK
MC33269T–12		Insertion Mount

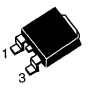
DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC33269D	Adj	MC33269D–5.0	5.0 V
MC33269DT	Adj	MC33269DT–5.0	5.0 V
MC33269T	Adj	MC33269T–5.0	5.0 V
MC33269D–3.3	3.3 V	MC33269D–12	12 V
MC33269DT–3.3	3.3 V	MC33269DT–12	12 V
MC33269T–3.3	3.3 V	MC33269T–12	12 V

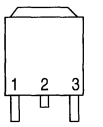
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)



(Top View)



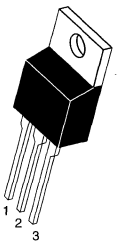
DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)



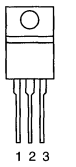
1. Gnd/Adj
2. V_{out}
3. V_{in}

(Top View)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.



T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin: 1. Gnd/Adj
2. V_{out}
3. V_{in}

(Top View)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{in}	20	V
Power Dissipation			
Case 369A (DPAK)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	92	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	6.0	°C/W
Case 751 (SOP–8)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	160	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	25	°C/W
Case 221A			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	65	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

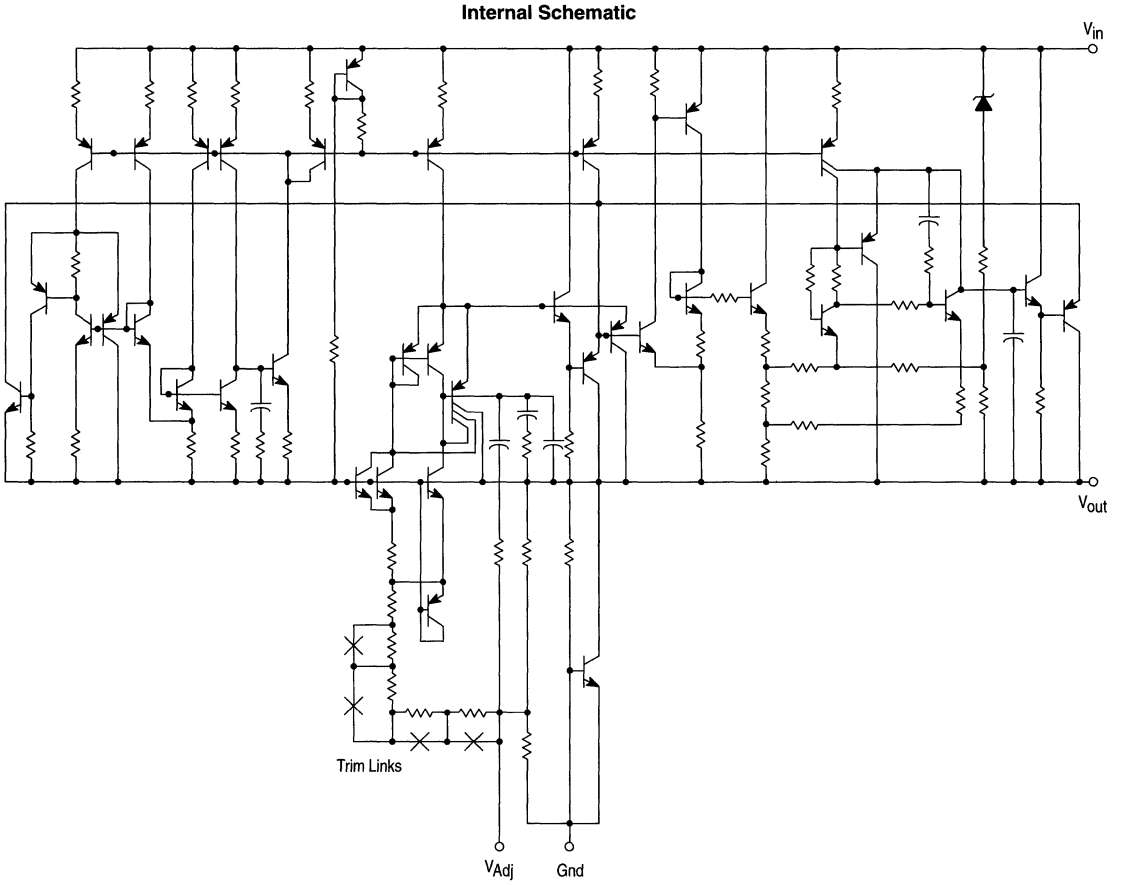
NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (C_O = 10 µF, T_A = 25°C, for min/max values T_J = –40°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_{out} = 10 mA, T_J = 25°C)	V_O				V
3.3 Suffix (V_{CC} = 5.3 V)		3.27	3.3	3.33	
5.0 Suffix (V_{CC} = 7.0 V)		4.95	5.0	5.05	
12 Suffix (V_{CC} = 14 V)		11.88	12	12.12	
Output Voltage (Line, Load and Temperature) (Note 1)	V_O				V
(1.25 V ≤ V_{in} – V_{out} ≤ 15 V, I_{out} = 500 mA)					
(1.35 V ≤ V_{in} – V_{out} ≤ 10 V, I_{out} = 800 mA)					
3.3 Suffix		3.23	3.3	3.37	
5.0 Suffix		4.9	5.0	5.1	
12 Suffix		11.76	12	12.24	
Reference Voltage (I_{out} = 10 mA, V_{in} – V_{out} = 2.0 V, T_J = 25°C) Adjustable	V_{ref}	1.235	1.25	1.265	V
Reference Voltage (Line, Load and Temperature) (Note 1)	V_{ref}	1.225	1.25	1.275	V
(1.25 V ≤ V_{in} – V_{out} ≤ 15 V, I_{out} = 500 mA)					
(1.35 V ≤ V_{in} – V_{out} ≤ 10 V, I_{out} = 800 mA)					
Adjustable					
Line Regulation (I_{out} = 10 mA, V_{in} = [V_{out} + 1.5 V] to V_{in} = 20 V, T_J = 25°C)	Reg_{line}	–	–	0.3	%
Load Regulation (V_{in} = V_{out} + 3.0 V, I_{out} = 10 mA to 800 mA, T_J = 25°C)	Reg_{load}	–	–	0.5	%
Dropout Voltage	$V_{in} - V_{out}$				V
(I_{out} = 500 mA)		–	1.0	1.25	
(I_{out} = 800 mA)		–	1.1	1.35	
Ripple Rejection (10 Vpp, 120 Hz Sinewave; I_{out} = 500 mA)	RR	55	–	–	dB
Current Limit (V_{in} – V_{out} = 10 V)	I_{Limit}	800	–	–	mA
Quiescent Current (Fixed Output)	I_Q	–	5.5	8.0	mA
Minimum Required Load Current	I_{Load}				mA
Fixed Output		–	–	0	
Adjustable		8.0	–	–	
Adjustment Pin Current	I_{Adj}	–	–	120	µA

NOTE 1: The MC33269–12, V_{in} – V_{out} is limited to 8.0 V maximum, because of the 20 V maximum rating applied to V_{in}.

Internal Schematic



This device contains 38 active transistors.

Figure 1. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

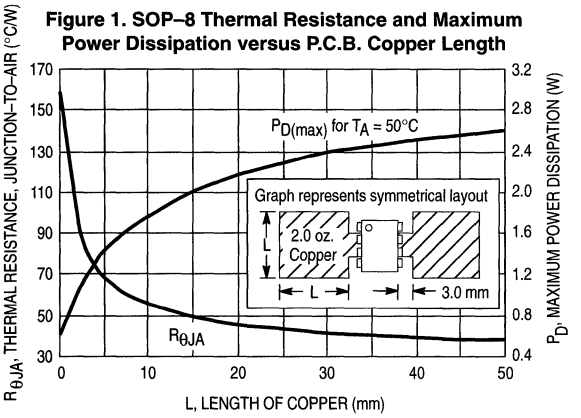


Figure 2. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

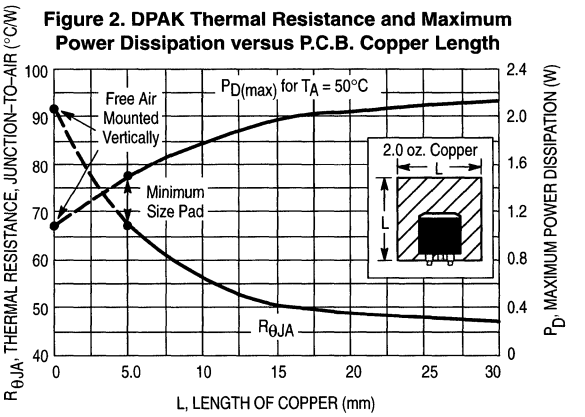


Figure 3. Dropout Voltage versus Output Load Current

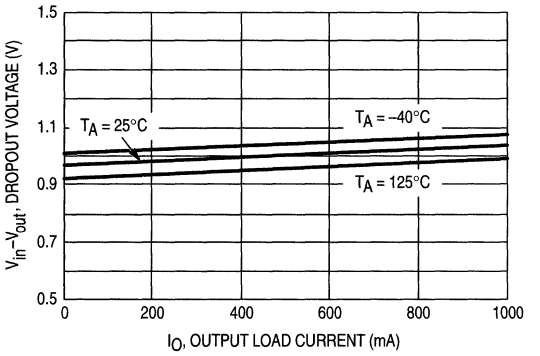


Figure 4. Transient Load Regulation

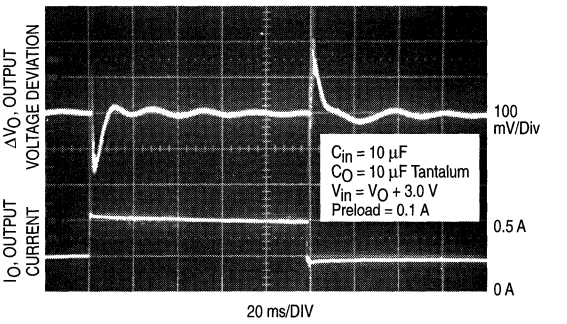


Figure 5. Dropout Voltage versus Temperature

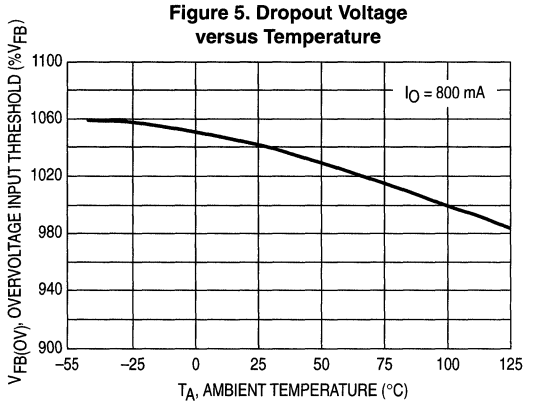


Figure 6. MC33269–XX Output DC Current versus Input–Output Differential Voltage

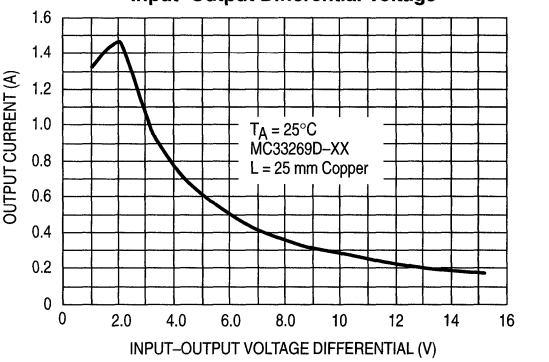


Figure 7. MC33269 Ripple Rejection versus Frequency

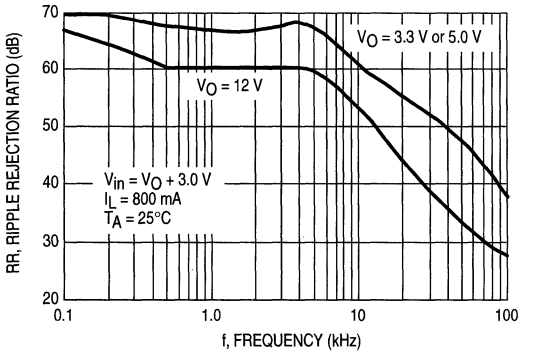
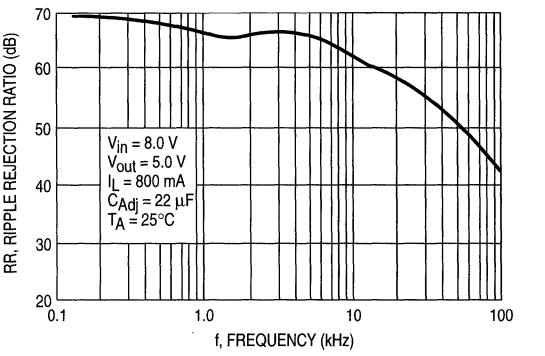


Figure 8. MC33269–ADJ Ripple Rejection versus Frequency



APPLICATIONS INFORMATION

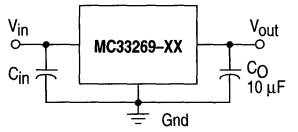
Figures 9 through 13 are typical application circuits. The output current capability of the regulator is in excess of 800 mA, with a typical dropout voltage of less than 1.0 V. Internal protective features include current and thermal limiting.

The MC33269 is not internally compensated and thus requires an external output capacitor for stability. The capacitor should be at least 10 μF with an equivalent series resistance (ESR) of less than 10 Ω over the anticipated operating temperature range. With economical electrolytic capacitors, cold temperature operation can pose a problem. As temperature decreases, the capacitance also decreases and the ESR increases, which could cause the circuit to oscillate. Solid tantalum capacitors may be a better choice if small size is a requirement. Also capacitance and ESR of a solid tantalum capacitor is more stable over temperature. An input bypass capacitor is recommended to improve transient response or if the regulator is connected to the supply input filter with long wire lengths. This will reduce the circuit's sensitivity to the input line impedance at high frequencies. A 0.33 μF or larger tantalum, mylar, ceramic, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with shortest possible lead or track length directly across the regulator's input terminals. **Applications should be tested over all operating conditions to insure stability.**

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the output is disabled. There is no hysteresis built into the thermal limiting circuit. As a result, if the device is overheating, the output will appear to be oscillating. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.**

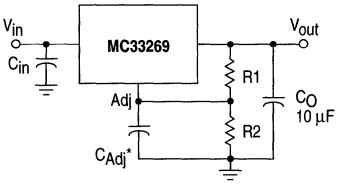
3

Figure 9. Typical Fixed Output Application



An input capacitor is not necessary for stability, however it will improve the overall performance.

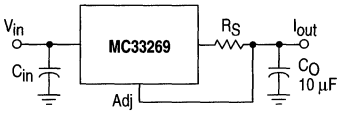
Figure 10. Typical Adjustable Output Application



$$V_{out} = 1.25 \left(1 + \frac{R2}{R1}\right) + I_{Adj} R2$$

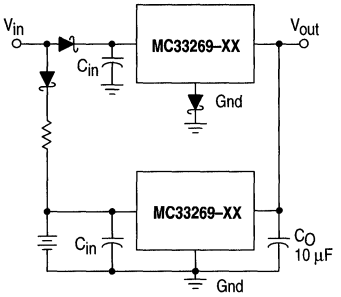
*C_{Adj} is optional, however it will improve the ripple rejection. The MC34269 develops a 1.25 V reference voltage between the output and the adjust terminal. Resistor R1, operates with constant current to flow through it and resistor R2. This current should be set such that the Adjust Pin current causes negligible drop across resistor R2. The total current with minimum load should be greater than 8.0 mA.

Figure 11. Current Regulator



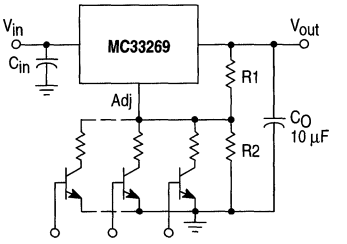
$$I_{out} = \frac{1.25}{R_S}$$

Figure 12. Battery Backed–Up Power Supply



The Schottky diode in series with the ground leg of the upper regulator shifts its output voltage higher by the forward voltage drop of the diode. This will cause the lower device to remain off until the input voltage is removed.

Figure 13. Digitally Controlled Voltage Regulator



R_2 sets the maximum output voltage. Each transistor reduces the output voltage when turned on.

MOTOROLA

MC33340

Product Preview

Battery Fast Charge Controller

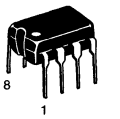
3

The MC33340 is a monolithic control IC that is specifically designed as a fast charge controller for Nickel Cadmium (NiCd) and Nickel Metal Hydride (NiMH) batteries. This device features negative slope voltage detection as the primary means for fast charge termination. Accurate detection is ensured by an output that momentarily interrupts the charge current for precise voltage sampling. An additional secondary backup termination method can be selected that consists of either a programmable time or temperature limit. Protective features include battery over and undervoltage detection, latched over temperature detection, and power supply input undervoltage lockout with hysteresis. Provisions for entering a rapid test mode are available to enhance end product testing. This device is available in an economical 8–lead surface mount package.

- Negative Slope Voltage Detection
- Accurate Zero Current Battery Voltage Sensing
- Programmable 1 to 4 Hour Fast Charge Time Limit
- Programmable Over/Under Temperature Detection
- Battery Over and Undervoltage Fast Charge Protection
- Rapid System Test Mode
- Power Supply Input Undervoltage Lockout with Hysteresis
- Operating Voltage Range of 3.0 V to 18 V

BATTERY FAST CHARGE CONTROLLER

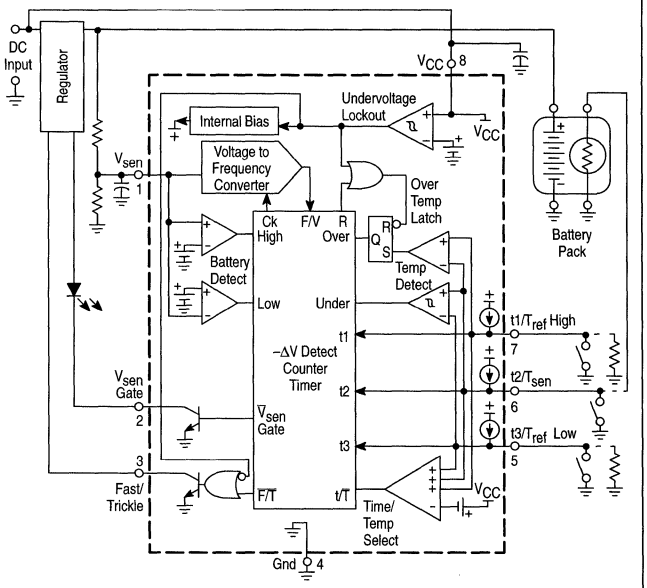
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

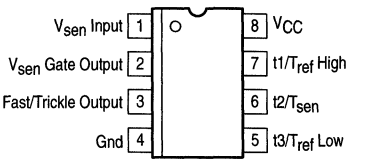
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Simplified Block Diagram



This device contains 2,512 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33340D	T_A = –25° to +85°C	SO–8
MC33340P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 8)	V_{CC}	18	V
Input Voltage Range Time/Temperature Select (Pins 5, 6, 7) Battery Sense, Note 1 (Pin 1)	 $V_{IR(t/T)}$ $V_{IR(sen)}$	 −1.0 to V_{CC} −1.0 to V_{CC} + 0.6 or −1.0 to 10	V
V_{sen} Gate Output (Pin 2) Voltage Current	 $V_{O(gate)}$ $I_{O(gate)}$	 20 50	 V mA
Fast/Trickle Output (Pin 3) Voltage Current	 $V_{O(F/T)}$ $I_{O(F/T)}$	 20 50	 V mA
Thermal Resistance, Junction–to–Air P Suffix, DIP Plastic Package, Case 626 D Suffix, SO–8 Plastic Package, Case 751	$R_{\theta JA}$	 100 178	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 2)	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 6.0 V, T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
BATTERY SENSE INPUT (Pin 1)					
Overvoltage Threshold T_A = 25°C T_A = T_{low} to T_{high}	$V_{th(OV)}$	 – –	 2.0 1.94 to 2.06	 – –	V
Undervoltage Threshold T_A = 25°C T_A = T_{low} to T_{high}	$V_{th(UV)}$	 – –	 1.0 1.97 to 1.03	 – –	V
Input Bias Current	I_{IB}	–	10	–	nA
Input Resistance	R_{in}	–	10	–	MΩ
TIME/TEMPERATURE INPUTS (Pins 5, 6, 7)					
Programming Inputs (V_{in} = 1.5 V) Input Current Input Current Matching	 I_{in} ΔI_{in}	 – –	 –30 0.5	 – –	 μA %
Input Offset Voltage, Over and Under Temperature Comparators	V_{IO}	–	5.0	–	mV
Under Temperature Comparator Hysteresis (Pin 5)	$V_{H(T)}$	–	44	–	mV
Temperature Select Threshold	$V_{th(t/T)}$	–	V_{CC} − 0.7	–	mV
INTERNAL TIMING					
Internal Clock Oscillator Frequency T_A = 25°C V_{CC} = 6.0 V V_{CC} = 3.0 V to 18 V T_A = T_{low} to T_{high} V_{CC} = 6.0 V V_{CC} = 3.0 V to 18 V	f_{OSC}	 – – – –	 840 693 to 987 680 to 1000 670 to 1010	 – – – –	kHz
V_{sen} Gate Output (Pin 2) Gate Time Gate Repetition Rate	t_{gate}	 – –	 30 1.25	 – –	 ms s
Trickle Mode Holdoff Time from −ΔV Detection	t_{hold}	–	160	–	s

NOTES: 1. Whichever voltage is lower.
2. Tested ambient temperature range for the MC33340: T_{low} = −25°C T_{high} = +85°C
Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 6.0 V, T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{sen} GATE OUTPUT (Pin 2)					
Off–State Leakage Current (V_O = 20 V)	I_{off}	–	0.1	–	µA
Low State Saturation Voltage (I_{sink} = 10 mA)	V_{OL}	–	1.2	–	V
FAST/TRICKLE OUTPUT (Pin 3)					
Off–State Leakage Current (V_O = 20 V)	I_{off}	–	0.1	–	µA
Low State Saturation Voltage (I_{sink} = 10 mA)	V_{OL}	–	1.0	–	V
UNDERVOLTAGE LOCKOUT (Pin 8)					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	–	3.0	–	V
Hysteresis (V_{CC} Decreasing)	V_H	–	100	–	mV
TOTAL DEVICE (Pin 8)					
Power Supply Current (Pins 5, 6, 7 Open)	I_{CC}				mA
Startup (V_{CC} = 2.9 V)		–	0.65	–	
Operating (V_{CC} = 6.0 V)		–	0.61	–	

NOTES: 1. Whichever voltage is lower.
2. Tested ambient temperature range for the MC33340: T_{low} = −25°C T_{high} = +85°C
Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Battery Sense Input Thresholds versus Temperature

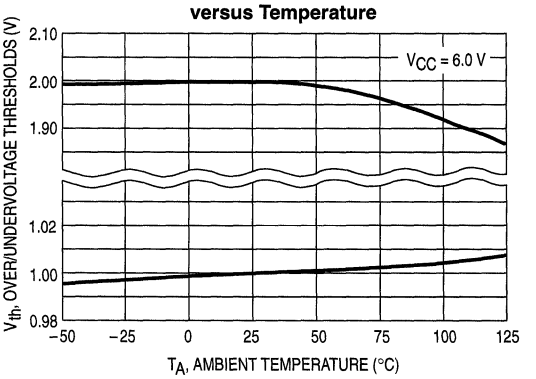


Figure 2. Oscillator Frequency versus Temperature

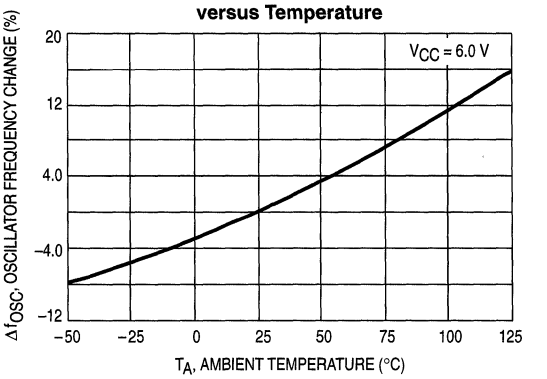


Figure 3. Temperature Select Threshold Voltage versus Temperature

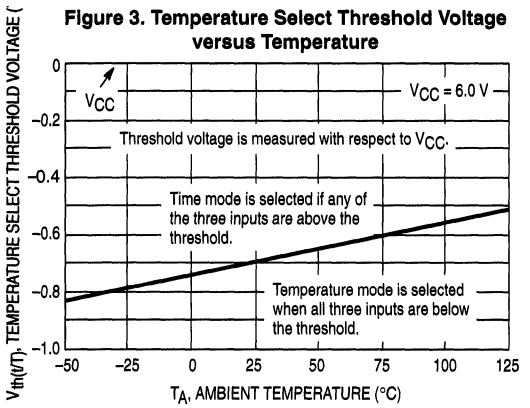


Figure 4. Saturation Voltage versus Sink Current V_{sen} Gate and Fast/Trickle Outputs

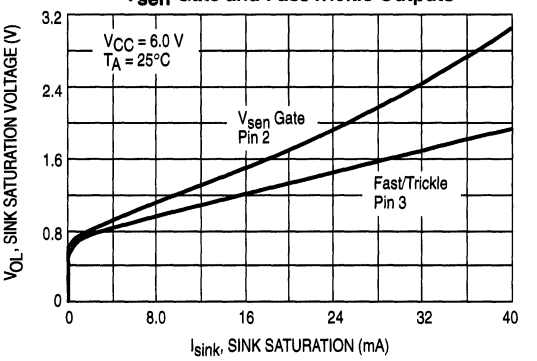


Figure 5. Undervoltage Lockout Thresholds versus Temperature

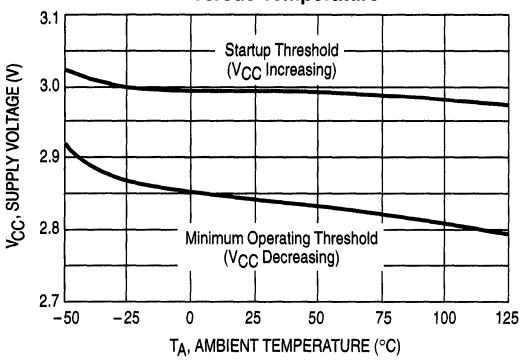
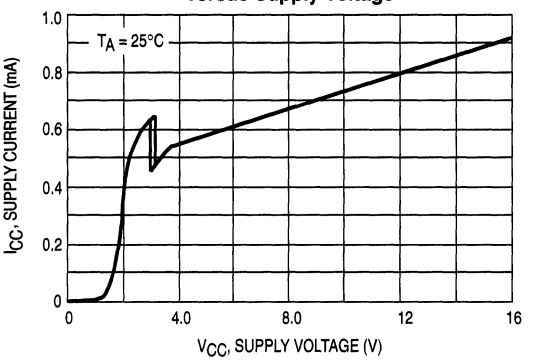


Figure 6. Supply Current versus Supply Voltage



INTRODUCTION

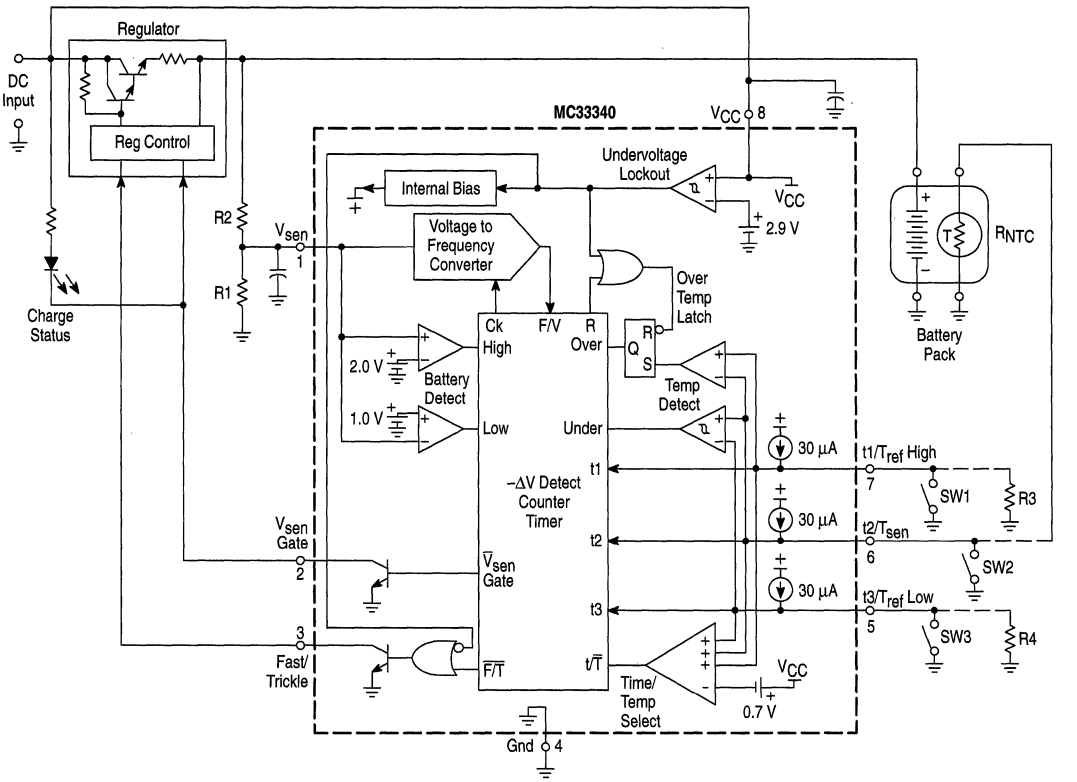
Nickel Cadmium and Nickel Metal Hydride batteries require precise charge termination control to maximize cell capacity and operating time while preventing overcharging. Overcharging can result in a reduction of battery life as well as physical harm to the end user. Since most portable applications require the batteries to be charged rapidly, a primary and usually a secondary or redundant charge sensing technique is employed into the charging system. It is also desirable to disable rapid charging if the battery voltage or temperature is either too high or too low. In order to address these issues, an economical and flexible fast charge controller was developed.

The MC33340 contains many of the building blocks and protection features that are employed in modern high performance battery charger controllers that are specifically designed for Nickel Cadmium and Nickel Metal Hydride batteries. The device is designed to interface with either primary or secondary side regulators for easy implementation of a complete charging system. A representative block diagram in a typical charging application is shown in Figure 7.

The battery voltage is monitored by the V_{sen} input that internally connects to a voltage to frequency converter and counter for detection of a negative slope in battery voltage. A timer with three programming inputs is available to provide backup charge termination. Alternatively, these inputs can be used to monitor the battery pack temperature and to set the over and under temperature limits also for backup charge termination.

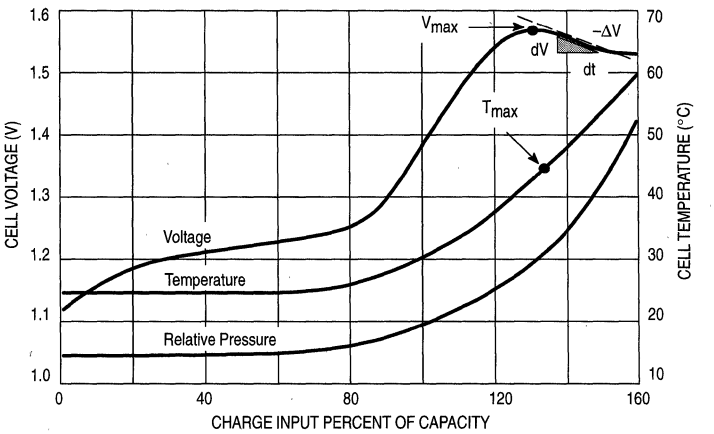
Two active low open collector outputs are provided to interface this controller with the external charging circuit. The first output furnishes a gating pulse that momentarily interrupts the charge current. This allows an accurate method of sampling the battery voltage by eliminating voltage drops that are associated with high charge currents and wiring resistances. Also, any noise voltages generated by the charging circuitry are eliminated. The second output is designed to switch the charging source between fast and trickle modes based upon the results of voltage, time, or temperature. These outputs normally connect directly to a linear or switching regulator control circuit in non–isolated primary or secondary side applications. Both outputs can be used to drive optoisolators in primary side applications that require galvanic isolation. Figure 8 shows the typical charge characteristics for NiCd and NiMh batteries.

Figure 7. Typical Battery Charging Application



$$R2 = R1\left(\frac{V_{Batt}}{V_{sen}} - 1\right)$$

Figure 8. Typical Charge Characteristics for NiCd and NiMh Batteries



OPERATING DESCRIPTION

The MC33340 starts up in the fast charge mode when power is applied to V_{CC}. A change to the trickle mode can occur as a result of three possible conditions. The first is if the V_{sen} input voltage is above 2.0 V or below 1.0 V. Above 2.0 V indicates that the battery pack is open or disconnected, while below 1.0 V indicates the possibility of a shorted or defective cell. The second condition is if a negative slope in battery voltage is detected after a minimum of 160 seconds of fast charging. This indicates that the battery pack is fully charged. The third condition is either due to the battery pack being out of a programmed temperature range, or that the preset timer period has been exceeded.

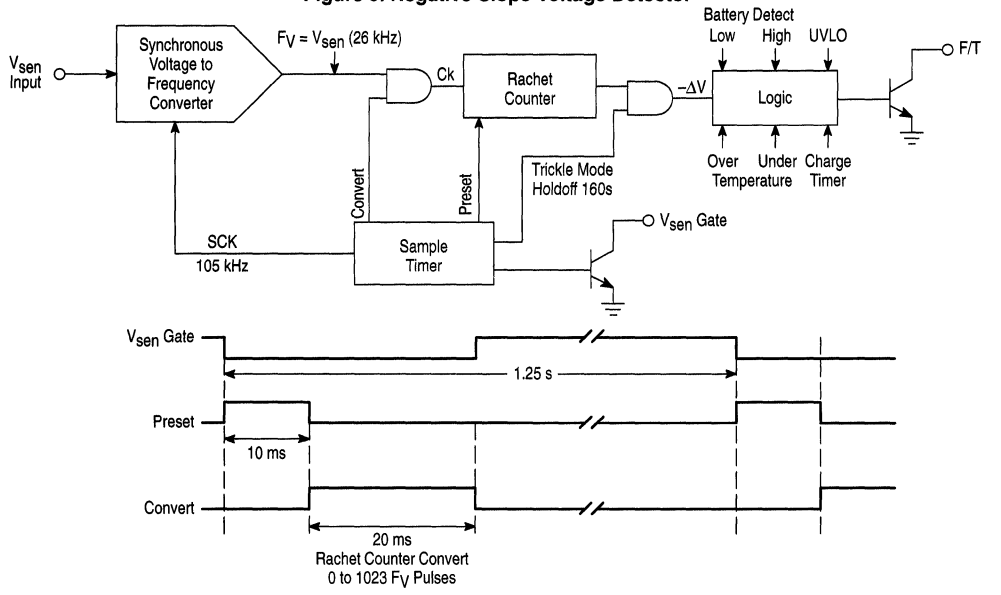
There are three conditions that will cause the controller to return from trickle to fast charge mode. The first is if the V_{sen} input voltage moved to within the 1.0 to 2.0 V range from initially being either too high or too low. The second is if the battery pack temperature moved to within the programmed temperature range, but only from initially being too cold. Third is by cycling V_{CC} off and then back on causing the internal logic to reset. A concise description of the major circuit blocks is given below.

Negative Slope Voltage Detection

A representative block diagram of the negative slope voltage detector is shown in Figure 9. It includes a Synchronous Voltage to Frequency Converter, a Sample Timer, and a Ratchet Counter. The V_{sen} pin is the input for the Voltage to Frequency Converter (VFC), and it connects to the rechargeable battery pack terminals through a resistive voltage divider. The input has an impedance of approximately 3.0 MΩ and a maximum voltage range of −1.0 V to V_{CC} + 0.6 V or 0 V to 10 V, whichever is lower. The 10 V upper limit is set by an internal zener clamp that provides protection in the event of an electrostatic discharge. The VFC is a charge–balanced synchronous type which generates output pulses at a rate of $F_V = V_{sen}$ (26 kHz).

The Sample Timer circuit provides a 105 kHz system clock signal (SCK) to the VFC. This signal synchronizes the F_V output to the other Sample Timer outputs used within the detector. At 1.25 second intervals the V_{sen} Gate output goes low for a 30 ms period. This output is used to momentarily interrupt the external charging power source so that a precise voltage measurement can be taken. As the V_{sen} Gate goes low, the internal Preset control line is driven high for 10 ms. During this time, the battery voltage at the V_{sen} input is allowed to stabilize and the previous F_V count is preloaded. At the Preset high–to–low transition, the Convert line goes high for 20 ms. This gates the F_V pulses into the ratchet counter for a comparison to the preloaded count. Since the Convert time is derived from the same clock that controls the VFC, the number of F_V pulses is independent of the clock frequency. If the new sample has more counts than were preloaded, it becomes the new peak count and the cycle is repeated 1.25 seconds later. If the new sample has two fewer counts, a less than peak voltage event has occurred, and a register is initialized. If two successive less than peak voltage events occur, the −ΔV 'AND' gate output goes high and the Fast/Trickle output is latched in a low state, signifying that the battery pack has reached full charge status. Negative slope voltage detection can only occur after 160 seconds have elapsed in the fast charge mode. The trickle mode holdoff time is implemented to ignore any initial drop in voltage that may occur when charging batteries that have been stored for an extended time period. The negative slope voltage detector has a maximum resolution of 2.0 V divided by 1023, or 1.955 mV per count with an uncertainty of ±1.0 count. In order to obtain maximum sensing accuracy, the R2/R1 voltage divider must be adjusted so that the V_{sen} input voltage is slightly less than 2.0 V when the battery pack is fully charged. Voltage variations due to temperature and cell manufacturing must be considered.

Figure 9. Negative Slope Voltage Detector



Fast Charge Timer

A programmable backup charge timer is available for fast charge termination. The timer is activated by the Time/Temp Select comparator, and is programmed from the $t1/T_{ref}$ High, $t2/T_{sen}$, and $t3/T_{ref}$ Low inputs. If one or more of these inputs is allowed to go above V_{CC} – 0.7 V or is left open, the comparator output will switch high, indicating that the timer feature is desired. The three inputs allow one of seven possible fast charge time limits to be selected. The programmable time limits, rounded to the nearest whole minute, are shown in Figure 10.

Over/Under Temperature Detection

A backup over/under temperature detector is available and can be used in place of the timer for fast charge termination. The timer is disabled by the Time/Temp Select comparator when each of the three programming inputs are held below V_{CC} – 0.7 V.

Temperature sensing is accomplished by placing a negative temperature coefficient (NTC) thermistor in thermal contact with the battery pack. The thermistor connects to the $t2/T_{sen}$ input which has a 30 μA current source pull–up for developing a temperature dependent voltage. The temperature limits are set by a resistor that connects from the $t1/T_{ref}$ High and the $t3/T_{ref}$ Low inputs to ground. Since all three inputs contain matched 30 μA current source pull–ups, the required programming resistor values are identical to that of the thermistor at the desired over and under trip temperature. The temperature window detector is composed of two comparators with a common input that connects to the $t2/T_{sen}$ input.

The lower comparator senses the presence of an under temperature condition. When the lower temperature limit is exceeded, the charger is switched to the trickle mode. The comparator has 44 mV of hysteresis to prevent erratic switching between the fast and trickle modes as the lower temperature limit is crossed. The amount of temperature rise to overcome the hysteresis is determined by the thermistor's rate of resistance change or sensitivity at the under temperature trip point. The required resistance change is:

$$\Delta R(T_{Low} \rightarrow T_{High}) = \frac{V_{H(T)}}{I_{in}} = \frac{44\ mV}{30\ \mu A} = 1.46\ k$$

The resistance change approximates a thermal hysteresis of 2°C with a 10 kΩ thermistor operating at 0°C. The under temperature fast charge inhibit feature can be disabled by biasing the $t3/T_{ref}$ Low input to a voltage that is greater than that present at $t2/T_{sen}$, and less than V_{CC} – 0.7 V. Under extremely cold conditions, it is possible that the thermistor resistance can become too high, allowing the $t2/T_{sen}$ input to go above V_{CC} – 0.7 V, and activate the timer. This condition can be prevented by placing a resistor in parallel with the thermistor. Note that the time/temperature threshold of V_{CC} – 0.7 V is a typical value at room temperature. Refer to the Electrical Characteristics table and to Figure 3 for additional information.

The upper comparator senses the presence of an over temperature condition. When the upper temperature limit is exceeded, the comparator output sets the Over Temperature Latch and the charger is switched to trickle mode. Once the latch is set, the charger cannot be returned to fast charge, even after the temperature falls below the limit. This feature prevents the battery pack from being continuously temperature cycled and overcharged. The latch can be reset by removing and reconnecting the battery pack or by cycling the power supply voltage.

If the charger does not require either the time or temperature backup features, they can both be easily disabled. This is accomplished by biasing the $t3/T_{ref}$ Low input to a voltage greater than $t2/T_{sen}$, and by grounding the $t1/T_{ref}$ High input. Under these conditions, the Time/Temp Select comparator output is low, indicating that the temperature mode is selected, and that the $t2/T_{sen}$ input is biased within the limits of an artificial temperature window.

Operating Logic

The order of events in the charging process is controlled by the logic circuitry. Each event is dependent upon the input conditions and the chosen method of charge termination. A table summary containing all of the possible operating modes is shown in Figure 11.

Figure 10. Fast Charge Backup Termination Time/Temperature Limit

Backup Termination Mode	Programming Inputs			Time Limit Fast Charge (Minutes)
	$t3/T_{ref}$ Low (Pin 5)	$t2/T_{sen}$ (Pin 6)	$t1/T_{ref}$ High (Pin 7)	
Time	Open	Open	Open	256
Time	Open	Open	Gnd	224
Time	Open	Gnd	Open	192
Time	Open	Gnd	Gnd	160
Time	Gnd	Open	Open	128
Time	Gnd	Open	Gnd	96
Time	Gnd	Gnd	Open	64
Temperature	0 V to V_{CC} – 0.7 V	0 V to V_{CC} – 0.7 V	0 V to V_{CC} – 0.7 V	Timer Disabled

Figure 11. Controller Operating Mode Table

Input Condition	Controller Operation
V_{sen} Input Voltage:	
>1.0 V and <2.0 V	The divided down battery pack voltage is within the fast charge voltage range. The charger switches from trickle to fast charge mode as V_{sen} enters this voltage range, and the reset signal that was applied to the timer and the over temperature latch is now released.
>1.0 V and <2.0 V with two consecutive $-\Delta V$ events detected after 160 s	The battery pack has reached full charge and the charger switches from fast to a latched trickle mode. A reset signal must be applied and then released for the charger to switch back to the fast mode. The reset signal is applied when either V_{sen} <1.0 V or >2.0 V, or V_{CC} <2.8 V. A signal is released when both V_{sen} >1.0 V and <2.0 V, and V_{CC} >3.0 V.
<1.0 V or >2.0 V	The divided down battery pack voltage is outside of the fast charge voltage range. The charger switches from fast to trickle mode, and a reset signal is applied to the timer and over temperature latch.
Timer Backup:	
Within time limit	The timer has not exceeded the programmed limit. The charger will be in fast charge mode if V_{sen} and V_{CC} are within their respective operating limits.
Beyond time limit	The timer has exceeded the programmed limit. The charger switches from fast to a latched trickle mode.
Temperature Backup:	
Within limits	The battery pack temperature is within the programmed limits. The charger will be in fast charge mode if V_{sen} and V_{CC} are within their respective operating limits.
Below lower limit	The battery pack temperature is below the programmed lower limit. The charger will stay in trickle mode until the lower temperature limit is exceeded. When exceeded, the charger will switch from trickle to fast charge mode.
Above upper limit	The battery pack temperature has exceeded the programmed upper limit. The charger switches from fast to a latched trickle mode. A reset signal must be applied and then released for the charger to switch back to the fast charge mode. A reset signal is applied when either V_{sen} <1.0 V or >2.0 V, or V_{CC} <2.8 V, and is released when both V_{sen} >1.0 V and <2.0 V, and V_{CC} >3.0 V.
Power Supply Voltage:	
V_{CC} >3.0 V and <18 V	This is the nominal power supply operating voltage range. The charger will be in fast charge mode if V_{sen}, and temperature backup or timer backup are within their respective operating limits.
V_{CC} >0.6 V and <2.8 V	The undervoltage lockout comparator will be activated and the charger will be in trickle mode. A reset signal is applied to the timer and over temperature latch.

Testing

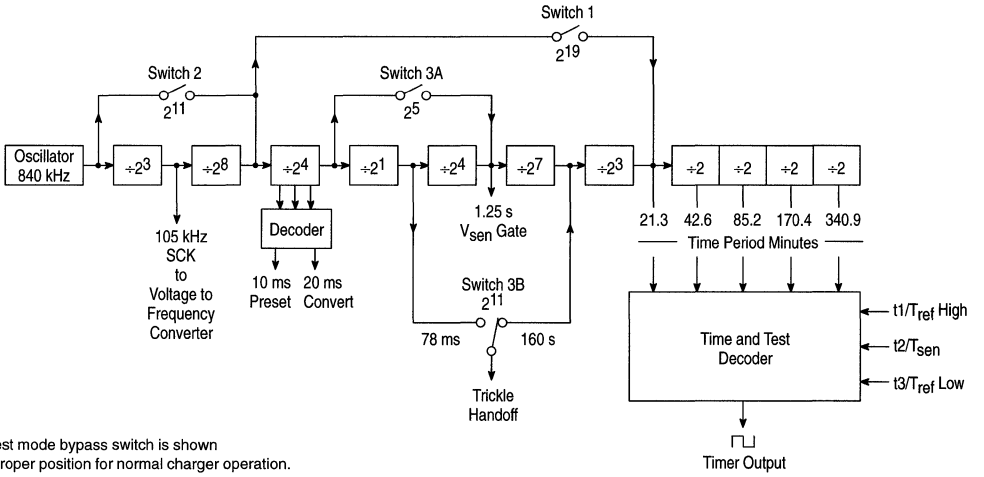
Under normal operating conditions, it would take 256 minutes to verify the operation of the 34 stage ripple counter used in the timer. In order to significantly reduce the test time, three digital switches were added to the circuitry and are used to bypass selected divider stages. Entering each of the test modes without requiring additional package pins or affecting normal device operation proved to be challenging. Refer to the timer functional block diagram in Figure 12.

Switch 1 bypasses 19 divider stages to provide a 524,288 times speedup of the clock. This switch is enabled when the V_{sen} input falls below 1.0 V. Verification of the programmed fast charge time limit is accomplished by measuring the propagation delay from when the V_{sen} input falls below 1.0 V, to when the F/T output changes from a high–to–low state. The 64, 96, 128, 160, 192, 224 and 256 minute timeouts will now correspond to 7.3, 11, 14.6, 18.3, 22, 25.6 and 29.3 ms delays. It is possible to enter this test mode during operation if the equivalent battery pack voltage was to fall below 1.0 V. This will not present a problem since the device would normally switch from fast to trickle mode under these conditions, and the relatively short variable time delay would be transparent to the user.

Switch 2 bypasses 11 divider stages to provide a 2048 times speedup of the clock. This switch is necessary for testing the 19 stages that were bypassed when switch 1 was enabled. Switch 2 is enabled when the V_{sen} input falls below 1.0 V and the $t1/T_{ref}$ Low input is biased at –100 mV. Verification of the 19 stages is accomplished by measuring a nominal propagation delay of 308 ms from when the V_{sen} input falls below 1.0 V, to when the F/T output changes from a high–to–low state.

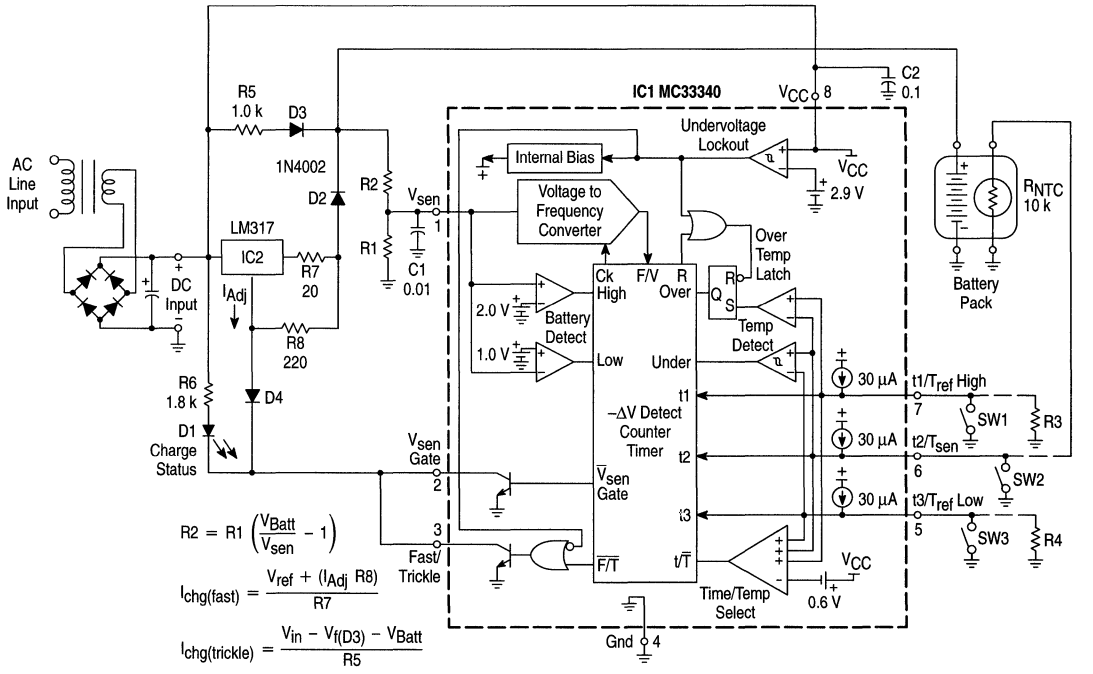
Switch 3 is a dual switch consisting of sections "A" and "B". Section "A" bypasses 5 divider stages to provide a 32 times speedup of the V_{sen} gate signal that is used in sampling the battery voltage. This speedup allows faster test verification of two successive $-\Delta V$ events. Section "B" bypasses 11 divider stages to provide a 2048 speedup of the trickle mode holdoff timer. Switches 3A and 3B are both activated when the $t1/T_{ref}$ Low input is biased at –100 mV with respect to Pin 4. Activation results in a reduction of the V_{sen} gate sample rate from 1.25 s to 39 ms, and a trickle mode holdoff time of 160 s to 68 ms.

Figure 12. Timer Functional Block Diagram



Each test mode bypass switch is shown
in the proper position for normal charger operation.

Figure 13. Line Isolated Linear Regulator Charger



This application combines the MC33340 with an adjustable three terminal regulator to form an isolated secondary side battery charger. Regulator IC2 operates as a constant current source with R7 setting the fast charge level. The trickle charge level is set by R5. The R2/R1 divider should be adjusted so that the V_{sen} input is less than 2.0 V when the batteries are fully charged. The printed circuit board shown below will accept the several TO–220 style heatsinks for IC2 and are all manufactured by AAVID Engineering Inc.

AAVID #	θ_{SA} °C/W
592502B03400	24.0
593002B03400	14.0
590302B03600	9.2

Figure 14. Printed Circuit Board and Component Layout (Circuit of Figure 13)

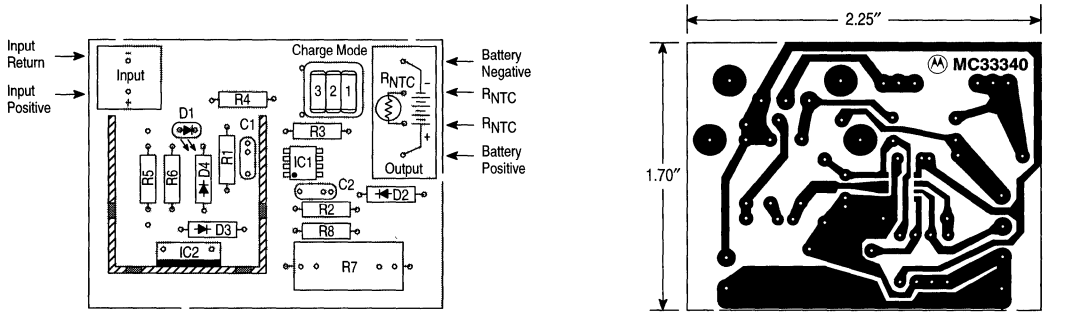
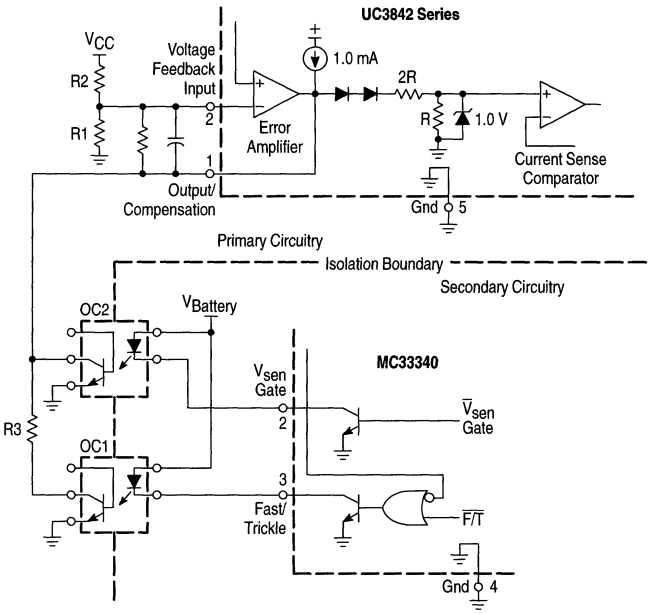
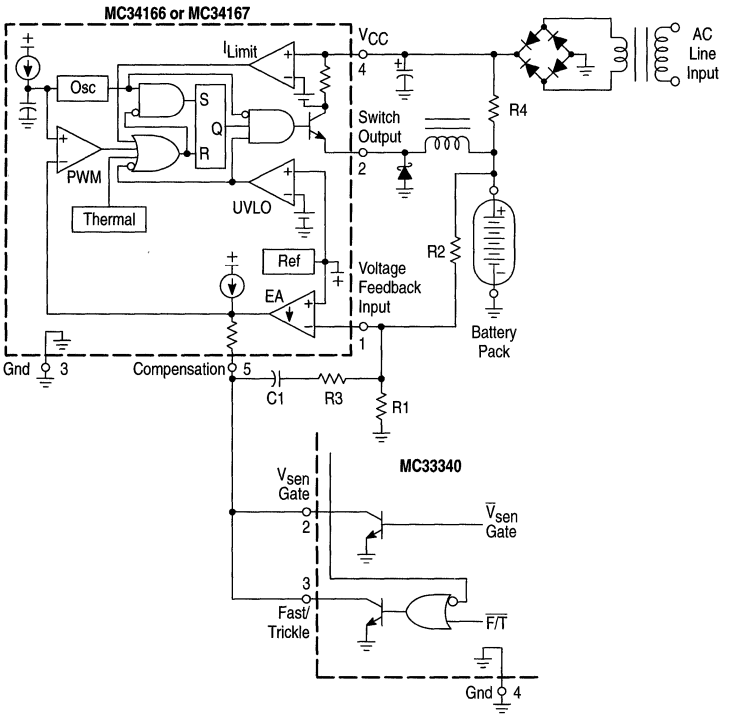


Figure 15. Line Isolated Switch Mode Charger



The MC33340 can be combined with any of the devices in the UC3842 family of current mode controllers to form a switch mode battery charger. In this example, optocouplers OC1 and OC2 are used to provide isolated control signals to the UC3842. During battery voltage sensing, OC2 momentarily grounds the Output/Compensation pin, effectively turning off the charger. When fast charge termination is reached, OC1 turns on, and grounds the lower side of R3. This reduces the peak switch current threshold of the Current Sense Comparator to a programmed trickle current level. For additional converter design information, refer to the UC3842 and UC3844 device family data sheets.

Figure 16. Switch Mode Fast Charger



The MC33340 can be used to control the MC34166 or MC34167 power switching regulators to produce an economical and efficient fast charger. These devices are capable of operating continuously in current limit with an input voltage range of 7.5 to 40 V. The typical charging current for the MC34166 and MC34167 is 4.3 A and 6.5 A respectively. Resistors R2 and R1 are used to set the battery pack fast charge float voltage. If precise float voltage control is not required, components R1, R2, R3 and C1 can be deleted, and Pin 1 must be grounded. The trickle current level is set by resistor R4. It is recommended that a redundant charge termination method be employed for end user protection. This is especially true for fast charger systems. For additional converter design information, refer to the MC34166 and MC34167 data sheets.

MOTOROLA

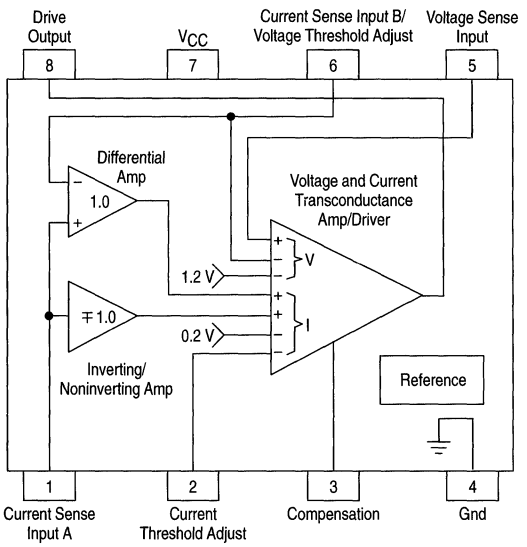
Product Preview

Power Supply Battery Charger Regulation Control Circuit

The MC33341 is a monolithic regulation control circuit that is specifically designed to close the voltage and current feedback loops in power supply and battery charger applications. This device features the unique ability to perform source high–side, load high–side, source low–side and load low–side current sensing, each with either an internally fixed or externally adjustable threshold. The various current sensing modes are accomplished by a means of selectively using the internal differential amplifier, inverting amplifier, or a direct input path. Positive voltage sensing is performed by an internal voltage amplifier. The voltage amplifier threshold is internally fixed and can be externally adjusted in all low–side current sensing applications. An active high drive output is provided to directly interface with economical optoisolators for isolated output power systems. This device is available in 8–lead dual–in–line and surface mount packages.

- Differential Amplifier for High–Side Source and Load Current Sensing
- Inverting Amplifier for Source Return Low–Side Current Sensing
- Non–Inverting Input Path for Load Low–Side Current Sensing
- Fixed or Adjustable Current Threshold in All Current Sensing Modes
- Positive Voltage Sensing in All Current Sensing Modes
- Fixed Voltage Threshold in All Current Sensing Modes
- Adjustable Voltage Threshold in All Low–Side Current Sensing Modes
- Output Driver Directly Interfaces with Economical Optoisolators
- Operating Voltage Range of 2.3 V to 18 V

Representative Block Diagram



This device contains 114 active transistors.

MC33341

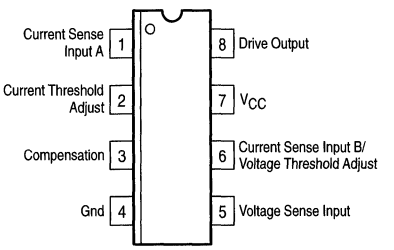
POWER SUPPLY BATTERY CHARGER REGULATION CONTROL CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33341D	T_A = –40° to +85°C	SO–8
MC33341P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 7)	V_{CC}	18	V
Voltage Range Current Sense Input A (Pin 1) Current Threshold Adjust (Pin 2) Compensation (Pin 3) Voltage Sense Input (Pin 5) Current Sense Input B/Voltage Threshold Adjust (Pin 6) Drive Output (Pin 8)	V_{IR}	−1.0 to V_{CC}	V
Drive Output Source Current (Pin 8)	I_{Source}	50	mA
Thermal Resistance, Junction–to–Air P Suffix, DIP Plastic Package, Case 626 D Suffix, SO–8 Plastic Package, Case 751	$R_{\theta JA}$	 100 178	°C/W
Operating Junction Temperature (Note 1)	T_J	−25 to +150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSING (Pins 1, 2, 6)					
Source High–Side and Load High–Side Sensing Pin 1 to Pin 6 (Pin 1 >1.6 V) Internally Fixed Threshold Voltage (Pin 2 = V_{CC}) T_A = 25°C T_A = T_{low} to T_{high} Externally Adjusted Threshold Voltage (Pin 2 = 0 V) Externally Adjusted Threshold Voltage (Pin 2 = 200 mV)	$V_{th(I\ HS)}$	 – – – –	 200 196 to 204 10 180	 – – – –	mV
Load Low–Side Sensing Pin 1 to Pin 4 (Pin 1 = 0 V to 0.8 V) Internally Fixed Threshold Voltage (Pin 2 = V_{CC}) T_A = 25°C T_A = T_{low} to T_{high} Externally Adjusted Threshold Voltage (Pin 2 = 0 V) Externally Adjusted Threshold Voltage (Pin 2 = 200 mV)	$V_{th(I\ LS+)}$	 – – – –	 200 196 to 204 10 180	 – – – –	mV
Source Return Low–Side Sensing Pin 1 to Pin 4 (Pin 1 = 0 V to −0.2 V) Internally Fixed Threshold Voltage (Pin 2 = V_{CC}) T_A = 25°C T_A = T_{low} to T_{high} Externally Adjusted Threshold Voltage (Pin 2 = 0 V) Externally Adjusted Threshold Voltage (Pin 2 = 200 mV)	$V_{th(I\ LS-)}$	 – – – –	 −200 −196 to −204 −10 −180	 – – – –	mV
Current Sense Input A (Pin 1) Input Bias Current, High–Side Source and Load Sensing (Pin 2 = 0 V to $V_{Pin\ 6}$ V) Input Bias Current, Low–Side Load Sensing (Pin 2 = 0 V to 0.8 V) Input Resistance, Low–Side Source Return Sensing (Pin 2 = −0.6 V to 0 V)	 $I_{IB(A\ HS)}$ $I_{IB(A\ LS+)}$ $R_{in(A\ LS-)}$	 – – –	 40 10 10	 – – –	 µA nA kΩ
Current Sense Input B/Voltage Threshold Adjust (Pin 6) Input Bias Current High–Side Source and Load Current Sensing (Pin 6 > 2.0 V) Voltage Threshold Adjust (Pin 6 < 1.2 V)	$I_{IB(B)}$	 – –	 20 100	 – –	 µA nA
Current Sense Threshold Adjust (Pin 2) Input Bias Current	$I_{IB(I\ th)}$	–	10	–	nA
Transconductance, Current Sensing Inputs to Drive Output (I_O − 0.7 mA)	$g_{m(I)}$	–	6.0	–	mhos

NOTE: 1. Tested ambient temperature range for the MC33341: T_{low} = −25°C, T_{high} = +85°C.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 6.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DIFFERENTIAL AMPLIFIER DISABLE LOGIC (Pins 1, 6)					
Logic Threshold Voltage Pin 1 (Pin 6 = 0 V)					V
Enabled, High–Side Source and Load Current Sensing	$V_{th(I\ HS)}$	–	1.2	–	
Disabled, Low–Side Load and Source Return Current Sensing	$V_{th(I\ LS)}$	–	1.2	–	
VOLTAGE SENSING (Pins 5, 6)					
Positive Sensing Pin 5 to Pin 4					
Internally Fixed Threshold Voltage	$V_{th(V)}$				
T_A = 25°C		–	1.200	–	V
T_A = T_{low} to T_{high}		–	1.176 to 1.224	–	mV
Externally Adjusted Threshold Voltage (Pin 6 = 0 V)		–	40	–	V
Externally Adjusted Threshold Voltage (Pin 6 = 1.2 V)		–	1.175	–	
Voltage Sense, Input Bias Current (Pin 5)	$I_{IB(V)}$	–	10	–	nA
Transconductance, Voltage Sensing Inputs to Drive Output (I_O = 0.7 mA)	$g_{m(V)}$	–	7.0	–	mhos
DRIVE OUTPUT (Pin 8)					
High State Source Voltage (I_{Source} = 8.0 mA)	V_{OH}	–	V_{CC} – 0.8	–	V
TOTAL DEVICE (Pin 7)					
Operating Voltage Range	V_{CC}	–	2.3 to 18	–	V
Power Supply Current (V_{CC} = 6.0 V)	I_{CC}	–	300	–	μA

NOTE: 1. Tested ambient temperature range for the MC33341: T_{low} = –25°C, T_{high} = +85°C.

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	Current Sense Input A	This multi–mode current sensing input can be used for either source high–side, load high–side, source–return low–side, or load low–side sensing. It is common to a Differential Amplifier, Inverting Amplifier, and a Noninverting input path. Each of these sensing paths indirectly connect to the current sense input of the Transconductance Amplifier. This input is connected to the high potential side of a current sense resistor when used in source high–side, load high–side, or load low–side current sensing modes. In source return low–side current sensing mode, this pin connects to the low potential side of a current sense resistor.
2	Current Threshold Adjust	The current sense threshold can be externally adjusted over a range of 0 V to 200 mV with respect to Pin 4, or internally fixed at 200 mV by connecting Pin 2 to V_{CC}.
3	Compensation	This pin is connected to a high impedance node within the transconductance amplifier and is made available for loop compensation. It can also be used as an input to directly control the Drive Output. An active low at this pin will force the Drive Output into a high state.
4	Ground	This pin is the regulation control IC ground. The control threshold voltages are with respect to this pin.
5	Voltage Sense Input	This is the voltage sensing input of the Transconductance Amplifier. It is normally connected to the power supply/battery charger output through a resistor divider. The input threshold is controlled by Pin 6.
6	Current Sense Input B/ Voltage Threshold Adjust	This is a dual function input that is used for either high–side current sensing, or as a voltage threshold adjustment for Pin 5. This input is connected to the low potential side of a current sense resistor when used in source high–side or load high–side current sensing modes. In all low–side current sensing modes, Pin 6 is available as a voltage threshold adjustment for Pin 5. The threshold can be externally adjusted over a range of 0 V to 1.2 V with respect to Pin 4, or internally fixed at 1.2 V by connecting Pin 6 to V_{CC}.
7	V_{CC}	This is the positive supply voltage for the regulation control IC. The typical operating voltage range is 2.3 V to 18 V with respect to Pin 4.
8	Drive Output	This is a source–only output that normally connects to a linear or switching regulator control circuit. This output is capable of 15 mA, allowing it to directly drive an optoisolator in primary side control applications where galvanic isolation is required.

Figure 1. Voltage Sensing Threshold Change versus Temperature

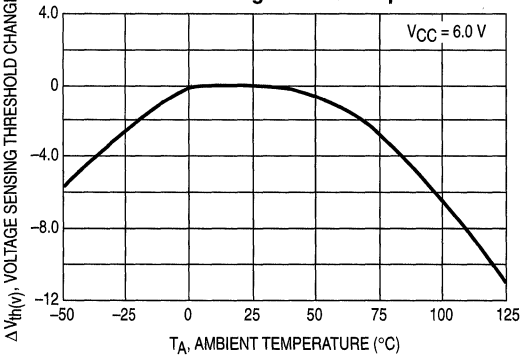


Figure 2. Current Sensing Threshold Change versus Temperature

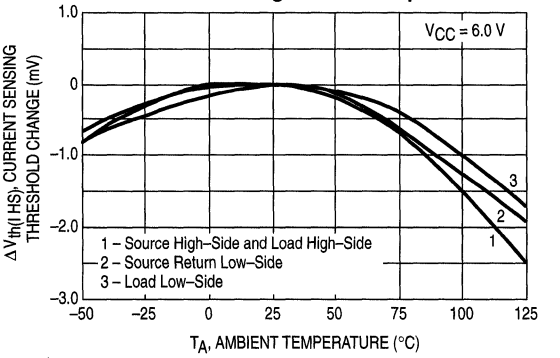


Figure 3. Closed–Loop Voltage Sensing Input versus Voltage Threshold Adjust

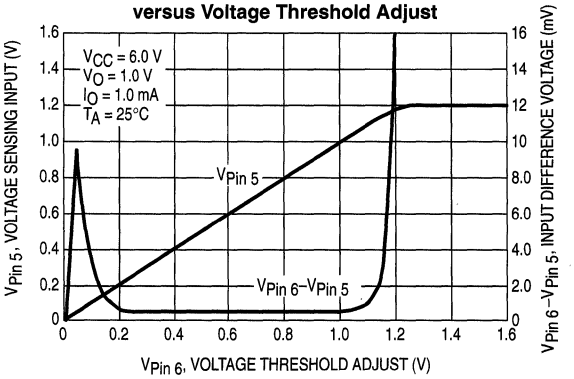


Figure 4. Closed–Loop Current Sense Input B versus Current Threshold Adjust

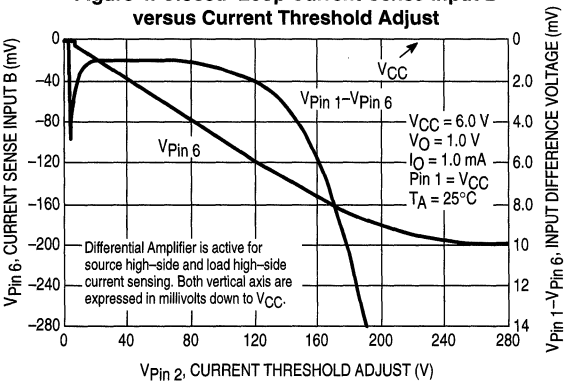


Figure 5. Closed–Loop Current Sensing Input A versus Current Threshold Adjust

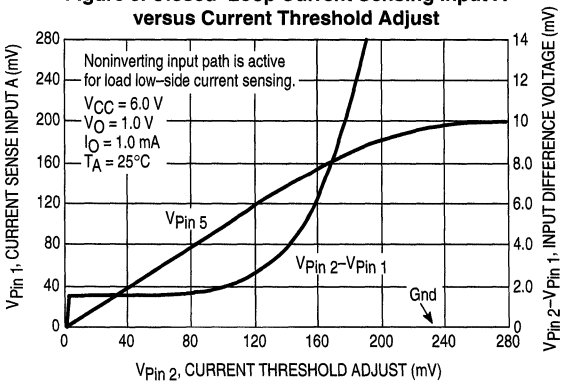


Figure 6. Closed–Loop Current Sensing Input A versus Current Threshold Adjust

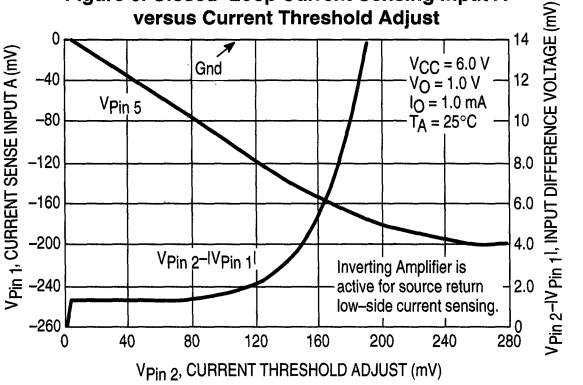


Figure 7. Bode Plot
Voltage Sensing Inputs to Drive Output

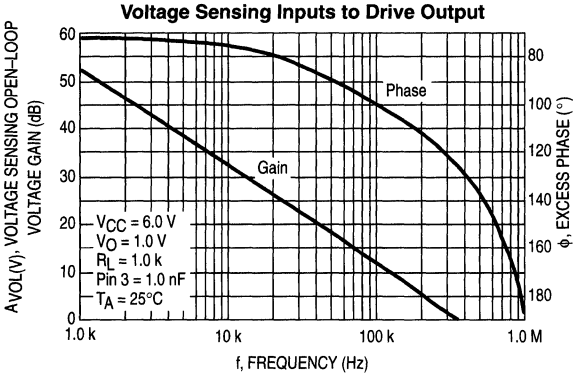


Figure 8. Bode Plot
Current Sensing Inputs to Drive Output

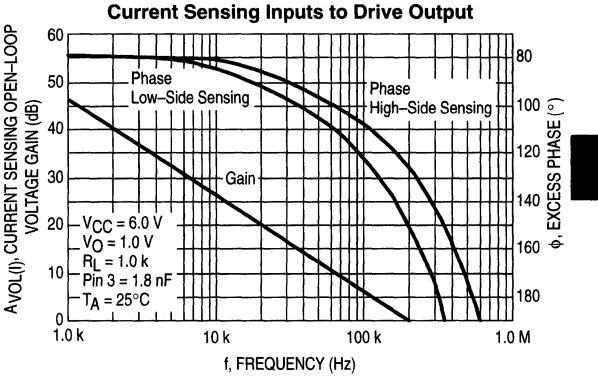


Figure 9. Transconductance
Voltage Sensing Inputs to Drive Output

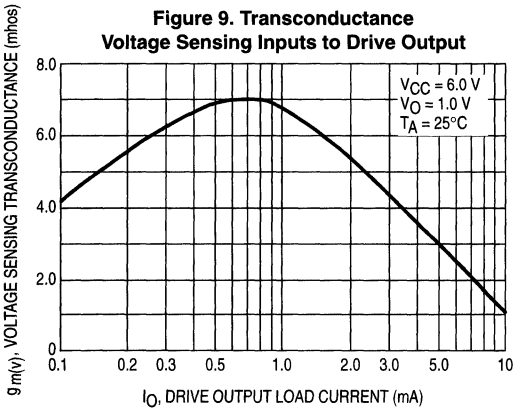


Figure 10. Transconductance
Current Sensing Inputs to Drive Output

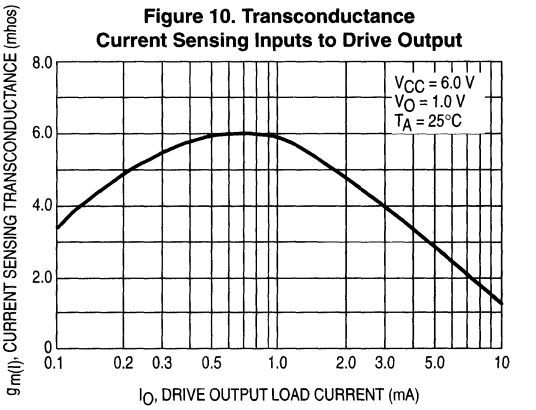


Figure 11. Drive Output High State
Source Saturation versus Load Current

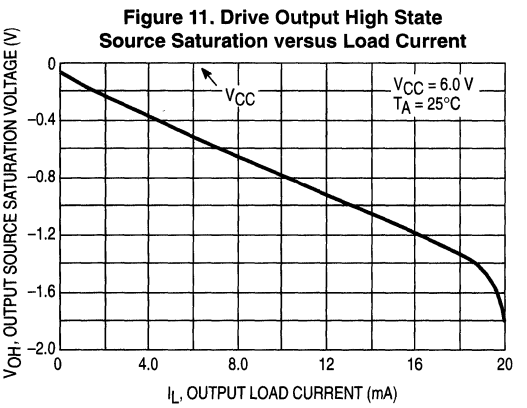
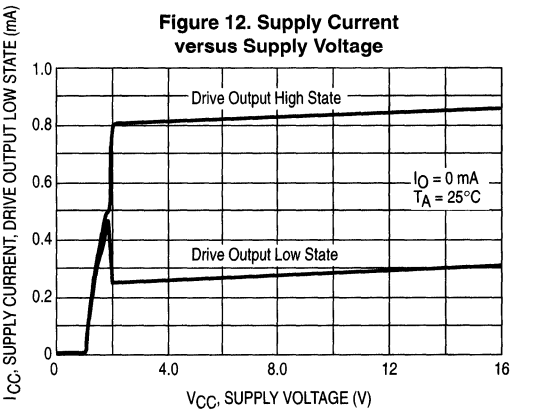


Figure 12. Supply Current
versus Supply Voltage



INTRODUCTION

Power supplies and battery chargers require precise control of output voltage and current in order to prevent catastrophic damage to the system load. Many present day power sources contain a wide assortment of building blocks and glue devices to perform the required sensing for proper regulation. Typical feedback loop circuits may consist of a voltage and current amplifier, level shifting circuitry, summing circuitry and a reference. The MC33341 contains all of these basic functions in a manner that is easily adaptable to many of the various power source–load configurations.

3

OPERATING DESCRIPTION

The MC33341 is an analog regulation control circuit that is specifically designed to simultaneously close the voltage and current feedback loops in power supply and battery charger applications. This device can control the feedback loop in either constant–voltage or constant–current mode with automatic crossover. A concise description of the integrated circuit blocks is given below. Refer to the block diagram in Figure 13.

Transconductance Amplifier

A quad input transconductance amplifier is used to control the feedback loop. This amplifier has separate voltage and current channels, each with a sense and a threshold input. Within a given channel, if the sense input level exceeds that of the threshold input, the amplifier output is driven high. The channel with the largest difference between the sense and threshold inputs will set the output source current of the amplifier and thus dominate control of the feedback loop. The amplifier output appears at Pin 8 and is a source–only type that is capable of 15 mA.

A high impedance node within the transconductance amplifier is made available at Pin 3 for loop compensation. This pin can sink and source up to 10 μA of current. System stability is achieved by connecting a capacitor from Pin 3 to ground. The Compensation Pin signal is out of phase with respect to the Drive Output. By actively clamping Pin 3 low, the Drive Output is forced into a high state. This, in effect, will shutdown the power supply or battery charger, by forcing the output voltage and current regulation threshold down towards zero.

Voltage Sensing

The voltage that appears across the load is monitored by the noninverting V_{sen} input of the transconductance amplifier. This voltage is resistively scaled down and connected to Pin 5. The threshold at which voltage regulation occurs is set by the level present at the inverting V_{th} input of the transconductance amplifier. This level is controlled by Pin 6. In source high–side and load high–side current sensing modes, Pin 6 must be connected to the low potential side of current sense resistor R_S. Under these conditions, the voltage regulation threshold is internally fixed at 1.2 V. In source return low–side and load low–side current sensing modes, Pin 6 is available, and can be used to lower the regulation threshold of Pin 5. This threshold can be externally adjusted over a range of 0 V to 1.2 V with respect to the IC ground at Pin 4.

Current Sensing

Current sensing is accomplished by monitoring the voltage that appears across sense resistor R_S, level shifting it with respect to Pin 4 if required, and applying it to the noninverting I_{sen} input of the transconductance amplifier. In order to allow for maximum circuit flexibility, there are three methods of current sensing, each with different internal paths.

In source high–side (Figures 13 and 14) and load high–side (Figures 17 and 18) current sensing, the Differential Amplifier is active with a gain of 1.0. Pin 1 connects to the high potential side of current sense resistor R_S while Pin 6 connects to the low side. Logic circuitry is provided to disable the Differential Amplifier output whenever low–side current sensing is required. This circuit clamps the Differential Amplifier output high which disconnects it from the I_{sen} input of the Transconductance Amplifier. This happens if Pin 1 is less than 1.2 V or if Pin 1 is less than Pin 6.

With source return low–side current sensing (Figures 15 and 16), the Inverting Amplifier is active with a gain of –1.0. Pin 1 connects to the low potential side of current sense resistor R_S while Pin 4 connects to the high side. Note that a negative voltage appears across R_S with respect to Pin 4.

In load low–side current sensing (Figures 19 and 20) a Noninverting input path is active with a gain of 1.0. Pin 1 connects to the high potential side of current sense resistor R_S while Pin 4 connects to the low side. The Noninverting input path lies from Pin 1, through the Inverting Amplifier input and feedback resistors R, to the cathode of the output diode. With load low–side current sensing, Pin 1 will be more positive than Pin 4, forcing the Inverting Amplifier output low. This causes the diode to be reverse biased, thus preventing the output stage of the amplifier from loading the input signal that is flowing through the feedback resistors.

The regulation threshold in all of the current sensing modes is internally fixed at 200 mV with Pin 2 connected to V_{CC}. Pin 2 can be used to externally adjust the threshold over a range of 0 to 200 mV with respect to the IC ground at Pin 4.

Reference

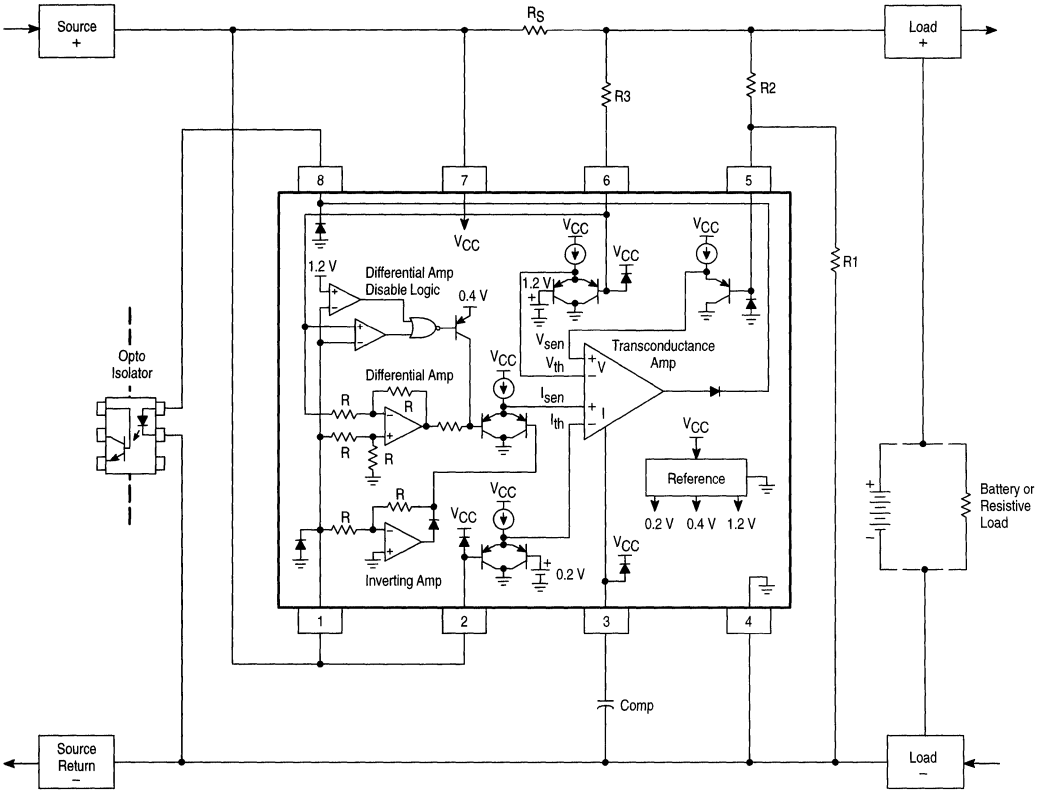
An internal band gap reference is used to set the 1.2 V voltage threshold and 200 mV current threshold. The reference is initially trimmed to a ±1.0% tolerance at T_A = 25°C and is guaranteed to be within ±2.0% over an ambient operating temperature range of –25° to 85°C.

Applications

Each of the application circuits illustrate the flexibility of this device. The circuits shown in Figures 13 through 20 contain an optoisolator connected from the Drive Output at Pin 8 to ground. This configuration is shown for ease of understanding and would normally be used to provide an isolated control signal to a primary side switching regulator controller. In non–isolated, primary or secondary side applications, a load resistor can be placed from Pin 8 to ground. This resistor will convert the Drive Output current to a voltage for direct control of a regulator.

In applications where excessively high peak currents are possible from the source or load, the load induced voltage drop across R_S could exceed 1.6 V. Depending upon the current sensing configuration used, this will result in forward biasing of either the internal V_{CC} clamp diode, Pin 6, or the device substrate, Pin 1. Under these conditions, input series resistor R3 is required. The peak input current should be limited to 20 mA. Excessively large values for R3 will degrade the current sensing accuracy. Figure 21 shows a method of bounding the voltage drop across R_S without sacrificing current sensing accuracy.

Figure 13. Source High–Side Current Sensing with Internally Fixed Voltage and Current Thresholds



The above figure shows the MC33341 configured for source high–side current sensing allowing a common ground path between Load – and Source Return –. The Differential Amplifier inputs, Pins 1 and 6, are used to sense the load induced voltage drop that appears across resistor R_S. The internal voltage and current regulation thresholds are selected by the respective external connections of Pins 2 and 6. Resistor R3 is required in applications where a high peak level of reverse current is possible if the source inputs are shorted. The resistor value should be chosen to limit the input current of the internal V_{CC} clamp diode to less than 20 mA. Excessively large values for R3 will degrade the current sensing accuracy.

$$V_{reg} = V_{th(V)}\left(\frac{R2}{R1} + 1\right)$$

$$= 1.2\left(\frac{R2}{R1} + 1\right)$$

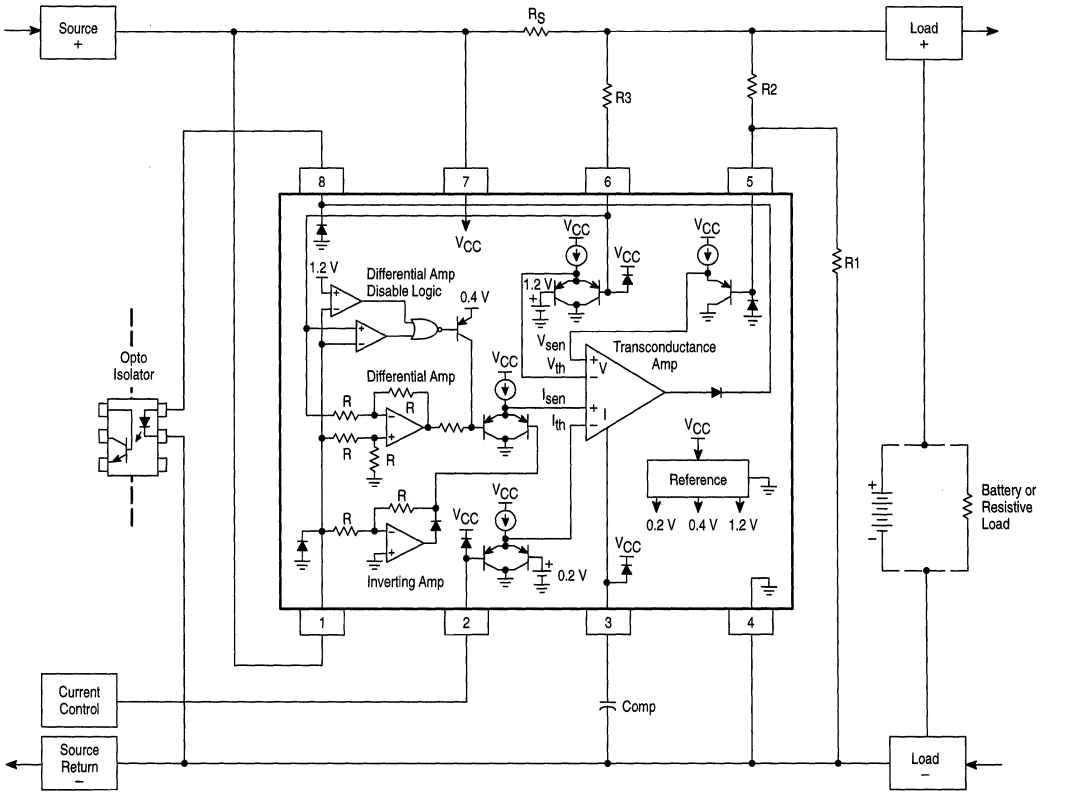
$$I_{reg} = \frac{V_{th(I\,HS)}}{R_S}$$

$$= \frac{0.2}{R_S}$$

$$R3 = \frac{\left(I_{pk}\,R_S\right) - 0.6}{0.02}$$

3

Figure 14. Source High–Side Current Sensing with Externally Adjustable Current and Internally Fixed Voltage Thresholds



The above figure shows the MC33341 configured for source high–side current sensing with an externally adjustable current threshold. Operation of this circuit is similar to that of Figure 13. The current regulation threshold can be adjusted over a range of 0 V to 200 mV with respect to Pin 4.

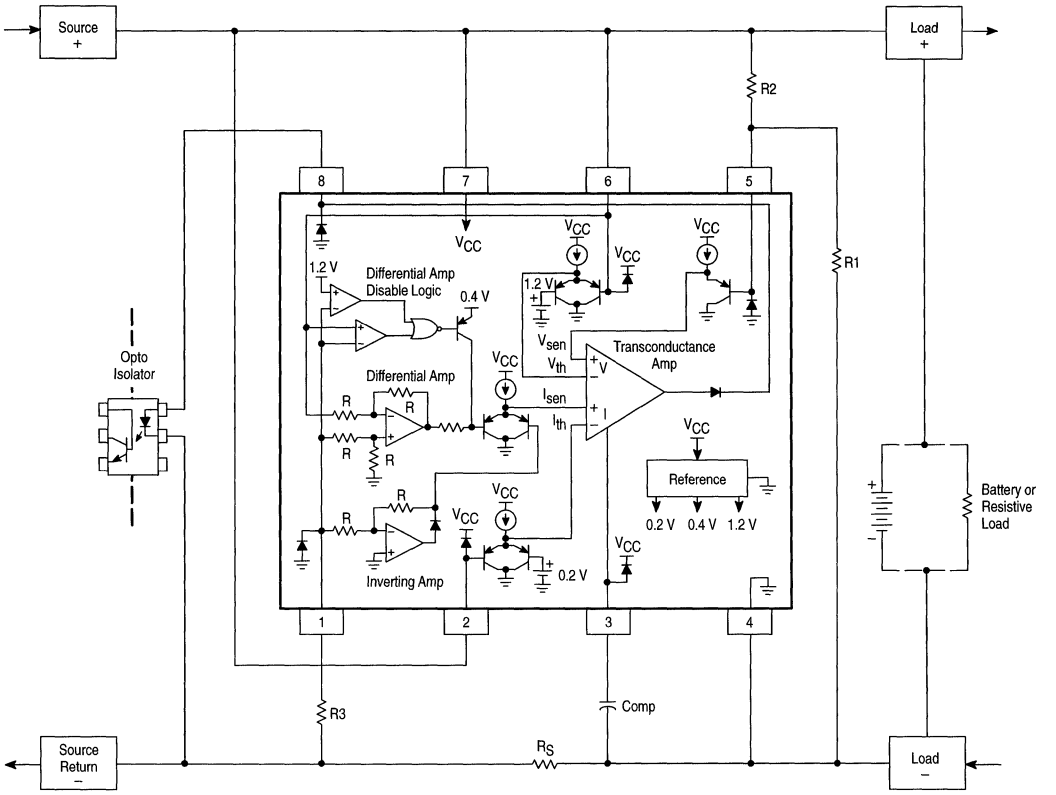
$$V_{reg} = V_{th(V)}\left(\frac{R2}{R1} + 1\right)$$

$$= 1.2\left(\frac{R2}{R1} + 1\right)$$

$$I_{reg} = \frac{V_{th(Pin\ 2)}}{R_S}$$

$$R3 = \frac{\left(I_{pk} R_S\right) - 0.6}{0.02}$$

Figure 15. Source Return Low–Side Current Sensing with Internally Fixed Current and Voltage Thresholds



The above figure shows the MC33341 configured for source return low–side current sensing allowing a common power path between Source + and Load +. This configuration is especially suited for negative output applications where a common ground path, Source + to Load +, is desired. The Inverting Amplifier inputs, Pins 1 and 4, are used to sense the load induced voltage drop that appears across resistor R_S. The internal voltage and current regulation thresholds are selected by the respective external connections of Pins 2 and 6. Resistor R3 is required in applications where high peak levels of inrush current are possible. The resistor value should be chosen to limit the negative substrate current to less than 20 mA. Excessively large values for R3 will degrade the current sensing accuracy.

$$V_{reg} = V_{th(V)}\left(\frac{R2}{R1} + 1\right)$$

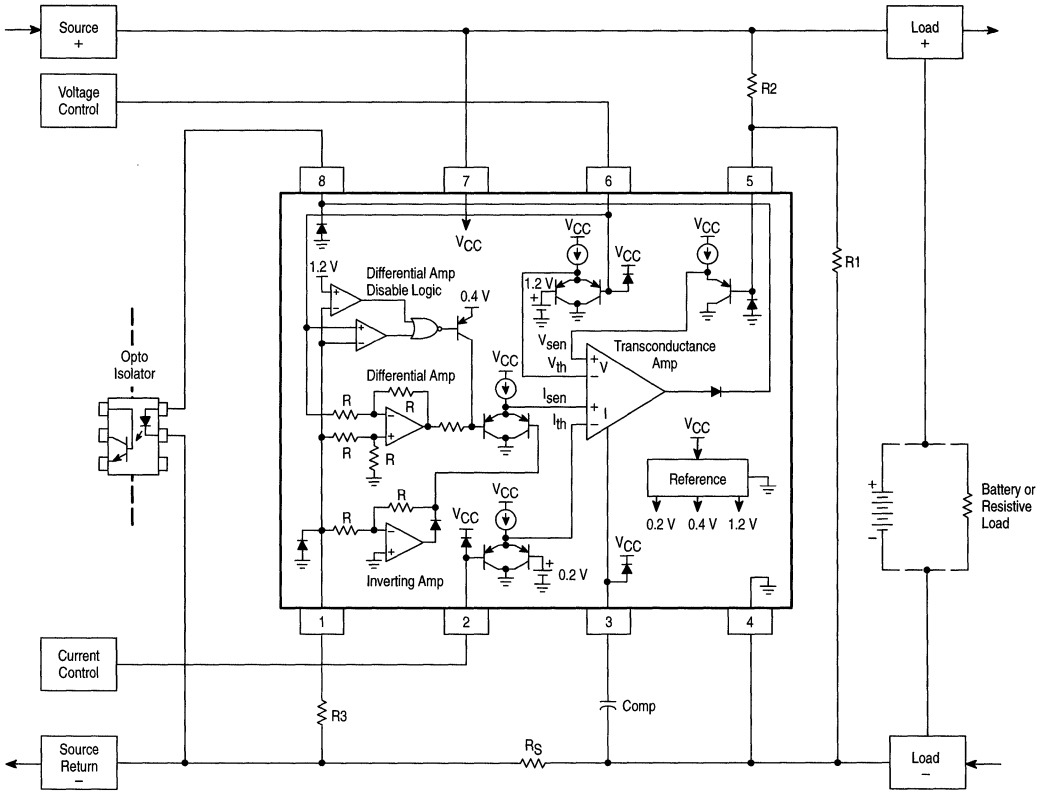
$$= 1.2\left(\frac{R2}{R1} + 1\right)$$

$$I_{reg} = \frac{V_{th(I\,LS-)}}{R_S}$$

$$= \frac{-0.2}{R_S}$$

$$R3 = \frac{\left(I_{pk}\,R_S\right) - 0.6}{0.02}$$

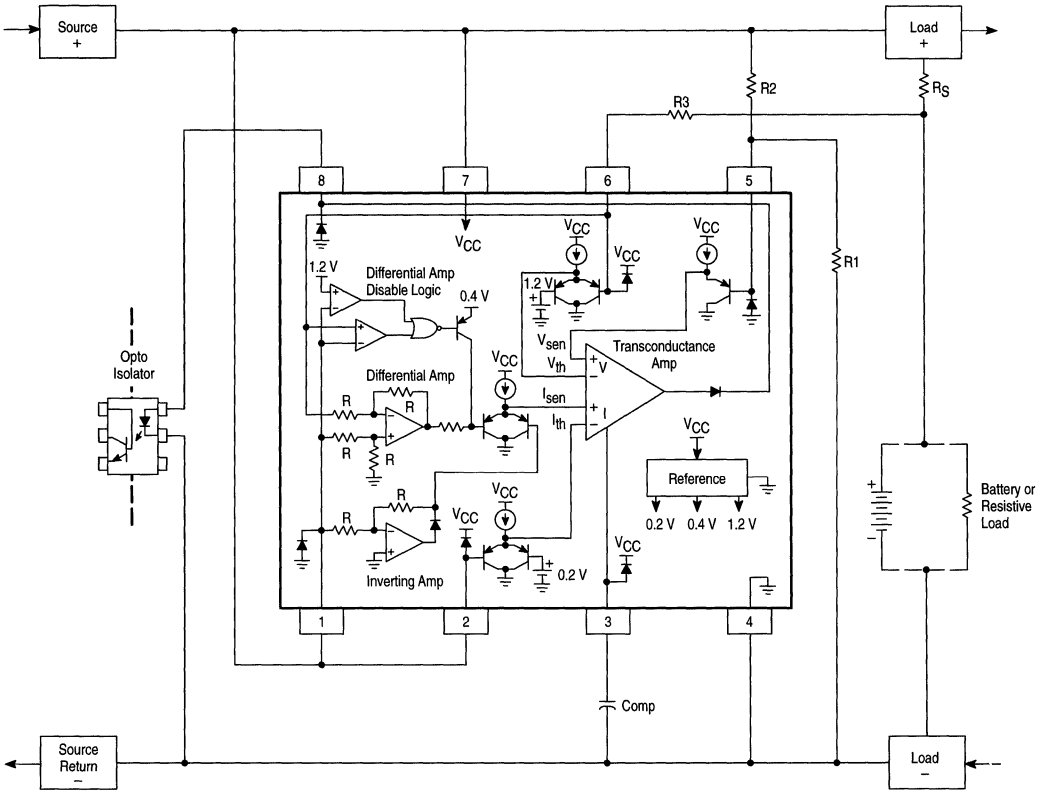
Figure 16. Source Return Low–Side Current Sensing with Externally Adjustable Current and Voltage Thresholds



The above figure shows the MC33341 configured for source return low–side current sensing with externally adjustable voltage and current thresholds. Operation of this circuit is similar to that of Figure 15. The respective voltage and current regulation threshold can be adjusted over a range of 0 to 1.6 V and 0 V to 200 mV with respect to Pin 4.

$$V_{reg} = V_{th(Pin\ 6)}\left(\frac{R2}{R1} + 1\right) \qquad I_{reg} = -\frac{V_{th(Pin\ 2)}}{R_S} \qquad R3 = \frac{\left(I_{pk}\,R_S\right) - 0.6}{0.02}$$

Figure 17. Load High–Side Current Sensing with Internally Fixed Current and Voltage Thresholds



The above figure shows the MC33341 configured for load high–side current sensing allowing common paths for both power and ground, between the source and load. The Differential Amplifier inputs, Pins 1 and 6, are used to sense the load induced voltage drop that appears across resistor R_S. The internal voltage and current regulation thresholds are selected by the respective external connections of Pins 2 and 6. Resistor R3 is required in applications where high peak levels of load current are possible from the battery or load bypass capacitor. The resistor value should be chosen to limit the input current of the internal V_{CC} clamp diode to less than 20 mA. Excessively large values for R3 ill degrade the current sensing accuracy.

$$V_{reg} = V_{th(V)}\left(\frac{R2}{R1} + 1\right)$$

$$= 1.2\left(\frac{R2}{R1} + 1\right)$$

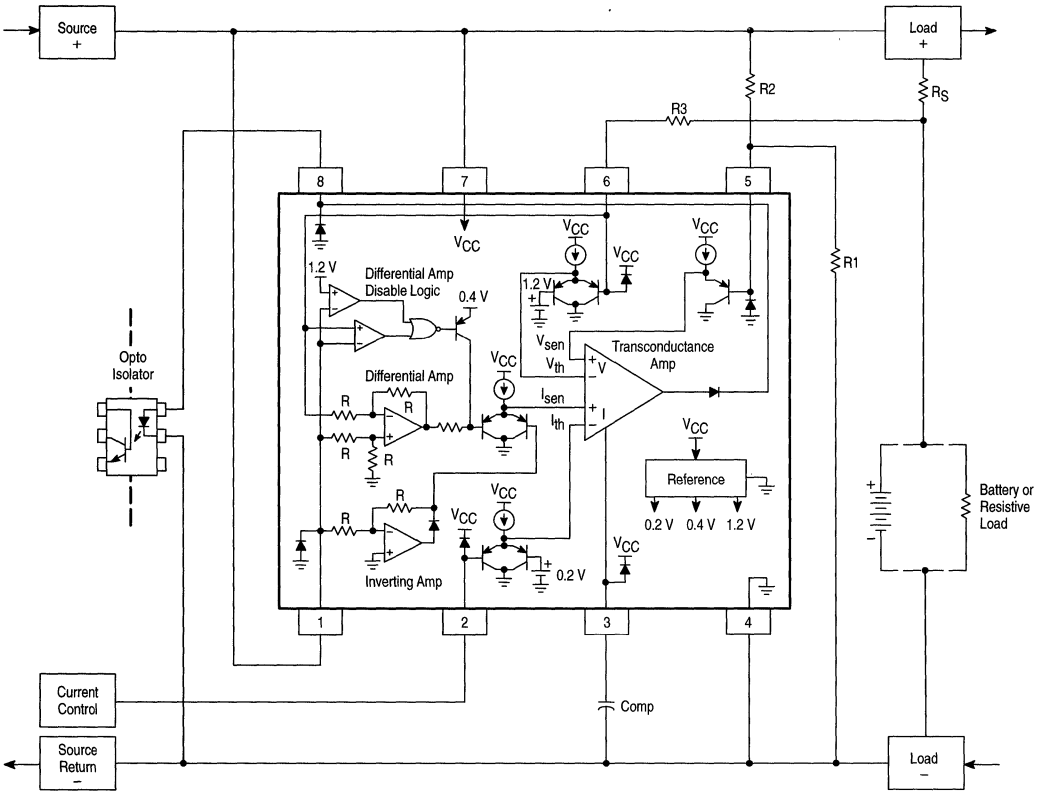
$$I_{reg} = \frac{V_{th(I\,HS)}}{R_S}$$

$$= \frac{0.2}{R_S}$$

$$R3 = \frac{\left(I_{pk} R_S\right) - 0.6}{0.02}$$

3

Figure 18. Load High–Side Current Sensing with Externally Adjustable Current and Internally Fixed Voltage Thresholds



The above figure shows the MC33341 configured for load high–side current sensing with an externally adjustable current threshold. Operation of this circuit is similar to that of Figure 17. The current regulation threshold can be adjusted over a range of 0 V to 200 mV with respect to Pin 4.

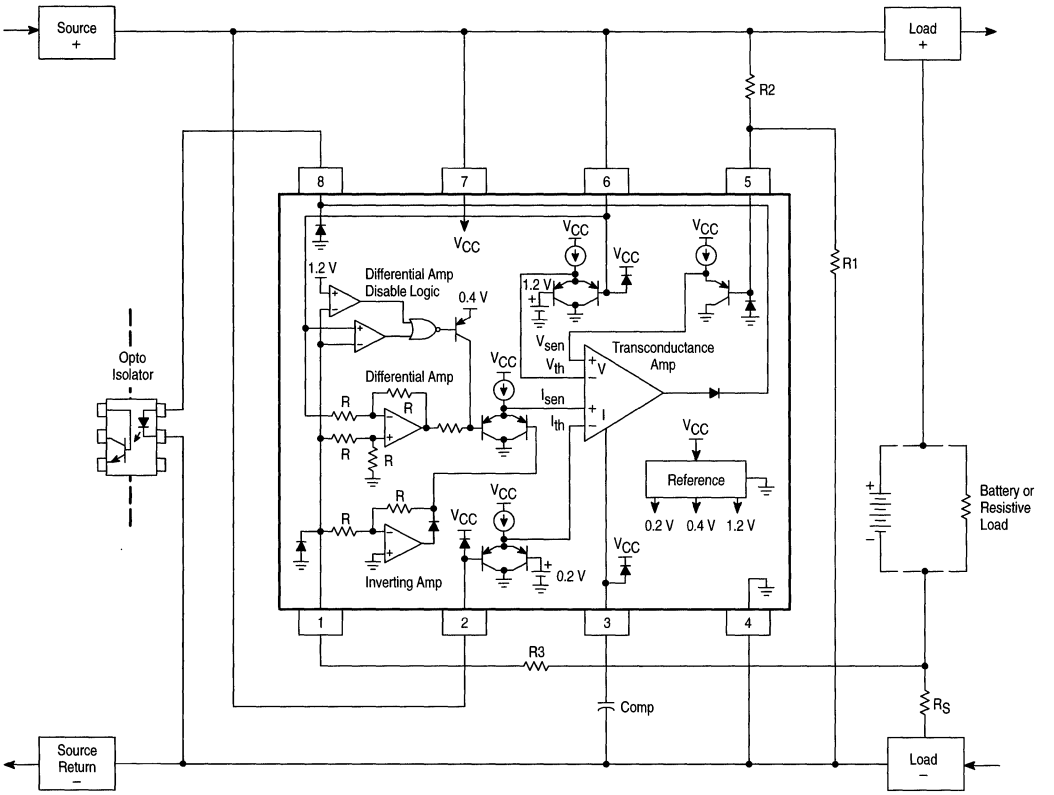
$$V_{reg} = V_{th(V)}\left(\frac{R2}{R1} + 1\right)$$

$$= 1.2\left(\frac{R2}{R1} + 1\right)$$

$$I_{reg} = \frac{V_{th(Pin\ 2)}}{R_S}$$

$$R3 = \frac{\left(I_{pk} R_S\right) - 0.6}{0.02}$$

Figure 19. Load Low–Side Current Sensing with Internally Fixed Current and Voltage Thresholds



The above figure shows the MC33341 configured for load low–side current sensing allowing common paths for both power and ground, between the source and load. The Noninverting input paths, Pins 1 and 4, are used to sense the load induced voltage drop that appears across resistor R_S. The internal voltage and current regulation thresholds are selected by the respective external connections of Pins 2 and 6. Resistor R3 is required in applications where high peak levels of load current are possible from the battery or load bypass capacitor. The resistor value should be chosen to limit the negative substratecurrent to less than 20 mA. Excessively large values for R3 will degrade the current sensing accuracy.

$$V_{reg} = V_{th(V)}\left(\frac{R2}{R1} + 1\right)$$

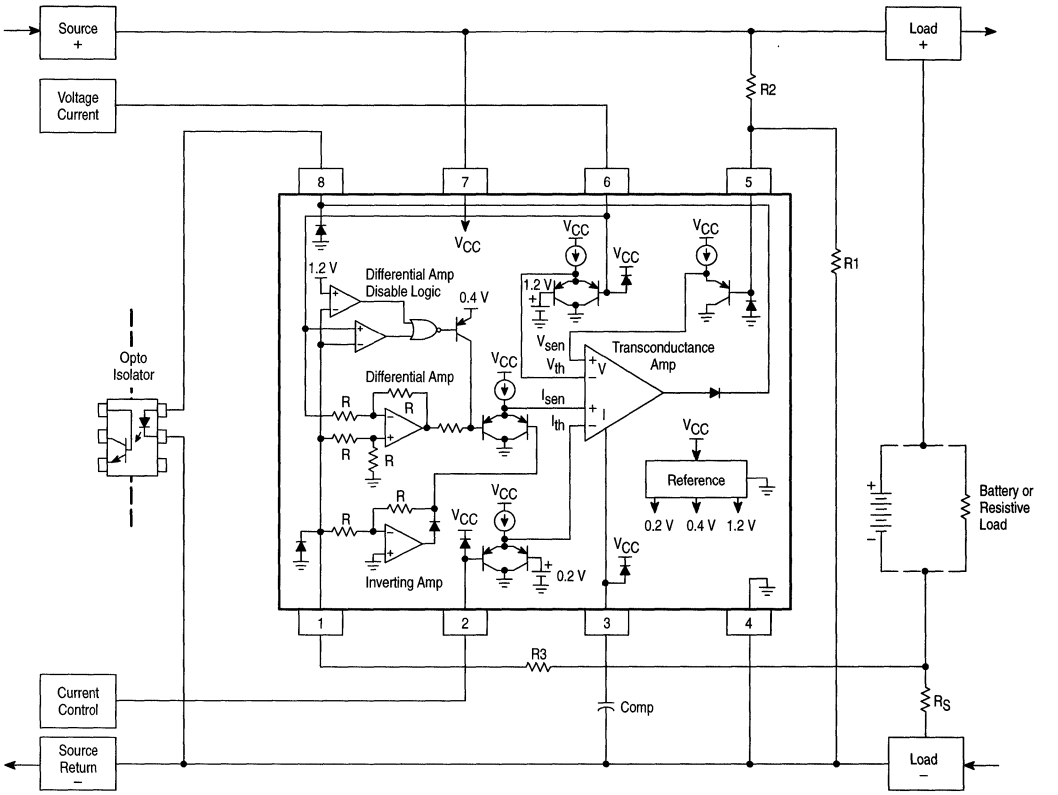
$$= 1.2\left(\frac{R2}{R1} + 1\right)$$

$$I_{reg} = \frac{V_{th(I\,LS+)}}{R_S}$$

$$= \frac{0.2}{R_S}$$

$$R3 = \frac{\left(I_{pk}\,R_S\right) - 0.6}{0.02}$$

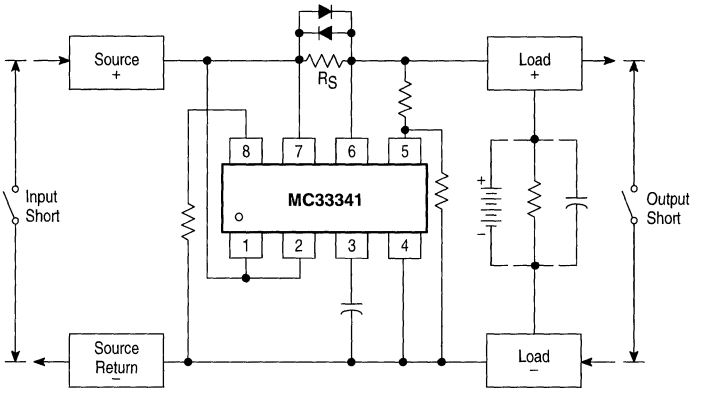
Figure 20. Load Low–Side Current Sensing with Externally Adjustable Current and Voltage Thresholds



The above figure shows the MC33341 configured for load low–side current sensing with an externally adjustable voltage and current threshold. Operation of this circuit is similar to that of Figure 19. The respective voltage and current regulation threshold can be adjusted over a range of 0 to 1.2 V and 0 V to 200 mV, with respect to Pin 4.

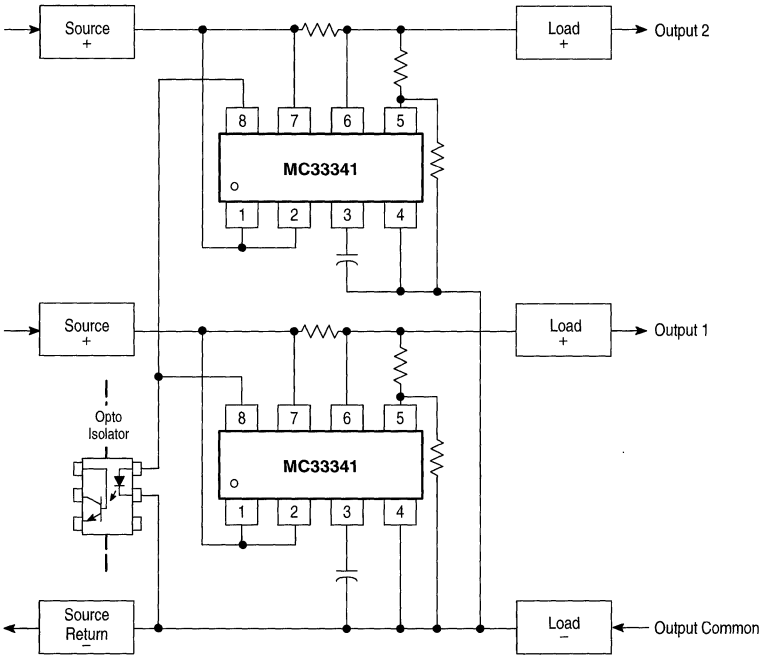
$$V_{reg} = V_{th(Pin\ 6)}\left(\frac{R2}{R1} + 1\right) \qquad I_{reg} = \frac{V_{th(Pin\ 2)}}{R_S} \qquad R3 = \frac{\left(I_{pk}\,R_S\right) - 0.6}{0.02}$$

Figure 21. Current Sense Resistor Bounding



NOTE: An excessive load induced voltage across R_S can occur if either the source input or load output is shorted. This voltage can easily be bounded with the addition of the diodes shown without degrading the current sensing accuracy. This bounding technique can be used in any of the MC33341 applications where high peak currents are anticipated.

Figure 22. Multiple Output Current and Voltage Regulation



NOTE: Multiple outputs can be controlled by summing the error signal into a common optoisolator. The converter output with the largest voltage or current error will dominate control of the feedback loop.

MOTOROLA

Product Preview

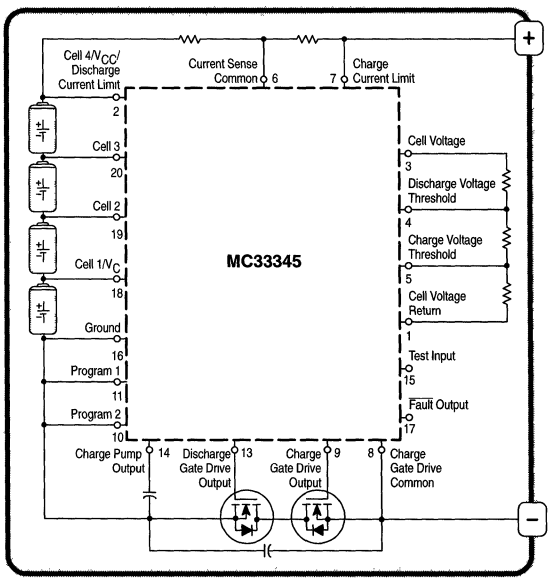
Lithium Battery Protection Circuit for One to Four Cell Battery Packs

3

The MC33345 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one to four cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, cell voltage balancing with on–chip balancing resistors, and a virtually zero current sleepmode state when the cells are discharged. Additional features include an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack, and the programmability for a one to four cell battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. The MC33345 is available in standard and low profile 20 lead surface mount packages.

- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Charge and Discharge Current Limit Detection with Delayed Shutdown
- Cell Voltage Balancing
- On–Chip Balancing Resistors
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Programmable for One, Two, Three or Four Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Four Cell Smart Battery Pack

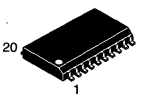


This device contains 1808 active transistors.

MC33345

LITHIUM BATTERY PROTECTION CIRCUIT FOR ONE TO FOUR CELL SMART BATTERY PACKS

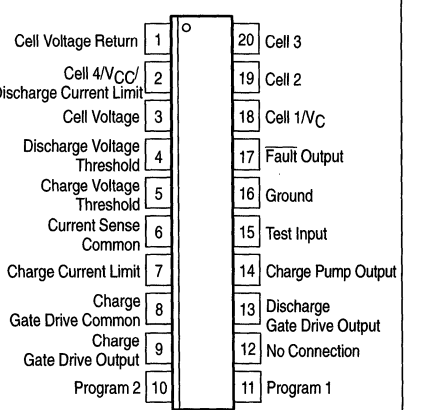
SEMICONDUCTOR TECHNICAL DATA



DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

DTB SUFFIX
PLASTIC PACKAGE
CASE 948E
(TSSOP–20)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33345DW	T_A = –25° to +85°C	SO–20L
MC33345DTB		TSSOP–20

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage (Measured with Respect to Ground, Pin 16)	V_{IR}		V
Cell Voltage Divider (Pins 1, 3, 4 and 5)		18	
Cell 1/V_C (Pin 18)		7.5	
Cell 2 (Pin 19)		10	
Cell 3 (Pin 20)		18	
Cell 4/V_{CC}/Discharge Current Limit (Pin 2)		20	
Current Sense Common (Pin 6)		30	
Charge Current Limit (Pin 7)		30	
Charge Gate Drive Common (Pin 8)		±20	
Charge Gate Drive Output (Pin 9)		18 to –20	
Program 1 (Pin 11)		7.5	
Program 2 (Pin 10)		7.5	
Discharge Gate Drive Output (Pin 13)		18	
Charge Pump Output (Pin 14)		12	
Test (Pin 15)		7.5	
$\overline{\text{Fault}}$ Output (Pin 17)		20	
Cell Voltage Divider Current	I_{div}		mA
Source Current (Pin 4 to 6)		0.5	
Sink Current (Pin 5 to 16)		0.5	
$\overline{\text{Fault}}$ Output Sink Current (Pin 17)	I_{flt}	10	mA
Thermal Resistance, Junction to Air	$R_{\theta JA}$		°C/W
DTB Suffix, TSSOP–20 Plastic Package, Case 948E		135	
DW Suffix, SO–20 Plastic Package, Case 751D		105	
Operating Junction Temperature (Notes 1, 2 and 3)	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS

(V_{CC} (Pin 2) = 8.0 V, V_C (Pin 18) = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Notes 2 and 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE SENSING					
Charge or Discharge Voltage Inputs (Pin 4 or 5 to Pin 1)					
Threshold Voltage	V_{th}	–	1.23	–	V
Input Bias Current	I_{IB}	–	20	–	nA
Input Hysteresis Source Current (Pin 5)	I_H	–	2.0	–	µA
Cell Charge or Discharge Programmable Input Voltage Range (Pin 4 or 5)	$V_{IR(pgm)}$	–	V_{th} to 7.5	–	V
Cell Selector Series Resistance					Ω
Cell Positive to Top of Divider (Pin 2, 20, 19, or 18 to Pin 3)	R_{S+}	–	100	–	
Cell Negative to Bottom of Divider (Pin 20, 19, 18 or 16 to Pin 1)	$R_{S–}$	–	100	–	
Cell Voltage Sampling Rate	$t_{(smpl)}$	–	1.0	–	s
Test Input Threshold Voltage (Pin 15)	V_{th}	–	$V_{Cell\ 1}$/2.0	–	V
CELL VOLTAGE BALANCING					
Internal Balancing Resistance (Pins 2, 20, 19 and 18)	R_{bal}	–	140	–	Ω
CURRENT SENSING					
Charge Current Limit (Pin 7 to Pin 6)					
Threshold Voltage	$V_{th(chg)}$	–	18	–	mV
Input Bias Current	$I_{IB(chg)}$	–	200	–	nA
Delay	$I_{dly(chg)}$	–	1.0	–	s

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
3. Tested ambient temperature range for the MC33345:
T_{low} = –25°C T_{high} = +85°C

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} (Pin 2) = 8.0 V, V_C (Pin 18) = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Notes 2 and 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSING					
Discharge Current Limit (Pin 2 to Pin 6)					
Threshold Voltage	$V_{th(dschg)}$	–	50	–	mV
Input Bias Current	$I_{IB(dschg)}$	–	200	–	nA
Delay	$I_{dly(dschg)}$	–	3.0	–	ms
CHARGE PUMP					
Output Voltage (Pin 14, $R_L \geq 10^{10}\ \Omega$)	V_O	–	10.2	–	V
TOTAL DEVICE					
Average Cell Current	I_{CC}				
Operating (V_{CC} = 8.0 V)		–	15	–	μA
Sleepmode (V_{CC} = 5.0 V)		–	5.0	–	nA
Minimum Operating Cell Voltage for Logic and Gate Drivers	V_{CC}				V
Programmed for One Cell Operation					
Cell 1 Voltage		–	2.2	–	
Programmed for Two, Three, or Four Cell Operation					
Cell 1 Voltage		–	1.5	–	
Cell 2, Cell 3, or Cell 4 Voltage, Sum Voltage of Cells		–	0.7	–	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
3. Tested ambient temperature range for the MC33345:
T_{low} = –25°C T_{high} = +85°C

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Cell Voltage Return	The bottom side of a three resistor divider string connects to this pin. The Cell Selector internally switches this point to the negative terminal of the cell that is to be monitored.
2	Cell 4/V_{CC}/ Discharge Current Limit	This is a multifunction pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 4 and to provide positive supply voltage for the protection IC. This pin is also used to monitor the voltage drop across the discharge current limit resistor and it provides a discharge path for the internal balancing of Cell 4.
3	Cell Voltage	The top side of a three resistor divider string connects to this pin. The Cell Selector internally switches this point to the positive terminal of the cell that is to be monitored.
4	Discharge Voltage Threshold	The upper tap of a three resistor divider string connects to this pin. The Cell Voltage Detector compares the divided down cell voltage to an internal reference. If the comparator detects that the cell voltage has fallen below the programmed level, discharge switch Q2 is disabled, and the protection circuit enters into a low current sleepmode state. This prevents further discharging of the battery pack.
5	Charge Voltage Threshold	The lower tap of a three resistor divider string connects to this pin. The Cell Voltage Detector compares the divided down cell voltage to an internal reference. If the comparator detects that the cell voltage has risen above the programmed level, charge switch Q1 is disabled, preventing further charging of the battery pack. A 2.0 μA current source pull–up is internally applied to this pin creating input hysteresis.
6	Current Sense Common	This pin is a common point that is used to monitor the voltage drop across the charge and discharge current limit resistors.
7	Charge Current Limit	This pin is used to monitor the voltage drop across the charge current limit resistor.
8	Charge Gate Drive Common	This pin provides a gate turn–off path for charge switch Q1. The charge switch source and the battery pack negative terminal connect to this point.
9	Charge Gate Drive Output	This output connects to the gate of charge switch Q1 allowing it to enable or disable battery pack charging.
10	Program 2	This pin is used in conjunction with Pin 11 to program the number of cells.
11	Program 1	This pin is used in conjunction with Pin 10 to program the number of cells.
12	No Connection	This pin is not internally connected.
13	Discharge Gate Drive Output	This output connects to the gate of discharge switch Q2 allowing it to enable or disable battery pack discharging.
14	Charge Pump Output	This is the charge pump output. A reservoir capacitor is connected from this pin to ground.
15	Test Input	This input is used to facilitate circuit testing and is normally not connected. It has an internal 2.0 k pull–up resistor.
16	Ground	This is the protection IC ground and all voltage ratings are with respect to this pin.
17	Fault Output	This is on open drain output that is active low when a charging fault limit has been exceeded. The limits sensed are both charge voltage and current.
18	Cell 1/V_C	This is a multifunction pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 1 and the negative terminal of Cell 2. This pin also provides logic biasing and a discharge path for the internal balancing of Cell 1.
19	Cell 2	This pin connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 2 and the negative terminal of Cell 3. This pin also provides a discharge path for the internal balancing of Cell 2.
20	Cell 3	This pin connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 3 and the negative terminal of Cell 4. This pin also provides a discharge path for the internal balancing of Cell 3.

3

INTRODUCTION

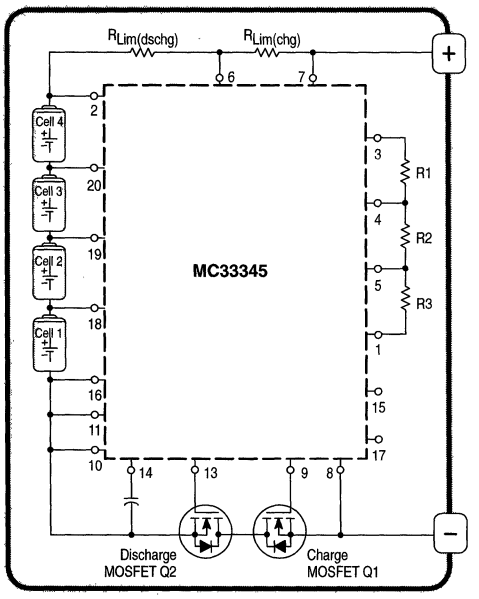
The insatiable demand for smaller lightweight portable electronic equipment has dramatically increased the requirements of battery performance. Batteries are expected to have higher energy densities, superior cycle life, be safe in operation and environmentally friendly. To address these high expectations, battery manufacturers have invested heavily in developing rechargeable lithium–based cells. Today's most attractive chemistries include lithium–polymer, lithium–ion, and lithium–metal. Each of these chemistries require electronic protection in order to constrain cell operation to within the manufacturers limits.

Rechargeable lithium–based cells require precise charge and discharge termination limits for both voltage and current in order to maximize cell capacity, cycle life, and to protect the end user from a catastrophic event. The termination limits are not as well defined as with older non–lithium chemistries. These limits are dependent upon a manufacturer's particular lithium chemistry, construction technique, and intended application. Battery pack assemblers may also choose to enhance cell capacity at the expense of cycle life. In order to address these requirements the MC33345 was developed. This device features programmable voltage and current limits, cell voltage balancing, low operating current, a virtually zero current sleepmode state, and requires few external components to implement a complete one to four cell smart battery pack.

OPERATING DESCRIPTION

The MC33345 is specifically designed to be placed in the battery pack where it is continuously powered from either one, two, three, or four lithium cells. In order to maintain cell operation within specified limits, the protection circuit senses both cell voltage and current, and correspondingly controls the state of two N–channel MOSFET switches. These switches, Q1 and Q2, are placed in series with the negative terminal of Cell 1 and the negative terminal of the battery pack.

Figure 1. Simplified Four Cell Smart Battery Pack



This configuration allows the protection circuit to interrupt the appropriate charge or discharge path FET in the event that a programmed voltage or current limit for any cell has been exceeded.

A functional description of the protection circuit blocks follows. Refer to the detailed block diagram shown in Figure 6.

Voltage Sensing

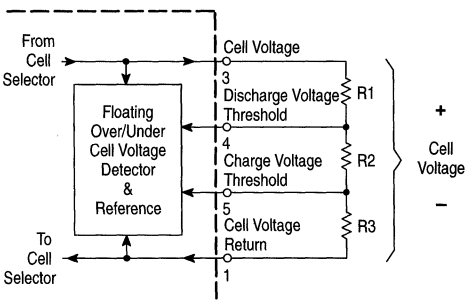
Individual cell voltage sensing is accomplished by the use of the Cell Selector in conjunction with the Floating Over/Under Voltage Detector and Reference block. The Cell Selector applies the voltage of each cell across an external resistor divider string that connects from Pins 3 to 1. The voltage at each of the tap points is sequentially polled and compared to an internal reference. If a limit has been exceeded, the result is stored in the Over/Under Data Latch and Control Logic block. The Cell Selector is gated on for an 8.0 ms period at a one second repetition rate. This low duty cycle sampling technique reduces the average load current that the divider presents across each cell, thus extending the useful battery pack capacity. The cells are sensed in the following sequence:

Figure 2. Cell Sensing Sequence

Polling Sequence	Time (ms)	Cell Sensed	Tested Limit
1	1.0	Cell 4	Overvoltage
2	1.0	Cell 3	Overvoltage
3	1.0	Cell 2	Overvoltage
4	1.0	Cell 1	Overvoltage
5	1.0	Cell 4	Undervoltage
6	1.0	Cell 3	Undervoltage
7	1.0	Cell 2	Undervoltage
8	1.0	Cell 1	Undervoltage

By incorporating this polling technique with a single floating comparator and voltage divider, a significant reduction of circuitry and trim elements is achieved. This results in a smaller die size, lower cost, and reduced operating current.

Figure 3. Cell Voltage Limit Programming



The cell charge and discharge voltage limits are controlled by the values selected for the resistor divider string and the 1.23 V input threshold of Pins 4 and 5. As the battery pack reaches full charge, the Cell Voltage Detector will sense an overvoltage fault condition on the first cell that exceeds the programmed overvoltage limit. The fault information is stored

in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. An internal 2.0 µA current source pull–up is then applied to Pin 5 creating an input hysteresis voltage. As a result of an overvoltage fault, the battery pack is available for discharging only.

The overvoltage fault is reset by applying a load to the battery pack. As the voltage across each cell falls below the input hysteresis level, charge MOSFET Q1 will turn on. The battery pack will now be available for charging or discharging. The over voltage limit and hysteresis voltage are given by:

$$V_{OV} = V_{th\ (Pin\ 5)}\left(\frac{R1 + R2 + R3}{R3}\right)$$

$$V_H = I_{H\ (Pin\ 5)}(R1 + R2)$$

As the load eventually depletes the battery pack charge, the Cell Voltage Detector will sense an undervoltage fault condition on the first cell that falls below the programmed undervoltage limit. After an undervoltage cell is detected, discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. The protection circuit will now enter a low current sleepmode state drawing just 5.0 nA typically, thus preventing any further cell discharging. As a result of the undervoltage fault, the battery pack is available for charging only. The undervoltage limit is given by:

$$V_{UV} = V_{th\ (Pin\ 4)}\left(\frac{R1 + R2 + R3}{R2 + R3}\right)$$

The undervoltage fault is reset by applying charge current to the battery pack. When the voltage on Pin 16 exceeds Pin 8 by 0.6 V, discharge MOSFET Q2 will turned on. The battery pack will now be available for charging or discharging.

Since the thresholds of Pins 4 and 5 are equal, the above equations can be rewritten to directly solve for specific resistor values as shown in the example below.

Let the desired limits be:

V_{OV} = 4.2 V, V_H = 0.4 V, and V_{UV} = 2.5 V

With nominal values for:

V_{th} = 1.23 V, and I_H = 2.0 µA

$$R3 = \frac{\left(\frac{V_H}{I_H}\right)}{\left(\frac{V_{OV}}{V_{th}} - 1\right)} = \frac{\left(\frac{0.4}{2.0 \times 10^{-6}}\right)}{\left(\frac{4.2}{1.23} - 1\right)} = 82{,}828\ \Omega$$

$$R2 = R3\left(\frac{V_{OV}}{V_{UV}} - 1\right) = 82{,}828\left(\frac{4.2}{2.5} - 1\right) = 56{,}323\ \Omega$$

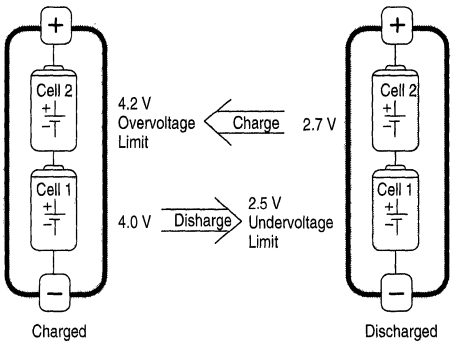
$$R1 = \left(\frac{V_H}{I_H}\right) - R2 = \left(\frac{0.4}{2.0 \times 10^{-6}}\right) - 56{,}323 = 143{,}677\ \Omega$$

Note that the Cell Selector has a typical total series resistance of 200 Ω. This will have a minimal effect on the programmed limits if the total divider resistance is in excess of 100 kΩ.

Cell Voltage Balancing

With series connected cells, successive charge and discharge cycles can result in a significant difference in cell voltage with a corresponding degradation of battery pack capacity. Figure 4 illustrates the operation of an unbalanced two cell pack. As the cells become unbalanced, the full battery pack capacity is not realized. This is due to the requirement that charging must terminate when Cell 2 reaches the overvoltage limit, and discharging must terminate when Cell 1 reaches the undervoltage limit. By employing a method of keeping the cell voltages equal, both cells can be charged and discharged to their specified limits, thus attaining the maximum possible capacity .

Figure 4. Unbalanced Battery Pack Operation



The MC33345 contains a Cell Voltage Balancing Logic circuit that controls four N–channel MOSFETs. The circuit samples the voltage of each cell during the polling period. If all of the cells are below the programmed overvoltage fault limit, no cell balancing takes place. If one or more cells reach the overvoltage fault limit, a specific latch is set for each cell. At the end of the polling period, charge MOSFET Q1 is turned off and the latches are interrogated. If all of the latches were set, no cell balancing takes place. If one, two, or three latches were set, the required cell balancing MOSFETs are then activated. The overvoltage cells are discharged to the programmed level of $V_{OV} - V_H$. As each cell attains this level, the discharge MOSFETs successively turn off. Upon completion of cell balancing, charge MOSFET Q1 is turned on. Cell voltage balancing is active during charge and discharge, but disabled during the low current sleepmode state.

Cell Programming and Test

The protection circuit can be programmed for operation with either one, two, three, or four cell battery packs. Programming inputs 1 and 2 are used to set up the internal logic for the number of cells to be monitored. If less than four cells are required, the input for each empty cell position must be connected to V_{CC}. This process starts with Cell 4 decending down to Cell 2 if required. Refer to the Cell Programming table shown below and the specific application figure.

Figure 5. Cell Sensing Sequence

Number of Cells	Program 1 (Pin 11)	Program 2 (Pin 10)	Application Figure
1	Ground	Cell 1/V_C	16
2	Cell 1/V_C	Ground	15
3	Cell 1/V_C	Cell 1/V_C	14
4	Ground	Ground	13

A test option is provided to speed up device and battery pack testing. By connecting Pin 15 to ground, the internal logic is held in a reset state and both MOSFET switches are turned on. Upon release, the Control Logic becomes active and the cells are polled within 8.0 ms.

Current Sensing

Charge and discharge current limit protection can be selectively added to the battery pack with the addition of a sense resistor. The resistors are placed in series with the positive terminal of the battery pack and the cells. Refer to Figure 1.

As the battery pack charges, Pins 6 and 7 sense the voltage drop across $R_{Lim(chg)}$. A charge current limit fault is detected if the voltage at Pin 7 exceeds Pin 6 by 18 mV for the entire delay period of 1.0 second. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. As a result of the charge current fault, the battery pack is available for discharging only. The charge current limit is given by:

$$I_{Lim(chg)} = \frac{V_{th(chg)}}{R_{Lim(chg)}} = \frac{18\ mV}{R_{Lim(chg)}}$$

The charge current fault is reset by either disconnecting the battery pack from the charger, or by connecting a load to the battery pack. When the voltage on Pin 16 no longer exceeds Pin 8 by approximately 2.0 V, the Sense Enable circuit will turn on charge MOSFET Q1. Charge current sensing can be disabled by connecting Pin 7 to Pin 6.

The discharge current limiting operates in a similar manner. As the battery pack discharges, Pins 2 and 6 sense the voltage drop across $R_{Lim(dschg)}$. A discharge current limit fault is detected if the voltage at Pin 2 is less than Pin 6 by 50 mV for more than 3.0 ms. The fault information is stored in a data latch and discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. As a result of the discharge current fault, the battery pack is available for charging only. The discharge current limit is given by:

$$I_{Lim(dschg)} = \frac{V_{th(dschg)}}{R_{Lim(dschg)}} = \frac{50\ mV}{R_{Lim(dschg)}}$$

The discharge current fault is reset by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger. When the voltage on Pin 8 no longer exceeds Pin 16 by approximately 2.0 V, the Sense Enable circuit will turn on discharge MOSFET Q2. Discharge current sensing can be disabled by connecting Pin 2 to Pin 6.

The charge and discharge current protection circuits contain a built in response delay of 1.0 s and 3.0 ms respectively. This helps to prevent fault activation when the battery pack is subjected to pulsed currents during charging or discharging.

Charge Pump and MOSFET Switches

The MC33345 contains an on chip Charge Pump to ensure that the MOSFET switches are fully enhanced for reduced power losses. An external reservoir capacitor normally connects from the Charge Pump output to ground, Pins 14 and 16. The capacitor value is not critical and is usually within the range of 10 nF to 100 nF. The Charge Pump output is regulated at 10.2 V allowing the use of economical logic level MOSFETs in one and two cell applications. The main requirement in selecting a particular type of MOSFET switch is to consider the desired on–resistance at the lowest anticipated operating voltage of the battery pack. A table of small outline surface mount devices is given in Figure 6. When using extremely low threshold MOSFETs, it may be desirable to disable the Charge Pump so that the maximum gate to source voltage is not exceeded. This is accomplished by connecting Pin 14 to Pin 19 with two, three, or four cell battery packs.

Battery Pack Application

Upon assembly of the battery pack, it is imperative that Cell 1 be connected first so that V_C is properly biased. The remaining cells can then be connected in any order. This assembly method prevents forward biasing the protection IC substrate which can result in overheating and non–functionality.

Each of the application figures show a capacitor labeled C_{ESD}. This capacitor provides a path around the MOSFET switches in the event of an electrostatic discharge.

Figure 6. Small Outline Surface Mount MOSFET Switches

Device Type	On–Resistance (Ω) versus Gate to Source Voltage (V)						
	2.5 V	3.0 V	4.0 V	5.0 V	6.0 V	7.5 V	9.0 V
MMFT3055VL	–	–	–	0.120 Ω	0.115 Ω	0.108 Ω	0.100 Ω
MMDF3N03HD	–	0.525 Ω	0.080 Ω	0.065 Ω	0.063 Ω	0.062 Ω	0.060 Ω
MMDF4N01HD	0.047 Ω	0.042 Ω	0.037 Ω	0.035 Ω	0.034 Ω	0.033 Ω	See Note
MMSF5N02HD	–	0.065 Ω	0.023 Ω	0.021 Ω	0.020 Ω	0.018 Ω	0.018 Ω
MMDF6N02HD	0.043 Ω	0.035 Ω	0.029 Ω	0.028 Ω	0.026 Ω	0.025 Ω	0.023 Ω

NOTE: Exceeds maximum V_{GS} voltage rating.

PROTECTION CIRCUIT OPERATING MODE TABLE

Input Conditions Cell Status	Circuit Operation Battery Pack Status	Outputs			
		MOSFET Switches		Function	
		Charge Q1	Discharge Q2	Charge Pump	Cell Balancing (See Note)
CELL CHARGING/DISCHARGING					
Storage or Nominal Operation: No current or voltage faults	Both Charge MOSFET Q1 and Discharge MOSFET Q2 are on. The battery pack is available for charging or discharging.	On	On	Active	Active
CELL CHARGING FAULT/RESET					
Charge Current Limit Fault: $V_{Pin\ 7} \geq (V_{Pin\ 6} + 18\ mV)$ for 1.0 s	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. Q1 will remain in the off state as long as $V_{Pin\ 16}$ exceeds $V_{Pin\ 11}$ by ≈ 2.0 V. The battery pack is available for discharging.	On to Off	On	Active	Active
Charge Current Limit Reset: $V_{Pin\ 16} - V_{Pin\ 8} < 2.0\ V$	The Sense Enable circuit will reset and turn on charge MOSFET Q1 when $V_{Pin\ 16}$ no longer exceeds $V_{Pin\ 11}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the charger from the battery pack, or by connecting a load to the battery pack.	Off to On	On	Active	Active
Charge Voltage Limit Fault: $V_{Pin\ 5} \geq 1.23\ V$ for 1.0 s	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. An internal current source pull–up of 2.0 μA is applied to Pin 8 creating an input hysteresis voltage of V_H with divider resistors R1 and R2. The battery pack is available for discharging.	On to Off	On	Active	Active
Charge Voltage Limit Reset: $V_{Pin\ 5} < 1.23\ V$ for 1.0 s	Charge MOSFET Q1 will turn on when the voltage across each cell falls sufficiently to overcome the input hysteresis voltage. This can be accomplished by applying a load to the battery pack.	Off to On	On	Active	Active
CELL DISCHARGING FAULT/RESET					
Discharge Current Limit Fault: $V_{Pin\ 6} \leq (V_{Pin\ 2} - 50\ mV)$ for 3.0 ms	Discharge MOSFET Q2 is latched off and the cells are disconnected from the load. Q2 will remain in the off state as long as $V_{Pin\ 11}$ exceeds $V_{Pin\ 16}$ by ≈ 2.0 V. The battery pack is available for charging.	On	On to Off	Active	Active
Discharge Current Limit Reset: $V_{Pin\ 8} - V_{Pin\ 16} < 2.0\ V$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 11}$ no longer exceeds $V_{Pin\ 16}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger.	On	Off to On	Active	Active
Discharge Voltage Limit Fault: $V_{Pin\ 4} \leq 1.23\ V$ for 1.0 s	Discharge MOSFET Q2 is latched off, the cells are disconnected from the load, and the protection circuit enters a low current sleepmode state. The battery pack is available for charging.	On	On to Off	Disabled	Disabled
Discharge Voltage Limit Reset: $V_{Pin\ 16} > (V_{Pin\ 8} + 0.6\ V)$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 16}$ exceeds $V_{Pin\ 8}$ by 0.6 V. This can be accomplished by connecting the battery pack to the charger.	On	Off to On	Active	Active
FAULTY CELL					
Simultaneous Charge and Discharge Voltage Limit Faults: $V_{Pin\ 5} \geq 1.23\ V$ for 1.0 s and $V_{Pin\ 4} \leq 1.23\ V$ for 1.0 s	This condition can happen if there is a defective cell in the battery pack. The protection circuit will remain in the sleepmode state until the battery pack is connected to a charger. If Cell 2, 3, or 4 is faulty and a charger is connected, the protection circuit will cycle in and out of sleepmode. If Cell 1 is faulty (<1.5 V), the protection circuit logic will not function and the battery pack cannot be charged.	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty

NOTE: Cell balancing is not active when programmed for one cell operation.

3

Figure 7. Four Cell Smart Battery Pack

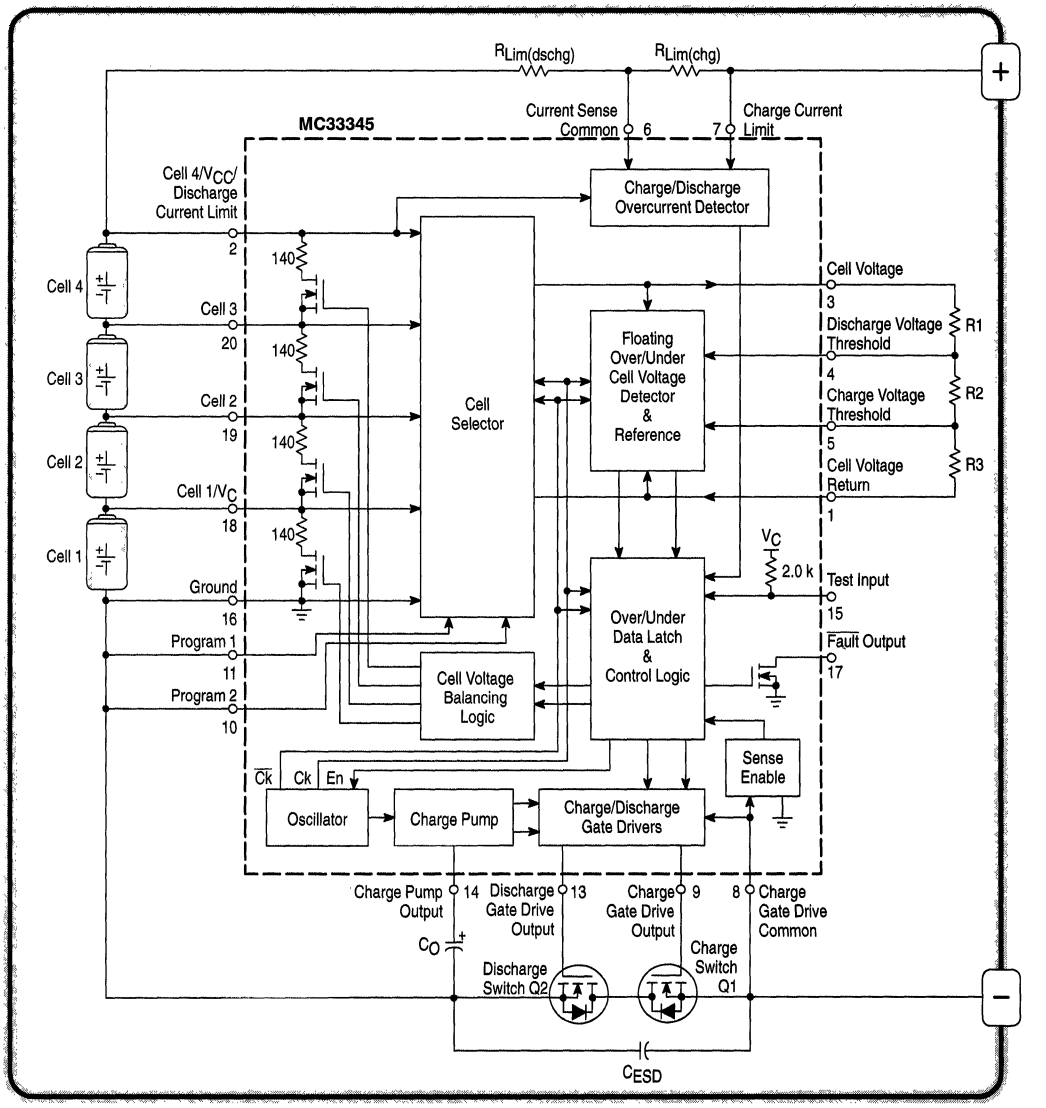
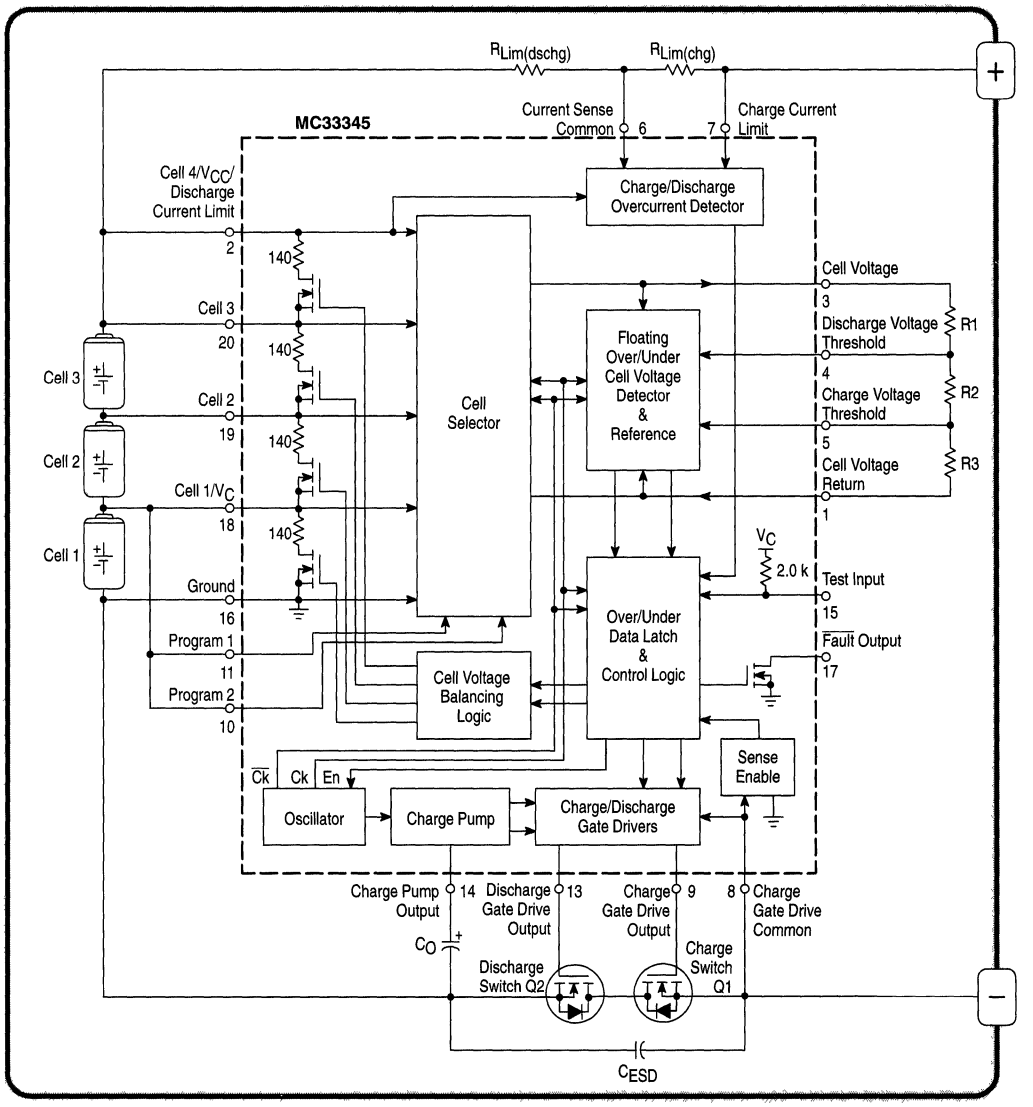


Figure 8. Three Cell Smart Battery Pack



3

Figure 9. Two Cell Smart Battery Pack

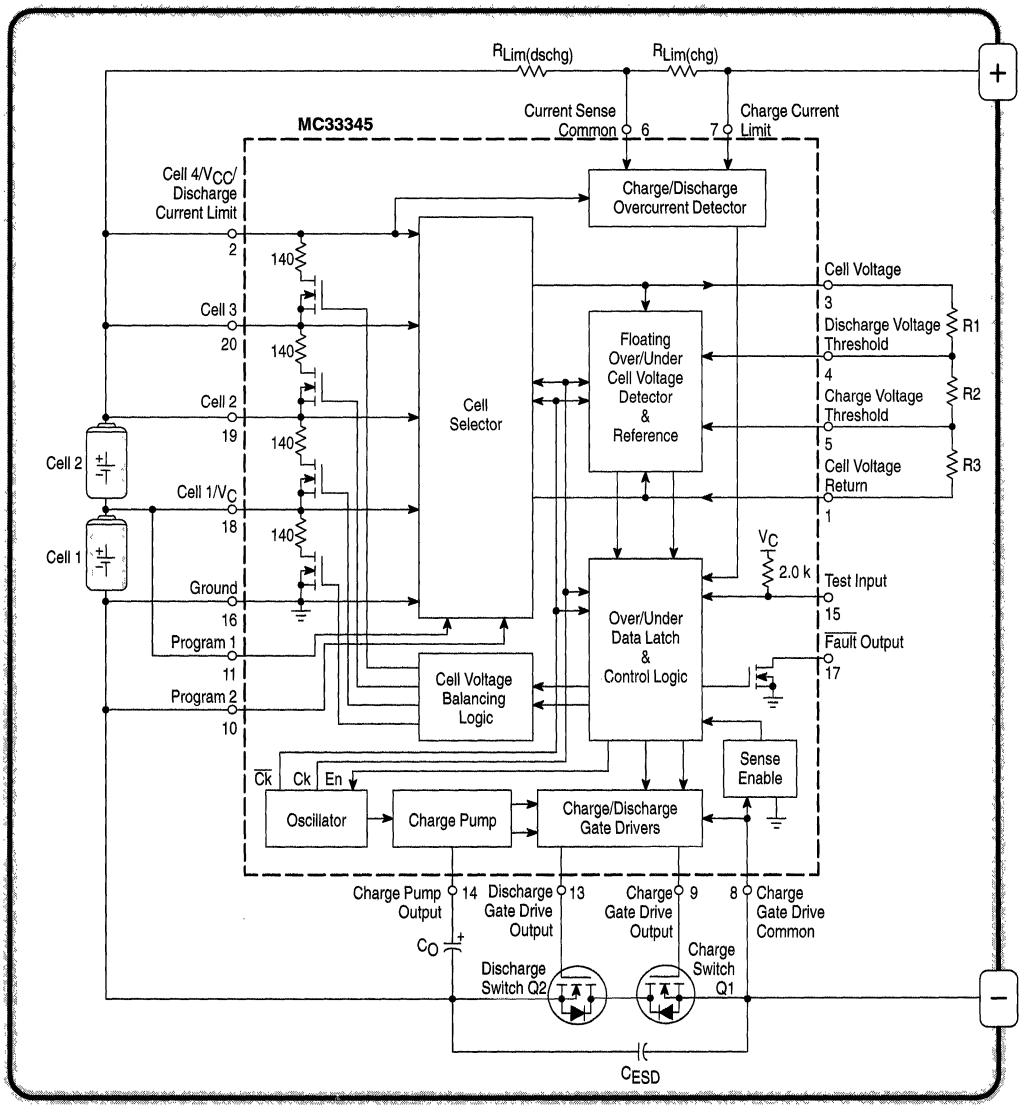
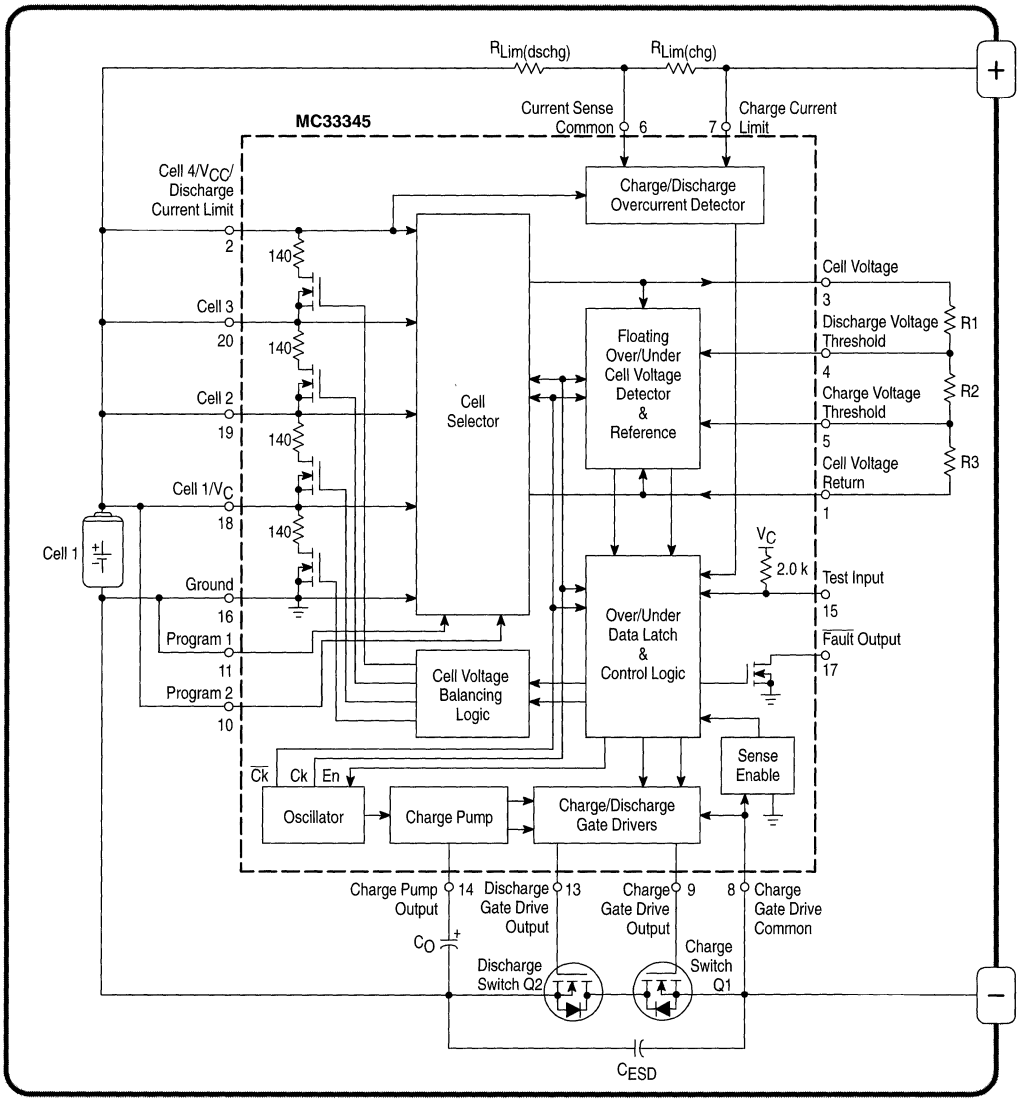


Figure 10. One Cell Smart Battery Pack



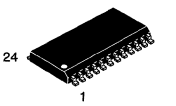
MC33346

Product Preview

Lithium Battery Protection Circuit for Three or Four Cell Battery Packs

LITHIUM BATTERY PROTECTION CIRCUIT FOR THREE OR FOUR CELL SMART BATTERY PACKS

The MC33346 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of three or four cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, cell voltage balancing with on–chip balancing resistors, and virtually zero current sleepmode state when the cells are discharged. Additional features consists of a six wire microcontroller interface bus that can selectively provide a pulse output that represents the internal reference voltage, cell voltage, cell current and temperature, as well as control the states of four internal balancing and two external MOSFET switches. A microcontroller time reference output is available for gas gauge implementation. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. The MC33346 is available in standard and low profile 24 lead surface mount packages.

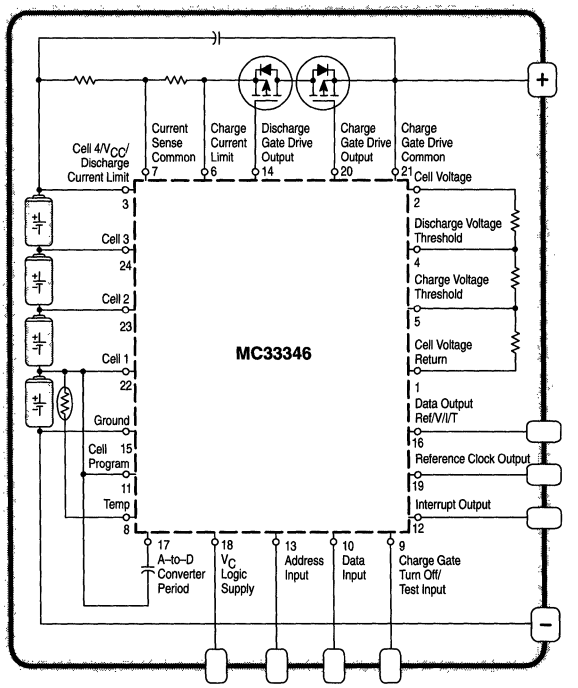


DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

DTB SUFFIX
PLASTIC PACKAGE
CASE 948H
(TSSOP–24)

- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Delayed Current Shutdown
- Cell Voltage Balancing with On–Chip Resistors
- Six Wire Microcontroller Interface Bus
- Data Output for Reference, Voltage, Current, and Temperature
- Microcontroller Time Reference Output for Gas Gauging
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Programmable for Three or Four Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Four Cell Smart Battery Pack



This device contains 4760 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33346DW	T_A = –40° to +85°C	SO–24L
MC33346DTB		TSSOP–24

MOTOROLA

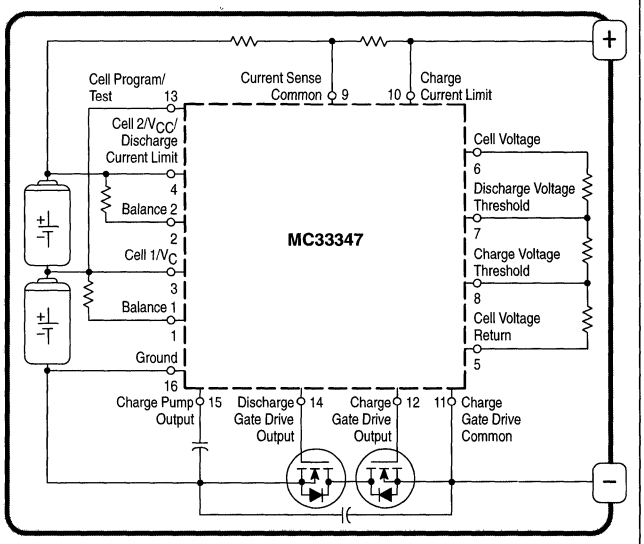
Product Preview

Lithium Battery Protection Circuit for One or Two Cell Battery Packs

The MC33347 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one or two cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, continuous cell voltage balancing with the choice of on–chip or external balancing resistors, and a virtually zero current sleepmode state when the cells are discharged. Additional features include an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack, and the programmability for one or two cell battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. This MC33347 is avaialble in standard and low profile 16 lead surface mount packages.

- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Charge and Discharge Current Limit Detection with Delayed Shutdown
- Continuous Cell Voltage Balancing
- On–Chip or External Balancing Resistors
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Programmable for One or Two Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Two Cell Smart Battery Pack



This device contains 1543 active transistors.

MC33347

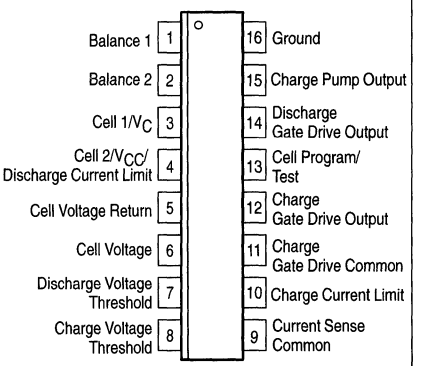
LITHIUM BATTERY PROTECTION CIRCUIT FOR ONE OR TWO CELL SMART BATTERY PACKS

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

DTB SUFFIX
PLASTIC PACKAGE
CASE 948F
(TSSOP–16)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33347D	T_A = −25° to +85°C	SO–16
MC33347DTB		TSSOP–16

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage (Measured with Respect to Ground, Pin 16)	V_{IR}		V
Balance 1, 2 (Pin 1, 2)		15	
Cell 1/V_C (Pin 3)		7.5	
Cell 2/V_{CC}/Discharge Current Limit (Pin 4)		18	
Cell Voltage Divider (Pins 5, 6, 7 and 8)		18	
Current Sense Common (Pin 9)		30	
Charge Current Limit (Pin 10)		30	
Charge Gate Drive Common (Pin 11)		±20	
Charge Gate Drive Output (Pin 12)		18 to –20	
Cell Program/Test (Pin 13)		7.5	
Discharge Gate Drive Output (Pin 14)		18	
Charge Pump Output (Pin 15)		18	
External Cell Balancing Current (Pin 1, 2, Note 1)	I_{bal}	1.0	A
Cell Voltage Divider Current	I_{div}		mA
Source Current (Pin 4 to 6)		0.5	
Sink Current (Pin 5 to 16)		0.5	
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$		°C/W
DTB Suffix, TSSOP–16 Plastic Package, Case 948F		176	
D Suffix, SO–16 Plastic Package, Case 751B		145	
Operating Junction Temperature (Notes 1, 2 and 3)	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS

(V_{CC} (Pin 4) = 8.0 V, V_C (Pin 3) = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Notes 2 and 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE SENSING					
Charge or Discharge Voltage Inputs (Pin 7 or 8 to Pin 5)					
Threshold Voltage	V_{th}	–	1.230	–	V
Input Bias Current	I_{IB}	–	20	–	nA
Input Hysteresis Source Current (Pin 8)	I_H	–	2.0	–	µA
Cell Charge or Discharge Programmable Input Voltage Range (Pin 7 or 8)	$V_{IR(pgm)}$	–	V_{th} to 7.5	–	V
Cell Selector Series Resistance					Ω
Cell Positive to Top of Divider (Pin 3 or 4 to Pin 6)	R_{S+}	–	100	–	
Cell Negative to Bottom of Divider (Pin 3 or 16 to Pin 5)	$R_{S–}$	–	100	–	
Cell Voltage Sampling Rate	$t_{(smpl)}$	–	1.0	–	s
Cell Program/ Test Input Threshold Voltage (Pin 13)	V_{th}	–	$V_{Cell\ 1}$/2.0	–	V
CELL VOLTAGE BALANCING					
Cell Voltage Balancing Accuracy (Note 4)	ΔV	–	1.0	–	%
Internal Balancing Resistance (Pin 3, 4)	R_{bal}	–	80	–	Ω
Balancing MOSFET On Resistance (Pin 1, 2)	$R_{DS(on)}$	–	1.0	–	Ω

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
3. Tested ambient temperature range for the MC33347:
T_{low} = –25°C T_{high} = +85°C
4. Cell voltage balancing accuracy is defined as: $\left|\frac{\Delta V}{V_{avg}}\right| \times 100 = \left|\frac{V_{Cell\ 1} - V_{Cell\ 2}}{\left(\frac{V_{Cell\ 1} + V_{Cell\ 2}}{2}\right)}\right| \times 100$

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} (Pin 4) = 8.0 V, V_C (Pin 3) = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Notes 2 and 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSING					
Charge Current Limit (Pin 10 to Pin 9)					
Threshold Voltage	$V_{th(chg)}$	–	18	–	mV
Input Bias Current	$I_{IB(chg)}$	–	200	–	nA
Delay	$I_{dly(chg)}$	–	3.0	–	ms
Discharge Current Limit (Pin 4 to Pin 9)					
Threshold Voltage	$V_{th(dschg)}$	–	50	–	mV
Input Bias Current	$I_{IB(dschg)}$	–	200	–	nA
Delay	$I_{dly(dschg)}$	–	3.0	–	ms
CHARGE PUMP					
Output Voltage (Pin 15, $R_L \geq 10^{10}\ \Omega$)	V_O	–	10.2	–	V
TOTAL DEVICE					
Average Cell Current	I_{CC}				
Operating (V_{CC} = 8.0 V)		–	12.5	–	μA
Sleepmode (V_{CC} = 5.0 V)		–	15	–	nA
Minimum Operating Cell Voltage for Logic and Gate Drivers	V_{CC}				V
Programmed for Two Cell Operation					
Cell 1 Voltage		–	1.5	–	
Cell 2 Voltage		–	0	–	
Programmed for One Cell Operation					
Cell 1 Voltage		–	1.5	–	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
3. Tested ambient temperature range for the MC33347:
T_{low} = −25°C T_{high} = +85°C
4. Cell voltage balancing accuracy is defined as: $\left|\frac{\Delta V}{V_{avg}}\right| \times 100 = \left|\frac{V_{Cell\ 1} - V_{Cell\ 2}}{\left(\frac{V_{Cell\ 1} + V_{Cell\ 2}}{2}\right)}\right| \times 100$

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Balance 1	This is the drain connection to an internal MOSFET. An external resistor is placed from this pin to the positive terminal of Cell 1 for increased cell balancing capability. This allows most of the additional power to be dissipated off–chip.
2	Balance 2	This is the drain connection to an internal MOSFET. An external resistor is placed from this pin to the positive terminal of Cell 2 for increased cell balancing capability. This allows most of the additional power to be dissipated off–chip.
3	Cell 1/V_C	This is a multifunction pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 1 and the negative terminal of Cell 2. This pin also provides logic biasing and a discharge path for the internal balancing of Cell 1.
4	Cell 2/V_{CC}/ Discharge Current Limit	This is a multifunction pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 2 and to provide positive supply voltage for the protection IC. This pin is also used to monitor the voltage drop across the discharge current limit resistor and it provides a discharge path for the internal balancing of Cell 2.
5	Cell Voltage Return	The bottom side of a three resistor divider string connects to this pin. The Cell Selector internally switches this point to the negative terminal of the cell that is to be monitored.
6	Cell Voltage	The top side of a three resistor divider string connects to this pin. The Cell Selector internally switches this point to the positive terminal of the cell that is to be monitored.
7	Discharge Voltage Threshold	The upper tap of a three resistor divider string connects to this pin. The Cell Voltage Detector compares the divided down cell voltage to an internal reference. If the comparator detects that the cell voltage has fallen below the programmed level for three consecutive samples, discharge switch Q2 is disabled, and the protection circuit enters into a low current sleepmode state. This prevents further discharging of the battery pack.
8	Charge Voltage Threshold	The lower tap of a three resistor divider string connects to this pin. The Cell Voltage Detector compares the divided down cell voltage to an internal reference. If the comparator detects that the cell voltage has risen above the programmed level, charge switch Q1 is disabled, preventing further charging of the battery pack. A 2.0 μA current source pull–up is internally applied to this pin creating input hysteresis.
9	Current Sense Common	This pin is a common point that is used to monitor the voltage drop across the charge and discharge current limit resistors.
10	Charge Current Limit	This pin is used to monitor the voltage drop across the charge current limit resistor.
11	Charge Gate Drive Common	This pin provides a gate turn–off path for charge switch Q1. The charge switch source and the battery pack negative terminal connect to this point.
12	Charge Gate Drive Output	This output connects to the gate of charge switch Q1 allowing it to enable or disable battery pack charging.
13	Cell Program/Test	This is a multifunction input that is used to program the number of cells and to facilitate circuit testing. This input is connected to Pin 3 for two cell operation, and to Pin 16 for one cell operation.
14	Discharge Gate Drive Output	This output connects to the gate of discharge switch Q2 allowing it to enable or disable battery pack discharging.
15	Charge Pump Output	This is the charge pump output. A reservoir capacitor is connected from this pin to ground.
16	Ground	This is the protection IC ground and all voltage ratings are with respect to this pin.

INTRODUCTION

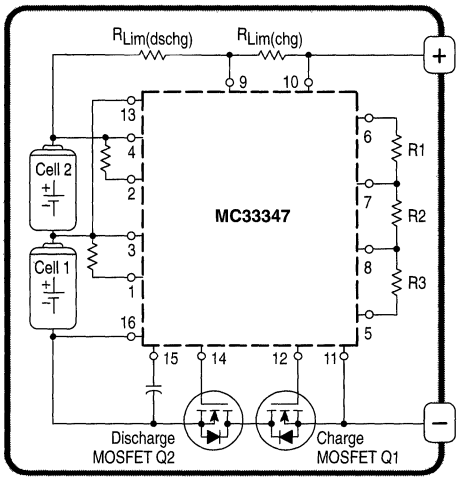
The insatiable demand for smaller lightweight portable electronic equipment has dramatically increased the requirements of battery performance. Batteries are expected to have higher energy densities, superior cycle life, be safe in operation and environmentally friendly. To address these high expectations, battery manufacturers have invested heavily in developing rechargeable lithium–based cells. Today's most attractive chemistries include lithium–polymer, lithium–ion, and lithium–metal. Each of these chemistries require electronic protection in order to constrain cell operation to within the manufacturers limits.

Rechargeable lithium–based cells require precise charge and discharge termination limits for both voltage and current in order to maximize cell capacity, cycle life, and to protect the end user from a catastrophic event. The termination limits are not as well defined as with older non–lithium chemistries. These limits are dependent upon a manufacturer's particular lithium chemistry, construction technique, and intended application. Battery pack assemblers may also choose to enhance cell capacity at the expense of cycle life. In order to address these requirements the MC33347 was developed. This device features programmable voltage and current limits, cell voltage balancing, low operating current, a virtually zero current sleepmode state, and requires few external components to implement a complete one or two cell smart battery pack.

OPERATING DESCRIPTION

The MC33347 is specifically designed to be placed in the battery pack where it is continuously powered from either one or two lithium cells. In order to maintain cell operation within specified limits, the protection circuit senses both cell voltage and current, and correspondingly controls the state of two N–channel MOSFET switches. These switches, Q1 and Q2, are placed in series with the negative terminal of Cell 1 and the negative terminal of the battery pack. This configuration allows the protection circuit to interrupt the appropriate charge or discharge path FET in the event that a programmed voltage or current limit for either cell has been exceeded.

Figure 1. Simplified Two Cell Smart Battery Pack



A functional description of the protection circuit blocks follows. Refer to the detailed block diagram shown in Figures 7 and 8.

Voltage Sensing

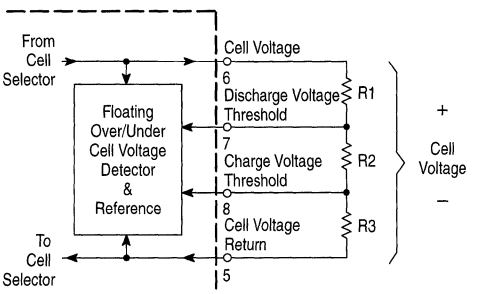
Individual cell voltage sensing is accomplished by the use of the Cell Selector in conjunction with the Floating Over/Under Voltage Detector and Reference block. The Cell Selector applies the voltage of each cell across an external resistor divider string that connects from Pins 6 to 5. The voltage at each of the tap points is sequentially polled and compared to an internal reference. If a limit has been exceeded, the result is stored in the Over/Under Data Latch and Control Logic block. The Cell Selector is gated on for a 1.0 ms period at a one second repetition rate. This low duty cycle sampling technique reduces the average load current that the divider presents across each cell, thus extending the useful battery pack capacity. The cells are sensed in the following sequence:

Figure 2. Cell Sensing Sequence

Polling Sequence	Time (ms)	Cell Sensed	Tested Limit
1	0.25	Cell 2	Overvoltage
2	0.25	Cell 1	Overvoltage
3	0.25	Cell 2	Undervoltage
4	0.25	Cell 1	Undervoltage

By incorporating this polling technique with a single floating comparator and voltage divider, a significant reduction of circuitry and trim elements is achieved. This results in a smaller die size, lower cost, and reduced operating current.

Figure 3. Cell Voltage Limit Programming



The cell charge and discharge voltage limits are controlled by the values selected for the resistor divider string and the 1.23 V input threshold of Pins 7 and 8. As the battery pack reaches full charge, the Cell Voltage Detector will sense an overvoltage fault condition on the first cell that exceeds the programmed overvoltage limit. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. An internal 2.0 μA current source pull–up is then applied to Pin 8 creating an input hysteresis voltage. As a result of an overvoltage fault, the battery pack is available for discharging only.

The overvoltage fault is reset by applying a load to the battery pack. As the voltage across each cell falls below the input hysteresis level, charge MOSFET Q1 will turn on. The battery pack will now be available for charging or discharging. The over voltage limit and hysteresis voltage are given by:

$$V_{OV} = V_{th\ (Pin\ 8)}\left(\frac{R1 + R2 + R3}{R3}\right)$$

$$V_H = I_{H\ (Pin\ 8)}(R1 + R2)$$

As the load eventually depletes the battery pack charge, the Cell Voltage Detector will sense an undervoltage fault condition on the first cell that falls below the programmed undervoltage limit. After three consecutive faults are detected, discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. The protection circuit will now enter a low current sleepmode state drawing just 15 nA, thus preventing any further cell discharging. As a result of the undervoltage fault, the battery pack is available for charging only. The undervoltage limit is given by:

$$V_{UV} = V_{th\ (Pin\ 7)}\left(\frac{R1 + R2 + R3}{R2 + R3}\right)$$

The undervoltage logic is designed to automatically reset if less than three consecutive faults appear. This helps to prevent a premature disconnection of the load during high current pulses when the battery pack charge is close to being depleted.

The undervoltage fault is reset by applying charge current to the battery pack. When the voltage on Pin 16 exceeds Pin 11 by 0.6 V, discharge MOSFET Q2 will turned on. The battery pack will now be available for charging or discharging.

Since the thresholds of Pin 7 and 8 are equal, the above equations can be rewritten to directly solve for specific resistor values as shown in the example below.

Let the desired limits be:

V_{OV} = 4.2 V, V_H = 0.4 V, and V_{UV} = 2.5 V

With nominal values for:

V_{th} = 1.23 V, and I_H = 2.0 μA

$$R3 = \frac{\left(\frac{V_H}{I_H}\right)}{\left(\frac{V_{OV}}{V_{th}} - 1\right)} = \frac{\left(\frac{0.4}{2.0 \times 10^{-6}}\right)}{\left(\frac{4.2}{1.23} - 1\right)} = 82{,}828\ \Omega$$

$$R2 = R3\left(\frac{V_{OV}}{V_{UV}} - 1\right) = 82{,}828\left(\frac{4.2}{2.5} - 1\right) = 56{,}323\ \Omega$$

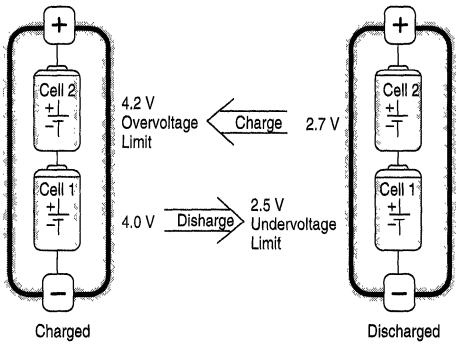
$$R1 = \left(\frac{V_H}{I_H}\right) - R2 = \left(\frac{0.4}{2.0 \times 10^{-6}}\right) - 56{,}323 = 143{,}677\ \Omega$$

Note that the Cell Selector has a maximum total series resistance of 200 Ω. This will have a minimal effect on the programmed limits if the total divider resistance is in excess of 100 kΩ.

Cell Voltage Balancing

With series connected cells, successive charge and discharge cycles can result in a significant difference in cell voltage with a corresponding degradation of battery pack capacity. Figure 4 illustrates the operation of an unbalanced pack. As the cells become unbalanced, the full battery pack capacity is not realized. This is due to the requirement that charging must terminate when Cell 2 reaches the overvoltage limit, and discharging must terminate when Cell 1 reaches the undervoltage limit. By employing a method of keeping the cell voltages equal, both cells can be charged and discharged to their specified limits, thus attaining the maximum possible capacity.

Figure 4. Unbalanced Battery Pack Operation



The MC33347 contains a Cell Voltage Balancing Amplifier that controls four N–channel MOSFETs. The amplifier samples the cell voltages during the polling period. If the detected cell voltage difference exceeds 1.0 %, the MOSFET that connects across the higher voltage cell is turned on. The excess charge will eventually be bled off through the internal 80 Ω resistor with a typical balancing current that ranges from 40 mA to 80 mA. If higher balancing currents are desired, Pins 1 and 2 provide a means for paralleling a lower value external resistor for in excess of 500 mA. The use of an external resistor allows a reduction of on–chip power dissipation. Cell voltage balancing is active during charge and discharge, but disabled during the low current sleepmode state.

Cell Programming and Test

The protection circuit can be programmed for operation with either one or two cell battery packs. The Cell Programming/Test input, Pin 13, is used to control the Cell Selector and to enable or disable the Cell Voltage Balancing Amplifier. For one cell operation, Pin 13 is connected to Pin 16, and Pin 4 is connected to Pin 3 and the positive terminal of Cell 1, refer to Figure 8. For two cell operation, Pin 13, is connected to Pin 3 and the positive terminal of Cell 1, and Pin 4 is connected to the positive terminal of Cell 2, refer to Figure 7.

A test option is provided to speed up device and battery pack testing. By biasing Pin 13 above Pin 3 by 2.0 V, the internal logic is held in a reset state and both MOSFET switches are turned on. Upon release, the logic becomes active and the cells are polled within 2.0 ms.

Current Sensing

Charge and discharge current limit protection can be selectively added to the battery pack with the addition of a sense resistor. The resistors are placed in series with the positive terminal of the battery pack and the cells. Refer to Figure 1.

As the battery pack charges, Pins 9 and 10 sense the voltage drop across $R_{Lim(chg)}$. A charge current limit fault is

detected if the voltage at Pin 10 exceeds Pin 9 by 18 mV. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. As a result of the charge current fault, the battery pack is available for discharging only. The charge current limit is given by:

$$I_{Lim(chg)} = \frac{V_{th(chg)}}{R_{Lim(chg)}} = \frac{18\ mV}{R_{Lim(chg)}}$$

The charge current fault is reset by either disconnecting the battery pack from the charger, or by connecting a load to the battery pack. When the voltage on Pin 16 no longer exceeds Pin 11 by approximately 2.0 V, the Sense Enable circuit will turn on charge MOSFET Q1. Charge current sensing can be disabled by connecting Pin 10 to Pin 9.

The discharge current limiting operates in a similar manner. As the battery pack discharges, Pins 4 and 9 sense the voltage drop across $R_{Lim(dschg)}$. A discharge current limit fault is detected if the voltage at Pin 4 is less than Pin 9 by 50 mV. The fault information is stored in a data latch and discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. As a result of the discharge current fault, the battery pack is available for charging only. The discharge current limit is given by:

$$I_{Lim(dschg)} = \frac{V_{th(dschg)}}{R_{Lim(dschg)}} = \frac{50\ mV}{R_{Lim(dschg)}}$$

The discharge current fault is reset by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger. When the voltage on Pin 11 no longer exceeds Pin 16 by approximately 2.0 V, the Sense Enable circuit will turn on discharge MOSFET Q2. Discharge current sensing can be disabled by connecting Pin 4 to Pin 9.

The charge and discharge current protection circuits contain a built in response delay of 3.0 ms. This helps to prevent fault activation when the battery pack is subjected to pulsed currents during charging or discharging. An additional current sense delay can selectively be added as shown in Figure 5.

3

Charge Pump and MOSFET Switches

The MC33347 contains an on chip Charge Pump to ensure that the MOSFET switches are fully enhanced for reduced power losses. An external reservoir capacitor normally connects from the Charge Pump output to ground, Pins 15 and 16. The capacitor value is not critical and is usually within the range of 10 nF to 100 nF. The Charge Pump output is regulated at 10.2 V allowing the use of economical logic level MOSFETs in one and two cell applications. The main requirement in selecting a particular type of MOSFET switch is to consider the desired on–resistance at the lowest anticipated operating voltage of the battery pack. A table of small outline surface mount devices is given in Figure 6. When using extremely low threshold MOSFETs, it may be desirable to disable the Charge Pump so that the maximum gate to source voltage is not exceeded. This is accomplished by connecting Pin 15 to Pin 4. Application Figures 7 and 8 show a capacitor labeled C_{ESD}. This capacitor provides a path around the MOSFET switches in the event of an electrostatic discharge.

Figure 5. Additional Current Limit Delay

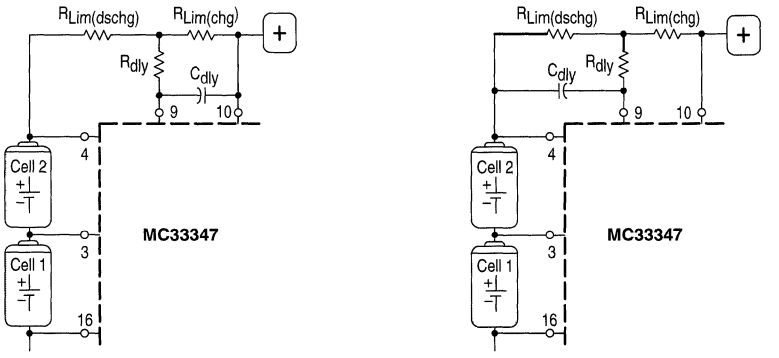


Figure 6. Small Outline Surface Mount MOSFET Switches

Device Type	On–Resistance (Ω) versus Gate to Source Voltage (V)						
	2.5 V	3.0 V	4.0 V	5.0 V	6.0 V	7.5 V	9.0 V
MMFT3055VL	–	–	–	0.120 Ω	0.115 Ω	0.108 Ω	0.100 Ω
MMDF3N03HD	–	0.525 Ω	0.080 Ω	0.065 Ω	0.063 Ω	0.062 Ω	0.060 Ω
MMDF4N01HD	0.047 Ω	0.042 Ω	0.037 Ω	0.035 Ω	0.034 Ω	0.033 Ω	See Note
MMSF5N02HD	–	0.065 Ω	0.023 Ω	0.021 Ω	0.020 Ω	0.018 Ω	0.018 Ω
MMDF6N02HD	0.043 Ω	0.035 Ω	0.029 Ω	0.028 Ω	0.026 Ω	0.025 Ω	0.023 Ω

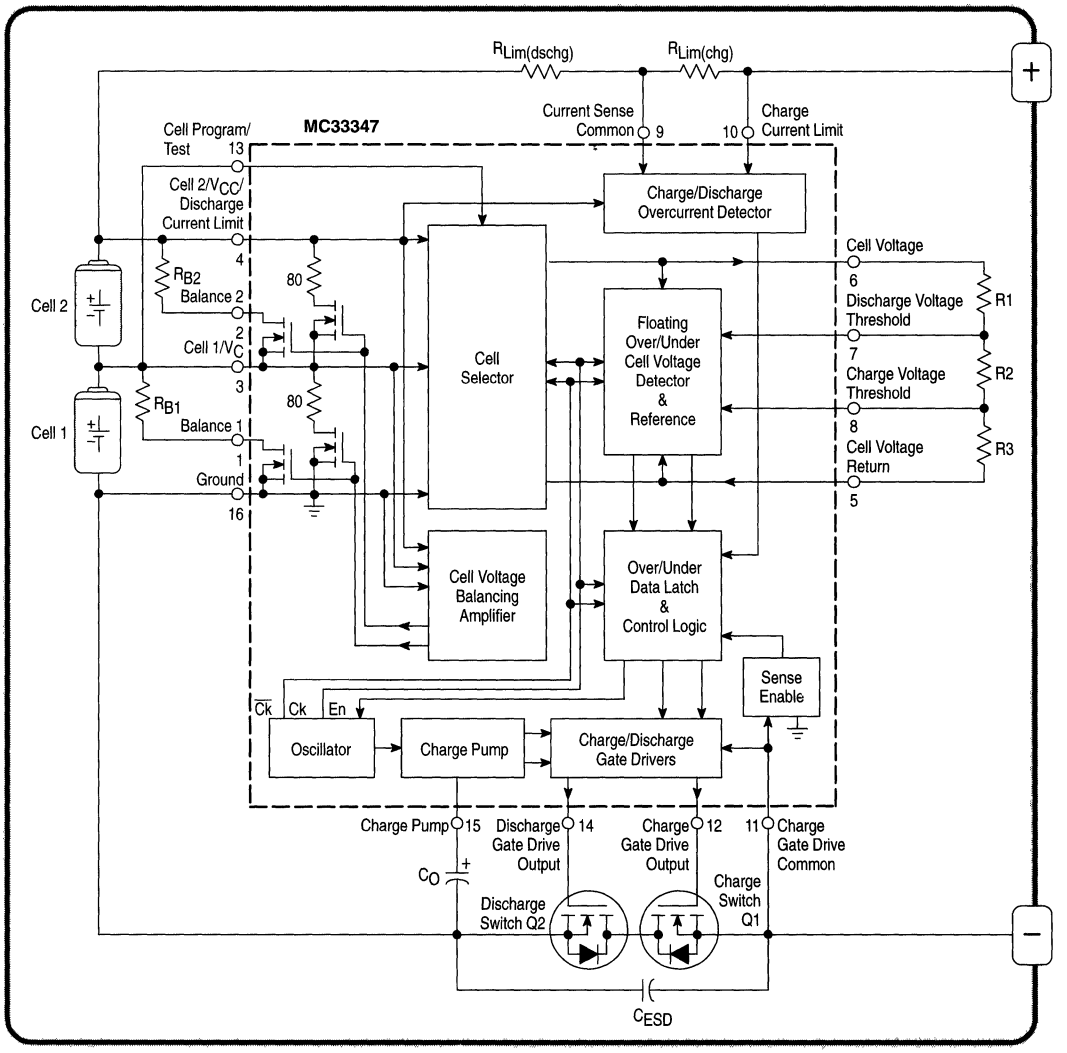
NOTE: Exceeds maximum V_{GS} voltage rating.

PROTECTION CIRCUIT OPERATING MODE TABLE

Input Conditions Cell Status	Circuit Operation Battery Pack Status	Outputs			
		MOSFET Switches		Function	
		Charge Q1	Discharge Q2	Charge Pump	Cell Balancing (See Note)
CELL CHARGING/DISCHARGING					
Storage or Nominal Operation: No current or voltage faults	Both Charge MOSFET Q1 and Discharge MOSFET Q2 are on. The battery pack is available for charging or discharging.	On	On	Active	Active
CELL CHARGING FAULT/RESET					
Charge Current Limit Fault: $V_{Pin\ 10} \geq (V_{Pin\ 9} + 18\ mV)$ for 3.0 ms	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. Q1 will remain in the off state as long as $V_{Pin\ 16}$ exceeds $V_{Pin\ 11}$ by ≈ 2.0 V. The battery pack is available for discharging.	On to Off	On	Active	Active
Charge Current Limit Reset: $V_{Pin\ 16} - V_{Pin\ 11} < 2.0\ V$	The Sense Enable circuit will reset and turn on charge MOSFET Q1 when $V_{Pin\ 16}$ no longer exceeds $V_{Pin\ 11}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the charger from the battery pack, or by connecting a load to the battery pack.	Off to On	On	Active	Active
Charge Voltage Limit Fault: $V_{Pin\ 8} \geq 1.23\ V$ for 1.0 s	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. An internal current source pull–up of 2.0 μA is applied to Pin 8 creating an input hysteresis voltage of V_H with divider resistors R1 and R2. The battery pack is available for discharging.	On to Off	On	Active	Active
Charge Voltage Limit Reset: $V_{Pin\ 8} < 1.23\ V$ for 1.0 s	Charge MOSFET Q1 will turn on when the voltage across each cell falls sufficiently to overcome the input hysteresis voltage. This can be accomplished by applying a load to the battery pack.	Off to On	On	Active	Active
CELL DISCHARGING FAULT/RESET					
Discharge Current Limit Fault: $V_{Pin\ 4} \leq (V_{Pin\ 9} - 50\ mV)$ for 3.0 ms	Discharge MOSFET Q2 is latched off and the cells are disconnected from the load. Q2 will remain in the off state as long as $V_{Pin\ 11}$ exceeds $V_{Pin\ 16}$ by ≈ 2.0 V. The battery pack is available for charging.	On	On to Off	Active	Active
Discharge Current Limit Reset: $V_{Pin\ 11} - V_{Pin\ 16} < 2.0\ V$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 11}$ no longer exceeds $V_{Pin\ 16}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger.	On	Off to On	Active	Active
Discharge Voltage Limit Fault: $V_{Pin\ 7} \leq 1.23\ V$ for three consecutive 1.0 s samples	Discharge MOSFET Q2 is latched off, the cells are disconnected from the load, and the protection circuit enters a low current sleepmode state. The battery pack is available for charging.	On	On to Off	Disabled	Disabled
Discharge Voltage Limit Reset: $V_{Pin\ 16} > (V_{Pin\ 11} + 0.6\ V)$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 16}$ exceeds $V_{Pin\ 11}$ by 0.6 V. This can be accomplished by connecting the battery pack to the charger.	On	Off to On	Active	Active
FAULTY CELL					
Simultaneous Charge and Discharge Voltage Limit Faults: $V_{Pin\ 8} \geq 1.23\ V$ for 1.0 s and $V_{Pin\ 7} \leq 1.23\ V$ for three consecutive 1.0 s samples	This condition can happen if there is a defective cell in the battery pack. The protection circuit will remain in the sleepmode state until the battery pack is connected to a charger. If Cell 2 is faulty and a charger is connected, the protection circuit will cycle in and out of sleepmode. If Cell 1 is faulty (<1.5 V), the protection circuit logic will not function and the battery pack cannot be charged.	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty

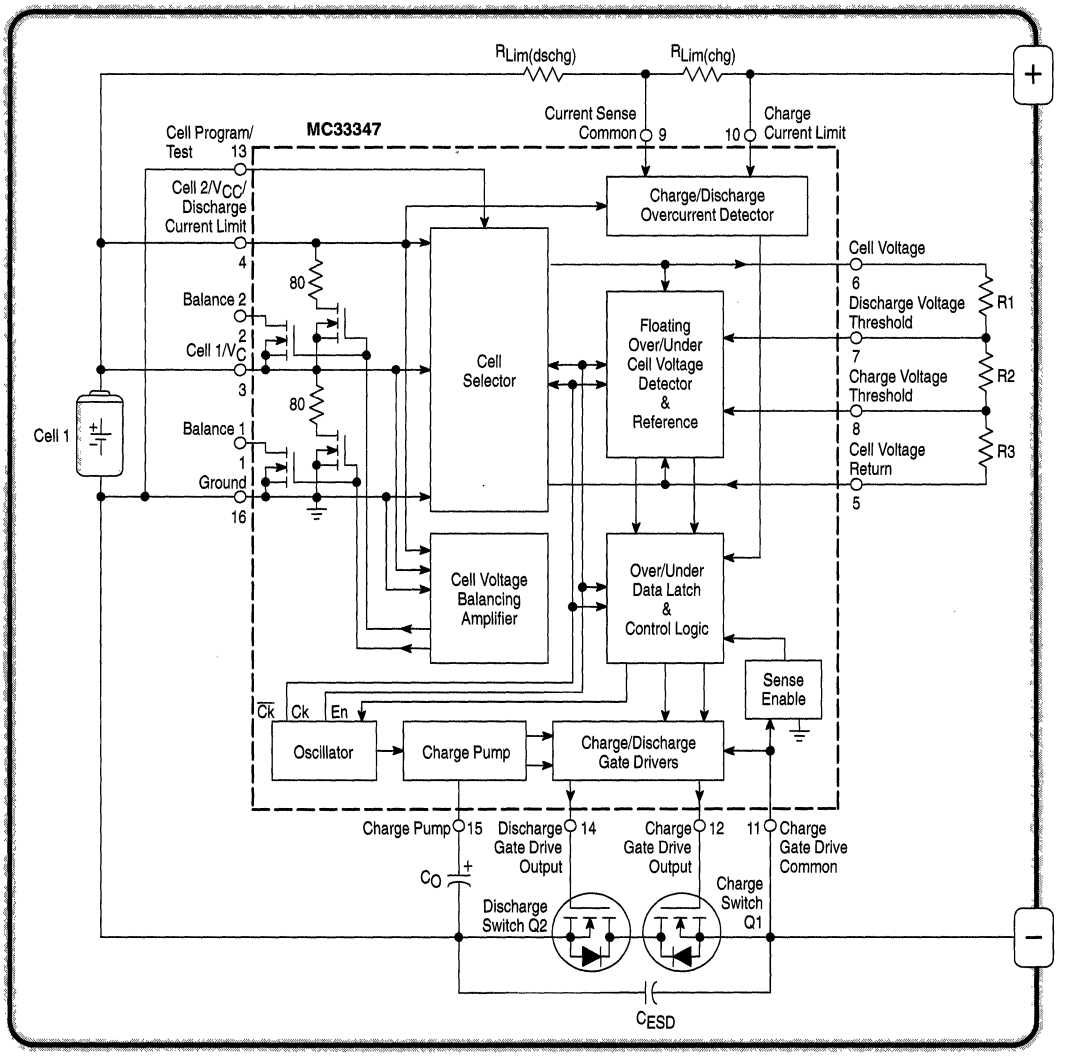
NOTE: Cell balancing is not active when programmed for one cell operation.

Figure 7. Two Cell Smart Battery Pack



3

Figure 8. One Cell Smart Battery Pack



MC33348

3

Product Preview

Lithium Battery Protection Circuit for One Cell Battery Packs

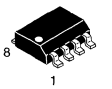
The MC33348 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one cell rechargeable battery pack. Cell protection features consist of internally trimmed charge and discharge voltage limits, discharge current limit detection with a delayed shutdown, and a virtually zero current sleepmode state when the cell is discharged. An additional feature includes an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. This MC33348 is available in standard and micro 8 lead surface mount packages.

- Internally Trimmed Charge and Discharge Voltage Limits
- Discharge Current Limit Detection with Delayed Shutdown
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Dedicated for One Cell Applications
- Minimum Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Ordering Information shown on following page.

LITHIUM BATTERY PROTECTION CIRCUIT FOR ONE CELL SMART BATTERY PACKS

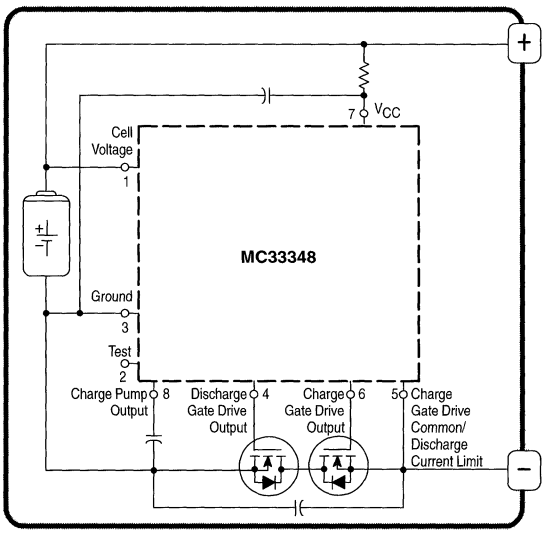
SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

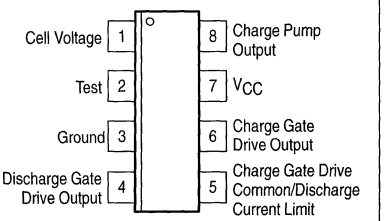
DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)

Typical One Cell Smart Battery Pack



This device contains 1170 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Charge Overvoltage Threshold (V)	Charge Overvoltage Hysteresis (mV)	Discharge Undervoltage Threshold (V)	Discharge Current Limit Threshold (mV)	Operating Temperature Range	Package
MC33348D–1	4.20	300	2.25	400	T_A = –25° to +85°C	SO–8
MC33348D–2				200		
MC33348D–3	4.25		2.28	400		
MC33348D–4				200		
MC33348D–5	4.35		2.30	400		
MC33348D–6				200		
MC33348DM–1	4.20		2.25	400		Micro–8
MC33348DM–2				200		
MC33348DM–3	4.25		2.28	400		
MC33348DM–4				200		
MC33348DM–5	4.35		2.30	400		
MC33348DM–6				200		

NOTE: Additional threshold limit options can be made available. Consult your local Motorola sales office for information.

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage (Measured with Respect to Ground, Pin 3)	V_{IR}		V
Cell Voltage (Pin 1)		7.5	
Test (Pin 2)		7.5	
Discharge Gate Drive Output (Pin 4)		18	
Charge Gate Drive Common/Discharge Current Limit (Pin 5)		±20	
Charge Gate Drive Output (Pin 6)		18 to –20	
V_{CC} (Pin 7)		7.5	
Charge Pump Output (Pin 8)		18	
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$		°C/W
DM Suffix, Micro–8 Plastic Package, Case 846A		240	
D Suffix, SO–8 Plastic Package, Case 751		178	
Operating Junction Temperature (Note 1)	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

NOTE: 1. Tested ambient temperature range for the MC33348:
T_{low} = –25°C T_{high} = +85°C
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE SENSING					
Cell Charging Cutoff (Pin 1 to Pin 3)					
Overvoltage Threshold, V_{Cell} Increasing	$V_{th(OV)}$				V
–1 Suffix		–	4.20	–	
–2 Suffix		–	4.20	–	
–3 Suffix		–	4.25	–	
–4 Suffix		–	4.25	–	
–5 Suffix		–	4.35	–	
–6 Suffix		–	4.35	–	
Overvoltage Hysteresis V_{Cell} Decreasing	V_H				mV
–1 Suffix		–	300	–	
–2 Suffix		–	300	–	
–3 Suffix		–	300	–	
–4 Suffix		–	300	–	
–5 Suffix		–	300	–	
–6 Suffix		–	300	–	
Cell Discharging Cutoff (Pin 1 to Pin 3, T_A = 25°C)					
Undervoltage Threshold, V_{Cell} Decreasing	$V_{th(UV)}$				V
–1 Suffix		–	2.25	–	
–2 Suffix		–	2.25	–	
–3 Suffix		–	2.28	–	
–4 Suffix		–	2.28	–	
–5 Suffix		–	2.30	–	
–6 Suffix		–	2.30	–	
Input Bias Current During Cell Voltage Sample (Pin 1)	I_{IIB}	–	28	–	µA
Cell Voltage Sampling Rate	$t_{(smpl)}$	–	1.0	–	s
CURRENT SENSING					
Discharge Current Limit (Pin 5 to Pin 3)					
Threshold Voltage	$V_{th(dschg)}$				mV
–1 Suffix		–	400	–	
–2 Suffix		–	200	–	
–3 Suffix		–	400	–	
–4 Suffix		–	200	–	
–5 Suffix		–	400	–	
–6 Suffix		–	200	–	
Delay	$I_{dly(dschg)}$	–	3.0	–	ms
CHARGE PUMP					
Output Voltage (Pin 8, $R_L \geq 10^{10}\ \Omega$)	V_O	–	10.2	–	V
TOTAL DEVICE					
Average Cell Current	I_{CC}				
Operating (V_{CC} = 4.0 V)		–	20	–	µA
Sleepmode (V_{CC} = 2.0 V)		–	1.4	–	nA
Minimum Operating Cell Voltage for Logic and Gate Drivers	V_{CC}	–	1.5	–	V

NOTE: 1. Tested ambient temperature range for the MC33348:
T_{low} = –25°C T_{high} = +85°C

Figure 1. Charge and Discharge Threshold Voltage Change versus Temperature

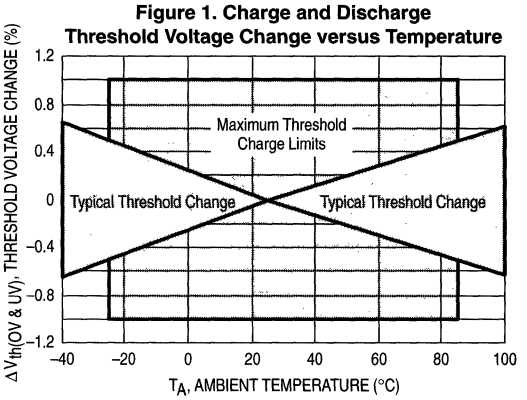


Figure 2. Discharge Current Limit Threshold Voltage Change versus Temperature

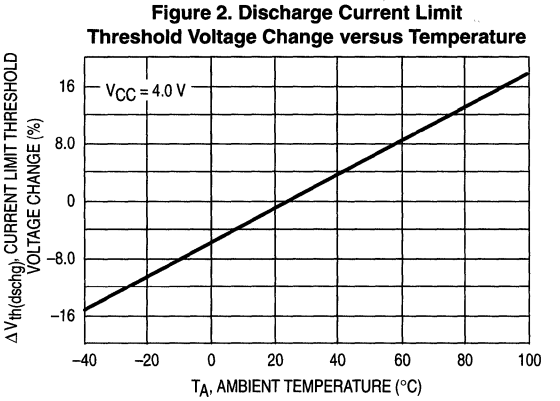


Figure 3. Gate Drive Output Voltage versus Load Current

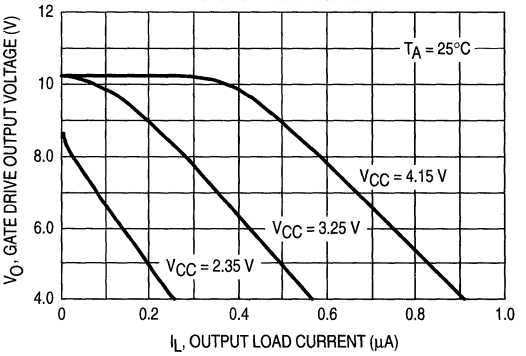


Figure 4. Gate Drive Output Voltage versus Supply Voltage

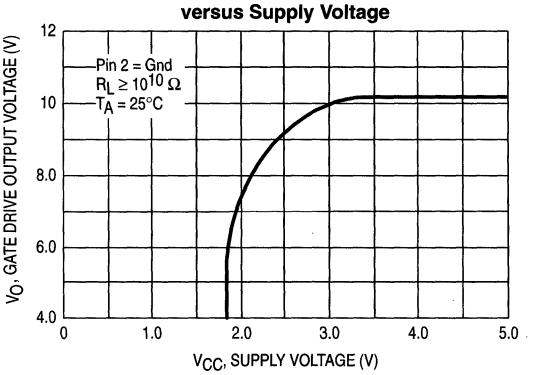


Figure 5. Charge Pump Output Voltage versus Temperature

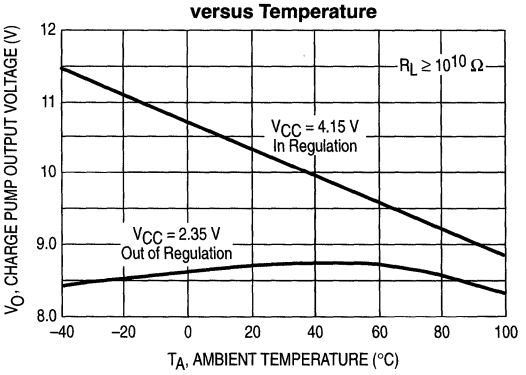
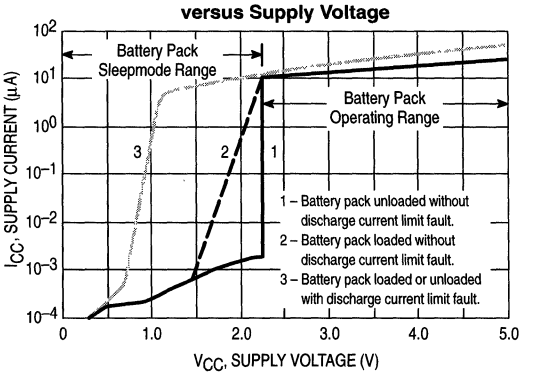


Figure 6. Supply Current versus Supply Voltage

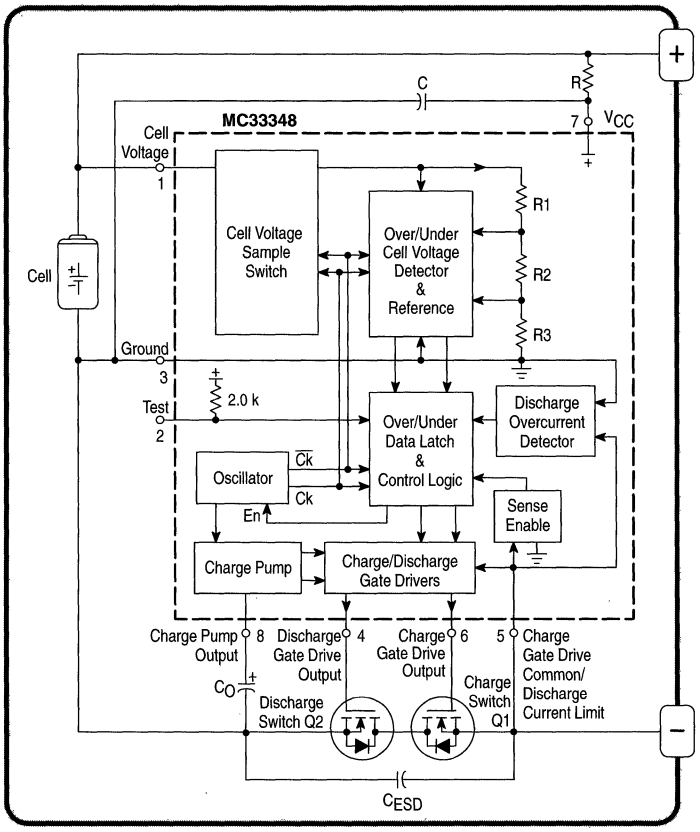


PROTECTION CIRCUIT OPERATING MODE TABLE

Input Conditions Cell Status	Circuit Operation Battery Pack Status	Outputs MOSFET Switches Charge Q1	Outputs MOSFET Switches Discharge Q2	Outputs Function Charge Pump
CELL CHARGING/DISCHARGING				
Storage or Nominal Operation: No current or voltage faults	Both Charge MOSFET Q1 and Discharge MOSFET Q2 are on. The battery pack is available for charging or discharging.	On	On	Active
CELL CHARGING FAULT/RESET				
Charge Voltage Limit Fault: $V_{Pin\ 1} \geq V_{th(OV)}$ for 1.0 s	Charge MOSFET Q1 is latched off and the cell is disconnected from the charging source. An internal current source pull–up is applied to divider resistors R1 and R2 creating a hysteresis voltage of V_H. The battery pack is available for discharging. Discharge current limit protection is disabled.	On to Off	On	Active
Charge Voltage Limit Reset: $V_{Pin\ 1} < (V_{th(OV)} - V_H)$ for 1.0 s	Charge MOSFET Q1 will turn on when the voltage across the cell falls sufficiently to overcome hysteresis voltage V_H. This can be accomplished by applying a load to the battery pack. Discharge current limit protection is enabled.	Off to On	On	Active
CELL DISCHARGING FAULT/RESET				
Discharge Current Limit Fault: $V_{Pin\ 5} \geq (V_{Pin\ 1} + 400\ mV)$ for 3.0 ms and $V_{Pin\ 1} < (V_{th(OV)} - V_H)$ for 1.0 ms	Discharge MOSFET Q2 is latched off and the cell is disconnected from the load. Q2 will remain in the off state as long as $V_{Pin\ 5}$ exceeds $V_{Pin\ 3}$ by ≈ 2.0 V. The battery pack is available for charging.	On	On to Off	Active
Discharge Current Limit Reset: $V_{Pin\ 5} - V_{Pin\ 3} < 2.0$ V	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 3}$ no longer exceeds $V_{Pin\ 5}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger.	On	Off to On	Active
Discharge Voltage Limit Fault: $V_{Pin\ 1} \leq V_{th(UV)}$ for three consecutive 1.0 s samples	Discharge MOSFET Q2 is latched off, the cells are disconnected from the load, and the protection circuit enters a low current sleepmode state. The battery pack is available for charging.	On	On to Off	Disabled
Discharge Voltage Limit Reset: $V_{Pin\ 3} > (V_{Pin\ 5} + 0.6\ V)$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 3}$ exceeds $V_{Pin\ 5}$ by 0.6 V. This can be accomplished by connecting the battery pack to the charger.	On	Off to On	Active
FAULTY CELL				
Discharge Voltage Limit Fault: $V_{Pin\ 1} \leq 1.5$ V	This condition can happen if the cell is a defective (<1.5 V). The protection circuit logic will not function and the battery pack cannot be charged.	Disabled	Disabled	Disabled

3

Figure 7. One Cell Smart Battery Pack



PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Cell Voltage	This input is connected to the positive terminal of the cell for voltage monitoring. Internally, the Cell Voltage Sample Switch applies this voltage to a resistor divider where it is compared by the Cell Voltage Detector to an internal reference.
2	Test	This pin is normally not connected and is used in testing the protection IC. An active low at this input resets the internal logic and turns on both MOSFET switches. Upon release, the logic becomes active and the cell voltage is sampled within 1.0 ms.
3	Ground	This is the protection IC ground and all voltage ratings are with respect to this pin.
4	Discharge Gate Drive Output	This output connects to the gate of discharge switch Q2 allowing it to enable or disable battery pack discharging.
5	Charge Gate Drive Common/Discharge Current Limit	This is a multifunction pin that is used to monitor cell discharge current and to provide a gate turn–off path for charge switch Q1. A discharge current limit fault is set when the battery pack load causes the combined voltage drop of charge switch Q1 and discharge switch Q2 to exceed the discharge current limit threshold voltage, $V_{th(dschg)}$, with respect to Pin 3.
6	Charge Gate Drive Output	This output connects to the gate of charge switch Q1 allowing it to enable or disable battery pack charging.
7	V_{CC}	This pin is the positive supply voltage for the protection IC.
8	Charge Pump Output	This is the charge pump output. A reservoir capacitor is connected from this pin to ground.

INTRODUCTION

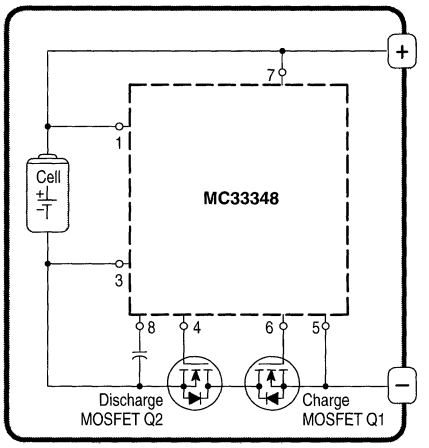
The insatiable demand for smaller lightweight portable electronic equipment has dramatically increased the requirements of battery performance. Batteries are expected to have higher energy densities, superior cycle life, be safe in operation and environmentally friendly. To address these high expectations, battery manufacturers have invested heavily in developing rechargeable lithium–based cells. Today's most attractive chemistries include lithium–polymer, lithium–ion, and lithium–metal. Each of these chemistries require electronic protection in order to constrain cell operation to within the manufacturers limits.

Rechargeable lithium–based cells require precise charge and discharge termination limits for both voltage and current in order to maximize cell capacity, cycle life, and to protect the end user from a catastrophic event. The termination limits are not as well defined as with older non–lithium chemistries. These limits are dependent upon a manufacturer's particular lithium chemistry, construction technique, and intended application. Battery pack assemblers may also choose to enhance cell capacity at the expense of cycle life. In order to address these requirements, six versions of the MC33348 protection circuit were developed. These devices feature charge overvoltage protection, discharge current limit protection with delayed shutdown, low operating current, a virtually zero current sleepmode state, and requires few external components to implement a complete one cell smart battery pack.

Operating Description

The MC33348 is specifically designed to be placed in the battery pack where it is continuously powered from a single lithium cell. In order to maintain cell operation within specified limits, the protection circuit senses both cell voltage and discharge current, and correspondingly controls the state of two N–channel MOSFET switches. These switches, Q1 and Q2, are placed in series with the negative terminal of the Cell and the negative terminal of the battery pack. This configuration allows the protection circuit to interrupt the appropriate charge or discharge path FET in the event that either a voltage threshold or the discharge current limit for the cell has been exceeded.

Figure 8. Simplified One Cell Smart Battery Pack



A functional description of the protection circuit blocks follows. Refer to the detailed block diagram shown in Figure 7.

Voltage Sensing

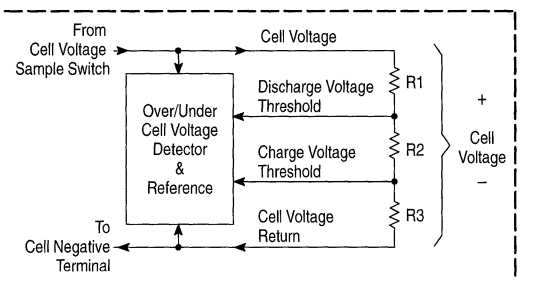
Voltage sensing is accomplished by the use of the Cell Voltage Sample Switch in conjunction with the Over/Under Voltage Detector and Reference block. The Sample Switch applies the cell voltage to the top resistor of an internal divider string. The voltage at each of the tap points is sequentially polled and compared to an internal reference. If a limit has been exceeded, the result is stored in the Over/Under Data Latch and Control Logic block. The Cell Voltage Sample Switch is gated on for a 1.0 ms period at a one second repetition rate. This low duty cycle sampling technique reduces the average load current that the divider presents across the cell, thus extending the useful battery pack capacity. The cell voltage limits are tested in the following sequence:

Figure 9. Cell Sensing Sequence

Polling Sequence	Time (ms)	Tested Limit
1	0.5	Overvoltage
2	0.5	Undervoltage

By incorporating this polling technique with a single comparator and voltage divider, a significant reduction of circuitry and trim elements is achieved. This results in a smaller die size, lower cost, and reduced operating current.

Figure 10. Cell Voltage Limit Sampling



The cell charge and discharge voltage limits are controlled by the values selected for the internal resistor divider string and the comparator input threshold. As the battery pack reaches full charge, the Cell Voltage Detector will sense an overvoltage fault condition when the cell exceeds the designed overvoltage limit. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. An internal current source pull–up is then applied to lower tap of the divider, creating a hysteresis voltage. As a result of an overvoltage fault, the battery pack is available for discharging only.

The overvoltage fault is reset by applying a load to the battery pack. As the voltage across the cell falls below the hysteresis level, charge MOSFET Q1 will turn on. The battery pack will now be available for charging or discharging.

As the load eventually depletes the battery pack charge, the Cell Voltage Detector will sense an undervoltage fault

condition when the cell falls below the designed undervoltage limit. After three consecutive faults are detected, discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. The protection circuit will now enter a low current sleepmode state drawing less than 10 nA, thus preventing any further cell discharging. As a result of the undervoltage fault, the battery pack is available for charging only. The typical cutoff thresholds and hysteresis voltage are shown in Figure 11.

Figure 11. Cutoff and Hysteresis Limits

Device Suffix	Charging Cutoff (V)	Hysteresis (mV)	Disharging Cutoff (V)
–1, –2	4.20	300	2.25
–3, –4	4.25	300	2.28
–5, –6	4.35	300	2.30

The undervoltage logic is designed to automatically reset if less than three consecutive faults appear. This helps to prevent a premature disconnection of the load during high current pulses when the battery pack charge is close to being depleted.

The undervoltage fault is reset by applying charge current to the battery pack. When the voltage on Pin 3 exceeds Pin 5 by 0.6 V, discharge MOSFET Q2 will turned on. The battery pack will now be available for charging or discharging.

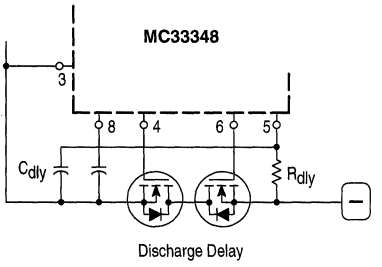
Current Sensing

Discharge current limit protection is internally provided by the MC33348. As the battery pack discharges, Pins 8 and 5 sense the voltage drop across MOSFETs Q1 and Q2. A discharge current limit fault is detected if the voltage at Pin 5 is greater than Pin 3 by 400 mV for –1, –3 and –5 suffix devices, or 200 mV for –2, –4 and –6 suffix devices. The fault information is stored in a data latch and discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. As a result of the discharge current fault, the battery pack is available for charging only. The discharge current limit is given by:

$$I_{Lim(dschg)} = \frac{V_{th(dschg)}}{R_{Lim(dschg)}} = \frac{V_{th(dschg)}}{R_{DS(on)Q1} + R_{DS(on)Q2}}$$

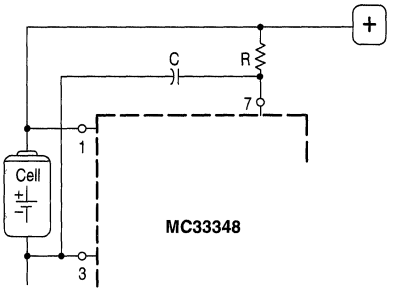
The discharge current fault is reset by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger. When the voltage on Pin 5 no longer exceeds Pin 3 by approximately 2.0 V, the Sense Enable circuit will turn on discharge MOSFET Q2.

Figure 12. Additional Current Limit Delay



Discharge Delay

Figure 13. V_{CC} Decoupling



Power Supply Decoupling

As previously stated in the voltage sensing operating description, charge MOSFET Q1 is held off during an overvoltage fault condition. When this condition is present, the discharge current limit protection function is internally disabled. This is required, since the voltage across Q1, in the off state, would exceed the current sense threshold. This would cause Q2 to turn off as well, preventing both charging and discharging of the cell. Discharge current limit protection is enabled whenever an overvoltage fault is not present.

The discharge current protection circuit contain a built in response delay of 3.0 ms. This helps to prevent fault activation when the battery pack is subjected to pulsed currents during discharging. An additional current sense delay can be added as shown in Figure 12. If the battery pack is subjected to extremely high discharge current pulses or is shorted, the V_{CC} pin must be decoupled from the cell. This is required so that the protection circuit will have sufficient operating voltage during the load transient, to ensure turn off of discharge MOSFET Q2. Figure 13 shows the placement of decoupling components.

Charge Pump and MOSFET Switches

The MC33348 contains an on chip Charge Pump to ensure that the MOSFET switches are fully enhanced for reduced power losses. An external reservoir capacitor normally connects from the Charge Pump output to ground, Pins 8 and 3. The capacitor value is not critical and is usually within the range of 10 nF to 100 nF. The Charge Pump output is regulated at 10.2 V allowing the use of economical logic level MOSFETs. The main requirement in selecting a particular type of MOSFET switch is to consider the desired on–resistance at the lowest anticipated operating voltage of the battery pack. A table of small outline surface mount devices is given in Figure 14. When using extremely low threshold MOSFETs, it may be desirable to disable the Charge Pump so that the maximum gate to source voltage is not exceeded. This is accomplished by connecting Pin 8 to Pin 7. Application Figure 7 show a capacitor labeled C_{ESD}. This capacitor provides a path around the MOSFET switches in the event of an electrostatic discharge.

Testing

A test pin is provided in order to speed up device and battery pack testing. By grounding Pin 2, the internal logic is held in a reset state and both MOSFET switches are turned on. Upon release, the logic becomes active and the cell voltage is polled within 1.0 ms.

Figure 14. Small Outline Surface Mount MOSFET Switches

Device Type	On–Resistance (Ω) versus Gate to Source Voltage (V)						
	2.5 V	3.0 V	4.0 V	5.0 V	6.0 V	7.5 V	9.0 V
MMFT3055VL	–	–	–	0.120 Ω	0.115 Ω	0.108 Ω	0.100 Ω
MMDF3N03HD	–	0.525 Ω	0.080 Ω	0.065 Ω	0.063 Ω	0.062 Ω	0.060 Ω
MMDF4N01HD	0.047 Ω	0.042 Ω	0.037 Ω	0.035 Ω	0.034 Ω	0.033 Ω	See Note
MMSF5N02HD	–	0.065 Ω	0.023 Ω	0.021 Ω	0.020 Ω	0.018 Ω	0.018 Ω
MMDF6N02HD	0.043 Ω	0.035 Ω	0.029 Ω	0.028 Ω	0.026 Ω	0.025 Ω	0.023 Ω

NOTE: Exceeds maximum V_{GS} voltage rating.

MC33362

Advance Information

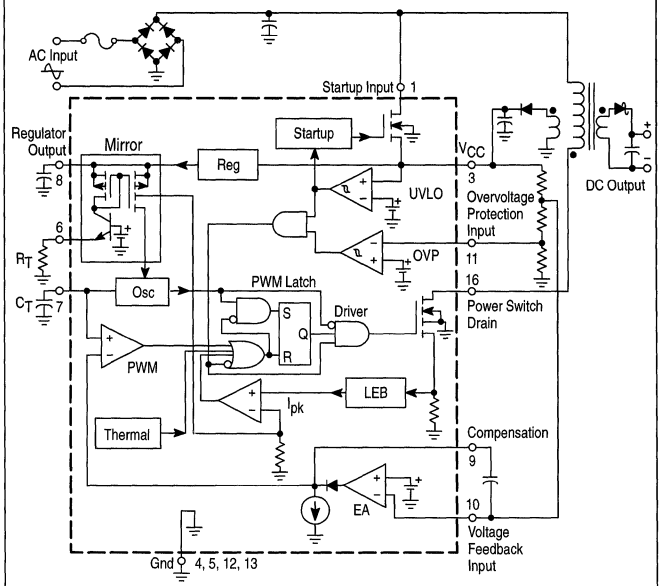
High Voltage Switching Regulator

3

The MC33362 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 120 VAC line source. This integrated circuit features an on–chip 500 V/2.0 A SenseFET power switch, 250 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16–lead dual–in–line and wide body surface mount packages.

- On–Chip 500 V, 2.0 A SenseFET Power Switch
- Rectified 120 VAC Line Source Operation
- On–Chip 250 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown

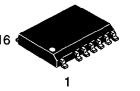
Simplified Application



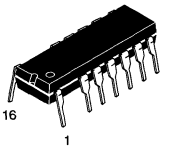
This device contains 221 active transistors.

HIGH VOLTAGE OFF–LINE SWITCHING REGULATOR

SEMICONDUCTOR TECHNICAL DATA

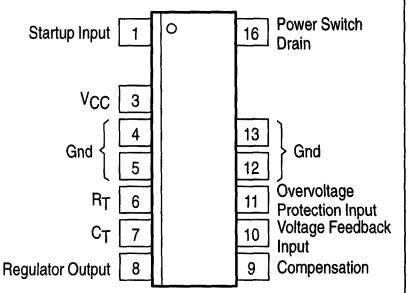


DW SUFFIX
PLASTIC PACKAGE
CASE 751N
(SOP–16L)



P SUFFIX
PLASTIC PACKAGE
CASE 648E
(DIP–16)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33362DW	T_J = –25° to +125°C	SOP–16L
MC33362P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Switch (Pin 16) Drain Voltage Drain Current	 V_{DS} I_{DS}	 500 2.0	 V A
Startup Input Voltage (Pin 1, Note 1) Pin 3 = Gnd Pin 3 ≤ 1000 μF to ground	V_{in}	 250 400	V
Power Supply Voltage (Pin 3)	V_{CC}	40	V
Input Voltage Range Voltage Feedback Input (Pin 10) Compensation (Pin 9) Overvoltage Protection Input (Pin 11) R_T (Pin 6) C_T (Pin 7)	V_{IR}	−1.0 to V_{reg}	V
Thermal Characteristics P Suffix, Dual–In–Line Case 648E Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13) DW Suffix, Surface Mount Case 751N Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13) Refer to Figures 15 and 16 for additional thermal information.	 $R_{\theta JA}$ $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JC}$	 80 15 95 15	°C/W
Operating Junction Temperature	T_J	− 25 to +150	°C
Storage Temperature	T_{stg}	− 55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 20 V, R_T = 10 k, C_T = 390 pF, $C_{Pin\ 8}$ = 1.0 μF, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REGULATOR (Pin 8)					
Output Voltage (I_O = 0 mA, T_J = 25°C)	V_{reg}	5.5	6.5	7.5	V
Line Regulation (V_{CC} = 20 V to 40 V)	Reg_{line}	–	30	500	mV
Load Regulation (I_O = 0 mA to 10 mA)	Reg_{load}	–	44	200	mV
Total Output Variation over Line, Load, and Temperature	V_{reg}	5.3	–	8.0	V
OSCILLATOR (Pin 7)					
Frequency C_T = 390 pF T_J = 25°C (V_{CC} = 20 V) T_J = T_{low} to T_{high} (V_{CC} = 20 V to 40 V) C_T = 2.0 nF T_J = 25°C (V_{CC} = 20 V) T_J = T_{low} to T_{high} (V_{CC} = 20 V to 40 V)	f_{OSC}	 260 255 60 59	 285 – 67.5 –	 310 315 75 76	kHz
Frequency Change with Voltage (V_{CC} = 20 V to 40 V)	$\Delta f_{OSC}/\Delta V$	–	0.1	2.0	kHz
ERROR AMPLIFIER (Pins 9, 10)					
Voltage Feedback Input Threshold	V_{FB}	2.52	2.6	2.68	V
Line Regulation (V_{CC} = 20 V to 40 V, T_J = 25°C)	Reg_{line}	–	0.6	5.0	mV
Input Bias Current (V_{FB} = 2.6 V)	I_{IB}	–	20	500	nA
Open Loop Voltage Gain (T_J= 25°C)	A_{VOL}	–	82	–	dB
Gain Bandwidth Product (f = 100 kHz, T_J= 25°C)	GBW	–	1.0	–	MHz

NOTES: 1. Maximum power dissipation limits must be observed.
2. Tested junction temperature range for the MC33362:
T_{low} = −25°C T_{high} = +125°C

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 20 V, R_T = 10 k, C_T = 390 pF, $C_{Pin\ 8}$ = 1.0 μF, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER (Pins 9, 10)					
Output Voltage Swing High State (I_{Source} = 100 μA, V_{FB} < 2.0 V) Low State (I_{Sink} = 100 μA, V_{FB} > 3.0 V)	 V_{OH} V_{OL}	 4.0 –	 5.3 0.2	 – 0.35	V
OVERVOLTAGE DETECTION (Pin 11)					
Input Threshold Voltage	V_{th}	2.47	2.6	2.73	V
Input Bias Current (V_{in} = 2.6 V)	I_{IB}	–	100	500	nA
PWM COMPARATOR (Pins 7, 9)					
Duty Cycle Maximum (V_{FB} = 0 V) Minimum (V_{FB} = 2.7 V)	 $DC_{(max)}$ $DC_{(min)}$	 48 –	 50 0	 52 0	%
POWER SWITCH (Pin 16)					
Drain–Source On–State Resistance (I_D = 200 mA) T_J = 25°C T_J = T_{low} to T_{high}	$R_{DS(on)}$	 – –	 4.4 –	 6.0 12	Ω
Drain–Source Off–State Leakage Current (V_{DS} = 500 V)	$I_{D(off)}$	–	0.2	50	μA
Rise Time	t_r	–	50	–	ns
Fall Time	t_f	–	50	–	ns
OVERCURRENT COMPARATOR (Pin 16)					
Current Limit Threshold (R_T = 10 k)	I_{lim}	0.7	0.9	1.1	A
STARTUP CONTROL (Pin 1)					
Peak Startup Current (V_{in} = 200 V) V_{CC} = 0 V V_{CC} = ($V_{th(on)}$ – 0.2 V)	I_{start}	 – –	 55 26	 – –	mA
Off–State Leakage Current (V_{in} = 50 V, V_{CC} = 20 V)	$I_{D(off)}$	–	40	200	μA
UNDERVOLTAGE LOCKOUT (Pin 3)					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	11	14.5	18	V
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$	7.5	9.5	11.5	V
TOTAL DEVICE (Pin 3)					
Power Supply Current Startup (V_{CC} = 10 V, Pin 1 Open) Operating	I_{CC}	 – –	 0.3 3.6	 0.5 5.0	mA

Figure 1. Oscillator Frequency versus Timing Resistor

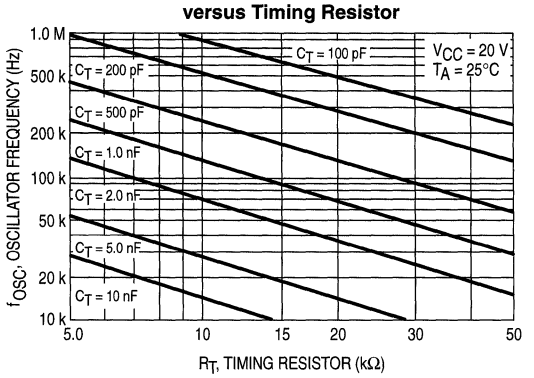


Figure 2. Power Switch Peak Drain Current versus Timing Resistor

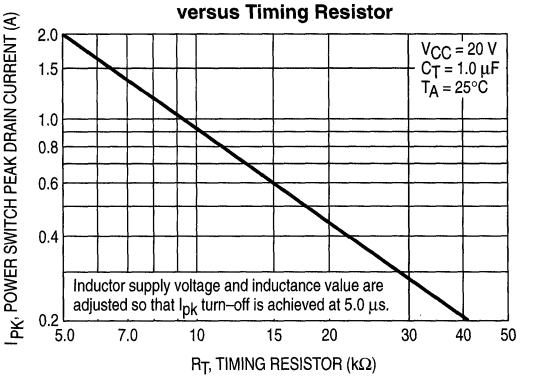


Figure 3. Oscillator Charge/Discharge Current versus Timing Resistor

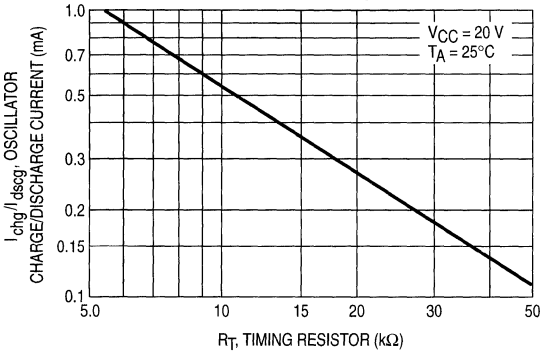


Figure 4. Maximum Output Duty Cycle versus Timing Resistor Ratio

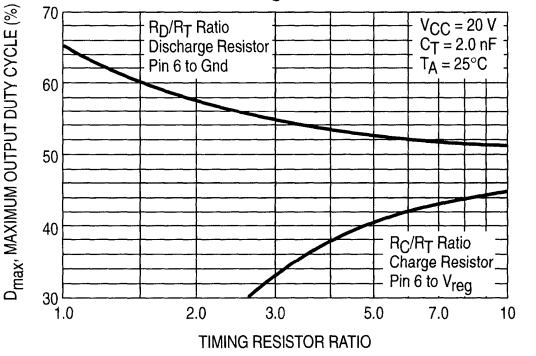


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

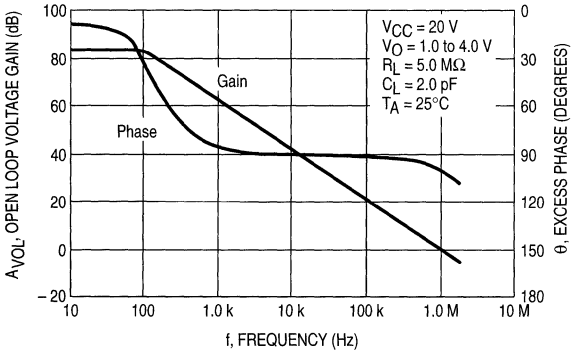


Figure 6. Error Amp Output Saturation Voltage versus Load Current

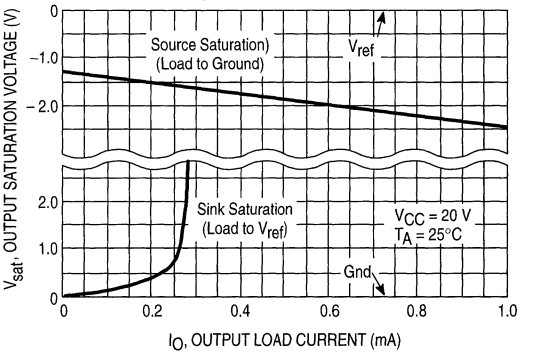


Figure 7. Error Amplifier Small Signal Transient Response

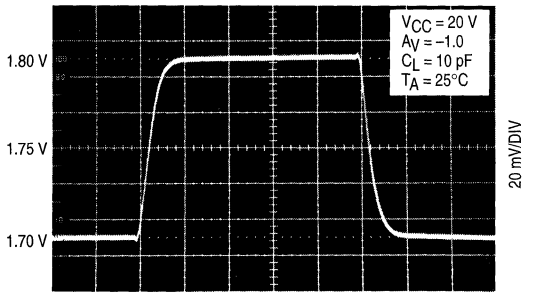


Figure 8. Error Amplifier Large Signal Transient Response

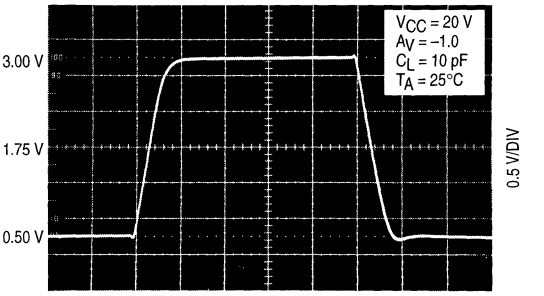


Figure 9. Regulator Output Voltage Change versus Source Current

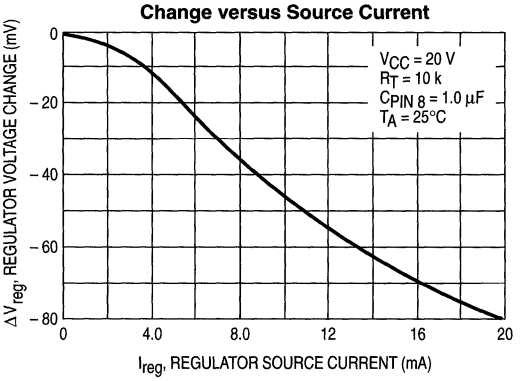


Figure 10. Peak Startup Current versus Power Supply Voltage

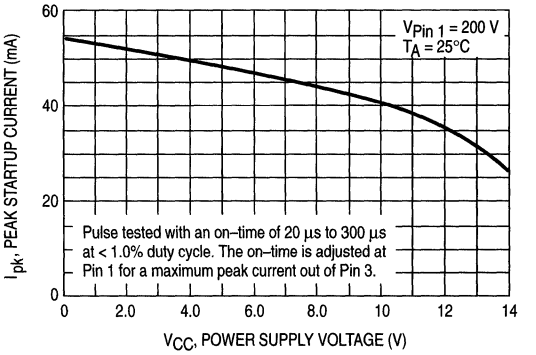


Figure 11. Power Switch Drain–Source On–Resistance versus Temperature

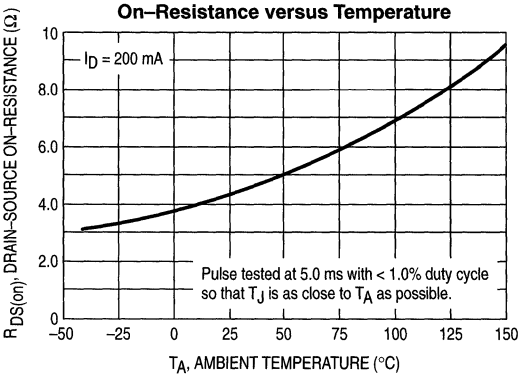


Figure 12. Power Switch Drain–Source Capacitance versus Voltage

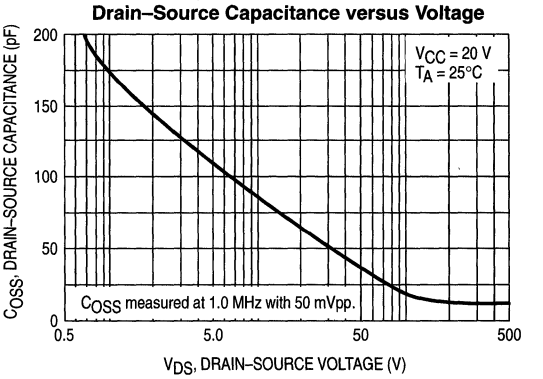


Figure 13. Supply Current versus Supply Voltage

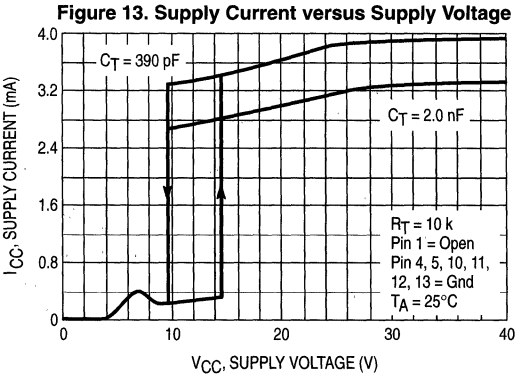


Figure 14. DW and P Suffix Transient Thermal Resistance

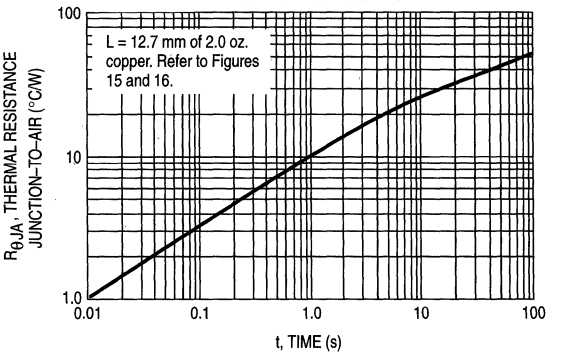


Figure 15. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

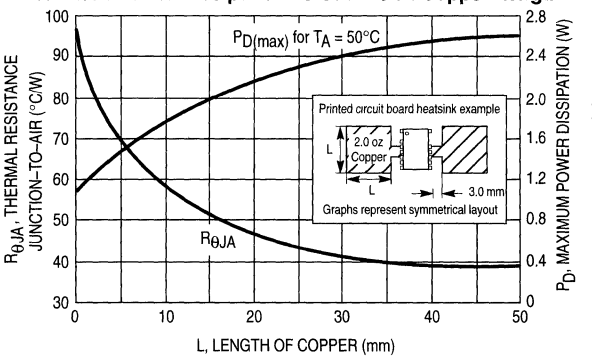
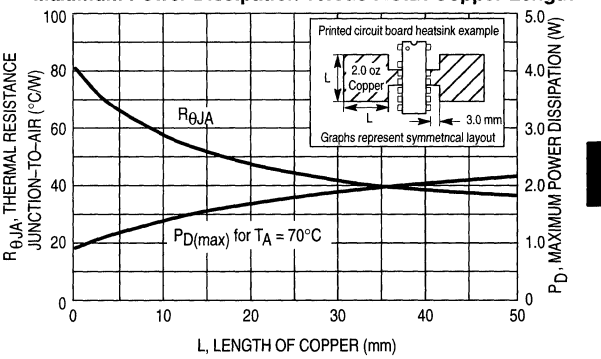


Figure 16. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



3

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Startup Input	This pin connects directly to the rectified ac line voltage source. Internally Pin 1 is tied to the drain of a high voltage startup MOSFET. During startup, the MOSFET supplies internal bias, and charges an external capacitor that connects from the V_{CC} pin to ground.
2	–	This pin has been omitted for increased spacing between the rectified AC line voltage on Pin 1 and the V_{CC} potential on Pin 3.
3	V_{CC}	This is the positive supply voltage input. During startup, power is supplied to this input from Pin 1. When V_{CC} reaches the UVLO upper threshold, the startup MOSFET turns off and power is supplied from an auxiliary transformer winding.
4, 5, 12, 13	Ground	These pins are the control circuit grounds. They are part of the IC lead frame and provide a thermal path from the die to the printed circuit board.
6	R_T	Resistor R_T connects from this pin to ground. The value selected will program the Current Limit Comparator threshold and affect the Oscillator frequency.
7	C_T	Capacitor C_T connects from this pin to ground. The value selected, in conjunction with resistor R_T, programs the Oscillator frequency.
8	Regulator Output	This 6.5 V output is available for biasing external circuitry. It requires an external bypass capacitor of at least 1.0 μF for stability.
9	Compensation	This pin is the Error Amplifier output and is made available for loop compensation. It can be used as an input to directly control the PWM Comparator.
10	Voltage Feedback Input	This is the inverting input of the Error Amplifier. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output.
11	Overvoltage Protection Input	This input provides runaway output voltage protection due to an external component or connection failure in the control loop feedback signal path. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output.
14, 15	–	These pins have been omitted for increased spacing between the high voltages present on the Power Switch Drain, and the ground potential on Pins 12 and 13.
16	Power Switch Drain	This pin is designed to directly drive the converter transformer and is capable of switching a maximum of 500 V and 2.0 A.

Figure 17. Representative Block Diagram

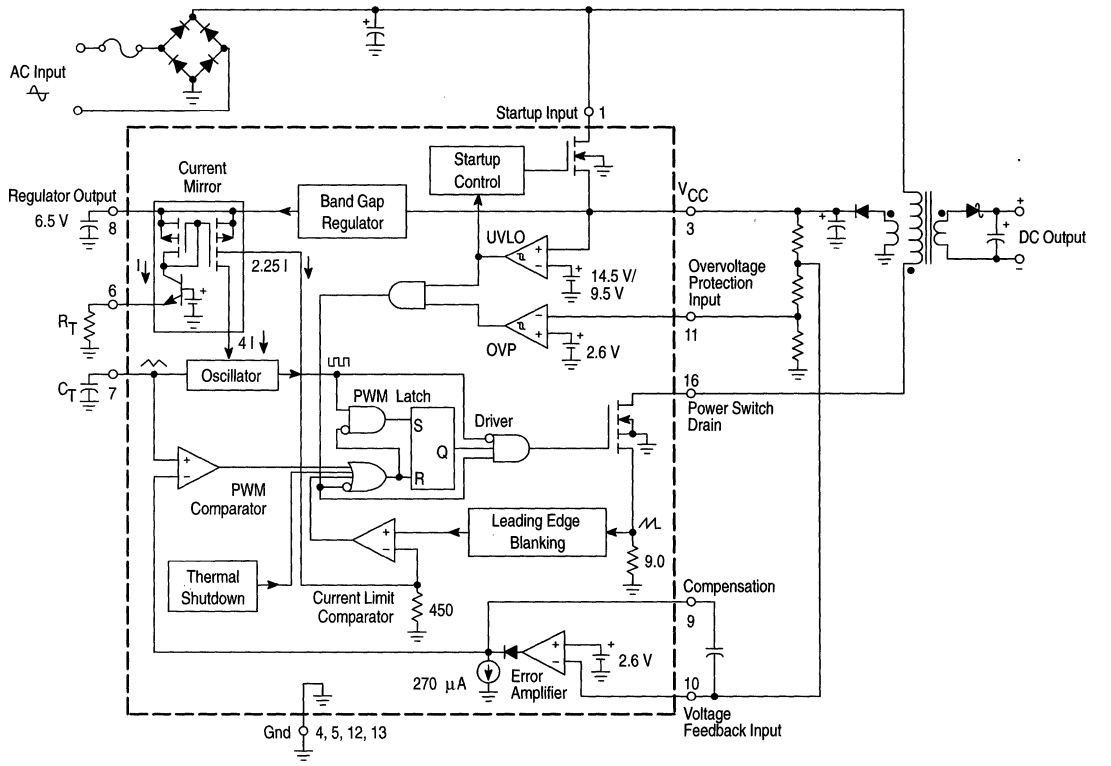
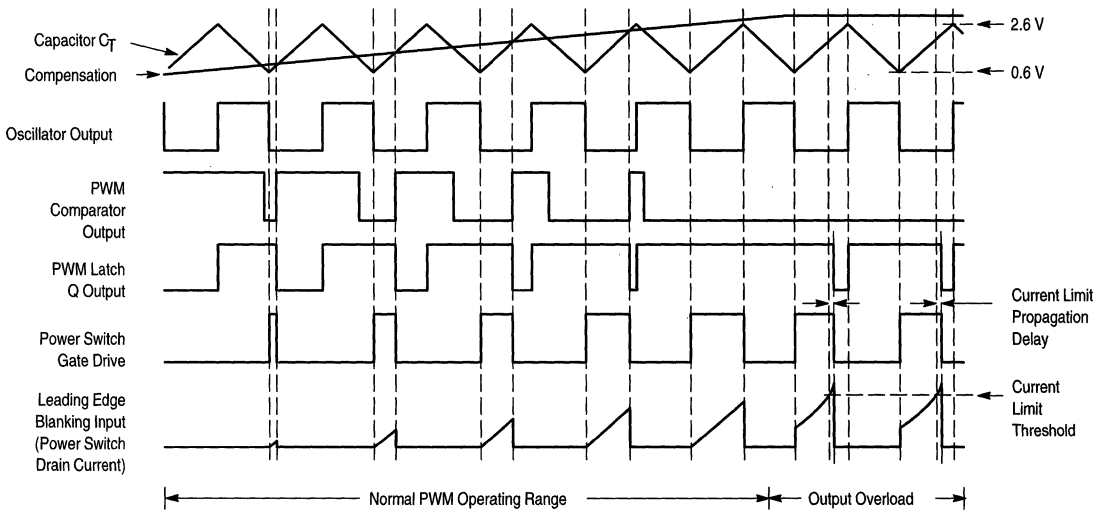


Figure 18. Timing Diagram



OPERATING DESCRIPTION

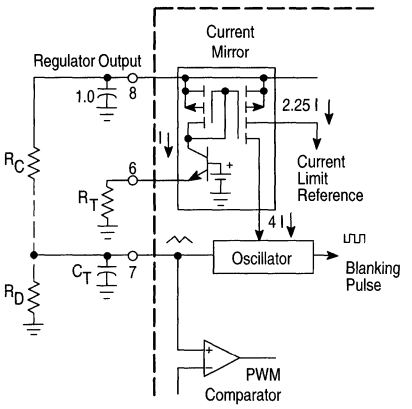
Introduction

The MC33362 represents a new higher level of integration by providing all the active high voltage power, control, and protection circuitry required for implementation of a flyback or forward converter on a single monolithic chip. This device is designed for direct operation from a rectified 120 VAC line source and requires a minimum number of external components to implement a complete converter. A description of each of the functional blocks is given below, and the representative block and timing diagrams are shown in Figures 17 and 18.

Oscillator and Current Mirror

The oscillator frequency is controlled by the values selected for the timing components R_T and C_T. Resistor R_T programs the oscillator charge/discharge current via the Current Mirror 4 I output, Figure 3. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink. This generates a symmetrical 50 percent duty cycle waveform at Pin 7, with a peak and valley threshold of 2.6 V and 0.6 V respectively. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate Driver high. This causes the Power Switch gate drive to be held in a low state, thus producing a well controlled amount of output deadtime. The amount of deadtime is relatively constant with respect to the oscillator frequency when operating below 1.0 MHz. The maximum Power Switch duty cycle at Pin 16 can be modified from the internal 50% limit by providing an additional charge or discharge current path to C_T, Figure 19. In order to increase the maximum duty cycle, a discharge current resistor R_D is connected from Pin 7 to ground. To decrease the maximum duty cycle, a charge current resistor R_C is connected from Pin 7 to the Regulator Output. Figure 4 shows an obtainable range of maximum output duty cycle versus the ratio of either R_C or R_D with respect to R_T.

Figure 19. Maximum Duty Cycle Modification



The formula for the charge/discharge current along with the oscillator frequency are given below. The frequency formula is a first order approximation and is accurate for C_T values greater than 500 pF. For smaller values of C_T, refer to Figure 1. Note that resistor R_T also programs the Current Limit Comparator threshold.

$$I_{chg/dscg} = \frac{5.4}{R_T} \qquad f \approx \frac{I_{chg/dscg}}{4C_T}$$

PWM Comparator and Latch

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the non–inverting input, while the error amplifier output is applied into the inverting input. The Oscillator applies a set pulse to the PWM Latch while C_T is discharging, and upon reaching the valley voltage, Power Switch conduction is initiated. When C_T charges to a voltage that exceeds the error amplifier output, the PWM Latch is reset, thus terminating Power Switch conduction for the duration of the oscillator ramp–up period. This PWM Comparator/Latch combination prevents multiple output pulses during a given oscillator clock cycle. The timing diagram shown in Figure 18 illustrates the Power Switch duty cycle behavior versus the Compensation voltage.

Current Limit Comparator and Power Switch

The MC33362 uses cycle–by–cycle current limiting as a means of protecting the output switch transistor from overstress. Each on–cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp–up period.

The Power Switch is constructed as a SenseFET allowing a virtually lossless method of monitoring the drain current. It consists of a total of 3770 cells, of which 50 are connected to a 9.0 Ω ground–referenced sense resistor. The Current Sense Comparator detects if the voltage across the sense resistor exceeds the reference level that is present at the inverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch. The current limit reference level is generated by the 2.25 I output of the Current Mirror. This current causes a reference voltage to appear across the 450 Ω resistor. This voltage level, as well as the Oscillator charge/discharge current are both set by resistor R_T. Therefore when selecting the values for R_T and C_T, R_T must be chosen first to set the Power Switch peak drain current, while C_T is chosen second to set the desired Oscillator frequency. A graph of the Power Switch peak drain current versus R_T is shown in Figure 2 with the related formula below.

$$I_{pk} = 12.3 \left(\frac{R_T}{1000}\right) - 1.115$$

The Power Switch is designed to directly drive the converter transformer and is capable of switching a maximum of 500 V and 2.0 A. Proper device voltage snubbing and heatsinking are required for reliable operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path. This circuit prevents a premature reset of the PWM Latch. The premature reset is generated each time the Power Switch is driven into conduction. It appears as a narrow voltage spike across the current sense resistor, and is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior in that it masks the current signal until the Power Switch turn–on transition is completed. The current limit propagation delay time is typically 233 ns. This time is measured from when an overcurrent appears at the Power Switch drain, to the beginning of turn–off.

Error Amplifier

An fully compensated Error Amplifier with access to the inverting input and output is provided for primary side voltage sensing, Figure 17. It features a typical dc voltage gain of 82 dB, and a unity gain bandwidth of 1.0 MHz with 78 degrees of phase margin, Figure 5. The noninverting input is internally biased at 2.6 V ±3.1% and is not pinned out. The Error Amplifier output is pinned out for external loop compensation and as a means for directly driving the PWM Comparator. The output was designed with a limited sink current capability of 270 μA, allowing it to be easily overridden with a pull–up resistor. This is desirable in applications that require secondary side voltage sensing, Figure 20. In this application, the Voltage Feedback Input is connected to the Regulator Output. This disables the Error Amplifier by placing its output into the sink state, allowing the optocoupler transistor to directly control the PWM Comparator.

Overvoltage Protection

An Overvoltage Protection Comparator is included to eliminate the possibility of runaway output voltage. This condition can occur if the control loop feedback signal path is broken due to an external component or connection failure. The comparator is normally used to monitor the primary side V_{CC} voltage. When the 2.6 V threshold is exceeded, it will immediately turn off the Power Switch, and protect the load from a severe overvoltage condition. This input can also be driven from external circuitry to inhibit converter operation.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. The UVLO comparator monitors the V_{CC} voltage at Pin 3 and when it exceeds 14.5 V, the reset signal is removed from the PWM Latch allowing operation of the Power Switch. To prevent erratic switching as the threshold is crossed, 5.0 V of hysteresis is provided.

Startup Control

An internal Startup Control circuit with a high voltage enhancement mode MOSFET is included within the MC33362. This circuitry allows for increased converter efficiency by eliminating the external startup resistor, and its associated power dissipation, commonly used in most off–line converters that utilize a UC3842 type of controller. Rectified ac line voltage is applied to the Startup Input, Pin 1. This causes the MOSFET to enhance and supply internal bias as well as charge current to the V_{CC} bypass capacitor that connects from Pin 3 to ground. When V_{CC} reaches the UVLO upper threshold of 14.5 V, the IC commences operation and the startup MOSFET is turned off. Operating bias is now derived from the auxiliary transformer winding, and all of the device power is efficiently converted down from the rectified ac line.

The startup MOSFET will provide an initial peak current of 55 mA, Figure 10, which decreases rapidly as V_{CC} and the die temperature rise. The steady state current will self limit in the range of 12 mA with V_{CC} shorted to ground. The startup MOSFET is rated at a maximum of 250 V with V_{CC} shorted to ground, and 400 V when charging a V_{CC} capacitor of 1000 μF or less.

Regulator

A low current 6.5 V regulated output is available for biasing the Error Amplifier and any additional control system circuitry. It is capable of up to 10 mA and has short–circuit protection. This output requires an external bypass capacitor of at least 1.0 μF for stability.

Thermal Shutdown and Package

Internal thermal circuitry is provided to protect the Power Switch in the event that the maximum junction temperature is exceeded. When activated, typically at 155°C, the Latch is forced into a 'reset' state, disabling the Power Switch. The Latch is allowed to 'set' when the Power Switch temperature falls below 145°C. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC33362 is contained in a heatsinkable plastic dual–in–line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 15 and 16 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. The examples are for a symmetrical layout on a single–sided board with two ounce per square foot of copper. Figure 22 shows a practical example of a printed circuit board layout that utilizes the copper foil as a heat dissipater. Note that a jumper was added to the layout from Pins 8 to 10 in order to enhance the copper area near the device for improved thermal conductivity. The application circuit requires two ounce copper foil in order to obtain 20 watts of continuous output power at room temperature.

Figure 20. 20 W Off–Line Converter

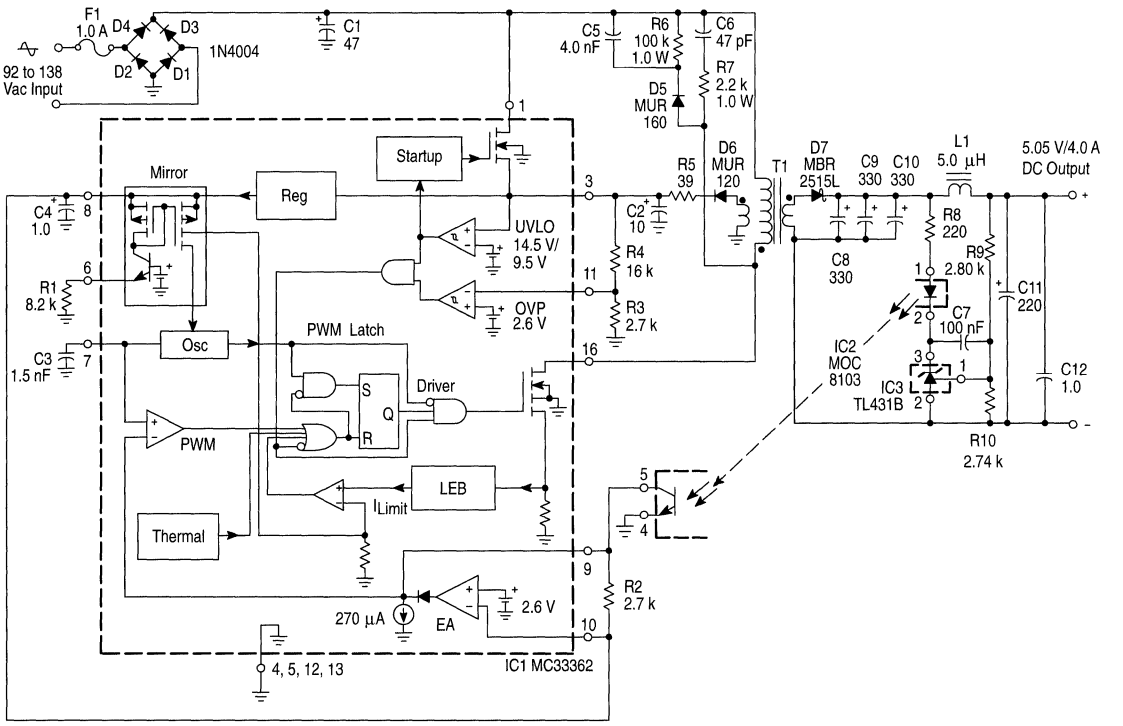


Figure 21. Converter Test Data

Test	Conditions	Results
Line Regulation	V_{in} = 92 Vac to 138 Vac, I_O 4.0 A	Δ = 1.0 mV
Load Regulation	V_{in} = 115 Vac, I_O = 1.0 A to 4.0 A	Δ = 9.0 mV
Output Ripple	V_{in} = 115 Vac, I_O = 4.0 A	Triangular = 10 mVpp Spike = 60 mVpp
Efficiency	V_{in} = 115 Vac, I_O = 4.0 A	78.4%

This data was taken with the components listed below mounted on the printed circuit board shown in Figure 22.

For high efficiency and small circuit board size, the Sanyo Os–Con capacitors are recommended for C8, C9, C10 and C11.

C8, C9, C10 = Sanyo Os–Con #6SA330M, 330 µF 6.3 V.

C11 = Sanyo Os–Con #10SA220M, 220 µF 10 V.

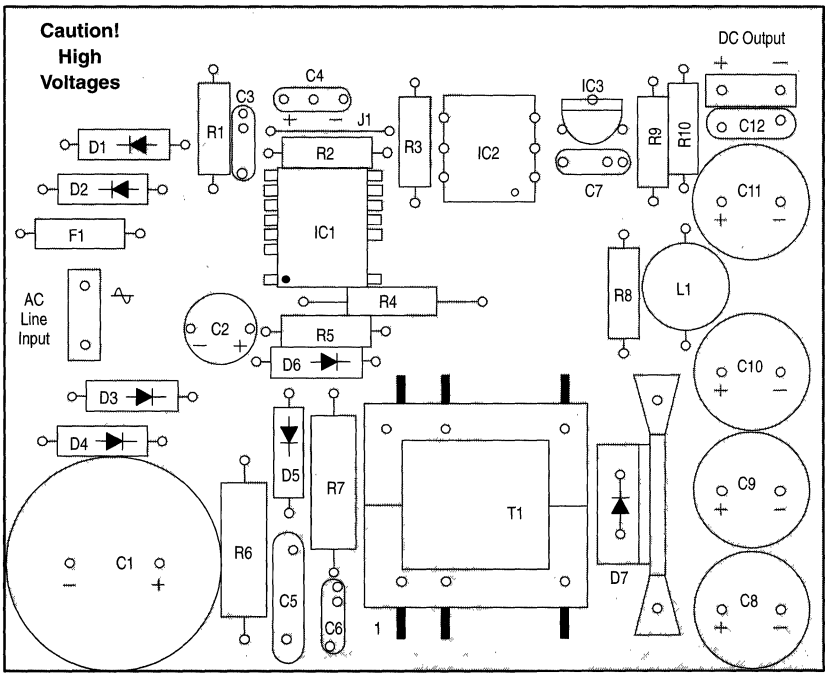
D7 = MBR2515L mounted on Aavid #592502B03400 heatsink.

L1 = Coilcraft S5088–A, 5.0 µH, 0.11 Ω.

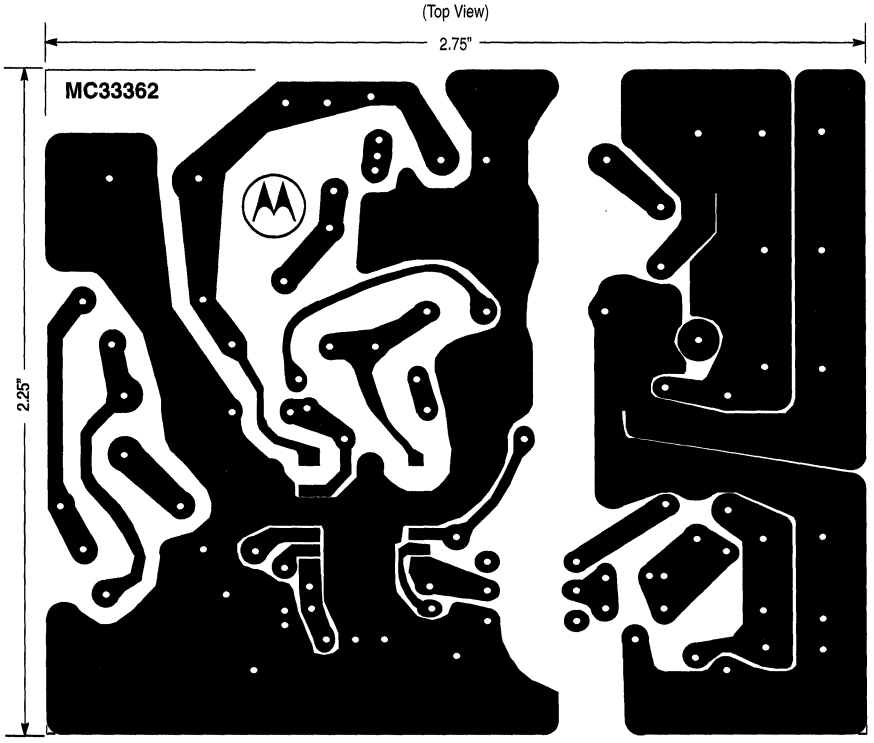
T1 = Coilcraft S5069–A

Primary: 58 turns of # 26 AWG, Pin 1 = start, Pin 8 = finish.
Two layers 0.002″ Mylar tape.
Secondary: 4 turns of # 18 AWG, 2 strands bifiliar wound, Pin 5 = start, Pin 4 = finish.
Two layers 0.002″ Mylar tape.
Auxiliary: 10 turns of # 26 AWG wound in center of bobbin, Pin 2 = start, Pin 7 = finish.
Two layers 0.002″ Mylar tape.
Gap: 0.014″ total for a primary inductance (L_P) of 330 µH.
Core and Bobbin: Coilcraft PT1950, E187, 3F3 material.

Figure 22. Printed Circuit Board and Component Layout
(Circuit of Figure 20)



(Top View)



(Bottom View)

MOTOROLA

MC33363

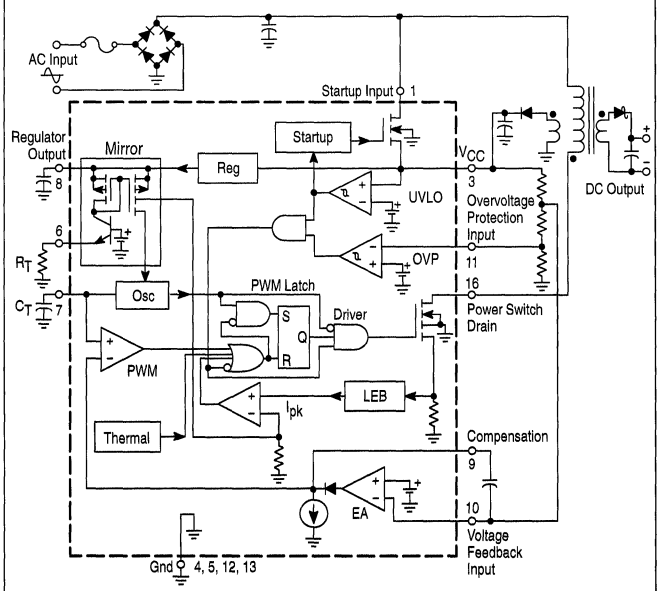
Advance Information

High Voltage Switching Regulator

The MC33363 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on–chip 700 V/1.0 A SenseFET power switch, 450 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16–lead dual–in–line and wide body surface mount packages.

- On–Chip 700 V, 1.0 A SenseFET Power Switch
- Rectified 240 Vac Line Source Operation
- On–Chip 450 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown

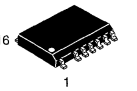
Simplified Application



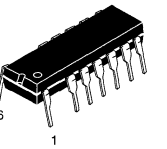
This device contains 221 active transistors.

HIGH VOLTAGE OFF–LINE SWITCHING REGULATOR

SEMICONDUCTOR TECHNICAL DATA

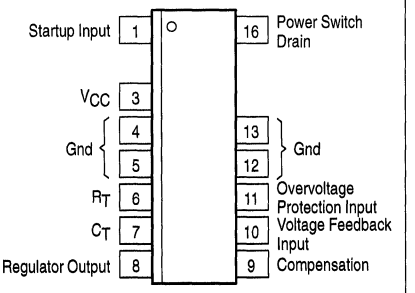


DW SUFFIX
PLASTIC PACKAGE
CASE 751N
(SOP–16L)



P SUFFIX
PLASTIC PACKAGE
CASE 648E
(DIP–16)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33363DW	T_J = –25° to +125°C	SOP–16L
MC33363P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Switch (Pin 16) Drain Voltage Drain Current	 V_{DS} I_{DS}	 700 1.0	 V A
Startup Input Voltage (Pin 1, Note 1) Pin 3 = Gnd Pin 3 ≤ 1000 μF to ground	V_{in}	 400 500	V
Power Supply Voltage (Pin 3)	V_{CC}	40	V
Input Voltage Range Voltage Feedback Input (Pin 10) Compensation (Pin 9) Overvoltage Protection Input (Pin 11) R_T (Pin 6) C_T (Pin 7)	V_{IR}	−1.0 to V_{reg}	V
Thermal Characteristics P Suffix, Dual–In–Line Case 648E Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13) DW Suffix, Surface Mount Case 751N Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13) Refer to Figures 15 and 16 for additional thermal information.	 $R_{\theta JA}$ $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JC}$	 80 15 95 15	°C/W
Operating Junction Temperature	T_J	− 25 to +150	°C
Storage Temperature	T_{stg}	− 55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 20 V, R_T = 10 k, C_T = 390 pF, $C_{Pin\ 8}$ = 1.0 μF, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REGULATOR (Pin 8)					
Output Voltage (I_O = 0 mA, T_J = 25°C)	V_{reg}	5.5	6.5	7.5	V
Line Regulation (V_{CC} = 20 V to 40 V)	Reg_{line}	–	30	500	mV
Load Regulation (I_O = 0 mA to 10 mA)	Reg_{load}	–	44	200	mV
Total Output Variation over Line, Load, and Temperature	V_{reg}	5.3	–	8.0	V
OSCILLATOR (Pin 7)					
Frequency C_T = 390 pF T_J = 25°C (V_{CC} = 20 V) T_J = T_{low} to T_{high} (V_{CC} = 20 V to 40 V) C_T = 2.0 nF T_J = 25°C (V_{CC} = 20 V) T_J = T_{low} to T_{high} (V_{CC} = 20 V to 40 V)	f_{OSC}	 260 255 60 59	 285 – 67.5 –	 310 315 75 76	kHz
Frequency Change with Voltage (V_{CC} = 20 V to 40 V)	$\Delta f_{OSC}/\Delta V$	–	0.1	2.0	kHz
ERROR AMPLIFIER (Pins 9, 10)					
Voltage Feedback Input Threshold	V_{FB}	2.52	2.6	2.68	V
Line Regulation (V_{CC} = 20 V to 40 V, T_J = 25°C)	Reg_{line}	–	0.6	5.0	mV
Input Bias Current (V_{FB} = 2.6 V)	I_{IB}	–	20	500	nA
Open Loop Voltage Gain (T_J = 25°C)	A_{VOL}	–	82	–	dB
Gain Bandwidth Product (f = 100 kHz, T_J = 25°C)	GBW	–	1.0	–	MHz

NOTES: 1. Maximum power dissipation limits must be observed.
2. Tested junction temperature range for the MC33363:
T_{low} = −25°C T_{high} = +125°C

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 20 V, R_T = 10 k, C_T = 390 pF, $C_{Pin\ 8}$ = 1.0 µF, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER (Pins 9, 10)					
Output Voltage Swing High State (I_{Source} = 100 µA, V_{FB} < 2.0 V) Low State (I_{Sink} = 100 µA, V_{FB} > 3.0 V)	 V_{OH} V_{OL}	 4.0 –	 5.3 0.2	 – 0.35	V
OVERVOLTAGE DETECTION (Pin 11)					
Input Threshold Voltage	V_{th}	2.47	2.6	2.73	V
Input Bias Current (V_{in} = 2.6 V)	I_{IB}	–	100	500	nA
PWM COMPARATOR (Pins 7, 9)					
Duty Cycle Maximum (V_{FB} = 0 V) Minimum (V_{FB} = 2.7 V)	 $DC_{(max)}$ $DC_{(min)}$	 48 –	 50 0	 52 0	%
POWER SWITCH (Pin 16)					
Drain–Source On–State Resistance (I_D = 200 mA) T_J = 25°C T_J = T_{low} to T_{high}	$R_{DS(on)}$	 – –	 14 –	 17 32	Ω
Drain–Source Off–State Leakage Current (V_{DS} = 700 V)	$I_{D(off)}$	–	0.2	50	µA
Rise Time	t_r	–	50	–	ns
Fall Time	t_f	–	50	–	ns
OVERCURRENT COMPARATOR (Pin 16)					
Current Limit Threshold (R_T = 10 k)	I_{lim}	0.5	0.72	0.9	A
STARTUP CONTROL (Pin 1)					
Peak Startup Current (V_{in} = 400 V) V_{CC} = 0 V V_{CC} = ($V_{th(on)}$ – 0.2 V)	I_{start}	 – –	 20 6.0	 – –	mA
Off–State Leakage Current (V_{in} = 50 V, V_{CC} = 20 V)	$I_{D(off)}$	–	40	200	µA
UNDERVOLTAGE LOCKOUT (Pin 3)					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	11	15.2	18	V
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$	7.5	9.5	11.5	V
TOTAL DEVICE (Pin 3)					
Power Supply Current Startup (V_{CC} = 10 V, Pin 1 Open) Operating	I_{CC}	 – –	 0.25 3.2	 0.5 5.0	mA

Figure 1. Oscillator Frequency versus Timing Resistor

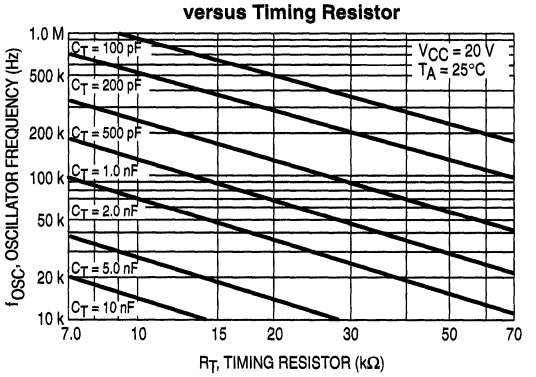


Figure 2. Power Switch Peak Drain Current versus Timing Resistor

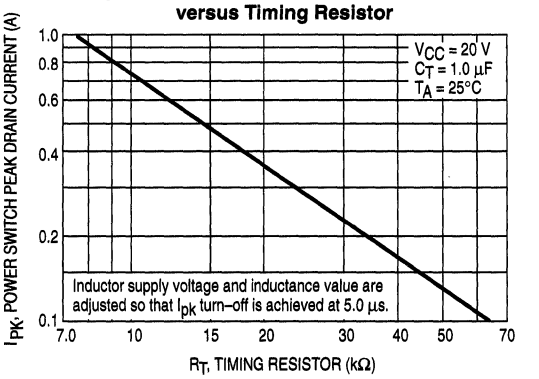


Figure 3. Oscillator Charge/Discharge Current versus Timing Resistor

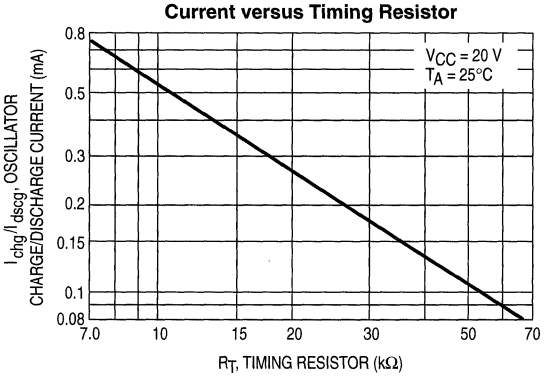


Figure 4. Maximum Output Duty Cycle versus Timing Resistor Ratio

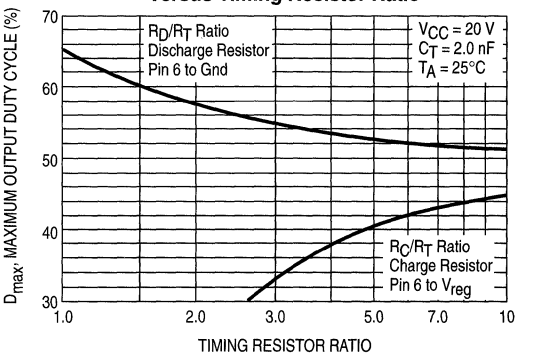


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

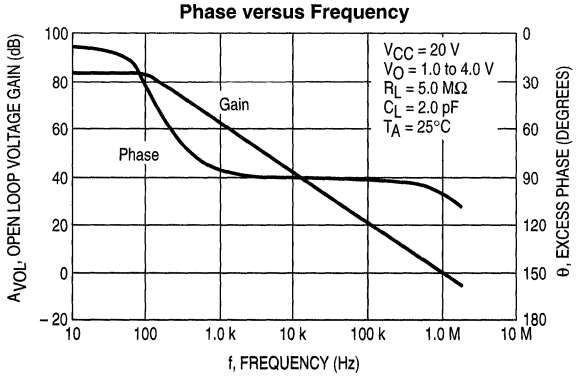


Figure 6. Error Amp Output Saturation Voltage versus Load Current

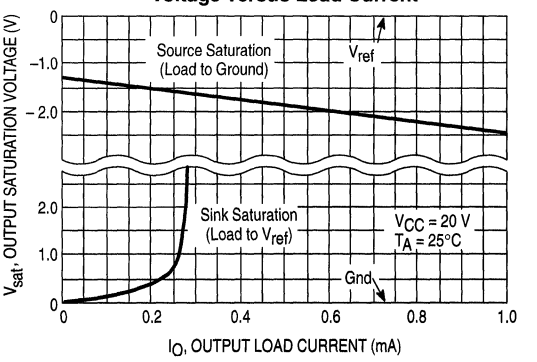


Figure 7. Error Amplifier Small Signal Transient Response

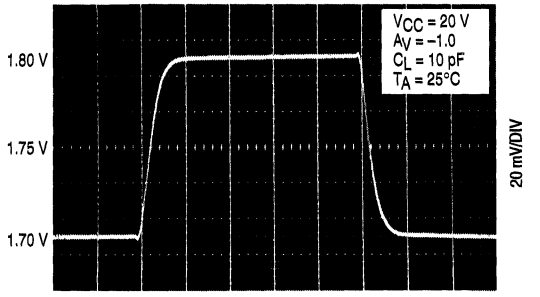


Figure 8. Error Amplifier Large Signal Transient Response

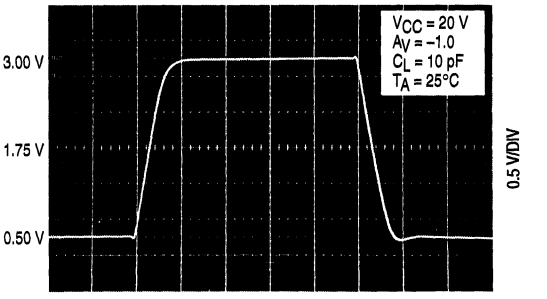


Figure 9. Regulator Output Voltage Change versus Source Current

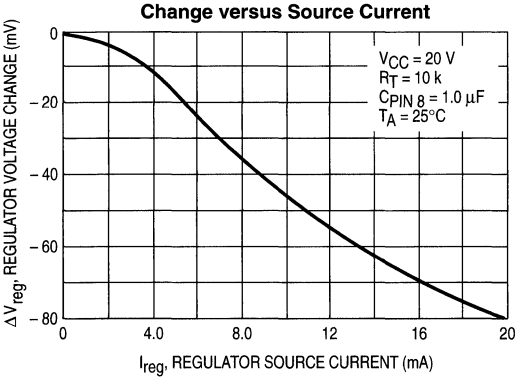


Figure 10. Peak Startup Current versus Power Supply Voltage

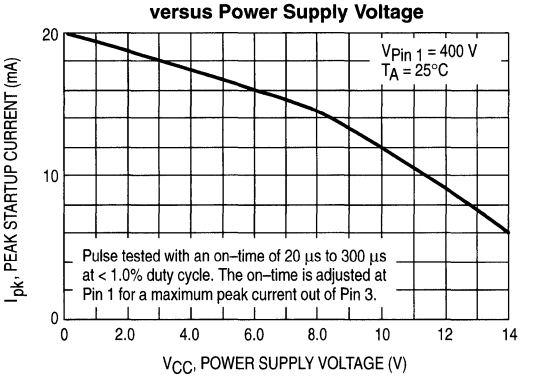


Figure 11. Power Switch Drain–Source On–Resistance versus Temperature

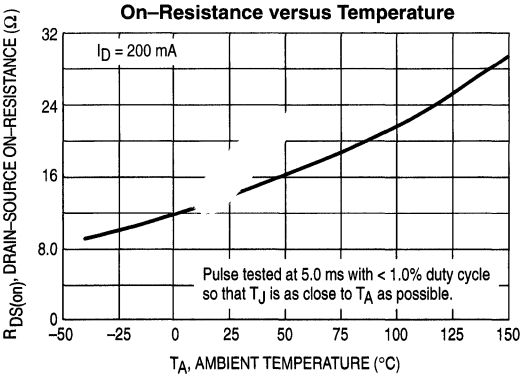


Figure 12. Power Switch Drain–Source Capacitance versus Voltage

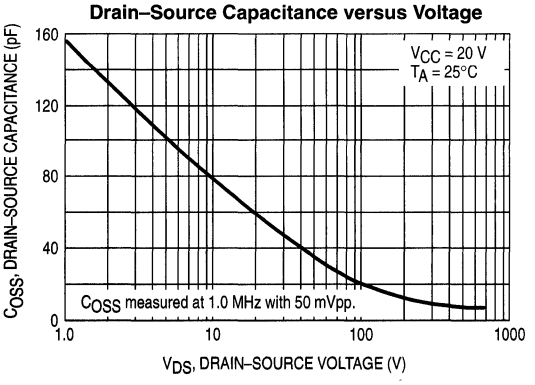


Figure 13. Supply Current versus Supply Voltage

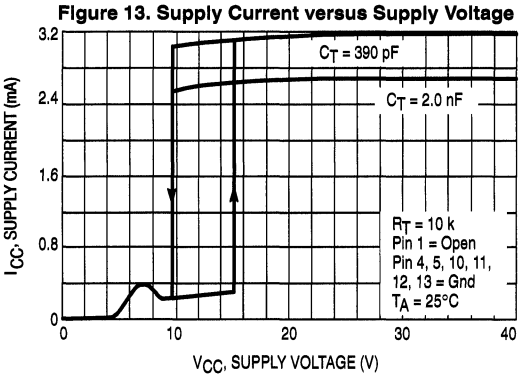


Figure 14. DW and P Suffix Transient Thermal Resistance

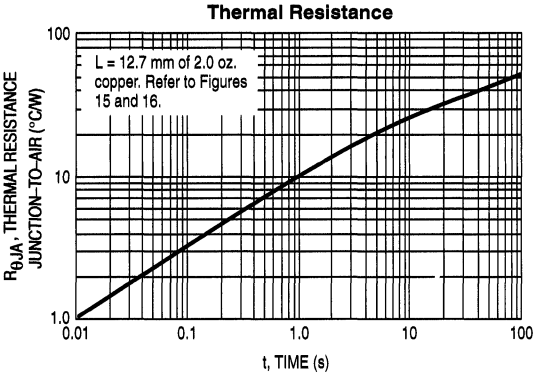


Figure 15. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

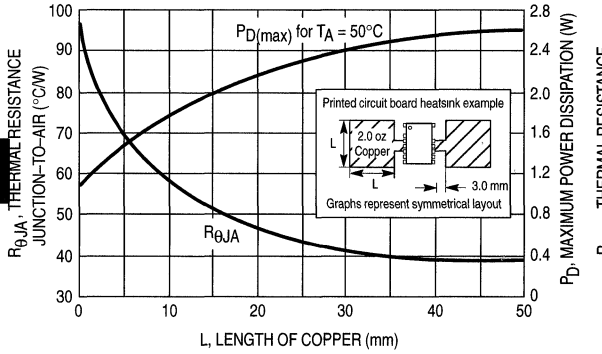
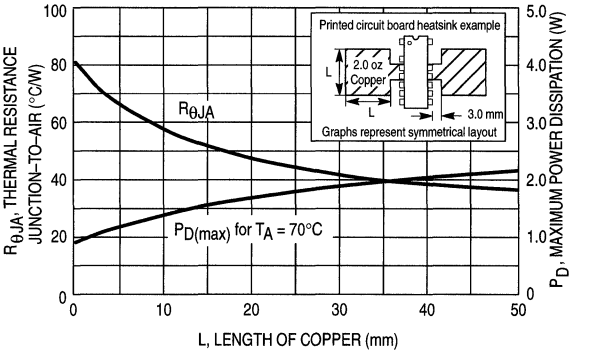


Figure 16. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Startup Input	This pin connects directly to the rectified ac line voltage source. Internally Pin 1 is tied to the drain of a high voltage startup MOSFET. During startup, the MOSFET supplies internal bias, and charges an external capacitor that connects from the V_{CC} pin to ground.
2	–	This pin has been omitted for increased spacing between the rectified ac line voltage on Pin 1 and the V_{CC} potential on Pin 3.
3	V_{CC}	This is the positive supply voltage input. During startup, power is supplied to this input from Pin 1. When V_{CC} reaches the UVLO upper threshold, the startup MOSFET turns off and power is supplied from an auxiliary transformer winding.
4, 5, 12, 13	Ground	These pins are the control circuit grounds. They are part of the IC lead frame and provide a thermal path from the die to the printed circuit board.
6	R_T	Resistor R_T connects from this pin to ground. The value selected will program the Current Limit Comparator threshold and affect the Oscillator frequency.
7	C_T	Capacitor C_T connects from this pin to ground. The value selected, in conjunction with resistor R_T, programs the Oscillator frequency.
8	Regulator Output	This 6.5 V output is available for biasing external circuitry. It requires an external bypass capacitor of at least 1.0 μF for stability.
9	Compensation	This pin is the Error Amplifier output and is made available for loop compensation. It can be used as an input to directly control the PWM Comparator.
10	Voltage Feedback Input	This is the inverting input of the Error Amplifier. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output.
11	Overvoltage Protection Input	This input provides runaway output voltage protection due to an external component or connection failure in the control loop feedback signal path. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output.
14, 15	–	These pins have been omitted for increased spacing between the high voltages present on the Power Switch Drain, and the ground potential on Pins 12 and 13.
16	Power Switch Drain	This pin is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A.

Figure 17. Representative Block Diagram

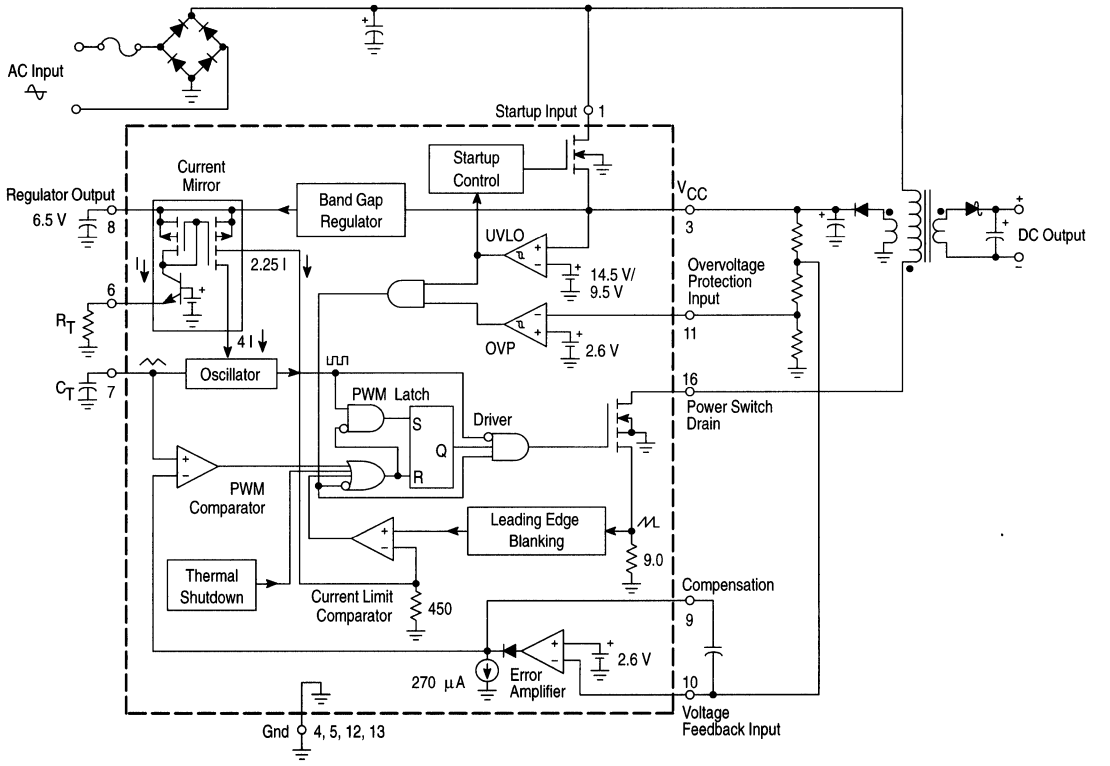
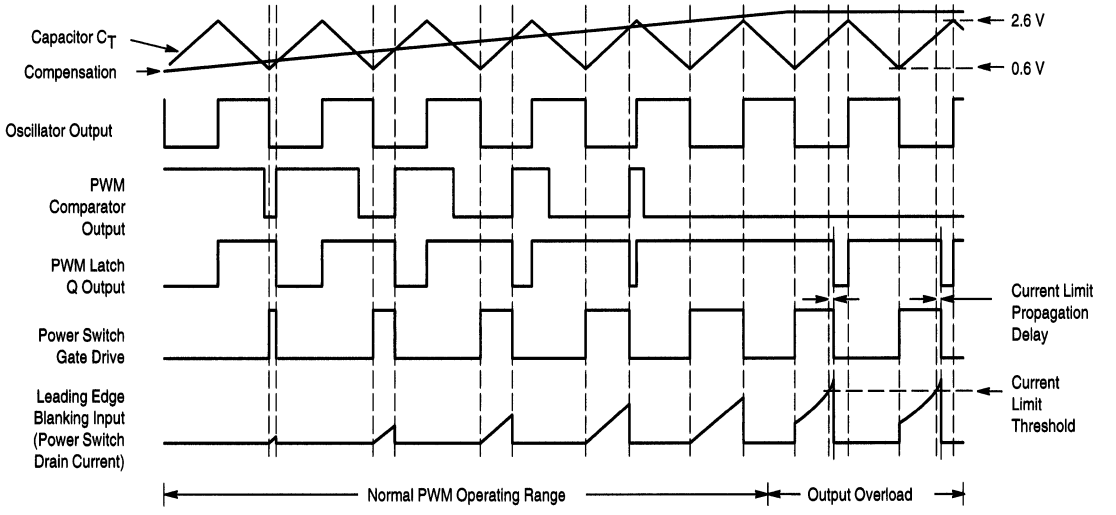


Figure 18. Timing Diagram



OPERATING DESCRIPTION

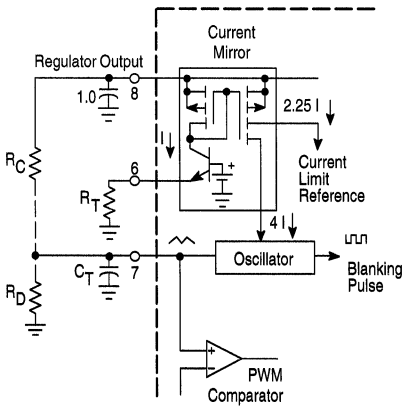
Introduction

The MC33363 represents a new higher level of integration by providing all the active high voltage power, control, and protection circuitry required for implementation of a flyback or forward converter on a single monolithic chip. This device is designed for direct operation from a rectified 240 Vac line source and requires a minimum number of external components to implement a complete converter. A description of each of the functional blocks is given below, and the representative block and timing diagrams are shown in Figures 17 and 18.

Oscillator and Current Mirror

The oscillator frequency is controlled by the values selected for the timing components R_T and C_T. Resistor R_T programs the oscillator charge/discharge current via the Current Mirror 4 I output, Figure 3. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink. This generates a symmetrical 50 percent duty cycle waveform at Pin 7, with a peak and valley threshold of 2.6 V and 0.6 V respectively. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate Driver high. This causes the Power Switch gate drive to be held in a low state, thus producing a well controlled amount of output deadtime. The amount of deadtime is relatively constant with respect to the oscillator frequency when operating below 1.0 MHz. The maximum Power Switch duty cycle at Pin 16 can be modified from the internal 50% limit by providing an additional charge or discharge current path to C_T, Figure 19. In order to increase the maximum duty cycle, a discharge current resistor R_D is connected from Pin 7 to ground. To decrease the maximum duty cycle, a charge current resistor R_C is connected from Pin 7 to the Regulator Output. Figure 4 shows an obtainable range of maximum output duty cycle versus the ratio of either R_C or R_D with respect to R_T.

Figure 19. Maximum Duty Cycle Modification



The formula for the charge/discharge current along with the oscillator frequency are given below. The frequency formula is a first order approximation and is accurate for C_T values greater than 500 pF. For smaller values of C_T, refer to Figure 1. Note that resistor R_T also programs the Current Limit Comparator threshold.

$$I_{chg/dscg} = \frac{5.4}{R_T} \qquad f \approx \frac{I_{chg/dscg}}{4C_T}$$

PWM Comparator and Latch

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the non–inverting input, while the error amplifier output is applied into the inverting input. The Oscillator applies a set pulse to the PWM Latch while C_T is discharging, and upon reaching the valley voltage, Power Switch conduction is initiated. When C_T charges to a voltage that exceeds the error amplifier output, the PWM Latch is reset, thus terminating Power Switch conduction for the duration of the oscillator ramp–up period. This PWM Comparator/Latch combination prevents multiple output pulses during a given oscillator clock cycle. The timing diagram shown in Figure 18 illustrates the Power Switch duty cycle behavior versus the Compensation voltage.

Current Limit Comparator and Power Switch

The MC33363 uses cycle–by–cycle current limiting as a means of protecting the output switch transistor from overstress. Each on–cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp–up period.

The Power Switch is constructed as a SenseFET allowing a virtually lossless method of monitoring the drain current. It consists of a total of 1780 cells, of which 46 are connected to a 9.0 Ω ground–referenced sense resistor. The Current Sense Comparator detects if the voltage across the sense resistor exceeds the reference level that is present at the inverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch. The current limit reference level is generated by the 2.25 I output of the Current Mirror. This current causes a reference voltage to appear across the 450 Ω resistor. This voltage level, as well as the Oscillator charge/discharge current are both set by resistor R_T. Therefore when selecting the values for R_T and C_T, R_T must be chosen first to set the Power Switch peak drain current, while C_T is chosen second to set the desired Oscillator frequency. A graph of the Power Switch peak drain current versus R_T is shown in Figure 2 with the related formula below.

$$I_{pk} = 8.8 \left(\frac{R_T}{1000} \right) - 1.077$$

The Power Switch is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A. Proper device voltage snubbing and heatsinking are required for reliable operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path. This circuit prevents a premature reset of the PWM Latch. The premature reset is generated each time the Power Switch is driven into conduction. It appears as a narrow voltage spike across the current sense resistor, and is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior in that it masks the current signal until the Power Switch turn–on transition is completed. The current limit propagation delay time is typically 233 ns. This time is measured from when an overcurrent appears at the Power Switch drain, to the beginning of turn–off.

Error Amplifier

An fully compensated Error Amplifier with access to the inverting input and output is provided for primary side voltage sensing, Figure 17. It features a typical dc voltage gain of 82 dB, and a unity gain bandwidth of 1.0 MHz with 78 degrees of phase margin, Figure 5. The noninverting input is internally biased at 2.6 V ±3.1% and is not pinned out. The Error Amplifier output is pinned out for external loop compensation and as a means for directly driving the PWM Comparator. The output was designed with a limited sink current capability of 270 μA, allowing it to be easily overridden with a pull–up resistor. This is desirable in applications that require secondary side voltage sensing, Figure 20. In this application, the Voltage Feedback Input is connected to the Regulator Output. This disables the Error Amplifier by placing its output into the sink state, allowing the optocoupler transistor to directly control the PWM Comparator.

Overvoltage Protection

An Overvoltage Protection Comparator is included to eliminate the possibility of runaway output voltage. This condition can occur if the control loop feedback signal path is broken due to an external component or connection failure. The comparator is normally used to monitor the primary side V_{CC} voltage. When the 2.6 V threshold is exceeded, it will immediately turn off the Power Switch, and protect the load from a severe overvoltage condition. This input can also be driven from external circuitry to inhibit converter operation.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. The UVLO comparator monitors the V_{CC} voltage at Pin 3 and when it exceeds 14.5 V, the reset signal is removed from the PWM Latch allowing operation of the Power Switch. To prevent erratic switching as the threshold is crossed, 5.0 V of hysteresis is provided.

Startup Control

An internal Startup Control circuit with a high voltage enhancement mode MOSFET is included within the MC33363. This circuitry allows for increased converter efficiency by eliminating the external startup resistor, and its associated power dissipation, commonly used in most off–line converters that utilize a UC3842 type of controller. Rectified ac line voltage is applied to the Startup Input, Pin 1. This causes the MOSFET to enhance and supply internal bias as well as charge current to the V_{CC} bypass capacitor that connects from Pin 3 to ground. When V_{CC} reaches the UVLO upper threshold of 15.2 V, the IC commences operation and the startup MOSFET is turned off. Operating bias is now derived from the auxiliary transformer winding, and all of the device power is efficiently converted down from the rectified ac line.

The startup MOSFET will provide an initial peak current of 20 mA, Figure 10, which decreases rapidly as V_{CC} and the die temperature rise. The steady state current will self limit in the range of 8.0 mA with V_{CC} shorted to ground. The startup MOSFET is rated at a maximum of 400 V with V_{CC} shorted to ground, and 500 V when charging a V_{CC} capacitor of 1000 μF or less.

Regulator

A low current 6.5 V regulated output is available for biasing the Error Amplifier and any additional control system circuitry. It is capable of up to 10 mA and has short–circuit protection. This output requires an external bypass capacitor of at least 1.0 μF for stability.

Thermal Shutdown and Package

Internal thermal circuitry is provided to protect the Power Switch in the event that the maximum junction temperature is exceeded. When activated, typically at 155°C, the Latch is forced into a 'reset' state, disabling the Power Switch. The Latch is allowed to 'set' when the Power Switch temperature falls below 145°C. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC33363 is contained in a heatsinkable plastic dual–in–line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 15 and 16 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. The examples are for a symmetrical layout on a single–sided board with two ounce per square foot of copper. Figure 22 shows a practical example of a printed circuit board layout that utilizes the copper foil as a heat dissipater. Note that a jumper was added to the layout from Pins 8 to 10 in order to enhance the copper area near the device for improved thermal conductivity. The application circuit requires two ounce copper foil in order to obtain 8.0 watts of continuous output power at room temperature.

Figure 20. 8.0 W Off–Line Converter

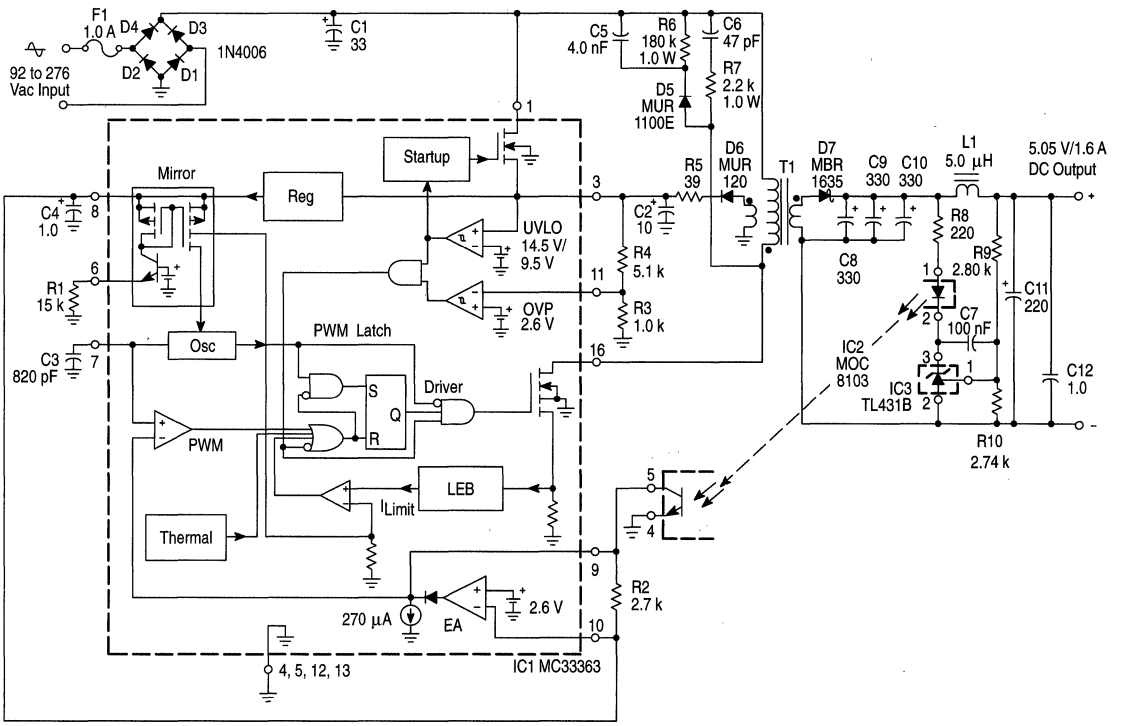


Figure 21. Converter Test Data

Test	Conditions	Results
Line Regulation	V_{in} = 92 Vac to 276 Vac, I_O 1.6 A	Δ = 1.0 mV
Load Regulation	V_{in} = 115 Vac, I_O = 0.4 A to 1.6 A	Δ = 4.0 mV
	V_{in} = 230 Vac, I_O = 0.4 A to 1.6 A	Δ = 4.0 mV
Output Ripple	V_{in} = 115 Vac, I_O = 1.6 A	Triangular = 2.0 mVpp, Spike = 12 mVpp
	V_{in} = 230 Vac, I_O = 1.6 A	Triangular = 2.0 mVpp, Spike = 12 mVpp
Efficiency	V_{in} = 115 Vac, I_O = 1.6 A	78.6%*
	V_{in} = 230 Vac, I_O = 1.6 A	75.6%

This data was taken with the components listed below mounted on the printed circuit board shown in Figure 22.

* With MBR2535CTL, 79.8% efficiency. PCB layout modification is required to use this rectifier.

For high efficiency and small circuit board size, the Sanyo Os–Con capacitors are recommended for C8, C9, C10 and C11.

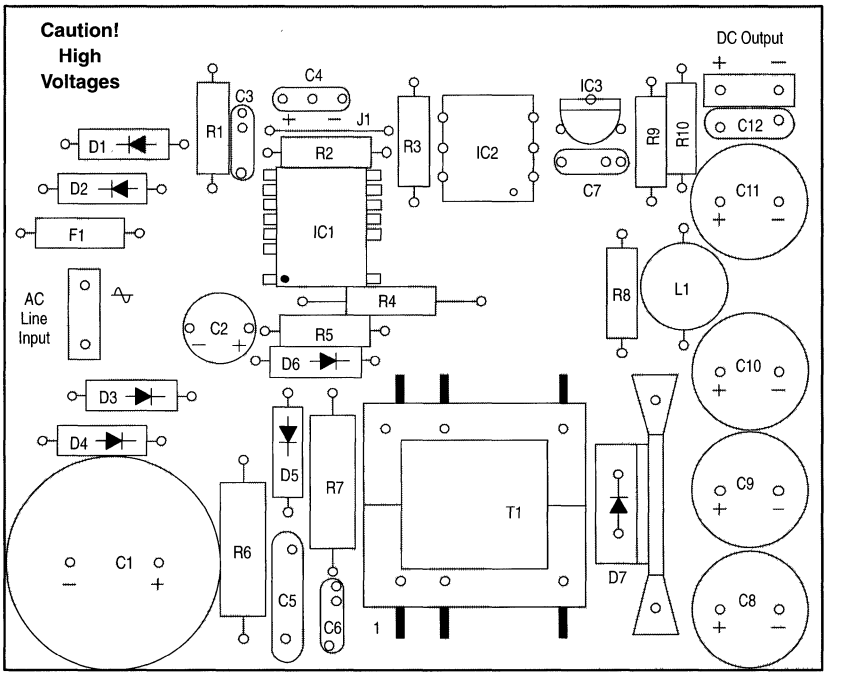
C8, C9, C10 = Sanyo Os–Con #6SA330M, 330 µF 6.3 V.

C11 = Sanyo Os–Con #10SA220M, 220 µF 10 V.

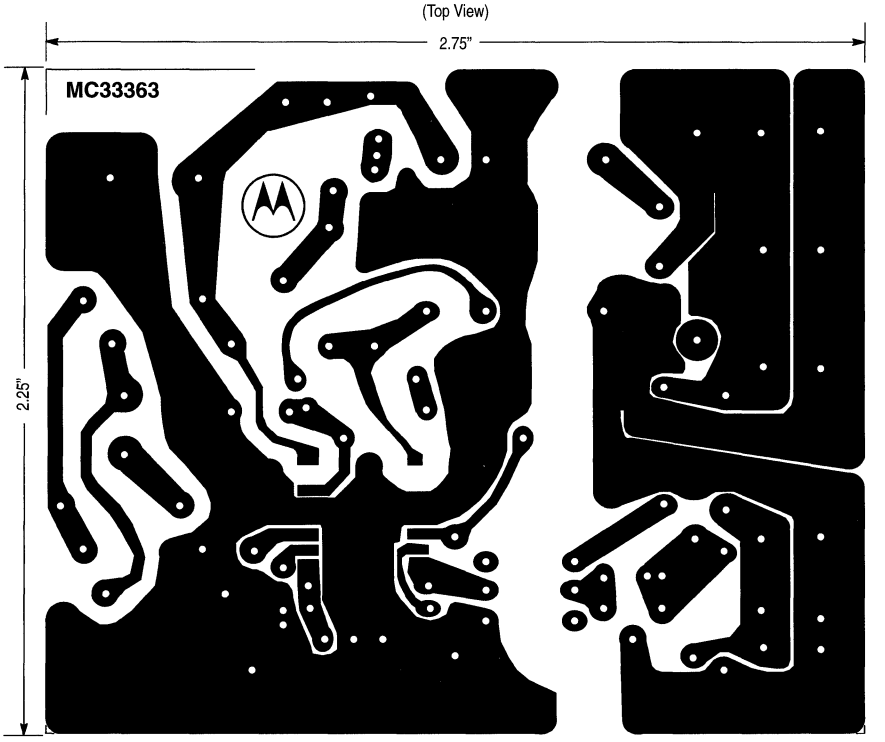
L1 = Coilcraft S5088–A, 5.0 µH, 0.11 Ω.

T1 = Coilcraft S5502–A
Primary: 77 turns of # 28 AWG, Pin 1 = start, Pin 8 = finish.
Two layers 0.002″ Mylar tape.
Secondary: 5 turns of # 22 AWG, 2 strands bifiliar wound, Pin 5 = start, Pin 4 = finish.
Two layers 0.002″ Mylar tape.
Auxiliary: 13 turns of # 28 AWG wound in center of bobbin, Pin 2 = start, Pin 7 = finish.
Two layers 0.002″ Mylar tape.
Gap: 0.006″ total for a primary inductance (L_P) of 1.0 mH.
Core and Bobbin: Coilcraft PT1950, E187, 3F3 material.

Figure 22. Printed Circuit Board and Component Layout
(Circuit of Figure 20)



(Top View)



(Bottom View)

MOTOROLA

MC33363A

3

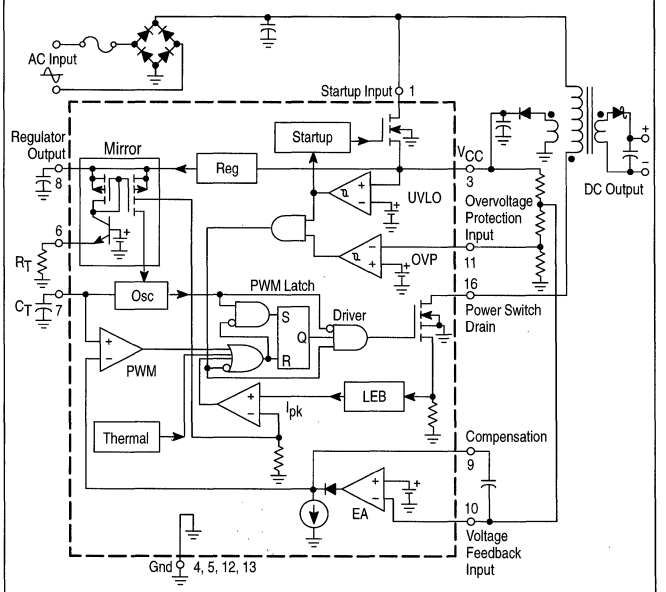
Product Preview

High Voltage Switching Regulator

The MC33363A is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on–chip 700 V/1.5 A SenseFET power switch, 450 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16–lead dual–in–line and wide body surface mount packages.

- Enhanced Power Capability Over MC33363
- On–Chip 700 V, 1.5 A SenseFET Power Switch
- Rectified 240 Vac Line Source Operation
- On–Chip 450 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown

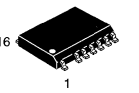
Simplified Application



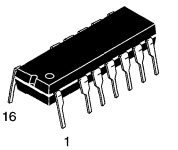
This device contains 221 active transistors.

HIGH VOLTAGE OFF–LINE SWITCHING REGULATOR

SEMICONDUCTOR TECHNICAL DATA

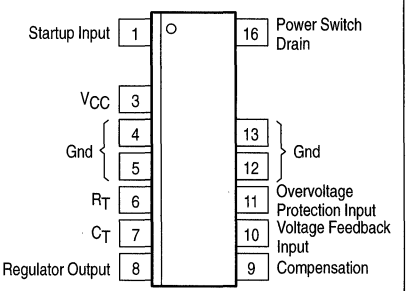


DW SUFFIX
PLASTIC PACKAGE
CASE 751N
(SOP–16L)



P SUFFIX
PLASTIC PACKAGE
CASE 648E
(DIP–16)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33363ADW	T_J = –25° to +125°C	SOP–16L
MC33363AP		DIP–16

MOTOROLA

Product Preview

Critical Conduction SMPS Controller

MC33364

CRITICAL CONDUCTION SMPS CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

3

The MC33364 series are variable frequency SMPS controllers that operate in the critical conduction mode. They are optimized for low power, high density power supplies requiring minimum board area, reduced component count, and low power dissipation. Each narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

Each MC33364 features an on–board reference, UVLO function, a watchdog timer to initiate output switching, a zero current detector to ensure critical conduction operation, a current sensing comparator, leading edge blanking, and a CMOS driver. Protection features include the ability to shut down switching, and cycle–by–cycle current limiting.

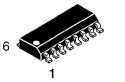
The MC33364D1 is available in a surface mount SO–8 package. It has an internal 144 kHz frequency clamp. For loads which have a low power operating condition, the frequency clamp limits the maximum operating frequency, preventing excessive switching losses and EMI radiation.

The MC33364D2 is available in the SO–8 package without an internal frequency clamp.

The MC33364D is available in the SO–16 package. It has an internal 144 kHz frequency clamp which is pinned out, so that the designer can adjust the clamp frequency by connecting appropriate values of resistance and capacitance.

- Lossless Off–Line Startup
- Leading Edge Blanking for Noise Immunity
- Watchdog Timer to Initiate Switching
- Minimum Number of Support Components
- Shutdown Capability
- Over Temperature Protection
- Optional Frequency Clamp

D1, D2 SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

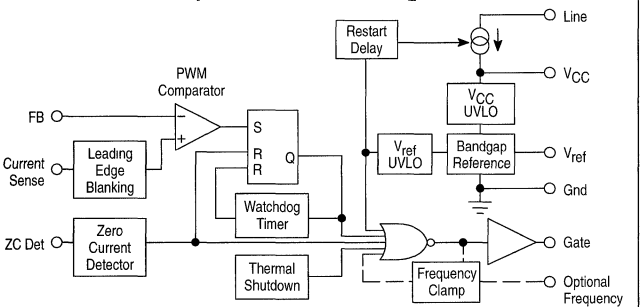


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33364D1	T_J = –25° to +125°C	SO–8
MC33364D2		SO–8
MC33364D		SO–16

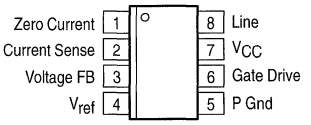
Representative Block Diagram



This device contains 173 active transistors.

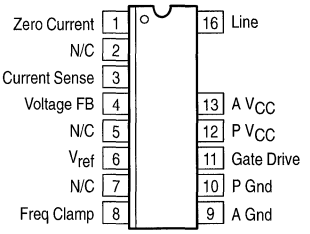
PIN CONNECTIONS

MC33364D1
MC33364D2



(Top View)

MC33364D



(Top View)

MC33368

3

Advance Information

High Voltage GreenLine™ Power Factor Controller

The MC33368 is an active power factor controller that functions as a boost preconverter in off–line power supply applications. MC33368 is optimized for low power, high density power supplies requiring a minimum board area, reduced component count and low power dissipation. The narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

The MC33368 features a watchdog timer to initiate output switching, a one quadrant multiplier to force the line current to follow the instantaneous line voltage a zero current detector to ensure critical conduction operation, a transconductance error amplifier, a current sensing comparator, a 5.0 V reference, an undervoltage lockout (UVLO) circuit which monitors the V_{CC} supply voltage and a CMOS driver for driving MOSFETs. The MC33368 also includes a programmable output switching frequency clamp. Protection features include an output overvoltage comparator to minimize overshoot, a restart delay timer and cycle–by–cycle current limiting.

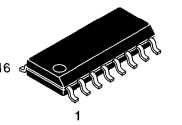
- Lossless Off–Line Startup
- Output Overvoltage Comparator
- Leading Edge Blanking (LEB) for Noise Immunity
- Watchdog Timer to Initiate Switching
- Restart Delay Timer

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33368D	T_J = –25° to +125°C	SO–16

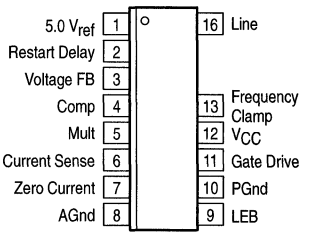
HIGH VOLTAGE GREENLINE™ POWER FACTOR CONTROLLER

SEMICONDUCTOR TECHNICAL DATA



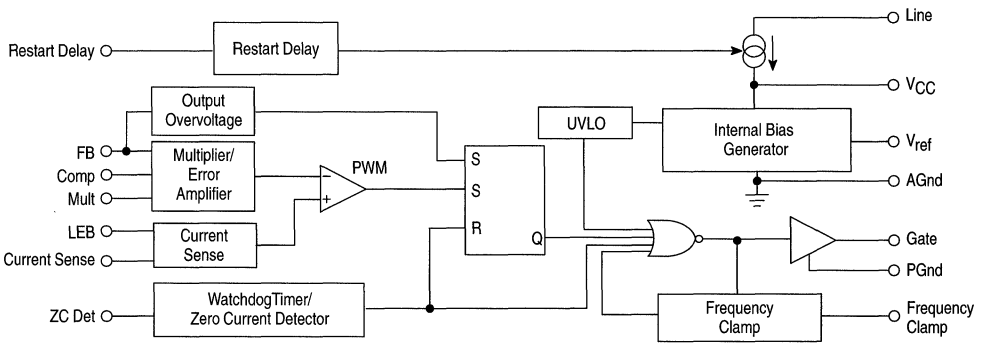
D SUFFIX
PLASTIC PACKAGE
CASE 751K
(SO–16)

PIN CONNECTIONS



(Top View)

Representative Block Diagram



This device contains 240 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage (Transient)	V_{CC}	20	V
Power Supply Voltage (Operating)	V_{CC}	16	V
Line Voltage	V_{Line}	500	V
Current Sense, Multiplier, Compensation, Voltage Feedback, Restart Delay and Zero Current Input Voltage	V_{in1}	−1.0 to +10	V
LEB Input, Frequency Clamp Input	V_{in2}	−1.0 to +20	V
Zero Current Detect Input	I_{in}	±5.0	mA
Restart Diode Current	I_{in}	5.0	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$	 450 178	 mW °C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	−25 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14.5 V, for typical values T_A = 25°C, for min/max values T_J = −25 to +125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	0	1.0	µA
Input Offset Voltage (V_{Comp} = 3.0 V)	V_{IO}	–	2.0	50	mV
Transconductance (V_{Comp} = 3.0 V)	g_m	30	51	80	µmho
Output Source (V_{FB} = 4.6 V, V_{Comp} = 3.0 V) Output Sink (V_{FB} = 5.4 V, V_{Comp} = 3.0 V)	I_O I_O	9.0 9.0	17.5 17.5	30 30	µA
OVERVOLTAGE COMPARATOR					
Voltage Feedback Input Threshold	$V_{FB(OV)}$	1.07 V_{FB}	1.084 V_{FB}	1.1 V_{FB}	V
Propagation Time to Output	T_P	–	705	–	ns
MULTIPLIER					
Input Bias Current, V_{Mult} (V_{FB} = 0 V)	I_{IB}	–	−0.2	−1.0	µA
Input Threshold, V_{Comp}	$V_{th(M)}$	1.8	2.1	2.4	V
Dynamic Input Voltage Range Multiplier Input Compensation	 V_{Mult} V_{Comp}	 0 to 2.5 $V_{th(M)}$ to ($V_{th(M)}$ + 1.0)	 0 to 3.5 $V_{th(M)}$ to ($V_{th(M)}$ + 2.0)	 – –	V
Multiplier Gain (V_{Mult} = 0.5 V, V_{Comp} = $V_{th(M)}$ + 1.0 V) $K = \frac{V_{CS}\ \text{Threshold}}{V_{Mult}\left(V_{Comp} - V_{th(M)}\right)}$	K	0.25	0.51	0.75	1/V
VOLTAGE REFERENCE					
Voltage Reference (I_O = 0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	V
Line Regulation (V_{CC} = 10 V to 16 V)	Reg_{line}	–	5.0	100	mV
Load Regulation (I_O = 0 – 5.0 mA)	Reg_{load}	–	5.0	100	mV
Total Output Variation Over Line, Load and Temperature	V_{ref}	4.8	–	5.2	V
Maximum Output Current	I_O	5.0	10	–	mA
Reference Undervoltage Lockout Threshold	V_{th}	–	4.5	–	V

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 14.5 V, for typical values T_A = 25°C, for min/max values T_J = –25 to +125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Increasing)	V_{th}	1.0	1.2	1.4	V
Hysteresis (V_{in} Decreasing)	V_H	100	200	300	mV
Delay to Output	T_{pd}	–	127	–	ns
CURRENT SENSE COMPARATOR					
Input Bias Current (V_{CS} = 0 to 2.0 V)	I_{IB}	–	0.2	1.0	µA
Input Offset Voltage (V_{Mult} = –0.2 V)	V_{IO}	–	4.0	50	mV
Maximum Current Sense Input Threshold (V_{Comp} = 5.0 V, V_{Mult} = 5.0 V)	$V_{th(max)}$	1.3	1.5	1.8	V
Delay to Output (V_{LEB} = 12 V, V_{Comp} = 5.0 V, V_{Mult} = 5.0 V) (V_{CS} = 0 to 5.0 V Step, C_L = 1.0 nF)	$t_{PHL(in/out)}$	50	270	425	ns
FREQUENCY CLAMP					
Frequency Clamp Input Threshold	$V_{th(FC)}$	1.9	2.0	2.1	V
Frequency Clamp Capacitor Reset Current (V_{FC} = 0.5 V)	I_{reset}	0.5	1.7	4.0	mA
Frequency Clamp Disable Voltage	V_{DFC}	–	7.3	8.0	V
DRIVE OUTPUT					
Source Resistance (Drive = 0 V, V_{Gate} = V_{CC} – 1.0 V) Sink Resistance (Drive = V_{CC}, V_{Gate} = 1.0 V)	R_{OH} R_{OL}	4.0 4.0	8.6 7.2	20 20	Ω
Output Voltage Rise Time (25% – 75%) (C_L = 1.0 nF)	t_r	–	55	200	ns
Output Voltage Fall Time (75% – 25%) (C_L = 1.0 nF)	t_f	–	70	200	ns
Output Voltage in Undervoltage (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{O(UV)}$	–	0.01	0.25	V
LEADING EDGE BLANKING					
Input Bias Current	I_{bias}	–	0.1	0.5	µA
Threshold (as Offset from V_{CC}) (V_{LEB} Increasing)	V_{LEB}	1.0	2.25	2.75	V
Hysteresis (V_{LEB} Decreasing)	V_H	100	270	500	mV
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	11.5	13	14.5	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{Shutdown}$	7.0	8.5	10	V
Hysteresis	V_H	–	4.5	–	V
TIMER					
Watchdog Timer	t_{DLY}	180	385	800	µs
Restart Timer Threshold	$V_{th(restart)}$	1.5	2.3	3.0	V
Restart Pin Output Current ($V_{restart}$ = 0 V, V_{ref} = 5.0 V)	$I_{restart}$	3.1	5.2	7.1	mA
TOTAL DEVICE					
Line Startup Current (V_{CC} = 0 V, V_{Line} = 50 V)	I_{SU}	5.0	16	25	mA
Line Operating Current (V_{CC} = $V_{th(on)}$, V_{Line} = 50 V)	I_{OP}	3.0	12.9	20	mA
V_{CC} Dynamic Operating Current (50 kHz, C_L = 1.0 nF) V_{CC} Static Operating Current (I_O = 0)	I_{CC}	– –	5.3 3.0	8.5 –	mA
Line Pin Leakage (V_{Line} = 500 V)	I_{Line}	–	30	80	µA

Figure 1. Current Sense Input Threshold versus Multiplier Input

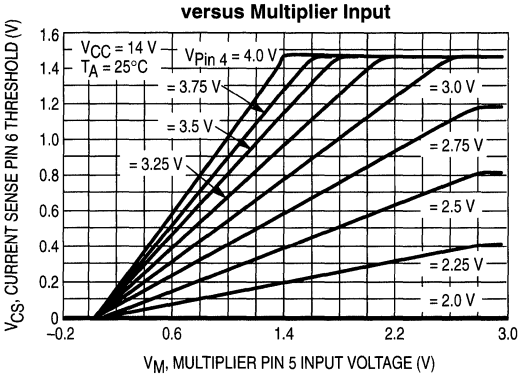


Figure 2. Current Sense Input Threshold versus Multiplier Input, Expanded View

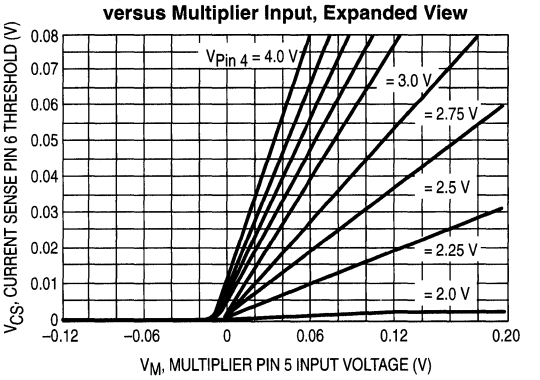


Figure 3. Reference Voltage versus Temperature

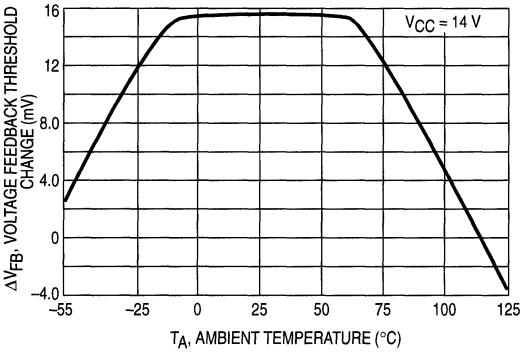


Figure 4. Overvoltage Comparator Input Threshold versus Temperature

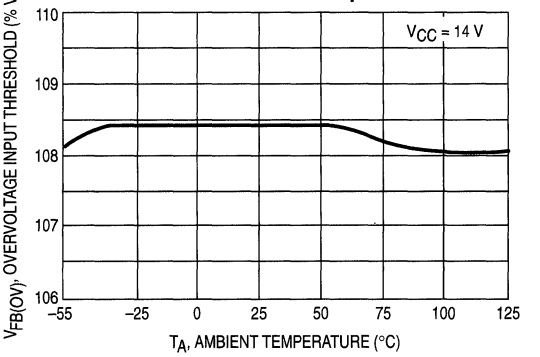


Figure 5. Error Amplifier Transconductance and Phase versus Frequency

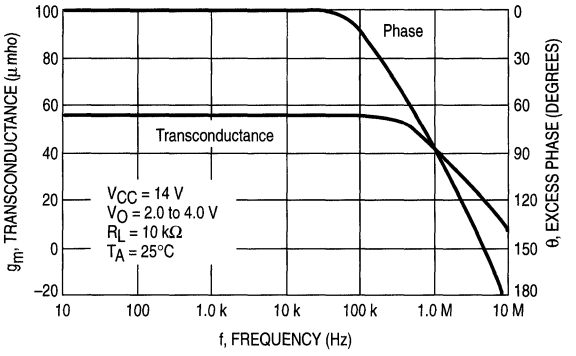
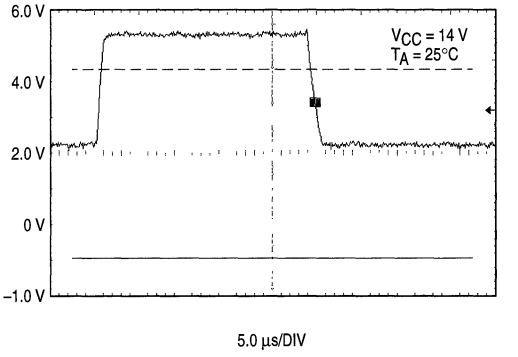


Figure 6. Error Amplifier Transient Response



3

Figure 7. Quickstart Charge Current versus Temperature

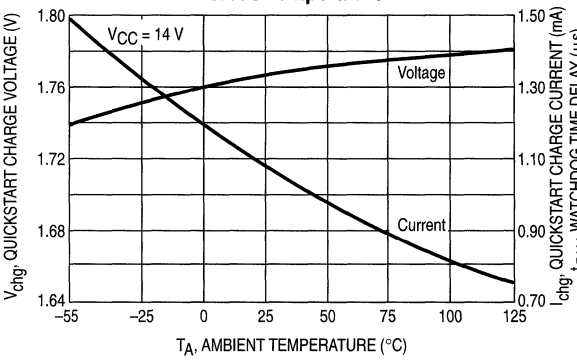


Figure 8. Watchdog Timer Delay versus Temperature

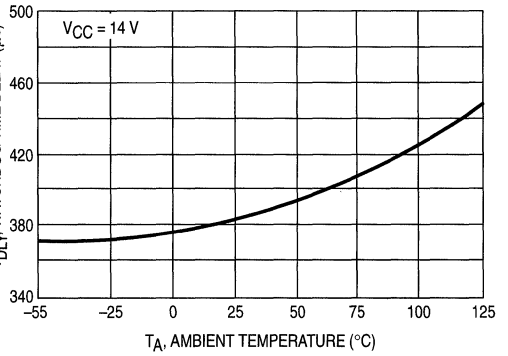


Figure 9. Drive Output Waveform

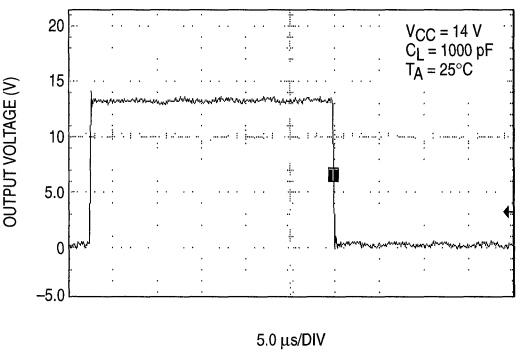


Figure 10. Supply Current versus Supply Voltage

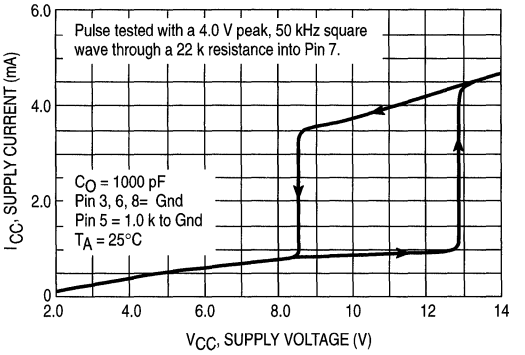


Figure 11. Transient Thermal Resistance

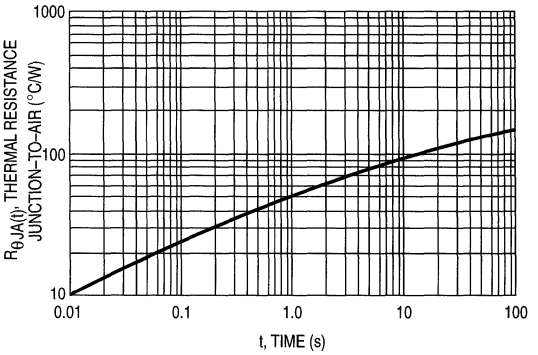
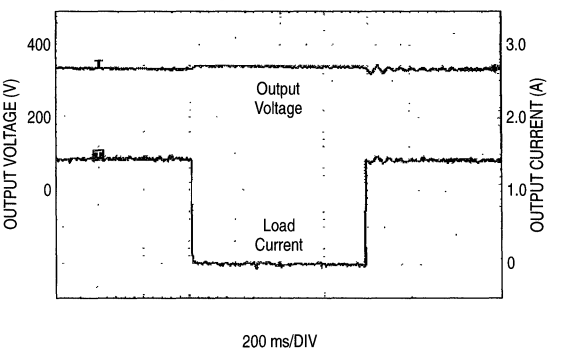


Figure 12. Low Load Detection Response Waveform



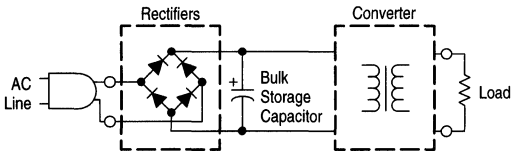
FUNCTIONAL DESCRIPTION

INTRODUCTION

With the goal of exceeding the requirements of legislation on line current harmonic content, there is an ever increasing demand for an economical method of obtaining a unity power factor. This data sheet describes a monolithic control IC that was specifically designed for power factor control with minimal external components. It offers the designer a simple cost effective solution to obtain the benefits of active power factor correction.

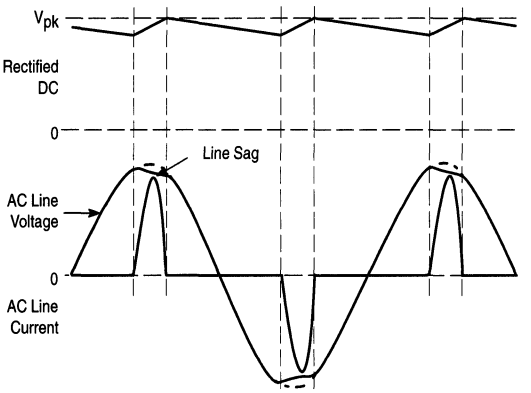
Most electronic ballasts and switching power supplies use a bridge rectifier and a bulk storage capacitor to derive raw dc voltage from the utility ac line, Figure 13.

Figure 13. Uncorrected Power Factor Circuit



This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike, Figure 14. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power. Power factor ratios of 0.5 to 0.7 are common.

Figure 14. Uncorrected Power Factor Input Waveforms



Power factor correction can be achieved with the use of either a passive or active input circuit. Passive circuits usually contain a combination of large capacitors, inductors, and rectifiers that operate at the ac line frequency. Active circuits incorporate some form of a high frequency switching converter for the power processing with the boost converter being the most popular topology. Since active input circuits operate at a frequency much higher than that of the ac line, they are smaller, lighter in weight, and more efficient than a passive circuit that yields similar results. With proper control of the preconverter, almost any complex load can be made to appear resistive to the ac line, thus significantly reducing the harmonic current content.

Operating Description

The MC33368 contains many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. Referring to the block diagram in Figure 15, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. A description of each of the functional blocks is given below.

Error Amplifier

An Error Amplifier with access to the inverting input and output is provided. The amplifier is a transconductance type, meaning that it has high output impedance with controlled voltage–to–current gain ($g_m \approx 50$ μmhos). The noninverting input is internally biased at 5.0 V ±2.0%. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is –1.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R2. The Error Amplifier output is internally connected to the Multiplier and is pinned out (Pin 4) for external loop compensation. Typically, the bandwidth is set below 20 Hz so that the amplifier's output voltage is relatively constant over a given ac line cycle. In effect, the error amplifier monitors the average output voltage of the converter over several line cycles resulting in a fixed Drive Output on–time. The amplifier output stage can sink and source 11.5 μA of current and is capable of swinging from 1.7 to 5.0 V, assuring that the Multiplier can be driven over its entire dynamic range.

Note that by using a transconductance type amplifier, the input is allowed to move independently with respect to the output, since the compensation capacitor is connected to ground. This allows dual usage of the Voltage Feedback pin by the Error Amplifier and Overvoltage Comparator.

Overvoltage Comparator

An Overvoltage Comparator is incorporated to eliminate the possibility of runaway output voltage. This condition can occur during initial startup, sudden load removal, or during output arcing and is the result of the low bandwidth that must be used in the Error Amplifier control loop. The Overvoltage Comparator monitors the peak output voltage of the converter, and when exceeded, immediately terminates MOSFET switching. The comparator threshold is internally set to 1.08 V_{ref}. In order to prevent false tripping during normal operation, the value of the output filter capacitor C3 must be large enough to keep the peak–to–peak ripple less than 16% of the average dc output.

Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The ac haversines are monitored at Pin 5 with respect to ground while the Error Amplifier output at Pin 4 is monitored with respect to the Voltage Feedback Input threshold. A graph of the Multiplier transfer curve is shown in Figure 1. Note that both inputs are extremely linear over a wide dynamic range, 0 to 3.2 V for Pin 5 and 2.5 to 4.0 V for Pin 4. The Multiplier output controls the Current Sense Comparator threshold as

the ac voltage traverses sinusoidally from zero to peak line. This has the effect of forcing the MOSFET on–time to track the input line voltage, thus making the preconverter load appear to be resistive.

$$\text{Pin 6 Threshold} \approx 0.55 \left(V_{\text{Pin 4}} - V_{\text{Pin 3}}\right) V_{\text{Pin 5}}$$

Zero Current Detector

The MC33368 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on–time by setting the R_S Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn–on until the inductor current reaches zero, the output rectifier's reverse recovery time becomes less critical allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous thus limiting the peak switch to twice the average input current

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.2 V. To prevent false tripping, 200 mV of hysteresis is provided. The Zero Current Detector input is internally protected by two clamps. The upper 10 V clamp prevents input overvoltage breakdown while the lower –0.7 V clamp prevents substrate injection. An external resistor must be used in series with the auxiliary winding to limit the current through the clamps to 5.0 mA or less.

Current Sense Comparator and RS Latch

The Current Sense Comparator R_S Latch configuration used ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground–referenced sense resistor R7 in series with the source of output switch. This voltage is monitored by the Current Sense Input and compared to a level derived from the Multiplier output. The peak inductor current under normal operating conditions is controlled by the threshold voltage of Pin 6 where:

$$I_{pk} = \frac{\text{Pin 6 Threshold}}{R7}$$

Abnormal operating conditions occur when the preconverter is running at extremely low line or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.5 V. Therefore, the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.5\ V}{R7}$$

With the component values shown in Figure 15, the Current Sense Comparator threshold, at the peak of the haversine, varies from 110 mV at 90 Vac to 100 mV at 268 Vac. The Current Sense Input to Drive Output propagation delay is typically 200 ns.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 385 μs after the inductor current reaches zero.

Undervoltage Lockout and Quickstart

The MC33368 has a 5.0 V internal reference brought out to Pin 1 and capable of sourcing 10 mA typically. It also contains an Undervoltage Lockout (UVLO) circuit which suppresses the Gate output at Pin 11 if the V_{CC} supply voltage drops below 8.5 V typical.

A Quickstart circuit has been incorporated to optimize converter startup. During initial startup, compensation capacitor C1 will be discharged, holding the Error Amplifier output below the Multiplier's threshold. This will prevent Drive Output switching and delay bootstraping of capacitor C4 by diode D6. If Pin 4 does not reach the multiplier threshold before C4 discharges below the lower SMPS UVLO threshold, the converter will hiccup and experience a significant startup delay. The Quickstart circuit is designed to precharge C1 to 1.7 V. This level is slightly below the Pin 4 Multiplier threshold, allowing immediate Drive Output switching.

Restart Delay

A restart delay pin is provided to allow hiccup mode fault protection in case of a short circuit condition and to prevent the SMPS from repeatedly trying to restart after the input line voltage has been removed. When power is first applied, there is no startup delay, but subsequent cycling of the V_{CC} voltage will result in delay times that are programmed by an external resistor and capacitor. The Restart Delay, Pin 2, is a high impedance, so that an external capacitor can provide delay times as long as several seconds.

If the SMPS output is short circuited, the transformer winding, which provides the V_{CC} voltage to the control IC and the MC33368, will be unable to sustain V_{CC} to the control circuits. The restart delay capacitor at Pin 2 of the MC33368 prevents the high voltage startup transistor within the IC from maintaining the voltage on C4. After V_{CC} drops below the UVLO threshold in the SMPS, the SMPS switching transistors are held off for the time programmed by the values of the restart capacitor (C9) and resistor (R8). In this manner, the SMPS switching transistors are operated at very low duty cyles, preventing their destruction. If the short circuit fault is removed, the power supply system will turn on by itself in a normal startup mode after the restart delay has timed out.

Output Switching Frequency Clamp

In normal operation, the MC33368 operates the boost inductor in the critical mode. That is, the inductor current ramps to a peak value, ramps down to zero, then immediately begins ramping positive again. The peak current is programmed by the multiplier output within the IC. As the input voltage haversine declines to near zero, the output switch on–time becomes constant, rather than going to zero because of the small integrated dc voltage at Pin 5 caused by C2, R3 and R5. Because of this, the average line current does not exactly follow the line voltage near the zero crossings. The Output Switching Frequency Clamp remedies this situation to improve power factor and minimize EMI generated in this operating region. The values of R10 and C7 program a minimum off–time in the frequency clamp which overrides the zero current detect signal, forcing a minimum off–time. This allows discontinuous conduction operation of the boost inductor in the zero crossing region, and the average line current more nearly follows the voltage. The Output Switching Frequency Clamp function can be disabled by connecting the FC input, Pin 13, to the V_{CC} supply Pin 12.

Output

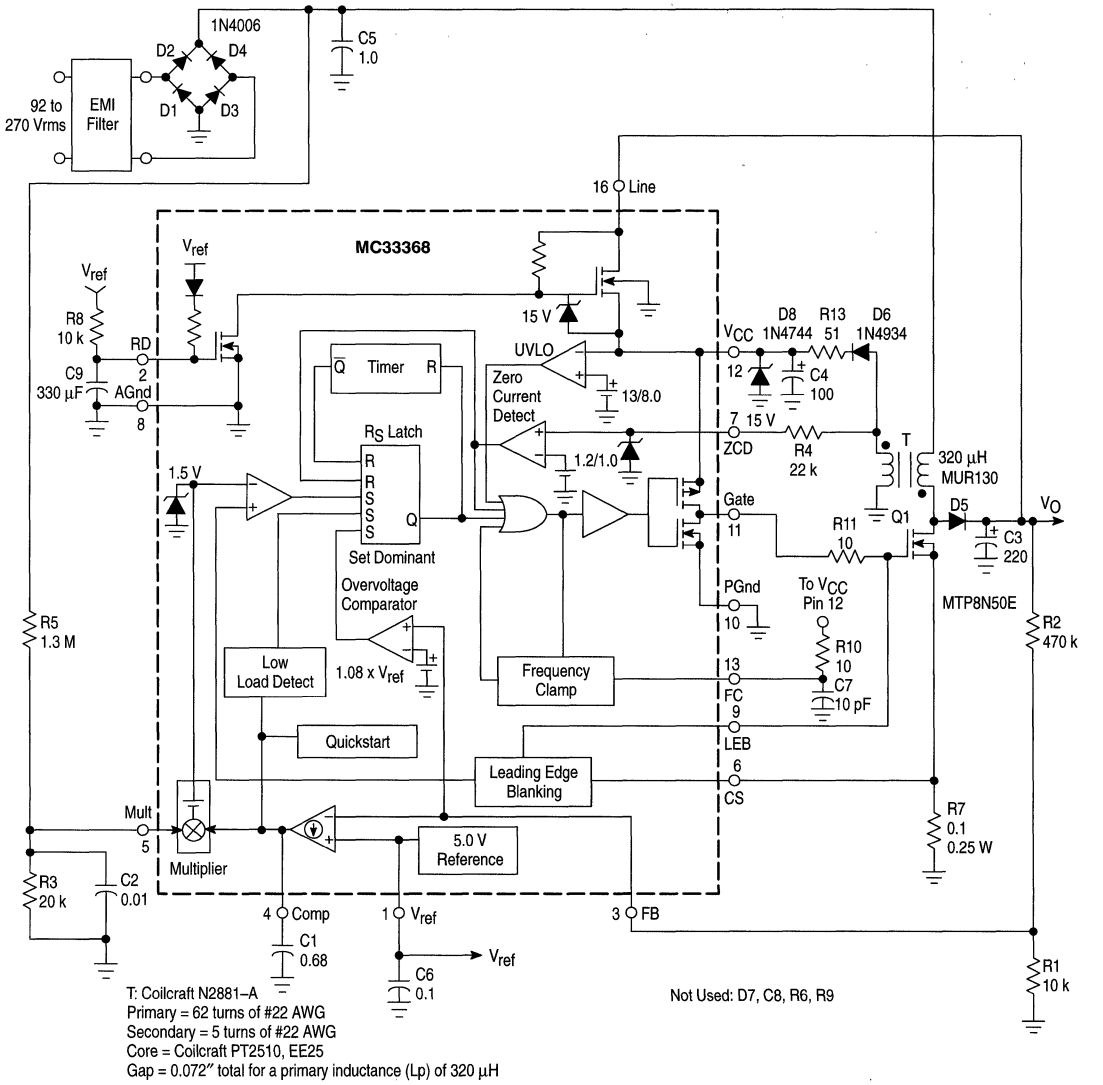
The IC contains a CMOS output driver that was specifically designed for direct drive of power MOSFETs. The Drive Output is capable of up to ±1500 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull–down resistor. The totem–pole output has been optimized to minimize cross–conduction current during high speed operation.

Table 1. Design Equations

Calculation	Formula	Notes
Converter Output Power	$P_O = V_O I_O$	Calculate the maximum required output power.
Peak Indicator Current	$I_{L(pk)} = \frac{2\sqrt{2}\ P_O}{\eta\ Vac_{(LL)}}$	Calculated at the minimum required ac line voltage for output regulation. Let the efficiency $\eta = 0.92$ for low line operation.
Inductance	$L_P = \frac{t\left(\frac{V_O}{\sqrt{2}} - Vac_{(LL)}\right)\eta\ Vac_{(LL)}^2}{\sqrt{2}\ V_O\ P_O}$	Let the switching cycle t = 40 μs for universal input (85 to 265 Vac) operation and 20 μs for fixed input (92 to 138 Vac, or 184 to 276 Vac) operation.
Switch On–Time	$t_{(on)} = \frac{2\ P_O\ L_P}{\eta\ Vac^2}$	In theory, the on–time $t_{(on)}$ is constant. In practice, $t_{(on)}$ tends to increase at the ac line zero crossings due to the charge on capacitor C5. Let Vac = $Vac_{(LL)}$ for initial $t_{(on)}$ and $t_{(off)}$ calculations.
Switch Off–Time	$t_{(off)} = \frac{t_{(on)}}{\frac{V_O}{\sqrt{2}\ Vac\ \lvert Sin\ \theta\rvert} - 1}$	The off–time $t_{(off)}$ is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (0) represents the angle of the ac line voltage.
Minimum Switch Off–Time	$t_{(off)min} = \frac{L_P\ I_{L(pk)}}{V_O}$	The off–time is at a minimum at ac line crossings. This equation is used to calculate $t_{(off)}$ as Theta approaches zero.
Delay Time	$t_d = -\ R10\ C7\ ln\left(\frac{V_{CC} - 2}{V_{CC}}\right)$	The delay time is used to override the minimum off–time at the ac line zero crossings by programming the Frequency Clamp with C7 and R10.
Switching Frequency	$f = \frac{1}{t_{(on)} + t_{(off)}}$	The minimum switching frequency occurs at the peak of the ac line voltage. As the ac line voltage traverses from peak to zero, $t_{(off)}$ approaches zero producing an increase in switching frequency.
Peak Switch Current	$R7 = \frac{V_{CS}}{I_{L(pk)}}$	Set the current sense threshold V_{CS} to 1.0 V for universal input (85 to 265 Vac) operation and to 0.5 V for fixed input (92 to 138 Vac, or 184 to 276 Vac) operation. Note that V_{CS} must be less than 1.4 V.
Multiplier Input Voltage	$V_M = \frac{Vac\ \sqrt{2}}{\left(\frac{R5}{R3} + 1\right)}$	Set the mulltiplier input voltage V_M to 3.0 V at high line. Empirically adjust V_M for the lowest distortion over the ac line voltage range while guaranteeing startup at minimum line.
Converter Output Voltage	$V_O = V_{ref}\left(\frac{R2}{R1} + 1\right) - I_{IB}\ R1$	The I_{IB} R1 error term can be minimized with a divider current in excess of 100 μA.
Converter Output Peak–to–Peak Ripple Voltage	$\Delta V_{O(pp)} = I_{L(pk)}\sqrt{\left(\frac{1}{2\ \pi\ f_{ac}\ C3}\right)^2 + ESR^2}$	The calculated peak–to–peak ripple must be less than 16% of the average dc output voltage to prevent false tripping of the Overvoltage Comparator. Refer to the Overvoltage Comparator Text. ESR is the equivalent series resistance of C3.
Error Amplifier Bandwidth	$BW = \frac{g_m}{2\ \pi\ C1}$	The bandwidth is typically set to 20 Hz. When operating at high ac line, the value of C1 may need to be increased.

NOTE: The following converter characteristics must be chosen:
V_O = Desired output voltage.
I_O = Desired output current.
Vac = AC RMS operating line voltage.
$Vac_{(LL)}$ = AC RMS minimum required operating line voltage for output regulation.
ΔV_O = Converter output peak–to–peak ripple voltage.

Figure 15. 80 W Power Factor Controller



T: Coilcraft N2881–A
Primary = 62 turns of #22 AWG
Secondary = 5 turns of #22 AWG
Core = Coilcraft PT2510, EE25
Gap = 0.072″ total for a primary inductance (Lp) of 320 µH

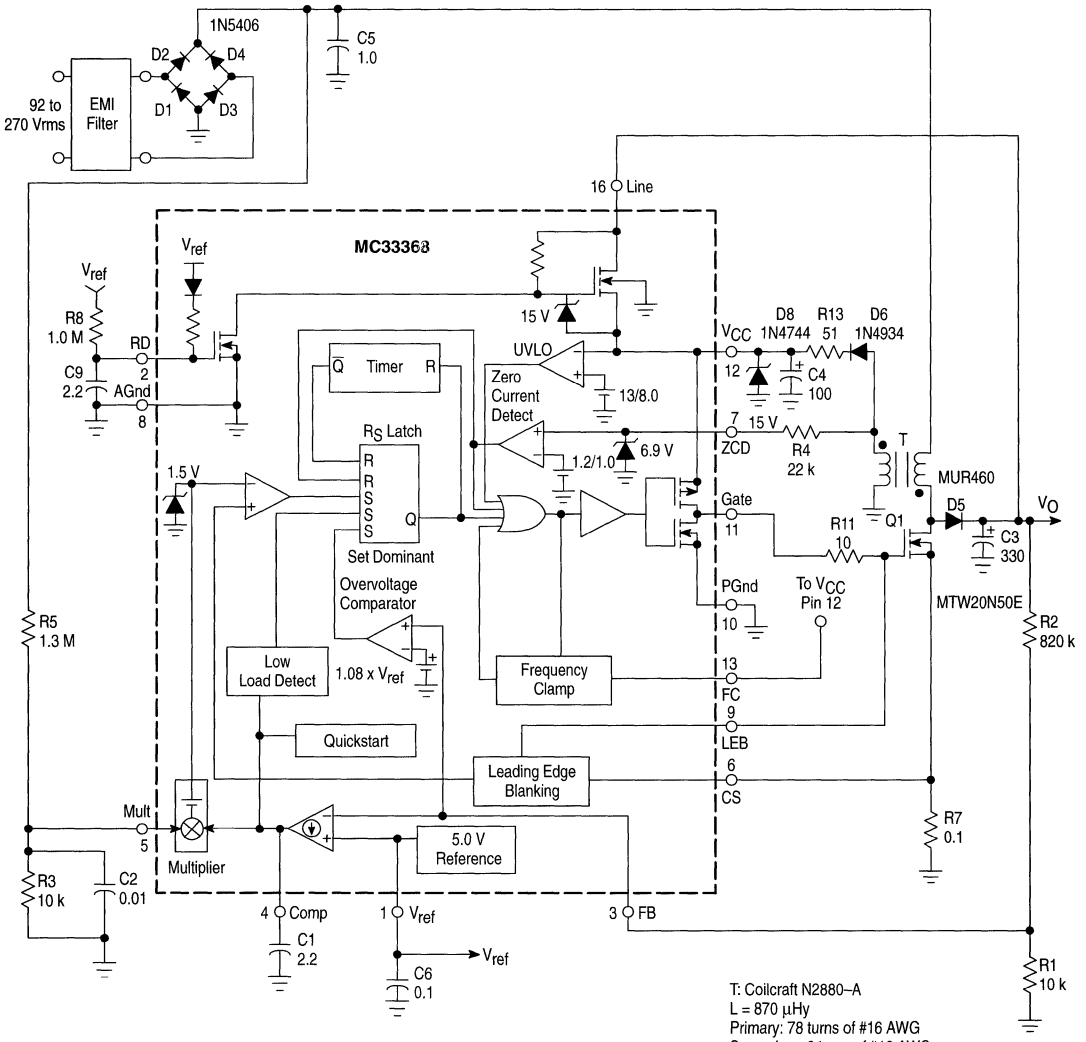
Not Used: D7, C8, R6, R9

Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	Pin	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	n(%)
90	79.7	0.999	0.89	0.5	0.15	0.09	0.06	0.09	3.0	244.4	0.31	76.01	95.4
100	79.3	0.998	0.79	0.5	0.14	0.09	0.08	0.10	3.0	242.9	0.31	75.54	95.3
110	78.9	0.997	0.72	0.5	0.16	0.13	0.08	0.10	3.0	242.9	0.31	75.30	95.4
120	78.5	0.996	0.66	0.5	0.15	0.12	0.08	0.13	3.0	243.0	0.31	75.57	96.3
130	78.1	0.994	0.60	0.5	0.14	0.12	0.07	0.14	3.0	243.0	0.31	75.57	96.7
138	77.8	0.991	0.57	0.5	0.15	0.14	0.08	0.14	3.0	243.0	0.31	75.57	97.1

Heatsink = AAVID Engineering Inc., 590302B03600, or 593002B03400

Figure 16. 175 W Universal Input Power Factor Controller



Not Used: D7, C7, C8, R6, R9, R10

T: Coilcraft N2880–A
L = 870 μHy
Primary: 78 turns of #16 AWG
Secondary: 6 turns of #18 AWG
Core: Coilcraft PT4215, EE42–15
Gap: 0.104″ total

Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	Pin	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	n(%)
90	190.4	0.995	2.11	5.8	0.16	0.32	0.24	0.80	3.6	398.0	0.44	175.9	92.4
120	192.1	0.997	1.60	3.2	0.08	0.17	0.07	0.30	3.6	398.9	0.44	177.1	92.2
138	192.7	0.997	1.40	0.9	0.08	0.24	0.03	0.15	3.6	402.3	0.45	179.0	92.9
180	194.3	0.995	1.08	0.9	0.04	0.18	0.04	0.08	3.6	409.1	0.45	182.9	94.1
240	189.3	0.983	0.80	0.7	0.08	0.21	0.08	0.06	3.6	407.0	0.45	181.1	95.7
268	186.3	0.972	0.71	0.6	0.11	0.32	0.10	0.10	3.6	406.2	0.44	180.4	96.8

Heatsink = AAVID Engineering Inc., 590302B03600

3

Figure 17. Power Factor Test Setup

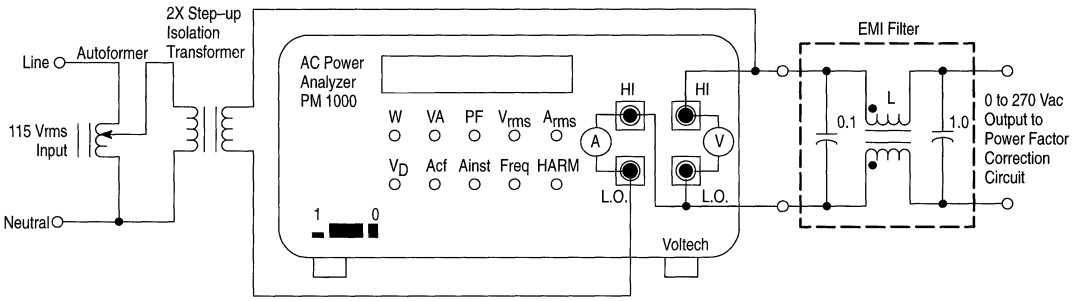


Figure 18. On/Off Control

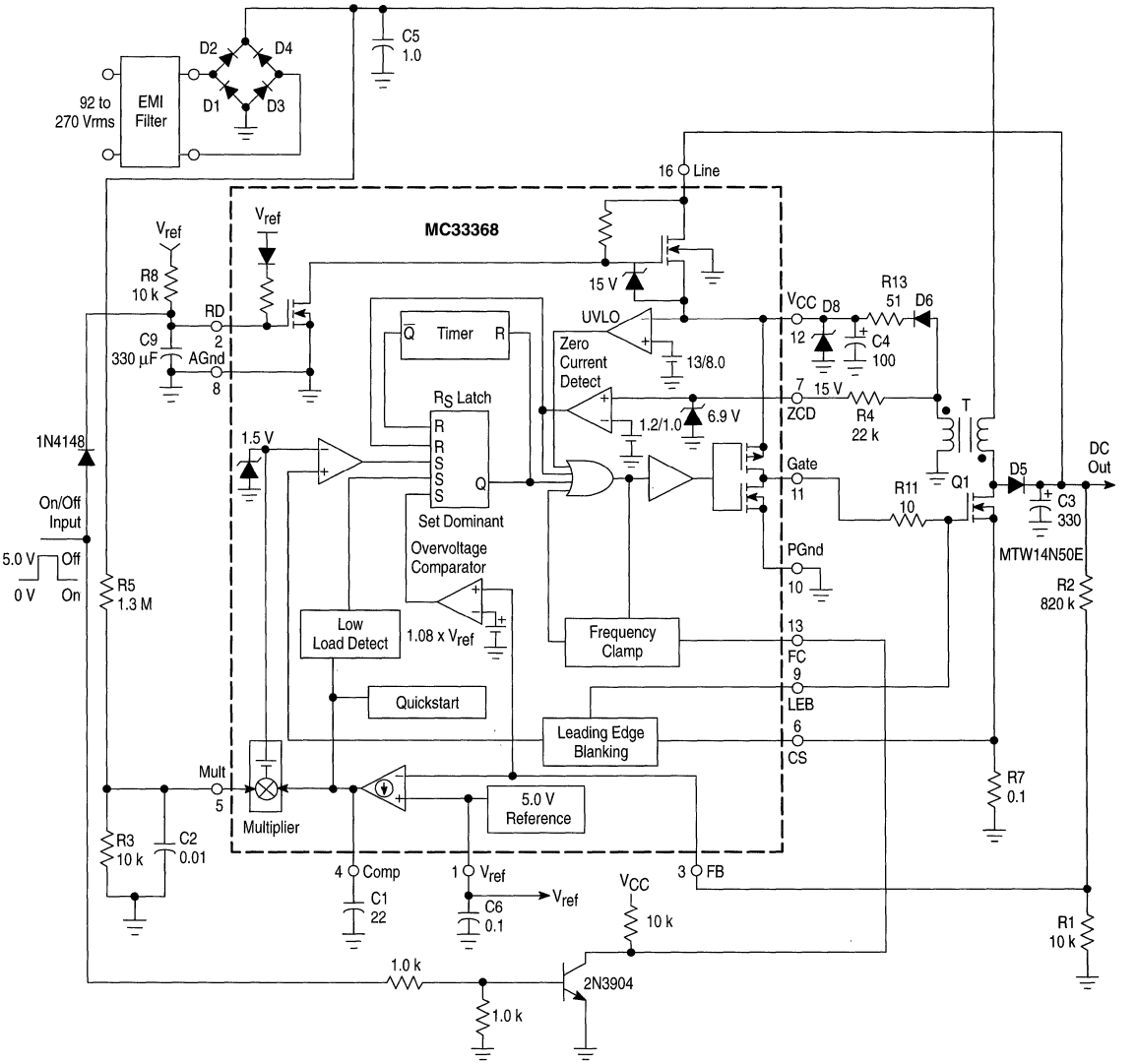
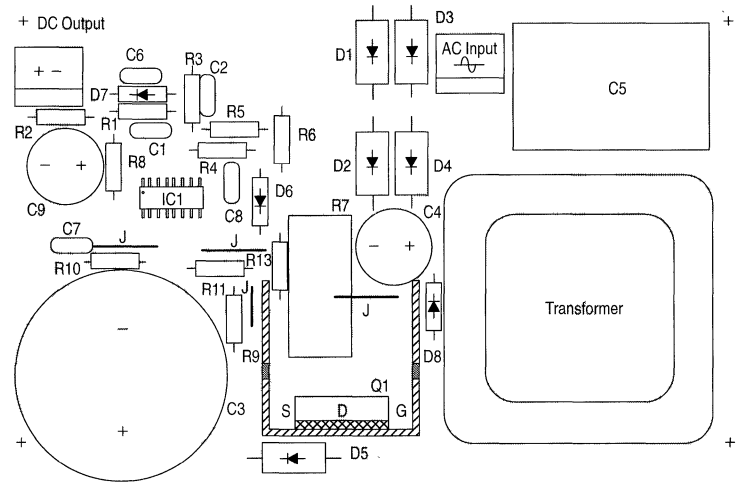
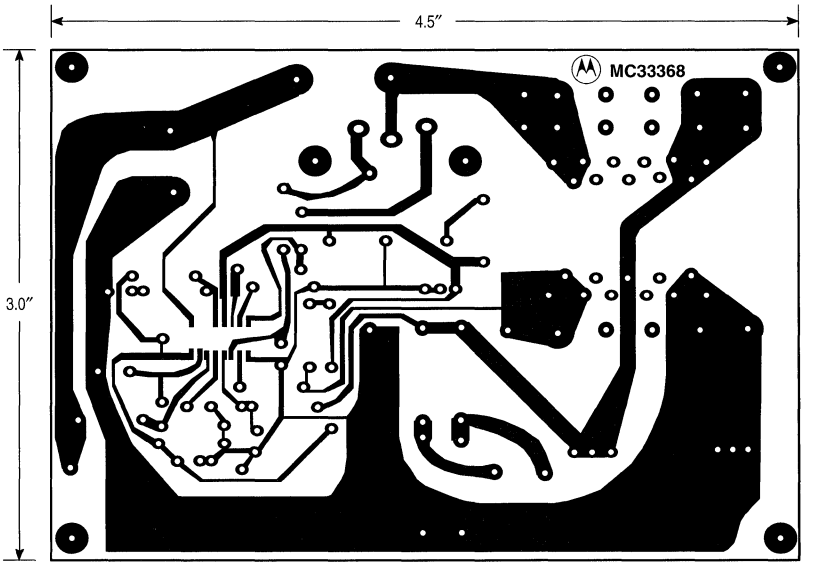


Figure 19. Printed Circuit Board and Component Layout (Circuits of Figures 15 and 16)





MOTOROLA

MC33463

3

Product Preview

Variable Frequency Micropower DC-to-DC Converter

The MC33463 series are micropower switching voltage regulators, specifically designed for handheld and laptop applications, to provide regulated output voltages using a minimum of external parts. A wide choice of output voltages are available. These devices feature a very low quiescent bias current of 4.0 μA typical.

The MC33463H–XXLT1 series features a highly accurate voltage reference, an oscillator, a variable frequency modulation (VFM) controller, a driver transistor (Lx), an error amplifier and feedback resistive divider.

The MC33463H–XXLT1 is identical to the MC33463H–XXKT1, except that a drive pin (EXT) for an external transistor is provided.

Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC33463 Series Features:

- Low Quiescent Bias Current of 4.0 μA
- High Output Voltage Accuracy of ±2.5%
- Low Startup Voltage of 0.9 V at 1.0 mA
- Surface Mount Package

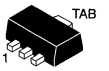
ORDERING INFORMATION

Device	Output Voltage	Type	Operating Temperature Range	Package (Tape/Reel)
MC33463H–30KT1 MC33463H–33KT1 MC33463H–50KT1	3.0 3.3 5.0	Int. Switch	T_A = –30° to +80°C	SOT–89 (Tape)
MC33463H–30LT1 MC33463H–33LT1 MC33463H–50LT1	3.0 3.3 5.0	Ext. Switch Drive		SOT–89 (Tape)

Other voltages from 2.5 V to 7.5 V, in 0.1 V increments are available upon request. Consult your local Motorola sales office for information.

VARIABLE FREQUENCY MICROPOWER DC–to–DC CONVERTER

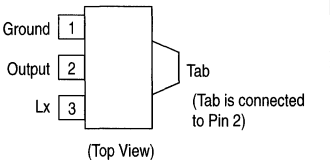
SEMICONDUCTOR TECHNICAL DATA



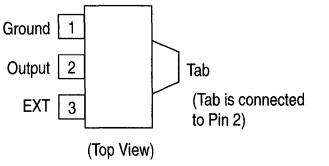
H SUFFIX
PLASTIC PACKAGE
CASE 1213
(SOT–89)

PIN CONNECTIONS

MC33463H–XXKT1

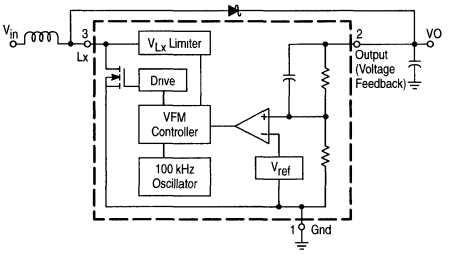


MC33463H–XXLT1

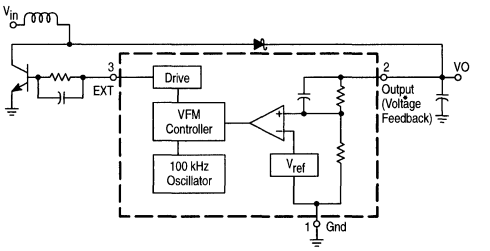


Representative Block Diagram

MC33463H–XXKT1



MC33463H–XXLT1



This device contains 100 active transistors.

MC33464

3

Product Preview

Micropower Undervoltage Sensing Circuits

MICROPOWER UNDERVOLTAGE SENSING CIRCUITS

SEMICONDUCTOR TECHNICAL DATA

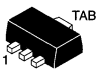
The MC33464 series are micropower undervoltage sensing circuits that are specifically designed for use with battery powered microprocessor based systems, where extended battery life is required. A choice of several threshold voltages from 0.9 V to 4.5 V are available. These devices feature a very low quiescent bias current of 0.8 μA typical.

The MC33464 series features a highly accurate voltage reference, a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation, a choice of output configurations between open drain or complementary MOS, and guaranteed operation below 1.0 V with extremely low standby current. These devices are available in either SOT–89 3–pin or SOT–23 5–pin surface mount packages.

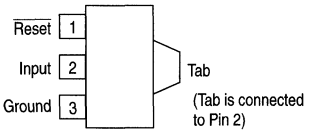
Applications include direct monitoring of the MPU/logic power supply used in portable, appliance, automotive and industrial equipment.

MC33464 Features:

- Extremely Low Standby Current of 0.8 μA at V_{in} = 1.5 V
- Wide Input Voltage Range (0.7 V to 10 V)
- Monitors Power Supply Voltages from 1.1 V to 5.0 V
- High Accuracy Detector Threshold (±2.5%)
- Two $\overline{\text{Reset}}$ Output Types (Open Drain or Complementary Drive)
- Two Surface Mount Packages (SOT–89 or SOT–23 5–Pin)

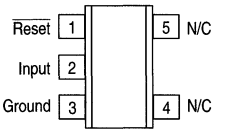


H SUFFIX
PLASTIC PACKAGE
CASE 1213
(SOT–89)



(Top View)

N SUFFIX
PLASTIC PACKAGE
CASE 1212
(SOT–23)



(Top View)

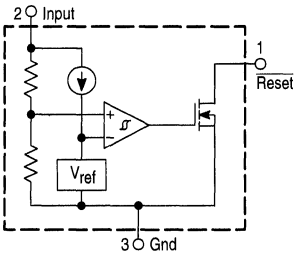
ORDERING INFORMATION

Device	Threshold Voltage	Type	Operating Temperature Range	Package (Qty/Reel)
MC33464H–09AT1	0.9	Open Drain $\overline{\text{Reset}}$	T_A = –30° to +80°C	SOT–89 (1000)
MC33464H–20AT1	2.0			
MC33464H–27AT1	2.7			
MC33464H–30AT1	3.0			
MC33464H–45AT1	4.5			
MC33464H–09CT1	0.9	Compl. MOS $\overline{\text{Reset}}$		
MC33464H–20CT1	2.0			
MC33464H–27CT1	2.7			
MC33464H–30CT1	3.0			
MC33464H–45CT1	4.5			
MC33464N–09ATR	0.9	Open Drain $\overline{\text{Reset}}$		SOT–23 (3000)
MC33464N–20ATR	2.0			
MC33464N–27ATR	2.7			
MC33464N–30ATR	3.0			
MC33464N–45ATR	4.5			
MC33464N–09CTR	0.9	Compl. MOS $\overline{\text{Reset}}$		
MC33464N–20CTR	2.0			
MC33464N–27CTR	2.7			
MC33464N–30CTR	3.0			
MC33464N–45CTR	4.5			

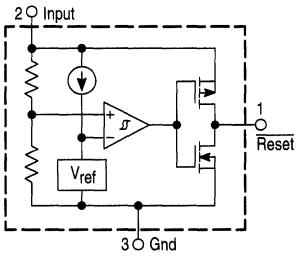
Other voltages from 0.9 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

Representative Block Diagrams

MC33464X–YYATZ
Open Drain Configuration



MC33464X–YYCTZ
Complementary Drive Configuration



X Denotes Package Type
YY Denotes Threshold Voltage
TZ Denotes Taping Type

This device contains 25 active transistors.

3

Product Preview

Micropower Undervoltage Sensing Circuits with Output Delay

The MC33465 series are micropower undervoltage sensing circuits that are specifically designed for use with battery powered microprocessor based systems, where extended battery life is required. A choice of several threshold voltages from 0.9 V to 4.5 V are available. This device features a very low quiescent bias current of 1.0 μA typical.

The MC33465 series features a highly accurate voltage reference, a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation, a choice of output configurations between open drain or complementary MOS, a time delayed output, which can be programmed by the system designer, and guaranteed operation below 1.0 V with extremely low standby current. This device is available in a SOT–23 5–pin surface mount packages.

Applications include direct monitoring of the MPU/logic power supply used in portable, appliance, automotive and industrial equipment.

MC33465 Features:

- Extremely Low Standby Current of 1.0 μA at V_{in} = 3.5 V
- Wide Input Voltage Range (0.7 V to 10 V)
- Monitors Power Supply Voltages from 1.1 V to 5.0 V
- High Accuracy Detector Threshold (±2.5%)
- Two $\overline{\text{Reset}}$ Output Types (Open Drain or Complementary Drive)
- Programmable Output Delay by External Capacitor (100 ms typ. with 0.15 μF)
- Surface Mount Package (SOT–23 5–Pin)
- Convenient Tape and Reel (3000 per Reel)

ORDERING INFORMATION

Device	Threshold Voltage	Type	Operating Temperature Range	Package
MC33465N–09ATR	0.9	Open Drain $\overline{\text{Reset}}$	T_A = –30° to +80°C	SOT–23
MC33465N–20ATR	2.0			
MC33465N–27ATR	2.7			
MC33465N–30ATR	3.0			
MC33465N–45ATR	4.5			
MC33465N–09CTR	0.9	Compl. MOS $\overline{\text{Reset}}$		
MC33465N–20CTR	2.0			
MC33465N–27CTR	2.7			
MC33465N–30CTR	3.0			
MC33465N–45CTR	4.5			

Other voltages from 0.9 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

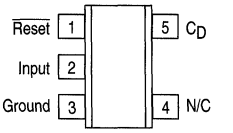
MC33465

MICROPOWER UNDERVOLTAGE SENSING CIRCUITS WITH OUTPUT DELAY

SEMICONDUCTOR TECHNICAL DATA

N SUFFIX
PLASTIC PACKAGE
CASE 1212
(SOT–23)

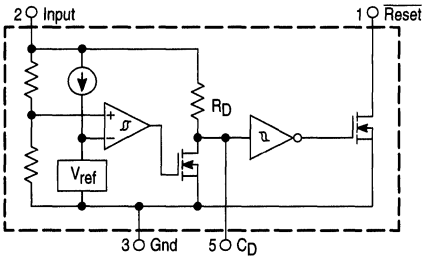
PIN CONNECTIONS



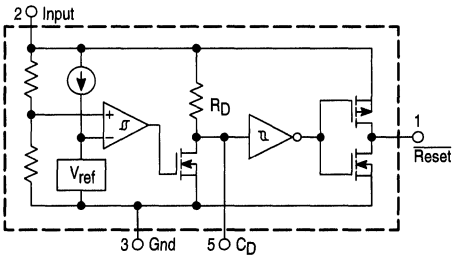
(Top View)

Representative Block Diagrams

MC33465N–YYATZ
Open Drain Configuration



MC33465N–YYCTZ
Complementary Drive Configuration



YY Denotes Threshold Voltage
TZ Denotes Taping Type

This device contains 28 active transistors.

MOTOROLA

MC33466

3

Product Preview

Fixed Frequency PWM Micropower DC-to-DC Converter

The MC33466 series are micropower switching voltage regulators, specifically designed for handheld and laptop applications, to provide regulated output voltages using a minimum of external parts. A wide choice of output voltages are available. These devices feature a very low quiescent bias current of 15 μA typical.

The MC33466H–XXJT1 series features a highly accurate voltage reference, an oscillator, a pulse width modulation (PWM) controller, a driver transistor (Lx), an error amplifier and feedback resistive divider.

The MC33466H–XXLT1 is identical to the MC33466H–XXJT1, except that a drive pin (EXT) for an external transistor is provided.

Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC33466 Series Features:

- Low Quiescent Bias Current of 15 μA
- High Output Voltage Accuracy of ±2.5%
- Low Startup Voltage of 0.9 V at 1.0 mA
- Soft–Start = 500 μs
- Surface Mount Package

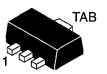
ORDERING INFORMATION

Device	Output Voltage	Type	Operating Temperature Range	Package (Tape/Reel)
MC33466H–30JT1 MC33466H–33JT1 MC33466H–50JT1	3.0 3.3 5.0	Int. Switch	T_A = –30° to +80°C	SOT–89 (Tape)
MC33466H–30LT1 MC33466H–33LT1 MC33466H–50LT1	3.0 3.3 5.0	Ext. Switch Drive	T_A = –30° to +80°C	SOT–89 (Tape)

Other voltages from 2.5 V to 7.5 V, in 0.1 V increments are available upon request. Consult your local Motorola sales office for information.

FIXED FREQUENCY PWM MICROPOWER DC–to–DC CONVERTER

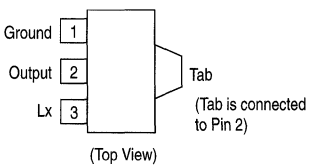
SEMICONDUCTOR TECHNICAL DATA



H SUFFIX
PLASTIC PACKAGE
CASE 1213
(SOT–89)

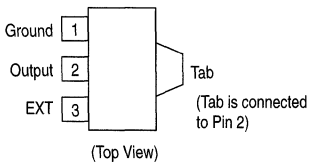
PIN CONNECTIONS

MC33466H–XXJT1



(Top View)

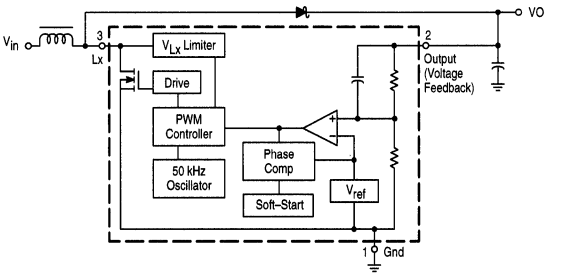
MC33466H–XXLT1



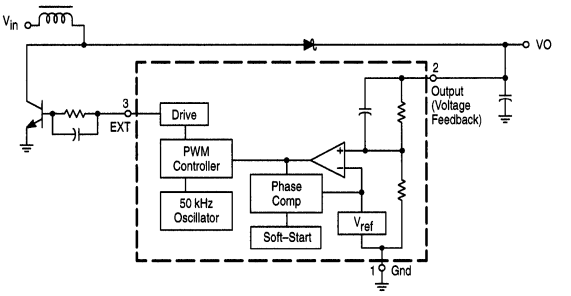
(Top View)

Representative Block Diagram

MC33466H–XXJT1



MC33466H–XXLT1



This device contains 100 active transistors.

MC34023
MC33023

High Speed Single-Ended PWM Controller

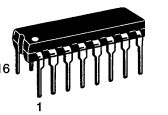
3

The MC34023 series are high speed, fixed frequency, single–ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off–Line and DC–to–DC converter applications offering the designer a cost–effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, a wide bandwidth error amplifier, a high speed current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

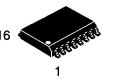
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, and a latch for single pulse metering.

The flexibility of this series allows it to be easily configured for either current mode or voltage mode control.

- 50 ns Propagation Delay to Output
- High Current Totem Pole Output
- Wide Bandwidth Error Amplifier
- Fully–Latched Logic with Double Pulse Suppression
- Latching PWM for Cycle–By–Cycle Current Limiting
- Soft–Start Control with Latched Overcurrent Reset
- Input Undervoltage Lockout with Hysteresis
- Low Start–Up Current (500 μA Typ)
- Internally Trimmed Reference with Undervoltage Lockout
- 90% Maximum Duty Cycle (Externally Adjustable)
- Precision Trimmed Oscillator
- Voltage or Current Mode Operation to 1.0 MHz
- Functionally Similar to the UC3823

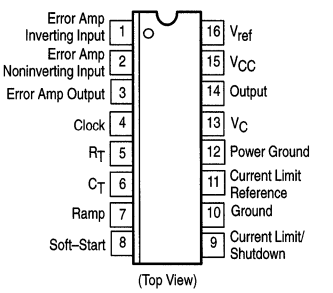


P SUFFIX
PLASTIC PACKAGE
CASE 648



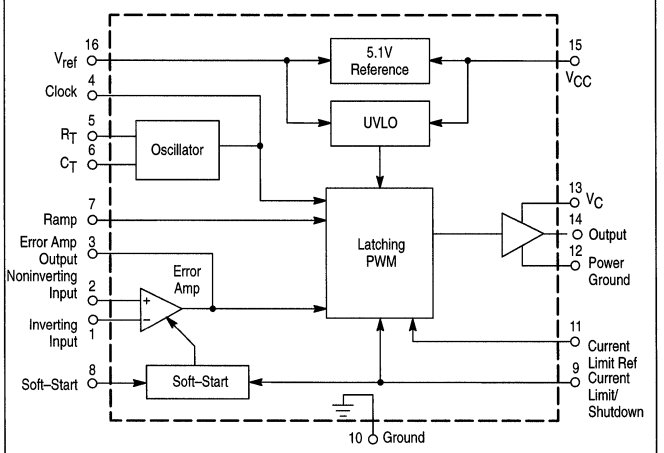
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

PIN CONNECTIONS



(Top View)

Simplified Application



This device contains 176 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33023P	$T_A = -40°$ to $+105°C$	Plastic DIP
MC33023DW		SO–16L
MC34023P	$T_A = 0°$ to $+70°C$	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	30	V
Output Driver Supply Voltage	V_C	20	V
Output Current, Source or Sink (Note 1) DC Pulsed (0.5 μs)	I_O	 0.5 2.0	A
Current Sense, Soft–Start, Ramp, and Error Amp Inputs	V_{in}	−0.3 to +7.0	V
Error Amp Output and Soft–Start Sink Current	I_O	10	mA
Clock and R_T Output Current	I_{CO}	5.0	mA
Power Dissipation and Thermal Characteristics SO–16L Package (Case 751G) Maximum Power Dissipation @ T_A = +25°C Thermal Resistance, Junction–to–Air DIP Package (Case 648) Maximum Power Dissipation @ T_A = +25°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 2) MC34023 MC33023	T_A	 0 to +70 −40 to +105	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = +25°C)	V_{ref}	5.05	5.1	5.15	V
Line Regulation (V_{CC} = 10 V to 30 V)	Reg_{line}	–	2.0	15	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	2.0	15	mV
Temperature Stability	T_S	–	0.2	–	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.95	–	5.25	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = +25°C)	V_n	–	50	–	μV
Long Term Stability (T_A = +125°C for 1000 Hours)	S	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	−30	−65	−100	mA
OSCILLATOR SECTION					
Frequency T_J = +25°C Line (V_{CC} = 10 V to 30 V) and Temperature (T_A = T_{low} to T_{high})	f_{osc}	 380 370	 400 400	 420 430	kHz
Frequency Change with Voltage (V_{CC} = 10 V to 30 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	%
Frequency Change with Temperature (T_A = T_{low} to T_{high})	$\Delta f_{osc}/\Delta T$	–	2.0	–	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	2.6	2.8	3.0	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	0.7	1.0	1.25	V
Clock Output Voltage High State Low State	 V_{OH} V_{OL}	 3.9 –	 4.5 2.3	 – 2.9	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34023, −40°C for MC33023 T_{high} = +70°C for MC34023, +105°C for MC33023

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage	V_{IO}	–	–	15	mV
Input Bias Current	I_{IB}	–	0.6	3.0	μA
Input Offset Current	I_{IO}	–	0.1	1.0	μA
Open–Loop Voltage Gain (V_O = 1.0 V to 4.0 V)	A_{VOL}	60	95	–	dB
Gain Bandwidth Product (T_J = +25°C)	GBW	4.0	8.3	–	MHz
Common Mode Rejection Ratio (V_{CM} = 1.5 V to 5.5 V)	CMRR	75	95	–	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 30 V)	PSRR	85	110	–	dB
Output Current, Source (V_O = 4.0 V) Sink (V_O = 1.0 V)	I_{Source} I_{Sink}	0.5 1.0	3.0 3.6	– –	mA
Output Voltage Swing, High State (I_O = −0.5 mA) Low State (I_O = 1 mA)	V_{OH} V_{OL}	4.5 0	4.75 0.4	5.0 1.0	V
Slew Rate	SR	6.0	12	–	V/μs
PWM COMPARATOR SECTION					
Ramp Input Bias Current	I_{IB}	–	−0.5	−5.0	μA
Duty Cycle, Maximum Minimum	$DC_{(max)}$ $DC_{(min)}$	80 –	90 –	– 0	%
Zero Duty Cycle Threshold Voltage Pin 3(4) (Pin 7(9) = 0 V)	V_{th}	1.1	1.25	1.4	V
Propagation Delay (Ramp Input to Output, T_J = +25°C)	$t_{PLH(in/out)}$	–	60	100	ns
SOFT–START SECTION					
Charge Current ($V_{Soft–Start}$ = 0.5 V)	I_{chg}	3.0	9.0	20	μA
Discharge Current ($V_{Soft–Start}$ = 1.5 V)	I_{dischg}	1.0	4.0	–	mA
CURRENT SENSE SECTION					
Input Bias Current (Pin 9(12) = 0 V to 4.0 V)	I_{IB}	–	–	15	μA
Current Limit Comparator Input Offset Voltage (Pin 11(14) = 1.1 V)	V_{IO}	–	–	45	mV
Current Limit Reference Input Common Mode Range (Pin 11(14))	V_{CMR}	1.0	–	1.25	V
Shutdown Comparator Threshold	V_{th}	1.25	1.40	1.55	V
Propagation Delay (Current Limit/Shutdown to Output, T_J = +25°C)	$t_{PLH(in/out)}$	–	50	80	ns
OUTPUT SECTION					
Output Voltage Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	 V_{OL} V_{OH} 	 – – 13 12	 0.25 1.2 13.5 13	 0.4 2.2 – –	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 0.5 mA)	$V_{OL(UVLO)}$	–	0.25	1.0	V
Output Leakage Current (V_C = 20 V)	I_L	–	100	500	μA
Output Voltage Rise Time (C_L = 1.0 nF, T_J = +25°C)	t_r	–	30	60	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = +25°C)	t_f	–	30	60	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start–Up Threshold (V_{CC} Increasing)	$V_{th(on)}$	8.8	9.2	9.6	V
UVLO Hysteresis Voltage (V_{CC} Decreasing After Turn–On)	V_H	0.4	0.8	1.2	V
TOTAL DEVICE					
Power Supply Current Start–Up (VCC = 8.0 V) Operating	I_{CC}	 – –	 0.5 20	 1.2 30	mA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34023 T_{high} = +70°C for MC34023
= −40°C for MC33023 = +105°C for MC33023

Figure 1. Timing Resistor versus Oscillator Frequency

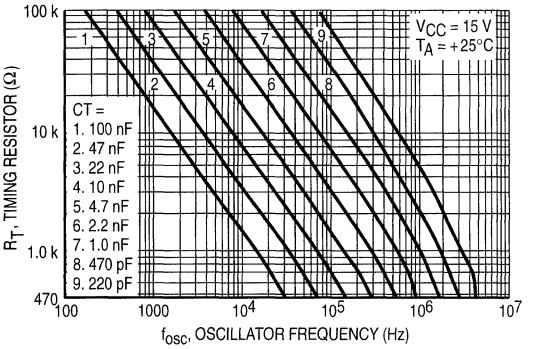


Figure 2. Oscillator Frequency versus Temperature

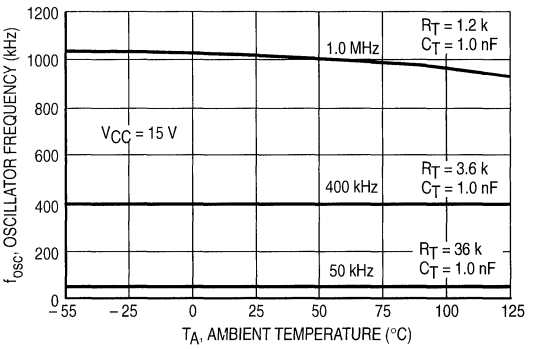


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

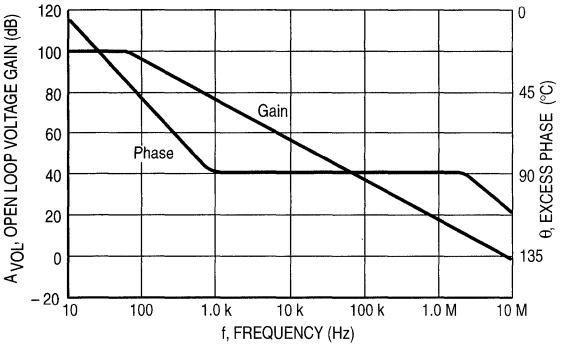


Figure 4. PWM Comparator Zero Duty Cycle Threshold Voltage versus Temperature

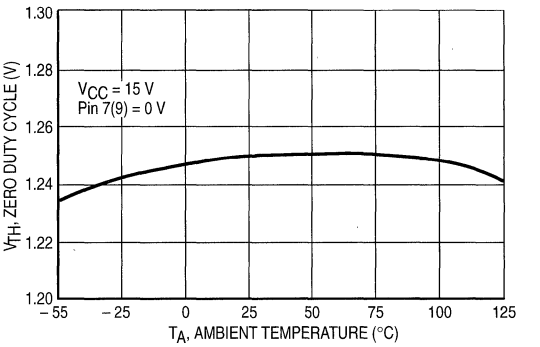


Figure 5. Error Amp Small Signal Transient Response

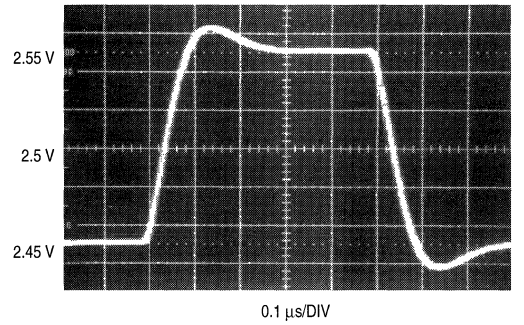


Figure 6. Error Amp Large Signal Transient Response

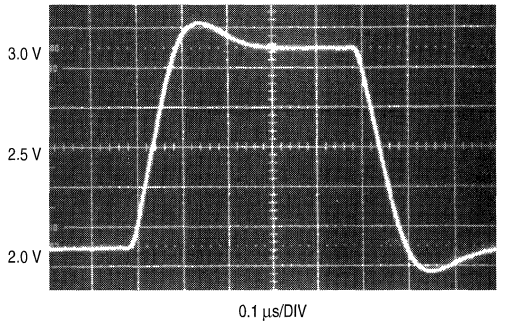


Figure 7. Reference Voltage Change versus Source Current

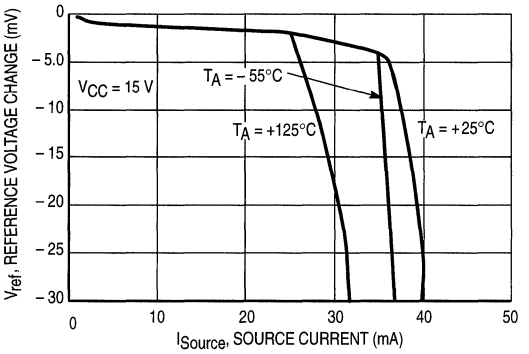


Figure 8. Reference Short Circuit Current versus Temperature

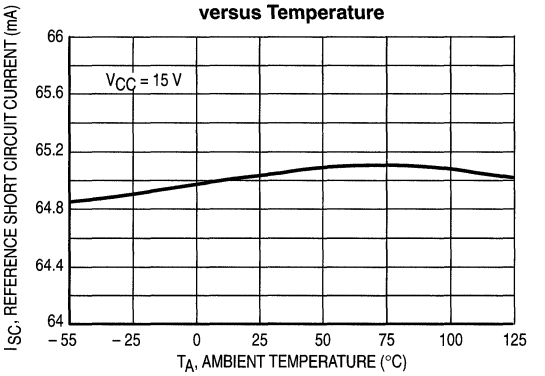
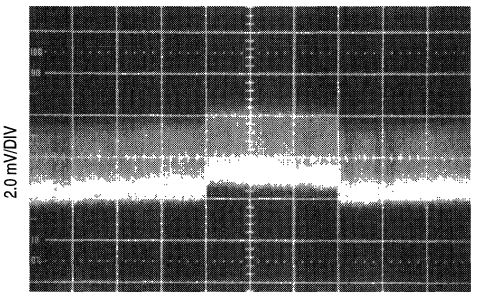
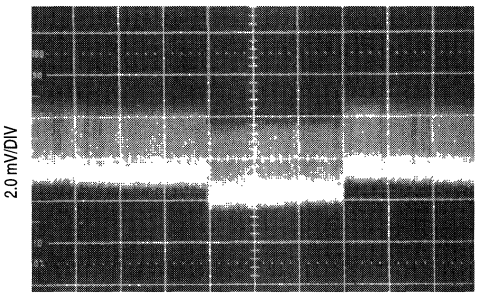


Figure 9. Reference Line Regulation



Vref LINE REGULATION 10 V to 24 V
(2.0 ms/DIV)

Figure 10. Reference Load Regulation



Vref LOAD REGULATION 1.0 mA to 10 mA
(2.0 ms/DIV)

Figure 11. Current Limit Comparator Input Offset Voltage versus Temperature

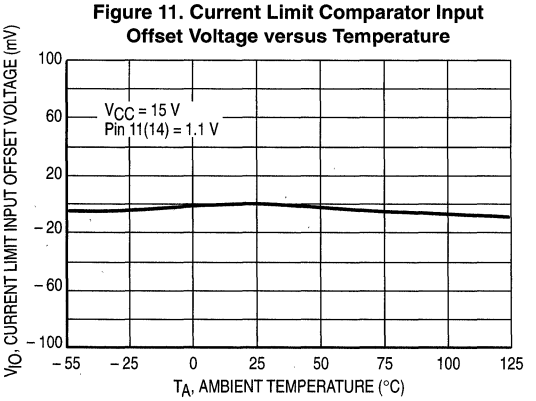


Figure 12. Shutdown Comparator Threshold Voltage versus Temperature

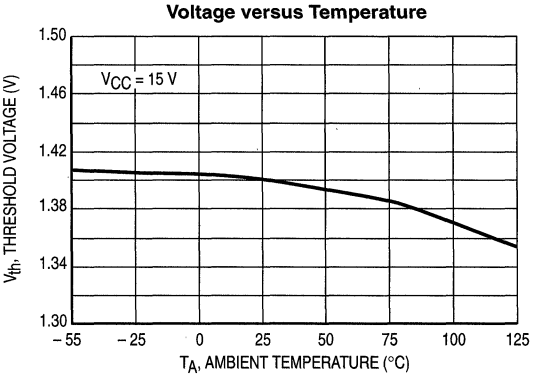


Figure 13. Soft–Start Charge Current versus Temperature

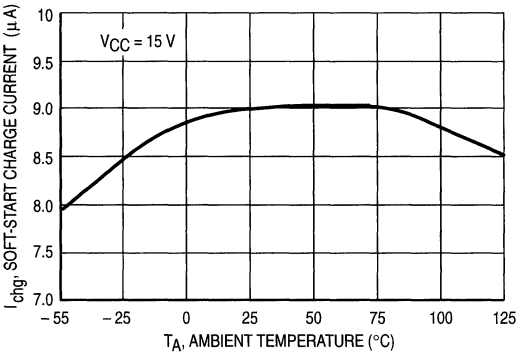


Figure 14. Output Saturation Voltage versus Load Current

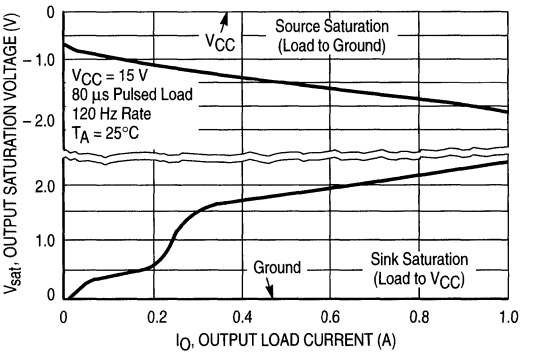
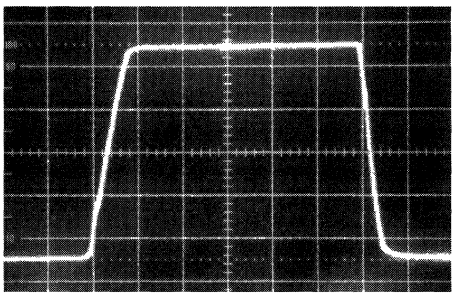
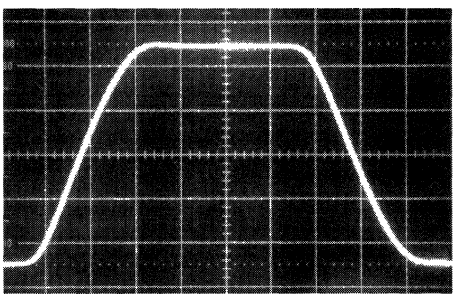


Figure 15. Drive Output Rise and Fall Time



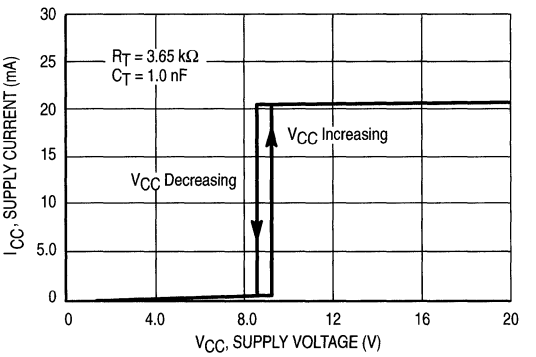
OUTPUT RISE & FALL TIME 1.0 nF LOAD
50 ns/DIV

Figure 16. Drive Output Rise and Fall Time



OUTPUT RISE & FALL TIME 10 nF LOAD
50 ns/DIV

Figure 17. Supply Voltage versus Supply Current



3

Figure 18. Representative Block Diagram

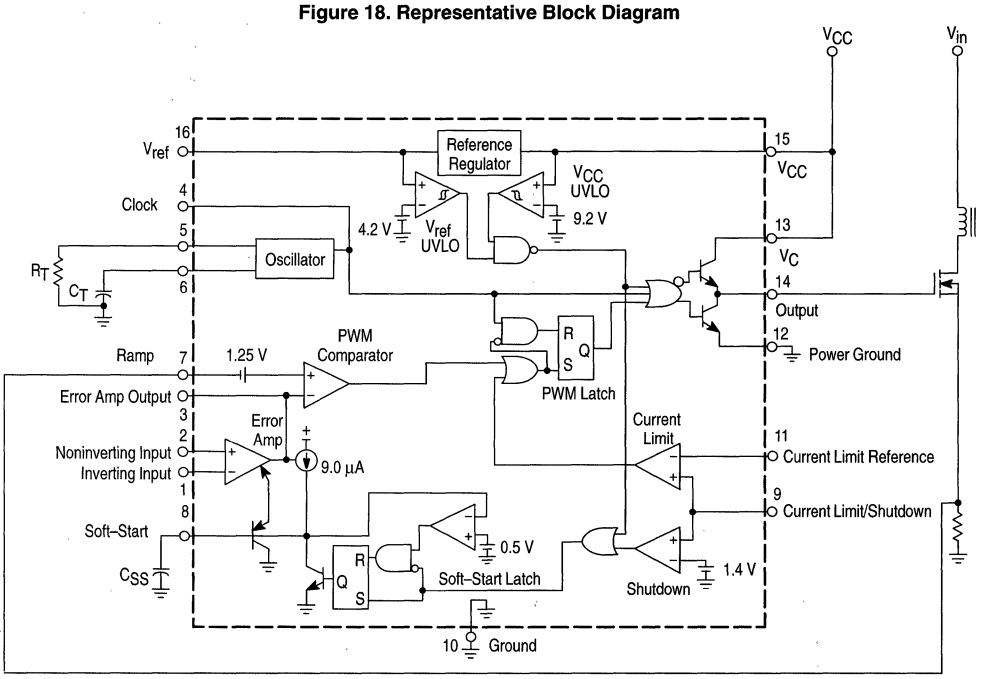
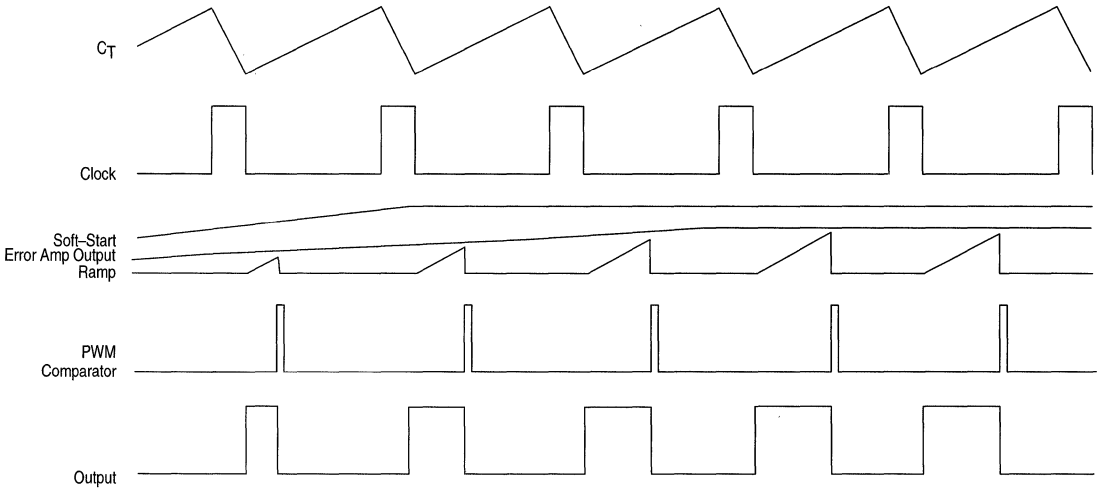


Figure 19. Current Limit Operating Waveforms



OPERATING DESCRIPTION

The MC33023 and MC34023 series are high speed, fixed frequency, single–ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off–Line and DC–to–DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 18.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. The R_T pin is set to a temperature compensated 3.0 V. By selecting the value of R_T, the charge current is set through a current mirror for the timing capacitor C_T. This charge current runs continuously through C_T. The discharge current is ratioed to be 10 times the charge current, which yields the maximum duty cycle of 90%. C_T is charged to 2.8 V and discharged to 1.0 V. During the discharge of C_T, the oscillator generates an internal blanking pulse that resets the PWM Latch and, inhibits the outputs. The threshold voltage on the oscillator comparator is trimmed to guarantee an oscillator accuracy of 5.0% at 25°C.

Additional dead time can be added by externally increasing the charge current to C_T as shown in Figure 23. This changes the charge to discharge ratio of C_T which is set internally to $I_{charge}/10\ I_{charge}$. The new charge to discharge ratio will be:

$$\% \text{ Deadtime} = \frac{I_{additional} + I_{charge}}{10\ (I_{charge})}$$

A bidirectional clock pin is provided for synchronization or for master/slave operation. As a master, the clock pin provides a positive output pulse during the discharge of C_T. As a slave, the clock pin is an input that resets the PWM latch and blanks the drive output, but does not discharge C_T. Therefore, the oscillator is not synchronized by driving the clock pin alone. Figures 27, 28 and 29 provide suggested synchronization.

Error Amplifier

A fully compensated Error Amplifier is provided. It features a typical DC voltage gain of 95 dB and a gain bandwidth product of 8.3 MHz with 75 degrees of phase margin (Figure 3). Typical application circuits will have the noninverting input tied to the reference. The inverting input will typically be connected to a feedback voltage generated from the output of the switching power supply. Both inputs have a common mode voltage (V_{CM}) input range of 1.5 V to 5.5 V. The Error Amplifier Output is provided for external loop compensation.

Soft–Start Latch

Soft–Start is accomplished in conjunction with an external capacitor. The Soft–Start capacitor is charged by an internal 9.0 μA current source. This capacitor clamps the output of the error amplifier to less than its normal output voltage, thus limiting the duty cycle. The time it takes for a capacitor to reach full charge is given by:

$$t \approx (4.5 \bullet 10^5)\ C_{Soft\text{-}Start}$$

A Soft–Start latch is incorporated to prevent erratic operation of this circuitry. Two conditions can cause the Soft–Start circuit to latch so that the Soft–Start capacitor stays discharged. The first condition is activation of an undervoltage lockout of either V_{CC} or V_{ref}. The second condition is when current sense input exceeds 1.4 V. Since this latch is "set dominant", it cannot be reset until either of these signals is removed and, the voltage at $C_{Soft\text{–}Start}$ is less than 0.5 V.

PWM Comparator and Latch

A PWM circuit typically compares an error voltage with a ramp signal. The outcome of this comparison determines the state of the output. In voltage mode operation the ramp signal is the voltage ramp of the timing capacitor. In current mode operation the ramp signal is the voltage ramp induced in a current sensing element. The ramp input of the PWM comparator is pinned out so that the user can decide which mode of operation best suits the application requirements. The ramp input has a 1.25 V offset such that whenever the voltage at this pin exceeds the error amplifier output voltage minus 1.25 V, the PWM comparator will cause the PWM latch to set, disabling the outputs. Once the PWM latch is set, only a blanking pulse by the oscillator can reset it, thus initiating the next cycle.

Current Limiting and Shutdown

A pin is provided to perform current limiting and shutdown operations. Two comparators are connected to the input of this pin. The reference voltage for the current limit comparator is not set internally. A pin is provided so the user can set the voltage. When the voltage at the current limit input pin exceeds the externally set voltage, the PWM latch is set, disabling the output. In this way cycle–by–cycle current limiting is accomplished. If a current limit resistor is used in series with the power devices, the value of the resistor is found by:

$$R_{Sense} = \frac{I_{Limit\ Reference\ Voltage}}{I_{pk\ (switch)}}$$

If the voltage at this pin exceeds 1.4 V, the second comparator is activated. This comparator sets a latch which, in turn, causes the soft start capacitor to be discharged. In this way a "hiccup" mode of recovery is possible in the case of output short circuits. If a current limit resistor is used in series with the output devices, the peak current at which the controller will enter a "hiccup" mode is given by:

$$I_{shutdown} = \frac{1.4\ V}{R_{Sense}}$$

Undervoltage Lockout

There are two undervoltage lockout circuits within the IC. The first senses V_{CC} and the second V_{ref}. During power–up, V_{CC} must exceed 9.2 V and V_{ref} must exceed 4.2 V before the outputs can be enabled and the Soft–Start latch released. If V_{CC} falls below 8.4 V or V_{ref} falls below 3.6 V, the outputs are disabled and the Soft–Start latch is activated. When the UVLO is active, the part is in a low current standby mode allowing the IC to have an off–line bootstrap start–up circuit. Typical start–up current is 500 μA.

Output

The MC34023 has a high current totem pole output specifically designed for direct drive of power MOSFETs. It is capable of up to ± 2.0 A peak drive current with a typical rise and fall time of 30 ns driving a 1.0 nF load.

Separate pins for V_C and Power Ground are provided. With proper implementation, a significant reduction of switching transient noise imposed on the control circuitry is possible. The separate V_C supply input also allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}.

Reference

A 5.1 V bandgap reference is pinned out and is trimmed to an initial accuracy of ±1.0% at 25°C. This reference has short circuit protection and can source in excess of 10 mA for powering additional control system circuitry.

Design Considerations

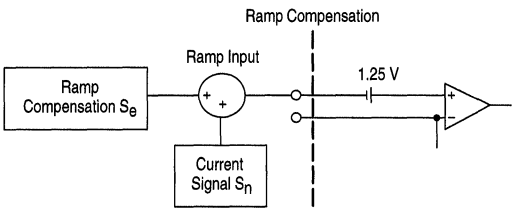
Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. With high frequency, high power, switching power supplies it is imperative to have separate current loops for the signal paths and for the power paths. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Shown in Figure 35 is a printed circuit layout of the application circuit. Note how the power and ground traces are run. All bypass capacitors and snubbers should be connected as close as possible to the specific part in question. The PC board lead lengths must be less than 0.5 inches for effective bypassing for snubbing.

Instabilities

In current mode control, an instability can be encountered at any given duty cycle. The instability is caused by the current feedback loop. It has been shown that the instability is caused by a double pole at half the switching frequency. If an external ramp (S_e) is added to the on–time ramp (S_n) of the current–sense waveform, stability can be achieved.

One must be careful not to add too much ramp compensation. If too much is added the system will start to perform like a voltage mode regulator. All benefits of current mode control will be lost. Figure 25 is an example of one way in which external ramp compensation can be implemented.

Figure 20. Ramp Compensation



A simple equation can be used to calculate the amount of external ramp slope necessary to add that will achieve stability in the current loop. For the following equations, the calculated values for the application circuit in Figure 34 are also shown.

$$S_e = \frac{V_O}{L}\left(\frac{N_S}{N_P}\right)(R_S)A_i$$

where: V_O = DC output voltage
N_P, N_S = number of power transformer primary or secondary turns
A_i = gain of the current sense network (see Figures 23 and 24)
L = output inductor
R_S = current sense resistance

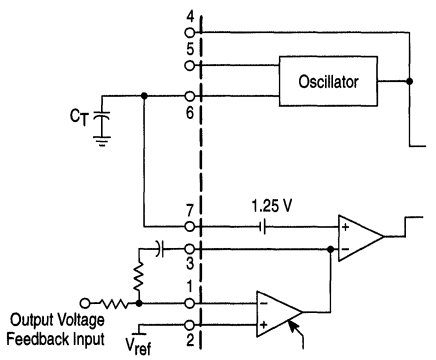
For the application circuit: $S_e = \frac{5}{1.8\ \mu}\left(\frac{2}{8}\right)(0.3)(0.55)$

$= 0.115$ V/ms

PIN FUNCTION DESCRIPTION

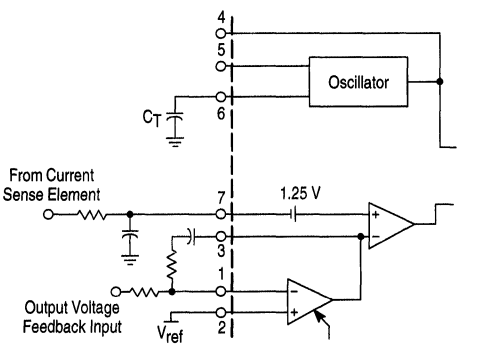
Pin DIP/SOIC	Function	Description
1	Error Amp Inverting Input	This pin is usually used for feedback from the output of the power supply.
2	Error Amp Noninverting Input	This pin is used to provide a reference in which an error signal can be produced on the output of the error amp. Usually this is connected to V_{ref}, however an external reference can also be used.
3	Error Amp Output	This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter.
4	Clock	This is a bidirectional pin used for synchronization.
5	R_T	The value of R_T sets the charge current through timing Capacitor, C_T.
6	C_T	In conjunction with R_T, the timing Capacitor sets the switching frequency.
7	Ramp Input	For voltage mode operation this pin is connected to C_T. For current mode operation this pin is connected through a filter to the current sensing element.
8	Soft–Start	A capacitor at this pin sets the Soft–Start time.
9	Current Limit/ Shutdown	This pin has two functions. First, it provides cycle–by–cycle current limiting. Second, if the current is excessive, this pin will reinitiate a Soft–Start cycle.
10	Ground	This pin is the ground for the control circuitry.
11	Current Limit Reference Input	This pin voltage sets the threshold for cycle–by–cycle current limiting.
12	Power Ground	This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
13	V_C	This is a separate power source connection for the outputs that is connected back to the power source input. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
14	Output	This is a high current totem pole output.
15	V_{CC}	This pin is the positive supply of the control IC.
16	V_{ref}	This is a 5.1 V reference. It is usually connected to the noninverting input of the error amplifier.

Figure 21. Voltage Mode Operation



In voltage mode operation, the control range on the output of the Error Amplifier from 0% to 90% duty cycle is from 2.25 V to 4.05 V.

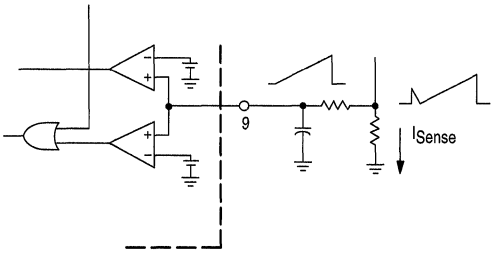
Figure 22. Current Mode Operation



In current mode control, an RC filter should be placed at the ramp input to filter the leading edge spike caused by turn–on of a power MOSFET.

3

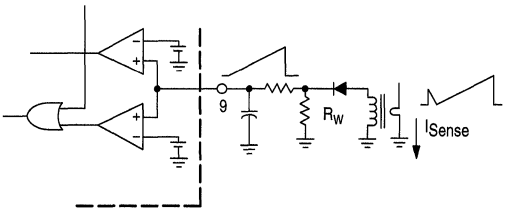
Figure 23. Resistive Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. If a transformer is used, the gain can be calculated by:

$$A_i = \frac{R_{Sense}}{\text{turns ratio}}$$

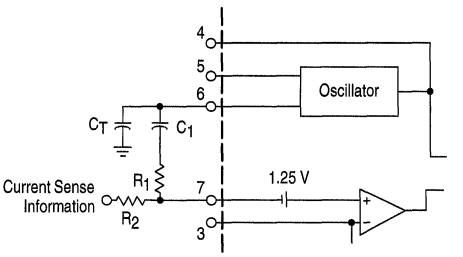
Figure 24. Primary Side Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. The gain can be calculated by:

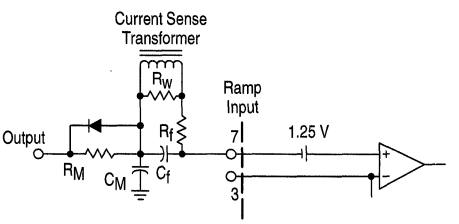
$$A_i = \frac{R_w}{\text{turns ratio}}$$

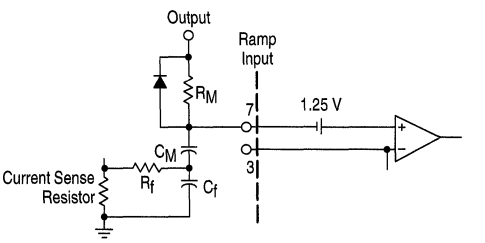
Figure 25A. Slope Compensation (Noise Sensitive)



This method of slope compensation is easy to implement, however, it is noise sensitive. Capacitor C_1 provides AC coupling. The oscillator signal is added to the current signal by a voltage divider consisting of resistors R_1 and R_2.

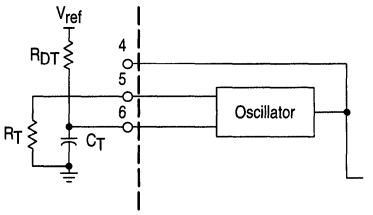
Figure 25B. Slope Compensation (Noise Immune)





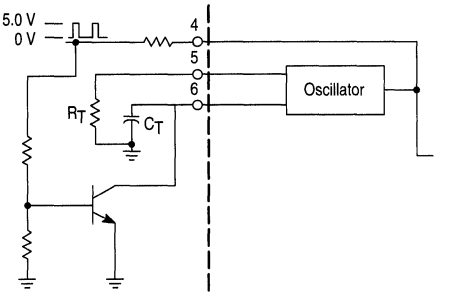
When only one output is used, this method of slope compensation can be used and it is relatively noise immune. Resistor R_M and capacitor C_M provide the added slope necessary. By choosing R_M and C_M with a larger time constant than the switching frequency, you can assume that its charge is linear. First choose C_M, then R_M can be adjusted to achieve the required slope. The diode provides a reset pulse at the ramp input at the end of every cycle. The charge current I_M can be calculated by $I_M = C_M S_e$. Then R_M can be calculated by $R_M = V_{CC}/I_M$.

Figure 26. Dead Time Addition



Additional dead time can be added by the addition of a dead time resistor from V_{ref} to C_T. See text on Oscillator section for more information.

Figure 27. External Clock Synchronization



The sync pulse fed into the clock pin must be at least 3.9 V. R_T and C_T need to be set 10% slower than the sync frequency. This circuit is also used in Voltage Mode operation for master/slave operation. The clock signal would be coming from the master which is set at the desired operating frequency, while the slave is set 10% slower.

Figure 28. Current Mode Master/Slave Operation Over Short Distances

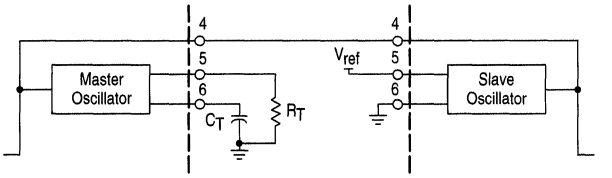
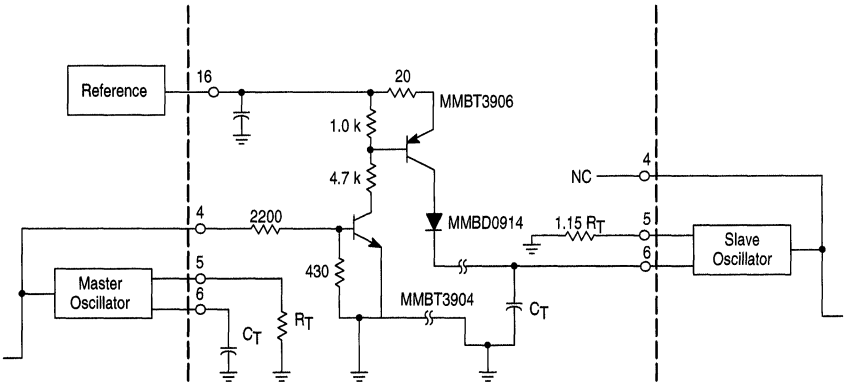
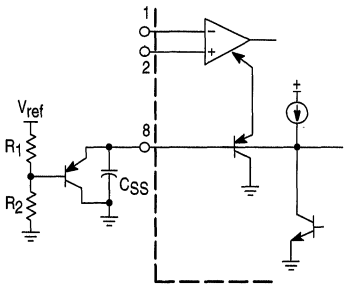


Figure 29. Synchronization Over Long Distances



3

Figure 30. Buffered Maximum Clamp Level

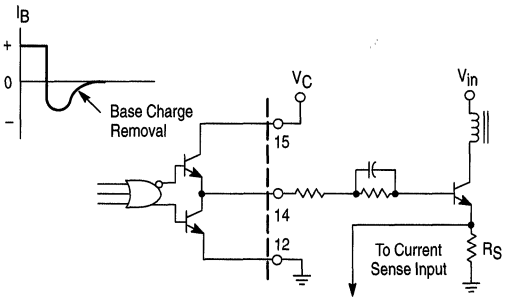


In voltage mode operation, the maximum duty cycle can be clamped. By the addition of a PNP transistor to buffer the clamp voltage, the Soft–Start current is not affected by R_1.

The new equation for Soft–Start is $t \approx \frac{V_{clamp} + 0.6}{9.0\ \mu A} (C_{SS})$

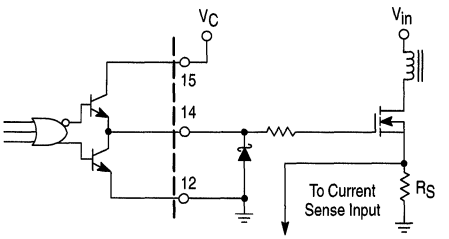
In current mode operation, this circuit will limit the maximum voltage allowed at the ramp input to end a cycle.

Figure 31. Bipolar Transistor Drive



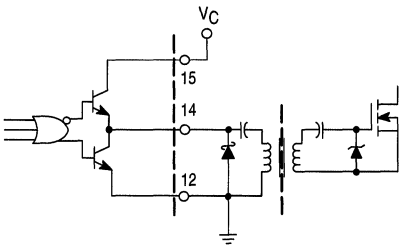
The totem pole output can furnish negative base current for enhanced transistor turn–off, with the addition of the capacitor in series with the base.

Figure 32. MOSFET Parasitic Oscillations



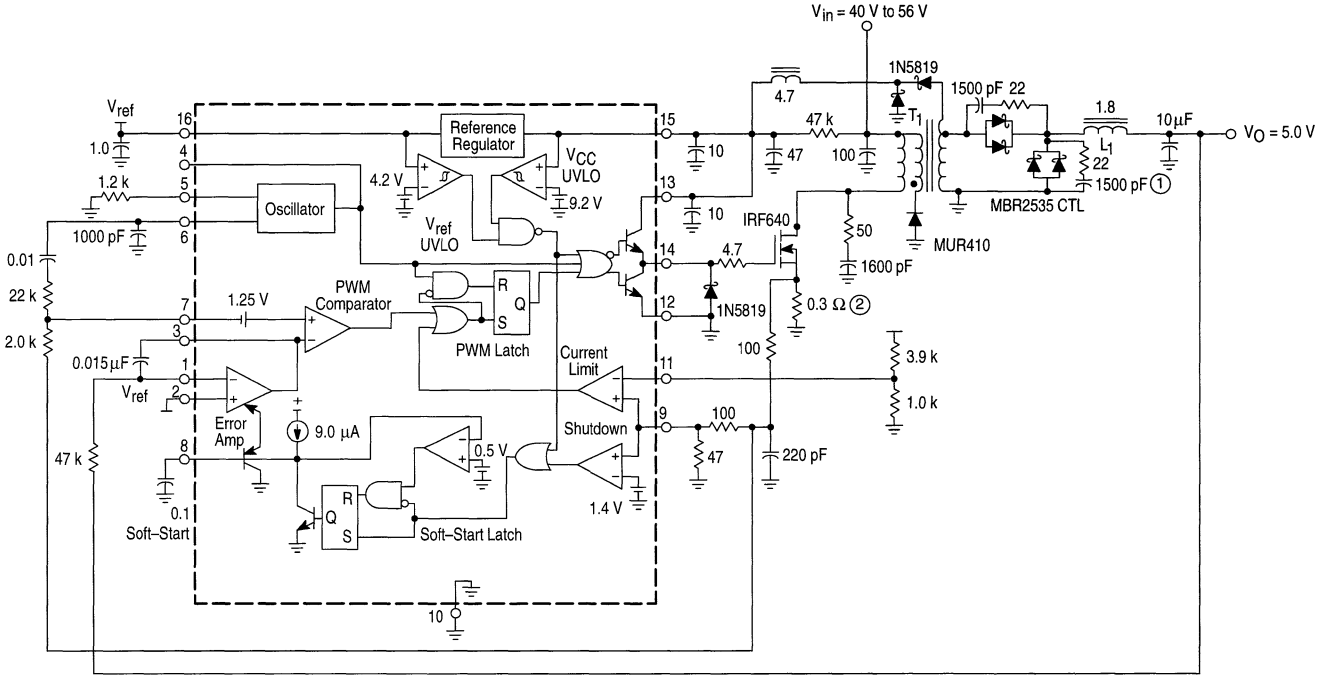
A series gate resistor may be needed to dampen high frequency parasitic oscillation caused by the MOSFET's input capacitance and any series wiring inductance in the gate–source circuit. The series resistor will also decrease the MOSFET switching speed. A Schottky diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground. The Schottky diode also prevents substrate injection when the output pin is driven below ground.

Figure 33. Isolated MOSFET Drive



The totem pole output can easily drive pulse transformers. A Schottky diode is recommended when driving inductive loads at high frequencies. The diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 34. Application Circuit



T_1 – Primary: 8 turns #48 AWG (1300 strands litz wire)
Secondary: 2 turns 0.003" (2 layers) copper foil
Bootstrap: 1 turn added to secondary #36 AWG
Core: Philips 3F3, part #4312 020 4124
Bobbin: Philips part #4322 021 3525
Coilcraft P3269–A

L_1 – 2 turns #48 AWG (1300 strands litz wire)
Core: Philips 3F3, part #EP10–3F3
Bobbin: Philips part #EP10PCB1–8
L = 1.8 µH
Coilcraft P3270–A

Heatsinks – Power FET: AAVID Heatsink #533902B02552 with clip
Output Rectifiers: AAVID Heatsink #533402B02552 with clip

Insulators – All power devices are insulated with Berquist Sil–Pad 150

① – 10(1.0 µF) ceramic capacitors in parallel

② – 5(1.5 Ω) resistors in parallel

Test	Condition	Result
Line Regulation	V_{in} = 40 V to 56 V, I_O = 7.5A	14 mV = ±0.275%
Load Regulation	V_{in} = 48 V, I_O = 4.0 A to 7.5 A	54 mV = ±1.0%
Output Ripple	V_{in} = 48 V, I_O = 7.5 A	10 mVp–p
Efficiency	V_{in} = 48 V, I_O = 7.5 A	69.8%

3

Figure 35. PC Board With Components

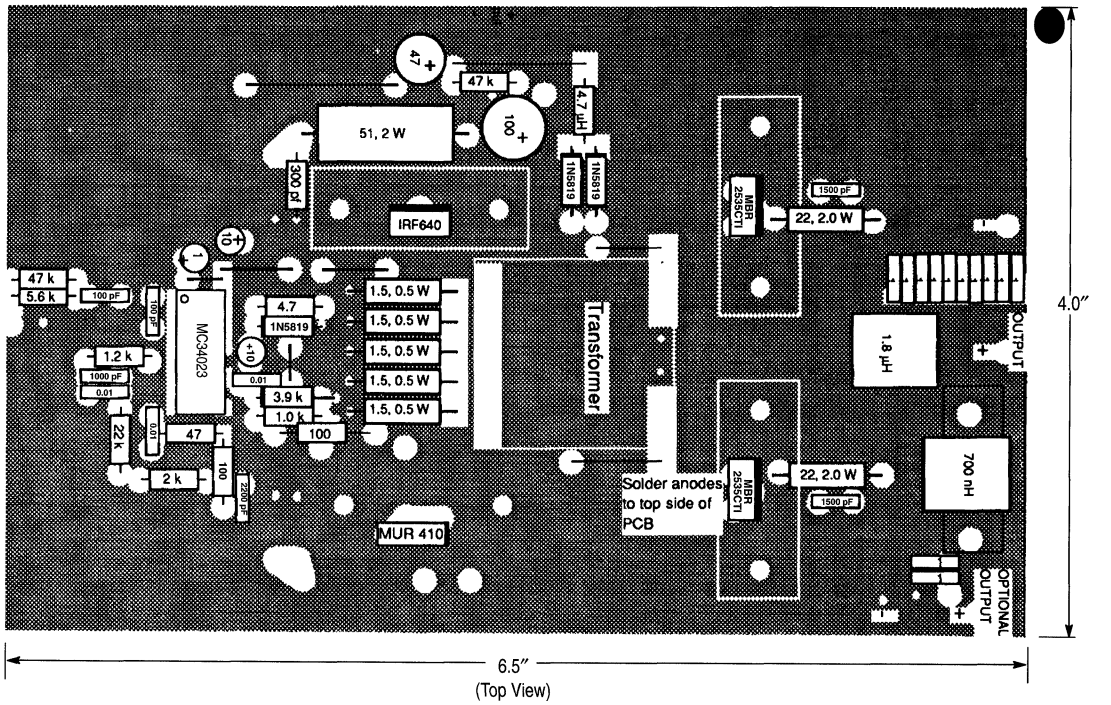
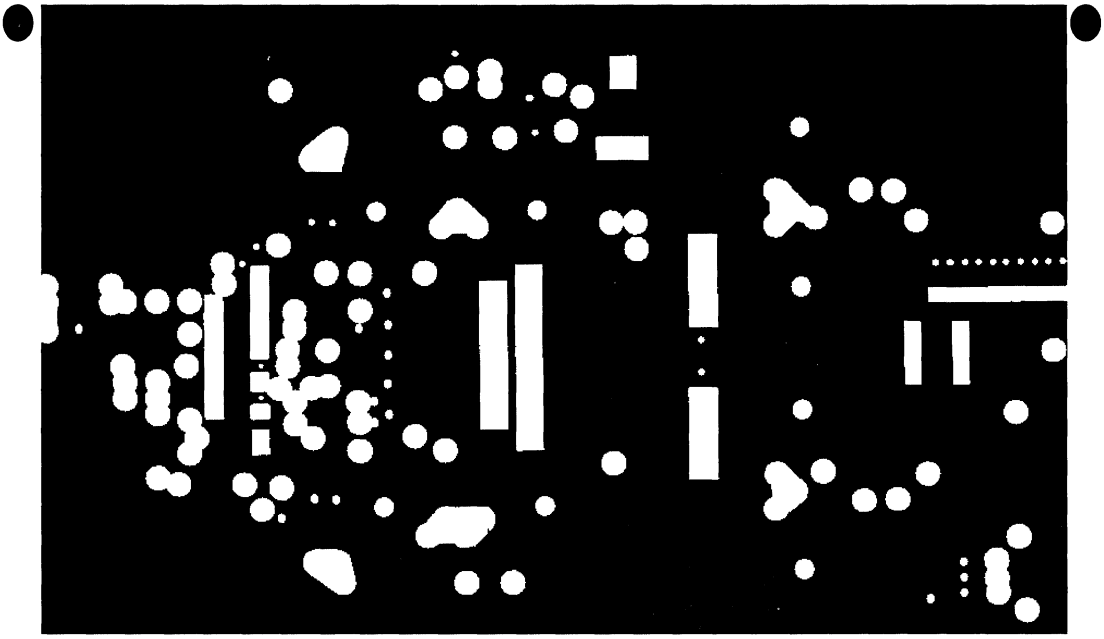
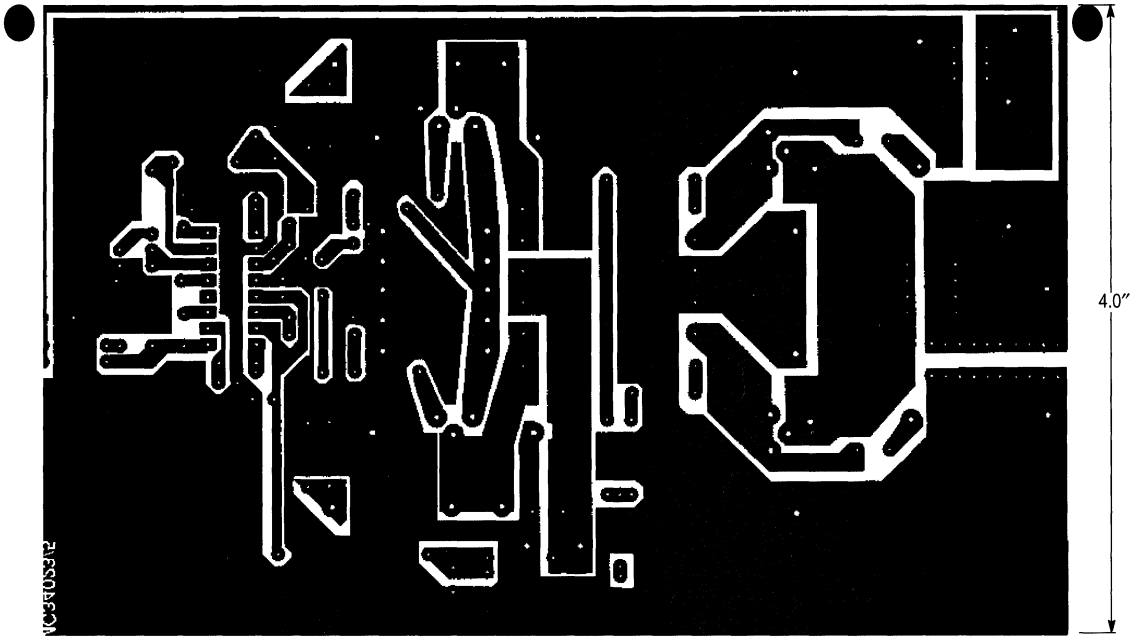


Figure 36. PC Board Without Components



(Top View)



(Bottom View)

MC34025
MC33025

High Speed Double-Ended PWM Controller

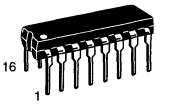
3

The MC34025 series are high speed, fixed frequency, double–ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off–Line and DC–to–DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, a wide bandwidth error amplifier, a high speed current sensing comparator, steering flip–flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

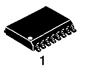
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, and a latch for single pulse metering.

The flexibility of this series allows it to be easily configured for either current mode or voltage mode control.

- 50 ns Propagation Delay to Outputs
- Dual High Current Totem Pole Outputs
- Wide Bandwidth Error Amplifier
- Fully–Latched Logic with Double Pulse Suppression
- Latching PWM for Cycle–By–Cycle Current Limiting
- Soft–Start Control with Latched Overcurrent Reset
- Input Undervoltage Lockout with Hysteresis
- Low Start–Up Current (500 μA Typ)
- Internally Trimmed Reference with Undervoltage Lockout
- 90% Maximum Duty Cycle (Externally Adjustable)
- Precision Trimmed Oscillator
- Voltage or Current Mode Operation to 1.0 MHz
- Functionally Similar to the UC3825

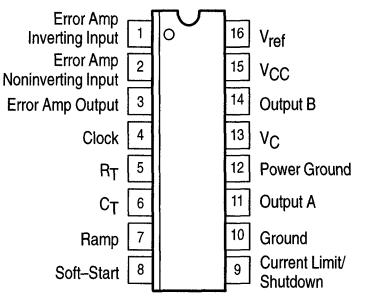


P SUFFIX
PLASTIC PACKAGE
CASE 648



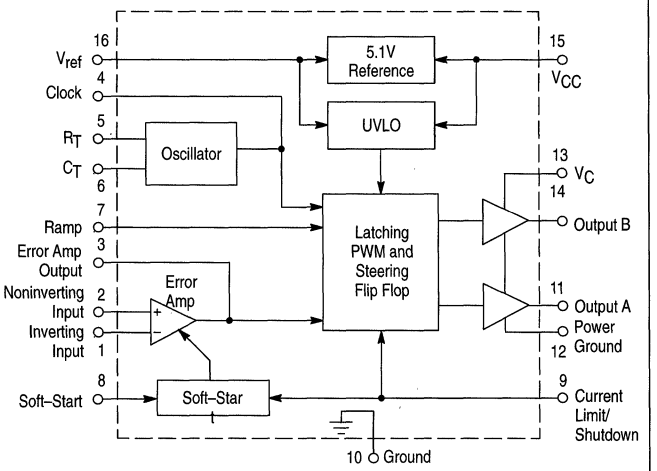
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

PIN CONNECTIONS



(Top View)

Simplified Application



This device contains 227 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33025DW	$T_A = -40°$ to $+105°C$	SO–16L
MC33025P		Plastic DIP
MC34025DW	$T_A = 0°$ to $+70°C$	SO–16L
MC34025P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	30	V
Output Driver Supply Voltage	V_C	20	V
Output Current, Source or Sink (Note 1) DC Pulsed (0.5 μs)	I_O	 0.5 2.0	A
Current Sense, Soft–Start, Ramp, and Error Amp Inputs	V_{in}	−0.3 to +7.0	V
Error Amp Output and Soft–Start Sink Current	I_O	10	mA
Clock and R_T Output Current	I_{CO}	5.0	mA
Power Dissipation and Thermal Characteristics SO–16 Package (Case 751G) Maximum Power Dissipation @ T_A = +25°C Thermal Resistance, Junction–to–Air DIP Package (Case 648) Maximum Power Dissipation @ T_A = +25°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 2) MC34025 MC33025	T_A	 0 to +70 −40 to +105	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = +25°C)	V_{ref}	5.05	5.1	5.15	V
Line Regulation (V_{CC} = 10 V to 30 V)	Reg_{line}	–	2.0	15	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	2.0	15	mV
Temperature Stability	T_S	–	0.2	–	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.95	–	5.25	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = +25°C)	V_n	–	50	–	μV
Long Term Stability (T_A = +125°C for 1000 Hours)	S	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	–30	–65	–100	mA
OSCILLATOR SECTION					
Frequency T_J = +25°C Line (V_{CC} = 10 V to 30 V) and Temperature (T_A = T_{low} to T_{high})	f_{osc}	 380 370	 400 400	 420 430	kHz
Frequency Change with Voltage (V_{CC} = 10 V to 30 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	%
Frequency Change with Temperature (T_A = T_{low} to T_{high})	$\Delta f_{osc}/\Delta T$	–	2.0	–	%
Sawtooth Peak Voltage	V_P	2.6	2.8	3.0	V
Sawtooth Valley Voltage	V_V	0.7	1.0	1.25	V
Clock Output Voltage High State Low State	 V_{OH} V_{OL}	 3.9 –	 4.5 2.3	 – 2.9	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34025 T_{high} = +70°C for MC34025
= – 40°C for MC33025 = +105°C for MC33025

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage	V_{IO}	–	–	15	mV
Input Bias Current	I_{IB}	–	0.6	3.0	μA
Input Offset Current	I_{IO}	–	0.1	1.0	μA
Open–Loop Voltage Gain (V_O = 1.0 V to 4.0 V)	A_{VOL}	60	95	–	dB
Gain Bandwidth Product (T_J = +25°C)	GBW	4.0	8.3	–	MHz
Common Mode Rejection Ratio (V_{CM} = 1.5 V to 5.5 V)	CMRR	75	95	–	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 30 V)	PSRR	85	110	–	dB
Output Current, Source (V_O = 4.0 V) Sink (V_O = 1.0 V)	I_{Source} I_{Sink}	0.5 1.0	3.0 3.6	– –	mA
Output Voltage Swing, High State (I_O = – 0.5 mA) Low State (I_O = 1.0 mA)	V_{OH} V_{OL}	4.5 0	4.75 0.4	5.0 1.0	V
Slew Rate	SR	6.0	12	–	V/μs
PWM COMPARATOR SECTION					
Ramp Input Bias Current	I_{IB}	–	–0.5	–5.0	μA
Duty Cycle, Maximum Minimum	$DC_{(max)}$ $DC_{(min)}$	80 –	90 –	– 0	%
Zero Duty Cycle Threshold Voltage Pin 3(4) (Pin 7(9) = 0 V)	V_{th}	1.1	1.25	1.4	V
Propagation Delay (Ramp Input to Output, T_J = +25°C)	$t_{PLH(in/out)}$	–	60	100	ns
SIFT–START SECTION					
Charge Current ($V_{Soft–Start}$ = 0.5 V)	I_{chg}	3.0	9.0	20	μA
Discharge Current ($V_{Soft–Start}$ = 1.5 V)	I_{dischg}	1.0	4.0	–	mA
CURRENT SENSE SECTION					
Input Bias Current (Pin 9(12) = 0 V to 4.0 V)	I_{IB}	–	–	15	μA
Current Limit Comparator Threshold Shutdown Comparator Threshold	V_{th} V_{th}	0.9 1.25	1.0 1.40	1.10 1.55	V
Propagation Delay (Current Limit/Shutdown to Output, T_J = +25°C)	$t_{PLH(in/out)}$	–	50	80	ns
OUTPUT SECTION					
Output Voltage					V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.25	0.4	
(I_{Sink} = 200 mA)		–	1.2	2.2	
High State (I_{Source} = 20 mA)	V_{OH}	13	13.5	–	
(I_{Source} = 200 mA)		12	13	–	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 0.5 mA)	$V_{OL(UVLO)}$	–	0.25	1.0	V
Output Leakage Current (V_C = 20 V)	I_L	–	100	500	μA
Output Voltage Rise Time (C_L = 1.0 nF, T_J = +25°C)	t_r	–	30	60	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = +25°C)	t_f	–	30	60	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start–Up Threshold (V_{CC} Increasing)	$V_{th(on)}$	8.8	9.2	9.6	V
UVLO Hysteresis Voltage (V_{CC} Decreasing After Turn–On)	V_H	0.4	0.8	1.2	V
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Start–Up (V_{CC} = 8.0 V)		–	0.5	1.2	
Operating		–	25	35	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34025 T_{high} = +70°C for MC34025
= – 40°C for MC33025 = +105°C for MC33025

Figure 1. Timing Resistor versus Oscillator Frequency

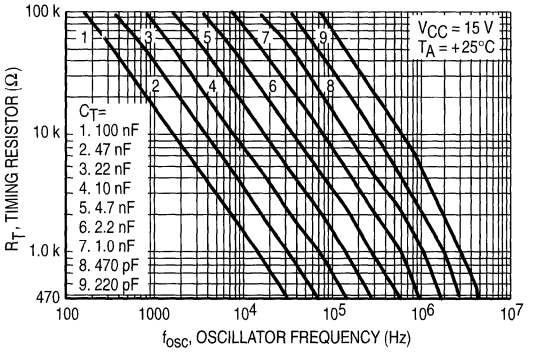


Figure 2. Oscillator Frequency versus Temperature

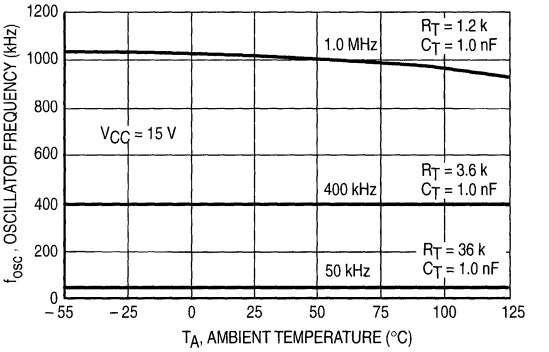


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

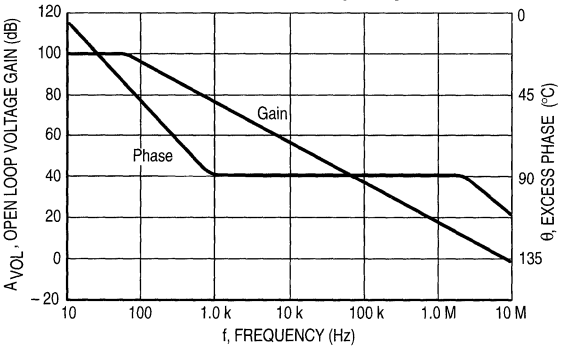


Figure 4. PWM Comparator Zero Duty Cycle Threshold Voltage versus Temperature

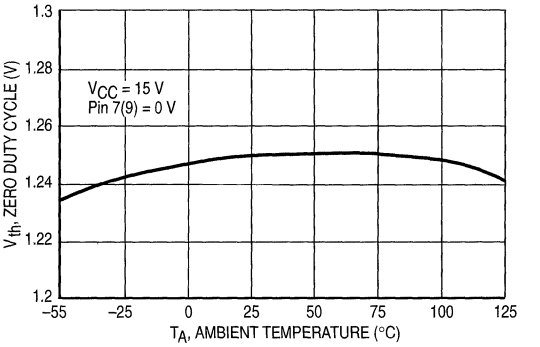


Figure 5. Error Amp Small Signal Transient Response

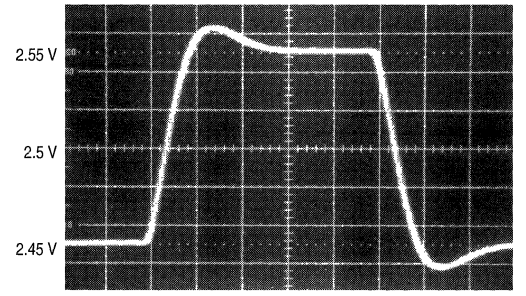


Figure 6. Error Amp Large Signal Transient Response

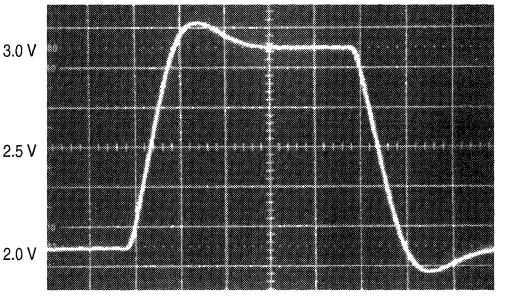


Figure 7. Reference Voltage Change versus Source Current

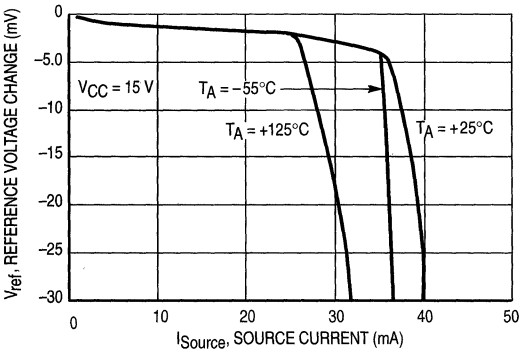


Figure 8. Reference Short Circuit Current versus Temperature

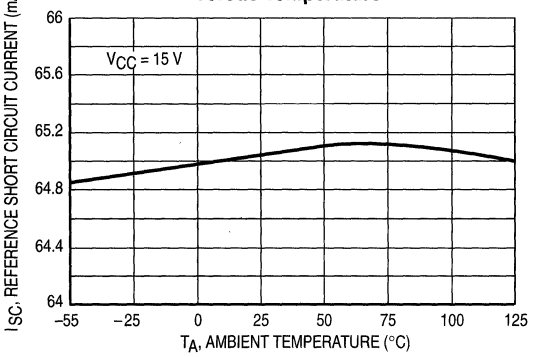
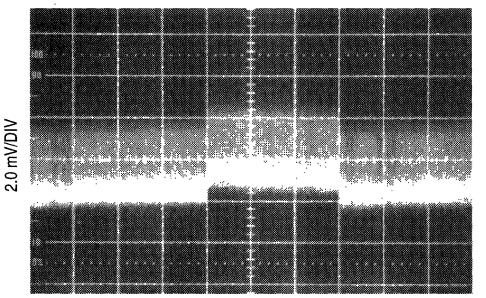
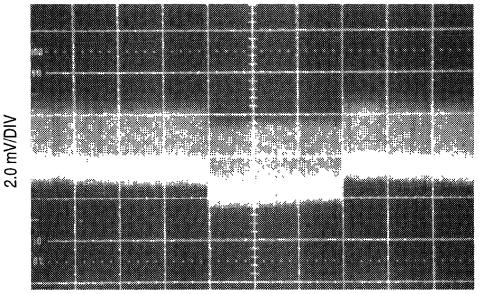


Figure 9. Reference Line Regulation



V_{ref} LINE REGULATION 10 V – 24 V
2.0 ms/DIV

Figure 10. Reference Load Regulation



V_{ref} LINE REGULATION 1.0 mA – 10 mA
2.0 ms/DIV

Figure 11. Current Limit Comparator Threshold Change versus Temperature

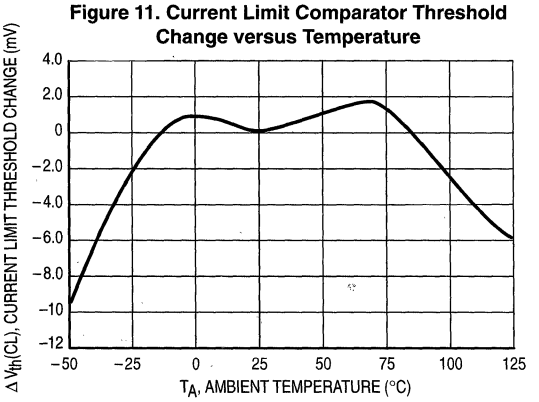


Figure 12. Shutdown Comparator Threshold Voltage versus Temperature

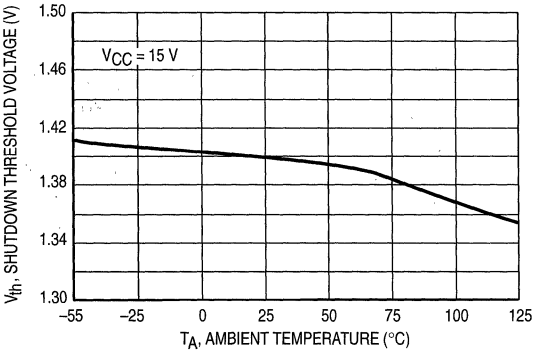


Figure 13. Soft–Start Charge Current versus Temperature

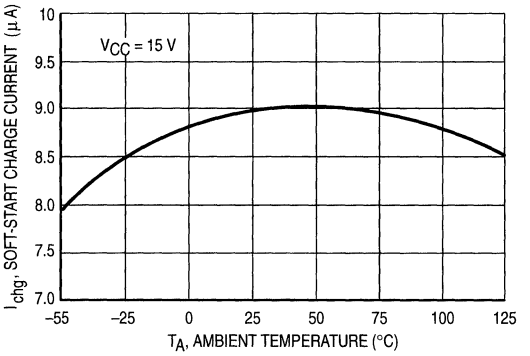


Figure 14. Output Saturation Voltage versus Load Current

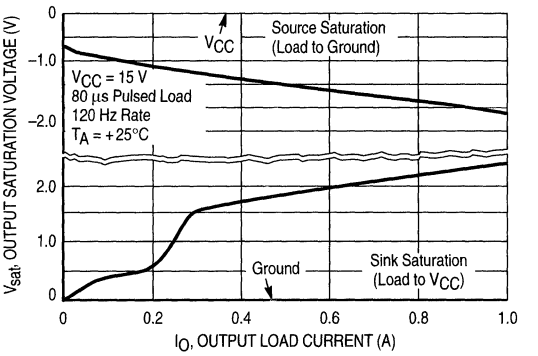
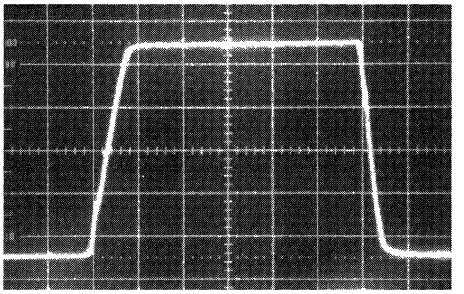
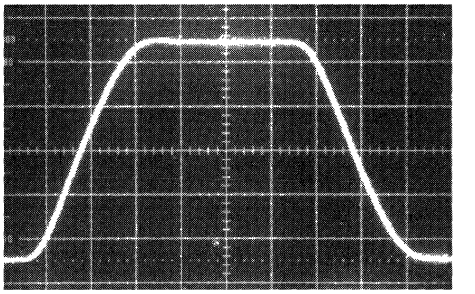


Figure 15. Drive Output Rise and Fall Time



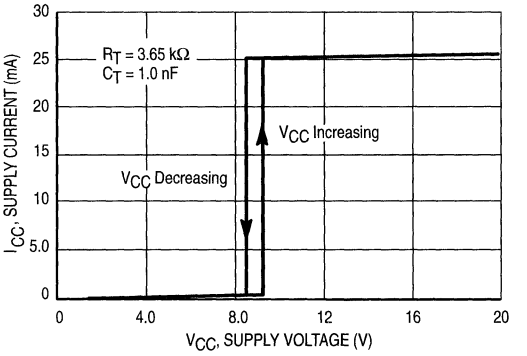
OUTPUT RISE & FALL TIME 1.0 nF LOAD
50 ns/DIV

Figure 16. Drive Output Rise and Fall Time



OUTPUT RISE & FALL TIME 10.0 nF LOAD
50 ns/DIV

Figure 17. Supply Voltage versus Supply Current



3

Figure 18. Representative Block Diagram

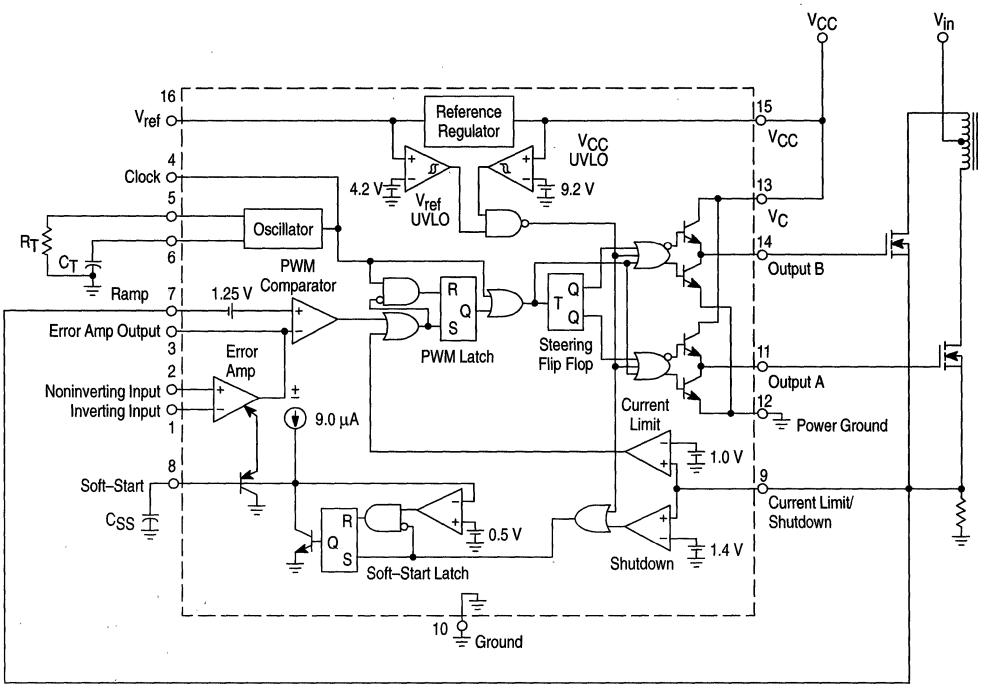
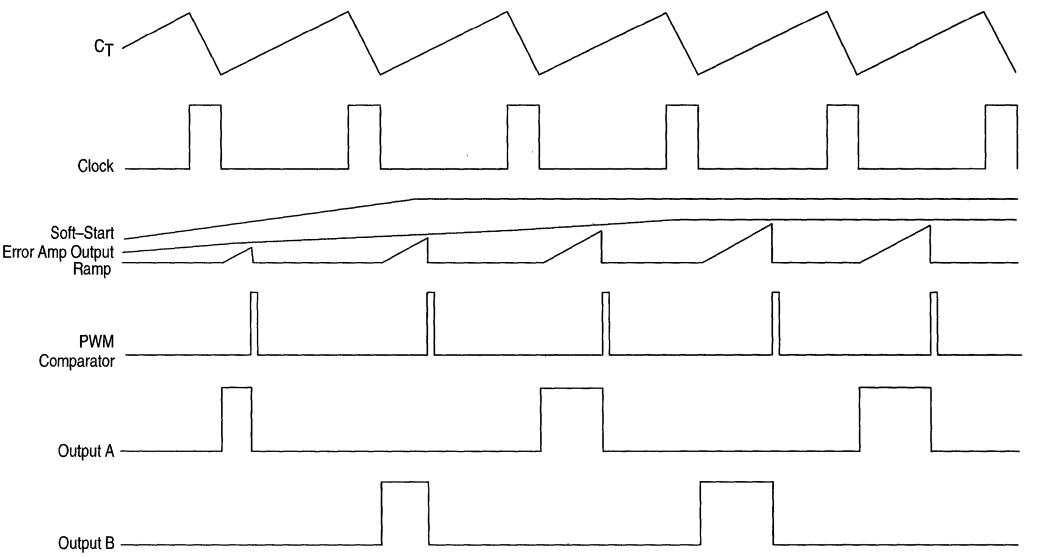


Figure 19. Current Limit Operating Waveforms



OPERATING DESCRIPTION

The MC33025 and MC34025 series are high speed, fixed frequency, double–ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off–Line and DC–to–DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 18.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. The R_T pin is set to a temperature compensated 3.0 V. By selecting the value of R_T, the charge current is set through a current mirror for the timing capacitor C_T. This charge current runs continuously through C_T. The discharge current is ratioed to be 10 times the charge current, which yields the maximum duty cycle of 90%. C_T is charged to 2.8 V and discharged to 1.0 V. During the discharge of C_T, the oscillator generates an internal blanking pulse that resets the PWM Latch, inhibits the outputs, and toggles the steering flip–flop. The threshold voltages on the oscillator comparator is trimmed to guarantee an oscillator accuracy of 5.0% at 25°C.

Additional dead time can be added by externally increasing the charge current to C_T as shown in Figure 23. This changes the charge to discharge ratio of C_T which is set internally to $I_{charge}/10\ I_{charge}$. The new charge to discharge ratio will be:

$$\% \text{ Deadtime} = \frac{I_{additional} + I_{charge}}{10\ (I_{charge})}$$

A bidirectional clock pin is provided for synchronization or for master/slave operation. As a master, the clock pin provides a positive output pulse during the discharge of C_T. As a slave, the clock pin is an input that resets the PWM latch and blanks the drive output, but does not discharge C_T. Therefore, the oscillator is not synchronized by driving the clock pin alone. Figures 29 and 30 provide suggested synchronization.

Error Amplifier

A fully compensated Error Amplifier is provided. It features a typical DC voltage gain of 95 dB and a gain bandwidth product of 8.3 MHz with 75 degrees of phase margin (Figure 3). Typical application circuits will have the noninverting input tied to the reference. The inverting input will typically be connected to a feedback voltage generated from the output of the switching power supply. Both inputs have a Common Mode Voltage (V_{CM}) input range of 1.5 V to 5.5 V. The Error Amplifier Output is provided for external loop compensation.

Soft–Start Latch

Soft–Start is accomplished in conjunction with an external capacitor. The soft start capacitor is charged by an internal 9.0 μA current source. This capacitor clamps the output of the error amplifier to less than its normal output voltage, thus limiting the duty cycle.

The time it takes for a capacitor to reach full charge is given by:

$$t \approx (4.5 \bullet 10^5)\ C_{Soft\text{-}Start}$$

A Soft–Start latch is incorporated to prevent erratic operation of this circuitry. Two conditions can cause the Soft–Start circuit to latch so that the Soft–Start capacitor stays discharged. The first condition is activation of an undervoltage lockout of either V_{CC} or V_{ref}. The second condition is when current sense input exceeds 1.4 V. Since this latch is "set dominant", it cannot be reset until either of these signals is removed, and the voltage at $C_{Soft\text{–}Start}$ is less than 0.5 V.

PWM Comparator and Latch

A PWM circuit typically compares an error voltage with a ramp signal. The outcome of this comparison determines the state of the output. In voltage mode operation the ramp signal is the voltage ramp of the timing capacitor. In current mode operation the ramp signal is the voltage ramp induced in a current sensing element. The ramp input of the PWM comparator is pinned out so that the user can decide which mode of operation best suits the application requirements. The ramp input has a 1.25 V offset such that whenever the voltage at this pin exceeds the Error Amplifier Output voltage minus 1.25 V, the PWM comparator will cause the PWM latch to set, disabling the outputs. Once the PWM latch is set, only a blanking pulse by the oscillator can reset it, thus initiating the next cycle.

A toggle flip flop connected to the output of the PWM latch controls which output is active. The flip flop is pulsed by an OR gate that gets its inputs from the oscillator clock and the output of the PWM latch. A pulse from either one will cause the flip flop to enable the other output.

Current Limiting and Shutdown

A pin is provided to perform current limiting and shutdown operations. Two comparators are connected to the input of this pin. When the voltage at this pin exceeds 1.0 V, one of the comparators is activated. The output of this comparator sets the PWM latch, which disables the output. In this way cycle–by–cycle current limiting is accomplished. If a current limit resistor is used in series with the power devices, the value of the resistor is found by:

$$R_{Sense} = \frac{1.0\ V}{I_{pk\ (switch)}}$$

If the voltage at this pin exceeds 1.4 V, the second comparator is activated. This comparator sets a latch which, in turn, causes the Soft–Start capacitor to be discharged. In this way a "hiccup" mode of recovery is possible in the case of output short circuits. If a current limit resistor is used in series with the output devices, the peak current at which the controller will enter a "hiccup" mode is given by:

$$I_{shutdown} = \frac{1.4\ V}{R_{Sense}}$$

3

Undervoltage Lockout

There are two undervoltage lockout circuits within the IC. The first senses V_{CC} and the second V_{ref}. During power–up, V_{CC} must exceed 9.2 V and V_{ref} must exceed 4.2 V before the outputs can be enabled and the Soft–Start latch released. If V_{CC} falls below 8.4 V or V_{ref} falls below 3.6 V, the outputs are disabled and the Soft–Start latch is activated. When the UVLO is active, the part is in a low current standby mode allowing the IC to have an off–line bootstrap start–up circuit. Typical start–up current is 500 μA.

Output

The MC34025 has two high current totem pole outputs specifically designed for direct drive of power MOSFETs. They are capable of up to ±2.0 A peak drive current with a typical rise and fall time of 30 ns driving a 1.0 nF load.

Separate pins for V_C and Power Ground are provided. With proper implementation, a significant reduction of switching transient noise imposed on the control circuitry is possible. The separate V_C supply input also allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}.

Reference

A 5.1 V bandgap reference is pinned out and is trimmed to an initial accuracy of ±1.0% at 25°C. This reference has short circuit protection and can source in excess of 10 mA for powering additional control system circuitry.

Design Considerations

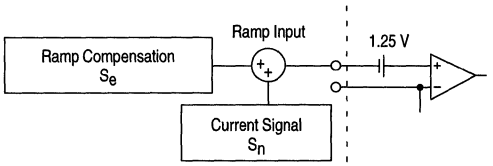
Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. With high frequency, high power, switching power supplies it is imperative to have separate current loops for the signal paths and for the power paths. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. All bypass capacitors and snubbers should be connected as close as possible to the specific part in question. The PC board lead lengths must be less than 0.5 inches for effective bypassing or snubbing.

Instabilities

In current mode control, an instability can be encountered at any given duty cycle. The instability is caused by the current feedback loop. It has been shown that the instability is caused by a double pole at half the switching frequency. If an external ramp (S_e) is added to the on–time ramp (S_n) of the current–sense waveform, stability can be achieved (see Figure 20).

One must be careful not to add too much ramp compensation. If too much is added, the system will start to perform like a voltage mode regulator. All benefits of current mode control will be lost. Figures 28A and 28B show examples of two different ways in which external ramp compensation can be implemented.

Figure 20. Ramp Compensation



A simple equation can be used to calculate the amount of external ramp necessary to add that will achieve stability in the current loop. For the following equations, the calculated values for the application circuit in Figure 36 are also shown.

$$S_e = \frac{V_O}{L}\left(\frac{N_S}{N_P}\right)(R_S)A_i$$

where:
V_O = DC output voltage
N_P, N_S = number of power transformer primary or secondary turns
A_i = gain of the current sense network (see Figures 25, 26 and 27)
L = output inductor
R_S = current sense resistance

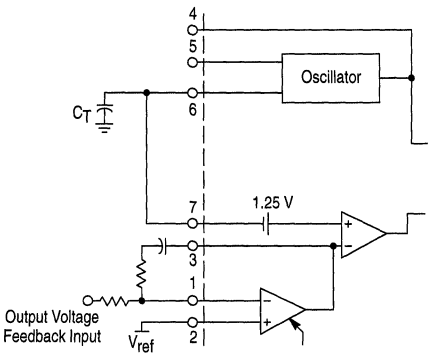
For the application circuit: $S_e = \frac{5}{1.8\ \mu}\left(\frac{4}{16}\right)(0.3)(0.55)$

$= 0.115\ V/\mu s$

PIN FUNCTION DESCRIPTION

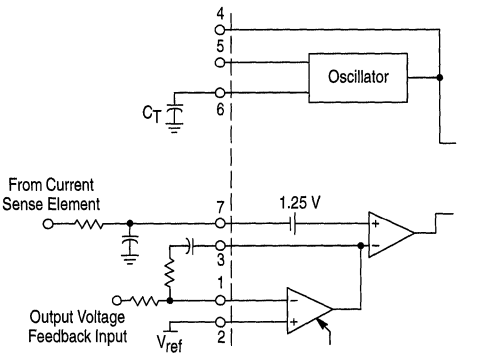
Pin No. DIP/SOIC	Function	Description
1	Error Amp Inverting Input	This pin is usually used for feedback from the output of the power supply.
2	Error Amp Noninverting Input	This pin is used to provide a reference in which an error signal can be produced on the output of the error amp. Usually this is connected to V_{ref}, however an external reference can also be used.
3	Error Amp Output	This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter.
4	Clock	This is a bidirectional pin used for synchronization.
5	R_T	The value of R_T sets the charge current through timing Capacitor, C_T.
6	C_T	In conjunction with R_T, the timing Capacitor sets the switching frequency. Because this part is a push–pull output, each output runs at one–half the frequency set at this pin.
7	Ramp Input	For voltage mode operation this pin is connected to C_T. For current mode operation this pin is connected through a filter to the current sensing element.
8	Soft–Start	A capacitor at this pin sets the Soft–Start time.
9	Current Limit/Shutdown	This pin has two functions. First, it provides cycle–by–cycle current limiting. Second, if the current is excessive, this pin will reinitiate a Soft–Start cycle.
10	Ground	This pin is the ground for the control circuitry.
11	Output A	This is a high current totem pole output.
12	Power Ground	This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
13	V_C	This is a separate power source connection for the outputs that is connected back to the power source input. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
14	Output B	This is a high current totem pole output.
15	V_{CC}	This pin is the positive supply of the control IC.
16	V_{ref}	This is a 5.1 V reference. It is usually connected to the noninverting input of the error amplifier.

Figure 21. Voltage Mode Operation



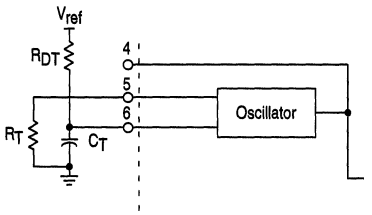
In voltage mode operation, the control range on the output of the Error Amplifier from 0% to 90% duty cycle is from 2.25 V to 4.05 V.

Figure 22. Current Mode Operation



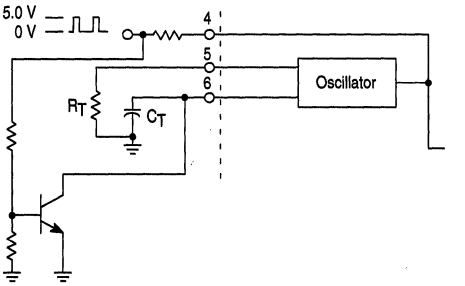
In current mode control, an RC filter should be placed at the ramp input to filter the leading edge spike caused by turn–on of a power MOSFET.

Figure 23. Dead Time Addition



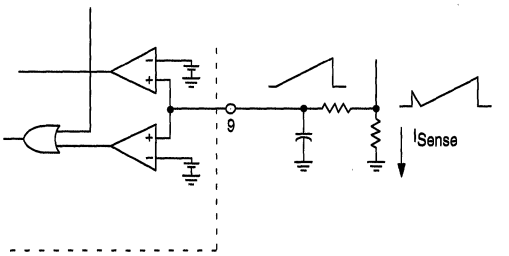
Additional dead time can be added by the addition of a dead time resistor from V_{ref} to C_T. See text on oscillator section for more information.

Figure 24. External Clock Synchronization



The sync pulse fed into the clock pin must be at least 3.9 V. R_T and C_T need to be set 10% slower than the sync frequency. This circuit is also used in voltage mode operation for master/slave operation. The clock signal would be coming from the master which is set at the desired operating frequency, while the slave is set 10% slower.

Figure 25. Resistive Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. If a transformer is used, the gain can be calculated by:

$$A_I = \frac{R_{Sense}}{\text{turns ratio}}$$

Figure 26. Primary Side Current Sensing

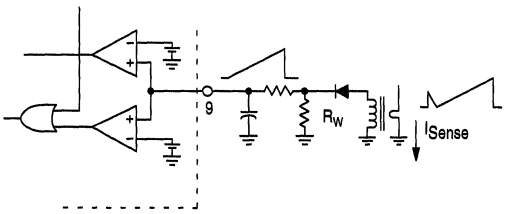
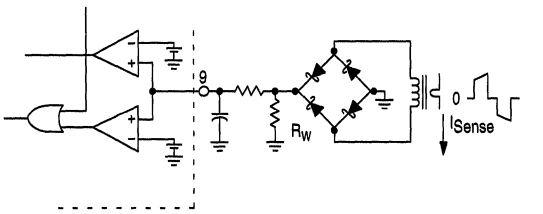


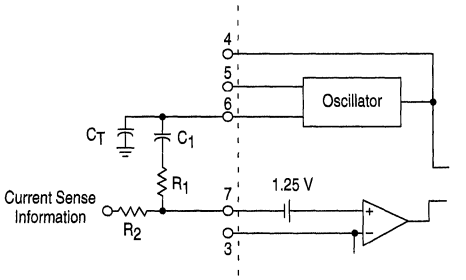
Figure 27. Primary or Secondary Side Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. The gain can be calculated by:

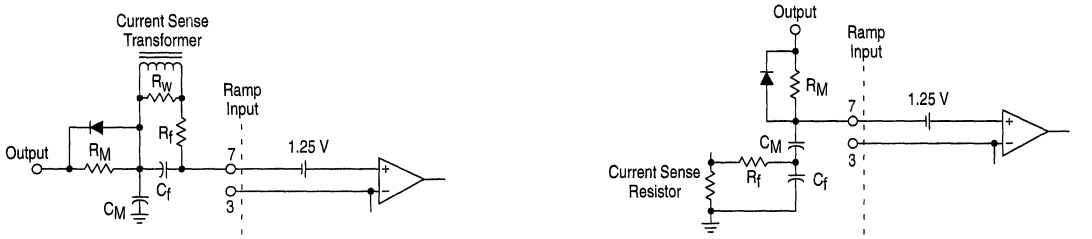
$$A_I = \frac{R_w}{\text{turns ratio}}$$

Figure 28A. Slope Compensation (Noise Sensitive)



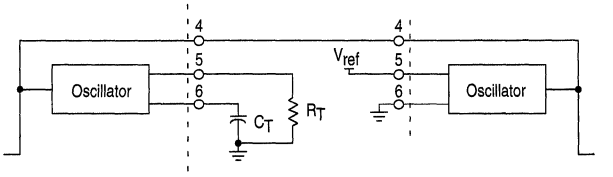
This method of slope compensation is easy to implement, however, it is noise sensitive. Capacitor C_1 provides AC coupling. The oscillator signal is added to the current signal by a voltage divider consisting of resistors R_1 and R_2.

Figure 28B. Slope Compensation (Noise Immune)



When only one output is used, this method of slope compensation can be used and it is relatively noise immune. Resistor R_M and capacitor C_M provide the added slope necessary. By choosing R_M and C_M with a larger time constant than the switching frequency, you can assume that its charge is linear. First choose C_M, then R_M can be adjusted to achieve the required slope. The diode provides a reset pulse at the ramp input at the end of every cycle. The charge current I_M can be calculated by $I_M = C_M S_e$. Then R_M can be calculated by $R_M = V_{CC}/I_M$.

Figure 29. Current Mode Master/Slave Operation Over Short Distances



3

Figure 30. Synchronization Over Long Distances

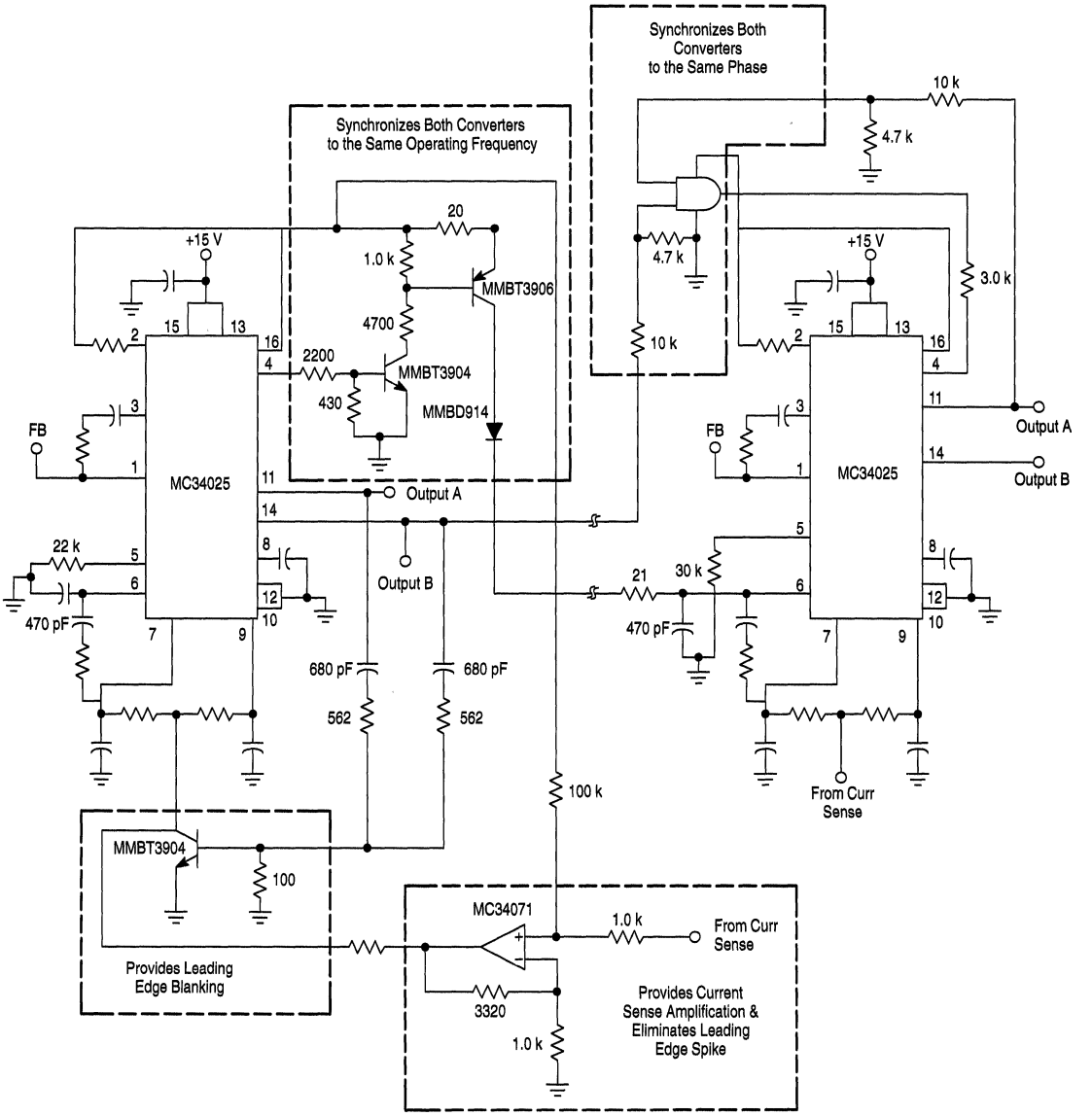
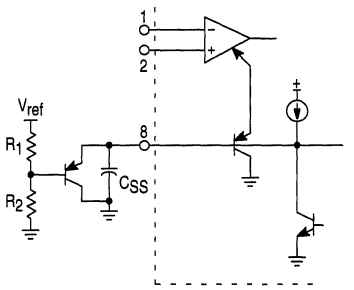


Figure 31. Buffered Maximum Clamp Level

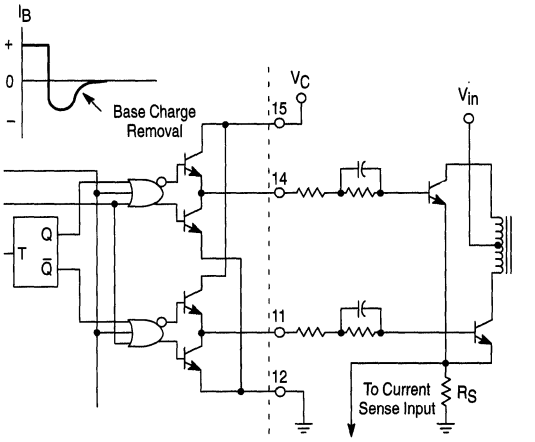


In voltage mode operation, the maximum duty cycle can be clamped. By the addition of a PNP transistor to buffer the clamp voltage, the Soft–Start current is not affected by R_1.

The new equation for Soft–Start is $t \approx \frac{V_{clamp} + 0.6}{9.0\ \mu A} (C_{SS})$

In current mode operation, this circuit will limit the maximum voltage allowed at the ramp input to end a cycle.

Figure 32. Bipolar Transistor Drive



The totem pole output can furnish negative base current for enhanced transistor turn–off, with the addition of the capacitor in series with the base.

Figure 33. Isolated MOSFET Drive

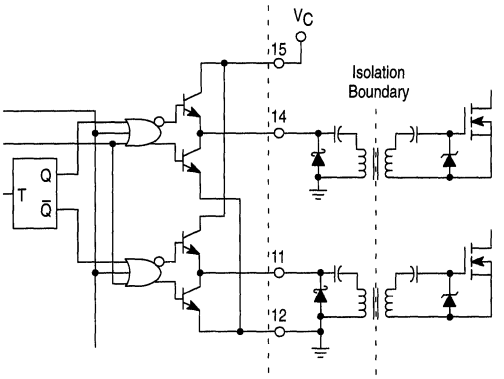
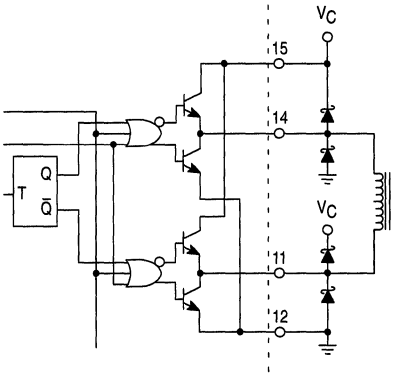
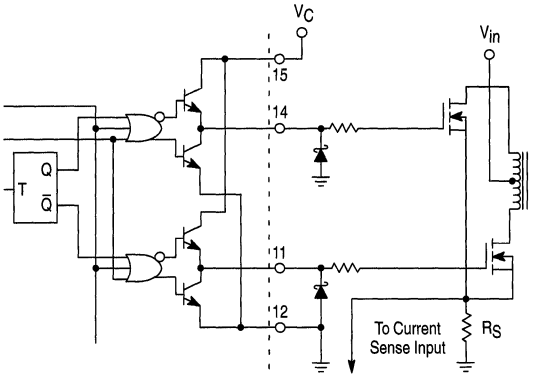


Figure 34. Direct Transformer Drive



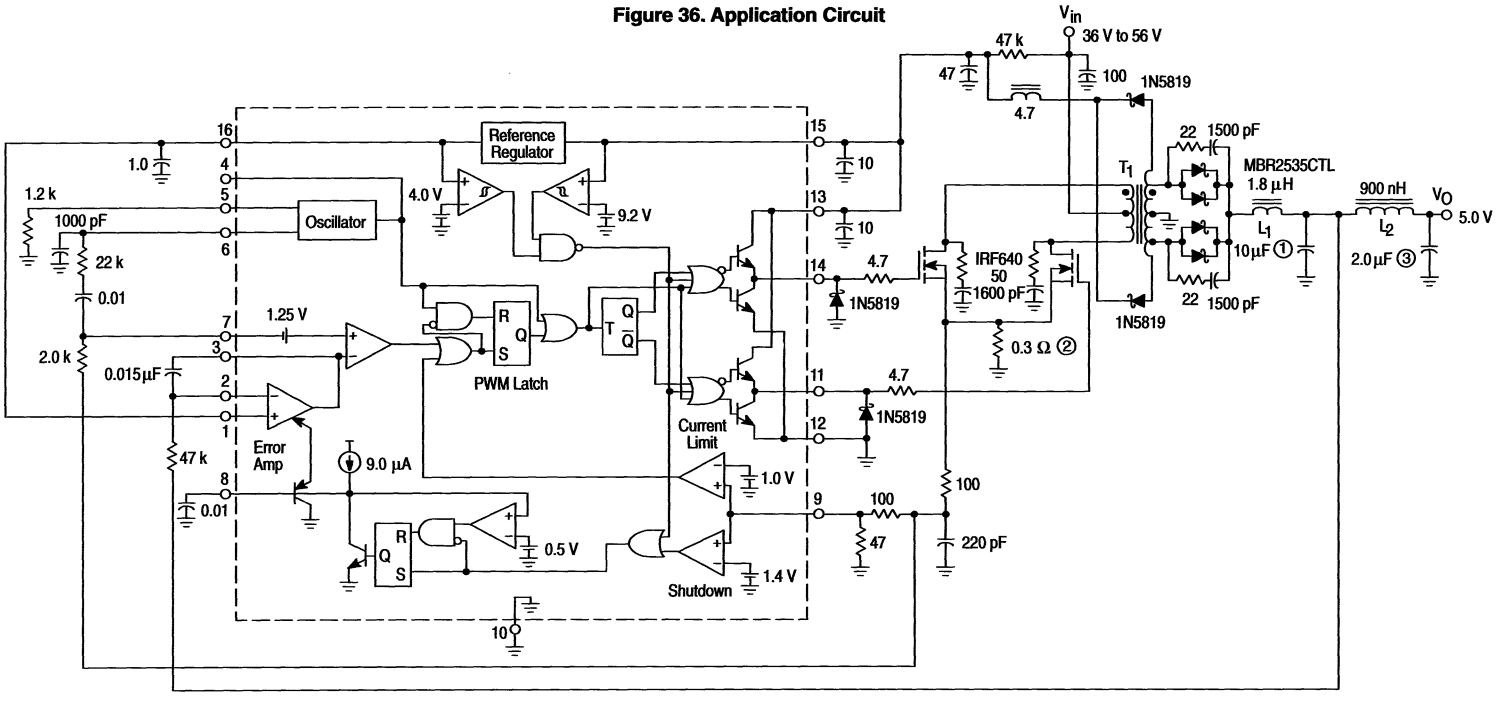
The totem pole output can easily drive pulse transformers. A Schottky diode is recommended when driving inductive loads at high frequencies. The diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 35. MOSFET Parasitic Oscillations



A series gate resistor may be needed to damp high frequency parasitic oscillation caused by a MOSFET's input capacitance and any series wiring inductance in the gate–source circuit. The series resistor will also decrease the MOSFET's switching speed. A Schottky diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground. The Schottky diode also prevents substrate injection when the output pin is driven below ground.

Figure 36. Application Circuit



T_1 – Primary: 16 turns center tapped #48 AWG (1300 strands litz wire)
Secondary: 4 turns center tapped 0.003" (2 layers) copper foil
Bootstrap: 1 turn added to each secondary output #36 AWG
Core: Philips 3F3, part #4312 020 4124
Bobbin: Philips part #4322 021 3525
Coilcraft P3269–A

L_1 – 2 turns #48 AWG (1300 strands litz wire)
Core: Philips 3F3, part #EP10–3F3
Bobbin: Philips part #EP10PCB1–8
L = 1.8 µH
Coilcraft P3270–A

L_2 – 7 turns #18 AWG, 1/2" diameter air core
Coilcraft P3271–A

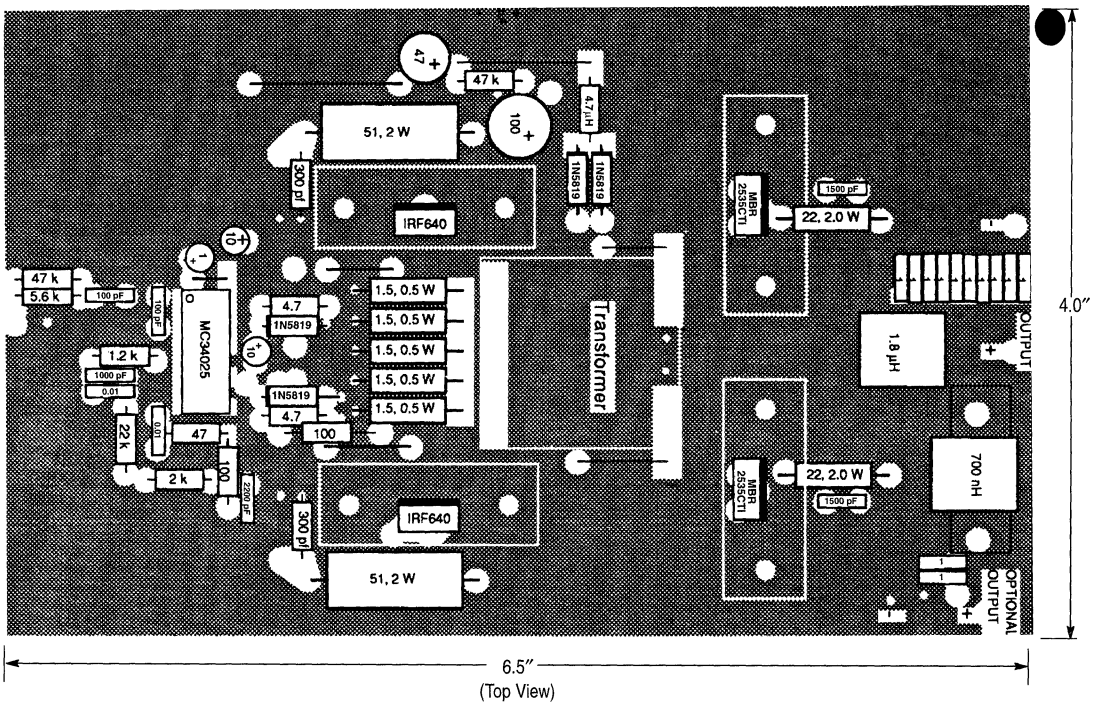
Heatsinks – Power FET: AAVID Heatsink #533902B02554 with clip
Output Rectifiers: AAVID Heatsink #533402B02552 with clip

Insulators – All power devices are insulated with Berquist Sil–Pad 1500

① – 10 (1.0 µF) ceramic capacitors in parallel
② – 5 (1.5 Ω) resistors in parallel
③ – 2 (1.0 µF) cearmic capacitors in parallel

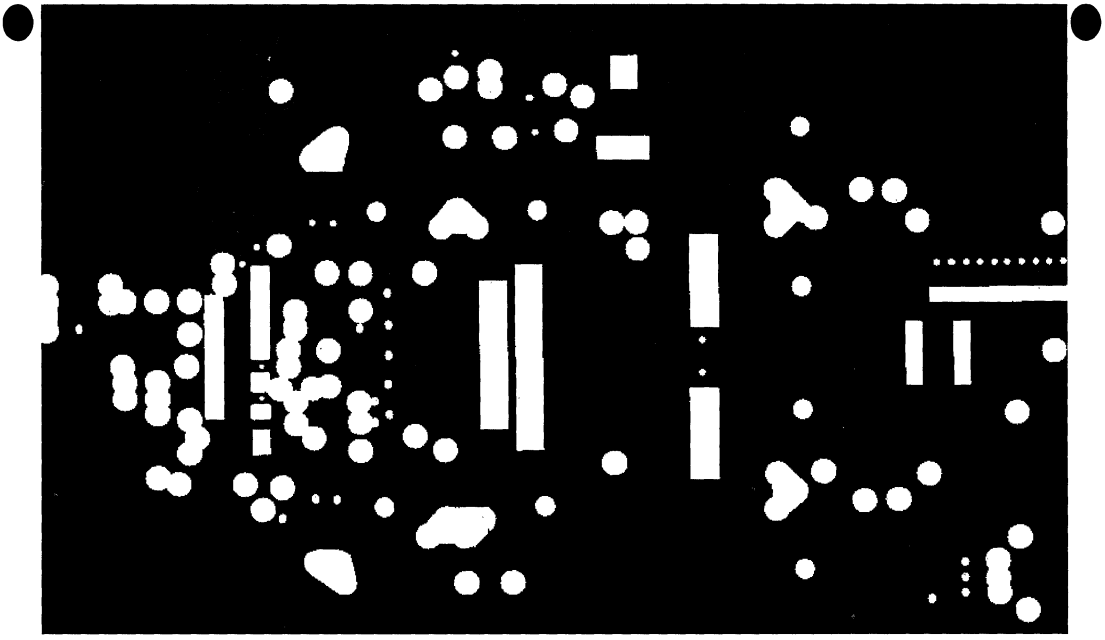
Test	Condition	Result
Line Regulation	V_{in} = 40 V to 56 V, I_O = 15 A	14 mV = ±0.275%
Load Regulation	V_{in} = 48 V, I_O = 8.0 V to 15 A	54 mV = ±1.0%
Output Ripple	V_{in} = 48 V, I_O = 15 A	50 mVp–p
Efficiency	V_{in} = 48 V, I_O = 15 A	71.2%

Figure 37. PC Board With Components

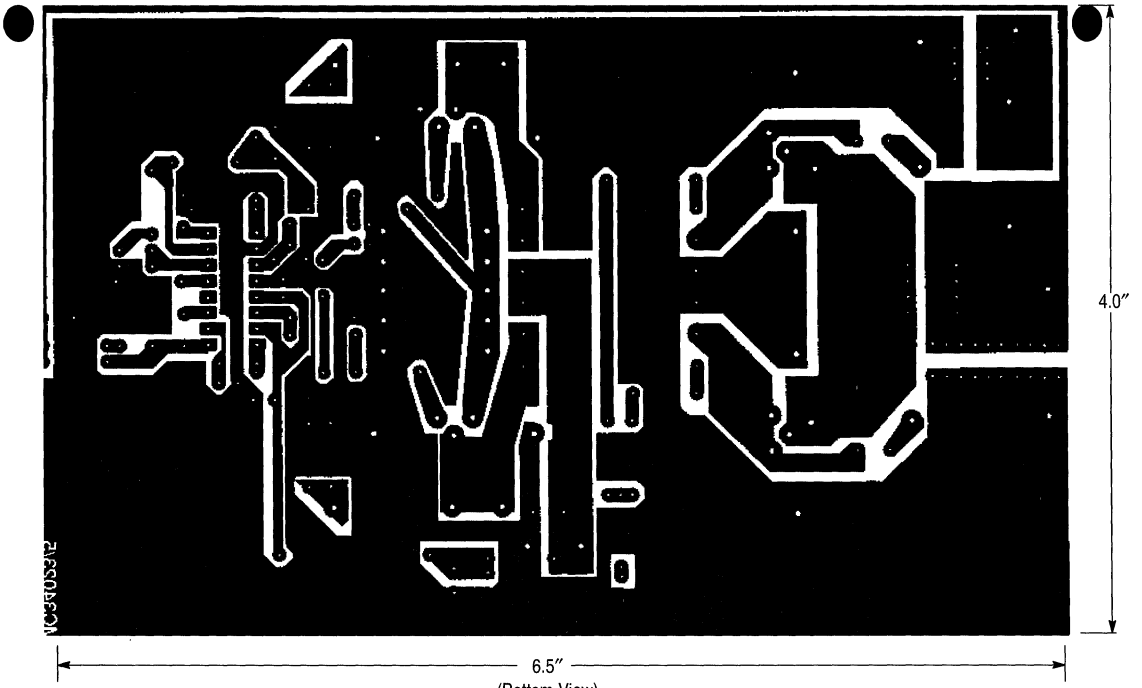


(Top View)

Figure 38. PC Board Without Components



(Top View)



(Bottom View)

MOTOROLA

MC34060A
MC33060A

3

Precision SWITCHMODE™ Pulse Width Modulator Control Circuit

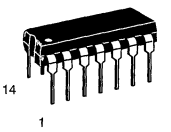
The MC34060A is a low cost fixed frequency, pulse width modulation control circuit designed primarily for single–ended SWITCHMODE power supply control.

The MC34060A is specified over the commercial operating temperature range of 0° to +70°C, and the MC33060A is specified over an automotive temperature range of –40° to +85°C.

- Complete Pulse Width Modulation Control Circuitry
- On–Chip Oscillator with Master or Slave Operation
- On–Chip Error Amplifiers
- On–Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Dead–Time Control
- Uncommitted Output Transistor Rated to 200 mA Source or Sink
- Undervoltage Lockout

PRECISION SWITCHMODE PULSE WIDTH MODULATOR CONTROL CIRCUIT

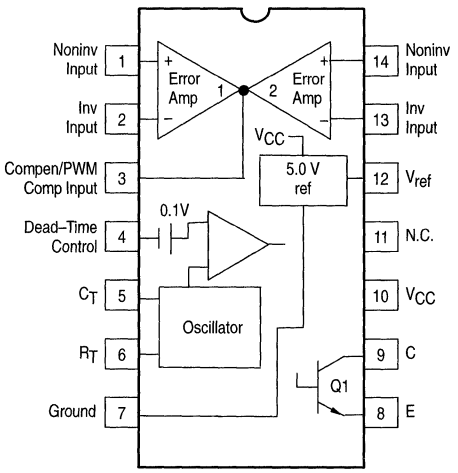
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34060AD	T_A = 0° to +70°C	SO–14
MC34060AP		Plastic DIP
MC33060AD	T_A = – 40° to +85°C	SO–14
MC33060AP		Plastic DIP

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	42	V
Collector Output Voltage	V_C	42	V
Collector Output Current (Note 1)	I_C	500	mA
Amplifier Input Voltage Range	V_{in}	–0.3 to +42	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	mW
Operating Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Operating Ambient Temperature Range For MC34060A For MC33060A	T_A	 0 to +70 –40 to +85	°C

NOTES: 1. Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristics	Symbol	P Suffix Package	D Suffix Package	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	80	120	°C/W
Derating Ambient Temperature	T_A	45	45	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	–	30	40	V
Collector Output Current	I_C	–	–	200	mA
Amplifier Input Voltage	V_{in}	–0.3	–	V_{CC} –2	V
Current Into Feedback Terminal	I_{fb}	–	–	0.3	mA
Reference Output Current	I_{ref}	–	–	10	mA
Timing Resistor	R_T	1.8	47	500	kΩ
Timing Capacitor	C_T	0.00047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz
PWM Input Voltage (Pins 3 and 4)	–	–0.3	–	5.3	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA, T_A 25°C) $T_A = T_{low}$ to T_{high} – MC34060A – MC33060A	V_{ref}	4.925 4.9 4.85	5.0 – –	5.075 5.1 5.1	V
Line Regulation (V_{CC} = 7.0 V to 40 V, I_O = 10 mA))	Reg_{line}	–	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	2.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OUTPUT SECTION					
Collector Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	–	2.0	100	μA
Emitter Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V, V_E = 0 V)	$I_{E(off)}$	–	–	–100	μA
Collector–Emitter Saturation Voltage (Note 2) Common–Emitter (V_E = 0 V, I_C = 200 mA) Emitter–Follower (V_C = 15 V, I_E = –200 mA)	$V_{sat(C)}$ $V_{sat(E)}$	– –	1.1 1.5	1.5 2.5	V
Output Voltage Rise Time (T_A = 25°C) Common–Emitter (See Figure 12) Emitter–Follower (See Figure 13)	t_r	 – –	 100 100	 200 200	ns
Output Voltage Fall Time (T_A = 25°C) Common–Emitter (See Figure 12 Emitter–Follower (See Figure 13)	t_r	 – –	 40 40	 100 100	ns
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O[Pin\ 3]}$ = 2.5 V)	V_{IO}	–	2.0	10	mV
Input Offset Current ($V_{C[Pin\ 3]}$ = 2.5 V)	I_{IO}	–	5.0	250	nA
Input Bias current ($V_{O[Pin\ 3]}$ = 2.5 V)	I_{IB}	–	–0.1	–2.0	μA
Input Common Mode Voltage Range (V_{CC} = 40 V)	V_{ICR}	0 to V_{CC} –2.0	–	–	V
Inverting Input Voltage Range	$V_{IR(INV)}$	–0.3 to V_{CC}–2.0	–	–	V
Open–Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	–	dB
Unity–Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_c	–	600	–	kHz
Phase Margin at Unity–Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	–	65	–	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V, V_{in} = 0 V to 38 V))	CMRR	65	90	–	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	–	100	–	dB
Output Sink Current ($V_{O[Pin\ 3]}$ = 0.7 V)	I_{O-}	0.3	0.7	–	mA
Output Source Current ($V_{O[Pin\ 3]}$ = 3.5 V)	I_{O+}	–2.0	–4.0	–	mA

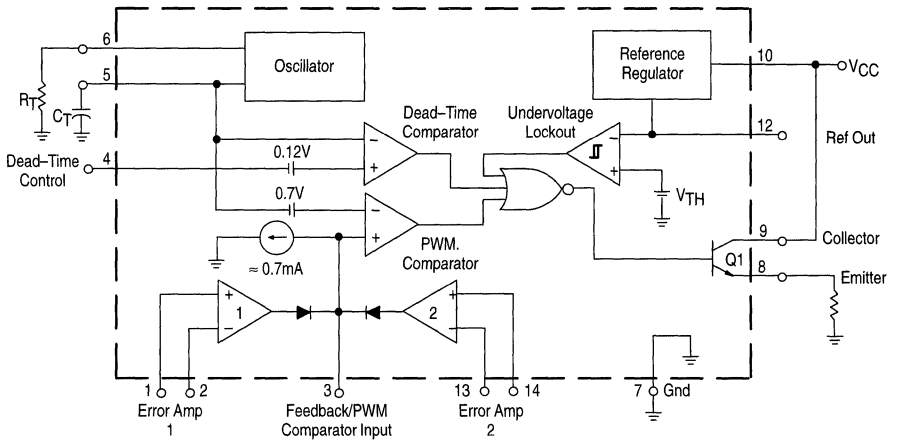
NOTES: 2. Low duty cycle techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.
T_{low} = –40°C for MC33060A T_{high} = +85°C for MC33060A
= 0°C for MC34060A = +70°Cfor MC34060A

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Test circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	3.5	4.5	V
Input Sink Current ($V_{[Pin\ 3]}$ = 0.7 V)	I_I	0.3	0.7	–	mA
DEAD–TIME CONTROL SECTION (Test circuit Figure 11)					
Input Bias Current (Pin 4) (V_{in} = 0 V to 5.25 V)	$I_{IB(DT)}$	–	–1.0	–10	μA
Maximum Output Duty Cycle	DC_{max}				%
(V_{in} = 0 V, C_T = 0.01 μF, R_T = 12 kΩ)		90	96	100	
(V_{in} = 0 V, C_T = 0.001 μF, R_T = 47 kΩ)		–	92	–	
Input Threshold Voltage (Pin 4)	V_{TH}				V
(Zero Duty Cycle)		–	2.8	3.3	
(Maximum Duty Cycle)		0	–	–	
OSCILLATOR SECTION					
Frequency	f_{osc}				kHz
(C_T = 0.01 μF, R_T = 12 kΩ, T_A = 25°C)		9.7	10.5	11.3	
T_A = T_{low} to T_{high} – MC34060A		9.5	–	11.5	
– MC33060A		9.0	–	11.5	
(C_T = 0.001 μF, R_T = 47 kΩ)		–	25	–	
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 47 kΩ)	σf_{osc}	–	1.5	–	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V)	$\Delta f_{osc}(\Delta V)$	–	0.5	2.0	%
Frequency Change with Temperature	$\Delta f_{osc}(\Delta T)$				%
(ΔT_A = T_{low} to T_{high})		–	4.0	–	
(C_T = 0.01 μF, R_T = 12 kΩ)		–	–	–	
UNDERVOLTAGE LOCKOUT SECTION					
Turn–On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	4.0	4.7	5.5	V
Hysteresis	V_H	50	150	300	mV
TOTAL DEVICE					
Standby Supply Current	I_{CC}				mA
(Pin 6 at V_{ref}, all other inputs and outputs open)					
(V_{CC} = 15 V)		–	5.5	10	
(V_{CC} = 40 V)		–	7.0	15	
Average Supply Current ($V_{[Pin\ 4]}$ = 2.0 V, C_T = 0.001 μF, R_T = 47 kΩ). See Figure 11.	I_S	–	7.0	–	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula; $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - x)^2}{N-1}}$

Figure 1. Block Diagram



This device contains 46 active transistors.

Description

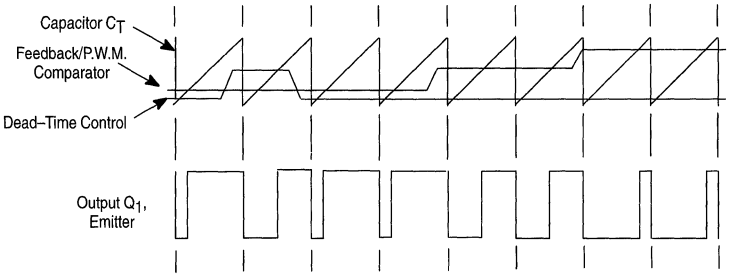
The MC34060A is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply (see Figure 1). An internal–linear sawtooth oscillator is frequency–programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.2}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control–signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

Figure 2. Timing Diagram



APPLICATIONS INFORMATION

The control signals are external inputs that can be fed into the dead–time control, the error amplifier inputs, or the feed–back input. The dead–time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth–cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time–control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on–time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from –0.3 V to (V_{CC} –2.0 V), and may be used to sense power supply output voltage and current. The error–amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC34060A has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of ±5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to +70°C.

3

Figure 3. Oscillator Frequency versus Timing Resistance

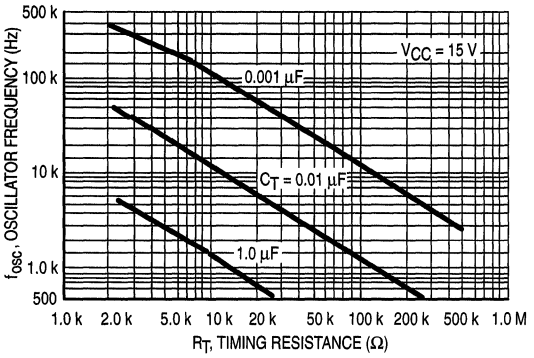


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

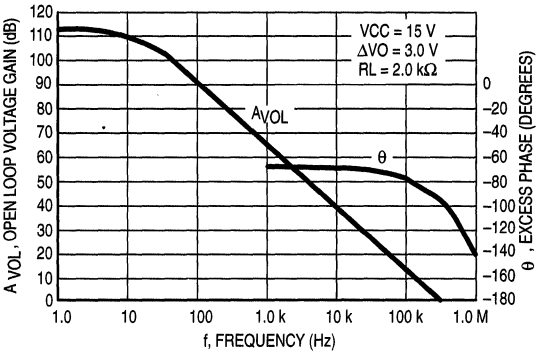


Figure 5. Percent Deadtime versus Oscillator Frequency

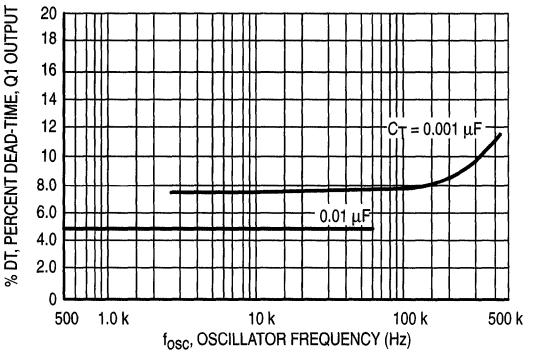


Figure 6. Percent Duty Cycle versus Dead–Time Control Voltage

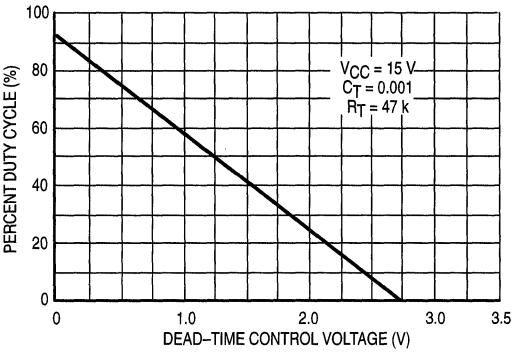


Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current

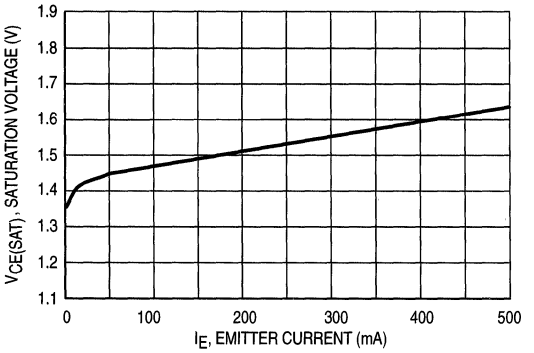


Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current

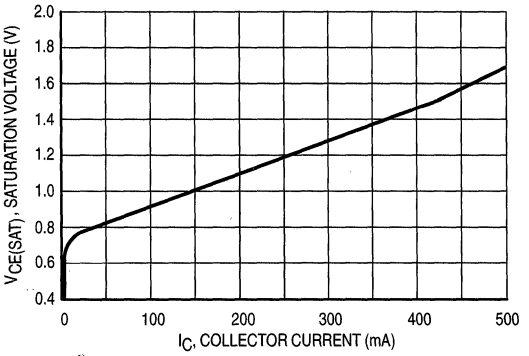


Figure 9. Standby Supply Current versus Supply Voltage

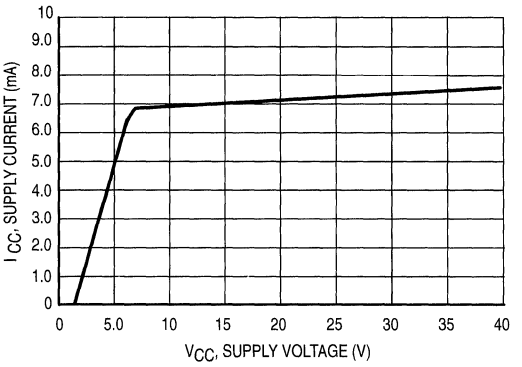


Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current

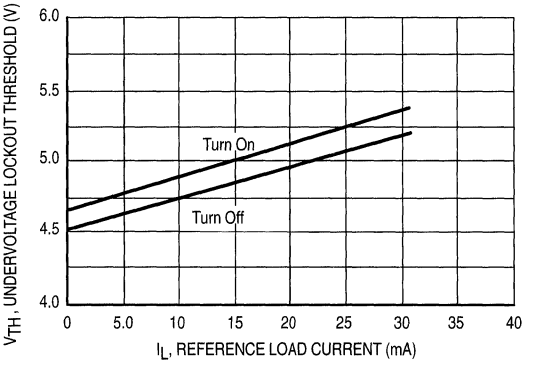


Figure 11. Error Amplifier Characteristics

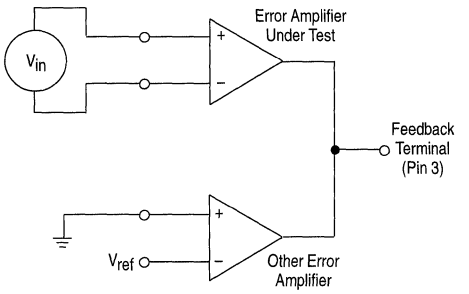


Figure 12. Deadtime and Feedback Control

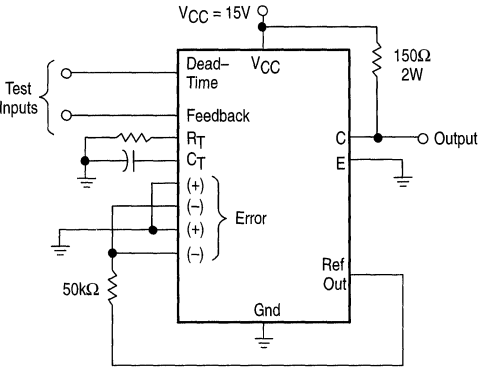


Figure 13. Common–Emitter Configuration and Waveform

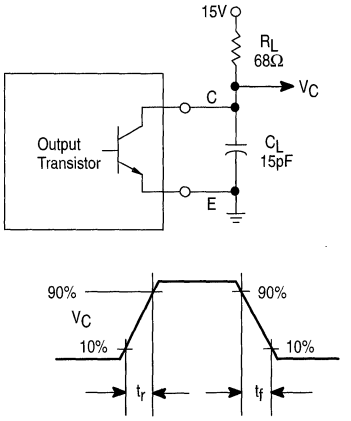


Figure 14. Emitter–Follower Configuration and Waveform

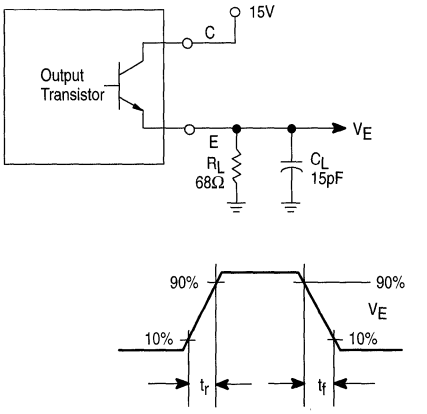


Figure 15. Error Amplifier Sensing Techniques

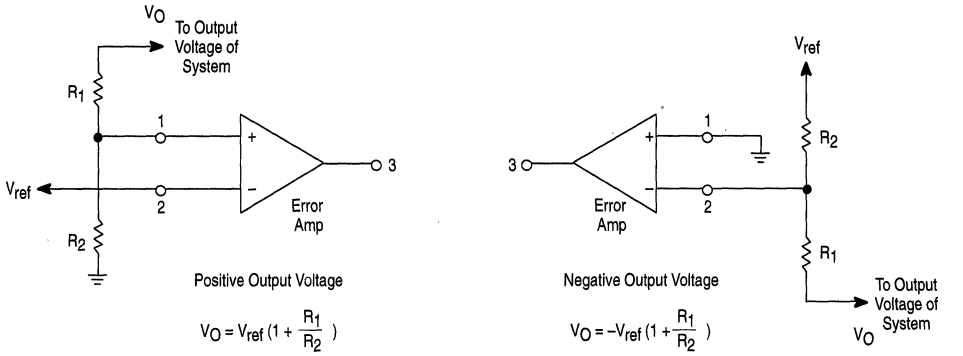


Figure 16. Deadtime Control Circuit

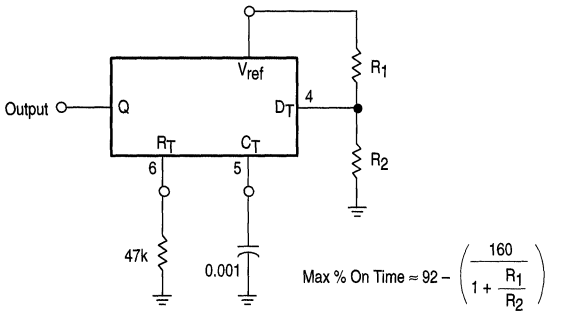


Figure 17. Soft–Start Circuit

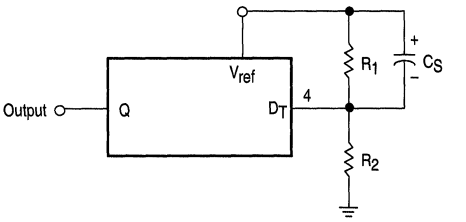


Figure 18. Slaving Two or More Control Circuits

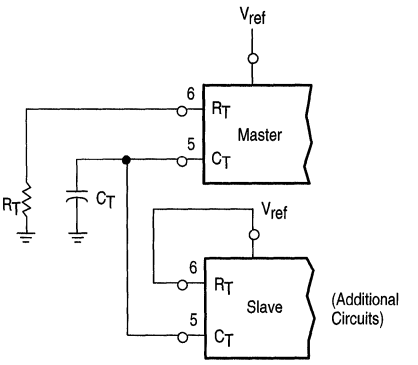
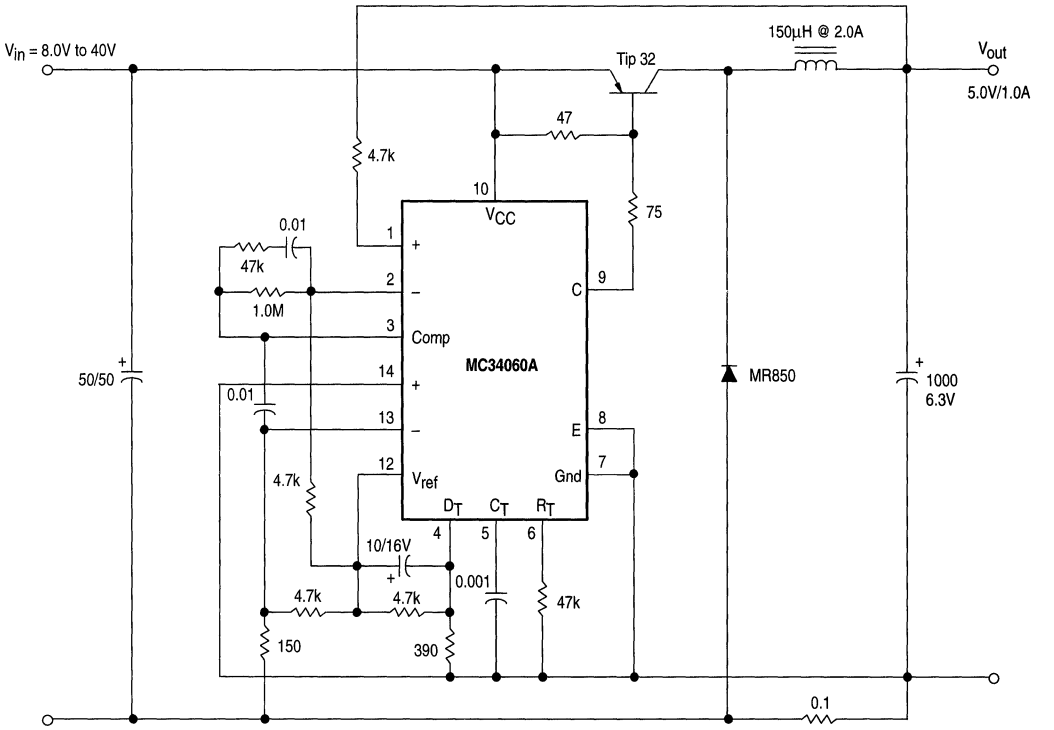
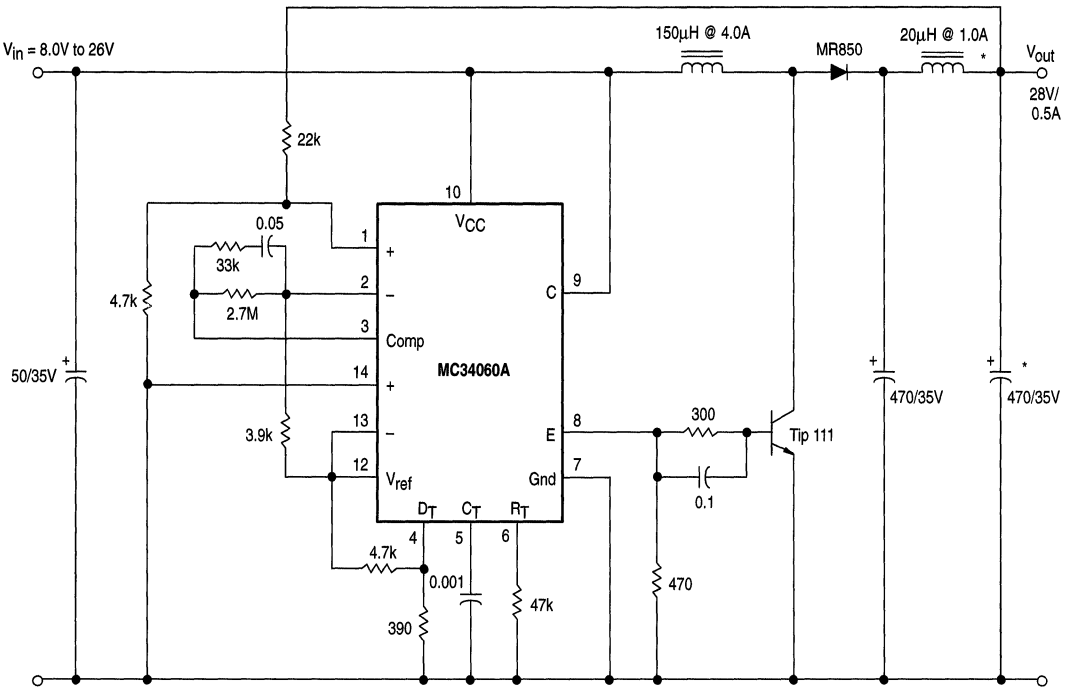


Figure 19. Step–Down Converter with Soft–Start and Output Current Limiting



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 1.0 A	25 mV 0.5%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	75 mV p–p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	73%

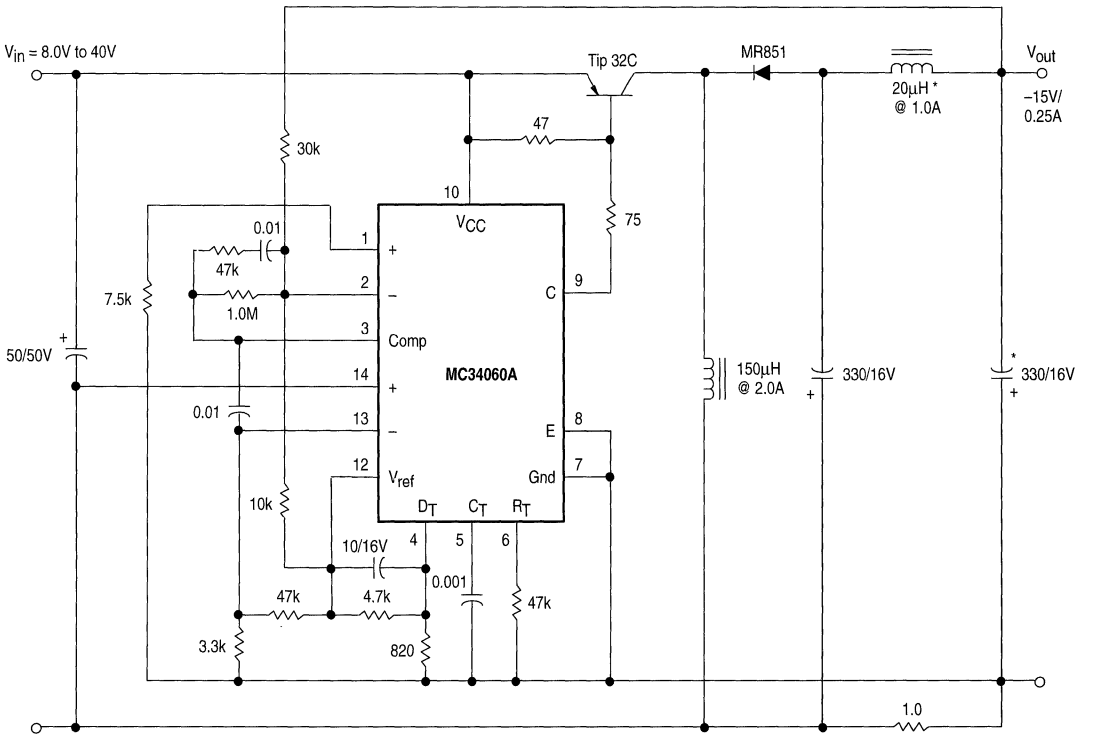
Figure 20. Step–Up Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 26 V, I_O = 0.5 A	40 mV 0.14%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 0.5 A	5.0 mV 0.18%
Output Ripple	V_{in} = 12 V, I_O = 0.5 A	24 mV p–p P.A.R.D.
Efficiency	V_{in} = 12 V, I_O = 0.5 A	75%

* Optional circuit to minimize output ripple

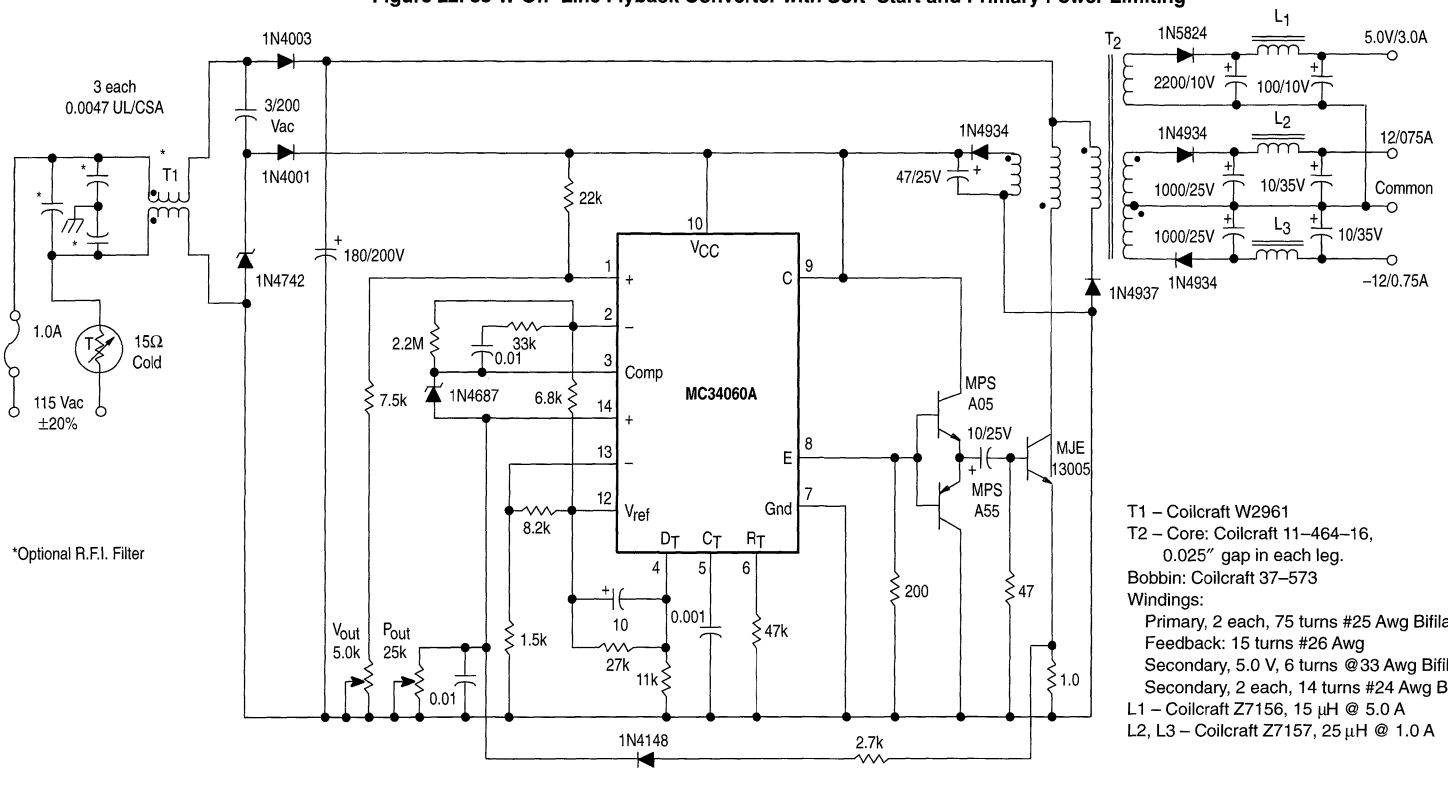
Figure 21. Step–Up/Down Voltage Inverting Converter with Soft–Start and Current Limiting



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 250 mA	52 mV 0.35%
Load Regulation	V_{in} = 12 V, I_O = 1.0 to 250 mA	47 mV 0.32%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	10 mV p–p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	330 mA
Efficiency	V_{in} = 12 V, I_O = 250 mA	86%

* Optional circuit to minimize output ripple

Figure 22. 33 W Off–Line Flyback Converter with Soft–Start and Primary Power Limiting



T1 – Coilcraft W2961
T2 – Core: Coilcraft 11–464–16,
0.025″ gap in each leg.
Bobbin: Coilcraft 37–573
Windings:
Primary, 2 each, 75 turns #25 Awg Bifilar wound
Feedback: 15 turns #26 Awg
Secondary, 5.0 V, 6 turns @33 Awg Bifilar wound
Secondary, 2 each, 14 turns #24 Awg Bifilar wound
L1 – Coilcraft Z7156, 15 μH @ 5.0 A
L2, L3 – Coilcraft Z7157, 25 μH @ 1.0 A

Test	Conditions	Results
Line Regulation 5.0 V	V_{in} = 95 Vac to 135 Vac, I_O = 3.0 A	20 mV 0.40%
Line Regulation ±12 V	V_{in} = 95 Vac to 135 Vac, I_O = ±0.75 A	52 mV 0.26%
Load Regulation 5.0 V	V_{in} = 115 Vac, I_O = 1.0 A to 4.0 A	476 mV 9.5%
Load Regulation ±12 V	V_{in} = 115 Vac, I_O = ±0.4 A to ±0.9 A	300 mV 2.5%
Output Ripple 5.0 V	V_{in} = 115 Vac, I_O = 3.0 A	45 mV p–p P.A.R.D.
Output Ripple ±12 V	V_{in} = 115 Vac, I_O = ±0.75 A	75 mV p–p P.A.R.D.
Efficiency	V_{in} = 115 Vac, I_O 5.0 V = 3.0 A I_O ±12 V = ±0.75 A	74%

MC34063A
MC33063A

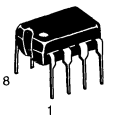
DC-to-DC Converter Control Circuits

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC–to–DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step–Down and Step–Up and Voltage–Inverting applications with a minimum number of external components. Refer to Application Notes AN920A/D and AN954/D for additional design information.

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

DC–to–DC CONVERTER CONTROL CIRCUITS

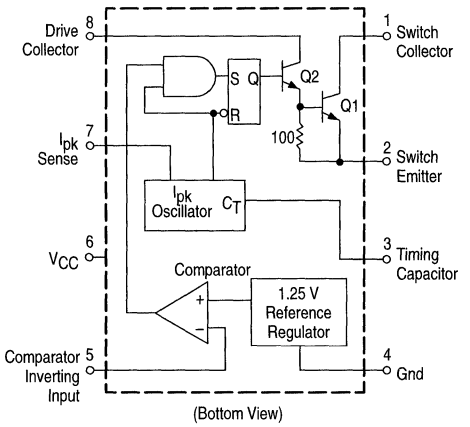
SEMICONDUCTOR TECHNICAL DATA



P, P1 SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

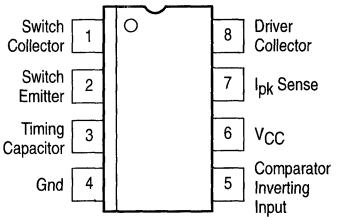
Representative Schematic Diagram



(Bottom View)

This device contains 51 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33063AD	T_A = – 40° to +85°C	SO–8
MC33063AP1		Plastic DIP
MC33063AVD	T_A = –40° to +125°C	SO–8
MC33063AVP		Plastic DIP
MC34063AD	T_A = 0° to +70°C	SO–8
MC34063AP1		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	−0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage ($V_{Pin\ 1}$ = 40 V)	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	A
Power Dissipation and Thermal Characteristics Plastic Package, P, P1 Suffix T_A = 25°C Thermal Resistance SOIC Package, D Suffix T_A = 25°C Thermal Resistance	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 1.25 100 625 160	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range MC34063A MC33063AV MC33063A	T_A	 0 to +70 −40 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES: 1. Maximum package power dissipation limits must be observed.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency ($V_{Pin\ 5}$ = 0 V, C_T = 1.0 nF, T_A = 25°C)	f_{osc}	24	33	42	kHz
Charge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{chg}	24	35	42	µA
Discharge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{dischg}	140	220	260	µA
Discharge to Charge Current Ratio (Pin 7 to V_{CC}, T_A = 25°C)	I_{dischg}/I_{chg}	5.2	6.5	7.5	–
Current Limit Sense Voltage (I_{chg} = I_{dischg}, T_A = 25°C)	$V_{ipk(sense)}$	250	300	350	mV
OUTPUT SWITCH (Note 4)					
Saturation Voltage, Darlington Connection (Note 5) (I_{SW} = 1.0 A, Pins 1, 8 connected)	$V_{CE(sat)}$	–	1.0	1.3	V
Saturation Voltage, Darlington Connection (I_{SW} = 1.0 A, $R_{Pin\ 8}$ = 82 Ω to V_{CC}, Forced β ≈ 20)	$V_{CE(sat)}$	–	0.45	0.7	V
DC Current Gain (I_{SW} = 1.0 A, V_{CE} = 5.0 V, T_A = 25°C)	h_{FE}	50	75	–	–
Collector Off–State Current (V_{CE} = 40 V)	$I_{C(off)}$	–	0.01	100	µA

NOTES: 3. T_{low} = 0°C for MC34063A, −40°C for MC33063A, AV T_{high} = +70°C for MC34063A, +85°C for MC33063A, +125°C for MC33063AV
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
5. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs for it to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended:

Forced β of output switch : $\frac{I_C \text{ output}}{I_C \text{ driver} - 7.0 \text{ mA}^*} \geq 10$

*The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage T_A = 25°C T_A = T_{low} to T_{high}	V_{th}	 1.225 1.21	 1.25 –	 1.275 1.29	V
Threshold Voltage Line Regulation (V_{CC} = 3.0 V to 40 V) MC33063A, MC34063A MC33363AV	Reg_{line}	 – –	 1.4 1.4	 5.0 6.0	mV
Input Bias Current (V_{in} = 0 V)	I_{IB}	–	–20	–400	nA
TOTAL DEVICE					
Supply Current (V_{CC} = 5.0 V to 40 V, C_T = 1.0 nF, Pin 7 = V_{CC}, $V_{Pin\ 5}$ > V_{th}, Pin 2 = Gnd, remaining pins open)	I_{CC}	–	–	4.0	mA

NOTES: 3. T_{low} = 0°C for MC34063A, –40°C for MC33063A, AV T_{high} = +70°C for MC34063A, +85°C for MC33063A, +125°C for MC33063AV

4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

5. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs for it to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended:

Forced β of output switch : $\frac{I_C \text{ output}}{I_C \text{ driver} - 7.0\ mA^*} \geq 10$

*The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

Figure 1. Output Switch On–Off Time versus Oscillator Timing Capacitor

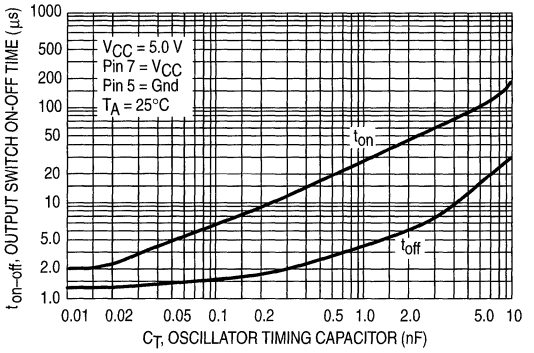


Figure 2. Timing Capacitor Waveform

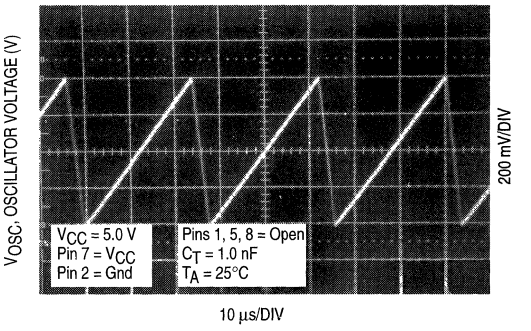


Figure 3. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

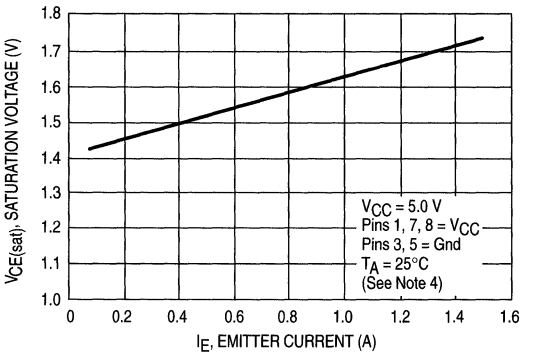


Figure 4. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current

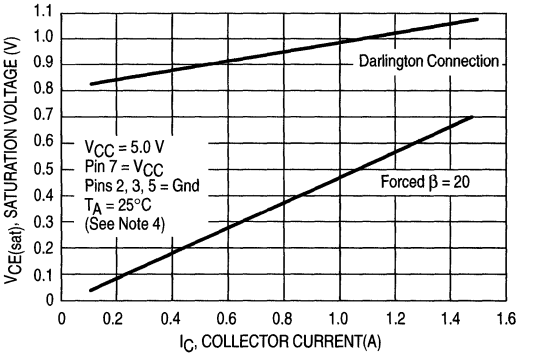


Figure 5. Current Limit Sense Voltage versus Temperature

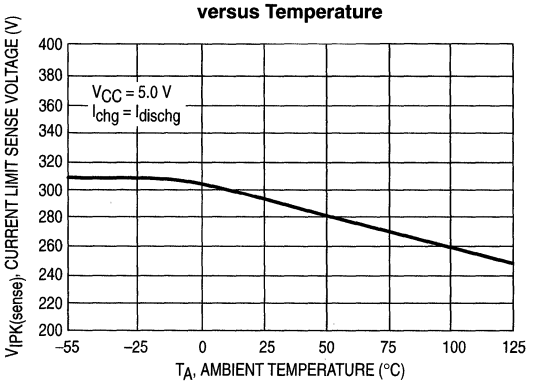
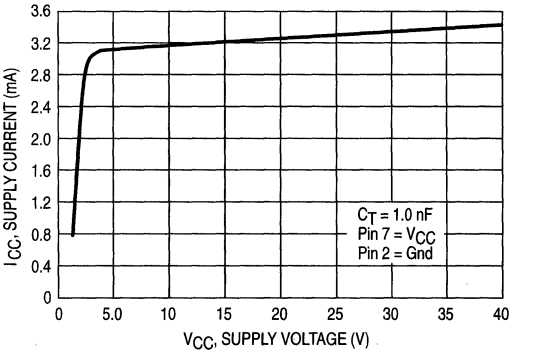
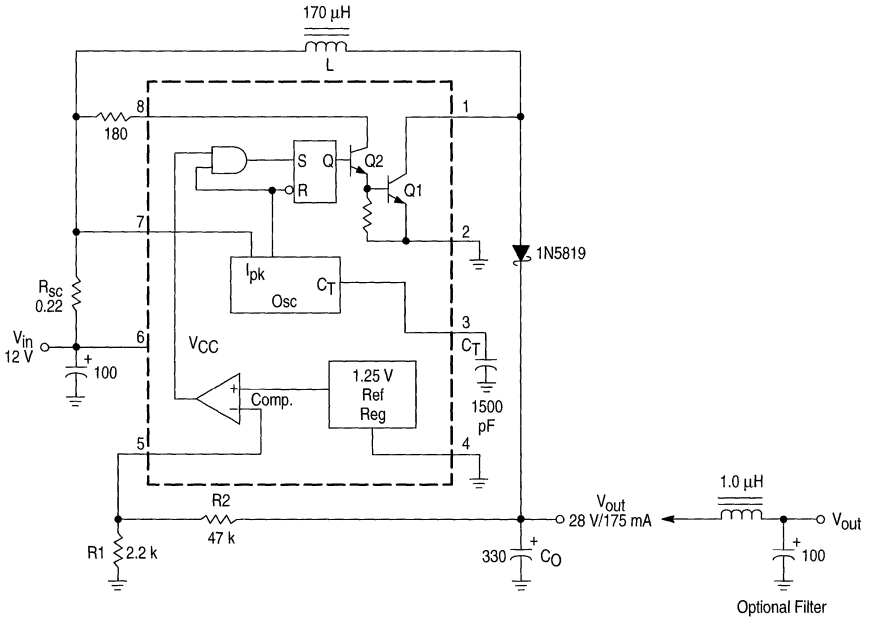


Figure 6. Standby Supply Current versus Supply Voltage



NOTE: 4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

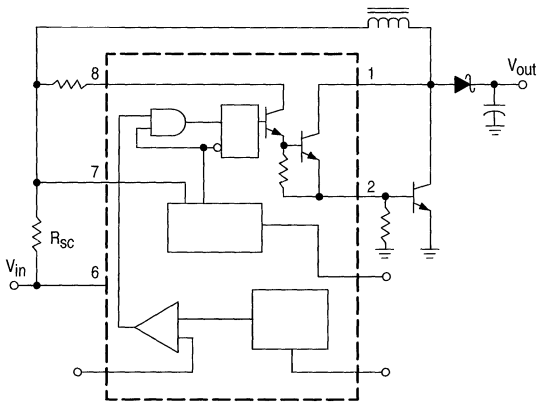
Figure 7. Step–Up Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 16 V, I_O = 175 mA	30 mV = ±0.05%
Load Regulation	V_{in} = 12 V, I_O = 75 mA to 175 mA	10 mV = ±0.017%
Output Ripple	V_{in} = 12 V, I_O = 175 mA	400 mVpp
Efficiency	V_{in} = 12 V, I_O = 175 mA	87.7%
Output Ripple With Optional Filter	V_{in} = 12 V, I_O = 175 mA	40 mVpp

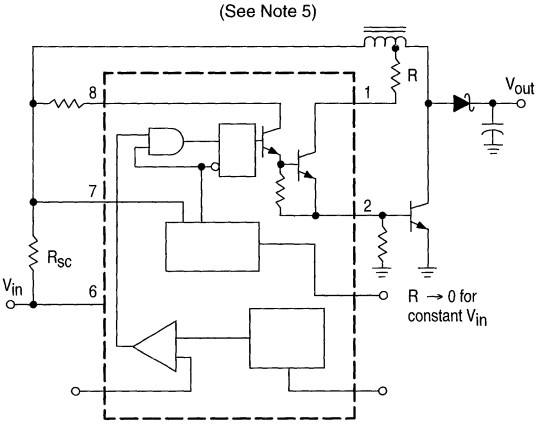
Figure 8. External Current Boost Connections for I_C Peak Greater than 1.5 A

8a. External NPN Switch



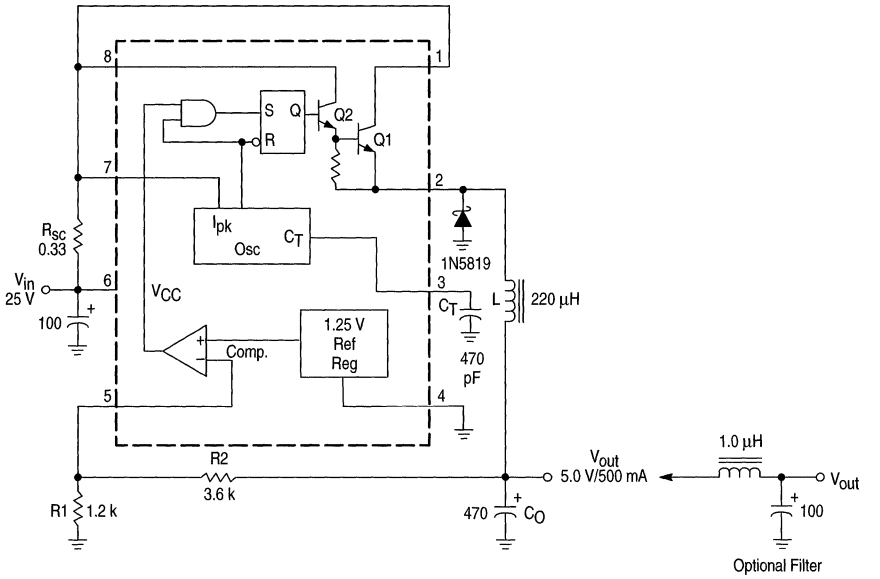
8b. External NPN Saturated Switch

(See Note 5)



NOTE: 5. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended.

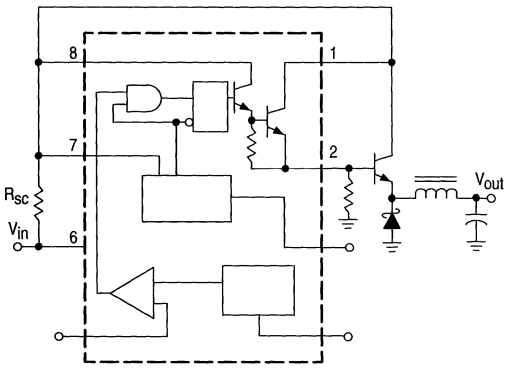
Figure 9. Step–Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 15 V to 25 V, I_O = 500 mA	12 mV = ±0.12%
Load Regulation	V_{in} = 25 V, I_O = 50 mA to 500 mA	3.0 mV = ±0.03%
Output Ripple	V_{in} = 25 V, I_O = 500 mA	120 mVpp
Short Circuit Current	V_{in} = 25 V, R_L = 0.1 Ω	1.1 A
Efficiency	V_{in} = 25 V, I_O = 500 mA	83.7%
Output Ripple With Optional Filter	V_{in} = 25 V, I_O = 500 mA	40 mVpp

Figure 10. External Current Boost Connections for I_C Peak Greater than 1.5 A

10a. External NPN Switch



10b. External PNP Saturated Switch

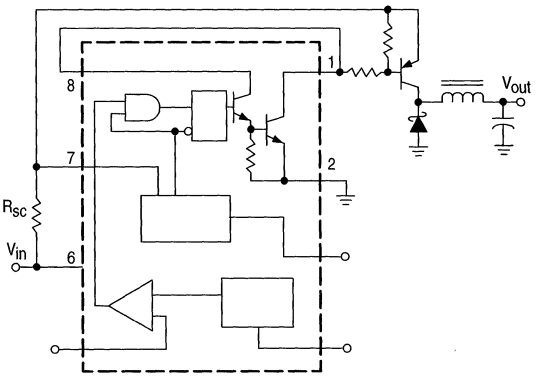
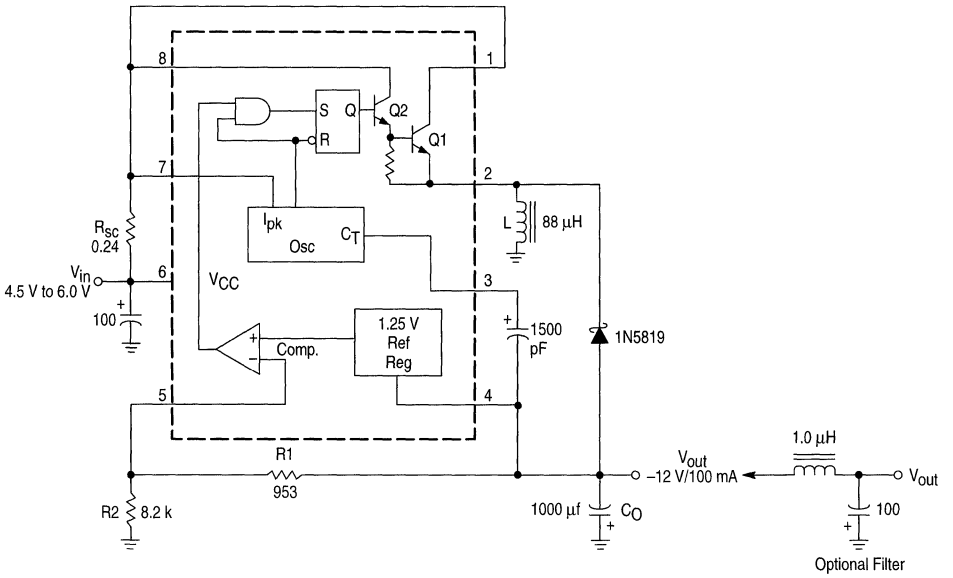


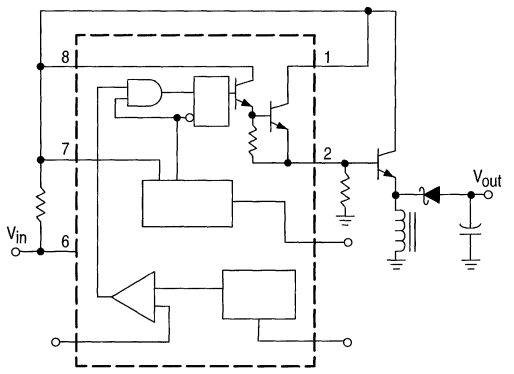
Figure 11. Voltage Inverting Converter



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 V to 6.0 V, I_O = 100 mA	3.0 mV = ±0.012%
Load Regulation	V_{in} = 5.0 V, I_O = 10 mA to 100 mA	0.022 V = ±0.09%
Output Ripple	V_{in} = 5.0 V, I_O = 100 mA	500 mVpp
Short Circuit Current	V_{in} = 5.0 V, R_L = 0.1 Ω	910 mA
Efficiency	V_{in} = 5.0 V, I_O = 100 mA	62.2%
Output Ripple With Optional Filter	V_{in} = 5.0 V, I_O = 100 mA	70 mVpp

Figure 12. External Current Boost Connections for I_C Peak Greater than 1.5 A

12a. External NPN Switch



12b. External PNP Saturated Switch

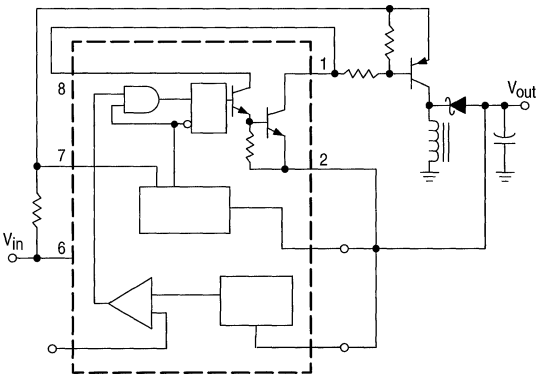
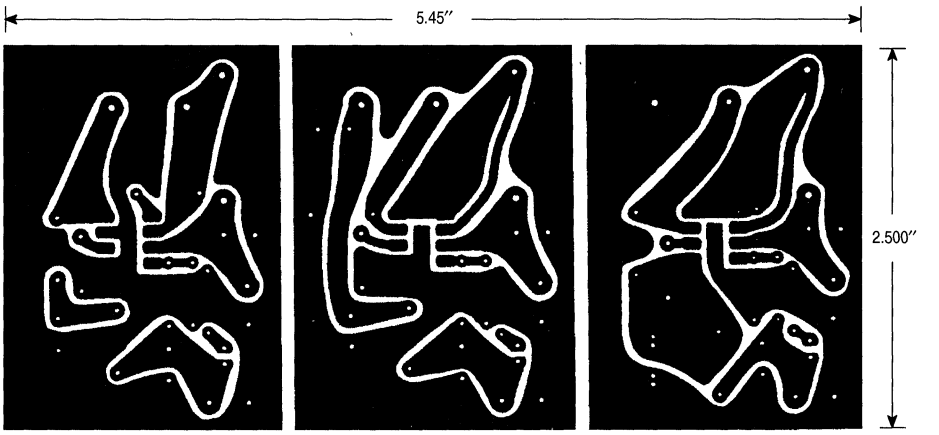
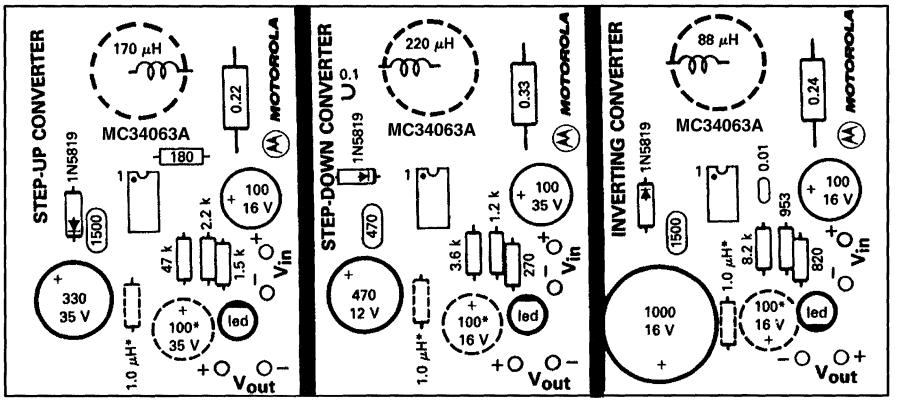


Figure 13. Printed Circuit Board and Component Layout
(Circuits of Figures 7, 9, 11)



(Top view, copper foil as seen through the board from the component side)



(Top View, Component Side) *Optional Filter.

INDUCTOR DATA

Converter	Inductance (μH)	Turns/Wire
Step–Up	170	38 Turns of #22 AWG
Step–Down	220	48 Turns of #22 AWG
Voltage–Inverting	88	28 Turns of #22 AWG

All inductors are wound on Magnetics Inc. 55117 toroidal core.

Figure 14. Design Formula Table

Calculation	Step–Up	Step–Down	Voltage–Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5}\, t_{on}$	$4.0 \times 10^{-5}\, t_{on}$	$4.0 \times 10^{-5}\, t_{on}$
$I_{pk(switch)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1\right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1\right)$
R_{sc}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$9\,\frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9\,\frac{I_{out} t_{on}}{V_{ripple(pp)}}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} – Nominal input voltage.
V_{out} – Desired output voltage, $|V_{out}| = 1.25 \left(1 + \frac{R2}{R1}\right)$
I_{out} – Desired output current.
f_{min} – Minimum desired output switching frequency at the selected values of V_{in} and I_O.
$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

NOTE: For further information refer to Application Note AN920A/D and AN954/D.

MOTOROLA

MC34064
MC33064

Undervoltage Sensing Circuit

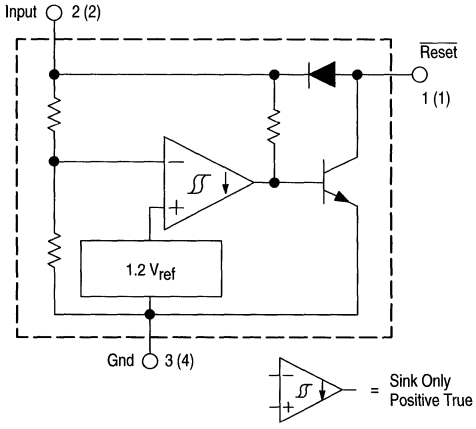
3

The MC34064 is an undervoltage sensing circuit specifically designed for use as a reset controller in microprocessor-based systems. It offers the designer an economical solution for low voltage detection with a single external resistor. The MC34064 features a trimmed-in-package bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation. The open collector reset output is capable of sinking in excess of 10 mA, and operation is guaranteed down to 1.0 V input with low standby current. These devices are packaged in 3-pin TO-226AA, 8-pin SO–8 and Micro–8 surface mount packages.

Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer and industrial equipment.

- Trimmed-In-Package Temperature Compensated Reference
- Comparator Threshold of 4.6 V at 25°C
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 10 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation with 1.0 V Input
- Low Standby Current
- Economical TO–226AA, SO–8 and Micro–8 Surface Mount Packages

Representative Block Diagram



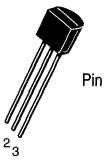
Pin numbers adjacent to terminals are for the 3–pin TO–226AA package.
Pin numbers in parenthesis are for the 8–lead packages.

This device contains 21 active transistors.

UNDERVOLTAGE SENSING CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

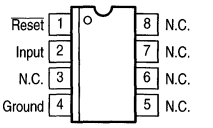
P SUFFIX
PLASTIC PACKAGE
CASE 29
(TO–226AA)



Pin 1. Reset
2. Input
3. Ground

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34064D–5	T_A = 0° to +70°C	SO–8
MC34064DM–5		Micro–8
MC34064P–5		TO–226AA
MC33064D–5	T_A = – 40° to +85°C	SO–8
MC33064DM–5		Micro–8
MC33064P–5		TO–226AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{in}	–1.0 to 10	V
$\overline{\text{Reset}}$ Output Voltage	V_O	10	V
$\overline{\text{Reset}}$ Output Sink Current (Note 1)	I_{Sink}	Internally Limited	mA
Clamp Diode Forward Current, Pin 1 to 2 (Note 1)	I_F	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	625	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	200	°C/W
D Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	625	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	200	°C/W
DM Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	520	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	240	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
MC34064		0 to +70	
MC33064		–40 to +85	
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3] unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	4.5	4.61	4.7	
Low State Output (V_{in} Decreasing)	V_{IL}	4.5	4.59	4.7	
Hysteresis	V_H	0.01	0.02	0.05	
$\overline{\text{RESET}}$ OUTPUT					
Output Sink Saturation	V_{OL}				V
(V_{in} = 4.0 V, I_{Sink} = 8.0 mA)		–	0.46	1.0	
(V_{in} = 4.0 V, I_{Sink} = 2.0 mA)		–	0.15	0.4	
(V_{in} = 1.0 V, I_{Sink} = 0.1 mA)		–	–	0.1	
Output Sink Current (V_{in}, $\overline{\text{Reset}}$ = 4.0 V)	I_{Sink}	10	27	60	mA
Output Off-State Leakage (V_{in}, $\overline{\text{Reset}}$ = 5.0 V)	I_{OH}	–	0.02	0.5	µA
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 10 mA)	V_F	0.6	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 6.5	–	–	V
Quiescent Input Current (V_{in} = 5.0 V)	I_{in}	–	390	500	µA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34064, –40°C for MC33064 T_{high} = +70°C for MC34064, +85°C for MC33064

3

Figure 1. $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

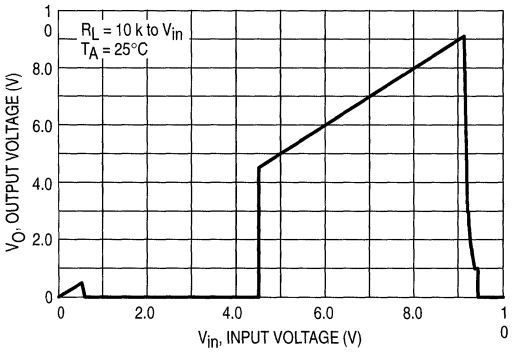


Figure 2. $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

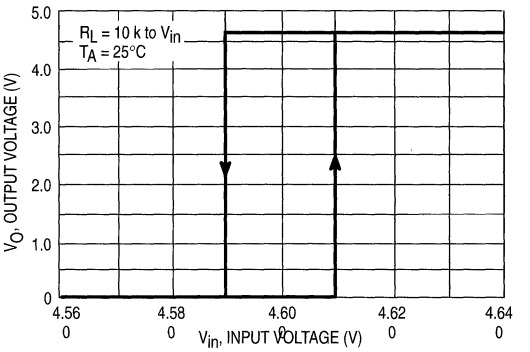


Figure 3. Comparator Threshold Voltage versus Temperature

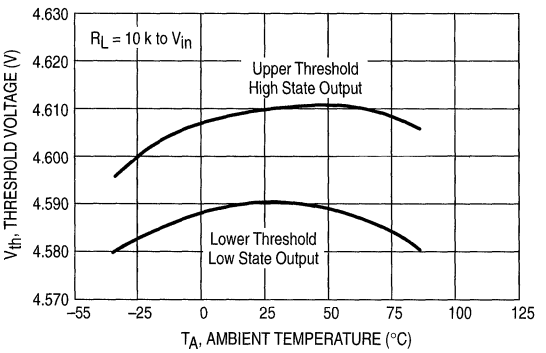


Figure 4. Input Current versus Input Voltage

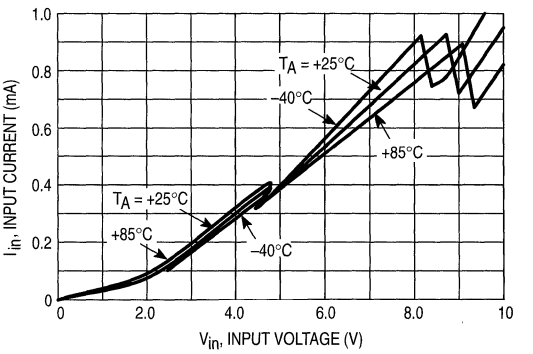


Figure 5. $\overline{\text{Reset}}$ Output Saturation versus Sink Current

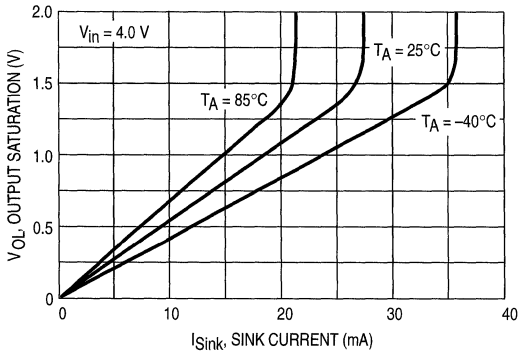


Figure 6. $\overline{\text{Reset}}$ Delay Time

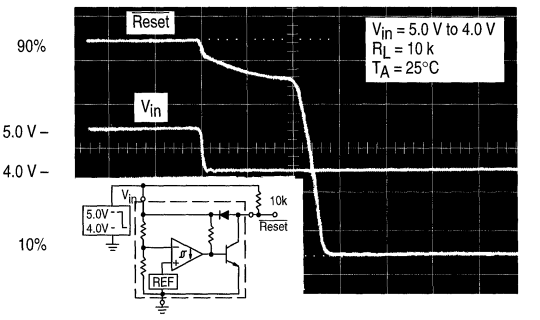


Figure 7. Clamp Diode Forward Current versus Voltage

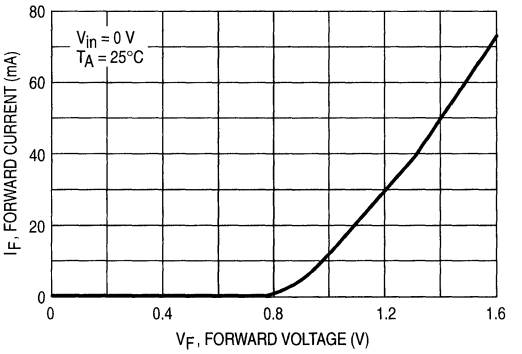
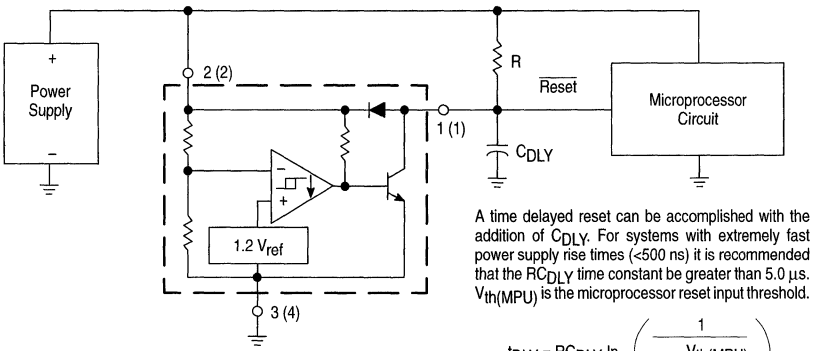


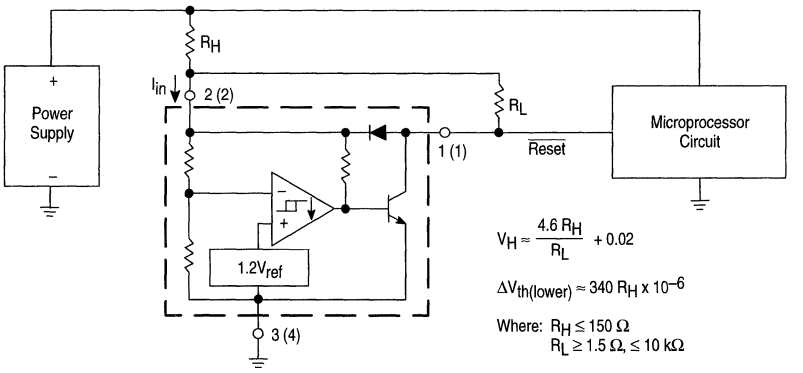
Figure 8. Low Voltage Microprocessor Reset



A time delayed reset can be accomplished with the addition of C_{DLY}. For systems with extremely fast power supply rise times (<500 ns) it is recommended that the RC_{DLY} time constant be greater than 5.0 μs. $V_{th(MPU)}$ is the microprocessor reset input threshold.

$$t_{DLY} = RC_{DLY} \ln \left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{in}}} \right)$$

Figure 9. Low Voltage Microprocessor Reset with Additional Hysteresis



$$V_H \approx \frac{4.6\,R_H}{R_L} + 0.02$$

$$\Delta V_{th(lower)} \approx 340\,R_H \times 10^{-6}$$

Where: $R_H \leq 150\ \Omega$
$R_L \geq 1.5\ \Omega, \leq 10\ k\Omega$

Comparator hysteresis can be increased with the addition of resistor R_H. The hysteresis equation has been simplified and does not account for the change of input current I_{in} as V_{CC} crosses the comparator threshold (Figure 4). An increase of the lower threshold $\Delta V_{th(lower)}$ will be observed due to I_{in} which is typically 340 μA at 4.59 V. The equations are accurate to ±10% with R_H less than 150 Ω and R_L between 1.5 kΩ and 10 kΩ.

Test Data			
V_H (mV)	ΔV_{th} (mV)	R_H (Ω)	R_L (kΩ)
20	0	0	0
51	3.4	10	1.5
40	6.8	20	4.7
81	6.8	20	1.5
71	10	30	2.7
112	10	30	1.5
100	16	47	2.7
164	16	47	1.5
190	34	100	2.7
327	34	100	1.5
276	51	150	2.7
480	51	150	1.5

3

Figure 10. Voltage Monitor

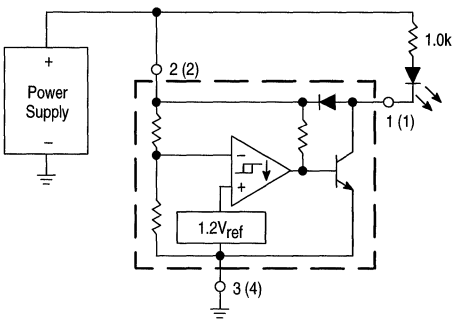


Figure 11. Solar Powered Battery Charger

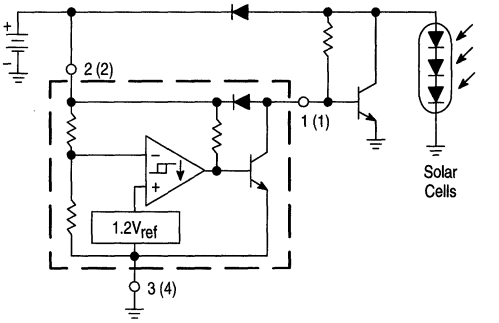
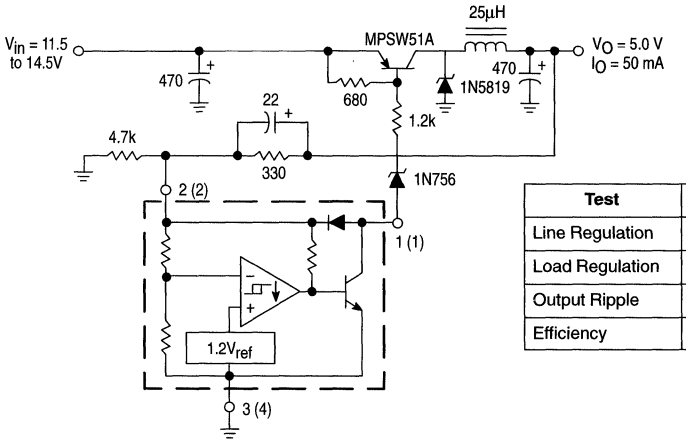
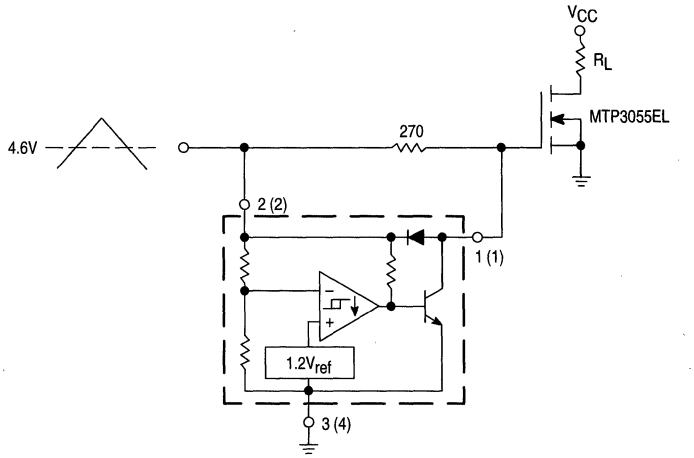


Figure 12. Low Power Switching Regulator



Test	Conditions	Results
Line Regulation	V_{in} = 11.5 V to 14.5 V, I_O = 50 mA	35 mV
Load Regulation	V_{in} = 12.6 V, I_O = 0 mA to 50 mA	12 mV
Output Ripple	V_{in} = 12.6 V, I_O = 50 mA	60 mVpp
Efficiency	V_{in} = 12.6 V, I_O = 50 mA	77%

Figure 13. MOSFET Low Voltage Gate Drive Protection



Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.6 V threshold of the MC34064, its output grounds the gate of the L^2 MOSFET.

MOTOROLA

MC34065
MC33065

3

High Performance Dual Channel Current Mode Controller

The MC34065 is a high performance, fixed frequency, dual current mode controllers. It is specifically designed for off–line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. This integrated circuit feature a unique oscillator for precise duty cycle limit and frequency control, a temperature compensated reference, two high gain error amplifiers, two current sensing comparators, Drive Output 2 Enable pin, and two high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, and a latch for single pulse metering of each output.

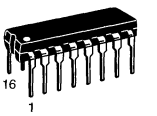
The MC34065 and MC33065 are available in dual–in–line and surface mount packages.

- Unique Oscillator for Precise Duty Cycle Limit and Frequency Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Separate Latching PWMs for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- Drive Output 2 Enable Pin
- Two High Current Totem Pole Outputs
- Input Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current

HIGH PERFORMANCE DUAL CHANNEL CURRENT MODE CONTROLLER

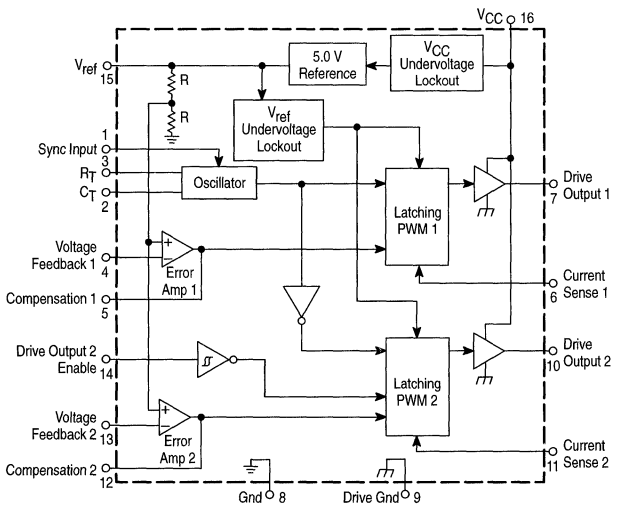
SEMICONDUCTOR TECHNICAL DATA

P SUFFIX
PLASTIC PACKAGE
CASE 648



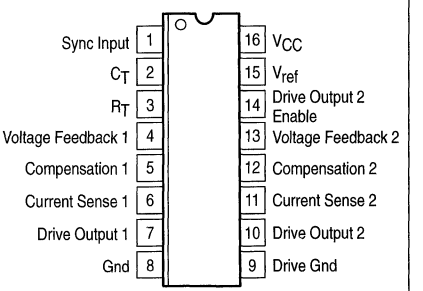
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

Representative Block Diagram



This device contains 208 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34065DW	T_A = 0° to +70°C	SO–16L
MC34065P		Plastic DIP
MC33065DW	T_A = –40° to +85°C	SO–16L
MC33065P		Plastic DIP

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	50	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense, Enable, and Voltage Feedback Inputs	V_{in}	–0.3 to +5.5	V
Sync Input High State (Voltage) Low State (Reverse Current)	 V_{IH} I_{IL}	 5.5 –5.0	 V mA
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics DW Suffix, Plastic Package Case 751G Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air P Suffix, Plastic Package Case 648 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34065 MC33065	T_A	 0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 11 V to 15 V)	Reg_{line}	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	3.0	25	mV
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.85	–	5.15	V
Output Short Circuit Current	I_{SC}	30	100	–	mA
OSCILLATOR AND PWM SECTIONS					
Total Frequency Variation over Line and Temperature V_{CC} = 11 V to 15 V, T_A = T_{low} to T_{high} MC34065 MC33065	f_{osc}	 46.5 45	 49 49	 51.5 53	kHz
Frequency Change with Voltage (V_{CC} = 11 V to 15 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	%
Duty Cycle at each Output Maximum Minimum	 DC_{max} DC_{min}	 46 –	 49.5 –	 52 0	%
Sync Input Current High State (V_{in} = 2.4 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 – –	 170 80	 250 160	μA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible:
T_{low} = 0°C for the MC34065 T_{high} = +70°C for MC34065
T_{low} = –40°C for the MC33065 T_{high} = +85°C for MC33065
4. This parameter is measured at the latch trip point with V_{FB} = 0 V
5. Comparator gain is defined as $AV = \frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense}}$

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIERS					
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	–1.0	μA
Open Loop Voltage Gain (V_O = 2.0 to 4.0 V)	A_{VOL}	65	100	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 11 V to 15 V)	PSRR	60	90	–	dB
Output Current					mA
Source (V_O = 3.0 V, V_{FB} = 2.3 V)	I_{source}	–0.45	–1.0	–	
Sink (V_O = 1.2 V, V_{FB} = 2.7 V)	I_{sink}	2.0	12	–	
Output Voltage Swing					V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}	–	0.8	1.1	
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 and 5)	A_V	2.75	3.0	3.25	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	430	480	530	mV
Input Bias Current	I_{IB}	–	–2.0	–10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLN(In/Out)}$	–	150	300	ns
DRIVE OUTPUT 2 ENABLE PIN					
Enable Pin Voltage					V
High State (Output 2 Enabled)	V_{IH}	3.5	–	V_{ref}	
Low State (Output 2 Disabled)	V_{IL}	0	–	1.5	
Low State Input Current (V_{IL} = 0 V)	I_{IB}	100	250	400	μA
DRIVE OUTPUTS					
Output Voltage					V
Low State (I_{sink} = 20 mA)	V_{OL}	–	0.1	0.4	
(I_{sink} = 200 mA)		–	1.6	2.5	
High State (I_{source} = 20 mA)	V_{OH}	13	13.5	–	
(I_{source} = 200 mA)		12	13.4	–	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	28	150	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	25	150	ns
UNDERVOLTAGE LOCKOUT SECTION					
Startup Threshold	V_{th}	13	14	15	V
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$	9.0	10	11	V
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Startup (V_{CC} = 12 V)		–	0.6	1.0	
Operating (Note 2)		–	20	25	
Power Supply Zener Voltage (I_{CC} = 30 mA)	V_Z	15.5	17	19	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible:
T_{low} = 0°C for the MC34065 T_{high} = +70°C for MC34065
T_{low} = –40°C for the MC33065 T_{high} = +85°C for MC33065
4. This parameter is measured at the latch trip point with V_{FB} = 0 V
5. Comparator gain is defined as $AV = \frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense}}$

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Sync Input	A narrow rectangular waveform applied to this input will synchronize the oscillator. A dc voltage within the range of 2.4 V to 5.5 V will inhibit the oscillator.
2	C_T	Timing capacitor C_T connects from this pin to ground setting the free–running oscillator frequency range.
3	R_T	Resistor R_T connects from this pin to ground precisely setting the charge current for C_T. R_T must be between 4.0 k and 16 k.
4	Voltage Feedback 1	This pin is the inverting input of Error Amplifier 1. It is normally connected to the switching power supply output through a resistor divider.
5	Compensation 1	This pin is the output of Error Amplifier 1 and is made available for loop compensation.
6	Current Sense 1	A voltage proportional to the inductor current is connected to this input. PWM 1 uses this information to terminate conduction of output switch Q1.
7	Drive Output 1	This pin directly drives the gate of a power MOSFET Q1. Peak currents up to 1.0 A are sourced and sunk by this pin.
8	Gnd	This pin is the control circuitry ground return and is connected back to the source ground.
9	Drive Gnd	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
10	Drive Output 2	This pin directly drives the gate of a power MOSFET Q2. Peak currents up to 1.0 A are sourced and sunk by this pin.
11	Current Sense 2	A voltage proportional to inductor current is connected to this input. PWM 2 uses this information to terminate conduction of output switch Q2.
12	Compensation 2	This pin is the output of Error Amplifier 2 and is made available for loop compensation.
13	Voltage Feedback 2	This pin is the inverting input of Error Amplifier 2. It is normally connected to the switching power supply output through a resistor divider.
14	Drive Output 2 Enable	A logic low at this input disables Drive Output 2.
15	V_{ref}	This is the 5.0 V reference output. It can provide bias for any additional system circuitry.
16	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after startup is 11 V to 15.5 V.

Figure 1. Timing Resistor versus Oscillator Frequency

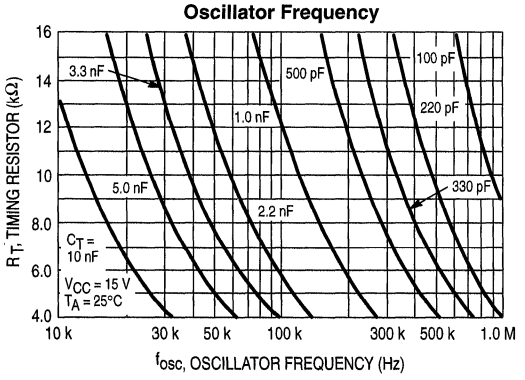


Figure 2. Maximum Output Duty Cycle versus Oscillator Frequency

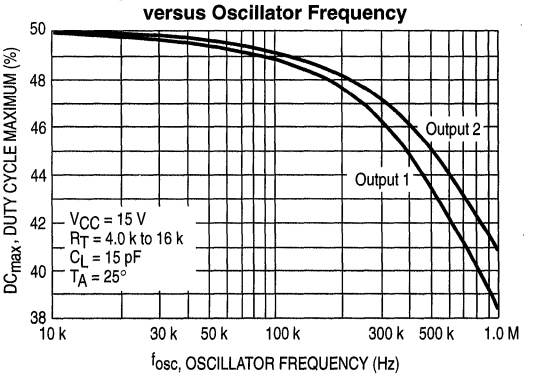


Figure 3. Error Amp Small–Signal Transient Response

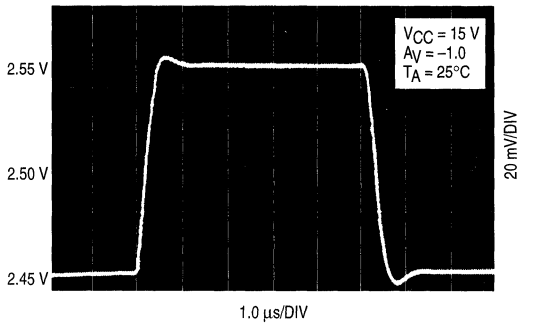


Figure 4. Error Amp Large–Signal Transient Response

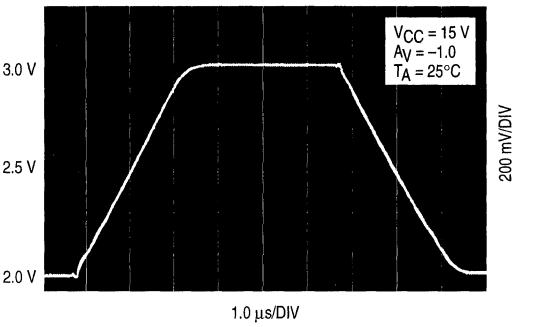


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

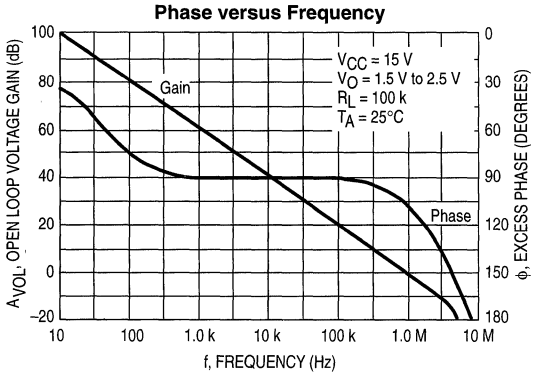


Figure 6. Current Sense Input Threshold versus Error Amp Output Voltage

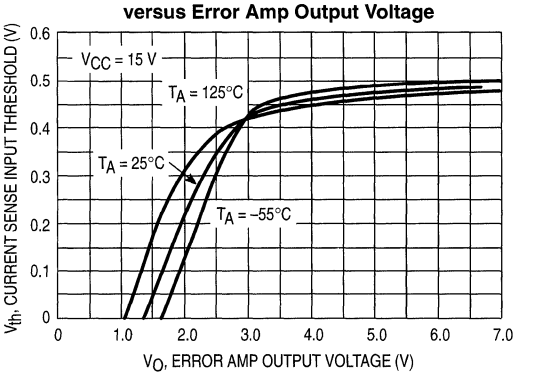


Figure 7. Reference Voltage Change versus Source Current

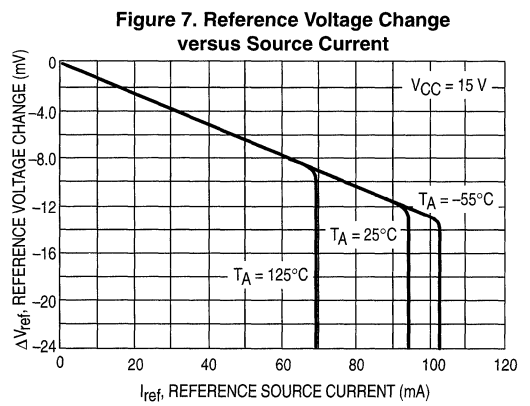
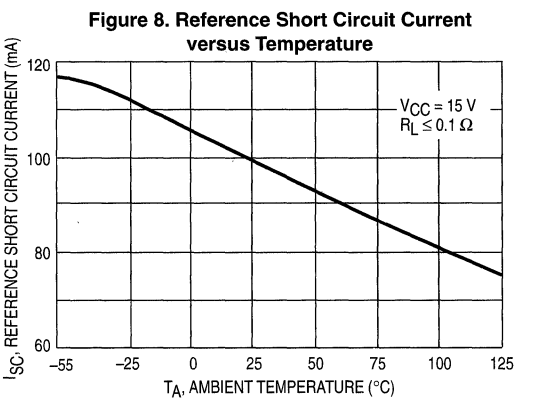


Figure 8. Reference Short Circuit Current versus Temperature



3

Figure 9. Reference Load Regulation

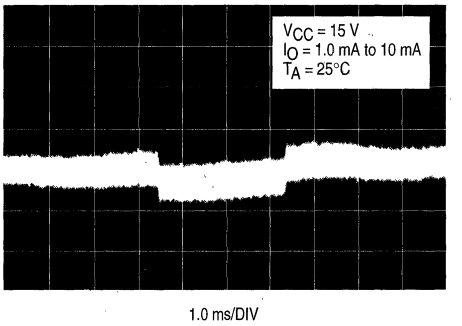


Figure 10. Reference Line Regulation

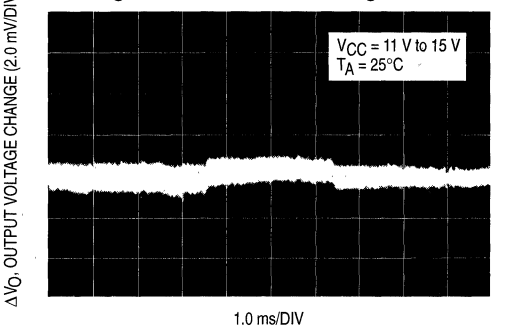


Figure 11. Output Saturation Voltage versus Load Current

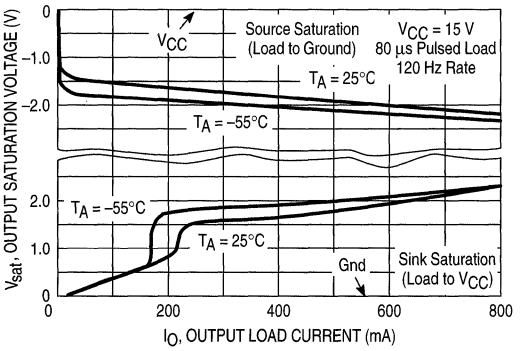


Figure 12. Output Waveform

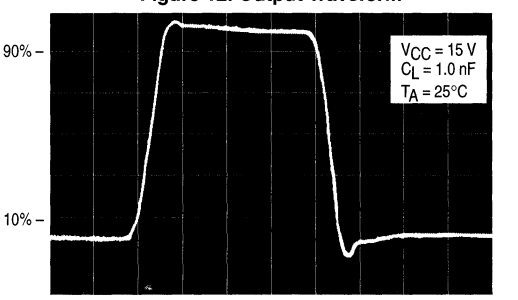


Figure 13. Output Cross Conduction Current

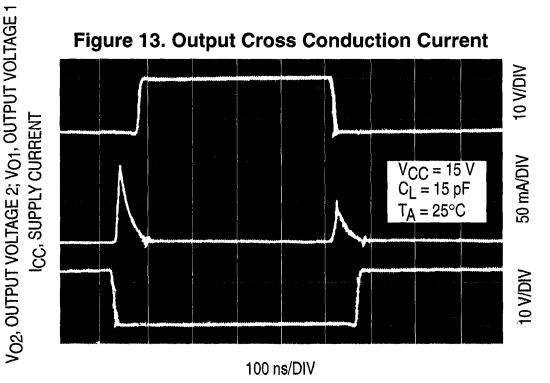
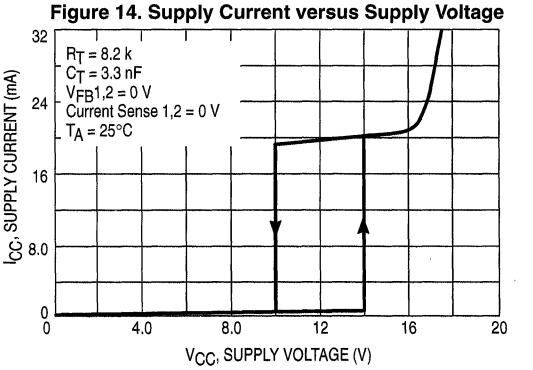


Figure 14. Supply Current versus Supply Voltage



OPERATING DESCRIPTION

The MC34065 series are high performance, fixed frequency, dual channel current mode controllers specifically designed for Off–Line and dc–to–dc converter applications. These devices offer the designer a cost effective solution with minimal external components where independent regulation of two power converters is required. The Representative Block Diagram is shown in Figure 15. Each channel contains a high gain error amplifier, current sensing comparator, pulse width modulator latch, and totem pole output driver. The oscillator, reference regulator, and undervoltage lock–out circuits are common to both channels.

Oscillator

The unique oscillator configuration employed features precise frequency and duty cycle control. The frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink, generating a symmetrical 50 percent duty cycle waveform at Pin 2. The oscillator peak and valley thresholds are 3.5 V and 1.6 V respectively. The source/sink current magnitude is controlled by resistor R_T. For proper operation over temperature it must be in the range of 4.0 kΩ to 16 kΩ as shown in Figure 1.

As C_T charges and discharges, an internal blanking pulse is generated that alternately drives the center inputs of the upper and lower NOR gates high. This, in conjunction with a precise amount of delay time introduced into each channel, produces well defined non–overlapping output duty cycles. Output 2 is enabled while C_T is charging, and Output 1 is enabled during the discharge. Figure 2 shows the Maximum Output Duty Cycle versus Oscillator Frequency. Note that even at 500 kHz, each output is capable of approximately 44% on–time, making this controller suitable for high frequency power conversion applications.

In many noise sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal as shown in Figure 17. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 16, the rising edge of the clock signal applied to the Sync input, terminates charging of C_T and Drive Output 2 conduction. By tailoring the clock waveform symmetry, accurate duty cycle clamping of either output can be achieved. A circuit method for this, and multi–unit synchronization, is shown in Figure 18.

Error Amplifier

Each channel contains a fully–compensated Error Amplifier with access to the inverting input and output. The amplifier features a typical dc voltage gain of 100 dB, and a unity gain bandwidth of 1.0 MHz with 71° of phase margin (Figure 5). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input through a resistor divider. The maximum input bias current is –1.0 μA which will cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 5, 12) is provided for external loop compensation. The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no pulses appear at the Drive Output (Pin 7, 10) when the error amplifier output is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 20, 21).

The minimum allowable Error Amp feedback resistance is limited by the amplifier's source current (0.5 mA) and the output voltage (V_{OH}) required to reach the comparator's 0.5 V clamp level with the inverting input at ground. This condition happens during initial system startup or when the sensed output is shorted:

$$R_{f(min)} \approx \frac{3.0\ (0.5\ V)\ +\ 1.4\ V}{0.5\ mA} = 5800\ \Omega$$

Current Sense Comparator and PWM Latch

The MC34065 operates as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output. Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator–PWM Latch configuration used ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting a ground–referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6, 11) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 5, 12 where:

$$I_{pk} = \frac{V_{(Pin\ 5,\ 12)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 0.5 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{0.5\ V}{R_S}$$

When designing a high power switching regulator it may be desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense input with a time constant that approximates the spike duration will usually eliminate the instability, refer to Figure 24.

Figure 15. Representative Block Diagram

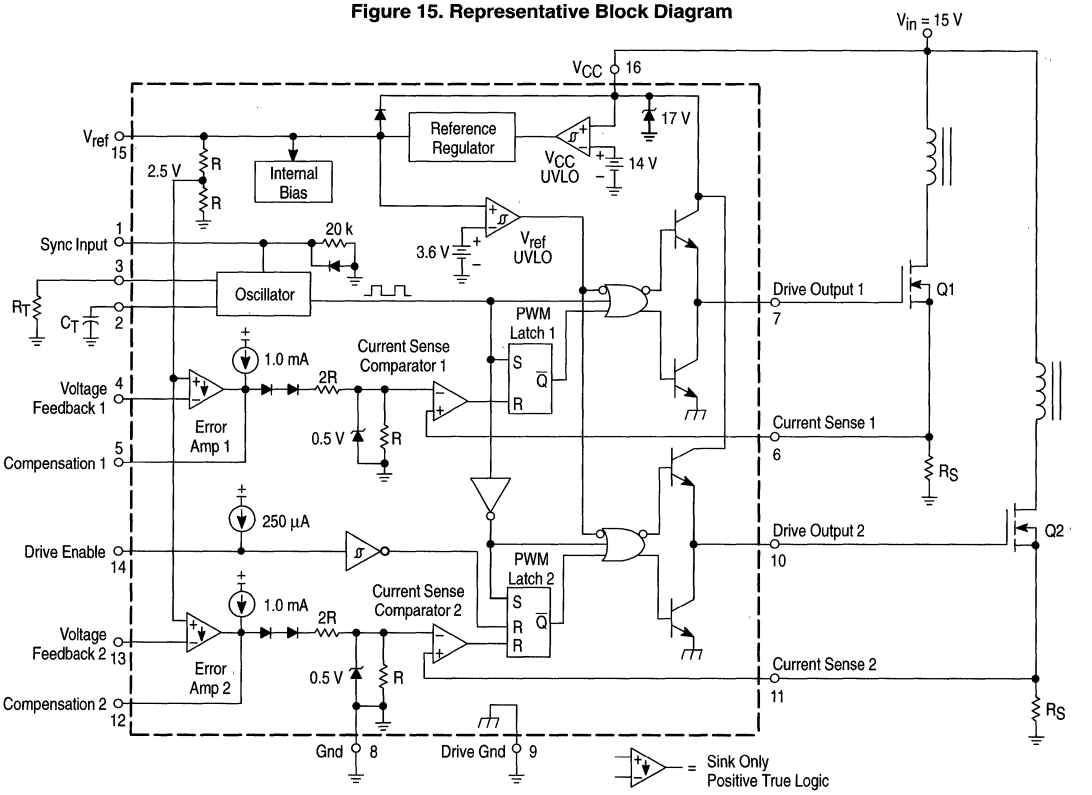
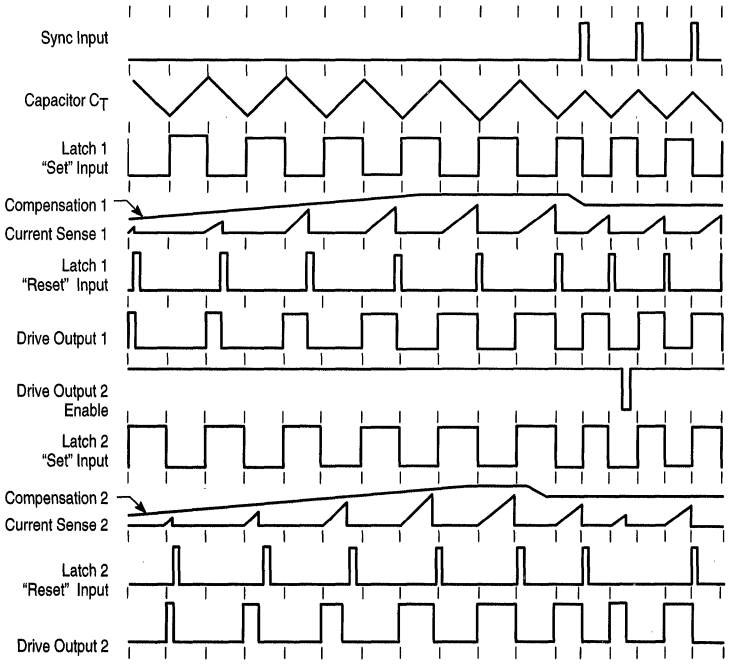


Figure 16. Timing Diagram



Undervoltage Lockout

Two Undervoltage Lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stages are enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14 V and 10 V respectively. The hysteresis and low startup current makes these devices ideally suited to off–line converter applications where efficient bootstrap startup techniques are required (Figure 28). The V_{ref} comparator disables the Drive Outputs until the internal circuitry is functional. This comparator has upper and lower thresholds of 3.6 V and 3.4 V. A 17 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC and power MOSFET gate from excessive voltage that can occur during system startup. The guaranteed minimum operating voltage after turn–on is 11 V.

Drive Outputs and Drive Ground

Each channel contains a single totem–pole output stage that is specifically designed for direct drive of power MOSFETs. The Drive Outputs are capable of up to ±1.0 A peak current with a typical rise and fall time of 28 ns with a 1.0 nF load. Internal circuitry has been added to keep the outputs in a sinking mode whenever an Undervoltage Lockout is active. This characteristic eliminates the need for an external pull–down resistor. Cross–conduction current in the totem–pole output stage has been minimized for high speed operation, as shown in Figure 13. The average added power due to cross–conduction with V_{CC} = 15 V is only 60 mW at 500 kHz.

Although the Drive Outputs were optimized for MOSFETs, they can easily supply the negative base current required by bipolar NPN transistors for enhanced turn–off (Figure 25). The outputs do not contain internal current limiting, therefore an external series resistor may be required to prevent the peak output current from exceeding the 1.0 A maximum rating. The sink saturation (V_{OL}) is less than 0.4 V at 100 mA.

A separate Drive Ground pin is provided and, with proper implementation, will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. Figure 23 shows the proper ground connections required for current sensing power MOSFET applications.

Drive Output 2 Enable Pin

This input is used to enable Drive Output 2. Drive Output 1 can be used to control circuitry that must run continuously such as volatile memory and the system clock, or a remote controlled receiver, while Drive Output 2 controls the high power circuitry that is occasionally turned off.

Reference

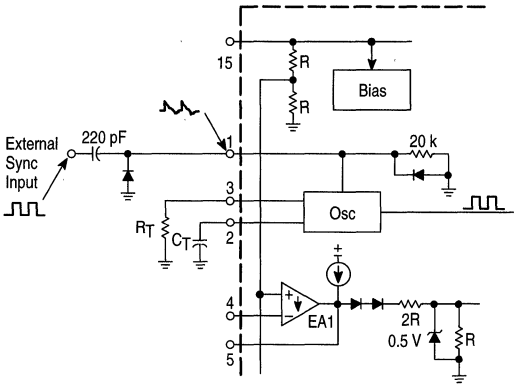
The 5.0 V bandgap reference is trimmed to ±2.0% tolerance at T_J = 25°C. The reference has short circuit protection and is capable of providing in excess of 30 mA for powering any additional control system circuitry.

Design Considerations

Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC} and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage–divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

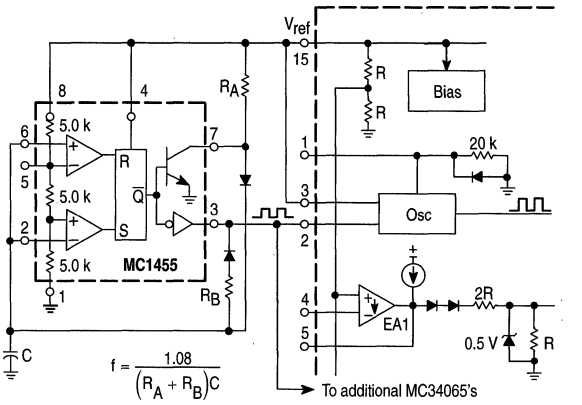
3

Figure 17. External Clock Synchronization



The external diode clamp is required if the negative Sync current is greater than –5.0 mA.

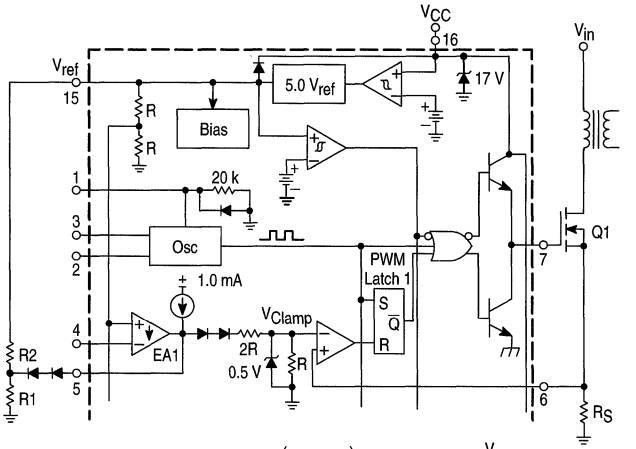
Figure 18. External Duty Cycle Clamp and Multi–Unit Synchronization



$$f = \frac{1.08}{(R_A + R_B)C}$$

$$D_{max}\ \text{Drive Output 1} = \frac{R_B}{R_A + R_B} \qquad D_{max}\ \text{Drive Output 2} = \frac{R_A}{R_A + R_B}$$

Figure 19. Adjustable Reduction of Clamp Level



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R2}{R1} + 1\right)} + 0.33 \times 10^{-3}\left(\frac{R1R2}{R1 + R2}\right) \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Where: $0 \le V_{Clamp} \le 0.5\ V$

Figure 20. Soft–Start Circuit

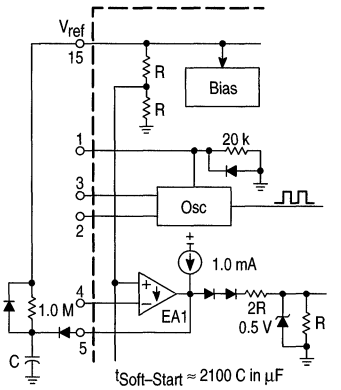
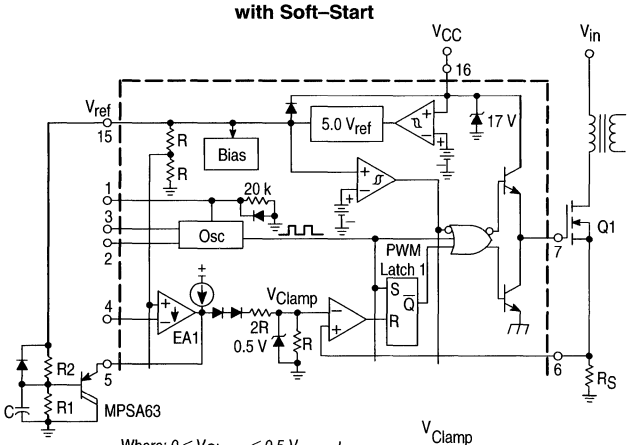


Figure 21. Adjustable Reduction of Clamp Level with Soft–Start



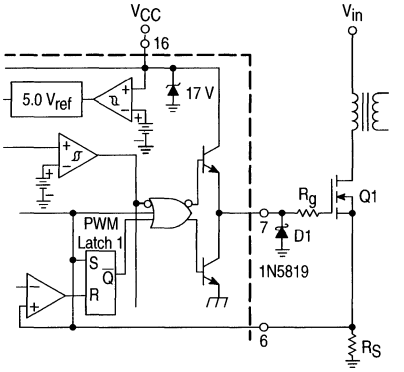
Where: $0 \le V_{Clamp} \le 0.5\ V$

$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R2}{R1} + 1\right)}$$

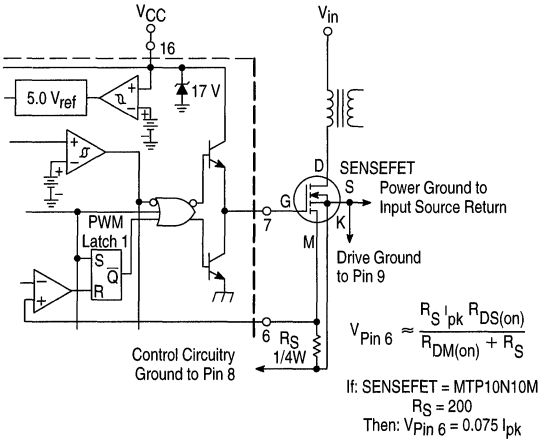
$$t_{Soft\text{-}Start} = \ln\left(\frac{1}{1 - \frac{V_C}{3\,V_{Clamp}}}\right) C\,\frac{R1R2}{R1 + R2}$$

Figure 22. MOSFET Parasitic Oscillations



Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D1 is required if circuit ringing drives the output pin below ground.

Figure 23. Current Sensing Power MOSFET



$$V_{Pin\ 6} \approx \frac{R_S\, I_{pk}\, R_{DS(on)}}{R_{DM(on)} + R_S}$$

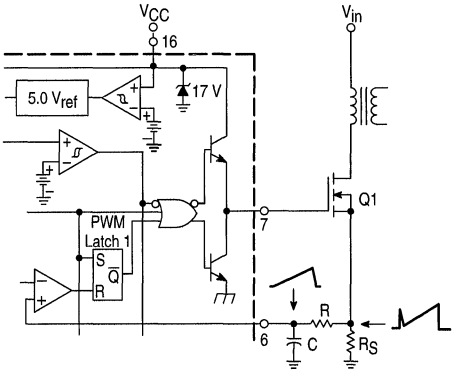
If: SENSEFET = MTP10N10M

$R_S = 200$

Then: $V_{Pin\ 6} = 0.075\ I_{pk}$

Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

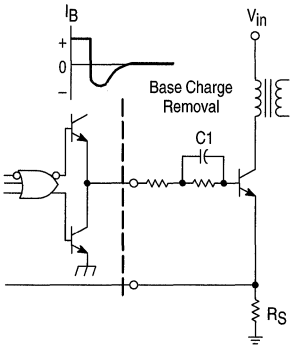
Figure 24. Current Waveform Spike Suppression



The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

3

Figure 25. Bipolar Transistor Drive



The totem–pole outputs can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C1.

Figure 26. Isolated MOSFET Drive

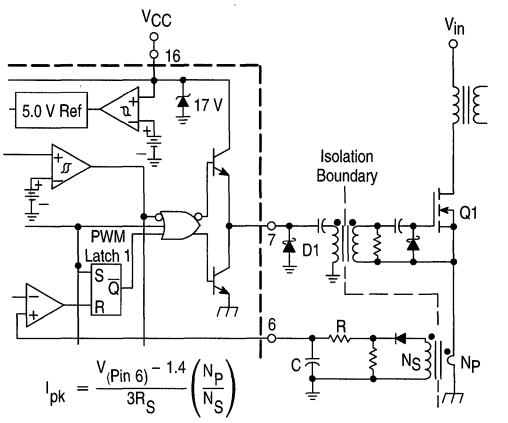
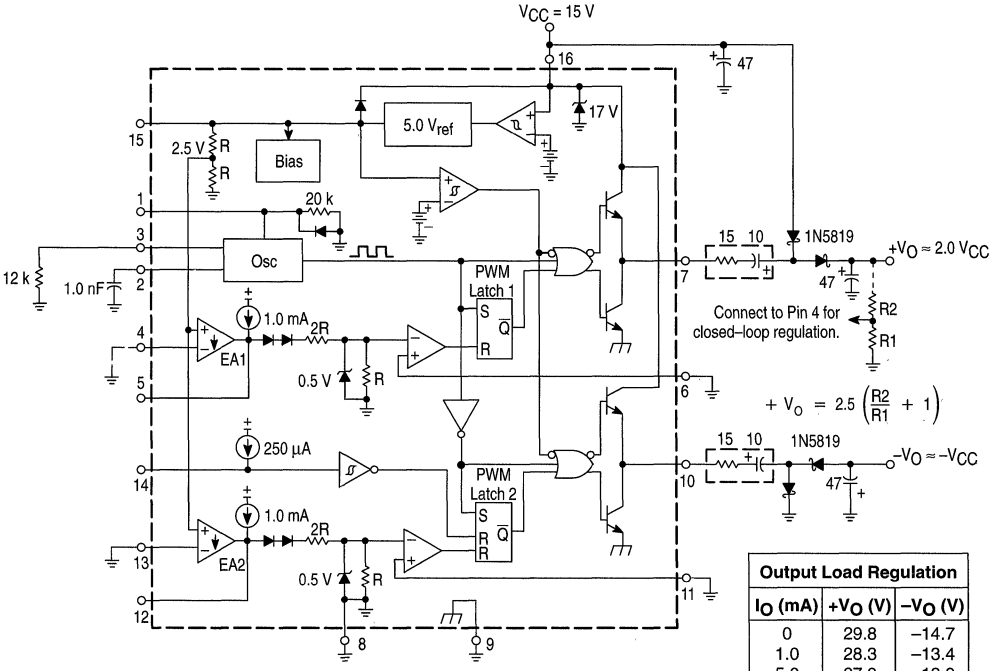


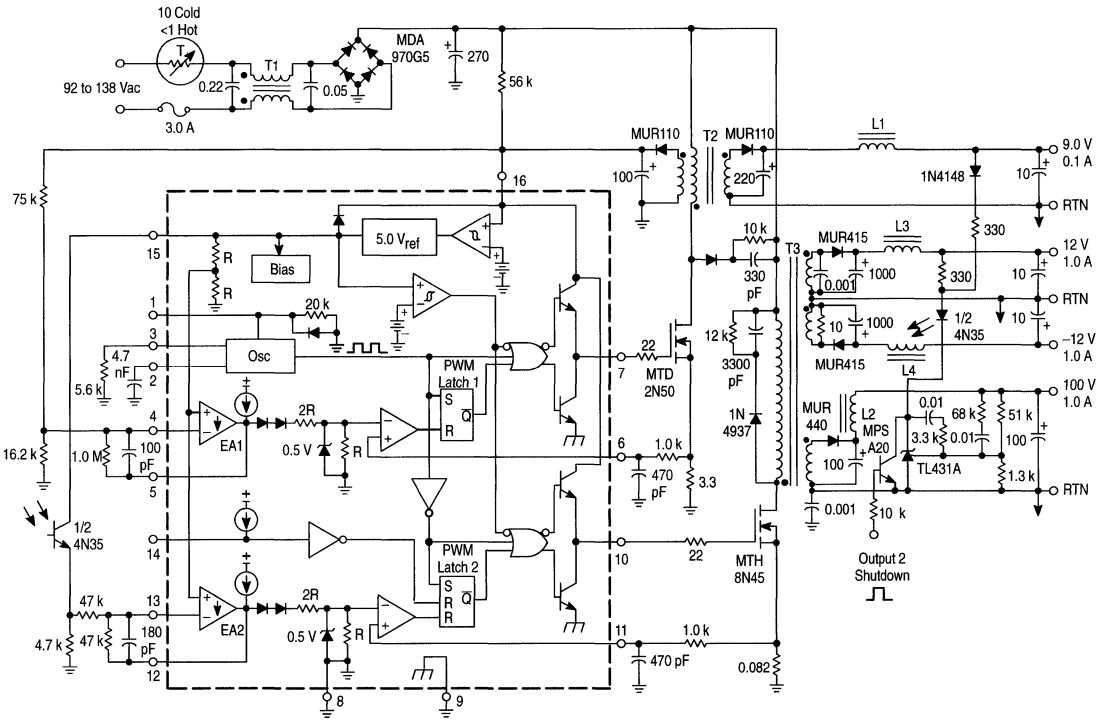
Figure 27. Dual Charge Pump Converter



Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	29.8	–14.7
1.0	28.3	–13.4
5.0	27.9	–12.9
10	27.5	–12.5
50	24.4	–9.5

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The positive output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

Figure 28. 125 Watt Off–Line Converter



Test	Conditions	Results
Line Regulation 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 92 to 138 Vac I_O = 1.0 A I_O = ±1.0 A I_O = 0.1 A	 Δ = 40 mV or ±0.02% Δ = 32 mV or ±0.13% Δ = 55 mV or ±0.31%
Load Regulation 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac I_O = 0.25 A to 1.0 A I_O = ±0.25 A to ±1.0 A I_O = 0.08 A to 0.1 A	 Δ = 50 mV or ±0.025% Δ = 320 mV or ±1.2% Δ = 234 mV or ±1.3%
Output Ripple 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac I_O = 1.0 A I_O = ±1.0 A I_O = 0.1 A	 40 mVpp 100 mVpp 60 mVpp
Short Circuit Current 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac, R_L = 0.1 Ω	 4.3 A 17 A Output Hiccups
Efficiency	Vin = 115 Vac, PO = 125 W	86%

T1 – 468 μH per section at 2.5 A, Coilcraft E3496A.

T2 – Primary: 156 Turns, #34 AWG
Primary Feedback: 19 Turns, #34 AWG
Secondary: 17 Turns, #28 AWG
Core: TDK H7C1EE22–Z
Bobbin: BE22–6H
Gap: ≈0.001″ for a primary inductance of 6.8 mH

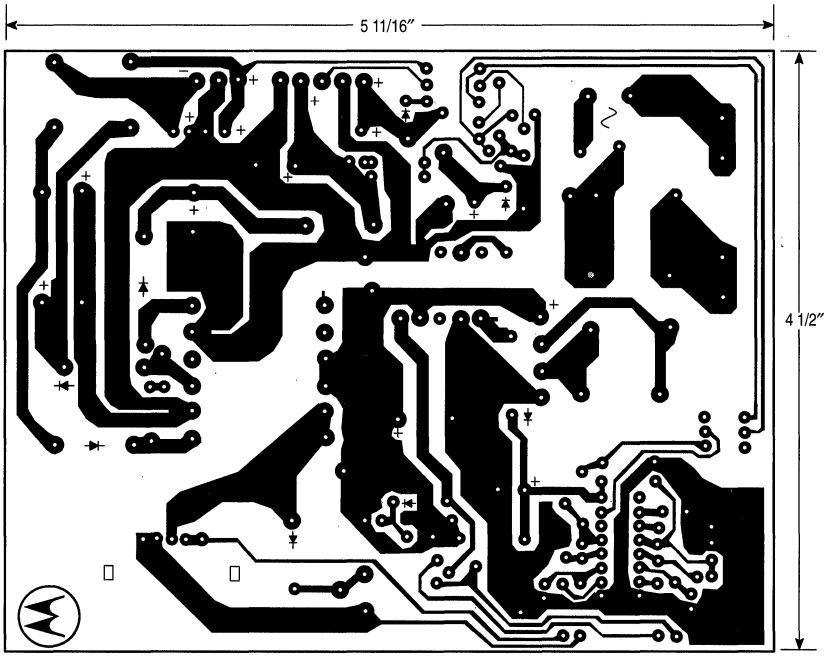
T3 – Primary: 56 Turns, #23 AWG (2 strands) Bifiliar Wound
Secondary: ±12 V, 4 Turns, #23 AWG (4 strands) Quadfiliar Wound
Secondary 100 V: 32 Turns, #23 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EEC 40–3C8
Bobbin: Ferroxcube 40–1112CP
Gap: ≈0.030″ for a primary inductance of 212 μH

L1, L3, L4 – 25 μH at 1.0 A, Coilcraft Z7157.

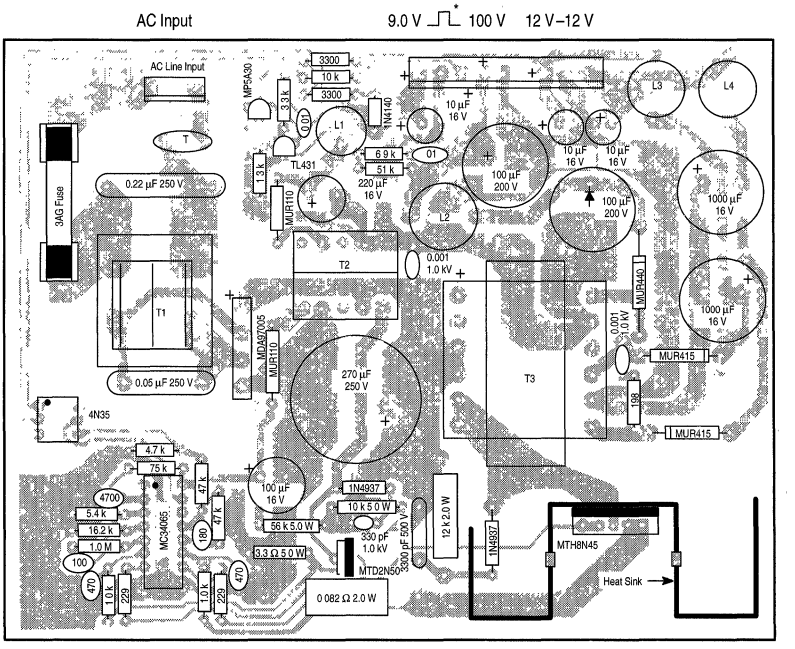
L2 – 10 μH at 3.0 A, Coilcraft PCV–0–010–03.

3

Figure 29. 125 Watt Off–Line Converter



Circuit View



Component View

*100 V and ±12 V Shutdown

MOTOROLA

High Performance Dual Channel Current Mode Controllers

MC34065-H, L
MC33065-H, L

3

HIGH PERFORMANCE DUAL CHANNEL CURRENT MODE CONTROLLERS

SEMICONDUCTOR TECHNICAL DATA

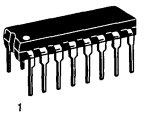
The MC34065–H,L series are high performance, fixed frequency, dual current mode controllers. They are specifically designed for off–line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a unique oscillator for precise duty cycle limit and frequency control, a temperature compensated reference, two high gain error amplifiers, two current sensing comparators, Drive Output 2 Enable pin, and two high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, and a latch for single pulse metering of each output. These devices are available in dual–in–line and surface mount packages.

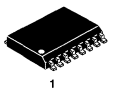
The MC34065–H has UVLO thresholds of 14 V (on) and 10 V (off), ideally suited for off–line converters. The MC34065–L is tailored for lower voltage applications having UVLO thresholds of 8.4 V (on) and 7.8 V (off).

- Unique Oscillator for Precise Duty Cycle Limit and Frequency Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Separate Latching PWMs for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- Drive Output 2 Enable Pin
- Two High Current Totem Pole Outputs
- Input Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current

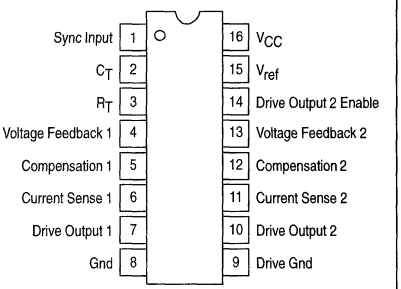
P SUFFIX
PLASTIC PACKAGE
CASE 648



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

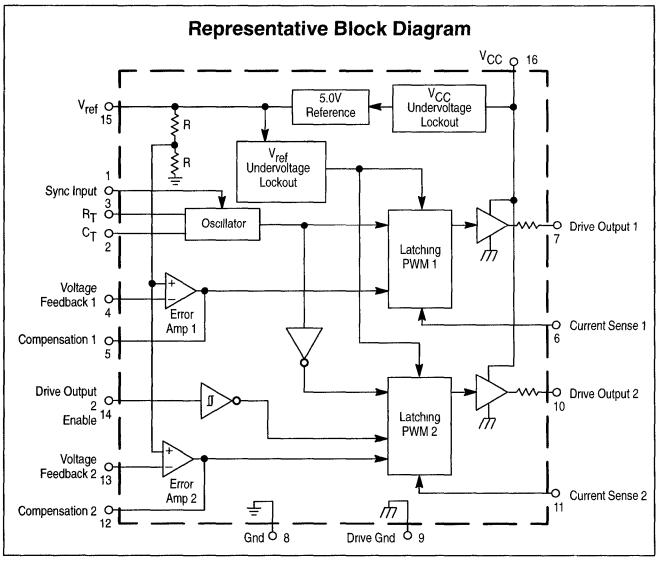


PIN CONNECTIONS



(Top View)

Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34065DW–H	T_A = 0° to +70°C	SO–16L
MC34065DW–L		
MC34065P–H		Plastic DIP
MC34065P–L		
MC33065DW–H	T_A = –40° to +85°C	SO–16L
MC33065DW–L		
MC33065P–H		Plastic DIP
MC33065P–L		

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Output Current, Source or Sink (Note 1)	I_O	400	mA
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense, Enable, and Voltage Feedback Inputs	V_{in}	– 0.3 to +5.5	V
Sync Input High State (Voltage) Low State (Reverse Current)	 V_{IH} I_{IL}	 +5.5 – 5.0	 V mA
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics DW Suffix, Plastic Package Case 751G Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air P Suffix, Plastic Package Case 648 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta}JA$ P_D $R_{\theta}JA$	 862 145 1.25 100	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34065 MC33065	T_A	 0 to +70 – 40 to +85	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies to [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.85	5.0	5.13	V
Line Regulation (V_{CC} = 11 V to 20 V)	Reg_{line}	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 10 mA, V_{CC} = 20 V)	Reg_{load}	–	3.0	25	mV
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.8	–	5.15	V
Output Short Circuit Current	I_{SC}	30	100	–	mA
OSCILLATOR AND PWM SECTIONS					
Total Frequency Variation over Line and Temperature V_{CC} = 11 V to 20 V, T_A = T_{low} to T_{high} MC34065 MC33065	f_{osc}	 46.5 45	 49 49	 51.5 53	kHz
Frequency Change with Voltage (V_{CC} = 11 V to 20 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	%
Duty Cycle at each Output Maximum Minimum	 DC_{max} DC_{min}	 46 –	 49.5 –	 52 0	%
Sync Input Current High State (V_{in} = 2.4 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 – –	 170 80	 250 160	μA
ERROR AMPLIFIERS					
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	– 1.0	μA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	100	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 11 V to 20 V)	PSRR	60	90	–	dB
Output Current Source (V_O = 3.0 V, V_{FB} = 2.3 V) Sink (V_O = 1.2 V, V_{FB} = 2.7 V)	 I_{source} I_{sink}	 0.45 2.0	 1.0 12	 – –	mA
Output Voltage Swing High State (R_L = 15 k to ground, V_{FB} = 2.3 V) Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	 V_{OH} V_{OL}	 5.0 –	 6.2 0.8	 – 1.1	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies to [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 and 5)	A_V	2.75	3.0	3.25	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	V
Input Bias Current	I_{IB}	–	– 2.0	– 10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLN(In/Out)}$	–	150	300	ns
DRIVE OUTPUT 2 ENABLE PIN					
Enable Pin Voltage – High State (Output 2 Enabled) – Low State (Output 2 Disabled)	V_{IH} V_{IL}	3.5 0	– –	V_{ref} 1.5	V
Low State Input Current (V_{IL} = 0 V)	I_{IB}	100	250	400	μA
DRIVE OUTPUTS					
Output Voltage – Low State (I_{sink} = 20 mA) (I_{sink} = 200 mA) – High State (I_{source} = 20 mA) (I_{source} = 200 mA)	V_{OL} V_{OH} 	– 1.6 12.8 10	0.3 2.4 13.3 11.2	0.5 3.0 – 12.3	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION					
Startup Threshold (V_{CC} Increasing) –L Suffix –H Suffix	V_{th}	 7.8 13	 8.4 14	 9.0 15	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing) –L Suffix –H Suffix	$V_{CC(min)}$	 7.2 9.0	 7.8 10	 8.4 11	V
TOTAL DEVICE					
Power Supply Current Startup –L Suffix (V_{CC} = 6.0 V) –H Suffix (V_{CC} = 12 V) Operating (Note 2)	I_{CC}	 – – –	 0.4 0.6 20	 0.8 1.0 25	mA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible:
T_{low} = 0°C for the MC34065 T_{high} = +70°C for MC34065
T_{low} = –40°C for the MC33065 T_{high} = +85°C for MC33065
4. This parameter is measured at the latch trip point with V_{FB} = 0 V
5. Comparator gain is defined as $AV = \frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense}}$

Figure 1. Timing Resistor versus Oscillator Frequency

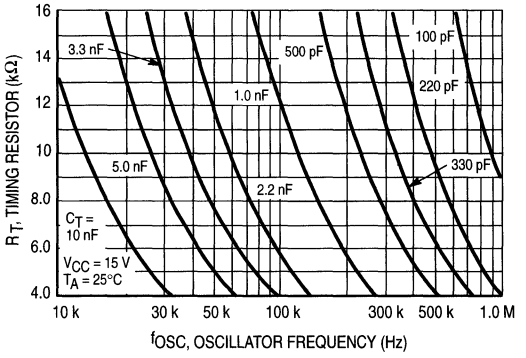


Figure 2. Maximum Output Duty Cycle versus Oscillator Frequency

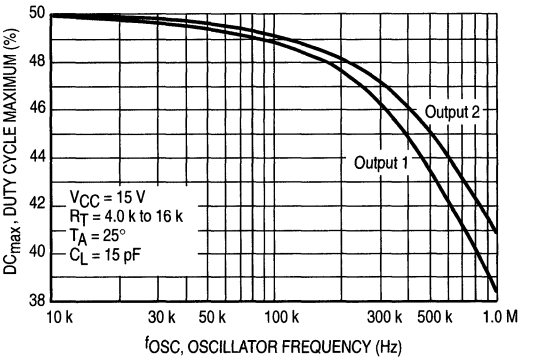


Figure 3. Error Amp Small–Signal Transient Response

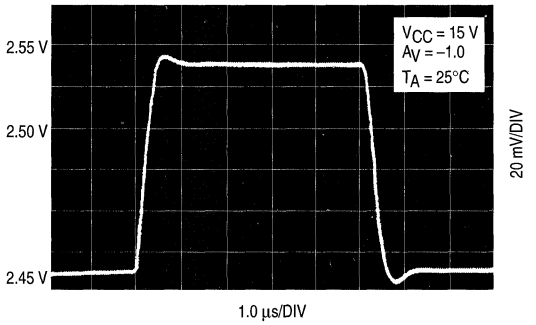


Figure 4. Error Amp Large–Signal Transient Response

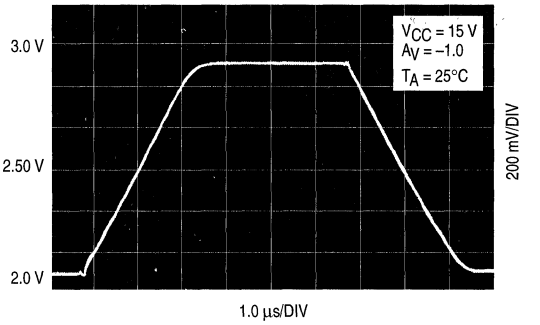


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

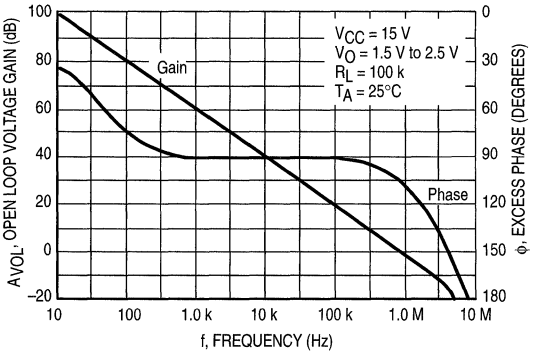


Figure 6. Current Sense Input Threshold versus Error Amp Output Voltage

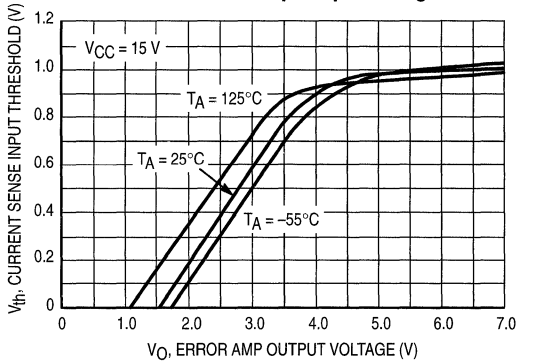


Figure 7. Reference Voltage Change versus Source Current

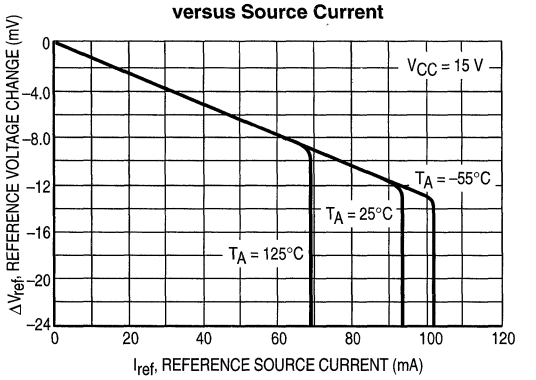


Figure 8. Reference Short Circuit Current versus Temperature

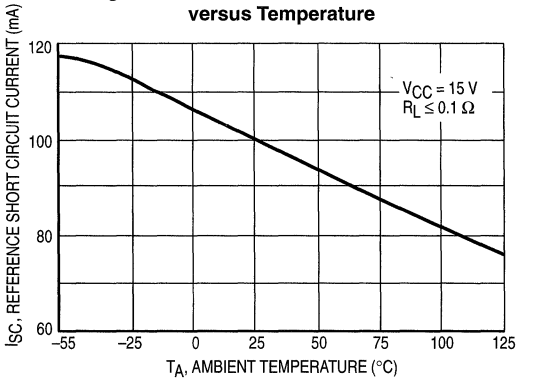


Figure 9. Reference Load Regulation

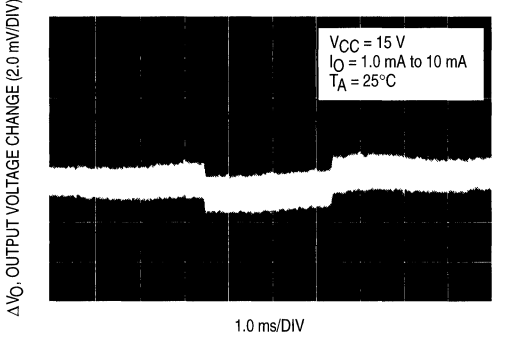


Figure 10. Reference Line Regulation

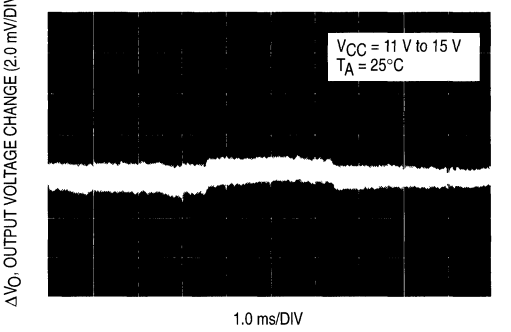


Figure 11. Output Saturation Voltage versus Load Current

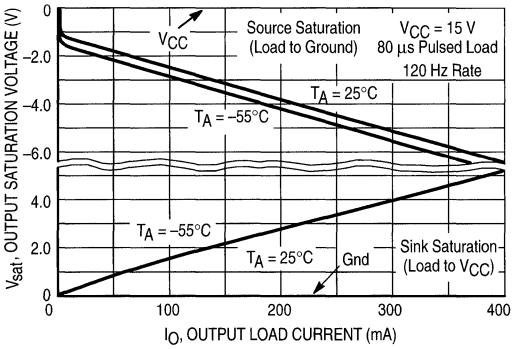


Figure 12. Output Waveform

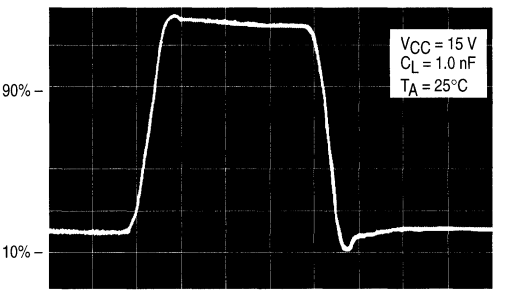


Figure 13. Output Cross Conduction Current

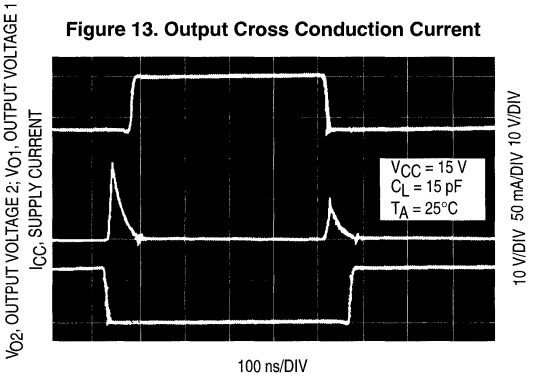
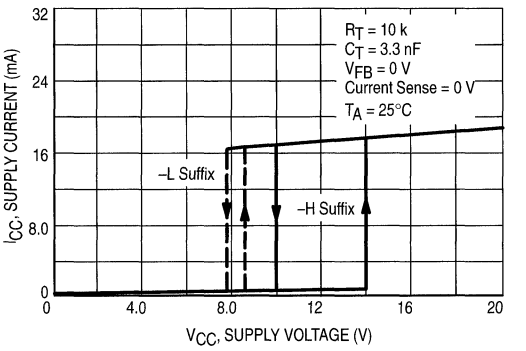


Figure 14. Supply Current versus Supply Voltage



OPERATING DESCRIPTION

The MC34065–H,L series are high performance, fixed frequency, dual channel current mode controllers specifically designed for Off–Line and dc–to–dc converter applications. These devices offer the designer a cost effective solution with minimal external components where independent regulation of two power converters is required. The Representative Block Diagram is shown in Figure 15. Each channel contains a high gain error amplifier, current sensing comparator, pulse width modulator latch, and totem pole output driver. The oscillator, reference regulator, and undervoltage lock–out circuits are common to both channels.

Oscillator

The unique oscillator configuration employed features precise frequency and duty cycle control. The frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink, generating a symmetrical 50 percent duty cycle waveform at Pin 2. The oscillator peak and valley thresholds are 3.5 V and 1.6 V respectively. The source/sink current magnitude is controlled by resistor R_T. For proper operation over temperature it must be in the range of 4.0 kΩ to 16 kΩ as shown in Figure 1.

As C_T charges and discharges, an internal blanking pulse is generated that alternately drives the center inputs of the upper and lower NOR gates high. This, in conjunction with a precise amount of delay time introduced into each channel, produces well defined non–overlapping output duty cycles. Output 2 is enabled while C_T is charging, and Output 1 is enabled during the discharge. Figure 2 shows the Maximum Output Duty Cycle versus Oscillator Frequency. Note that even at 500 kHz, each output is capable of approximately 44% on–time, making this controller suitable for high frequency power conversion applications.

In many noise sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal as shown in Figure 17. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 16, the rising edge of the clock signal applied to the Sync input, terminates charging of C_T and Drive Output 2 conduction. By tailoring the clock waveform symmetry, accurate duty cycle clamping of either output can be achieved. A circuit method for this, and multi–unit synchronization, is shown in Figure 18.

Error Amplifier

Each channel contains a fully–compensated Error Amplifier with access to the inverting input and output. The amplifier features a typical dc voltage gain of 100 dB, and a unity gain bandwidth of 1.0 MHz with 71° of phase margin (Figure 5). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input through a resistor divider. The maximum input bias current is –1.0 μA which will cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 5, 12) is provided for external loop compensation. The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no pulses appear at the Drive Output (Pin 7, 10) when the error amplifier output is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 20, 21).

The minimum allowable Error Amp feedback resistance is limited by the amplifier's source current (0.5 mA) and the output voltage (V_{OH}) required to reach the comparator's 1.0 V clamp level with the inverting input at ground. This condition happens during initial system startup or when the sensed output is shorted:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V)\ +\ 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The MC34065 operates as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output. Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator–PWM Latch configuration used ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting a ground–referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6, 11) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 5, 12 where:

$$I_{pk} = \frac{V_{(Pin\ 5,\ 12)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it may be desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense input with a time constant that approximates the spike duration will usually eliminate the instability, refer to Figure 24.

Undervoltage Lockout

Two Undervoltage Lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stages are enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14 V/10 V for –H suffix, and 8.4 V/7.6 V for –L suffix. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V respectively. The large hysteresis and low startup current of the –H suffix version makes it ideally suited in off–line converter applications where efficient bootstrap startup techniques are required (Figure 28). The –L suffix version is intended for lower voltage dc–to–dc converter applications. The minimum operating voltage for the –H suffix is 11 V and 8.2 V for the –L suffix.

Drive Outputs and Drive Ground

Each section contains a single totem–pole output stage that is specifically designed for direct drive of power MOSFETs. The Drive Outputs are capable of up to ±400 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the outputs in a sinking mode whenever an Undervoltage Lockout is active. This characteristic eliminates the need for an external pull–down resistor. The totem–pole output has been optimized to minimize cross–conduction current in high speed operation. The addition of two 10 Ω resistors, one in series with the source output transistor and one in series with the sink output transistor, reduces the cross–conduction current to minimal levels, as shown in Figure 13.

Although the Drive Outputs were optimized for MOSFETs, they can easily supply the negative base current required by bipolar NPN transistors for enhanced turn–off (Figure 25).

Figure 15. Representative Block Diagram

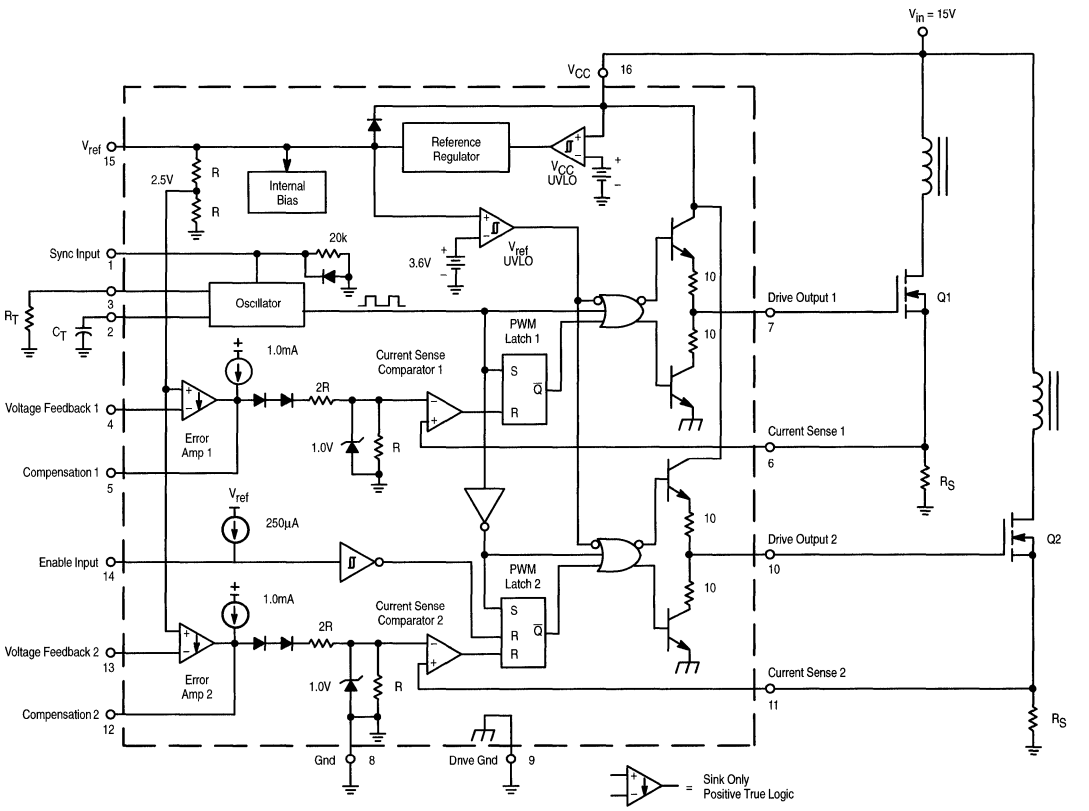
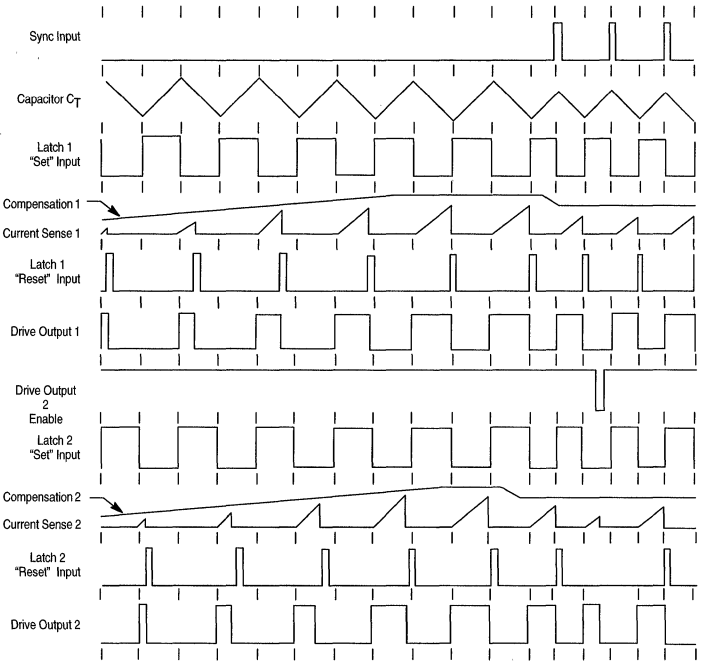


Figure 16. Timing Diagram



The outputs do not contain internal current limiting, therefore an external series resistor may be required to prevent the peak output current from exceeding the ±400 mA maximum rating. The sink saturation (V_{OL}) is less than 0.75 V at 50 mA.

A separate Drive Ground pin is provided and, with proper implementation, will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. Figure 23 shows the proper ground connections required for current sensing power MOSFET applications.

Drive Output 2 Enable Pin

This input is used to enable Drive Output 2. Drive Output 1 can be used to control circuitry that must run continuously such as volatile memory and the system clock, or a remote controlled receiver, while Drive Output 2 controls the high power circuitry that is occasionally turned off.

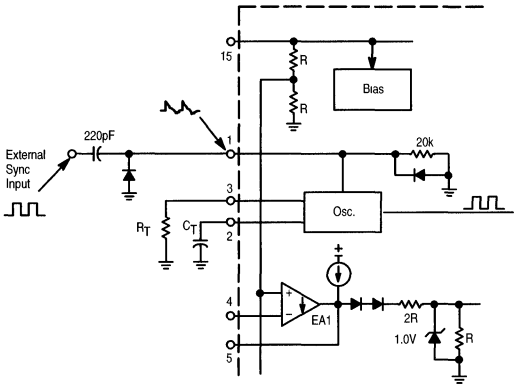
Reference

The 5.0 V bandgap reference is trimmed to ±2.0% tolerance at T_J = 25°C. The reference has short circuit protection and is capable of providing in excess of 30 mA for powering any additional control system circuitry.

Design Considerations

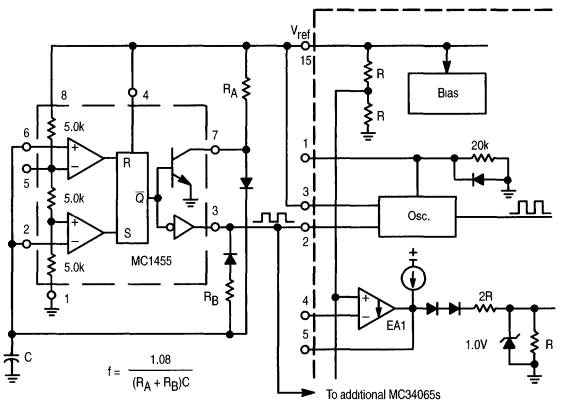
Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC} and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage–divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Figure 17. External Clock Synchronization



The external diode clamp is required if the negative Sync current is greater than –5.0 mA.

Figure 18. External Duty Cycle Clamp and Multi–Unit Synchronization



$$f = \frac{1.08}{(R_A + R_B)C}$$

$$D_{max}\ \text{Drive Output 1} = \frac{R_B}{R_A + R_B}$$

$$D_{max}\ \text{Drive Output 2} = \frac{R_A}{R_A + R_B}$$

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Sync Input	A narrow rectangular waveform applied to this input will synchronize the oscillator. A dc voltage within the range of 2.4 V to 5.5 V will inhibit the oscillator.
2	C_T	Timing capacitor C_T connects from this pin to ground setting the free–running oscillator frequency range.
3	R_T	Resistor R_T connects from this pin to ground precisely setting the charge current for C_T. R_T must be between 4.0 k and 16 k.
4	Voltage Feedback 1	This pin is the inverting input of Error Amplifier 1. It is normally connected to the switching power supply output through a resistor divider.
5	Compensation 1	This pin is the output of Error Amplifier 1 and is made available for loop compensation.
6	Current Sense 1	A voltage proportional to the inductor current is connected to this input. PWM 1 uses this information to terminate conduction of output switch Q1.
7	Drive Output 1	This pin directly drives the gate of a power MOSFET Q1. Peak currents up to 400 mA are sourced and sunk by this pin.
8	Gnd	This pin is the control circuitry ground return and is connected back to the source ground.
9	Drive Gnd	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
10	Drive Output 2	This pin directly drives the gate of a power MOSFET Q2. Peak currents up to 400 mA are sourced and sunk by this pin.
11	Current Sense 2	A voltage proportional to inductor current is connected to this input. PWM 2 uses this information to terminate conduction of output switch Q2.
12	Compensation 2	This pin is the output of Error Amplifier 2 and is made available for loop compensation.
13	Voltage Feedback 2	This pin is the inverting input of Error Amplifier 2. It is normally connected to the switching power supply output through a resistor divider.
14	Drive Output 2 Enable	A logic low at this input disables Drive Output 2.
15	V_{ref}	This is the 5.0 V reference output. It can provide bias for any additional system circuitry.
16	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after startup is 11 V to 15.5 V for the –H suffix, 8.2 V to 9.5 V for the –L suffix.

3

Figure 19. Adjustable Reduction of Clamp Level

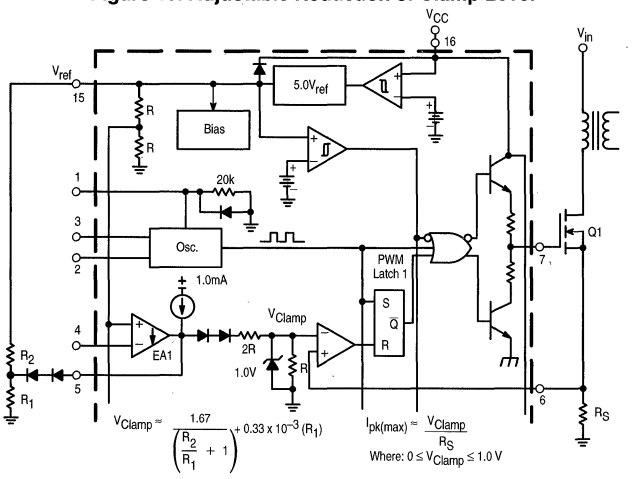


Figure 20. Soft–Start Circuit

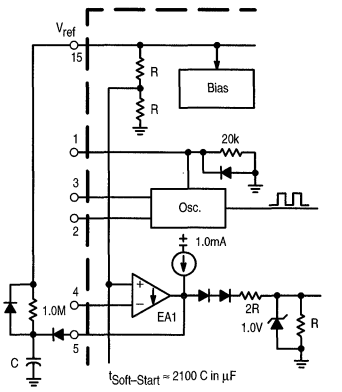


Figure 21. Adjustable Reduction of Clamp Level with Soft–Start

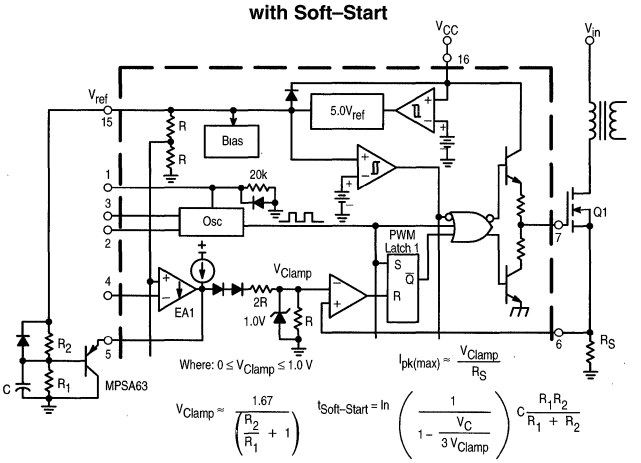
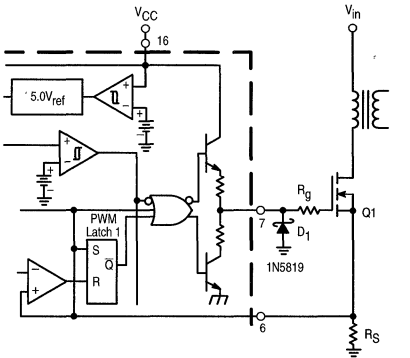
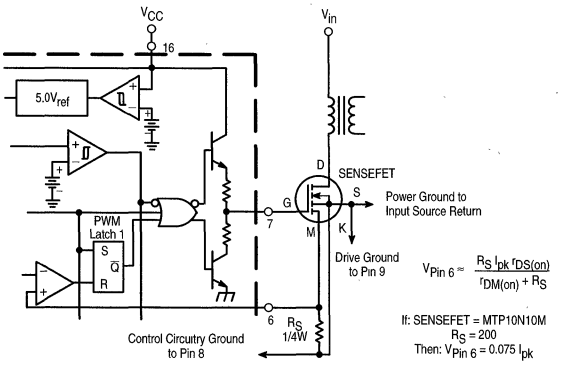


Figure 22. MOSFET Parasitic Oscillations



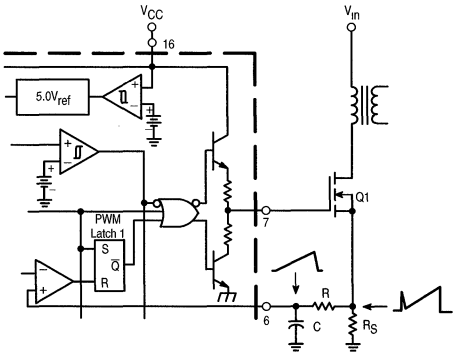
Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 is required if circuit ringing drives the output pin below ground.

Figure 23. Current Sensing Power MOSFET



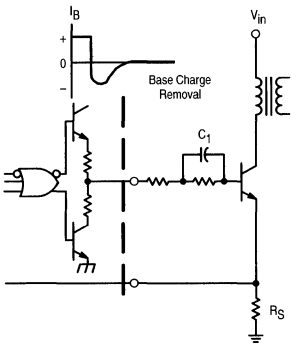
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation durng over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

Figure 24. Current Waveform Spike Suppression



The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 25. Bipolar Transistor Drive



The totem–pole outputs can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 26. Isolated MOSFET Drive

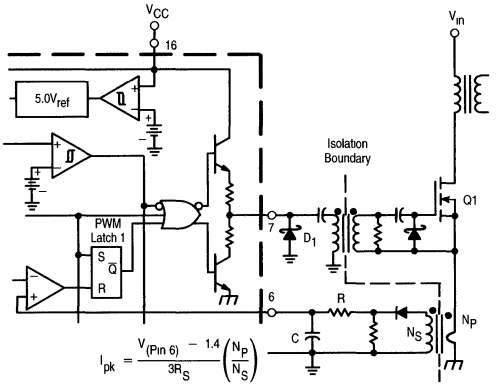
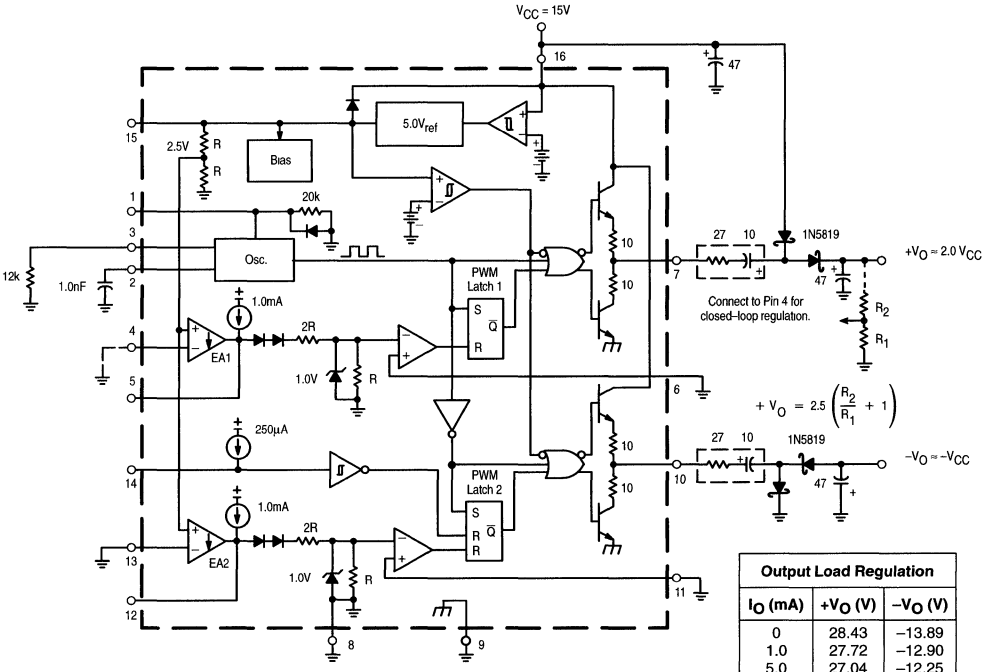


Figure 27. Dual Charge Pump Converter

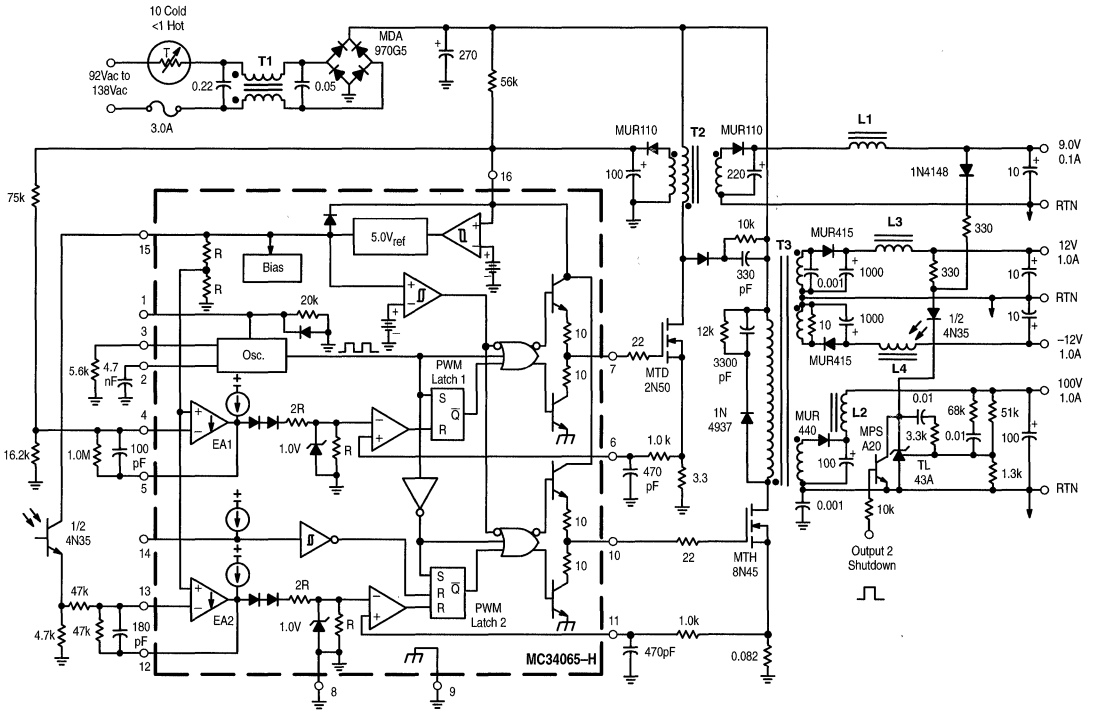


Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	28.43	–13.89
1.0	27.72	–12.90
5.0	27.04	–12.25
10	26.20	–11.44
50	20.52	–5.80

The capacitor's equivalent series resistance must limit the Drive Output current to 400 mA. An additional series resistor may be required when using tantalum or other low ESR capacitors. The positive output can provide excellent line and load regulation by connecting the R_2/R_1 resistor divider as shown.

3

Figure 28. 125 Watt Off–Line Converter



Test	Conditions	Results
Line Regulation 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 92 Vac to 138 Vac I_O = 1.0 A I_O = ±1.0 A I_O = 0.1 A	 Δ = 40 mV or ±0.02% Δ = 32 mV or ±0.13% Δ = 55 mV or ±0.31%
Load Regulation 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac I_O = 0.25 A to 1.0 A I_O = ±0.25 A to ±1.0 A I_O = 0.08 A to 0.1 A	 Δ = 50 mV or ±0.025% Δ = 320 mV or ±1.2% Δ = 234 mV or ±1.3%
Output Ripple 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac I_O = 1.0 A I_O = ±1.0 A I_O = 0.1 A	 40 mVpp 100 mVpp 60 mVpp
Short Circuit Current 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac, R_L = 0.1 Ω	 4.3 A 17 A Output Hiccups
Efficiency	Vin = 115 Vac, PO = 125 W	86%

T1 – 468 μH per section at 2.5 A, Coilcraft E3496A.

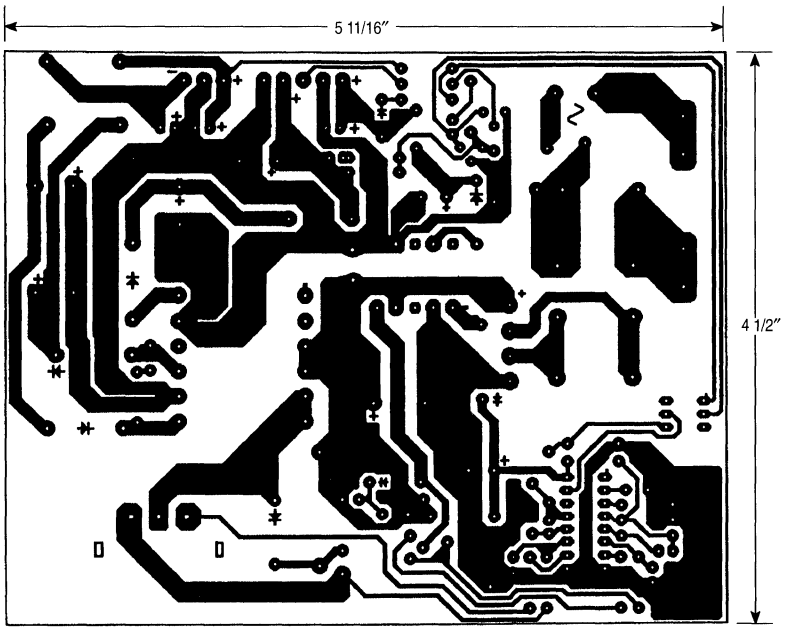
T2 – Primary: 156 Turns, #34 AWG
Primary Feedback: 19 Turns, #34 AWG
Secondary: 17 Turns, #28 AWG
Core: TDK PC30 EE22–Z
Bobbin: BE22–118CP
Gap: ≈0.001″ for a primary inductance of 6.8 mH

T3 – Primary: 56 Turns, #23 AWG (2 strands) Bifiliar Wound
Secondary: ±12 V, 4 Turns, #23 AWG (4 strands) Quadfiliar Wound
Secondary 100 V: 32 Turns, #23 AWG (2 strands) Bifiliar Wound
Core: TDK PC30 EER40 G0.76
Bobbin: BEER40–1112CP
Gap: ≈0.030″ for a primary inductance of 212 μH

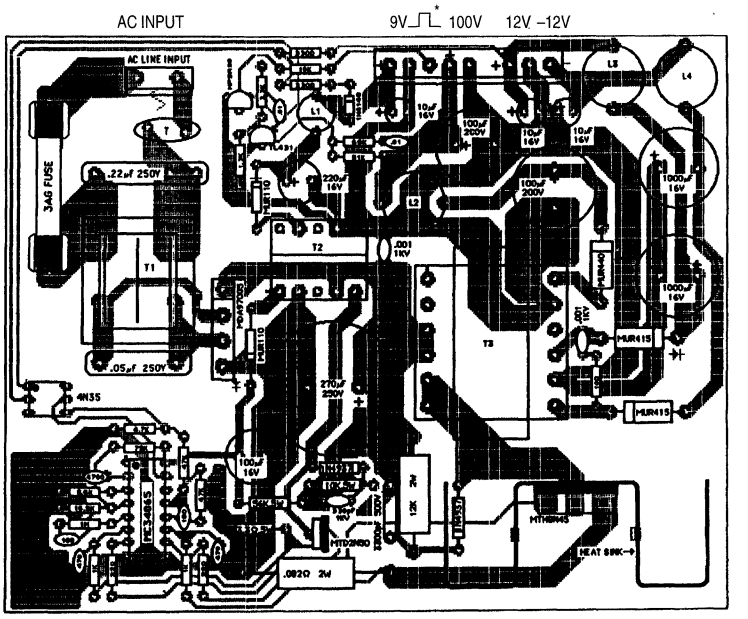
L1, L3, L4 – 25 μH at 1.0 A, Coilcraft Z7157.

L2 – 10 μH at 3.0 A, Coilcraft PCV–0–010–03.

Figure 29. PC Board Circuit Side and Component View



(CIRCUIT VIEW)



(COMPONENT VIEW)

*100 V and ±12 V Shutdown

MC34066
MC33066

3

High Performance Resonant Mode Controllers

The MC34066/MC33066 are high performance resonant mode controllers designed for off–line and dc–to–dc converter applications that utilize frequency modulated constant on–time or constant off–time control. These integrated circuits feature a variable frequency oscillator with programmable deadtime, precision retriggerable one–shot timer, temperature compensated reference, high gain wide–bandwidth error amplifier with a precision output clamp, steering flip–flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

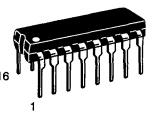
Also included are protective features consisting of a high speed fault comparator and latch, programmable soft–start circuitry, input undervoltage lockout with selectable thresholds, and reference undervoltage lockout.

These devices are available in dual–in–line and surface mount packages.

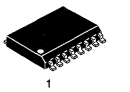
- Variable Frequency Oscillator with a Control Range Exceeding 1000:1
- Programmable Oscillator Deadtime Allows Constant Off–Time Operation
- Precision Retriggerable One–Shot Timer
- Internally Trimmed Bandgap Reference
- 5.0 MHz Error Amplifier with Precision Output Clamp
- Dual High Current Totem Pole Outputs
- Selectable Undervoltage Lockout Thresholds with Hysteresis
- Enable Input
- Programmable Soft–Start Circuitry
- Low Startup Current for Off–Line Operation

HIGH PERFORMANCE RESONANT MODE CONTROLLERS

SEMICONDUCTOR TECHNICAL DATA

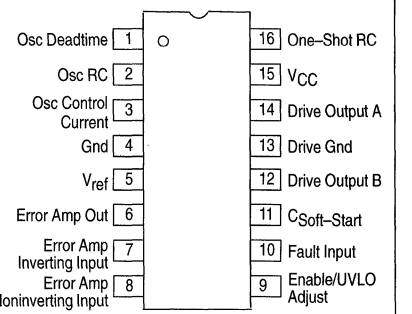


P SUFFIX
PLASTIC PACKAGE
CASE 648



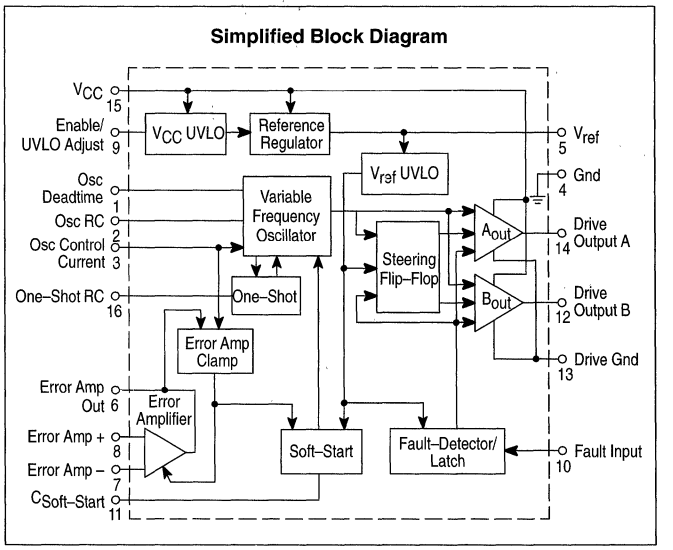
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34066DW	T_A = 0° to +70°C	SO–16L
MC34066P		Plastic DIP
MC33066DW	T_A = –40° to +85°C	SO–16L
MC33066P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{CC}	20	V
Drive Output Current, Source or Sink (Note 1) Continuous Pulsed (0.5 μs, 25% Duty Cycle)	I_O	 0.3 1.5	A
Error Amplifier, Fault, One–Shot, Oscillator, and Soft–Start Inputs	V_{in}	–1.0 to +6.0	V
UVLO Adjust Input	$V_{in(UVLO)}$	–1.0 to V_{CC}	V
Soft–Start Discharge Current	I_{dchg}	20	mA
Power Dissipation and Thermal Characteristics DW Suffix Package, Case 751G Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air P Suffix Package, Case 648 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34066 MC33066	T_A	 0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V [Note 2], R_{OSC} = 95.3 k, R_{DT} = 0 Ω, R_{VFO} = 5.62 k, C_{OSC} = 300 pF, R_T = 14.3 k, C_T = 300 pF, C_L = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 0 mA, T_A = 25°C)	V_{ref}	5.0	5.1	5.2	V
Line Regulation (V_{CC} = 10 V to 18 V)	Reg_{line}	–	1.0	20	mV
Load Regulation (I_O = 0 mA to 10 mA)	Reg_{load}	–	1.0	20	mV
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	–	5.3	mV
Output Short Circuit Current	I_O	25	100	190	mA
Reference Undervoltage Lockout Threshold	V_{th}	3.8	4.3	4.8	V
ERROR AMPLIFIER					
Input Offset Voltage (V_{CM} = 1.5 V)	V_{IO}	–	1.0	10	mV
Input Bias Current (V_{CM} = 1.5 V)	I_{IB}	–	0.2	1.0	μA
Input Offset Current (V_{CM} = 1.5 V)	I_{IO}	–	0	0.5	μA
Open Loop Voltage Gain (V_{CM} = 1.5 V, V_O = 2.0 V)	A_{VOL}	70	100	–	dB
Gain Bandwidth Product (f = 100 kHz)	GBW	2.5	4.2	–	MHz
Input Common Mode Rejection Ratio (V_{CM} = 1.5 V to 5.0 V)	CMRR	70	95	–	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 18 V, f = 120 Hz)	PSRR	80	100	–	dB
Output Voltage Swing High State with Respect to Pin 3 (I_{Source} = 2.0 mA) Low State with Respect to Ground (I_{Sink} = 1.0 mA)	 V_{OH} V_{OL}	 2.3 –	 2.7 0.4	 3.1 0.6	V

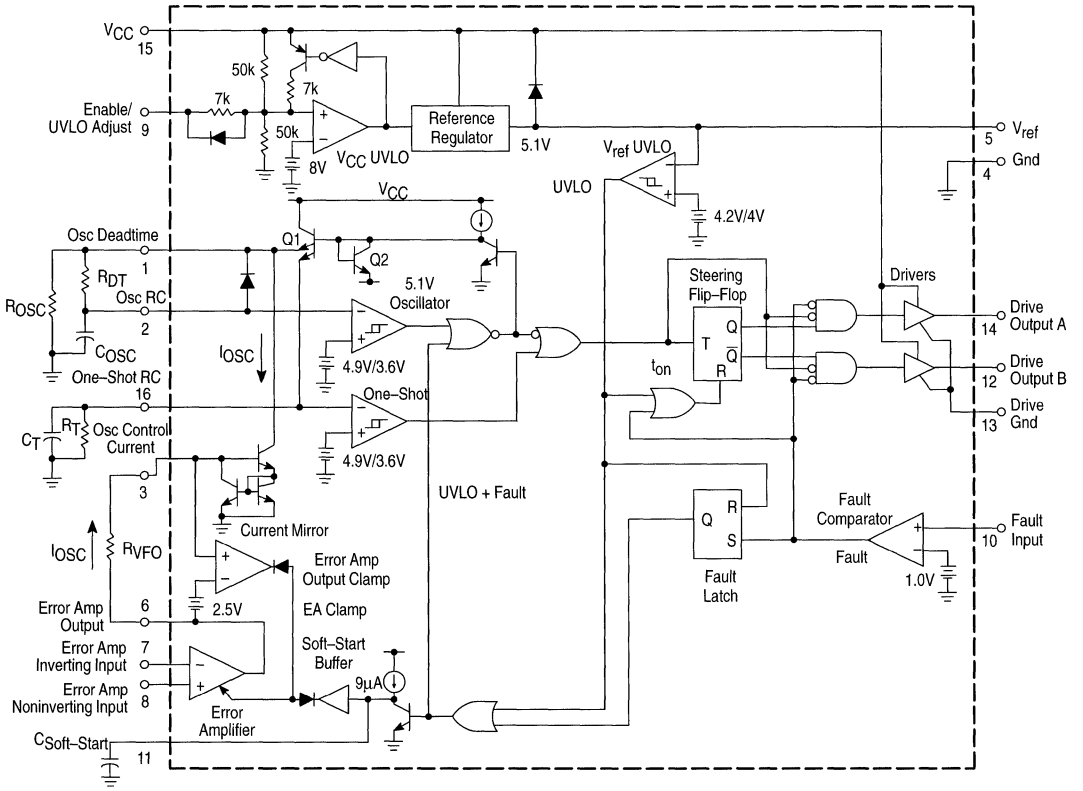
NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 12 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34066, –40°C for MC33066 T_{high} = +70°C for MC34066, +85°C for MC33066

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 12 V [Note 2], R_{OSC} = 95.3 k, R_{DT} = 0 Ω, R_{VFO} = 5.62 k, C_{OSC} = 300 pF, R_T = 14.3 k, C_T = 300 pF, C_L = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (Error Amp Output Low)	$f_{OSC(low)}$				kHz
T_A = 25°C		90	100	110	
Total Variation (V_{CC} = 10 V to 18 V, T_A = T_{Low} to T_{High})		85	–	115	
Frequency (Error Amp Output High)	$f_{OSC(high)}$				kHz
T_A = 25°C		900	1000	1100	
Total Variation (V_{CC} = 10 V to 18 V, T_A = T_{Low} to T_{High})		850	–	1150	
Oscillator Control Input Voltage, Pin 3 (I_{Sink} = 0.5 mA, T_A = 25°C)	V_{in}	1.3	1.4	1.5	V
Output Deadtime (Error Amp Output High)	DT				ns
R_{DT} = 0 Ω		–	70	100	
R_{DT} = 1.0 k		600	700	800	
ONE–SHOT					
Drive Output On–Time (R_{DT} = 1.0 k)	t_{OS}				µs
T_A = 25°C		1.43	1.5	1.57	
Total Variation (V_{CC} = 10 V to 18 V, T_A = T_{Low} to T_{High})		1.4	–	1.6	
DRIVE OUTPUTS					
Output Voltage					V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.8	1.2	
(I_{Sink} = 200 mA)		–	1.5	2.0	
High State (I_{Source} = 20 mA)	V_{OH}	9.5	10.3	–	
(I_{Source} = 200 mA)		9.0	9.8	–	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.8	1.2	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	20	50	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	20	50	ns
FAULT COMPARATOR					
Input Threshold	V_{th}	0.95	1.0	1.05	V
Input Bias Current ($V_{Pin\ 10}$ = 0 V)	I_{IB}	–	–2.0	–10	µA
Propagation Delay to Drive Outputs (100 mV Overdrive)	$t_{PLH(In/Out)}$	–	60	100	ns
SOFT–START					
Capacitor Charge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{chg}	4.5	8.1	14	µA
Capacitor Discharge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{Idchg}	1.0	8.0	–	mA
UNDERVOLTAGE LOCKOUT					
Startup Threshold, V_{CC} Increasing	$V_{th(UVLO)}$				V
Enable/UVLO Adjust Pin Open		14.8	16	17.2	
Enable/UVLO Adjust Pin Connected to V_{CC}		8.0	9.0	10	
Minimum Operating Voltage after Turn–On	$V_{CC(min)}$				V
Enable/UVLO Adjust Pin Open		8.0	9.0	10	
Enable/UVLO Adjust Pin Connected to V_{CC}		7.6	8.6	9.6	
Enable/UVLO Adjust Shutdown Threshold Voltage	$V_{th(Enable)}$	6.0	7.0	–	V
Enable/UVLO Adjust Input Current (Pin 9 = 0V)	$I_{in(Enable)}$	–	–0.2	–1.0	mA
TOTAL DEVICE					
Power Supply Current (Enable/UVLO Adjust Pin Open)	I_{CC}				mA
Startup (V_{CC} = 13.5 V)		–	0.45	0.6	
Operating (f_{OSC} = 100 kHz) (Note 2)		–	21	30	

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 12 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34066, –40°C for MC33066 T_{high} = +70°C for MC34066, +85°C for MC33066

Figure 1. MC34066 Representative Block Diagram



OPERATING DESCRIPTION

Introduction

As power supply designers have strived to increase power conversion efficiency and reduce passive component size, high frequency resonant mode power converters have emerged as attractive alternatives to conventional square–wave control. When compared to square–wave converters, resonant mode control offers several benefits including lower switching losses, higher efficiency, lower EMI emission, and smaller size. This integrated circuit has been developed to support new trends in power supply design. The MC34066 Resonant Mode Controller is a high performance bipolar IC dedicated to variable frequency power control at frequencies exceeding 1.0 MHz. This integrated circuit provides the features, performance and flexibility for a wide variety of resonant mode power supply applications.

The primary purpose of the control chip is to supply precise pulses to the gates of external power MOSFETs at a repetition rate regulated by a feedback control loop. The MC34066 can be operated in any of three modes as follows: 1) fixed on–time, variable frequency; 2) fixed off–time, variable frequency; and 3) combinations of 1 and 2 that change from fixed on–time to fixed off–time as the frequency increases. Additional features of the IC ensure that system startup and fault conditions are administered in a safe, controlled manner.

A simplified block diagram of the IC is shown on the first page of this data sheet, which identifies the main functional blocks and the block–to–block interconnects. Figure 1 is a detailed functional diagram which accurately represents the internal circuitry. The various functions can be divided into two sections. The first section includes the primary control path which produces precise output pulses at the desired frequency Oscillator, a One–Shot, a pulse Steering Flip–Flop, a pair of power MOSFET Drivers, and a wide bandwidth Error Amplifier. The second section provides several peripheral support functions including a voltage reference, undervoltage lockout, Soft–Start circuit, and a fault detector.

Primary Control Path

The output pulse width and repetition rate are regulated through the interaction of the variable frequency Oscillator, One–Shot timer and Error Amplifier. The Oscillator triggers the One–Shot which generates a pulse that is alternately steered to a pair of totem–pole output drivers by a toggle Flip–Flop. The Error Amplifier monitors the output of the regulator and modulates the frequency of the Oscillator. High–speed Schottky logic is used throughout the primary control channel to minimize delays and enhance high frequency characteristics.

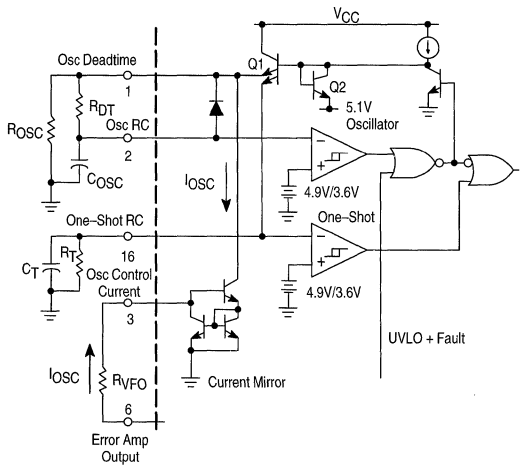
3

Oscillator

The characteristics of the variable frequency Oscillator are crucial for precise controller performance at high operating frequencies. In addition to triggering the One–Shot timer and initiating the output pulse, the Oscillator also determines the initial voltage for the One–Shot capacitor and defines the minimum deadtime between output pulses. The Oscillator is designed to operate at frequencies exceeding 1.0 MHz. The Error Amplifier can control the oscillator frequency over a 1000:1 frequency range, and both the minimum and maximum frequencies are easily and accurately programmed by the proper selection of external components. The Oscillator also includes an adjustable deadtime feature for applications requiring additional time between output pulses.

The functional diagram of the Oscillator and One–Shot timer is shown in Figure 2. The oscillator capacitor C_{OSC} is initially charged by transistor Q1 through the optional deadtime resistor R_{DT}. When C_{OSC} exceeds the 4.9 V upper threshold of the oscillator comparator, the base of Q1 is pulled low allowing C_{OSC} to discharge through the external resistors and the internal Current Mirror. When the voltage on C_{OSC} falls below the comparator's 3.6 V lower threshold, Q1 turns on and again charges C_{OSC}.

Figure 2. Oscillator and One–Shot Timer



If R_{DT} is 0 Ω, C_{OSC} charges from 3.6 V to 5.1 V in less than 50 ns. The high slew rate of C_{OSC} and the propagation delay of the comparator make it difficult to control the peak voltage. This accuracy issue is overcome by clamping the base of Q1 through diode Q2 to a voltage reference. The peak voltage of the oscillator waveform is thereby precisely set at 5.1 V.

The frequency of the Oscillator is modulated by varying the current I_{OSC} flowing through R_{VFO} into the Osc Control Current pin. The control current drives a unity gain Current Mirror which pulls an identical current from the C_{OSC} capacitor. As I_{OSC} increases, C_{OSC} discharges faster thus decreasing the Oscillator period and increasing the frequency. The maximum frequency occurs when the Error Amplifier output is at the upper clamp level, nominally 2.5 V above the voltage at the Osc Control Current pin. The minimum discharge time for C_{OSC}, which corresponds to the maximum oscillator frequency, is given by Equation 1.

$$t_{dchg(min)} = (R_{DT} + R_{OSC})C_{OSC}\ln\left[\frac{\frac{2.5R_{OSC}}{R_{VFO}} + 5.1}{\frac{2.5R_{OSC}}{R_{VFO}} + 3.6}\right] \quad (1)$$

The minimum oscillator frequency will result when the I_{OSC} current is zero, and C_{OSC} is discharged through the external resistors R_{OSC} and R_{DT}. This occurs when the Error Amplifier output voltage is less than the two diode drops required to bias the input of the Current Mirror. The maximum oscillator discharge time is given by Equation 2.

$$t_{dchg(max)} = (R_{DT} + R_{OSC})\, C_{OSC}\ln\left(\frac{5.1}{3.6}\right) \quad (2)$$

The outputs of the control IC are off whenever the oscillator capacitor C_{OSC} is being charged by transistor Q1. The minimum time between output pulses (deadtime) can be programmed by controlling the charge time of C_{OSC}. Resistor R_{DT} reduces the current delivered by Q1 to C_{OSC}, thus increasing the charge time and output deadtime. Varying R_{DT} from 0 Ω to 1000 Ω will increase the output deadtime from 80 ns to 680 ns with C_{OSC} equal to 300 pF. The general expression for the oscillator charge time is give by Equation 3.

$$t_{chg(max)} = R_{DT}\, C_{OSC}\ln\left(\frac{5.1-3.6}{5.1-4.9}\right) + 80\ \text{ns} \quad (3)$$

The minimum and maximum oscillator frequencies are programmed by the proper selection of resistor R_{OSC} and R_{VFO}. After selecting R_{DT} for the desired deadtime, the minimum frequency is programmed by R_{OSC} using Equations 2 and 3 in Equation 4:

$$\frac{1}{f_{OSC(min)}} = t_{dchg(max)} + t_{chg} \quad (4)$$

The maximum oscillator frequency is set by resistor R_{VFO} in a similar fashion using Equations 1 and 3 in Equation 5:

$$\frac{1}{f_{OSC(max)}} = t_{dchg(min)} + t_{chg} \quad (5)$$

The value chosen for resistor R_{DT} will affect the peak voltage of the oscillator waveform. As R_{DT} is increased from zero, the time required to charge C_{OSC} becomes large with respect to the propagation delay through the oscillator comparator. Consequently, the overshoot of the upper threshold is reduced and the peak voltage on the oscillator waveform drops from 5.1 V to 4.9 V. The best frequency accuracy is achieved when R_{DT} is zero ohms.

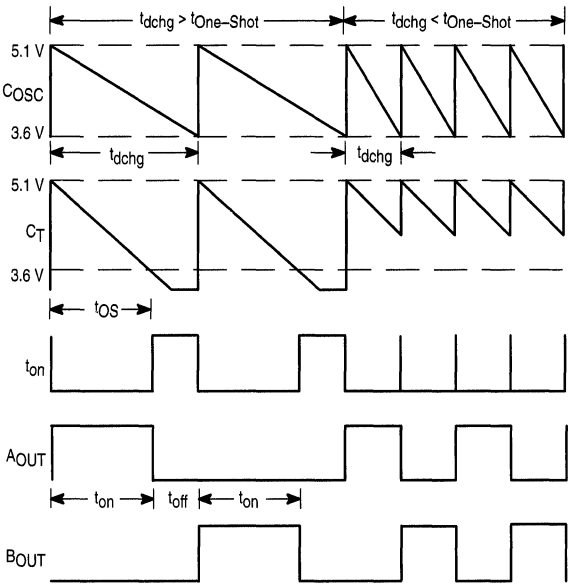
One–Shot Timer

The One–Shot capacitor C_T is charged concurrently with the oscillator capacitor by transistor Q1, as shown in Figure 2. The One–Shot period begins when the oscillator comparator turns off Q1, allowing C_T to discharge. The period ends when resistor R_T discharges C_T to the threshold of the One–Shot comparator. Discharging C_T from an initial voltage of 5.1 V to a threshold voltage of 3.6 V results in the One–Shot period given by Equation 6.

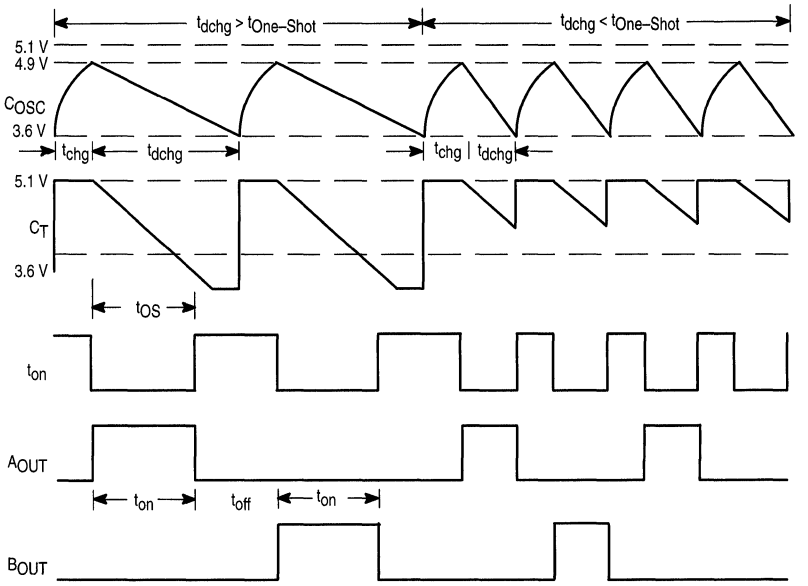
$$t_{OS} = R_T\, C_T\ln\left(\frac{5.1}{3.6}\right) = 0.348\, R_T\, C_T \quad (6)$$

Figure 3. Timing Waveforms

R_{DT} = 0



R_{DT} = 1.0 k



Errors in the threshold voltage and propagation delays through the output drivers will affect the One–Shot period. To guarantee accuracy, the output pulse of the control ship is trimmed to within 5% of 1.5 μs with nominal values of R_T and C_T.

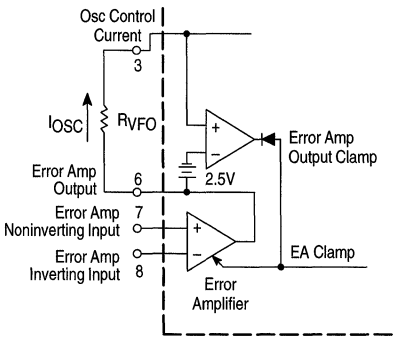
The outputs of the Oscillator and One–Shot comparators are OR'd together to produce the pulse t_{on}, which drives the Flip–Flop and output drivers. The output pulse t_{on} is initiated by the Oscillator, but either the oscillator comparator or the One–Shot comparator can terminate the pulse. When the oscillator discharge time exceeds the one–shot period, the complete one–shot period is delivered to the output section. If the oscillator discharge time is less than the one–shot period, then the oscillator comparator terminates the pulse prematurely and retriggers the One–Shot. The waveforms on the left side of Figure 3 correspond to nonretriggered operation with constant on–time and variable off–times. The right side of Figure 3 represents retriggered operation with variable on–time and constant off–time.

Error Amplifier

A fully accessible high performance Error Amplifier is provided for feedback control of the power supply system. The Error Amplifier is internally compensated and features dc open loop gain greater than 70 dB, input offset voltage less than 10 mV and guaranteed minimum gain–bandwidth product of 2.5 MHz. The input common mode range extends from 1.5 V to 5.1 V, which includes the reference voltage. For common mode voltages below 1.5 V, the Error Amplifier output is forced low providing minimum oscillator frequency.

The Oscillator Control Current pin is biased by the Error Amplifier output voltage through R_{VFO} as illustrated in Figure 4. The output swing of the Error Amplifier is restricted by a clamp circuit to limit the maximum oscillator frequency. The clamp circuit limits the voltage across R_{VFO} to 2.5 V, thus limiting I_{OSC} to 2.5 V/R_{VFO}. Oscillator accuracy is improved by trimming the clamp voltage to obtain the $f_{OSC(high)}$ specification of 1.0 MHz with nominal value external components.

Figure 4. Error Amplifier and Clamp

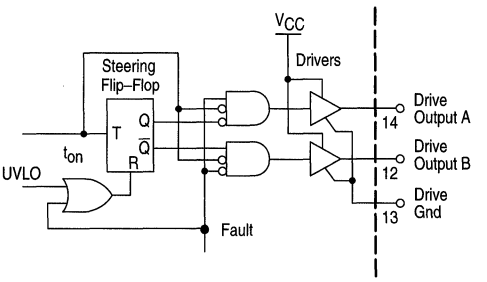


Output Section

The pulse, t_{on}, generated by the Oscillator and One–Shot timer is gated to dual totem pole output drives by the Steering Flip–Flop shown in Figure 5. Positive transitions of t_{on} toggle the Flip–Flop, which causes the pulses to alternate between Output A and Output B. The flip–flop is reset by the undervoltage lockout circuit during startup to guarantee that the first pulse appears at Output A.

The totem–pole output drives are ideally suited for driving power MOSFETs and are capable of sourcing and sinking 1.5 A. Rise and fall times are typically 20 ns when driving a 1.0 nF load. High source/sink capability in a totem–pole driver normally increases the risk of high cross conduction current during output transitions. The MC34066 utilizes a unique design that virtually eliminates cross conduction, thus controlling the chip power dissipation at high frequencies. A separate ground terminal is provided for the output drivers to isolate the sensitive analog circuitry from large transient currents.

Figure 5. Steering Flip–Flop and Output Drivers



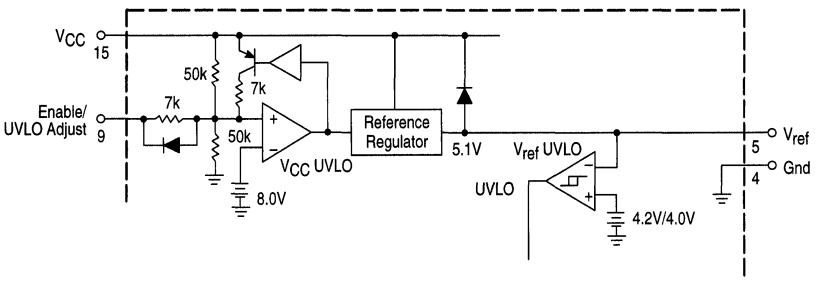
PERIPHERAL SUPPORT FUNCTIONS

The MC34066 Resonant Controller provides a number of support and protection functions including a precision voltage reference, undervoltage lockout comparators, soft–start circuitry, and a fault detector. These peripheral circuits ensure that the power supply can be turned on and off in a safe, controlled manner and that the system will be quickly disabled when a fault condition occurs.

Undervoltage Lockout and Voltage Reference

Separate undervoltage lockout comparators sense the input V_{CC} voltage and the regulated reference voltage as illustrated in Figure 6. When V_{CC} increases to the upper threshold voltage, the V_{CC} UVLO comparator enables the Reference Regulator. After the V_{ref} output of the Reference Regulator rises to 4.2 V, the V_{ref} UVLO comparator switches the UVLO signal to a logic zero state enabling the primary control path. Reducing V_{CC} to the lower threshold voltage causes the V_{CC} UVLO comparator to disable the Reference Regulator. The V_{ref} UVLO comparator then switches the UVLO output to a logic one state disabling the controller.

Figure 6. Undervoltage Lockout and Reference



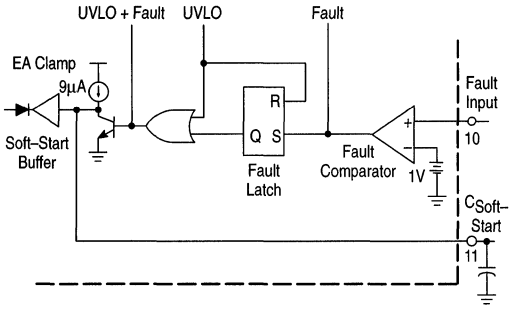
The Enable/UVLO Adjust terminal allows the power supply designer to select the V_{CC} UVLO threshold voltages. When this pin is open, the comparator switches the controller on at 16 V and off at 9.0 V. If this pin is connected to the V_{CC} terminal, the upper and lower thresholds are reduced to 9.0 V and 8.6 V, respectively. Forcing the Enable/UVLO Adjust pin low will pull the V_{CC} UVLO comparator input low (through an internal diode) turning off the controller.

The Reference Regulator provides a precise 5.1 V reference to internal circuitry and can deliver up to 10 mA to external loads. The reference is trimmed to better than 2% initial accuracy and includes active short circuit protection.

Fault Detector

The high–speed Fault Comparator and Latch illustrated in Figure 7 can protect a power supply from destruction under fault conditions. The Fault Input pin connects to the input of the Fault Comparator. If this input exceeds the 1.0 V threshold of the comparator, the Fault Latch is set and two logic signals simultaneously disable the primary control path. The signal labeled Fault at the output of the Fault Comparator is connected directly to the output drivers. This direct path reduces the propagation delay from the Fault Input to the A and B outputs to typically 70 ns. The Fault Latch output is OR'd with UVLO output from the V_{ref} UVLO comparator to produce the logic output labeled UVLO + Fault. This signal disables the Oscillator and One–Shot by forcing both the C_{OSC} and C_T capacitors to be continually charged.

Figure 7. Fault Detector and Soft–Start



The Fault Latch is reset during startup by a logic one at the UVLO output of the V_{ref} UVLO comparator. The latch can also be reset after startup by pulling the Enable/UVLO Adjust pin momentarily low to disable the Reference Regulator.

Soft–Start Circuit

The Soft–Start circuit shown in Figure 7 forces the variable frequency Oscillator to start at the minimum frequency and ramp upward until regulated by the feedback control loop. The external capacitor at the $C_{Soft–Start}$ terminal is initially discharged by the UVLO + Fault signal. The low voltage on the capacitor pass through the Soft–Start Buffer to hold the Error Amplifier output low. After UVLO + Fault switches to a logic zero, the soft–start capacitor is charged by a 9.0 μA current source. The buffer allows the Error Amplifier output to follow the soft–start capacitor until it is regulated by the Error Amplifier inputs (or reaches the 2.5 V clamp). The soft–start function is generally applicable to controllers operating below resonance and can be disabled by simply opening the $C_{Soft–Start}$ terminal.

APPLICATIONS

The MC34066 can be used for the control of series, parallel or higher order half/full bridge resonant converters. The IC is designed to provide control in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) or a combination of the two. For example, in a parallel resonant converter (PRC) operating in the DCM, the IC is programmed to operate in fixed on–time, variable frequency mode of operation. For a PRC operating in the CCM, the IC can be programmed to operate in the variable frequency mode with a fixed off–time.

When operating with a wide input voltage range, such as a universal input power supply, a PRC can operate in the DCM for high input voltage and in the CCM for low input voltage. In this particular case, on–time is programmed corresponding to DCM. The deadtime of the chip is programmed to provide the desired off–time in the CCM. The frequency range is chosen to cover the complete frequency range from the DCM to the CCM. When programmed as such, the controller will operate in the fixed on–time, variable frequency mode at low frequencies. At the frequency which causes the Oscillator to retrigger the One–Shot, the control law changes to variable frequency with fixed off–time. At higher frequencies the supply will operate in the CCM with this control law.

Although the IC is designed and optimized for double ended push–pull type converters, it can also be used for single ended applications, such as forward and flyback resonant converters.

MC34067
MC33067

3

High Performance Resonant Mode Controllers

The MC34067/MC33067 are high performance zero voltage switch resonant mode controllers designed for off–line and dc–to–dc converter applications that utilize frequency modulated constant off–time or constant deadtime control. These integrated circuits feature a variable frequency oscillator, a precise retriggerable one–shot timer, temperature compensated reference, high gain wide bandwidth error amplifier, steering flip–flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of a high speed fault comparator and latch, programmable soft–start circuitry, input undervoltage lockout with selectable thresholds, and reference undervoltage lockout.

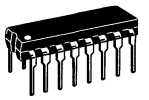
These devices are available in dual–in–line and surface mount packages.

- Zero Voltage Switch Resonant Mode Operation
- Variable Frequency Oscillator with a Control Range Exceeding 1000:1
- Precision One–Shot Timer for Controlled Off–Time
- Internally Trimmed Bandgap Reference
- 4.0 MHz Error Amplifier
- Dual High Current Totem Pole Outputs
- Selectable Undervoltage Lockout Thresholds with Hysteresis
- Enable Input
- Programmable Soft–Start Circuitry
- Low Startup Current for Off–Line Operation

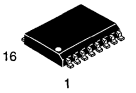
HIGH PERFORMANCE ZERO VOLTAGE SWITCH RESONANT MODE CONTROLLERS

SEMICONDUCTOR TECHNICAL DATA

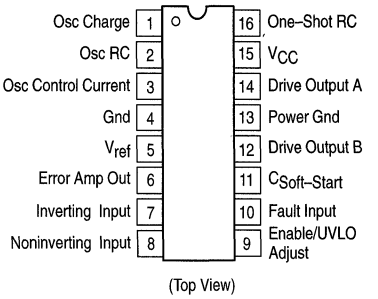
P SUFFIX
PLASTIC PACKAGE
CASE 648



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

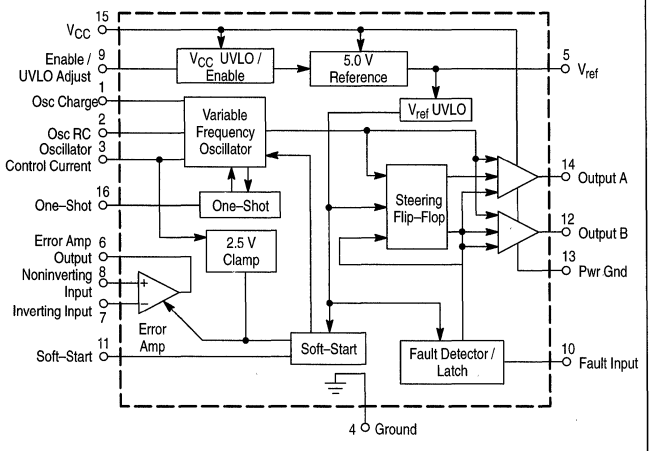


PIN CONNECTIONS



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34067DW	T_A = 0 to + 70°C	SO–16L
MC34067P		Plastic DIP
MC33067DW	T_A = – 40° to + 85°C	SO–16L
MC33067P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Drive Output Current, Source or Sink (Note 1) Continuous Pulsed (0.5 μs, 25% Duty Cycle	I_O	 0.3 1.5	A
Error Amplifier, Fault, One–Shot, Oscillator and Soft–Start Inputs	V_{in}	– 1.0 to + 6.0	V
UVLO Adjust Input	$V_{in(UVLO)}$	– 1.0 to V_{CC}	V
Power Dissipation and Thermal Characteristics DW Suffix, Plastic Package, Case 751G T_A = 25°C Thermal Resistance, Junction–to–Air P Suffix, Plastic Package, Case 648 T_A = 25°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature MC34067 MC33067	T_A	 0 to + 70 – 40 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V [Note 2], R_{OSC}= 18.2 k, R_{VFO} = 2940, C_{OSC} = 300 pF, R_T = 2370 k, C_T = 300 pF, C_L = 1.0 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 0 mA, T_J = 25°C)	V_{ref}	5.0	5.1	5.2	V
Line Regulation (V_{CC} = 10 TO 18 V)	Reg_{line}	–	1.0	20	mV
Load Regulation (I_O = 0 mA to 10 mA)	Reg_{load}	–	1.0	20	mV
Total Output Variation Over Line, Load, and Temperature	V_{ref}	4.9	–	5.3	V
Output Short Circuit Current	I_O	25	100	190	mA
Reference Undervoltage Lockout Threshold	V_{th}	3.8	4.3	4.8	V
ERROR AMPLIFIER					
Input Offset Voltage (V_{CM} = 1.5 V)	V_{IO}	–	1.0	10	mV
Input Bias Current (V_{CM} = 1.5 V)	I_{IB}	–	0.2	1.0	μA
Input Offset Current (V_{CM} = 1.5 V)	I_{IO}	–	0	0.5	μA
Open Loop Voltage Gain (V_{CM} = 1.5 V, V_O = 2.0 V)	A_{VOL}	70	100	–	dB
Gain Bandwidth Product (f = 100 kHz)	GBW	3.0	5.0	–	MHz
Input Common Mode Rejection Ratio (V_{CM} = 1.5 to 5.0 V)	CMR	70	95	–	dB
Power Supply Rejection Ratio (V_{CC} = 10 to 18 V, f = 120 Hz)	PSR	80	100	–	dB
Output Voltage Swing High State Low State	 V_{OH} V_{OL}	 2.8 –	 3.2 0.6	 – 0.8	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 12 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for the MC34067 = – 40°C for the MC33067 T_{high} = + 70°C for MC34067 = + 85°C for MC33067

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V [Note 2], R_{OSC}= 18.2 k, R_{VFO} = 2940, C_{OSC} = 300 pF, R_T = 2370 k, C_T = 300 pF, C_L = 1.0 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (Error Amp Output Low) T_A = 25°C Total Variation (V_{CC} = 10 to 18 V, T_A = T_{Low} to T_{High}	$f_{OSC(low)}$	 500 490	 525 –	 540 550	kHz
Frequency (Error Amp Output High) T_A = 25°C Total Variation (V_{CC} = 10 to 18 V, T_A = T_{Low} to T_{High}	$f_{OSC(high)}$	 1900 1850	 2050 –	 2150 2200	kHz
Oscillator Control Input Voltage, Pin 3 @ 25°C	V_{in}	–	2.5	–	V
ONE–SHOT					
Drive Output Off–Time T_A = 25°C Total Variation (V_{CC} = 10 to 18 V, T_A = T_{Low} to T_{High}	t_{Blank}	 235 225	 250 –	 270 280	ns
DRIVE OUTPUTS					
Output Voltage Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	 V_{OL} V_{OH} 	 – – 9.5 9.0	 0.8 1.5 10.3 9.7	 1.2 2.0 – –	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.8	1.2	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	20	50	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	15	50	ns
FAULT COMPARATOR					
Input Threshold	V_{th}	0.93	1.0	1.07	V
Input Bias Current ($V_{Pin\ 10}$ = 0 V)	I_{IB}	–	– 2.0	– 10	µA
Propagation Delay to Drive Outputs (100 mV Overdrive)	$t_{PLH(In/Out)}$	–	60	100	ns
SOFT–START					
Capacitor Charge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{chg}	4.5	9.0	14	µA
Capacitor Discharge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{dischg}	3.0	8.0	–	mA
UNDERVOLTAGE LOCKOUT					
Startup Threshold, V_{CC} Increasing Enable/UVLO Adjust Pin Open Enable/UVLO Adjust Pin Connected to V_{CC}	$V_{th(UVLO)}$	 14.8 8.0	 16 9.0	 17.2 10	V
Minimum Operating Voltage After Turn–On Enable/UVLO Adjust Pin Open Enable/UVLO Adjust Pin Connected to V_{CC}	$V_{CC(min)}$	 8.0 7.6	 9.0 8.6	 10 9.6	V
Enable/UVLO Adjust Shutdown Threshold Voltage	$V_{th(Enable)}$	6.0	7.0	–	V
Enable/UVLO Adjust Input Current (Pin 9 = 0 V)	$I_{in(Enable)}$	–	– 0.2	– 1.0	mA
TOTAL DEVICE					
Power Supply Current (Enable/UVLO Adjust Pin Open) Startup (V_{CC} = 13.5 V) Operating (f_{OSC} = 500 kHz) (Note 2)	I_{CC}	 – –	 0.5 27	 0.8 35	mA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 12 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for the MC34067 = – 40°C for the MC33067 T_{high} = + 70°C for MC34067 = + 85°C for MC33067

Figure 1. Oscillator Timing Resistor versus Discharge Time

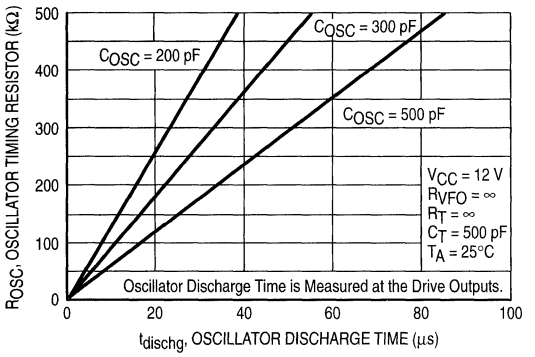


Figure 2. Oscillator Frequency versus Oscillator Control Current

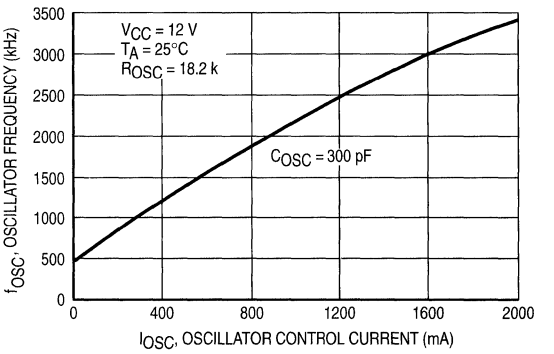


Figure 3. Error Amp Output Saturation Voltage versus Oscillator Control Current

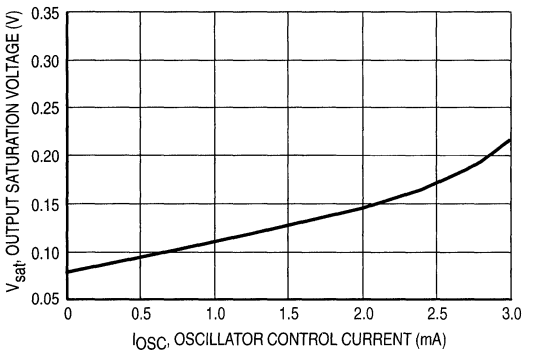


Figure 4. One–Shot Timing Resistor versus Period

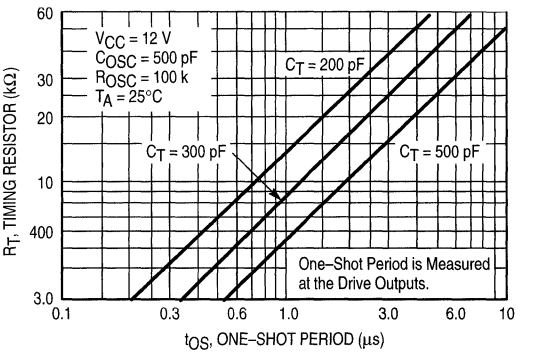


Figure 5. Open Loop Voltage Gain and Phase versus Frequency

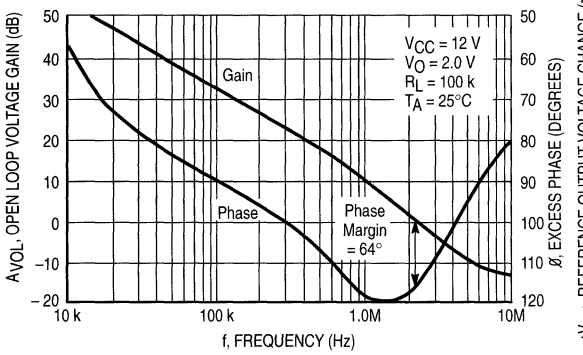


Figure 6. Reference Output Voltage Change versus Temperature

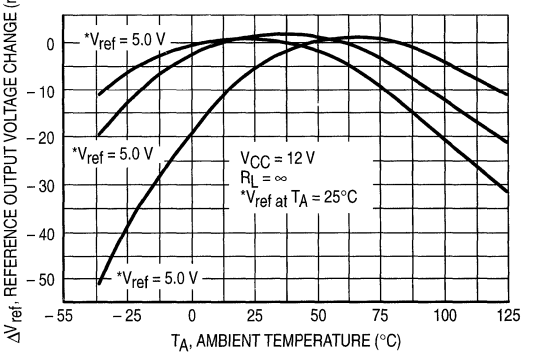


Figure 7. Reference Voltage Change versus Source Current

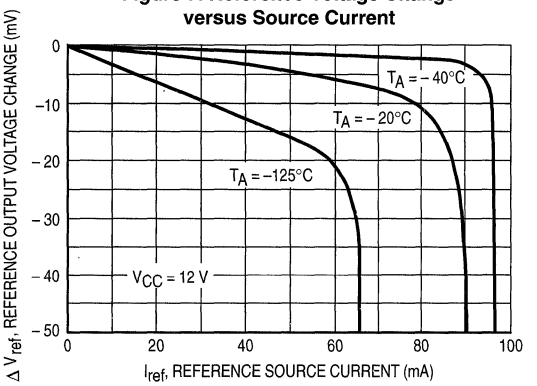


Figure 8. Drive Output Saturation Voltage versus Load Current

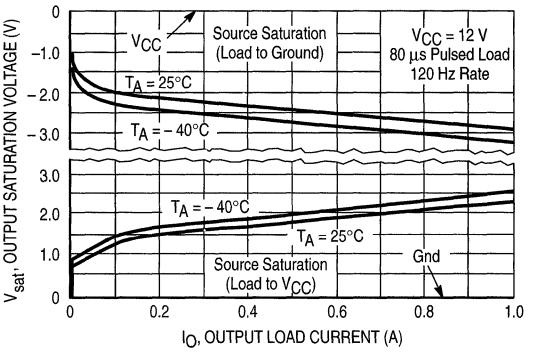


Figure 9. Drive Output Waveform

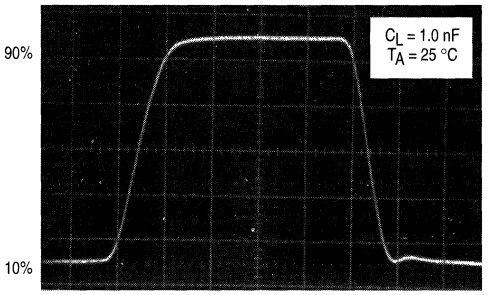


Figure 10. Soft–Start Saturation Voltage versus Capacitor Discharge Current

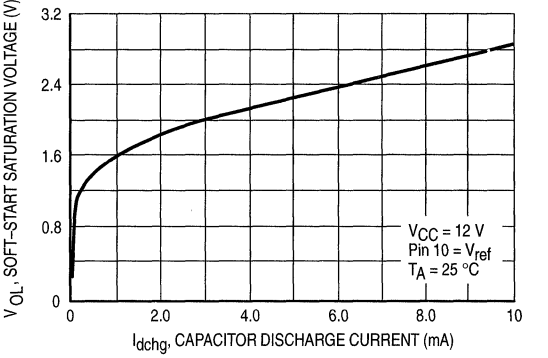


Figure 11. Operating Frequency versus Supply Current

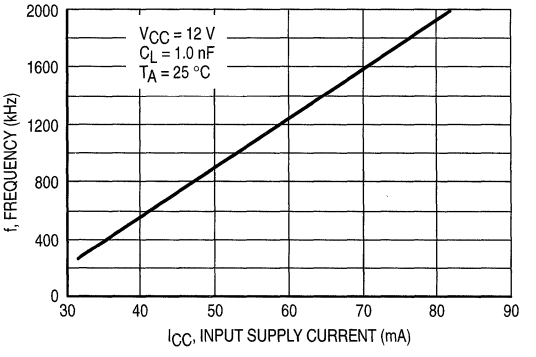


Figure 12. Supply Current versus Supply Voltage

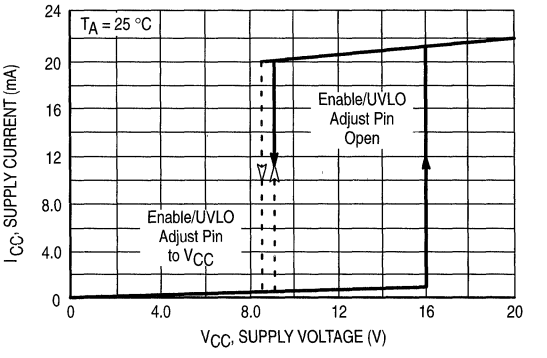
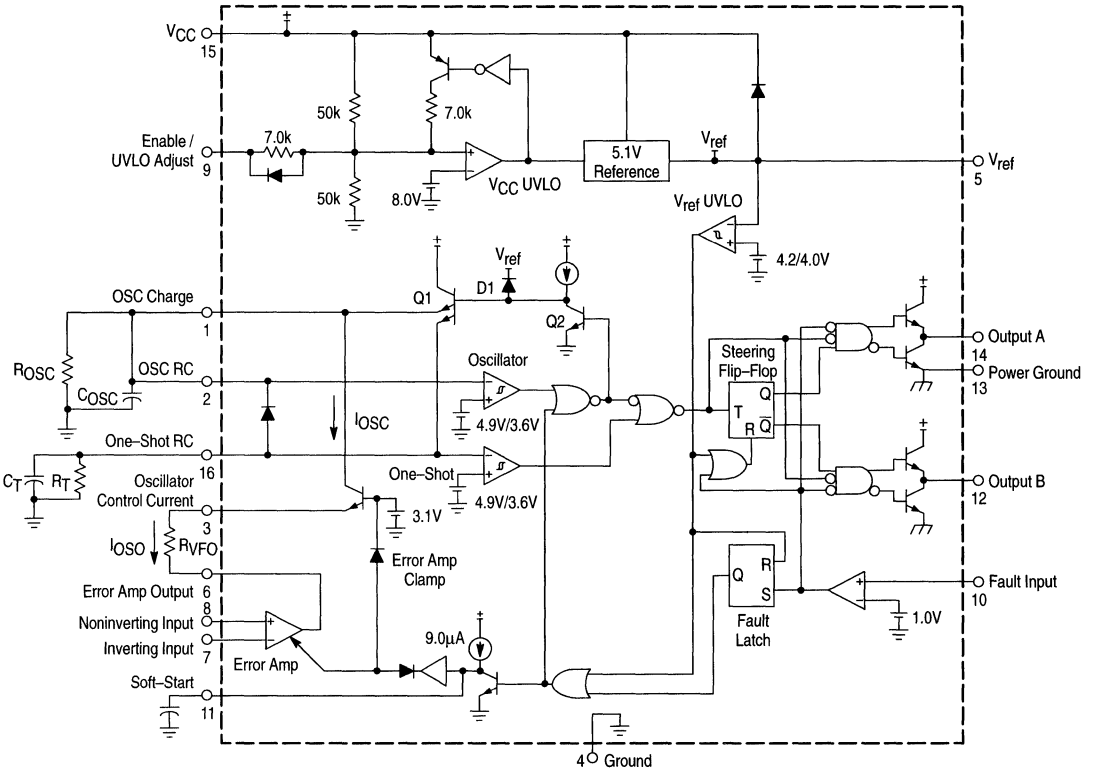
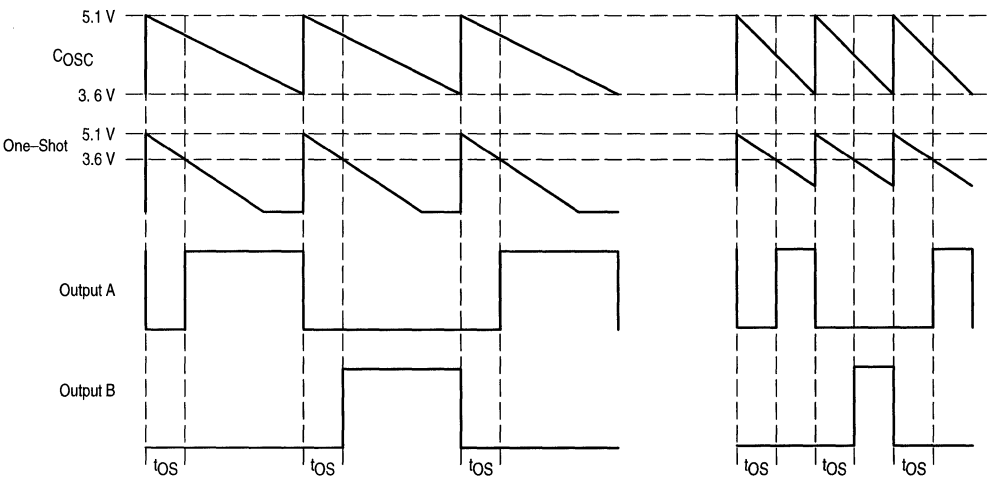


Figure 13. MC34067 Representative Block Diagram



Timing Diagram



Error Amp output high, minimum I_{OSC} current occurring at minimum input voltage, maximum load.

Error Amp output low, maximum I_{OSC} current occurring at maximum input voltage, minimum load.

OPERATING DESCRIPTION

Introduction

As power supply designers have strived to increase power conversion efficiency and reduce passive component size, high frequency resonant mode power converters have emerged as attractive alternatives to conventional pulse–width modulated control. When compared to pulse–width modulated converters, resonant mode control offers several benefits including lower switching losses, higher efficiency, lower EMI emission, and smaller size. A new integrated circuit has been developed to support this trend in power supply design. The MC34067 Resonant Mode Controller is a high performance bipolar IC dedicated to variable frequency power control at frequencies exceeding 1.0 MHz. This integrated circuit provides the features and performance specifically for zero voltage switching resonant mode power supply applications.

The primary purpose of the control chip is to provide a fixed off–time to the gates of external power MOSFETs at a repetition rate regulated by a feedback control loop. Additional features of the IC ensure that system startup and fault conditions are administered in a safe, controlled manner.

A simplified block diagram of the IC is shown on the front page, which identifies the main functional blocks and the block–to–block interconnects. Figure 13 is a detailed functional diagram which accurately represents the internal circuitry. The various functions can be divided into two sections. The first section includes the primary control path which produces precise output pulses at the desired frequency. Included in this section are a variable frequency Oscillator, a One–Shot, a pulse Steering Flip–Flop, a pair of power MOSFET Drivers, and a wide bandwidth Error Amplifier. The second section provides several peripheral support functions including a voltage reference, undervoltage lockout, Soft–Start circuit, and a fault detector.

Primary Control Path

The output pulse width and repetition rate are regulated through the interaction of the variable frequency Oscillator, One–Shot timer and Error Amplifier. The Oscillator triggers the One–Shot which generates a pulse that is alternately steered to a pair of totem pole output drivers by a toggle Flip–Flop. The Error Amplifier monitors the output of the regulator and modulates the frequency of the Oscillator. High speed Schottky logic is used throughout the primary control channel to minimize delays and enhance high frequency characteristics.

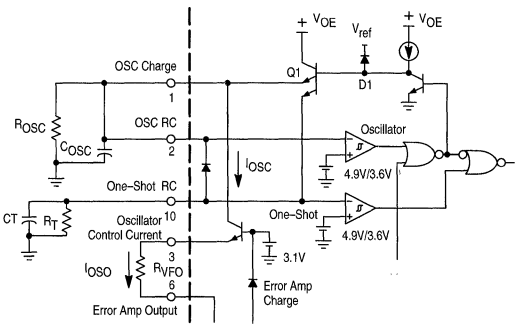
Oscillator

The characteristics of the variable frequency Oscillator are crucial for precise controller performance at high operating frequencies. In addition to triggering the One–Shot timer and initiating the output deadtime, the oscillator also determines the initial voltage for the one–shot capacitor. The Oscillator is designed to operate at frequencies exceeding 1.0 MHz. The Error Amplifier can control the oscillator frequency over a 1000:1 frequency range, and both the minimum and maximum frequencies are easily and accurately programmed by the proper selection of external components.

The functional diagram of the Oscillator and One–Shot timer is shown in Figure 14. The oscillator capacitor (C_{OSC}) is initially charged by transistor Q1. When C_{OSC} exceeds the 4.9 V upper threshold of the oscillator comparator, the base of Q1 is pulled low allowing C_{OSC} to discharge through the external resistor, (R_{OSC}), and the oscillator control current, (I_{OSC}). When the voltage on C_{OSC} falls below the comparator's 3.6 V lower threshold, Q1 turns on and again charges C_{OSC}.

C_{OSC} charges from 3.6 V to 5.1 V in less than 50 ns. The high slew rate of C_{OSC} and the propagation delay of the comparator make it difficult to control the peak voltage. This accuracy issue is overcome by clamping the base of Q1 through a diode to a voltage reference. The peak voltage of the oscillator waveform is thereby precisely set at 5.1 V.

Figure 14. Oscillator and One–Shot Timer



The frequency of the Oscillator is modulated by varying the current flowing out of the Oscillator Control Current (I_{OSC}) pin. The I_{OSC} pin is the output of a voltage regulator. The input of the voltage regulator is tied to the variable frequency oscillator. The discharge current of the Oscillator increases by increasing the current out of the I_{OSC} pin. Resistor R_{VFO} is used in conjunction with the Error Amp output to change the I_{OSC} current. Maximum frequency occurs when the Error Amplifier output is at its low state with a saturation voltage of 0.1 V at 1.0 mA.

The minimum oscillator frequency will result when the I_{OSC} current is zero, and C_{OSC} is discharged through the external resistor (R_{OSC}). This occurs when the Error Amplifier output is at its high state of 2.5 V. The minimum and maximum oscillator frequencies are programmed by the proper selection of resistor R_{OSC} and R_{VFO}. The minimum frequency is programmed by R_{OSC} using Equation 1:

$$R_{OSC} = \frac{\frac{1}{f_{(min)}} - t_{PD}}{C_{OSC}\,\ell n\left(\frac{5.1}{3.6}\right)} = \frac{t_{(max)} - 70\ ns}{0.348\,C_{OSC}} \qquad (1)$$

where t_{PD} is the internal propagation delay.

The maximum oscillator frequency is set by the current through resistor R_{VFO}. The current required to discharge C_{OSC} at the maximum oscillator frequency can be calculated by Equation 2:

$$I_{(max)} = C_{OSC}\frac{5.1 - 3.6}{\frac{1}{f_{(max)}}} = 1.5C_{OSC}f_{(max)} \quad (2)$$

The discharge current through R_{OSC} must also be known and can be calculated by Equation 3:

$$I_{R_{OSC}} = \frac{5.1 - 3.6}{R_{OSC}}\varepsilon^{\left(-\frac{\frac{1}{f_{(min)}}}{R_{OSC}C_{OSC}}\right)} = \frac{1.5}{R_{OSC}}\varepsilon^{\left(-\frac{1}{f_{(min)}R_{OSC}C_{OSC}}\right)} \quad (3)$$

Resistor R_{VFO} can now be calculated by Equation 4:

$$R_{VFO} = \frac{2.5 - V_{EAsat}}{I_{(max)} - I_{R_{OSC}}} \quad (4)$$

One–Shot Timer

The One–Shot is designed to disable both outputs simultaneously providing a deadtime before either output is enabled. The One–Shot capacitor (C_T) is charged concurrently with the oscillator capacitor by transistor Q1, as shown in Figure 14. The one–shot period begins when the oscillator comparator turns off Q1, allowing C_T to discharge. The period ends when resistor R_T discharges C_T to the threshold of the One–Shot comparator. The lower threshold of the One–Shot is 3.6 V. By choosing C_T, R_T can by solved by Equation 5:

$$R_T = \frac{t_{OS}}{C_T \ell n\left(\frac{5.1}{3.6}\right)} = \frac{t_{OS}}{0.348\ C_T} \quad (5)$$

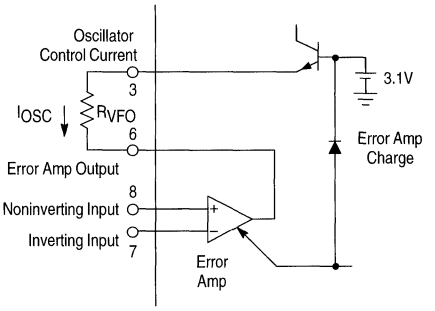
Errors in the threshold voltage and propagation delays through the output drivers will affect the One–Shot period. To guarantee accuracy, the output pulse of the control chip is trimmed to within 5% of 250 ns with nominal values of R_T and C_T.

The outputs of the Oscillator and One–Shot comparators are OR'd together to produce the pulse t_{OS}, which drives the Flip–Flop and output drivers. The output pulse (t_{OS}) is initiated by the Oscillator and terminated by the One–Shot comparator. With zero–voltage resonant mode converters, the oscillator discharge time should never be set less than the one–shot period.

Error Amplifier

A fully accessible high performance Error Amplifier is provided for feedback control of the power supply system. The Error Amplifier is internally compensated and features dc open loop gain greater than 70 dB, input offset voltage of less than 10 mV and a guaranteed minimum gain–bandwidth product of 2.5 MHz. The input common mode range extends from 1.5 V to 5.1 V, which includes the reference voltage.

Figure 15. Error Amplifier and Clamp

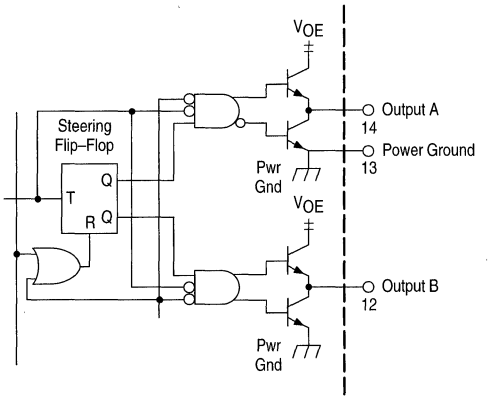


When the Error Amplifier output is coupled to the I_{OSC} pin by R_{VFO}, as illustrated in Figure 15, it provides the Oscillator Control Current, I_{OSC}. The output swing of the Error Amplifier is restricted by a clamp circuit to improve its transient recovery time.

Output Section

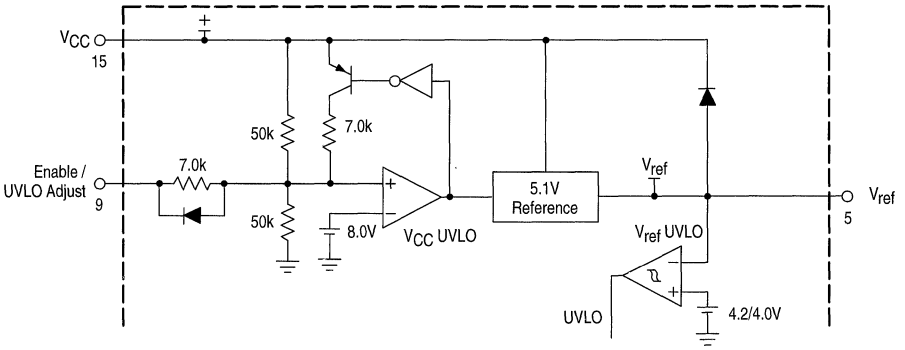
The pulse(t_{OS}), generated by the Oscillator and One–Shot timer is gated to dual totem–pole output drives by the Steering Flip–Flop shown in Figure 16. Positive transitions of t_{OS} toggle the Flip–Flop, which causes the pulses to alternate between Output A and Output B. The flip–flop is reset by the undervoltage lockout circuit during startup to guarantee that the first pulse appears at Output A.

Figure 16. Steering Flip–Flop and Output Drivers



The totem–pole output drivers are ideally suited for driving power MOSFETs and are capable of sourcing and sinking 1.5 A. Rise and fall times are typically 20 ns when driving a 1.0 nF load. High source/sink capability in a totem–pole driver normally increases the risk of high cross conduction current during output transitions. The MC34067 utilizes a unique design that virtually eliminates cross conduction, thus controlling the chip power dissipation at high frequencies. A separate power ground pin is provided to isolate the sensitive analog circuitry from large transient currents.

Figure 17. Undervoltage Lockout and Reference



PERIPHERAL SUPPORT FUNCTIONS

The MC34067 Resonant Controller provides a number of support and protection functions including a precision voltage reference, undervoltage lockout comparators, soft–start circuitry, and a fault detector. These peripheral circuits ensure that the power supply can be turned on and off in a controlled manner and that the system will be quickly disabled when a fault condition occurs.

Undervoltage Lockout and Voltage Reference

Separate undervoltage lockout comparators sense the input V_{CC} voltage and the regulated reference voltage as illustrated in Figure 17. When V_{CC} increases to the upper threshold voltage, the V_{CC} UVLO comparator enables the Reference Regulator. After the V_{ref} output of the Reference Regulator rises to 4.2 V, the V_{ref} UVLO comparator switches the UVLO signal to a logic zero state enabling the primary control path. Reducing V_{CC} to the lower threshold voltage causes the V_{CC} UVLO comparator to disable the Reference Regulator. The V_{ref} UVLO comparator then switches the UVLO output to a logic one state disabling the controller.

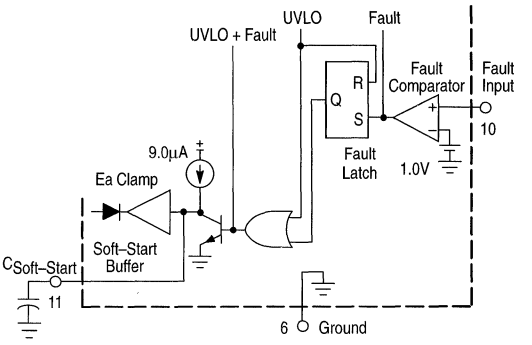
The Enable/UVLO Adjust pin allows the power supply designer to select the V_{CC} UVLO threshold voltages. When this pin is open, the comparator switches the controller on at 16 V and off at 9.0 V. If this pin is connected to the V_{CC} terminal, the upper and lower thresholds are reduced to 9.0 V and 8.6 V, respectively. Forcing the Enable/UVLO Adjust pin low will pull the V_{CC} UVLO comparator input low (through an internal diode) turning off the controller.

The Reference Regulator provides a precise 5.1 V reference to internal circuitry and can deliver up to 10 mA to external loads. The reference is trimmed to better than 2% initial accuracy and includes active short circuit protection.

Fault Detector

The high speed Fault Comparator and Latch illustrated in Figure 18 can protect a power supply from destruction under fault conditions. The Fault Input pin connects to the input of the Fault Comparator. If this input exceeds the 1.0 V threshold of the comparator, the Fault Latch is set and two logic signals simultaneously disable the primary control path. The signal labeled "Fault" at the output of the Fault Comparator is connected directly to the output drivers. This direct path reduces the propagation delay from the Fault Input to the A and B outputs to typically 70 ns. The Fault Latch output is OR'd with the UVLO output from the V_{ref} UVLO comparator to produce the logic output labeled "UVLO+Fault". This signal disables the Oscillator and One–Shot by forcing both the C_{OSC} and C_T capacitors to be continually charged.

Figure 18. Fault Detector and Soft–Start



The Fault Latch is reset during startup by a logic "1" at the UVLO output of the V_{ref} UVLO comparator. The latch can also be reset after startup by pulling the Enable/UVLO Adjust pin momentarily low to disable the Reference Regulator.

Soft–Start Circuit

The Soft–Start circuit shown in Figure 18 forces the variable frequency Oscillator to start at the maximum frequency and ramp downward until regulated by the feedback control loop. The external capacitor at the $C_{Soft–Start}$ terminal is initially discharged by the UVLO+Fault signal. The low voltage on the capacitor passes through the Soft–Start Buffer to hold the Error Amplifier output low. After UVLO+Fault switches to a logic zero, the soft–start capacitor is charged by a 9.0 µA current source. The buffer allows the Error Amplifier output to follow the soft–start capacitor until it is regulated by the Error Amplifier inputs. The soft–start function is generally applicable to controllers operating below resonance and can be disabled by simply opening the $C_{Soft–Start}$ terminal.

APPLICATIONS INFORMATION

The MC34067 is specifically designed for zero voltage switching (ZVS) quasi–resonant converter (QRC) applications. The IC is optimized for double–ended push–pull or bridge type converters operating in continuous conduction mode. Operation of this type of ZVS with resonant properties is similar to standard push–pull or bridge circuits in that the energy is transferred during the transistor on–time. The difference is that a series resonant tank is usually introduced to shape the voltage across the power transistor prior to turn–on. The resonant tank in this topology is not used to deliver energy to the output as is the case with zero current switch topologies. When the power transistor is enabled the voltage across it should already be zero, yielding minimal switching loss. Figure 19 shows a timing diagram for a half–bridge ZVS QRC. An application circuit is shown in Figure 20. The circuit built is a dc to dc half–bridge converter delivering 75 W to the output from a 48 V source.

When building a zero voltage switch (ZVS) circuit, the objective is to waveshape the power transistor's voltage waveform so that the voltage across the transistor is zero when the device is turned on. The purpose of the control IC is to allow a resonant tank to waveshape the voltage across the power transistor while still maintaining regulation. This is accomplished by maintaining a fixed deadtime and by varying the frequency; thus the effective duty cycle is changed.

Primary side resonance can be used with ZVS circuits. In the application circuit, the elements that make the resonant tank are the primary leakage inductance of the transformer (L_L) and the average output capacitance (C_{OSS}) of a power MOSFET (C_R). The desired resonant frequency for the application circuit is calculated by Equation 6:

$$f_r = \frac{1}{2\pi\sqrt{L_L 2C_R}} \qquad (6)$$

In the application circuit, the operating voltage is low and the value of C_{OSS} versus Drain Voltage is known. Because the C_{OSS} of a MOSFET changes with drain voltage, the value of the C_R is approximated as the average C_{OSS} of the MOSFET. For the application circuit the average C_{OSS} can be calculated by Equation 7:

$$C_R = \sqrt{2} * C_{OSS} \text{ measured at } \frac{1}{2} V_{in} \qquad (7)$$

The MOSFET chosen fixes C_R and that L_L is adjusted to achieve the desired resonant frequency.

However, the desired resonant frequency is less critical than the leakage inductance. Figure 19 shows the primary current ramping toward its peak value during the resonant transition. During this time, there is circulating current flowing through the secondary inductance, which effectively makes the primary inductance appear shorted. Therefore, the current through the primary will ramp to its peak value at a rate controlled by the leakage inductance and the applied voltage. Energy is not transferred to the secondary during this stage, because the primary current has not overcome the circulating current in the secondary. The larger the leakage inductance, the longer it takes for the primary current to slew. The practical effect of this is to lower the duty cycle, thus reducing the operating range.

The maximum duty cycle is controlled by the leakage inductance, not by the MC34067. The One–Shot in the MC34067 only assures that the power switch is turned on under a zero voltage condition. Adjust the one–shot period so that the output switch is activated while the primary current is slewing but before the current changes polarity. The resonant stage should then be designed to be as long as the time for the primary current to go to zero amps.

Figure 19. Application Timing Diagram

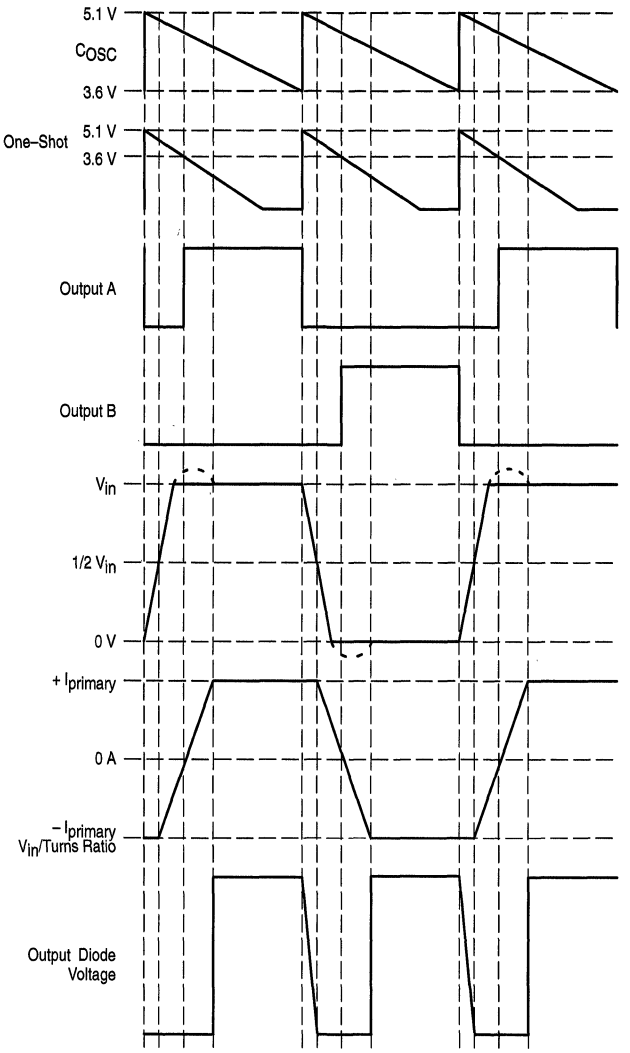
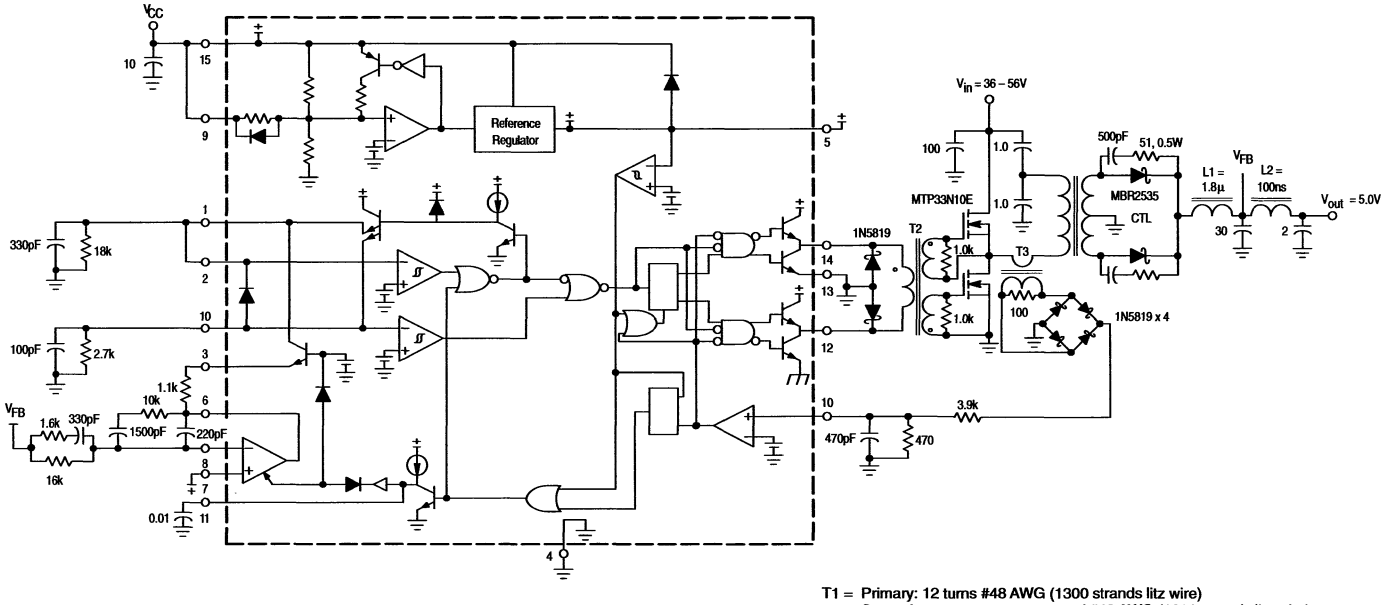


Figure 20. Application Circuit



Test	Conditions	Results
Line Regulation	V_{in} = 40 V to 56 V, I_O =15 A	20 mV = ±0.198%
Load Regulation	V_{in} = 48 V, I_O = 10 A to 15 A	4.0 mV = ±0.039%
Output Ripple	V_{in} = 48 V, I_O = 15 A, f_{switch} = 1.0 MHz	25 mV_{p-p}
Efficiency	V_{in} = 48 V, I_O = 10 A, f_{switch} = 1.7 MHz V_{in} = 48 V, I_O = 15 A, f_{switch} = 1.0 MHz	83.5% 84.2%

T1 = Primary: 12 turns #48 AWG (1300 strands litz wire)
Secondary: 6 turns center tapped #48 AWG (1300 strands litz wire)
Core: Philips 3F3 4312 020 4124
Bobbin: Philips 4322 021 3525
Primary Leakage Inductance = 1.0 µH

T2 = All windings: 8 turns #36 AWG
Core: Philips 3F3 EP7–3F3
Bobbin: Philips EP7PCB1–6

T3 = Coilcraft D1870 (100 turns)

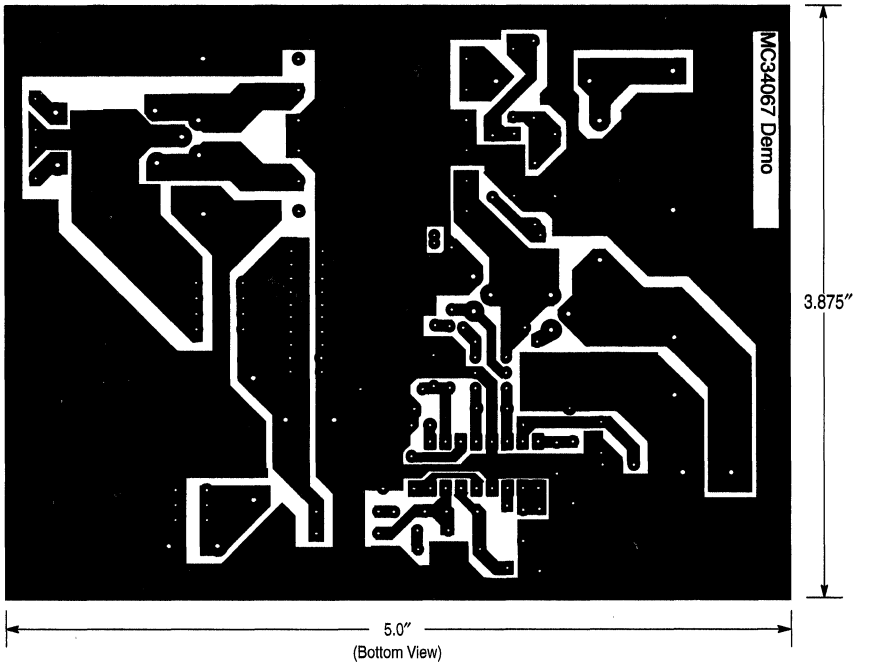
L1 = 2 turns #48 AWG (1300 strands litz wire)
Core: Philips 3F3 EP10–3F3
Bobbin: Philips EP10PCB1–8
Inductance = 1.8 µH

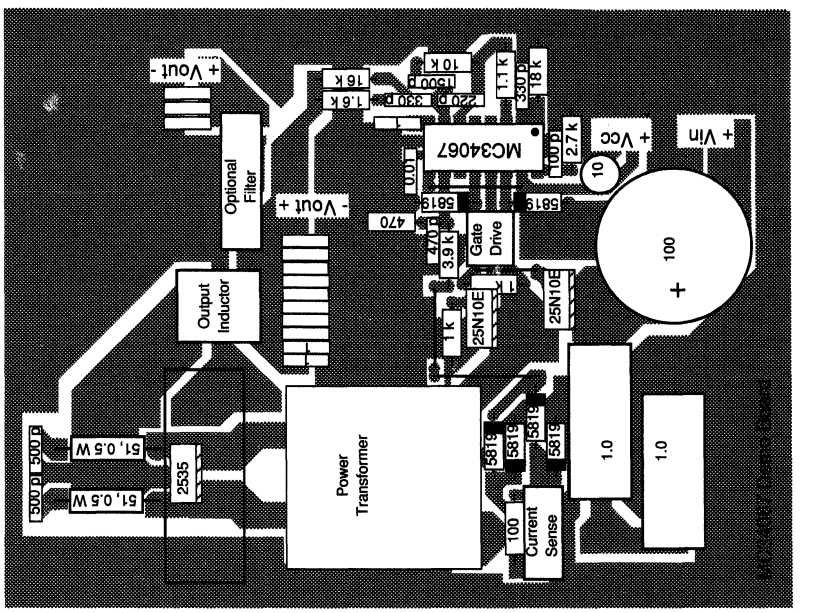
L2 = 5 turns #48 AWG (1300 strands litz wire)
Core: 0.5″ diameter air code
Inductance = 100 nH

Heatsinks = AAVID Engineering Inc. 533402B02552 with clip
MC34067–5803

Insulators = Berquist Sil–Pad 1500

Figure 21. Printed Circuit Board and Component Layout





(Top View)

MC34129
MC33129

High Performance Current Mode Controllers

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

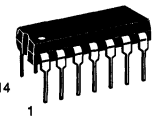
SEMICONDUCTOR TECHNICAL DATA

The MC34129/MC33129 are high performance current mode switching regulators specifically designed for use in low power digital telephone applications. These integrated circuits feature a unique internal fault timer that provides automatic restart for overload recovery. For enhanced system efficiency, a start/run comparator is included to implement bootstrapped operation of V_{CC}. Other functions contained are a temperature compensated reference, reference amplifier, fully accessible error amplifier, sawtooth oscillator with sync input, pulse width modulator comparator, and a high current totem pole driver ideally suited for driving a power MOSFET.

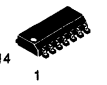
Also included are protective features consisting of soft–start, undervoltage lockout, cycle–by–cycle current limiting, adjustable deadtime, and a latch for single pulse metering.

Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in many other applications.

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Continuous Retry after Fault Timeout
- Soft–Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- High Current Totem Pole Driver
- Input Undervoltage Lockout
- Low Startup and Operating Current
- Direct Interface with Motorola SENSEFET Products

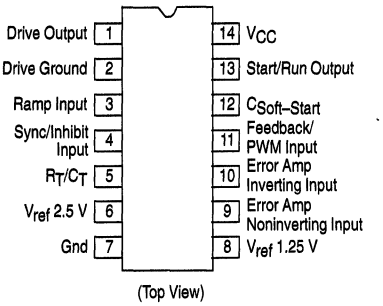


P SUFFIX
PLASTIC PACKAGE
CASE 646



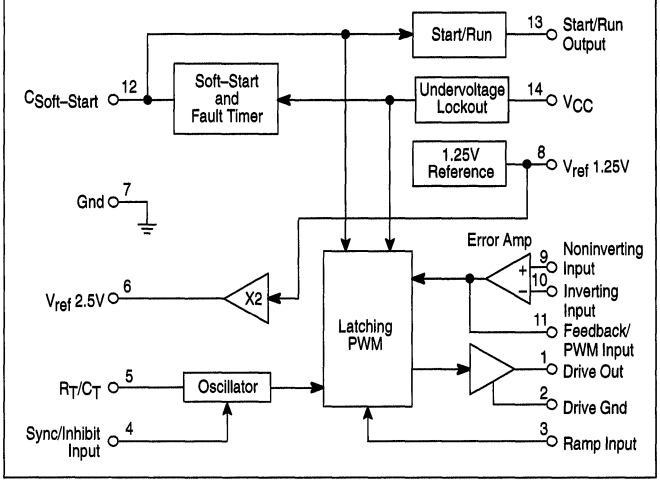
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34129D	T_A = 0° to +70°C	SO–14
MC34129P		Plastic DIP
MC33129D	T_A = –40° to +85°C	SO–14
MC33129P		Plastic DIP

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(VCC)}$	50	mA
Start/Run Output Zener Current	$I_{Z(Start/Run)}$	50	mA
Analog Inputs (Pins 3, 5, 9, 10, 11, 12)	–	–0.3 to 5.5	V
Sync Input Voltage	V_{sync}	–0.3 to V_{CC}	V
Drive Output Current, Source or Sink	I_{DRV}	1.0	A
Current, Reference Outputs (Pins 6, 8)	I_{ref}	20	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Case 751A Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air P Suffix, Plastic Package Case 646 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 552 145 800 100	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34129 MC33129	T_A	 0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTIONS					
Reference Output Voltage, T_A = 25°C 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.225 2.375	 1.250 2.500	 1.275 2.625	V
Reference Output Voltage, T_A = T_{low} to T_{high} 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.200 2.250	 – –	 1.300 2.750	V
Line Regulation (V_{CC} = 4.0 V to 12 V) 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	Reg_{line}	 – –	 2.0 10	 12 50	mV
Load Regulation 1.25 V Ref., I_L = –10 μA to +500 μA 2.50 V Ref., I_L = –0.1 mA to +1.0 mA	Reg_{load}	 – –	 1.0 3.0	 12 25	mV
ERROR AMPLIFIER					
Input Offset Voltage (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	V_{IO}	 – –	 1.5 –	 – 10	mV
Input Offset Current (V_{in} = 1.25 V)	I_{IO}	–	10	–	nA
Input Bias Current (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	I_{IB}	 – –	 25 –	 – 200	nA
Input Common Mode Voltage Range	V_{ICR}	–	0.5 to 5.5	–	V
Open Loop Voltage Gain (V_O = 1.25 V)	A_{VOL}	65	87	–	dB
Gain Bandwidth Product (V_O = 1.25 V, f = 100 kHz)	GBW	500	750	–	kHz
Power Supply Rejection Ratio (V_{CC} = 5.0 V to 10 V)	PSRR	65	85	–	dB
Output Source Current (V_O = 1.5 V)	I_{Source}	40	80	–	μA
Output Voltage Swing High State (I_{Source} = 0 μA) Low State (I_{Sink} = 500 μA)	 V_{OH} V_{OL}	 1.75 –	 1.96 0.1	 2.25 0.15	V

NOTE: 1. T_{low} = 0°C for MC34129, –40°C for MC33129 T_{high} = +70°C for MC34129, +85°C for MC33129

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR					
Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	150	275	400	mV
Input Bias Current	I_{IB}	–	–120	–250	µA
Propagation Delay, Ramp Input to Drive Output	$t_{PLH(IN/DRV)}$	–	250	–	ns
SOFT–START					
Capacitor Charge Current (Pin 12 = 0 V)	I_{chg}	0.75	1.2	1.50	µA
Buffer Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	–	15	40	mV
Buffer Output Voltage (I_{Sink} = 100 µA)	V_{OL}	–	0.15	0.225	V
FAULT TIMER					
Restart Delay Time	t_{DLY}	200	400	600	µs
START/RUN COMPARATOR					
Threshold Voltage (Pin 12)	V_{th}	–	2.0	–	V
Threshold Hysteresis Voltage (Pin 12)	V_H	–	350	–	mV
Output Voltage (I_{Sink} = 500 µA)	V_{OL}	9.0	10	10.3	V
Output Off–State Leakage Current (V_{OH} = 15 V)	$I_{S/R(leak)}$	–	0.4	2.0	µA
Output Zener Voltage (I_Z = 10 mA)	V_Z	–	(V_{CC} + 7.6)	–	V
OSCILLATOR					
Frequency (R_T = 25.5 kΩ, C_T = 390 pF)	f_{OSC}	80	100	120	kHz
Capacitor C_T Discharge Current (Pin 5 = 1.2 V)	I_{dischg}	240	350	460	µA
Sync Input Current High State (V_{in} = 2.0 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 – –	 40 15	 125 35	µA
Sync Input Resistance	R_{in}	12.5	32	50	kΩ
DRIVE OUTPUT					
Output Voltage High State (I_{Source} = 200 mA) Low State (I_{Source} = 200 mA)	 V_{OH} V_{OL}	 8.3 –	 8.9 1.4	 – 1.8	V
Low State Holding Current	I_H	–	225	–	µA
Output Voltage Rise Time (C_L = 500 pF)	t_r	–	390	–	ns
Output Voltage Fall Time (C_L = 500 pF)	t_f	–	30	–	ns
Output Pull–Down Resistance	R_{PD}	100	225	350	kΩ
UNDERVOLTAGE LOCKOUT					
Startup Threshold	V_{th}	3.0	3.6	4.2	V
Hysteresis	V_H	5.0	10	15	%
TOTAL DEVICE					
Power Supply Current R_T = 25.5 kΩ, C_T = 390 pF, C_L = 500 pF	I_{CC}	1.0	2.5	4.0	mA
Power Supply Zener Voltage (I_Z = 10 mA)	V_Z	12	14.3	–	V

NOTE: 1. T_{low} = 0°C for MC34129, –40°C for MC33129 T_{high} = +70°C for MC34129, +85°C for MC33129

3

Figure 1. Timing Resistor versus Oscillator Frequency

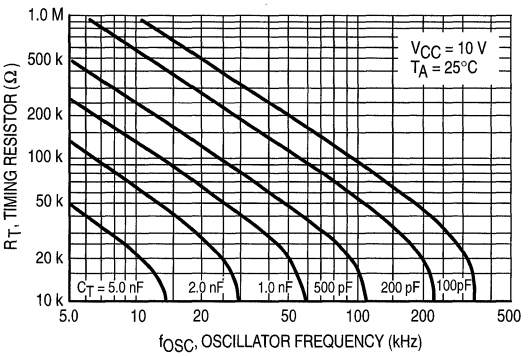


Figure 2. Output Deadtime versus Oscillator Frequency

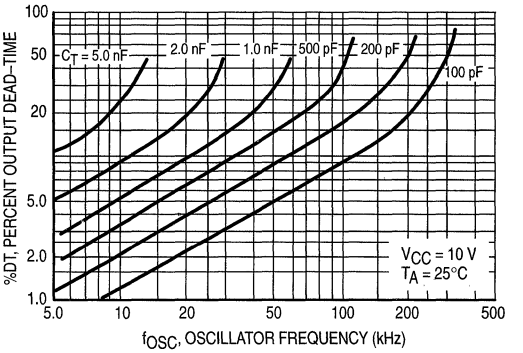


Figure 3. Oscillator Frequency Change versus Temperature

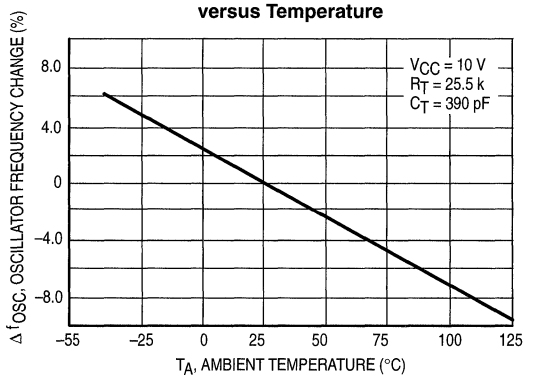


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency

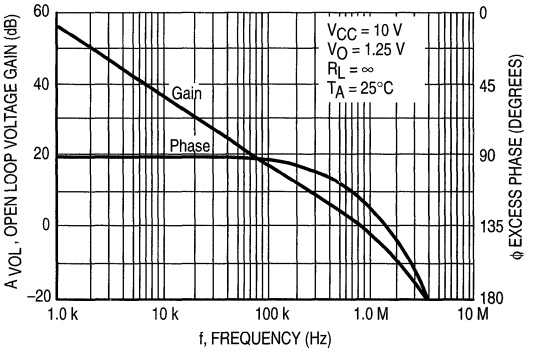


Figure 5. Error Amp Small–Signal Transient Response

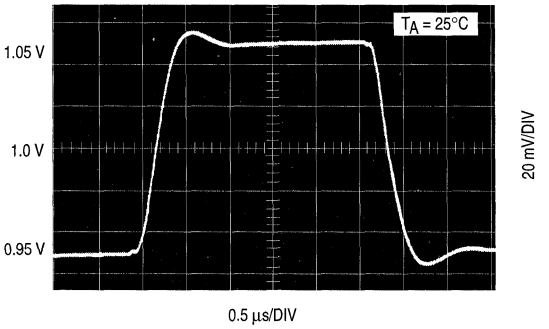


Figure 6. Error Amp Large–Signal Transient Response

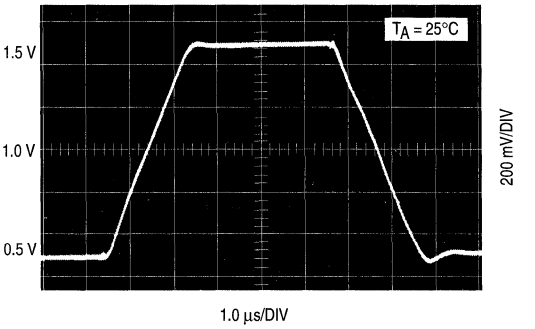


Figure 7. Error Amp Open Loop DC Gain versus Load Resistance

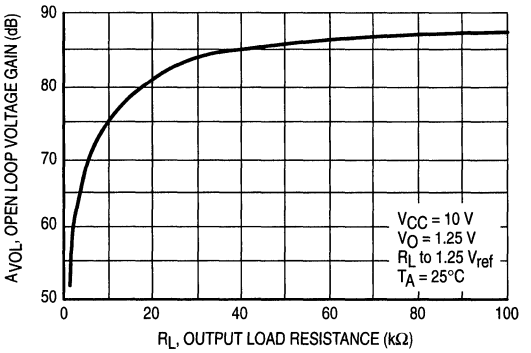


Figure 8. Error Amp Output Saturation versus Sink Current

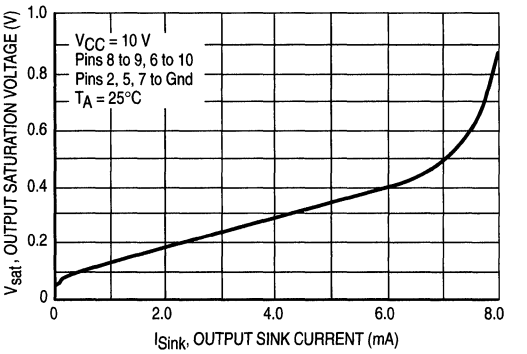


Figure 9. Soft–Start Buffer Output Saturation versus Sink Current

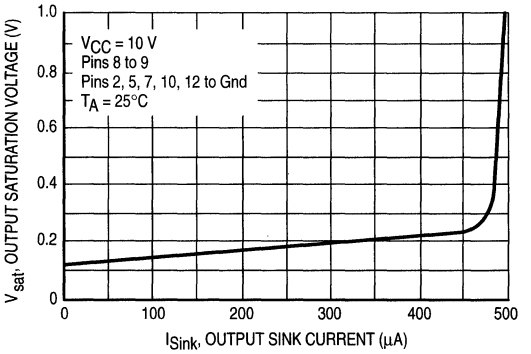


Figure 10. Reference Output Voltage versus Supply Voltage

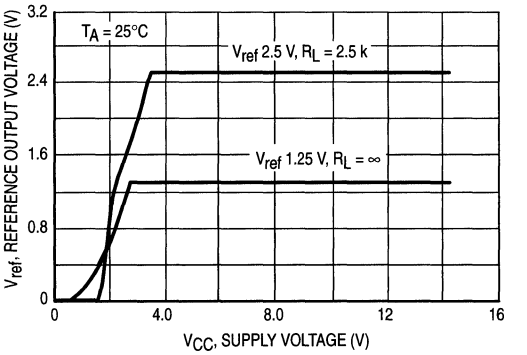


Figure 11. 1.25 V Reference Output Voltage Change versus Source Current

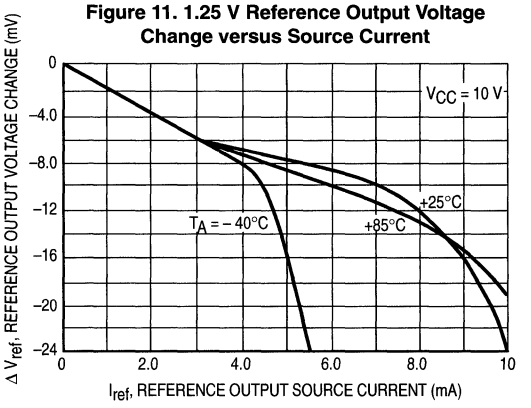
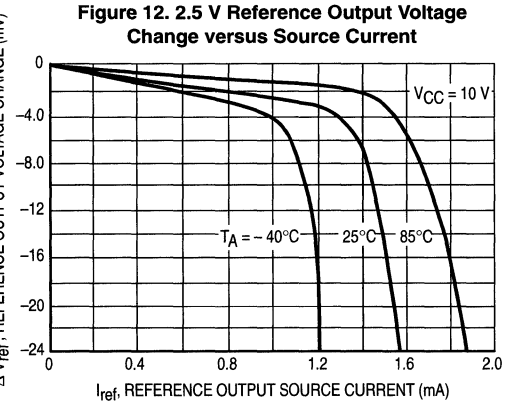


Figure 12. 2.5 V Reference Output Voltage Change versus Source Current



3

Figure 13. 1.25 V Reference Output Voltage versus Temperature

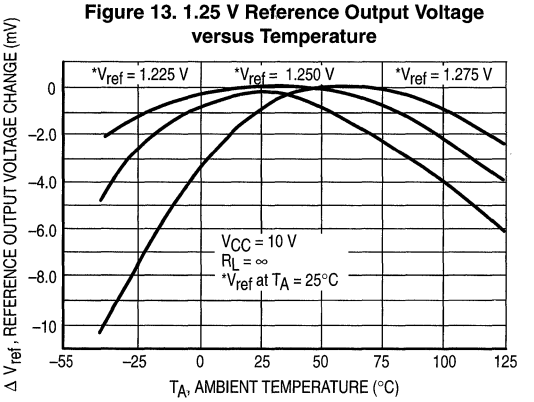


Figure 14. 2.5 V Reference Output Voltage versus Temperature

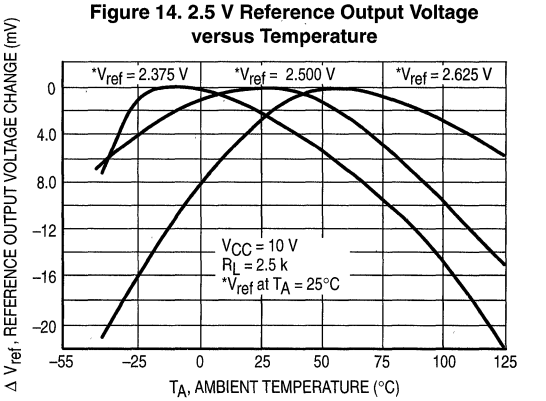


Figure 15. Drive Output Saturation versus Load Current

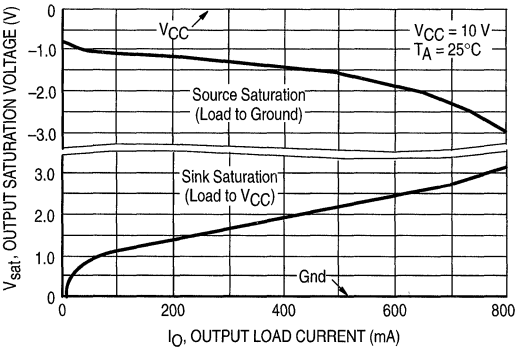


Figure 16. Drive Output Waveform

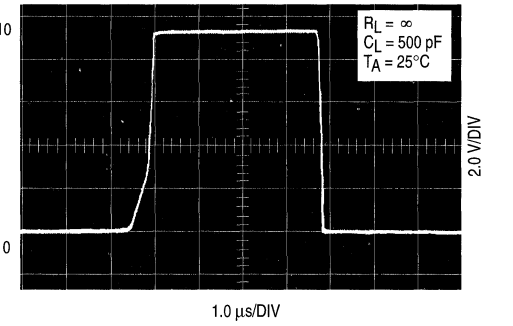
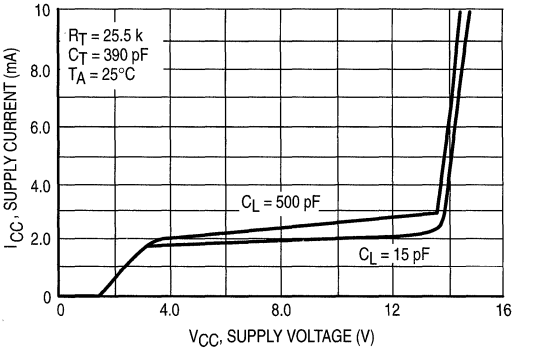


Figure 17. Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Drive Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sinked by this pin.
2	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
3	Ramp Input	A voltage proportional to the inductor current is connected to this input. The PWM uses this information to terminate output switch conduction.
4	Sync/Inhibit Input	A rectangular waveform applied to this input will synchronize the Oscillator and limit the maximum Drive Output duty cycle. A dc voltage within the range of 2.0 V to V_{CC} will inhibit the controller.
5	R_T/C_T	The free–running Oscillator frequency and maximum Drive Output duty cycle are programmed by connecting resistor R_T to V_{ref} 2.5 V and capacitor C_T to Ground. Operation to 300 kHz is possible.
6	V_{ref} 2.50 V	This output is derived from V_{ref} 1.25 V. It provides charging current for capacitor C_T through resistor R_T.
7	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
8	V_{ref} 1.25 V	This output furnishes a voltage reference for the Error Amplifier noninverting input.
9	Error Amp Noninverting Input	This is the noninverting input of the Error Amplifier. It is normally connected to the 1.25 V reference.
10	Error Amp Inverting Input	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
11	Feedback/PWM Input	This pin is available for loop compensation. It is connected to the Error Amplifier and Soft–Start Buffer outputs, and the Pulse Width Modulator input.
12	$C_{Soft–Start}$	A capacitor $C_{Soft–Start}$ is connected from this pin to Ground for a controlled ramp–up of peak inductor current during startup.
13	Start/Run Output	This output controls the state of an external bootstrap transistor. During the start mode, operating bias is supplied by the transistor from V_{in}. In the run mode, the transistor is switched off and bias is supplied by an auxiliary power transformer winding.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 4.2 V to 12 V.

OPERATING DESCRIPTION

The MC34129 series are high performance current mode switching regulator controllers specifically designed for use in low power telecommunication applications. Implementation will allow remote digital telephones and terminals to shed their power cords and derive operating power directly from the twisted pair used for data transmission. Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in a wide range of converter applications. A representative block diagram is shown in Figure 18.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 2.5 V reference through resistor R_T to approximately 1.25 V and discharged by an internal current sink to ground. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the lower input of the NOR gate high. This causes the Drive Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows Oscillator Frequency versus R_T and Figure 2 Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a give frequency. In many noise sensitive applications it may be desirable to frequency–lock one or more switching regulators to an external system clock. This can be accomplished by applying the clock signal to the Synch/Inhibit Input. For reliable locking, the free–running oscillator frequency should be about 10% less than the clock frequency. Referring to the timing diagram shown Figure 19, the rising edge of the clock signal applied to the Sync/Inhibit Input, terminates charging of C_T and Drive Output conduction. By tailoring the clock waveform, accurate duty cycle clamping of the Drive Output can be achieved. A circuit method is shown in Figure 20. The Sync/Inhibit Input may also be used as a means for system shutdown by applying a dc voltage that is within the range of 2.0 V to V_{CC}.

PWM Comparator and Latch

The MC34129 operates as a current mode controller whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches a threshold level established by the output of the Error Amp or Soft–Start Buffer (Pin 11). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The PWM Comparator–Latch configuration used, ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground–referenced resistor R_S in series with the source of output switch Q_1. The Ramp Input adds an offset of 275 mV to this voltage to guarantee that no pulses appear at the Drive Output when Pin 11 is at its lowest state. This occurs at the beginning of the soft–start interval or when the power supply is operating and the load is removed. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 11 where:

$$I_{pk} = \frac{V_{(Pin\ 11)} - 0.275\ V}{R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the voltage at Pin 11 will be internally clamped to 1.95 V by the output of the Soft–Start Buffer. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.95\ V - 0.275}{R_S} = \frac{1.675\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method which adjusts this voltage in discrete increments is shown in Figure 22. This method is possible because the Ramp Input bias current is always negative (typically –120 μA). A positive temperature coefficient equal to that of the diode string will be exhibited by $I_{pk(max)}$. An adjustable method that is more precise and temperature stable is shown in Figure 23. Erratic operation due to noise pickup can result if there is an excessive reduction of the clamp voltage. In this situation, high frequency circuit layout techniques are imperative.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 25.

Error Amp and Soft–Start Buffer

A fully–compensated Error Amplifier with access to both inputs and output is provided for maximum design flexibility. The Error Amplifier output is common with that of the Soft–Start Buffer. These outputs are open–collector (sink only) and are ORed together at the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the loop. Soft–Start is mandatory for stable startup when power is provided through a high source impedance such as the long twisted pair used in telecommunications. It effectively removes the load from the output of the switching power supply upon initial startup. The Soft–Start Buffer is configured as a unity gain follower with the noninverting input connected to Pin 12. An internal 1.0 μA current source charges the soft–start capacitor ($C_{Soft–Start}$) to an internally clamped level of 1.95 V. The rate of change of peak inductor current, during startup, is programmed by the capacitor value selected. Either the Fault Timer or the Undervoltage Lockout can discharge the soft–start capacitor.

Figure 18. Representative Block Diagram

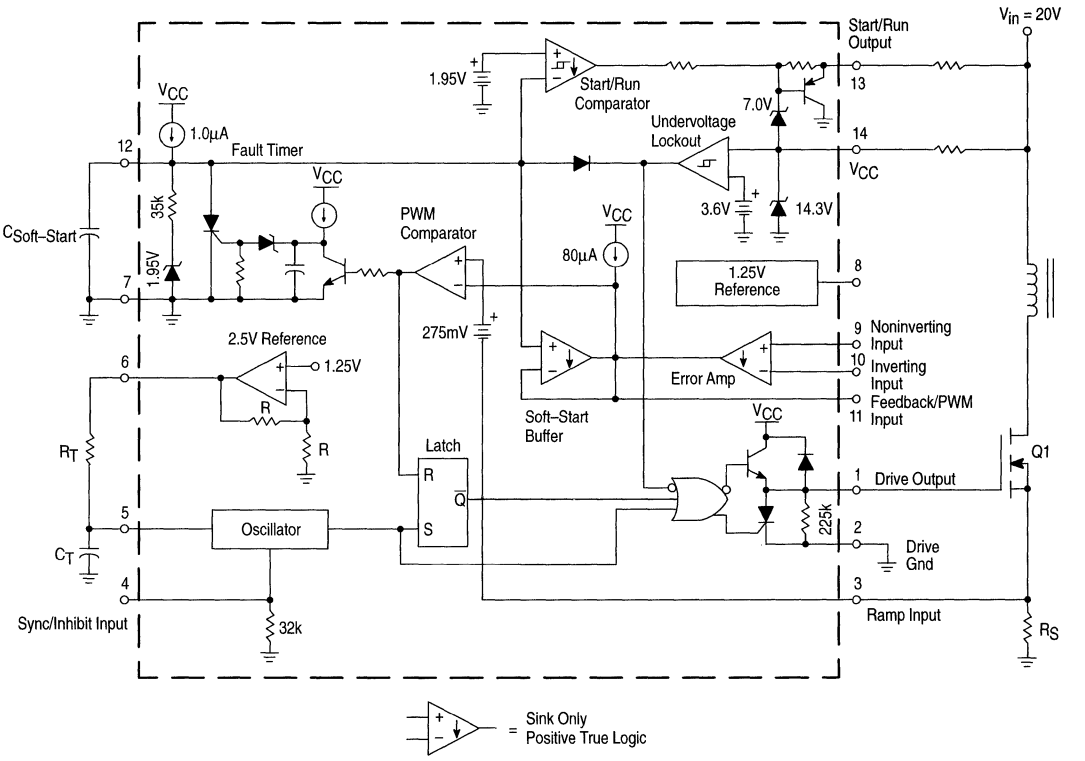
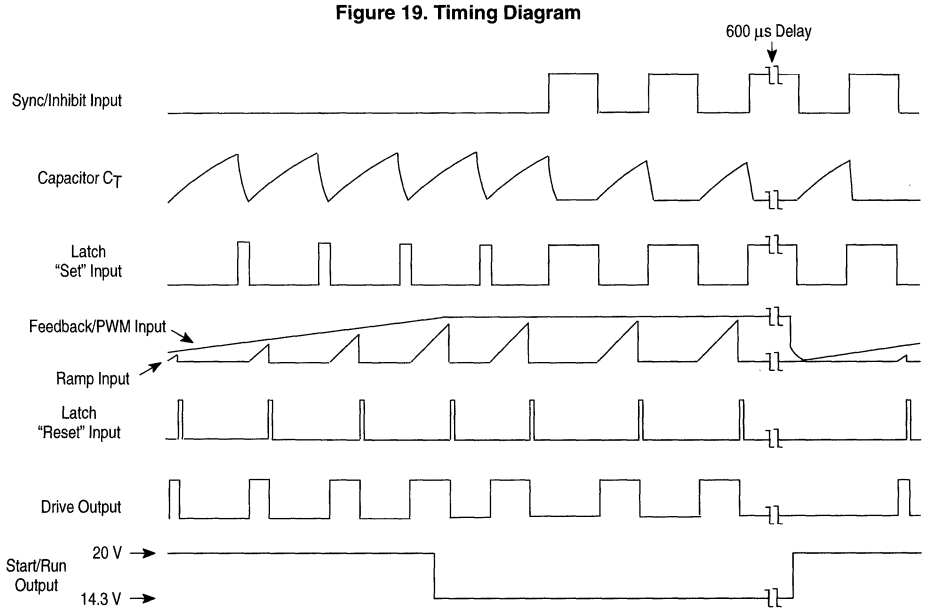


Figure 19. Timing Diagram



Fault Timer

This unique circuit prevents sustained operating in a lockout condition. This can occur with conventional switching control ICs when operating from a power source with a high series impedance. If the power required by the load is greater than that available from the source, the input voltage will collapse, causing the lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions, the output of the PWM Comparator will reset the Latch and discharge the internal Fault Timer capacitor on a cycle–by–cycle basis. Under operating conditions where the required power into the load is greater than that available from the source (V_{in}), the Ramp Input voltage (plus offset) will not reach the comparator threshold level (Pin 11), and the output of the PWM Comparator will remain low. If this condition persists for more that 600 μs, the Fault Timer will active, discharging $C_{Soft–Start}$ and initiating a soft–start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load power or source impedance is reduced. The minimum fault timeout is 200 μs, which limits the useful switching frequency to a minimum of 5.0 kHz.

Start/Run Comparator

A bootstrap startup circuit is included to improve system efficiency when operating from a high input voltage. The output of the Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 21. While $C_{Soft–Start}$ is charging, startup bias is supplied to V_{CC} (Pin 14) from V_{in} through transistor Q2. When $C_{Soft–Start}$ reaches the 1.95 V clamp level, the Start–Run output switches low (V_{CC} = 50 mV), turning off Q2. Operating bias is now derived from the auxiliary bootstrap winding of the transformer, and all drive power is efficiently converted down from V_{in}. The start time must be long enough for the power supply output to reach regulation. This will ensure that there is sufficient bias voltage at the auxiliary bootstrap winding for sustained operation.

$$t_{Start} = \frac{1.95 V C_{Soft–Start}}{1.0\ \mu A} = 1.95\ C_{Soft–Start\ in\ \mu F}$$

The Start/Run Comparator has 350 mV of hysteresis. The output off–state is clamped to V_{CC} + 7.6 V by the internal zener and PNP transistor base–emitter junction.

Drive Output and Drive Ground

The MC34129 contains a single totem–pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem–pole stage consists of an NPN transistor for turn–on drive and a high speed SCR for turn–off. The SCR design requires less average supply current (I_{CC}) when compared to conventional switching control ICs that use an all NPN totem–pole. The SCR accomplishes this during turn–off of the MOSFET, by utilizing the gate charge as regenerative on–bias, whereas the conventional all transistor design requires continuous base current. Conversion efficiency in low power applications is greatly enhanced with this reduction of I_{CC}. The SCR's low–state holding current (I_H) is typically 225 μA. An internal 225 kΩ pull–down resistor is included to shunt the Drive Output off–state leakage to ground when the Undervoltage Lockout is active. A separate Drive Ground is provided to reduce the effects of switching transient noise imposed on the Ramp Input. This feature becomes particularly useful when the $I_{pk(max)}$ clamp level is reduced. Figure 24 shows the proper implementation of the MC34129 with a current sensing power MOSFET.

Undervoltage Lockout

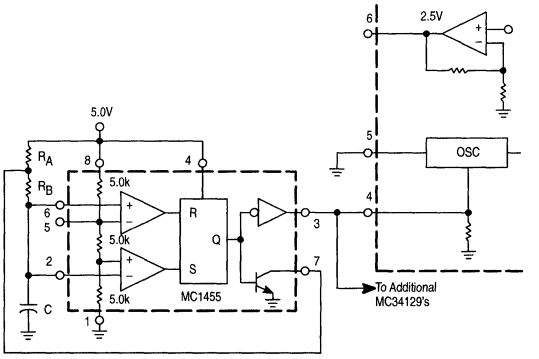
The Undervoltage Lockout comparator holds the Drive Output and $C_{Soft–Start}$ pins in the low state when V_{CC} is less than 3.6 V. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft–start cycle begins. A built–in hysteresis of 350 mV prevents erratic output behavior as V_{CC} crosses the comparator threshold voltage. A 14.3 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the MOSFET gate from excessive drove voltage during system startup. An external 9.1 V zener is required when driving low threshold MOSFETs. Refer to Figure 21. The minimum operating voltage range of the IC is 4.2 V to 12 V.

References

The 1.25 V bandgap reference is trimmed to ±2.0% tolerance at T_A = 25°C. It is intended to be used in conjunction with the Error Amp. The 2.50 V reference is derived from the 1.25 V reference by an internal op amp with a fixed gain of 2.0. It has an output tolerance of ±5.0% at T_A = 25°C and its primary purpose is to supply charging current to the oscillator timing capacitor.

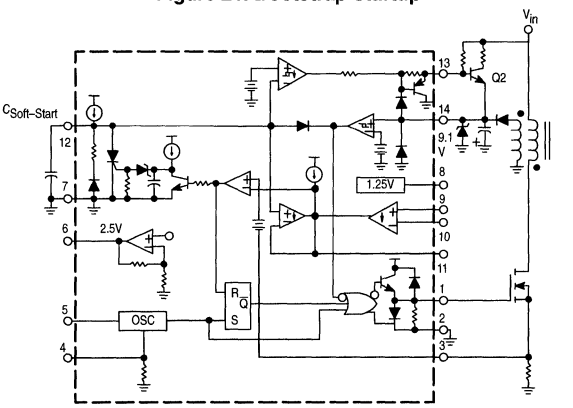
For further information, please refer to AN976.

Figure 20. External Duty Cycle Clamp and Multi–Unit Synchronization



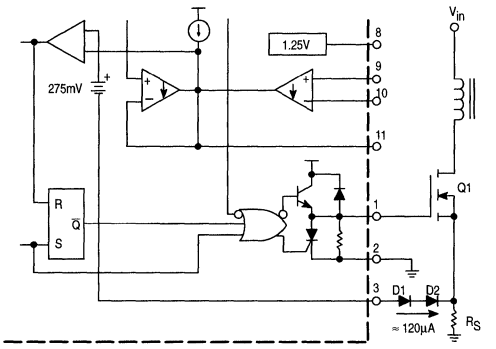
$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

Figure 21. Bootstrap Startup



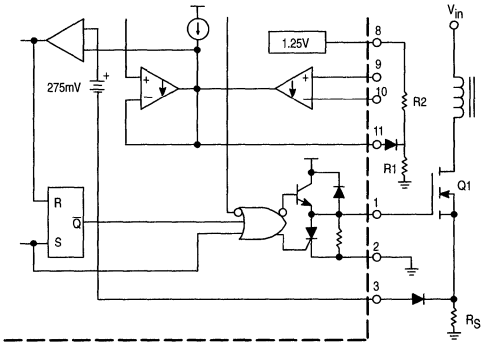
The external 9.1 V zener is required when driving low threshold MOSFETs.

Figure 22. Discrete Step Reduction of Clamp Level



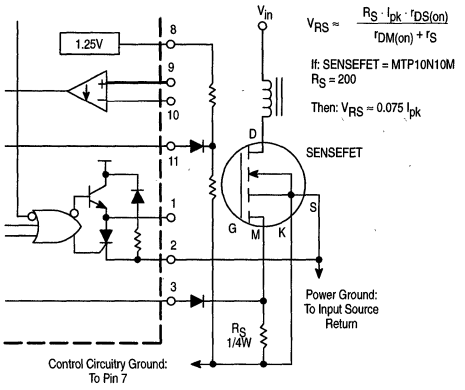
$$I_{pk(max)} = \frac{1.675 - (V_{F(D1)} + V_{F(D2)})}{R_S}$$

Figure 23. Adjustable Reduction of Clamp Level



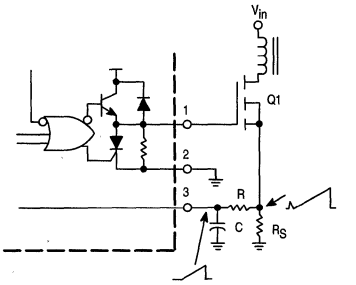
If: $\frac{1.25\ V}{R1 + R2} \geq 1.0\ mA$ Then: $I_{pk(max)} \approx \frac{\frac{1.25}{\left(\frac{R2}{R1} + 1\right)} - 0.275}{R_S}$

Figure 24. Current Sensing Power MOSFET



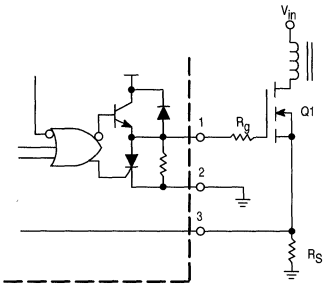
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch.

Figure 25. Current Waveform Spike Suppression



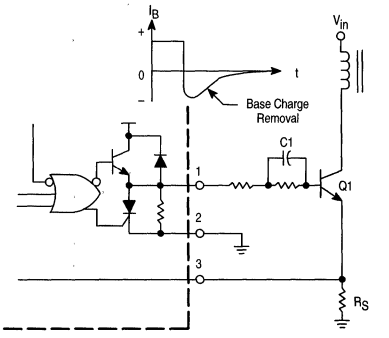
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 26. MOSFET Parasitic Oscillations



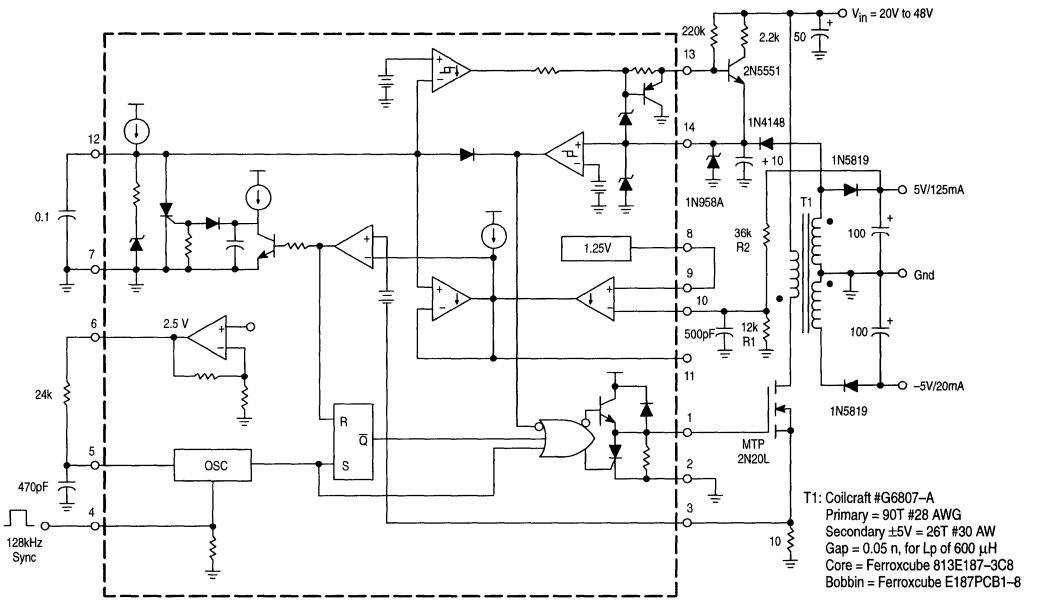
Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit.

Figure 27. Bipolar Transistor Drive



The totem–pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C1.

Figure 28. Non–Isolated 725 mW Flyback Regulator

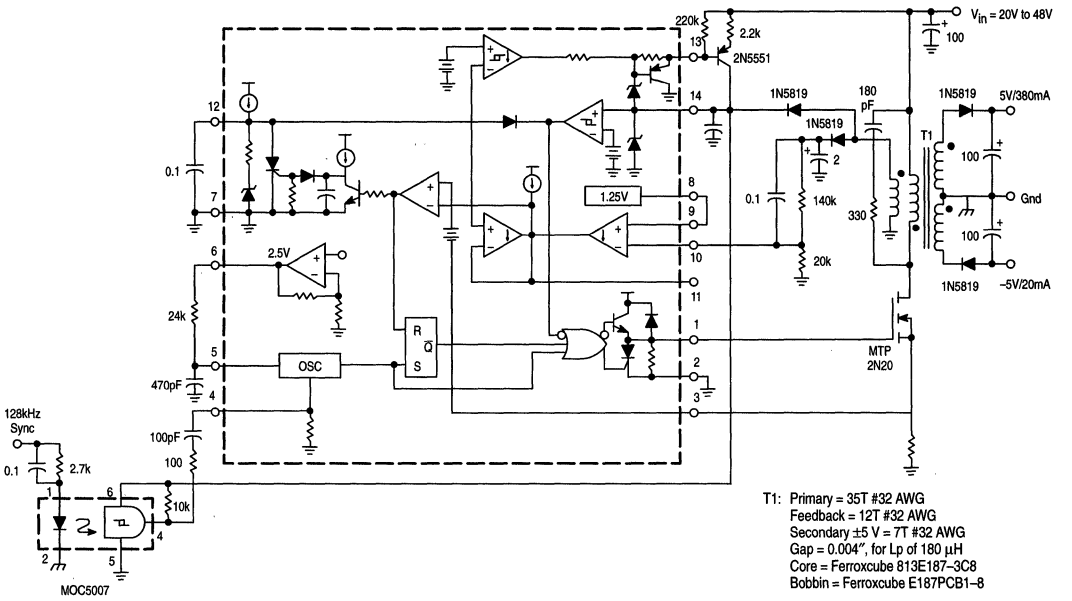


Test	Conditions	Results
Line Regulation 5.0 V	V_{in} = 20 V to 40 V, I_{out} 5.0 V = 125 mA, I_{out} –5.0 V = 20 mA	Δ = 1.0 mV
Load Regulation 5.0 V	V_{in} = 30 V, I_{out} 5.0 V = 0 mA to 150 mA, I_{out} –5.0 V = 20 mA	Δ = 2.0 mV
Output Ripple 5.0 V	V_{in} = 30 V, I_{out} 5.0 V = 125 mA, I_{out} –5.0 V = 20 mA	150 mVpp
Efficiency	V_{in} = 30 V, I_{out} 5.0 V = 125 mA, I_{out} –5.0 V = 20 mA	77%

$$V_{out} = 1.25 \left(\frac{R2}{R1} + 1 \right)$$

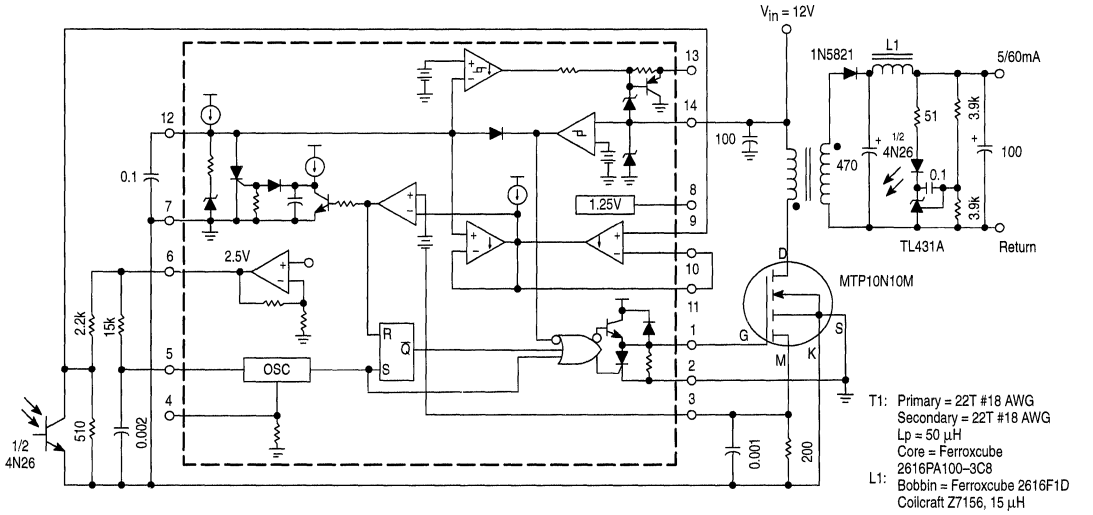
3

Figure 29. Isolated 2.0 W Flyback Regulator



Test	Conditions	Results
Line Regulation 5.0 V	V_{in} = 20 V to 40 V, I_{out} 5.0 V = 380 mA, I_{out} –5.0 V = 20 mA	Δ = 1.0 mV
Load Regulation 5.0 V	V_{in} = 30 V, I_{out} 5.0 V = 100 mA to 380 mA, I_{out} –5.0 V = 20 mA	Δ = 15 mV
Output Ripple 5.0 V	V_{in} = 30 V, I_{out} 5.0 V = 380 mA, I_{out} –5.0 V = 20 mA	150 mVpp
Efficiency	V_{in} = 30 V, I_{out} 5.0 V = 380 mA, I_{out} –5.0 V = 20 mA	73%

Figure 30. Isolated 3.0 W Flyback Regulator with Secondary Side Sensing



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 12 V, I_{out} 600 mA	Δ = 1.0 mV
Load Regulation	V_{in} = 12 V, I_{out} = 100 mA to 600 mA	Δ = 8.0 mV
Output Ripple	V_{in} = 12 V, I_{out} = 600 mA	20 mVpp
Efficiency	V_{in} = 12 V, I_{out} = 600 mA	81%

An economical method of achieving secondary sensing is to combine the TL431A with a 4N26 optocoupler.

MC34151
MC33151

3

High Speed Dual MOSFET Drivers

The MC34151/MC33151 are dual inverting high speed drivers specifically designed for applications that require low current digital circuitry to drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS and LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent erratic system operation at low supply voltages.

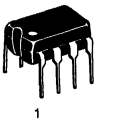
Typical applications include switching power supplies, dc to dc converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

These devices are available in dual–in–line and surface mount packages.

- Two Independent Channels with 1.5 A Totem Pole Output
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs
- Pin Out Equivalent to DS0026 and MMH0026

HIGH SPEED DUAL MOSFET DRIVERS

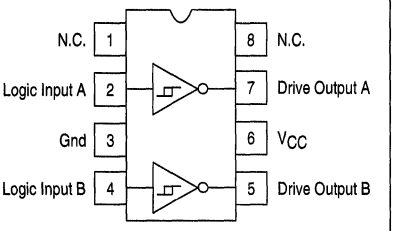
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

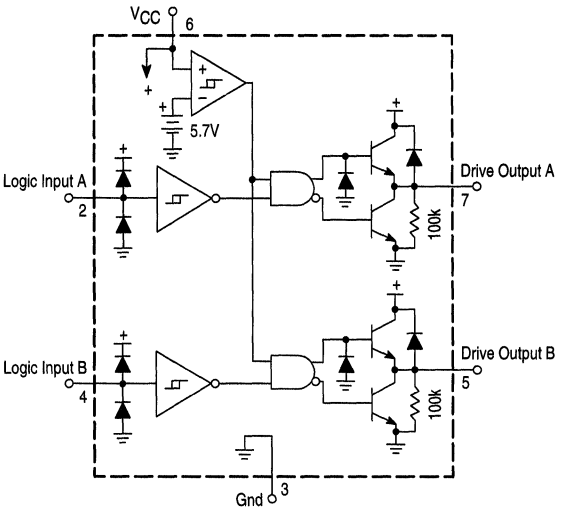
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34151D	T_A = 0° to +70°C	SO–8
MC34151P		Plastic DIP
MC33151D	T_A = –40° to +85°C	SO–8
MC33151P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Logic Inputs (Note 1)	V_{in}	–0.3 to V_{CC}	V
Drive Outputs (Note 2) Totem Pole Sink or Source Current Diode Clamp Current (Drive Output to V_{CC})	 I_O $I_{O(clamp)}$	 1.5 1.0	A
Power Dissipation and Thermal Characteristics D Suffix SO–8 Package Case 751 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air P Suffix 8–Pin Package Case 626 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 0.56 180 1.0 100	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34151 MC33151	T_A	 0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the only operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage – High State Logic 1 – Low State Logic 0	V_{IH} V_{IL}	2.6 –	1.75 1.58	– 0.8	V
Input Current – High State (V_{IH} = 2.6 V) – Low State (V_{IL} = 0.8 V)	I_{IH} I_{IL}	– –	200 20	500 100	μA
DRIVE OUTPUT					
Output Voltage – Low State (I_{Sink} = 10 mA) (I_{Sink} = 50 mA) (I_{Sink} = 400 mA) – High State (I_{Source} = 10 mA) (I_{Source} = 50 mA) (I_{Source} = 400 mA)	V_{OL} V_{OH} 	– – – 10.5 10.4 9.5	0.8 1.1 1.7 11.2 11.1 10.9	1.2 1.5 2.5 – – –	V
Output Pull–Down Resistor	R_{PD}	–	100	–	kΩ
SWITCHING CHARACTERISTICS (T_A = 25°C)					
Propagation Delay (10% Input to 10% Output, C_L = 1.0 nF) Logic Input to Drive Output Rise Logic Input to Drive Output Fall	 $t_{PLH(in/out)}$ $t_{PHL(in/out)}$	 – –	 35 36	 100 100	ns
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF C_L = 2.5 nF	t_r	– –	14 31	30 –	ns
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF C_L = 2.5 nF	t_f	– –	16 32	30 –	ns
TOTAL DEVICE					
Power Supply Current Standby (Logic Inputs Grounded) Operating (C_L = 1.0 nF Drive Outputs 1 and 2, f = 100 kHz)	I_{CC}	 – –	 6.0 10.5	 10 15	mA
Operating Voltage	V_{CC}	6.5	–	18	V

NOTES: 1. For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC}, whichever is less.
2. Maximum package power dissipation limits must be observed.
3. T_{low} = 0°C for MC34151, –40°C for MC33151; T_{high} = +70°C for MC34151, +85°C for MC33151

3

Figure 1. Switching Characteristics Test Circuit

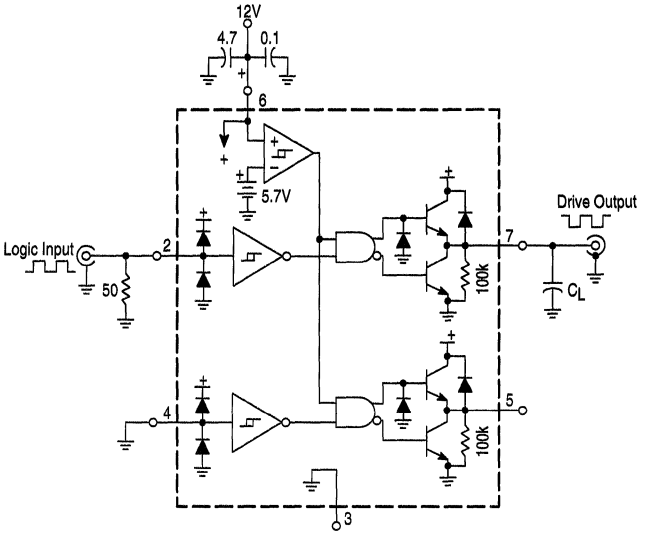


Figure 2. Switching Waveform Definitions

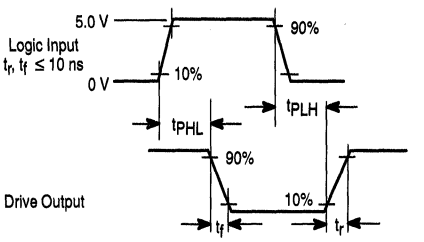


Figure 3. Logic Input Current versus Input Voltage

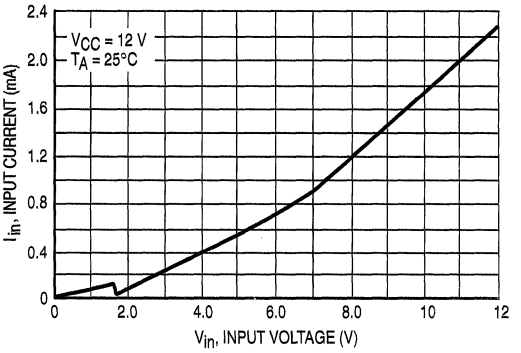


Figure 4. Logic Input Threshold Voltage versus Temperature

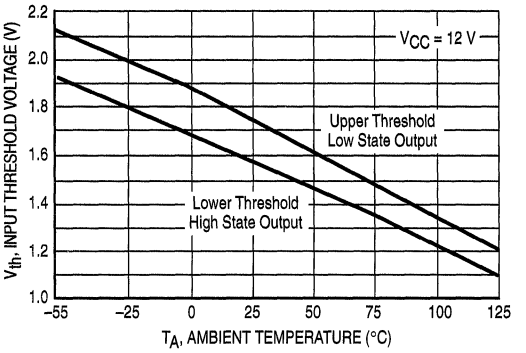


Figure 5. Drive Output Low–to–High Propagation Delay versus Logic Overdrive Voltage

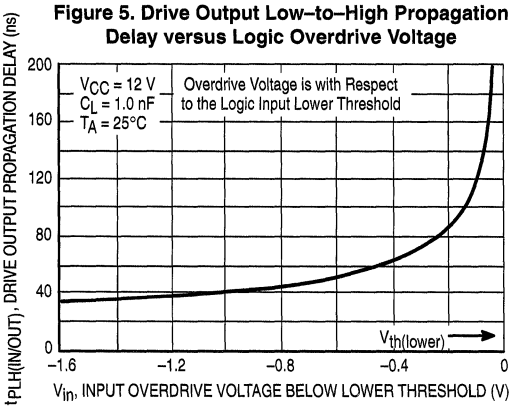


Figure 6. Drive Output High–to–Low Propagation Delay versus Logic Input Overdrive Voltage

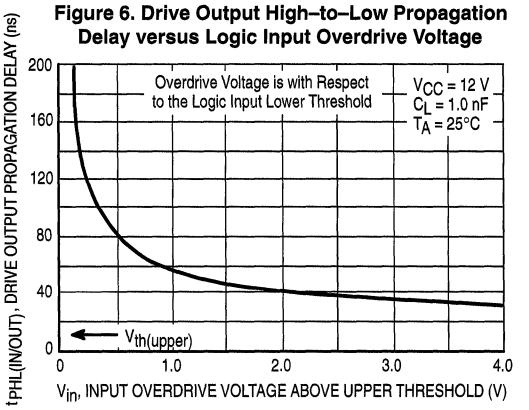


Figure 7. Propagation Delay

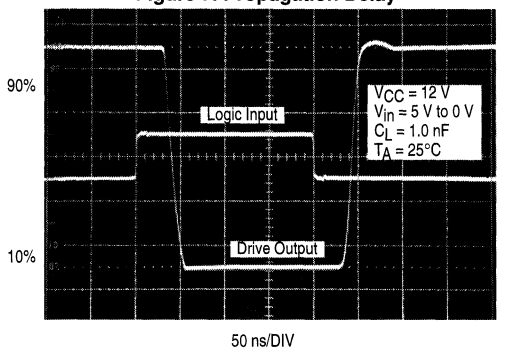


Figure 8. Drive Output Clamp Voltage versus Clamp Current

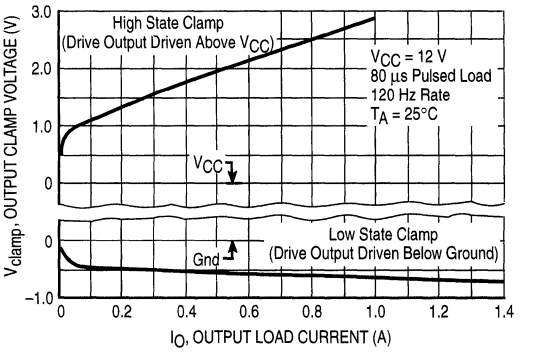


Figure 9. Drive Output Saturation Voltage versus Load Current

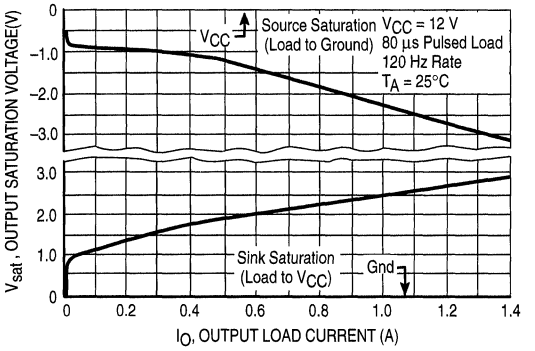


Figure 10. Drive Output Saturation Voltage versus Temperature

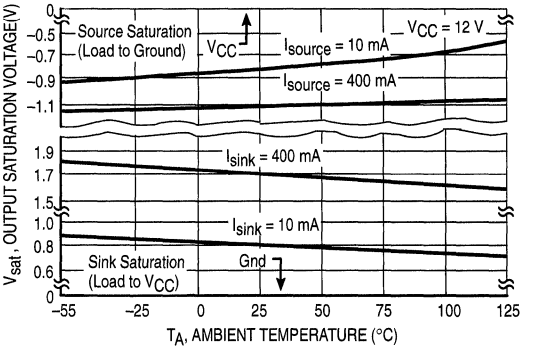


Figure 11. Drive Output Rise Time

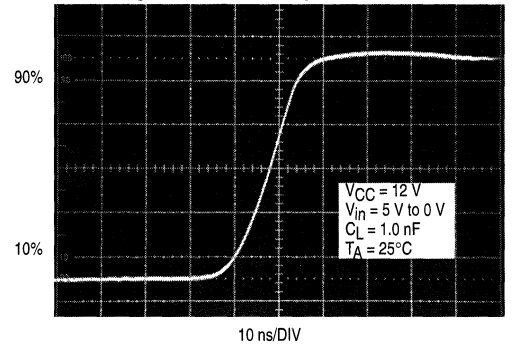


Figure 12. Drive Output Fall Time

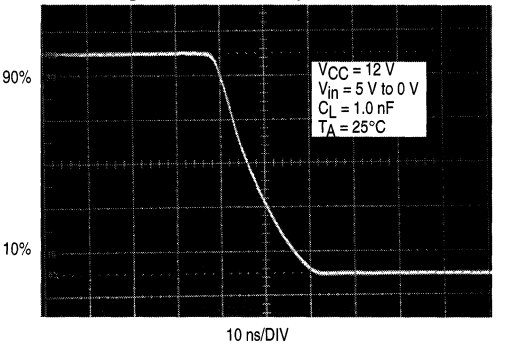


Figure 13. Drive Output Rise and Fall Time versus Load Capacitance

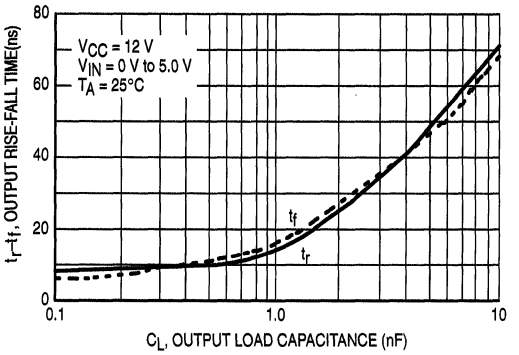


Figure 14. Supply Current versus Drive Output Load Capacitance

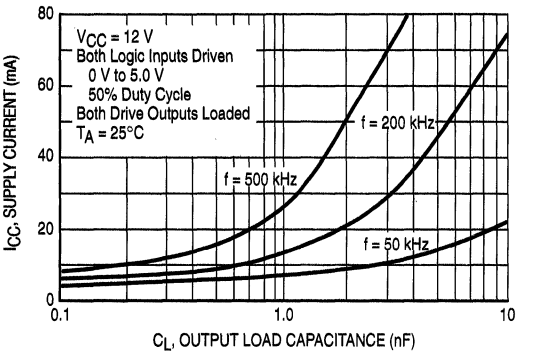


Figure 15. Supply Current versus Input Frequency

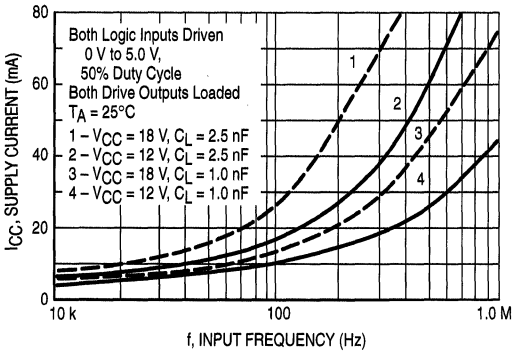
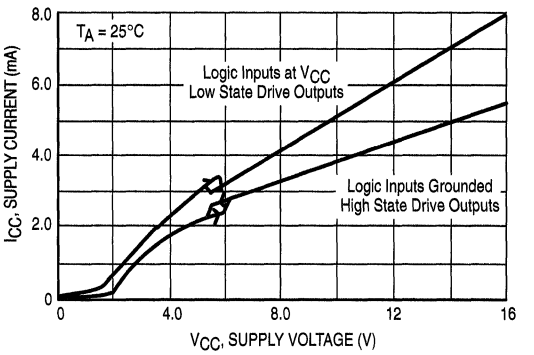


Figure 16. Supply Current versus Supply Voltage



APPLICATIONS INFORMATION

Description

The MC34151 is a dual inverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V. The input thresholds are insensitive to V_{CC} making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to V_{CC}. This allows the output of one channel to directly drive the input of a second channel for master–slave operation. Each input has a 30 kΩ pull–down resistor so that an unconnected open input will cause the associated Drive Output to be in a known high state.

Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical 'on' resistance of 2.4 Ω at 1.0 A. The low 'on' resistance allows high output currents to be attained at a lower V_{CC} than with comparative CMOS drivers. Each output has a 100 kΩ pull–down resistor to keep the MOSFET gate low when V_{CC} is less than 1.4 V. No over current or thermal protection has been designed into the device, so output shorting to V_{CC} or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above V_{CC} during the turn–on transition, and below ground during the turn–off transition. With CMOS drivers, this mode of operation can cause a destructive output latch–up condition. The MC34151 is immune to output latch–up. The Drive Outputs contain an internal diode to V_{CC} for clamping positive voltage transients. When operating with V_{CC} at 18 V, proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pull–up transistor. Since full supply voltage is applied across the NPN pull–up during the negative output transient, power dissipation at high frequencies can become excessive. Figures 19, 20, and 21 show a method of using external Schottky diode clamps to reduce driver power dissipation.

Undervoltage Lockout

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as V_{CC} rises from 1.4 V to

the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V, yielding about 500 mV of hysteresis.

Power Dissipation

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D (R_{\theta JA})$$

where: T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
$R_{\theta JA}$ = Thermal Resistance Junction to Ambient

There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$$P_D = P_Q + P_C + P_T$$

where: P_Q = Quiescent Power Dissipation
P_C = Capacitive Load Power Dissipation
P_T = Transition Power Dissipation

The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 16. The device's quiescent power dissipation is:

$$P_Q = V_{CC} \left(I_{CCL} (1-D) + I_{CCH} (D) \right)$$

where: I_{CCL} = Supply Current with Low State Drive Outputs
I_{CCH} = Supply Current with High State Drive Outputs
D = Output Duty Cycle

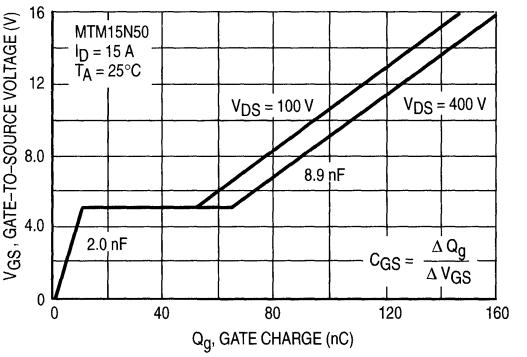
The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

$$P_C = V_{CC} (V_{OH} - V_{OL}) C_L f$$

where: V_{OH} = High State Drive Output Voltage
V_{OL} = Low State Drive Output Voltage
C_L = Load Capacitance
f = frequency

When driving a MOSFET, the calculation of capacitive load power P_C is somewhat complicated by the changing gate to source capacitance C_{GS} as the device switches. To aid in this calculation, power MOSFET manufacturers provide gate charge information on their data sheets. Figure 17 shows a curve of gate voltage versus gate charge for the Motorola MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on', the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge Q_g of 110 nC is required when operating the MOSFET with a drain to source voltage V_{DS} of 400 V.

Figure 17. Gate–To–Source Voltage versus Gate Charge



The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$$P_{C(MOSFET)} = V_C Q_g f$$

The flat region from 10 nC to 55 nC is caused by the drain–to–gate Miller capacitance, occuring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34151 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34151 at a higher V_{CC}, additional charge can be provided to bring the gate above 10 V. This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$$P_T \approx V_{CC} (1.08\ V_{CC}\ C_L\ f - 8 \times 10^{-4})$$

P_T must be greater than zero.

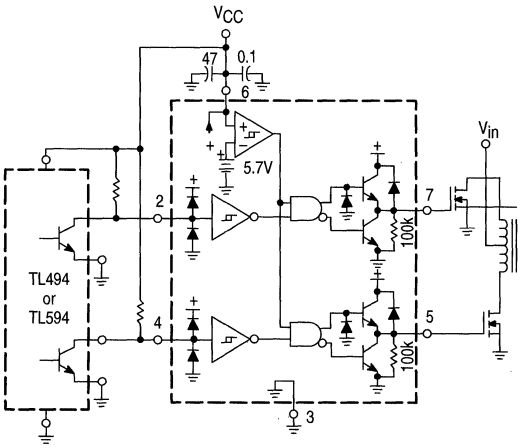
Switching time characterization of the MC34151 is performed with fixed capacitive loads. Figure 13 shows that for small capacitance loads, the switching speed is limited by transistor turn–on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

LAYOUT CONSIDERATIONS

High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. **Do not attempt to construct the driver circuit on wire–wrap or plug–in prototype boards.** When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For optimum drive performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the V_{CC} pin and ground as the layout will permit. Suggested capacitors are a low inductance 0.1 μF ceramic in parallel with a 4.7 μF tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

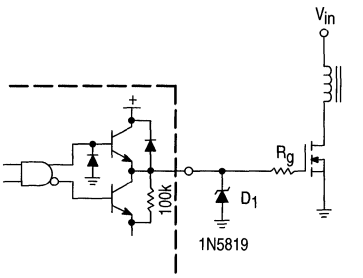
Proper printed circuit board layout is extremely critical and cannot be over emphasized.

Figure 18. Enhanced System Performance with Common Switching Regulators



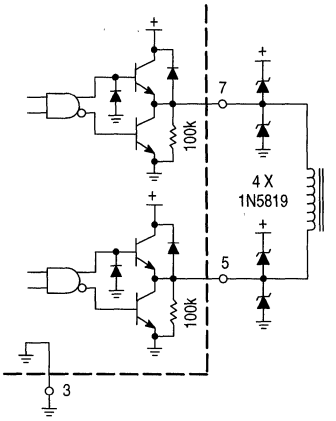
The MC34151 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

Figure 19. MOSFET Parasitic Oscillations



Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 20. Direct Transformer Drive



Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above V_{CC} and below ground.

Figure 21. Isolated MOSFET Drive

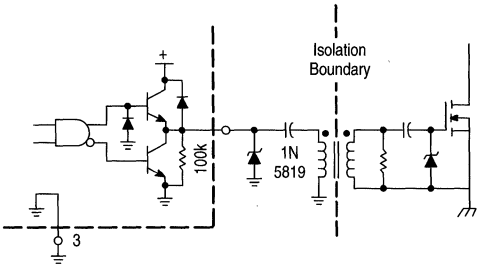
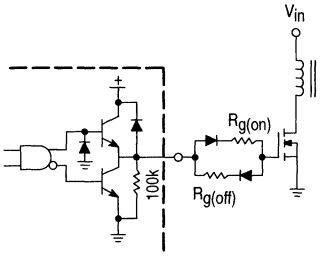
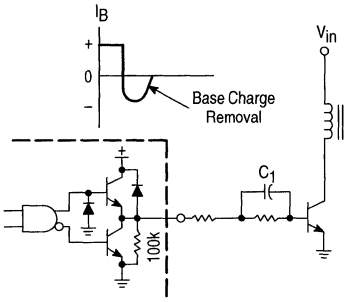


Figure 22. Controlled MOSFET Drive



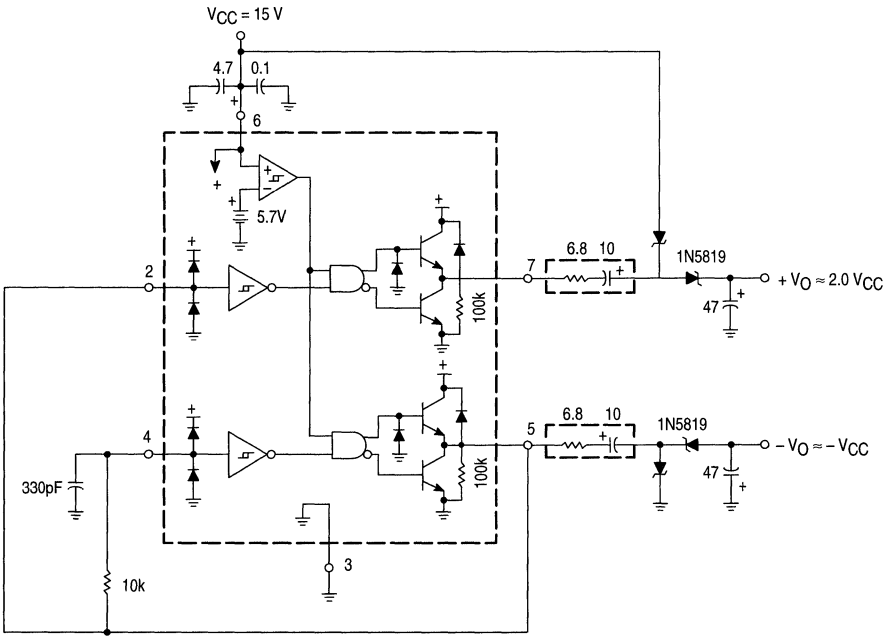
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn–on and turn–off times.

Figure 23. Bipolar Transistor Drive



The totem–pole outputs can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 24. Dual Charge Pump Converter



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	27.7	–13.3
1.0	27.4	–12.9
10	26.4	–11.9
20	25.5	–11.2
30	24.6	–10.5
50	22.6	–9.4

MOTOROLA

High Speed Dual MOSFET Drivers

MC34152
MC33152

3

The MC34152/MC33152 are dual noninverting high speed drivers specifically designed for applications that require low current digital signals to drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS/LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent system erratic operation at low supply voltages.

Typical applications include switching power supplies, dc–to–dc converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

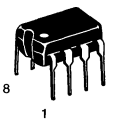
This device is available in dual–in–line and surface mount packages.

- Two Independent Channels with 1.5 A Totem Pole Outputs
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs

HIGH SPEED DUAL MOSFET DRIVERS

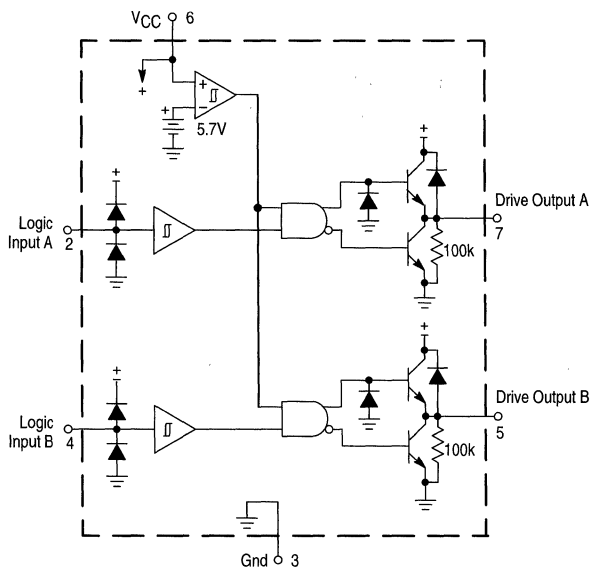
SEMICONDUCTOR TECHNICAL DATA

P SUFFIX
PLASTIC PACKAGE
CASE 626

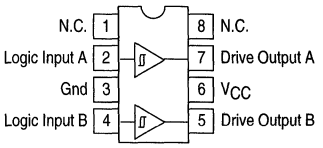


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Representative Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34152D	T_A = 0° to +70°C	SO–8
MC34152P		Plastic DIP
MC33152D	T_A = −40° to +85°C	SO–8
MC33152P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Logic Inputs (Note 1)	V_{in}	–0.3 to +V_{CC}	V
Drive Outputs (Note 2)			A
Totem Pole Sink or Source Current	I_O	1.5	
Diode Clamp Current (Drive Output to V_{CC})	$I_{O(clamp)}$	1.0	
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package Case 751			
Maximum Power Dissipation @ T_A = 50°C	P_D	0.56	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	180	°C/W
P Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 50°C	P_D	1.0	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34152 MC33152	T_A	0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics		Symbol	Min	Typ	Max	Unit
LOGIC INPUTS						
Input Threshold Voltage						V
High State Logic 1		V_{IH}	2.6	1.75	–	
Low State Logic 0		V_{IL}	–	1.58	0.9	
Input Current						μA
High State (V_{IH} = 2.6 V)		I_{IH}	–	100	300	
Low State (V_{IL} = 0.8 V)		I_{IL}	–	20	100	
DRIVE OUTPUT						
Output Voltage						V
Low State (I_{sink} = 10 mA)		V_{OL}	–	0.8	1.2	
(I_{sink} = 50 mA)			–	1.1	1.5	
(I_{sink} = 400 mA)			–	1.8	2.5	
High State (I_{source} = 10 mA)		V_{OH}	10.5	11.2	–	
(I_{source} = 50 mA)			10.4	11.1	–	
(I_{source} = 400 mA)			10	10.8	–	
Output Pull–Down Resistor		R_{PD}	–	100	–	kΩ
SWITCHING CHARACTERISTICS (T_A = 25°C)						
Propagation Delay (C_L = 1.0 nF)						ns
Logic Input to:						
Drive Output Rise (10% Input to 10% Output)		t_{PLH} (IN/OUT)	–	55	120	
Drive Output Fall (90% Input to 90% Output)		t_{PHL} (IN/OUT)	–	40	120	
Drive Output Rise Time (10% to 90%)	C_L = 1.0 nF	t_r	–	14	30	ns
	C_L = 2.5 nF		–	36	–	
Drive Output Fall Time (90% to 10%)	C_L = 1.0 nF	t_f	–	15	30	ns
	C_L = 2.5 nF		–	32	–	
TOTAL DEVICE						
Power Supply Current		I_{CC}				mA
Standby (Logic Inputs Grounded)			–	6.0	8.0	
Operating (C_L = 1.0 nF Drive Outputs 1 and 2, f = 100 kHz)			–	10.5	15	
Operating Voltage		V_{CC}	6.5	–	18	V

NOTES: 1. For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC}, whichever is less.
2. Maximum package power dissipation limits must be observed.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34152 T_{high} = +70°C for MC34152
= –40°C for MC33152 = +85°C for MC33152

3

Figure 1. Switching Characteristics Test Circuit

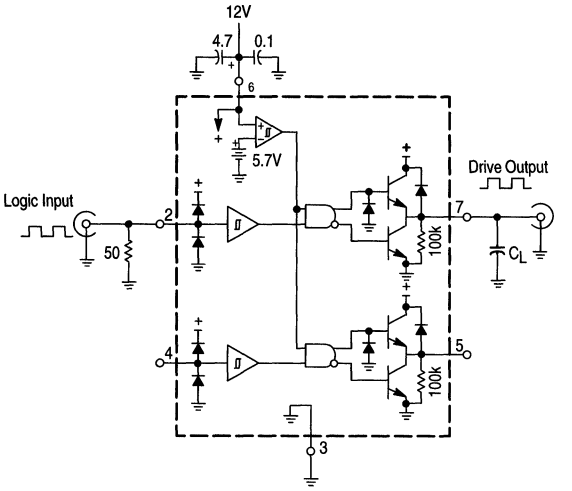


Figure 2. Switching Waveform Definitions

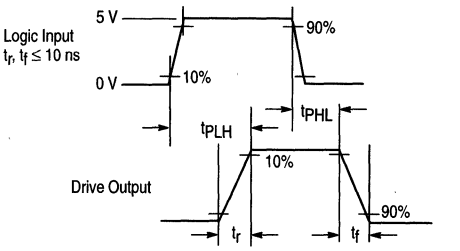


Figure 3. Logic Input Current versus Input Voltage

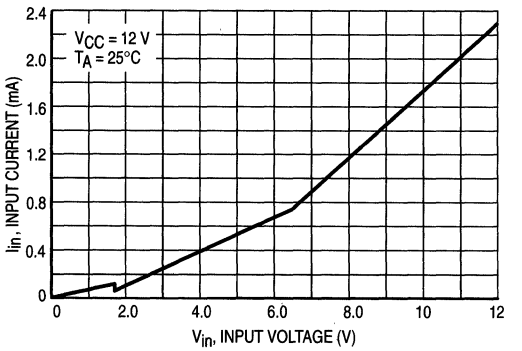


Figure 4. Logic Input Threshold Voltage versus Temperature

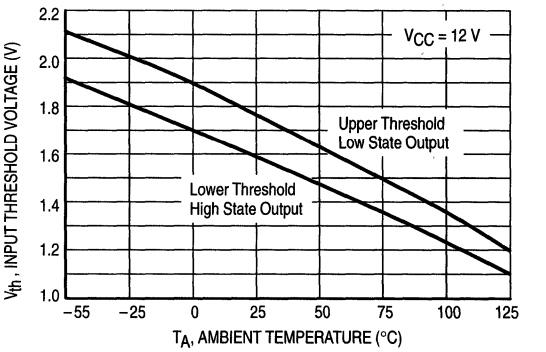


Figure 5. Drive Output High to Low Propagation Delay versus Logic Input Overdrive Voltage

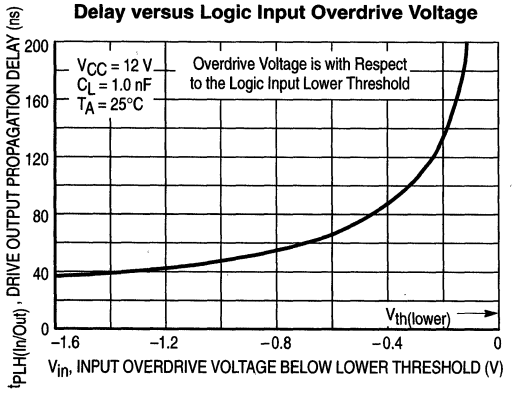


Figure 6. Drive Output Low to High Propagation Delay versus Logic Input Overdrive Voltage

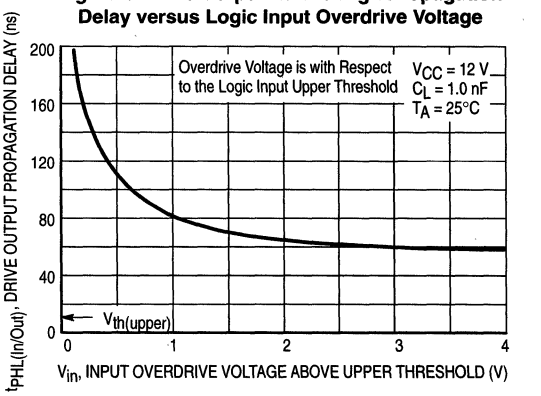


Figure 7. Propagation Delay

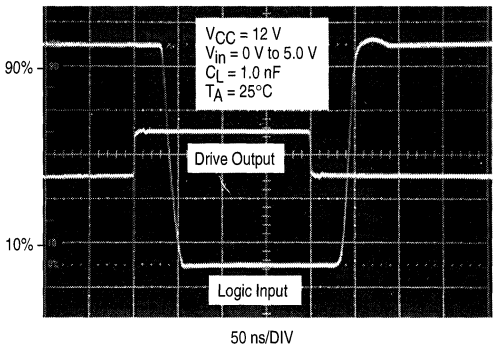


Figure 8. Drive Output Clamp Voltage versus Clamp Current

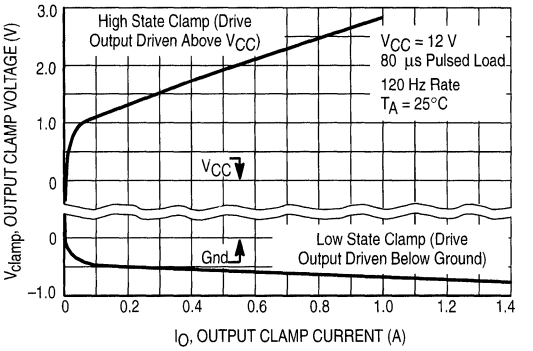


Figure 9. Drive Output Saturation Voltage versus Load Current

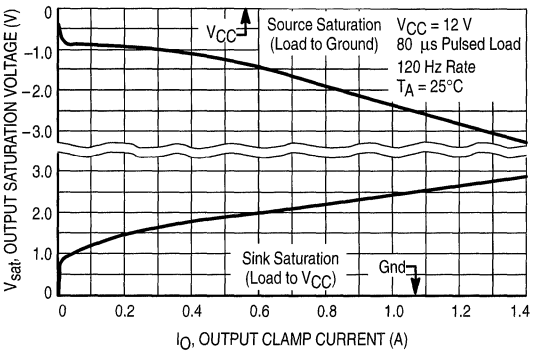


Figure 10. Drive Output Saturation Voltage versus Temperature

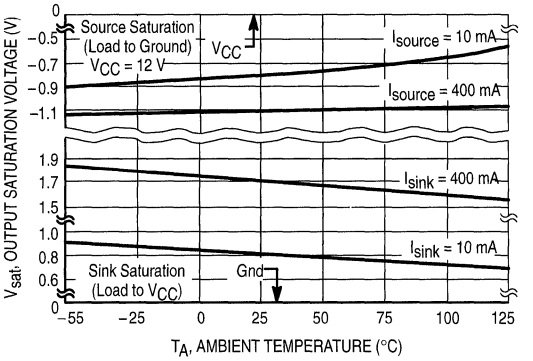


Figure 11. Drive Output Rise Time

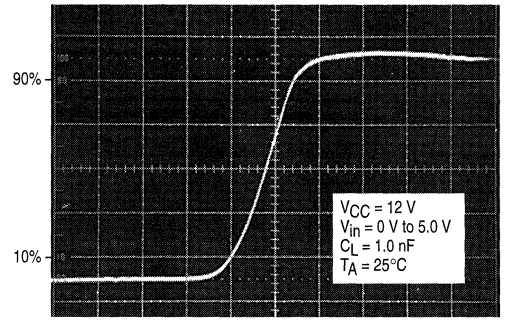


Figure 12. Drive Output Fall Time

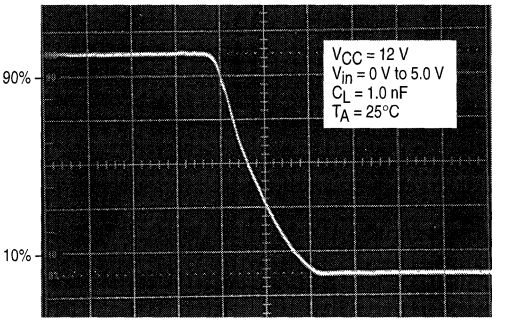


Figure 13. Drive Output Rise and Fall Time versus Load Capacitance

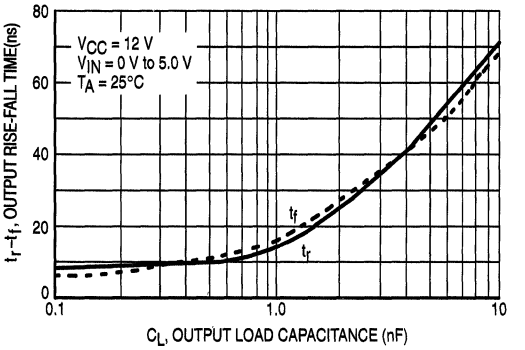


Figure 14. Supply Current versus Drive Output Load Capacitance

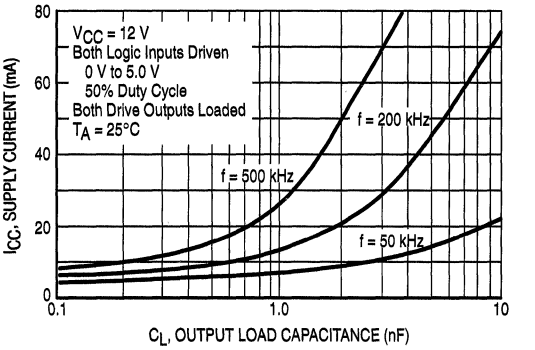


Figure 15. Supply Current versus Input Frequency

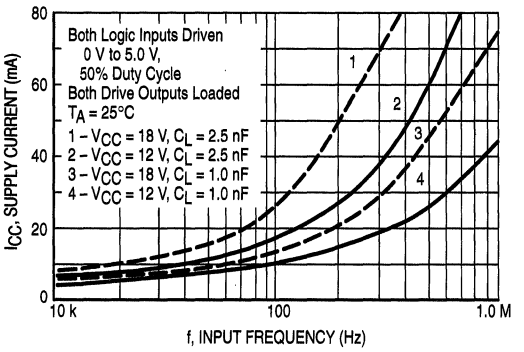
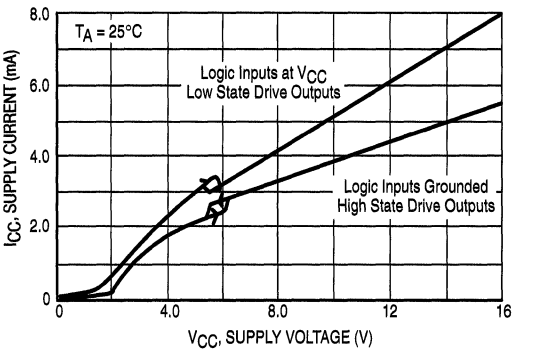


Figure 16. Supply Current versus Supply Voltage



APPLICATIONS INFORMATION

Description

The MC34152 is a dual noninverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V. The input thresholds are insensitive to V_{CC} making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to V_{CC}. This allows the output of one channel to directly drive the input of a second channel for master–slave operation. Each input has a 30 kΩ pull–down resistor so that an unconnected open input will cause the associated Drive Output to be in a known low state.

Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical 'on' resistance of 2.4 Ω at 1.0 A. The low 'on' resistance allows high output currents to be attained at a lower V_{CC} than with comparative CMOS drivers. Each output has a 100 kΩ pull–down resistor to keep the MOSFET gate low when V_{CC} is less than 1.4 V. No over current or thermal protection has been designed into the device, so output shorting to V_{CC} or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above V_{CC} during the turn–on transition, and below ground during the turn–off transition. With CMOS drivers, this mode of operation can cause a destructive output latch–up condition. The MC34152 is immune to output latch–up. The Drive Outputs contain an internal diode to V_{CC} for clamping positive voltage transients. When operating with V_{CC} at 18 V, proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pull–up transistor. Since full supply voltage is applied across the NPN pull–up during the negative output transient, power dissipation at high frequencies can become excessive. Figures 19, 20, and 21 show a method of using external Schottky diode clamps to reduce driver power dissipation.

Undervoltage Lockout

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as V_{CC} rises from 1.4 V to

the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V, yielding about 500 mV of hysteresis.

Power Dissipation

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D (R_{\theta JA})$$

where: T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
$R_{\theta JA}$ = Thermal Resistance Junction to Ambient

There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$$P_D = P_Q + P_C + P_T$$

where: P_Q = Quiescent Power Dissipation
P_C = Capacitive Load Power Dissipation
P_T = Transition Power Dissipation

The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 16. The device's quiescent power dissipation is:

$$P_Q = V_{CC} (I_{CCL} [1-D] + I_{CCH} [D])$$

where: I_{CCL} = Supply Current with Low State Drive Outputs
I_{CCH} = Supply Current with High State Drive Outputs
D = Output Duty Cycle

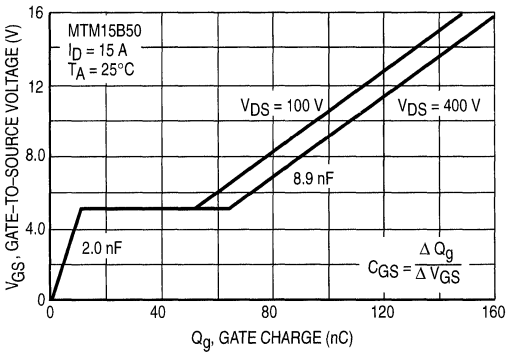
The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

$$P_C = V_{CC} (V_{OH} - V_{OL}) C_L f$$

where: V_{OH} = High State Drive Output Voltage
V_{OL} = Low State Drive Output Voltage
C_L = Load Capacitance
f = Frequency

When driving a MOSFET, the calculation of capacitive load power P_C is somewhat complicated by the changing gate to source capacitance C_{GS} as the device switches. To aid in this calculation, power MOSFET manufacturers provide gate charge information on their data sheets. Figure 17 shows a curve of gate voltage versus gate charge for the Motorola MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on,' the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge Q_g of 110 nC is required when operating the MOSFET with a drain to source voltage V_{DS} of 400 V.

Figure 17. Gate–to–Source Voltage versus Gate charge



The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$$P_{C(MOSFET)} = V_{CC} Q_g f$$

The flat region from 10 nC to 55 nC is caused by the drain–to–gate Miller capacitance, occurring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34152 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34152 at a higher V_{CC}, additional charge can be provided to bring the gate above 10 V. This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$$P_T \approx V_{CC} (1.08 V_{CC} C_L f - 8 \times 10^{-4})$$

P_T must be greater than zero.

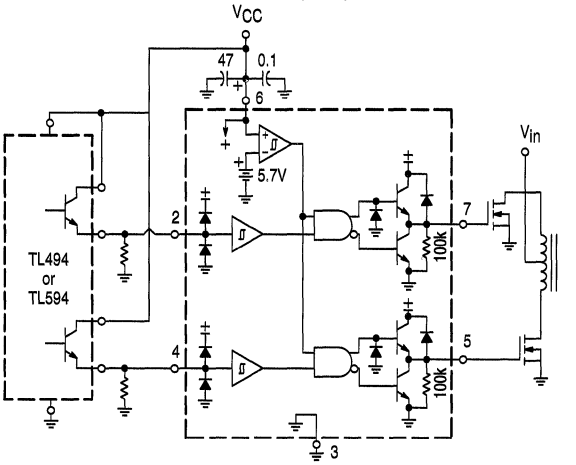
Switching time characterization of the MC34152 is performed with fixed capacitive loads. Figure 13 shows that for small capacitance loads, the switching speed is limited by transistor turn–on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

LAYOUT CONSIDERATIONS

High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. **Do not attempt to construct the driver circuit on wire–wrap or plug–in prototype boards.** When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For optimum drive performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the V_{CC} pin and ground as the layout will permit. Suggested capacitors are a low inductance 0.1 μF ceramic in parallel with a 4.7 μF tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

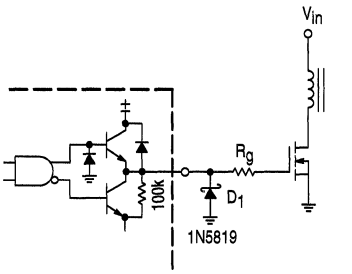
Proper printed circuit board layout is extremely critical and cannot be over emphasized.

Figure 18. Enhanced System Performance with Common Switching Regulators



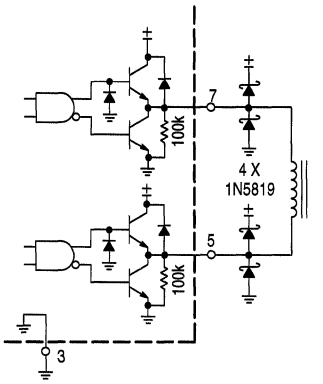
The MC34152 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

Figure 19. MOSFET Parasitic Oscillations



Series gate resistor R_G may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit. R_G will decrease the MOSFET switching speed. Schottky diode D_1 can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 20. Direct Transformer Drive



Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above V_{CC} and below ground.

Figure 21. Isolated MOSFET Drive

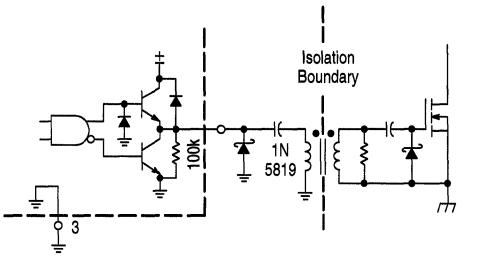
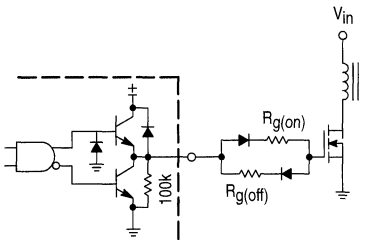
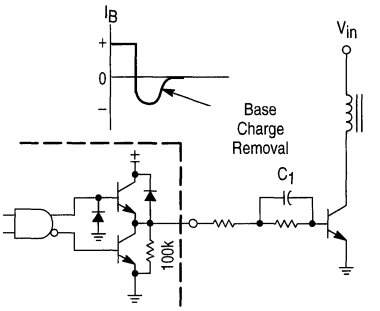


Figure 22. Controlled MOSFET Drive



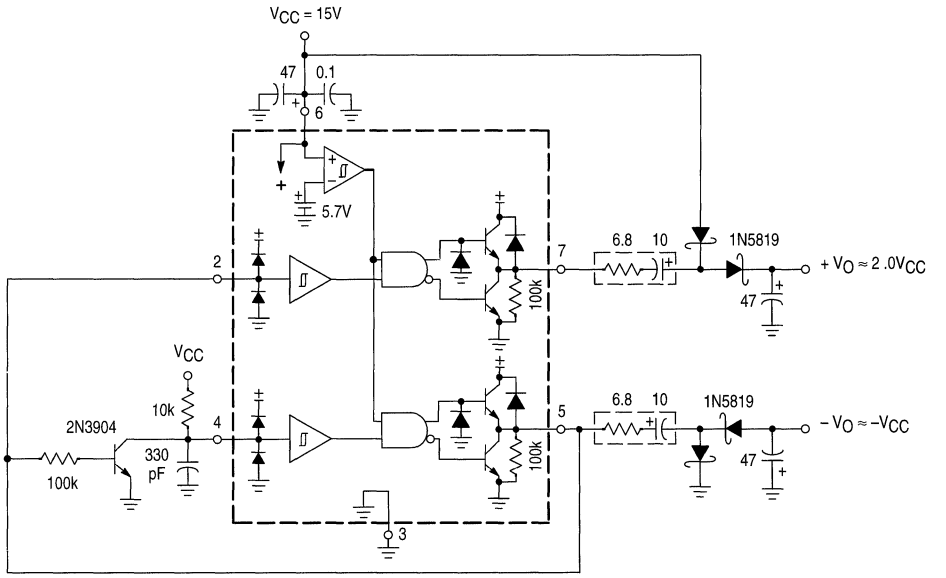
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn–on and turn–off times.

Figure 23. Bipolar Transistor Drive



The totem–pole outputs can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 24. Dual Charge Pump Converter



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	27.7	–13.3
1.0	27.4	–12.9
10	26.4	–11.9
20	25.5	–11.2
30	24.6	–10.5
50	22.6	–9.4

MOTOROLA

MC34160
MC33160

3

Microprocessor Voltage Regulator and Supervisory Circuit

The MC34160 Series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V/100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

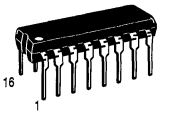
Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

These devices are contained in a 16 pin dual–in–line heat tab plastic package for improved thermal conduction.

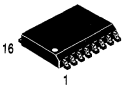
- 5.0 V Regulator Output Current in Excess of 100 mA
- Internal Short Circuit Current Limiting
- Pinned Out 2.6 V Reference
- Low Voltage Reset Comparator
- Power Warning Comparator with Programmable Hysteresis
- Uncommitted Comparator
- Low Standby Current
- Internal Thermal Shutdown Protection
- Heat Tab Power Package

MICROPROCESSOR VOLTAGE REGULATOR/ SUPERVISORY CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

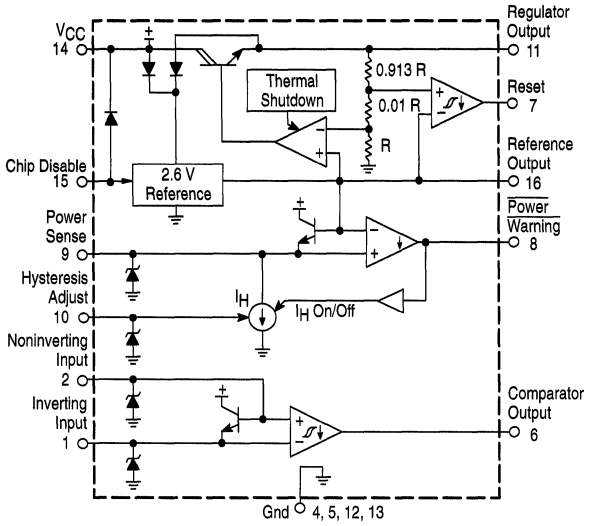


P SUFFIX
PLASTIC PACKAGE
CASE 648C
(DIP–16)



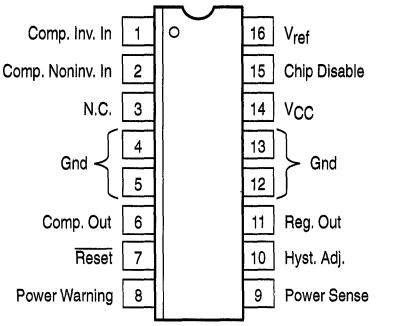
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP–16L)

Representative Block Diagram



This device contains 72 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34160DW	T_A = 0° to +70°C	SOP–16L
MC34160P		DIP–16
MC33160DW	T_A = – 40° to +85°C	SOP–16L
MC33160P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Chip Disable Input Voltage (Pin 15, Note 1)	V_{CD}	–0.3 to V_{CC}	V
Comparator Input Current (Pins 1, 2, 9)	I_{in}	–2.0 to +2.0	mA
Comparator Output Voltage (Pins 6, 7, 8)	V_O	40	V
Comparator Output Sink Current (Pins 6, 7, 8)	I_{Sink}	10	mA
Power Dissipation and Thermal Characteristics			°C/W
P Suffix, Dual–In–Line Case 648C			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	80	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	15	
DW Suffix, Surface Mount Case 751G			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	94	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	18	
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
MC34160		0 to +70	
MC33160		–40 to +85	
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 30 V, I_O = 10 mA, I_{ref} = 100 µA) For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REGULATOR SECTION					
Total Output Variation (V_{CC} = 7.0 V to 40 V, I_O = 1.0 mA to 100 mA, T_A = T_{low} to T_{high})	V_O	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Reg_{line}	–	5.0	40	mV
Load Regulation (I_O = 1.0 V to 100 mA, T_A = 25°C)	Reg_{load}	–	20	50	mV
Ripple Rejection (V_{CC} = 25 V to 35 V, I_O = 40 mA, f = 120 Hz, T_A = 25°C)	RR	50	6.5	–	dB
REFERENCE SECTION					
Total Output Variation (V_{CC} = 7.0 to 40 V, I_O = 0.1 mA to 2.0 mA, T_A = T_{low} to T_{high})	V_{ref}	2.47	2.6	2.73	V
Line Regulation (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	Reg_{line}	–	2.0	20	mV
Load Regulation (I_O = 0.1 mA to 2.0 mA, T_A = 25°C)	Reg_{load}	–	4.0	30	mV
RESET COMPARATOR					
Threshold Voltage					V
High State Output (Pin 11 Increasing)	V_{IH}	–	(V_O–0.11)	(V_O–0.05)	
Low State Output (Pin 11 Decreasing)	V_{IL}	4.55	(V_O–0.18)	–	
Hysteresis	V_H	0.02	0.07	–	
Output Sink Saturation (V_{CC} = 4.5 V, I_{Sink} = 2.0 mA)	V_{OL}	–	–	0.4	V
Output Off–State Leakage (V_{OH} = 40 V)	I_{OH}	–	–	4.0	µA

NOTES: 1. The maximum voltage range is –0.3 V to V_{CC} or +35 V, whichever is less.
2. T_{low} = 0°C for MC34160, –40°C for MC33160; T_{high} = 70°C for MC34160, 85°C for MC33160
3. Low duty cycle pulse testing techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 30 V, I_O = 10 mA, I_{ref} = 100 µA) For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER WARNING COMPARATOR					
Input Offset Voltage	V_{IO}	–	1.2	10	mV
Input Bias Current ($V_{Pin\ 9}$ = 3.0 V)	I_{IB}	–	–	0.5	µA
Input Hysteresis Current ($V_{Pin\ 9} = V_{ref} - 100$ mV) $R_{Pin\ 10}$ = 24 k $R_{Pin\ 10} = \infty$	I_H	 40 4.5	 50 7.5	 60 11	µA
Output Sink Saturation (I_{Sink} = 2.0 mA)	V_{OL}	–	0.13	0.4	V
Output Off–State Leakage (V_{OH} = 40 V)	I_{OH}	–	–	4.0	µA
UNCOMMITTED COMPARATOR					
Input Offset Voltage (Output Transition Low to High)	V_{IO}	–	–	20	mV
Input Hysteresis Voltage (Output Transition High to Low)	I_H	140	200	260	mV
Input Bias Current ($V_{Pin\ 1, 2}$ = 2.6 V)	I_{IB}	–	–	–1.0	µA
Input Common Mode Voltage Range	V_{ICR}	0.6 to 5.0	–	–	V
Output Sink Saturation (I_{Sink} = 2.0 mA)	V_{OL}	–	0.13	0.4	V
Output Off–State Leakage (V_{OH} = 40 V)	I_{OH}	–	–	4.0	µA
TOTAL DEVICE					
Chip Disable Threshold Voltage (Pin 15) High State (Chip Disabled) Low State (Chip Enabled)	 V_{IH} V_{IL}	 2.5 –	 – –	 – 0.8	V
Chip Disable Input Current (Pin 15) High State (V_{in} = 2.5 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 – –	 – –	 100 30	µA
Chip Disable Input Resistance (Pin 15)	R_{in}	50	100	–	kΩ
Operating Voltage Range V_O (Pin 11) Regulated V_{ref} (Pin 16) Regulated	V_{CC}	 7.0 to 40 5.0 to 40	 – –	 – –	V
Power Supply Current Standby (Chip Disable High State) Operating (Chip Disable Low State)	I_{CC}	 – –	 0.18 1.5	 0.35 3.0	mA

NOTES: 1. The maximum voltage range is –0.3 V to V_{CC} or +35 V, whichever is less.
2. T_{low} = 0°C for MC34160, –40°C for MC33160; T_{high} = 70°C for MC34160, 85°C for MC33160
3. Low duty cycle pulse testing techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Regulator Output Voltage Change versus Source Current

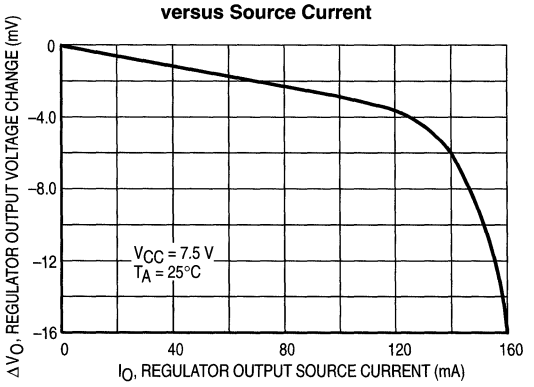


Figure 2. Reference and Regulator Output versus Supply Voltage

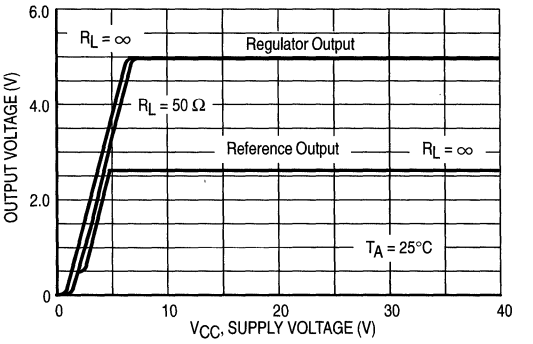


Figure 3. Reference Output Voltage Change versus Source Current

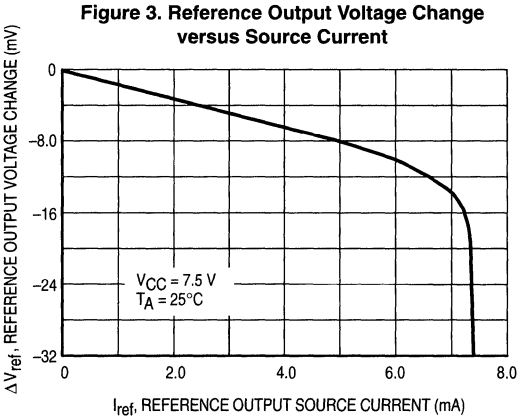


Figure 4. Power Warning Hysteresis Current versus Programming Resistor

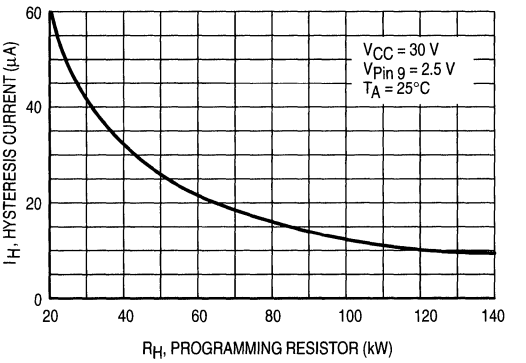


Figure 5. Power Warning Comparator Delay versus Temperature

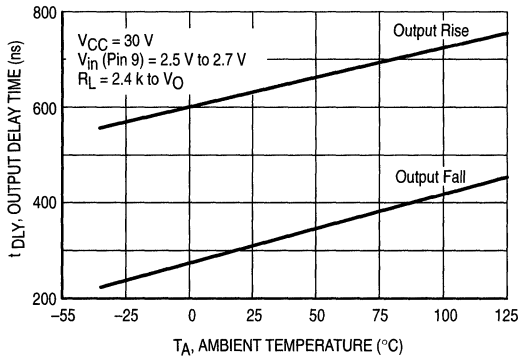


Figure 6. Uncommitted Comparator Delay versus Temperature

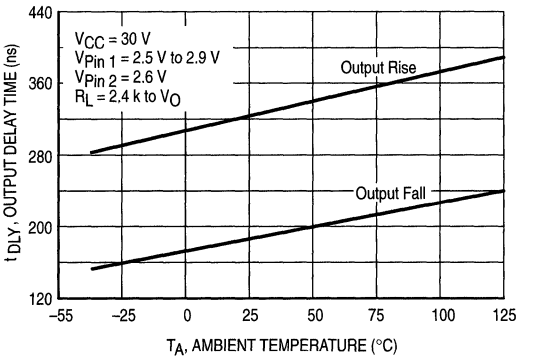


Figure 7. Comparator Output Saturation versus Sink Current

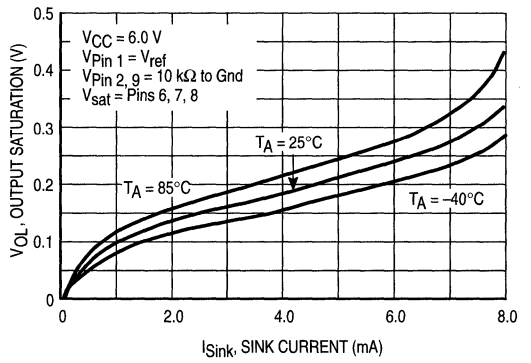
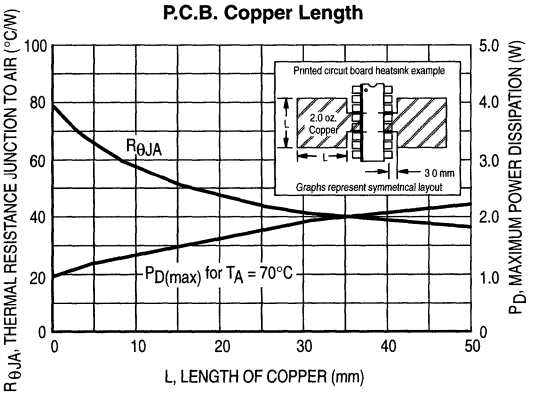
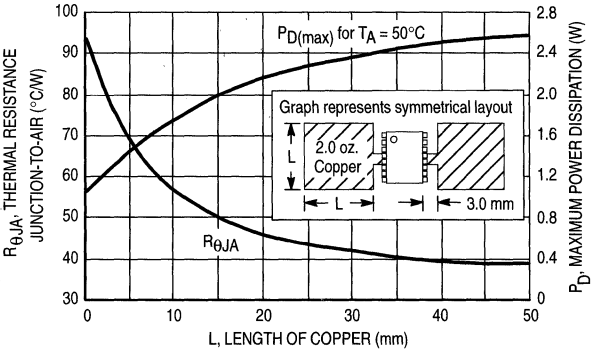


Figure 8. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



3

Figure 9. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Comparator Inverting Input	This is the Uncommitted Comparator Inverting input. It is typically connected to a resistor divider to monitor a voltage.
2	Comparator Noninverting Input	This is the Uncommitted Comparator Noninverting input. It is typically connected to a reference voltage.
3	N.C.	No connection. This pin is not internally connected.
4, 5, 12, 13	Gnd	These pins are the control circuit grounds and are connected to the source and load ground returns. They are part of the IC lead frame and can be used for heatsinking.
6	Comparator Output	This is the Uncommitted Comparator output. It is an open collector sink–only output requiring a pull–up resistor.
7	Reset	This is the Reset Comparator output. It is an open collector sink–only output requiring a pull–up resistor.
8	Power Warning	This is the Power Warning Comparator output. It is an open collector sink–only output requiring a pull–up resistor.
9	Power Sense	This is the Power Warning Comparator noninverting input. It is typically connected to a resistor divider to monitor the input power source voltage.
10	Hysteresis Adjust	The Power Warning Comparator hysteresis is programmed by a resistor connected from this pin to ground.
11	Regulator Output	This is the 5.0 V Regulator output.
14	V_{CC}	This pin is the positive supply input of the control IC.
15	Chip Disable	This input is used to switch the IC into a standby mode turning off all outputs.
16	V_{ref}	This is the 2.6 V Reference output. It is intended to be used in conjunction with the Power Warning and Uncommitted comparators.

OPERATING DESCRIPTION

The MC34160 series is a monolithic voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These devices are specified for operation over an input voltage of 7.0 V to 40 V, and with a junction temperature of –40° to +150°C. A typical microprocessor application is shown in Figure 10.

Regulator

The 5.0 V regulator is designed to source in excess of 100 mA output current and is short circuit protected. The output has a guaranteed tolerance of ±5.0% over line, load, and temperature. Internal thermal shutdown circuitry is included to limit the maximum junction temperature to a safe level. When activated, typically at 170°C, the regulator output turns off.

In specific situations a combination of input and output bypass capacitors may be required for regulator stability. If the regulator is located an appreciable distance (≥ 4″) from the supply filter, an input bypass capacitor (C_{in}) of 0.33 μF or greater is suggested. Output capacitance values of less than 5.0 nF may cause regulator instability at light load (≤ 1.0 mA) and cold temperature. An output bypass capacitor of 0.1 μF or greater is recommended to ensure stability under all load conditions. The capacitors selected must provide good high frequency characteristics.

Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator does not have external sense inputs.

Reference

The 2.6 V bandgap reference is short circuit protected and has a guaranteed output tolerance of ±5.0% over line, load, and temperature. It is intended to be used in conjunction with the Power Warning and Uncommitted comparator. The reference can source in excess of 2.0 mA and sink a maximum of 10 μA. For additional current sinking capability, an external load resistor to ground must be used.

Reference biasing is internally derived from either V_{CC} or V_O, allowing proper operation if either drops below nominal.

Chip Disable

This input is used to switch the IC into a standby mode. When activated, internal biasing for the entire die is removed causing all outputs to turn off. This reduces the power supply current (I_{CC}) to less than 0.3 mA.

Comparators

Three separate comparators are incorporated for voltage monitoring. Their outputs can provide diagnostic information to the microprocessor, preventing system malfunctions.

The Reset Comparator Inverting Input is internally connected to the 2.6 V reference while the Noninverting Input monitors V_O. The $\overline{\text{Reset}}$ Output is active low when V_O falls approximately 180 mV below its regulated voltage. To prevent erratic operation when crossing the comparator threshold, 70 mV of hysteresis is provided.

The Power Warning Comparator is typically used to detect an impending loss of system power. The Inverting Input is internally connected to the reference, fixing the threshold at 2.6 V. The input power source V_{in} is monitored by the Noninverting Input through the R_1/R_2 divider (Figure 10). This input features an adjustable 10 μA to 50 μA current sink I_H that is programmed by the value selected for resistor R_H. A default current of 6.5 μA is provided if R_H is omitted. When the comparator input falls below 2.6 V, the current sink is activated. This produces hysteresis if V_{in} is monitored through a series resistor (R_1). The comparator thresholds are defined as follows:

$$V_{th(lower)} = V_{ref}\left(1 + \frac{R1}{R2}\right) - I_{IB}\,R_1$$

$$V_{th(upper)} = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_H\,R_1$$

The nominal hysteresis current I_H equals 1.2 V/R_H (Figure 4).

The Uncommitted Comparator can be used to synchronize the microprocessor with the ac line signal for timing functions, or for synchronous load switching. It can also be connected as a line loss detector as shown in Figure 11. The comparator contains 200 mV of hysteresis preventing erractic output behavior when crossing the input threshold.

The Power Warning and Uncommitted Comparators each have a transistor base–emitter connected across their inputs. The base input normally connects to a voltage reference while the emitter input connects to the voltage to be monitored. The transistor limits the negative excursion on the emitter input to – 0.7 V below the base input by supply current from V_{CC}. This clamp current will prevent forward biasing the IC substrate. Zener diodes are connected to the comparator inputs to enhance the ICs electrostatic discharge capability. Resistors R_1 and R_{in} must limit the input current to a maximum of ±2.0 mA.

Each comparator output consists of an open collector NPN transistor capable of sinking 2.0 mA with a saturation voltage less than 0.4 V, and standing off 40 V with minimal leakage. Internal bias for the Reset and Power Warning Comparators is derived from either V_{CC} or the regulator output to ensure functionality when either is below nominal.

Heat Tab Package

The MC34160 is contained in a 16 lead plastic dual–in–line package in which the die is mounted on a special Heat Tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the surrounding air. The pictorial in Figure 8 shows a simple but effective method of utilizing the printed circuit board medium as a heat dissipator by soldering these tabs to an adequate area of copper foil. This permits the use of standard board layout and mounting practices while having the ability to more than halve the junction to air thermal resistance. The example and graph are for a symmetrical layout on a single sided board with one ounce per square foot copper.

Figure 10. Typical Microprocessor Application

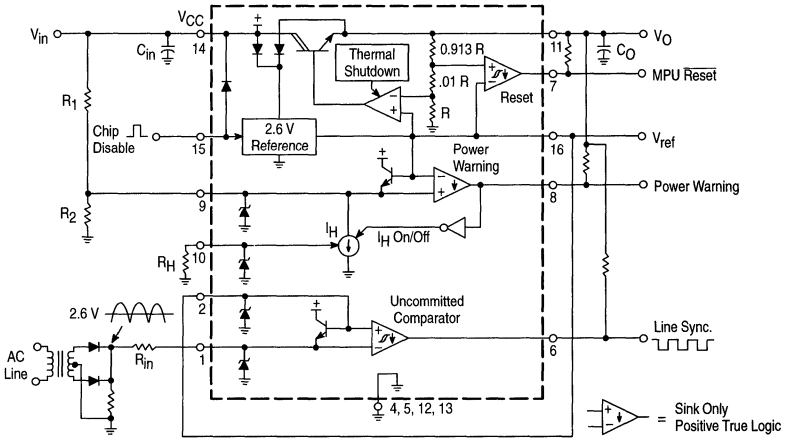


Figure 11. Line Loss Detector Application

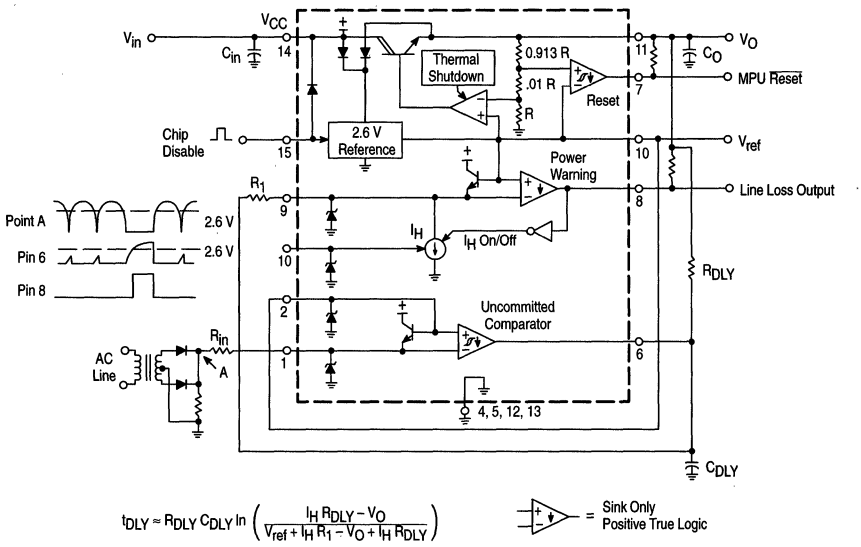
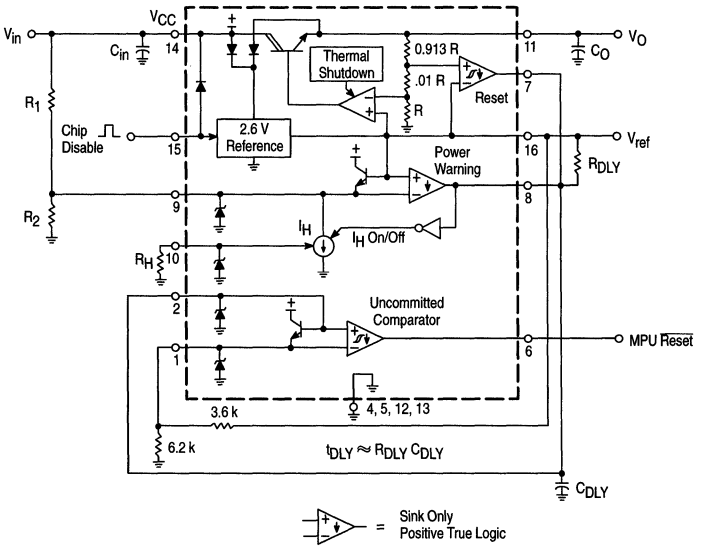


Figure 12. Time Delayed Microprocessor Reset



MOTOROLA

MC34161
MC33161

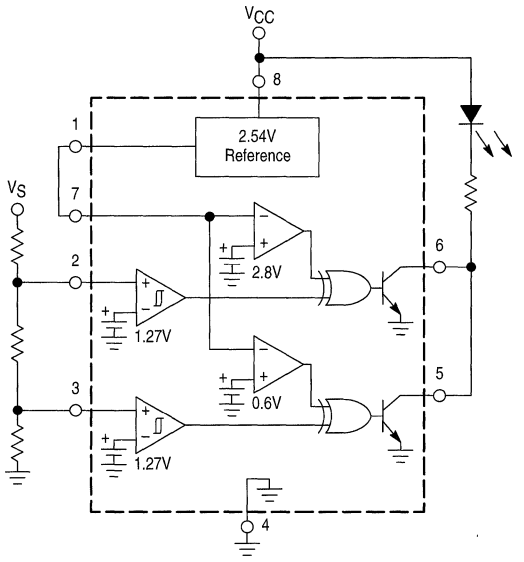
Universal Voltage Monitors

The MC34161/MC33161 are universal voltage monitors intended for use in a wide variety of voltage sensing applications. These devices offer the circuit designer an economical solution for positive and negative voltage detection. The circuit consists of two comparator channels each with hysteresis, a unique Mode Select Input for channel programming, a pinned out 2.54 V reference, and two open collector outputs capable of sinking in excess of 10 mA. Each comparator channel can be configured as either inverting or noninverting by the Mode Select Input. This allows over, under, and window detection of positive and negative voltages. The minimum supply voltage needed for these devices to be fully functional is 2.0 V for positive voltage sensing and 4.0 V for negative voltage sensing.

Applications include direct monitoring of positive and negative voltages used in appliance, automotive, consumer, and industrial equipment.

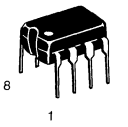
- Unique Mode Select Input Allows Channel Programming
- Over, Under, and Window Voltage Detection
- Positive and Negative Voltage Detection
- Fully Functional at 2.0 V for Positve Voltage Sensing and 4.0 V for Negative Voltage Sensing
- Pinned Out 2.54 V Reference with Current Limit Protection
- Low Standby Current
- Open Collector Outputs for Enhanced Device Flexibility

Simplified Block Diagram
(Positive Voltage Window Detector Application)



UNIVERSAL VOLTAGE MONITORS

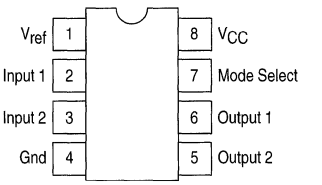
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(TOP VIEW)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34161D	T_A = 0° to +70°C	SO–8
MC34161P		Plastic DIP
MC33161D	T_A = –40° to +85°C	SO–8
MC33161P		Plastic DIP

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	40	V
Comparator Input Voltage Range	V_{in}	– 1.0 to +40	V
Comparator Output Sink Current (Pins 5 and 6) (Note 1)	I_{Sink}	20	mA
Comparator Output Voltage	V_{out}	40	V
Power Dissipation and Thermal Characteristics (Note 1) P Suffix, Plastic Package, Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air D Suffix, Plastic Package, Case 751 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 800 100 450 178	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34161 MC33161	T_A	 0 to +70 – 40 to +85	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
COMPARATOR INPUTS					
Threshold Voltage, V_{in} Increasing (T_A = 25°C) (T_A = T_{min} to T_{max})	V_{th}	1.245 1.235	1.27 –	1.295 1.295	V
Threshold Voltage Variation (V_{CC} = 2.0 V to 40 V)	ΔV_{th}	–	7.0	15	mV
Threshold Hysteresis, V_{in} Decreasing	V_H	15	25	35	mV
Threshold Difference $\lvert V_{th1} - V_{th2} \rvert$	V_D	–	1.0	15	mV
Reference to Threshold Difference ($V_{ref} - V_{in1}$), ($V_{ref} - V_{in2}$)	V_{RTD}	1.20	1.27	1.32	V
Input Bias Current (V_{in} = 1.0 V) (V_{in} = 1.5 V)	I_{IB}	– –	40 85	200 400	nA
MODE SELECT INPUT					
Mode Select Threshold Voltage (Figure 5) Channel 1 Channel 2	$V_{th(CH\ 1)}$ $V_{th(CH\ 2)}$	V_{ref}+0.15 0.3	V_{ref}+0.23 0.63	V_{ref}+0.30 0.9	V
COMPARATOR OUTPUTS					
Output Sink Saturation Voltage (I_{Sink} = 2.0 mA) (I_{Sink} = 10 mA) (I_{Sink} = 0.25 mA, V_{CC} = 1.0 V)	V_{OL}	– – –	0.05 0.22 0.02	0.3 0.6 0.2	V
Off–State Leakage Current (V_{OH} = 40 V)	I_{OH}	–	0	1.0	μA
REFERENCE OUTPUT					
Output Voltage (I_O = 0 mA, T_A = 25°C)	V_{ref}	2.48	2.54	2.60	V
Load Regulation (I_O = 0 mA to 2.0 mA)	Reg_{load}	–	0.6	15	mV
Line Regulation (V_{CC} = 4.0 V to 40 V)	Reg_{line}	–	5.0	15	mV
Total Output Variation over Line, Load, and Temperature	ΔV_{ref}	2.45	–	2.60	V
Short Circuit Current	I_{SC}	–	8.5	30	mA
TOTAL DEVICE					
Power Supply Current (V_{Mode}, V_{in1}, V_{in2} = Gnd) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	– –	450 560	700 900	μA
Operating Voltage Range (Positive Sensing) (Negative Sensing)	V_{CC}	2.0 4.0	– –	40 40	V

NOTES: 1. Maximum package power dissipation must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34161, –40°C for MC33161; T_{high} = +70°C for MC34161, +85°C for MC33161

Figure 1. Comparator Input Threshold Voltage

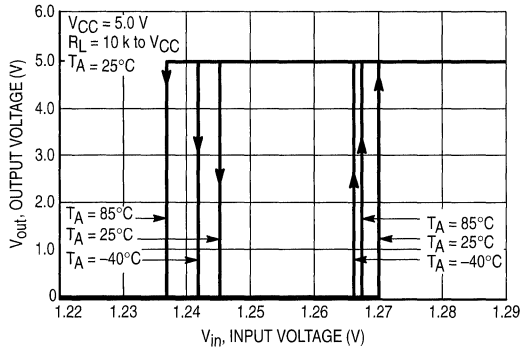


Figure 2. Comparator Input Bias Current versus Input Voltage

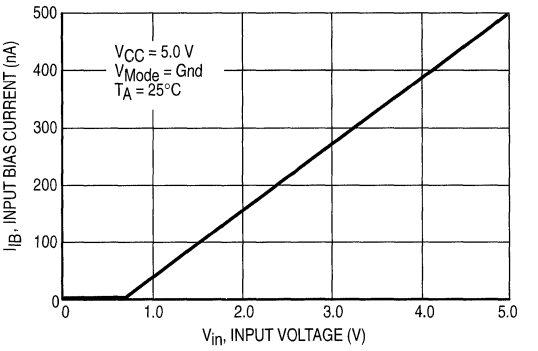


Figure 3. Output Propagation Delay Time versus Percent Overdrive

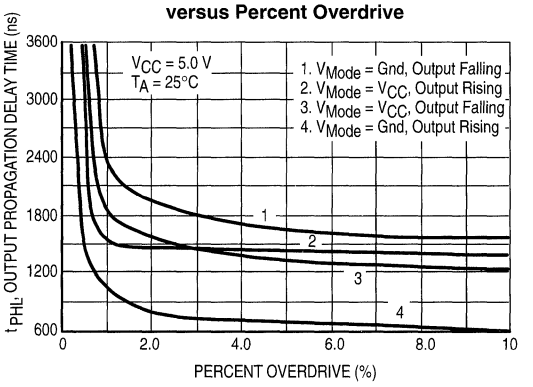


Figure 4. Output Voltage versus Supply Voltage

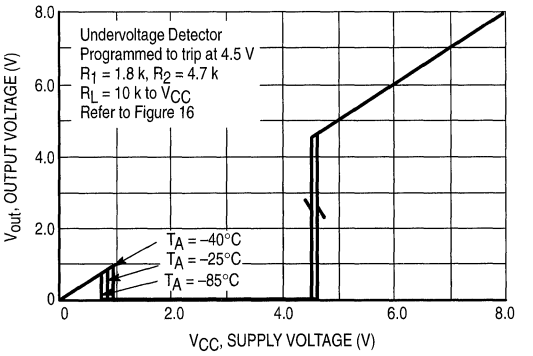


Figure 5. Mode Select Thresholds

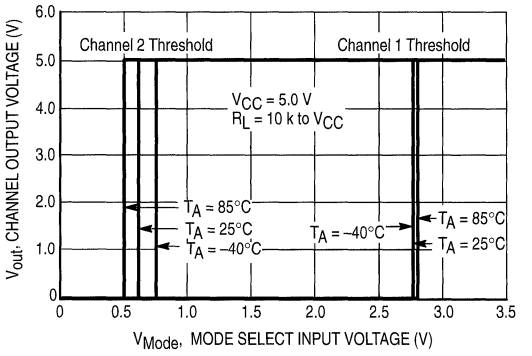


Figure 6. Mode Select Input Current versus Input Voltage

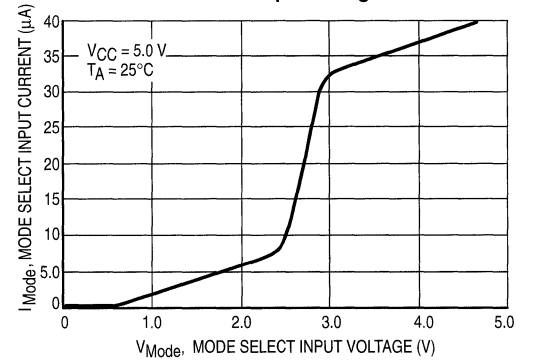


Figure 7. Reference Voltage versus Supply Voltage

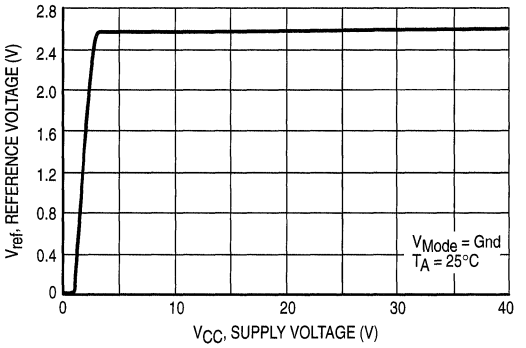


Figure 8. Reference Voltage versus Ambient Temperature

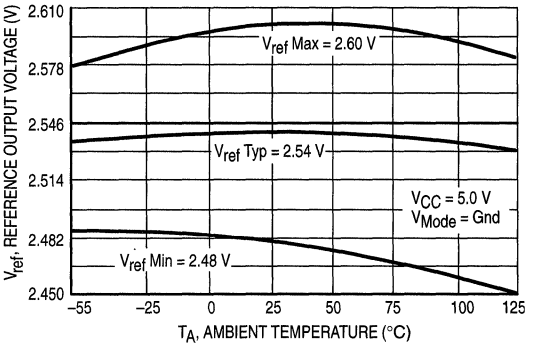


Figure 9. Reference Voltage Change versus Source Current

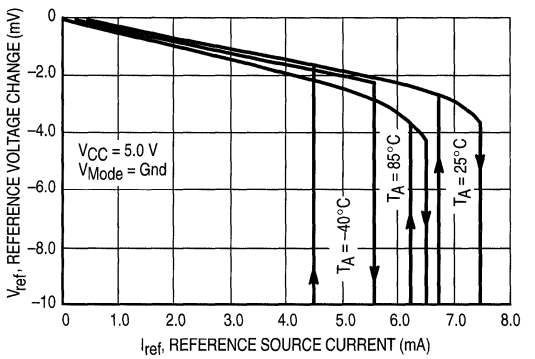


Figure 10. Output Saturation Voltage versus Output Sink Current

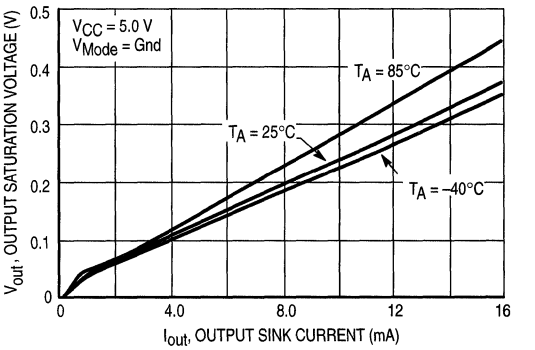


Figure 11. Supply Current versus Supply Voltage

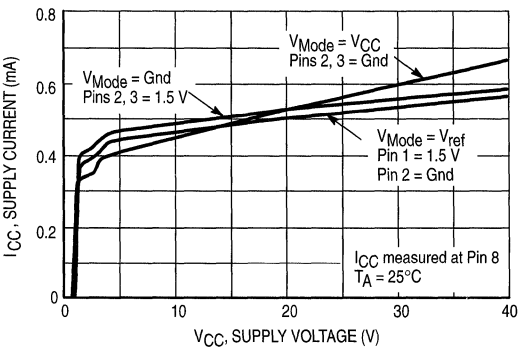


Figure 12. Supply Current versus Output Sink Current

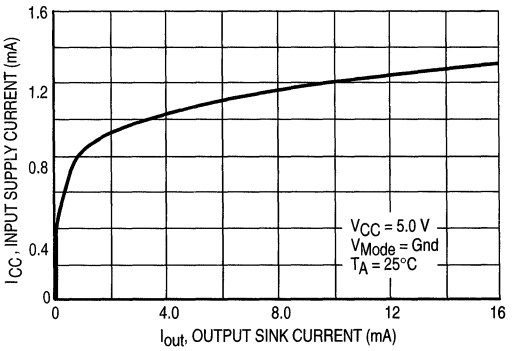


Figure 13. MC34161 Representative Block Diagram

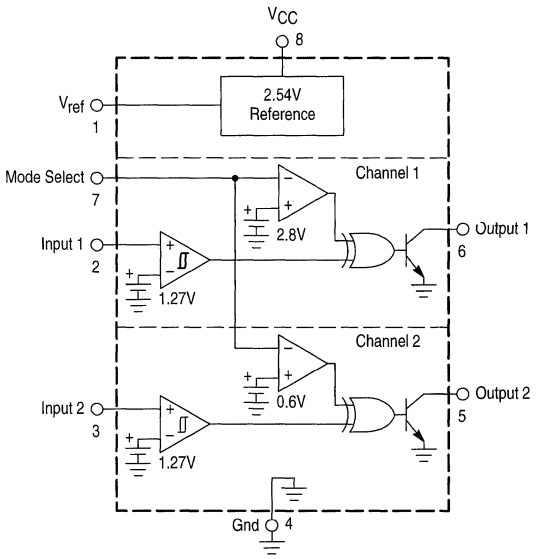


Figure 14. Truth Table

Mode Select Pin 7	Input 1 Pin 2	Output 1 Pin 6	Input 2 Pin 3	Output 2 Pin 5	Comments
GND	0 1	0 1	0 1	0 1	Channels 1 & 2: Noninverting
V_{ref}	0 1	0 1	0 1	1 0	Channel 1: Noninverting Channel 2: Inverting
V_{CC} (>2.0 V)	0 1	1 0	0 1	1 0	Channels 1 & 2: Inverting

FUNCTIONAL DESCRIPTION

Introduction

To be competitive in today's electronic equipment market, new circuits must be designed to increase system reliability with minimal incremental cost. The circuit designer can take a significant step toward attaining these goals by implementing economical circuitry that continuously monitors critical circuit voltages and provides a fault signal in the event of an out–of–tolerance condition. The MC34161, MC33161 series are universal voltage monitors intended for use in a wide variety of voltage sensing applications. The main objectives of this series was to configure a device that can be used in as many voltage sensing applications as possible while minimizing cost. The flexibility objective is achieved by the utilization of a unique Mode Select input that is used in conjunction with traditional circuit building blocks. The cost objective is achieved by processing the device on a standard Bipolar Analog flow, and by limiting the package to eight pins. The device consists of two comparator channels each with hysteresis, a mode select input for channel programming, a pinned out reference, and two open collector outputs. Each comparator channel can be configured as either inverting or noninverting by the Mode Select input. This allows a single device to perform over, under, and window detection of positive and negative voltages. A detailed description of each section of the device is given below with the representative block diagram shown in Figure 13.

Input Comparators

The input comparators of each channel are identical, each having an upper threshold voltage of 1.27 V ±2.0% with 25 mV of hysteresis. The hysteresis is provided to enhance output switching by preventing oscillations as the comparator thresholds are crossed. The comparators have an input bias current of 60 nA at their threshold which approximates a 21.2 MΩ resistor to ground. This high impedance minimizes loading of the external voltage divider for well defined trip points. For all positive voltage sensing applications, both comparator channels are fully functional at a V_{CC} of 2.0 V. In order to provide enhanced device ruggedness for hostile industrial environments, additional circuitry was designed into the inputs to prevent device latch–up as well as to suppress electrostatic discharges (ESD).

Reference

The 2.54 V reference is pinned out to provide a means for the input comparators to sense negative voltages, as well as a means to program the Mode Select input for window detection applications. The reference is capable of sourcing in excess of 2.0 mA output current and has built–in short circuit protection. The output voltage has a guaranteed tolerance of ±2.4% at room temperature.

The 2.54 V reference is derived by gaining up the internal 1.27 V reference by a factor of two. With a power supply voltage of 4.0 V, the 2.54 V reference is in full regulation, allowing the device to accurately sense negative voltages.

Mode Select Circuit

The key feature that allows this device to be flexible is the Mode Select input. This input allows the user to program each of the channels for various types of voltage sensing applications. Figure 14 shows that the Mode Select input has three defined states. These states determine whether Channel 1 and/or Channel 2 operate in the inverting or noninverting mode. The Mode Select thresholds are shown in Figure 5. The input circuitry forms a tristate switch with thresholds at 0.63 V and V_{ref} + 0.23 V. The mode select input current is 10 μA when connected to the reference output, and 42 μA when connected to a V_{CC} of 5.0 V, refer to Figure 6.

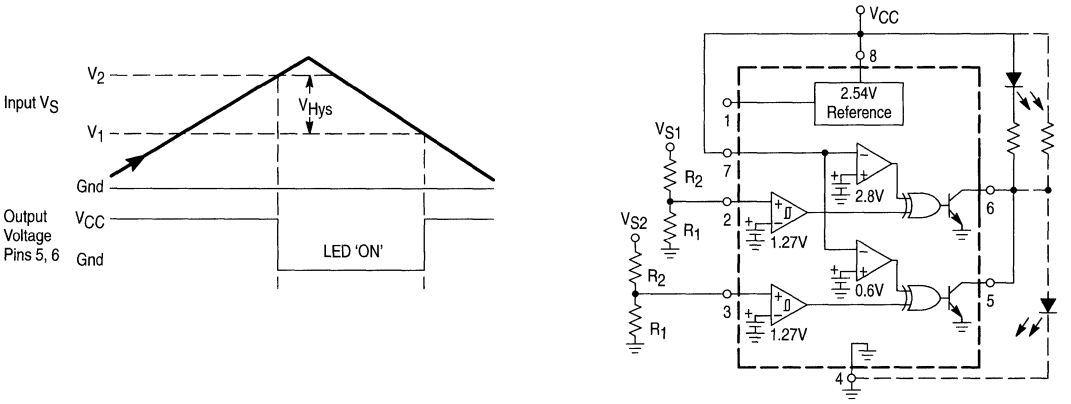
Output Stage

The output stage uses a positive feedback base boost circuit for enhanced sink saturation, while maintaining a relatively low device standby current. Figure 10 shows that the sink saturation voltage is about 0.2 V at 8.0 mA over temperature. By combining the low output saturation characteristics with low voltage comparator operation, this device is capable of sensing positive voltages at a V_{CC} of 1.0 V. These characteristics are important in undervoltage sensing applications where the output must stay in a low state as V_{CC} approaches ground. Figure 4 shows the Output Voltage versus Supply Voltage in an undervoltage sensing application. Note that as V_{CC} drops below the programmed 4.5 V trip point, the output stays in a well defined active low state until V_{CC} drops below 1.0 V.

APPLICATIONS

The following circuit figures illustrate the flexibility of this device. Included are voltage sensing applications for over, under, and window detectors, as well as three unique configurations. Many of the voltage detection circuits are shown with the open collector outputs of each channel connected together driving a light emitting diode (LED). This 'ORed' connection is shown for ease of explanation and it is only required for window detection applications. Note that many of the voltage detection circuits are shown with a dashed line output connection. This connection gives the inverse function of the solid line connection. For example, the solid line output connection of Figure 15 has the LED 'ON' when input voltage V_S is above trip voltage V_2, for overvoltage detection. The dashed line output connection has the LED 'ON' when V_S is below trip voltage V_2, for undervoltage detection.

Figure 15. Dual Postive Overvoltage Detector



The above figure shows the MC34161 configured as a dual positive overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when V_{S1} or V_{S2} exceeds V_2. With the dashed line output connection, the circuit becomes a dual positive undervoltage detector. As the input voltage decreases from the peak towards ground, the LED will turn 'ON' when V_{S1} or V_{S2} falls below V_1.

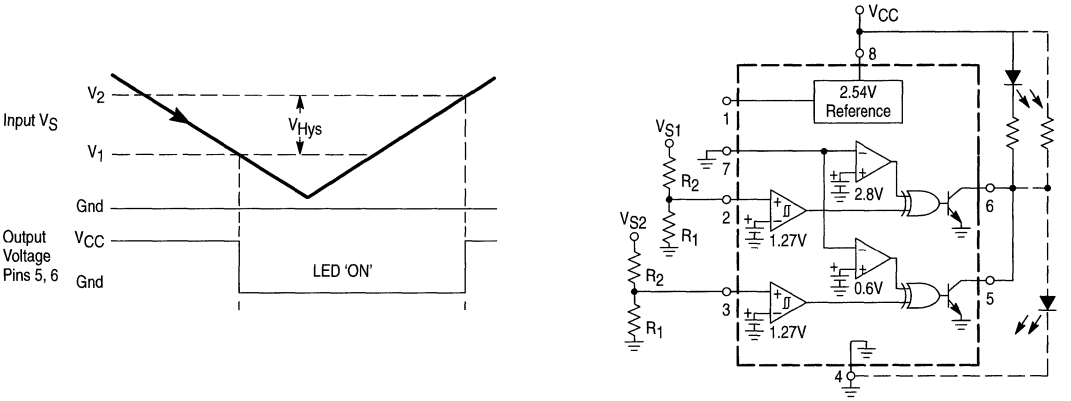
For known resistor values, the voltage trip points are:

$$V_1 = (V_{th} - V_H)\left(\frac{R_2}{R_1} + 1\right) \qquad V_2 = V_{th}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_1}{V_{th} - V_H} - 1 \qquad \frac{R_2}{R_1} = \frac{V_2}{V_{th}} - 1$$

Figure 16. Dual Postive Undervoltage Detector



The above figure shows the MC34161 configured as a dual positive undervoltage detector. As the input voltage decreases towards ground, the LED will turn 'ON' when V_{S1} or V_{S2} falls below V_1. With the dashed line output connection, the circuit becomes a dual positive overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when V_{S1} or V_{S2} exceeds V_2.

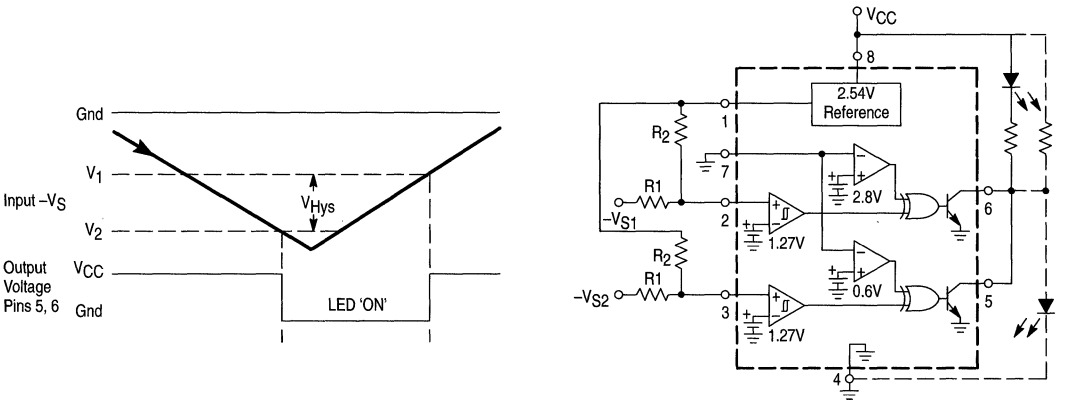
For known resistor values, the voltage trip points are:

$$V_1 = (V_{th} - V_H)\left(\frac{R_2}{R_1} + 1\right) \qquad V_2 = V_{th}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_1}{V_{th} - V_H} - 1 \qquad \frac{R_2}{R_1} = \frac{V_2}{V_{th}} - 1$$

Figure 17. Dual Negative Overvoltage Detector



The above figure shows the MC34161 configured as a dual negative overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when $-V_{S1}$ or $-V_{S2}$ exceeds V_2. With the dashed line output connection, the circuit becomes a dual negative undervoltage detector. As the input voltage decreases from the peak towards ground, the LED will turn 'ON' when $-V_{S1}$ or $-V_{S2}$ falls below V_1.

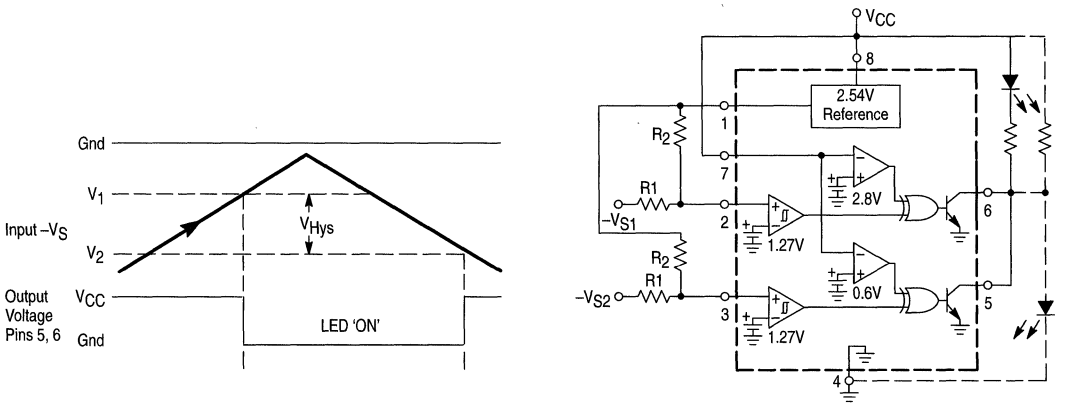
For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_1}{R_2}(V_{th} - V_{ref}) + V_{th} \qquad V_2 = \frac{R_1}{R_2}(V_{th} - V_H - V_{ref}) + V_{th} - V_H$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_1}{R_2} = \frac{V_1 - V_{th}}{V_{th} - V_{ref}} \qquad \frac{R_1}{R_2} = \frac{V_2 - V_{th} + V_H}{V_{th} - V_H - V_{ref}}$$

Figure 18. Dual Negative Undervoltage Detector



The above figure shows the MC34161 configured as a dual negative undervoltage detector. As the input voltage decreases towards ground, the LED will turn 'ON' when $-V_{S1}$ or $-V_{S2}$ falls below V_1. With the dashed line output connection, the circuit becomes a dual negative overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when $-V_{S1}$ or $-V_{S2}$ exceeds V_2.

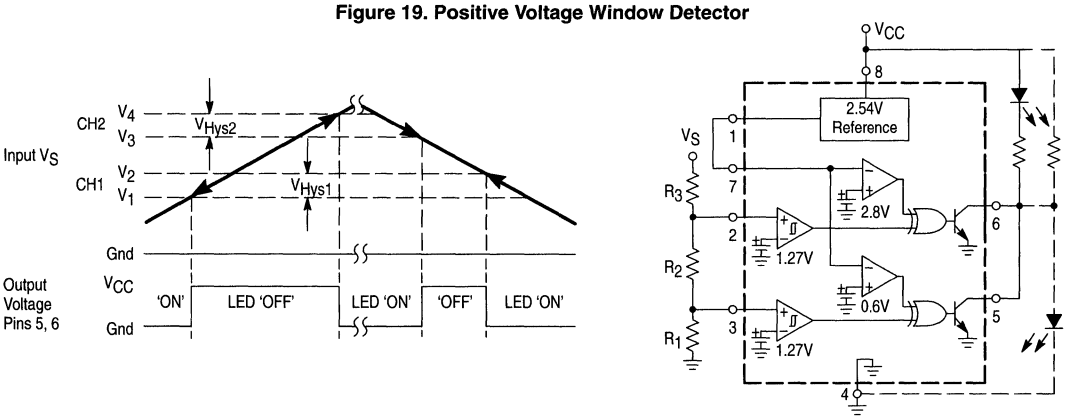
For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_1}{R_2}(V_{th} - V_{ref}) + V_{th} \qquad V_2 = \frac{R_1}{R_2}(V_{th} - V_H - V_{ref}) + V_{th} - V_H$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_1}{R_2} = \frac{V_1 - V_{th}}{V_{th} - V_{ref}} \qquad \frac{R_1}{R_2} = \frac{V_2 - V_{th} + V_H}{V_{th} - V_H - V_{ref}}$$

Figure 19. Positive Voltage Window Detector



The above figure shows the MC34161 configured as a positive voltage window detector. This is accomplished by connecting channel 1 as an undervoltage detector, and channel 2 as an overvoltage detector. When the input voltage V_S falls out of the window established by V_1 and V_4, the LED will turn 'ON'. As the input voltage falls within the window, V_S increasing from ground and exceeding V_2, or V_S decreasing from the peak towards ground and falling below V_3, the LED will turn 'OFF'. With the dashed line output connection, the LED will turn 'ON' when the input voltage V_S is within the window.

For known resistor values, the voltage trip points are:

$$V_1 = (V_{th1} - V_{H1})\left(\frac{R_3}{R_1 + R_2} + 1\right) \qquad V_3 = (V_{th2} - V_{H2})\left(\frac{R_2 + R_3}{R_1} + 1\right)$$

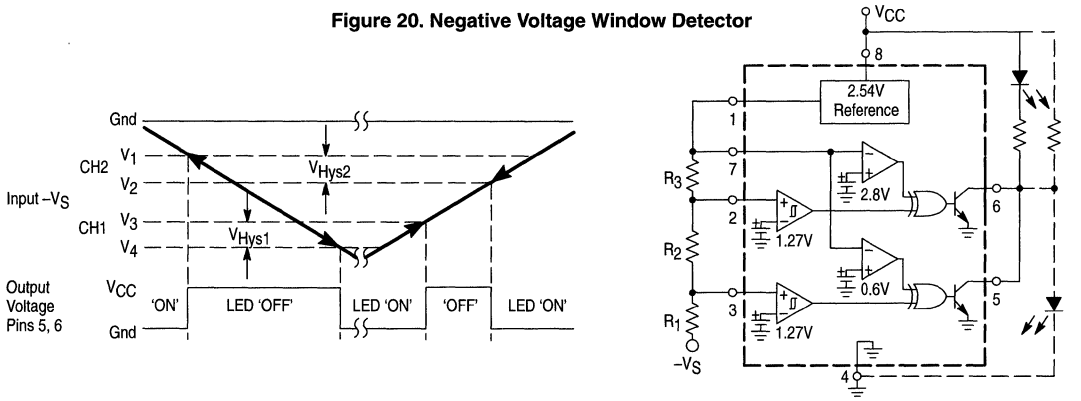
$$V_2 = V_{th1}\left(\frac{R_3}{R_1 + R_2} + 1\right) \qquad V_4 = V_{th2}\left(\frac{R_2 + R_3}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_3(V_{th2} - V_{H2})}{V_1(V_{th1} - V_{H1})} - 1 \qquad \frac{R_3}{R_1} = \frac{V_3(V_1 - V_{th1} + V_{H1})}{V_1(V_{th2} - V_{H2})}$$

$$\frac{R_2}{R_1} = \frac{V_4 \times V_{th2}}{V_2 \times V_{th1}} - 1 \qquad \frac{R_3}{R_1} = \frac{V_4(V_2 - V_{th1})}{V_2 \times V_{th2}}$$

Figure 20. Negative Voltage Window Detector



The above figure shows the MC34161 configured as a negative voltage window detector. When the input voltage $-V_S$ falls out of the window established by V_1 and V_4, the LED will turn 'ON'. As the input voltage falls within the window, $-V_S$ increasing from ground and exceeding V_2, or $-V_S$ decreasing from the peak towards ground and falling below V_3, the LED will turn 'OFF'. With the dashed line output connection, the LED will turn 'ON' when the input voltage $-V_S$ is within the window.

For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_1(V_{th2} - V_{ref})}{R_2 + R_3} + V_{th2}$$

$$V_2 = \frac{R_1(V_{th2} - V_{H2} - V_{ref})}{R_2 + R_3} + V_{th2} - V_{H2}$$

$$V_3 = \frac{(R_1 + R_2)(V_{th1} - V_{ref})}{R_3} + V_{th1}$$

$$V_4 = \frac{(R_1 + R_2)(V_{th1} - V_{H1} - V_{ref})}{R_3} + V_{th1} - V_{H1}$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_1}{R_2 + R_3} = \frac{V_1 - V_{th2}}{V_{th2} - V_{ref}}$$

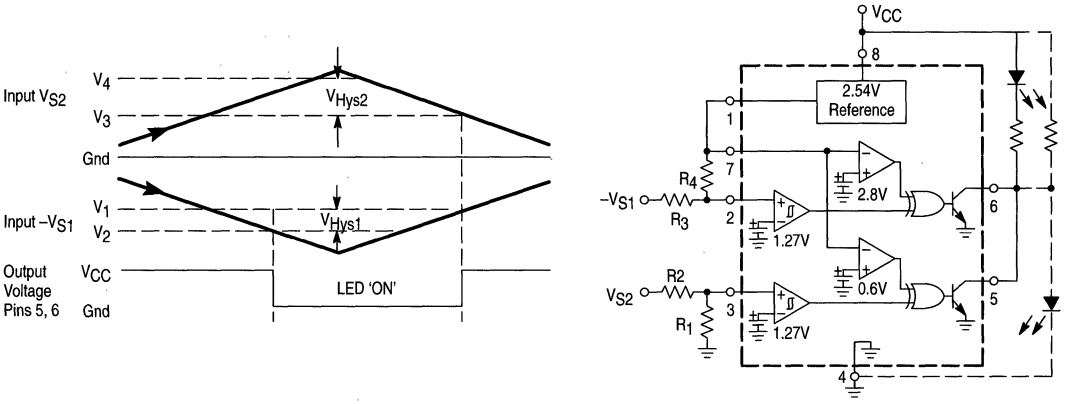
$$\frac{R_1}{R_2 + R_3} = \frac{V_2 - V_{th2} + V_{H2}}{V_{th2} - V_{H2} - V_{ref}}$$

$$\frac{R_3}{R_1 + R_2} = \frac{V_{th1} - V_{ref}}{V_3 - V_{th1}}$$

$$\frac{R_3}{R_1 + R_2} = \frac{V_{th1} - V_{H1} - V_{ref}}{V_4 + V_{H1} - V_{th1}}$$

3

Figure 21. Positive and Negative Overvoltage Detector



The above figure shows the MC34161 configured as a positive and negative overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when either $-V_{S1}$ exceeds V_2, or V_{S2} exceeds V_4. With the dashed line output connection, the circuit becomes a positive and negative undervoltage detector. As the input voltage decreases from the peak towards ground, the LED will turn 'ON' when either V_{S2} falls below V_3, or $-V_{S1}$ falls below V_1.

For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_3}{R_4}(V_{th1} - V_{ref}) + V_{th1} \qquad V_3 = (V_{th2} - V_{H2})\left(\frac{R_2}{R_1} + 1\right)$$

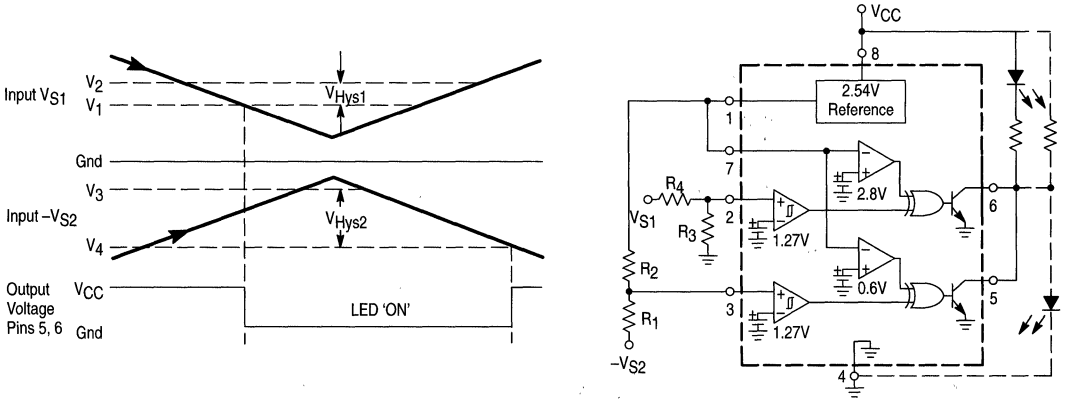
$$V_2 = \frac{R_3}{R_4}(V_{th1} - V_{H1} - V_{ref}) + V_{th1} - V_{H1} \qquad V_4 = V_{th2}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_3}{R_4} = \frac{(V_1 - V_{th1})}{(V_{th1} - V_{ref})} \qquad \frac{R_2}{R_1} = \frac{V_4}{V_{th2}} - 1$$

$$\frac{R_3}{R_4} = \frac{(V_2 - V_{th1} + V_{H1})}{(V_{th1} - V_{H1} - V_{ref})} \qquad \frac{R_2}{R_1} = \frac{V_3}{V_{th2} - V_{H2}} - 1$$

Figure 22. Positive and Negative Undervoltage Detector



The above figure shows the MC34161 configured as a positive and negative undervoltage detector. As the input voltage decreases toward ground, the LED will turn 'ON' when either V_{S1} falls below V_1, or $-V_{S2}$ falls below V_3. With the dashed line output connection, the circuit becomes a positive and negative overvoltage detector. As the input voltage increases from the ground, the LED will turn 'ON' when either V_{S1} exceeds V_2, or $-V_{S1}$ exceeds V_1.

For known resistor values, the voltage trip points are:

$$V_1 = (V_{th1} - V_{H1})\left(\frac{R_4}{R_3} + 1\right) \qquad V_3 = \frac{R_1}{R_2}(V_{th} - V_{ref}) + V_{th2}$$

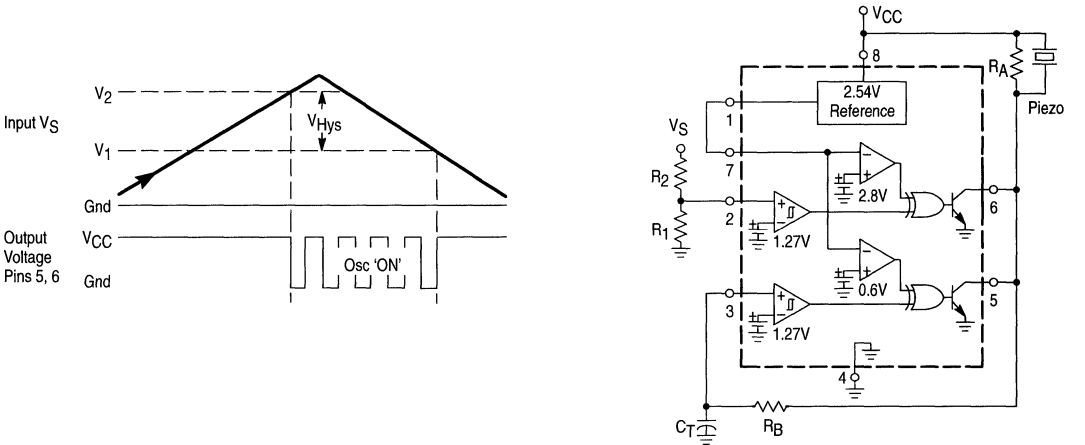
$$V_2 = V_{th1}\left(\frac{R_4}{R_3} + 1\right) \qquad V_4 = \frac{R_1}{R_2}(V_{th} - V_{H2} - V_{ref}) + V_{th2} - V_{H2}$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_4}{R_3} = \frac{V_2}{V_{th1}} - 1 \qquad \frac{R_1}{R_2} = \frac{V_4 + V_{H2} - V_{th2}}{V_{th2} - V_{H2} - V_{ref}}$$

$$\frac{R_4}{R_3} = \frac{V_1}{V_{th1} - V_{H1}} - 1 \qquad \frac{R_1}{R_2} = \frac{V_3 - V_{th2}}{V_{th2} - V_{ref}}$$

Figure 23. Overvoltage Detector with Audio Alarm



The above figure shows the MC34161 configured as an overvoltage detector with an audio alarm. Channel 1 monitors input voltage V_S while channel 2 is connected as a simple RC oscillator. As the input voltage increases from ground, the output of channel 1 allows the oscillator to turn 'ON' when V_S exceeds V_2.

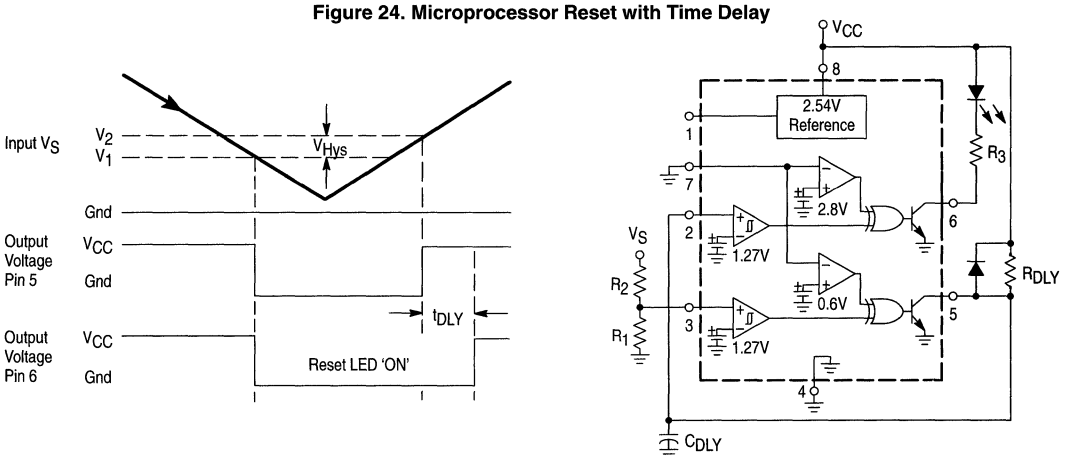
For known resistor values, the voltage trip points are:

$$V_1 = (V_{th} - V_H)\left(\frac{R_2}{R_1} + 1\right) \quad V_2 = V_{th}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_1}{V_{th} - V_H} - 1 \qquad \frac{R_2}{R_1} = \frac{V_2}{V_{th}} - 1$$

Figure 24. Microprocessor Reset with Time Delay



The above figure shows the MC34161 configured as a microprocessor reset with a time delay. Channel 2 monitors input voltage V_S while channel 1 performs the time delay function. As the input voltage decreases towards ground, the output of channel 2 quickly discharges C_{DLY} when V_S falls below V_1. As the input voltage increases from ground, the output of channel 2 allows R_{DLY} to charge C_{DLY} when V_S exceeds V_2.

For known resistor values, the voltage trip points are:

$$V_1 = (V_{th} - V_H)\left(\frac{R_2}{R_1} + 1\right) \quad V_2 = V_{th}\left(\frac{R_2}{R_1} + 1\right)$$

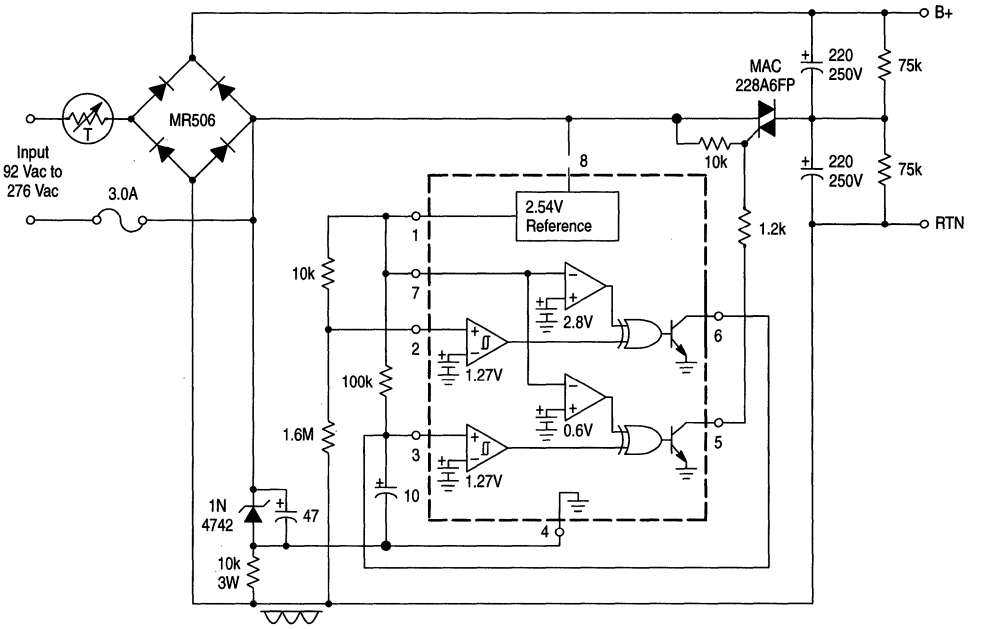
For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_1}{V_{th} - V_H} - 1 \qquad \frac{R_2}{R_1} = \frac{V_2}{V_{th}} - 1$$

For known R_{DLY} C_{DLY} values, the reset time delay is:

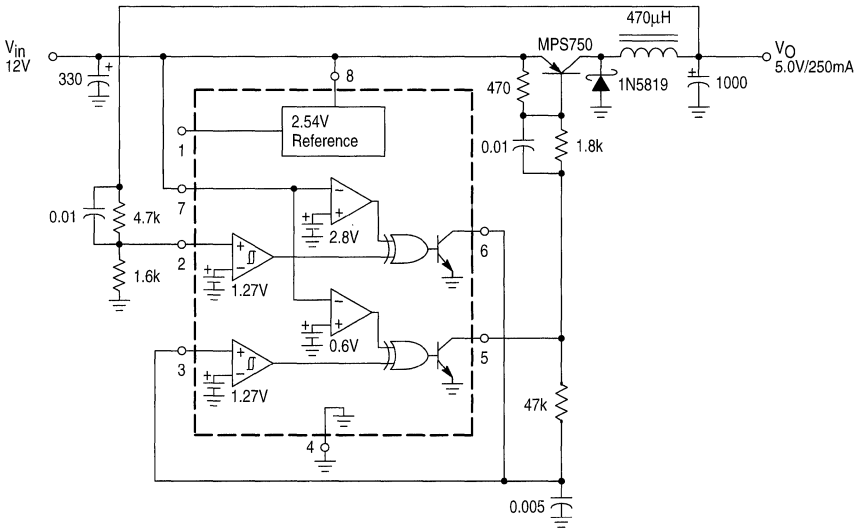
$$t_{DLY} = R_{DLY}C_{DLY} \ln\left(\frac{1}{1 - \frac{V_{th}}{V_{CC}}}\right)$$

Figure 25. Automatic AC Line Voltage Selector



The above circuit shows the MC34161 configured as an automatic line voltage selector. The IC controls the triac, enabling the circuit to function as a fullwave voltage doubler or a fullwave bridge. Channel 1 senses the negative half cycles of the AC line voltage. If the line voltage is less than150 V, the circuit will switch from bridge mode to voltage doubling mode after a preset time delay. The delay is controlled by the 100 kΩ resistor and the 10 μF capacitor. If the line voltage is greater than 150 V, the circuit will immediately return to fullwave bridge mode.

Figure 26. Step–Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 9.5 V to 24 V, I_O = 250 mA	40 mV = ±0.1%
Load Regulation	V_{in} = 12 V, I_O = 0.25 mA to 250 mA	2.0 mV = ±0.2%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	50 mVpp
Efficiency	V_{in} = 12 V, I_O = 250 mA	87.8%

The above figure shows the MC34161 configured as a step–down converter. Channel 1 monitors the output voltage while Channel 2 performs the oscillator function. Upon initial power–up, the converters output voltage will be below nominal, and the output of Channel 1 will allow the oscillator to run. The external switch transistor will eventually pump–up the output capacitor until its voltage exceeds the input threshold of Channel 1. The output of Channel 1 will then switch low and disable the oscillator. The oscillator will commence operation when the output voltage falls below the lower threshold of Channel 1.

MOTOROLA

MC34163
MC33163

Power Switching Regulators

3

The MC34163 series are monolithic power switching regulators that contain the primary functions required for dc–to–dc converters. This series is specifically designed to be incorporated in step–up, step–down, and voltage–inverting applications with a minimum number of external components.

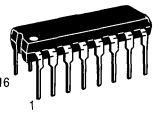
These devices consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle–by–cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

These devices are contained in a 16 pin dual–in–line heat tab plastic package for improved thermal conduction.

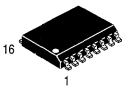
- Output Switch Current in Excess of 3.0 A
- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Precision 2% Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle–by–Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package

POWER SWITCHING REGULATORS

SEMICONDUCTOR TECHNICAL DATA

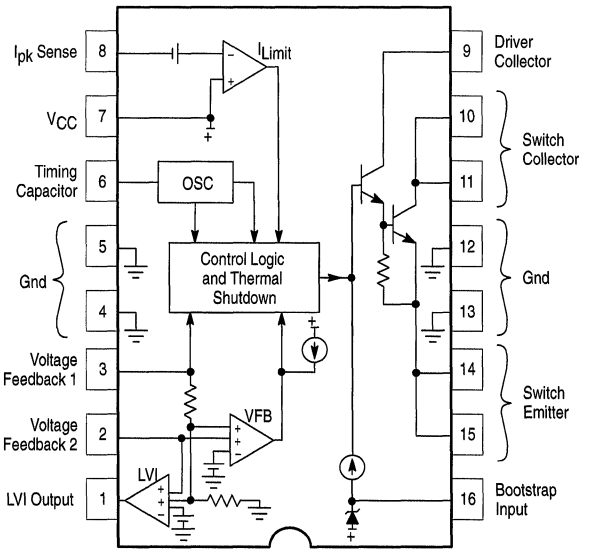


P SUFFIX
PLASTIC PACKAGE
CASE 648C
(DIP–16)



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP–16L)

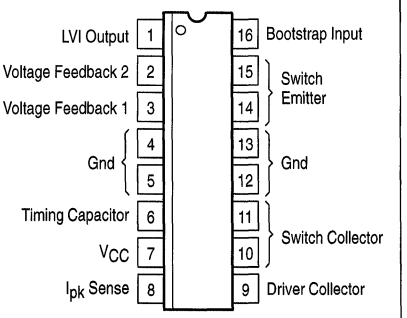
Representative Block Diagram



(Bottom View)

This device contains 114 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34163DW	T_A = 0° to +70°C	SOP–16L
MC34163P		DIP–16
MC33163DW	T_A = – 40° to +85°C	SOP–16L
MC33163P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Switch Collector Voltage Range	$V_{C(switch)}$	−1.0 to + 40	V
Switch Emitter Voltage Range	$V_{E(switch)}$	− 2.0 to $V_{C(switch)}$	V
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	V
Switch Current (Note 1)	I_{SW}	3.4	A
Driver Collector Voltage	$V_{C(driver)}$	−1.0 to +40	V
Driver Collector Current	$I_{C(driver)}$	150	mA
Bootstrap Input Current Range (Note 1)	I_{BS}	−100 to +100	mA
Current Sense Input Voltage Range	$V_{Ipk(Sense)}$	(V_{CC}−7.0) to (V_{CC}+1.0)	V
Feedback and Timing Capacitor Input Voltage Range	V_{in}	−1.0 to + 7.0	V
Low Voltage Indicator Output Voltage Range	$V_{C(LVI)}$	−1.0 to + 40	V
Low Voltage Indicator Output Sink Current	$I_{C(LVI)}$	10	mA
Thermal Characteristics P Suffix, Dual–In–Line Case 648C Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13) DW Suffix, Surface Mount Case 751G Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	 $R_{\theta JA}$ $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JC}$	 80 15 94 18	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34163 MC33163	T_A	 0 to +70 − 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency T_A = 25°C Total Variation over V_{CC} = 2.5 V to 40 V, and Temperature	f_{OSC}	 46 45	 50 –	 54 55	kHz
Charge Current	I_{chg}	–	225	–	µA
Discharge Current	I_{dischg}	–	25	–	µA
Charge to Discharge Current Ratio	I_{chg}/I_{dischg}	8.0	9.0	10	–
Sawtooth Peak Voltage	$V_{OSC(P)}$	–	1.25	–	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	–	0.55	–	V
FEEDBACK COMPARATOR 1					
Threshold Voltage T_A = 25°C Line Regulation (V_{CC} = 2.5 V to 40 V, T_A = 25°C) Total Variation over Line, and Temperature	$V_{th(FB1)}$	 4.9 – 4.85	 5.05 0.008 –	 5.2 0.03 5.25	 V %/V V
Input Bias Current (V_{FB1} = 5.05 V)	$I_{IB(FB1)}$	–	100	200	µA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34163 T_{high} = + 70°C for MC34163
= − 40°C for MC33163 = + 85°C for MC33163

3

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FEEDBACK COMPARATOR 2					
Threshold Voltage	$V_{th(FB2)}$				
T_A = 25°C		1.225	1.25	1.275	V
Line Regulation (V_{CC} = 2.5 V to 40 V, T_A = 25°C)		–	0.008	0.03	%/V
Total Variation over Line, and Temperature		1.213	–	1.287	V
Input Bias Current (V_{FB2} = 1.25 V)	$I_{IB(FB2)}$	– 0.4	0	0.4	µA
CURRENT LIMIT COMPARATOR					
Threshold Voltage	$V_{th(Ipk\ Sense)}$				mV
T_A = 25°C		–	250	–	
Total Variation over V_{CC} = 2.5 V to 40 V, and Temperature		230	–	270	
Input Bias Current ($V_{Ipk\ (Sense)}$ = 15 V)	$I_{IB(sense)}$	–	1.0	20	µA
DRIVER AND OUTPUT SWITCH (Note 2)					
Sink Saturation Voltage (I_{SW} = 2.5 A, Pins 14, 15 grounded)	$V_{CE(sat)}$				V
Non–Darlington Connection ($R_{Pin\ 9}$ = 110 Ω to V_{CC}, $I_{SW}/I_{DRV} \approx 20$)		–	0.6	1.0	
Darlington Connection (Pins 9, 10, 11 connected)		–	1.0	1.4	
Collector Off–State Leakage Current (V_{CE} = 40 V)	$I_{C(off)}$	–	0.02	100	µA
Bootstrap Input Current Source (V_{BS} = V_{CC} + 5.0 V)	$I_{source(DRV)}$	0.5	2.0	4.0	mA
Bootstrap Input Zener Clamp Voltage (I_Z = 25 mA)	V_Z	V_{CC} + 6.0	V_{CC} + 7.0	V_{CC} + 9.0	V
LOW VOLTAGE INDICATOR					
Input Threshold (V_{FB2} Increasing)	V_{th}	1.07	1.125	1.18	V
Input Hysteresis (V_{FB2} Decreasing)	V_H	–	15	–	mV
Output Sink Saturation Voltage (I_{sink} = 2.0 mA)	$V_{OL(LVI)}$	–	0.15	0.4	V
Output Off–State Leakage Current (V_{OH} = 15 V)	I_{OH}	–	0.01	5.0	µA
TOTAL DEVICE					
Standby Supply Current (V_{CC} = 2.5 V to 40 V, Pin 8 = V_{CC}, Pins 6, 14, 15 = Gnd, remaining pins open)	I_{CC}	–	6.0	10	mA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34163, = – 40°C for MC33163; T_{high} = + 70°C for MC34163, = + 85°C for MC33163

Figure 1. Output Switch On–Off Time versus Oscillator Timing Capacitor

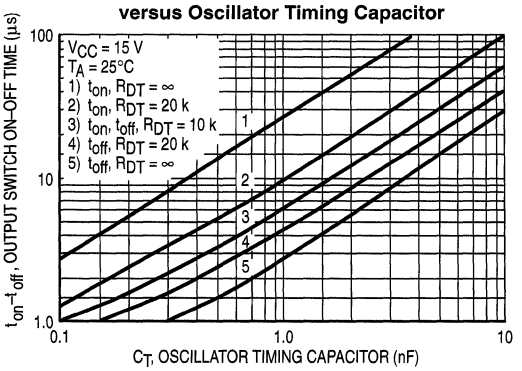


Figure 2. Oscillator Frequency Change versus Temperature

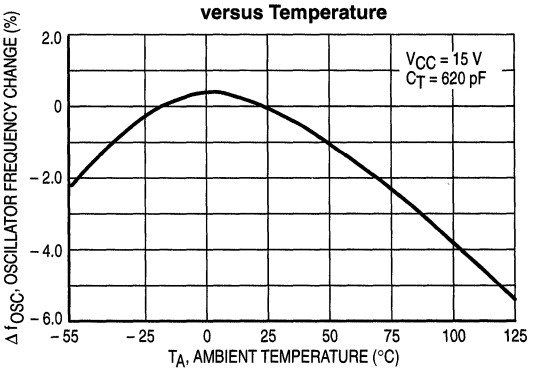


Figure 3. Feedback Comparator 1 Input Bias Current versus Temperature

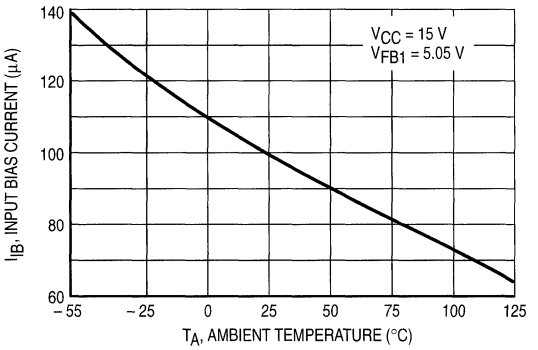


Figure 4. Feedback Comparator 2 Threshold Voltage versus Temperature

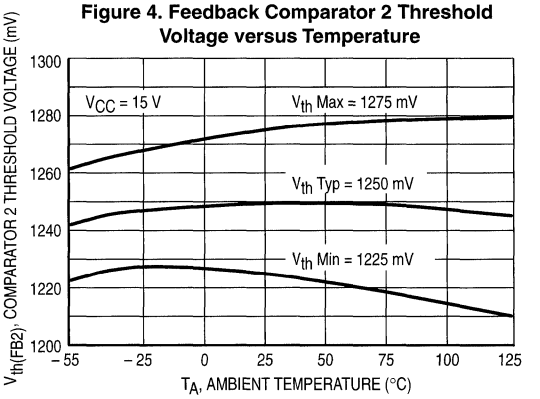


Figure 5. Bootstrap Input Current Source versus Temperature

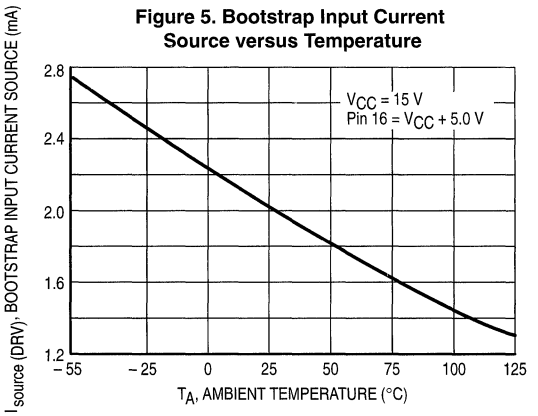


Figure 6. Bootstrap Input Zener Clamp Voltage versus Temperature

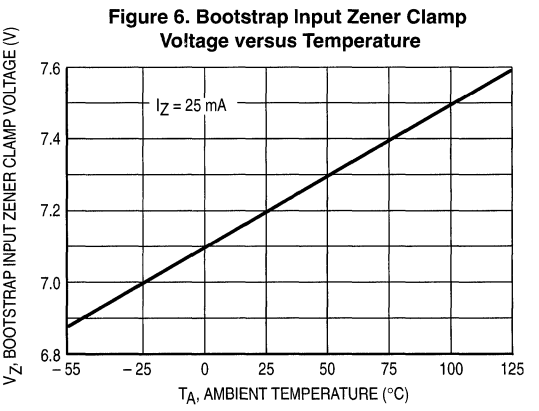


Figure 7. Output Switch Source Saturation versus Emitter Current

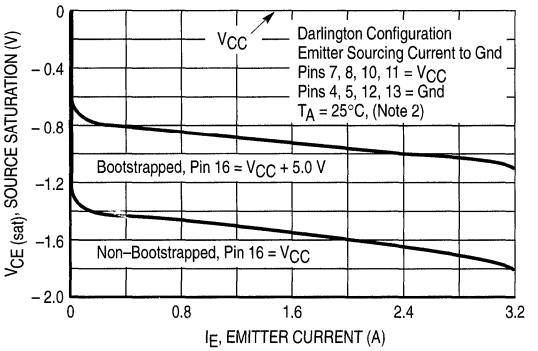
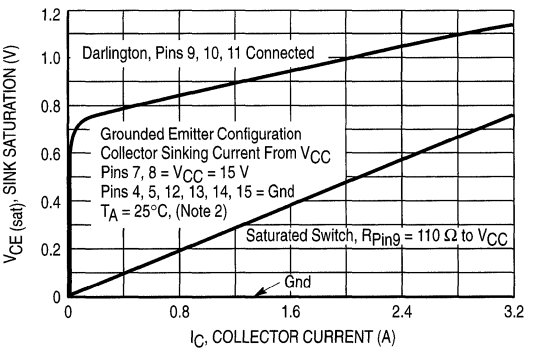


Figure 8. Output Switch Sink Saturation versus Collector Current



3

Figure 9. Output Switch Negative Emitter Voltage versus Temperature

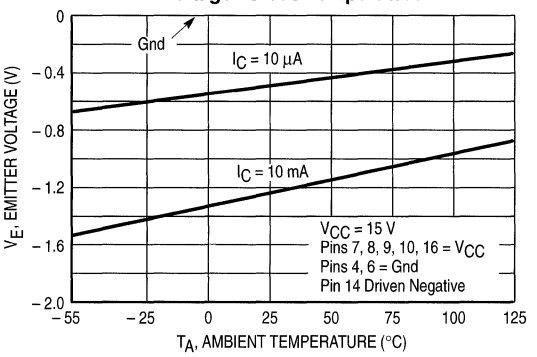


Figure 10. Low Voltage Indicator Output Sink Saturation Voltage versus Sink Current

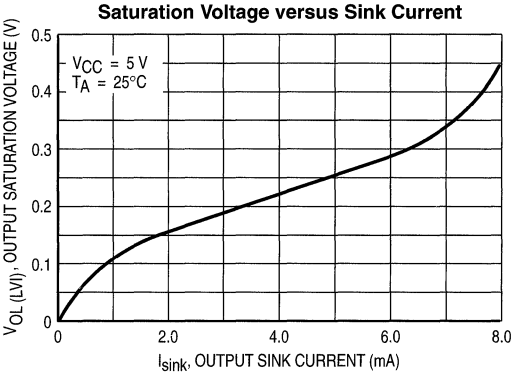


Figure 11. Current Limit Comparator Threshold Voltage versus Temperature

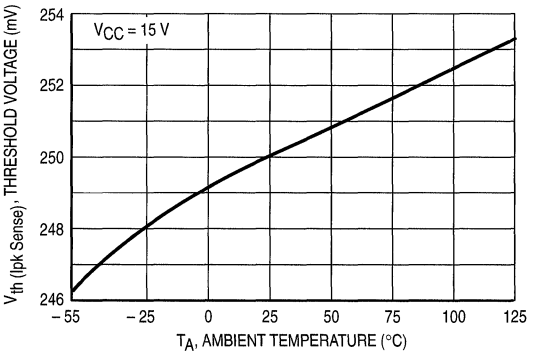


Figure 12. Current Limit Comparator Input Bias Current versus Temperature

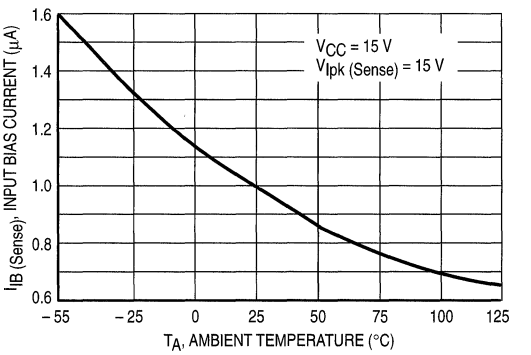


Figure 13. Standby Supply Current versus Supply Voltage

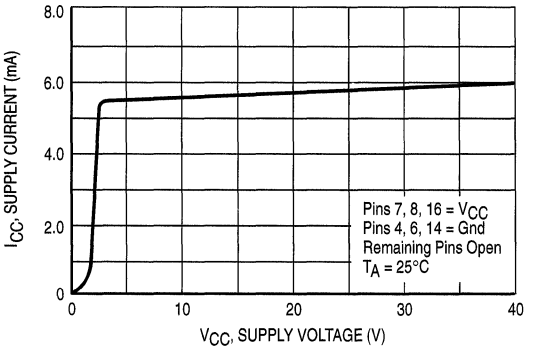


Figure 14. Standby Supply Current versus Temperature

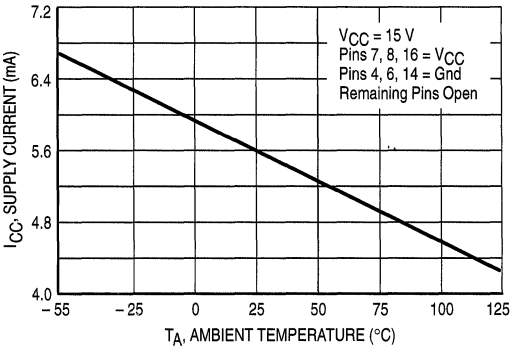


Figure 15. Minimum Operating Supply Voltage versus Temperature

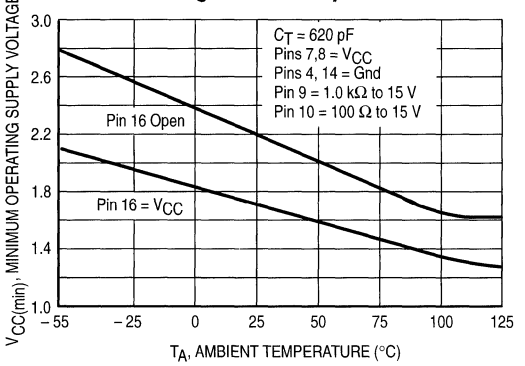


Figure 16. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

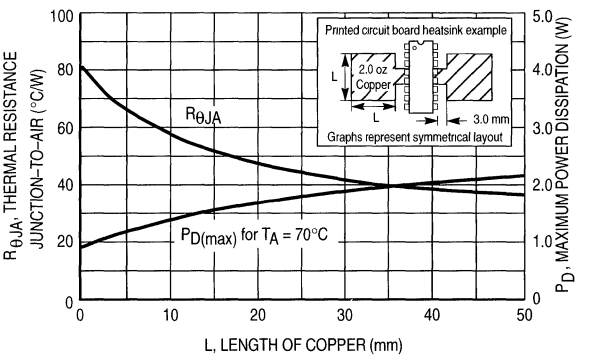
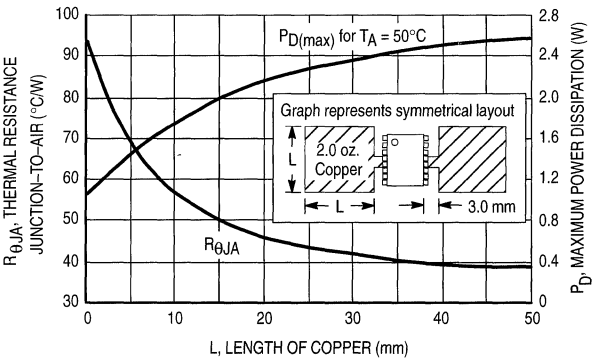


Figure 17. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



3

Figure 18. Representative Block Diagram

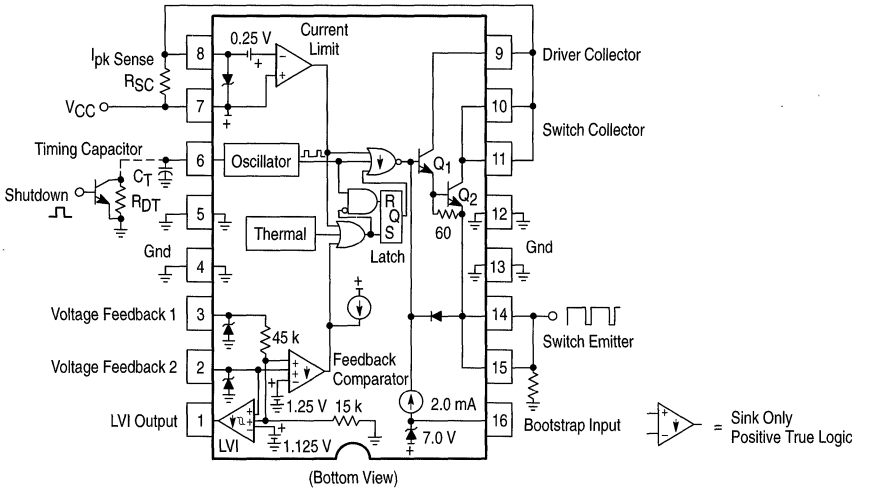
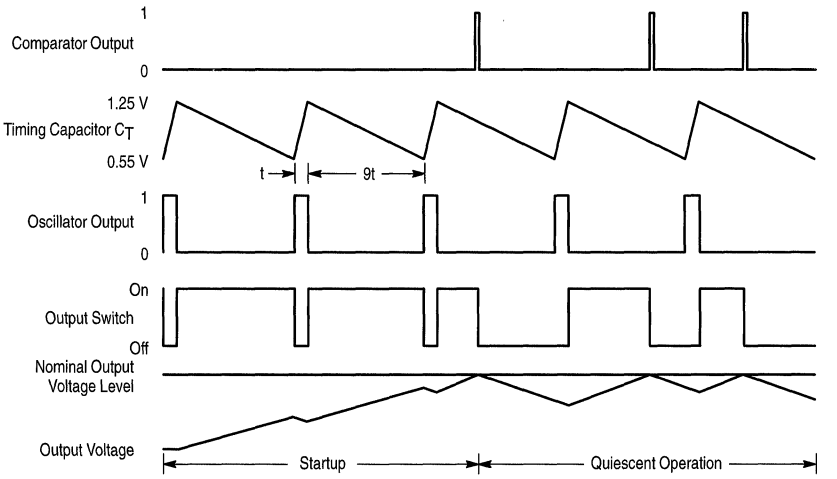


Figure 19. Typical Operating Waveforms



INTRODUCTION

The MC34163 series are monolithic power switching regulators optimized for dc–to–dc converter applications. The combination of features in this series enables the system designer to directly implement step–up, step–down, and voltage–inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. A Representative Block Diagram is shown in Figure 18.

OPERATING DESCRIPTION

The MC34163 operates as a fixed on–time, variable off–time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 19. The output voltage waveform shown is for a step–down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and on–time of the output switch are programmed by the value selected for timing capacitor C_T. Capacitor C_T is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As C_T charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp–up and can be enabled by the comparator output only at the start of ramp–down. The oscillator peak and valley thresholds are 1.25 V and 0.55 V, respectively, with a charge current of 225 μA and a discharge current of 25 μA, yielding a maximum on–time duty cycle of 90%. A reduction of the maximum duty cycle may be required for specific converter configurations. This can be accomplished with the addition of an external deadtime resistor (R_{DT}) placed across C_T. The resistor increases the discharge current which reduces the on–time of the output switch. A graph of the Output Switch On–Off Time versus Oscillator Timing Capacitance for various values of R_{DT} is shown in Figure 1. Note that the maximum output duty cycle, $t_{on}/t_{on} + t_{off}$, remains constant for values of C_T greater than 0.2 nF. The converter output can be inhibited by clamping C_T to ground with an external NPN small–signal transistor.

Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25 V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is ±0.4 μA, which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0 V, the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05 V. The additional 50 mV compensates for a 1.0% voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's output state is controlled by the highest voltage applied to either of the two noninverting inputs.

The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor–based systems. The inverting input is internally biased at 1.125 V, which sets the noninverting input thresholds to 90% of nominal. The LVI comparator has 15 mV of hysteresis to prevent erratic reset operation. The Open Collector output is capable of sinking in excess of 6.0 mA (see Figure 10). An external resistor (R_{LVI}) and capacitor (C_{DLY}) can be used to program a reset delay time (t_{DLY}) by the formula shown below, where $V_{th(MPU)}$ is the microprocessor reset input threshold. Refer to Figure 20.

$$t_{DLY} = R_{LVI}\, C_{DLY}\, \ln\left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{out}}}\right)$$

Current Limit Comparator, Latch and Thermal Shutdown

With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC}, in series with V_{CC} and output switch transistor Q_2. The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 250 mV with respect to V_{CC}, the comparator will set the latch and terminate output switch conduction on a cycle–by–cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on–time during a given oscillator cycle. The calculation for a value of R_{SC} is:

$$R_{SC} = \frac{0.25\ V}{I_{pk(Switch)}}$$

Figures 11 and 12 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of 1.0 μA. The propagation delay from the comparator input to the Output Switch is typically 200 ns. The parasitic inductance associated with R_{SC} and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the Latch is forced into the "Set" state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch has a typical current gain of 70 at 2.5 A and is designed to switch a maximum of 40 V collector to emitter, with up to 3.4 A peak collector current. The minimum value for R_{SC} is:

$$R_{SC(min)} = \frac{0.25\,V}{3.4\,A} = 0.0735\,\Omega$$

When configured for step–down or voltage–inverting applications, as in Figures 20 and 24, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn–on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency.

Figure 9 shows that by clamping the emitter to 0.5 V, the collector current will be in the range 10 μA over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

A bootstrap input is provided to reduce the output switch saturation voltage in step–down and voltage–inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0 mA bias current source above V_{CC}. An internal zener limits the bootstrap input voltage to V_{CC} +7.0 V. The capacitor's equivalent series resistance must limit the zener current to less than 100 mA. An additional series resistor may be required when using tantalum or other low ESR capacitors. The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$C_{B(min)} = I\,\frac{\Delta t}{\Delta V} = 4.0\ mA\,\frac{t_{on}}{4.0\,V} = 0.001\,t_{on}$$

Parametric operation of the MC34163 is guaranteed over a supply voltage range of 2.5 V to 40 V. When operating below 3.0 V, the Bootstrap Input should be connected to V_{CC}. Figure 15 shows that functional operation down to 1.7 V at room temperature is possible.

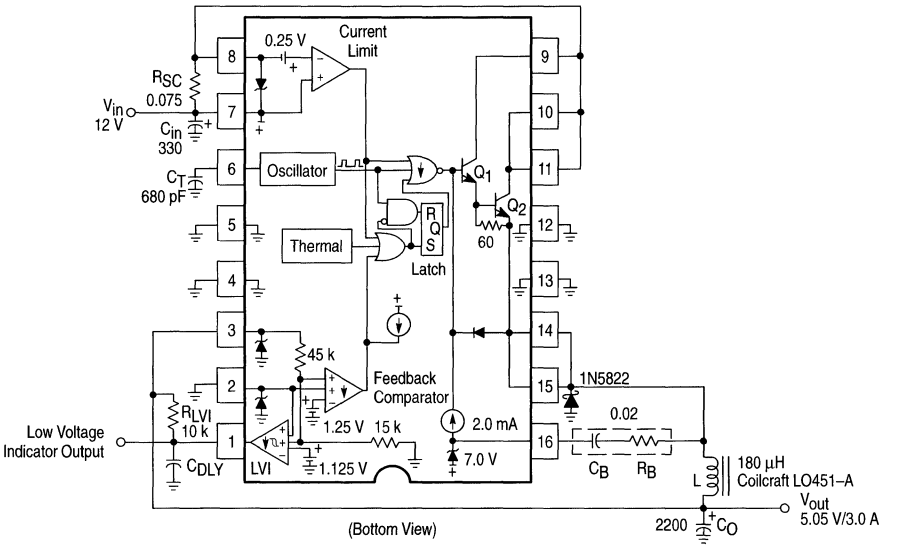
Package

The MC34163 is contained in a heatsinkable 16–lead plastic dual–in–line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 16 and 17 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction–to–air thermal resistance. These examples are for a symmetrical layout on a single–sided board with two ounce per square foot of copper.

APPLICATIONS

The following converter applications show the simplicity and flexibility of this circuit architecture. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

Figure 20. Step–Down Converter



Test	Condition	Results
Line Regulation	V_{in} = 8.0 V to 24 V, I_O = 3.0 A	6.0 mV = ± 0.06%
Load Regulation	V_{in} = 12 V, I_O = 0.6 A to 3.0 A	2.0 mV = ± 0.02%
Output Ripple	V_{in} = 12 V, I_O = 3.0 A	36 mVpp
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	3.3 A
Efficiency, Without Bootstrap	V_{in} = 12 V, I_O = 3.0 A	76.7%
Efficiency, With Bootstrap	V_{in} = 12 V, I_O = 3.0 A	81.2%

Figure 21. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 3.4 A

Figure 21A. External NPN Switch

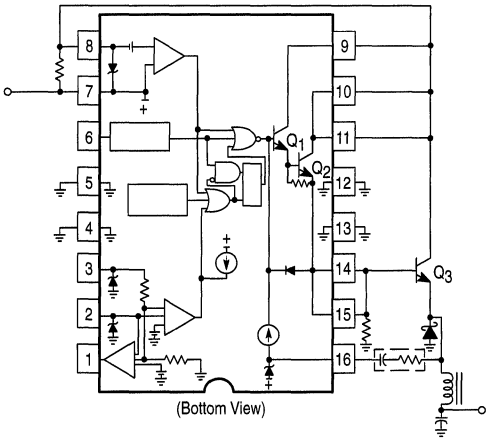
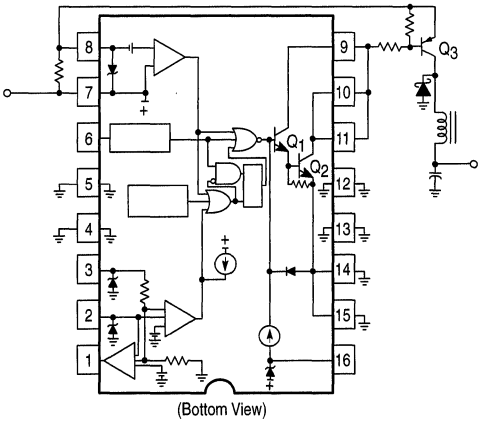
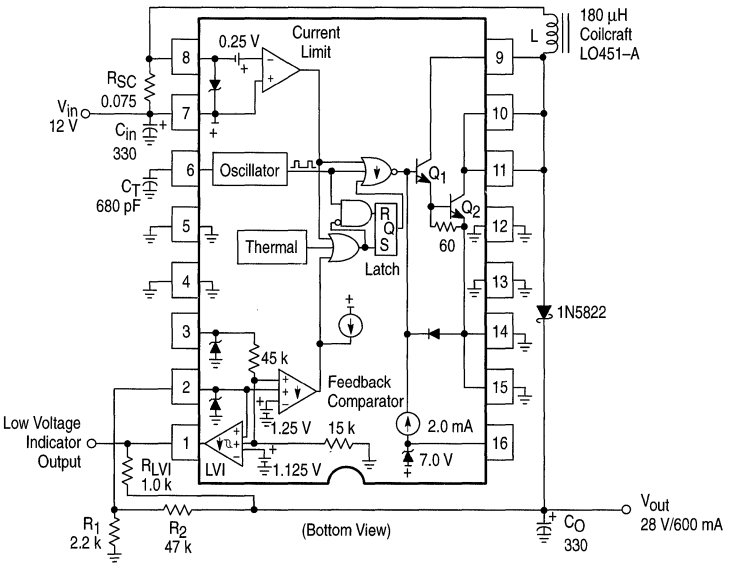


Figure 21B. External PNP Saturated Switch



3

Figure 22. Step–Up Converter



Test	Condition	Results
Line Regulation	V_{in} = 9.0 V to 16 V, I_O = 0.6 A	30 mV = ± 0.05%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 0.6 A	50 mV = ± 0.09%
Output Ripple	V_{in} = 12 V, I_O = 0.6 A	140 mVpp
Efficiency	V_{in} = 12 V, I_O = 0.6 A	88.1%

Figure 23. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 3.4 A

Figure 23A. External NPN Switch

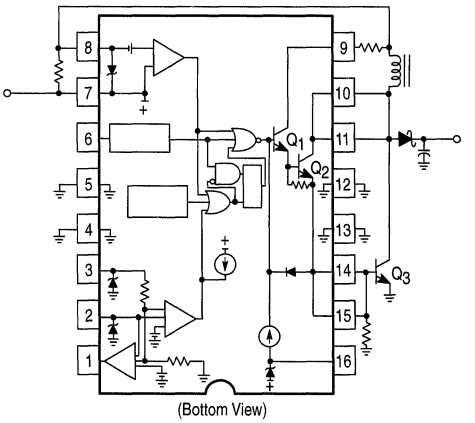


Figure 23B. External PNP Saturated Switch

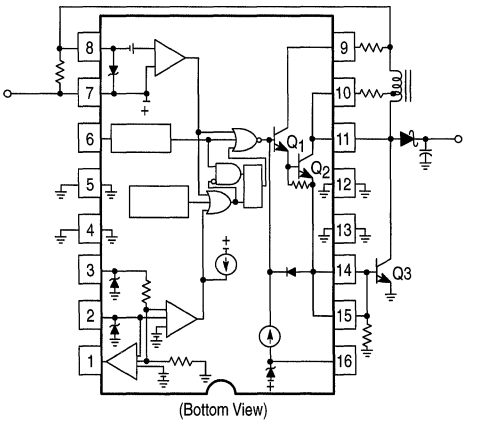
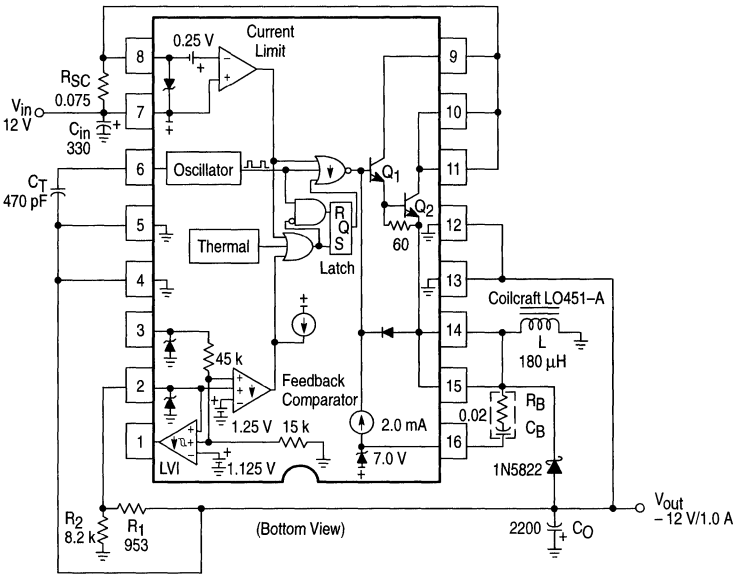


Figure 24. Voltage–Inverting Converter



Test	Condition	Results
Line Regulation	V_{in} = 9.0 V to 16 V, I_O = 1.0 A	5.0 mV = ± 0.02%
Load Regulation	V_{in} = 12 V, I_O = 0.6 A to 1.0 A	2.0 mV = ± 0.01%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	130 mVpp
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	3.2 A
Efficiency, Without Bootstrap	V_{in} = 12 V, I_O = 1.0 A	73.1%
Efficiency, With Bootstrap	V_{in} = 12 V, I_O = 1.0 A	77.5%

Figure 25. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 3.4 A

Figure 25A. External NPN Switch

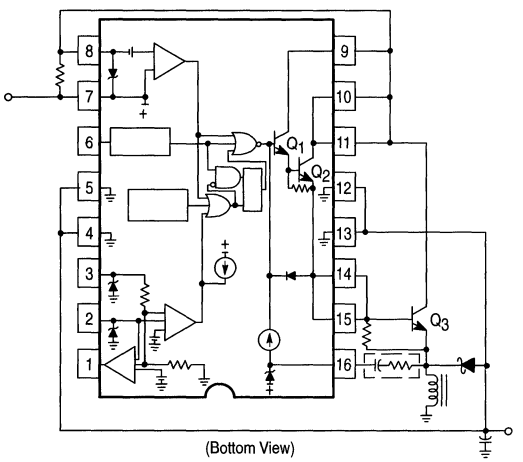


Figure 25B. External PNP Saturated Switch

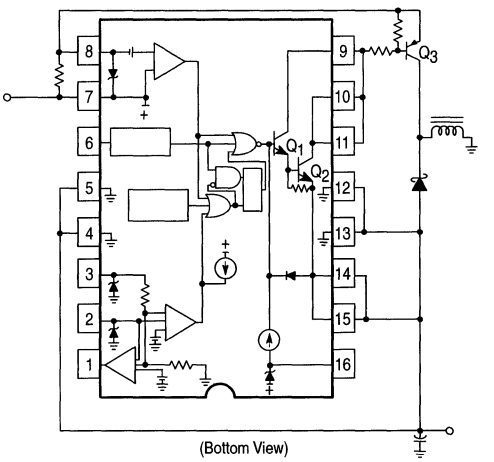
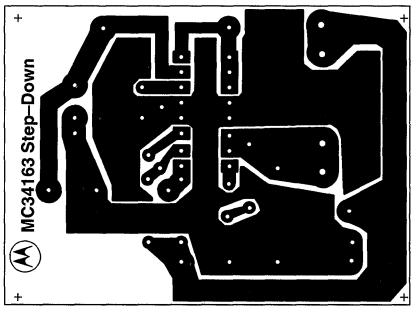
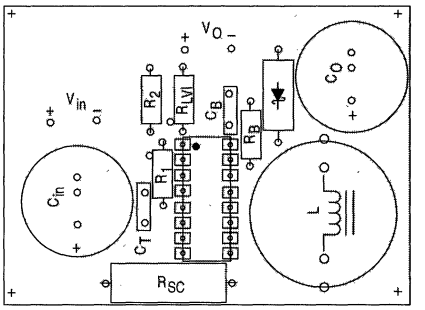


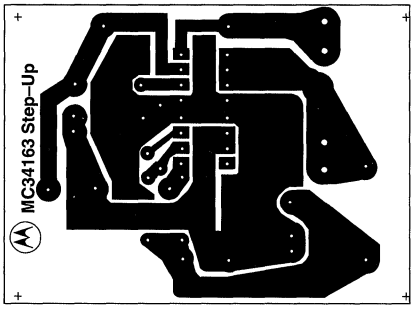
Figure 26. Printed Circuit Board and Component Layout
(Circuits of Figures 20, 22, 24)



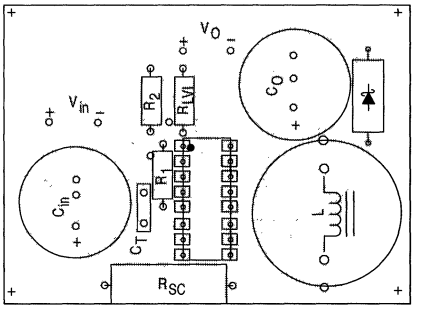
Bottom View



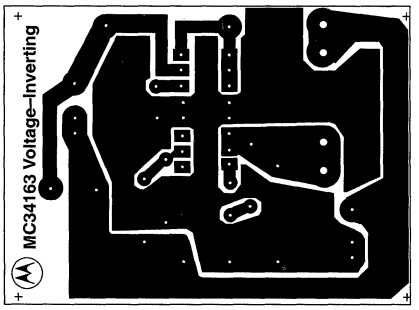
Top View



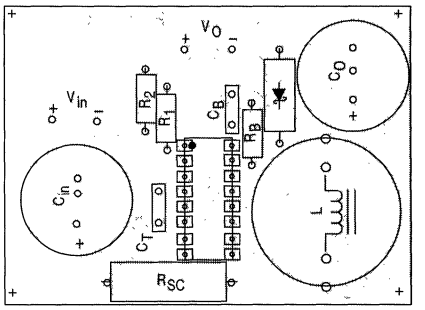
Bottom View



Top View



Bottom View



Top View

All printed circuit boards are 2.58" in width by 1.9" in height.

Figure 27. Design Equations

Calculation	Step–Down	Step–Up	Voltage–Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2, 3)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$
C_T	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$
$I_{L(avg)}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk\ (Switch)}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.25}{I_{pk\ (Switch)}}$	$\frac{0.25}{I_{pk\ (Switch)}}$	$\frac{0.25}{I_{pk\ (Switch)}}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8f\,C_O}\right)^2 + (ESR)^2}$	$\approx \frac{t_{on}\, I_{out}}{C_O}$	$\approx \frac{t_{on}\, I_{out}}{C_O}$
V_{out}	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$

The following Converter Characteristics must be chosen:

V_{in} – Nominal operating input voltage.
V_{out} – Desired output voltage.
I_{out} – Desired output current.
ΔI_L – Desired peak–to–peak inductor ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk\ (Switch)}$ from reaching the current limit threshold set by R_{SC}. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.
f – Maximum output switch frequency.
$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

NOTES: 1. V_{sat} – Saturation voltage of the output switch, refer to Figures 7 and 8.
2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5 V.
3. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8, at the minimum operating input voltage.

MC34164
MC33164

3

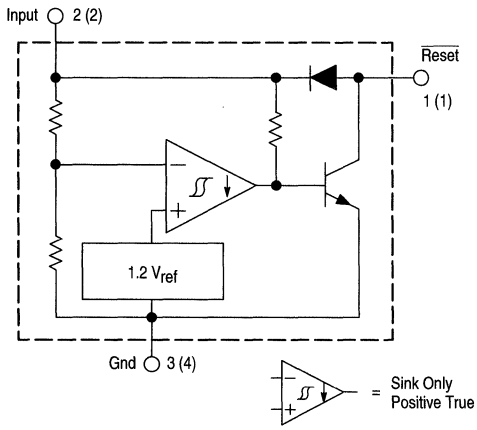
Micropower Undervoltage Sensing Circuits

The MC34164 series are undervoltage sensing circuits specifically designed for use as reset controllers in portable microprocessor based systems where extended battery life is required. These devices offer the designer an economical solution for low voltage detection with a single external resistor. The MC34164 series features a bandgap reference, a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation, an open collector reset output capable of sinking in excess of 6.0 mA, and guaranteed operation down to 1.0 V input with extremely low standby current. These devices are packaged in 3–pin TO–226AA, 8–pin SO–8 and Micro–8 surface mount packages.

Applications include direct monitoring of the 3.0 or 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.

- Temperature Compensated Reference
- Monitors 3.0 V (MC34164–3) or 5.0 V (MC34164–5) Power Supplies
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 6.0 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation With 1.0 V Input
- Extremely Low Standby Current: As Low as 9.0 μA
- Economical TO–226AA, SO–8 and Micro–8 Surface Mount Packages

Representative Block Diagram



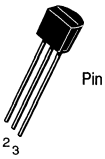
Pin numbers adjacent to terminals are for the 3–pin TO–226AA package.
Pin numbers in parenthesis are for the 8–lead packages.

This device contains 28 active transistors.

MICROPOWER UNDERVOLTAGE SENSING CIRCUITS

SEMICONDUCTOR TECHNICAL DATA

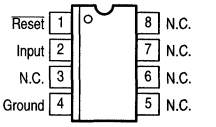
P SUFFIX
PLASTIC PACKAGE
CASE 29
(TO–226AA)



Pin 1. $\overline{\text{Reset}}$
2. Input
3. Ground

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34164D–3	T_A = 0° to +70°C	SO–8
MC34164D–5		
MC34164DM–3		Micro–8
MC34164DM–5		
MC34164P–3		TO–226AA
MC34164P–5		
MC33164D–3	T_A = –40° to +125°C	SO–8
MC33164D–5		
MC33164DM–3		Micro–8
MC33164DM–5		
MC33164P–3		TO–226AA
MC33164P–5		

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{in}	–1.0 to 12	V
$\overline{\text{Reset}}$ Output Voltage	V_O	–1.0 to 12	V
$\overline{\text{Reset}}$ Output Sink Current	I_{Sink}	Internally Limited	mA
Clamp Diode Forward Current, Pin 1 to 2 (Note 1)	I_F	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	700	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
D Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	700	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
DM Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	520	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	240	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A		°C
MC34164 Series		0 to +70	
MC33164 Series		– 40 to + 85	
Storage Temperature Range	T_{stg}	– 65 to +150	°C

NOTE: ESD data available upon request.

MC34164–3, MC33164–3 SERIES

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 & 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	2.55	2.71	2.80	
Low State Output (V_{in} Decreasing)	V_{IL}	2.55	2.65	2.80	
Hysteresis (I_{Sink} = 100 μA)	V_H	0.03	0.06	–	
$\overline{\text{RESET}}$ OUTPUT					
Output Sink Saturation	V_{OL}				V
(V_{in} = 2.4 V, I_{Sink} = 1.0 mA)		–	0.14	0.4	
(V_{in} = 1.0 V, I_{Sink} = 0.25 mA)		–	0.1	0.3	
Output Sink Current (V_{in}, $\overline{\text{Reset}}$ = 2.4 V)	I_{Sink}	6.0	12	30	mA
Output Off–State Leakage	$I_{\overline{R}(leak)}$				μA
(V_{in}, $\overline{\text{Reset}}$ = 3.0 V)		–	0.02	0.5	
(V_{in}, $\overline{\text{Reset}}$ = 10 V)		–	0.02	1.0	
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 5.0 mA)	V_F	6.0	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 10	–	–	V
Quiescent Input Current	I_{in}				μA
V_{in} = 3.0 V		–	9.0	15	
V_{in} = 6.0 V		–	24	40	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34164, – 40°C for MC33164; T_{high} = + 70°C for MC34164, = + 85°C for MC33164

3

MC34164–5, MC33164–5 SERIES

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 & 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	4.15	4.33	4.45	
Low State Output (V_{in} Decreasing)	V_{IL}	4.15	4.27	4.45	
Hysteresis (I_{Sink} = 100 μA)	V_H	0.02	0.09	–	
$\overline{\text{RESET}}$ OUTPUT					
Output Sink Saturation	V_{OL}				V
(V_{in} = 4.0 V, I_{Sink} = 1.0 mA)		–	0.14	0.4	
(V_{in} = 1.0 V, I_{Sink} = 0.25 mA)		–	0.1	0.3	
Output Sink Current (V_{in}, $\overline{\text{Reset}}$ = 4.0 V)	I_{Sink}	7.0	20	50	mA
Output Off–State Leakage	$I_{\overline{R}(leak)}$				μA
(V_{in}, $\overline{\text{Reset}}$ = 5.0 V)		–	0.02	0.5	
(V_{in}, $\overline{\text{Reset}}$ = 10 V)		–	0.02	2.0	
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 5.0 mA)	V_F	0.6	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 10	–	–	V
Quiescent Input Current	I_{in}				μA
V_{in} = 5.0 V		–	12	20	
V_{in} = 10 V		–	32	50	

NOTES: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34164, –40°C for MC33164; T_{high} = +70°C for MC34164, = +85°C for MC33164

Figure 1. MC3X164–3 $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

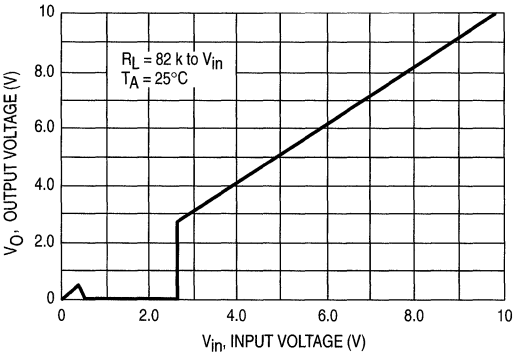


Figure 2. MC3X164–5 $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

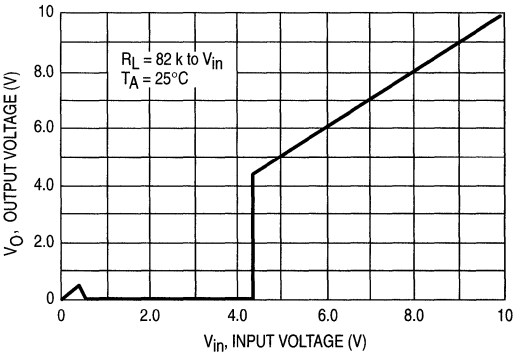


Figure 3. MC3X164–3 $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

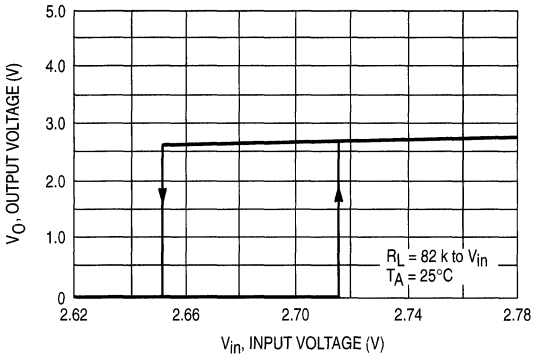


Figure 4. MC3X164–5 $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

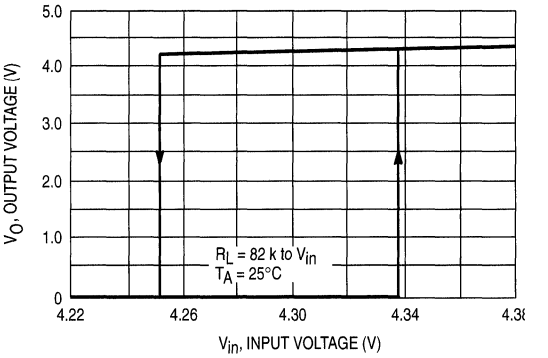


Figure 5. MC3X164–3 Comparator Threshold Voltage versus Temperature

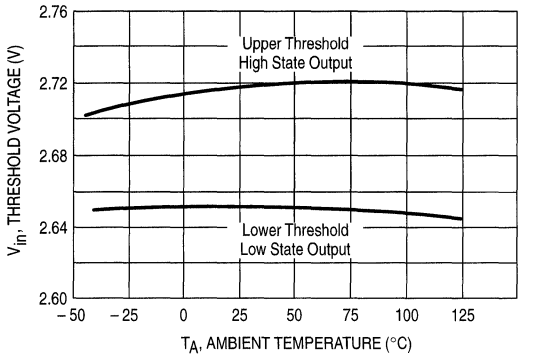


Figure 6. MC3X164–5 Comparator Threshold Voltage versus Temperature

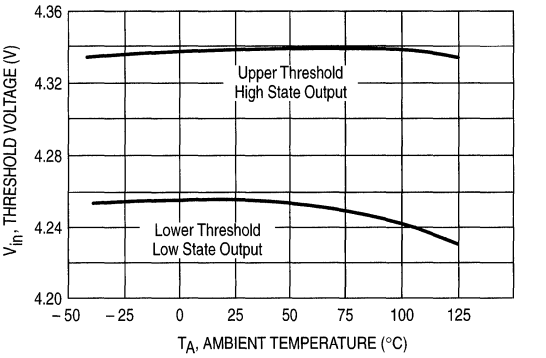


Figure 7. MC3X164–3 Input Current versus Input Voltage

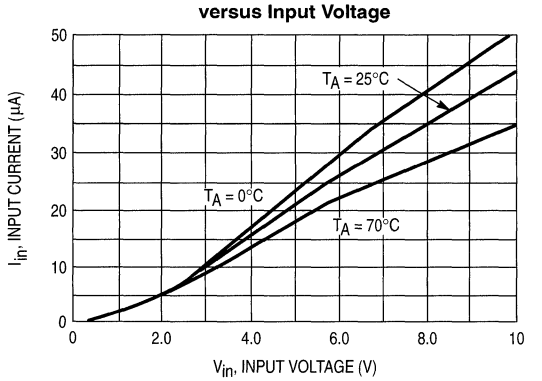


Figure 8. MC3X164–5 Input Current versus Input Voltage

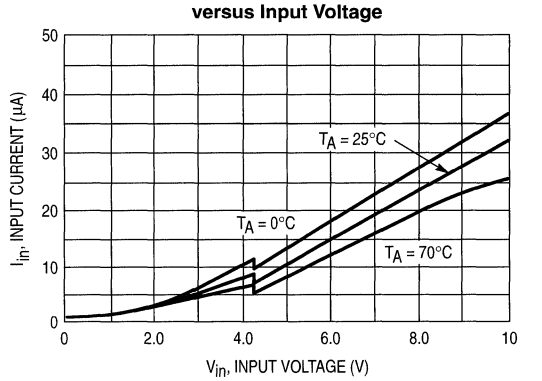


Figure 9. MC3X164–3 $\overline{\text{Reset}}$ Output Saturation versus Sink Current

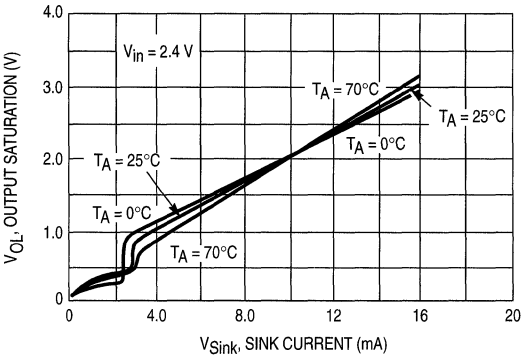


Figure 10. MC3X164–5 $\overline{\text{Reset}}$ Output Saturation versus Sink Current

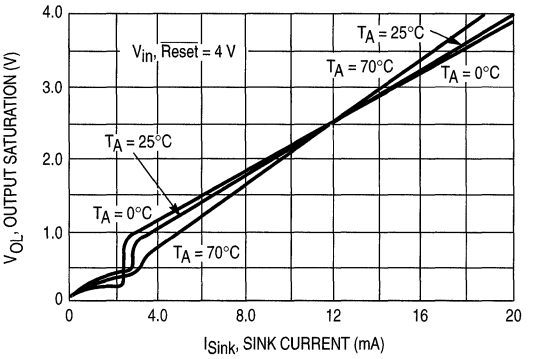


Figure 11. Clamp Diode Forward Current versus Voltage

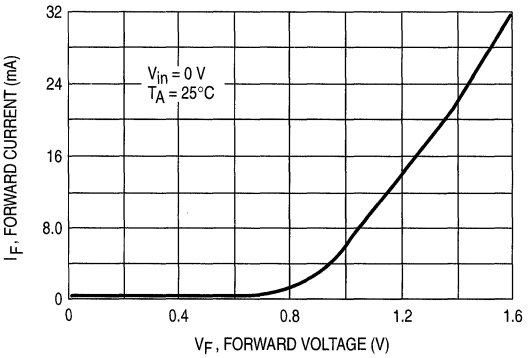


Figure 12. $\overline{\text{Reset}}$ Delay Time (MC3X164–5 Shown)

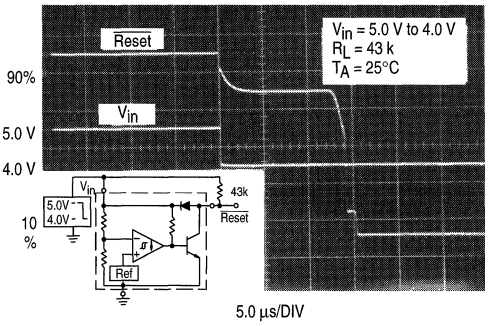
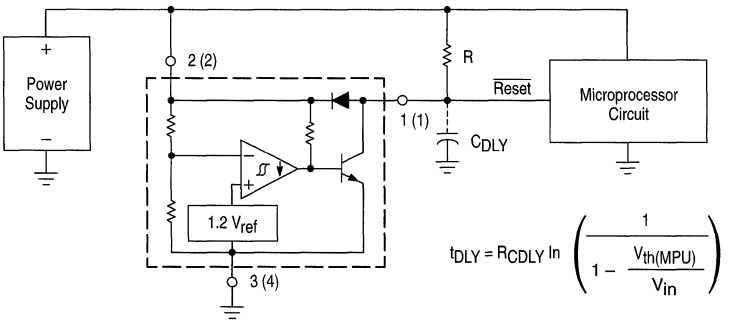
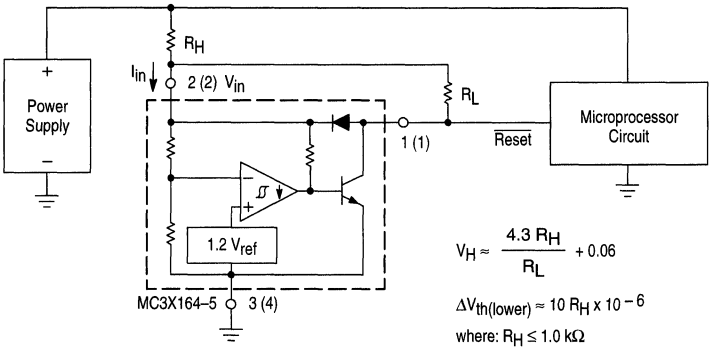


Figure 13. Low Voltage Microprocessor Reset



A time delayed reset can be accomplished with the addition of C_{DLY}. For systems with extremely fast power supply rise times (< 500 ns) it is recommended that the RCDLY time constant be greater than 5.0 µs. $V_{th(MPU)}$ is the microprocessor reset input threshold.

Figure 14. Low Voltage Microprocessor Reset With Additional Hysteresis (MC3X164–5 Shown)



Test Data			
V_H (mV)	ΔV_{th} (mV)	R_H (Ω)	R_L (kΩ)
60	0	0	43
103	1.0	100	10
123	1.0	100	6.8
160	1.0	100	4.3
155	2.2	220	10
199	2.2	220	6.8
280	2.2	220	4.3
262	4.7	470	10
306	4.7	470	8.2
357	4.7	470	6.8
421	4.7	470	5.6
530	4.7	470	4.3

Comparator hysteresis can be increased with the addition of resistor R_H. The hysteresis equation has been simplified and does not account for the change of input current I_{in} as V_{in} crosses the comparator threshold (Figure 8). An increase of the lower threshold $\Delta V_{th(lower)}$ will be observed due to I_{in} which is typically 10 µA at 4.3 V. The equations are accurate to ±10% with R_H less than 1.0 kΩ and R_L between 4.3 kΩ and 43 kΩ.

Figure 15. Voltage Monitor

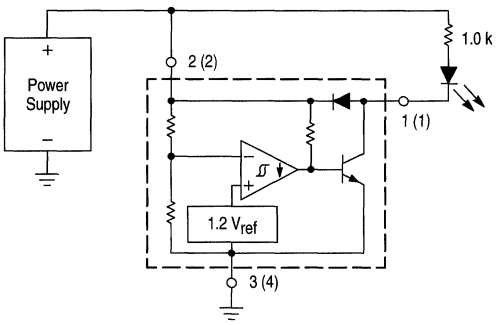


Figure 16. Solar Powered Battery Charger

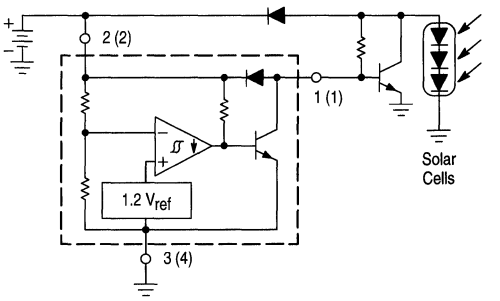
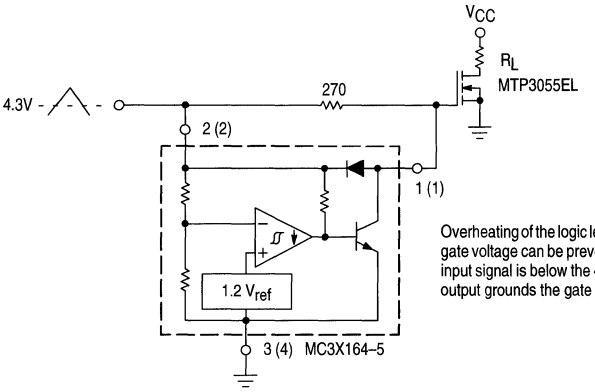


Figure 17. MOSFET Low Voltage Gate Drive Protection Using the MC3X164–5



Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.3 V threshold of the MC3X164–5, its output grounds the gate of the L^2 MOSFET.

MC34165
MC33165

Power Switching Regulators

3

The MC34165 series are monolithic power switching regulators that contain the primary functions required for DC–to–DC converters. This series is specifically designed to be incorporated in step–up, step–down, and voltage–inverting applications with a minimum number of external components.

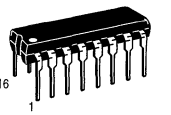
These devices consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle–by–cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

These devices are contained in a 16 pin dual–in–line heat tab plastic package for improved thermal conduction.

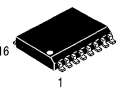
- Output Switch Current in Excess of 1.5 A
- Operation from 3.0 V to 65 V Input
- Low Standby Current
- Precision 2% Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle–by–Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package

POWER SWITCHING REGULATORS

SEMICONDUCTOR TECHNICAL DATA

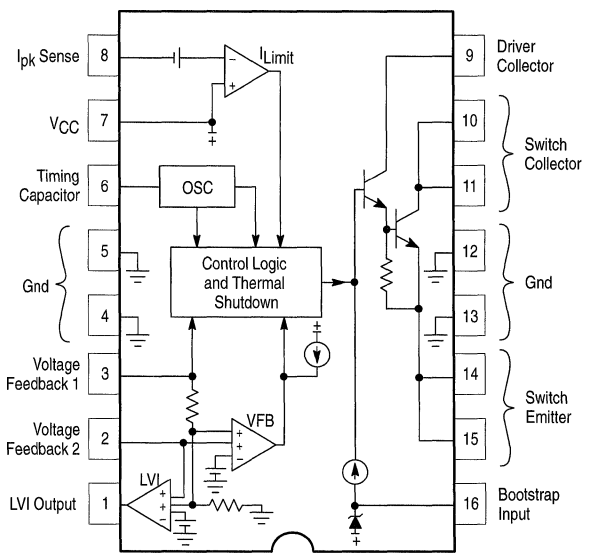


P SUFFIX
PLASTIC PACKAGE
CASE 648C
(DIP–16)



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP–16L)

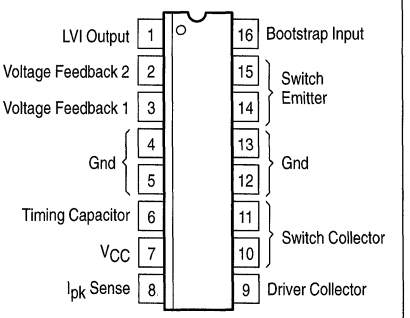
Representative Block Diagram



(Bottom View)

This device contains 114 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC34165DW	T_A = 0° to +70°C	SOP–16L
MC34165P		DIP–16
MC33165DW	T_A = – 40° to +85°C	SOP–16L
MC33165P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	65	V
Switch Collector Voltage Range	$V_{C(switch)}$	−1.0 to + 65	V
Switch Emitter Voltage Range	$V_{E(switch)}$	− 2.0 to $V_{C(switch)}$	V
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	65	V
Switch Current (Note 1)	I_{SW}	1.5	A
Driver Collector Voltage	$V_{C(driver)}$	−1.0 to +65	V
Driver Collector Current	$I_{C(driver)}$	70	mA
Bootstrap Input Current Range (Note 1)	I_{BS}	−100 to +100	mA
Current Sense Input Voltage Range	$V_{Ipk(Sense)}$	(V_{CC}−7.0) to (V_{CC}+1.0)	V
Feedback and Timing Capacitor Input Voltage Range	V_{in}	−1.0 to + 7.0	V
Low Voltage Indicator Output Voltage Range	$V_{C(LVI)}$	−1.0 to + 65	V
Low Voltage Indicator Output Sink Current	$I_{C(LVI)}$	10	mA
Thermal Characteristics P Suffix, Dual In Line Case 648C Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13) DW Suffix, Surface Mount Case 751G Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	 $R_{\theta JA}$ $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JC}$	 80 15 94 18	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34165 MC33165	T_A	 0 to +70 − 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency T_A = 25°C Total Variation over V_{CC} = 3.0 V to 65 V, and Temperature	f_{OSC}	 46 45	 50 –	 54 55	kHz
Charge Current	I_{chg}	–	225	–	µA
Discharge Current	I_{dischg}	–	25	–	µA
Charge to Discharge Current Ratio	I_{chg}/I_{dischg}	7.5	9.0	10	–
Sawtooth Peak Voltage	$V_{OSC(P)}$	–	1.25	–	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	–	0.55	–	V
FEEDBACK COMPARATOR 1					
Threshold Voltage T_A = 25°C Line Regulation (V_{CC} = 3.0 V to 65 V, T_A = 25°C) Total Variation over Line, and Temperature	$V_{th(FB1)}$	 4.9 – 4.85	 5.05 0.008 –	 5.2 0.03 5.25	 V %/V V
Input Bias Current (V_{FB1} = 5.05 V)	$I_{IB(FB1)}$	–	100	200	µA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34165 T_{high} = + 70°C for MC34165
= − 40°C for MC33165 = + 85°C for MC33165
4. The Low Voltage Indicator threshold tracks $V_{th(FB2)}$ and is expressed as a percent of the $V_{th(FB2)}$ threshold.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FEEDBACK COMPARATOR 2					
Threshold Voltage T_A = 25°C Line Regulation (V_{CC} = 3.0 V to 65 V, T_A = 25°C) Total Variation over Line, and Temperature	$V_{th(FB2)}$	 1.225 – 1.220	 1.25 0.008 –	 1.275 0.03 1.280	 V %/V V
Input Bias Current (V_{FB2} = 1.25 V)	$I_{IB(FB2)}$	– 0.4	0	0.4	µA
CURRENT LIMIT COMPARATOR					
Threshold Voltage T_A = 25°C Total Variation over V_{CC} = 3.0 V to 65 V, and Temperature	$V_{th(Ipk\ Sense)}$	 – 225	 245 –	 – 270	mV
Input Bias Current ($V_{Ipk\ (Sense)}$ = 15 V)	$I_{IB(sense)}$	–	1.0	5.0	µA
DRIVER AND OUTPUT SWITCH (Note 2)					
Sink Saturation Voltage (I_{SW} = 1.0 A, Pins 14, 15 grounded) Non–Darlington Connection ($R_{Pin\ 9}$ = 110 Ω to V_{CC}, I_{SW}/I_{DRV} ≈ 8) Darlington Connection (Pins 9, 10, 11 connected)	$V_{CE(sat)}$	 – –	 0.3 1.1	 0.7 1.4	V
Collector Off–State Leakage Current (V_{CE} = 65 V)	$I_{C(off)}$	–	0.02	100	µA
Bootstrap Input Current Source (V_{BS} = V_{CC} + 5.0 V)	$I_{source(DRV)}$	0.5	2.0	4.0	mA
Bootstrap Input Zener Clamp Voltage (I_Z = 25 mA)	V_Z	V_{CC} + 6.0	V_{CC} + 7.0	V_{CC} + 9.0	V
LOW VOLTAGE INDICATOR					
LVI Threshold (Percent of V_{FB}, Note 4) V_{FB2} Decreasing V_{FB2} Increasing	$V_{th(LVI)}$	 87 88	 88.3 89.9	 90 92	%
Hysteresis	V_H	–	20	–	mV
Output Sink Saturation Voltage (I_{sink} = 0.5 mA)	$V_{OL(LVI)}$	–	0.15	0.4	V
Output Off–State Leakage Current (V_{OH} = 15 V)	I_{OH}	–	0.01	1.0	µA
TOTAL DEVICE					
Standby Supply Current (V_{CC} = 3.0 V to 65 V, Pin 8 = V_{CC}, Pins 6, 14, 15 = Gnd, remaining pins open)	I_{CC}	–	6.0	10	mA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain as close to ambient as possible.
3. T_{low} = 0°C for MC34165 T_{high} = + 70°C for MC34165
= – 40°C for MC33165 = + 85°C for MC33165
4. The Low Voltage Indicator threshold tracks $V_{th(FB2)}$ and is expressed as a percent of the V_{FB2} threshold.

Figure 1. Output Switch On–Off Time versus Oscillator Timing Capacitor

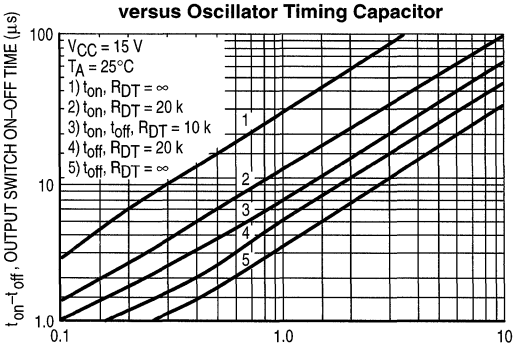


Figure 2. Oscillator Frequency Change versus Temperature

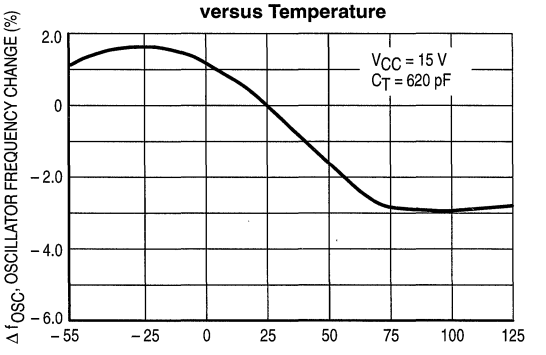


Figure 3. Feedback Comparator 1 Input Bias Current versus Temperature

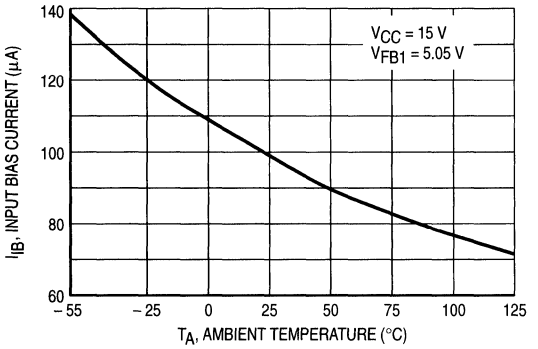


Figure 4. Feedback Comparator 2 Threshold Voltage versus Temperature

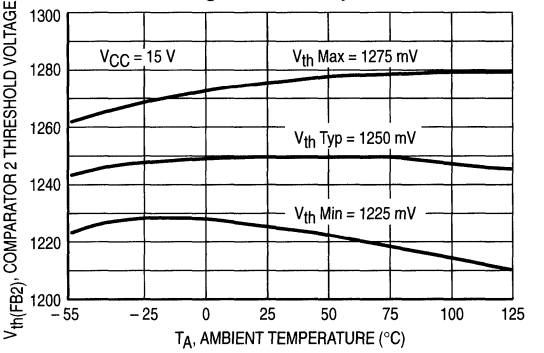


Figure 5. Bootstrap Input Current Source versus Temperature

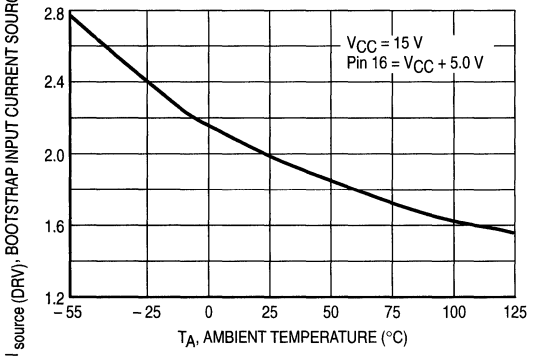


Figure 6. Bootstrap Input Zener Clamp Voltage versus Temperature

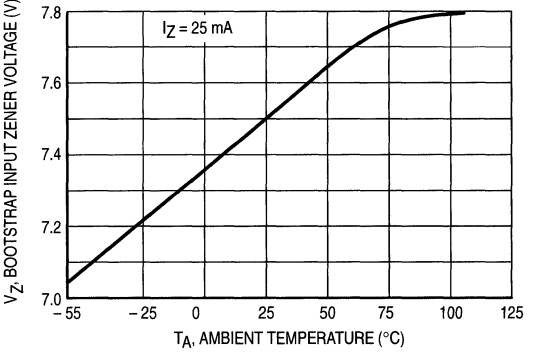


Figure 7. Output Switch Source Saturation versus Emitter Current

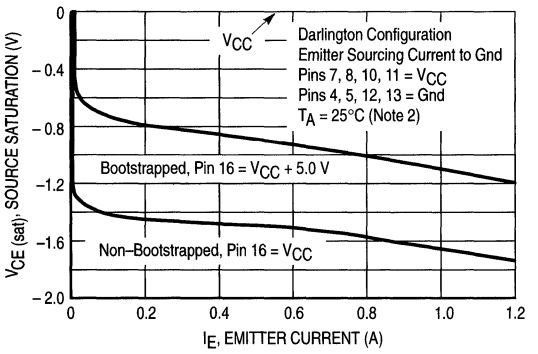


Figure 8. Output Switch Sink Saturation versus Collector Current

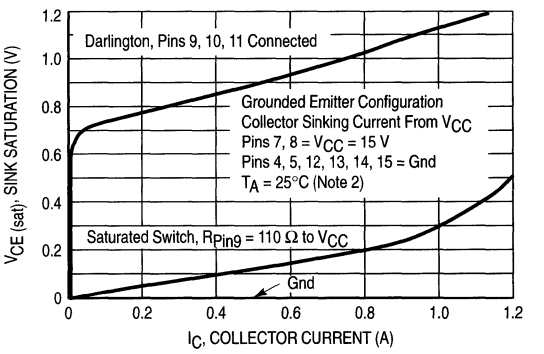


Figure 9. Output Switch Negative Emitter Voltage versus Temperature

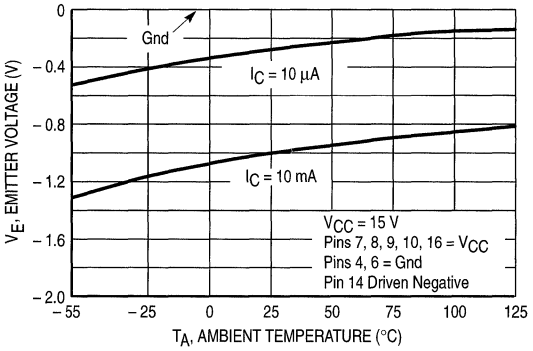


Figure 10. Low Voltage Indicator Output Sink Saturation Voltage versus Sink Current

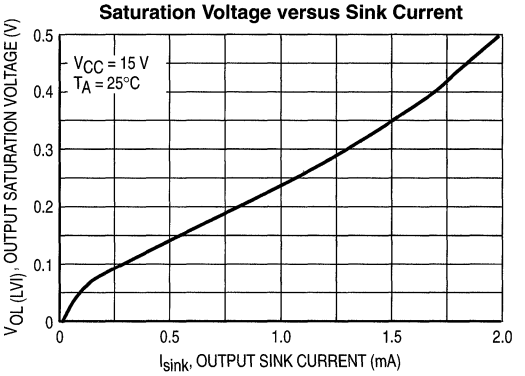


Figure 11. Current Limit Comparator Threshold Voltage versus Temperature

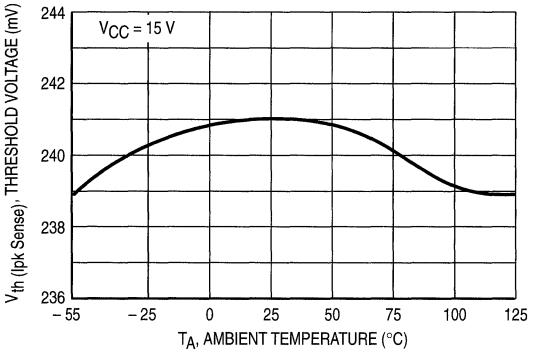


Figure 12. Current Limit Comparator Input Bias Current versus Temperature

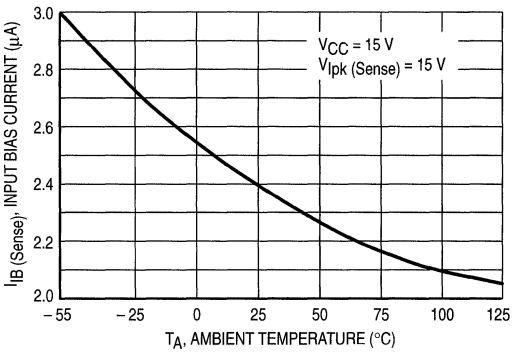


Figure 13. Standby Supply Current versus Supply Voltage

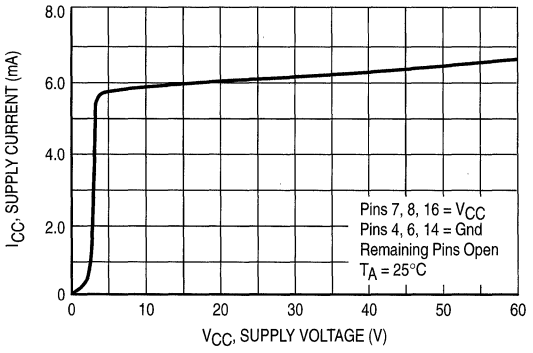


Figure 14. Standby Supply Current versus Temperature

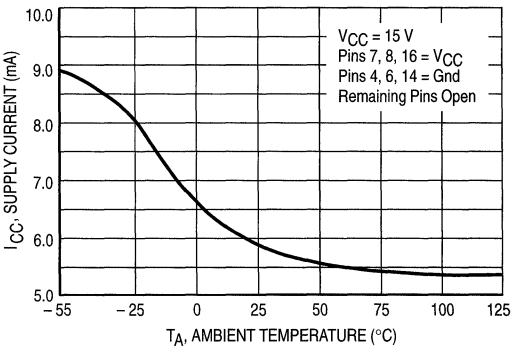


Figure 15. Minimum Operating Supply Voltage versus Temperature

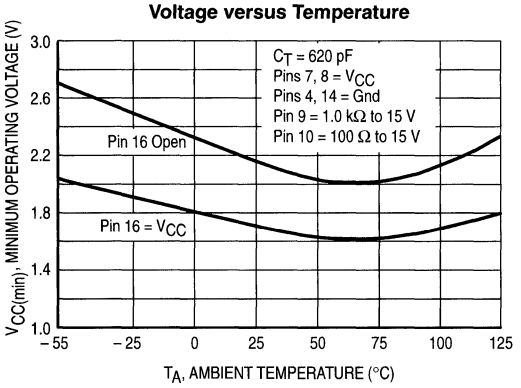


Figure 16. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

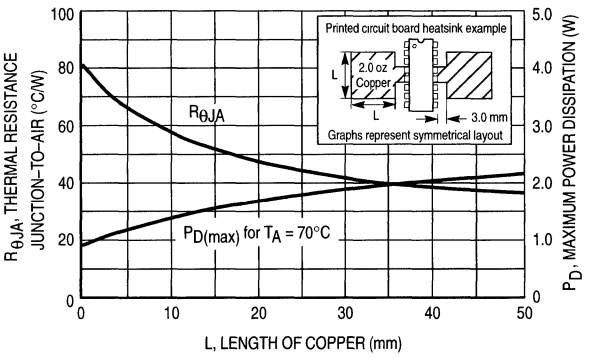
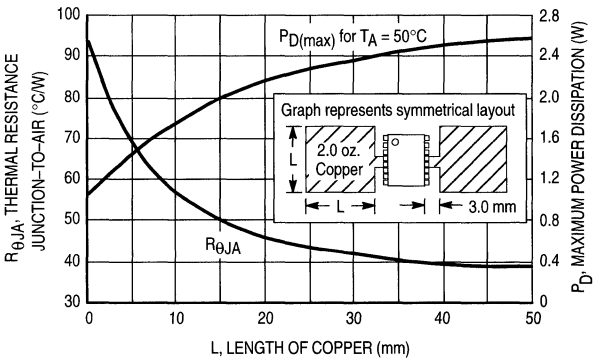


Figure 17. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



3

Figure 18. Representative Block Diagram

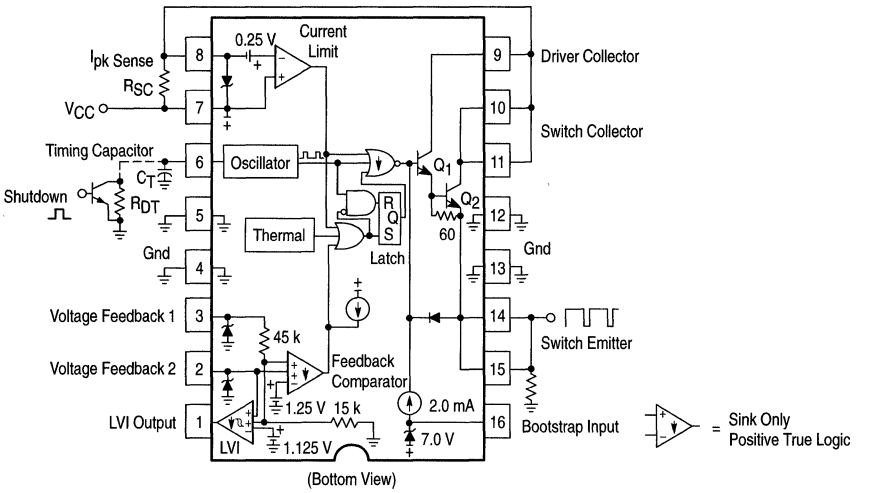
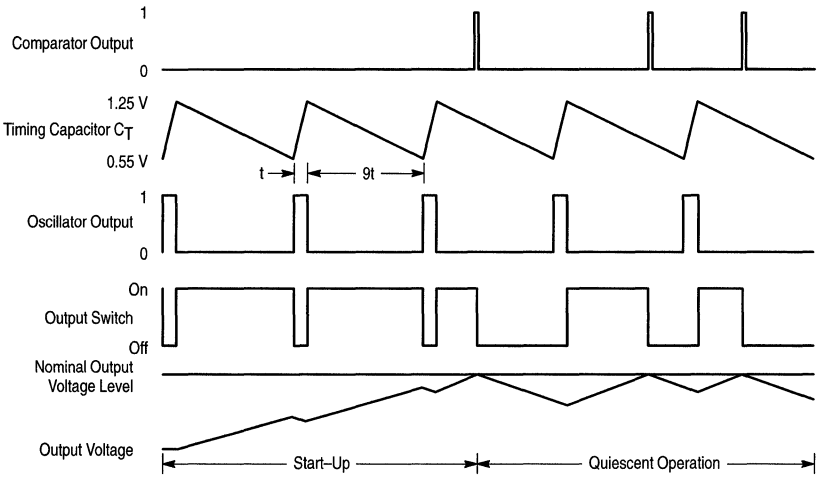


Figure 19. Typical Operating Waveforms



INTRODUCTION

The MC34165 series are monolithic power switching regulators optimized for DC–to–DC converter applications. The combination of features in this series enables the system designer to directly implement step–up, step–down, and voltage–inverting converters with a minimum number of external components. This series is constructed on a special high voltage process making it ideal for telecommunication applications. Other potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. The Representative Block Diagram is shown in Figure 18.

OPERATING DESCRIPTION

The MC34165 operates as a fixed on–time, variable off–time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 19. The output voltage waveform shown is for a step–down converter, with the ripple and phasing exaggerated for clarity. During initial converter start–up, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and on–time of the output switch are programmed by the value selected for timing capacitor C_T. Capacitor C_T is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As C_T charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp–up and can be enabled by the comparator output only at the start of ramp–down. The oscillator peak and valley thresholds are 1.25 V and 0.55 V, respectively, with a charge current of 225 μA and a discharge current of 25 μA, yielding a maximum on–time duty cycle of 90%. Since the MC34165 is a ripple mode regulator, the switch frequency will vary with line and load. The value selected for C_T will set the maximum switching frequency of the converter. A reduction of the maximum duty cycle may be required for specific converter configurations. This can be accomplished with the addition of an external dead–time resistor (R_{DT}) placed across C_T. The resistor increases the discharge current which reduces the on–time of the output switch. A graph of the Output Switch On–Off Time versus Oscillator Timing Capacitance for various values of R_{DT} is shown in Figure 1. Note that the maximum output duty cycle, $t_{on}/t_{on} + t_{off}$, remains constant for values of C_T greater than 0.2 nF. The converter output can be inhibited by clamping C_T to ground with an external NPN small–signal transistor.

Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25 V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is ±0.4 μA, which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0 V, the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05 V. The additional 50 mV compensates for a 1.0% voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's output state is controlled by the highest voltage applied to either of the two noninverting inputs.

The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor–based systems. The inverting input is internally biased at 1.125 V, which sets the noninverting input thresholds to 90% of nominal. The LVI comparator has 15 mV of hysteresis to prevent erratic reset operation. The open collector output is capable of sinking in excess of 1.5 mA (see Figure 10). An external resistor (R_{LVI}) and capacitor (C_{DLY}) can be used to program a reset delay time (t_{DLY}) by the formula shown below, where $V_{th(MPU)}$ is the microprocessor reset input threshold.

$$t_{DLY} = R_{LVI}\, C_{DLY}\, \ln\left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{out}}}\right)$$

Current Limit Comparator, Latch and Thermal Shutdown

With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

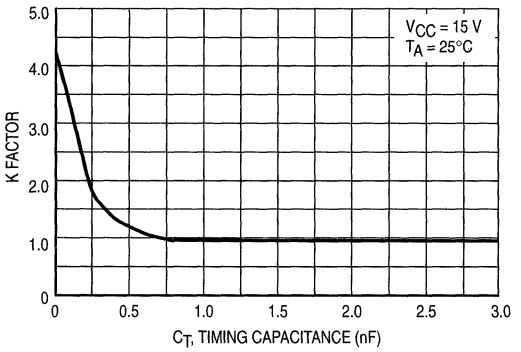
The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC}, in series with V_{CC} and output switch transistor Q_2. The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 250 mV with respect to V_{CC}, the comparator will set the latch and terminate output switch conduction on a cycle–by–cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on–time during a given oscillator cycle. The calculation for a value of R_{SC} is:

$$R_{SC} = \frac{0.25\ V \cdot K}{I_{pk(Switch)}}$$

The K factor was added to the previous equation in order to account for a 200 ns propagation delay that occurs from the Current Limit comparator input to the output switch. This propagation delay can cause the actual peak switch current to rise above the calculated peak switch current for small values of C_T. The following figure shows the relationship of the ratio $I_{pk(actual)}/I_{pk\ (Switch)}$, expressed as K versus C_T. Note the ratio rises above 1.0 for C_T values less than 1.0 nF.

3

Figure 20. K Factor versus Timing Capacitance



When analyzing a design, the actual short circuit current must be measured to verify that it is less than the maximum rating of the device.

Figures 11 and 12 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of 1.0 μA. The parasitic inductance associated with R_{SC} and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the Latch is forced into the "Set" state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch is designed to switch a maximum of 65 V collector to emitter, with up to 1.5 A peak collector current. The minimum value for R_{SC} is:

$$R_{SC(min)} = \frac{0.25\ V}{1.5\ A} = 0.166\ \Omega$$

When configured for step–down or voltage–inverting applications, as in Figures 20 and 24, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn–on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency.

Figure 9 shows that by clamping the emitter to less than 0.5 V, the collector current will be in the range 10 μA over temperature. A MBR160 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

A bootstrap input is provided to reduce the output switch saturation voltage in step–down and voltage–inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0 mA bias current source above V_{CC}. An internal zener limits the bootstrap input voltage to V_{CC} +7.0 V. The capacitor's equivalent series resistance may be large enough to limit the zener current to less than the maximum 100 mA rating. However, in most high voltage applications, an additional series resistor will probably be required. It is recommended that this resistor limit the zener current to approximately 25 mA for optimal performance. The circuit can be optimized by adjusting the zener current (R_B) during operation, while observing the circuit's efficiency. The value of the series resistor can be calculated as follows:

$$R_B \approx \frac{V_{in(max)}}{I_Z}$$

The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$C_{B(min)} = I\frac{\Delta t}{\Delta V} = 4.0\ mA\frac{t_{on}}{4.0\ V} = 0.001\ t_{on}$$

Parametric operation of the MC34165 is guaranteed over a supply voltage range of 3.0 V to 65 V. When operating below 3.0 V, the Bootstrap Input should be connected to V_{CC}. Figure 15 shows that non–parametric operation down to 1.7 V at room temperature is possible.

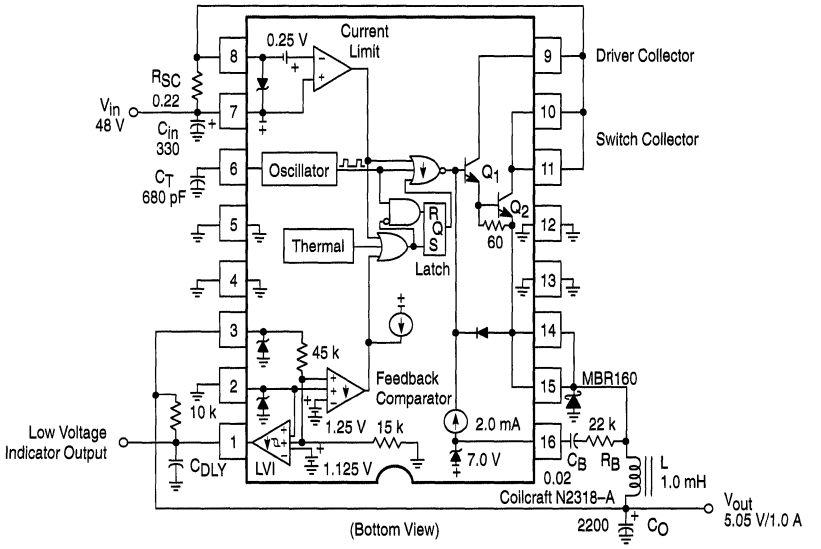
Package

The MC34165 is contained in a heatsinkable 16–lead plastic dual–in–line power package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 16 and 17 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction–to–air thermal resistance. These examples are for a symmetrical layout on a single–sided board with two ounce per square foot of copper.

APPLICATIONS

The following converter applications show the simplicity and flexibility of this circuit architecture. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

Figure 21. Step–Down Converter



Test	Condition	Results
Line Regulation	V_{in} = 12 V to 56 V, I_O = 1.0 A	9.0 mV = ± 0.049%
Load Regulation	V_{in} = 48 V, I_O = 0.1 A to 1.0 A	9.0 mV = ± 0.049%
Output Ripple	V_{in} = 48 V, I_O = 1.0 A	20 mVp–p
Short Circuit Current	V_{in} = 48 V, R_L = 0.1 Ω	1.23 A
Efficiency, Without Bootstrap	V_{in} = 48 V, I_O = 1.0 A	74.9%
Efficiency, With Bootstrap	V_{in} = 48 V, I_O = 1.0 A	75.5%

L = 65 turns of # 18 AWG on Magenetics Inc. 55345–A2 core.

Figure 22. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 1.5 A

Figure 22A. External NPN Switch

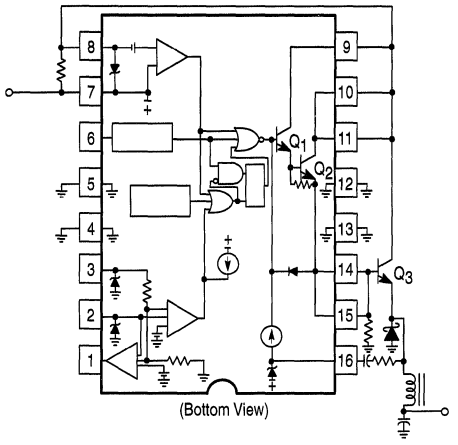
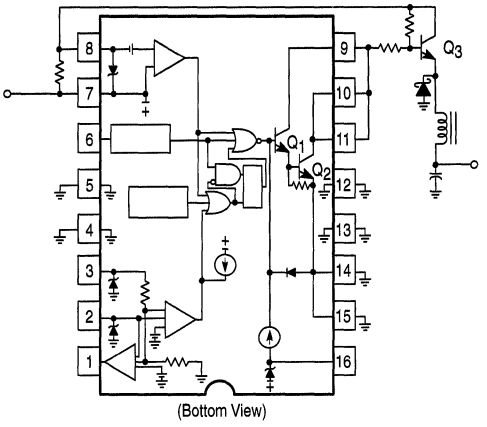
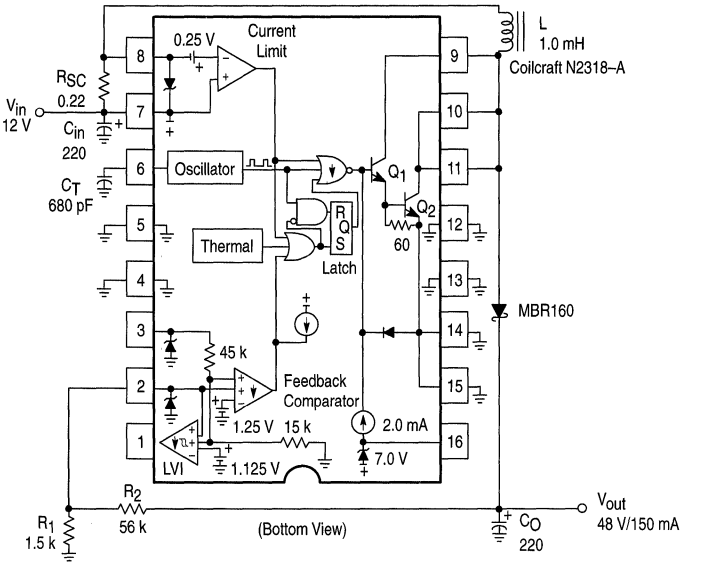


Figure 22B. External PNP Saturated Switch



3

Figure 23. Step–Up Converter



Test	Condition	Results
Line Regulation	V_{in} = 10 V to 20 V, I_O = 150 mA	11 mV = ± 0.11%
Load Regulation	V_{in} = 12 V, I_O = 15 mA to 150 mA	9.0 mV = ± 0.09%
Output Ripple	V_{in} = 12 V, I_O = 150 mA	125 mVp–p
Efficiency	V_{in} = 12 V, I_O = 150 mA	85.8%

L = 65 turns of # 18 AWG on Magenetics Inc. 55345–A2 core.

Figure 24. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 1.5 A

Figure 24A. External NPN Switch

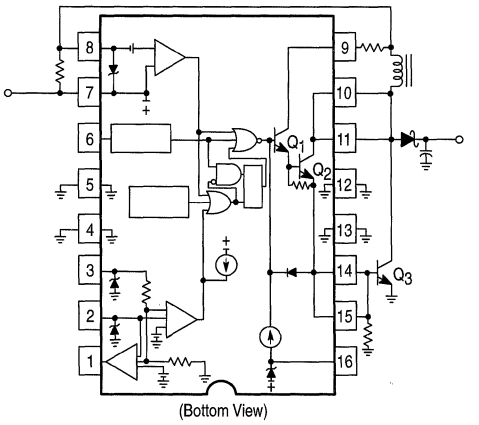


Figure 24B. External NPN Saturated Switch

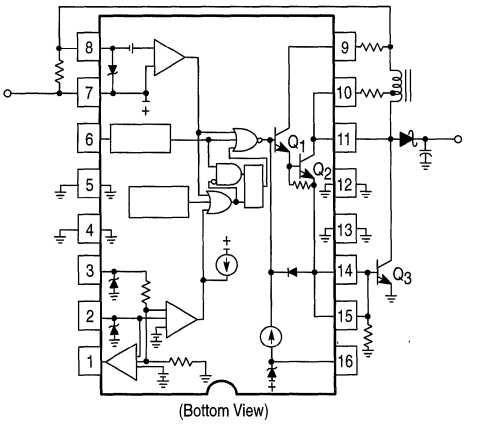
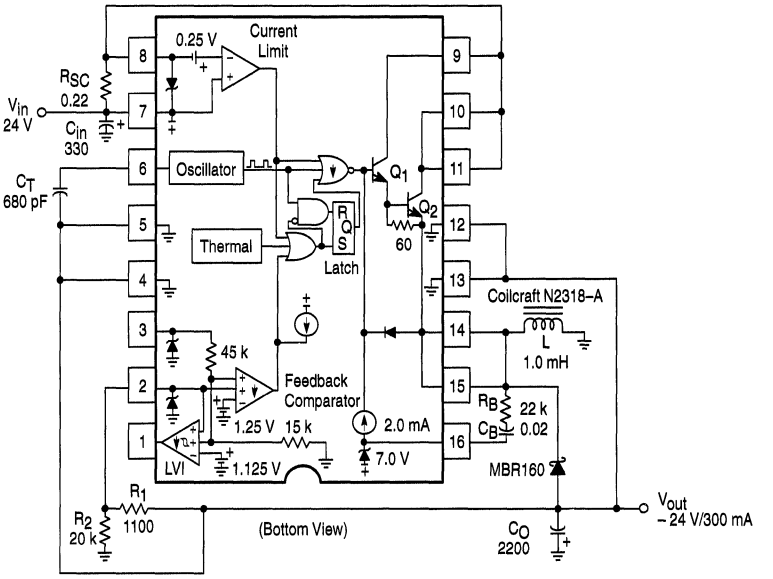


Figure 25. Voltage–Inverting Converter



Test	Condition	Results
Line Regulation	V_{in} = 15 V to 30 V, I_O = 300 mA	3.0 mV = ± 0.06%
Load Regulation	V_{in} = 24 V, I_O = 30 mA to 300 mA	1.0 mV = ± 0.02%
Output Ripple	V_{in} = 24 V, I_O = 300 mA	50 mVp–p
Short Circuit Current	V_{in} = 24 V, R_L = 0.1 Ω	1.12 A
Efficiency, Without Bootstrap	V_{in} = 24 V, I_O = 300 mA	81.3%
Efficiency, With Bootstrap	V_{in} = 24 V, I_O = 300 mA	82.7%

L = 65 turns of # 18 AWG on Magenetics Inc. 55345–A2 core.

Figure 26. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 1.5 A

Figure 26A. External NPN Switch

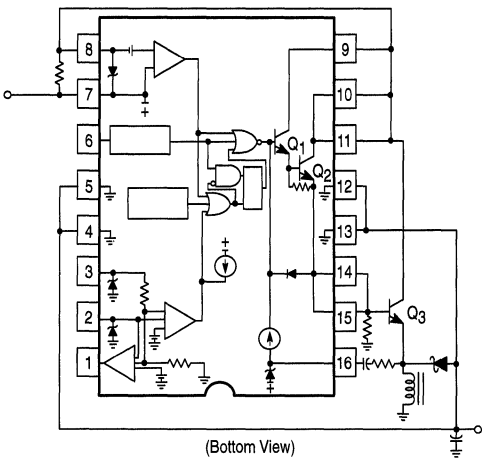


Figure 26B. External PNP Saturated Switch

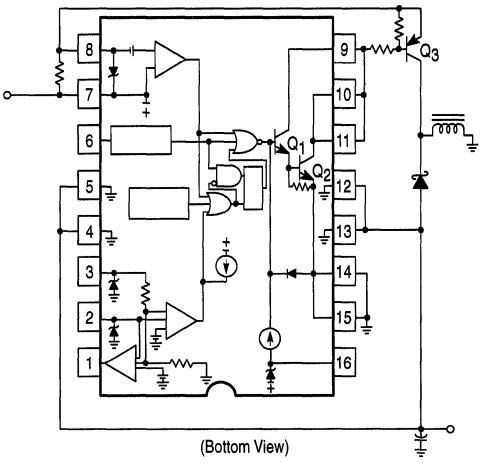
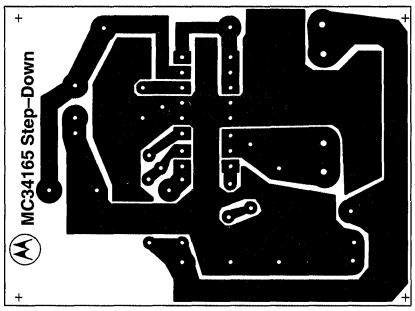
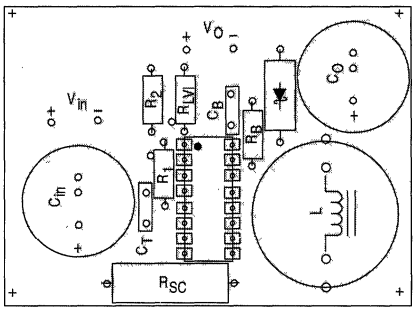


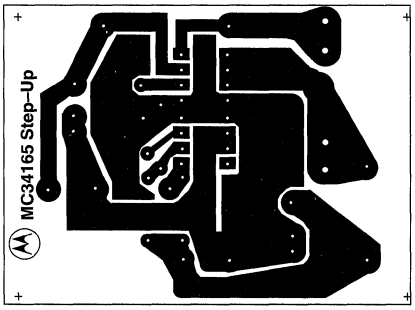
Figure 27. Printed Circuit Board and Component Layout (Circuits of Figures 21, 23, 25)



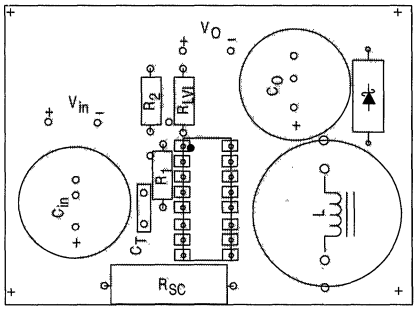
Bottom View



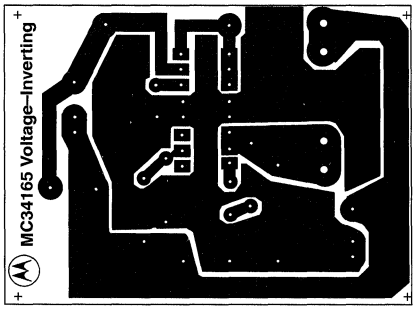
Top View



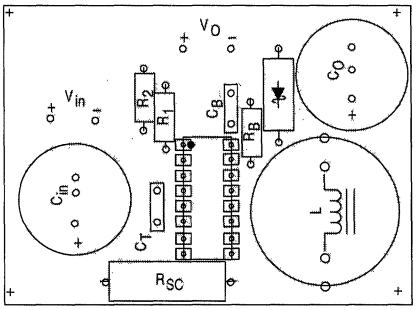
Bottom View



Top View



Bottom View



Top View

All printed circuit boards are 2.58" in width by 1.9" in height.

Table 1. Design Equations

Calculation	Step–Down	Step–Up	Voltage–Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2, 3)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$
C_T	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$
$I_{L(avg)}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
I_{pk} (Switch)	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.25 \cdot K}{I_{pk}\text{ (Switch)}}$	$\frac{0.25 \cdot K}{I_{pk}\text{ (Switch)}}$	$\frac{0.25 \cdot K}{I_{pk}\text{ (Switch)}}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$
$V_{ripple(p-p)}$	$\Delta I_L \sqrt{\left(\frac{1}{8f\,C_O}\right)^2 + (ESR)^2}$	$\approx \frac{t_{on}\, I_{out}}{C_O}$	$\approx \frac{t_{on}\, I_{out}}{C_O}$
V_{out}	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$

The following Converter Characteristics must be chosen:

- V_{in} – Nominal operating input voltage.
- V_{out} – Desired output voltage.
- I_{out} – Desired output current.
- ΔI_L – Desired peak–to–peak inductor ripple current. For maximum output current, it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent I_{pk} (Switch) from reaching the current threshold set by R_{SC}. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.
- f – Maximum output switch frequency.
- $V_{ripple(p-p)}$ – Desired peak–to–peak output ripple voltage. For best performance, the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.
- K – Multiplier number as determined by Figure 20, for determining the appropriate value for R_{SC}.

NOTES: 1. V_{sat} – Saturation voltage of the output switch, refer to Figures 7 and 8.

2. V_F – Output rectifier forward voltage drop. Typical value for MBR160 Schottky barrier rectifier is 0.6 V.

3. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8, at the minimum operating input voltage.

MC34166
MC33166

Power Switching Regulators

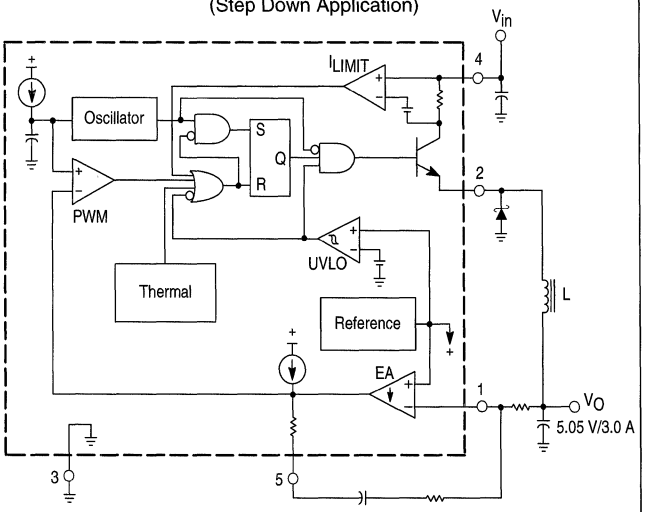
The MC34166, MC33166 series are high performance fixed frequency power switching regulators that contain the primary functions required for dc–to–dc converters. This series was specifically designed to be incorporated in step–down and voltage–inverting configurations with a minimum number of external components and can also be used cost effectively in step–up applications.

These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on–chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Protective features consist of cycle–by–cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36 μA.

- Output Switch Current in Excess of 3.0 A
- Fixed Frequency Oscillator (72 kHz) with On–Chip Timing
- Provides 5.05 V Output without External Resistor Divider
- Precision 2% Reference
- 0% to 95% Output Duty Cycle
- Cycle–by–Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5 V to 40 V
- Standby Mode Reduces Power Supply Current to 36 μA
- Economical 5–Lead TO–220 Package with Two Optional Leadforms
- Also Available in Surface Mount D^2PAK Package

Simplified Block Diagram
(Step Down Application)

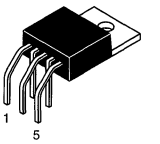


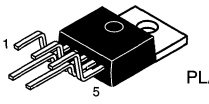
This device contains 143 active transistors.

POWER SWITCHING REGULATORS

SEMICONDUCTOR TECHNICAL DATA

TH SUFFIX
PLASTIC PACKAGE
CASE 314A

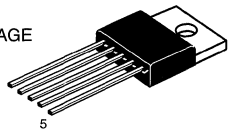




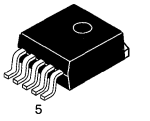
TV SUFFIX
PLASTIC PACKAGE
CASE 314B

Heatsink surface connected to Pin 3.

T SUFFIX
PLASTIC PACKAGE
CASE 314D



Pin 1. Voltage Feedback Input
2. Switch Output
3. Ground
4. Input Voltage/V_{CC}
5. Compensation/Standby



D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^2PAK)

Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33166D2T	T_A = – 40° to + 85°C	Surface Mount
MC33166T		Straight Lead
MC33166TH		Horiz. Mount
MC33166TV		Vertical Mount
MC34166D2T	T_A = 0° to + 70°C	Surface Mount
MC34166T		Straight Lead
MC34166TH		Horiz. Mount
MC34166TV		Vertical Mount

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	40	V
Switch Output Voltage Range	$V_{O(switch)}$	−1.5 to + V_{in}	V
Voltage Feedback and Compensation Input Voltage Range	V_{FB}, V_{Comp}	−1.0 to + 7.0	V
Power Dissipation			
Case 314A, 314B and 314D (T_A = +25°C)	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	65	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Case 936A (D^2PAK) (T_A = +25°C)	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	70	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3)	T_A		°C
MC34166		0 to + 70	
MC33166		− 40 to + 85	
Storage Temperature Range	T_{stg}	− 65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2, 3], unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OSCILLATOR						
Frequency (V_{CC} = 7.5 V to 40 V)	T_A = +25°C	f_{OSC}	65	72	79	kHz
	T_A = T_{low} to T_{high}		62	–	81	
ERROR AMPLIFIER						
Voltage Feedback Input Threshold	T_A = +25°C	$V_{FB(th)}$	4.95	5.05	5.15	V
	T_A = T_{low} to T_{high}		4.85	–	5.2	
Line Regulation (V_{CC} = 7.5 V to 40 V, T_A = +25°C)		Reg_{line}	–	0.03	0.078	%/V
Input Bias Current (V_{FB} = $V_{FB(th)}$ + 0.15 V)		I_{IB}	–	0.15	1.0	µA
Power Supply Rejection Ratio (V_{CC} = 10 V to 20 V, f = 120 Hz)		PSRR	60	80	–	dB
Output Voltage Swing						V
High State (I_{Source} = 75 µA, V_{FB} = 4.5 V)		V_{OH}	4.2	4.9	–	
Low State (I_{Sink} = 0.4 mA, V_{FB} = 5.5 V)		V_{OL}	–	1.6	1.9	
PWM COMPARATOR						
Duty Cycle						%
Maximum (V_{FB} = 0 V)		$DC_{(max)}$	92	95	100	
Minimum (V_{Comp} = 1.9 V)		$DC_{(min)}$	0	0	0	
SWITCH OUTPUT						
Output Voltage Source Saturation (V_{CC} = 7.5 V, I_{Source} = 3.0 A)		V_{sat}	–	(V_{CC} –1.5)	(V_{CC} –1.8)	V
Off–State Leakage (V_{CC} = 40 V, Pin 2 = Gnd)		$I_{sw(off)}$	–	0	100	µA
Current Limit Threshold		$I_{pk(switch)}$	3.3	4.3	6.0	A
Switching Times (V_{CC} = 40 V, I_{pk} = 3.0 A, L = 375 µH, T_A = +25°C)						ns
Output Voltage Rise Time		t_r	–	100	200	
Output Voltage Fall Time		t_f	–	50	100	
UNDERVOLTAGE LOCKOUT						
Startup Threshold (V_{CC} Increasing, T_A = +25°C)		$V_{th(UVLO)}$	5.5	5.9	6.3	V
Hysteresis (V_{CC} Decreasing, T_A = +25°C)		$V_{H(UVLO)}$	0.6	0.9	1.2	V
TOTAL DEVICE						
Power Supply Current (T_A = +25°C)		I_{CC}				
Standby (V_{CC} = 12 V, V_{Comp} < 0.15 V)			–	36	100	µA
Operating (V_{CC} = 40 V, Pin 1 = Gnd for maximum duty cycle)			–	31	55	mA

NOTES: 1. Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34166 T_{high} = + 70°C for MC34166
= – 40°C for MC33166 = + 85°C for MC33166

Figure 1. Voltage Feedback Input Threshold versus Temperature

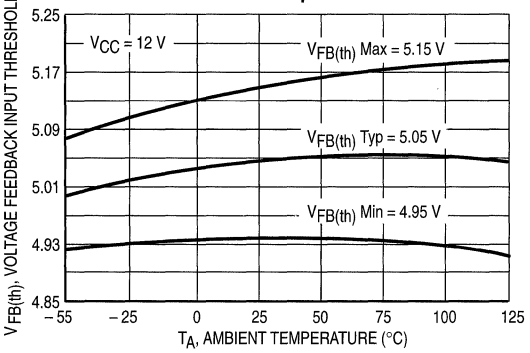


Figure 2. Voltage Feedback Input Bias Current versus Temperature

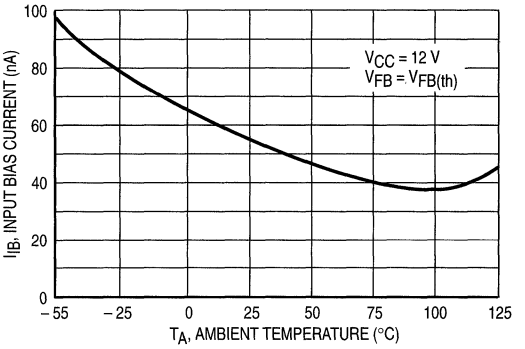


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

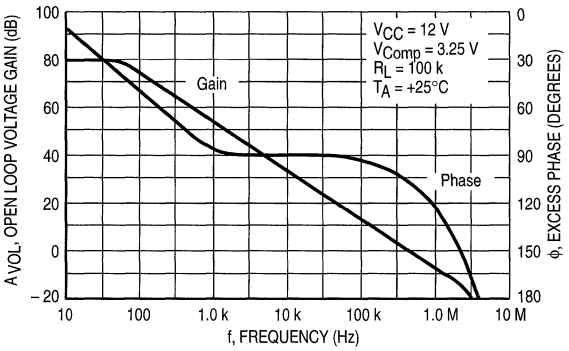


Figure 4. Error Amp Output Saturation versus Sink Current

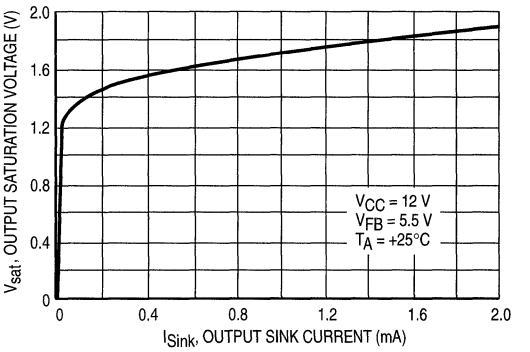


Figure 5. Oscillator Frequency Change versus Temperature

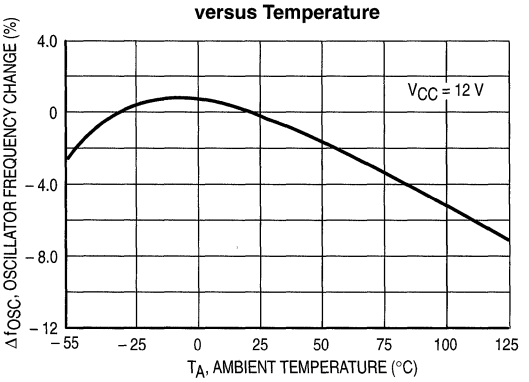


Figure 6. Switch Output Duty Cycle versus Compensation Voltage

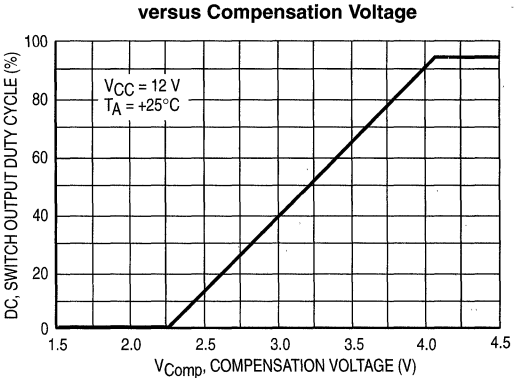


Figure 7. Switch Output Source Saturation versus Source Current

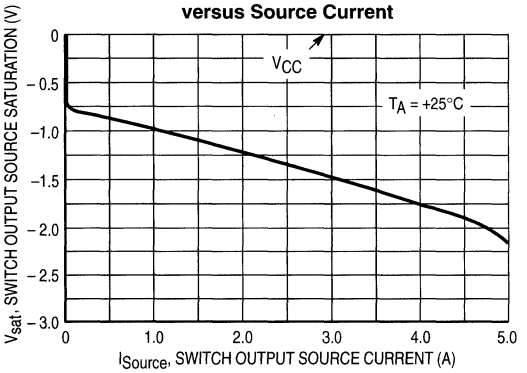


Figure 8. Negative Switch Output Voltage versus Temperature

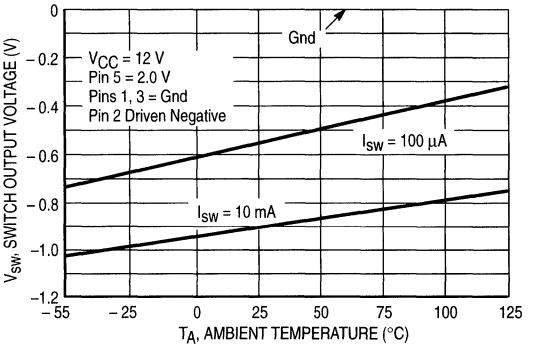


Figure 9. Switch Output Current Limit Threshold versus Temperature

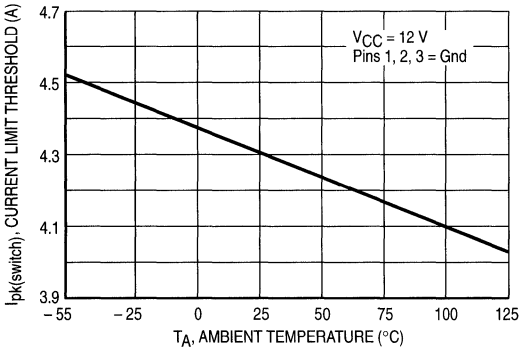


Figure 10. Standby Supply Current versus Supply Voltage

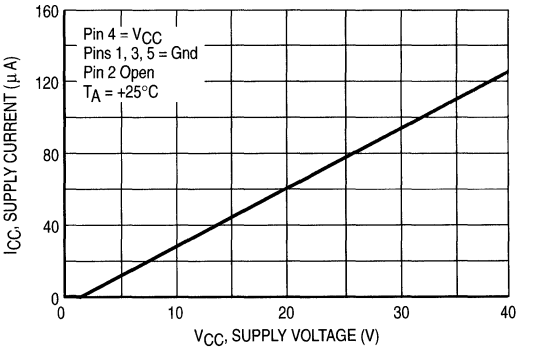


Figure 11. Undervoltage Lockout Threshold versus Temperature

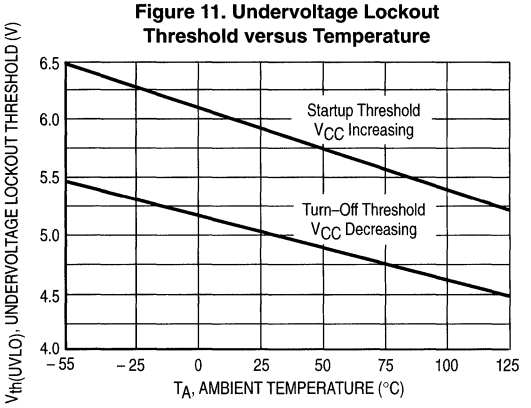


Figure 12. Operating Supply Current versus Supply Voltage

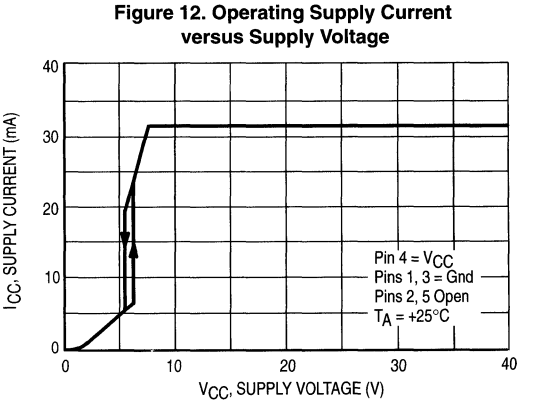


Figure 13. MC34166 Representative Block Diagram

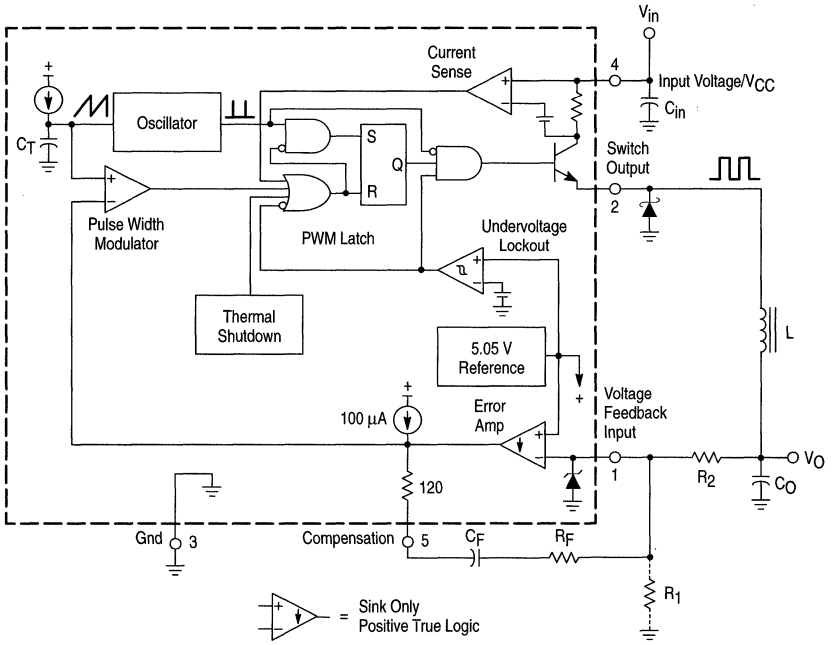
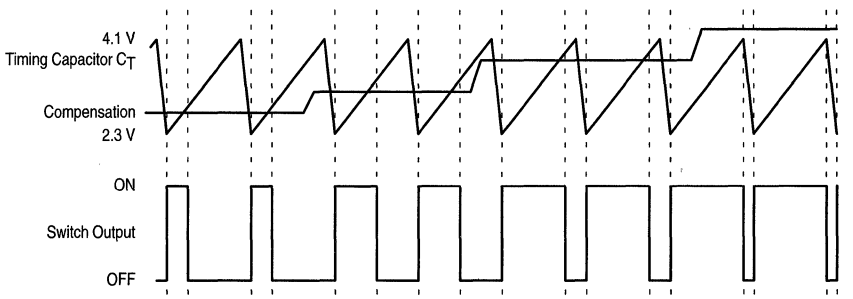


Figure 14. Timing Diagram



INTRODUCTION

The MC34166, MC33166 series are monolithic power switching regulators that are optimized for dc–to–dc converter applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step–down and voltage–inverting converters with a minimum number of external components. They can also be used cost effectively in step–up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 13.

Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor C_T and a trimmed current source. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the Switch Output. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1 V and 2.3 V respectively.

Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when C_T is discharged to the oscillator valley voltage. As C_T charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp–up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 6 and 14 illustrate the switch output duty cycle versus the compensation voltage.

Current Sense

The MC34166 series utilizes cycle–by–cycle current limiting as a means of protecting the output switch transistor from overstress. Each on–cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp–up period.

The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch. The current limit threshold is typically set at 4.3 A. Figure 9 illustrates switch output current limit threshold versus temperature.

Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical dc voltage gain of 80 dB, and a unity gain bandwidth of 600 kHz with 70 degrees of phase margin (Figure 3). The noninverting input is biased to the internal 5.05 V reference and is not pinned out. The reference has an accuracy of ± 2.0% at room temperature. To provide 5.0 V at the load, the reference is programmed 50 mV above 5.0 V to compensate for a 1.0% voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input as shown in Figures 13 and 18. The equation for determining the output voltage with the divider network is:

$$V_{out} = 5.05 \left(\frac{R_2}{R_1} + 1\right)$$

External loop compensation is required for converter stability. A simple low–pass filter is formed by connecting a resistor (R_2) from the regulated output to the inverting input, and a series resistor–capacitor (R_F, C_F) between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step–down converter (Figure 18) is the easiest to compensate for stability. The step–up (Figure 20) and voltage–inverting (Figure 22) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting R_F and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150 mV, the internal circuitry will be placed into a low power standby mode, reducing the power supply current to 36 μA with a 12 V supply voltage. Figure 10 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a 100 μA current source pull–up that can be used to implement soft–start. Figure 17 shows the current source charging capacitor C_{SS} through a series diode. The diode disconnects C_{SS} from the feedback loop when the 1.0 M resistor charges it above the operating range of Pin 5.

Switch Output

The output transistor is designed to switch a maximum of 40 V, with a minimum peak collector current of 3.3 A. When configured for step–down or voltage–inverting applications, as in Figures 18 and 22, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn–on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 8 shows that by clamping the emitter to 0.5 V, the collector current will be in the range of 100 μA over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully functional before the output stage is enabled. The internal 5.05 V reference is monitored by the comparator which enables the output stage when V_{CC} exceeds 5.9 V. To prevent erratic output switching as the threshold is crossed, 0.9 V of hysteresis is provided.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the latch is forced into a 'reset' state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.** The MC34166 is contained in a 5–lead TO–220 type package. The tab of the package is common with the center pin (Pin 3) and is normally connected to ground.

3

DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire–wrap or plug–in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a tight component layout is recommended. Capacitors C_{IN}, C_O, and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

Figure 15. Low Power Standby Circuit

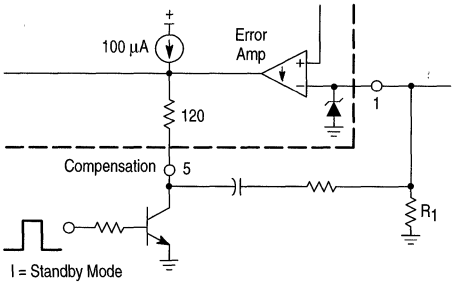
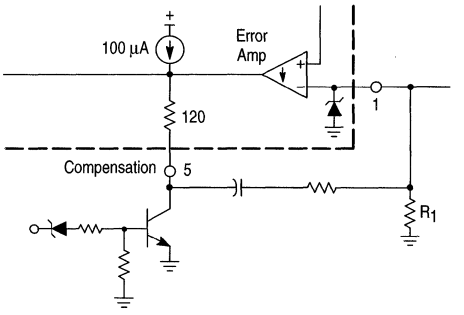
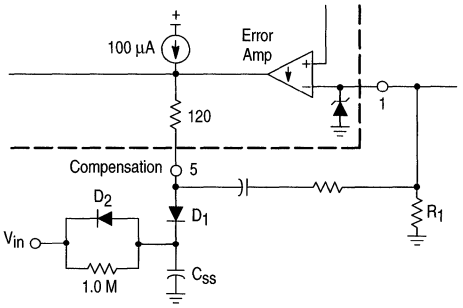


Figure 16. Over Voltage Shutdown Circuit



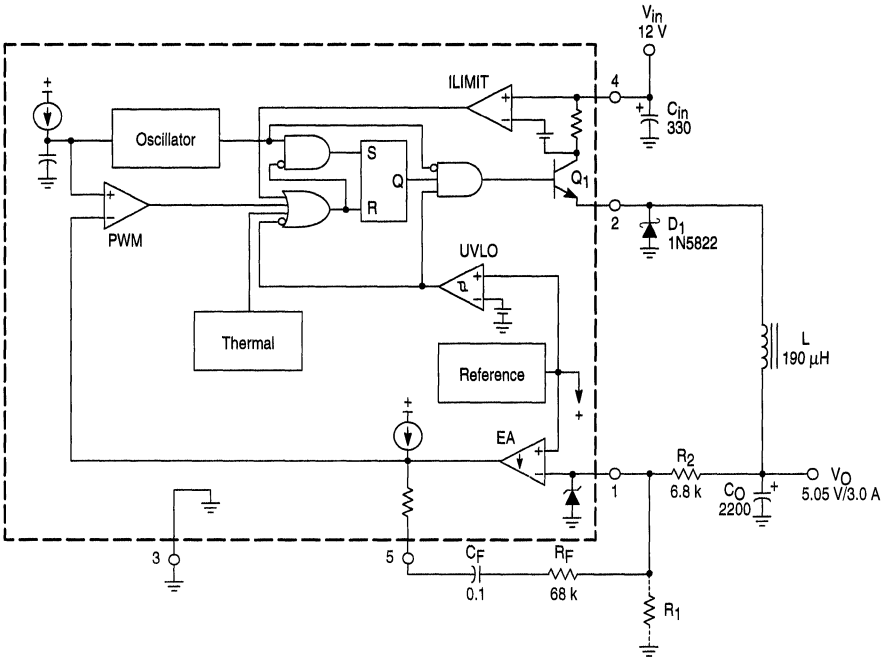
$V_{Shutdown} = V_{Zener} + 0.7$

Figure 17. Soft–Start Circuit



$t_{Soft-Start} \approx 35{,}000\ C_{SS}$

Figure 18. Step–Down Converter

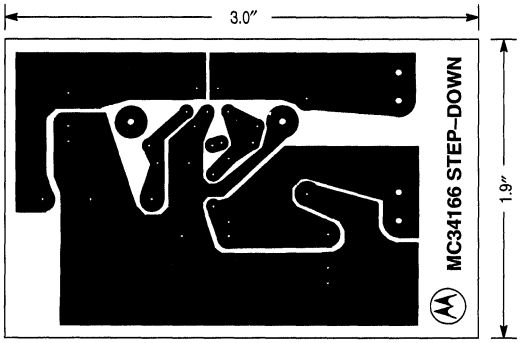


Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 36 V, I_O = 3.0 A	5.0 mV = ± 0.05%
Load Regulation	V_{in} = 12 V, I_O = 0.25 A to 3.0 A	2.0 mV = ± 0.02%
Output Ripple	V_{in} = 12 V, I_O = 3.0 A	10 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	4.3 A
Efficiency	V_{in} = 12 V, I_O = 3.0 A	82.8%

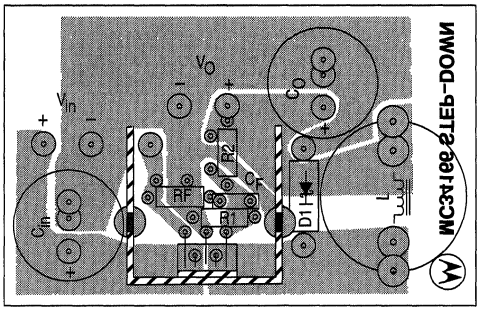
L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

The Step–Down Converter application is shown in Figure 18. The output switch transistor Q_1 interrupts the input voltage, generating a squarewave at the LC_O filter input. The filter averages the squarewaves, producing a dc output voltage that can be set to any level between V_{in} and V_{ref} by controlling the percent conduction time of Q_1 to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input.

Figure 19. Step–Down Converter Printed Circuit Board and Component Layout



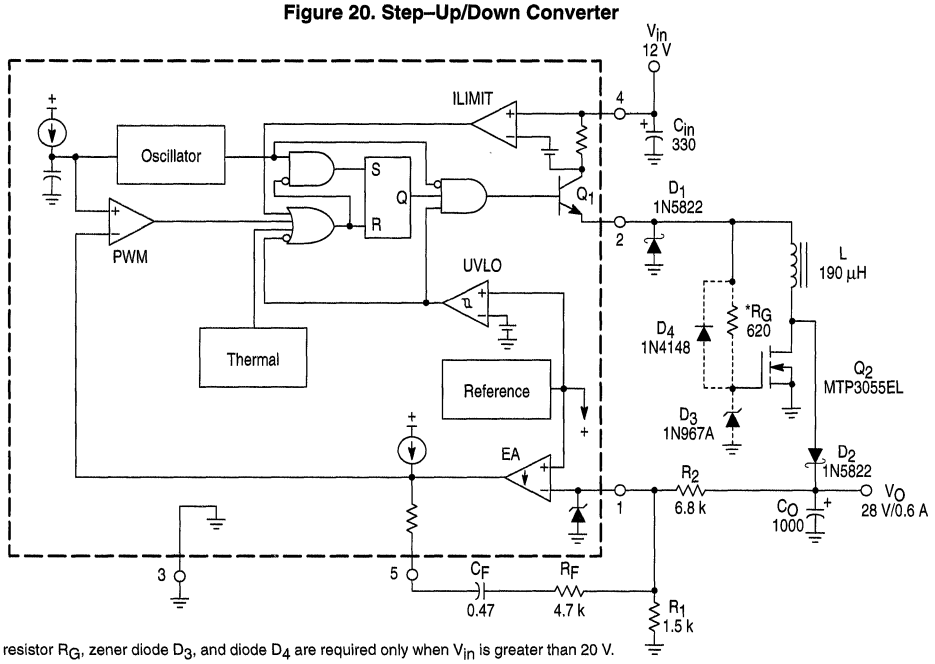
(Bottom View)



(Top View)

3

Figure 20. Step–Up/Down Converter



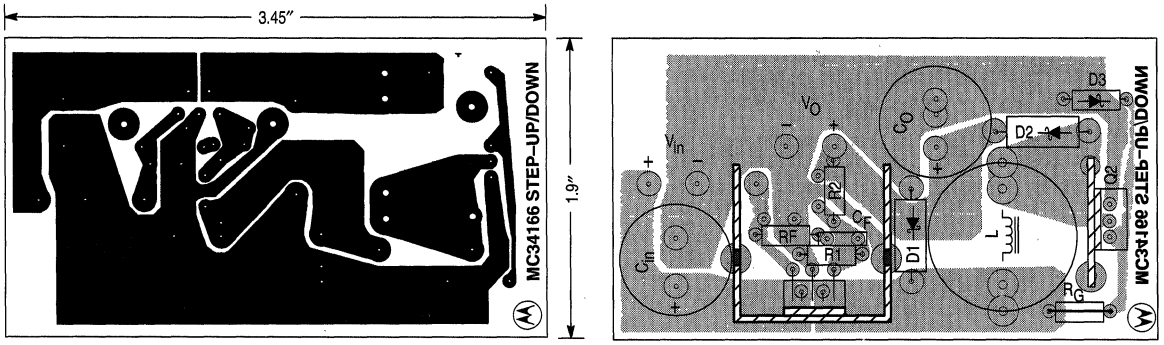
*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 24 V, I_O = 0.6 A	23 mV = ± 0.41%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 0.6 A	3.0 mV = ± 0.005%
Output Ripple	V_{in} = 12 V, I_O = 0.6 A	100 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	4.0 A
Efficiency	V_{in} = 12 V, I_O = 0.6 A	82.8%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core.
Heatsink = AAVID Engineering Inc.
MC34166: 5903B, or 5930B
MTP3055EL: 5925B

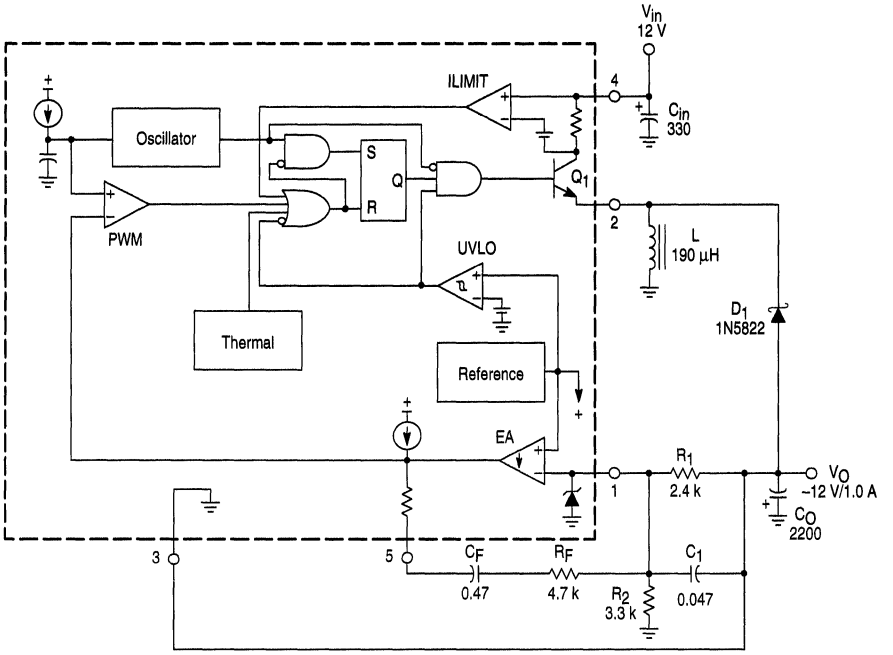
Figure 20 shows that the MC34166 can be configured as a step–up/down converter with the addition of an external power MOSFET. Energy is stored in the inductor during the on–time of transistors Q_1 and Q_2. During the off–time, the energy is transferred, with respect to ground, to the output filter capacitor and load. This circuit configuration has two significant advantages over the basic step–up converter circuit. The first advantage is that output short–circuit protection is provided by the MC34166, since Q_1 is directly in series with V_{in} and the load. Second, the output voltage can be programmed to be less than V_{in}. Notice that during the off–time, the inductor forward biases diodes D_1 and D_2, transferring its energy with respect to ground rather than with respect to V_{in}. When operating with V_{in} greater than 20 V, a gate protection network is required for the MOSFET. The network consists of components R_G, D_3, and D_4.

Figure 21. Step–Up/Down Converter Printed Circuit Board and Component Layout



(Bottom View) (Top View)

Figure 22. Voltage–Inverting Converter

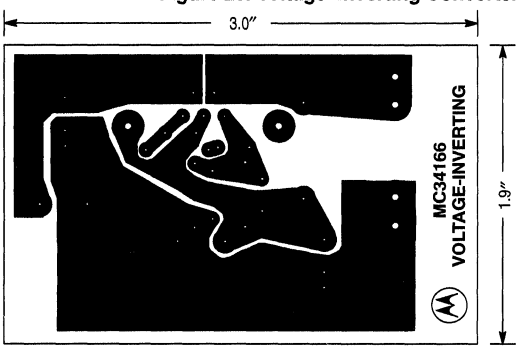


Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 24 V, I_O = 1.0 A	3.0 mV = ± 0.01%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 1.0 A	4.0 mV = ± 0.017%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	80 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	3.74 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	81.2%

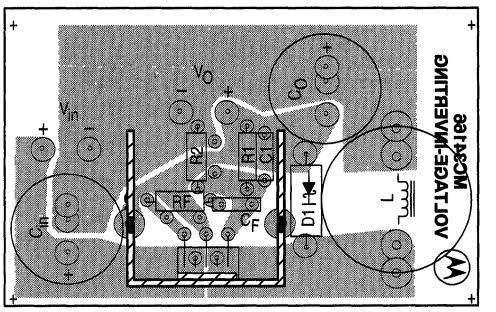
L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Two potential problems arise when designing the standard voltage–inverting converter with the MC34166. First, the Switch Output emitter is limited to –1.5 V with respect to the ground pin and second, the Error Amplifier's noninverting input is internally committed to the reference and is not pinned out. Both of these problems are resolved by connecting the IC ground pin to the converter's negative output as shown in Figure 22. This keeps the emitter of Q_1 positive with respect to the ground pin and has the effect of reversing the Error Amplifier inputs. Note that the voltage drop across R_1 is equal to 5.05 V when the output is in regulation.

Figure 23. Voltage–Inverting Converter Printed Circuit Board and Component Layout



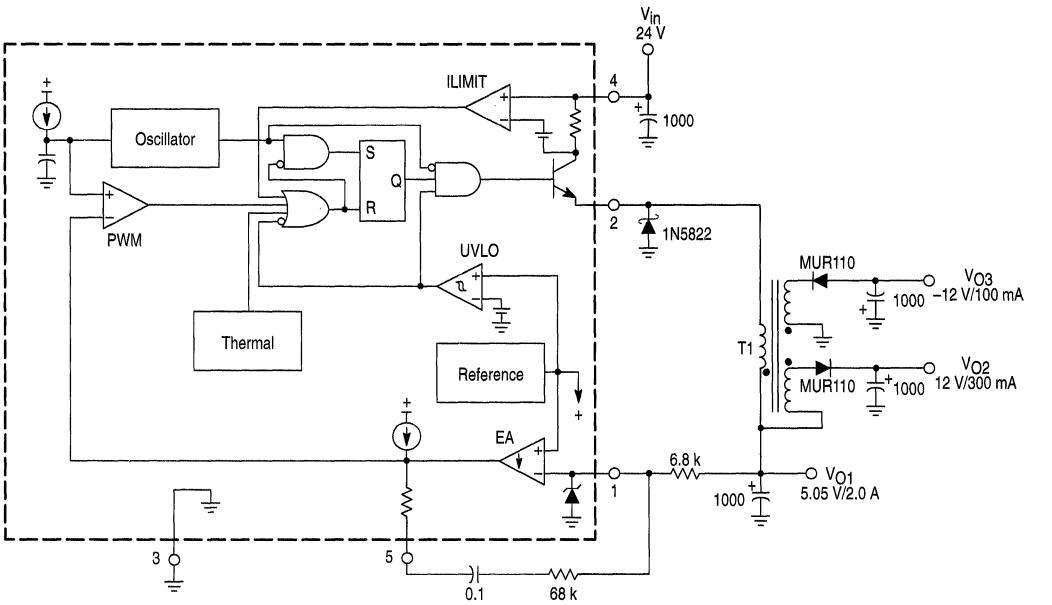
(Bottom View)



(Top View)

3

Figure 24. Triple Output Converter



Tests		Conditions	Results
Line Regulation	5.0 V 12 V −12 V	V_{in} = 15 V to 30 V, I_{O1} = 2.0 A, I_{O2} = 300 mA, I_{O3} = 100 mA	4.0 mV = ± 0.04% 450 mV = ±1.9% 350 mV = ±1.5%
Load Regulation	5.0 V 12 V −12 V	V_{in} = 24 V, I_{O1} = 500 mA to 2.0 A, I_{O2} = 300 mA, I_{O3} = 100 mA V_{in} = 24 V, I_{O1} = 2.0 A, I_{O2} = 100 mA to 300 mA, I_{O3} = 100 mA V_{in} = 24 V, I_{O1} = 2.0 A, I_{O2} = 300 mA, I_{O3} = 30 mA to 100 mA	2.0 mV = ± 0.02% 420 mV = ±1.7% 310 mV = ±1.3%
Output Ripple	5.0 V 12 V −12 V	V_{in} = 24 V, I_{O1} = 2.0 A, I_{O2} = 300 mA, I_{O3} = 100 mA	50 mV_{pp} 25 mV_{pp} 10 mV_{pp}
Short Circuit Current	5.0 V 12 V −12 V	V_{in} = 24 V, R_L = 0.1 Ω	4.3 A 1.83 A 1.47 A
Efficiency	TOTAL	V_{in} = 24 V, I_{O1} = 2.0 A, I_{O2} = 300 mA, I_{O3} = 100 mA	83.3%

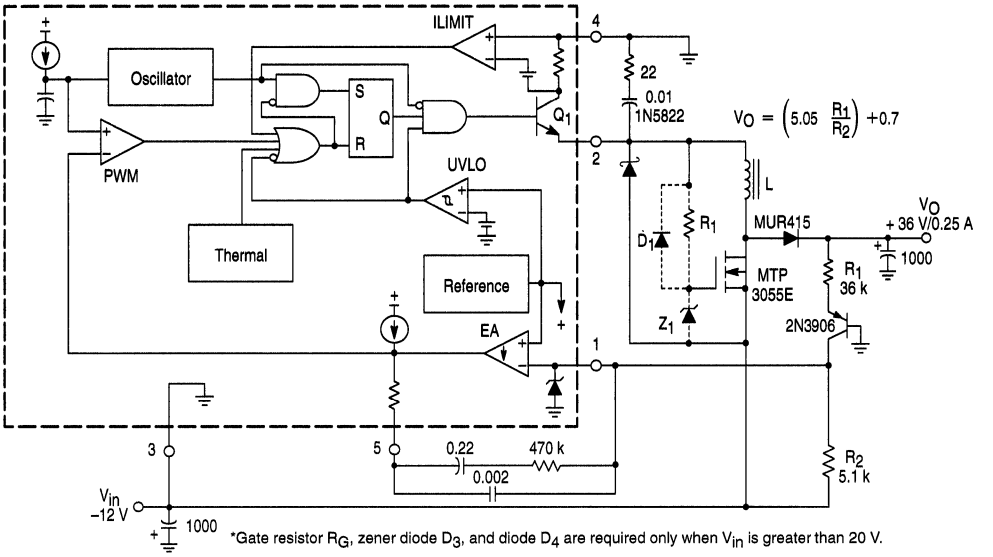
T1 = Primary: Coilcraft M1496-A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Secondary: V_{O2} — 65 turns of #26 AWG
V_{O3} — 96 turns of #28 AWG
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the OFF time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$\#\ TURNS_{(SEC)} = \frac{V_{O(SEC)} + V_{F(SEC)}}{\left(\frac{V_{O(PRI)} + V_{F(PRI)}}{\#TURNS_{(PRI)}}\right)}$$

Note that the 12 V winding is stacked on top of the 5.0 V output. This reduces the number of secondary turns and improves lead regulation. For best auxiliary regulation, the auxiliary outputs should be less than 33% of the total output power.

Figure 25. Negative Input/Positive Output Regulator

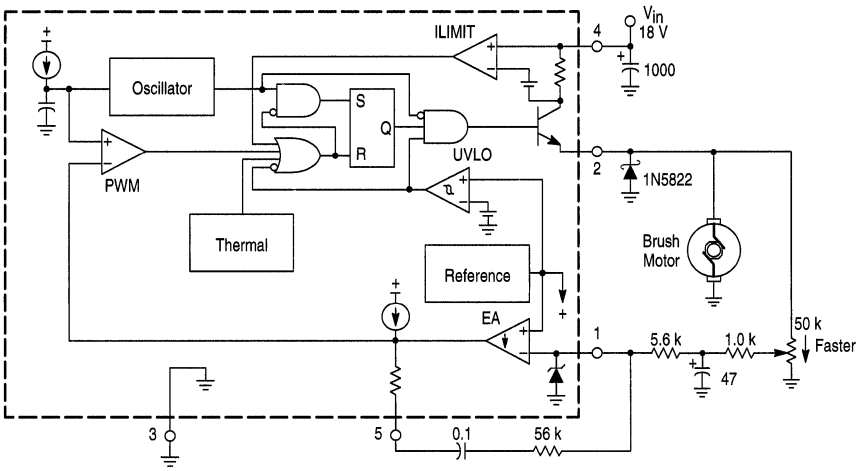


*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Conditions	Results
Line Regulation	V_{in} = −10 V to − 20 V, I_O = 0.25 A	250 mV = ± 0.35%
Load Regulation	V_{in} = −12 V, I_O = 0.025 A to 0.25 A	790 mV = ±1.19%
Output Ripple	V_{in} = −12 V, I_O = 0.25 A	80 mV_{pp}
Efficiency	V_{in} = −12 V, I_O = 0.25 A	79.2%

L = Coilcraft M1496–A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core.
Heatsink = AAVID Engineering Inc. 5903B or 5930B

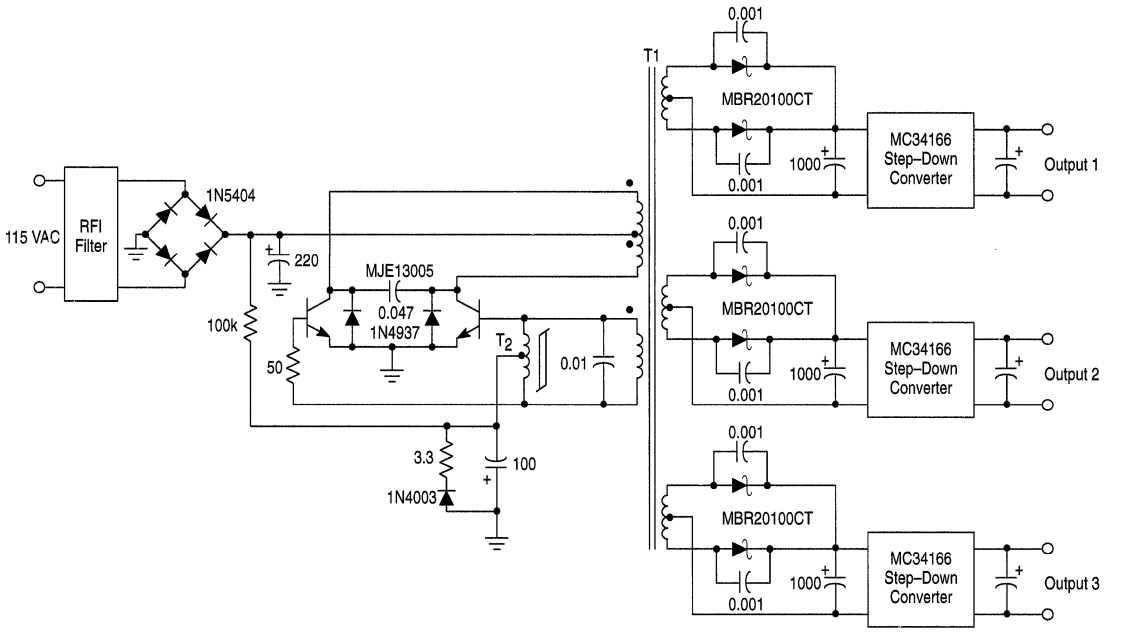
Figure 26. Variable Motor Speed Control with EMF Feedback Sensing



Test	Conditions	Results
Low Speed Line Regulation	V_{in} = 12 V to 24 V	1760 RPM ±1%
High Speed Line Regulation	V_{in} = 12 V to 24 V	3260 RPM ± 6%

3

Figure 27. Off–Line Preconverter



T_1 = Core and Bobbin – Coilcraft PT3595
Primary – 104 turns #26 AWG
Base Drive – 3 turns #26 AWG
Secondaries – 16 turns #16 AWG
Total Gap – 0.002″

T_2 = Core – TDK T6 x 1.5 x 3 H5C2
14 turns center tapped #30 AWG
Heatsink = AAVID Engineering Inc.
MC34166 and MJE13005 – 5903B
MBR20100CT – 5925B

The MC34166 can be used cost effectively in off–line applications even though it is limited to a maximum input voltage of 40 V. Figure 27 shows a simple and efficient method for converting the AC line voltage down to 24 V. This preconverter has a total power rating of 125 W with a conversion efficiency of 90%. Transformer T_1 provides output isolation from the AC line and isolation between each of the secondaries. The circuit self–oscillates at 50 kHz and is controlled by the saturation characteristics of T_2. Multiple MC34166 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

Figure 28. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

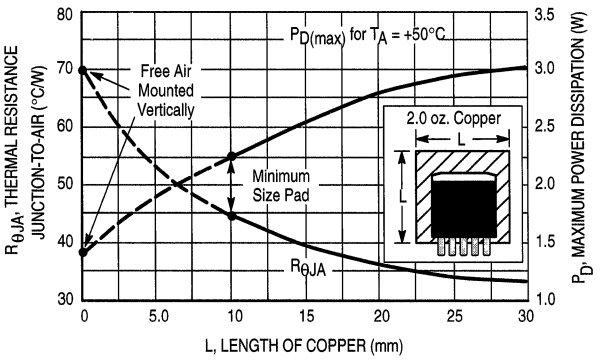


Table 1. Design Equations

Calculation	Step–Down	Step–Up/Down	Voltage–Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_{F1} + V_{F2}}{V_{in} - V_{satQ1} - V_{satQ2}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$
Duty Cycle (Note 3)	$t_{on}\, f_{osc}$	$t_{on}\, f_{osc}$	$t_{on}\, f_{osc}$
$I_{L\ avg}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk(switch)}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L}\right)t_{on}$	$\left(\frac{V_{in} - V_{satQ1} - V_{satQ2}}{\Delta I_L}\right)t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right)t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 f_{osc} C_o}\right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1\right)\sqrt{\left(\frac{1}{f_{osc} C_o}\right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1\right)\sqrt{\left(\frac{1}{f_{osc} C_o}\right)^2 + (ESR)^2}$
V_{out}	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$

NOTES: 1. V_{sat} – Switch Output source saturation voltage, refer to Figure 7.
2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5 V.
3. Duty cycle is calculated at the minimum operating input voltage and must not exceed the guaranteed minimum $DC_{(max)}$ specification of 0.92.

The following converter characteristics must be chosen:

V_{out} – Desired output voltage.

I_{out} – Desired output current.

ΔI_L – Desired peak–to–peak inductor ripple current. For maximum output current especially when the duty cycle is greater than 0.5, it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L\ avg}$. This will help prevent $I_{pk(switch)}$ from reaching the guaranteed minimum current limit threshold of 3.3 A. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2\ (I_{L\ avg})$. This will proportionally reduce the converter's output current capability.

$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. For best performance, the ripple voltage should be kept to less than 2% of V_{out}. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

MOTOROLA

Power Switching Regulators

3

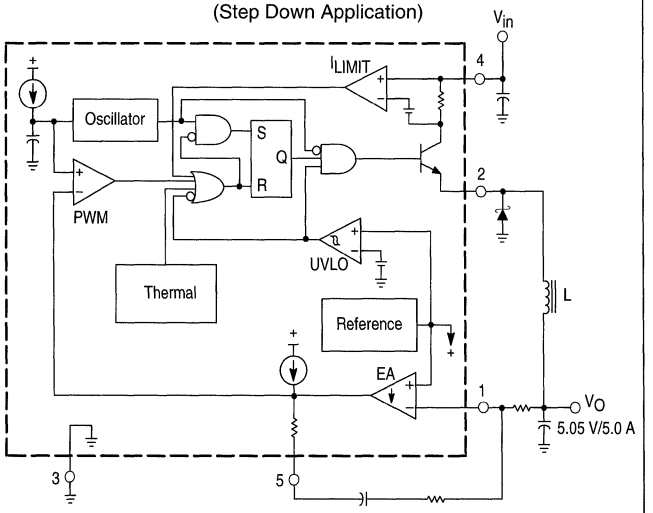
The MC34167, MC33167 series are high performance fixed frequency power switching regulators that contain the primary functions required for dc–to–dc converters. This series was specifically designed to be incorporated in step–down and voltage–inverting configurations with a minimum number of external components and can also be used cost effectively in step–up applications.

These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on–chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Protective features consist of cycle–by–cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36 μA.

- Output Switch Current in Excess of 5.0 A
- Fixed Frequency Oscillator (72 kHz) with On–Chip Timing
- Provides 5.05 V Output without External Resistor Divider
- Precision 2% Reference
- 0% to 95% Output Duty Cycle
- Cycle–by–Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5 V to 40 V
- Standby Mode Reduces Power Supply Current to 36 μA
- Economical 5–Lead TO–220 Package with Two Optional Leadforms
- Also Available in Surface Mount D^{2}PAK Package

Simplified Block Diagram
(Step Down Application)



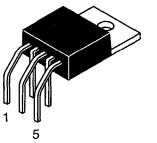
This device contains 143 active transistors.

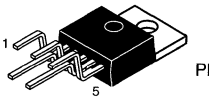
MC34167
MC33167

POWER SWITCHING REGULATORS

SEMICONDUCTOR TECHNICAL DATA

TH SUFFIX
PLASTIC PACKAGE
CASE 314A

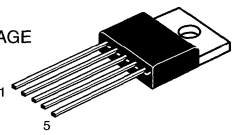




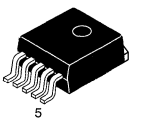
TV SUFFIX
PLASTIC PACKAGE
CASE 314B

Heatsink surface connected to Pin 3.

T SUFFIX
PLASTIC PACKAGE
CASE 314D



Pin 1. Voltage Feedback Input
2. Switch Output
3. Ground
4. Input Voltage/V_{CC}
5. Compensation/Standby



D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^{2}PAK)

Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33167D2T	T_A = −40° to +85°C	Surface Mount
MC33167T		Straight Lead
MC33167TH		Horiz. Mount
MC33167TV		Vertical Mount
MC34167D2T	T_A = 0° to + 70°C	Surface Mount
MC34167T		Straight Lead
MC34167TH		Horiz. Mount
MC34167TV		Vertical Mount

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	40	V
Switch Output Voltage Range	$V_{O(switch)}$	−2.0 to + V_{in}	V
Voltage Feedback and Compensation Input Voltage Range	V_{FB},V_{Comp}	−1.0 to + 7.0	V
Power Dissipation			
Case 314A, 314B and 314D (T_A = +25°C)	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	65	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Case 936A (D^2PAK) (T_A = +25°C)	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	70	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34167 MC33167	T_A	 0 to + 70 − 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2, 3], unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OSCILLATOR						
Frequency (V_{CC} = 7.5 V to 40 V)	T_A = +25°C T_A = T_{low} to T_{high}	f_{OSC}	65 62	72 –	79 81	kHz
ERROR AMPLIFIER						
Voltage Feedback Input Threshold	T_A =+ 25°C T_A = T_{low} to T_{high}	$V_{FB(th)}$	4.95 4.85	5.05 –	5.15 5.20	V
Line Regulation (V_{CC} = 7.5 V to 40 V, T_A = +25°C)		Reg_{line}	–	0.03	0.078	%/V
Input Bias Current (V_{FB} = $V_{FB(th)}$ + 0.15 V)		I_{IB}	–	0.15	1.0	µA
Power Supply Rejection Ratio (V_{CC} = 10 V to 20 V, f = 120 Hz)		PSRR	60	80	–	dB
Output Voltage Swing	High State (I_{Source} = 75 µA, V_{FB} = 4.5 V) Low State (I_{Sink} = 0.4 mA, V_{FB} = 5.5 V)	V_{OH} V_{OL}	4.2 –	4.9 1.6	– 1.9	V
PWM COMPARATOR						
Duty Cycle (V_{CC} = 20 V)	Maximum (V_{FB} = 0 V) Minimum (V_{Comp} = 1.9 V)	$DC_{(max)}$ $DC_{(min)}$	92 0	95 0	100 0	%
SWITCH OUTPUT						
Output Voltage Source Saturation (V_{CC} = 7.5 V, I_{Source} = 5.0 A)		V_{sat}	–	(V_{CC} −1.5)	(V_{CC} −1.8)	V
Off–State Leakage (V_{CC} = 40 V, Pin 2 = Gnd)		$I_{sw(off)}$	–	0	100	µA
Current Limit Threshold (V_{CC} = 7.5 V)		$I_{pk(switch)}$	5.5	6.5	8.0	A
Switching Times (V_{CC} = 40 V, I_{pk} = 5.0 A, L = 225 µH, T_A = +25°C) Output Voltage Rise Time Output Voltage Fall Time		 t_r t_f	 – –	 100 50	 200 100	ns
UNDERVOLTAGE LOCKOUT						
Startup Threshold (V_{CC} Increasing, T_A = +25°C)		$V_{th(UVLO)}$	5.5	5.9	6.3	V
Hysteresis (V_{CC} Decreasing, T_A = +25°C)		$V_{H(UVLO)}$	0.6	0.9	1.2	V
TOTAL DEVICE						
Power Supply Current (T_A = +25°C) Standby (V_{CC} = 12 V, V_{Comp} < 0.15 V) Operating (V_{CC} = 40 V, Pin 1 = Gnd for maximum duty cycle)		I_{CC}	 – –	 36 40	 100 60	µA mA

NOTES: 1. Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34167 T_{high} = + 70°C for MC34167
= − 40°C for MC33167 = + 85°C for MC33167

Figure 1. Voltage Feedback Input Threshold versus Temperature

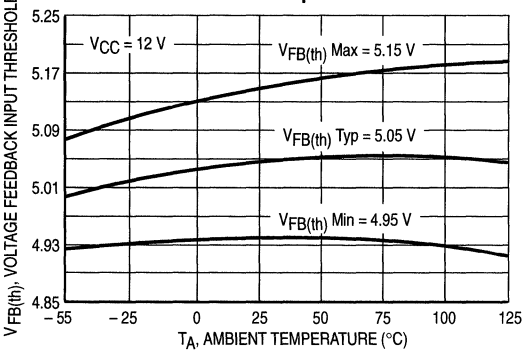


Figure 2. Voltage Feedback Input Bias Current versus Temperature

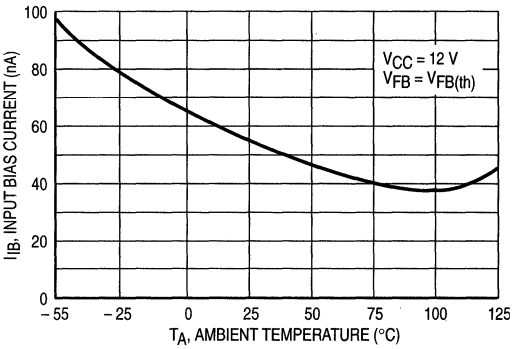


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

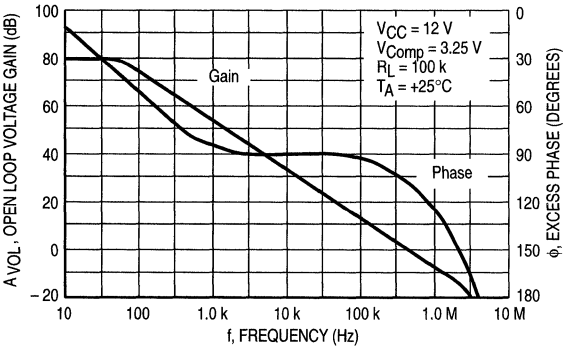


Figure 4. Error Amp Output Saturation versus Sink Current

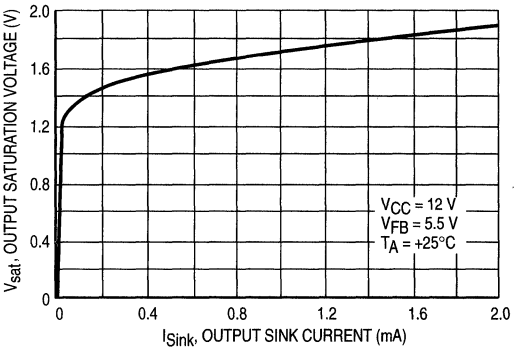


Figure 5. Oscillator Frequency Change versus Temperature

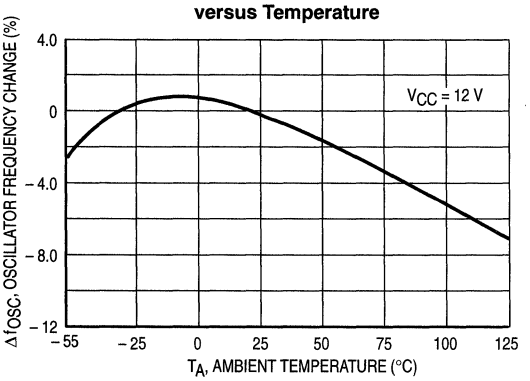


Figure 6. Switch Output Duty Cycle versus Compensation Voltage

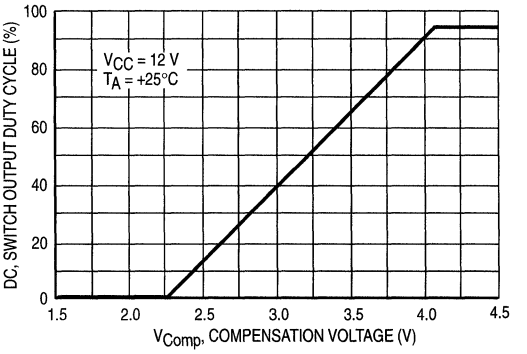


Figure 7. Switch Output Source Saturation versus Source Current

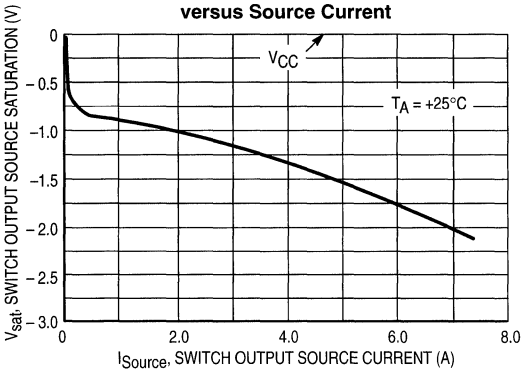


Figure 8. Negative Switch Output Voltage versus Temperature

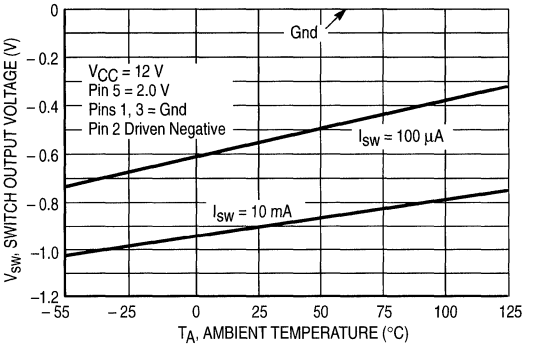


Figure 9. Switch Output Current Limit Threshold versus Temperature

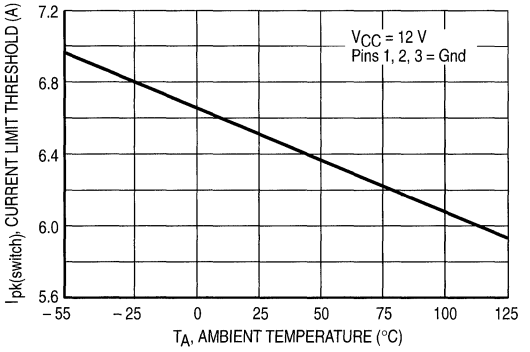


Figure 10. Standby Supply Current versus Supply Voltage

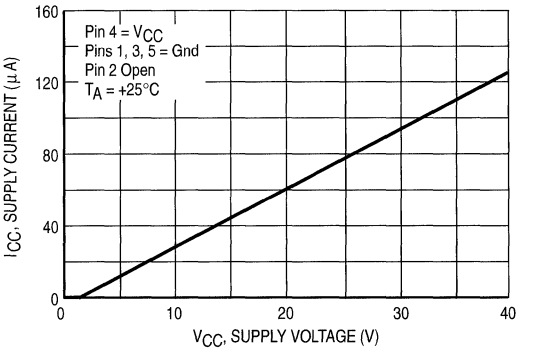


Figure 11. Undervoltage Lockout Thresholds versus Temperature

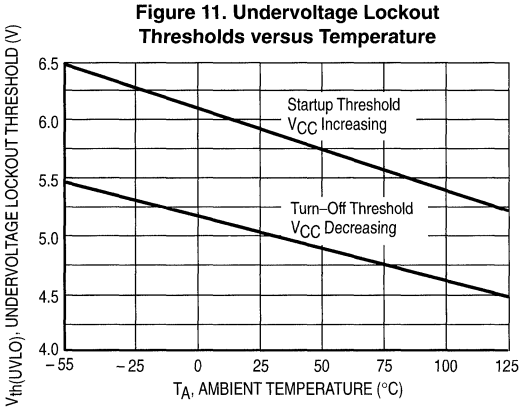
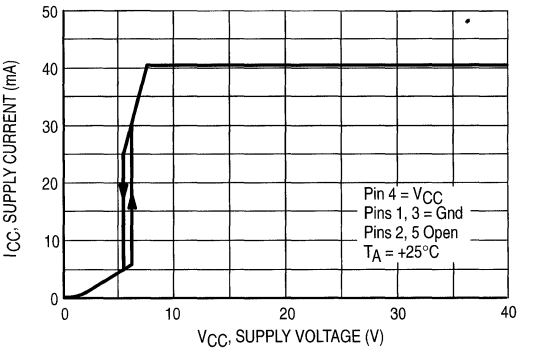


Figure 12. Operating Supply Current versus Supply Voltage



3

Figure 13. MC34167 Representative Block Diagram

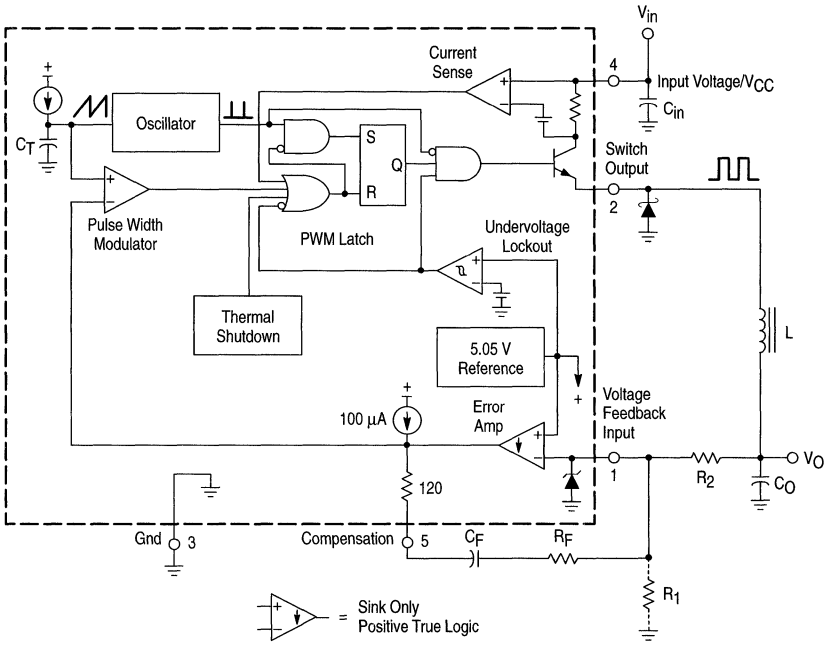
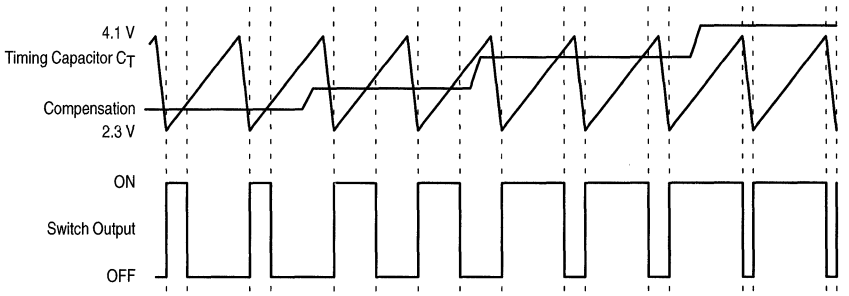


Figure 14. Timing Diagram



INTRODUCTION

The MC34167, MC33167 series are monolithic power switching regulators that are optimized for dc–to–dc converter applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step–down and voltage–inverting converters with a minimum number of external components. They can also be used cost effectively in step–up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 13.

Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor C_T and a trimmed current source. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the Switch Output. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1 V and 2.3 V respectively.

Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when C_T is discharged to the oscillator valley voltage. As C_T charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp–up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 6 and 14 illustrate the switch output duty cycle versus the compensation voltage.

Current Sense

The MC34167 series utilizes cycle–by–cycle current limiting as a means of protecting the output switch transistor from overstress. Each on cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp–up period.

The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch. The current limit threshold is typically set at 6.5 A. Figure 9 illustrates switch output current limit threshold versus temperature.

Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical dc voltage gain of 80 dB, and a unity gain bandwidth of 600 kHz with 70 degrees of phase margin (Figure 3). The noninverting input is biased to the internal 5.05 V reference and is not pinned out. The reference has an accuracy of ± 2.0% at room temperature. To provide 5.0 V at the load, the reference is programmed 50 mV above 5.0 V to compensate for a 1.0% voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input as shown in Figures 13 and 18. The equation for determining the output voltage with the divider network is:

$$V_{out} = 5.05 \left(\frac{R_2}{R_1} + 1\right)$$

External loop compensation is required for converter stability. A simple low–pass filter is formed by connecting a resistor (R_2) from the regulated output to the inverting input, and a series resistor–capacitor (R_F, C_F) between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step–down converter (Figure 18) is the easiest to compensate for stability. The step–up (Figure 20) and voltage–inverting (Figure 22) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting R_F and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150 mV, the internal circuitry will be placed into a low power standby mode, reducing the power supply current to 36 μA with a 12 V supply voltage. Figure 10 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a 100 μA current source pull–up that can be used to implement soft–start. Figure 17 shows the current source charging capacitor C_{SS} through a series diode. The diode disconnects C_{SS} from the feedback loop when the 1.0 M resistor charges it above the operating range of Pin 5.

Switch Output

The output transistor is designed to switch a maximum of 40 V, with a minimum peak collector current of 5.5 A. When configured for step–down or voltage–inverting applications, as in Figures 18 and 22, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 8 shows that by clamping the emitter to 0.5 V, the collector current will be in the range of 100 μA over temperature. A 1N5825 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully functional before the output stage is enabled. The internal reference voltage is monitored by the comparator which enables the output stage when V_{CC} exceeds 5.9 V. To prevent erratic output switching as the threshold is crossed, 0.9 V of hysteresis is provided.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the latch is forced into a 'reset' state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.** The MC34167 is contained in a 5–lead TO–220 type package. The tab of the package is common with the center pin (Pin 3) and is normally connected to ground.

3

DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire–wrap or plug–in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a tight component layout is recommended. Capacitors C_{in}, C_O, and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

Figure 15. Low Power Standby Circuit

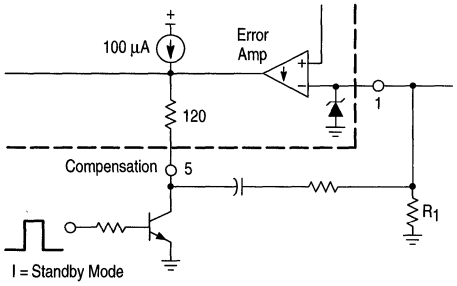
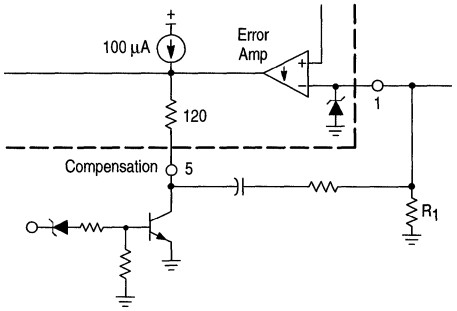
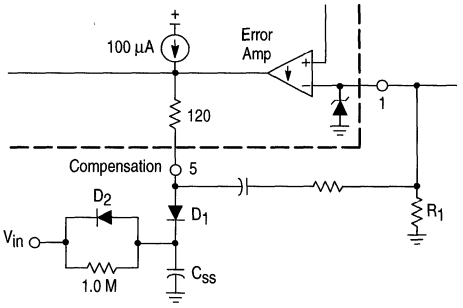


Figure 16. Over Voltage Shutdown Circuit



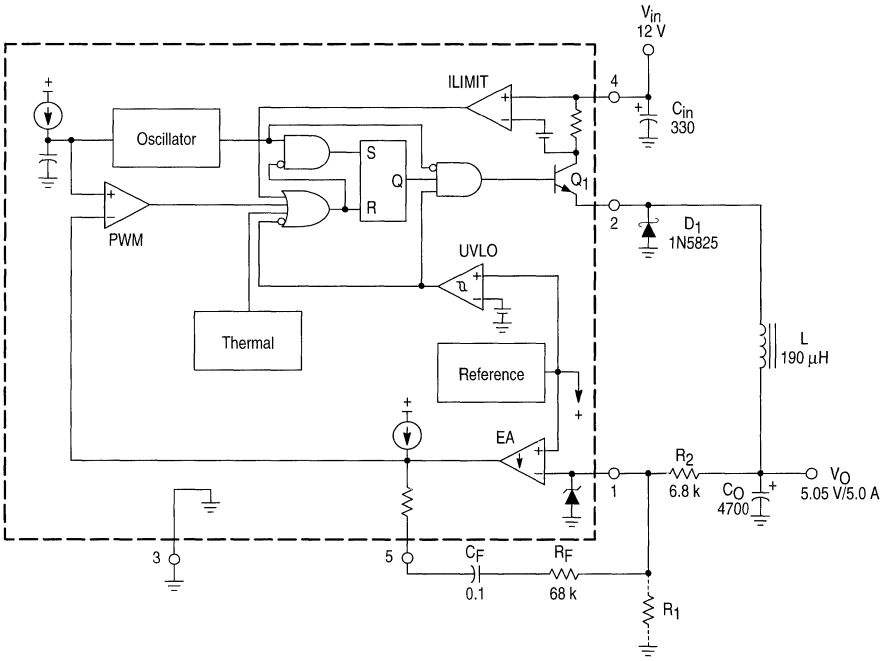
$V_{Shutdown} = V_{Zener} + 0.7$

Figure 17. Soft–Start Circuit



$t_{Soft-Start} \approx 35{,}000\ C_{SS}$

Figure 18. Step–Down Converter

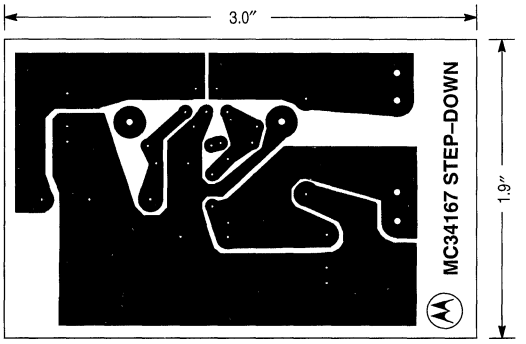


Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 36 V, I_O = 5.0 A	4.0 mV = ± 0.039%
Load Regulation	V_{in} = 12 V, I_O = 0.25 A to 5.0 A	1.0 mV = ± 0.01%
Output Ripple	V_{in} = 12 V, I_O = 5.0 A	20 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	6.5 A
Efficiency	V_{in} = 12 V, I_O = 5.0 A V_{in} = 24 V, I_O = 5.0 A	78.9% 82.6%

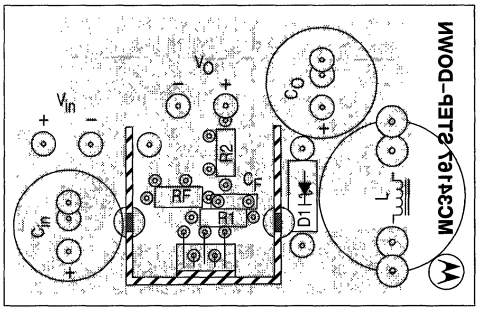
L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

The Step–Down Converter application is shown in Figure 18. The output switch transistor Q_1 interrupts the input voltage, generating a squarewave at the LC_O filter input. The filter averages the squarewaves, producing a dc output voltage that can be set to any level between V_{in} and V_{ref} by controlling the percent conduction time of Q_1 to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input.

Figure 19. Step–Down Converter Printed Circuit Board and Component Layout



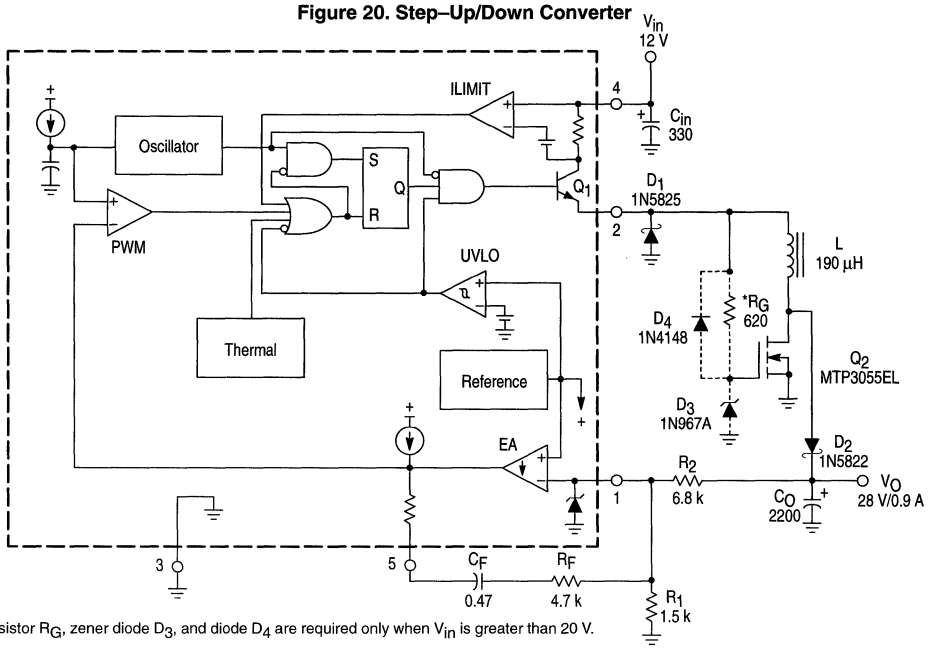
(Bottom View)



(Top View)

3

Figure 20. Step–Up/Down Converter



*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 24 V, I_O = 0.9 A	10 mV = ± 0.017%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 0.9 A	30 mV = ± 0.053%
Output Ripple	V_{in} = 12 V, I_O = 0.9 A	140 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	6.0 A
Efficiency	V_{in} = 12 V, I_O = 0.9 A V_{in} = 24 V, I_O = 0.9 A	80.1% 87.8%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core.
Heatsink = AAVID Engineering Inc.
MC34167: 5903B, or 5930B
MTP3055EL: 5925B

Figure 20 shows that the MC34167 can be configured as a step–up/down converter with the addition of an external power MOSFET. Energy is stored in the inductor during the ON time of transistors Q_1 and Q_2. During the OFF time, the energy is transferred, with respect to ground, to the output filter capacitor and load. This circuit configuration has two significant advantages over the basic step–up converter circuit. The first advantage is that output short circuit protection is provided by the MC34167, since Q_1 is directly in series with V_{in} and the load. Second, the output voltage can be programmed to be less than V_{in}. Notice that during the OFF time, the inductor forward biases diodes D_1 and D_2, transferring its energy with respect to ground rather than with respect to V_{in}. When operating with V_{in} greater than 20 V, a gate protection network is required for the MOSFET. The network consists of components R_G, D_3, and D_4.

Figure 21. Step–Up/Down Converter Printed Circuit Board and Component Layout

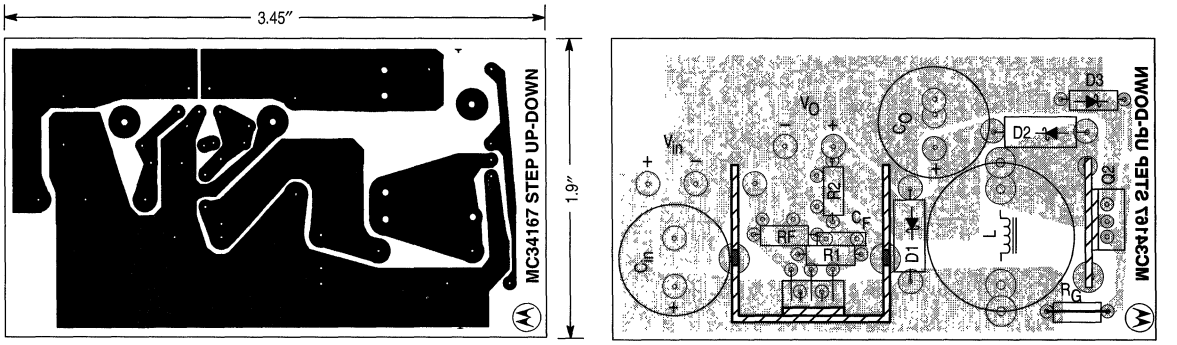
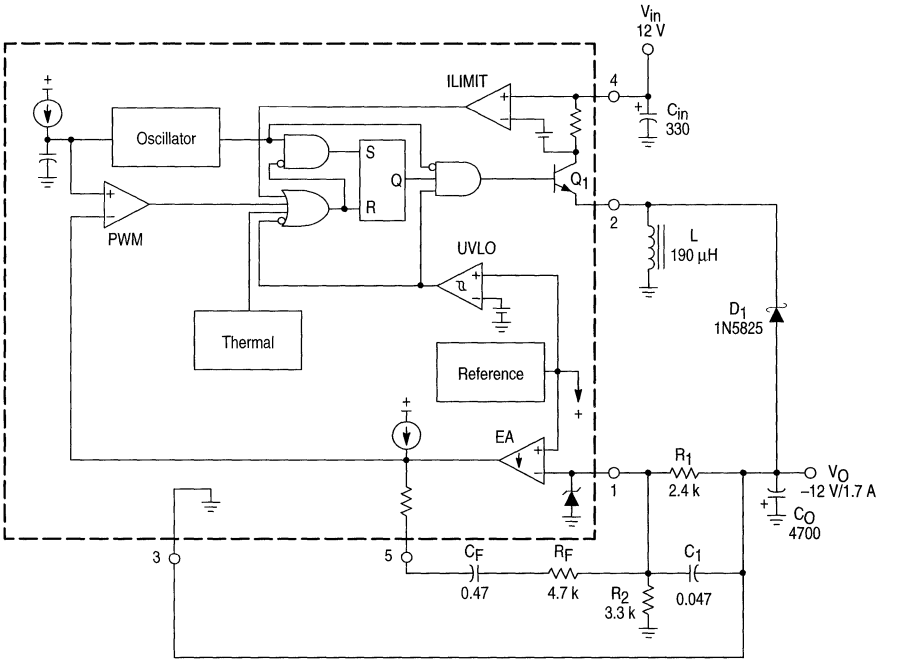


Figure 22. Voltage–Inverting Converter



Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 24 V, I_O = 1.7 A	15 mV = ± 0.61%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 1.7 A	4.0 mV = ± 0.020%
Output Ripple	V_{in} = 12 V, I_O = 1.7 A	78 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	5.7 A
Efficiency	V_{in} = 12 V, I_O = 1.7 A V_{in} = 24 V, I_O = 1.7 A	79.5% 86.2%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Two potential problems arise when designing the standard voltage–inverting converter with the MC34167. First, the Switch Output emitter is limited to –1.5 V with respect to the ground pin and second, the Error Amplifier's noninverting input is internally committed to the reference and is not pinned out. Both of these problems are resolved by connecting the IC ground pin to the converter's negative output as shown in Figure 22. This keeps the emitter of Q_1 positive with respect to the ground pin and has the effect of reversing the Error Amplifier inputs. Note that the voltage drop across R_1 is equal to 5.05 V when the output is in regulation.

Figure 23. Voltage–Inverting Converter Printed Circuit Board and Component Layout

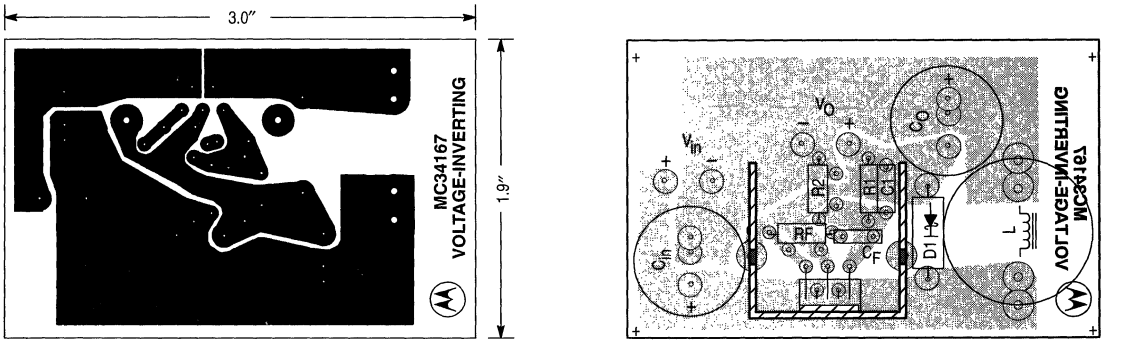
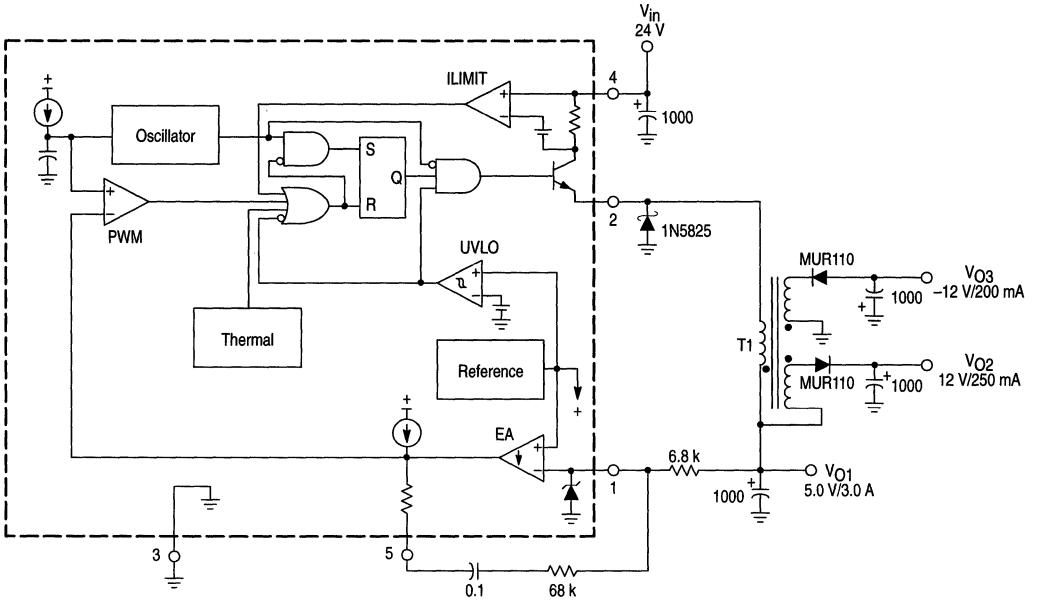


Figure 24. Triple Output Converter



Tests		Conditions	Results
Line Regulation	5.0 V 12 V –12 V	V_{in} = 15 V to 30 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA	3.0 mV = ± 0.029% 572 mV = ± 2.4% 711 mV = ± 2.9%
Load Regulation	5.0 V 12 V –12 V	V_{in} = 24 V, I_{O1} = 30 mA to 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 100 mA to 250 mA, I_{O3} = 200 mA V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 75 mA to 200 mA	1.0 mV = ± 0.009% 409 mV = ±1.5% 528 mV = ± 2.0%
Output Ripple	5.0 V 12 V –12 V	V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA	75 mV_{pp} 20 mV_{pp} 20 mV_{pp}
Short Circuit Current	5.0 V 12 V –12 V	V_{in} = 24 V, R_L = 0.1 Ω	6.5 A 2.7 A 2.2 A
Efficiency	TOTAL	V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA	84.2%

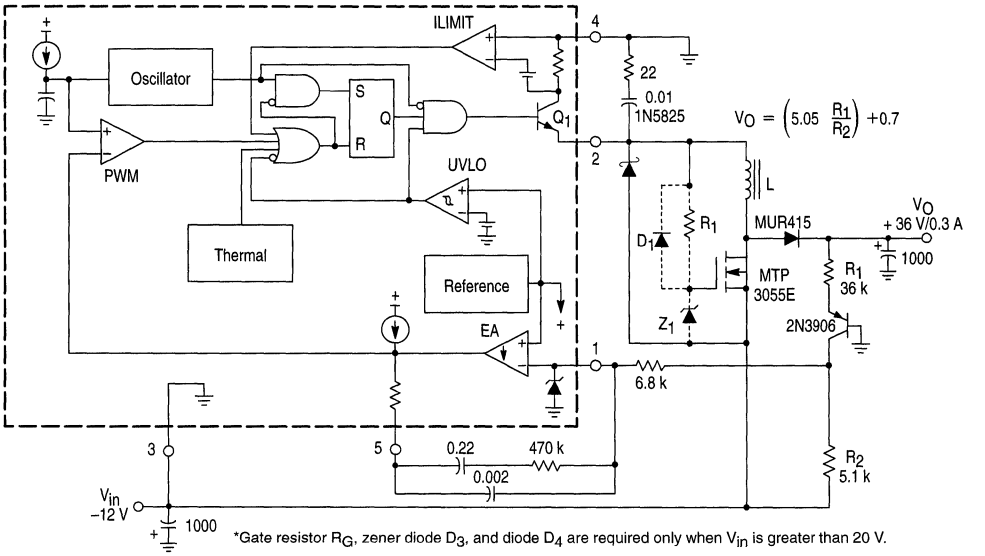
T1 = Primary: Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core.
Secondary: V_{O2} – 69 turns of #26 AWG
V_{O3} – 104 turns of #28 AWG
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the OFF time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$\#\ TURNS_{(SEC)} = \frac{V_{O(SEC)} + V_{F(SEC)}}{\left(\frac{V_{O(PRI)} + V_{F(PRI)}}{\#TURNS_{(PRI)}}\right)}$$

Note that the 12 V winding is stacked on top of the 5.0 V output. This reduces the number of secondary turns and improves lead regulation. For best auxiliary regulation, the auxiliary outputs should be less than 33% of the total output power.

Figure 25. Negative Input/Positive Output Regulator

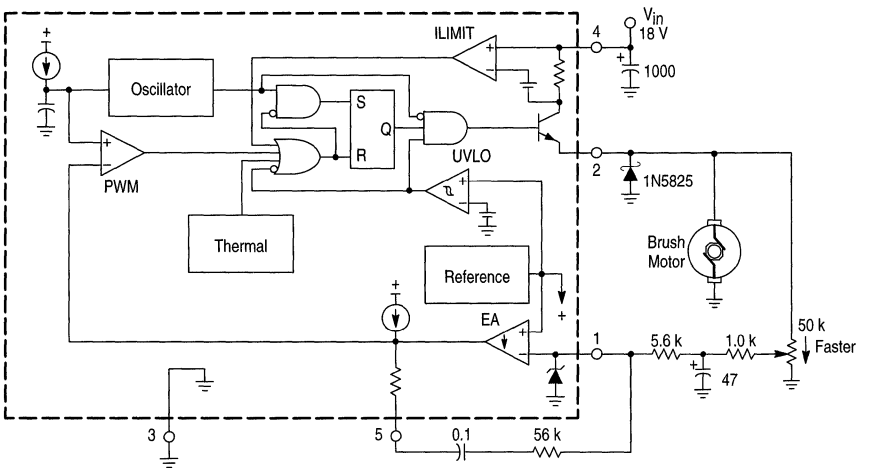


*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Conditions	Results
Line Regulation	V_{in} = −10 V to − 20 V, I_O = 0.3 A	266 mV = ± 0.38%
Load Regulation	V_{in} = −12 V, I_O = 0.03 A to 0.3 A	7.90 mV = ±1.1%
Output Ripple	V_{in} = −12 V, I_O = 0.3 A	100 mV_{pp}
Efficiency	V_{in} = −12 V, I_O = 0.3 A	78.4%

L = General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B or 5930B

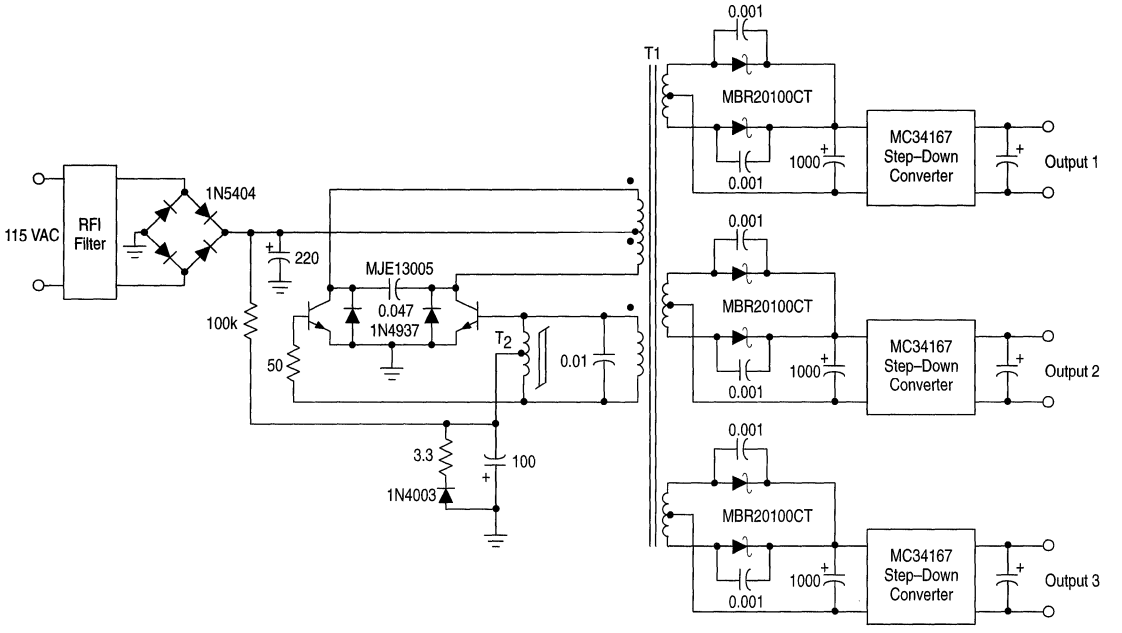
Figure 26. Variable Motor Speed Control with EMF Feedback Sensing



Test	Conditions	Results
Low Speed Line Regulation	V_{in} = 12 V to 24 V	1760 RPM ±1%
High Speed Line Regulation	V_{in} = 12 V to 24 V	3260 RPM ± 6%

3

Figure 27. Off–Line Preconverter



T_1 = Core and Bobbin – Coilcraft PT3595
Primary – 104 turns #26 AWG
Base Drive – 3 turns #26 AWG
Secondaries – 16 turns #16 AWG
Total Gap – 0.002,

T_2 = Core – TDK T6 x 1.5 x 3 H5C2
14 turns center tapped #30 AWG
Heatsink = AAVID Engineering Inc.
MC34167 and MJE13005 – 5903B
MBR20100CT – 5925B

The MC34167 can be used cost effectively in off–line applications even though it is limited to a maximum input voltage of 40 V. Figure 27 shows a simple and efficient method for converting the AC line voltage down to 24 V. This preconverter has a total power rating of 125 W with a conversion efficiency of 90%. Transformer T_1 provides output isolation from the AC line and isolation between each of the secondaries. The circuit self–oscillates at 50 kHz and is controlled by the saturation characteristics of T_2. Multiple MC34167 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

Figure 28. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

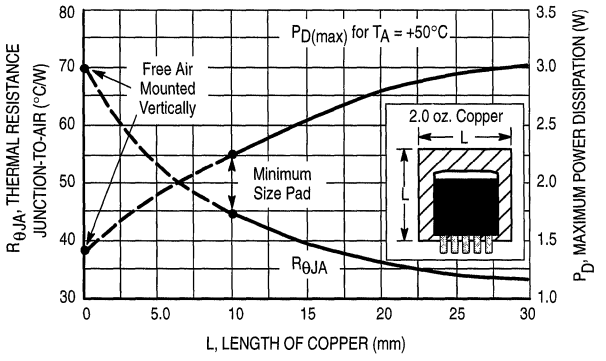


Table 1. Design Equations

Calculation	Step–Down	Step–Up/Down	Voltage–Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_{F1} + V_{F2}}{V_{in} - V_{satQ1} - V_{satQ2}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$
Duty Cycle (Note 3)	$t_{on}\, f_{osc}$	$t_{on}\, f_{osc}$	$t_{on}\, f_{osc}$
$I_{L\ avg}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk(switch)}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L}\right)t_{on}$	$\left(\frac{V_{in} - V_{satQ1} - V_{satQ2}}{\Delta I_L}\right)t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right)t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 f_{osc} C_o}\right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1\right)\sqrt{\left(\frac{1}{f_{osc} C_o}\right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1\right)\sqrt{\left(\frac{1}{f_{osc} C_o}\right)^2 + (ESR)^2}$
V_{out}	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$

NOTES: 1. V_{sat} – Switch Output source saturation voltage, refer to Figure 7.
2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.35 V.
3. Duty cycle is calculated at the minimum operating input voltage and must not exceed the guaranteed minimum $DC_{(max)}$ specification of 0.92.

The following converter characteristics must be chosen:

V_{out} – Desired output voltage.

I_{out} – Desired output current.

ΔI_L – Desired peak–to–peak inductor ripple current. For maximum output current especially when the duty cycle is greater than 0.5, it is suggested that ΔI_L be chosen minimum current limit threshold of 5.5 A. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2\ (I_{L\ avg})$. This will proportionally reduce the converter's output current capability.

$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. For best performance, the ripple voltage should be kept to less than 2% of V_{out}. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

MOTOROLA

MC34261
MC33261

Power Factor Controllers

3

The MC34261/MC33261 are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off–line power converter applications. These integrated circuits feature an internal startup timer, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, high gain error amplifier, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input undervoltage lockout with hysteresis, cycle–by–cycle current limiting, and a latch for single pulse metering. These devices are available in dual–in–line and surface mount plastic packages.

- Internal Startup Timer
- One Quadrant Multiplier
- Zero Current Detector
- Trimmed 2% Internal Bandgap Reference
- Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- Pinout Equivalent to the SG3561
- Functional Equivalent to the TDA4817

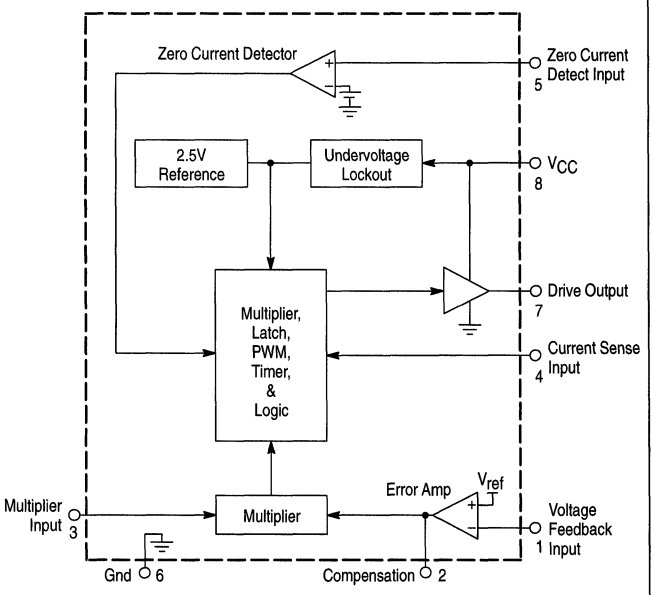
POWER FACTOR CONTROLLERS

SEMICONDUCTOR TECHNICAL DATA

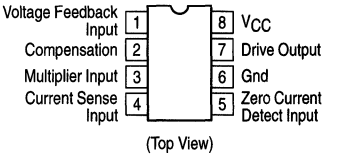
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34261D	T_A = 0° to +70°C	SO–8
MC34261P		Plastic DIP
MC33261D	T_A = –40° to +85°C	SO–8
MC33261P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	500	mA
Current Sense, Multiplier, and Voltage Feedback Inputs	V_{in}	–1.0 to 10	V
Zero Current Detect Input High State Forward Current Low State Reverse Current	I_{in}	 50 –10	mA
Power Dissipation and Thermal Characteristics P Suffix, Plastic Package Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air D Suffix, Plastic Package Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 800 100 450 178	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34261 MC33261	T_A	 0 to +70 –40 to +85	°C
Storage Temperature	T_{stg}	–55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Voltage Feedback Input Threshold T_A = 25°C $T_A = T_{low}$ to T_{high} (V_{CC} = 12 V to 28 V)	V_{FB}	 2.465 2.44	2.5	 2.535 2.54	V
Line Regulation (V_{CC} = 12 V to 28 V, T_A = 25°C)	Reg_{line}	–	1.0	10	mV
Input Bias Current (V_{FB} = 0 V)	I_{IB}	–	–0.3	–1.0	µA
Open Loop Voltage Gain	A_{VOL}	65	85	–	dB
Gain Bandwidth Product (T_A = 25°C)	GBW	0.7	1.0	–	MHz
Output Source Current (V_O = 4.0 V, V_{FB} = 2.3 V)	I_{Source}	0.25	0.5	0.75	mA
Output Voltage Swing High State (I_{Source} = 0.2 mA, V_{FB} = 2.3 V) Low State (I_{Sink} = 0.4 mA, V_{FB} = 2.7 V)	 V_{OH} V_{OL}	 5.0 –	 5.7 2.1	 – 2.44	V
MULTIPLIER					
Dynamic Input Voltage Range Multiplier Input (Pin 3) Compensation (Pin 2)	 $V_{Pin\ 3}$ $V_{Pin\ 2}$	 0 to 2.5 V_{FB} to (V_{FB} + 1.0)	 0 to 3.5 V_{FB} to (V_{FB} + 1.5)	 – –	V
Input Bias Current (V_{FB} = 0 V)	I_{IB}	–	–0.3	–1.0	µA
Multiplier Gain ($V_{Pin\ 3}$ = 0.5 V, $V_{Pin\ 2} = V_{FB}$ + 1.0 V) (Note 2)	K	0.4	0.62	0.8	1/V
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Increasing)	V_{th}	1.3	1.6	1.8	V
Hysteresis (V_{in} Decreasing)	V_H	40	110	200	mV
Input Clamp Voltage High State (I_{DET} = 3.0 mA) Low State (I_{DET} = –3.0 mA)	 V_{IH} V_{IL}	 6.1 0.3	 6.7 0.7	 – 1.0	V

NOTES: 1. Maximum package power dissipation limits must be observed.

2. $K = \dfrac{\text{Pin 4 Threshold Voltage}}{V_{Pin\ 3}(V_{Pin\ 2} - V_{FB})}$

3. T_{low} = 0°C for MC34261, –40°C for MC33261 $\quad$ T_{high} = +70°C for MC34261, +85°C for MC33261

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE COMPARATOR					
Input Bias Current ($V_{Pin\ 4}$ = 0 V)	I_{IB}	–	–0.5	–2.0	µA
Input Offset Voltage ($V_{Pin\ 2}$ = 1.1 V, $V_{Pin\ 3}$ = 0 V)	V_{IO}	–	3.5	15	mV
Delay to Output	t_{PHL} (in/out)	–	200	400	ns
DRIVE OUTPUT					
Output Voltage (V_{CC} = 12 V)					V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.3	0.8	
(I_{Sink} = 200 mA)		1.8	2.4	3.3	
High State (I_{Source} = 20 mA)	V_{OH}	9.8	10.3	–	
(I_{Source} = 200 mA)		7.8	8.3	8.8	
Output Voltage (V_{CC} = 30 V)	$V_{O(max)}$				V
High State (I_{Source} = 20 mA, C_L = 15 pF)		14	16	18	
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	50	120	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	50	120	ns
Output Voltage with UVLO Activated (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{OH(UVLO)}$	–	0.2	0.8	V
RESTART TIMER					
Restart Time Delay	t_{DLY}	150	400	–	µs
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing)	V_{th}	9.2	10.0	10.8	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{Shutdown}$	7.0	8.0	9.0	V
Hysteresis	V_H	1.75	2.0	2.5	V
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Startup (V_{CC} = 7.0 V)		–	0.3	0.5	
Operating		–	7.1	12	
Dynamic Operating (50 kHz, C_L = 1.0 nF)		–	9.0	20	
Power Supply Zener Voltage	V_Z	30	36	–	V

NOTES: 1. Maximum package power dissipation limits must be observed.

2. $K = \dfrac{\text{Pin 4 Threshold Voltage}}{V_{Pin\ 3}(V_{Pin\ 2} - V_{FB})}$

3. T_{low} = 0°C for MC34261, –40°C for MC33261 $\quad T_{high}$ = +70°C for MC34261, +85°C for MC33261

Figure 1. Current Sense Input Threshold versus Multiplier Input

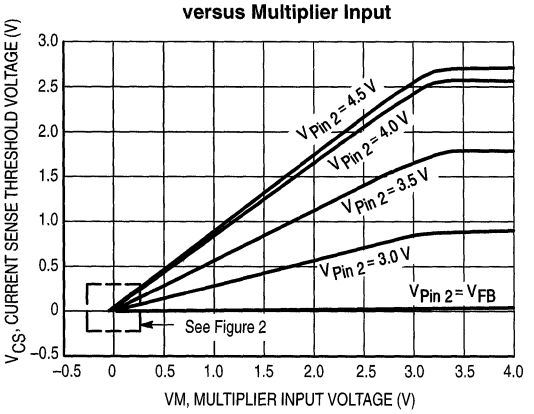


Figure 2. Current Sense Input Threshold versus Multiplier Input

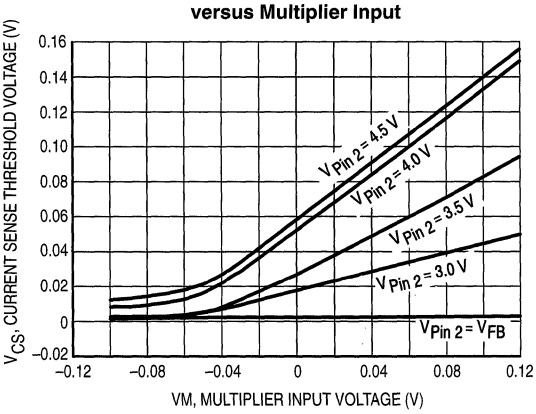


Figure 3. Voltage Feedback Input Threshold Change versus Temperature

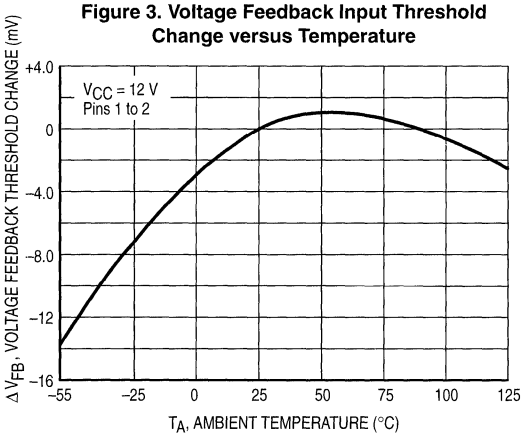


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency

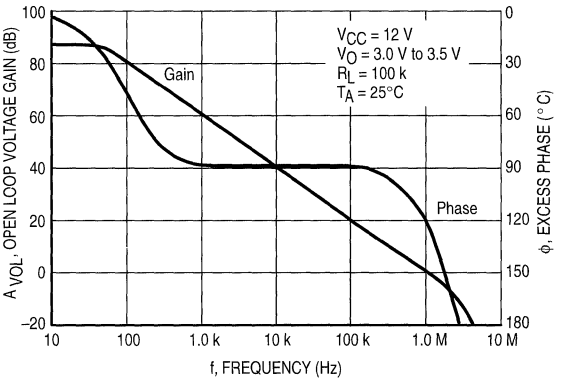


Figure 5. Error Amp Small Signal Transient Response

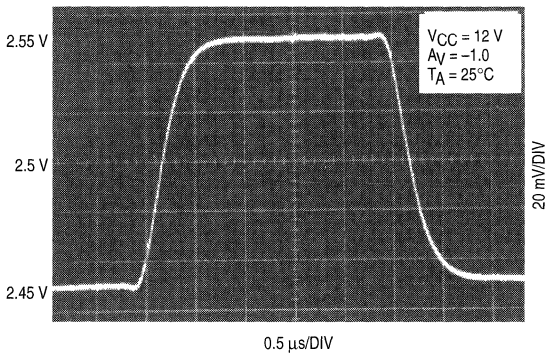


Figure 6. Error Amp Large Signal Transient Response

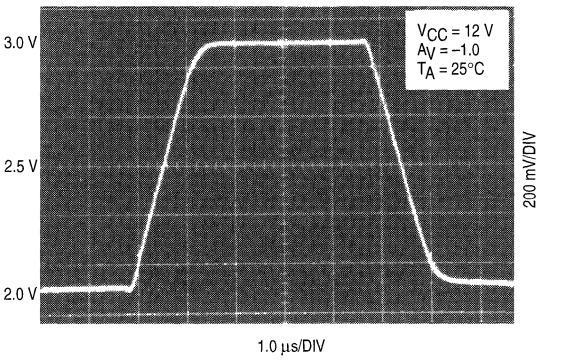


Figure 7. Error Amp Output Saturation versus Sink Current

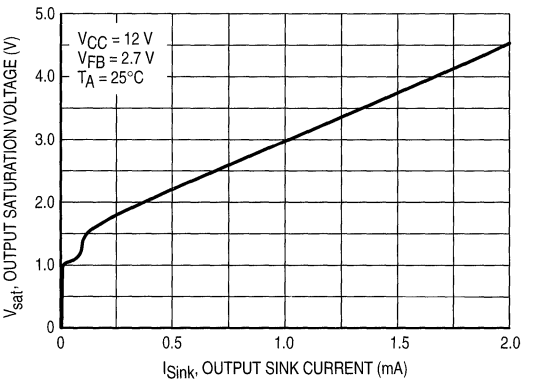
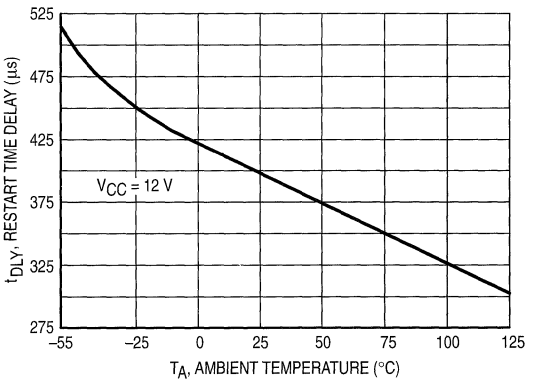


Figure 8. Restart Time Delay versus Temperature



3

Figure 9. Zero Current Detector Input Threshold Voltage Change versus Temperature

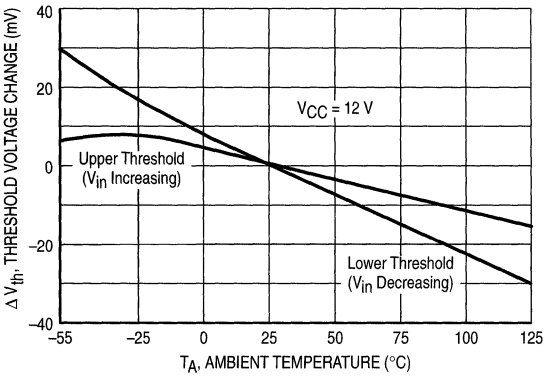


Figure 10. Output Saturation Voltage versus Load Current

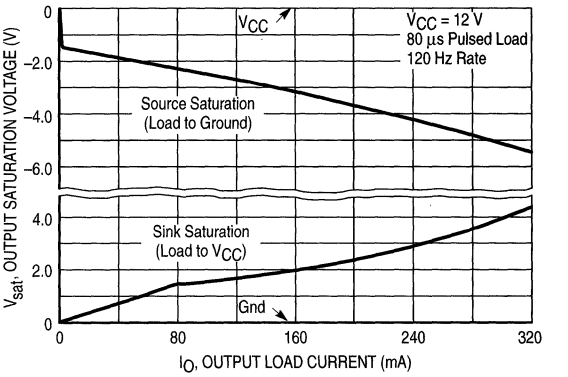


Figure 11. Drive Output Waveform

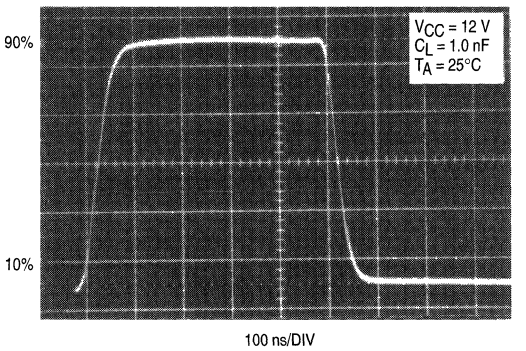


Figure 12. Drive Output Cross Conduction

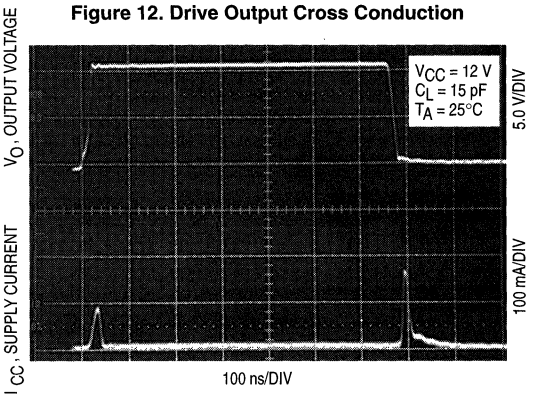


Figure 13. Supply Current versus Supply Voltage

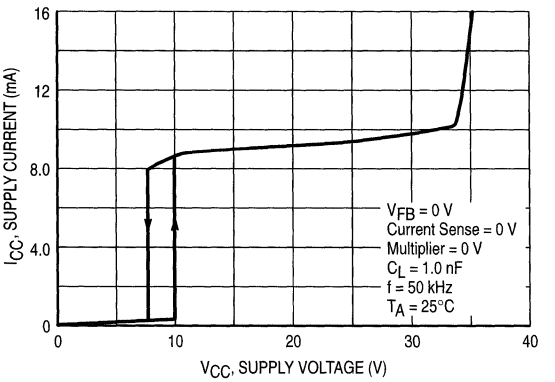
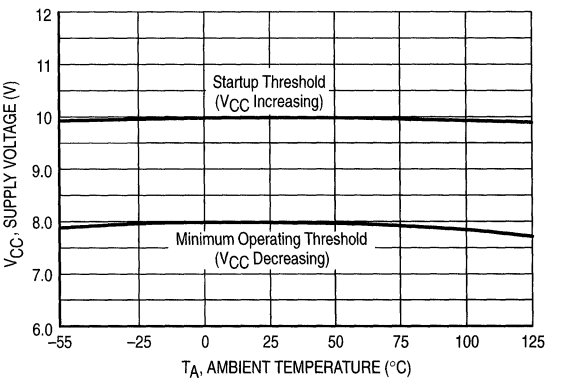


Figure 14. Undervoltage Lockout Thresholds versus Temperature



FUNCTIONAL DESCRIPTION

Introduction

Most electronic ballasts and switching power supplies use a bridge rectifier and a filter capacitor to derive raw dc voltage from the utility ac line. This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor's voltage. This occurs near the line voltage peak and results in a high charge current spike. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power.

The MC34261, MC33261 are high performance, critical conduction, current mode power factor controllers specifically designed for use in off–line active preconverters. These devices provide the necessary features required to significantly enhance poor power factor loads by keeping the ac line current sinusoidal and in phase with the line voltage. With proper control of the preconverter, almost any complex load can be made to appear resistive to the ac line, thus significantly reducing the harmonic current content.

Operating Description

The MC34261, MC33261 contains many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. There are, however, two areas where there is a major difference when compared to popular devices such as the UC3842 series. Referring to the block diagram in Figure 15, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. A description of each of the functional blocks is given below.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 85 dB, and a unity gain bandwidth of 1.0 MHz with 58° of phase margin (Figure 4). The noninverting input is internally biased at 2.5 V ±2.0% and is not pinned out. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is –1.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R_2. The Error Amp Output is internally connected to the Multiplier and is pinned out (Pin 2) for external loop compensation. Typically, the bandwidth is set below 20 Hz, so that the Error Amp output voltage is relatively constant over a given ac line cycle. The output stage consists of a 500 μA current source pull–up with a Darlington transistor pull–down. It is capable of swinging from 2.1 V to 5.7 V, assuring that the Multiplier can be driven over its entire dynamic range.

Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The ac haversines are monitored at Pin 3 with respect to ground while the Error Amp output at Pin 2 is monitored with respect to the Voltage Feedback Input threshold. A graph of the Multiplier transfer curve is shown in Figure 1. Note that both inputs are extremely linear over a wide dynamic range, 0 V to 3.2 V for the Multiplier input (Pin 3), and 2.5 V to 4.0 V for the Error Amp output (Pin 2). The Multiplier output controls the Current Sense Comparator threshold (Pin 4) as the ac voltage traverses sinusoidally from zero to peak line. This has the effect of forcing the MOSFET peak current to track the input line voltage, thus making the preconverter load appear to be resistive.

$$\text{Pin 4 Threshold} \approx 0.62(V_{\text{Pin 2}} - V_{FB})V_{\text{Pin 3}}$$

Zero Current Detector

The MC34261 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on–time by setting the RS Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn on until the inductor current reaches zero, the output rectifier's reverse recovery time becomes less critical allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous thus limiting the peak switch to twice the average input current.

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.6 V. To prevent false tripping, 110 mV of hysteresis is provided. The Zero Current Detector input is internally protected by two clamps. The upper 6.7 V clamp prevents input overvoltage breakdown while the lower 0.7 V clamp prevents substrate injection. Device destruction can result if this input is shorted to ground. An external resistor must be used in series with the auxiliary winding to limit the current through the clamps.

Current Sense Comparator and RS Latch

The Current Sense Comparator RS Latch configuration ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground referenced sense resistor R_9 in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input and compared to the Multiplier output voltage. The peak inductor current is controlled by the threshold voltage of Pin 4 where:

$$I_{pk} = \frac{\text{Pin 4 Threshold}}{R_9}$$

With the component values shown in Figure 16, the Current Sense Comparator threshold, at the peak of the haversine varies from 1.1 V at 90 Vac to 100 mV at 268 Vac. The Current Sense Input to Drive Output propagation delay is typically 200 ns.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 400 μs after the inductor current reaches zero.

Undervoltage Lockout

An Undervoltage Lockout comparator guarantees that the IC is fully functional before enabling the output stage. The positive power supply terminal (V_{CC}) is monitored by the UVLO comparator with the upper threshold set at 10 V and the lower threshold at 8.0 V (Figure 14). In the standby mode, with V_{CC} at 7.0 V, the required supply current is less than 0.5 mA (Figure 13). This hysteresis and low startup current allow the implementation of efficient bootstrap startup techniques, making these devices ideally suited for wide input range off line preconverter applications. An internal 36 V clamp has been added from V_{CC} to ground to protect the IC and capacitor C_5 from an overvoltage condition. This feature is desirable if external circuitry is used to delay the startup of the preconverter.

Output

The MC34261/MC33261 contain a single totem pole output stage specifically designed for direct drive of power MOSFETs. The Drive Output is capable of up to ±500 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull–down resistor. The totem pole output has been optimized to minimize cross conduction current during high speed operation. The addition of two 10 Ω resistors, one in series with the source output transistor and one in series with the sink output transistor, reduces the cross conduction current, as shown in Figure 12. A 16 V clamp has been incorporated into the output stage to limit the high state V_{OH}. This prevents rupture of the MOSFET gate when V_{CC} exceeds 20 V.

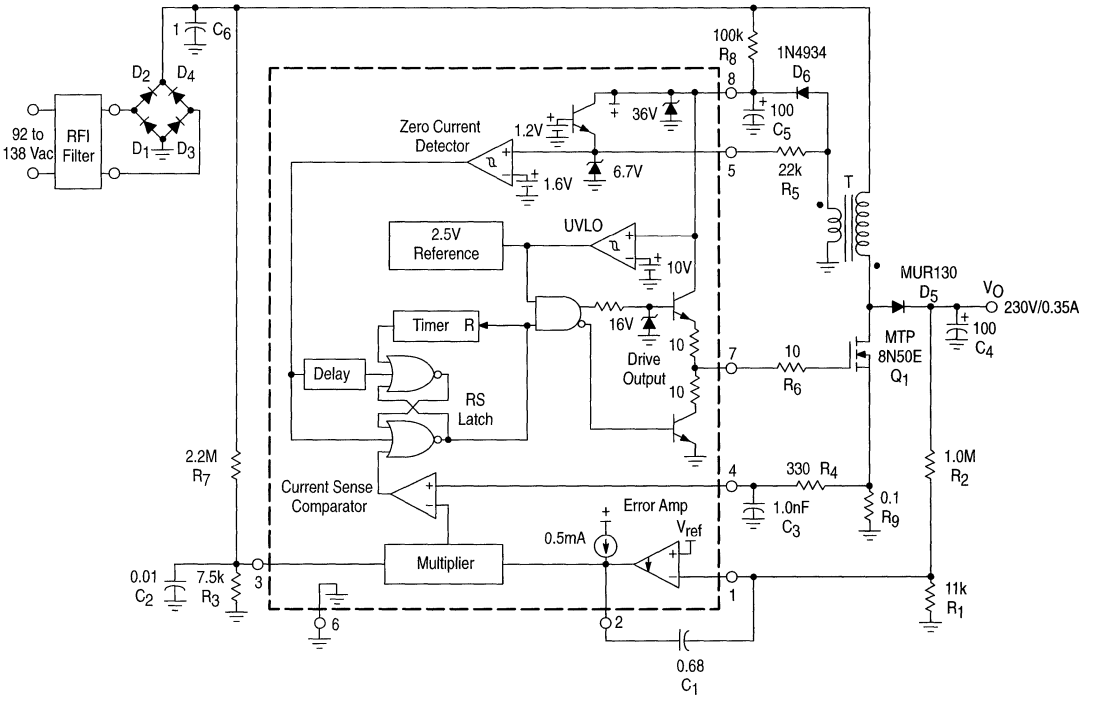
Table 1. Design Equations

Notes	Calculation	Formula
Calculate the maximum required output power.	Required Converter Output Power	$P_O = V_O I_O$
Calculated at the minimum required ac line for regulation. Let the efficiency n = 0.95.	Peak Inductor Current	$I_{L(pk)} = \frac{2\sqrt{2}\,P_O}{\eta Vac_{(LL)}}$
Let the switching cycle t = 20 μs.	Inductance	$L = \frac{2t\left(\frac{V_O}{\sqrt{2}} - Vac\right) Vac^2}{V_O\, Vac_{(LL)}\, I_{L(pk)}}$
In theory the on–time t_{on} is constant. In practice t_{on} tends to increase at the ac line zero crossings due to the charge on capacitor C_6.	Switch On–Time	$t_{on} = \frac{2\,P_O\,L}{\eta\, Vac^2}$
The off–time t_{off} is greatest at peak ac line and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.	Switch Off–Time	$t_{off} = \frac{t_{on}}{\frac{V_O}{\sqrt{2}\, Vac\, \lvert Sin\,\theta \rvert} - 1}$
The minimum switching frequency occurs at peak ac line and increases as t_{off} decreases.	Switching Frequency	$f = \frac{1}{t_{on} + t_{off}}$
Set the current sense threshold V_{CS} to 1.0 V for universal input (85 Vac to 265 Vac) operation and to 0.5 V for fixed input (92 Vac to 138 Vac, or 184 to 276 Vac) operation.	Peak Switch Current	$R_9 = \frac{V_{CS}}{I_{L(pk)}}$
Set the multiplier input voltage V_M to 3.0 V at high line. Empirically adjust V_M for the lowest distortion over the ac line range while guaranteeing startup at minimum line.	Multiplier Input Voltage	$V_M = \frac{Vac\,\sqrt{2}}{\left(\frac{R_7}{R_3} + 1\right)}$
The $I_{IB}\,R_1$ error term can be minimized with a divider current in excess of 100 μA.	Converter Output Voltage	$V_O = V_{ref}\left(\frac{R_2}{R_1} + 1\right) - I_{IB}\,R_2$
The bandwidth is typically set to 20 Hz for minimum output ripple over the ac line haversine.	Error Amplifier Bandwidth	$BW = \frac{1}{2\pi \frac{R_1 R_2}{R_1 + R_2} C_1}$

The following converter characteristics must be chosen:

V_O – Desired output voltage
I_O – Desired output current
Vac – AC RMS line voltage
$Vac_{(LL)}$ – AC RMS low line voltage

Figure 15. 80 W Power Factor Controller



Power Factor Controller Test Data

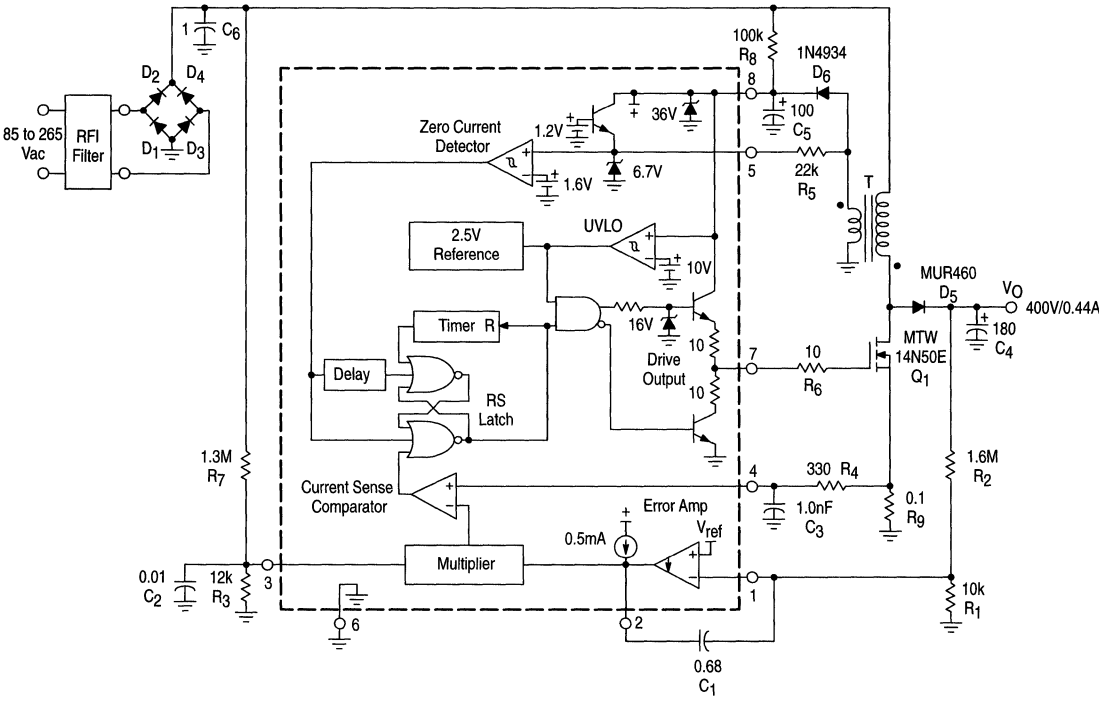
AC Line Input								DC Output				
			Current Harmonic Distortion (%)									
V_{rms}	P_{in}	PF	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	n(%)
90	85.6	–0.998	2.4	0.11	0.52	1.3	0.67	10.0	230	0.350	80.5	94.0
100	85.1	–0.997	5.0	0.13	1.7	2.4	1.4	10.1	230	0.350	80.5	94.6
110	84.8	–0.997	5.3	0.12	2.5	2.6	1.5	10.2	230	0.350	80.5	94.9
120	84.5	–0.997	5.8	0.12	3.2	2.7	1.4	10.2	230	0.350	80.5	95.3
130	84.2	–0.996	6.6	0.12	4.0	2.8	1.5	10.2	230	0.350	80.5	95.6
138	84.1	–0.995	7.2	0.13	4.5	3.0	1.6	10.2	230	0.350	80.5	95.7

This data was taken with the test set–up shown in Figure 17.

T = Coilcraft N2881–A
Primary: 62 turns of # 22 AWG
Secondary: 5 turns of # 22 AWG
Core: Coilcraft PT2510, EE 25
Gap: 0.072″ total for a primary inductance of 320 μH

Heatsink = AAVID Engineering Inc. 5903B, or 5930B

Figure 16. 175 W Universal Input Power Factor Controller



Power Factor Controller Test Data

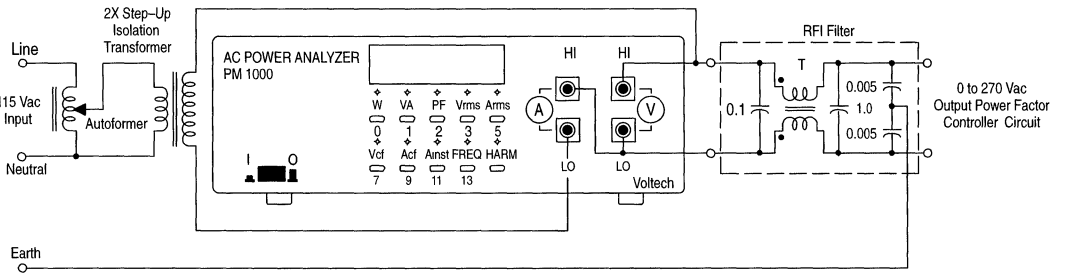
AC Line Input								DC Output				
			Current Harmonic Distortion (%)									
V_{rms}	P_{in}	PF	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	n(%)
90	187.5	–0.998	2.0	0.10	0.98	0.90	0.78	8.0	400.7	0.436	174.7	93.2
120	184.6	–0.997	1.8	0.09	1.3	1.3	0.93	8.0	400.7	0.436	174.7	94.6
138	183.6	–0.997	2.3	0.05	1.6	1.5	1.0	8.0	400.7	0.436	174.7	95.2
180	181.0	–0.995	4.3	0.16	2.5	2.0	1.2	8.0	400.6	0.436	174.7	95.6
240	179.3	–0.993	6.0	0.08	3.7	2.7	1.4	8.0	400.6	0.436	174.7	97.4
268	178.6	–0.992	6.7	0.16	2.8	3.7	1.7	8.0	400.6	0.436	174.7	97.8

This data was taken with the test set–up shown in Figure 17.

T = Coilcraft N2880–A
Primary: 78 turns of # 16 AWG
Secondary: 6 turns of # 18 AWG
Core: Coilcraft PT4215, EE 42–15
Gap: 0.104″ total for a primary inductance of 870 μH

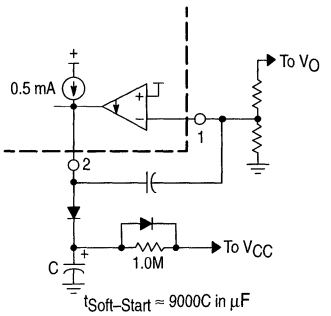
Heatsink = AAVID Engineering Inc. 5903B

Figure 17. Power Factor Test Set–Up



An RFI filter is required for best performance when connecting the preconverter directly to the AC line. Commercially available two stage filters such as the Delta Electronics 03DPCG5 work excellent. The simple single stage test filter shown above can easily be constructed with a common mode transformer. Transformer (T) is a Coilcraft CMT3–28–2 with 28 mH minimum inductance and a 2.0 A maximum current rating.

Figure 18. Soft–Start Circuit



Startup overshoot can be eliminated with the addition of a Soft–Start circuit.

Figure 19. Error Amp Compensation

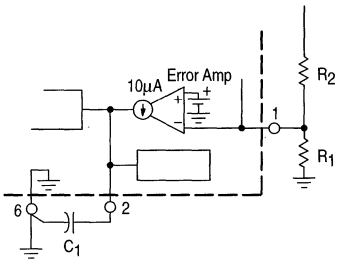
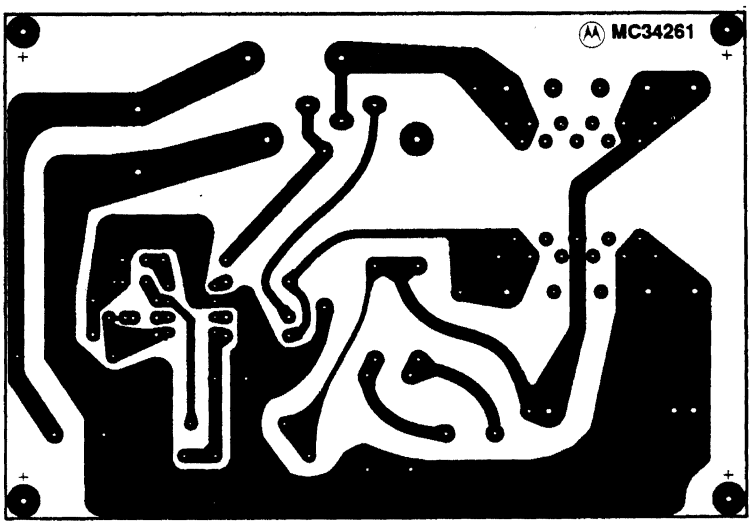
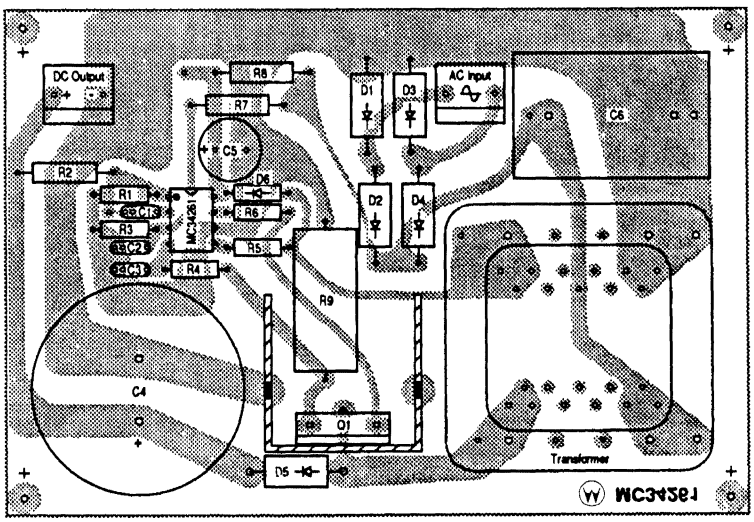


Figure 20. Printed Circuit Board and Component Layout
(Circuits of Figures 15 and 16)





MOTOROLA

MC34262
MC33262

3

POWER FACTOR CONTROLLERS

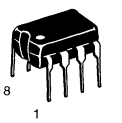
SEMICONDUCTOR TECHNICAL DATA

Power Factor Controllers

The MC34262/MC33262 are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off–line power converter applications. These integrated circuits feature an internal startup timer for stand–alone applications, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, transconductance error amplifier, quickstart circuit for enhanced startup, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of an overvoltage comparator to eliminate runaway output voltage due to load removal, input undervoltage lockout with hysteresis, cycle–by–cycle current limiting, multiplier output clamp that limits maximum peak switch current, an RS latch for single pulse metering, and a drive output high state clamp for MOSFET gate protection. These devices are available in dual–in–line and surface mount plastic packages.

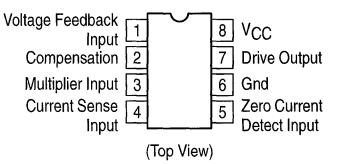
- Overvoltage Comparator Eliminates Runaway Output Voltage
- Internal Startup Timer
- One Quadrant Multiplier
- Zero Current Detector
- Trimmed 2% Internal Bandgap Reference
- Totem Pole Output with High State Clamp
- Undervoltage Lockout with 6.0 V of Hysteresis
- Low Startup and Operating Current
- Supersedes Functionality of SG3561 and TDA4817



P SUFFIX
PLASTIC PACKAGE
CASE 626

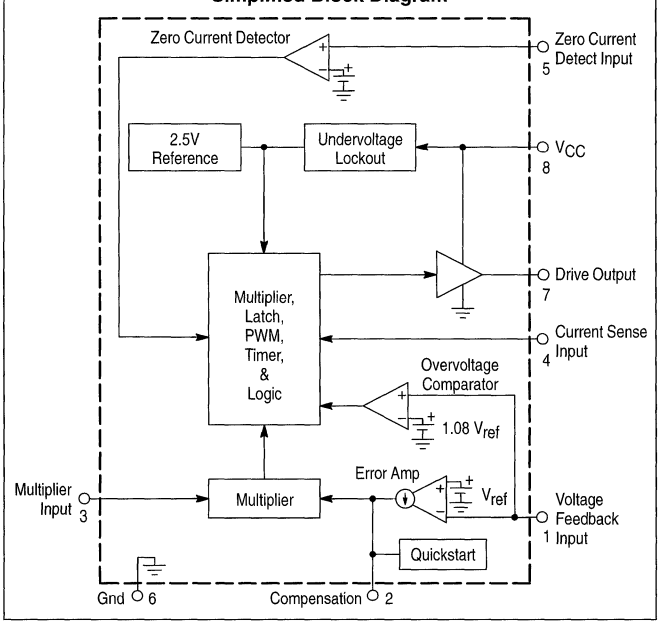
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34262D	T_A = 0° to +85°C	SO–8
MC34262P		Plastic DIP
MC33262D	T_A = –40° to +105°C	SO–8
MC33262P		Plastic DIP

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	500	mA
Current Sense, Multiplier, and Voltage Feedback Inputs	V_{in}	−1.0 to +10	V
Zero Current Detect Input High State Forward Current Low State Reverse Current	I_{in}	 50 −10	mA
Power Dissipation and Thermal Characteristics P Suffix, Plastic Package, Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air D Suffix, Plastic Package, Case 751 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 800 100 450 178	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34262 MC33262	T_A	 0 to + 85 − 40 to +105	°C
Storage Temperature	T_{stg}	− 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V (Note 2), for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Voltage Feedback Input Threshold T_A = 25°C $T_A = T_{low}$ to T_{high} (V_{CC} = 12 V to 28 V)	V_{FB}	 2.465 2.44	 2.5 —	 2.535 2.54	V
Line Regulation (V_{CC} = 12 V to 28 V, T_A = 25°C)	Reg_{line}	—	1.0	10	mV
Input Bias Current (V_{FB} = 0 V)	I_{IB}	—	− 0.1	− 0.5	µA
Transconductance (T_A = 25°C)	g_m	80	100	130	µmho
Output Current Source (V_{FB} = 2.3 V) Sink (V_{FB} = 2.7 V)	I_O	 — —	 10 10	 — —	µA
Output Voltage Swing High State (V_{FB} = 2.3 V) Low State (V_{FB} = 2.7 V)	 $V_{OH(ea)}$ $V_{OL(ea)}$	 5.8 —	 6.4 1.7	 — 2.4	V
OVERVOLTAGE COMPARATOR					
Voltage Feedback Input Threshold	$V_{FB(OV)}$	1.065 V_{FB}	1.08 V_{FB}	1.095 V_{FB}	V
MULTIPLIER					
Input Bias Current, Pin 3 (V_{FB} = 0 V)	I_{IB}	—	− 0.1	− 0.5	µA
Input Threshold, Pin 2	$V_{th(M)}$	1.05 $V_{OL(EA)}$	1.2 $V_{OL(EA)}$	—	V
Dynamic Input Voltage Range Multiplier Input (Pin 3) Compensation (Pin 2)	 $V_{Pin\ 3}$ $V_{Pin\ 2}$	 0 to 2.5 $V_{th(M)}$ to ($V_{th(M)}$ + 1.0)	 0 to 3.5 $V_{th(M)}$ to ($V_{th(M)}$ + 1.5)	 — —	V
Multiplier Gain ($V_{Pin\ 3}$ = 0.5 V, $V_{Pin\ 2} = V_{th(M)}$ + 1.0 V) (Note 4)	K	0.43	0.65	0.87	1/V
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Increasing)	V_{th}	1.33	1.6	1.87	V
Hysteresis (V_{in} Decreasing)	V_H	100	200	300	mV
Input Clamp Voltage High State (I_{DET} = + 3.0 mA) Low State (I_{DET} = − 3.0 mA)	 V_{IH} V_{IL}	 6.1 0.3	 6.7 0.7	 — 1.0	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V (Note 2), for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE COMPARATOR					
Input Bias Current ($V_{Pin\ 4}$ = 0 V)	I_{IB}	—	– 0.15	–1.0	µA
Input Offset Voltage ($V_{Pin\ 2}$ = 1.1 V, $V_{Pin\ 3}$ = 0 V)	V_{IO}	—	9.0	25	mV
Maximum Current Sense Input Threshold (Note 5)	$V_{th(max)}$	1.3	1.5	1.8	V
Delay to Output	$t_{PHL(in/out)}$	—	200	400	ns
DRIVE OUTPUT					
Output Voltage (V_{CC} = 12 V) Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	 V_{OL} V_{OH} 	 — — 9.8 7.8	 0.3 2.4 10.3 8.4	 0.8 3.3 — —	V
Output Voltage (V_{CC} = 30 V) High State (I_{Source} = 20 mA, C_L = 15 pF)	$V_{O(max)}$	14	16	18	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	—	50	120	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	—	50	120	ns
Output Voltage with UVLO Activated (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{O(UVLO)}$	—	0.1	0.5	V
RESTART TIMER					
Restart Time Delay	t_{DLY}	200	620	—	µs
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	11.5	13	14.5	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{Shutdown}$	7.0	8.0	9.0	V
Hysteresis	V_H	3.8	5.0	6.2	V
TOTAL DEVICE					
Power Supply Current Startup (V_{CC} = 7.0 V) Operating Dynamic Operating (50 kHz, C_L = 1.0 nF)	I_{CC} 	 — — —	 0.25 6.5 9.0	 0.4 12 20	mA
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	—	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the startup threshold before setting to 12 V.
3. T_{low} = 0°C for MC34262 = – 40°C for MC33262 T_{high} = + 85°C for MC34262 = +105°C for MC33262
4. $K = \dfrac{\text{Pin 4 Threshold}}{V_{Pin\ 3}\,(V_{Pin\ 2} - V_{th(M)})}$
5. This parameter is measured with V_{FB} = 0 V, and $V_{Pin\ 3}$ = 3.0 V

Figure 1. Current Sense Input Threshold versus Multiplier Input

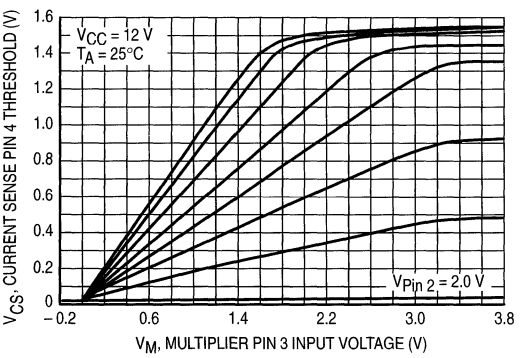


Figure 2. Current Sense Input Threshold versus Multiplier Input, Expanded View

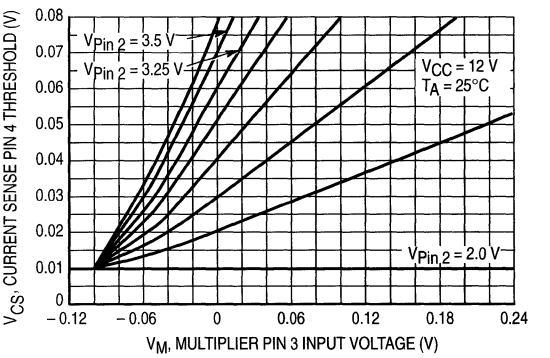


Figure 3. Voltage Feedback Input Threshold Change versus Temperature

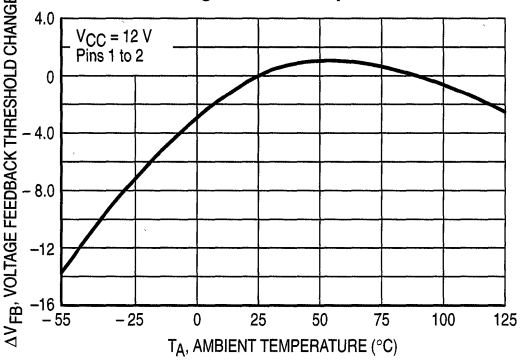


Figure 4. Overvoltage Comparator Input Threshold versus Temperature

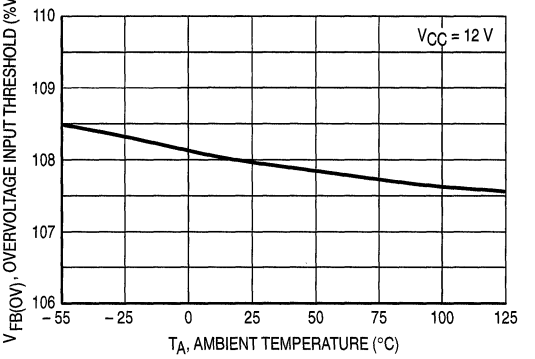


Figure 5. Error Amp Transconductance and Phase versus Frequency

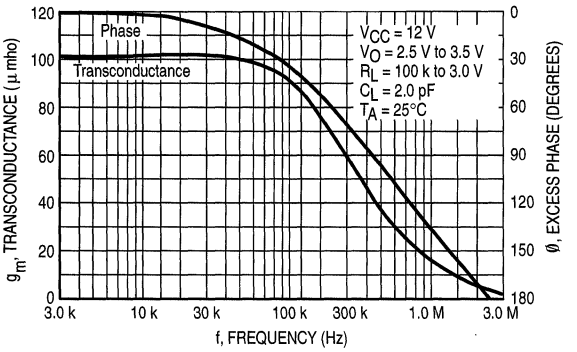


Figure 6. Error Amp Transient Response

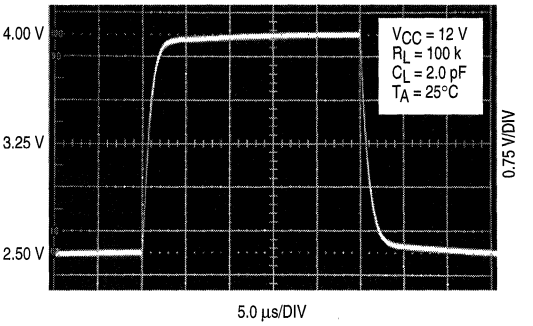


Figure 7. Quickstart Charge Current versus Temperature

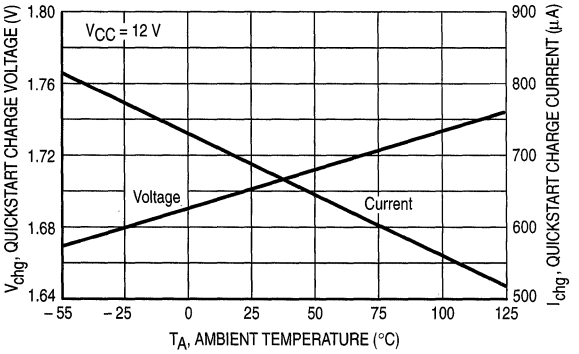


Figure 8. Restart Timer Delay versus Temperature

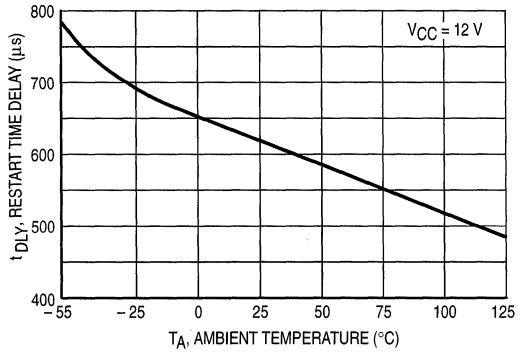


Figure 9. Zero Current Detector Input Threshold Voltage versus Temperature

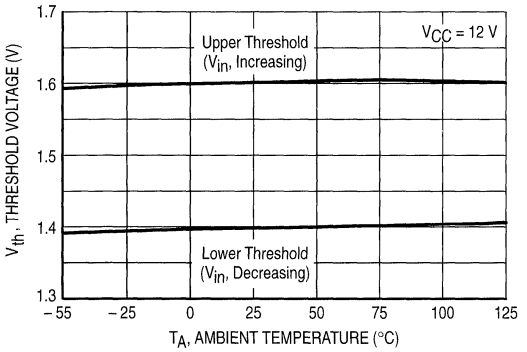


Figure 10. Output Saturation Voltage versus Load Current

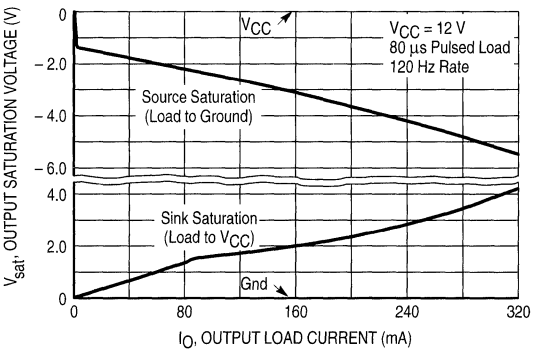


Figure 11. Drive Output Waveform

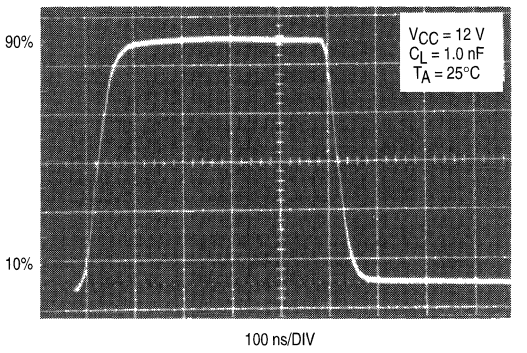


Figure 12. Drive Output Cross Conduction

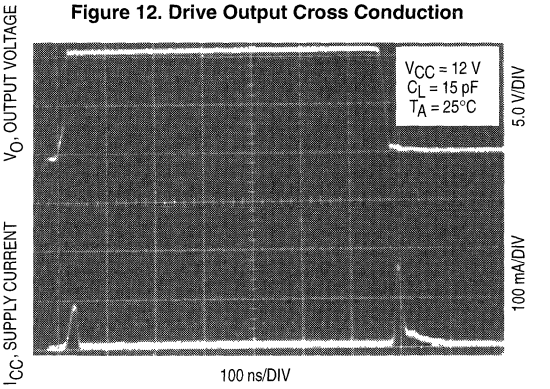


Figure 13. Supply Current versus Supply Voltage

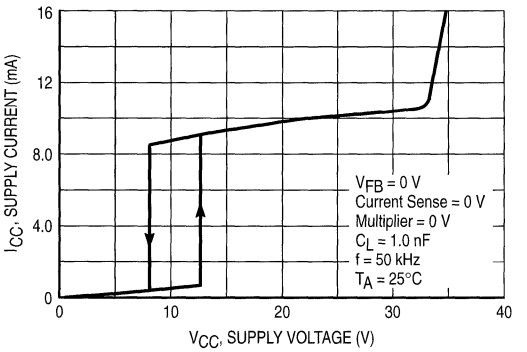
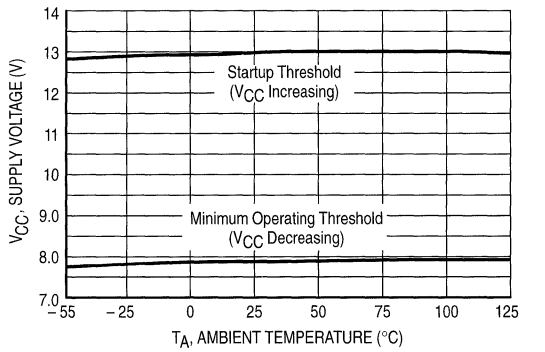


Figure 14. Undervoltage Lockout Thresholds versus Temperature



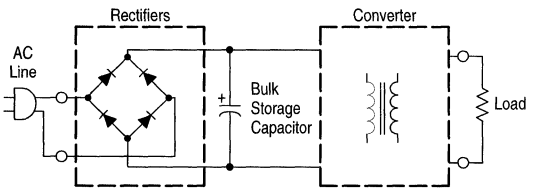
FUNCTIONAL DESCRIPTION

Introduction

With the goal of exceeding the requirements of legislation on line–current harmonic content, there is an ever increasing demand for an economical method of obtaining a unity power factor. This data sheet describes a monolithic control IC that was specifically designed for power factor control with minimal external components. It offers the designer a simple, cost–effective solution to obtain the benefits of active power factor correction.

Most electronic ballasts and switching power supplies use a bridge rectifier and a bulk storage capacitor to derive raw dc voltage from the utility ac line, Figure 15.

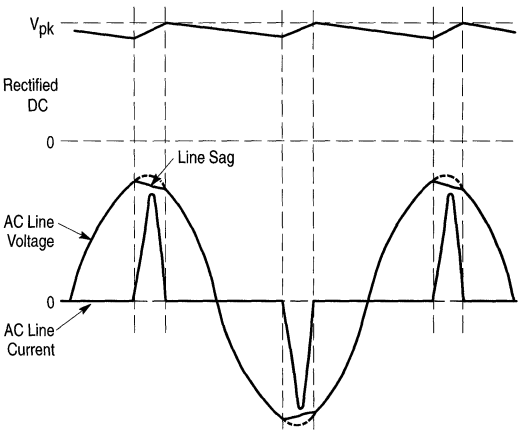
Figure 15. Uncorrected Power Factor Circuit



This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike, Figure 16. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power. Power factor ratios of 0.5 to 0.7 are common.

Power factor correction can be achieved with the use of either a passive or an active input circuit. Passive circuits usually contain a combination of large capacitors, inductors, and rectifiers that operate at the ac line frequency. Active circuits incorporate some form of a high frequency switching converter for the power processing, with the boost converter being the most popular topology, Figure 17. Since active input circuits operate at a frequency much higher than that of the ac line, they are smaller, lighter in weight, and more efficient than a passive circuit that yields similar results. With proper control of the preconverter, almost any complex load can be made to appear resistive to the ac line, thus significantly reducing the harmonic current content.

Figure 16. Uncorrected Power Factor Input Waveforms

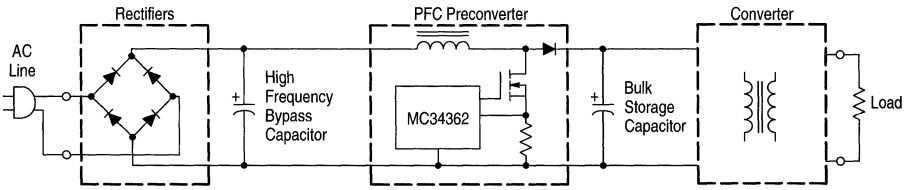


The MC34262, MC33262 are high performance, critical conduction, current–mode power factor controllers specifically designed for use in off–line active preconverters. These devices provide the necessary features required to significantly enhance poor power factor loads by keeping the ac line current sinusoidal and in phase with the line voltage.

Operating Description

The MC34262, MC33262 contain many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. There are, however, two areas where there is a major difference when compared to popular devices such as the UC3842 series. Referring to the block diagram in Figure 19, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. The reasons for these differences will become apparent in the following discussion. A description of each of the functional blocks is given below.

Figure 17. Active Power Factor Correction Preconverter



Error Amplifier

An Error Amplifier with access to the inverting input and output is provided. The amplifier is a transconductance type, meaning that it has high output impedance with controlled voltage–to–current gain. The amplifier features a typical gm of 100 μmhos (Figure 5). The noninverting input is internally biased at 2.5 V ± 2.0% and is not pinned out. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is – 0.5 μA, which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R_2. The Error Amp output is internally connected to the Multiplier and is pinned out (Pin 2) for external loop compensation. Typically, the bandwidth is set below 20 Hz, so that the amplifier's output voltage is relatively constant over a given ac line cycle. In effect, the error amp monitors the average output voltage of the converter over several line cycles. The Error Amp output stage was designed to have a relatively constant transconductance over temperature. This allows the designer to define the compensated bandwidth over the intended operating temperature range. The output stage can sink and source 10 μA of current and is capable of swinging from 1.7 V to 6.4 V, assuring that the Multiplier can be driven over its entire dynamic range.

A key feature to using a transconductance type amplifier, is that the input is allowed to move independently with respect to the output, since the compensation capacitor is connected to ground. This allows dual usage of of the Voltage Feedback Input pin by the Error Amplifier and by the Overvoltage Comparator.

Overvoltage Comparator

An Overvoltage Comparator is incorporated to eliminate the possibility of runaway output voltage. This condition can occur during initial startup, sudden load removal, or during output arcing and is the result of the low bandwidth that must be used in the Error Amplifier control loop. The Overvoltage Comparator monitors the peak output voltage of the converter, and when exceeded, immediately terminates MOSFET switching. The comparator threshold is internally set to 1.08 V_{ref}. In order to prevent false tripping during normal operation, the value of the output filter capacitor C_3 must be large enough to keep the peak–to–peak ripple less than 16% of the average dc output. The Overvoltage Comparator input to Drive Output turn–off propagation delay is typically 400 ns. A comparison of startup overshoot without and with the Overvoltage Comparator circuit is shown in Figure 23.

Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The ac full wave rectified haversines are monitored at Pin 3 with respect to ground while the Error Amp output at Pin 2 is monitored with respect to the Voltage Feedback Input threshold. The Multiplier is designed to have an extremely linear transfer curve over a wide dynamic range, 0 V to 3.2 V for Pin 3, and 2.0 V to 3.75 V for Pin 2, Figure 1. The Multiplier output controls the Current Sense Comparator threshold as the ac voltage traverses sinusoidally from zero to peak line, Figure 18. This has the effect of forcing the MOSFET on–time to track the input line voltage, resulting in a fixed Drive Output on–time, thus making the preconverter load appear to be resistive to the ac line. An approximation of the Current Sense Comparator threshold can be calculated from the following equation. This equation is accurate only under the given test condition stated in the electrical table.

$$V_{CS}, \text{ Pin 4 Threshold} \approx 0.65\,(V_{Pin\ 2} - V_{th(M)})\,V_{Pin\ 3}$$

A significant reduction in line current distortion can be attained by forcing the preconverter to switch as the ac line voltage crosses through zero. The forced switching is achieved by adding a controlled amount of offset to the Multiplier and Current Sense Comparator circuits. The equation shown below accounts for the built–in offsets and is accurate to within ten percent. Let $V_{th(M)} = 1.991$ V

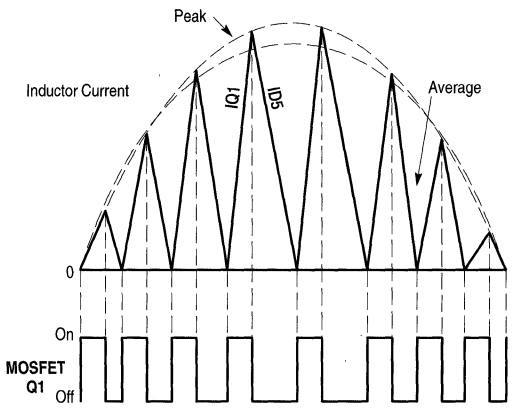
$$V_{CS}, \text{ Pin 4 Threshold} = 0.544\,(V_{Pin\ 2} - V_{th(M)})\,V_{Pin\ 3} + 0.0417\,(V_{Pin\ 2} - V_{th(M)})$$

Zero Current Detector

The MC34262 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on–time by setting the RS Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn–on until the inductor current reaches zero, the output rectifier reverse recovery time becomes less critical, allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous, thus limiting the peak switch to twice the average input current.

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.4 V. To prevent false tripping, 200 mV of hysteresis is provided. Figure 9 shows that the thresholds are well–defined over temperature. The Zero Current Detector input is internally protected by two clamps. The upper 6.7 V clamp prevents input overvoltage breakdown while the lower 0.7 V clamp prevents substrate injection. Current limit protection of the lower clamp transistor is provided in the event that the input pin is accidentally shorted to ground. The Zero Current Detector input to Drive Output turn–on propagation delay is typically 320 ns.

Figure 18. Inductor Current and MOSFET Gate Voltage Waveforms



Current Sense Comparator and RS Latch

The Current Sense Comparator RS Latch configuration used ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground–referenced sense resistor R_7 in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input and compared to a level derived from the Multiplier output. The peak inductor current under normal operating conditions is controlled by the threshold voltage of Pin 4 where:

$$I_{L(pk)} = \frac{\text{Pin 4 Threshold}}{R_7}$$

Abnormal operating conditions occur during preconverter startup at extremely high line or if output voltage sensing is lost. Under these conditions, the Multiplier output and Current Sense threshold will be internally clamped to 1.5 V. Therefore, the maximum peak switch current is limited to:

$$I_{pk(max)} = \frac{1.5\ V}{R_7}$$

An internal RC filter has been included to attenuate any high frequency noise that may be present on the current waveform. This filter helps reduce the ac line current distortion especially near the zero crossings. With the component values shown in Figure 20, the Current Sense Comparator threshold, at the peak of the haversine varies from 1.1 V at 90 Vac to 100 mV at 268 Vac. The Current Sense Input to Drive Output turn–off propagation delay is typically less than 200 ns.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand–alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 620 μs after the inductor current reaches zero. The restart time delay versus temperature is shown in Figure 8.

Undervoltage Lockout and Quickstart

An Undervoltage Lockout comparator has been incorporated to guarantee that the IC is fully functional before enabling the output stage. The positive power supply terminal (V_{CC}) is monitored by the UVLO comparator with the upper threshold set at 13 V and the lower threshold at 8.0 V. In the stand–by mode, with V_{CC} at 7.0 V, the required supply current is less than 0.4 mA. This large hysteresis and low startup current allow the implementation of efficient bootstrap startup techniques, making these devices ideally suited for wide input range off–line preconverter applications. An internal 36 V clamp has been added from V_{CC} to ground to protect the IC and capacitor C_4 from an overvoltage condition. This feature is desirable if external circuitry is used to delay the startup of the preconverter. The supply current, startup, and operating voltage characteristics are shown in Figures 13 and 14.

A Quickstart circuit has been incorporated to optimize converter startup. During initial startup, compensation capacitor C_1 will be discharged, holding the error amp output below the Multiplier threshold. This will prevent Drive Output switching and delay bootstrapping of capacitor C_4 by diode D_6. If Pin 2 does not reach the multiplier threshold before C_4 discharges below the lower UVLO threshold, the converter will "hiccup" and experience a significant startup delay. The Quickstart circuit is designed to precharge C_1 to 1.7 V, Figure 7. This level is slightly below the Pin 2 Multiplier threshold, allowing immediate Drive Output switching and bootstrap operation when C_4 crosses the upper UVLO threshold.

Drive Output

The MC34262/MC33262 contain a single totem–pole output stage specifically designed for direct drive of power MOSFETs. The Drive Output is capable of up to ± 500 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull–down resistor. The totem–pole output has been optimized to minimize cross–conduction current during high speed operation. The addition of two 10 Ω resistors, one in series with the source output transistor and one in series with the sink output transistor, helps to reduce the cross–conduction current and radiated noise by limiting the output rise and fall time. A 16 V clamp has been incorporated into the output stage to limit the high state V_{OH}. This prevents rupture of the MOSFET gate when V_{CC} exceeds 20 V.

APPLICATIONS INFORMATION

The application circuits shown in Figures 19, 20 and 21 reveal that few external components are required for a complete power factor preconverter. Each circuit is a peak detecting current–mode boost converter that operates in critical conduction mode with a fixed on–time and variable off–time. A major benefit of critical conduction operation is that the current loop is inherently stable, thus eliminating the need for ramp compensation. The application in Figure 19 operates over an input voltage range of 90 Vac to 138 Vac and provides an output power of 80 W (230 V at 350 mA) with an associated power factor of approximately 0.998 at nominal line. Figures 20 and 21 are universal input preconverter examples that operate over a continuous input voltage range of 90 Vac to 268 Vac. Figure 20 provides an output power of 175 W (400 V at 440 mA) while Figure 21 provides 450 W (400 V at 1.125 A). Both circuits have an observed worst–case power factor of approximately 0.989. The input current and voltage waveforms of Figure 20 are shown in Figure 22 with operation at 115 Vac and 230 Vac. The data for each of the applications was generated with the test set–up shown in Figure 24.

Table 1. Design Equations

Notes	Calculation	Formula
Calculate the maximum required output power.	Required Converter Output Power	$P_O = V_O I_O$
Calculated at the minimum required ac line voltage for output regulation. Let the efficiency $\eta = 0.92$ for low line operation.	Peak Inductor Current	$I_{L(pk)} = \frac{2\sqrt{2}\,P_O}{\eta Vac_{(LL)}}$
Let the switching cycle t = 40 μs for universal input (85 to 265 Vac) operation and 20 μs for fixed input (92 to 138 Vac, or 184 to 276 Vac) operation.	Inductance	$L_P = \frac{t\left(\frac{V_O}{\sqrt{2}} - Vac_{(LL)}\right)\eta\, Vac_{(LL)}^2}{\sqrt{2}\,V_O\,P_O}$
In theory the on–time t_{on} is constant. In practice t_{on} tends to increase at the ac line zero crossings due to the charge on capacitor C_5. Let Vac = $Vac_{(LL)}$ for initial t_{on} and t_{off} calculations.	Switch On–Time	$t_{on} = \frac{2\,P_O\,L_P}{\eta\, Vac^2}$
The off–time t_{off} is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.	Switch Off–Time	$t_{off} = \frac{t_{on}}{\frac{V_O}{\sqrt{2}\,Vac\,\lvert Sin\,\theta\rvert} - 1}$
The minimum switching frequency occurs at the peak of the ac line voltage. As the ac line voltage traverses from peak to zero, t_{off} approaches zero producing an increase in switching frequency.	Switching Frequency	$f = \frac{1}{t_{on} + t_{off}}$
Set the current sense threshold V_{CS} to 1.0 V for universal input (85 Vac to 265 Vac) operation and to 0.5 V for fixed input (92 Vac to 138 Vac, or 184 Vac to 276 Vac) operation. Note that V_{CS} must be <1.4 V.	Peak Switch Current	$R_7 = \frac{V_{CS}}{I_{L(pk)}}$
Set the multiplier input voltage V_M to 3.0 V at high line. Empirically adjust V_M for the lowest distortion over the ac line voltage range while guaranteeing startup at minimum line.	Multiplier Input Voltage	$V_M = \frac{Vac\,\sqrt{2}}{\left(\frac{R_5}{R_3} + 1\right)}$
The $I_{IB}\,R_1$ error term can be minimized with a divider current in excess of 50 μA.	Converter Output Voltage	$V_O = V_{ref}\left(\frac{R_2}{R_1} + 1\right) - I_{IB}\,R_2$
The calculated peak–to–peak ripple must be less than 16% of the average dc output voltage to prevent false tripping of the Overvoltage Comparator. Refer to the Overvoltage Comparator text. ESR is the equivalent series resistance of C_3	Converter Output Peak to Peak Ripple Voltage	$\Delta V_{O(pp)} = I_O\sqrt{\left(\frac{1}{2\pi f_{ac}\,C_3}\right)^2 + ESR^2}$
The bandwidth is typically set to 20 Hz. When operating at high ac line, the value of C_1 may need to be increased. (See Figure 25)	Error Amplifier Bandwidth	$BW = \frac{gm}{2\,\pi\,C_1}$

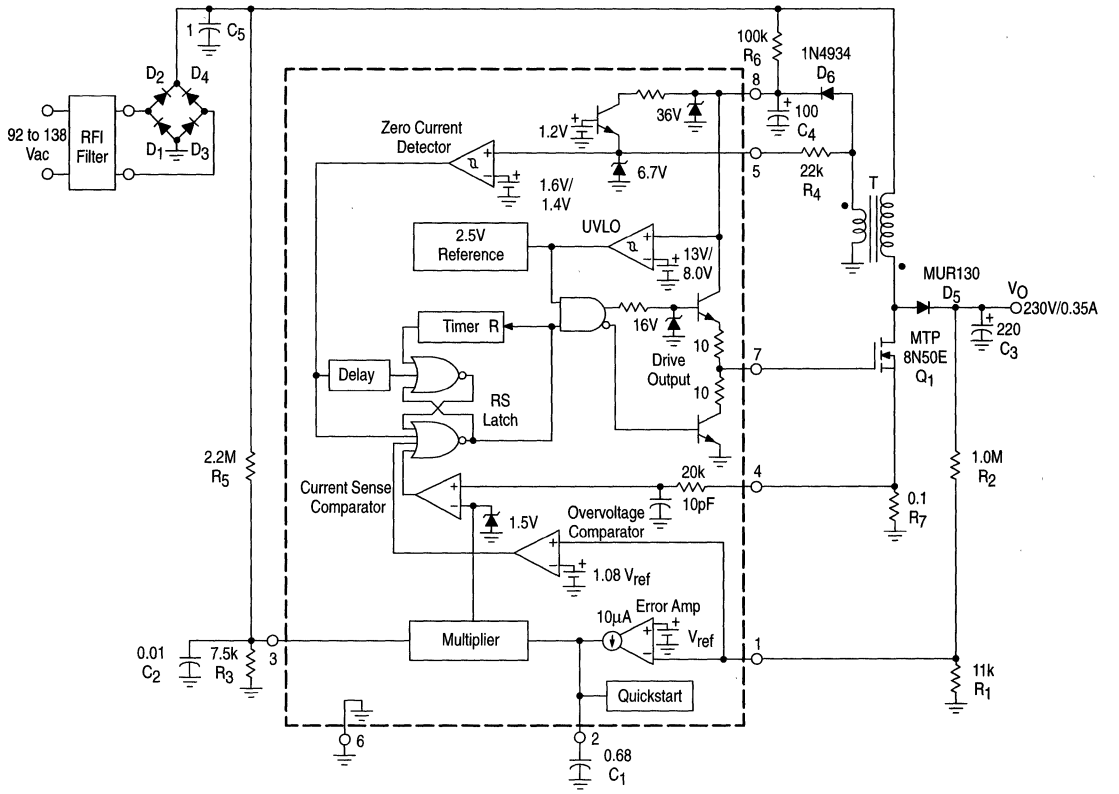
The following converter characteristics must be chosen:

V_O — Desired output voltage Vac — AC RMS line voltage

I_O — Desired output current $Vac_{(LL)}$ — AC RMS low line voltage

ΔV_O — Converter output peak–to–peak ripple voltage

Figure 19. 80 W Power Factor Controller



Power Factor Controller Test Data

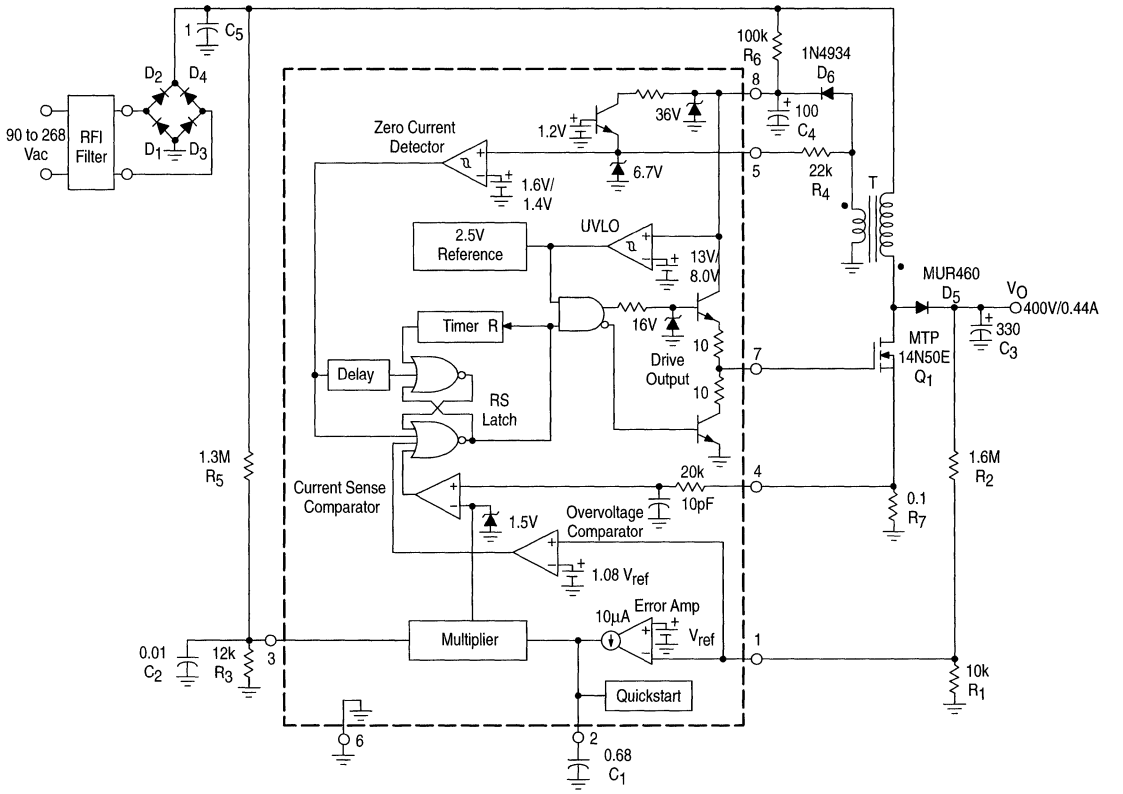
AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	η(%)
90	85.9	0.999	0.93	2.6	0.08	1.6	0.84	0.95	4.0	230.7	0.350	80.8	94.0
100	85.3	0.999	0.85	2.3	0.13	1.0	1.2	0.73	4.0	230.7	0.350	80.8	94.7
110	85.1	0.998	0.77	2.2	0.10	0.58	1.5	0.59	4.0	230.7	0.350	80.8	94.9
120	84.7	0.998	0.71	3.0	0.09	0.73	1.9	0.58	4.1	230.7	0.350	80.8	95.3
130	84.4	0.997	0.65	3.9	0.12	1.7	2.2	0.61	4.1	230.7	0.350	80.8	95.7
138	84.1	0.996	0.62	4.6	0.16	2.4	2.3	0.60	4.1	230.7	0.350	80.8	96.0

This data was taken with the test set–up shown in Figure 24.

T = Coilcraft N2881–A
Primary: 62 turns of # 22 AWG
Secondary: 5 turns of # 22 AWG
Core: Coilcraft PT2510, EE 25
Gap: 0.072″ total for a primary inductance (L_P) of 320 µH

Heatsink = AAVID Engineering Inc. 590302B03600, or 593002B03400

Figure 20. 175 W Universal Input Power Factor Controller



Power Factor Controller Test Data

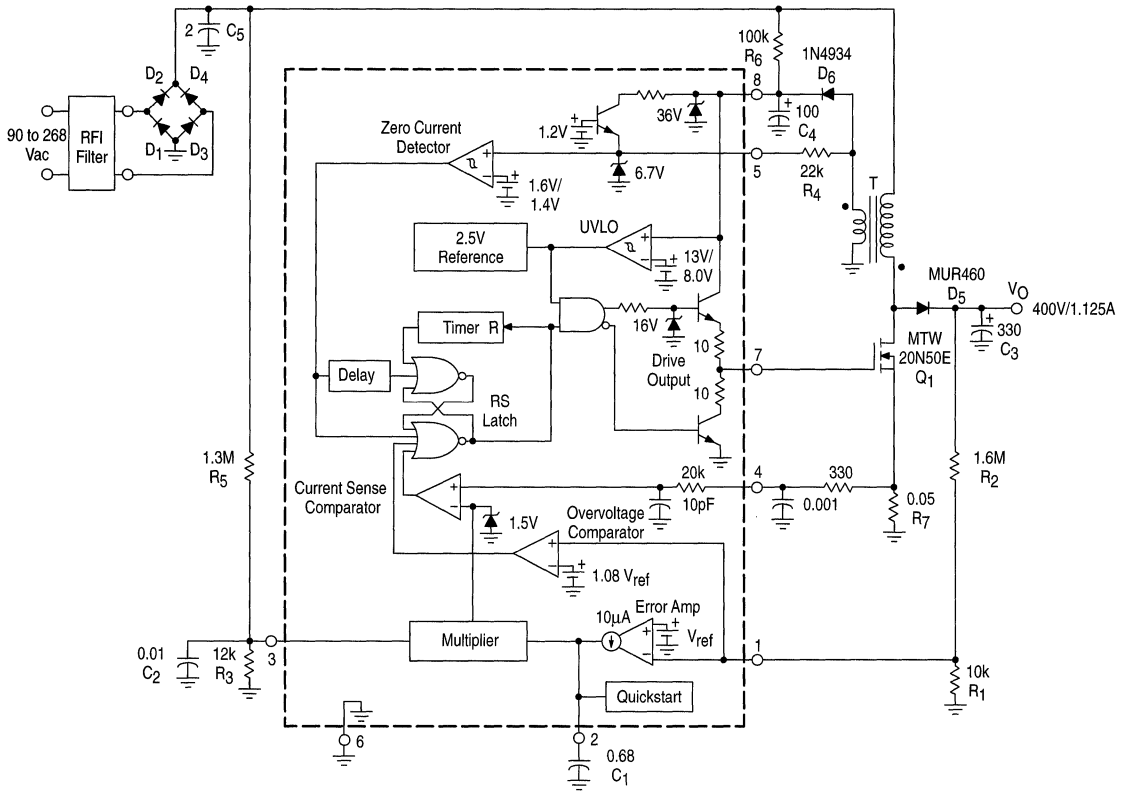
AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	η(%)
90	193.3	0.991	2.15	2.8	0.18	2.6	0.55	1.0	3.3	402.1	0.44	176.9	91.5
120	190.1	0.998	1.59	1.6	0.10	1.4	0.23	0.72	3.3	402.1	0.44	176.9	93.1
138	188.2	0.999	1.36	1.2	0.12	1.3	0.65	0.80	3.3	402.1	0.44	176.9	94.0
180	184.9	0.998	1.03	2.0	0.10	0.49	1.2	0.82	3.4	402.1	0.44	176.9	95.7
240	182.0	0.993	0.76	4.4	0.09	1.6	2.3	0.51	3.4	402.1	0.44	176.9	97.2
268	180.9	0.989	0.69	5.9	0.10	2.3	2.9	0.46	3.4	402.1	0.44	176.9	97.8

This data was taken with the test set–up shown in Figure 24.

T = Coilcraft N2880–A
Primary: 78 turns of # 16 AWG
Secondary: 6 turns of # 18 AWG
Core: Coilcraft PT4215, EE 42–15
Gap: 0.104″ total for a primary inductance (L_P) of 870 µH

Heatsink = AAVID Engineering Inc. 590302B03600

Figure 21. 450 W Universal Input Power Factor Controller



Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	η(%)
90	489.5	0.990	5.53	2.2	0.10	1.5	0.25	0.83	8.8	395.5	1.14	450.9	92.1
120	475.1	0.998	3.94	2.5	0.12	0.29	0.62	0.52	8.8	395.5	1.14	450.9	94.9
138	470.6	0.998	3.38	2.1	0.06	0.70	1.1	0.41	8.8	395.5	1.14	450.9	95.8
180	463.4	0.998	2.57	4.1	0.21	2.0	1.6	0.71	8.9	395.5	1.14	450.9	97.3
240	460.1	0.996	1.91	4.8	0.14	4.3	2.2	0.63	8.9	395.5	1.14	450.9	98.0
268	459.1	0.995	1.72	5.8	0.10	5.0	2.5	0.61	8.9	395.5	1.14	450.9	98.2

This data was taken with the test set–up shown in Figure 24.

T = Coilcraft P3657–A
Primary: 38 turns Litz wire, 1300 strands of #48 AWG, Kerrigan–Lewis, Chicago, IL
Secondary: 3 turns of # 20 AWG
Core: Coilcraft PT4220, EE 42–20
Gap: 0.180″ total for a primary inductance (L_P) of 190 µH

Heatsink = AAVID Engineering Inc. 604953B04000 Extrusion

Figure 22. Power Factor Corrected Input Waveforms (Figure 20 Circuit)

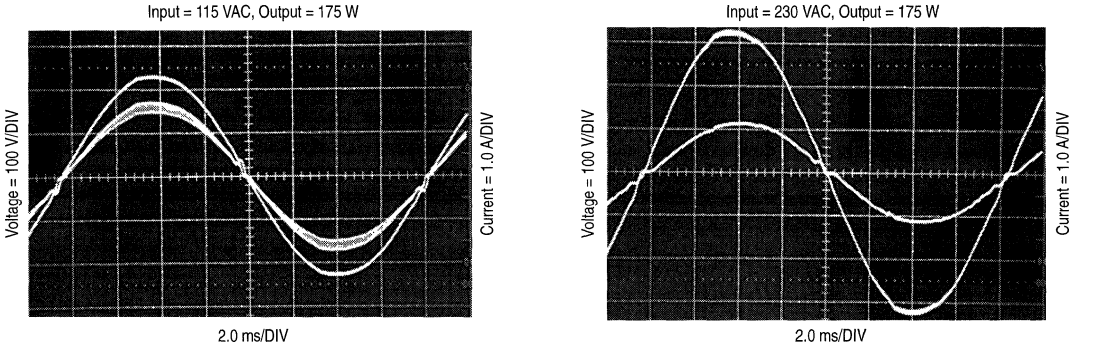


Figure 23. Output Voltage Startup Overshoot (Figure 20 Circuit)

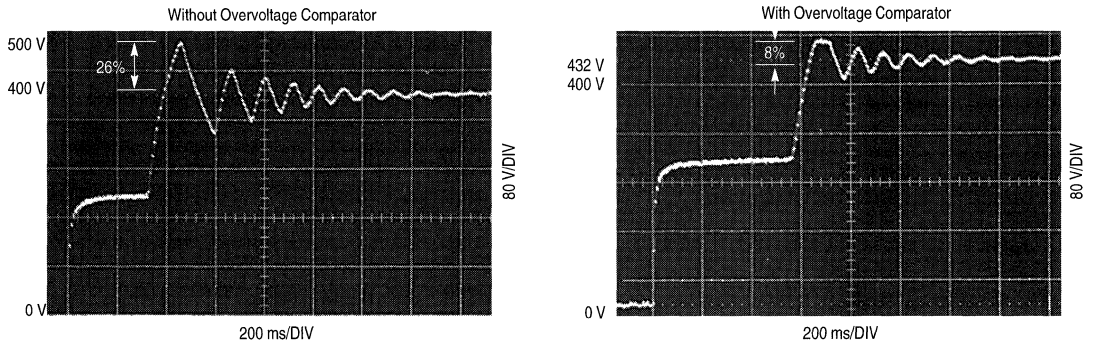
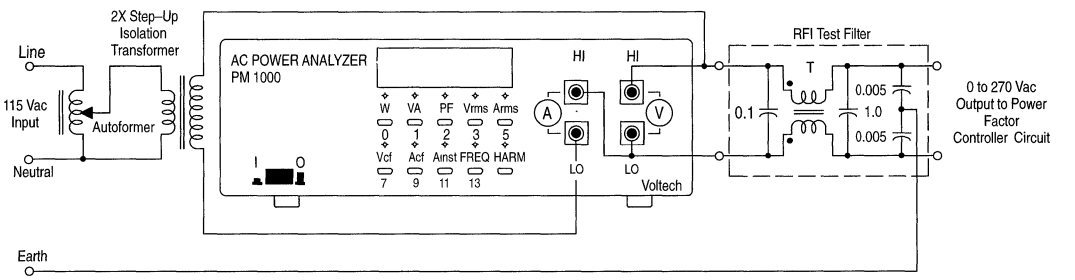


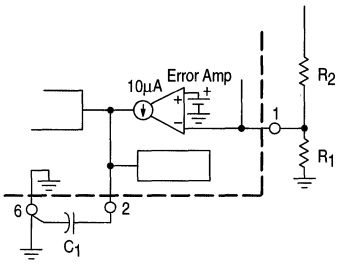
Figure 24. Power Factor Test Set–Up



An RFI filter is required for best performance when connecting the preconverter directly to the ac line. The filter attenuates the level of high frequency switching that appears on the ac line current waveform. Figures 19 and 20 work well with commercially available two stage filters such as the Delta Electronics 03DPCG5. Shown above is a single stage test filter that can easily be constructed with four ac line rated capacitors and a common–mode transformer. Coilcraft CMT3–28–2 was used to test Figures 19 and 20. It has a minimum inductance of 28 mH and a maximum current rating of 2.0 A. Coilcraft CMT4–17–9 was used to test Figure 21. It has a minimum inductance of 17 mH and a maximum current rating of 9.0 A. Circuit conversion efficiency η (%) was calculated without the power loss of the RFI filter.

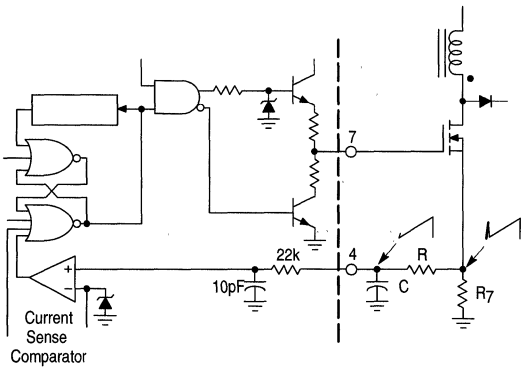
3

Figure 25. Error Amp Compensation



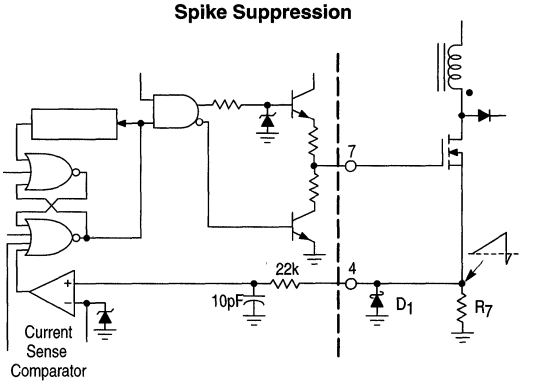
The Error Amp output is a high impedance node and is susceptible to noise pickup. To minimize pickup, compensation capacitor C_1 must be connected as close to Pin 2 as possible with a short, heavy ground returning directly to Pin 6. When operating at high ac line, the voltage at Pin 2 may approach the lower threshold of the Multiplier, ≈ 2.0 V. If there is excessive ripple on Pin 2, the Multiplier will be driven into cut–off causing circuit instability, high distortion and poor power factor. This problem can be eliminated by increasing the value of C_1.

Figure 26. Current Waveform Spike Suppression



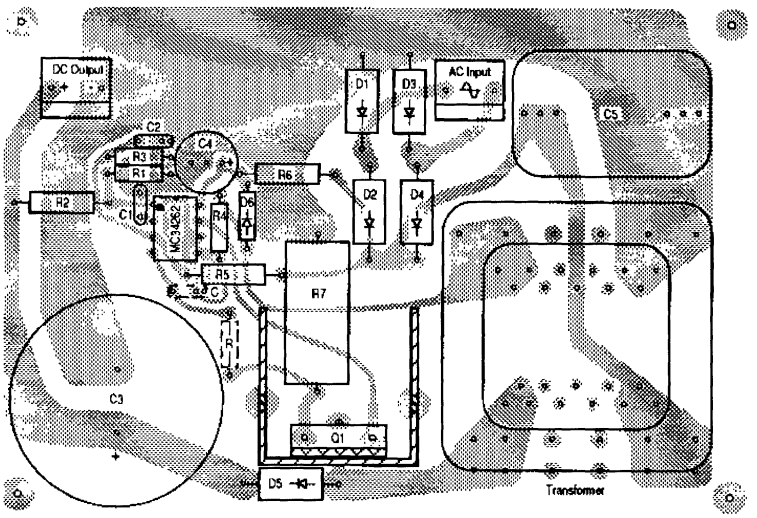
A narrow turn–on spike is usually present on the leading edge of the current waveform and can cause circuit instability. The MC34262 provides an internal RC filter with a time constant of 220 ns. An additional external RC filter may be required in universal input applications that are above 200 W. It is suggested that the external filter be placed directly at the Current Sense Input and have a time constant that approximates the spike duration.

Figure 27. Negative Current Waveform Spike Suppression

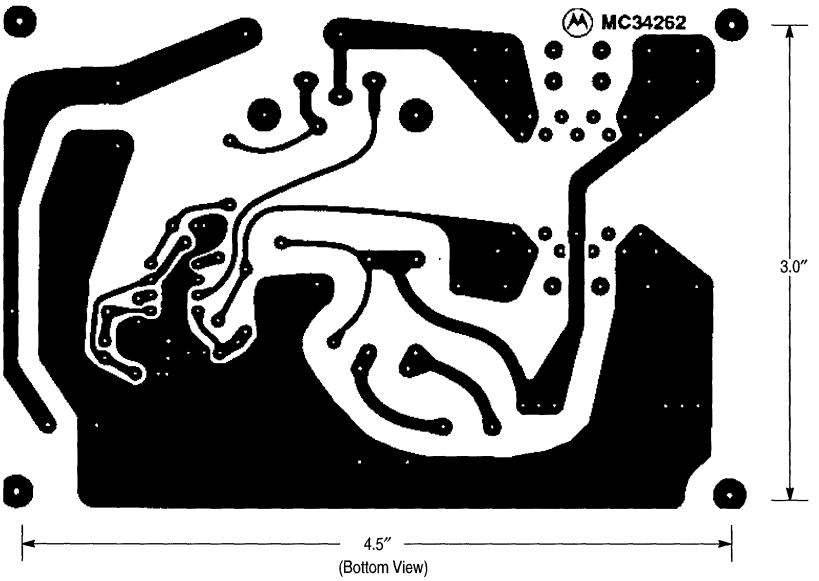


A negative turn–off spike can be observed on the trailing edge of the current waveform. This spike is due to the parasitic inductance of resistor R_7, and if it is excessive, it can cause circuit instability. The addition of Shottky diode D_1 can effectively clamp the negative spike. The addition of the external RC filter shown in Figure 26 may provide sufficient spike attenuation.

Figure 28. Printed Circuit Board and Component Layout (Circuits of Figures 15 and 16)



(Top View)



(Bottom View)

NOTE: Use 2 oz. copper laminate for optimum circuit performance.

MC34268

SCSI-2 Active Terminator Regulator

3

The MC34268 is a medium current, low dropout positive voltage regulator specifically designed for use in SCSI–2 active termination circuits. This device offers the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum. The regulator consists of a 1.0 V dropout composite PNP/NPN pass transistor, current limiting, and thermal limiting. These devices are packaged in the 8–pin SOP–8 and 3–pin DPAK surface mount power packages.

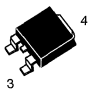
Applications include active SCSI–2 terminators and post regulation of switching power supplies.

- 2.85 V Output Voltage for SCSI–2 Active Termination
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to 1.4% Tolerance
- No Minimum Load Required
- Space Saving DPAK and SOP–8 Surface Mount Power Packages

SCSI–2 ACTIVE TERMINATOR REGULATOR

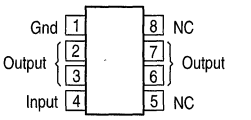
SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)



DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)

PIN CONNECTIONS

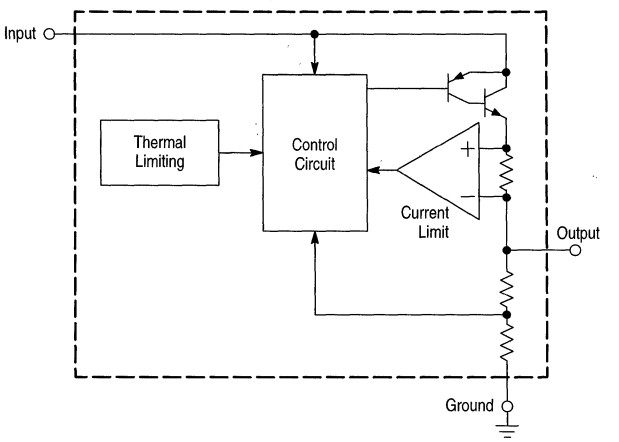


(Top View)

Pin 1. Ground
2. Output
3. Input
4. Output

(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34268D	T_J = 0° to +125°C	SOP–8
MC34268DT		DPAK

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{in}	15	V
Power Dissipation and Thermal Characteristics			
DT Suffix, Plastic Package, Case 369A			
T_A = 25°C, Derate Above T_A = 25°C	P_D	Internally Limted	W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	87	°C/W
D Suffix, Plastic Package, Case 751			
T_A = 25°C, Derate Above T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	22	°C/W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	140	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Storage Temperature	T_{stg}	– 55 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{in} = 4.25 V, C_O = 10 µF, for typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C, I_O = 0 mA) Output Voltage, over Line, Load, and Temperature (V_{in} = 3.9 V to 15 V, I_O = 0 mA to 490 mA)	V_O	2.81 2.76	2.85 2.85	2.89 2.93	V
Line Regulation (V_{in} = 4.25 V to 15 V, I_O = 0 mA, T_J = 25°C)	Reg_{line}	—	—	0.3	%
Load Regulation (I_O = 0 mA to 800 mA, T_J = 25°C)	Reg_{load}	—	—	0.5	%
Dropout Voltage (I_O = 490 mA)	$V_{in} - V_O$	—	0.95	1.1	V
Ripple Rejection (f = 120 Hz)	RR	55	—	—	dB
Maximum Output Current (V_{in} = 5.0 V)	$I_{(max)}$	800	—	—	mA
Bias Current (V_{in} = 4.25 V, I_O = 0 mA)	I_B	—	5.0 to 3.0	8.0	mA
Minimum Load Current to maintain Regulation (V_{in} = 15 V)	$I_{L(min)}$	—	—	0	mA

Figure 1. Dropout Voltage versus Output Load Current

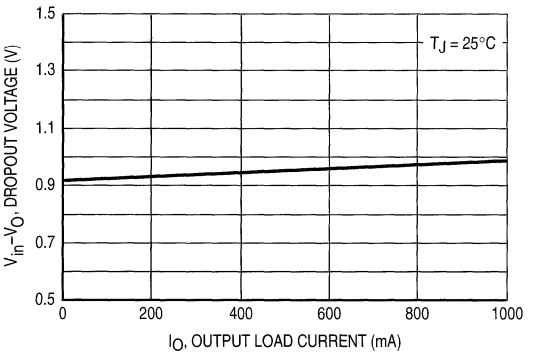


Figure 2. Transient Load Regulation

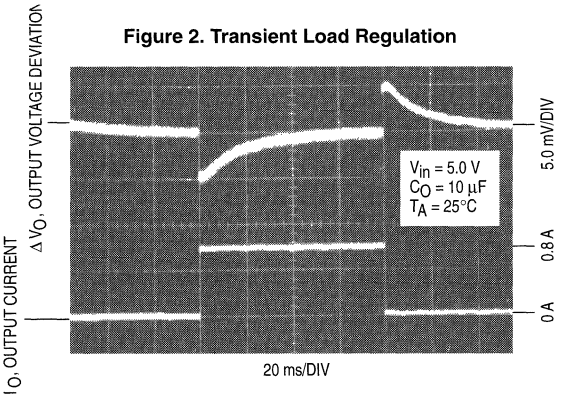


Figure 3. Typical SCSI Application

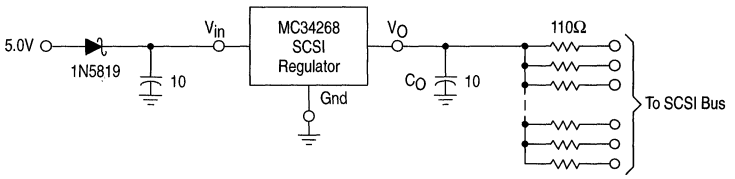


Figure 3 is a circuit of a typical SCSI terminator application. The MC34268 is designed specifically to provide 2.85 V required to drive a SCSI–2 bus. The output current capability of the regulator is in excess of 800 mA; enough to drive standard SCSI–2, fast SCSI–2, and some wide SCSI–2 applications. The typical dropout voltage is less than 1.0 V, allowing the IC to regulate to input voltages less than 4.0 V. Internal protective features include current and thermal limiting.

The MC34268 requires an external 10 μF capacitor with an ESR of less than 10 Ω for stability over temperature. With economical electrolytic capacitors, cold temperature operation can pose a stability problem. As temperature decreases, the capacitance also decreases and the ESR increases, which could cause the circuit to oscillate. Tantalum capacitors may be a better choice if small size is a requirement. Also, the capacitance and ESR of a tantalum capacitor is more stable over temperature.

Figure 4. SOP–8 Thermal Resistance versus P.C.B. Copper Length

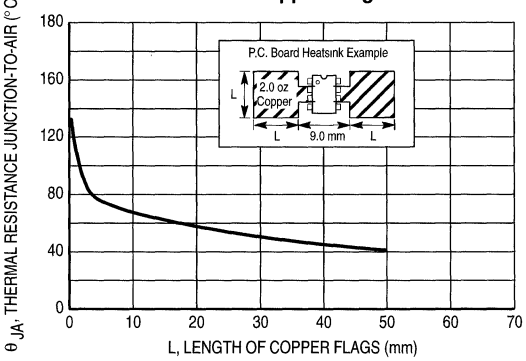
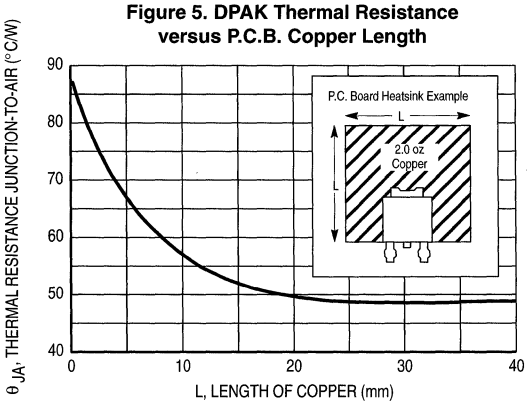


Figure 5. DPAK Thermal Resistance versus P.C.B. Copper Length



MOTOROLA

MC34270
MC34271

Liquid Crystal Display and Backlight Integrated Controller

3

LIQUID CRYSTAL DISPLAY AND BACKLIGHT INTEGRATED CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

The MC34270 and MC34271 are low power dual switching voltage regulators, specifically designed for handheld and laptop applications, to provide several regulated output voltages using a minimum of external parts. Two uncommitted switching regulators feature a very low standby bias current of 5.0 μA, and an operating current of 7.0 mA capable of supplying output currents in excess of 200 mA.

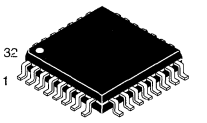
Both devices have three additional features. The first is an ELD Output that can be used to drive a backlight or a liquid crystal display. The ELD output frequency is the clock divided by 256. The second feature allows four additional output bias voltages, in specific proportions to V_B, one of the switching regulated output voltages. It allows use of mixed logic circuitry and provides a voltage bias for N–Channel load control MOSFETs™. The third feature is an Enable input that allows a logic level signal to turn–"off" or turn–"on" both switching regulators.

Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC34270 and MC34271 Features:

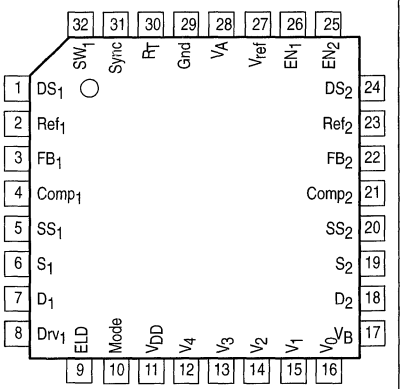
- Low Standby Bias Current of 5.0 μA
- Uncommitted Switching Regulators Allow Both Positive and Negative Supply Voltages
- Logic Enable Allows Microprocessor Control of All Outputs
- Synchronizable to External Clock
- Mode Commandable for ELD and LCD Interface
- Frequency Synchronizable
- Auxiliary Output Bias Voltages Enable Load Control via N–Channel FETs

MOSFET is a trademark of Motorola, Inc.



FB SUFFIX
PLASTIC PACKAGE
CASE 873

PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

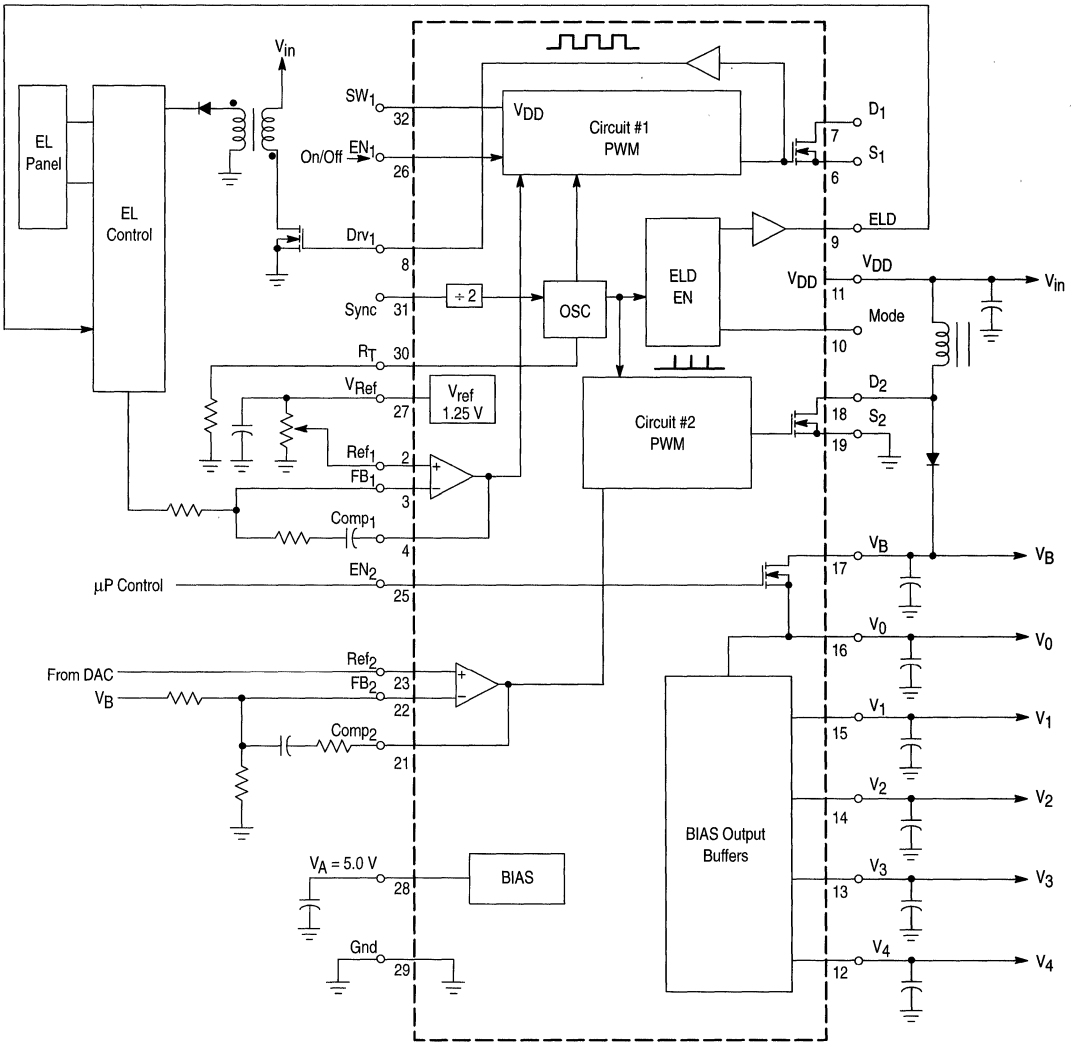
Rating	Symbol	Value	Unit
Input Voltage	V_{DD}	16	Vdc
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation	P_D	1.43	W
Case 873			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	100	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	60	°C/W
Output #1 and #2 Switch Current	I_{SL} & I_{SB}	500	mA
Output #1 and #2 "Off"–State Voltage	V_{SL}	60	Vdc
Feedback Enable MOSFETs "Off"–State Voltage	V_{LF}	20	Vdc
Operating Junction Temperature	T_J	125	°C
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34270FB	T_A = 0° to +70°C	QFP–32
MC34271FB		QFP–32

3

Representative Block Diagram



This device contains 350 active transistors.

ELECTRICAL CHARACTERISTICS (V_{DD} = 6.0 V, for typical values T_A = Low to High [Note 1], for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (T_J = 25°C)	V_{ref}	1.225	1.250	1.275	V
Line Regulation (V_{DD} = 5.0 V to 12.5 V)	Reg_{line}	–	2.0	10	mV
Load Regulation (I_O = 0 to 120 μA)	Reg_{load}	–	2.0	10	mV
Total Variation (Line, Load and Temperature)	V_{ref}	1.215	–	1.285	V
ERROR AMPLIFIERS					
Input Offset Voltage (V_{CM} = 1.25 V)	V_{IO}	–	1.0	10	mV
Input Bias Current (V_{CM} = 1.25 V)	I_{IB}	–	120	600	nA
Open Loop Voltage Gain (V_{CM} = 1.25 V, V_{COMP} = 2.0 V)	A_{VOL}	80	100	–	dB
Output Voltage Swing					V
High State (I_{OH} = –100 μA)	Ve_{OH}	V_A–1.5	4.0	5.5	
Low State (I_{OL} = 100 μA)	Ve_{OL}	0	–	1.0	
BIAS VOLTAGE					
Voltage (V_{DD} = 5.0 V to 12.5 V, I_O = 0)	V_A	4.6	5.0	5.4	V
OSCILLATOR AND PWM SECTIONS					
Total Frequency Variation Over Line and Temperature	f_{OSC}				kHz
V_{DD} = 5.0 V to 10 V, T_A = 0° to 70°C, R_T = 169 k		90	115	140	
Duty Cycle at Each Output					%
Maximum	DC_{max}	92	95	–	
Minimum	DC_{min}	–	–	0	
Sync Input					
Input Resistance (V_{sync} = 3.5 V)	R_{sync}	25	50	100	kΩ
Minimum Sync Pulse Width	T_p	–	1.0	–	μs
OUTPUT MOSFETs					
Output Voltage – "On"–State (I_{sink} = 200 mA)	V_{OL}	–	150	250	mV
Output Current – "Off"–State (V_{OH} = 40 V)	I_{OH}	–	0.1	1.0	μA
Rise and Fall Times	t_r, t_f	–	50	–	ns
EL DISCHARGE OUTPUT (ELD) AND DRV_1					
Output Voltage – "On"–State (I_{sink} = 100 μA)	V_{OL}	–	30	100	mV
Output Voltage – "On"–State (I_{sink} = 50 mA)	V_{OL}	–	2.0	2.5	V
Output Voltage – "Off"–State (I_{source} = –100 μA)	V_{OH}	V_{DD}–0.5	5.9	–	V
Output Voltage – "Off"–State (I_{source} = –50 mA)	V_{OH}	V_{DD}–3.5	3.3	–	V
FEEDBACK ENABLE SWITCHES (DS_1, DS_2)					
Output Voltage – "Low"–State (I_{sink} = 1.0 mA)	Vfe_{OL}	–	10	100	mV
Output Current – "Off"–State (V_{OH} = 12.5 V)	Ife_{OH}	–	0.6	1.0	μA
SWITCHED V_{DD} OUTPUT (SW_1)					
Output Voltage					V
Switch "On" (EN_1 = 1, I_{source} = 100 μA)	Vsw_{OH}	5.5	5.9	6.0	
Switch "Off" (EN_1 = 0, I_{sink} = 100 μA)	Vsw_{OL}	0	0.1	0.2	
AUXILIARY VOLTAGE OUTPUTS					
V_0 Enable Switch					
"On"–Resistance: V_B to V_0	Rds	0	2.0	10	Ω
"Off"–State Leakage Current (V_B = 10 V)	I_{lkg}	0	0.1	2.0	μA
V_0 Voltage (V_B = 30 V, I_{source} = 0 mA)	V_0	29.5	29.9	30	V
V_0 Resistance (I_{source} = 4.0 mA)	R_0	20	40	60	Ω

NOTE: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (continued) (V_{DD} = 6.0 V, for typical values T_A = Low to High [Note 1], for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
AUXILIARY VOLTAGE OUTPUTS						
V_1, V_2, V_3, V_4 Outputs						
1–V_1/V_0 Ratio:	MC34270		0.0565	0.0580	0.0595	
	MC34271		0.0500	0.0520	0.0535	
1–V_2/V_0 Ratio:	MC34270		0.1135	0.1160	0.1185	
	MC34271		0.1010	0.1035	0.1065	
V_3/V_0 Ratio:	MC34270		0.1135	0.1160	0.1185	
	MC34271		0.1010	0.1035	0.1065	
V_4/V_0 Ratio:	MC34270		0.0565	0.0580	0.0595	
	MC34271		0.0500	0.0520	0.0535	
Output Resistance (I_{source} = 4.0 mA)		R_o	20	40	60	Ω
Output Short Circuit Current		I_{ss}	5.0	10	20	mA
LOGIC INPUTS (EN_1, EN_2, MODE)						
Input Low State		V_{IL}	0	–	0.8	V
Input High State		V_{IH}	2.0	–	6.0	V
Input Impedance		R_{in}	25	50	100	kΩ
SOFT START CONTROL (SS_1,SS_2)						
Charge Current (Capacitor Voltage = 1.0 V to 4.0 V)		I_{chg}	0.5	1.0	2.5	µA
Discharge Current (Capacitor Voltage = 1.0 V)		I_{dschg}	250	650	–	µA
TOTAL SUPPLY CURRENT						
V_{DD} Current Standby Mode (EN_1 = EN_2 = 0)	V_{DD} = 6.0 V V_{DD} = 16 V	I_{CC}	– –	2.0 3.0	5.0 15	µA
V_{DD} Current Backlight "On" (EN_1 = 1; EN_2 = 0)		I_{CC}	–	0.7	3.0	mA
V_{DD} Current LCD "On" (No Inductor) (EN_1 = 0; EN_2 = 1)		I_{CC}	–	0.9	2.0	mA
V_B Current (V_0 = 35 V)		I_O	–	1.2	3.0	mA

NOTE: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Switch Output Duty Cycle versus Compensation Voltage

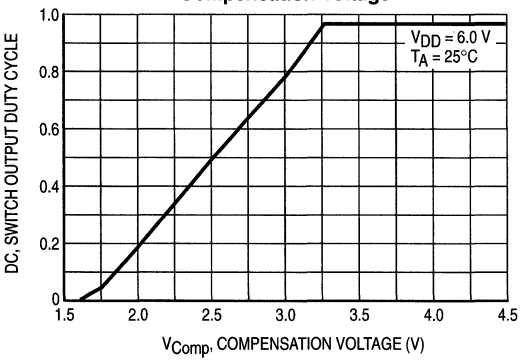


Figure 2. Error Amp Open Loop Gain and Phase versus Frequency

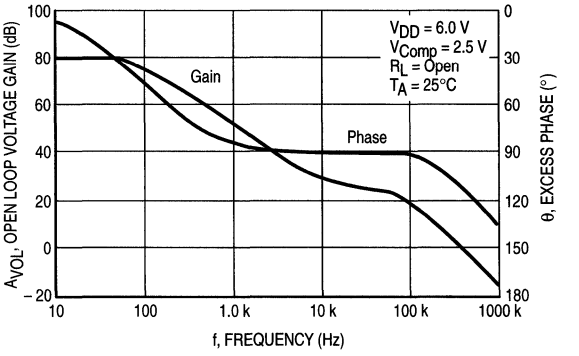


Figure 3. Reference Voltage Change versus Reference Current

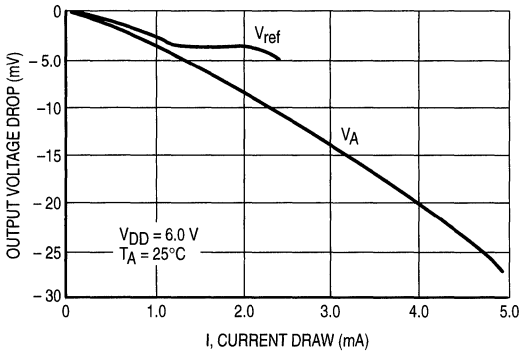


Figure 4. Quiescent Current versus Supply Voltage

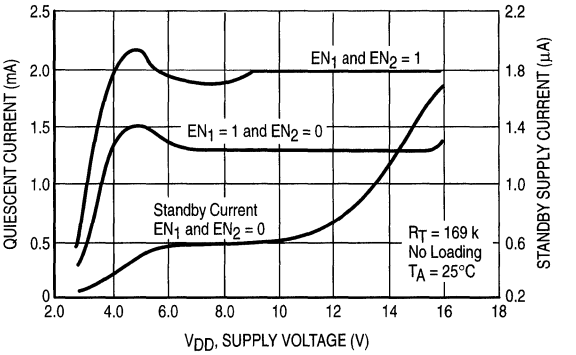


Figure 5. FET Drain Voltage versus Sink Current

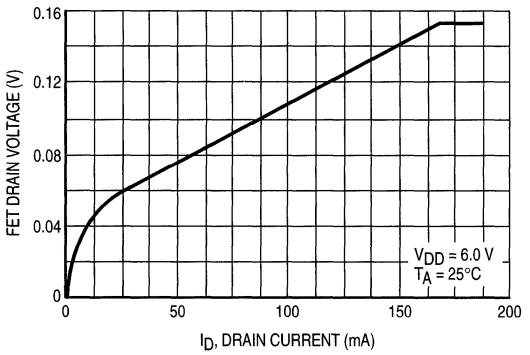


Figure 6. ELD and DRV1 Switch Output Source and Sink Saturation versus Current

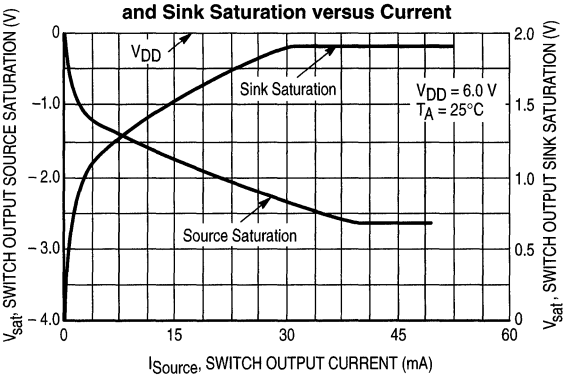


Figure 7. V_{ref} and V_A Variation versus Temperature

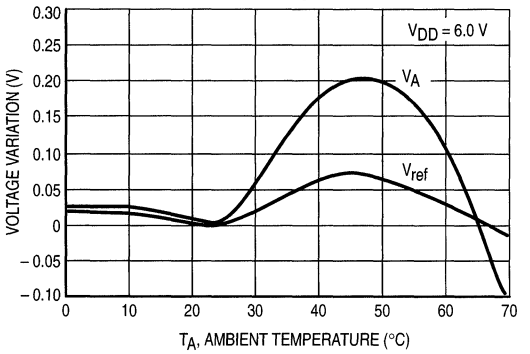


Figure 8. Oscillator Frequency Variation versus Temperature

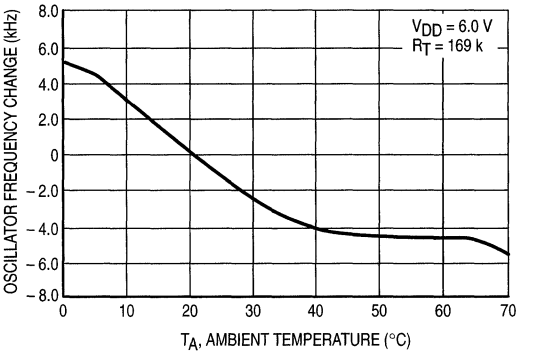


Figure 9. Frequency versus Timing

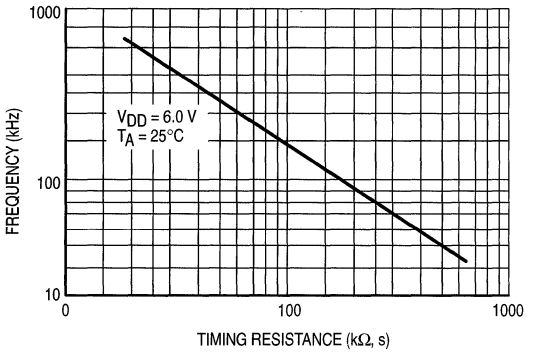
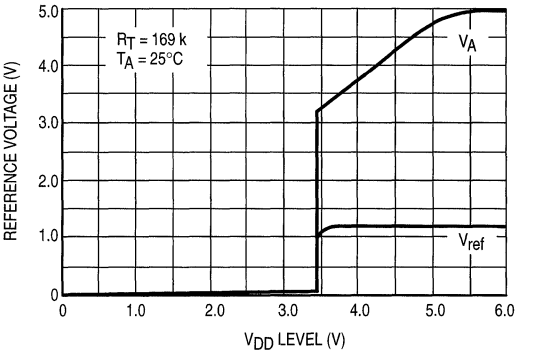


Figure 10. V_A, V_{ref} versus V_{DD}



OPERATING DESCRIPTION

The MC34270 and MC34271 series are monolithic, fixed frequency power switching regulators specifically designed for dc to dc converter and battery powered applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step–up, step–down and voltage inverting converters with a minimum number of external components. Potential markets include battery powered, handheld, automotive, computer, industrial and cost sensitive consumer products. A description of each section is given below with the representative block diagram shown in Figure 9.

Oscillator

The oscillator frequency is programmed by resistor R_T. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the switch outputs. During the fall time of the internal sawtooth waveform, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gates high, disabling the output switching MOSFETs. The internal sawtooth waveform has a nominal peak voltage of 3.3 V and a valley voltage of 1.7 V.

Pulse Width Modulators

Both pulse width modulators consist of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied to the inverting input. A third input to the comparator has a 0.5 mA typical current source that can be used to implement soft start. Output switch conduction is initiated when the ramp waveform is discharged to the valley voltage. As the ramp voltage increases to a voltage that exceeds the error amplifier output, the latch resets, terminating output MOSFET conduction for the duration of the oscillator ramp. This PWM/latch combination prevents multiple output pulses during a given oscillator cycle.

Each PWM circuit is enabled by a logic input. When disabled, the entire block is turned off, drawing only leakage current from the power source. Shared circuits, like the reference and oscillator, can be activated by either EN_1 or EN_2.

Circuit #1 has an ELD output which may be used to drive an LCD or backlight. Its output frequency is the oscillator frequency divided by 1024.

Error Amplifiers and Reference

Each error amplifier is provided with access to both inverting and noninverting inputs, and the output. The Error Amplifiers' Common Mode Input Range is 0 to 2.5 V. The amplifiers have a minimum dc voltage gain of 60 dB. The 1.25 V reference has an accuracy of ±4.0% at room temperature.

External loop compensation is required for converter stability. A simple low–pass filter is formed by connecting a resistive divider from the output to the error amplifier inverting input, and a series resistor–capacitor from the error amplifier output also to the to the inverting input. The step down converter is easiest to compensate for stability. The step–up and voltage inverting configurations, when operated as continuous conduction boost or flyback converters, are more difficult to compensate, and may require a lower loop design bandwidth.

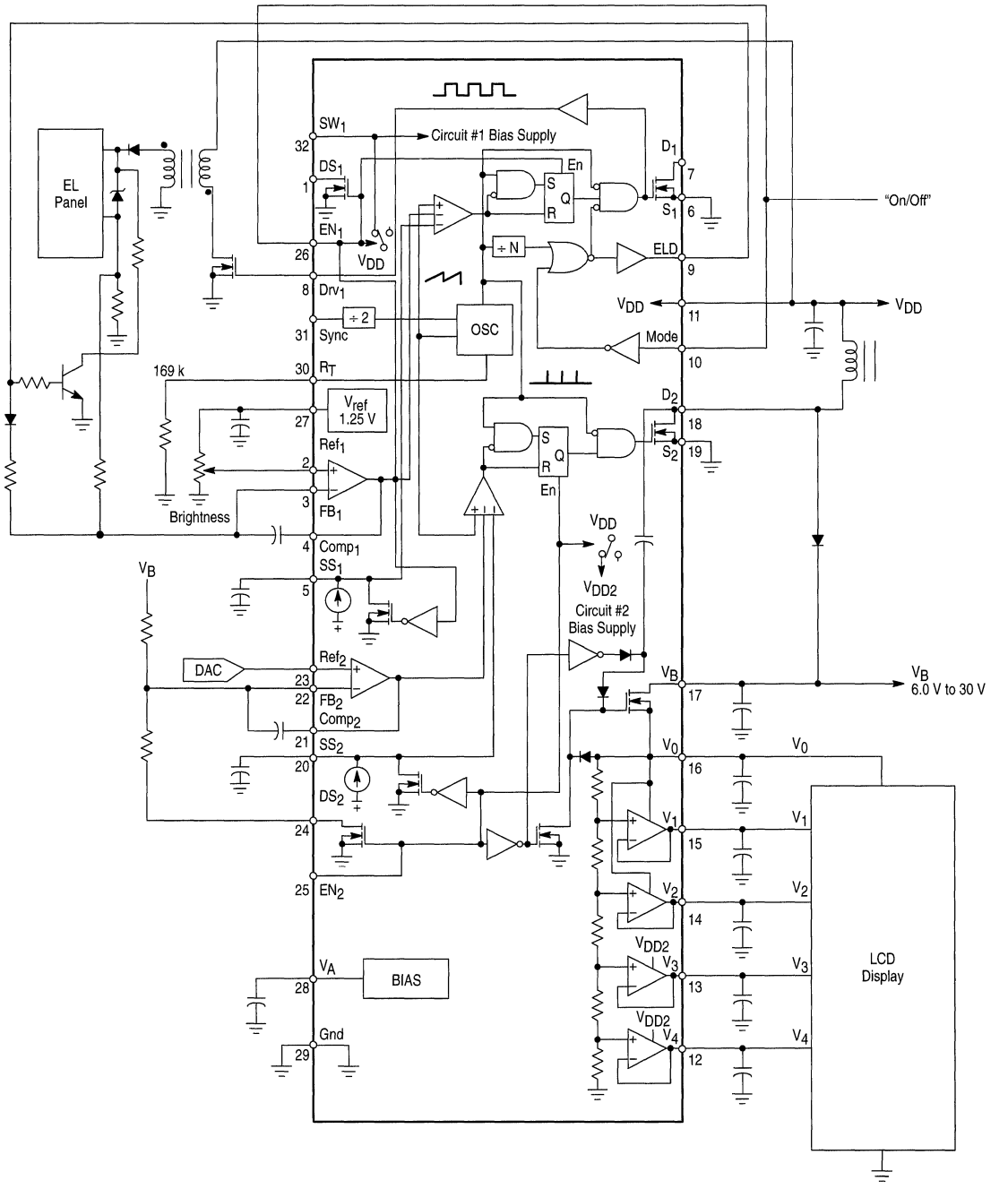
MOSFET Switch Outputs

The output MOSFETs are designed to switch a maximum of 60 V, with a peak drain current capability of 500 mA. In circuit #1 an additional DRV_1 output is provided for interfacing with an external MOSFET.The gates of the MOSFETs are held low when the circuit is disabled.

Auxiliary Output Voltages

Output voltages V_0 through V_4 are provided for use as references or bias voltages. V_0 is the circuit #2 output voltage, when an internal FET switch is activated. The other auxiliary output voltages are proportional to V_B. The amplifiers for V_1 and V_2 are powered from V_0, while the amplifiers for V_3 and V_4 are powered from V_{DD}.

Figure 11. Representative Block Diagram Electroluminescent Backlight Configuration



3

Figure 12. Auxiliary Supply Configuration

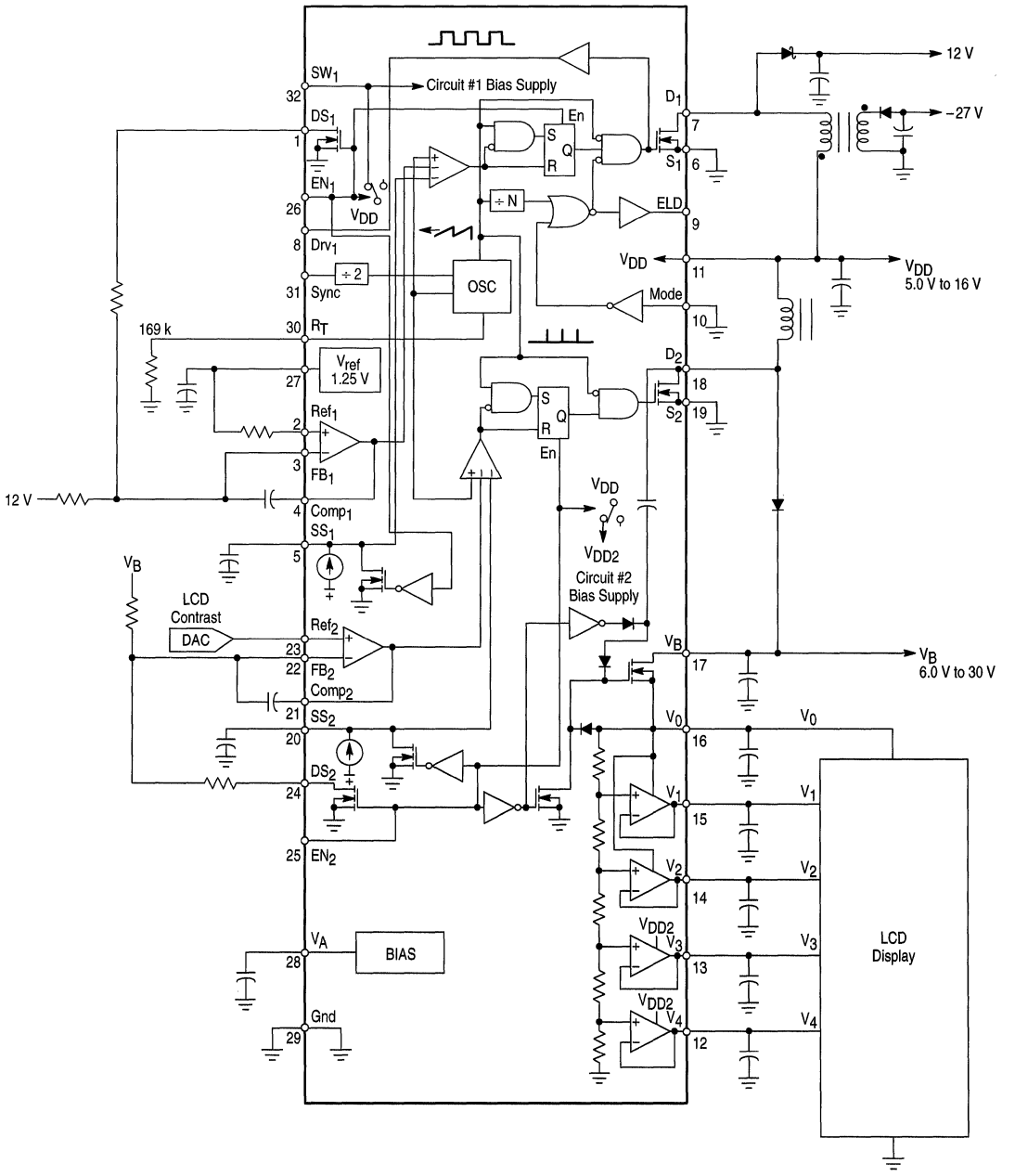
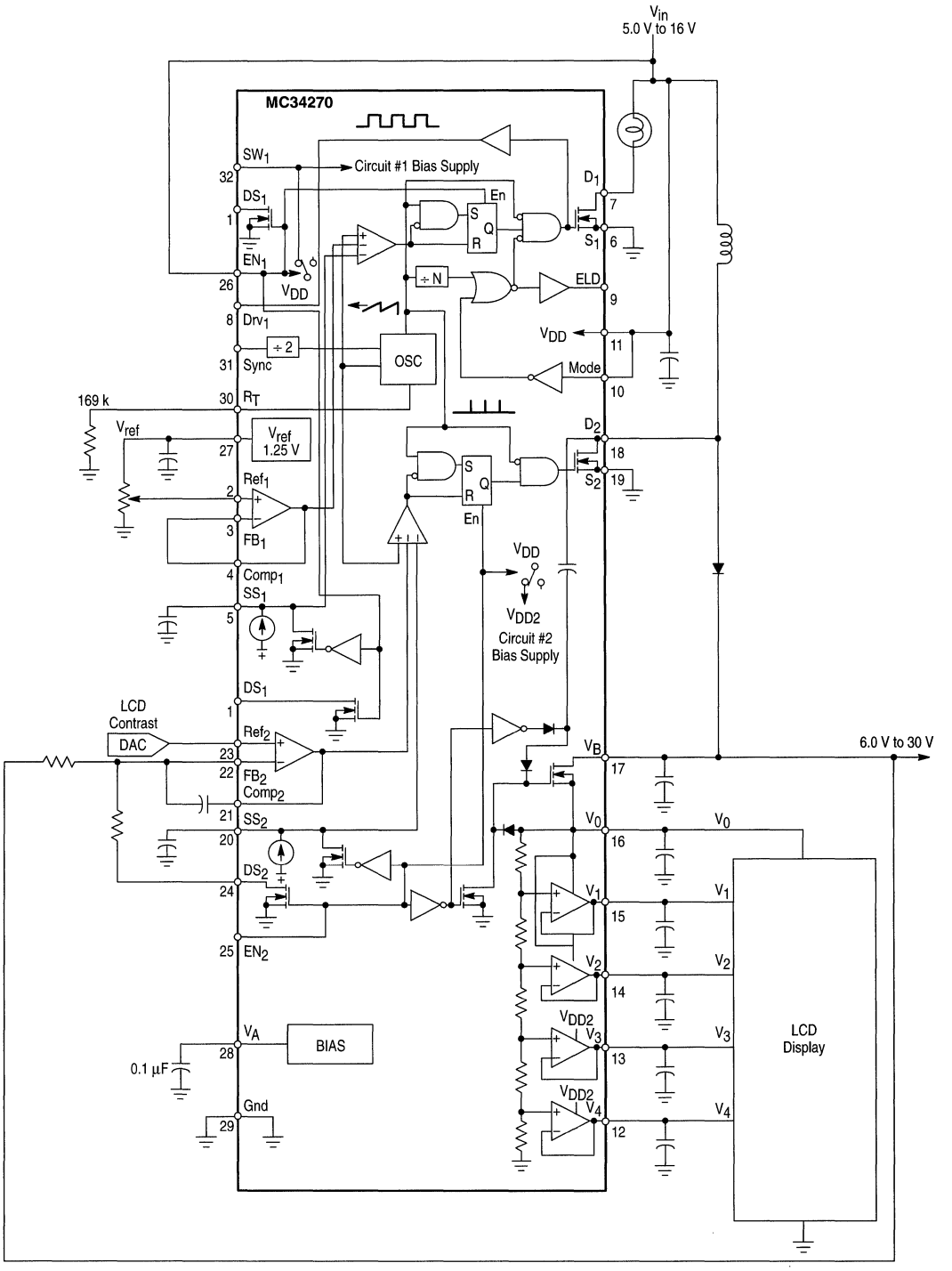
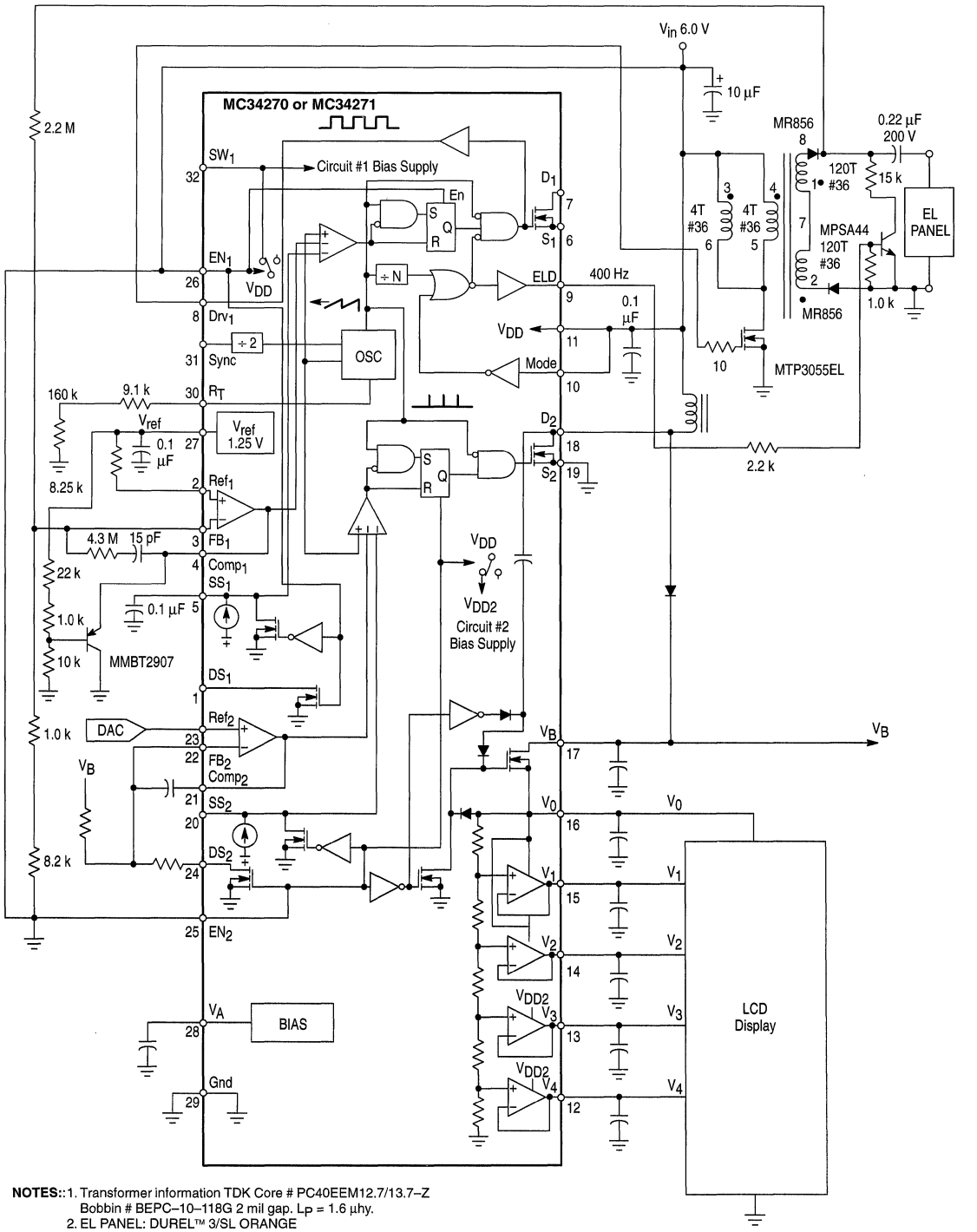


Figure 13. MC34270 Incandescent Backlight Configuration



3

Figure 14. EL PANEL Drive Circuit



NOTES:: 1. Transformer information TDK Core # PC40EEM12.7/13.7–Z
Bobbin # BEPC–10–118G 2 mil gap. L_P = 1.6 µhy.
2. EL PANEL: DUREL™ 3/SL ORANGE

MOTOROLA

MC44602

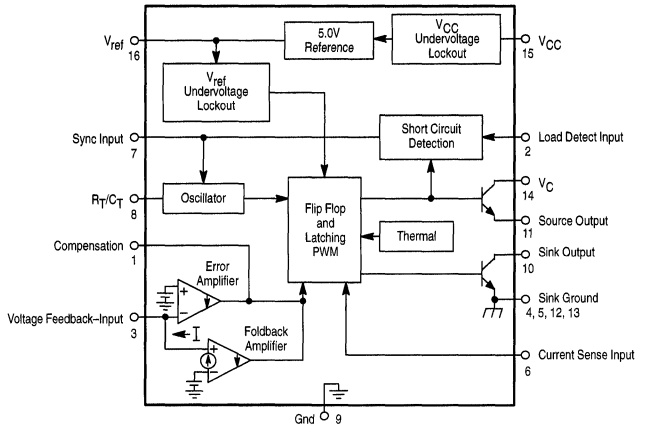
High Performance Current Mode Controller

The MC44602 is an enhanced high performance fixed frequency current mode controller that is specifically designed for off–line and high voltage dc–to–dc converter applications. This device has the unique ability of changing operating modes if the converter output is overloaded or shorted, offering the designer additional protection for increased system reliability. The MC44602 has several distinguishing features when compared to conventional current mode controllers. These features consist of a foldback amplifier for overload detection, valid load and demag comparators with a fault latch for short circuit detection, thermal shutdown, and separate high current source and sink outputs that are ideally suited for driving a high voltage bipolar power transistor, such as the MJE18002, MJE18004, or MJE18006.

Standard features include an oscillator with a sync input, a temperature compensated reference, high gain error amplifier, and a current sensing comparator. Protective features consist of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, a latch for single pulse metering, and a flip–flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed from 50% to 70%. This device is manufactured in a 16 pin dual–in–line heat tab package for improved thermal conduction.

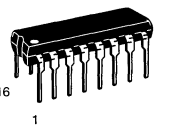
- Separate High Current Source and Sink Outputs Ideally Suited for Driving Bipolar Power Transistors: 1.0 A Source, 1.5 A Sink
- Unique Overload and Short Circuit Protection
- Thermal Protection
- Oscillator with Sync Input
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Input and Reference Undervoltage Lockouts with Hysteresis
- Low Startup and Operating Current

Simplified Block Diagram



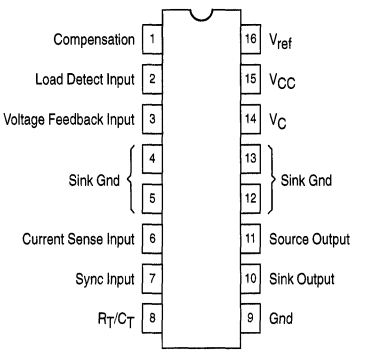
HIGH PERFORMANCE CURRENT MODE CONTROLLER

SEMICONDUCTOR TECHNICAL DATA



P2 SUFFIX
PLASTIC PACKAGE
CASE 648C
DIP (12 + 2 + 2)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44602	T_A = –25 to 85°C	DIP (12 + 2 + 2)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Sink Ground Voltage with Respect to Gnd (Pin 9)	$V_{Sink(neg)}$	–5.0	V
Output Supply Voltage with Respect to Sink Gnd (Pins 4, 5, 12, 13)	V_C	20	V
Output Current (Note 1)			A
Source	$I_{O(Source)}$	1.0	
Sink	$I_{O(Sink)}$	1.5	
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	–0.3 to 5.5	V
Sync Input			
High State Voltage	V_{IH}	5.5	V
Low State Reverse Current	I_{IL}	–20	mA
Load Detect Input Current	I_{in}	–20 to +10	mA
Error Amplifier Output Sink Current	$I_{EA\ (Sink)}$	10	mA
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation at T_A = 25°C	P_D	2.5	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	80	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	15	°C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–25 to +85	°C

NOTE: 1. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 2], R_T = 10k, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Voltage Feedback Input (V_O = 2.5V)	V_{FB}	2.45	2.5	2.65	V
Input Bias Current (V_{FB} = 2.5 V)	I_{IB}	–	–0.6	–2.0	μA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	dB
Unity Gain Bandwidth	BW				MHz
T_J = 25°C		1.0	1.4	1.8	
T_A = –25 to +85°C		0.8	–	2.0	
Power Supply Rejection Ratio (V_{CC} = 10 V to 16 V)	PSRR	65	70	–	dB
Output Current					mA
Sink (V_O = 1.5 V, V_{FB} = 2.7 V)	I_{Sink}				
T_J = 25°C		–	5.0	–	
T_A = –25 to +85°C		1.5	–	10	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}				
T_J = 25°C		–	–1.1	–	
T_A = –25 to +85°C		–2.0	–	–0.2	
Output Voltage Swing					V
High State ($I_{O(Source)}$ = 0.5 mA, V_{FB} = 2.3 V)	V_{OH}	6.0	7.0	–	
Low State ($I_{O(Sink)}$ = 0.33 mA, V_{FB} = 2.7 V)	V_{OL}	–	1.0	1.1	

NOTES: 2. Adjust V_{CC} above the startup threshold before setting to 12V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 2], R_T = 10k, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Frequency T_J = 25°C T_A = –25°C to +85°C	f_{OSC}	 168 160	 180 –	 192 200	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 18 V)	$\Delta f_{OSC}/\Delta V$	–	0.1	0.2	%/V
Frequency Change with Temperature	$\Delta f_{OSC}/\Delta T$	–	0.05	–	%/°C
Oscillator Voltage Swing (Peak–to–Peak)	$V_{OSC(pp)}$	1.3	1.6	–	V
Discharge Current (V_{OSC} = 3.0 V) T_J = 25°C T_A = –25°C to +85°C	I_{dischg}	 6.5 6.0	 10 –	 13.5 14	mA
Sync Input Threshold Voltage High State Low State	 V_{IH} V_{IL}	 2.5 1.0	 2.8 1.3	 3.2 1.7	V
Sync Input Resistance T_J = 25°C T_A = –25°C to +85°C	R_{in}	 6.5 6.0	 10 –	 13.5 18	kΩ
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA)	V_{ref}	4.7	5.0	5.3	V
Line Regulation (V_{CC} = 12 V to 18 V)	Reg_{line}	–	1.0	10	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	15	mV
Temperature Stability	T_S	–	0.2	–	mV/°C
Total Output Variation over Line, Load and Temperature	V_{ref}	4.65	–	5.35	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	mV
Output Short Circuit Current T_J = 25°C T_A = –25°C to +85°C	I_{SC}	 – –70	 –130 –	 – –180	mA
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 & 5) T_J = 25°C T_A = –25°C to +85°C	A_V	 2.85 2.7	 3.0 –	 3.15 3.2	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	V
Input Bias Current	I_{IB}	–	–4.0	–10	μA
Propagation Delay (Current Sense Input to Sink Output)	$t_{PLH(in/out)}$	–	100	150	ns
UNDERVOLTAGE LOCKOUT SECTIONS					
Startup Threshold (V_{CC} Increasing)	V_{th}	13	14.1	15	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{CC(min)}$	9.0	10.2	11	V
Reference Undervoltage Threshold (V_{ref} Decreasing)	$V_{ref(UVLO)}$	3.0	3.35	3.7	V

NOTES: 2. Adjust V_{CC} above the startup threshold before setting to 12V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
4. This parameter is measured at the latch trip point with I_{FB} = –5.0 μA, refer to Figure 9.
5. Comparator gain is defined as $A_V = \frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense Input}}$

3

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 2], R_T = 10k, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT SECTION					
Output Voltage (T_A = 25°C)					V
Low State (I_{Sink} = 100 mA)	V_{OL}	–	0.6	0.3	
(I_{Sink} = 1.0A)		–	1.8	2.0	
(I_{Sink} = 1.5 A)		–	2.1	2.6	
High State (I_{Source} = 50 mA)	(V_{CC}–V_{OH})	–	1.4	1.7	
(I_{Source} = 0.5 A)		–	1.7	2.0	
(I_{Source} = 0.75 A)		–	1.8	2.2	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	ns
PWM SECTION					
Duty Cycle					%
Maximum	$DC_{(max)}$	46	48	50	
Minimum	$DC_{(min)}$	–	–	0	
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Startup (V_{CC} = 5 V)		–	0.2	0.5	
Operating (Note 2)					
T_J = 25° C		–	17	20	
T_A = –25°C to +85° C		10	–	22	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	18	20	23	V
OVERLOAD AND SHORT CIRCUIT PROTECTION					
Foldback Amplifier Threshold (Figures 9,10)	ΔV_{FB}	(V_{FB}–100)	(V_{FB}–200)	(V_{FB}–300)	mV
Load Detect Input					
Valid Load Comparator Threshold ($V_{Pin\ 2}$ Increasing)	$V_{th(VL)}$	2.0	2.5	3.0	V
Demag Comparator Threshold ($V_{Pin\ 2}$ Decreasing)	$V_{th(Demag)}$	50	88	120	mV
Propagation Delay (Input to Sink or Source Output)	$t_{PLH(in/out)}$	–	1.1	1.6	µS
Input Resistance	R_{in}	12	18	30	kΩ

NOTES: 2. Adjust V_{CC} above the startup threshold before setting to 12V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Timing Resistor versus Oscillator Frequency

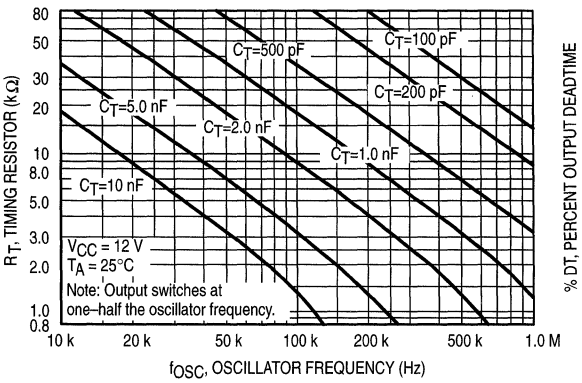


Figure 2. Output Deadtime versus Oscillator Frequency

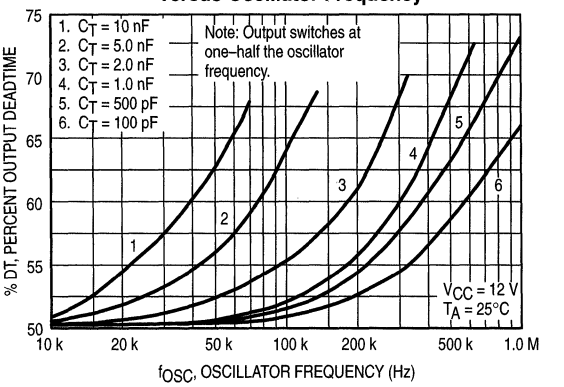


Figure 3. Oscillator Discharge Current versus Temperature

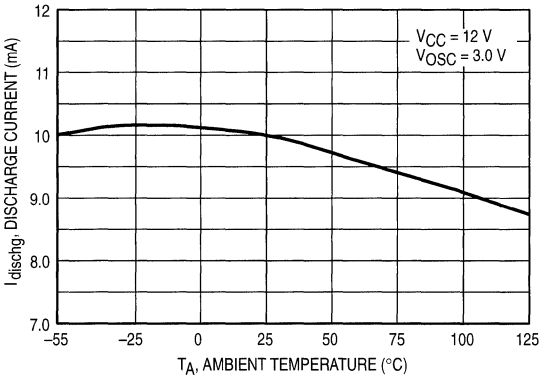


Figure 4. Oscillator Voltage Swing versus Temperature

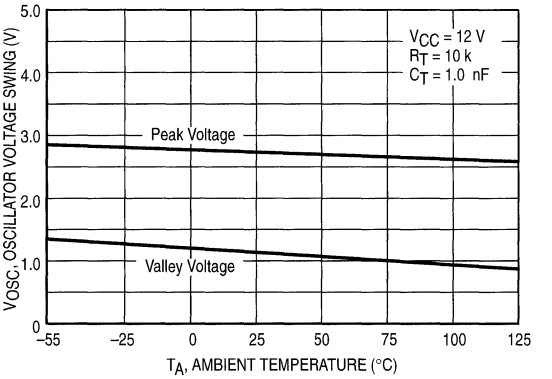


Figure 5. Error Amp Small Signal Transient Response

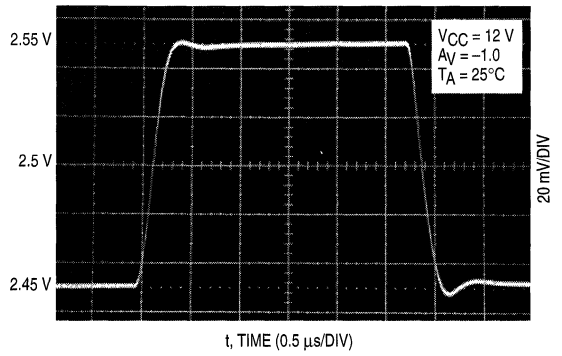


Figure 6. Error Amp Large Signal Transient Response

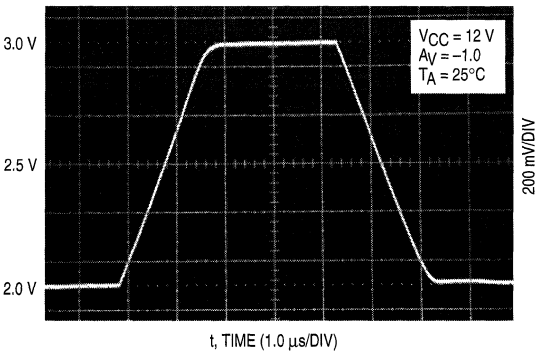


Figure 7. Error Amp Open Loop Gain and Phase versus Frequency

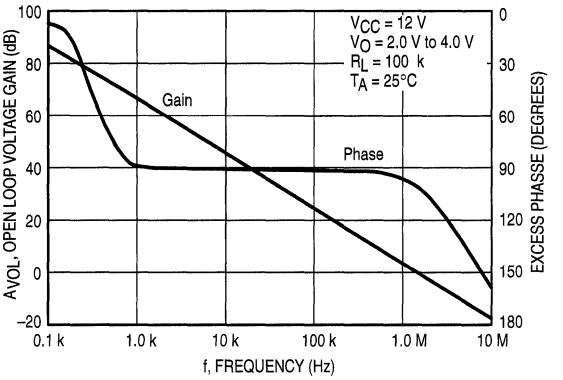
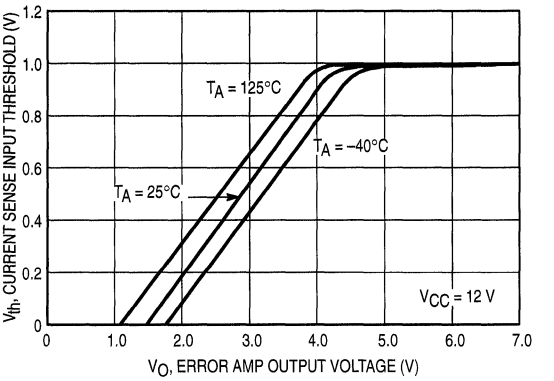


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage



3

Figure 9. Voltage Feedback Input, Voltage versus Current

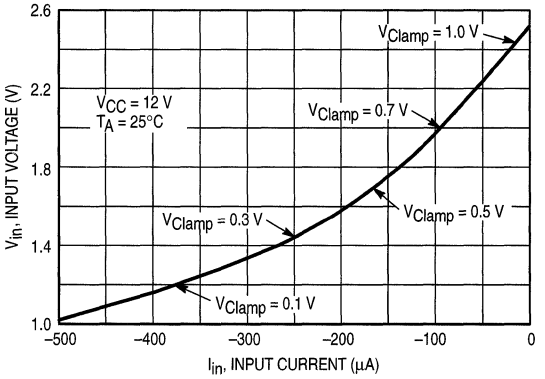


Figure 10. Voltage Feedback Input versus Current Sense Clamp Level

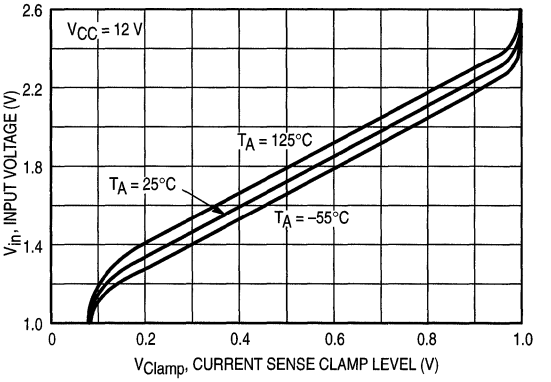


Figure 11. Reference Short Circuit Current versus Temperature

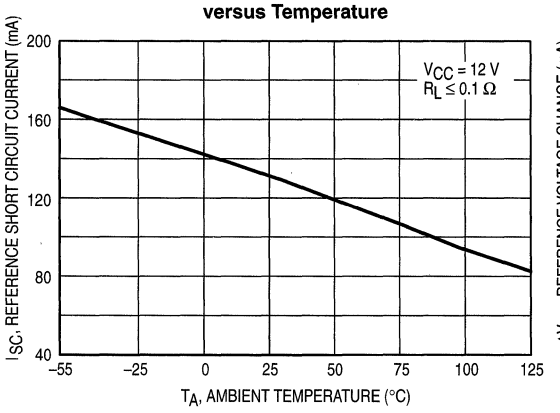


Figure 12. Reference Line and Load Regulation versus Temperature

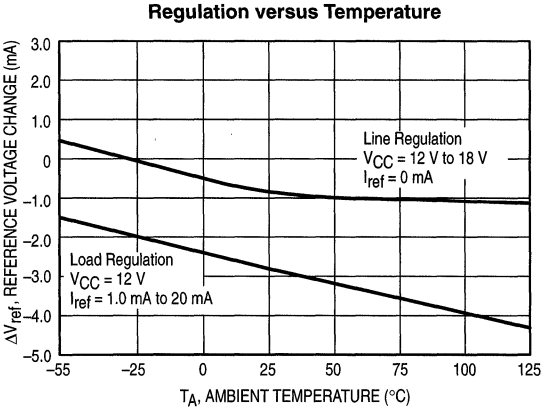


Figure 13. Reference Voltage Change versus Source Current

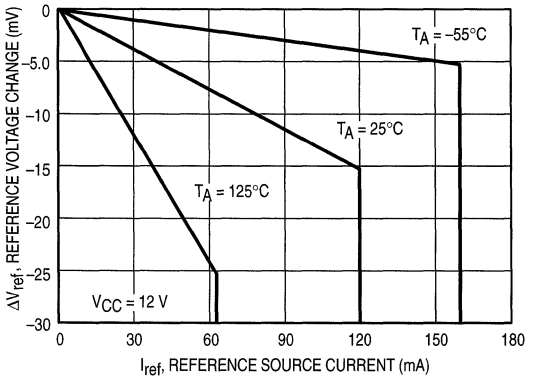


Figure 14. Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

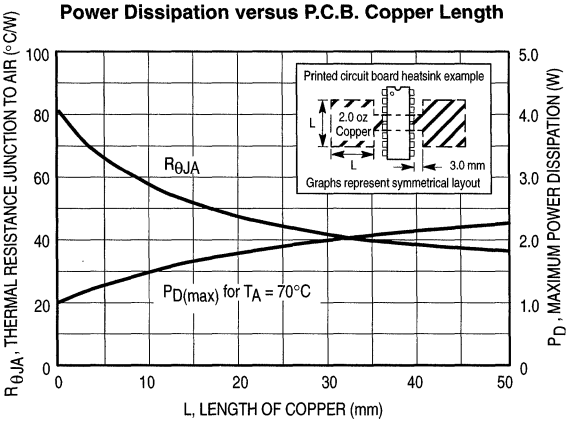


Figure 15. Output Waveform

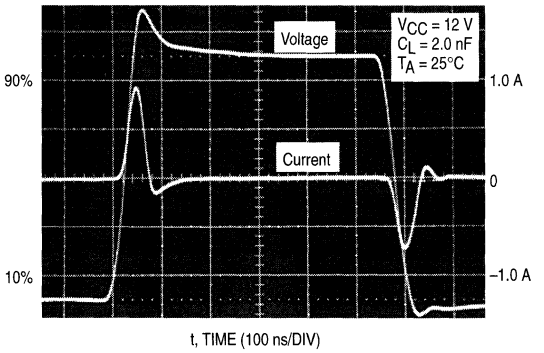
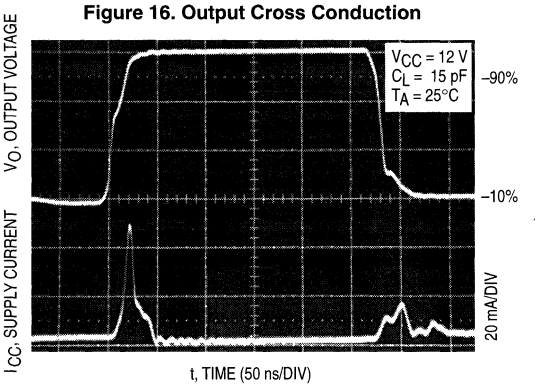


Figure 16. Output Cross Conduction



3

Figure 17. Sink Output Saturation Voltage versus Sink Current

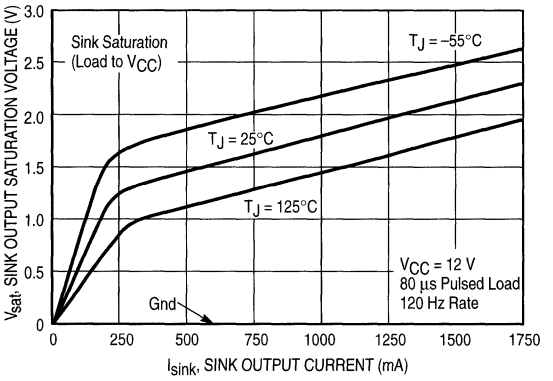


Figure 18. Source Output Saturation Voltage versus Load Current

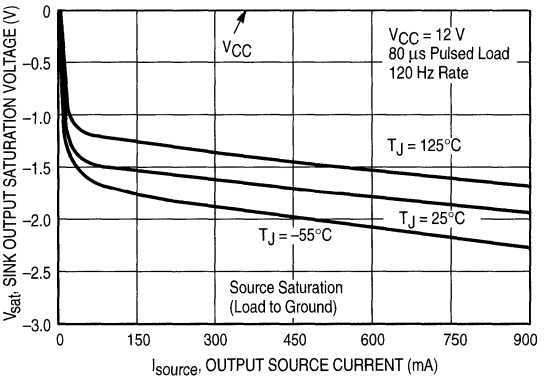


Figure 19. Supply Current versus Supply Voltage

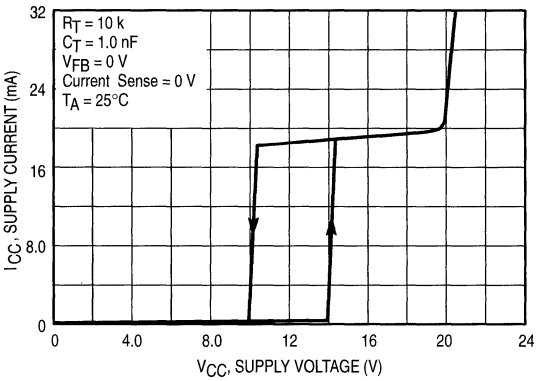


Figure 20. Power Supply Zener Voltage versus Temperature

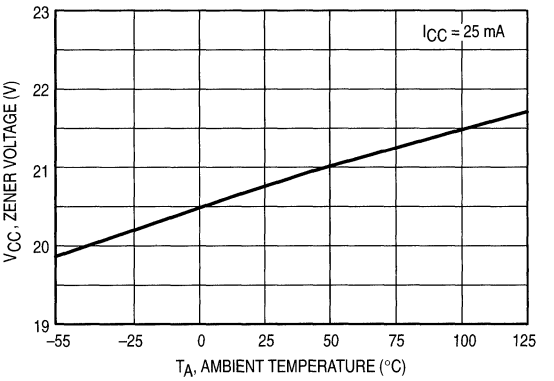


Figure 21. Valid Load Comparator Threshold versus Temperature

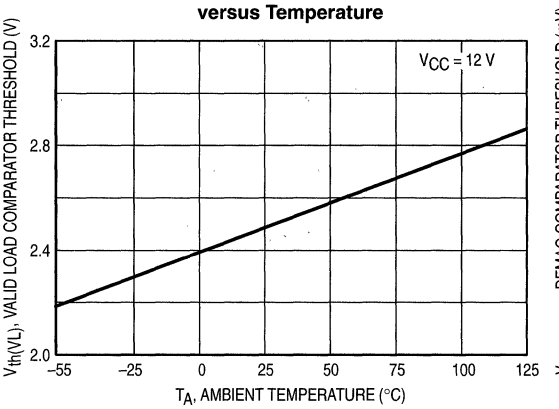


Figure 22. Demag Comparator Threshold versus Temperature

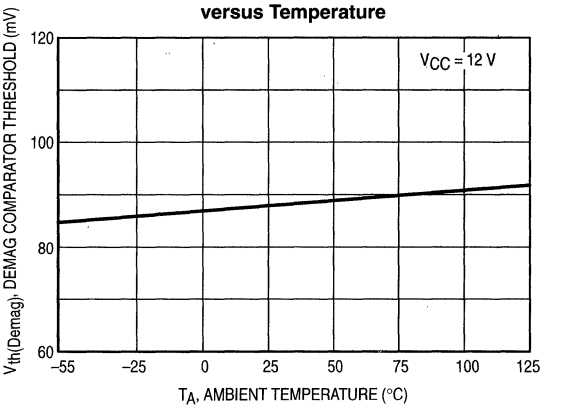


Figure 23. Load Detect Input Propagation Delay versus Temperature

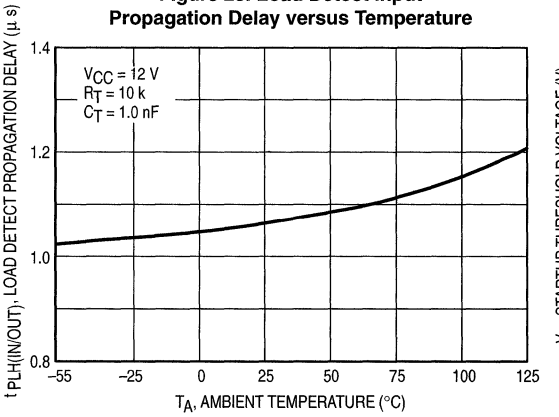


Figure 24. Startup Threshold Voltage versus Temperature

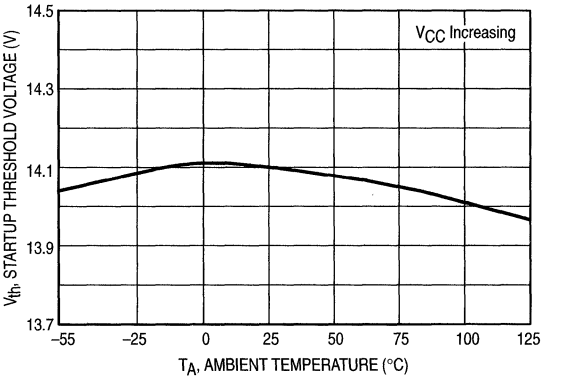


Figure 25. Minimum Operating Voltage After Turn–On versus Temperature

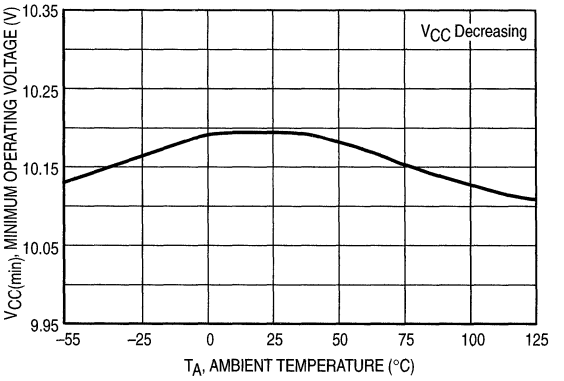


Figure 26. Reference Undervoltage Threshold versus Temperature

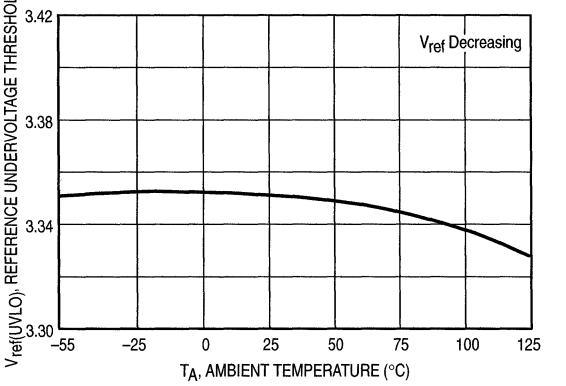


Figure 27. Representative Block Diagram

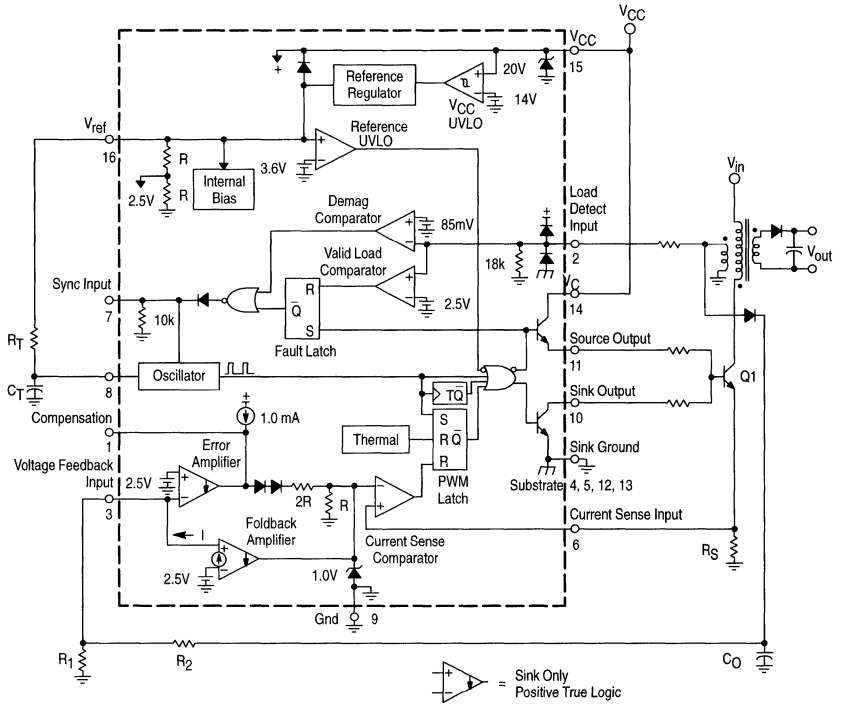
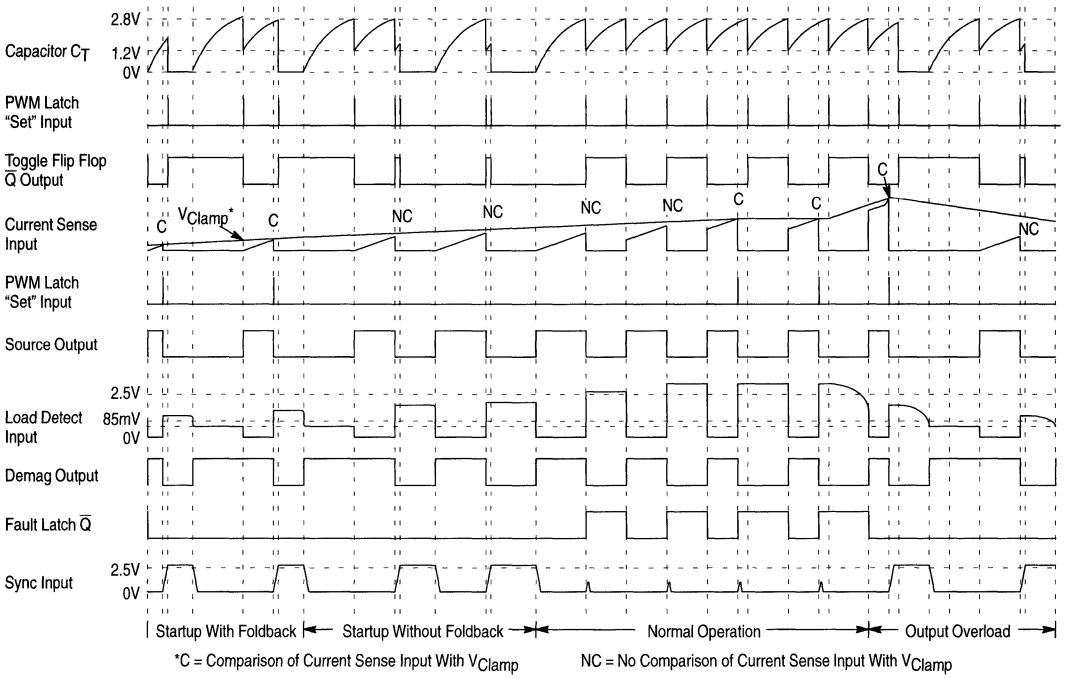


Figure 28. Timing Diagram



OPERATING DESCRIPTION

The MC44602 is a high performance, fixed frequency, current mode controller specifically designed to directly drive a bipolar power switch in off–line and high voltage dc–to–dc converter applications. This device offers the designer a cost effective solution with minimal external components. The representative block and timing diagrams are shown in Figures 27 and 28.

3

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds one of the inputs of the NOR gate high. This causes the Source and Sink outputs to be in a low state, thus producing a controlled amount of output deadtime. An internal toggle flip–flop has been incorporated in the MC44602 which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for a given value of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency.

In many noise sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a narrow rectangular clock signal with an amplitude of 3.2 V to 5.5 V to the Sync Input (Pin 7). For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. If the clock signal is ac coupled through a capacitor, an external clamp diode may be required if the negative sync input current is greater than –5.0 mA. Connecting Pin 7 to V_{ref} will cause C_T to discharge to 0 V, inhibiting the Oscillator and conduction of the Source Output. Multi–unit synchronization can be accomplished by connecting the C_T pin of each IC to a single MC1455 timer.

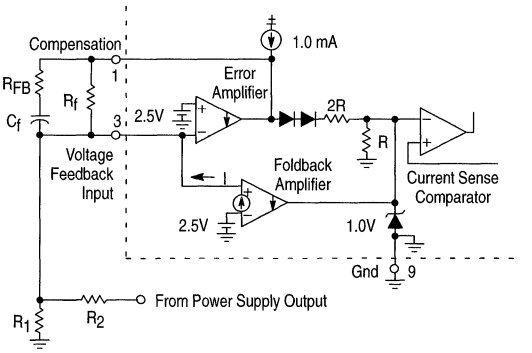
Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwith of 1.0 MHz with 57 degrees of phase margin (Figure 7). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current with the inverting input at 2.5 V is –2.0 μA. This can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 29). The output voltage is offset by two diodes drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Source Output (Pin 11) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval. The Error Amp minimum feedback resistance is limited by the amplifier's minimum source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5mA} = 8800\ \Omega$$

Figure 29. Error Amplifier Compensation



Current Sense Comparator and PWM Latch

The MC44602 operates as a current mode controller, where output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output (Pin 1). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Source Output during the appropriate oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the emitter of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 1 where:

$$I_{pk} \approx \frac{V\ (Pin1) - 1.4V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} \approx \frac{1.0\ V}{R_S}$$

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and the output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 30.

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14.1 V/10.2 V. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.3 V. The large hysteresis and low startup current of the MC44602 make it ideally suited for off–line converter applications (Figures 33, 34) where efficient bootstrap startup techniques are required.

A 20 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The upper limit for the minimum operating voltage of the MC44602 is 11V.

Outputs

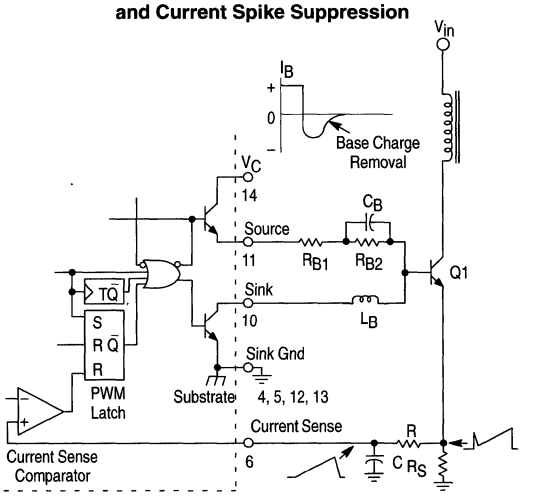
The MC44602 contains a high current split totem pole output that was specifically designed for direct drive of Bipolar Power Transistors. By splitting the totem pole into separate source and sink outputs, the power supply designer has the ability to independently adjust the turn–on and turn–off base drive to the external power transistor for optimal switching. The Source and Sink outputs are capable of up to 1.0 A and 1.5 A respectively and feature 50 ns switching times with a 1.0 nF load. Additional internal circuitry has been added to keep the Source Output "Off" and the Sink Output "On" whenever an undervoltage lockout is active. This feature eliminates the need for an external pull–down resistor and guarantees that the power transistor will be held in the "Off" state.

Separate output stage power and ground pins are provided to give the designer added flexibility in tailoring the base drive circuitry for a specific application. The Source Output high–state is controlled by applying a positive voltage to V_C (Pin 14) and is independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20V. The Sink Output low–state is controlled by applying a negative voltage to the Sink Ground (Pins 4, 5, 12, 13). The Sink Ground can be biased as much as 5.0 V negative with respect to Ground (Pin 7). Proper implementation of the V_C and Sink Ground pins will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level.

Reference

The 5.0 V bandgap reference has a tolerance of ±6.0% over a junction temperature range of –25°C to 85°C. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Figure 30. Bipolar Transistor Drive and Current Spike Suppression



Thermal Protection and Package

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the PWM Latch is held in the "reset" state, forcing the Source Output "Off" and the Sink Output "On". This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC44602 is contained in a heatsinkable 16–lead plastic dual–in–line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center Sink Ground pins that are specifically designed to improve the thermal conduction from the die to the circuit board. Figure 14 shows a simple and effective method of utilizing the printed circuit medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. This example is for a symmetrical layout on a single–sided board with two ounce per square foot of copper.

Design Considerations

Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low–current signal, and high current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

PROTECTION MODES

The MC44602 operates as a conventional fixed frequency current mode controller when the power supply output load is less than the design limit. For enhanced system reliability, this device has the unique ability of changing operating modes if the power supply output is overloaded or shorted.

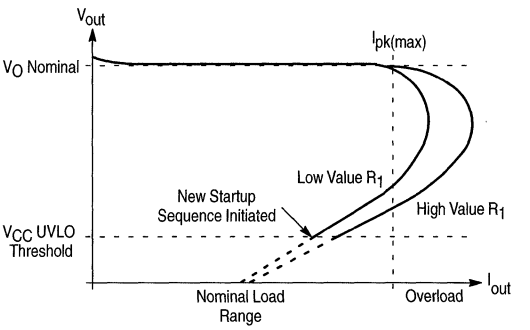
Overload Protection

Power supply overload protection is provided by the Foldback Amplifier. As the output load gradually increases, the Error Amplifier senses that the voltage at Pin 3 is less than the 2.5 V threshold. This causes the voltage at Pin 1 to rise, increasing the Current Sense Comparator threshold in order to maintain output regulation. As the load further increases, the inverting input of the Current Sense Comparator reaches the internal 1.0 V clamp level, limiting the switch current to the calculated $I_{pk(max)}$. At this point any further increase in load will cause the power supply output to fall out of regulation. As the voltage at Pin 3 falls below 2.5 V, current will flow out of the Foldback Amplifier input, and the internal clamp level will be proportionally reduced (Figures 9, 10). The increase in current flowing out of the Foldback Amplifier input in conjunction with the reduced clamp level, causes the power supply output voltage to fall at a faster rate than the voltage at Pin 3. This results in the output foldback characteristic shown in Figure 31. The shape of the current limit "knee" can be modified by the value of resistor R_1 in the feedback divider. Lower values of R_1 will reduce the $I_{pk(max)}$ clamp level at a faster rate.

Improper operation of the Foldback Amp can be encountered when the Error Amp compensation capacitor C_f exceeds 2.0 nF. The problem appears at Startup when the output voltage of the power supply is below nominal, causing the Error Amp output to rise quickly. The rapid change in output voltage will be coupled through C_f to the Inverting Input (Pin 3), keeping it at its 2.5 V threshold as the 1.0 mA Error Amp current source charges C_f. This has the effect of disabling the Foldback Amp by preventing Pin 3 and the clamp level at the inverting input of the Current Sense Comparator, from rising in proportion to the power supply output voltage. By adding resistor R_{FB} in series with C_f, the voltage at Pin 3 can be held to 1.0 V, corresponding to a Current Sense clamp level of 0.08 V (Figure 10), while allowing the Error Amp output to reach its high state V_{OH} of 7.0 V. The required resistor to keep Pin 3 below 1.0 V during initial Startup is:

$$\frac{R_{FB}\,R_f}{R_{FB}+R_f} \geq 6\left(\frac{R_1\,R_2}{R_1+R_2}\right)$$

Figure 31. Output Foldback Characteristic



Short Circuit Protection

Short circuit protection for the power supply is provided by the Valid Load Comparator, Fault Latch, and Demag Comparator. Figure 32 shows the logic truth table of the functional blocks. When operating the power supply with nominal output loading, the Fault Latch is "Set" by the NOR gate driver during the Power Transistor "On" time and "Reset" by the Fault Comparator during the "Off" time. When a severe overload or short circuit occurs on any output, the voltage during the "Off" time (flyback voltage) at the Load Detect Input, is unable to reach the 2.5 V threshold of the Valid Load Comparator. This causes the Fault Latch to remain in the "Set" state with output $\overline{Q}$ "Low". During the "Off" time the Demag Comparator output will also be "Low". This causes the NOR gate to internally hold the Sync Input "High", inhibiting the next fixed frequency Oscillator cycle and switching of the Power Transistor. As the load dissipates the stored transformer energy, the voltage at the Load Detect Input will fall. When this voltage reaches 85 mV, the Demag Comparator output goes "High", allowing the Sync Input to go "Low", and the Power Transistor to turn "On".

Note that as long as there is an output short, the switching frequency will shift to a much lower frequency than that set by R_T/C_T. The frequency shift has the effect of lowering the duty cycle, resulting in a significant reduction in Power Transistor and Output Rectifier heating when compared to conventional current mode controllers. The extended "On" time is the result of C_T charging from 0 V to 2.8 V instead of 1.2 V to 2.8 V. The extended "Off" time is the result of the output short time constant. The time constant consists of the output filter capacitance, and the equivalent series resistance (ESR) of the capacitor plus the associated wire resistance.

Figure 32. Logic Truth Table of Functional Blocks

Output Load	Power Transistor	Demag		Fault Latch			Sync	Operating Comments
		Input	Out	S	R	$\overline{Q}$	Input	
Nominal	On	<85mV	1	1	0	0	0	NOR gate driver sets Fault Latch.
	At Turn–Off	>85 mV, <2.5 V	0	0	0	0	⎍	Narrow spike at Sync Input (<2.5 V) as transformer voltage rises quickly, Oscillator is not affected.
	Off	>2.5 V	0	0	1	1	0	Valid Load Comparator resets Fault Latch.
Short	On	<85 mV	1	1	0	0	0	Short is not detected until transistor turn–off.
	At Turn–Off	>85 mV, <2.5 V	0	0	0	0	1	Valid Load Comparator fails to reset Fault Latch, Pulse at Sync Input exceeds 2.5 V, Oscillator is disabled.
	Off	<85 mV	1	0	0	0	0	Load dissipates transformer energy, Oscillator enabled.

3

During the initial power supply startup the controller sequences through the Short Circuit and Overload Protection modes as the output filter capacitors charge–up. If an output is shorted and the auxiliary feedback winding is used to power the control IC as in Figure 33, the V_{CC} UVLO lower threshold level will be reached after several cycles, disabling the IC and initiating a new startup sequence. The Short Circuit Protection mode can be disabled by grounding the Sync Input. Narrow switching spikes are present on this pin during normal operation. These spikes are caused by the rise time of the flyback voltage from the 85 mV Demag Comparator threshold to the 2.5 V Valid Load Comparator threshold. In high power applications, the increased negative current at the Load Detect Input can extend the switching spikes to the point where they exceed the Sync Input threshold. This problem can be eliminated by placing an external small signal clamp diode at the Load Detect Input. The diode is connected with the cathode at Pin 2 and the anode at ground.

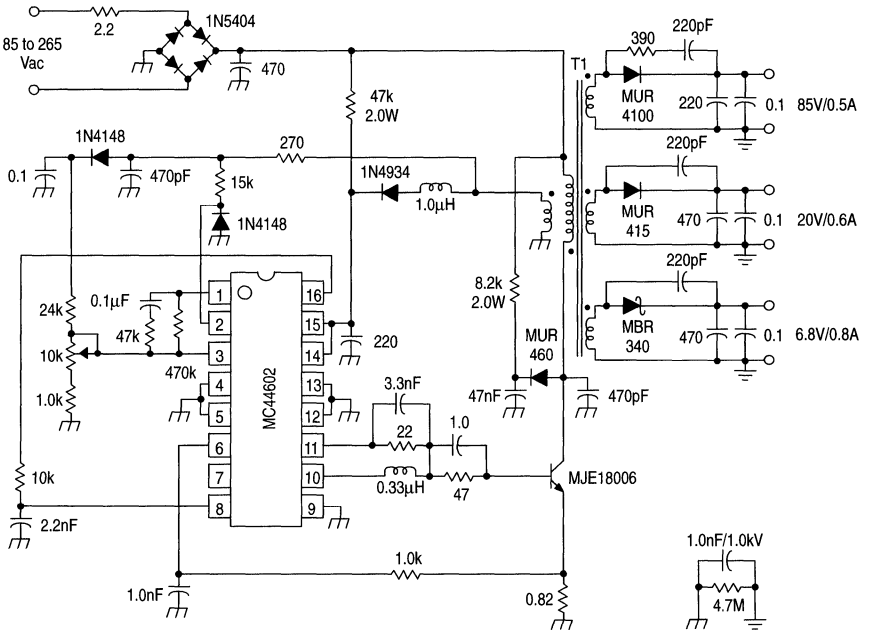
The divide–by–two toggle flip–flop will appear not to function properly during power supply startup without foldback, or operation with an overloaded output. This phenomena appears at the end of the oscillator cycle if there was not a current sense comparison, and after the flyback voltage at the Load Detect Input failed to exceed 2.5 V. Under these conditions, the Sync input will go high approximately 1.0 μs after the Load Detect Input exceeds the 85 mV Demag Comparator threshold. This causes C_T to discharge down towards ground, generating a second negative going edge on the oscillator waveform. This second edge results in the divide–by–two flip–flop being clocked twice for each "On" time of the switch transistor. During initial startup, this effect can be eliminated by insuring that the Foldback Amplifier is fully active with the addition of resistor R_{FB}. With the Foldback Amplifier active, the clamp level at the inverting input of the Current Sense Comparator will be low, allowing a comparison to take place during the switch transistor "On" time. When the Load Detect Input exceeds 85 mV, the Sync Input will go high, discharging C_T to ground after 1.0 μs, thus eliminating the second negative edge. Operation with the output overloaded will cause the toggle flip–flop to be clocked twice for each "On" time. This should not be a problem since the next "On" time is delayed by the Demag Comparator until the load dissipates the transformers energy.

The point where the IC detects that there is a severe output overload, or that the transformer has reached zero current, is controlled by the voltage of the auxiliary winding and a resistor divider. The divider consists of an external series resistor and an internal shunt resistor. The shunt resistor is nominally 18 kΩ but can range from 12 kΩ to 30 kΩ due to process variations. If more precise overload and zero current detection is required, the internal resistor variations can be swamped out by connecting a low value external resistor (≤2.7 kΩ) from Pin 2 to ground.

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	Load Detect Input	A voltage indicating a severe overload or short circuit condition at any output of the switching power supply is connected to this input. The Oscillator is controlled by this information making the power supply short circuit proof.
3	Voltage Feedback Input	This is the inverting input of the Error Amplifier and the noninverting input of the Foldback Amplifier. It is normally connected to the switching power supply output through a resistor divider.
4, 5, 12, 13	Sink Ground	The Sink Ground pins form a single power return that is typically connected back to the power source on a separate path from Pin 9 Ground, to reduce the effects of switching transient noise on the control circuitry. These pins can be used to enhance the package power capabilities (Figure 14). The Sink Output low state (V_{OL}) can be modified by applying a negative voltage to these pins with respect to Ground (Pin 9) to optimize turn–off of a bipolar junction transistor.
6	Current Sense Input	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate conduction of the output switch transistor.
7	Sync Input	A narrow rectangular waveform applied to this input will synchronize the Oscillator. A dc voltage within the range of 3.2 V to 5.5 V will inhibit the Oscillator.
8	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed at this pin by connecting resistor R_T to V_{ref} and capacitor C_T to ground.
9	Ground	This pin is the control circuitry ground and is typically connected back to the power source on a separate path from the Sink Ground (Pins 4, 5, 12, 13).
10	Sink Output	Peak currents up to 1.5 A are sunk by this output suiting it ideally for turning–off a bipolar junction transistor. The output switches at one–half the oscillator frequency.
11	Source Output	Peak currents up to 1.0 A are sourced by this output suiting it ideally for turning–on a bipolar junction transistor. The output switches at one–half the oscillator frequency.
14	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate connection to the power source, it can reduce the effects of switching transient noise on the control circuitry.
15	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after startup is 11 V to 18 V.
16	V_{ref}	This is the 5.0 V reference output. It provides charging current for capacitor C_T through resistor R_T and can be used to bias any additional system circuitry.

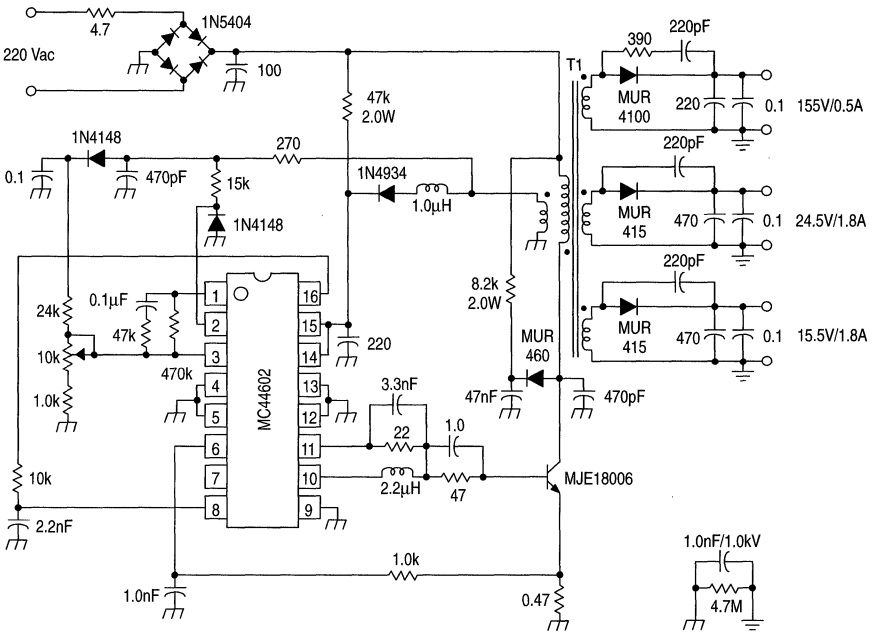
Figure 33. 60 Watt Off–Line Flyback Regulator



Test	Conditions	Results
Line Regulation	V_{in} = 85 Vac to 265 Vac	
85V	I_O = 0.5 A	Δ = 1.0 V or ± 0.6%
20V	I_O = 0.5 A	Δ = 0.04 V or ± 0.1%
6.8V	I_O = 0.8 A	Δ = 0.07 V or ± 0.5%
Load Regulation	V_{in} = 220 Vac	
85V	I_O = 0.1 A to 0.5 A	Δ = 1.0 V or ± 0.6%
20V	I_O = 0.1 A to 0.5 A	Δ = 0.4 V or ± 1.0%
6.8V	I_O = 0.1 A to 0.8 A	Δ = 0.2 V or ± 1.5%
Efficiency	V_{in} = 110 Vac, P_O = 58 W	81%
Standby Power	V_{in} = 110 Vac, P_O = 0 W	2.0 W

T1 – Orega SMT2 (G4787–01)
Primary: 41 Turns, #25AWG
Auxiliary Feedback: 12 Turns, #25AWG
Secondary: 85 V – 60 Turns, #25AWG
20 V – 15 Turns, #25AWG (2 Strands) Bifiliar Wound
6.8 V – 5 Turns, #25AWG (2 Strands) Bifiliar Wound
Core – ETD39 34x17x11 B52
Gap – ≈ 0.020″ for a primary inductance of 750 µH, A_L = 500 nH/Turn^2

Figure 34. 150 Watt Off–Line Flyback Regulator



Test	Conditions	Results
Line Regulation	V_{in} = 185 Vac to 265 Vac	
155V	I_O = 0.5 A	Δ = 1.0 V or ± 0.3%
24.5V	I_O = 1.0. A	Δ = 0.4 V or ± 0.8%
15.5V	I_O = 1.0 A	Δ = 0.3 V or ± 1.0%
Load Regulation	V_{in} = 220 Vac	
155V	I_O = 0.1 A to 0.5 A	Δ = 2.0 V or ± 0.7%
24.5V	I_O = 0.1 A to 1.0 A	Δ = 0.4 V or ± 0.8%
15.5V	I_O = 0.1 A to 1.0 A	Δ = 0.2 V or ± 0.7%
Efficiency	V_{in} = 220 Vac, P_O = 117.5 W	83%
Standby Power	V_{in} = 220 Vac, P_O = 0 W	5.0 W

T1 – Orega SMT2 (G4717–01)
Primary: 55 Turns, #25AWG
Auxiliary Feedback: 6 Turns, #25AWG
Secondary: 155 V – 52 Turns, #25AWG
24.5 V – 9 Turns, #25AWG (2 Strands) Bifiliar Wound
15.5 V – 6 Turns, #25AWG (2 Strands) Bifiliar Wound
Core – GETV 53x18x18 B52
Gap – ≈ 0.020″ for a primary inductance of 1.35 µH, A_L = 450 nH/Turn^2

MC44603

Advance Information

Mixed Frequency Mode GreenLine™ PWM Controller:

Fixed Frequency, Variable Frequency, Standby Mode

MIXED FREQUENCY MODE GREENLINE PWM* CONTROLLER:

VARIABLE FREQUENCY, FIXED FREQUENCY, STANDBY MODE

* PWM = Pulse Width Modulation

The MC44603 is an enhanced high performance controller that is specifically designed for off–line and dc–to–dc converter applications. This device has the unique ability of automatically changing operating modes if the converter output is overloaded, unloaded, or shorted, offering the designer additional protection for increased system reliability. The MC44603 has several distinguishing features when compared to conventional SMPS controllers. These features consist of a foldback facility for overload protection, a standby mode when the converter output is slightly loaded, a demagnetization detection for reduced switching stresses on transistor and diodes, and a high current totem pole output ideally suited for driving a power MOSFET. It can also be used for driving a bipolar transistor in low power converters (< 150 W). It is optimized to operate in discontinuous mode but can also operate in continuous mode. Its advanced design allows use in current mode or voltage mode control applications.

Current or Voltage Mode Controller

- Operation up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Oscillator with Precise Frequency Control

High Flexibility

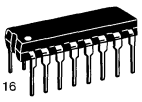
- Externally Programmable Reference Current
- Secondary or Primary Sensing
- Synchronization Facility
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis

Safety/Protection Features

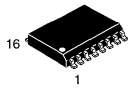
- Overvoltage Protection Against Open Current and Open Voltage Loop
- Protection Against Short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft–Start Feature
- Accurate Maximum Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference

GreenLine Controller: Low Power Consumption in Standby Mode

- Low Startup and Operating Current
- Fully Programmable Standby Mode
- Controlled Frequency Reduction in Standby Mode
- Low dV/dT for Low EMI Radiations

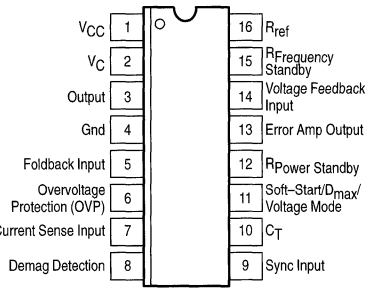


P SUFFIX
PLASTIC PACKAGE
CASE 648



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP–16L)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44603P	T_A = –25° to +85°C	Plastic DIP–16
MC44603DW		SOP–16L

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Supply Voltage with Respect to Ground (Pin 4)	V_C V_{CC}	18	V
Output Current (Note 1) Source Sink	 $I_{O(Source)}$ $I_{O(Sink)}$	 –750 750	mA
Output Energy (Capacitive Load per Cycle)	W	5.0	µJ
$R_{F\ Stby}$, C_T, Soft–Start, R_{ref}, $R_{P\ Stby}$ Inputs	V_{in}	–0.3 to 5.5	V
Foldback Input, Current Sense Input, E/A Output, Voltage Feedback Input, Overvoltage Protection, Synchronization Input	V_{in}	 –0.3 to V_{CC} + 0.3	V
Synchronization Input High State Voltage Low State Reverse Current	 V_{IH} V_{IL}	 V_{CC} + 0.3 –20	 V mA
Demagnetization Detection Input Current Source Sink	 $I_{demag–ib\ (Source)}$ $I_{demag–ib\ (Sink)}$	 –4.0 10	mA
Error Amplifier Output Sink Current	$I_{E/A\ (Sink)}$	20	mA
Power Dissipation and Thermal Characteristics P Suffix, Dual–In–Line, Case 648 Maximum Power Dissipation at T_A = 85°C Thermal Resistance, Junction–to–Air DW Suffix, Surface Mount, Case 751G Maximum Power Dissipation at T_A = 85°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 0.6 100 0.45 145	 W °C/W W °C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–25 to +85	°C

NOTES: 1. Maximum package power dissipation limits must be observed.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V, [Note 3], R_{ref} = 10 kΩ, C_T = 820 pF, for typical values T_A = 25°C, for min/max values T_A = –25° to +85°C [Note 4], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT SECTION					
Output Voltage (Note 5)					V
Low State (I_{Sink} = 100 mA)	V_{OL}	–	1.0	1.2	
(I_{Sink} = 500 mA)		–	1.4	2.0	
High State (I_{Source} = 200 mA)	V_{OH}	–	1.5	2.0	
(I_{Source} = 500 mA)		–	2.0	2.7	
Output Voltage During Initialization Phase	V_{OL}				V
V_{CC} = 0 to 1.0 V, I_{Sink} = 10 µA		–	–	1.0	
V_{CC} = 1.0 to 5.0 V, I_{Sink} = 100 µA		–	0.1	1.0	
V_{CC} = 5.0 to 13 V, I_{Sink} = 1.0 mA		–	0.1	1.0	
Output Voltage Rising Edge Slew–Rate (C_L = 1.0 nF, T_J = 25°C)	dVo/dT	–	300	–	V/µs
Output Voltage Falling Edge Slew–Rate (C_L = 1.0 nF, T_J = 25°C)	dVo/dT	–	–300	–	V/µs
ERROR AMPLIFIER SECTION					
Voltage Feedback Input ($V_{E/A\ out}$ = 2.5 V)	V_{FB}	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 2.5 V)	$I_{FB–ib}$	–2.0	–0.6	–	µA
Open Loop Voltage Gain ($V_{E/A\ out}$ = 2.0 to 4.0 V)	A_{VOL}	65	70	–	dB

NOTES: 3. Adjust V_{CC} above the startup threshold before setting to 12 V.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
5. V_C must be greater than 5.0 V.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} and V_C = 12 V, [Note 3], R_{ref} = 10 kΩ, C_T = 820 pF, for typical values T_A = 25°C, for min/max values T_A = –25° to +85°C [Note 4], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION (continued)					
Unity Gain Bandwidth	BW				MHz
T_J = 25°C		–	4.0	–	
T_J = –25° to +85°C		–	–	5.5	
Voltage Feedback Input Line Regulation (V_{CC} = 10 to 15 V)	$V_{FBline-reg}$	–10	–	10	mV
Output Current					mA
Sink ($V_{E/A\ out}$ = 1.5 V, V_{FB} = 2.7 V) T_A = –25° to +85°C	I_{Sink}	2.0	12	–	
Source ($V_{E/A\ out}$ = 5.0 V, V_{FB} = 2.3 V) T_A = –25° to +85°C	I_{Source}	–2.0	–	–0.2	
Output Voltage Swing					V
High State ($I_{E/A\ out\ (source)}$ = 0.5 mA, V_{FB} = 2.3 V)	V_{OH}	5.5	6.5	7.5	
Low State ($I_{E/A\ out\ (sink)}$ = 0.33 mA, V_{FB} = 2.7 V)	V_{OL}	–	1.0	1.1	
REFERENCE SECTION					
Reference Output Voltage (V_{CC} = 10 to 15 V)	V_{ref}	2.4	2.5	2.6	V
Reference Current Range ($I_{ref} = V_{ref}/R_{ref}$, R = 5.0 k to 25 kΩ)	I_{ref}	–500	–	–100	µA
Reference Voltage Over I_{ref} Range	ΔV_{ref}	–40	–	40	mV
OSCILLATOR AND SYNCHRONIZATION SECTION					
Frequency	f_{OSC}				kHz
T_A = 0° to +70°C		44.5	48	51.5	
T_A = –25° to +85°C		44	–	52	
Frequency Change with Voltage (V_{CC} = 10 to 15 V)	$\Delta f_{OSC}/\Delta V$	–	0.05	–	%/V
Frequency Change with Temperature (T_A = –25° to +85°C)	$\Delta f_{OSC}/\Delta T$	–	0.05	–	%/°C
Oscillator Voltage Swing (Peak–to–Peak)	$V_{OSC(pp)}$	1.65	1.8	1.95	V
Ratio Charge Current/Reference Current	I_{charge}/I_{ref}				–
T_A = 0° to +70°C (V_{CT} = 2.0 V)		0.375	0.4	0.425	
T_A = –25° to +85°C		0.37	–	0.43	
Fixed Maximum Duty Cycle = $I_{discharge}/(I_{discharge} + I_{charge})$	D	78	80	82	%
Ratio Standby Discharge Current versus $I_{R\ F\ Stby}$ (Note 6)	$I_{disch-Stby}/I_{R\ F\ Stby}$				–
T_A = 0° to +70°C		0.46	0.53	0.6	
T_A = –25° to +85°C (Note 8)		0.43	–	0.63	
$V_{R\ F\ Stby}$ ($I_{R\ F\ Stby}$ = 100 µA)	$V_{R\ F\ Stby}$	2.4	2.5	2.6	V
Frequency in Standby Mode ($R_{F\ Stby}$ (Pin 15) = 25 kΩ)	F_{Stby}	18	21	24	kHz
Current Range	$I_{R\ F\ Stby}$	–200	–	–50	µA
Synchronization Input Threshold Voltage (Note 7)	V_{inthH}	3.2	3.7	4.3	V
	V_{inthL}	0.45	0.7	0.9	
Synchronization Input Current	$I_{Sync-in}$	–5.0	–	0	µA
Minimum Synchronization Pulse Width (Note 8)	T_{Sync}	–	–	0.5	µs
UNDERVOLTAGE LOCKOUT SECTION					
Startup Threshold	$V_{stup-th}$	13.6	14.5	15.4	V
Output Disable Voltage After Threshold Turn–On (UVLO 1)	$V_{disable1}$				V
T_A = 0° to +70°C		8.6	9.0	9.4	
T_A = –25° to +85°C		8.3	–	9.6	
Reference Disable Voltage After Threshold Turn–On (UVLO 2)	$V_{disable2}$	7.0	7.5	8.0	V

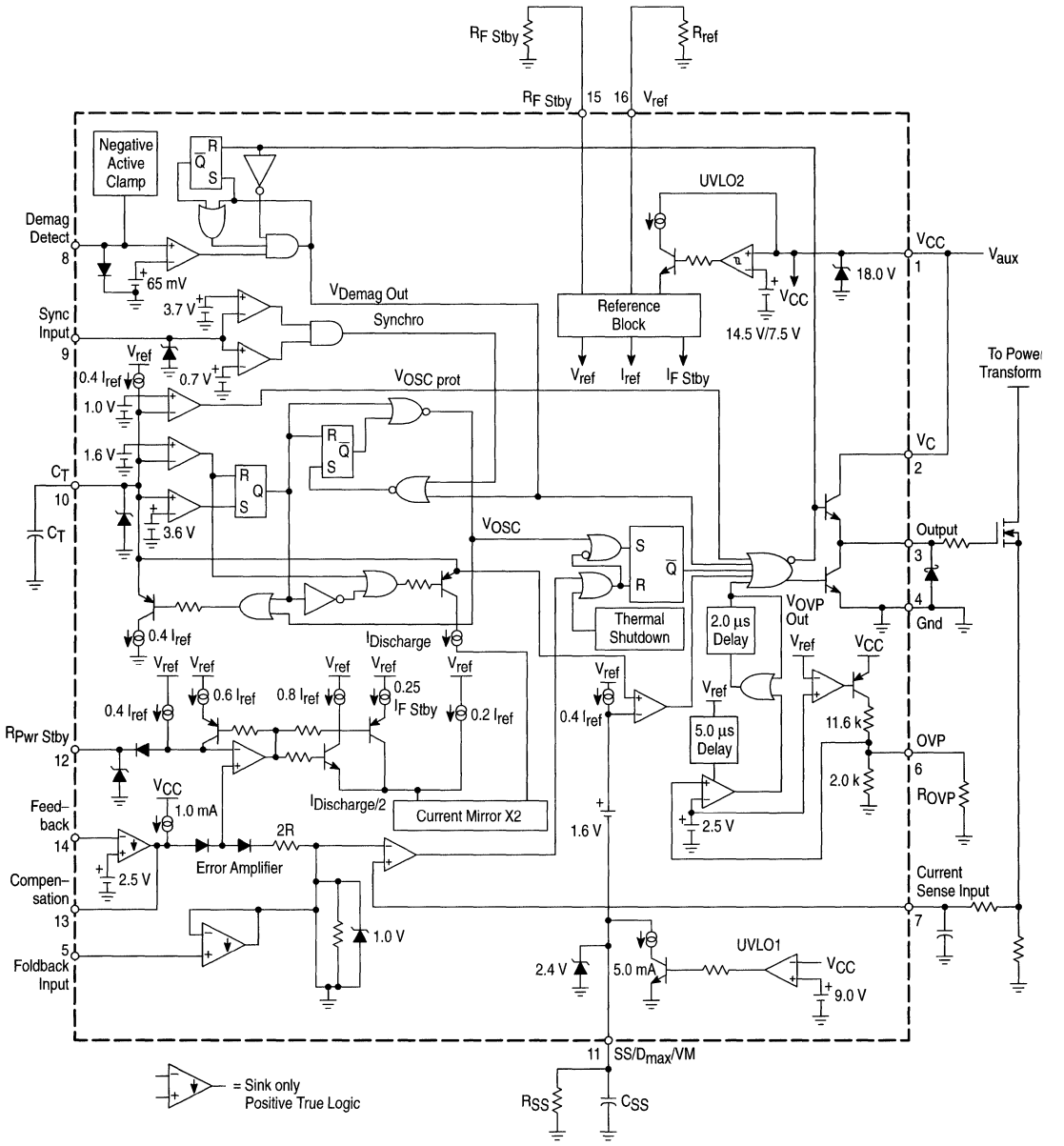
NOTES: 3. Adjust V_{CC} above the startup threshold before setting to 12 V.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
6. Standby is disabled for $V_{R\ P\ Stby}$ < 25 mV typical.
7. If not used, Synchronization input must be connected to Ground.
8. Synchronization Pulse Width must be shorter than $T_{OSC} = 1/f_{OSC}$.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} and V_C = 12 V, [Note 3], R_{ref} = 10 kΩ, C_T = 820 pF, for typical values T_A = 25°C, for min/max values T_A = −25° to +85°C [Note 4], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DEMAGNETIZATION DETECTION SECTION (Note 9)					
Demagnetization Detect Input					
Demagnetization Comparator Threshold ($V_{Pin\ 9}$ Decreasing)	$V_{demag-th}$	50	65	80	mV
Propagation Delay (Input to Output, Low to High)	–	–	0.25	–	µs
Input Bias Current (V_{demag} = 65 mV)	$I_{demag-Ib}$	−0.5	–	–	µA
Negative Clamp Level (I_{demag} = −2.0 mA)	$C_{L(neg)}$	–	−0.38	–	V
Positive Clamp Level (I_{demag} = 2.0 mA)	$C_{L(pos)}$	–	0.72	–	V
SOFT–START SECTION (Note 11)					
Ratio Charge Current/I_{ref}	$I_{ss(ch)}/I_{ref}$				–
T_A = 0° to +70°C		0.37	0.4	0.43	
T_A = −25° to +85°C		0.36	–	0.44	
Discharge Current ($V_{soft-start}$ = 1.0 V)	$I_{discharge}$	1.5	5.0	–	mA
Clamp Level	$V_{ss(CL)}$	2.2	2.4	2.6	V
Duty Cycle ($R_{soft-start}$ = 12 kΩ)	$D_{soft-start\ 12k}$	36	42	49	%
($V_{soft-start\ (Pin\ 11)}$ = 0.1 V)	$D_{soft-start}$	–	–	0	
OVERVOLTAGE SECTION					
Protection Threshold Level on V_{OVP}	V_{OVP-th}	2.42	2.5	2.58	V
Propagation Delay (V_{OVP} > 2.58 V to V_{out} Low)		1.0	–	3.0	µs
Protection Level on V_{CC}	$V_{CC\ prot}$				V
T_A = 0° to +70°C		16.1	17	17.9	
T_A = −25° to +85°C		15.9	–	18.1	
Input Resistance	–				kΩ
T_A = 0° to +70°C		1.5	2.0	3.0	
T_A = −25° to +85°C		1.4	–	3.4	
FOLDBACK SECTION (Note 10)					
Current Sense Voltage Threshold ($V_{foldback\ (Pin\ 5)}$ = 0.9 V)	V_{CS-th}	0.86	0.89	0.9	V
Foldback Input Bias Current ($V_{foldback\ (Pin\ 5)}$ = 0 V)	$I_{foldback-Ib}$	−6.0	−2.0	–	µA
STANDBY SECTION					
Ratio $I_{R\ P\ Stby}/I_{ref}$	$I_{R\ P\ Stby}/I_{ref}$				–
T_A = 0° to +70°C		0.37	0.4	0.43	
T_A = −25° to +85°C		0.36	–	0.44	
Ratio Hysteresis (V_h Required to Return to Normal Operation from Standby Operation)	$V_h/V_{R\ P\ Stby}$				–
T_A = 0° to +70°C		1.42	1.5	1.58	
T_A = −25° to +85°C		1.4	–	1.6	
Current Sense Voltage Threshold ($V_{R\ P\ Stby\ (Pin\ 12)}$ = 1.0 V)	$V_{CS-Stby}$	0.28	0.31	0.34	V
CURRENT SENSE SECTION					
Maximum Current Sense Input Threshold ($V_{feedback\ (Pin\ 14)}$ = 2.3 V and $V_{foldback\ (Pin\ 6)}$ = 1.2 V)	V_{CS-th}	0.96	1.0	1.04	V
Input Bias Current	I_{CS-ib}	−10	−2.0	–	µA
Propagation Delay (Current Sense Input to Output at V_{TH} of MOS transistor = 3.0 V)	–	–	120	200	ns
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Startup (V_{CC} = 13 V with V_{CC} Increasing)		–	0.3	0.45	
Operating T_A = −25° to +85°C (Note 3)		13	17	20	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	18.5	–	–	V
Thermal Shutdown	–	–	155	–	°C

NOTES: 3. Adjust V_{CC} above the startup threshold before setting to 12 V.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
9. This function can be inhibited by connecting Pin 8 to Gnd. This allows a continuous current mode operation.
10. This function can be inhibited by connecting Pin 5 to V_{CC}.
11. The MC44603 can be shut down by connecting the Soft–Start pin (Pin 11) to Ground.

Representative Block Diagram



This device contains 243 active transistors.

Figure 1. Timing Resistor versus Oscillator Frequency

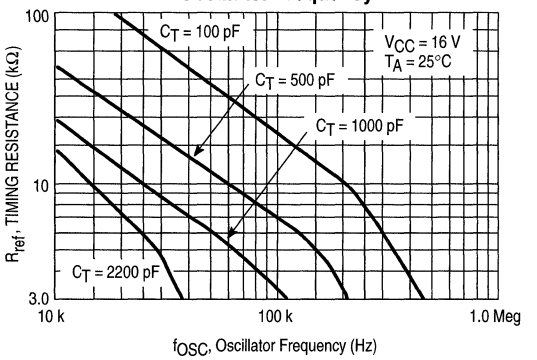


Figure 2. Standby Mode Timing Capacitor versus Oscillator Frequency

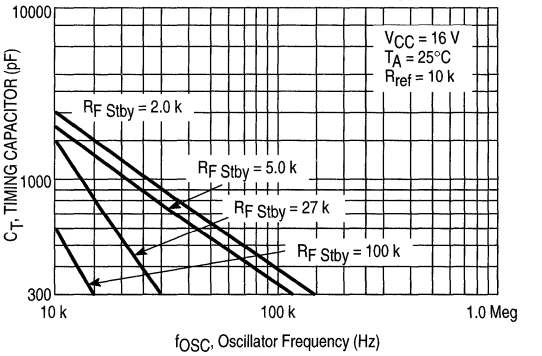


Figure 3. Oscillator Frequency versus Temperature

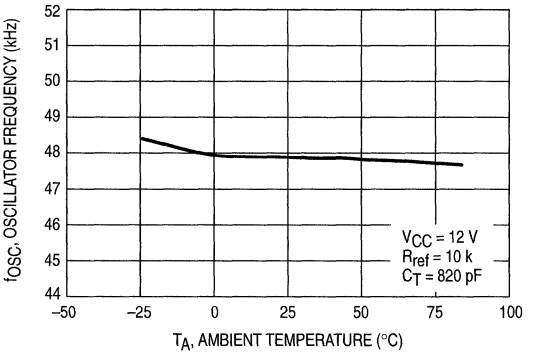


Figure 4. Ratio Charge Current/Reference Current versus Temperature

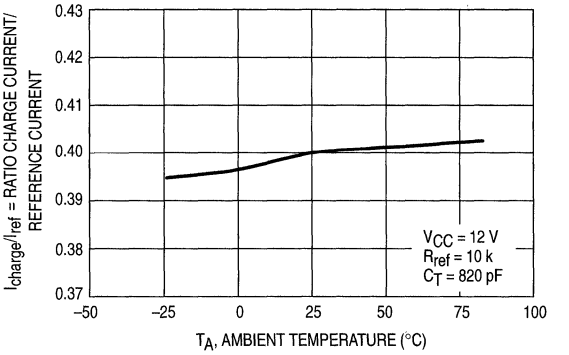


Figure 5. Output Waveform

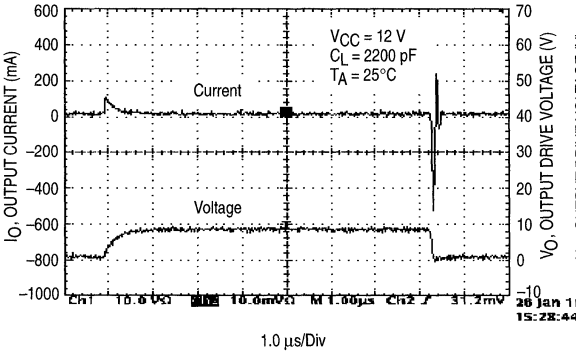


Figure 6. Output Cross Conduction

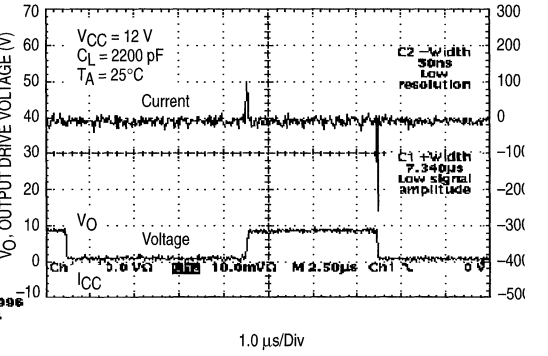


Figure 7. Oscillator Discharge Current versus Temperature

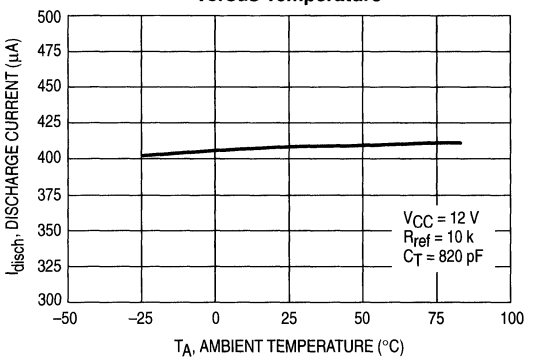


Figure 8. Source Output Saturation Voltage versus Load Current

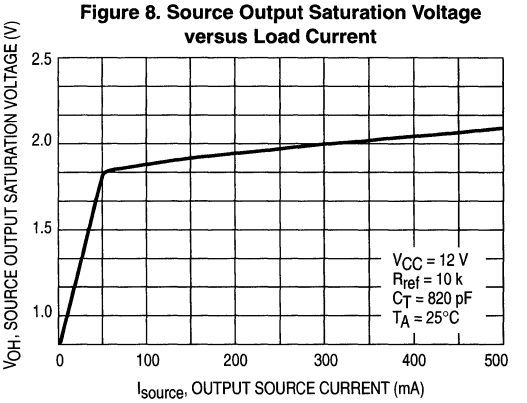


Figure 9. Sink Output Saturation Voltage versus Sink Current

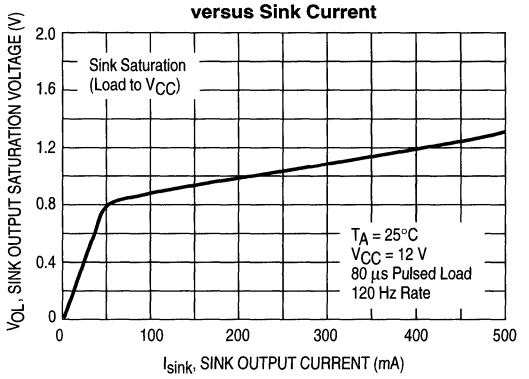


Figure 10. Error Amplifier Gain and Phase versus Frequency

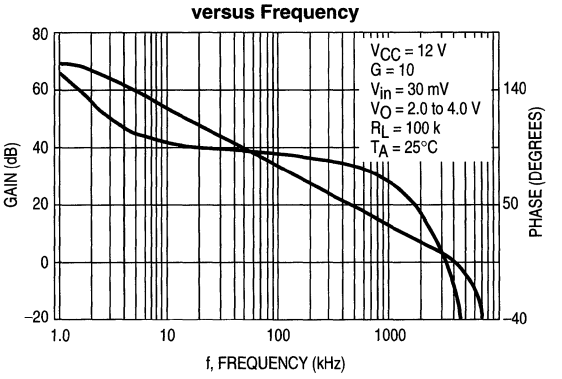


Figure 11. Voltage Feedback Input versus Temperature

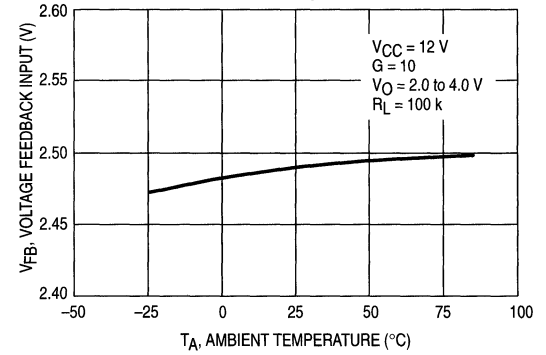


Figure 12. Demag Comparator Threshold versus Temperature

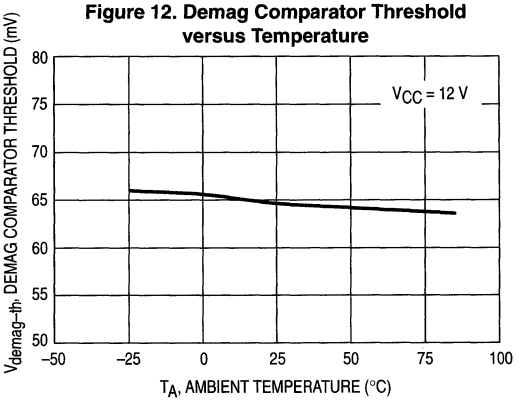


Figure 13. Current Sense Gain versus Temperature

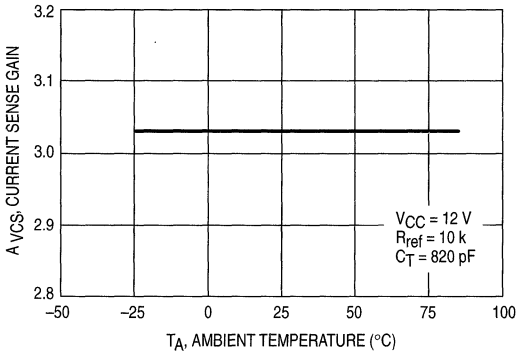


Figure 14. Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

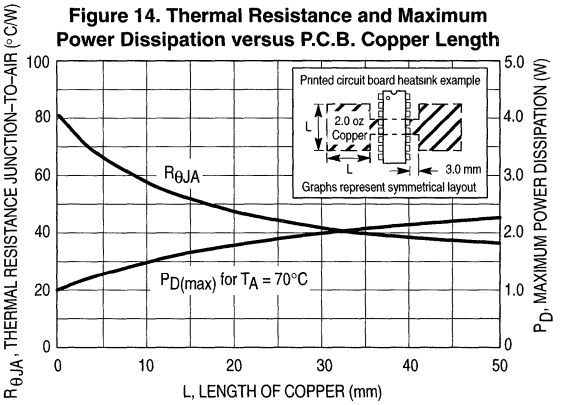


Figure 15. Propagation Delay Current Sense Input to Output versus Temperature

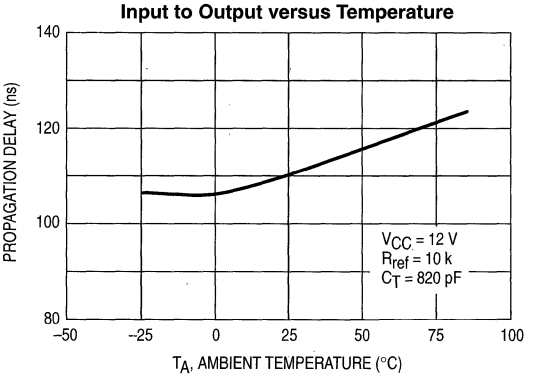


Figure 16. Startup Current versus V_{CC}

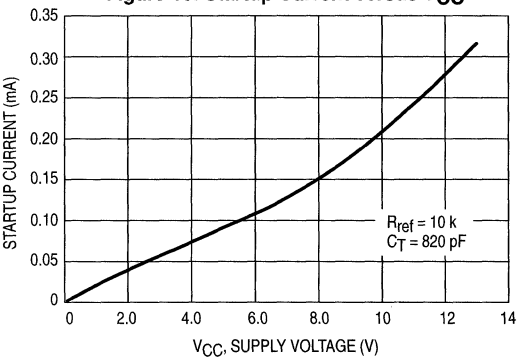


Figure 17. Supply Current versus Supply Voltage

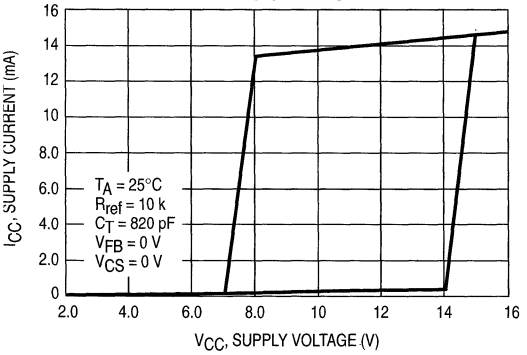


Figure 18. Power Supply Zener Voltage versus Temperature

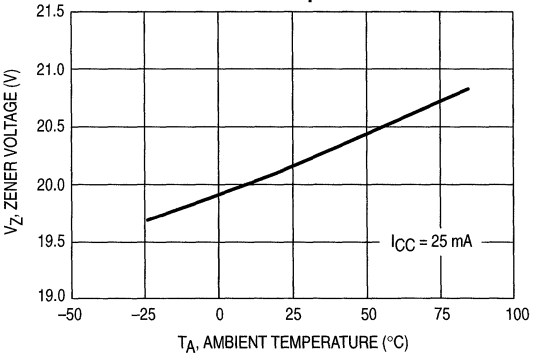


Figure 19. Startup Threshold Voltage versus Temperature

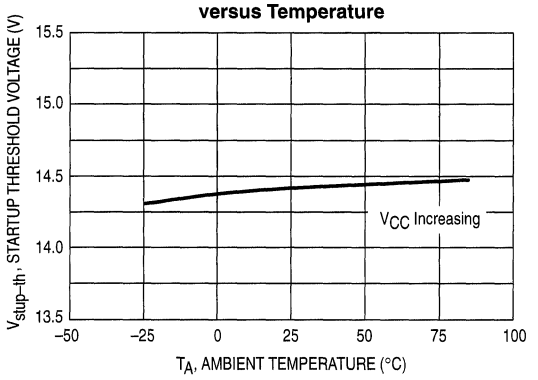


Figure 20. Disable Voltage After Threshold Turn–On (UVLO1) versus Temperature

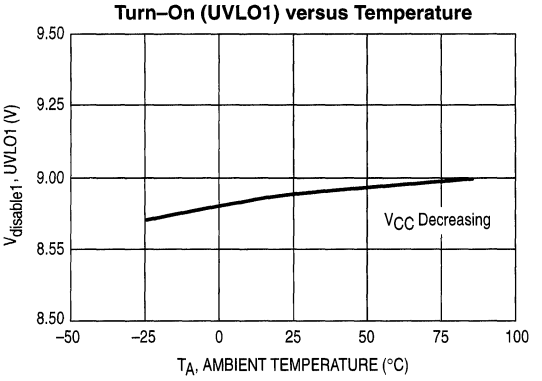


Figure 21. Disable Voltage After Threshold Turn–On (UVLO2) versus Temperature

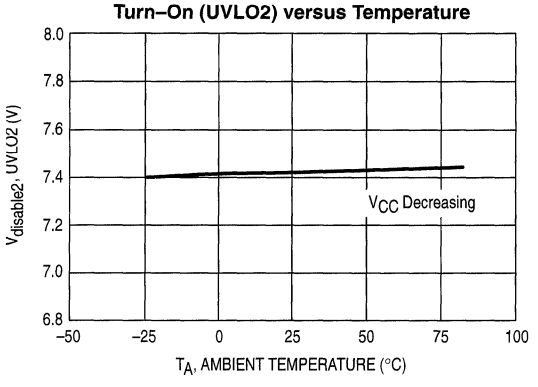


Figure 22. Protection Threshold Level on V_{OVP} versus Temperature

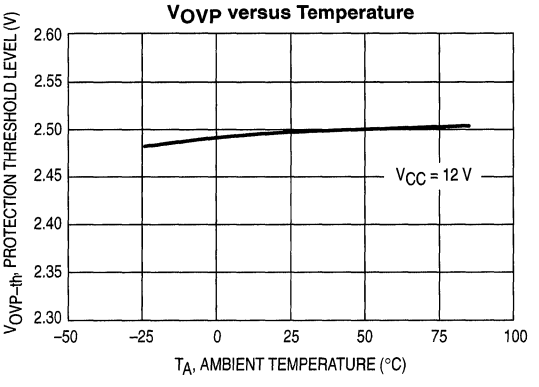


Figure 23. Protection Level on V_{CC} versus Temperature

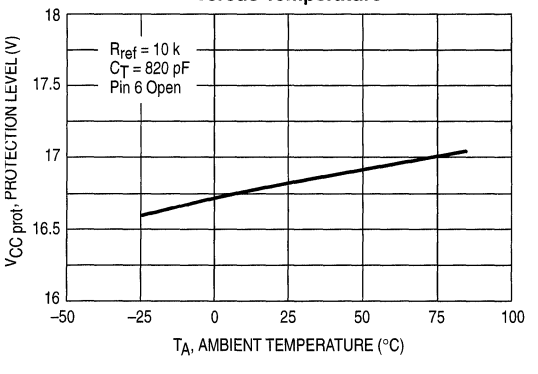


Figure 24. Propagation Delay (V_{OVP} > 2.58 V to V_{out} Low) versus Temperature

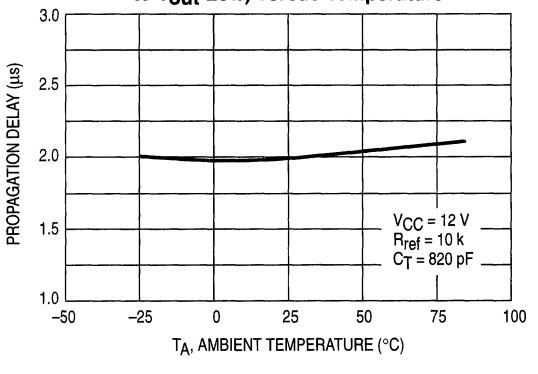


Figure 25. Standby Reference Current versus Temperature

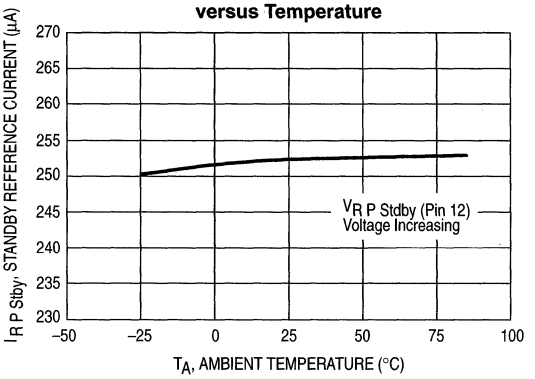
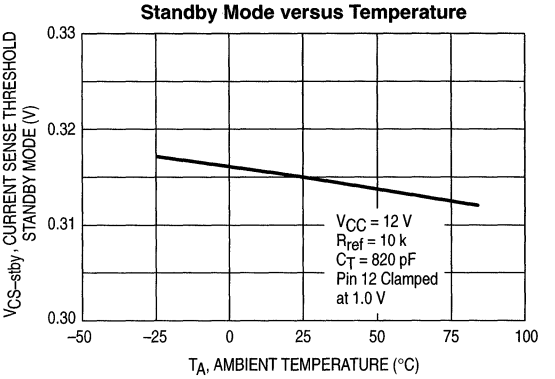


Figure 26. Current Sense Voltage Threshold Standby Mode versus Temperature



PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	V_{CC}	This pin is the positive supply of the IC. The operating voltage range after startup is 9.0 to 14.5 V.
2	V_C	The output high state (V_{OH}) is set by the voltage applied to this pin. With a separate connection to the power source, it can reduce the effects of switching noise on the control circuitry.
3	Output	Peak currents up to 750 mA can be sourced or sunk, suitable for driving either MOSFET or Bipolar transistors. This output pin must be shunted by a Schottky diode, 1N5819 or equivalent.
4	Gnd	The ground pin is a single return, typically connected back to the power source; it is used as control and power ground.
5	Foldback Input	The foldback function provides overload protection. Feeding the foldback input with a portion of the V_{CC} voltage (1.0 V max) establishes on the system control loop a foldback characteristic allowing a smoother startup and sharper overload protection. Above 1.0 V the foldback input is inactive.
6	Overvoltage Protection	When the overvoltage protection pin receives a voltage greater than 17 V, the device is disabled and requires a complete restart sequence. The overvoltage level is programmable.
7	Current Sense Input	A voltage proportional to the current flowing into the power switch is connected to this input. The PWM latch uses this information to terminate the conduction of the output buffer when working in a current mode of operation. A maximum level of 1.0 V allows either current or voltage mode operation.
8	Demagnetization Detection	A voltage delivered by an auxiliary transformer winding provides to the demagnetization pin an indication of the magnetization state of the flyback transformer. A zero voltage detection corresponds to complete core saturation. The demagnetization detection ensures a discontinuous mode of operation. This function can be inhibited by connecting Pin 8 to Gnd.
9	Synchronization Input	The synchronization input pin can be activated with either a negative pulse going from a level between 0.7 V and 3.7 V to Gnd or a positive pulse going from a level between 0.7 V and 3.7 V up to a level higher than 3.7 V. The oscillator runs free when Pin 9 is connected to Gnd.
10	C_T	The normal mode oscillator frequency is programmed by the capacitor C_T choice together with the R_{ref} resistance value. C_T, connected between Pin 10 and Gnd, generates the oscillator sawtooth.
11	Soft–Start/D_{max}/ Voltage–Mode	A capacitor, resistor or a voltage source connected to this pin limits the switching duty–cycle. This pin can be used as a voltage mode control input. By connecting Pin 11 to Ground, the MC44603 can be shut down.
12	R_P Standby	A voltage level applied to the R_P Standby pin determines the output power level at which the oscillator will turn into the reduced frequency mode of operation (i.e. standby mode). An internal hysteresis comparator allows to return in the normal mode at a higher output power level.
13	E/A Out	The error amplifier output is made available for loop compensation.
14	Voltage Feedback	This is the inverting input of the Error Amplifier. It can be connected to the switching power supply output through an optical (or other) feedback loop.
15	R_F Standby	The reduced frequency or standby frequency programming is made by the R_F Standby resistance choice.
16	R_{ref}	R_{ref} sets the internal reference current. The internal reference current ranges from 100 μA to 500 μA. This requires that 5.0 kΩ ≤ R_{ref} ≤ 25 kΩ.

Figure 27. Starting Behavior and Overvoltage Management

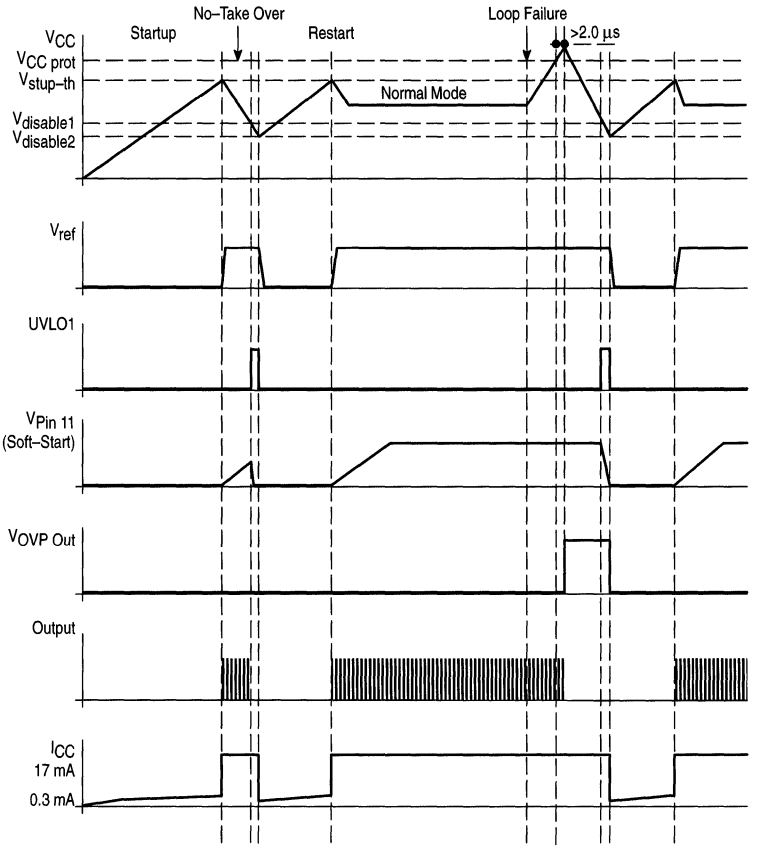
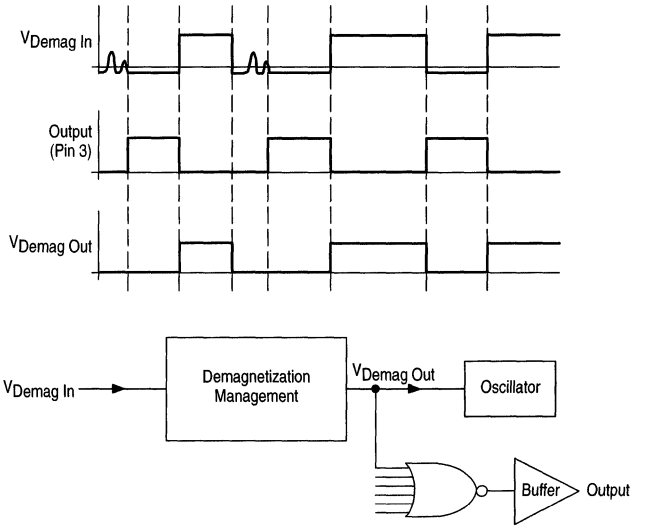


Figure 28. Demagnetization



3

Figure 29. Switching Off Behavior

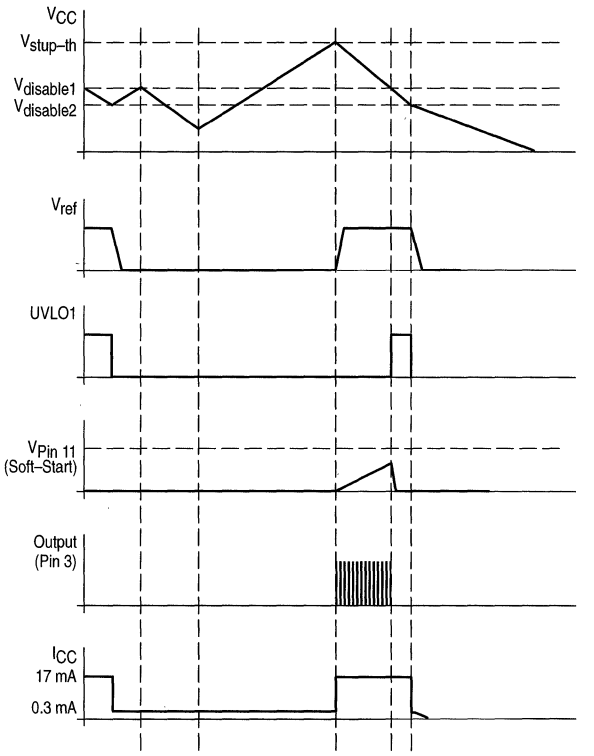


Figure 30. Oscillator

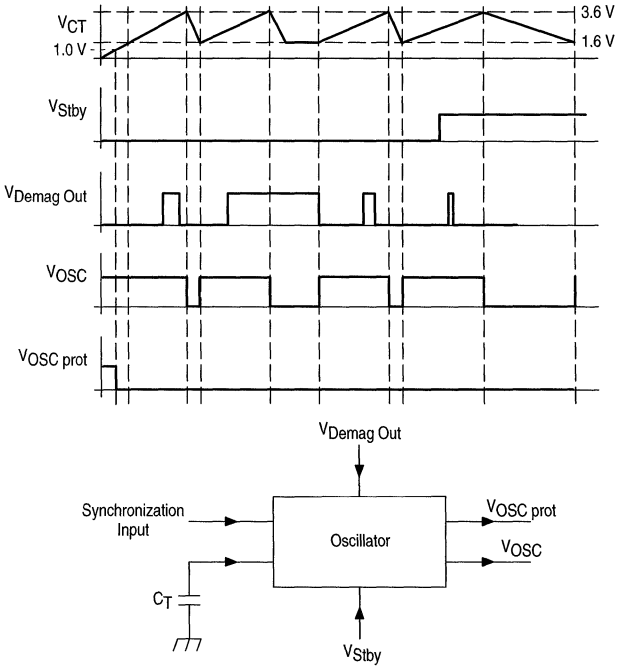
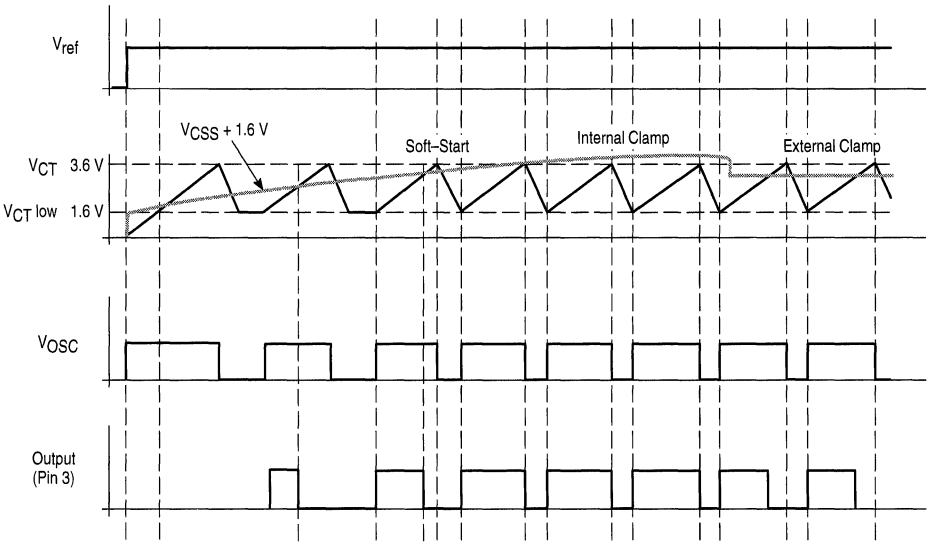


Figure 31. Soft–Start & D_{max}



OPERATING DESCRIPTION

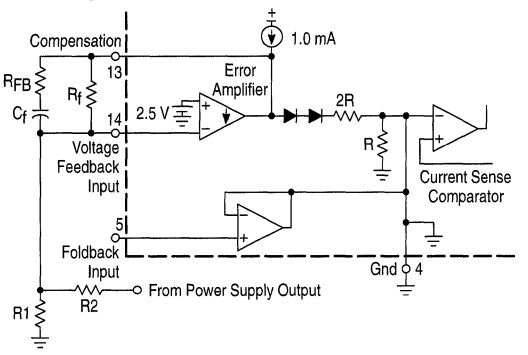
Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 70 dB. The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current with the inverting input at 2.5 V is –2.0 μA. This can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 13) is provided for external loop compensation. The output voltage is offset by two diode drops (≈ 1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 3) when Pin 13 is at its lowest state (V_{OL}). The Error Amp minimum feedback resistance is limited by the amplifier's minimum source current (0.2 mA) and the required output voltage (V_{OH}) to reach the current sense comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.2\ mA} = 22\ k\Omega$$

Figure 32. Error Amplifier Compensation



Current Sense Comparator and PWM Latch

The MC44603 can operate as a current mode controller or as a voltage mode controller. In current mode operation, the MC44603 uses the current sense comparator. The output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level

established by the Error Amplifier output (Pin 13). Thus, the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator PWM Latch ensures that only a single pulse appears at the Source Output during the appropriate oscillator cycle.

The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the power switch Q1.

This voltage is monitored by the Current Sense Input (Pin 7) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 13 where:

$$I_{pk} \approx \frac{V_{(Pin\ 13)} - 1.4\ V}{3\ R_S}$$

The Current Sense Comparator threshold is internally clamped to 1.0 V. Therefore, the maximum peak switch current is:

$$I_{pk(max)} \approx \frac{1.0\ V}{R_S}$$

Figure 33. Output Totem Pole

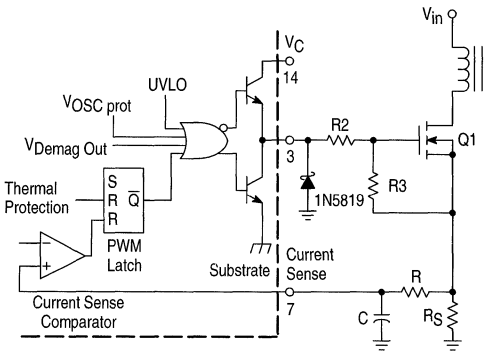


Figure 34. Oscillator

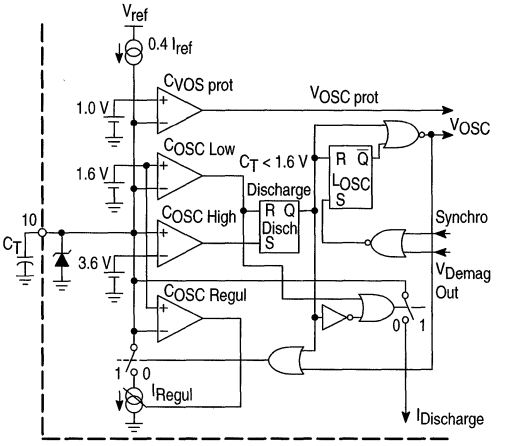
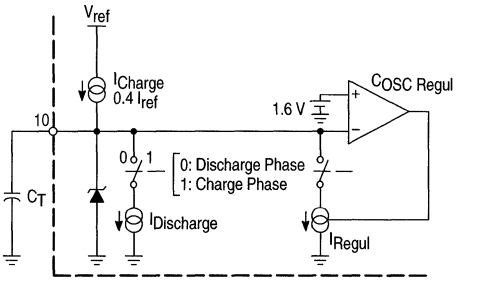


Figure 35. Simplified Block Oscillator



Oscillator

The oscillator is a very accurate sawtooth generator that can work either in free mode or in synchronization mode. In this second mode, the oscillator stops in the low state and waits for a demagnetization or a synchronization pulse to start a new charging cycle.

- **The Sawtooth Generation:**

In the steady state, the oscillator voltage varies between about 1.6 V and 3.6 V.

The sawtooth is obtained by charging and discharging an external capacitor C_T (Pin 10), using two distinct current sources = I_{charge} and $I_{discharge}$. In fact, C_T is permanently connected to the charging current source (0.4 I_{ref}) and so, the discharge current source has to be higher than the charge current to be able to decrease the C_T voltage (refer to Figure 35).

This condition is performed, its value being (2.0 I_{ref}) in normal working and (0.4 I_{ref} + 0.5 $I_{F\ Stby}$ in standby mode).

Two comparators are used to generate the sawtooth. They compare the C_T voltage to the oscillator valley (1.6 V) and peak reference (3.6 V) values. A latch (L_{disch}) memorizes the oscillator state.

In addition to the charge and discharge cycles, a third state can exist. This phase can be produced when, at the end of the discharge phase, the oscillator has to wait for a synchronization or demagnetization pulse before restarting. During this delay, the C_T voltage must remain equal to the oscillator valley value ($\simeq$1.6 V). So, a third regulated current source I_{Regul} controlled by $C_{OSC\ Regul}$, is connected to C_T in order to perfectly compensate the (0.4 I_{ref}) current source that permanently supplies C_T.

The maximum duty cycle is 80%. Indeed, the on–time is allowed only during the oscillator capacitor charge.

Consequently:

$T_{charge} = C_T \times \Delta V / I_{charge}$

$T_{discharge} = C_T \times \Delta V / I_{discharge}$

where:

T_{charge} is the oscillator charge time

ΔV is the oscillator peak–to–peak value

I_{charge} is the oscillator charge current

and

$T_{discharge}$ is the oscillator discharge time

$I_{discharge}$ is the oscillator discharge current

So, as $f_S = 1/(T_{charge} + T_{discharge})$ when the Regul arrangement is not activated, the operating frequency can be obtained from the graph in Figure 1.

NOTE: The output is disabled by the signal $V_{OSC\ prot}$ when V_{CT} is lower than 1.0 V (refer to Figure 30).

Synchronization and Demagnetization Blocks

To enable the output, the L_{OSC} latch complementary output must be low. Reset is activated by the L_{disch} output during the discharge phase. To restart, the L_{OSC} has to be set (refer to Figure 34). To perform this, the demagnetization signal and the synchronization must be low.

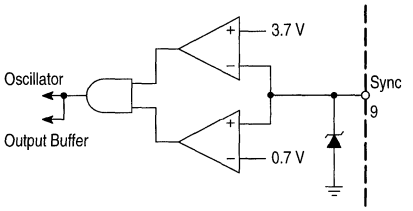
- **Synchronization:**

The synchronization block consists of two comparators that compare the synchronization signal (external) to 0.7 and 3.7 V (typical values). The comparators' outputs are connected to the input of an AND gate so that the final output of the block should be :

– high when 0.7 < SYNC < 3.7 V
– low in the other cases.

As a low level is necessary to enable the output, synchronized low level pulses have to be generated on the output of the synchronization block. If synchronization is not required, the Pin 9 must be connected to the ground.

Figure 36. Synchronization



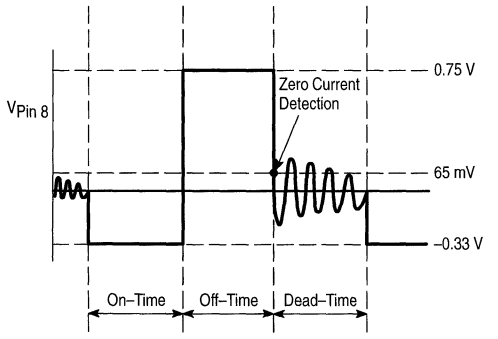
- **Demagnetization:**

In flyback applications, a good means to detect magnetic saturation of the transformer core, or demagnetization, consists in using the auxiliary winding voltage. This voltage is:

– negative during the on–time,
– positive during the off–time,
– equal to zero for the dead–time with generally some ringing (refer to Figure 37).

That is why, the MC44603 demagnetization detection consists of a comparator that can compare the auxiliary winding voltage to a reference that is typically equal to 65 mV.

Figure 37. Demagnetization Detection



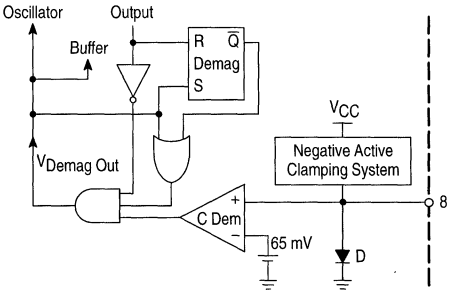
A diode D has been incorporated to clamp the positive applied voltages while an active clamping system limits the negative voltages to typically –0.33 V. This negative clamp level is sufficient to avoid the substrate diode switching on.

In addition to the comparator, a latch system has been incorporated in order to keep the demagnetization block output level low as soon as a voltage lower than 65 mV is detected and as long as a new restart is produced (high level on the output) (refer to Figure 38). This process prevents ringing on the signal at Pin 8 from disrupting the demagnetization detection. This results in a very accurate demagnetization detection.

The demagnetization block output is also directly connected to the output, disabling it during the demagnetization phase (refer to Figure 33).

NOTE: The demagnetization detection can be inhibited by connecting Pin 8 to the ground.

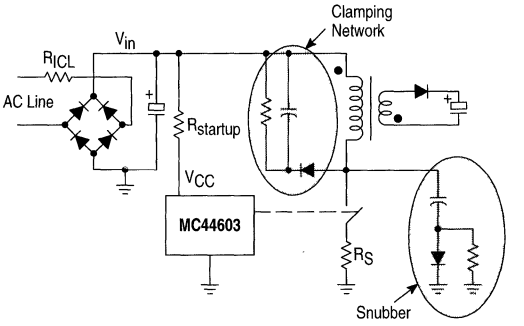
Figure 38. Demagnetization Block



Standby

- **Power Losses in a Classical Flyback Structure**

Figure 39. Power Losses in a Classical Flyback Structure



In a classical flyback (as depicted in Figure 39), the standby losses mainly consist of the energy waste due to:

– the startup resistor $R_{startup}$	$P_{startup}$
– the consumption of the IC and the power switch control	$P_{control}$
– the inrush current limitation resistor R_{ICL}	P_{ICL}
– the switching losses in the power switch	P_{SW}
– the snubber and clamping network	$P_{SN–CLN}$

$P_{startup}$ is nearly constant and is equal to:

$$((V_{in}–V_{CC})^2/R_{startup})$$

3

P_{ICL} only depends on the current drawn from the mains. Losses can be considered constant. This waste of energy decreases when the standby losses are reduced.

$P_{control}$ increases when the oscillator frequency is increased (each switching requires some energy to turn on the power switch).

P_{SW} and P_{SN-CLN} are proportional to the switching frequency.

Consequently, standby losses can be minimized by decreasing the switching frequency as much as possible.

The MC44603 was designed to operate at a standby frequency lower than the normal working one.

- **Standby Power Calculations with MC44603**

During a switching period, the energy drawn by the transformer during the on–time to be transferred to the output during the off–time, is equal to:

$$E = \frac{1}{2} \times L \times I_{pk}^2$$

where:

– L is the transformer primary inductor,
– I_{pk} is the inductor peak current.

Input power is labelled P_{in}:

$$P_{in} = 0.5 \times L \times I_{pk}^2 \times f_S$$

where f_S is the normal working switching frequency.

Also,

$$I_{pk} = \frac{V_{CS}}{R_S}$$

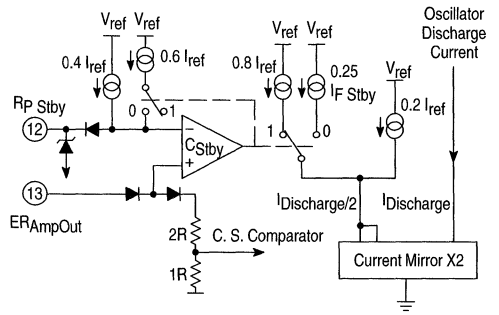
where R_S is the resistor used to measure the power switch current.

Thus, the input power is proportional to V_{CS}^2 (V_{CS} being the internal current sense comparator input).

That is why the standby detection is performed by creating a V_{CS} threshold. An internal current source ($0.4 \times I_{ref}$) sets the threshold level by connecting a resistor to Pin 12.

As depicted in Figure 40, the standby comparator noninverting input voltage is typically equal to ($3.0 \times V_{CS} + V_F$) while the inverter input value is ($V_{R\ P\ Stby} + V_F$).

Figure 40. Standby



The V_{CS} threshold level is typically equal to [($V_{R\ P\ Stby}$)/3] and if the corresponding power threshold is labelled P_{thL}:

$$P_{thL} = 0.5 \times L \times \left(\frac{V_{R\ P\ Stby}}{3.0\ R_S}\right)^2 \times f_S$$

And as:

$$V_{R\ P\ Stby} = R_{P\ Stby} \times 0.4 \times I_{ref}$$

$$= R_{R\ P\ Stby} \times 0.4 \times \frac{V_{ref}}{R_{ref}}$$

$$R_{P\ Stby} = \frac{10.6 \times R_S \times R_{ref}}{V_{ref}} \times \sqrt{\frac{P_{thL}}{L \times f_S}}$$

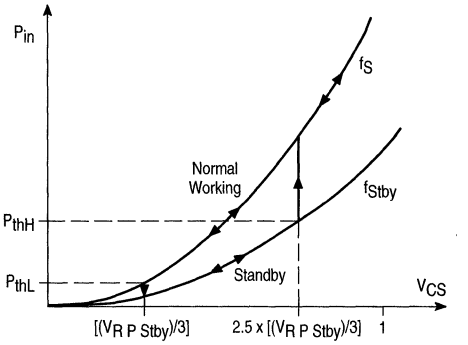
Thus, when the power drawn by the converter decreases, V_{CS} decreases and when V_{CS} becomes lower than [V_{CS-th} x ($V_{R\ P\ Stby}$)/3], the standby mode is activated. This results in an oscillator discharge current reduction in order to increase the oscillator period and to diminish the switching frequency. As it is represented in Figure 40, the ($0.8 \times I_{ref}$) current source is disconnected and is replaced by a lower value one ($0.25 \times I_{F\ Stby}$).

Where: $I_{F\ Stby} = V_{ref}/R_{F\ Stby}$

In order to prevent undesired mode switching when power is close to the threshold value, a hysteresis that is proportional to $V_{R\ P\ Stby}$ is incorporated creating a second V_{CS} threshold level that is equal to [2.5 x ($V_{R\ P\ Stby}$)/3]. When the standby comparator output is high, a second current source ($0.6 \times I_{ref}$) is connected to Pin 12.

Finally, the standby mode function can be shown graphically in Figure 41.

Figure 41. Dynamic Mode Change



This curve shows that there are two power threshold levels:

– the low one:

P_{thL} fixed by $V_{R\ P\ Stby}$

– the high one:

$$P_{thH} = (2.5)^2 \times P_{thL} \times \frac{f_{Stby}}{f_S}$$

$$P_{thH} = 6.25 \times P_{thL} \times \frac{f_{Stby}}{f_S}$$

Maximum Duty Cycle and Soft–Start Control

Maximum duty cycle can be limited to values less than 80% by utilizing the D_{max} and soft–start control. As depicted in Figure 42, the Pin 11 voltage is compared to the oscillator sawtooth.

Figure 42. D_{max} and Soft–Start

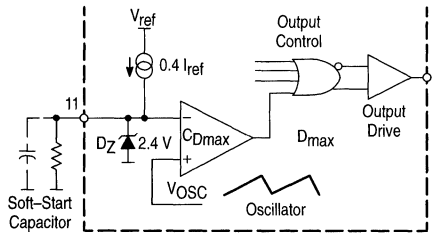
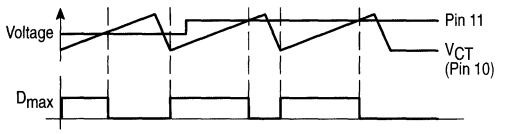


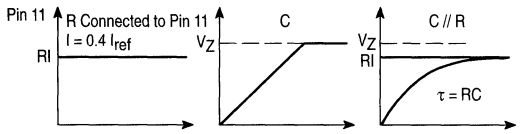
Figure 43. Maximum Duty Cycle Control



Using the internal current source (0.4 I_{ref}), the Pin 11 voltage can easily be set by connecting a resistor to this pin.

If a capacitor is connected to Pin 11, the voltage increases from 0 to its maximum value progressively (refer to Figure 44), thereby, implementing a soft–start. The soft–start capacitor is discharged internally when the V_{CC} (Pin 1) voltage drops below 9.0 V.

Figure 44. Different Possible Uses of Pin 11



If no external component is connected to Pin 11, an internal zener diode clamps the Pin 11 voltage to a value V_Z that is higher than the oscillator peak value, disabling soft–start and maximum duty cycle limitation.

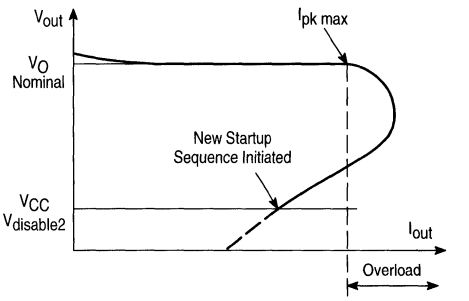
Foldback

As depicted in Fgure 32, the foldback input (Pin 5) can be used to reduce the maximum V_{CS} value, providing foldback protection. The foldback arrangement is a programmable peak current limitation.

If the output load is increased, the required converter peak current becomes higher and V_{CS} increases until it reaches its maximum value (normally, $V_{CS\ max}$ = 1.0 V).

Then, if the output load keeps on increasing, the system is unable to supply enough energy to maintain the output voltages in regulation. Consequently, the decreasing output can be applied to Pin 5, in order to limit the maximum peak current. In this way, the well known foldback characteristic can be obtained (refer to Figure 45).

Figure 45. Foldback Characteristic



NOTE: Foldback is disabled by connecting Pin 5 to V_{CC}.

Overvoltage Protection

The overvoltage arrangement consists of a comparator that compares the Pin 6 voltage to V_{ref} (2.5 V) (refer to Figure 46).

If no external component is connected to Pin 6, the comparator noninverting input voltage is nearly equal to:

$$\left(\frac{2.0\ k\Omega}{11.6\ k\Omega + 2.0\ k\Omega}\right) \times V_{CC}$$

The comparator output is high when:

$$\left(\frac{2.0\ k\Omega}{11.6\ k\Omega + 2.0\ k\Omega}\right) \times V_{CC} \geq 2.5\ V$$

$$\Leftrightarrow V_{CC} \geq 17\ V$$

A delay latch (2.0 µs) is incorporated in order to sense overvoltages that last at least 2.0 µs.

If this condition is achieved, $V_{OVP\ out}$, the delay latch output, becomes high. As this level is brought back to the input through an OR gate, $V_{OVP\ out}$ remains high (disabling the IC output) until V_{ref} is disabled.

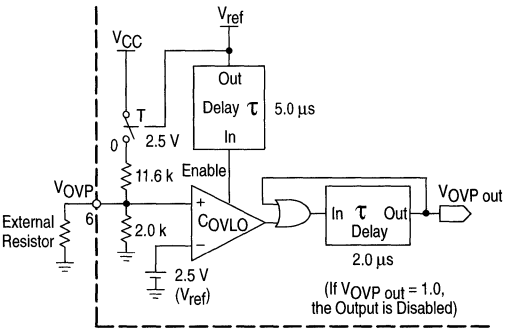
Consequently, when an overvoltage longer than 2.0 µs is detected, the output is disabled until V_{CC} is removed and then re–applied.

The V_{CC} is connected after V_{ref} has reached steady state in order to limit the circuit startup consumption.

The overvoltage section is enabled 5.0 µs after the regulator has started to allow the reference V_{ref} to stabilize.

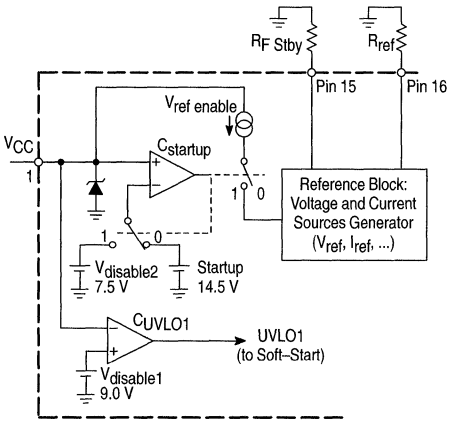
By connecting an external resistor to Pin 6, the threshold V_{CC} level can be changed.

Figure 46. Overvoltage Protection



Undervoltage Lockout Section

Figure 47. V_{CC} Management



As depicted in Figure 47, an undervoltage lockout has been incorporated to guarantee that the IC is fully functional before allowing system operation.

This block particularly, produces V_{ref} (Pin 16 voltage) and I_{ref} that is determined by the resistor R_{ref} connected between Pin 16 and the ground:

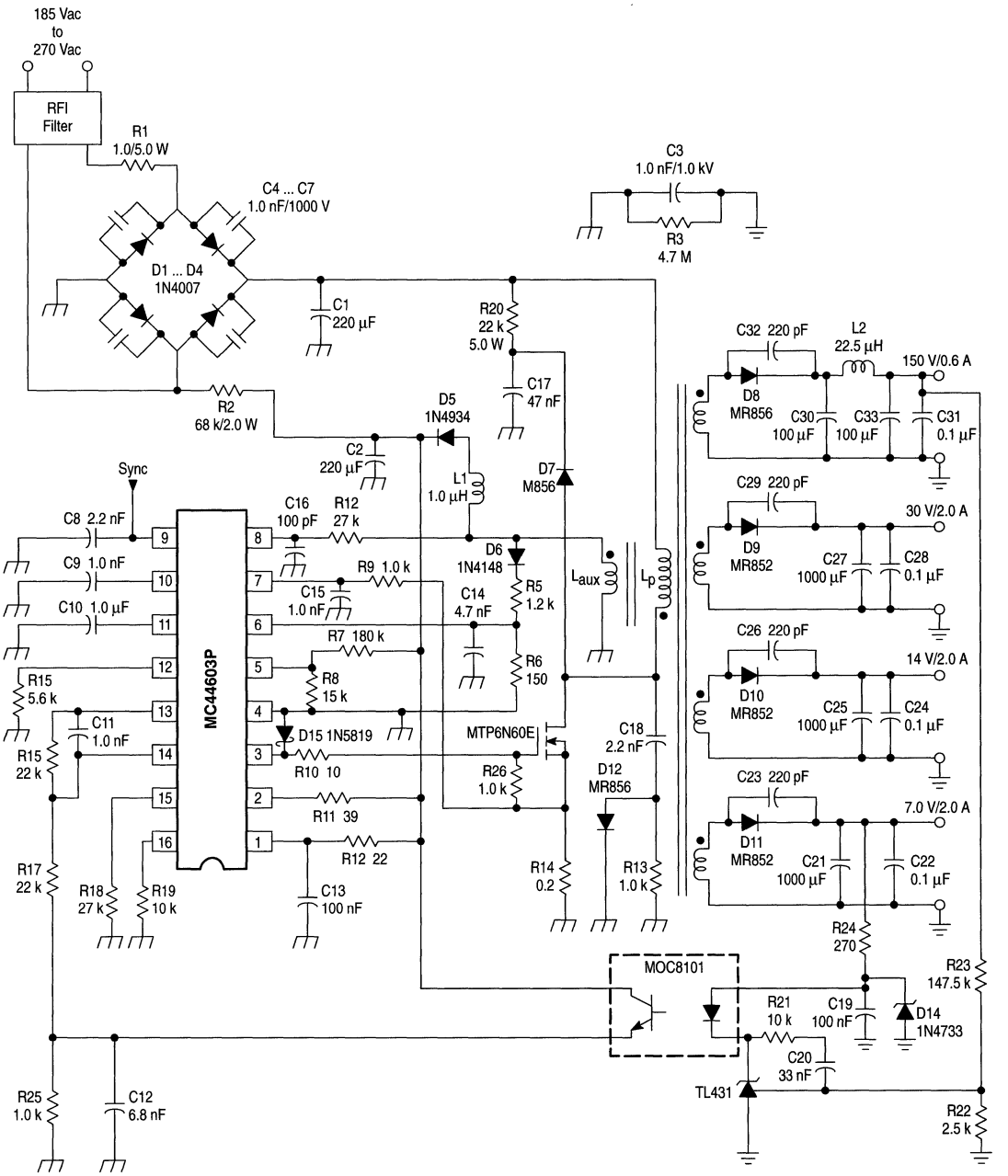
$$I_{ref} = \frac{V_{ref}}{R_{ref}} \text{ where } V_{ref} = 2.5 \text{ V (typically)}$$

Another resistor is connected to the Reference Block: $R_{F\ Stby}$ that is used to fix the standby frequency.

In addition to this, V_{CC} is compared to a second threshold level that is nearly equal to 9.0 V ($V_{disable1}$). UVLO1 is generated to reset the maximum duty cycle and soft–start block disabling the output stage as soon as V_{CC} becomes lower than $V_{disable1}$. In this way, the circuit is reset and made ready for the next startup, before the reference block is disabled (refer to Figure 29). Finally, the upper limit for the minimum normal operating voltage is 9.4 V (maximum value of $V_{disable1}$) and so the minimum hysteresis is 4.2 V. ($(V_{stup–th})_{min}$ = 13.6 V).

The large hysteresis and the low startup current of the MC44603 make it ideally suited for off–line converter applications where efficient bootstrap startup techniques are required.

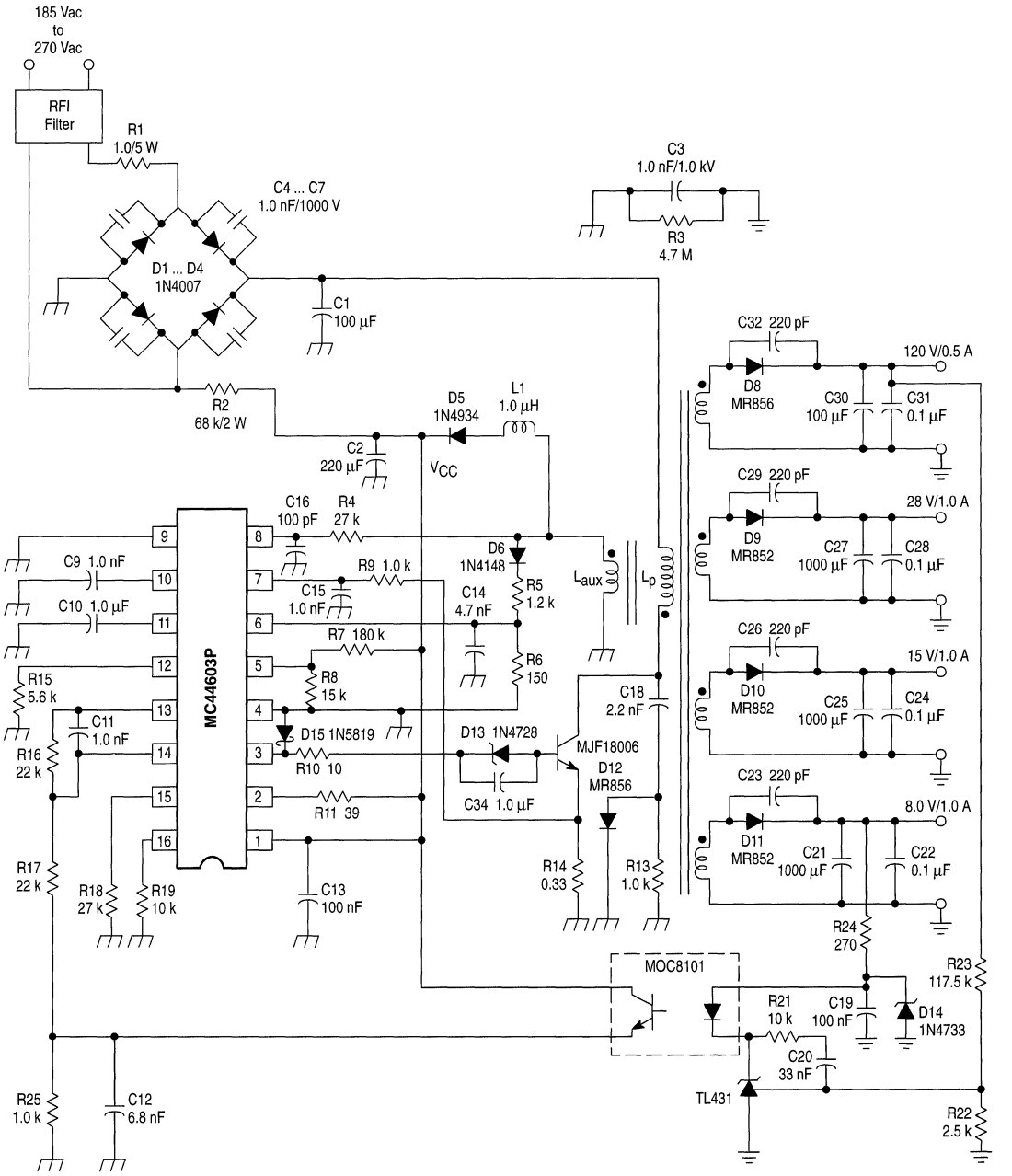
Figure 48. 250 W Input Power Off–Line Flyback Converter with MOSFET Switch



250 W Input Power Fly–Back Converter
185 V – 270 V Mains Range
MC44603P & MTP6N60E

Tests	Conditions	Results
Line Regulation 150 V 30 V 14 V 7.0 V	V_{in} = 185 Vac to 270 Vac F_{mains} = 50 Hz I_{out} = 0.6 A I_{out} = 2.0 A I_{out} = 2.0 A I_{out} = 2.0 A	 10 mV 10 mV 10 mV 20 mV
Load Regulation 150 V	V_{in} = 220 Vac I_{out} = 0.3 A to 0.6 A	 50 mV
Cross Regulation 150 V	V_{in} = 220 Vac I_{out} (150 V) = 0.6 A I_{out} (30 V) = 0 A to 2.0 A I_{out} (14 V) = 2.0 A I_{out} (7.0 V) = 2.0 A	 < 1.0 mV
Efficiency	V_{in} = 220 Vac, P_{in} = 250 W	81%
Standby Mode P input Switching Frequency	 V_{in} = 220 Vac, P_{out} = 0 W	 3.3 W 20 kHz fully stable
Output Short Circuit	$P_{out\ (max)}$ = 270 W	Safe on all outputs
Startup	P_{in} = 250 W	Vac = 160 V

Figure 49. 125 W Input Power Off–Line Flyback Converter with Bipolar Switch



3

125 W Input Power Fly–Back Converter
185 V – 270 V Mains Range
MC44603P & MJF18006

Tests	Conditions	Results
Line Regulation	V_{in} = 185 Vac to 270 Vac F_{mains} = 60 Hz	
120 V	I_{out} = 0.5 A	10 mV
28 V	I_{out} = 1.0 A	10 mV
15 V	I_{out} = 1.0 A	10 mV
8.0 V	I_{out} = 1.0 A	20 mV
Load Regulation 120 V	V_{in} = 220 Vac I_{out} = 0.2 A to 0.5 A	= 0.05 V
Cross Regulation	V_{in} = 220 Vac I_{out} (120 V) = 0.5 A I_{out} (28 V) = 0 A to 1.0 A I_{out} (15 V) = 1.0 A I_{out} (8.0 V) = 1.0 A	
120 V		< 1.0 mV
Efficiency	V_{in} = 220 Vac, P_{in} = 125 W	85%
Standby Mode P input	V_{in} = 220 Vac, P_{out} = 0 W	2.46 W
Switching Frequency		20 kHz fully stable
Output Short Circuit	$P_{out\ (max)}$ = 140 W	Safe on all outputs
Startup	P_{in} = 125 W	Vac = 150 V

MOTOROLA

MC44604

3

Product Preview

High Safety Standby Ladder Mode GreenLine™ PWM Controller

The MC44604 is an enhanced high performance controller that is specifically designed for off–line and dc–to–dc converter applications.

The MC44604 is a modification of the MC44603. The MC44604 offers enhanced safety and reliable power management in its protection features (foldback, overvoltage detection, soft–start, accurate demagnetization detection). Its high current totem pole output is also ideally suited for driving a power MOSFET but can also be used for driving a bipolar transistor in low power converters (< 150 W).

In addition, the MC44604 offers a new efficient way to reduce the standby operating power by means of a patented standby ladder mode operation of the converter significantly reducing the converter consumption in standby mode.

Current or Voltage Mode Controller

- Operation Up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Oscillator with Precise Frequency Control

High Flexibility

- Externally Programmable Reference Current
- Secondary or Primary Sensing
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis

Safety/Protection Features

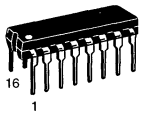
- Overvoltage Protection Facility Against Open Loop
- Protection Against Short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft–Start Feature
- Accurate Maximum Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference

GreenLine™ Controller:

- Low Startup and Operating Current
- Patented Standby Ladder Mode for Low Standby Losses
- Low dV/dT for Low EMI

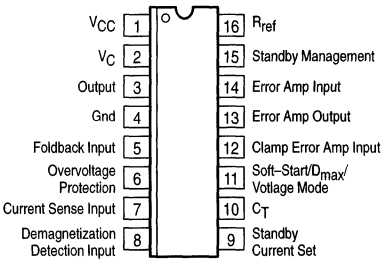
HIGH SAFETY STANDBY LADDER MODE GREENLINE™ PWM CONTROLLER

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44604P	T_A = –25° to +85°C	Plastic DIP

MOTOROLA

Product Preview

High Safety Latched Mode GreenLine™ PWM Controller for (Multi)Synchronized Applications

3

The MC44605 is a high performance current mode controller that is specifically designed for off–line converters. The MC44605 has several distinguishing features that make it particularly suitable for multisynchronized monitor applications.

The MC44605 synchronization arrangement enables operation from 16 kHz up to 130 kHz. This product was optimized to operate with universal ac mains voltage from 80 V to 280 V, and its high current totem pole output makes it ideally suited for driving a power MOSFET.

The MC44605 protections provide well controlled, safe power management. Safety enhancements detect four different fault conditions and provide protection through a disabling latch.

Current or Voltage Mode Controller

- Current Mode Operation Up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Oscillator with Precise Frequency Control
- Externally Programmable Reference Current
- Secondary or Primary Sensing (Availability of Error Amplifier Output)
- Synchronization Facility
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Output dV/dT for Low EMI
- Low Startup and Operating Current

Safety/Protection Features

- Soft–Start Feature
- Demagnetization (Zero Current Detection) Protection
- Overvoltage Protection Facility Against Open Loop
- EHT Overvoltage Protection (E.H.T.OVP): Protection Against Excessive Amplitude Synchronization Pulses
- Winding Short Circuit Detection (W.S.C.D.)
- Limitation of the Maximum Input Power (M.P.L.): Calculation of Input Power for Overload Protection
- Over Heating Detection (O.H.D.): to Prevent the Power Switch from Excessive Heating

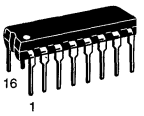
Latched Disabling Mode

- When one of the following faults is detected: EHT overvoltage, Winding Short Circuit (WSCD), excessive input power (M.P.L.), power switch over heating (O.H.D.), a counter is activated
- If the counter is activated for a time that is long enough, the circuit gets definitively disabled. The latch can only be reset by removing and then re–applying power

MC44605

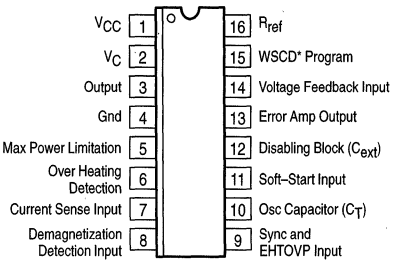
HIGH SAFETY LATCHED MODE GREENLINE™ PWM CONTROLLER FOR (MULTI)SYNCHRONIZED APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



(Top View)

* Winding Short Circuit Detection

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44605P	T_A = –25° to +85°C	Plastic DIP

MOTOROLA

SG3525A
SG3527A

3

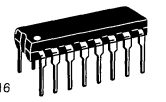
Pulse Width Modulator Control Circuits

PULSE WIDTH MODULATOR CONTROL CIRCUITS

SEMICONDUCTOR TECHNICAL DATA

The SG3525A, SG3527A pulse width modulator control circuits offer improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on–chip +5.1 V reference is trimmed to ±1% and the error amplifier has an input common–mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of deadtime can be programmed by a single resistor connected between the C_T and Discharge pins. These devices also feature built–in soft–start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft–start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft–start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft–start capacitor when V_{CC} is below nominal. The output stages are totem–pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG3525A features NOR logic resulting in a low output for an off–state while the SG3527A utilized OR logic which gives a high output when off.

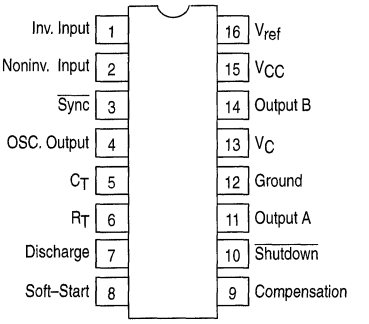
- 8.0 V to 35 V Operation
- 5.1 V ± 1.0% Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Deadtime Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse–by–Pulse Shutdown
- Dual Source/Sink Outputs: ±400 mA Peak



N SUFFIX
PLASTIC PACKAGE
CASE 648

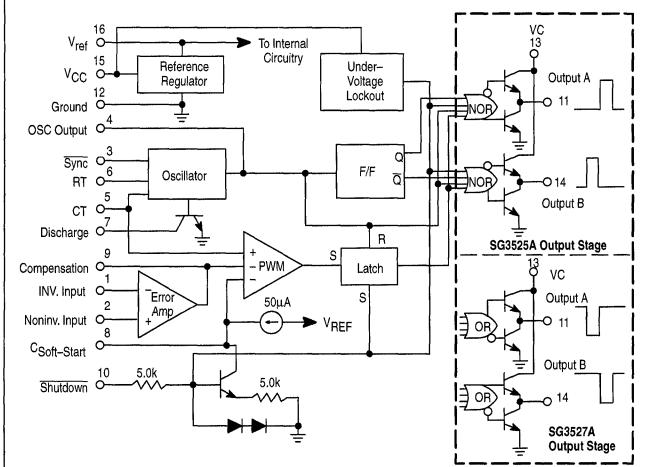
DW SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16L)

PIN CONNECTIONS



(Top View)

Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
SG3525AN	T_A = 0° to +70°C	Plastic DIP
SG3525ADW		SO–16L
SG3527AN		Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs		–0.3 to +5.5	V
Analog Inputs		–0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±500	mA
Reference Output Current	I_{ref}	50	mA
Oscillator Charging Current		5.0	mA
Power Dissipation (Plastic & Ceramic Package) T_A = +25°C (Note 2) T_C = +25°C (Note 3)	P_D	 1000 2000	mW
Thermal Resistance Junction–to–Air	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction–to–Case	$R_{\theta JC}$	60	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Lead Temperature (Soldering, 10 seconds)	T_{Solder}	+300	°C

NOTES: 1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for ambient temperatures above +50°C.
3. Derate at 16 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	8.0	35	Vdc
Collector Supply Voltage	V_C	4.5	35	Vdc
Output Sink/Source Current (Steady State) (Peak)	I_O	 0 0	 ±100 ±400	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.1	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	0.2	µF
Deadtime Resistor Range	R_D	0	500	Ω
Operating Ambient Temperature Range	T_A	0	+70	°C

APPLICATION INFORMATION

Shutdown Options (See Block diagram, front page)

Since both the compensation and soft–start terminals (Pins 9 and 8) have current source pull–ups, either can readily accept a pull–down signal which only has to sink a maximum of 100 µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn–off signal to the outputs; and a 150 µA current sink begins to discharge the external soft–start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft–start capacitor, thus, allowing, for example, a convenient implementation of pulse–by–pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn–on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, T_A = T_{low} to T_{high} [Note 4], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (T_J = +25°C)	V_{ref}	5.00	5.10	5.20	Vdc
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	–	10	20	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	–	20	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	–	20	–	mV
Total Output Variation Includes Line and Load Regulation over Temperature	ΔV_{ref}	4.95	–	5.25	Vdc
Short Circuit Current (V_{ref} = 0 V, T_J = +25°C)	I_{SC}	–	80	100	mA
Output Noise Voltage (10 Hz ≤ f ≤ 10 kHz, T_J = +25°C)	V_n	–	40	200	μV_{rms}
Long Term Stability (T_J = +125°C) (Note 5)	S	–	20	50	mV/khr
OSCILLATOR SECTION (Note 6, unless otherwise noted.)					
Initial Accuracy (T_J = +25°C)		–	±2.0	±6.0	%
Frequency Stability with Voltage (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{D\ V_{CC}}$	–	±1.0	±2.0	%
Frequency Stability with Temperature	$\frac{\Delta f_{osc}}{D\ T}$	–	±0.3	–	%
Minimum Frequency (R_T = 150 kΩ, C_T = 0.2 μF)	f_{min}	–	50	–	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 1.0 nF)	f_{max}	400	–	–	kHz
Current Mirror (I_{RT} = 2.0 mA)		1.7	2.0	2.2	mA
Clock Amplitude		3.0	3.5	–	V
Clock Width (T_J = +25°C)		0.3	0.5	1.0	μs
Sync Threshold		1.2	2.0	2.8	V
Sync Input Current (Sync Voltage = +3.5 V)		–	1.0	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = +5.1 V)					
Input Offset Voltage	V_{IO}	–	2.0	10	mV
Input Bias Current	I_{IB}	–	1.0	10	μA
Input Offset Current	I_{IO}	–	–	1.0	μA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	75	–	dB
Low Level Output Voltage	V_{OL}	–	0.2	0.5	V
High Level Output Voltage	V_{OH}	3.8	5.6	–	V
Common Mode Rejection Ratio (+1.5 V ≤ V_{CM} ≤ +5.2 V)	CMRR	60	75	–	dB
Power Supply Rejection Ratio (+8.0 V ≤ V_{CC} ≤ +35 V)	PSRR	50	60	–	dB
PWM COMPARATOR SECTION					
Minimum Duty Cycle	DC_{min}	–	–	0	%
Maximum Duty Cycle	DC_{max}	45	49	–	%
Input Threshold, Zero Duty Cycle (Note 6)	V_{th}	0.6	0.9	–	V
Input Threshold, Maximum Duty Cycle (Note 6)	V_{th}	–	3.3	3.6	V
Input Bias Current	I_{IB}	–	0.05	1.0	μA

NOTES: 4. T_{low} = 0° for SG3525A, 3527A T_{high} = +70°C for SG3525A, 3527A
5. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Tested at f_{osc} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 μF, R_D = 0Ω).

3

ELECTRICAL CHARACTERISTICS (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
SOFT–START SECTION					
Soft–Start Current ($V_{shutdown}$ = 0 V)		25	50	80	μA
Soft–Start Voltage ($V_{shutdown}$ = 2.0 V)		–	0.4	0.6	V
Shutdown Input Current ($V_{shutdown}$ = 2.5 V)		–	0.4	1.0	mA
OUTPUT DRIVERS (Each Output, V_{CC} = +20 V)					
Output Low Level (I_{sink} = 20 mA) (I_{sink} = 100 mA)	V_{OL}	 – –	 0.2 1.0	 0.4 2.0	V
Output High Level (I_{source} = 20 mA) (I_{source} = 100 mA)	V_{OH}	 18 17	 19 18	 – –	V
Under Voltage Lockout (V8 and V9 = High)	V_{UL}	6.0	7.0	8.0	V
Collector Leakage, V_C = +35 V (Note 7)	$I_{C(leak)}$	–	–	200	μA
Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	100	600	ns
Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	300	ns
Shutdown Delay (V_{DS} = +3.0 V, C_S = 0, T_J = +25°C)	t_{ds}	–	0.2	0.5	μs
Supply Current (V_{CC} = +35 V)	I_{CC}	–	14	20	mA

NOTE: 7. Applies to SG3525A only, due to polarity of output pulses.

Lab Test Fixture

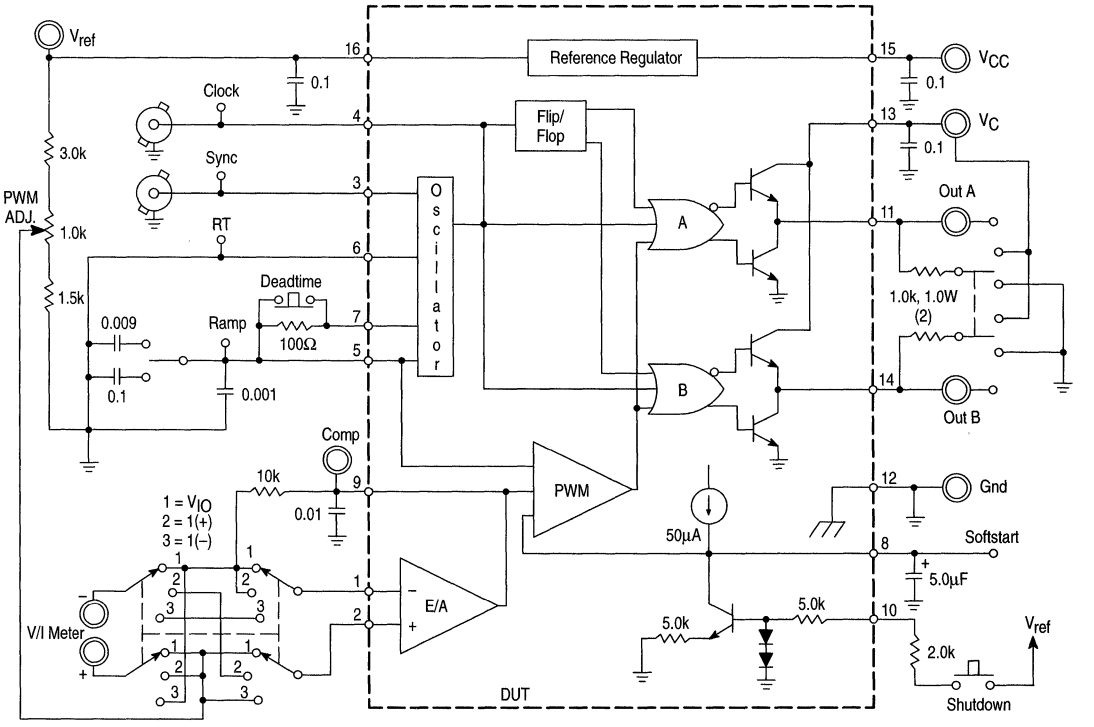


Figure 1. Oscillator Charge Time versus R_T

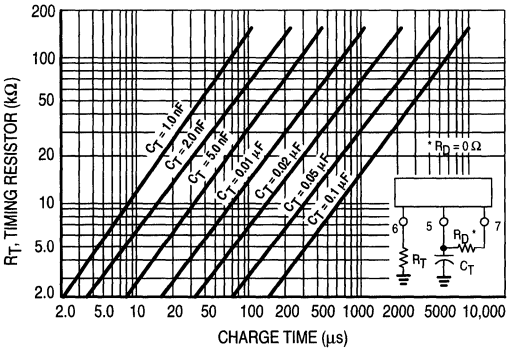


Figure 2. Oscillator Discharge Time versus R_D

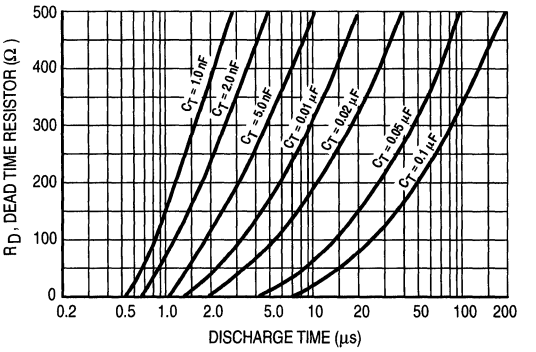


Figure 3. Error Amplifier Open Loop Frequency Response

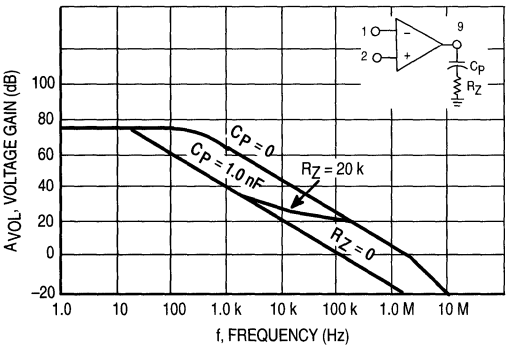


Figure 4. Output Saturation Characteristics (SG3525A)

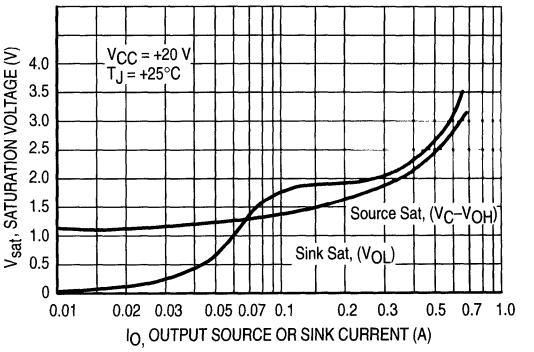


Figure 5. Oscillator Schematic (SG3525A)

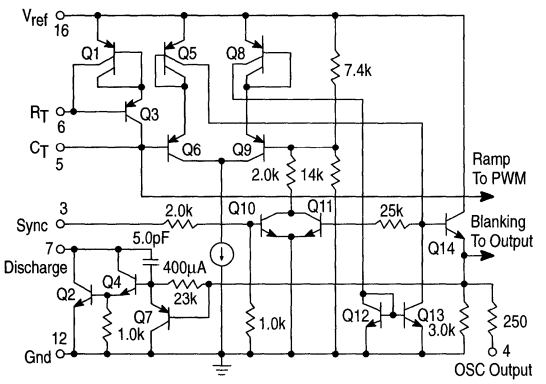
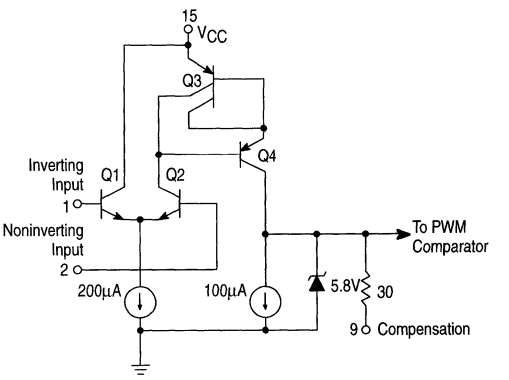


Figure 6. Error Amplifier Schematic (SG3525A)



3

Figure 7. SG3525A Output Circuit
(1/2 Circuit Shown)

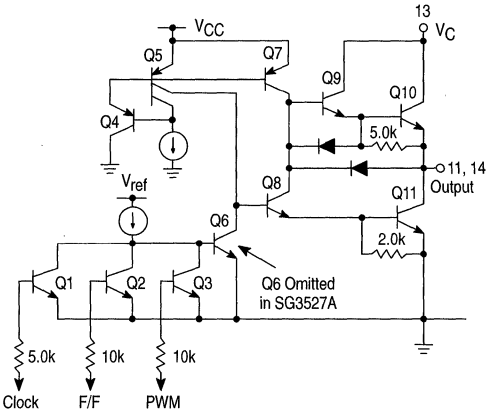
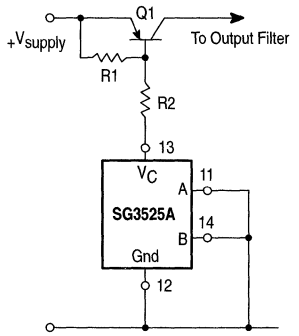
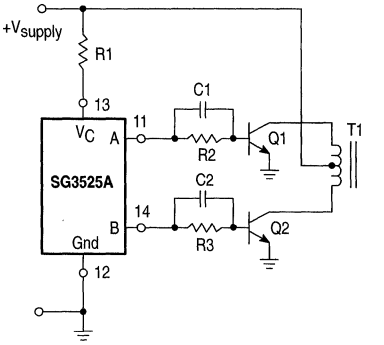


Figure 8. Single–Ended Supply



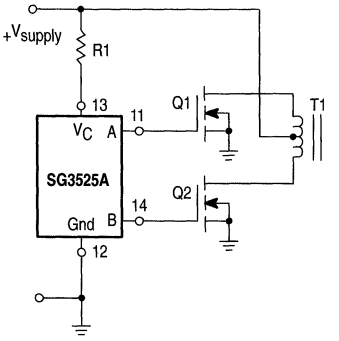
For single–ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem–pole source transistors on alternate oscillator cycles.

Figure 9. Push–Pull Configuration



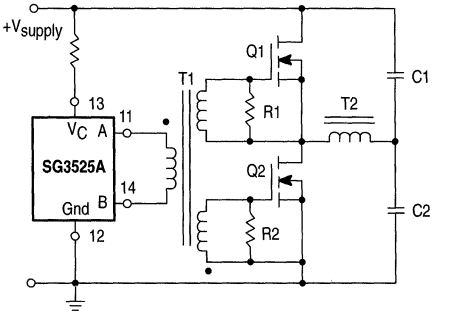
In conventional push–pull bipolar designs, forward base drive is controlled by R1–R3. Rapid turn–off times for the power devices are achieved with speed–up capacitors C1 and C2.

Figure 10. Driving Power FETS



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

Figure 11. Driving Transformers in a Half–Bridge Configuration



Low power transformers can be driven directly by the SG3525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

MOTOROLA

SG3526

Pulse Width Modulation Control Circuit

3

PULSE WIDTH MODULATION CONTROL CIRCUIT

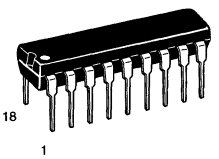
SEMICONDUCTOR TECHNICAL DATA

The SG3526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

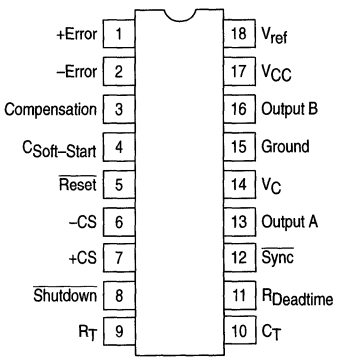
Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports are TTL and B–series CMOS compatible. Active low logic design allows easy wired–OR connections for maximum flexibility. The versatility of this device enables implementation in single–ended or push–pull switching regulators that are transformerless or transformer coupled. The SG3526 is specified over a junction temperature range of 0° to +125°C.

- 8.0 V to 35 V Operation
- 5.0 V ±1% Trimmed Reference
- 1.0 Hz to 400 kHz Oscillator Range
- Dual Source/Sink Current Outputs: ±100 mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage Lockout
- Single Pulse Metering
- Programmable Soft–Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization



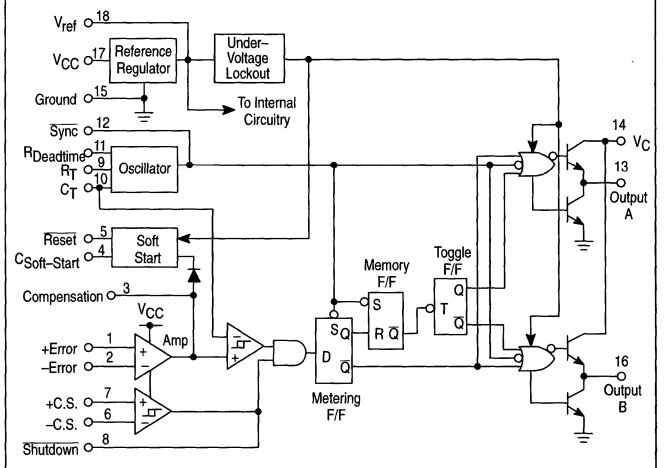
N SUFFIX
PLASTIC PACKAGE
CASE 707

PIN CONNECTIONS



(Top View)

Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
SG3526N	T_J = 0° to +125°C	Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs		–0.3 to +5.5	V
Analog Inputs		–0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±200	mA
Reference Load Current (V_{CC} = 40 V, Note 2)	I_{ref}	50	mA
Logic Sink Current		15	mA
Power Dissipation T_A = +25°C (Note 3) T_C = +25°C (Note 4)	P_D	 1000 3000	mW
Thermal Resistance Junction–to–Air	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction–to–Case	$R_{\theta JC}$	42	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	T_{Solder}	±300	°C

NOTES: 1. Values beyond which damage may occur.
2. Maximum junction temperature must be observed.
3. Derate at 10 mW/°C for ambient temperatures above +50°C.
4. Derate at 24 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	8.0	35	Vdc
Collector Supply Voltage	V_C	4.5	35	Vdc
Output Sink/Source Current (Each Output)	I_O	0	±100	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.001	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	20	µF
Available Deadtime Range (40 kHz)	–	3.0	50	%
Operating Junction Temperature Range	T_J	0	+125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, T_J = T_{low} to T_{high} [Note 5], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION (Note 6)					
Reference Output Voltage (T_J = +25°C)	V_{ref}	4.90	5.00	5.10	V
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	–	10	30	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	–	10	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	–	10	–	mV
Total Reference Output Voltage Variation (+8.0 V ≤ V_{CC} ≤ +35 V, 0 mA ≤ I_L ≤ 20 mA)	ΔV_{ref}	4.85	5.00	5.15	V
Short Circuit Current (V_{ref} = 0 V) (Note 2)	I_{SC}	25	80	125	mA
UNDERVOLTAGE LOCKOUT					
$\overline{Reset}$ Output Voltage (V_{ref} = +3.8 V)		–	0.2	0.4	V
$\overline{Reset}$ Output Voltage (V_{ref} = +4.8 V)		2.4	4.8	–	V
OSCILLATOR SECTION (Note 7)					
Initial Accuracy (T_J = +25°C)		–	±3.0	±8.0	%
Frequency Stability over Power Supply Range (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	–	0.5	1.0	%
Frequency Stability over Temperature (ΔT_J = T_{low} to T_{high})	$\frac{\Delta f_{osc}}{\Delta T_J}$	–	2.0	–	%
Minimum Frequency (R_T = 150 kΩ, C_T = 20 μF)	f_{min}	–	0.5	–	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 0.001 μF)	f_{max}	400	–	–	kHz
Sawtooth Peak Voltage (V_{CC} = +35 V)	$V_{osc}(P)$	–	3.0	3.5	V
Sawtooth Valley Voltage (V_{CC} = +8.0 V)	$V_{osc}(V)$	0.45	0.8	–	V
ERROR AMPLIFIER SECTION (Note 8)					
Input Offset Voltage (R_S ≤ 2.0 kΩ)	V_{IO}	–	2.0	10	mV
Input Bias Current	I_{IB}	–	–350	–2000	nA
Input Offset Current	I_{IO}	–	35	200	nA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	72	–	dB
High Output Voltage ($V_{Pin\ 1}$–$V_{Pin\ 2}$ ≥ +150 mV, I_{source} = 100 μA)	V_{OH}	3.6	4.2	–	V
Low Output Voltage ($V_{Pin\ 2}$–$V_{Pin\ 1}$ ≥ +150 mV, I_{sink} = 100 μA)	V_{OL}	–	0.2	0.4	V
Common Mode Rejection Ratio (R_S ≤ 2.0 kΩ)	CMRR	70	94	–	dB
Power Supply Rejection Ratio (+12 V ≤ V_{CC} ≤ +18 V)	PSRR	66	80	–	dB

NOTES: 2. Maximum junction temperature must be observed.
5. T_{low} = 0°C T_{high} = +125°C
6. I_L = 0 mA unless otherwise noted.
7. f_{osc} = 40 kHz (R_T = 4.12 kΩ ± 1%, C_T = 0.01 μF ± 1%, R_D = 0 Ω)
8. 0 V ≤ V_{CM} ≤ +5.2 V.

ELECTRICAL CHARACTERISTICS (continued)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Note 7)					
Minimum Duty Cycle ($V_{Compensation}$ = +0.4 V)	DC_{min}	–	–	0	%
Maximum Duty Cycle ($V_{Compensation}$ = +3.6 V)	DC_{max}	45	49	–	%
DIGITAL PORTS (SYNC, SHUTDOWN, RESET)					
Output Voltage					V
(High Logic Level) (I_{source} = 40 μA)	V_{OH}	2.4	4.0	–	
(Low Logic Level) (I_{sink} = 3.6 mA)	V_{OL}	–	0.2	0.4	
Input Current — High Logic Level					μA
(High Logic Level) (V_{IH} = +2.4 V)	I_{IH}	–	–125	–200	
(Low Logic Level) (V_{IL} = +0.4 V)	I_{IL}	–	–225	–360	
CURRENT LIMIT COMPARATOR SECTION (Note 9)					
Sense Voltage ($R_S \leq 50\ \Omega$)	V_{sense}	80	100	120	mA
Input Bias Current	I_{IB}	—	–3.0	–10	μA
SOFT–START SECTION					
Error Clamp Voltage ($\overline{Reset}$ = +0.4 V)		–	0.1	0.4	V
$C_{Soft–Start}$ Charging Current ($\overline{Reset}$ = +2.4 V)	I_{CS}	50	100	150	μA
OUTPUT DRIVERS (Each Output, V_C = +15 Vdc, unless otherwise noted.)					
Output High Level	V_{OH}				V
I_{source} = 20 mA		12.5	13.5	–	
I_{source} = 100 mA		12	13	–	
Output Low Level	V_{OL}				V
I_{sink} = 20 mA		–	0.2	0.3	
I_{sink} = 100 mA		–	1.2	2.0	
Collector Leakage, V_C = +40 V	$I_{C(leak)}$	–	50	150	μA
Rise Time (C_L = 1000 pF)	t_r	–	0.3	0.6	μs
Fall Time (C_L = 1000 pF)	t_f	–	0.1	0.2	μs
Supply Current ($\overline{Shutdown}$ = +0.4 V, V_{CC} = +35 V, R_T = 4.12 kΩ)	I_{CC}	–	18	30	mA

NOTES: 7. f_{osc} = 40 kHz (R_T = 4.12 kΩ ± 1%, C_T = 0.01 μF ± 1%, R_D = 0 Ω)
8. 0 V ≤ V_{CM} ≤ +5.2 V
9. 0 V ≤ V_{CM} ≤ +12 V

Figure 1. Reference Stability over Temperature

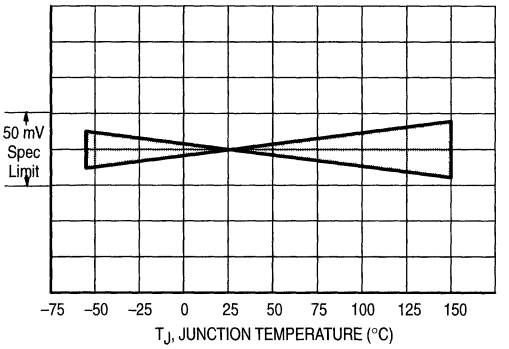


Figure 2. Reference Voltage as a Function Supply Voltage

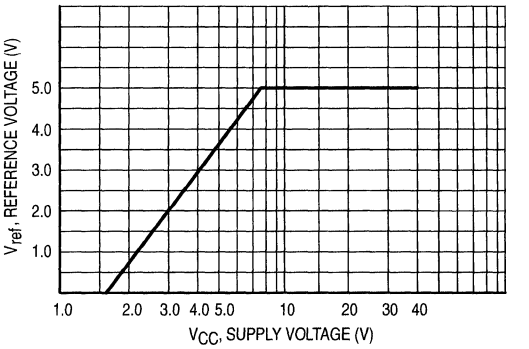


Figure 3. Error Amplifier Open Loop Frequency Response

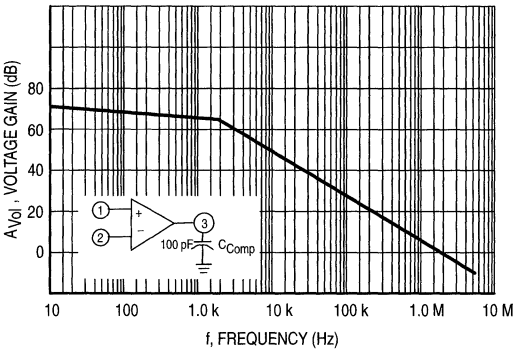


Figure 4. Current Limit Comparator Threshold

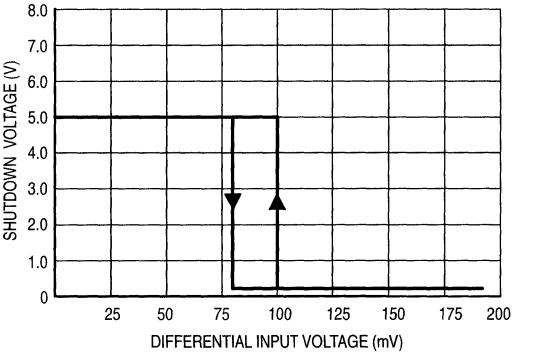


Figure 5. Undervoltage Lockout Characteristic

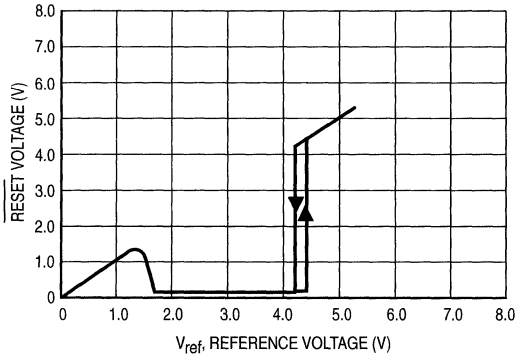
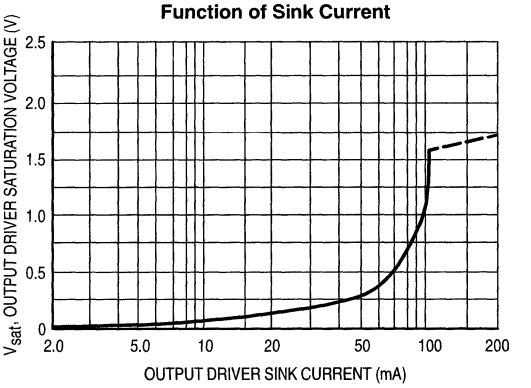


Figure 6. Output Driver Saturation Voltage as a Function of Sink Current



3

Figure 7. V_C Saturation Voltage as a Function of Sink Current

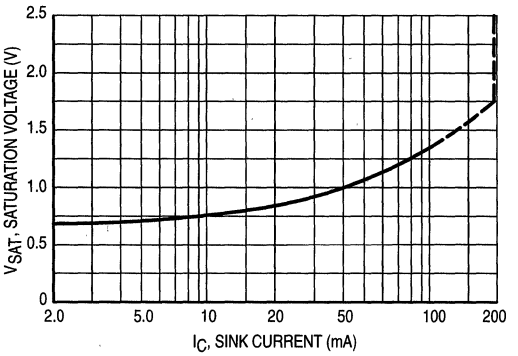


Figure 8. Oscillator Period

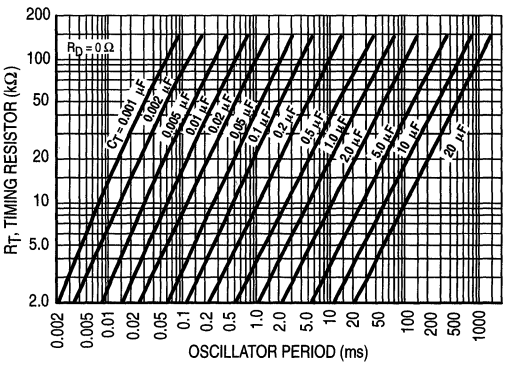


Figure 9. Error Amplifier

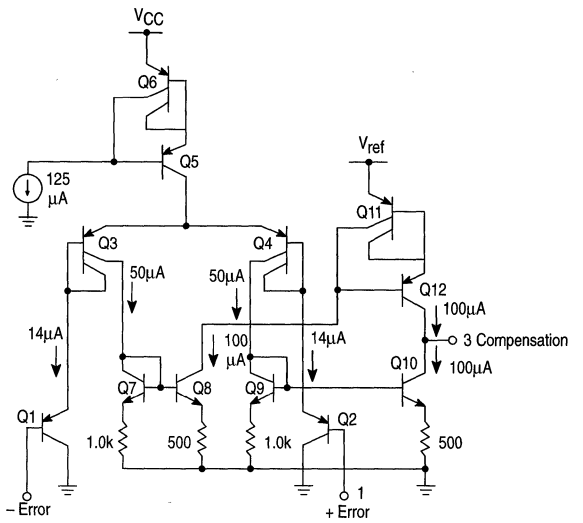


Figure 10. Undervoltage Lockout

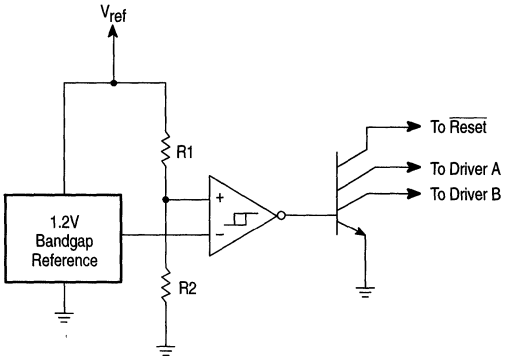
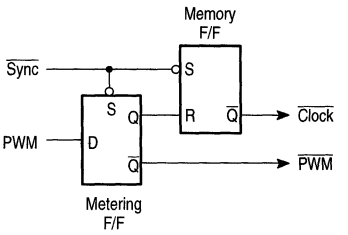


Figure 11. Pulse Processing Logic

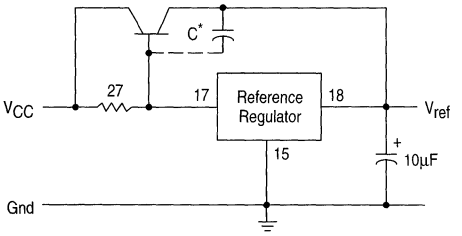


The metering Flip–Flop is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory Flip–Flop prevents double pulsing in a push–pull configuration by remembering which output produced the last pulse.

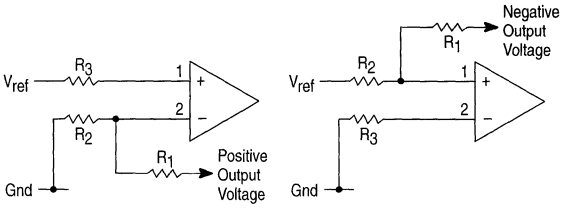
APPLICATIONS INFORMATION

Figure 12. Extending Reference Output Current Capability



* May be required with some types of transistors

Figure 13. Error Amplifier Connections



$$V_{out} = V_{ref}\left(\frac{R_1 + R_2}{R2}\right) \qquad V_{out} = V_{ref}\left(\frac{R_1}{R_2}\right)$$

$$R_3 = \left(\frac{R_1 R_2}{R_1 + R_2}\right)$$

Figure 14. Oscillator Connections

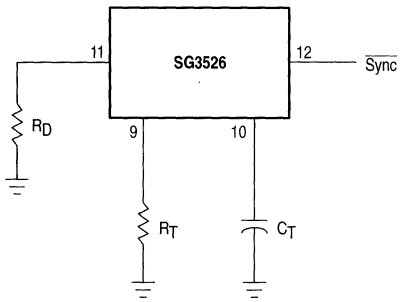
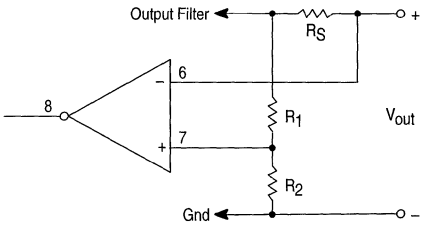


Figure 15. Foldback Current Limiting



$$I_{(max)} = \frac{\left(0.1\ V + \frac{V_{out}\,R_1}{R1 + R2}\right)}{R_S} \qquad I_{SC} = \left(\frac{0.1\ V}{R_S}\right)$$

Figure 16. Soft–Start Circuity

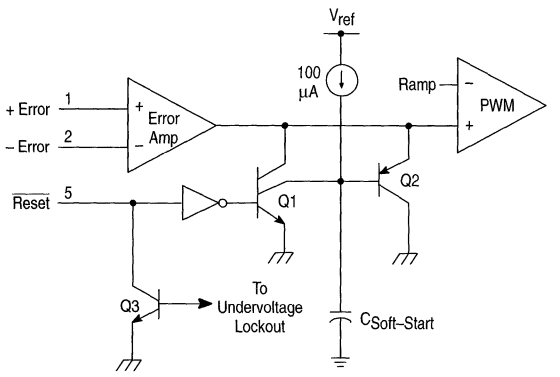
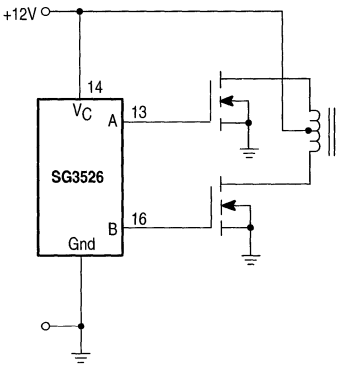


Figure 17. Driving VMOS Power FETs



The totem pole output drivers of the SG3526 are ideally suited for driving the input capacitance of power FETs at high speeds.

Figure 18. Half–Bridge Configuration

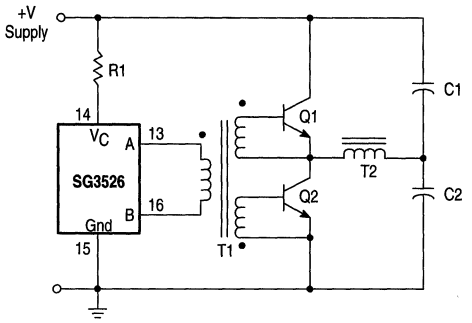
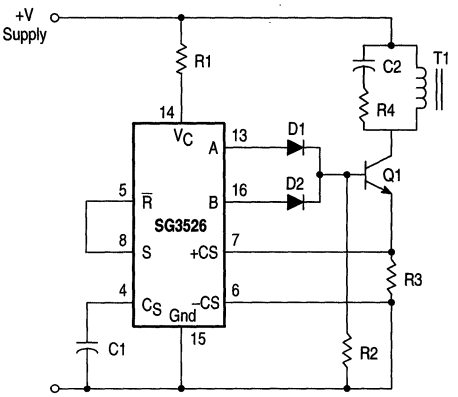


Figure 19. Flyback Converter with Current Limiting



In the above circuit, current limiting is accomplished by using the current limit comparator output to reset the soft–start capacitor.

Figure 20. Single–Ended Configuration

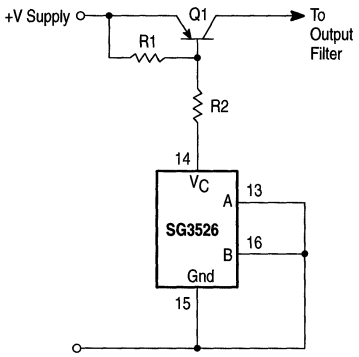
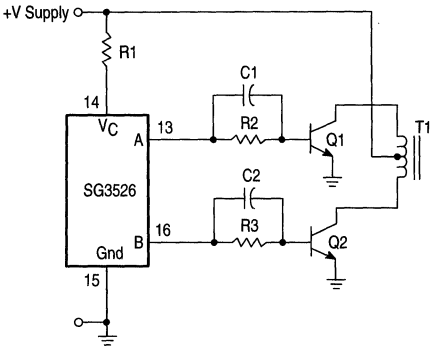


Figure 21. Push–Pull Configuration



TCA5600
TCF5600

Universal Microprocessor Power Supply/Controllers

UNIVERSAL MICROPROCESSOR POWER SUPPLY/CONTROLLERS

SEMICONDUCTOR TECHNICAL DATA

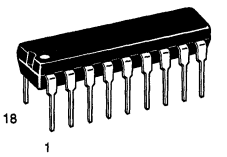
The TCA5600, TCF5600 are versatile power supply control circuits for microprocessor based systems and are mainly intended for automotive applications and battery powered instruments. To cover a wide range of applications, the devices offer high circuit flexibility with a minimum of external components.

Functions included in this IC are a temperature compensated voltage reference, on–chip dc/dc converter, programmable and remote controlled voltage regulator, fixed 5.0 V supply voltage regulator with external PNP power device, undervoltage detection circuit, power–on RESET delay and watchdog feature for safe and hazard free microprocessor operations.

- 6.0 V to 30 V Operation Range
- 2.5 V Reference Voltage Accessible for Other Tasks
- Fixed 5.0 V ± 4% Microprocessor Supply Regulator Including Current Limitation, Overvoltage Protection and Undervoltage Monitor.
- Programmable 6.0 V to 30 V Voltage Regulator Exhibiting High Peak Current (150mA), Current Limiting and Thermal Protection.
- Two Remote Inputs to Select the Regulator's Operation Mode:
  OFF = 5.0 V, 5.0 V Standby
  Programmable Output Voltage
- Self–Contained dc/dc Converter Fully Controlled by the Programmable Regulator to Guarantee Safe Operation Under All Working Conditions
- Programmable Power–On RESET Delay
- Watchdog Select Input
- Negative Edge Triggered Watchdog Input
- Low Current Consumption in the V_{CC1} Standby Mode
- All Digital Control Ports are TTL and MOS–Compatible

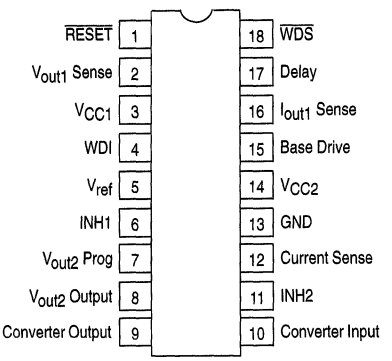
Applications Include:

- Microprocessor Systems with E^2PROMs
- High Voltage Crystal and Plasma Displays
- Decentralized Power Supplies in Computer Telecom Systems



PLASTIC PACKAGE
CASE 707

PIN CONNECTIONS



(Top View)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC1} V_{CC2}	5.0 5.5	30 30	V
Collector Current	I_C	—	800	mA
Output Voltage	V_{out2}	6.0	30	V
Reference Source Current	I_{ref}	0	2.0	mA

ORDERING INFORMATION

Device	Operating Temperature Range	Package
TCA5600	T_J = 0° to +125°C	Plastic DIP
TCF5600	T_J = – 40° to +150°C	Plastic DIP

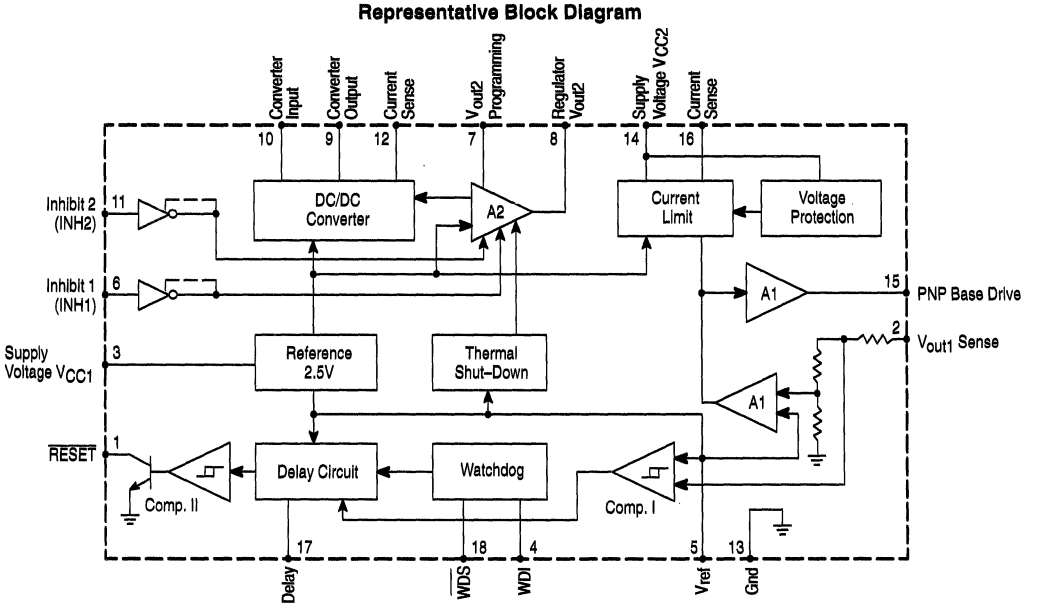
3

MAXIMUM RATINGS (T_A = +25°C [Note 1], unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 3,14)	V_{CC1}, V_{CC2}	35	Vdc
Base Drive Current (Pin 15)	I_B	20	mA
Collector Current (Pin 10)	I_C	1.0	A
Forward Rectifier Current (Pin 10 to Pin 9)	I_F	1.0	A
Logic Inputs INH1, INH2, $\overline{WDS}$ (Pin 6, 11, 18)	V_{INP}	−0.3 V to V_{CC1}	Vdc
Logic Input Current WDI (Pin 4)	I_{WDI}	±0.5	mA
Output Sink Current $\overline{RESET}$ (Pin 1)	$I_{\overline{RES}}$	10	mA
Analog Inputs (Pin 2) (Pin 7)		−0.3 to 10 −0.3 to 5.0	V
Reference Source Current (Pin 5)	I_{ref}	5.0	mA
Power Dissipation (Note 2) T_A = +75°C TCA5600 T_A = +85°C TCF5600	P_D	 500 650	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Ambient Temperature Range TCA5600 TCF5600	T_A	 0 to +75 −40 to +85	°C
Operating Junction Temperature Range TCA5600 TCF5600	T_J	 +125 +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES: 1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for junction temperature above +75°C (TCA5600).
Derate at 10 mW/°C for junction temperature above +85°C (TCF5600).

Representative Block Diagram



ELECTRICAL CHARACTERISTICS (V_{CC1} = V_{CC2} = 12 V; T_J = 25°C; I_{ref} = 0; I_{out1} = 0 [Note 3]; R_{SC} = 0.5 Ω; INH = High INH2 = High; $\overline{WDS}$ = High; I_{out2} = 0 [Note 4]; unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION						
Nominal Reference Voltage	1	$V_{ref\ nom}$	2.42	2.5	2.58	V
Reference Voltage I_{ref} = 0.5 mA, $T_{low} \le T_J \le T_{high}$ (Note 5), 6.0 V ≤ V_{CC1} ≤ 18 V		V_{ref}	2.4	—	2.6	V
Line Regulation (6.0 V ≤ V_{CC2} ≤ 18 V)		Reg_{line}	—	2.0	15	mV
Average Temperature Coefficient $T_{low} \le T_J \le T_{high}$ (Note 5)	2	$\frac{\Delta V_{ref}}{\Delta T_J}$	—	—	±0.5	mV/°C
Ripple Rejection Ratio f = 1.0 kHz, V_{sin} = 1.0 V_{pp}	3	RR	60	70	—	dB
Output Impedance 0 ≤ I_{ref} ≤ 2.0 mA		Z_O	—	1.0	—	Ω
Standby Current Consumption V_{CC2} = Open	4	I_{CC1}	—	3.0	—	mA
5.0 V MICROPROCESSOR VOLTAGE REGULATOR SECTION						
Nominal Output Voltage		$V_{out1(nom)}$	4.8	5.0	5.2	V
Output Voltage 5.0 mA ≤ I_{out1} ≤ 300 mA, $T_{low} \le T_J \le T_{high}$ (Note 5) 6.0 V ≤ V_{CC2} ≤ 18 V	5 6	V_{out1}	4.75	—	5.25	V
Line Regulation (6.0 V ≤ V_{CC2} ≤ 18 V)		Reg_{line}	—	10	50	mV
Load Regulation (5.0 mA ≤ I_{out1} ≤ 300 mA)		Reg_{load}	—	20	100	mV
Base Current Drive (V_{CC2} = 6.0 V, V_{15} = 4.0 V)		I_B	10	15	—	mA
Ripple Rejection Ratio f = 1.0 kHz, V_{sin} = 1.0 V_{pp}	3	RR	50	65	—	dB
Undervoltage Detection Level (R_{SC} = 5.0 Ω)	7	V_{low}	4.5	0.93 × V_{out1}	—	V
Current Limitation Threshold (R_{SC} = 5.0 Ω)		V_{RSC}	210	250	290	mV
Average Temperature Coefficient $T_{low} \le T_J \le T_{high}$ (Note 5)		$\frac{\Delta V_{out1}}{\Delta T_J}$	—	—	±1.0	mV/°C
DC/DC CONVERTER SECTION						
Collector Current Detection Level High RC = 10 k Low	9	$V_{12(H)}$ $V_{12(L)}$	350 —	400 50	450 —	mV
Collector Saturation Voltage I_C = 600 mA (Note 6)	10	$V_{CE(sat)}$	—	—	1.6	V
Rectifier Forward Voltage Drop I_F = 600 mA (Note 6)	11	V_F	—	—	1.4	V

NOTES: 3. The external PNP power transistor satisfies the following minimum specifications:
h_{FE} ≥ 60 at I_C = 500 mA and V_{CE} = 5.0 V;
$V_{CE(sat)}$ ≤ 300 mV at I_B = 10 mA and I_C = 300 mA
4. Regulator V_{out2} programmed for nominal 24 V output by means of R4, R5 (see Figure 1).
5. T_{low} = 0°C for TCA5600 T_{low} = −40°C for TCF5600
T_{high} = +125°C for TCA5600 T_{high} = +150°C for TCF5600
6. Pulse tested $t_p \le 300\ \mu s$.

ELECTRICAL CHARACTERISTICS ($V_{CC1} = V_{CC2} = 12$ V; $T_J = 25°C$; $I_{ref} = 0$; $I_{out1} = 0$ [Note 3]; $R_{SC} = 0.5\ \Omega$; INH = High INH2 = High; $\overline{WDS}$ = High; $I_{out2} = 0$ [Note 4]; unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
PROGRAMMABLE VOLTAGE REGULATOR SECTION (Note 6)					
Nominal Output Voltage	$V_{out2(nom)}$	23	24	25	V
Output Voltage (Figure 8) 1.0 mA ≤ I_{out2} ≤ 100 mA, $T_{low} \le T_J \le T_{high}$ (Notes 5, 7)	V_{out2}	22.8	—	25.2	V
Load Regulation 1.0 mA ≤ I_{out2} ≤ 100 mA (Note 7)	Reg_{load}	—	40	200	mV
DC Output Current	I_{out2}	100	—	—	mA
Peak Output Current (Internally Limited)	$I_{out2\ p}$	150	200	—	mA
Ripple Rejection Ratio f = 20 kHz, V = 0.4 V_{pp}	RR	45	55	—	dB
Output Voltage (Fixed 5.0 V) 1.0 mA ≤ I_{out2} ≤ 20 mA, $T_{low} \le T_J \le T_{high}$ INH1 = HIGH (Note 5)	$V_{out2(5.0\ V)}$	4.75	—	5.25	V
Off State Output Impedance (INH2 = Low)	R_{out1}	—	10	—	kΩ
Average Temperature Coefficient $T_{low} \le T_J \le T_{high}$ (Note 5)	$\frac{\Delta V_{out2}}{\Delta T_J V_{out2}}$	—	—	±0.25	mV/°C V
WATCHDOG AND $\overline{RESET}$ CIRCUIT SECTION					
Threshold Voltage High (Static) Low	$V_{C5(H)}$ $V_{C5(L)}$	— —	2.5 1.0	— —	V
Current Source $T_{low} \le T_J \le T_{high}$ (Note 5) Power–Up $\overline{RESET}$ Watchdog Time Out Watchdog $\overline{RESET}$	I_{C5}	 –1.8 — —	 –2.5 5×I_{C5} –50×I_{C5}	 –3.2 — —	µA
Watchdog Input Voltage Swing	V_{WDI}	—	—	±5.5	V
Watchdog Input Impedance	r_I	12	15	—	kΩ
Watchdog Reset Pulse Width (C8 = 1.0 nF) (Note 9)	t_p	—	—	10	µs
DIGITAL PORTS: $\overline{WDS}$, INH 1, INH 2, $\overline{RESET}$ (Note 8)					
Input Voltage Range	V_{INP}	—	—	–0.3 to V_{CC1}	V
Input High Current 2.0 V ≤ V_{IH} ≤ 5.5 V 5.5 V ≤ $V_{IH} \le V_{CC1}$	I_{IH}	 — —	 — —	 100 150	µA
Input Low Current –0.3 V ≤ V_{IL} ≤ 0.8 V for INH1, INH2, –0.3 V ≤ V_{IL} ≤ 0.4 V for $\overline{WDS}$	I_{IL}	—	—	–100	µA
Leakage Current Immunity (INH2, High "Z" State) (Figure 12)	I_Z	±20	—	—	µA
Output Low Voltage $\overline{RESET}$ (I_{OL} = 6.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage $\overline{RESET}$ (V_{OH} = 5.5 V)	V_{OH}	—	—	20	µA

NOTES: 3. The external PNP power transistor satisfies the following minimum specifications:
$h_{FE} \ge 60$ at I_C = 500 mA and V_{CE} = 5.0 V;
$V_{CE(sat)} \le 300$ mV at I_B = 10 mA and I_C = 300 mA
4. Regulator V_{out2} programmed for nominal 24 V output by means of R4, R5 (see Figure 1).
5. T_{low} = 0°C for TCA5600 T_{low} = –40°C for TCF5600
T_{high} = +125°C for TCA5600 T_{high} = +150°C for TCF5600
6. V_9 = 28 V, INH1 = LOW for this Electrical Characteristic section unless otherwise noted.
7. Pulse tested $t_p \le 300$ µs.
8. Temperature range $T_{low} \le T_J \le T_{high}$ applies to this Electrical Characteristics section.
9. For test purposes, a negative pulse is applied to Pin 4 (–2.5 V ≥ V_4 ≥ –5.5 V).

Figure 1. Reference Voltage versus Supply Voltage

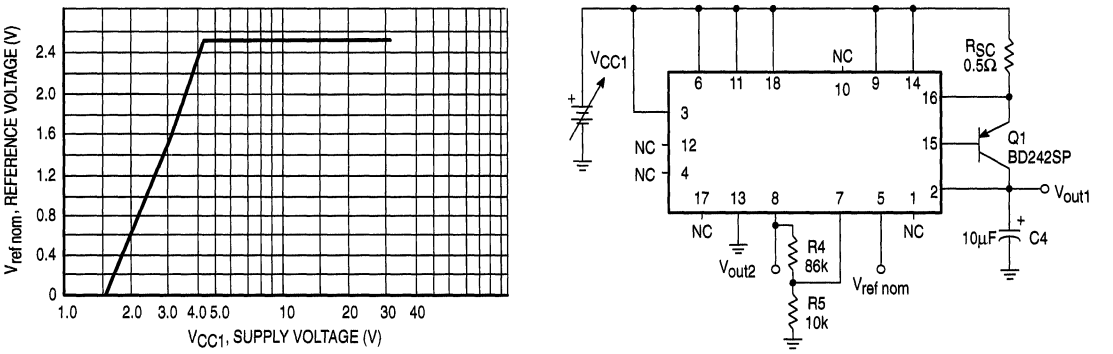


Figure 2. Reference Stability versus Temperature

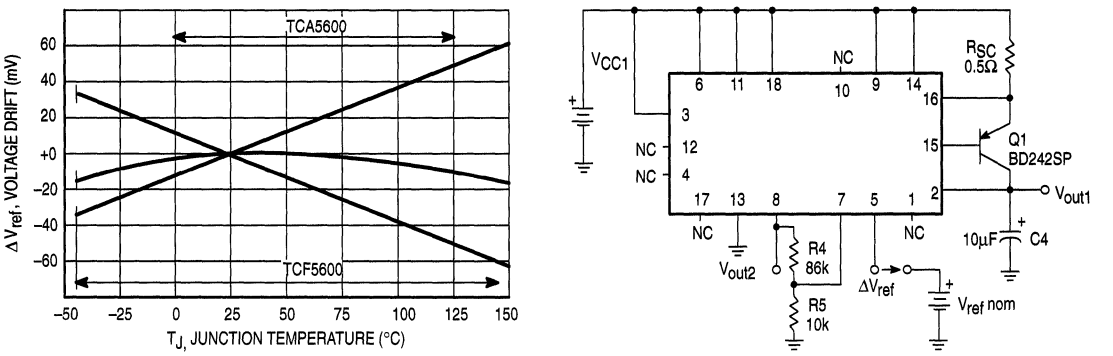
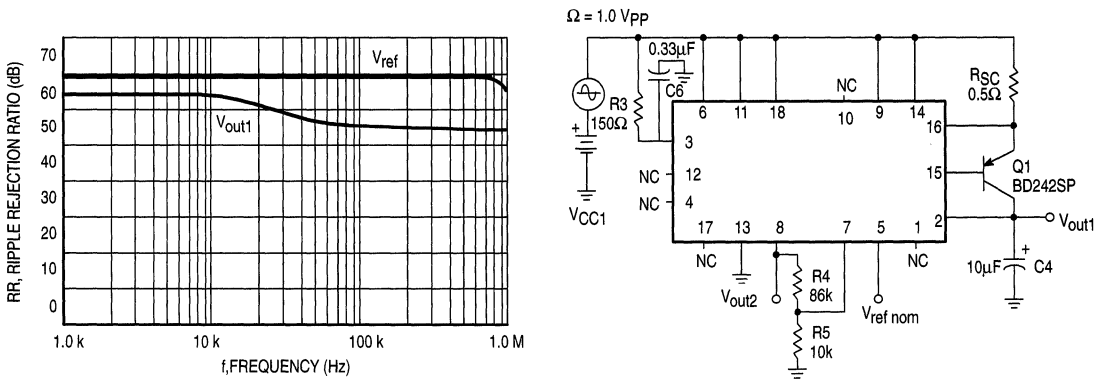


Figure 3. Ripple Rejection versus Frequency



3

Figure 4. Standby Current versus Supply Voltage

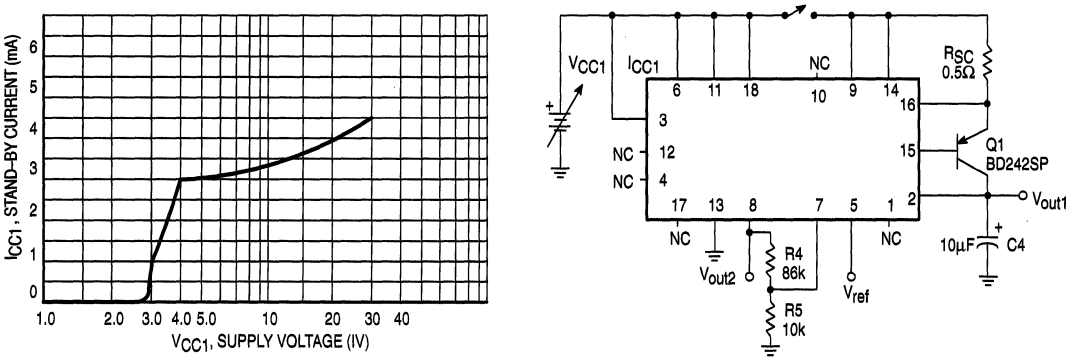


Figure 5. Power–Up Behavior of the 5.0 V Regulator

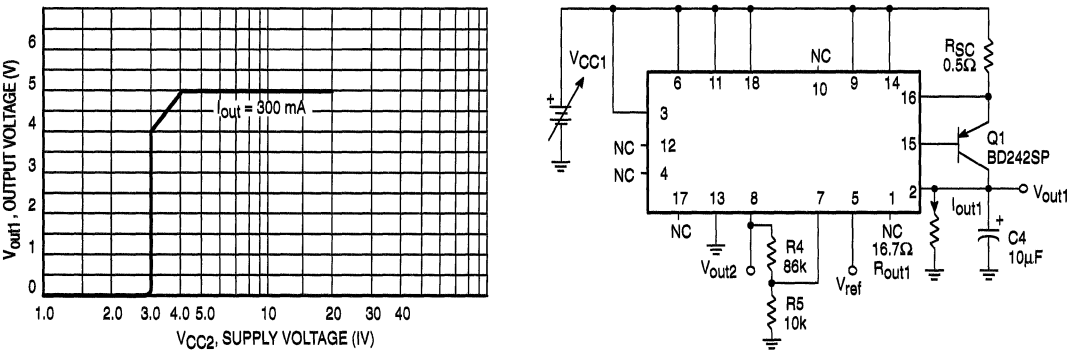


Figure 6. Foldback Characteristics of the 5.0 V Regulator

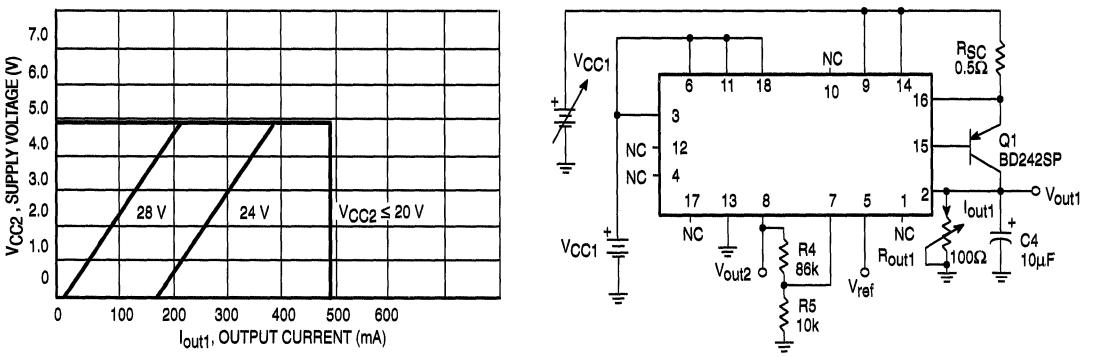


Figure 7. Undervoltage Lockout Characteristics

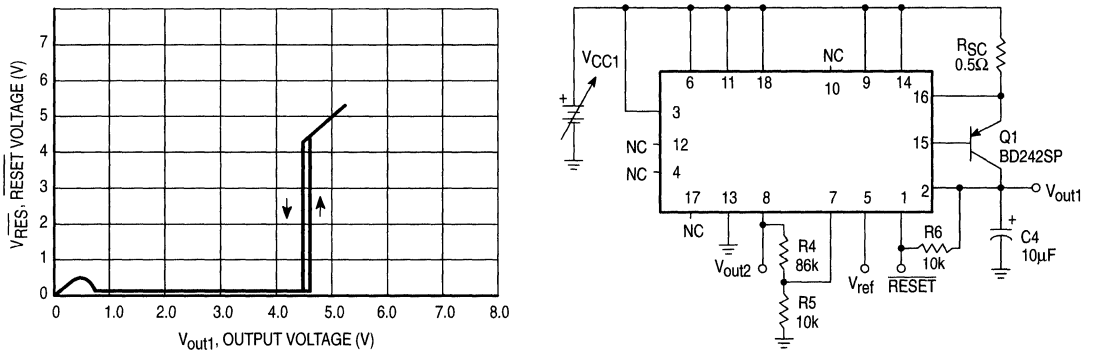


Figure 8. Output Current Capability of the Programming Regulator

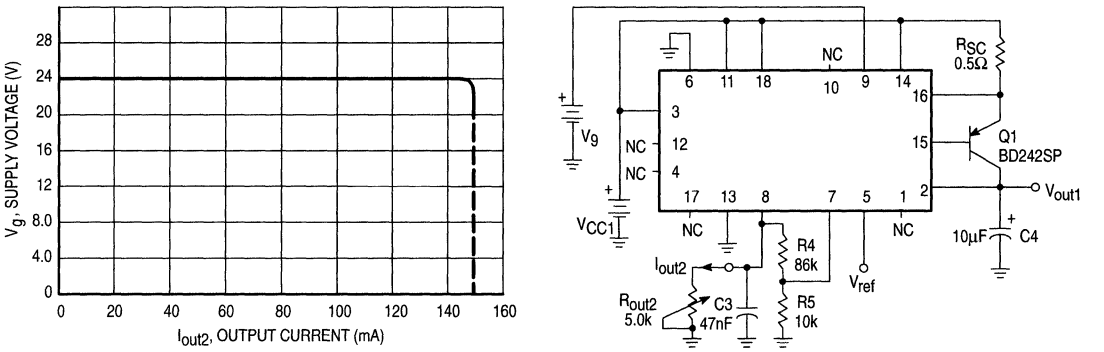
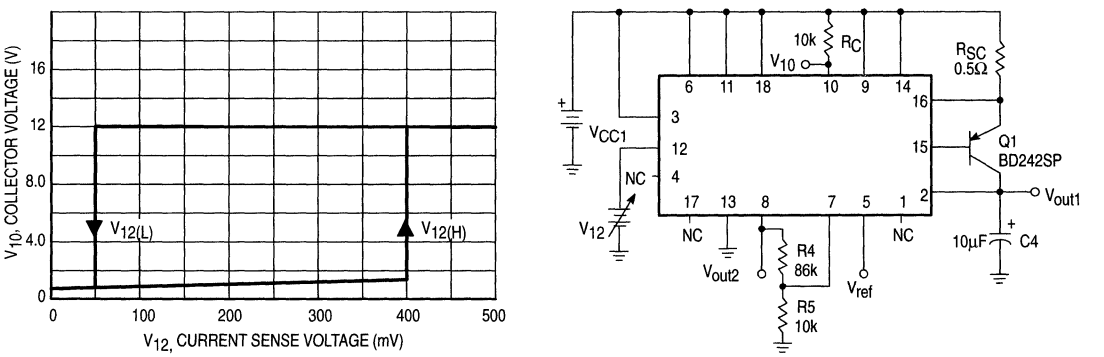


Figure 9. Collector Current Detection Level



3

Figure 10. Power Switch Characteristics

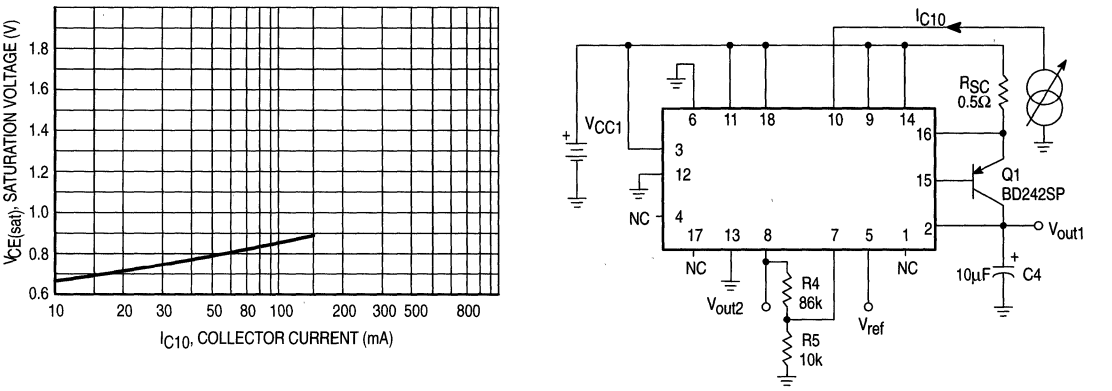


Figure 11. Rectifier Characteristics

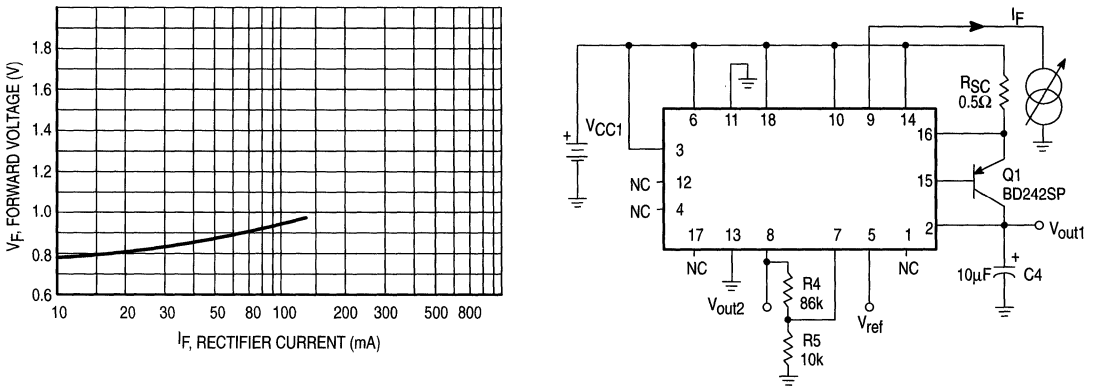
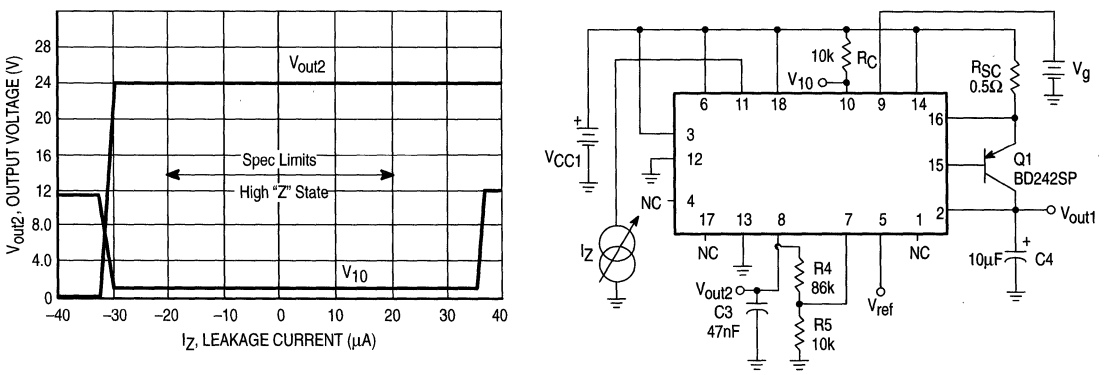


Figure 12. INH 2 Leakage Current Immunity



APPLICATIONS INFORMATION

(See Figure 18)

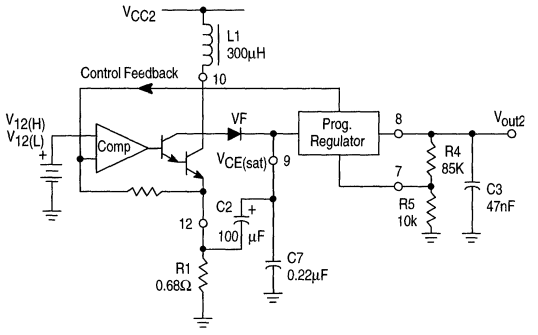
Voltage Reference (V_{ref})

The voltage reference V_{ref} is based upon a highly stable bandgap voltage reference and is accessible on Pin 5 for additional tasks. This circuit part has its own supply connection on Pin 3 and is, therefore, able to operate in standby mode. The RC network R3, C6 improves the ripple rejection on both regulators.

DC/DC Converter

The dc/dc converter performs according to the flyback principle and does not need a time base circuit. The maximum coil current is well defined by means of the current sensing resistor R1 under all working conditions (startup phase, circuit overload, wide supply voltage range and extreme load current change). Figure 13 shows the Simplified Converter Schematic.

Figure 13. Simplified Converter Schematic



A simplified method on "how to calculate the coil inductance" is given below. The operation point at minimum supply voltage (V_{CC2}) and max. output current (I_{out2}) for a fixed output voltage (V_{out2}) determines the coil data. Figure 14 shows the typical voltage and current waveforms on the coil L1 (coil losses neglected).

Equations (1) and (2) yield the respective coil voltage V_L- and V_L+ (see Figure 14):

$$V_L+ = V_{out2} + \Delta V_{(Pin\ 9\ -\ Pin\ 8)} + V_F - V_{CC2} \quad (1)$$

$$V_L- = V_{CC2} - V_{CE(sat)} - V_{12(H)} \quad (2)$$

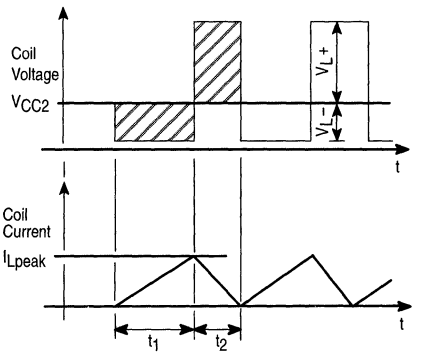
[$\Delta V_{(Pin\ 9\ -\ Pin\ 8)}$: input/output voltage drop of the regulator, 2.5 V typical]

[V_F, $V_{CE(sat)}$, $V_{12(H)}$: see Electrical Characteristics Table]

The time ratio α for the charging time to dumping time is defined by Equation (3):

$$\alpha = \frac{t_1}{t_2} = \frac{V_L+}{V_L-} \quad (3)$$

Figure 14. Voltage and Current Waveform on the Coil (not to scale)



The coil charging time t_1 is found using Equation (4):

$$t_1 = \frac{1}{(1 + \frac{1}{\alpha}) \cdot f} \quad (4)$$

[f : minimum oscillation frequency which should be chosen above the audio frequency band (e.g. 20 kHz)]

Knowing the dc output current I_{out2} of the programmable regulator, the peak coil current $I_{L(peak)}$ can now be calculated:

$$I_{L(peak)} = 2 \cdot (I_{out2})\ (1 + \alpha) \quad (5)$$

The coil inductance L1 of the nonsaturated coil is given by Equation (6):

$$L1 = \frac{t_1}{I_{L(peak)}}\ (V_L-) \quad (6)$$

The formula (6a) yields the current sensing resistor R1 for a defined peak coil current $I_{L(peak)}$:

$$R1 = \frac{V_{12(H)}}{I_{L(peak)}} \quad (6a)$$

In order to limit the by–pass current through capacitor C7 during the energy dumping phase the value C2>>C7 should be implemented.

For all other operation conditions, the feedback signal from the programmable voltage regulator controls the activity of the converter.

Programmable Voltage Regulator

This series voltage regulator is programmable by the voltage divider R4, R5 for a nominal output voltage of 6.0 V ≤ V_{out2} ≤ 30 V.

$$R4 = \frac{(V_{out2} - V_{ref\ nom}) \cdot R5}{V_{ref\ nom}} \quad (7)$$

[R5 = 10 k, $V_{ref\ nom}$ = 2.5 V]

Current limitation and thermal shutdown capability are standard features of this regulator. The voltage drop $\Delta V_{(Pin\ 9 - Pin\ 8)}$ across the series pass transistor generates the feedback signal to control the dc/dc converter (see Figure 13).

Control Inputs INH1, INH2

The dc/dc converter and/or the regulator V_{out2} are remote controllable through the TTL, MOS compatible inhibit inputs INH1 and INH2 where the latter is a three–level detector (Logic "0", High Impedance "Z", Logic "1"). Both inputs are set–up to provide the following truth table:

Figure 15. INH1, INH2 TruthTable

Mode	INH1	INH2	V_{out2}	DC/DC
1	0	0	OFF	INT
2	0	High "Z"	V_{out2}	ON
3	0	1	V_{out2}	INT
4	1	0	OFF	INT
5	1	High "Z"	5.0 V	ON
6	1	1	5.0 V	INT

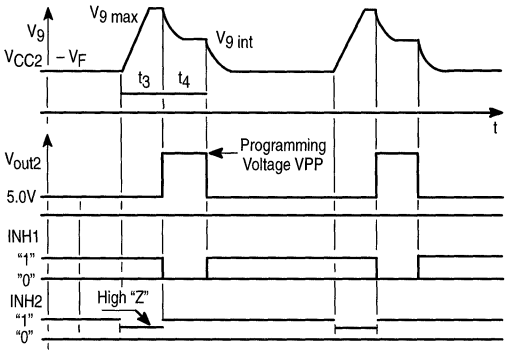
INT: Intermittent operation of the converter means that the converter operates only if $V_{CC2} < V_{out2}$.

ON: The converter loads the storage capacitor C2 to its full charge (V_9 = 33 V), allowing fast response time of the regulator V_{out2} when addressed by the control software.

OFF: High impedance (internal resistor 10 k to ground)

Figure 16 represents a typical timing diagram for an E²PROM programming sequence in a microprocessor based system. The High "Z" state enables the dc/dc converter to ramp during t_3 to the voltage V_9 at Pin 9 to a high level before the write cycle takes place in the memory.

Figure 16. Typical E²PROM Programming Sequence
(not to scale)



Microprocessor Supply Regulator

Together with an external PNP power transistor (Q1), a 5.0 V supply exhibiting low voltage drop is obtained to power microprocessor systems and auxiliary circuits. Using a power Darlington with adequate heat sink in the output stage boosts the output current I_{out1} above 1.0 A.

The current limitation circuit measures the emitter current of Q1 by means of the sensing resistor, R_{SC}:

$$R_{SC} = \frac{V_{RSC}}{I_E} \quad (8)$$

[I_E: emitter current of Q1]

[V_{RSC}: threshold voltage (see Electrical Characteristics Table)]

The voltage protection circuit performs a foldback characteristic above a nominal operating voltage, V_{CC2} ≥ 18 V.

Delay and Watchdog Circuit

The undervoltage monitor supervises the power supply V_{out1} and releases the delay circuit $\overline{RESET}$ as soon as the regulator output reaches the microprocessor operating a range [e.g., $V_{low} \geq 0.93 \cdot V_{out1(nom)}$]. The $\overline{RESET}$ output has an open–collector and may be connected in a "wired–OR" configuration.

The watchdog circuit consists of a retriggerable monostable with a negative edge sensitive control input WDI. The watchdog feature may be disabled by means of the watchdog select input $\overline{WDS}$ driven to a "1". Figure 17 displays the Typical $\overline{RESET}$ Timing Diagram.

The commuted current source I_{C5} on Pin 17, threshold voltage $V_{C5(L)}$, $V_{C5(H)}$ and an external capacitor C5 define the $\overline{RESET}$ delay and the watchdog timing. The relationship of the timing signals are indicated by the Equations (9) to (11).

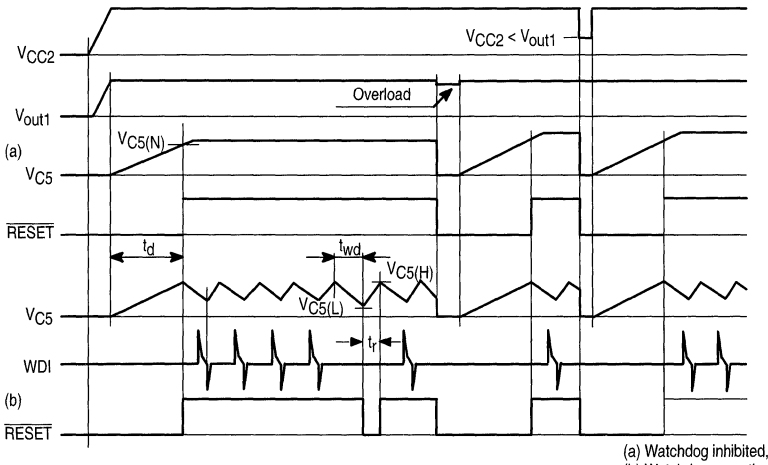
$$\overline{RESET}\ \text{delay:}\quad t_d = \frac{C5 \cdot V_{C5(H)}}{|I_{C5}|} \quad (9)$$

$$\text{Watchdog timeout:}\quad t_{wd} = \frac{C5 \cdot (V_{C5(H)} - V_{C5(L)})}{5 \cdot I_{C5}} \quad (10)$$

$$\text{Watchdog } \overline{RESET}\text{:}\quad t_r = \frac{C5 \cdot (V_{C5(H)} - V_{C5(L)})}{50 \cdot |I_{C5}|} \quad (11)$$

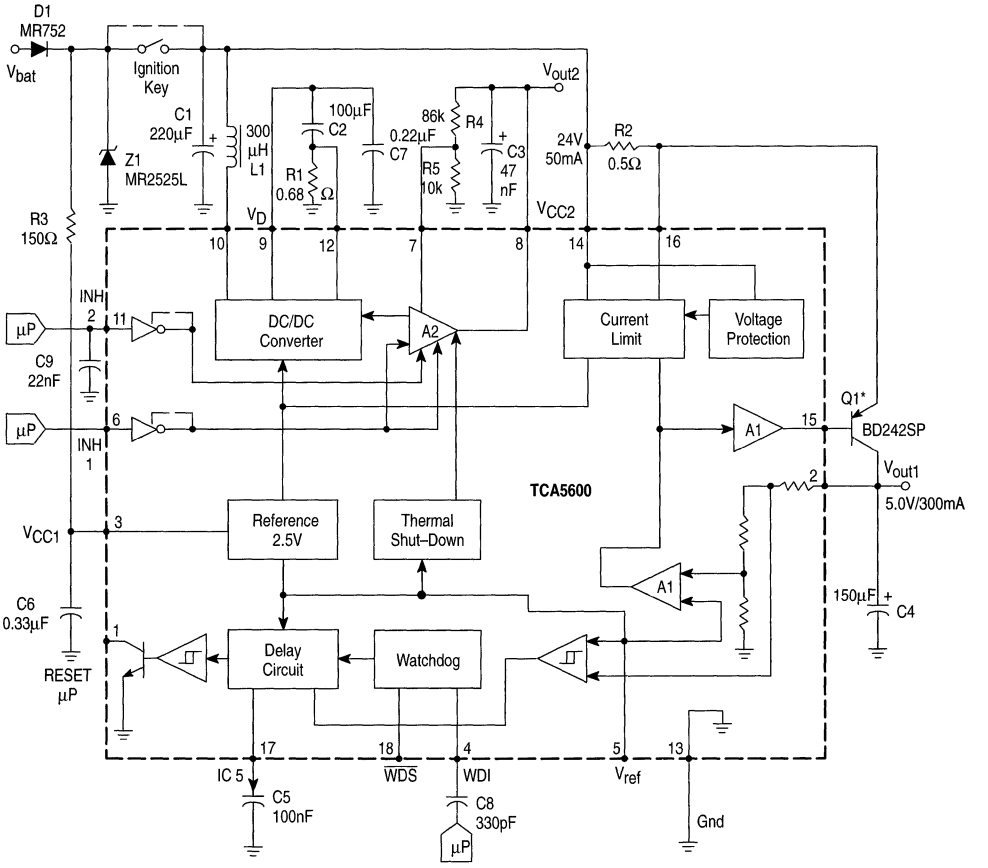
[I_{C5}, $V_{C5(H)}$, $V_{C5(L)}$: see Electrical Characteristics Table]

Figure 17. Typical $\overline{\text{RESET}}$ Timing Diagram (not to scale)



(a) Watchdog inhibited, $\overline{\text{WDS}}$ = "1"
(b) Watchdog operational, $\overline{\text{WDS}}$ = "0"

Figure 18. Typical Automative Application



TL494

SWITCHMODE™ Pulse Width Modulation Control Circuit

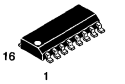
3

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for SWITCHMODE power supply control.

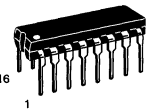
- Complete Pulse Width Modulation Control Circuitry
- On–Chip Oscillator with Master or Slave Operation
- On–Chip Error Amplifiers
- On–Chip 5.0 V Reference
- Adjustable Deadtime Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push–Pull or Single–Ended Operation
- Undervoltage Lockout

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

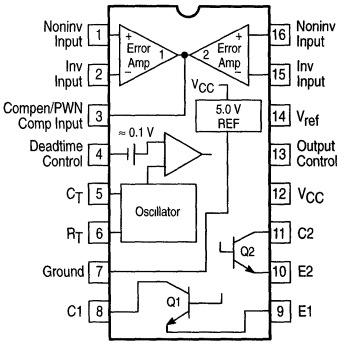


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	TL494C	TL494I	Unit
Power Supply Voltage	V_{CC}	42		V
Collector Output Voltage	V_{C1}, V_{C2}	42		V
Collector Output Current (Each transistor) (Note 1)	I_{C1}, I_{C2}	500		mA
Amplifier Input Voltage Range	V_{IR}	–0.3 to +42		V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000		mW
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	80		°C/W
Operating Junction Temperature	T_J	125		°C
Storage Temperature Range	T_{stg}	–55 to +125		°C
Operating Ambient Temperature Range TL494C TL494I	T_A	0 to +70 –25 to +85		°C
Derating Ambient Temperature	T_A	45		°C

NOTE: 1. Maximum thermal limits must be observed.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
TL494CD	T_A = 0° to +70°C	SO–16
TL494CN		Plastic
TL494IN	T_A = – 25° to +85°C	Plastic

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	–	30	40	V
Collector Output Current (Each transistor)	I_{C1}, I_{C2}	–	–	200	mA
Amplified Input Voltage	V_{in}	–0.3	–	V_{CC} – 2.0	V
Current Into Feedback Terminal	I_{fb}	–	–	0.3	mA
Reference Output Current	I_{ref}	–	–	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted.)

For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	–	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	3.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	mA
OUTPUT SECTION					
Collector Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	–	2.0	100	μA
Emitter Off–State Current V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	–	–	–100	μA
Collector–Emitter Saturation Voltage (Note 2)					V
Common–Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	–	1.1	1.3	
Emitter–Follower (V_C = 15 V, I_E = –200 mA)	$V_{sat(E)}$	–	1.5	2.5	
Output Control Pin Current					
Low State (V_{OC} ≤ 0.4 V)	I_{OCL}	–	10	–	μA
High State (V_{OC} = V_{ref})	I_{OCH}	–	0.2	3.5	mA
Output Voltage Rise Time	t_r				ns
Common–Emitter (See Figure 12)		–	100	200	
Emitter–Follower (See Figure 13)		–	100	200	
Output Voltage Fall Time	t_f				ns
Common–Emitter (See Figure 12)		–	25	100	
Emitter–Follower (See Figure 13)		–	40	100	

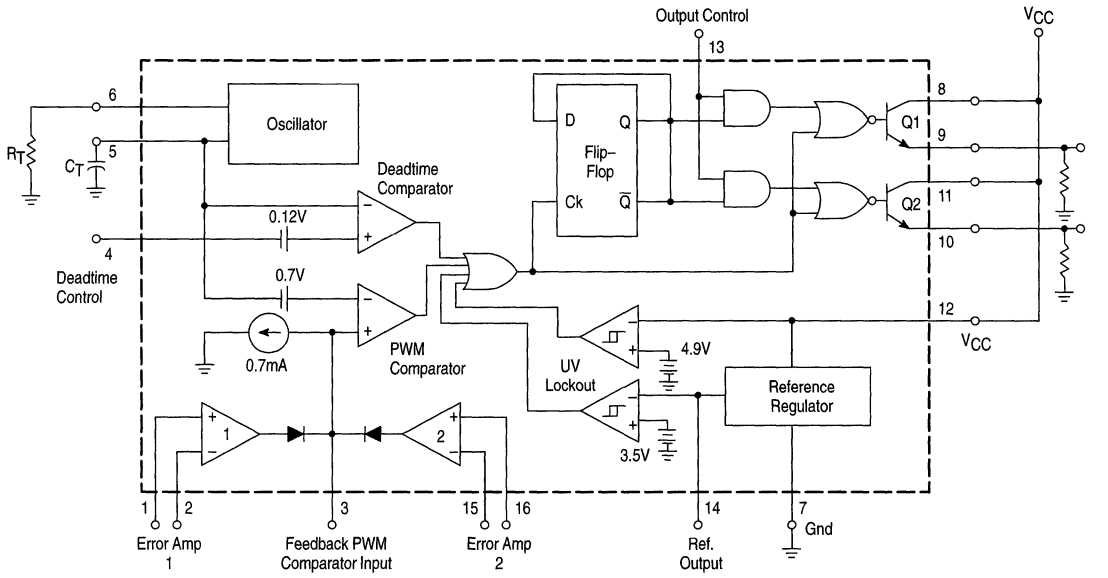
NOTE: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O\ (Pin\ 3)}$ = 2.5 V)	V_{IO}	–	2.0	10	mV
Input Offset Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IO}	–	5.0	250	nA
Input Bias Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IB}	–	–0.1	–1.0	μA
Input Common Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	–0.3 to V_{CC}–2.0			V
Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	–	dB
Unity–Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_{C-}	–	350	–	kHz
Phase Margin at Unity–Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	–	65	–	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	–	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	–	100	–	dB
Output Sink Current ($V_{O\ (Pin\ 3)}$ = 0.7 V)	I_{O-}	0.3	0.7	–	mA
Output Source Current ($V_{O\ (Pin\ 3)}$ = 3.5 V)	I_{O+}	2.0	–4.0	–	mA
PWM COMPARATOR SECTION (Test Circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	2.5	4.5	V
Input Sink Current ($V_{(Pin\ 3)}$ = 0.7 V)	I_{I-}	0.3	0.7	–	mA
DEADTIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 V to 5.25 V)	$I_{IB\ (DT)}$	–	–2.0	–10	μA
Maximum Duty Cycle, Each Output, Push–Pull Mode ($V_{Pin\ 4}$ = 0 V, C_T = 0.01 μF, R_T = 12 kΩ) ($V_{Pin\ 4}$ = 0 V, C_T = 0.001 μF, R_T = 30 kΩ)	DC_{max}	 45 –	 48 45	 50 50	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{th}	 – 0	 2.8 –	 3.3 –	V
OSCILLATOR SECTION					
Frequency (C_T = 0.001 μF, R_T = 30 kΩ)	f_{osc}	–	40	–	kHz
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 30 kΩ)	σf_{osc}	–	3.0	–	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	–	0.1	–	%
Frequency Change with Temperature ($\Delta T_A = T_{low}$ to T_{high}) (C_T = 0.01 μF, R_T = 12 kΩ)	Δf_{osc} (ΔT)	–	–	12	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn–On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	5.5	6.43	7.0	V
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All other inputs and outputs open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 – –	 5.5 7.0	 10 15	mA
Average Supply Current (C_T = 0.01 μF, R_T = 12 kΩ, $V_{(Pin\ 4)}$ = 2.0 V) (V_{CC} = 15 V) (See Figure 12)		–	7.0	–	mA

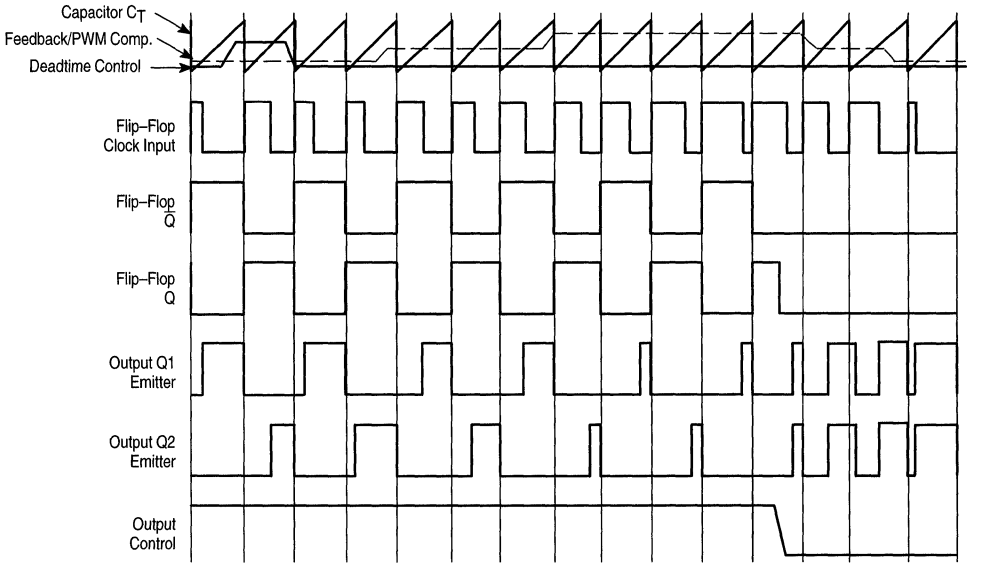
* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \overline{X})^2}{N-1}}$

Figure 1. Representative Block Diagram



This device contains 46 active transistors.

Figure 2. Timing Diagram



APPLICATIONS INFORMATION

Description

The TL494 is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal–linear sawtooth oscillator is frequency–programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip–flop clock–input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control–signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first 4% of the sawtooth–cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime–control input to a fixed voltage, ranging between 0 V to 3.3 V.

Functional Table

Input/Output Controls	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single–ended PWM @ Q1 and Q2	1.0
@ V_{ref}	Push–pull Operation	0.5

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on–time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from –0.3 V to (V_{CC} – 2V), and may be used to sense power–supply output voltage and current. The error–amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse–steering flip–flop and inhibits the output transistors, Q1 and Q2. With the output–control connected to the reference line, the pulse–steering flip–flop directs the modulated pulses to each of the two output transistors alternately for push–pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single–ended operation with a maximum on–time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output–drive currents are required for single–ended operation, Q1 and Q2 may be connected in parallel, and the output–mode pin must be tied to ground to disable the flip–flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±5.0% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C.

Figure 3. Oscillator Frequency versus Timing Resistance

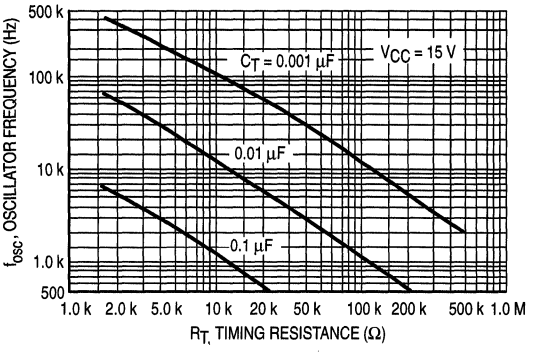


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

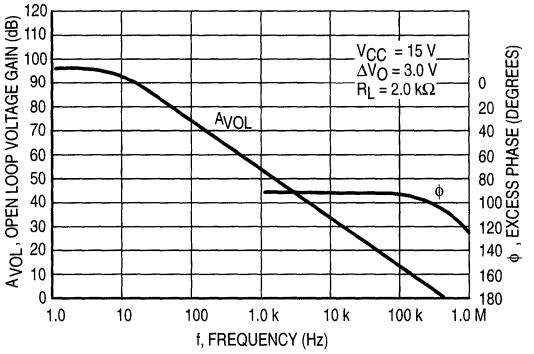


Figure 5. Percent Deadtime versus Oscillator Frequency

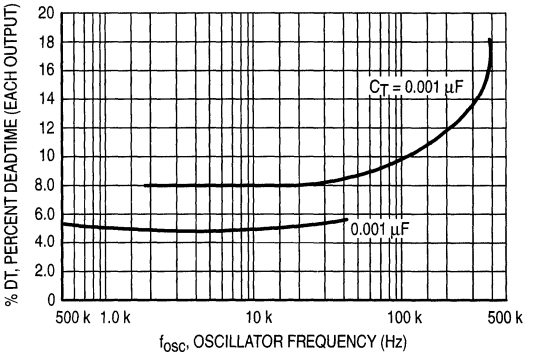


Figure 6. Percent Duty Cycle versus Deadtime Control Voltage

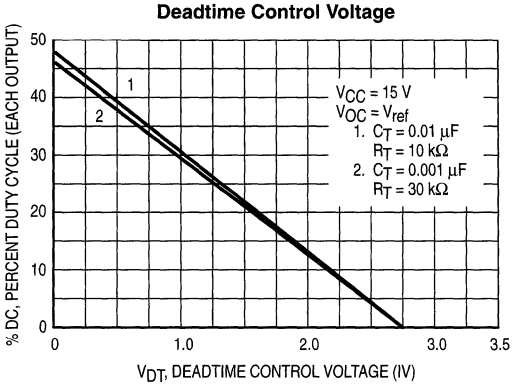


Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current

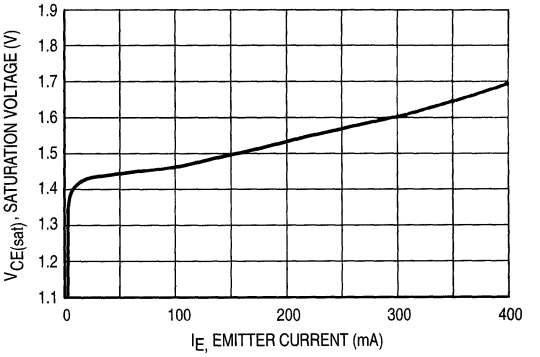


Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current

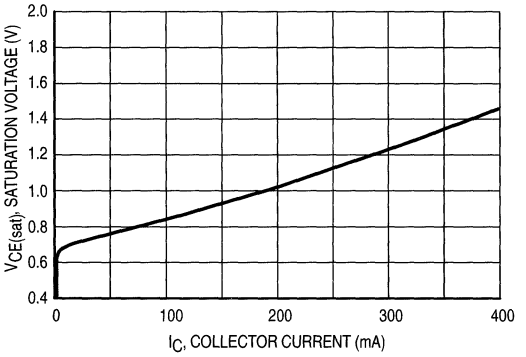


Figure 9. Standby Supply Current versus Supply Voltage

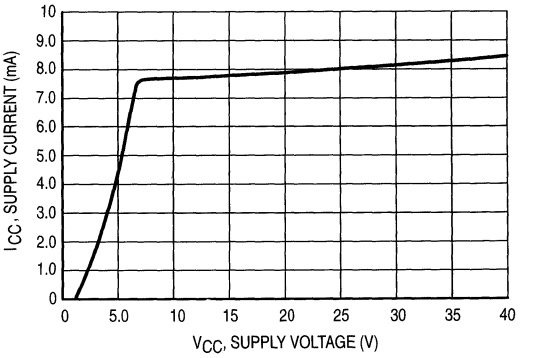


Figure 10. Error–Amplifier Characteristics

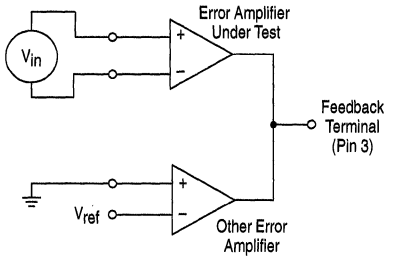


Figure 11. Deadtime and Feedback Control Circuit

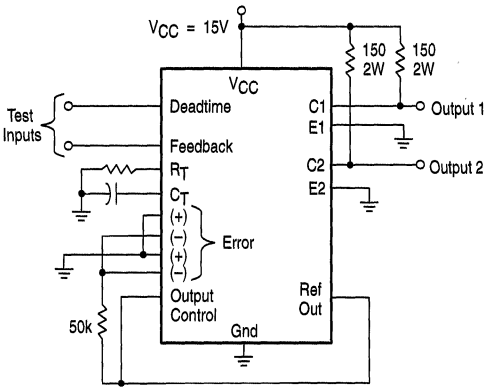


Figure 12. Common–Emitter Configuration Test Circuit and Waveform

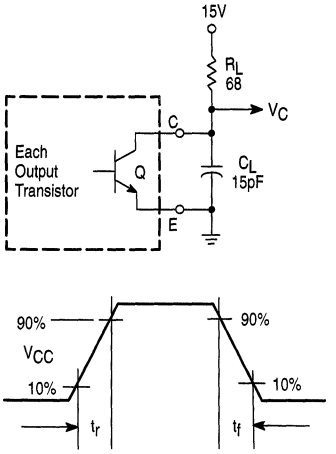


Figure 13. Emitter–Follower Configuration Test Circuit and Waveform

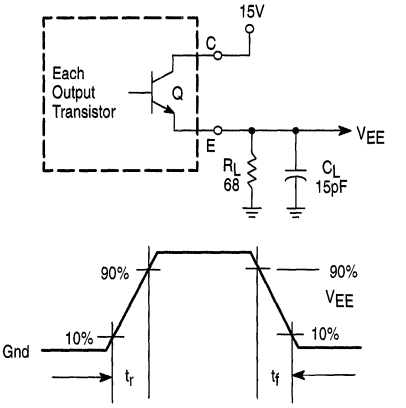
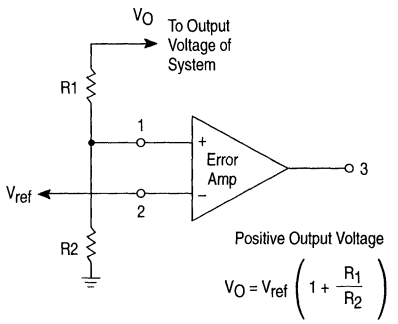


Figure 14. Error–Amplifier Sensing Techniques



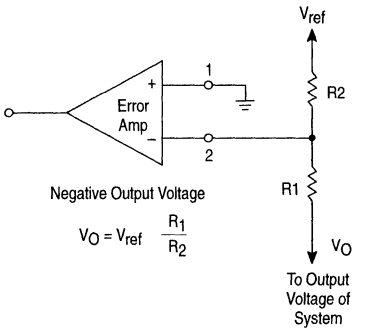


Figure 15. Deadtime Control Circuit

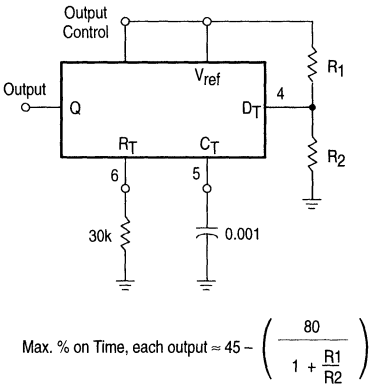


Figure 16. Soft–Start Circuit

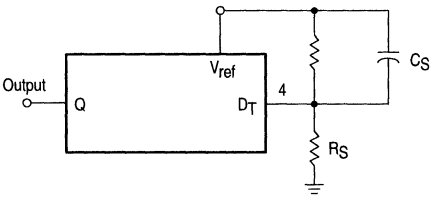
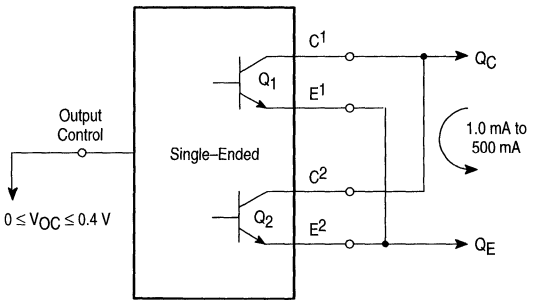


Figure 17. Output Connections for Single–Ended and Push–Pull Configurations



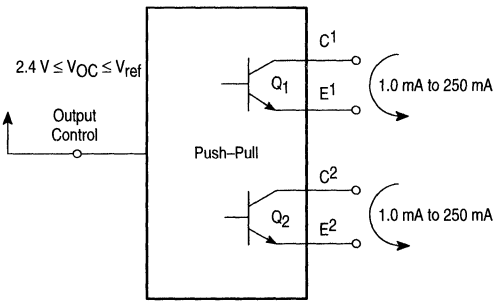


Figure 18. Slaving Two or More Control Circuits

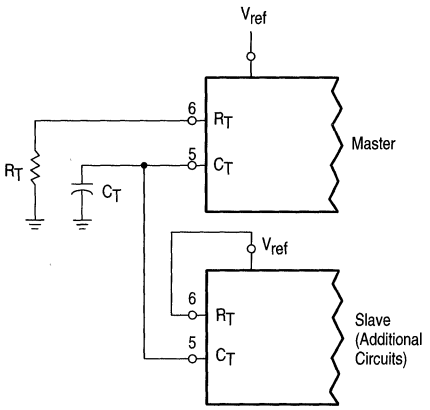


Figure 19. Operation with V_{in} > 40 V Using External Zener

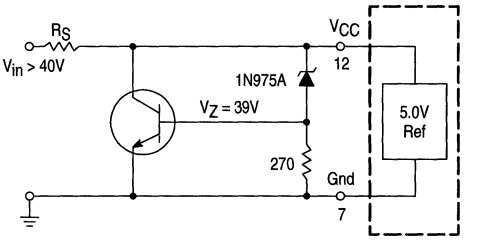
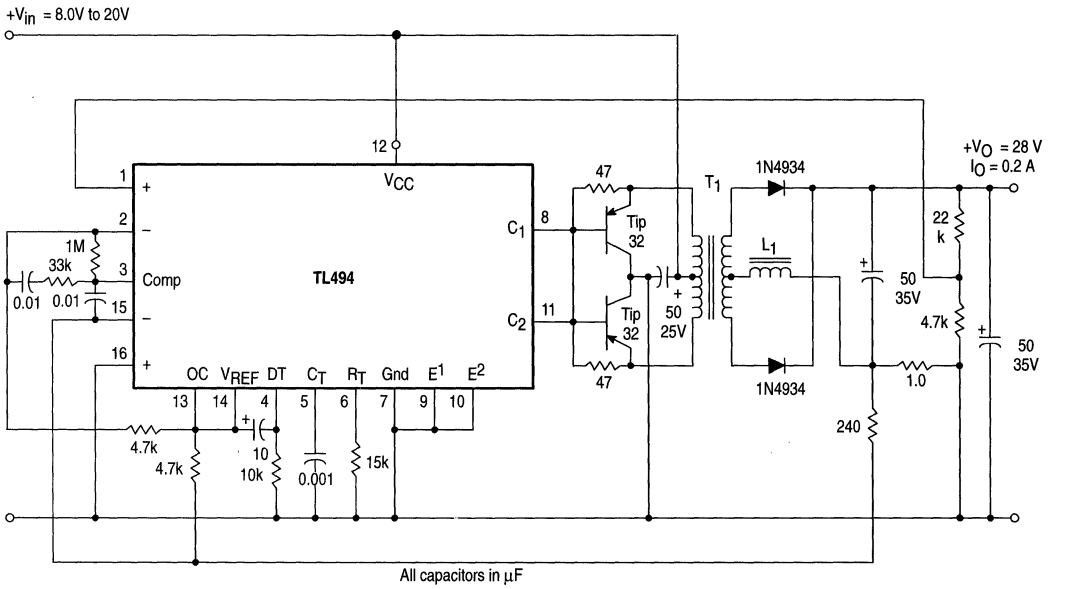


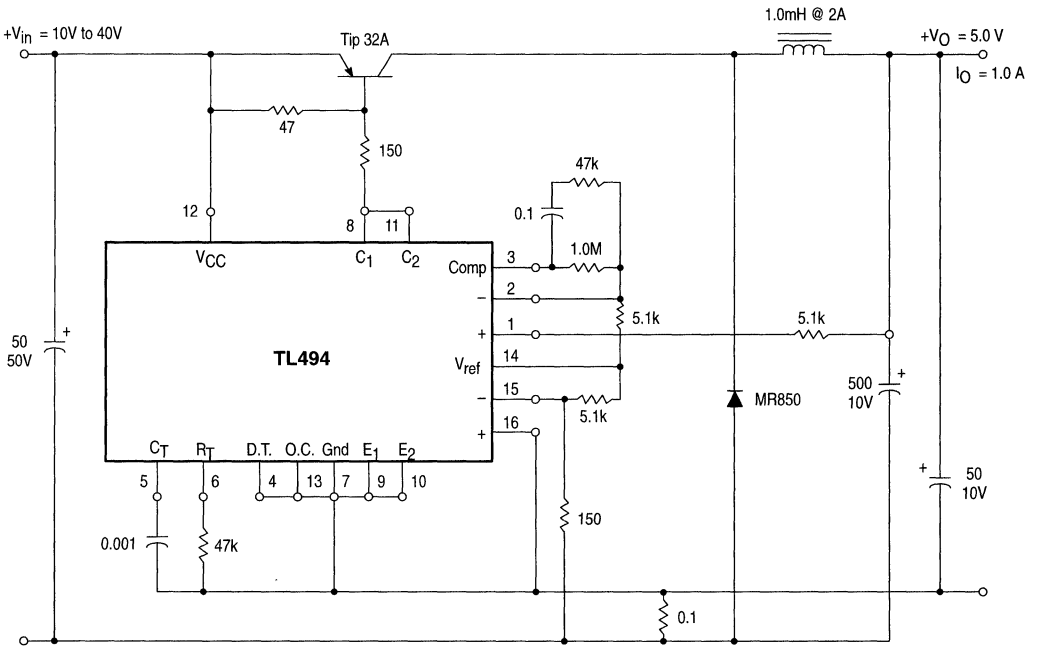
Figure 20. Pulse Width Modulated Push–Pull Converter



Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mV pp P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 28 V, I_O = 1.0 A	71%

L1 – 3.5 mH @ 0.3 A
T1 – Primary: 20T C.T. #28 AWG
Secondary: 12OT C.T. #36 AWG
Core: Ferroxcube 1408P–L00–3CB

Figure 21. Pulse Width Modulated Step–Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 mA to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mV pp P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

MOTOROLA

TL594

3

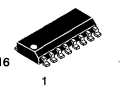
Precision Switchmode Pulse Width Modulation Control Circuit

The TL594 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control.

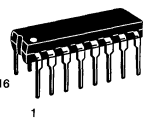
- Complete Pulse Width Modulation Control Circuitry
- On–Chip Oscillator with Master or Slave Operation
- On–Chip Error Amplifiers
- On–Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Deadtime Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push–Pull or Single–Ended Operation
- Undervoltage Lockout

PRECISION SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

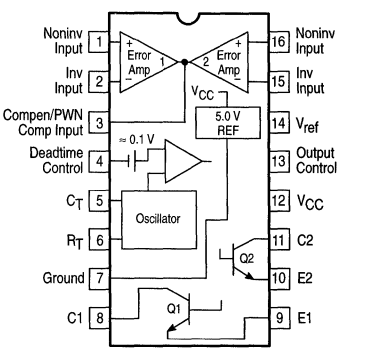


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	42	V
Collector Output Voltage	V_{C1}, V_{C2}	42	V
Collector Output Current (each transistor) (Note 1)	I_{C1}, I_{C2}	500	mA
Amplifier Input Voltage Range	V_{IR}	–0.3 to +42	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	mW
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	80	°C/W
Operating Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Operating Ambient Temperature Range TL594ID, CN TL594CD, IN	T_A	0 to +70 –25 to +85	°C
Derating Ambient Temperature	T_A	45	°C

NOTES: 1. Maximum thermal limits must be observed.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
TL594CD	$T_A = 0°$ to +70°C	SO–16
TL594CN		Plastic
TL594IN	$T_A = -25°$ to +85°C	Plastic

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	–	30	40	V
Collector Output Current (Each transistor)	I_{C1}, I_{C2}	–	–	200	mA
Amplified Input Voltage	V_{in}	0.3	–	V_{CC} – 2.0	V
Current Into Feedback Terminal	I_{fb}	–	–	0.3	mA
Reference Output Current	I_{ref}	–	–	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz
PWM Input Voltage (Pins 3, 4, 13)	–	0.3	–	5.3	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted.)

For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA, T_A = 25°C) (I_O = 1.0 mA)	V_{ref}	 4.925 4.9	 5.0 –	 5.075 5.1	V
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	–	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	2.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	40	75	mA
OUTPUT SECTION					
Collector Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	–	2.0	100	μA
Emitter Off–State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	–	–	–100	μA
Collector–Emitter Saturation Voltage (Note 2) Common–Emitter (V_E = 0 V, I_C = 200 mA) Emitter–Follower (V_C = 15 V, I_E = –200 mA)	 $V_{SAT(C)}$ $V_{SAT(E)}$	 – –	 1.1 1.5	 1.3 2.5	V
Output Control Pin Current Low State ($V_{OC} \leq$ 0.4 V) High State (V_{OC} = V_{ref})	 I_{OCL} I_{OCH}	 – –	 0.1 2.0	 – 20	μA
Output Voltage Rise Time Common–Emitter (See Figure 13) Emitter–Follower (See Figure 14)	t_r	 – –	 100 100	 200 200	ns
Output Voltage Fall Time Common–Emitter (See Figure 13) Emitter–Follower (See Figure 14)	t_f	 – –	 40 40	 100 100	ns
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O\ (Pin\ 3)}$ = 2.5 V)	V_{IO}	–	2.0	10	mV
Input Offset Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IO}	–	5.0	250	nA
Input Bias Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IB}	–	–0.1	–1.0	μA
Input Common Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	0 to V_{CC}–2.0			V
Inverting Input Voltage Range	$V_{IR(INV)}$	–0.3 to V_{CC}–2.0			V
Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	–	dB
Unity–Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_C	–	700	–	kHz
Phase Margin at Unity–Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕm	–	65	–	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	–	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	–	100	–	dB
Output Sink Current ($V_{O\ (Pin\ 3)}$ = 0.7 V)	I_{O-}	0.3	0.7	–	mA
Output Source Current ($V_{O\ (Pin\ 3)}$ = 3.5 V)	I_{O+}	–2.0	–4.0	–	mA

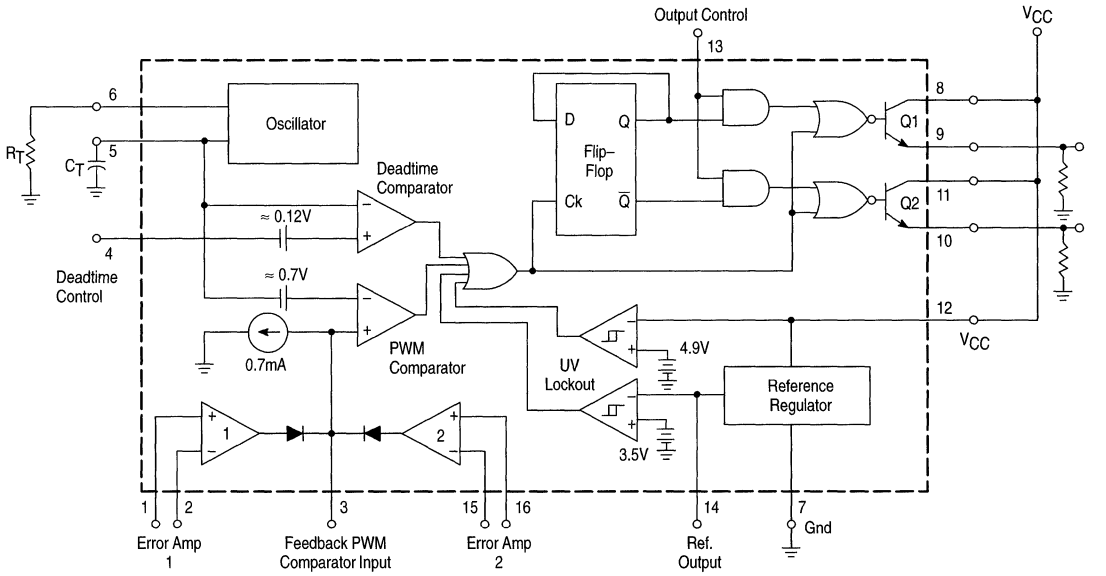
NOTE: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Test Circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	3.6	4.5	V
Input Sink Current ($V_{Pin\ 3}$ = 0.7 V)	I_{I-}	0.3	0.7	–	mA
DEADTIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 V to 5.25 V)	I_{IB} (DT)	–	–2.0	–10	μA
Maximum Duty Cycle, Each Output, Push–Pull Mode ($V_{Pin\ 4}$ = 0 V, C_T = 0.01 μF, R_T = 12 kΩ) ($V_{Pin\ 4}$ = 0 V, C_T = 0.001 μF, R_T = 30 kΩ)	DC_{max}	 45 –	 48 45	 50 –	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 – 0	 2.8 –	 3.3 –	V
OSCILLATOR SECTION					
Frequency (C_T = 0.001 μF, R_T = 30 kΩ) (C_T = 0.01 μF, R_T = 12 kΩ, T_A = 25°C) (C_T = 0.01 μF, R_T = 12 kΩ, T_A = T_{low} to T_{high})	f_{osc}	 – 9.2 9.0	 40 10 –	 – 10.8 12	kHz
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 30 kΩ)	σf_{osc}	–	1.5	–	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	–	0.2	1.0	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}, C_T = 0.01 μF, R_T = 12 kΩ)	Δf_{osc} (ΔT)	–	4.0	–	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn–On Threshold (V_{CC} Increasing, I_{ref} = 1.0 mA) T_A = 25°C T_A = T_{low} to T_{high}	V_{th}	 4.0 3.5	 5.2 –	 6.0 6.5	V
Hysteresis TL594C,I TL594M	V_H	 100 50	 150 150	 300 300	mV
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All other inputs and outputs open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 – –	 8.0 8.0	 15 18	mA
Average Supply Current ($V_{Pin\ 4}$ = 2.0 V, C_T = 0.01 μF, R_T = 12 kΩ, V_{CC} = 15 V, See Figure 11)		–	11	–	mA

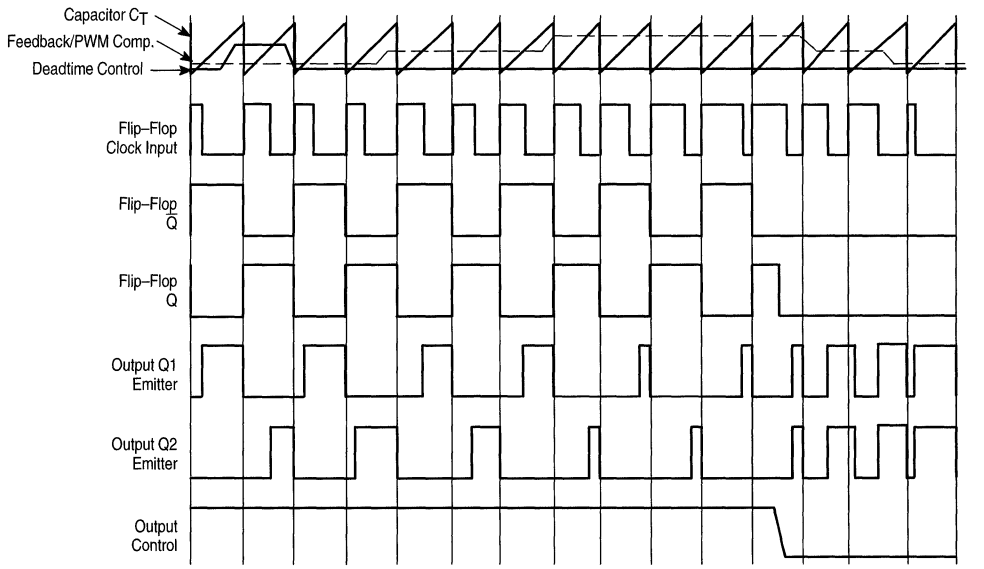
* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \bar{X})^2}{N-1}}$

Figure 1. Representative Block Diagram



This device contains 46 active transistors.

Figure 2. Timing Diagram



APPLICATIONS INFORMATION

Description

The TL594 is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal–linear sawtooth oscillator is frequency–programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip–flop clock–input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control–signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first 4% of the sawtooth–cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime–control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on–time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common–mode input range from –0.3 V to (V_{CC} – 2 V), and may be used to sense power–supply output voltage and current. The error–amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse–steering flip–flop and inhibits the output transistors, Q1 and Q2. With the output–control connected to the reference line, the pulse–steering flip–flop directs the modulated pulses to each of the two output transistors alternately for push–pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single–ended operation with a maximum on–time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output–drive currents are required for single–ended operation, Q1 and Q2 may be connected in parallel, and the output–mode pin must be tied to ground to disable the flip–flop. The output frequency will now be equal to that of the oscillator.

The TL594 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±1.5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C.

Functional Table

Input/Output Controls	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single–ended PWM @ Q1 and Q2	1.0
@ V_{ref}	Push–pull Operation	0.5

Figure 3. Oscillator Frequency versus Timing Resistance

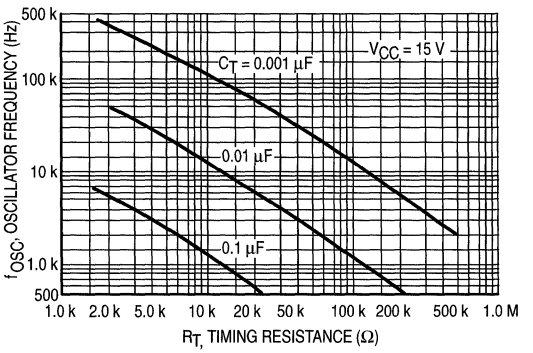


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

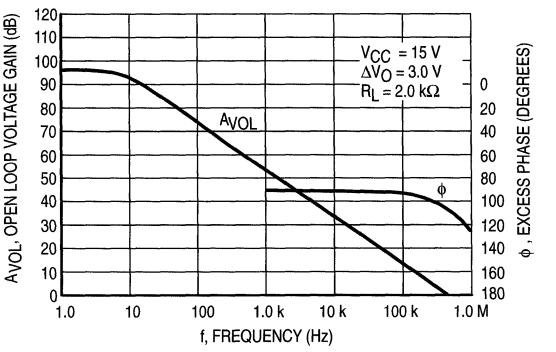


Figure 5. Percent Deadtime versus Oscillator Frequency

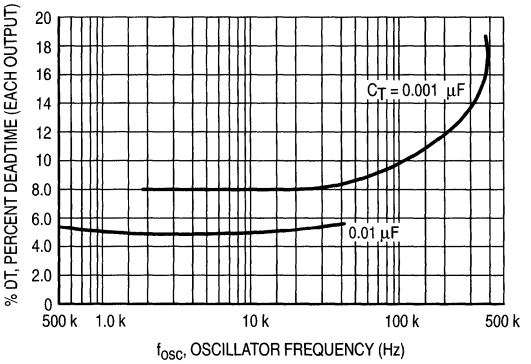


Figure 6. Percent Duty Cycle versus Deadtime Control Voltage

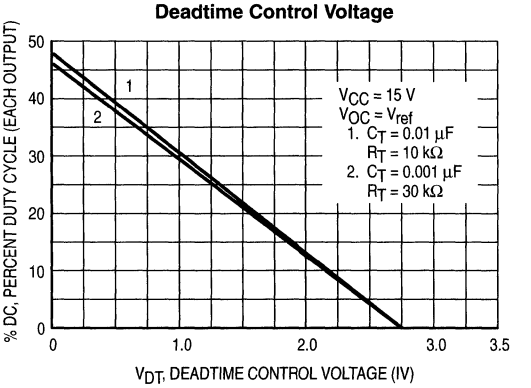


Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current

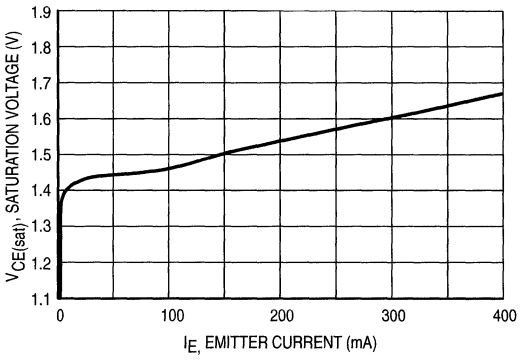


Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current

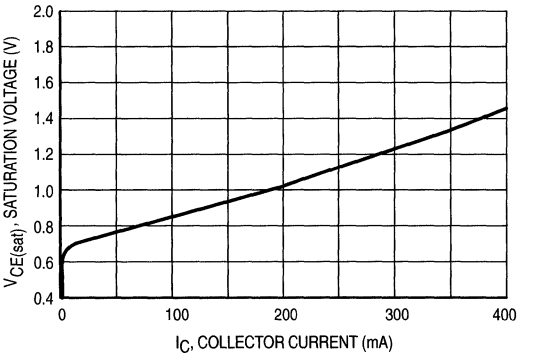


Figure 9. Standby Supply Current versus Supply Voltage

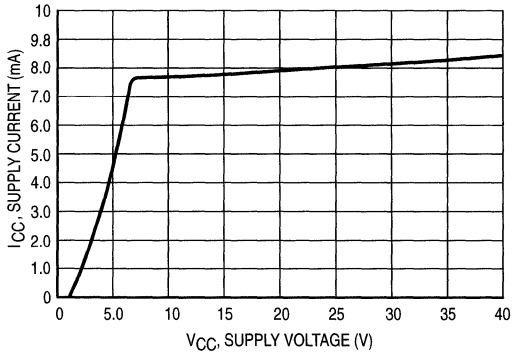


Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current

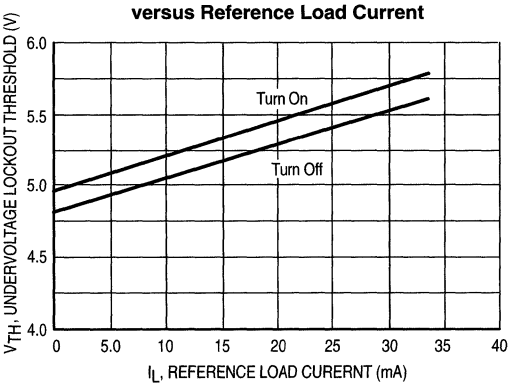


Figure 11. Error–Amplifier Characteristics

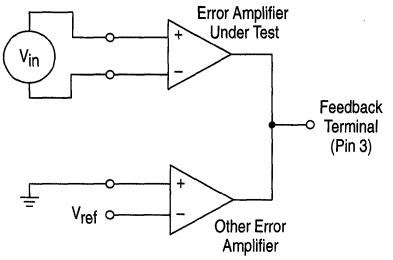


Figure 12. Deadtime and Feedback Control Circuit

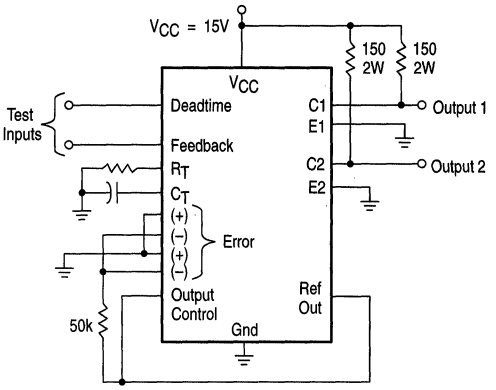


Figure 13. Common–Emitter Configuration Test Circuit and Waveform

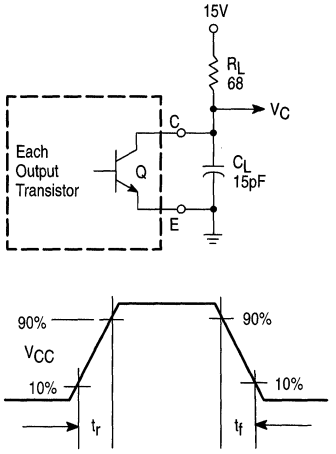


Figure 14. Emitter–Follower Configuration Test Circuit and Waveform

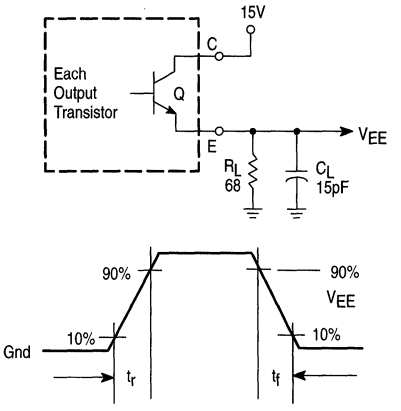
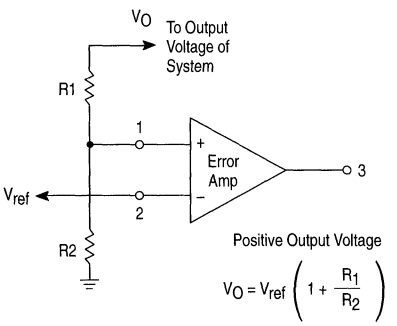


Figure 15. Error–Amplifier Sensing Techniques



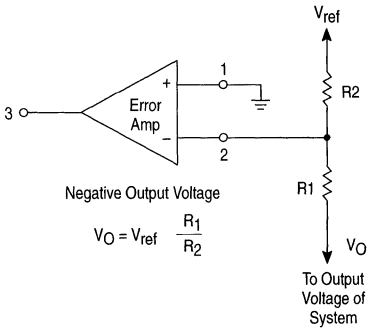
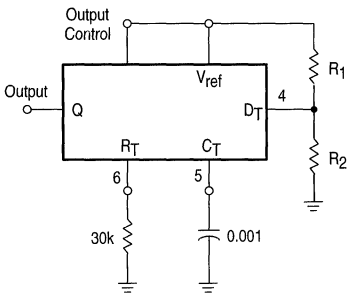


Figure 16. Deadtime Control Circuit



Max. % on Time, each output ≈ 45 – (80 / (1 + R1/R2))

Figure 17. Soft–Start Circuit

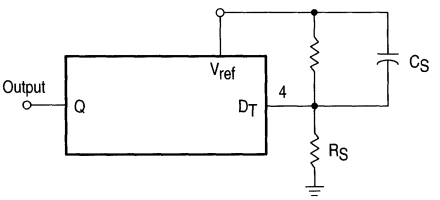
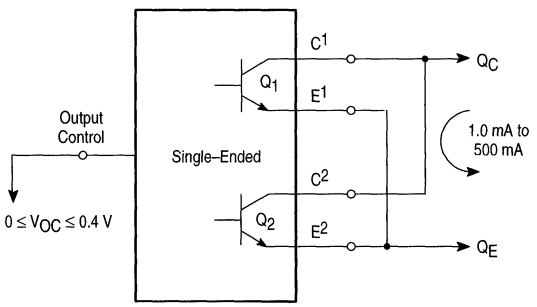
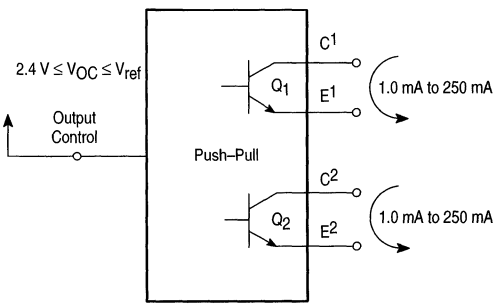


Figure 18. Output Connections for Single–Ended and Push–Pull Configurations





3

Figure 19. Slaving Two or More Control Circuits

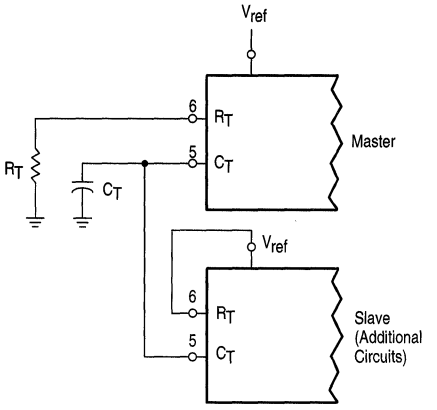


Figure 20. Operation with V_{in} > 40 V Using External Zener

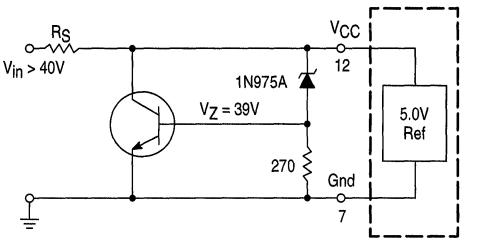
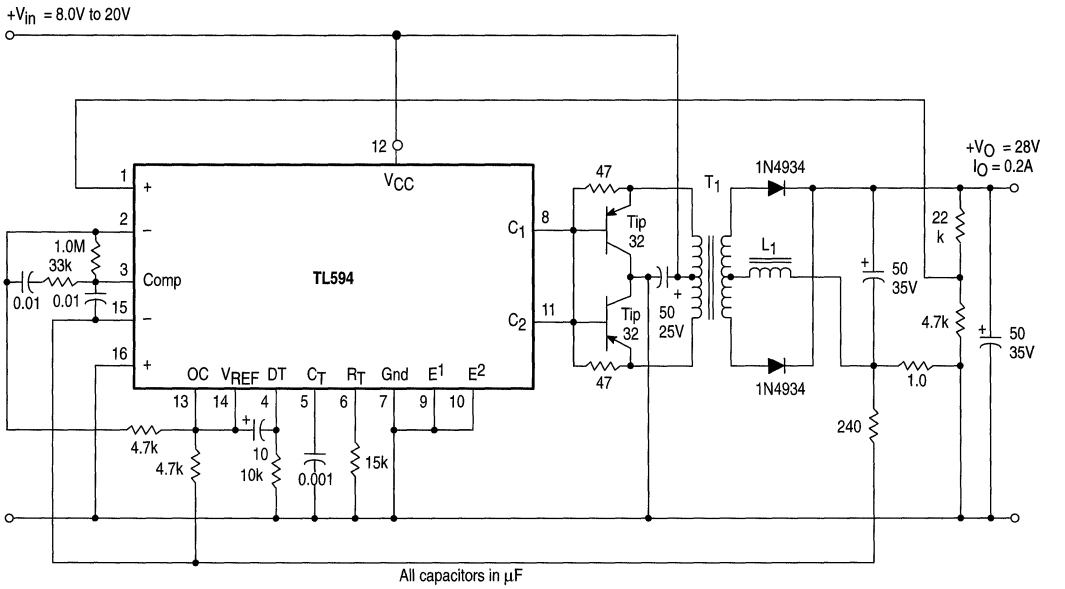


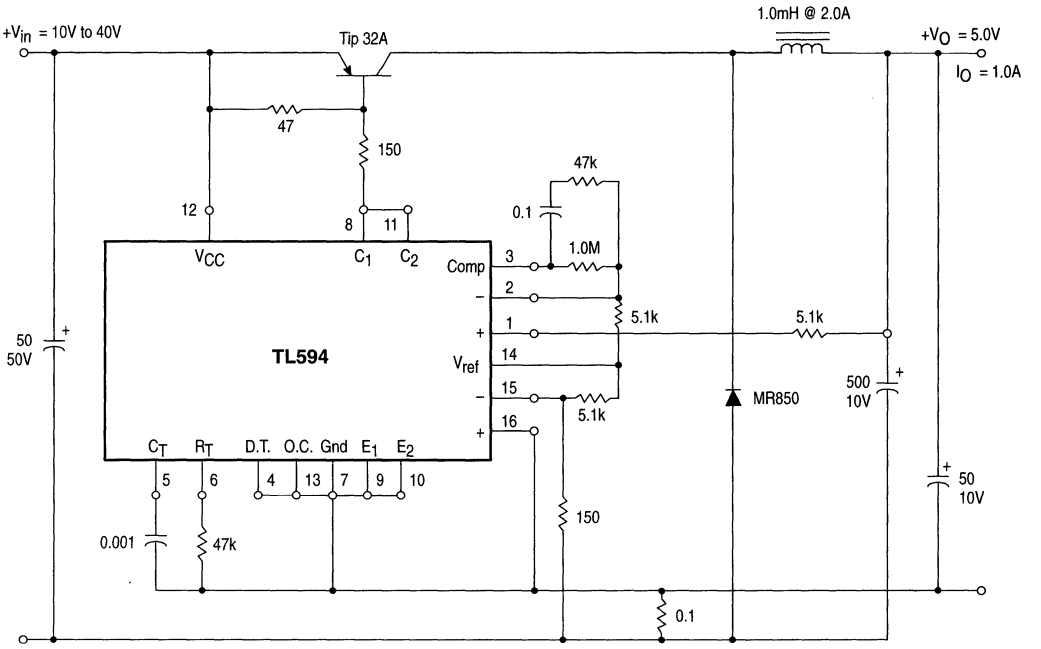
Figure 21. Pulse Width Modulated Push–Pull Converter



Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mVpp P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 28 V, I_O = 1.0 A	71%

L1 – 3.5 mH @ 0.3 A
T1 – Primary: 20T C.T. #28 AWG
Secondary: 12OT C.T. #36 AWG
Core: Ferroxcube 1408P–L00–3CB

Figure 22. Pulse Width Modulated Step–Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 mA to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mVpp P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

MOTOROLA

TL780 Series

3

Three-Terminal Positive Fixed Voltage Regulators

This family of precision fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.5 A. Innovative design concepts, coupled with advanced thermal layout techniques have resulted in improved accuracy and excellent load, line and thermal regulation characteristics. Internal current limiting, thermal shutdown and safe–area compensation are employed, making these devices extremely rugged and virtually immune to overload.

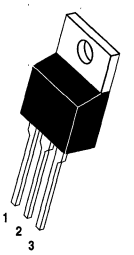
- ±1% Output Voltage Tolerance @ 25°C
- ±2% Output Voltage Tolerance over Full Operating Temperature Range
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- Output Transistor Safe–Area Compensation
- No External Components Required
- Pinout Compatible with MC7800 Series

THREE–TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA

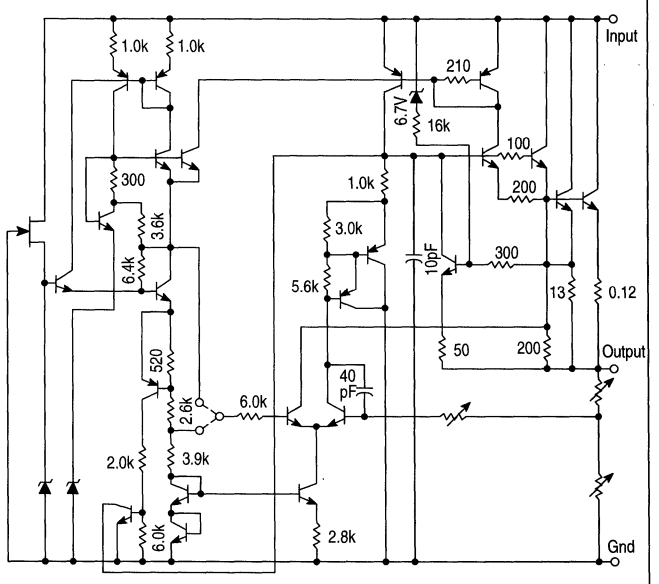
KC SUFFIX
PLASTIC PACKAGE
CASE 221A

Pin 1. Input
2. Ground
3. Output

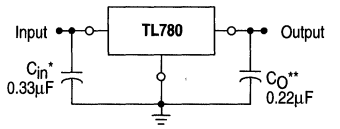


Heatsink surface is connected to Pin 2.

Representative Schematic Diagram



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

(XX), these two digits of the type number indicate voltage.

* C_{in} is required if regulator is located an appreciable distance from power supply filter.

** C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Nominal Output	Device	Operating Temperature Range
5.0 V	TL780–05CKC	T_J = 0° to 125°C
12 V	TL780–12CKC	
15 V	TL780–15CKC	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation and Thermal Characteristics			
T_A = +25°C	P_D	2.0	W
Derate above T_A = +25°C	$1/\theta_{JA}$	16	mW/°C
Thermal Resistance, Junction–to–Air	θ_{JA}	62.5	°C/W
T_A = +25°C	P_D	15	W
Derate above T_C = +75°C (See Figure 1)	$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	TL780–05C			Unit
		Min	Typ	Max	
Output Voltage	V_O				V
5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
7.0 V ≤ V_{in} ≤ 20 V					
T_J = +25°C		4.95	5.0	5.05	
0°C ≤ T_J ≤ +125°C		4.90	—	5.10	
Line Regulation (T_J = +25°C)	Reg_{line}				mV
7.0 V ≤ V_{in} ≤ 25 V		—	0.5	5.0	
8.0 V ≤ V_{in} ≤ 12 V		—	0.5	5.0	
Load Regulation (T_J = +25°C)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	4.0	25	
250 mA ≤ I_O ≤ 750 mA		—	1.5	15	
Ripple Rejection	RR				dB
8.0 V ≤ V_{in} ≤ 18 V, f = 120 Hz		70	80	—	
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	W
Average Temperature Coefficient of Output Voltage	TCV_O				mV°C
I_O = 5.0 mA		—	0.06	—	
Output Noise Voltage (T_J = +25°C)	V_n				μV
10 Hz ≤ f ≤ 100 kHz		—	75	—	
Dropout Voltage (T_J = +25°C)	$V_{in}–V_O$				V
I_O = 1.0 mA		—	2.0	—	
Bias Current (T_J = +25°C)	I_B	—	3.5	8.0	mA
Bias Current Change	ΔI_B				mA
7.0 V ≤ V_{in} ≤ 25 V, I_O = 500 mA		—	0.7	1.3	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} ≤ 10 V		—	0.03	0.5	
Short Circuit Output Current (T_J = +25°C)	I_{SC}				mA
V_{in} = 35 V		—	200	—	
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

NOTE: 1. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	TL780–12C			Unit
		Min	Typ	Max	
Output Voltage	V_O				V
5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W, 14.5 ≤ V_{in} ≤ 27 V					
T_J = +25°C		11.88	12	12.12	
0°C ≤ T_J ≤ +125°C		11.76	—	12.24	
Line Regulation (T_J = +25°C)	Reg_{line}				mV
14.5 V ≤ V_{in} ≤ 30		—	1.2	12	
16 V ≤ V_{in} ≤ 22		—	1.2	12	

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	TL780–12C			Unit
		Min	Typ	Max	
Load Regulation (T_J = +25°C) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 6.5 2.5	 60 36	mV
Ripple Rejection 15 V ≤ V_{in} ≤ 25 V, f = 120 Hz	RR	 65	 77	 —	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	W
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	 —	 0.15	 —	mV°C
Output Noise Voltage (T_J = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	 —	 180	 —	μV
Dropout Voltage (T_J = +25°C) I_O = 1.0 mA	V_{in}–V_O	 —	 2.0	 —	V
Bias Current (T_J = +25°C)	I_B	—	3.5	8.0	mA
Bias Current Change 14.5 V ≤ V_{in} ≤ 30 V, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} ≤ 19 V	ΔI_B	 — —	 0.4 0.03	 1.3 0.5	mA
Short Circuit Output Current (T_J = +25°C) V_{in} = 35 V	I_{SC}	 —	 200	 —	mA
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	TL780–15C			Unit
		Min	Typ	Max	
Output Voltage 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W, 17.5 V ≤ V_{in} ≤ 30 V T_J = +25°C 0°C ≤ T_J ≤ +125°C	V_O	 14.85 14.70	 15 —	 15.15 15.30	V
Line Regulation (T_J = +25°C) 17.5 V ≤ V_{in} ≤ 30 V 20 V ≤ V_{in} ≤ 26 V	Reg_{line}	 — —	 1.5 1.5	 15 15	mV
Load Regulation (T_J = +25°C) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 7.0 2.5	 75 45	mV
Ripple Rejection 18.5 V ≤ V_{in} ≤ 28.5 V, f = 120 Hz	RR	 60	 75	 —	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	W
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	 —	 0.18	 —	mV°C
Output Noise Voltage (T_J = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	 —	 225	 —	μV
Dropout Voltage (T_J = +25°C) I_O = 1.0 A	V_{in}–V_O	 —	 2.0	 —	V
Bias Current (T_J = +25°C)	I_B	—	3.6	8.0	mA
Bias Current Change 17.5 V ≤ V_{in} ≤ 30 V, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} ≤ 23 V	ΔI_B	 — —	 0.4 0.02	 1.3 0.5	mA
Short Circuit Output Current (T_J = +25°C) V_{in} = 35 V	I_{SC}	 —	 200	 —	mA
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

NOTE: 1. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical TL780–05C to a 10 W input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical TL780–05C to a 15 W load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

Figure 1. Line and Thermal Regulation

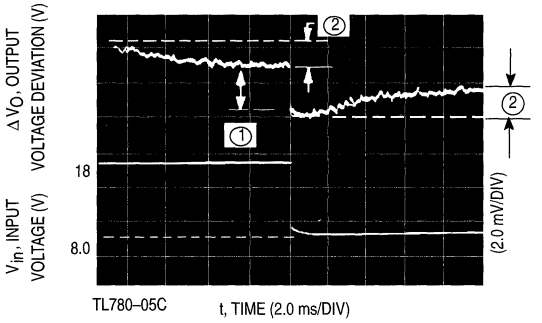


Figure 2. Load and Thermal Regulation

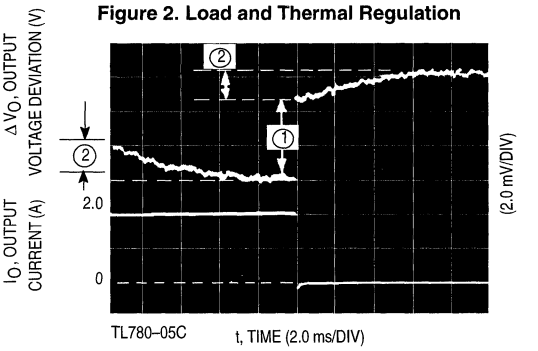


Figure 3. Temperature Stability

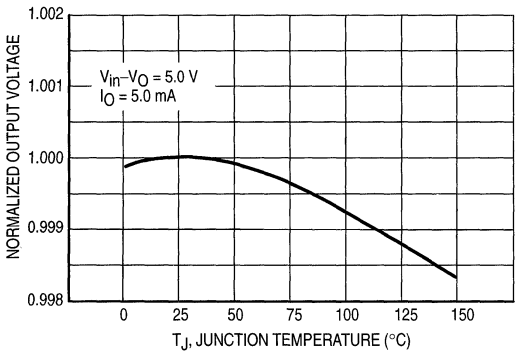


Figure 4. Output Impedance

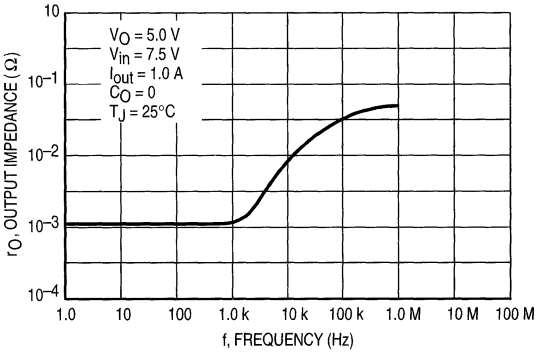


Figure 5. Ripple Rejection versus Frequency

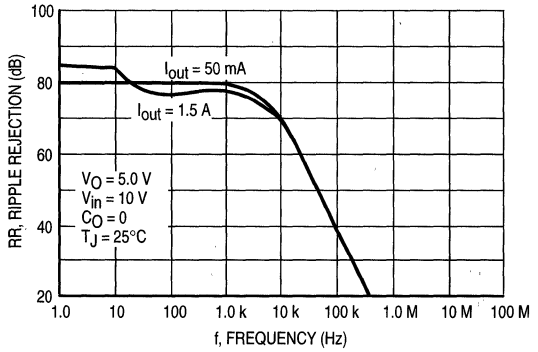


Figure 6. Ripple Rejection versus Output Current

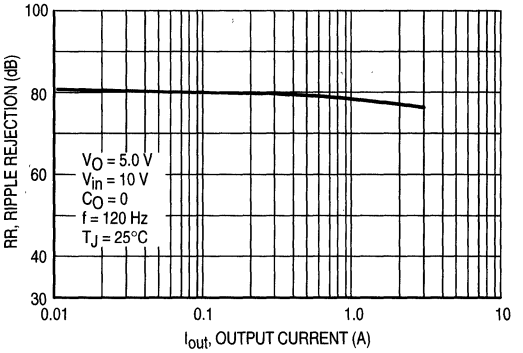


Figure 7. Bias Current versus Input Voltage

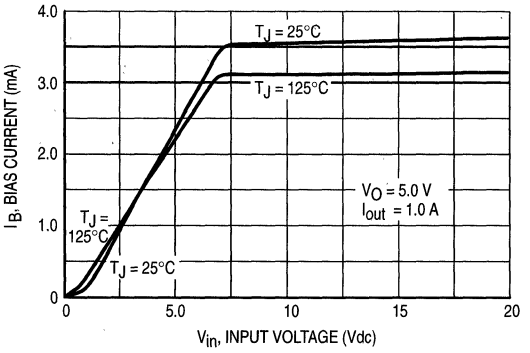


Figure 8. Bias Current versus Output Current

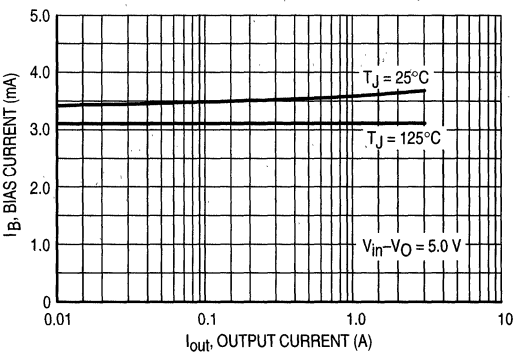


Figure 9. Dropout Voltage

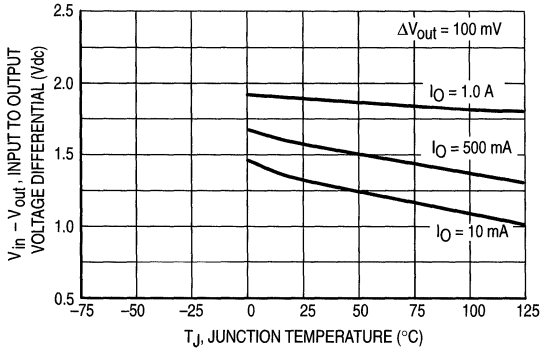


Figure 10. Peak Output Current

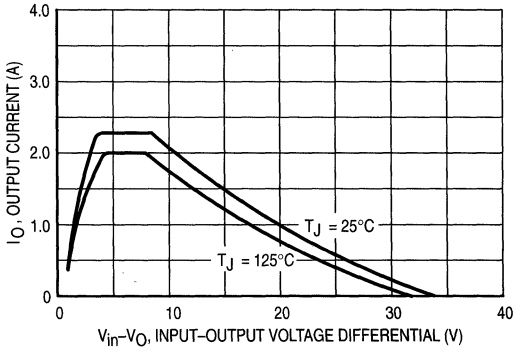


Figure 11. Line Transient Response

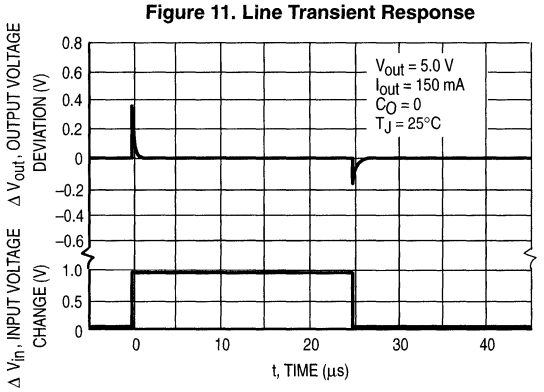


Figure 12. Load Transient Response

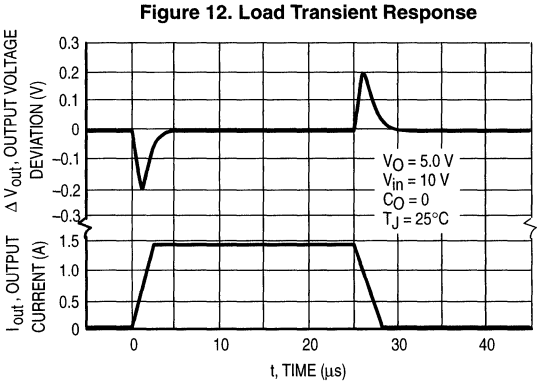
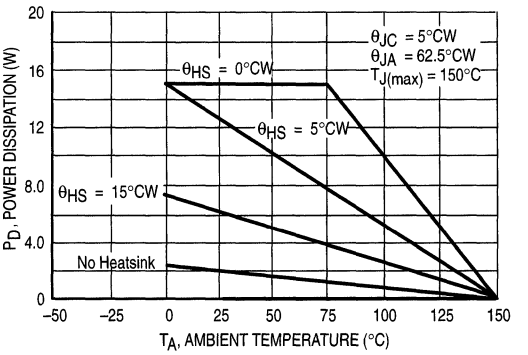


Figure 13. Worst Case Power Dissipation versus Ambient Temperature



UC3842A, 43A
UC2842A, 43A

3

High Performance Current Mode Controllers

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

The UC3842A, UC3843A series of high performance fixed frequency current mode controllers are specifically designed for off–line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

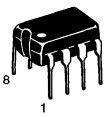
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

These devices are available in an 8–pin dual–in–line plastic package as well as the 14–pin plastic surface mount (SO–14). The SO–14 package has separate power and ground pins for the totem pole output stage.

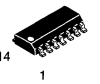
The UCX842A has UYLO thresholds of 16 V (on) and 10 V (off), ideally suited for off–line converters. The UCX843A is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator Discharge Current for Precise Duty Cycle Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- Direct Interface with Motorola SENSEFET Products

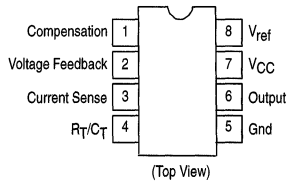
N SUFFIX
PLASTIC PACKAGE
CASE 626



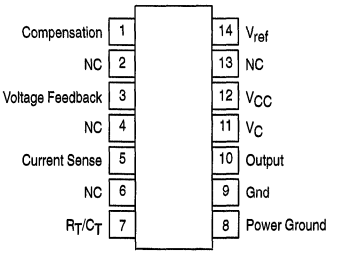
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



PIN CONNECTIONS

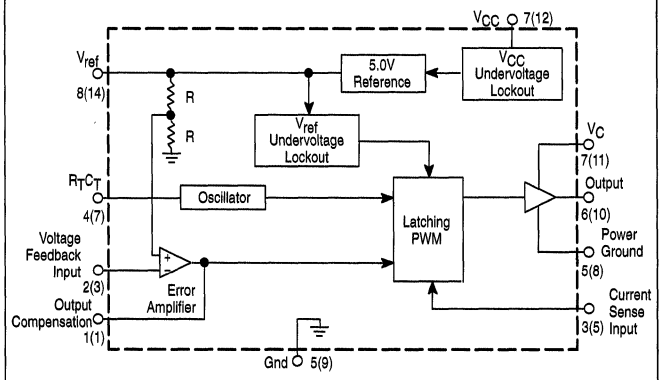


(Top View)



(Top View)

Simplified Block Diagram



Pin numbers in parenthesis are for the D suffix SO–14 package.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
UC3842AD	T_A = 0° to +70°C	SO–14
UC3843AD		SO–14
UC3842AN		Plastic
UC3843AN		Plastic
UC2842AD	T_A = – 25° to +85°C	SO–14
UC2843AD		SO–14
UC2842AN		Plastic
UC2843AN		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	– 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air N Suffix, Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature UC3842A, UC3843A UC2842A, UC2843A	T_A	 0 to + 70 – 25 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XA			UC384XA			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	–	2.0	20	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	25	–	3.0	25	mV
Temperature Stability	T_S	–	0.2	–	–	0.2	–	mV/°C
Total Output Variation over Line, Load, Temperature	V_{ref}	4.9	–	5.1	4.82	–	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	–	50	–	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	– 30	– 85	– 180	– 30	– 85	– 180	mA
OSCILLATOR SECTION								
Frequency T_J = 25°C T_A = T_{low} to T_{high}	f_{osc}	 47 46	 52 –	 57 60	 47 46	 52 –	 57 60	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	–	0.2	1.0	%
Frequency Change with Temperature T_A = T_{low} to T_{high}	$\Delta f_{osc}/\Delta T$	–	5.0	–	–	5.0	–	%
Oscillator Voltage Swing (Peak–to–Peak)	V_{osc}	–	1.6	–	–	1.6	–	V
Discharge Current (V_{osc} = 2.0 V) T_J = 25°C T_A = T_{low} to T_{high}	I_{dischg}	 7.5 7.2	 8.4 –	 9.3 9.5	 7.5 7.2	 8.4 –	 9.3 9.5	mA

NOTES: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible
T_{low} = 0°C for UC3842A, UC3843A; –25°C for UC2842A, UC2843A
T_{high} = +70°C for UC3842A, UC3843A; +85°C for UC2842A, UC2843A

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XA Min	UC284XA Typ	UC284XA Max	UC384XA Min	UC384XA Typ	UC384XA Max	Unit
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 2.7 V)	I_{IB}	–	–0.1	–1.0	–	–0.1	–2.0	µA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	–	2.0	12	–	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	–0.5	–1.0	–	–0.5	–1.0	–	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}	–	0.8	1.1	–	0.8	1.1	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V	2.85	3.0	3.15	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	0.9	1.0	1.1	V
Power Supply Rejection Ratio	PSRR							dB
V_{CC} = 12 to 25 V (Note 4)		–	70	–	–	70	–	
Input Bias Current	I_{IB}	–	–2.0	–10	–	–2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(in/out)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{Sink} = 200 mA)		–	1.6	2.2	–	1.6	2.2	
High State (I_{Sink} = 20 mA)	V_{OH}	13	13.5	–	13	13.5	–	
(I_{Sink} = 200 mA)		12	13.4	–	12	13.4	–	
Output Voltage with UVLO Activated	$V_{OL(UVLO)}$							V
V_{CC} = 6.0 V, I_{Sink} = 1.0 mA		–	0.1	1.1	–	0.1	1.1	
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold	V_{th}							V
UCX842A		15	16	17	14.5	16	17.5	
UCX843A		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$							V
UCX842A		9.0	10	11	8.5	10	11.5	
UCX843A		7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION								
Duty Cycle								%
Maximum	DC_{max}	94	96	–	94	96	–	
Minimum	DC_{min}	–	–	0	–	–	0	
TOTAL DEVICE								
Power Supply Current (Note 2)	I_{CC}							mA
Startup:								
(V_{CC} = 6.5 V for UCX843A,								
14 V for UCX842A) Operating		–	0.5	1.0	–	0.5	1.0	
		–	12	17	–	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible
   T_{low} = 0°C for UC3842A, UC3843A; –25°C for UC2842A, UC2843A
   T_{high} = +70°C for UC3842A, UC3843A; +85°C for UC2842A, UC2843A

4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

Figure 1. Timing Resistor versus Oscillator Frequency

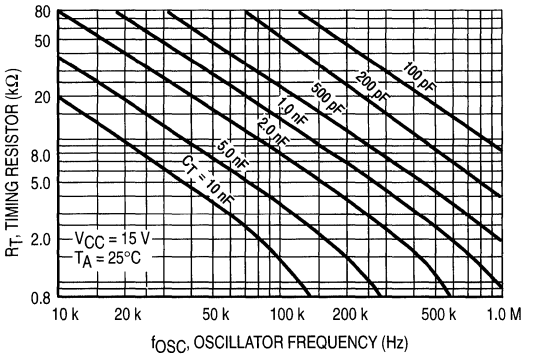


Figure 2. Output Deadtime versus Oscillator Frequency

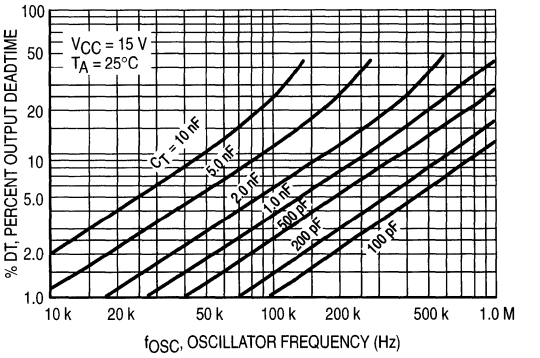


Figure 3. Oscillator Discharge Current versus Temperature

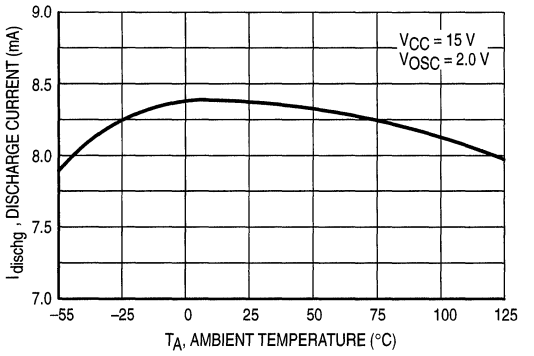


Figure 4. Maximum Output Duty Cycle versus Timing Resistor

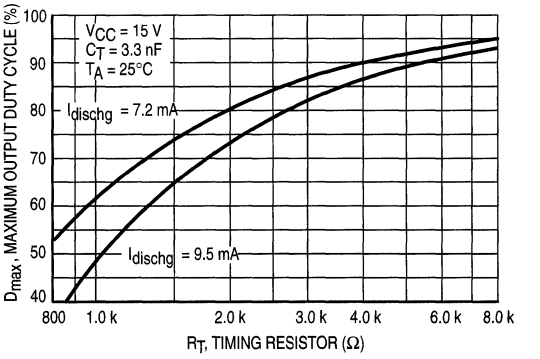


Figure 5. Error Amp Small Signal Transient Response

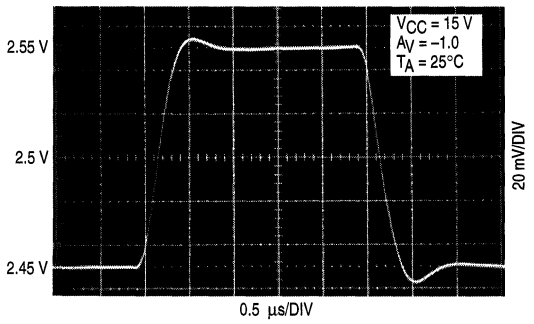
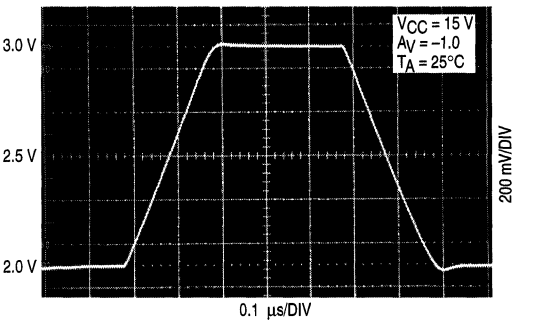


Figure 6. Error Amp Large Signal Transient Response



3

Figure 7. Error Amp Open Loop Gain and Phase versus Frequency

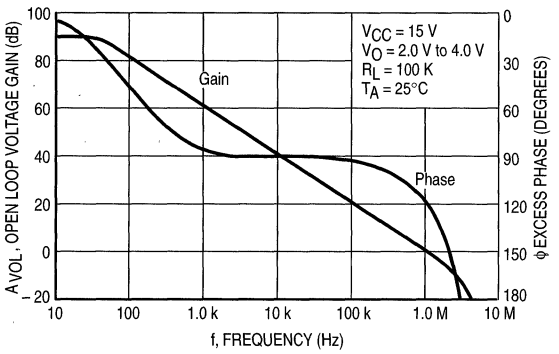


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

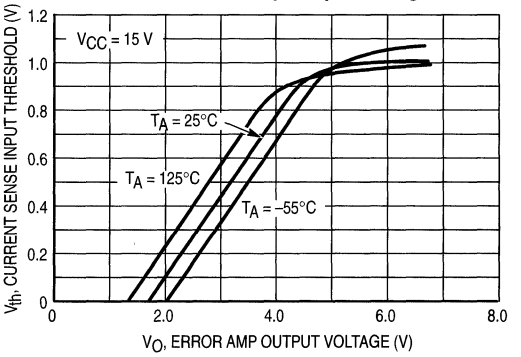


Figure 9. Reference Voltage Change versus Source Current

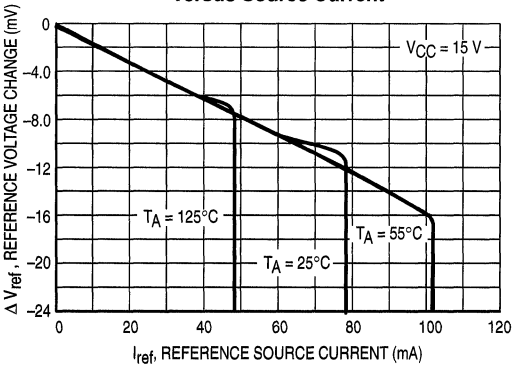


Figure 10. Reference Short Circuit Current versus Temperature

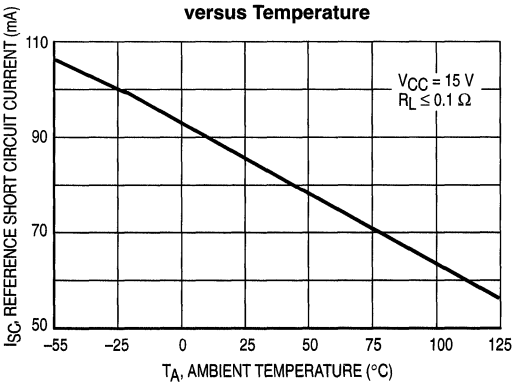


Figure 11. Reference Load Regulation

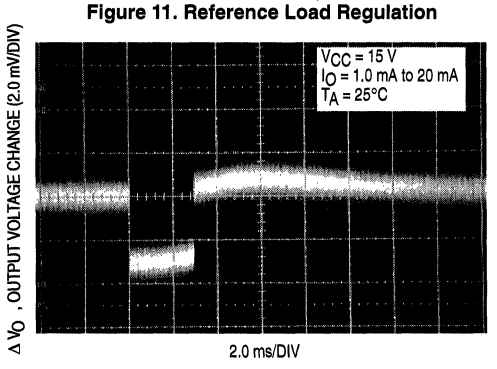


Figure 12. Reference Line Regulation

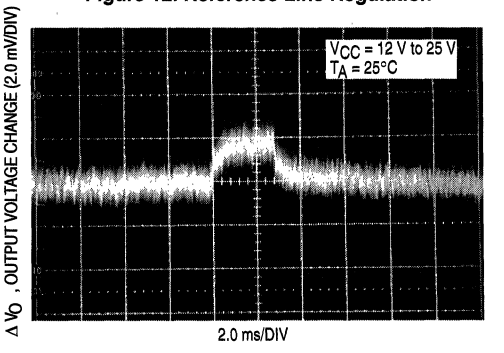


Figure 13. Output Saturation Voltage versus Load Current

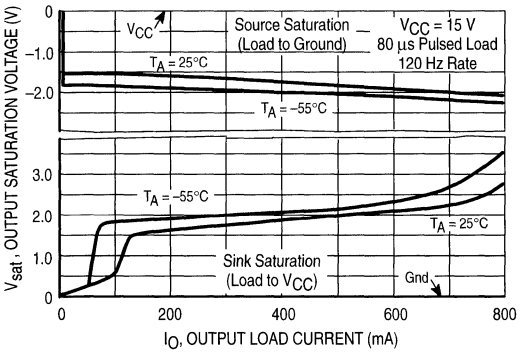


Figure 14. Output Waveform

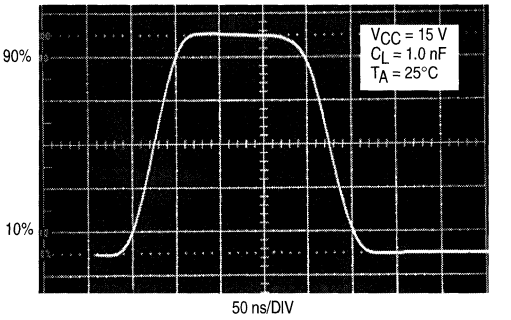


Figure 15. Output Cross Conduction

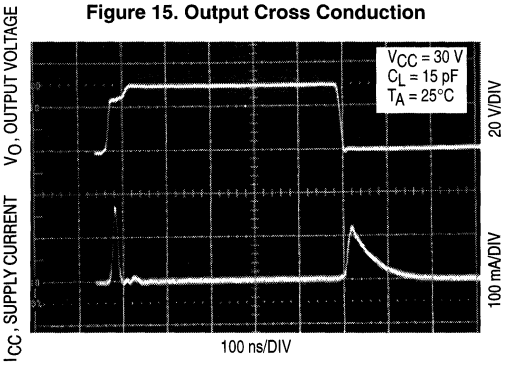


Figure 16. Supply Current versus Supply Voltatage

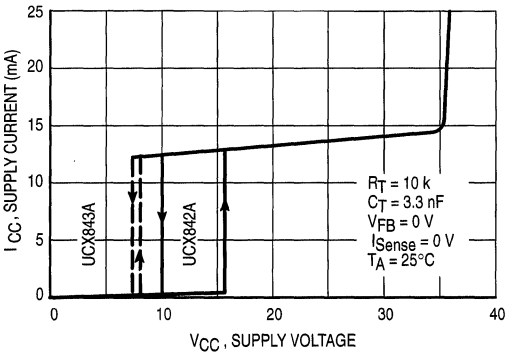
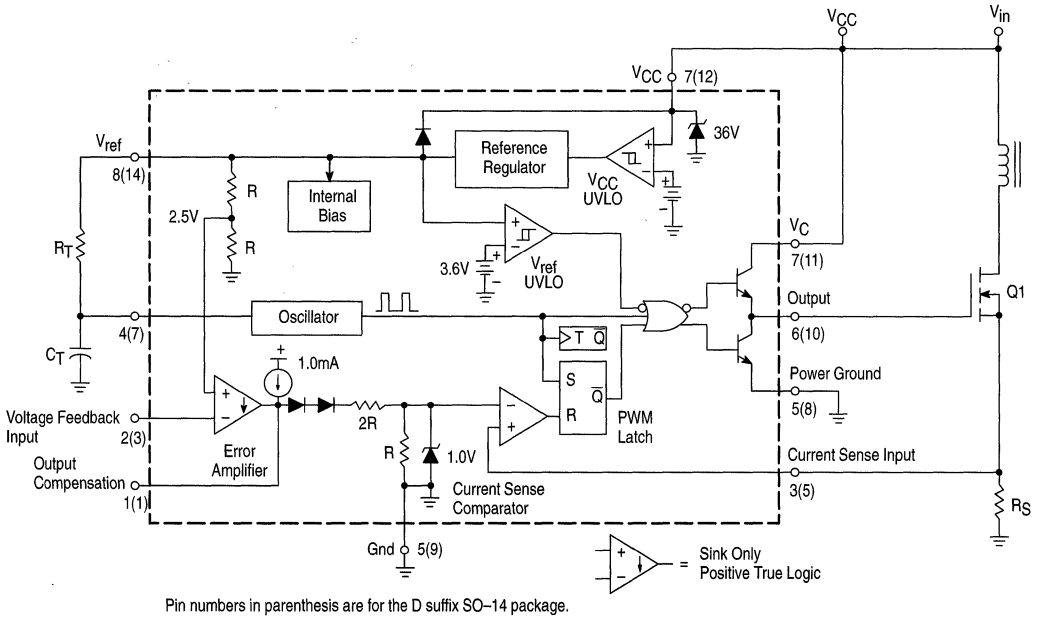
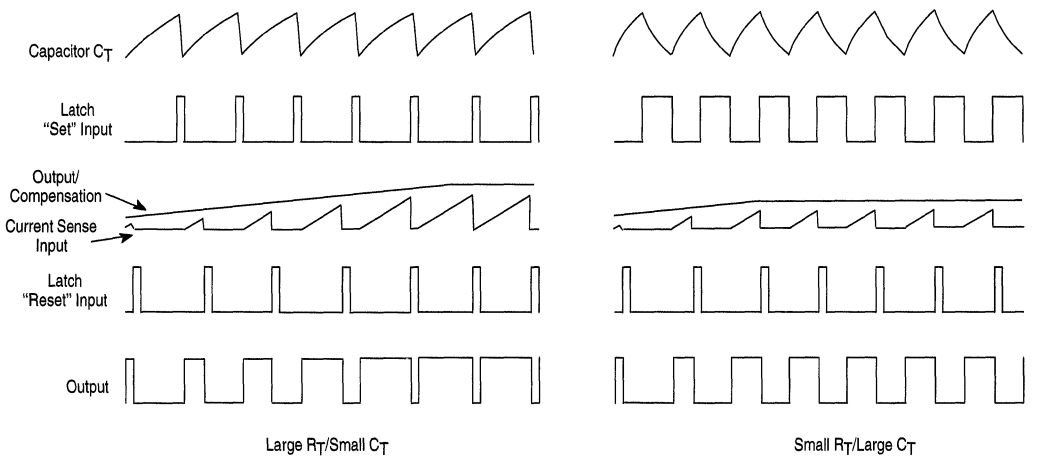


Figure 17. Representative Block Diagram



Pin numbers in parenthesis are for the D suffix SO–14 package.

Figure 18. Timing Diagram



OPERATING DESCRIPTION

The UC3842A, UC3843A series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 17.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates and internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated, and the discharge current is trimmed and guaranteed to within ± 10% at T_J = 25°C. These internal circuit refinements minimize variations of oscillator frequency and maximum output duty cycle. The results are shown in Figures 3 and 4.

In many noise sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 20. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 21. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 7). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 µA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provide for external loop compensation (Figure 30). The output voltage is offset by two diode drops (≈ 1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 23, 24). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3842A, UC3843A operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin1). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 22. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 26.

PIN FUNCTION DESCRIPTION

Pin		Function	Description
8–Pin	14–Pin		
1	1	Compensation	This pin is Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5	–	Gnd	This pin is the combined control circuitry and power ground (8–pin package only).
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
–	8	Power Ground	This pin is a separate power ground return (14–pin package only) that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
–	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin (14–pin package only). With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
–	9	Gnd	This pin is the control circuitry ground return (14–pin package only) and is connected back to the power source ground.
–	2,4,6,13	NC	No connection (14–pin package only). These pins are not internally connected.

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX842A, and 8.4 V/7.6 V for the UCX843A. The V_{ref} comparator upper and lower thresholds are 3.6V/3.4 V. The large hysteresis and low startup current of the UCX842A makes it ideally suited in off–line converter applications where efficient bootstrap startup techniques are required (Figure 33). The UCX843A is intended for lower voltage dc to dc converter applications. A 36 V zener is connected as a shunt regulator form V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for the UCX842A is 11 V and 8.2 V for the UCX843A.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull–down resistor.

The SO–14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater that 20 V. Figure 25 shows proper power and control ground connections in a current sensing power MOSFET application.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284XA, and ± 2.0% on the UC384XA. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

DESIGN CONSIDERATIONS

Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High Frequency circuit layout techniques are imperative to prevent pulsewidth jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low–current signal and high–current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulators closed–loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 19A shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2 until the next oscillator cycle. The unstable condition can be shown if a pertubation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn–on (t_2) is increased by ΔI + ΔI m2/m1. The minimum current at the next cycle (t_3) decreases to (ΔI + ΔI m_2/m_1) (m_2/m_1). This pertubation is multiplied by $m_2.m_1$ on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn–on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Figure 19B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI pertubation will decrease to zero on succeeding cycles. This compensation ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 32).

Figure 19. Continuous Current Waveforms

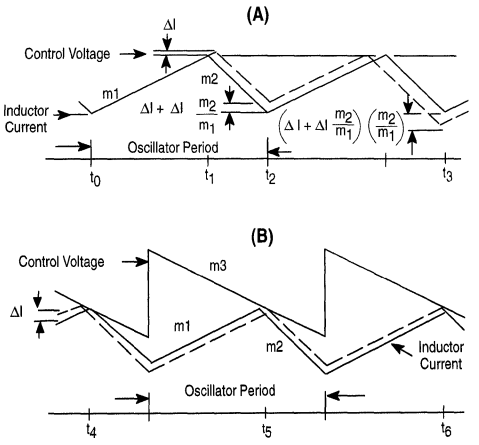
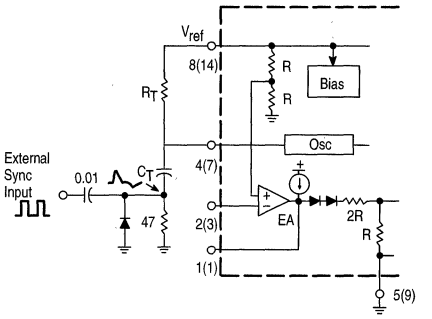
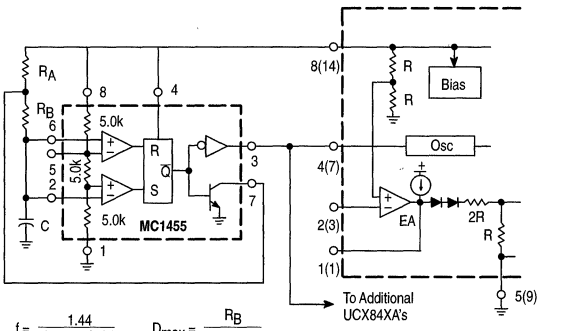


Figure 20. External Clock Synchronization



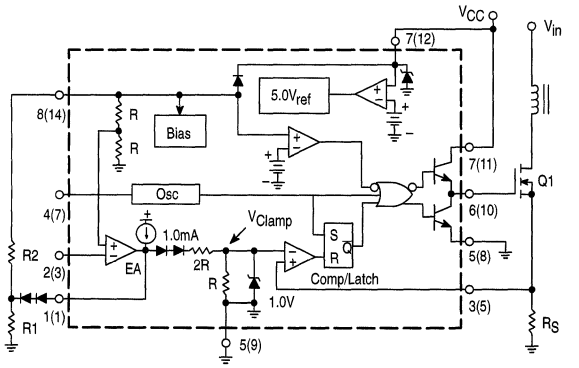
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of CT to go more than 300 mV below ground.

Figure 21. External Duty Cycle Clamp and Multi Unit Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

Figure 22. Adjustable Reduction of Clamp Level



$$V_{Clamp} = \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{-3}\left(\frac{R_1 R_2}{R_1 + R_2}\right) \qquad I_{pk(max)} = \frac{V_{Clamp}}{RS}$$

Where: $0 \le V_{Clamp} \le 1.0\ V$

Figure 23. Soft–Start Circuit

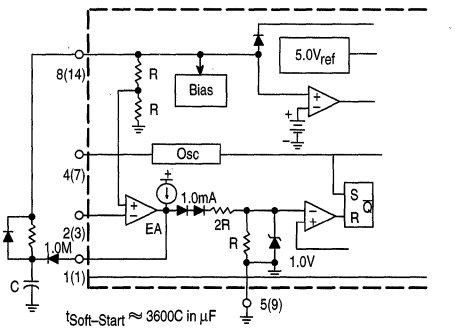
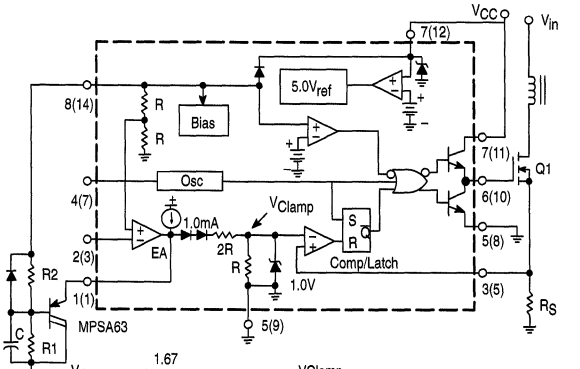


Figure 24. Adjustable Buffered Reduction of Clamp Level with Soft–Start

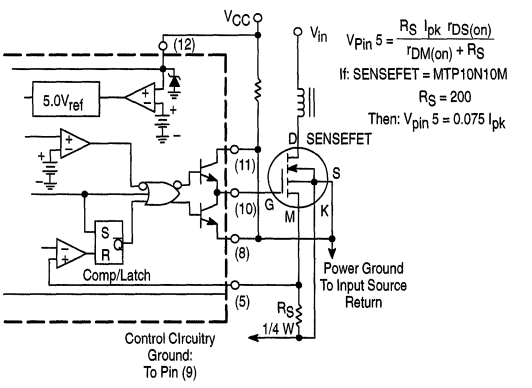


$$V_{Clamp} = \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} \qquad I_{pk(max)} = \frac{V_{Clamp}}{RS}$$

Where: $0 \le V_{Clamp} \le 1.0\ V$

$$t_{Softstart} = -\ln\left[1 - \frac{V_C}{3V_{Clamp}}\right] C\,\frac{R_1 R_2}{R_1 + R_2}$$

Figure 25. Current Sensing Power MOSFET



$$V_{Pin\,5} = \frac{R_S\, I_{pk}\, r_{DS(on)}}{r_{DM(on)} + R_S}$$

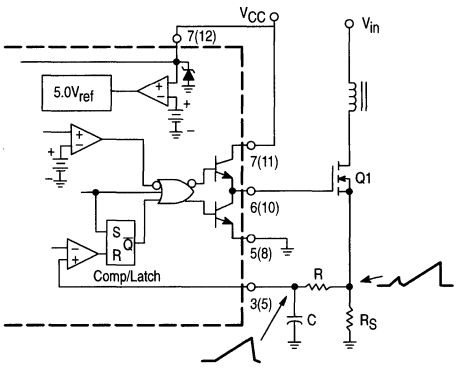
If: SENSEFET = MTP10N10M

$R_S = 200$

Then: $V_{pin\,5} = 0.075\, I_{pk}$

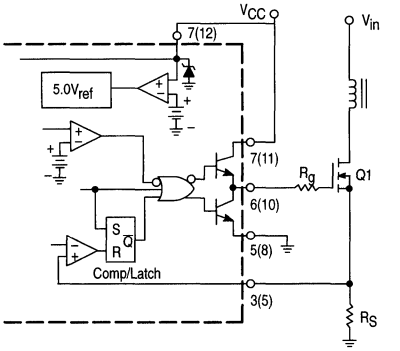
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 22 and 24.

Figure 26. Current Waveform Spike Suppression



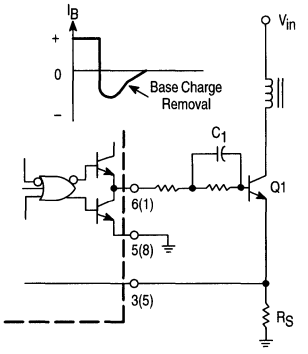
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 27. MOSFET Parasitic Oscillations



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit.

Figure 28. Bipolar Transistor Drive



The totem–pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 29. Isolated MOSFET Drive

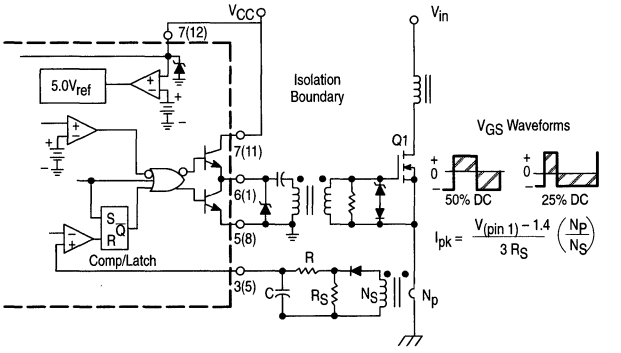
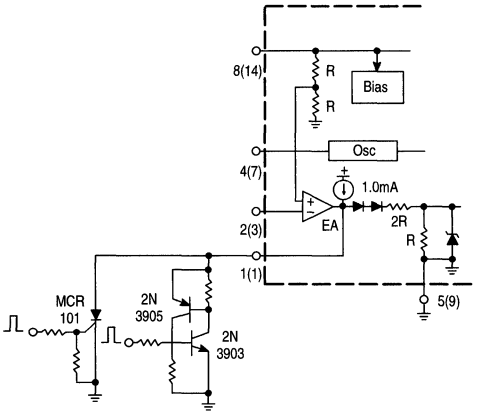
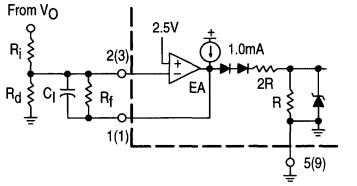


Figure 30. Latched Shutdown

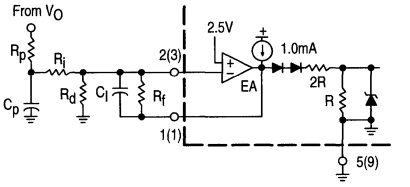


The MCR101 SCR must be selected for a holding of less than 0.5 mA at $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 31. Error Amplifier Compensation

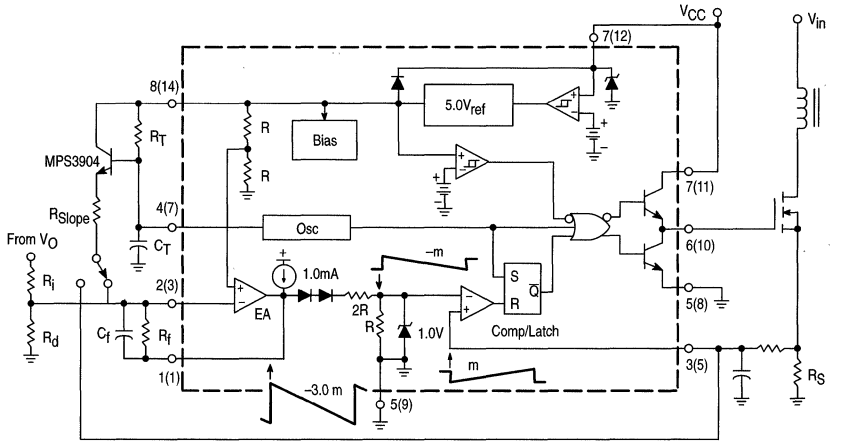


Error Amp compensation circuit for stabilizing any current–mode topology except for boost and flyback converters operating with continuous inductor current.



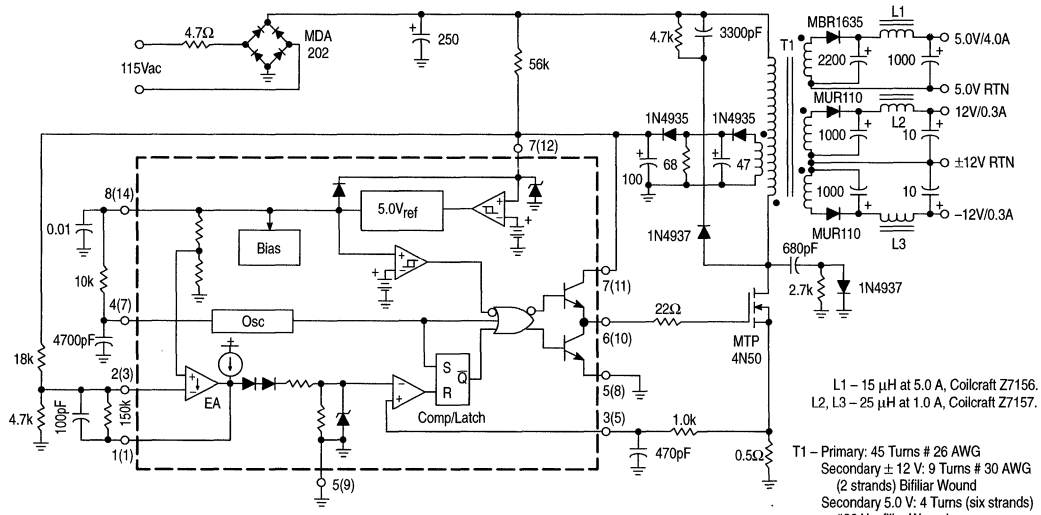
Error Amp compensation circuit for stabilizing current–mode boost and flyback topologies operating with continuous inductor current.

Figure 32. Slope Compensation



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

Figure 33. 27 Watt Off–Line Flyback Regulator



L1 – 15 μH at 5.0 A, Coilcraft Z7156.
L2, L3 – 25 μH at 1.0 A, Coilcraft Z7157.

T1 – Primary: 45 Turns # 26 AWG
Secondary ± 12 V: 9 Turns # 30 AWG
(2 strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands)
#26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG
(2 strands) Bifiliar Wound
Core: Ferroxcube EC35–3C8
Bobbin: Ferroxcube EC35PCB1
Gap ≈ 0.01" for a primary inductance of 1.0 mH

Test	Conditions	Results
Line Regulation: 5.0 V	V_{in} = 95 Vac to 130 Vac	Δ = 50 mV or ± 0.5%
± 12 V		Δ = 24 mV or ± 0.1%
Load Regulation: 5.0 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A	Δ = 300 mV or ± 3.0%
± 12 V	V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 60 mV or ± 0.25%
Output Ripple: 5.0 V	V_{in} = 115 Vac	40 mV_{pp}
± 12 V		80 mV_{pp}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted.

MOTOROLA

UC3842B, 43B
UC2842B, 43B

3

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

High Performance Current Mode Controllers

The UC3842B, UC3843B series are high performance fixed frequency current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost–effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

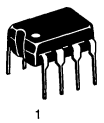
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

These devices are available in an 8–pin dual–in–line and surface mount (SO–8) plastic package as well as the 14–pin plastic surface mount (SO–14). The SO–14 package has separate power and ground pins for the totem pole output stage.

The UCX842B has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off–line converters. The UCX843B is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

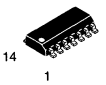
- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current

N SUFFIX
PLASTIC PACKAGE
CASE 626

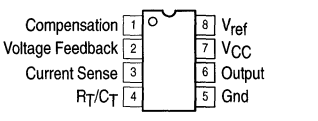


D1 SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

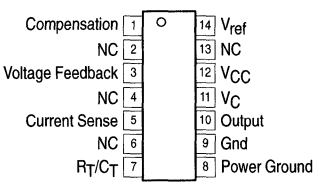
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



PIN CONNECTIONS

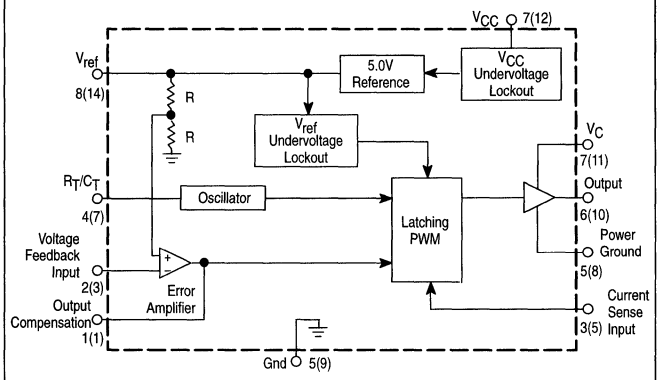


(Top View)



(Top View)

Simplified Block Diagram



Pin numbers in parenthesis are for the D suffix SO–14 package.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
UC384XBD	T_A = 0° to +70°C	SO–14
UC384XBD1		SO–8
UC384XBN		Plastic
UC284XBD	T_A = – 25° to +85°C	SO–14
UC284XBD1		SO–8
UC284XBN		Plastic
UC384XBVD	T_A = –40° to +105°C	SO–14
UC384XBVD1		SO–8
UC384XBVN		Plastic

X indicates either a 2 or 3 to define specific device part numbers.

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	– 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package, SO–14 Case 751A			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	145	°C/W
D1 Suffix, Plastic Package, SO–8 Case 751			
Maximum Power Dissipation @ T_A = 25°C	P_D	702	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
N Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
UC3842B, UC3843B		0 to + 70	
UC2842B, UC2843B		– 25 to + 85	
UC3842BV, UC3843BV		–40 to +105	
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	–	2.0	20	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	25	–	3.0	25	mV
Temperature Stability	T_S	–	0.2	–	–	0.2	–	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	–	5.1	4.82	–	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	–	50	–	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	– 30	– 85	–180	– 30	– 85	–180	mA
OSCILLATOR SECTION								
Frequency	f_{OSC}							kHz
T_J = 25°C		49	52	55	49	52	55	
$T_A = T_{low}$ to T_{high}		48	–	56	48	–	56	
T_J = 25°C (R_T = 6.2 k, C_T = 1.0 nF)		225	250	275	225	250	275	
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	–	0.2	1.0	–	0.2	1.0	%
Frequency Change with Temperature $T_A = T_{low}$ to T_{high}	$\Delta f_{OSC}/\Delta T$	–	1.0	–	–	0.5	–	%
Oscillator Voltage Swing (Peak–to–Peak)	V_{OSC}	–	1.6	–	–	1.6	–	V
Discharge Current (V_{OSC} = 2.0 V)	I_{dischg}							mA
T_J = 25°C		7.8	8.3	8.8	7.8	8.3	8.8	
$T_A = T_{low}$ to T_{high} (UC284XB, UC384XB)		7.5	–	8.8	7.6	–	8.8	
(UC384XBV)		–	–	–	7.2	–	8.8	

NOTES: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3842B, UC3843B; –25°C for UC2842B, UC2843B; –40°C for UC3842BV, UC3843BV
T_{high} = +70°C for UC3842B, UC3843B; +85°C for UC2842B, UC2843B; +105°C for UC3842BV, UC3843BV

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	–1.0	–	– 0.1	– 2.0	µA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	–	2.0	12	–	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	– 0.5	–1.0	–	– 0.5	–1.0	–	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}							
(UC284XB, UC384XB)		–	0.8	1.1	–	0.8	1.1	
(UC384XBV)		–	–	–	–	0.8	1.2	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V							V/V
(UC284XB, UC384XB)		2.85	3.0	3.15	2.85	3.0	3.15	
(UC384XBV)		–	–	–	2.85	3.0	3.25	
Maximum Current Sense Input Threshold (Note 4)	V_{th}							V
(UC284XB, UC384XB)		0.9	1.0	1.1	0.9	1.0	1.1	
(UC384XBV)		–	–	–	0.85	1.0	1.1	
Power Supply Rejection Ratio	PSRR	–	70	–	–	70	–	dB
V_{CC} = 12 V to 25 V, Note 4								
Input Bias Current	I_{IB}	–	– 2.0	–10	–	– 2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(In/Out)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{Sink} = 200 mA) (UC284XB, UC384XB)		–	1.6	2.2	–	1.6	2.2	
(UC384XBV)		–	–	–	–	1.6	2.3	
High State (I_{Source} = 20 mA) (UC284XB, UC384XB)	V_{OH}	13	13.5	–	13	13.5	–	
(UC384XBV)		–	–	–	12.9	13.5	–	
(I_{Source} = 200 mA)		12	13.4	–	12	13.4	–	
Output Voltage with UVLO Activated	$V_{OL(UVLO)}$	–	0.1	1.1	–	0.1	1.1	V
V_{CC} = 6.0 V, I_{Sink} = 1.0 mA								
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold (V_{CC})	V_{th}							V
UCX842B, BV		15	16	17	14.5	16	17.5	
UCX843B, BV		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn–On (V_{CC})	$V_{CC(min)}$							V
UCX842B, BV		9.0	10	11	8.5	10	11.5	
UCX843B, BV		7.0	7.6	8.2	7.0	7.6	8.2	

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for UC3842B, UC3843B; T_{high} = +70°C for UC3842B, UC3843B
   –25°C for UC2842B, UC2843B; +85°C for UC2842B, UC2843B
   –40°C for UC3842BV, UC3843BV; +105°C for UC3842BV, UC3843BV

4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XB Min	UC284XB Typ	UC284XB Max	UC384XB, BV Min	UC384XB, BV Typ	UC384XB, BV Max	Unit
PWM SECTION								
Duty Cycle								%
Maximum (UC284XB, UC384XB)	$DC_{(max)}$	94	96	–	94	96	–	
(UC384XBV)		–	–	–	93	96	–	
Minimum	$DC_{(min)}$	–	–	0	–	–	0	
TOTAL DEVICE								
Power Supply Current	$I_{CC} + I_C$							mA
Startup (V_{CC} = 6.5 V for UCX843B, (V_{CC} 14 V for UCX842B, BV)		–	0.3	0.5	–	0.3	0.5	
Operating (Note 2)		–	12	17	–	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3842B, UC3843B; –25°C for UC2842B, UC2843B; –40°C for UC3842BV, UC3843BV
T_{high} = +70°C for UC3842B, UC3843B; +85°C for UC2842B, UC2843B; +105°C for UC3842BV, UC3843BV

Figure 1. Timing Resistor versus Oscillator Frequency

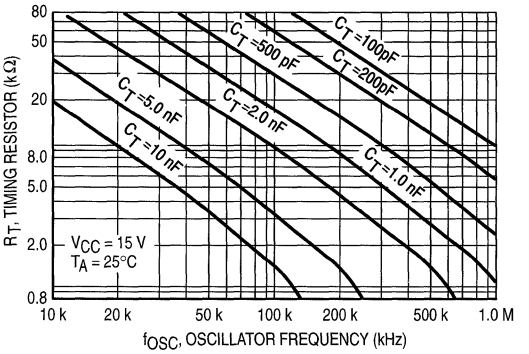


Figure 2. Output Deadtime versus Oscillator Frequency

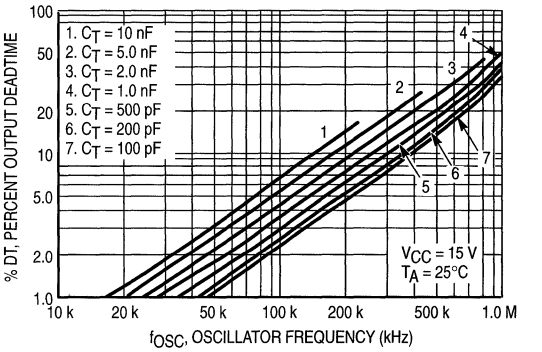


Figure 3. Oscillator Discharge Current versus Temperature

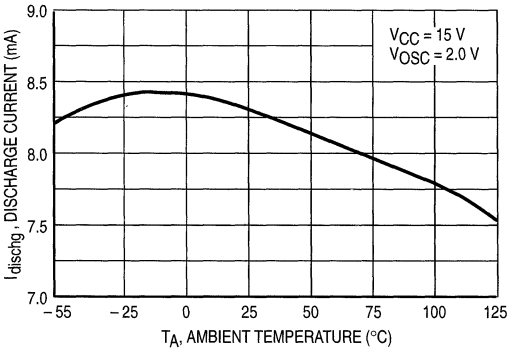


Figure 4. Maximum Output Duty Cycle versus Timing Resistor

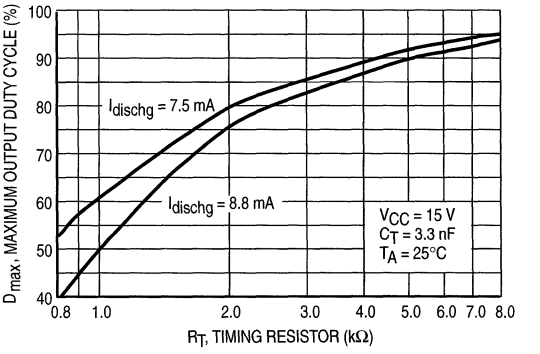


Figure 5. Error Amp Small Signal Transient Response

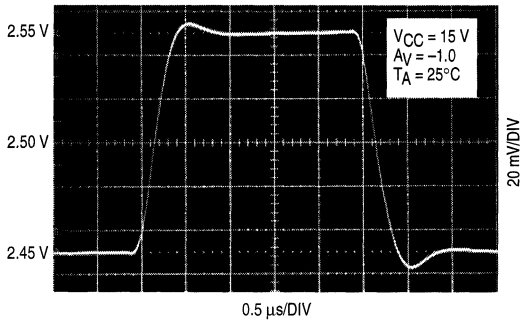


Figure 6. Error Amp Large Signal Transient Response

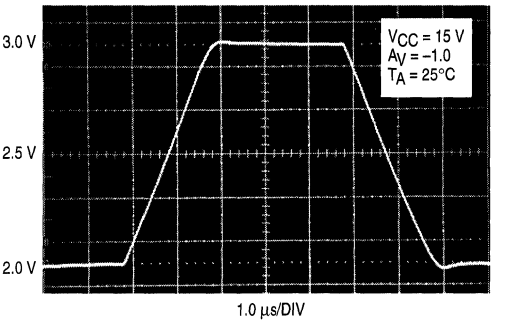


Figure 7. Error Amp Open Loop Gain and Phase versus Frequency

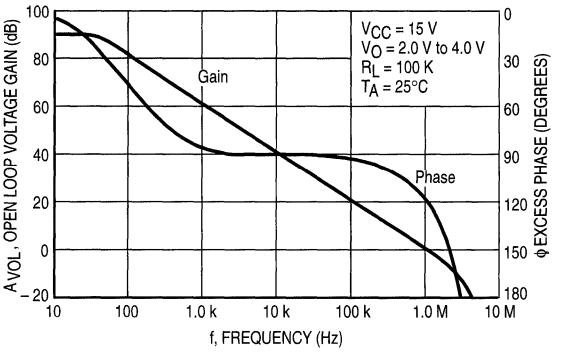


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

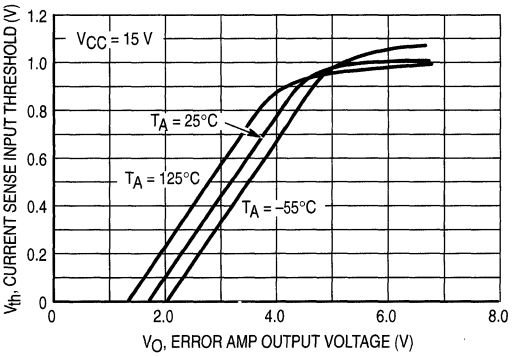


Figure 9. Reference Voltage Change versus Source Current

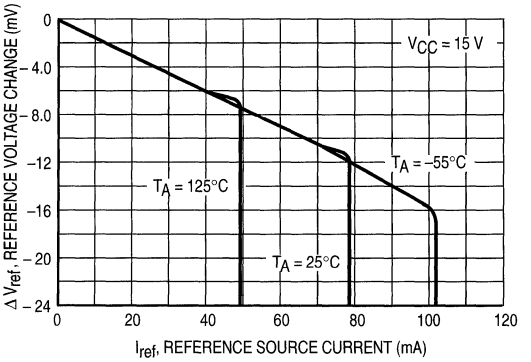
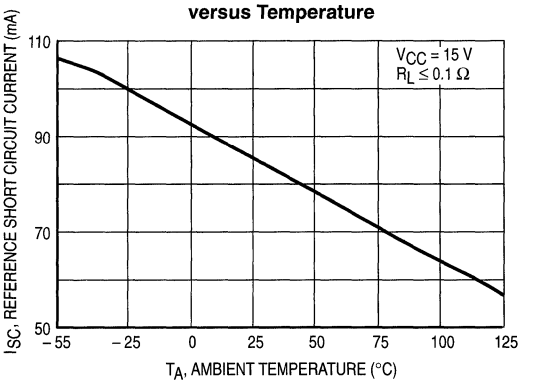


Figure 10. Reference Short Circuit Current versus Temperature



3

Figure 11. Reference Load Regulation

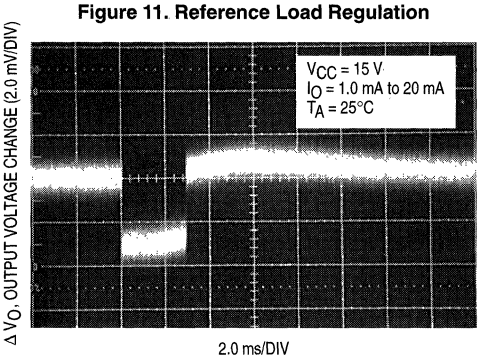


Figure 12. Reference Line Regulation

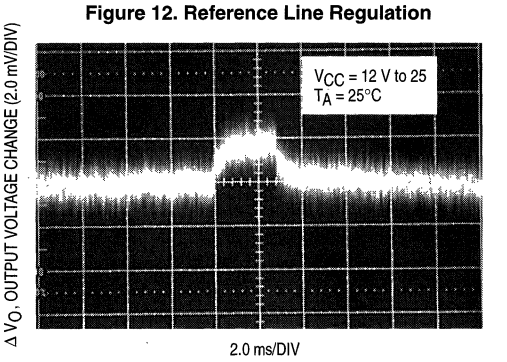


Figure 13. Output Saturation Voltage versus Load Current

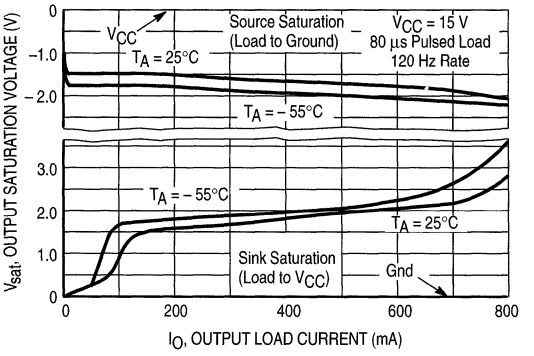


Figure 14. Output Waveform

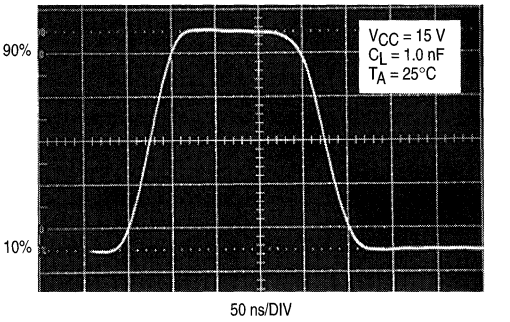


Figure 15. Output Cross Conduction

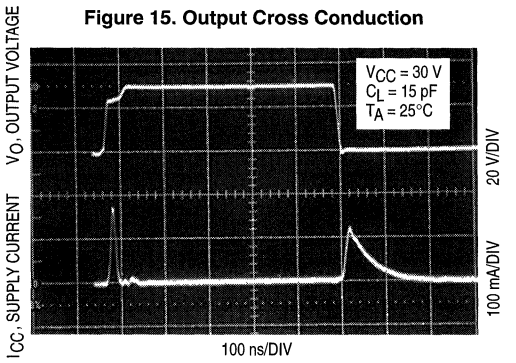
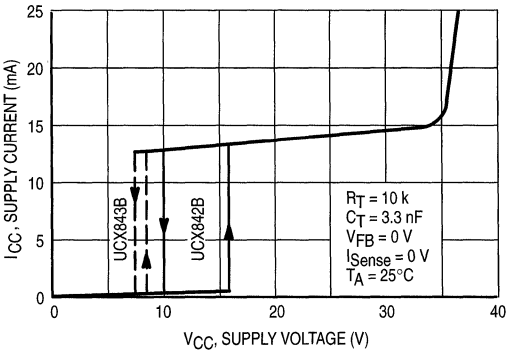


Figure 16. Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin		Function	Description
8–Pin	14–Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5		Gnd	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	Gnd	This pin is the control circuitry ground return and is connected back to the power source ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

OPERATING DESCRIPTION

The UC3842B, UC3843B series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost–effective solution with minimal external components. A representative block diagram is shown in Figure 17.

3

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated to within ±6% at 50 kHz. Also because of industry trends moving the UC384X into higher and higher frequency applications, the UC384XB is guaranteed to within ±10% at 250 kHz. These internal circuit refinements minimize variations of oscillator frequency and maximum output duty cycle. The results are shown in Figures 3 and 4.

In many noise–sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 20. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. A method for multi–unit synchronization is shown in Figure 21. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 7). The non–inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 µA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 31). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the non–inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 23, 24). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3842B, UC3843B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground–referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 22. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 26).

Figure 17. Representative Block Diagram

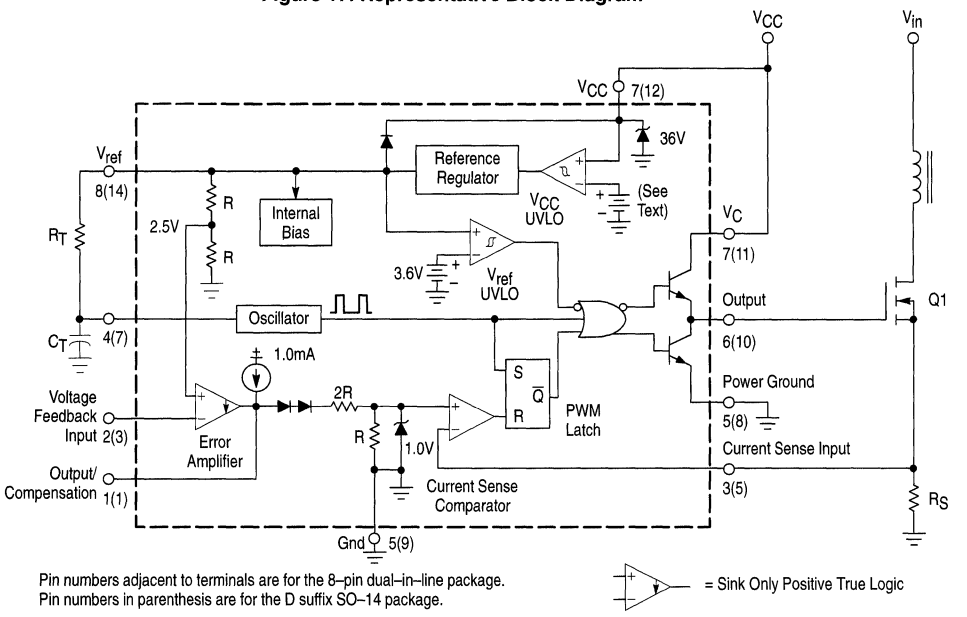
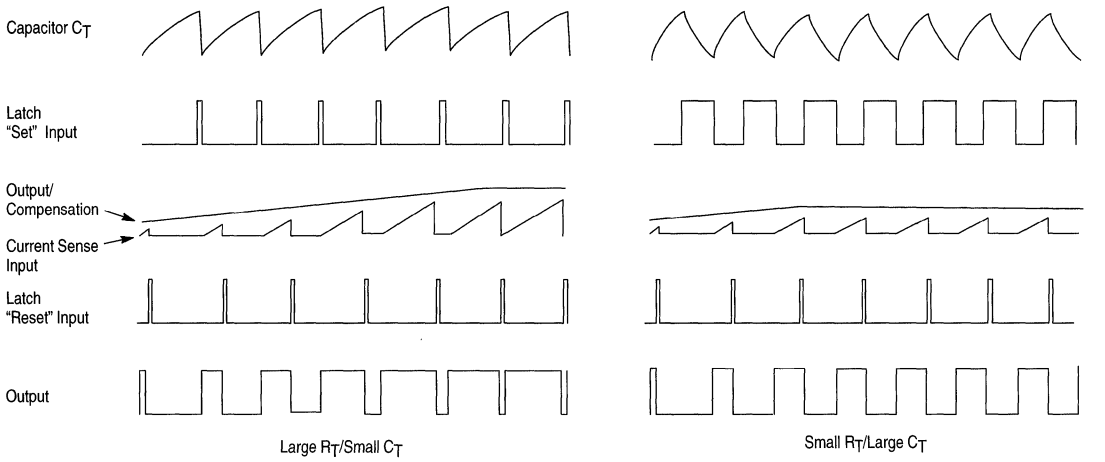


Figure 18. Timing Diagram



3

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX842B, and 8.4 V/7.6 V for the UCX843B. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low startup current of the UCX842B makes it ideally suited in off–line converter applications where efficient bootstrap startup techniques are required (Figure 33). The UCX843B is intended for lower voltage dc–to–dc converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage (V_{CC}) for the UCX842B is 11 V and 8.2 V for the UCX843B.

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull–down resistor.

The SO–14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 25 shows proper power and control ground connections in a current–sensing power MOSFET application.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284XB, and ±2.0% on the UC384XB. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short–circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low–current signal and high–current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise–generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulator's closed loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 19A shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2, until the next oscillator cycle. The unstable condition can be shown if a perturbation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn–on (t_2) is increased by $\Delta I + \Delta I\, m_2/m_1$. The minimum current at the next cycle (t_3) decreases to ($\Delta I + \Delta I\, m_2/m_1$) ($m_2/m_1$). This perturbation is multiplied by m_2/m_1 on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn–on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Figure 19B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI perturbation will decrease to zero on succeeding cycles. This compensating ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage, yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 32).

Figure 19. Continuous Current Waveforms

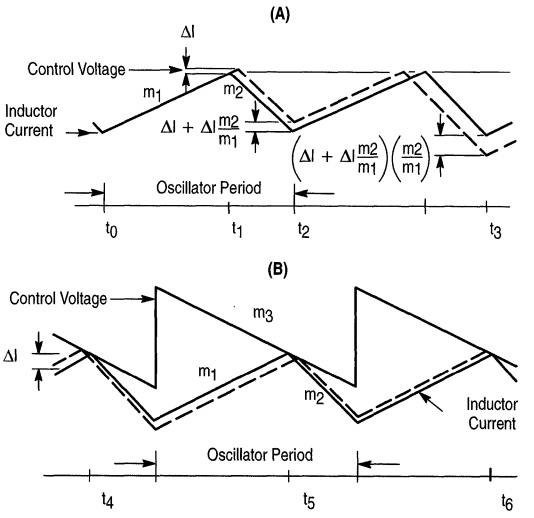
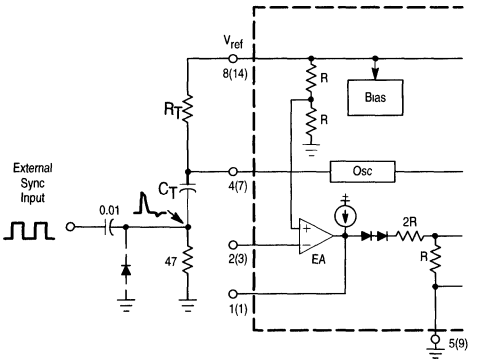
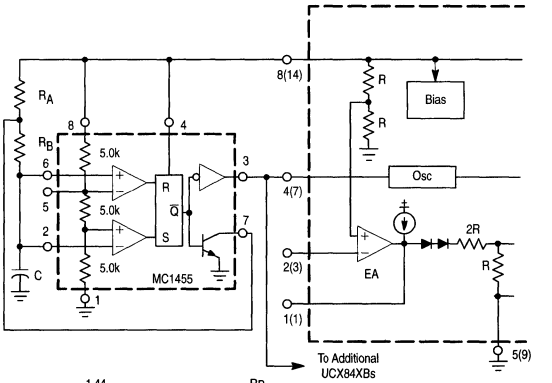


Figure 20. External Clock Synchronization



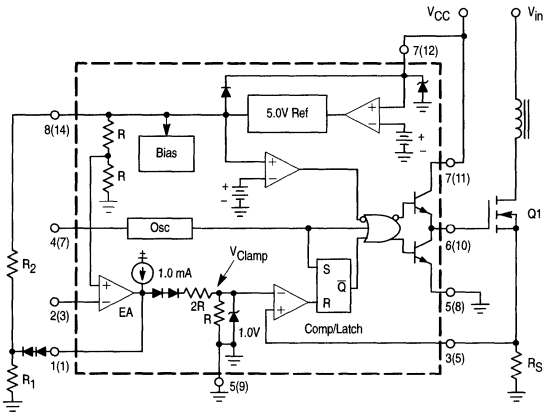
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 21. External Duty Cycle Clamp and Multi–Unit Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D(max) = \frac{R_B}{R_A + 2R_B}$$

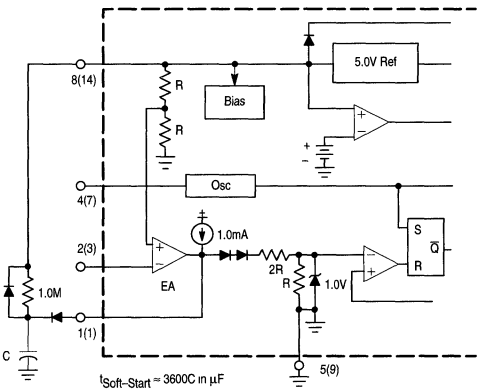
Figure 22. Adjustable Reduction of Clamp Level



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{-3} \left(\frac{R_1 R_2}{R_1 + R_2}\right) \qquad \text{Where: } 0 \le V_{Clamp} \le 1.0\ V$$

$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

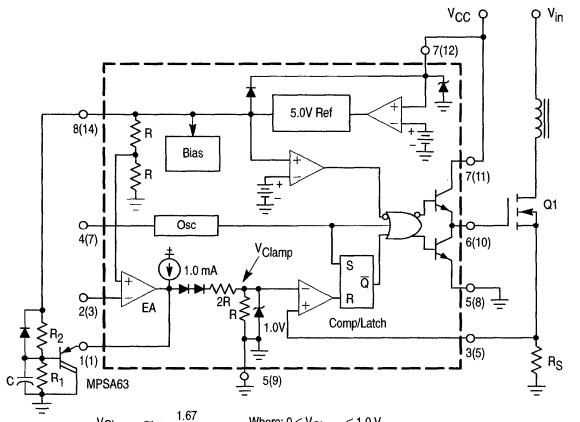
Figure 23. Soft–Start Circuit



$$t_{Soft\text{-}Start} \approx 3600C \text{ in } \mu F$$

3

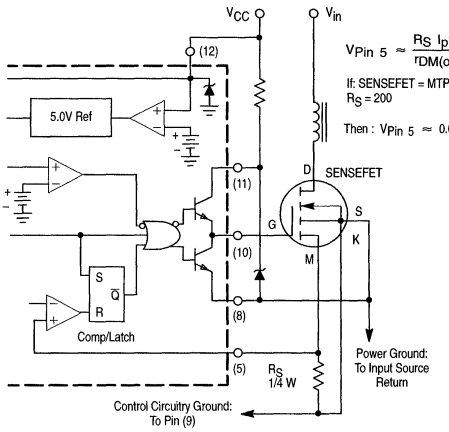
Figure 24. Adjustable Buffered Reduction of Clamp Level with Soft–Start



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} \qquad \text{Where: } 0 \le V_{Clamp} \le 1.0\ V$$

$$t_{Soft\text{-}Start} = -\ln\left[1 - \frac{V_C}{3\ V_{Clamp}}\right] C \frac{R_1\ R_2}{R_1 + R_2} \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 25. Current Sensing Power MOSFET



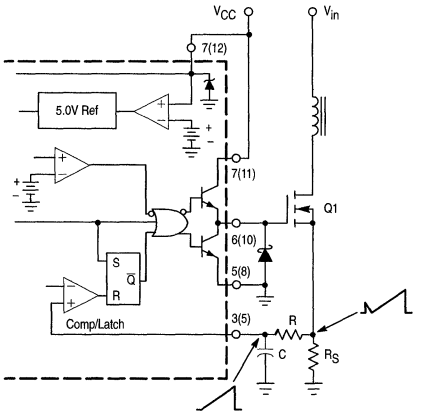
$$V_{Pin\ 5} \approx \frac{R_S\ I_{pk}\ r_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
R_S = 200

Then : $V_{Pin\ 5} \approx 0.075\ I_{pk}$

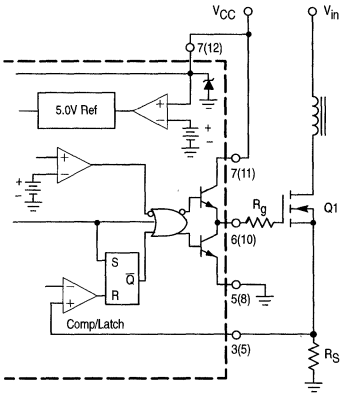
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over–current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 22 and 24.

Figure 26. Current Waveform Spike Suppression



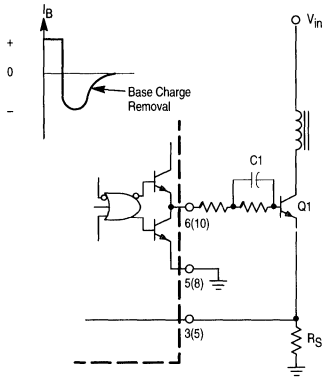
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 27. MOSFET Parasitic Oscillations



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit.

Figure 28. Bipolar Transistor Drive



The totem pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 29. Isolated MOSFET Drive

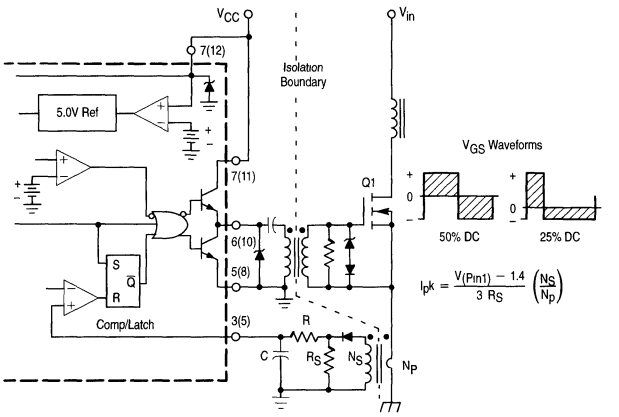
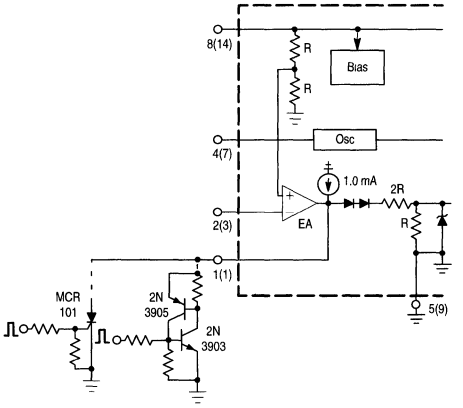
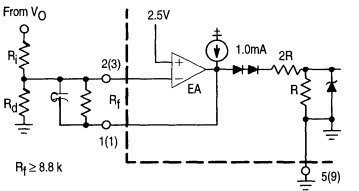


Figure 30. Latched Shutdown

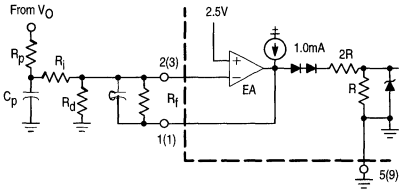


The MCR101 SCR must be selected for a holding of < 0.5 mA @ $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 31. Error Amplifier Compensation



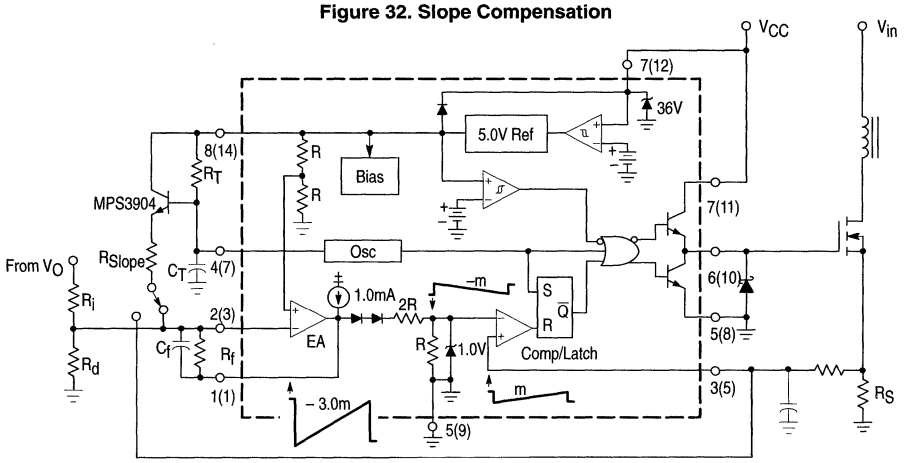
Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

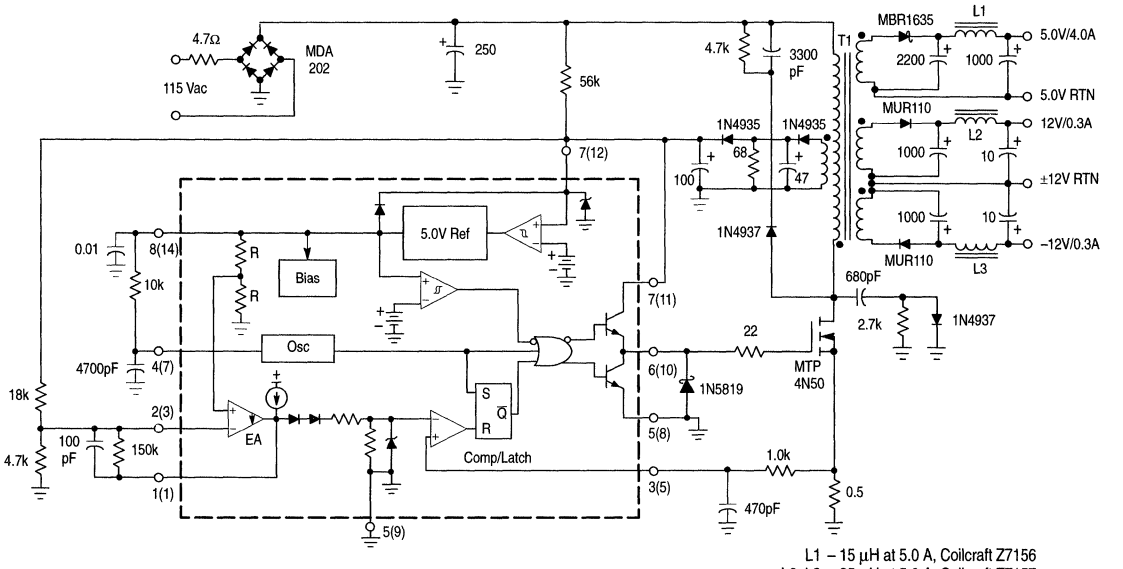
3

Figure 32. Slope Compensation



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

Figure 33. 27 W Off–Line Flyback Regulator



L1 – 15 μH at 5.0 A, Coilcraft Z7156
L2, L3 – 25 μH at 5.0 A, Coilcraft Z7157

Test	Conditions	Results
Line Regulation: 5.0 V	V_{in} = 95 to 130 Vac	Δ = 50 mV or ± 0.5%
±12 V		Δ = 24 mV or ± 0.1%
Load Regulation: 5.0 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A	Δ = 300 mV or ± 3.0%
±12 V	V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 60 mV or ± 0.25%
Output Ripple: 5.0 V	V_{in} = 115 Vac	40 mV_{pp}
±12 V		80 mV_{pp}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted

T1 – Primary: 45 Turns #26 AWG
Secondary ±12 V: 9 Turns #30 AWG (2 Strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35–3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10" for a primary inductance of 1.0 mH

MOTOROLA

UC3844, 45
UC2844, 45

3

High Performance Current Mode Controllers

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

The UC3844, UC3845 series are high performance fixed frequency current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

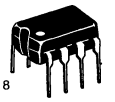
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, a latch for single pulse metering, and a flip–flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed for 50% to 70%.

These devices are available in an 8–pin dual–in–line plastic package as well as the 14–pin plastic surface mount (SO–14). The SO–14 package has separate power and ground pins for the totem pole output stage.

The UCX844 has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off–line converters. The UCX845 is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

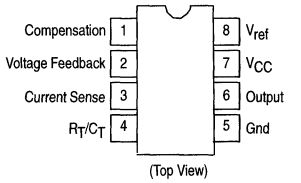
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Input Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- Direct Interface with Motorola SENSEFET Products

N SUFFIX
PLASTIC PACKAGE
CASE 626

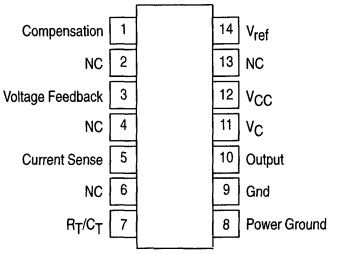


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS

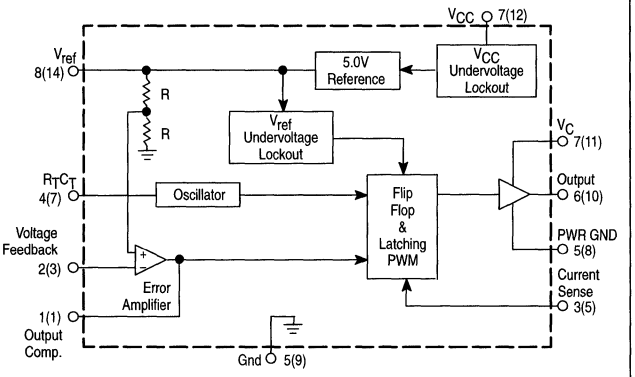


(Top View)



(Top View)

Simplified Block Diagram



Pin numbers in parenthesis are for the D suffix SO–14 package.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
UC3844D	T_A = 0° to +70°C	SO–14
UC3845D		SO–14
UC3844N		Plastic
UC3845N		Plastic
UC2844D	T_A = – 25° to +85°C	SO–14
UC2845D		SO–14
UC2844N		Plastic
UC2845N		Plastic

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	– 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package, Case 751A Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction–to–Air N Suffix, Plastic Package, Case 626 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature UC3844, UC3845 UC2844, UC2845	T_A	 0 to + 70 – 25 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284X			UC384X			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	–	2.0	20	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	25	–	3.0	25	mV
Temperature Stability	T_S	–	0.2	–	–	0.2	–	mV/°C
Total Output Variation over Line, Load, Temperature	V_{ref}	4.9	–	5.1	4.82	–	5.18	V
Output Noise Voltage (f = 10 Hz to kHz, T_J = 25°C)	V_n	–	50	–	–	50	–	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	– 30	– 85	– 180	– 30	– 85	– 180	mA
OSCILLATOR SECTION								
Frequency T_J = 25°C T_A = T_{low} to T_{high}	f_{osc}	 47 46	 52 –	 57 60	 47 46	 52 –	 57 60	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	–	0.2	1.0	%
Frequency Change with Temperature T_A = T_{low} to T_{high}	$\Delta f_{osc}/\Delta T$	–	5.0	–	–	5.0	–	%
Oscillator Voltage Swing (Peak–to–Peak)	V_{osc}	–	1.6	–	–	1.6	–	V
Discharge Current (V_{osc} = 2.0 V, T_J = 25°C)	I_{dischg}	–	10.8	–	–	10.8	–	mA

NOTES: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible
T_{low} = 0°C for UC3844, UC3845; –25°C for UC2844, UC2845
T_{high} = +70°C for UC3844, UC3845; +85°C for UC2844, UC2845

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted,)

Characteristics	Symbol	UC284X Min	UC284X Typ	UC284X Max	UC384X Min	UC384X Typ	UC384X Max	Unit
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 2.7 V)	I_{IB}	–	–0.1	–1.0	–	–0.1	–2.0	µA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	–	2.0	12	–	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	–0.5	–1.0	–	–0.5	–1.0	–	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}	–	0.8	1.1	–	0.8	1.1	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V	2.85	3.0	3.15	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	0.9	1.0	1.1	V
Power Supply Rejection Ratio	PSRR							dB
V_{CC} = 12 V to 25 V (Note 4)		–	70	–	–	70	–	
Input Bias Current	I_{IB}	–	–2.0	–10	–	–2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(IN/OUT)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{Sink} = 200 mA)		–	1.6	2.2	–	1.6	2.2	
High State (I_{Sink} = 20 mA)	V_{OH}	12	13.5	–	13	13.5	–	
(I_{Sink} = 200 mA)		12	13.4	–	12	13.4	–	
Output Voltage with UVLO Activated	$V_{OL(UVLO)}$							V
V_{CC} = 6.0 V, I_{Sink} = 1.0 mA		–	0.1	1.1	–	0.1	1.1	
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold	V_{th}							V
UCX844		15	16	17	14.5	16	17.5	
UCX845		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$							V
UCX844		9.0	10	11	8.5	10	11.5	
UCX845		7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION								
Duty Cycle								%
Maximum	DC_{max}	46	48	50	47	48	50	
Minimum	DC_{min}	–	–	0	–	–	0	
TOTAL DEVICE								
Power Supply Current (Note 2)	I_{CC}							mA
Startup:								
(V_{CC} = 6.5 V for UCX845A,		–	0.5	1.0	–	0.5	1.0	
14 V for UCX844) Operating		–	12	17	–	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible
   T_{low} = 0°C for UC3844, UC3845; –25°C for UC2844, UC2845 T_{high} = +70°C for UC3844, UC3845; +85°C for UC2844, UC2845

4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

3

Figure 1. Timing Resistor versus Oscillator Frequency

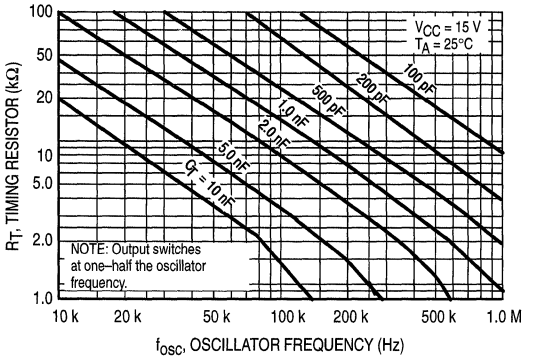


Figure 2. Output Deadtime versus Oscillator Frequency

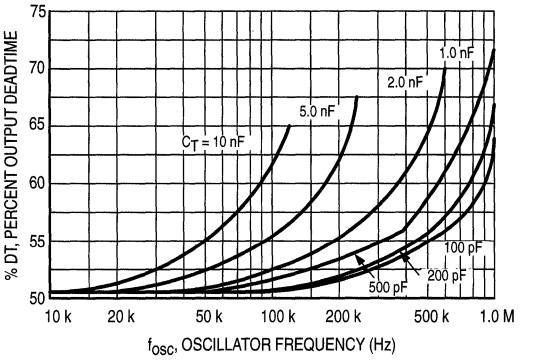


Figure 3. Error Amp Small Signal Transient Response

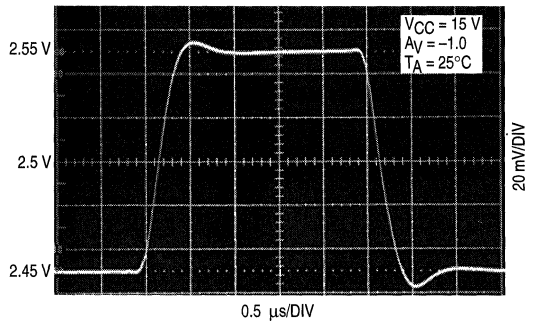


Figure 4. Error Amp Large Signal Transient Response

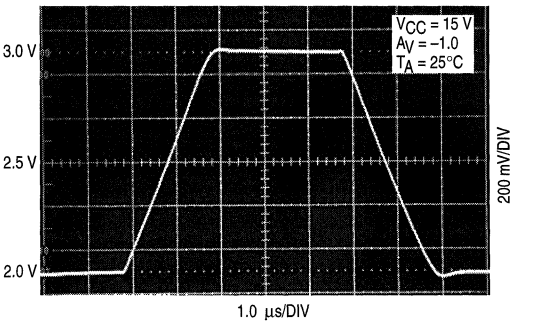


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

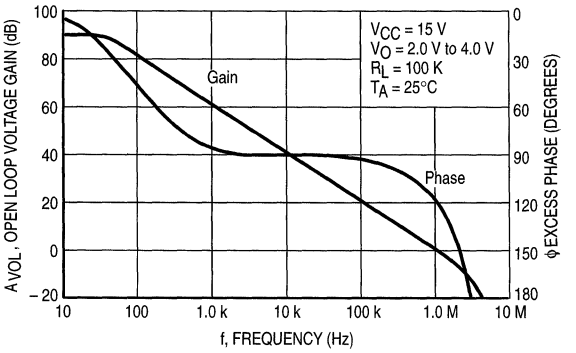


Figure 6. Current Sense Input Threshold versus Error Amp Output Voltage

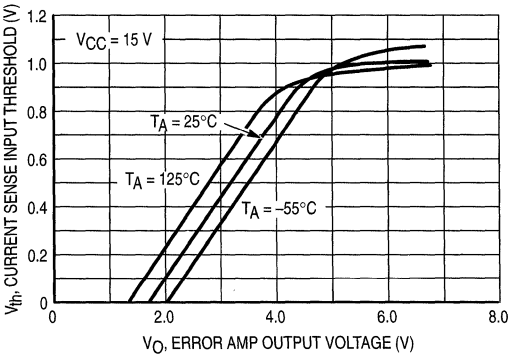


Figure 7. Reference Voltage Change versus Source Current

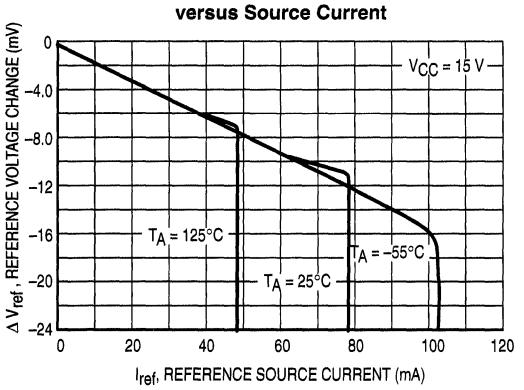


Figure 8. Reference Short Circuit Current versus Temperature

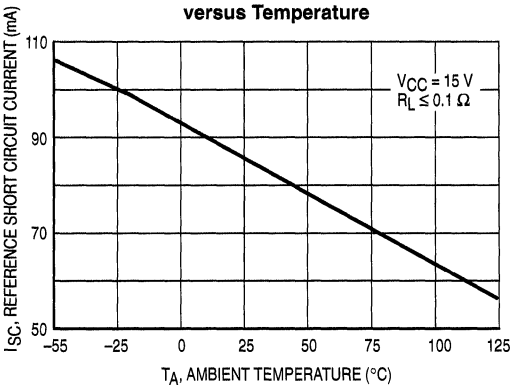


Figure 9. Reference Load Regulation

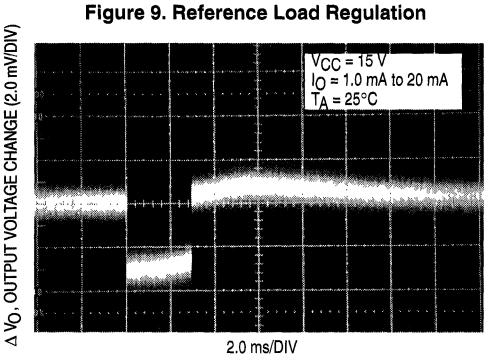


Figure 10. Reference Line Regulation

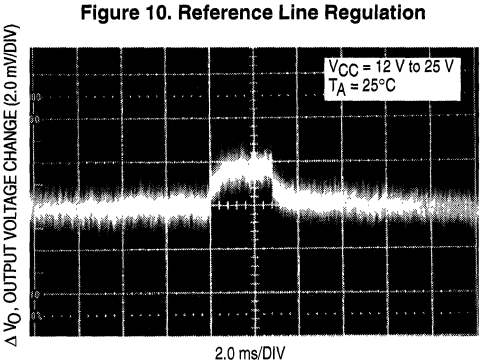


Figure 11. Output Saturation Voltage versus Load Current

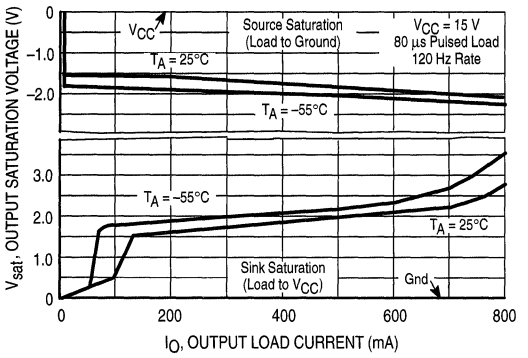


Figure 12. Output Waveform

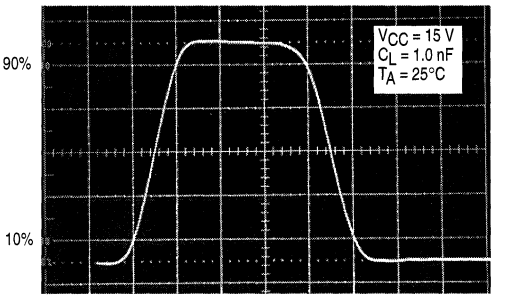


Figure 13. Output Cross Conduction

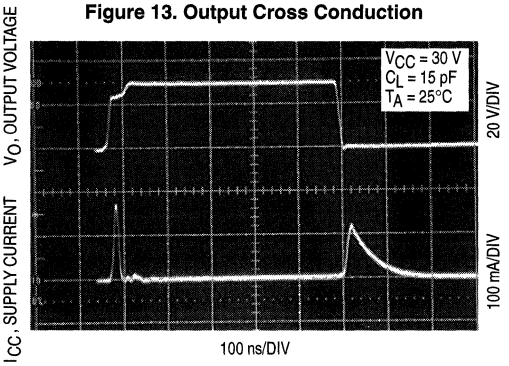
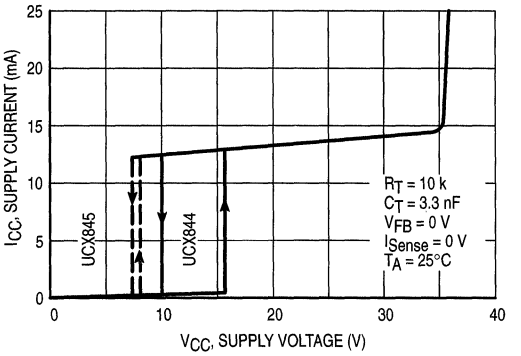


Figure 14. Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin		Function	Description
8–Pin	14–Pin		
1	1	Compensation	This pin is Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 1.0 MHz is possible.
5	–	Gnd	This pin is combined control circuitry and power ground (8–pin package only).
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin. The output switches at one–half the oscillator frequency.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
–	8	Power Ground	This pin is a separate power ground return (14–pin package only) that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
–	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin (14–pin package only). With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
–	9	Gnd	This pin is the control circuitry ground return (14–pin package only) and is connected to back to the power source ground.
–	2,4,6,13	NC	No connection (14–pin package only). These pins are not internally connected.

OPERATING DESCRIPTION

The UC3844, UC3845 series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 15.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. An internal flip–flop has been incorporated in the UCX844/5 which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 1 shows R_T versus Oscillator Frequency and figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency.

In many noise sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 17. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 18. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved to realize output deadtimes of greater than 70%

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 5). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provide for external loop compensation (Figure 28). The output voltage is offset by two diode drops (≈ 1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 20, 21). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3844, UC3845 operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin1). Thus the error signal controls the inductor current on a cycle–by–cycle basis. The current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

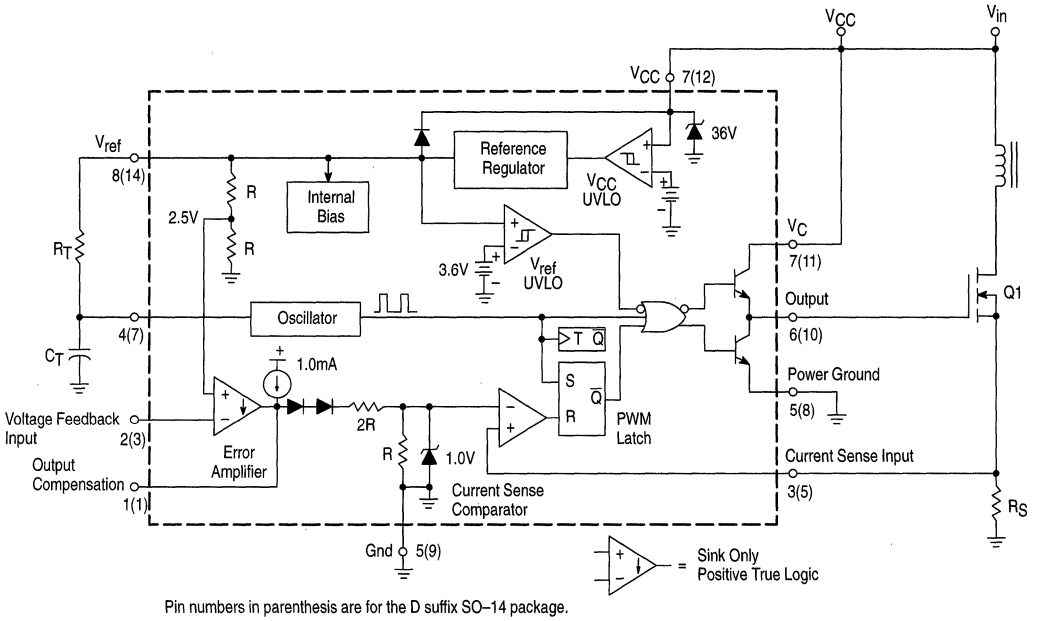
$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 23.

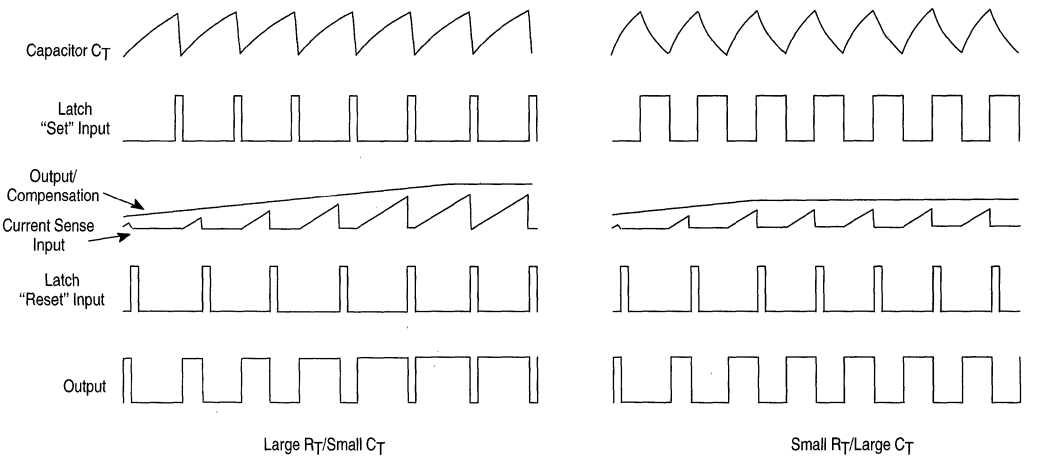
3

Figure 15. Representative Block Diagram



Pin numbers in parenthesis are for the D suffix SO–14 package.

Figure 16. Timing Diagram



Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guartantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC} and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX844, and 8.4 V/7.6 V for the UCX845. The V_{ref} comparator upper and lower thresholds are 3.6 V/3/4 V. The large hysteresis and low startup current of the UCX844 makes it ideally suited in off–line converter applications where efficient bootstrap startup techniques later required (Figure 29). The UCX845 is intended for lower voltage dc–to–dc converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for the UCX844 is 11 V and 8.2 V for the UCX845.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ± 1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever and undervoltage lockout is active. This characteristic eliminates the need for an external pull–down resistor.

The SO–14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater the 20 V. Figure 22 shows proper power and control ground connections in a current sensing power MOSFET application.

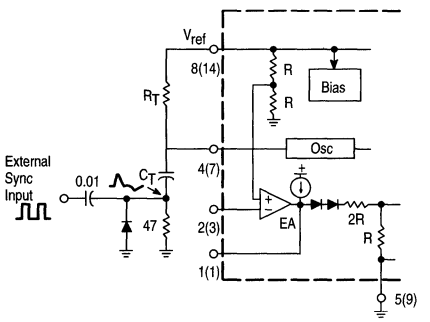
Reference

The 5.0 V bandgap reference is trimmed to ± 1.0% tolerance at T_J = 25°C on the UC284X, and ± 2.0% on the UC384X. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

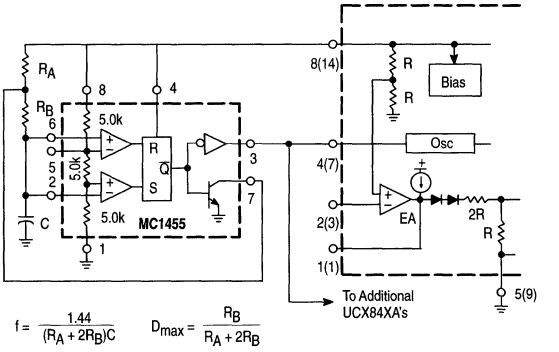
Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulsewidth jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low–current signal and high–current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Figure 17. External Clock Synchronization



The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of CT to go more than 300 mV below ground.

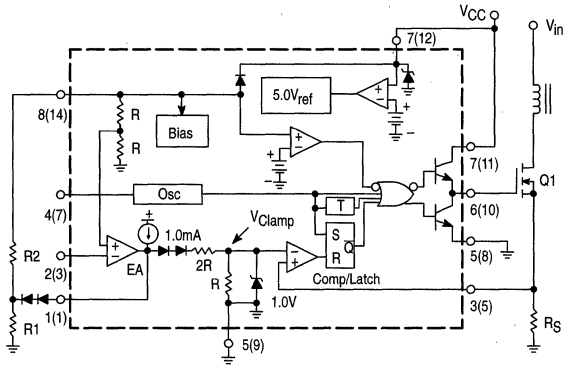
Figure 18. External Duty Cycle Clamp and Multi–Unit Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

3

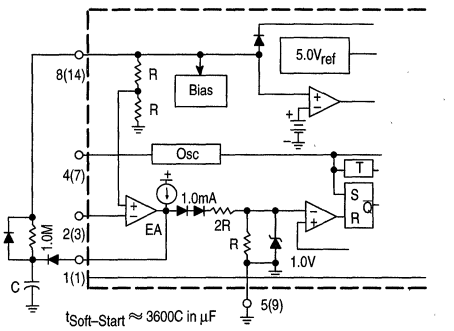
Figure 19. Adjustable Reduction of Clamp Level



$$V_{Clamp} \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{-3} \left(\frac{R_1 R_2}{R_1 + R_2}\right) \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

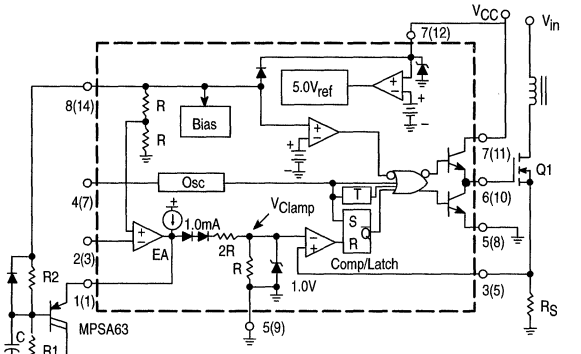
Where: $0 \le V_{Clamp} \le 1.0$ V

Figure 20. Soft–Start Circuit



$t_{Soft\text{-}Start} \approx 3600C$ in μF

Figure 21. Adjustable Buffered Reduction of Clamp Level with Soft–Start

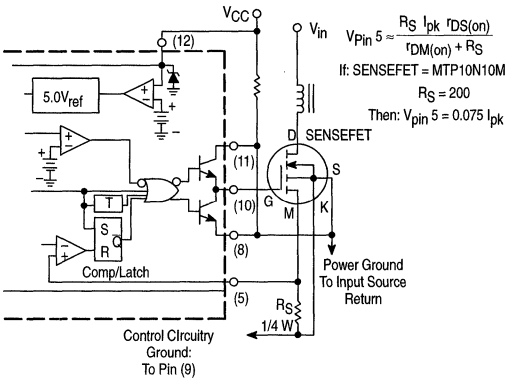


$$V_{Clamp} \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{-3} \frac{R_1 R_2}{R_1 + R_2}$$

$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S} \quad \text{Where: } 0 \le V_{Clamp} \le 1.0 \text{ V}$$

$$t_{Softstart} = -\ln \left[1 - \frac{V_C}{3V_{Clamp}}\right] C \frac{R_1 R_2}{R_1 + R_2}$$

Figure 22. Current Sensing Power MOSFET



$$V_{Pin\,5} \approx \frac{R_S\, I_{pk}\, r_{DS(on)}}{r_{DM(on)} + R_S}$$

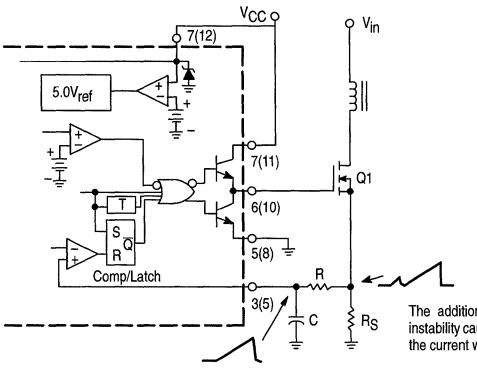
If: SENSEFET = MTP10N10M

$R_S = 200$

Then: $V_{pin\,5} = 0.075\, I_{pk}$

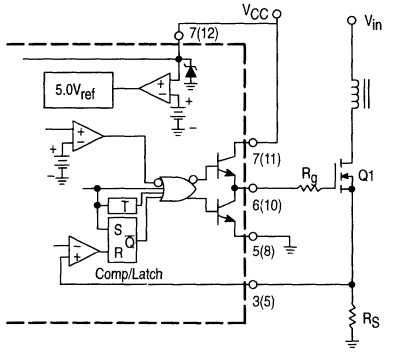
Virtually lossless current sensing can be achieved with the implement of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

Figure 23. Current Waveform Spike Suppression



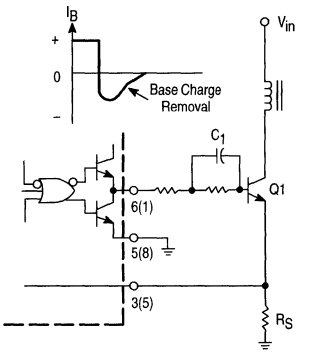
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 24. MOSFET Parasitic Oscillations



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit.

Figure 25. Bipolar Transistor Drive



The totem–pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 26. Isolated MOSFET Drive

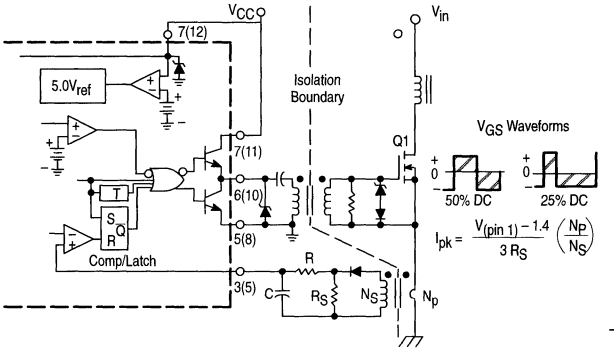
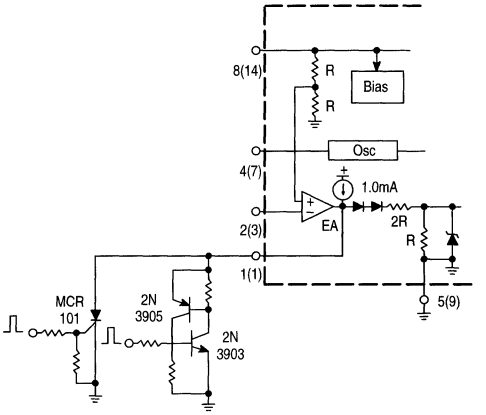
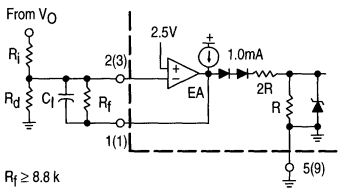


Figure 27. Latched Shutdown

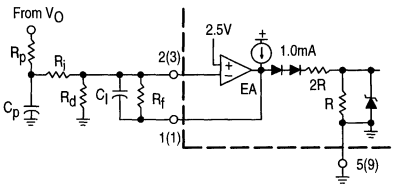


The MCR101 SCR must be selected for a holding of less than 0.5 mA at $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 28. Error Amplifier Compensation

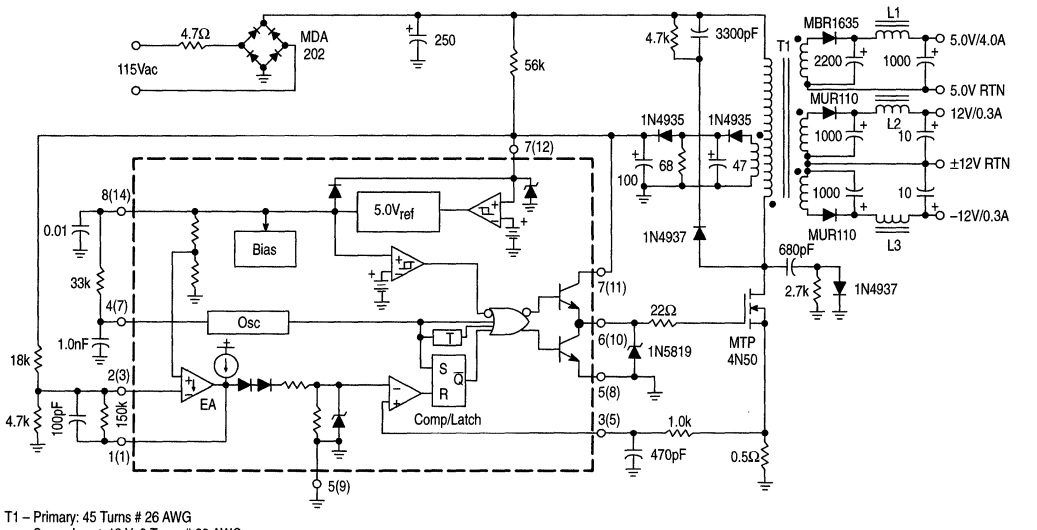


Error Amp compensation circuit for stabilizing any current–mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current–mode boost and flyback topologies operating with continuous inductor current.

Figure 29. 27 Watt Off–Line Flyback Regulator



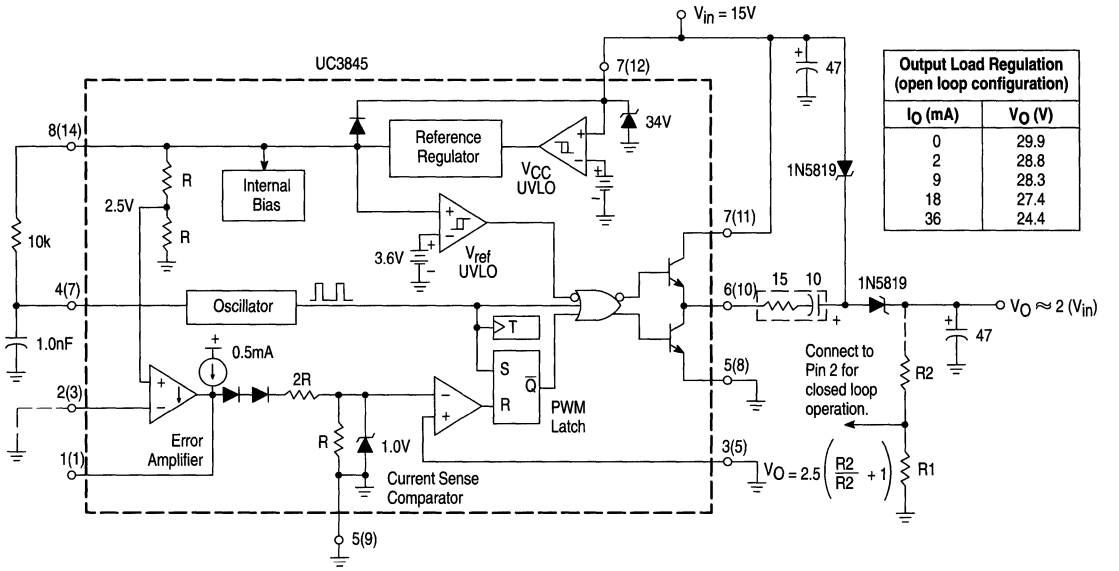
T1 – Primary: 45 Turns # 26 AWG
Secondary ± 12 V: 9 Turns # 30 AWG
(2 strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands)
#26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG
(2 strands) Bifiliar Wound
Core: Ferroxcube EC35–3C8
Bobbin: Ferroxcube EC35PCB1
Gap = 0.01" for a primary inductance of 1.0 mH

L1 – 15 µH at 5.0 A, Coilcraft Z7156.
L2, L3 – 25 µH at 1.0 A, Coilcraft Z7157.

Test		Conditions	Results
Line Regulation:	5.0 V ± 12 V	V_{in} = 95 Vac to 130 Vac	Δ = 50 mV or ± 0.5% Δ = 24 mV or ± 0.1%
Load Regulation:	5.0 V ± 12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ± 3.0% Δ = 60 mV or ± 0.25%
Output Ripple:	5.0 V ± 12 V	V_{in} = 115 Vac	40 mV_{pp} 80 mV_{pp}
Efficiency		V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted.

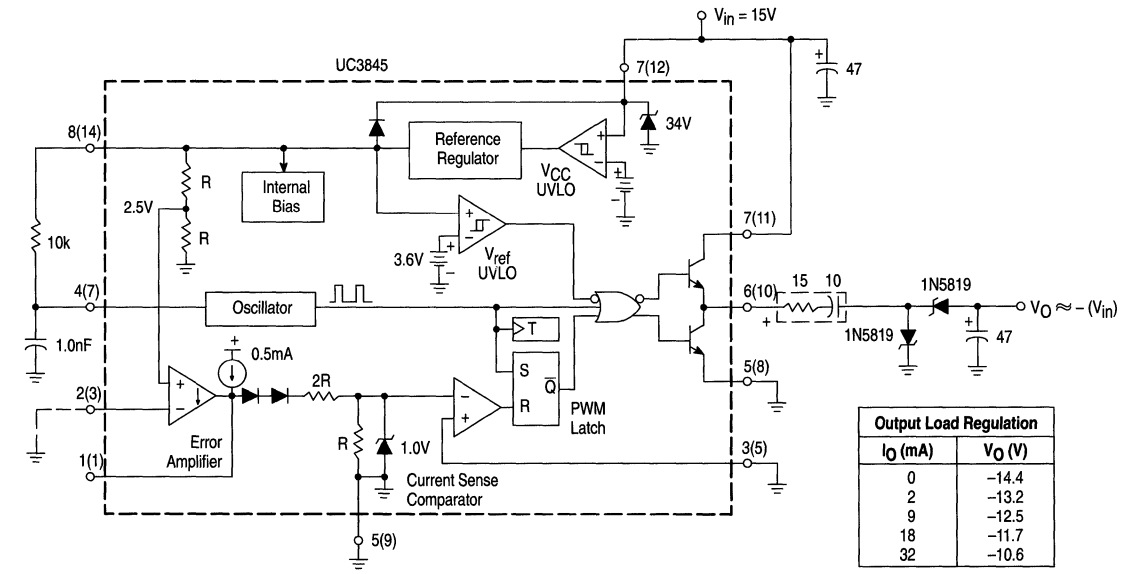
Figure 30. Step–Up Charge Pump Converter



Output Load Regulation (open loop configuration)	
I_O (mA)	V_O (V)
0	29.9
2	28.8
9	28.3
18	27.4
36	24.4

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The converter's output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

Figure 31. Voltage–Inverting Charge Pump Converter



Output Load Regulation	
I_O (mA)	V_O (V)
0	–14.4
2	–13.2
9	–12.5
18	–11.7
32	–10.6

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A.
An additional series resistor may be required when using tantalum or other low ESR capacitors.

UC3844B, 45B
UC2844B, 45B

3

High Performance Current Mode Controllers

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

The UC3844B, UC3845B series are high performance fixed frequency current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost–effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

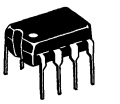
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, a latch for single pulse metering, and a flip–flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed from 50% to 70%.

These devices are available in an 8–pin dual–in–line and surface mount (SO–8) plastic package as well as the 14–pin plastic surface mount (SO–14). The SO–14 package has separate power and ground pins for the totem pole output stage.

The UCX844B has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off–line converters. The UCX845B is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current

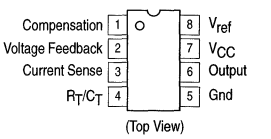
N SUFFIX
PLASTIC PACKAGE
CASE 626



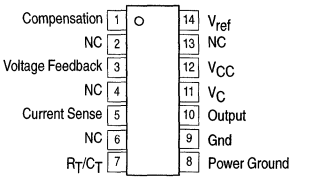
D1 SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS

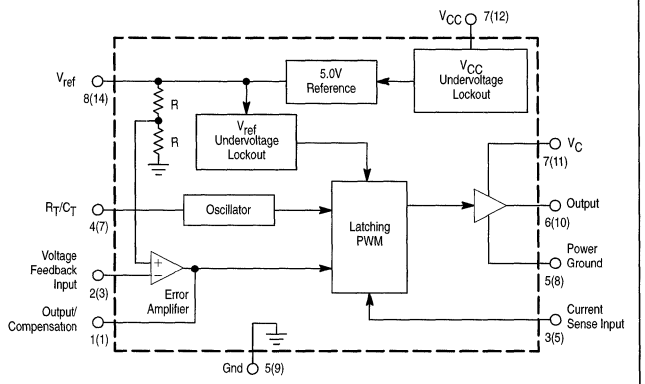


(Top View)



(Top View)

Simplified Block Diagram



Pin numbers in parenthesis are for the D suffix SO–14 package.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
UC384XBD	T_A = 0° to + 70°C	SO–14
UC384XBD1		SO–8
UC384XBN		Plastic
UC284XBD	T_A = – 25° to + 85°C	SO–14
UC284XBD1		SO–8
UC284XBN		Plastic
UC384XBVD	T_A = – 40° to +105°C	SO–14
UC384XBVD1		SO–8
UC384XBVN		Plastic

X indicates either a 4 or 5 to define specific device part numbers.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	– 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package, SO–14 Case 751A			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	145	°C/W
D1 Suffix, Plastic Package, SO–8 Case 751			
Maximum Power Dissipation @ T_A = 25°C	P_D	702	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
N Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
UC3844B, UC3845B		0 to + 70	
UC2844B, UC2845B		– 25 to + 85	
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	–	2.0	20	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	25	–	3.0	25	mV
Temperature Stability	T_S	–	0.2	–	–	0.2	–	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	–	5.1	4.82	–	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	–	50	–	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	– 30	– 85	–180	– 30	– 85	–180	mA
OSCILLATOR SECTION								
Frequency	f_{OSC}							kHz
T_J = 25°C		49	52	55	49	52	55	
T_A = T_{low} to T_{high}		48	–	56	48	–	56	
T_J = 25°C (R_T = 6.2 k, C_T = 1.0 nF)		225	250	275	225	250	275	
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	–	0.2	1.0	–	0.2	1.0	%
Frequency Change with Temperature T_A = T_{low} to T_{high}	$\Delta f_{OSC}/\Delta T$	–	1.0	–	–	0.5	–	%
Oscillator Voltage Swing (Peak–to–Peak)	V_{OSC}	–	1.6	–	–	1.6	–	V
Discharge Current (V_{OSC} = 2.0 V)	I_{dischg}							mA
T_J = 25°C		7.8	8.3	8.8	7.8	8.3	8.8	
T_A = T_{low} to T_{high} (UC284XB, UC384XB)		7.5	–	8.8	7.6	–	8.8	
(UC384XBV)		–	–	–	7.2	–	8.8	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3844B, UC3845B; T_{high} = + 70°C for UC3844B, UC3845B
= – 25°C for UC2844B, UC2845B; = + 85°C for UC2844B, UC2845B
= – 40°C for UC3844BV, UC3845BV; = +105°C for UC3844BV, UC3845BV

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	UC284XB Min	UC284XB Typ	UC284XB Max	UC384XB, XBV Min	UC384XB, XBV Typ	UC384XB, XBV Max	Unit
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	–1.0	–	– 0.1	– 2.0	µA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	–	2.0	12	–	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	– 0.5	–1.0	–	– 0.5	–1.0	–	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}							
(UC284XB, UC384XB)		–	0.8	1.1	–	0.8	1.1	
(UC384XBV)		–	–	–	–	0.8	1.2	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V							V/V
(UC284XB, UC384XB)		2.85	3.0	3.15	2.85	3.0	3.15	
(UC384XBV)		–	–	–	2.85	3.0	3.25	
Maximum Current Sense Input Threshold (Note 4)	V_{th}							V
(UC284XB, UC384XB)		0.9	1.0	1.1	0.9	1.0	1.1	
(UC384XBV)		–	–	–	0.85	1.0	1.1	
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V) (Note 4)	PSRR	–	70	–	–	70	–	dB
Input Bias Current	I_{IB}	–	– 2.0	–10	–	– 2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(In/Out)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{Sink} = 200 mA, UC284XB, UC384XB)		–	1.6	2.2	–	1.6	2.2	
(I_{Sink} = 200 mA, UC384XBV)		–	–	–	–	1.6	2.3	
High State (I_{Source} = 20 mA, UC284XB, UC384XB)	V_{OH}	13	13.5	–	13	13.5	–	
(I_{Source} = 20 mA, UC384XBV)		–	–	–	12.9	–	–	
(I_{Source} = 200 mA)		12	13.4	–	12	13.4	–	
Output Voltage with UVLO Activated V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	–	0.1	1.1	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold	V_{th}							V
UCX844B, BV		15	16	17	14.5	16	17.5	
UCX845B, BV		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$							V
UCX844B, BV		9.0	10	11	8.5	10	11.5	
UCX845B, BV		7.0	7.6	8.2	7.0	7.6	8.2	

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for UC3844B, UC3845B; T_{high} = + 70°C for UC3844B, UC3845B
   = – 25°C for UC2844B, UC2845B; = + 85°C for UC2844B, UC2845B
   = – 40°C for UC3844BV, UC3845BV; = +105°C for UC3844BV, UC3845BV

4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V = \frac{\Delta V \text{ Output/Compensation}}{\Delta V \text{ Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
PWM SECTION								
Duty Cycle								%
Maximum (UC284XB, UC384XB)	$DC_{(max)}$	47	48	50	47	48	50	
(UC384XBV)		–	–	–	46	48	50	
Minimum	$DC_{(min)}$	–	–	0	–	–	0	
TOTAL DEVICE								
Power Supply Current	I_{CC}							mA
Startup (V_{CC} = 6.5 V for UCX845B, 14 V for UCX844B, BV)		–	0.3	0.5	–	0.3	0.5	
Operating (Note 2)		–	12	17	–	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3844B, UC3845B; T_{high} = + 70°C for UC3844B, UC3845B
= – 25°C for UC2844B, UC2845B = + 85°C for UC2844B, UC2845B
= – 40°C for UC3844BV, UC3845BV = +105°C for UC3844BV, UC3845BV

Figure 1. Timing Resistor versus Oscillator Frequency

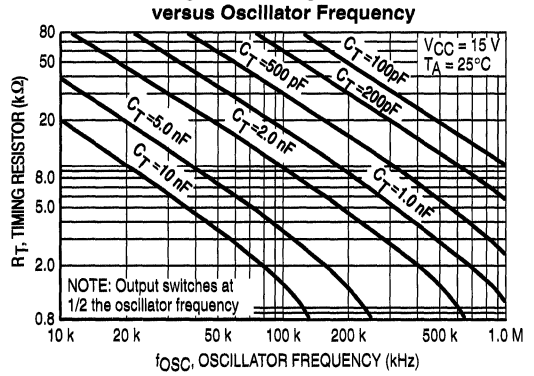


Figure 2. Output Deadtime versus Oscillator Frequency

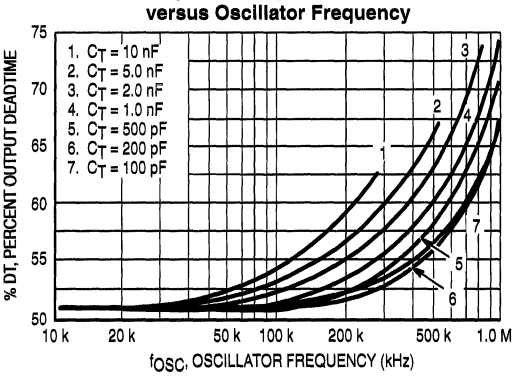


Figure 3. Error Amp Small Signal Transient Response

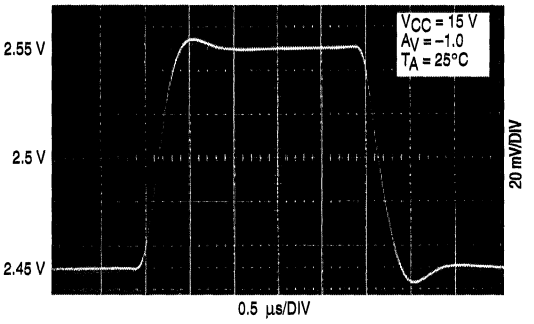
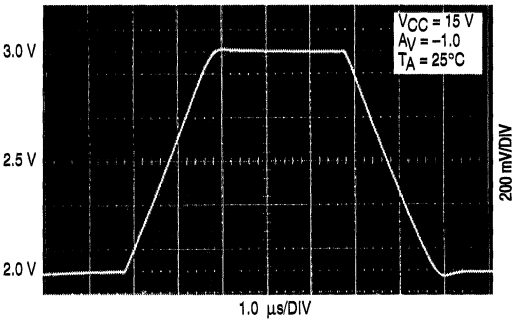


Figure 4. Error Amp Large Signal Transient Response



3

Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

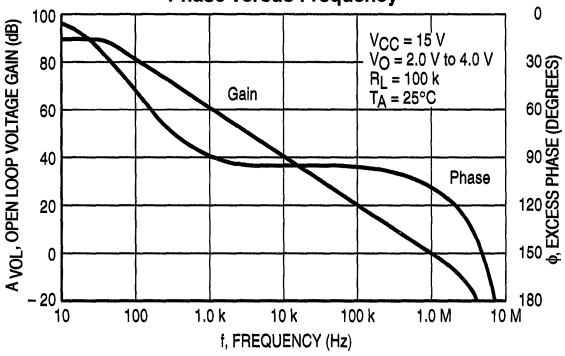


Figure 6. Current Sense Input Threshold versus Error Amp Output Voltage

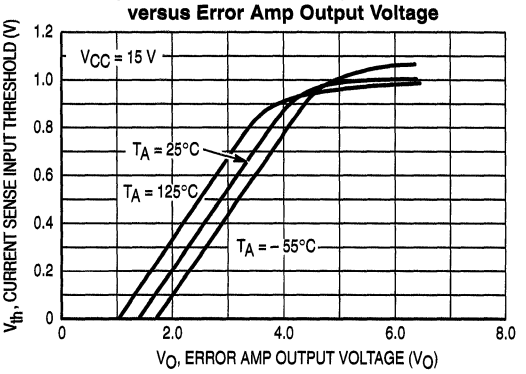


Figure 7. Reference Voltage Change versus Source Current

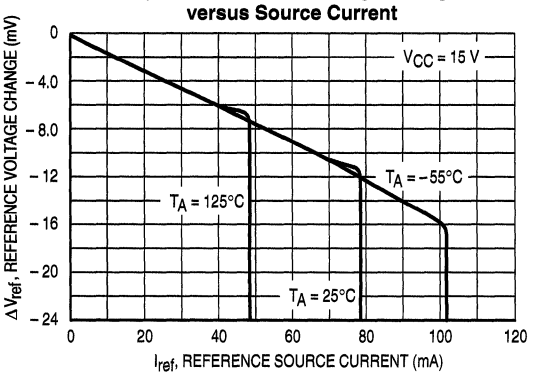


Figure 8. Reference Short Circuit Current versus Temperature

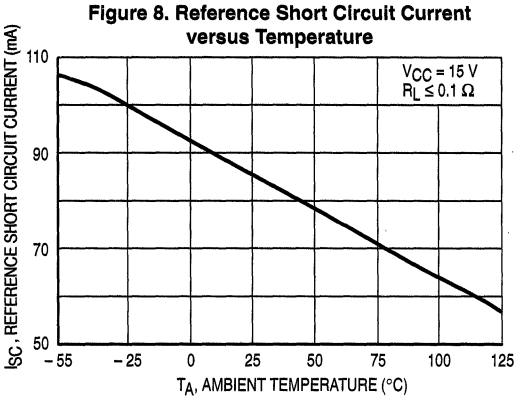


Figure 9. Reference Load Regulation

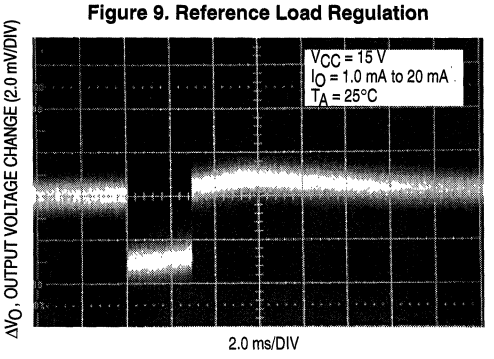


Figure 10. Reference Line Regulation

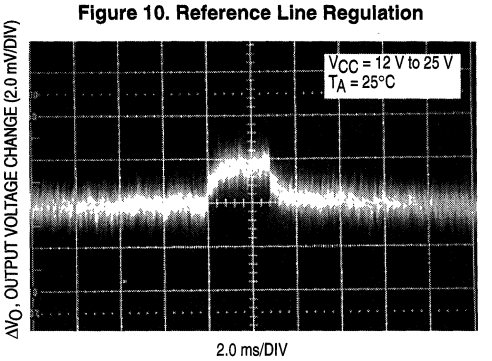


Figure 11. Output Saturation Voltage versus Load Current

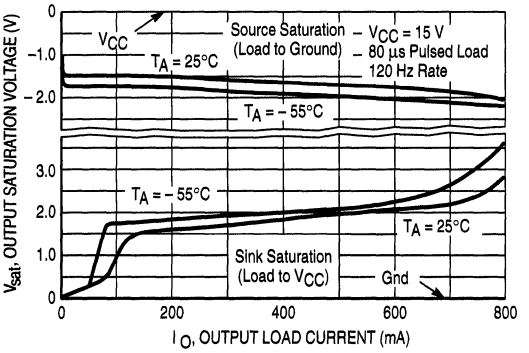


Figure 12. Output Waveform

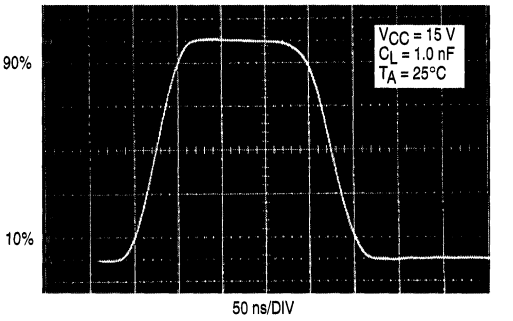


Figure 13. Output Cross Conduction

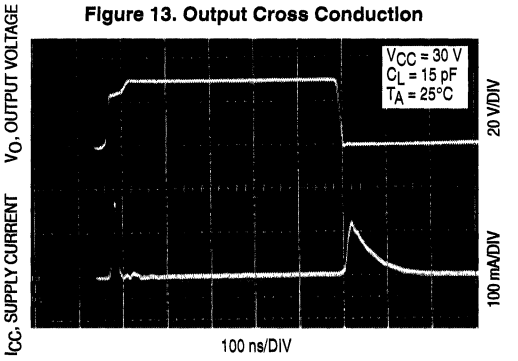
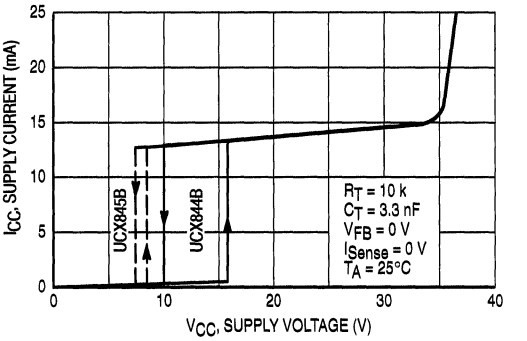


Figure 14. Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin			
8–Pin	14–Pin	Function	Description
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Oscillator operation to 1.0 kHz is possible.
5		Gnd	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin. The output switches at one–half the oscillator frequency.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	Gnd	This pin is the control circuitry ground return and is connected back to the power source ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

OPERATING DESCRIPTION

The UC3844B, UC3845B series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost–effective solution with minimal external components. A representative block diagram is shown in Figure 15.

3

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. An internal flip–flop has been incorporated in the UCX844/5B which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated to within ±6% at 50 kHz. Also, because of industry trends moving the UC384X into higher and higher frequency applications, the UC384XB is guaranteed to within ±10% at 250 kHz.

In many noise–sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 17. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. A method for multi–unit synchronization is shown in Figure 18. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved to realize output deadtimes of greater than 70%.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 5). The non–inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 28). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 20, 21). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3844B, UC3845B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground–referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 23).

Figure 15. Representative Block Diagram

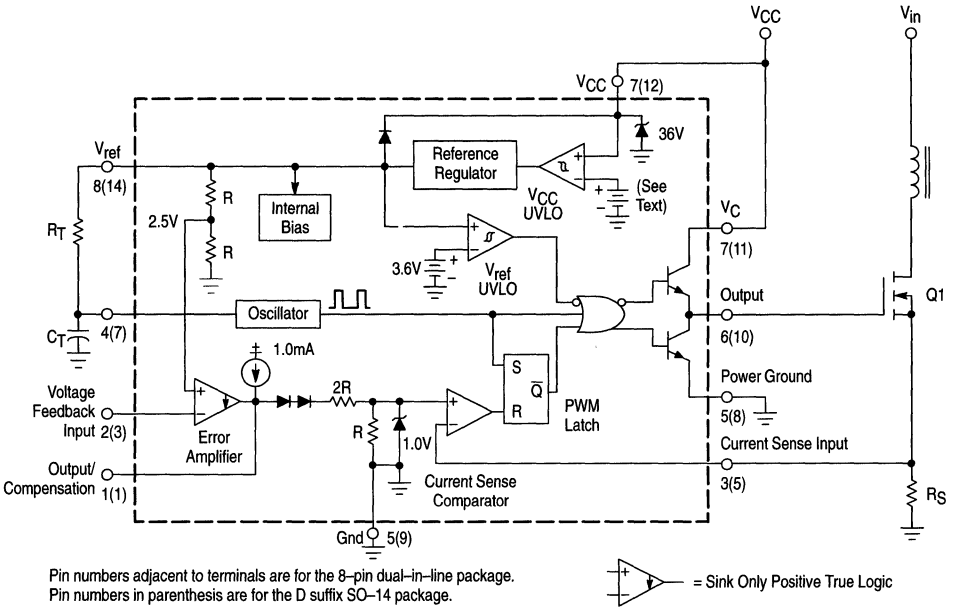
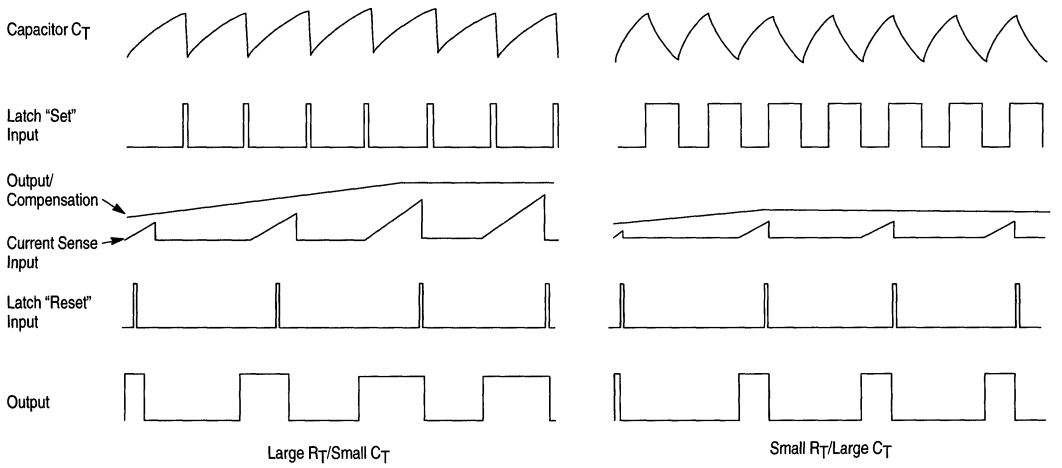


Figure 16. Timing Diagram



3

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX844B, and 8.4 V/7.6 V for the UCX845B. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low startup current of the UCX844B makes it ideally suited in off–line converter applications where efficient bootstrap startup techniques are required (Figure 29). The UCX845B is intended for lower voltage dc–to–dc converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for the UCX845B is 11 V and 8.2 V for the UCX845B.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull–down resistor.

The SO–14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 22 shows proper power and control ground connections in a current–sensing power MOSFET application.

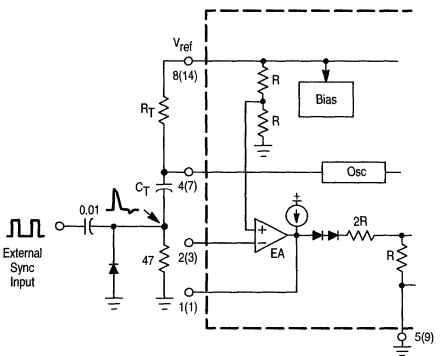
Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284XB, and ±2.0% on the UC384XB. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short–circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

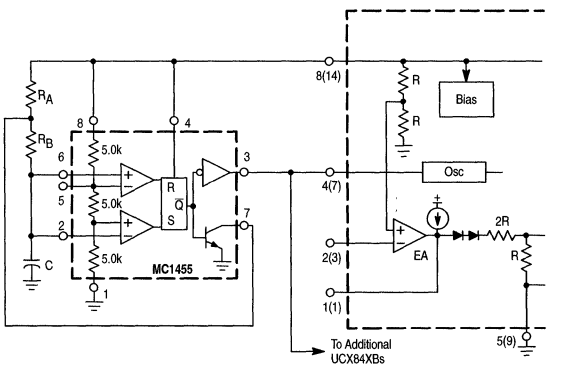
Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low–current signal and high–current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise–generating components.

Figure 17. External Clock Synchronization



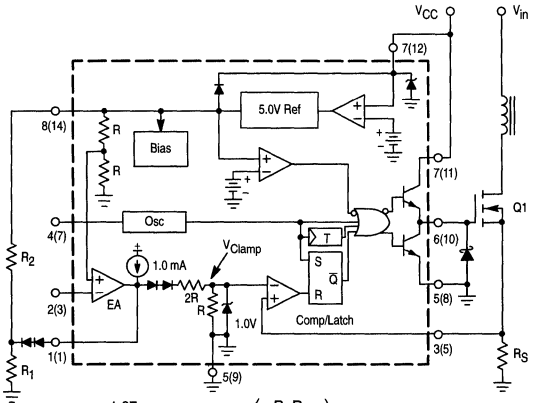
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 18. External Duty Cycle Clamp and Multi–Unit Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D(max) = \frac{R_A}{R_A + 2R_B}$$

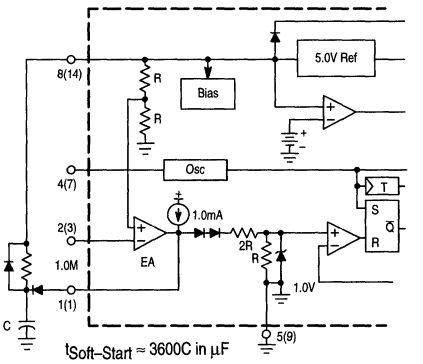
Figure 19. Adjustable Reduction of Clamp Level



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{-3} \left(\frac{R_1 R_2}{R_1 + R_2}\right) \quad \text{Where: } 0 \le V_{Clamp} \le 1.0\ V$$

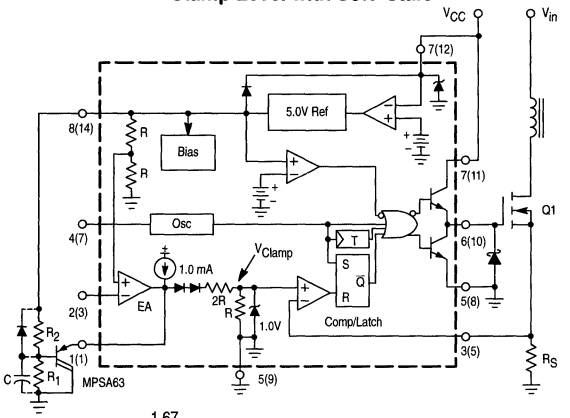
$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 20. Soft–Start Circuit



$t_{Soft\text{-}Start} \approx 3600C$ in μF

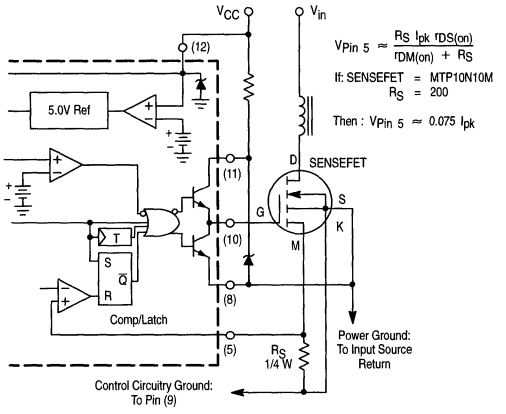
Figure 21. Adjustable Buffered Reduction of Clamp Level with Soft–Start



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} \quad \text{Where: } 0 \le V_{Clamp} \le 1.0\ V$$

$$t_{Soft\text{-}Start} = -\ln\left[1 - \frac{V_C}{3V_{Clamp}}\right] C \frac{R_1 R_2}{R_1 + R_2} \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 22. Current Sensing Power MOSFET

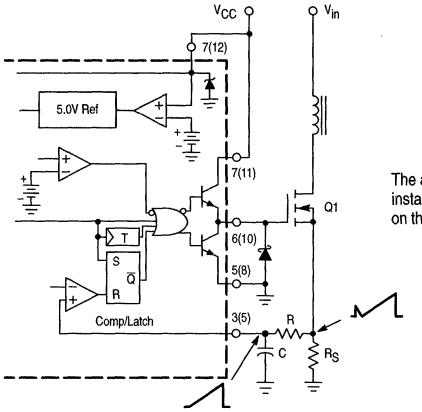


$$V_{Pin\ 5} \approx \frac{R_S\ I_{pk}\ r_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
R_S = 200
Then : $V_{Pin\ 5} \approx 0.075\ I_{pk}$

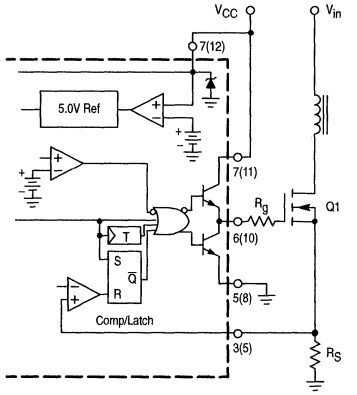
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over–current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

Figure 23. Current Waveform Spike Suppression



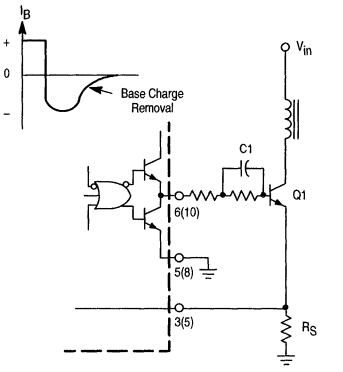
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 24. MOSFET Parasitic Oscillations



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit.

Figure 25. Bipolar Transistor Drive



The totem pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 26. Isolated MOSFET Drive

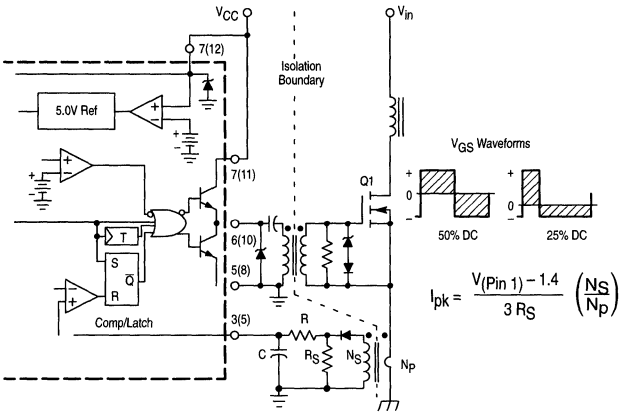
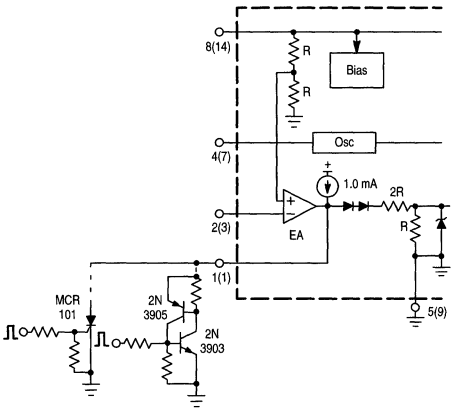
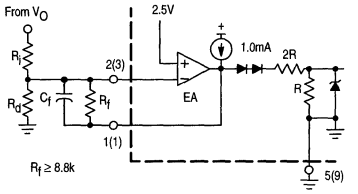


Figure 27. Latched Shutdown

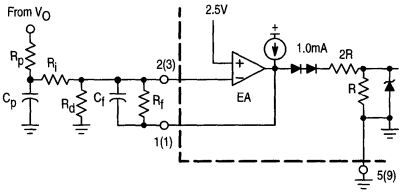


The MCR101 SCR must be selected for a holding of < 0.5 mA @ $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 28. Error Amplifier Compensation

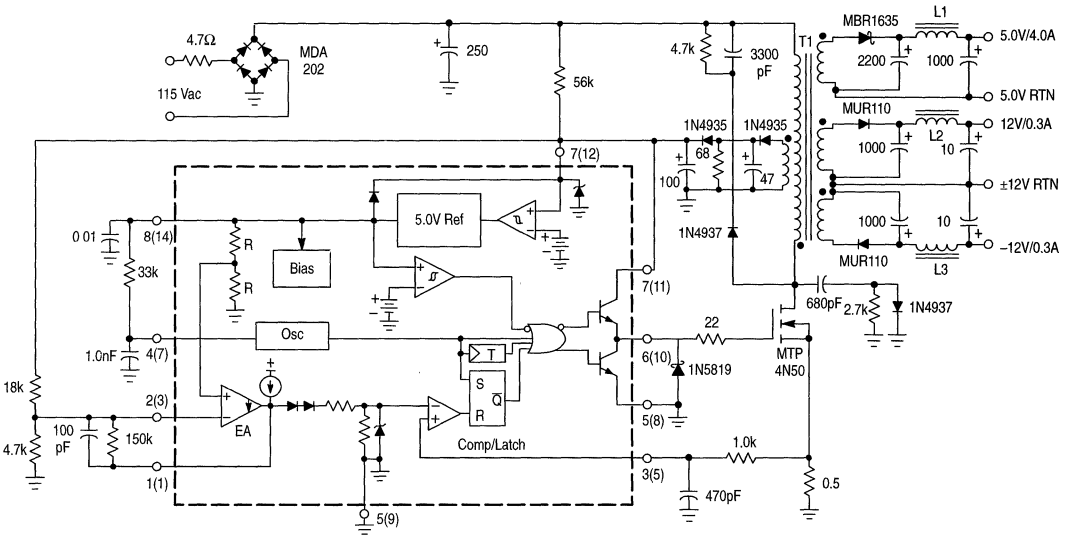


Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

Figure 29. 7 W Off–Line Flyback Regulator



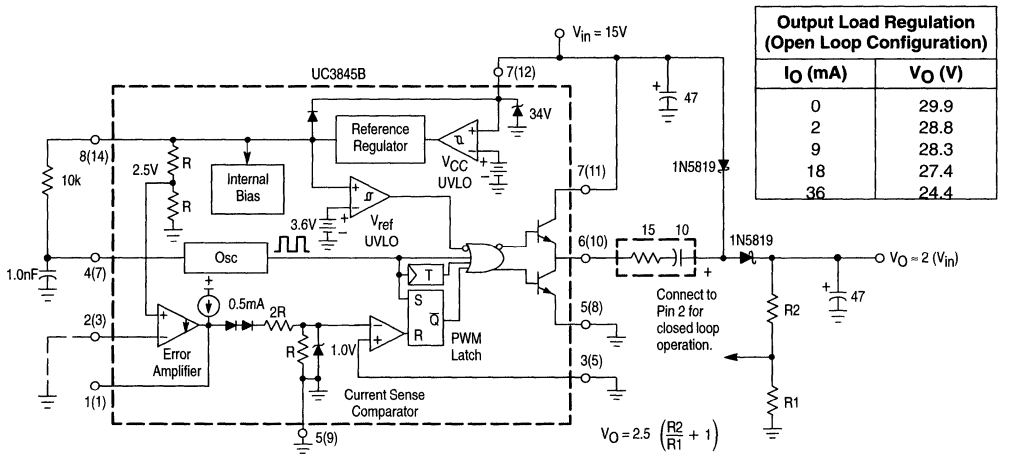
T1 – Primary: 45 Turns #26 AWG
Secondary ±12 V: 9 Turns #30 AWG (2 Strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35–3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10" for a primary inductance of 1.0 mH

L1 – 15 μH at 5.0 A, Coilcraft Z7156
L2, L3 – 25 μH at 5.0 A, Coilcraft Z7157

Test	Conditions	Results
Line Regulation: 5.0 V ±12 V	V_{in} = 95 Vac to 130 Vac	Δ = 50 mV or ±0.5% Δ = 24 mV or ±0.1%
Load Regulation: 5.0 V ±12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ±3.0% Δ = 60 mV or ±0.25%
Output Ripple: 5.0 V ±12 V	V_{in} = 115 Vac	40 mV_{pp} 80 mV_{pp}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents unless otherwise noted.

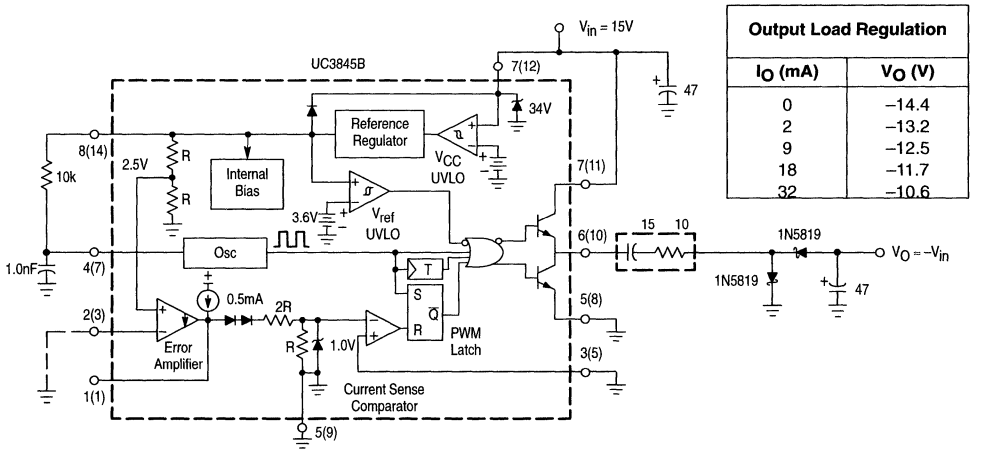
Figure 30. Step–Up Charge Pump Converter



Output Load Regulation (Open Loop Configuration)	
I_O (mA)	V_O (V)
0	29.9
2	28.8
9	28.3
18	27.4
36	24.4

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The converter's output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

Figure 31. Voltage–Inverting Charge Pump Converter



Output Load Regulation	
I_O (mA)	V_O (V)
0	−14.4
2	−13.2
9	−12.5
18	−11.7
32	−10.6

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A.
An additional series resistor may be required when using tantalum or other low ESR capacitors.

μA78S40

3

Universal Switching Regulator Subsystem

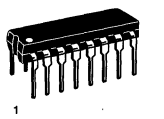
The μA78S40 is a switching regulator subsystem, consisting of a temperature compensated voltage reference, controlled–duty cycle oscillator with an active current limit circuit, comparator, high–current and high–voltage output switch, capable of 1.5 A and 40 V, pinned–out power diode and an uncommitted operational amplifier, which can be powered up or down independent of the IC supply. The switching output can drive external NPN or PNP transistors when voltages greater the 40 V, or currents in excess of 1.5 A, are required. Some of the features are wide–supply voltage range, low standby current, high efficiency and low drift. The μA78S40 is available in commercial (0° to + 70°C), and automotive (–40° to + 85°C) temperature ranges.

Some of the applications include use in step–up, step–down, and inverting regulators, with extremely good results obtained in battery–operated systems.

- Output Adjustable from 1.25 V to 40 V
- Peak Output Current of 1.5 A Without External Transistor
- 80 dB Line and Load Regulation
- Operation from 2.5 V to 40 V Supply
- Low Standby Current Drain
- High Gain, High Output Current, Uncommitted Op Amp

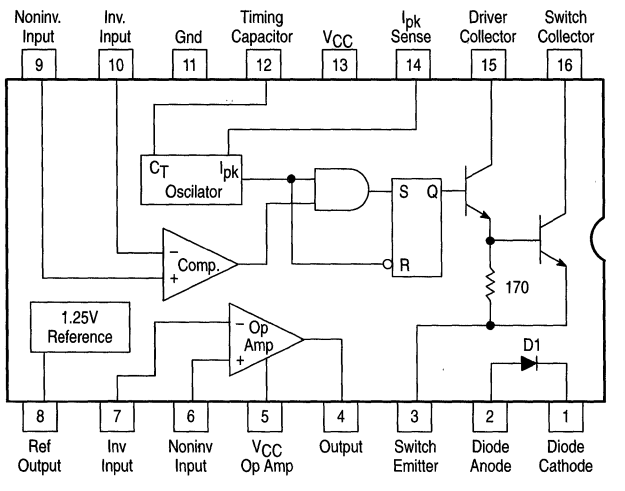
UNIVERSAL SWITCHING REGULATOR SUBSYSTEM

SEMICONDUCTOR TECHNICAL DATA



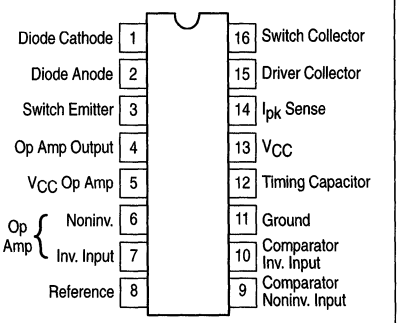
P SUFFIX
PLASTIC PACKAGE
CASE 648

Simplified Block Diagram



(Bottom View)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
μA78S40PC	T_A = 0° to +70°C	Plastic
μA78S40PV	T_A = – 40° to +85°C	Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Op Amp Power Supply Voltage	V_{CC} (Op Amp)	40	V
Common Mode Input Range (Comparator and Op Amp)	V_{ICR}	−0.3 to V_{CC}	V
Differential Input Voltage (Note 2)	V_{ID}	± 30	V
Output Short Circuit Duration (Op Amp)		Continuous	–
Reference Output Current	I_{ref}	10	mA
Voltage from Switch Collectors to Gnd		40	V
Voltage from Switch Emitters to Gnd		40	V
Voltage from Switch Collectors to Emitter		40	V
Voltage from Power Diode to Gnd		40	V
Reverse–Power Diode Voltage	V_{DR}	40	V
Current through Power Switch	I_{SW}	1.5	A
Current through Power Diode	I_D	1.5	A
Power Dissipation and Thermal Characteristics: Plastic Package (T_A = + 25°C) Derate above + 25°C (Note 1)	 P_D $1/R_{\theta JA}$	 1500 14	 mW mW/°C
Storage Temperature Range	T_{stg}	−65 to + 150	°C
Operating Temperature Range μA78S40V μA78S40C	T_A	 −40 to +85 0 to +70	°C

NOTES: 1. T_{low} = −40° for μA78S40PV T_{high} = +85° for μA78S40PV
= 0° for μA78S40PC = +70° for μA78S40PC
2. For supply voltages less than 30 V the maximum differential input voltage (Error Amp and Op Amp) is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC} (Op Amp) 5.0 V, T_A = T_{low} to T_{high}, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Supply Voltage	V_{CC}	2.5	–	40	V
Supply Current (Op Amp V_{CC}, disconnected) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	 – –	 1.8 2.3	 3.5 5.0	mA
Supply Current (Op Amp V_{CC}, connected) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	 – –	 – –	 4.0 5.5	mA
REFERENCE					
Reference Voltage (I_{ref} = 1.0 mA)	V_{ref}	1.180	1.245	1.310	V
Reference Voltage Line Regulation (3.0 V ≤ V_{CC} ≤ 40 V, I_{ref} = 1.0 mA, T_A = 25°C)	Reg_{line}	–	0.04	0.2	mV/V
Reference Voltage Load Regulation (1.0 mA ≤ I_{ref} ≤ 10 mA, T_A = 25°C)	Reg_{load}	–	0.2	0.5	mV/mA

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC} (Op Amp) 5.0 V, T_A = T_{low} to T_{high}, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Charging Current (T_A = 25°C) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{chg}	 20 20	 – –	 50 70	μA
Discharging Current (T_A = 25°C) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{dis}	 150 150	 – –	 250 350	μA
Oscillator Voltage Swing (T_A = 25°C) (V_{CC} = 5.0 V)	V_{osc}	–	0.5	–	V
Ratio of Charge/Discharge Time	t_{chg}/t_{dis}	–	6.0	–	–
CURRENT LIMIT					
Current–Limit Sense Voltage (T_A = 25°C) (V_{CC} – V_{Ipk} Sense)	V_{CLS}	250	–	350	mV
OUTPUT SWITCH					
Output Saturation Voltage 1 (I_{SW} = 1.0 A, Pin 15 tied to Pin 16)	V_{sat1}	–	0.93	1.3	V
Output Saturation Voltage 2 (I_{SW} = 1.0 A, I_{15} = 50 mA)	V_{sat2}	–	0.5	0.7	V
Output Transistor Current Gain (T_A = 25°C) (I_C = 1.0 A, V_{CE} = 5.0 V)	h_{FE}	–	70	–	–
Output Leakage Current (T_A = 25°C) (V_{CE} = 40 V)	$I_{C(off)}$	–	10	–	nA
POWER DIODE					
Forward Voltage Drop (I_D = 1.0 A)	V_D	–	1.25	1.5	V
Diode Leakage Current (T_A = 25°C) (V_{DR} = 40 V)	I_{DR}	–	10	–	nA
COMPARATOR					
Input Offset Voltage (V_{CM} = V_{ref})	V_{IO}	–	1.5	15	mV
Input Bias Current (V_{CM} = V_{ref})	I_{IB}	–	35	200	nA
Input Offset Current (V_{CM} = V_{ref})	I_{IO}	–	5.0	75	nA
Common Mode Voltage Range (T_A = 25°C)	V_{ICR}	0	–	V_{CC} – 2.0	V
Power–Supply Rejection Ratio (T_A = 25°C) (3.0 ≤ V_{CC} ≤ 40 V)	PSRR	70	96	–	dB
OUTPUT OPERATION AMPLIFIER					
Input Offset Voltage (V_{CM} = 2.5 V)	V_{IO}	–	4.0	15	mV
Input Bias Current (V_{CM} = 2.5 V)	I_{IB}	–	30	200	nA
Input Offset Current (V_{CM} = 2.5 V)	I_{IO}	–	5.0	75	nA
Voltage Gain + (T_A = 25°C) (R_L = 2.0 kΩ to Gnd, 1.0 V ≤ V_O ≤ 2.5 V)	A_{VOL}+	25	250	–	V/mV
Voltage Gain – (T_A = 25°C) (R_L = 2.0 kΩ to V_{CC} (Op Amp), 1.0 V ≤ V_O ≤ 2.5 V)	A_{VOL}–	25	250	–	V/mV
Common Mode Voltage Range (T_A = 25°C)	V_{ICR}	0	–	V_{CC} – 2.0	V
Common Mode Rejection Ratio (T_A = 25°C) (V_{CM} = 0 V to 3.0 V)	CMRR	76	100	–	dB
Power–Supply Rejection Ratio (T_A = 25°C) (3.0 V ≤ V_{CC} (Op Amp) ≤ 40 V)	PSRR	76	100	–	dB
Output Source Current (T_A = 25°C)	I_{Source}	75	150	–	mA
Output Sink Current (T_A = 25°C)	I_{Sink}	10	35	–	mA
Slew Rate (T_A = 25°C)	SR	–	0.6	–	V/μs
Output Low Voltage (T_A = 25°C, I_L = –5.0 mA)	V_{OL}	–	–	1.0	V
Output High Voltage (T_A = 25°C, I_L = 50 mA)	V_{OH}	V_{CC}(Op Amp) – 3.0	–	–	V

Figure 1. Output Switch On/Off Time versus Oscillator Timing Capacitor

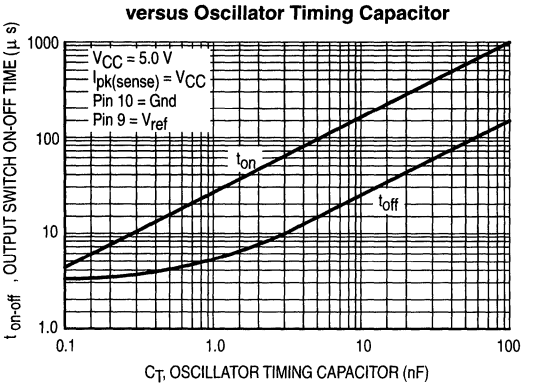


Figure 2. Standby Supply Current versus Supply Voltage

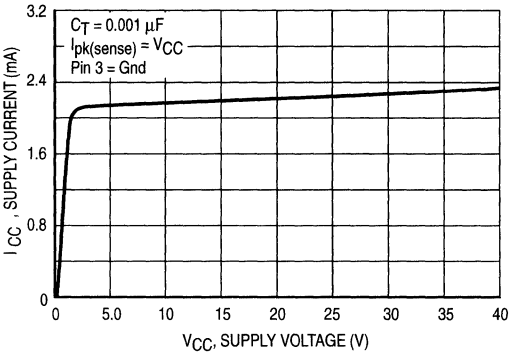


Figure 3. Emitter–Follower Configuration Output Switch Saturation Voltage versus Emitter Current

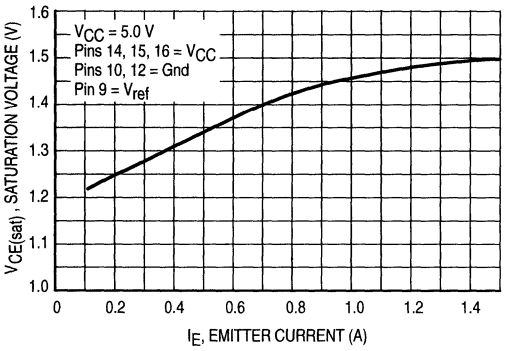
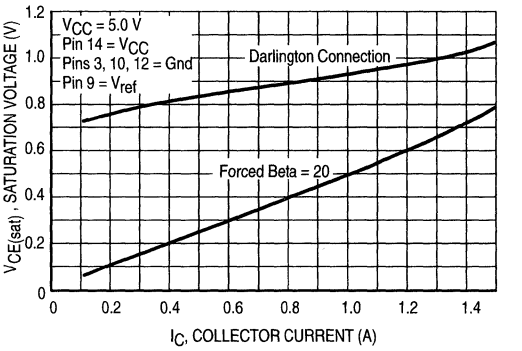


Figure 4. Common–Emitter Configuration Output Switch Saturation Voltage versus Collector Current



3

Figure 5. Step–Down Converter

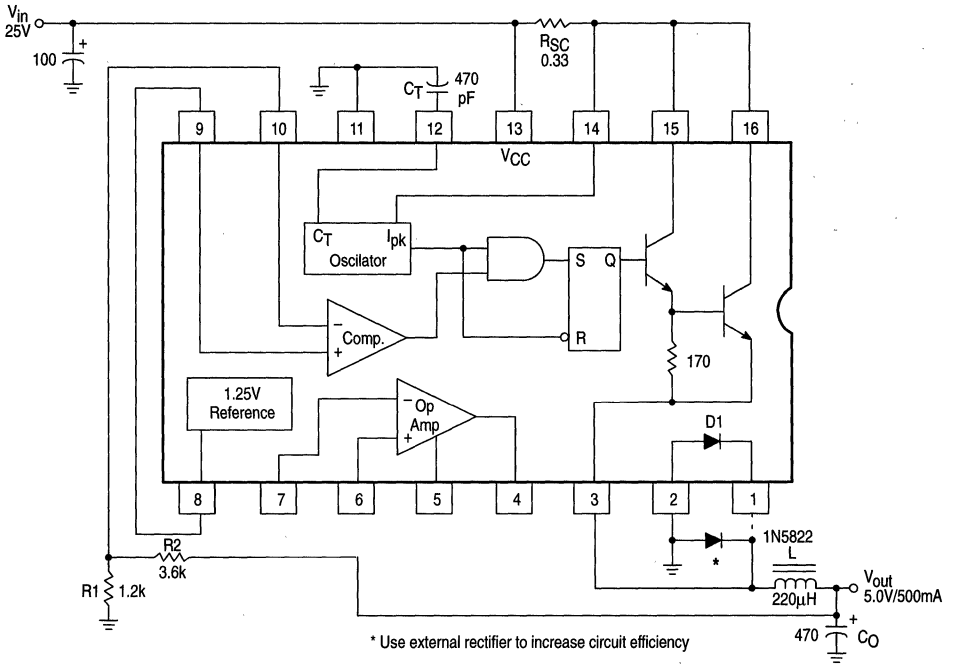


Figure 6. Step–Up Converter

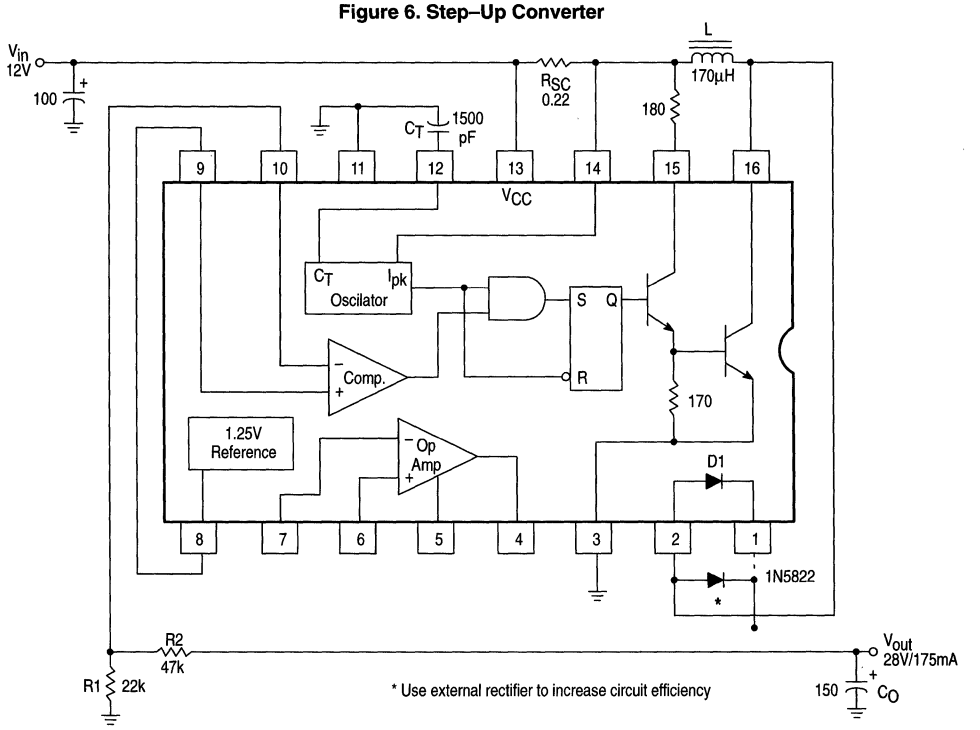
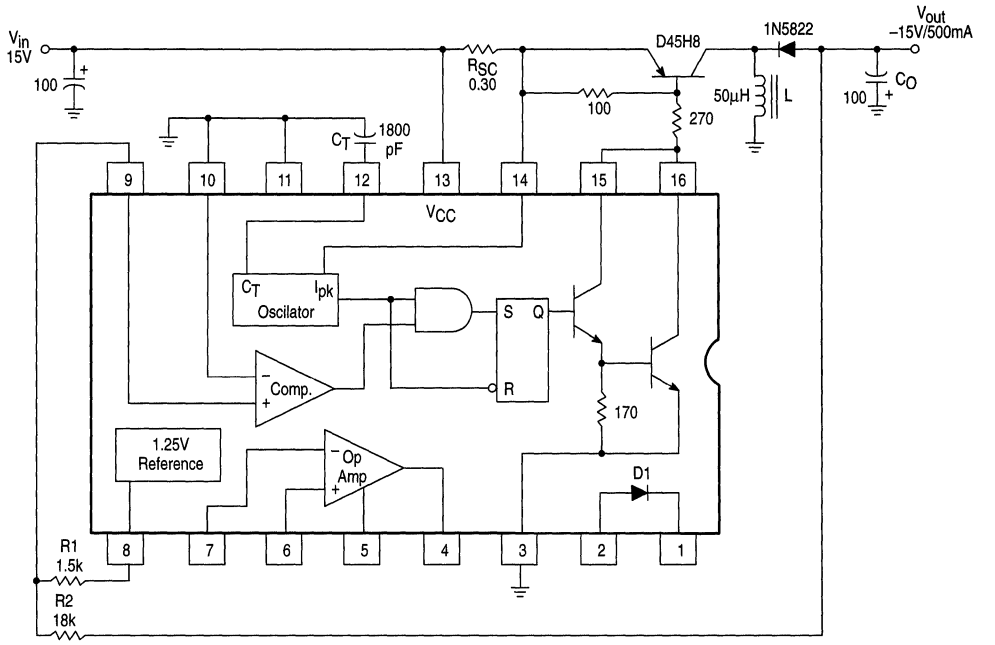


Figure 7. Inverting Converter



Design Formula Table

Calculation	Step–Down	Step–Up	Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} - V_F \quad V_{in(min)}}{V_{in(min)} \quad V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat}}$
$(t_{on} + t_{off})$ max	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4 \times 10^5 t_{on}$	$4 \times 10^5 t_{on}$	$4 \times 10^5 t_{on}$
$I_{pk(switch)}$	$2 I_{out(max)}$	$2 I_{out(max)} \left(\frac{t_{on} - t_{off}}{t_{off}}\right)$	$2 I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$
R_{SC}	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$\frac{I_{pk(switch)} (t_{on} + t_{off})}{8 V_{ripple(pp)}}$	$\approx \frac{I_{out} t_{on}}{V_{ripple}}$	$\approx \frac{I_{out} t_{on}}{V_{ripple}}$

V_{sat} = Saturation voltage of the output switch. V_F = Forward voltage drop of the ringback rectifier.

The following power supply characteristics must be chosen:

V_{in} – Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step–down and $V_{in(min)}$ for step–up and inverting convertor.

V_{out} – Desired output voltage: $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1}\right)$ for step–down and step–up: $V_{out} = \frac{1.25\ R_2}{R_1}$ for inverting.

I_{out} – Desired output current.

f_{min} – Minimum desired output switching frequency at the selected values for V_{in} and I_O.

$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

See Application Note AN920 for further information

3

Addendum
Linear & Switching Voltage Regulator Applications Information

In Brief . . .

In most electronic systems, voltage regulation is required for various functions. Today's complex electronic systems are requiring greater regulating performance, higher efficiency and lower parts count. Present integrated circuit and power package technology has produced IC voltage regulators which can ease the task of regulated power supply design, provide the performance required and remain cost effective. Available in a growing variety, Motorola offers a wide range of regulator products from fixed and adjustable voltage types to special–function and switching regulator control ICs.

This handbook describes Motorola's voltage regulator products and provides information on applying these products. Basic Linear regulator theory and switching regulator topologies have been included along with practical design examples. Other relevant topics include trade–offs of Linear versus switching regulators, series pass elements for Linear regulators, switching regulator component design considerations, heatsinking, construction and layout, power supply supervision and protection, and reliability.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

SECTION 1
BASIC LINEAR REGULATOR THEORY

3

A. IC Voltage Regulator

The basic functional block diagram of an integrated circuit voltage regulator is shown in Figure 1–1. It consists of a stable reference, whose output voltage is V_{ref}, and a high gain error amplifier. The output voltage (V_O), is equal to or a multiple of V_{ref}. The regulator will tend to keep V_O constant by sensing any changes in V_O and trying to return it to its original value. Therefore, the ideal voltage regulator could be considered a voltage source with a constant output voltage. However, in practice the IC regulator is better represented by the model shown in Figure 1–2.

In this figure, the regulator is modeled as a voltage source with a positive output impedance (Z_O). The value of the voltage source (V) is not constant; instead it varies with changes in supply voltage (V_{CC}) and with changes in IC junction temperature (T_J) induced by changes in ambient temperature and power dissipation. Also, the regulator output voltage (V_O) is affected by the voltage drop across Z_O, caused by the output current (I_O). In the following text, the reference and amplifier sections will be described, and their contributions to the changes in the output voltage analyzed.

B. Voltage Reference

Naturally, the major requirement for the reference is that it be stable; variations in supply voltage or junction temperature should have little or no effect on the value of the reference voltage (V_{ref}).

1. Zener Diode Reference

The simplest form of a voltage reference is shown in Figure 1–3a. It consists of a resistor and a zener diode. The zener voltage (V_Z) is used as the reference voltage. In order to determine V_Z, consider Figure 1–3b. The zener diode (VR1) of Figure 1–3a has been replaced with its equivalent circuit model and the value of V_Z is therefore given by (at a constant junction temperature):

$$V_Z = V_{BZ} + I_Z Z_Z = V_{BZ} + \left(\frac{V_{CC} - V_{BZ}}{R + Z_Z}\right) Z_Z \qquad (1)$$

where: V_{BZ} = zener breakdown voltage
I_Z = zener current
Z_Z = zener impedance at I_Z.

Note that changes in the supply voltage give rise to changes in the zener current, thereby changing the value of the reference voltage (V_Z).

Figure 1–1. Voltage Regulator Functional Block Diagram

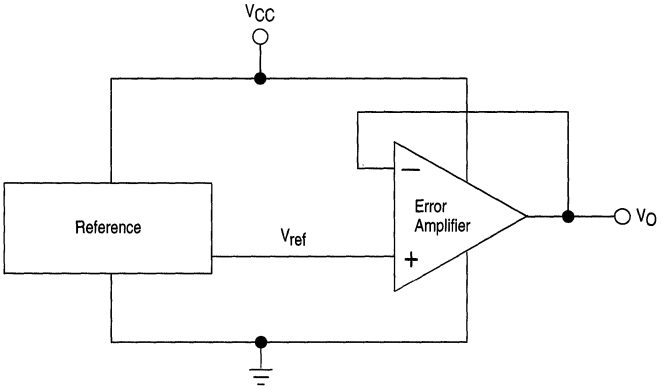


Figure 1–2. Voltage Regulator Equivalent Circuit Model

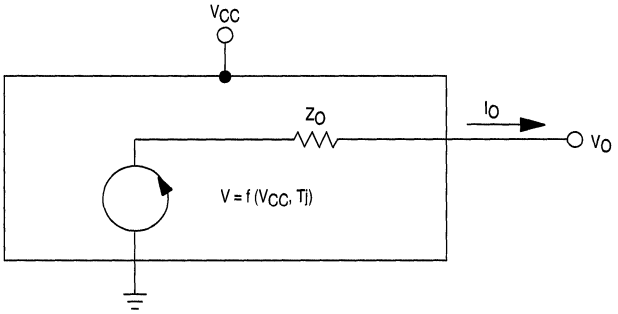
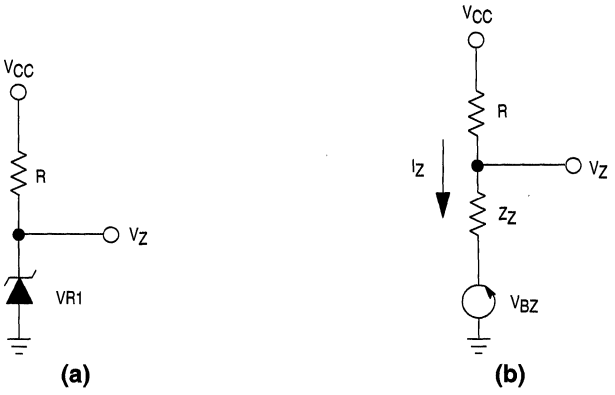


Figure 1–3. Zener Diode Reference



2. Constant Current — Zener Reference

The effect of zener impedance can be minimized by driving the zener diode with a constant current as shown in Figure 1–4. The value of the zener current is largely independent of V_{CC} and is given by:

$$I_Z = \frac{V_{BEQ1}}{R_{SC}} \quad (2)$$

where: V_{BEQ1} = base–emitter voltage of Q1.

This gives a reference voltage of:

$$V_{ref} = V_Z + V_{BEQ1} = V_{BZ} + I_Z Z_Z + V_{BEQ1} \quad (3)$$

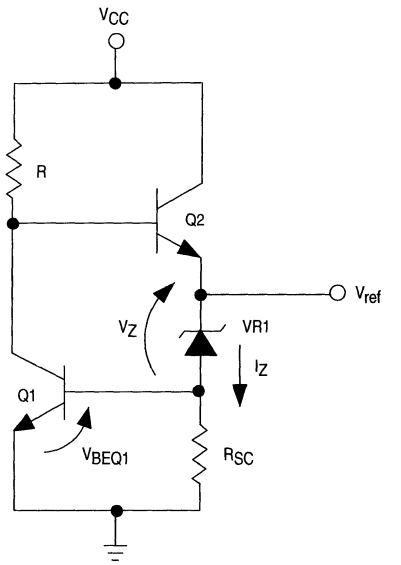
where I_Z is constant and given by Equation 2.

The reference voltage (about 7.0 V) of this configuration is therefore largely independent of supply voltage variations. This configuration has the additional benefit of better temperature stability than that of a simple resistor–zener reference.

Referring back to Figure 1–3a, it can be seen that the reference voltage temperature stability is equal to that of the zener diode, VR1. The stability of zener diodes used in most integrated circuitry is about + 2.2 mV/°C or ≃ 0.04%/°C (for a 6.2 V zener). If the junction temperature varies 100°C, the zener or reference voltage would vary 4%. A variation this large is usually unacceptable.

However, the circuit of Figure 1–4 does not have this drawback. Here the positive 2.2 mV/°C temperature coefficient (TC) of the zener diode is offset by the negative 2.2 mV/°C TC of the V_{BE} of Q1. This results in a reference voltage with very stable temperature characteristics.

Figure 1–4. Constant Current (Zener Reference)



3. Bandgap Reference

Although very stable, the circuit of Figure 1–4 does have a disadvantage in that it requires a supply voltage of 9.0 V or more. Another type of stable reference which requires only a few volts to operate was described by Widlar[1] and is shown in Figure 1–5. In this circuit V_{ref} is given by:

$$V_{ref} = V_{BEQ3} + I_2R_2 \tag{4}$$

where: $$I_2 = \frac{V_{BEQ1} - V_{BEQ2}}{R_1}$$ (neglecting base currents)

The change in V_{ref} with junction temperature is given by:

$$\Delta V_{ref} = \Delta V_{BE3} + \left\{ \frac{\Delta V_{BEQ1} - \Delta V_{BEQ2}}{R_1} \right\} R_2 \tag{5}$$

It can be shown that,

$$\Delta V_{BEQ1} = \Delta T_J K \ln I_1 \tag{6}$$

and, $$\Delta V_{BEQ2} = \Delta T_J K \ln I_2 \tag{7}$$

where: K = a constant

ΔT_J = change in junction temperature

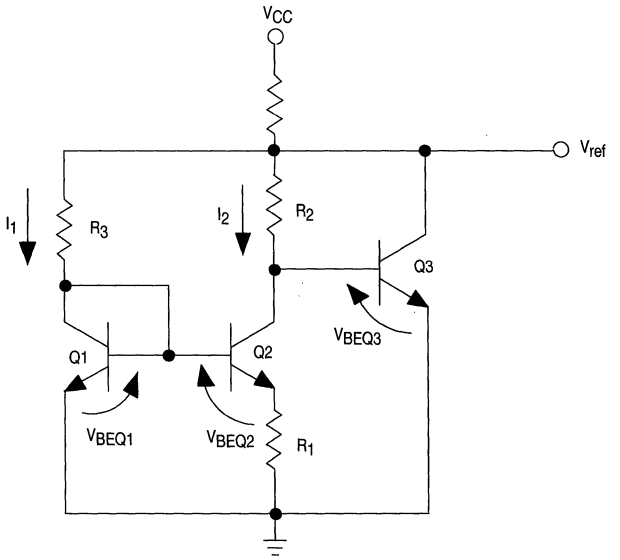
and, $I_1 > I_2$

Combining (5), (6), and (7)

$$\Delta V_{ref} = \Delta V_{BEQ3} + \Delta T_J K \left(\frac{R_2}{R_1} \right) \ln \frac{I_1}{I_2} \tag{8}$$

Since ΔV_{BEQ3} is negative, and with $I_1 > I_2$, $\ln I_1/I_2$ is positive, the net change in V_{ref} with temperature variations can be made to equal zero by appropriately selecting the values of I_1, R_1, and R_2.

Figure 1–5. Bandgap Reference



C. The Error Amplifier

Given a stable reference, the error amplifier becomes the determining factor in integrated circuit voltage regulator performance. Figure 1–6 shows a typical differential error amplifier in a voltage regulator configuration. With a constant supply voltage (V_{CC}) and junction temperature, the output voltage is given by:

$$V_O = A_{VOL}\, \upsilon_i - Z_{OL}\, I_O = A_{VOL}\, \{(V_{ref} \pm V_{IO}) - V_O\, \beta\} - Z_{OL}\, I_O \quad (9)$$

where: A_{VOL} = amplifier open loop gain

V_{IO} = input offset voltage

Z_{OL} = open loop output impedance

$\beta = \dfrac{R_1}{R_1 + R_2}$ = feedback ratio (β is always ≤ 1)

I_O = output current

υ_i = true differential input voltage

Manipulating Equation 9:

$$V_O = \frac{(V_{ref} \pm V_{IO}) - \dfrac{Z_{OL}}{A_{VOL}}\, I_O}{\beta + \dfrac{1}{A_{VOL}}} \quad (10)$$

Note that if the amplifier open loop gain is infinite, this expression reduces to:

$$V_O = \frac{1}{\beta}\, (V_{ref} \pm V_{IO}) = (V_{ref} \pm V_{IO}) \left(1 + \frac{R_2}{R_1}\right) \quad (11)$$

The output voltage can thus be set any value equal to or greater than ($V_{ref} \pm V_{IO}$). Note also that if A_{VOL} is not infinite, with constant output current (a non–varying output load), the output voltage can still be "tweaked–in" by varying R_1 and R_2, even though V_O will not exactly equal that given by Equation 11.

Assuming a stable reference and a finite value of A_{VOL}, inaccuracy of the output voltage can be traced to the following amplifier characteristics:

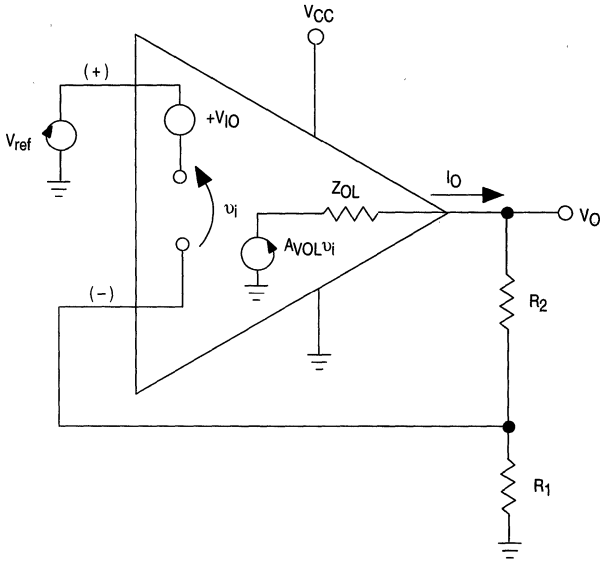
1. Amplifier Input Offset Voltage Drift

The input transistors of integrated circuit amplifiers are usually not perfectly matched. As in operational amplifiers, this is expressed in terms of an input offset voltage (V_{IO}). At a given temperature, this effect can be nulled out of the desired output voltage by adjusting V_{ref} or $1/\beta$. However, V_{IO} drifts with temperature, typically $\pm 5.0\ \mu V/°C$ to $+15\ \mu V/°C$, causing a proportional change in the output voltage. Closer matching of the internal amplifier input transistors minimizes this effect, as does selecting a feedback ratio (β) to be close to unity.

2. Amplifier Power Supply Sensitivity

Changes in regulator output voltage due to power supply voltage variations can be attributed to two amplifier performance parameters: power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR). In modern integrated circuit regulator amplifiers, the utilization of constant current sources gives such large values of PSRR that this effect on V_O can usually be neglected. However, supply voltage changes can affect the output voltage since these changes appear as common mode voltage changes, and they are best measured by the CMRR.

Figure 1–6. Typical Voltage Regulator Configuration



The definition of common mode voltage (V_{CM}), illustrated by Figure 1–7a, is:

$$V_{CM} = \left[\frac{V_1 + V_2}{2}\right] - \left[\frac{(V+) + (V-)}{2}\right] \quad (12)$$

where: V_1 = voltage on amplifier noninverting input
V_2 = voltage on amplifier inverting input
$V+$ = positive supply voltage
$V-$ = negative supply voltage

Figure 1–7. Definition of Common Mode Voltage Error

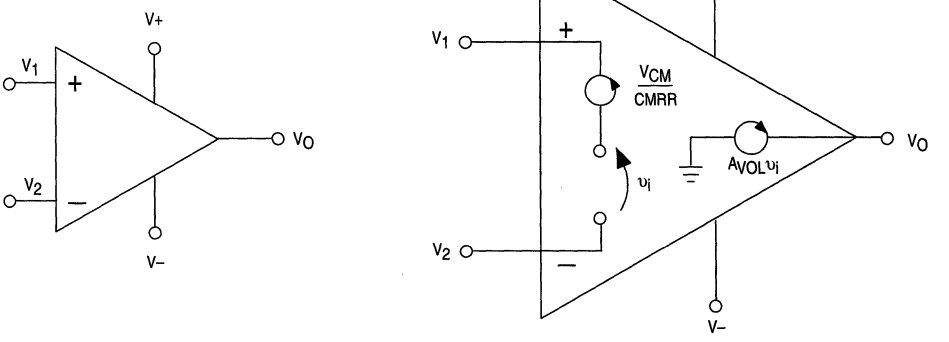
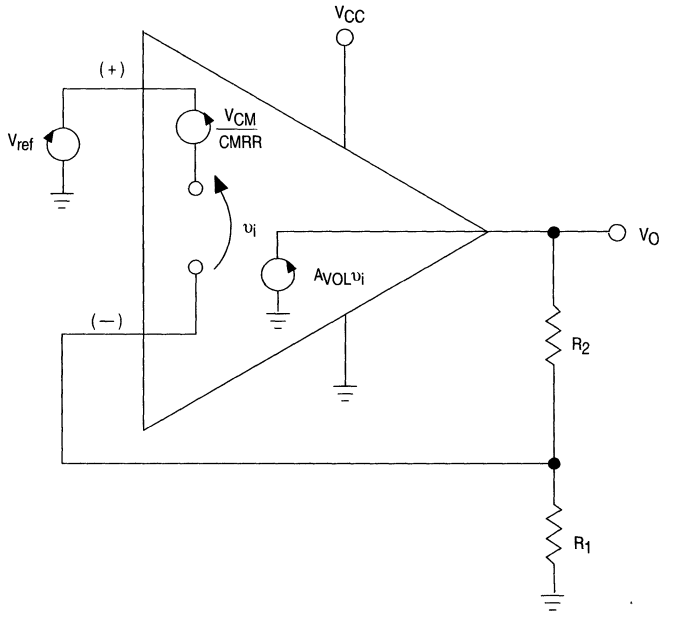


Figure 1–8. Common Mode Regulator Effects



In an ideal amplifier, only the differential input voltage ($V_1 - V_2$) has any effect on the output voltage; the value of V_{CM} would not effect the output. In fact, V_{CM} does influence the amplifier output voltage. This effect can be modeled as an additional voltage offset at the amplifier input equal to $V_{CM}/CMRR$ as shown in Figures 1–7b and 1–8. The latter figure is the same configuration as Figure 1–6, with amplifier input offset voltage and output impedance deleted for clarity and common mode voltage effects added. The output voltage of this configuration is given by:

$$V_O = A_{VOL}\,\upsilon_i = A_{VOL}\left(V_{ref} - \frac{V_{CM}}{CMRR} - \beta V_O\right) \tag{13}$$

Manipulating,

$$V_O = \frac{\left(V_{ref} - \frac{V_{CM}}{CMRR}\right)}{\beta + \frac{1}{A_{VOL}}} \tag{14}$$

where: $$V_{CM} = V_{ref} - \frac{V_{CC}}{2} \tag{15}$$

and, CMRR = common mode rejection ratio

It can be seen from Equations (14) and (15) that the output can vary when V_{CC} varies. This can be reduced by designing the amplifier to have a high A_{VOL}, a high CMRR, and by choosing the feedback ratio (β) to be unity.

3. Amplifier Output Impedance

Referring back to Equation (9), it can be seen that the equivalent regulator output impedance (Z_O) is given by:

$$Z_O = \frac{\Delta V_O}{\Delta I_O} \simeq \frac{Z_{OL}}{\beta A_{VOL}} \tag{16}$$

3

This impedance must be as low as possible, in order to minimize load current effects on the output voltage. This can be accomplished by lowering Z_{OL}, choosing an amplifier with high A_{VOL}, and by selecting the feedback ratio (β) to be unity.

A simple way of lowering the effective value of Z_{OL} is to make an impedance transformation with an emitter follower, as shown in Figure 1–9. Given a change in output current (ΔI_O) the amplifier will see a change of only $\Delta I_O/h_{FEQ1}$ in its output current (I_O'). Therefore, (Z_{OL}) in Equation (16) has been effectively reduced to Z_{OL}/h_{FEQ1}, reducing the overall regulator output impedance (Z_O).

D. The Regulator within a Regulator Approach

In the preceding text, we have analyzed the sections of an integrated circuit voltage regulator and determined how they contribute to its non–ideal performance characteristics. These are shown in Table 1–1 along with procedures which minimize their effects.

It can be seen that in all cases regulator performance can be improved by selecting A_{VOL} as high as possible and $\beta = 1$. Since a limit is soon approached in how much A_{VOL} can be practically obtained in an integrated circuit amplifier, selecting a feedback ratio (β) equal to unity is the only viable way of improving total regulator performance, especially in reducing regulator output impedance. However, this method presents a basic problem to the regulator designer. If the configuration of Figure 1–6 is used, the output voltage cannot be adjusted to a value other than V_{ref}. The solution is to utilize a different regulator configuration known as the *regulator within a regulator* approach.[2] Its greatest benefit is in reducing total regulator output impedance.

Figure 1–9. Emitter Follower Output

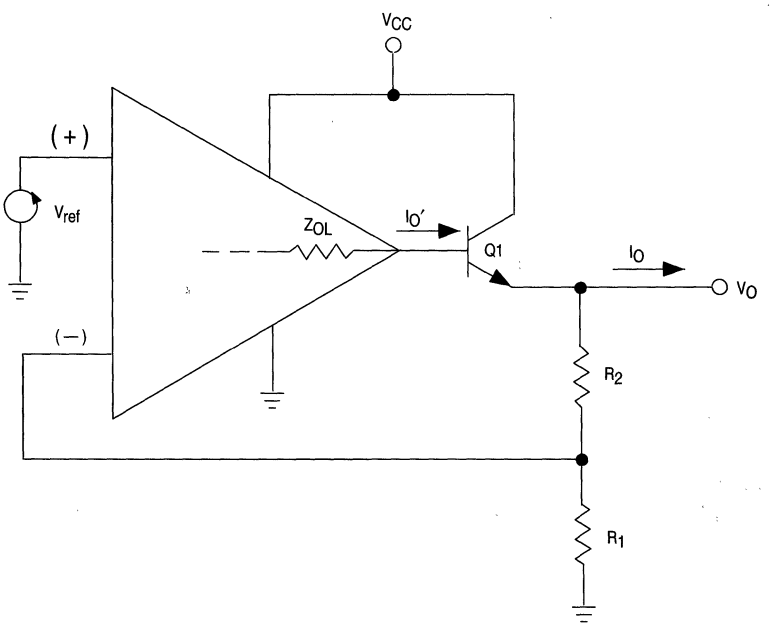


Table 1–1

V_O Changes Section	Effect Can Be Induced By:	Minimized By Selecting:
Reference	V_{CC}	• Constant current–zener method • Bandgap reference
	T_J	• Bandgap reference • TC compensated zener method
Amplifier	V_{CC}	• High CMRR amplifier • High A_{VOL} amplifier • $\beta = 1$
	T_J	• Low V_{IO} drift amplifier • High A_{VOL} amplifier • $\beta = 1$
	I_O	• Low Z_{OL} amplifier • High A_{VOL} amplifier • Additional emitter follower output • $\beta = 1$

3

As shown in Figure 1–10, amplifier A1 sets up a voltage (V_1) given by:

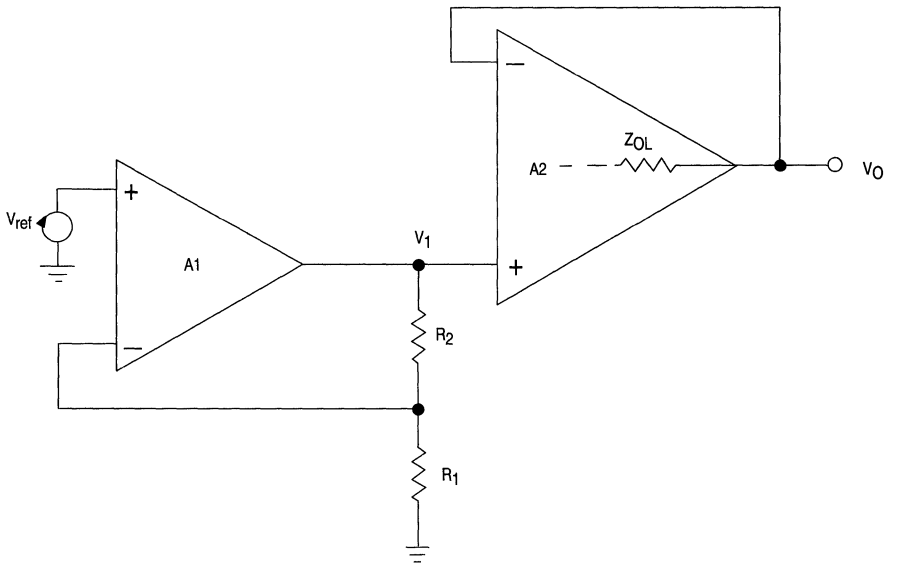
$$V_1 \simeq V_{ref}\left(1 + \frac{R_2}{R_1}\right) \tag{17}$$

V_1 now serves as the reference voltage for amplifier A2, whose output voltage (V_O) is given by:

$$V_O \simeq V_1 \simeq V_{ref}\left(1 + \frac{R_2}{R_1}\right) \tag{18}$$

Note that the output impedance of A2, and therefore the regulator output impedance, has been minimized by selecting A2's feedback factor to be unity; and that output voltage can still be set at voltages greater than V_{ref} by adjusting R_1 and R_2.

Figure 1–10. The "Regulator within a Regulator" Configuration



(1)Widlar, R. J., *New Developments in IC Voltage Regulators*, IEEE Journal of Solid State Circuits, Feb.1971, Vol. SC–6, pgs. 2–7.
(2)Tom Fredericksen, IEEE Journal of Solid State Circuits, Vol. SC–3, Number 4, Dec. 1968, *A Monolithic High Power Series Voltage Regulator.*

3

SECTION 2
SELECTING A LINEAR IC VOLTAGE REGULATOR

A. Selecting the Type of Regulator

There are five basic linear regulator types; positive, negative, fixed output, tracking and floating regulators. Each has its own particular characteristics and best uses, and selection depends on the designer's needs and trade–offs in performance and cost.

1. Positive Versus Negative Regulators

In most cases, a positive regulator is used to regulate positive voltages and a negative regulator negative voltages. However, depending on the system's grounding requirements, each regulator type may be used to regulate the "opposite" voltage.

Figures 2–1a and 2–1b show the regulators used in the conventional and obvious mode. Note that the ground reference for each (indicated by the heavy line) is continuous. Several positive regulators could be used with the same input supply to deliver several voltages with common grounds; negative regulators may be utilized in a similar manner.

If no other common supplies or system components operate off the input supply to the regulator, the circuits of Figures 2–1c and 2–1d may be used to regulate positive voltages with a negative regulator and vice versa. In these configurations, the input supply is essentially floated, i.e., neither side of the input is tied to the system ground.

There are methods of utilizing positive regulators to obtain negative output voltages without sacrificing ground bus continuity. However, these methods are only possible at the expense of increased circuit complexity and cost. An example of this technique is shown in Section 3.

2. Three–Terminal, Fixed Output Regulators

These regulators offer the designer a simple, inexpensive way to obtain a source of regulated voltage. They are available in a variety of positive or negative output voltages and current ranges.

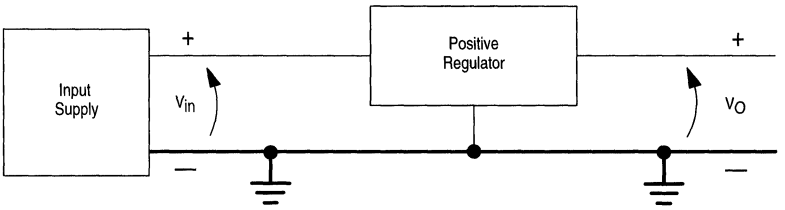
The advantages of these regulators are:

a) Easy to use.
b) Internal overcurrent and thermal protection.
c) No circuit adjustments necessary.
d) Low cost.

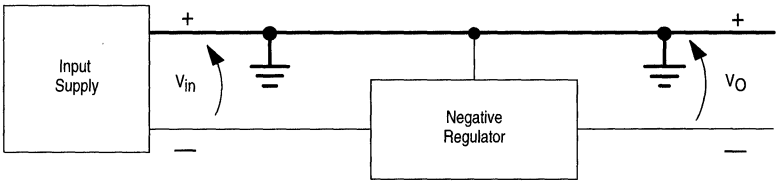
Their disadvantages are:

a) Output voltage cannot be precisely adjusted. (Methods for obtaining adjustable outputs are shown in Section 3).
b) Available only in certain output voltages and currents.
c) Obtaining greater current capability is more difficult than with other regulators. (Methods for obtaining greater output currents are shown in Section 3.)

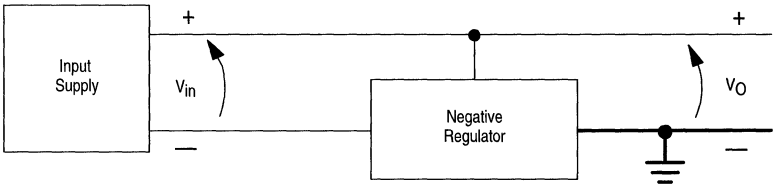
Figure 2–1. Regulator Configurations



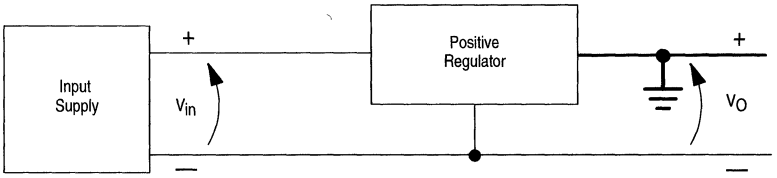
(a) Positive Output Using Positive Regulator



(b) Negative Output Using Negative Regulator



(c) Positive Output Using Negative Regulator



(d) Negative Output Using Positive Regulator

3. Three–Terminal, Adjustable Output Regulators

Like the three–terminal fixed regulators, the three–terminal adjustable regulators are easy and inexpensive to use. These devices provide added flexibility with output voltage adjustable over a wide range, from 1.2 V to nearly 40 V, by means of an external, two–resistor voltage divider. A variety of current ranges from 100 mA to 3.0 A are available.

3

B. Selecting an IC Regulator

Once the type of regulator is decided upon, the next step is to choose a specific device. To provide higher currents than are available from monolithic technologies, an IC regulator will often be used as a driver to a boost transistor. This complicates the selection and design task, as there are now several overlapping solutions to many of the design problems.

Unfortunately, there is no exact step–by–step procedure that can be followed which will lead to the ideal regulator and circuit configuration for a specific application. The regulating circuit that is finally accepted will be a compromise between such factors as performance, cost, size and complexity. Because of this, the following general design procedure is suggested:

1. Select the regulators which meet or exceed the requirements for line regulation, load regulation, TC of the output voltage and operating ambient temperature range. At this point, do not be overly concerned with the regulator capabilities in terms of output voltage, output current, SOA and special features.

2. Next, select application circuits from Section 3 which meet the requirements for output current, output voltage, special features, etc. Preliminary designs using the chosen regulators and circuit configurations are then possible. From these designs a judgement can be made by the designer as to which regulator circuit configuration combination best meets his or her requirements in terms of cost, size and complexity.

SECTION 3
LINEAR REGULATOR CIRCUIT CONFIGURATION AND DESIGN CONSIDERATIONS

Once the IC regulators, which meet the designer's performance requirements, have been selected, the next step is to determine suitable circuit configurations. Initial designs are devised and compared to determine the IC regulator/circuit configuration that best meets the designer's requirements. In this section, several circuit configurations and design equations are given for the various regulator ICs. Additional circuit configurations can be found on the device data sheets. Organization is first by regulator type and then by variants, such as current boost. Each circuit diagram has component values for a particular voltage and current regulator design.

A. Positive, Adjustable
B. Negative, Adjustable
C. Positive, Fixed
D. Negative, Fixed
E. Tracking
F. Special
    1. Obtaining Extended Output Voltage Range
    2. Electronic Shutdown
G. General Design Considerations

It should be noted that all circuit configurations shown have constant current limiting. If foldback limiting is desired, see Section 4C for techniques and design equations.

A. Positive, Adjustable Output IC Regulator Configurations

1. Basic Regulator Configurations

Positive Three–Terminal Adjustables

These adjustables, comprised of the LM317L, LM317, and LM350 series devices range in output currents of 100 mA, 500 mA, 1.5 A, and 3.0 A respectively. All of these devices utilize the same basic circuit configuration as shown in Figure 3–1A.

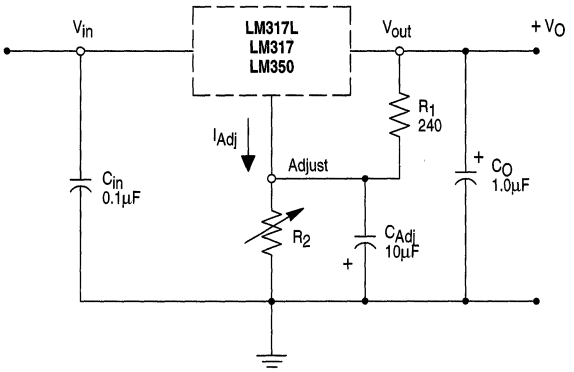
MC1723C

The basic circuit configurations for the MC1723C regulator are shown in Figures 3–2A and 3–3A. For output voltages from ≃ 7.0 V to 37 V the configuration of Figure 3–2A can be used, while Figure 3–3A can be used to obtain output voltages from 2.0 V to ≃ 7.0 V.

2. Output Current Boosting

If output currents greater than those available from the basic circuit configurations are desired, the current boost circuits shown in this section can be used. The output currents which can be obtained with this configurations are limited only by capabilities of the external pass element(s).

Figure 3–1A. Basic Configuration for Positive, Adjustable Output Three–Terminal Regulators



C_{in}: required if regulator is located an appreciable distance from power supply filter.

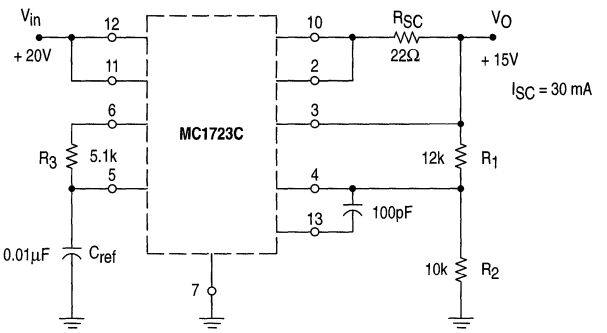
C_O: improves transient response.

C_{Adj}: improves Ripple Rejection.

$$V_{out} = 1.25\ V\ \left(1 + \left(\frac{R_2}{R_1}\right)\right) + I_{Adj}\ R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

Figure 3–2A. MC1723C Basic Circuit Configuration for $V_{ref} \leq V_O \leq 37$ V



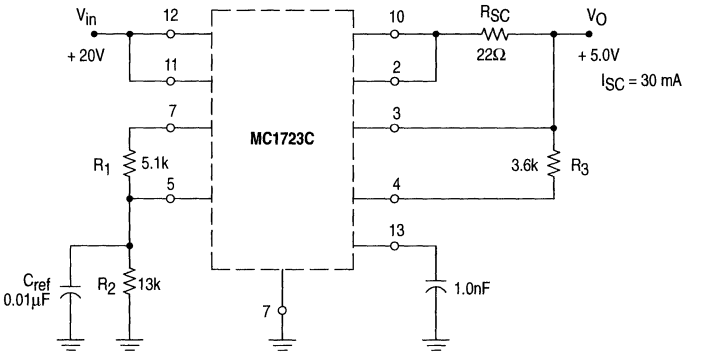
$$R_{SC} \cong \frac{0.66\ V}{I_{SC}}\ ;\ 10\ k\Omega < R_1 + R_2 < 100\ k\Omega$$

$$R_3 \cong R_1 \parallel R_2\ ;\ 0 \leq C_{ref} \leq 0.1\ \mu F$$

$$R_2 = \frac{V_{ref}}{V_O}\ (R_1 + R_2) \approx \frac{7.0\ V}{V_O}\ (R_1 + R_2)$$

Values shown are for a 15 V, 30 mA regulator using an MC1723CP for a $T_{A(max)} = 25°C$.

Figure 3–3A. MC1723C Basic Circuit Configuration for 2.0 V ≤ V_O ≤ V_{ref}



$$R_{SC} \simeq \frac{0.66V}{I_{SC}} \; ; \; 10\,k\Omega < R_1 + R_2 < 100\,k\Omega$$

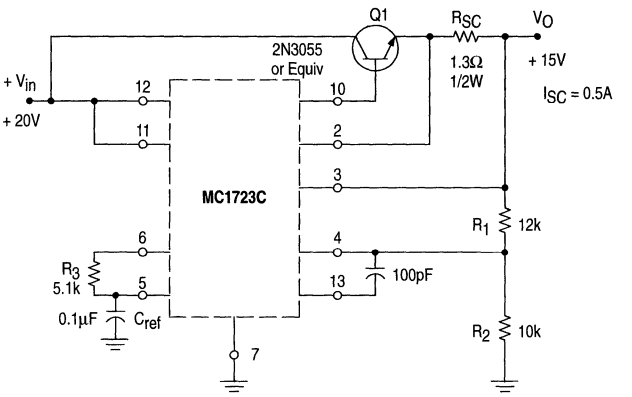
$$R_2 = \frac{V_O}{V_{ref}} (R_1 + R_2) \simeq \frac{V_O}{7.0\,V} (R_1 + R_2)$$

$$R_3 = R_1 \,||\, R_2; \; 0 \le C_{ref} \le 0.1\,\mu F$$

Values shown are for a 5.0 V, 30 mA regulator using an MC1723CP for a $T_{A(max)}$ = 70°C.

To obtain greater output currents with the MC1723C the configurations shown in Figures 3–4A and 3–5A can be used. Figure 3–4A uses an NPN external pass element, while a PNP is used in Figure 3–5A.

Figure 3–4A. MC1723C NPN Boost Configuration



$$R_{SC} \cong \frac{0.66\,V}{I_{SC}} \; ; \; 10\,k\Omega < R_1 + R_2 < 100\,k\Omega$$

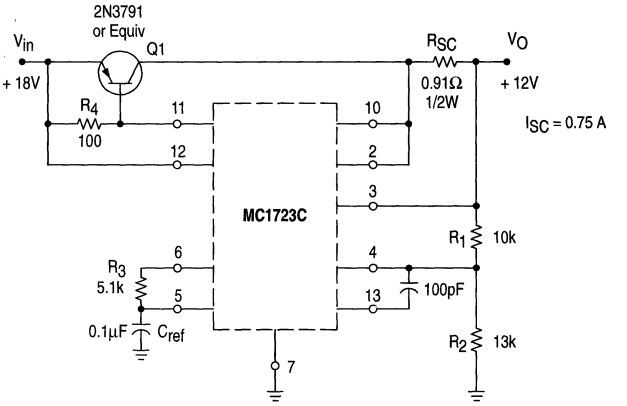
$$R_2 = \frac{V_{ref}}{V_O} (R_1 + R_2) \cong \frac{7.0\,V}{V_O} (R_1 + R_2)$$

$$0 \le C_{ref} \le 0.1\,\mu F \; ; \; R_3 \cong R_1 \,||\, R_2$$

Selection of Q1 based on considerations of Section 4.

Values shown are for a 15 V, 500 mA regulator using an unheatsinked MC1723CP and a 2N3055 on a 6°C/W heatsink for T_A up to + 70°C.

Figure 3–5A. MC1723C PNP Boost Configuration



$$R_{SC} \cong \frac{0.66\ V}{I_{SC}} \; ; \; 10\ k\Omega < R_1 + R_2 < 100\ k\Omega \; ; \; 0 \le C_{ref} \le 0.1\ \mu F$$

$$R_2 = \frac{V_{ref}}{V_O}(R_1 + R_2) \cong \frac{7.0\ V}{V_O}(R_1 + R_2)$$

$$R_3 = R_1 \parallel R_2$$

$$0 < R_4 \le V_{BE_{on}\,(Q1)} / 5.0\ mA$$

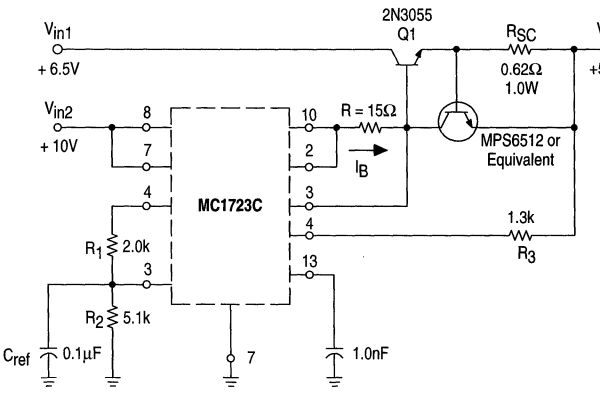
Selection of Q1 based on considerations of Section 4.

Values shown are for a 12 V, 750 mA regulator using an unheatsinked MC1723CP and a 2N3791 on a 4°C/W heatsink for T_A up to + 70°C.

3. High Efficiency Regulator Configurations

When large output currents at voltages under approximately 9.0 V are desired, the configuration of Figure 3–6A can be utilized to obtain increased operating efficiency. This is accomplished by providing a separate low voltage input supply for the pass element. This method, however, usually necessitates that separate short circuit protection be provided for the IC regulator and external pass element. Figure 3–6A shows a high efficiency regulator configuration for the MC1723C.

Figure 3–6A. MC1723C High Efficiency Regulator Configuration



$$R_{SC} \cong \frac{0.6\ V}{I_{SC}}$$

$$R \cong \frac{0.66\ V}{I_{b(max)}} \; ; \; 10\ k\Omega < R_1 + R_2 < 100\ k\Omega$$

$$R_2 = \frac{V_O}{V_{ref}}(R_1 + R_2) \cong \frac{V_O}{7.0\ V}(R_1 + R_2)$$

$$0 \le C_{ref} \le 0.1\ \mu F$$

$$R_3 \cong R_1 \parallel R_2$$

See Section 3F for general design considerations.
Selection of Q1 based on considerations of Section 4.

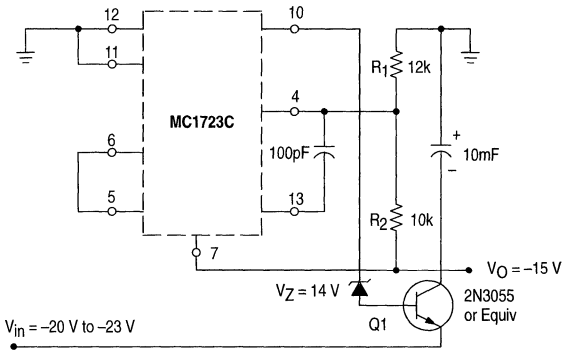
Values shown for a 5.0 V, 1.0 A regulator using an unheatsinked MC1723CP and a 2N3055 on a 10°C/W heatsink for T_A up to + 70°C.

B. Negative, Adjustable Output IC Regulator Configurations

1. Basic Regulator Configurations (MC1723C)

Although a positive regulator, the MC1723C can be used in a negative regulator circuit configuration. This is done by using an external pass element and a zener level shifter as shown in Figure 3–1B. It should be noted that for proper operation, the input supply must not vary over a wide range, since the correct value for V_Z depends directly on this voltage. In addition, it should be noted that this circuit will not operate with a shorted output.

Figure 3–1B. MC1723C Negative Regulator Configuration



$$|V_O| \geq 10\ V;\ 10\ k\Omega \leq R_1 + R_2 \leq 100\ k\Omega$$

$$R_2 = \frac{V_{ref}}{|V_O|}\ (R_1 + R_2) \cong \frac{7.0\ V}{|V_O|}\ (R_1 + R_2)$$

$$V_Z \leq |V_{in}| - V_{BE(Q1)} - 3.0\ V;\ V_Z \geq |V_{in}| - |V_O| - V_{BE(Q1)} + 6.0\ V$$

Selection of Q1 based on considerations of Section 4.

Values shown are for a –15 V, 750 mA regulator using the MC1723CP with Q1 mounted on a 20°C/W heatsink at T_A up to +70°C. **Do not short circuit output.**

C. Positive, Fixed Output IC Regulator Configurations

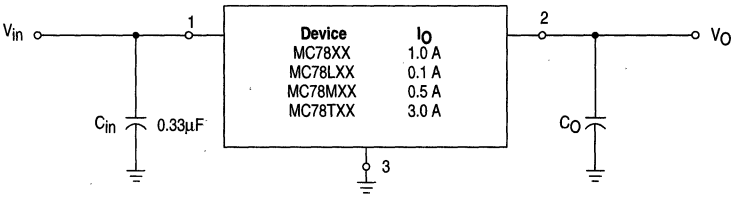
1. Basic Regulator Configuration

The basic current configuration for the positive three–terminal regulators is shown in Figure 3–1C. Depending on which regulator type is used, this configuration can provide output currents in excess of 3.0 A.

2. Output Current Boosting

Figure 3–2C illustrates a method for obtaining greater output currents with the three–terminal positive regulators. Although any of these regulators may be used, usually it is most economical to use the 1.0 A MC7800C in this configuration.

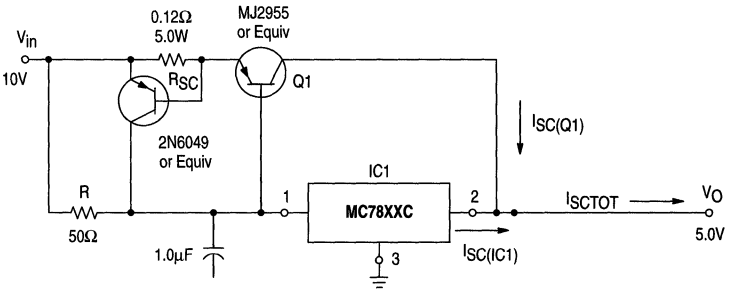
Figure 3–1C. Basic Circuit Configuration for Positive, Fixed Output, Three–Terminal Regulators



C_{in}: required if regulator is located more than a few (≈2 to 4) inches away from input supply capacitor; for long input leads to regulator, up to 1.0 µF may be needed for C_{in}. (C_{in} should be a high frequency type capacitor.)
C_O: improves transient response.
XX: two digits of type number indicating nominal output voltage.

See Section 15 for heatsinking.

Figure 3–2C. Current Boost Configuration for Positive Three–Terminal Regulators



XX: two digits of type number indicating nominal output voltage.
R: used to divert IC regulator bias current and determines at what output current level Q1 begins conducting.

$$0 < R \leq \frac{V_{BE\ on(Q1)}}{I_{Bias\ (IC1)}} \; ; \; R_{SC} \approx \frac{0.6\ V}{I_{SC(Q1)}} \; ; \; I_{SCTOT} = I_{SC(Q1)} + I_{SC(IC1)}$$

Selection of Q1 based on considerations of Section 4.

Values shown are for a 5.0 V, 5.0 A regulator using an MC7805CT on a 2.5°C/W heatsink and Q1 on a 1°C/W heatsink for T_A up to 70°C.

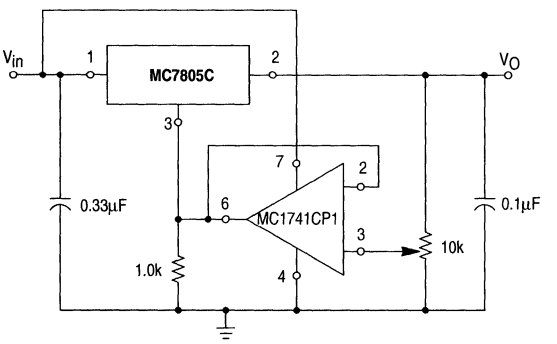
3. Obtaining an Adjustable Output Voltage

With the addition of an op amp, an adjustable output voltage supply can be obtained with the MC7805C. Regulation characteristics of the three–terminal regulators are retained in this configuration, shown in Figure 3–3C. If lower output currents are required, then an MC78M05C (0.5 A) could be used in place of the MC7805C.

4. Current Regulator

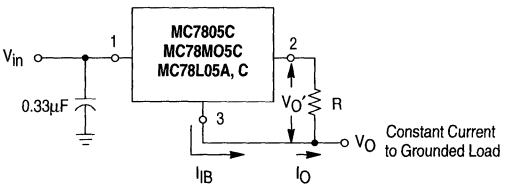
In addition to providing voltage regulation, the three–terminal positive regulators can also be used as current regulators to provide a constant current source. Figure 3–4C shows this configuration. The output current can be adjusted to any value from ≈ 8.0 mA (I_Q, the regulator bias current) up to the available output current of the regulator. Five–volt regulators should be used to obtain the greatest output voltage compliance range for a given input voltage.

Figure 3–3C. Adjustable Output Voltage Configuration Using a Three–Terminal Positive Regulator



V_O = 7.0 V to 33 V
$V_{in} - V_O \geq 2.0$ V
$V_{in} \geq 35$ V

Figure 3–4C. Current Regulator Configuration



$$I_O = \frac{V_O'}{R} + I_{IB}$$

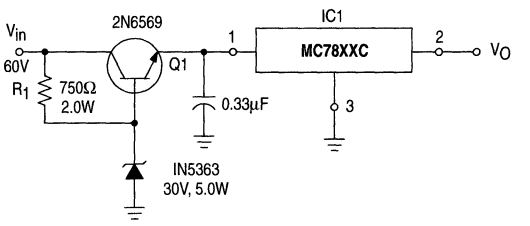
$$\text{Current Reg } \Delta I_O = \frac{\Delta V_O'}{R} + \Delta I_{IB}$$

$V_O + V_O' + 2.0\text{ V} \leq V_{in} \leq 35$ V

5. High Input Voltage

Occasionally, it may be necessary to power a three–terminal regulator from a supply voltage greater than $V_{in(max)}$, 35 V or 40 V. In these cases a preregulator circuit, as shown in Figure 3–5C, may be used.

Figure 3–5C. Preregulator for Input Voltages Above $V_{in(max)}$



$$R_1 = \left(\frac{V_{in} - 30}{1.5}\right) \bullet h_{fe(Q1)}$$

$V_{CEO(Q1)} \leq V_{in}$

XX: two digits of type number indicating nominal output voltage.

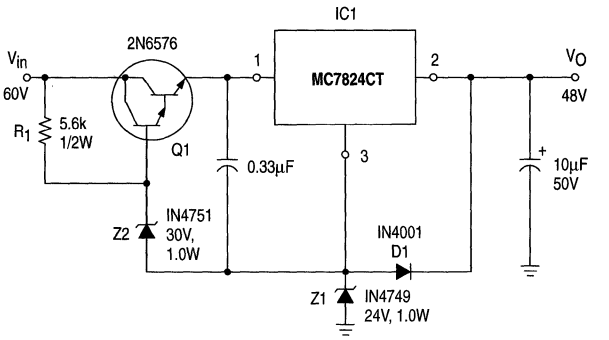
Values shown for V_{in} = 60 V

Q1 should be mounted on a 2°C/W heatsink for operation at T_A up to +70°C. IC1 should be appropriately heatsinked for the package type used.

6. High Output Voltage

If output voltages above 24 V are desired, the circuit configuration of Figure 3–6C may be used. Zener diode (Z1) sets the output voltage, while Q1, Z2, and D1 assure that the MC7824C does not have more than 30 V across it during short circuit conditions.

Figure 3–6C. High Output Voltage Configuration for Three–Terminal Positive Regulators



$$V_O = V_{Z1} + 24;\ R_1 = \left(\frac{V_{in} - (V_{Z1} + V_{Z2})}{1.5}\right) \bullet h_{fe(Q2)}$$

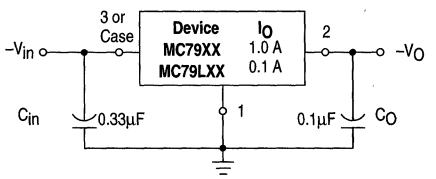
Values shown are for a 48 V, 1.0 A regulator
Q1 mounted on a 10°C/W heatsink
and IC1 mounted on a 2°C/W heatsink for T_A up to +70°C.

D. Negative, Fixed Output IC Regulator Configurations

1. Basic Regulator Configurations

Figure 3–1D gives the basic circuit configuration for the MC79XX and MC79LXX three–terminal negative regulators.

Figure 3–1D. Basic Circuit Configuration for Negative Three–Terminal Regulators



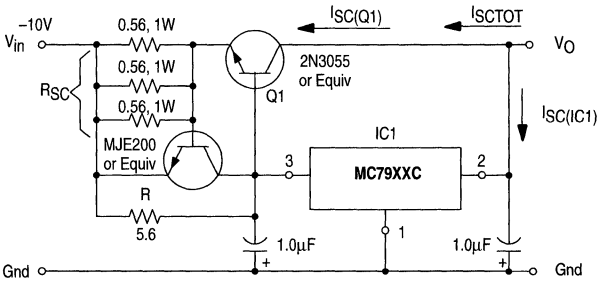
C_{in}: required if regulator is located more than a few (≈ 2 to 4) inches away from input supply capacitor; for long input leads to regulator, up to 1.0 µF may be required. C_{in} should be a high frequency type capacitor.
C_O: improves stability and transient response.
XX: two digits of type number indicating nominal output voltage.

See Section 15 for heatsinking.

Output Current Boosting

In order to obtain increased output current capability from the negative three–terminal regulators, the current boost configuration of Figure 3–2D may be used. Currents which can be obtained with this configuration are limited only by the capabilities of the external pass transistor(s).

Figure 3–2D. Output Current Boost Configuration for Three–Terminal Negative Regulators



XX: two digits of type number indicating output voltage. See Section 2 for available voltages.
R: used to divert regulator bias current and determine at what output current level Q1 begins conducting.

$$0 < R \leq \frac{V_{BE\ on(Q1)}}{I_{Bias(IC1)}}$$

$$I_{SCTOT} = I_{SC(Q1)} + I_{SC(IC1)}$$

$$R_{SC} \approx \frac{0.6\ V}{I_{SC(Q1)}}$$

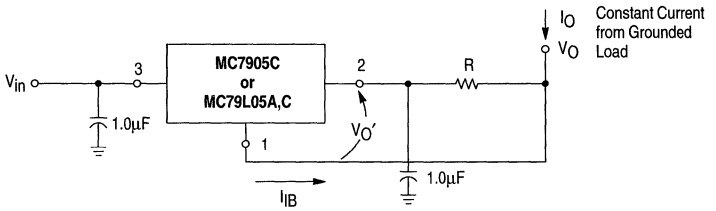
Selection of Q1 based on considerations of Section 4.

Values shown are for a −5.0 V, +4.0 A regulator; using an MC7905CT on a 1.5°C/W heatsink with Q1 mounted on a 1°C/W heatsink for T_A up to +70°C.

2. Current Regulator

The three–terminal negative regulators may also be used to provide a constant current sink, as shown in Figure 3–3D. In order to obtain the greatest output voltage compliance range at a given input voltage, the MC7905C or MC79L05C should be used in this configuration.

Figure 3–3D. Current Regulator Configuration for the Three–Terminal Negative Regulators



$V_{in} \geq -35$ V for MC7905C
$V_{in} \geq -30$ V for MC79L05C
$V_{in} \leq V_O + V_O - 2.0$ V

$$I_O = \frac{V_{O'}}{R} + I_{IB}$$

Current regulation: $\Delta I_O = \frac{\Delta V_{O'}}{R} + \Delta I_{IB}$

F. General Design Considerations

In addition to the design equations given in the regulator circuit configuration panels of Sections 3A–E, there are a few general design considerations which apply to all regulator circuits. These considerations are given below.

3

1. Regulator Voltages

For any circuit configuration, the worse–case voltages present on each pin of the IC regulator must be within the maximum and/or minimum limits specified on the device data sheets. These limits are instantaneous values, not averages.

They include: a. $V_{in(min)}$
b. $V_{in(max)}$
c. $(V_{in} - V_{out})$ min
d. $V_{out(min)}$
e. $V_{out(max)}$

For example, the voltage between Pins 12 and 7 (V_{in}) of an MC1723CP must never fall below 9.5 V, even instantaneously, or the regulator will not function properly, (see Figure 3–1B).

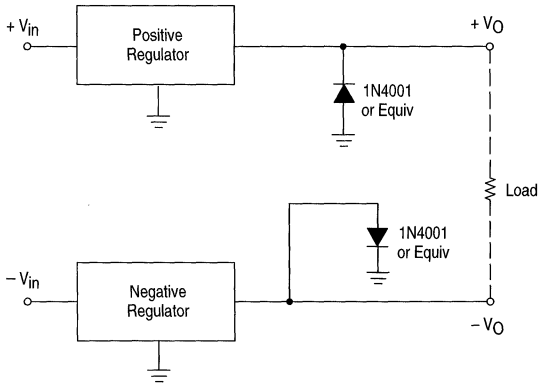
2. Regulator Power Dissipation, Junction Temperature and Safe Operating Area

The junction temperature, power dissipation output current or safe operating area limits of the IC regulator *must never be exceeded.*

3. Operation with a Load Common to a Voltage of Opposite Polarity

In many cases, a regulator powers a load which is not connected to ground but instead is connected to a voltage source of opposite polarity (e.g. op amps, level shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 3–1F. This protects the regulator, during startup and short circuit operation, from output polarity reversals.

Figure 3–1F. Output Polarity Reversal Protection



4. Reverse Bias Protection

Occasionally, there exists the possibility that the input voltage to the regulator can collapse faster than the output voltage. This could occur, for example, if the input supply is "crowbarred" during an output overvoltage condition. If the output voltage is greater ≈ 7.0 V, the emitter–base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed, as shown in Figure 3–2F.

Figure 3–3F shows a three–terminal positive–adjustable regulator with the recommended protection diodes for output voltages in excess of 25 V, or high output capacitance values (C_O > 25 μF, C_{Adj} >10 μF). Diode D1 prevents C_O from discharging through the regulator during an input short circuit. Diode D2 protects against capacitor C_{Adj} from discharging through the regulator during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the regulator during an input short circuit.

Figure 3–2F. Reverse Bias Protection

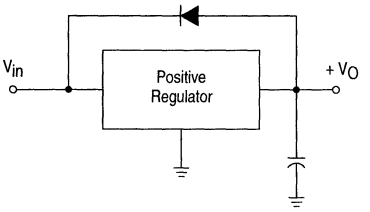
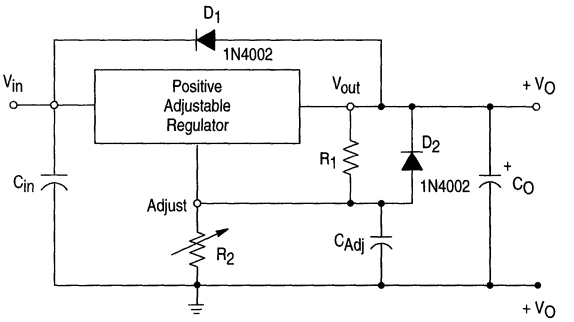


Figure 3–3F. Reverse Bias Protection for Three–Terminal Adjustable Regulators



3

SECTION 4
SERIES PASS ELEMENT CONSIDERATIONS FOR LINEAR REGULATORS

Presently, most monolithic IC voltage regulators that are available have output current capabilities from 100 mA to 3.0 A. If greater current capability is required, or if the IC regulator does not possess sufficient safe–operating–area (SOA), the addition of an external series pass element is necessary.

In this section, configurations, specifications and current limit techniques for external series pass elements will be considered. For illustrative purposes, pass elements for only positive regulator types will be discussed. However, the same considerations apply for pass elements used with negative regulators.

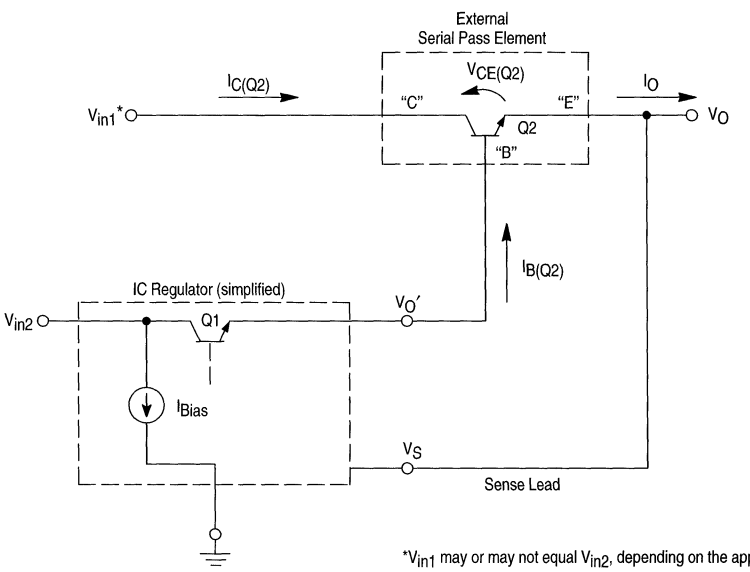
A. Series Pass Element Configurations

Using an NPN Type Transistor

If the IC regulator has an external sense lead, an NPN type series pass element may be used, as shown in Figure 4–1 A. This pass element could be a single transistor or multiple transistors arranged in Darlington and/or paralleled configurations.

In this configuration, the IC regulator supplies the base current (I_B) to the pass element (Q2) which acts as a current amplifier and provides the increased output current (I_O) capability.

Figure 4–1A. NPN Type Series Pass Element Configuration

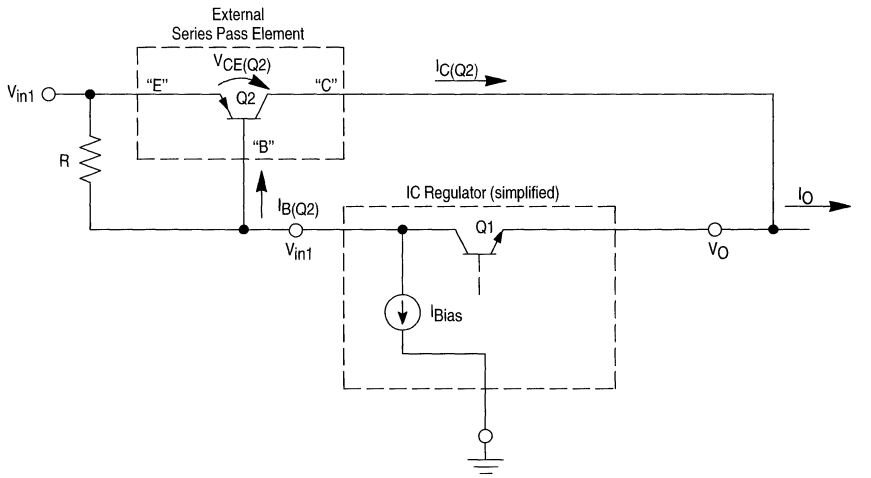


*V_{in1} may or may not equal V_{in2}, depending on the application.

Using a PNP Type Transistor

If the IC regulator does not have an external sense lead, as in the case of the three–terminal fixed output regulators, the configuration of Figure 4–1B can be used. (Regulators which possess an external sense lead may also be used with this configuration.) As before, the PNP type pass element can be a single transistor or multiple transistors.

Figure 4–1B. PNP Type Series Pass Element Configuration



This configuration functions in a similar manner to that of Figure 4–1A, in that the regulator supplies base current to pass element. The resistor (R) serves to route the IC regulator bias current (I_{Bias}) away from the base of Q2. If not included, regulation would be lost at low output currents. The value of R is low enough to prevent Q2 from turning on when I_{Bias} flows through this resistor, and is given by:

$$0 < R \leq \frac{V_{BEon(Q2)}}{I_{Bias}} \tag{4.0}$$

B. Series Pass Element Specifications

Independent of which configuration is utilized, the transistor or transistors that compose the pass element must have adequate ratings for $I_{C(max)}$, V_{CEO}, h_{fe}, power dissipation, and safe operating area.

1. $I_{C(max)}$ — for the pass element of Figure 4–1A, $I_{C(max)}$ is given by:

$$I_{C(max)(Q2)} \geq I_{O(max)} - I_{B(max)(Q2)} = I_{O(max)} - \frac{I_{C(max)(Q2)}}{h_{fe(Q2)}} \tag{4.1}$$

$$\geq I_{O(max)} \tag{4.2}$$

For the configuration of Figure 4–1B:

$$I_{C(max)(Q2)} \geq I_{O(max)} + I_{B(max)(Q2)} \tag{4.3}$$

$$\geq I_{O(max)} \tag{4.4}$$

2. V_{CEO} — since $V_{CE(Q2)}$ is equal to $V_{in1(max)}$ when the output is shorted or during start up:

$$V_{CEO(Q2)} \leq V_{in1(max)} \tag{4.5}$$

3. h_{fe} — the minimum DC current gain for Q2 in Figures 4–1A and 4–1B is given by:

$$h_{fe(min)(Q2)} \geq \frac{I_{C(max)(Q2)}}{I_{B(max)(Q2)}} \text{ @ } V_{CE} = (V_{in1(min)} - V_O) \tag{4.6}$$

3

4. Maximum Power Dissipation $P_{D(max)}$, and Safe Operating Area (SOA)

For any transistor there are certain combinations of I_C and V_{CE} at which it may safely be operated. When plotted on a graph, whose axes are V_{CE} and I_C, a safe–operating region is formed.

As an example, the safe–operating–area (SOA) curve for the well known 2N3055 NPN silicon power transistor is shown in Figure 4–2. The boundaries of the SOA curve are formed by $I_{C(max)}$, power dissipation, second breakdown and V_{CEO} ratings of the transistor. Notice that the power dissipation and second breakdown ratings are given for a case temperature of +25°C and must be derated at higher case temperatures. (Derating factors may be found in the transistors' data sheets.) These boundaries must never be exceeded during operation, or destruction of the transistor(s) which constitute the pass element may result. (In addition, the maximum operating junction temperature *must not be exceeded,* see Section 15.)

C. Current Limiting Techniques

In order to select a transistor or transistors with adequate SOA, the locus of pass element I_C and V_{CE} operating points must be known. This locus of points is determined by the input voltage (V_{in1}, output voltage (V_O), output current (I_O) and the type of output current limiting technique employed.

In most cases, V_{in1}, V_O, and the required output current are already known. All that is left to determine is how the chosen current limit scheme affects required pass element SOA.

Note, since the external pass element is merely an extension of the IC regulator, the following discussions apply equally well to IC regulators not using an external pass element.

1. Constant Current Limiting

This method is the simplest to implement and is extensively used, especially at the lower output current levels. The basic circuit configuration is shown in Figure 4–3A, and operates in the following manner.

As the output current increases, the voltage drop across R_{SC} increases, proportionately. When the output current has increased to the point that the voltage drop across R_{SC} is equal to the base–emitter ON voltage of Q3 ($V_{BEon(Q3)}$), Q3 conducts. This diverts base current (I_{Drive}) away from Q1, the IC regulator's internal series pass element. Base drive ($I_{B(Q2)}$) of Q2 is therefore reduced and its collector–emitter voltage increases, thereby reducing the output voltage below its regulated value, V_{out}. The resulting output voltage–current characteristic is shown in Figure 4–3B.

The value of I_{SC} is given by:

$$I_{SC} = \frac{V_{BEon(Q3)}}{R_{SC}} \tag{4.7}$$

Figure 4–2. 2N3055 Safe Operating Area (SOA)

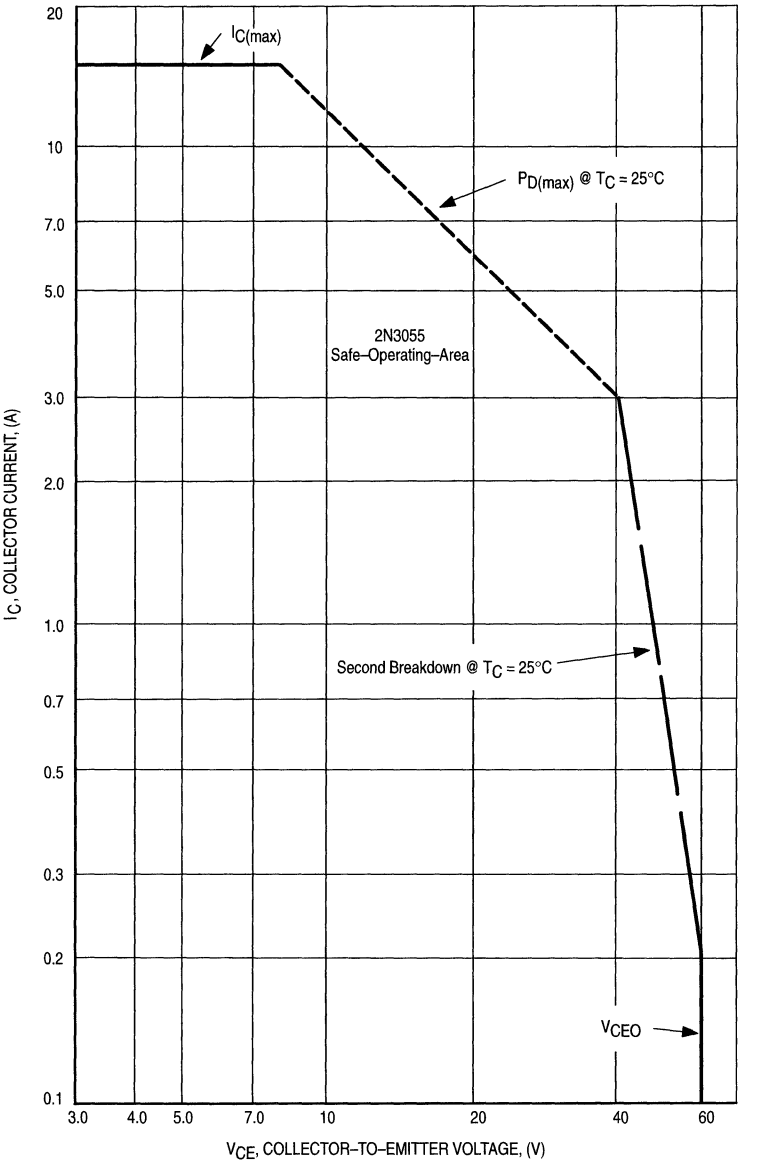
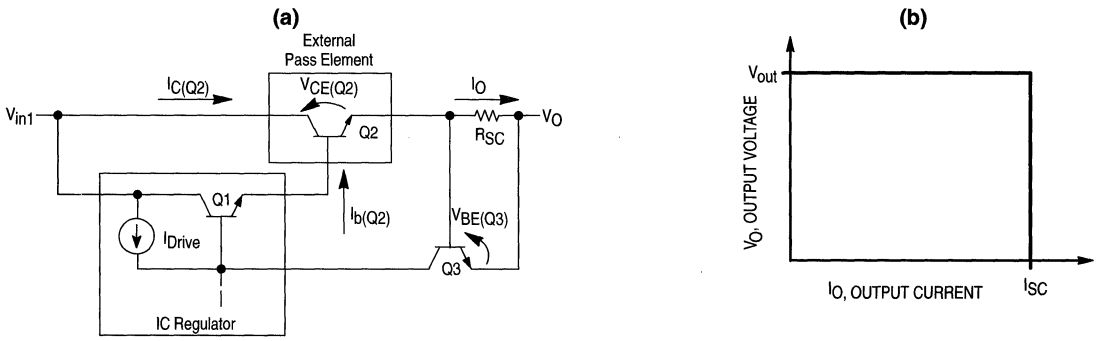


Figure 4–3. Constant Current Limiting



By using the base of Q1 in the IC regulator as a control point, this configuration has the added benefit of limiting the IC regulator output current ($I_{B(Q2)}$) to $I_{sc}/h_{fe(Q2)}$, as well as limiting the collector current of Q2 to I_{SC}. Of course, access to this point is necessary. Fortunately, it is usually available in the form of a separate pin or as the regulator's compensation terminal.(1)

The required safe–operating–area for Q2 can be obtained by plotting the V_{CE} and I_C of Q2 given by:

$$V_{CE(Q2)} = V_{in1} - V_O - I_O R_{SC} \simeq V_{in1} - V_O \quad (4.8)$$

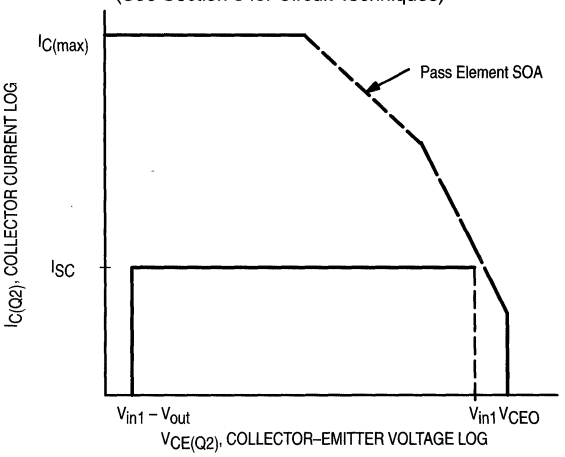
$$I_{C(Q2)} \simeq I_O \quad (4.9)$$

$$\text{where, } V_O = V_{out} \text{ for } 0 \leq I_O \leq I_{SC} \quad (4.10)$$

$$\text{and, } I_O = I_{SC} \text{ for } 0 \leq V_O \leq V_{out} \quad (4.11)$$

The resulting plot is shown in Figure 4–4. The transistor chosen for Q2 must have an SOA which encloses this plot, see Figure 4–4. Note that the greatest demand on the transistor's SOA capability occurs when the output of the regulator is short circuited and the pass element must support the full input voltage and short circuit current simultaneously.

Figure 4–4. Constant Current Limit SOA Requirements
(See Section 3 for Circuit Techniques)



(1) The three–terminal regulators have internal current limiting and therefore do not provide access to this point. If an external pass element is used with these regulators, constant current limiting can still be accomplished by diverting pass element drive.

2. Foldback Current Limiting

A disadvantage of the constant current limit technique is that in order to obtain sufficient SOA the pass element must have a much greater collector current capability than is actually needed. If the short circuit current could be reduced, while still allowing full output current to be obtained during normal regulator operation, more efficient utilization of the pass elements SOA capability would result. This can be done by using a "foldback" current limiting technique instead of constant current limiting.

The basic circuit configuration for this method is shown in Figure 4–5(A). The circuit operates in a manner similar to that of the constant current limiting circuit, in that output current control is obtained by diverting base drive away from Q1 with Q3.

At low output currents, V_A approximately equals V_O and V_{R2} is less than than V_O. Q3 is therefore non–conducting and the output voltage remains constant. As the output current increases, the voltage drop across R_{SC} increases until V_A and V_{R2} are great enough to bias Q3 on. The output current at which this occurs is I_K, the "knee" current.

Figure 4–5. Foldback Current Limiting

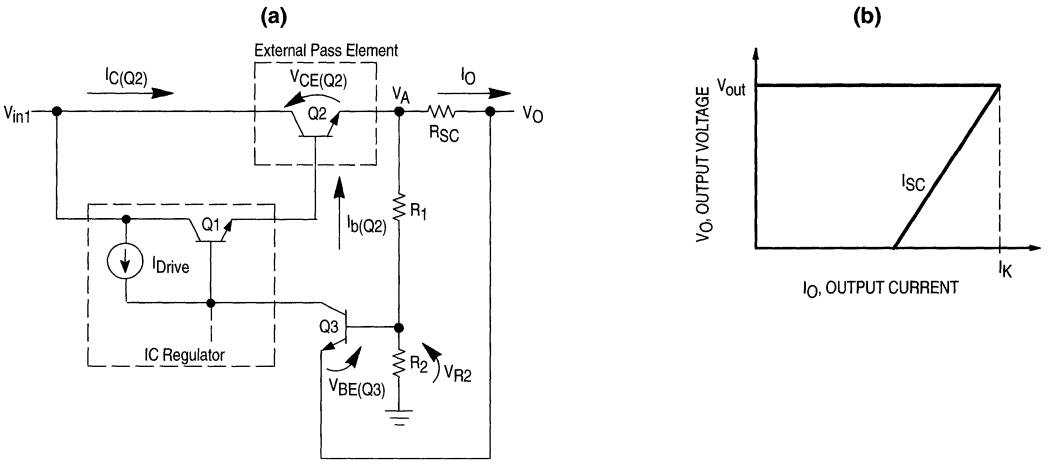
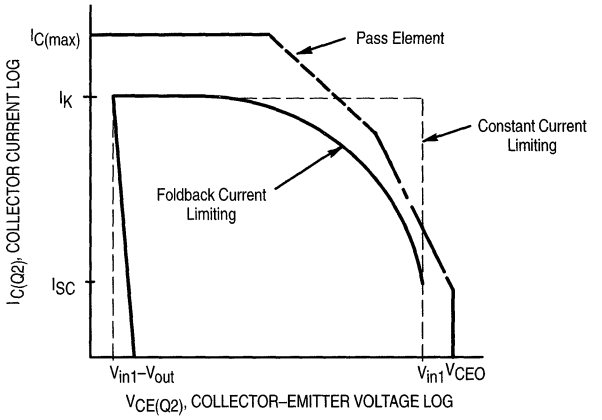


Figure 4–6. Foldback Current Limit SOA Requirements



The output voltage will now decrease. Less output current is now required to keep V_A and V_{R2} at a level sufficient to bias Q3 on since the voltage at its emitter has the tendency to decrease faster than that at its base. The output current will continue to "foldback" as the output voltage decreases, until an output short circuit current level (I_{SC}) is reached when the output voltage is zero. The resulting output current–voltage characteristic is shown in Figure 4–5B. The values for R_1, R_2, and R_{SC} (neglecting base current of Q3) are given by:

$$R_{SC} = \frac{V_{out}/I_{SC}}{\left(1 + \frac{V_{out}}{V_{BEon(Q3)}}\right) - \frac{I_K}{I_{SC}}} \tag{4.12}$$

$$\frac{R_2}{R_1 + R_2} = \frac{V_{BEon(Q3)}}{I_{SC}\, R_{SC}} \tag{4.13}$$

$$\text{and, } R_1 + R_2 \leq \frac{V_{out}}{I_{Drive}} \tag{4.14}$$

where: V_{out} = normal regulator output voltage
I_K = knee current
I_{SC} = short circuit current
I_{Drive} = base drive to regulator's internal pass element(s)

A plot of Q2 operating points, which result when using this technique, is shown in Figure 4–6. Note that the pass element is required to operate with a collector current of only I_{SC} during short circuit conditions, not the full output current, I_K. This results in a more efficient utilization of the SOA of Q2 allowing the use of a smaller transistor than if constant current limiting were used. Although foldback current limiting allows use of smaller pass element transistors for a given regulator output current than does constant current limiting, it does have a few disadvantages.

Referring to Equation (4.12), as the foldback ratio (I_K/I_{SC}) is increased, the required value of R_{SC} increases. This results in a greater input voltage at higher foldback ratios. In addition, it can be seen for Equation (4.12) that there exists an absolute limit to the foldback ratio equal to:

$$\left(\frac{I_K}{I_{SC(max)}}\right) = 1 + \frac{V_{out}}{V_{BEon(Q3)}} \text{ for } R_{SC} = \infty \tag{4.15}$$

For these reasons, foldback ratios greater than 2:1 or 3:1 are not usually practical for the lower output voltage regulators.

D. Paralleling Pass Element Transistors

Occasionally, it will not be possible to obtain a transistor with sufficient safe–operating–area. In these cases it is necessary to parallel two or more transistors. Even if a single transistor with sufficient capability is available, it is possible that paralleling two smaller transistors is more economical.

In order to insure that the collector currents of the paralleled transistors are approximately equal, the configuration of Figure 4–7 can be used. Emitter–ballasting resistors are used to force collector–current sharing between Q1 and Q2. The collector–current mismatch can be determined by considering the following, from Figure 4–7,

$$V_{BE1} + V_1 = V_{BE2} + V_2 \tag{4.16}$$

$$\text{and, } \Delta V_{BE} = \Delta V \tag{4.17}$$

where: $V_{BE} = V_{BE1} - V_{BE2}$ and, $\Delta V = V_2 - V_1$

Assuming $I_{E1} \simeq I_{C1}$ and $I_{E2} \simeq O_{C2}$, the collector–current mismatch is given by,

$$\frac{I_{C2} - I_{C1}}{I_{C2}} = \frac{\left(\frac{V_2}{R_E}\right) - \left(\frac{V_1}{R_E}\right)}{\left(\frac{V_2}{R_E}\right)} = \frac{V_2 - V_1}{V_2} = \frac{\Delta V}{V_2} = \frac{\Delta V_{BE}}{V_2} \tag{4.18}$$

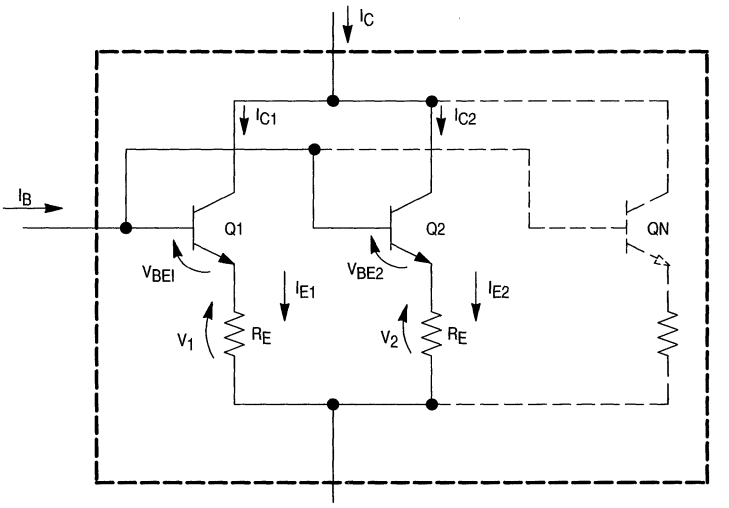
(4.19)

$$\text{and, percent collector–current mismatch} = \frac{\Delta V_{BE}}{V_2} \times 100\% \tag{4.20}$$

From Equation (4.20), the collector–current mismatch is dependent on ΔV_{BE} and V_2. Since ΔV_{BE} is usually acceptable, V_2 should be 1.0 V to 0.5 V, respectively. R_E is therefore given by:

$$R_E = \frac{0.5\text{ V to }1.0\text{ V}}{I_{C1}} = \frac{0.5\text{ V to }1.0\text{ V}}{I_{C2}} = \frac{0.5\text{ V to }1.0\text{ V}}{I_{C/2}} \tag{4.21}$$

Figure 4–7. Paralleling Pass Element Transistors



3

SECTION 5
LINEAR REGULATOR CONSTRUCTION AND LAYOUT

An important, and often neglected, aspect of the total regulator circuit design is the actual layout and component placement of the circuit. In order to obtain excellent transient response performance, high frequency transistors are used in modern integrated circuit voltage regulators. Proper attention to circuit layout is therefore necessary to prevent regulator instability or oscillations, or degraded performance.

In this section, guidelines will be given on proper regulator layout and placement of circuit components. In addition, topics such as remote voltage sensing, semiconductor mounting techniques, and thermal system evaluations will also be discussed.

1. General Layout and Component Placement Considerations

As mentioned previously, modern integrated circuit regulators are necessarily high bandwidth devices in order to obtain good transient response characteristics. To insure stable closed–loop operation, all these devices are frequency compensated, either internally or externally. This compensation can easily be upset by unwanted stray circuit capacitances and lead inductances, resulting in spurious oscillations. Therefore, it is important that the circuit lead lengths be short and the layout as tight as possible. Particular attention should be paid to locating the compensation and bypass capacitors as close to the IC as possible. Lead lengths associated with the external pass element(s), if used, should also be minimized.

Often overlooked is the stray inductance associated with the input leads to the regulator circuit. If the lead length from the input supply filter capacitor to the regulator input is more than a couple of inches, a 0.01 μF to 1.0 μF high frequency type capacitor (tantalum, ceramic, etc.) should be used to bypass the supply leads close to the regulator input pins.

2. Ground Loops and Remote Voltage Sensing

Ground Loops — Regulator performance can also suffer if ground loops in the circuit wiring are not avoided. The most common ground loop problem occurs when the return lead of the input supply filter capacitor is improperly located, as shown in Figure 5–1. If this return lead is physically connected between the load return and the regulator circuit ground point ("B"), a ripple voltage component (60 Hz or 120 Hz) can be induced on the load voltage (V_L). This is due to the high peaks of the filter capacitor ripple current (I_{ripple}) flowing through the lead resistance between the load and regulator. These peaks can be 5 to 15 times the value of load current. Since the regulator will only keep constant the voltage between its sense lead and ground point, points "A" and "B" in Figure 5–1, this additional ripple voltage (V_{lead}), will appear at the load.

This problem can be avoided by proper placement and connection of the filter capacitor return load as shown in Figure 5–2.

Remote Voltage Sensing — Closely related to the above ground loop problem is resistance in the current carrying leads to the load. This can cause poorer than expected load regulation in cases where the load currents are large or where the load is located some distance from the regulator. This is illustrated in Figure 5–3. As stated previously, the regulator circuit will keep the voltage present between its sense and ground pins constant. From Figure 5–3 we can see that any lead resistance between these points and the load will cause the load voltage (V_L) to vary with varying load current, I_L. This effectively lowers the load regulation of the circuit.

Figure 5–1. Filter Capacitor Ground Loop — WRONG!

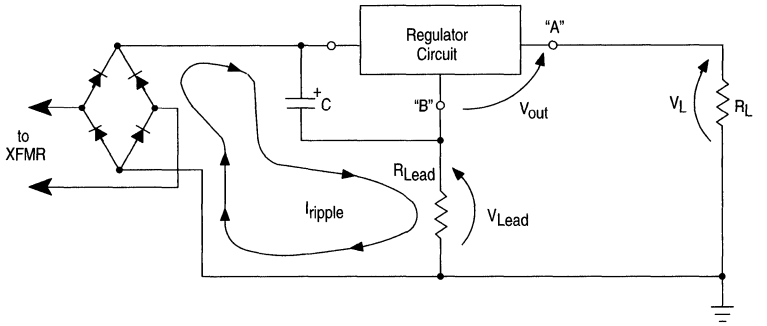
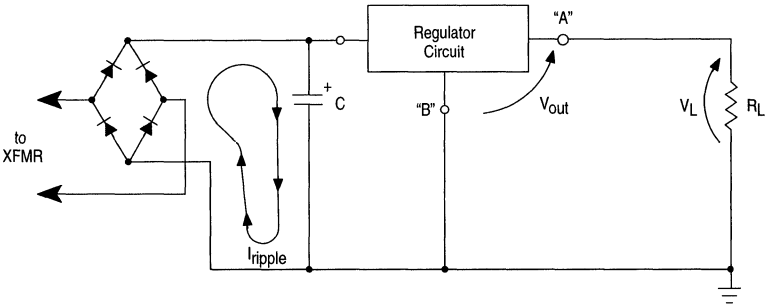


Figure 5–2. Filter Capacitor Ground Loop — RIGHT!



This problem can be avoided by the use of remote Sense leads, as shown in Figure 5–4. The voltage drops in the high current carrying leads now have no effect on the load voltage (V_L). However, since the Sense and Ground leads are usually rather long, care must be exercised that their associated lead inductance is minimized, or loop instability may result. The Ground and Sense leads should be formed into a twisted pair lead to minimize their lead inductance and noise pickup.

Figure 5–3. Effects of Resistance In Output Leads

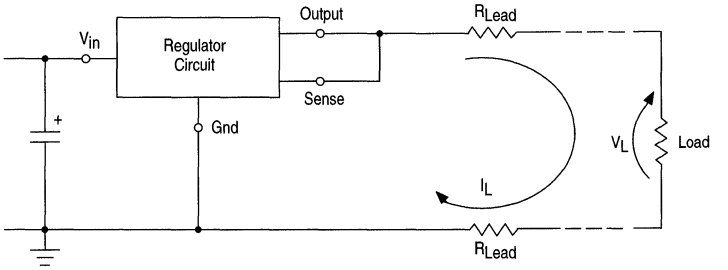
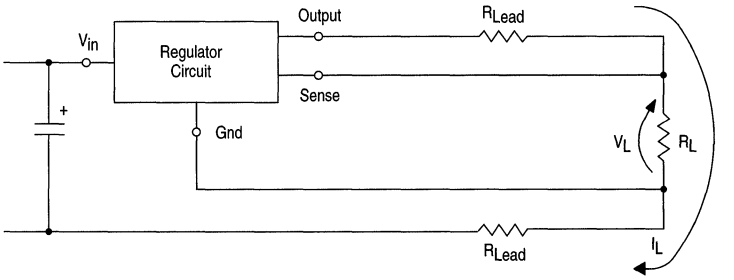


Figure 5–4. Remote Voltage Sensing



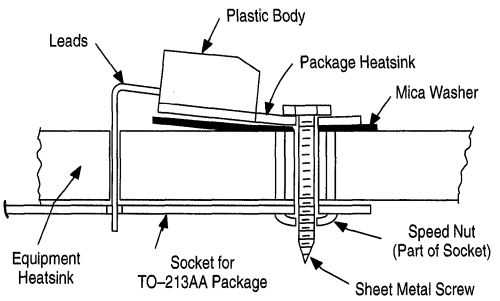
3. Mounting Considerations for Power Semiconductors

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead–mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one–half for a decrease in junction temperature from 160° to 135°C.(1) Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.(2) Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

Figure 5–5 shows an example of doing nearly everything wrong. A tab mount TO–220 package is shown being used as a replacement for a TO–213AA (TO–66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet metal screw through a 1/4″ hole containing a fiber–insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package, the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

Figure 5–5. Extreme Case of Improperly Mounting a Semiconductor (Distortion Exaggerated)



(1) MIL–HANDBOOK — 2178, SECTION 2.2.
(2) *Navy Power Supply Reliability — Design and Manufacturing Guidelines* NAVMAT P4855–1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.

In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc–over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Flange Mount Tab Mount
Plastic Body Mount Surface Mount

Appendix A contains a brief review of thermal resistance concepts.

Appendix B discusses measurement difficulties with interface thermal resistance tests.

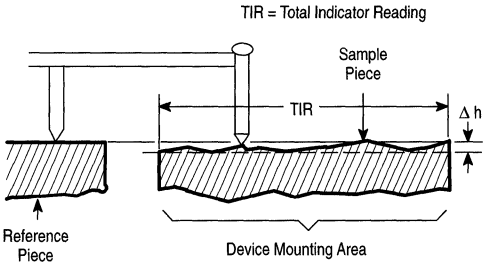
Mounting Surface Preparation

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 5–6. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness (i.e, $\Delta h/TIR$) if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

Figure 5–6. Surface Flatness Measurement



Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 μin. to 60 μin. is satisfactory. A finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO–204 (TO–3) package with a typical 32 μin. finish, showed that heatsink finishes between 16 μin. and 64 μin. caused less than ±2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.(3) Most commercially available cast or extruded heatsinks will require spotfacing when used in high power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO–204AA, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat–dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early–life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine–edge blanking or sheared–through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four–post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black–anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromate–acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of the paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 V.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

(3) Catalog #87–HS–9 (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381–0839.

Interface Decisions

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise, the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pockmarked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section. To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease–like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct, a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic–encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 5–1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Table 5–1. Approximate Values for Interface Thermal Resistance Data from Measurements Performed In Motorola Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
JEDEC Outlines	Description	Test Torque In–Lb	Metal–to–Metal		With Insulator			See Note
			Dry	Lubed	Dry	Lubed	Type	
TO–204AA (TO–3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO–220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figures 5–7 and 5–8 for additional data on TO–204AA and TO–220 packages.
2. Screw not insulated (see Figure 5–12).

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil, a dry graphite compound, is shown in the data of Figure 5–7. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from AAVID is called KON–DUX. It is made with a unique, grain oriented, flake–like structure (patent pending). Highly compressible, it becomes formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

Insulation Considerations

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non–isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the Motorola Full Pak and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal–to–metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

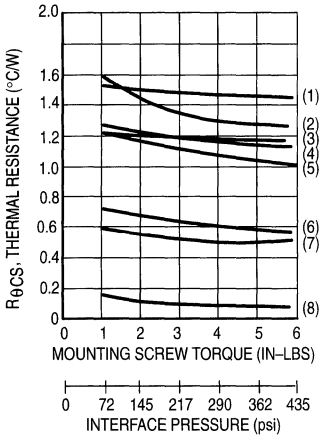
Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO–204 (TO–3) and TO–220 packages, is shown in Figure 5–7, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction–to–case).

Referring to Figure 5–7, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraided, as the dust is highly toxic.) Thermafilm is a filled polyimide material which is used for isolation (variation of Kapton). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high break down voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

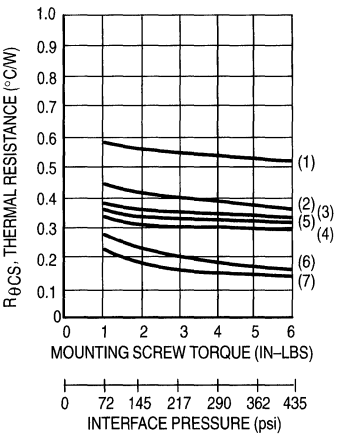
Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut–through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By comparing Figures 5–7(c) and 5–7(d), it can be noted that Thermasil, a filled silicone rubber without grease, has about the same interface thermal resistance as greased mica for the TO–220 package.

Figure 5–7. Interface Thermal Resistance Using Different Insulating Materials as a Function of Mounting Screw Torque

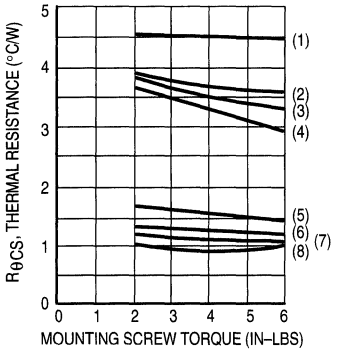


(a) TO–204AA (TO–3) Without Thermal Grease

(1) **Thermalfilm,** .002 (.05) thick
(2) **Mica,** .003 (.08) thick
(3) **Mica,** .002 (.05) thick
(4) **Hard anodized,** .020 (.51) thick
(5) **Aluminum oxide,** .062 (1.57) thick
(6) **Berylium oxide,** .062 (1.57) thick
(7) **Bare joint** — no finish
(8) **Grafoil,** .005 (.13) thick*
*Grafoil is not an insulating material

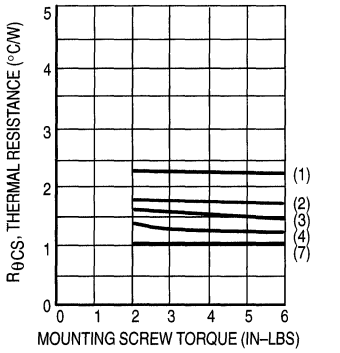


(b) TO–204AA (TO–3) With Thermal Grease



(c) TO–220 Without Thermal Grease

(1) **Thermalfilm,** .022 (.05) thick
(2) **Mica,** .003 (.08) thick
(3) **Mica,** .002 (.05) thick
(4) **Hard anodized,** .020 (.51) thick
(5) **Thermalsil II,** .009 (.23) thick
(6) **Thermalsil II,** .006 (.15) thick
(7) **Bare joint** — no finish
(8) **Grafoil,** .005 (.13) thick*
*Grafoil is not an insulating material



(d) TO–220 With Thermal Grease

Data Courtesy of Thermalloy

A number of manufacturers offer silicone rubber insulators. Table 5–2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out–of–flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K–10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called Rubber–Duc, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from AAVID shows $R\theta_{CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

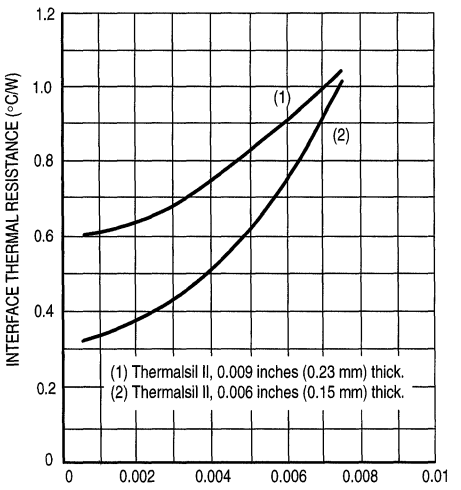
Table 5–2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakefield	Delta Pad 173–7	0.790	1.175
Bergquist	Sil Pad K–4	0.752	1.470
Stockwell Rubber	1867	0.742	1.015
Bergquist	Sil Pad 400–9	0.735	1.205
Thermalloy	Thermalsil II	0.680	1.045
Shin–Etsu	TC–30AG	0.664	1.260
Bergquist	Sil Pad 400–7	0.633	1.060
Chomerics	1674	0.592	1.190
Wakefield	Delta Pad 174–9	0.574	0.755
Bergquist	Sil Pad 1000	0.529	0.935
Ablestik	Thermal Wafers	0.500	0.990
Thermalloy	Thermalsil III	0.440	1.035
Chomerics	1671	0.367	0.655

*Test Fixture Deviation from flat Thermalloy EIR86–1010.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO–204AA (TO–3) package insulated with Thermasil is shown on Figure 5–8. Observe that the "worst case" encountered (7.5 mils) yields results having about twice the thermal resistance of the "typical case" (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.

Figure 5–8. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators



Data Courtesy of Thermalloy

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho–Therm 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R\theta_{CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in–lb from an initial 6 in–lb. With non–conformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 5–3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Table 5–3. Performance of Silicon Rubber Insulators Tested per MIL–I–49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data(1)	Bergquist Data(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho–Therm, 1617	0.233	—
Q Pad (non–insulated)	—	0.009
Sil–Pad, K–10	0.263	0.200
Thermasil III	0.267	—
Mica, greased	0.329	0.400
Sil–Pad 1000	0.400	0.300
Cho–therm 1674	0.433	—
Thermasil II	0.500	—
Sil–Pad 400	0.533	0.440
Sil–Pad K–4	0.583	0.440

(1) From Thermalloy EIR 87–1030
(2) From Bergquist Data Sheet

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly, so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi–pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost–effective insulated packages since the 1950s. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The second category contains parts which have a plastic overmold covering the metal mounting base. The Full Pak (Case 221C) illustrated in Figure 5–13, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non–insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

Fastener and Hardware Characteristics

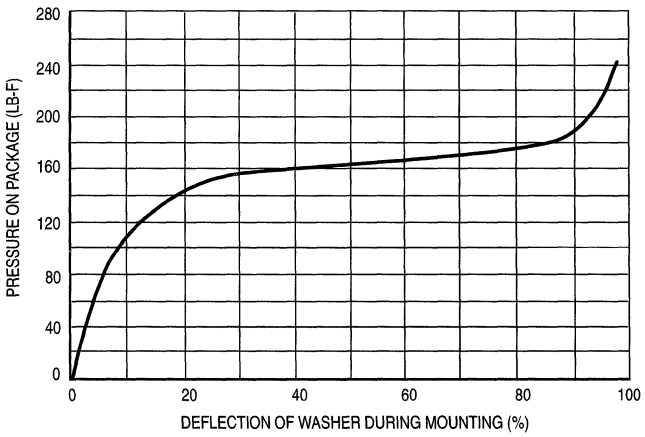
3

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 5–9, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut, the patented device can be soldered to a PC board and the semiconductor mounted with a 6–32 machine screw.(4)

Figure 5–9. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors



(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board–mounted or free–standing heat dissipators with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO–220 and TO–126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO–220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or Sync Nut) can form a trouble–free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self–Tapping Screws

Under carefully controlled conditions, sheet metal screws are acceptable. However, during the tapping process with a standard screw, a volcano–like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speed nut. If a self–tapping process is desired, the screw type must be used which roll–forms machine screw threads.

Rivets

Rivets are not recommended fasteners for any of the plastic packages. When a rugged metal flange–mount package is being mounted directly to a heatsink, rivets can be used provided press–riveting is used. Crimping force must be applied slowly and evenly. Pop–riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt–furnace, irons, vapor–phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.(5) Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non–field–serviceable systems or low strength types for field–serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

Fastening Techniques

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel or gold–plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

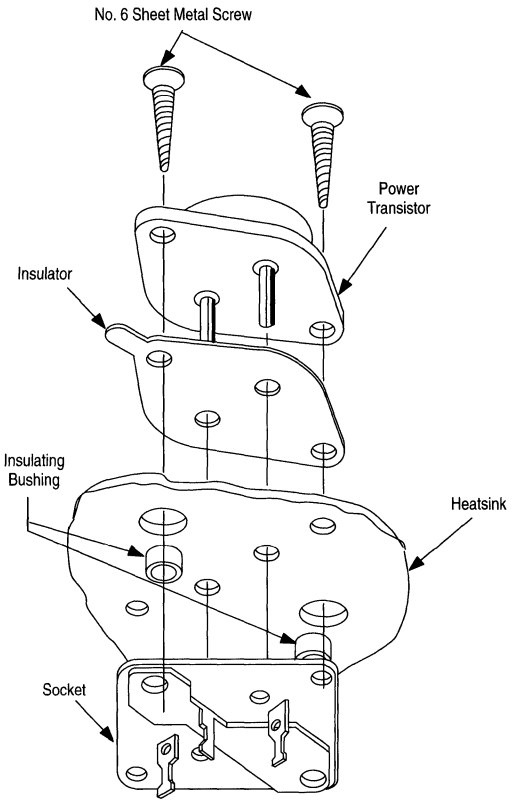
1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

Flange Mount

Few known mounting difficulties exist with the smaller flange mount packages, such as the TO–204 (TO–3). The rugged base and distance between die and mounting hose combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger–tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 5–10. Machine screws (preferred), self–tapping screws, islets or rivets may be used to secure the package using guidelines in the previous section, **Fastener and Hardware Characteristics**.

(5) Robert Batson, Elliot Fraunglass and James P. Moran, *Heat Dissipation Through Thermalloy Conductive Adhesives*, EMTAS '83 Conference, February 1–3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.

Figure 5–10. Hardware Used for a TO–204AA (TO–3) Flange Mount Part



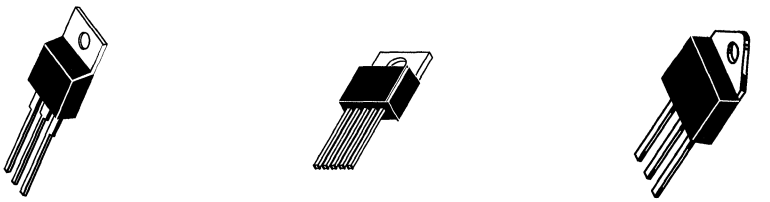
Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 5–11. Mounting considerations for all varieties are similar to that for the popular TO–220 package, whose suggested mounting arrangements and hardware are shown in Figure 5–12. The rectangular washer shown in Figure 5–12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch–pounds is suggested when using a 6–32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO–220 packages have a chamfer on one end. TO–220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO–220 package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.[6] In addition, it separates the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 5–14(c). To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

Figure 5–11. Several Types of Tab Mounted Parts



CASE 221A (TO–220AB) **CASE 314D** **CASE 340 (TO–218)**

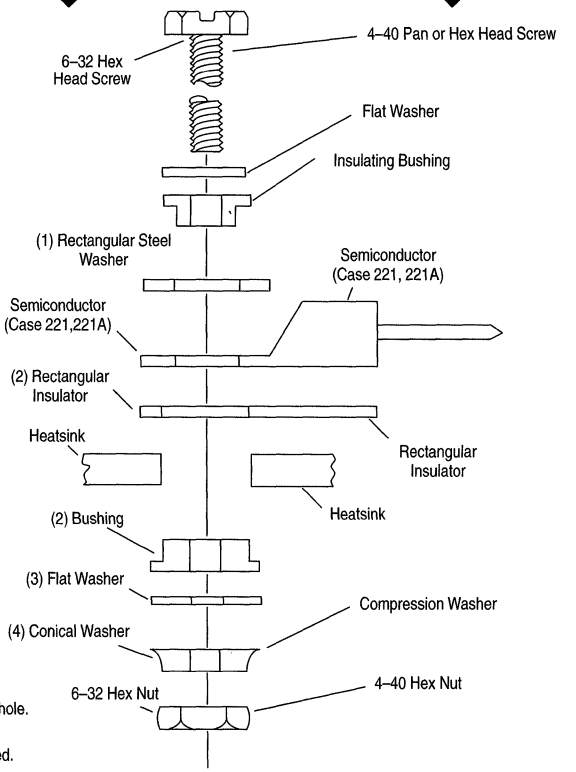
Figure 5–12. Mounting Arrangements for Tab Mount TO–220

a) Preferred Arrangement for Isolated or Non–isolated Mounting. Screw is at Semiconductor Case Potential. 6–32 Hardware is Used.

Choose from Parts Listed Below.

b) Alternate Arrangement for Isolated Mounting when Screw must be at Heatsink Potential. 4–40 Hardware is Used.

Use Parts Listed Below.



(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing is used.

(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.

Plastic Body Mount

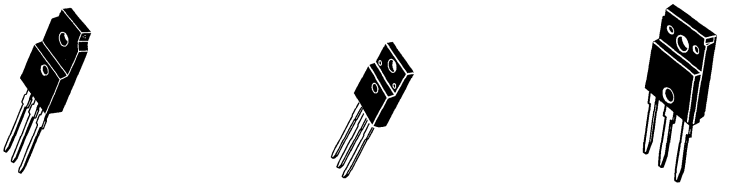
The Full Pak plastic power packages shown in Figure 5–13 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance.

The Full Pak (Case 221C) is similar to a TO–220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO–220 and is similar to that of the Thermopad.

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air–driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 5–9.

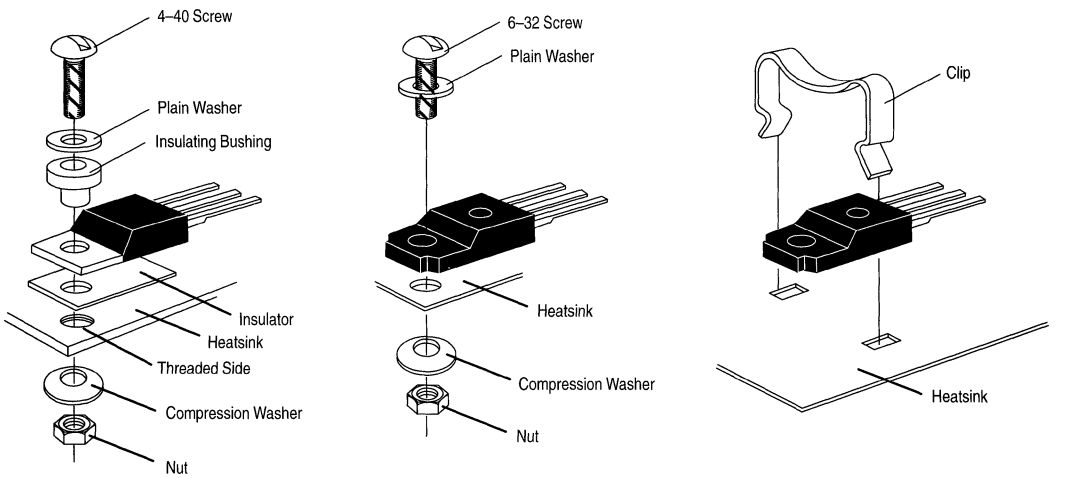
The Full Pak (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO–220. As shown in Figure 5–14(c), one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 5–14(b) may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO–220 package which is shown in Figure 5–14(a).

Figure 5–13. Plastic Body Mounted Packages



CASE 221C (Full Pak) | **CASE 221D (Full Pak)** | **CASE 340B (Full Pak)**

Figure 5–14. Mounting Arrangements for the Full Pak as Compared to a Conventional TO–220



(a) Screw Mounted TO–220 | **(b) Screw Mounted Full Pak** | **(c) Clip Mounted Full Pak**

Surface Mount

Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 5–15, for example, will accommodate a die up to 112 mils × 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

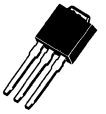
3

Standard glass–epoxy 2 oz. boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 5–16 shows, thermal resistance assymtotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlayed with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.(7) The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

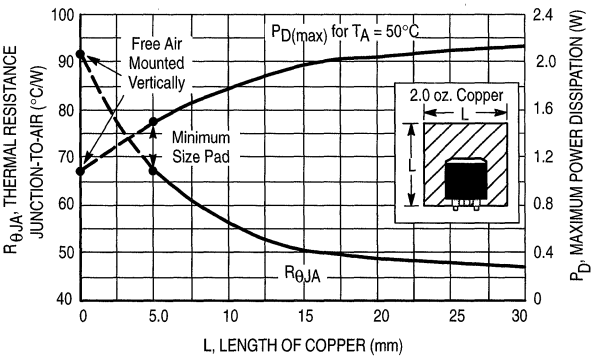
Figure 5–15. Surface Mounted DPAK Packages



CASE 369

CASE 369A

Figure 5–16. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass–Epoxy Board



(7) Herb Fick, *Thermal Management of Surface Mount Power Devices*, Powerconversion and Intelligent Motion, August 1987.

Free Air and Socket Mounting

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO–220 Package and other similar types is offered by heatsink accessory vendors.

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

Connecting and Handling Terminals

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead–bending unnecessary. Numerous lead and tab–forming options are available from Motorola on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead–bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/32 inch for TO–220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead–to–plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

Cleaning Circuit Boards

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free–standing without support.

3

Thermal System Evaluation

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN569.

Other applications, notably switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where, T_J = junction temperature (°C),
T_C = case temperature (°C),
$R_{\theta JC}$ = thermal resistance junction–to–case as specified on the data sheet (°C/W),
P_D = power dissipated in the device (W).

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

Appendix A
Thermal Resistance Concepts

The basic equation for heat transfer under steady–state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where, q = rate of heat transfer or power dissipation (P_D),
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

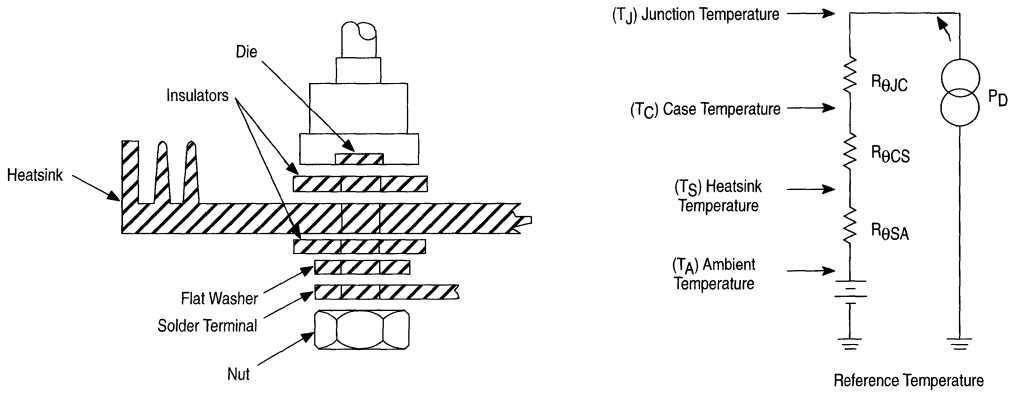
However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance (R_θ) is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation 2 and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A–1.

Figure A–1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor



The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_\theta JC + R_\theta CS + R_\theta SA) + T_A \quad (3)$$

where, T_J = junction temperature,
P_D = power dissipation,
$R_\theta JC$ = semiconductor thermal resistance (junction–to–case),
$R_\theta CS$ = interface thermal resistance (case–to–heatsink),
$R_\theta SA$ = heatsink thermal resistance (heatsink–to–ambient),
T_A = ambient temperature.

The thermal resistance junction–to–ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance ($R_\theta CS$) may be significant compared to the other thermal resistance terms. A proper mounting procedure can minimize $R_\theta CS$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short–pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

Appendix B
Measurement of Interface Thermal Resistance

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring dc power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

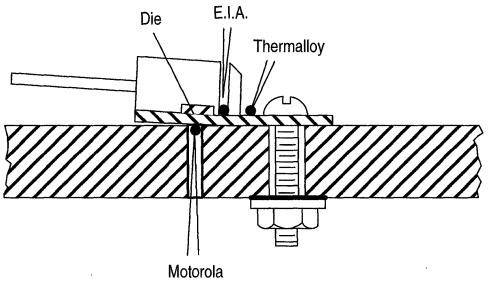
When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO–204AA package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL–I–49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented".

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The Motorola fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO–220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15% to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO–220 package shown in Figure B–1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, Motorola TO–220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure.

B–1. JEDEC TO–220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End



Three thermocouple locations are shown.

a) The Motorola location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b) The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c) The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in Figure B–1. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction–to–sink thermal resistance must be constant for a given test setup, the calculated junction–to–case thermal resistance values decrease and case–to–sink values increase as the case temperature thermocouple readings become warmer. Thus the choice of reference point for the case temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The Motorola location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO–220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction–to–case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1.0 mil/inch, has a finish better than 63 μin., and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application–oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction–to–case thermal resistance while testing for interface thermal resistance. If the junction–to–case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

SECTION 6
LINEAR REGULATOR DESIGN EXAMPLE

As an illustration of the use of the material contained in the preceding sections, the following regulator design example is given.

Regulator Performance Requirements:

Output Voltage, V_O = +10 V ± 0.1 V
Output Current, I_O = 1.0 A, current limited
Load Regulation, ≤ 0.1% for I_O = 10 mA to 750 mA
Line Regulation, ≤ 0.1%
Output ripple, ≤ 2.0 mVpp
Max Ambient Temperature, T_A ≤ +70°C
Supply will have common loads to a negative supply.

1. IC Regulator Selection

Study of the available regulators given in the selection guide reveals that the MC1723C would meet the regulation performance requirements. This regulator must be current boosted to obtain the required 1.0 A output current. A rough cost estimate shows that an MC1723C series pass element combination is the most economical approach.

2. Circuit Configuration

In Section 3, an appropriate circuit configuration is found. This is the MC1723C NPN boost configuration of Figure 3–4A.

3. Determination of Component Values

Using the equations given in Figure 3–4A, the values of C_{ref}, R_1, R_2, R_3 and R_{SC} are determined.

a) C_{ref} is chosen to be 0.1 μF for low noise operation.

b) $R_1 + R_2$ is chosen to be ≈ 10 k.

c) R_2 is then given by: $R_2 \approx \frac{7.0\ V}{V_O} (R_1 + R_2) = 0.7\ (10\ k) = 7.0\ k$

d) Since V_{ref} can vary by as much as ± 5% for the MC1723C, R_2 should be made variable by at least that much, so that V_O can be set to the required value of +10 V ± 0.1 V. R_2 is therefore chosen to consist of a 62 k resistor and a 2.0 k trimpot.

e) $R_1 = 10\ k - R_2 = 10\ k - 7.0\ k = 3.0\ k$

f) $R_{SC} \approx \frac{0.6\ V}{I_{SC}} = \frac{0.6\ V}{1.0\ A} = 0.6\ \Omega$; 0.56 Ω, 1.0 W chosen for R_{SC}.

g) $R_3 = R_1 \,||\, R_2 \cong 2.2\ k$

4. Determination of Input Voltage (V_{in})

There are two basic constraints on the input voltage: 1) the device limits for minimum and maximum V_{in} and, 2) the minimum input–output voltage differential. These limits are found on the device data sheet to be:

$$9.5\ V \le V_{in} \le 40\ V \text{ and } (V_{in} - V_O) \ge 3.0\ V$$

For the configuration of Figure 3–5A, $(V_{in} - V_O)$ is given by:

$$(V_{in} - V_O) = [V_{in} - (V_O + 2\phi)] \ge 3.0\ V, \text{ where } \phi = V_{BEon} \approx 0.6\ V$$

Note that $(V_{in} - V_O)$ is defined on the device data sheet to be the differential between the input and output pins. Since the base–emitter junction drops of Q1 and R_{SC} have been added to the circuit, they must be added to the minimum value of $(V_{in} - V_O)$. Therefore,

$$V_{in} \ge V_O + 2\phi + 3.0\ V = 10 + 1.2 + 3$$

$$V_{in} \ge 14.2\ V$$

This condition also satisfies the requirement for a minimum V_{in} of 9.5 V.

In order to simplify the design of the input supply (see Section 8), V_{in} is chosen to be 16 V average with a 3.0 Vpp ripple at full load and up to 25 V at no load. This assures that the input voltage is always above the required minimum value of 14.2 V. Now, the output ripple can be determined. The MC1723C has a typical ripple rejection ratio of –74 db, as given on its data sheet. With an input ripple of 3.0 Vpp, the output ripple would be less than 1.0 mVpp, which meets the regulator output ripple requirements.

5. Selection of the Series Pass Element (Q1)

The transistor type chosen for Q1 must have the following characteristics (see Section 4):

a) $V_{CEO} \ge V_{in(max)}$

b) $I_{C(max)} \ge I_{SC}$

c) $h_{fe} \ge \frac{I_{SC}}{I_O}$ @ $V_{CE} = V_{in} - V_O - \phi$, where $\phi = V_{BEon} \approx 0.6\ V$

d) $P_{D(max)} \ge V_{in,} \times I_{SC}$

e) θ_{JC} such to allow practical heatsinking

f) SOA such that it can withstand $V_{CE} = V_{in}$ @ $I_C = I_{SC}$

For this example: $V_{CEO} \ge 25\ V$

$I_{C(max)} \ge 1.0\ A$

$h_{fe} \ge 25$ @ $V_{CE} = 5.0\ V$ @ $I_C = 1.0\ A$

$P_{D(max)} \ge 16\ W$

$\theta_{JC} = 1.52°C/W$

SOA = 1.0 A @ 16 V

A 2N3055 transistor is chosen as a suitable device for Q1 using the selection guide of Section 4 and the transistor data sheets (available from the device manufacturer).

6. Q1 Heatsink Calculation

$$T_J = T_A + P_D\,\theta_{JA} \quad \text{(Equation 15.1 from Section 15)}$$

where, $P_D = V_{in} \times I_{SC}$

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ (Equation 6.2)

Solving for θ_{SA}:

$$\theta_{SA} = \left[\frac{T_J - T_A}{P_D}\right] - (\theta_{JC} + \theta_{CS}) \qquad (6.2)$$

From the 2N3055 data sheet, $T_J = 200°C$ and $\theta_{JC} = 1.52°C/W$. The transistor will be mounted with thermal grease directly to the heatsink. Therefore, θ_{CS} is found to be 0.1°C/W from Table 15–1.
Solving for Equation 6.2:

$$\theta_{SA} = \left[\frac{200°C - 70°C}{16\ V \times 1.0\ A}\right] - (1.52 + 0.1)\ °C/W$$

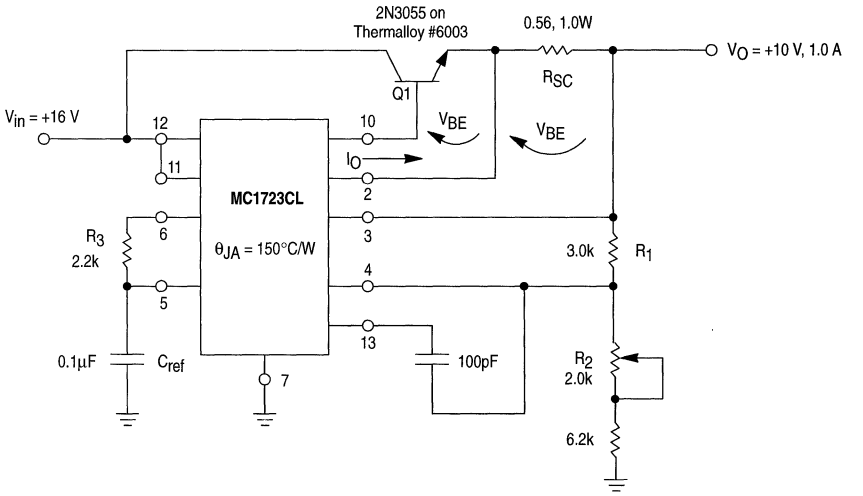
$$\leq 6.6°C/W$$

A commercial heatsink is now chosen from Table 15–2 or one custom designed using the methods given in Section 15. For this example, a Thermalloy #6003 heatsink, having a θ_{CS} of 6.2°C/W, was used.

7. Clamp Diode

Since the regulator can power a load which is also connected to a negative supply, a 1N4001 diode is connected to the output for protection. The complete circuit schematic is shown in Figure 6–1.

Figure 6–1. 10 V, 1.0 A Design Example



8. Construction Input Supply Design

The input supply is now designed using the information contained in Section 8 and the regulator circuit is constructed using the guidelines given in Section 5.

SECTION 7

LINEAR REGULATOR CIRCUIT TROUBLESHOOTING CHECKLIST

Occasionally, the designer's prototype regulator circuit will not operate properly. If problems do occur, the trouble can be traced to a design error in 99.9% of the cases. As a troubleshooting aid to the designer, the following guide is presented.

Of course, it would be difficult, if not impossible, to devise a troubleshooting guide which would cover all possible situations. However, the checklist provided will help the designer pinpoint the problem in the majority of cases. To use the guide, first locate the problem's symptom(s) and then carefully recheck the regulator design in the area indicated using the information contained in the referenced handbook section.

If, after carefully rechecking the circuit, the designer is not successful in resolving the problem, seek assistance from the factory by contacting the nearest Motorola Sales office.

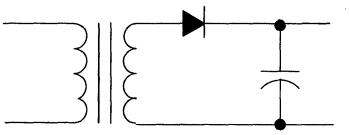
Symptoms	Design Area to Check	Section
Regulator oscillates	1. Layout 2. Compensation capacitor too small 3. Input leads not bypassed 4. External pass element parasitically oscillating	5 3 5 5
Loss of regulation at light loads	1. Emitter–base resistor in "PNP" type boost configuration too large 2. Absence of 1.0 mA "minimum" load. (See load regulation test spec on device data sheet) 3. Improper circuit configuration	4 3
Loss of regulation at heavy loads	1. Input voltage too low [$V_{in(min)}$, $\|V_{in} - V_O\|_{min}$] 2. External pass element gain too low 3. Current limit too low 4. Line resistance between sense points and load 5. Inadequate heatsinking	2, 3 4 3 5 15
IC regulator or pass element fails after warm–up or at high T_A.	1. Inadequate heatsinking 2. Input Voltage Transient $V_{in(max)}$, V_{CEO}	15 2, 4, 5
Pass element fails during short circuit.	1. Insufficient pass element ratings SOA, $I_{C(max)}$ 2. Inadequate heatsinking	4 15
IC regulator fails during short circuit.	1. IC current or SOA capability exceeded 2. Inadequate heatsinking	2
IC regulator fails during power–up	1. Input voltage transient $V_{in(max)}$ 2. IC current or SOA capability exceeded as load (capacitor) is charged up.	2 2
IC regulator fails during power–down.	1. Regulator reverse biased	3
Output voltage does not come up during power–up or after short circuit	1. Out polarity reversal 2. Load has "latched–up" in some manner. (Usually seen with op amps, current sources, etc.)	3
Excessive 60 Hz or 120 Hz output ripple	1. Input supply filter capacitor ground loop	5

3

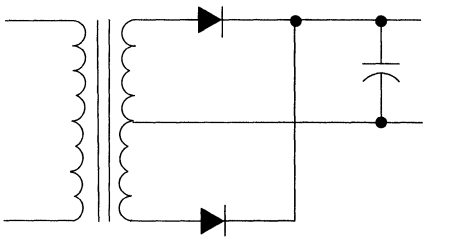
SECTION 8
DESIGNING THE INPUT SUPPLY

Most input supplies used to power series pass regulator circuits consist of a 60 Hz, single phase step–down transformer followed by a rectifier circuit whose output is smoothed by a choke or capacitor input filter. The type of rectifier circuit used can be either a half–wave, full–wave, or full–wave bridge type, as shown in Figure 8–1. The half–wave circuit is used in low current applications, while the full–wave is preferable in high–current, low output voltage cases. The full–wave bridge is usually used in all other high–current applications.

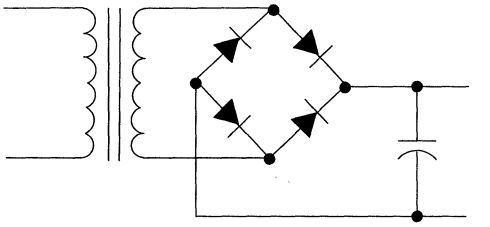
Figure 8–1. Rectification Schemes



(a) Half–Wave



(b) Full–Wave or Full–Wave Center Tap



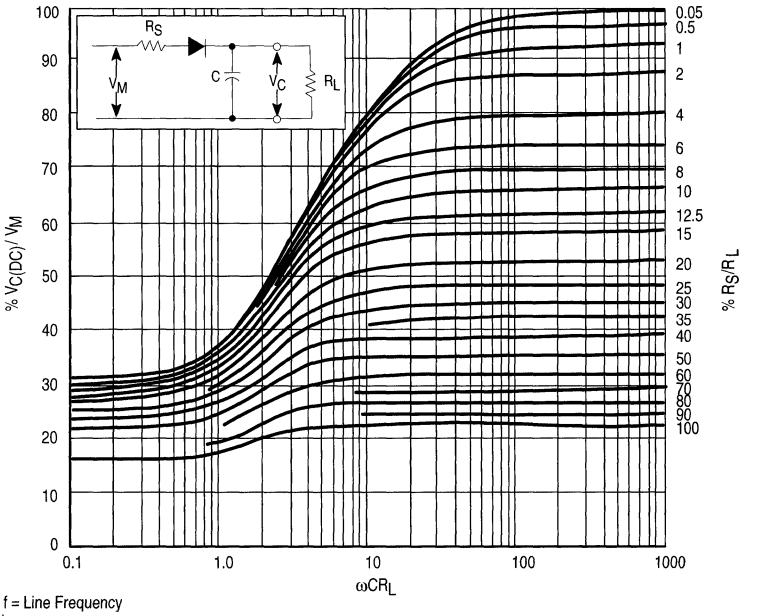
(c) Full–Wave Bridge

In this section, specification of the filter capacitor, rectifier and transformer ratings will be discussed. The specifications for the choke input filter will not be considered since the simpler capacitor input type is more commonly used in series regulated circuits. A detailed description of this type of filter can be found in the reference listed at the end of this section.

1. Design of Capacitor–Input Filters

The best practical procedure for the design of capacitor–input filters still remains based on the graphical data presented by Schade(1) in 1943. The curves shown in Figures 8–2 through 8–5 give all the required design information for half–wave and full–wave rectifier circuits. Whereas Schade originally also gave curves for the impedance of vacuum–tube rectifiers, the equivalent values for semiconductor diodes must be substituted. However, the rectifier forward drop often assumes more significance than the dynamic resistance in low–voltage supply applications, as the dynamic resistance can generally be neglected when compared with the sum of the transformer secondary–winding resistance plus the reflected primary–winding resistance. The forward drop may be of considerable importance, however, since it is about 1.0 V, which clearly cannot be ignored in supplies of 12 V or less.

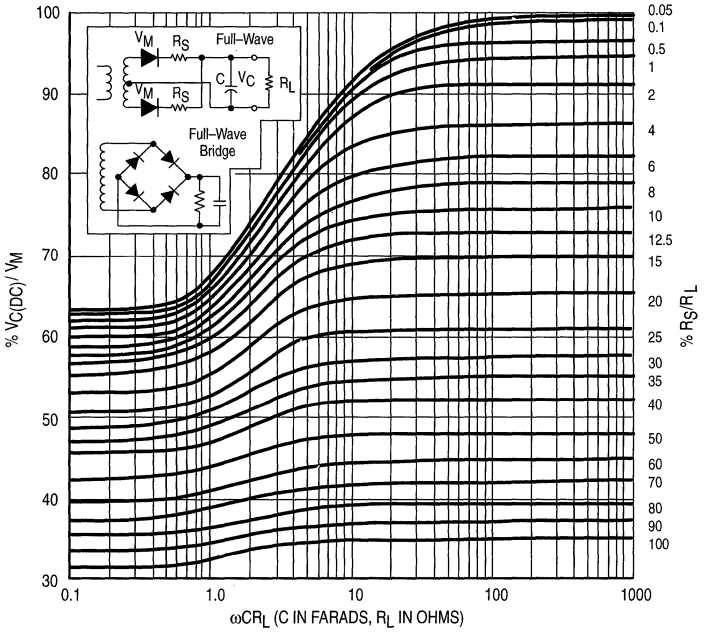
Figure 8–2. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Half–Wave Capacitor–Input Circuits



ω = 2 π f, f = Line Frequency
C in Farads
R_L in Ohms

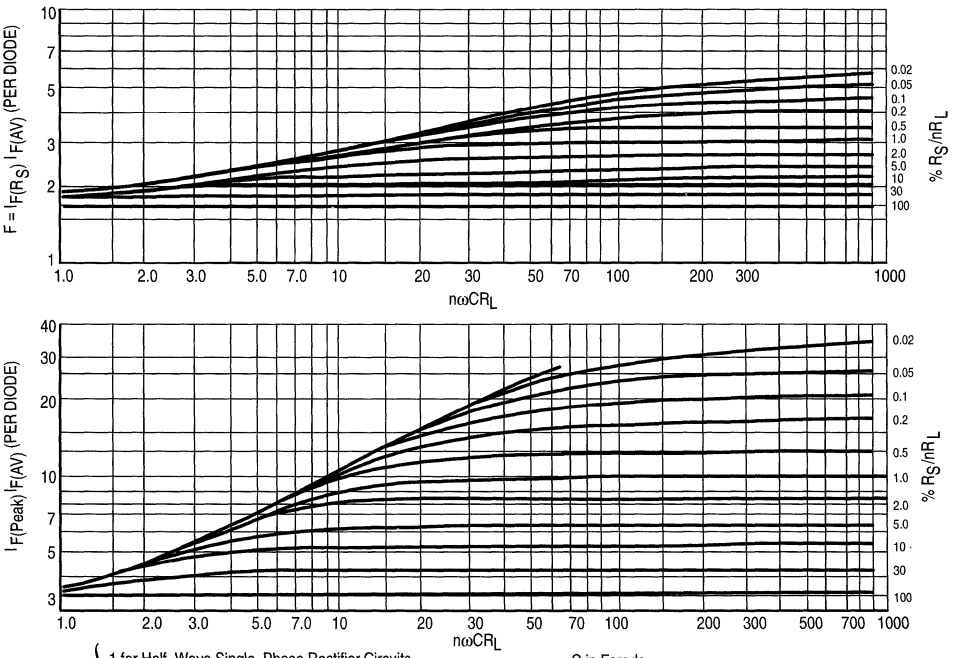
(1)From O. H. Schade, Proc. IRE, Vol. 31, p. 356, 1943.

Figure 8–3. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Full–Wave Capacitor–Input Circuits



$\omega = 2\pi f$, f = Line Frequency

Figure 8–4. Relation of RMS and Peak–to–Average Diode Current in Capacitor–Input Circuits

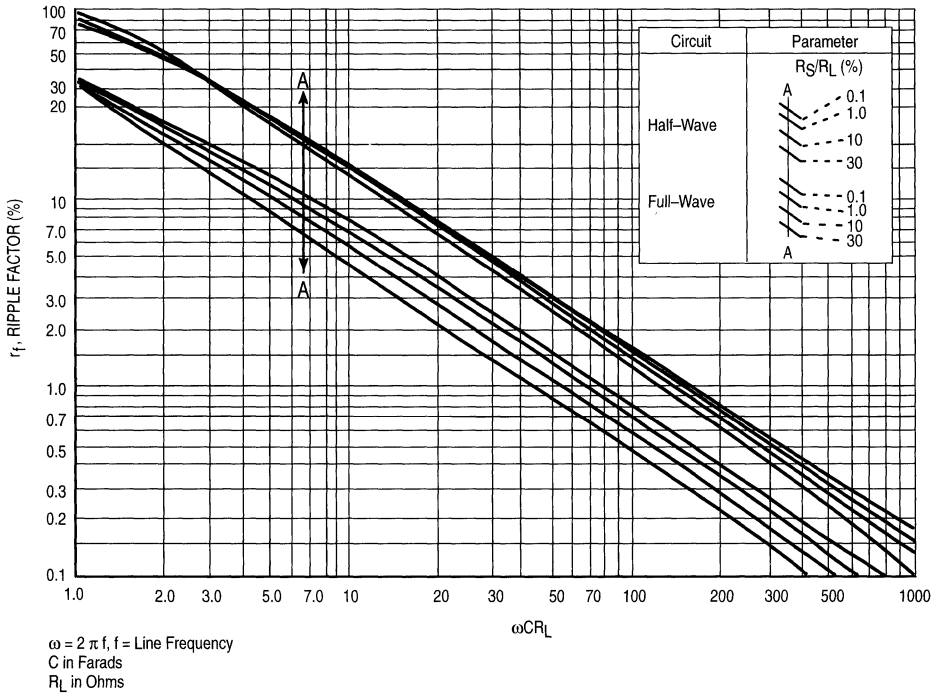


n = { 1 for Half–Wave Single–Phase Rectifier Circuits
2 for Full–Wave Single–Phase Rectifier Circuits

$\omega = 2\pi f$, where f = Line Frequency

C in Farads
R_L in Ohms
R_S = RMS Equivalent Source Resistance

Figure 8–5. Root–Mean–Square Ripple Voltage for Capacitor–Input Circuits



ω = 2 π f, f = Line Frequency
C in Farads
R_L in Ohms

Returning to the above curves, the full–wave circuit will be considered. Figure 8–3 shows that a circuit must operate with $\omega CR_L \geq 10$ in order to hold the voltage reduction to less than 10% and $\omega CR_L \geq 40$ to obtain less than 2.0% reduction. However, it will also be seen that these voltage reduction figures require R_S/R_L, where R_S is now the total series resistance, to be about 0.1% which, if attainable, causes repetitive peak–to–average current ratios from 10 to 17 respectively, as can be seen from Figure 8–4. These ratios can be satisfied by many diodes; however, they may not be able to tolerate the turn–on surge current generated when the input–filter capacitor is discharged and the transformer primary is energized at the peak of the input waveform. The rectifier is then required to pass a surge current determined by the peak secondary voltage less the rectifier forward drop and limited only by the series resistance R_S. In order to control this turn–on surge, additional resistance must often be provided in series with each rectifier. It becomes evident, then, that a compromise must be made between voltage reduction on the one hand and diode surge rating and hence average current–carrying capacity on the other hand. If small voltage reduction, that is good voltage regulation, is required, a much larger diode is necessary than that demanded by the average current rating.

Surge Current

The capacitor–input filter allows a large surge to develop, because the reactance of the transformer leakage inductance is rather small. The maximum instantaneous surge current is approximately V_M/R_S and the capacitor charges with a time constant $\tau \approx R_S C_1$. As a rough — but conservative — check, the surge will not damage the diode if V_M/R_S is less than the diode I_{FSM} rating and τ is less than 8.3 ms. It is wise to make R_S as large as possible and not pursue tight voltage regulation; therefore, not only will the surge be reduced but rectifier and transformer ratings will more nearly approach the DC power requirements of the supply.

2. Design Procedure

A) From the regulator circuit design (see Section 6), we know:

$V_{C(DC)}$ = the required full load average dc output voltage of the capacitor input filter
$V_{Ripple(pp)}$ = the maximum no load peak–to–peak ripple voltage
V_m = the maximum no load output voltage
I_O = the full–load filter output current
f = the input ac line frequency

3

B) From Figure 8–5, we can determine a range of minimum capacitor values to obtain sufficient ripple attenuation. First determine r_f:

$$r_f = \frac{V_{Ripple(pp)}}{2\sqrt{2}\,V_{C(DC)}} \times 100\% \tag{8.1}$$

A range for ωCR_L can now be found from Figure 8–5.

C) Next, determine the range of R_S/R_L from Figure 8–2 or 8–3 using $V_{C(DC)}$ and the values for ωCR_L found in part B. If the range of ωCR_L values initially determined from Figure 8–5 is above $\simeq 10$, R_S/R_L can be found from Figures 8–2 and 8–3 using the lowest ωCR_L value. Otherwise, several iterations between Figures 8–2 or 8–3 and 8–5 may be necessary before an exact solution for R_S/R_L and ωCR_L for a given r_f and $V_{C(DC)}/V_m$ can be found.

D) Once ωCR_L is found, the value of the filter capacitor (C) can be determined from:

$$C = \frac{\omega CR_L}{2\pi f\left(\frac{V_{C(DC)}}{I_O}\right)} \tag{8.2}$$

E) The rectifier requirements may now be determined:

1. Average current per diode;

$$I_{F(avg)} = I_O \text{ for half–wave rectification} = I_O/2 \text{ for full–wave rectification} \tag{8.3}$$

2. RMS and Peak repetitive rectifier current ratings can be determined from Figure 8–4.
3. The rectifier PIV rating is 2 V_m for the half–wave and full–wave circuits, V_m for the full wave bridge circuit. In addition, a minimum safety margin of 20% to 50% is advisable due to the possibility of line transients.
4. Maximum surge current, $I_{surge} = V_m/(R_S + ESR)$ (8.4)
   where, ESR = minimum equivalent series resistance of filter capacitor from its data sheet.

F) Transformer Specification

1. Secondary leg RMS voltage, $V_S = \{V_m + (n)\ 1.0\}/\sqrt{2}$ (8.5)
   where; n = 1 for half–wave and full–wave
   n = 2 for full–wave bridge
2. Total resistance of secondary and any external resistors to be equal to R_S found from Figures 8–2, 8–3, and 8–4 (see Part C).
3. Secondary RMS current; half–wave = I_{rms}; full–wave = I_{rms}; full–wave bridge = $\sqrt{2}\,I_{rms}$ (8.6)
   where, I_{rms} = rms rectifier current (from part E.1 and E.2).
4. Transformer VA rating; half–wave = $V_S\,I_{rms}$; full–wave = $2\,V_S\,I_{rms}$; full–wave bridge = $V_S\,I_{rms}(\sqrt{2})$ (8.7)
   where, I_{rms} = rms rectifier current (from part E.1 and E.2) and,
   V_S = secondary leg RMS voltage.

3. Design Example

A) Find the values for the filter capacitor, transformer rectifier ratings, given Full–Wave Bridge Rectification;

$$V_{C(DC)} = 16\ V$$
$$V_{Ripple(pp)} = 3.0\ V$$
$$V_M = 25\ V$$
$$I_O = 1.0\ A$$
$$f = 60\ Hz$$

B) Using Equation (8.1),

$$r_f = \frac{3}{2\sqrt{2}\,(16)} \times 100\% = 6.6\%$$

from Figure 8.5, $\omega CR_L \simeq 7$ to 15

C) Using $\omega CR_L = 10$, R_S/R_L is found from Figure 8–3 using,

$$\frac{V_{C(DC)}}{V_M} = \frac{16}{25} = 0.64 = 64\%$$

$$R_S/R_L = 20\% \text{ or } R_S = 0.2 \times R_L = 0.2\left(\frac{V_{C(DC)}}{I_O}\right) = 0.2\,(16)$$

$$R_S = 3.2\ \Omega$$

D) From Equation (8.2), the filter capacitor size is found:

$$C = \frac{\omega CR_L}{2\pi f\left(\frac{V_{C(DC)}}{I_O}\right)} = \frac{10}{2\pi f(60)16} = 1658\ \mu F$$

E) The rectifier ratings are now specified:
1. $I_{F(avg)} = I_O/2 = 0.5$ A from Equation (8.3)
2. $I_{F(rms)} = 2 \times I_{F(AVG)} = 1.0$ A from Figure 8–4
3. $I_{F(Peak)} = 5.2 \times I_{F(AVG)} = 2.6$ A from Figure 8–4
4. PIV = $V_M = 25$ V (use 50 V for safety margin)
5. $I_{surge} = V_M/(R_S + ESR) \simeq 25/3.2 = 7.8$ A from Equation (8.4), neglecting capacitor ESR.

F) The transformer should have the following ratings:
1. $V_S = \{V_M + n(1.0)\}/\sqrt{2} = (25 + 2)/\sqrt{2} = 19$ VRMS {from Equation (8.5)}
2. Secondary Resistance should be 3.2 Ω
3. Secondary RMS current rating should be 1.4 A, (from Equation (8.6)).
4. From Equation (8.7), the transformer should have a 27 VA rating.

It should be noted that, in order to simplify the procedure, the above design does not allow for line voltage variations or component tolerances. The designer should take these factors into account when designing his input supply. Typical tolerances would be: line voltage = +10% to –15% and filter capacitors = +75% to –10%.

REFERENCES
1. O. H. Schade, Proc. IRE, Vol. 31, 1943.
2. Motorola Silicon Rectifier Manual, 1980.

3

SECTION 9
AN INTRODUCTION TO SWITCHING POWER SUPPLIES

The Switching Power Supply continues to increase in popularity and is one of the fastest growing markets in the world of power conversion. Its performance and size advantages meet the needs of today's modern and compact electronic equipment and the increasing variety of components directed at these applications makes new designs even more practical.

This guide is intended to provide the designer with an overview of the more popular inverter circuits, their basic theory of operation, and some of the subtle characteristics involved in selecting a circuit and the appropriate components. Also included are valuable design tips on both the major passive and active components needed for a successful design. Finally, a complete set of selector guides to Motorola's Switchmode components is provided which gives a detailed listing of the industry's most comprehensive line of semiconductor products for switching power supplies.

Comparison with Linear Regulators

The primary advantages of a switching power supply are efficiency, size,and weight. It is also a more complex design, cannot meet some of the performance capabilities of linear supplies and generates a considerable amount of electrical noise. However switchers are being accepted in the industry, particularly where size and efficiency are of prime importance. Performance continues to improve and for most applications they are usually cost competitive down to the 20 W power level.

In the past the switcher's advantage versus the linear regulator was in the high power arena where passive components such as transformers and filters were small compared to the linear regulator at the same power level. However, active component count was high and tended to make the switcher less cost effective at low power levels. In recent years, Switchers have been significantly cost reduced because designers have been able to simplify the control circuits with new, cost effective integrated circuits and have found even lower cost alternatives in the passive component area.

A performance comparison chart of switching versus linear supplies is shown in Table 9–1. Switcher efficiencies run from 70% to 80% but occasionally fall to (60% to 65%) when linear post regulators are used for the auxiliary outputs. Some linear power supplies on the other hand, are operated with up to 50% efficiency but these are areas where line variations or hold–up time problems are minimal. Most linears operate with typical efficiencies of only 30%. The overall size reduction of a 20 kHz switcher is about 4:1 and newer designs in the 100 kHz to 200 kHz region end up at about 8:1 (versus a linear). Other characteristics such as static regulation specs are comparable, while ripple and load transient response are usually worse. Output noise specs can be somewhat misleading. Very often a 500 mV switching spike at the output may be attenuated considerably at the load itself due to the series inductance of the connecting cables and the additional filter capacitors found in many logic circuits. In the future, the noise generated at higher switching frequencies (100 kHz to 500 kHz) will probably be easier to filter and the transient response will be faster. Hold–up time is greater for switchers because it is easier to store energy in high voltage capacitors (200 V to 400 V) than in the lower voltage (20 V to 50 V) filter capacitors common to linear power supplies. This is due to the fact that the physical size of a capacitor is dependent on its CV product while energy storage is proportional to CV^2.

Table 9–1. 20 kHz Switcher versus Linear Performance

Parameter	Switcher	Linear
Efficiency	75%	30%
Size	2.0 W/in^3	0.5 W/in^3
Weight	40 W/lb	10 W/lb
Line and Load Regulation	0.1%	0.1%
Output Ripple V_{pp}	50 mV	5.0 mV
Noise V_{pp}	50 mV to 200 mV	—
Transient Response	1.0 ms	20 μs
Hold–Up Time	20 ms to 30 ms	1.0 ms to 2.0 ms

Basic Configurations

A switching power supply is a relatively complex circuit as is shown by the four basic building blocks of Figure 9–1. It is apparent here that the heart of the supply is really the high frequency inverter. It is here that the work of chopping the rectified line at a high frequency (20 kHz to 200 kHz) is done. It is here also that the line voltage is transformed down to the correct output level for use by logic or other electronic circuits. The remaining blocks support this basic function. The 60 Hz input line is rectified and filtered by one block and after the inverter steps this voltage down, the output is again rectified and filtered by another. The task of regulating the output voltage is left to the control circuit which closes the loop from the output to the inverter. Most control circuits generate a fixed frequency internally and utilize pulse width modulation techniques to implement the desired regulation. Basically, the on–time of the square wave drive to the inverter is controlled by the output voltage. As load is removed or input voltage increases,the slight rise in output voltage will signal the control circuit to deliver shorter pulses to the inverter and conversely as the load is increased or input voltage decreases, wider pulses will be fed to the inverter.

The inverter configurations used in today's switchers actually evolved from the buck and boost circuits shown in Figures 9–2a and 9–2b. In each case the regulating means and loop analysis will remain the same but a transformer is added in order to provide electrical isolation between the line and load. The forward converter family which includes the push–pull and half bridge circuits evolved from the buck regulator (Figure 9–2a). And the newest switcher, the flyback converter, actually evolved from the boost regulator. The buck circuit interrupts the line and provides a variable pulse width square wave to a simple averaging LC filter. In this case, the first order approximation of the output voltage is $V_{out} = V_{in} \times$ duty cycle and regulation is accomplished by simply varying the duty cycle. This is satisfactory for most analysis work and only the transformer turns ratio will have to be adjusted slightly to compensate for IR drops, diode drops, and transistor saturation voltages.

Operation of the boost circuit is more subtle in that it first stores energy in a choke and then delivers this energy plus the input line to the load. However, the flyback regulators which evolved from this configuration delivers only the energy stored in the choke to the load. This method of operation is actually based on the buck boost model shown in Figure 9–2c. Here, when the switch is opened, only the stored inductive energy is delivered to the load. The true boost circuit can also regulate by stepping up (or boosting) the input voltage whereas the buck–boost or flyback regulator can step the input voltage up or down. Analysis of the boost regulator begins by dealing with the choke as an energy storage element which delivers a fixed amount of power to the load: $P_O = 1/2\ L\ If_O$ where, I = the peak choke current; f_O = the operating frequency; and, L = the inductance.

Because it delivers a fixed amount of power to the load regardless of load impedance (except for short circuits), the boost regulator is the designer's first choice in photoflash and capacitive–discharge (CD) automotive ignition circuits to recharge the capacitive load. It also makes a good battery charger. For an electronic circuit load, however, the load resistance must be known in order to determine the output voltage:

$$V_O = \sqrt{P_O R_L} = I \sqrt{\frac{Lf_O R_L}{2}} \quad \text{where, } R_L = \text{the load resistance.}$$

In this case, the choke current is proportional to the on–time or duty cycle of the switch and regulation for fixed loads simply involves varying the duty cycle as before. However, the output also depends on the load which was not the case with buck regulators and results in a variation of loop gain with load.

Figure 9–1. Functional Block Diagram — Switching Power Supply

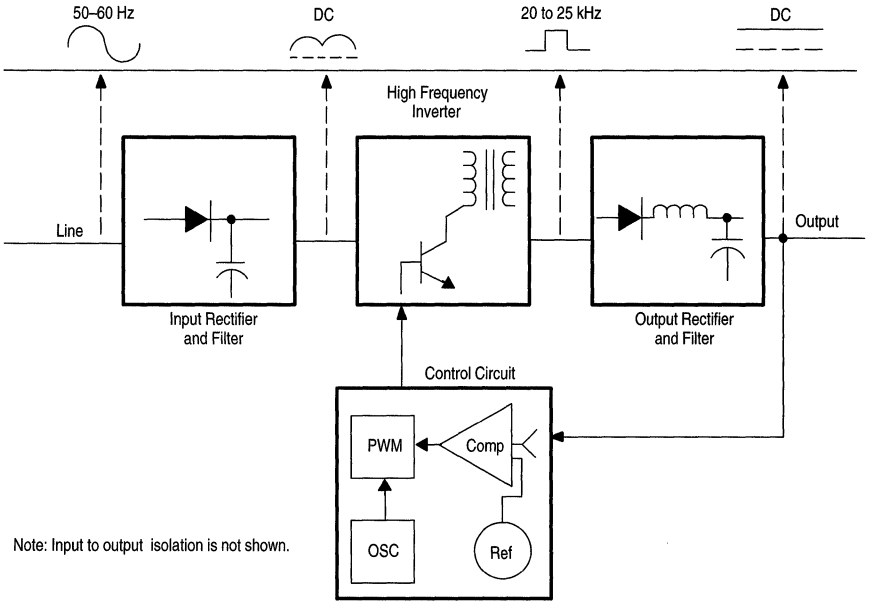
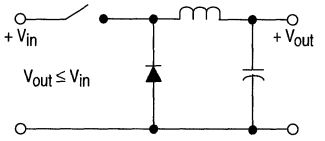
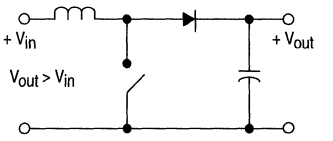


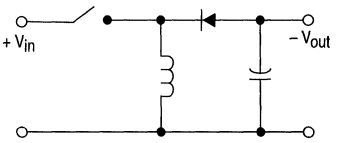
Figure 9–2. Nonisolated DC–DC Converters



(a) Buck (Step–Down)



(b) Boost (Step–Up)



(c) Buck–Boost Regulator which Resembles the Flyback Regulator (Step–Up or Down)

For both regulators, transient response or responses to step changes in load are very difficult to analyze. They lead to what is termed a "load dump" problem. This requires that energy already stored in the choke or filter be provided with a place to go when load is abruptly removed. Practical solutions to this problem include limiting the minimum load and using the right amount of filter capacitance to give the regulator time to respond to this change.

The Future

The future offers a lot of growth potential for switchers in general and low power switchers (20 W to 100 W) in particular. The latter are responding to the growth in microprocessor based equipment as well as computer peripherals. Today's configurations have already been challenged by the sine wave inverter which reduces noise and improves transistor reliability but does effect a cost penalty. Also, a trend to higher switching frequencies to reduce size and cost even further has begun. The latest bipolar designs operate efficiently up to 100 kHz and the FET seems destined to own the 200 kHz to 500 kHz range.

At this time there are a lot of safety and noise specifications. Originally governed only by MIL specs and the VDE in Europe, now both UL and the FCC have released a set of specifications that apply to electronic systems which often include switchers (see Table 9–2). It seems probable, however, that system engineers or power supply designers will be able to add the necessary line filters and EMI shields without evoking a significant cost penalty in the design.

The most optimistic note concerning switchers is in the component area. Switching power supply components have actually evolved from components used in similar applications. And it is very likely that newer and more mature products specifically for switchers will continue to appear over the next several years. The ultimate effect of this evolution will be to further simplify, cost reduce and increase the reliability of these designs.

Table 9–2. SMPS Specifications

Specification	Area
UL 478, VDE 0730, VDE 0806	Safety
VDE 0871, VDE 0875	EMI
MIL–STD–217D	Reliability
MIL–STD–461A	EMI
DOD–STD–1399	Harmonic Content
FCC Class A & B	EMI
CSA C22.2, IEC 380	Safety

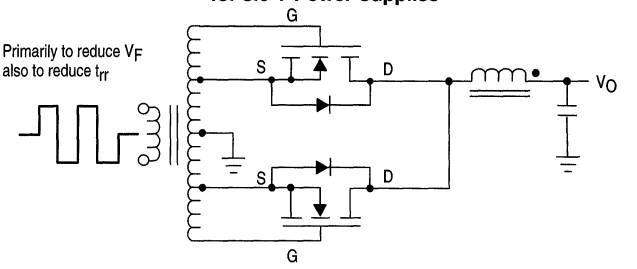
The synchronous rectifier is one example of a new component developed specifically for low voltage switchers. As requirements for 2.0 V and 3.0 V supplies emerge for use by fine geometry VLSI chips, the only way to maintain decent conversion efficiency is to develop lower forward drop rectifiers. The differences in 3.0 V and 5.0 V rectifier requirements are shown in Table 9–3. At this time, Motorola offers low V_F Schottky and area efficient TMOS III FETs for this task and is considering a variety of additional technology options. The direct approach involves using low V_F Schottkys or pinch rectifiers which will feature V_Fs of 0.3 V to 0.4 V. The indirect approach involves using FETs or bipolar transistors and slightly more complex circuitry like that shown in Figure 9–3. Both transistors will feature V_Fs of 0.2 V and, in addition, the bipolar will have high EBOs (30 V) and high gain (100) with a recovery time of 100 ns.

And for designers who are not satisfied with the relatively low frequency limitations of square wave switchers, there is the SRPS. The series resonant power supply topology seems to offer the possibility of working in the 1.0 MHz region. If components like the relatively exotic power transformer can be cost reduced, then it will be possible for this topology to become dominant in the market. The features generally associated with this type of power supply are listed in Table 9–4 and a typical half bridge circuit is shown in Figure 9–4. In a design now being studied in Motorola's advanced products laboratory, standard FETs, Schottkys and ultrafast rectifiers all appear to work very well at 1.0 MHz.

Table 9–3. Synchronous Rectifier Requirements

Output Voltage	Rectifier Characteristics	
	V_F	V_R
5.0 V	0.5 V–1.0 V	30 V–60 V
3.0 V	0.3 V–0.6 V	20 V–40 V

Figure 9–3. Synchronous Rectifiers for 3.0 V Power Supplies

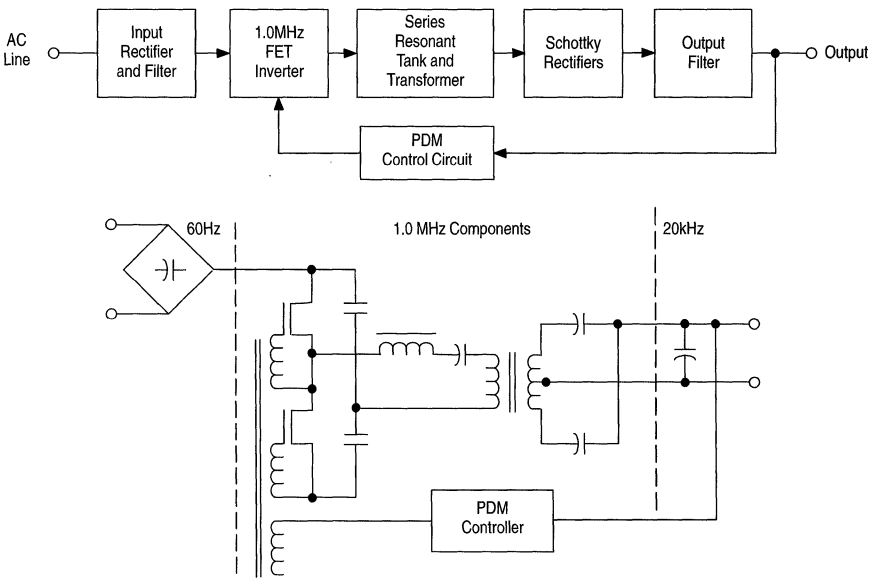


Note: The FET must be operated below V_F of the diode in order to gain the t_{rr} advantage.

Table 9–4. SRPS Features

Feature	Description
High Frequency	Today's line operated designs use sine waves in the 500 kHz to 1.0 MHz range.
Small Size	The ferrite transformer and polypropylene coupling capacitor are smaller than those found in lower frequency square wave designs.
Low Noise	Switching occurs at zero crossings which reduces component stress and lowers EMI.
Efficient	Because switching losses are reduced, efficiency is high (typically 80%).
High Peak to Average Current Ratios	Current ratings of the transistors and rectifiers are twice as high as similar flyback designs.
Special Control Circuit	PDM (density) rather than PWM (width) control is used and requires a control IC with a programmable VCO.
Market	The SRPS is expected to own 15% of the power supply market by 1990.

Figure 9–4. SRPS Block Diagram



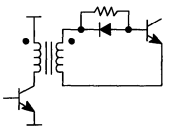
SECTION 10
SWITCHING REGULATOR TOPOLOGIES

FET and Bipolar Drive Considerations

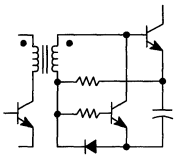
There are probably as many base drive circuits for bipolars as there are designers. Ideally, the transistor would like just enough forward drive (current) to stay in or near saturation and reverse drive that varies with the amount of stored base charge such as a low impedance reverse voltage. Many of today's common drive circuits are shown in Figure 10–1. The fixed drive circuits of Figure 10(a), (b) and (c) tend to emphasize economy, while the Baker clamp and proportional drive circuits of Figure 10(d) and (e) emphasize performance over cost.

FET drive circuits are another alternative. The standard that has evolved at this time is shown in Figure 10–2A. This transformer coupled circuit will produce forward and reverse voltages applied to the FET gate which vary with the duty cycle as shown. For this example, a V_{GS} rating of 20 V would be adequate for the worst case condition of high logic supply (12 V) and minimum duty cycle. And yet, minimum gate drive levels of 10 V are still available with duty cycles up to 50%. If wide variations in duty cycle are anticipated, it might be wise to consider using a semi–regulated logic supply for these situations. Finally, one point that is not obvious when looking at the circuit is that FETs can be directly coupled to many ICs with only 100 mA of sink and source capability and still switch efficiently at 20 kHz. However, to achieve switching efficiently at higher frequencies, 1.0 A to 2.0 A of drive may be required on a pulsed basis in order to quickly charge and discharge the gate capacitances. A simple example will serve to illustrate this point and also show that the Miller effect, produced by C_{DG}, is the predominant speed limitation when switching high voltages (see Figure 10–2B). A FET responds instantaneously to changes in gate voltage and will begin to conduct when the threshold is reached (V_{GS} = 2.0 V to 3.0 V) and be fully on with V_{GS} = 7.0 V to 8.0 V. Gate waveforms will show a porch at a point just above the threshold voltage which varies in duration depending on the amount of drive current available and this determines both the rise and fall times for the drain current.

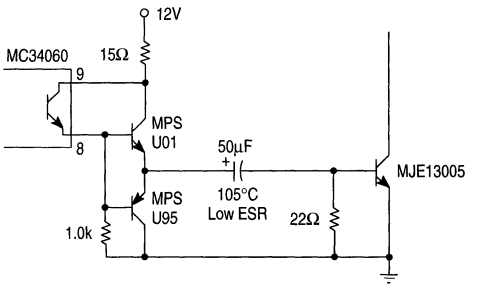
Figure 10–1. Typical Bipolar Base Drive Circuits



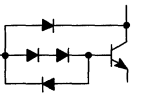
(a) Fixed Drive, Turn–Off Energy Stored in Transformer



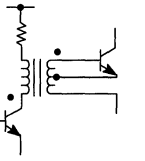
(b) Fixed Drive, Turn–Off Energy Stored in Capacitor



(c) Direct Drive



(d) Standard Baker Clamp



(e) Proportional Base Drive

Figure 10–2A. Typical Transformer Coupled FET Drive

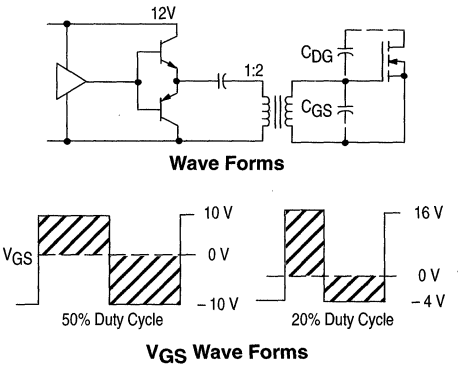
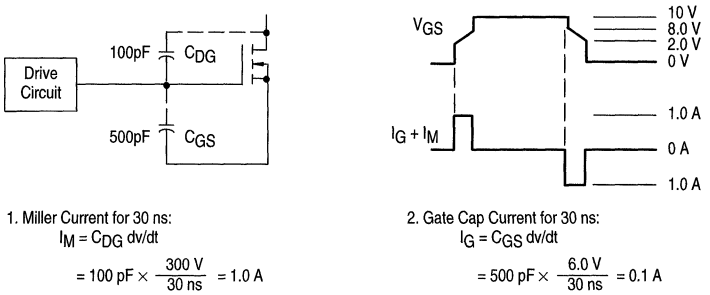


Figure 10–2B. FET Drive Current Requirements



1. Miller Current for 30 ns:
$I_M = C_{DG}\, dv/dt$
$= 100\ pF \times \frac{300\ V}{30\ ns} = 1.0\ A$

2. Gate Cap Current for 30 ns:
$I_G = C_{GS}\, dv/dt$
$= 500\ pF \times \frac{6.0\ V}{30\ ns} = 0.1\ A$

To estimate drive current requirements, two simple calculations with gate capacitances can be made:

1. $I_M = C_{DG}dv/dt$ and,
2. $I_G = C_{GS}dv/dt$

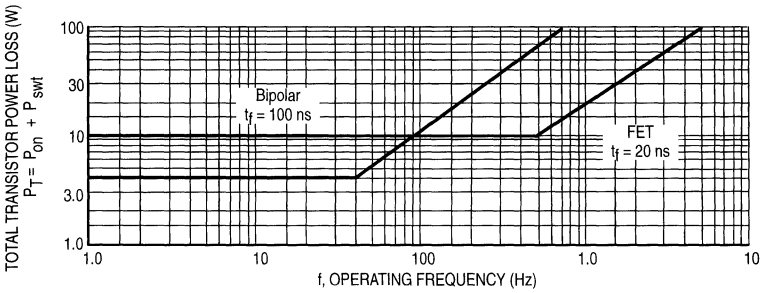
I_M is the current required by the Miller Effect to charge the drain–to–gate capacitance at the rate it is desired to move the drain voltage (and current). And I_G is usually the lesser amount of current required to charge the gate–to–source capacitance through the linear region (2.0 V to 8.0 V). As an example, if 30 ns switching times are desired at 300 V, where C_{DG} = 100 pF and C_{GS} = 500 pF, then:

1. I_M = 100 pF × 300 V/30 ns = 1.0 A and,
2. I_G = 500 pF × 6.0 V/30 ns = 0.1 A

This example shows the direct proportion of drive current capability to speed and also illustrates that for most devices, C_{DG} will have the greatest effect on switching speed and that C_{GS} is important only in estimating turn–on and turn–off delays.

Aside from its unique drive requirements, a FET is very similar to a bipolar transistor. Today's 400 V FETs compete with bipolar transistors in many switching applications. They are faster and easier to drive, but do cost more and have higher saturation, or more accurately, "on" voltages. The performance or efficiency tradeoffs are analyzed using Figure 10–3, where typical power losses for switching transistors versus frequency are shown. The FET (and bipolar) losses were calculated at 100°C rather than 25°C because on resistance and switching times are highest here and 100°C is typical of many applications. These curves are asymptotes of the actual device performance, but are useful in establishing the "breakpoint" of various devices, which is the point where saturation and switching losses are equal.

Figure 10–3. Typical Switching Losses at 300 V and 5.0 A (T_J = 100°C)



Control Circuits

Over the years, a variety of control ICs for SMPS have been introduced. The voltage mode controllers diagramed in Table 10–1 still dominate this market. The basic regulating function is performed in the pulse width modulator (PWM) section. Here, the dc feedback signal is compared to a fixed frequency sawtooth waveform. The result is a variable duty cycle pulse train which, with suitable buffer or interface circuits, can be used to drive the power switching transistor. Some ICs provide only a single output while others provide a phase splitter or flip–flop to alternately pulse two output channels. Additionally, most ICs provide an error amplifier and reference section shown as a means to process, compare and amplify the feedback signal.

Features required by a control IC vary to some extent because of the particular needs of a designer and on the circuit configuration chosen. However, most of today's current generation ICs have evolved with the following capabilities or features:

- Programmable (to 500 kHz) Fixed Frequency Oscillator
- Linear PWM Section with Duty Cycle from 0% to 100%
- On Board Error Amplifiers
- On Board Reference Regulator
- Adjustable Deadtime
- Under Voltage (low V_{CC}) Inhibit
- Good Output Drive (100 mA to 200 mA)
- Option of Single or Dual Channel Output
- Uncommitted Output Collector and Emitter or Totem Pole Drive Configuration
- Soft–Start
- Digital Current Limiting
- Oscillator Sync Capability

It is primarily the cost differences in these parts that determine whether all or only part of these features will be incorporated. Most of these are evident to the designer who has already started comparing competitive device data sheets.

In addition to the control circuits listed in Table 10–2, Motorola also has two dc converter control chips, the μA78S40 and the MC34063A. These chips feature an on–board 40 V, 2.0 A switching transistor and operate by dropping pulses from a fixed frequency, fixed duty cycle oscillator depending on load demand.

Today there is a demand for simple, low cost, single control ICs. These ICs, like Motorola's MC34060A and MC34063A components, are used to run the low–power flyback type configurations and are usually part of a three chip rather than a single chip system. The differences in these two approaches are illustrated in Figure 10–6.

When it is necessary to drive two or more power transistors, drive transformers are a practical interface element and are driven by the conventional dual channel ICs. In the case of a single transistor converter, however, it is usually more cost effective to directly drive the transistor from the IC. In this situation, an optocoupler is commonly used to couple the feedback signal from the output back to this control IC. And the error amplifier in this case is nothing more than a programmable zener like Motorola's TL431.

Overvoltage Protection

Linear and switching power supplies can be protected from overvoltage with a crowbar circuit. For linear supplies, the pass transistor can fail shorted, allowing high line transformer voltage to the load. For switching power supplies, a loose or disconnected remote sense lead can allow high voltage to the load.

3

Table 10–1. Basic SM Control ICs

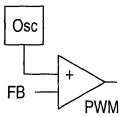
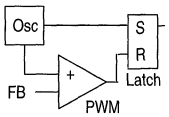
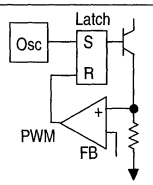
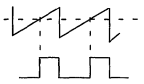
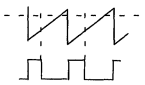
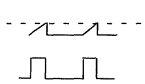
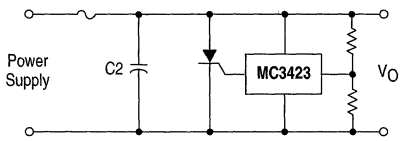
Control Technique	Type A Voltage Mode	Type B Voltage Mode w/Latch	Type C Current Mode
Schematic			
Single Channel Parts	MC34060A	—	UC3842 MC34129
Dual Channel Parts	TL494/594	SG3525A/27A SG3526	—
Features	Low Cost	Digital Current Limiting, Good Noise Immunity	Designed for Flyback, Inherent Feed Forward
PWM Waveforms Output			

Table 10–2. Control Circuits

Overvoltage Protection (OVP)		Over/Undervoltage Protection (O/UVP)	Undervoltage Sense MPU/MCU Reset
Standard	High Performance		
TL431	MC3423 TL431A	MC3425 MC34161	MC34064–5 MC34164–3 MC34164–5

The list of available circuits is shown in Table 10–2 and a typical 0 V application is shown in Figure 10–4. This crowbar circuit ignores noise spikes but will fire the SCR when a valid overvoltage condition is detected. The SCR will discharge C2 and either blow the fuse or cause the power supply to shut down.

Figure 10–4. Crowbar Circuit



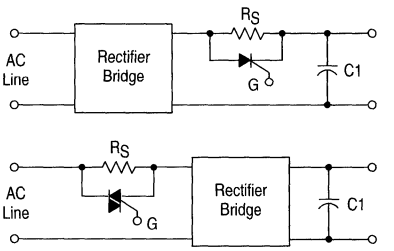
For further information, see the MC3423 data sheet.

Surge Current Protection

Many high current PWM switching supplies operate directly off the ac line. They have very large capacitive input filters with high inrush surge currents. The line circuit breaker and the rectifier bridge must be protected during turn–on.

Surge current limiting can be accomplished by adding R_S and an SCR short after charging C1, as shown in Figure 10–5, or by phase controlling the line voltage with a Triac.

Figure 10–5. Surge Current Limiting for a Switching Power Supply



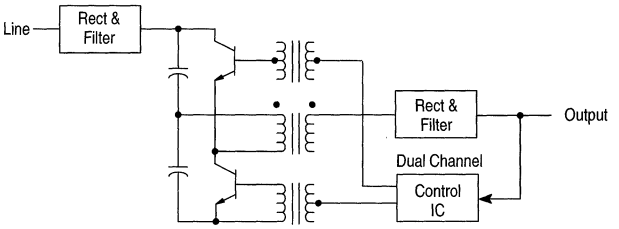
Transformer Design

With respect to transformer design, many of today's designers would say don't try it. They'd advise using a consultant or winding house to perform this task and with good reason. It takes quite a bit of time to develop a feel for this craft and be able to use both experience and intuition to find solutions to second and third order problems. Because of these subtle problems, most designers find that after the first paper design is done, as many as four or five lab iterations may be necessary before the transformer meets the design goals. However, there is a considerable design challenge in this area and a great deal of satisfaction can be obtained by mastering it.

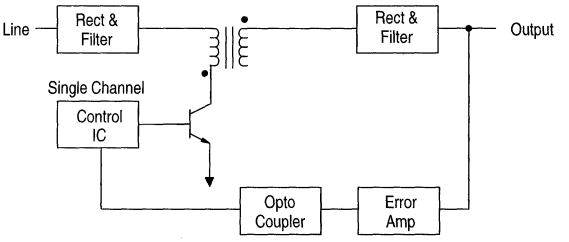
This component design, as do all others, begins by requesting all available literature from the appropriate manufacturers and then following this up with phone calls when specific questions arise. A partial list of companies is shown in Table 10–3. Designs below 20 W generally use pot cores, but for 20 W and above, E cores are preferred. E cores expose the windings to air so that heat is not trapped inside and make it easier to bring out connections for several windings. Remember that flyback designs require lower permeability cores than the others. The classic approach is to consult manufacturers charts like the one shown in Figure 10–8 and then to pick a core with the required power handling ability. Both E and EC (E cores with a round center leg) are popular now and they are available from several manufacturers. EC cores offer a performance advantage (better coupling) but standard E cores cost less and are also used in these applications. Another approach that seems to work equally well is to do a paper design of the estimated windings and turns required. Size the wire for 500 circular mils (CM) per amp and then find a core that has the required window area for this design. Now, before the windings are put on, it is a good idea to modify the turns so that they fit on one layer or an integral number of layers on that bobbin. This involves checking the turns per inch of the wire against the bobbin length. The primary generally goes on first and then the secondaries. If the primary hangs over an extra half layer, try reducing the turns or the wire size. Conversely, if the secondary does not take up a full layer, try bifilar winding (parallel) using wire half the size originally chosen (i.e., 3 wire sizes smaller, like 23 versus 20). This technique ultimately results in the use of foil for the higher current (20 A) low voltage windings. Most windings can be separated with 3 mil mylar (yellow) tape but for good isolation, cloth is recommended between primary and secondary.

Finally, once a mechanical fit has been obtained, it is time for the circuit tests. The isolation voltage rating is strictly a mechanical problem and is one of the reasons why cloth is preferred over tape between the primary and secondary. The inductance and saturating current level of the primary are inherent to the design, and should be checked in the circuit or other suitable test fixture. Such a fixture is shown in Figure 10–7 where the transistor and diode are sized to handle the anticipated currents. The pulse generator is run at a low enough duty cycle to allow the core to reset. Pulse width is increased until the start of saturation is observed (I_{sat}). Inductance is found using $L = E/(di/dt)$.

Figure 10–6. Control Circuit Topologies



(a) Single Chip System — Drive Transformer Isolation



(b) Three Chip System — Opto Coupler Isolation

In forward converters, the transformer generally has no gap in order to minimize the magnetizing current (I_M). For these applications the core should be chosen large enough so that the resulting LI product insures that I_M at operating voltages is less than I_{sat}. For flyback designs, a gap is necessary and the test circuit is useful again to evaluate the effect of the gap. The gap will normally be quite large, $Lg >> L_m/u$,

where, Lg = gap length
L_m = magnetic path length, and
u = permeability.

Under this stipulation, the gap directly controls the LI parameters and doubling it will decrease L by two and increase I_{sat} by two until fringing effects occur. Gaps of 5 mils to 20 mils are common. Again, the anticipated switching currents must be less than I_{sat} when the core is gapped for the correct inductance.

Table 10–3. Partial List of Core (C) and Transformer (T) Manufacturers

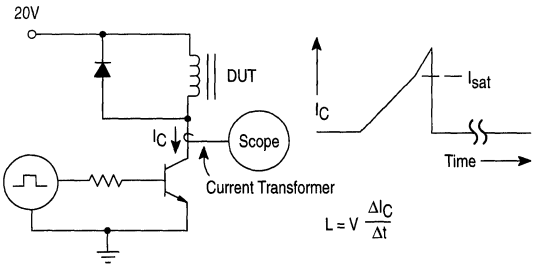
Company	Location	Code
Ferroxcube Inc.	Sauggerties, NY	C
Indiana General	Keasby, NJ	C
Stackpole	St. Marys, PA	C
TDK	El Segundo, CA	C
Pulse Engineering	San Diego, CA	T
Coilcraft	Cary, IL	T

Transformer tests in the actual supply are usually done with a high voltage dc power supply on the primary and with a pulse generator or other manual control for the pulse width (such as using the control IC in the open loop configuration). Here the designer must recheck three areas:

1. Core saturation
2. Correct amount of secondary voltage
3. Transformer heat rise

If problems are detected in any of these areas, the ultimate fix may be to redesign using the next larger core size. However, if problems are minimal, or none exist, it is possible to stay with the same core or even consider using the next smaller size.

Figure 10–7. Simple Coil Tester



Filter Capacitor Considerations

In today's 20 kHz switchers, aluminum electrolytics still predominate. The good news is that most have been characterized, improved, and cost reduced for this application. The input filter requires a voltage rating that depends on the peak line voltage; i.e., 400 V to 450 V for a 220 V switcher. If voltage is increased beyond this point, the capacitor will begin to act like a zener and be thermally destroyed from high leakage currents if the rating is exceeded for enough time. In doubler circuits, voltage sharing of the two capacitors in series can be a problem. Here extra voltage capability may be needed to make up for the imbalances caused by different values of capacitance and leakage current. A bleeder resistor is normally used here not only for safety but to mask the differences in leakage current. The RMS current rating is also an important consideration for input capacitors and is an example of improvements offered by today's manufacturers. Earlier "lytics" usually lacked this rating and often overheated. Large capacitors that were not needed for performance were used just to reduce this heating. However, today's devices offer lower thermal resistance, improved connection to the foil and good RMS ratings. A partial list of manufacturers that supply both high voltage input and the lower voltage output capacitors for switchers is shown in Table 10–4. Most of the companies offer not only the standard 85°C components, but devices with up to 125°C ratings which are required because of the high ambient temperatures (55° to 85°C) that many switchers have to operate in, many times without the benefit of fans.

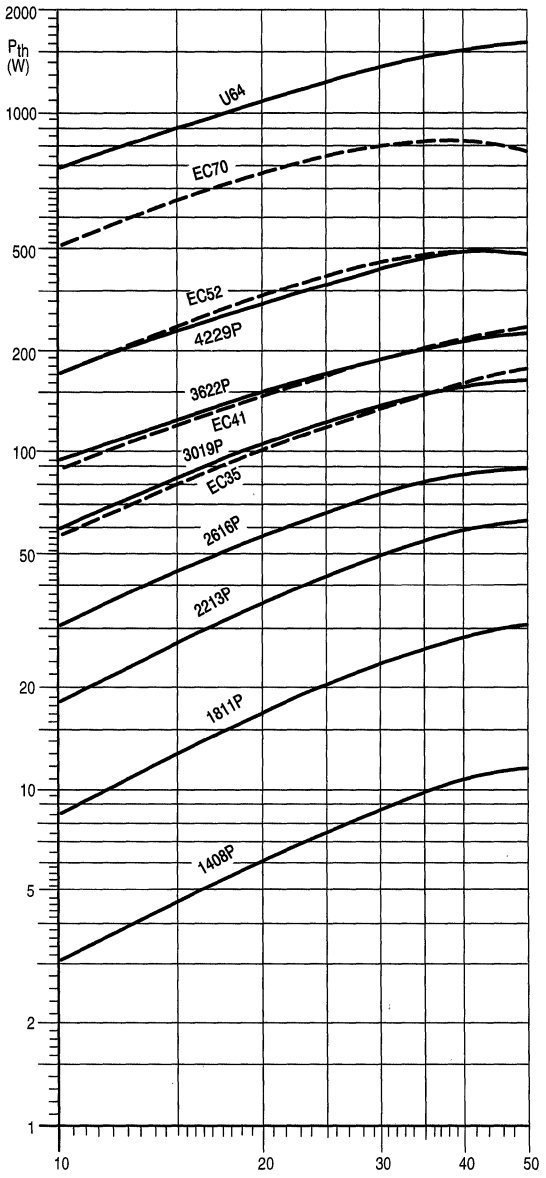
Table 10–4. Partial List of Capacitor Companies

Company (U.S.)	Location
MEPCO/Electra	Columbia, SC
Cornell–Dublier	Sanford, NC
Sangamo	Pickens, SC
Mallory	Indianapolis, IN

For output capacitors the buzz word is low ESR (equivalent series resistance). It turns out that for most capacitors even in the so–called "low ESR" series, the output ripple depends more on this resistance than on the capacitor value itself. Although typical and maximum ESR ratings are now available on most capacitors designed for switchers, the lead inductance generally is not specified except for the ultra–high frequency four terminal capacitors from some vendors. This parameter is responsible for the relatively high switching spikes that appear at the output. However, at this point in time, most designers find it less costly and more effective to add a high frequency noise filter rather than use a relatively expensive capacitor with low equivalent series inductance (ESL).

These LC noise or spike filters are made using small powdered iron toroids (1/2″ to 1″ OD) with distributed windings to minimize interwinding capacitance. And the output is bypassed using a small 0.1 μF ceramic or a 10 μF to 50 μF tantalum or both. Larger powered iron toroids are often used in the main LC output filter although the higher permeability ferrite EC and E cores with relatively large gaps can also be used. Calculations for the size of this component should take into account the minimum load so that the choke will not run "dry" as stated earlier.

Figure 10–8. Core Selection for Bridge Configurations (Reprinted from Ferroxcube Design Manual)



Note: Power handling decreases by a factor of 2 in forward and by 4 in flyback configurations.

SECTION 11
SWITCHING REGULATOR COMPONENT DESIGN TIPS

Transistors

The initial selection of a transistor for a switcher is basically a problem of finding the one with voltage and current capabilities that are compatible with the application. For the final choice performance and cost tradeoffs among devices from the same or several manufacturers have to be weighed. Before these devices can be put in the circuit, both protective and drive circuits will have to be designed.

Motorola's first line of devices for switchers were trademarked "Switchmode" transistors and introduced in the early 70's with data sheets that provided all the information that a designer would need including reverse bias safe operating area (RBSOA) and performance at elevated temperature (100°C). The first series was the 2N6542 through 2N6547, TO–204 (TO–3) and was followed by the MJE13002 through MJE13009 series in a plastic TO–220 package. Finally, high voltage (1.0 kV) requirements were met by the metal MJ8500 thru MJ8505 series and the plastic MJE8500 series. The Switchmode II series is an advanced version of Switchmode I that features faster switching. Switchmode III is a state of the art bipolar with exceptional speed, RBSOA, and up to 1.5 kV blocking capacity. Here, device cost is somewhat higher, but system costs may be lowered because of reduced snubber requirements and higher operating frequencies. A similar argument applies to Motorola TMOS Power FETs. These devices make it possible to switch efficiently at higher frequencies (200 kHz to 500 kHz) but the main selling point is that they are easier to drive. This latter point is the one most often made to show that systems savings are again quite possible even though the initial device cost is higher.

Table 11–1. Motorola High Voltage Switching Transistor Technologies

Family	Typical Device	Typical Fall Time	Approximate Switching Frequency
SWITCHMODE I	2N6545 MJE13005 MJE12007	200 ns to 500 ns	20 k
SWITCHMODE II	MJ13081	100 ns	100 k
SWITCHMODE III	MJ16010	50 ns	200 k
TMOS	MTP5N40	20 ns	500 k

Table 11–2 is a chart of the transistor voltage requirements for the various off–line converter circuits. As illustrated, the most stringent requirement for single transistor circuits (flyback and forward) is the blocking or V_{CEV} rating. Bridge circuits, on the other hand, turn on and off from the dc bus and their most critical voltage is the turn–on or $V_{CEO(sus)}$ rating.

Table 11–2. Power Transistor Voltage Chart

Line Voltage	Circuit			
	Flyback, Forward or Push–Pull		Half or Full–Bridge	
	V_{CEV}	$V_{CEO(sus)}$	$V_{CEO(sus)}$	V_{CEV}
220 120	850 kV to 1.0 kV 450	450 250	450 250	450 250

Most switchmode transistor load lines are inductive during turn–on and turn–off. Turn–on is generally inductive because the short circuit created by output rectifier reverse recovery times is isolated by leakage inductance in the transformer. This inductance effectively snubs most turn–on load lines so that the rectifier recovery (or short circuit) current and the input voltage are not applied simultaneously to the transistor. Sometimes primary interwinding capacitance presents a small current spike but usually turn–on transients are not a problem. Turn–off transients due to this same leakage inductance, however, are almost always a problem. In bridge circuits, clamp diodes can be used to limit these voltage spikes. If the resulting inductive load line exceeds the transistor's reverse bias switching capability (RBSOA) then an RC network may also be added across the primary to absorb some of this transient energy. The time constant of this network should equal the anticipated switching time of the transistor (50 ns to 500 ns). Resistance values of 100 Ω to 1000 Ω in this RC network are generally appropriate. Trial and error will indicate how low the resistor has to be to provide the correct amount of snubbing. For single transistor converters, the circuits shown in Figure 11–1 are generally used.

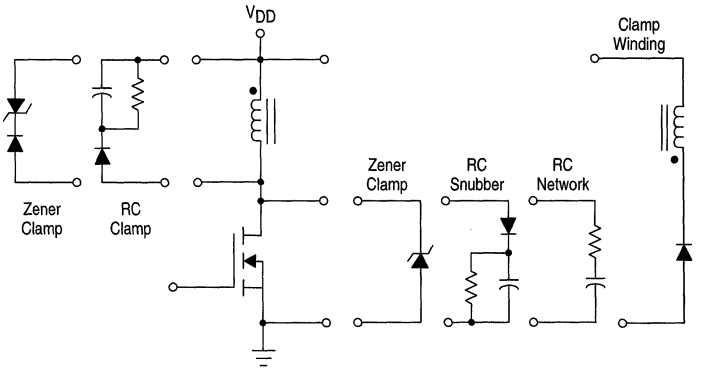
Here slightly different criteria are used to define the R and C snubber values:

$$C = \frac{I\, t_f}{V}$$

where; I = the peak switching current
t_f = the transistor fall time
V = the peak switching voltage (Approximately twice the DC bus)
also, $R = t_{on}/C$ (it is not necessary to completely discharge this capacitor in order to obtain the desired effects of this circuit)
where, t_{on} = the minimum on–time or pulse width
and, $P_R = \frac{CV^2f}{2}$
where, P_R = the power rating of the resistor
and, f = the operating frequency.

In most of today's designs snubber elements are small or nonexistent and voltage spikes from energy left in the leakage inductance a more critical problem depending on how good the coupling is between the primary and clamp windings and how fast the clamp diode turns on. FETs often have to be slowed down to prevent self destruction from this spike.

Figure 11–1. Protection Circuits for Switching Transistors



Zener and Mosorb Transient Suppressors

If necessary, protection from voltage spikes may be obtained by adding a zener and rectifier across the primary as shown in Figure 11–1. Here Motorola's 5.0 W zener lines with ratings up to 200 V, and 10 W TO–220 Mosorbs with ratings up to 250 V can provide the clamping or spike limiting function. If the zener must handle most of the power, its size can be estimated using:

$$P_Z = \frac{L_L I^2 f}{2}$$

where, P_Z = the zener power rating
and, L_L = the leakage inductance (measured with the clamp winding or secondary shorted)
I = peak collector current
f = operating frequency

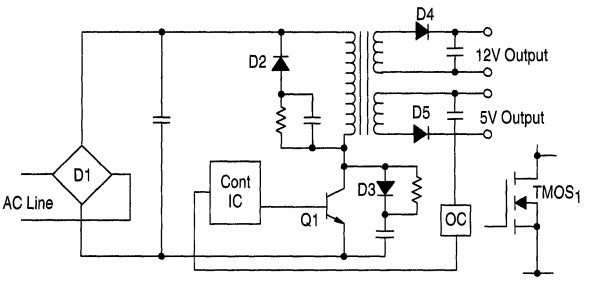
Distinction is sometimes made between devices trademarked Mosorb (by Motorola, Inc.), and standard zener/avalanche diodes used for reference, low–level regulation and low–level protection purposes. It must be emphasized that Mosorb devices are, in fact, zener diodes. The basic semiconductor technology and processing are identical. The primary difference is in the applications for which they are designed. Mosorb devices are intended specifically for transient protection purposes and are designed, therefore, with a large effective junction area that provides high pulse power capability while minimizing the total silicon use. Thus, Mosorb pulse power ratings begin at 600 W — well in excess of low power conventional zener diodes which in many cases do not even include pulse power ratings among their specifications.

MOVs, like Mosorbs, do have the pulse power capabilities for transient suppression. They are metal oxide varistors (not semiconductors) that exhibit bidirectional avalanche characteristics, similar to those of back–to–back connected zeners. The main attributes of such devices are low manufacturing cost, the ability to absorb high energy surges (up to 600 joules) and symmetrical bidirectional "breakdown" characteristics. Major disadvantages are: high clamping factor, an internal wear–out mechanism and an absence of low–end voltage capability. These limitations restrict the use of MOVs primarily to the protection of insensitive electronic components against high energy transients in applications above 20 V, whereas, Mosorbs are best suited for precise protection of sensitive equipment even in the low voltage range the same range covered by conventional zener diodes.

Rectifiers

Once components for the inverter section of a switcher have been chosen, it is time to determine how to get power into and out of this section. This is where the all–important rectifier comes into play. (See Figure 11–2.) The input rectifier is generally a standard recovery bridge that operates off the ac line and into a capacitive filter. For the output section, most designers use Schottkys for efficient rectification of the low voltage, 5.0 V output windings and for the higher voltage, 12 V to 15 V outputs, the more economical fast recovery or ultrafast diodes are used.

Figure 11–2. Switchmode Power Supply Flyback or Boost Design



D1 — Bridge Rectifier — Line Voltage
D2 — Clamp Diode — HV/Fast–Ultrafast
D3 — Snubber Diode — HV/Fast–Ultrafast
D4 — Output Rectifier — Fast/Ultrafast
D5 — Output Rectifier — Schottky

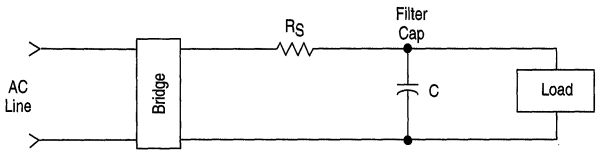
For the process of choosing an input rectifier, it is useful to visualize the circuit shown in Figure 11–3. To reduce cost, most earlier approaches of using choke input filters, soft start relays (Triacs), or SCRs to bypass a large limiting resistor have been abandoned in favor of using small limiting resistors or thermistors and a large bridge. The bridge must be able to withstand the surge currents that exist from repetitive starts at peak line. The procedure for finding the right component and checking its fit is as follows:

1. Choose a rectifier with 2 to 5 times the average I_O required.
2. Estimate the peak surge current (I_p) and time (t) using:

$$I_p = \frac{1.4\ V_{in}}{R_S} \qquad t = R_S C$$

Where V_{in} is the RMS input voltage; R_S is the total series resistance; and C is the filter capacitor size.

Figure 11–3. Choosing Input Rectifiers



3. Compare this current pulse to the sub cycle surge current rating (I_S) of the diode itself. If the curve of I_S versus time is not given on the data sheet, the approximate value for I_S at a particular pulse width (t) may be calculated knowing:
   - I_{FSM} — the single cycle (8.3 ms) surge current rating and using.
   - $I^2\sqrt{t}$ = K, which applies when the diode temperature rise is controlled by its thermal response as well as power (i.e., $T = K'P\sqrt{t}$ for t < 8.0 ms).

   This gives:

$$I_S^2\sqrt{t} = I_{FSM}^2\sqrt{8.3\ ms} \quad \text{or,} \quad I_S = I_{FSM}\left(\frac{8.3\ ms}{t}\right)^{1/4}, \text{ t is in milliseconds.}$$

4. If $I_S < I_P$, consider either increasing the limiting resistor (R_S) or utilizing a larger diode.

In the output section where high frequency rectifiers are needed, there are several types available to the designer. In addition to the Schottky (SBR) and fast recovery (FR), there is also an ultrafast recovery (UFR). Comparative performance for devices with similar current ratings is shown in Table 11–3. The obvious point here is that lower forward voltage improves efficiency and lower recovery times reduce turn–on losses in the switching transistors, but the tradeoff is higher cost. As stated earlier, Schottkys are generally used for 5.0 V outputs and fast recovery and ultrafast devices for 12 V outputs and greater. The ultrafast is competing both with the Schottky where higher breakdown is needed and with the fast recovery in those applications where performance is more important than cost. Ten years ago Schottkys were very fragile and could fail short from either excessive dv/dt (1.0 V to 5.0 V per nanosecond) or reverse avalanche. Since that time, Motorola has incorporated a "guard ring" or internal zener which minimizes these earlier problems and reduces the need for RC snubbers and other external protective networks.

Table 11–3. Motorola Rectifier Product Portfolio

Parameter	Schottky	Ultrafast	Fast Recovery	Standard Recovery
Forward Voltage (V_F)	0.5 V to 0.6 V	0.9 V to 1.0 V	1.2 V to 1.4 V	1.2 V to 1.4 V
Reverse Recovery Time (t_{rr})	<10 ns	25 ns to 100 ns	150 ns	1.0 μs
t_{rr} Form	Soft	Soft	Soft	Soft
DC Blocking Voltage (V_R)	20 V to 60 V	50 V to 1000 V	50 V to 1000 V	50 V to 1000 V
Cost Ratio	3:1	3:1	2:1	1:1

SECTION 12
BASIC SWITCHING POWER SUPPLY CONFIGURATIONS

The implementation of switching power supplies by the non–specialist is becoming increasingly easy due to the availability of power devices and control ICs especially developed for this purpose by the semiconductor manufacturer.

This section is meant to help in the preliminary selection of the devices required for the implementation of the listed switching power supplies.

Flyback and Forward Converter Switching Power Supplies (50 W to 250 W)

- Input line variation: V_{in} + 10%, – 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ variation: $\delta_{(max)} = 0.4$)
- Maximum Transistor working current:

$$I_W = \frac{2.0\ P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{5.5\ P_{out}}{V_{in}} \text{ (Flyback)}$$

$$= \frac{P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{2.25\ P_{out}}{V_{in}} \text{ (Forward)}$$

- Maximum transistor working voltage: $V_W = 2 \times V_{in(max)} \times \sqrt{2}$ + guardband
- Working frequency: f = 20 kHz to 200 kHz

Basic Flyback Configuration

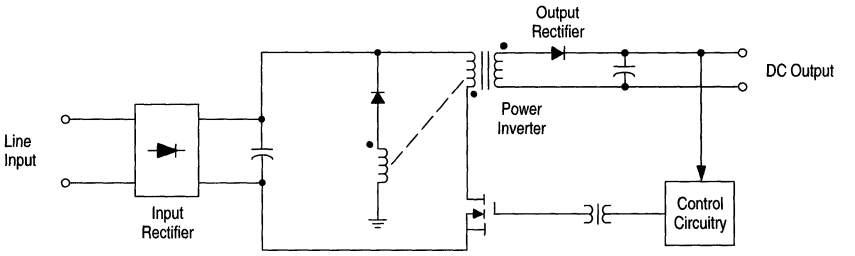


Table 12–1. Flyback and Forward Converter Semiconductor Selection Chart

Output Power	50 W		100 W		175 W		250 W
Input Line Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V	120 V
MOSFET Requirements: Max Working Current (I_W) Max Working Voltage (V_W)	 2.25 A 380 V	 1.2 A 750 V	 4.0 A 380 V	 2.5 A 750 V	 8.0 A 380 V	 4.4 A 750 V	 11.4 A 380 V
Power MOSFETs Recommended: Metal (TO–204AA) (TO–3) Plastic (TO–220AB) Plastic (TO–218AC)	 MTM4N45 MTP4N45 —	 MTM2N90 MTP2N90 —	 MTM4N45 MTP4N45 —	 MTM2N90 MTP2N90 —	 MTM7N45 — MTH7N45	 MTM4N90 — —	 MTM15N45 — —
Input Rectifiers: Max Working Current (I_W) Recommended Types	 0.4 A MDA104A	 0.25 A MDA106A	 0.4 A MDA206	 0.5 A MDA210	 2.35 A MDA970	 1.25 A MDA210	 4.6 A MDA3506
Output Rectifiers: Recommended types for Output Voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MUR3010PT MUR1615CT MUR1615CT MUR 440, MUR840A		 MBR3035PT MUR3010PT MUR1615CT MUR1615CT MUR840A		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902						

Flyback and Forward Converters

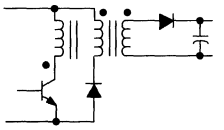
To take advantage of the regulating techniques discussed earlier and also provide isolation, a total of seven popular configurations have evolved and are listed below. Each circuit has a practical power range or capability associated with it as follows:

Circuit	Power Range	Parts Cost
DC Converter	5.0 W	$ 4.00
Converter w/30 V Transformer	10 W	7.00
Blocking OSC	20 W	10.00
Flyback	50 W	15.00
Forward	100 W	20.00
Half–Bridge	200 W	30.00
Full–Bridge	500 W	75.00

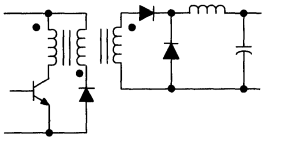
First to be discussed will be the low power (20 W to 200 W) converters which are dominated by the single transistor circuits shown in Figure 12–1. All of these circuits operate the magnetic element in the unipolar rather than bipolar mode. This means that transformer size is sacrificed for circuit simplicity.

The flyback (alternately known as the "ringing choke") regulator stores energy in the primary winding and dumps it into the secondary windings, see Figure 12–1(a). A clamp winding is usually present to allow energy stored in the leakage reactance to return safely to the line instead of avalanching the switching transistor. The operating model for this circuit is the buck–boost discussed earlier. The flyback is the lowest cost regulator because output filter chokes are not required since the output capacitors feed from a current source rather than a voltage source. It does have higher output ripple than the forward converters because of this. However, it is an excellent choice when multiple output voltages are required and does tend to provide better cross regulation than the other types. In other words changing the load on one winding will have little effect on the output voltage of the others.

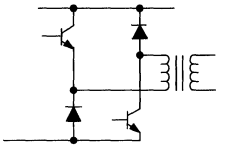
Figure 12–1. Low Power Popular (20 to 200 W) Converter Configurations



(a) Flyback (Clamp Winding is Optional)



(b) Forward (Clamp Winding is Necessary)

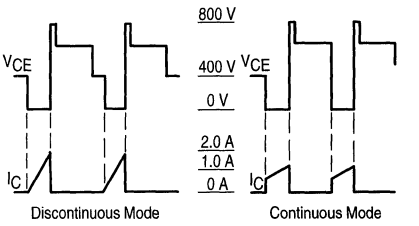


(c) Two Transistor Forward or Flyback
(Clamp Winding is not Needed)

A 120/220 Vac flyback design requires transistors that block twice the peak line plus transients or about 1.0 kV. Motorola's MJE13000 and 16000A series with ratings of 750 V to 1000 V are normally used here. These bipolar devices are relatively fast (100 ns) and are typically used in the 20 kHz to 50 kHz operating frequency range. The recent availability of 900 V and 1000 V TMOS FETs allows designers to operate in the next higher range (50 kHz to 80 kHz) and some have even gone as high as 300 kHz with square wave designs and FETs. Faster 1.0 kV bipolar transistors are also planned in the future and will provide another design alternative. The two transistor variations of this circuit, Figure 12–1(c), eliminate the clamp winding and add a transistor and diode to effectively clamp peak transistor voltages to the line. With this circuit a designer can use the faster 400 V to 500 V FET transistors and push operating frequencies considerably higher. There is a cost penalty here over the single transistor circuit due to the extra transistor, diodes and gate drive circuitry.

A subtle variation in the method of operation can be applied to the flyback regulator. The difference is referred to as operation in the discontinuous or continuous mode and the waveform diagrams are shown in Figure 12–2. The analysis given in the earlier section on boost regulators dealt strictly with the discontinuous mode where all the energy is dumped from the choke before the transistor turns on again. If the transistor is turned on while energy is still being dumped into the load, the circuit is operating in the continuous mode. This is generally an advantage for the transistor in that it needs to switch only half as much peak current in order to deliver the same power to the load. In many instances, the same transformer transformer may be used with only the gap reduced to provide more inductance. Sometimes the core size will need to be increased to support the higher LI product (2 to 4 times) now required because the inductance must increase by almost 10 times to effectively reduce the peak current by two. In dealing with the continuous mode, it should also be noted that the transistor must now turn on from 500 V to 600 V rather than 400 V level because there no longer is any deadtime to allow the flyback voltage to settle back down in the input voltage level. Generally, it is advisable to have $V_{CEO(sus)}$ ratings comparable to the turn–on requirements except for SMIII where turn–on up to V_{CEV} is permitted.

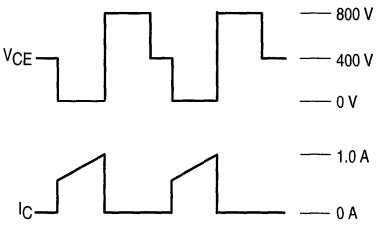
Figure 12–2. Flyback Transistor Waveforms



The flyback converter stands out from the others in its need for a low inductance, high current primary. Conventional E and pot core ferrites are difficult to work with because their permeability is too high even with relatively large gaps (50 to 100 milli–inches). The industry needs something better that will provide permeabilities of 60 to 120 instead of 2000 to 3000 for this application.

The single transistor forward converter is shown in Figure 12–1(b). Although it initially appears very similar to the flyback, it is not. The operating model for this circuit is actually the buck regulator discussed earlier. Instead of storing energy in the transformer and then delivering it to the load, this circuit uses the transformer in the active or forward mode and delivers power to the load while the transistor is on. The additional output rectifier is used as a freewheeling diode for the LC filter and the third winding is actually a reset winding. It generally has the same turns as the primary, (is usually bifilar wound) and does clamp the reset voltage to twice the line. However, its main function is to return energy stored in the magnetizing inductance to the line and thereby reset the core after each cycle of operation. Because it takes the same time to set and reset the core, the duty cycle of this circuit cannot exceed 50%. This also is a very popular low power converter and like the flyback is practically immune from transformer saturation problems. Transistor waveforms shown in Figure 12–3 illustrate that the voltage requirements are identical to the flyback. For the single transistor versions, 400 V turn–on and 1.0 kV blocking devices like the MJE13000 and MJE16000 transistors are required. The two transistor circuit variations shown in Figure 12–1(b) again adds a cost penalty but allows a designer to use the faster 400 V to 500 V devices. With this circuit, operation in the discontinuous mode refers to the time when the load is reduced to a point where the filter choke runs "dry." This means that choke current starts at and returns to zero during each cycle of operation. Most designers prefer to avoid this type of mode because of higher ripple and noise even though there are no adverse effects on the components themselves. Standard ferrite cores work fine here and in the high power converters as well. In these applications, no gap is used as the high permeability (3000) results in the desirable effect of very low magnetizing current levels. And, zeners or RC clamps may be used to reset the core in lieu of the clamp winding to lower the voltage stress on the switching transistors.

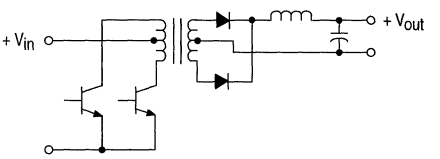
Figure 12–3. Forward Converter Transistor Waveforms



Push–Pull and Bridge Converters

The high power circuits shown in Figures 12–4 to 12–7 all operate the magnetic element in the bipolar or push–pull mode and require 2 to 4 inverter transistors. Because the transformers operate in this mode they tend to be almost half the size of the equivalent single transistor converters and thereby provide a cost advantage over their counterparts at power levels of 200 kW to 1.0 kW.

Figure 12–4. Push–Pull Converter (200 W to 1.0 kW)



The push–pull converter shown in Figure 12–4 is one of the oldest converter circuits around. Its early use was in low voltage inverters such as the 12 Vdc to 120 Vdc power source for recreational vehicles and in dc to dc converters. Because these converters are free running rather than driven and operate from low voltages, transformer saturation problems are minimal. In the high voltage off–line switchers, saturation problems are common and were difficult to solve. The transistors are also subjected to twice the peak line voltage which requires the use of high voltage (1.0 kV) transistors. Both of these drawbacks have tended to discourage designers of off–line switchers from using this configuration until current mode control ICs were introduced. Now these circuits are being looked at with renewed interest.

Push–Pull Switching Power Supplies (100 W to 500 W)

- Input line variation: V_{in} + 10%, – 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: $\delta_{(max)}$ = 0.8
- Maximum transistor working current:

$$I_W = \frac{P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{1.4\ P_{out}}{V_{in}}$$

- Maximum transistor working voltage: $V_W = 2 \times V_{in(max)} \times \sqrt{2}$ + guardband
- Working frequency: f = 20 kHz to 200 kHz

Basic Push–Pull Configuration

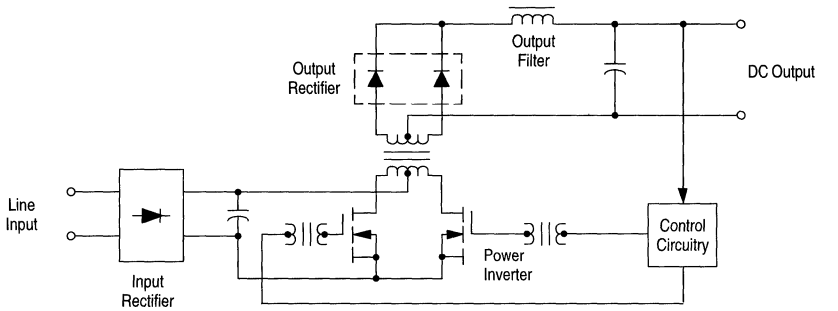


Table 12–2. Push–Pull Semiconductor Selection Chart

Output Power	100 W		250 W		500 W	
Input Line Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Current (I_W) Max Working Voltage (V_W)	 1.2 A 380 V	 0.6 A 750 A	 2.9 A 380 V	 1.6 A 750 V	 5.7 A 380 V	 3.1 A 750 V
Power MOSFETs Recommended: Metal (TO–204AA) (TO–3) Plastic (TO–220AB) Plastic (TO–218AC)	 MTM2N50 MTP2N45 —	 MTM2N90 MTP2N90 —	 MTM4N45 MTP4N45 —	 MTM2N90 MTP2N94 —	 MTM7N45 — MTH7N45	 MTM4N90 — —
Input Rectifiers: Max Working Current (I_W) Recommended Types	 0.9 A MDA206	 0.5 A MDA210	 2.35 A MDA970–5	 1.25 A MDA210	 4.6 A MDA3506	 2.5 A MDA3510
Output Rectifiers: Recommended types for output voltages of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MBR3045PT, MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902					

Half–Bridge/Full–Bridge Switching Power Supplies (100 W to 500 W/500 W to 1000 W)

- Input line variation: V_{in} + 10%, – 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: $\delta_{(max)}$ = 0.8
- Maximum working current:

$$I_W = \frac{2\,P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{2.8\,P_{out}}{V_{in}} \quad \text{(Half–Bridge)}$$

$$= \frac{P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{1.4\,P_{out}}{V_{in}} \quad \text{(Full–Bridge)}$$

- Maximum transistor working voltage: $V_W = V_{in(max)} \times \sqrt{2}$ + guardband
- Working frequency: f = 20 kHz to 200 kHz

Basic Half–Bridge Configuration

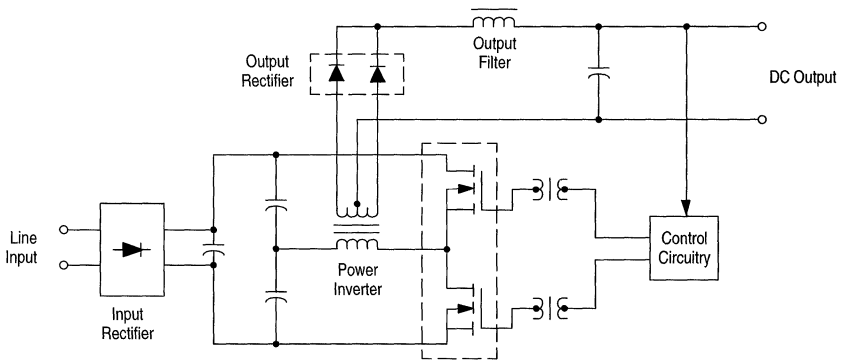


Table 12–3. Half–Bridge Semiconductor Selection Chart

Output Power	100 W		350 W		500 W	
Input Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Current (I_W) Max Working Voltage (V_W)	 2.3 A 190 V	 1.25 A 380 V	 5.7 A 190 V	 3.1 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended: Metal (TO–204AA) (TO–3) Plastic (TO–220AB) Plastic (TO–218AC)	 MTM5N35 MTP3N40 —	 MTM2N45 MTP2N45 —	 MTM8N40 — MTH8N40	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 — MTH7N45
Input Rectifiers: Max Working Current (I_W) Recommended Types	 0.9 A MDA206	 0.5 A MDA210	 2.3 A MDA970–5	 1.25 A MDA210	 4.6 A MDA3506	 2.5 A MDA3510
Output Rectifiers: Recommended types for output voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MBR3045PT, MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902					

Half and Full–Bridge

The most popular high power converter is the half–bridge (Figure 12–6). It has two clear advantages over the push–pull and became the favorite rather quickly. First, the transistors never see more than the peak line voltage and the standard 400 V fast switchmode transistors that are readily available may be used. And second, and probably even more important, transformer saturation problems are easily minimized by use of a small coupling capacitor (about 2.0 μF to 5.0 μF) as shown above. Because the primary winding is driven in both directions, a full–wave output filter, rather than half, is now used and the core is actually utilized more effectively. Another more subtle advantage of this circuit is that the input filter capacitors are placed in series across the rectified 220 V line which allows them to be used as the voltage doubler elements on a 120 V line. This still allows the inverter transformer to operate from a nominal 320 V bus when the circuit is connected to either 120 V or 220 V. Finally, this topology allows diode clamps across each transistor to contain destructive switching transients. The designer's dream, of course, is for fast transistors that can handle a clamped inductive load line at rated current. And a few (like the MJE16000 series from Motorola) are beginning to appear on the market. With the improved RBSOA that these transistors feature, less snubbing is required and this improves both the cost and efficiency of these designs.

Figure 12–5. Half–Bridge Converter with Split Windings

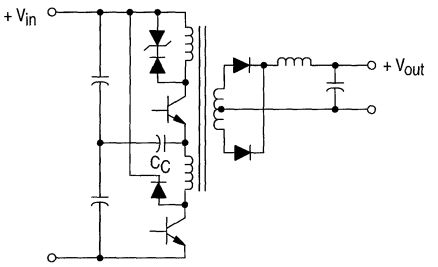
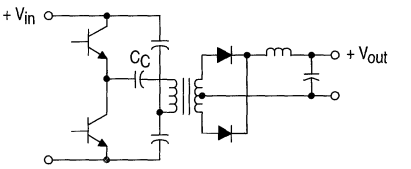


Figure 12–6. Half–Bridge Converter (200 W to 1.0 kW)



Basic Full–Bridge Configuration

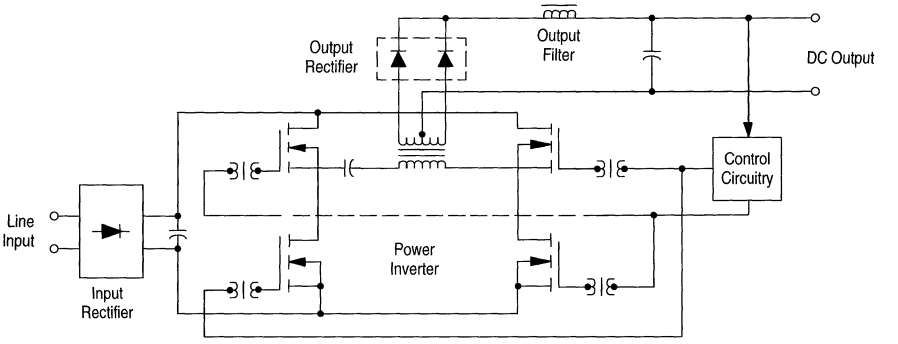


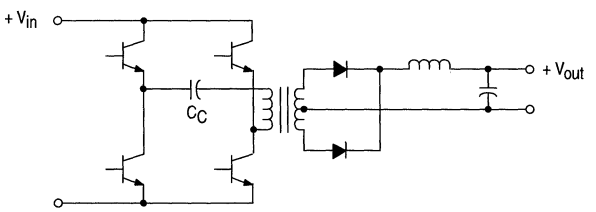
Table 12–4. Full–Bridge Semiconductor Selection Chart

Output Power	500 W		750 W		1000 W	
Input Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Curren (I_W) Max Working Voltage (V_W)	 5.7 A 190 V	 3.1 A 380 V	 8.6 A 190 V	 4.7 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended: Metal (TO–204AA) (TO–3) Plastic (TO–220AB) Plastic (TO–218AC)	 MTM8N20 MTP8N20 —	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 MTP4N45 MTH7N45	 MTM15N20 MTP12N20 MTH15N20	 MTM7N45 — MTH7N45
Input Rectifiers: Max Working Current (I_W) Recommended Types	 4.6 A MDA3506	 2.5 A MDA3510	 7.0 A	 3.8 A	 9.25 A	 5.0 A
Output Rectifiers: Recommended types for output voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR804PT		 MBR30035CT MUR10010CT* MUR10015CT MUR3015PT* MUR3040PT		 MBR30035CT* MUR10010CT* MUR10015CT* MUR10015CT MUR3040PT	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902					

*More than one device per leg, matched.

The effective current limit of today's low cost TO–218 discrete transistors (250 mil die) is somewhere in the 10 A to 20 A area. Once this limit is reached, the designer generally changes to the full–bridge configurations shown in Figure 12–7. Because full line rather than half is applied to the primary winding, the power out can be almost double that of the half–bridge with the same switching transistors. Power Darlington transistors are a logical choice for higher power control with current, voltage and speed capabilities allowing very high performance and cost effective designs. Another variation of the half–bridge is the split winding circuit, shown in Figure 12–5. A diode clamp can protect the lower transistor but a snubber or zener clamp must still be used to protect the top transistor from switching transients. Because both emitters are at an ac ground point, expensive drive transformers can now be replaced by lower cost capacitively–coupled drive circuits.

Figure 12–7. Full–Bridge Converter (200 W to 1.0 kW)



SECTION 13
SWITCHING REGULATOR DESIGN EXAMPLES

In addition to the application materials in this data book, Motorola publishes several application notes which contain basic information on the design of power supplies using a variety of Motorola Analog ICs. AN920 describes in detail the principles of operation of the MC34063A and μA78S40 Switching Regulator Subsystems. Several converter design examples and numerous applications circuits with test data are included in this application note. The circuit techniques described in this note are also applicable to the MC34163 and MC34165 Power Switching Regulators.

Operating details of the MC34129 Current Mode Switching Regulator Controller, and examples of its use with Motorola SENSEFET™ products, are provided in AN976. The application note AN983 focuses on a 400 W half-bridge power supply design which uses the TL494 PWM control circuit. The TL594 can be used in this same application.

Essentially all of the data sheets for newer power supply control and supervisory circuits include extensive applications information with test conditions and performance results. Many data sheets also include printed circuit board layouts for some key applications so that the designer can evaluate the integrated circuits in an actual power supply. This data book presents all data sheets in their entirety so that the applications information is readily available for each device.

3

SECTION 14

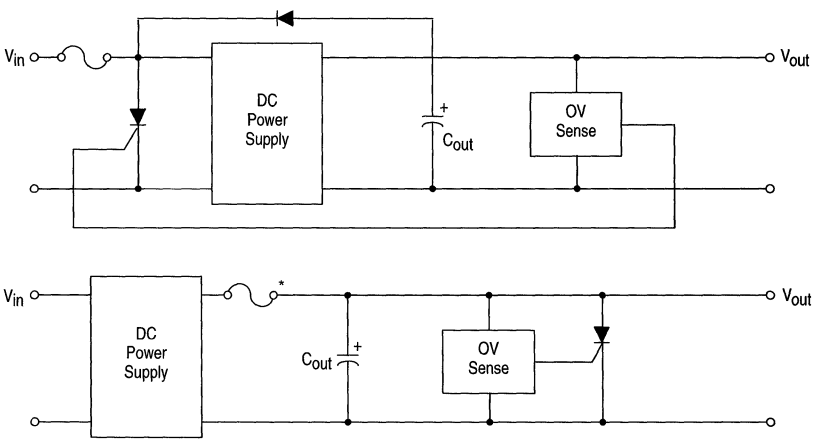
POWER SUPPLY SUPERVISORY AND PROTECTION CONSIDERATIONS

The use of SCR crowbar overvoltage protection (OVP) circuits has been, for many years, a popular method of providing protection from accidental overvoltage stress for the load. In light of the recent advances in LSI circuitry, this technique has taken on added importance. It is not uncommon to have several hundred dollars worth of electronics supplied from a single low voltage supply. If this supply were to fail due to component failure or other accidental shorting of higher voltage supply busses to the low voltage bus, several hundred dollars worth of circuitry could literally go up in smoke. The small additional investment in protection circuitry can easily be justified in such applications.

A. The Crowbar Technique

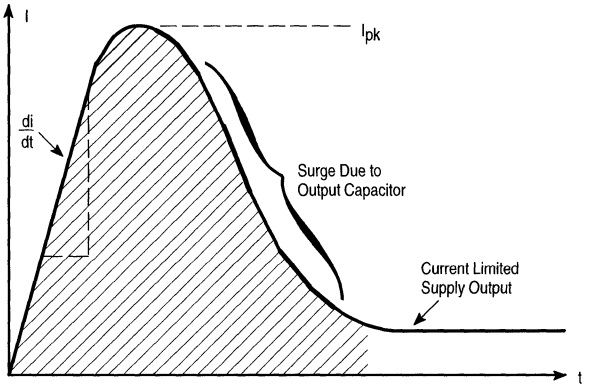
One of the simplest and most effective methods of obtaining overvoltage protection is to use a "crowbar" SCR placed across the equipment's dc power supply bus. As the name implies, the SCR is used much like a crowbar would be, to short the dc supply when an overvoltage condition is detected. Typical circuit configurations for this circuit are shown on Figure 14–1. This method is very effective in eliminating the destructive overvoltage condition. However, the effectiveness is lost if the OVP circuitry is not reliable.

Figure 14–1. Typical Crowbar OVP Circuit Configurations



*Needed if supply not current–limited.

Figure 14–2. Crowbar SCR Surge Current Waveform



B. SCR Considerations

Referring to Figure 14–1, it can easily be seen that, when activated, the crowbar SCR is subjected to a large current surge from the filter and output capacitors. This large current surge, illustrated in Figure 14–2, can cause SCR failure or degradation by any one of three mechanisms: di/dt, peak surge current, or I2 t. In many instances the designer must empirically determine the SCR and circuit elements which will result in reliable and effective OVP operation. To aid in the selection of devices for this application, Motorola has characterized several devices specifically for crowbar applications. A summary of these specifications and a selection guide for this application is shown in Table 14–1. This significantly reduces the amount of empirical testing that must be done by the designer. A good understanding of the factors that influence the SCR's di/dt and surge current capability will greatly simplify the total circuit design task.

Table 14–1. Crowbar SCRs

Device Type**	Peak Discharge Current*	di/dt*
MCR67	300 A	75 A/μs
MCR68	300 A	75 A/μs
MCR69	750 A	100 A/μs
MCR70	850 A	100 A/μs
MCR71	1700 A	200 A/μs

* tw = 1.0 μs, exponentially decaying

** All devices available with 25, 50, and 100 V ratings

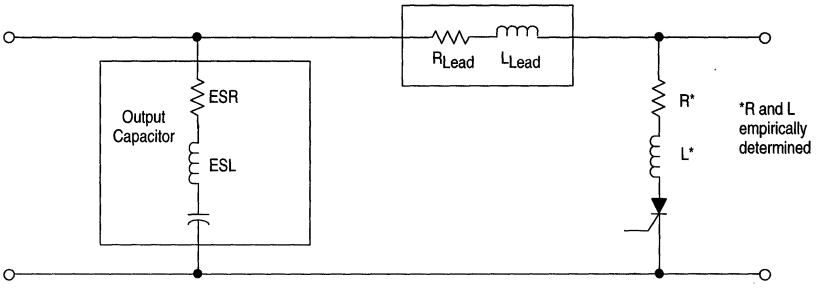
1. di/dt — As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned–on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities, depending upon the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center–gate–fire SCR has more di/dt capability than a corner–gate–fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast <1.0 μs rise time signal will maximize its di/dt capability. A typical maximum di/dt in phase control SCRs of less than 50 A rms rating might be 200 A/μs, assuming a gate current of five times IGT and <1.0 μs rise time. If having done this, a di/dt problem still exists, the designer can also decrease the di/dt of the current saveform by adding inductance in series with the SCR, as shown in Figure 14–3. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage, and a tradeoff must be made between speedy voltage reduction and di/dt.

2. Surge Current — If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance, see Figure 14–3) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

3

Figure 14–3. Circuit Elements Affecting SCR Surge & di/dt



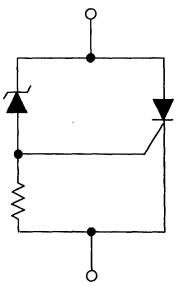
(For additional information on SCRs in crowbar applications refer to *Characterizing the SCR for Crowbar Applications*, Al Pshaenich, Motorola AN789).

C. The Sense and Drive Circuit

In order to maximize the crowbar SCR's di/dt capability, it should receive a fast rise time high–amplitude gate–drive signal. This must be one of the primary factors considered when selecting the sensing and drive circuitry. Also important is the sense circuitry's noise immunity.

Noise immunity can be a major factor in the selection of the sense circuitry employed. If the sensing circuit has low immunity and is operated in a noisy environment, nuisance tripping of the OVP circuit can occur on short localized noise spikes, which would not normally damage the load. This results in excessive system down time. There are several types of sense circuits presently being used in OVP applications. These can be classified into three types: zener, discrete, and "723."

Figure 14–4. The Zener Sense Circuit



1. The Zener Sense Circuit — Figure 14–4 shows the use of a zener to trigger the crowbar SCR. This method is NOT recommended since it provides very poor gate drive and greatly decreases the SCR's di/dt handling capability, especially since the SCR steals its own very necessary gate drive as it turns on. Additionally, this method does not allow the trip point to be adjusted except by zener replacement.

2. The Discrete Sense Circuit — A technique which can provide adequate gate drive and an adjustable, low temperature coefficient trip point is shown in Figure 14–5. While overcoming the disadvantages of the zener sense circuit, this technique requires many components and is more costly. In addition, this method is not particularly noise immune and often suffers from nuisance tripping.

3. The "723" Sense Circuit — By using an integrated circuit voltage regulator, such as the industry standard "723" type, a considerable reduction in component count can be achieved. This is illustrated in Figure 14–6. Unfortunately, this technique is not noise immune, and suffers an additional disadvantage in that it must be operated at voltages above 9.5 V.

Figure 14–5. The Discrete Sense Circuit

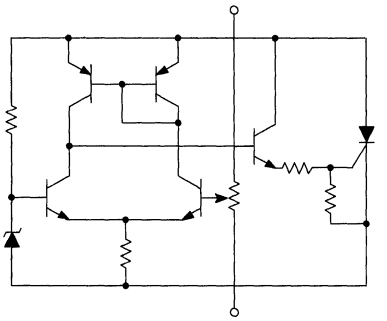
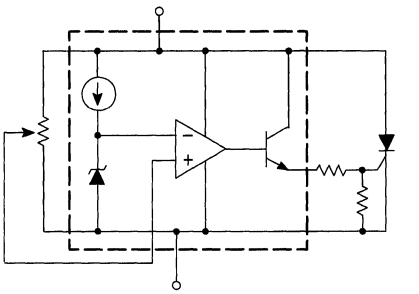


Figure 14–6. The "723" Sense Circuit



4. The MC3423 — To fill the need for a low cost, low complexity method of implementing crowbar overvoltage protection which does not suffer the disadvantages of previous techniques, an IC has been developed for use as an OVP sense and drive circuit, the MC3423.

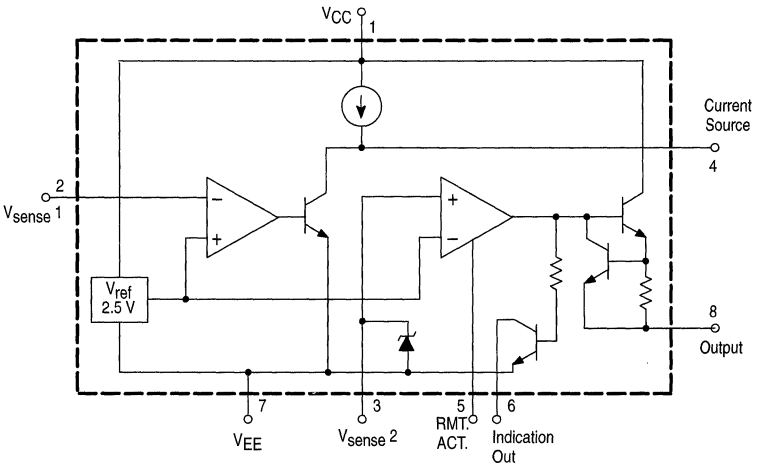
The MC3423 was designed to provide output currents of up to 300 mA with a 400 mA/μs rise time in order to maximize the di/dt capabilities of the crowbar SCR. In addition, its features include:

1. Operation off 4.5 V to 40 V supply voltages.
2. Adjustable low temperature coefficient trip point.
3. Adjustable minimum overvoltage duration before actuation to reduce nuisance tripping in noisy environments.
4. Remote activation input.
5. Indication output.

5. Block Diagram — The block diagram of the MC3423 is shown in Figure 14–7. It consists of a stable 2.6 V reference, two comparators and a high current output. This output, together with the indication output transistor, is activated either by a voltage greater than 2.6 V on Pin 3 or by a TTL/5.0 V CMOS high logic level on the remote activation input, Pin 5.

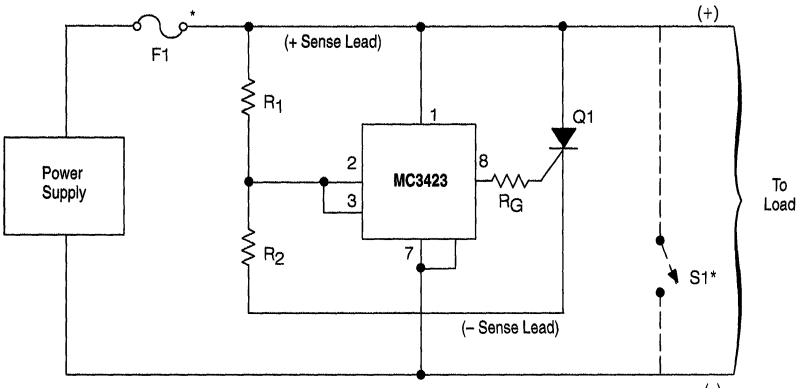
The circuit also has a comparator–controlled current source which can be used in conjunction with and external timing capacitor to set a minimum overvoltage duration (0.5 μs to 1.0 ms) before actuation occurs. This feature allows the OVP circuit to operate in noisy environments without nuisance tripping.

Figure 14–7. MC3423 Block Diagram



6. Basic Circuit Configuration — The basic circuit configuration of the MC3423 OVP is shown in Figure 14–8. In this circuit the voltage sensing inputs of both the internal amplifiers are tied together for sensing the overvoltage condition. The shortest possible propagation delay is thus obtained. The threshold or trip voltage at which the MC3423 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R_1 and R_2. Their values can be determined by the equations given in Figure 14–8 or by the graph shown in Figure 14–9. The switch (S1) shown in Figure 14–8 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current–limited supply is used a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

Figure 14–8. MC3423 Basic Circuit Configuration



$$V_{trip} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) \approx 2.6\ V\left(1 + \frac{R_1}{R_2}\right)$$

$R_2 \leq 10\ k\Omega$ for minimum drift

*Needed if supply is not current–limited

7. MC3423 Programmable Configuration — In many instances, MC3423 OVP will be used in a noisy environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 14–10 is used.

Here a capacitor is connected from Pin 3 and Pin 4 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition (t_D) which is necessary to trip the OVP. The value of C_D can be found from Figure 14–11. The circuit operates in the following manner: when V_{CC} rises above the trip point set by R_1 and R_2, the internal current source begins charging the capacitor, C_D, connected to Pins 3 and 4. If the overvoltage condition remains present long enough for the capacitor voltage, V_{CD} to reach V_{ref}, the output is activated. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

8. Indication Output — An additional output for use as an indicator of OVP activation is provided by the MC3423. This output (Pin 6) is an open–collector transistor which saturates when the MC3423 OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC}, below 4.5 V as in Figure 14–10. This output can be used to clock an edge triggered flip–flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

Figure 14–9. R_1 versus Trip Voltage for the MC3423 OVP

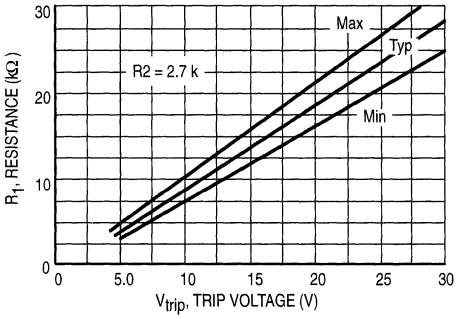
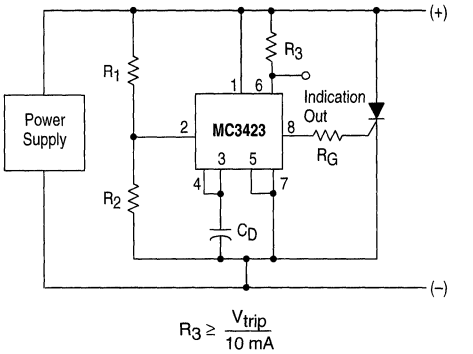


Figure 14–10. MC3423 Configuration for Programmable Minimum Duration of Overvoltage Condition Before Tripping



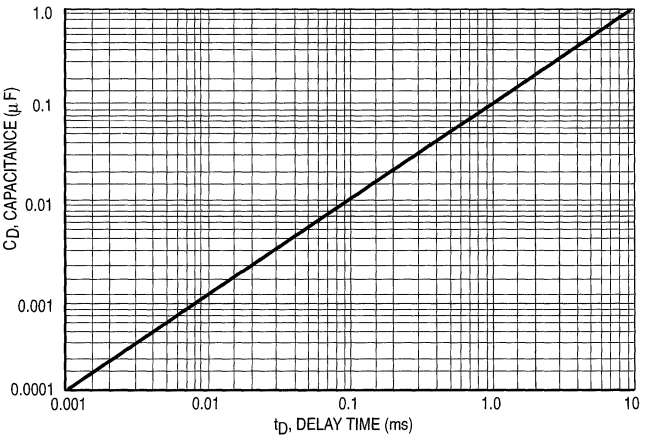
9. Remote Activation Input — Another feature of the MC3423 is its Remote Activation Input, Pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.7 V, the MC3423 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present.

This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the Indication Output of one MC3423 can be used to activate another MC3423, if a single transistor inverter is used to interface the former's Indication Output to the latter's Remote Activation Input.

D. MC3425 Power Supply Supervisory Circuit

In addition to the MC3423 a second IC, the MC3425 has been developed. Similar in many respects to the MC3423, the MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. The block diagram is shown below in Figure 14–12. The Overvoltage (OV) and Undervoltage (UV) Input Comparators are both referenced to an internal 2.5 V regulator. The UV Input Comparator has a feedback activated 12.5 μA current sink (I_H) which is used for programming the input hysteresis voltage (V_H). The source resistance feeding this input (R_H) determines the amount of hysteresis voltage by $V_H = I_H R_H = 12.5 \times 10^{-6} R_H$.

Figure 14–11. C_D versus Minimum Overvoltage Duration, t_D for The MC3423 OVP



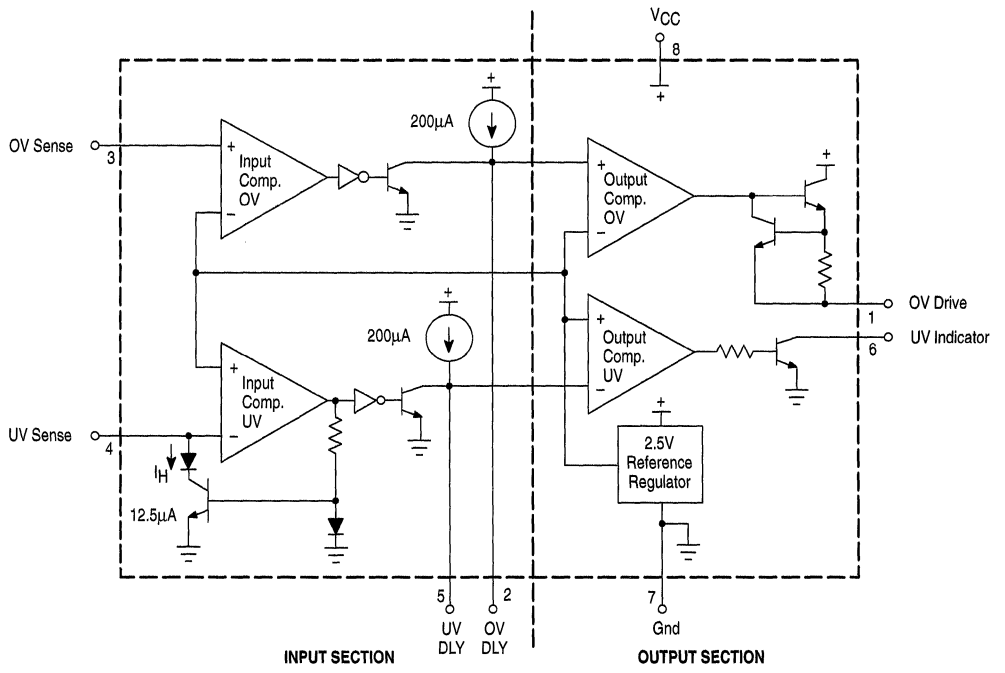
Separate Delay pins (OV DLY, UV DLY) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY(source)}$, of typically 200 μA when the noninverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time (t_{DLY}) for the Drive and Indicator outputs. The Delay pins are internally connected to the non–inverting inputs of the OV and UV Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time (t_{DLY}) is based on the constant current source, $I_{DLY(source)}$, charging the external delay capacitor (C_{DLY}) to 2.5 V.

$$t_{DLY} = \frac{V_{ref}\, C_{DLY}}{I_{DLY(source)}} = \frac{2.5\, C_{DLY}}{200\ \mu A} = 12500\, C_{DLY}$$

Figure 14–13 provides C_{DLY} values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's non–inverting input is less than the inverting input. The sink current $I_{DLY(sink)}$ capability of the Delay pins is ≥1.8 mA and is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

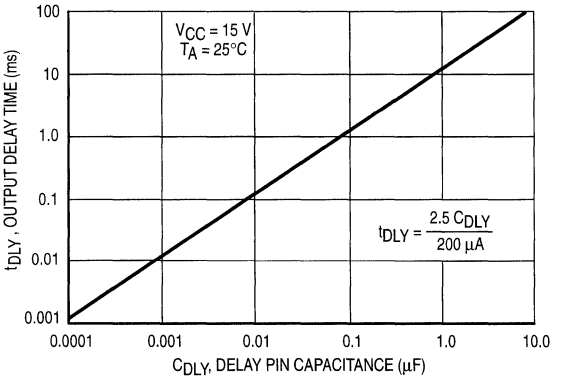
The Overvoltage Drive Output is a current–limited emitter–follower capable of sourcing 300 mA at a turn–on slew rate of 2.0 A/μs, ideal for driving crowbar SCRs. The Undervoltage Indicator Output is an open–collector NPN transistor, capable of sinking 30 mA to provide sufficient drive for LEDs, small relays or shutdown circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded. The MC3425 has an internal 2.5 V bandgap reference regulator with an accuracy of ± 4.0% for the basic devices.

Figure 14–12. Block Diagram



Note: All voltages and currents are nominal.

Figure 14–13. Output Delay Time versus Delay Capacitance

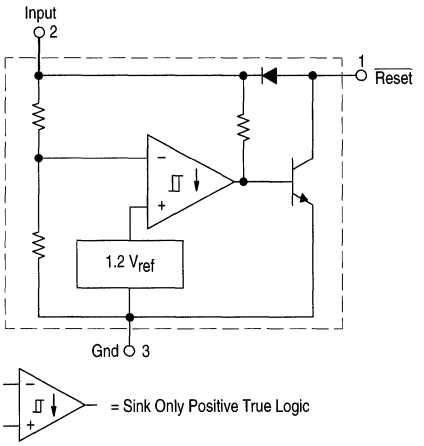


E. MC34064 and MC34164 Series

The MC34064 and MC34164 series are two families of undervoltage sensing circuits specifically designed for use as reset controllers in microprocessor–based systems. They offer the designer an economical solution for low voltage detection with a single external resistor. Both parts feature a trimmed bandgap reference, and a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation.

The two families of undervoltage sensing circuits, taken together, cover the needs of the most commonly specified power supplies used in MCU/MPU systems. Key parameter specifications of the MC34164 family were chosen to complement the MC34064 series. The table summarizes critical parameters of both families. The MC34064 fulfills the needs of a 5.0 V ± 5% system and features a tighter hysteresis specification. The MC34164 series covers 5.0 V ± 10% and 3.0 V ± 5% power supplies with significantly lower power consumption, making them ideal for applications where extended battery life is required such as consumer products or hand held equipment.

Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment. The MC34164 is specifically designed for battery powered applications where low bias current (1/25th of the MC34064's) is an important characteristic.



REFERENCES
1. *Characterizing the SCR for Crowbar Applications*, Al Pshaenich, Motorola AN789. **(Out of Print)**
2. *Semiconductor Considerations for DC Power Supply SCR Crowbar Circuits*, Henry Wurzburg, Third National Sold–State Power Conversion Conference, June 25, 1976.
3. *Is a Crowbar Enough?* Willis C. Pierce Jr., Hewlett–Packard, Electronic Design 20, Sept. 27, 1974.
4. *Transient Thermal Response — General Data and Its Use*, Bill Roehr and Brice Shiner, Motorola AN569. **(Out of Print)**

3

SECTION 15
HEATSINKING

A. The Thermal Equation

A necessary and primary requirement for the safe operation of any semiconductor device, whether it be an IC or a transistor, is that its junction temperature be kept below the specified maximum value given on its data sheet. The operating junction temperature is given by:

$$T_J = T_A + P_D \theta_{JA} \quad (15.1)$$

where: T_J = junction temperature (°C)
T_A = ambient air temperature (°C)
P_D = power dissipated by device (W)
θ_{JA} = thermal resistance from junction–to–ambient air (°C/W)

The junction–to–ambient thermal resistance (θ_{JA}) in Equation (15.1), can be expressed as a sum of thermal resistances as shown below:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad (15.2)$$

where: θ_{JC} = junction–to–case thermal resistance
θ_{CS} = case–to–heatsink thermal resistance
θ_{SA} = heatsink–to–ambient thermal resistance

Equation (15.2) applies only when an external heatsink is used. If no heatsink is used, θ_{JA} is equal to the device package θ_{JA} given on the data sheet.

θ_{JC} depends on the device and its package (case) type, while θ_{SA} is a property of the heatsink and θ_{CS} depends on the type of package/heatsink interface employed. Values for θ_{JC} and θ_{SA} are found on the device and heatsink data sheets, while θ_{CS} is given in Table 15–1.

Table 15–1. θ_{CS} For Various Packages & Mounting Arrangements

	θ_{CS}			
	Metal–to–Metal*		Using an Insulator*	
Case	Dry	With Heatsink Compound	With Heatsink Compound	Type
TO–204	0.5°C/W	0.1°C/W	0.36°C/W 0.28°C/W	3 mil MICA Anodized Aluminum
TO–220	1.2°C/W	1.0°C/W	1.6°C/W	2 mil MICA

*Typical values; heatsink surface should be free of oxidation, paint, and anodization

Examples showing the use of Equations (15.1) and (15.2) in thermal calculations are as follows:

Example 1: Find required heatsink θ_{SA} for an MC7805CT, given:

$$T_{J(max)} \text{ (desired)} = +125°C$$
$$T_{A(max)} = +70°C$$
$$P_D = 2.0 \text{ W}$$

Mounted directly to heatsink with silicon thermal grease at interface:

1. From MC7805CT data sheet, $\theta_{JC} = 5°C/W$
2. From Table 15–1. $\theta_{CS} = 1.6°C/W$
3. Using Equation (15.1) and (15.2), solve for θ_{SA}:

$$\theta_{SA} = \frac{(T_J - T_A)}{P_D} - \theta_{CS} - \theta_{JC}$$

$$\theta_{SA} = \frac{(125 - 70)}{2} - 5.0 - 1.6 \; (\leq 20.9°C/W \text{ required})$$

Example 2: Find the maximum allowable T_A for an unheatsinked MC78L15CT, given:

$$T_{J(max)} \text{ (desired)} = +125°C$$
$$P_D = 0.25 \text{ W}$$

1. From MC78L15CT data sheet, $\theta_{JA} = 200°C/W$
2. Using Equation (15.1), find T_A:

$$T_A = T_j - P_D \theta_{JA}$$
$$= 125 - 0.25 \; (200)$$
$$= +75°C$$

B. Selecting a Heatsink

Usually, the maximum ambient temperature, power being dissipated, the $T_{J(max)}$, and θ_{JC} for the device being used are known. The required θ_{SA} for the heatsink is then determined using Equations (15.1) and (15.2), as in Example 1. The designer may elect to use a commercially available heatsink, or if packaging or economy demands it, design his own.

1. Commercial Heatsinks

As an aid in selecting a heatsink, a representative listing is shown in Table 15–2. This listing is by no means complete and is only included to give the designer an idea of what is available.

Table 15–2. Commercial Heatsink Selection Guide

TO–204AA (TO–3)	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
0.3–1.0	Thermalloy — 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0–3.0	Wakefield — 641 Thermalloy — 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0–5.0	Wakefield — 621, 623 Thermalloy — 6606, 6129, 6141, 6303 IERC — HP Staver — V3–3–2
5.0–7.0	Wakefield — 690 Thermalloy — 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301 IERC — LB Staver — V3–5–2
7.0–10	Wakefield — 672 Thermalloy — 6001, 6016, 6051, 6105, 6601 IERC — LA µP Staver — V1–3, V1–5, V3–3, V3–5, V3–7
10–25	Thermalloy — 6013, 6014, 6015, 6103, 6104, 6105, 6117

*All values are typical as given by the manufacturer or as determined from characteristic curves supplied by the manufacturer.

Table 15–2. Commercial Heatsink Selection Guide (continued)

TO–204AA (TO–5)	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
12 to 20	Wakefield — 260 Thermalloy — 1101, 1103 Staver — V3A–5
20 to 30	Wakefield — 209 Thermalloy — 1116, 1121, 1123, 1130, 1131, 1132, 2227, 3005 IERC — LP Staver — F5–5
30 to 50	Wakefield — 207 Thermalloy — 2212, 2215, 225, 2228, 2259, 2263, 2264 Staver — F5–5, F6–5
	Wakefield — 204, 205, 208 Thermalloy — 1115, 1129, 2205, 2207, 2209, 2210, 2211, 2226, 2230, 2257, 2260, 2262 Staver — F1–5, F5–5

TO–204AB	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
5.0 to 10	IERC H P3 Series Staver — V3–7–225, V3–7–96
10 to 15	Thermalloy — 6030, 6032, 6034 Staver — V4–3–192, V–5–1
20 to 30	Wakefield — 295 Thermalloy — 6025, 6107
15 to 20	Thermalloy — 6106 Staver — V4–3–128, V6–2

TO–226AA (TO–92)	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
46	Staver F5–7A, F5–8
50	IERC AUR
57	Staver F5–7D
65	IERC RU
72	Staver F1–8, F2–7
80 to 90	Wakefield 292
85	Thermalloy 2224
DUAL–IN–LINE–PACKAGE ICs	
20	Thermalloy — 6007
30	Thermalloy — 6010
32	Thermalloy — 6011
34	Thermalloy — 6012
45	IERC — LIC
60	Wakefield — 650, 651

*All values are typical as given by the manufacturer or as determined from characteristic curves supplied by the manufacturer.

Staver Co., Inc.: 41–51 N. Saxon Ave., Bay Shore, NY 11706
IERC: 135 W. Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W. Valley View Ln. Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880

2. Custom Heatsink Design

Custom heatsinks are usually either forced air cooled or convection cooled. The design of forced air cooled heatsinks is usually done empirically, since it is difficult to obtain accurate air flow measurements. On the other hand, convection cooled heatsinks can be designed with fairly predictable characteristics. It must be emphasized, however, that any custom heatsink design should be thoroughly tested in the actual equipment configuration to be certain of its performance. In the following sections, a design procedure for convection cooled heatsinks is given.

Obviously, the basic goal of any heatsink design is to produce a heatsink with an adequately low thermal resistance, θ_{SA}. Therefore, a means of determining θ_{SA} is necessary in the design. Unfortunately, a precise calculation method for θ_{SA} is beyond the scope of this book.* However, a first order approximation can be calculated for a convection cooled heatsink if the following conditions are met:

1. The heatsink is a flat rectangular or circular plate whose thickness is smaller than its length or width.
2. The heatsink will not be located near other heat radiating surfaces.
3. The aspect ratio of a rectangular heatsink (length:width) is not greater than 2:1.
4. Unrestricted convective air flow.

For the above conditions, the heatsink thermal resistance can be approximated by:

$$\theta_{SA} \simeq \frac{1}{A\eta\,(Fchc + \epsilon Hr)}\ (°C/W) \qquad (15.3)$$

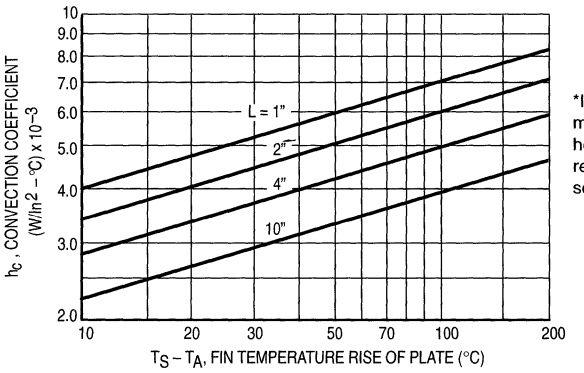
where: A = area of the heatsink surface
η = heatsink effectiveness
F_C = convective correction factor
h_C = convection heat transfer coefficient
ϵ = emissivity
H_r = normalized radiation heat transfer coefficient

The convective heat transfer coefficient, h_C, can be found from Figure 15–1. Note that it is a function of the heatsink fin temperature rise ($T_S - T_A$) and the heatsink significant dimension (L). The fin temperature rise ($T_S - T_A$) is given by:

$$T_S - T_A = \theta_{SA}\, P_D \qquad (15.4)$$

where: T_S = heatsink temperature
T_A = ambient temperature
θ_{SA} = heatsink–to–ambient thermal resistance
P_D = power dissipated

Figure 15–1. Convection Coefficient (h_C)



*If greater precision is desired, or more information on heat flow and heatsinking is sought, consult the references list at the end of this section.

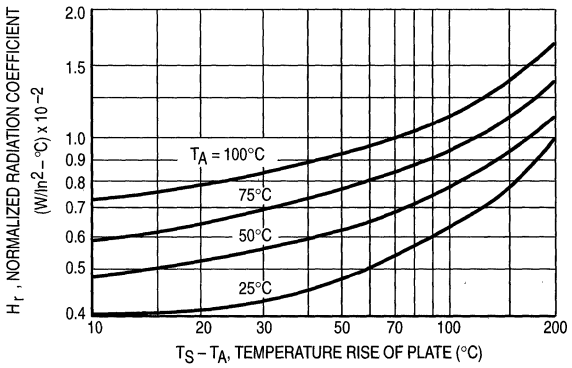
The significant heatsink dimension (L) is dependent on the heatsink shape and mounting place and is given in Table 15–3. The convective correction factor (F_C) is likewise dependent on shape and mounting plane of the heatsink and is also given in Table 15–3.

Table 15–3. Significant Dimension (L) and Correction Factor (F_C) for Convection Thermal Resistance

Surface	Significant Dimension L		Correction Factor F_C	
	Position	L	Position	F_C
Rectangular Plane	Vertical	Height (max 2 ft)	Vertical Plane	1.0
	Horizontal	$\frac{\text{length} \times \text{width}}{\text{length} + \text{width}}$	Horizontal Plane both surfaces exposed	1.35
Circular Plane	Vertical	$\pi / 1 \times$ diameter	Top only exposed	0.9

The normalized radiation heat transfer coefficient (H_r) is dependent on the ambient temperature (T_A) and the heatsink temperature rise ($T_S - T_A$) given by Equation (15.4). H_r can be determined from Figure 15–2.

Figure 15–2. Normalized Radiation Coefficient (H_r)



The emissivity (ϵ) can be found in Table 15–4 for various heatsink surfaces.

Table 15–4. Typical Emissivities of Common Surfaces

Surface	Emissivity (ϵ)
Alodine on Aluminum	0.15
Aluminum, Anodized	0.7 to 0.9
Aluminum, Polished	0.05
Copper, Polished	0.07
Copper, Oxidized	0.70
Rolled Sheet Steel	0.66
Air Drying Enamel (any color)	0.85 to 0.91
Oil Paints (any color)	0.92 to 0.96
Varnish	0.89 to 0.93

Finally, the heatsink efficient (η) can be found from the nomograph of Figure 15–3. Use of the nomograph is as follows:

a) Find $h_T = Fchc + \in H_r$ from Figures 15–1, 15–2 and Tables 15–3 and 15–4, and locate this point on the nomograph.

b) Draw a line from h_T through chosen heatsink fin thickness (x) to find α.

c) Determine D for the heatsink shape as given in Figure 15–4 and draw a line from this point through α, which was found in (b), to determine η.

d) If power dissipating element is not located at heatsink's center of symmetry, multiply η by 0.7 (for vertically mounted plates only).

Note that in order to calculate θ_{SA} from Equation (15.3), it is necessary to know the heatsink size. Therefore, in order to arrive at a suitable heatsink design, a trial size is selected, its θ_{SA} evaluated, and the original size reduced or enlarged as necessary. This process is iterated until the smallest heatsink is obtained that has the required θ_{SA}. The following design example is given to illustrate this procedure.

Figure 15–3. Fin Effectiveness Nomogram for Symmetrical Flat, Uniformly Thick Fins

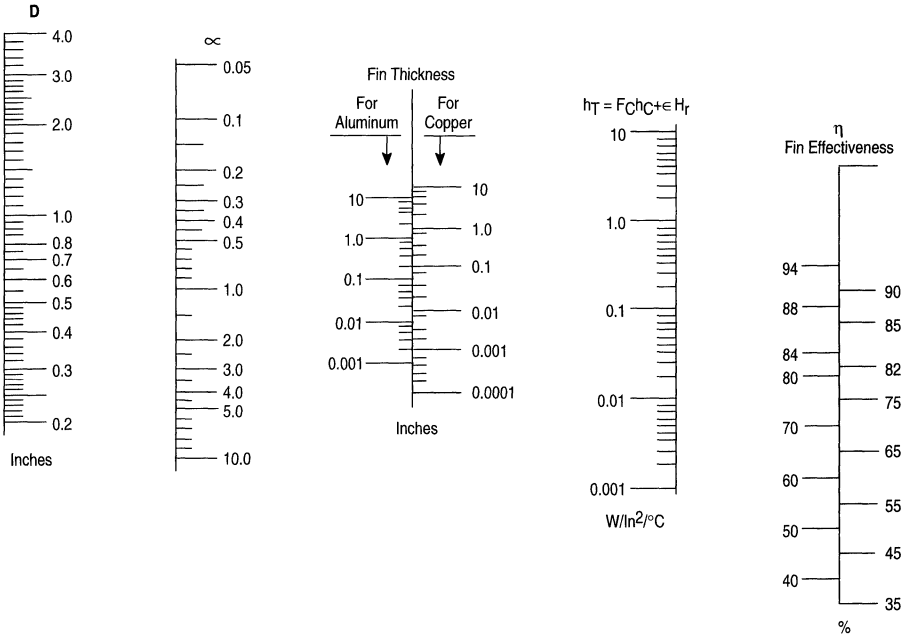


Figure 15–4. Determination of D for Use in η Nomograph of Figure 15–3

$D \cong \sqrt{\frac{ab}{\pi}}$, if $a,b \gg S$ & $b \leq 2a$

$D \simeq \frac{d}{2}$, if $d \gg s$

Heatsink Design Example

Design a flat rectangular heatsink for use with a horizontally mounted power device on a PC board, given the following:

1. Heatsink $\theta_{SA} = 25°C/W$
2. Power to be dissipated, $P_D = 2.0$ W
3. Maximum ambient temperature, $T_A = 50°C$
4. Heatsink to be constructed from 1/8″ (0.125″) thick anodized aluminum.

a) First, a trial heatsink is chosen: 2″ × 3″ (experience will simplify this selection and reduce the number of necessary iterations.)

b) The factors in Equation (15.3) are evaluated by using the Figures and Tables given:

$A = 2'' \times 3'' = 6$ sq. in.

$L = 6/5'' = 1.2$ in. (from Table 15–3)

$T_S - T_A = 50°C$ (from Figure 15–4)

$h_C = 5.8 \times 10^{-3}$ W/in^2 – °C (from Figure 15–1)

$F_C = 0.9$ (from Table 15–3)

$H_r = 6.1 \times 10^{-3}$ W/in^2 – °C (from Figure 15–2)

$\epsilon = 0.9$ (from Table 15–4)

$h_T = Fchc + H_{r\epsilon} = 10.7 \times 10^{-3}$ W/in^2 – °C

$\alpha = 0.13$ (from Figure 15–3)

$D = 1.77$ (from Figure 15–4)

$\eta > 0.94 \simeq 1$ (from Figure 15–3)

c) Using Equation (15.3), find θ_{SA}:

$$\theta_{SA} \simeq \frac{1}{A\eta\,(Fchc + \epsilon H_r)} = 16.66°C/W < 25°C/W$$

d) Since 2″ × 3″ is too large, try 2″ × 2″. Following the same procedure, θ_{SA} is found to be 25°C/W, which exactly meets the design requirements.

SOIC MINIATURE IC PLASTIC PACKAGE

Thermal Information

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(typ)}$$

where: $P_{D(T_A)}$ = power dissipation allowable at a given operating ambient temperature,

$T_{J(max)}$ = maximum operating junction temperature as listed in the maximum ratings section,

T_A = desired operating ambient temperature,

$R_{\theta JA}$ (typ) = typical thermal resistance junction–to–ambient.

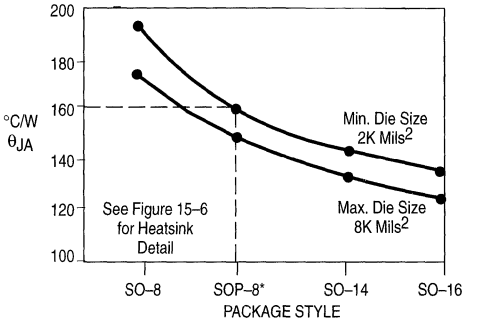
Maximum Ratings

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70 – 40 to +85	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

THERMAL CHARACTERISTICS OF SOIC PACKAGES

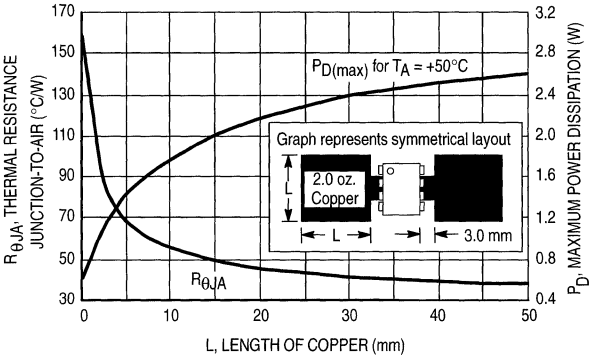
Measurement specimens are solder mounted on a Philips SO test board #7322–078, 80873 in still air. No auxiliary thermal conduction aids are used. As thermal resistance varies inversely with die area, a given package takes thermal resistance values between the max and min curves shown. These curves represent the smallest (2000 square mils) and largest (8000 square mils) die areas expected to be assembled in the SOIC package.

Figure 15–5. Thermal Resistance, Junction–to–Ambient (°C/W)



Data taken using Philips SO test board #7322–078, 80873
*SOP–8 using standard SO–8 footprint — minimum pad size

Figure 15–6. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



SOP–8 and SOP–16L Packaged Devices

Several families of voltage regulators and power control ICs have been introduced in surface mounted packages which were developed by the Analog IC Division. The SOP–8 and SOP–16L packages have external dimensions which are identical to the standard SO–8 and SO–16L surface mount devices, but the center four leads of the packages are all connected to the leadframe die flag. This internal modification decreases the package thermal resistance and therefore increases its power dissipation capability. This advantage is fully realized when the package is mounted on a printed circuit board with a single pad for the four center leads. This large area of copper then acts as an external heat spreader, efficiently conducting heat away from the package.

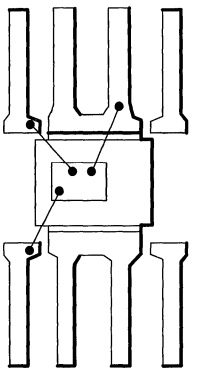
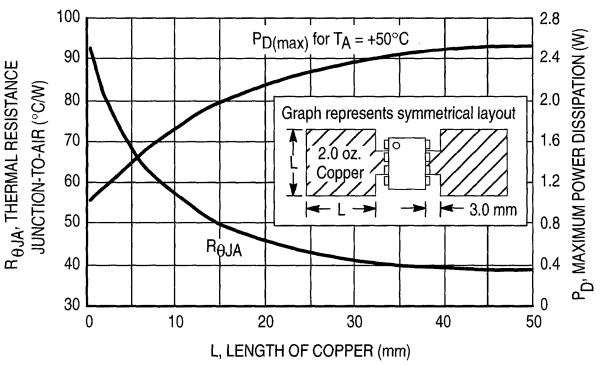


Figure 15–7. SOP–16L Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

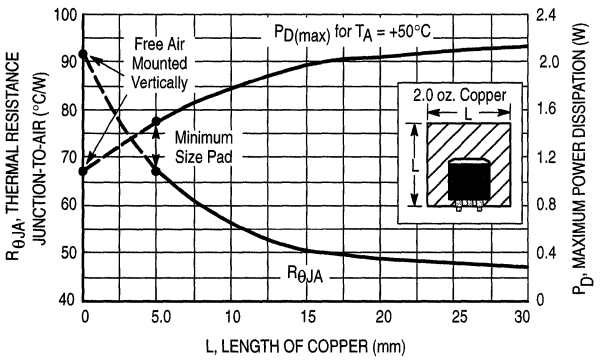


THERMAL CHARACTERISTICS OF DPAK AND D²PAK PACKAGE

The evaluation was performed using an active device (4900 square mils) mounted on 2.0 ounce copper foil epoxied to a GIO type printed circuit board. Measurements were made in still air and no auxiliary thermal conduction aids were used. The size of a square copper pad was varied, and all measurements were made with the unit mounted as shown in Figure 15–8. The curve shown in Figure 15–8 is a plot of junction–to–air thermal resistance versus the length of the square copper pad in millimeters. This shows that when the DPAK is mounted on a 10 mm × 10 mm square pad of 2.0 ounce copper it has a thermal resistance which is comparable to a TO–220 device mounted vertically without additional heatsinking.

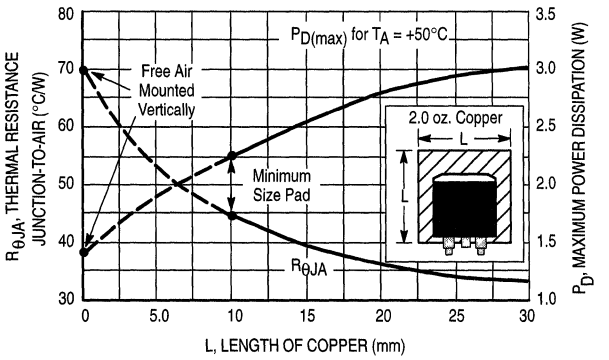
3

Figure 15–8. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



The thermal characteristics of the D²PAK are shown in Figure 15–9. The device was mounted on 2.0 oz. copper on an FR4–type P.C. board. The maximum power dissipation was measured with a junction temperature of 150°C.

Figure 15–9. 3–Pin and 5–Pin D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



Power/Motor Control Circuits

In Brief . . .

With the expansion of electronics into more and more mechanical systems, there comes an increasing demand for simple but intelligent circuits that can blend these two technologies. In the past, the task of power/motor control was once accomplished with discrete devices. But today this task is being performed by bipolar IC technology due to cost, size, and reliability constraints. Motorola offers integrated circuits designed to anticipate the requirements for both simple and sophisticated control systems, while providing cost effective solutions to meet the needs of the applications.

Power Controllers

An assortment of battery and ac line–operated control ICs for specific applications are shown. They are designed to enhance system performance and reduce complexity in a wide variety of control applications.

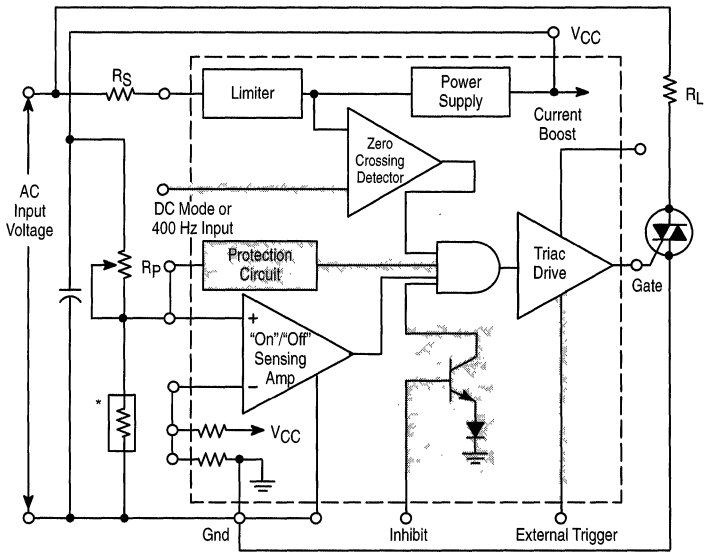
Zero Voltage Switch

CA3059

T_A = –40° to +85°C, Case 646

This device is designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 227 V @ 50/60 Hz.

- **Limiter–Power Supply** – Allows operation directly from an ac line.
- **Differential "On"/"Off" Sensing Amplifier** – Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented.
- **Zero–Crossing Detector** – Synchronizes the output pulses to the zero voltage point of the ac cycle. Eliminates RFI when used with resistive loads.
- **Triac Drive** – Supplies high current pulses to the external power controlling thyristor.
- **Protection Circuit** (CA3059 only) – A built–in circuit may be actuated, if the sensor opens or shorts, to remove the drive circuit from the external triac.
- **Inhibit Capability** (CA3059 only) – Thyristor firing may be inhibited by the action of an internal diode gate.
- **High Power DC Comparator Operation** (CA3059 only) – Operation in this mode is accomplished by connecting Pin 7 to 12 (thus overriding the action of the zero–crossing detector).



*NTC Sensor
NOTE: Shaded Area Not Included with CA3079.

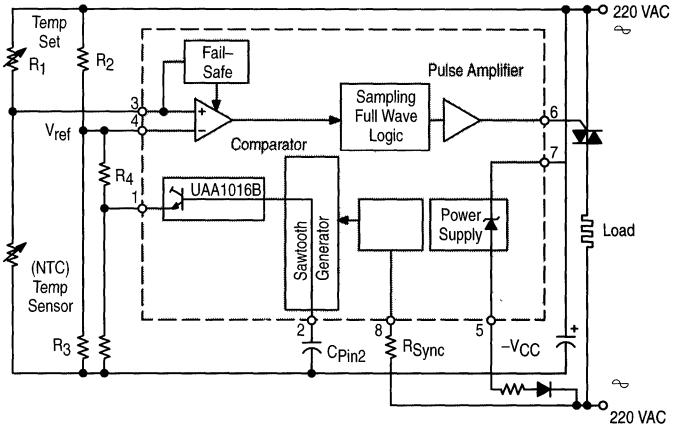
Zero Voltage Controller

UAA1016B

T_A = –20° to +100°C, Case 626

The UAA1016B is designed to drive triacs with the Zero voltage technique which allows RFI free power regulation of resistive loads. It provides the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- No DC Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triac Quadrants 2 and 3)
- Direct AC Line Operation
- Low External Components Count



Zero Voltage Controller

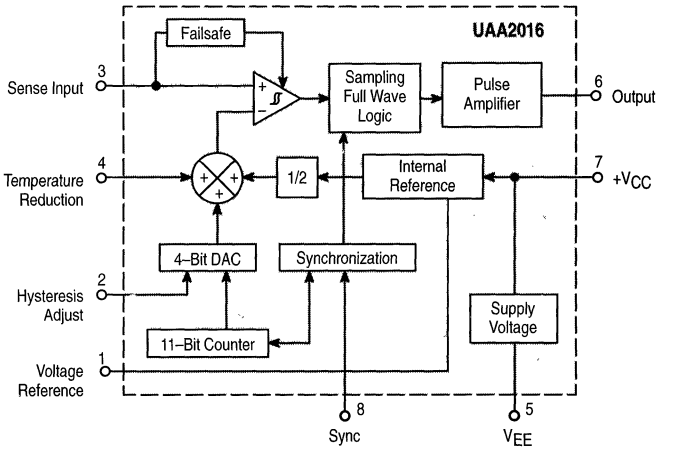
UAA2016P, D

T_A = –20° to +85°C, Case 626, 751

The UAA2016 is designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. Operating directly on the ac power line, its main application is the precision regulation of electrical heating systems such as panel heaters or irons.

A built–in digital sawtooth waveform permits proportional temperature regulation action over a ±1°C band around the set point. For energy savings there is a programmable temperature reduction function, and for security, a sensor failsafe inhibits output pulses when the sensor connection is broken. Preset temperature (i.e., defrost) application is also possible. In applications where high hysteresis is needed, its value can be adjusted up to 5°C around the set point. All these features are implemented with a very low external component count.

- Zero Voltage Switch for Triacs, up to 2.0 kW (MAC212A8)
- Direct AC Line Operation
- Proportional Regulation of Temperature over a 1°C Band
- Programmable Temperature Reduction
- Preset Temperature (i.e., Defrost)
- Sensor Failsafe
- Adjustable Hysteresis
- Low External Component Count



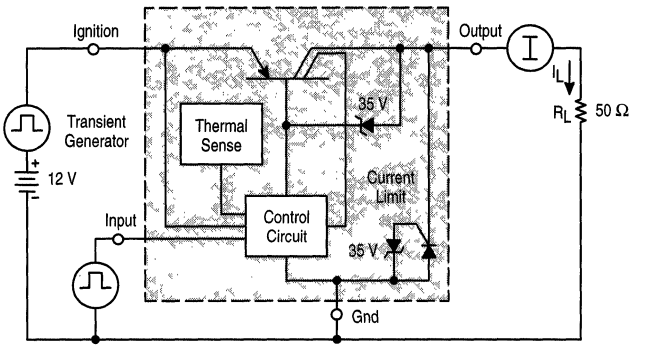
High–Side Driver Switch

MC3399T, DW

T_J = –40° to +150°C, Case 314D, 751G

The MC3399T is a high side driver switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the "on" state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive or negative–going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

The MC3399T is fabricated on a Power BiMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.



Motor Controllers

This section contains integrated circuits designed for cost effective control of specific motor families. Included are controllers for brushless, dc servo, stepper, and universal type motors.

Brushless DC Motor Controllers

Advances in magnetic materials technology and integrated circuits have contributed to the unprecedented rise in popularity of brushless dc motors. Analog control ICs are making the many features and advantages of brushless motors available at a much more economical price. Motorola offers a family of monolithic integrated brushless dc motor controllers. These ICs provide a choice of control functions which allow many system features to be easily implemented at a fraction of the cost of discrete solutions. The following table summarizes and compares the features of Motorola's brushless motor controllers.

1Features Summary for Motorola Brushless DC Motor Controllers

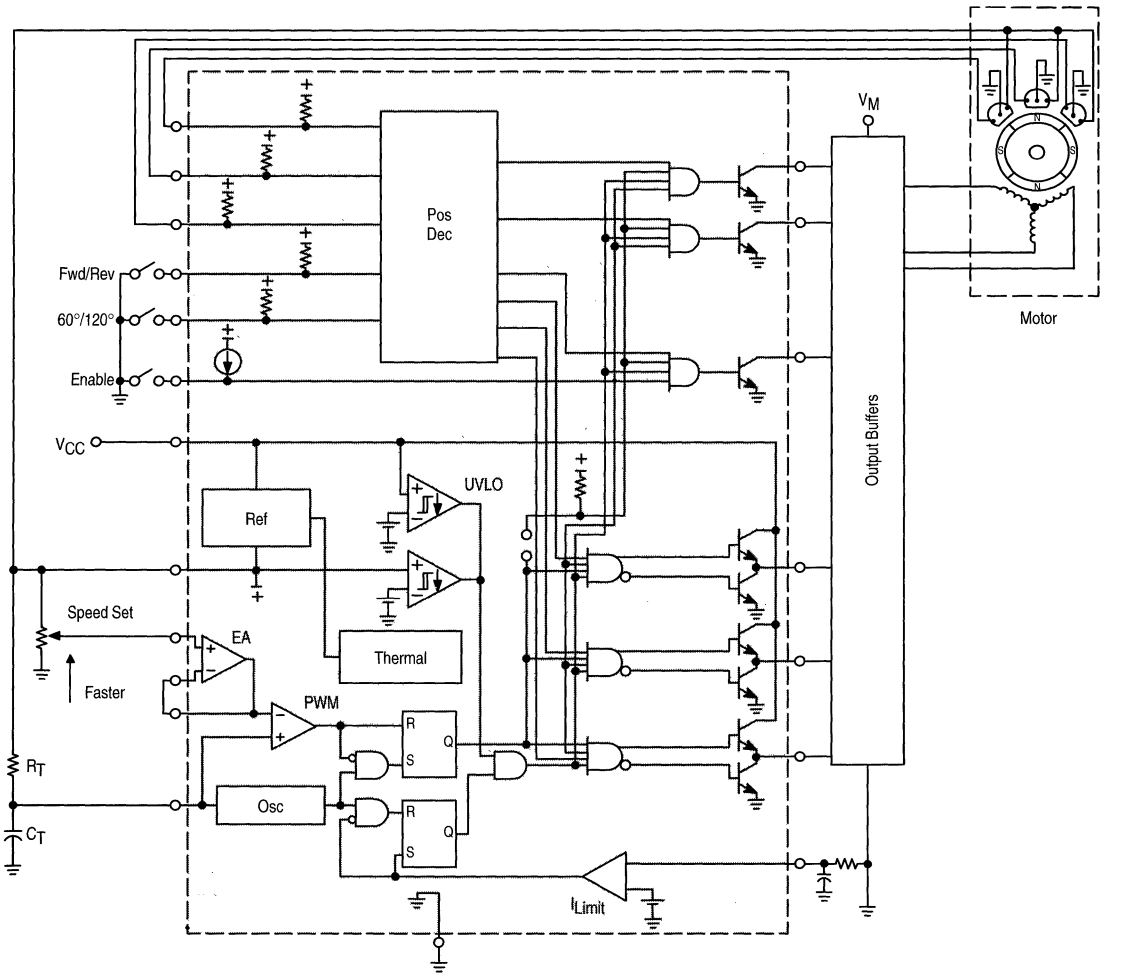
Device	Operating Voltage Range (V)		Undervoltage Lockout	Internal Thermal Shutdown	Fwd/Rev Control	Sensor Electrical Phasing	Output Enable	Output Drivers		6.25 V Reference Output	Current Sense Comparator Input(s)	Error Amplifier	$\overline{\text{FAULT}}$ Output	Separate Drive V_C	Brake Input	Suffix/ Package
	V_{CC}	V_C						Totem Pole (Bottom)	Open Collector (Top)							
MC33033	10–30	–	✓	✓	✓	60°/300° and 120°/240°	✓	✓	✓	✓	Noninv. Only	✓	–	–	–	P/738, DW/751D
MC33035	10–40	10–30	✓	✓	✓		✓	✓	✓	✓	Noninv. and Inv.	✓	✓	✓	✓	P/724, DW/751E

MC33033P, DW

T_A = −40° to +85°C, Case 738, 751D

The MC33033 is a lower cost second generation brushless dc motor controller which has evolved from the full featured MC33034 and MC33035 controllers. The MC33033 contains all of the active functions needed to implement a low cost open loop motor control system. This IC has all of the key control and protection functions of the two full featured devices with the following secondary features deleted: separate drive–circuit supply and ground pins, the brake input, and the fault output signal. Like its MC33035 predecessor, the MC33033 has a control pin which allows the user to select 60°/300° or 120°/240° sensor electrical phasings.

Because of its low cost, the MC33033 can efficiently be used to control brush dc motors as well as brushless. A brush dc motor can be driven using two of the three drive output phases provided in the MC33033, while the Hall sensor input pins are selectively tied to V_{ref} or ground. Other features such as forward/reverse, output enable, speed control, current limiting, undervoltage lockout and internal thermal shutdown will still remain functional.

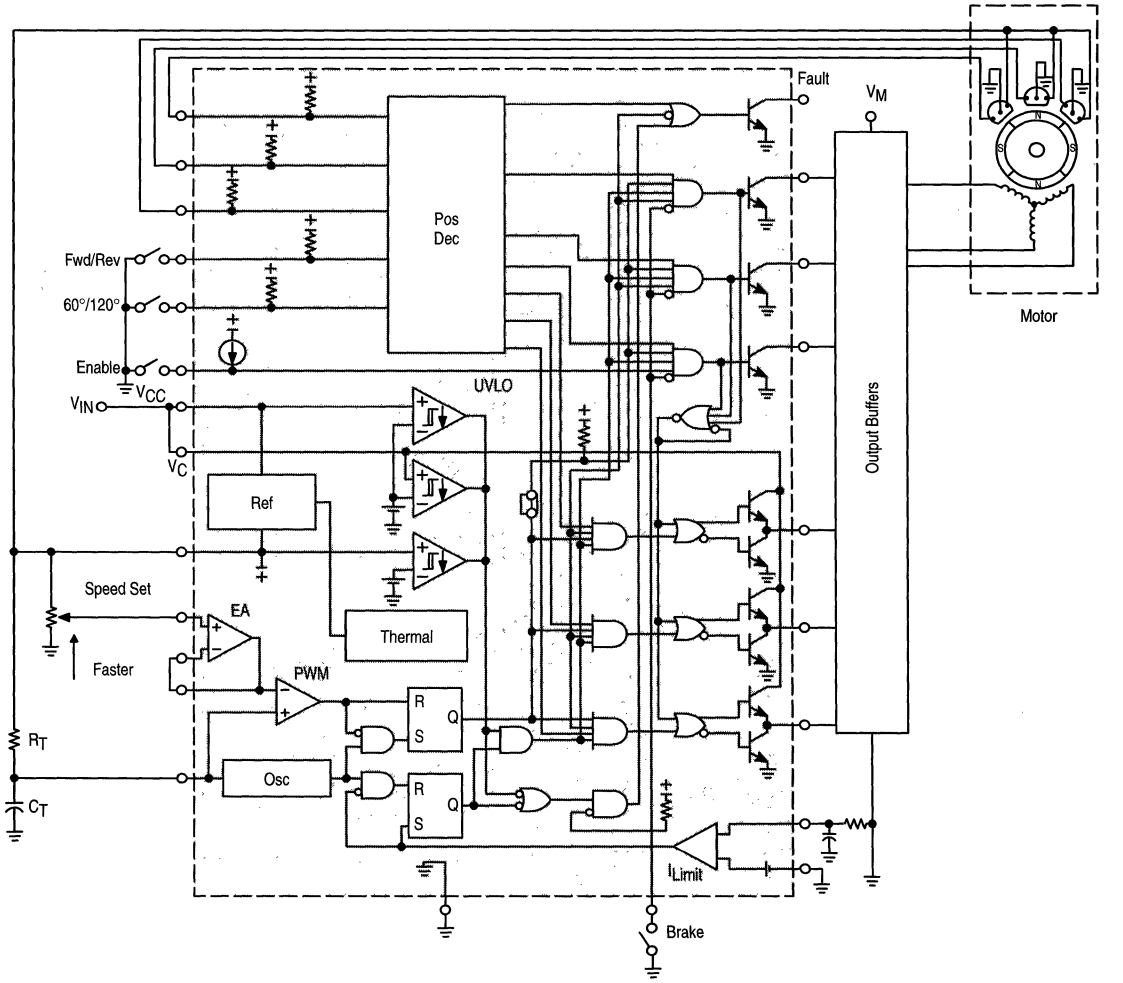


4

MC33035P, DW

T_A = –40° to +85°C, Case 724, 751E

The MC33035 is a second generation high performance brushless dc motor controller which contains all of the active functions required to implement a full featured open loop motor control system. While being pin–compatible with its MC33034 predecessor, the MC33035 offers additional features at a lower price. The two additional features provided by the MC33035 are a pin which allows the user to select 60°/300° or 120°/240° sensor electrical phasings, and access to both inverting and noninverting inputs of the current sense comparator. The earlier devices had two part numbers which were needed to support the different sensor phasings, and the inverting input to the current sense comparator was internally grounded. All of the control and protection features of the MC33034 are also provided in the MC33035.

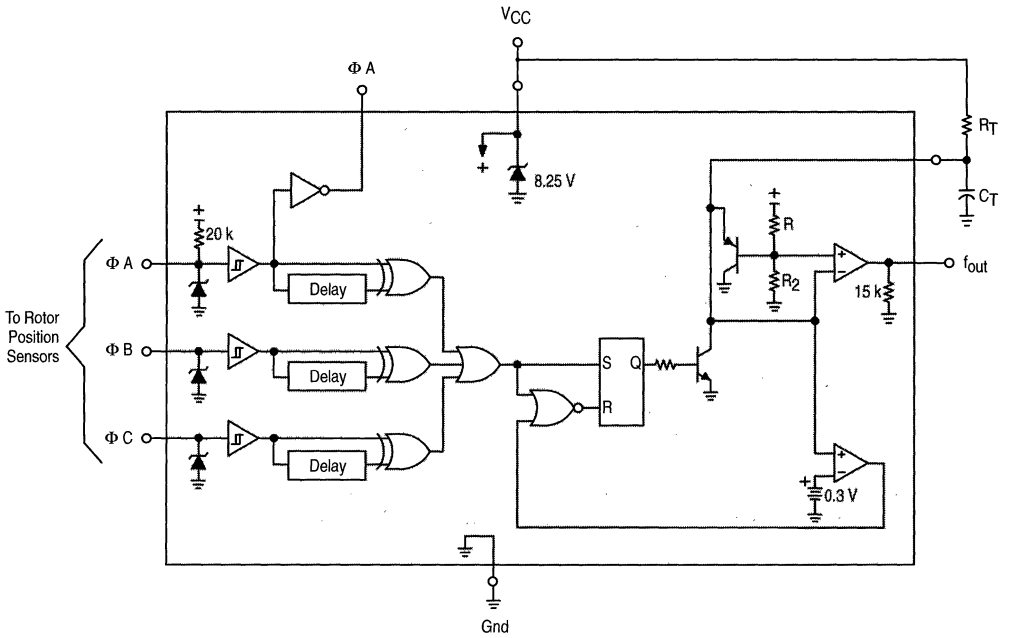


Closed Loop Brushless Motor Adapter

MC33039P, D

T_A = –40° to +85°C, Case 626, 751

The MC33039 is a high performance close loop speed control adapter specifically designed for use in brushless dc motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. These devices contain three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33033/35 brushless motor controllers, it can be used cost effectively in many other closed loop speed control applications.

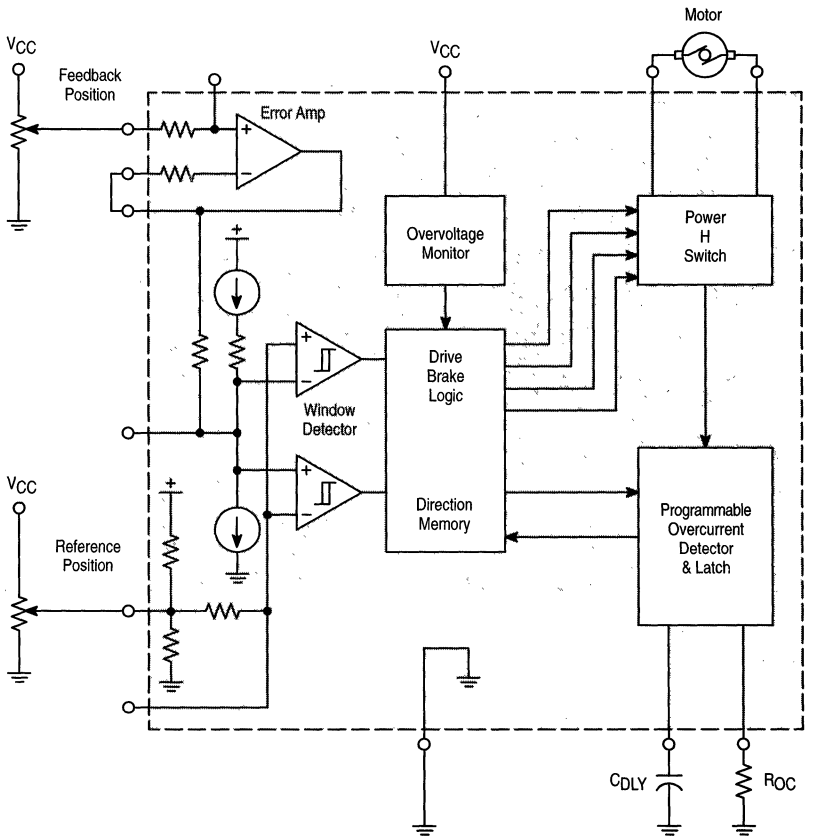


DC Servo Motor Controller/Driver

MC33030P, DW

T_A = –40° to +85°C, Case 648C, 751G

A monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on–chip op amp and window comparator with wide input common mode range, drive and brake logic with direction memory, a power H switch driver capable of 1.0 A, independently programmable over current monitor and shutdown delay, and over voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.



Stepper Motor Driver

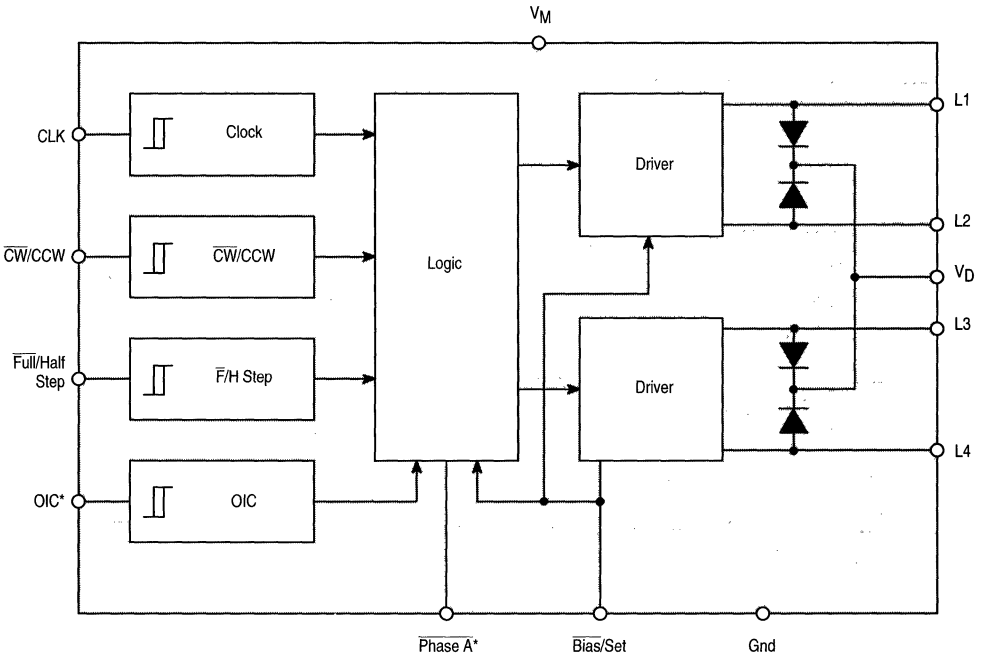
MC3479P, FN

T_A = 0° to +70°C, Case 648C, 775

SAA1042V

T_A = –30° to +125°C, Case 648C

These Stepper Motor Drivers provide up to 500 mA of drive per coil for two phase 6.0 V to 24 V stepper motors. Control logic is provided to accept commands for clockwise, counter clockwise and half or full step operation. The MC3479 has an added Output Impedance Control (OIC) and a $\overline{\text{Phase A}}$ drive state indicator (not available on SAA1042 devices).



* MC3479 Only

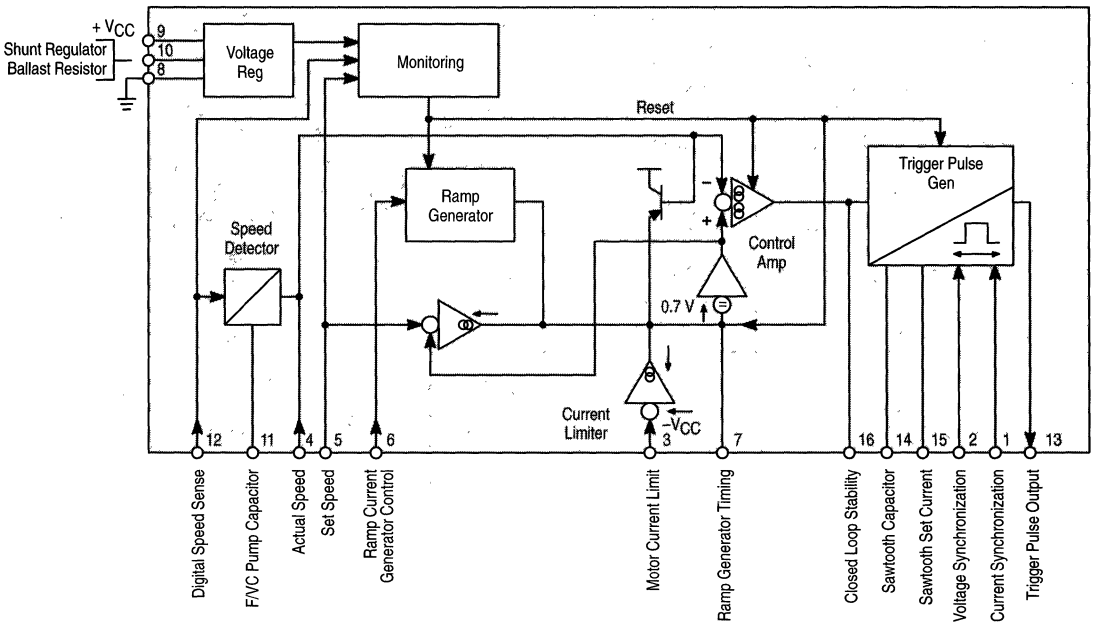
Universal Motor Speed Controller

TDA1085C, CD

T_A = –10° to +120°C, Case 648, 751B

The TDA1085C is a phase angle triac controller having all the necessary functions for universal motor speed control in washing machines. It operates in closed loop configuration and provides two ramp possibilities.

- On-Chip Frequency to Voltage Converter
- On-Chip Ramps Generator
- Soft Start
- Load Current Limitation
- Tachogenerator Circuit Sensing
- Direct Supply from AC Line
- Security Functions Peformed by Monitor



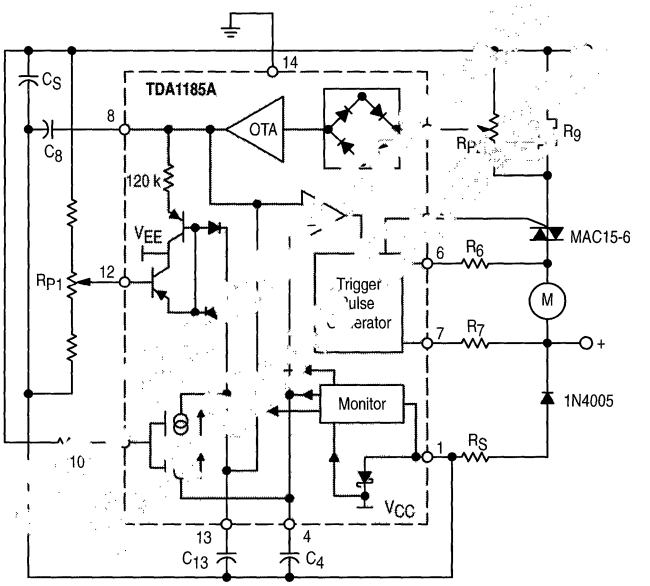
Triac Phase Angle Controller

TDA1185A

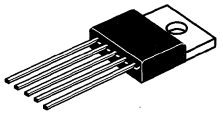
T_A = 0° to +70°C, Case 646

This device generates controlled triac triggering pulses and allows tachless speed stabilization of universal motors by an integrated positive feedback function.

- Low Cost External Components Count
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses when Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensed to Allow Inductive Loads
- Soft–Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 1.0 mA

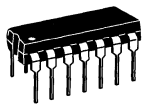


Power/Motor Control Circuits Package Overview

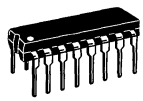


CASE 314D
T SUFFIX

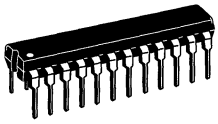
CASE 626
B, P SUFFIX



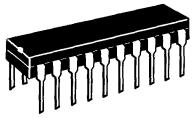
CASE 646



CASE 648, 648C
P, V SUFFIX



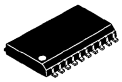
CASE 724
P SUFFIX



CASE 738
P SUFFIX

CASE 751
D SUFFIX

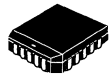
CASE 751B
D SUFFIX



CASE 751D
DW SUFFIX

CASE 751E
DW SUFFIX

CASE 751G
DW SUFFIX



CASE 775
FN SUFFIX

Device Listing

Power Controller

4

Motor Controllers

NOTE: * Not recommended for new designs.

MOTOROLA

CA3059

Zero Voltage Switch

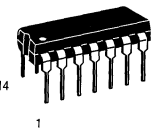
This series is designed for thyristor control in a variety of AC power switching applications for AC input voltages of 24 V, 120 V, 208/230 V, and 277 V @ 50/60 Hz.

Applications:

- Relay Control
- Heater Control
- Valve Control
- Lamp Control
- On–Off Motor Switching
- Differential Comparator with Self–Contained Power Supply for Industrial Applications
- Synchronous Switching of Flashing Lights

ZERO VOLTAGE SWITCH

SEMICONDUCTOR TECHNICAL DATA

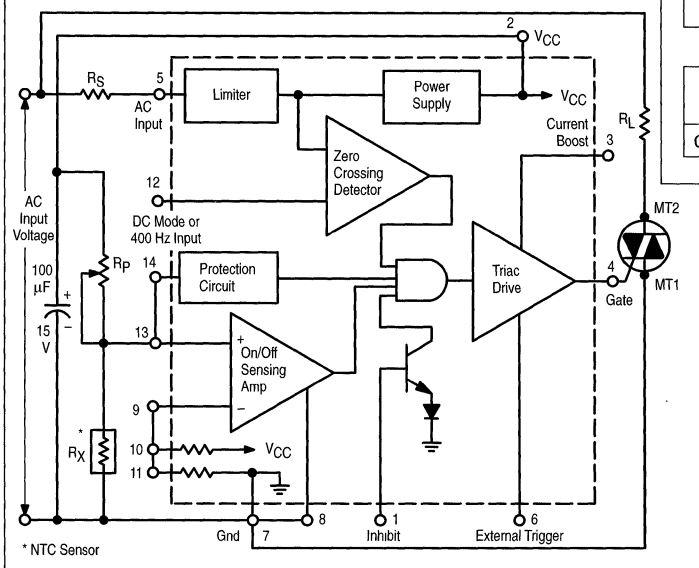


PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

Device	Operating Temperature Range	Package
CA3059	T_A = – 40° to +85°C	Plastic DIP

Figure 1. Representative Block Diagram



AC Input Voltage (50/60 Hz) Vac	Input Series Resistor (R_S) kΩ	Dissipation Rating for R_S W
24	2.0	0.5
120	10	2.0
208/230	20	4.0
277	25	5.0

FUNCTIONAL BLOCK DESCRIPTION

1. **Limiter–Power Supply** — Allows operation of the CA3059 directly from an AC line. Suggested dropping resistor (R_S) values are given in the table below.
2. **Differential On/Off Sensing Amplifier** — Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented using this block.
3. **Zero–Crossing Detector** — Synchronizes the output pulses to the zero voltage point of the AC cycle. This synchronization eliminates RFI when used with resistive loads.
4. **Triac Drive** — Supplies high–current pulses to the external power controlling thyristor.
5. **Protection Circuit** — A built–in circuit may be actuated, if the sensor opens or shorts, to remove the drive current from the external triac.
6. **Inhibit Capability** — Thyristor firing may be inhibited by the action of an internal diode gate at Pin 1.
7. **High Power DC Comparator Operation** — Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero–crossing detector). When Pin 13 is positive with respect to Pin 9, current to the thyristor is continuous.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage (Between Pins 2 and 7)	V_{CC}	12	Vdc
DC Supply Voltage (Between Pins 2 and 8)	V_{CC}	12	Vdc
Peak Supply Current (Pins 5 and 7)	$I_{5,7}$	± 50	mA
Fail–Safe Input Current (Pin 14)	I_{14}	2.0	mA
Output Pulse Current (Pin 4) (Note 1)	I_{out}	150	mA
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (Operation @ 120 Vrms, 50–60 Hz, T_A = 25°C [Note 2])

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	2	V_S				Vdc
Inhibit Mode						
R_S = 10 k, I_L = 0			6.1	6.5	7.0	
R_S = 5.0 k, I_L = 2.0 mA			—	6.1	—	
Pulse Mode						
R_S = 10 k, I_L = 0			6.0	6.4	7.0	
R_S = 5.0 k, R_L = 2.0 mA			—	6.2	—	
Gate Trigger Current (V_{GT} = 1.0 V, Pins 3 and 2 connected)	3	I_{GT}	—	160	—	mA
Peak Output Current, Pulsed	3	I_{OM}				mA
With Internal Power Supply, V_{GT} = 0						
Pin 3 Open			50	125	—	
Pins 3 and 2 Connected			90	190	—	
With External Power Supply, V_{CC} = 12 V, V_{GT} = 0	4					
Pin 3 Open			—	230	—	
Pins 3 and 2 Connected			—	300	—	
Inhibit Input Ratio (Ratio of Voltage @ Pin 9 to Pin 2)	5	V_9/V_2	0.465	0.485	0.520	—
Total Gate Pulse Duration (C_{Ext} = 0)	6					µs
Positive dv/dt		t_p	70	100	140	
Negative dv/dt		t_n	70	100	140	
Pulse Duration After Zero Crossing (C_{Ext} = 0, R_{Ext} = ∞)	6					µs
Positive dv/dt		t_{p1}	—	50	—	
Negative dv/dt		t_{n1}	—	60	—	
Output Leakage Current Inhibit Mode (Note 3)	3	I_4	—	0.001	10	µA
Input Bias Current	7	I_{IB}	—	0.15	1.0	µA
Common Mode Input Voltage Range (Pins 9 and 13 Connected)	—	V_{CMR}	—	1.4 to 5.0	—	Vdc
Inhibit Input Voltage	8	V_1	—	1.4	1.6	Vdc
External Trigger Voltage	—	V_6–V_4	—	1.4	—	Vdc

NOTES: 1. Care must be taken, especially when using an external power supply, that total package dissipation is not exceeded.
2. The values given in the Electrical Characteristics Table at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration test. However, the series resistor (R_S) must have the indicated value, shown in Table A for the specified input voltage.
3. I_4 out of Pin 4, 2.0 V on Pin 1, S_1 position 2.

TEST CIRCUITS

(All resistor values are in ohms)

4

Figure 2. DC Supply Voltage

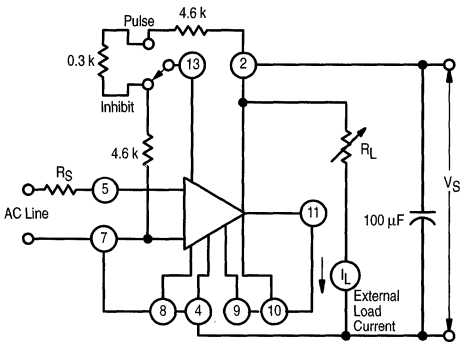


Figure 3. Peak Output (Pulsed) and Gate Trigger Current with Internal Power Supply

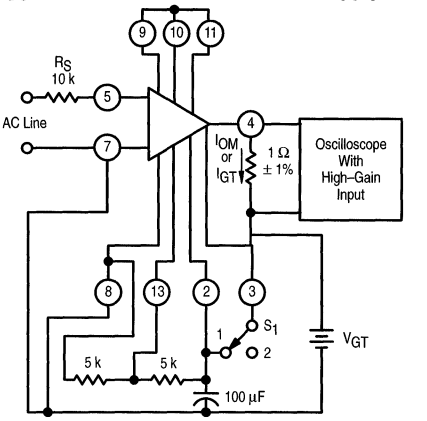


Figure 4. Peak Output Current (Pulsed) with External Power Supply

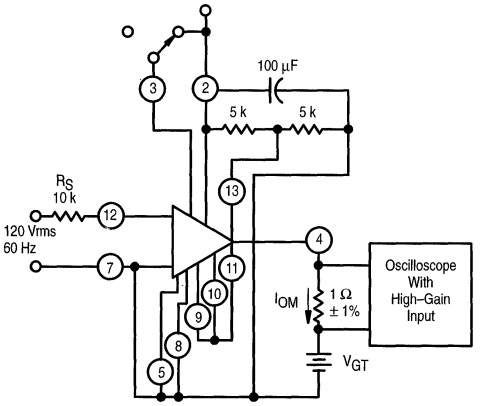


Figure 5. Input Inhibit Ratio

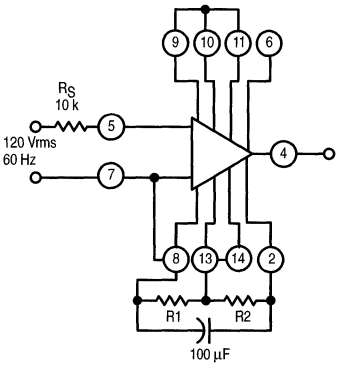


Figure 6. Gate Pulse Duration Test Circuit with Associated Waveform

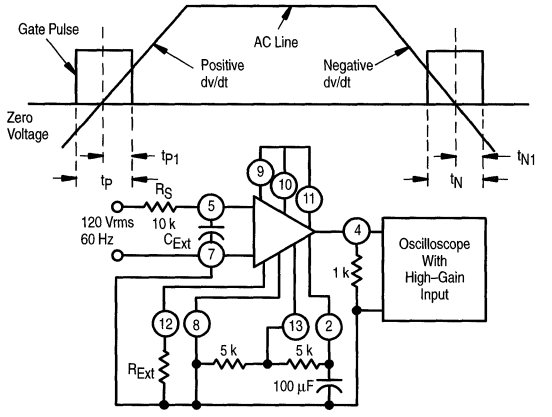
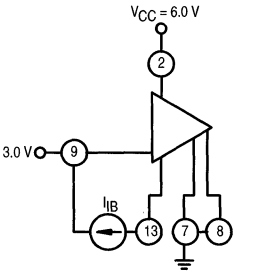


Figure 7. Input Bias Current Test Circuit



TYPICAL CHARACTERISTICS

Figure 8. Inhibit Input Voltage Test

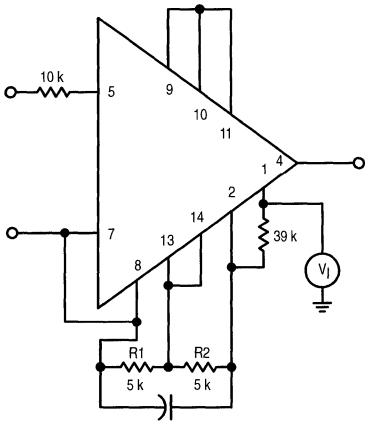
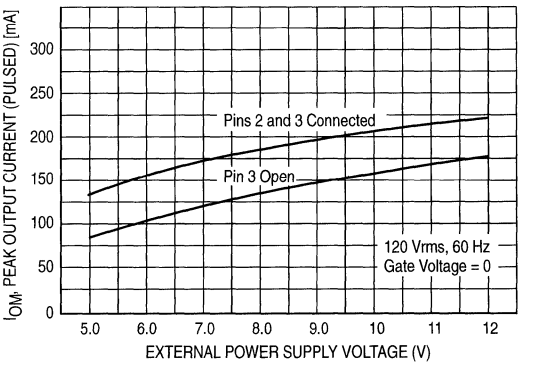


Figure 9. Peak Output Current (Pulsed) versus External Power Supply Voltage



4

Figure 10. Peak Output Current (Pulsed) versus Ambient Temperature

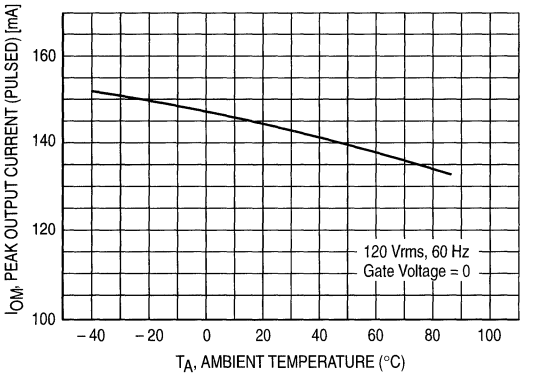


Figure 11. Total Pulse Width versus Ambient Temperature

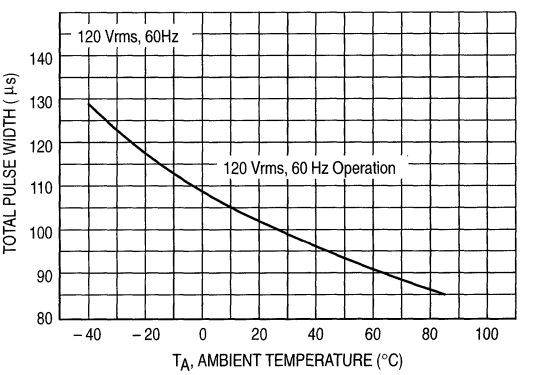


Figure 12. Internal Supply versus Ambient Temperature

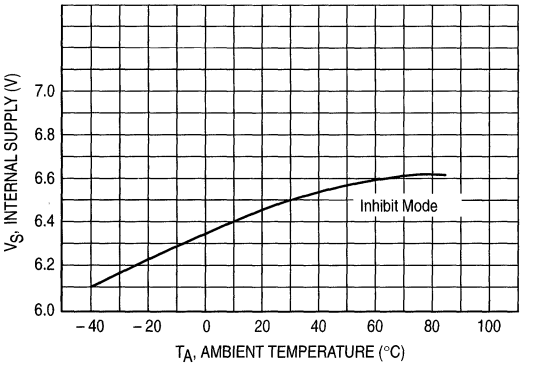


Figure 13. Inhibit Voltage Ratio versus Ambient Temperature

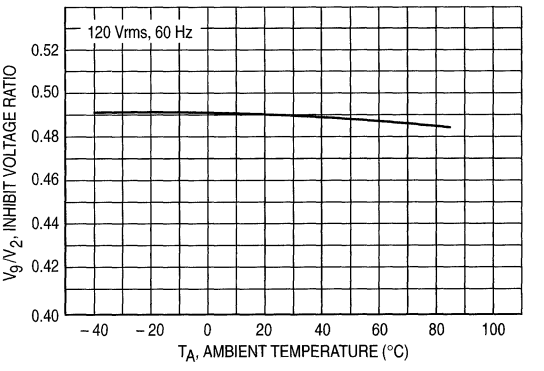
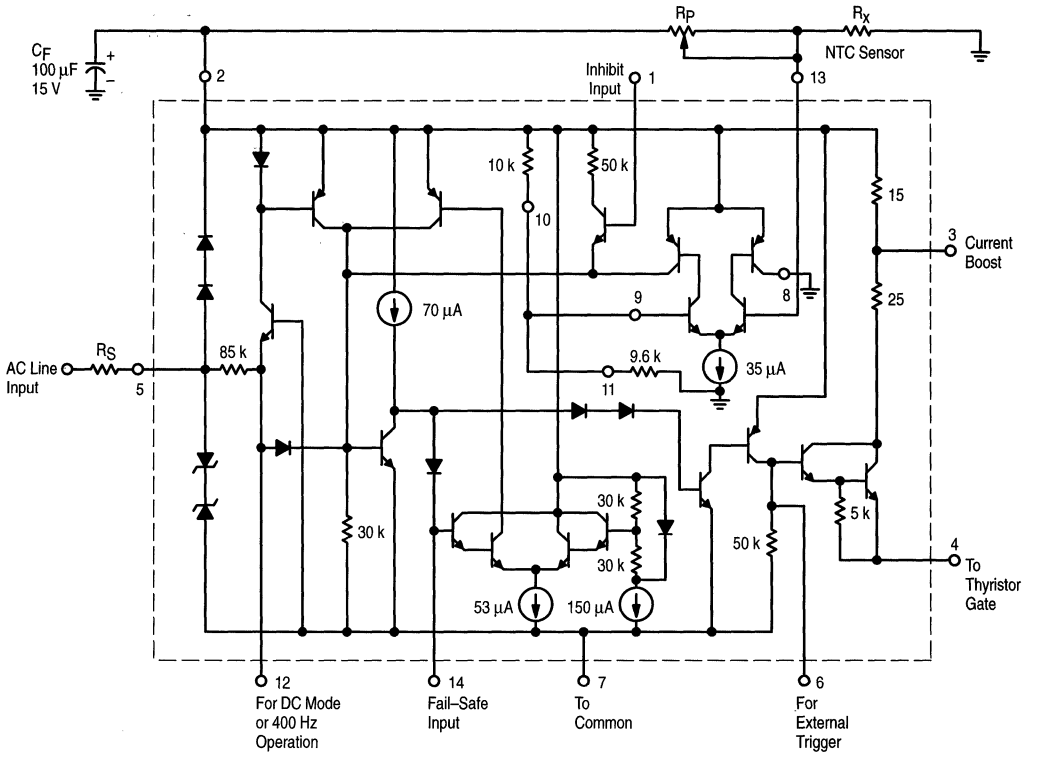


Figure 14. Circuit Schematic



NOTE: Current sources are established by an internal reference.

APPLICATION INFORMATION

Power Supply

The CA3059 is a self–powered circuit, powered from the AC line through an appropriate dropping resistor (see Table A). The internal supply is designed to power the auxiliary power circuits.

In applications where more output current from the internal supply is required, an external power supply of higher voltage should be used. To use an external power supply, connect Pin 5 and Pin 7 together and apply the synchronizing voltage to Pin 12 and the DC supply voltage to Pin 2 as shown in Figure 4.

Operation of Protection Circuit

The protection circuit, when connected, will remove current drive from the triac if an open or shorted sensor is detected. This circuit is activated by connecting Pin 13 to Pin 14 (see Figure 1).

The following conditions should be observed when the protection circuit is utilized:

a. The internal supply should be used and the external load current must be limited to 2 mA with a 5 kΩ dropping resistor.

b. Sensor Resistance (R_X) and R_P values should be between 2 kΩ and 100 kΩ.

c. The relationship $0.33 < R_X/R_P < 3$ must be met over the anticipated temperature range to prevent undesired activation of the circuit. A shunt or series resistor may have to be added.

External Inhibit Function

A priority inhibit command applied to Pin 1 will remove current drive from the thyristor. A command of at least +1.2 V @ 10 µA is required. A DTL or TTL logic 1 applied to Pin 1 will activate the inhibit function.

DC Gate Current Mode

When comparator operation is desired or inductive loads are being switched, Pins 7 and 12 should be connected. This connection disables the zero–crossing detector to permit the flow of gate current from the differential sensing amplifier on demand. Care should be exercised to avoid possible overloading of the internal power supply when operating the device in this mode. A resistor should be inserted between Pin 4 and the thyristor gate in order to limit the current.

MOTOROLA

MC3479

Stepper Motor Driver

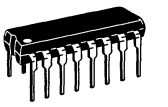
The MC3479 is designed to drive a two–phase stepper motor in the bipolar mode. The circuit consists of four input sections, a logic decoding/sequencing section, two driver–stages for the motor coils, and an output to indicate the $\overline{\text{Phase A}}$ drive state.

- Single Supply Operation: 7.2 to 16.5 V
- 350 mA/Coil Drive Capability
- Clamp Diodes Provided for Back–EMF Suppression
- Selectable $\overline{\text{CW}}$/CCW and $\overline{\text{Full}}$/Half Step Operation
- Selectable High/Low Output Impedance (Half Step Mode)
- TTL/CMOS Compatible Inputs
- Input Hysteresis: 400 mV Minimum
- Phase Logic Can Be Initialized to $\overline{\text{Phase A}}$
- $\overline{\text{Phase A}}$ Output Drive State Indication (Open–Collector)
- Available in Standard DIP and Surface Mount

STEPPER MOTOR DRIVER

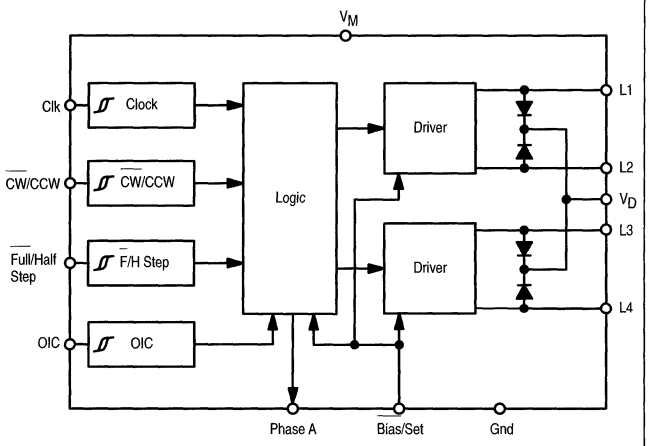
SEMICONDUCTOR TECHNICAL DATA

4

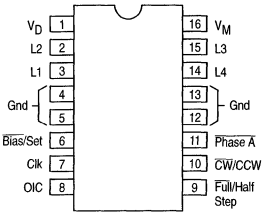


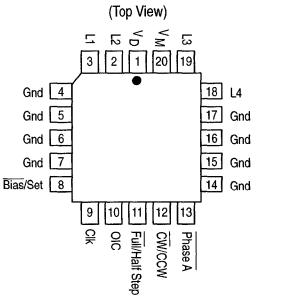
P SUFFIX
PLASTIC PACKAGE
CASE 648C

Figure 1. Representative Block Diagram



PIN CONNECTIONS





ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3479P	T_A = 0° to +70°C	Plastic

INPUT TRUTH TABLE

	Input Low	Input High
$\overline{\text{CW}}$/CCW	CW	CCW
$\overline{\text{Full}}$/Half Step	Full Step	Half Step
OIC	Hi Z	Low Z
Clk	Positive Edge Triggered	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_M	+ 18	Vdc
Clamp Diode Cathode Voltage (Pin 1)	V_D	V_M + 5.0	Vdc
Driver Output Voltage	V_{OD}	V_M + 6.0	Vdc
Drive Output Current/Coil	I_{OD}	± 500	mA
Input Voltage (Logic Controls)	V_{in}	− 0.5 to + 7.0	Vdc
$\overline{\text{Bias}}$/Set Current	I_{BS}	− 10	mA
$\overline{\text{Phase A}}$ Output Voltage	V_{OA}	+ 18	Vdc
$\overline{\text{Phase A}}$ Sink Current	I_{OA}	20	mA
Junction Temperature	T_J	+ 150	°C
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_M	+ 7.2	+ 16.5	Vdc
Clamp Diode Cathode Voltage	V_D	V_M	V_M + 4.5	Vdc
Driver Output Current (Per Coil) (Note 1)	I_{OD}	—	350	mA
Input Voltage (Logic Controls)	V_{in}	0	+ 5.5	Vdc
$\overline{\text{Bias}}$/Set Current (Outputs Active)	I_{BS}	− 300	− 75	µA
$\overline{\text{Phase A}}$ Output Voltage	V_{OA}	—	V_M	Vdc
$\overline{\text{Phase A}}$ Sink Current	I_{OA}	0	8.0	mA
Operating Ambient Temperature	T_A	0	+ 70	°C

NOTE: 1. See section on Power Dissipation in Application Information.

DC ELECTRICAL CHARACTERISTICS (Specifications apply over the recommended supply voltage and temperature range, [Notes 2, 3] unless otherwise noted.)

Characteristic	Pins	Symbol	Min	Typ	Max	Unit
INPUT LOGIC LEVELS						
Threshold Voltage (Low–to–High)	7, 8, 9, 10	V_{TLH}	—	—	2.0	Vdc
Threshold Voltage (High–to–Low)		V_{THL}	0.8	—	—	Vdc
Hysteresis		V_{HYS}	0.4	—	—	Vdc
Current: (V_I = 0.4 V) (V_I = 5.5 V) (V_I = 2.7 V)		I_{IL}	−100 — —	— — —	— +100 +20	µA
DRIVER OUTPUT LEVELS						
Output High Voltage (I_{BS} = − 300 µA): (I_{OD} = − 350 mA) (I_{OD} = − 0.1 mA)	2, 3, 14, 15	V_{OHD}	 V_M − 2.0 V_M − 1.2	 — —	 — —	Vdc
Output Low Voltage (I_{BS} = − 300 µA, I_{OD} = 350 mA)		V_{OLD}	—	—	0.8	Vdc
Differential Mode Output Voltage Difference (Note 4) (I_{BS} = − 300 µA, I_{OD} = 350 mA)		DV_{OD}	—	—	0.15	Vdc
Common Mode Output Voltage Difference (Note 5) (I_{BS} = − 300 µA, I_{OD} = − 0.1 mA)		CV_{OD}	—	—	0.15	Vdc
Output Leakage, Hi Z State (0 ≤ V_{OD} ≤ V_M, I_{BS} = − 5.0 µA) (0 ≤ V_{OD} ≤ V_M, I_{BS} = − 300 µA, F/H = 2.0 V, OIC = 0.8 V)		 I_{OZ1} I_{OZ2}	 − 100 − 100	 — —	 + 100 + 100	µA

NOTES: 2. Algebraic convention rather than absolute values is used to designate limit values.
3. Current into a pin is designated as positive. Current out of a pin is designated as negative.
4. $DV_{OD} = |V_{OD1,2} - V_{OD3,4}|$ where: $V_{OD1,2} = (V_{OHD1} - V_{OLD2})$ or $(V_{OHD2} - V_{OLD1})$, and $V_{OD3,4} = (V_{OHD3} - V_{OLD4})$ or $(V_{OHD4} - V_{OLD3})$.
5. $CV_{OD} = |V_{OHD1} - V_{OHD2}|$ or $|V_{OHD3} - V_{OHD4}|$.

DC ELECTRICAL CHARACTERISTICS (Specifications apply over the recommended supply voltage and temperature range, [Notes 2, 3] unless otherwise noted.)

Characteristic	Pins	Symbol	Min	Typ	Max	Unit
CLAMP DIODES						
Forward Voltage (I_D = 350 mA)	1, 2, 3, 14, 15	V_{DF}	—	2.5	3.0	Vdc
Leakage Current (Per Diode) (Pin 1 = 21 V; Outputs = 0 V; I_{BS} = 0 µA)		I_{DR}	—	—	100	µA
$\overline{\text{PHASE A}}$ OUTPUT						
Output Low Voltage (I_{OA} = 8.0 mA)	11	V_{OLA}	—	—	0.4	Vdc
Off State Leakage Current (V_{OHA} = 16.5 V)		I_{OHA}	—	—	100	µA
POWER SUPPLY						
Power Supply Current (I_{OD} = 0 µA, I_{BS} = – 300 µA)	16					mA
(L1 = V_{OHD}, L2 = V_{OLD}, L3 = V_{OHD}, L4 = V_{OLD})		I_{MW}	—	—	70	
(L1 = V_{OHD}, L2 = V_{OLD}, L3 = Hi Z, L4 = Hi Z)		I_{MZ}	—	—	40	
(L1 = V_{OHD}, L2 = V_{OLD}, L3 = V_{OHD}, L4 = V_{OHD})		I_{MN}	—	—	75	
$\overline{\text{BIAS}}$/SET CURRENT						
To Set $\overline{\text{Phase A}}$	6	I_{BS}	– 5.0	—	—	µA

PACKAGE THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction–to–Ambient (No Heatsink)	$R_{\theta JA}$	—	45	—	°C/W

AC SWITCHING CHARACTERISTICS (T_A = + 25°C, V_M = 12 V) (See Figures 2, 3, 4)

Characteristic	Pins	Symbol	Min	Typ	Max	Unit
Clock Frequency	7	f_{CK}	0	—	50	kHz
Clock Pulse Width (High)	7	PW_{CKH}	10	—	—	µs
Clock Pulse Width (Low)	7	PW_{CKL}	10	—	—	µs
$\overline{\text{Bias}}$/Set Pulse Width	6	PW_{BS}	10	—	—	µs
Setup Time ($\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS)	10–7 9–7	t_{su}	5.0	—	—	µs
Hold Time ($\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS)	10–7 9–7	t_h	10	—	—	µs
Propagation Delay (Clk–to–Driver Output)		t_{PCD}	—	8.0	—	µs
Propagation Delay ($\overline{\text{Bias}}$/Set–to–Driver Output)		t_{PBSD}	—	1.0	—	µs
Propagation Delay (Clk–to–$\overline{\text{Phase A}}$ Low)	7–11	t_{PHLA}	—	12	—	µs
Propagation Delay (Clk–to–$\overline{\text{Phase A}}$ High)	7–11	t_{PLHA}	—	5.0	—	µs

NOTES: 2. Algebraic convention rather than absolute values is used to designate limit values.
3. Current into a pin is designated as positive. Current out of a pin is designated as negative.

Figure 2. AC Test Circuit

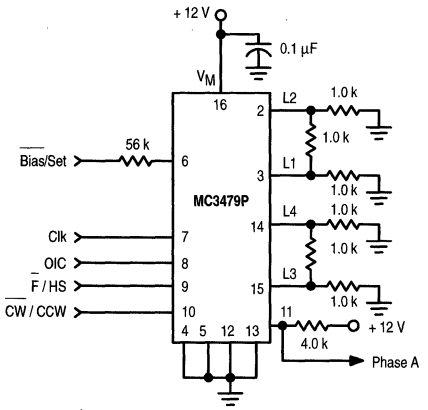
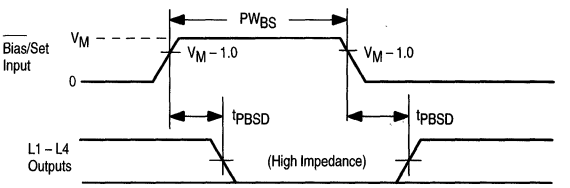


Figure 3. Bias/Set Timing (Refer to Figure 2)



Note: t_r, t_f (10% to 90%) for input signals are ≤ 25 ns.

PIN FUNCTION DESCRIPTION

Pin No. 20–Pin	Pin No. 16–Pin	Function	Symbol	Description
20	16	Power Supply	V_M	Power supply pin for both the logic circuit and the motor coil current. Voltage range is + 7.2 to + 16.5 volts.
4, 5, 6, 7, 14, 15, 16, 17	4, 5, 12, 13	Ground	Gnd	Ground pins for the logic circuit and the motor coil current. The physical configuration of the pins aids in dissipating heat from within the IC package.
1	1	Clamp Diode Voltage	V_D	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and Pin 16. See Figure 11.
2, 3, 18, 19	2, 3, 14, 15	Driver Outputs	L1, L2 L3, L4	High current outputs for the motor coils. L1 and L2 are connected to one coil, and L3 and L4 to the other coil.
8	6	$\overline{\text{Bias}}$/Set	$\overline{\text{B}}$/S	This pin is typically 0.7 volts below V_M. The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened (I_{BS} < 5.0 µA) the outputs assume a high impedance condition, while the internal logic presets to a $\overline{\text{Phase A}}$ condition.
9	7	Clock	Clk	The positive edge of the clock input switches the outputs to the next position. This input has no effect if Pin 6 is open.
11	9	$\overline{\text{Full}}$/Half Step	$\overline{\text{F}}$/HS	When low (Logic "0"), each clock input pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one–half step. See Figure 7 for sequence.
12	10	$\overline{\text{Clockwise}}$/ Counterclockwise	$\overline{\text{CW}}$/CCW	This input allows reversing the rotation of the motor. See Figure 7 for sequence.
10	8	Output Impedance Control	OIC	This input is relevant only in the half step mode (Pin 9 > 2.0 V). When low (Logic "0"), the two driver outputs of the non–energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance referenced to V_M. See Figure 7.
13	11	Phase A	Ph A	This open–collector output indicates (when low) that the driver outputs are in the $\overline{\text{Phase A}}$ condition (L1 = L3 = V_{OHD}, L2 = L4 = V_{OLD}).

APPLICATION INFORMATION

General

The MC3479 integrated circuit is designed to drive a stepper positioning motor in applications such as disk drives and robotics. The outputs can provide up to 350 mA to each of two coils of a two–phase motor. The outputs change state with each low–to–high transition of the clock input, with the new output state depending on the previous state, as well as the input conditions at the logic controls.

Outputs

The outputs (L1–L4) are high current outputs (see Figure 5), which when connected to a two–phase motor, provide two full–bridge configurations (L3 and L4 are not shown in Figure 5). The polarities applied to the motor coils depend on which transistor (Q_H or Q_L) of each output is on, which in turn depends on the inputs and the decoding circuitry.

Figure 4. Clock Timing
(Refer to Figure 2)

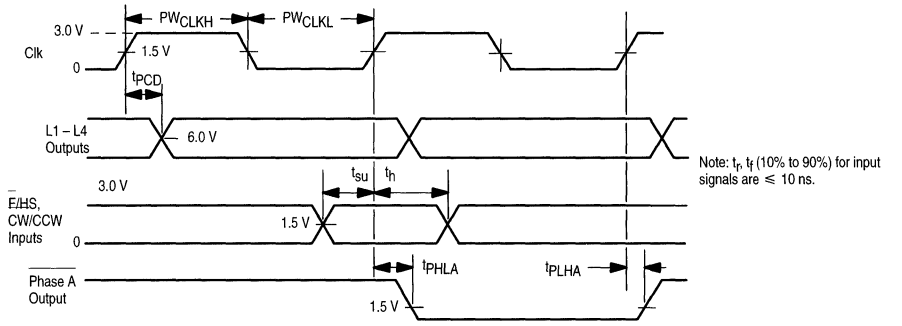
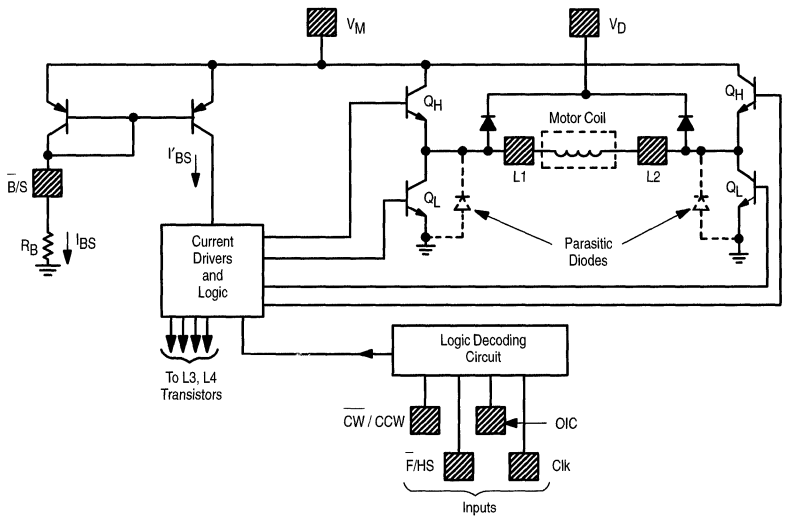


Figure 5. Output Stages

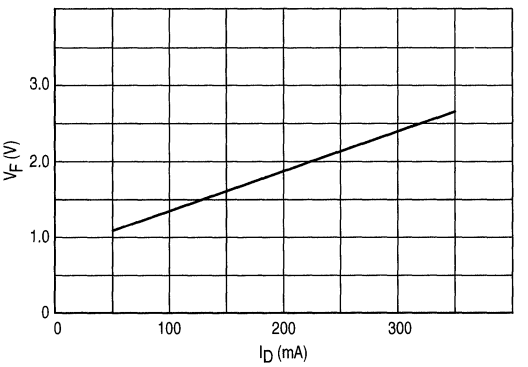


The maximum sink current available at the outputs is a function of the resistor connected between Pin 6 and ground (see section on Bias/Set operation). Whenever the outputs are to be in a high impedance state, both transistors (Q_H and Q_L of Figure 5) of each output are off.

V_D

This pin allows for provision of a current path for the motor coil current during switching, in order to suppress back–EMF voltage spikes. V_D is normally connected to V_M (Pin 16) through a diode (zener or regular), a resistor, or directly. The peaks instantaneous voltage at the outputs must not exceed V_M by more than 6.0 V. The voltage drop across the internal clamping diodes must be included in this portion of the design (see Figure 6). Note the parasitic diodes (Figure 5) across each Q_L of each output provide for a complete circuit path for the switched current.

Figure 6. Clamp Diode Characteristics



$\overline{\text{Full}}$/Half Step

When this input is at a Logic "0" (<0.8 V), the outputs change a full step with each clock cycle, with the sequence direction depending on the $\overline{\text{CW}}$/CCW input. There are four steps ($\overline{\text{Phase A}}$, $\overline{\text{B}}$, $\overline{\text{C}}$, $\overline{\text{D}}$) for each complete cycle of the sequencing logic. Current flows through both motor coils during each step, as shown in Figure 7.

When taken to a Logic "1" (>2.0 V), the outputs change a half step with each clock cycle, with the sequence direction depending on the $\overline{\text{CW}}$/CCW input. Eight steps ($\overline{\text{Phase A}}$ to $\overline{\text{H}}$) result for each complete cycle of the sequencing logic. $\overline{\text{Phase A}}$, $\overline{\text{C}}$, $\overline{\text{E}}$ and $\overline{\text{G}}$ correspond (in polarity) to $\overline{\text{Phase A}}$, $\overline{\text{B}}$, $\overline{\text{C}}$, and $\overline{\text{D}}$, respectively, of the full step sequence. $\overline{\text{Phase B}}$, $\overline{\text{D}}$, $\overline{\text{F}}$ and $\overline{\text{H}}$ provide current to one motor coil, while de–energizing the other coil. The condition of the outputs of the de–energized coil depends on the OIC input, see Figure 7 timing diagram.

OIC

The output impedance control input determines the output impedance to the de–energized coil when operating in the half–step mode. When the outputs are in $\overline{\text{Phase B}}$, $\overline{\text{D}}$, $\overline{\text{F}}$ or $\overline{\text{H}}$ (Figure 7) and this input is at a Logic "0" (<0.8 V), the two outputs to the de–energized coil are in a high impedance condition — Q_L and Q_H of both outputs (Figure 5) are off. When this input is at a Logic "1" (>2.0 V), a low impedance output is provided to the de–energized coil as both outputs have Q_H on (Q_L off). To complete the low impedance path requires connecting V_D to V_M as described elsewhere in this data sheet.

$\overline{\text{Bias}}$/Set

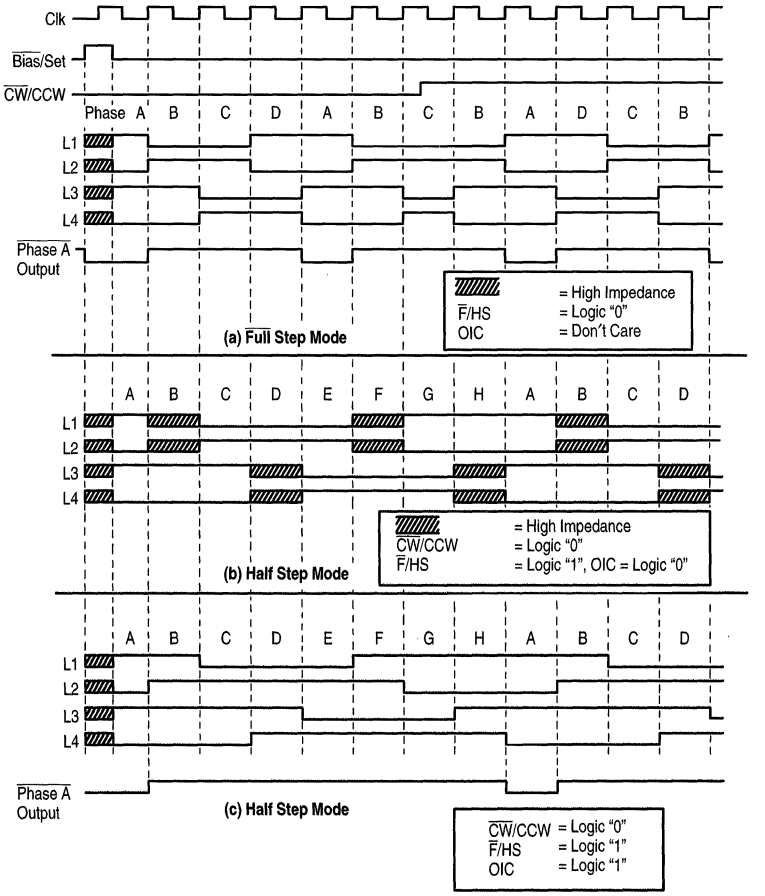
This pin can be used for three functions: a) determining the maximum output sink current; b) setting the internal logic to a known state; and c) reducing power consumption.

a) The maximum output sink current is determined by the base drive current supplied to the lower transistors (Q_Ls of Figure 5) of each output, which in turn, is a function of I_{BS}. The appropriate value of I_{BS} is determined by:

$$I_{BS} = I_{OD} \times 0.86$$

where I_{BS} is in microamps, and I_{OD} is the motor current/coil in milliamps.

Figure 7. Output Sequence



The value of R_B (between this pin and ground) is then determined by:

$$R_B = \frac{V_M - 0.7\ V}{I_{BS}}$$

b) When this pin is opened (raised to V_M) such that I_{BS} is <5.0 μA, the internal logic is set to the $\overline{\text{Phase A}}$ condition, and the four driver outputs are put into a high impedance state. The $\overline{\text{Phase A}}$ output (Pin 11) goes active (low), and input signals at the controls are ignored during this time. Upon re–establishing I_{BS}, the driver outputs become active, and will be in the $\overline{\text{Phase A}}$ position (L1 = L3 = V_{OHD}, L2 = L4 = V_{OLD}). The circuit will then respond to the inputs at the controls.

The Set function (opening this pin) can be used as a power–up reset while supply voltages are settling. A CMOS logic gate (powered by V_M) can be used to control this pin as shown in Figure 11.

c) Whenever the motor is not being stepped, power dissipation in the IC and in the motor may be lowered by reducing I_{BS}, so as to reduce the output (motor) current. Setting I_{BS} to 75 μA will reduce the motor current, but will not reset the internal logic as described above. See Figure 12 for a suggested circuit.

Power Dissipation

The power dissipated by the MC3479 must be such that the junction temperature (T_J) does not exceed 150°C. The power dissipated can be expressed as:

$$P = (V_M \times I_M) + (2 \times I_{OD})\ [(V_M - V_{OHD}) + V_{OLD}]$$

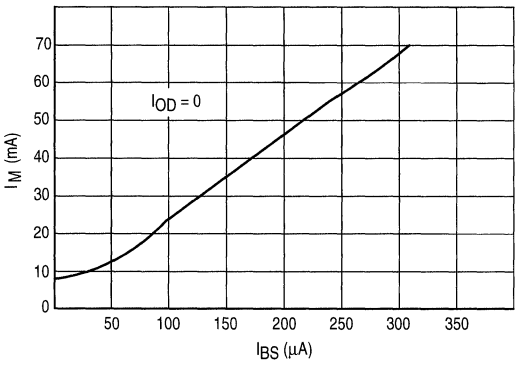
where V_M = Supply voltage;
I_M = Supply current other than I_{OD};
I_{OD} = Output current to each motor coil;
V_{OHD} = Driver output high voltage;
V_{OLD} = Driver output low voltage.

The power supply current (I_M) is obtained from Figure 8. After the power dissipation is calculated, the junction temperature can be calculated using:

$$T_J = (P \times R_{\theta JA}) + T_A$$

where $R_{\theta JA}$ = Junction–to–ambient thermal resistance (52°C/W for the DIP, 72°C/W for the FN Package);
T_A = Ambient Temperature.

Figure 8. Power Supply Current



For example, assume an application where V_M = 12 V, the motor requires 200 mA/coil, operating at room temperature with no heatsink on the IC. I_{BS} is calculated:

$I_{BS} = 200 \times 0.86$
$I_{BS} = 172\ \mu A$

R_B is calculated:

$R_B = (12 - 0.7)\ V/172\ \mu A$
$R_B = 65.7\ k\Omega$

From Figure 8, I_M (max) is determined to be 40 mA. From Figure 9, V_{OLD} is 0.46 volts, and from Figure 10, ($V_M - V_{OHD}$) is 1.4 volts.

$P = (12 \times 0.040) + (2 \times 0.2)\ (1.4 + 0.46)$
$P = 1.22\ W$
$T_J = (1.22\ W \times 52°C/W) + 25°C$
$T_J = 88°C$

This temperature is well below the maximum limit. If the calculated T_J had been higher than 150°C, a heatsink such as the Staver Co. V–7 Series, Aavid #5802, or Thermalloy #6012 could be used to reduce $R_{\theta JA}$. In extreme cases, forced air cooling should be considered.

The above calculation, and $R_{\theta JA}$, assumes that a ground plane is provided under the MC3479 (either or both sides of the PC board) to aid in the heat dissipation. Single nominal width traces leading from the four ground pins should be avoided as this will increase T_J, as well as provide potentially disruptive ground noise and I_R drops when switching the motor current.

Figure 9. Maximum Saturation Voltage — Driver Output Low

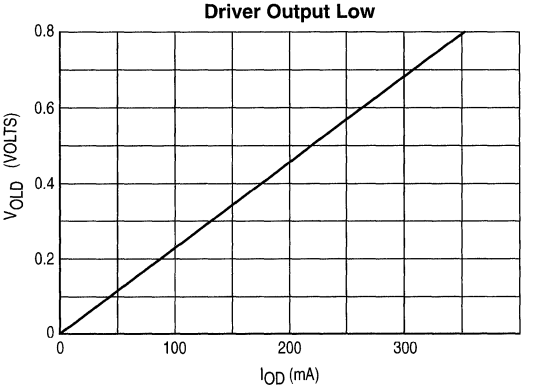


Figure 10. Maximum Saturation Voltage — Driver Output High

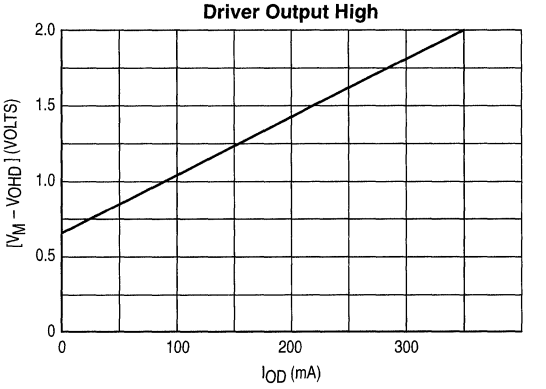


Figure 11. Typical Applications Circuit

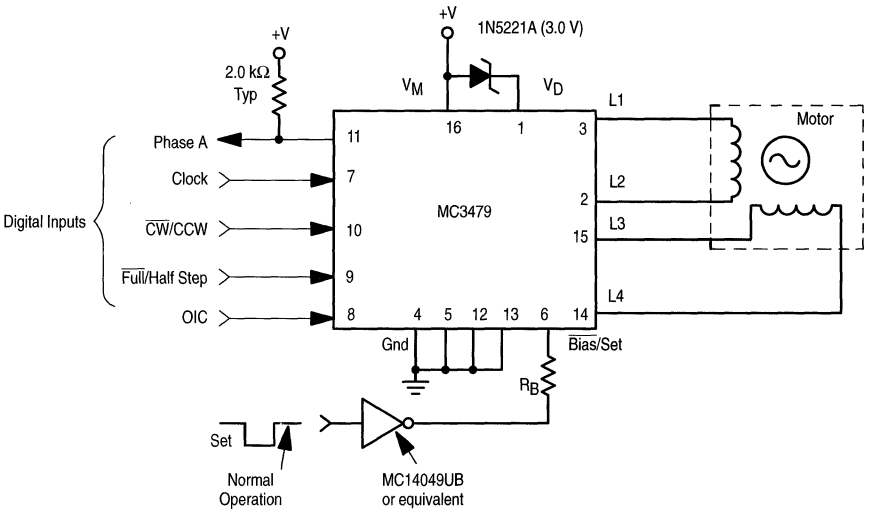
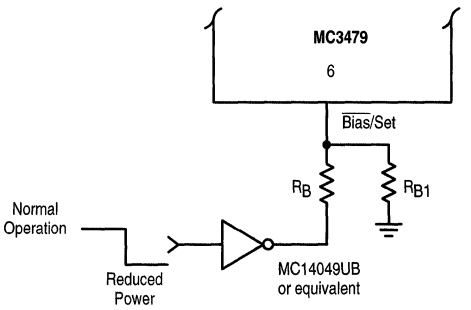


Figure 12. Power Reduction



— Suggested value for R_{B1} (V_M = 12 V) is 150 kΩ.
— R_B calculation (see text) must take into account the current through R_{B1}.

MOTOROLA

MC33030

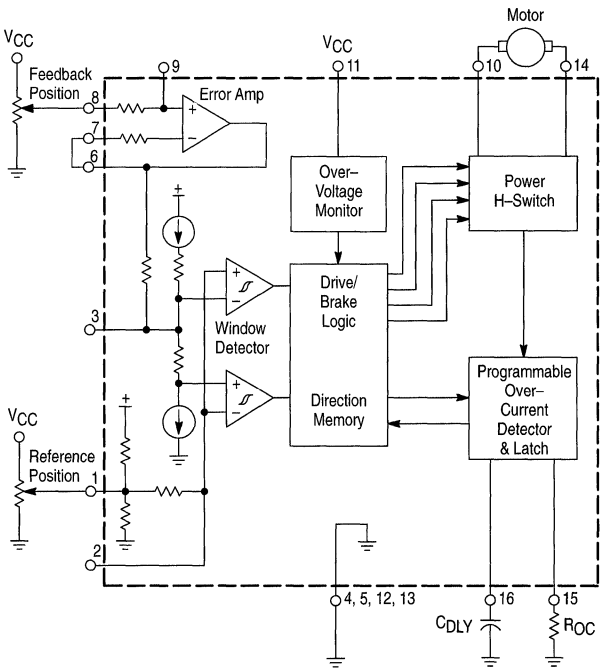
DC Servo Motor Controller/Driver

The MC33030 is a monolithic DC servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on–chip op amp and window comparator with wide input common–mode range, drive and brake logic with direction memory, Power H–Switch driver capable of 1.0 A, independently programmable over–current monitor and shutdown delay, and over–voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.

Although this device is primarily intended for servo applications, it can be used as a switchmode motor controller.

- On–Chip Error Amp for Feedback Monitoring
- Window Detector with Deadband and Self Centering Reference Input
- Drive/Brake Logic with Direction Memory
- 1.0 A Power H–Switch
- Programmable Over–Current Detector
- Programmable Over–Current Shutdown Delay
- Over–Voltage Shutdown

Representative Block Diagram

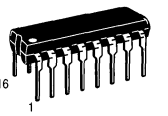


This device contains 119 active transistors.

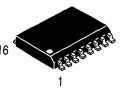
DC SERVO MOTOR CONTROLLER/DRIVER

SEMICONDUCTOR TECHNICAL DATA

4

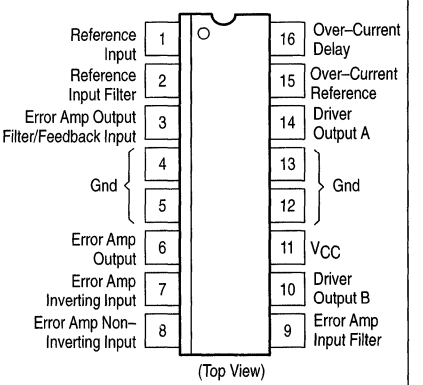


P SUFFIX
PLASTIC PACKAGE
CASE 648C
(DIP–16)



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP–16L)

PIN CONNECTIONS



(Top View)

Pins 4, 5, 12 and 13 are electrical ground and heat sink pins for IC.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33030DW	$T_A = -40°$ to $+85°C$	SOP–16L
MC33030P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	36	V
Input Voltage Range Op Amp, Comparator, Current Limit (Pins 1, 2, 3, 6, 7, 8, 9, 15)	V_{IR}	−0.3 to V_{CC}	V
Input Differential Voltage Range Op Amp, Comparator (Pins 1, 2, 3, 6, 7, 8, 9)	V_{IDR}	−0.3 to V_{CC}	V
Delay Pin Sink Current (Pin 16)	$I_{DLY(sink)}$	20	mA
Output Source Current (Op Amp)	I_{source}	10	mA
Drive Output Voltage Range (Note 1)	V_{DRV}	−0.3 to (V_{CC} + V_F)	V
Drive Output Source Current (Note 2)	$I_{DRV(source)}$	1.0	A
Drive Output Sink Current (Note 2)	$I_{DRV(sink)}$	1.0	A
Brake Diode Forward Current (Note 2)	I_F	1.0	A
Power Dissipation and Thermal Characteristics			°C/W
P Suffix, Dual In Line Case 648C			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	80	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	15	
DW Suffix, Dual In Line Case 751G			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	94	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	18	
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES: 1. The upper voltage level is clamped by the forward drop, V_F, of the brake diode.
2. These values are for continuous DC current. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMP					
Input Offset Voltage (− 40°C ≤ T_A ≤ 85°C) $V_{Pin\ 6}$ = 7.0 V, R_L = 100 k	V_{IO}	–	1.5	10	mV
Input Offset Current ($V_{Pin\ 6}$ = 1.0 V, R_L = 100 k)	I_{IO}	–	0.7	–	nA
Input Bias Current ($V_{Pin\ 6}$ = 7.0 V, R_L = 100 k)	I_{IB}	–	7.0	–	nA
Input Common–Mode Voltage Range ΔV_{IO} = 20 mV, R_L = 100 k	V_{ICR}	–	0 to (V_{CC} − 1.2)	–	V
Slew Rate, Open Loop (V_{ID} = 0.5 V, C_L = 15 pF)	SR	–	0.40	–	V/μs
Unity–Gain Crossover Frequency	f_c	–	550	–	kHz
Unity–Gain Phase Margin	ϕm	–	63	–	deg.
Common–Mode Rejection Ratio ($V_{Pin\ 6}$ = 7.0 V, R_L = 100 k)	CMRR	50	82	–	dB
Power Supply Rejection Ratio V_{CC} = 9.0 to 16 V, $V_{Pin\ 6}$ = 7.0 V, R_L = 100 k	PSRR	–	89	–	dB
Output Source Current ($V_{Pin\ 6}$ = 12 V)	I_{O+}	–	1.8	–	mA
Output Sink Current ($V_{Pin\ 6}$ = 1.0 V)	I_{O-}	–	250	–	μA
Output Voltage Swing (R_L = 17 k to Ground)	V_{OH} V_{OL}	12.5 –	13.1 0.02	– –	V V

NOTES: 3. The upper or lower hysteresis will be lost when operating the Input, Pin 3, close to the respective rail. Refer to Figure 4.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 14 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
WINDOW DETECTOR					
Input Hysteresis Voltage ($V_1 - V_4$, $V_2 - V_3$, Figure 18)	V_H	25	35	45	mV
Input Dead Zone Range ($V_2 - V_4$, Figure 18)	V_{IDZ}	166	210	254	mV
Input Offset Voltage ($\lvert [V_2 - V_{Pin\ 2}] - [V_{Pin\ 2} - V_4] \rvert$ Figure 18)	V_{IO}	–	25	–	mV
Input Functional Common–Mode Range (Note 3) Upper Threshold Lower Threshold	 V_{IH} V_{IL}	 – –	 (V_{CC} – 1.05) 0.24	 – –	V
Reference Input Self Centering Voltage Pins 1 and 2 Open	V_{RSC}	–	(1/2 V_{CC})	–	V
Window Detector Propagation Delay Comparator Input, Pin 3, to Drive Outputs V_{ID} = 0.5 V, $R_{L(DRV)}$ = 390 Ω	$t_{p(IN/DRV)}$	–	2.0	–	µs
OVER–CURRENT MONITOR					
Over–Current Reference Resistor Voltage (Pin 15)	R_{OC}	3.9	4.3	4.7	V
Delay Pin Source Current V_{DLY} = 0 V, R_{OC} = 27 k, I_{DRV} = 0 mA	$I_{DLY(source)}$	–	5.5	6.9	µA
Delay Pin Sink Current (R_{OC} = 27 k, I_{DRV} = 0 mA) V_{DLY} = 5.0 V V_{DLY} = 8.3 V V_{DLY} = 14 V	$I_{DLY(sink)}$	 – – –	 0.1 0.7 16.5	 – – –	mA
Delay Pin Voltage, Low State (I_{DLY} = 0 mA)	$V_{OL(DLY)}$	–	0.3	0.4	V
Over–Current Shutdown Threshold V_{CC} = 14 V V_{CC} = 8.0 V	$V_{th(OC)}$	 6.8 5.5	 7.5 6.0	 8.2 6.5	V
Over–Current Shutdown Propagation Delay Delay Capacitor Input, Pin 16, to Drive Outputs, V_{ID} = 0.5 V	$t_{p(DLY/DRV)}$	–	1.8	–	µs
POWER H–SWITCH					
Drive–Output Saturation (– 40°C ≤ T_A ≤ + 85°C, Note 4) High–State (I_{source} = 100 mA) Low–State (I_{sink} = 100 mA)	 $V_{OH(DRV)}$ $V_{OL(DRV)}$	 (V_{CC} – 2) –	 (V_{CC} – 0.85) 0.12	 – 1.0	V
Drive–Output Voltage Switching Time (C_L = 15 pF) Rise Time Fall Time	 t_r t_f	 – –	 200 200	 – –	ns
Brake Diode Forward Voltage Drop (I_F = 200 mA, Note 4)	V_F	–	1.04	2.5	V
TOTAL DEVICE					
Standby Supply Current	I_{CC}	–	14	25	mA
Over–Voltage Shutdown Threshold (– 40°C ≤ T_A ≤ + 85°C)	$V_{th(OV)}$	16.5	18	20.5	V
Over–Voltage Shutdown Hysteresis (Device "off" to "on")	$V_{H(OV)}$	0.3	0.6	1.0	V
Operating Voltage Lower Threshold (– 40°C ≤ T_A ≤ + 85°C)	V_{CC}	–	7.5	8.0	V

NOTES: 3. The upper or lower hysteresis will be lost when operating the Input, Pin 3, close to the respective rail. Refer to Figure 4.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

Figure 1. Error Amp Input Common–Mode Voltage Range versus Temperature

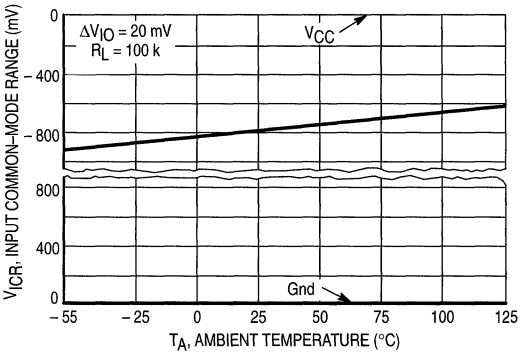


Figure 2. Error Amp Output Saturation versus Load Current

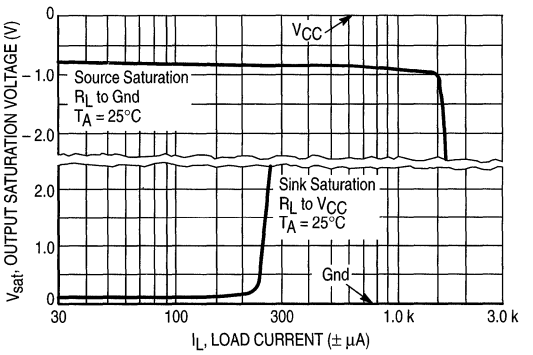


Figure 3. Open Loop Voltage Gain and Phase versus Frequency

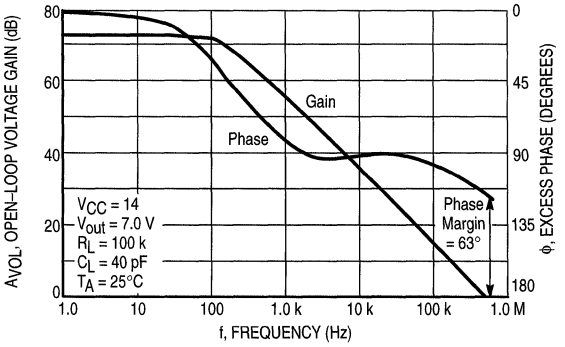


Figure 4. Window Detector Reference–Input Common–Mode Voltage Range versus Temperature

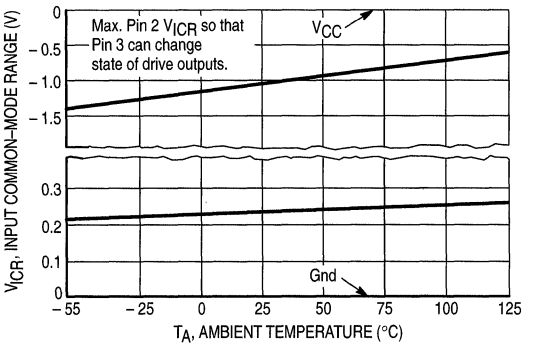


Figure 5. Window Detector Feedback–Input Thresholds versus Temperature

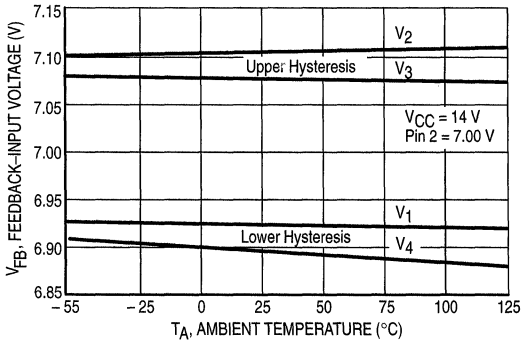


Figure 6. Output Driver Saturation versus Load Current

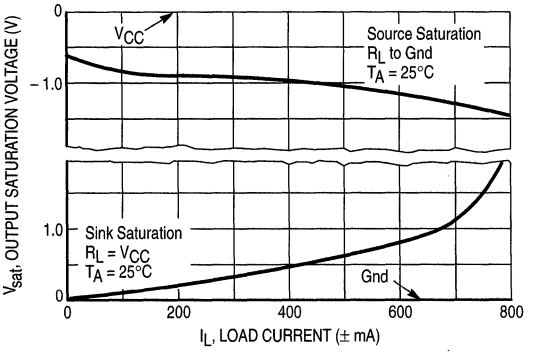


Figure 7. Brake Diode Forward Current versus Forward Voltage

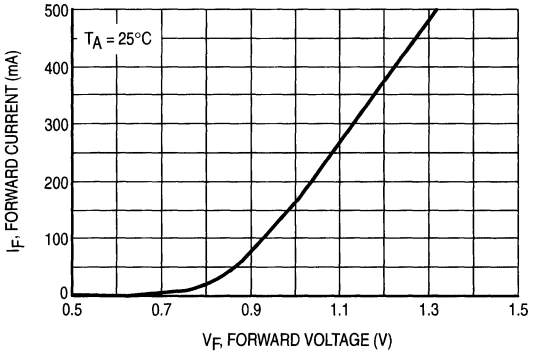


Figure 8. Output Source Current–Limit versus Over–Current Reference Resistance

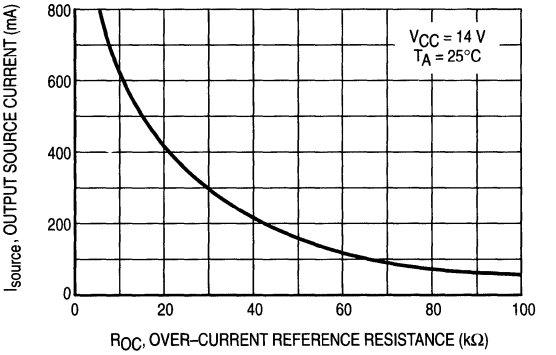


Figure 9. Output Source Current–Limit versus Temperature

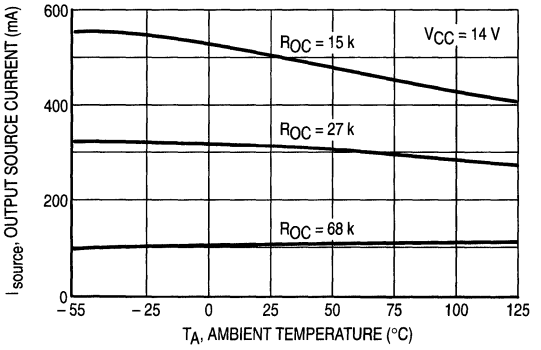


Figure 10. Normalized Delay Pin Source Current versus Temperature

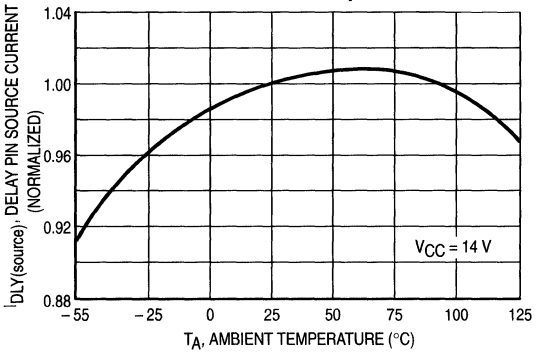


Figure 11. Normalized Over–Current Delay Threshold Voltage versus Temperature

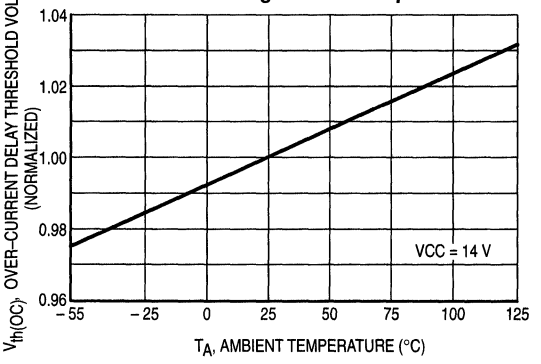


Figure 12. Supply Current versus Supply Voltage

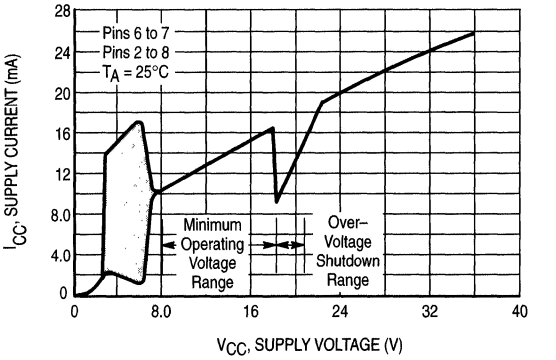


Figure 13. Normalized Over–Voltage Shutdown Threshold versus Temperature

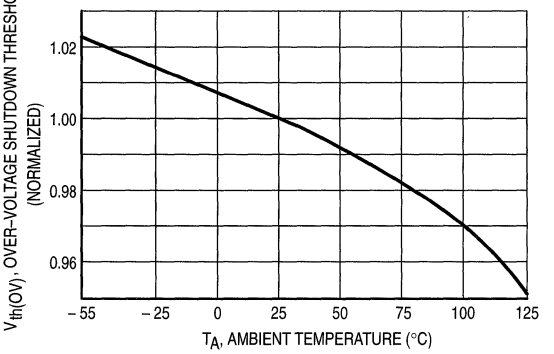


Figure 14. Normalized Over–Voltage Shutdown Hysteresis versus Temperature

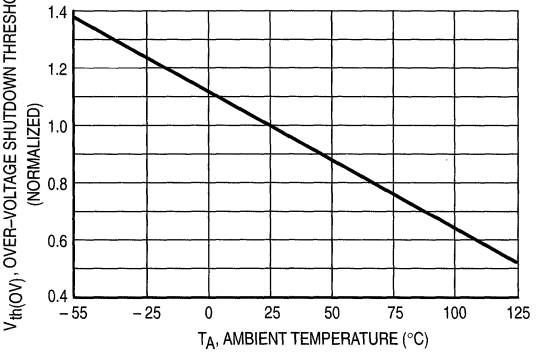


Figure 15. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

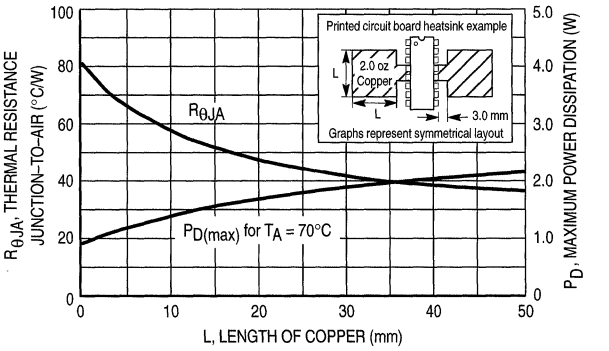
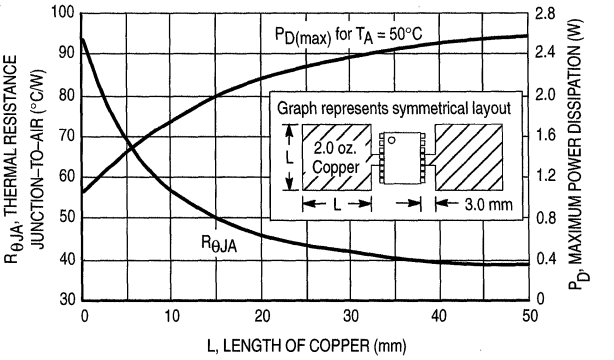


Figure 16. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



OPERATING DESCRIPTION

The MC33030 was designed to drive fractional horsepower DC motors and sense actuator position by voltage feedback. A typical servo application and representative internal block diagram are shown in Figure 17. The system operates by setting a voltage on the reference input of the Window Dectector (Pin 1) which appears on (Pin 2). A DC motor then drives a position sensor, usually a potentiometer driven by a gear box, in a corrective fashion so that a voltage proportional to position is present at Pin 3. The servo motor will continue to run until the voltage at Pin 3 falls within the dead zone, which is centered about the reference voltage.

The Window Detector is composed of two comparators, A and B, each containing hysteresis. The reference input, common to both comparators, is pre–biased at 1/2 V_{CC} for simple two position servo systems and can easily be overriden by an external voltage divider. The feedback voltage present at Pin 3 is connected to the center of two resistors that are driven by an equal magnitude current source and sink. This generates an offset voltage at the input of each comparator which is centered about Pin 3 that can float virtually from V_{CC} to ground. The sum of the upper and lower offset voltages is defined as the window detector input dead zone range.

To increase system flexibility, an on–chip Error Amp is provided. It can be used to buffer and/or gain–up the actuator position voltage which has the effect of narrowing the dead zone range. A PNP differential input stage is provided so that the input common–mode voltage range will include ground. The main design goal of the error amp output stage was to be able to drive the window detector input. It typically can source 1.8 mA and sink 250 μA. Special design considerations must be made if it is to be used for other applications.

The Power H–Switch provides a direct means for motor drive and braking with a maximum source, sink, and brake current of 1.0 A continuous. Maximum package power dissipation limits must be observed. Refer to Figure 15 for thermal information. For greater drive current requirements, a method for buffering that maintains all the system features is shown in Figure 30.

The Over–Current Monitor is designed to distinguish between motor start–up or locked rotor conditions that can occur when the actuator has reached its travel limit. A fraction of the Power H–Switch source current is internally fed into one of the two inverting inputs of the current comparator, while the non–inverting input is driven by a programmable current reference. This reference level is controlled by the resistance value selected for R_{OC}, and must be greater than the required motor run–current with its mechanical load over temperature; refer to Figure 8. During an over–current condition, the comparator will turn off and allow the current source to charge the delay capacitor, C_{DLY}. When C_{DLY} charges to a level of 7.5 V, the set input of the over–current latch will go high, disabling the drive and brake functions of the Power H–Switch. The programmable time delay is determined by the capacitance value–selected for C_{DLY}.

$$t_{DLY} = \frac{V_{ref}\ C_{DLY}}{I_{DLY(source)}} = \frac{7.5\ C_{DLY}}{5.5\ \mu A} = 1.36\ C_{DLY}\ \text{in}\ \mu F$$

This system allows the Power H–Switch to supply motor start–up current for a predetermined amount of time. If the rotor is locked, the system will time–out and shut–down. This feature eliminates the need for servo end–of–travel or limit switches. Care must be taken so as not to select too large of a capacitance value for C_{DLY}. An over–current condition for an excessively long time–out period can cause the integrated circuit to overheat and eventually fail. Again, the maximum package power dissipation limits must be observed. The over–current latch is reset upon power–up or by readjusting $V_{Pin\ 2}$ as to cause $V_{Pin\ 3}$ to enter or pass through the dead zone. This can be achieved by requesting the motor to reverse direction.

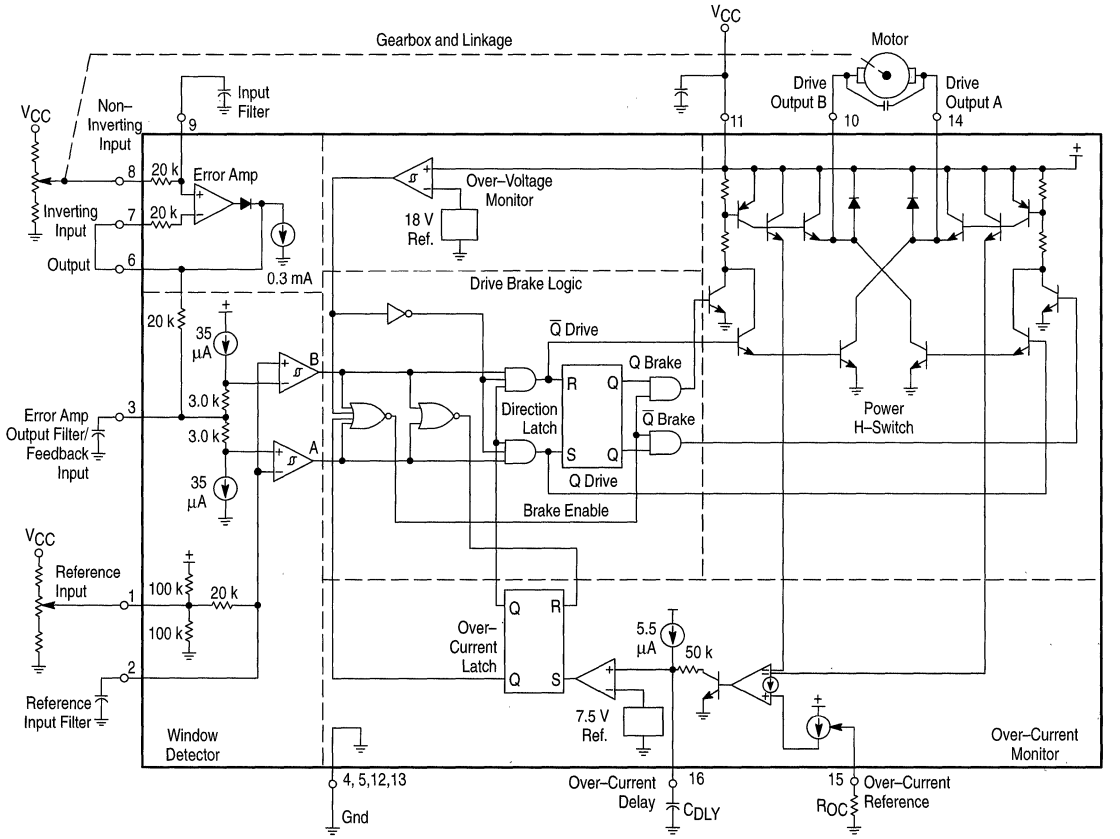
An Over–Voltage Monitor circuit provides protection for the integrated circuit and motor by disabling the Power H–Switch functions if V_{CC} should exceed 18 V. Resumption of normal operation will commence when V_{CC} falls below 17.4 V.

A timing diagram that depicts the operation of the Drive/Brake Logic section is shown in Figure 18. The waveforms grouped in [1] show a reference voltage that was preset, appearing on Pin 2, which corresponds to the desired actuator position. The true actuator position is represented by the voltage on Pin 3. The points V_1 through V_4 represent the input voltage thresholds of comparators A and B that cause a change in their respective output state. They are defined as follows:

V_1 = Comparator B turn–off threshold
V_2 = Comparator A turn–on threshold
V_3 = Comparator A turn–off threshold
V_4 = Comparator B turn–on threshold
V_1–V_4 = Comparator B input hysteresis voltage
V_2–V_3 = Comparator A input hysteresis voltage
V_2–V_4 = Window detector input dead zone range
$|(V_2–V_{Pin2}) – (V_{Pin2} – V_4)|$ = Window detector input voltage

It must be remembered that points V_1 through V_4 always try to follow and center about the reference voltage setting if it is within the input common–mode voltage range of Pin 3; Figures 4 and 5. Initially consider that the feedback input voltage level is somewhere on the dashed line between V_2 and V_4 in [1]. This is within the dead zone range as defined above and the motor will be off. Now if the reference voltage is raised so that $V_{Pin\ 3}$ is less than V_4, comparator B will turn–on [3] enabling $\overline{Q}$ Drive, causing Drive Output A to sink and B to source motor current [8]. The actuator will move in Direction B until $V_{Pin\ 3}$ becomes greater than V_1. Comparator B will turn–off, activating the brake enable [4] and $\overline{Q}$ Brake [6] causing Drive Output A to go high and B to go into a high impedance state. The inertia of the mechanical system will drive the motor as a generator creating a positive voltage on Pin 10 with respect to Pin 14. The servo system can be stopped quickly, so as not to over–shoot through the dead zone range, by braking. This is accomplished by shorting the motor/generator terminals together. Brake current will flow into the diode at Drive Output B, through the internal V_{CC} rail, and out the emitter of the sourcing transistor at Drive Output A. The end of the solid line and beginning of the dashed for $V_{Pin\ 3}$ [1] indicates the possible resting position of the actuator after braking.

Figure 17. Representative Block Diagram and Typical Servo Application



If $V_{Pin\ 3}$ should continue to rise and become greater than V_2, the actuator will have over shot the dead zone range and cause the motor to run in Direction A until $V_{Pin\ 3}$ is equal to V_3. The Drive/Brake behavior for Direction A is identical to that of B. Overshooting the dead zone range in both directions can cause the servo system to continuously hunt or oscillate. Notice that the last motor run–direction is stored in the direction latch. This information is needed to determine whether Q or $\overline{Q}$ Brake is to be enabled when $V_{Pin\ 3}$ enters the dead zone range. The dashed lines in [8,9] indicate the resulting waveforms of an over–current condition that has exceeded the programmed time delay. Notice that both Drive Outputs go into a high impedance state until $V_{Pin\ 2}$ is readjusted so that $V_{Pin\ 3}$ enters or crosses through the dead zone [7, 4].

The inputs of the Error Amp and Window Detector can be susceptible to the noise created by the brushes of the DC motor and cause the servo to hunt. Therefore, each of these inputs are provided with an internal series resistor and are pinned out for an external bypass capacitor. It has been found that placing a capacitor with *short leads* directly across the brushes will significantly reduce noise problems. Good quality RF bypass capacitors in the range of 0.001 to 0.1 µF may be required. Many of the more economical motors will generate significant levels of RF energy over a spectrum that extends from DC to beyond 200 MHz. The capacitance value and method of noise filtering must be determined on a system by system basis.

Thus far, the operating description has been limited to servo systems in which the motor mechanically drives a potentiometer for position sensing. Figures 19, 20, 27, and 31 show examples that use light, magnetic flux, temperature, and pressure as a means to drive the feedback element. Figures 21, 22 and 23 are examples of two position, open loop servo systems. In these systems, the motor runs the actuator to each end of its travel limit where the Over–Current Monitor detects a locked rotor condition and shuts down the drive. Figures 32 and 33 show two possible methods of using the MC33030 as a switching motor controller. In each example a fixed reference voltage is applied to Pin 2. This causes $V_{pin\ 3}$ to be less than V_4 and Drive Output A, Pin 14, to be in a low state saturating the TIP42 transistor. In Figure 32, the motor drives a tachometer that generates an ac voltage proportional to RPM. This voltage is rectified, filtered, divided down by the speed set potentiometer, and applied to Pin. 8. The motor will accelerate until $V_{Pin\ 3}$ is equal to V_1 at which time Pin 14 will go to a high state and terminate the motor drive. The motor will now coast until $V_{Pin\ 3}$ is less than V_4 where upon drive is then reapplied. The system operation of Figure 31 is identical to that of 32 except the signal at Pin 3 is an amplified average of the motors drive and back EMF voltages. Both systems exhibit excellent control of RPM with variations of V_{CC}; however, Figure 32 has somewhat better torque characteristics at low RPM.

Figure 18. Timing Diagram

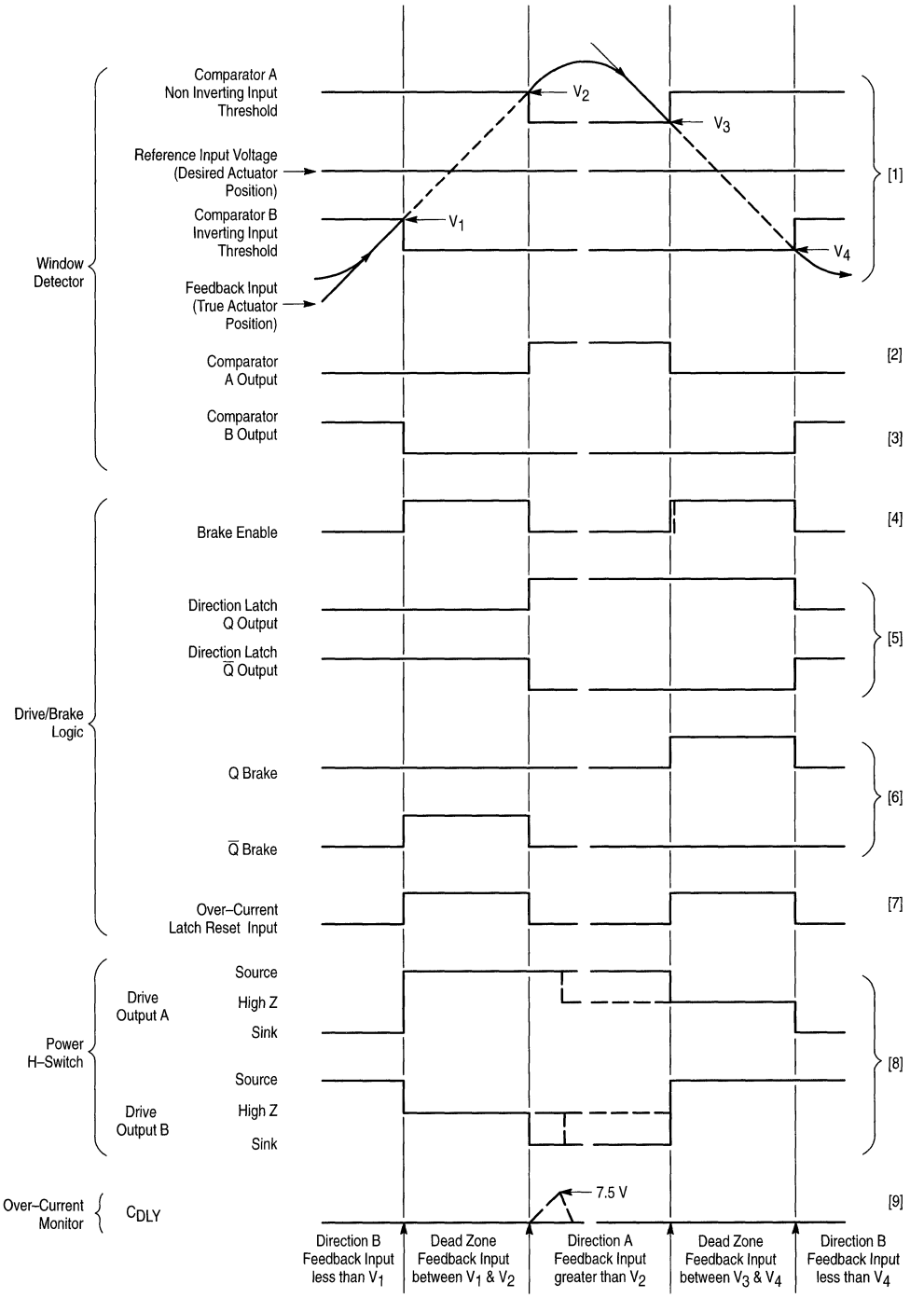


Figure 19. Solar Tracking Servo System

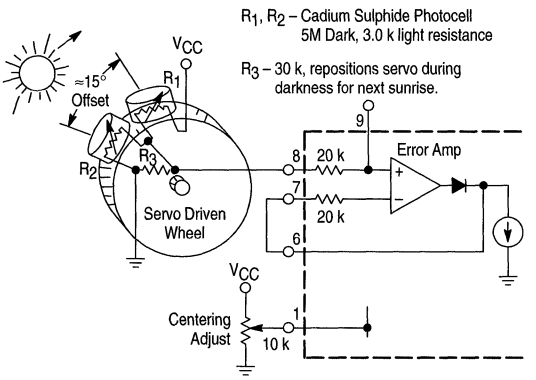
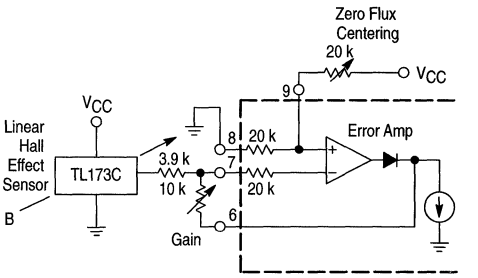
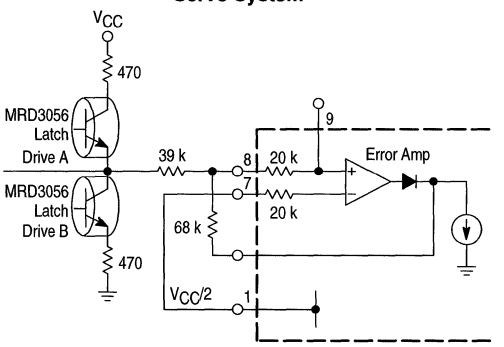


Figure 20. Magnetic Sensing Servo System



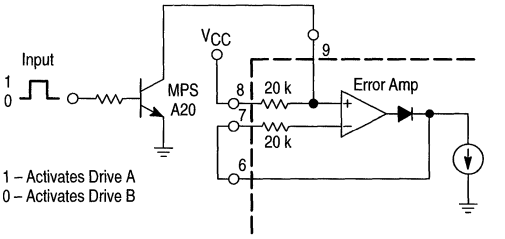
Typical sensitivity with gain set at 3.9 k is 1.5 mV/gauss.
Servo motor controls magnetic field about sensor.

Figure 21. Infrared Latched Two Position Servo System



Over–current monitor (not shown) shuts down
servo when end stop is reached.

Figure 22. Digital Two Position Servo System



Over–current monitor (not shown) shuts down
servo when end stop is reached.

Figure 23. 0.25 Hz Square–Wave Servo Agitator

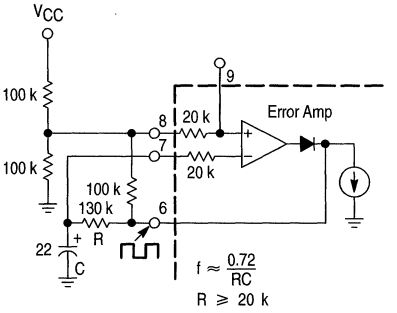
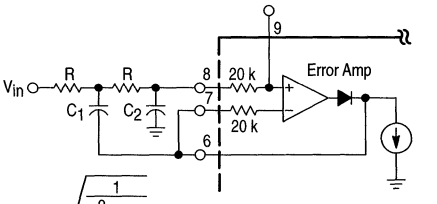


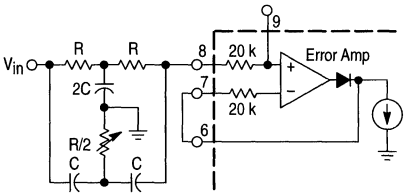
Figure 24. Second Order Low–Pass Active Filter



$$f_o = \frac{\sqrt{\frac{1}{R^2 C_1 C_2}}}{2\pi}$$

$$Q = \frac{\sqrt{\frac{C_1}{C_2}}}{2}$$

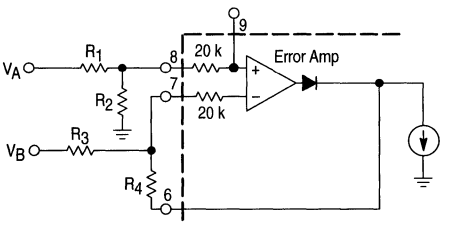
Figure 25. Notch Filter



$$f_{notch} = \frac{1}{2\pi RC}$$

For 60 Hz R = 53.6 k, C = 0.05

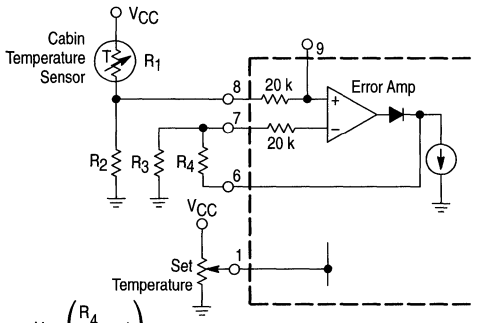
Figure 26. Differential Input Amplifier



$$V_{Pin\ 6} = V_A\left(\frac{R_3 + R_4}{R_1 + R_2}\right)\frac{R_2}{R_3} - \left(\frac{R_4}{R_3}\ V_B\right)$$

4

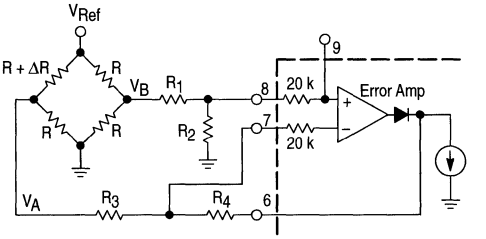
Figure 27. Temperature Sensing Servo System



$$V_{Pin\ 6} = \frac{V_{CC}\left(\frac{R_4}{R_3} + 1\right)}{\left(\frac{R_1}{R_2} + 1\right)}$$

In this application the servo motor drives the heat/air conditioner modulator door in a duct system.

Figure 28. Bridge Amplifier

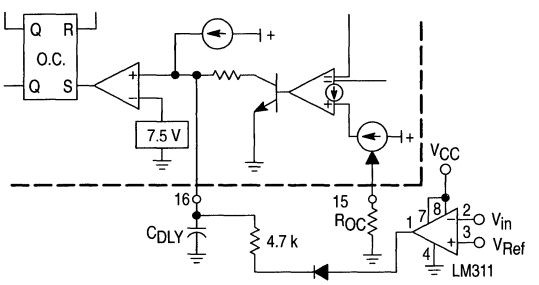


$$V_A - V_B = V_{Ref}\left(\frac{\Delta R}{4R + 2\Delta R}\right)$$

$$R_1 = R_3,\ R_2 = R_4,\ R_1 >> R$$

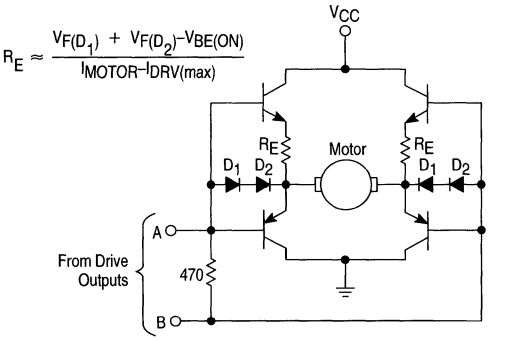
$$V_{Pin\ 6} = \frac{R_4}{R_3}\ (V_A - V_B)$$

Figure 29. Remote Latched Shutdown



A direction change signal is required at Pins 2 or 3 to reset the over–current latch.

Figure 30. Power H–Switch Buffer



$$R_E \approx \frac{V_{F(D_1)} + V_{F(D_2)} - V_{BE(ON)}}{I_{MOTOR} - I_{DRV(max)}}$$

This circuit maintains the brake and over–current features of the MC33030. Set R_{OC} to 15 k for $I_{DRV(max)} \approx 0.5$ A.

Figure 31. Adjustable Pressure Differential Regulator

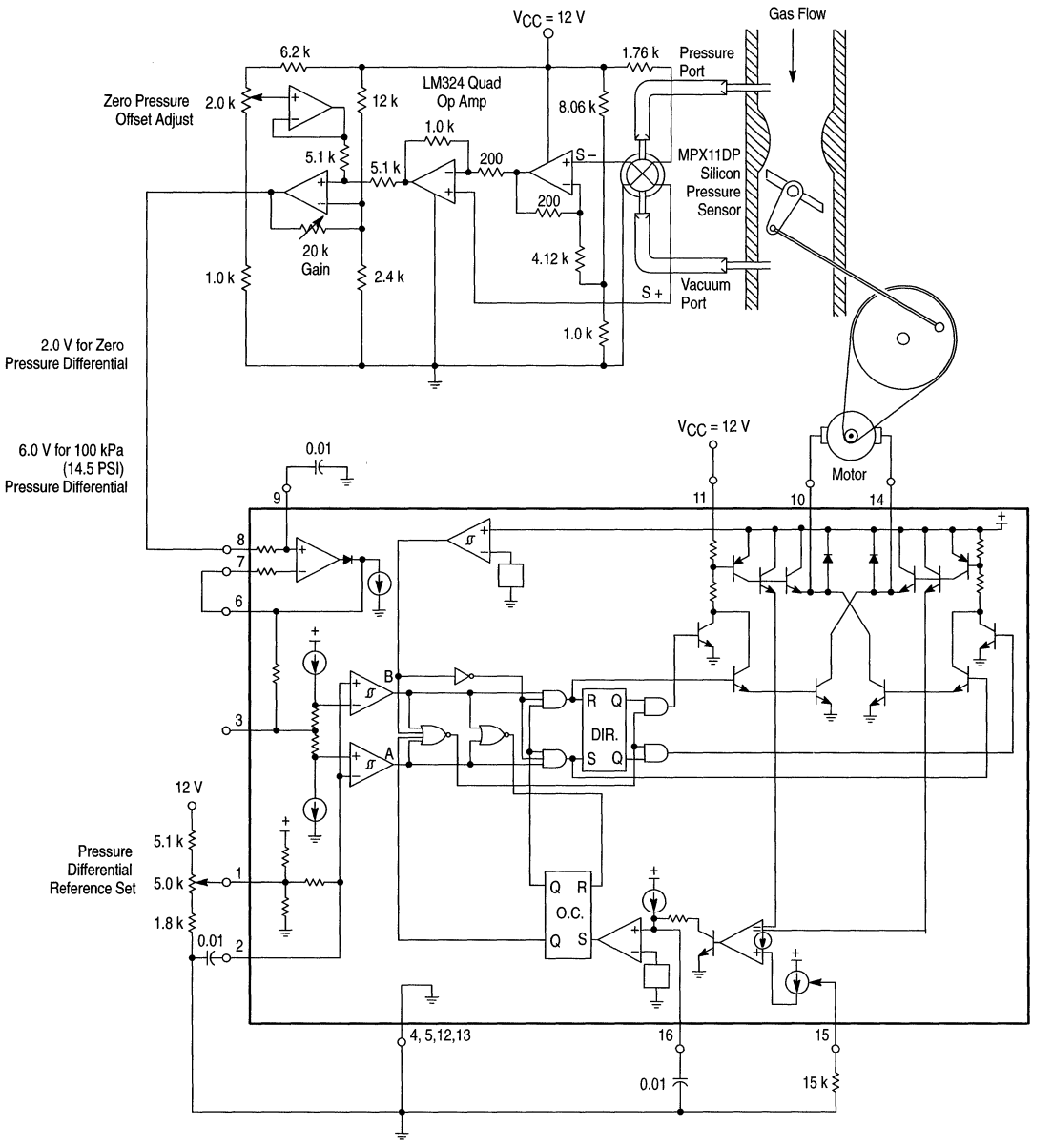
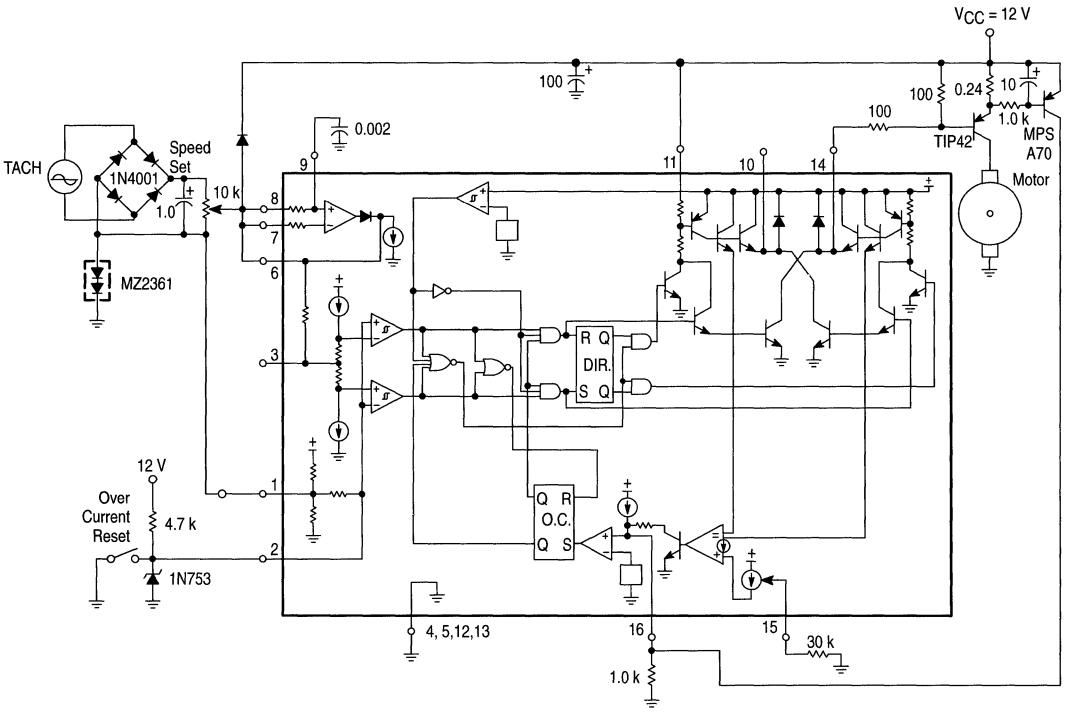
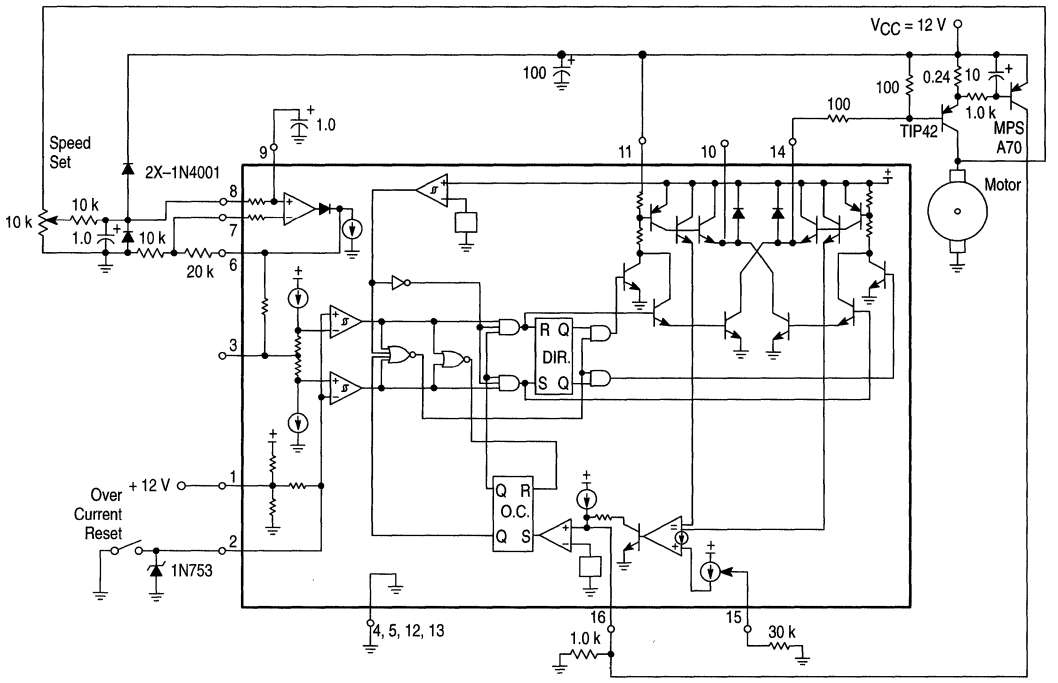


Figure 32. Switching Motor Controller With Buffered Output and Tach Feedback



4

Figure 33. Switching Motor Controller With Buffered Output and Back EMF Sensing



MOTOROLA

MC33033

Brushless DC Motor Controller

The MC33033 is a high performance second generation, limited feature, monolithic brushless dc motor controller which has evolved from Motorola's full featured MC33034 and MC33035 controllers. It contains all of the active functions required for the implementation of open loop, three or four phase motor control. The device consists of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs. Unlike its predessors, it does not feature separate drive circuit supply and ground pins, brake input, or fault output signal.

Included in the MC33033 are protective features consisting of undervoltage lockout, cycle–by–cycle current limiting with a selectable time delayed latched shutdown mode, and internal thermal shutdown.

Typical motor control functions include open loop speed, forward or reverse direction, and run enable.The MC33033 is designed to operate brushless motors with electrical sensor phasings of 60°/300° or 120°/240°, and can also efficiently control brush dc motors.

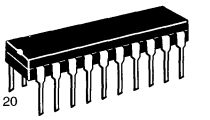
- 10 to 30 V Operation
- Undervoltage Lockout
- 6.25 V Reference Capable of Supplying Sensor Power
- Fully Accessible Error Amplifier for Closed Loop Servo Applications
- High Current Drivers Can Control External 3–Phase MOSFET Bridge
- Cycle–By–Cycle Current Limiting
- Internal Thermal Shutdown
- Selectable 60°/300° or 120°/240° Sensor Phasings
- Also Efficiently Control Brush DC Motors with External MOSFET H–Bridge

ORDERING INFORMATION

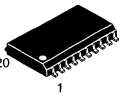
Device	Operating Temperature Range	Package
MC33033DW	$T_A = -40°$ to $+85°C$	SO–20L
MC33033P		Plastic DIP

BRUSHLESS DC MOTOR CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

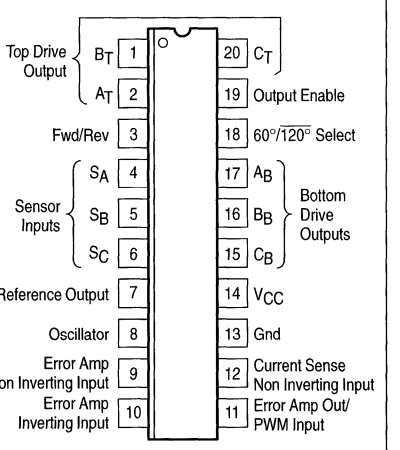


P SUFFIX
PLASTIC PACKAGE
CASE 738



DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

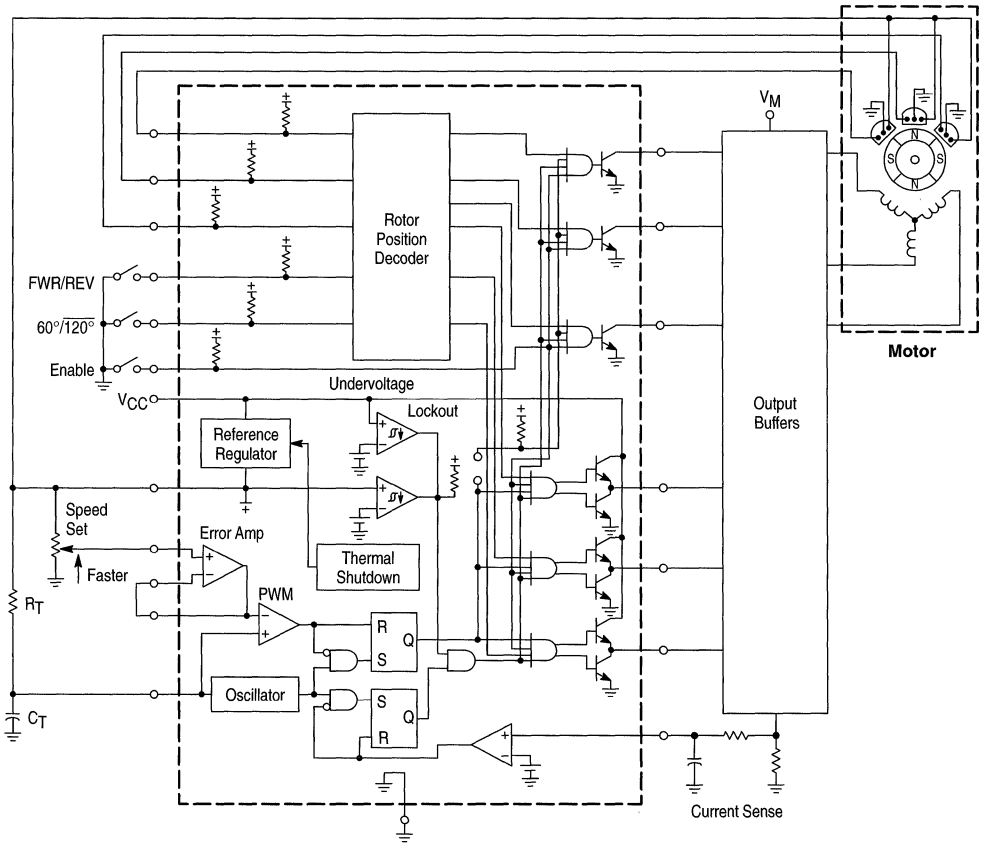
PIN CONNECTIONS



(Top View)

4

Representative Schematic Diagram



This device contains 266 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	30	V
Digital Inputs (Pins 3, 4, 5, 6, 18, 19)	–	V_{ref}	V
Oscillator Input Current (Source or Sink)	I_{OSC}	30	mA
Error Amp Input Voltage Range (Pins 9, 10, Note 1)	V_{IR}	−0.3 to V_{ref}	V
Error Amp Output Current (Source or Sink, Note 2)	I_{Out}	10	mA
Current Sense Input Voltage Range	V_{Sense}	−0.3 to 5.0	V
Top Drive Voltage (Pins 1, 2, 20)	$V_{CE(top)}$	40	V
Top Drive Sink Current (Pins 1, 2, 20)	$I_{Sink(top)}$	50	mA
Bottom Drive Output Current (Source or Sink, Pins 15,16, 17)	I_{DRV}	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Dual–In–Line, Case 738			
Maximum Power Dissipation @ T_A = 85°C	P_D	867	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	75	°C/W
DW Suffix, Surface Mount, Case 751D			
Maximum Power Dissipation @ T_A = 85°C	P_D	619	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	105	°C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_{ref} = 1.0 mA)	V_{ref}				V
T_A = 25°C		5.9	6.24	6.5	
T_A = −40° to + 85°C		5.82	–	6.57	
Line Regulation (V_{CC} = 10 V to 30 V, I_{ref} = 1.0 mA)	Reg_{line}	–	1.5	30	mV
Load Regulation (I_{ref} = 1.0 mA to 20 mA)	Reg_{load}	–	16	30	mV
Output Short–Circuit Current (Note 3)	I_{SC}	40	75	–	mA
Reference Under Voltage Lockout Threshold	V_{th}	4.0	4.5	5.0	V
ERROR AMPLIFIER					
Input Offset Voltage (T_A = −40° to + 85°C)	V_{IO}	–	0.4	10	mV
Input Offset Current (T_A = −40° to + 85°C)	I_{IO}	–	8.0	500	nA
Input Bias Current (T_A = −40° to + 85°C)	I_{IB}	–	−46	−1000	nA
Input Common Mode Voltage Range	V_{ICR}		(0 V to V_{ref})		V
Open Loop Voltage Gain (V_O = 3.0 V, R_L = 15 k)	A_{VOL}	70	80	–	dB
Input Common Mode Rejection Ratio	CMRR	55	86	–	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 30 V)	PSRR	65	105	–	dB
Output Voltage Swing					V
High State (R_L = 15 k to Gnd)	V_{OH}	4.6	5.3	–	
Low State (R_L = 17 k to V_{ref})	V_{OL}	–	0.5	1.0	

NOTES: 1. The input common mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V.
2. The compliance voltage must not exceed the range of −0.3 to V_{ref}.
3. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Oscillator Frequency	f_{OSC}	22	25	28	kHz
Frequency Change with Voltage (V_{CC} = 10 V to 30 V)	$\Delta f_{OSC}/\Delta V$	–	0.01	5.0	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	–	4.1	4.5	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	1.2	1.5	–	V
LOGIC INPUTS					
Input Threshold Voltage (Pins 3, 4, 5, 6, 18, 19) High State Low State	 V_{IH} V_{IL}	 3.0 –	 2.2 1.7	 – 0.8	V
Sensor Inputs (Pins 4, 5, 6) High State Input Current (V_{IH} = 5.0 V) Low State Input Current (V_{IL} = 0 V)	 I_{IH} I_{IL}	 –150 –600	 –70 –337	 –20 –150	µA
Forward/Reverse, 60°/120° Select and Output Enable (Pins 3, 18, 19) High State Input Current (V_{IH} = 5.0 V) Low State Input Current (V_{IL} = 0 V)	 I_{IH} I_{IL}	 –75 –300	 –36 –175	 –10 –75	µA
CURRENT–LIMIT COMPARATOR					
Threshold Voltage	V_{th}	85	101	115	mV
Input Common Mode Voltage Range	V_{ICR}	–	3.0	–	V
Input Bias Current	I_{IB}	–	–0.9	–5.0	µA
OUTPUTS AND POWER SECTIONS					
Top Drive Output Sink Saturation (I_{Sink} = 25 mA)	$V_{CE(sat)}$	–	0.5	1.5	V
Top Drive Output Off–State Leakage (V_{CE} = 30 V)	$I_{DRV(leak)}$	–	0.06	100	µA
Top Drive Output Switching Time (C_L = 47 pF, R_L = 1.0 k) Rise Time Fall Time	 t_r t_f	 – –	 107 26	 300 300	ns
Bottom Drive Output Voltage High State (V_{CC} = 30 V, I_{source} = 50 mA) Low State (V_{CC} = 30 V, I_{sink} = 50 mA)	 V_{OH} V_{OL}	 (V_{CC} – 2.0) –	 (V_{CC} – 1.1) 1.5	 – 2.0	V
Bottom Drive Output Switching Time (C_L = 1000 pF) Rise Time Fall Time	 t_r t_f	 – –	 38 30	 200 200	ns
Under Voltage Lockout Drive Output Enabled (V_{CC} Increasing) Hysteresis	 $V_{th(on)}$ V_H	 8.2 0.1	 8.9 0.2	 10 0.3	V
Power Supply Current	I_{CC}	–	15	22	mA

Figure 1. Oscillator Frequency versus Timing Resistor

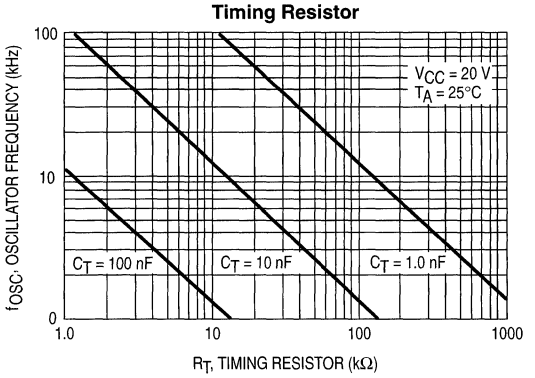
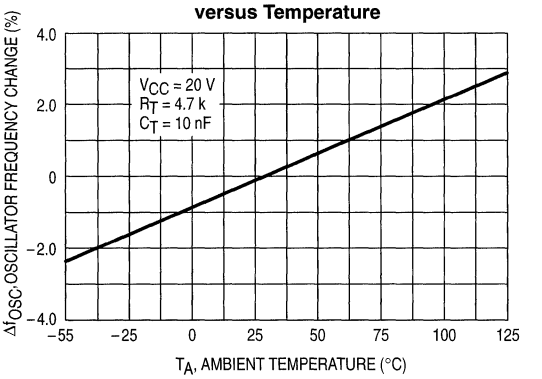


Figure 2. Oscillator Frequency Change versus Temperature



4

Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

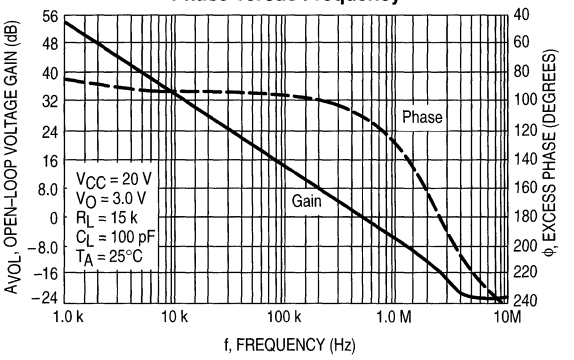


Figure 4. Error Amp Output Saturation Voltage versus Load Current

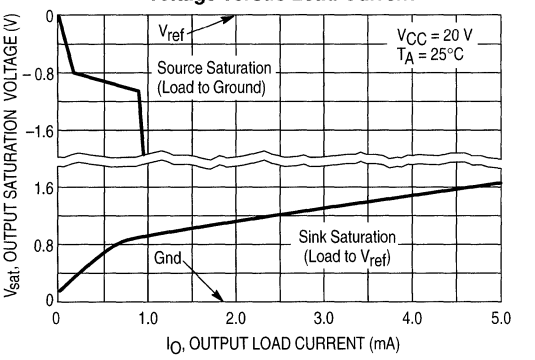


Figure 5. Error Amp Small–Signal Transient Response

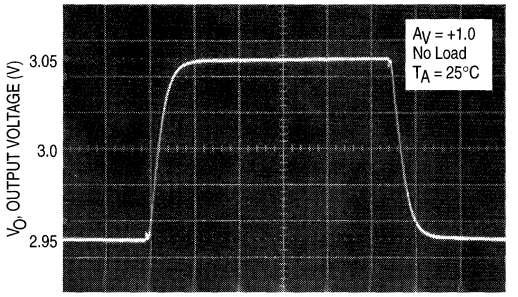


Figure 6. Error Amp Large–Signal Transient Response

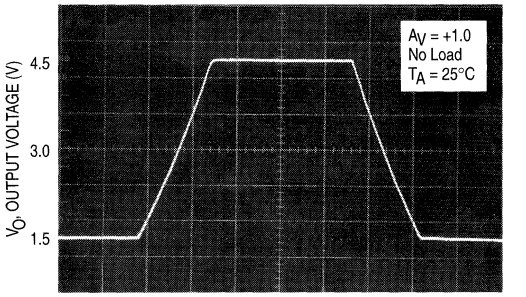


Figure 7. Reference Output Voltage Change versus Output Source Current

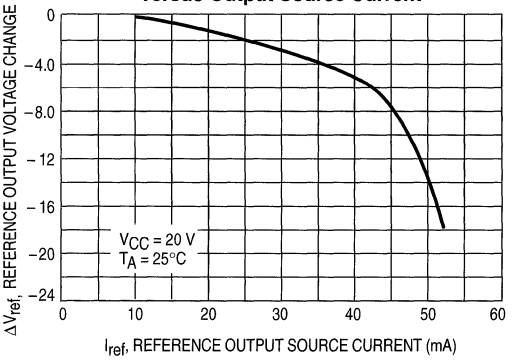


Figure 8. Reference Output Voltage versus Supply Voltage

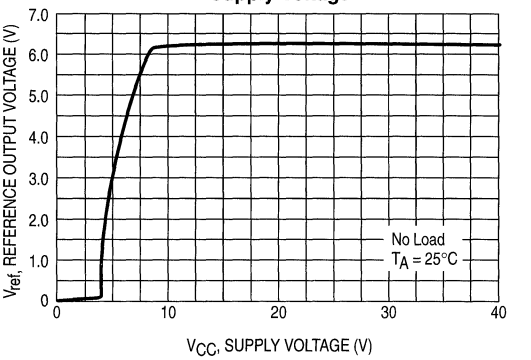


Figure 9. Reference Output Voltage versus Temperature

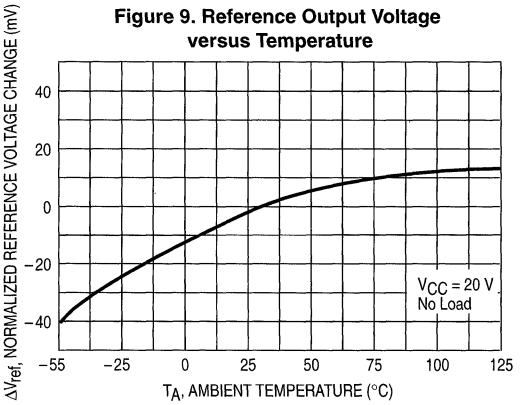


Figure 10. Output Duty Cycle versus PWM Input Voltage

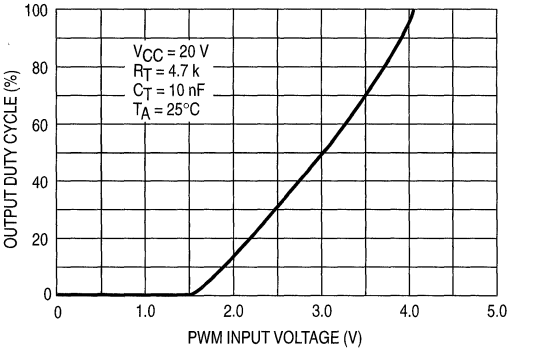


Figure 11. Bottom Drive Response Time versus Current Sense Input Voltage

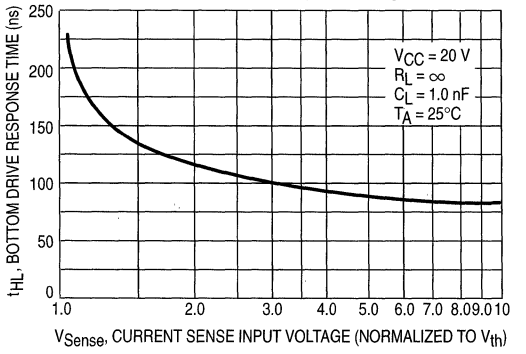


Figure 12. Top Drive Output Saturation Voltage versus Sink Current

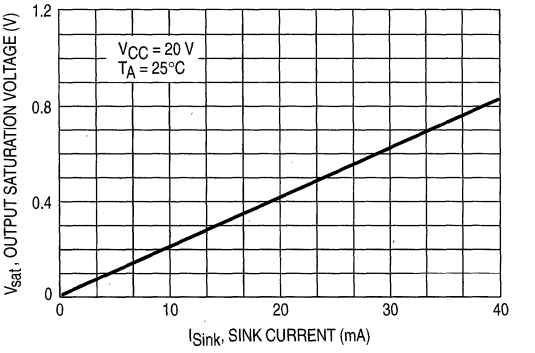


Figure 13. Top Drive Output Waveform

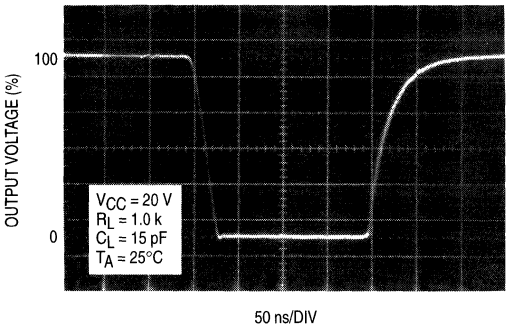


Figure 14. Bottom Drive Output Waveform

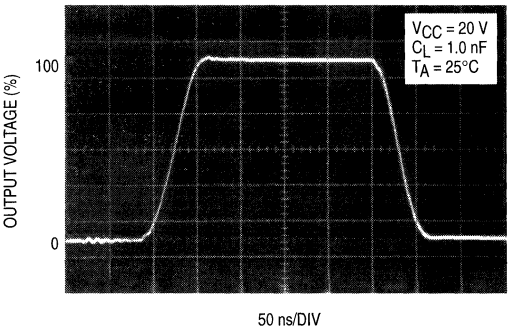


Figure 15. Bottom Drive Output Waveform

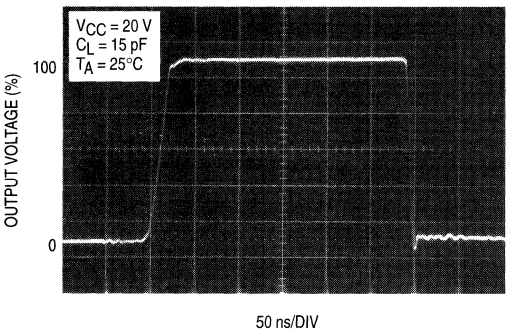


Figure 16. Bottom Drive Output Saturation Voltage versus Load Current

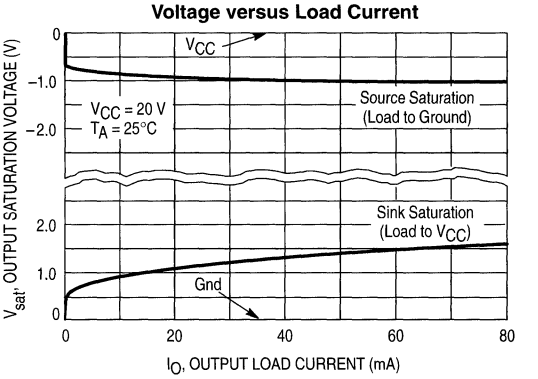
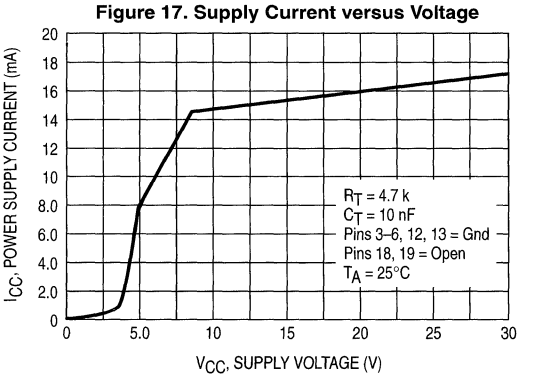


Figure 17. Supply Current versus Voltage



4

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1, 2, 20	B_T, A_T, C_T	These three open collector Top Drive Outputs are designed to drive the external upper power switch transistors.
3	Fwd//Rev	The Forward/Reverse Input is used to change the direction of motor rotation.
4, 5, 6	S_A, S_B, S_C	These three Sensor Inputs control the commutation sequence.
7	Reference Output	This output provides charging current for the oscillator timing capacitor C_T and a reference for the Error Amplifier. It may also serve to furnish sensor power.
8	Oscillator	The Oscillator frequency is programmed by the values selected for the timing components, R_T and C_T.
9	Error Amp Noninverting Input	This input is normally connected to the speed set potentiometer.
10	Error Amp Inverting Input	This input is normally connected to the Error Amp Output in open loop applications.
11	Error Amp Out/PWM Input	This pin is available for compensation in closed loop applications.
12	Current Sense Noninverting Input	A 100 mV signal, with respect to Pin 13, at this input terminates output switch conduction during a given oscillator cycle. This pin normally connects to the top side of the current sense resistor.
13	Gnd	This pin supplies a separate ground return for the control circuit and should be referenced back to the power source ground.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a V_{CC} range of 10 to 30 V.
15, 16, 17	C_B, B_B, A_B	These three totem pole Bottom Drive Outputs are designed for direct drive of the external bottom power switch transistors.
18	60°/$\overline{120°}$ Select	The electrical state of this pin configures the control circuit operation for either 60° (high state) or 120° (low state) sensor electrical phasing inputs.
19	Output Enable	A logic high at this input causes the motor to run, while a low causes it to coast.

INTRODUCTION

The MC33033 is one of a series of high performance monolithic dc brushless motor controllers produced by Motorola. It contains all of the functions required to implement a limited–feature, open loop, three or four phase motor control system. Constructed with Bipolar Analog technology, it offers a high degree of performance and ruggedness in hostile industrial environments.The MC33033 contains a rotor position decoder for proper commutation sequencing, a temperature compensated reference capable of supplying sensor power, a frequency programmable sawtooth oscillator, a fully accessible error amplifier, a pulse width modulator comparator, three open collector top drive outputs, and three high current totem pole bottom driver outputs ideally suited for driving power MOSFETs.

Included in the MC33033 are protective features consisting of undervoltage lockout, cycle–by–cycle current limiting with a latched shutdown mode, and internal thermal shutdown.

Typical motor control functions include open loop speed control, forward or reverse rotation, and run enable. In addition, the MC33033 has a 60°/$\overline{120°}$ select pin which configures the rotor position decoder for either 60° or 120° sensor electrical phasing inputs.

FUNCTIONAL DESCRIPTION

A representative internal block diagram is shown in Figure 18, with various applications shown in Figures 34, 36, 37, 41, 43, and 44. A discussion of the features and function of each of the internal blocks given below and referenced to Figures 18 and 36.

Rotor Position Decoder

An internal rotor position decoder monitors the three sensor inputs (Pins 4, 5, 6) to provide the proper sequencing of the top and bottom drive outputs. The Sensor Inputs are designed to interface directly with open collector type Hall Effect switches or opto slotted couplers. Internal pull–up resistors are included to minimize the required number of external components. The inputs are TTL compatible, with their thresholds typically at 2.2 V. The MC33033 series is designed to control three phase motors and operate with four of the most common conventions of sensor phasing. A 60°/$\overline{120°}$ Select (Pin 18) is conveniently provided which affords the MC33033 to configure itself to control motors having either 60°, 120°, 240° or 300° electrical sensor phasing. With three Sensor Inputs there are eight possible input code combinations, six of which are valid rotor positions. The remaining two codes are invalid and are usually caused by an open or shorted sensor line. With six valid input codes, the decoder can resolve the motor rotor position to within a window of 60 electrical degrees.

The Forward/Reverse input (Pin 3) is used to change the direction of motor rotation by reversing the voltage across the stator winding. When the input changes state, from high to low with a given sensor input code (for example 100), the enabled top and bottom drive outputs with the same alpha designation are exchanged (A_T to A_B, B_T to B_B, C_T to C_B). In effect the commutation sequence is reversed and the motor changes directional rotation.

Motor on/off control is accomplished by the Output Enable (Pin19). When left disconnected, an internal pull–up resistor to a positive source enables sequencing of the top and bottom drive outputs. When grounded, the Top Drive Outputs turn off and the bottom drives are forced low, causing the motor to coast.

The commutation logic truth table is shown in Figure 19. In half wave motor drive applications, the Top Drive Outputs are not required and are typically left disconnected.

Error Amplifier

A high performance, fully compensated Error Amplifier with access to both inputs and output (Pins 9, 10, 11) is provided to facilitate the implementation of closed loop motor speed control. The amplifier features a typical dc voltage gain of 80 dB, 0.6 MHz gain bandwidth, and a wide input common mode voltage range that extends from ground to V_{ref}. In most open loop speed control applications, the amplifier is configured as a unity gain voltage follower with the Noninverting Input connected to the speed set voltage source. Additional configurations are shown in Figures 29 through 33.

Oscillator

The frequency of the internal ramp oscillator is programmed by the values selected for timing components R_T and C_T. Capacitor C_T is charged from the Reference Output (Pin 7) through resistor R_T and discharged by an internal discharge transistor. The ramp peak and valley voltages are typically 4.1 V and 1.5 V respectively. To provide a good compromise between audible noise and output switching efficiency, an oscillator frequency in the range of 20 to 30 kHz is recommended. Refer to Figure 1 for component selection.

Pulse Width Modulator

The use of pulse width modulation provides an energy efficient method of controlling the motor speed by varying the average voltage applied to each stator winding during the commutation sequence. As C_T discharges, the oscillator sets both latches, allowing conduction of the Top and Bottom Drive Outputs. The PWM comparator resets the upper latch, terminating the Bottom Drive Output conduction when the positive–going ramp of C_T becomes greater than the Error Amplifier output. The pulse width modulator timing diagram is shown in Figure 20. Pulse width modulation for speed control appears only at the Bottom Drive Outputs.

Current Limit

Continuous operation of a motor that is severely over–loaded results in overheating and eventual failure. This destructive condition can best be prevented with the use of cycle–by–cycle current limiting. That is, each on–cycle is treated as a separate event. Cycle–by–cycle current limiting is accomplished by monitoring the stator current build–up each time an output switch conducts, and upon sensing an over current condition, immediately turning off the switch and holding it off for the remaining duration of

Figure 18. Representative Block Diagram

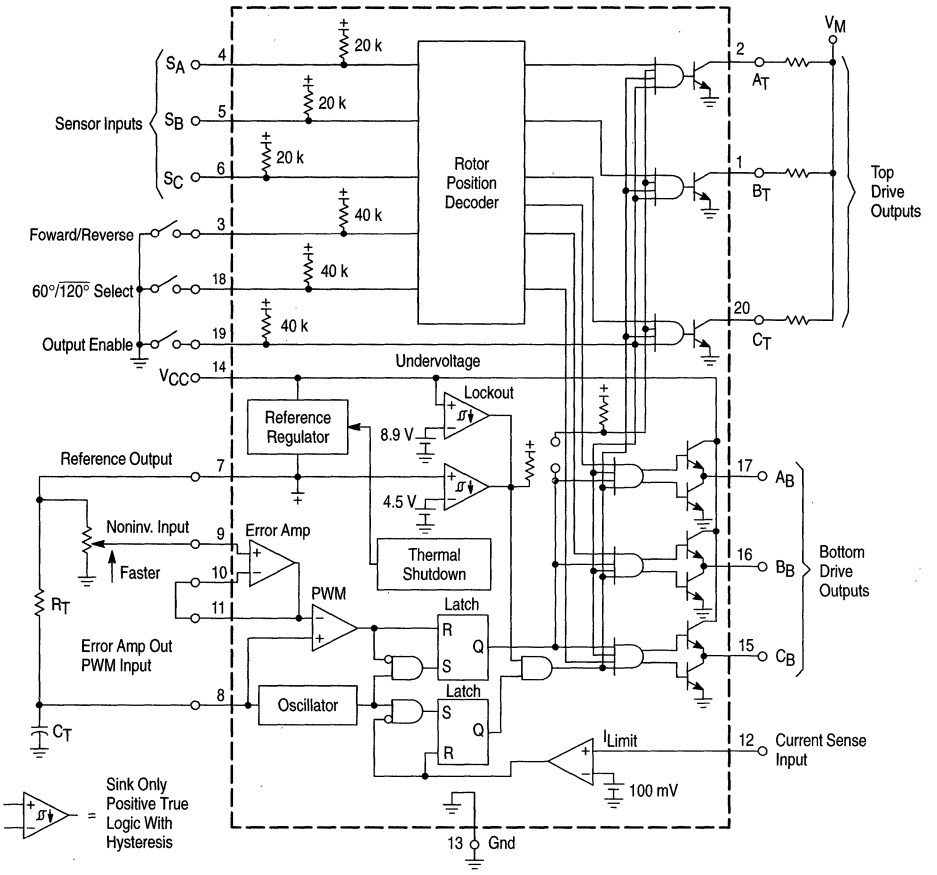


Figure 19. Three Phase, Six Step Commutation Truth Table (Note 1)

Inputs (Note 2)									Outputs (Note 3)						
Sensor Electrical Phasing (Note 4)									Top Drives			Bottom Drives			
60°			120°					Current							
S_A	S_B	S_C	S_A	S_B	S_C	F/R	Enable	Sense	A_T	B_T	C_T	A_B	B_B	C_B	
1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	(Note 5)
1	1	0	1	1	0	1	1	0	1	0	1	0	0	1	F/R = 1
1	1	1	0	1	0	1	1	0	1	0	1	1	0	0	
0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	
0	0	1	0	0	1	1	1	0	1	1	0	0	1	0	
0	0	0	1	0	1	1	1	0	0	1	1	0	1	0	
1	0	0	1	0	0	0	1	0	1	1	0	1	0	0	(Note 5)
1	1	0	1	1	0	0	1	0	1	1	0	0	1	0	F/R = 0
1	1	1	0	1	0	0	1	0	0	1	1	0	1	0	
0	1	1	0	1	1	0	1	0	0	1	1	0	0	1	
0	0	1	0	0	1	0	1	0	1	0	1	0	0	1	
0	0	0	1	0	1	0	1	0	1	0	1	1	0	0	
1	0	1	1	1	1	X	X	X	1	1	1	0	0	0	(Note 6)
0	1	0	0	0	0	X	X	X	1	1	1	0	0	0	
V	V	V	V	V	V	X	0	X	1	1	1	0	0	0	(Note 7)
V	V	V	V	V	V	X	1	1	1	1	1	0	0	0	(Note 8)

NOTES: 1. V = Any one of six valid sensor or drive combinations.
X = Don't care.
2. The digital inputs (Pins 3, 4, 5, 6, 18, 19) are all TTL compatible. The current sense input (Pin 12) has a 100 mV threshold with respect to Pin 13. A logic 0 for this input is defined as < 85 mV, and a logic 1 is > 115 mV.
3. The top drive outputs are open collector design and active in the low (0) state.
4. With 60°/120° (Pin 18) in the high (1) state, configuration is for 60° sensor electrical phasing inputs. With Pin 18 in the low (0) state, configuration is for 120° sensor electrical phasing inputs.
5. Valid 60° or 120° sensor combinations for corresponding valid top and bottom drive outputs.
6. Invalid sensor inputs; All top and bottom drives are off.
7. Valid sensor inputs with enable = 0; All top and bottom drives are off.
8. Valid sensor inputs with enable and current sense = 1; All top and bottom drives are off.

oscillator ramp–up period. The stator current is converted to a voltage by inserting a ground–referenced sense resistor R_S (Figure 34) in series with the three bottom switch transistors (Q_4, Q_5, Q_6). The voltage developed across the sense resistor is monitored by the current sense input (Pin 12), and compared to the internal 100 mV reference. If the current sense threshold is exceeded, the comparator resets the lower latch and terminates output switch conduction. The value for the sense resistor is:

$$R_S = \frac{0.1}{I_{stator(max)}}$$

The dual–latch PWM configuration ensures that only one single output conduction pulse occurs during any given oscillator cycle, whether terminated by the output of the Error Amplifier or the current limit comparator.

Reference

The on–chip 6.25 V regulator (Pin 7) provides charging current for the oscillator timing capacitor, a reference for the Error Amplifier, and can supply 20 mA of current suitable for directly powering sensors in low voltage applications. In higher voltage applications it may become necessary to transfer the power dissipated by the regulator off the IC. This is easily accomplished with the addition of an external pass transistor as shown in Figure 21. A 6.25 V reference level was chosen to allow implementation of the simpler NPN circuit, where $V_{ref} - V_{BE}$ exceeds the minimum voltage required by Hall Effect sensors over temperature. With proper transistor selection, and adequate heatsinking, up to one amp of load current can be obtained.

Undervoltage Lockout

A dual Undervoltage Lockout has been incorporated to prevent damage to the IC and the external power switch transistors. Under low power supply conditions, it guarantees that the IC and sensors are fully functional, and that there is sufficient Bottom Drive Output voltage. The positive power supply to the IC (V_{CC}) is monitored to a threshold of 8.9 V. This level ensures sufficient gate drive necessary to attain low $R_{DS(on)}$ when interfacing with standard power MOSFET devices. When directly powering the Hall sensors from the reference, improper sensor operation can result if the reference output voltage should fall below 4.5 V. If one or both of the comparators detects an undervoltage condition, the top drives are turned off and the Bottom Drive Outputs are held in a low state. Each of the comparators contain hysteresis to prevent oscillations when crossing their respective thresholds.

Figure 20. PWM Timing Diagram

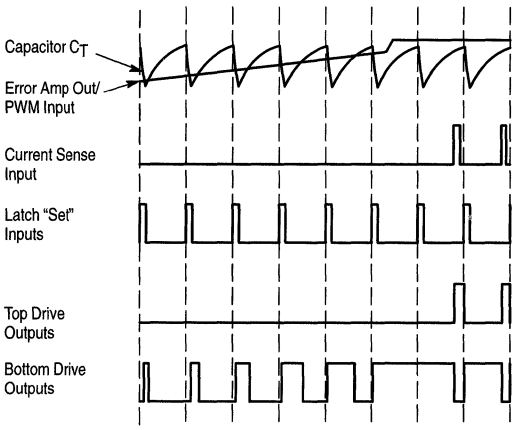
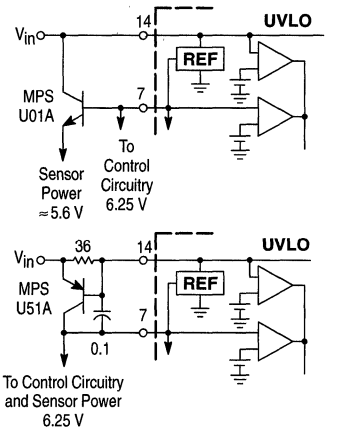
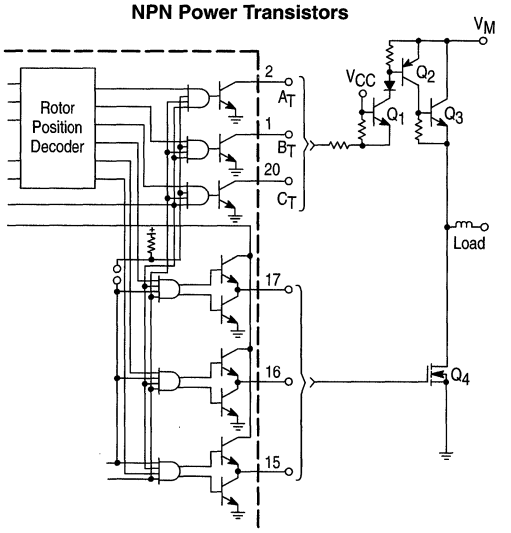


Figure 21. Reference Output Buffers



The NPN circuit is recommended for powering Hall or opto sensors, where the output voltage temperature coefficient is not critical. The PNP circuit is slightly more complex, but also more accurate. Neither circuit has current limiting.

Figure 22. High Voltage Interface with NPN Power Transistors



Transistor Q_1 is a common base stage used to level shift from V_{CC} to the high motor voltage, V_M. The collector diode is required if V_{CC} is present while V_M is low.

Figure 23. High Voltage Interface with N–Channel Power MOSFETs

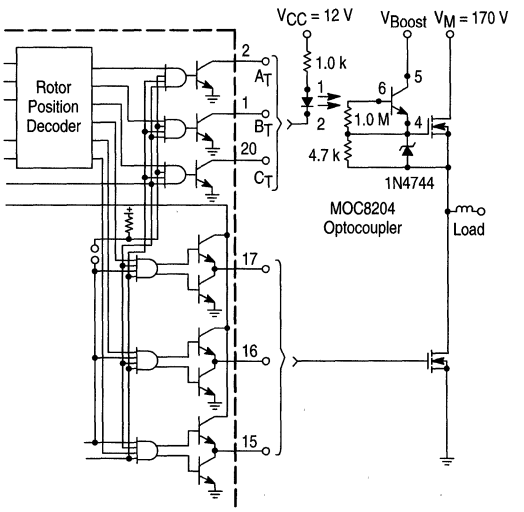
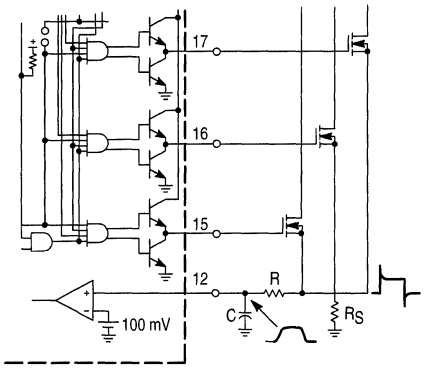
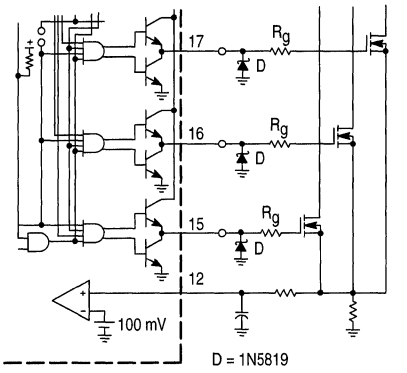


Figure 24. Current Waveform Spike Suppression



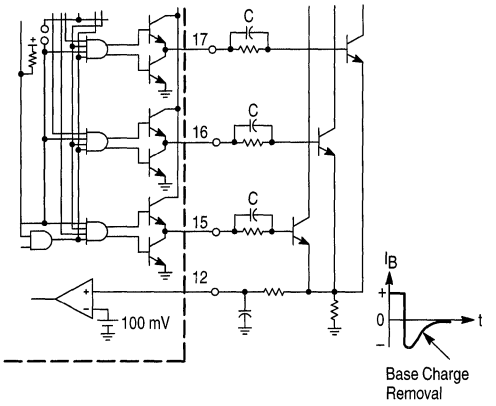
The addition of the RC filter will eliminate current–limit instability caused by the leading edge spike on the current waveform. Resistor R_S should be a low inductance type.

Figure 25. MOSFET Drive Precautions



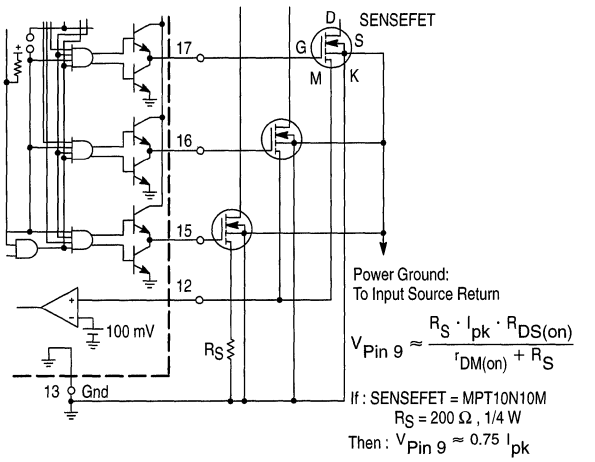
Series gate resistor R_g will damp any high frequency oscillations caused by the MOSFET input capacitance and any series wiring induction in the gate–source circuit. Diode D is required if the negative current into the Bottom Drive Outputs exceeds 50 mA.

Figure 26. Bipolar Transistor Drive



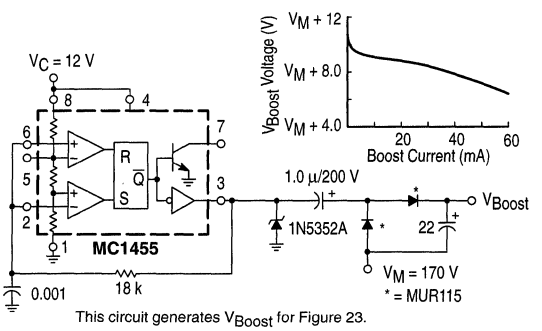
The totem pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C.

Figure 27. Current Sensing Power MOSFETs



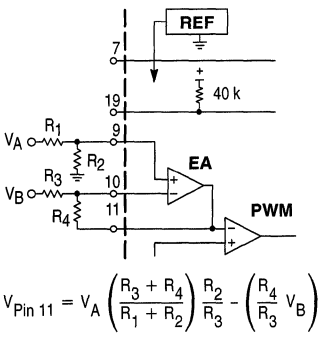
Virtually lossless current sensing can be achieved with the implementation of SENSEFET power switches.

Figure 28. High Voltage Boost Supply



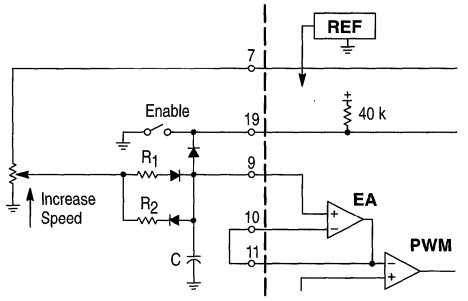
This circuit generates V_{Boost} for Figure 23.

Figure 29. Differential Input Speed Controller



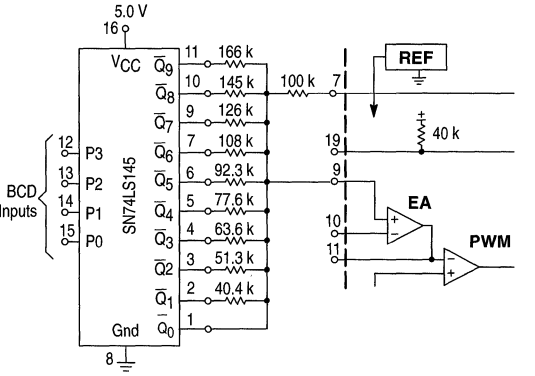
$$V_{Pin\ 11} = V_A \left(\frac{R_3 + R_4}{R_1 + R_2}\right)\frac{R_2}{R_3} - \left(\frac{R_4}{R_3} V_B\right)$$

Figure 30. Controlled Acceleration/Deceleration



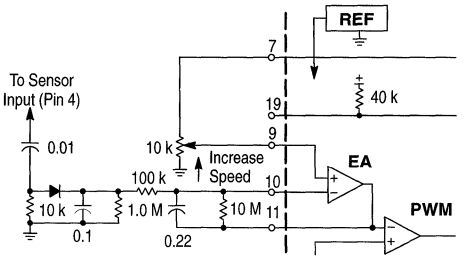
Resistor R_1 with capacitor C sets the acceleration time constant while R_2 controls the deceleration. The values of R_1 and R_2 should be at least ten times greater than the speed set potentiometer to minimize time constant variations with different speed settings.

Figure 31. Digital Speed Controller



The SN74LS145 is an open collector BCD to One of Ten decoder. When connected as shown, input codes 0000 through 1001 steps the PWM in increments of approximately 10% from 0 to 90% on–time. Input codes 1010 through 1111 will produce 100% on–time or full motor speed.

Figure 32. Closed Loop Speed Control



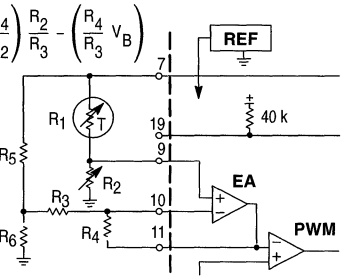
The rotor position sensors can be used as a tachometer. By differentiating the positive–going edges and then integrating them over time, a voltage proportional to speed can be generated. The error amp compares this voltage to that of the speed set to control the PWM.

Figure 33. Closed Loop Temperature Control

$$V_{Pin\ 11} = V_{ref}\left(\frac{R_3 + R_4}{R_1 + R_2}\right)\frac{R_2}{R_3} - \left(\frac{R_4}{R_3}\,V_B\right)$$

$$V_B = \frac{V_{ref}}{\left(\frac{R_5}{R_6} + 1\right)}$$

$$R_3 >> R_6 \parallel R_6$$



This circuit can control the speed of a cooling fan proportional to the difference between the sensor and set temperatures. The control loop is closed as the forced air cools the NTC thermistor. For controlled heating applications, exchange the positions of R_1 and R_2.

Drive Outputs

The three Top Drive Outputs (Pins 1, 2, 20) are open collector NPN transistors capable of sinking 50 mA with a minimum breakdown of 30 V. Interfacing into higher voltage applications is easily accomplished with the circuits shown in Figures 22 and 23.

The three totem pole Bottom Drive Outputs (Pins 15, 16, 17) are particularly suited for direct drive of N–Channel MOSFETs or NPN bipolar transistors (Figures 24, 25, 26, and 27). Each output is capable of sourcing and sinking up to 100 mA.

Thermal Shutdown

Internal thermal shutdown circuity is provided to protect the IC in the event the maximum junction temperature is exceeded. When activated, typically at 170°C, the IC acts as though the regulator was disabled, in turn shutting down the IC.

SYSTEM APPLICATIONS

Three Phase Motor Commutation

The three phase application shown in Figure 34 is an open loop motor controller with full wave, six step drive. The upper power switch transistors are Darlington PNPs while the lower switches are N–Channel power MOSFETs. Each of these devices contains an internal parasitic catch diode that is used to return the stator inductive energy back to the power supply. The outputs are capable of driving a delta or wye connected stator, and a grounded neutral wye if split supplies are used. At any given rotor position, only one top and one bottom power switch (of different totem poles) is enabled. This configuration switches both ends of the stator winding from supply to ground which causes the current flow to be bidirectional or full wave. A leading edge spike is usually present on the current waveform and can cause a current–limit error. The spike can be eliminated by adding an RC filter in series with the Current Sense Input. Using a low inductance type resistor for R_S will also aid in spike reduction. Figure 35 shows the commutation waveforms over two electrical cycles. The first cycle (0° to 360°) depicts motor operation at full speed while the second cycle (360° to 720°) shows a reduced speed with about 50% pulse width modulation. The current waveforms reflect a constant torque load and are shown synchronous to the commutation frequency for clarity.

Figure 34. Three Phase, Six Step, Full Wave Motor Controller

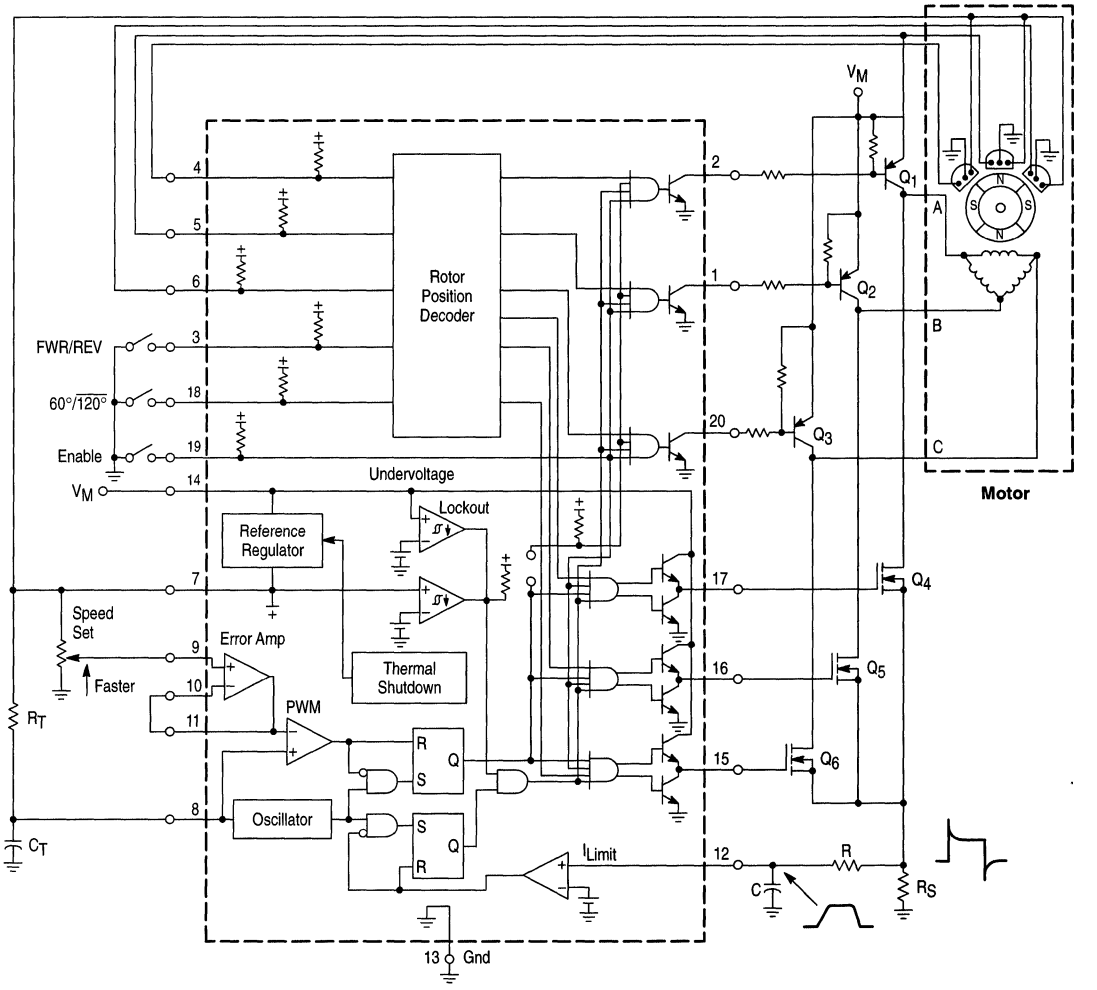


Figure 35. Three Phase, Six Step, Full Wave Commutation Waveforms

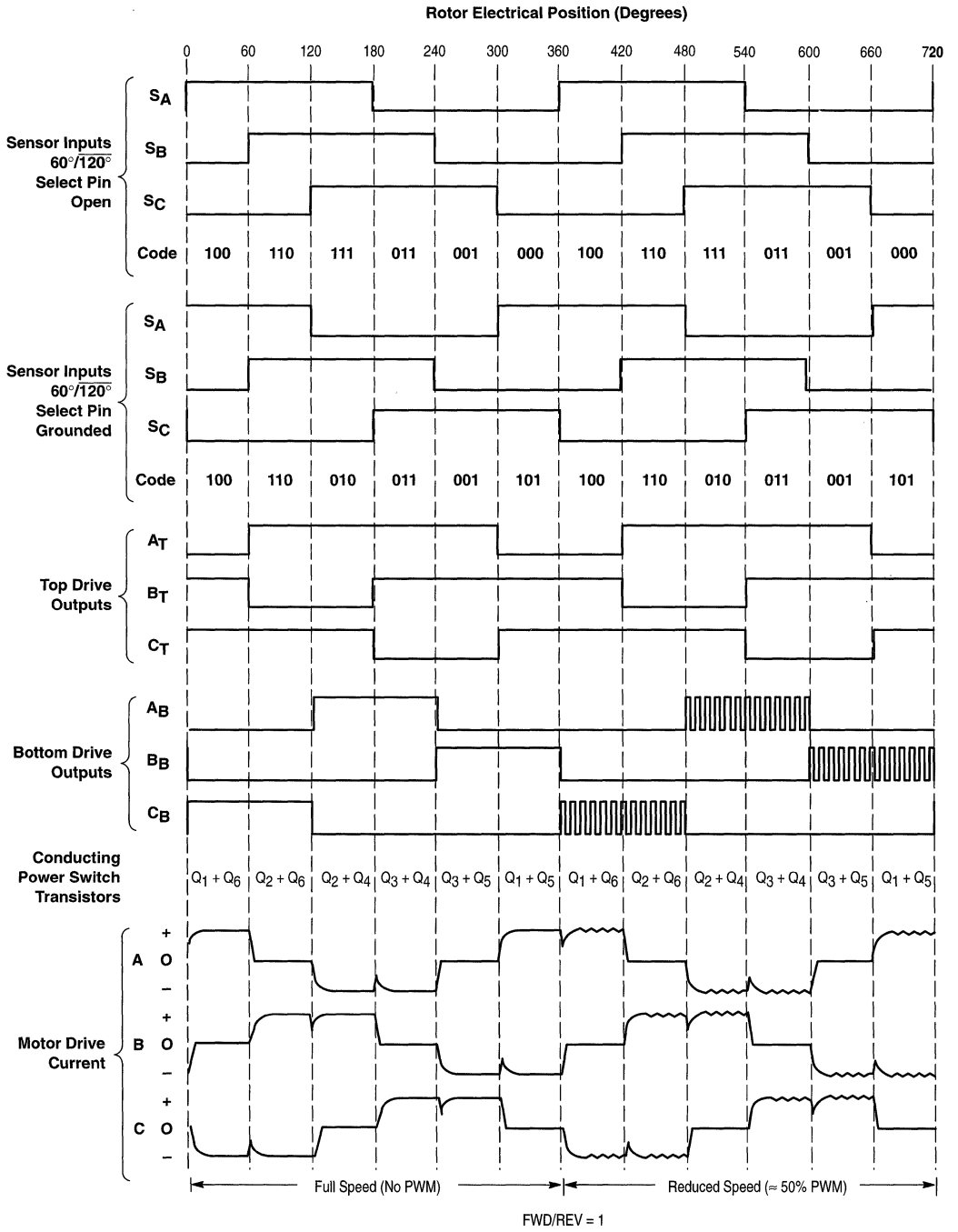
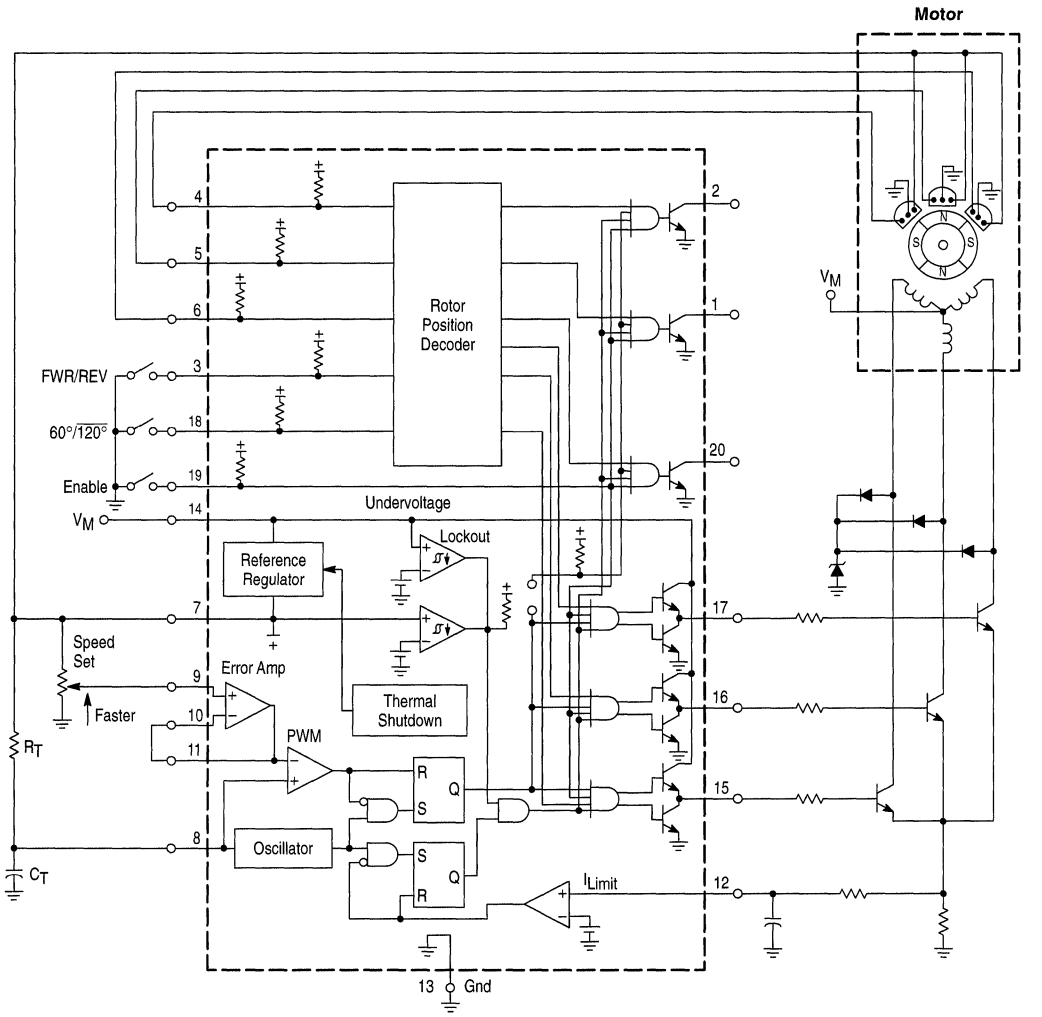


Figure 36 shows a three phase, three step, half wave motor controller. This configuration is ideally suited for automobile and other low voltage applications since there is only one power switch voltage drop in series with a given stator winding. Current flow is unidirectional or half wave because only one end of each winding is switched. The stator flyback voltage is clamped by a single zener and three diodes.

Figure 36. Three Phase, Three Step, Half Wave Motor Controller

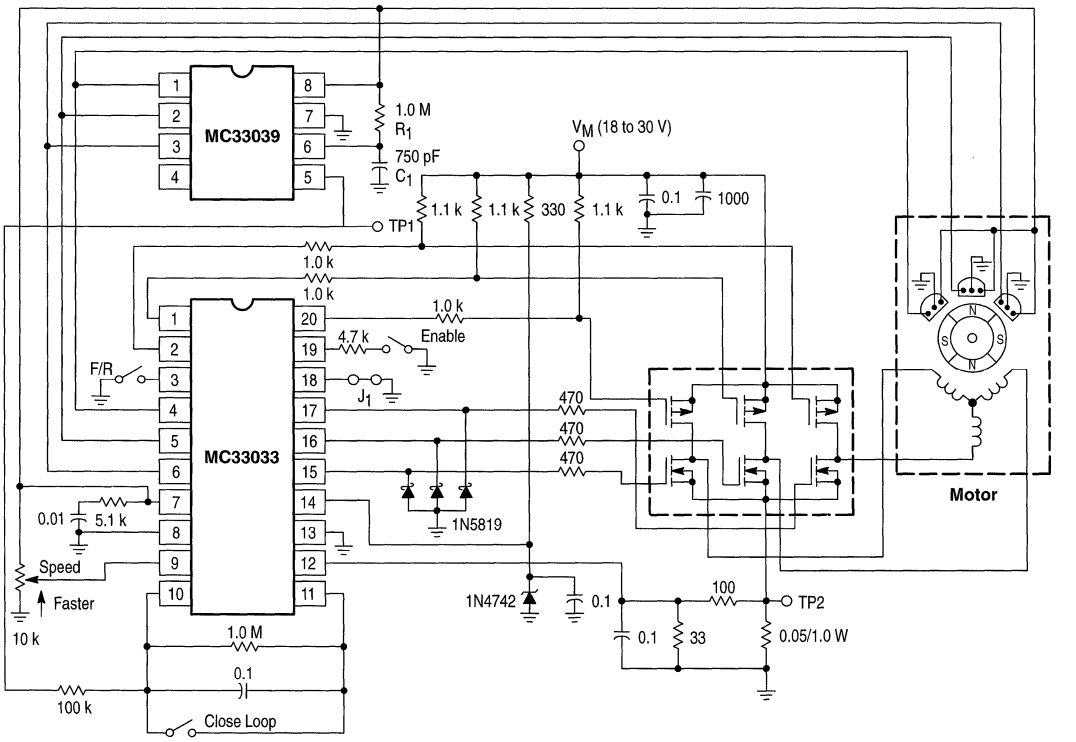


Three Phase Closed Loop Controller

The MC33033, by itself, is capable of open loop motor speed control. For closed loop speed control, the MC33033 requires an input voltage proportional to the motor speed. Traditionally this has been accomplished by means of a tachometer to generate the motor speed feedback voltage. Figure 37 shows an application whereby an MC33039, powered from the 6.25 V reference (Pin 7) of the MC33033, is used to generate the required feedback voltage without the need of a costly tachometer. The same Hall sensor signals used by the MC33033 for rotor position decoding are utilized by the MC33039. Every positive or negative going transition of the Hall sensor signals on any of the sensor lines causes the MC33039 to produce an output pulse of defined amplitude and time duration, as determined by the external resistor R_1 and capacitor C_1. The resulting output train of pulses present at Pin 5 of the MC33039 are integrated by the Error Amplifier of the MC33033 configured as an integrator, to produce a dc voltage level which is proportional to the motor speed. This speed proportional voltage establishes the PWM reference level at Pin 11 of the MC33033 motor controller and completes or closes the feedback loop. The MC33033 ouputs drive a TMOS power MOSFET 3–phase bridge. High current can be expected during conditions of start–up and when changing direction of the motor.

The system shown in Figure 37 is designed for a motor having 120/240 degrees Hall sensor electrical phasing. The system can easily be modified to accommodate 60/300 degree Hall sensor electrical phasing by removing the jumper (J_1) at Pin 18 of the MC33033.

Figure 37. Closed Loop Brushless DC Motor Control With the MC33033 Using the MC33039



Sensor Phasing Comparison

There are four conventions used to establish the relative phasing of the sensor signals in three phase motors. With six step drive, an input signal change must occur every 60 electrical degrees, however, the relative signal phasing is dependent upon the mechanical sensor placement. A comparison of the conventions in electrical degrees is shown in Figure 38. From the sensor phasing table (Figure 39), note that the order of input codes for 60° phasing is the reverse of 300°. This means the MC33033, when the 60°/$\overline{120°}$ select (Pin 18) and the FWD/REV (Pin 3) both in the high state (open), is configured to operate a 60° sensor phasing motor in the forward direction. Under the same conditions a 300° sensor phasing motor would operate equally well but in the reverse direction. One would simply have to reverse the FWD/REV switch (FWD/REV closed) in order to cause the 300° motor to also operate in the same direction. The same difference exists between the 120° and 240° conventions.

Figure 38. Sensor Phasing Comparison

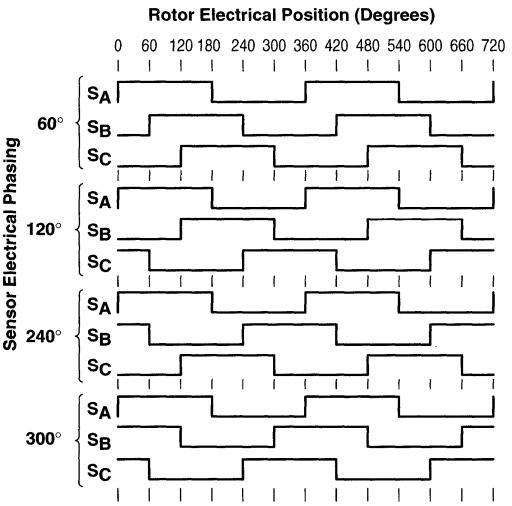


Figure 39. Sensor Phasing Table

Sensor Electrical Phasing (Degrees)												
60°			120°			240°			300°			
S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C
1	0	0	1	0	1	1	1	0	1	1	1
1	1	0	1	0	0	1	0	0	1	1	0
1	1	1	1	1	0	1	0	1	1	0	0
0	1	1	0	1	0	0	0	1	0	0	0
0	0	1	0	1	1	0	1	1	0	0	1
0	0	0	0	0	1	0	1	0	0	1	1

In this data sheet, the rotor position has always been given in electrical degrees since the mechanical position is a function of the number of rotating magnetic poles. The relationship between the electrical and mechanical position is:

$$\text{Electrical Degrees} = \text{Mechanical Degrees}\left(\frac{\#\text{Rotor Poles}}{2}\right)$$

An increase in the number of magnetic poles causes more electrical revolutions for a given mechanical revolution. General purpose three phase motors typically contain a four pole rotor which yields two electrical revolutions for one mechanical.

Two and Four Phase Motor Commutation

The MC33033 configured for 60° sensor inputs is capable of providing a four step output that can be used to drive two or four phase motors. The truth table in Figure 40 shows that by connecting sensor inputs S_B and S_C together, it is possible to truncate the number of drive output states from six to four. The output power switches are connected to B_T, C_T, B_B, and C_B. Figure 41 shows a four phase, four step, full wave motor control application. Power switch transistors Q_1 through Q_8 are Darlington type, each with an internal parasitic catch diode. With four step drive, only two rotor position sensors spaced at 90 electrical degrees are required. The commutation waveforms are shown in Figure 42.

Figure 43 shows a four phase, four step, half wave motor controller. It has the same features as the circuit in Figure 36, except for the deletion of speed adjust.

Figure 40. Two and Four Phase, Four Step, Commutation Truth Table

MC33033 (60°/$\overline{120°}$ Select Pin Open)						
Inputs			Outputs			
Sensor Electrical Spacing* = 90°			Top Drives		Bottom Drives	
S_A	S_B	F/R	B_T	C_T	B_B	C_B
1	0	1	1	1	0	1
1	1	1	0	1	0	0
0	1	1	1	0	0	0
0	0	1	1	1	1	0
1	0	0	1	0	0	0
1	1	0	1	1	1	0
0	1	0	1	1	0	1
0	0	0	0	1	0	0

*With MC33033 sensor input S_B connected to S_C

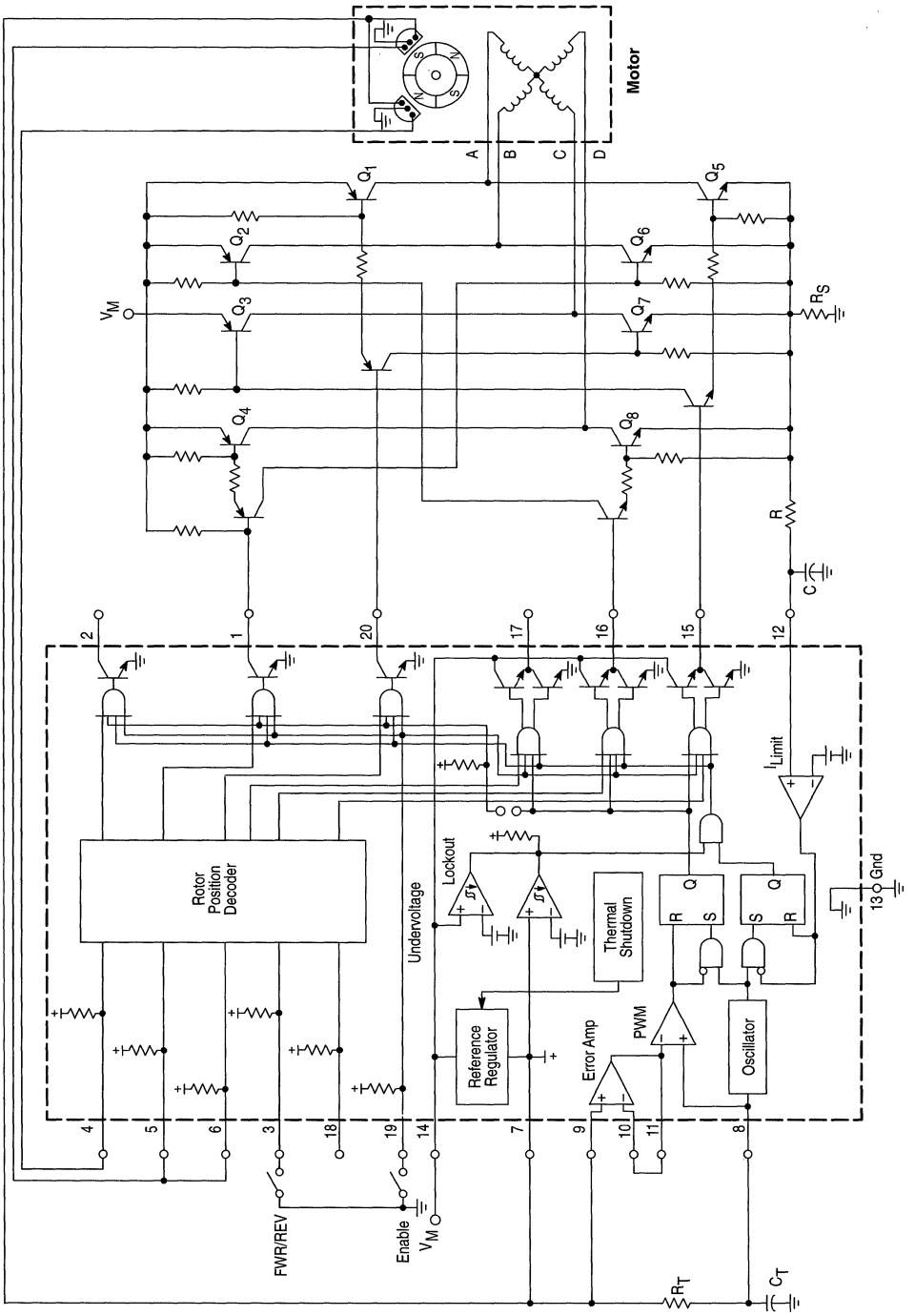
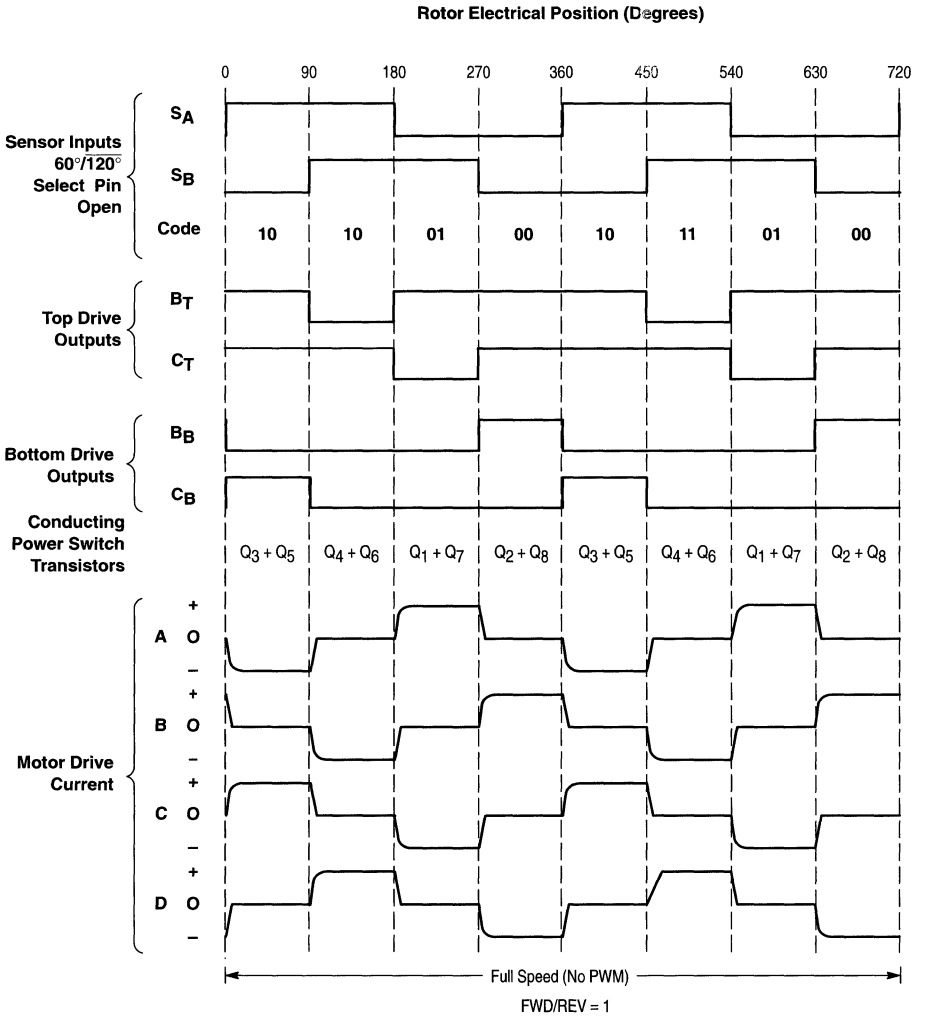


Figure 41. Four Phase, Four Step, Full Wave Controller

Figure 42. Four Phase, Four Step, Full Wave Commutation Waveforms



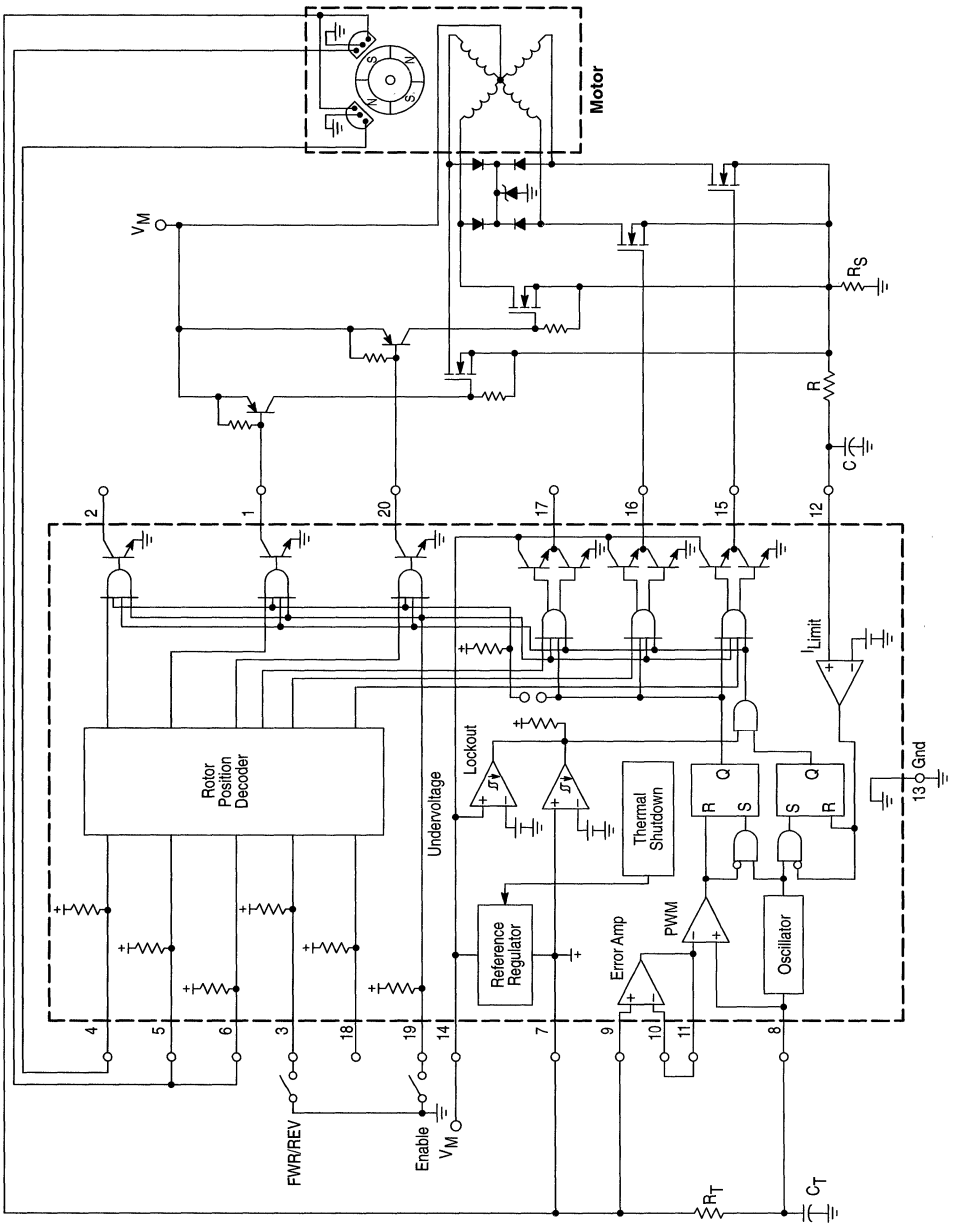


Figure 43. Four Phase, Four Step, Half Wave Motor Controller

Brush Motor Control

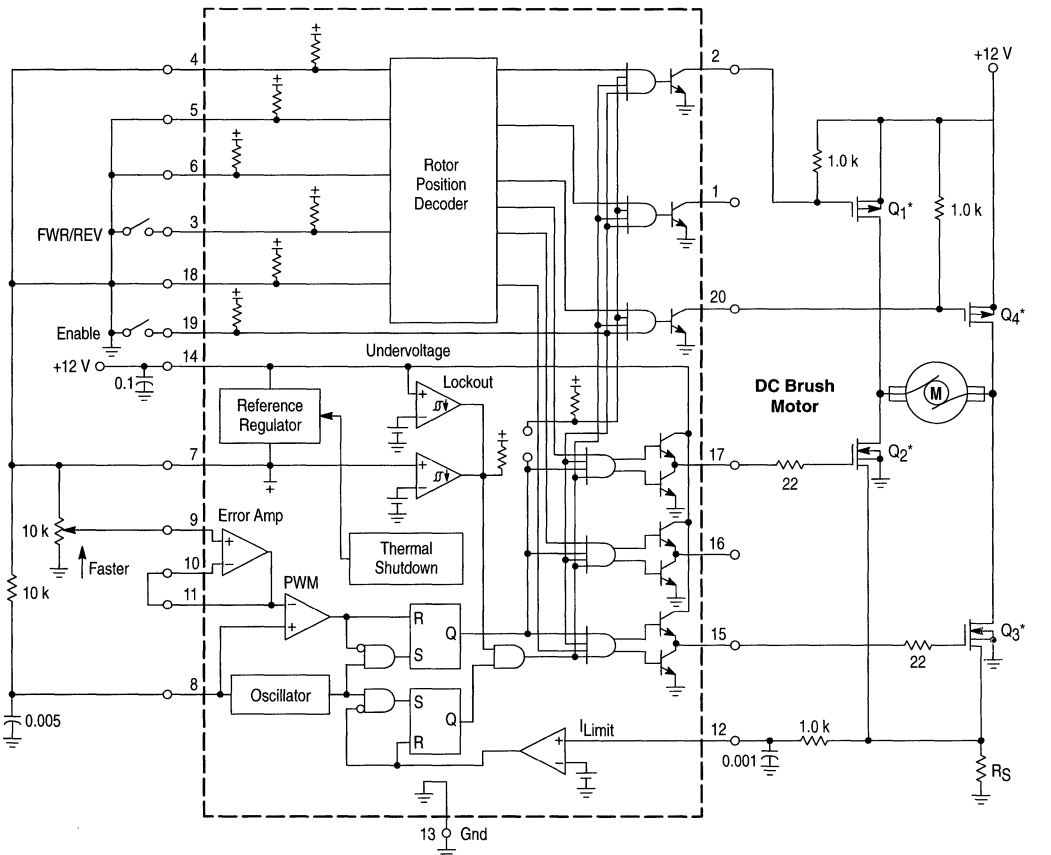
Though the MC33033 was designed to control brushless dc motors, it may also be used to control dc brush–type motors. Figure 44 shows an application of the MC33033 driving a H–bridge affording minimal parts count to operate a brush–type motor. Key to the operation is the input sensor code [100] which produces a top–left (Q_1) and a bottom–right (Q_3) drive when the controller's Forward/Reverse pin is at logic [1]; top–right (Q_4), bottom–left (Q_2) drive is realized when the Forward/Reverse pin is at logic [0]. This code supports the requirements necessary for H–bridge drive accomplishing both direction and speed control.

The controller functions in a normal manner with a pulse width modulated frequency of approximately 25 kHz. Motor speed is controlled by adjusting the voltage presented to the noninverting input of the Error Amplifier establishing the PWM's slice or reference level. Cycle–by–cycle current limiting of the motor current is accomplished by sensing the voltage (100 mV threshold) across the R_S resistor to ground of the H–bridge motor current. The over current sense circuit makes it possible to reverse the direction of the motor, on the fly, using the normal Forward/Reverse switch, and not have to completely stop before reversing.

LAYOUT CONSIDERATIONS

Do not attempt to construct any of the motor control circuits on wire–wrap or plug–in prototype boards. High frequency printed circuit layout techniques are imperative to prevent pulse jitter. This is usually caused by excessive noise pick–up imposed on the current sense or error amp inputs. The printed circuit layout should contain a ground plane with low current signal and high drive and output buffer grounds returning on separate paths back to the power supply input filter capacitor V_M. Ceramic bypass capacitors (0.01 μF) connected close to the integrated circuit at V_{CC}, V_{ref} and error ampliflier noninverting input may be required depending upon circuit layout. This provides a low impedance path for filtering any high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI.

Figure 44. H–Bridge Brush–Type Controller



MC33035

Brushless DC Motor Controller

The MC33035 is a high performance second generation monolithic brushless DC motor controller containing all of the active functions required to implement a full featured open loop, three or four phase motor control system. This device consists of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs.

Also included are protective features consisting of undervoltage lockout, cycle–by–cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique fault output that can be interfaced into microprocessor controlled systems.

Typical motor control functions include open loop speed, forward or reverse direction, run enable, and dynamic braking. The MC33035 is designed to operate with electrical sensor phasings of 60°/300° or 120°/240°, and can also efficiently control brush DC motors.

- 10 to 30 V Operation
- Undervoltage Lockout
- 6.25 V Reference Capable of Supplying Sensor Power
- Fully Accessible Error Amplifier for Closed Loop Servo Applications
- High Current Drivers Can Control External 3–Phase MOSFET Bridge
- Cycle–By–Cycle Current Limiting
- Pinned–Out Current Sense Reference
- Internal Thermal Shutdown
- Selectable 60°/300° or 120°/240° Sensor Phasings
- Can Efficiently Control Brush DC Motors with External MOSFET H–Bridge

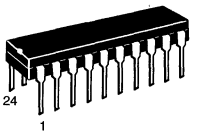
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33035DW	$T_A = -40°$ to $+85°C$	SO–24L
MC33035P		Plastic DIP

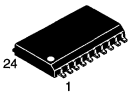
BRUSHLESS DC MOTOR CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

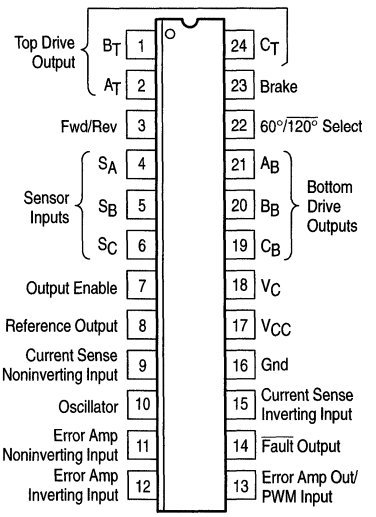
P SUFFIX
PLASTIC PACKAGE
CASE 724



DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

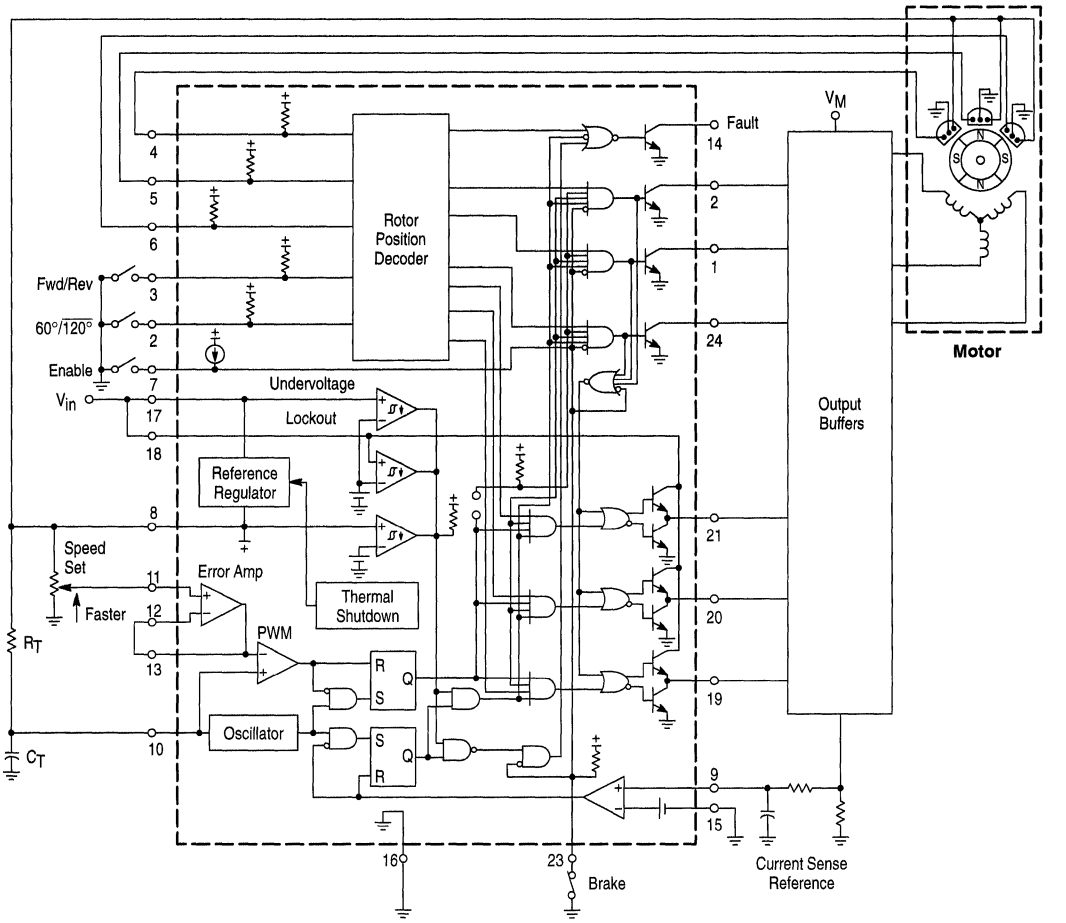


PIN CONNECTIONS



(Top View)

Representative Schematic Diagram



This device contains 285 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Digital Inputs (Pins 3, 4, 5, 6, 22, 23)	–	V_{ref}	V
Oscillator Input Current (Source or Sink)	I_{OSC}	30	mA
Error Amp Input Voltage Range (Pins 11, 12, Note 1)	V_{IR}	−0.3 to V_{ref}	V
Error Amp Output Current (Source or Sink, Note 2)	I_{Out}	10	mA
Current Sense Input Voltage Range (Pins 9, 15)	V_{Sense}	−0.3 to 5.0	V
$\overline{\text{Fault}}$ Output Voltage	$V_{CE(\overline{Fault})}$	20	V
$\overline{\text{Fault}}$ Output Sink Current	$I_{Sink(\overline{Fault})}$	20	mA
Top Drive Voltage (Pins 1, 2, 24)	$V_{CE(top)}$	40	V
Top Drive Sink Current (Pins 1, 2, 24)	$I_{Sink(top)}$	50	mA
Bottom Drive Supply Voltage (Pin 18)	V_C	30	V
Bottom Drive Output Current (Source or Sink, Pins 19, 20, 21)	I_{DRV}	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Dual In Line, Case 724			
Maximum Power Dissipation @ T_A = 85°C	P_D	867	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	75	°C/W
DW Suffix, Surface Mount, Case 751E			
Maximum Power Dissipation @ T_A = 85°C	P_D	650	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = V_C = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_{ref} = 1.0 mA)	V_{ref}				V
T_A = 25°C		5.9	6.24	6.5	
T_A = −40° to +85°C		5.82	–	6.57	
Line Regulation (V_{CC} = 10 to 30 V, I_{ref} = 1.0 mA)	Reg_{line}	–	1.5	30	mV
Load Regulation (I_{ref} = 1.0 to 20 mA)	Reg_{load}	–	16	30	mV
Output Short Circuit Current (Note 3)	I_{SC}	40	75	–	mA
Reference Under Voltage Lockout Threshold	V_{th}	4.0	4.5	5.0	V
ERROR AMPLIFIER					
Input Offset Voltage (T_A = −40° to +85°C)	V_{IO}	–	0.4	10	mV
Input Offset Current (T_A = −40° to +85°C)	I_{IO}	–	8.0	500	nA
Input Bias Current (T_A = −40° to +85°C)	I_{IB}	–	−46	−1000	nA
Input Common Mode Voltage Range	V_{ICR}		(0 V to V_{ref})		V
Open Loop Voltage Gain (V_O = 3.0 V, R_L = 15 k)	A_{VOL}	70	80	–	dB
Input Common Mode Rejection Ratio	CMRR	55	86	–	dB
Power Supply Rejection Ratio (V_{CC} = V_C = 10 to 30 V)	PSRR	65	105	–	dB

NOTES: 1. The input common mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V.
2. The compliance voltage must not exceed the range of −0.3 to V_{ref}.
3. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = V_C = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Output Voltage Swing					V
High State (R_L = 15 k to Gnd)	V_{OH}	4.6	5.3	–	
Low State (R_L = 15 k to V_{ref})	V_{OL}	–	0.5	1.0	
OSCILLATOR SECTION					
Oscillator Frequency	f_{OSC}	22	25	28	kHz
Frequency Change with Voltage (V_{CC} = 10 to 30 V)	$\Delta f_{OSC}/\Delta V$	–	0.01	5.0	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	–	4.1	4.5	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	1.2	1.5	–	V
LOGIC INPUTS					
Input Threshold Voltage (Pins 3, 4, 5, 6, 7, 22, 23)					V
High State	V_{IH}	3.0	2.2	–	
Low State	V_{IL}	–	1.7	0.8	
Sensor Inputs (Pins 4, 5, 6)					µA
High State Input Current (V_{IH} = 5.0 V)	I_{IH}	–150	–70	–20	
Low State Input Current (V_{IL} = 0 V)	I_{IL}	–600	–337	–150	
Forward/Reverse, 60°/$\overline{120°}$ Select (Pins 3, 22, 23)					µA
High State Input Current (V_{IH} = 5.0 V)	I_{IH}	–75	–36	–10	
Low State Input Current (V_{IL} = 0 V)	I_{IL}	–300	–175	–75	
Output Enable					µA
High State Input Current (V_{IH} = 5.0 V)	I_{IH}	–60	–29	–10	
Low State Input Current (V_{IL} = 0 V)	I_{IL}	–60	–29	–10	
CURRENT–LIMIT COMPARATOR					
Threshold Voltage	V_{th}	85	101	115	mV
Input Common Mode Voltage Range	V_{ICR}	–	3.0	–	V
Input Bias Current	I_{IB}	–	–0.9	–5.0	µA
OUTPUTS AND POWER SECTIONS					
Top Drive Output Sink Saturation (I_{sink} = 25 mA)	$V_{CE(sat)}$	–	0.5	1.5	V
Top Drive Output Off–State Leakage (V_{CE} = 30 V)	$I_{DRV(leak)}$	–	0.06	100	µA
Top Drive Output Switching Time (C_L = 47 pF, R_L = 1.0 k)					ns
Rise Time	t_r	–	107	300	
Fall Time	t_f	–	26	300	
Bottom Drive Output Voltage					V
High State (V_{CC} = 20 V, V_C = 30 V, I_{source} = 50 mA)	V_{OH}	(V_{CC} –2.0)	(V_{CC} –1.1)	–	
Low State (V_{CC} = 20 V, V_C = 30 V, I_{sink} = 50 mA)	V_{OL}	–	1.5	2.0	
Bottom Drive Output Switching Time (C_L = 1000 pF)					ns
Rise Time	t_r	–	38	200	
Fall Time	t_f	–	30	200	
$\overline{Fault}$ Output Sink Saturation (I_{sink} = 16 mA)	$V_{CE(sat)}$	–	225	500	mV
$\overline{Fault}$ Output Off–State Leakage (V_{CE} = 20 V)	$I_{FLT(leak)}$	–	1.0	100	µA
Under Voltage Lockout					V
Drive Output Enabled (V_{CC} or V_C Increasing)	$V_{th(on)}$	8.2	8.9	10	
Hysteresis	V_H	0.1	0.2	0.3	
Power Supply Current					mA
Pin 17 (V_{CC} = V_C = 20 V)	I_{CC}	–	12	16	
Pin 17 (V_{CC} = 20 V, V_C = 30 V)		–	14	20	
Pin 18 (V_{CC} = V_C = 20 V)	I_C	–	3.5	6.0	
Pin 18 (V_{CC} = 20 V, V_C = 30 V)		–	5.0	10	

4

Figure 1. Oscillator Frequency versus Timing Resistor

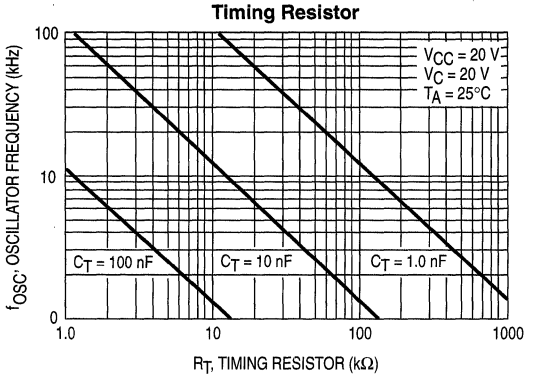


Figure 2. Oscillator Frequency Change versus Temperature

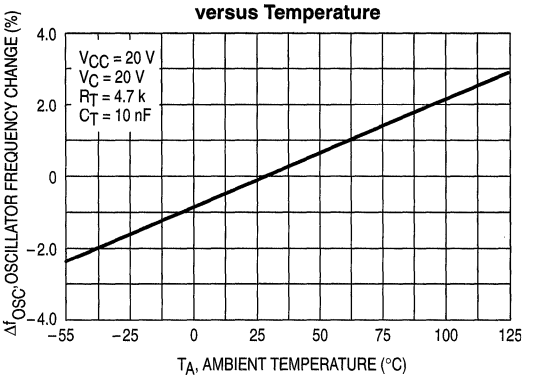


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

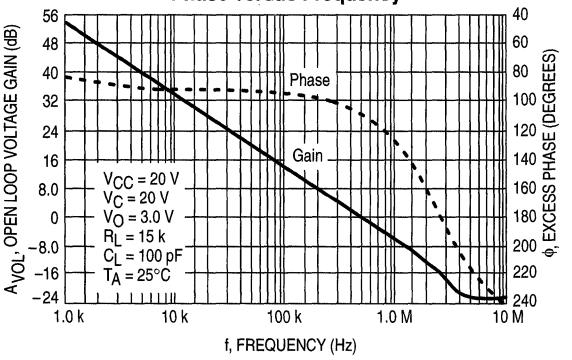


Figure 4. Error Amp Output Saturation Voltage versus Load Current

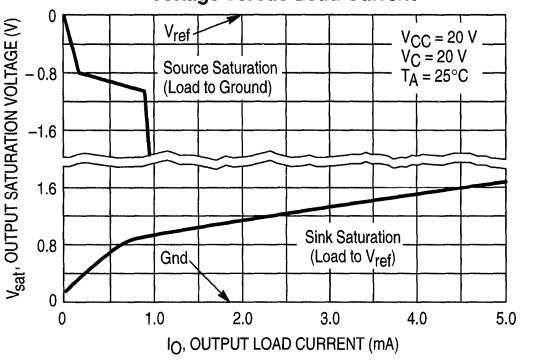


Figure 5. Error Amp Small–Signal Transient Response

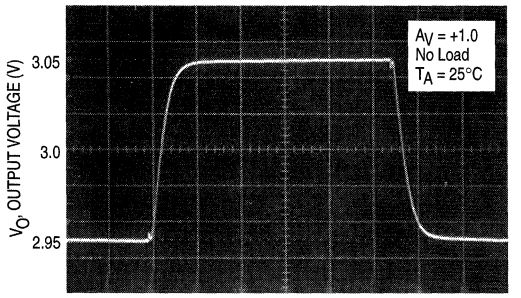


Figure 6. Error Amp Large–Signal Transient Response

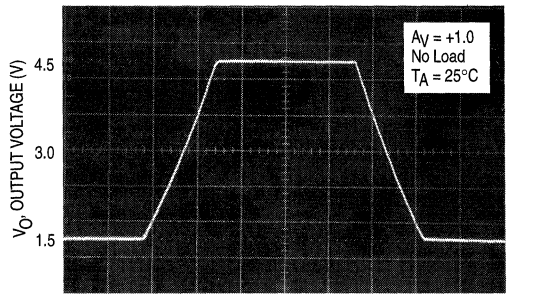


Figure 7. Reference Output Voltage Change versus Output Source Current

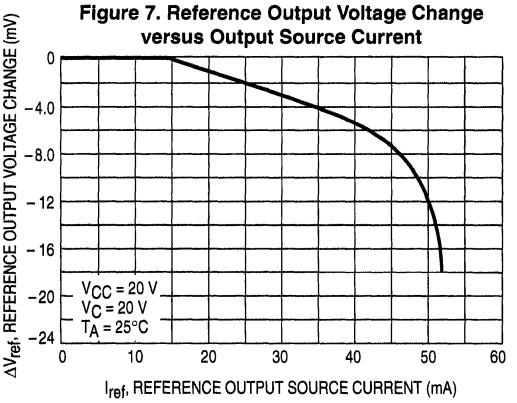


Figure 8. Reference Output Voltage versus Supply Voltage

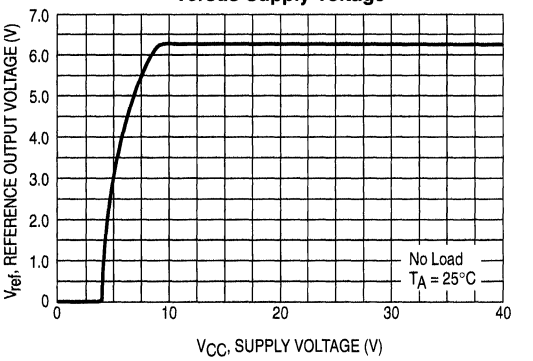


Figure 9. Reference Output Voltage versus Temperature

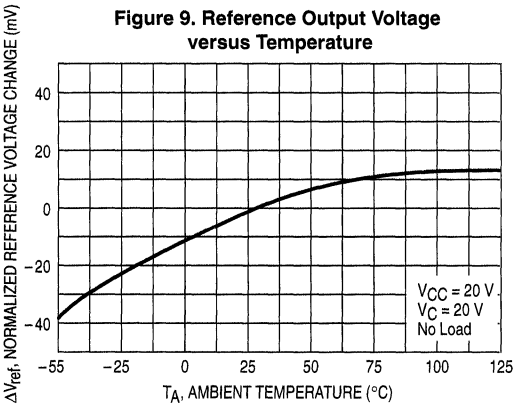


Figure 10. Output Duty Cycle versus PWM Input Voltage

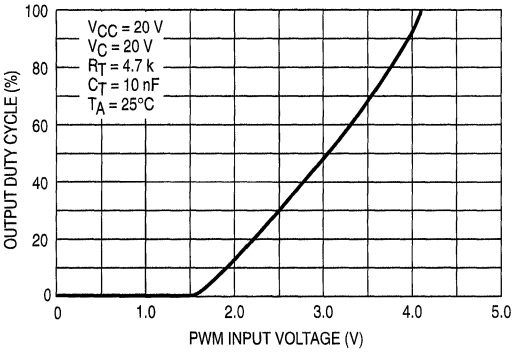


Figure 11. Bottom Drive Response Time versus Current Sense Input Voltage

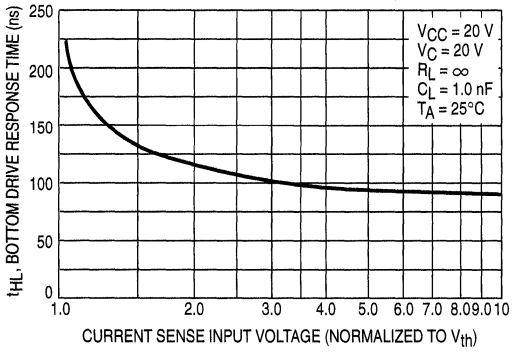


Figure 12. $\overline{\text{Fault}}$ Output Saturation versus Sink Current

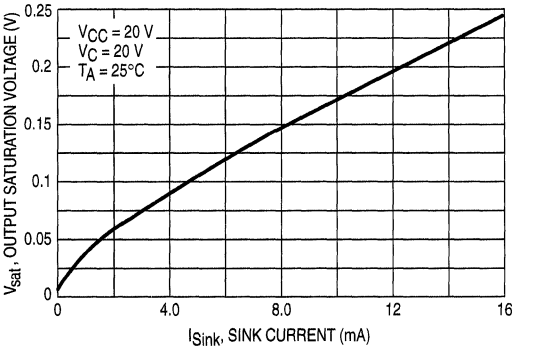


Figure 13. Top Drive Output Saturation Voltage versus Sink Current

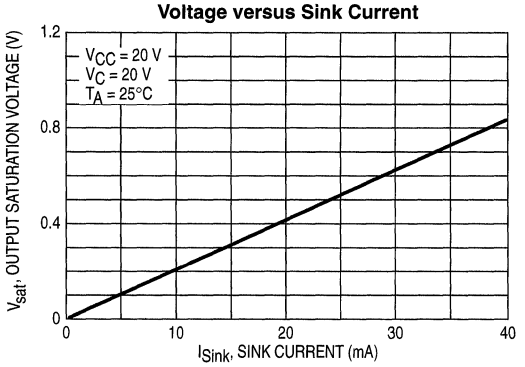
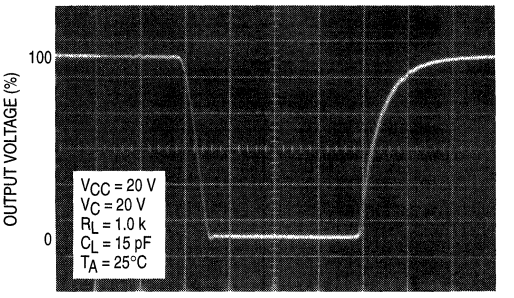
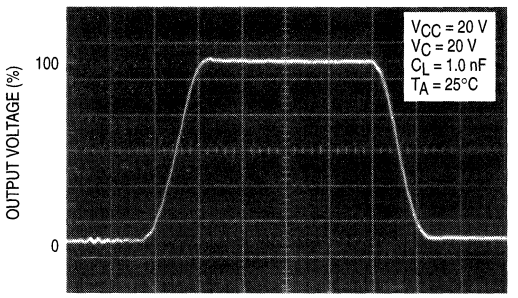


Figure 14. Top Drive Output Waveform



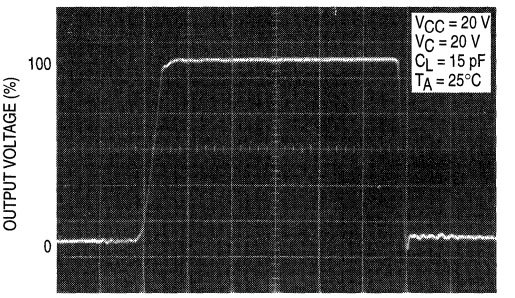
100 ns/DIV

Figure 15. Bottom Drive Output Waveform



50 ns/DIV

Figure 16. Bottom Drive Output Waveform



50 ns/DIV

Figure 17. Bottom Drive Output Saturation Voltage versus Load Current

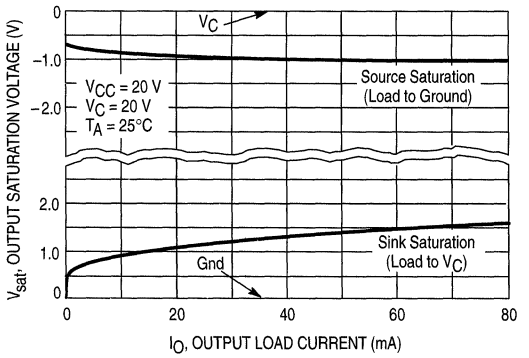
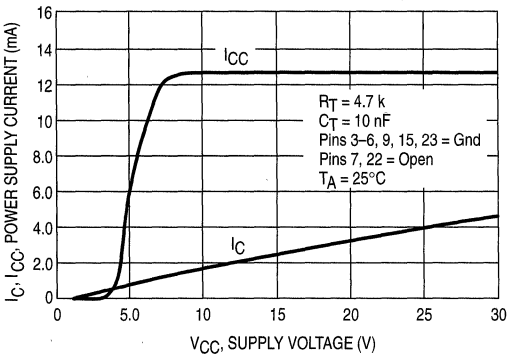


Figure 18. Power and Bottom Drive Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1, 2, 24	B_T, A_T, C_T	These three open collector Top Drive outputs are designed to drive the external upper power switch transistors.
3	Fwd/Rev	The Forward/Reverse Input is used to change the direction of motor rotation.
4, 5, 6	S_A, S_B, S_C	These three Sensor Inputs control the commutation sequence.
7	Output Enable	A logic high at this input causes the motor to run, while a low causes it to coast.
8	Reference Output	This output provides charging current for the oscillator timing capacitor C_T and a reference for the error amplifier. It may also serve to furnish sensor power.
9	Current Sense Noninverting Input	A 100 mV signal, with respect to Pin 15, at this input terminates output switch conduction during a given oscillator cycle. This pin normally connects to the top side of the current sense resistor.
10	Oscillator	The Oscillator frequency is programmed by the values selected for the timing components, R_T and C_T.
11	Error Amp Noninverting Input	This input is normally connected to the speed set potentiometer.
12	Error Amp Inverting Input	This input is normally connected to the Error Amp Output in open loop applications.
13	Error Amp Out/PWM Input	This pin is available for compensation in closed loop applications.
14	$\overline{\text{Fault}}$ Output	This open collector output is active low during one or more of the following conditions: Invalid Sensor Input code, Enable Input at logic 0, Current Sense Input greater than 100 mV (Pin 9 with respect to Pin 15), Undervoltage Lockout activation, and Thermal Shutdown.
15	Current Sense Inverting Input	Reference pin for internal 100 mV threshold. This pin is normally connected to the bottom side of the current sense resistor.
16	Gnd	This pin supplies a ground for the control circuit and should be referenced back to the power source ground.
17	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 10 to 30 V.
18	V_C	The high state (V_{OH}) of the Bottom Drive Outputs is set by the voltage applied to this pin. The controller is operational over a minimum V_C range of 10 to 30 V.
19, 20, 21	C_B, B_B, A_B	These three totem pole Bottom Drive Outputs are designed for direct drive of the external bottom power switch transistors.
22	60°/$\overline{120°}$ Select	The electrical state of this pin configures the control circuit operation for either 60° (high state) or 120° (low state) sensor electrical phasing inputs.
23	Brake	A logic low state at this input allows the motor to run, while a high state does not allow motor operation and if operating causes rapid deceleration.

INTRODUCTION

The MC33035 is one of a series of high performance monolithic DC brushless motor controllers produced by Motorola. It contains all of the functions required to implement a full–featured, open loop, three or four phase motor control system. In addition, the controller can be made to operate DC brush motors. Constructed with Bipolar Analog technology, it offers a high degree of performance and ruggedness in hostile industrial environments. The MC33035 contains a rotor position decoder for proper commutation sequencing, a temperature compensated reference capable of supplying a sensor power, a frequency programmable sawtooth oscillator, a fully accessible error amplifier, a pulse width modulator comparator, three open collector top drive outputs, and three high current totem pole bottom driver outputs ideally suited for driving power MOSFETs.

Included in the MC33035 are protective features consisting of undervoltage lockout, cycle–by–cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique fault output that can easily be interfaced to a microprocessor controller.

Typical motor control functions include open loop speed control, forward or reverse rotation, run enable, and dynamic braking. In addition, the MC33035 has a 60°/$\overline{120°}$ select pin which configures the rotor position decoder for either 60° or 120° sensor electrical phasing inputs.

FUNCTIONAL DESCRIPTION

A representative internal block diagram is shown in Figure 19 with various applications shown in Figures 36, 38, 39, 43, 45, and 46. A discussion of the features and function of each of the internal blocks given below is referenced to Figures 19 and 36.

Rotor Position Decoder

An internal rotor position decoder monitors the three sensor inputs (Pins 4, 5, 6) to provide the proper sequencing of the top and bottom drive outputs. The sensor inputs are designed to interface directly with open collector type Hall Effect switches or opto slotted couplers. Internal pull–up resistors are included to minimize the required number of external components. The inputs are TTL compatible, with their thresholds typically at 2.2 V. The MC33035 series is designed to control three phase motors and operate with four of the most common conventions of sensor phasing. A 60°/$\overline{120°}$ Select (Pin 22) is conveniently provided and affords the MC33035 to configure itself to control motors having either 60°, 120°, 240° or 300° electrical sensor phasing. With three sensor inputs there are eight possible input code combinations, six of which are valid rotor positions. The remaining two codes are invalid and are usually caused by an open or shorted sensor line. With six valid input codes, the

decoder can resolve the motor rotor position to within a window of 60 electrical degrees.

The Forward/Reverse input (Pin 3) is used to change the direction of motor rotation by reversing the voltage across the stator winding. When the input changes state, from high to low with a given sensor input code (for example 100), the enabled top and bottom drive outputs with the same alpha designation are exchanged (A_T to A_B, B_T to B_B, C_T to C_B). In effect, the commutation sequence is reversed and the motor changes directional rotation.

Motor on/off control is accomplished by the Output Enable (Pin 7). When left disconnected, an internal 25 μA current source enables sequencing of the top and bottom drive outputs. When grounded, the top drive outputs turn off and the bottom drives are forced low, causing the motor to coast and the $\overline{\text{Fault}}$ output to activate.

Dynamic motor braking allows an additional margin of safety to be designed into the final product. Braking is accomplished by placing the Brake Input (Pin 23) in a high state. This causes the top drive outputs to turn off and the bottom drives to turn on, shorting the motor–generated back EMF. The brake input has unconditional priority over all other inputs. The internal 40 kΩ pull–up resistor simplifies interfacing with the system safety–switch by insuring brake activation if opened or disconnected. The commutation logic truth table is shown in Figure 20. A four input NOR gate is used to monitor the brake input and the inputs to the three top drive output transistors. Its purpose is to disable braking until the top drive outputs attain a high state. This helps to prevent simultaneous conduction of the the top and bottom power switches. In half wave motor drive applications, the top drive outputs are not required and are normally left disconnected. Under these conditions braking will still be accomplished since the NOR gate senses the base voltage to the top drive output transistors.

Error Amplifier

A high performance, fully compensated error amplifier with access to both inputs and output (Pins 11, 12, 13) is provided to facilitate the implementation of closed loop motor speed control. The amplifier features a typical DC voltage gain of 80 dB, 0.6 MHz gain bandwidth, and a wide input common mode voltage range that extends from ground to V_{ref}. In most open loop speed control applications, the amplifier is configured as a unity gain voltage follower with the noninverting input connected to the speed set voltage source. Additional configurations are shown in Figures 31 through 35.

Oscillator

The frequency of the internal ramp oscillator is programmed by the values selected for timing components R_T and C_T. Capacitor C_T is charged from the Reference Output (Pin 8) through resistor R_T and discharged by an internal discharge transistor. The ramp peak and valley voltages are typically 4.1 V and 1.5 V respectively. To provide a good compromise between audible noise and output switching efficiency, an oscillator frequency in the range of 20 to 30 kHz is recommended. Refer to Figure 1 for component selection.

Figure 19. Representative Block Diagram

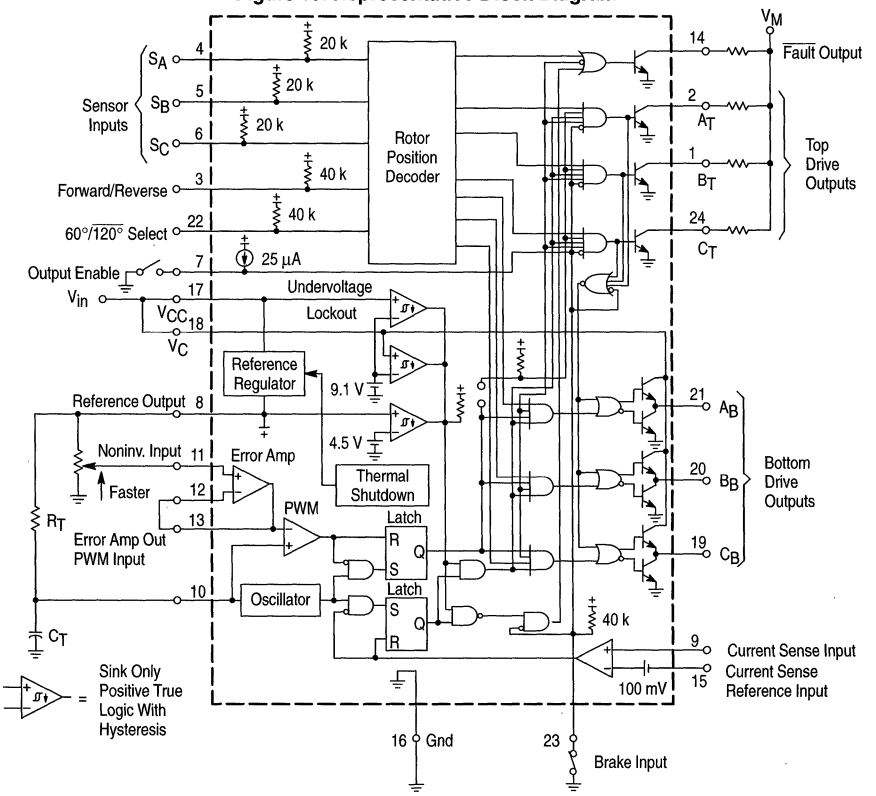


Figure 20. Three Phase, Six Step Commutation Truth Table (Note 1)

Inputs (Note 2)										Outputs (Note 3)							
Sensor Electrical Phasing (Note 4)										Top Drives			Bottom Drives				
60°			120°														
S_A	S_B	S_C	S_A	S_B	S_C	F/R	Enable	Brake	Current Sense	A_T	B_T	C_T	A_B	B_B	C_B	$\overline{Fault}$	
1	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1	1	(Note 5) F/R = 1
1	1	0	1	1	0	1	1	0	0	1	0	1	0	0	1	1	
1	1	1	0	1	0	1	1	0	0	1	0	1	1	0	0	1	
0	1	1	0	1	1	1	1	0	0	1	1	0	1	0	0	1	
0	0	1	0	0	1	1	1	0	0	1	1	0	0	1	0	1	
0	0	0	1	0	1	1	1	0	0	0	1	1	0	1	0	1	
1	0	0	1	0	0	0	1	0	0	1	1	0	1	0	0	1	(Note 5) F/R = 0
1	1	0	1	1	0	0	1	0	0	1	1	0	0	1	0	1	
1	1	1	0	1	0	0	1	0	0	0	1	1	0	1	0	1	
0	1	1	0	1	1	0	1	0	0	0	1	1	0	0	1	1	
0	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1	1	
0	0	0	1	0	1	0	1	0	0	1	0	1	1	0	0	1	
1	0	1	1	1	1	X	X	0	X	1	1	1	0	0	0	0	(Note 6) Brake = 0
0	1	0	0	0	0	X	X	0	X	1	1	1	0	0	0	0	
1	0	1	1	1	1	X	X	1	X	1	1	1	1	1	1	0	(Note 7) Brake = 1
0	1	0	0	0	0	X	X	1	X	1	1	1	1	1	1	0	
V	V	V	V	V	V	X	1	1	X	1	1	1	1	1	1	1	(Note 8)
V	V	V	V	V	V	X	0	1	X	1	1	1	1	1	1	0	(Note 9)
V	V	V	V	V	V	X	0	0	X	1	1	1	0	0	0	0	(Note 10)
V	V	V	V	V	V	X	1	0	1	1	1	1	0	0	0	0	(Note 11)

NOTES: 1. V = Any one of six valid sensor or drive combinations X = Don't care.
2. The digital inputs (Pins 3, 4, 5, 6, 7, 22, 23) are all TTL compatible. The current sense input (Pin 9) has a 100 mV threshold with respect to Pin 15. A logic 0 for this input is defined as < 85 mV, and a logic 1 is > 115 mV.
3. The fault and top drive outputs are open collector design and active in the low (0) state.
4. With 60°/120° select (Pin 22) in the high (1) state, configuration is for 60° sensor electrical phasing inputs. With Pin 22 in low (0) state, configuration is for 120° sensor electrical phasing inputs.
5. Valid 60° or 120° sensor combinations for corresponding valid top and bottom drive outputs.
6. Invalid sensor inputs with brake = 0; All top and bottom drives off, Fault low.
7. Invalid sensor inputs with brake = 1; All top drives off, all bottom drives on, Fault low.
8. Valid 60° or 120° sensor inputs with brake = 1; All top drives off, all bottom drives on, Fault high.
9. Valid sensor inputs with brake = 1 and enable = 0; All top drives off, all bottom drives on, Fault low.
10. Valid sensor inputs with brake = 0 and enable = 0; All top and bottom drives off, Fault low.
11. All bottom drives off, Fault low.

Pulse Width Modulator

The use of pulse width modulation provides an energy efficient method of controlling the motor speed by varying the average voltage applied to each stator winding during the commutation sequence. As C_T discharges, the oscillator sets both latches, allowing conduction of the top and bottom drive outputs. The PWM comparator resets the upper latch, terminating the bottom drive output conduction when the positive–going ramp of C_T becomes greater than the error amplifier output. The pulse width modulator timing diagram is shown in Figure 21. Pulse width modulation for speed control appears only at the bottom drive outputs.

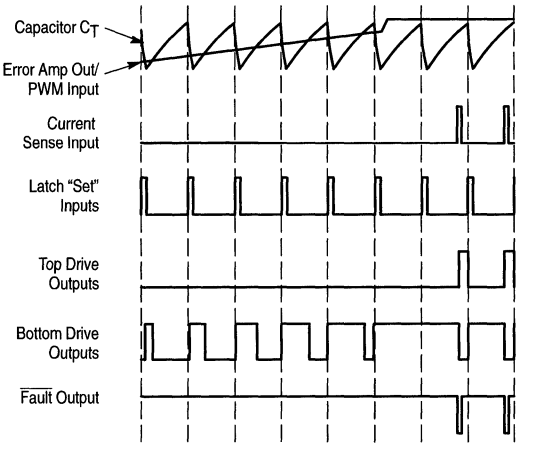
Current Limit

Continuous operation of a motor that is severely over–loaded results in overheating and eventual failure. This destructive condition can best be prevented with the use of cycle–by–cycle current limiting. That is, each on–cycle is treated as a separate event. Cycle–by–cycle current limiting is accomplished by monitoring the stator current build–up each time an output switch conducts, and upon sensing an over current condition, immediately turning off the switch and holding it off for the remaining duration of oscillator ramp–up period. The stator current is converted to a voltage by inserting a ground–referenced sense resistor R_S (Figure 36) in series with the three bottom switch transistors (Q_4, Q_5, Q_6). The voltage developed across the sense resistor is monitored by the Current Sense Input (Pins 9 and 15), and compared to the internal 100 mV reference. The current sense comparator inputs have an input common mode range of approximately 3.0 V. If the 100 mV current sense threshold is exceeded, the comparator resets the lower sense latch and terminates output switch conduction. The value for the current sense resistor is:

$$R_S = \frac{0.1}{I_{stator(max)}}$$

The $\overline{Fault}$ output activates during an over current condition. The dual–latch PWM configuration ensures that only one single output conduction pulse occurs during any given oscillator cycle, whether terminated by the output of the error amp or the current limit comparator.

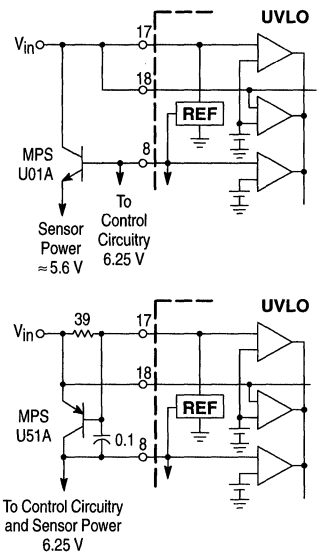
Figure 21. Pulse Width Modulator Timing Diagram



Reference

The on–chip 6.25 V regulator (Pin 8) provides charging current for the oscillator timing capacitor, a reference for the error amplifier, and can supply 20 mA of current suitable for directly powering sensors in low voltage applications. In higher voltage applications, it may become necessary to transfer the power dissipated by the regulator off the IC. This is easily accomplished with the addition of an external pass transistor as shown in Figure 22. A 6.25 V reference level was chosen to allow implementation of the simpler NPN circuit, where $V_{ref} - V_{BE}$ exceeds the minimum voltage required by Hall Effect sensors over temperature. With proper transistor selection and adequate heatsinking, up to one amp of load current can be obtained.

Figure 22. Reference Output Buffers



The NPN circuit is recommended for powering Hall or opto sensors, where the output voltage temperature coefficient is not critical. The PNP circuit is slightly more complex, but is also more accurate over temperature. Neither circuit has current limiting.

Undervoltage Lockout

A triple Undervoltage Lockout has been incorporated to prevent damage to the IC and the external power switch transistors. Under low power supply conditions, it guarantees that the IC and sensors are fully functional, and that there is sufficient bottom drive output voltage. The positive power supplies to the IC (V_{CC}) and the bottom drives (V_C) are each monitored by separate comparators that have their thresholds at 9.1 V. This level ensures sufficient gate drive necessary to attain low $R_{DS(on)}$ when driving standard power MOSFET devices. When directly powering the Hall sensors from the reference, improper sensor operation can result if the reference output voltage falls below 4.5 V. A third comparator is used to detect this condition. If one or more of the comparators detects an undervoltage condition, the $\overline{\text{Fault}}$ Output is activated, the top drives are turned off and the bottom drive outputs are held in a low state. Each of the comparators contain hysteresis to prevent oscillations when crossing their respective thresholds.

$\overline{\text{Fault}}$ Output

The open collector $\overline{\text{Fault}}$ Output (Pin 14) was designed to provide diagnostic information in the event of a system malfunction. It has a sink current capability of 16 mA and can directly drive a light emitting diode for visual indication. Additionally, it is easily interfaced with TTL/CMOS logic for use in a microprocessor controlled system. The $\overline{\text{Fault}}$ Output is active low when one or more of the following conditions occur:

1) Invalid Sensor Input code
2) Output Enable at logic [0]
3) Current Sense Input greater than 100 mV
4) Undervoltage Lockout, activation of one or more of the comparators
5) Thermal Shutdown, maximum junction temperature being exceeded

This unique output can also be used to distinguish between motor start–up or sustained operation in an overloaded condition. With the addition of an RC network between the $\overline{\text{Fault}}$ Output and the enable input, it is possible to create a time–delayed latched shutdown for overcurrent. The added circuitry shown in Figure 23 makes easy starting of motor systems which have high inertial loads by providing additional starting torque, while still preserving overcurrent protection. This task is accomplished by setting the current limit to a higher than nominal value for a predetermined time. During an excessively long overcurrent condition, capacitor C_{DLY} will charge, causing the enable input to cross its threshold to a low state. A latch is then formed by the positive feedback loop from the $\overline{\text{Fault}}$ Output to the Output Enable. Once set, by the Current Sense Input, it can only be reset by shorting C_{DLY} or cycling the power supplies.

Drive Outputs

The three top drive outputs (Pins 1, 2, 24) are open collector NPN transistors capable of sinking 50 mA with a minimum breakdown of 30 V. Interfacing into higher voltage applications is easily accomplished with the circuits shown in Figures 24 and 25.

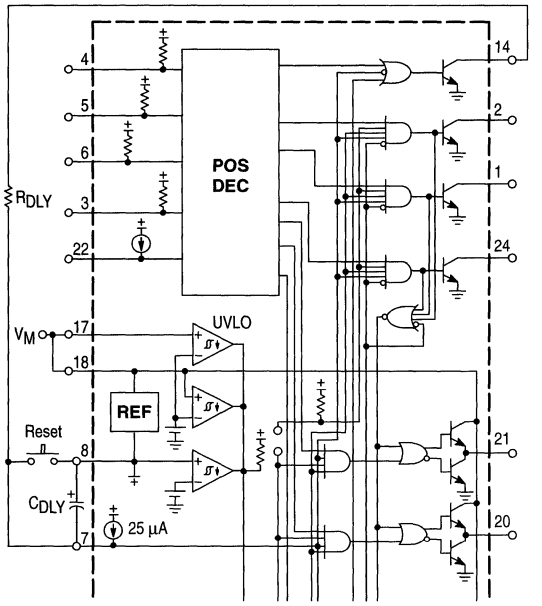
The three totem pole bottom drive outputs (Pins 19, 20, 21) are particularly suited for direct drive of N–Channel MOSFETs or NPN bipolar transistors (Figures 26, 27, 28 and 29). Each output is capable of sourcing and sinking up to 100 mA. Power for the bottom drives is supplied from V_C (Pin 18). This separate supply input allows the designer added flexibility in tailoring the drive voltage, independent of V_{CC}. A zener clamp should be connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V so as to prevent rupture of the MOSFET gates.

The control circuitry ground (Pin 16) and current sense inverting input (Pin 15) must return on separate paths to the central input source ground.

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event the maximum junction temperature is exceeded. When activated, typically at 170°C, the IC acts as though the Output Enable was grounded.

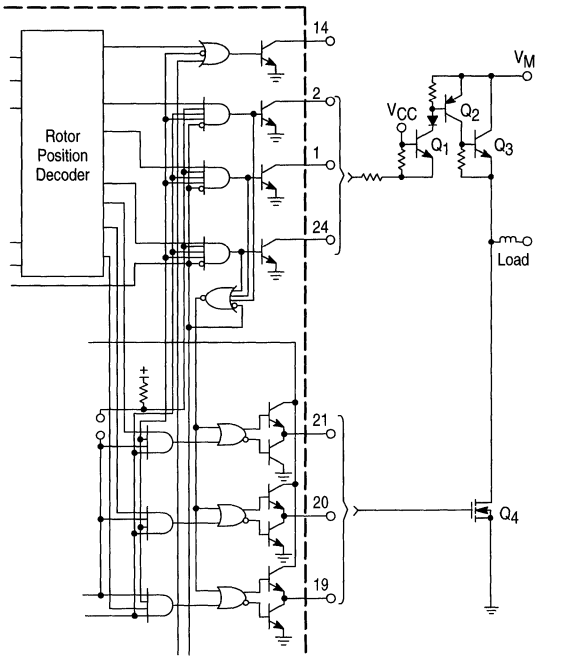
Figure 23. Timed Delayed Latched Over Current Shutdown



$$t_{DLY} \approx R_{DLY}\, C_{DLY}\, \ln\left(\frac{V_{ref} - (I_{IL}\ \text{enable}\ R_{DLY})}{V_{th}\ \text{enable} - (I_{IL}\ \text{enable}\ R_{DLY})}\right)$$

$$\approx R_{DLY}\, C_{DLY}\, \ln\left(\frac{6.25 - (20 \times 10^{-6}\, R_{DLY})}{1.4 - (20 \times 10^{-6}\, R_{DLY})}\right)$$

Figure 24. High Voltage Interface with NPN Power Transistors



Transistor Q_1 is a common base stage used to level shift from V_{CC} to the high motor voltage, V_M. The collector diode is required if V_{CC} is present while V_M is low.

Figure 25. High Voltage Interface with N–Channel Power MOSFETs

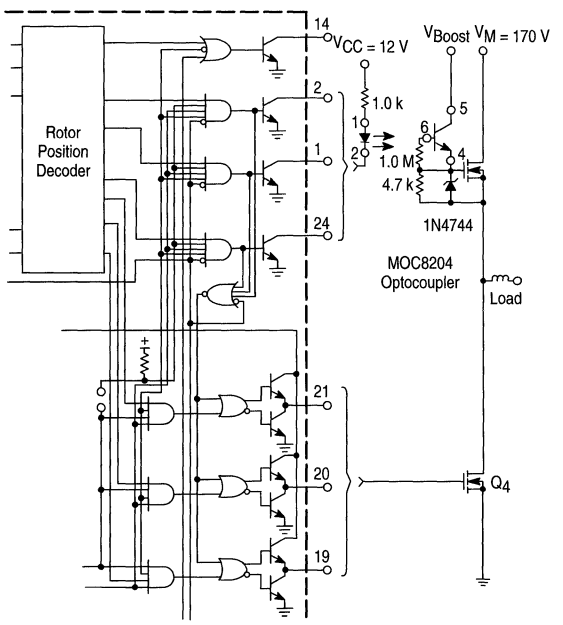
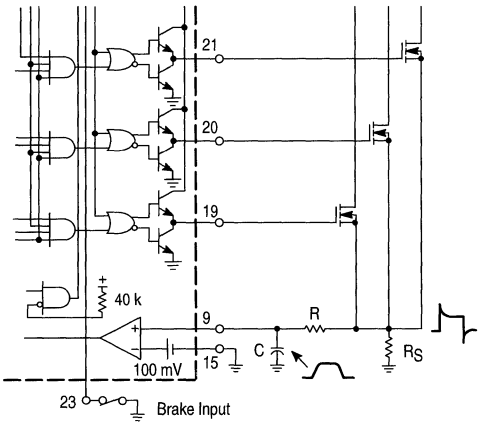
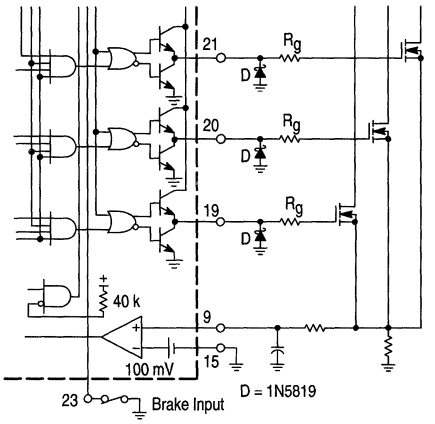


Figure 26. Current Waveform Spike Suppression



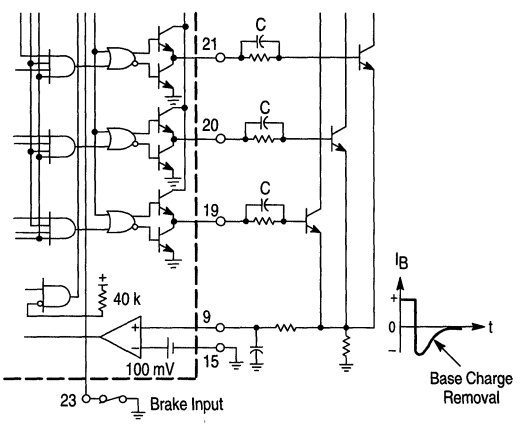
The addition of the RC filter will eliminate current–limit instability caused by the leading edge spike on the current waveform. Resistor R_S should be a low inductance type.

Figure 27. MOSFET Drive Precautions



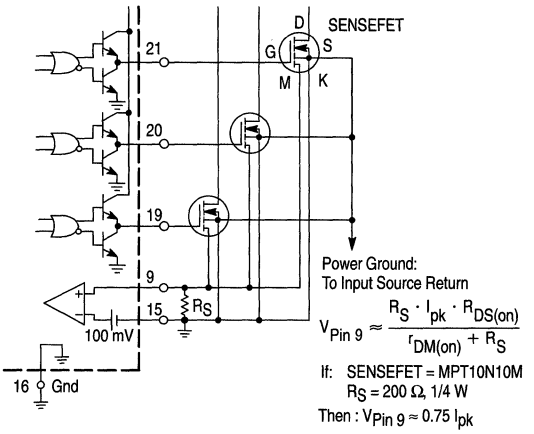
Series gate resistor R_g will dampen any high frequency oscillations caused by the MOSFET input capacitance and any series wiring induction in the gate–source circuit. Diode D is required if the negative current into the Bottom Drive Outputs exceeds 50 mA.

Figure 28. Bipolar Transistor Drive



The totem–pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C.

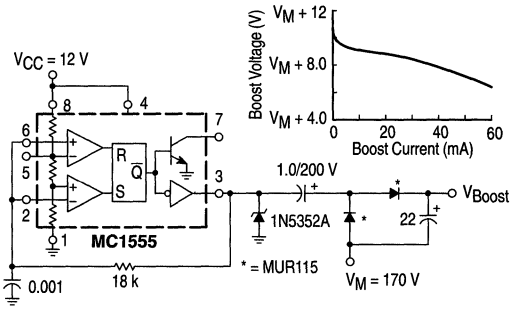
Figure 29. Current Sensing Power MOSFETs



Control Circuitry Ground (Pin 16) and Current Sense Inverting Input (Pin 15) must return on separate paths to the Central Input Source Ground.

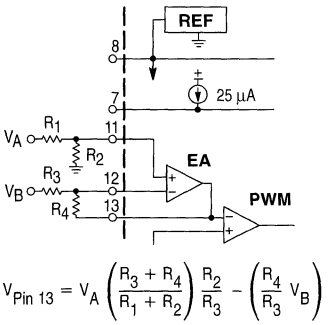
Virtually lossless current sensing can be achieved with the implementation of SENSEFET power switches.

Figure 30. High Voltage Boost Supply



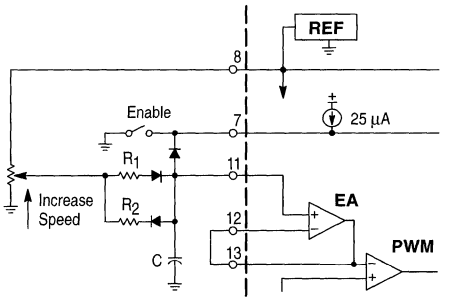
This circuit generates V_{Boost} for Figure 25.

Figure 31. Differential Input Speed Controller



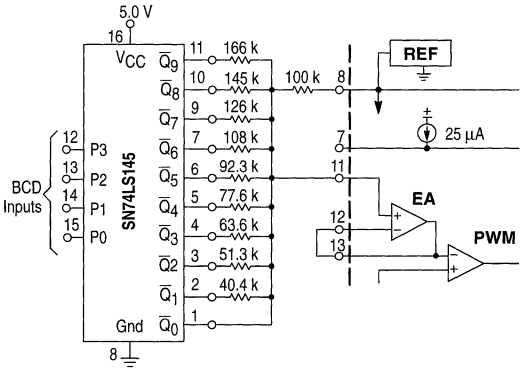
$$V_{Pin\ 13} = V_A \left(\frac{R_3 + R_4}{R_1 + R_2}\right)\frac{R_2}{R_3} - \left(\frac{R_4}{R_3} V_B\right)$$

Figure 32. Controlled Acceleration/Deceleration



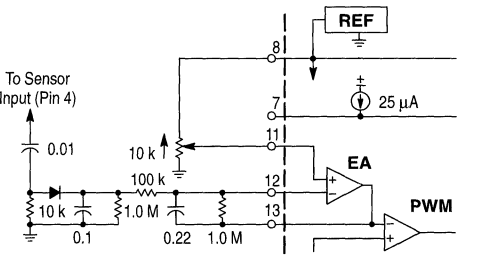
Resistor R_1 with capacitor C sets the acceleration time constant while R_2 controls the deceleration. The values of R_1 and R_2 should be at least ten times greater than the speed set potentiometer to minimize time constant variations with different speed settings.

Figure 33. Digital Speed Controller



The SN74LS145 is an open collector BCD to One of Ten decoder. When connected as shown, input codes 0000 through 1001 steps the PWM in increments of approximately 10% from 0 to 90% on–time. Input codes 1010 through 1111 will produce 100% on–time or full motor speed.

Figure 34. Closed Loop Speed Control



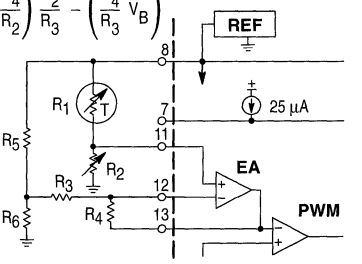
The rotor position sensors can be used as a tachometer. By differentiating the positive–going edges and then integrating them over time, a voltage proportional to speed can be generated. The error amp compares this voltage to that of the speed set to control the PWM.

Figure 35. Closed Loop Temperature Control

$$V_{Pin\ 3} = V_{ref}\left(\frac{R_3 + R_4}{R_1 + R_2}\right)\frac{R_2}{R_3} - \left(\frac{R_4}{R_3} V_B\right)$$

$$V_B = \frac{V_{ref}}{\left(\frac{R_5}{R_6} + 1\right)}$$

$$R_3 >> R_5 \parallel R_6$$



This circuit can control the speed of a cooling fan proportional to the difference between the sensor and set temperatures. The control loop is closed as the forced air cools the NTC thermistor. For controlled heating applications, exchange the positions of R_1 and R_2.

SYSTEM APPLICATIONS

Three Phase Motor Commutation

The three phase application shown in Figure 36 is a full–featured open loop motor controller with full wave, six step drive. The upper power switch transistors are Darlingtons while the lower devices are power MOSFETs. Each of these devices contains an internal parasitic catch diode that is used to return the stator inductive energy back to the power supply. The outputs are capable of driving a delta or wye connected stator, and a grounded neutral wye if split supplies are used. At any given rotor position, only one top and one bottom power switch (of different totem poles) is enabled. This configuration switches both ends of the stator winding from supply to ground which causes the current flow to be bidirectional or full wave. A leading edge spike is usually present on the current waveform and can cause a current–limit instability. The spike can be eliminated by adding an RC filter in series with the Current Sense Input. Using a low inductance type resistor for R_S will also aid in spike reduction. Care must be taken in the selection of the bottom power switch transistors so that the current during braking does not exceed the device rating. During braking, the peak current generated is limited only by the series resistance of the conducting bottom switch and winding.

$$I_{peak} = \frac{V_M + EMF}{R_{switch} + R_{winding}}$$

If the motor is running at maximum speed with no load, the generated back EMF can be as high as the supply voltage, and at the onset of braking, the peak current may approach twice the motor stall current. Figure 37 shows the commutation waveforms over two electrical cycles. The first cycle (0° to 360°) depicts motor operation at full speed while the second cycle (360° to 720°) shows a reduced speed with about 50% pulse width modulation. The current waveforms reflect a constant torque load and are shown synchronous to the commutation frequency for clarity.

Figure 36. Three Phase, Six Step, Full Wave Motor Controller

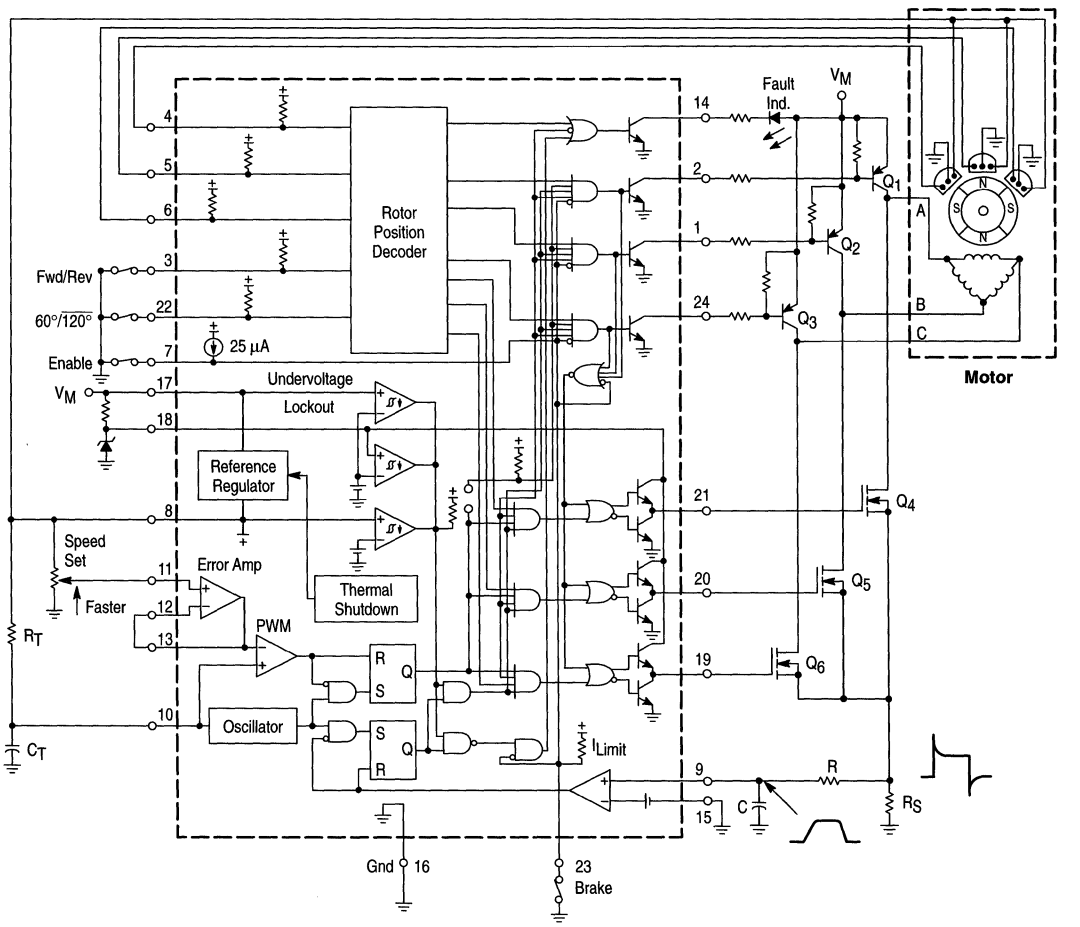


Figure 37. Three Phase, Six Step, Full Wave Commutation Waveforms

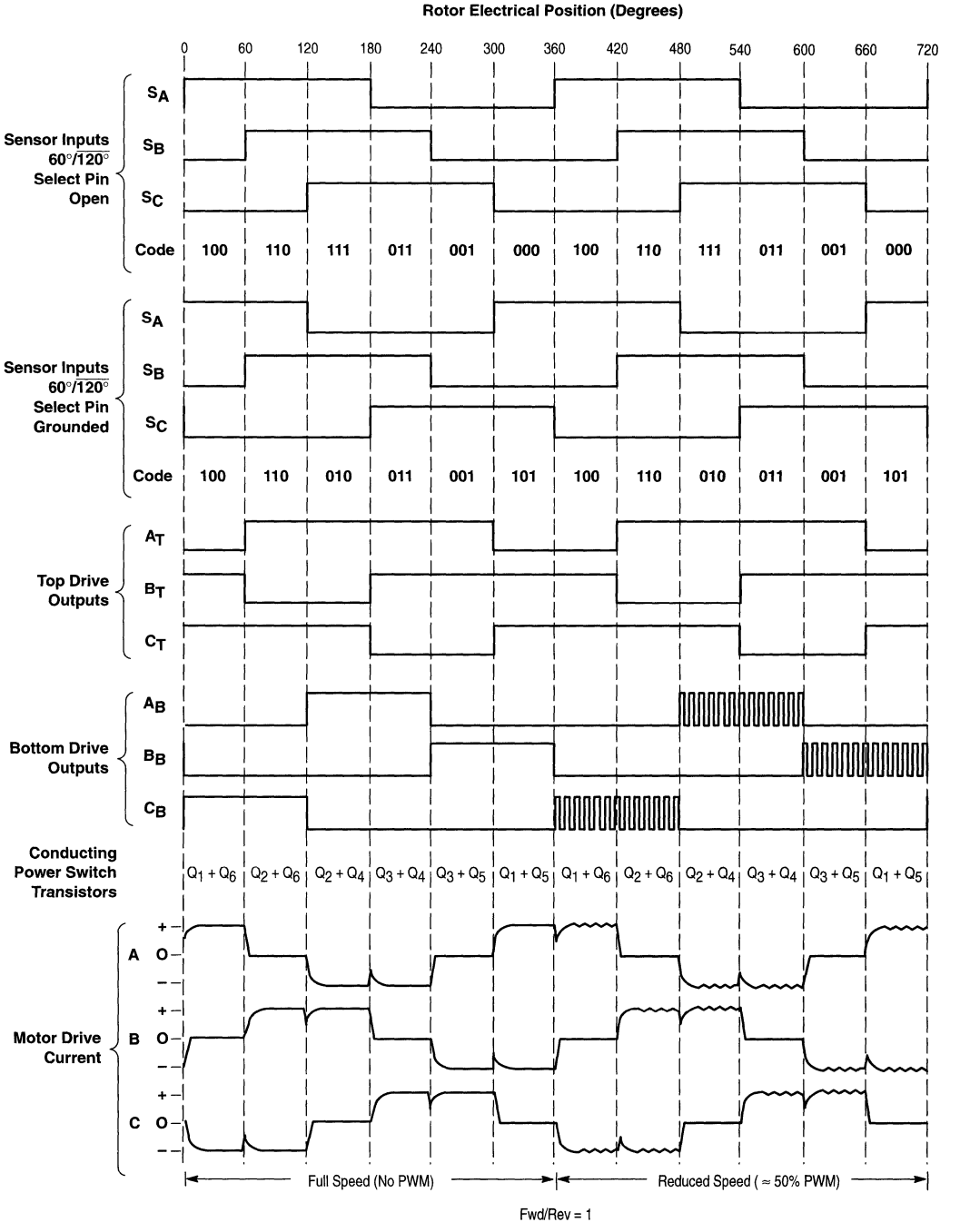
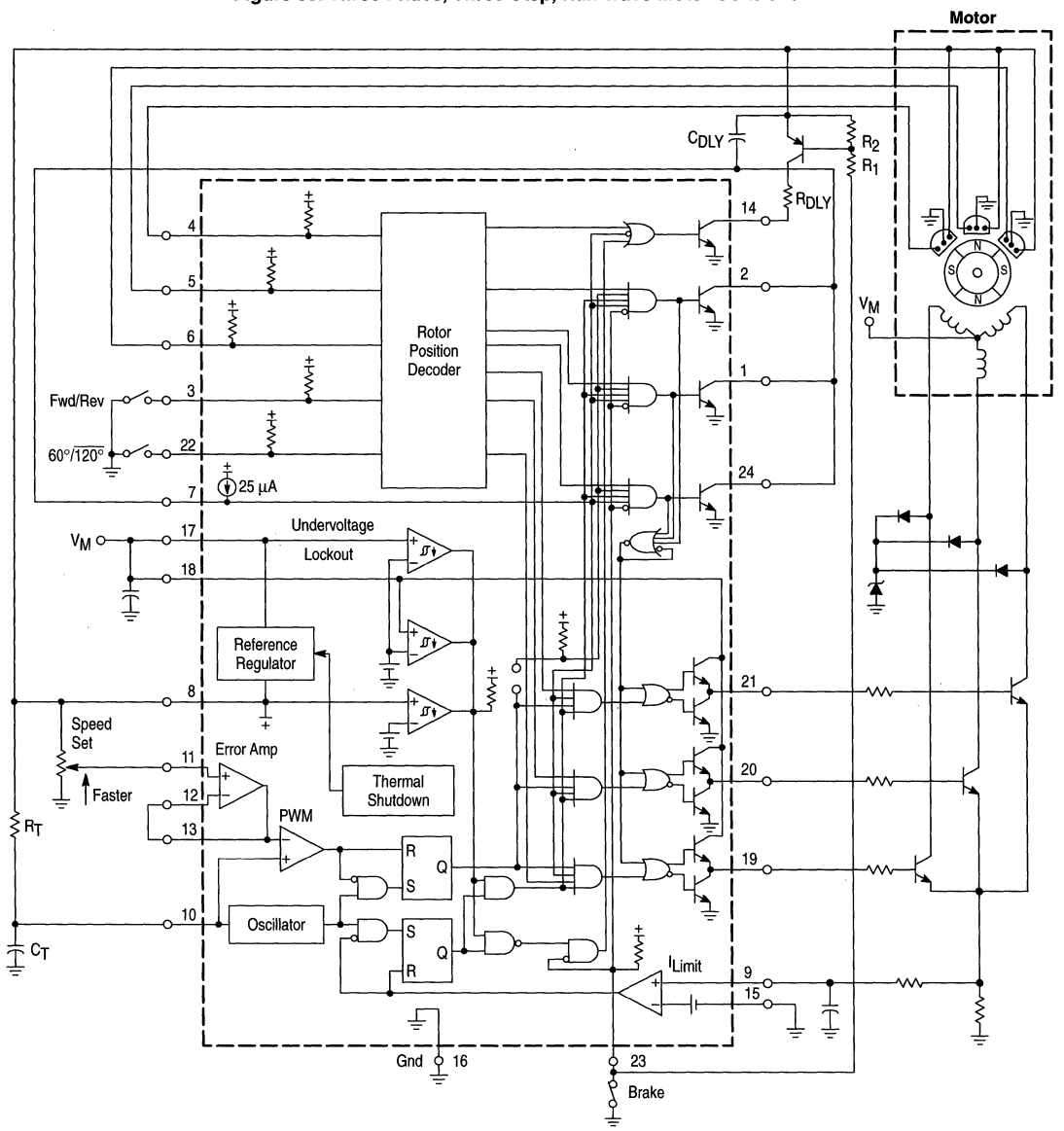


Figure 38 shows a three phase, three step, half wave motor controller. This configuration is ideally suited for automotive and other low voltage applications since there is only one power switch voltage drop in series with a given stator winding. Current flow is unidirectional or half wave because only one end of each winding is switched. Continuous braking with the typical half wave arrangement presents a motor overheating problem since stator current is limited only by the winding resistance. This is due to the lack of upper power switch transistors, as in the full wave circuit, used to disconnect the windings from the supply voltage V_M. A unique solution is to provide braking until the motor stops and then turn off the bottom drives. This can be accomplished by using the $\overline{\text{Fault}}$ Output in conjunction with the Output Enable as an over current timer. Components R_{DLY} and C_{DLY} are selected to give the motor sufficient time to stop before latching the Output Enable and the top drive AND gates low. When enabling the motor, the brake switch is closed and the PNP transistor (along with resistors R_1 and R_{DLY}) are used to reset the latch by discharging C_{DLY}. The stator flyback voltage is clamped by a single zener and three diodes.

4

Figure 38. Three Phase, Three Step, Half Wave Motor Controller



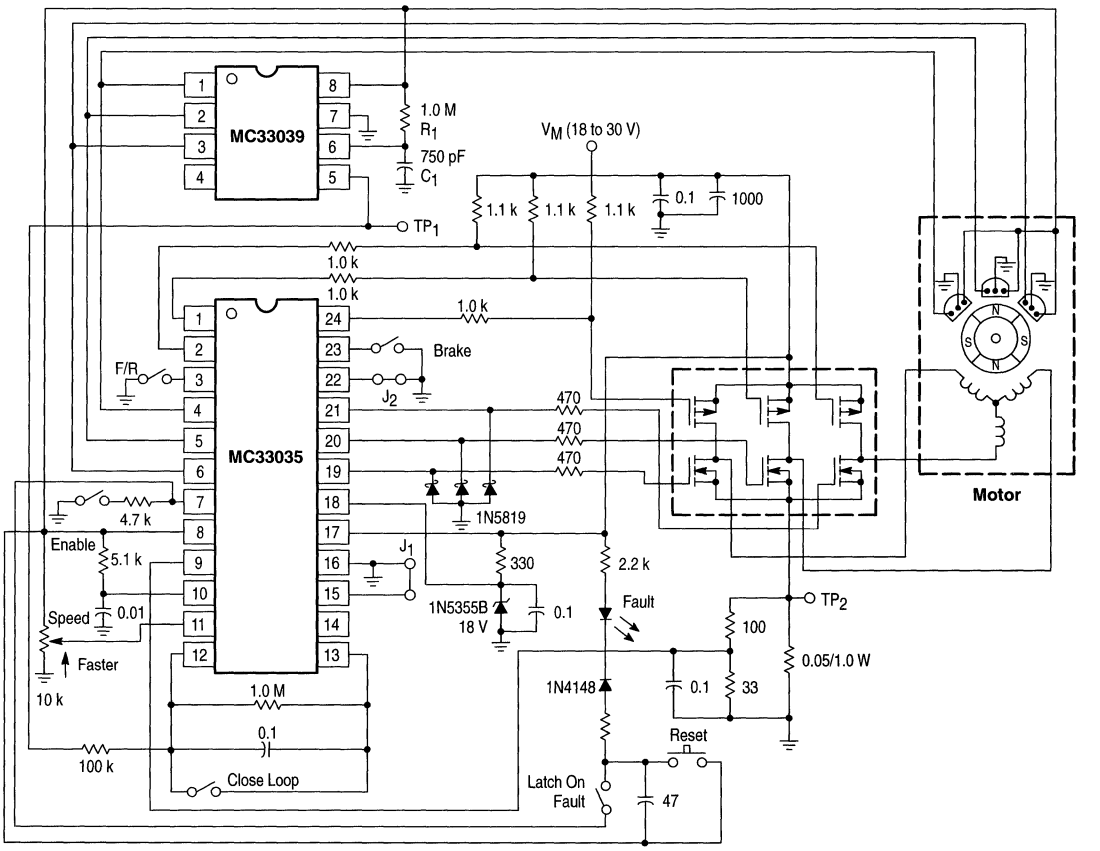
Three Phase Closed Loop Controller

The MC33035, by itself, is only capable of open loop motor speed control. For closed loop motor speed control, the MC33035 requires an input voltage proportional to the motor speed. Traditionally, this has been accomplished by means of a tachometer to generate the motor speed feedback voltage. Figure 39 shows an application whereby an MC33039, powered from the 6.25 V reference (Pin 8) of the MC33035, is used to generate the required feedback voltage without the need of a costly tachometer. The same Hall sensor signals used by the MC33035 for rotor position decoding are utilized by the MC33039. Every positive or negative going transition of the Hall sensor signals on any of the sensor lines causes the MC33039 to produce an output pulse of defined amplitude and time duration, as determined by the external resistor R_1 and capacitor C_1. The output train of pulses at Pin 5 of the MC33039 are integrated by the error amplifier of the MC33035 configured as an integrator to produce a DC voltage level which is proportional to the motor speed. This speed proportional voltage establishes the PWM reference level at Pin 13 of the MC33035 motor controller and closes the feedback loop. The MC33035 outputs drive a TMOS power MOSFET 3–phase bridge. High currents can be expected during conditions of start–up, breaking, and change of direction of the motor.

The system shown in Figure 39 is designed for a motor having 120/240 degrees Hall sensor electrical phasing. The system can easily be modified to accommodate 60/300 degree Hall sensor electrical phasing by removing the jumper (J_2) at Pin 22 of the MC33035.

4

Figure 39. Closed Loop Brushless DC Motor Control Using The MC33035 and MC33039



4

Sensor Phasing Comparison

There are four conventions used to establish the relative phasing of the sensor signals in three phase motors. With six step drive, an input signal change must occur every 60 electrical degrees; however, the relative signal phasing is dependent upon the mechanical sensor placement. A comparison of the conventions in electrical degrees is shown in Figure 40. From the sensor phasing table in Figure 41, note that the order of input codes for 60° phasing is the reverse of 300°. This means the MC33035, when configured for 60° sensor electrical phasing, will operate a motor with either 60° or 300° sensor electrical phasing, but resulting in opposite directions of rotation. The same is true for the part when it is configured for 120° sensor electrical phasing; the motor will operate equally, but will result in opposite directions of rotation for 120° for 240° conventions.

Figure 40. Sensor Phasing Comparison

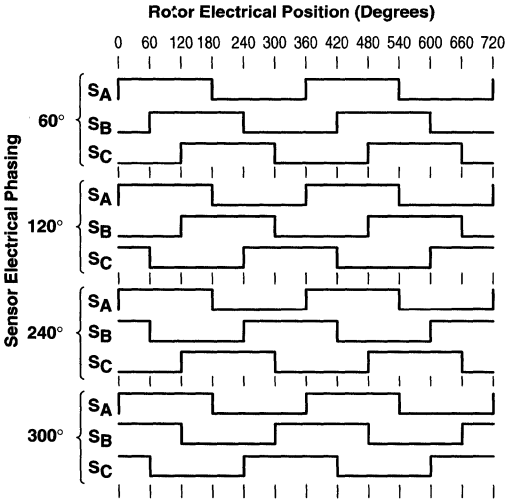


Figure 41. Sensor Phasing Table

Sensor Electrical Phasing (Degrees)												
60°			120°			240°			300°			
S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C	
1	0	0	1	0	1	1	1	0	1	1	1	
1	1	0	1	0	0	1	0	0	1	1	0	
1	1	1	1	1	0	1	0	1	1	0	0	
0	1	1	0	1	0	0	0	1	0	0	0	
0	0	1	0	1	1	0	1	1	0	0	1	
0	0	0	0	0	1	0	1	0	0	1	1	

In this data sheet, the rotor position is always given in electrical degrees since the mechanical position is a function of the number of rotating magnetic poles. The relationship between the electrical and mechanical position is:

$$\text{Electrical Degrees} = \text{Mechanical Degrees}\left(\frac{\#\text{Rotor Poles}}{2}\right)$$

An increase in the number of magnetic poles causes more electrical revolutions for a given mechanical revolution. General purpose three phase motors typically contain a four pole rotor which yields two electrical revolutions for one mechanical.

Two and Four Phase Motor Commutation

The MC33035 is also capable of providing a four step output that can be used to drive two or four phase motors. The truth table in Figure 42 shows that by connecting sensor inputs S_B and S_C together, it is possible to truncate the number of drive output states from six to four. The output power switches are connected to B_T, C_T, B_B, and C_B. Figure 43 shows a four phase, four step, full wave motor control application. Power switch transistors Q_1 through Q_8 are Darlington type, each with an internal parasitic catch diode. With four step drive, only two rotor position sensors spaced at 90 electrical degrees are required. The commutation waveforms are shown in Figure 44.

Figure 45 shows a four phase, four step, half wave motor controller. It has the same features as the circuit in Figure 38, except for the deletion of speed control and braking.

Figure 42. Two and Four Phase, Four Step, Commutation Truth Table

MC33035 (60°/$\overline{120°}$ Select Pin Open)						
Inputs			Outputs			
Sensor Electrical Spacing* = 90°			Top Drives		Bottom Drives	
S_A	S_B	F/R	B_T	C_T	B_B	C_B
1	0	1	1	1	0	1
1	1	1	0	1	0	0
0	1	1	1	0	0	0
0	0	1	1	1	1	0
1	0	0	1	0	0	0
1	1	0	1	1	1	0
0	1	0	1	1	0	1
0	0	0	0	1	0	0

*With MC33035 sensor input S_B connected to S_C.

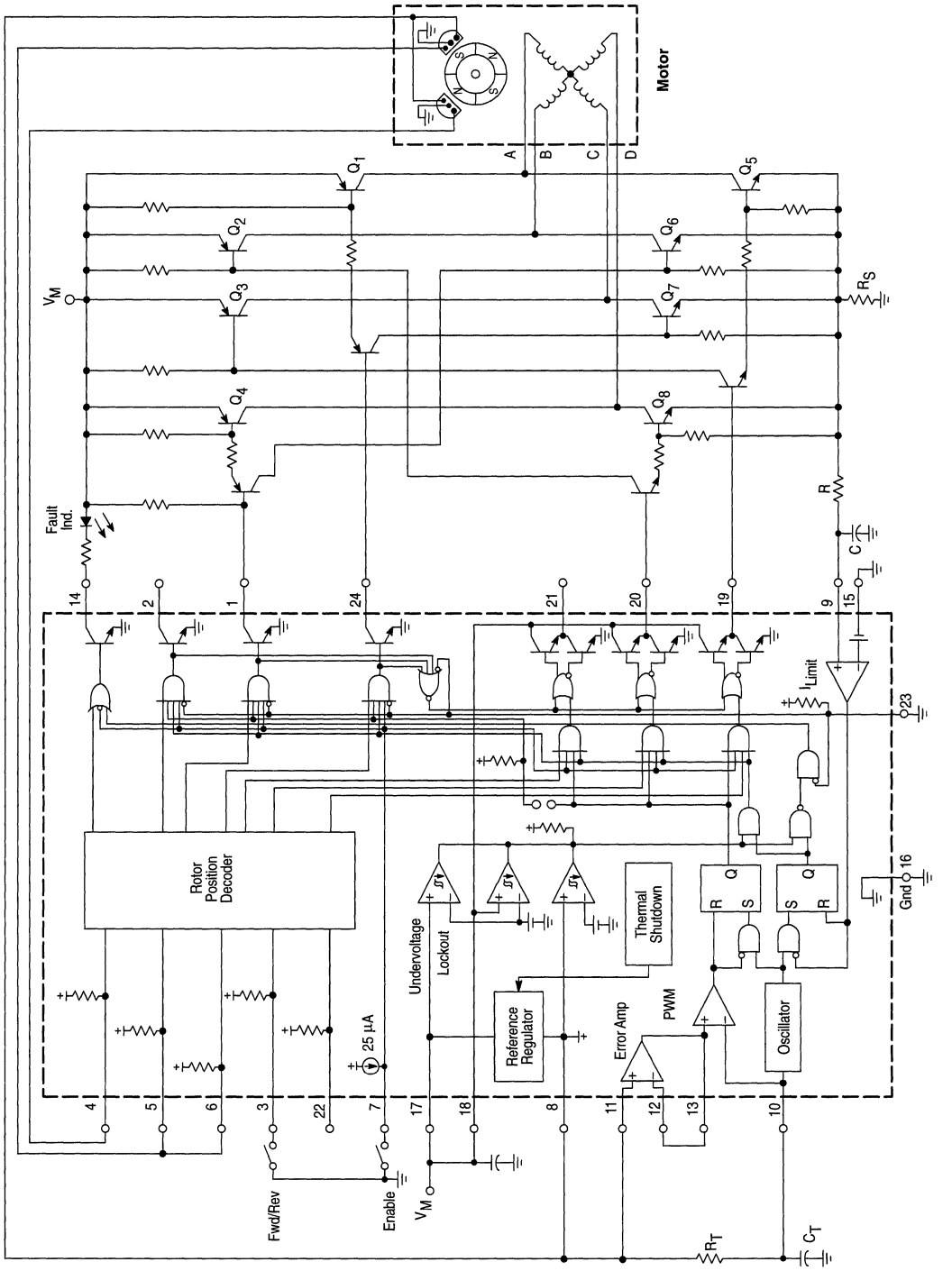
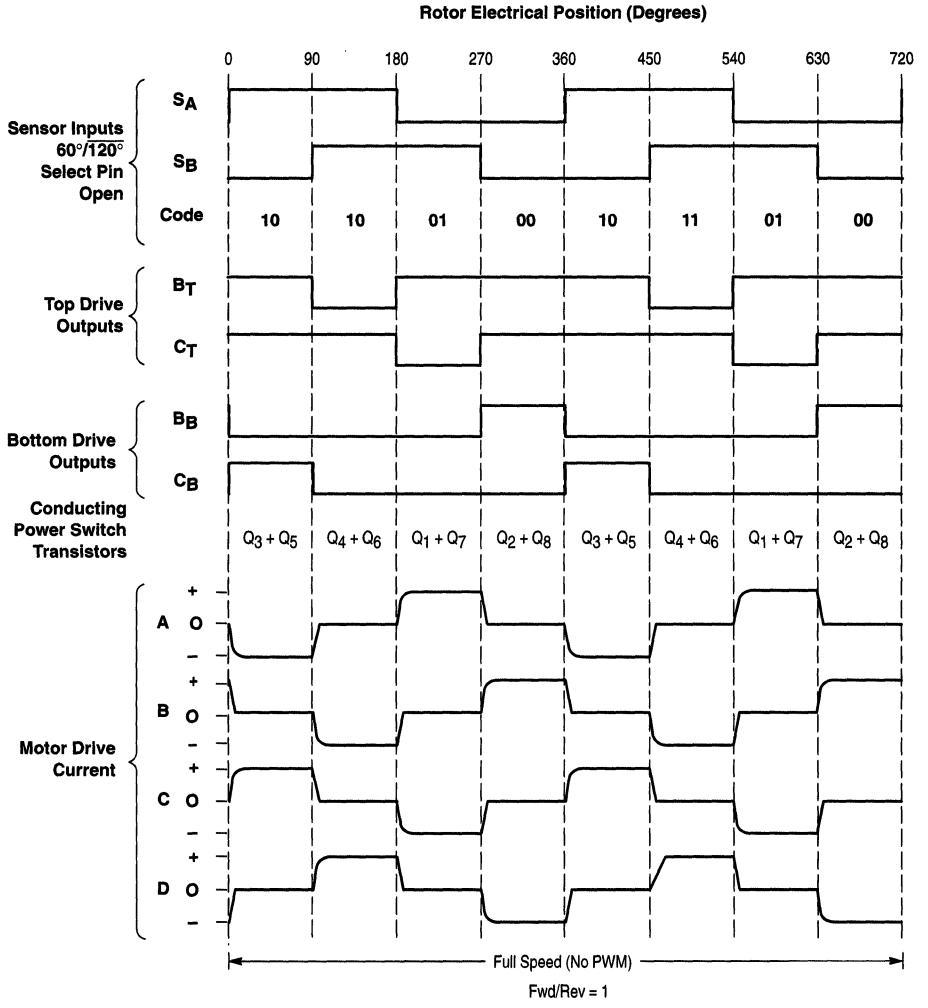


Figure 43. Four Phase, Four Step, Full Wave Motor Controller

4

Figure 44. Four Phase, Four Step, Full Wave Motor Controller



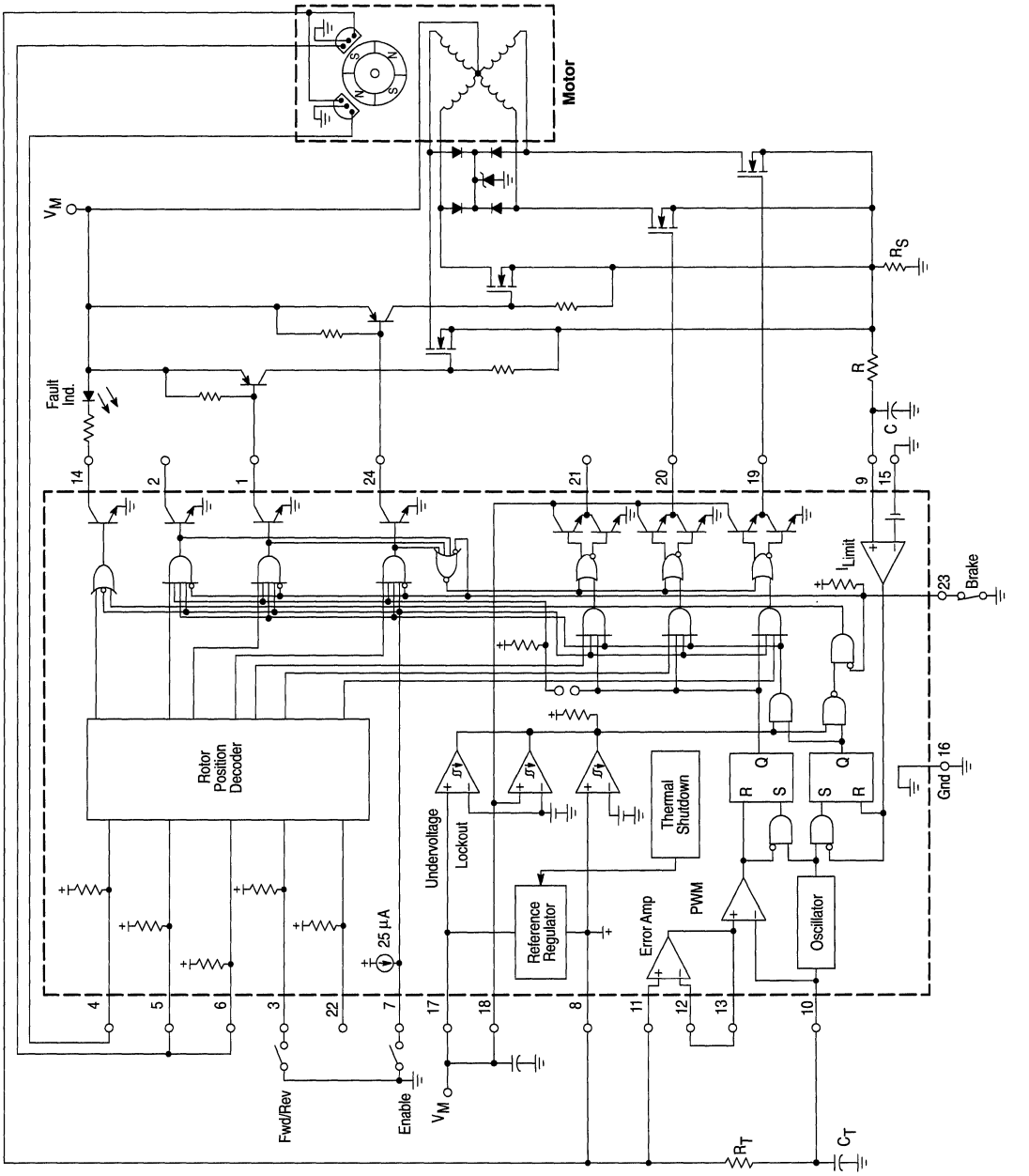


Figure 45. Four Phase, Four Step, Half Wave Motor Controller

Brush Motor Control

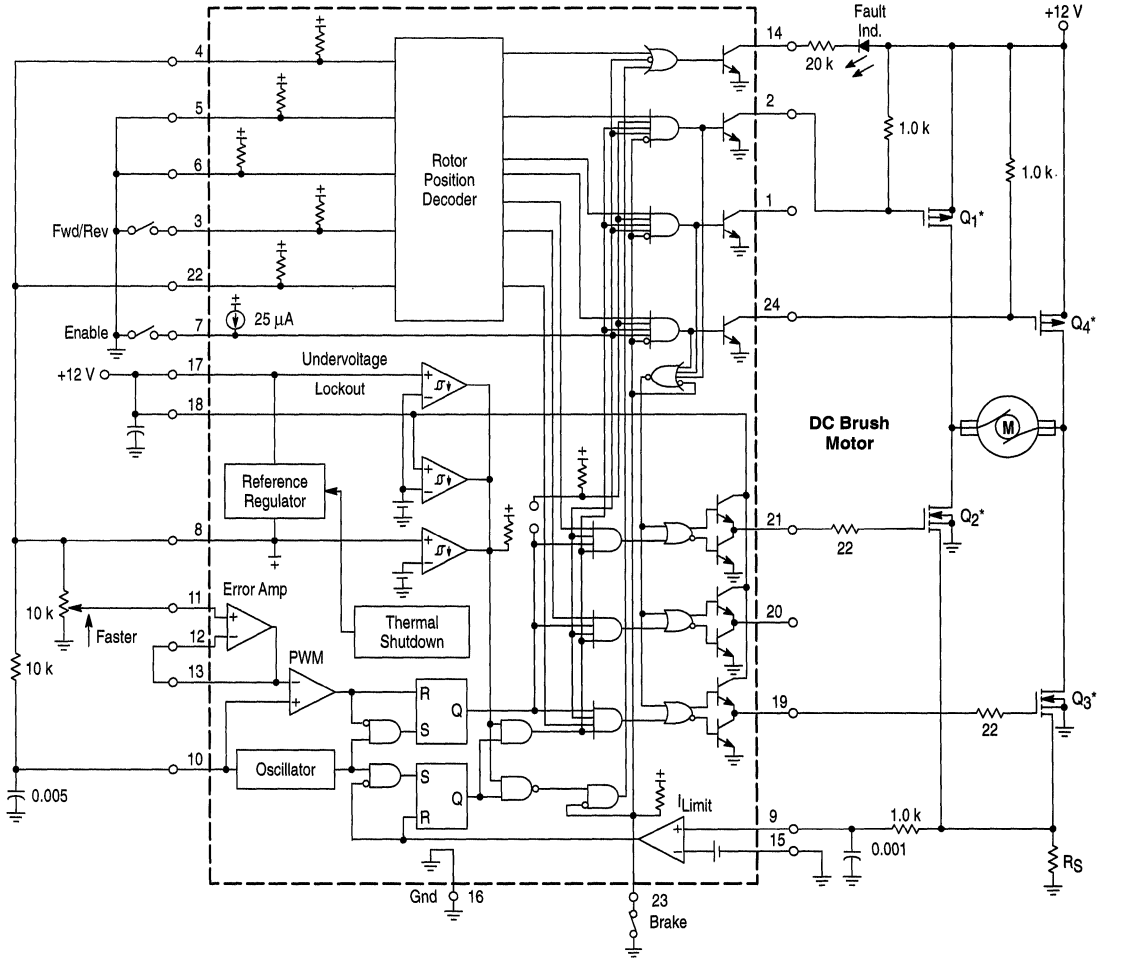
Though the MC33035 was designed to control brushless DC motors, it may also be used to control DC brush type motors. Figure 46 shows an application of the MC33035 driving a MOSFET H–bridge affording minimal parts count to operate a brush–type motor. Key to the operation is the input sensor code [100] which produces a top–left (Q_1) and a bottom–right (Q_3) drive when the controller's forward/reverse pin is at logic [1]; top–right (Q_4), bottom–left (Q_2) drive is realized when the Forward/Reverse pin is at logic [0]. This code supports the requirements necessary for H–bridge drive accomplishing both direction and speed control.

The controller functions in a normal manner with a pulse width modulated frequency of approximately 25 kHz. Motor speed is controlled by adjusting the voltage presented to the noninverting input of the error amplifier establishing the PWM's slice or reference level. Cycle–by–cycle current limiting of the motor current is accomplished by sensing the voltage (100 mV) across the R_S resistor to ground of the H–bridge motor current. The over current sense circuit makes it possible to reverse the direction of the motor, using the normal forward/reverse switch, on the fly and not have to completely stop before reversing.

LAYOUT CONSIDERATIONS

Do not attempt to construct any of the brushless motor control circuits on wire–wrap or plug–in prototype boards. High frequency printed circuit layout techniques are imperative to prevent pulse jitter. This is usually caused by excessive noise pick–up imposed on the current sense or error amp inputs. The printed circuit layout should contain a ground plane with low current signal and high drive and output buffer grounds returning on separate paths back to the power supply input filter capacitor V_M. Ceramic bypass capacitors (0.1 μF) connected close to the integrated circuit at V_{CC}, V_C, V_{ref} and the error amp noninverting input may be required depending upon circuit layout. This provides a low impedance path for filtering any high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI.

Figure 46. H–Bridge Brush–Type Controller



MC33039

Closed Loop Brushless Motor Adapter

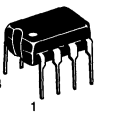
The MC33039 is a high performance closed–loop speed control adapter specifically designed for use in brushless DC motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. This device contains three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33035 brushless motor controller, it can be used cost effectively in many other closed–loop speed control applications.

- Digital Detection of Each Input Transition for Improved Low Speed Motor Operation
- TTL Compatible Inputs With Hysteresis
- Operation Down to 5.5 V for Direct Powering from MC33035 Reference
- Internal Shunt Regulator Allows Operation from a Non–Regulated Voltage Source
- Inverter Output for Easy Conversion between 60°/300° and 120°/240° Sensor Phasing Conventions

CLOSED LOOP BRUSHLESS MOTOR ADAPTER

SEMICONDUCTOR TECHNICAL DATA

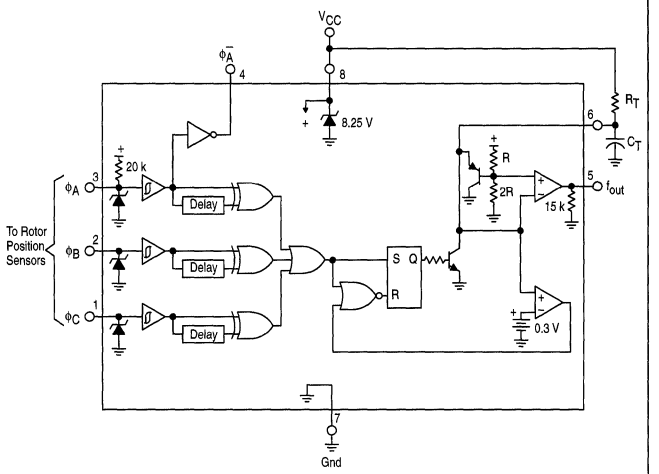
4



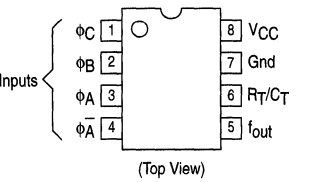
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Representative Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33039D	T_A = – 40° to +85°C	SO–8
MC33039P		Plastic DIP

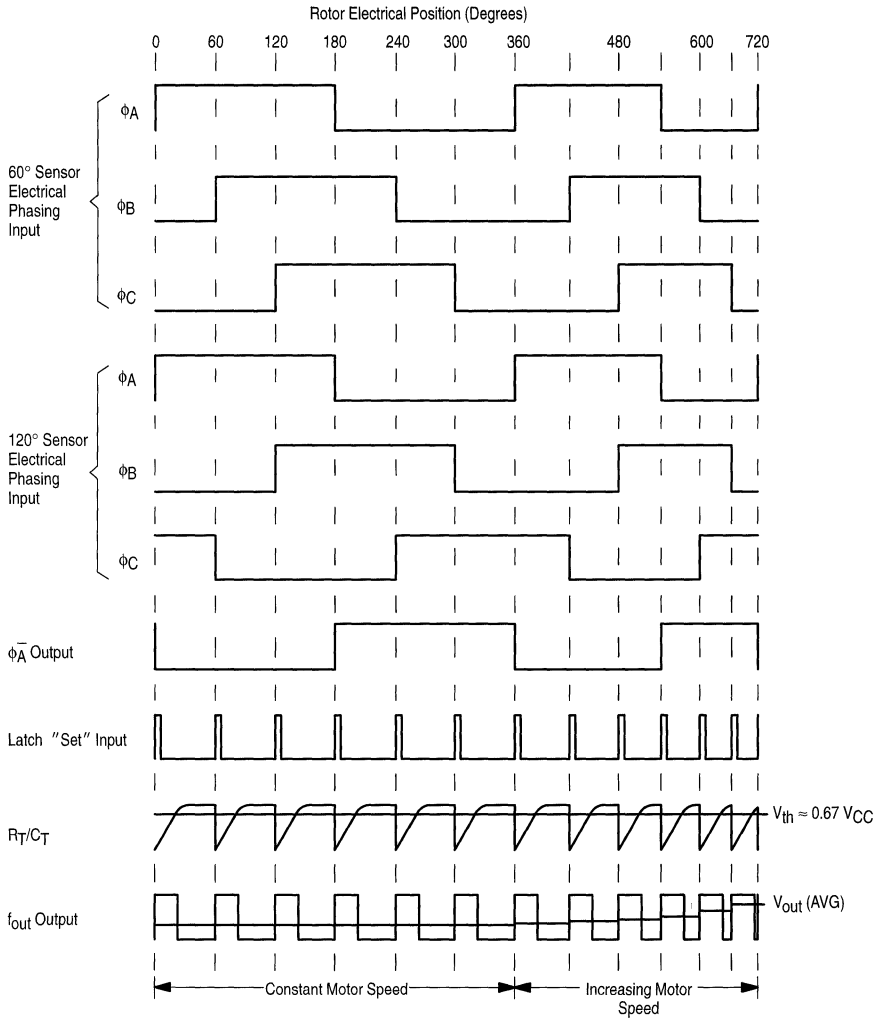
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(V_{CC})}$	30	mA
Logic Input Current (Pins 1, 2, 3)	I_{IH}	5.0	mA
Output Current (Pins 4, 5), Sink or Source	I_{DRV}	20	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = + 85°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$	 650 100	 mW °C/W
Operating Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.25 V, R_T = 10 k, C_T = 22 nF, T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage					V
High State	V_{IH}	2.4	2.1	—	
Low State	V_{IL}	—	1.4	1.0	
Hysteresis	V_H	0.4	0.7	0.9	
Input Current					μA
High State (V_{IH} = 5.0 V)	I_{IH}				
ϕA		– 40	– 60	– 80	
ϕB, ϕC		—	– 0.3	– 5.0	
Low State (V_{IL} = 0 V)	I_{IL}				
ϕA		– 190	– 300	– 380	
ϕB, ϕC		—	– 0.3	– 5.0	
MONOSTABLE AND OUTPUT SECTIONS					
Output Voltage					V
High State	V_{OH}				
f_{out} (I_{source} = 5.0 mA)		3.60	3.95	4.20	
ϕA (I_{source} = 2.0 mA)		4.20	4.75	—	
Low State	V_{OL}				
f_{out} (I_{sink} = 10 mA)		—	0.25	0.50	
ϕA (I_{sink} = 10 mA)		—	0.25	0.50	
Capacitor C_T Discharge Current	I_{dischg}	20	35	60	mA
Output Pulse Width (Pin 5)	t_{PW}	205	225	245	μs
POWER SUPPLY SECTION					
Power Supply Operating Voltage Range (T_A = – 40° to + 85°C)	V_{CC}	5.5	—	V_Z	V
Power Supply Current	I_{CC}	1.8	3.9	5.0	mA
Zener Voltage (I_Z = 10 mA)	V_Z	7.5	8.25	9.0	V
Zener Dynamic Impedance (ΔI_Z = 10 mA to 20 mA, f ≤ 1.0 kHz)	$\lvert Z_{ka} \rvert$	—	2.0	5.0	Ω

Figure 1. Typical Three Phase, Six Step Motor Application



OPERATING DESCRIPTION

The MC33039 provides an economical method of implementing closed–loop speed control of brushless DC motors by eliminating the need for a magnetic or optical tachometer. Shown in the timing diagram of Figure 1, the three inputs (Pins 1, 2, 3) monitor the brushless motor rotor position sensors. Each sensor signal transition is digitally detected, OR'ed at the Latch 'Set' Input, and causes C_T to discharge. A corresponding output pulse is generated at f_{out} (Pin 5) of a defined amplitude, and programmable width determined by the values selected for R_T and C_T (Pin 6). The average voltage of the output pulse train increases with motor speed. When fed through a low pass filter or integrator, a DC voltage proportional to speed is generated. Figure 2 shows the proper connections for a typical closed loop application using the MC33035 brushless motor controller. Constant speed operation down to 100 RPM is possible with economical three phase four pole motors.

The ϕ_A inverter output (Pin 4) is used in systems where the controller and motor sensor phasing conventions are not compatible. A method of converting from either convention to the other is shown in Figure 3. For a more detailed explanation of this subject, refer to the text above Figure 39 on the MC33035 data sheet.

The output pulse amplitude V_{OH} is constant with temperature and controlled by the supply voltage on V_{CC} (Pin 8). Operation down to 5.5 V is guaranteed over temperature. For systems without a regulated power supply, an internal 8.25 V shunt regulator is provided.

Figure 2. Typical Closed Loop Speed Control Application

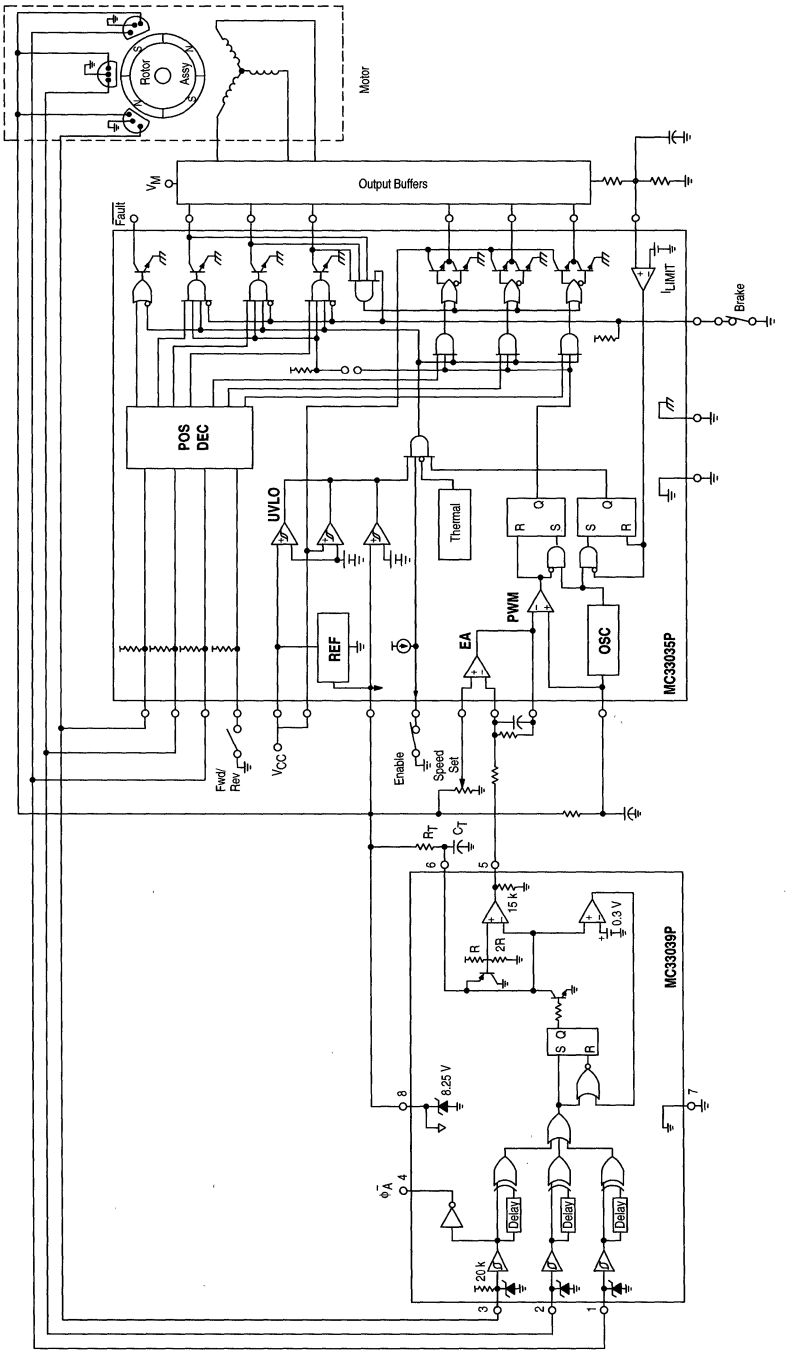


Figure 3. f_{out}, Pulse Width versus Timing Resistor

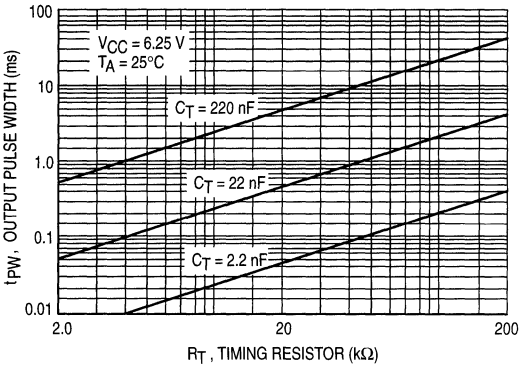


Figure 4. f_{out}, Pulse Width Change versus Temperature

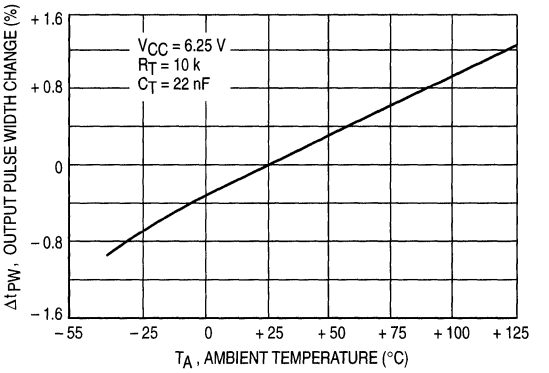


Figure 5. f_{out}, Pulse Width Change versus Supply Voltage

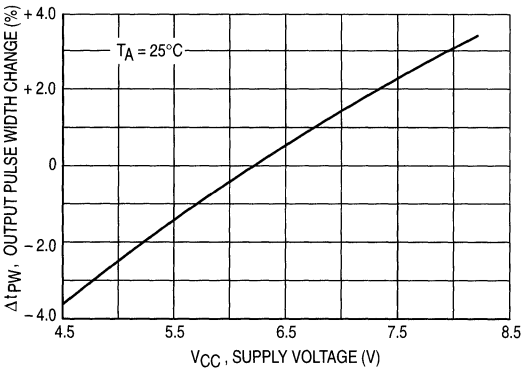


Figure 6. Supply Current versus Supply Voltage

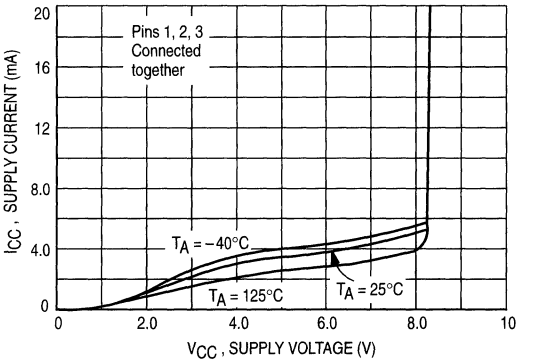


Figure 7. f_{out}, Saturation versus Load Current

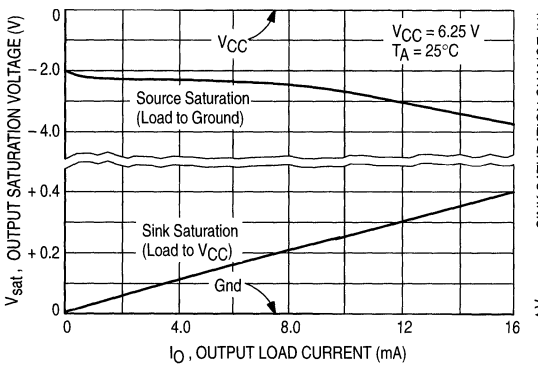
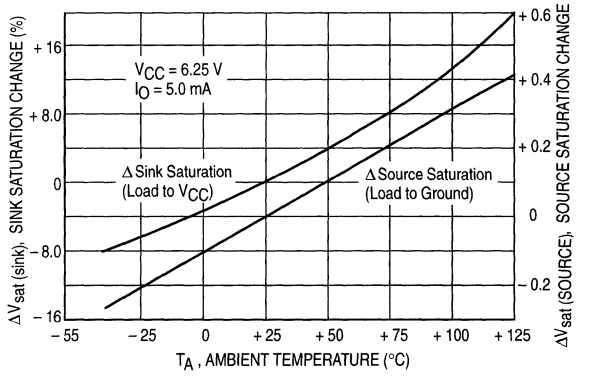


Figure 8. f_{out}, Saturation Change versus Temperature



SAA1042

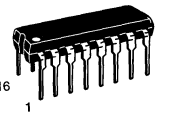
Stepper Motor Driver

The SAA1042 drives a two–phase stepper motor in the bipolar mode. The device contains three input stages, a logic section and two output stages. The IC is contained in a 16 pin dual–in–line heat tab plastic package for improved heatsinking capability. The center four ground pins are connected to the copper alloy heat tab and improve thermal conduction from the die to the circuit board.

- Drive Stages Designed for Motors: 6.0 V and 12 V: SAA1042V
- 500 mA/Coil Drive Capability
- Built–In Clamp Diodes for Overvoltage Suppression
- Wide Logic Supply Voltage Range
- Accepts Commands for CW/CCW and Half/Full Step Operation
- Inputs Compatible with Popular Logic Families: MOS, TTL, DTL
- Set Input Defined Output State
- Drive Stage Bias Adaptable to Motor Power Dissipation for Optimum Efficiency

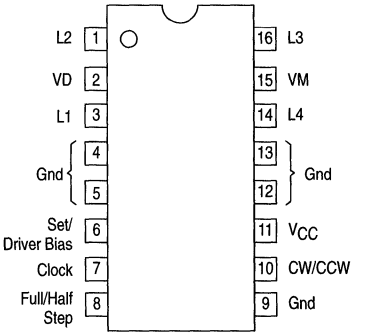
STEPPER MOTOR DRIVER

SEMICONDUCTOR TECHNICAL DATA



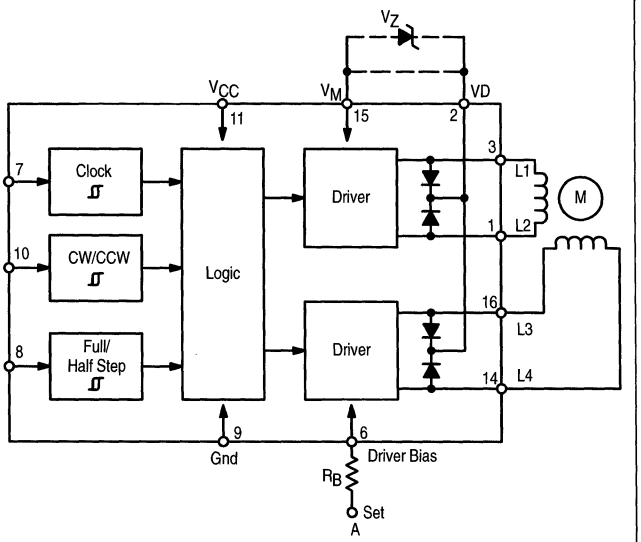
V SUFFIX
PLASTIC PACKAGE
CASE 648C

PIN CONNECTIONS



(Top View)

Figure 1. Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
SAA1042V	$T_J = -30°$ to $+125°C$	Plastic DIP

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	SAA1042V	Unit
Clamping Voltage (Pins 1, 3, 14, 16)	V_{clamp}	20	V
Over Voltage ($V_{OV} = V_{clamp} - V_M$)	V_{OV}	6.0	V
Supply Voltage	V_{CC}	20	V
Switching or Motor Current/Coil	I_M	500	mA
Input Voltage (Pins 7, 8, 10)	V_{in} clock V_{in} Full/Half V_{in} CW/CCW	V_{CC}	V
Power Dissipation (Note 1) Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case	P_D θJA θJC	2.0 80 15	W °C/W
Operating Junction Temperature Range	T_J	–30 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: 1. The power dissipation (P_D) of the circuit is given by the supply voltage (V_M and V_{CC}) and the motor current (I_M), and can be determined from Figures 3 and 5. $P_D = P_{drive} - P_{logic}$.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristics	Pin(s)	Symbol	V_{CC}	Min	Typ	Max	Unit
Supply Current	11	I_{CC}	5.0 V 20 V	— —	— —	3.5 8.5	mA
Motor Supply Current ($I_{Pin\ 6}$ = –400 µA, Pins 1, 3, 14, 16 Open) V_M = 6.0 V V_M = 12 V V_M = 24 V	15	I_M	 5.0 V 5.0 V 5.0 V	 — — —	 25 30 40	 — — —	mA
Input Voltage, High State	7, 8, 10	V_{IH}	5.0 V 10 V 15 V 20 V	2.0 7.0 10 14	— — — —	— — — —	V
Input Voltage, Low State		V_{IL}	5.0 V 10 V 15 V 20 V	— — — —	— — — —	0.8 1.5 2.5 3.5	
Input Reverse Current, High State ($V_{in} = V_{CC}$)	7, 8, 10	I_{IR}	5.0 V 10 V 15 V 20 V	— — — —	— — — —	2.0 2.0 3.0 5.0	µA
Input Forward Current, Low State (V_{in} = Gnd)		I_{IF}	5.0 V 10 V 15 V 20 V	–10 –25 –40 –50	— — — —	— — — —	
Output Voltage, High State (V_M = 12 V) I_{out} = –500 mA I_{out} = –50 mA	1, 3, 14, 16	V_{OH}	5.0 – 20 V	— —	V_M – 2.0 V_M – 1.2	— —	V
Output Voltage, Low State I_{out} = 500 mA I_{out} = 50 mA		V_{OL}	5.0 – 20 V	— —	0.7 0.2	— —	
Output Leakage Current, Pin 6 = Open ($V_M = V_D = V_{clamp\ max}$)	1, 3, 14, 16	I_{DR}	5.0 – 20 V	–100	—	—	µA
Clamp Diode Forward Voltage (Drop at I_M = 500 mA)	2	V_F	—	—	2.5	3.5	V
Clock Frequency	7	f_c	5.0 – 20 V	0	—	50	kHz
Clock Pulse Width	7	t_w	5.0 – 20 V	10	—	—	µs
Set Pulse Width	6	t_s	—	10	—	—	µs
Set Control Voltage, High State Low State	6	—	—	V_M —	— —	— 0.5	V

INPUT/OUTPUT FUNCTIONS

Clock — (Pin 7) This input is active on the positive edge of the clock pulse and accepts Logic '1' input levels dependent on the supply voltage and includes hysteresis for noise immunity.

CW/CCW — (Pin 10) This input determines the motor's rotational direction. When the input is held low, (OV, see the electrical characteristics) the motor's direction is nominally clockwise (CW). When the input is in the high state, Logic '1', the motor direction is nominally counter clockwise (CCW), depending on the motor connections.

Full/Half Step — (Pin 8) This input determines the angular rotation of the motor for each clock pulse. In the low state, the motor will make a full step for each applied clock pulse, while in the high state, the motor will make half a step.

V_D — (Pin 2) This pin is used to protect the outputs (1, 3,14, 16) where large positive spikes occur due to switching the motor coils. The maximum allowable voltage on these pins is the clamp voltage (V_{clamp}). Motor performance is improved if a zener diode is connected between Pin 2 and 15, as shown in Figure 1.

The following conditions have to be considered when selecting the zener diode:

$$V_{clamp} = V_M + 6.0\ V$$
$$V_Z = V_{clamp} - V_M - V_F$$

where: V_F = clamp diodes forward voltage drop (see Figure 4)

V_{clamp}: ≤ 20 V for SAA1042V ≤ 30 V for SAA1042AV

Pins 2 and 15 can be linked, in this case V_Z = 0 V.

Set/Bias Input — (Pin 6) This input has two functions:

1) The resistor R_B adapts the drivers to the motor current.
2) A pulse via the resistor R_B sets the outputs (1, 3, 14, 16) to a defined state.

The resistor R_B can be determined from the graph of Figure 2 according to the motor current and voltage. Smaller values of R_B will increase the power dissipation of the circuit and larger values of R_B may increase the saturation voltage of the driver transistors.

When the "set" function is not used, terminal A of the resistor R_B must be grounded. When the set function is used, terminal A has to be connected to an open–collector (buffer) circuit. Figure 7 shows this configuration. The buffer circuit (off–state) has to sustain the motor voltage (V_M). When a pulse is applied via the buffer and the bias resistor (R_B), the motor driver transistors are turned off during the pulse and after the pulse has ended, the outputs will be in defined states. Figure 6 shows the Timing Diagram.

Figure 7 illustrates a typical application in which the SAA1042 drives a 12 V stepper motor with a current consumption of 200 mA/coil. A bias resistor (R_B) of 56 kΩ is chosen according to Figure 2.

The maximum voltage permitted at the output pin is V_M + 6.0 V (see Maximum Ratings table), in this application V_M = 12 V, therefore the maximum voltage is 18 V. The outputs are protected by the internal diodes and an external zener connected between Pins 2 and 15.

From Figure 4, it can be seen that the voltage drop across the internal diodes is about 1.7 V at 200 mA. This results in a zener voltage between Pins 2 and 15 of:

$$V_Z = 6.0\ V - 1.7\ V = 4.3\ V.$$

To allow for production tolerances and a safety margin, a 3.9 V zener has been chosen for this example.

The clock is derived from the line frequency which is phase–locked by the MC14046B and the MC14024. The voltage on the clock input is normally low (Logic '0'). The motor steps on the positive going transition of the clock pulse.

The Logic '0' applied to the Full/Half input (Pin 8) operates the motor in Full Step mode. A Logic '1' at this input will result in Half Step mode. The logic level state on the CW/CCW input (Pin 10), and the connection of the motor coils to the outputs determines the rotational direction of the motor.

These two inputs should be biased to a Logic '0' or '1' and not left floating. In the event of non–use, they should be tied to ground or the logic supply line, V_{CC}.

The output drivers can be set to a fixed operating point by use of the Set input and a bias resistor, R_B. A positive pulse to this input turns the drivers off and sets the logic state of the outputs.

After the negative going transition of the Set pulse, and until the first positive going transition of the clock, the outputs will be:

L1 = L3 = high and L2 = L4 = low, (see Figure 6).

The Set input can be driven by a MC14007B or a transistor whose collector resistor is R_B. **If the input is not used, the bottom of R_B must be grounded.**

The total power dissipation of the circuit can be determined from Figures 3 and 5:

$$P_D = 0.9\ W + 0.08\ W = 0.98\ W.$$

The junction temperature can then be computed using Figure 8.

Figure 2. Bias Resistor R_B versus Motor Current

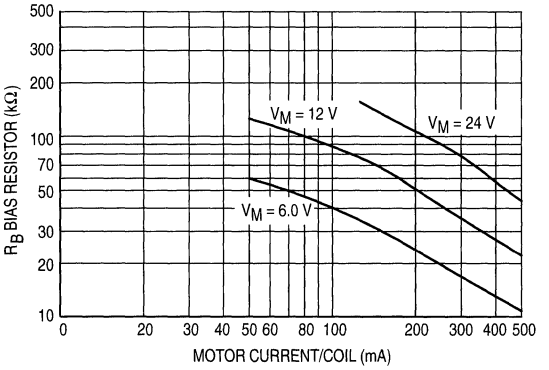


Figure 3. Drive Stage Power Dissipation

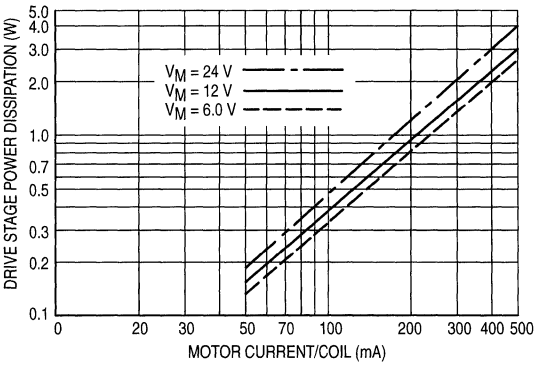


Figure 4. Clamp Diode Forward Current versus Forward Voltage

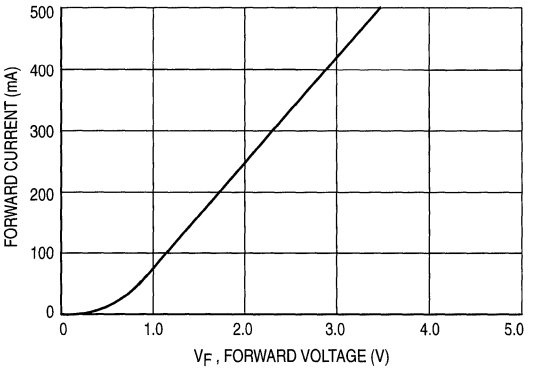


Figure 5. Power Dissipation versus Logic Supply Voltage

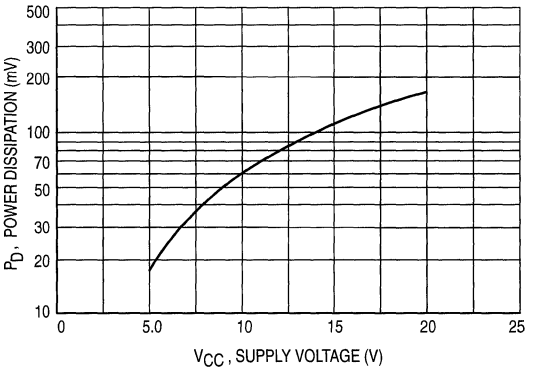


Figure 6. Timing Diagram

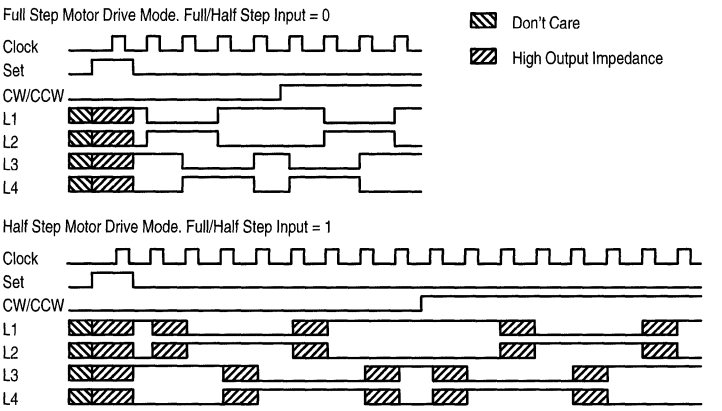


Figure 7. Typical Application
Selectable Step Rates with the Time Base Derived from the Line Frequency

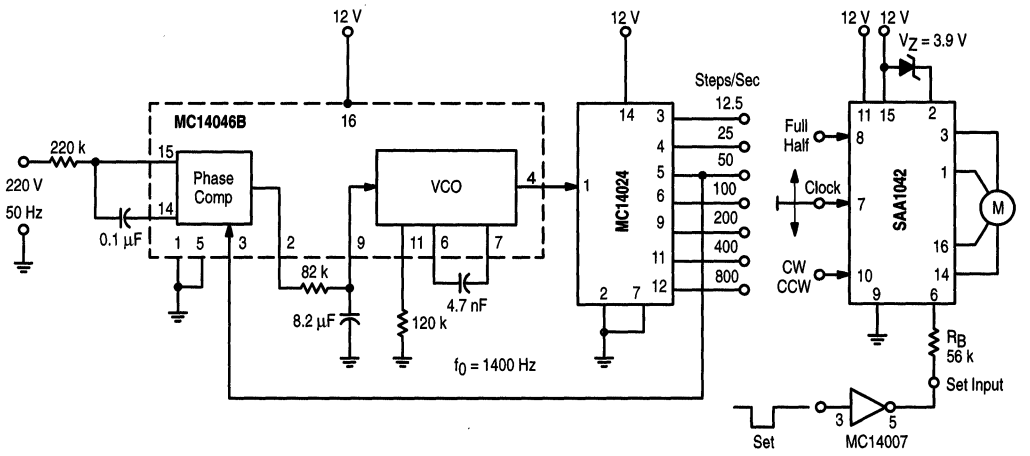
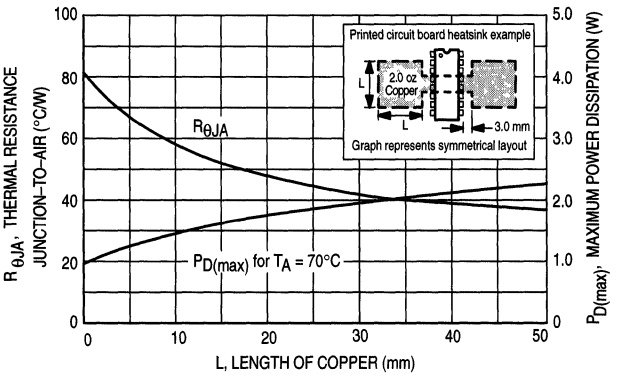


Figure 8. Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MOTOROLA

TDA1085C

Universal Motor Speed Controller

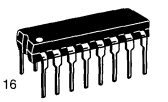
The TDA1085C is a phase angle triac controller having all the necessary functions for universal motor speed control in washing machines. It operates in closed loop configuration and provides two ramp possibilities.

- On–Chip Frequency to Voltage Converter
- On–Chip Ramps Generator
- Soft–Start
- Load Current Limitation
- Tachogenerator Circuit Sensing
- Direct Supply from AC Line
- Security Functions Peformed by Monitor

UNIVERSAL MOTOR SPEED CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

4



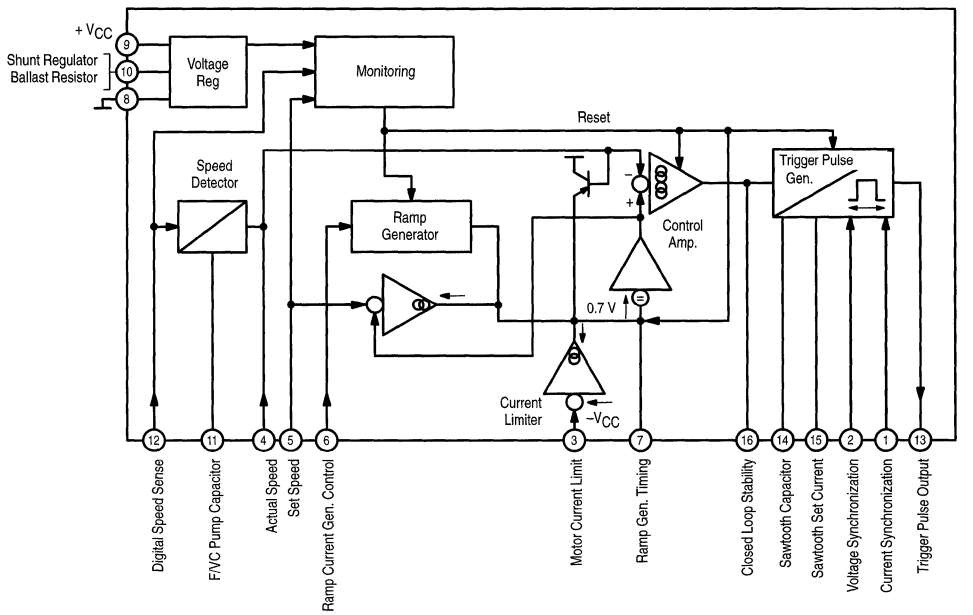
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
TDA1085CD	$T_J = -10°$ to $+120°C$	SO–16
TDA1085C		Plastic DIP

Figure 1. Representative Block Diagram and Pin Connections



MAXIMUM RATINGS (T_A = 25°C, voltages are referenced to Pin 8, ground)

Rating	Symbol	Value	Unit
Power Supply, when externally regulated, $V_{Pin\ 9}$	V_{CC}	15	V
Maximum Voltage per listed pin Pin 3 Pin 4–5–6–7–13–14–16 Pin 10	V_{Pin}	 + 5.0 0 to + V_{CC} 0 to + 17	V
Maximum Current per listed pin Pin 1 and 2 Pin 3 Pin 9 (V_{CC}) Pin 10 shunt regulator Pin 12 Pin 13	I_{Pin}	 – 3.0 to + 3.0 – 1.0 to + 0 15 35 – 1.0 to + 1.0 – 200	mA
Maximum Power Dissipation	P_D	1.0	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	65	°C/W
Operating Junction Temperature	T_J	– 10 to + 120	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR					
Internally Regulated Voltage ($V_{Pin\ 9}$) ($I_{Pin\ 7}$ = 0, $I_{Pin\ 9}$ + $I_{Pin\ 10}$ = 15 mA, $I_{Pin\ 13}$ = 0)	V_{CC}	15	15.3	15.6	V
V_{CC} Temperature Factor	TF	—	– 100	—	ppm/°C
Current Consumption ($I_{Pin\ 9}$) (V_9 = 15 V, V_{12} = V_8 = 0, I_1 = I_2 = 100 μA, all other pins not connected)	I_{CC}	—	4.5	6.0	mA
V_{CC} Monitoring Enable Level Disable Level	V_{CC} EN V_{CC} DIS	— —	V_{CC} – 0.4 V_{CC} – 1.0	— —	V
RAMP GENERATOR					
Reference Speed Input Voltage Range	$V_{Pin\ 5}$	0.08	—	13.5	V
Reference Input Bias Current	– $I_{Pin\ 5}$	0	0.8	1.0	μA
Ramp Selection Input Bias Current	– $I_{Pin\ 6}$	0	—	1.0	μA
Distribution Starting Level Range	V_{DS}	0	—	2.0	V
Distribution Final Level $V_{Pin\ 6}$ = 0.75 V	V_{DF}/V_{DS}	2.0	2.09	2.2	
High Acceleration Charging Current $V_{Pin\ 7}$ = 0 V $V_{Pin\ 7}$ = 10 V	– $I_{Pin\ 7}$	 1.0 1.0	 — 1.2	 1.7 1.4	mA
Distribution Charging Current $V_{Pin\ 7}$ = 2.0 V	– $I_{Pin\ 7}$	4.0	5.0	6.0	μA

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT LIMITER					
Limiter Current Gain — $I_{Pin\ 7}/I_{Pin\ 3}$ ($I_{Pin3} = -\ 300\ \mu A$)	C_g	130	180	250	
Detection Threshold Voltage $I_{Pin\ 3} = -\ 10\ \mu A$	$V_{Pin\ 3\ TH}$	50	65	80	mV
FREQUENCY TO VOLTAGE CONVERTER					
Input Signal "Low Voltage" Input Signal "High Voltage" Monitoring Reset Voltage	$V_{12\ L}$ $V_{12\ H}$ $V_{12\ R}$	−100 +100 5.0	— — —	— — —	mV mV V
Negative Clamping Voltage $I_{Pin\ 12} = -\ 200\ \mu A$	$-V_{12\ CL}$	—	0.6	—	V
Input Bias Current	$-I_{Pin12}$	—	25	—	μA
Internal Current Source Gain $G = \frac{I_{Pin\ 4}}{I_{Pin\ 11}}, V_{Pin\ 4} = V_{Pin\ 11} = 0$	G.0	9.5	—	11	
Gain Linearity versus Voltage on Pin 4 ($G_{8.6}$ = Gain for $V_{Pin\ 4} = 8.6$ V) $V_4 = 0$ V $V_4 = 4.3$ V $V_4 = 12$ V	$G/G_{8.6}$	 1.04 1.015 0.965	 1.05 1.025 0.975	 1.06 1.035 0.985	
Gain Temperature Effect ($V_{Pin\ 4} = 0$)	TF	—	350	—	ppm/°C
Output Leakage Current ($I_{Pin\ 11} = 0$)	$-I_{Pin\ 4}$	0	—	100	nA
CONTROL AMPLIFIER					
Actual Speed Input Voltage Range	$V_{Pin\ 4}$	0	—	13.5	V
Input Offset Voltage $V_{Pin\ 5} - V_{Pin\ 4}$ ($I_{Pin\ 16} = 0$, $V_{Pin\ 16} = 3.0$ and 8.0 V)	V_{off}	0	—	50	mV
Amplifier Transconductance ($I_{Pin\ 16}/\Delta\ (V_5 - V_4)$ ($I_{Pin\ 16} = +$ and $-\ 50\ \mu A$, $V_{Pin\ 16} = 3.0$ V)	T	270	340	400	μA/V
Output Current Swing Capability Source Sink	$I_{Pin\ 16}$	 − 200 50	 − 100 100	 − 50 200	μA
Output Saturation Voltage	$V_{16\ sat}$	—	—	0.8	V
TRIGGER PULSE GENERATOR					
Synchronization Level Currents Voltage Line Sensing Triac Sensing	 $I_{Pin\ 2}$ $I_{Pin\ 1}$	 — —	 ± 50 ± 50	 ± 100 ± 100	μA
Trigger Pulse Duration ($C_{Pin\ 14} = 47$ nF, $R_{Pin\ 15} = 270$ kΩ)	T_p	—	55	—	μs
Trigger Pulse Repetition Period, conditions as a.m.	T_R	—	220	—	μs
Output Pulse Current $V_{Pin\ 13} = V_{CC} - 4.0$ V	$-I_{Pin\ 13}$	180	192	—	mA
Output Leakage Current $V_{Pin\ 13} = -\ 3.0$ V	$I_{13\ L}$	—	—	30	μA
Full Angle Conduction Input Voltage	V_{14}	—	11.7	—	V
Saw Tooth "High" Level Voltage	$V_{14\ H}$	12	—	12.7	V
Saw Tooth Discharge Current, $I_{Pin15} = 100\ \mu A$	$I_{Pin\ 14}$	95	—	105	μA

GENERAL DESCRIPTION

The TDA 1085C triggers a triac accordingly to the speed regulation requirements. Motor speed is digitally sensed by a tachogenerator and then converted into an analog voltage.

The speed set is externally fixed and is applied to the internal linear regulation input after having been submitted to programmable acceleration ramps. The overall result consists in a full motor speed range with two acceleration ramps which allow efficient washing machine control (Distribute function).

Additionally, the TDA 1085C protects the whole system against AC line stop or variations, overcurrent in the motor and tachogenerator failure.

INPUT/OUTPUT FUNCTIONS (Refer to Figures 1 and 8)

4

Voltage Regulator – (Pins 9 and 10) This is a parallel type regulator able to sink a large amount of current and offering good characteristics. Current flow is provided from AC line by external dropping resistors R1, R2, and rectifier: This half wave current is used to feed a smoothering capacitor, the voltage of which is checked by the IC.

When V_{CC} is reached, the excess of current is derived by another dropping resistor R10 and by Pin 10. These three resistors must be determined in order:

- To let 1.0 mA flow through Pin 10 when AC line is minimum and V_{CC} consumption is maximum (fast ramps and pulses present).
- To let V_{10} reach 3.0 V when AC line provides maximum current and V_{CC} consumption is minimum (no ramps and no pulses).
- All along the main line cycle, the Pin 10 dynamic range must not be exceeded unless loss of regulation.

An AC line supply failure would cause shut down.

The double capacitive filter built with R1 and R2 gives an efficient V_{CC} smoothing and helps to remove noise from set speeds.

Speed Sensing – (Pins 4, 11, 12) The IC is compatible with an external analog speed sensing: its output must be applied to Pin 4, and Pin 12 connected to Pin 8.

In most of the applications it is more convenient to use a digital speed sensing with an unexpensive tachogenerator which doesn't need any tuning. During every positive cycle at Pin 12, the capacitor $C_{Pin\ 11}$ is charged to almost V_{CC} and during this time, Pin 4 delivers a current which is 10 times the one charging $C_{Pin\ 11}$. The current source gain is called G and is tightly specified, but nevertheless requires an adjustment on $R_{Pin\ 4}$. The current into this resistor is proportional to $C_{Pin\ 11}$ and to the motor speed; being filtered by a capacitor, $V_{Pin\ 4}$ becomes smothered and represents the "true actual motor speed".

To maintain linearity into the high speed range, it is important to verify that $C_{Pin\ 11}$ is fully charged: the internal source on Pin 11 has 100 KΩ impedance. Nevertheless $C_{Pin\ 11}$ has to be as high as possible as it has a large influence on FV/C temperature factor. A 470 KΩ resistor between Pins 11 and 9 reduces leakage currents and temperature factor as well, down to neglectable effects.

Pin 12 also has a monitoring function: when its voltage is above 5.0 V, the trigger pulses are inhibited and the IC is reset. It also senses the tachogenerator continuity, and in case of any circuit aperture, it inhibits pulse, avoiding the motor to run out of control. In the TDA 1085C, Pin 12 is negatively clamped by an internal diode which removes the necessity of the external one used in the former circuit.

Ramp Generator – (Pins 5, 6, 7) The true Set Speed value taken in consideration by the regulation is the output of the ramp generator (Pin 7). With a given value of speed set input (Pin 5), the ramp generator charges an external capacitor $C_{Pin\ 7}$ up to the moment $V_{Pin\ 5}$ (set speed) equals $V_{Pin\ 4}$ (true speed), see Figure 2. The IC has an internal charging current source of 1.2mA and delivers it from 0 to 12 V at Pin 7. It is the high acceleration ramp (5.0 s typical) which allows rapid motor speed changes without excessive strains on the mechanics. In addition, the TDA 1085C offers the possibility to break this high acceleration with the introduction of a low acceleration ramp (called Distribution) by reducing the Pin 7 source current down to 5.0 µA under Pin 6 full control, as shown by following conditions:

- Presence of high acceleration ramp $V_{Pin\ 5} > V_{Pin\ 4}$
- Distribution occurs in the $V_{Pin\ 4}$ range (true motor speed) defined by $V_{Pin\ 6} \leqq V_{Pin\ 4} \leqq 2.0\ V_{Pin\ 6}$

For two fixed values of $V_{Pin\ 5}$ and $V_{Pin\ 6}$, the motor speed will have high acceleration, excluding the time for $V_{Pin\ 4}$ to go from $V_{Pin\ 6}$ to two times this value, high acceleration again, up to the moment the motor has reached the set speed value, at which it will stay, see Figure 3.

Should a reset happen (whatever the cause would be), the above mentioned successive ramps will be fully reprocessed from 0 to the maximum speed. If $V_{Pin\ 6} = 0$, only the high acceleration ramp occurs.

To get a real zero speed position, Pin 5 has been designed in such a way that its voltage from 0 to 80 mV is interpreted as a true zero. As a consequence, when changing the speed set position, the designer must be sure that any transient zero would not occur: if any, the entire circuit will be reset.

As the voltages applied by Pins 5 and 6 are derived from the internal voltage regulator supply and Pin 4 voltage is also derived from the same source, motor speed (which is determined by the ratios between above mentioned voltages) is totally independent from V_{CC} variations and temperature factor.

Control Amplifier – (Pin 16) It amplifies the difference between true speed (Pin 4) and set speed (Pin 5), through the ramp generator. Its output available at Pin 16 is a double sense current source with a maximum capability of ± 100 µA and a specified transconductance (340 µA/V typical). Pin 16 drives directly the trigger pulse generator, and must be loaded by an electrical network which compensates the mechanical characteristics of the motor and its load, in order to provide stability in any condition and shortest transient response; see Figure 4.

This network must be adjusted experimentally.

In case of a periodic torque variations, Pin 16 directly provides the phase angle oscillations.

Trigger Pulse Generator – (Pins 1, 2, 5, 13, 14, 15)
This circuit performs four functions:

- The conversion of the control amplifier DC output level to a proportional firing angle at every main line half cycle.
- The calibration of pulse duration.
- The repetition of the pulse if the triac fails to latch on if the current has been interrupted by brush bounce.
- The delay of firing pulse until the current crosses zero at wide firing angles and inductive loads.

$R_{Pin\ 15}$ programs the Pin 14 discharging current. Saw tooth signal is then fully determined by R15 and C14 (usually 47 nF). Firing pulse duration and repetition period are in inverse ratio to the saw tooth slope.

Pin 13 is the pulse output and an external limiting resistor is mandatory. Maximum current capability is 200 mA.

Current Limiter – (Pin 3) Safe operation of the motor and triac under all conditions is ensured by limiting the peak current. The motor current develops an alternative voltage in the shunt resistor (0.05 Ω in Figure 4). The negative half waves are transferred to Pin 3 which is positively preset at a voltage determined by resistors R3 and R4. As motor current increases, the dynamical voltage range of Pin 3 increases and when Pin 3 becomes slightly negative in respect to Pin 8, a current starts to circulate in it. This current, amplified typically 180 times, is then used to discharge Pin 7 capacitor and, as a result, reduces firing angle down to a value where an equilibrium is reached. The choice of resistors R3, R4 and shunt determines the magnitude of the discharge current signals on $C_{Pin\ 7}$.

Notice that the current limiter acts only on peak triac current.

4

APPLICATION NOTES
(Refer to Figure 4)

Printed Circuit Layout Rules
In the common applications, where TDA 1085C is used, there is on the same board, presence of high voltage, high currents as well as low voltage signals where millivolts count. It is of first magnitude importance to separate them from each other and to respect the following rules:

- Capacitor decoupling pins, which are the inputs of the same comparator, must be physically close to the IC, close to each other and grounded in the same point.
- Ground connection for tachogenerator must be directly connected to Pin 8 and should ground only the tacho. In effect, the latter is a first magnitude noise generator due to its proximity to the motor which induces high $d\phi/dt$ signals.
- The ground pattern must be in the "star style" in order to fully eliminate power currents flowing in the ground network devoted to capacitors decoupling sensitive Pins: 4, 5, 7, 11, 12, 14, 16.

As an example, Figure 5 presents a PC board pattern which concerns the group of sensitive Pins and their associated capacitors into which the a.m. rules have been implemented. Notice the full separation of "Signal World" from "Power", one by line AB and their communication by a unique strip.

These rules will lead to much satisfactory volume production in the sense that speed adjustment will stay valid in the entire speed range.

Power Supply
As dropping resistor dissipates noticeable power, it is necessary to reduce the I_{CC} needs down to a minimum. Triggering pulses, if a certain number of repetitions are kept in reserve to cope with motor brush wearing at the end of its life, are the largest I_{CC} user. Classical worst case configuration has to be considered to select dropping resistor. In addition, the parallel regulator must be always into its dynamic range, i.e., $I_{Pin\ 10}$ over 1.0 mA and $V_{Pin\ 10}$ over 3.0 V in any extreme configuration. The double filtering cell is mandatory.

Tachogenerator Circuit
The tacho signal voltage is proportional to the motor speed. Stablility considerations, in addition, require an RC filter, the pole of which must be looked at. The combination of both elements yield a constant amplitude signal on Pin 12 in most of the speed range. It is recommended to verify this maximum amplitude to be within 1.0 V peak in order to have the largest signal/noise ratio without resetting the integrated circuit (which occurs if $V_{Pin\ 12}$ reaches 5.5 V). It must be also verified that the Pin 12 signal is approximately balanced between "high" (over 300 mV) and "low". An 8–poles tacho is a minimum for low speed stability and a 16–poles is even better.

The RC pole of the tacho circuit should be chosen within 30 Hz in order to be as far as possible from the 150 Hz which corresponds to the AC line 3rd harmonic generated by the motor during starting procedure. In addition, a high value resistor coming from V_{CC} introduces a positive offset at Pin 12, removes noise to be interpreted as a tacho signal. This offset should be designed in order to let Pin 12 reach at least – 200 mV (negative voltage) at the lowest motor speed. We remember the necessity of an individual tacho ground connection.

Frequency to Voltage Converter – F V/C
$C_{Pin\ 11}$ has a recommended value of 820 pF for 8–poles tachos and maximum motor rpm of 15000, and $R_{Pin\ 11}$ must be always 470 K.

$R_{Pin\ 4}$ should be choosen to deliver within 12 V at maximum motor speed in order to maximize signal/noise ratio. As the FV/C ratio as well as the $C_{Pin\ 11}$ value are dispersed, $R_{Pin\ 4}$ must be adjustable and should be made of a fixed resistor in serice with a trimmer representing 25% of the total. Adjustment would become easier.

Once adjusted, for instance at maximum motor speed, the FV/C presents a residual non linearity; the conversion factor (mV per RPM) increases by within 7.7% as speed draws to zero. The guaranteed dispersion of the latter being very narrow, a maximum 1% speed error is guaranteed if during Pin 5 network design the small set values are modified, once forever, according this increase.

The following formulas give $V_{Pin\ 4}$:

$$V_{Pin\ 4} = G.0 \cdot (V_{CC} - V_a) \cdot C_{Pin\ 11} \cdot R_4 \cdot f \cdot \frac{1}{\left(1 + \frac{120k}{R_{Pin11}}\right)} \text{ In volts.}$$

$G.0 \cdot (V_{CC} - V_a) \simeq 140$
$V_a = 2.0\ V_{BE}$
$120\ k = R_{int}$, on Pin 11

Speed Set – (Pin 5) Upon designer choice, a set of external resistors apply a series of various voltages corresponding to the various motor speeds. When switching external resistors, verify that no voltage below 80 mV is ever applied to Pin 5. If so, a full circuit reset will occur.

Ramps Generator – (Pin 6) If only a high acceleration ramp is needed, connect Pin 6 to ground.

When a Distribute ramp should occur, preset a voltage on Pin 6 which corresponds to the motor speed starting ramp point. Distribution (or low ramp) will continue up to the moment the motor speed would have reached twice the starting value.

The ratio of two is imposed by the IC. Nevertheless, it could be externally changed downwards (Figure 6) or upwards (Figure 7).

The distribution ramp can be shortened by an external resistor from V_{CC} charging $C_{Pin\ 7}$, adding its current to the internal 5.0 µA generator.

4

Power Circuits
Triac Triggering pulse amplitude must be determined by Pin 13 resistor according to the needs in Quadrant IV. Trigger pulse duration can be disturbed by noise signals generated by the triac itself, which interfere within Pins 14 and 16, precisely those which determine it. While easily visible, this effect is harmless.

The triac must be protected from high AC line dV/dt during external disturbances by 100 nF x 100 Ω network.

Shunt resistor must be as non–inductive as possible. It can be made locally by using constantan alloy wire.

When the load is a DC fed universal motor through a rectifier bridge, the triac must be protected from commutating dV/dt by a 1.0 to 2.0 mH coil in series with MT_2.

Synchronization functions are performed by resistors sensing AC line and triac conduction. 820 k values are normal but could be reduced down to 330 k in order to detect the "zeros" with accuracy and to reduce the residual DC line component below 20 mA.

Current Limitation
The current limiter starts to discharge Pin 7 capacitor (reference speed) as the motor current reaches the designed threshold level. The loop gain is determined by the resistor connecting Pin 3 to the series shunt. Experience has shown that its optimal value for a 10 Arms limitation is within 2.0 kΩ. Pin 3 input has a sensitivity in current which is limited to reasonable values and should not react to spikes.

If not used, Pin 3 must be connected to a maximum positive voltage of 5.0 V rather than be left open.

Loop Stability
The Pin 16 network is predominant and must be adjusted experimentally during module development. The values indicated in Figure 4 are typical for washing machine applications but accept large modifications from one model to another. R16 (the sole restriction) should not go below 33 k, otherwise slew rate limitation will cause large transient errors for load steps.

Figure 2. Acceleration Ramp

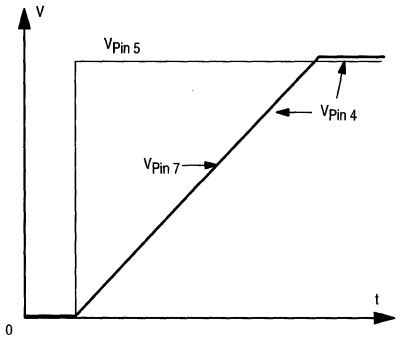


Figure 3. Programmable Double Acceleration Ramp

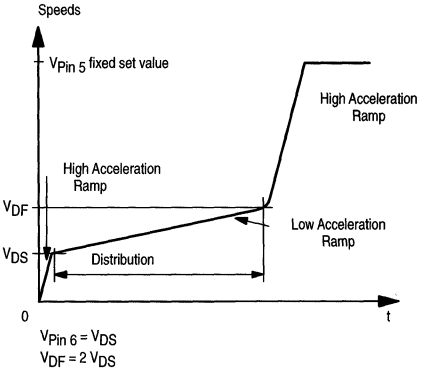
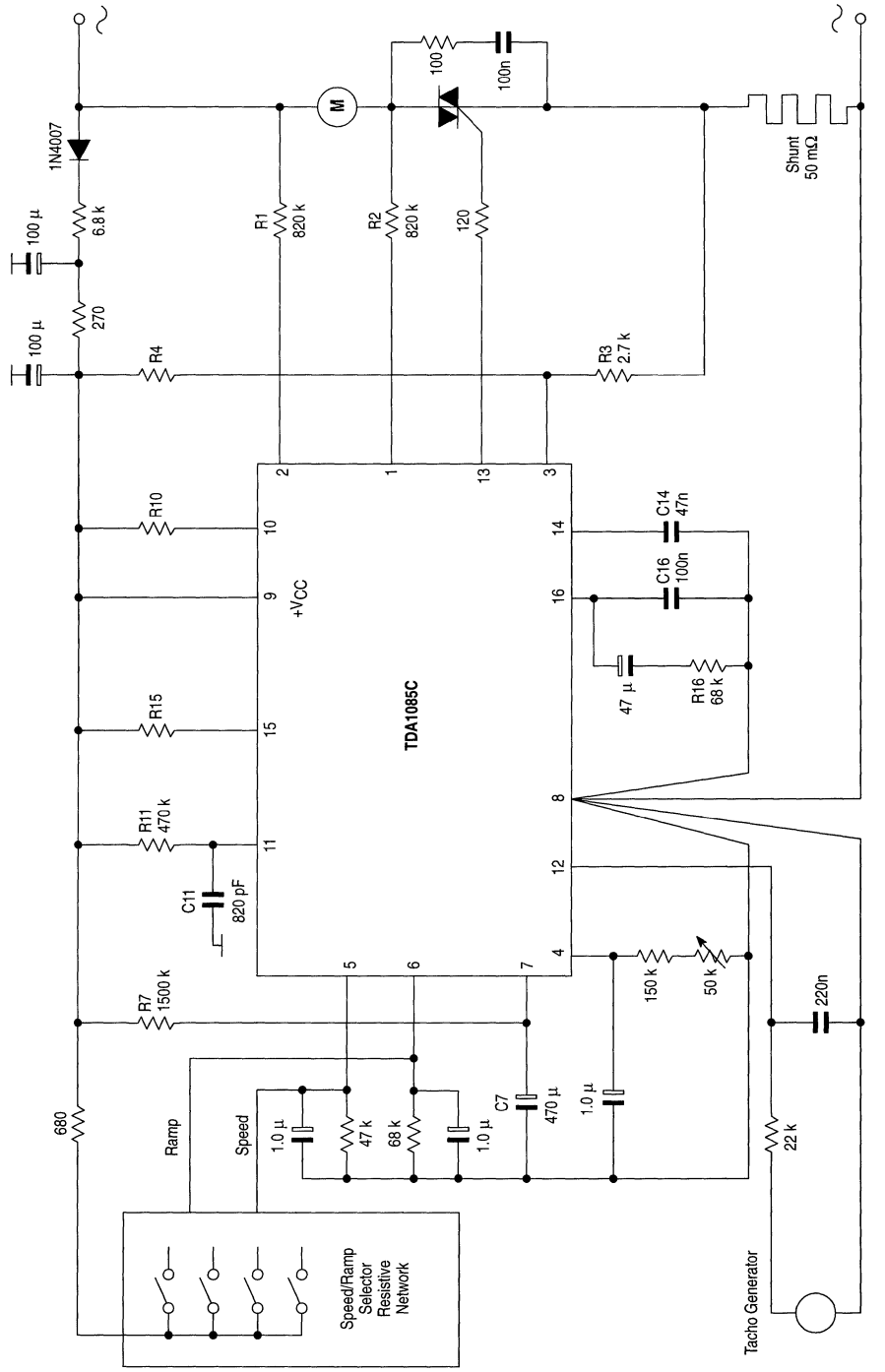


Figure 4. Basic Application Circuit



4

Figure 5. PC Board Layout

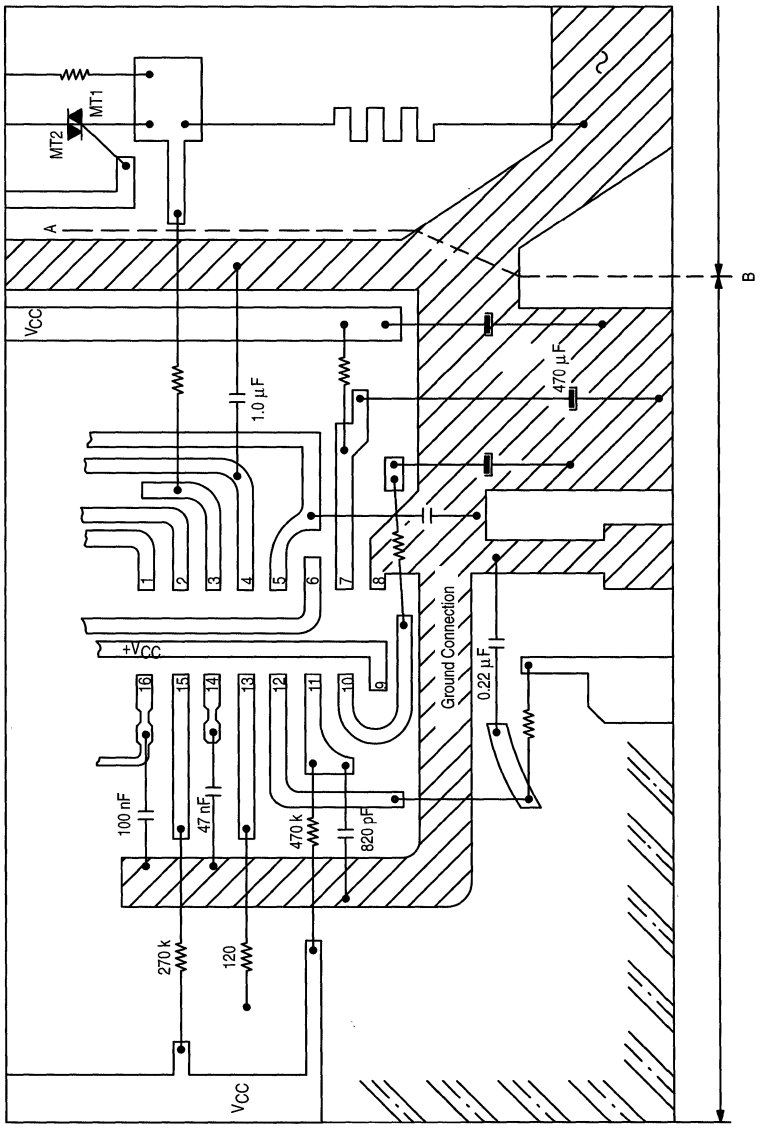


Figure 6. Distribution Speed k < 2

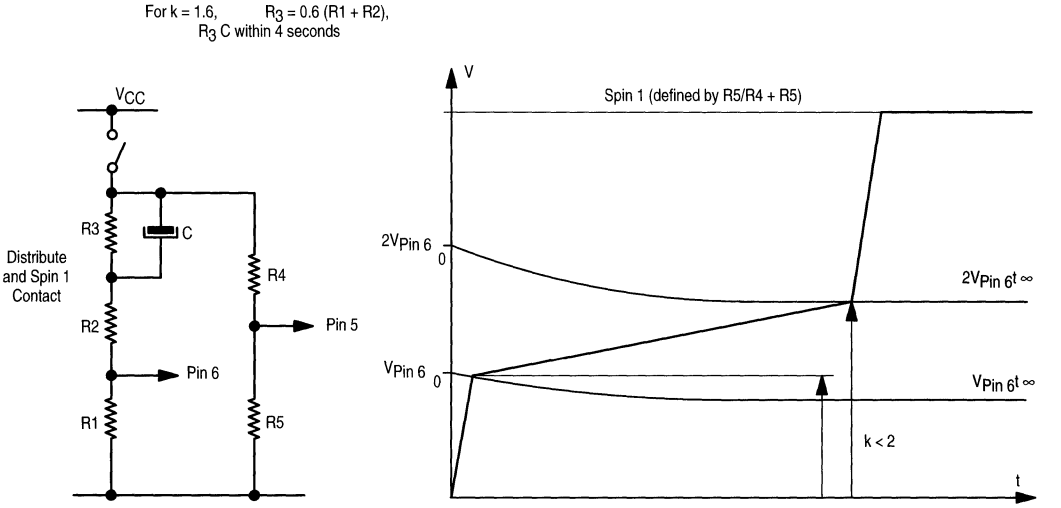


Figure 7. Distribution Speed k > 2

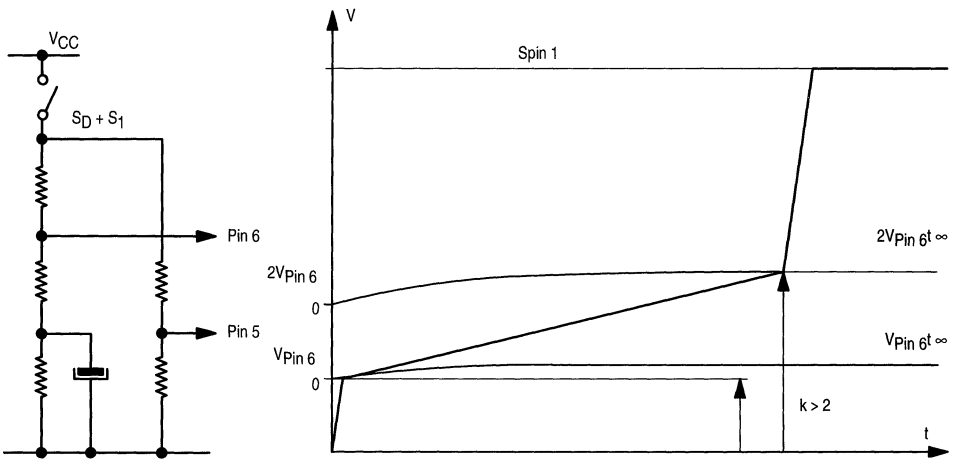
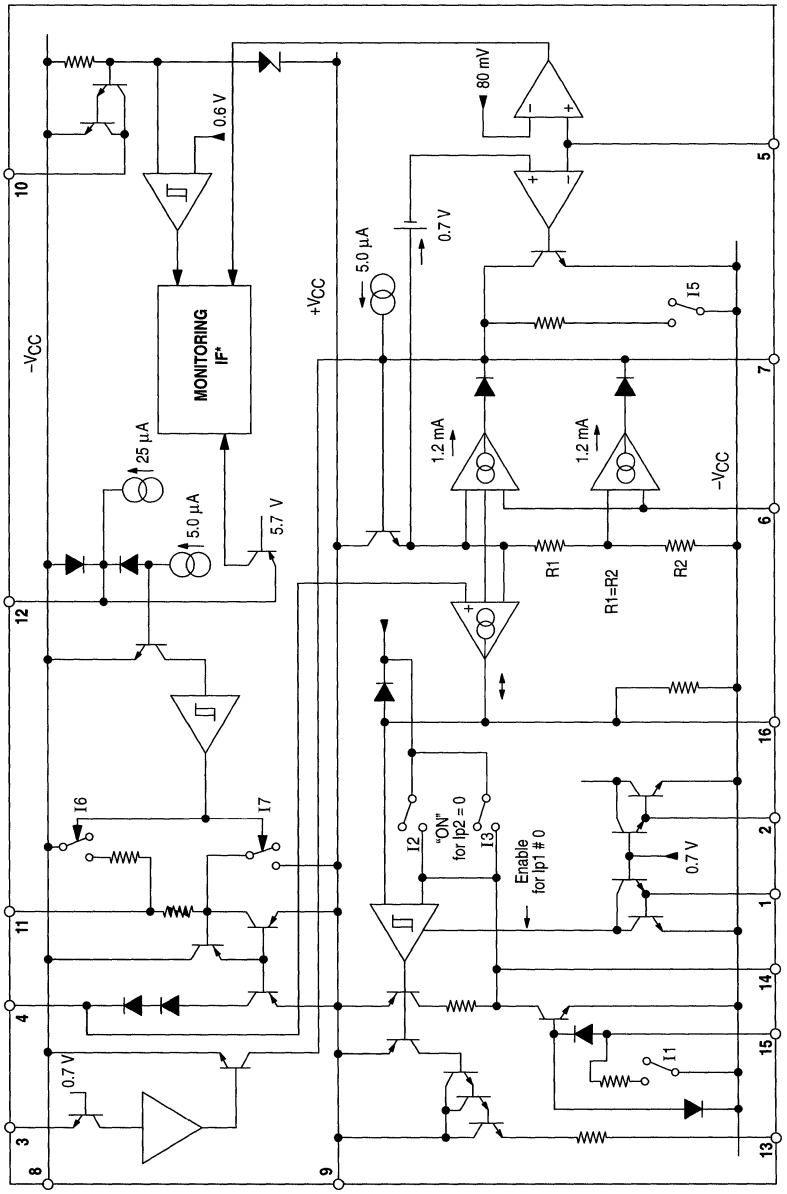


Figure 8. Simplified Schematic



MOTOROLA

TDA1185A

Triac Phase Angle Controller

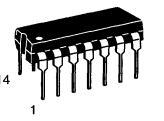
The TDA1185A generates controlled triac triggering pulses and allows tachless speed stabilization of universal motors by an integrated positive feedback function. Typical applications are power hand tools, vacuum cleaners, mixers, light dimmer and other small appliances.

- Supply Power Obtained from AC Line
- Can be used with 220 V/50 Hz or 110 V/60 Hz
- Low Count/Cost External Components
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses when Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensing to Allow Inductive Loads
- Programmable Soft–Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 6.0 mA

TRIAC PHASE ANGLE CONTROLLER

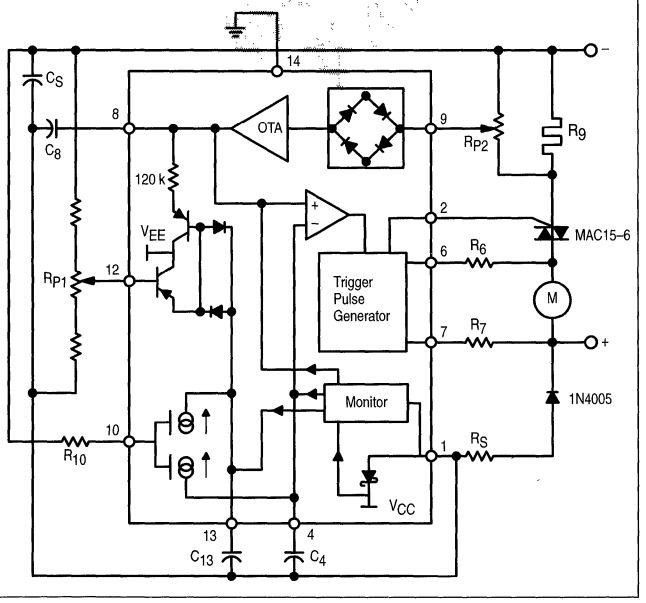
SEMICONDUCTOR TECHNICAL DATA

4

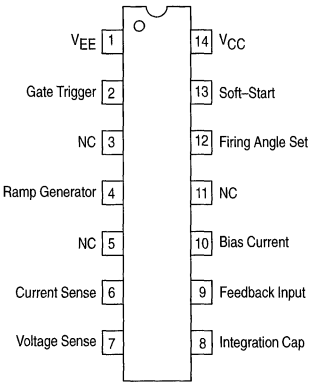


PLASTIC PACKAGE
CASE 646

Figure 1. Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
TDA1185A	T_A = 0° to +70°C	Plastic DIP

MAXIMUM RATINGS (Voltages are referenced to Pin 14, ground)

Rating	Symbol	Value	Unit
Maximum Voltage Range per Listed Pin	V_{Pin}		V
Pins 3, 5, 11 (not connected)		– 20 to + 20	
Pins 4, 8, 13		$-V_{CC}$ to 0	
Pin 2		– 3.0 to + 3.0	
Maximum Positive Voltage (No minimum value allowed; see current ratings)	$V_{Pin\ 12}$ $V_{Pin\ 1}$	0 0.5	
Maximum Current per Listed Pin	I_{Pin}		
Pin 1		± 20	mA
Pins 6 and 7		± 2.0	mA
Pin 9		± 0.5	mA
Pin 10		± 300	µA
Pin 12		– 500	µA
Maximum Power Dissipation (@ T_A = 25°C)	P_D	250	mW
Maximum Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	100	°C/W
Operating Ambient Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, voltages are referenced to Pin 14 [ground] unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply					
Zener Regulated Voltage, ($V_{Pin\ 1}$) $I_{Pin\ 1}$ = 2.0 mA	$-V_{CC}$	– 9.6	– 8.6	– 7.6	V
Circuit Current Consumption, $I_{Pin\ 1}$					
$V_{Pin\ 1}$ = – 6.0 V, $I_{Pin\ 2}$ = 0 A	$-I_{CC}$	– 2.0	– 1.0	—	mA
Monitoring Enable Supply Voltage (V_{EN})	$V_{Pin\ 1EN}$	V_{CC} + 0.2	—	V_{CC} + 0.5	V
Monitoring Disable Supply Voltage (V_{DIS})	$V_{Pin\ 1DIS}$	V_{EN} + 0.12	—	V_{EN} + 0.3	
Phase Set					
Control Voltage Static Offset $V_{Pin\ 8} - V_{Pin\ 12}$	V_{off}	1.2	—	2.0	V
Pin 12 Input Bias Current	$I_{Pin\ 12}$	– 200	—	0	nA
$V_{Pin\ 4} - V_{Pin\ 12}$ Residual Offset		—	180	—	mV
Soft–Start	$I_{Pin\ 13}$	– 17	– 14	– 11	µA
Capacitor Charging Current					
$R_{Pin\ 10}$ = 100 kΩ, $V_{Pin\ 13}$ from $-V_{CC}$ to – 3.0 V					
Sawtooth Generator					
Sawtooth Capacitor Discharge Current					
R_{10} = 100 kΩ $V_{Pin\ 4}$ from – 2.0 to – 6.0 V	$I_{Pin\ 4}$	67	70	73	µA
Capacitor Charging Current	$I_{Pin\ 4}$	– 10	—	– 1.5	mA
Sawtooth "High" Voltage ($V_{Pin\ 4}$)	V_{HTH}	– 2.5	– 1.6	– 1.0	V
Sawtooth Minimum "Low" Voltage ($V_{Pin\ 4}$)	V_{LTH}	—	– 7.1	—	V
Positive Feedback					
Pin 9 Input Bias Current, $V_{Pin\ 9}$ = 0	$I_{Pin\ 9}$	—	2 x $I_{Pin\ 10}$	—	
Programming Pin Voltage Related to Pin 1	$V_{Pin\ 10}$	1.0	1.25	1.5	V
Transfer Function Gain $\Delta V_{Pin\ 8}/\Delta V_{Pin\ 9}$					
R_{10} = 100 kΩ , $\Delta V_{Pin\ 9}$ = 50 mV	A	—	75	—	
R_{10} = 270 kΩ , $\Delta V_{Pin\ 9}$ = 50 mV	A	—	36	—	
Pin 8 Output Internal Impedance	$Z_{Pin\ 8}$	—	120	—	kΩ
Trigger Pulse Generator					
Output Current (Sink) $V_{Pin\ 2}$ = 0 V	$I_{Pin\ 2}$	60	—	80	mA
Output Leakage Current $V_{Pin\ 2}$ = + 2.0 V		—	—	4.0	µA
Output Pulse Width	t_P				
C_4 = 47 nF R_{10} = 270 kΩ		—	55	—	µs
Output Pulse Repetition Period	t				
C_4 = 47 nF R_{10} = 270 kΩ		—	420	—	µs
Current Synchronization Threshold Levels $I_{Pin\ 6}$, $I_{Pin\ 7}$	I_{sync}	– 40	—	+ 40	µA

PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	V_{EE}	This pin is the negative supply for the chip and is clamped at – 8.6 V by an internal zener.
2	Gate Trigger Pulse	This pin supplies – 1.0 V triac trigger pulse at twice the line frequency.
3	NC	Not connected.
4	Ramp Generator	The value of the capacitor at this pin determines the slope of the ramp.
5	NC	Not connected.
6	Current Sense	This pin senses if the triac is on, and if so, will disable the gate trigger pulse.
7	Voltage Sense	The internal timing of the chip is set by the frequency of the voltage at this pin.
8	Integration Capacitor	This pin is the output of the feedback and the variation in voltage is averaged out by the capacitor.
9	Feedback Input	The change in load current is detected by the change in voltage across R9.
10	Current Program	The bias current for the circuit is determined by the resistor value at this pin.
11	NC	Not connected.
12	Phase Angle Set	The voltage at this pin sets the no–load firing angle.
13	Soft–Start	The firing angle is slowly increased from 180° to the set value of Pin 12.
14	V_{CC}	Ground

Introduction

The Motorola TDA1185A generates trigger pulses (Pin 2) for triac control of power into an AC load. The triac trigger pulse is determined by generating a ramp voltage (Pin 4) synchronized to twice the AC line frequency and compared to an external set voltage (Pin 12) representing the conduction angle. Gate pulses are negative (sink current) and thus the triac is driven into its most effective quadrants (Q2 to Q3).

If the load is a Universal motor (the speed of which decreases as torque increases), the TDA1185A allows to increase the conduction angle proportionally to the motor current, sensed (Pin 9) by a low value resistor in series with the load.

FUNCTIONAL DESCRIPTION

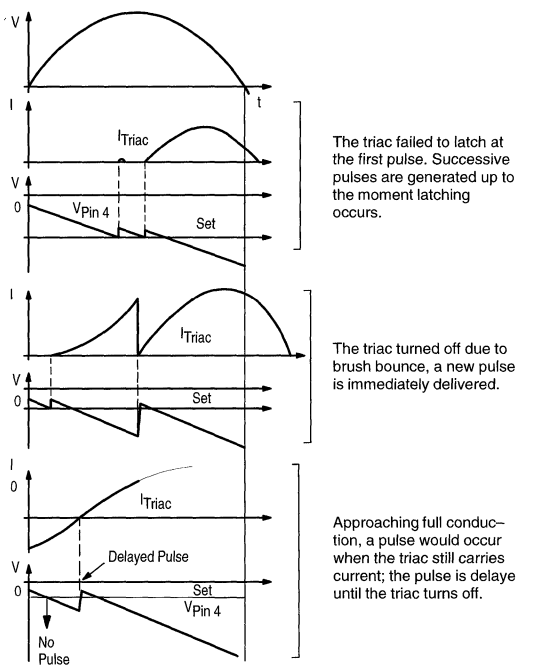
DC Power Supply

DC power is directly derived from the AC line through a 2.0 W resistor, half–wave rectifier and filtering capacitor circuit. The V_{EE} voltage is internally regulated by an integrated zener. Referenced to ground (Pin 14), the power supply voltage is – 8.6 V. The TDA1185A internal consumption is 6.0 mA.

Trigger Pulse Generator

It delivers a 60 mA minimum sink current pulse (Pin 2) through an internally short circuit protected output. Pulse width is roughly proportional to $R_{10} \times C_4$ and is repeated every 420 µs if triac fails to latch or is switched off by brush bounce. With inductive loads, the current lags in respect to the voltage. Pin 6 delays the triggering pulse up to the moment the triac is off, in order to prevent erratic power control (see Figure 2).

Figure 2. Multipulse Generation Delayed Pulse



Ramp Generator

A constant current sink discharges capacitor C_4 producing a negative voltage ramp synchronized with the main line. Pin 4 voltage is reset to – 1.6 V at every AC line zero crossing (see Figure 3) and ramps down to – 7.1 V. The constant current sink is externally programmable by R_{10} using the equation below.

$$I_4 = I_{10} \pm 5\%$$

$$I_{10} = \frac{|V_{EE} + 1.25|}{R_{10}}$$

Main Comparator

Its role is to determine the trigger pulse which occurs when the ramp voltage equals the phase angle set voltage at Pin 12. Fixed phase angle set voltage values lead to a constant TRIAC conduction angle unless positive current feedback (Pin 9) is connected or the Soft–Start capacitor (Pin 13) is not charged.

Soft–Start

The TDA1185A allows the user to avoid any abrupt inrush of current into the load. This provides protection for fragile loads, light bulbs or tubes. Another advantage is that the AC line disturbance is minimized.

The conduction angle is established from zero to the set value at Pin 12 according to a voltage ramp generated by a constant current delivered to C_{13}. The value of current I_{13} can be expressed by the following equation:

$$I_{13} = 0.2 \times I_{10} \pm 10\%$$

The voltage ramp lasts as long as V_{13} is lower than the set voltage V_{12}. Upon reset, V_{13} is forced to V_{EE} as shown in Figure 4. If the load is a universal motor, it will not turn until a minimum conduction angle is achieved to overcome friction. The time the voltage ramp requires to reach its threshold value is considered deadtime, and can be eliminated by an appropriate series resistor at Pin 13. The voltage drop developed by I_{13} thru the resistor causes the conduction angle to immediately reach the threshold value and have the Soft–Start function without dead time (see Figure 5).

Figure 3. Triggering Pulse Timing

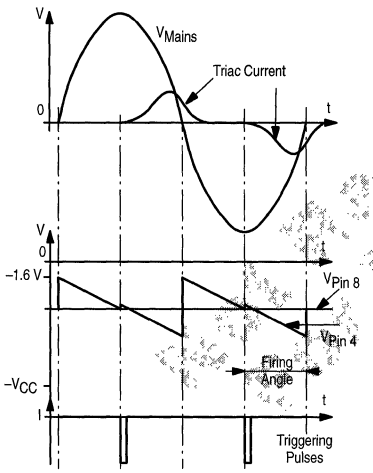


Figure 4. Soft–Start

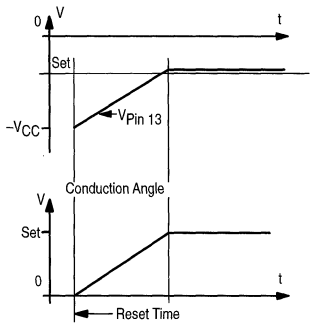


Figure 5. Soft–Start without Deadtime

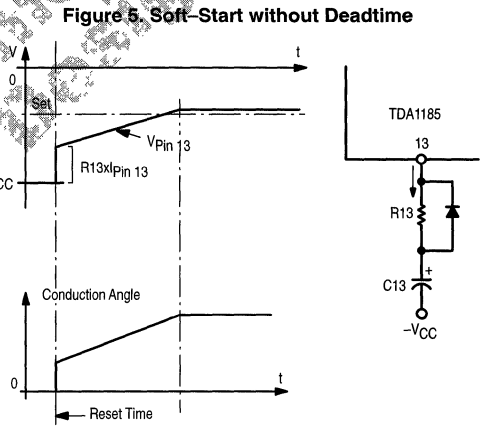
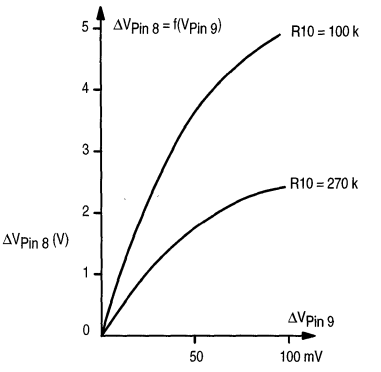


Figure 6. Transfer Function



Positive Current Feedback

The Universal motor speed drops as load increases. To maintain the speed, the triac conduction angle must be increased. For this purpose, Pin 9 senses the motor current as a **voltage** developed in a low value resistor, R_9, amplifies, rectifies and adds it internally to the set voltage at Pin 12. Any voltage variation at the output of the feedback, Pin 8, is smoothed out by capacitor C_8. The transfer function, $\Delta V_8 = f(\Delta V_9)$, is shown in Figure 6.

The gain in the linear region is dependent on R_{10}. The voltage transferred to Pin 8 is proportional to the current RMS value, as motor current is not far from a sine wave. This averaging effect is shown in Figure 7.

With large amplitude signals at Pin 9, the change in voltage at Pin 8 reaches a maximum value. This saturation effect limits the maximum conduction angle increase. This effect is illustrated in Figure 8 where the total Pin 8 voltage can be written as follows:

$$V_8 = V_{12} + f(|V_9|, R_{10}) + 1.25$$

The effect of the feedback is illustrated in Figure 9.

Monitoring

A central logic block performs the ENABLE/DISABLE function of the IC with respect to power supply voltage. Under DISABLE conditions, Pin 4, 8, 12 and 13 are forced to appropriate voltages to prepare for the next reset. Refer to the block diagram in Figure 10.

APPLICATION CONSIDERATIONS

Component Selection

To regulate the speed of a universal motor, it is necessary to determine how much gain in the feedback is needed. A change in motor current (due to load increase) causes the conduction angle to change by the appropriate amount to keep the speed constant. This entails, through trial and error, choosing an appropriate resistor value for R_{10}, since the gain of the feedback is determined by value of R_{10} as shown in Figure 8.

Figure 7. Averaging Effect of Transfer Function

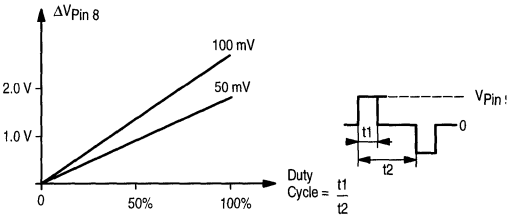
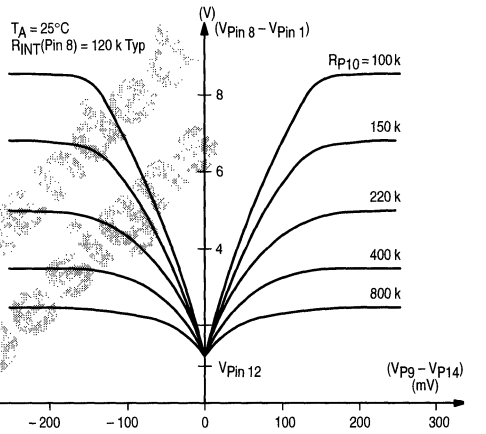


Figure 8. Transfer Function (Pin 8/Pin 9)



Once R_{10} is picked, C_4 can be calculated from the following equation:

$$C_4 \approx \frac{.672}{f_{line} \times R_{10}}$$

where f_{line} is the line frequency.

Figure 9. Positive Feedback Effect (Offset voltages have been neglected)

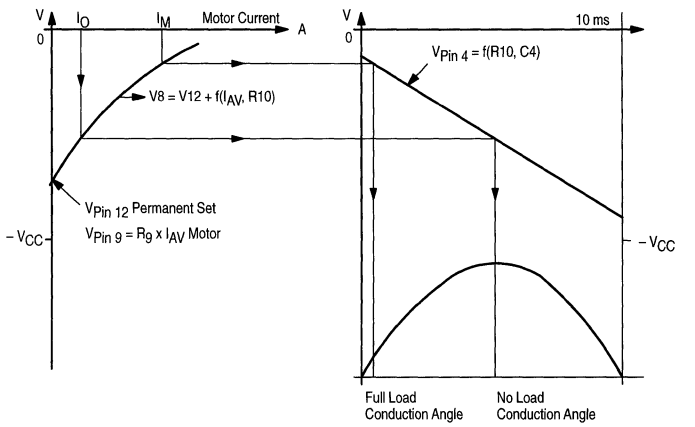
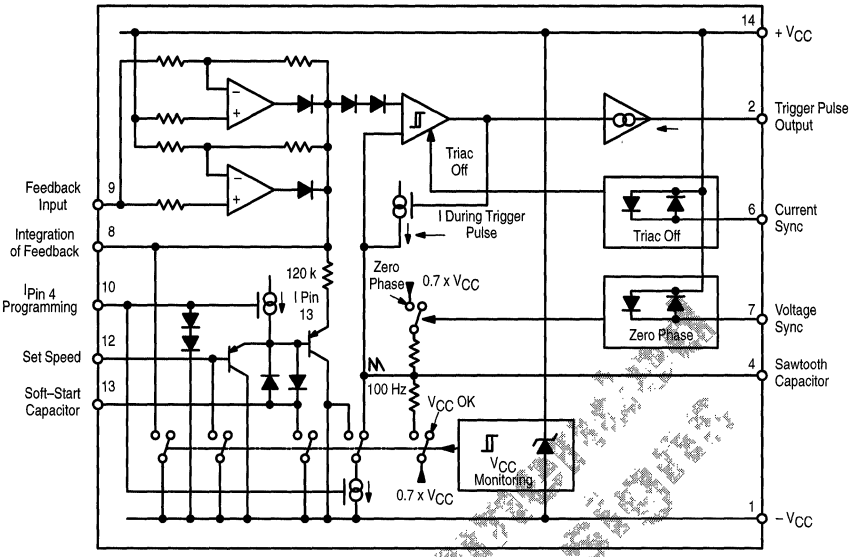


Figure 10. Internal Block Diagram



Capacitor C_8 is an integration cap used to smooth out the voltage at Pin 8. The value should be large enough to accomplish this task yet not too large to slow the response of the system.

Capacitor C_{13} determines how fast the conduction angle reaches the set value programmed at Pin 12. To achieve a desired delay, the value for C_{13} can be calculated by the following equation:

$$C_{13} \approx \frac{8 \times t_d}{|8.6 - V_{12}| \times R_{10}}$$

The remaining component values have experimentally been determined and are constant, regardless of application. The following table lists typical values for 110 V application.

Component	Value	Units
R_S	10/2.0 W	kΩ
R_{P1}	100	kΩ
R_{P2}	100	Ω
R_6	330/0.5 W	kΩ
R_7	330/0.5 W	kΩ
R_9	0.05/5.0 W	Ω
R_{10}	100	kΩ
C_4	0.1	µF
C_8	0.22	µF
C_{13}	10	µF

Using an oscilloscope, it should be verified that the ramp generator is ramping down from – 1.6 to – 7.1 V. The slope of the ramp can be changed by C_4 and the DC level of the waveform can be adjusted by R_7.

Pin 9 has a low internal impedance and requires R_{P2} to adjust the feedback level. Pin 8 must always be connected to V_{EE} through a filtering capacitor. For values of R_{10} less than 100 kΩ, the circuit becomes sensitive and could become unstable. Figures 11 and 12 show typical waveforms. As shown, the increase in motor current has resulted in the firing angle to decrease. This translates to an increase in the average power delivered to the load.

Figure 11. No Load Applied

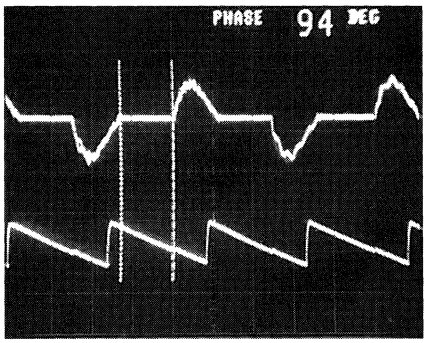
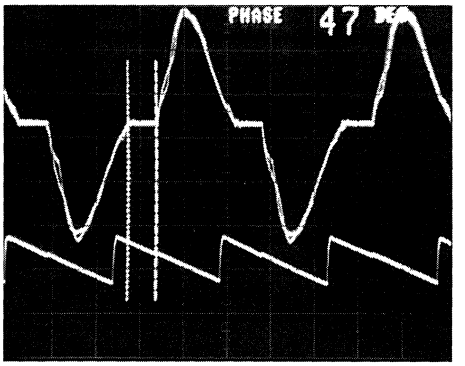


Figure 12. Load Applied



Temperature Effects

The TDA1185A has a very efficient internal temperature compensation. If the current feedback is not connected, the RMS power delivered to the load is stabilized within ± 0.2% over a temperature range of 20 to 70°C. The feedback introduces, in the same temperature range, a drift of 250 mV on the voltage of Pin 8; this slight increase in conduction angle may be successfully used to compensate a motor ohmic resistance increase with temperature.

Main Line Voltage Compensation

As the conduction angle is independent of main line voltage, any change in the latter induces a power variation to the load. A resistor connected to the rectifier anode and to Pin 12 with a capacitor to V_{EE} will introduce a decrease in voltage at Pin 12 as the line voltage is increasing. The values of the RC network can experimentally be determined.

Firing Angle Dynamics

With purely resistive loads, the effective RMS applied voltage to the load is directly proportional to the firing angle (Figure 13). With inductive loads, since the current lags with respect to voltage, 100% power corresponds to a firing angle which is less than 180°.

APPLICATION IDEAS

Soft–Start

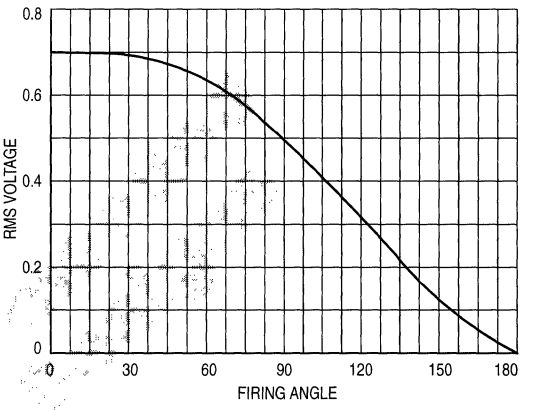
The Soft–Start feature of the TDA1185A in itself opens the door to a lot of interesting applications. For example, the TDA1185A can be used to bring up fragile loads slowly. Expensive and sensitive tubes can be turned on slowly, thus eliminating the inrush of current that could lead to burn out. In this application, R_{P1} is replaced with a resistor divider such that the voltage at Pin 12 results in a conduction angle of 180°. Pin 9 should be grounded, since the feedback portion of the TDA1185A is not necessary (see Figure 14). The time to achieve full conduction is found by the equation below:

$$\Delta t \approx 8.71 \times R_{10} \times C_{13}$$

Light Dimmer

With practically no modification the TDA1185A can be used in a light dimmer application. All that is required is to ground the input to the feedback Pin 9. By grounding Pin 9, we have disconnected the feedback loop and the conduction angle is controlled solely by R_{P1}. Further, since the feedback is disconnected, R_9 and R_{P2} are no longer necessary. The Soft–Start feature can still be used to protect the bulb from an inrush of current. This setup can be used in any application that requires manual control of the power delivered to the load (see Figure 15).

Figure 13. RMS Voltage versus Firing Angle



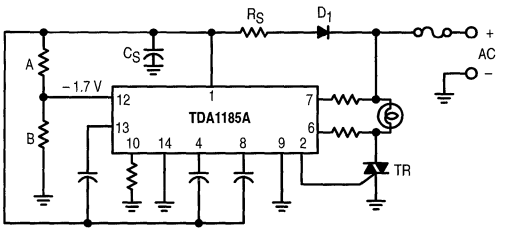
Soft Shut–Off

Once again with little modification, the TDA1185A can be used to turnoff the load slowly. An example of this is in automatic garage lighting. Typically, lights that are on a timer go off without a warning, usually in the most inopportune time (like when you're about to step over the dog). With a soft shut–off, the light dims out slowly, alerting you that it is about to go off. As in the previous case, the feedback is disconnected and R_{P1} is replaced with capacitor C_{12} and a switch (see Figure 16). The turn–off time can be calculated by the following equation:

$$\Delta t \approx R_{12} \times C_{12}$$

R_{12} is the sum of the two resistors on both sides of C_{12}.

Figure 14. Soft–Start Circuit



R_S = 10 kΩ 2 W
R_6 = 470 kΩ 1/2 W
R_7 = 470 kΩ 1/2 W
R_{10} = 200 kΩ
$R_{12A} = 4 \times R_{12B}$

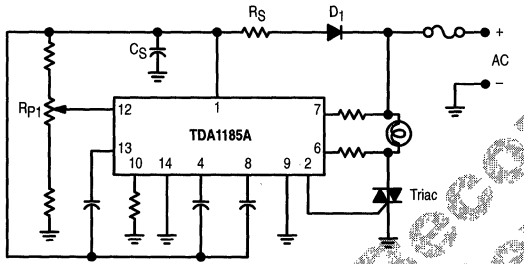
C_4 = 44 nF
C_{13} = 10 µF
C_S = 100 µF
Turn–off time = $8.71 \times R_{10} \times C_{13}$

PC Board

The printed circuit board in Figure 17 is included for the designer's convenience to evaluate the TDA1185A. The size of the board is intentionally small to show the compactness that can be achieved. Figure 18 shows the component layout for the PC board. R_{P1} has one of the outer leads connected to V_{EE} and the other to R_{12}. The center lead of R_{P1} is connected to Pin 12.

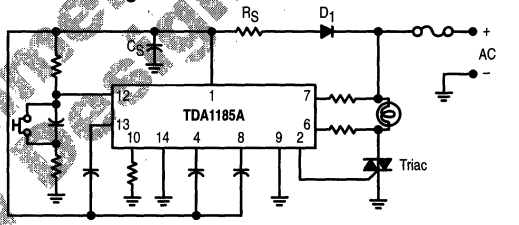
Warning Shock Hazard: It is highly recommended that an isolation transformer be used. Remove the chassis ground for all test equipment.

Figure 15. Light Dimmer Circuit



R_P = 100 k
R_S = 10 k 2 W
R_6 = 470 k 1/2 W
R_7 = 470 k 1/2 W
R_{10} = 200 k
C_4 = 44 nF
C_8 = 0.22 µF
C_{13} = 4.7 µF
C_S = 100 µF 16 V

Figure 16. Soft Shut–Off Circuit



R_S = 10 k 2 W
R_6 = 470 k 1/2 W
R_7 = 470 k 1/2 W
R_{12} = Designer's Choice
R_{10} = 200 k
C_4 = 44 nF
C_{12} = Designer's Choice
C_{13} = 0.47 µF
C_S = 100 µF
Turn–off time = $R_{12} \times C_{12}$

Figure 17. Evaluation Board (Component Side)

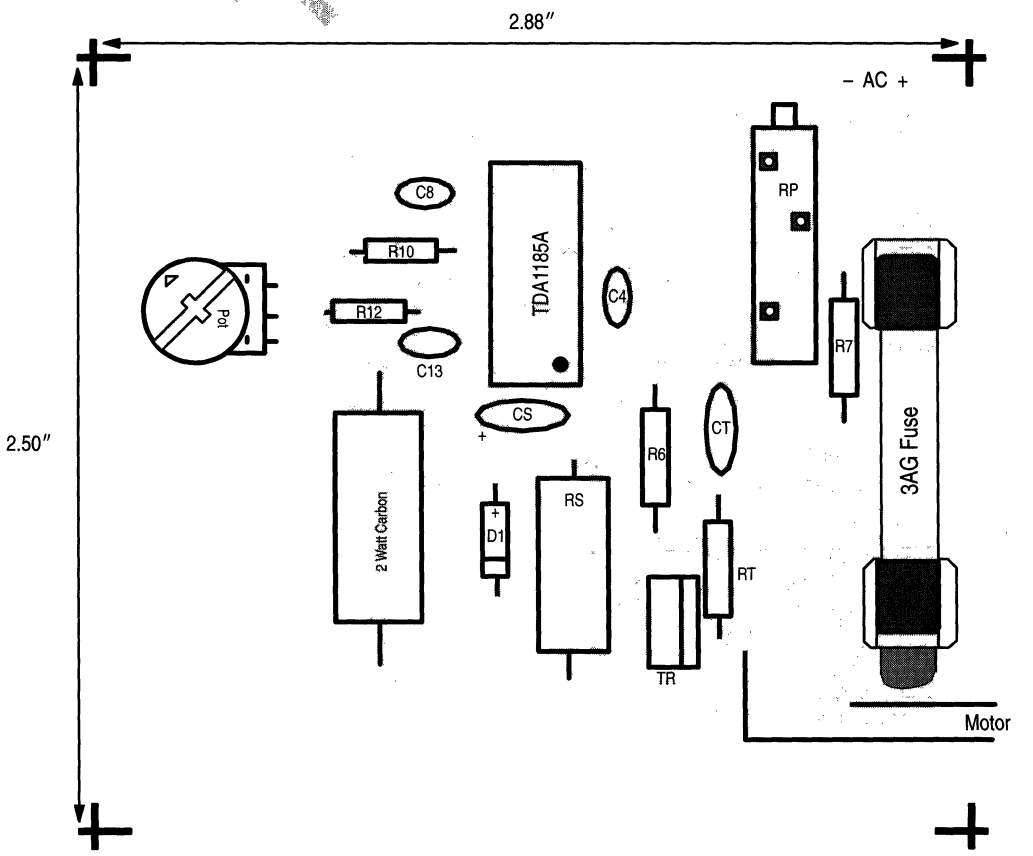
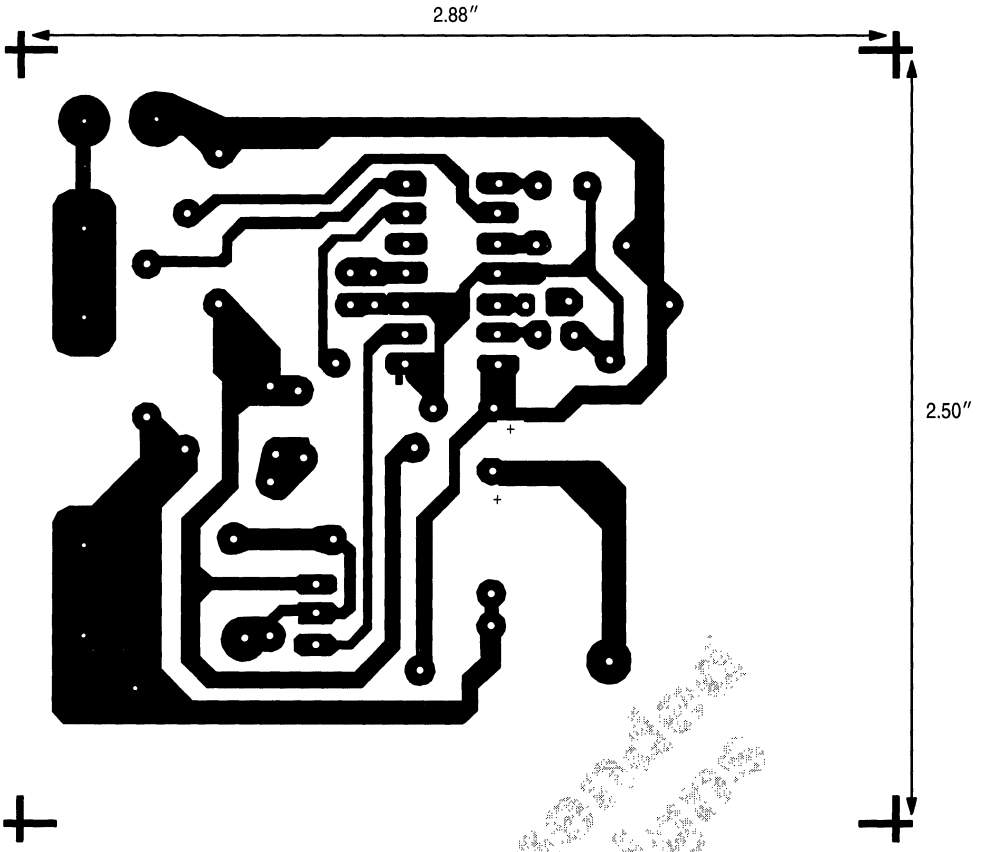


Figure 18. Evaluation Board
(Copper Side)



MOTOROLA

UAA1016B

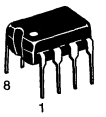
Zero Voltage Controller

The UAA1016B is designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. It provides the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- No DC Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triac Quadrants 2 and 3)
- Direct AC Line Operation
- Low External Components Count

ZERO VOLTAGE SWITCH PROPORTIONAL BAND TEMPERATURE CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

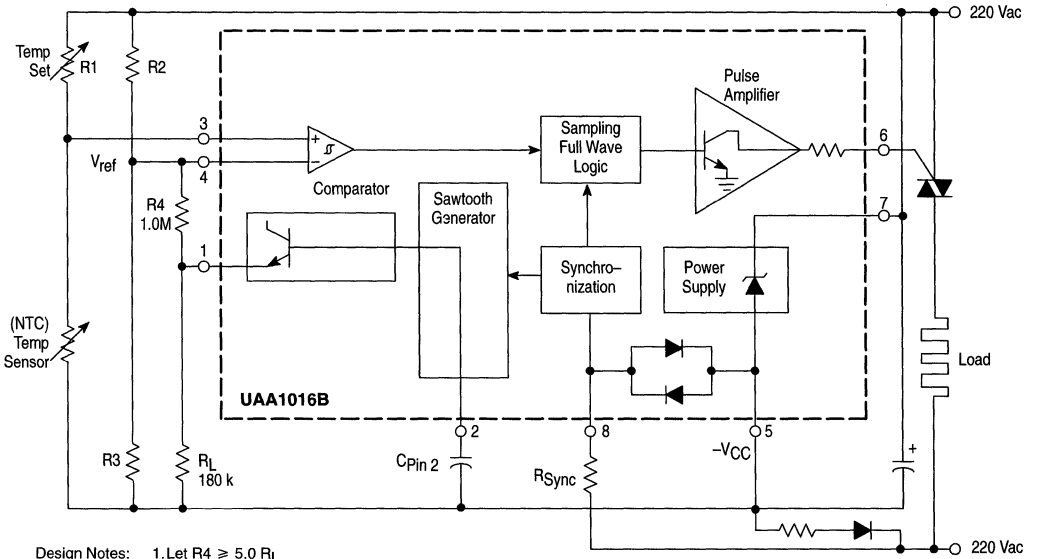


PLASTIC PACKAGE
CASE 626

ORDERING INFORMATION

Device	Operating Temperature Range	Package
UAA1016B	T_A = –20° to +100°C	Plastic DIP

Representative Block Diagram and Pin Connections



Design Notes: 1. Let R4 ≥ 5.0 R_L

2. Select $\frac{R2}{R3}$ Ratio for a symmetrical reference deviation centered about Pin 1 output swing, R2 will be slightly greater than R3.

3. Select R2 and R3 values for the desired reference deviation where $\Delta V_{ref} = \frac{\Delta V_{Pin1}}{\frac{R4}{R2 \mid\mid R3} + 1}$

This device contains 30 active transistors.

MAXIMUM RATINGS (Voltages Referred to Pin 7)

Parameter	Symbol	Max. Rating	Unit
Supply Current ($I_{Pin\ 5}$)	I_{CC}	15	mA
Nonrepetitive Supply Current ($I_{Pin\ 5}$)	I_{CCP}	200	mA
AC Synchronization Current (Pin 8)	I_{syn}	3.0	mArms
Maximum Pin Voltages	$V_{Pin\ 1}$ $V_{Pin\ 2}$ $V_{Pin\ 3}$ $V_{Pin\ 4}$ $V_{Pin\ 6}$	0; – V_{CC} 0; – V_{CC} 0; – V_{CC} 0; – V_{CC} 2.0; – V_{CC}	V
Maximum Current Drain	$I_{Pin\ 1}$	1.0	mA
Power Dissipation T_A = 25°C	P_D	625	mW
Maximum Thermal Resistance	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	–20 to +100	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Voltages Referred to Pin 7, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Current Consumption (Pins 6 and 8 not connected)	I_{CC}	–	0.8	1.5	mA
Stabilized Supply Voltage ($V_{Pin\ 5}$) I_{CC} = 2.0 mA max	–V_{CC}	–9.6	–8.6	–7.6	V
Output Pulse Current ($V_{Pin\ 6}$ from –1.0 to +1.0 V)	I_{out}	60	90	120	mA
Output Pulse Width $R_{Pin\ 8}$ = 220 kΩ, V_{mains} = 220 Vac/50 Hz, (Figures 3 and 4)	t_{p1} t_{p2}	58 160	60 220	120 320	µs
Comparator Input Offset Voltage ($V_{Pin\ 3}$ – $V_{Pin\ 4}$)	V_{off}	–10	–	10	mV
Comparator Common Mode Voltage Range	V_{CM}	–V_{CC} + 1	–	–1.5	V
Input Bias Current (Pins 3 and 4)	I_{IB}	–	–	1.0	µA
Output Leakage Current ($I_{Pin\ 6}$) $V_{Pin\ 6}$ = +2.0 V	I_{outL}	–	–	10	µA
Capacitor Charging Current (Source)	$I_{Pin\ 2}$	–20	–16	–12	µA
Capacitor Discharge Current (Sink)	$I'_{Pin\ 2}$	–	6.4	–	mA
Sawtooth Pulse Length ($C_{Pin\ 2}$ = 1.0 µF)	t_{saw}	–	0.85	–	S
Output Threshold Sawtooth Levels ($V_{Pin\ 2}$)	V_{TH1} V_{TH2}	– –	–1.0 –V_{CC} + 1.25	– –	V
Output Voltage Pin 1	$V_{Pin\ 1}$	–	$V_{Pin\ 2}$ – 0.75	–	V

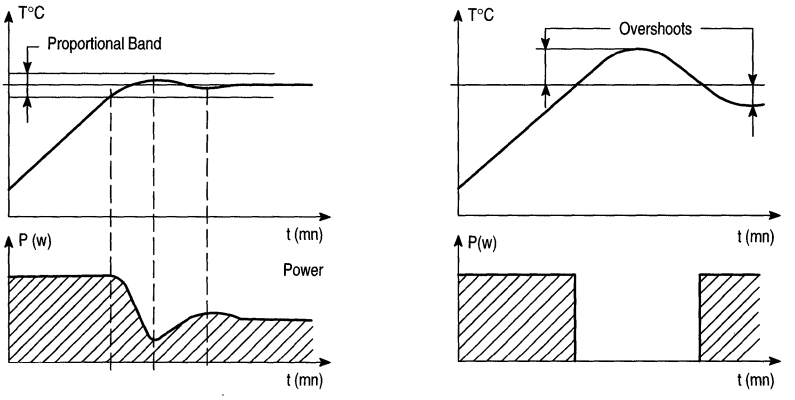
CIRCUIT DESCRIPTION

The circuit delivers current pulses to the triac at zero crossings of the main line sensed by Pin 8 through R_{sync}. An internal full wave logic allows the triac to latch during full wave periods in order to avoid any dc component in the main line, in compliance with European regulations. Trigger pulses are generated when the comparator detects $V_{Pin\ 3}$ is above $V_{Pin\ 4}$ (or $V_{reference}$) as sensed temperature through the NTC is then lower than the set value (V_{ref} corresponding to the external Wheatstone bridge equilibrium).

In order to comply with norms limiting the frequency at which a kW sized load, or above, may be connected to the main line (fluorescent tubes "flickering"), the UAA1016B has an internal time base providing (power is delivered by bursts to the load) a proportional temperature band control. In fact, most of the heating regulation systems require low temperature overshoot for more precision and stability which cannot be accomplished by direct on/off regulation (see Figure 1). An internal low frequency sawtooth generator whose output is available at Pin 1, allows the designer to introduce a periodic linear change of V_{ref}. This deviation defines the temperature band allowing proportional power control (see Figure 2).

The IC is directly powered from the mains by a dropping resistor, a diode and a filter capacitor.

Figure 1. Proportional Temperature Control versus On/Off Control



(PROPORTIONAL TEMPERATURE CONTROL)

Reduced Overshoot
Stability

(ON/OFF CONTROL)

Large Overshoot
Marginal Stability

KEY CIRCUIT FUNCTIONS DESCRIPTION

Power Supply

The rectified supply current is Zener regulated to 8.6 V. Current consumption of the UAA1016B is typically less than 1.0 mA. The major part of the current fed by the dropping resistor is used for the sensor bridge and triac gate pulses. Any excess of supply current is excess power dissipation into the integrated Zener. Current consumption of the triac pulses may be derived from Figure 3 and 4 (Igt maximum and pulse duration). Usually an 18 kΩ, 2.0 W dropping resistor is convenient to feed the UAA1016.

Comparator

When $V_{Pin\ 3}$ is higher than $V_{Pin\ 4}$ (V_{ref}), the comparator allows the triggering logic to deliver pulses to the triac (Figure 2). The offset hysteresis input voltage has been designed to be as low as possible (±10 mV maximum) in order to minimize the uncontrollable temperature band (proportional to the hysteresis) as per Figure 5. Noise rejection is performed by a synchronous sampling of the comparator output during very short times (typical less than 100 ns).

Sawtooth Generator

A sawtooth voltage signal is generated by a constant current source (typical 7.5 µA), charging an external capacitor $C_{Pin\ 2}$ between two threshold levels, V_{TH1} and V_{TH2}, which are respectively:

$V_{TH1} = -1.0$ V

$V_{TH2} = -V_{CC} + 1.25$ V

Charging and discharging currents occur only with negative halfcycles of the line. In the UAA1016B, the sawtooth signal is available at Pin 1 as a voltage source $V_{Pin\ 1} = V_{Pin\ 2} - 0.75$ V. Maximum source current is 1.0 mA, but to keep good linearity of sawtooth signal, a source current of 40 µA is recommended (see Figure 6).

Sampling Full Wave Logic

Two consecutive zero–crossing trigger pulses are generated at every positive mains half–cycle of the line to minimize generation of noise (as per Figure 7). Within every zero–crossing the pulses are positioned as per Figure 3. Pulse length is also adjustable by R_{sync} on Pin 8 to allow positive triggering of the triac at this critical moment (firing with low voltage between main terminals requires long pulses).

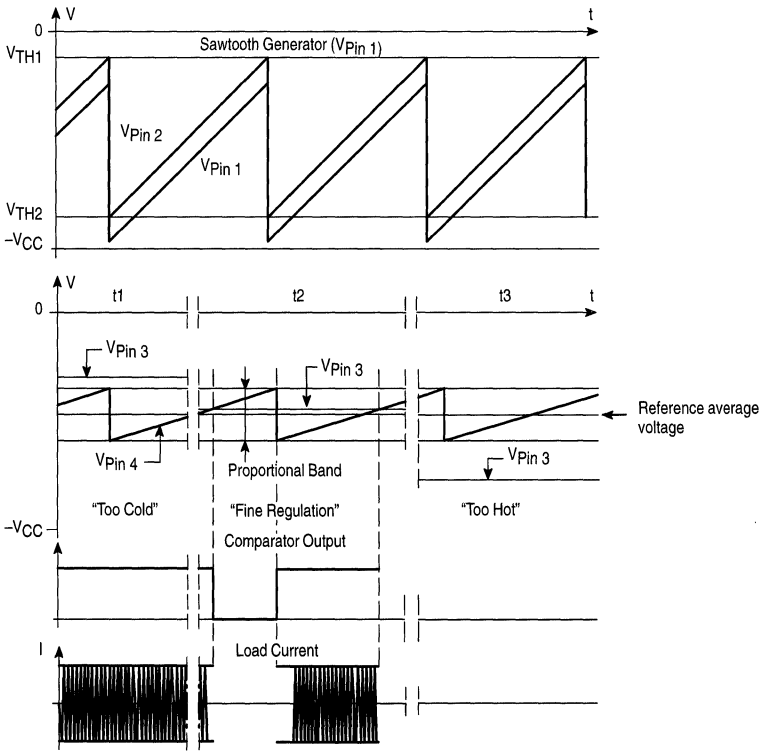
Pulse Amplifier

The pulse amplifier circuit delivers minimum current pulses of 60 mA (sink). The triac is triggered in quadrants II and III.

Synchronization Circuit

This circuit detects mains zero–crossings through R_{sync} and the value selected determines the trigger pulse length. A zero crossing current detector is employed with typical thresholds of ±27 µA to ±98 µA (see Figures 3 and 4).

Figure 2. Sawtooth Generator and Proportional Band



4

COMMENTS TO FIGURE 2

Referring to Figure 1, the average value of V_{ref} is set by R2 and R3. R4 defines the amplitude of the sawtooth signal superimposed on V_{ref}, defining the Proportional Band.

Figure 2 shows three conditions:

1) During time t1 we always have $V_{Pin\ 3} > V_{ref}$, and as a result, the comparator is always "on" and the triac fired (100% maximum power)

2) During time t2, $V_{Pin\ 3}$ is in the proportional band, and the average power delivered to the load is a fraction of maximum power.

3) During time t3, $V_{Pin\ 3} < V_{ref}$, and the triac is always "off."

When the sensor temperature is above the set value and is slowly decreasing as no heating occurs, $V_{Pin\ 3} - V_{Pin\ 4}$ must exceed half the hysteresis value before power is applied again (1). A similar effect occurs in the opposite direction when temperature sensor is below the set value and can remain stable as position (2). This defines the "uncontrollable temperature band" which will be very small if hysteresis is also very small.

SUGGESTIONS FOR USE

The temperature sensor circuit is a Wheatstone bridge including the sensor element. Comparator inputs may be free from power line noise only if the sensor element is purely resistive (NTC resistor). Usage of any P–N junction sensor would drastically reduce noise rejection.

Fixed phase sensing of the internal comparator output eliminates parasitic signals.

Some loads, even designed to be resistive, have in fact a slight inductive component. A phase shift at Pin 8 can be achieved with external capacitor C3 connected to Pin 8 network (see Figure 8).

Suggested maximum source current at Pin 1 is 40 μA, in order to have acceptable sawtooth signal linearity.

Figure 3. Output Pulse Width Definitions

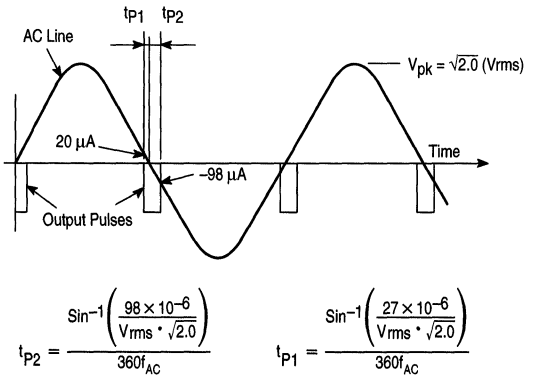


Figure 4. Typical Output Pulse Length versus Synchronization Resistor

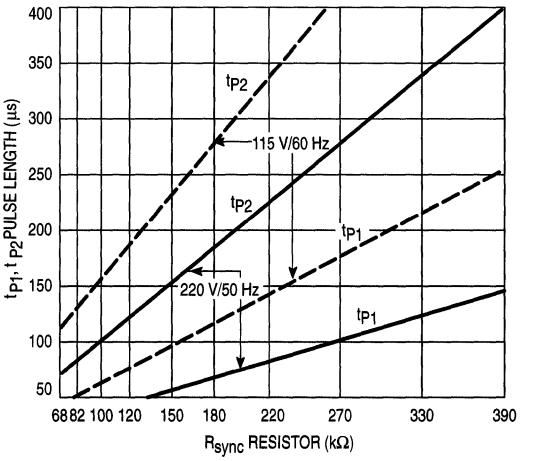


Figure 5. Effects of Inputs Comparator Hysteresis

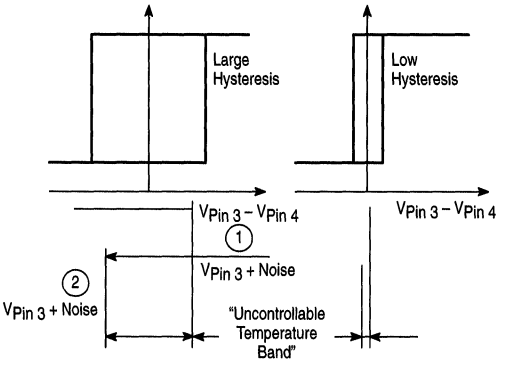


Figure 6. Pin 1 Internal Network

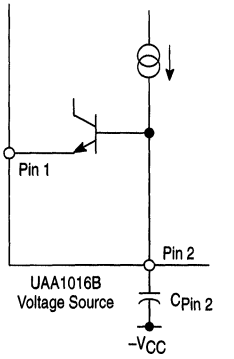
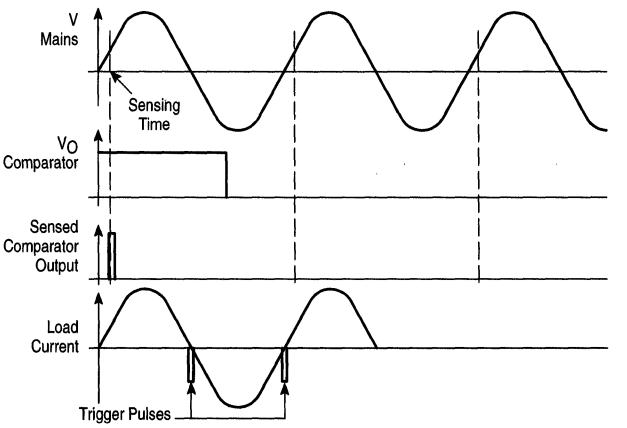


Figure 7. Trigger Pulse Generation



APPLICATION CIRCUITS

Figure 8 shows a very simple application of the UAA1016B as an electronic rheostat having 100% efficiency. C3 is required only if load has an inductive component. Figure 9 shows a typical application as a panel heater thermostat with a proportional temperature band of 1.0°C at 25°C.

Figure 8. Electronic Rheostat

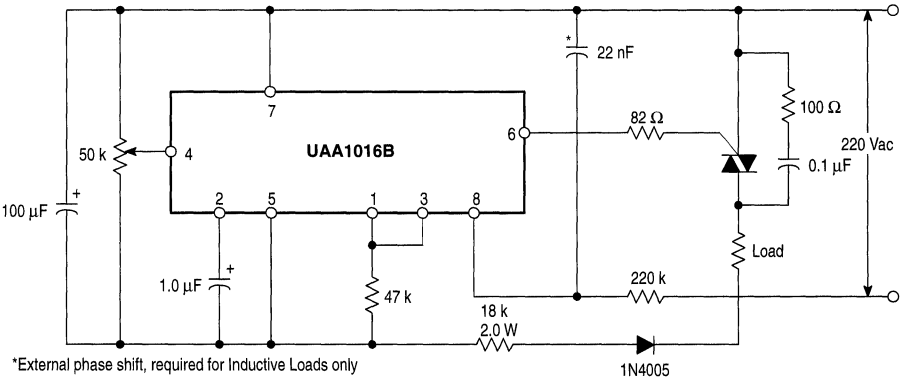
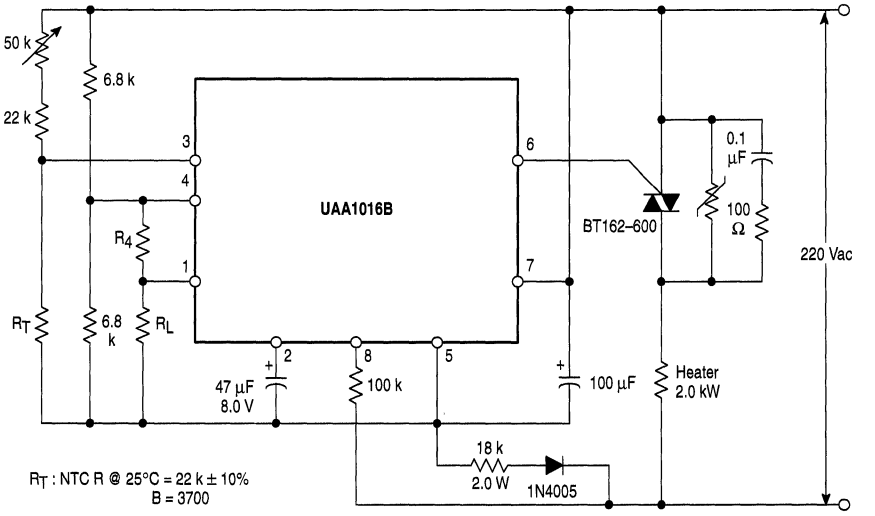


Figure 9. Application Circuit–Electric Radiator with Proportional Band Thermostat
(Proportional Band 1°C at 25°C)



MOTOROLA

UAA2016

Product Preview

Zero Voltage Switch Power Controller

4

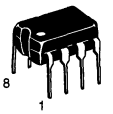
The UAA2016 is designed to drive triacs with the Zero Voltage technique which allows RFI–free power regulation of resistive loads. Operating directly on the AC power line, its main application is the precision regulation of electrical heating systems such as panel heaters or irons.

A built–in digital sawtooth waveform permits proportional temperature regulation action over a ±1°C band around the set point. For energy savings there is a programmable temperature reduction function, and for security a sensor failsafe inhibits output pulses when the sensor connection is broken. Preset temperature (i.e. defrost) application is also possible. In applications where high hysteresis is needed, its value can be adjusted up to 5°C around the set point. All these features are implemented with a very low external component count.

- Zero Voltage Switch for Triacs, up to 2.0 kW (MAC212A8)
- Direct AC Line Operation
- Proportional Regulation of Temperature over a 1°C Band
- Programmable Temperature Reduction
- Preset Temperature (i.e. Defrost)
- Sensor Failsafe
- Adjustable Hysteresis
- Low External Component Count

ZERO VOLTAGE SWITCH POWER CONTROLLER

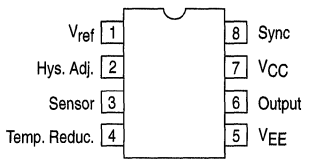
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

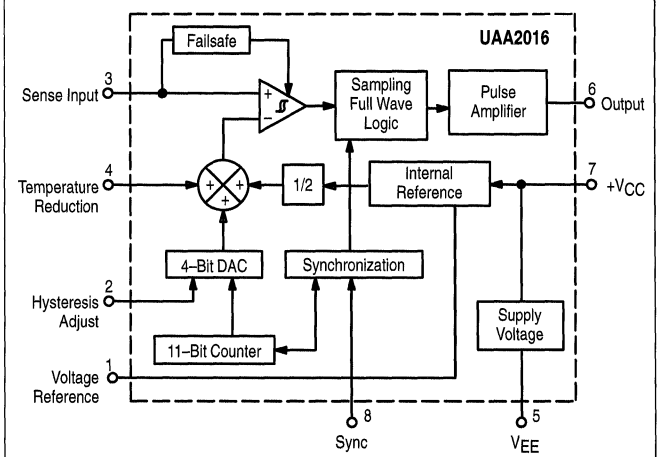
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
UAA2016D	T_A = – 20° to +85°C	SO–8
UAA2016P		Plastic DIP

MAXIMUM RATINGS (Voltages referenced to Pin 7)

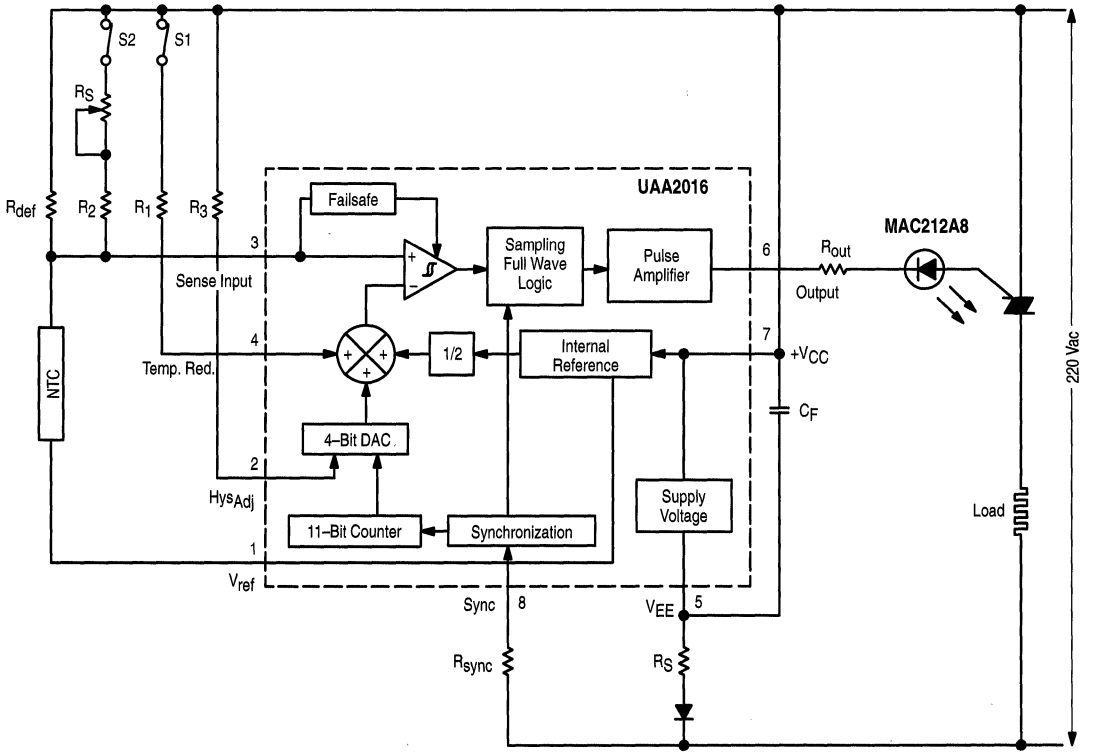
Rating	Symbol	Value	Unit
Supply Current ($I_{Pin\ 5}$)	I_{CC}	15	mA
Non–Repetitive Supply Current (Pulse Width = 1.0 µs)	I_{CCP}	200	mA
AC Synchronization Current	I_{sync}	3.0	mA
Pin Voltages	$V_{Pin\ 2}$ $V_{Pin\ 3}$ $V_{Pin\ 4}$ $V_{Pin\ 6}$	0; V_{ref} 0; V_{ref} 0; V_{ref} 0; V_{EE}	V
V_{ref} Current Sink	$I_{Pin\ 1}$	1.0	mA
Output Current (Pin 6) (Pulse Width < 400 µs)	I_O	150	mA
Power Dissipation	P_D	625	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	– 20 to + 85	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{EE} = –7.0 V, voltages referred to Pin 7, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Pins 6, 8 not connected) (T_A = – 20° to + 85°C)	I_{CC}	—	0.9	1.5	mA
Stabilized Supply Voltage (Pin 5) (I_{CC} = 2.0 mA)	V_{EE}	–10	– 9.0	– 8.0	V
Reference Voltage (Pin 1)	V_{ref}	– 6.5	– 5.5	– 4.5	V
Output Pulse Current (T_A = – 20° to + 85°C) (R_{out} = 60 W, V_{EE} = – 8.0 V)	I_O	90	100	130	mA
Output Leakage Current (V_{out} = 0 V)	I_{OL}	—	—	10	µA
Output Pulse Width (T_A = – 20° to + 85°C) (Note 1) (Mains = 220 Vrms, R_{sync} = 220 kΩ)	T_P	50	—	100	µs
Comparator Offset (Note 5)	V_{off}	–10	—	+10	mV
Sensor Input Bias Current	I_{IB}	—	—	0.1	µA
Sawtooth Period (Note 2)	T_S	—	40.96	—	sec
Sawtooth Amplitude (Note 6)	A_S	50	70	90	mV
Temperature Reduction Voltage (Note 3) (Pin 4 Connected to V_{CC})	V_{TR}	280	350	420	mV
Internal Hysteresis Voltage (Pin 2 Not Connected)	V_{IH}	—	10	—	mV
Additional Hysteresis (Note 4) (Pin 2 Connected to V_{CC})	V_H	280	350	420	mV
Failsafe Threshold (T_A = – 20° to + 85°C) (Note 7)	V_{FSth}	180	—	300	mV

NOTES: 1. Output pulses are centered with respect to zero crossing point. Pulse width is adjusted by the value of R_{sync}. Refer to application curves.
2. The actual sawtooth period depends on the AC power line frequency. It is exactly 2048 times the corresponding period. For the 50 Hz case it is 40.96 sec. For the 60 Hz case it is 34.13 sec. This is to comply with the European standard, namely that 2.0 kW loads cannot be connected or removed from the line more than once every 30 sec.
3. 350 mV corresponds to 5°C temperature reduction. This is tested at probe using internal test pad. Smaller temperature reduction can be obtained by adding an external resistor between Pin 4 and V_{CC}. Refer to application curves.
4. 350 mV corresponds to a hysteresis of 5°C. This is tested at probe using internal test pad. Smaller additional hysteresis can be obtained by adding an external resistor between Pin 2 and V_{CC}. Refer to application curves.
5. Parameter guaranteed but not tested. Worst case 10 mV corresponds to 0.15°C shift on set point.
6. Measured at probe by internal test pad. 70 mV corresponds to 1°C. Note that the proportional band is independent of the NTC value.
7. At very low temperature the NTC resistor increases quickly. This can cause the sensor input voltage to reach the failsafe threshold, thus inhibiting output pulses; refer to application schematics. The corresponding temperature is the limit at which the circuit works in the typical application. By setting this threshold at 0.05 V_{ref}, the NTC value can increase up to 20 times its nominal value, thus the application works below – 20°C.

Figure 1. Application Schematic



APPLICATION INFORMATION

(For simplicity, the LED in series with R_{out} is omitted in the following calculations.)

Triac Choice and R_{out} Determination

Depending on the power in the load, choose the triac that has the lowest peak gate trigger current. This will limit the output current of the UAA2016 and thus its power consumption. Use Figure 4 to determine R_{out} according to the triac maximum gate current (I_{GT}) and the application low temperature limit. For a 2.0 kW load at 220 Vrms, a good triac choice is the Motorola MAC212A8. Its maximum peak gate trigger current at 25°C is 50 mA.

For an application to work down to – 20°C, R_{out} should be 60 Ω. It is assumed that: $I_{GT}(T) = I_{GT}(25°C) \times \exp(-T/125)$ with T in °C, which applies to the MAC212A8.

Output Pulse Width, R_{sync}

The pulse with T_P is determined by the triac's I_{Hold}, I_{Latch} together with the load value and working conditions (frequency and voltage):

Given the RMS AC voltage and the load power, the load value is:

$$R_L = V^2rms/POWER$$

The load current is then:

$$I_{Load} = (Vrms \times \sqrt{2} \times \sin(2\pi ft) - V_{TM})/R_L$$

where V_{TM} is the maximum on state voltage of the triac, f is the line frequency.

Set $I_{Load} = I_{Latch}$ for $t = T_P/2$ to calculate T_P.

Figures 6 and 7 give the value of T_P which corresponds to the higher of the values of I_{Hold} and I_{Latch}, assuming that V_{TM} = 1.6 V. Figure 8 gives the R_{sync} that produces the corresponding T_P.

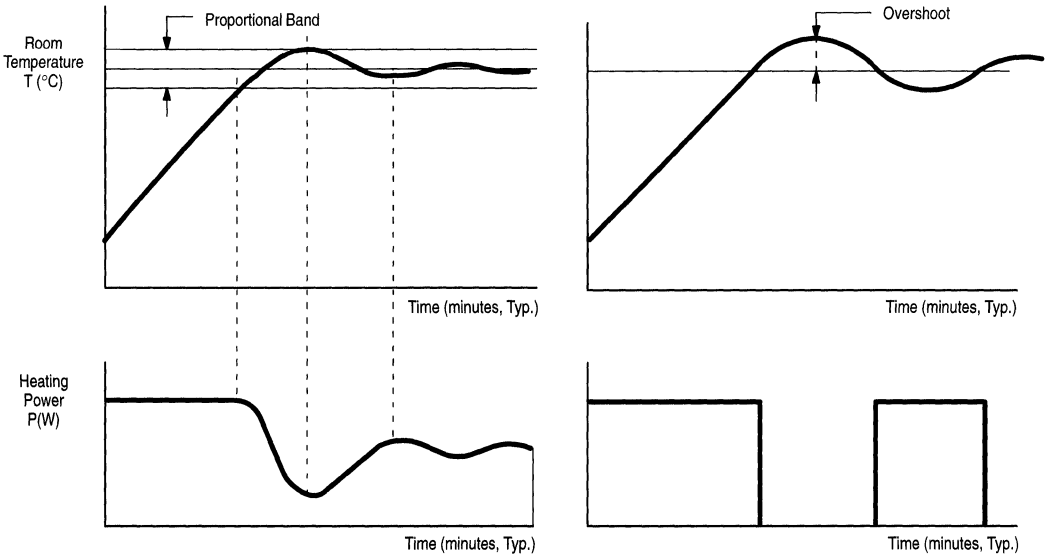
R_{Supply} and Filter Capacitor

With the output current and the pulse width determined as above, use Figures 9 and 10 to determine R_{Supply}, assuming that the sinking current at V_{ref} pin (including NTC bridge current) is less than 0.5 mA. Then use Figure 11 and 12 to determine the filter capacitor (C_F) according to the ripple desired on supply voltage. The maximum ripple allowed is 1.0 V.

Temperature Reduction Determined by R_1

(Refer to Figures 13 and 14.)

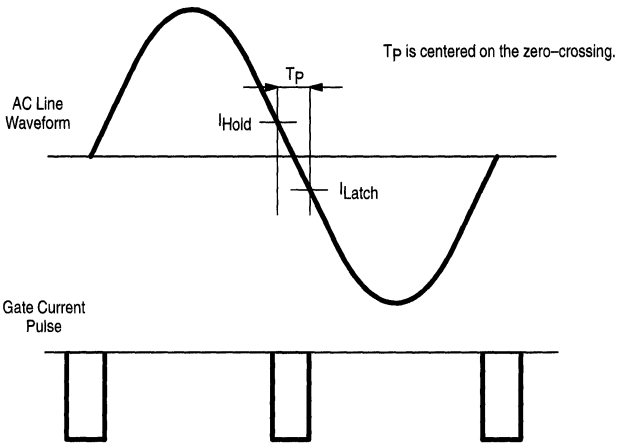
Figure 2. Comparison Between Proportional Control and ON/OFF Control



Proportional Temperature Control
- Reduced Overshoot
- Good Stability

ON/OFF Temperature Control
- Large Overshoot
- Marginal Stability

Figure 3. Zero Voltage Technique



$$T_P = \frac{14 \times R_{sync} + 7 \times 10^5}{Vrms \times \sqrt{2} \times \pi f} (\mu s)$$

f = AC Line Frequency (Hz)
Vrms = AC Line RMS Voltage (V)
R_{sync} = Synchronization Resistor (Ω)

CIRCUIT FUNCTIONAL DESCRIPTION

Power Supply (Pin 5 and Pin 7)

The application uses a current source supplied by a single high voltage rectifier in series with a power dropping resistor. An integrated shunt regulator delivers a V_{EE} voltage of – 8.6 V with respect to Pin 7. The current used by the total regulating system can be shared in four functional blocks: IC supply, sensing bridge, triac gate firing pulses and zener current. The integrated zener, as in any shunt regulator, absorbs the excess supply current. The 50 Hz pulsed supply current is smoothed by the large value capacitor connected between Pins 5 and 7.

4

Temperature Sensing (Pin 3)

The actual temperature is sensed by a negative temperature coefficient element connected in a resistor divider fashion. This two element network is connected between the ground terminal Pin 5 and the reference voltage – 5.5 V available on Pin 1. The resulting voltage, a function of the measured temperature, is applied to Pin 3 and internally compared to a control voltage whose value depends on several elements: Sawtooth, Temperature Reduction and Hysteresis Adjust. (Refer to Application Information.)

Temperature Reduction

For energy saving, a remotely programmable temperature reduction is available on Pin 4. The choice of resistor R_1 connected between Pin 4 and V_{CC} sets the temperature reduction level.

Comparator

When the positive input (Pin 3) receives a voltage greater than the internal reference value, the comparator allows the triggering logic to deliver pulses to the triac gate. To improve the noise immunity, the comparator has an adjustable hysteresis. The external resistor R_3 connected to Pin 2 sets the hysteresis level. Setting Pin 2 open makes a 10 mV hysteresis level, corresponding to 0.15°C. Maximum hysteresis is obtained by connecting Pin 2 to V_{CC}. In that case the level is set at 5°C. This configuration can be useful for low temperature inertia systems.

Sawtooth Generator

In order to comply with European norms, the ON/OFF period on the load must exceed 30 seconds. This is achieved by an internal digital sawtooth which performs the proportional regulation without any additional component. The sawtooth signal is added to the reference applied to the comparator negative input. Figure 2 shows the regulation improvement using the proportional band action.

Noise Immunity

The noisy environment requires good immunity. Both the voltage reference and the comparator hysteresis minimize the noise effect on the comparator input. In addition the effective triac triggering is enabled every 1/3 sec.

Failsafe

Output pulses are inhibited by the "failsafe" circuit if the comparator input voltage exceeds the specified threshold voltage. This would occur if the temperature sensor circuit is open.

Sampling Full Wave Logic

Two consecutive zero–crossing trigger pulses are generated at every positive mains half–cycle. This ensures that the number of delivered pulses is even in every case. The pulse length is selectable by R_{sync} connected on Pin 8. The pulse is centered on the zero–crossing mains waveform.

Pulse Amplifier

The pulse amplifier circuit sinks current pulses from Pin 6 to V_{EE}. The minimum amplitude is 70 mA. The triac is then triggered in quadrants II and III. The effective output current amplitude is given by the external resistor R_{out}. Eventually, an LED can be inserted in series with the Triac gate (see Figure 1).

Figure 4. Output Resistor versus Triac Gate Current

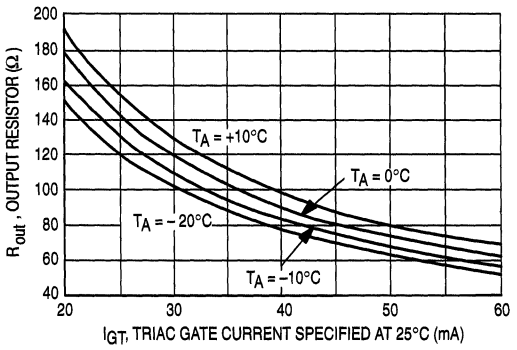


Figure 5. Minimum Output Current versus Output Resistor

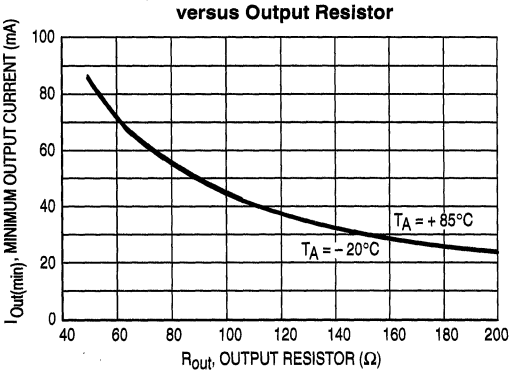


Figure 6. Output Pulse Width versus Maximum Triac Latch Current

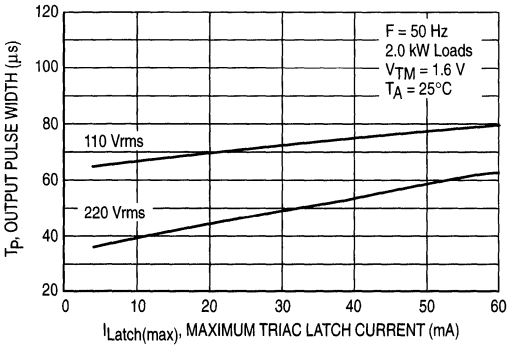
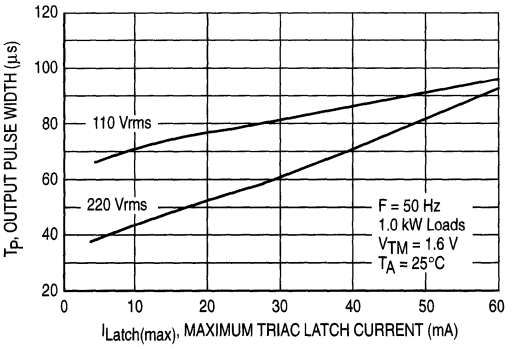


Figure 7. Output Pulse Width versus Maximum Triac Latch Current



4

Figure 8. Synchronization Resistor versus Output Pulse Width

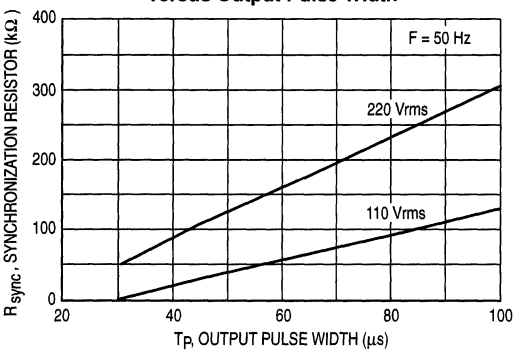


Figure 9. Maximum Supply Resistor versus Output Current

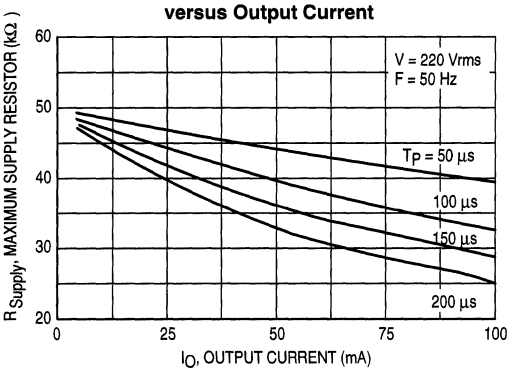


Figure 10. Maximum Supply Resistor versus Output Current

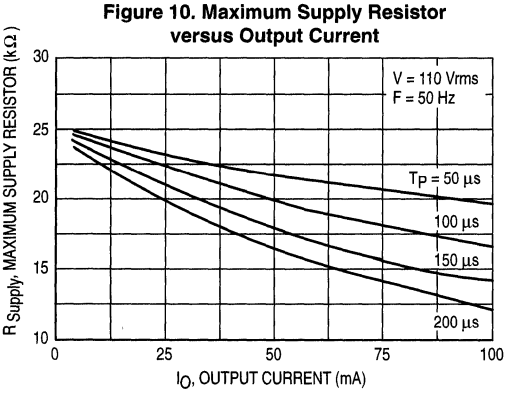


Figure 11. Minimum Filter Capacitor versus Output Current

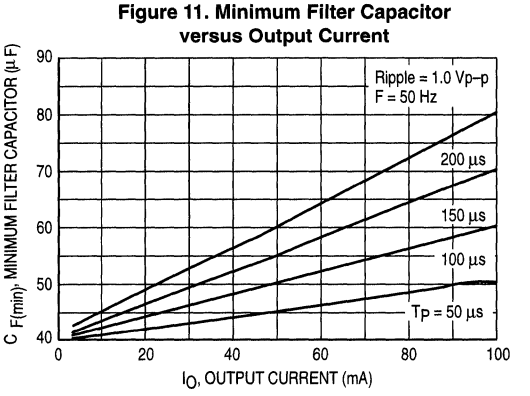


Figure 12. Minimum Filter Capacitor versus Output Current

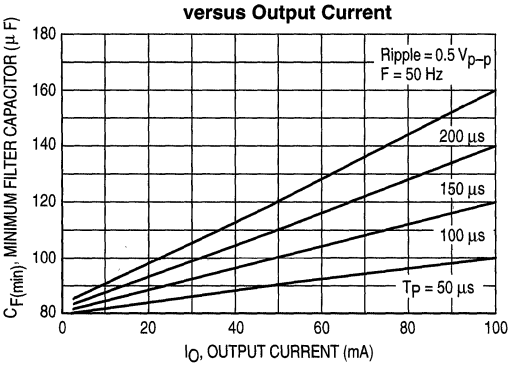


Figure 13. Temperature Reduction versus R_1

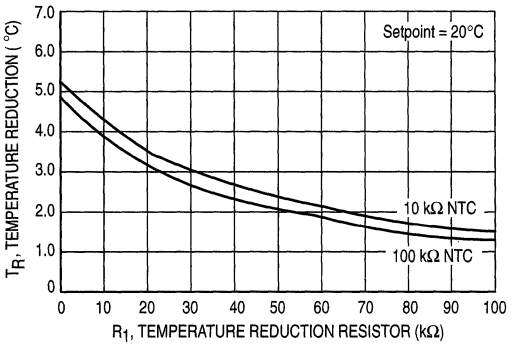


Figure 14. Temperature Reduction versus Temperature Setpoint

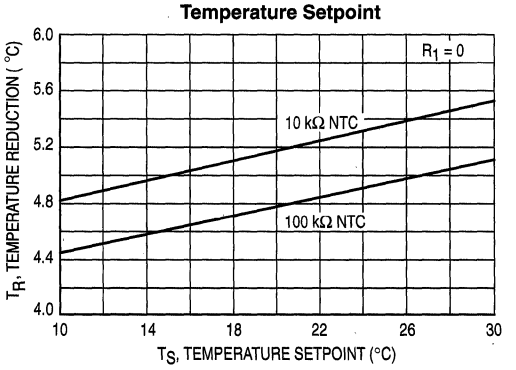


Figure 15. R_{DEF} versus Preset Temperature

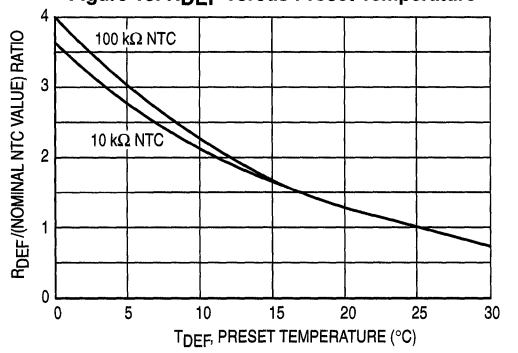


Figure 16. $R_S + R_2$ versus Preset Setpoint

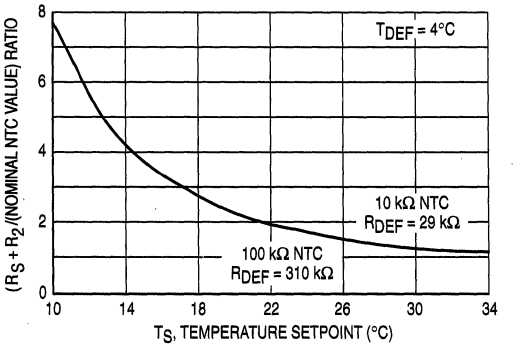
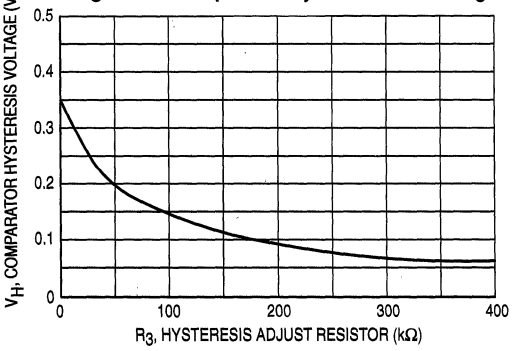


Figure 17. Comparator Hysteresis versus R_3



Tape and Reel Options

In Brief . . .

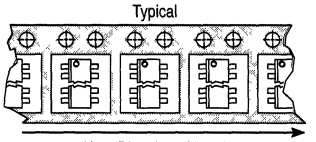
Motorola offers the convenience of Tape and Reel packaging for our growing family of standard integrated circuit products. Reels are available to support the requirements of both first and second generation pick–and–place equipment. The packaging fully conforms to the latest EIA–481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel–back cover tape.

12

Tape and Reel Configurations

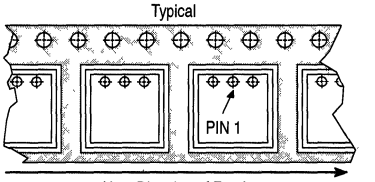
Mechanical Polarization

SOIC and Micro–8 DEVICES
Typical



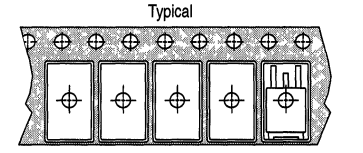
User Direction of Feed

PLCC DEVICES
Typical



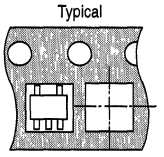
User Direction of Feed

DPAK and D^2PAK DEVICES
Typical



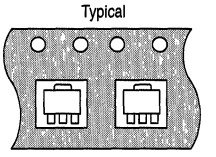
User Direction of Feed

SOT–23 (5 Pin) DEVICES
Typical



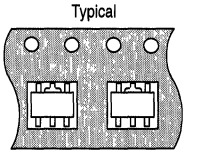
User Direction of Feed

SOT–89 (3 Pin) DEVICES
Typical



User Direction of Feed

SOT–89 (5 Pin) DEVICES
Typical



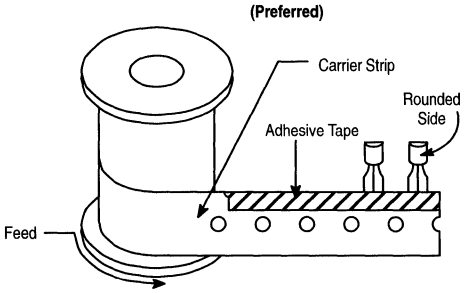
User Direction of Feed

12

Tape and Reel Configurations (continued)

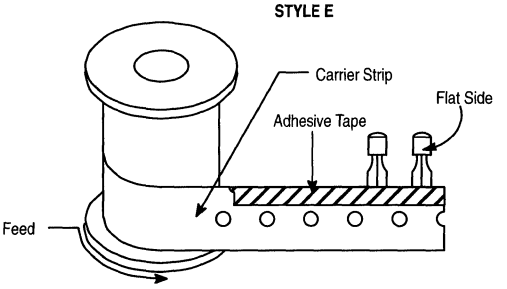
TO–92 Reel Styles

STYLE A
(Preferred)



Rounded side of transistor and adhesive tape visible.

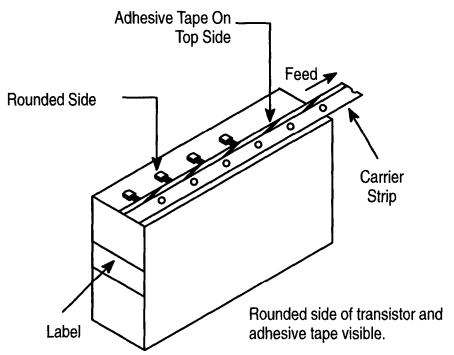
STYLE E



Flat side of transistor and adhesive tape visible.

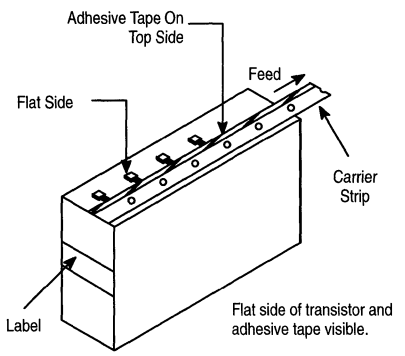
TO–92 Ammo Pack Styles

STYLE P
(Preferred)



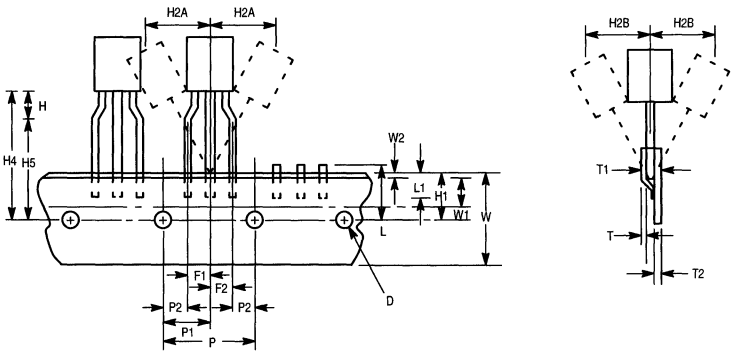
Style P ammo pack is equivalent to Styles A and B of reel pack dependent on feed orientation from box.

STYLE M



Style M ammo pack is equivalent to Style E of reel pack dependent on feed orientation from box.

TO–92 EIA Radial Tape in Fan Fold Box or On Reel



12

Tape and Reel Information Table

Package	Tape Width (mm)	Devices[1] per Reel	Reel Size (inch)	Device Suffix
SO–8, SOP–8	12	2,500	13	R2
SO–14	16	2,500	13	R2
SO–16	16	2,500	13	R2
SO–16L, SO–8+8L WIDE	16	1,000	13	R2
SO–20L WIDE	24	1,000	13	R2
SO–24L WIDE	24	1,000	13	R2
SO–28L WIDE	24	1,000	13	R2
SO–28L WIDE	32	1,000	13	R3
Micro–8	12	2,500	13	R2
PLCC–20	16	1,000	13	R2
PLCC–28	24	500	13	R2
PLCC–44	32	500	13	R2
PLCC–52	32	500	13	R2
PLCC–68	44	250	13	R2
PLCC–84	44	250	13	R2
TO–226AA (TO–92)[2]	18	2,000	13	RA, RE, RP, or RM (Ammo Pack) only
DPAK	16	2,500	13	RK
D^2PAK	24	800	13	R4
SOT–23 (5 Pin)	8	3,000	7	TR
SOT–89 (3/5 Pin)	12	1,000	7	T1

(1) Minimum order quantity is 1 reel. Distributors/OEM customers may break lots or reels at their option, however broken reels may not be returned.
(2) Integrated circuits in TO–226AA packages are available in Styes A and E only, with optional "Ammo Pack" (Suffix RP or RM). The RA and RP configurations are preferred. For ordering information please contact your local Motorola Semiconductor Sales Office.

Analog MPQ Table

Tape/Reel and Ammo Pack

Package Type	Package Code	MPQ
PLCC		
Case 775	0802	1000/reel
Case 776	0804	500/reel
Case 777	0801	500/reel
SOIC		
Case 751	0095	2500/reel
Case 751A	0096	2500/reel
Case 751B	0097	2500/reel
Case 751G	2003	1000/reel
Case 751D	2005	1000/reel
Case 751E	2008	1000/reel
Case 751F	2009	1000/reel
Micro–8		
Case 846A	–	2500/reel
TO–92		
Case 29	0031	2000/reel
Case 29	0031	2000/Ammo Pack
DPAK		
Case 369A	–	2500/reel
D^2PAK		
Case 936	–	800/reel
SOT–23 (5 Pin)		
Case 1212	–	3000/reel
SOT–89 (3 Pin)		
Case 1213	–	1000/reel
SOT–89 (5 Pin)		
Case 1214	–	1000/reel

12

Packaging Information

In Brief . . .

The packaging availability for each device type is indicated on the individual data sheets and the Selector Guide. All of the outline dimensions for the packages are given in this section.

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(TA)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

where:

$P_{D(TA)}$ = *Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.*

$T_{J(max)}$ = *Maximum operating Junction Temperature as listed in the Maximum Ratings Section. See individual data sheets for $T_{J(max)}$ information.*

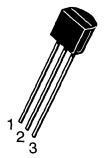
T_A = *Maximum desired operating Ambient Temperature*

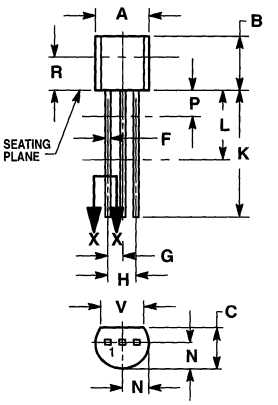
$R_{\theta JA(Typ)}$ = *Typical Thermal Resistance Junction-to-Ambient*

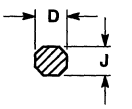
13

Case Outline Dimensions

LP, P, Z SUFFIX
CASE 29-04
Plastic Package
(TO-226AA/TO-92)
ISSUE AD





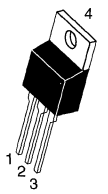


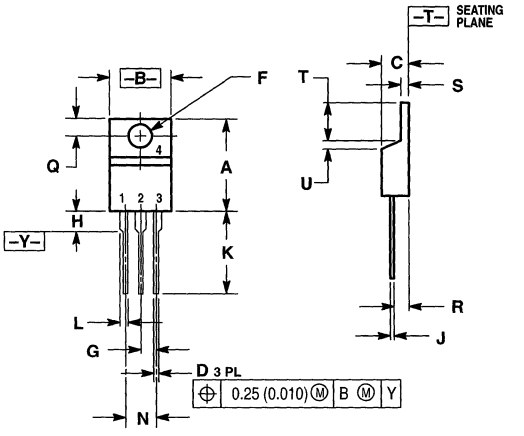
SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

KC, T SUFFIX
CASE 221A-06
Plastic Package
ISSUE Y



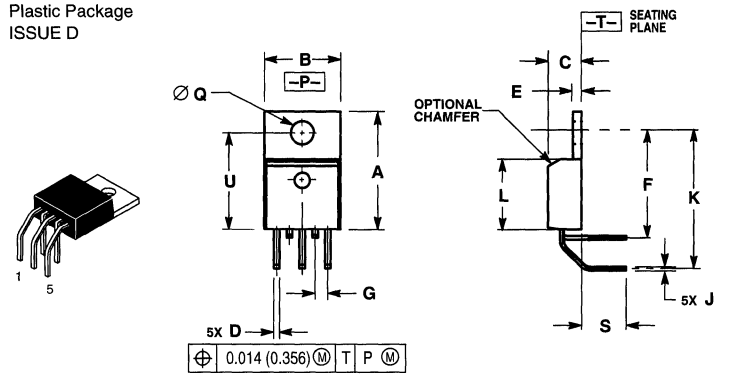


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.155	3.53	3.93
G	0.100 BSC		2.54 BSC	
H	—	0.280	—	7.11
J	0.012	0.045	0.31	1.14
K	0.500	0.580	12.70	14.73
L	0.045	0.070	1.15	1.77
N	0.200 BSC		5.08 BSC	
Q	0.100	0.135	2.54	3.42
R	0.080	0.115	2.04	2.92
S	0.020	0.055	0.51	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27

13

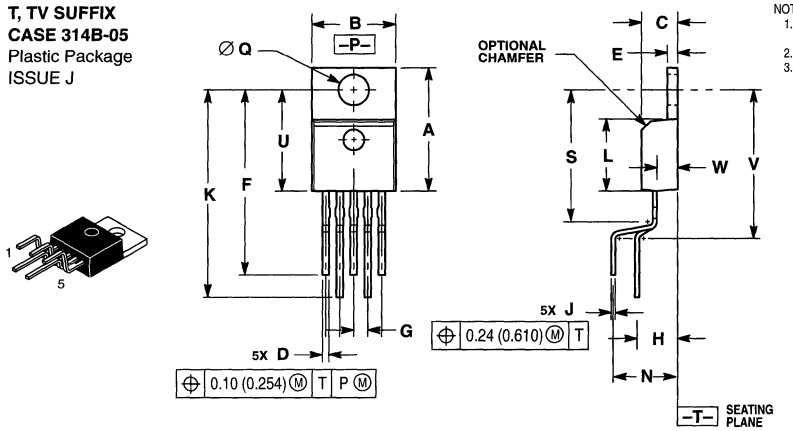
TH SUFFIX
CASE 314A-03
Plastic Package
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.570	0.585	14.478	14.859
G	0.067 BSC		1.702 BSC	
J	0.015	0.025	0.381	0.635
K	0.730	0.745	18.542	18.923
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
S	0.210	0.260	5.334	6.604
U	0.468	0.505	11.888	12.827

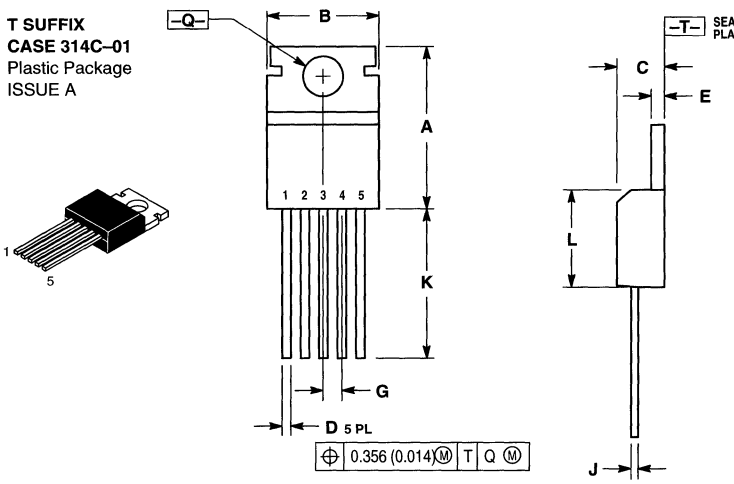
T, TV SUFFIX
CASE 314B-05
Plastic Package
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.850	0.935	21.590	23.749
G	0.067 BSC		1.702 BSC	
H	0.166 BSC		4.216 BSC	
J	0.015	0.025	0.381	0.635
K	0.900	1.100	22.860	27.940
L	0.320	0.365	8.128	9.271
N	0.320 BSC		8.128 BSC	
Q	0.140	0.153	3.556	3.886
S	—	0.620	—	15.748
U	0.468	0.505	11.888	12.827
V	—	0.735	—	18.669
W	0.090	0.110	2.286	2.794

T SUFFIX
CASE 314C–01
Plastic Package
ISSUE A

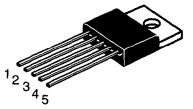


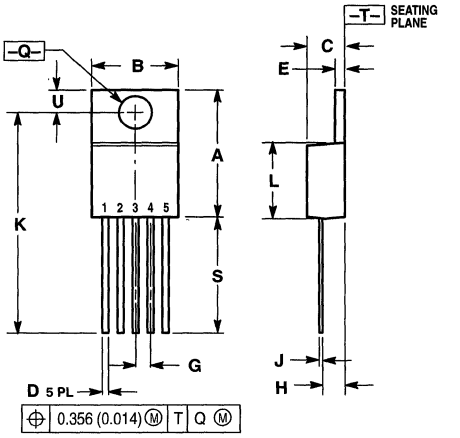
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.610	0.625	15.59	15.88
B	0.380	0.420	9.65	10.67
C	0.160	0.190	4.06	4.83
D	0.020	0.040	0.51	1.02
E	0.035	0.055	0.89	1.40
G	0.067 BSC		1.702 BSC	
J	0.015	0.025	0.38	0.64
K	0.500	—	12.70	—
L	0.355	0.370	9.02	9.40
Q	0.139	0.147	3.53	3.73

13

T, T1 SUFFIX
CASE 314D-03
Plastic Package
ISSUE D

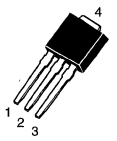


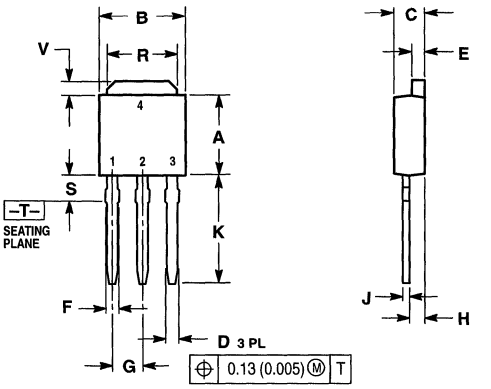


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	1.020	1.065	25.908	27.051
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972
S	0.543	0.582	13.792	14.783

DT-1 SUFFIX
CASE 369-07
Plastic Package
(DPAK)
ISSUE K

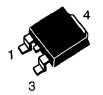


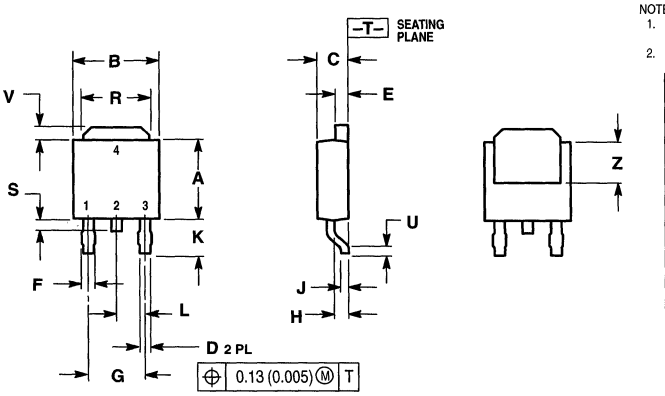


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

DT SUFFIX
CASE 369A-13
Plastic Package
(DPAK)
ISSUE Y



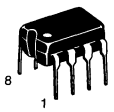


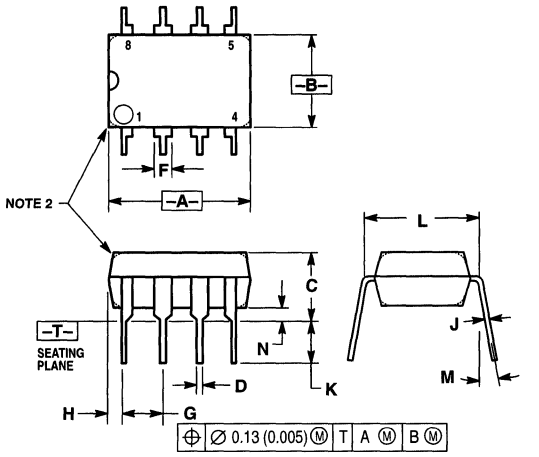
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

13

DP1, N, P, P1 SUFFIX
CASE 626-05
Plastic Package
ISSUE K

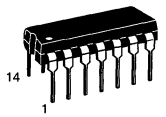


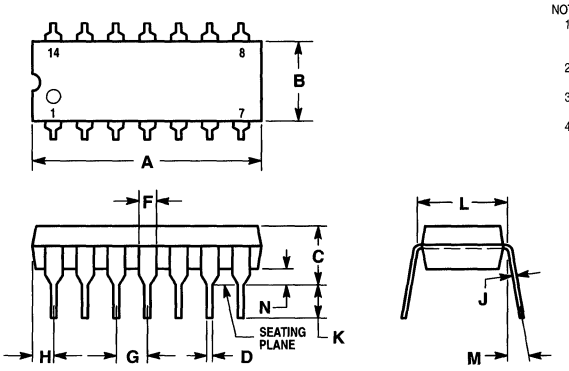


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

N, P, N-14, P2 SUFFIX
CASE 646-06
Plastic Package
ISSUE L

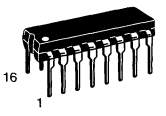


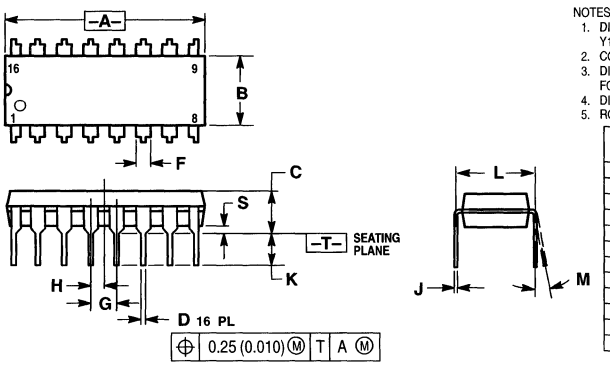


NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

DP2, N, P, PC SUFFIX
CASE 648-08
Plastic Package
ISSUE R



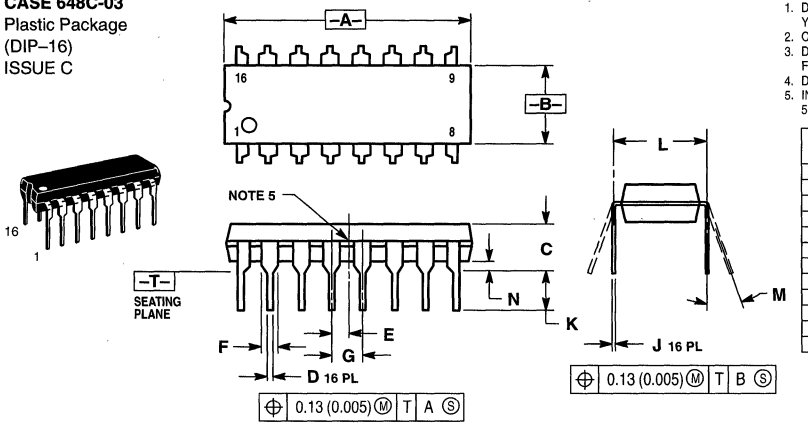


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

13

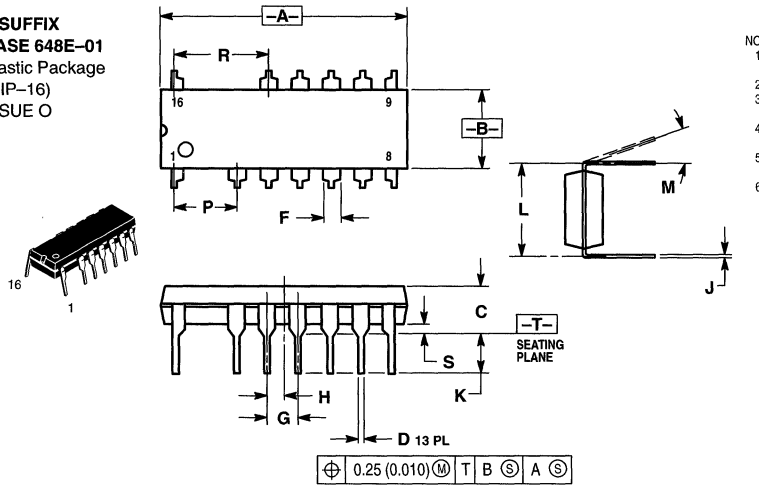
B, P, P2, V SUFFIX
CASE 648C-03
Plastic Package
(DIP–16)
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. INTERNAL LEAD CONNECTION BETWEEN 4 AND 5, 12 AND 13.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.840	18.80	21.34
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
E	0.050 BSC		1.27 BSC	
F	0.040	0.70	1.02	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.040	0.39	1.01

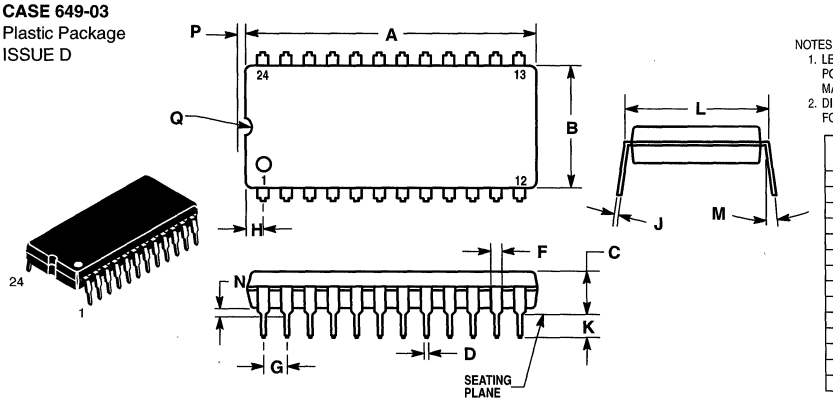
P SUFFIX
CASE 648E–01
Plastic Package
(DIP–16)
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD PROTRUSION.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 (0.010).
6. ROUNDED CORNER OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.760	18.80	19.30
B	0.245	0.260	6.23	6.60
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.120	0.140	3.05	3.55
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
P	0.200 BSC		5.08 BSC	
R	0.300 BSC		7.62 BSC	
S	0.015	0.035	0.39	0.88

P SUFFIX
CASE 649-03
Plastic Package
ISSUE D

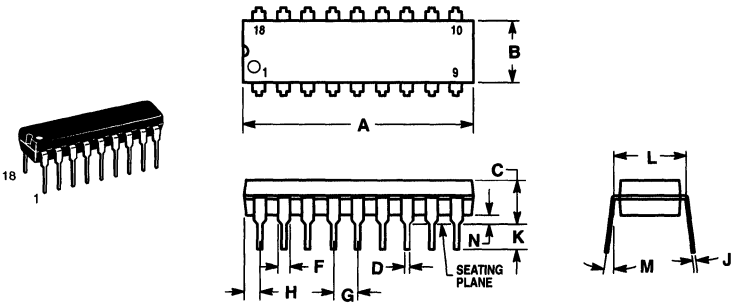


NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

13

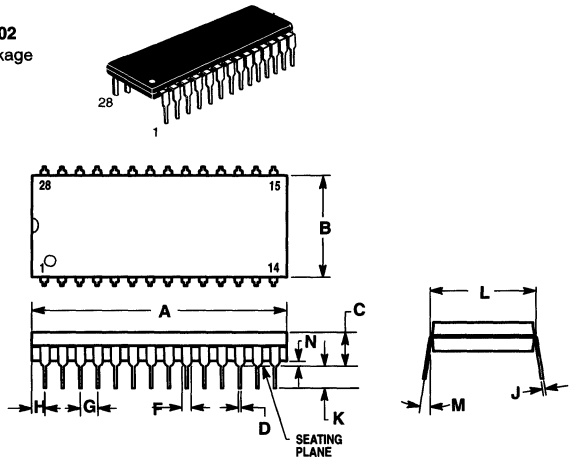
A, B, N, P SUFFIX
CASE 707-02
Plastic Package
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

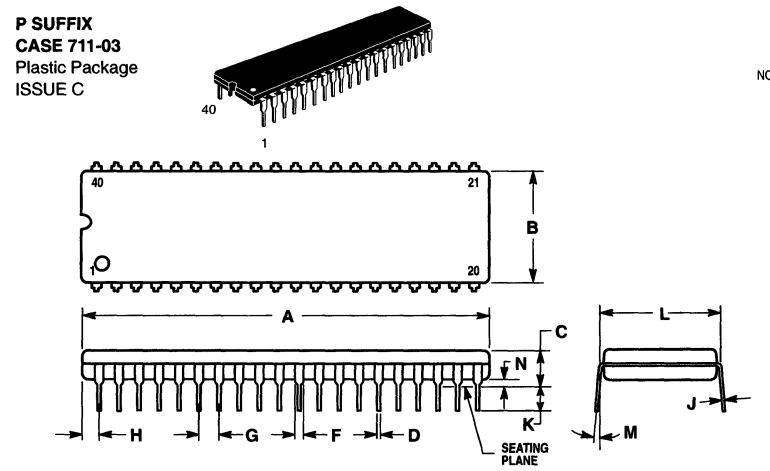
P SUFFIX
CASE 710-02
Plastic Package
ISSUE B



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

P SUFFIX
CASE 711-03
Plastic Package
ISSUE C

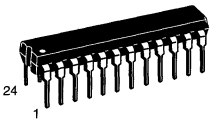


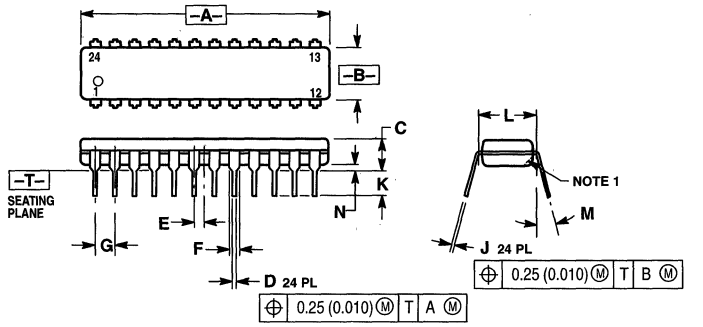
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

13

F, P, P-3 SUFFIX
CASE 724-03
Plastic Package
(NDIP–24)
ISSUE D

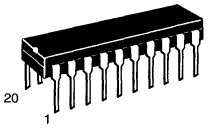


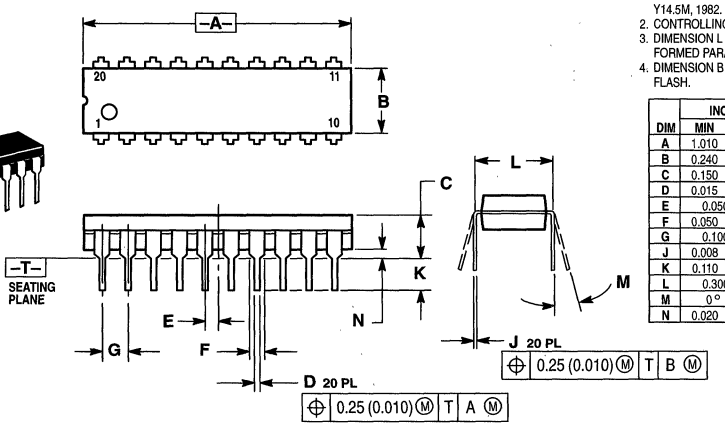


NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

H, P, DP SUFFIX
CASE 738-03
Plastic Package
ISSUE E

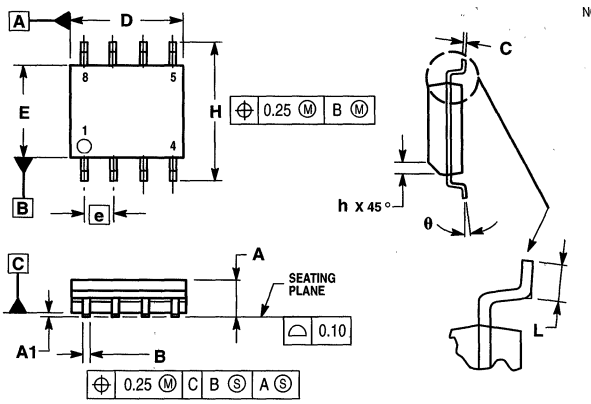




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

D, D1, D2 SUFFIX
CASE 751-05
Plastic Package
(SO-8, SOP-8)
ISSUE R

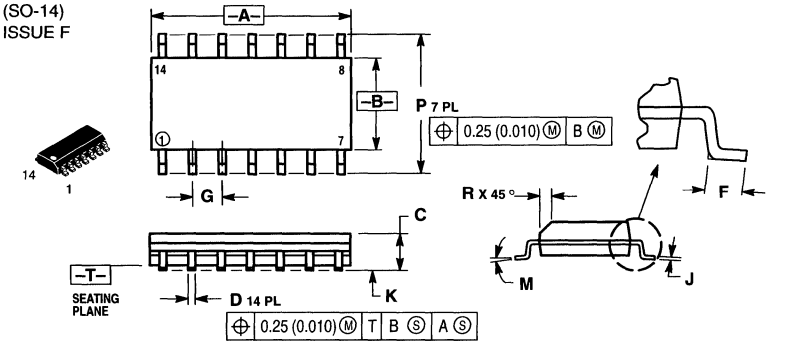


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

13

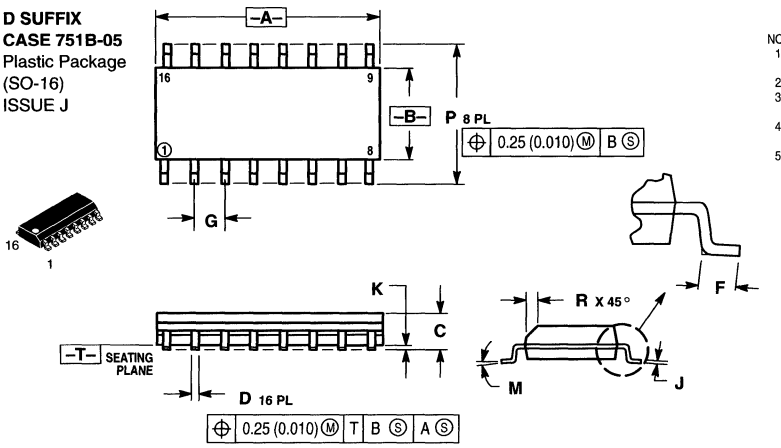
D SUFFIX
CASE 751A-03
Plastic Package
(SO-14)
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

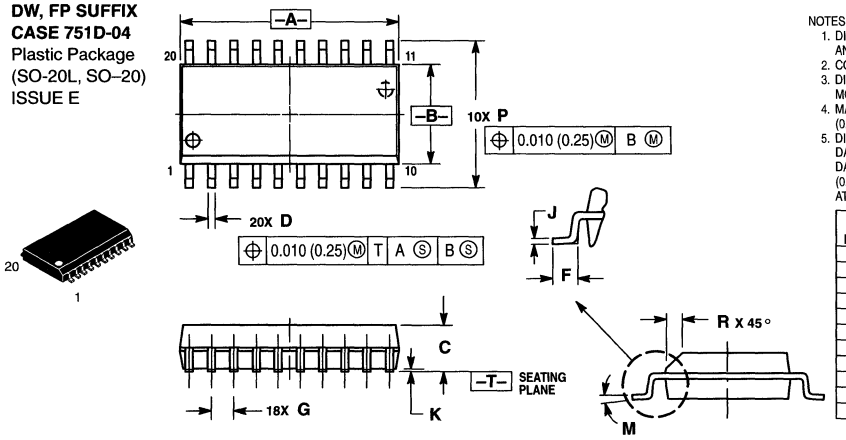
D SUFFIX
CASE 751B-05
Plastic Package
(SO-16)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DW, FP SUFFIX
CASE 751D-04
Plastic Package
(SO-20L, SO-20)
ISSUE E

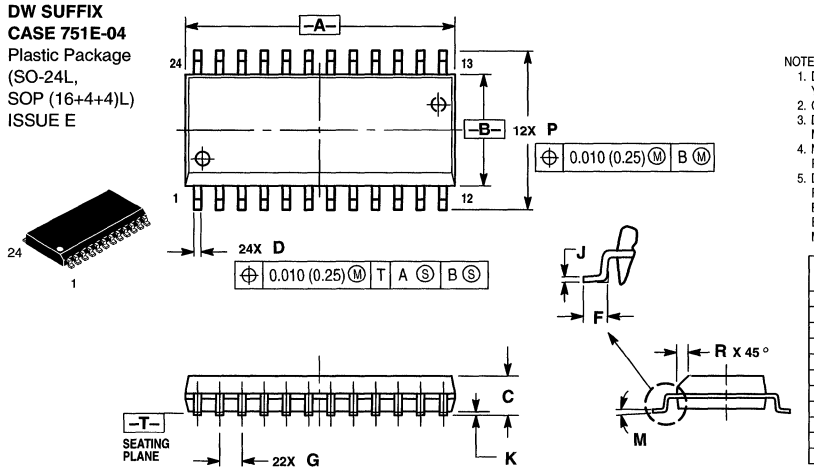


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

13

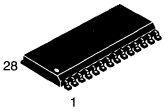
DW SUFFIX
CASE 751E-04
Plastic Package
(SO-24L,
SOP (16+4+4)L)
ISSUE E

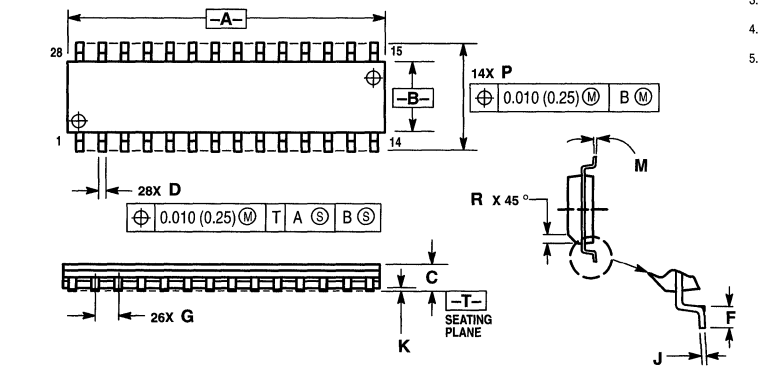


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX
CASE 751F-04
Plastic Package
(SO-28L, SOIC-28)
ISSUE E

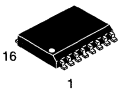


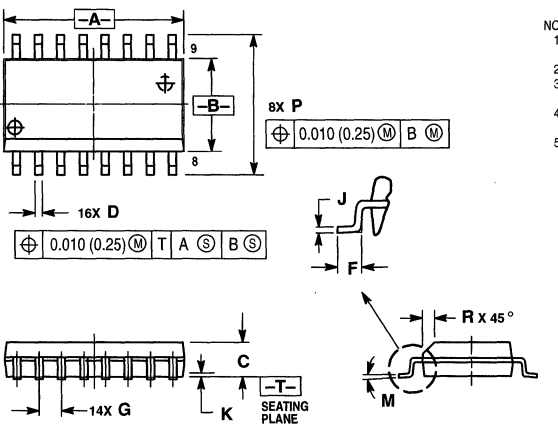


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.01	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX
CASE 751G-02
Plastic Package
(SO-16L, SOP-16L,
SOP-8+8L)
ISSUE A



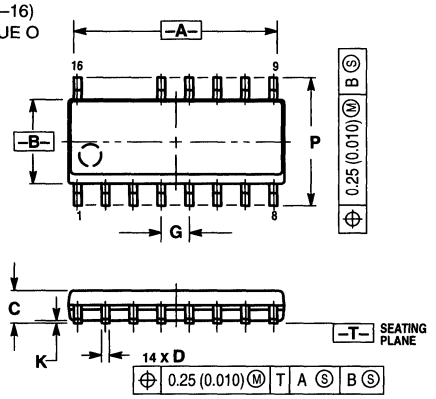


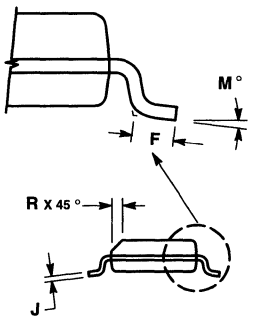
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

13

D SUFFIX
CASE 751K–01
Plastic Package
(SO–16)
ISSUE O

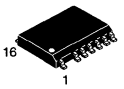


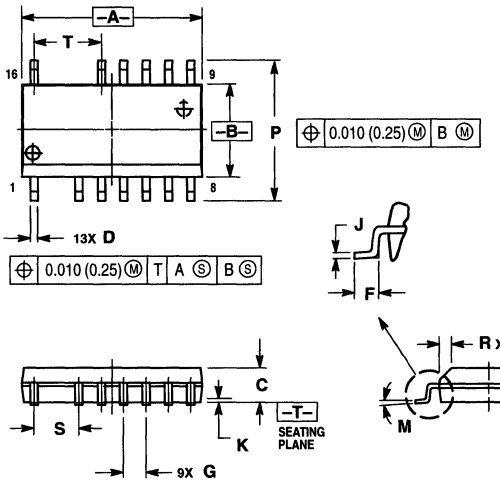


NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4 MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.368	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DW SUFFIX
CASE 751N–01
Plastic Package
(SOP–16L)
ISSUE O



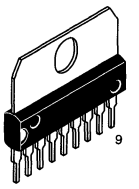


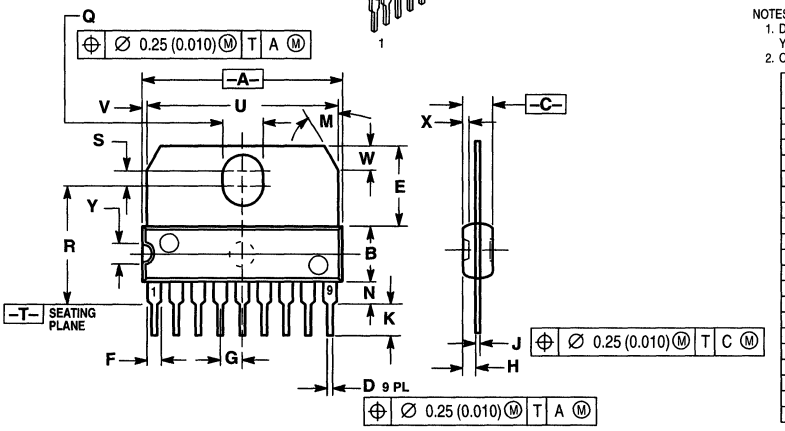
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029
S	2.54 BSC		0.100 BSC	
T	3.81 BSC		0.150 BSC	

13

CASE 762-01
Plastic Medium Power Package
(SIP-9)
ISSUE C

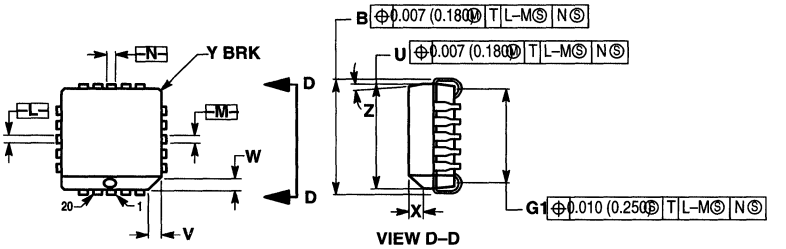




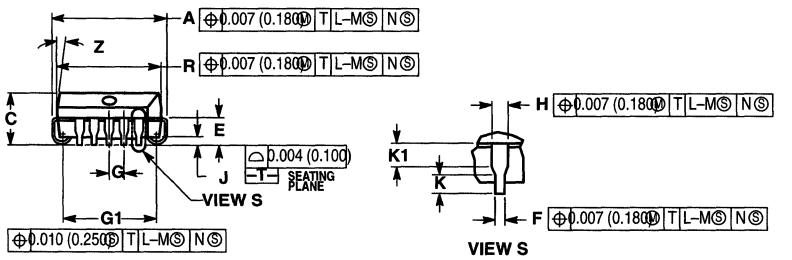
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.40	23.00	0.873	0.897
B	6.40	6.60	0.252	0.260
C	3.45	3.65	0.135	1.143
D	0.40	0.55	0.015	0.021
E	9.35	9.60	0.368	0.377
F	1.40	1.60	0.055	0.062
G	2.54 BSC		0.100 BSC	
H	1.51	1.71	0.059	0.067
J	0.360	0.400	0.014	0.015
K	3.95	4.20	0.155	0.165
M	30° BSC		30° BSC	
N	2.50	2.70	0.099	0.106
Q	3.15	3.45	0.124	0.135
R	13.60	13.90	0.535	0.547
S	1.65	1.95	0.064	0.076
U	22.00	22.20	0.866	0.874
V	0.55	0.75	0.021	0.029
W	2.89 BSC		0.113 BSC	
X	0.65	0.75	0.025	0.029
Y	2.70	2.80	0.106	0.110

FN SUFFIX
CASE 775-02
Plastic Package
(PLCC-20)
ISSUE C



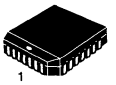
NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

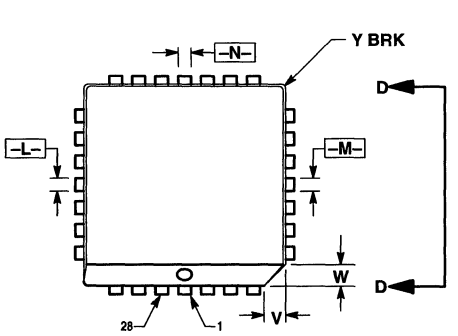


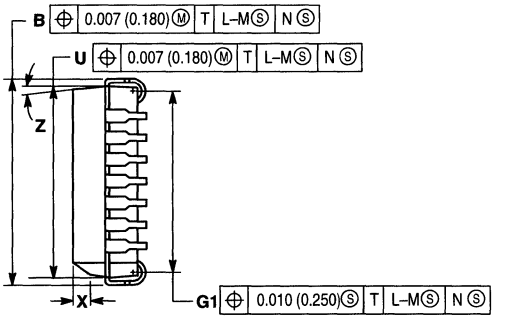
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

13

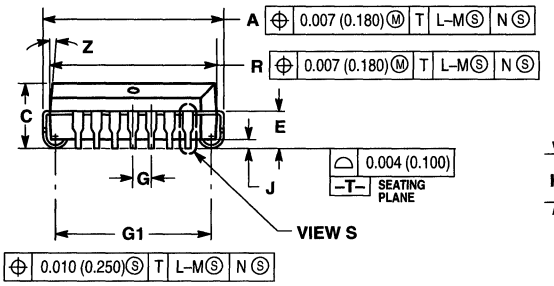
FN SUFFIX
CASE 776-02
Plastic Package
(PLCC–28)
ISSUE D

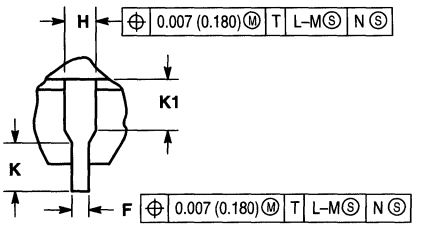






VIEW D–D





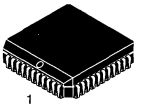
VIEW S

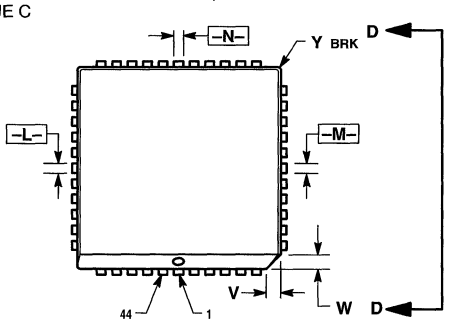
NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

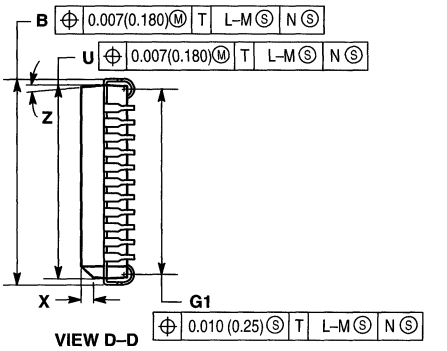
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

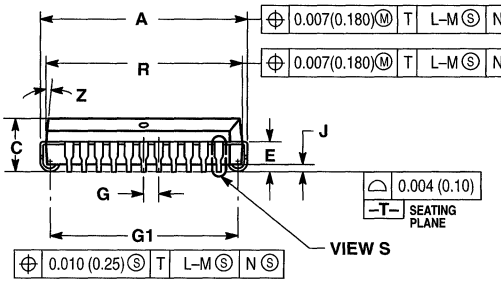
13

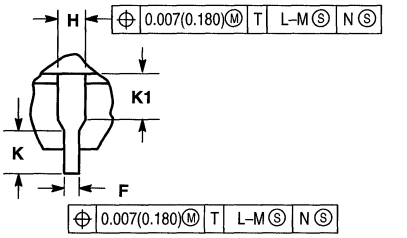
FN SUFFIX
CASE 777-02
Plastic Package
(PLCC)
ISSUE C







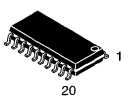


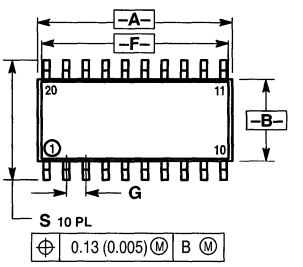


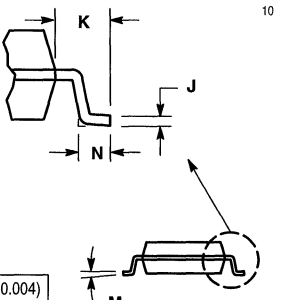
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

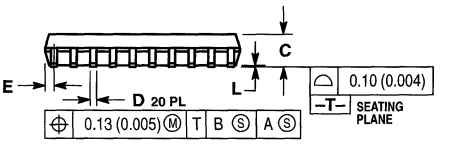
NOTES:
1. DATUMS -L-, -M-, AND -N- ARE DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

M SUFFIX
CASE 803C
PRELIMINARY
Plastic Package









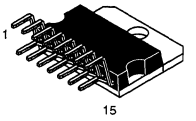
NOTES:
6 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
7 CONTROLLING DIMENSION: MILLIMETER.
8 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
9 MAXIMUM MOLD PROTRUSION 0.15 (0.008) PER SIDE.
10 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.006) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

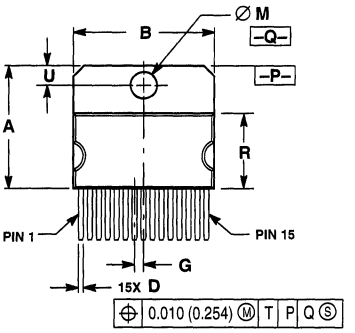
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.35	12.80	0.486	0.504
B	5.10	5.45	0.201	0.215
C	1.95	2.05	0.077	0.081
D	0.35	0.50	0.014	0.020
E	—	0.81	—	0.032
F	12.40*		0.488*	
G	1.15	1.39	0.045	0.055
H	0.59	0.81	0.023	0.032
J	0.18	0.27	0.007	0.011
K	1.10	1.50	0.043	0.059
L	0.05	0.20	0.001	0.008
M	0°	10°	0°	10°
N	0.50	0.85	0.020	0.033
S	7.40	8.20	0.291	0.323

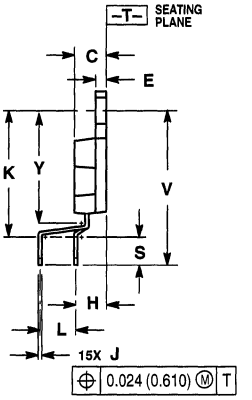
*APPROXIMATE

13

TV SUFFIX
CASE 821C-04
Plastic Package
(15-Pin ZIP)
ISSUE D



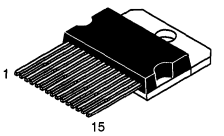


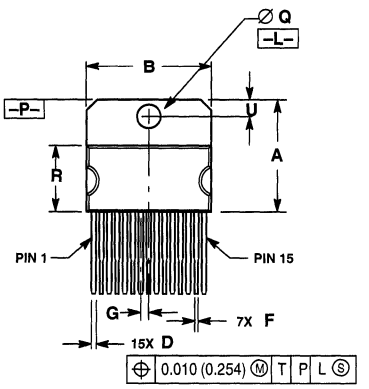


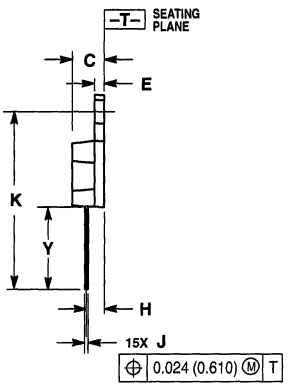
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 (0.250).
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION. AT MAXIMUM MATERIAL CONDITION.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.684	0.694	17.374	17.627
B	0.784	0.792	19.914	20.116
C	0.173	0.181	4.395	4.597
D	0.024	0.031	0.610	0.787
E	0.058	0.062	1.473	1.574
G	0.050 BSC		1.270 BSC	
H	0.169 BSC		4.293 BSC	
J	0.018	0.024	0.458	0.609
K	0.700	0.710	17.780	18.034
L	0.200 BSC		5.080 BSC	
M	0.148	0.151	3.760	3.835
R	0.416	0.426	10.567	10.820
S	0.157	0.167	3.988	4.242
U	0.105	0.115	2.667	2.921
V	0.868 REF		22.047 REF	
Y	0.625	0.639	15.875	16.231

T SUFFIX
CASE 821D-03
Plastic Package
ISSUE C





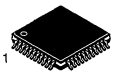


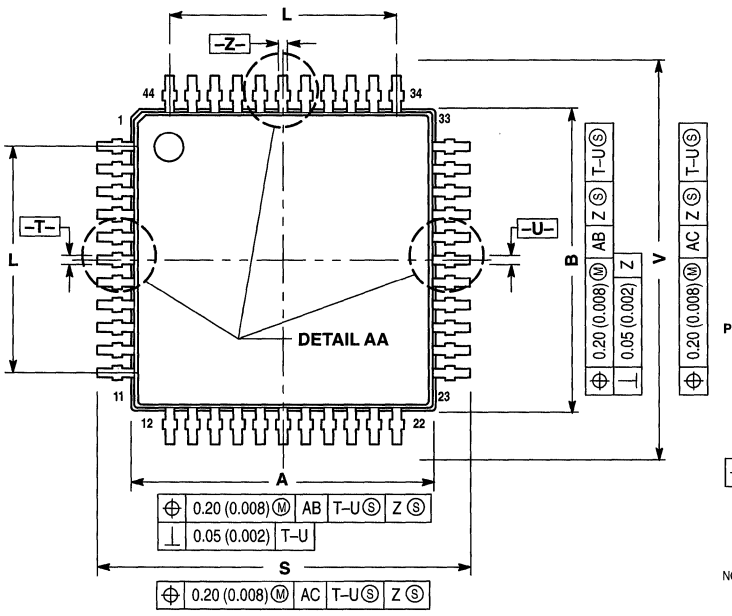
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 (0.250).
6. DELETED
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION. AT MAXIMUM MATERIAL CONDITION.

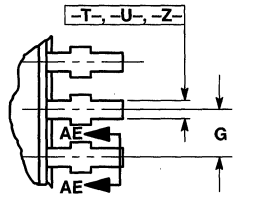
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.681	0.694	17.298	17.627
B	0.784	0.792	19.914	20.116
C	0.173	0.181	4.395	4.597
D	0.024	0.031	0.610	0.787
E	0.058	0.062	1.473	1.574
F	0.016	0.023	0.407	0.584
G	0.050 BSC		1.270 BSC	
H	0.110 BSC		2.794 BSC	
J	0.018	0.024	0.458	0.609
K	1.078	1.086	27.382	27.584
Q	0.148	0.151	3.760	3.835
R	0.416	0.426	10.567	10.820
U	0.110 BSC		2.794 BSC	
Y	0.503 REF		12.776 REF	

13

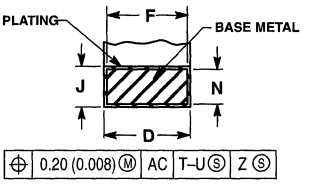
FTB SUFFIX
CASE 824D–01
Plastic Package
(TQFP–44)
ISSUE O



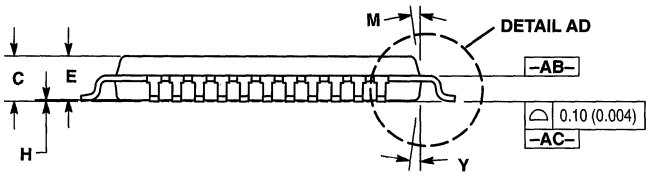


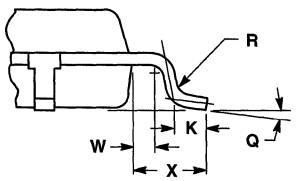


DETAIL AA



SECTION AE–AE





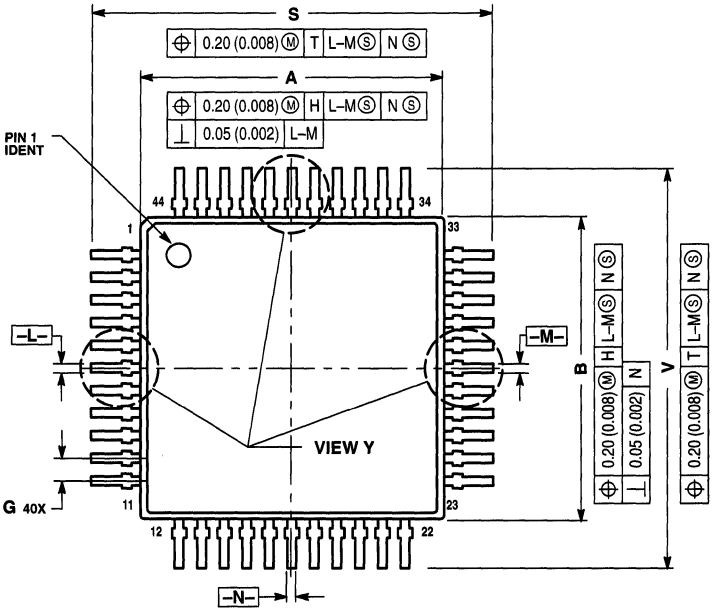
VIEW AD

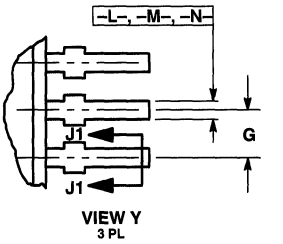
NOTES.
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U– AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.530 (0.021).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.950	10.050	0.392	0.396
B	9.950	10.050	0.392	0.396
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.550	0.018	0.022
L	8.000 BSC		0.315 BSC	
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
Q	1°	5°	1°	5°
R	0.100	0.200	0.004	0.008
S	11.900	12.100	0.469	0.476
V	11.900	12.100	0.469	0.476
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	
Y	12° REF		12° REF	

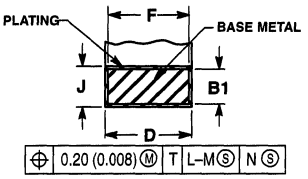
13

FB SUFFIX
CASE 824E–02
Plastic Package
(QFP)
ISSUE A



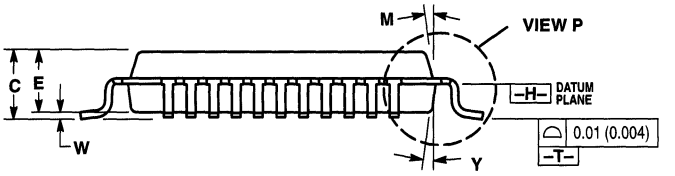


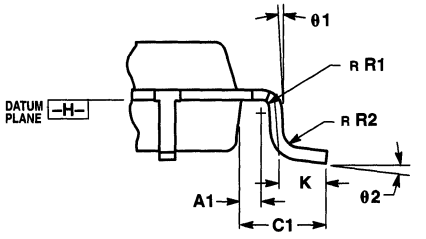
VIEW Y
3 PL



SECTION J1–J1
44 PL

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.530 (0.021).



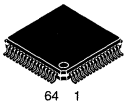


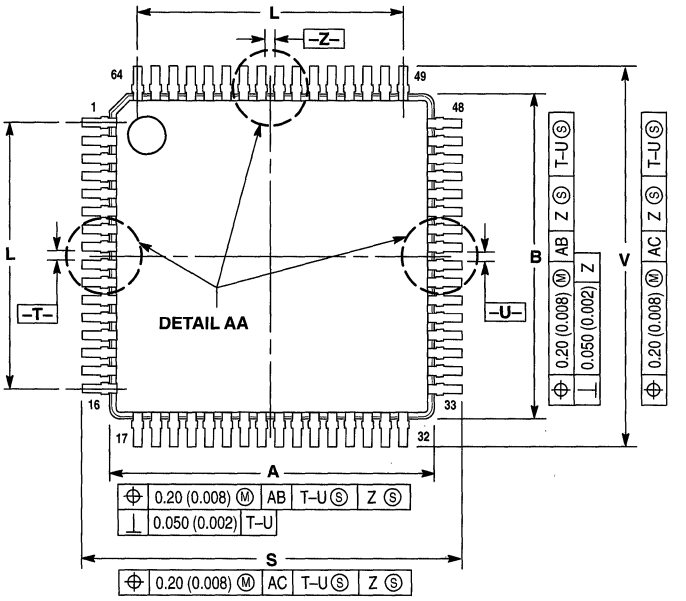
VIEW P

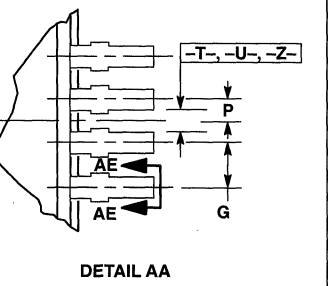
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.00	2.21	0.079	0.087
D	0.30	0.45	0.0118	0.0177
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
M	5°	10°	5°	10°
S	12.95	13.45	0.510	0.530
V	12.95	13.45	0.510	0.530
W	0.000	0.210	0.000	0.008
Y	5°	10°	5°	10°
A1	0.450 REF		0.018 REF	
B1	0.130	0.170	0.005	0.007
C1	1.600 REF		0.063 REF	
R1	0.130	0.300	0.005	0.012
R2	0.130	0.300	0.005	0.012
θ1	5°	10°	5°	10°
θ2	0°	7°	0°	7°

13

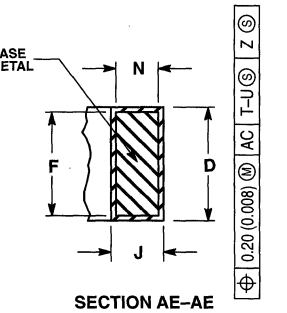
FB SUFFIX
CASE 840F–01
Plastic Package
ISSUE O



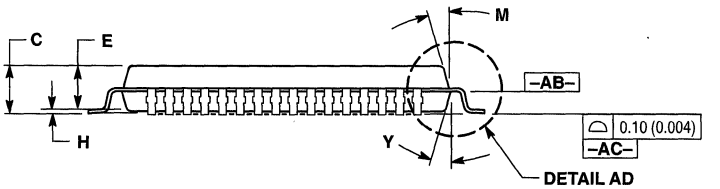




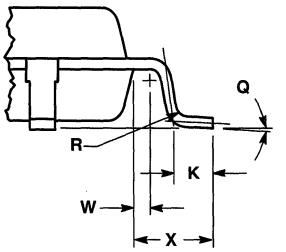
DETAIL AA



SECTION AE–AE



DETAIL AD



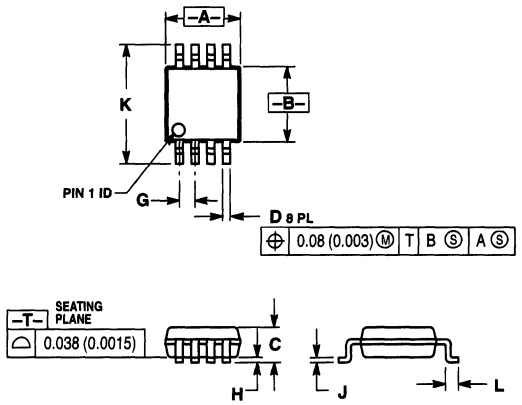
DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U– AND –Z– TO BE DETERMINED AT DATUM PLANE –AC–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.950	10.050	0.392	0.396
B	9.950	10.050	0.392	0.396
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.550	0.018	0.022
L	7.500 BSC		0.295 BSC	
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.250 BSC		0.010 BSC	
Q	1°	5°	1°	5°
R	0.100	0.200	0.004	0.008
S	11.900	12.100	0.469	0.476
V	11.900	12.100	0.469	0.476
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	
Y	12° REF		12° REF	

13

DM SUFFIX
CASE 846A–02
Plastic Package
(Micro–8)
ISSUE C

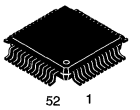


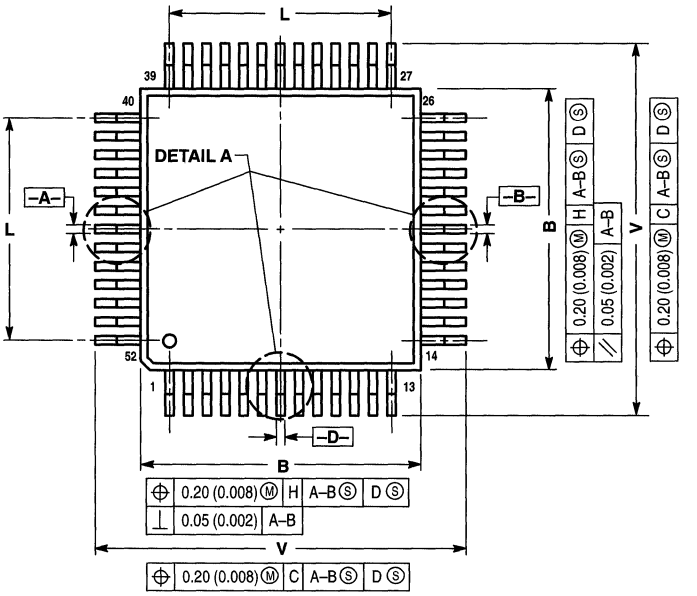
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

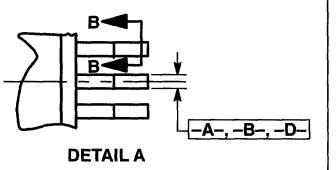
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	—	1.10	—	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

13

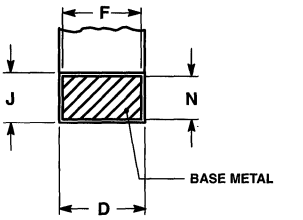
FB SUFFIX
CASE 848B-04
Plastic Package
(TQFP–52)
ISSUE C



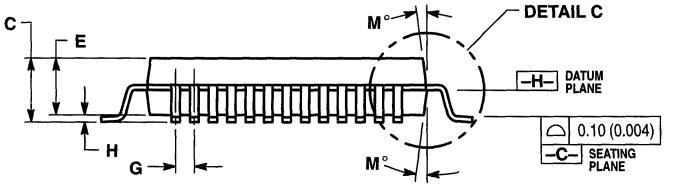


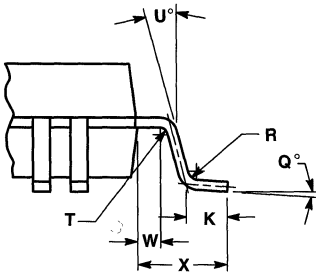


DETAIL A



SECTION B–B





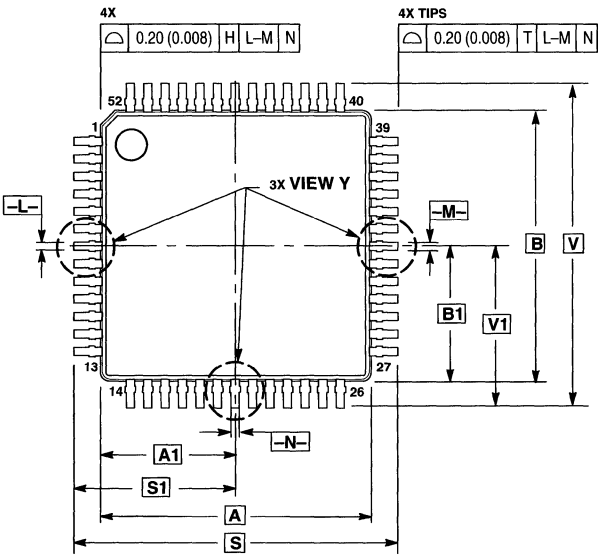
DETAIL C

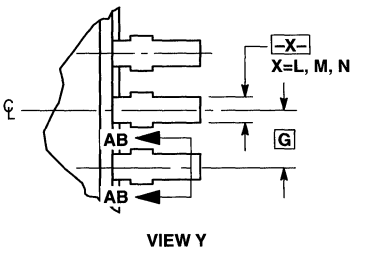
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

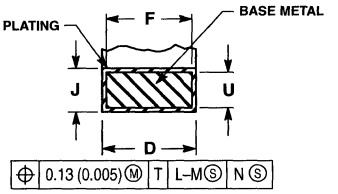
13

FB SUFFIX
CASE 848D–03
Plastic Package
ISSUE C

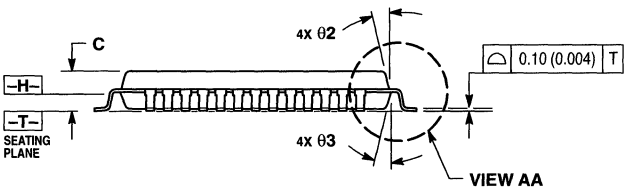




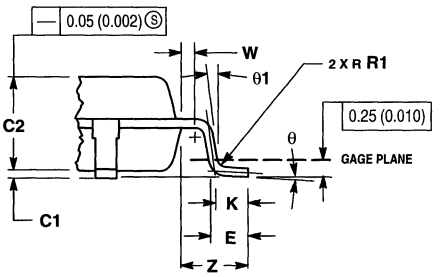
VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE



VIEW AA



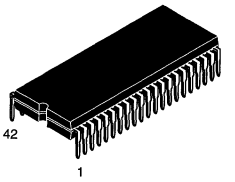
VIEW AA

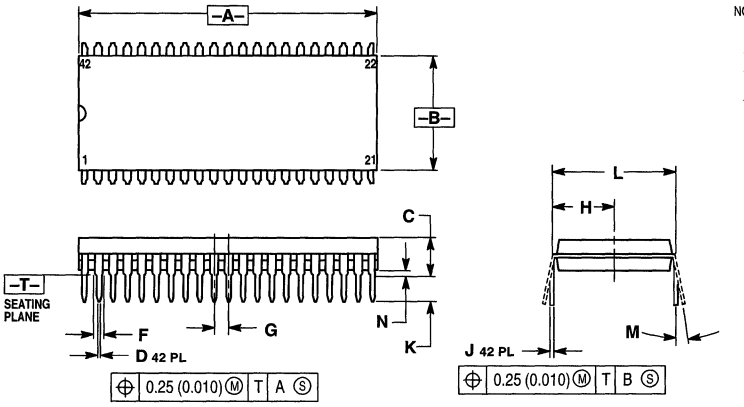
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	5°	13°	5°	13°

13

B SUFFIX
CASE 858–01
Plastic Package
ISSUE O

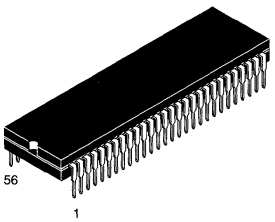


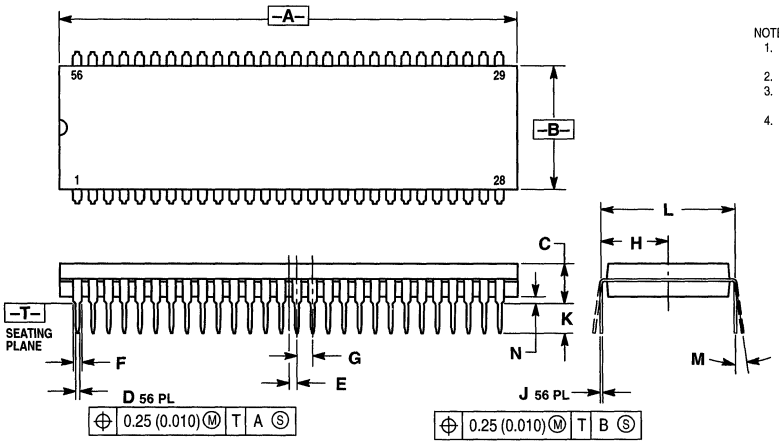


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

B SUFFIX
CASE 859–01
Plastic Package
(SDIP)
ISSUE O



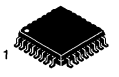


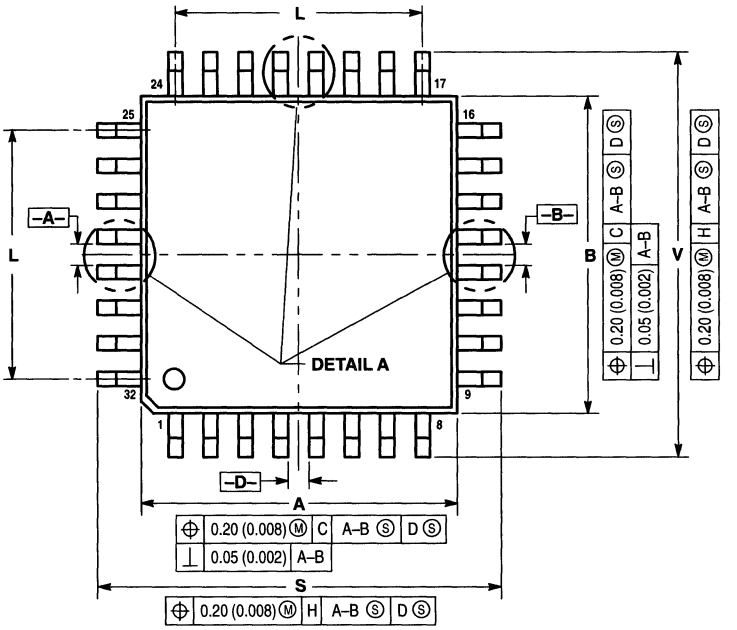
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010)

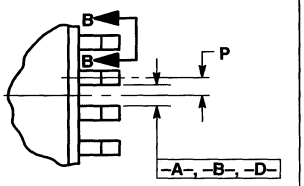
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.035	2.065	51.69	52.45
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
E	0.035 BSC		0.89 BSC	
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

13

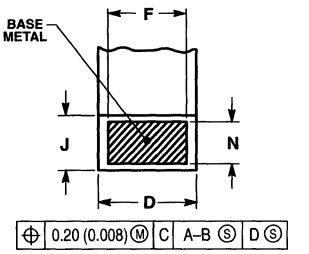
FB, FTB SUFFIX
CASE 873-01
Plastic Package
(TQFP–32)
ISSUE A



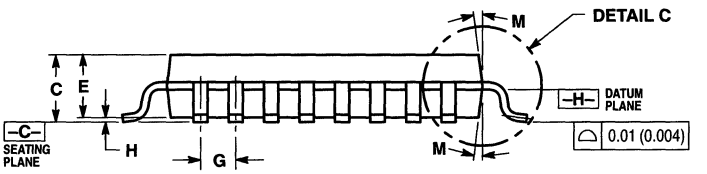


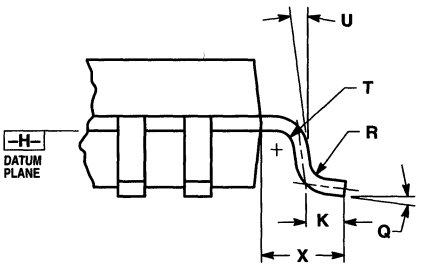


DETAIL A



SECTION B–B
VIEW ROTATED 90 ° CLOCKWISE





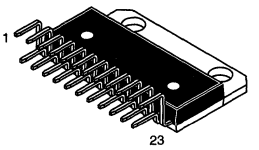
DETAIL C

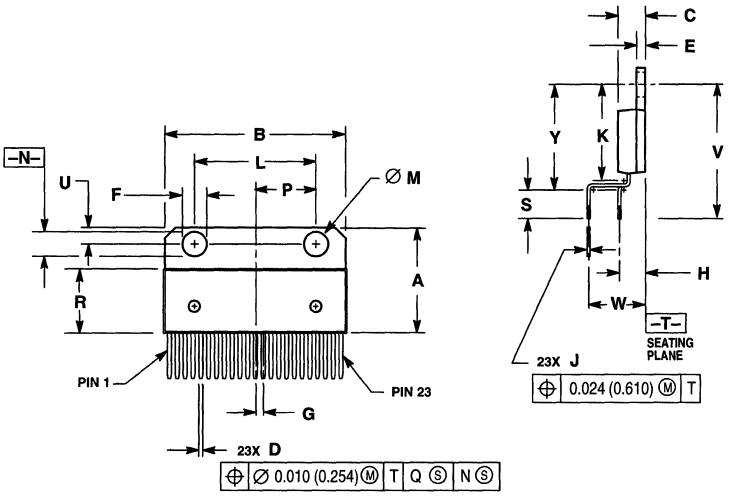
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.00 REF		0.039 REF	

13

T SUFFIX
CASE 894-03
Plastic Package
(23-Pin SZIP)
ISSUE B



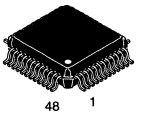


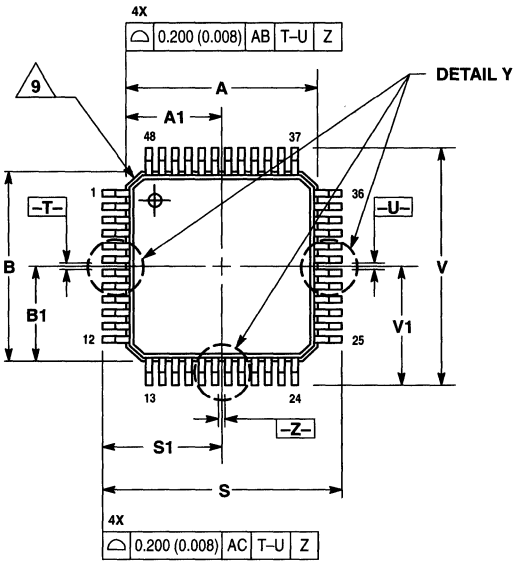
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 (0.250).
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

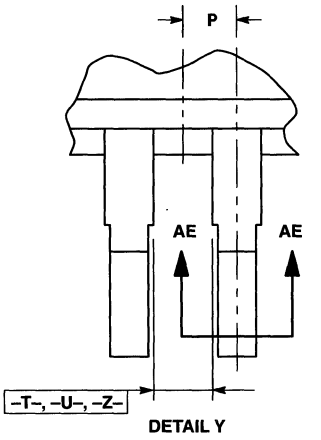
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.684	0.694	17.374	17.627
B	1.183	1.193	30.048	30.302
C	0.175	0.179	4.445	4.547
D	0.026	0.031	0.660	0.787
E	0.058	0.062	1.473	1.574
F	0.165	0.175	4.191	4.445
G	0.050 BSC		1.270 BSC	
H	0.169 BSC		4.293 BSC	
J	0.014	0.020	0.356	0.508
K	0.625	0.639	15.875	16.231
L	0.770	0.790	19.558	20.066
M	0.148	0.152	3.760	3.861
N	0.148	0.152	3.760	3.861
P	0.390 BSC		9.906 BSC	
R	0.416	0.424	10.566	10.770
S	0.157	0.167	3.988	4.242
U	0.105	0.115	2.667	2.921
V	0.868 REF		22.047 REF	
W	0.200 BSC		5.080 BSC	
Y	0.700	0.710	17.780	18.034

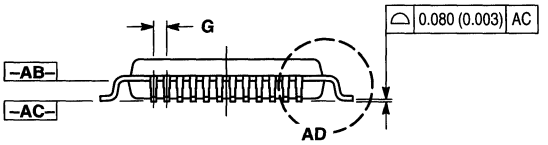
13

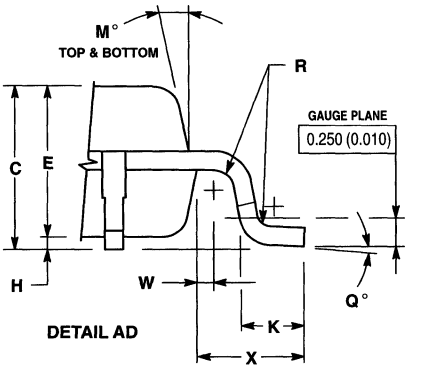
FTA SUFFIX
CASE 932–02
Plastic Package
(TQFP–48)
ISSUE D

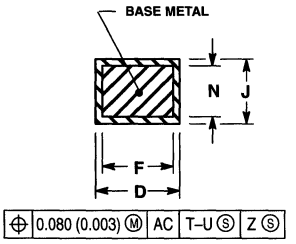










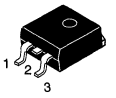


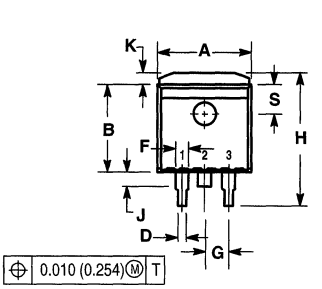
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

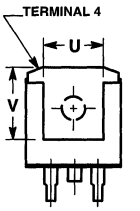
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BASIC		0.020 BASIC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12 °REF		12 °REF	
N	0.090	0.160	0.004	0.006
P	0.250 BASIC		0.010 BASIC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

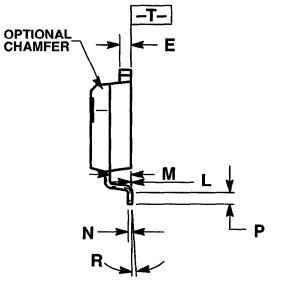
13

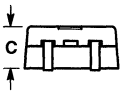
D2T SUFFIX
CASE 936–03
Plastic Package
ISSUE B







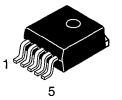


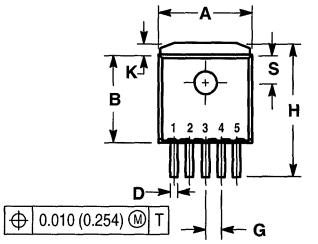


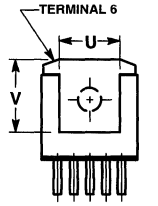
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

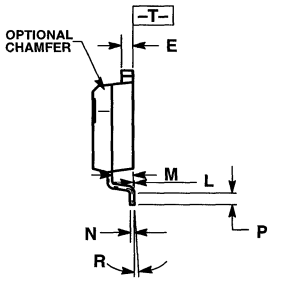
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

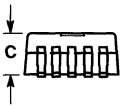
D2T SUFFIX
CASE 936A–02
Plastic Package
(D^2PAK)
ISSUE A









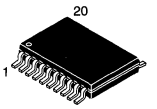


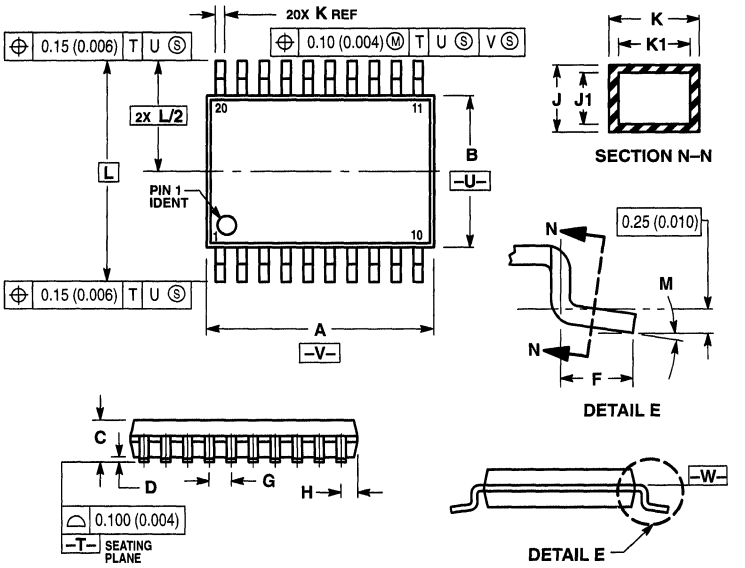
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

13

DT, DTB SUFFIX
CASE 948E–02
Plastic Package
(TSSOP–20)
ISSUE A

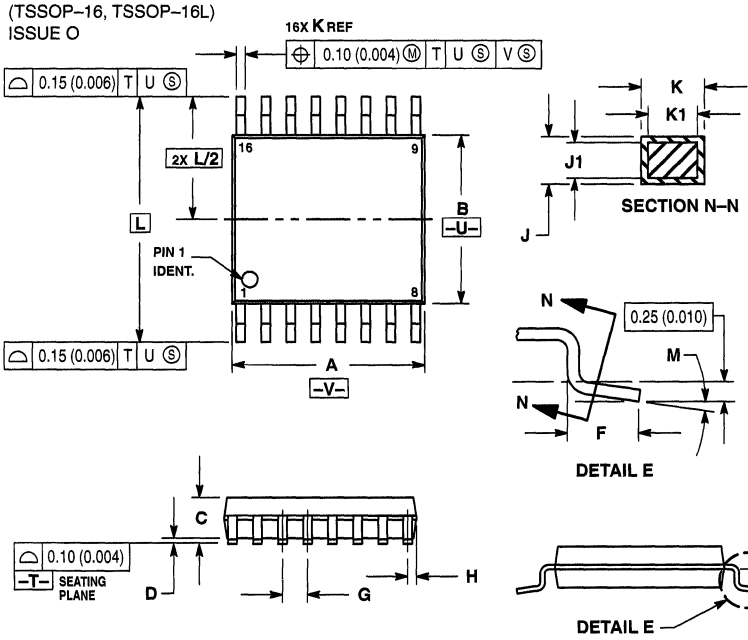




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

DTB SUFFIX
CASE 948F–01
Plastic Package
(TSSOP–16, TSSOP–16L)
ISSUE O

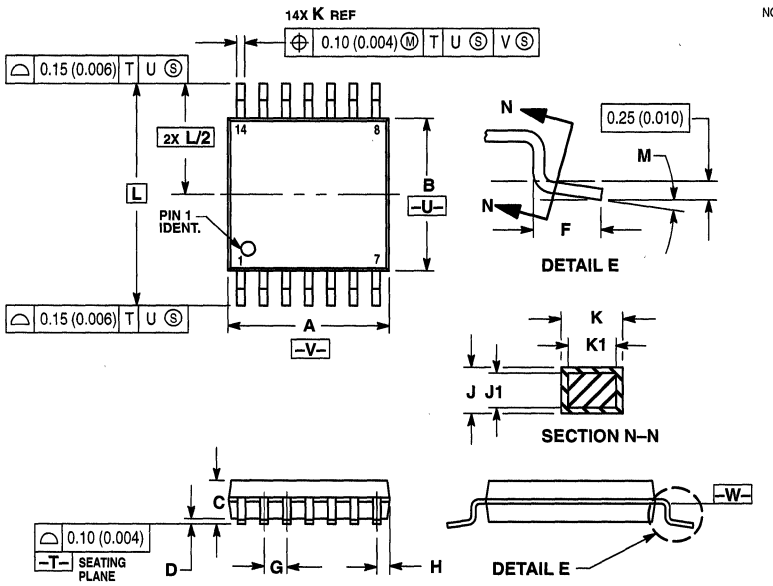


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

13

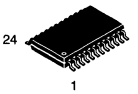
DTB SUFFIX
CASE 948G–01
Plastic Package
(TSSOP–14)
ISSUE O

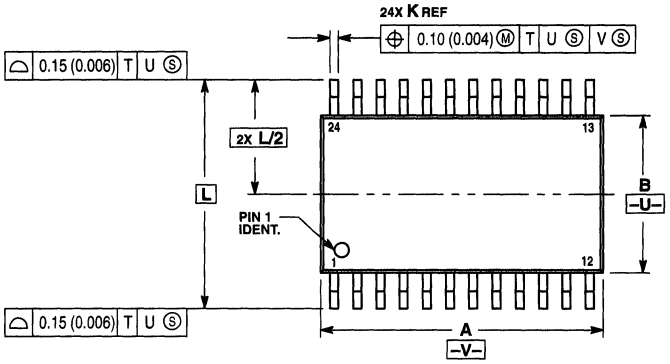


NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

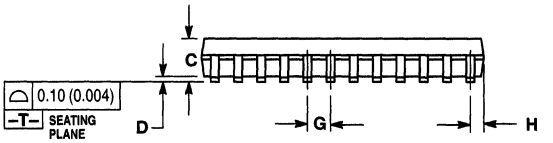
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

DTB SUFFIX
CASE 948H–01
Plastic Package
ISSUE O

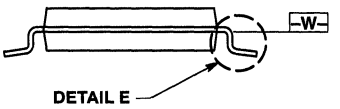


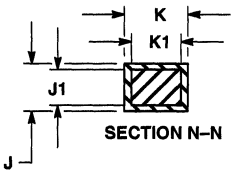


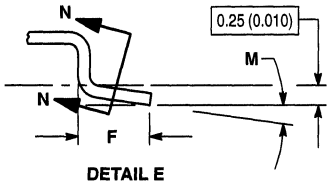
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

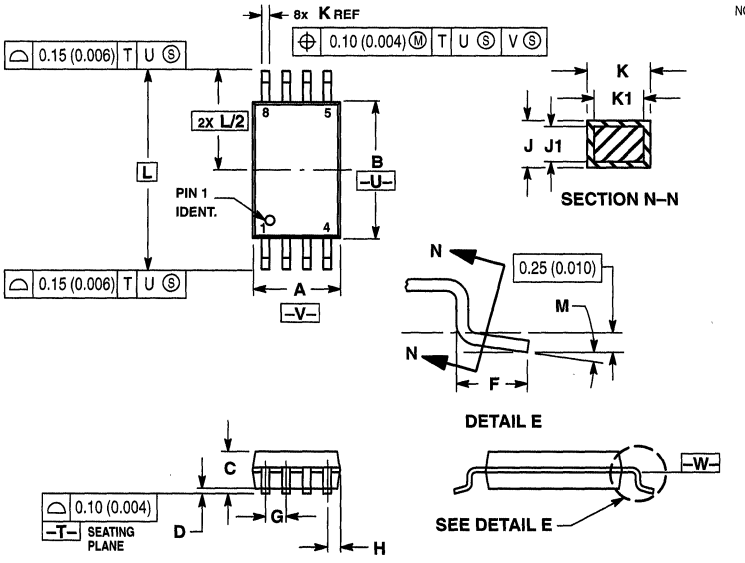






13

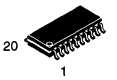
DTB SUFFIX
CASE 948J–01
Plastic Package
(TSSOP–8)
ISSUE O

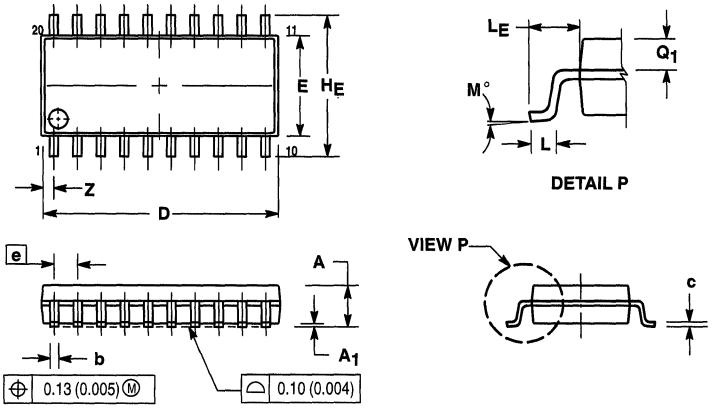


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

M SUFFIX
CASE 967–01
Plastic Package
(EIAJ–20)
ISSUE O



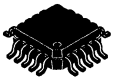


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

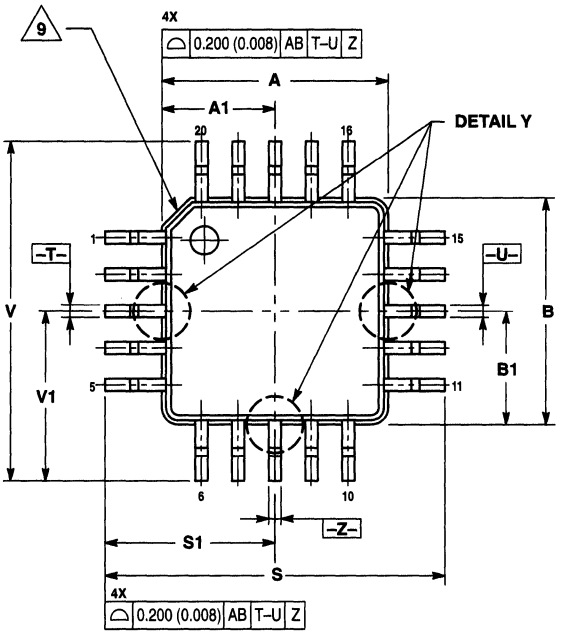
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q_1	0.70	0.90	0.028	0.035
Z	—	0.81	—	0.032

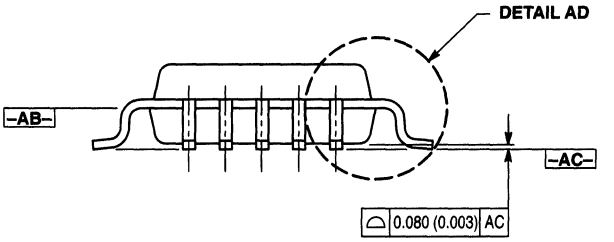
13

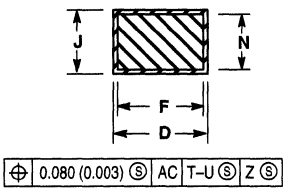
FTB SUFFIX
CASE 976–01
Plastic Package
(TQFP–20)
ISSUE O



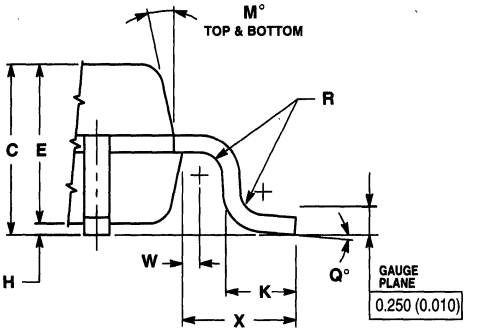
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT DATUM PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.



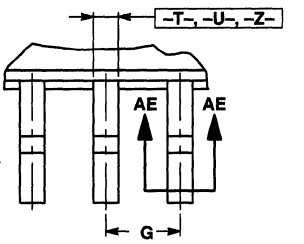




SECTION AE–AE



DETAIL AD

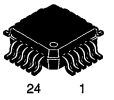


DETAIL Y

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.000 BSC		0.157 BSC	
A1	2.000 BSC		0.079 BSC	
B	4.000 BSC		0.157 BSC	
B1	2.000 BSC		0.079 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.650 BSC		0.026 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.250 BSC		0.010 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	6.000 BSC		0.236 BSC	
S1	3.000 BSC		0.118 BSC	
V	6.000 BSC		0.236 BSC	
V1	3.000 BSC		0.118 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

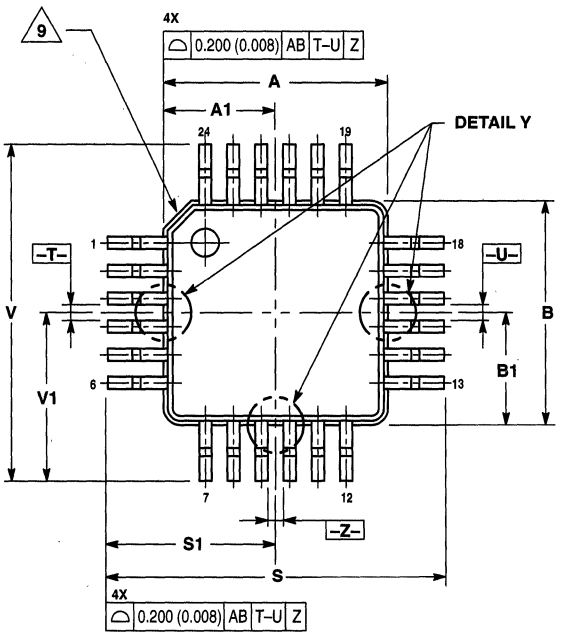
13

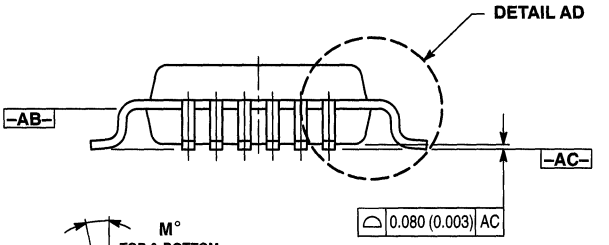
FTA SUFFIX
CASE 977–01
Plastic Package
ISSUE O

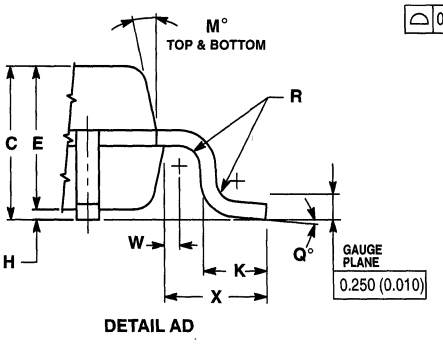


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT DATUM PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

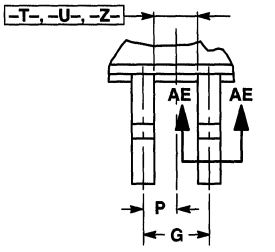
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.000 BSC		0.157 BSC	
A1	2.000 BSC		0.079 BSC	
B	4.000 BSC		0.157 BSC	
B1	2.000 BSC		0.079 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.250 BSC		0.010 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	6.000 BSC		0.236 BSC	
S1	3.000 BSC		0.118 BSC	
V	6.000 BSC		0.236 BSC	
V1	3.000 BSC		0.118 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	



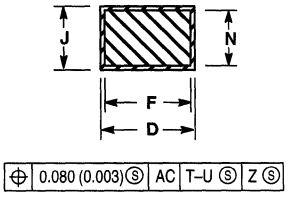




DETAIL AD



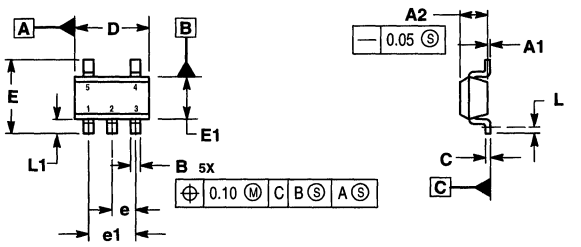
DETAIL Y



SECTION AE–AE

13

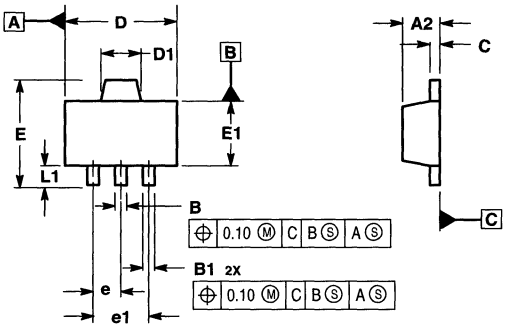
N SUFFIX
CASE 1212–01
Plastic Package
(SOT–23)
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM C IS A SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A1	0.00	0.10
A2	1.00	1.30
B	0.30	0.50
C	0.10	0.25
D	2.80	3.00
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
e1	1.90 BSC	
L	0.20	—
L1	0.45	0.75

H SUFFIX
CASE 1213–01
Plastic Package
(SOT–89)
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUM C IS A SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A2	1.40	1.60
B	0.37	0.57
B1	0.32	0.52
C	0.30	0.50
D	4.40	4.60
D1	1.50	1.70
E	—	4.25
E1	2.40	2.60
e	1.50 BSC	
e1	3.00 BSC	
L1	0.80	—

13

1PHX16946-15 Printed in USA 12/96 BANTA CO. MOTO#40 30,000 LITLINIF

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center,
3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

DL128/D