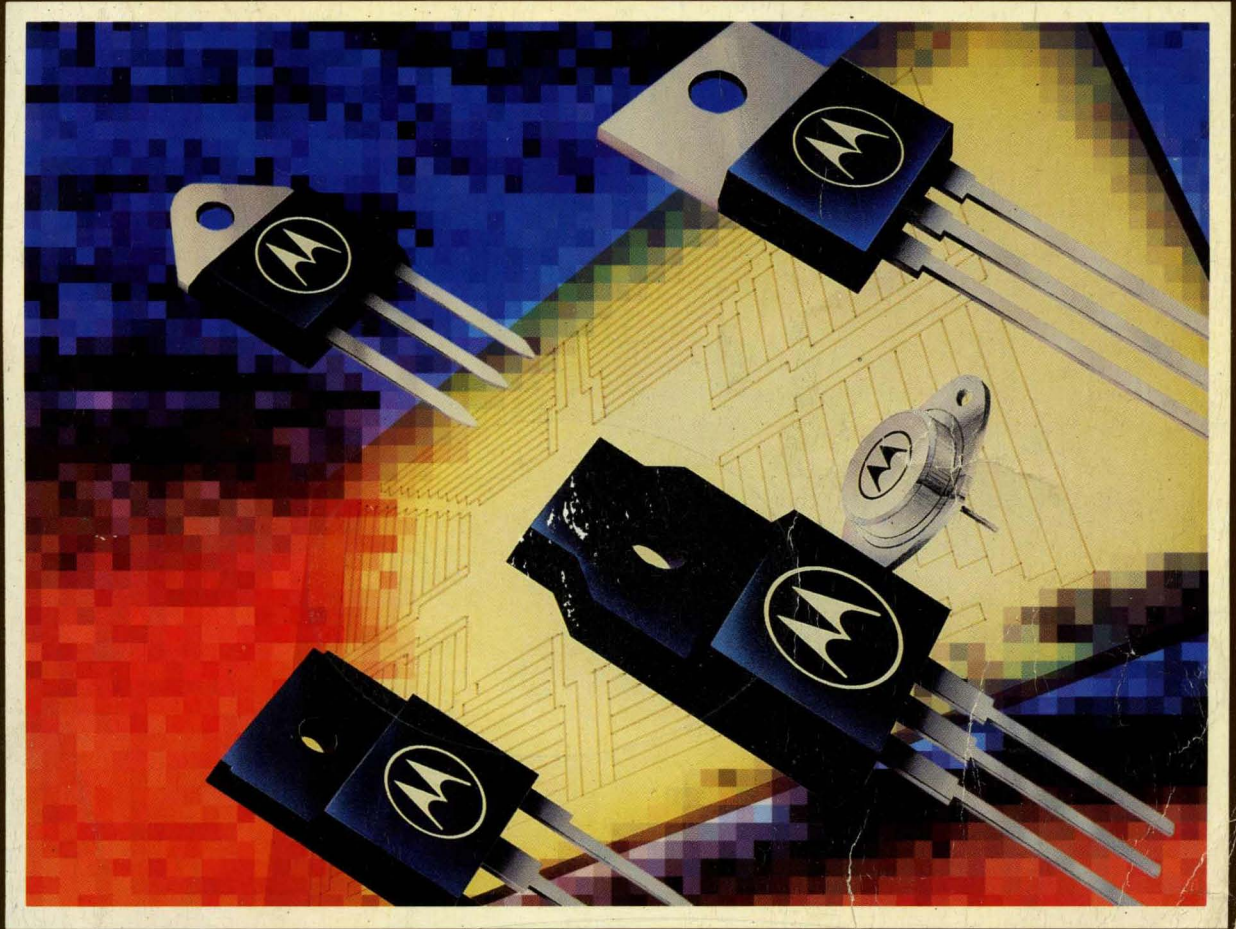




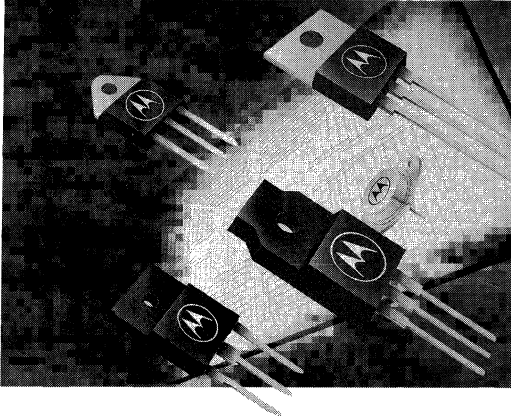
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MOTOROLA BIPOLAR POWER TRANSISTOR DATA



BIPOLAR POWER TRANSISTOR DATA

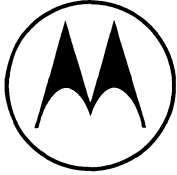


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POWER DEVICE DATA

Prepared by
Technical Information Center

This book presents technical data for Motorola's broad line of silicon power transistors. Complete specifications are provided in the form of data sheets and accompanying selection guides provide a quick comparison of characteristics to simplify the task of choosing the best device for a circuit.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

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MOTOROLA POWER TRANSISTORS IN BRIEF

Wide Range of Transistor Specifications

Bipolar transistors, NPNs and PNPs, single and multiple (Darlington) transistor structures, metal and plastic packages, Motorola's inventory of more than 1100 standard (off-the-shelf) power transistors covers the widest range of specifications for virtually every potential applications requirement.

Current Range — 0.5 to 100 Amperes

Voltage Range — 25 to 1800 Volts

Power Dissipation Range — 5 to 250 Watts.

Darlingtons

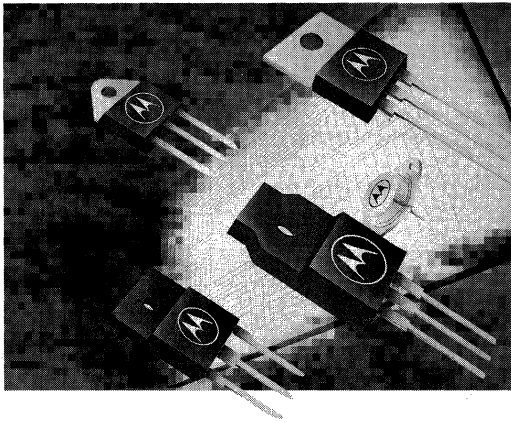
Consisting of two transistors, up to two resistors, and (up to) two diodes on a single chip, Darlington transistors achieve gain figures up to 20,000 in a single package. Rapid line expansion, and the resulting widespread implementation make Motorola Darlingtons highly cost-effective in a fast growing number of applications.

Chips, Chips, Chips!

Designing a hybrid? Motorola's wide range of power transistors is available. . . . UNENCAPSULATED through authorized chip distributors: Check with your Motorola Sales representative for the chip distributor in your area, preferred parts list, price and delivery.

Specials

Need a unique transistor with specifications not available off-the-shelf? Chances are Motorola can produce it quickly and inexpensively. Routine use of four major power processes and more than two decades of experience in the pioneering of new structures and geometries provide the insight and capability to meet any required specification within the limits of today's technology. Specials will require minimum order quantities and minimum yearly run rates. Check with your local Motorola representative for more information on special devices.



Alphanumeric Index and Cross Reference

1

The table on the subsequent pages contains an Alphanumeric index of Silicon power transistors currently manufactured and available to the industry.

The column headed "Similar" lists units with characteristics that might represent suitable replacements. In cases where such a replacement is contemplated, the Motorola device data sheet should be carefully compared with one for the device being replaced to determine any variations that could affect circuit performance.

ALPHANUMERIC INDEX — CROSS-REFERENCE

The following table represents an index and cross-reference guide for all low-frequency power transistors which are either manufactured directly by Motorola or for which Motorola manufactures a suitable equivalent. Where the Motorola part number differs from the Indus-

try part number, the Motorola device is a "form, fit and function" replacement for the industry type number — however, subtle differences in characteristics and/or specifications may exist.

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*Consult Motorola if a direct replacement is necessary.

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*Consult Motorola if a direct replacement is necessary.

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CM Consult Motorola if a direct replacement is necessary.

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*Consult Motorola if a direct replacement is necessary.

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SDT9207		2N5878	3-127
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SDT9209		MJ15001	3-844
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SE9401	SE9401		—
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CM Consult Motorola if a direct replacement is necessary.

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SVT350-3C		2N6308	3-194
SVT350-5		2N6308	3-194
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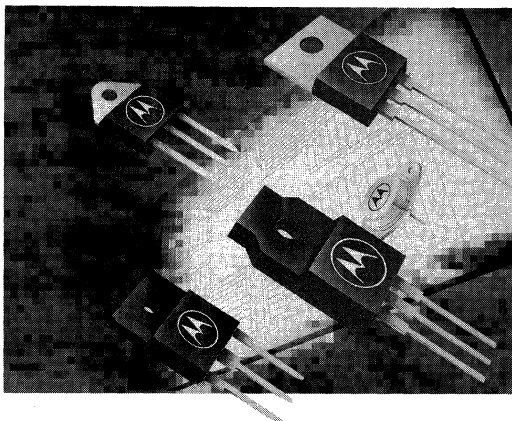
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*Consult Motorola if a direct replacement is necessary.

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TIPL752		MJ13080	3-810
TIPL752A		MJ13080	3-810
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TIPL753A		MJ13080	3-810
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Selector Guide

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The selector guides on the subsequent pages offer a quick "first-selection" capability for devices that fit specific applications categories.

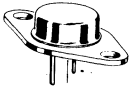
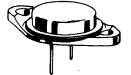









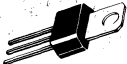
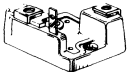
Because designers have different application prerequisites, the devices are categorized in three ways:

1. by package
2. by major product category
3. by major applications

In each case, pertinent electrical characteristics are supplied to permit rapid comparison of potentially suitable devices.

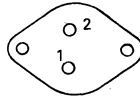
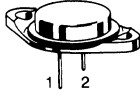
Selection By Package

Motorola power transistors are available in a wide variety of metal and plastic packages to match thermal, electrical and cost requirements. The following table compares the basic packages from the standpoint of current, voltage and power capabilities. The devices available in the various packages are tabulated on the succeeding pages.

Package	IC Range (Amps)	VCE Range (Volts)	PD (Watts)	Page #
 TO-204AA (TO-3) Case 1 Case 11	2.5-30	40-1500	36-250	2-3
 TO-204AE Case 197	2.5-70	40-1500	36-350	2-3
 TO-205AA Case 31 (TO-5)	3.0	40-800	6.0	2-8
 TO-205AD (TO-39) Case 79	0.5-5.0	40-400	5.0-10	2-8
 TO-213AA (TO-66) Case 80	1.0-10	40-325	20-90	2-9
 DPAK Case 369-03	0.5-10	40-400	12.5-20	2-18
 DPAK Case 369A-04	0.5-10	40-400	12.5-20	2-18
 TO-218AC Case 340	5.0-25	40-1500	80-150	2-10
 TO-220AB Case 221A	0.5-15	30-1800	15-125	2-12
 TO-225AA TYPE Case 77	0.3-5.0	25-400	12.5-40	2-15
 TO-225AB Case 90	5.0-15	40-100	65-100	2-17
 Case 152	0.5-2.0	30-300	10	2-17
 Case 353	25-100	250-850	250	2-18

Bipolar Power Transistors

TABLE 1 — METAL TO-204AA (Formerly TO-3) — TO-204AE (Type)



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

CASE 11-01, 11-3 — 40 mil pins
 CASE 1-04, 1-05 — 40 mil pins
 MODIFIED TO-3
 CASE 197-01 — 60 mil pins

I _C Cont Amps Max	V _{CEO(sus)} Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C			
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp					
2.5	800	MJ8501		7.5 min	0.5	4	2	1		125			
	1500*	BU205 MJ12002		2 min 1.11 min	2	2	0.75 typ 1	2 2	4 typ 4 typ	36 75			
3.5	325	2N3902		30/90	1	1.2 typ	0.1 typ	1	2.8	100			
4	1500*	MJ12003		2.5 min	3		1	3		100			
5	200	MJ410		30/90	1				2.5	100			
	250	MJ3029		30 min	0.4		1	3		125			
	300	MJ411		30/90	1				2.5	100			
	400	2N6543 MJ13070		7/35 8 min	3 3	4 1.5	0.8 0.5	3 3		6	100 125		
			450	MJ13071 MJ16002 MJ16004 2N6834		8 min	3	1.5	0.5	3		125	
		5 min			5	3	0.3	3		125			
		7 min			5	2.7	0.35	3		125			
		10/30			3	2.7	0.35	3	15	125			
	500	MJ16002A		5 min	5	3	0.3	3		125			
	700	MJ8502		7.5 min	1	4	2	2.5		150			
800	MJ8503		7.5 min	1	4	2	2.5		150				
850*	MJ12020		5 min	5		0.13 typ	3	15	125				
1500*	BU208 BU208A BU208D† MJ12004		2.25 min 2.25 min 2.25 min 2.5 min	4.5 4.5 4.5 4.5	8 typ	0.6 typ 0.4 typ 0.6 typ 1	4.5 4.5 4.5 4.5	4 typ 4 typ 4 typ 4	60 90 60 100				
		6	100	2N5758		2N6226	25/100	3	0.7 typ	0.5 typ	3	1	150
			120	2N5759		2N6227	20/80	3	0.7 typ	0.5 typ	3	1	150
			140	2N5760		2N6228	15/60	3	0.7 typ	0.5 typ	3	1	150

|h_{FE}| @ 1 MHz, ## Darlington

* V(BR)CEX or V(BR)CES

† D Suffix on this device signifies internal C-E Diode

(continued)

TABLE 1 — METAL TO-204AA — TO-204AE (Type) (continued)

I _C Cont Amps Max	V _{CEO(sus)} Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C		
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp				
6	375	BU326		30 typ	0.6	3.5	1**	2.5	6	90		
	400	BU326A		30 typ	0.6	3.5	1**	2.5	6	90		
7	300	MJ3041##		250 min	2.5					175		
	350	MJ3042##		250 min	2.5					175		
7.5	60	2N3447		40/120	5	2	0.35	5	10	115		
	80	2N3448		40/120	5	2	0.35	5	10	115		
8	60	MJ1000##	MJ900##	1k min	3					90		
		2N6055##	2N6053##	750/18k	4	1.5 typ	1.5 typ	4	4#	100		
	80	MJ1001##	MJ901##	1k min	3					90		
		2N6056##	2N6054##	750/18k	4	1.5 typ	1.5 typ	4	4#	100		
	250	2N6306		15/75	3	1.6	0.4	3	5	125		
	300	2N6307		15/75	3	1.6	0.4	3	5	125		
	350	2N6308		12/60	3	1.6	0.4	5	5	125		
	400	2N6545		MJ6503	7/35	5	4	1	5	6	125	
			15 min		2	2	0.5	4	125			
		MJ13080		8 min	5	1.5	0.5	5		150		
	450	MJ13081	MJ16006	MJ16008	2N6835	8 min	5	1.5	0.5	5		150
						5 min	8	2.5	0.25	5		150
						7 min	8	2.2	0.25	5		150
10/30						5	2.5	0.25	5	10	150	
500	MJ16006A		5 min	8	3	0.4	5		150			
850*	MJ12021		5 min	8		0.1 typ	5		150			
1400*	MJ10011##		20 min	4		1	4		80			
1500*	MJ12005		5 min	5		1	5		100			
9	400	BUS47		7 min	6	2	0.4	6		150		
	450	BUS47A		7 min	5	2	0.4	5		150		
10	40	2N6383##	2N6648##	1k/20k	5				20#	100		
		60	BD311	BD312	25 min	5				4	115	
			2N3789	15 min	3	0.3 typ	0.4 typ	5	4	150		
	2N3715		2N3791	30 min	3	0.3 typ	0.4 typ	5	4	150		
	2N5877		2N5875	20/100	4	1	0.8	4	4	150		
	2N6384##			1k/20k	5				20#	100		
	MJ3000##		MJ2500##	1k min	5					150		
	80	2N3714	2N3790	15 min	3	0.3 typ	0.4 typ	5	4	150		
		2N3716	2N3792	30 min	3	0.3 typ	0.4 typ	5	4	150		
		2N5878	2N5876	20/100	4	1	0.8	4	4	150		
		2N6385##		1k/20k	5				20#	100		
		MJ3001##	MJ2501##	1k min	5					150		
	140	2N5634		15/60	5	0.9 typ	0.9 typ	5	1	150		
2N3442			20/70	4					117			

* V_{(BR)CEX}, # |h_{FE}| @ 1 MHz, ## Darlington

(continued)

JAN, JTX, JTXV Available

TABLE 1 — METAL TO-204AA — TO-204AE (Type) (continued)

I _C Cont Amps Max	V _{CEO} (sus) Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp			
10	250	MJ15011	MJ15012	20/100	2					200	
	325	BUX43		8 min	5					8	120
		MJ413		20/80	0.5	2.2	0.9	5	2.5	125	
		MJ423		30/90	1				2.5	125	
		MJ431		15/35	2.5				2.5	125	
	350	BU323##		150 min	6	7.5 typ	5.2 typ	6		175	
		MJ13014		8/20	5	2	0.5	5		150	
		MJ10002##		3/300	5	2.5	1	5	10#	150	
		MJ10006##		30/300	5	1.5	0.5	5	10#	150	
	400	BU323A##		150 min	6	7.5 typ	5.2 typ	6		175	
MJ10007##			30/300	5	1.5	0.5	5	10#	150		
MJ10012##			100/2k	6	15	15	6		175		
MJ13015			8/20	5	2	0.5	5		150		
600	MJ10014##		10/250	10	2.5	0.8	10		175		
700	MJ8504		7.5 min	1.5	4	2	5		175		
800	MJ8505		7.5 min	1.5	4	2	5		175		
	MJ16018		4 min	5	4.5 typ	0.2 typ	5		150		
950*	MJ12010		4.2 min	5		1	5		100		
12	60	2N6057##	2N6050##	750/18k	6	1.6 typ	1.5 typ	6	4#	150	
	80	2N6058##	2N6051##	750/18k	6	1.6 typ	1.5 typ	6	4#	150	
	100	2N6059##	2N6052##	750/18k	6	1.6 typ	1.5 typ	6	4#	150	
	250	BUX42		8 min	6	2	0.4	6	8	120	
	1000	BUT16##		5 min	8	3.3	1.5	8		150	
15	60	2N3055	MJ2955	20/70	4	0.7 typ	0.3 typ	4	2.5	115	
		2N3055A	MJ2955A	20/70	4				0.8	115	
		2N6576##		2k/20k	4	2	7	10	10-200#	120	
		2N5881	2N5879	20/100	6	1	0.8	6	4	160	
	80	2N5882	2N5880	20/100	6	1	0.8	6	4	160	
	90	2N6577##		2k/20k	4	2	7	10	10-200#	120	
	120	MJ15015	MJ15016	20/70	4				1	180	
		2N6578##		2k/20k	4	2	7	10	10-200#	120	
	140	MJ15001	MJ15002	25/150	4				2	200	
	150	MJ11018##	MJ11017##	100 min	15				3#	175	
	200	BUX41		8 min	8	1.5	0.4	8	8	120	
		2N6249		10/50	10	3.5	1	10	2.5	175	
		MJ11020##	MJ11019##	100 min	15				3#	175	
	250	MJ11022##	MJ11021##	100 min	15				3#	175	
	275	2N6250		8/50	10	3.5	1	10	2.5	175	
	300	2N6546		6/30	10	4	0.7	10	6 to 24	175	
		2N6676		8 min	15	2.5	0.5	15	3	175	
	325	BUX13		8 min	8	2.5	0.8	8	8	150	
	400	BUS48		8 min	10	2	0.4	10		175	
BUX48					3	0.8	10		175		
2N6547			6/30	10	4	0.7	10	6 to 24	175		
2N6678			8 min	15	2.5	0.5	15	3	175		
MJ13090			8 min	10	2.5	0.5	10		175		
450	BUS48A		8 min	10	2	0.4	10		175		
	BUX48A				3	0.8	8		175		
	MJ13091		8 min	10	2.5	0.5	10		175		
	MJ16010		5 min	15	1.2 typ	0.2 typ	10		175		

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JAN, JTX, JTXV Available

* V(BR)CEX, # I_{hFE} @ 1 MHz, ## Darlington

(continued)

TABLE 1 — METAL TO-204AA — TO-204AE (Type) (continued)

Ic Cont Amps Max	VCEO(sus) Volts Min	Device Type		hFE Min/Max	@ Ic Amp	Resistive Switching			fT MHz Min	PD (Case) Watts @ 25°C
		NPN	PNP			ts μs Max	tf μs Max	@ Ic Amp		
		15				MJ16012 2N6836		7 min 10/30		
	500	MJ16010A		5 min	15	3	0.4	10		175
	850*	MJ12022		5 min	15		0.1 typ	10		175
16	60	MJ4033##	MJ4030##	1k/	10					150
	80	BD315 MJ4034##	BD316 MJ4031##	25 min 1k/	5 10				1	200 150
	100	BD317 2N5629 MJ4035##	BD318 2N6029 MJ4032##	25 min 25/100 1k/	5 8 10	1.2 typ	1.2 typ	8	1 1	200 200 150
	120	2N5630	2N6030	20/80	8	1.2 typ	1.2 typ	8	1	200
	140	2N3773 2N5631	2N6609 2N6031	15/60 15/60	8 8	1.1 typ 1.2 typ	1.5 typ 1.2 typ	8 8	4 1	150 200
	200	MJ15022	MJ15023	15/60	8				5	250
	250	MJ15024	MJ15025	15/60	8				5	250
18	160	BUX41N		8 min	12	1.2	0.25	12	8	120
20	60	2N3772 2N6282##	2N6285##	15/60 750/18k	10 10	2.5 typ	2.5 typ	10	2 4#	150 160
	75	2N5039		20/100	10	1.5	0.5	10	60	140
	80	2N5303 2N6283##	2N5745 2N6286##	15/60 750/18k	10 10	2 2.5 typ	1 2.5 typ	10 10	2 4#	200 160
	90	2N5038		20/100	12	1.5	0.5	12	60	140
	100	2N6284##	2N6287##	750/18k	10	2.5 typ	2.5 typ	10	4#	160
	125	BUX40		8 min	15	1	0.25	15	8	120
	140	MJ15003	MJ15004	25/150	5				2	250
	160	BUV11N		10 min	15	1.2	0.25	15	8	150
	200	BUV11 MJ13330		10 min 8/40	12 10	1.8 3.5	0.4 0.7	12 10	8 5 to 40	150 175
	250	BUV12 MJ13331		10 min 8/40	10 10	1.5 3.5	0.5 0.7	10 10	8 5 to 40	150 175
	350	MJ10000## MJ10004##		40/400 40/400	10 10	3 1.5	1.8 0.5	10 10	10# 10#	175 175
	400	BUV24 MJ10001## MJ10005## MJ13333		8 min 40/400 40/400 10/60	12 10 10 5	3 1.5 4	0.9 1.8 0.5 0.7	12 10 10 10	8 10# 10#	250 175 175 175
	450	MJ10008## MJ16014 MJ16016 2N6837		30/300 5 min 7 min 10/30	10 20 20 15	2 2.7 2.2 2.5	0.6 0.35 0.25 0.25	10 20 20 15	8#	175 250 250 250
	500	MJ10009## MJ13335		30/300 10/60	10 5	2 4	0.6 0.7	10 10	8#	175 175
	700	BUT15##		15 min	12	2.5	0.8	12		175
	750	MJ10024##		50/600	20	5	1.8	10		250
	850	MJ10025##		50/600	20	5	1.8	10		250

* V(BR)CEX, # |hfe| @ 1 MHz, ## Darlington



JAN, JTX, JTXV Available

TABLE 1 — METAL TO-204AA — TO-204AE (Type) (continued)

I _C Cont Amps Max	V _{CEO} (sus) Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp			
24	1000	BUT36##		5 min	16	6	2.5	16		250	
25	60	2N5885	2N5883	20/100	10	1	0.8	10	4	200	
	80	2N5886	2N5884 2N6436	20/100 30/120	10 10	1 1	0.8 0.25	10 10	4 40	200 200	
	100	2N6336	2N6437	30/120	10	1	0.25	10	40	200	
	120	2N6339	2N6438	30/120	10	1	0.25	10	40	200	
	125	BUV10 BUV10N		10 min 10 min	20 20	1.2 1.55	0.25 0.45	20 15	8 10	150 175	
	140	2N6340		30/120	10	1	0.25	10	40	200	
	150	2N6341		30/120	10	1	0.25	10	40	200	
	500	BUT14##		15 min	16	2.8	0.8	16		175	
28	400	BUT13##		20 min	20	2.6	0.8	18		175	
30	40	2N3771 2N5301	2N4398	15/60 15/60	15 15	2	1	10	2 2	150 200	
	60	2N5302 MJ11012##	2N4399 MJ11011##	15/60 1k min	15 20	2	1	10	2 4#	200 200	
	90	BUX39 MJ11014##	MJ11013##	8 min 1k min	20 20	1	0.25	20	8 4#	120 200	
	100	2N6328 MJ802	MJ4502	6/30 25/100	30 7.5				3 2	200 200	
	120	MJ11016##	MJ11015##	1k min	20				4#	200	
	325	BUV23•		8 min	16	1.8	0.4	16	8	250	
	400	BUS98• BUX98		8 min	20	2.3 3	0.4 0.8	20 20		250 250	
	450	BUS98A• BUX98A MJ16020• MJ16022•		8 min 5 min 7 min	16 30 30	2.3 3 1.8 1.5	0.4 0.8 0.2 0.15	16 16 20 20		250 250 250 250	
	40	160	BUV21N•		10 min	40	1	0.2	40	8	250
		200	BUV21•		10 min	25	1.8	0.4	25	8	150
250		BUS52• BUV22•		15 min 10 min	40 20	1.1	0.35	20	8	350 250	
350		MJ10022•##		50/600	120	2.5	0.9	20		250	
400		MJ10023•##		50/600	10	2.5	0.9	20		250	
700		BUT35•##		15 min	24	4	1.2	24		250	
50		60	2N5685• MJ11028•##	2N5683• MJ11029•##	15/60 400 min	25 50	0.5 typ	0.3 typ	25	2	300 300
	80	2N5686•	2N5684• 2N6377•	15/60 30/120	25 20	0.5 typ 0.8	0.3 typ 0.25	25 20	2 30	300 250	
	90	MJ11030•##	MJ11031•##	400 min	50					300	
	100	2N6274•	2N6378•	30/120	20	0.8	0.25	20	30	250	
	120	2N6275• MJ11032•##	2N6379• MJ11033•##	30/120 400 min	20 50	0.8	0.25	20	30	250 300	
	125	BUV20•		10 min	50	1.2	0.25	50	8	250	
	150	2N6277•		30/120	20	0.8	0.25	20	30	250	

• Modified TO-3, 60 mil pins, # |h_{FE}| @ 1 MHz, ## Darlington



JAN, JTX, JTXV Available

TABLE 1 — METAL TO-204AA — TO-204AE (Type) (continued)

IcCont Amps Max	VCEO(sus) Volts Min	Device Type		hFE Min/Max	@ Ic Amp	Resistive Switching			fT MHz Min	PD (Case) Watts @ 25°C
		NPN	PNP			ts μs Max	tf μs Max	@ Ic Amp		
		50	200			BUS51*		15 min		
	400	MJ10015***		10 min	40	2.5	1	20	250	
	500	BUT34*** MJ10016***		15 min 10 min	32 40	3 2.5	1.5 1	32 20	250 250	
56	400	BUT33***		20 min	36	3.3	1.6	36	250	
60	60	MJ14000*	MJ14001*	15/100	50				300	
	80	MJ14002*	MJ14003*	15/100	50				300	
	200	MJ10020***		75 min	15	3.5	0.5	30	250	
	250	MJ10021***		75 min	15	3.5	0.5	30	250	
70	125	BUS50*		15 min	50				350	

* Modified TO-3, 60 mil pins, # hfe @ 1 MHz, ** Darlington

TABLE 2 — METAL TO-205AA PACKAGE (Formerly TO-5)

CASE 31-03



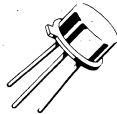
STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

IcCont Amps Max	VCEO(sus) Volts Min	Device Type		hFE Min/Max	@ Ic Amp	Resistive Switching			fT MHz Min	PD (Case) Watts @ 25°C
		NPN	PNP			ts μs Max	tf μs Max	@ Ic Amp		
		3	40				2N3719 2N3867	25/180 40/200		
60	2N3720 2N3868			25/180 30/150	1 1.5	0.4* 0.4*		1 1.5	60 60	6 6
	80		2N6303	30/150	1.5	0.4*		1.5	60	6

*toff

TABLE 3 — METAL TO-205AD PACKAGE (Formerly TO-39)

CASE 79-02



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(Pin 3 connected to case)

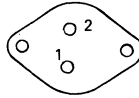
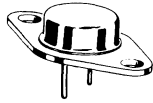
IcCont Amps Max	VCEO(sus) Volts Min	Device Type		hFE Min/Max	@ Ic Amp	Resistive Switching			fT MHz Min	PD (Case) Watts @ 25°C
		NPN	PNP			ts μs Max	tf μs Max	@ Ic Amp		
		0.5	300				MJ4646	20 min		
400			MJ4647	20 min	0.5	0.72*		0.05	30	5
4	60	2N4877		20/100	4	1.5	0.5	4	4	10
5	80	2N5336	2N6190	30/120	2	2	0.2	2	30	6
		2N5337	2N6191	60/240	2	2	0.2	2	30	6
100	100	2N5338		30/120	2	2	0.2	2	30	10
		2N5339	2N6193	60/240	2	2	0.2	2	30	6

JAN, JTX, JTXV Available

*toff

TABLE 4 — METAL TO-213AA PACKAGE (Formerly TO-66)

CASE 80-02



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

I _C Cont Amps Max	V _{CEO} (sus) Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp			
1	40		2N4898	20/100	0.5	0.6 typ	0.3 typ	0.5	3	25	
	60		2N4899	20/100	0.5	0.6 typ	0.3 typ	0.5	3	25	
	80	2N4912	2N4900	20/100	0.5	0.6 typ	0.3 typ	0.5	3	25	
	175	2N3583	2N6420	40/200	0.5	2 typ	0.23 typ	0.5	10	35	
	225	2N3738		40/200	0.1	3 typ	0.3 typ	0.1	10	20	
	250		2N5344	25/100	0.5	0.6	0.1	0.5	60	40	
	300	2N3739		40/200	0.1	3 typ	0.3 typ	0.1	10	20	
2	225		2N6211	10/100	1	2.5	0.6	1	20	35	
	250	2N3584	2N6421	25/100	1	4	3	1	10	35	
	300		2N6212	10/100	1	2.5	0.6	1	20	35	
			2N3585	2N6422	25/100	1	4	3	1	10	35
			2N4240		30/150	0.75	6	3	0.75	15	35
350		2N6213	10/100	1	2.5	0.6	1	20	35		
3	140	2N3441		25/100	0.5				0.2	25	
4	60		2N3740	30/100	0.25	1.3 typ	0.27 typ	0.25	4	25	
		2N3054,A	2N6049	25/100	0.5	1 typ	0.3 typ	0.5	3	75	
		2N3766		40/160	0.5	0.9 typ	0.09 typ	0.5	10	20	
		2N6294##	2N6296##	750/18k	2	0.9 typ	0.7 typ	2	4#	50	
	80		2N3741	30/100	0.25	1.3 typ	0.27 typ	0.25	4	25	
		2N3767	2N6295##	2N6297##	40/160	0.5	0.9 typ	0.09 typ	0.5	10	20
	750/18k			2	0.9 typ	0.7 typ	2	4	50		
5	80	2N4233A		25/100	1.5	0.5 typ	0.2 typ	1.5	4	75	
	275	2N6233		25/125	1	3.5	0.5	1	20	50	
	325	2N6235		25/125	1	3.5	0.5	1	20	50	
7	60	2N6315	2N6317	20/100	2.5	1	0.8	2.5	4	90	
	80	2N5428		60/240	2	2	0.2	2	30	40	
		2N6316	2N6318	20/100	2.5	1	0.8	2.5	4	90	
	100	2N5429		30/120	2	2	0.2	2	30	40	
		2N5430		60/240	2	2	0.2	2	30	40	
8	60	2N6300##	2N6298##	750/18k	4	1.5 typ	1.5 typ	4	4#	75	
	80	2N6301##	2N6299##	750/18k	4	1.5 typ	1.5 typ	4	4#	75	
10	80	2N6495		10/60	10	0.15 typ	0.05 typ	10	25	70	

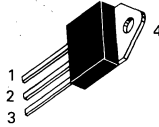
|h_{FE}| @ 1 MHz, ## Darlington

JAN, JTX, JTXV Available

2

TABLE 5 — PLASTIC TO-218AC PACKAGE

STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR



CASE 340-01

I _C Cont Amps Max	V _{CEO} (sus) Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp			
3	750	MJH16032		4 min	3	2	1.5	2		125	
	850	MJH16034		4 min	3	2	1.5	2		125	
5	400	BUW11		6 min	3	4	0.8	3		125	
	450	BUW11A MJH16002 MJH16004		6 min	2.5	4	0.8	2.5		125	
				5 min	5	3	0.3	3		100	
				7 min	5	2.7	0.35	3		100	
	500	MJH16002A		5 min	5	3	0.3	3		100	
1500*	MJH12004		2.5 min	4.5	—	1	4.5	4		100	
6	375	BU426		30 typ	0.6	2 typ	0.5 typ	2.5	6 typ	113	
	400	BU426A		30 typ	0.6	2 typ	0.5 typ	2.5	6 typ	113	
8	400	BUW12		6 min	6	4	0.8	5		125	
	450	BUW12A MJH16006 MJH16008		6 min	5	4	0.8	5		125	
				5 min	8	2.5	0.25	5		125	
				7 min	8	2.2	0.25	5		125	
	500	BUT50P## MJH16006A		30 min	2	0.75 typ	0.1 typ	5		100	
				5 min	8	2.5	0.25	5		125	
700	BU508,A BU508D,AD		2.25 min	4.5	8 typ	0.5 typ	4.5	7	125		
			2.25 min	4.5	8 typ	0.5 typ	4.5	7	125		
750	MJH12005					0.4 typ	5	4	100		
9	400	BUS47P		7 min	5	2	0.4	6		128	
	450	BUS47AP		7 min	6	2	0.4	6		128	
10	40	TIP33	TIP34	20 min	3				3	80	
	60	BDV65## TIP33A TIP140##	BDV64## TIP34A TIP145##	1k min	5					3	125
				20 min	3				4#	80	
				500 min	10	2.5 typ	2.5 typ	5	4#	125	
	80	BDV65A## TIP33B TIP141##	BDV64A## TIP34B TIP146##	1k min	5					3	125
				20 min	3				4#	80	
				500 min	10	2.5 typ	2.5 typ	5	4#	125	
	100	BDV65B## TIP33C TIP142##	BDV64B## TIP34C TIP147##	1k min	5					3	125
				20 min	3				4#	80	
				500 min	10	2.5 typ	2.5 typ	5	4#	125	
120	BDV65C##	BDV64C##	1k min	5					125		
200	BU323P##		150 min	6	15	15	6		125		
250	BU323AP##		150 min	6	15	15	6		125		
400	MJH10012##		100/2k	6	15	15	6		118		
800	MJH16018		4 min	5	4.5 typ	0.2 typ	5		150		
15	60	TIP3055	TIP2955	5 min	10				2.5	80	
	150	MJH11018	MJH11017	400/15k	10				3#	150	

[h_{FE}] @ 1 MHz, ## Darlington
 * V(BR)CEX or V(BR)CES

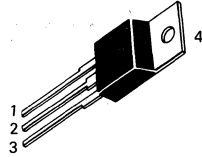
(continued)

TABLE 5 — PLASTIC TO-218AC PACKAGE (continued)

I _C Cont Amps Max	V _{CEO(sus)} Volts Min	Device Type		hFE Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp			
15	200	MJH11020	MJH11019	400/15k	10				3#	150	
	250	MJH11022	MJH11021	400/15k	10				3#	150	
	300	MJH6676		8 min	15	2.5	0.5	15		125	
	350	MJH6677		8 min	15	2.5	0.5	15		125	
	400	BUS48P BUW13 MJH6678 MJH13090			8 min	10	2	0.4	10		150
						15	4	0.8	10		175
					8 min	15	2.5	0.5	15		125
					8 min	10	2.5	0.5	10		125
	450	BUS48AP BUW13A MJH13091 MJH16010 MJH16012			8 min	8	2	0.4	10		150
						10	4	0.8	8		175
8 min					10	2.5	0.5	10		125	
5 min					15	1.2	0.2	10		150	
7 min					15	0.9	0.15	10		150	
500	BUT51P## MJH16010A			40 min	5	1.1	0.16	10		125	
				5 min	15	3	0.4	10		150	
16	100	MJE4340	MJE4350	15 min	8	1.2 typ	1.2 typ	8	1	125	
	120	MJE4341	MJE4351	15 min	8	1.2 typ	1.2 typ	8	1	125	
	140	MJE4342	MJE4352	15 min	8	1.2 typ	1.2 typ	8	1	125	
	160	MJE4343	MJE4353	15 min	8	1.2 typ	1.2 typ	8	1	125	
20	60	MJH6282##	MJH6285##	750/18k	10				4#	125	
	80	MJH6283##	MJH6286##	750/18k	10				4#	125	
	100	MJH6284##	MJH6287##	750/18k	10				4#	125	
25	40	TIP35	TIP36	10/75	15	0.6 typ	0.3 typ	10	3	125	
	45	BD249	BD250	10 min	15				3	125	
	60	BD249A TIP35A	BD250A TIP36A	10 min	15				3	125	
				10/75	15	0.6 typ	0.3 typ	10	3	125	
	80	BD249B TIP35B	BD250B TIP36B	10 min	15				3	125	
				10/75	15	0.6 typ	0.3 typ	10	3	125	
100	BD249C TIP35C	BD250C TIP36C	10 min 10/75	15 15	0.6 typ	0.3 typ	10	3 3	125 125		

|h_{fe}| @ 1 MHz, ## Darlington

TABLE 6 — PLASTIC TO-220AB PACKAGE



STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 221A-02

I _C Cont Amps Max	V _{CE0(sus)} Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp		
		0.5	350			MJE2360T MJE2361T		15 min 40 min		
1	40	TIP29	TIP30	15/75	1	0.6 typ	0.3 typ	1	3	30
	60	TIP29A	TIP30A	15/75	1	0.6 typ	0.3 typ	1	3	30
	80	TIP29B	TIP30B	15/75	1	0.6 typ	0.3 typ	1	3	30
	100	TIP29C	TIP30C	15/75	1	0.6 typ	0.3 typ	1	3	30
	250	TIP47		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	300	TIP48		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	350	TIP49		30/150	0.3	2 typ	0.18 typ	0.3	10	40
2	400	TIP50		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	45	BD239	BD240	15 min	1				3	30
	60	BD239A TIP110##	BD240A TIP115##	15 min 500 min	1 2	1.7 typ	1.3 typ	2	3 25#	30 50
	80	BD239B TIP111##	BD240B TIP116##	15 min 500 min	1 2	1.7 typ	1.3 typ	2	3 25#	30 50
	100	BD239C TIP112##	BD240C TIP117##	15 min 500 min	1 2	1.7 typ	1.3 typ	2	3 25#	30 50
	400	BUX84		30 min	0.1	3.5	1.4	1	4	50
	450	BUX85		30 min	0.1	3.5	1.4	1	4	50
2.5	900	MJE1320		3 min	1	4 typ	0.8 typ	1		80
	700	MJE8500		7.5 min	0.5	4	2	1		65
	750	MJE12007		1.1 min	2		1	2	4 typ	65
3	800	MJE8501		7.5 min	0.5	4	2	1		65
	40	TIP31	TIP32	25 min	1	0.6 typ	0.3 typ	1	3	40
	45	BD241	BD242	25 min	1				3	40
	60	BD241A TIP31A	BD242A TIP32A	25 min 25 min	1 1	0.6 typ	0.3 typ	1	3 3	40 40
	80	BD241B TIP31B	BD242B TIP32B	25 min 25 min	1 1	0.6 typ	0.3 typ	1	3 3	40 40
	100	BD241C TIP31C	BD242C TIP32C	25 min 25 min	1 1	0.6 typ	0.3 typ	1	3 3	40 40
	750	MJE16032		4 min	3	2	1.5	2		80
4	850	MJE16034		4 min	3	2	1.5	2		80
	45	2N6121 BD533	2N6124 BD534	25/100 25 min	1.5 2	0.4 typ	0.3 typ	1.5	2.5 3	40 50
	60	2N6122 BD535 MJE800T##	2N6125 BD536 MJE700T##	25/100 25 min 750 min	1.5 2 1.5	0.4 typ	0.3 typ	1.5	2.5 3 1#	40 50 40
	80	2N6123 BD537	BD538	20/80 15 min	1.5 2	0.4 typ	0.3 typ	1.5	2.5 3	40 50
	300	MJE13004		6/30	3	3	0.7	3	4	60
	400	MJE13005		6/30	3	3	0.7	3	4	60
5	60	TIP120##	TIP125##	1k min	3	1.5 typ	1.5 typ	3	4#	65
	80	TIP121##	TIP126##	1k min	3	1.5 typ	1.5 typ	3	4#	65
	100	TIP122##	TIP127##	1k min	3	1.5 typ	1.5 typ	4	4#	75

|h_{FE}| @ 1 MHz, ## Darlington

(continued)

TABLE 6 — PLASTIC TO-220AB PACKAGE (continued)

I _C Cont Amps Max	V _{CE0} (sus) Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp			
5	250	2N6497		10/75	2.5	1.8	0.8	2.5	5	80	
	300	2N6498		10/75	2.5	1.8	0.8	2.5	5	80	
	400	MJE13070		8 min	3	1.5	0.5	3		80	
	450		BUS46P		7 min	3	1.5	0.5	2		75
			MJE13071		8 min	3	1.5	0.5	3		80
			MJE16002		5 min	5	3	0.3	3		80
			MJE16004		7 min	5	2.7	0.35	3		80
700	MJE8502		7.5 min	1	4	2	2.5		80		
800	MJE8503		7.5 min	1	4	2	2.5		80		
6	40	TIP41	TIP42	15/75	3	0.4 typ	0.15 typ	3	3	65	
	45	BD243	BD244	15 min	3				3	65	
	60	BD243A TIP41A	BD244A	15 min	3				3	65	
			TIP42A	15/75	3	0.4 typ	0.15 typ	3	3	65	
	80	BD243B TIP41B	BD244B	15 min	3				3	65	
			TIP42B	15/75	3	0.4 typ	0.15 typ	3	3	65	
100	BD243C TIP41C	BD244C TIP42C	15 min 15/75	3 3	0.4 typ	0.15 typ	3	3 3	65 65		
7	30	2N6288	2N6111	30/150	3	0.4 typ	0.15 typ	3	4	40	
	45	BD795	BD796	25 min	3				3	65	
	50	2N6290	2N6109	30/150	2.5	0.4 typ	0.15 typ	3	4	40	
	60	BD797	BD798	25 min	3				3	65	
	70	2N6292	2N6107	30/150	3	0.4 typ	0.15 typ	3	4	40	
	80	BD799	BD800	15 min	3				3	65	
	100	BD801	BD802	15 min	3				3	65	
	150	BU407,D		30 min	1.5		0.75	5	10	60	
	200	BU406,D		30 min	1.5		0.75	5	10	60	
	375	BU522##		250 min	2.5				7.5	75	
	425	BU522A##		250 min	2.5				7.5	75	
	450	BU522B##		250 min	2.5				7.5	75	
8	40	2N6386##		1k/20k	3				20#	65	
	45	BDX53##	BDX54##	750 min	3				4#	60	
		BD895##	BD896##	750 min	3				1#	70	
		BD895A##	BD896A##	750 min	4				1#	70	
	60	2N6043##	2N6040##	1k/10k	4	1.5 typ	1.5 typ	3	4#	75	
		BDX53A##	BDX54A##	750 min	3				4#	60	
		BD897##	BD898##	750 min	3				1#	70	
		BD897A##	BD898A##	750 min	4				1#	70	
		TIP100##	TIP105##	1k/20k	3	1.5 typ	1.5 typ	3	4#	80	
	80	2N6044##	2N6041##	1k/10k	4	1.5 typ	1.5 typ	3	4#	75	
		BDX53B##	BDX54B##	750 min	3				4#	60	
		BD899##	BD900##	750 min	3				1#	70	
		BD899A##	BD900A##	750 min	4				1#	70	
		TIP101##	TIP106##	1k/20k	3	1.5 typ	1.5 typ	3	4#	80	
	100	2N6045##	2N6042##	1k/10k	3	1.5 typ	1.5 typ	3	4#	75	
		BDX53C##	BDX54C##	750 min	3				4#	60	
BD901##		BD902##	750 min	3				1#	70		
TIP102##		TIP107##	1k/20k	3	1.5 typ	1.5 typ	3	4#	80		

|h_{FE}| @ 1 MHz, ## Darlington

(continued)



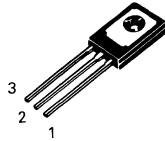
TABLE 6 — PLASTIC TO-220AB PACKAGE (continued)

I _C Cont Amps Max	V _{CEO(sus)} Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp		
8	120	BDX53D##	BDX54D##	750 min	3				4#	60
		MJE15028	MJE15029	20 min	4				30	50
	150	MJE15030	MJE15031	20 min	4				30	50
		BU807##		100 min	5	0.55 typ	0.2 typ	5		60
	200	BU806##		100 min	5	0.55 typ	0.2 typ	5		60
		300	MJE13006	MJE5850	5/30	5	3	0.7	5	4
	MJE5740##		200 min		4	8 typ	2 typ	6		80
			15 min		2	2	0.5	4		80
350	MJE5741##	MJE5851	200 min	4	8 typ	2 typ	6		80	
			15 min	2	2	0.5	4		80	
400	MJE5742## MJE13007 MJE16080	MJE5852	200 min	4	8 typ	2 typ	6	4	80	
			5/30	5	3	0.7	5		80	
			15 min	2	2	0.5	4		80	
			5 min	8	2	0.5	5		80	
450	MJE16080		5 min	8	2	0.5	5		80	
10	30		D45H1	20 min	4					50
			D45H2	40 min	4					50
	40	D44E1##		1000 min	5	2 typ	0.5 typ	10		50
		45	BDX33##	BDX34##	750 min	4				3
	BD805		BD806	15 min	4				1.5	90
	D44H4		D45H4	20 min	4					50
	D44H5		D45H5	40 min	4					50
	60	BDX33A##	BDX34A##	750 min	4				3	70
		BD807	BD808	15 min	4				1.5	90
		D44H7	D45H7	20 min	4					50
D44H8		D45H8	40 min	4					50	
		D45H9	40 min	4					50	
MJE2801T			25/100	3					75	
MJE3055T		MJE2955T	20/70	4					75	
2N6387##	2N6667##	1k/20k	5				20#	65		
SE9300	SE9400	1k min	4				1#	70		
80	BDX33B##	BDX34B##	750 min	3				3	70	
	BD809	BD810	15 min	4				1.5	90	
	D44E3##		1000 min	5	2 typ	0.5 typ	10		50	
		D45H12	40 min	4					50	
	2N6388##	2N6668##	1k/20k	5				20#	65	
	D44H10	D45H10	20 min	4	0.5 typ	0.14 typ	5	50 typ	50	
	D44H11	D45H11	40 min	4	0.5 typ	0.14 typ	5	50 typ	50	
SE9301	SE9401	1k min	4				1#	70		
100	BDX33C##	BDX34C##	750 min	3				3	70	
	SE9302	SE9402	1k min	4				1#	70	
12	300	MJE13008		6/30	8	3	0.7	8	4	100
	400	MJE13009		6/30	8	3	0.7	8	4	100
15	30	D44VH1	D45VH1	20 min	4	0.7	0.09	8	50 typ	83
	40	2N6486	2N6489	20/150	5	0.6 typ	0.3 typ	5	5	75
	45	D44VH4	D45VH4	20 min	4	0.5	0.09	8	50 typ	83
	60	2N6487	2N6490	20/150	5	0.6 typ	0.3 typ	5	5	75
		D44VH7		20 min	4	0.5	0.09	8	50 typ	83
	80	2N6488	2N6491	20/150	5	0.6 typ	0.3 typ	5	5	75
	D44VH10	D45VH10	20 min	4	0.5	0.09	8	50 typ	83	

[h_{FE}] @ 1 MHz, ## Darlington

TABLE 7 — PLASTIC TO-225AA PACKAGE (Formerly TO-126)

STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. BASE



STYLE 3:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER

CASE 77-04
 PLASTIC

IcCont Amps Max	VCE(sus) Volts Min	Device Type		hFE Min/Max	@ IC Amp	Resistive Switching			fT MHz Min	PD (Case) Watts @ 25°C	
		NPN	PNP			ts µs Max	tf µs Max	@ IC Amp			
		0.3	250			MJE3440		40/160			0.02
	350	MJE3439		40/160	0.02				15	15	
0.5	150	MJE341		25/200	0.05				15	20.8	
	200	MJE344		30/300	0.05				15	20.8	
	250	2N5655 BD157		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20	20
				30/240	0.05						
	300	BD158 BD232 MJE340 2N5656	MJE350	30/240	0.05	3.5 typ	0.24 typ	0.1	10	20	20
				20 min	0.15						
30/240	0.05										
30/250	0.1				3.5 typ	0.24 typ	0.1	10	20	20	
1	40	2N4921	2N4918	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30	
	60	2N4922	2N4919	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30	
	80	2N4923	2N4920	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30	
1.5	40	MJE720		8 min	1					20	
	45	BD165 BD135 BD135.6 BD135.10 BD135.16	BD166 BD136 BD136.6 BD136.10 BD136.16	15 min	0.5					6	20
				40/250	0.15					12.5	
				40/100	0.15				12.5		
				63/160	0.15				12.5		
				100/250	0.15				12.5		
	60	BD167 BD137 BD137.6 BD137.10 BD137.16	BD168 BD138 BD138.6 BD138.10 BD138.16	15 min	0.5					6	20
				40/250	0.15				12.5		
				40/100	0.15			12.5			
				63/160	0.15			12.5			
100/250				0.15			12.5				
80	BD169 BD139 BD139.6 BD139.10 BD139.16	BD170 BD140 BD140.6 BD140.10 BD140.16	15 min	0.5					6	20	
			40/250	0.15				12.5			
			40/100	0.15			12.5				
			63/160	0.15			12.5				
			100/250	0.15			12.5				
300	MJE13002*		5/25	1	4	0.7	1	5	40		
400	MJE13003*		5/25	1	4	0.7	1	5	40		
2	45	BD233	BD234	25 min	1				3	25	
	60	BD235	BD236	25 min	1				3	25	
	80	BD237	BD238	25 min	1				3	25	
	100	MJE270	MJE271	1.5k min	0.12				6	15	
3	30	MJE520	MJE370	25 min	1					25	

* Case 77 (Style 3), # |hFE| @ 1 MHz, ## Darlington

(continued)

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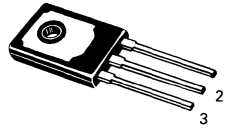
TABLE 7 — PLASTIC TO-225AA PACKAGE (Formerly TO-126) (continued)

I _C Cont Amps Max	V _{CEO(sus)} Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp		
3	40	MJE180	MJE170	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	45	BD175	BD176	40/250	0.15				3	30
		BD175.6	BD176.6	40/100	0.15				3	30
		BD175.10	BD176.10	63/160	0.15				3	30
		BD175.16	BD176.16	100/250	0.15				3	30
	60	BD177	BD178	40/250	0.15				3	30
BD177.6		BD178.6	40/100	0.15				3	30	
BD177.10		BD178.10	63/160	0.15				3	30	
BD177.16		BD178.16	100/250	0.15				3	30	
MJE181		MJE171	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5	
80	BD179	BD180	40/250	0.15				3	30	
	BD179.6	BD180.6	40/100	0.15				3	30	
	BD179.10	BD180.10	63/160	0.15				3	30	
	BD179.16	BD180.16	100/250	0.15				3	30	
	MJE182	MJE172	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5	
200	BUY49P		30 min	0.5				25	20	
4	20	BD433	BD434	50 min	2				3	36
	30	BD185	BD186	15 min	2				20	40
		BD435	BD436	50 min	2				3	36
	40	2N5190	2N5193	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		MJE521	MJE371	40 min	1				40	40
		2N6037##	2N6034##	750/18k	2	1.7 typ	1.2 typ	2	25	40
	45	BD187	BD188	15 min	2				20	40
		BD437	BD438	40 min	2				3	36
		BD675##	BD676##	750 min	1.5				40	40
		BD675A##	BD676A##	750 min	2				40	40
		BD785	BD786	20 min	2				50	15
		BD775##	BD776##	750 min	2				20	15
	60	BD189	BD190	15 min	2				20	40
BD439		BD440	25 min	2				3	36	
BD677##		BD678##	750 min	1.5				40	40	
BD677A##		BD678A##	750 min	2				40	40	
BD787		BD788	20 min	2				50	15	
BD777##		BD778##	750 min	2				20	15	
2N5191		2N5194	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40	
MJE800##		MJE700##	750 min	1.5				1#	40	
MJE801##		MJE701##	750 min	2				1#	40	
2N6038##		2N6035##	750/18k	2	1.7 typ	1.2 typ	2	25	40	
80		2N5192	2N5195	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
	BD441	BD442	15 min	2				3	36	
	BD679##	BD680##	750 min	1.5				40	40	
	BD679A##	BD680A##	750 min	2				40	40	
	BD789	BD790	10 min	2				40	15	
	BD779##	BD780##	750 min	2				20	15	
	MJE802##	MJE702##	750 min	1.5				1#	40	
	MJE803##	MJE703##	750 min	2				1#	40	
	2N6039##	2N6036##	750/18k	2	1.7 typ	1.2 typ	2	25	40	
100	BD681##	BD682##	750 min	1.5				40	15	
	BD791	BD792	10 min	2				40	15	
	MJE243	MJE253	40/120	0.2	0.7 typ	0.08 typ	0.2	40	15	
5	25	MJE200	MJE210	45/180	2	0.13 typ	0.035 typ	2	65	15

• Case 77 (Style 3), # |h_{FE}| @ 1 MHz, ## Darlington

TABLE 8 — PLASTIC TO-225AB (Formerly TO-127)

STYLE 2:
 PIN 1. EMITTER
 2. COLLECTOR
 3. BASE



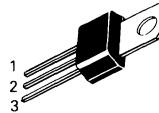
CASE 90-05
 PLASTIC

I _C Cont Amps Max	V _{CEO(sus)} Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp		
5	50		MJE105	25/100	2					65
	60	MJE1100##	MJE1090##	750 min	3A				1	70
		MJE1101##		750 min	4A				1	70
80	MJE1102##	MJE1092##	750 min	3A				1	70	
	MJE1103##	MJE1093##	750 min	4A				1	70	
8	60	MJE6043##	MJE6040##	1k/20k	4	1.5 typ	1.5 typ	4	4#	75
	80	MJE6044##	MJE6041##	1k/20k	4	1.5 typ	1.5 typ	4	4#	75
	100	MJE6045##		1k/20k	4	1.5 typ	1.5 typ	4	4#	75
10	45		BD206	15 min	4				1.5	90
	60	BD207	BD208	15 min	4				1.5	90
		MJE2801	MJE2901	25/100	3					90
MJE3055		MJE2955	20/70	4				2	90	
12	40	2N5989	2N5986	20/120	6	0.5 typ	0.25 typ	6	2	100
	60		2N5987	20/120	6	0.5 typ	0.25 typ	6	2	100
	80	2N5991	2N5988	20/120	6	0.5 typ	0.25 typ	6	2	100
15	40	MJE1660		20/100	5				3	90
	60	MJE1661		20/100	5				3	90

|h_{FE}| @ 1 MHz, ## Darlington

TABLE 9 — PLASTIC CASE 152

STYLE 1:
 PIN 1. EMITTER
 2. BASE
 3. COLLECTOR
 (COLLECTOR CONNECTED TO TAB)



I _C Cont Amps Max	V _{CEO(sus)} Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp		
0.5	300	MPS-U10	MPS-U60	30 min	0.03				60	10
0.8	40	MPS-U02	MPS-U52	30 min	0.5				150	10
1	120	MPS-U03		40 min	0.01				100	10
	180	MPS-U04		40 min	0.01				100	10
2	20	BD505	BD506	40 min	1				50	10
	30	BD507	BD508	40 min	1				50	10
		MPS-U01	MPS-U51	50 min	1				50	10
40	BD509	BD510	40 min	1					50	10
	MPS-U01A	MPS-U51A	50 min	1					50	10
	MPS-U45##	MPS-U95##	4k min	1					100	10

Darlington

(continued)

TABLE 9 — PLASTIC CASE 152 (continued)

I _C Cont Amps Max	V _{CEO} (sus) Volts Min	Device Type		hFE Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp		
		2	45			BD515	BD516	25 min		
	60	BD517 MPS-U05	BD518 MPS-U55	25 min 60 min	0.5 0.25				50 50	10 10
	80	BD519 MPS-U06	BD520 MPS-U56	25 min 60 min	0.5 0.25				50 50	10 10
	100	BD529 MPS-U07	BD530 MPS-U57	30 min 30 min	0.25 0.25				50 50	10 10

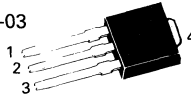
Darlington

TABLE 10 — DPAK — SURFACE MOUNT POWER PACKAGE

CASE 369A-04



CASE 369-03



STYLE 1:

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

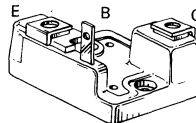
I _C Cont Amps Max	V _{CEO} (sus) Volts Min	Device Type*		hFE Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C
		NPN	PNP			t _s μs Typ	t _f μs Typ	@ I _C Amp		
		0.5	300			MJD340	MJD350	30/240		
1	40	MJD29	MJD30	15/75	1	0.6	0.3	1	3	15
	100	MJD29C	MJD30C	15/75	1	0.6	0.3	1	3	15
	250	MJD47		30/150	0.3	2	0.2	0.3	10	15
	400	MJD50		30/150	0.3	2	0.2	0.3	10	20
1.5	400	MJD13003		5/25	1	4 max	0.7 max	1	4	15
2	100	MJD112##	MJD117##	500 min	2	1.7	1.3	2	25#	20
3	40	MJD31	MJD32	25 min	1	0.6	0.3	1	3	15
	100	MJD31C	MJD32C	25 min	1	0.6	0.3	1	3	15
4	80	MJD6039##	MJD6036##	1k/12k	2	1.7	1.2	2	25	20
5	25	MJD200	MJD210	45/180	2	0.15	0.04	2	65	12.5
6	100	MJD41C	MJD42C	15/75	3	0.4	0.15	3	3	20
8	80	MJD44H11	MJD45H11	40 min	4	0.5	0.14	5	50 typ	20
	100	MJD122##	MJD127##	1k/12k	4	1.5	2	4	4#	20
10	60	MJD3055	MJD2955	20/100	4	1.5	1.5	3	2	20
	80	MJD44E3##		1k min	5	2	0.5	10		20

Darlington

* Case 369-03 may be ordered by adding -1 suffix to part number.

TABLE 11 — PLASTIC MO-040AA[†]

CASE 353-01



I _C Cont Amps Max	V _{CEO} (sus) Volts Min	Device Type		hFE Min/Max	@ I _C Amp	t _s μs Max	t _f μs Max	@ I _C Amp	P _D (Case) Watts @ 25°C
		NPN	PNP						
50	450	MJ10044##		50 min	50	3.8	1.3	50	250
100	250	MJ10047##		75 min	100	4	1	100	250
		MJ10048##		75 min	100	20	8	100	250

Darlington † Not recommended for new designs — consult Motorola.

Selection By Major Product Categories

TABLE 12 — MILITARY SPECIFIED POWER TRANSISTORS

I _C Cont Amps Max	V _{CEO} (sus) Volts Min	Device Type		hFE Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT	
		NPN/#	PNP/#			t _s μs Max	t _f μs Max	@ I _C Amp				
1	300	2N3739J,/402A TX, TXV		40/200	0.1	3.5*		0.5	10	20	TO-213AA/80	
3	40		2N3867J,/350A TX, TXV 2N3867SJ,/350A TX, TXV	40/200	1.5	0.5	0.1	1.5	60	10	TO-205AA/31	
				40/200	1.5	0.5	0.1	1.5	60	10	TO-205AD/79	
	60		2N3868J,/350A TX, TXV 2N3868SJ,/350A TX, TXV	30/150	1.5	0.5	0.1	1.5	60	10	TO-205AA/31	
				30/150	1.5	0.055	0.035	1.5	60	5	TO-205AD/79	
4	60	2N3766J,/518 TX, TXV	2N3740J,/441A TX, TXV	30/100	0.25	1*		1	5	25	TO-213AA/80	
				40/160	0.5	2.5*		0.5	10	25	TO-213AA/80	
	80	2N3767J,/518 TX, TXV	2N3741J,/441A TX, TXV	30/100	0.25	1*		1	5	25	TO-213AA/80	
				40/160	0.5	2.5*		0.5	10	25	TO-213AA/80	
5	100	2N5339J,/560 TX, TXV	2N6193J,/561 TX, TXV	60/240	2	2	0.2	2	30	6	TO-205AD/79	
8	60	2N6300J,/540** TX, TXV	2N6298J,/540** TX, TXV	750/18k	4	8*		4	25	75	TO-213AA/80	
	80	2N6301J,/540** TX, TXV	2N6299J,/540** TX, TXV	750/18k	4	8*		4	25	75	TO-213AA/80	
	250	2N6306J,/498		15/75	3	3*		3	5	125	TO-204/1	
	350	2N6308J,/498		12/60	3	3*		3	5	125	TO-204/1	
10	40	2N6383J,/523** TX, TXV	2N6648J,/527 TX, TXV	1k/20k	5	10*		5	20	100	TO-204/1	
			2N6648J,/527** TX, TXV	1k/20k	5	10*		5	50	85	TO-204/1	
	60	2N3715J,/408B TX, TXV 2N6384J,/523** TX, TXV	2N3791J,/379B TX, TXV	30/120	3	2*		5	4	150	TO-204/1	
			2N6649J,/527 TX, TXV	1k/20k	5	10*		5	20	100	TO-204/1	
		80	2N3716J,/408B TX, TXV 2N6385J,/523** TX, TXV	2N3792J,/379B TX, TXV	30/120	3	2*		5	4	150	TO-204/1
				2N6650J,/527** TX, TXV	1k/20k	5	10*		5	50	85	TO-204/1
12	80	2N6058J,/502** TX, TXV	2N6051J,/501** TX, TXV	1k/18k	6	10*		5	10	150	TO-204/1	
	100	2N6059J,/502** TX, TXV	2N6052J,/501** TX, TXV	1k/18k	6	10*		5	10	150	TO-204/1	
15	300	2N6546J,/525 TX		12/60	5	4.7*		10	6	175	TO-204/1	

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MIL-S-19500 Detailed Spec. shown by Device Type

* t_{off}

** Consult Factory for qualification status.

TABLE 12 — MILITARY SPECIFIED POWER TRANSISTORS (continued)

I _C Cont Amps Max	V _{CE0(sus)} Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT
		NPN/#	PNP/#			t _s μs Max	t _f μs Max	@ I _C Amp			
15	400	2N6547J,525 TX		12/60	5	4.7*		10	6	175	TO-204/1
20	75	2N5039J,439 TX, TXV**		30/150	2	2*		10	60	140	TO-204/1
		2N5303J,456A TX, TXV 2N6283J,504** TX, TXV	2N5745J,433 TX, TXV 2N6286J,505** TX, TXV	15/60 1250/18k	10 10	3* 10*		10 10	2 8	200 175	TO-204/1 TO-204/1
	80	2N5038J,439 TX, TXV**		50/200	2	2*		12	60	140	TO-204/1
	100	2N6284J,504** TX, TXV	2N6287J,505 TX, TXV	1250/18k	10	10*		10	8	175	TO-204/1
25	100	2N6338J,509 TX, TXV**		30/120	10	1		10	40	200	TO-204/1
			2N6437J,508 TX, TXV**	30/120	10	1		10	40	200	TO-204/1
	120		2N6438J,509 TX, TXV**	30/120	10	1		10	40	200	TO-204/1
150	2N6341J,509 TX, TXV**		30/120	1	1		10	40	200	TO-204/1	
30	60	2N5302J,456A TX, TXV	2N4399J,433 TX, TXV	15/60	15	3*		10	2	200	TO-204/1
50	60	2N5685J,464 TX, TXV	2N5683J,466 TX, TXV	15/60	25	3*		25	2	300	TO-204/197 MOD
		2N5686J,464 TX, TXV	2N5684J,466 TX, TXV	15/60	25	3*		25	2	300	TO-204/197 MOD
	100	2N6274J,514 TX, TXV**	2N6378J,515 TX, TXV**	30/120	20	1.05*		20	30	250	TO-204/197 MOD
	120		2N6379J,515 TX, TXV**	30/120	20	1.05*		20	30	250	TO-204/197 MOD
	150	2N6277J,514 TX, TXV**		30/120	20	1.05*		20	30	250	TO-204/197

MIL-S-19500 Detailed
Spec. shown by
Device Type

* t_{off}

** Consult
Factory for
qualification
status.

TABLE 13 — POWER DARLINGTONS

I _C Cont Amps Max	V _{CE0(sus)} Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			h _{fe} @ 1 MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp			
2	40	MPS-U45	MPS-U95	4k min	1				100	10	/152
	60	TIP110	TIP115	1k min	1	2 typ	1 typ	1	25	50	TO-220/221A
	80	TIP111	TIP116	1k min	1	2 typ	1 typ	1	25	50	TO-220/221A
	100	TIP112 MJE270	TIP117 MJE271	1k min 1.5k min	1 0.12	2 typ	1 typ	1	25 6	50 25	TO-220/221A TO-225AA/77

(continued)

TABLE 13 — POWER DARLINGTONS (continued)

I _C Cont Amps Max	V _{CEO(sus)} Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			h _{FE} @ 1 MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT	
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp				
4	40	MJE3300	MJE3310	1k min	1					15	TO-225AA/77R	
		2N6037	2N6034	750/1k	2	1.7 typ	1.2 typ	2	25	40	TO-225AA/77	
	45	BD675	BD676	750 min	1.5					40	TO-225AA/77	
		BD675A	BD676A	750 min	2					40	TO-225AA/77	
		BD775	BD776	750 min	2				20	15	TO-225AA/77	
	60	BD677	BD678	750 min	1.5					15	TO-225AA/77	
		BD677A	BD678A	750 min	2					40	TO-225AA/77	
		BD777	BD778	750 min	2				20	40	TO-225AA/77	
		MJE3301		1k min	1				20	15	TO-225AA/77R	
		MJE800	MJE700	750 min	1.5				1	40	TO-225AA/77	
		MJE800T	MJE700T	750 min	1.5				1	40	TO-220/221A	
		MJE801	MJE701	750 min	2				1	40	TO-225AA/77	
		2N6038	2N6035	750/18k	2	1.7 typ	1.2 typ	2	25	40	TO-225AA/77	
		2N6294	2N6296	750/18k	2	0.9 typ	0.7 typ	2	4	50	TO-213AA/80	
		80	BD679	BD680	750 min	1.5					40	TO-225AA/77
	BD679A		BD680A	750 min	2					40	TO-225AA/77	
	BD779		BD780	750 min	2				20	15	TO-225AA/77	
	MJE802		MJE702	750 min	1.5					40	TO-225AA/77	
MJE803	MJE703		750 min	2					40	TO-225AA/77		
2N6039	2N6036		750/18k	2	1.7 typ	1.2 typ	2	25	40	TO-225AA/77		
2N6295	2N6297		750/18k	2	0.9 typ	0.7 typ	2	4	50	TO-213AA/80		
100	BD681		BD682	750 min	1.5					40	TO-225AA/77	
5	60	MJE1100	MJE1090	750 min	3A				1	70	TO-225AB/90	
		MJE1101	MJE1091	750 min	4A				1	70	TO-225AB/90	
		TIP120	TIP125	1k min	3	1.5 typ	1.5 typ	3	4	65	TO-220/221A	
	80	MJE1102	MJE1092	750 min	3A				1	70	TO-225AB/90	
		MJE1103	MJE1102	750 min	4A				1	70	TO-225AB/90	
		TIP121	TIP126	1k min	3	1.5 typ	1.5 typ	3	4	65	TO-220/221A	
100	TIP122	TIP127	1k min	3	1.5 typ	1.5 typ	3	4	65	TO-220/221A		
7	300	MJ3041		250 min	2.5					100	TO-204/1	
	350	MJ3042		250 min	2.5					100	TO-204/1	
	375	BU522		250 min	2.5				7.5	75	TO-220/221A	
	425	BU522A		250 min	2.5				7.5	75	TO-220/221A	
	450	BU522B		250 min	2.5				7.5	75	TO-220/221A	
8	40	2N6386		1k/20k	3				20	65	TO-220/221A	
		45	BDX53	BDX54	750 min	3				4	60	TO-220/221A
			BD895	BD896	750 min	3				1	70	TO-220/221A
	BD895A		BD896A	750 min	4				1	70	TO-220/221A	
	60	BDX53A	BDX54A	750 min	3				4	60	TO-220/221A	
		BD897	BD898	750 min	3				1	70	TO-220/221A	
		BD897A	BD898A	750 min	4				1	70	TO-220/221A	
		MJ1000	MJ900	1k min	3					90	TO-204/11	
		TIP100	TIP105	1k/20k	3	1.5 typ	1.5 typ	3	4	80	TO-220/221A	
		2N6043	2N6040	1k/10k	4	1.5 typ	1.5 typ	3	4	75	TO-220/221A	
		2N6300	2N6298	750k/18k	4	1.5 typ	1.5 typ	4	4	75	TO-213AA/80	
		2N6055	2N6053	750k/18k	4	1.5 typ	1.5 typ	4	4	100	TO-204/11	
		MJE6043	MJE6040	1k/20k	4	1.5 typ	1.5 typ	4	2	75	TO-225AB/90	
		80	BDX53B	BDX54B	750 min	3				4	60	TO-220/221A
	BD899		BD900	750 min	3				1	70	TO-220/221A	
	BD899A		BD900A	750 min	4				1	70	TO-220/221A	
	MJ1001		MJ901	1k min	3					90	TO-204/11	
	TIP101		TIP106	1k/20k	3	1.5 typ	1.5 typ	3	4	80	TO-220/221A	

(continued)



TABLE 13 — POWER DARLINGTONS (continued)

I _C Cont Amps Max	V _{CEO} (sus) Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			h _{FE} @ 1 MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp			
8		2N6044	2N6041	1k/10k	4	1.5 typ	1.5 typ	3	4	75	TO-220/221A
		2N6301	2N6299	750k/18k	4	1.5 typ	1.5 typ	4	4	75	TO-213A/80
		2N6056	2N6054	750k/18k	4	1.5 typ	1.5 typ	4	4	100	TO-204A/11
		MJE6044	MJE6041	1k/20k	4	1.5 typ	1.5 typ	4	2	75	TO-225AB/90
	100	BDX53C	BDX54C	750 min	3				4	60	TO-220/221A
		BD901	BD902	750 min	3				1	70	TO-220/221A
		MJE6045		1k/20k	4	1.5 typ	1.5 typ	4	2	75	TO-225AB/90
		TIP102	TIP107	1k/20k	3	1.5 typ	1.5 typ	3	4	80	TO-220/221A
	2N6045	2N6042		1k/10k	4	1.5 typ	1.5 typ	3	4	75	TO-220/221A
	120	BDX53D	BDX54D	750 min	3				4	60	TO-220/221A
	150	BU807●		100 min	5	0.55 typ	0.2 typ	5		60	TO-220/221A
	200	BU806●		100 min	5	0.55 typ	0.2 typ	5		60	TO-220/221A
	300	MJE5740		200/400	4	8 typ	2 typ	6		80	TO-220/221A
350	MJE5741		200/400	4	8 typ	2 typ	6		80	TO-220/221A	
400	MJE5742		200/400	4	8 typ	2 typ	6		80	TO-220/221A	
500	BUT50P●		30 min	2	0.75 typ	0.1 typ	5		100	TO-218/340	
1400*	MJ10011		20 min	4			1	4	80	TO-204/1	
10	40	2N6383	2N6648	1k/20k	5				20	100	TO-204/11
		D44E1		1000 min	5	2 typ	0.5 typ	10		50	TO-220/221A
	45	BDX33	BDX34	750 min	4				3	70	TO-220/221A
	60	BDV65	BDV64	1k min	5					125	TO-218/340
		BDX33A	BDX34A	750 min	4				3	70	TO-220/221A
		MJ3000	MJ2500	1k min	5					150	TO-204/1
		2N6387	2N6667	1k/20k	5				20	65	TO-220/221A
		2N6384		1k/20k	5				20	100	TO-204/11
	D44E2		1000 min	5	2 typ	0.5 typ	10		50	TO-220/221A	
	D44E3		500 min	10	2.5 typ	2.5 typ	5	4	125	TO-218/340	
	TIP140	TIP145									
	80	2N6388	2N6668	1k/20k	5				20	65	TO-220/221A
		2N6385		1k/20k	5				20	100	TO-204/11
		BDV65A	BDV64A	1k min	5					125	TO-218/340
		BDX33B	BDX34B	750 min	3				3	70	TO-220/221A
		D44E3		1000 min	5	2 typ	0.5 typ	10		50	TO-220/221A
	TIP141	TIP146	500 min	10	2.5 typ	2.5 typ	5	4	125	TO-218/340	
	100	BDV65B	BDV64B	1k min	5					125	TO-218/340
		BDX33C	BDX34C	750 min	3				3	70	TO-220/221A
TIP142		TIP147	500 min	10	2.5 typ	2.5 typ	5	4	125	TO-218/340	
120	BDV65C	BDV64C	1k min	5					125	TO-218/340	
	BDX33D	BDX34D	750 min	3				3	70	TO-220/221A	
200	BU323P		150 min	6	15	15	6		125	TO-218/340	
250	BU323AP		150 min	6	15	15	6		125	TO-218/340	
350	BU323		150 min	6	7.5 typ	5.2 typ	6		175	TO-204/1	
	MJ10002		30/300	5	2.5	1	5	10	150	TO-204/1	
	MJ10006●		30/300	5	1.5	0.5	5	10	150	TO-204/1	
400	BU323A		150 min	6	7.5 typ	5.2 typ	6		175	TO-204/1	
	MJH10012		100/2k	6	15	15	6		118	TO-218/340	
	MJ10007●		30/300	5	1.5	0.5	5	10	150	TO-204/1	
	MJ10012		100/2k	6	15	15	6		175	TO-204/1	
600	MJ10014●		10/250	10	2.5	0.8	10		175	TO-204/1	

● Darlington with speed-up diode.

(continued)

TABLE 13 — POWER DARLINGTONS (continued)

I _C Cont Amps Max	V _{CEO} (sus) Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			h _{FE} @ 1 MHz	P _D (Case) Watts @ 25°C	Case JEDEC/MOT
						t _s μs Max	t _f μs Max	@ I _C Amp			
		NPN	PNP								
12	60	2N6057	2N6050	750/18k	6	1.6 typ	1.5 typ	6	4	150	TO-204/1
	80	2N6058	2N6051	750/18k	6	1.6 typ	1.5 typ	6	4	150	TO-204/1
	100	2N6059	2N6052	750/18k	6	1.6 typ	1.5 typ	6		150	TO-204/11
	1000	BUT16●		5 min	8	3.3	1.5	8		150	TO-204/1
15	60	2N6576		2k/20k	4	2	7	10	10/200	120	TO-204/11
	90	2N6577		2k/20k	4	2	7	10	10/200	120	TO-204/11
	120	2N6578		2k/20k	4	2	7	10	10/200	120	TO-204/11
	150	MJ11018	MJ11017	100 min	15				3	175	TO-204/1
		MJH11018	MJH11017	100 min	15				3	150	TO-218/340
	200	MJ11020	MJ11019	100 min	15				3	175	TO-204/1
		MJH11020	MJH11019	100 min	15				3	150	TO-218/340
	250	MJ11022	MJ11021	100 min	15				3	175	TO-204/1
MJH11022		MJH11021	100 min	15				3	150	TO-218/340	
500	BUT51P		40 min	5	1.1	0.16	10		125	TO-218/340	
16	60	MJ4033	MJ4030	1k min	10					150	TO-204/1
	80	MJ4034	MJ4031	1k min	10					150	TO-204/1
	100	MJ4035	MJ4032	1k min	10					150	TO-204/1
20	60	2N6282	2N6285	750/18k	10	2.5 typ	2.5 typ	10	4	160	TO-204/1
		MJH6282	MJH6285	750/18k	10	2.5 typ	2.5 typ	10	4	125	TO-218/340
	80	2N6283	2N6286	750/18k	10	2.5 typ	2.5 typ	10	4	160	TO-204/1
		MJH6283	MJH6286	750/18k	10	2.5 typ	2.5 typ	10	4	125	TO-218/340
	100	2N6284	2N6287	750/18k	10	2.5 typ	2.5 typ	10	4	160	TO-204/1
		MJH6284	MJH6287	750/18k	10	2.5 typ	2.5 typ	10	4	125	TO-218/340
	350	MJ10000		40/400	10	3	1.8	10	10	175	TO-204/1
		MJ10004●		40/400	10	1.5	0.5	10	10	175	TO-204/1
	400	MJ10001		40/400	10	3	1.8	10	10	175	TO-204/1
		MJ10005●		40/400	10	1.5	0.5	10	10	175	TO-204/1
	450	MJ10008●		30/300	10	2	0.6	10	8	175	TO-204/1
	500	MJ10009●		30/300	10	2	0.6	10	8	175	TO-204/1
	700	BUT15●		15 min	12	2.5	0.8	12		175	TO-204/1
750	MJ10024●		50/600	5	5	1.8	10		250	TO-204/1	
850	MJ10025●		50/600	5	5	1.8	10		250	TO-204/1	
24	1000	BUT36●		5 min	16	6	2.5	16		250	TO-204 Mod/197
25	500	BUT14●		15 min	16	2.8	0.8	16		175	TO-204/1
28	400	BUT13●		20 min	20	2.6	0.8	18		175	TO-204/1
30	60	MJ11012	MJ11011	1k min	20				4	200	TO-204/1
	90	MJ11014	MJ11013	1k min	20				4	200	TO-204/1
	120	MJ11016	MJ11015	1k min	20				4	200	TO-204/1
40	350	MJ10022●		50/600	10	2.5	0.9	20		250	TO-204 Mod/197
	400	MJ10023●		50/600	10	2.5	0.9	20		250	TO-204 Mod/197
	700	BUT35●		15 min	24	4	1.2	24		250	TO-204 Mod/197
50	60	MJ11028	MJ11029	400 min	50					300	TO-204 Mod/197

● Darlington with speed-up diode.

(continued)



TABLE 13 — POWER DARLINGTONS (continued)

I _C Cont Amps Max	V _{CE0} (sus) Volts Min	Device Type		hFE Min/Max	@ I _C Amp	Resistive Switching			h _{FE} @ 1 MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp			
50	90	MJ11030	MJ11031	400 min	50					300	TO-204 Mod/197
	120	MJ11032	MJ11033	400 min	50					300	TO-204 Mod/197
	400	MJ10015•		10 min	40	2.5	0.5	20	10	250	TO-204 Mod/197
	450	MJ10044•		50 min	50	3.8	1.3	50		250	— /353
	500	BUT34• MJ10016•		15 min 10 min	32 40	3 2.5	1.5 0.5	32 20	10	250 250	TO-204 Mod/197 TO-204 Mod/197
56	400	BUT33•		20 min	36	3.3	1.6	36		250	TO-204 Mod/197
60	200	MJ10020•		75/1k min	15	3.5	0.5	30		250	TO-204 Mod/197
	250	MJ10021•		75/1k min	15	3.5	0.5	30		250	TO-204 Mod/197
100	250	MJ10047•		75 min	100	4	1	100		250	— /353
		MJ10048•		75 min	100	20	8	100		250	— /353

• Darlington with speed-up diode.

TABLE 14 — POWER SWITCHING TRANSISTORS

V_{CE0} < 200 V

I _C Cont Amps Max	V _{CE0} (sus) Volts Min	Device Type		hFE Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp			
0.8	40	MPS-U02	MPS-U52	30 min	0.5				150	10	—/152
1	120	MPS-U03		40 min	0.1				100	10	—/152
	180	MPS-U04		40 min	0.1				100	10	—/152
2	20	BD505	BD506	40 min	1				50	10	—/152
	30	BD507	BD508	40 min	1				50	10	—/152
		MPS-U01	MPS-U51	50 min	1				50	10	—/152
	40	BD509	BD510	40 min	1				50	10	—/152
		MPS-U01A	MPS-U51A	50 min	1				50	10	—/152
		MPS-U45#	MPS-U95#	4k min	1				100	10	—/152
	45	BD515	BD516	25 min	0.5				50	10	—/152
	60	BD517	BD518	25 min	0.5				50	10	—/152
		MPS-U05	MPS-U55	60 min	0.25				50	10	—/152
80	BD519	BD520	25 min	0.5				50	10	—/152	
	MPS-U06	MPS-U56	60 min	0.25				50	10	—/152	
100	BD529	BD530	30 min	0.25				50	10	—/152	
	MPS-U07	MPS-U57	60 min	0.25				50	10	—/152	
150	2N5051		25/100	0.75	3.5	1.2	0.75	10	40	TO-213AA/80	
3	40		2N3719	25/180	2	0.4*		1	60	6	TO-205AA/31
			2N3867	40/200	2	0.4*		1	60	6	TO-205AA/31
	60		2N3720	25/180	2	0.4*		1	60	6	TO-205AA/31
			2N3868	30/150	2	0.4*		1	60	6	TO-205AA/31
80		2N6303	30/150	2	0.4*		1	60	6	TO-205AA/31	

Darlington

* t_{off} @ 1 MHz

(continued)

TABLE 14 — POWER SWITCHING TRANSISTORS (continued)

I _C Cont Amps Max	V _{CEO} (sus) Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp			
4	30	BD185	BD186	15 min	2				20	40	TO-225AA/77
	45	BD187	BD188	15 min	2				20	40	TO-225AA/77
		BD785	BD786	20 min	2				50	15	TO-225AA/77
	60	2N4877	BD190 BD788	20/100	4	1.5	0.5	4	30	10	TO-205AD/79
		BD189		15 min	2			20	40	TO-225AA/77	
		BD787		20 min	2			50	15	TO-225AA/77	
80	BD789	BD790	10 min	2				40	15	TO-225AA/77	
100	BD791	BD792	10 min	2				40	15	TO-225AA/77	
5	60		MJ8100	25/180	2	1	0.15	2	30	10	TO-205AD/79
	80	2N5337	2N6191	60/240	2	2	0.2	2	30	10	TO-205AD/79
	100	2N5339	2N6193	60/240	2	2	0.2	2	30	10	TO-205AD/79
7	60	2N6315	2N6317	20/100	2.5	1	0.8	2.5	4	90	TO-213AA/80
	80	2N5428	2N6187 2N6318	60/240	2	2	0.2	2	30	60	TO-213AA/80
		2N5347		60/240	2	2	0.2	2	30	60	TO-210AA/160
		2N6316		20/100	2.5	1	0.8	2.5	4	90	TO-213AA/80
100	2N5430	2N6189	60/240	2	2	0.2	2	30	60	TO-213AA/80	
	2N5349		60/240	2	2	0.2	2	30	60	TO-210AA/160	
7.5	60	2N3447		40/120	5	2	0.35	5	10	115	TO-204/11
	80	2N3448		40/120	5	2	0.35	5	10	115	TO-204/11
8	120	MJ3247	MJ3237	40 min	3	0.4 typ	0.18 typ	5	20	75	TO-213AA/80
		MJ4247	MJ4237	40 min	3	0.4 typ	0.18 typ	5	20	90	TO-204/11
		MJE15028	MJE15029	20 min	4	0.4 typ	0.18 typ	5	30	50	TO-220/221A
	150	MJ3248	MJ3238	40 min	3	0.4 typ	0.18 typ	5	20	75	TO-213AA/80
MJ4248		MJ4238	40 min	3	0.4 typ	0.18 typ	5	20	90	TO-204/11	
MJE15030		MJE15031	20 min	4	0.4 typ	0.18 typ	5	30	50	TO-220/221A	
10	60		MJ6700	25/180	2	1	0.15	2	30	60	TO-210AA/160
		2N5877	2N5875	20/100	4	1	0.8	4	4	150	TO-204/11
	80	2N5878	2N5876	20/100	4	1	0.8	4	4	150	TO-204/11
15	60	2N5881	2N5879	20/100	6	1	0.8	6	4	160	TO-204/11
	80	2N5882	2N5880	20/100	6	1	0.8	6	4	160	TO-204/11
18	160	BUX41N		8 min	12	1.2	0.25	12	8	120	TO-204/1
20	75	2N5039		20/100	10	1.5	0.5	10	60	140	TO-204/1
	80	2N5303	2N5745	15/60	10	2	1	10	2	200	TO-204/11
	90	2N5038		20/100	12	1.5	0.5	12	60	140	TO-204/1
	125	BUX40		8 min	15	1	0.25	15	8	120	TO-204/1
	160	BUV11N		10 min	15	1.2	0.25	15	8	150	TO-204/1
25	60	2N5885	2N5883	20/100	10	1	0.8	10	4	200	TO-204/11
		2N5886	2N5884 2N6436	20/100 30/120	10 10	1 1	0.8 0.25	10 10	4 40	200 200	TO-204/11 TO-204/1
	100	2N6338	2N6437	30/120	10	1	0.25	10	40	200	TO-204/1
		30/120		10	1	0.25	10	40	200	TO-204/1	
	120	2N6339	2N6438	30/120	10	1	0.25	10	40	200	TO-204/1
		30/120		10	1	0.25	10	40	200	TO-204/1	
125	BUV10		10 min	20	1.2	0.25	20	8	150	TO-204/1	
	BUV10N		10 min	20	1.55	0.45	15	10	175	TO-204/1	

(continued)

TABLE 14 — POWER SWITCHING TRANSISTORS (continued)

I _C Cont Amps Max	V _{CE0(sus)} Volts Min	Device Type		h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT
		NPN	PNP			t _s μs Max	t _f μs Max	@ I _C Amp			
		25	140			2N6340		30/120			
	150	2N6341		30/120	10	1	0.25	10	40	200	TO-204/1
30	40	2N5301	2N4398	15/60	15	2	1	10	2	200	TO-204/11
	60	2N5302	2N4399	15/60	15	2	1	10	2	200	TO-204/11
	90	BUX39		8 min	20	1	0.25	20	8	120	TO-204/1
40	160	BUV21N		10 min	40	1	0.2	40	8	250	TO-204 Mod/197
50	80		2N6377	30/120	20	0.8					TO-204 Mod/197
	100	2N6274	2N6378	30/120	20	0.8	0.25	20	30	250	TO-204 Mod/197
	120	2N6275	2N6379	30/120	20	0.8	0.25	20	30	250	TO-204 Mod/197
	125	BUV20		10 min	50	1.2	0.25	50	8	250	TO-204 Mod/197
	140	2N6276		30/120	20	0.8	0.25	20	30	250	TO-204 Mod/197
	150	2N6277		30/120	20	0.8	0.25	20	30	250	TO-204 Mod/197
70	125	BUS50		15 min	50					350	TO-204 Mod/197

TABLE 15 — SWITCHMODE POWER TRANSISTORS

V_{CE0} ≥ 200 V

Devices are listed in descending order of V_{CE0(sus)}, and I_CCont

V _{CE0(sus)} Volts Min	I _C Cont Amps Max	V _{CEV} Volts Min	Device Type NPN unless otherwise noted	h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT
						t _s μs Max	t _f μs Max	@ I _C Amp			
1000	24	1400	BUT36##	5 min	16	6	2.5	16		250	TO-204 Mod/197
	12	1400	BUT16##	5 min	8	3.3	1.5	8		150	TO-204/1
900	2	1800	MJE1320	3 min	1	4 typ	0.8 typ	1		80	TO-220/221A
850	20	1200	MJ10025##★	50/600	20	5	1.8	10			TO-204/1
	3	1500	MJE16034 MJH16034	4 min 4 min	3 3	2 2	1.5 1.5	2 2		80 125	TO-220/221A TO-218/340
800	10	1400	MJ8505★	7.5 min	1.5	4	2	5			TO-204/1
		1500	MJ16018★	4 min	5	4.5 typ	0.2 typ	5			TO-204/1
		1500	MJH16018★	4 min	5	4.5 typ	0.2 typ	5			TO-218/340
	5	1400	MJ8503★	7.5 min	1	4	2	2.5			TO-204/1
		1400	MJE8503★	7.5 min	1	4	2	2.5			TO-220/221A
	2.5	1400	MJ8501★	7.5 min	0.5	4	2	1			TO-204/1
1400		MJE8501★	7.5 min	0.5	4	2	1			TO-220/221A	
750	20	1000	MJ10024##★	50/600	20	5	1.8	10			TO-204/1
	8	1500	MJ12005	5 min	5		1	5	4 typ		TO-204/1
		1500	MJH12005				0.4 typ	5	4	100	TO-218/340
	5	1500	MJ12004★	2.5 min	4.5		1	4.5	4 typ		TO-204/1
	4	1500	MJ12003	2.5 min	3		1	3	4 typ		TO-204/1

* Designers Data Sheet characterization
Darlington ## Darlington with speed-up diode

* I_{off} ** |h_{FE}| @ 1 MHz

(continued)

TABLE 15 — SWITCHMODE POWER TRANSISTORS (continued)

V _{CEO(sus)} Volts Min	I _C Cont Amps Max	V _{CEV} Volts Min	Device Type NPN unless otherwise noted	h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT	
						t _s μs Max	t _f μs Max	@ I _C Amp				
750	3	1500	MJE16032 MJH16032	4 min 4 min	3 3	2 2	1.5 1.5	2 2		80 125	TO-220/221A TO-218/340	
	2.5	1500	MJ12002★ MJE12007★	1.11 min 1.1 min	2 2		1 1	2 2	4 typ 4 typ		TO-204/1 TO-220/221A	
700	40	1000	BUT35##	15 min	24	4	1.2	24		250	TO-204 Mod/197	
	20	1000	BUT15##	15 min	12	2.5	0.8	12		175	TO-204/1	
	10	1200	MJ8504★	7.5 min	1.5	4	2	5			TO-204/1	
	8	1400 1500	1500	MJ10011#	20 min	4		1	4			TO-204/1
				BU508,A BU508D,AD	2.25 min 2.25 min	4.5 4.5	8 typ 8 typ	0.5 typ 0.5 typ	4.5 4.5	7 7	125 125	TO-218/340 TO-218/340
	5	1200 1200	1500	MJ8502★	7.5 min	1	4	2	2.5			TO-204/1
				MJE8502★	7.5 min	1	4	2	2.5			TO-220/221A
BU208A BU208D				2.25 min 2.25 min	4.5 4.5	8 typ 8 typ	0.4 typ 0.6 typ	4.5 4.5	4 typ	90	TO-204/1 TO-204/1	
2.5	1200	MJE8500★	7.5 min	0.5	4	2	1			TO-220/221A		
600	15	700	MJ10014###	10/250	10	2.5	0.8	10			TO-204/1	
550		650	MJ10013###	10/250	10	2.5	0.8	10			TO-204/1	
500	50	750	MJ10016###	10 min	40	2.5	1	20			TO-204 Mod/197	
			850	BUT34##	15 min	32	3	1.5	32		250	TO-204 Mod/197
	25	850	BUT14##	15 min	16	2.8	0.8	16		175	TO-204/1	
	20	600	800	MJ10009###	30/300	10	2	0.6	10	8**		TO-204/1
				MJ13335★	10/60	5	4	0.7	10		TO-204/1	
	15	850	1000	BUT51P##	40 min	5	1.1	0.16	10		125	TO-218/340
				MJ16010A★	5 min	15	3	0.4	10			TO-204/1
				MJH16010A★	5 min	15	3	0.4	10			TO-218/340
	8	850	1000	BUT50P##	30 min	2	0.75 typ	0.1 typ	5		100	TO-218/340
MJ16006A★				5 min	15	3	0.4	10			TO-204/1	
MJH16006A★				5 min	15	3	0.4	10			TO-218/340	
5	1000	1000	MJ16002A★	5 min	15	3	0.3	3			TO-204/1	
			MJH16002A★	5 min	15	3	0.3	3			TO-218/340	
450	50	500	MJ10044###	50 min	50	3.8	1.3	50			—/353	
	30	850	MJ16020	5 min	30	1.8	0.2	20		250	TO-204/1	
			MJ16022	7 min	30	1.5	0.15	20		250	TO-204/1	
			BUS98A	8 min	16	2.3	0.4	16		250	TO-204 Mod/197	
	20	650	850	MJ10008###	30/300	10	2	0.6	10	8**		TO-204/1
				2N6837★	10/30	15	2.5	0.25	15		15	TO-204/1
				MJ16014★	5 min	20	2.7	0.35	20			TO-204/197
				MJ16016★	7 min	20	2.2	0.25	20			TO-204/197
	15	750	850	MJ13091★	8 min	10	2.5	0.5	10	10		TO-204/1
				2N6836★	10/30	10	3	0.35	10			TO-204/1
				MJ12022★	5 min	15		0.1 typ	10			TO-204/1
				MJ16010★	5 min	15	1.2 typ	0.2 typ	10			TO-204/1
				MJ16012★	7 min	15	0.9 typ	0.15 typ	10			TO-204/1
MJH16010★				5 min	15	1.2	0.2	10			175	TO-218/340
MJH16012★				7 min	15	0.9	0.15	10			150	TO-218/340
1000	BUS48A	8 min	10	2	0.4	10		175	TO-204/1			

★ Designers Data Sheet characterization
Darlington ## Darlington with speed-up diode

* t_{off} ** |h_{FE}| @ 1 MHz

(continued)

TABLE 15 — SWITCHMODE POWER TRANSISTORS (continued)

V _{CEO} (sus) Volts Min	I _C Cont Amps Max	V _{CEV} Volts Min	Device Type NPN unless otherwise noted	hFE Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT
						t _s μs Max	t _f μs Max	@ I _C Amp			
450	15	1000 1000	BUS48AP	8 min	8	2	0.4	10		150 175	TO-218/340 TO-218/340
			BUW13A			4	0.8	8			
	9	1000 1000	BUS47A	7 min	5	2	0.4	5		150 128	TO-204/1 TO-218/340
			BUS47AP	7 min	6	2	0.4	6			
	8	750 850 850 850 850 850 850 1000	MJ13081★	8 min	5	1.5	0.5	5	10	80	TO-204/1 TO-204/1 TO-220/221A TO-204/1 TO-204/1 TO-204/1 TO-218/340 TO-218/340
			2N6835★	7.5/3	5	2.5	0.25	5			
			MJE16080	5 min	8	2	0.5	5			
			MJ12021★	5 min	8		0.1 typ	8			
			MJ16006★	5 min	8	2.5	0.25	5			
			MJ16008★	7 min	8	2.2	0.25	5			
			MJH16006★	5 min	8	2.5	0.25	5			
			MJH16008★	7 min	8	2.2	0.25	5			
	BUW12A	6 min	5	4	0.8	5					
	5	750 750 850 850 850 850 850 850 850 1000	MJ13071★	8 min	3	1.5	0.5	3	15	125	TO-204/1 TO-220/221A TO-204/1 TO-204/1 TO-204/1 TO-204/1 TO-220/221A TO-220/221A TO-218/340 TO-218/340
			MJE13071★	8 min	3	1.5	0.5	3			
			2N6834★	10/30	3	2.7	0.35	3			
			MJ12020★	5 min	5		0.13 typ	3			
			MJ16002★	5 min	5	3	0.3	3			
MJ16004★			8 min	3	2.7	0.35	3				
MJE16002★			5 min	5	3	0.3	3				
MJE16004★			7 min	5	2.7	0.35	3				
MJH16002★			5 min	5	3	0.3	3				
MJH16004★			7 min	5	2.7	0.35	3				
BUW11A	6 min	2.5	4	0.8	2.5						
3	1000	BUX85	30 min	0.1	3.5	1.4	1	4	50	TO-220/221A	
400	56	600	BUT33##	20 min	36	3.3	1.6	36		250	TO-204 Mod/197
	50	650	MJ10015##★	10 min	40	2.5	1	20			TO-204 Mod/197
	40	600	MJ10023##★	50/600	10	2.5	0.9	20			TO-204 Mod/197
	30	850	BUS98	8 min	20	2.3	0.4	20		250	TO-204 Mod/197
	28	600	BUT13##	20 min	20	2.6	0.8	18		175	TO-204/1
	20	450	BUV24	8 min	12	3	0.9	12	8	250	TO-204/1 TO-204/1 TO-204/1 TO-204/1
		500	MJ10001##★	40/400	10	3	1.8	10	10**		
		500	MJ10005##★	40/400	10	1.5	0.5	10	10**		
		500	MJ13333★	10/60	5	4	0.7	10			
	15	650	MJ13090★	8 min	10	2.5	0.5	10	6 to 24	125	TO-204/1 TO-218/340 TO-204/1 TO-204/1 TO-204/1 TO-218/340 TO-218/340
		650	MJH6678	8 min	15	2.5	0.5	15			
		650	2N6678	8 min	15	2.5	0.5	15			
		850	2N6547★	6/30	10	4	0.7	10			
		850	BUS48	8 min	10	2	0.4	10			
		850	BUS48P	8 min	10	2	0.4	10			
		850	BUW13			4	0.8	10			
	850	BUX48			3	0.6	10				
	12	700	MJE13009★	6/30	8	3	0.7	8	4**		TO-220/221A
10	950	MJ12010	4.2 min	5		1	5	6 typ		TO-204/1 TO-204/1 TO-204/1 TO-204/1 TO-204/1	
	550	MJ10012#	100/2k	6	6	15	15	6			
	500	MJ10003##★	30/300	5	2.5	1	5	10**			
	500	MJ10007##★	30/300	5	1.1	0.25	5	10**			
	450	MJ13015★	8/20	5	2	0.5	5				
9	850	BUS47	7 min	6	2	0.4	6		150	TO-204/1	
	850	BUS47P	7 min	5	2	0.4	6		128	TO-218/340	

★ Designers Data Sheet characterization
Darlington ## Darlington with speed-up diode

* t_{off} ** |h_{fe}| @ 1 MHz

(continued)

TABLE 15 — SWITCHMODE POWER TRANSISTORS (continued)

V _{CEO(sus)} Volts Min	I _C Cont Amps Max	V _{CEV} Volts Min	Device Type NPN unless otherwise noted	h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz	P _D (Case) Watts @ 25°C	Case JEDEC/MOT	
						t _s μs Max	t _f μs Max	@ I _C Amp				
	8	850	2N6545★	7/35	5	4	1	5	6	80 125 50	TO-204/1	
		800	MJE5742#	200/400	4	8 typ	2 typ	6			TO-220/221A	
		800	MJE16080	5 min	8	2	0.5	5			TO-220/221A	
		850	BUW12	6 min	6	4	0.8	5			TO-218/340	
		850	BUX84	30 min	0.1	3.5	1.4	1			TO-220/221A	
		700	MJE13007★	6/30	5	3	0.7	5			TO-220/221A	
		650	MJ13080★	8 min	5	1.5	0.5	5			TO-204/1	
		450	MJ6503-PNP★	15 min	2	2	0.5	4			TO-204/1	
		450	MJE5852-PNP★	15 min	2	2	0.5	4			TO-220/221A	
	6	900	BU326A	30 typ	0.6	3.5	1**	2.5	6	90	TO-204/1	
		900	BU426A	30 typ	0.6	2 typ	0.5 typ	2.5			6 typ	113
	5	850	2N6543★	7/35	3	4	0.8	3	6	125	TO-204/1	
850		BUW11	6 min	3	4	0.8	3	TO-218/340				
650		MJ13070★	8 min	3	1.5	0.5	3	TO-204/1				
650		MJE13070★	8 min	3	1.5	0.5	3	TO-220/221A				
4	700	MJE13005★	6/30	3	3	0.7	3	4		TO-220/221A		
1.5	700	MJE13003★	5/25	1	4	0.7	1	5		TO-225AA/77R		
0.5	400	MJ4647-PNP	20 min	0.5	0.72*		0.05	40		TO-205AD/79		
375	6	800	BU326	30 typ	0.6	3.5	1**	2.5	6	90	TO-204/1	
		800	BU426	30 typ	0.6	2 typ	0.5 typ	2.5			6 typ	113
350	40	450	MJ10022##★	50/600	10	2.5	0.9	20			TO-204 Mod/197	
		450	MJ10000##★	40/400	10	3	1.8	10	10**		TO-204/1	
	450	MJ10004##★	40/400	10	1.5	0.5	10	10**		TO-204/1		
	15	550	2N6677	8 min	15	2.5	0.5	15	3	125	TO-204/1	
		375	2N6251	6/50	10	3.5	1	10			2.5	TO-204/1
		550	MJH6677	8 min	15	2.5	0.5	15			TO-218/340	
	10	450	MJ10002##★	30/300	5	2.5	1	5	10**		TO-204/1	
		450	MJ10006##★	30/300	5	1.5	0.5	5	10**		TO-204/1	
		400	MJ13014★	8/20	5	2	0.5	5			TO-204/1	
	8	700	2N6308	12/60	3	1.6	0.4	5	5		TO-204/1	
700		MJE5741#	200/400	4	8 typ	2 typ	6	TO-220/221A				
400		MJE5851-PNP	15 min	2	2	0.5	4	TO-220/221A				
2	400	2N6213-PNP	10/100	1	2.5	0.6	1	4		TO-213AA/80		
325	30	400	BUV23	8 min	16	1.8	0.4	16	8	250	TO-204 Mod/197	
		400	BUX13	8 min	8	2.5	0.8	8			8	150
	5	350	2N6235	25/125	1	3.5	0.5	1	20		TO-213AA/80	
300	15	650	2N6546★	6/30	10	4	0.7	10	6 to 24	125	TO-204/1	
		450	2N6676	8 min	15	2.5	0.5	15			3	TO-204/1
		450	MJH6676	8 min	15	2.5	0.5	15				TO-218/340
	12	600	MJE13008★	6/30	8	3	0.7	8	4**		TO-220/221A	
	8	600	2N6307	15/75	3	1.6	0.4	3	5		TO-204/1	
		600	MJE13006★	6/30	5	3	0.7	5			4	TO-220/221A
		600	MJE5740	200/400	4	8 typ	2 typ	6			TO-220/221A	
		350	MJE5850-PNP★	15 min	2	2	0.5	4			TO-220/221A	
	5	400	2N6498	10/75	2.5	1.8	0.8	2.5	5		TO-220/221A	
	4	600	MJE13004★	6/30	3	3	0.7	3	4		TO-220/221A	
	2	500	2N3585	25/100	1	4	3	1	10		TO-213AA/80	
		500	2N6422-PNP	25/100	1	4	3	1	10		TO-213AA/80	
		350	2N6212-PNP	10/100	1	2.5	0.6	1	4		TO-213AA/80	
1.5	600	MJE13002★	5/25	1	4	0.7	1	5		TO-225AA/77R		

★ Designers Data Sheet characterization
 # Darlington ## Darlington with speed-up diode * t_{off} ** |h_{FE}| @ 1 MHz



TABLE 15 — SWITCHMODE POWER TRANSISTORS (continued)

V _{CEO(sus)} Volts Min	I _C Cont Amps Max	V _{CEV} Volts Min	Device Type NPN unless otherwise noted	h _{FE} Min/Max	@ I _C Amp	Resistive Switching			f _T MHz Min	P _D (Case) Watts @ 25°C	Case JEDEC/MOT
						t _s μs Max	t _f μs Max	@ I _C Amp			
300	1	300	2N5345-PNP	25/100	0.5	0.6	0.1	0.5	60		TO-213AA/80
	0.5	300	MJ4646-PNP	20 min	0.5	0.72*		0.05	40		TO-205AD/79
275	15	300	2N6250	8/50	10	3.5	1	10	2.5		TO-204/1
250	100	300	MJ10047##★	75 min	100	4	1	100			—/353
		300	MJ10048#★	75 min	100	2	8	100			—/353
	60	350	MJ10021##★	25 min	30	3.5	0.5	30			TO-204 Mod/197
	40	300	BUV22	10 min	20	1.1	0.35	20	8	250	TO-204/1
		350	BUS52	15 min	40					350	TO-204/1
	20	300	BUV12	10 min	10	1.5	0.5	10	8	150	TO-204/1
		450	MJ13331★	8/40	10	3.5	0.7	10	5/40		TO-204/1
	15	250	MJ11021#-PNP	100 min	15				3#		TO-204/1
		250	MJ11022#	100 min	15				3#		TO-204/1
	12	300	BUX42	8 min	6	2	0.4	6	8	120	TO-204/1
	8	500	2N6306	15/75	3	1.6	0.4	3	5		TO-204/1
		400	MJ6502-PNP★	15 min	2	2	0.5	4			TO-204/1
	5	500	MJ3029	30 min	0.4		1	3			TO-204/11
350		2N6497	10/75	2.5	1.8	0.8	2.5	5		TO-220/221A	
2	375	2N3584	25/100	1	4	3	1	10		TO-213AA/80	
	375	2N6421-PNP	25/100	1	4	3	1	10		TO-213AA/80	
1	250	2N5344-PNP	25/100	0.5	0.6	0.1	0.5	60		TO-213AA/80	
225	2	275	2N6211	10/100	1	2.5	0.6	1	20		TO-213AA/80
200	60	300	MJ10020##★	25 min	30	3.5	0.5	30			TO-204 Mod/197
	50	300	BUS51	15 min	50					350	TO-204/1
	40	250	BUV21	10 min	25	1.8	0.4	25	8	150	TO-204/1
	20	250	BUV11	10 min	12	1.8	0.4	12	8	150	TO-204/1
		400	MJ13330★	8/40	10	3.5	0.7	10	5/40		TO-204/11
	15	225	2N6249	10/50	10	3.5	1	10	2.5		TO-204/11
250		BUX41	8 min	8	1.5	0.4	8	8	120	TO-204/1	
200		MJ11019#-PNP	100 min	15				3#		TO-204/1	
200		MJ11020#	100 min	15				3#		TO-204/1	
3	250	BUY49P	30 min	0.5				25	20	TO-225AA/77	

★ Designers Data Sheet characterization

Darlington

Darlington with speed-up diode

* t_{off}

** |h_{FE}| @ 1 MHz

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Application Selector Guides

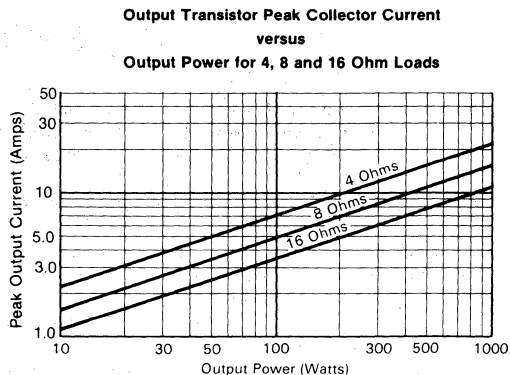
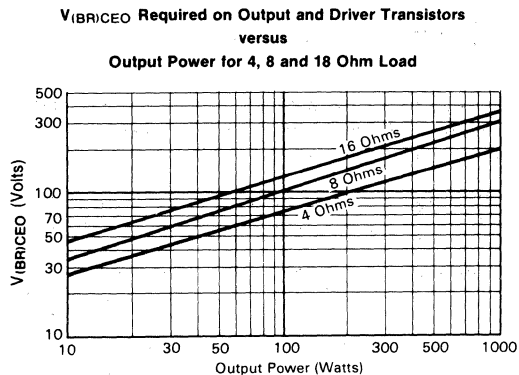
Application Literature

To obtain copies of these notes, simply list the AN, AR, EB or EN numbers and send your request to:
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|----------------|--|---------------|--|
| AN-222A | The ABC's of Solid-State DC-to-AC Inverters | AN-875 | Power Transistor Safe Operating Area — Special Considerations for Switching Power Supplies |
| AN-484A | Medium Power Audio Amplifiers | AN-915 | Characterizing Collector-To-Emitter and Drain-To-Source Diodes for Switchmode Applications |
| AN-485 | High-Power Audio Amplifiers with Short-Circuit Protection | AN-951 | Drive Optimization for 1 kV Offline Converter Transistors |
| AN-569 | Transient Thermal Resistance — General Data and its Use | AN-952 | Ultrafast Recovery Rectifiers Extend Power Transistor SOA |
| AN-703 | Designing Digitally-Controlled Power Supplies | AR-109 | Power Transistor Safe Operating Area — Special Considerations for Motor Drives |
| AN-719 | A New Approach to Switching Regulators | AR-119 | Dynamic Saturation Voltage — A Designers Comparison |
| AN-766 | A Variable Frequency Control for 3 ϕ Induction Motors | AR-120 | Speeding Up the High Voltage Transistor Baker Clamps, Traditional Concepts Updated. . . |
| AN-767 | A Line Operated, Regulated 5 V/50 A Switching Power Supply | AR-131 | Electronic Ballasts |
| AN-778 | Mounting Techniques for Power Semiconductors | AR-180 | Bipolar Transistors Excel in Off-Line Resonant Converters |
| AN-785 | Reverse-Bias Safe Operating Area | EB-76 | Horizontal CRT Deflection Techniques |
| AN-786 | Power Darlington Load Line Considerations | EB-78 | New ICs in Switching Supplies |
| AN-803 | The Effect of Emitter-Base Avalanching on High-Voltage Power Switching | EB-85A | Full-Bridge Switching Power Supplies |
| AN-828 | The Effects of Base Drive Conditions on RBSOA | EB-86A | Half-Bridge Switching Power Supplies |
| AN-845 | New Bipolars Compare Favorably with FETs for Switching Efficiency | EB-87A | Flyback Switching Power Supplies |
| AN-861 | Power Transistors Safe Operating Area — Special Considerations for Motor Drives | EB-88A | Push-Pull Switching Power Supplies |
| AN-873 | Understanding Power Transistor Dynamic Behavior — dv/dt Effects on Switching RBSOA | EB-99 | Proportional Reverse Base Current Drive Circuit |
| | | EN-101 | Verifying Collector Voltage Ratings |

Audio

GENERAL DESIGN CURVES FOR POWER AUDIO OUTPUT STAGES



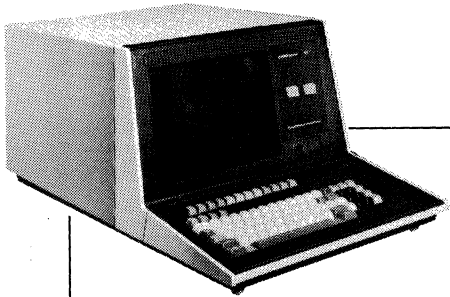
Another important parameter that must be considered before selecting the output transistors is the safe-operating area these devices must withstand. For a complete discussion on these see Application Notes AN-484A and AN-485.

TABLE 16 — RECOMMENDED POWER TRANSISTORS FOR AUDIO/SERVO LOADS

RMS Power Output	NPN	PNP	Case	P _D Watts @ 25°C	V _{CEO}	h _{FE} @ Min/Max	I _C Amps	f _T MHz Typ	ISB Volts/Amps
To 25W	MJE15030	MJE15031	TO-220	50W	150 V	20 min	4A	70	14/3.6
25 to 50W	2N3055A MJ15001	MJ2955A MJ15002	TO-204	120W	120 V	20/70	4A	3	60/2
			TO-204	200W	140 V	25/150	4A	3	40/5
50 to 100W	MJ15015 MJ15003	MJ15016 MJ15004	TO-204	180W	120 V	20/70	4A	3	60/3
			TO-204	250W	140 V	25/150	5A	3	100/1
Over 100W	MJ15024	MJ15025	TO-204	250W	250 V	15/60	8A	8	80/2.2

The Power Transistors shown are provided for reference only and show device capability. The final choice of the Power Transistors used is left to the circuit designer and depends upon the particular safe-operating area required and the mounting and heat sinking configuration used.

CRT Deflection



The typical raster scanning television or CRT data monitor normally uses an inductive switched horizontal output stage. The horizontal output switching is accomplished by a high voltage bipolar power transistor. This device switches from 0.5 to 5 A or higher collector current levels and must block a 100 to 1500 V retrace or flyback pulse. The listed Motorola semiconductor power devices will easily handle this task if the circuit electrical parameters have been properly established.

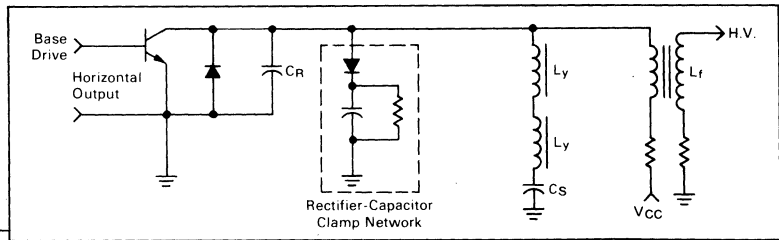


TABLE 17 — HORIZONTAL CRT DEFLECTION TRANSISTOR SELECTOR GUIDE

2

Applications	Retrace Voltage	I _{PK} Amps	Scan Rate	Preferred Devices*	V _{CEX} Volts	I _C Amps
Line Operated T.V. (120 Vac) Small Screen B/W Large Screen B/W, or Small Color Large Screen Color	Up to 975	1 to 2	15 k	MJ12002	1500	2.5
	Up to 975	2 to 3	15 k	MJ12003	1500	4
	Up to 975	4 to 5	15 k	BU508,D	1500	8
Battery Operated T.V.	Up to 250	3 to 10	15 k	BU407	350	7
Display Monitors Low End High End	Up to 250	3 to 10	20 k	BU407	350	7
	Up to 975	2 to 5	30 k	MJH16018	1500	8

* Additional selections are available for specific circuit requirements — see Device Selection By Package Type.

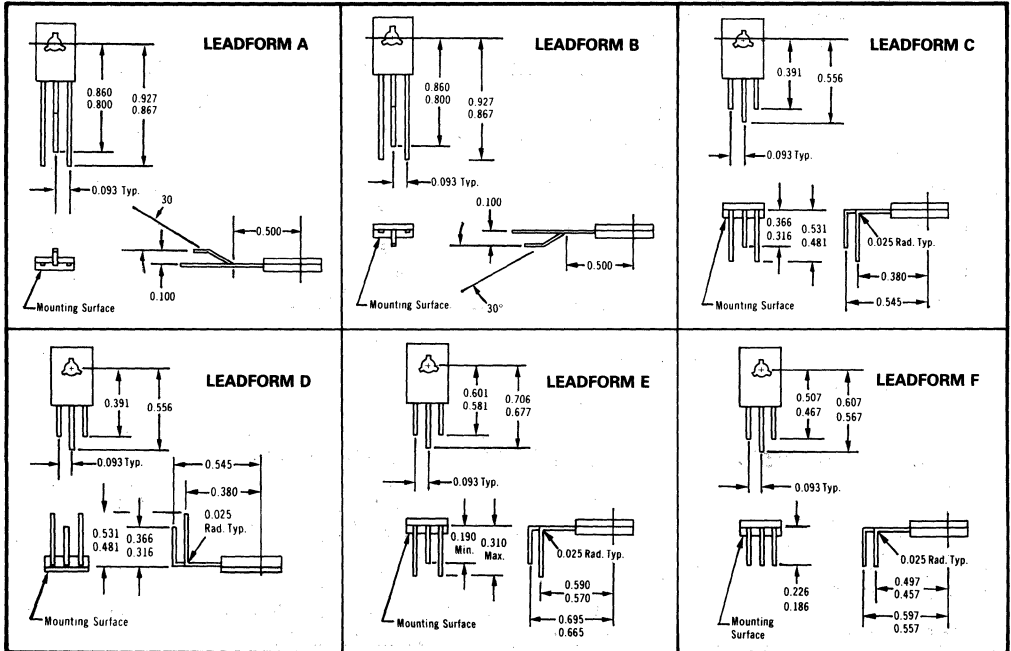
Preferred Leadform Options For Motorola Plastic Power Transistors

ORDERING INFORMATION

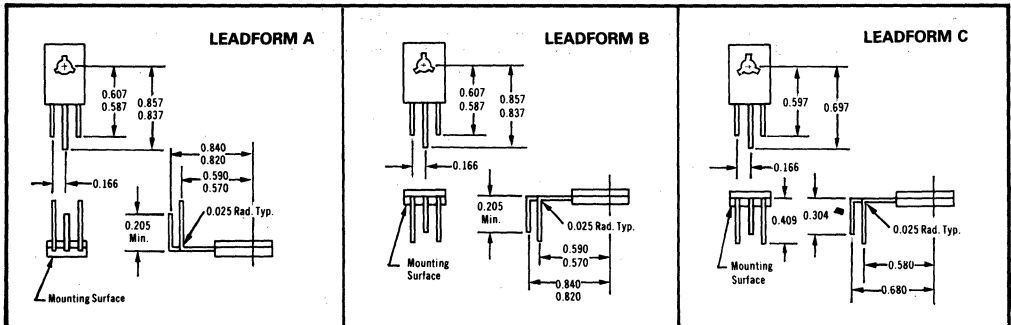
TO-225AA (Case 77), TO-225AB (Case 90), TO-220AB (Case 221A)

Devices may be leadformed by first converting to a special "SJE" number. The factory must be given the designation of the package and the applicable leadform suffix letter. The factory must be consulted.

TO-225AA LEADFORMS



TO-225AB LEADFORMS

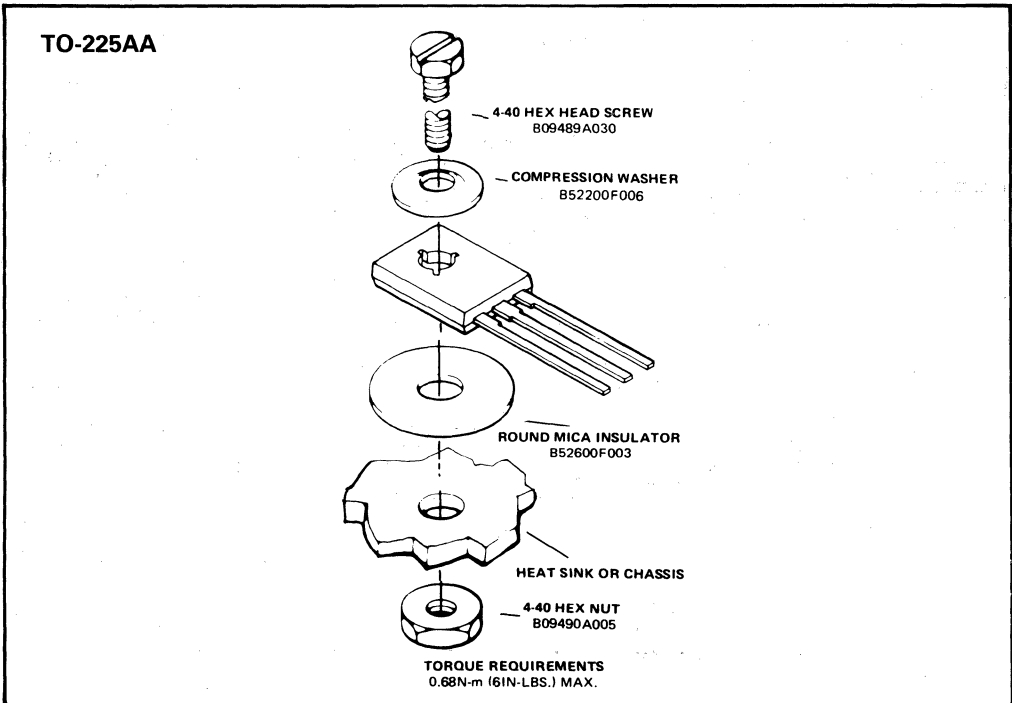
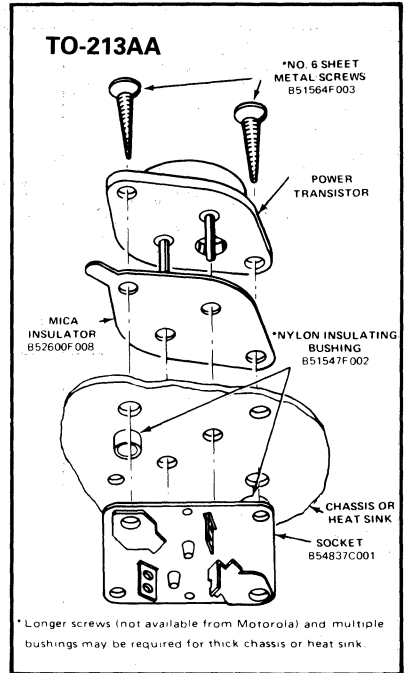
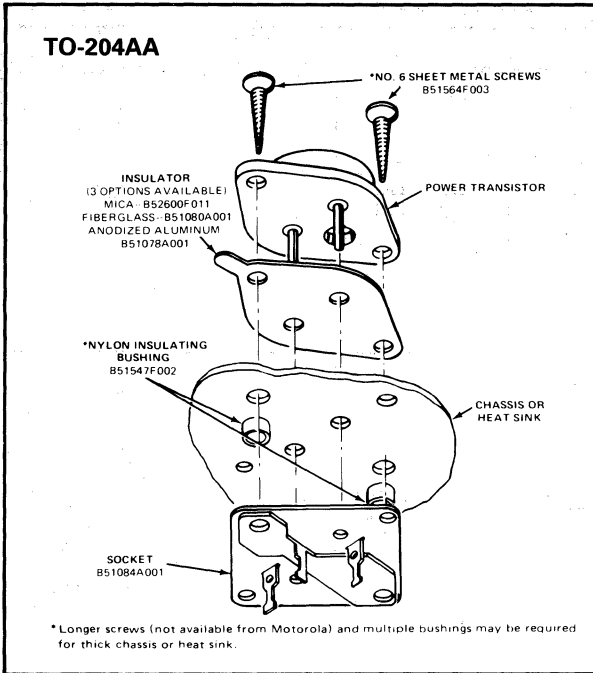


TO-220 LEADFORMS

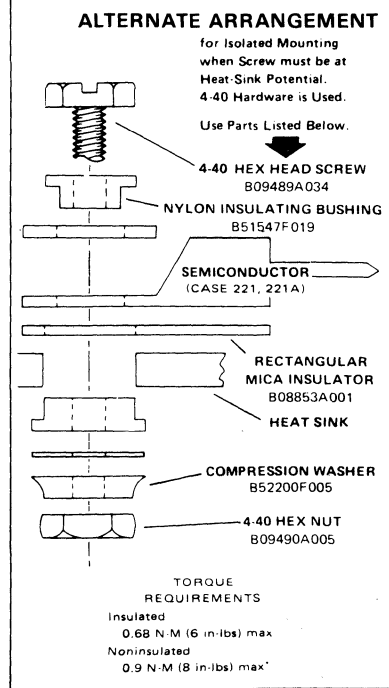
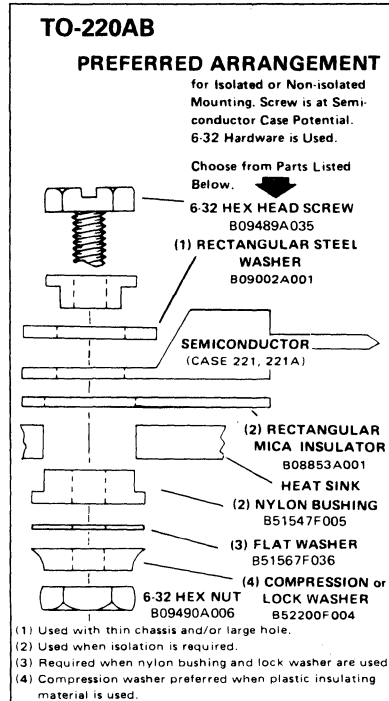
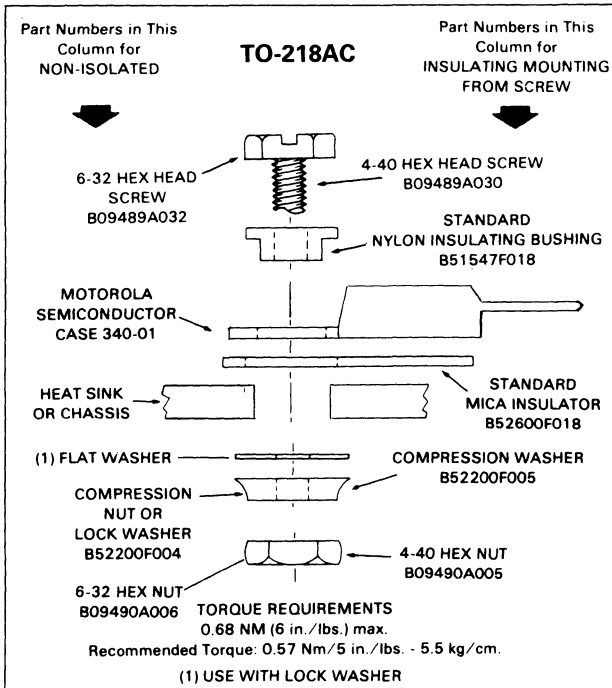
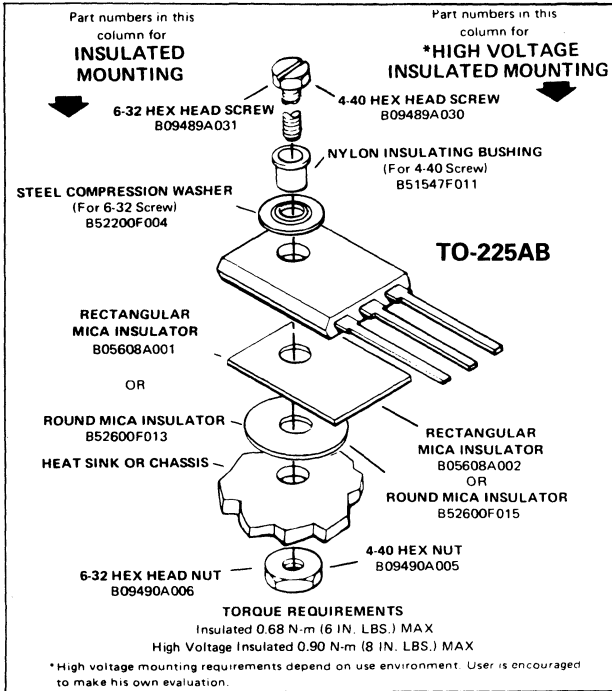
Options are listed in parenthesis below standard dimensions.

<p>LEADFORM AJ</p>	<p>LEADFORM AK</p>	<p>LEADFORM S</p>
<p>LEADFORMS W & WC</p>	<p>LEADFORM 2A</p>	<p>LEADFORMS 3 & 3A</p>
<p>LEADFORMS 5F & 5FA</p>	<p>LEADFORMS 5R & 5RA</p>	<p>LEADFORMS 10R & 10RC</p>
<p>LEADFORM 15FA</p>	<p>LEADFORM 16</p>	

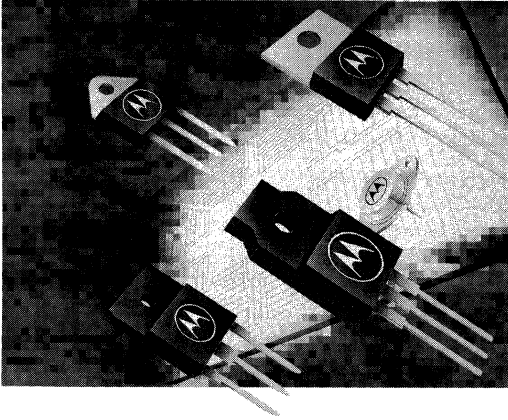
Mounting Hardware



MOUNTING HARDWARE — continued



2



Data Sheets

3

The following power transistor data sheets are arranged in alphanumeric sequence, some data sheets may contain information applying to more than one transistor — e.g. 2N4398, 2N4399, 2N5745. To determine if a particular device type is covered by a data sheet in this section, either refer to the alphanumeric listing of the Index and Cross Reference on page 1-2 or simply turn to the proper sequence for indication of where the Data Sheet can be found.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N3054
2N3054A

MEDIUM-POWER NPN SILICON TRANSISTORS

... designed for general purpose switching and amplifier applications.

- Excellent Safe Operating Area
- DC Current Gain Specified to 3.0 Amperes
- Complement to PNP Type 2N6049 or 2N4912

***MAXIMUM RATINGS**

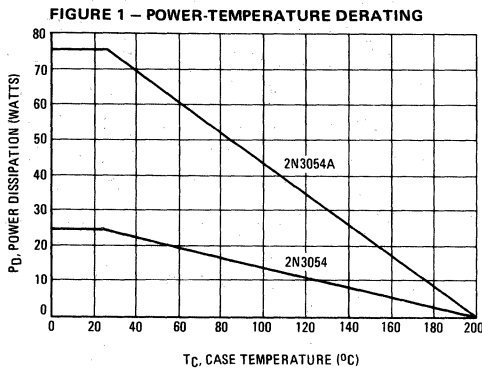
Rating	Symbol	2N3054A	2N3054	Unit
Collector-Emitter Voltage	V_{CEO}	55		Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	60		Vdc
Collector-Base Voltage	V_{CB}	90		Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current – Continuous Peak	I_C	4.0 10**		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	75 0.43	25 0.143	Watts W/ $^\circ C$
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ C$

*Indicates JEDEC Registered Data

**Addition to JEDEC Registered Data

THERMAL CHARACTERISTICS

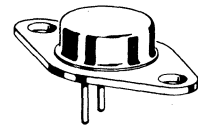
Characteristic	Symbol	2N3054A	2N3054	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.33	7.0	$^\circ C/W$



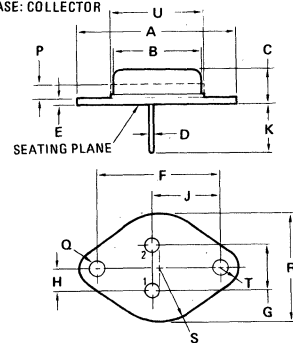
4 AMPERE

POWER TRANSISTORS
NPN SILICON

55 VOLTS
25 WATTS – 2N3054
75 WATTS – 2N3054A



STYLE 1:
 PIN 1, BASE
 2, EMITTER
 CASE, COLLECTOR



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

2N3054,A

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
*OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 100 mA _{dc} , I _B = 0)	V _{CEO(sus)}	55	—	V _{dc}
Collector-Emitter Sustaining Voltage (1) (I _C = 100 mA _{dc} , R _{BE} = 100 Ω)	V _{CER(sus)}	60	—	V _{dc}
Collector Cutoff Current (V _{CE} = 30 V _{dc} , I _B = 0)	I _{CEO}	—	500	μA _{dc}
Collector Cutoff Current (V _{CE} = 90 V _{dc} , V _{BE(off)} = 1.5 V _{dc}) (V _{CE} = 90 V _{dc} , V _{BE(off)} = 1.5 V _{dc} , T _C = 150°C)	I _{CEX}	—	1.0 6.0	mA _{dc}
Emitter Cutoff Current (V _{BE} = 7.0 V _{dc} , I _C = 0)	I _{EBO}	—	1.0	mA _{dc}

*ON CHARACTERISTICS (1)

DC Current Gain (I _C = 0.5 A _{dc} , V _{CE} = 4.0 V _{dc}) (I _C = 3.0 A _{dc} , V _{CE} = 4.0 V _{dc})	h _{FE}	25 5.0	150 —	—
Collector-Emitter Saturation Voltage (I _C = 500 mA _{dc} , I _B = 50 mA _{dc}) (I _C = 3.0 A _{dc} , I _B = 1.0 A _{dc})	V _{CE(sat)}	— —	1.0 6.0	V _{dc}
Base-Emitter On Voltage (I _C = 500 mA _{dc} , V _{CE} = 4.0 V _{dc})	V _{BE(on)}	—	1.7	V _{dc}

DYNAMIC CHARACTERISTICS

Current-Gain—Bandwidth Product (I _C = 200 mA _{dc} , V _{CE} = 10 V _{dc})	f _T	3.0	—	MHz
*Small-Signal Current Gain (I _C = 100 mA _{dc} , V _{CE} = 4.0 V _{dc} , f = 1.0 kHz)	h _{fe}	25	180	—
*Common-Emitter Cutoff Frequency (I _C = 100 mA _{dc} , V _{CE} = 4.0 V _{dc})	f _{hfe}	30	—	kHz

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

3

FIGURE 2 — SWITCHING TIME EQUIVALENT TEST CIRCUIT

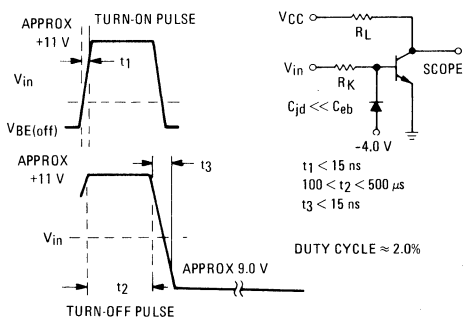


FIGURE 3 — TURN-ON TIME

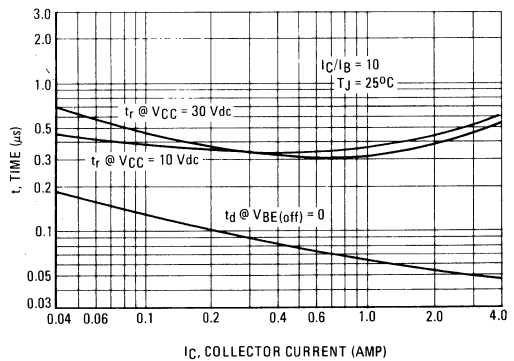


FIGURE 4 – THERMAL RESPONSE

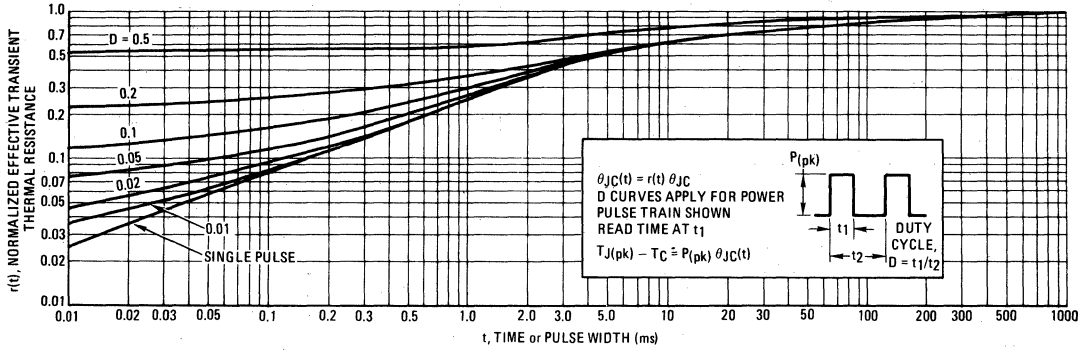
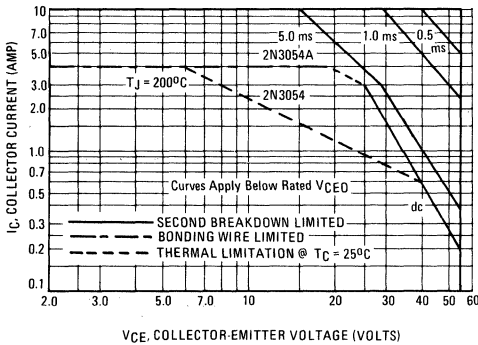


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

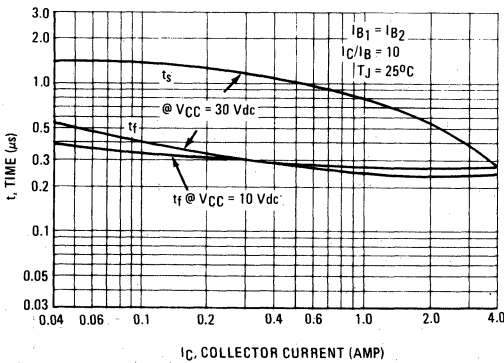


FIGURE 7 – CAPACITANCE

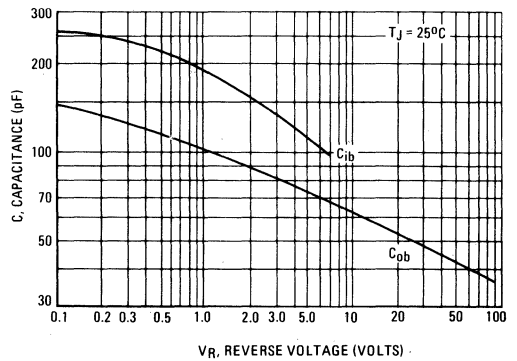


FIGURE 8 – DC CURRENT GAIN

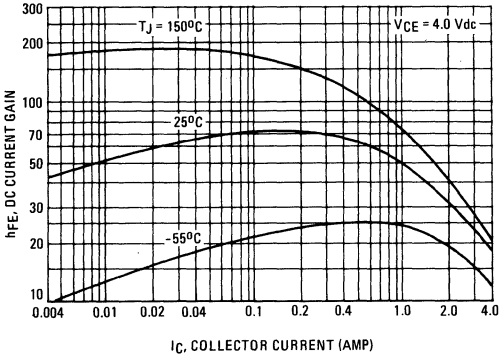


FIGURE 9 – COLLECTOR SATURATION REGION

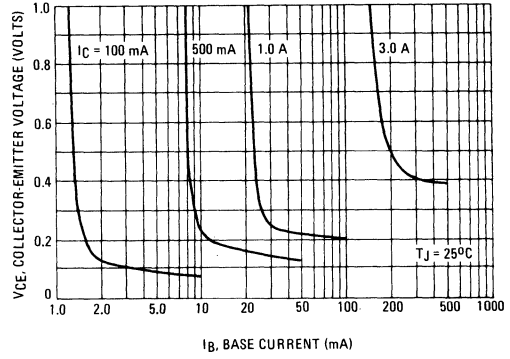


FIGURE 10 – TEMPERATURE COEFFICIENTS

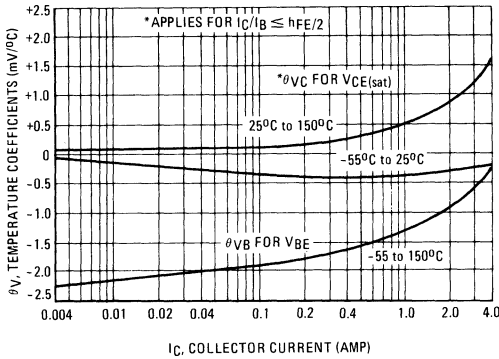


FIGURE 11 – "ON" VOLTAGES

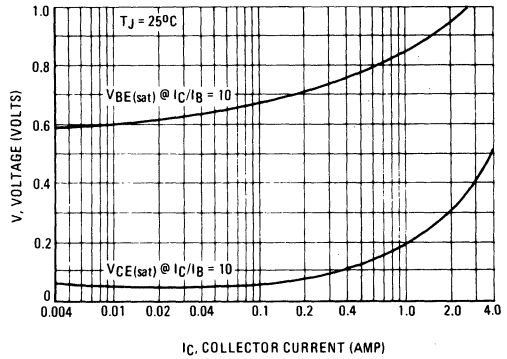


FIGURE 12 – COLLECTOR CUT-OFF REGION

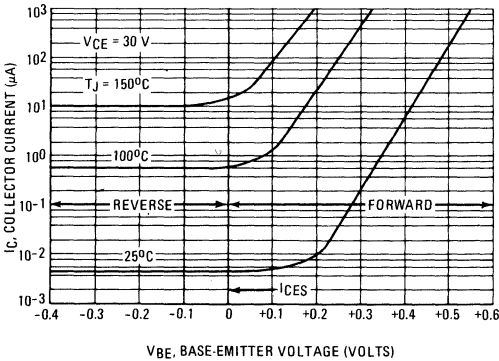
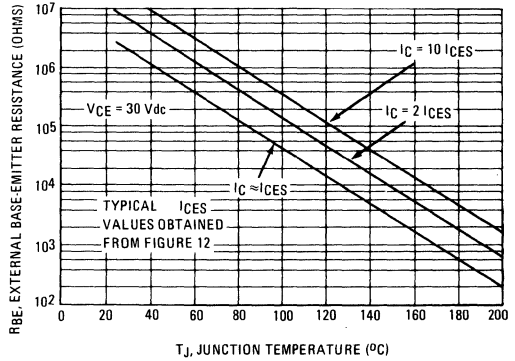


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

**NPN
2N3055
PNP
MJ2955**

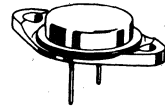
COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for general-purpose switching and amplifier applications.

- DC Current Gain – $h_{FE} = 20-70 @ I_C = 4 \text{ Adc}$
- Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.1 \text{ Vdc (Max) @ } I_C = 4 \text{ Adc}$
- Excellent Safe Operating Area

15 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

**60 VOLTS
115 WATTS**

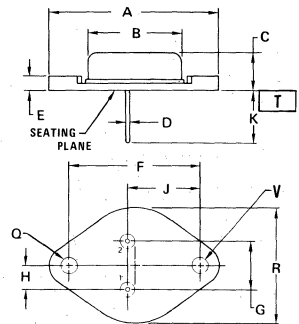


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Emitter Voltage	V_{CER}	70	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	7	Vdc
Collector Current – Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	115 0.657	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	$^\circ\text{C/W}$



NOTES:

1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\text{M } \varnothing 0.25 (0.010) \text{ M } T | V \text{ M}$
3. POSITIONAL TOLERANCE FOR LEADS:
 $\text{M } \varnothing 0.30 (0.012) \text{ M } T | V \text{ M } Q \text{ M}$
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

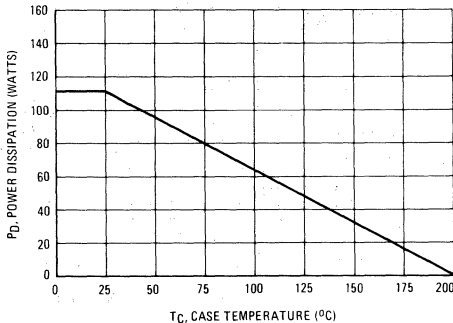
STYLE 1:

PIN 1: BASE
2: EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050
V	3.84	4.09	0.151	0.161

**CASE 11-01
TO-204AA**

FIGURE 1 – POWER DERATING



2N3055 NPN/MJ2955 PNP

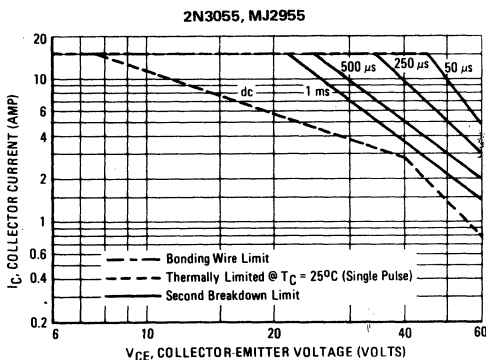
ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
*OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	60	—	Vdc
Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mAdc}$, $R_{BE} = 100 \text{ Ohms}$)	$V_{CER(sus)}$	70	—	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current ($V_{CE} = 100 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 100 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	—	1.0 5.0	mAdc
Emitter Cutoff Current ($V_{BE} = 7.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	5.0	mAdc
*ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 10 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	20 5.0	70 —	—
Collector-Emitter Saturation Voltage ($I_C = 4.0 \text{ Adc}$, $I_B = 400 \text{ mAdc}$) ($I_C = 10 \text{ Adc}$, $I_B = 3.3 \text{ Adc}$)	$V_{CE(sat)}$	—	1.1 3.0	Vdc
Base-Emitter On Voltage ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.5	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 40 \text{ Vdc}$, $t = 1.0 \text{ s}$; Nonrepetitive)	$I_{s/b}$	2.87	—	Adc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	f_T	2.5	—	MHz
*Small-Signal Current Gain ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	15	120	—
*Small-Signal Current Gain Cutoff Frequency ($V_{CE} = 4.0 \text{ Vdc}$, $I_C = 1.0 \text{ Adc}$, $f = 1.0 \text{ kHz}$)	f_{hfe}	10	—	kHz

* Indicates Within JEDEC Registration. (2N3055)

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

2N3055 NPN/MJ2955 PNP

NPN
2N3055

PNP
MJ2955

FIGURE 3 – DC CURRENT GAIN

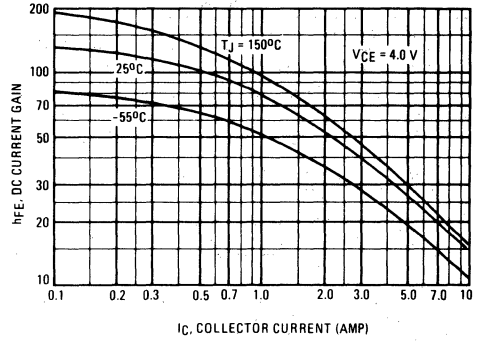
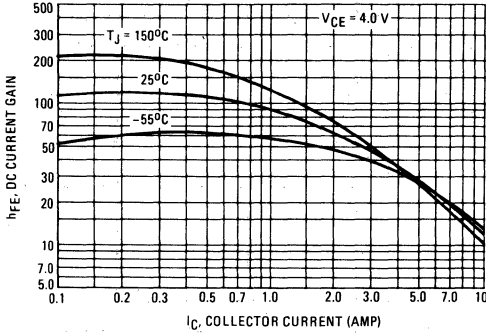


FIGURE 4 – COLLECTOR SATURATION REGION

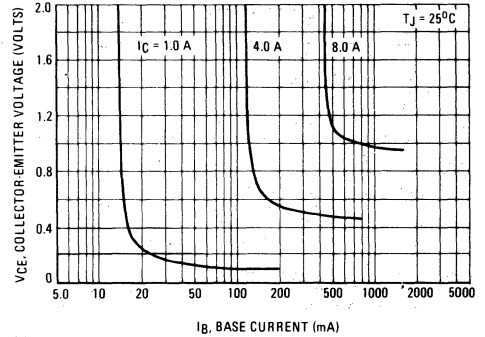
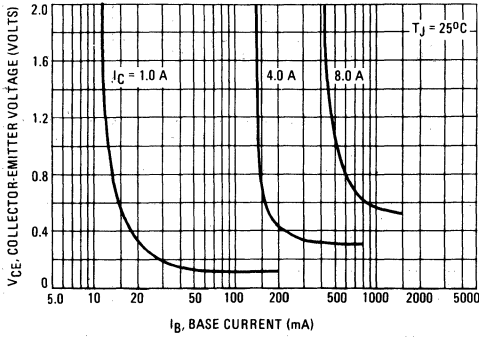
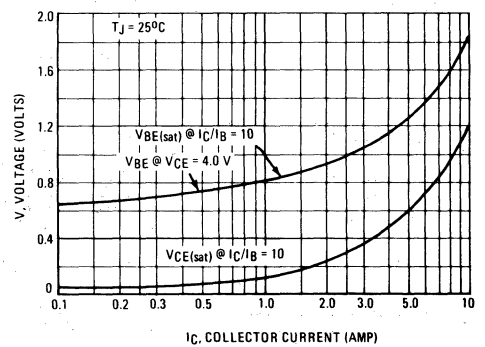
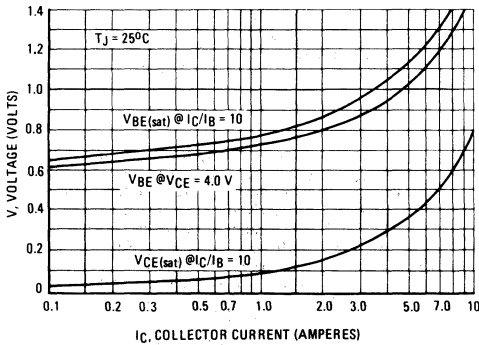


FIGURE 5 – "ON" VOLTAGES



3

NPN **PNP**
2N3055A **MJ2955A**
MJ15015 **MJ15016**

**COMPLEMENTARY SILICON
 HIGH-POWER TRANSISTORS**

... PowerBase complementary transistors designed for high power audio, stepping motor and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc-to-dc converters, inverters, or for inductive loads requiring higher safe operating area than the 2N3055 and MJ2955.

- Current-Gain – Bandwidth-Product @ $I_C = 1.0$ Adc
 $f_T = 0.8$ MHz (Min) – NPN
 $= 2.2$ MHz (Min) – PNP
- Safe Operating Area – Rated to 60 V and 120 V, Respectively

***MAXIMUM RATINGS**

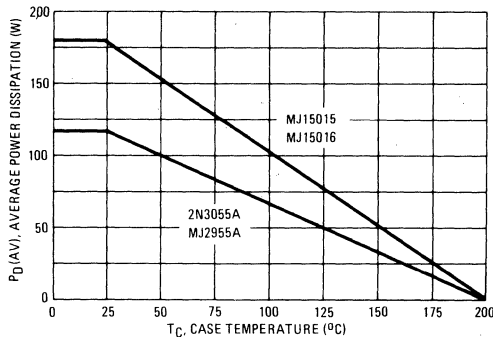
Rating	Symbol	2N3055A MJ2955A	MJ15015 MJ15016	Unit
Collector-Emitter Voltage	V_{CEO}	60	120	Vdc
Collector-Base Voltage	V_{CBO}	100	200	Vdc
Collector-Emitter Voltage Base Reversed Biased	V_{CEV}	100	200	Vdc
Emitter-Base Voltage	V_{EBO}	7.0		Vdc
Collector Current – Continuous	I_C	15		Adc
Base Current	I_B	7.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	115 0.65	180 1.03	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.52	0.98	$^\circ\text{C}/\text{W}$

*Indicates JEDEC Registered Data (2N3055A)

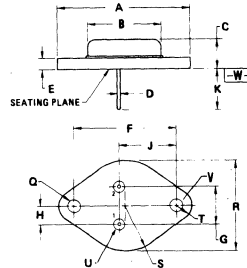
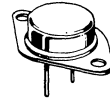
FIGURE 1 – POWER DERATING



15 AMPERE

**COMPLEMENTARY SILICON
 POWER TRANSISTORS**

60, 120 VOLTS
115, 180 WATTS



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

- NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.
 2. DIAMETER V AND SURFACE W ARE DATUMS.
 3. POSITIONAL TOLERANCE FOR HOLE Q:
 $\text{⌀} \pm 0.25 (0.010) \text{ Ⓜ } | \text{ V } \text{Ⓜ}$
 4. POSITIONAL TOLERANCE FOR LEADS:
 $\text{Ⓜ} \pm 0.30 (0.012) \text{ Ⓜ } | \text{ W } | \text{ V } \text{Ⓜ} \text{Ⓜ} \text{Ⓜ}$

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.03	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.37 BSC	—	0.430 BSC	—
H	3.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

**CASE 1-04
 TO-204AA**

NPN 2N3055A, MJ15015
PNP MJ2955A, MJ15016

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS (1)					
*Collector-Emitter Sustaining Voltage ($I_C = 200 \text{ mA}$, $I_B = 0$)	2N3055A, MJ2955A MJ15015, MJ15016	$V_{CE(sus)}$	60 120	— —	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $V_{BE(off)} = 0 \text{ Vdc}$) ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 0 \text{ Vdc}$)	2N3055A, MJ2955A MJ15015, MJ15016	I_{CEO}	— —	0.7 0.1	mAdc
*Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5 \text{ Vdc}$)	2N3055A, MJ2955A MJ15015, MJ15016	I_{CEV}	— —	5.0 1.0	mAdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	2N3055A, MJ2955A MJ15015, MJ15016	I_{CEV}	— —	30 6.0	mAdc
*Emitter Cutoff Current ($V_{EB} = 7.0 \text{ Vdc}$, $I_C = 0$)	2N3055A, MJ2955A MJ15015, MJ15016	I_{EBO}	— —	5.0 0.2	mAdc
*SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased ($t = 0.5 \text{ s}$ non-repetitive) ($V_{CE} = 60 \text{ Vdc}$)	2N3055A, MJ2955A MJ15015, MJ15016	$I_{S/b}$	1.95 3.0	— —	A
*ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 10 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)		h_{FE}	10 20 5.0	70 70 —	—
Collector-Emitter Saturation Voltage ($I_C = 4.0 \text{ Adc}$, $I_B = 400 \text{ mAdc}$) ($I_C = 10 \text{ Adc}$, $I_B = 3.3 \text{ Adc}$) ($I_C = 15 \text{ Adc}$, $I_B = 7.0 \text{ Adc}$)		$V_{CE(sat)}$	— — —	1.1 3.0 5.0	Vdc
Base-Emitter On Voltage ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)		$V_{BE(on)}$	0.7	1.8	Vdc
*DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	2N3055A, MJ15015 MJ2955A, MJ15016	f_T	0.8 2.2	6.0 18	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)		C_{ob}	60	600	pF
*SWITCHING CHARACTERISTICS (2N3055A only)					
RESISTIVE LOAD					
Delay Time	($V_{CC} = 30 \text{ Vdc}$, $I_C = 4.0 \text{ Adc}$, $I_{B1} = I_{B2} = 0.4 \text{ Adc}$, $t_p = 25 \mu\text{s}$ Duty Cycle $\leq 2\%$)	t_d	—	0.5	μs
Rise Time		t_r	—	4.0	μs
Storage Time		t_s	—	3.0	μs
Fall Time		t_f	—	6.0	μs

(1) Pulse Test: Pulse Width = $300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

*Indicates JEDEC Registered Data (2N3055A)

NPN 2N3055A, MJ15015
PNP MJ2955A, MJ15016

FIGURE 2 – DC CURRENT GAIN

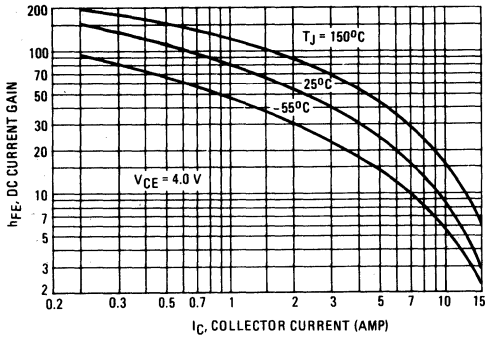


FIGURE 3 – COLLECTOR SATURATION REGION

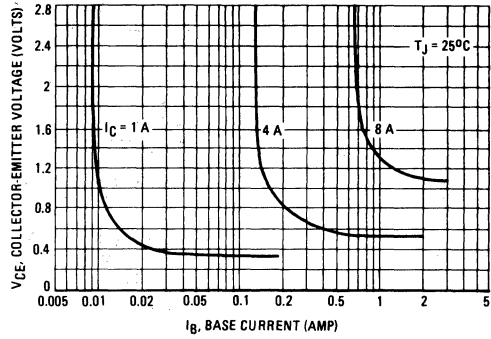


FIGURE 4 – "ON" VOLTAGES

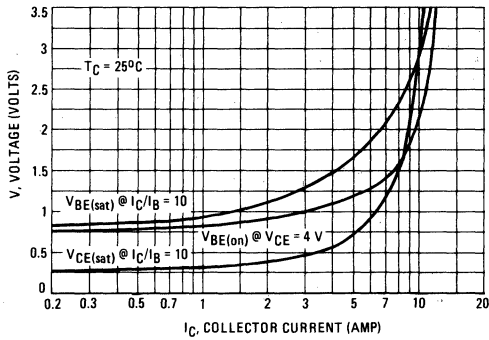


FIGURE 5 – CURRENT-GAIN-BANDWIDTH PRODUCT

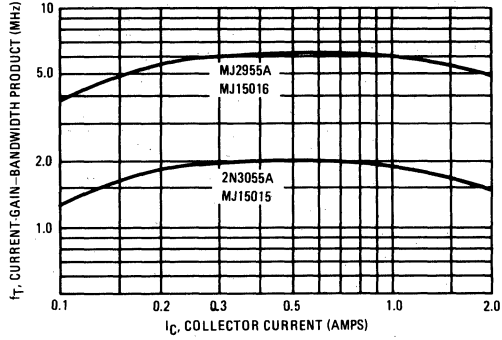


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT
 (Circuit shown is for NPN)

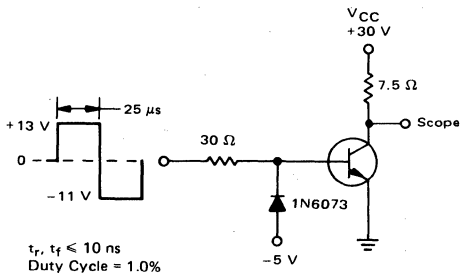
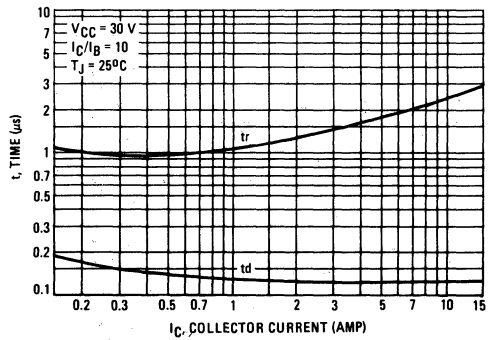


FIGURE 7 – TURN-ON TIME



NPN 2N3055A, MJ15015
PNP MJ2955A, MJ15016

FIGURE 8 – TURN-OFF TIMES

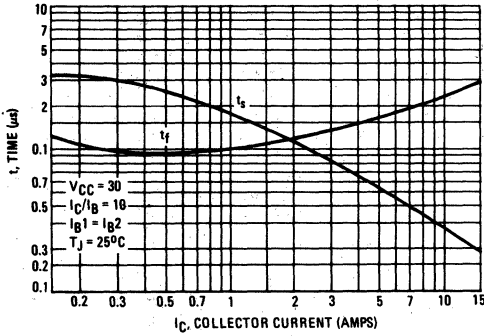
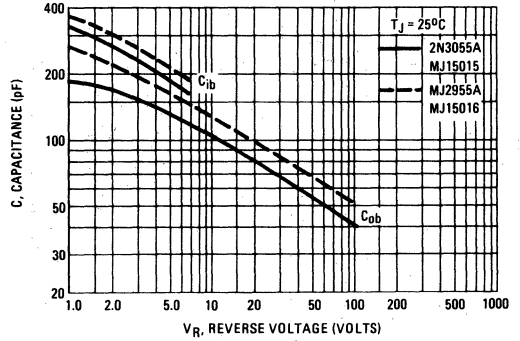
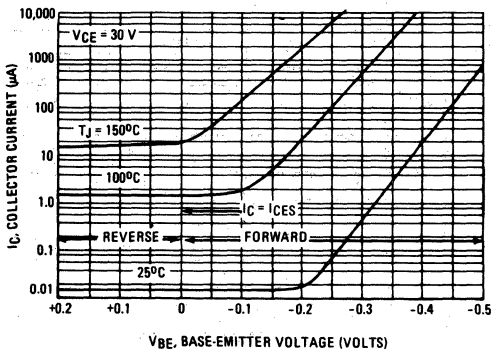


FIGURE 9 – CAPACITANCES



NPN
FIGURE 10 – 2N3055A, MJ15015



PNP
FIGURE 11 – MJ2955A, MJ15016

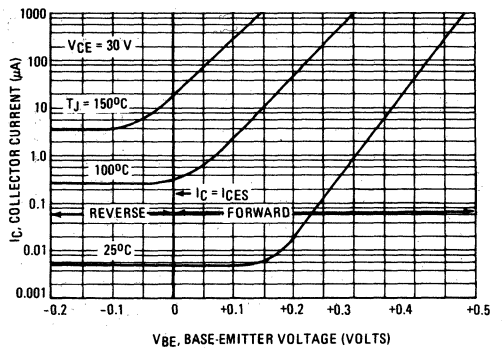


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA
2N3055A, MJ2955A

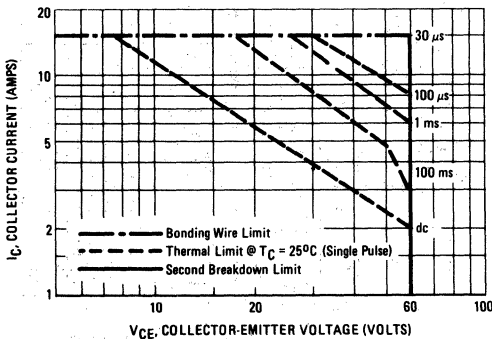
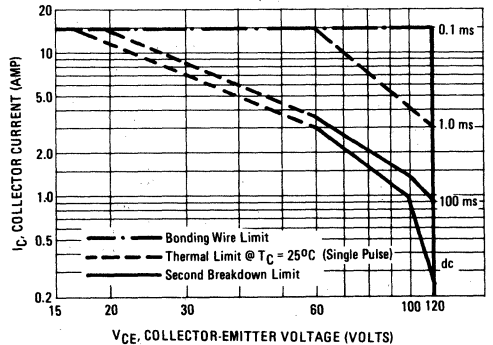


FIGURE 13 – FORWARD BIAS SAFE OPERATING AREA
MJ15015, MJ15016



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe Operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater

dissipation than the curves indicate.

The data of Figures 12 and 13 is based on $T_C = 25^\circ C$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

2N3441

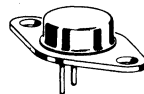
NPN SILICON POWER TRANSISTOR

... 2N3441 transistor is designed for use in general-purpose switching and linear amplifier applications requiring high breakdown voltages. It is characterized for use as:

- Driver for High Power Outputs
- Series and Shunt Regulators
- Audio and Servo Amplifiers
- Solenoid and Relay Drivers
- Power Switching Circuits

3 AMPERES
NPN SILICON
POWER TRANSISTOR

140 VOLTS
25 WATTS

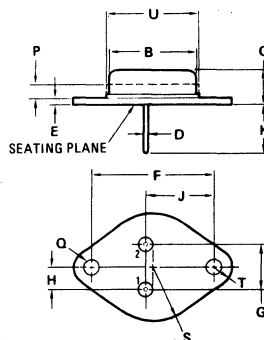


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CEO}	140	Vdc
Collector-Base Voltage	V _{CBO}	160	Vdc
Emitter-Base Voltage	V _{EBO}	7	Vdc
Collector Current — Continuous	I _C	3	Adc
Base Current — Continuous	I _B	2	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	25 0.142	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	7	°C/W



STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

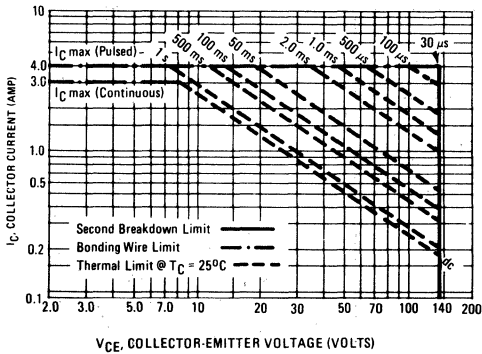
All JEDEC Dimensions and Notes Apply.

CASE 80-02
TO-213AA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 100\text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	140	—	Vdc
Collector Cutoff Current ($V_{CE} = 140\text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	100	mA
Collector Cutoff Current ($V_{CE} = 140\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ V}$) ($V_{CE} = 140\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ V}$ @ 150°C)	I_{CEX}	—	5.0 6.0	mA
Emitter Cutoff Current ($V_{BE} = 7.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	mA
ON CHARACTERISTICS				
DC Current Gain (1) ($I_C = 0.5\text{ Adc}$, $V_{CE} = 4.0\text{ V}$) ($I_C = 2.7\text{ Adc}$, $V_{CE} = 4.0\text{ V}$)	h_{FE}	25 5.0	100 —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 2.7\text{ Adc}$, $I_B = 0.9\text{ Adc}$)	$V_{CE(sat)}$	—	6.0	Vdc
Base-Emitter On Voltage (1) ($I_C = 2.7\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	$V_{BE(on)}$	—	6.7	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$, $f_{test} = 1\text{ kHz}$)	h_{fe}	15	75	—
Small-Signal Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$, $f_{test} = 0.4\text{ MHz}$)	$ h_{fe} $	5.0	—	—

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

2N3442
2N4347

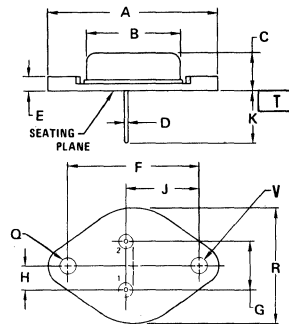
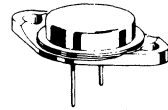
HIGH-POWER INDUSTRIAL TRANSISTORS

NPN silicon power transistors designed for applications in industrial and commercial equipment including high fidelity audio amplifiers, series and shunt regulators and power switches.

- Low Collector-Emitter Saturation Voltage –
V_{CE(sat)} = 1.0 Vdc (Max) @ I_C = 2.0 Adc – 2N4347
- Collector-Emitter Sustaining Voltage –
V_{CE0(sus)} = 120 Vdc (Min) – 2N4347
140 Vdc (Min) – 2N3442
- Excellent Second-Breakdown Capability

5.0 AND 10 AMPERE
POWER TRANSISTORS
NPN SILICON

120, 140 VOLTS
100, 117 WATTS



STYLE 1:

- PIN 1. BASE
- 2. EMITTER
- CASE: COLLECTOR

- DIAMETERS Q, V AND SURFACE T ARE DATUMS.
- POSITIONAL TOLERANCE FOR HOLE Q:
Ⓢ 0.25 (0.010) Ⓢ T | V Ⓢ
- POSITIONAL TOLERANCE FOR LEADS:
Ⓢ 0.30 (0.012) Ⓢ T | V Ⓢ Q Ⓢ
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	-	3.43	-	0.135
F	30.15	BSC	1.187	BSC
G	10.92	BSC	0.430	BSC
H	5.46	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	-	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

***MAXIMUM RATINGS**

Rating	Symbol	2N4347	2N3442	Unit
Collector-Emitter Voltage	V _{CE0}	120	140	Vdc
Collector-Base Voltage	V _{CB}	140	160	Vdc
Emitter-Base Voltage	V _{EB}	7.0		Vdc
Collector Current – Continuous Peak	I _C	5.0 10	10 15**	A dc
Base Current – Continuous Peak	I _B	3.0 8.0	7.0 -	A dc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	100 0.57	117 0.67	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N4347	2N3442	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.75	1.5	°C/W

*Indicates JEDEC Registered Data.
**This data guaranteed in addition to JEDEC registered data.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($I_C = 200 \text{ mAdc}$, $I_B = 0$)	2N4347 2N3442	$V_{CE(sus)}$	120 140	— —	Vdc
Collector Cutoff Current ($V_{CE} = 100 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 140 \text{ Vdc}$, $I_B = 0$)	2N4327 2N3422	I_{CEO}	— —	200 200	mAdc
Collector Cutoff Current ($V_{CE} = 125 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 140 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 120 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 140 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	2N4347 2N3442 2N4347 2N3442	I_{CEX}	— — — —	2.0 5.0 10 30	mAdc
Emitter Cutoff Current ($V_{BE} = 7.0 \text{ Vdc}$, $I_C = 0$)	2N4347, 2N3442	I_{EBO}	—	5.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 5.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 10 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	2N4347 2N4347 2N3442 2N3442	h_{FE}	15 10 20 7.5	60 — 70 —	—
Collector-Emitter Saturation Voltage ($I_C = 2.0 \text{ Adc}$, $I_B = 200 \text{ mAdc}$) ($I_C = 5.0 \text{ Adc}$, $I_B = 0.63 \text{ Adc}$) ($I_C = 10 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$)	2N4347 2N4347 2N3442	$V_{CE(sat)}$	— — —	1.0 2.0 5.0	Vdc
Base-Emitter On Voltage ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 5.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 10 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	2N4347 2N4347 2N3442	$V_{BE(on)}$	— — —	2.0 3.0 5.7	Vdc

DYNAMIC CHARACTERISTICS

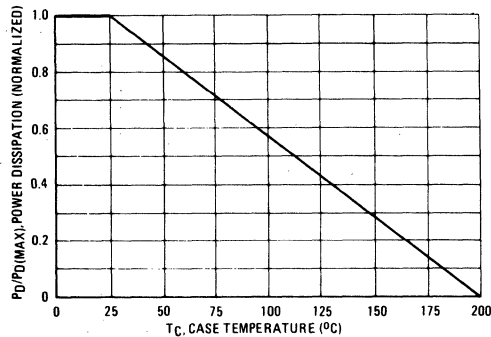
Current-Gain-Bandwidth Product (2) ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$, $f_{test} = 50 \text{ kHz}$) ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$, $f_{test} = 40 \text{ kHz}$)	2N4347 2N3442	f_T	200 80	— —	kHz
Small-Signal Current Gain ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$) ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	2N4347 2N3442	h_{fe}	40 12	— 72	—

*Indicates JEDEC Registered Data

NOTES: 1. Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.

2. $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 1 – POWER DERATING



ACTIVE REGION SAFE OPERATING AREA INFORMATION

FIGURE 2 - 2N3442

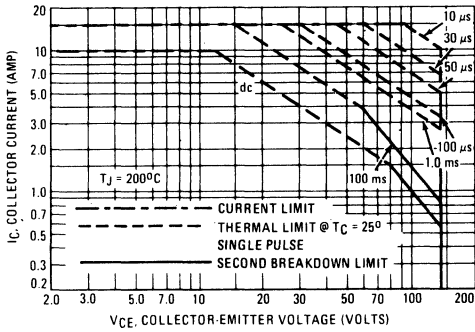


FIGURE 3 - 2N4347

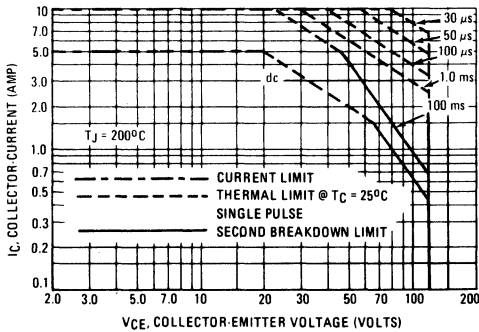


FIGURE 4 - DC CURRENT GAIN

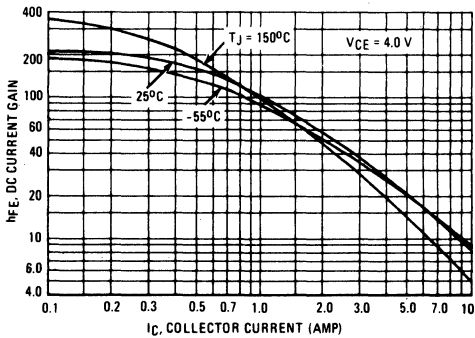
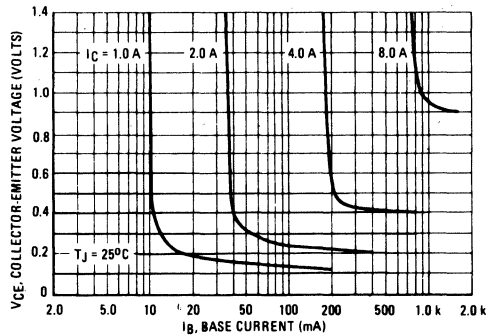


FIGURE 5 - COLLECTOR-SATURATION REGION



There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 and 3 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

2N3447
2N3448

**HIGH-SPEED SILICON ANNULAR
 NPN POWER TRANSISTORS**

... for switching and amplifier applications

FEATURES

- Fast Switching: Total Switching Time = 1.2 μ s (Typ) @ 5.0 A
- High Gain: h_{FE} = 40 to 120 @ 5.0 Amps
- Guaranteed DC Safe Area: 1.5 Amps (Min) @ V_{CE} = 40 Vdc
- Low $V_{CE(sat)}$: 1.0 Volt (Typ), 1.5 Volts (Max) @ 5.0 Amps
- Excellent Beta Linearity

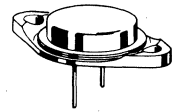
APPLICATIONS

- Specified safe area of this series allows reliable design for inverters, converters, hammer, and servo drivers.
- Fast response makes it ideal for series regulators; high switching speeds enhance its use in switching regulators.
- Wide bandwidth and flat beta hold-up result in exceptional amplifier characteristics.

7.5 AMPERE

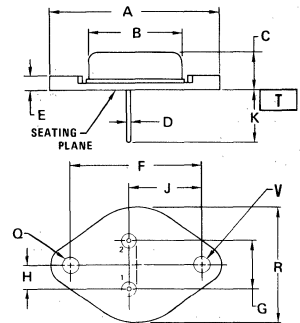
**POWER TRANSISTORS
 SILICON NPN**

**60-80 VOLTS
 115 WATTS**



MAXIMUM RATING

Rating	Symbol	2N3447	2N3448	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0	10	Vdc
Collector Current-Continuous	I_C		7.5	Adc
Base Current - Continuous	I_B		4.0	Adc
Total Device Dissipation	P_D	Figure 1, 2	Figure 1, 3	Watts
Operating Junction Temperature Range	T_J	-65 to +200		$^{\circ}$ C



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE: COLLECTOR

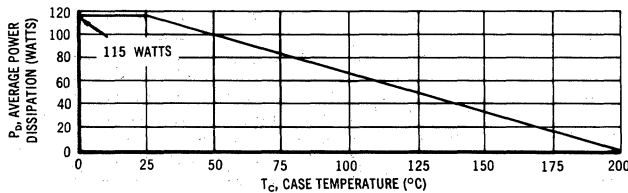
- NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
 2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\phi \pm 0.25 (0.010) \text{ @ } T | V \text{ @}$
 3. POSITIONAL TOLERANCE FOR LEADS:
 $\phi \pm 0.30 (0.012) \text{ @ } T | V \text{ @ } Q \text{ @}$
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050
V	3.84	4.09	0.151	0.161

**CASE 11-01
 TO-204AA**

3

FIGURE 1 - POWER DERATING CURVE



These transistors are also subject to safe area curves as indicated by Figures 2, 3. Both limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Emitter-Base Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$) ($V_{EB} = 10\text{ Vdc}$)	I_{EBO} 2N3447 2N3448	— —	— —	0.25 0.25	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 60\text{ Vdc}$, $V_{BE} = -1.0\text{ Vdc}$) ($V_{CE} = 60\text{ Vdc}$, $V_{BE} = -1.0\text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 80\text{ Vdc}$, $V_{BE} = -1.0\text{ Vdc}$) ($V_{CE} = 80\text{ Vdc}$, $V_{BE} = -1.0\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX} 2N3447 2N3447 2N3448 2N3448	— — — —	— — — —	0.1 1.0 0.1 1.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 40\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 60\text{ Vdc}$, $I_B = 0$)	I_{CEO} 2N3447 2N3448	— —	— —	1.0 1.0	mAdc
Collector-Base Breakdown Voltage ($I_C = 1.0\text{ mAdc}$, $I_E = 0$)	$V_{(BR)CBO}$ 2N3447 2N3448	80 100	— —	— —	Vdc
Collector-Emitter Sustaining Voltage ($I_C = 100\text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$ 2N3447 2N3448	60 80	— —	— —	Vdc
DC Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$) ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	40 40	85 75	— 120	—
Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.5\text{ Adc}$)	$V_{CE(sat)}$	—	0.8	1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.5\text{ Adc}$)	$V_{BE(sat)}$	—	1.0	1.5	Vdc
Base-Emitter Voltage ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	V_{BE}	—	1.0	1.4	Vdc
Small Signal Current Gain ($V_{CE} = 10\text{ Vdc}$, $I_C = 0.5\text{ Adc}$, $f = 1.0\text{ kHz}$) ($V_{CE} = 10\text{ Vdc}$, $I_C = 0.5\text{ Adc}$, $f = 10\text{ MHz}$)	h_{fe}	40 1.0	— 1.6	200 —	—
Common Base Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $f = 0.1\text{ MHz}$)	C_{ob}	—	260	400	pF
Switching Times ($V_{CC} = 25\text{ Vdc}$, $R_L = 5.0\text{ ohms}$, $I_C = 5.0\text{ A}$, $I_{B1} = I_{B2} = 0.5\text{ A}$)					μs
Delay Time plus Rise Time	$t_d + t_r$	—	0.15	0.35	
Storage Time	t_s	—	0.9	2.0	
Fall Time	t_f	—	0.15	0.35	

SAFE OPERATING AREAS

FIGURE 2 — 2N3447

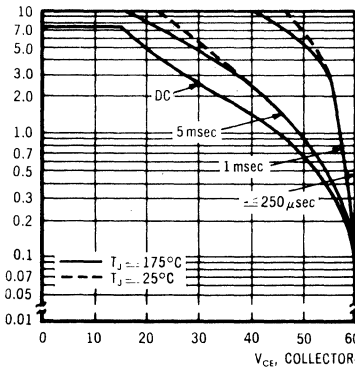
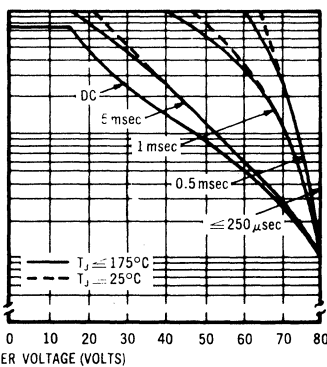


FIGURE 3 — 2N3448



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J , the power-temperature derating curve must be observed for both steady state and pulse power conditions.

NPN
2N3583 thru 2N3585
2N4240
PNP
2N6420 thru 2N6422

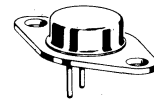
**COMPLEMENTARY MEDIUM-POWER HIGH VOLTAGE
 POWER TRANSISTORS**

... designed for high-speed switching and linear amplifier applications for high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

- Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 175 \text{ to } 300 \text{ Vdc @ } I_C = 200 \text{ mAdc}$
- Second Breakdown Collector Current –
 $I_{s/b} = 350 \text{ mAdc @ } V_{CE} = 100 \text{ Vdc - NPN}$
 $= 150 \text{ mAdc @ } V_{CE} = 100 \text{ Vdc - PNP}$
- Usable DC Current Gain to 2.0 Adc

**1.0 AND 2.0 AMPERE
 POWER TRANSISTORS
 COMPLEMENTARY SILICON**

**250-500 VOLTS
 35 WATTS**



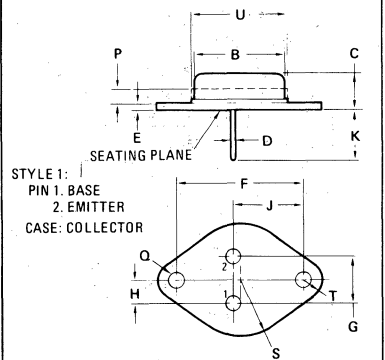
***MAXIMUM RATINGS**

Rating	Symbol	2N3583 2N6420	2N3584 2N6421	2N3585 2N6422	2N4240	Unit
Collector-Emitter Voltage	V_{CEO}	175	250	300	300	Vdc
Collector-Base Voltage	V_{CB}	250	375	500	500	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →				Vdc
Collector Current – Continuous – Peak (1)	I_C	1.0 5.0	← 2.0 → ← 5.0 →			Adc
Base Current	I_B	← 1.0 →				Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$, Derate above 25°C	P_D	← 35 → ← 0.2 →				Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →				$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.0	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data
 (1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle $\leq 10\%$.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

**CASE 80-02
 TO-213AA**

2N3583 thru 2N3585 • 2N4240 — NPN
2N6420 thru 2N6422 — PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	NPN	PNP	Symbol	NPN		PNP		Unit
				Min	Max	Min	Max	
*OFF CHARACTERISTICS (1)								
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$) NPN ($I_C = 50\text{ mA}$, $I_B = 0$) PNP	2N3583 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422	$V_{CE(sus)}$	175 250 300 300	— — — —	175 250 300 300	— — — —	Vdc
Collector Cutoff Current ($V_{CE} = 150\text{ Vdc}$, $I_B = 0$)	2N3583 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422	I_{CEO}	— — — —	10 5.0 5.0 5.0	— — — —	10 5.0 5.0 5.0	mAdc
Collector Cutoff Current ($V_{CE} = 225\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 340\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 450\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 225\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 300\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	2N3583 2N3584 2N3585 2N4240 2N3583 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422 2N6420 2N6421 2N6422	I_{CEX}	— — — — — — — —	1.0 1.0 1.0 2.0 3.0 3.0 3.0 5.0	— — — — — — — —	1.0 1.0 1.0 2.0 3.0 3.0 3.0 5.0	mAdc
Emitter Cutoff Current ($V_{BE} = 6.0\text{ Vdc}$, $I_C = 0$)	2N3583 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422	I_{EBO}	— — — —	5.0 0.5 0.5 0.5	— — — —	5.0 0.5 0.5 0.5	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 0.1\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$) * ($I_C = 0.5\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$) * ($I_C = 0.75\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$) ($I_C = 0.75\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$) * ($I_C = 1.0\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$) ($I_C = 1.0\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$)	All	All	h_{FE}	40	—	40	—	—
	2N3583	2N6420		40	200	40	200	
	2N4240			10	100	10	100	
	2N4240			30	150	30	150	
	2N3584	2N6421		8.0	80	8.0	80	
	2N3585	2N6422		8.0	80	8.0	80	
	2N3583*	2N6420		10	—	10	—	
	2N3584	2N6421		25	100	25	100	
2N3585	2N6422	25	100	25	100			
*Collector-Emitter Saturation Voltage ($I_C = 0.75\text{ Adc}$, $I_B = 75\text{ mA}$) ($I_C = 1.0\text{ Adc}$, $I_B = 125\text{ mA}$)	2N4240 2N3583 2N3584 2N3585	2N6420 2N6421 2N6422	$V_{CE(sat)}$	— — — —	1.0 5.0 0.75 0.75	— — — —	1.0 5.0 0.75 0.75	Vdc
*Base-Emitter Saturation Voltage ($I_C = 0.75\text{ Adc}$, $I_B = 75\text{ mA}$) ($I_C = 1.0\text{ Adc}$, $I_B = 100\text{ mA}$)	2N4240 2N3584 2N3585	2N6421 2N6422	$V_{BE(sat)}$	— — —	1.8 1.4 1.4	— — —	1.8 1.4 1.4	Vdc
Base-Emitter On Voltage ($I_C = 1.0\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$)	All	All	$V_{BE(on)}$	—	1.4	—	1.4	Vdc

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

2N3583 thru 2N3585 • 2N4240 — NPN
2N6420 thru 2N6422 — PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

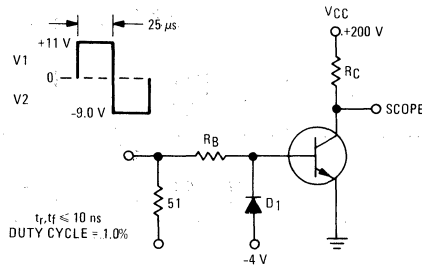
Characteristic	NPN	PNP	Symbol	NPN		PNP		Unit
				Min	Max	Min	Max	
DYNAMIC CHARACTERISTICS								
*Current Gain — Bandwidth Product ⁽¹⁾ ($I_C = 200 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{\text{test}} = 5.0 \text{ MHz}$)	2N3583 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422	f_T	10 15	—	10 15	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	All		C_{ob}	—	120	—	120	pF
*Small-Signal Current Gain ($I_C = 100 \text{ mAdc}$, $V_{CE} = 30 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	2N3583	2N6420	h_{fe}	25	350	25	350	—
*SWITCHING CHARACTERISTICS								
Rise Time ($V_{CC} = 200 \text{ Vdc}$, $I_C = 1.0 \text{ Adc}$, $R_L = 200 \text{ Ohms}$, $I_{B1} = 100 \text{ mAdc}$) ($V_{CC} = 200 \text{ Vdc}$, $I_C = 0.75 \text{ Adc}$, $R_L = 267 \text{ Ohms}$, $I_{B1} = 75 \text{ mAdc}$)	2N3584 2N3585 2N4240	2N6421 2N6422	t_r	—	3.0 0.5	—	3.0 0.5	μs
Storage Time ($V_{CC} = 200 \text{ Vdc}$, $I_C = 1.0 \text{ Adc}$, $I_{B1} = I_{B2} = 100 \text{ mAdc}$) ($V_{CC} = 200 \text{ Vdc}$, $I_C = 0.75 \text{ Adc}$, $I_{B1} = I_{B2} = 75 \text{ mAdc}$)	2N3584 2N3585 2N4240	2N6421 2N6422	t_s	—	4.0 6.0	—	4.0 6.0	μs
Fall Time ($V_{CC} = 200 \text{ Vdc}$, $I_C = 1.0 \text{ Adc}$, $I_{B1} = I_{B2} = 100 \text{ mAdc}$) ($V_{CC} = 200 \text{ Vdc}$, $I_C = 0.75 \text{ Adc}$, $I_{B1} = I_{B2} = 75 \text{ mAdc}$)	2N3584 2N3585 2N4240	2N6421 2N6422	t_f	—	3.0 3.0	—	3.0 3.0	μs
Second Breakdown Collector Current ($V_{CE} = 100 \text{ Vdc}$)	All	All	$I_{s/b}$	350	—	150	—	mAdc

*Indicates JEDEC Registered Data

(1) $f_T = |h_{fe}| \cdot f_{\text{test}}$

3

FIGURE 1 — SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg:

MB05300 USED ABOVE $I_B \approx 100 \text{ mA}$

MSD6100 USED BELOW $I_B \approx 100 \text{ mA}$

FOR t_d and t_r , D1 IS DISCONNECTED AND $V_2 = 0$.

FOR PNP TEST CIRCUIT, REVERSE DIODE AND VOLTAGE POLARITIES.

2N3583 thru 2N3585 • 2N4240 — NPN
2N6420 thru 2N6422 — PNP

NPN
2N3583 thru 2N3585, 2N4240

PNP
2N6420 thru 2N6422

FIGURE 2 — TURN-ON TIME

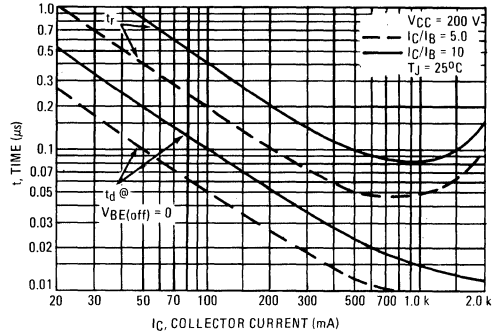
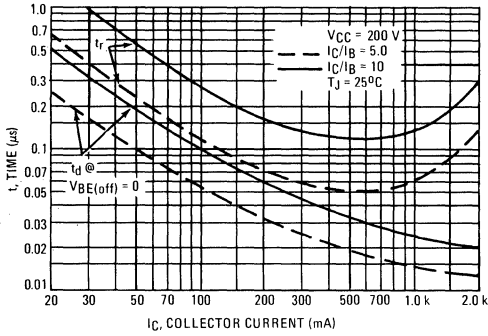


FIGURE 3 — TURN-OFF TIME

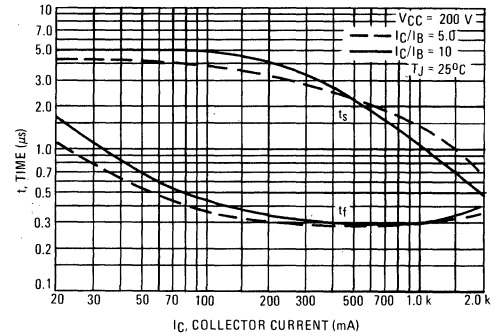
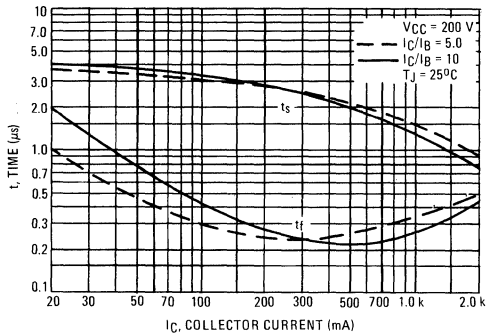


FIGURE 4 — CURRENT-GAIN — BANDWIDTH PRODUCT

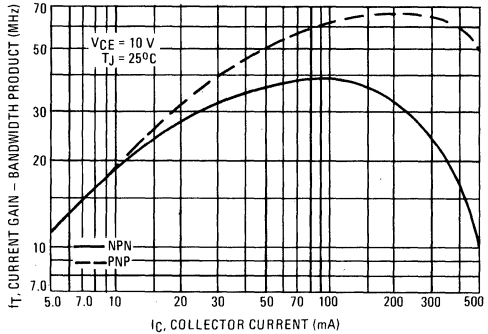
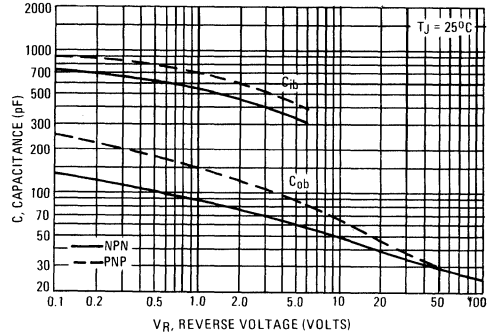
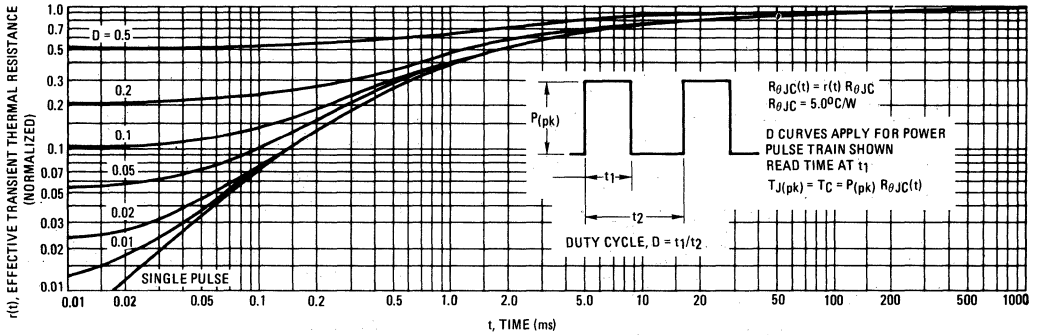


FIGURE 5 — CAPACITANCE



2N3583 thru 2N3585 • 2N4240 — NPN
2N6420 thru 2N6422 — PNP

FIGURE 6 — THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 7 — 2N3583 thru 2N3585, 2N4240

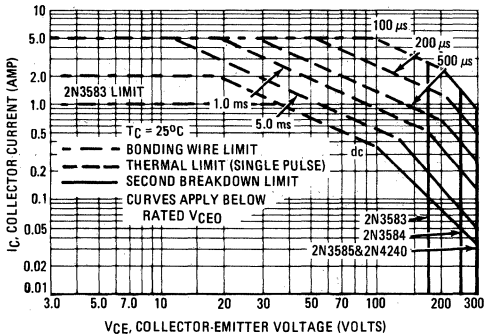


FIGURE 8 — 2N6420 thru 2N6422

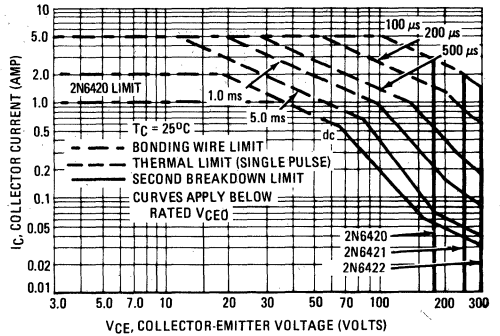
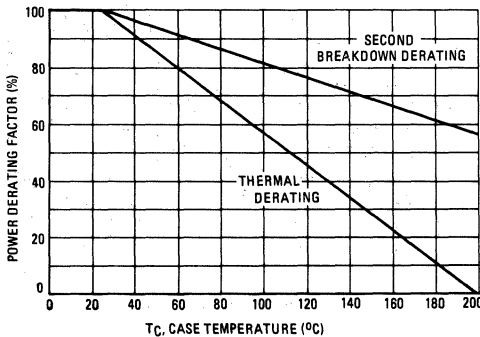


FIGURE 9 — POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 7 and 8 is based on $T_C = 25^{\circ}\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 9.

$T_J(pk)$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 7 and 8 may be found at any case temperature by using the appropriate curve on Figure 9.

2N3583 thru 2N3585 • 2N4240 — NPN
2N6420 thru 2N6422 — PNP

NPN
2N3583 thru 2N3585, 2N4240

PNP
2N6420 thru 2N6422

FIGURE 10 — DC CURRENT GAIN

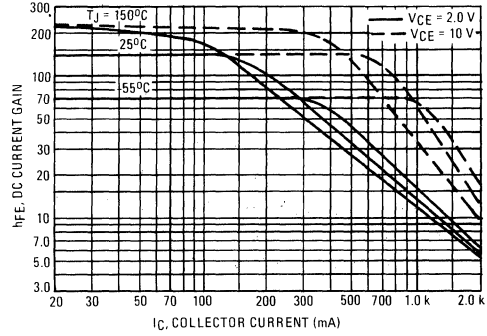
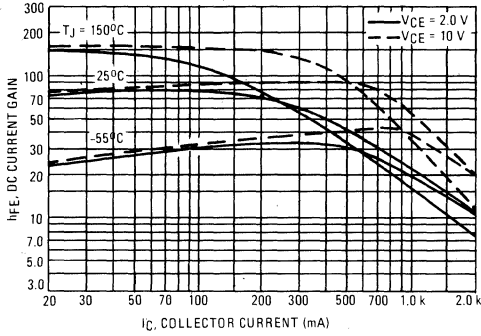


FIGURE 11 — COLLECTOR SATURATION REGION

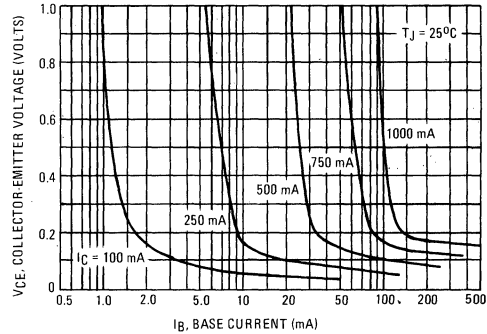
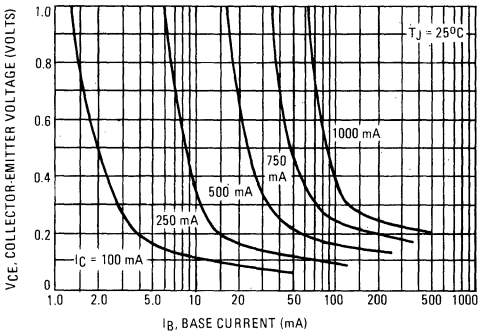
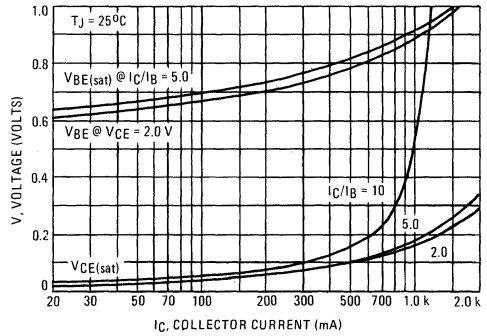
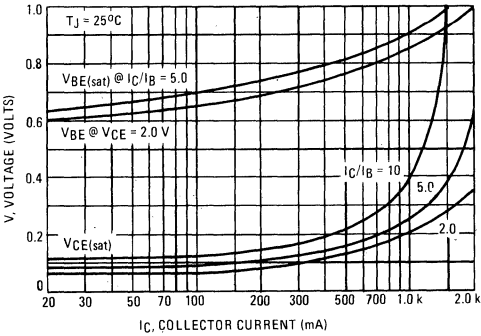


FIGURE 12 — "ON" VOLTAGES



NOTE: DC CURRENT LIMIT FOR 2N3583, 2N6420 is 1.0 Amp.



SILICON NPN POWER TRANSISTORS

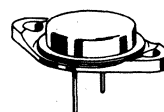
... designed for medium-speed switching and amplifier applications.
These devices feature:

- Total Switching Time at 3 A typically 1.15 μ s
- Gain Ranges Specified at 1 A and 3 A
- Low $V_{CE(sat)}$: typically 0.5V at $I_C = 5A$ and $I_B = 0.5A$
- Excellent Safe Operating Areas
- Complement to 2N3789-92

10 AMPERE

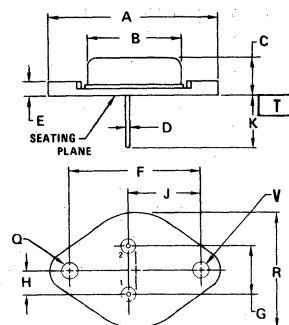
POWER TRANSISTORS
SILICON NPN

60-80 VOLTS
150 WATTS



MAXIMUM RATINGS

Rating	Symbol	2N3715	2N3714 2N3716	Unit
Collector-Base Voltage	V_{CB}	80	100	Volts
Collector-Emitter Voltage	V_{CEO}	60	80	Volts
Emitter-Base Voltage	V_{EB}	7.0	7.0	Volts
Collector Current	I_C	10	10	Amps
Base Current	I_B	4.0	4.0	Amps
Power Dissipation	P_D	150	150	Watts
Thermal Resistance	θ_{JC}	1.17	1.17	$^{\circ}C/W$
Operating Junction and Storage Temperature Range	T_J and T_{stg}	-65 to +200		$^{\circ}C$



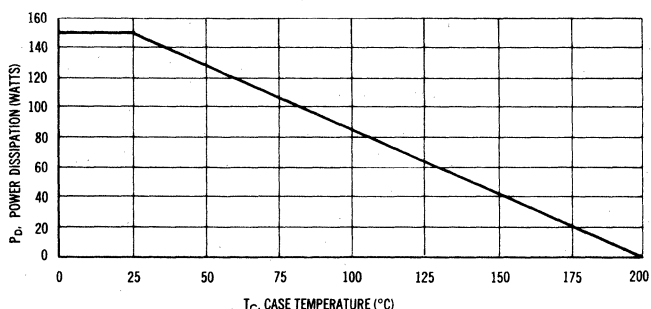
STYLE 1:

- PIN 1: BASE
2: EMITTER
CASE: COLLECTOR

NOTES:

1. DIAMETERS Q, V, AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\phi \pm 0.25 (0.010) \text{ } \textcircled{T} \text{ } \textcircled{V} \text{ } \textcircled{Q}$
3. POSITIONAL TOLERANCE FOR LEADS:
 $\phi \pm 0.30 (0.012) \text{ } \textcircled{T} \text{ } \textcircled{V} \text{ } \textcircled{Q} \text{ } \textcircled{Q}$
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Limits are indicated by Figures 12, 13. Both limits are applicable and must be observed.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	30.15	BSC	1.187	BSC
G	10.92	BSC	0.430	BSC
H	5.46	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

2N3714 thru 2N3716 NPN

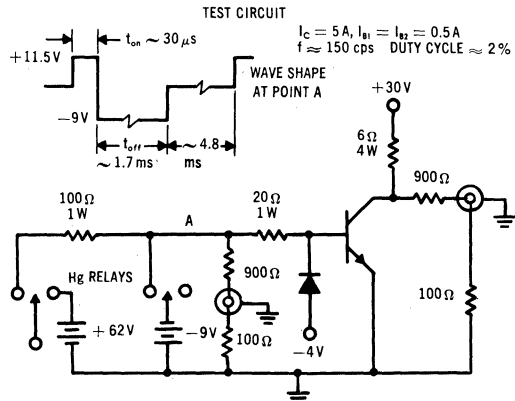
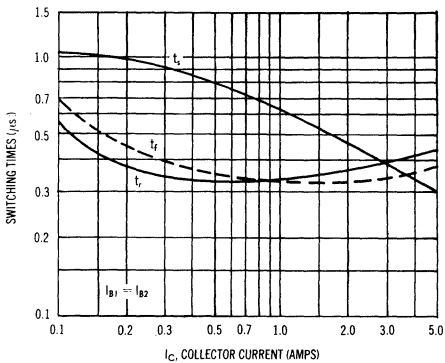
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Emitter-Base Cutoff Current (V _{EB} = 7 Vdc)	I _{EBO}	—	5	mAdc
Collector-Emitter Cutoff Current (V _{CE} = 80 Vdc, V _{BE} = -1.5 Vdc) (V _{CE} = 100 Vdc, V _{BE} = -1.5 Vdc) (V _{CE} = 60 Vdc, V _{BE} = -1.5 Vdc, T _C = 150°C) (V _{CE} = 80 Vdc, V _{BE} = -1.5 Vdc, T _C = 150°C)	I _{CEX}	— — — —	1 1 10 10	mAdc
Collector-Emitter Sustaining Voltage* (I _C = 200 mAdc, I _B = 0)	V _{CEO(sus)} *	60 80	— —	Vdc
DC Current Gain* (I _C = 1 Adc, V _{CE} = 2 Vdc) (I _C = 3 Adc, V _{CE} = 2 Vdc)	h _{FE} *	25 50 15 30	90 150 — —	—
Collector-Emitter Saturation Voltage* (I _C = 5 Adc, I _B = 0.5 Adc)	V _{CE(sat)} *	— —	1.0 0.8	Vdc
Base-Emitter Saturation Voltage* (I _C = 5 Adc, I _B = 0.5 Adc)	V _{BE(sat)} *	— —	2.0 1.5	Vdc
Base-Emitter Voltage* (I _C = 3 Adc, V _{CE} = 2 Vdc)	V _{BE} *	—	1.5	Vdc
Small Signal Current Gain (V _{CE} = 10 Vdc, I _C = 0.5 Adc, f = 1 MHz)	h _{fe}	4	—	—
Switching Times (Figure 2) (I _C = 5 A, I _{B1} = I _{B2} = 0.5 Adc)			Typ	μs
Rise Time	t _r		0.45	
Storage Time	t _s		0.3	
Fall Time	t _f		0.4	

*Use sweep test to prevent overheating

3

FIGURE 2 — TYPICAL SWITCHING TIMES



2N3714 thru 2N3716 NPN

FIGURE 3 – COLLECTOR CURRENT versus BASE CURRENT

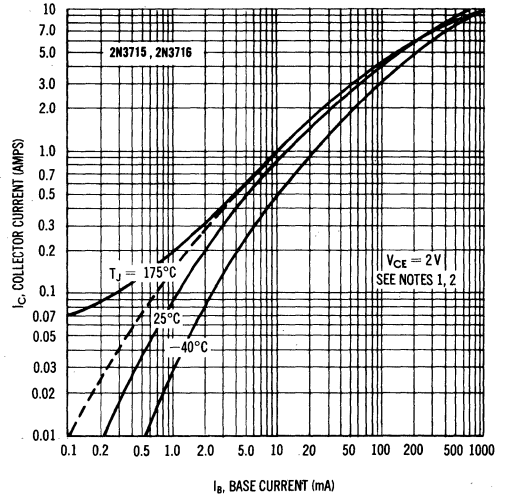
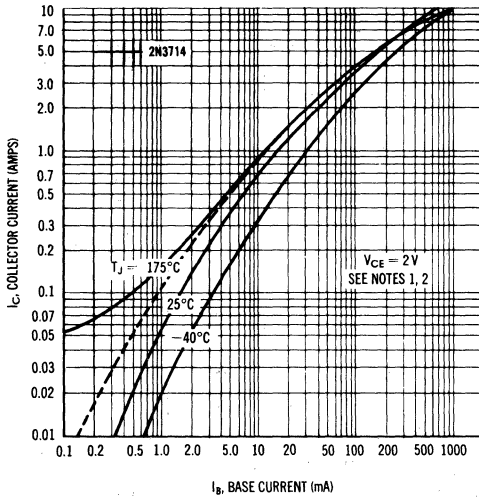


FIGURE 4 – BASE CURRENT-VOLTAGE VARIATIONS

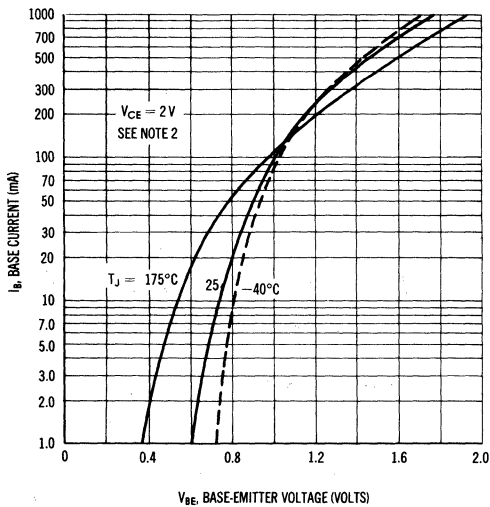
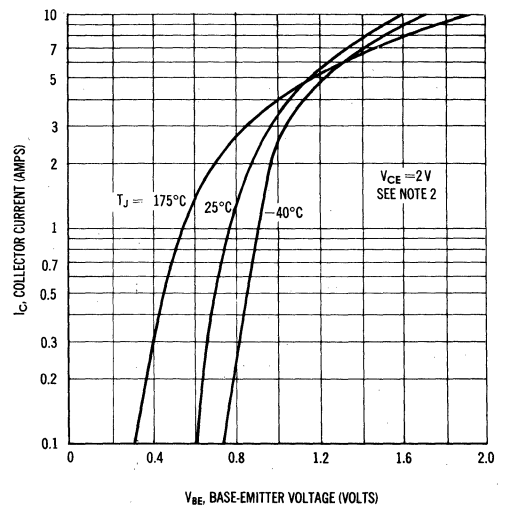


FIGURE 5 – COLLECTOR CURRENT-VOLTAGE VARIATIONS



NOTE 1. Dotted line indicates metered base current plus the I_{CBO} of the transistor at 175°C .

NOTE 2. Pulse test: pulse width $\approx 200 \mu\text{sec}$, duty cycle $\approx 1.5\%$

3

2N3714 thru 2N3716 NPN

FIGURE 6 – COLLECTOR-EMITTER SATURATION VOLTAGE VARIATIONS

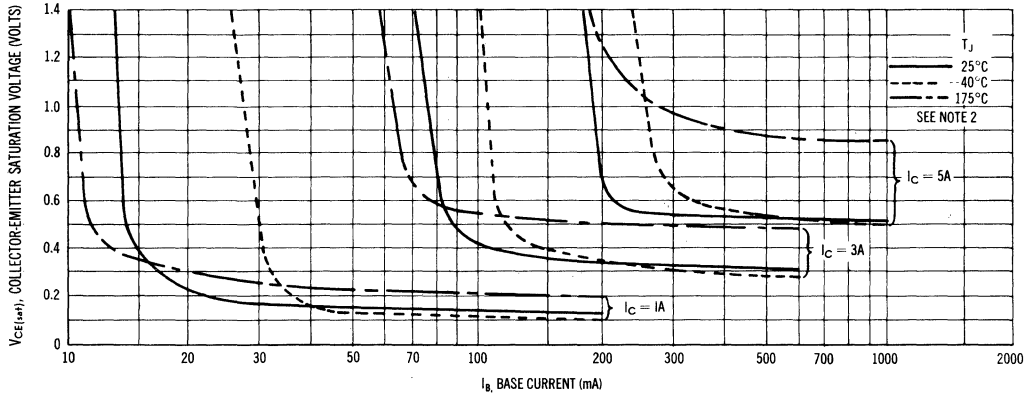


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE VARIATIONS

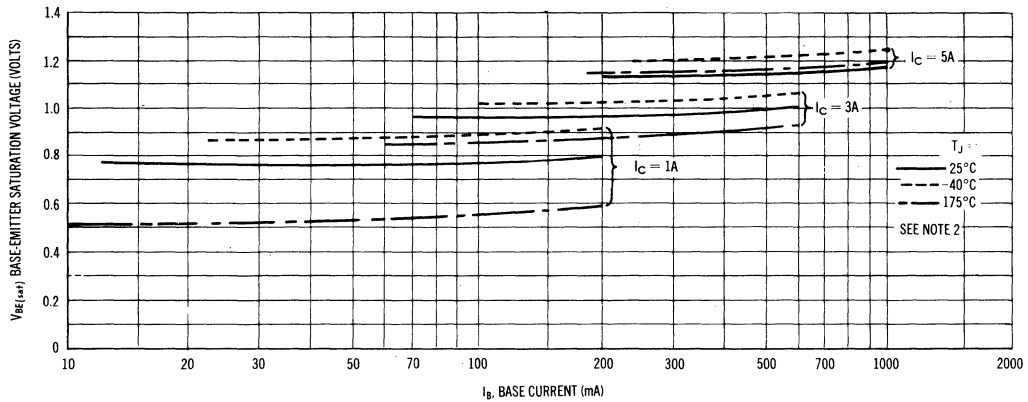


FIGURE 8 – COLLECTOR CURRENT versus BASE-EMITTER VOLTAGE

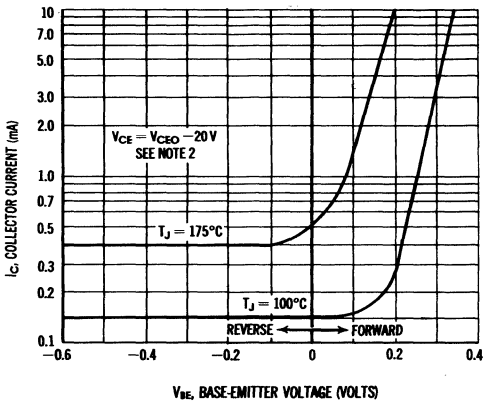
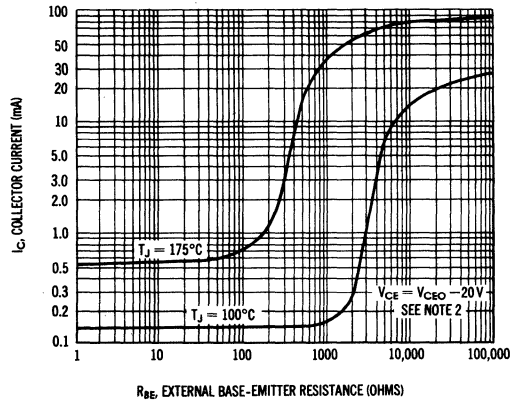


FIGURE 9 – COLLECTOR CURRENT versus BASE-EMITTER RESISTANCE



2N3714 thru 2N3716 NPN

FIGURE 10 - CURRENT GAIN VARIATIONS

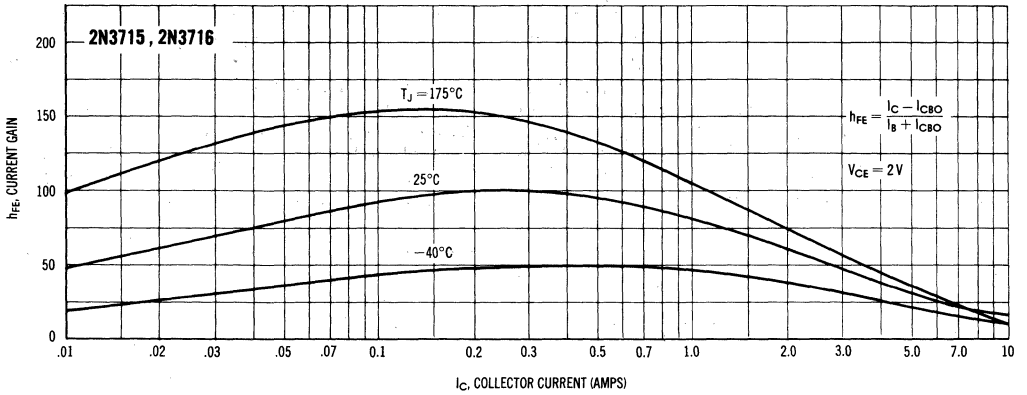
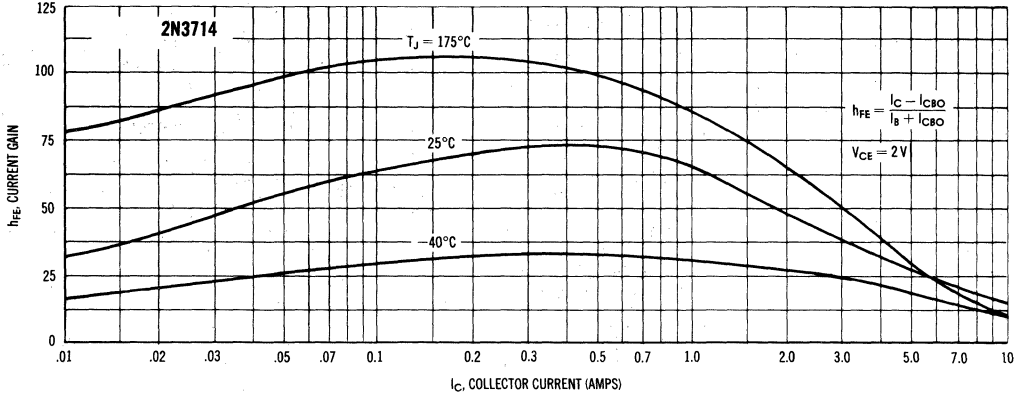
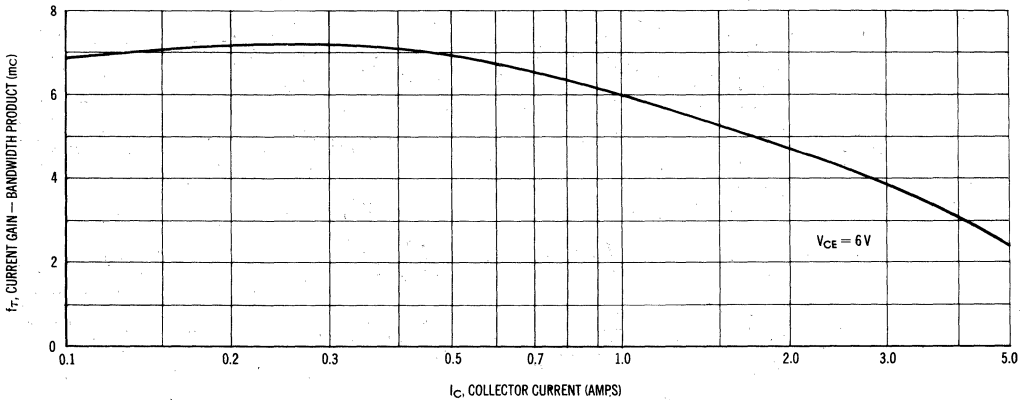


FIGURE 11 - CURRENT GAIN - BANDWIDTH PRODUCT versus COLLECTOR CURRENT



3

2N3714 thru 2N3716 NPN

SAFE OPERATING AREAS

FIGURE 12 - 2N3715

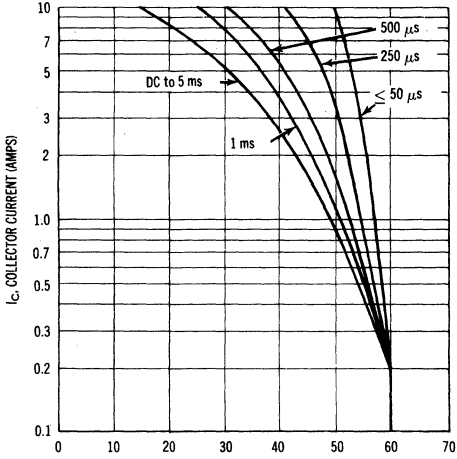
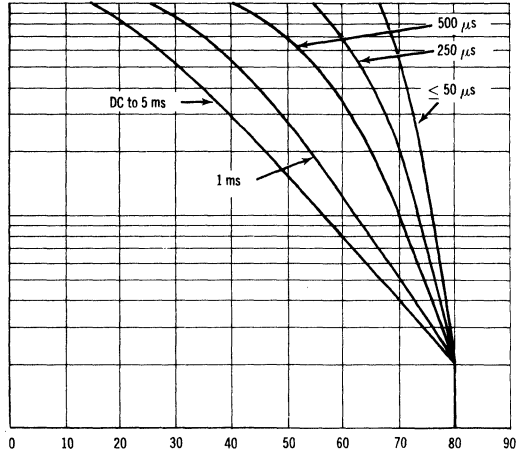


FIGURE 13 - 2N3714, 2N3716



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no signifi-

cant change in these safe areas.) To insure operation below the maximum T_J , the power-temperature derating curve must be observed for both steady state and pulse power conditions.

2N3719, 2N3720
2N3867, 2N3868
2N6303

SILICON PNP POWER TRANSISTORS

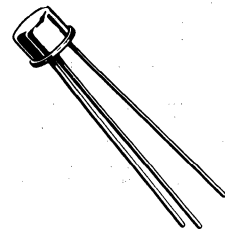
... designed for high-speed, medium-current switching and high-frequency amplifier applications.

- Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 40 \text{ Vdc (Min)} - 2N3719, 2N3867$
 $= 60 \text{ Vdc (Min)} - 2N3720, 2N3868$
 $= 80 \text{ Vdc (Min)} - 2N6303$
- DC Current Gain –
 $h_{FE} = 25-180 @ I_C = 1.0 \text{ Adc} - 2N3719, 2N3720$
 $= 40-200 @ I_C = 1.5 \text{ Adc} - 2N3867$
 $= 30-150 @ I_C = 1.5 \text{ Adc} - 2N3868, 2N6303$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.75 \text{ Vdc} @ I_C = 1.0 \text{ Adc} - 2N3719, 2N3720$
 $= 0.75 \text{ Vdc} @ I_C = 1.5 \text{ Adc} - 2N3867, 2N3868,$
 $2N6303$
- High Current-Gain – Bandwidth Product –
 $f_T = 90 \text{ MHz (Typ)}$
- 2N3867 JAN and 2N3868 JAN also Available

3 AMPERE

POWER TRANSISTORS
PNP SILICON

40,60,80 VOLTS
6 WATTS



***MAXIMUM RATINGS**

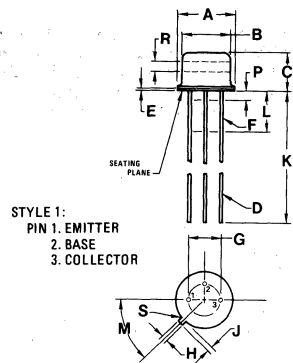
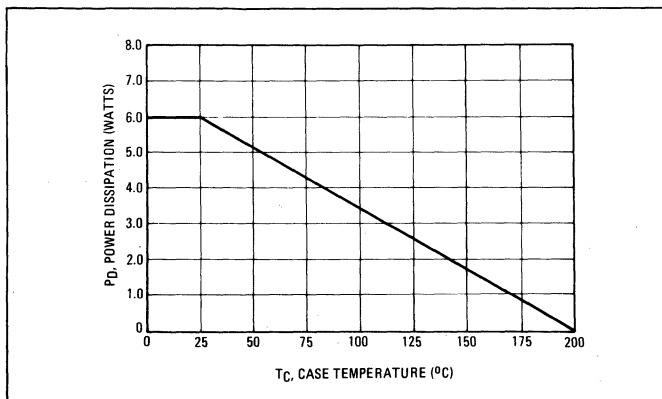
Rating	Symbol	2N3719 2N3867	2N3720 2N3868	2N6303	Unit
Collector-Emitter Voltage	V_{CE}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0			Vdc
Collector Current – Continuous	I_C	3.0			Adc
Peak		1.0			
Base Current	I_B	0.5			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	6.0			Watts
Derate above 25°C		34.3			mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.0			Watt
Derate above 25°C		5.71			mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_{J,Tstg}$	-65 to +200			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	29	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	175	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING



STYLE 1:
 PIN 1. EMITTER
 2. BASE
 3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	6.10	6.80	0.240	0.280
D	0.406	0.533	0.016	0.021
E	0.229	0.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.711	0.864	0.028	0.034
J	0.734	1.14	0.029	0.045
K	38.10	44.45	1.500	1.750
L	6.35		0.250	
M	45° BSC		45° BSC	
N				
P		1.27		0.050
R	2.54		0.100	
S		0.25		0.010

All JEDEC dimensions and notes apply.

CASE 31-03
TO-205AA

2N3719, 2N3720, 2N3867, 2N3868, 2N6303

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 20 mA _{dc} , I _B = 0)	V _{CEO(sus)}	40 60 80	—	V _{dc}
Collector-Base Breakdown Voltage (I _C = 100 μA _{dc} , I _E = 0)	V _{(BR)CBO}	40 60 80	—	V _{dc}
Emitter-Base Breakdown Voltage (I _E = 100 μA _{dc} , I _C = 0)	V _{(BR)EBO}	4.0	—	V _{dc}
Collector Cutoff Current (V _{CE} = Rated V _{CB} , V _{BE(off)} = 2.0 V _{dc})	I _{CEX}	—	1.0	μA _{dc}
Collector Cutoff Current (V _{CB} = Rated V _{CB} , I _E = 0, T _C = 150°C)	I _{CBO}	—	150	μA _{dc}
ON CHARACTERISTICS (1)				
DC Current Gain (I _C = 500 mA _{dc} , V _{CE} = 1.0 V _{dc})	h _{FE}	50 35	—	—
(I _C = 1.5 A _{dc} , V _{CE} = 2.0 V _{dc})		40 30	200 150	
(I _C = 2.5 A _{dc} , V _{CE} = 3.0 V _{dc})		25 20	—	
(I _C = 3.0 A _{dc} , V _{CE} = 5.0 V _{dc})		20	—	
Collector-Emitter Saturation Voltage (I _C = 500 mA _{dc} , I _B = 50 mA _{dc}) (I _C = 1.5 A _{dc} , I _B = 150 mA _{dc}) (I _C = 2.5 A _{dc} , I _B = 250 mA _{dc})	V _{CE(sat)}	—	0.5 0.75 1.3	V _{dc}
Base-Emitter Saturation Voltage (I _C = 500 mA _{dc} , I _B = 50 mA _{dc}) (I _C = 1.5 A _{dc} , I _B = 150 mA _{dc}) (I _C = 2.5 A _{dc} , I _B = 250 mA _{dc})	V _{BE(sat)}	— 0.9 —	1.0 1.4 2.0	V _{dc}
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (2) (I _C = 100 mA _{dc} , V _{CE} = 5.0 V _{dc} , f _{test} = 20 MHz)	f _T	60	—	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 0.1 MHz)	C _{ob}	—	120	pF
Input Capacitance (V _{EB} = 3.0 V _{dc} , I _C = 0, f = 0.1 MHz)	C _{ib}	—	1000	pF
SWITCHING CHARACTERISTICS				
Delay Time (V _{CC} = 30 V _{dc} , V _{BE(off)} = 0, I _C = 1.5 A _{dc} , I _{B1} = 150 mA _{dc})	t _d	—	35	ns
Rise Time	t _r	—	65	ns
Storage Time (V _{CC} = 30 V _{dc} , I _C = 1.5 A _{dc} , I _{B1} = I _{B2} = 150 mA _{dc})	t _s	—	325	ns
Fall Time	t _f	—	75	ns

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) f_T = |h_{fe}| • f_{test}.

2N3719, 2N3720, 2N3867, 2N3868, 2N6303

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 20 mA, I _B = 0)	V _{CEO(sus)}	40 60	—	Vdc
Collector Cutoff Current (V _{CE} = 40 Vdc, V _{BE(off)} = 2.0 Vdc)	I _{CEx}	—	10	μA
(V _{CE} = 60 Vdc, V _{BE(off)} = 2.0 Vdc)		—	10	
(V _{CE} = 40 Vdc, V _{BE(off)} = 2.0 Vdc, T _C = 150°C)		—	1.0	mA
(V _{CE} = 60 Vdc, V _{BE(off)} = 2.0 Vdc, T _C = 150°C)		—	1.0	
Collector Cutoff Current (V _{CB} = 40 Vdc, I _E = 0)	I _{CBO}	—	10	μA
(V _{CB} = 60 Vdc, I _E = 0)		—	10	
Emitter Cutoff Current (V _{BE} = 4.0 Vdc, I _C = 0)	I _{EBO}	—	1.0	mA

ON CHARACTERISTICS (1)				
DC Current Gain (I _C = 500 mA, V _{CE} = 1.5 Vdc)	h _{FE}	20	—	
(I _C = 1.0 A, V _{CE} = 1.5 Vdc)		25	180	
(I _C = 1.0 A, V _{CE} = 1.5 Vdc, T _C = -40°C)		15	—	
Collector-Emitter Saturation Voltage (I _C = 1.0 A, I _B = 100 mA, T _C = -40°C to +100°C)	V _{CE(sat)}	—	0.75	Vdc
(I _C = 3.0 A, I _B = 300 mA, T _C = -40°C to +100°C)		—	1.5	
Base-Emitter Saturation Voltage (I _C = 1.0 A, I _B = 100 mA, T _C = -40°C to +100°C)	V _{BE(sat)}	—	1.5	Vdc
(I _C = 3.0 A, I _B = 300 mA, T _C = -40°C to +100°C)		—	2.3	

DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (2) (I _C = 500 mA, V _{CE} = 10 Vdc, f _{test} = 30 MHz)	f _T	60	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	—	120	pF
Input Capacitance (V _{EB} = 0.5 Vdc, I _C = 0, f = 0.1 MHz)	C _{ib}	—	1000	pF

SWITCHING CHARACTERISTICS				
Turn-On Time (V _{CC} = 12 Vdc, V _{BE(off)} = 0, I _C = 1.0 A, I _{B1} = 0.1 A)	t _{on}	—	100	ns
Turn-Off Time (V _{CC} = 12 Vdc, I _C = 1.0 A, I _{B1} = I _{B2} = 100 mA)	t _{off}	—	400	ns

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%. (2) f_T = |h_{fe}| • f_{test}

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

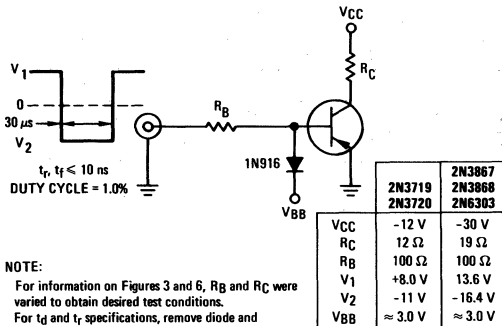


FIGURE 3 – TURN-ON TIME

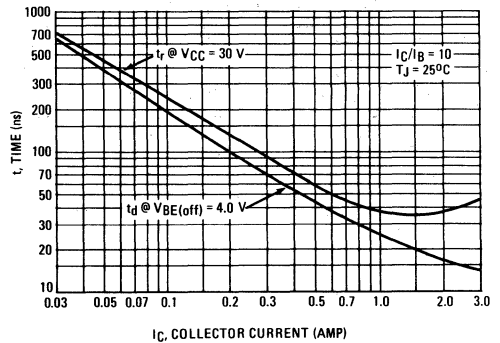


FIGURE 4 – THERMAL RESISTANCE

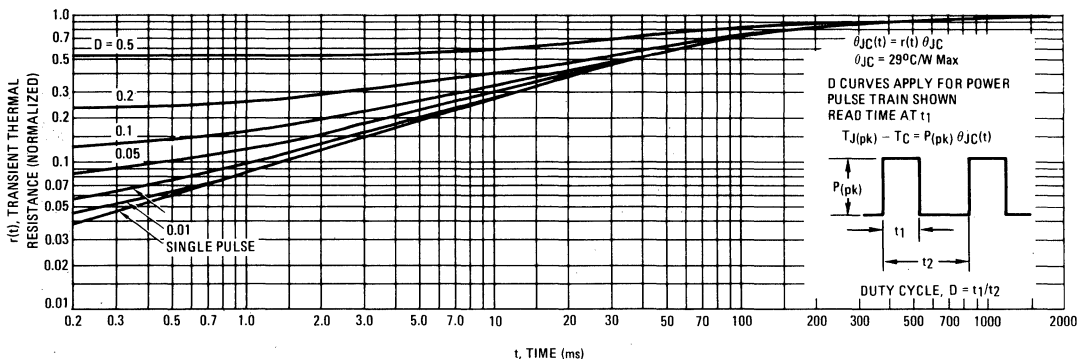
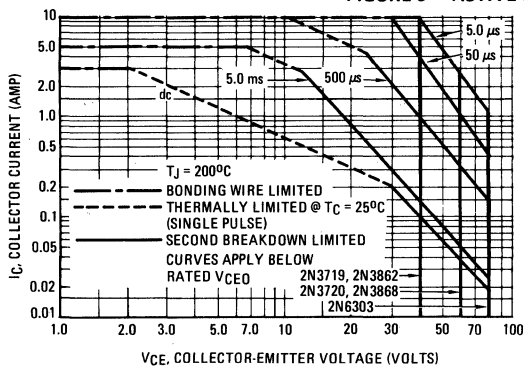


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

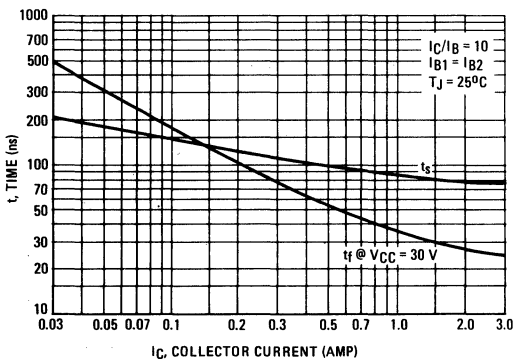


FIGURE 7 – CAPACITANCE

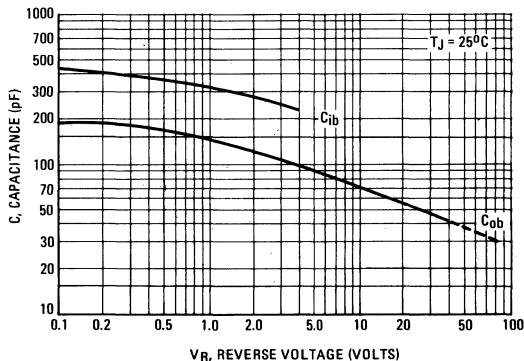


FIGURE 8 – DC CURRENT GAIN

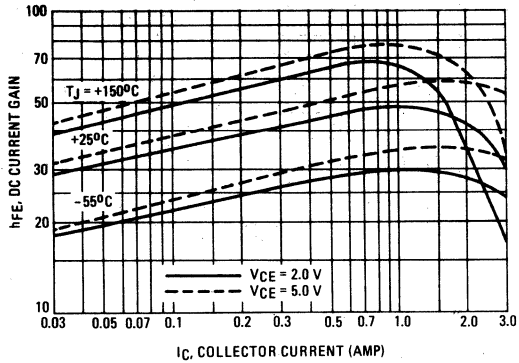


FIGURE 9 – COLLECTOR SATURATION REGION

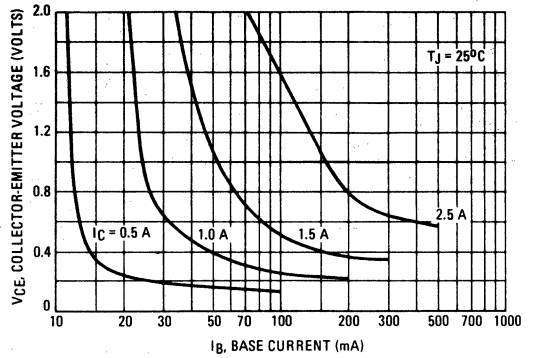


FIGURE 10 – "ON" VOLTAGES

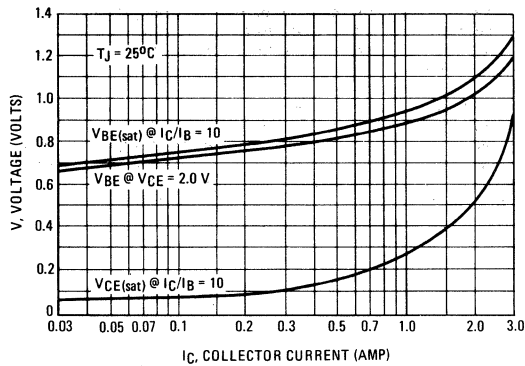
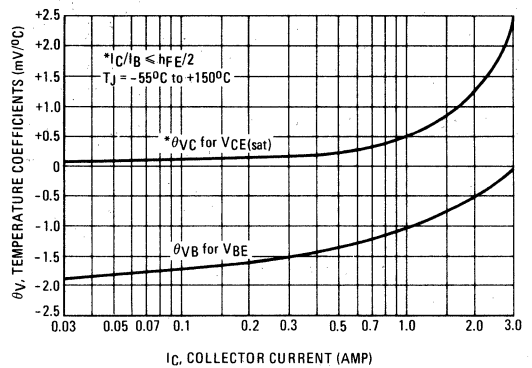


FIGURE 11 – TEMPERATURE COEFFICIENTS



3

FIGURE 12 – COLLECTOR CUT-OFF REGION

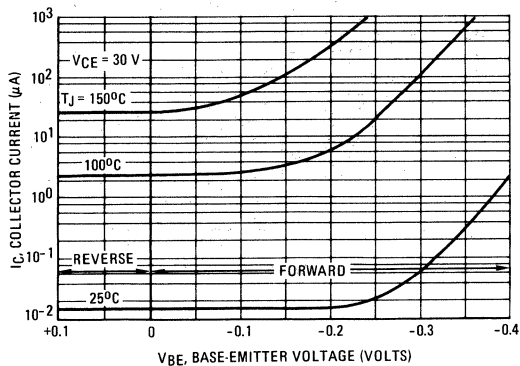
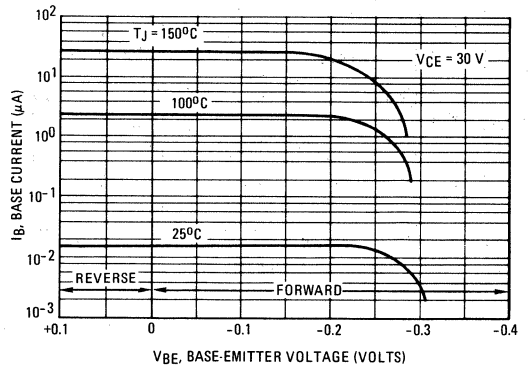


FIGURE 13 – BASE CUT-OFF REGION



2N3738
2N3739

HIGH VOLTAGE SILICON POWER TRANSISTORS

... designed for high-speed switching, linear amplifier applications, high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

- Collector-Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 225 \text{ Vdc @ } I_C = 5.0 \text{ mAdc (2N3738)}$
 $= 300 \text{ Vdc @ } I_C = 5.0 \text{ mAdc (2N3739)}$
- DC Current Gain –
 $h_{FE} = 40-200 @ I_C = 100 \text{ mAdc}$
- Current-Gain – Bandwidth Product –
 $f_T = 10 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- I_S/b Rated to 2.0 Amperes

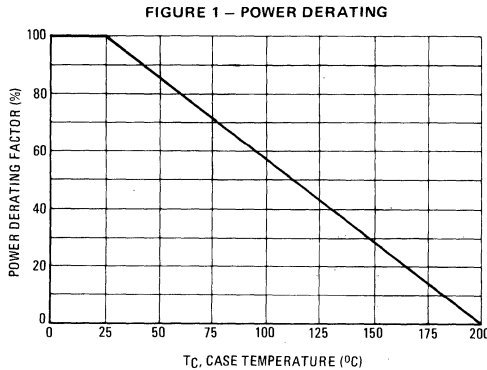
***MAXIMUM RATINGS**

Rating	Symbol	2N3738	2N3739	Unit
Collector-Emitter Voltage	V_{CEO}	225	300	Vdc
Collector-Base Voltage	V_{CB}	250	325	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous	I_C	1.0		Adc
– Peak		2.0		
Base Current – Continuous	I_B	0.50		Adc
– Peak		1.0		
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20	0.133	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

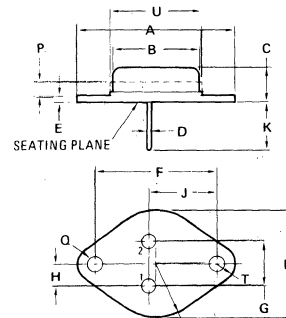
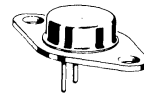
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.5	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data



1.0 AMPERE

POWER TRANSISTORS
NPN SILICON
225, 300 VOLTS
20 WATTS



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	3.14		0.360	
P		1.27		0.050
Q	3.61	3.86	0.142	0.152
S		8.89		0.350
T		3.68		0.145
U		15.75		0.620

All JEDEC Dimensions and Notes Apply.

CASE 80-02
TO-213AA

2N3738, 2N3739

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

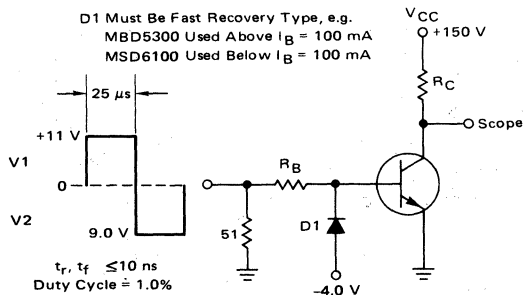
Characteristic	Symbol	Min	Max	Unit
*OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 5.0 mA, I _B = 0)	V _{CEO(sus)}	225 300	—	V _{dc}
Collector-Emitter Cutoff Current (V _{CE} = 125 V _{dc} , I _B = 0) (V _{CE} = 200 V _{dc} , I _B = 0)	I _{CEO}	— —	0.25 0.25	mA _{dc}
Collector-Base Cutoff Current (V _{CB} = 250 V _{dc} , I _E = 0) (V _{CB} = 325 V _{dc} , I _E = 0)	I _{CBO}	— —	0.1 0.1	mA _{dc}
Collector Cutoff Current (V _{CE} = 250 V _{dc} , V _{EB(off)} = 1.5 V _{dc}) (V _{CE} = 300 V _{dc} , V _{EB(off)} = 1.5 V _{dc}) (V _{CE} = 125 V _{dc} , V _{EB(off)} = 1.5 V _{dc} , T _C = 100°C) (V _{CE} = 200 V _{dc} , V _{EB(off)} = 1.5 V _{dc} , T _C = 100°C)	I _{CEV}	— — — —	0.5 0.5 1.0 1.0	mA _{dc}
Emitter-Base Cutoff Current (V _{EB} = 6.0 V _{dc})	I _{EBO}	—	0.1	mA _{dc}
*ON CHARACTERISTICS				
DC Current Gain (1) (I _C = 50 mA, V _{CE} = 10 V _{dc}) (I _C = 100 mA, V _{CE} = 10 V _{dc}) (I _C = 250 mA, V _{CE} = 10 V _{dc})	h _{FE}	30 40 25	— 200 —	—
Collector-Emitter Saturation Voltage (1) (I _C = 250 mA, I _B = 25 mA)	V _{CE(sat)}	—	2.5	V _{dc}
Base-Emitter "ON" Voltage (1) (I _C = 100 mA, V _{CE} = 10 V _{dc})	V _{BE(on)}	—	1.0	V _{dc}
SMALL SIGNAL CHARACTERISTICS				
Current-Gain – Bandwidth Product (2) (I _C = 100 mA, V _{CE} = 10 V _{dc} , f = 10 MHz)	f _T	10	—	MHz
*Output Capacitance (V _{CB} = 100 V _{dc} , I _E = 0, f = 100 kHz)	C _{ob}	—	20	pF
*Small-Signal Current Gain (I _C = 100 mA, V _{CE} = 20 V _{dc} , f = 1.0 kHz)	h _{fe}	35	—	—

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) f_T = |h_{fe}| • frequency

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

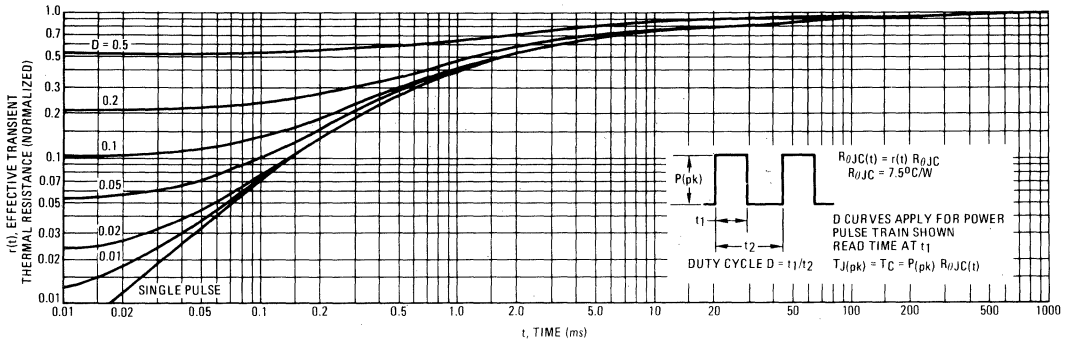


R_B and R_C Varied to Obtain Desired Current Levels

For t_d and t_r, D1 is disconnected and V2 = 0

For PNP test circuit, reverse diode and voltage polarities.

FIGURE 3 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 4 – 2N3738, 2N3739

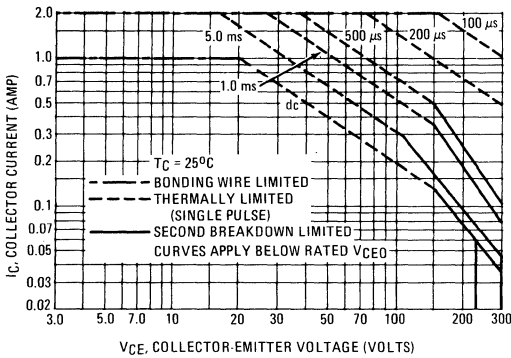
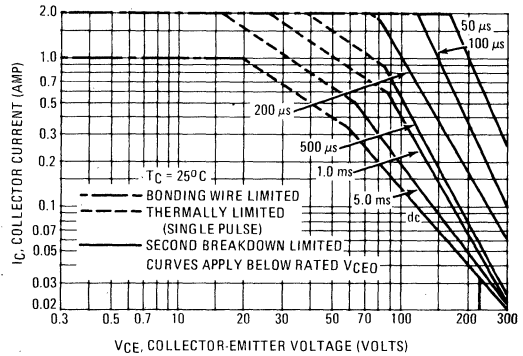


FIGURE 5 – 2N6425



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 4 and 5 is based on $T_C = 25^{\circ}\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 175^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 4 and 5 may be found at any case temperature by using the appropriate curve on Figure 1.

2N3738, 2N3739

FIGURE 6 - DC CURRENT GAIN

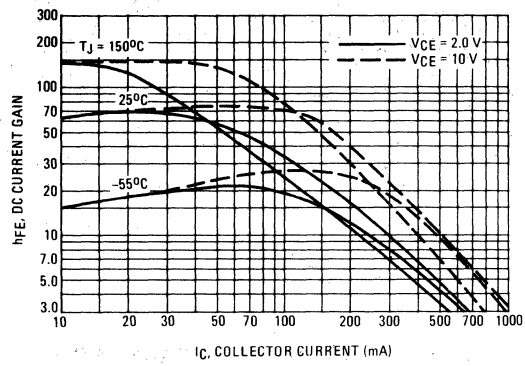


FIGURE 7 - COLLECTOR SATURATION REGION

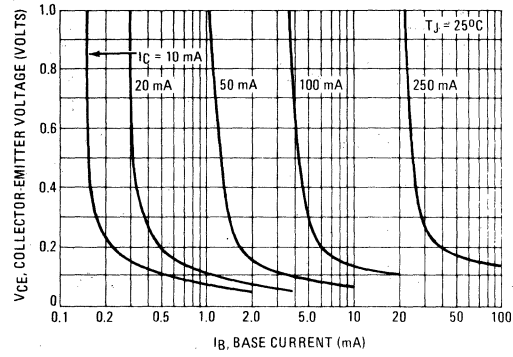
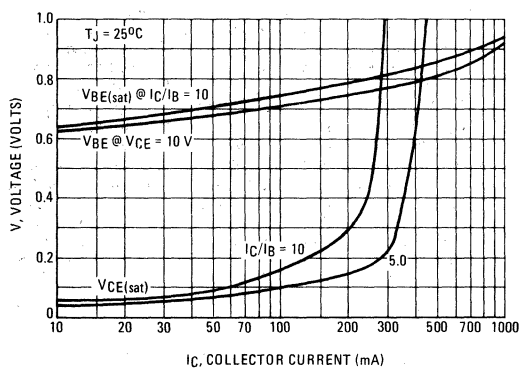


FIGURE 8 - "ON" VOLTAGE



3

2N3740
2N3741,A

MEDIUM-POWER PNP TRANSISTORS

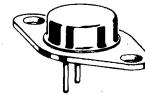
... ideal for use as drivers, switches and medium-power amplifier applications. These devices feature:

- Low Saturation Voltage – $0.6 V_{CE(sat)}$ @ $I_C = 1.0$ Amp
- High Gain Characteristics – h_{FE} @ $I_C = 250$ mA: 30–100
- Excellent Safe Area Limits (See Figure 2)
- Low Collector Cutoff Current – 100 nA (Max) 2N3740, 2N3741A
- Complementary to NPN 2N3766 (2N3740) and 2N3767 (2N3741)

POWER TRANSISTORS

PNP SILICON

60–80 VOLTS
25 WATTS

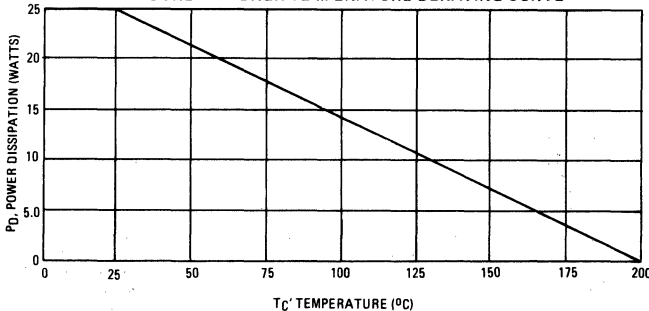


***MAXIMUM RATINGS**

Rating	Symbol	2N3740	2N3741 2N3741A	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	7.0	7.0	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Collector Current – Continuous	I_C		4.0	Adc
– Peak (Note 1)			10	
Base Current	I_B		2.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D		25 0.143	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +200	$^\circ\text{C}$

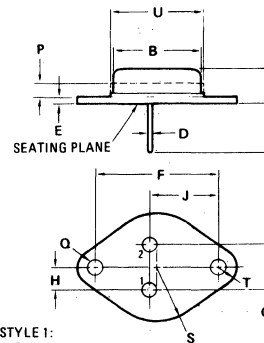
Note 1: See Figure 2

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2.
 Both limits are applicable and must be observed.

*Indicates JEDEC Registered Data.



STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

2N3740, 2N3741,A

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ^① ($I_C = 100 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$ ^①	60 80	— —	Vdc
Emitter Base Cutoff Current ($V_{EB} = 7.0 \text{ Vdc}$)	I_{EBO}	—	0.5 100	mAdc nAdc
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$)	I_{CEX}	—	100	μAdc
($V_{CE} = 80 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$)		—	100	nAdc
($V_{CE} = 40 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)		—	100	μAdc
($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)		—	100	nAdc
Collector-Emitter Cutoff Current ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	1.0	mAdc
($V_{CE} = 60 \text{ Vdc}$, $I_B = 0$)		—	1.0	μAdc
Collector Base Cutoff Current ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	100	μAdc
($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$)		—	100	nAdc

ON CHARACTERISTICS

DC Current Gain ($I_C = 100 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 250 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$)	h_{FE} ^①	40 30 20 10	— 100 — —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0 \text{ Adc}$, $I_B = 125 \text{ mAdc}$)	$V_{CE(sat)}$ ^①	—	0.6	Vdc
Base-Emitter Voltage ($I_C = 250 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$)	V_{BE} ^①	—	1.0	Vdc

TRANSIENT CHARACTERISTICS

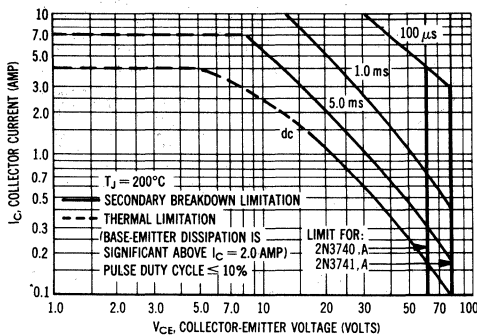
Current-Gain-Bandwidth Product ($I_C = 100 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	f_T	3.0 4.0†	— —	MHz
Common Base Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_C = 0$, $f = 100 \text{ kHz}$)	C_{ob}	—	100	pF
Small-Signal Current Gain ($I_C = 50 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	25	—	—

*Indicates JEDEC Registered Data.

†Motorola guarantees this value in addition to the JEDEC registered data shown.

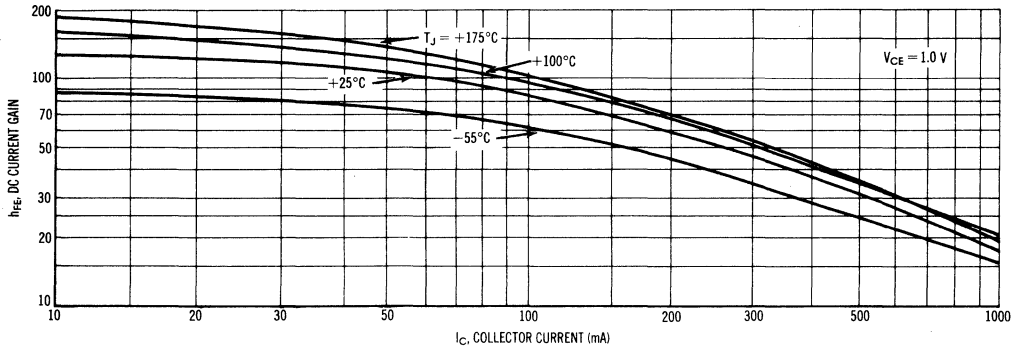
① Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 3 – CURRENT GAIN



SATURATION REGION CHARACTERISTICS
FIGURE 4 – COLLECTOR SATURATION REGION

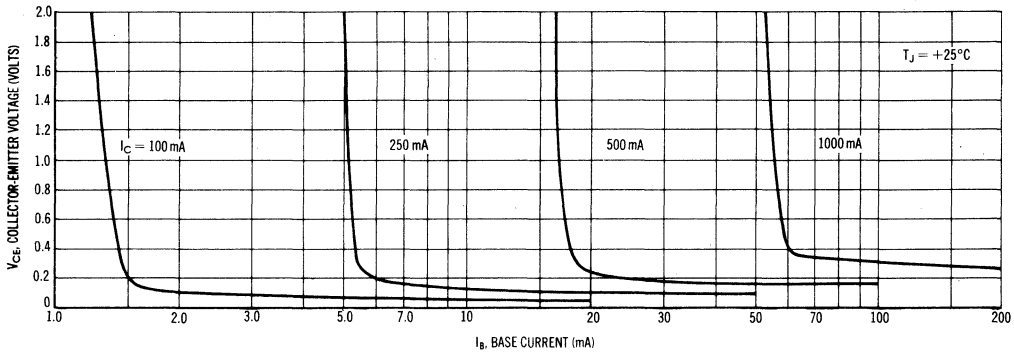


FIGURE 5 – "ON" VOLTAGES

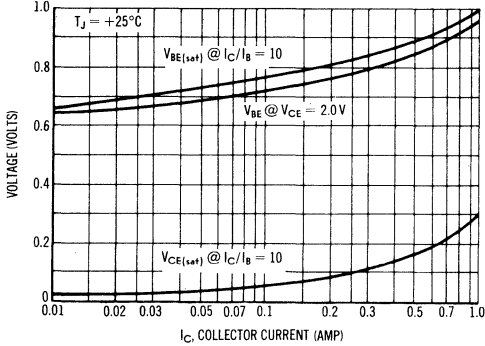
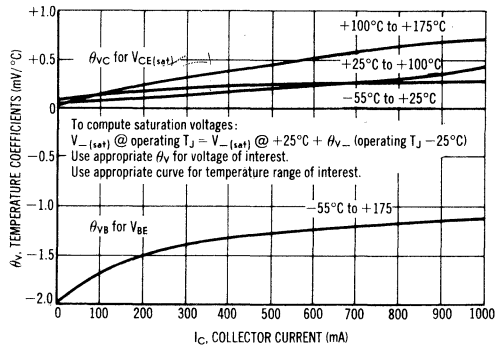


FIGURE 6 – TEMPERATURE COEFFICIENTS



MEDIUM-POWER NPN SILICON TRANSISTORS

... for use in driver circuits, switching, and medium-power-amplifiers applications. These high performance devices feature:

- Low Saturation Voltage — $1.0 V_{CE(sat)}$ @ $I_C = 500 \text{ mA}$
- High Gain Characteristics — $h_{FE} = 40-160$ @ $I_C = 500 \text{ mA}$
- Packaged in the Compact, High-Efficiency TO-213AA Package
- Complementary to PNP 2N3740 (2N3766) and 2N3741 (2N3767)

4 AMPERE
POWER TRANSISTORS

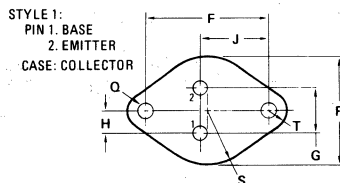
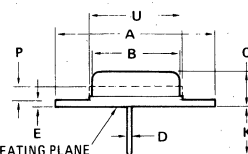
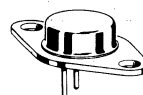
NPN SILICON
60-80 VOLTS
20 WATTS

MAXIMUM RATINGS

Rating	Symbol	2N3766	2N3767	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20	0.133	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	7.5	$^\circ\text{C}/\text{W}$



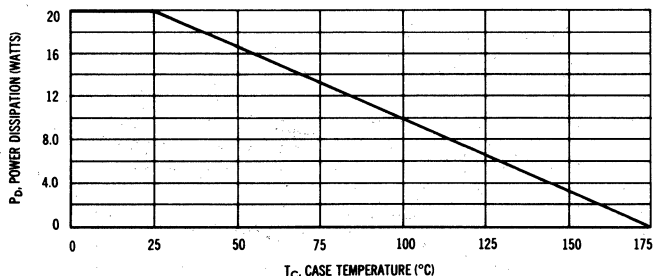
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC Dimensions and Notes Apply.

CASE 80-02
TO-213AA

3

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2. Both limits are applicable and must be observed.

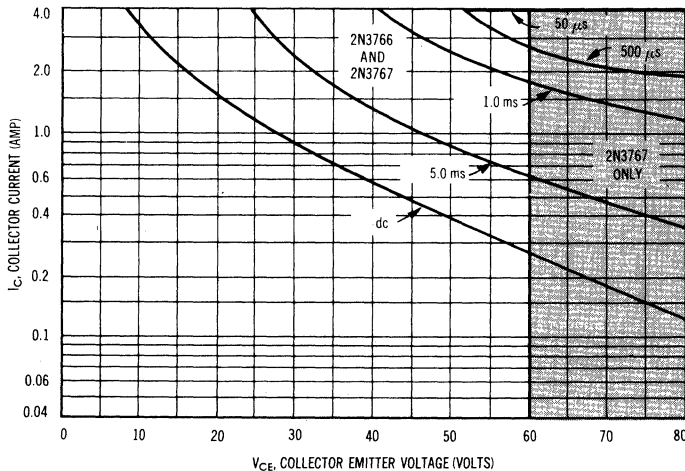
2N3766, 2N3767

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Voltage ⁽¹⁾ (I _C = 100 mA _{dc} , I _B = 0)	2N3766 2N3767	V _{(BR)CEO}	60 80	—	V _{dc}
Emitter-Base Cutoff Current (V _{EB} = 6.0 V _{dc})		I _{EBO}	—	0.75	mA _{dc}
Collector Cutoff Current (V _{CE} = 80 V _{dc} , V _{BE} = 1.5 V _{dc})	2N3766	I _{CCEX}	—	0.1	mA _{dc}
(V _{CE} = 100 V _{dc} , V _{BE} = 1.5 V _{dc})	2N3767		—	0.1	
(V _{CE} = 50 V _{dc} , V _{BE} = 1.5 V _{dc} , T _C = 150°C)	2N3766		—	1.0	
(V _{CE} = 70 V _{dc} , V _{BE} = 1.5 V _{dc} , T _C = 150°C)	2N3767		—	1.0	
Collector-Emitter Cutoff Current (V _{CE} = 80 V _{dc} , I _B = 0)	2N3766	I _{CCEO}	—	0.7	mA _{dc}
(V _{CE} = 80 V _{dc} , I _B = 0)	2N3767		—	0.7	
Collector-Base Cutoff Current (V _{CB} = 80 V _{dc} , I _E = 0)	2N3766	I _{CBO}	—	0.1	mA _{dc}
(V _{CB} = 100 V _{dc} , I _E = 0)	2N3767		—	0.1	
ON CHARACTERISTICS					
DC Current Gain (I _C = 50 mA _{dc} , V _{CE} = 5.0 V _{dc})		h _{FE}	30	—	—
(I _C = 500 mA _{dc} , V _{CE} = 5.0 V _{dc})			40	160	
(I _C = 1.0 A _{dc} , V _{CE} = 10 V _{dc})			20	—	
Collector-Emitter Saturation Voltage (I _C = 1.0 A _{dc} , I _B = 0.1 A _{dc})		V _{CE(sat)}	—	2.5	V _{dc}
(I _C = 500 mA _{dc} , I _B = 50 mA _{dc})			—	1.0	
Base-Emitter Voltage (I _C = 1.0 A _{dc} , V _{CE} = 10 V _{dc})		V _{BE}	—	1.5	V _{dc}
TRANSIENT CHARACTERISTICS					
Current-Gain - Bandwidth Product (I _C = 500 mA _{dc} , V _{CE} = 10 V _{dc} , f = 10 MHz)		f _T	10	—	MHz
Common-Base Output Capacitance (V _{CB} = 10 V _{dc} , I _C = 0 A _{dc} , f = 100 kHz)		C _{ob}	—	50	pF
Small-Signal Current Gain (I _C = 100 mA _{dc} , V _{CE} = 10 V _{dc} , f = 1.0 kHz)		h _{fe}	40	—	—

⁽¹⁾ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – ACTIVE REGION SAFE AREAS



The Safe Operating Area Curves indicate I_C-V_{CE} limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Case temperature and duty cycle of the excursions make no significant change in these safe areas.) The load line may exceed the BV_{CEO} voltage limit only if the collector current has been reduced to 20 mA or less before or at the BV_{ES} limit; then and only then may the load line be extended to the absolute maximum voltage rating of BV_{CEO}. To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

LARGE SIGNAL CHARACTERISTICS

FIGURE 3 - TRANSCONDUCTANCE

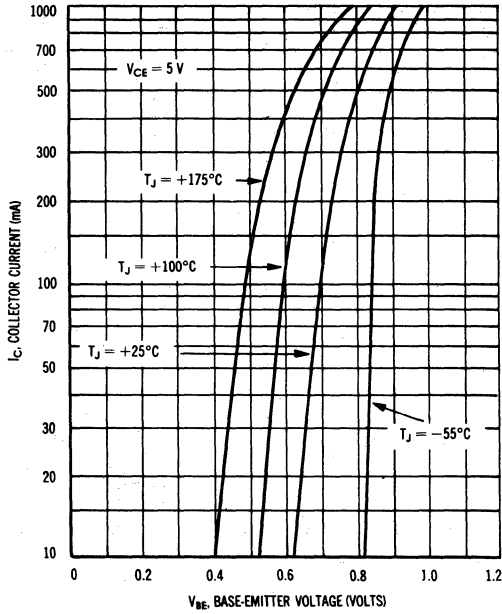
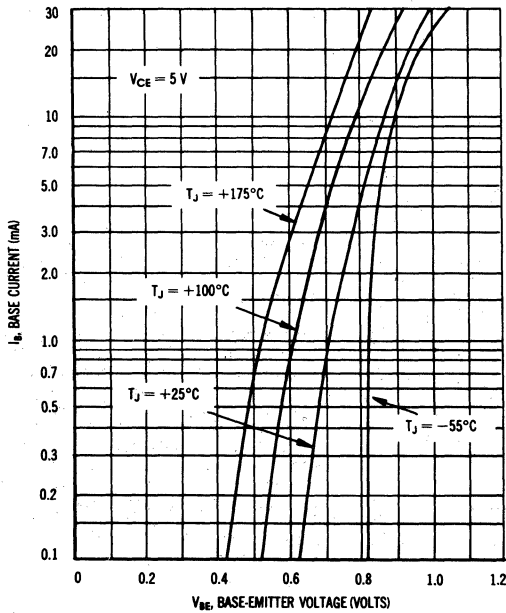


FIGURE 5 - INPUT ADMITTANCE



CUT-OFF CHARACTERISTICS

FIGURE 4 - TRANSCONDUCTANCE

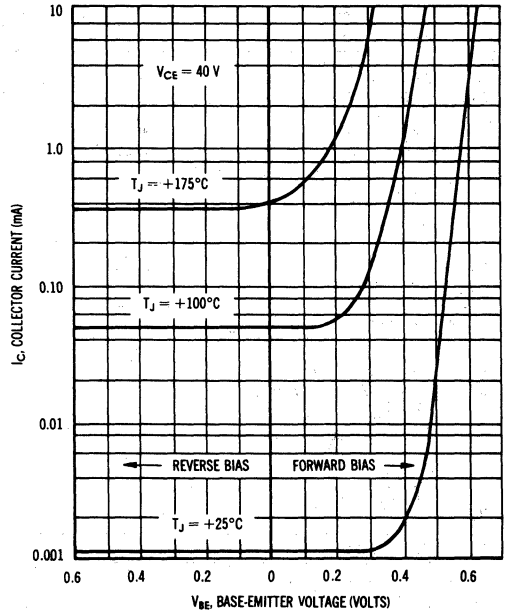


FIGURE 6 - EFFECT OF BASE-EMITTER RESISTANCE

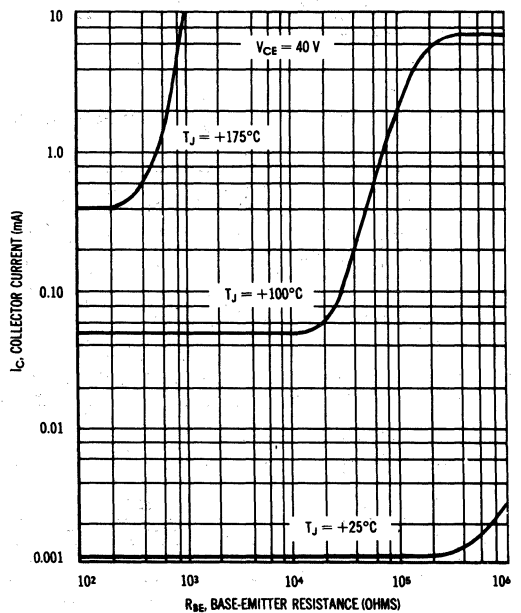


FIGURE 7 – CURRENT GAIN

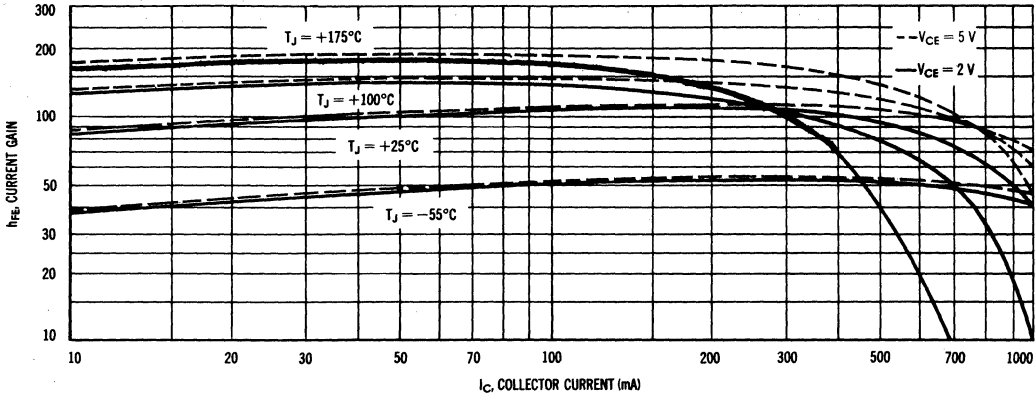


FIGURE 8 – COLLECTOR SATURATION REGION

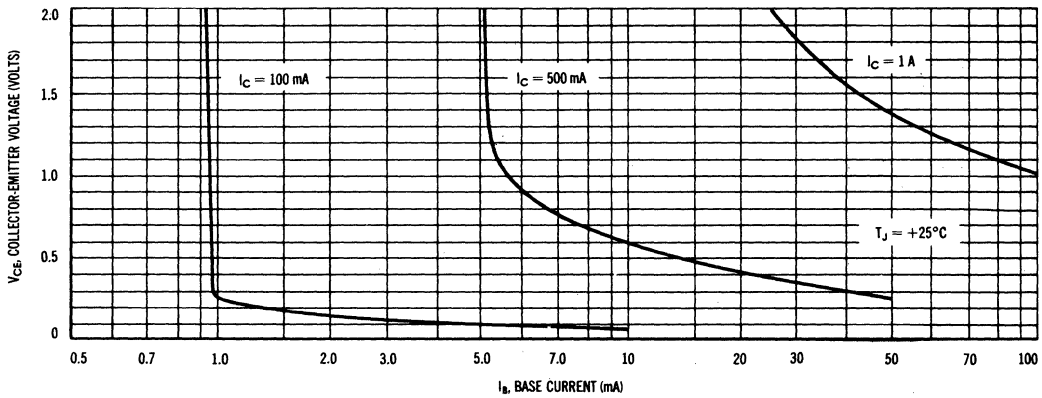


FIGURE 9 – "ON" VOLTAGES

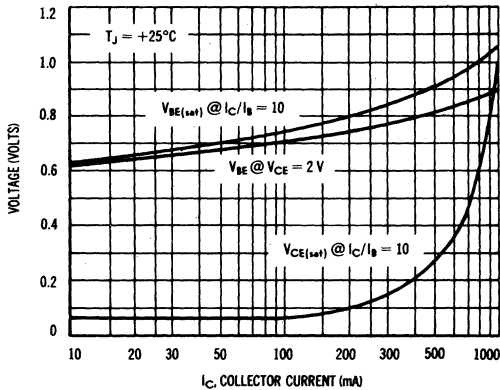
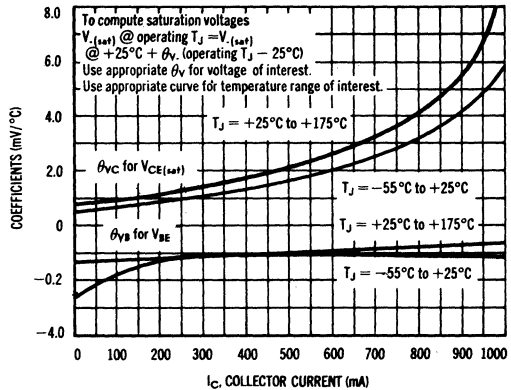


FIGURE 10 – TEMPERATURE COEFFICIENTS



HIGH POWER NPN SILICON POWER TRANSISTORS

... designed for linear amplifiers, series pass regulators, and inductive switching applications.

- Forward Biased Second Breakdown Current Capability

$$I_{S/b} = 3.75 \text{ Adc @ } V_{CE} = 40 \text{ Vdc} - 2\text{N}3771$$

$$= 2.5 \text{ Adc @ } V_{CE} = 60 \text{ Vdc} - 2\text{N}3772$$

***MAXIMUM RATINGS**

Rating	Symbol	2N3771	2N3772	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Emitter Voltage	V_{CEX}	50	80	Vdc
Collector-Base Voltage	V_{CB}	50	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0	7.0	Vdc
Collector Current - Continuous Peak	I_C	30	20	Adc
Base Current - Continuous Peak	I_B	7.5	5.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	150	0.855	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

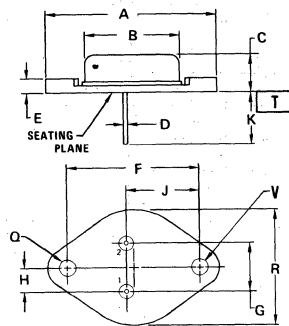
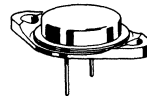
Characteristic	Symbol	2N3771, 2N3772	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C}/\text{W}$

*Indicates JEDEC Registered Data

20 and 30 AMPERE

POWER TRANSISTORS
NPN SILICON

40 and 60 VOLTS
150 WATTS



STYLE 1: PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 3: PIN 1. ANODE
2. CATHODE

NOTES:

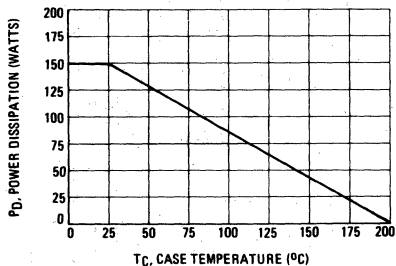
- DIAMETERS Q, V AND SURFACE T ARE DATUMS.
- POSITIONAL TOLERANCE FOR HOLE Q:
 $\varnothing 0.25 (0.010) \text{ @ } | T | V \text{ @ }$
- POSITIONAL TOLERANCE FOR LEADS:
 $\varnothing 0.30 (0.012) \text{ @ } | T | V \text{ @ } | Q \text{ @ }$
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.06	0.039	0.043
E	-	3.43	-	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.45 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	-	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

3

FIGURE 1 - POWER DERATING



2N3771, 2N3772

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
*Collector-Emitter Sustaining Voltage (1) (I _C = 0.2 Adc, I _B = 0)	2N3771 2N3772	V _{CEO(sus)} 40 60	— —	Vdc
Collector-Emitter Sustaining Voltage (I _C = 0.2 Adc, V _{EB(off)} = 1.5 Vdc, R _{BE} = 100 Ohms)	2N3771 2N3772	V _{CEX(sus)} 50 80	— —	Vdc
Collector-Emitter Sustaining Voltage (I _C = 0.2 Adc, R _{BE} = 100 Ohms)	2N3771 2N3772	V _{CER(sus)} 45 70	— —	Vdc
*Collector Cutoff Current (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 50 Vdc, I _B = 0) (V _{CE} = 25 Vdc, I _B = 0)	2N3771 2N3772	I _{CEO} — —	10 10	mAdc
*Collector Cutoff Current (V _{CE} = 50 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 100 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 45 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 30 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C) (V _{CE} = 45 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C)	2N3771 2N3772 2N6257 2N3771 2N3772	I _{CEV} — — — —	2.0 5.0 4.0 10 10	mAdc
*Collector Cutoff Current (V _{CB} = 50 Vdc, I _E = 0) (V _{CB} = 100 Vdc, I _E = 0)	2N3771 2N3772	I _{CBO} — —	2.0 5.0	mAdc
*Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0) (V _{BE} = 7.0 Vdc, I _C = 0)	2N3771 2N3772	I _{EBO} — —	5.0 5.0	mAdc
*ON CHARACTERISTICS				
DC Current Gain (1) (I _C = 15 Adc, V _{CE} = 4.0 Vdc) (I _C = 10 Adc, V _{CE} = 4.0 Vdc) (I _C = 8.0 Adc, V _{CE} = 4.0 Vdc) (I _C = 30 Adc, V _{CE} = 4.0 Vdc) (I _C = 20 Adc, V _{CE} = 4.0 Vdc)	2N3771 2N3772 2N3771 2N3772	h _{FE} 15 15 5.0 5.0	60 60 — —	—
Collector-Emitter Saturation Voltage (I _C = 15 Adc, I _B = 1.5 Adc) (I _C = 10 Adc, I _B = 1.0 Adc) (I _C = 30 Adc, I _B = 6.0 Adc) (I _C = 20 Adc, I _B = 4.0 Adc)	2N3771 2N3772 2N3771 2N3772	V _{CE(sat)} — — — —	2.0 1.4 4.0 4.0	Vdc
Base-Emitter On Voltage (I _C = 15 Adc, V _{CE} = 4.0 Vdc) (I _C = 10 Adc, V _{CE} = 4.0 Vdc) (I _C = 8.0 Adc, V _{CE} = 4.0 Vdc)	2N3771 2N3772	V _{BE(on)} — —	2.7 2.2	Vdc
*DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I _C = 1.0 Adc, V _{CE} = 4.0 Vdc, f _{test} = 50 kHz)		f _T	0.2	MHz
Small-Signal Current Gain (I _C = 1.0 Adc, V _{CE} = 4.0 Vdc, f = 1.0 kHz)		h _{fe}	40	—
SECOND BREAKDOWN				
Second Breakdown Energy with Base Forward Biased t = 1.0 s (non-repetitive) (V _{CE} = 40 Vdc) (V _{CE} = 60 Vdc)	2N3771 2N3772	I _{S/b} 3.75 2.5	— —	Adc

*Indicates JEDEC Registered Data

(1) Pulse Test: 300 μs, Rep. Rate 60 cps.

FIGURE 2 - THERMAL RESPONSE - 2N3771, 2N3772

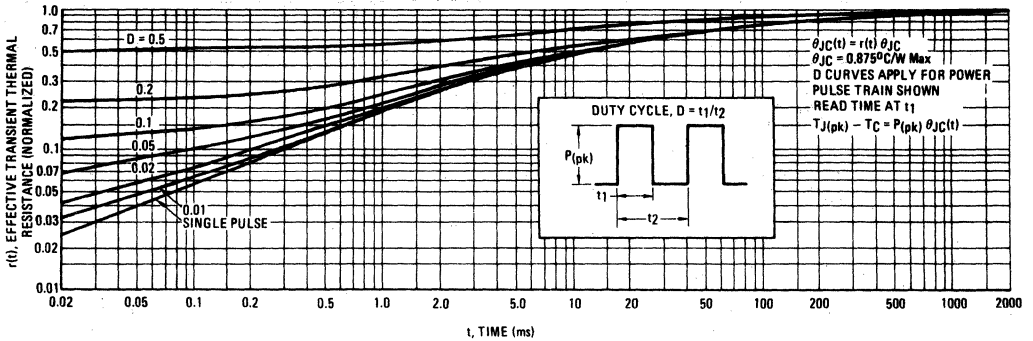
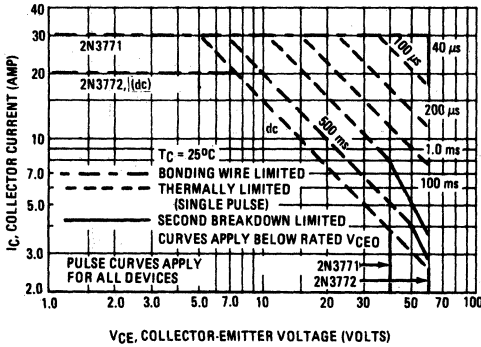


FIGURE 3 - ACTIVE-REGION SAFE OPERATING AREA - 2N3771, 2N3772



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based upon JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3, $T_{J(pk)}$ will be found to be less than $T_{J(max)}$ for pulse widths of 1 ms and less. When using Motorola transistors, it is permissible to increase the pulse power limits until limited by $T_{J(max)}$.

FIGURE 4 - SWITCHING TIME TEST CIRCUIT

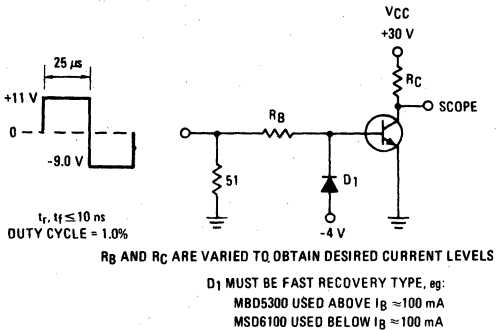


FIGURE 5 - TURN-ON TIME

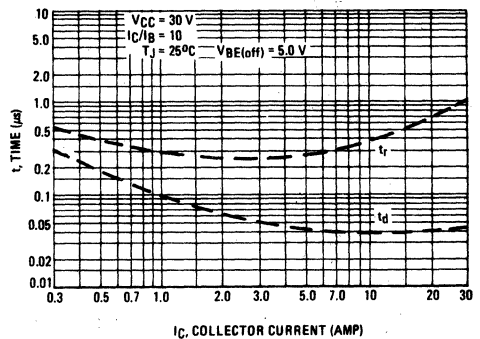


FIGURE 6 – TURN-OFF TIME

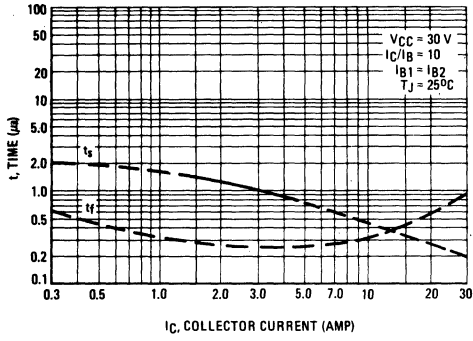


FIGURE 7 – CAPACITANCE

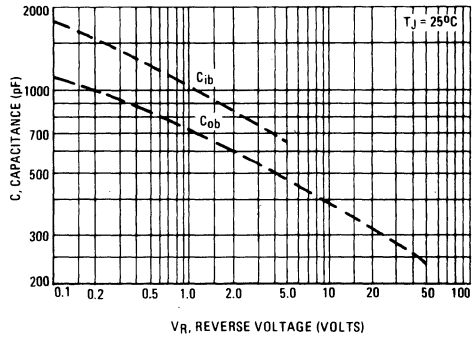


FIGURE 8 – DC CURRENT GAIN

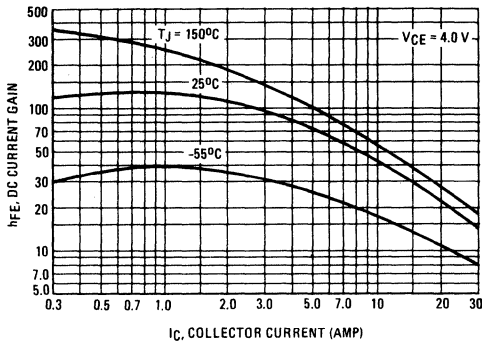
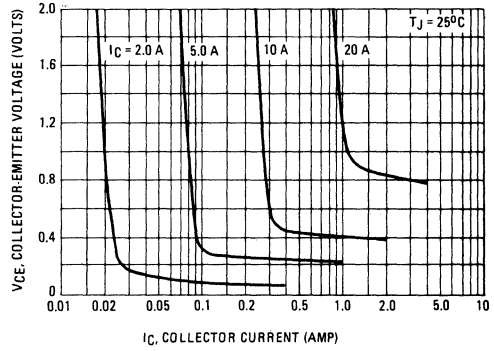


FIGURE 9 – COLLECTOR SATURATION REGION



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

**NPN
2N3773
PNP
2N6609**

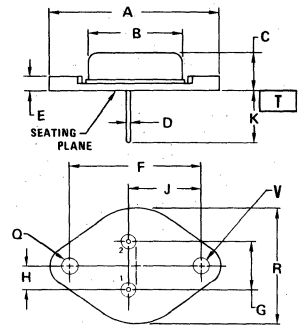
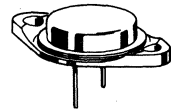
COMPLEMENTARY SILICON POWER TRANSISTORS

The 2N3773 and 2N6609 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc to dc converters or inverters.

- High Safe Operating Area (100% Tested)
150 W @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
hFE = 15 (Min) @ 8 A, 4 V
VCE(sat) = 1.4 V (Max) @ IC = 8 A, IB = 0.8 A
- For Low Distortion Complementary Designs

16 AMPERE COMPLEMENTARY POWER TRANSISTORS

**140 VOLTS
150 WATTS**



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 3:
PIN 1. ANODE
2. CATHODE

- NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
 2. POSITIONAL TOLERANCE FOR HOLE Q:
⌀ ± 0.25 (0.010) Ⓜ T V Ⓜ
 3. POSITIONAL TOLERANCE FOR LEADS:
⌀ ± 0.30 (0.012) Ⓜ T V Ⓜ Q Ⓜ
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	-	3.43	-	0.135
F	30.15	BSC	1.187	BSC
G	10.92	BSC	0.430	BSC
H	5.46	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	-	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

* MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CEO}	140	Vdc
Collector-Emitter Voltage	V _{CEX}	160	Vdc
Collector-Base Voltage	V _{CBO}	160	Vdc
Emitter-Base Voltage	V _{EBO}	7	Vdc
Collector Current — Continuous	I _C	16	Adc
— Peak (1)		30	
Base Current — Continuous	I _B	4	Adc
— Peak (1)		15	
Total Power Dissipation @ T _C = 25°C	P _D	150	Watts
Derate above 25°C		0.855	W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.17	°C/W

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

2N3773 NPN/2N6609 PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

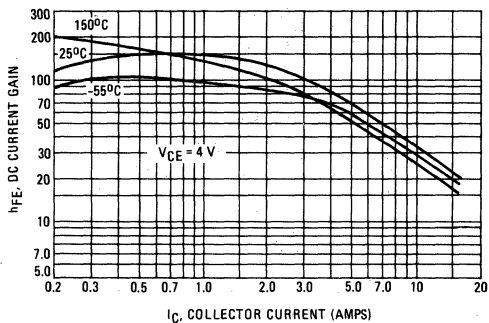
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
*Collector-Emitter Breakdown Voltage (I _C = 0.2 Adc, I _B = 0)	V _{CEO(sus)}	140	—	Vdc
*Collector-Emitter Sustaining Voltage (I _C = 0.1 Adc, V _{BE(off)} = 1.5 Vdc, R _{BE} = 100 Ohms)	V _{CEX(sus)}	160	—	Vdc
Collector-Emitter Sustaining Voltage (I _C = 0.2 Adc, R _{BE} = 100 Ohms)	V _{CER(sus)}	150	—	Vdc
*Collector Cutoff Current (V _{CE} = 120 Vdc, I _B = 0)	I _{CEO}	—	10	mAdc
*Collector Cutoff Current (V _{CE} = 140 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CE} = 140 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 150°C)	I _{CEx}	—	2 10	mAdc
Collector Cutoff Current (V _{CB} = 140 Vdc, I _E = 0)	I _{CBO}	—	2	mAdc
*Emitter Cutoff Current (V _{BE} = 7 Vdc, I _C = 0)	I _{EBO}	—	5	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain *(I _C = 8 Adc, V _{CE} = 4 Vdc) (I _C = 16 Adc, V _{CE} = 4 Vdc)	h _{FE}	15 5	60	—
Collector-Emitter Saturation Voltage *(I _C = 8 Adc, I _B = 800 mAdc) (I _C = 16 Adc, I _B = 3.2 Adc)	V _{CE(sat)}	—	1.4 4	Vdc
*Base-Emitter On Voltage (I _C = 8 Adc, V _{CE} = 4 Vdc)	V _{BE(on)}	—	2.2	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common-Emitter Small-Signal, Short-Circuit, Forward Current Transfer Ratio (I _C = 1 A, f = 50 kHz)	h _{fe}	4	—	—
*Small-Signal Current Gain (I _C = 1 Adc, V _{CE} = 4 Vdc, f = 1 kHz)	h _{fe}	40	—	—
SECOND BREAKDOWN CHARACTERISTICS				
Second Breakdown Collector Current with Base Forward Biased t = 1 s (non-repetitive), V _{CE} = 100 V, See Figure 12	I _{S/b}	1.5	—	Adc

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

*Indicates JEDEC Registered Data

NPN

FIGURE 1 - DC CURRENT GAIN



PNP

FIGURE 2 - DC CURRENT GAIN

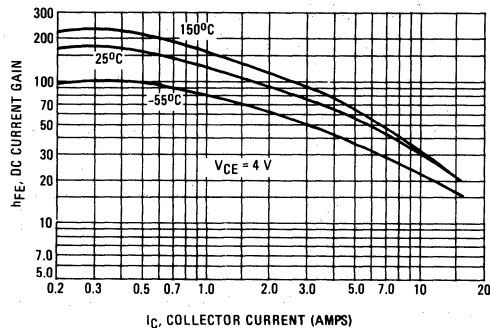


FIGURE 3 - COLLECTOR SATURATION REGION

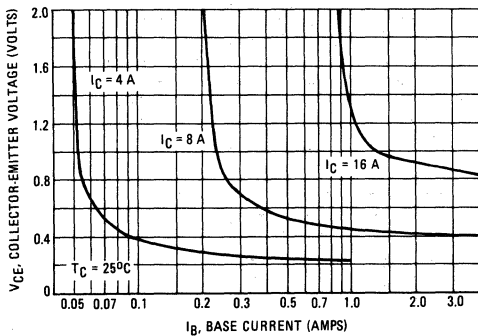


FIGURE 4 - COLLECTOR SATURATION REGION

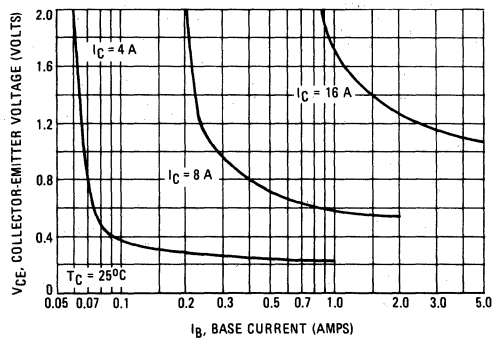


FIGURE 5 - "ON" VOLTAGE

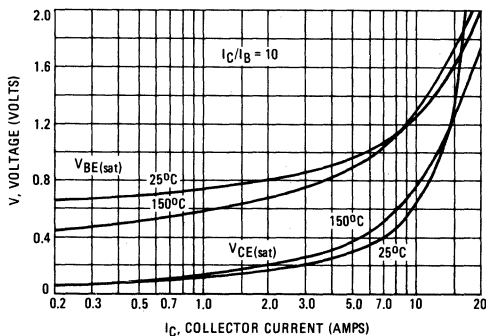
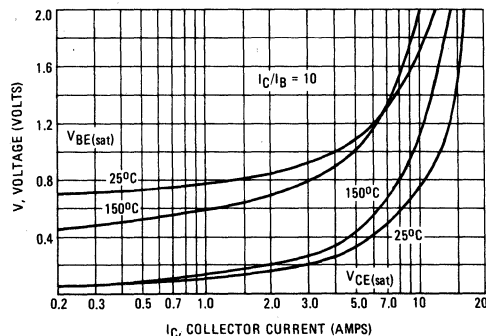
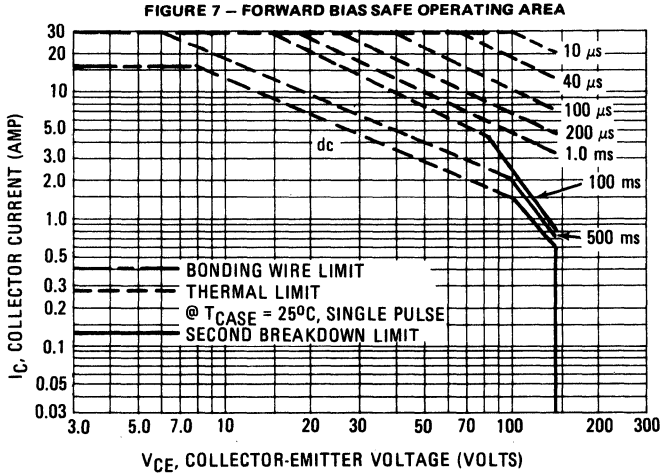


FIGURE 6 - "ON" VOLTAGE

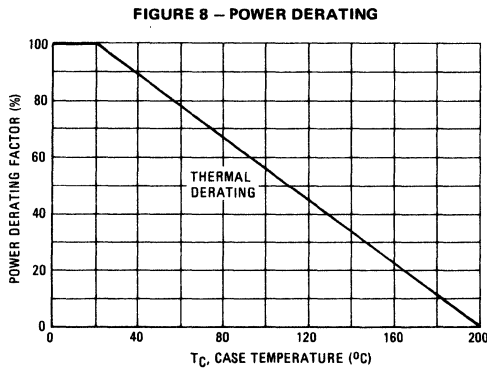


3



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)} = 200^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^\circ C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



2N3789
thru
2N3792

SILICON PNP POWER TRANSISTORS

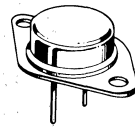
... designed for medium-speed switching and amplifier applications.
 These devices feature:

- Total Switching Time @ 3 A \approx 1 μ s (typ)
- Two Gain Ranges:
 h_{FE} (min) = 15 and 30 @ 3 A (2N3789, 2N3790)
 25 and 50 @ 1 A (2N3791, 2N3792)
- Low $V_{CE(sat)} = 0.5$ V (typ) @ $I_C = 4.0$ A, $I_B = 0.4$ A
- Excellent Safe Area Limits
- Complementary NPN types available – 2N3713 thru 2N3716

10 AMPERE

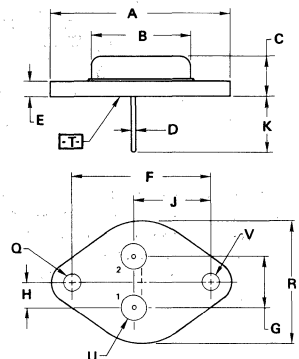
POWER TRANSISTORS
PNP SILICON

60-80 VOLTS
150 WATTS



MAXIMUM RATINGS

Characteristic	Symbol	2N3789 2N3791	2N3790 2N3792	Unit
Collector-Base Voltage	V_{CB}	60	80	Volts
Collector-Emitter Voltage	V_{CEO}	60	80	Volts
Emitter-Base Voltage	V_{EB}	7.0	7.0	Volts
Collector Current (Continuous)	I_C	10	10	Amps
Base Current (Continuous)	I_B	4.0	4.0	Amps
Power Dissipation	P_D	150	150	Watts
Thermal Resistance	θ_{JC}	1.17	1.17	$^{\circ}C/W$
Junction Operating and Storage Temperature Range	T_J, T_{stg}	-65 to +200		$^{\circ}C$



NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. \square IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\phi \pm 0.13 (0.005) \text{ M T V } \textcircled{Q}$$

FOR LEADS:

$$\phi \pm 0.13 (0.005) \text{ M T V } \textcircled{Q} \textcircled{U}$$

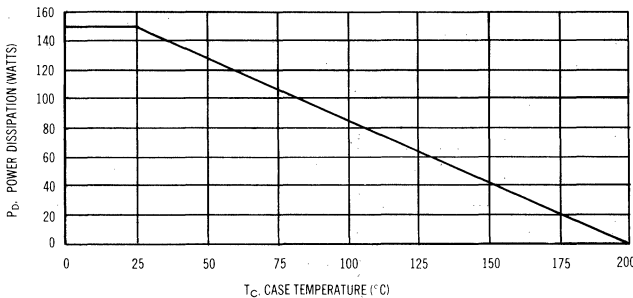
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-		26.67	
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Limits are indicated by Figures 15, 16. Both limits are applicable and must be observed.

2N3789 thru 2N3792

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I _C = 200 mA, I _B = 0)	V _{CEO(sus)} *	60	—	Vdc
	2N3789, 2N3791 2N3790, 2N3792	80	—	
Collector-Emitter Cutoff Current (V _{CE} = 60 Vdc, V _{BE} = -1.5 Vdc) (V _{CE} = 80 Vdc, V _{BE} = -1.5 Vdc) (V _{CE} = 60 Vdc, V _{BE} = -1.5 Vdc, T _C = 150°C) (V _{CE} = 80 Vdc, V _{BE} = -1.5 Vdc, T _C = 150°C)	I _{CEX}	—	1	mA
	2N3789, 2N3791 2N3790, 2N3792	—	1	
	2N3789, 2N3791 2N3790, 2N3792	—	5	
	2N3789, 2N3791 2N3790, 2N3792	—	5	
Emitter-Base Cutoff Current (V _{EB} = 7 Vdc)	I _{EBO}	—	5	mA
DC Current Gain* (I _C = 1 A, V _{CE} = 2 Vdc)	h _{FE} *	25	90	—
	2N3789, 2N3790 2N3791, 2N3792	50	180	
	2N3789, 2N3790 2N3791, 2N3792	15	—	
	2N3789, 2N3790 2N3791, 2N3792	30	—	
Collector-Emitter Saturation Voltage* (I _C = 4 A, I _B = 0.4 A) (I _C = 5 A, I _B = 0.5 A)	V _{CE(sat)} *	—	1.0	Vdc
	2N3789, 2N3790 2N3791, 2N3792	—	1.0	
Base-Emitter On Voltage* (I _C = 5 A, V _{CE} = 2 Vdc)	V _{BE(on)} *	—	2.0	Vdc
	2N3789, 2N3790 2N3791, 2N3792	—	1.8	
	All Types	—	4.0	
Current Gain – Bandwidth Product (V _{CE} = 10 Vdc, I _C = 0.5 A, f = 1 MHz)	f _T	4	—	MHz
	All Types			

*Sweep Test: 1/2 sine wave cycle @ 60 cps.

FIGURE 2 – TYPICAL SWITCHING TIMES AND TEST CIRCUIT

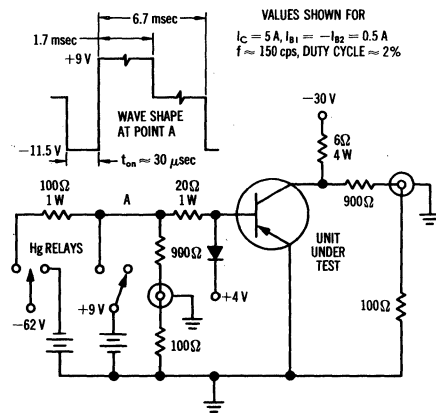
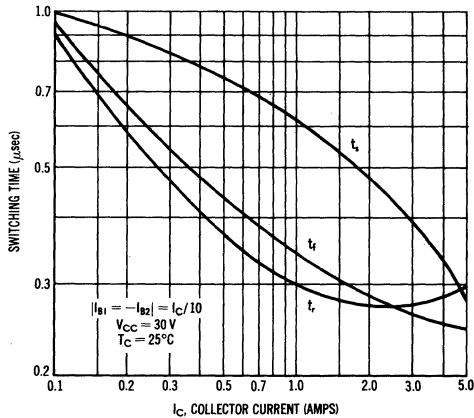


FIGURE 3 – CURRENT GAIN VARIATIONS

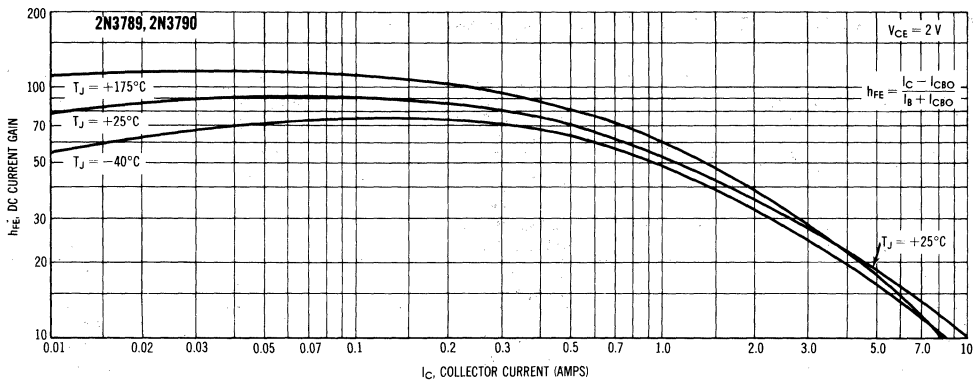


FIGURE 4 – CURRENT GAIN VARIATIONS

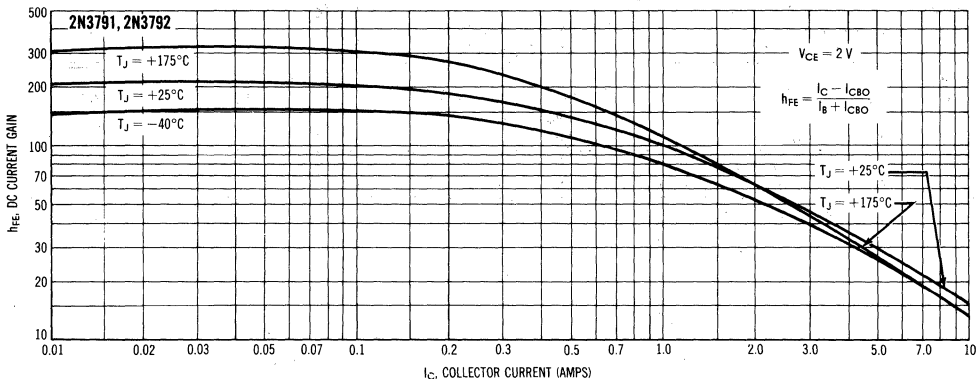


FIGURE 5 – SATURATION VOLTAGES

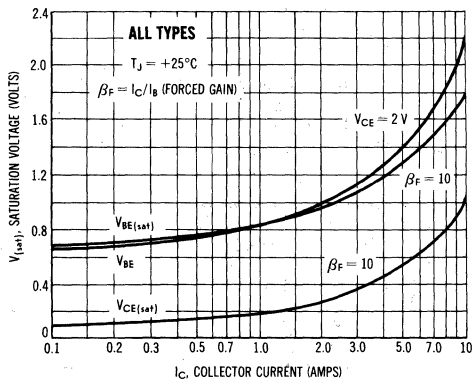
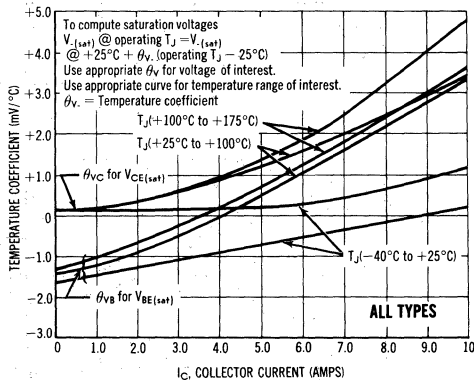


FIGURE 6 – TEMPERATURE COEFFICIENTS



3

SAFE OPERATING AREAS

FIGURE 7 - 2N3789, 2N3791

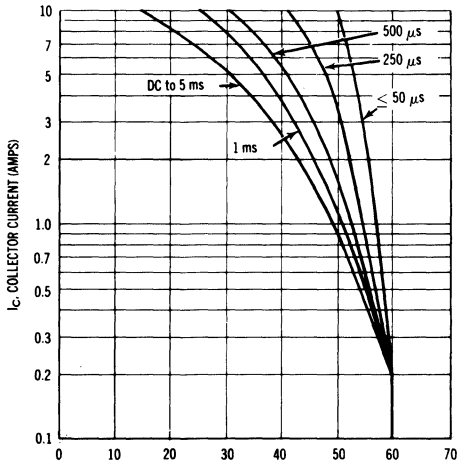
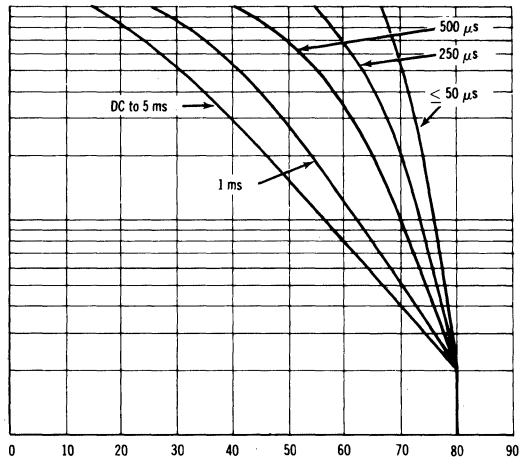


FIGURE 8 - 2N3790, 2N3792



V_{CE} COLLECTOR-EMITTER VOLTAGE (VOLTS)

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short.

(Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J , the power-temperature derating curve must be observed for both steady state and pulse power conditions.

FIGURE 9 - CUT-OFF REGION TRANSCONDUCTANCE

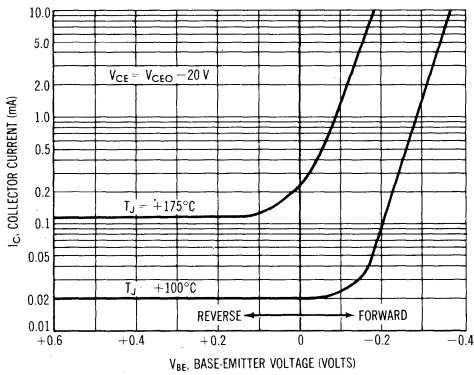
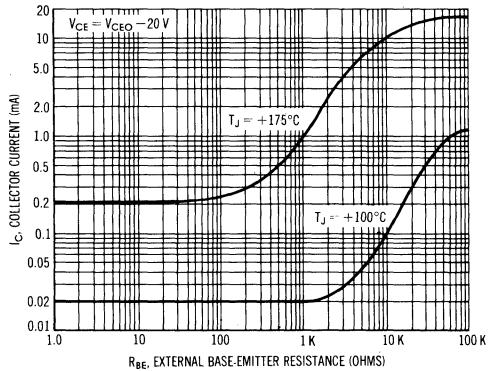


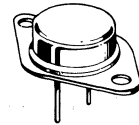
FIGURE 10 - COLLECTOR CUT-OFF CURRENT versus BASE-EMITTER RESISTANCE



NPN
2N3902

3.5 AMPERE
POWER TRANSISTORS
NPN SILICON

400 VOLTS
100 WATTS



HIGH VOLTAGE NPN SILICON TRANSISTORS

... designed for use in high-voltage inverters, converters, switching regulators and line operated amplifiers.

- High Collector-Emitter Voltage – $V_{CEX} = 700$ Vdc
- Excellent DC Current Gain –
 $h_{FE} = 10$ (Min) @ $I_C = 2.5$ Adc
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.8$ Vdc (Max) @ $I_C = 1.0$ Adc

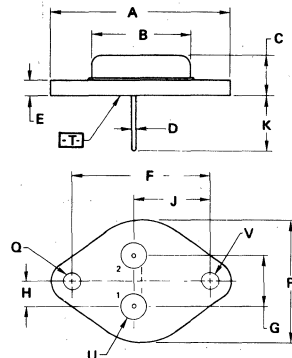
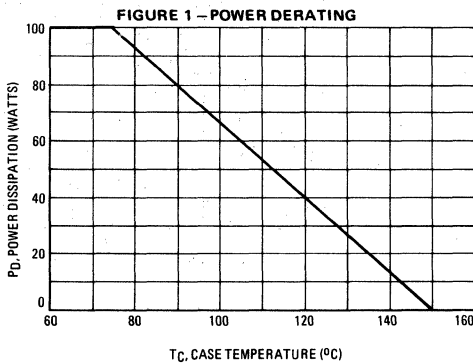
***MAXIMUM RATINGS**

Rating	Symbol	2N3902	Unit
Collector-Emitter Voltage	V_{CEO}	400	Vdc
Collector-Emitter Voltage	V_{CEX}	700	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	3.5	A dc
Base Current	I_B	2.0	A dc
Total Device Dissipation @ $T_C = 75^\circ\text{C}$ Derate above 75°C	P_D	100 1.33	Watts W/ $^\circ\text{C}$
Operating Junction Temperature Range	T_J	-65 to +150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.75	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data



NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\phi \pm 0.13 (0.005) \text{ M T V } \textcircled{\text{M}}$$

FOR LEADS:

$$\phi \pm 0.13 (0.005) \text{ M T V } \textcircled{\text{M}} \textcircled{\text{Q}}$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

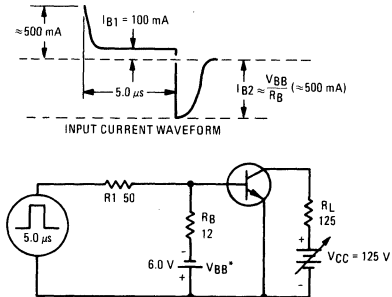
***ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ($I_C = 100 \text{ mA}$, $I_B = 0$) (See Figure 12)	$V_{CE(sus)}$	325	—	Vdc
Collector Cutoff Current ($V_{CE} = 400 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	0.25	mA
Collector Cutoff Current ($V_{CE} = 700 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 400 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$)	I_{CEX}	—	2.5 0.5	mA
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	5.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 1.0 \text{ A}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 2.5 \text{ A}$, $V_{CE} = 5.0 \text{ Vdc}$)	h_{FE}	30 10	90 —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0 \text{ A}$, $I_B = 0.1 \text{ A}$) ($I_C = 2.5 \text{ A}$, $I_B = 0.5 \text{ A}$)	$V_{CE(sat)}$	— —	0.8 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0 \text{ A}$, $I_B = 0.1 \text{ A}$) ($I_C = 2.5 \text{ A}$, $I_B = 0.5 \text{ A}$)	$V_{BE(sat)}$	— —	1.5 2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product ($I_C = 0.2 \text{ A}$, $V_{CE} = 10 \text{ Vdc}$)	f_T	2.8	—	MHz

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



5.0% Duty Cycle
 $t_r = 100 \text{ ns}$

FIGURE 3 — TURN-ON TIME

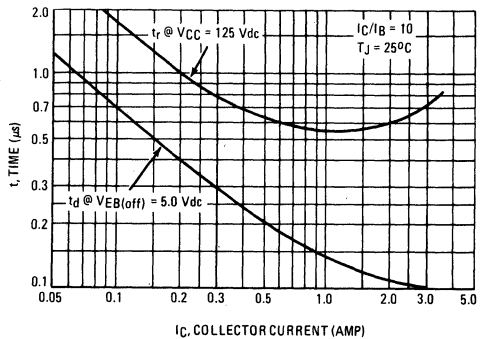


FIGURE 4 – THERMAL RESPONSE

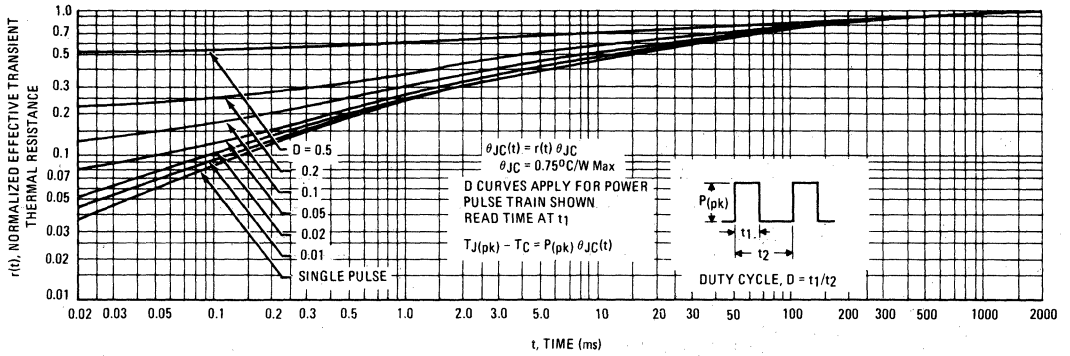
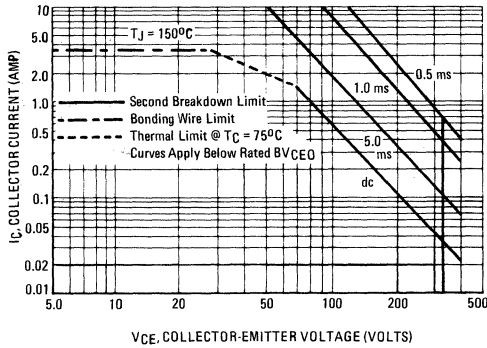


FIGURE 5 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_J(pk) = 150^\circ\text{C}$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_J(pk) \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

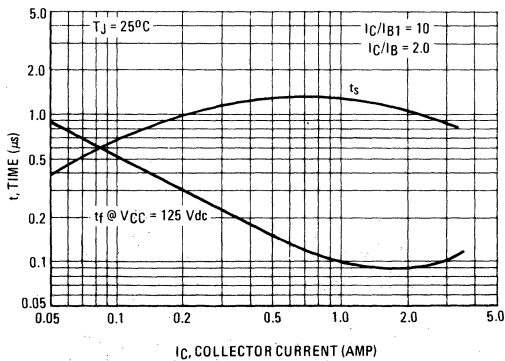
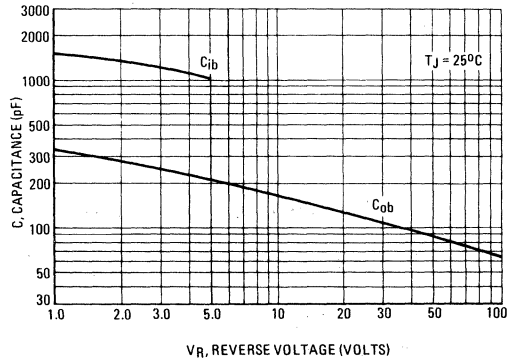


FIGURE 7 – CAPACITANCE



3

FIGURE 8 – DC CURRENT GAIN

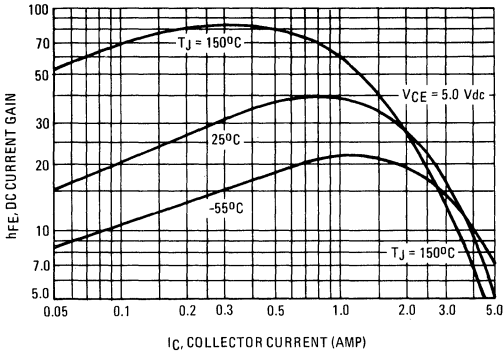


FIGURE 9 – "ON" VOLTAGES

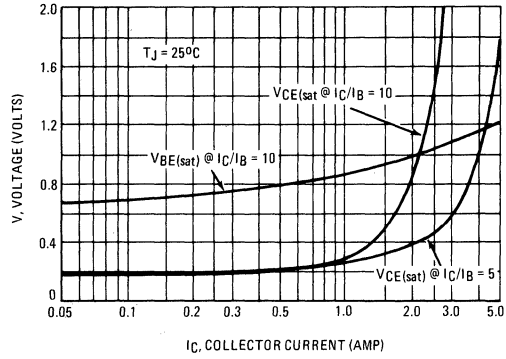


FIGURE 10 – COLLECTOR CUT-OFF REGION

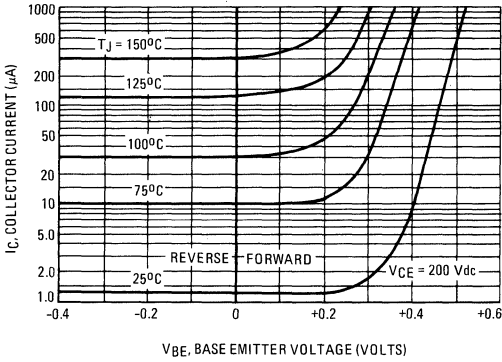


FIGURE 11 – TEMPERATURE COEFFICIENTS

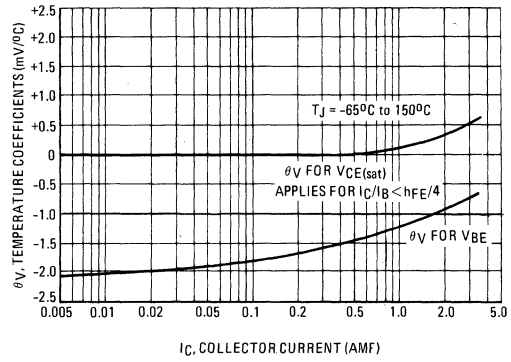
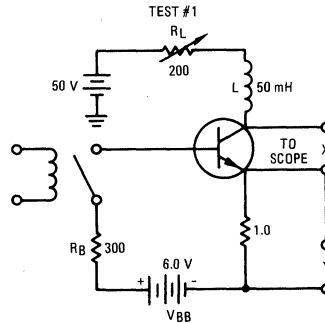
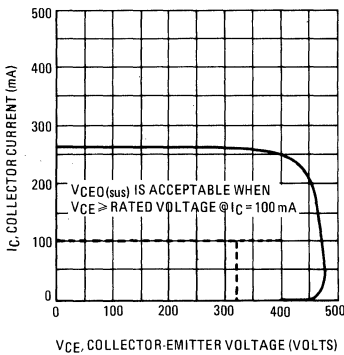


FIGURE 12 – COLLECTOR-EMITTER SUSTAINING VOLTAGE TEST CIRCUITS AND LOAD LINES



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N4233A

MEDIUM-POWER SILICON TRANSISTOR

... designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)} = 0.7 \text{ Vdc (Max) @ } I_C = 1.5 \text{ Adc}$
- Low Leakage Current – $I_{CEX} = 0.1 \text{ mAdc (Max)}$
- Excellent DC Current Gain – $h_{FE} = 25-100 @ I_C = 1.5 \text{ Adc}$
- High Current Gain – Bandwidth Product – $f_T = 4.0 \text{ MHz @ } I_C = 0.25 \text{ Adc}$

***MAXIMUM RATINGS**

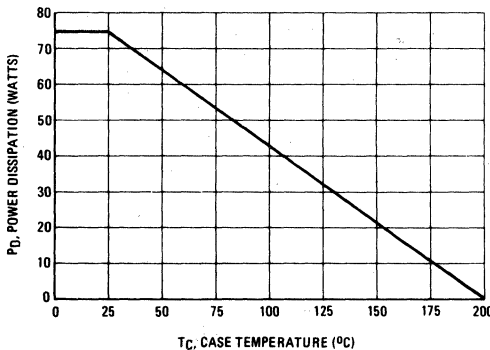
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	5.0	Adc
Peak		10	
Base Current	I_B	2.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	75	Watts
Derate above 25°C		0.43	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*** THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.32	°C/W

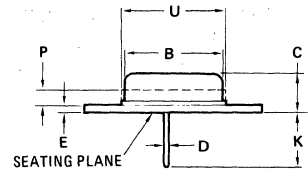
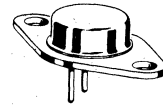
* Indicates JEDEC registered data. (All values meet or exceed JEDEC registered data).

FIGURE 1 – POWER DERATING



**5.0 AMPERE
 SILICON
 POWER TRANSISTOR**

**80 VOLTS
 75 WATTS**

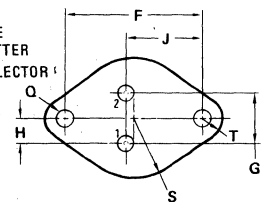


STYLE 1:

PIN 1: BASE

2: EMITTER

CASE: COLLECTOR



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC Dimensions and Notes Apply.
CASE 80-02
TO-213AA

3

2N4233A

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
*OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	80	—	Vdc
Collector Cutoff Current ($V_{CE} = 70\text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	1.0	mA
Collector Cutoff Current ($V_{CE} = 80\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 80\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	—	0.1 1.0	mA
Collector Cutoff Current ($V_{CB} = 80\text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	0.05	mA
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	0.5	mA
ON CHARACTERISTICS				
DC Current Gain (1) *($I_C = 0.5\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$) *($I_C = 1.5\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$) *($I_C = 3.0\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$) *($I_C = 5.0\text{ A}$, $V_{CE} = 4.0\text{ Vdc}$)	h_{FE}	40 25 10 4.0	— 100 — —	—
*Collector-Emitter Saturation Voltage (1) ($I_C = 1.5\text{ A}$, $I_B = 0.15\text{ A}$) ($I_C = 3.0\text{ A}$, $I_B = 0.3\text{ A}$) ($I_C = 5.0\text{ A}$, $I_B = 1.25\text{ A}$)	$V_{CE(sat)}$	— — —	0.7 2.0 4.0	Vdc
*Base-Emitter On Voltage (1) ($I_C = 1.5\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$)	$V_{BE(on)}$	—	1.4	Vdc
*DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product ($I_C = 0.5\text{ A}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1.0\text{ MHz}$)	f_T	4.0	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	—	300	pF
Small-Signal Current Gain ($I_C = 0.5\text{ A}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ kHz}$)	h_{fe}	20	—	—

*Indicates JEDEC registered data.

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

3

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

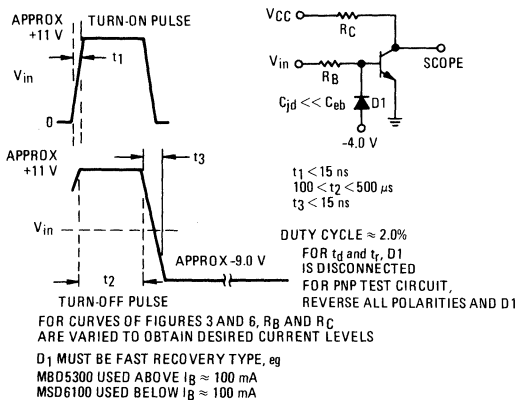


FIGURE 3 — TURN "ON" TIME

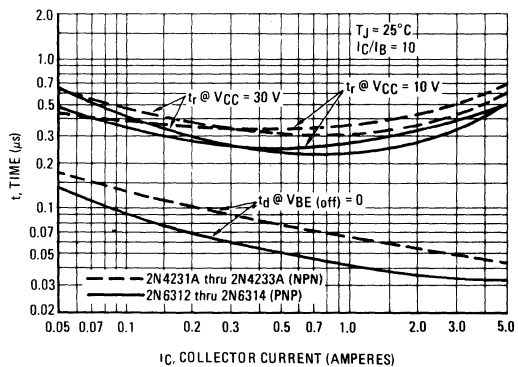


FIGURE 4 - THERMAL RESPONSE

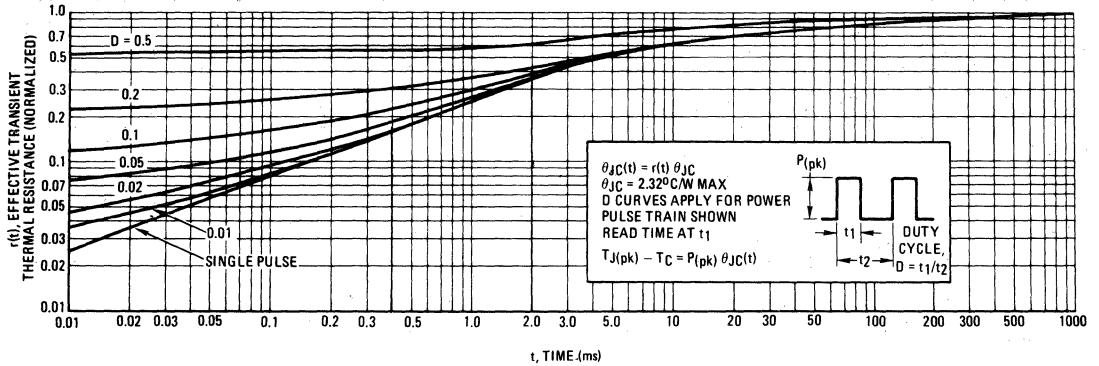
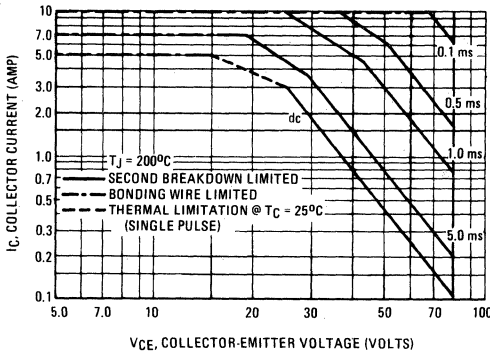


FIGURE 5 - ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 - TURN "OFF" TIME

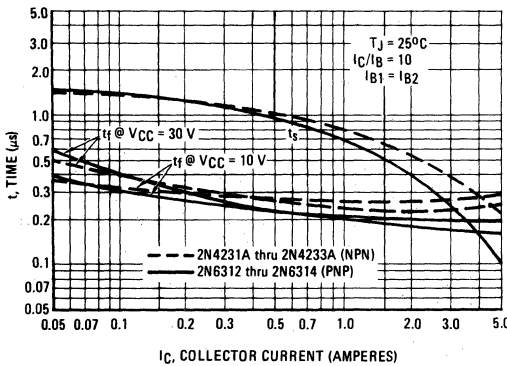
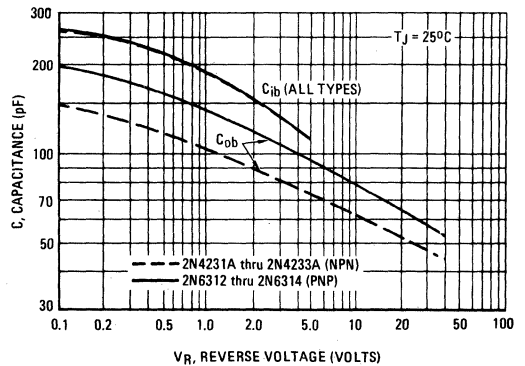


FIGURE 7 - CAPACITANCE



3

FIGURE 8 - DC CURRENT GAIN

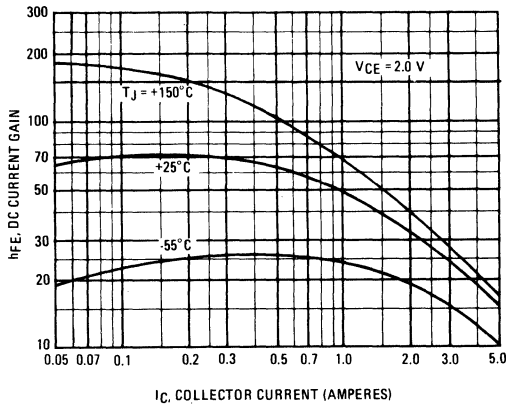


FIGURE 9 - COLLECTOR SATURATION REGION

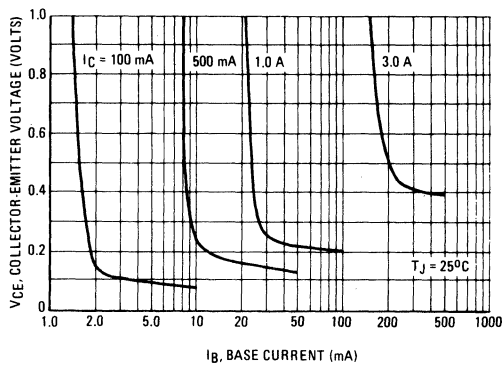
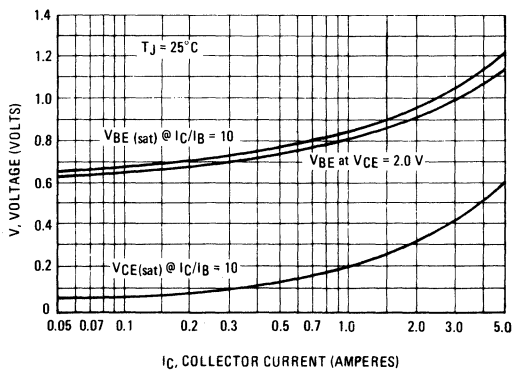


FIGURE 10 - "ON" VOLTAGES



3

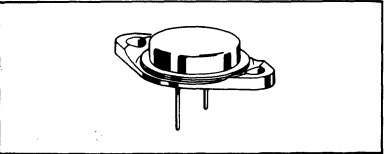
PNP SILICON HIGH-POWER TRANSISTORS

... designed for use in power amplifier and switching circuits.

- Low Collector-Emitter Saturation Voltage —
 $I_C = 15 \text{ Adc}, V_{CE(sat)} = 1.0 \text{ Vdc (Max) 2N4398,99}$
 $= 1.5 \text{ Vdc (Max) 2N5745}$
- DC Current Gain Specified — 1.0 to 30 Adc
- Complements to NPN 2N5301, 2N5302, 2N5303

20, 30 AMPERE
POWER TRANSISTORS
PNP SILICON

40-60-180 VOLTS
200 WATTS



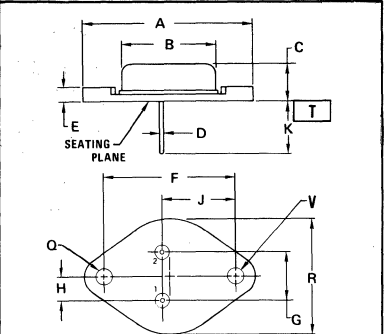
***MAXIMUM RATINGS**

Rating	Symbol	2N4398	2N4399	2N5745	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous	I_C	30	30	20	Adc
Peak		50	50	50	
Base Current — Continuous	I_B	7.5			Adc
Peak		15			
Total Device Dissipation @ $T_A = 25^\circ\text{C}^{**}$	P_D	5.0			Watts
Derate above 25°C		28.6			mW/°C
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	200			Watts
Derate above 25°C		1.15			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	35	°C/W

* Indicates JEDEC Registered Data
 ** Motorola guarantees this data in addition to JEDEC Registered Data.



STYLE 1: PIN 1. BASE
 STYLE 3: PIN 1. ANODE
 PIN 2. EMITTER
 PIN 2. CATHODE
 CASE: COLLECTOR

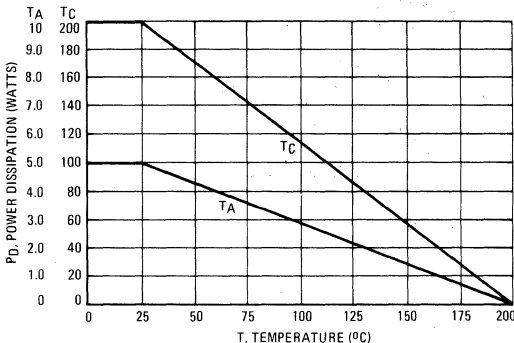
- NOTES:
- DIAMETERS Q, V AND SURFACE T ARE DATUMS.
 - POSITIONAL TOLERANCE FOR HOLE Q:
 $\text{HOLE Q: } \text{H} \text{ } \phi 0.25 (0.010) \text{ } \text{M} \text{ } \text{T} \text{ } \text{V} \text{ } \text{Q}$
 - POSITIONAL TOLERANCE FOR LEADS:
 $\text{LEADS: } \text{H} \text{ } \phi 0.30 (0.012) \text{ } \text{M} \text{ } \text{T} \text{ } \text{V} \text{ } \text{Q} \text{ } \text{Q}$
 - DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.560
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	30.15	BSC	1.187	BSC
G	10.92	BSC	0.430	BSC
H	5.46	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

3

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 13. All limits are applicable and must be observed.

2N4398, 2N4399, 2N5745

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 200\text{ mAdc}, I_B = 0$)	2N4398 2N4399 2N5745	$V_{CE(sus)}$	40 60 80	Vdc
Collector Cutoff Current ($V_{CE} = 40\text{ Vdc}, I_B = 0$) ($V_{CE} = 60\text{ Vdc}, I_B = 0$) ($V_{CE} = 80\text{ Vdc}, I_B = 0$)	2N4398 2N4399 2N5745	I_{CEO}	— — —	5.0 5.0 5.0 mAdc
Collector Cutoff Current ($V_{CE} = 40\text{ Vdc}, V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 60\text{ Vdc}, V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 80\text{ Vdc}, V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 30\text{ Vdc}, V_{BE(off)} = 1.5\text{ Vdc}, T_C = 150^\circ\text{C}$) ($V_{CE} = 80\text{ Vdc}, V_{BE(off)} = 1.5\text{ Vdc}, T_C = 150^\circ\text{C}$)	2N4398 2N4399 2N5745 2N4398, 2N4399 2N5745	I_{CEX}	— — — — —	5.0 5.0 5.0 10 10 mAdc
Collector Cutoff Current ($V_{CB} = 40\text{ Vdc}, I_E = 0$) ($V_{CB} = 60\text{ Vdc}, I_E = 0$) ($V_{CB} = 80\text{ Vdc}, I_E = 0$)	2N4398 2N4399 2N5745	I_{CBO}	— — —	1.0 1.0 1.0 mAdc
Emitter Cutoff Current ($V_{EB} = 5.0\text{ Vdc}, I_C = 0$)		I_{EBO}	—	5.0 mAdc
ON CHARACTERISTICS				
DC Current Gain (1) ($I_C = 1.0\text{ Adc}, V_{CE} = 2.0\text{ Vdc}$) ($I_C = 10\text{ Adc}, V_{CE} = 2.0\text{ Vdc}$) ($I_C = 15\text{ Adc}, V_{CE} = 2.0\text{ Vdc}$) ($I_C = 20\text{ Adc}, V_{CE} = 2.0\text{ Vdc}$) ($I_C = 30\text{ Adc}, V_{CE} = 4.0\text{ Vdc}$)	All Types 2N5745 2N4398, 2N4399 2N5745 2N4398, 2N4399	h_{FE}	40 15 15 5.0 5.0	— 60 60 — —
Collector-Emitter Saturation Voltage (1) ($I_C = 10\text{ Adc}, I_B = 1.0\text{ Adc}$) ($I_C = 15\text{ Adc}, I_B = 1.5\text{ Adc}$) ($I_C = 20\text{ Adc}, I_B = 2.0\text{ Adc}$) ($I_C = 20\text{ Adc}, I_B = 4.0\text{ Adc}$) ($I_C = 30\text{ Adc}, I_B = 6.0\text{ Adc}$)	2N4398, 2N4399 2N5745 2N4398, 2N4399 2N5745 2N4398, 2N4399	$V_{CE(sat)}$	— — — — —	0.75 1.0 1.0 1.5 2.0 2.0 4.0 Vdc
Base-Emitter Saturation Voltage (1) ($I_C = 10\text{ Adc}, I_B = 1.0\text{ Adc}$)** ($I_C = 15\text{ Adc}, I_B = 1.5\text{ Adc}$) ($I_C = 20\text{ Adc}, I_B = 2.0\text{ Adc}$)** ($I_C = 20\text{ Adc}, I_B = 4.0\text{ Adc}$)	2N4398, 2N4399 2N5745 2N4398, 2N4399 2N5745 2N4398, 2N4399 2N5745	$V_{BE(sat)}$	— — — — —	1.6 1.7 1.85 2.0 2.5 2.5 Vdc
Base-Emitter On Voltage (1) ($I_C = 10\text{ Adc}, V_{CE} = 2.0\text{ Vdc}$) ($I_C = 15\text{ Adc}, V_{CE} = 2.0\text{ Vdc}$) ($I_C = 20\text{ Adc}, V_{CE} = 4.0\text{ Vdc}$) ($I_C = 30\text{ Adc}, V_{CE} = 4.0\text{ Vdc}$)	2N5745 2N4398, 2N4399 2N5745 2N4398, 2N4399	$V_{BE(on)}$	— — — —	1.5 1.7 2.5 3.0 Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain Bandwidth Product (2) ($I_C = 1.0\text{ Adc}, V_{CE} = 10\text{ Vdc}, f = 1.0\text{ MHz}$)	2N4398, 2N4399 2N5745	f_T	4.0 2.0	— — MHz
Small-Signal Current Gain ($I_C = 1.0\text{ Adc}, V_{CE} = 10\text{ Vdc}, f = 1.0\text{ kHz}$)		h_{fe}	40	—
SWITCHING CHARACTERISTICS				
Rise Time	2N4398, 2N4399 2N5745	t_r	— —	0.4 1.0 μs
Storage Time	($V_{CC} = 30\text{ Vdc}, I_C = 10\text{ Adc}, I_{B1} = I_{B2} = 1.0\text{ Adc}$) 2N4398, 2N4399 2N5745	t_s	— —	1.5 2.0 μs
Fall Time	2N4398, 2N4399 2N5745	t_f	— —	0.6 1.0 μs

*Indicates JEDEC Registered Data.
 **Motorola Guarantees this Data in Addition to JEDEC Registered Data.
 (1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.
 (2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.



SWITCHING TIME EQUIVALENT TEST CIRCUITS

FIGURE 2 – TURN-ON TIME

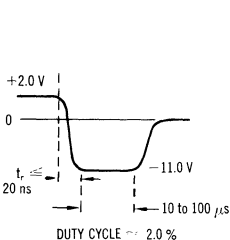
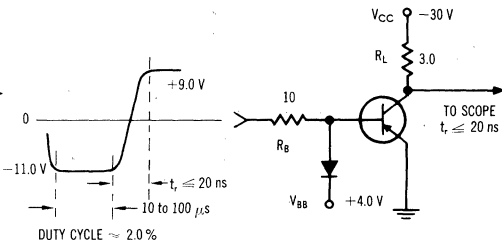


FIGURE 3 – TURN-OFF TIME



TYPICAL "ON" REGION CHARACTERISTICS

FIGURE 4 - DC CURRENT GAIN

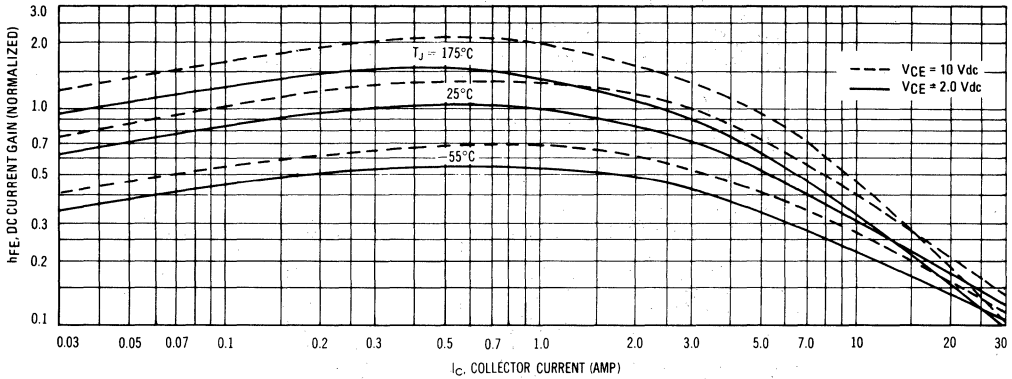


FIGURE 5 - COLLECTOR SATURATION REGION

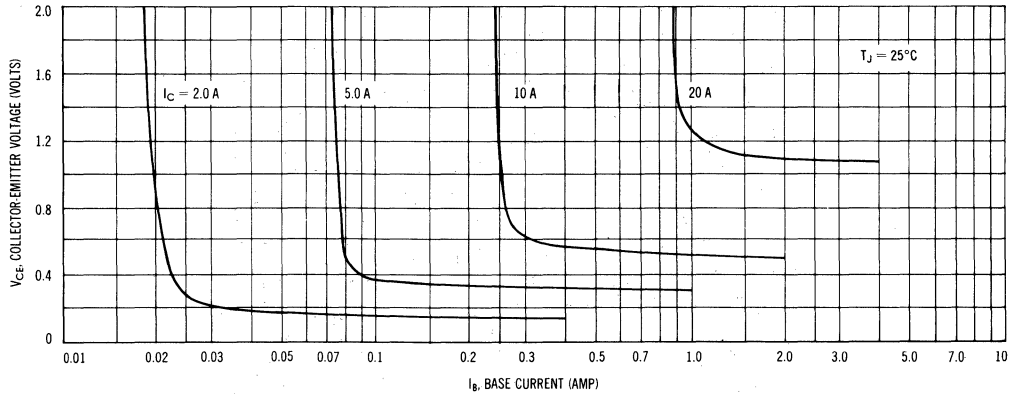


FIGURE 6 - "ON" VOLTAGES

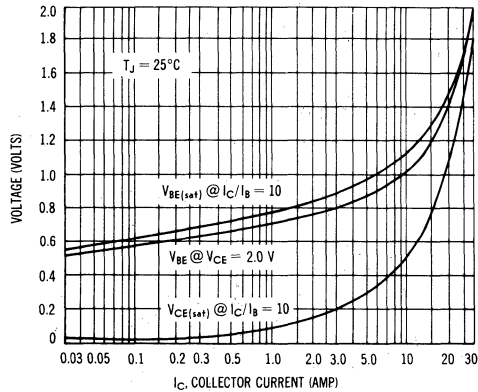
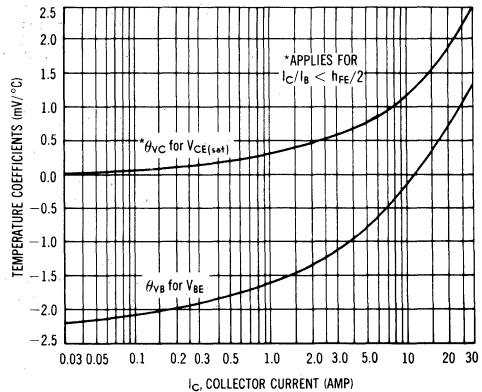


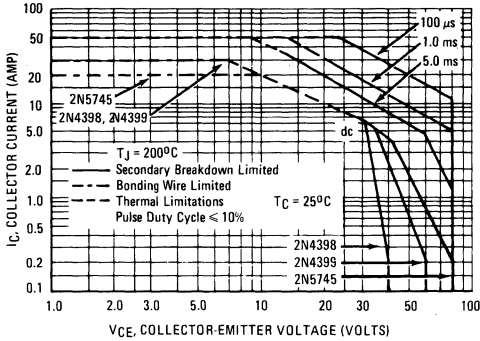
FIGURE 7 - TEMPERATURE COEFFICIENTS



3

RATINGS AND THERMAL DATA

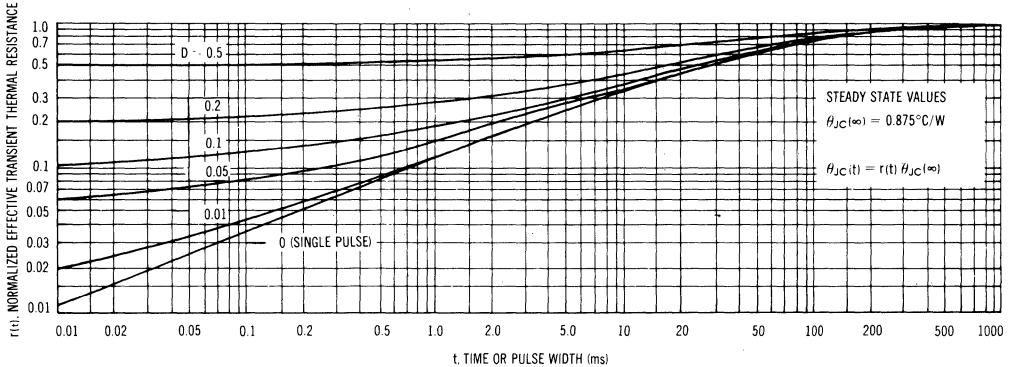
FIGURE 8 – ACTIVE REGION SAFE OPERATING AREA



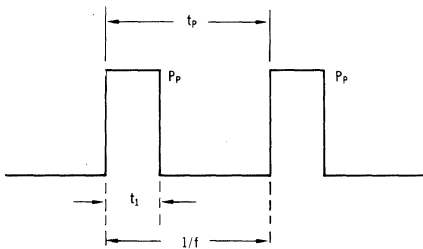
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 8 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 9 – THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



DUTY CYCLE $D = t_p f$
 PEAK PULSE POWER P_p

A train of periodical power pulses can be represented by the model as shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 9 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 9 by the steady state value $\theta_{JC}(\infty)$.

Example:

The 2N4398 is dissipating 100 watts under the following conditions: $t_1 = 1.0$ ms, $t_p = 5.0$ ms. ($D = 0.2$)

Using Figure 9, at a pulse width of 1.0 ms and $D = 0.2$, the reading of $r(t)$ is 0.28.

The peak rise in junction temperature is therefore
 $\Delta T = r(t) \times P_p \times \theta_{JC}(\infty) = 0.28 \times 100 \times 0.875 = 24.5^\circ\text{C}$

2N4898
thru
2N4900

MEDIUM-POWER PNP SILICON TRANSISTORS

... designed for driver circuits, switching, and amplifier applications. These high-performance devices feature:

- Low Saturation Voltage – $V_{CE(sat)} = 0.6\text{ V max @ } I_C = 1.0\text{ Amp}$
- Excellent Safe Operating Area
- Gain Specified to $I_C = 1.0\text{ Ampere}$
- 2N4900 Complementary to NPN 2N4912

4 AMPERE

GENERAL PURPOSE
POWER TRANSISTORS

40-80 VOLTS
25 WATTS

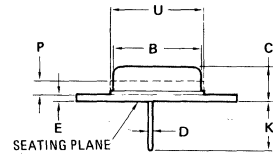
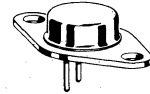
MAXIMUM RATINGS

Rating	Symbol	2N4898	2N4899	2N4900	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous*	I_C^*	← 1.0 →			Adc
		← 4.0 →			
Base Current	I_B	← 1.0 →			Adc
Total Device Dissipation $T_C = 25^\circ\text{C}$	P_D	← 25 →			Watts
Derate above 25°C		← 0.143 →			W/ $^\circ\text{C}$
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			$^\circ\text{C}$

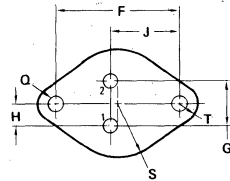
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	7.0	$^\circ\text{C/W}$

*The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements.
The 4.0 Amp maximum value is based upon actual current-handling capability of the device (see Figure 5).



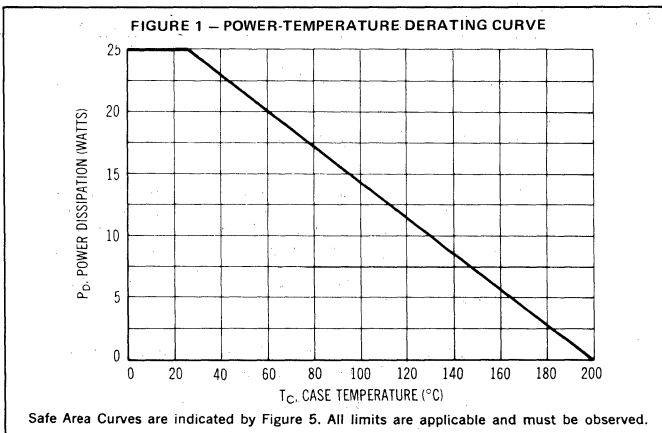
STYLE 1:
PIN 1, BASE
2, EMITTER
CASE: COLLECTOR



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC Dimensions and Notes Apply.

CASE 80-02
TO-213AA



2N4898 thru 2N4900

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage* (I _C = 0.1 Adc, I _B = 0)	V _{CEO(sus)} *	40 60 80	- - -	Vdc
Collector Cutoff Current (V _{CE} = 20 Vdc, I _B = 0) (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 40 Vdc, I _B = 0)	I _{CEO}	- - -	0.5 0.5 0.5	mAcd
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , V _{BE(off)} = 1.5 Vdc) (V _{CE} = Rated V _{CEO} , V _{BE(off)} = 1.5 Vdc, T _C = 150°C)	I _{CEX}	- -	0.1 1.0	mAcd
Collector Cutoff Current (V _{CB} = Rated V _{CB} , I _E = 0)	I _{CBO}	-	0.1	mAcd
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	-	1.0	mAcd

ON CHARACTERISTICS

DC Current Gain* (I _C = 50 mAcd, V _{CE} = 1.0 Vdc) (I _C = 500 mAcd, V _{CE} = 1.0 Vdc) (I _C = 1.0 Adc, V _{CE} = 1.0 Vdc)	h _{FE} *	40 20 10	- 100 -	-
Collector-Emitter Saturation Voltage* (I _C = 1.0 Adc, I _B = 0.1 Adc)	V _{CE(sat)} *	-	0.6	Vdc
Base-Emitter Saturation Voltage* (I _C = 1.0 Adc, I _B = 0.1 Adc)	V _{BE(sat)} *	-	1.3	Vdc
Base-Emitter On Voltage* (I _C = 1.0 Adc, V _{CE} = 1.0 Vdc)	V _{BE(on)} *	-	1.3	Vdc

SMALL SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product (I _C = 250 mAcd, V _{CE} = 10 Vdc, f = 1.0 MHz)	f _T	3.0	-	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 100 kHz)	C _{ob}	-	100	pF
Small-Signal Current Gain (I _C = 250 mAcd, V _{CE} = 10 Vdc, f = 1.0 kHz)	h _{fe}	25	-	-

* Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%

FIGURE 2 - SWITCHING TIME EQUIVALENT CIRCUIT

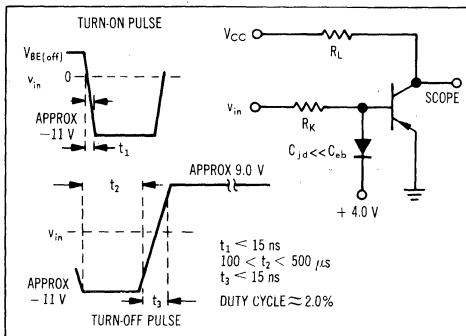


FIGURE 3 - TURN-ON TIME

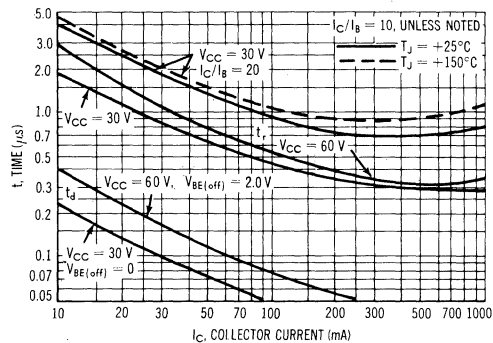


FIGURE 4 - THERMAL RESPONSE

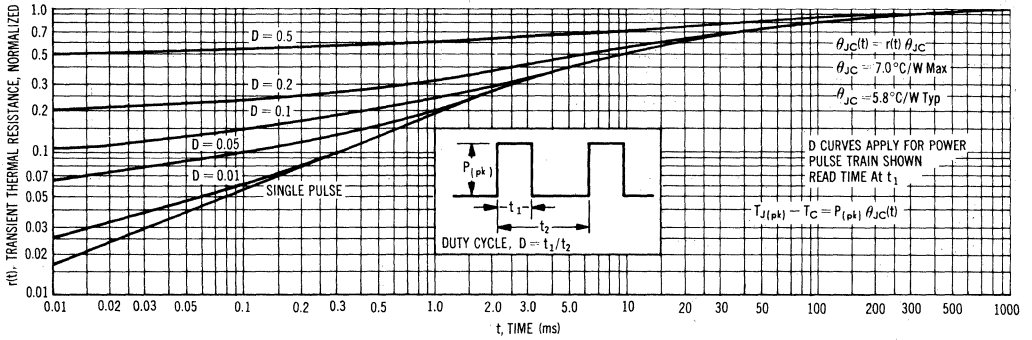
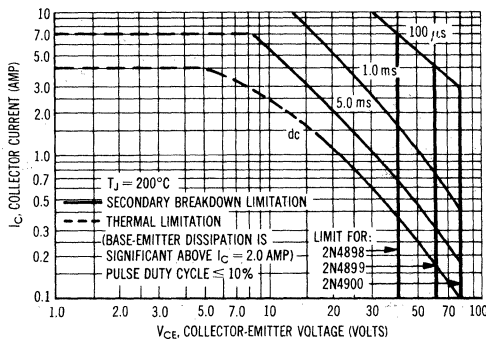


FIGURE 5 - ACTIVE-REGION SAFE OPERATING AREA



The safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor which must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 5 is based upon $T_{J(pk)} = 200^{\circ}\text{C}$; T_C is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \approx 200^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power which can be handled to values less than the limitations imposed by secondary breakdown.

3

FIGURE 6 - STORAGE TIME

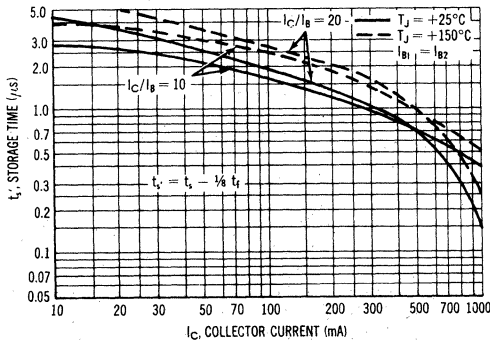
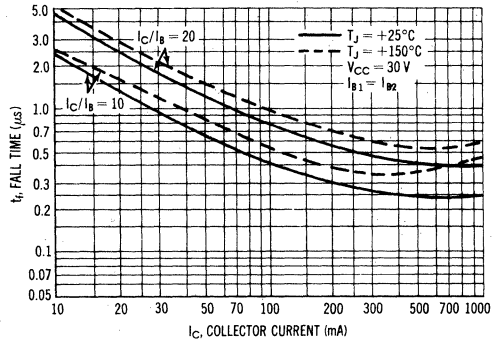


FIGURE 7 - FALL TIME



2N4912

NPN SILICON TRANSISTOR

... designed for driver circuits, switching, and amplifier applications.
 This high-performance device features:

- Low Saturation Voltage – $V_{CE(sat)} = 0.6 \text{ V max @ } I_C = 1.0 \text{ Amp}$
- Excellent Safe Operating Area
- Gain Specified to $I_C = 1.0 \text{ Amp}$
- Complement to PNP 2N4900

1 AMPERE
NPN SILICON
POWER TRANSISTOR

80 VOLTS
25 WATTS

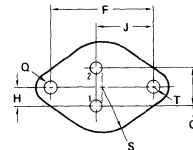
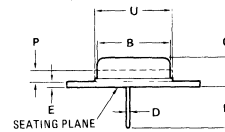
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous*	I_C^*	1.0	Adc
Base Current – Continuous	I_B	1.0	Adc
Total Device Dissipation $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	25 0.143	Watts mW/ $^\circ\text{C}$
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.0	$^\circ\text{C/W}$

*The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements.



STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

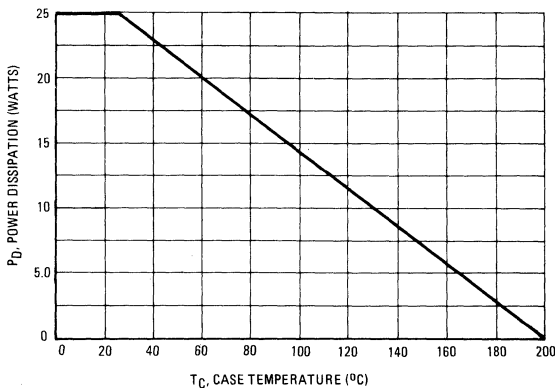
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC Dimensions and Notes Apply.

CASE 80-02
TO-213AA

3

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 0.1 \text{ Adc}, I_B = 0$)	$V_{CE(sus)}$	80	—	Vdc
Collector Cutoff Current ($V_{CE} = 40 \text{ Vdc}, I_B = 0$)	I_{CEO}	—	0.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CE0}, V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CE0}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)	I_{CEX}	—	0.1 1.0	mAdc
Collector Cutoff Current ($V_{CB} = \text{Rated } V_{CB}, I_E = 0$)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current ($V_{EB} = 5.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 50 \text{ mAdc}, V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}, V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}, V_{CE} = 1.0 \text{ Vdc}$)	h_{FE}	40 20 10	— 100 —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0 \text{ Adc}, I_B = 0.1 \text{ Adc}$)	$V_{CE(sat)}$	—	0.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0 \text{ Adc}, I_B = 0.1 \text{ Adc}$)	$V_{BE(sat)}$	—	1.3	Vdc
Base-Emitter On Voltage ($I_C = 1.0 \text{ Adc}, V_{CE} = 1.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product ($I_C = 250 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$)	f_T	3.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 100 \text{ kHz}$)	C_{ob}	—	100	pF
Small-Signal Current Gain ($I_C = 250 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}$)	h_{fe}	25	—	

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2.0%.

3

FIGURE 2 — SWITCHING TIME EQUIVALENT CIRCUIT

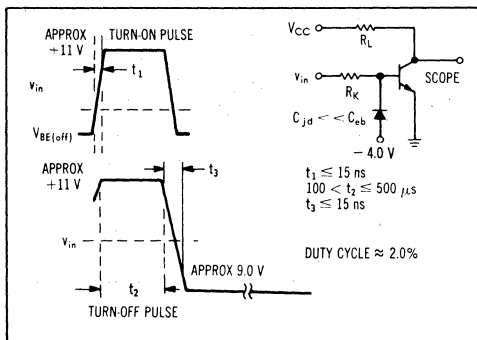


FIGURE 3 — TURN-ON TIME

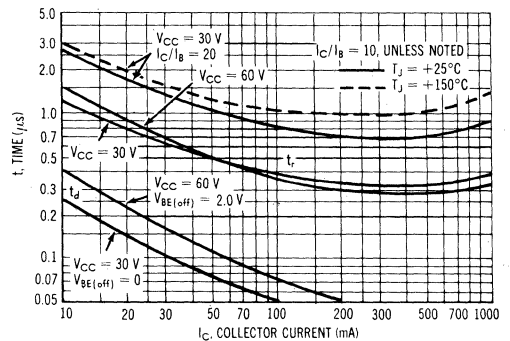


FIGURE 4 - THERMAL RESPONSE

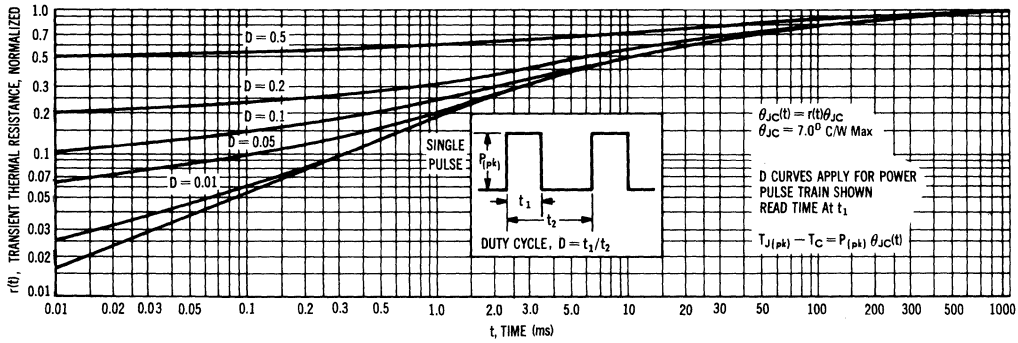
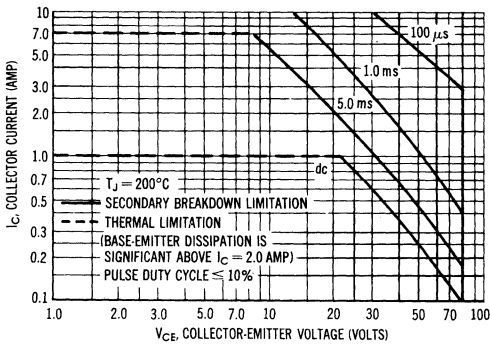


FIGURE 5 - ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}\text{C}$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 - STORAGE TIME

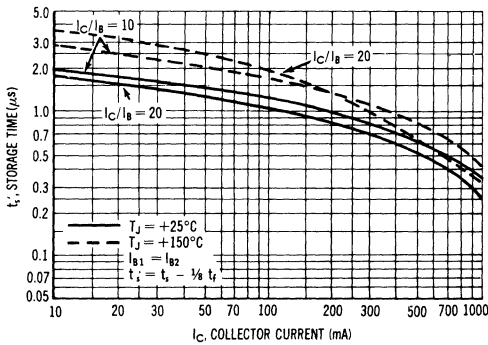
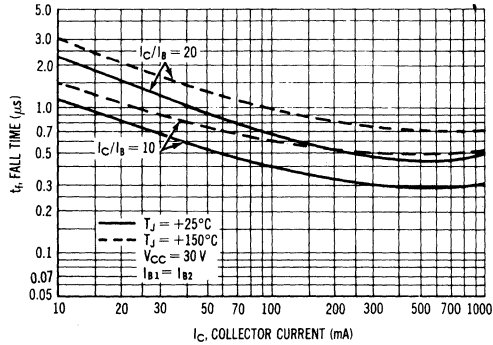


FIGURE 7 - FALL TIME



2N4918
thru
2N4920

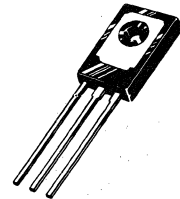
MEDIUM-POWER PLASTIC PNP SILICON TRANSISTORS

... designed for driver circuits, switching, and amplifier applications. These high-performance plastic devices feature:

- Low Saturation Voltage – $V_{CE(sat)} = 0.6 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Amp}$
- Excellent Power Dissipation Due to Thermopad Construction – $P_D = 30 \text{ @ } T_C = 25^\circ\text{C}$
- Excellent Safe Operating Area
- Gain Specified to $I_C = 1.0 \text{ Amp}$
- Complement to NPN 2N4921, 2N4922, 2N4923

3 AMPERE
GENERAL-PURPOSE
POWER TRANSISTORS

40-80 VOLTS
30 WATTS



***MAXIMUM RATINGS**

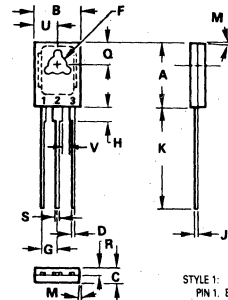
Ratings	Symbol	2N4918	2N4919	2N4920	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous (1)	I_C^*	← 1.0 →			Adc
		← 3.0 →			
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	30			Watts W/ $^\circ\text{C}$
		0.24			
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			$^\circ\text{C}$

THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data for 2N4918 Series

- (1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current-handling capability of the device (See Figure 5).
- (2) Recommend use of thermal compound for lowest thermal resistance.



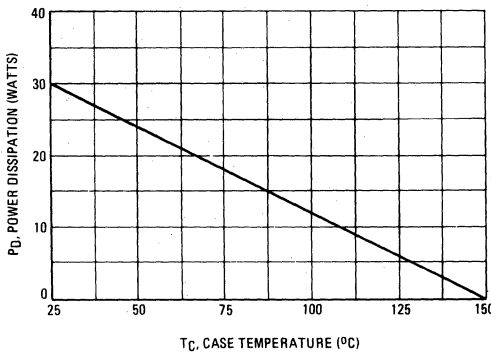
STYLE 1: PIN 1, EMITTER
 2, COLLECTOR
 3, BASE

NOTES:
 1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.025
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3" TYP		3" TYP	
Q	3.75	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-225AA

FIGURE 1 – POWER DERATING



2N4918 thru 2N4920

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 0.1 \text{ Adc}, I_B = 0$)	2N4918 2N4919 2N4920	$V_{CE(sus)}$	40 60 80	— — —	Vdc
Collector Cutoff Current ($V_{CE} = 20 \text{ Vdc}, I_B = 0$) ($V_{CE} = 30 \text{ Vdc}, I_B = 0$) ($V_{CE} = 40 \text{ Vdc}, I_B = 0$)	2N4918 2N4919 2N4920	I_{CEO}	— — —	0.5 0.5 0.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEO}, V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CEO}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$)		I_{CEX}	— —	0.1 0.5	mAdc
Collector Cutoff Current ($V_{CB} = \text{Rated } V_{CB}, I_E = 0$)		I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)		I_{EBO}	—	1.0	mAdc

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 50 \text{ mAdc}, V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}, V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}, V_{CE} = 1.0 \text{ Vdc}$)		h_{FE}	40 30 10	— 150 —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 1.0 \text{ Adc}, I_B = 0.1 \text{ Adc}$)		$V_{CE(sat)}$	—	0.6	Vdc
Base-Emitter Saturation Voltage (1) ($I_C = 1.0 \text{ Adc}, I_B = 0.1 \text{ Adc}$)		$V_{BE(sat)}$	—	1.3	Vdc
Base-Emitter On Voltage (1) ($I_C = 1.0 \text{ Adc}, V_{CE} = 1.0 \text{ Vdc}$)		$V_{BE(on)}$	—	1.3	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain – Bandwidth Product ($I_C = 250 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$)		f_T	3.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 100 \text{ kHz}$)		C_{ob}	—	100	pF
Small-Signal Current Gain ($I_C = 250 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}$)		h_{fe}	25	—	—

*Indicates JEDEC Registered Data

(1) Pulse Test: $PW \approx 300 \mu\text{s}$, Duty Cycle $\approx 2.0\%$

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

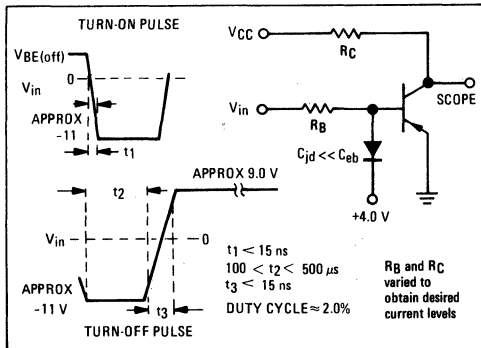


FIGURE 3 – TURN-ON TIME

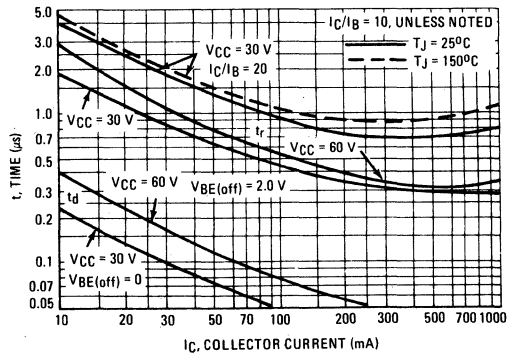


FIGURE 4 - THERMAL RESPONSE

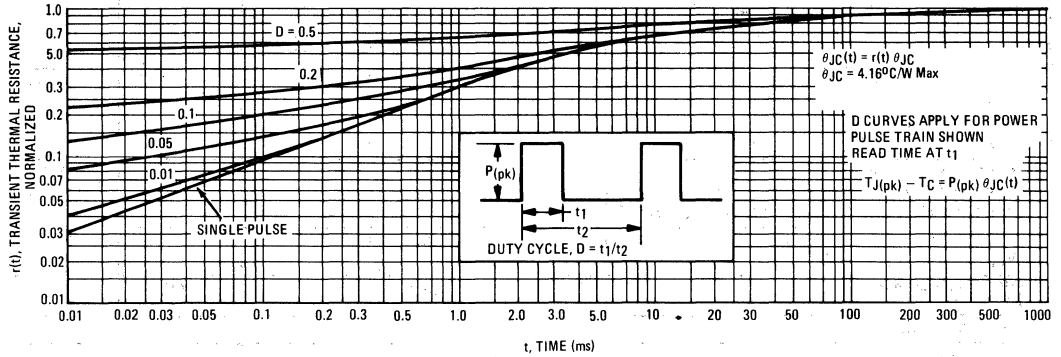
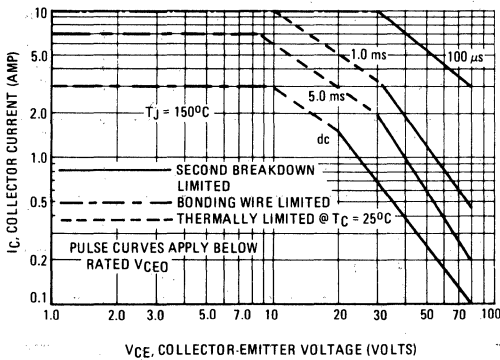


FIGURE 5 - ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 - STORAGE TIME

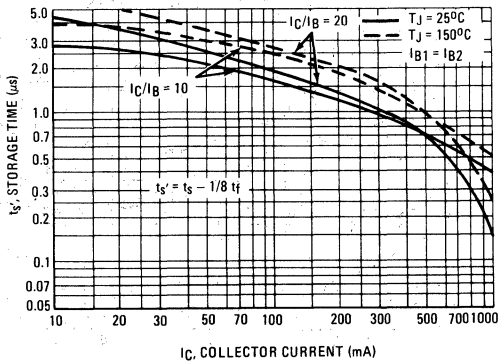
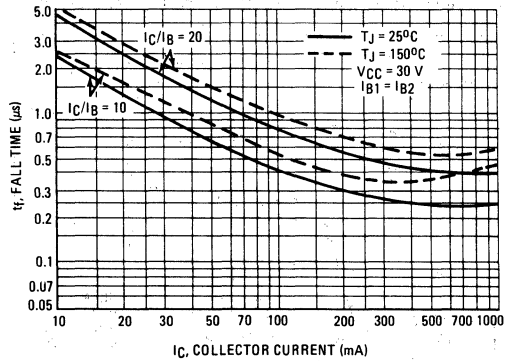


FIGURE 7 - FALL TIME



TYPICAL DC CHARACTERISTICS

FIGURE 8 – CURRENT GAIN

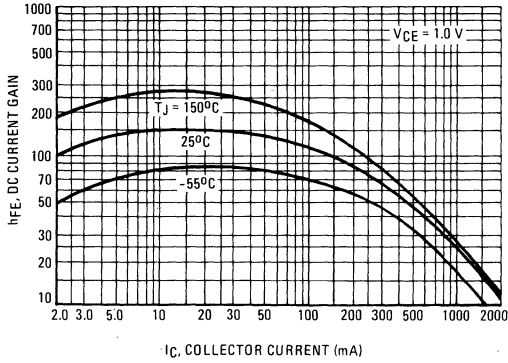


FIGURE 9 – COLLECTOR SATURATION REGION

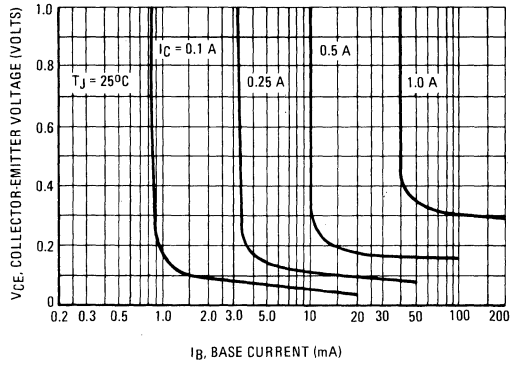


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

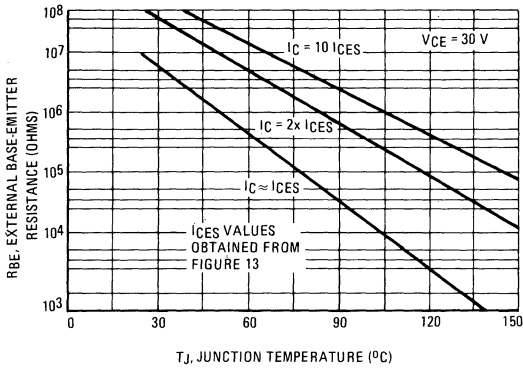


FIGURE 11 – "ON" VOLTAGE

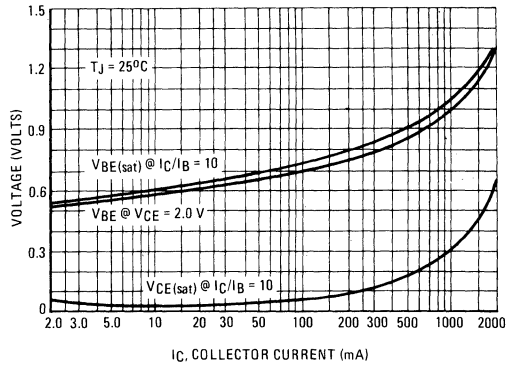


FIGURE 12 – COLLECTOR CUTOFF REGION

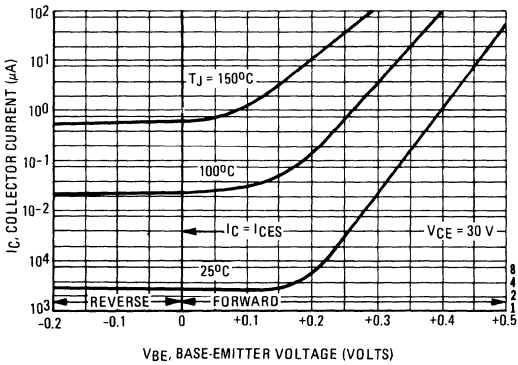
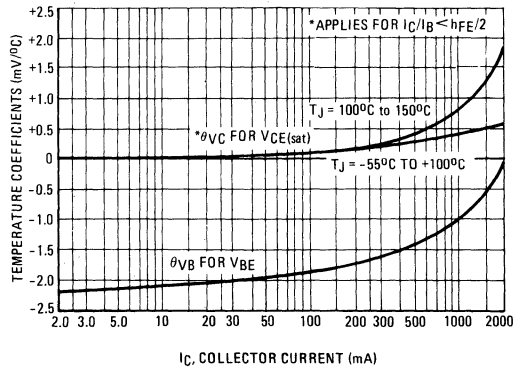


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N4921
thru
2N4923

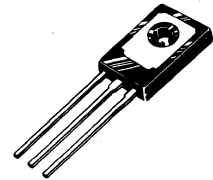
MEDIUM-POWER PLASTIC NPN SILICON TRANSISTORS

... designed for driver circuits, switching, and amplifier applications. These high-performance plastic devices feature:

- Low Saturation Voltage — $V_{CE(sat)} = 0.6 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Amp}$
- Excellent Power Dissipation Due to Thermopad Construction — $P_D = 30 \text{ W @ } T_C = 25^\circ\text{C}$
- Excellent Safe Operating Area
- Gain Specified to $I_C = 1.0 \text{ Amp}$
- Complement to PNP 2N4918, 2N4919, 2N4920

3 AMPERE
GENERAL-PURPOSE
POWER TRANSISTORS

40-80 VOLTS
30 WATTS



***MAXIMUM RATINGS**

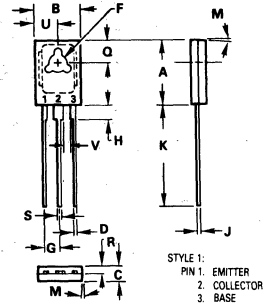
Rating	Symbol	2N4921	2N4922	2N4923	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current - Continuous (1)	I_C	← 1.0 →			Adc
		← 3.0 →			
Base Current - Continuous	I_B	← 1.0 →			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	30			Watts
Derate above 25°C		0.24			Watts/ $^\circ\text{C}$
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			$^\circ\text{C}$

THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16 $^\circ\text{C/W}$

- (1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current-handling capability of the device (see Figures 5 and 6).
- (2) Recommend use of thermal compound for lowest thermal resistance.

*Indicates JEDEC Registered Data.

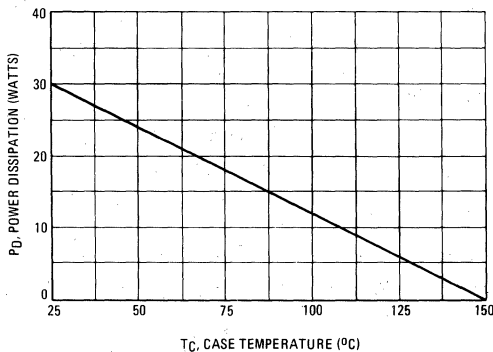


- NOTES:
 1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	15.63	0.575	0.615
M	3 TYP		3 TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-225AA

FIGURE 1 — POWER DERATING



2N4921 thru 2N4923

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 0.1 Adc, I _B = 0)	V _{CEO(sus)}	40	—	Vdc
2N4921		60	—	
2N4922		80	—	
2N4923				
Collector Cutoff Current (V _{CE} = 20 Vdc, I _B = 0)	I _{CEO}	—	0.5	mAdc
2N4921		—	0.5	
2N4922		—	0.5	
2N4923		—	0.5	
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , V _{EB(off)} = 1.5 Vdc)	I _{CEX}	—	0.1	mAdc
(V _{CE} = Rated V _{CEO} , V _{EB(off)} = 1.5 Vdc, T _C = 125°C)		—	0.5	
Collector Cutoff Current (V _{CB} = Rated V _{CB} , I _E = 0)	I _{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V _{EB} = 5.0 Vdc, I _C = 0)	I _{EBO}	—	1.0	mAdc

ON CHARACTERISTICS

DC Current Gain (1) (I _C = 50 mAdc, V _{CE} = 1.0 Vdc)	h _{FE}	40	—	—
(I _C = 500 mAdc, V _{CE} = 1.0 Vdc)		30	150	
(I _C = 1.0 Adc, V _{CE} = 1.0 Vdc)		10	—	
Collector-Emitter Saturation Voltage (1) (I _C = 1.0 Adc, I _B = 0.1 Adc)	V _{CE(sat)}	—	0.6	Vdc
Base-Emitter Saturation Voltage (1) (I _C = 1.0 Adc, I _B = 0.1 Adc)	V _{BE(sat)}	—	1.3	Vdc
Base-Emitter On Voltage (1) (I _C = 1.0 Adc, V _{CE} = 1.0 Vdc)	V _{BE(on)}	—	1.3	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain – Bandwidth Product (I _C = 250 mAdc, V _{CE} = 10 Vdc, f = 1.0 MHz)	f _T	3.0	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 100 kHz)	C _{ob}	—	100	pF
Small-Signal Current Gain (I _C = 250 mAdc, V _{CE} = 10 Vdc, f = 1.0 kHz)	h _{fe}	25	—	—

(1) Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%.
*Indicates JEDEC Registered Data

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

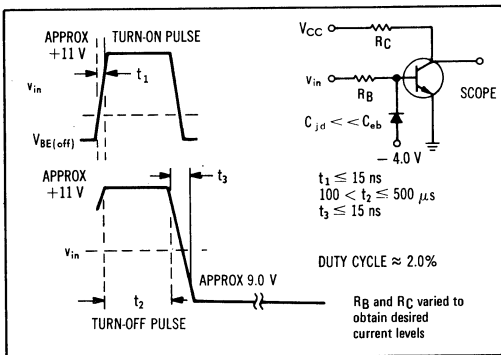


FIGURE 3 – TURN-ON TIME

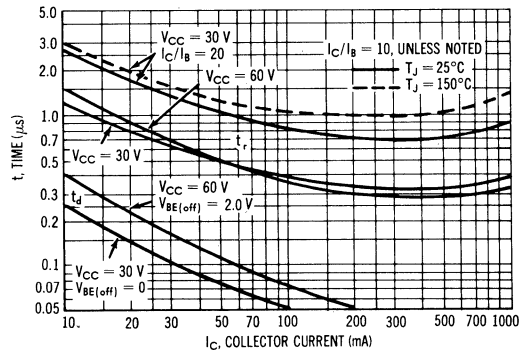


FIGURE 4 - THERMAL RESPONSE

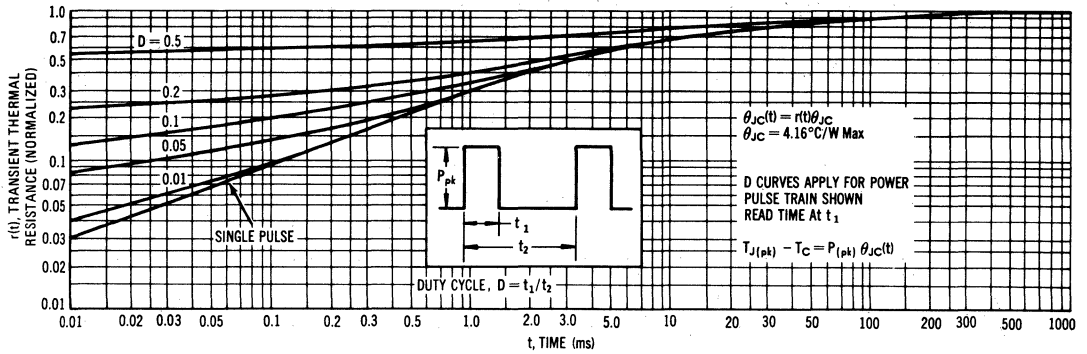
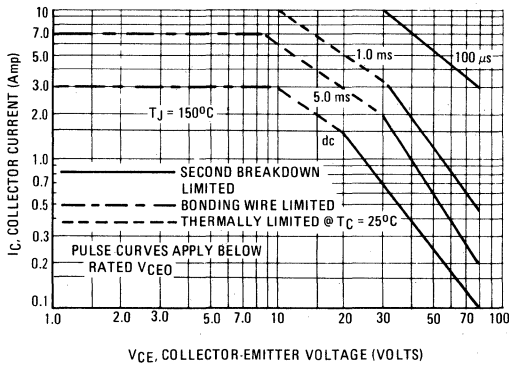


FIGURE 5 - ACTIVE - REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 - STORAGE TIME

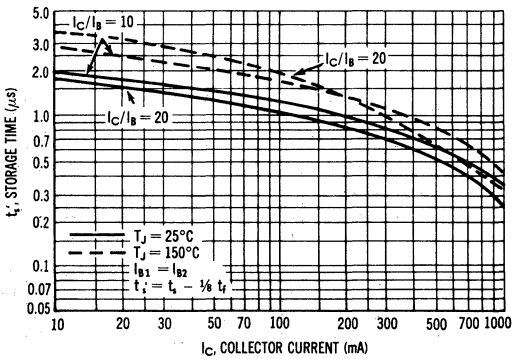
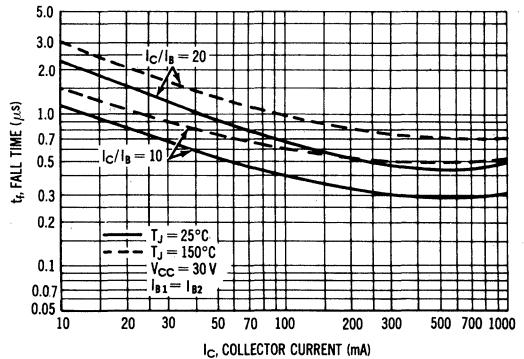


FIGURE 7 - FALL TIME



3

FIGURE 8 – CURRENT GAIN

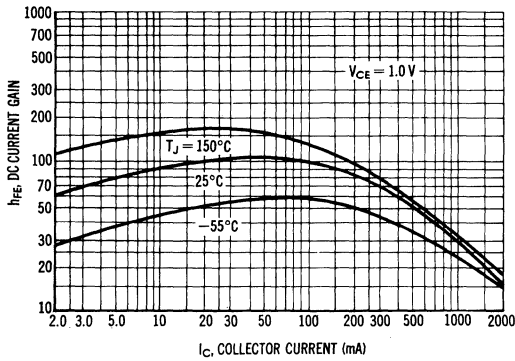


FIGURE 9 – COLLECTOR SATURATION REGION

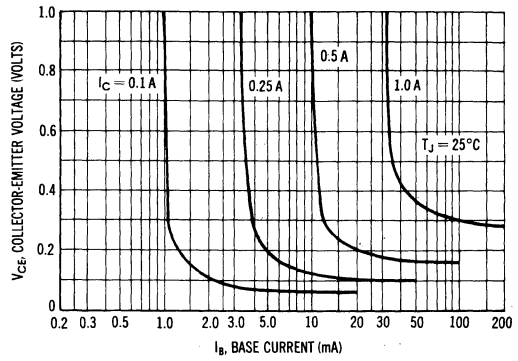


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

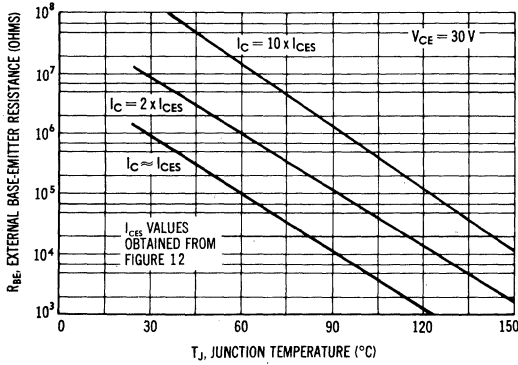


FIGURE 11 – "ON" VOLTAGE

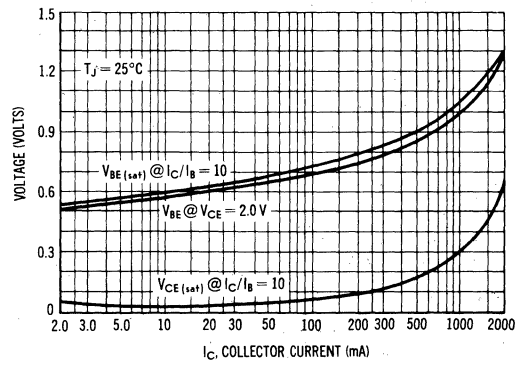


FIGURE 12 – COLLECTOR CUTOFF REGION

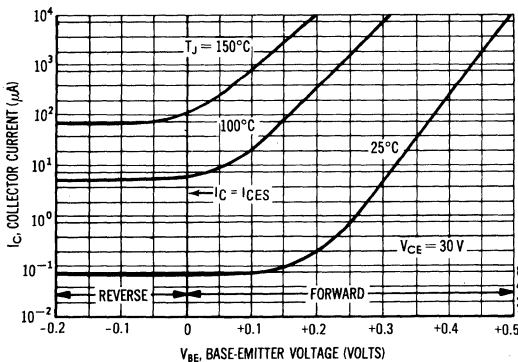
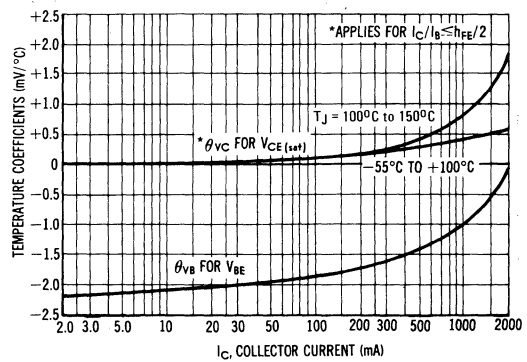


FIGURE 13 – TEMPERATURE COEFFICIENTS



NPN SILICON TRANSISTORS

... fast switching speeds and high current capacity ideally suit these parts for use in switching regulators, inverters, wide-band amplifiers and power oscillators in industrial and commercial applications.

- High Speed — $t_f = 0.5 \mu s$ (Max)
- High Current — $I_{C(max)} = 30$ Amps
- Low Saturation — $V_{CE(sat)} = 2.5$ V (Max) @ $I_C = 20$ Amps

20 AMPERE

NPN SILICON
POWER TRANSISTORS

75 and 90 VOLTS
140 WATTS

***MAXIMUM RATINGS**

Rating	Symbol	2N5038	2N5039	Unit
Collector-Base Voltage	V_{CBO}	150	120	Vdc
Collector-Emitter Voltage	V_{CEV}	150	120	Vdc
Emitter-Base Voltage	V_{EBO}	7		Vdc
Collector Current — Continuous	I_C	20		Adc
Peak (1)	I_{CM}	30		
Base Current — Continuous	I_B	5		Adc
Total Device Dissipation @ $T_C = 25^\circ C$	P_D	140		Watts
Derate above $25^\circ C$		0.8		W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^\circ C/W$

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width < 10 ms, Duty Cycle $\leq 50\%$.

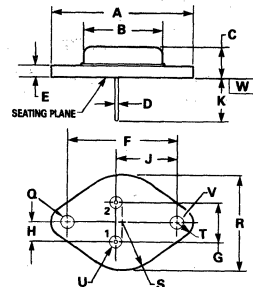
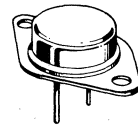
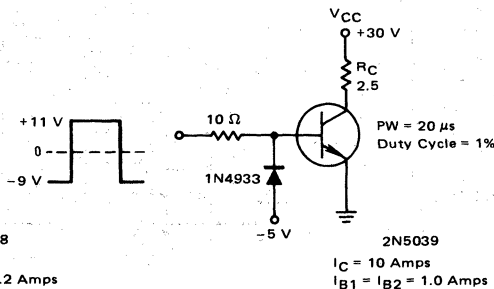


FIGURE 1 — SWITCHING TIME TEST CIRCUIT



STYLE 1

PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:

1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

CASE 1-04
TO-204AA

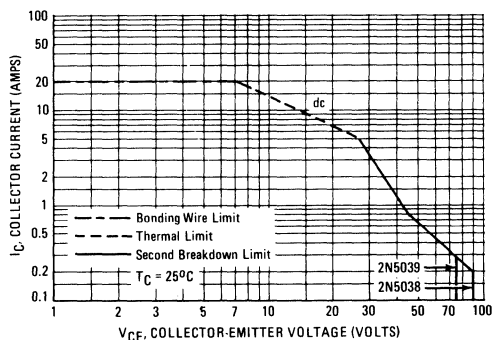
***ELECTRICAL CHARACTERISTICS** ($T_C = 25^{\circ}\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mAdc}, I_B = 0$)	$V_{CE0(sus)}$	90	—	Vdc
2N5038		75	—	
2N5039				
Collector Cutoff Current ($V_{CE} = 140 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ V}$)	I_{CEX}	—	50	mAdc
2N5038		—	50	
($V_{CE} = 110 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ V}$)		—	50	
2N5039		—	50	
($V_{CE} = 100 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 150^{\circ}\text{C}$)		—	10	
2N5038		—	10	
($V_{CE} = 85 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 150^{\circ}\text{C}$)		—	10	
2N5039		—	10	
Emitter Cutoff Current ($V_{EB} = 5 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	5	mAdc
2N5038		—	5	
2N5039		—	15	
($V_{EB} = 7 \text{ Vdc}, I_C = 0$)		—	50	
Both		—	50	
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 12 \text{ Adc}, V_{CE} = 5 \text{ Vdc}$)	h_{FE}	20	100	—
2N5038		20	100	
($I_C = 10 \text{ Adc}, V_{CE} = 5 \text{ Vdc}$)		20	100	
2N5039				
Collector-Emitter Saturation Voltage ($I_C = 20 \text{ Adc}, I_B = 5 \text{ Adc}$)	$V_{CE(sat)}$	—	2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 20 \text{ Adc}, I_B = 5 \text{ Adc}$)	$V_{BE(sat)}$	—	3.3	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common-Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio ($I_C = 2 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 5 \text{ MHz}$)	$ h_{fe} $	12	—	—
SWITCHING CHARACTERISTICS				
RESISTIVE LOAD				
Rise Time	($V_{CC} = 30 \text{ Vdc}$)	t_r	—	0.5
Storage Time	($I_C = 12 \text{ Adc}, I_{B1} = I_{B2} = 1.2 \text{ Adc}$)	t_s	—	1.5
Fall Time	($I_C = 10 \text{ Adc}, I_{B1} = I_{B2} = 1 \text{ Adc}$)	t_f	—	0.5
	2N5038			μs
	2N5039			μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Second breakdown pulse limits are valid for duty cycles to 10%. At high case temperatures, thermal limitations may reduce the power that can be handled to values less than the limitations imposed by second breakdown.



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N5190
thru
2N5192

SILICON NPN POWER TRANSISTORS

... for use in power amplifier and switching circuits, — excellent safe area limits. Complement to PNP 2N5193, 2N5194, 2N5195

4 AMPERE
POWER TRANSISTORS
SILICON NPN

40-80 VOLTS
40 WATTS

*** MAXIMUM RATINGS**

Rating	Symbol	2N5190	2N5191	2N5192	Unit
Collector-Emitter Voltage	V _{CEO}	40	60	80	Vdc
Collector-Base Voltage	V _{CB}	40	60	80	Vdc
Emitter-Base Voltage	V _{EB}	5.0			Vdc
Collector Current	I _C	4.0			Adc
Base Current	I _B	1.0			Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	40	320		Watts mW/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ _{JC}	3.12	°C/W

*** ELECTRICAL CHARACTERISTICS (I_C = 25°C unless otherwise noted)**

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) (I _C = 0.1 Adc, I _B = 0)	V _{CEO(sus)}	40 60 80	— — —	Vdc
Collector Cutoff Current (V _{CE} = 40 Vdc, I _B = 0) (V _{CE} = 60 Vdc, I _B = 0) (V _{CE} = 80 Vdc, I _B = 0)	I _{CEO}	— — —	1.0 1.0 1.0	mA dc
Collector Cutoff Current (V _{CE} = 40 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 60 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 80 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 40 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 125°C) (V _{CE} = 60 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 125°C) (V _{CE} = 80 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 125°C)	I _{C EX}	— — — — — —	0.1 0.1 0.1 2.0 2.0 2.0	mA dc
Collector Cutoff Current (V _{CB} = 40 Vdc, I _E = 0) (V _{CB} = 60 Vdc, I _E = 0) (V _{CB} = 80 Vdc, I _E = 0)	I _{CBO}	— — —	0.1 0.1 0.1	mA dc
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	—	1.0	mA dc

ON CHARACTERISTICS

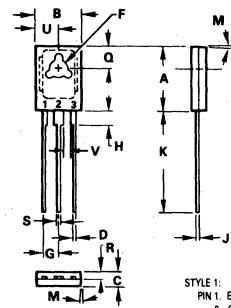
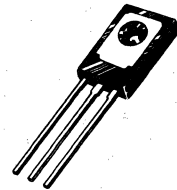
DC Current Gain (1) (I _C = 1.5 Adc, V _{CE} = 2.0 Vdc) (I _C = 4.0 Adc, V _{CE} = 2.0 Vdc)	h _{FE}	25 25 20	100 100 80	—
Collector-Emitter Saturation Voltage (1) (I _C = 1.5 Adc, I _B = 0.15 Adc) (I _C = 4.0 Adc, I _B = 1.0 Adc)	V _{CE(sat)}	—	0.6 1.4	Vdc
Base-Emitter On Voltage (1) (I _C = 1.5 Adc, V _{CE} = 2.0 Vdc)	V _{BE(on)}	—	1.2	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product (I _C = 1.0 Adc, V _{CE} = 10 Vdc, f = 1.0 MHz)	f _T	2.0	—	MHz
---	----------------	-----	---	-----

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

* Indicates JEDEC Registered Data



NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA. TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.94	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-225AA

FIGURE 1 - DC CURRENT GAIN

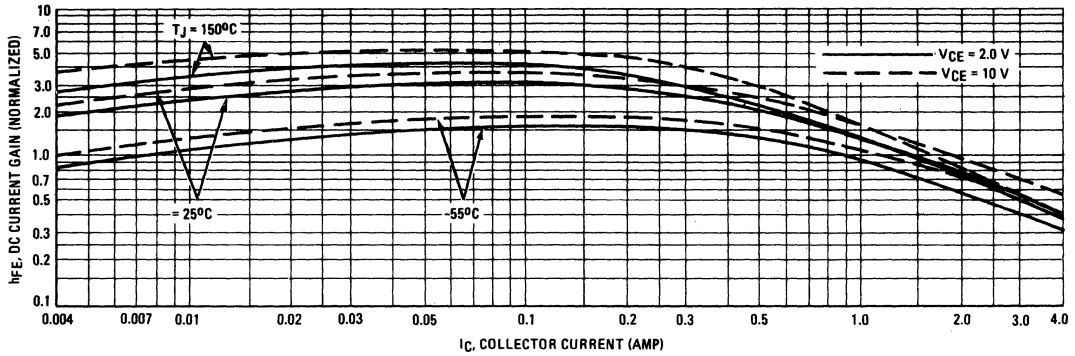


FIGURE 2 - COLLECTOR SATURATION REGION

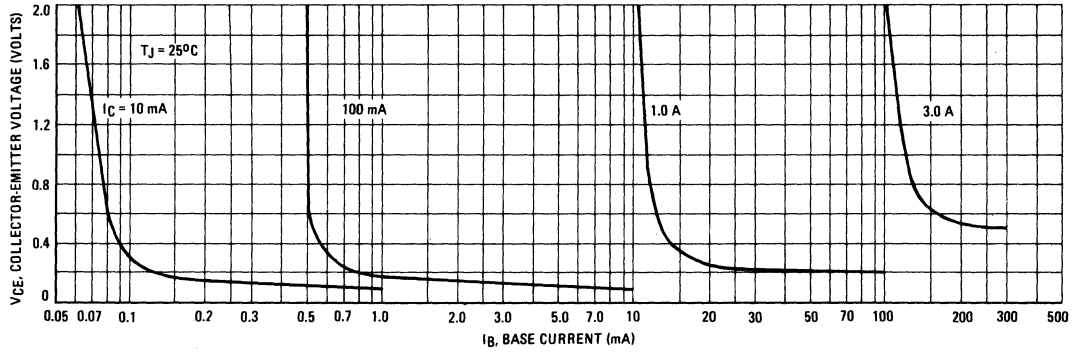


FIGURE 3 - "ON" VOLTAGES

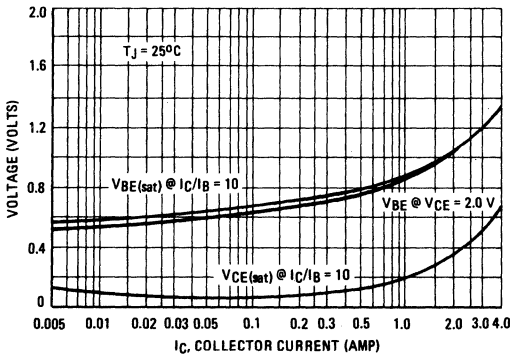


FIGURE 4 - TEMPERATURE COEFFICIENTS

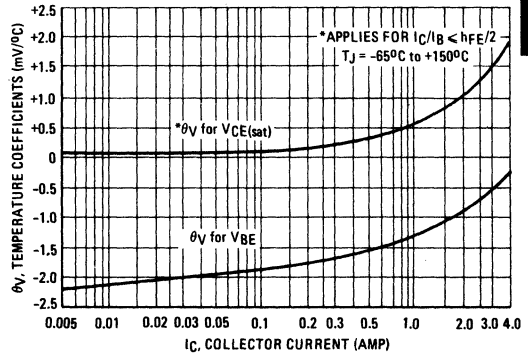


FIGURE 5 - COLLECTOR CUT-OFF REGION

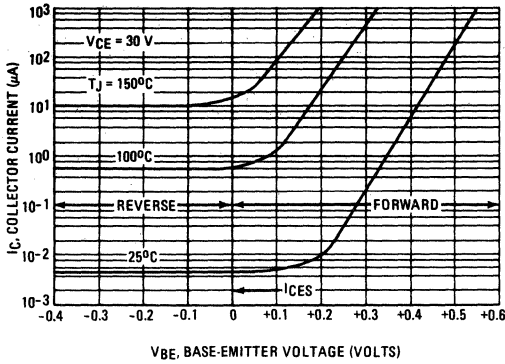


FIGURE 6 - EFFECTS OF BASE-EMITTER RESISTANCE

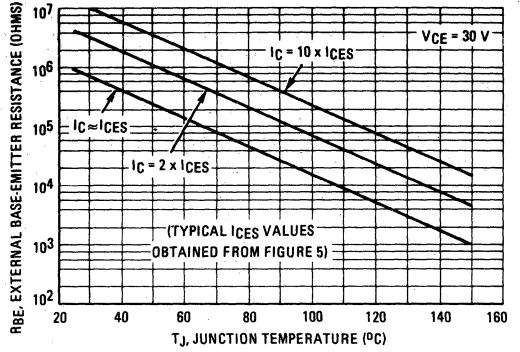


FIGURE 7 - SWITCHING TIME EQUIVALENT CIRCUIT

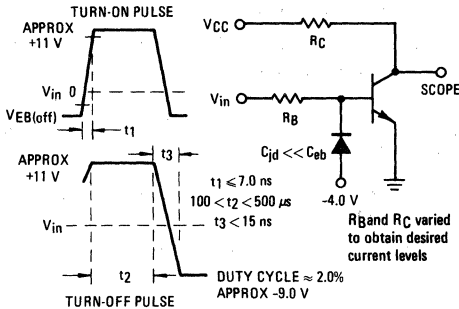


FIGURE 8 - CAPACITANCE

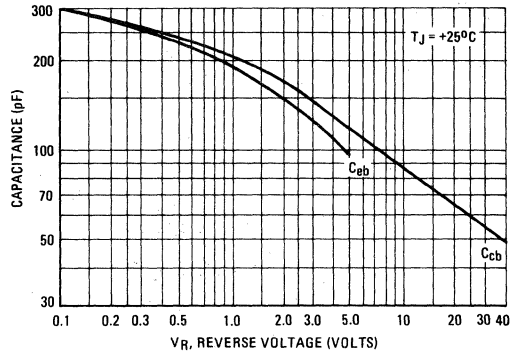


FIGURE 9 - TURN-ON TIME

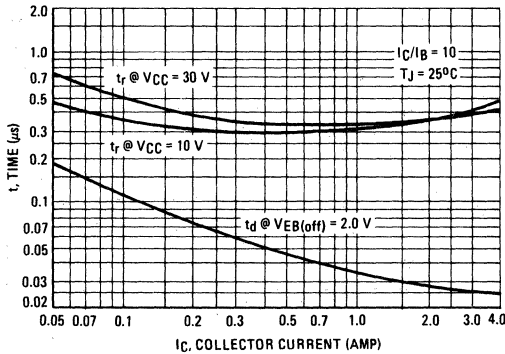
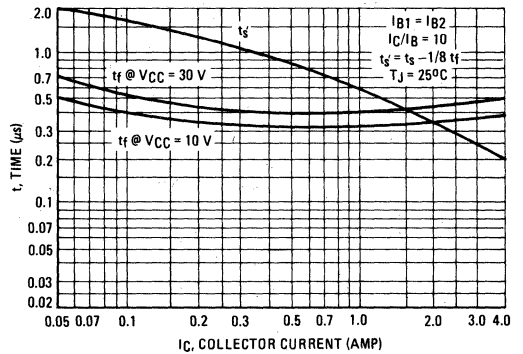
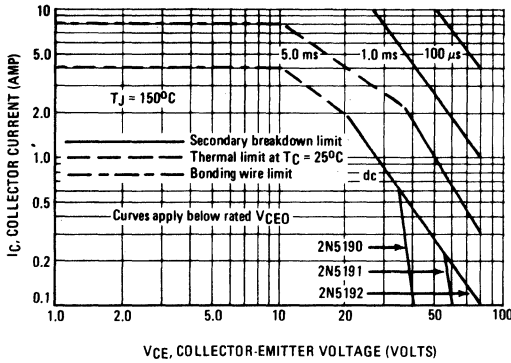


FIGURE 10 - TURN-OFF TIME



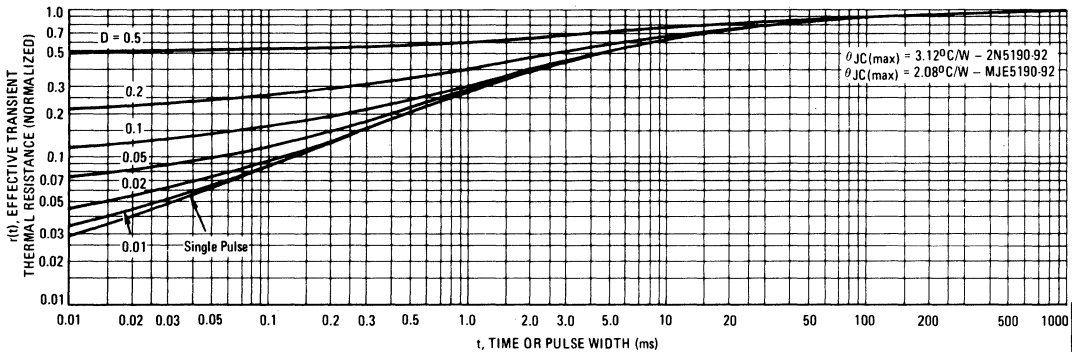
**FIGURE 11 RATING AND THERMAL DATA
ACTIVE-REGION SAFE OPERATING AREA**



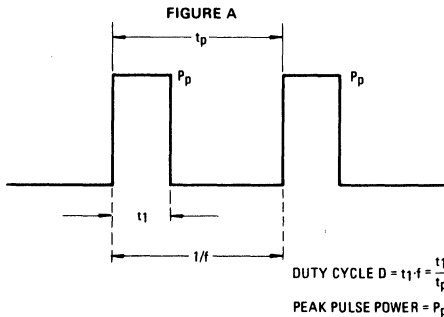
There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_J(pk) = 150^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(pk) \leq 150^\circ C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 12 – THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC} .

Example:

The 2N5190 is dissipating 50 watts under the following conditions: $t_1 = 0.1$ ms, $t_p = 0.5$ ms. ($D = 0.2$).

Using Figure 12, at a pulse width of 0.1 ms and $D = 0.2$, the reading of $r(t_1, D)$ is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ C$$

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

2N5193 thru 2N5195

SILICON PNP POWER TRANSISTORS

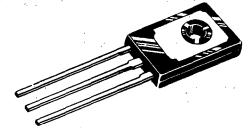
... for use in power amplifier and switching circuits, — excellent safe area limits. Complement to NPN 2N5190, 2N5191, 2N5192

4 AMPERE POWER TRANSISTORS SILICON PNP

40-80 VOLTS

*MAXIMUM RATINGS

Rating	Symbol	2N5193	2N5194	2N5195	Unit
Collector-Emitter Voltage	V_{CE0}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current	I_C	← 4.0 →			A dc
Base Current	I_B	← 1.0 →			A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 40 →			Watts
		← 320 →			mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			$^\circ\text{C/W}$



THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	$^\circ\text{C/W}$

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 0.1 \text{ A dc}, I_B = 0$)	2N5193 2N5194 2N5195	$V_{CE0(sus)}$	40 60 80	Vdc	
Collector Cutoff Current ($V_{CE} = 40 \text{ Vdc}, I_B = 0$) ($V_{CE} = 60 \text{ Vdc}, I_B = 0$) ($V_{CE} = 80 \text{ Vdc}, I_B = 0$)	2N5193 2N5194 2N5195	I_{CEO}	— — —	1.0 1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 40 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 60 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 40 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$) ($V_{CE} = 60 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$) ($V_{CE} = 80 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$)	2N5193 2N5194 2N5195	I_{CEX}	— — —	0.1 0.1 0.1 2.0 2.0 2.0	mAdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}, I_E = 0$) ($V_{CB} = 60 \text{ Vdc}, I_E = 0$) ($V_{CB} = 80 \text{ Vdc}, I_E = 0$)	2N5193 2N5194 2N5195	I_{CBO}	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)		I_{EBO}	—	1.0	mAdc

ON CHARACTERISTICS

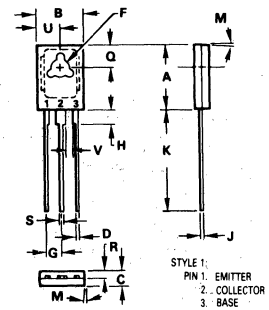
DC Current Gain (1) ($I_C = 1.5 \text{ A dc}, V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 4.0 \text{ A dc}, V_{CE} = 2.0 \text{ Vdc}$)	2N5193 2N5194 2N5195 2N5193 2N5194 2N5195	h_{FE}	25 25 20 10 10 7.0	100 100 80 — — —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 1.5 \text{ A dc}, I_B = 0.15 \text{ A dc}$) ($I_C = 4.0 \text{ A dc}, I_B = 1.0 \text{ A dc}$)		$V_{CE(sat)}$	— —	0.6 1.4	Vdc
Base-Emitter On Voltage (1) ($I_C = 1.5 \text{ A dc}, V_{CE} = 2.0 \text{ Vdc}$)		$V_{BE(on)}$	—	1.2	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 1.0 \text{ A dc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$)		f_T	2.0	—	MHz
--	--	-------	-----	---	-----

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$



NOTES

- LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
K	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3" TYP		3" TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-225AA

FIGURE 1 - DC CURRENT GAIN

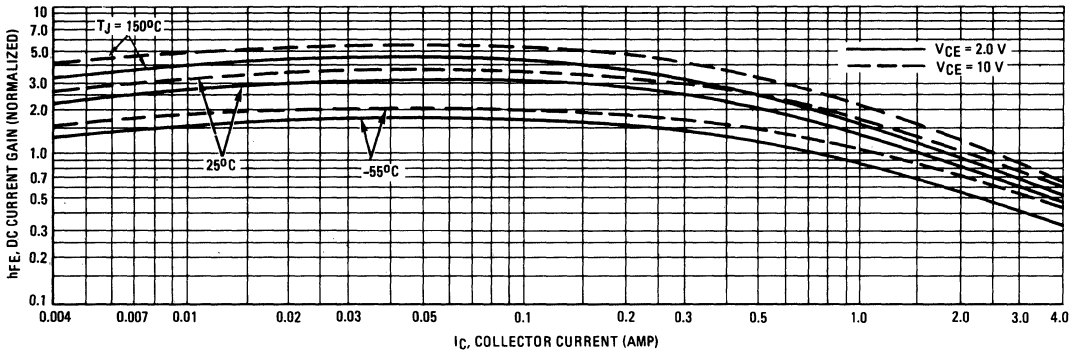


FIGURE 2 - COLLECTOR SATURATION REGION

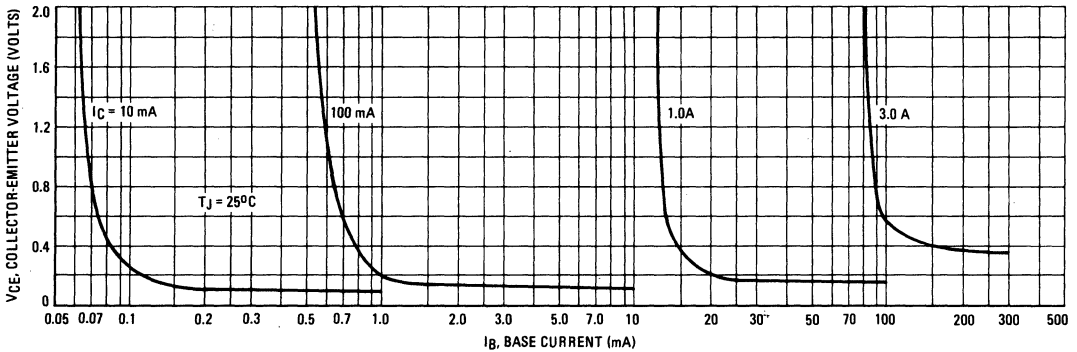


FIGURE 3 - "ON" VOLTAGE

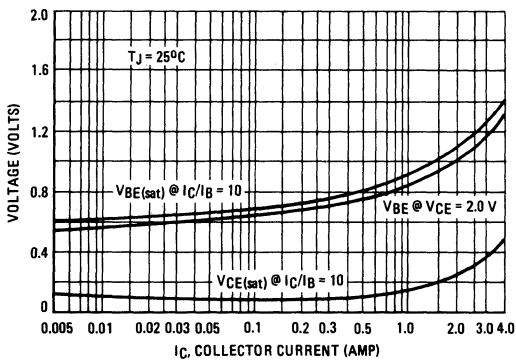


FIGURE 4 - TEMPERATURE COEFFICIENTS

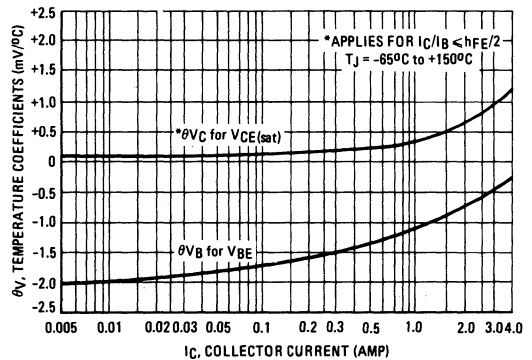


FIGURE 5 – COLLECTOR CUT-OFF REGION

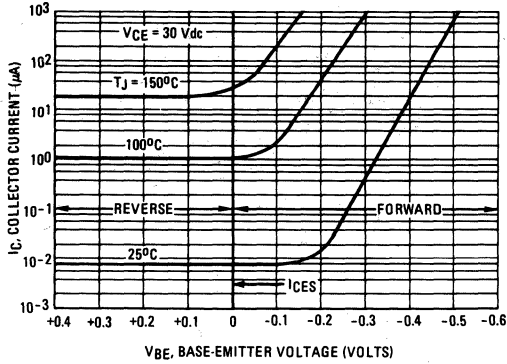


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

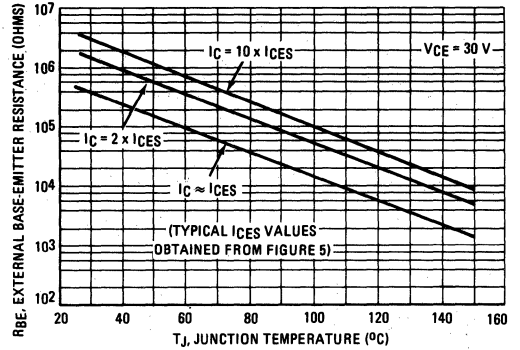


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT

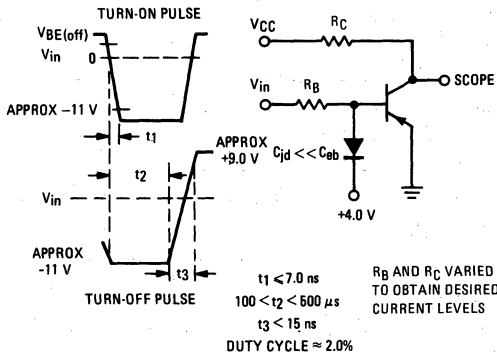


FIGURE 8 – CAPACITANCE

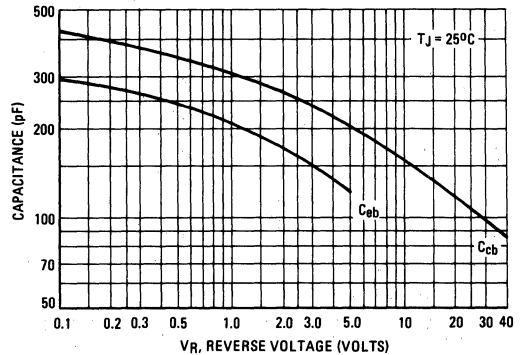


FIGURE 9 – TURN-ON TIME

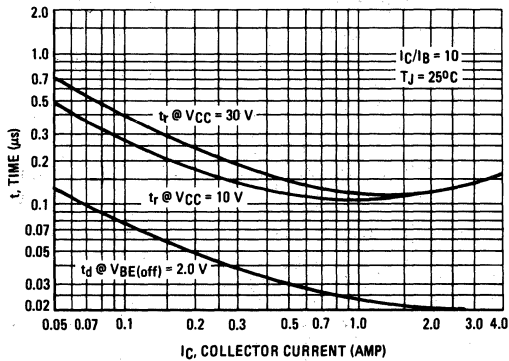
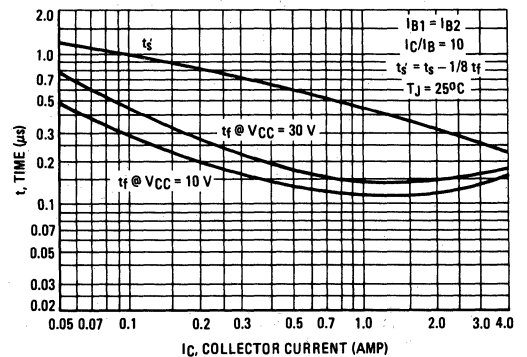
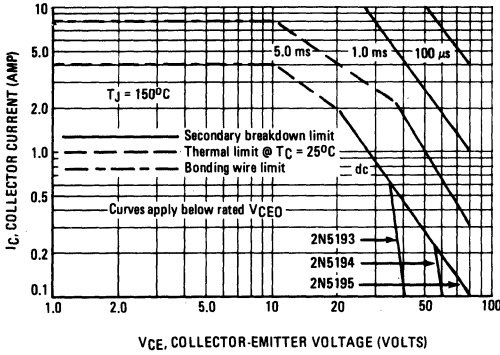


FIGURE 10 – TURN-OFF TIME



3

FIGURE 11
RATING AND THERMAL DATA
ACTIVE-REGION SAFE OPERATING AREA

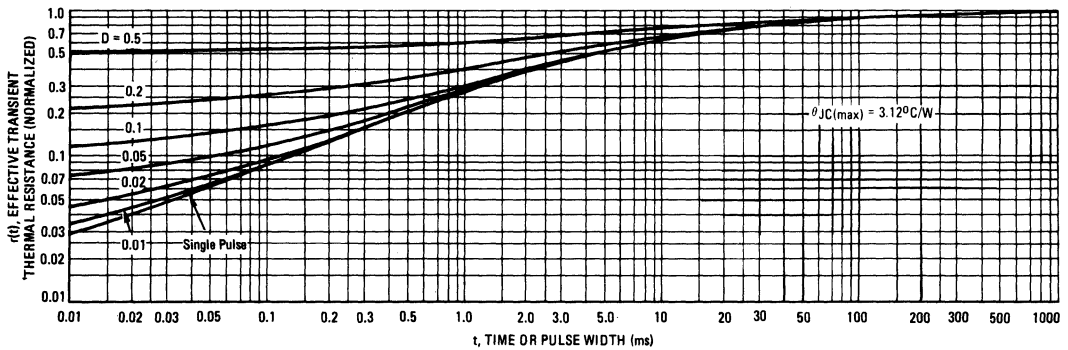


Note 1:

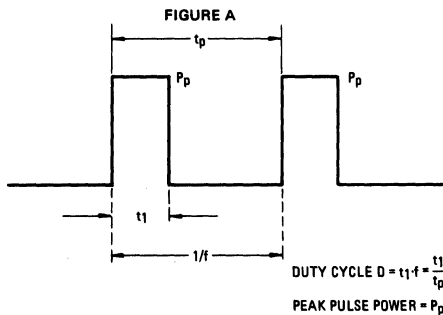
There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)} = 150^\circ\text{C}$. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high-case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 12 – THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC} .

Example:

The 2N5193 is dissipating 50 watts under the following conditions: $t_1 = 0.1$ ms, $t_p = 0.5$ ms. ($D = 0.2$).

Using Figure 12, at a pulse width of 0.1 ms and $D = 0.2$, the reading of $r(t_1, D)$ is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ\text{C}$$

2N5301
2N5302
2N5303

HIGH-POWER NPN SILICON TRANSISTORS

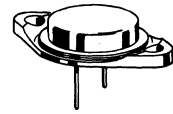
... for use in power amplifier and switching circuits applications.

- High Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 80 \text{ Vdc (Min) @ } I_C = 200 \text{ mAdc (2N5303)}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.75 \text{ Vdc (Max) @ } I_C = 10 \text{ Adc (2N5301, 2N5302)}$
 $1.0 \text{ Vdc (Max) @ } I_C = 10 \text{ Adc (2N5303)}$
- Excellent Safe Operating Area –
 200 Watt dc Power Rating to 30 Vdc (2N5303)
- Complements to PNP 2N4398, 2N4399 and 2N5745

20 AND 30 AMPERE
POWER TRANSISTORS

NPN SILICON

40-60-80 VOLTS
200 WATTS



***MAXIMUM RATINGS**

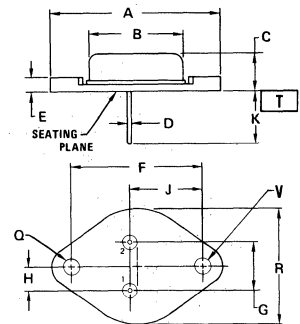
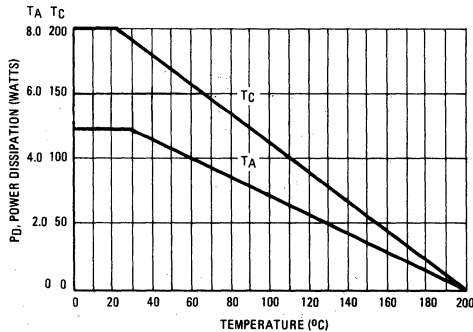
Rating	Symbol	2N5301	2N5302	2N5303	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Collector Current – Continuous	I_C	30	30	20	Adc
Base Current	I_B	7.5			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	200			Watts
		1.14			W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	$^\circ\text{C/W}$
Thermal Resistance, Case to Ambient	θ_{CA}	34	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER TEMPERATURE DERATING CURVE



STYLE 1: PIN 1. BASE
 2. EMITTER
 CASE: COLLECTOR

STYLE 3: PIN 1. ANODE
 2. CATHODE

- NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
 2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\text{H} \begin{matrix} \text{H} \\ \text{H} \end{matrix} 0.25 (0.010) \text{ T } \begin{matrix} \text{T} \\ \text{T} \end{matrix} \text{ V } \begin{matrix} \text{V} \\ \text{V} \end{matrix}$
 3. POSITIONAL TOLERANCE FOR LEADS:
 $\text{H} \begin{matrix} \text{H} \\ \text{H} \end{matrix} 0.30 (0.012) \text{ T } \begin{matrix} \text{T} \\ \text{T} \end{matrix} \text{ V } \begin{matrix} \text{V} \\ \text{V} \end{matrix} \text{ Q } \begin{matrix} \text{Q} \\ \text{Q} \end{matrix}$
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
*OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Note 1) (I _C = 200 mA, I _B = 0)	2N5301 2N5302 2N5303	V _{CEO(sus)}	40 80 80	— — —	Vdc
Collector Cutoff Current (V _{CE} = 40 Vdc, I _B = 0) (V _{CE} = 60 Vdc, I _B = 0) (V _{CE} = 80 Vdc, I _B = 0)	2N5301 2N5302 2N5303	I _{CEO}	— — —	5.0 5.0 5.0	mA
Collector Cutoff Current (V _{CE} = 40 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 60 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 80 Vdc, V _{EB(off)} = 1.5 Vdc)	2N5301 2N5302 2N5303	I _{CEX}	— — —	1.0 1.0 1.0	mA
Collector Cutoff Current (V _{CE} = 40 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C) (V _{CE} = 60 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C) (V _{CE} = 80 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C)	2N5301 2N5302 2N5303	I _{CEX}	— — —	10 10 10	mA
Collector Cutoff Current (V _{CB} = 40 Vdc, I _E = 0) (V _{CB} = 60 Vdc, I _E = 0) (V _{CB} = 80 Vdc, I _E = 0)	2N5301 2N5302 2N5303	I _{CB0}	— — —	1.0 1.0 1.0	mA
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)		I _{EBO}	—	5.0	mA
ON CHARACTERISTICS					
DC Current Gain (Note 1) *(I _C = 1.0 A, V _{CE} = 2.0 Vdc) *(I _C = 10 A, V _{CE} = 2.0 Vdc) *(I _C = 15 A, V _{CE} = 2.0 Vdc) (I _C = 20 A, V _{CE} = 4.0 Vdc) (I _C = 30 A, V _{CE} = 4.0 Vdc)	ALL TYPES 2N5303 2N5301, 2N5302 2N5303 2N5301, 2N5302	h _{FE}	40 15 15 5.0 5.0	— — — — —	—
*Collector-Emitter Saturation Voltage (Note 1) (I _C = 10 A, I _B = 1.0 A) (I _C = 10 A, I _B = 1.0 A) (I _C = 15 A, I _B = 1.5 A) (I _C = 20 A, I _B = 2.0 A) (I _C = 20 A, I _B = 4.0 A) (I _C = 30 A, I _B = 6.0 A)	2N5301, 2N5302 2N5303 2N5303 2N5301, 2N5302 2N5303 2N5301, 2N5302	V _{CE(sat)}	— — — — — —	0.75 1.0 1.5 2.0 2.0 3.0	Vdc
*Base-Emitter Saturation Voltage (Note 1) (I _C = 10 A, I _B = 1.0 A) (I _C = 15 A, I _B = 1.5 A) (I _C = 15 A, I _B = 1.5 A) (I _C = 20 A, I _B = 2.0 A) (I _C = 20 A, I _B = 4.0 A)	ALL TYPES 2N5301, 2N5302 2N5303 2N5301, 2N5302 2N5303	V _{BE(sat)}	— — — — —	1.7 1.8 2.0 2.5 2.5	Vdc
*Base-Emitter On Voltage (Note 1) (I _C = 10 A, V _{CE} = 2.0 Vdc) (I _C = 15 A, V _{CE} = 2.0 Vdc) (I _C = 20 A, V _{CE} = 4.0 Vdc) (I _C = 30 A, V _{CE} = 4.0 Vdc)	2N5303 2N5301, 2N5302 2N5303 2N5301, 2N5302	V _{BE(on)}	— — — —	1.5 1.7 2.5 3.0	Vdc
*DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I _C = 1.0 A, V _{CE} = 10 Vdc, f = 1.0 MHz)		f _T	2.0	—	MHz
Small-Signal Current Gain (I _C = 1.0 A, V _{CE} = 10 Vdc, f = 1.0 kHz)		h _{fe}	40	—	—
*SWITCHING CHARACTERISTICS					
Rise Time Storage Time Fall Time	(V _{CC} = 30 Vdc, I _C = 10 A, I _{B1} = I _{B2} = 1.0 A)	t _r t _s t _f	— — —	1.0 2.0 1.0	μs

*Indicates JEDEC Registered Data.
Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

FIGURE 2 – TURN-ON TIME

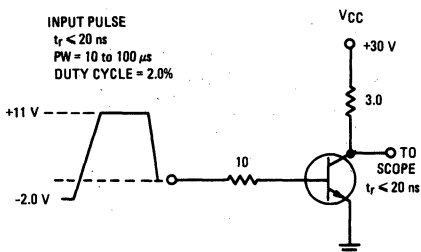


FIGURE 3 – TURN-OFF TIME

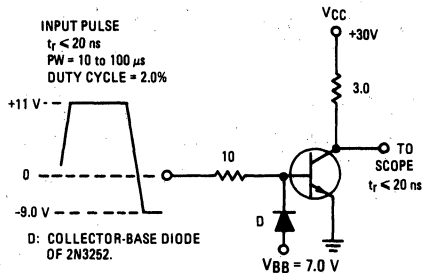


FIGURE 4 - THERMAL RESPONSE

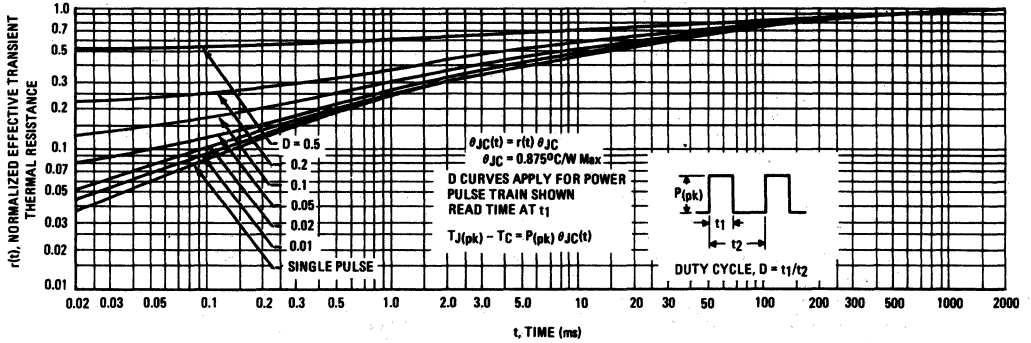


FIGURE 5 - ACTIVE-REGION SAFE OPERATING AREA

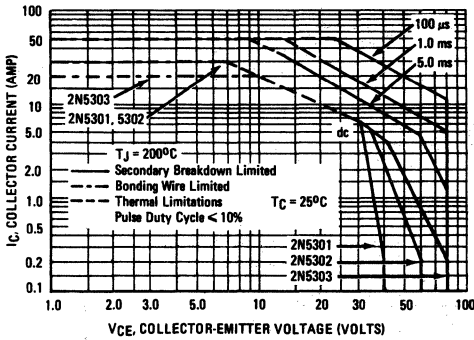


FIGURE 6 - CAPACITANCE versus VOLTAGE

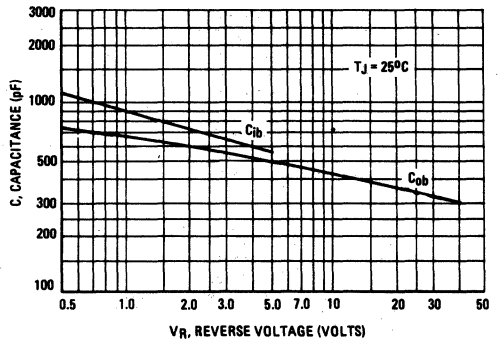


FIGURE 7 - TURN-ON TIME

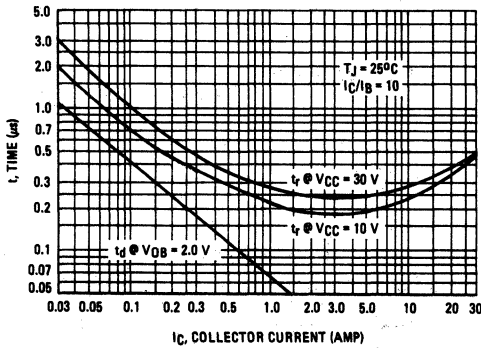
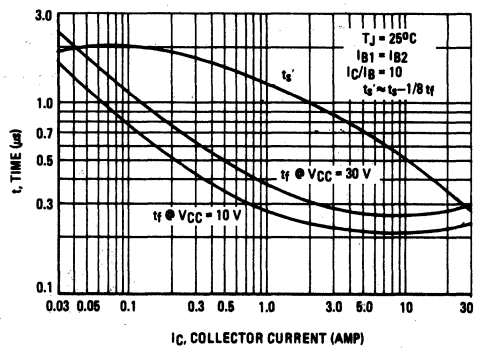


FIGURE 8 - TURN-OFF TIME



3

FIGURE 9 – DC CURRENT GAIN

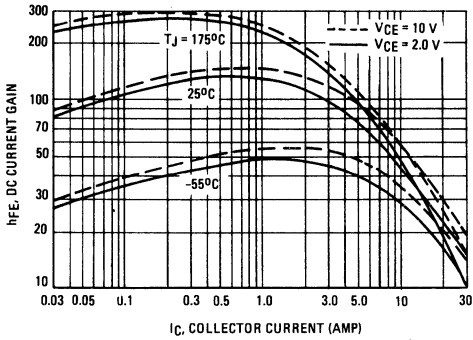


FIGURE 10 – COLLECTOR SATURATION REGION

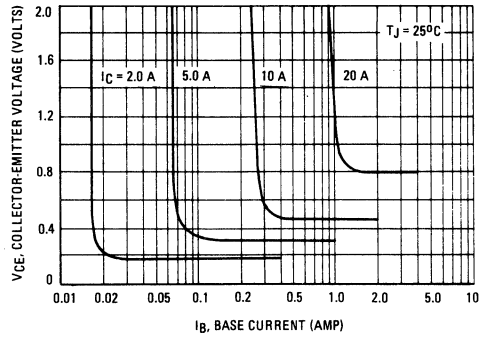


FIGURE 11 – EFFECTS OF BASE-EMITTER RESISTANCE

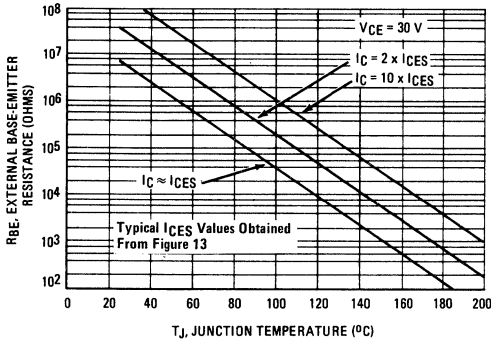


FIGURE 12 – "ON" VOLTAGES

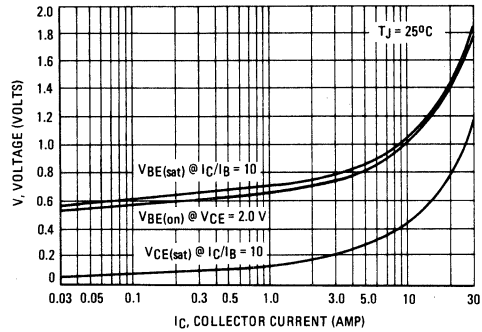


FIGURE 13 – COLLECTOR CUT-OFF REGION

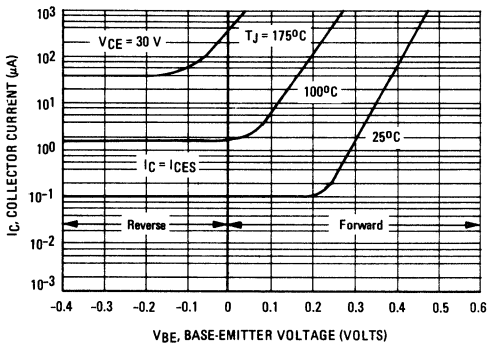
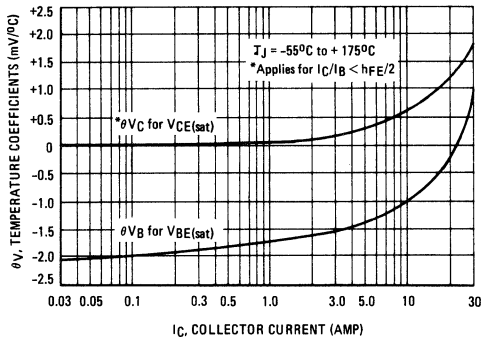


FIGURE 14 – TEMPERATURE COEFFICIENTS



2N5336
thru
2N5339

MEDIUM-POWER NPN SILICON TRANSISTORS

... designed for switching and wide band amplifier applications.

- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 1.2 \text{ Vdc (Max) @ } I_C = 5.0 \text{ Amp}$
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-205AD Case for Critical Space-Limited Applications
- Complement to 2N6190 thru 2N6193

5 AMPERE
POWER TRANSISTORS
NPN SILICON

80-100 VOLTS
6 WATTS

MAXIMUM RATINGS

Rating	Symbol	2N5336 2N5337	2N5338 2N5339	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	6.0	34.3	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	29.2	$^\circ\text{C/W}$

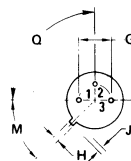
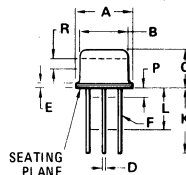
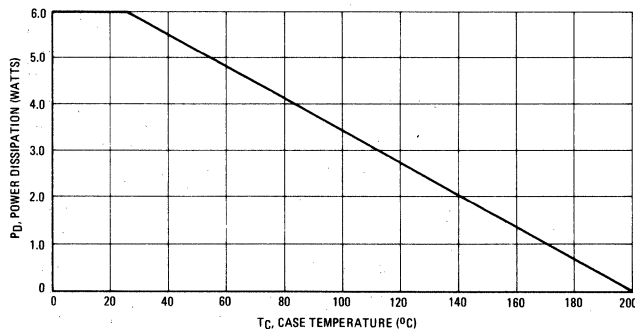


FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° NOM	45° NOM	—	—
P	—	1.27	—	0.050
Q	90° NOM	90° NOM	—	—
R	2.54	—	0.100	—

All JEDEC dimensions and notes apply.

CASE 79-02
TO-205AD

2N5336 thru 2N5339

ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage* (I _C = 50 mA _{dc} , I _B = 0)	2N5336, 2N5337 2N5338, 2N5339	—	V _{CEO(sus)} *	80 100	— —	V _{dc}
Collector Cutoff Current (V _{CE} = 75 V _{dc} , I _B = 0) (V _{CE} = 90 V _{dc} , I _B = 0)	2N5336, 2N5337 2N5338, 2N5339	—	I _{CEO}	— —	100 100	μA _{dc}
Collector Cutoff Current (V _{CE} = 75 V _{dc} , V _{EB(off)} = 1.5 V _{dc}) (V _{CE} = 90 V _{dc} , V _{EB(off)} = 1.5 V _{dc}) (V _{CE} = 75 V _{dc} , V _{EB(off)} = 1.5 V _{dc} , T _C = 150°C) (V _{CE} = 90 V _{dc} , V _{EB(off)} = 1.5 V _{dc} , T _C = 150°C)	2N5336, 2N5337 2N5338, 2N5339 2N5336, 2N5337 2N5338, 2N5339	12	I _{CEx}	— —	10 10	μA _{dc}
Collector Cutoff Current (V _{CB} = 80 V _{dc} , I _E = 0) (V _{CB} = 100 V _{dc} , I _E = 0)	2N5336, 2N5337 2N5338, 2N5339	—	I _{CBO}	— —	10 10	μA _{dc}
Emitter Cutoff Current (V _{BE} = 6.0 V _{dc} , I _C = 0)	—	—	I _{EBO}	—	100	μA _{dc}

ON CHARACTERISTICS

DC Current Gain* (I _C = 500 mA _{dc} , V _{CE} = 2.0 V _{dc}) (I _C = 2.0 A _{dc} , V _{CE} = 2.0 V _{dc}) (I _C = 5.0 A _{dc} , V _{CE} = 2.0 V _{dc})	2N5336, 2N5338 2N5337, 2N5339 2N5336, 2N5338 2N5337, 2N5339 2N5336, 2N5338 2N5337, 2N5339	8	h _{FE} *	30 60 30 60 20 40	— — 120 240 — —	—
Collector-Emitter Saturation Voltage* (I _C = 2.0 A _{dc} , I _B = 0.2 A _{dc}) (I _C = 5.0 A _{dc} , I _B = 0.5 A _{dc})	—	9, 11, 13	V _{CE(sat)} *	— —	0.7 1.2	V _{dc}
Base-Emitter Saturation Voltage* (I _C = 2.0 A _{dc} , I _B = 0.2 A _{dc}) (I _C = 5.0 A _{dc} , I _B = 0.5 A _{dc})	—	11, 13	V _{BE(sat)} *	— —	1.2 1.8	V _{dc}

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product (I _C = 0.5 A _{dc} , V _{CE} = 10 V _{dc} , f = 10 MHz)	—	f _T	30	—	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 100 kHz)	7	C _{ob}	—	250	pF
Input Capacitance (V _{BE} = 2.0 V _{dc} , I _C = 0, f = 100 kHz)	7	C _{ib}	—	1,000	pF

SWITCHING CHARACTERISTICS

Delay Time (V _{CC} = 40 V _{dc} , V _{EB(off)} = 3.0 V _{dc})	2, 3	t _d	—	100	ns
Rise Time (I _C = 2.0 A _{dc} , I _{B1} = 0.2 A _{dc})	—	t _r	—	100	ns
Storage Time (V _{CC} = 40 V _{dc} , I _C = 2.0 A _{dc})	2, 6	t _s	—	2.0	μs
Fall Time (I _{B1} = I _{B2} = 0.2 A _{dc})	—	t _f	—	200	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

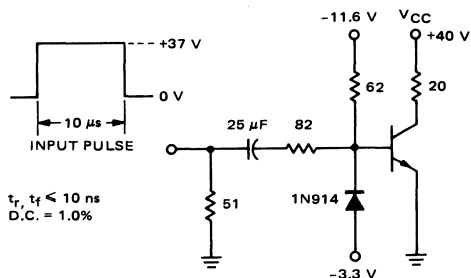


FIGURE 3 — TURN-ON TIME

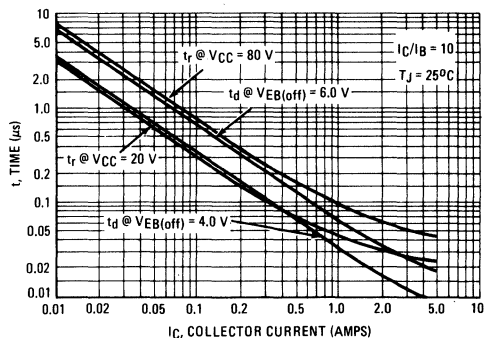


FIGURE 4 – THERMAL RESPONSE

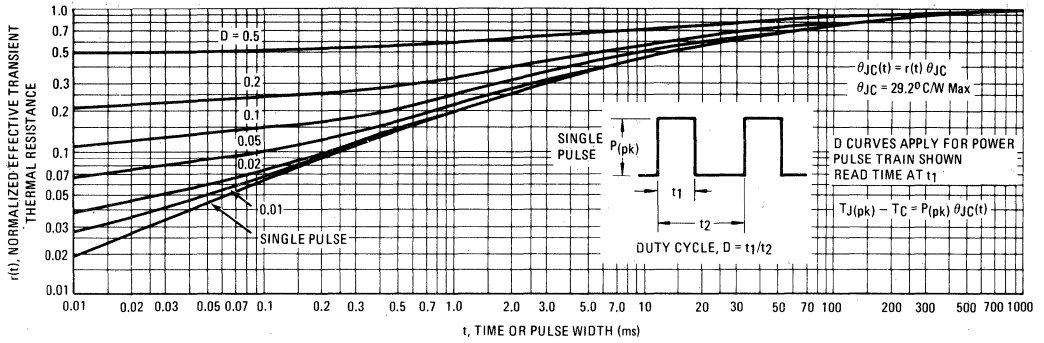
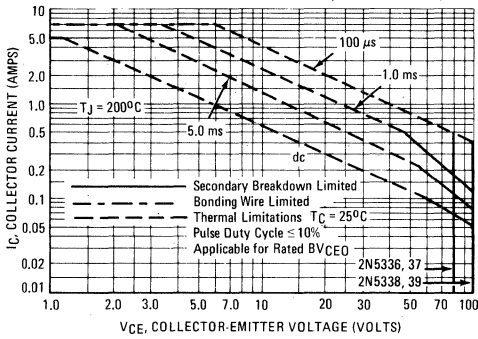


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

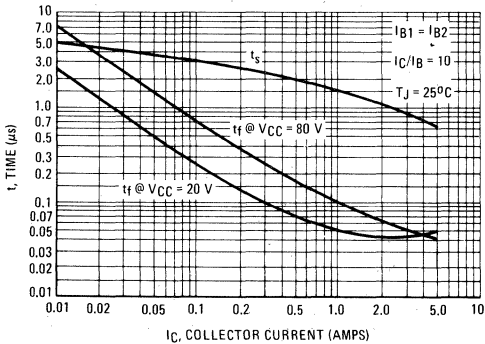
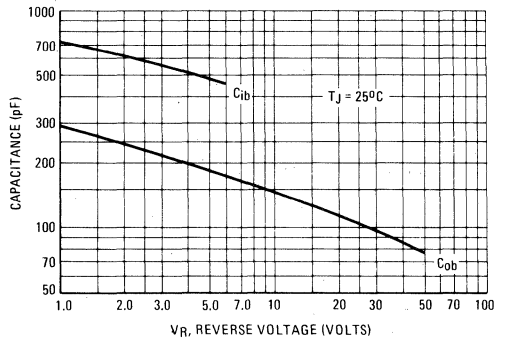


FIGURE 7 – CAPACITANCE versus VOLTAGE



3

FIGURE 8 – DC CURRENT GAIN

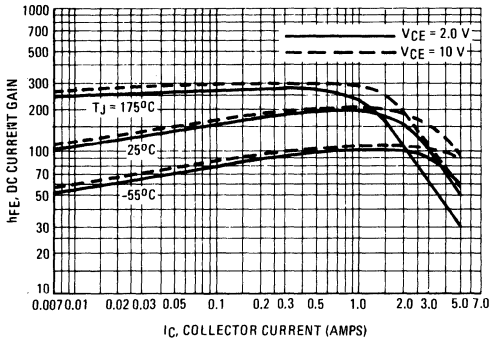


FIGURE 9 – COLLECTOR SATURATION REGION

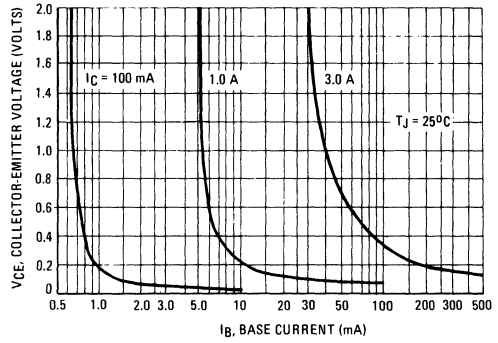


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

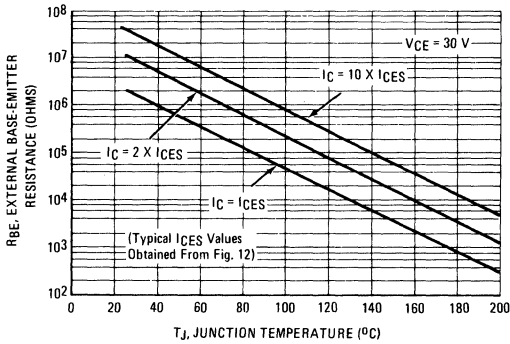


FIGURE 11 – ON VOLTAGES

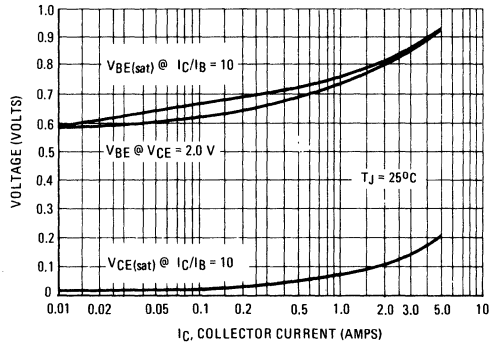


FIGURE 12 – COLLECTOR CUT-OFF REGION

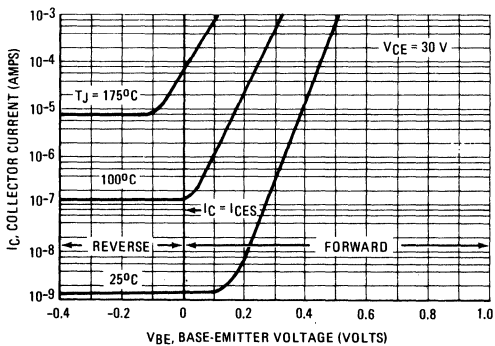
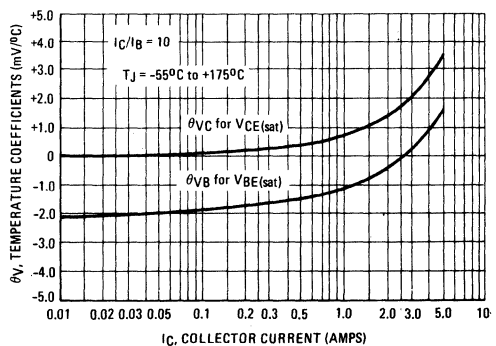


FIGURE 13 – TEMPERATURE COEFFICIENTS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

2N5344

HIGH VOLTAGE POWER PNP SILICON TRANSISTOR

... designed for high-voltage switching and amplifier applications.

- High Voltage Rating — $V_{CEO} = 250$ Vdc
- Fast Switching Time — Typically Less Than 550 ns
Total @ $V_{CC} = 100$ Vdc
- High Current-Gain-Bandwidth Product —
 $f_T = 60$ MHz (Min) @ $I_C = 100$ mAdc
- Packaged in the Compact, High-Efficiency TO-213AA Case

**1 AMPERE
POWER TRANSISTOR
PNP SILICON**

**250-300 VOLTS
40 WATTS**

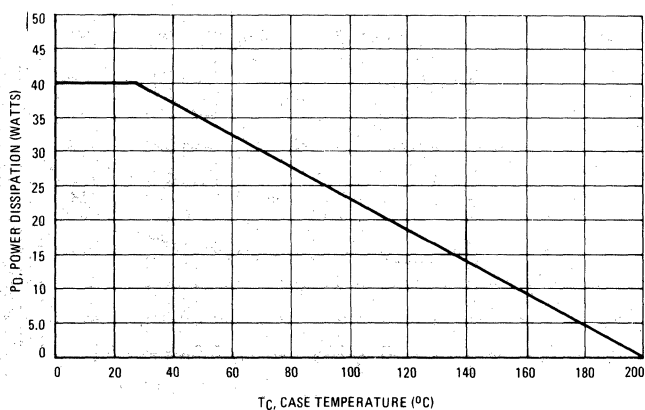
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	250	Vdc
Collector-Base Voltage	V_{CB}	250	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	1.0	Adc
Base Current — Continuous	I_B	0.5	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40 228	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$

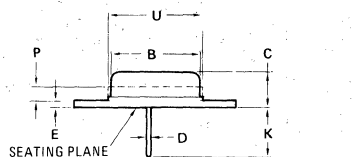
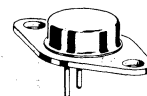
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.38	$^\circ\text{C}/\text{W}$

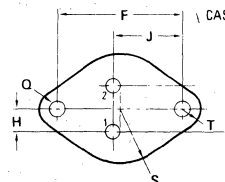
FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves Are Indicated By Figure 5.
All Limits Are Applicable And Must Be Observed



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC Dimensions and Notes Apply.

**CASE 80-02
TO-213AA**

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1) ($I_C = 10 \text{ mAdc}, I_B = 0$)	2N5344	5	$V_{CEO(sus)}$	250	—	Vdc
Collector Cutoff Current ($V_{CE} = 225 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$)	2N5344	10, 12	I_{CEX}	—	100	μAdc
($V_{CE} = 225 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)	2N5344	—	—	—	1.0	mAdc
Collector Cutoff Current ($V_{CB} = \text{Rated } V_{CB}, I_E = 0$)	—	—	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)	—	—	I_{EBO}	—	0.1	mAdc

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 500 \text{ mAdc}, V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}$)	8	h_{FE}	25 7.0	150	—	—
Collector-Emitter Saturation Voltage ($I_C = 1.0 \text{ Adc}, I_B = 0.2 \text{ Adc}$)	9, 11, 13	$V_{CE(sat)}$	—	3.0	—	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0 \text{ Adc}, I_B = 0.2 \text{ Adc}$)	11, 13	$V_{BE(sat)}$	—	1.5	—	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain—Bandwidth Product ($I_C = 100 \text{ mAdc}, V_{CE} = 20 \text{ Vdc}, f = 10 \text{ MHz}$)	—	f_T	60	—	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0$)	7	C_{ob}	—	200	—	pF

SWITCHING CHARACTERISTICS

Turn-On ($V_{CC} = 100 \text{ Vdc}, I_C = 500 \text{ mAdc}, I_{B1} = I_{B2} = 50 \text{ mAdc}$)	2, 3	t_{on}	—	200	—	ns
Turn-Off ($V_{CC} = 100 \text{ Vdc}, I_C = 500 \text{ mAdc}, I_{B1} = I_{B2} = 50 \text{ mAdc}$)	2, 6	t_{off}	—	700	—	ns

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\approx 2.0\%$.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

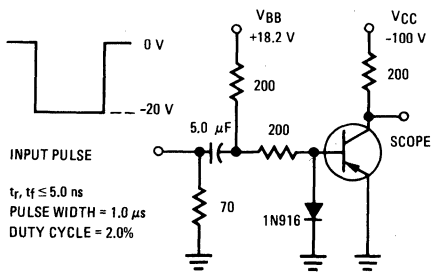


FIGURE 3 – TURN-ON TIME

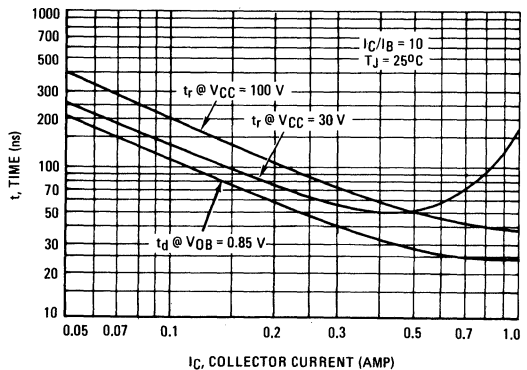


FIGURE 4 – THERMAL RESPONSE

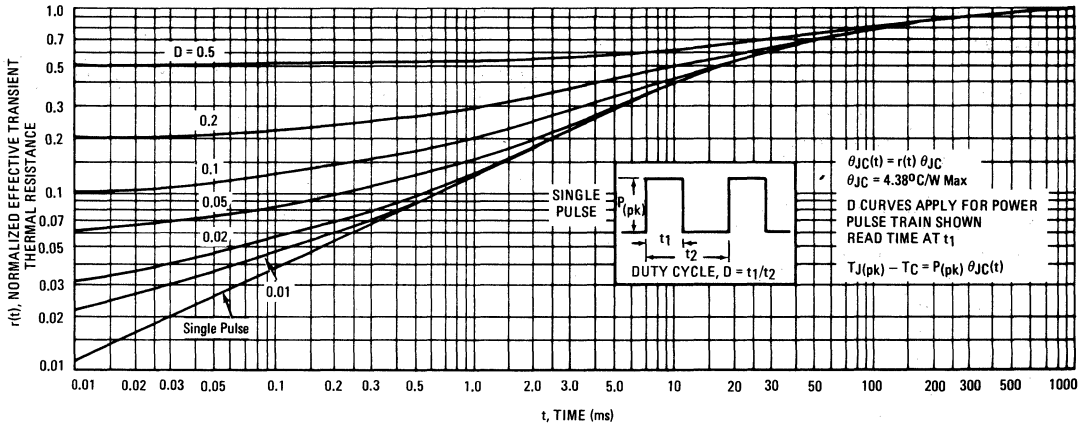
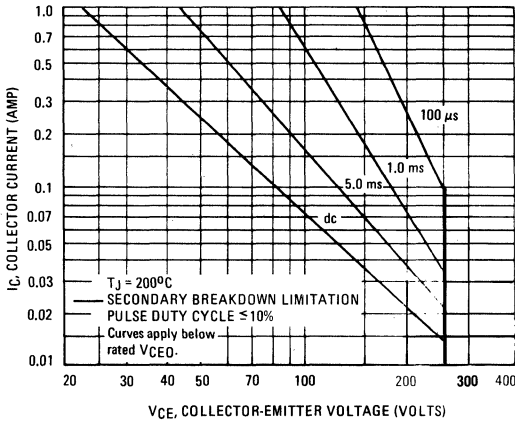


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_J(pk) = 200^\circ\text{C}$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_J(pk) \leq 200^\circ\text{C}$. $T_J(pk)$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

3

FIGURE 6 – TURN-OFF TIME

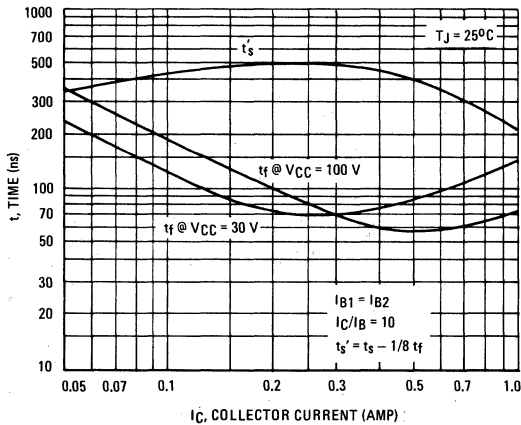
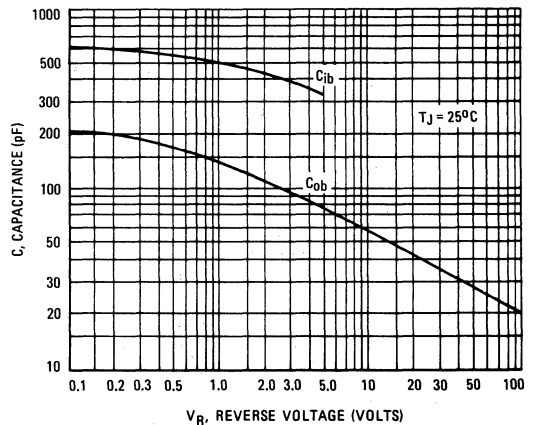


FIGURE 7 – CAPACITANCES



TYPICAL DC CHARACTERISTICS

FIGURE 8 – DC CURRENT GAIN

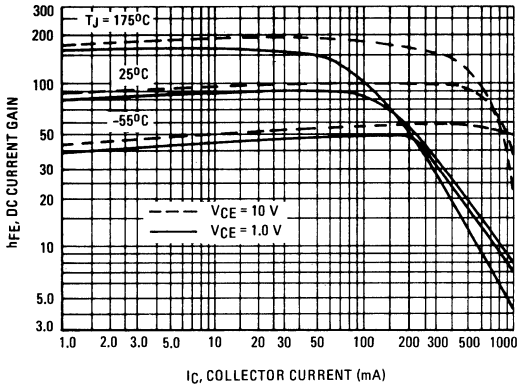


FIGURE 9 – COLLECTOR SATURATION REGION

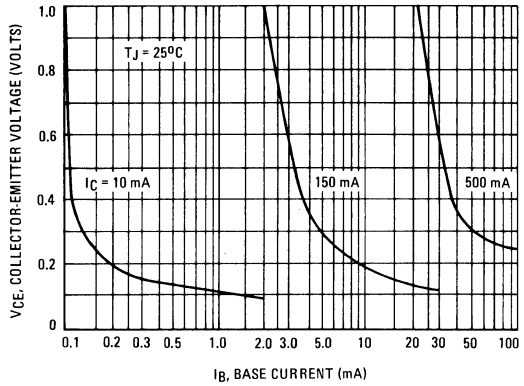


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

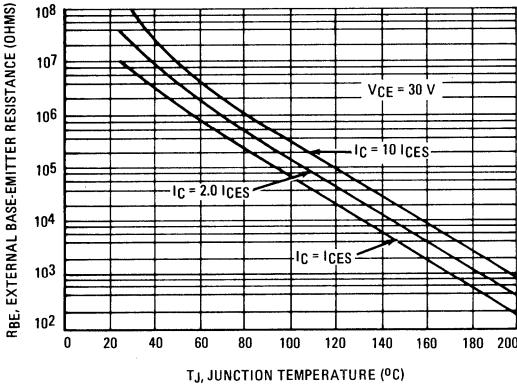
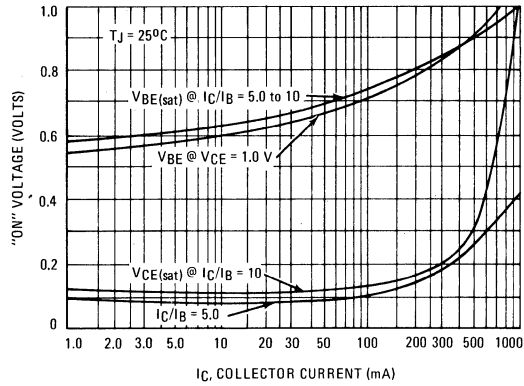


FIGURE 11 – "ON" VOLTAGES



3

FIGURE 12 – COLLECTOR CUT-OFF REGION

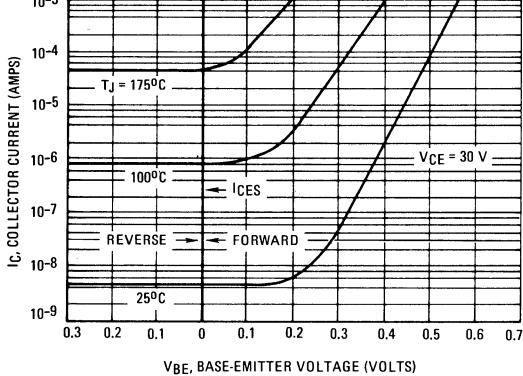
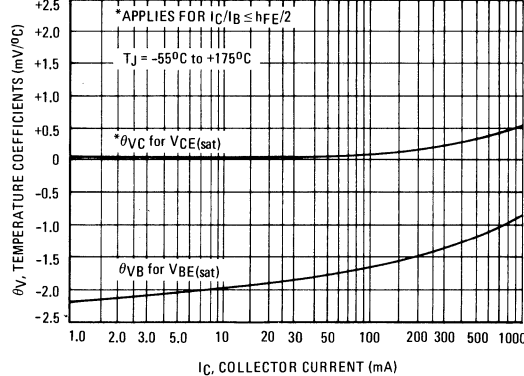


FIGURE 13 – TEMPERATURE COEFFICIENTS



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N5428
thru
2N5430

MEDIUM-POWER NPN SILICON TRANSISTORS

... designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 1.2 \text{ Vdc (Max) @ } I_C = 7.0 \text{ Adc}$
- DC Current Gain Specified to 7 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-213AA Case

7 AMPERE

POWER TRANSISTORS
NPN SILICON

80-100 VOLTS
40 WATTS

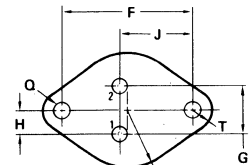
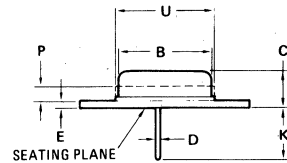
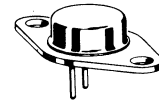
***MAXIMUM RATINGS**

Rating	Symbol			Unit
		2N5428	2N5429 2N5430	
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	7.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40	228	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.37	$^\circ\text{C/W}$

* Indicates JEDEC Registered Data



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE: COLLECTOR

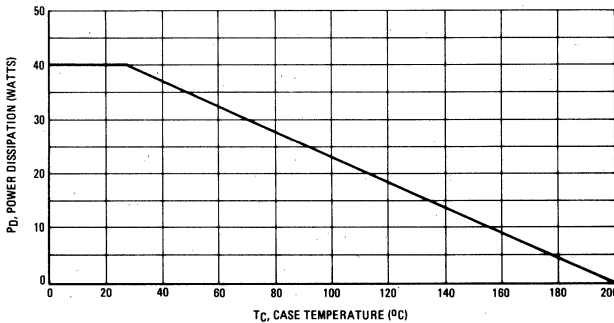
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC Dimensions and Notes Apply.

CASE 80-02
TO-213AA

3

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



2N5428 thru 2N5430

*ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I _C = 50 mAdc, I _B = 0)	—	V _{CEO(sus)*}	80 100	— —	Vdc
	2N5428 2N5429, 2N5430				
Collector Cutoff Current (V _{CE} = 75 Vdc, I _B = 0)	—	I _{CEO}	—	100	μAdc
	2N5428 2N5429, 2N5430		— —	100	
Collector Cutoff Current (V _{CE} = 75 Vdc, V _{EB(off)} = 1.5 Vdc)	12	I _{CEX}	—	10	μAdc
	2N5428 2N5429, 2N5430		— —	10	
(V _{CE} = 90 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C)	2N5428		—	1.0	mAdc
(V _{CE} = 90 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C)	2N5429, 2N5430		—	1.0	
Collector Cutoff Current (V _{CB} = Rated V _{CB} , I _E = 0)	—	I _{CBO}	—	10	μAdc
Emitter Cutoff Current (V _{BE} = 6.0 Vdc, I _C = 0)	—	I _{EBO}	—	100	μAdc

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 500 mAdc, V _{CE} = 2.0 Vdc)	8	h _{FE} *	30 60	— —	—
	2N5429 2N5428, 2N5430				
(I _C = 2.0 Adc, V _{CE} = 2.0 Vdc)	2N5429		30	120	
	2N5428, 2N5430		60	240	
(I _C = 5.0 Adc, V _{CE} = 2.0 Vdc)	2N5429		20	—	
	2N5428, 2N5430		40	—	
Collector-Emitter Saturation Voltage (I _C = 2.0 Adc, I _B = 0.2 Adc)	9, 11, 13	V _{CE(sat)*}	—	0.7	Vdc
			—	1.2	
(I _C = 7.0 Adc, I _B = 0.7 Adc)	11, 13	V _{BE(sat)*}	—	1.2	Vdc
			—	2.0	

DYNAMIC CHARACTERISTICS

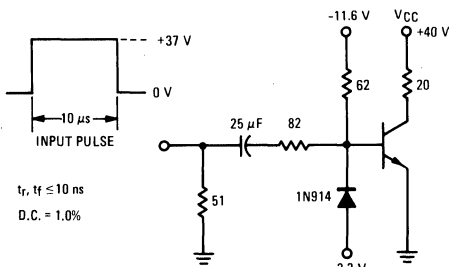
Current-Gain-Bandwidth Product (I _C = 500 mAdc, V _{CE} = 10 Vdc, f = 10 MHz)	—	f _T	30	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 100 kHz)	7	C _{ob}	—	250	pF
Input Capacitance (V _{BE} = 2.0 Vdc, I _C = 0, f = 100 kHz)	7	C _{ib}	—	1,000	pF

SWITCHING CHARACTERISTICS

Delay Time (V _{CC} = 40 Vdc, V _{EB(off)} = 3.0 Vdc,	2, 3	t _d	—	100	ns
Rise Time (I _C = 2.0 Adc, I _{B1} = 200 mAdc)		t _r	—	100	ns
Storage Time (V _{CC} = 40 Vdc, I _C = 2.0 Adc,	2, 6	t _s	—	2.0	μs
Fall Time I _{B1} = I _{B2} = 200 mAdc)		t _f	—	200	ns

*Indicates JEDEC Registered Data. (1) Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



t_r, t_f ≤ 10 ns
D.C. = 1.0%

FIGURE 3 – TURN-ON TIME

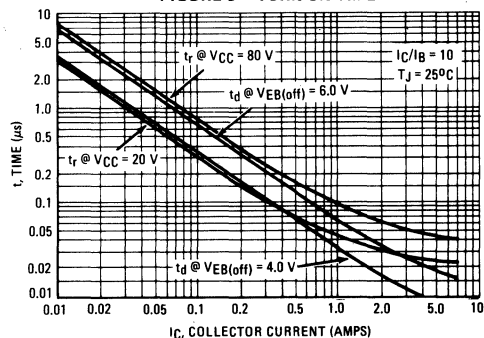


FIGURE 4 - THERMAL RESPONSE

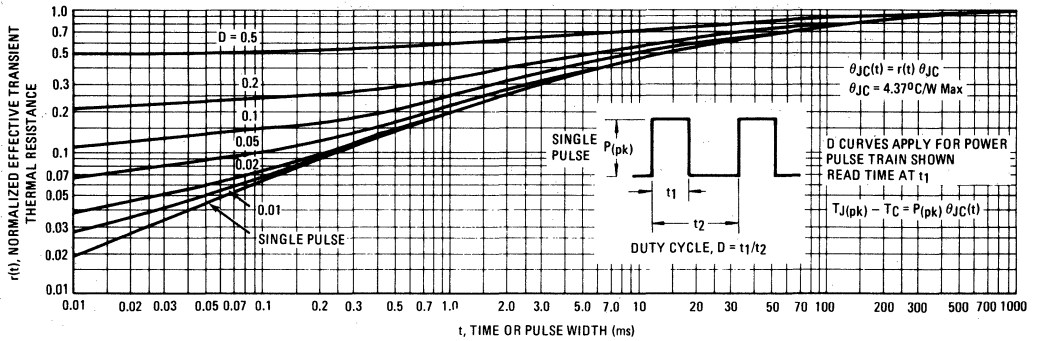
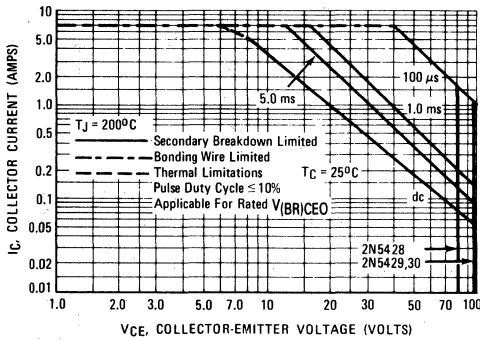


FIGURE 5 - ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_J(pk) = 200^\circ\text{C}$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_J(pk) \leq 200^\circ\text{C}$. $T_J(pk)$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 - TURN-OFF TIME

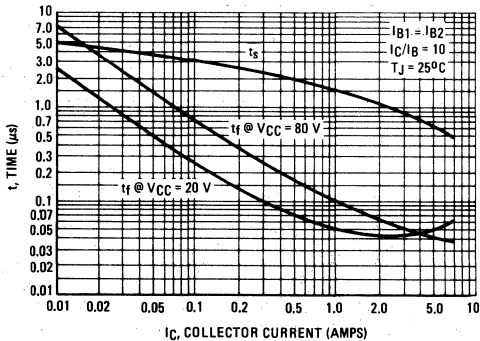


FIGURE 7 - CAPACITANCE versus VOLTAGE

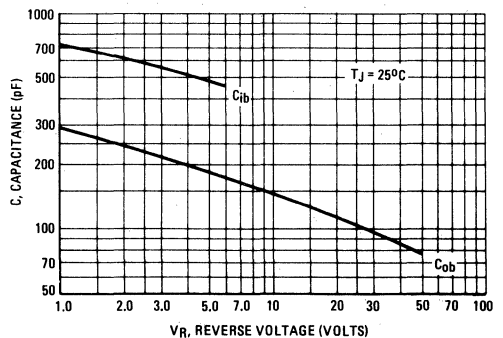


FIGURE 8 – DC CURRENT GAIN

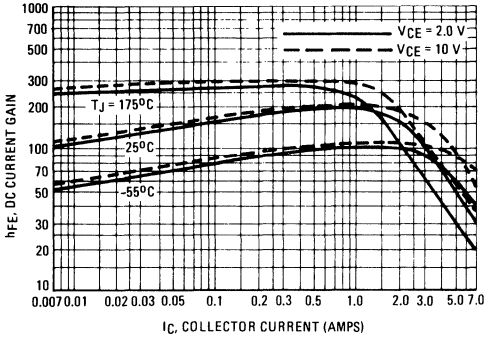


FIGURE 9 – COLLECTOR SATURATION REGION

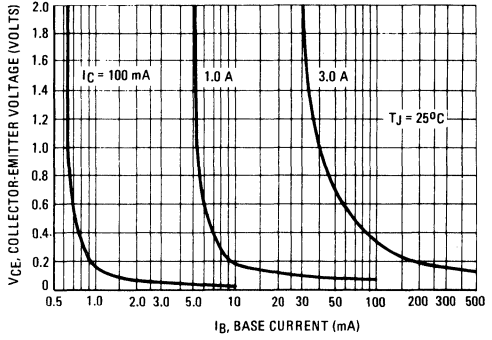


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

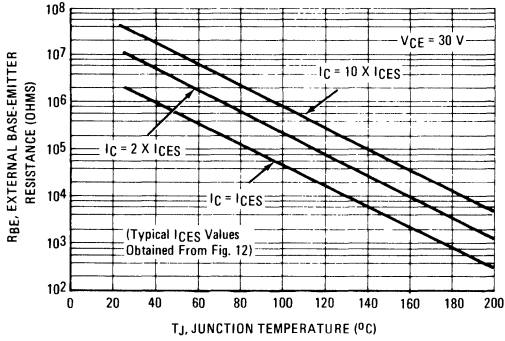


FIGURE 11 – "ON" VOLTAGES

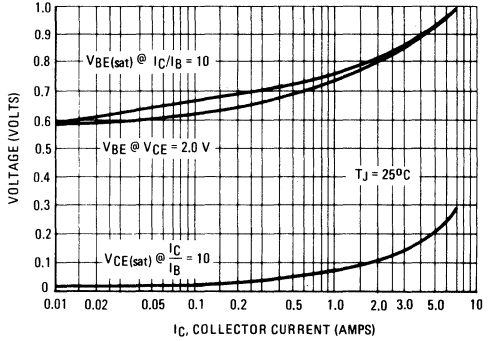


FIGURE 12 – COLLECTOR CUT-OFF REGION

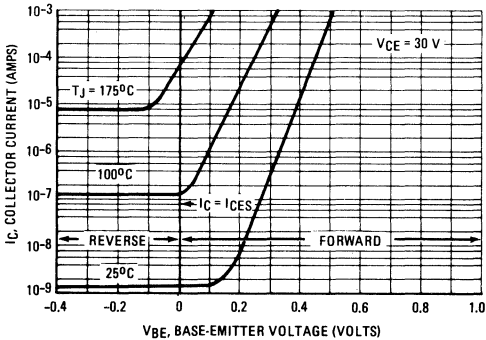
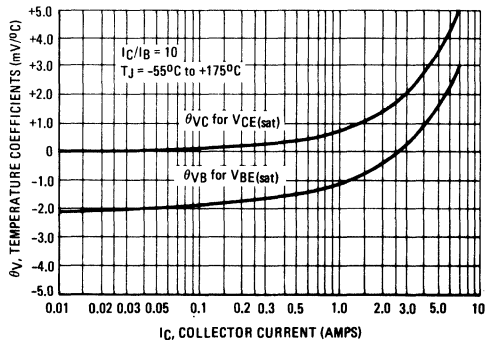


FIGURE 13 – TEMPERATURE COEFFICIENTS



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

NPN	PNP
2N5629	2N6029
2N5630	2N6030
2N5631	2N6031

HIGH-VOLTAGE – HIGH POWER TRANSISTORS

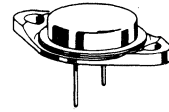
... designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 100 \text{ Vdc} - 2N5629, 2N6029$
 $= 120 \text{ Vdc} - 2N5630, 2N6030$
 $= 140 \text{ Vdc} - 2N5631, 2N6031$
- High DC Current Gain – @ $I_C = 8.0 \text{ Adc}$
 $h_{FE} = 25 \text{ (Min)} - 2N5629, 2N6029$
 $= 20 \text{ (Min)} - 2N5630, 2N6030$
 $= 15 \text{ (Min)} - 2N5631, 2N6031$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max)} @ I_C = 10 \text{ Adc}$

16 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

100-120-140 VOLTS
200 WATTS



*MAXIMUM RATINGS

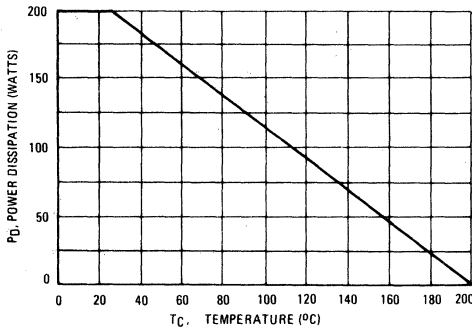
Rating	Symbol	2N5629 2N6029	2N5630 2N6030	2N5631 2N6031	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current	Continuous	← 16 →			Adc
		Peak			
Base Current	Continuous	← 5.0 →			Adc
		Derate above 25°C			
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	← 200 →			Watts
		Derate above 25°C			
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

*THERMAL CHARACTERISTICS

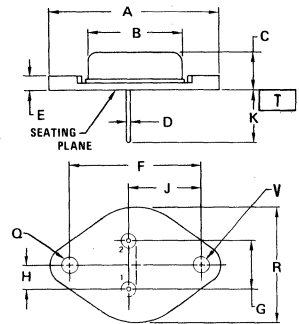
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



Safe Area Curves are indicated by Figure 5. All Limits are applicable and must be observed.



STYLE 1: PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 3: PIN 1. ANODE
2. CATHODE

NOTES:

1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\text{HOLE Q: } \text{Ø } 0.25 (0.010) \text{ @ } T | V \text{ @}$
3. POSITIONAL TOLERANCE FOR LEADS:
 $\text{LEADS: } \text{Ø } 0.30 (0.012) \text{ @ } T | V \text{ @ } Q \text{ @}$
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	30.15	BSC	1.187	BSC
G	10.92	BSC	0.430	BSC
H	5.46	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

2N5629, 2N5630, 2N5631 NPN 2N6029, 2N6030, 2N6031 PNP

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mAdc}$, $I_B = 0$)	2N5629, 2N6029 2N5630, 2N6030 2N5631, 2N6031	$V_{CE0(sus)}$	100 120 140	— — —	Vdc
Collector-Emitter Cutoff Current ($V_{CE} = 50 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 60 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 70 \text{ Vdc}$, $I_B = 0$)	2N5629, 2N6029 2N5630, 2N6030 2N5631, 2N6031	I_{CEO}	— — —	2.0 2.0 2.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = \text{Rated } V_{CB}$, $V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CB}$, $V_{EB(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)		I_{CEX}	— —	2.0 7.0	mAdc
Collector-Base Cutoff Current ($V_{CB} = \text{Rated } V_{CB}$, $I_E = 0$)		I_{CBO}	—	2.0	mAdc
Emitter-Base Cutoff Current ($V_{BE} = 7.0 \text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	5.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 8.0 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 16 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$)	2N5629, 2N6029 2N5630, 2N6030 2N5631, 2N6031 All Types	h_{FE}	25 20 15 4.0	100 80 60 —	—
Collector-Emitter Saturation Voltage ($I_C = 10 \text{ Adc}$, $I_B = 1.0 \text{ Adc}$) ($I_C = 16 \text{ Adc}$, $I_B = 4.0 \text{ Adc}$)	All Types	$V_{CE(sat)}$	— —	1.0 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10 \text{ Adc}$, $I_B = 1.0 \text{ Adc}$)		$V_{BE(sat)}$	—	1.8	Vdc
Base-Emitter On Voltage ($I_C = 8.0 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$)		$V_{BE(on)}$	—	1.5	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product (2) ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 20 \text{ Vdc}$, $f_{test} = 0.5 \text{ MHz}$)		f_T	1.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	2N5629, 30, 31 2N6029, 30, 31	C_{ob}	—	500 1000	pF
Small-Signal Current Gain ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)		h_{fe}	15	—	—

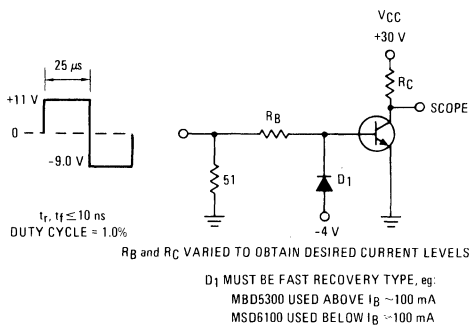
* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\geq 2.0\%$.

(2) $f_T = |h_{fe}| \cdot f_{test}$

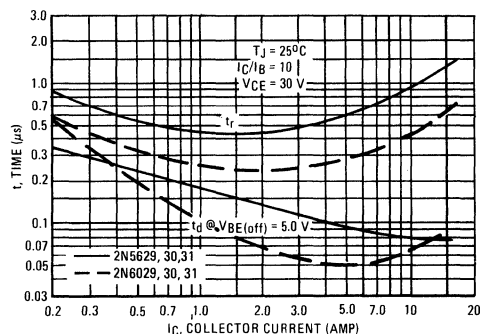
3

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For PNP test circuit, reverse all polarities and D_1 .

FIGURE 3 – TURN-ON TIME



2N5629, 2N5630, 2N5631 NPN
2N6029, 2N6030, 2N6031 PNP

FIGURE 4 – THERMAL RESPONSE

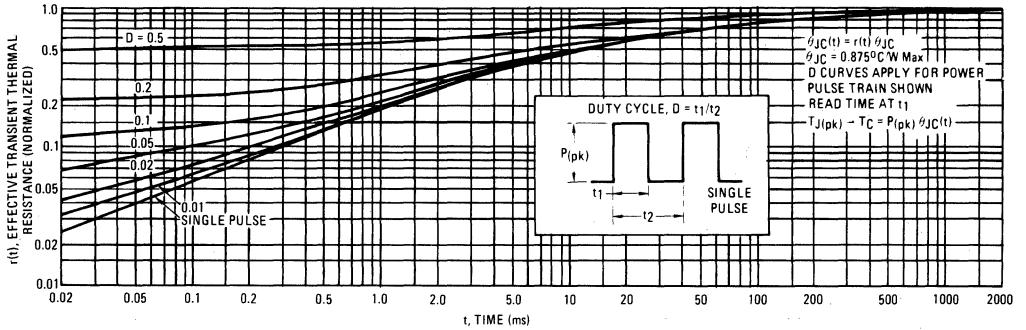
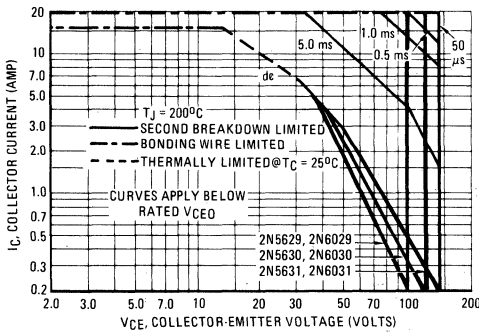


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

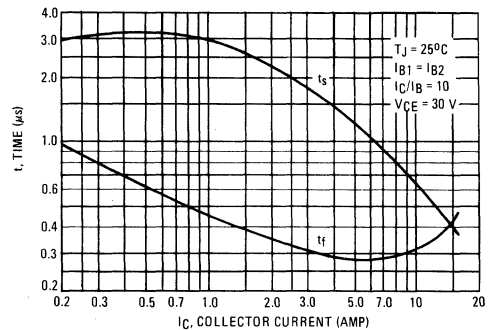
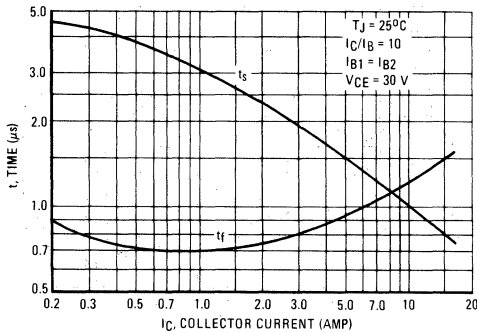
The data of Figure 5 is based on $T_J(pk) = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(pk) \leq 200^\circ\text{C}$. $T_J(pk)$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

NPN
2N5629, 2N5630, 2N5631

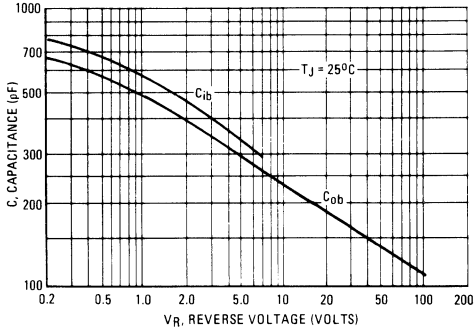
PNP
2N6029, 2N6030, 2N6031

FIGURE 6 – TURN-OFF TIME



2N5629, 2N5630, 2N5631 NPN
2N6029, 2N6030, 2N6031 PNP

NPN
2N5629, 2N5630, 2N5631



PNP
2N6029, 2N6030, 2N6031

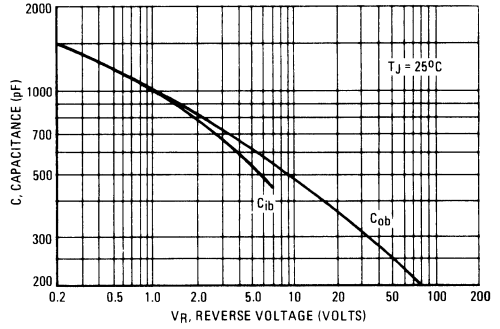


FIGURE 7 – CAPACITANCE

FIGURE 8 – DC CURRENT GAIN

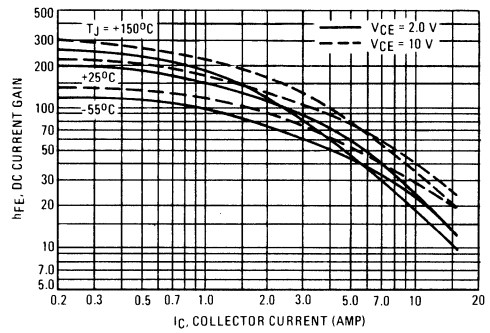
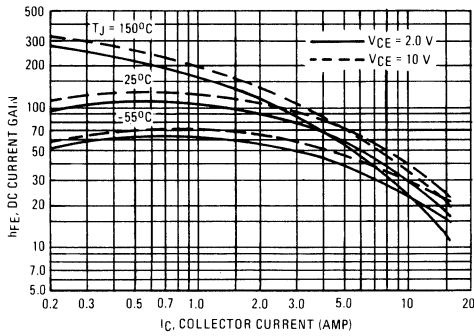
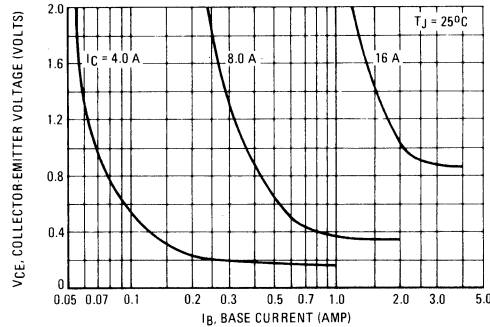
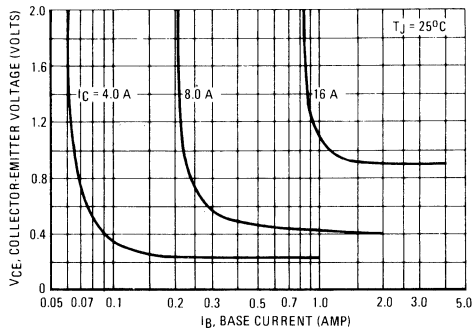


FIGURE 9 – COLLECTOR SATURATION REGION



2N5655
2N5656
2N5657

**PLASTIC NPN SILICON HIGH-VOLTAGE
 POWER TRANSISTOR**

... designed for use in line-operated equipment such as audio output amplifiers; low-current, high-voltage converters; and AC line relays

- Excellent DC Current Gain – $h_{FE} = 30-250$ @ $I_C = 100$ mA
- Current-Gain – Bandwidth Product –
 $f_T = 10$ MHz (Min) @ $I_C = 50$ mA
- Packaged in Thermopad Case for Low Cost

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON
250-300-350 VOLTS
20 WATTS

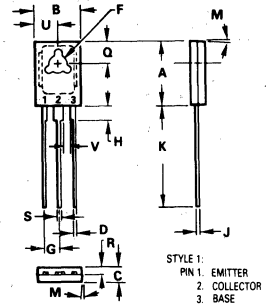
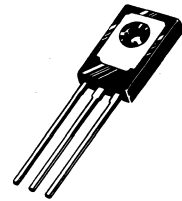
***MAXIMUM RATINGS**

Rating	Symbol	2N5655	2N5656	2N5657	Unit
Collector-Emitter Voltage	V_{CE0}	250	300	350	Vdc
Collector-Base Voltage	V_{CB}	275	325	375	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current – Continuous	I_C	← 0.5 →			Adc
Collector Current – Peak		← 1.0 →			Adc
Base Current	I_B	← 0.25 →			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	20			Watts
Derate above 25°C		0.16			W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^\circ\text{C/W}$

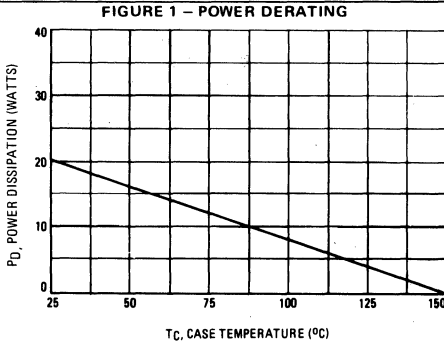
*Indicates JEDEC Registered Data



NOTES:
 1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3" TYP		3" TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.84	0.88	0.032	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-225AA



Safe Area Limits are indicated by Figures 3 and 4. Both limits are applicable and must be observed.

2N5655, 2N5656, 2N5657

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ($I_C = 100$ mA dc (inductive), $L = 50$ mH)	2N5655 2N5656 2N5657	$V_{CE(sus)}$	250 300 350	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 1.0$ mA dc, $I_B = 0$)	2N5655 2N5656 2N5657	$V_{(BR)CEO}$	250 300 350	Vdc
Collector Cutoff Current ($V_{CE} = 150$ Vdc, $I_B = 0$) ($V_{CE} = 200$ Vdc, $I_B = 0$) ($V_{CE} = 250$ Vdc, $I_B = 0$)	2N5655 2N5656 2N5657	I_{CEO}	— — —	0.1 0.1 0.1
Collector Cutoff Current ($V_{CE} = 250$ Vdc, $V_{EB(off)} = 1.5$ Vdc) ($V_{CE} = 300$ Vdc, $V_{EB(off)} = 1.5$ Vdc) ($V_{CE} = 350$ Vdc, $V_{EB(off)} = 1.5$ Vdc) ($V_{CE} = 150$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 100^\circ\text{C}$) ($V_{CE} = 200$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 100^\circ\text{C}$) ($V_{CE} = 250$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 100^\circ\text{C}$)	2N5655 2N5656 2N5657 2N5655 2N5656 2N5657	I_{CEX}	— — — — — —	0.1 0.1 0.1 1.0 1.0 1.0
Collector Cutoff Current ($V_{CB} = 275$ Vdc, $I_E = 0$) ($V_{CB} = 325$ Vdc, $I_E = 0$) ($V_{CB} = 375$ Vdc, $I_E = 0$)	2N5655 2N5656 2N5657	I_{CBO}	— — —	10 10 10
Emitter Cutoff Current ($V_{EB} = 6.0$ Vdc, $I_C = 0$)		I_{EBO}	—	10

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 50$ mA dc, $V_{CE} = 10$ Vdc) ($I_C = 100$ mA dc, $V_{CE} = 10$ Vdc) ($I_C = 250$ mA dc, $V_{CE} = 10$ Vdc) ($I_C = 500$ mA dc, $V_{CE} = 10$ Vdc)		h_{FE}	25 30 15 5.0	— 250 — —
Collector-Emitter Saturation Voltage (1) ($I_C = 100$ mA dc, $I_B = 10$ mA dc) ($I_C = 250$ mA dc, $I_B = 25$ mA dc) ($I_C = 500$ mA dc, $I_B = 100$ mA dc)		$V_{CE(sat)}$	— — —	1.0 2.5 10
Base-Emitter Voltage (1) ($I_C = 100$ mA dc, $V_{CE} = 10$ Vdc)		V_{BE}	—	1.0

DYNAMIC CHARACTERISTICS

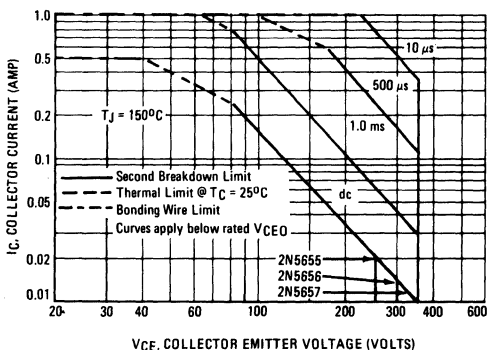
Current-Gain-Bandwidth Product (2) ($I_C = 50$ mA dc, $V_{CE} = 10$ Vdc, $f = 10$ MHz)		f_T	10	—
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f = 100$ kHz)		C_{ob}	—	25
Small-Signal Current Gain ($I_C = 100$ mA dc, $V_{CE} = 10$ Vdc, $f = 1.0$ kHz)		h_{fe}	20	—

*Indicates JEDEC Registered Data for 2N5655 Series.

(1) Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$.

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 3 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 – CURRENT GAIN

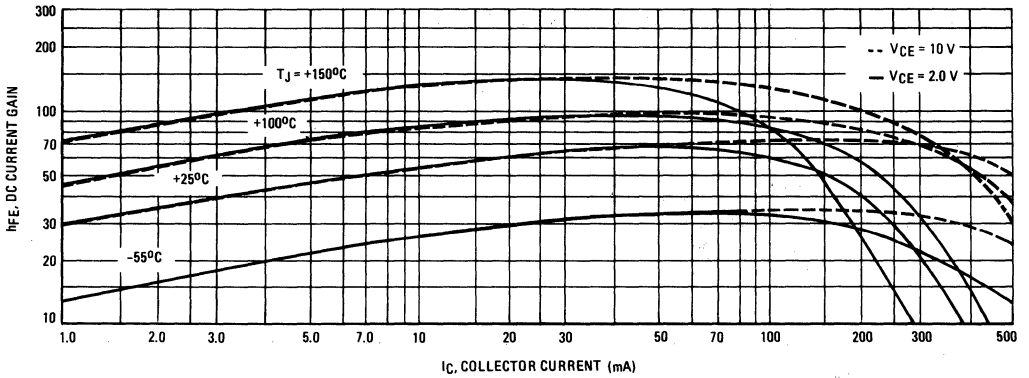


FIGURE 5 – "ON" VOLTAGES

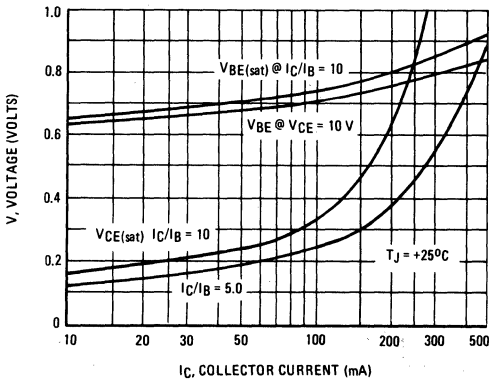


FIGURE 6 – CAPACITANCE

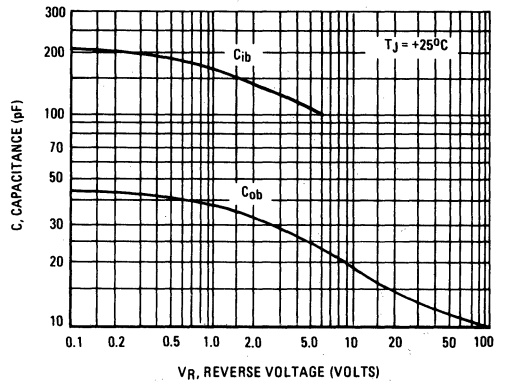


FIGURE 7 – TURN-ON TIME

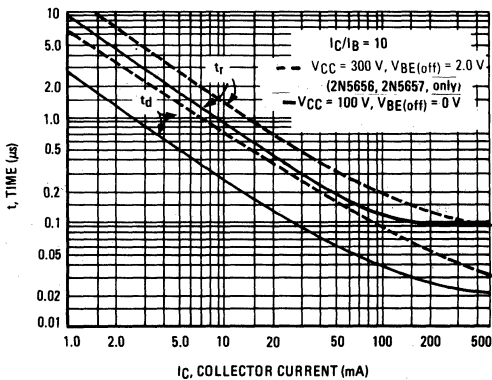
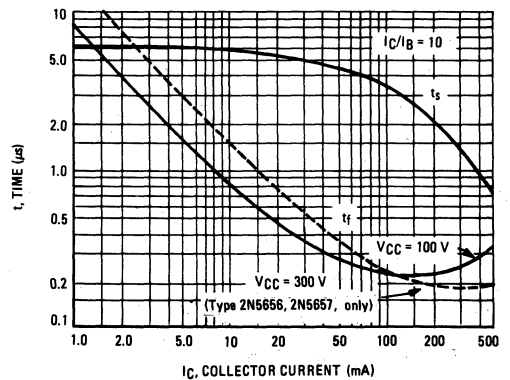


FIGURE 8 – TURN-OFF TIME



PNP
2N5683, 2N5684
NPN
2N5685, 2N5686

HIGH-CURRENT COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for use in high-power amplifier and switching circuit applications.

- High Current Capability – I_C Continuous = 50 Amperes.
- DC Current Gain –
 $h_{FE} = 15 - 60 @ I_C = 25 \text{ Adc}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) @ } I_C = 25 \text{ Adc}$

50 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
300 WATTS



***MAXIMUM RATINGS**

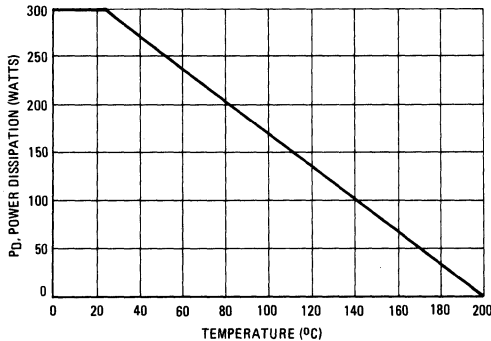
Rating	Symbol	2N5683 2N5685	2N5684 2N5686	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	50		Adc
Base Current	I_B	15		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	300 1.715		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

***THERMAL CHARACTERISTICS**

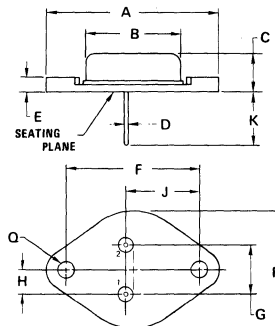
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.584	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



STYLE 1:
 PIN 1, BASE
 2, EMITTER
 CASE, COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.80	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

2N5683, 2N5684 PNP, 2N5685, 2N5686 NPN

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

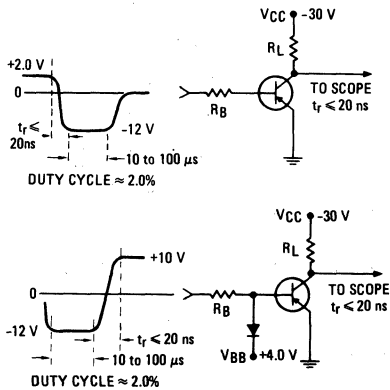
Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Note 1) ($I_C = 0.2 \text{ Adc}, I_B = 0$)	2N5683, 2N5685 2N5684, 2N5686	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}, I_B = 0$) ($V_{CE} = 40 \text{ Vdc}, I_B = 0$)	2N5683, 2N5685 2N5684, 2N5686	I_{CEO}	— —	1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 60 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$) ($V_{CE} = 80 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)	2N5683, 2N5685 2N5684, 2N5686 2N5683, 2N5685 2N5684, 2N5686	I_{CEX}	— — — —	2.0 2.0 10 10	mAdc
Collector Cutoff Current ($V_{CB} = 60 \text{ Vdc}, I_E = 0$) ($V_{CB} = 80 \text{ Vdc}, I_E = 0$)	2N5683, 2N5685 2N5684, 2N5686	I_{CBO}	— —	2.0 2.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)		I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1) ($I_C = 25 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 50 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}$)		h_{FE}	15 5.0	60 —	—
Collector-Emitter Saturation Voltage (Note 1) ($I_C = 25 \text{ Adc}, I_B = 2.5 \text{ Adc}$) ($I_C = 50 \text{ Adc}, I_B = 10 \text{ Adc}$)		$V_{CE(sat)}$	— —	1.0 5.0	Vdc
Base-Emitter Saturation Voltage (Note 1) ($I_C = 25 \text{ Adc}, I_B = 2.5 \text{ Adc}$)		$V_{BE(sat)}$	—	2.0	Vdc
Base-Emitter On Voltage (Note 1) ($I_C = 25 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$)		$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product ($I_C = 5.0 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$)		f_T	2.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz}$)	2N5683, 2N5684 2N5685, 2N5686	C_{ob}	— —	2000 1200	pF
Small-Signal Current Gain ($I_C = 10 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}, f = 1.0 \text{ kHz}$)		h_{fe}	15	—	

* Indicates JEDEC Registered Data

Note 1: Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

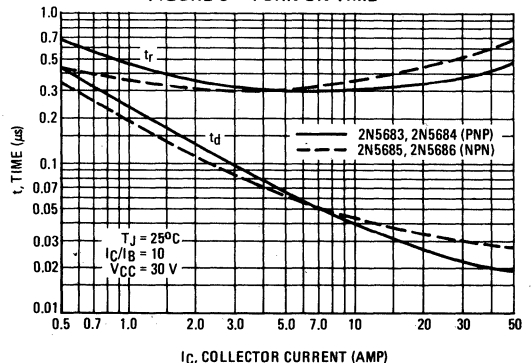
3

FIGURE 2 - SWITCHING TIME TEST CIRCUIT



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

FIGURE 3 - TURN-ON TIME



2N5683, 2N5684 PNP, 2N5685, 2N5686 NPN

FIGURE 4 – THERMAL RESPONSE

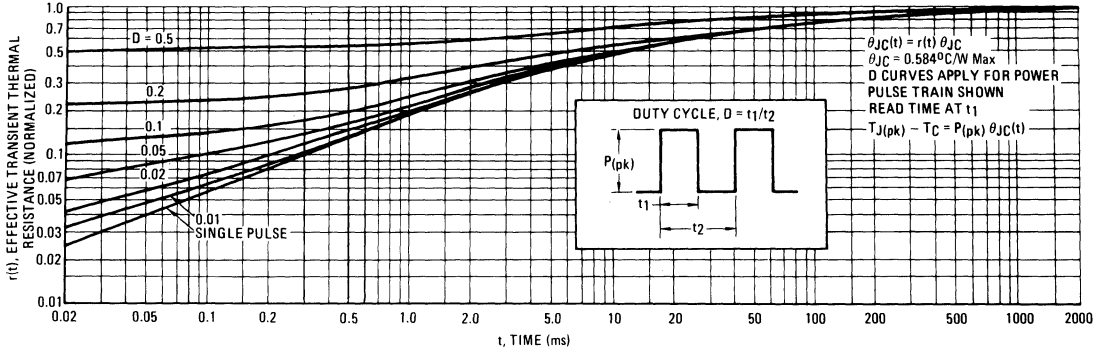
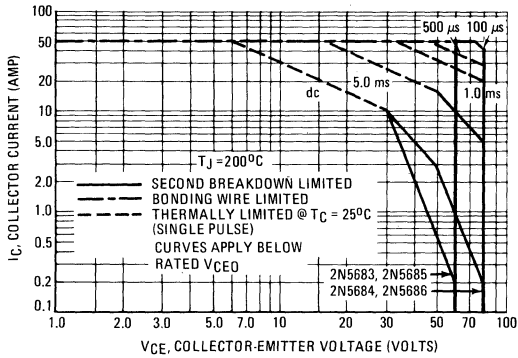


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

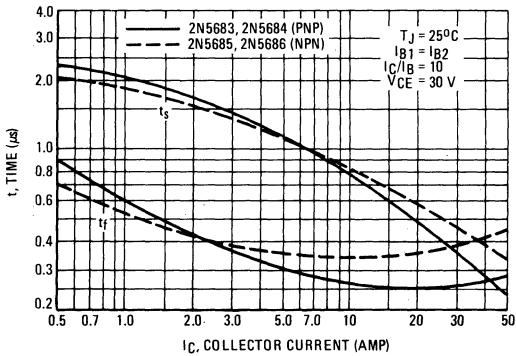
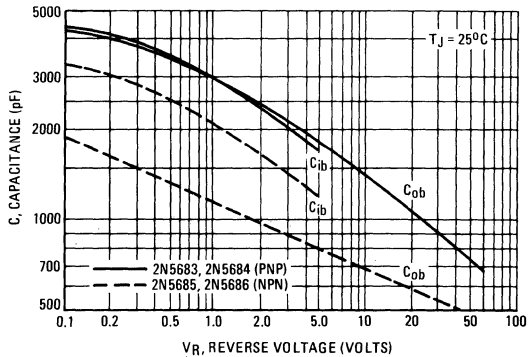


FIGURE 7 – CAPACITANCE



2N5683, 2N5684 PNP, 2N5685, 2N5686 NPN

PNP
2N5683, 2N5684

NPN
2N5685, 2N5686

FIGURE 8 - DC CURRENT GAIN

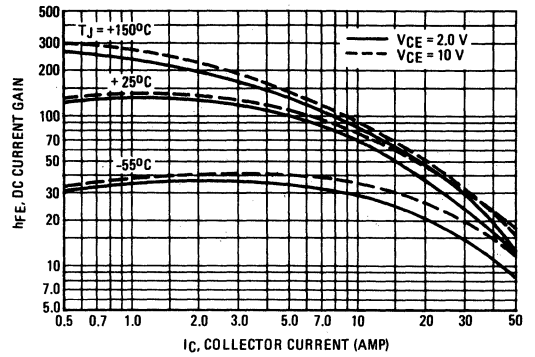
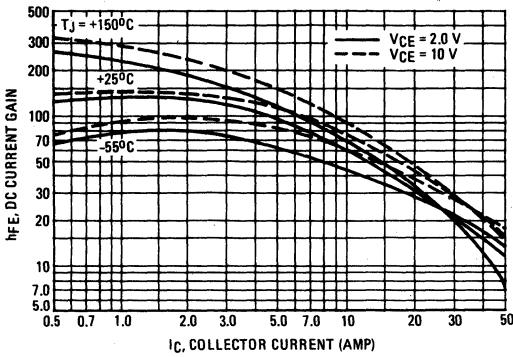


FIGURE 9 - COLLECTOR SATURATION REGION

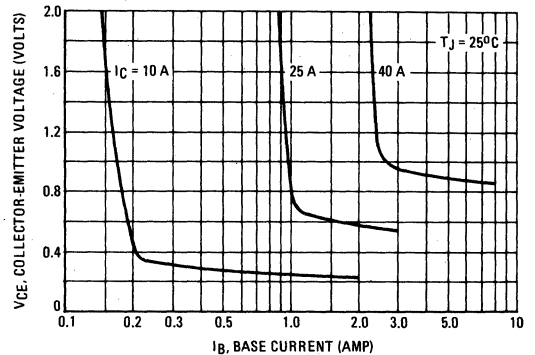
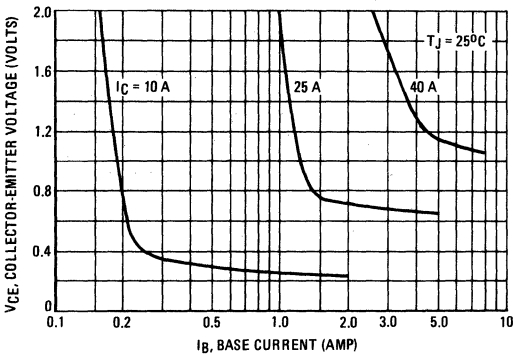
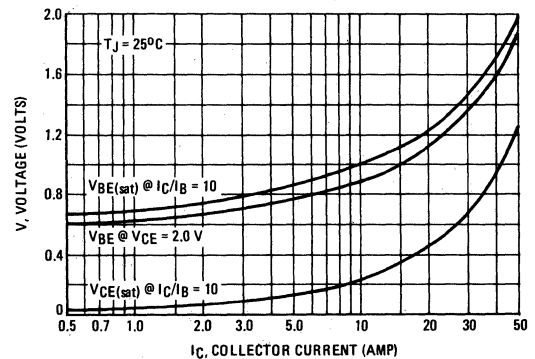
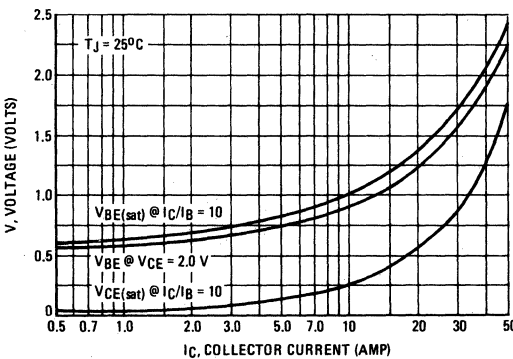


FIGURE 10 - "ON" VOLTAGES



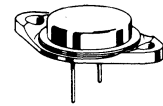
3

**HIGH-VOLTAGE HIGH-POWER
 SILICON TRANSISTORS**

... designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage —
 $V_{CE(sus)} = 100 \text{ Vdc (Min) — 2N5758}$
 $= 140 \text{ Vdc (Min) — 2N5760}$
- DC Current Gain @ $I_C = 3.0 \text{ Adc}$ —
 $h_{FE} = 25 \text{ (Min) — 2N5758}$
 $= 15 \text{ (Min) — 2N5760}$
- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$

**6 AMPERE
 POWER TRANSISTORS
 NPN SILICON
 100–140 VOLTS
 150 WATTS**



***MAXIMUM RATINGS**

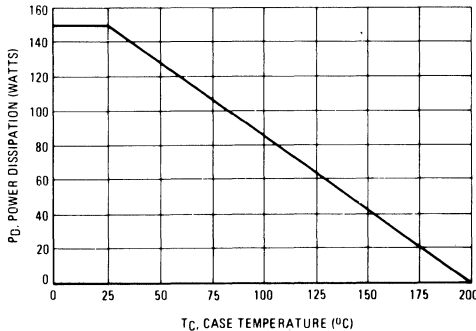
Rating	Symbol	2N5758	2N5760	Unit
Collector-Emitter Voltage	V_{CEO}	100	140	Vdc
Collector-Base Voltage	V_{CB}	100	140	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	6.0 10		A dc
Base Current	I_B	4.0		A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	150 0.857		Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

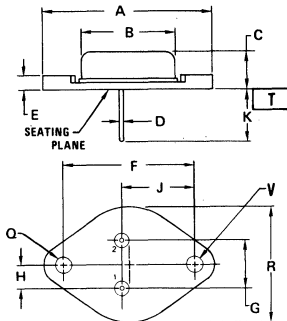
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING



Safe area limits are indicated by Figure 5.
 Both limits are applicable and must be observed.



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE: COLLECTOR

- NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
 2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\text{Ⓢ } \text{Ⓢ } 0.25 \text{ (0.010) } \text{Ⓢ } \text{Ⓢ } T \text{Ⓢ } \text{Ⓢ } V \text{Ⓢ } \text{Ⓢ } \text{Ⓢ }$
 3. POSITIONAL TOLERANCE FOR LEADS:
 $\text{Ⓢ } \text{Ⓢ } 0.30 \text{ (0.012) } \text{Ⓢ } \text{Ⓢ } T \text{Ⓢ } \text{Ⓢ } V \text{Ⓢ } \text{Ⓢ } \text{Ⓢ } \text{Ⓢ } \text{Ⓢ } \text{Ⓢ }$
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050
V	3.84	4.09	0.151	0.161

**CASE 11-01
 TO-204AA**

2N5758, 2N5760

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

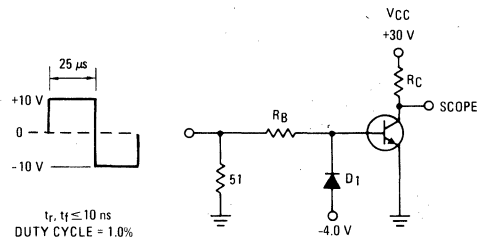
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 200 mA, I _B = 0)	V _{CEO(sus)}	100 120 140	—	Vdc
Collector Cutoff Current (V _{CE} = 50 Vdc, I _B = 0) (V _{CE} = 60 Vdc, I _B = 0) (V _{CE} = 70 Vdc, I _B = 0)	I _{CEO}	—	1.0 1.0 1.0	mA
Collector Cutoff Current (V _{CE} = Rated V _{CB} , V _{BE(off)} = 1.5 Vdc) (V _{CE} = Rated V _{CB} , V _{BE(off)} = 1.5 Vdc, T _C = 150°C)	I _{CEX}	—	1.0 5.0	mA
Collector Cutoff Current (V _{CB} = Rated V _{CB} , I _E = 0)	I _{CBO}	—	1.0	mA
Emitter Cutoff Current (V _{BE} = 7.0 Vdc, I _C = 0)	I _{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain (I _C = 3.0 A, V _{CE} = 2.0 Vdc)	h _{FE}	25	100	—
(I _C = 6.0 A, V _{CE} = 2.0 Vdc)		15	60	
(All Types)		5.0	—	
Collector-Emitter Saturation Voltage (I _C = 3.0 A, I _B = 0.3 A) (I _C = 6.0 A, I _B = 1.2 A)	V _{CE(sat)}	—	1.0 2.0	Vdc
Base-Emitter On Voltage (I _C = 3.0 A, V _{CE} = 2.0 Vdc)	V _{BE(on)}	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I _C = 0.5 A, V _{CE} = 20 Vdc, f _{test} = 0.5 MHz)	f _T	1.0	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	—	300	pF
Small-Signal Current Gain (I _C = 2.0 A, V _{CE} = 10 Vdc, f = 1.0 kHz)	h _{fe}	15	—	—

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

(2) f_T = |h_{fe}| • f_{test}

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D₁ MUST BE FAST RECOVERY TYPE, eg:
MBS300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

*For PNP test circuit, reverse all polarities and D1.

FIGURE 3 – TURN-ON TIME

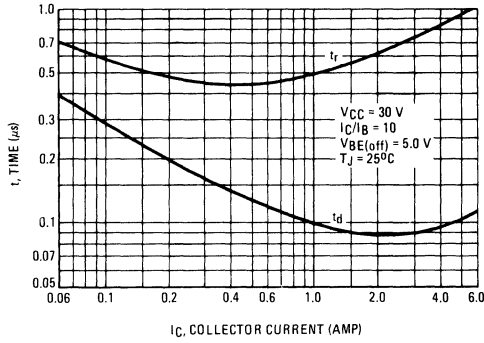


FIGURE 4 – THERMAL RESPONSE

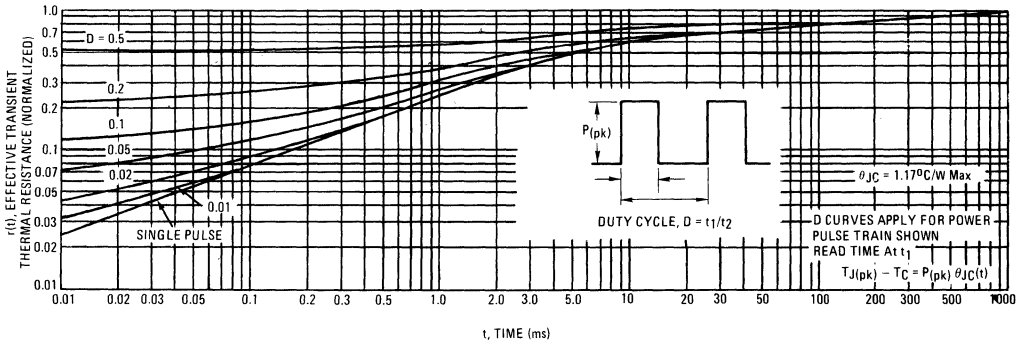
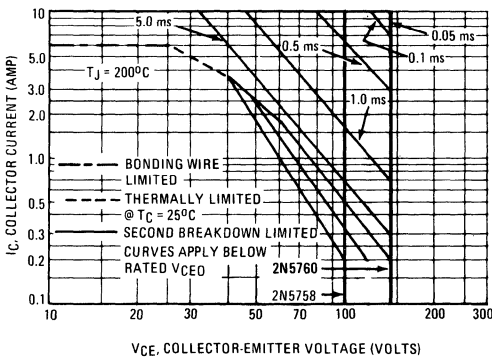


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 - TURN-OFF TIME

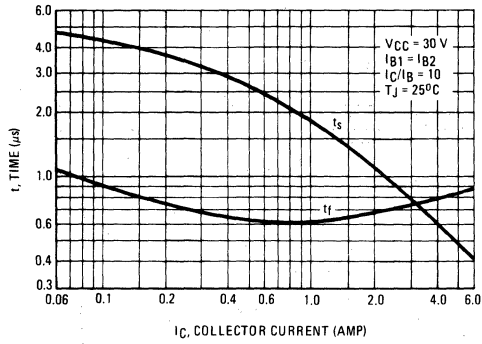


FIGURE 7 - CAPACITANCE

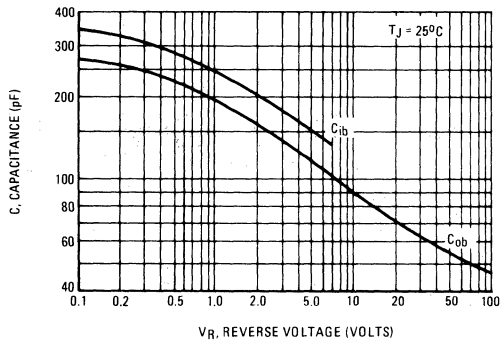
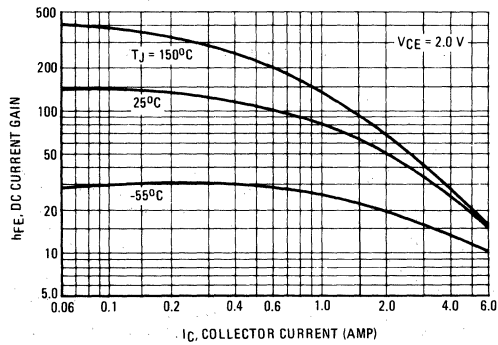


FIGURE 8 - DC CURRENT GAIN



PNP
2N5875, 2N5876
NPN
2N5877, 2N5878

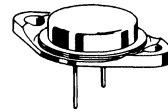
**COMPLEMENTARY SILICON
 HIGH-POWER TRANSISTORS**

... designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) @ } I_C = 5.0 \text{ Adc}$
- Low Leakage Current –
 $I_{CEX} = 0.5 \text{ mAdc (Max) @ Rated Voltage}$
- Excellent DC Current Gain –
 $h_{FE} = 20 \text{ (Min) @ } I_C = 4.0 \text{ Adc}$
- High Current Gain – Bandwidth Product –
 $f_T = 4.0 \text{ MHz (Min) @ } I_C = 0.5 \text{ A}$

**10 AMPERE
 COMPLEMENTARY SILICON
 POWER TRANSISTORS**

**60-80 VOLTS
 150 WATTS**



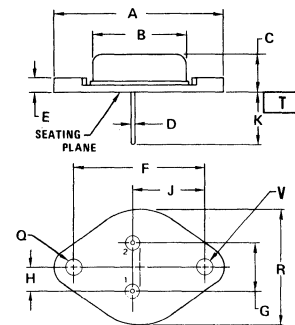
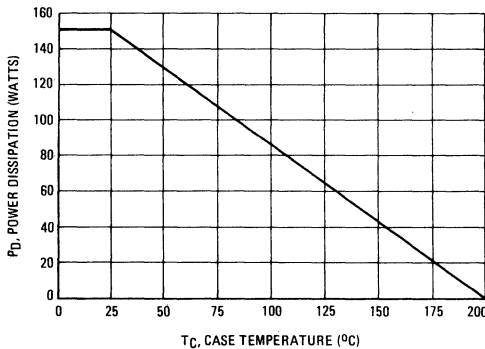
***MAXIMUM RATINGS**

Rating	Symbol	2N5875 2N5877	2N5876 2N5878	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	10 20		Adc
Base Current	I_B	4.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	150 0.857		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C/W}$

FIGURE 1 – POWER DERATING



STYLE 1: PIN 1. BASE
 2. EMITTER
 CASE: COLLECTOR

STYLE 3: PIN 1. ANODE
 2. CATHODE

- NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
 2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\phi \pm 0.25 (0.010) \text{ @ } T | V \text{ @}$
 3. POSITIONAL TOLERANCE FOR LEADS:
 $\phi \pm 0.30 (0.012) \text{ @ } T | V \text{ @ } Q \text{ @}$
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050
V	3.84	4.09	0.151	0.161

**CASE 11-01
 TO-204AA**

2N5875, 2N5876 PNP, 2N5877, 2N5878 NPN

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	60 80	— —	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	— —	1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	— — — —	0.5 0.5 5.0 5.0	mAdc
Collector Cutoff Current ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	— —	0.5 0.5	mAdc
Emitter Cutoff Current ($V_{EB} = 5.0 \text{ Vdc}$, $I_E = 0$)	I_{EBO}	—	1.0	mAdc

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 10 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	35 20 4.0	— 100 —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 5.0 \text{ Adc}$, $I_B = 0.5 \text{ Adc}$) ($I_C = 10 \text{ Adc}$, $I_B = 2.5 \text{ Adc}$)	$V_{CE(sat)}$	— —	1.0 3.0	Vdc
Base-Emitter Saturation Voltage (1) ($I_C = 10 \text{ Adc}$, $I_B = 2.5 \text{ Adc}$)	$V_{BE(sat)}$	—	2.5	Vdc
Base-Emitter On Voltage (1) ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.5	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain - Bandwidth Product (2) ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 1.0 \text{ MHz}$)	f_T	4.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	C_{ob}	— — —	500 300	pF
Small-Signal Current Gain ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	20	—	—

SWITCHING CHARACTERISTICS

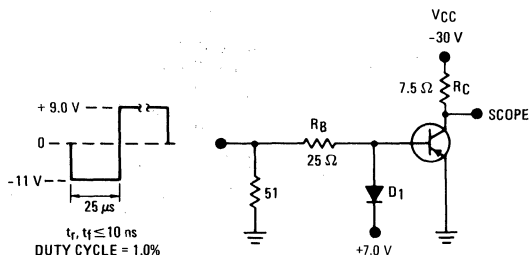
Rise Time	$(V_{CC} = 30 \text{ Vdc}$, $I_C = 4.0 \text{ Adc}$, $I_{B1} = I_{B2} = 0.4 \text{ Adc}$, See Figure 2)	t_r	—	0.7	μs
Storage Time		t_s	—	1.0	μs
Fall Time		t_f	—	0.8	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 - SWITCHING TIME TEST CIRCUIT

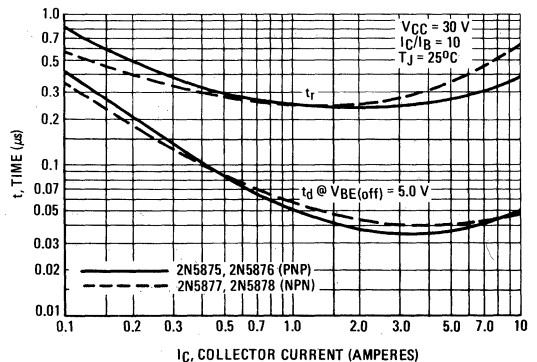


FOR CURVES OF FIGURES 3 and 6,
 R_B and R_C ARE VARIED TO OBTAIN
DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.
MBD5300 USED ABOVE $I_B \approx 100 \text{ mA}$
MSD6100 USED BELOW $I_B \approx 100 \text{ mA}$

For NPN test circuit,
reverse all polarities.

FIGURE 3 - TURN-ON TIME



2N5875, 2N5876 PNP, 2N5877, 2N5878 NPN

FIGURE 4 – THERMAL RESPONSE

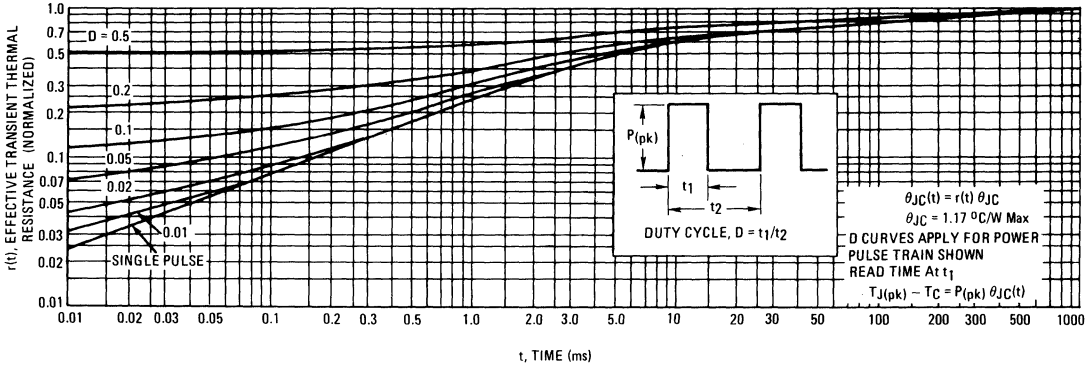
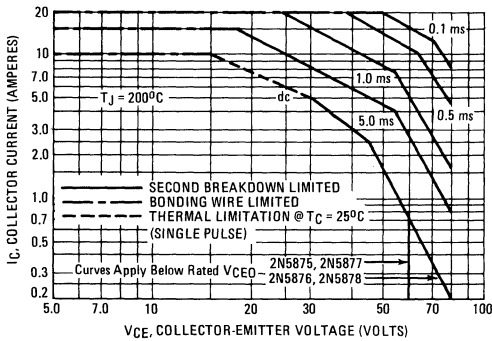


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

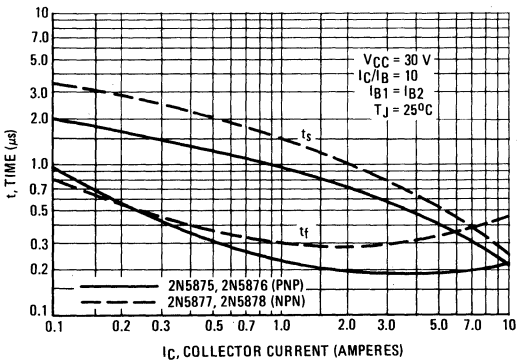
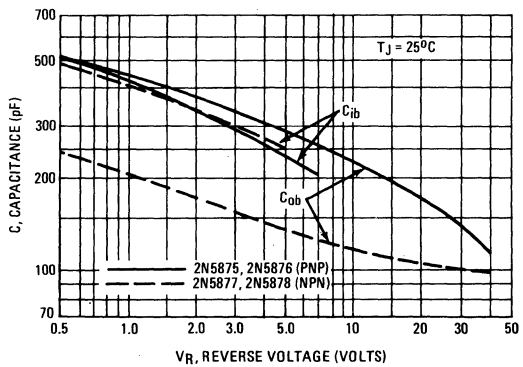


FIGURE 7 – CAPACITANCE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
2N5879, 2N5880
NPN
2N5881, 2N5882

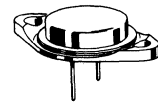
**COMPLEMENTARY SILICON
HIGH-POWER TRANSISTORS**

... designed for general-purpose power amplifier and switching applications.

- Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 60 \text{ Vdc (Min) - 2N5879, 2N5881}$
 $= 80 \text{ Vdc (Min) - 2N5880, 2N5882}$
- DC Current Gain –
 $h_{FE} = 20 \text{ (Min) @ } I_C = 6.0 \text{ Adc}$
- Low Collector – Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) @ } I_C = 7.0 \text{ Adc}$
- High Current – Gain-Bandwidth Product –
 $f_T = 4.0 \text{ MHz (Min) @ } I_C = 1.0 \text{ Adc}$
- Recommended for New Circuit Designs

**15 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS**

**60-80 VOLTS
160 WATTS**



***MAXIMUM RATINGS**

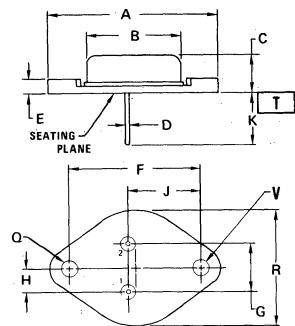
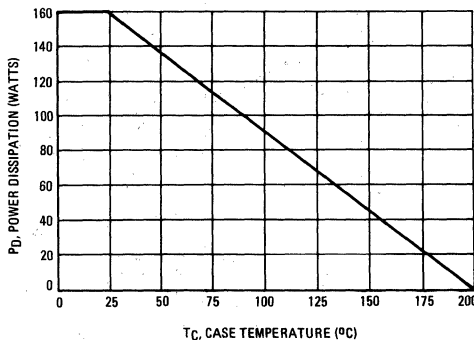
Rating	Symbol	2N5879 2N5881	2N5880 2N5882	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	15 30		A dc
Base Current	I_B	5.0		A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	160 0.915		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.1	$^\circ\text{C/W}$

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

FIGURE 1 – POWER DERATING



STYLE 1:
PIN 1: BASE
2: EMITTER
CASE: COLLECTOR

- NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\text{H} \begin{matrix} \text{H} \\ \text{H} \end{matrix} 0.25 (0.010) \text{ T V } \text{M}$
3. POSITIONAL TOLERANCE FOR LEADS:
 $\text{H} \begin{matrix} \text{H} \\ \text{H} \end{matrix} 0.30 (0.012) \text{ T V } \text{M}$
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050
V	3.84	4.09	0.151	0.161

**CASE 11-01
TO-204AA**

2N5879, 2N5880 PNP, 2N5881, 2N5882 NPN

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 200 mA, I _B = 0)	V _{CEO(sus)}	60 80	—	Vdc
Collector Cutoff Current (V _{CE} = 30 Vdc, I _B = 0)	I _{CEO}	—	1.0	mA
(V _{CE} = 40 Vdc, I _B = 0)		—	1.0	
Collector Cutoff Current (V _{CE} = 60 Vdc, V _{BE(off)} = 1.5 Vdc)	I _{CEX}	—	0.5	mA
(V _{CE} = 80 Vdc, V _{BE(off)} = 1.5 Vdc)		—	0.5	
(V _{CE} = 60 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 150°C)		—	5.0	
(V _{CE} = 80 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 150°C)		—	5.0	
Collector Cutoff Current (V _{CB} = 60 Vdc, I _E = 0)	I _{CBO}	—	0.5	mA
(V _{CB} = 80 Vdc, I _E = 0)		—	0.5	
Emitter Cutoff Current (V _{EB} = 5.0 Vdc, I _C = 0)	I _{EBO}	—	1.0	mA

ON CHARACTERISTICS				
DC Current Gain (1) (I _C = 2.0 A, V _{CE} = 4.0 Vdc)	h _{FE}	35	—	—
(I _C = 6.0 A, V _{CE} = 4.0 Vdc)		20	100	
(I _C = 15 A, V _{CE} = 4.0 Vdc)		4.0	—	
Collector-Emitter Saturation Voltage (1) (I _C = 7.0 A, I _B = 0.7 A)	V _{CE(sat)}	—	1.0	Vdc
(I _C = 15 A, I _B = 3.75 A)		—	4.0	
Base-Emitter Saturation Voltage (1) (I _C = 15 A, I _B = 3.75 A)	V _{BE(sat)}	—	2.5	Vdc
Base-Emitter On Voltage (1) (I _C = 6.0 A, V _{CE} = 4.0 Vdc)	V _{BE(on)}	—	1.5	Vdc

DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (2) (I _C = 1.0 A, V _{CE} = 10 Vdc, f _{test} = 1.0 MHz)	f _T	4.0	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 100 kHz)	C _{ob}	—	600 400	pF
Small-Signal Current Gain (I _C = 2.0 A, V _{CE} = 4.0 Vdc, f = 1.0 kHz)	h _{fe}	20	—	—

SWITCHING CHARACTERISTICS					
Rise Time	(V _{CC} = 30 Vdc, I _C = 6.0 A, I _{B1} = I _{B2} = 0.6 A. See Figure 2)	t _r	—	0.7	μs
Storage Time		t _s	—	1.0	μs
Fall Time		t _f	—	0.8	μs

*Indicates JEDEC Registered Data.
 (1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
 (2) f_T = |h_{fe}| • f_{test}

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

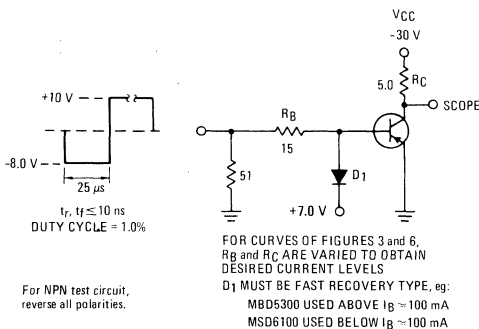
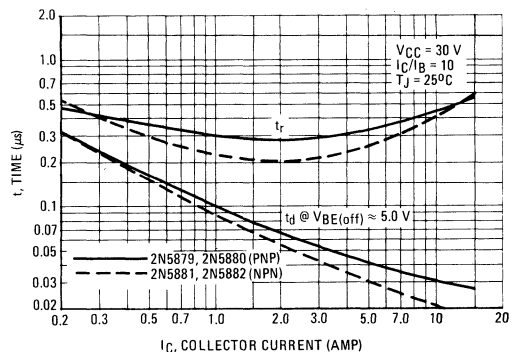


FIGURE 3 – TURN-ON TIME



2N5879, 2N5880 PNP, 2N5881, 2N5882 NPN

FIGURE 4 – THERMAL RESPONSE

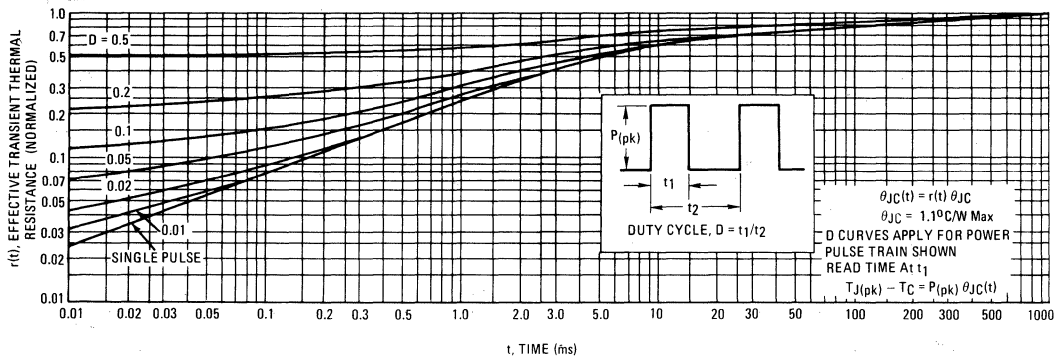
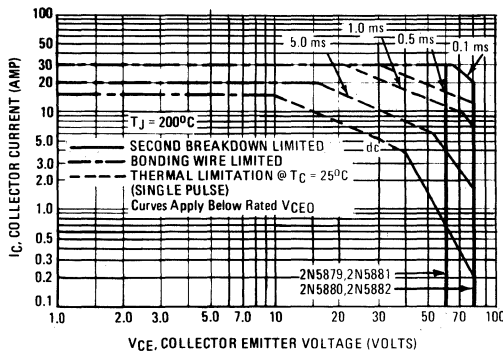


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

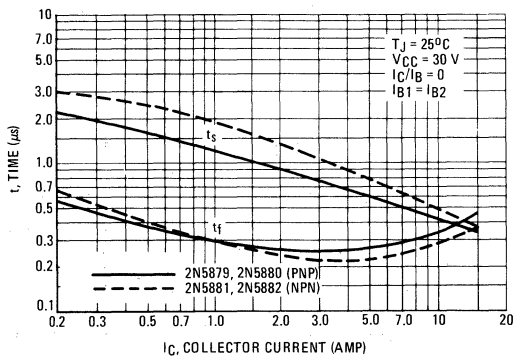
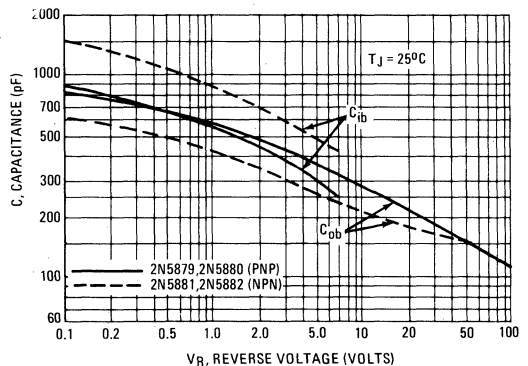


FIGURE 7 – CAPACITANCE



3

2N5879, 2N5880 PNP, 2N5881, 2N5882 NPN

PNP
2N5879, 2N5880

NPN
2N5881, 2N5882

FIGURE 8 – DC CURRENT GAIN

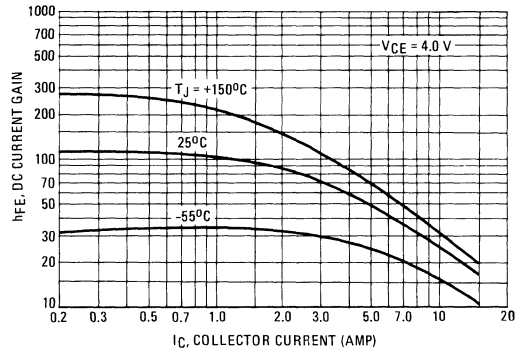
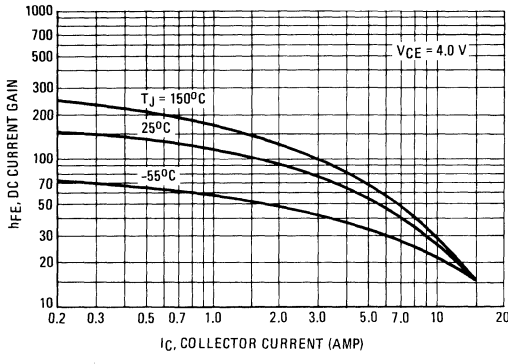


FIGURE 9 – COLLECTOR SATURATION REGION

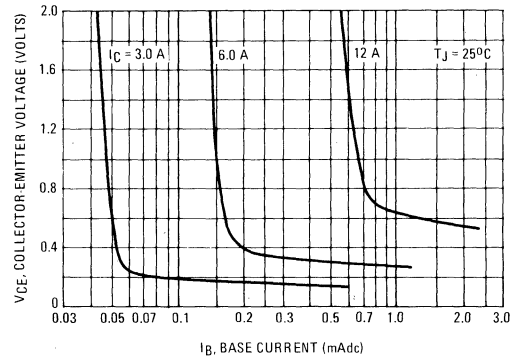
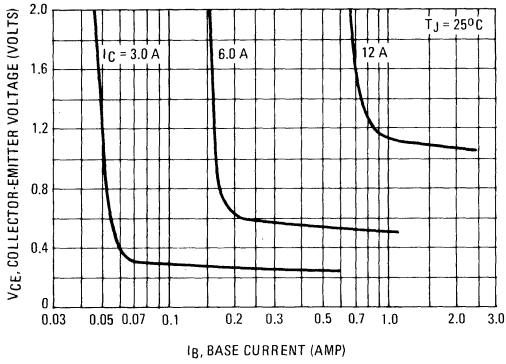
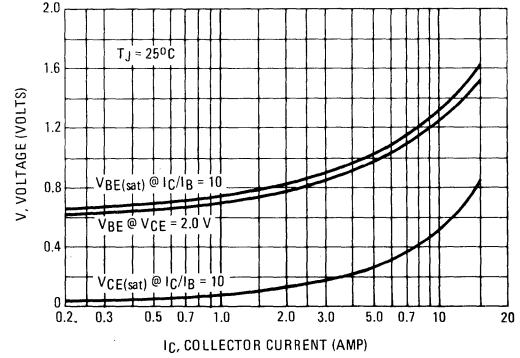
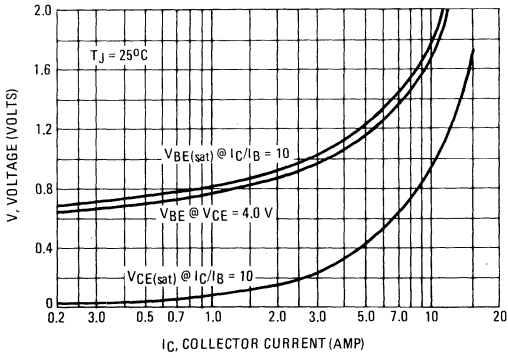


FIGURE 10 – "ON" VOLTAGES



PNP
2N5883, 2N5884
NPN
2N5885, 2N5886

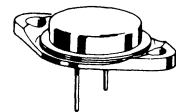
**COMPLEMENTARY SILICON
HIGH-POWER TRANSISTORS**

... designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)} = 1.0$ Vdc, (max) at $I_C = 15$ Adc
- Low Leakage Current
 $I_{CEX} = 1.0$ mA (max) at Rated Voltage
- Excellent DC Current Gain —
 $h_{FE} = 20$ (min) at $I_C = 10$ Adc
- High Current Gain Bandwidth Product —
 $f_T = 4.0$ MHz (min) at $I_C = 1.0$ Adc

25 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS

60-80 VOLTS
200 WATTS



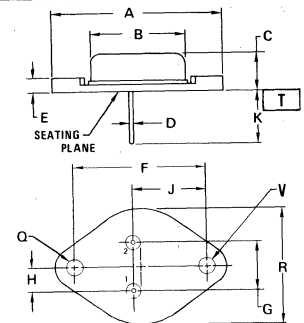
***MAXIMUM RATINGS**

Rating	Symbol	2N5883 2N5885	2N5884 2N5886	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	25 50		A dc
Base Current	I_B	7.5		A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	200 1.15		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	$^\circ\text{C/W}$

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.



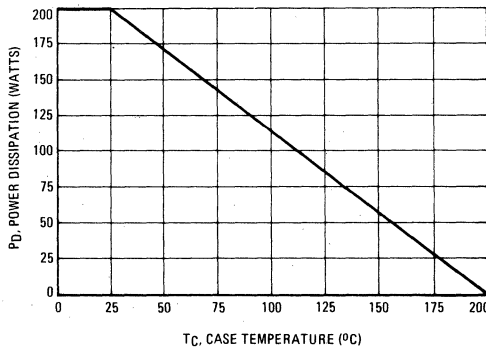
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

- NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
 2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\text{M} \varnothing 0.25 (0.010) \text{ M} \varnothing \text{T} | \text{V} \text{ M}$
 3. POSITIONAL TOLERANCE FOR LEADS:
 $\text{M} \varnothing 0.30 (0.012) \text{ M} \varnothing \text{T} | \text{V} \text{ M} \varnothing \text{Q} \text{ M}$
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

FIGURE 1 — POWER DERATING



2N5883, 2N5884 PNP, 2N5885, 2N5886 NPN

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mA dc}, I_B = 0$)	$V_{CE(sus)}$	60 80	—	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}, I_B = 0$) ($V_{CE} = 40 \text{ Vdc}, I_B = 0$)	I_{CEO}	—	2.0 2.0	mA dc
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 60 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$) ($V_{CE} = 80 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)	I_{CEX}	—	1.0 1.0 10 10	mA dc
Collector Cutoff Current ($V_{CB} = 60 \text{ Vdc}, I_E = 0$) ($V_{CB} = 80 \text{ Vdc}, I_E = 0$)	I_{CBO}	—	1.0 1.0	mA dc
Emitter Cutoff Current ($V_{EB} = 5.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	1.0	mA dc

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 3.0 \text{ A dc}, V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 10 \text{ A dc}, V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 25 \text{ A dc}, V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	35 20 4.0	— 100 —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 15 \text{ A dc}, I_B = 1.5 \text{ A dc}$) ($I_C = 25 \text{ A dc}, I_B = 6.25 \text{ A dc}$)	$V_{CE(sat)}$	—	1.0 4.0	Vdc
Base-Emitter Saturation Voltage (1) ($I_C = 25 \text{ A dc}, I_B = 6.25 \text{ A dc}$)	$V_{BE(sat)}$	—	2.5	Vdc
Base-Emitter On Voltage (1) ($I_C = 10 \text{ A dc}, V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.5	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product (2) ($I_C = 1.0 \text{ A dc}, V_{CE} = 10 \text{ Vdc}, f_{test} = 1.0 \text{ MHz}$)	f_T	4.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 1.0 \text{ MHz}$)	C_{ob}	—	1000 500	pF
Small-Signal Current Gain ($I_C = 3.0 \text{ A dc}, V_{CE} = 4.0 \text{ Vdc}, f_{test} = 1.0 \text{ kHz}$)	h_{fe}	20	—	—

SWITCHING CHARACTERISTICS

Rise Time	($V_{CC} = 30 \text{ Vdc}, I_C = 10 \text{ A dc},$ $I_{B1} = I_{B2} = 1.0 \text{ A dc}$)	t_r	—	0.7	μs
Storage Time		t_s	—	1.0	μs
Fall Time		t_f	—	0.8	μs

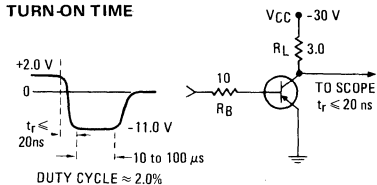
*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

(2) $f_T = |h_{fe}| \cdot f_{test}$.

FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUITS

TURN-ON TIME



TURN-OFF TIME

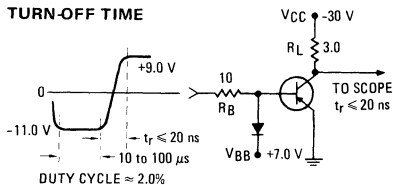
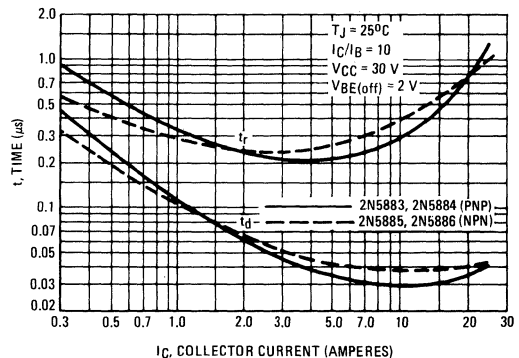


FIGURE 3 – TURN-ON TIME



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES

FIGURE 4 – THERMAL RESPONSE

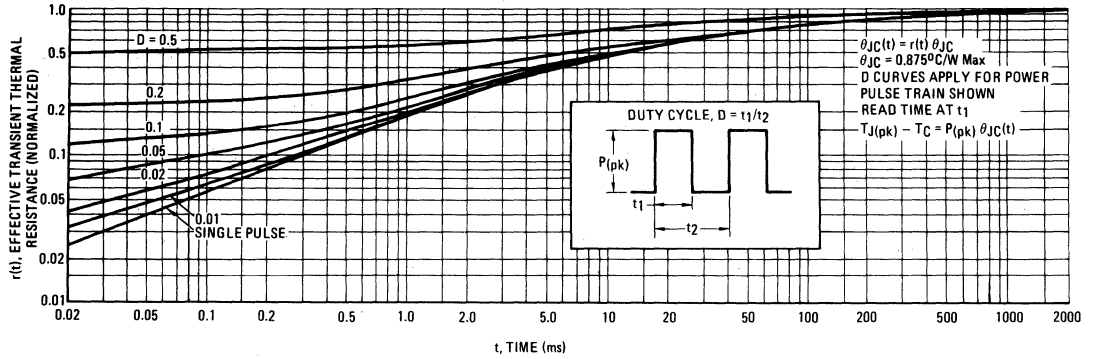
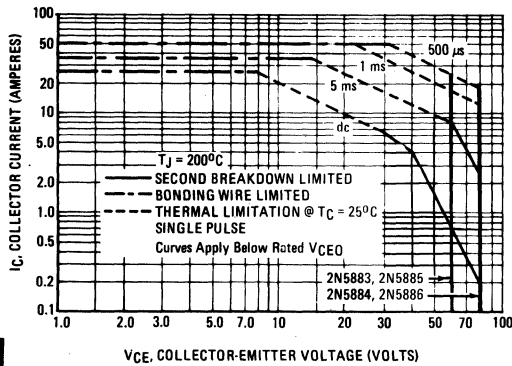


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_J(pk) = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(pk) \leq 200^\circ\text{C}$. $T_J(pk)$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

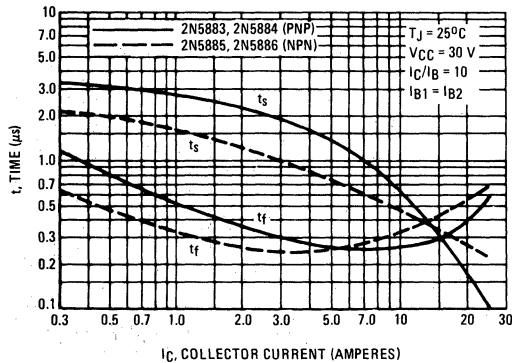
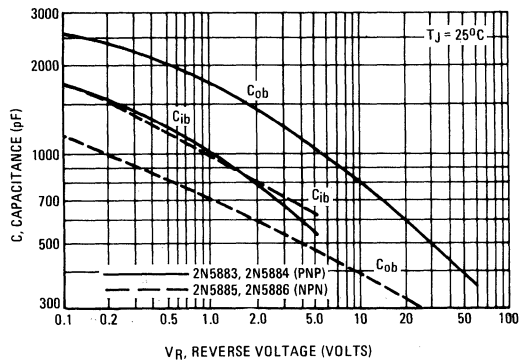


FIGURE 7 – CAPACITANCE



2N5883, 2N5884 PNP, 2N5885, 2N5886 NPN

PNP DEVICES
2N5883 and 2N5884

NPN DEVICES
2N5885 and 2N5886

FIGURE 8 – DC CURRENT GAIN

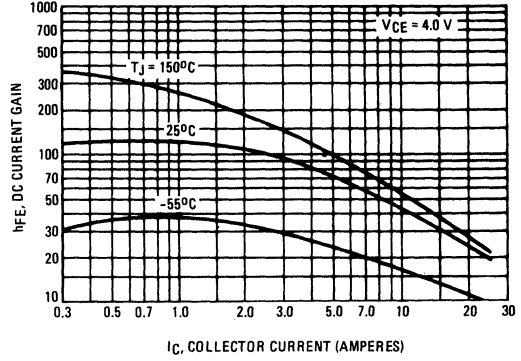
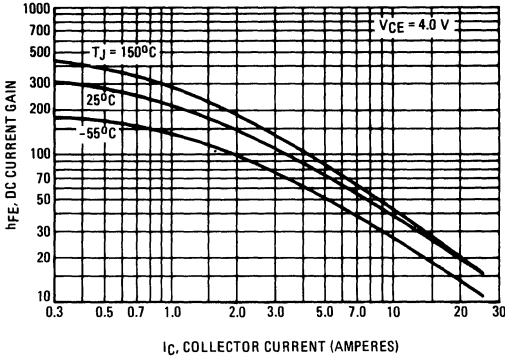


FIGURE 9 – COLLECTOR SATURATION REGION

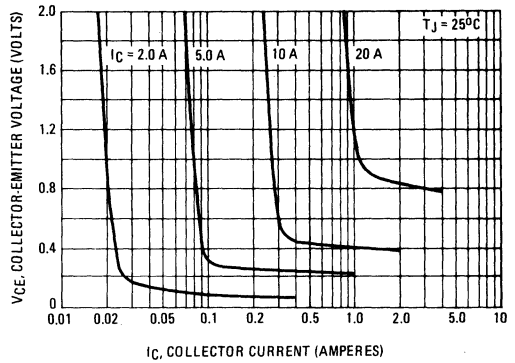
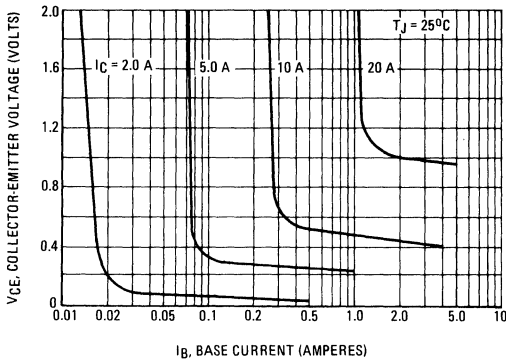
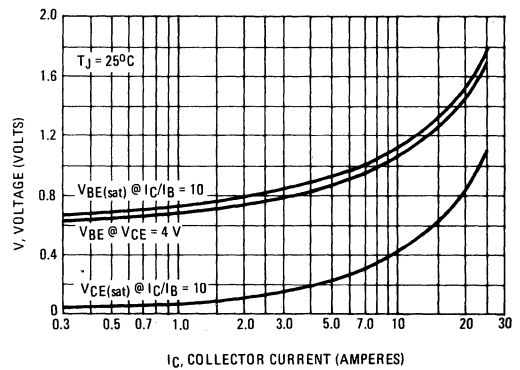
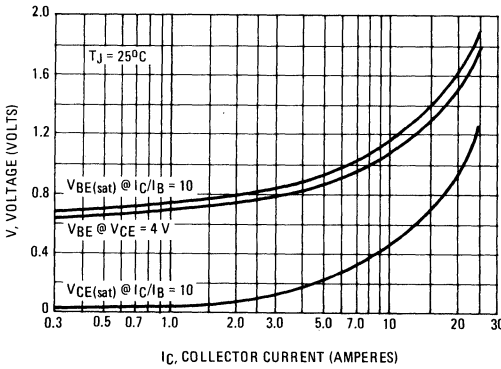


FIGURE 10 – "ON" VOLTAGES



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

PNP
2N5986, 2N5987
2N5988
NPN
2N5989, 2N5991

HIGH POWER PLASTIC COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for use in general-purpose amplifier and switching circuits.

- Collector-Base Voltage – $V_{CB0} = 60 \text{ Vdc} - 2N5986, 2N5989$
 $= 80 \text{ Vdc} - 2N5987$
 $= 100 \text{ Vdc} - 2N5988, 2N5991$
- Collector-Emitter Voltage – $V_{CE0} = 40 \text{ Vdc} - 2N5986, 2N5989$
 $= 60 \text{ Vdc} - 2N5987$
 $= 80 \text{ Vdc} - 2N5988, 2N5991$
- DC Current Gain –
 $h_{FE} = 20-120 @ I_C = 6.0 \text{ Adc}$
 $= 7.0 \text{ (Min) } @ I_C = 12 \text{ Adc}$
- Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.7 \text{ Vdc (Max) } @ I_C = 6.0 \text{ Adc}$

*MAXIMUM RATINGS

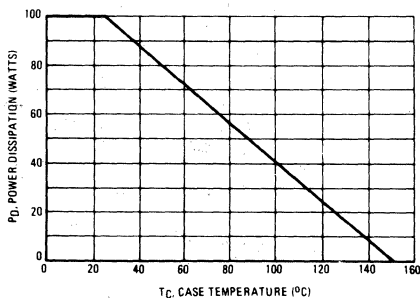
Rating	Symbol	2N5986 2N5989	2N5987	2N5988 2N5991	Unit
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Collector-Emitter Voltage	V_{CE0}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	12 20			Adc
Base Current	I_B	4.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	100 0.8			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.25	$^\circ\text{C/W}$

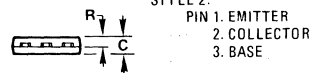
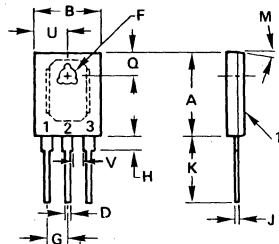
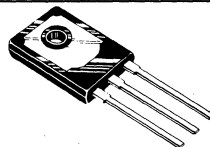
*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING



12 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

40, 60, 80 VOLTS
100 WATTS



STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

- NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	90 TYP		90 TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	—	0.080	—

CASE 90-05
TO-225AB

2N5986, 2N5987, 2N5988 PNP / 2N5989, 2N5991 NPN

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I _C = 0.2 Adc, I _B = 0)	V _{CE(sus)}	40 60 80	— — —	Vdc
Collector Cutoff Current (V _{CE} = 20 Vdc, I _B = 0) (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 40 Vdc, I _B = 0)	I _{CEO}	— — —	2.0 2.0 2.0	mA _{dc}
Collector Cutoff Current (V _{CE} = 60 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CE} = 80 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CE} = 100 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CE} = 40 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 125°C) (V _{CE} = 60 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 125°C) (V _{CE} = 80 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 125°C)	I _{CEx}	— — — — — —	200 200 200 2.0 2.0 2.0	μA _{dc} mA _{dc}
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	—	1.0	mA _{dc}
ON CHARACTERISTICS				
DC Current Gain (I _C = 1.5 Adc, V _{CE} = 2.0 Vdc) (I _C = 6.0 Adc, V _{CE} = 2.0 Vdc) (I _C = 12 Adc, V _{CE} = 2.0 Vdc)	h _{FE}	40 20 7.0	— 120 —	—
Collector-Emitter Saturation Voltage (I _C = 6.0 Adc, I _B = 0.6 Adc) (I _C = 12 Adc, I _B = 1.8 Adc)	V _{CE(sat)}	— —	0.6 1.7	Vdc
Base-Emitter Saturation Voltage (I _C = 12 Adc, I _B = 1.8 Adc)	V _{BE(sat)}	—	2.5	Vdc
Base-Emitter On Voltage (I _C = 6.0 Adc, V _{CE} = 2.0 Vdc)	V _{BE(on)}	—	1.4	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I _C = 0.5 Adc, V _{CE} = 10 Vdc, f _{test} = 1.0 MHz)	f _T	2.0	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 MHz)	C _{ob}	— —	500 300	pF
Small-Signal Current Gain (I _C = 2.0 Adc, V _{CE} = 4.0 Vdc, f = 1.0 kHz)	h _{fe}	20	—	—

*Indicates JEDEC Registered Data.

(1) f_T = |h_{fe}| • f_{test}

3

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

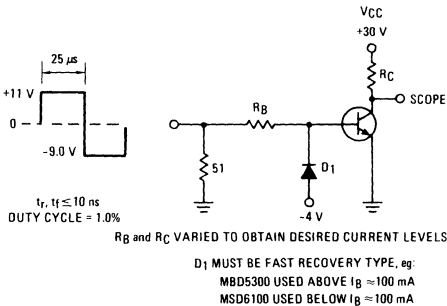


FIGURE 3 – TURN-ON TIME

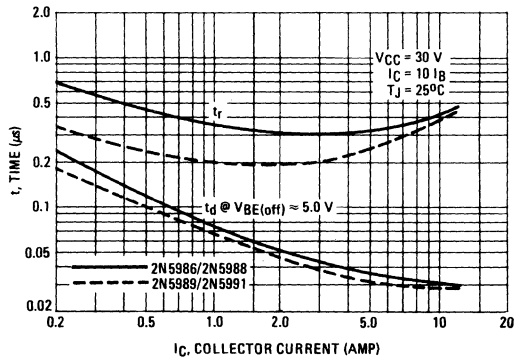


FIGURE 4 – THERMAL RESPONSE

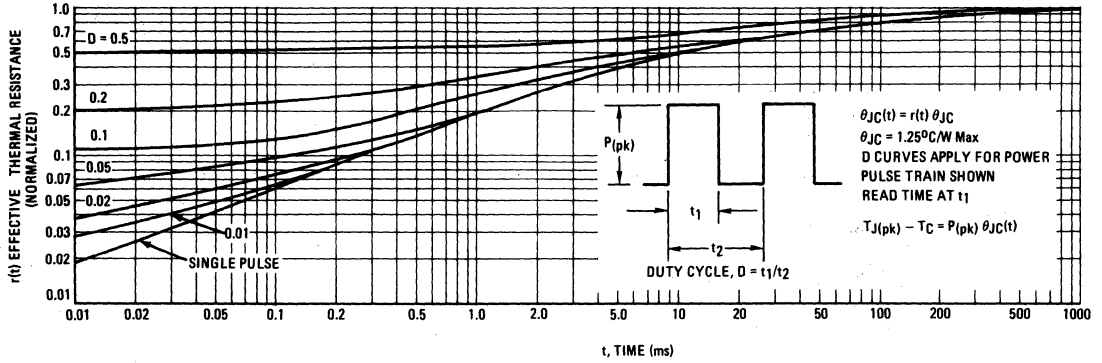
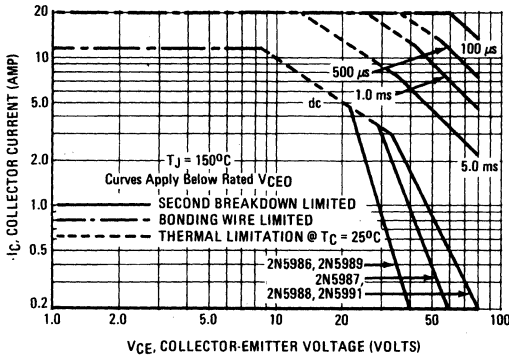


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

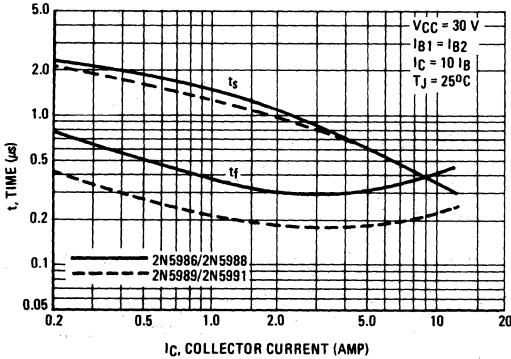
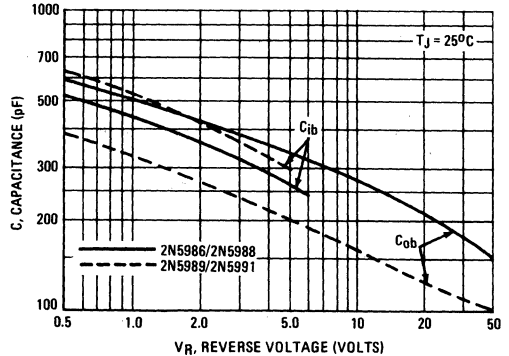


FIGURE 7 – CAPACITANCE



2N5986, 2N5987, 2N5988 PNP / 2N5989, 2N5991 NPN

PNP
2N5986 thru 2N5988

NPN
2N5989, 2N5991

FIGURE 8 - DC CURRENT GAIN

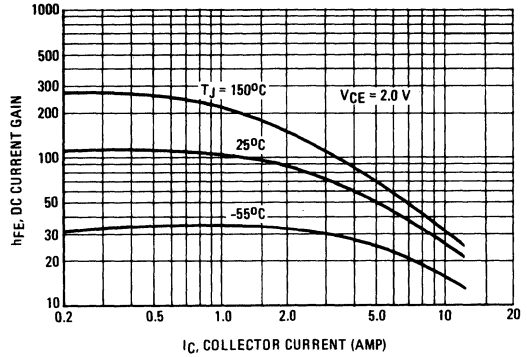
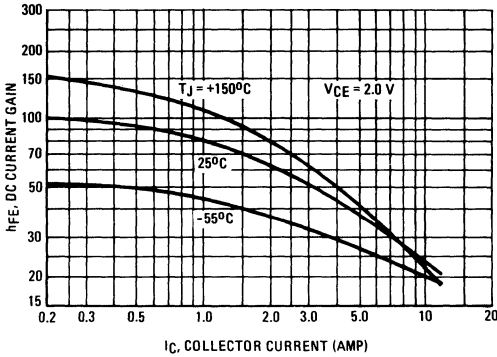


FIGURE 9 - COLLECTOR SATURATION REGION

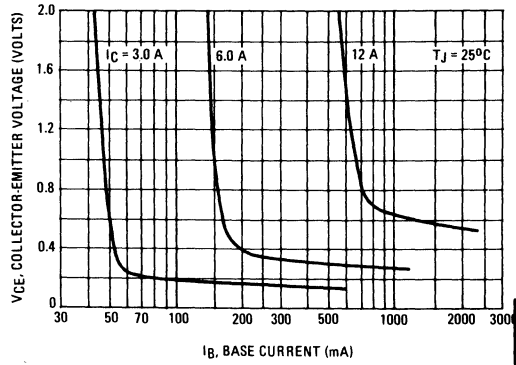
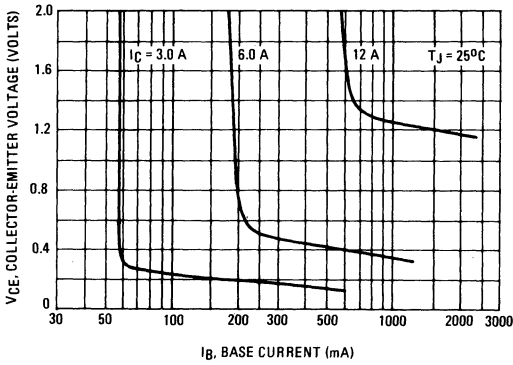
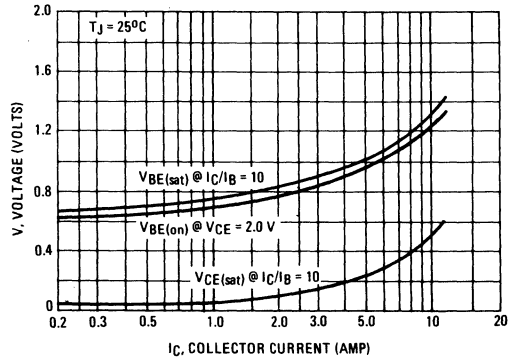
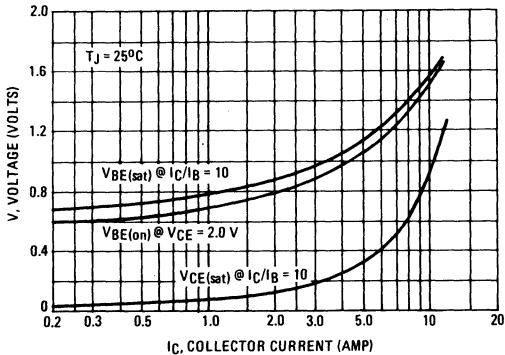


FIGURE 10 - "ON" VOLTAGES



PNP	NPN
2N6034	2N6037
2N6035	2N6038
2N6036	2N6039

PLASTIC DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

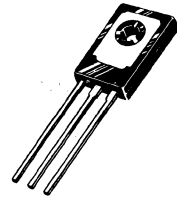
... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
h_{FE} = 2000 (Typ) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mAdc
V_{CEO(sus)} = 40 Vdc (Min) — 2N6034, 2N6037
= 60 Vdc (Min) — 2N6035, 2N6038
= 80 Vdc (Min) — 2N6036, 2N6039
- Forward Biased Second Breakdown Current Capability
I_{S/b} = 1.5 Adc @ 25 Vdc
- Monolithic Construction with Built-In Base-Emitter Resistors to Limit Leakage Multiplication
- Space-Saving High Performance-to-Cost Ratio
TO-225AA Plastic Package

DARLINGTON
4-AMPERE

COMPLEMENTARY SILICON
POWER TRANSISTORS

40, 60, 80 VOLTS
40 WATTS



***MAXIMUM RATINGS**

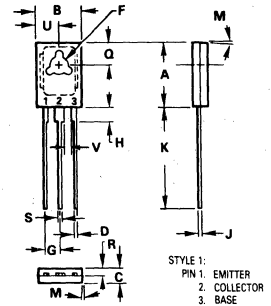
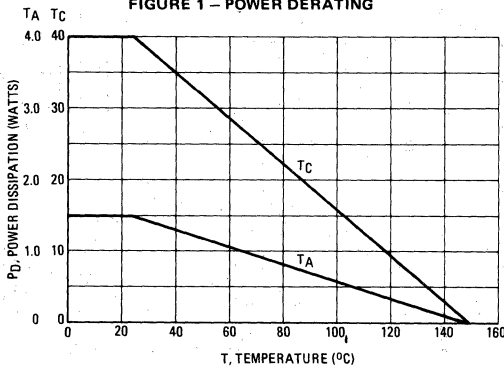
Rating	Symbol	2N6034 2N6037	2N6035 2N6038	2N6036 2N6039	Unit
Collector-Emitter Voltage	V _{CEO}	40	60	80	Vdc
Collector-Base Voltage	V _{CB}	40	60	80	Vdc
Emitter-Base Voltage	V _{EB}	5.0			Vdc
Collector Current — Continuous	I _C	4.0			Adc
Peak		8.0			
Base Current	I _B	100			mAdc
Total Power Dissipation @ T _C = 25°C	P _D	40			Watts
Derate above 25°C		0.32			W/°C
Total Power Dissipation @ T _A = 25°C	P _D	1.5			Watts
Derate above 25°C		0.012			W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ _{JC}	3.12	°C/W
Thermal Resistance, Junction to Ambient	θ _{JA}	83.3	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING



NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	2.50	2.74	0.095	0.105
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.35	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	° TYP		° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-225AA

2N6034, 2N6035, 2N6036 PNP 2N6037, 2N6038, 2N6039 NPN

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	40 60 80	— — —	Vdc
Collector-Cutoff Current (V _{CE} = 40 Vdc, I _B = 0) (V _{CE} = 60 Vdc, I _B = 0) (V _{CE} = 80 Vdc, I _B = 0)	I _{CEO}	— — —	100 100 100	μA
Collector Cutoff Current (V _{CE} = 40 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CE} = 60 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CE} = 80 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CE} = 40 Vdc, V _{BE(off)} = 1.5 Vdc T _C = 125°C) (V _{CE} = 60 Vdc, V _{BE(off)} = 1.5 Vdc T _C = 125°C) (V _{CE} = 80 Vdc, V _{BE(off)} = 1.5 Vdc T _C = 125°C)	I _{CEX}	— — — — — —	100 100 100 500 500 500	μA
Collector Cutoff Current (V _{CB} = 40 Vdc, I _E = 0) (V _{CB} = 60 Vdc, I _E = 0) (V _{CB} = 80 Vdc, I _E = 0)	I _{CBO}	— — —	0.5 0.5 0.5	mA
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	—	2.0	mA
ON CHARACTERISTICS				
DC Current Gain (I _C = 0.5 Adc, V _{CE} = 3.0 Vdc) (I _C = 2.0 Adc, V _{CE} = 3.0 Vdc) (I _C = 4.0 Adc, V _{CE} = 3.0 Vdc)	h _{FE}	500 750 100	— 15,000 —	—
Collector-Emitter Saturation Voltage (I _C = 2.0 Adc, I _B = 8.0 mA) (I _C = 4.0 Adc, I _B = 40 mA)	V _{CE(sat)}	— —	2.0 3.0	Vdc
Base-Emitter Saturation Voltage (I _C = 4.0 Adc, I _B = 40 mA)	V _{BE(sat)}	—	4.0	Vdc
Base-Emitter On Voltage (I _C = 2.0 Adc, V _{CE} = 3.0 Vdc)	V _{BE(on)}	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current-Gain (I _C = 0.75 Adc, V _{CE} = 10 Vdc, f = 1.0 MHz)	h _{fe}	25	—	—
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	— —	200 100	pF

*Indicates JEDEC Registered Data.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

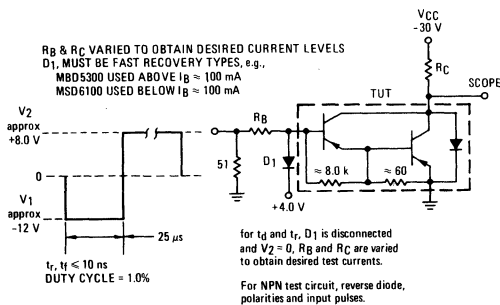
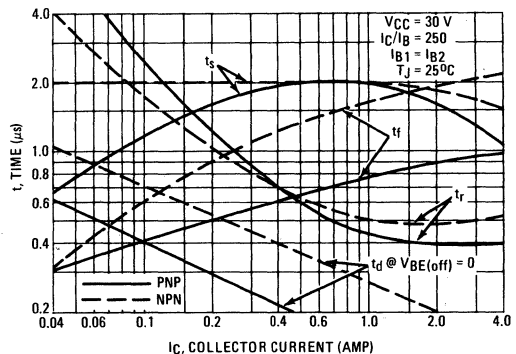
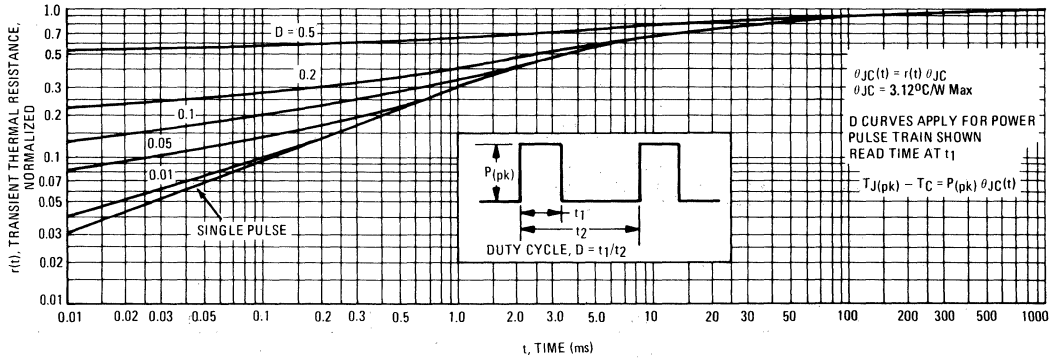


FIGURE 3 – SWITCHING TIMES



2N6034, 2N6035, 2N6036 PNP
2N6037, 2N6038, 2N6039 NPN

FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 5 – 2N6034, 2N6035, 2N6036

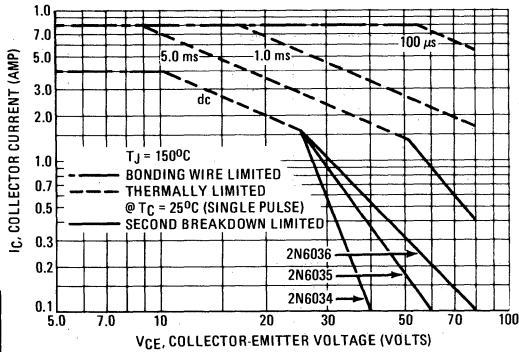
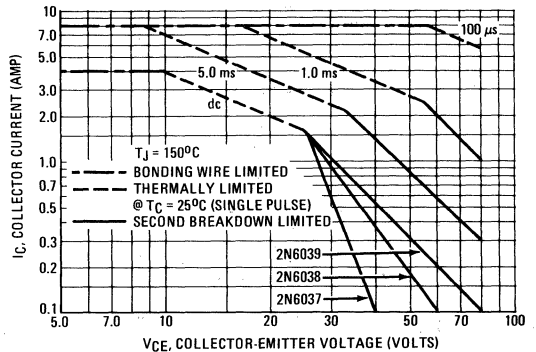


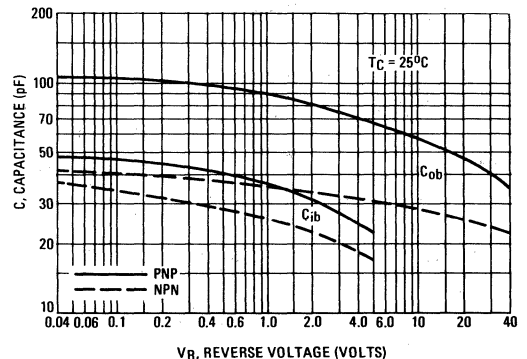
FIGURE 6 – 2N6037, 2N6038, 2N6039



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 – CAPACITANCE



3

2N6034, 2N6035, 2N6036 PNP
2N6037, 2N6038, 2N6039 NPN

PNP
2N6034, 2N6035, 2N6036

NPN
2N6037, 2N6038, 2N6039

FIGURE 8 - DC CURRENT GAIN

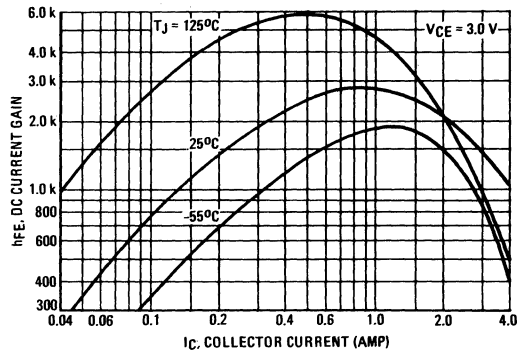
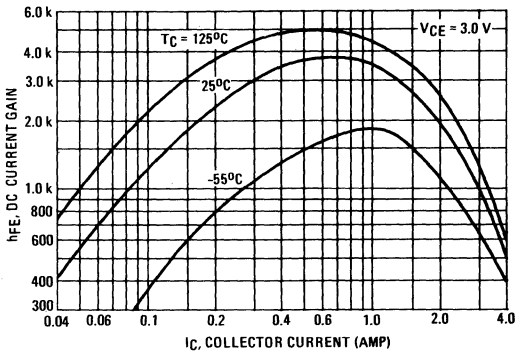


FIGURE 9 - COLLECTOR SATURATION REGION

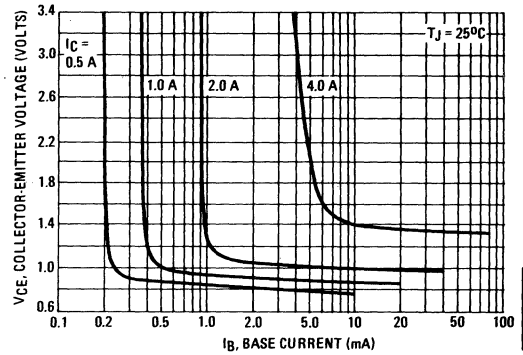
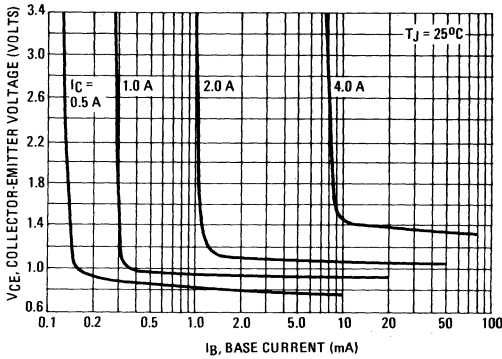
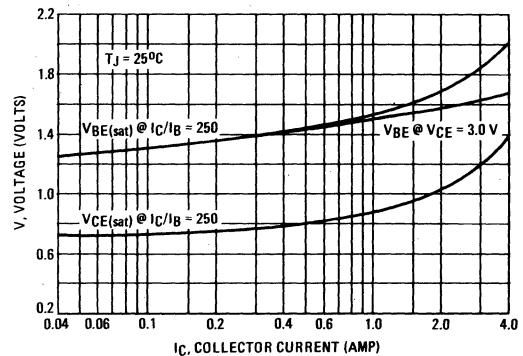
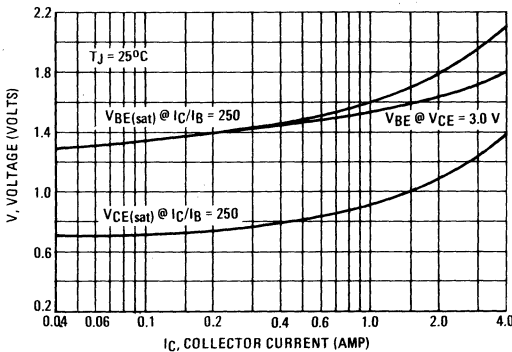


FIGURE 10 - "ON" VOLTAGES



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

2N6040 thru 2N6042 PNP
2N6043 thru 2N6045 NPN
MJE6040 thru MJE6041 PNP
MJE6043 thru MJE6045 NPN

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
 $h_{FE} = 2500$ (Typ) @ $I_C = 4.0$ Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc (1)
 $V_{CE(sus)} = 60$ Vdc (Min) – 2N6040, 2N6043
 $= 80$ Vdc (Min) – 2N6041, 2N6044
 $= 100$ Vdc (Min) – 2N6042, 2N6045
- Low Collector-Emitter Saturation Voltage – (1)
 $V_{CE(sat)} = 2.0$ Vdc (Max) @ $I_C = 4.0$ Adc – 2N6040, 41, 2N6043, 44
 $= 2.0$ Vdc (Max) @ $I_C = 3.0$ Adc – 2N6042, 2N6045
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

(1) Applies to corresponding in-house part numbers also.

*MAXIMUM RATINGS

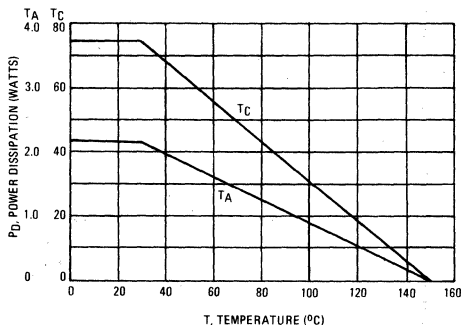
Rating	Symbol	2N6040 2N6043 MJE6040	2N6041 2N6044 MJE6041	2N6042 2N6045 MJE6045	Unit
Collector-Emitter Voltage	V_{CE0}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous	I_C	← 8.0 →			Adc
Peak		← 16 →			
Base Current	I_B	← 120 →			mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	← 75 →			Watts
Derate above 25°C		← 0.60 →			W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	← 2.2 →			Watts
Derate above 25°C		← 0.0175 →			W/ $^\circ\text{C}$
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	← -65 to +150 →			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	57	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data

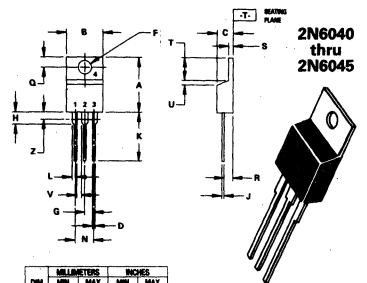
FIGURE 1 – POWER DERATING



DARLINGTON 8 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80-100 VOLTS
75 WATTS



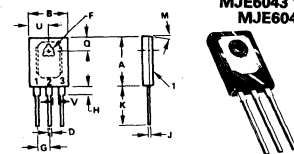
DIM	MILLIMETERS	MIN	MAX	INCHES	MIN	MAX
A	14.40	15.75	0.571	0.620		
B	6.86	10.29	0.269	0.405		
C	4.97	4.82	0.199	0.190		
D	0.94	0.98	0.035	0.035		
F	3.81	3.73	0.142	0.147		
G	2.42	2.86	0.095	0.115		
H	2.00	3.51	0.110	0.135		
J	0.46	0.71	0.018	0.028		
E	15.70	14.27	0.580	0.567		
L	1.15	1.28	0.045	0.050		
M	4.80	5.33	0.190	0.210		
N	2.54	3.08	0.100	0.120		
R	2.04	2.73	0.080	0.110		
S	1.15	1.28	0.045	0.050		
T	1.07	1.07	0.228	0.228		
U	0.50	1.27	0.020	0.050		
V	1.15	—	0.045	—		
Z	—	2.54	—	0.100		

STYLE 1:
 PIN 1 BASE
 2 COLLECTOR
 3 EMITTER
 4 COLLECTOR

NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1987
 2. CONTROLLING DIMENSION: INCH
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD PROJECTIONS ARE ALLOWED

**CASE 221A-04
TO-220AB**

MJE6040, MJE6041 and MJE6043 thru MJE6045



DIM	MILLIMETERS	MIN	MAX	INCHES	MIN	MAX
A	15.13	16.36	0.630	0.645		
B	15.23	12.83	0.600	0.505		
C	3.18	3.43	0.125	0.135		
D	1.69	1.24	0.066	0.049		
F	3.51	3.76	0.138	0.148		
G	4.22	8.50	0.168	0.333		
H	2.67	2.92	0.105	0.115		
J	0.813	0.864	0.032	0.034		
K	15.11	16.38	0.595	0.645		
M	—	2.54	—	0.100		
N	—	2.54	—	0.100		
O	4.70	4.95	0.185	0.195		
R	1.91	2.16	0.075	0.085		
U	2.22	2.48	0.245	0.255		
V	2.03	—	0.080	—		

STYLE 2:
 PIN 1 EMITTER
 2 COLLECTOR
 3 BASE

NOTES:
 1. DIM "D" UNCONTROLLED IN ZONE "H"
 2. DIM "F" DIA THRU
 3. HEAT SINK CONTACT AREA (BOTTOM)
 4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TOP) AT MAXIMUM MATERIAL CONDITION

**CASE 90-05
TO-225AB**

2N6040 thru 2N6042 PNP
2N6043 thru 2N6045 NPN
MJE6040 thru MJE6041 PNP
MJE6043 thru MJE6045 NPN

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ($I_C = 100 \text{ mA dc}$, $I_B = 0$)	$V_{CE(sus)}$	60 80 100	—	Vdc
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 80 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 100 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	— — —	20 20 20	μA
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 100 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 100 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	— — — — —	20 20 20 200 200	μA
Collector Cutoff Current ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	— — —	20 20 20	μA
Emitter Cutoff Current ($V_{GE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 8.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) All Types	h_{FE}	1000 1000 100	20,000 20,000 —	—
Collector-Emitter Saturation Voltage ($I_C = 4.0 \text{ Adc}$, $I_B = 16 \text{ mAdc}$) ($I_C = 3.0 \text{ Adc}$, $I_B = 12 \text{ mAdc}$) ($I_C = 8.0 \text{ Adc}$, $I_B = 80 \text{ mAdc}$) All Types	$V_{CE(sat)}$	— — —	2.0 2.0 4.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 8.0 \text{ Adc}$, $I_B = 80 \text{ mAdc}$)	$V_{BE(sat)}$	—	4.5	Vdc
Base-Emitter On Voltage ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	$ h_{fe} $	4.0	—	—
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	—	300 200	pF
Small-Signal Current Gain ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	300	—	—

*Indicates JEDEC Registered Data.

3

FIGURE 2 - SWITCHING TIMES TEST CIRCUIT

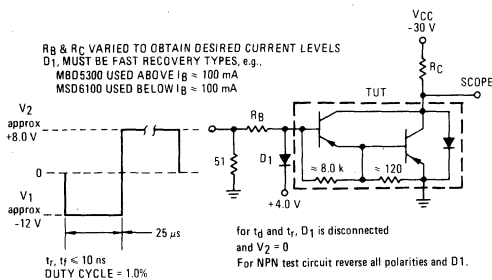
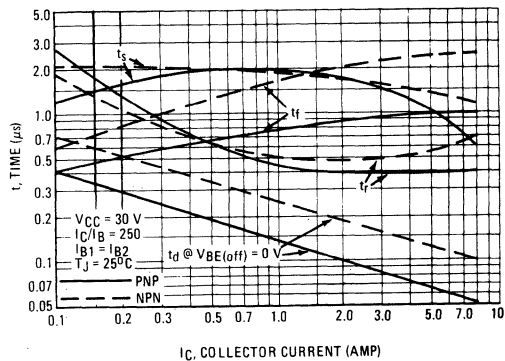


FIGURE 3 - SWITCHING TIMES



2N6040 thru 2N6042 PNP
2N6043 thru 2N6045 NPN
MJE6040 thru MJE6041 PNP
MJE6043 thru MJE6045 NPN

FIGURE 4 - THERMAL RESPONSE

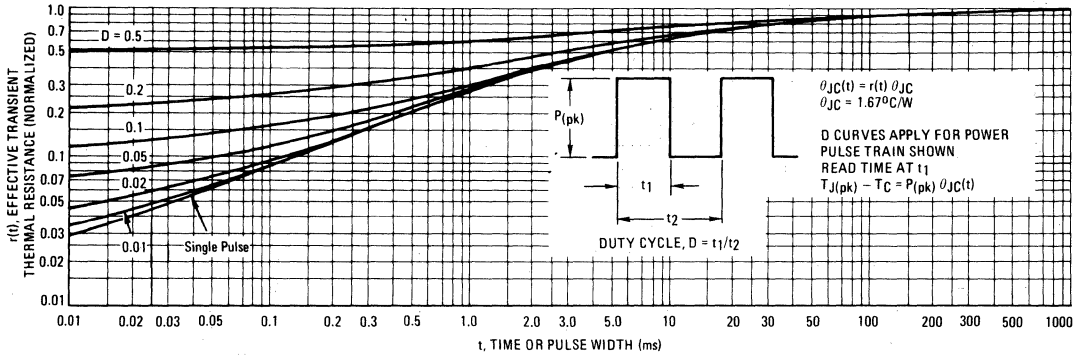
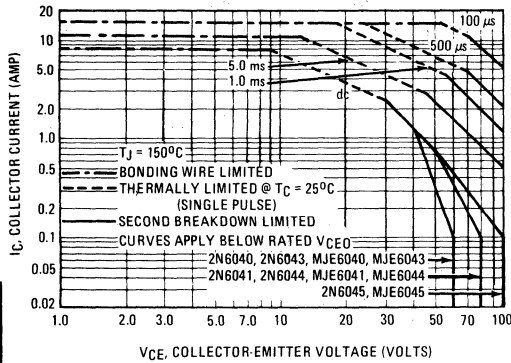


FIGURE 5 - ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 - SMALL-SIGNAL CURRENT GAIN

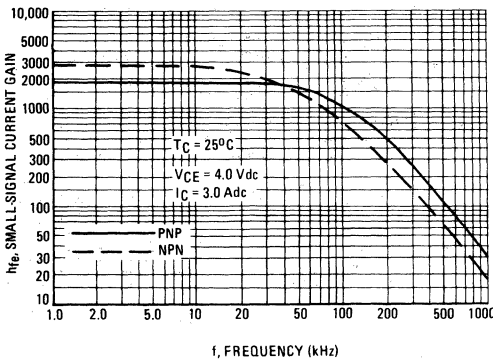
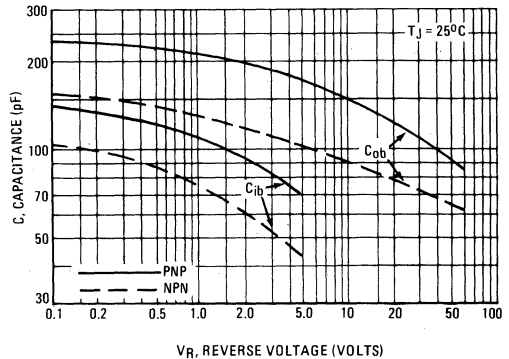


FIGURE 7 - CAPACITANCE



3

2N6040 thru 2N6042 PNP
2N6043 thru 2N6045 NPN
MJE6040 thru MJE6041 PNP
MJE6043 thru MJE6045 NPN

PNP
2N6040, 2N6041, 2N6042
MJE6040, MJE6041

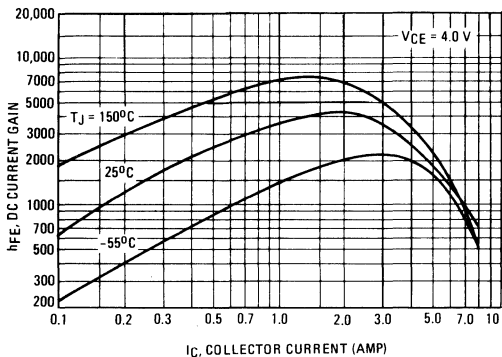


FIGURE 8 - DC CURRENT GAIN

NPN
2N6043, 2N6044, 2N6045
MJE6043, MJE6044, MJE6045

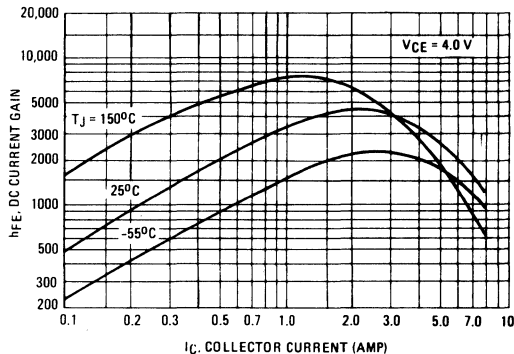


FIGURE 9 - COLLECTOR SATURATION REGION

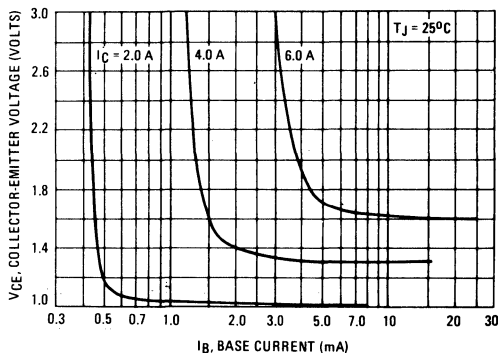
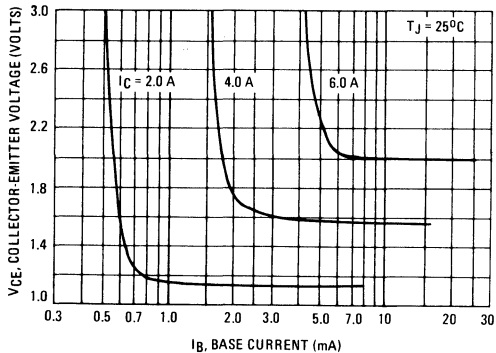
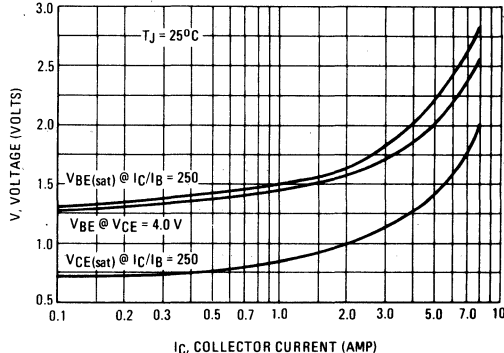
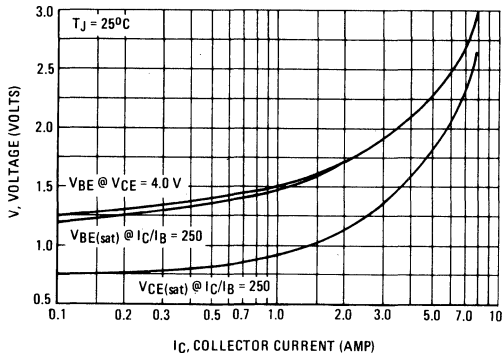


FIGURE 10 - "ON" VOLTAGES



MEDIUM-POWER PNP SILICON TRANSISTOR

... designed for general-purpose switching and amplifier applications

- Excellent Safe Operating Area
- DC Current Gain Specified to 4.0 Amperes
- Complement to NPN Type 2N3054A

4 AMPERE
POWER TRANSISTOR
PNP SILICON
55 VOLTS
75 WATTS

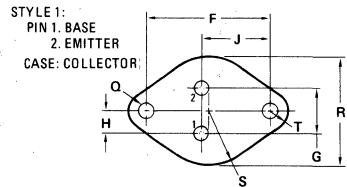
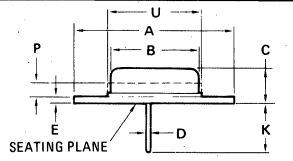
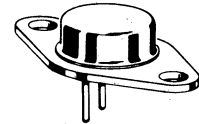
***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	55	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	60	Vdc
Collector-Base Voltage	V_{CB}	90	Vdc
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current - Continuous	I_C	4.0	Adc
Peak		10	
Base Current	I_B	2.0	Adc
Total Device Dissipation @ $T_C = 25^\circ C$	P_D	75	Watts
Derate above 25°		0.43	W/ $^\circ C$
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ C$

*Indicates JEDEC Registered Data

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.33	$^\circ C/W$

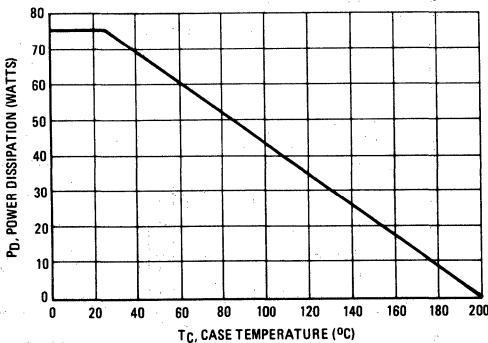


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	-	0.360	-
P	-	1.27	-	0.050
Q	3.61	3.86	0.142	0.152
S	-	8.89	-	0.350
T	-	3.68	-	0.145
U	-	15.75	-	0.620

All JEDEC Dimensions and Notes Apply.

CASE 80-02
TO-213AA

FIGURE 1 - POWER-TEMPERATURE DERATING



*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 100 \text{ mAdc}, I_B = 0$)	$V_{CEO(sus)}$	55	—	Vdc
Collector-Emitter Sustaining Voltage (1) ($I_C = 100 \text{ mAdc}, R_{BE} = 100 \Omega$)	$V_{CER(sus)}$	60	—	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}, I_B = 0$)	I_{CEO}	—	500	μAdc
Collector Cutoff Current ($V_{CE} = 90 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 90 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)	I_{CEX}	—	1.0 6.0	mAdc
Emitter Cutoff Current ($V_{BE} = 7.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	1.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 500 \text{ mAdc}, V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 3.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	25 6.0	100	—
Collector-Emitter Saturation Voltage ($I_C = 500 \text{ mAdc}, I_B = 50 \text{ mAdc}$) ($I_C = 4.0 \text{ Adc}, I_B = 800 \text{ mAdc}$)	$V_{CE(sat)}$	—	0.5 2.0	Vdc
Base-Emitter On Voltage ($I_C = 500 \text{ mAdc}, V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($I_C = 200 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$)	f_T	3.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz}$)	C_{ob}	—	200	pF
Small-Signal Current Gain ($I_C = 100 \text{ mAdc}, V_{CE} = 4.0 \text{ Vdc}, f = 1.0 \text{ kHz}$)	h_{fe}	25	180	

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$

FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUIT

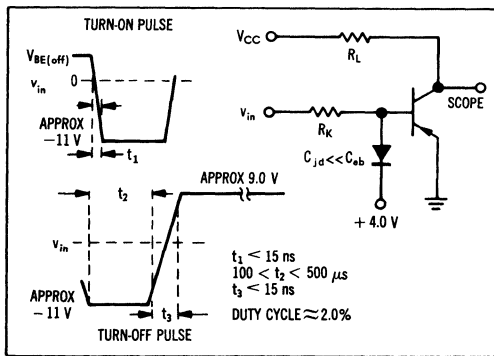


FIGURE 3 – TURN-ON TIME

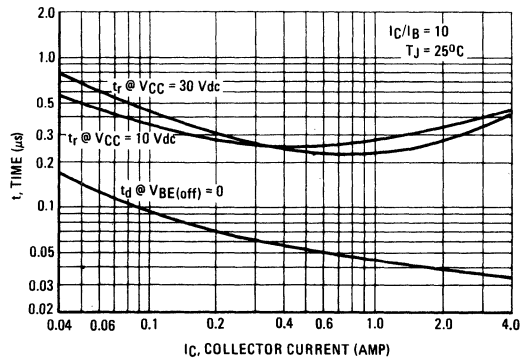


FIGURE 4 - THERMAL RESPONSE

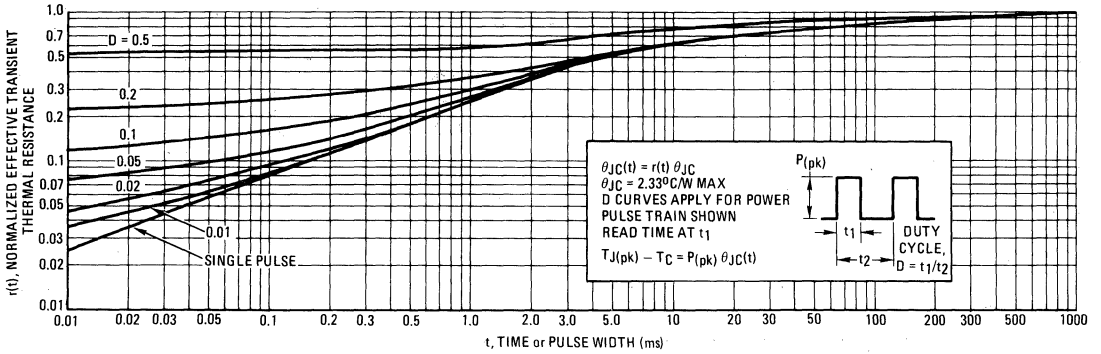
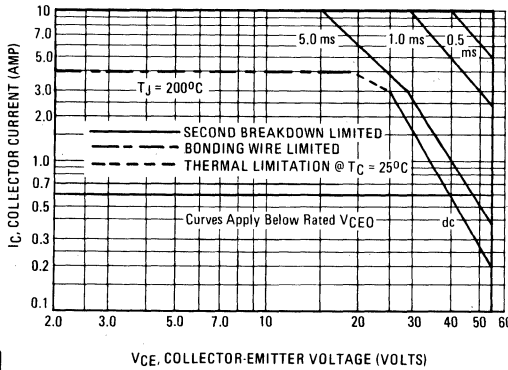


FIGURE 5 - ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 - TURN-OFF TIME

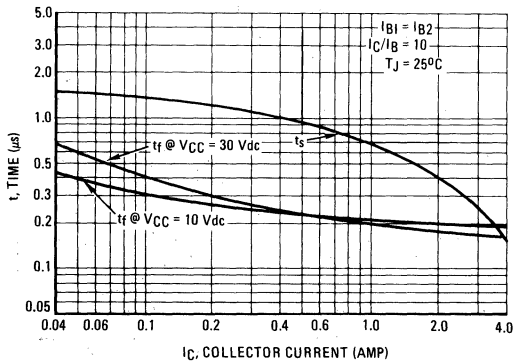
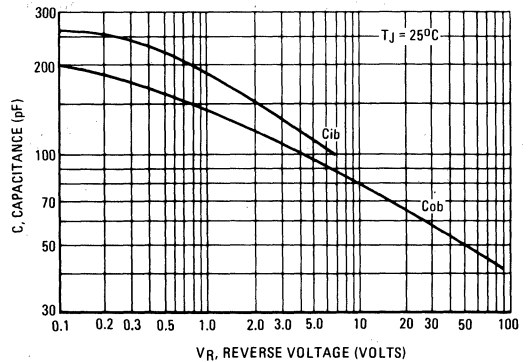


FIGURE 7 - CAPACITANCE



PNP
2N6050 thru 2N6052
NPN
2N6057 thru 2N6059

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain –
 $h_{FE} = 3500$ (Typ) @ $I_C = 5.0$ Adc
- Collector-Emitter Sustaining Voltage – @ 100 mA
 $V_{CE(sus)} = 60$ Vdc (Min) – 2N6050, 2N6057
 80 Vdc (Min) – 2N6051, 2N6058
 100 Vdc (Min) – 2N6052, 2N6059
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON
12 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60-80-100 VOLTS
150 WATTS

***MAXIMUM RATINGS**

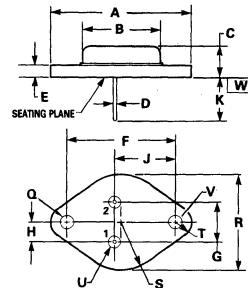
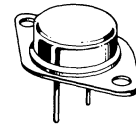
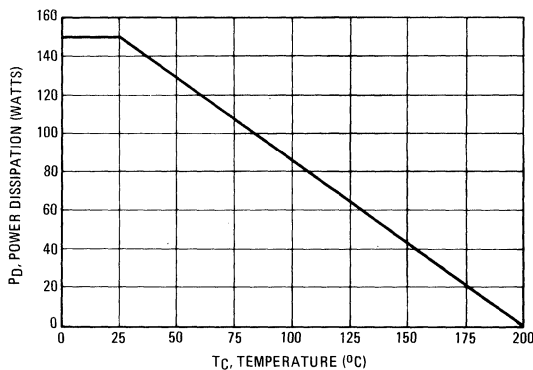
Rating	Symbol	2N6050 2N6057	2N6051 2N6058	2N6052 2N6059	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 12 → ← 20 →			Adc
Base Current	I_B	← 0.2 →			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 150 →			Watts
		← 0.857 →			W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to $+200^\circ\text{C}$ →			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Rating	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	$^\circ\text{C}/\text{W}$

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING



STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA

NOTES:
 1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

2N6050 thru 2N6052 PNP/2N6057 thru 2N6059 NPN

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	60 80 100	— — —	V _{dc}
Collector Cutoff Current (V _{CE} = 30 V _{dc} , I _B = 0) (V _{CE} = 40 V _{dc} , I _B = 0) (V _{CE} = 50 V _{dc} , I _B = 0)	I _{CEO}	— — —	1.0 1.0 1.0	mA _{dc}
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , V _{BE(off)} = 1.5 V _{dc}) (V _{CE} = Rated V _{CEO} , V _{BE(off)} = 1.5 V _{dc} , T _C = 150°C)	I _{CEX}	—	0.5 5.0	mA _{dc}
Emitter Cutoff Current (V _{BE} = 5.0 V _{dc} , I _C = 0)	I _{EBO}	—	2.0	mA _{dc}

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 6.0 A _{dc} , V _{CE} = 3.0 V _{dc}) (I _C = 12 A _{dc} , V _{CE} = 3.0 V _{dc})	h _{FE}	750 100	18,000 —	—
Collector-Emitter Saturation Voltage (I _C = 6.0 A _{dc} , I _B = 24 mA _{dc}) (I _C = 12 A _{dc} , I _B = 120 mA _{dc})	V _{CE(sat)}	—	2.0 3.0	V _{dc}
Base-Emitter Saturation Voltage (I _C = 12 A _{dc} , I _B = 120 mA _{dc})	V _{BE(sat)}	—	4.0	V _{dc}
Base-Emitter On Voltage (I _C = 6.0 A _{dc} , V _{CE} = 3.0 V _{dc})	V _{BE(on)}	—	2.8	V _{dc}

DYNAMIC CHARACTERISTICS

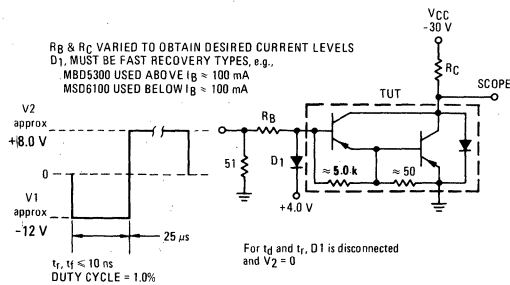
Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio (I _C = 5.0 A _{dc} , V _{CE} = 3.0 V _{dc} , f = 1.0 MHz)	h _{fe}	4.0	—	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 0.1 MHz)	C _{ob}	—	500 300	pF
Small-Signal Current Gain (I _C = 5.0 A _{dc} , V _{CE} = 3.0 V _{dc} , f = 1.0 kHz)	h _{fe}	300	—	—

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

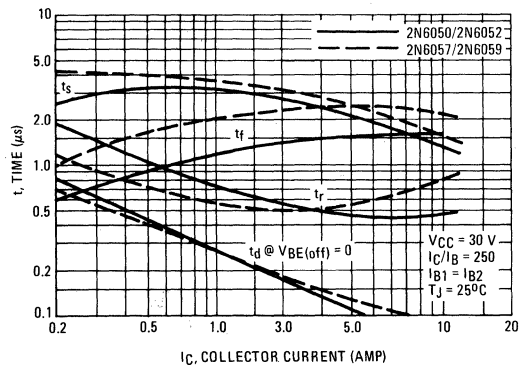
3

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



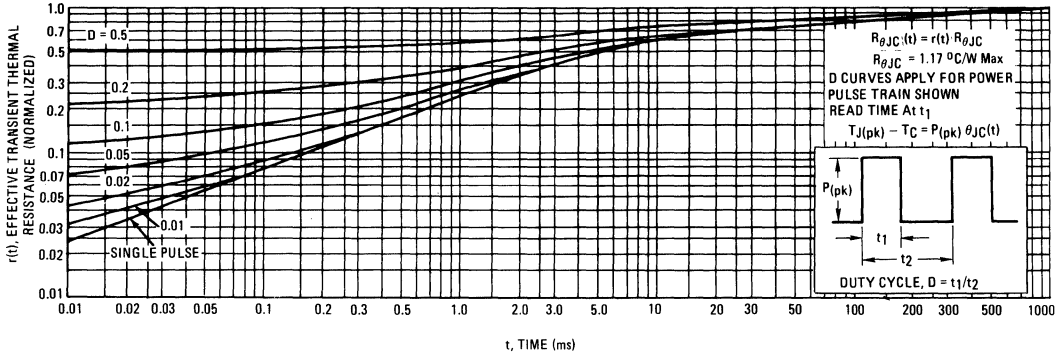
For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 – SWITCHING TIMES



2N6050 thru 2N6052 PNP/2N6057 thru 2N6059 NPN

FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6050, 2N6057

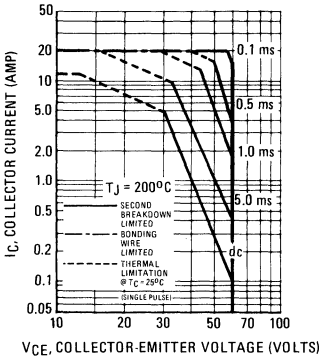


FIGURE 6 – 2N6051, 2N6058

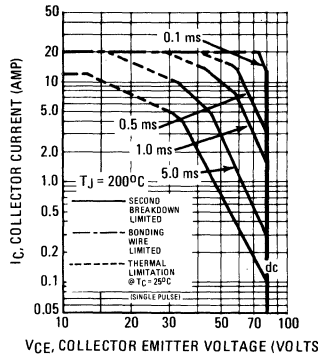
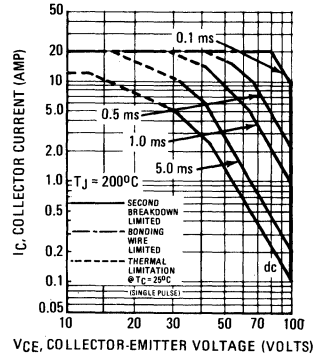


FIGURE 7 – 2N6052, 2N6059



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6 and 7 is based on $T_{J(pk)} = 200^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 – SMALL-SIGNAL CURRENT GAIN

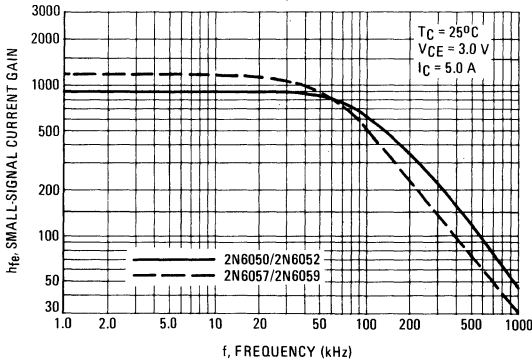
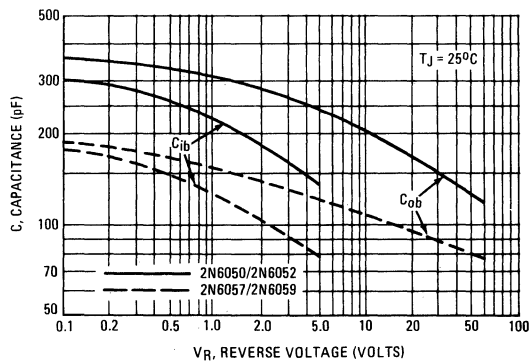


FIGURE 9 – CAPACITANCE



2N6050 thru 2N6052 PNP/2N6057 thru 2N6059 NPN

PNP
2N6050, 2N6051, 2N6052

NPN
2N6057, 2N6058, 2N6059

FIGURE 10 – DC CURRENT GAIN

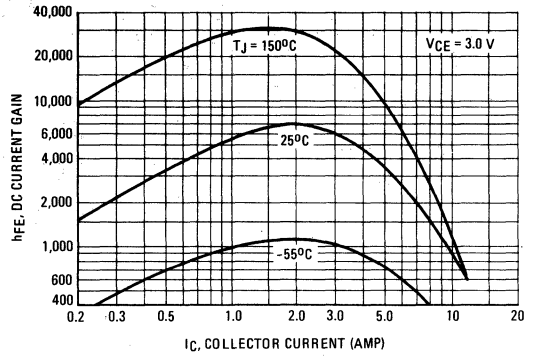
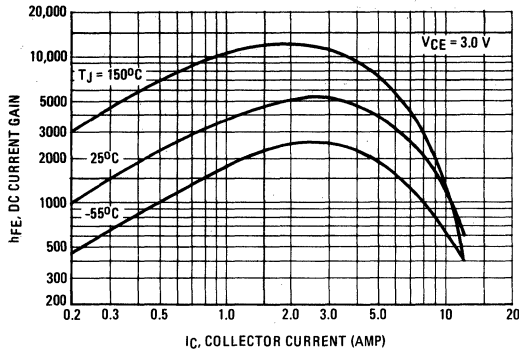


FIGURE 11 – COLLECTOR SATURATION REGION

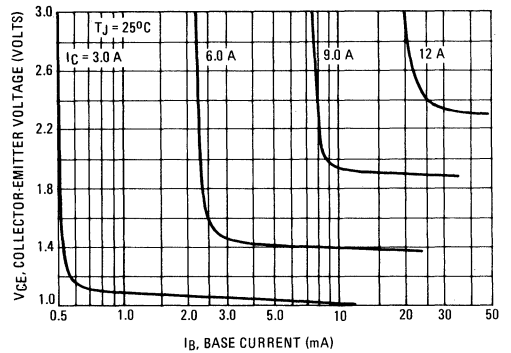
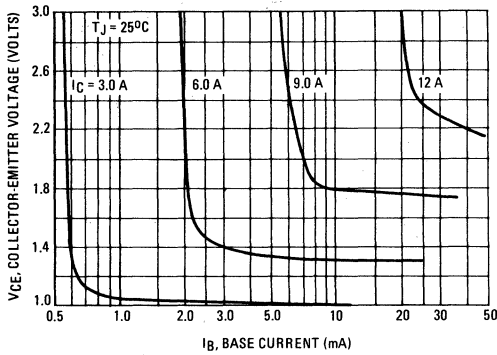
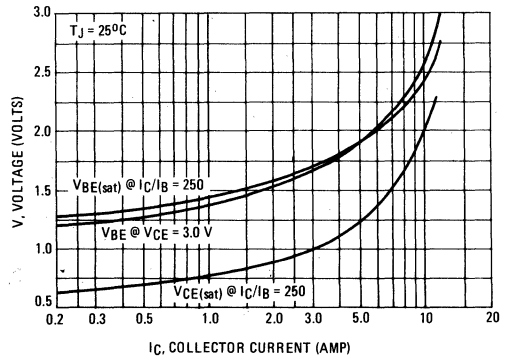
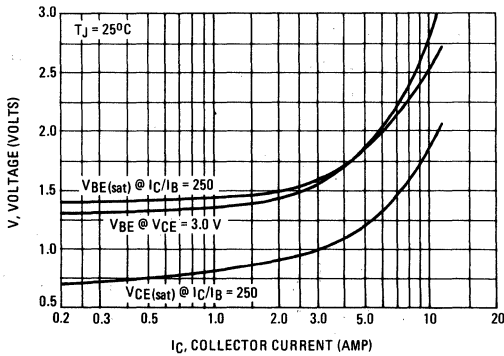


FIGURE 12 – "ON" VOLTAGES



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

2N6053, 2N6054 2N6298, 2N6299 PNP 2N6055, 2N6056 2N6300, 2N6301 NPN

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain –
 $h_{FE} = 3000$ (Typ) @ $I_C = 4.0$ Adc
- Collector-Emitter Sustaining Voltage – @ 100 mA
 $V_{CE(sus)} = 60$ Vdc (Min) – 2N6053, 2N6055, 2N6298, 2N6300
 $= 80$ Vdc (Min) – 2N6054, 2N6056, 2N6299, 2N6301
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 2.0$ Vdc (Max) @ $I_C = 4.0$ Adc
 $= 3.0$ Vdc (Max) @ $I_C = 8.0$ Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
75,100 WATTS

*MAXIMUM RATINGS

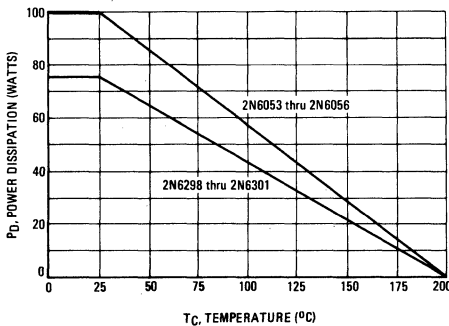
Rating	Symbol	2N6053 2N6055 2N6298 2N6300	2N6054 2N6056 2N6299 2N6301	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	8.0		Adc
Base Current	I_B	16		Adc
		2N6053 2N6054 2N6055 2N6056	2N6298 2N6299 2N6300 2N6301	
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	100 0.571	75 0.428	Watts $\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N6053 2N6054 2N6055 2N6056	2N6298 2N6299 2N6300 2N6301	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	2.33	$^\circ\text{C}/\text{W}$

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING

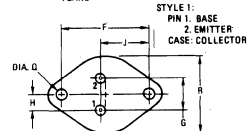
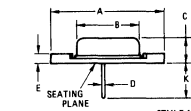


DARLINGTON 8 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
75,100 WATTS

2N6053
2N6054
2N6055
2N6056



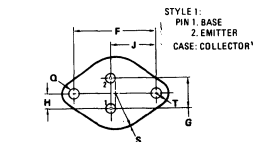
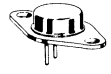
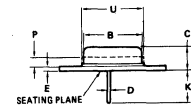
NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS			INCHES		
	MIN	MAX	TYP	MIN	MAX	TYP
A	-	38.37	-	1.550	-	-
B	-	21.08	-	0.830	-	-
C	6.35	7.62	0.250	0.250	0.300	-
D	0.95	1.05	0.635	0.045	-	-
E	-	3.43	-	0.135	-	-
F	29.90	30.40	1.177	1.197	-	-
G	10.61	11.15	0.420	0.440	-	-
H	5.33	5.59	0.210	0.220	-	-
J	18.84	17.15	0.855	0.675	-	-
K	11.18	12.15	0.440	0.480	-	-
L	3.84	4.08	0.151	0.161	-	-
R	-	28.67	-	1.050	-	-

Collector connected to case.

CASE 11-01
TO-204AA

2N6298
2N6299
2N6300
2N6301



DIM	MILLIMETERS			INCHES		
	MIN	MAX	TYP	MIN	MAX	TYP
B	11.94	12.70	0.470	0.500	-	-
C	5.35	6.84	0.250	0.240	-	-
D	0.71	0.86	0.028	0.034	-	-
E	1.27	1.31	0.050	0.075	-	-
F	24.33	24.43	0.959	0.962	-	-
G	6.83	5.33	0.190	0.210	-	-
H	2.41	2.97	0.095	0.105	-	-
J	14.48	14.99	0.570	0.590	-	-
K	9.14	-	0.360	-	-	-
L	-	1.27	-	0.050	-	-
M	3.81	3.88	0.142	0.152	-	-
N	-	8.89	-	0.350	-	-
O	-	3.58	-	0.145	-	-
U	-	15.75	-	0.620	-	-

All JEDEC Dimensions and Notes Apply.

CASE 80-02
TO-213AA

2N6053, 2N6054, 2N6298, 2N6299 PNP, 2N6055, 2N6056, 2N6300, 2N6301 NPN

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 100 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	60 80	— —	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	— —	0.5 0.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	— —	0.5 5.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	2.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 8.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	h_{FE}	750 100	18000 —	—
Collector-Emitter Saturation Voltage ($I_C = 4.0 \text{ Adc}$, $I_B = 16 \text{ mAdc}$) ($I_C = 8.0 \text{ Adc}$, $I_B = 80 \text{ mAdc}$)	$V_{CE(sat)}$	— —	2.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 8.0 \text{ Adc}$, $I_B = 80 \text{ mAdc}$)	$V_{BE(sat)}$	—	4.0	Vdc
Base-Emitter On Voltage ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	$V_{BE(on)}$	—	2.8	Vdc

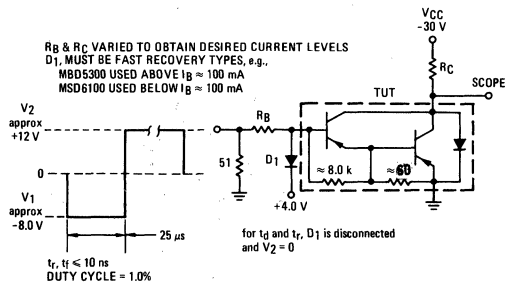
DYNAMIC CHARACTERISTICS

Magnitude of Common Emitter Small-Signal Short Circuit Current Transfer Ratio ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	$ h_{fe} $	4.0	—	—
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	— —	300 200	pF
Small-Signal Current Gain ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	300	—	—

*Indicates JEDEC Registered Data.

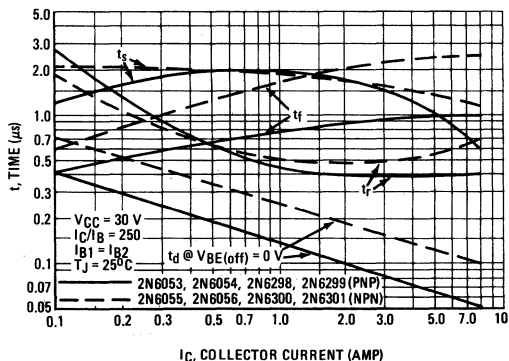
(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2.0 %.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



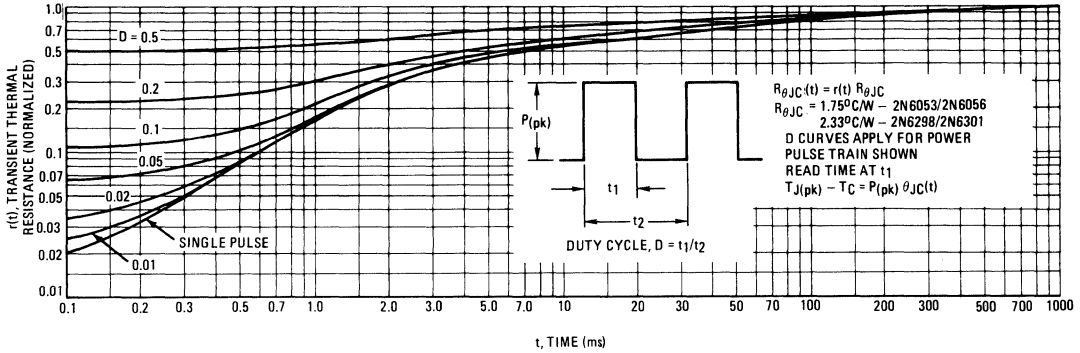
For NPN test circuit reverse diode, polarities and input pulses.

FIGURE 3 – SWITCHING TIMES



**2N6053, 2N6054, 2N6298, 2N6299 PNP,
2N6055, 2N6056, 2N6300, 2N6301 NPN**

FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6053 thru 2N6056

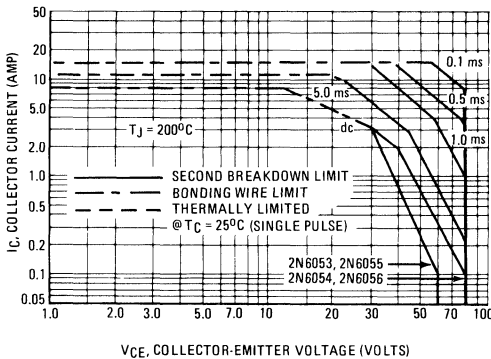
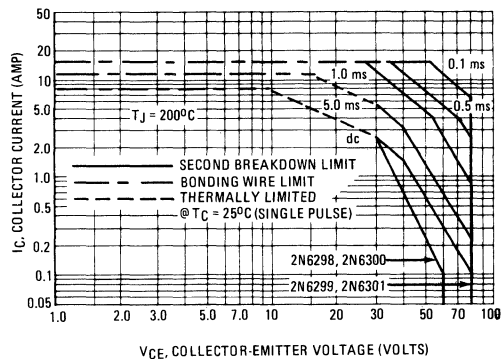


FIGURE 6 – 2N6298 thru 2N6301



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figures 5 and 6 is based on $T_{J(pk)} = 200^{\circ}\text{C}$; T_C is

variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



FIGURE 7 – SMALL-SIGNAL CURRENT GAIN

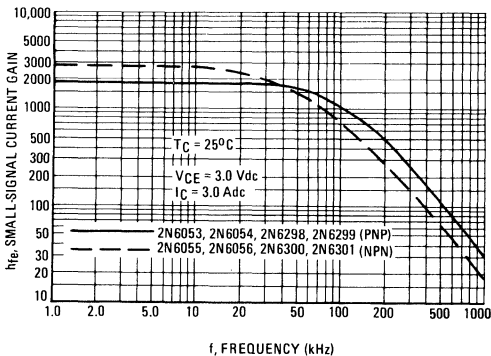
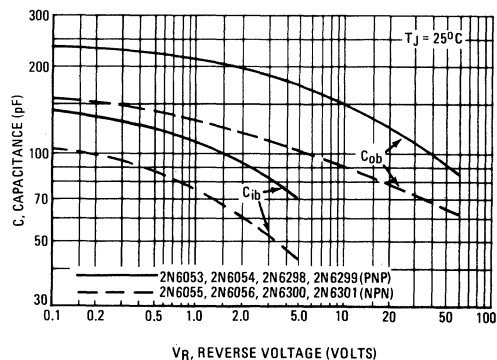


FIGURE 8 – CAPACITANCE



**2N6053, 2N6054, 2N6298, 2N6299 PNP,
2N6055, 2N6056, 2N6300, 2N6301 NPN**

PNP

2N6053, 2N6054, 2N6298, 2N6299

NPN

2N6055, 2N6056, 2N6300, 2N6301

FIGURE 9 – DC CURRENT GAIN

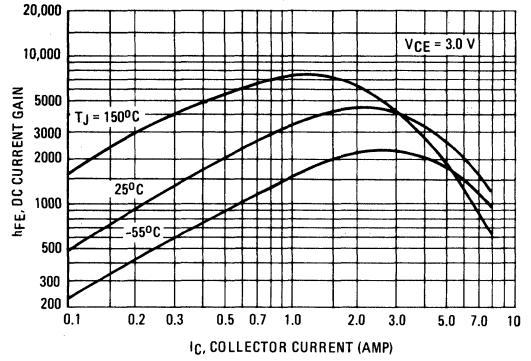
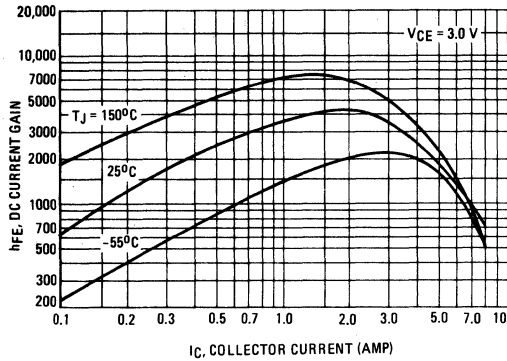


FIGURE 10 – COLLECTOR SATURATION REGION

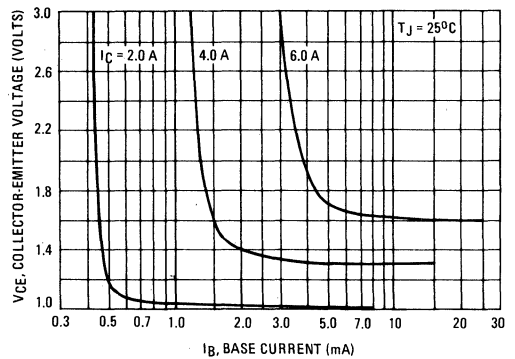
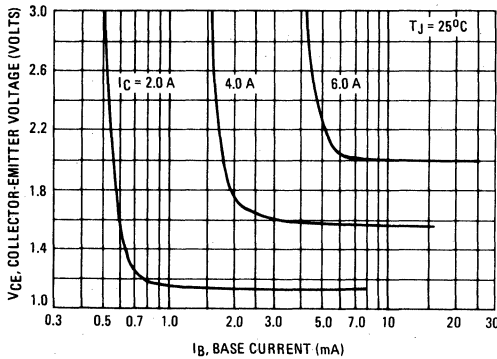
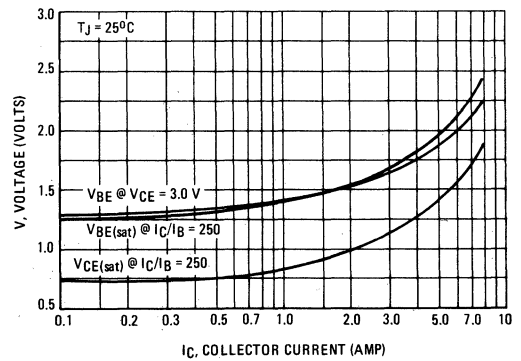
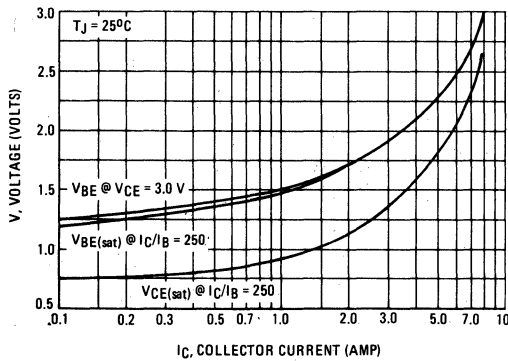


FIGURE 11 – "ON" VOLTAGES



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

2N6057 thru 2N6059
See Page 3-153

PNP
2N6107, 2N6109
2N6111
NPN
2N6288, 2N6292

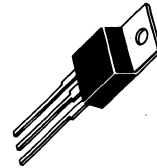
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

... designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 7.0 Amperes
 $h_{FE} = 30-150 @ I_C = 3.0 \text{ Adc} - 2N6111, 2N6288$
 $= 2.3 (\text{Min}) @ I_C = 7.0 \text{ Adc} - \text{All Devices}$
- Collector-Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 30 \text{ Vdc (Min)} - 2N6111, 2N6288$
 $= 50 \text{ Vdc (Min)} - 2N6109$
 $= 70 \text{ Vdc (Min)} - 2N6107, 2N6292$
- High Current Gain – Bandwidth Product
 $f_T = 4.0 \text{ MHz (Min)} @ I_C = 500 \text{ mAdc} - 2N6288, 90, 92$
 $= 10 \text{ MHz (Min)} @ I_C = 500 \text{ mAdc} - 2N6107, 09, 11$
- TO-220AB Compact Package
- TO-213AA Leadform Also Available

7 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

30-50-70 VOLTS
40 WATTS



*MAXIMUM RATINGS

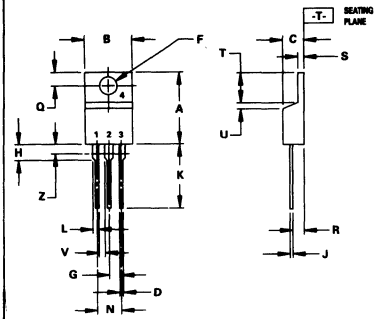
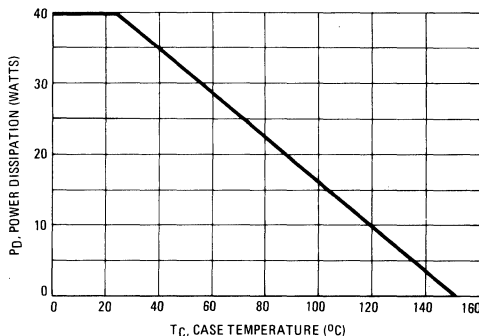
Rating	Symbol	2N6111 2N6288	2N6109	2N6107 2N6292	Unit
Collector-Emitter Voltage	V_{CEO}	30	50	70	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	7.0 10			Adc
Base Current	I_B	3.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40 0.32			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.42	15.75	0.570	0.620
B	9.65	10.20	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.90	3.30	0.110	0.130
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.30	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.70	0.080	0.110
S	1.15	1.30	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:

1. PIN 1: BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

2N6107, 2N6109, 2N6111 PNP, 2N6288, 2N6292 NPN

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

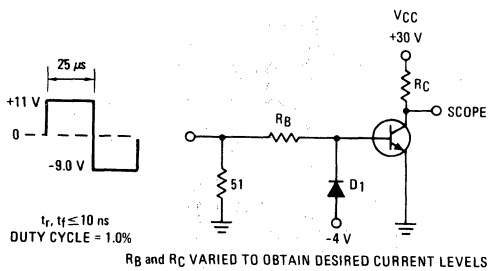
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 100 mA _{dc} , I _B = 0)	V _{CEO(sus)}	30 50 70	— — —	V _{dc}
Collector Cutoff Current (V _{CE} = 20 V _{dc} , I _B = 0) (V _{CE} = 40 V _{dc} , I _B = 0) (V _{CE} = 60 V _{dc} , I _B = 0)	I _{CEO}	— — —	1.0 1.0 1.0	mA _{dc}
Collector Cutoff Current (V _{CE} = 40 V _{dc} , V _{EB(off)} = 1.5 V _{dc}) (V _{CE} = 60 V _{dc} , V _{EB(off)} = 1.5 V _{dc}) (V _{CE} = 80 V _{dc} , V _{EB(off)} = 1.5 V _{dc}) (V _{CE} = 30 V _{dc} , V _{EB(off)} = 1.5 V _{dc} , T _C = 150°C) (V _{CE} = 50 V _{dc} , V _{EB(off)} = 1.5 V _{dc} , T _C = 150°C) (V _{CE} = 70 V _{dc} , V _{EB(off)} = 1.5 V _{dc} , T _C = 150°C)	I _{CEX}	— — — — — —	100 100 100 2.0 2.0 2.0	μA _{dc} mA _{dc}
Emitter Cutoff Current (V _{BE} = 5.0 V _{dc} , I _C = 0)	I _{EBO}	—	1.0	mA _{dc}
ON CHARACTERISTICS (1)				
DC Current Gain (I _C = 2.0 A _{dc} , V _{CE} = 4.0 V _{dc}) (I _C = 2.5 A _{dc} , V _{CE} = 4.0 V _{dc}) (I _C = 3.0 A _{dc} , V _{CE} = 4.0 V _{dc}) (I _C = 7.0 A _{dc} , V _{CE} = 4.0 V _{dc})	h _{FE}	30 30 30 2.3	150 150 150 —	—
Collector-Emitter Saturation Voltage (I _C = 7.0 A _{dc} , I _B = 3.0 A _{dc})	V _{CE(sat)}	—	3.5	V _{dc}
Base-Emitter On Voltage (I _C = 7.0 A _{dc} , V _{CE} = 4.0 V _{dc})	V _{BE(on)}	—	3.0	V _{dc}
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I _C = 500 mA _{dc} , V _{CE} = 4.0 V _{dc} , f _{test} = 1.0 MHz)	f _T	4.0 10	— —	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 1.0 MHz)	C _{ob}	—	250	pF
Small-Signal Current Gain (I _C = 0.5 A _{dc} , V _{CE} = 4.0 V _{dc} , f = 50 kHz)	h _{fe}	20	—	—

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

(2) f_T = |h_{fe}| • f_{test}

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



D₁ MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

FIGURE 3 — TURN-ON TIME

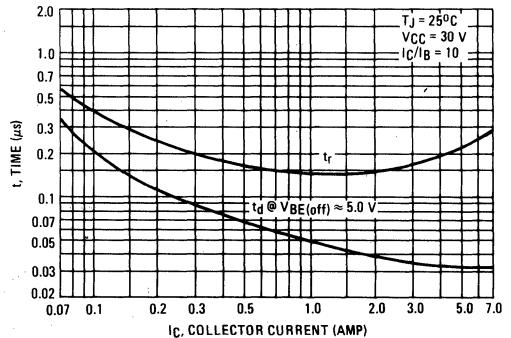


FIGURE 4 – THERMAL RESPONSE

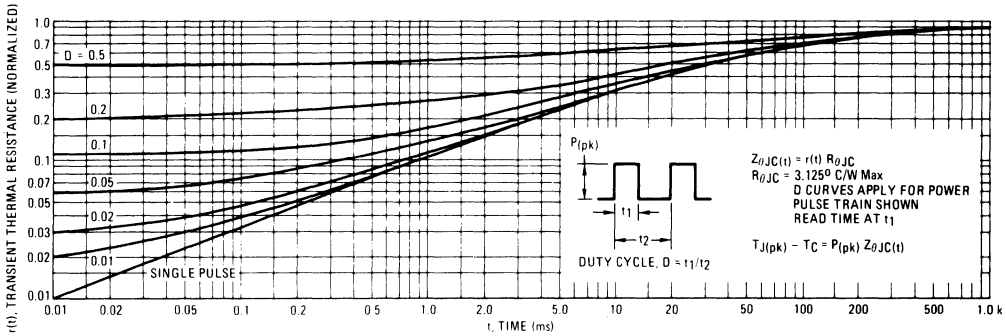
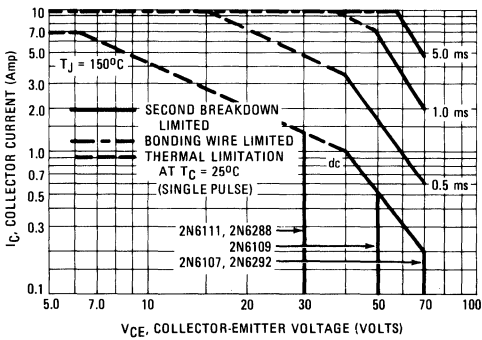


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – TURN-OFF TIME

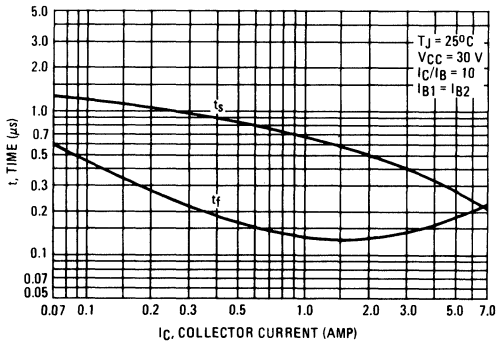
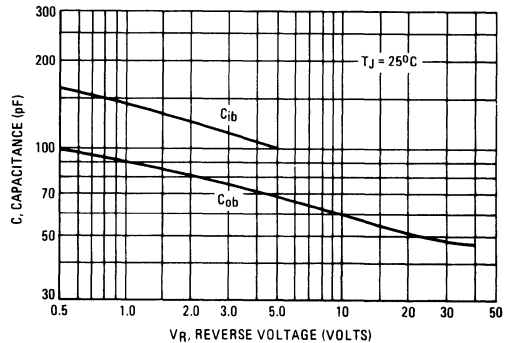


FIGURE 7 – CAPACITANCE



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

NPN
2N6121, 2N6122
2N6123
PNP
2N6124, 2N6125

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

... designed for use in power amplifier and switching circuits, - packaged in the compact TO-220AB outline. TO-66 leadform also available.

*MAXIMUM RATINGS

Rating	Symbol	2N6121 2N6124	2N6122 2N6125	2N6123	Unit
Collector-Emitter Voltage	V_{CE0}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current	I_C	4.0			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40			Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	$^\circ\text{C/W}$

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 0.1 \text{ Adc}, I_B = 0$)	2N6121, 2N6124 2N6122, 2N6125 2N6123	$V_{CE0(sus)}$	45 60 80	-	Vdc
Collector Cutoff Current ($V_{CE} = 45 \text{ Vdc}, I_B = 0$) ($V_{CE} = 60 \text{ Vdc}, I_B = 0$) ($V_{CE} = 80 \text{ Vdc}, I_B = 0$)	2N6121, 2N6124 2N6122, 2N6125 2N6123	I_{CE0}	-	1.0	mAdc
Collector Cutoff Current ($V_{CE} = 45 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 60 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 45 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$) ($V_{CE} = 60 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$) ($V_{CE} = 80 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$)	2N6121, 2N6124 2N6122, 2N6125 2N6123 2N6121, 2N6124 2N6122, 2N6125 2N6123, 2N6126	I_{CEX}	-	0.1 0.1 0.1 2.0 2.0 2.0	mAdc
Collector Cutoff Current ($V_{CB} = 45 \text{ Vdc}, I_E = 0$) ($V_{CB} = 60 \text{ Vdc}, I_E = 0$) ($V_{CB} = 80 \text{ Vdc}, I_E = 0$)	2N6121, 2N6124 2N6122, 2N6125 2N6123	I_{CBO}	-	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)		I_{EBO}	-	1.0	mAdc

ON CHARACTERISTICS

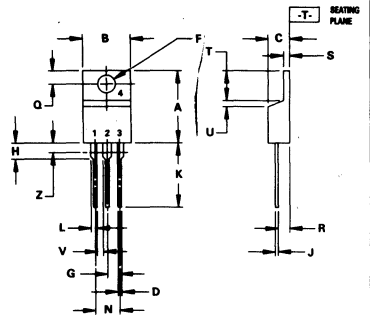
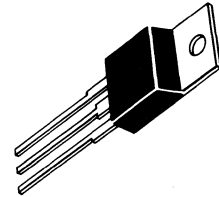
DC Current Gain (1) ($I_C = 1.5 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$)	2N6126, 2N6124 2N6122, 2N6125 2N6123	h_{FE}	25 25 20	100 100 80	-
($I_C = 4.0 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$)	2N6121, 2N6124 2N6122, 2N6125 2N6123	h_{FE}	10 10 7.0	-	-
Collector-Emitter Saturation Voltage (1) ($I_C = 1.5 \text{ Adc}, I_B = 0.15 \text{ Adc}$) ($I_C = 4.0 \text{ Adc}, I_B = 1.0 \text{ Adc}$)		$V_{CE(sat)}$	-	0.6 1.4	Vdc
Base-Emitter On Voltage (1) ($I_C = 1.5 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$)		$V_{BE(on)}$	-	1.2	Vdc

DYNAMIC CHARACTERISTICS

Small-Signal Current Gain ($I_C = 0.1 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}, f = 1.0 \text{ kHz}$)	h_{fe}	25	-	-
Current-Gain-Bandwidth Product ($I_C = 1.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}, f = 1.0 \text{ MHz}$)	f_T	2.5	-	MHz

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.
*Indicates JEDEC Registered Data.

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
45-80 VOLTS
40 WATTS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.65	10.29	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	-	0.045	-
Z	-	2.04	-	0.080

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

**2N6121, 2N6122, 2N6123, NPN,
2N6124, 2N6125, PNP**

FIGURE 1 – DC CURRENT GAIN

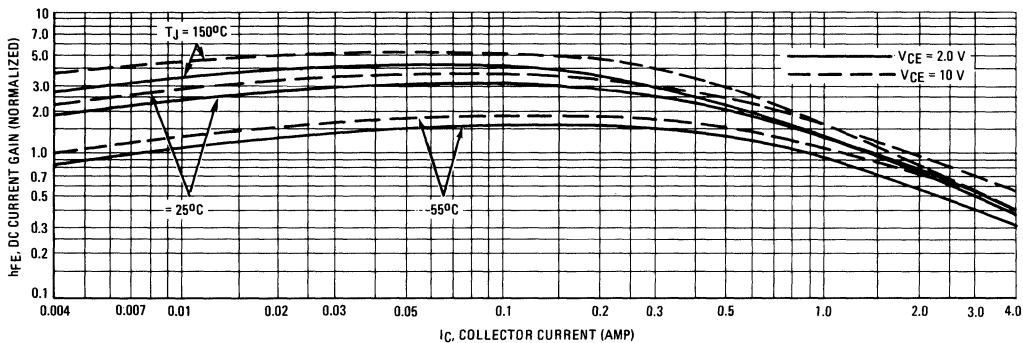


FIGURE 2 – COLLECTOR SATURATION REGION

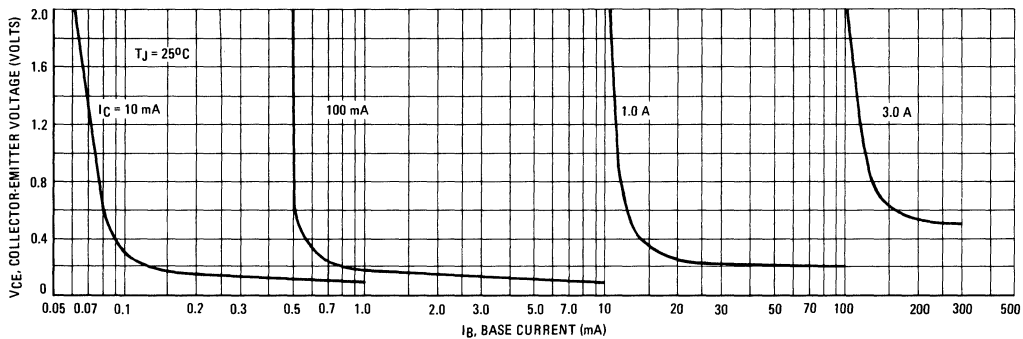


FIGURE 3 – "ON" VOLTAGES

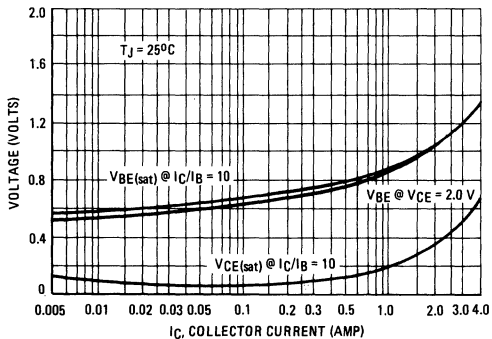
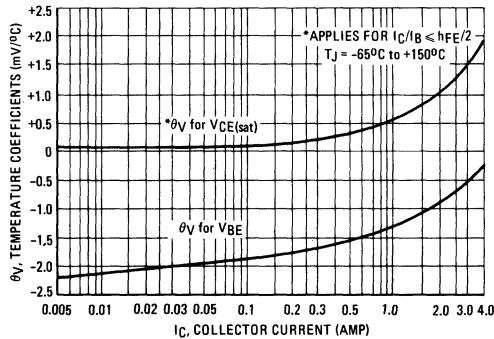


FIGURE 4 – TEMPERATURE COEFFICIENTS



3

**2N6121, 2N6122, 2N6123, NPN,
2N6124, 2N6125, PNP**

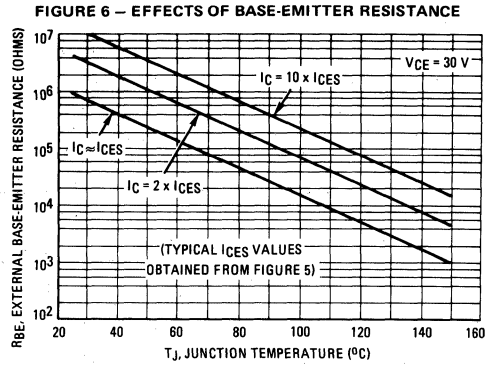
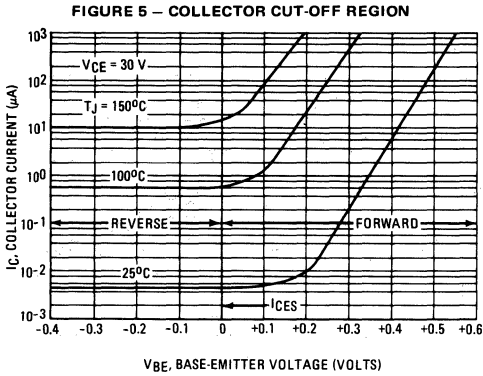
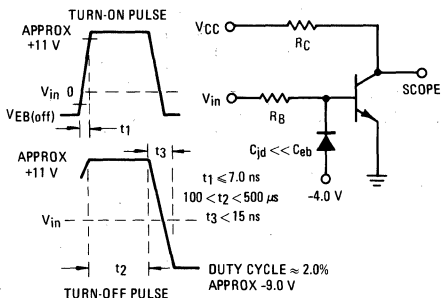
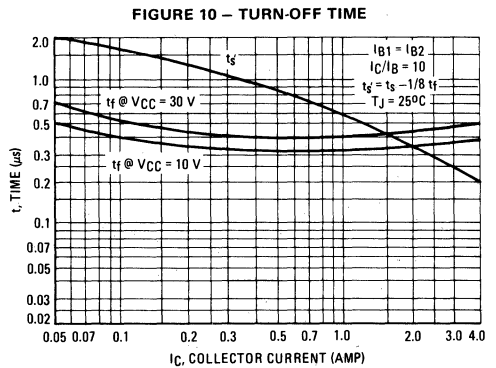
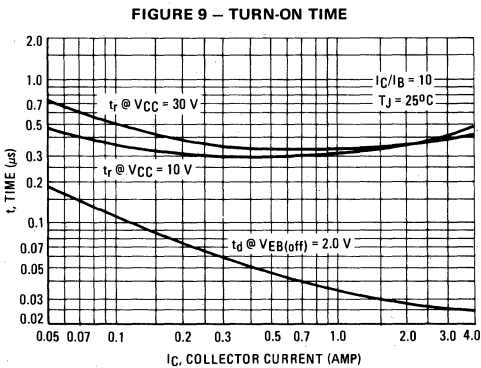
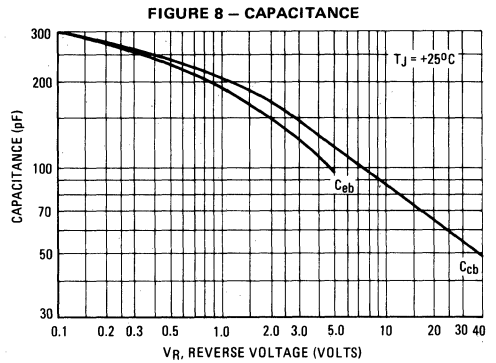


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT



R_B AND R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

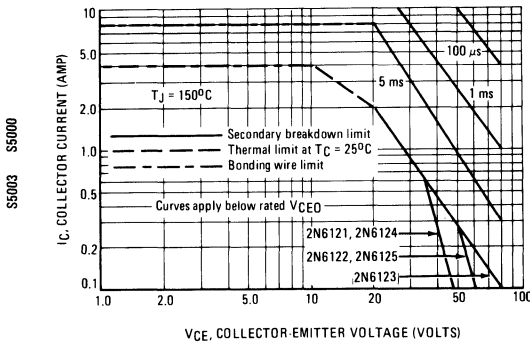
Reverse all polarities and diode for PNP transistors.



**2N6121, 2N6122, 2N6123, NPN,
2N6124, 2N6125, PNP**

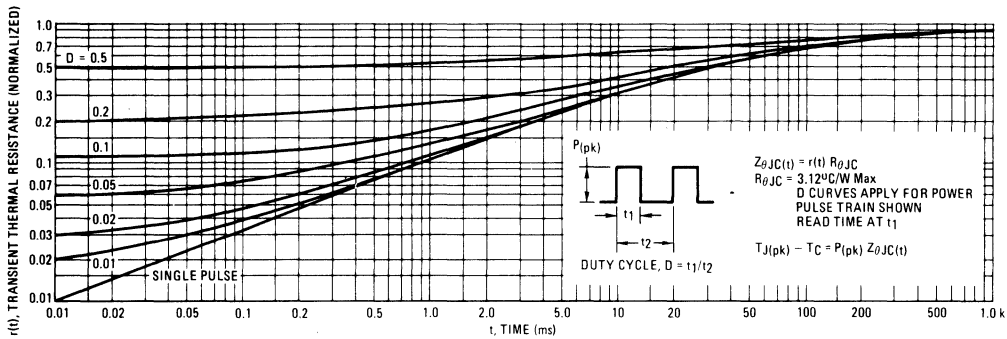
RATING AND THERMAL DATA

FIGURE 11 – ACTIVE REGION SAFE OPERATING AREA

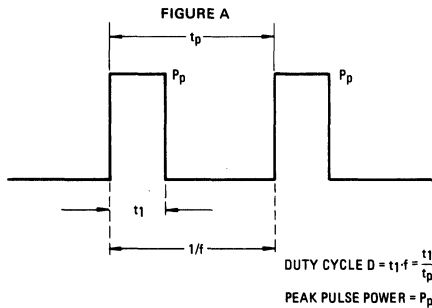


There are two limitations on the power handling ability of a transistor: **peak junction temperature and second breakdown.** Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 11 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 12 – THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC} .

Example:

The 2N6121 is dissipating 50 watts under the following conditions: $t_1 = 0.1$ ms, $t_p = 0.5$ ms. ($D = 0.2$).

Using Figure 12, at a pulse width of 0.1 ms and $D = 0.2$, the reading of $r(t_1, D)$ is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ\text{C}$$

2N6190
2N6191
2N6193

MEDIUM-POWER PNP SILICON TRANSISTORS

... designed for switching and wide band amplifier applications.

- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 1.2 \text{ Vdc (Max) @ } I_C = 5.0 \text{ Amp}$
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-205AD Case for Critical Space Limited Applications
- Complement to NPN 2N5336 thru 2N5339

5 AMPERE

POWER TRANSISTORS
PNP SILICON

80-100 VOLTS
10 WATTS

*** MAXIMUM RATINGS**

Rating	Symbol	2N6190 2N6191	2N6193	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	10		Watts
Derate above 25°C		57.1		mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C



THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	17.5	°C/W

*Indicates JEDEC Registered Data.

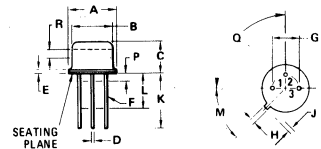
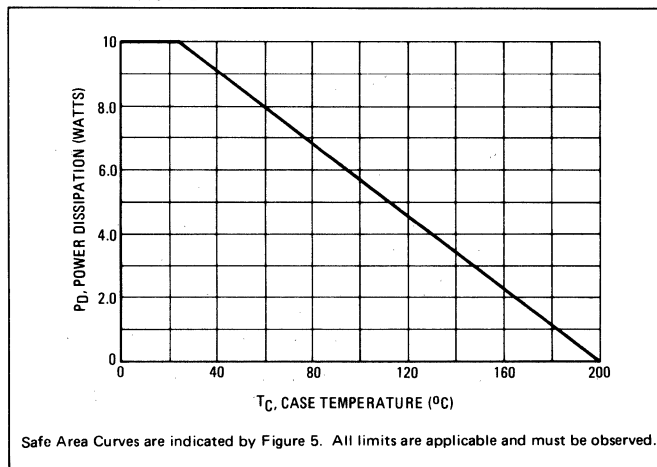


FIGURE 1 — POWER-TEMPERATURE DERATING



STYLE 1:
 PIN 1. EMITTER
 2. BASE
 3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° NOM	—	45° NOM	—
P	—	1.27	—	0.050
Q	90° NOM	—	90° NOM	—
R	2.54	—	0.100	—

All JEDEC dimensions and notes apply.

CASE 79-02
TO-205AD

2N6190, 2N6191, 2N6193

* ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 50 mA, I _B = 0)	V _{CEO(sus)}	80 100	— —	V _{dc}
Collector Cutoff Current (V _{CE} = 75 Vdc, I _B = 0) (V _{CE} = 90 Vdc, I _B = 0)	I _{CEO}	— —	100 100	μA _{dc}
Collector Cutoff Current (V _{CE} = 75 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CE} = 90 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CE} = 75 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 150°C) (V _{CE} = 90 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 150°C)	I _{CEx}	— — — —	10 10 1.0 1.0	μA _{dc} mA _{dc}
Collector Cutoff Current (V _{CB} = 80 Vdc, I _E = 0) (V _{CB} = 100 Vdc, I _E = 0)	I _{CBO}	— —	10 10	μA _{dc}
Emitter Cutoff Current (V _{BE} = 6.0 Vdc, I _C = 0)	I _{EBO}	—	100	μA _{dc}
ON CHARACTERISTICS (1)				
DC Current Gain (I _C = 500 mA, V _{CE} = 2.0 Vdc) (I _C = 2.0 A, V _{CE} = 2.0 Vdc) (I _C = 5.0 A, V _{CE} = 2.0 Vdc)	h _{FE}	30 60 30 60 20 40	— — 120 240 — —	—
Collector-Emitter Saturation Voltage (I _C = 2.0 A, I _B = 0.2 A) (I _C = 5.0 A, I _B = 0.5 A)	V _{CE(sat)}	— —	0.7 1.2	V _{dc}
Base-Emitter Saturation Voltage (I _C = 2.0 A, I _B = 0.2 A) (I _C = 5.0 A, I _B = 0.5 A)	V _{BE(sat)}	— —	1.2 1.8	V _{dc}
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (2) (I _C = 0.5 A, V _{CE} = 10 Vdc, f _{Test} = 10 MHz)	f _T	30	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 100 kHz)	C _{ob}	—	300	pF
Input Capacitance (V _{BE} = 2.0 Vdc, I _C = 0, f = 100 kHz)	C _{ib}	—	1250	pF
SWITCHING CHARACTERISTICS				
Delay Time (V _{CC} = 40 Vdc, V _{BE(off)} = 3.0 Vdc, I _C = 2.0 A, I _{B1} = 0.2 A)	t _d	—	100	ns
Rise Time (I _C = 2.0 A, I _{B1} = 0.2 A)	t _r	—	100	ns
Storage Time (V _{CC} = 40 Vdc, I _C = 2.0 A, I _{B1} = I _{B2} = 0.2 A)	t _s	—	2.0	μs
Fall Time (I _{B1} = I _{B2} = 0.2 A)	t _f	—	200	ns

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

(2) f_T = 1/h_{FE} · f_{Test}

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

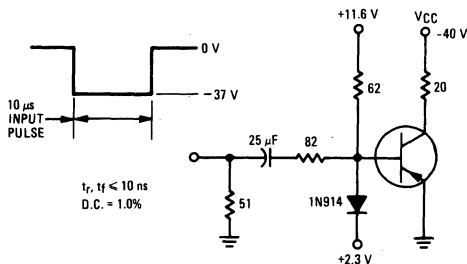


FIGURE 3 – TURN ON TIME

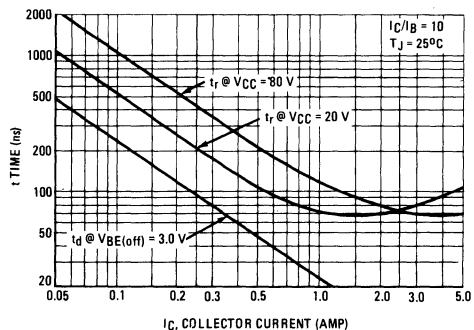


FIGURE 4 – THERMAL RESPONSE

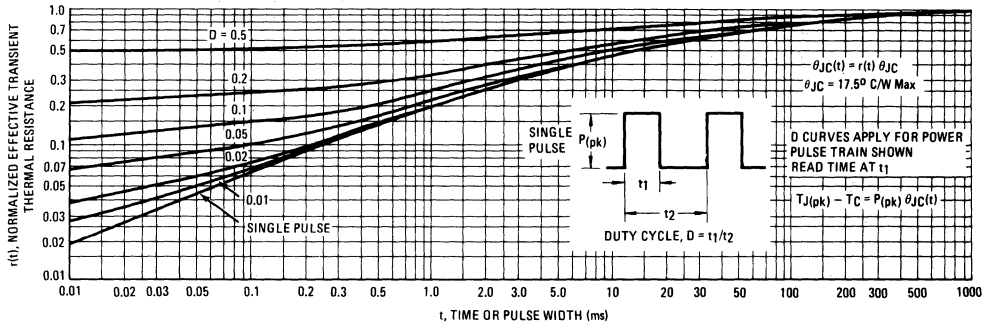
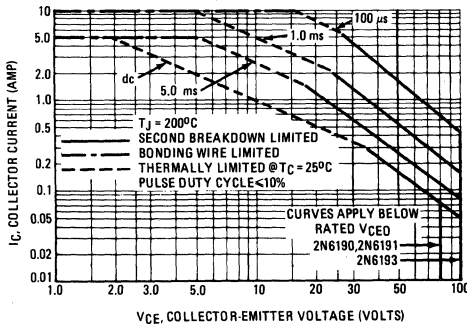


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

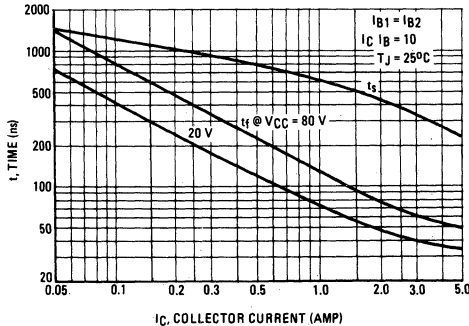
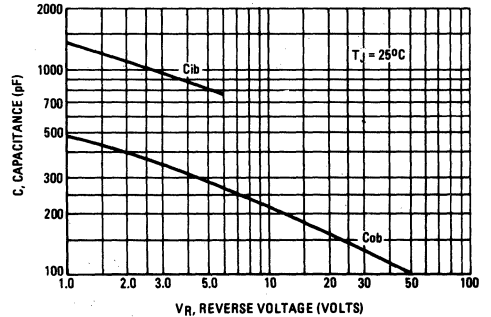


FIGURE 7 – CAPACITANCE versus VOLTAGE



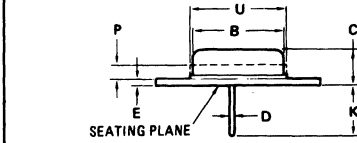
2N6211
2N6212
2N6213

MEDIUM-POWER HIGH-VOLTAGE
PNP POWER TRANSISTORS

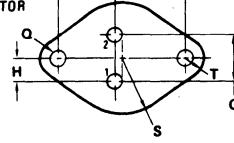
... designed for high-speed switching and linear amplifier applications for high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

- Collector-Emitter Sustaining Voltage – $V_{CE(sus)} = 225 \text{ to } 350 \text{ Vdc @ } I_C = 200 \text{ mAdc}$
- Second Breakdown Collector Current – $I_{s/b} = 875 \text{ mAdc @ } V_{CE} = 40 \text{ Vdc}$
- $t_f = 0.6 \mu\text{s}$ Resistive Fall Time
- Usable DC Current Gain to 2.0 Adc

2 AMPERE
POWER TRANSISTORS
PNP SILICON
225–350 VOLTS
35 WATTS



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE: COLLECTOR



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC Dimensions and Notes Apply.
CASE 80-02
TO-213AA

***MAXIMUM RATINGS**

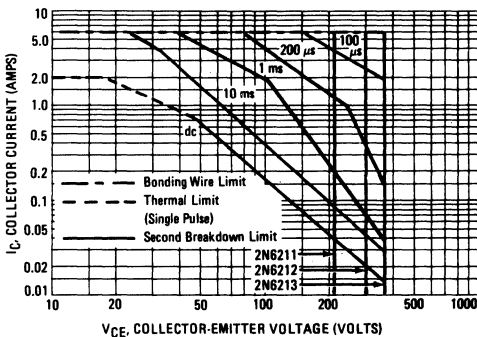
Rating	Symbol	2N6211	2N6212	2N6213	Unit
Collector-Emitter Voltage	V_{CEO}	225	300	350	Vdc
Collector-Base Voltage	V_{CB}	275	350	400	Vdc
Emitter-Base Voltage	V_{EB}	← 6 →			Vdc
Collector Current – Continuous	I_C	← 2 →			Adc
Peak		← 5 →			
Base Current	I_B	← 1 →			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	← 35 →			Watts
Derate above 25°C		← 0.2 →			$\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	$^\circ\text{C}/\text{W}$

*Indicates JEDEC Registered Data.

FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_J(pk) = 200$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See Figure 8).

2N6211, 2N6212, 2N6213

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mA}, I_B = 0$)	2N6211 2N6212 2N6213	$V_{CE(sus)}$	225 300 350	— — —	Vdc
*Collector-Emitter Sustaining Voltage ($I_C = 200 \text{ mA}, V_{BE} = -1.5 \text{ V}, L = 10 \text{ mH}$)	2N6211 2N6212 2N6213	$V_{CEX(sus)}$	275 350 400	— — —	Vdc
*Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mA}, I_B = 0, R_{BE} = 50 \Omega$)	2N6211 2N6212 2N6213	$V_{CER(sus)}$	250 325 375	— — —	Vdc
*Emitter-Base Breakdown Voltage (1) ($I_E = 0.5 \text{ mA}, I_C = 0$) ($I_E = 1.0 \text{ mA}, I_C = 0$)	2N6212/13 2N6211	V_{EBO}	6.0 6.0	— —	Vdc
*Collector Cutoff Current ($V_{CE} = 250 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 25^\circ\text{C}$) ($T_C = 100^\circ\text{C}$) ($V_{CE} = 315 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 25^\circ\text{C}$) ($T_C = 100^\circ\text{C}$) ($V_{CE} = 360 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 25^\circ\text{C}$) ($T_C = 100^\circ\text{C}$)		I_{CEV}	— — — —	0.5 5.0 0.5 5.0	mAdc
Collector Cutoff Current ($V_{CE} = 150 \text{ Vdc}, I_B = 0$)	All Types	I_{CEO}	—	5.0	mAdc
*Emitter Cutoff Current ($V_{EB} = 6.0 \text{ Vdc}, I_C = 0$)	2N6211 2N6212 2N6213	I_{EBO}	— — —	1.0 0.5 0.5	mAdc

*ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 1.0 \text{ Adc}, V_{CE} = 2.8 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}, V_{CE} = 3.2 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$)	2N6211 2N6212 2N6213	h_{FE}	10 10 10	100 100 100	—
Collector-Emitter Saturation Voltage ($I_C = 1.0 \text{ Adc}, I_B = 125 \text{ mAdc}$)	2N6211 2N6212 2N6213	$V_{CE(sat)}$	— — —	1.4 1.6 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0 \text{ Adc}, I_B = 125 \text{ mAdc}$)	All Types	$V_{BE(sat)}$	—	1.4	Vdc

DYNAMIC CHARACTERISTICS

*Current Gain—Bandwidth Product (2) ($I_C = 200 \text{ mA}, V_{CE} = 10 \text{ Vdc}, f_{test} = 5.0 \text{ MHz}$)		f_T	20	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 1.0 \text{ MHz}$)		C_{ob}	—	220	pF

*SECOND BREAKDOWN

*Second Breakdown Collector Current with Base Forward Biased $t = 1.0 \text{ s}$ (non-repetitive) ($V_{CE} = 40 \text{ Vdc}$)		$I_{S/b}$	0.875	—	A
--	--	-----------	-------	---	---

*SWITCHING CHARACTERISTICS

Rise Time	$V_{CC} = 200 \text{ Vdc}, I_C = 1.0 \text{ Adc}, I_{B1} = I_{B2} = 0.125 \text{ Adc}$	t_r	—	0.6	μs
Storage Time		t_s	—	2.5	μs
Fall Time		t_f	—	0.6	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $< 300 \mu\text{s}$, Duty Cycle $< 2.0\%$

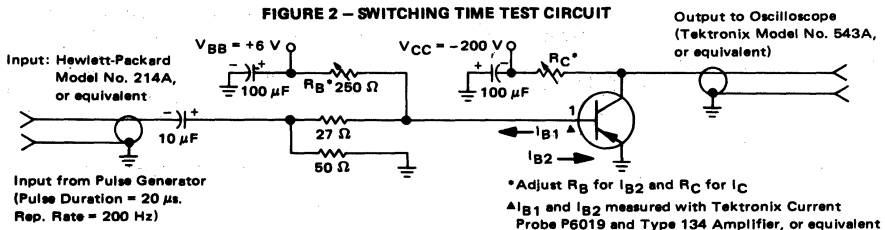


FIGURE 3 – DC CURRENT GAIN

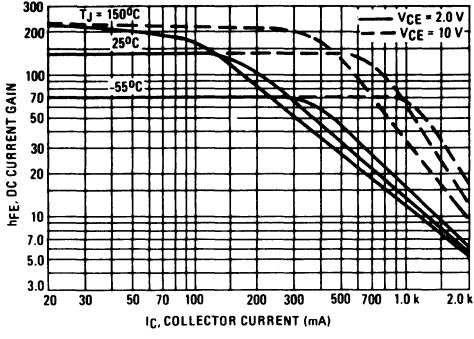


FIGURE 4 – COLLECTOR SATURATION REGION

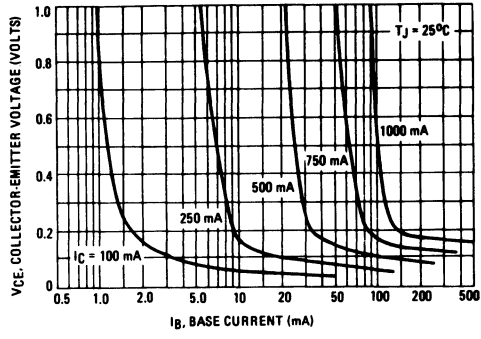


FIGURE 5 – COLLECTOR CUTOFF REGION

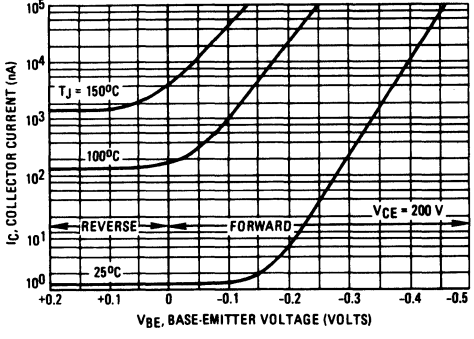


FIGURE 6 – TEMPERATURE COEFFICIENTS

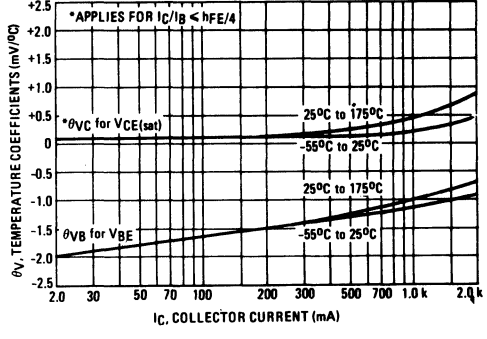


FIGURE 7 – BASE CUTOFF REGION

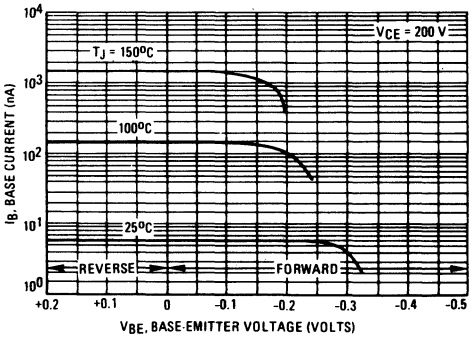
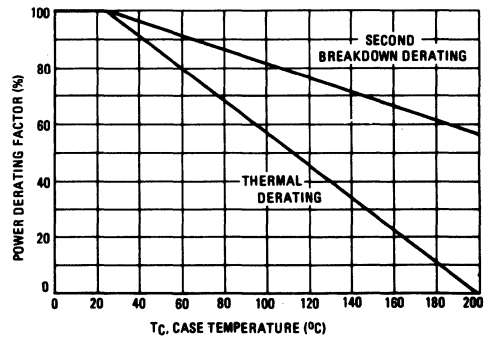


FIGURE 8 – POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6233
2N6235

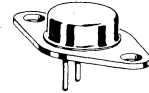
HIGH VOLTAGE NPN SILICON TRANSISTORS

... useful for high-voltage medium power applications such as switching regulators.

- High Collector-Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 225 \text{ Vdc} - 2N6233$
 $325 \text{ Vdc} - 2N6235$
- DC Current Gain – $h_{FE} = 25 \text{ to } 125 - I_C = 1.0 \text{ Adc}$
- Low Collector-Emitter Saturation Voltage
 $V_{CE(sat)} = 0.5 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Adc}$
- High Frequency Response – $f_T = 20 \text{ MHz (Min)}$
- Fast Switching Times @ 1.0 Adc –
 $t_r = 0.5 \mu\text{s (Max)}$
 $t_s = 3.5 \mu\text{s (Max)}$
 $t_f = 0.5 \mu\text{s (Max)}$

5 AMPERE
POWER TRANSISTORS
NPN SILICON

225,275,325 VOLTS
50 WATTS



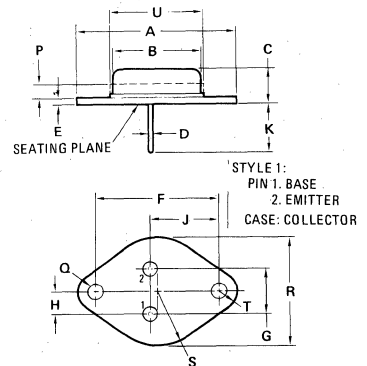
***MAXIMUM RATINGS**

Rating	Symbol	2N6233	2N6235	Unit
Collector-Emitter Voltage	V_{CEO}	225	325	Vdc
Collector-Base Voltage	V_{CB}	250	350	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous	I_C	5.0		Adc
Peak		10		
Base Current	I_B	2.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	50		Watts
		0.286		
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.5	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data.



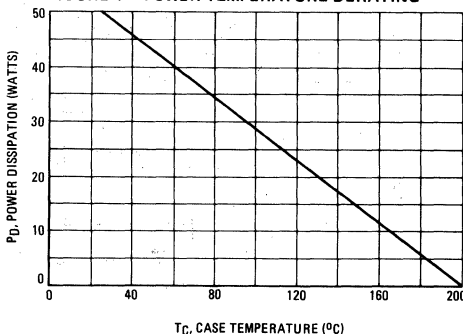
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC Dimensions and Notes Apply.

CASE 80-02
TO-213AA

3

FIGURE 1 – POWER TEMPERATURE DERATING



***ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted)

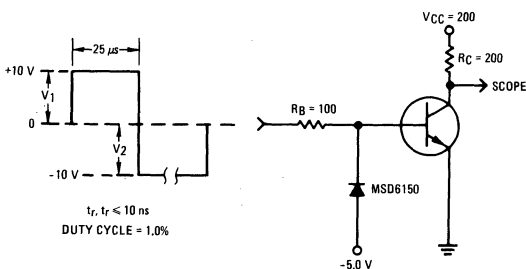
Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 20\text{ mAdc}, I_B = 0$)	2N6233 2N6235	$V_{CE(sus)}$	225 325	— —	Vdc
Collector Cutoff Current ($V_{CE} = 225, I_B = 0$) ($V_{CE} = 325, I_B = 0$)	2N6233 2N6235	I_{CEO}	— —	1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 250\text{ Vdc}, V_{EB(off)} = 1.5\text{ Vdc}, T_C = 150^\circ\text{C}$) ($V_{CE} = 350\text{ Vdc}, V_{EB(off)} = 1.5\text{ Vdc}, T_C = 150^\circ\text{C}$)	2N6233 2N6235	I_{CEX}	— —	1.0 1.0	mAdc
Collector Cutoff Current ($V_{CB} = 250\text{ Vdc}, I_E = 0$) ($V_{CB} = 350\text{ Vdc}, I_E = 0$)	2N6233 2N6235	I_{CBO}	— —	0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 6.0\text{ Vdc}, I_C = 0$)		I_{EBO}	—	0.1	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 0.1\text{ Adc}, V_{CE} = 5.0\text{ Vdc}$) ($I_C = 1.0\text{ Adc}, V_{CE} = 5.0\text{ Vdc}$) ($I_C = 3.0\text{ Adc}, V_{CE} = 5.0\text{ Vdc}$)		h_{FE}	25 25 10	— 125 —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}, I_B = 0.1\text{ Adc}$) ($I_C = 5.0\text{ Adc}, I_B = 1.0\text{ Adc}$)		$V_{CE(sat)}$	— —	0.5 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}, I_B = 0.1\text{ Adc}$) ($I_C = 5.0\text{ Adc}, I_B = 1.0\text{ Adc}$)		$V_{BE(sat)}$	— —	1.0 2.0	Vdc
Base-Emitter On Voltage ($I_C = 1.0\text{ Adc}, V_{CE} = 5.0\text{ Vdc}$)		$V_{BE(on)}$	—	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (2) ($I_C = 0.25\text{ Adc}, V_{CE} = 10\text{ Vdc}, f_{test} = 10\text{ MHz}$)		f_T	20	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}, I_E = 0, f = 0.1\text{ MHz}$)		C_{ob}	—	250	pF
SWITCHING CHARACTERISTICS					
Rise Time ($V_{CC} = 200\text{ Vdc}, I_C = 1.0\text{ Adc}, I_B = 0.1\text{ Adc}$)		t_r	—	0.5	μs
Storage Time ($V_{CC} = 200\text{ Vdc}, I_C = 1.0\text{ Adc}, I_{B1} = I_{B2} = 0.1\text{ Adc}$)		t_s	—	3.5	μs
Fall Time ($V_{CC} = 200\text{ Vdc}, I_C = 1.0\text{ Adc}, I_{B1} = I_{B2} = 0.1\text{ Adc}$)		t_f	—	0.5	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



FOR INFORMATION ON FIGURES 3 and 6
 R_B AND R_C ARE VARIED TO OBTAIN
 DESIRED CURRENT LEVELS; D_1 DIS-
 CONNECTED AND V_2 REDUCED TO 5
 VOLTS FOR t_d MEASUREMENT.

FIGURE 3 – TURN-ON TIME

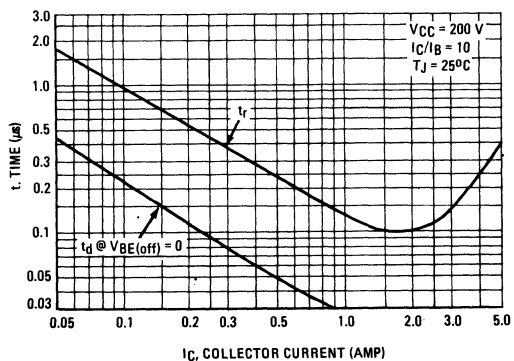


FIGURE 4 – THERMAL RESPONSE

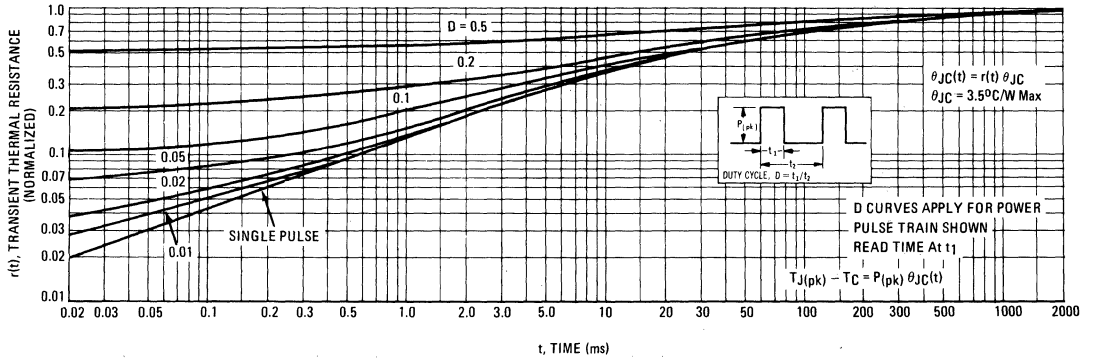
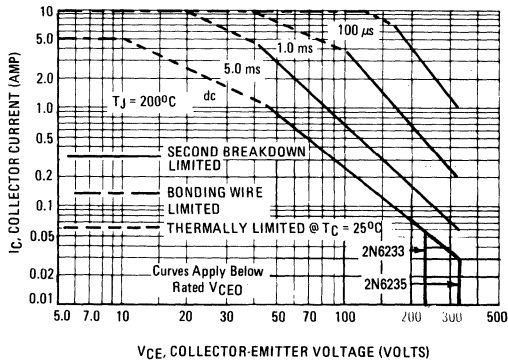


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

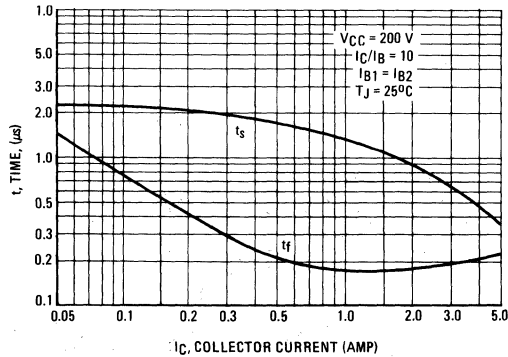
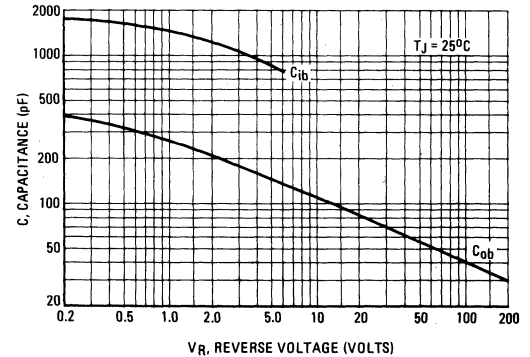


FIGURE 7 – CAPACITANCES



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6249
2N6250
2N6251

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

... designed for high voltage inverters, switching regulators and line operated amplifier applications. Especially well suited for switching power supply applications.

- High Voltage Breakdown Rating
- Low Saturation Voltages
- Fast Switching Capability
- High E_S/b Energy Handling Capability

MAXIMUM RATINGS

Rating	Symbol	2N6249	2N6250	2N6251	Unit
*Collector-Emitter Voltage	$V_{CE0(sus)}$	200	275	350	Vdc
*Collector-Emitter Voltage	$V_{CER(sus)}$	225	300	375	Vdc
*Collector-Base Voltage	V_{CB}	300	375	450	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current — Continuous*	I_C	← 15 →			Adc
— Peak	I_{CM}	← 30 →			Adc
Base Current — Continuous*	I_B	← 10 →			Adc
— Peak	I_{BM}	← 20 →			Adc
Emitter Current — Continuous	I_E	← 25 →			Adc
— Peak	I_{EM}	← 50 →			Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	← 175 →			Watts
@ $T_C = 100^\circ C$		← 100 →			Watts
Derate above $25^\circ C$ *		← 1.0 →			W/ $^\circ C$
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			$^\circ C$

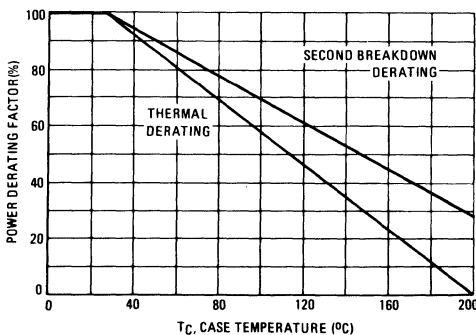
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ C$

*Indicates JEDEC Registered Data.

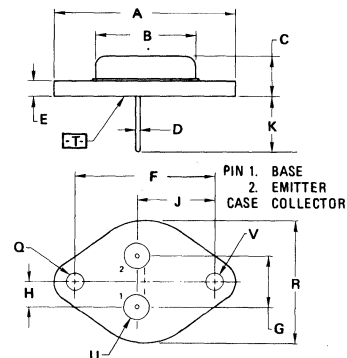
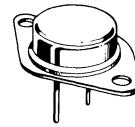
**JEDEC Registered Value is 10 A, Motorola Guaranteed Value is 15 A.

FIGURE 1 — POWER DERATING



15 AMPERE
POWER TRANSISTORS
NPN SILICON

200, 275, 350 VOLTS
175 WATTS



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
 2. \perp IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\phi \pm 0.13 (0.005) \text{ (M) } \text{ (T) } \text{ (V) } \text{ (M)}$$

FOR LEADS:

$$\phi \pm 0.13 (0.005) \text{ (M) } \text{ (T) } \text{ (V) } \text{ (M) } \text{ (Q) } \text{ (M)}$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

2N6249, 2N6250, 2N6251

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 200 mA, I _B = 0)	V _{CEO(sus)}	200 275 350	— — —	V _{dc}	
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 200 mA)	V _{CER(sus)}	225 300 375	— — —	V _{dc}	
Collector Cutoff Current (V _{CE} = Rated V _{CER} , V _{BE(off)} = 1.5 V _{dc}) (V _{CE} = Rated V _{CER} , V _{BE(off)} = 1.5 V _{dc} , T _C = 125°C)	I _{CEV}	— —	5.0 10	mAdc	
Collector Cutoff Current (V _{CE} = 150 V _{dc} , I _B = 0) (V _{CE} = 225 V _{dc} , I _B = 0) (V _{CE} = 300 V _{dc} , I _B = 0)	I _{CEO}	— — —	5.0 5.0 5.0	mAdc	
Emitter Cutoff Current (V _{EB} = 6.0 V _{dc} , I _C = 0)	I _{EBO}	—	1.0	mAdc	
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward (V _{CE} = 30 V) biased t = 1.0 s (non-repetitive)	I _{S/b}	5.8 0.3	— —	V _{dc}	
Second Breakdown Energy with base reverse biased (Table 1) (I _C = 10 A, V _{BE(off)} = 4.0 V _{dc} , L = 50 μH)	E _{S/b}	2.5	—	mJ	
ON CHARACTERISTICS (1)					
DC Current Gain (I _C = 10 Adc, V _{CE} = 3.0 V _{dc})	h _{FE}	10 8.0 6.0	50 50 50	—	
Collector-Emitter Saturation Voltage (I _C = 10 Adc, I _B = 1.0 Adc) (I _C = 10 Adc, I _B = 1.25 Adc) (I _C = 10 Adc, I _B = 1.67 Adc)	V _{CE(sat)}	— — —	1.5 1.5 1.5	V _{dc}	
Base-Emitter Saturation Voltage (I _C = 10 Adc, I _B = 1.0 Adc) (I _C = 10 Adc, I _B = 1.25 Adc) (I _C = 10 Adc, I _B = 1.67 Adc)	V _{BE(sat)}	— — —	2.5 2.5 2.5	V _{dc}	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I _C = 1.0 Adc, V _{CE} = 10 V _{dc} , f _{test} = 1.0 MHz)	f _T	2.5	—	MHz	
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Rise Time	(V _{CC} = 200 V _{dc} , I _C = 10 A, Duty Cycle ≤ 2.0%, t _p = 100 μs)	t _r	—	2.0	μs
Storage Time	(I _{B1} = I _{B2} = 1.0 Adc) 2N6249 (I _{B1} = I _{B2} = 1.25 Adc) 2N6250 (I _{B1} = I _{B2} = 1.67 Adc) 2N6251	t _s	—	3.5	μs
Fall Time		t _f	—	1.0	μs

* Indicates JEDEC Registered Data.

(1) Measured on a curve tracer (60 Hz full-wave rectified sine wave).

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CEO(sus)}	V _{CEr(sus)}	E _{s/h}	RESISTIVE SWITCHING
INPUT CONDITIONS				
CIRCUIT VALUES	L _{coil} = 42 mH R _{coil} = 0.7 Ω, f _o = 60 Hz V _{CC} = 0 to 50 V	L _{coil} = 14 mH R _{coil} = 0.05 Ω V _{CC} = 0 to 50 V f _o = 60 Hz	L _{coil} = 50 μH V _{CC} = 11.5 V R _{coil} = 0.2 Ω	V _{CC} = 200 V R _L = 20 Ω
TEST CIRCUITS			t ₁ Adjusted to Obtain I _C $t_1 = \frac{L_{coil} (I_{Cpk})}{V_{CC}}$	

FIGURE 2 – THERMAL RESPONSE

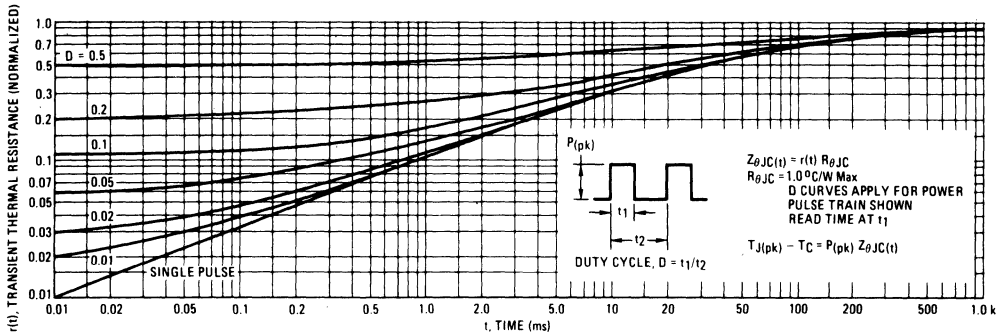
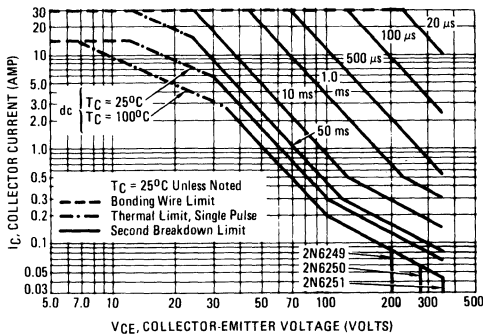


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC-VCE limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_C = 25^{\circ}C$, $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^{\circ}C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 3 may be found at any case temperature by using the appropriate curve on Figure 1.

$T_J(pk)$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

DC CHARACTERISTICS

FIGURE 4 - DC CURRENT GAIN

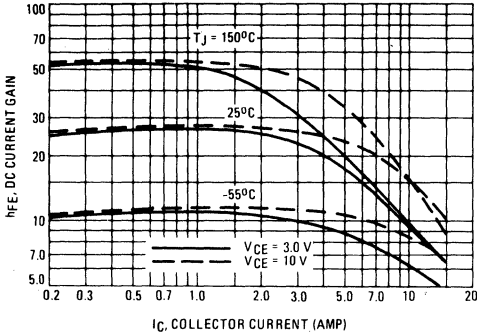


FIGURE 5 - COLLECTOR SATURATION REGION

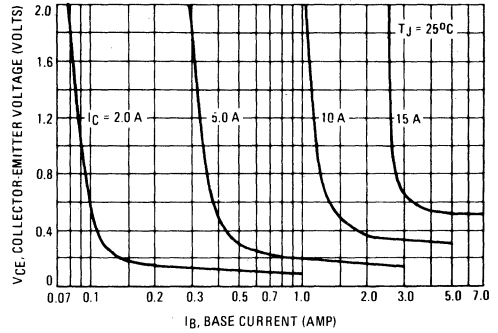


FIGURE 6 - "ON" VOLTAGE

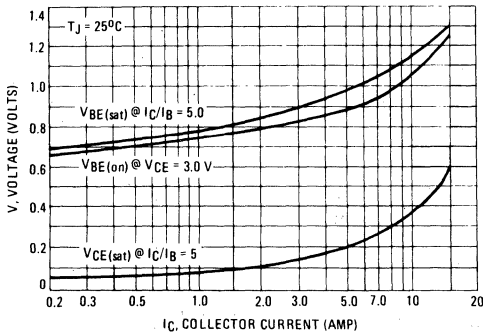
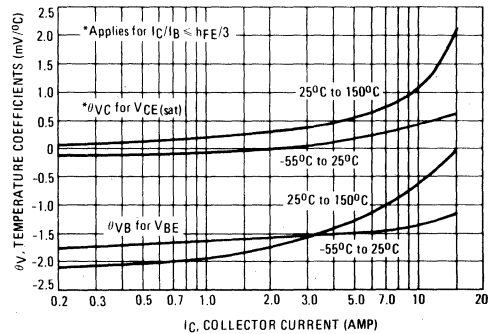


FIGURE 7 - TEMPERATURE COEFFICIENTS



RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 - TURN-ON TIME

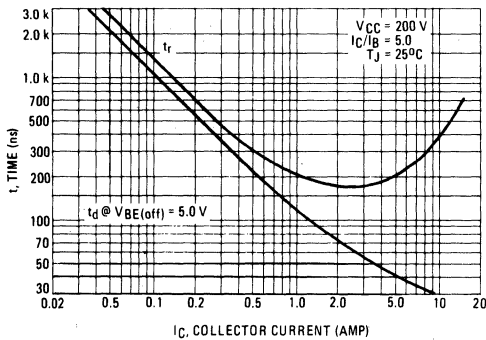
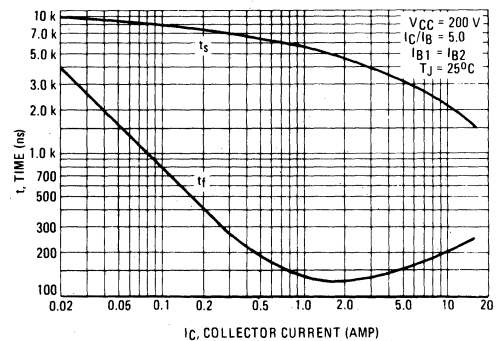


FIGURE 9 - TURN-OFF TIME



3

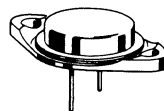
2N6274
2N6275
2N6277

HIGH-POWER NPN SILICON TRANSISTORS

... designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector Emitter Sustaining Voltage –
 $V_{CE(sus)} = 100 \text{ Vdc (Min) – 2N6274}$
 $= 120 \text{ Vdc (Min) – 2N6275}$
 $= 150 \text{ Vdc (Min) – 2N6277}$
- High DC Current Gain –
 $h_{FE} = 30\text{-}120 @ I_C = 20 \text{ Adc}$
 $= 10 \text{ (Min) } @ I_C = 50 \text{ Adc}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) } @ I_C = 20 \text{ Adc}$
- Fast Switching Times @ $I_C = 20 \text{ Adc}$
 $t_r = 0.35 \mu\text{s (Max)}$
 $t_s = 0.8 \mu\text{s (Max)}$
 $t_f = 0.25 \mu\text{s (Max)}$
- Complement to 2N6377-79

50 AMPERE
POWER TRANSISTORS
NPN SILICON
100, 120, 140, 150 VOLTS
250 WATTS



***MAXIMUM RATINGS**

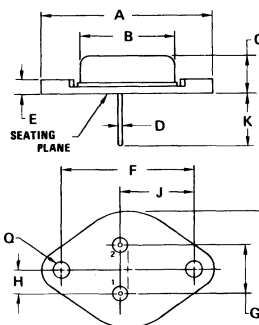
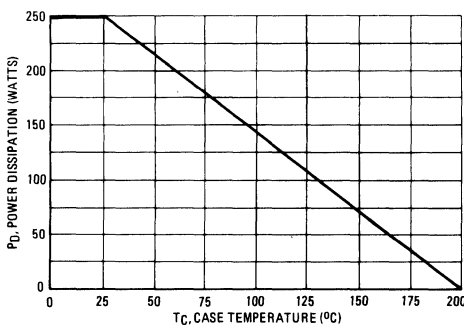
Rating	Symbol	2N6274	2N6275	2N6277	Unit
Collector-Base Voltage	V_{CB}	120	140	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	150	Vdc
Emitter-Base Voltage	V_{EB}	6.0			Vdc
Collector Current – Continuous Peak	I_C	50 100			Adc
Base Current	I_B	20			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	250 1.43			Watts $W/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	-	3.43	-	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-204AE

2N6274, 2N6275, 2N6277

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 50 mA, I _B = 0)	V _{CEO(sus)}	100 120 150	—	V _{dc}
Collector Cutoff Current (V _{CE} = 50 V _{dc} , I _B = 0) (V _{CE} = 60 V _{dc} , I _B = 0) (V _{CE} = 75 V _{dc} , I _B = 0)	I _{CEO}	— — —	50 50 50	μA _{dc}
Collector Cutoff Current (V _{CE} = Rated V _{CB} , V _{EB(off)} = 1.5 V _{dc}) (V _{CE} = Rated V _{CB} , V _{EB(off)} = 1.5 V _{dc} , T _C = 150°C)	I _{CEX}	— —	10 1.0	μA _{dc} mA _{dc}
Emitter Cutoff Current (V _{BE} = 6.0 V _{dc} , I _C = 0)	I _{EBO}	—	100	μA _{dc}

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 1.0 A _{dc} , V _{CE} = 4.0 V _{dc}) (I _C = 20 A _{dc} , V _{CE} = 4.0 V _{dc}) (I _C = 50 A _{dc} , V _{CE} = 4.0 V _{dc})	h _{FE}	50 30 10	— 120 —	—
Collector-Emitter Saturation Voltage (I _C = 20 A _{dc} , I _B = 2.0 A _{dc}) (I _C = 50 A _{dc} , I _B = 10 A _{dc})	V _{CE(sat)}	— —	1.0 3.0	V _{dc}
Base-Emitter Saturation Voltage (I _C = 20 A _{dc} , I _B = 2.0 A _{dc}) (I _C = 50 A _{dc} , I _B = 10 A _{dc})	V _{BE(sat)}	— —	1.8 3.5	V _{dc}
Base-Emitter On Voltage (I _C = 20 A _{dc} , V _{CE} = 4.0 V _{dc})	V _{BE(on)}	—	1.8	V _{dc}

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product (2) (I _C = 1.0 A _{dc} , V _{CE} = 10 V _{dc} , f _{test} = 10 MHz)	f _T	30	—	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 0.1 MHz)	C _{ob}	—	600	pF

SWITCHING CHARACTERISTICS

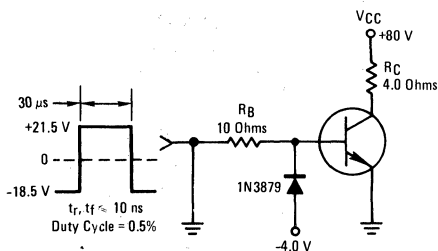
Rise Time (V _{CC} = 80 V _{dc} , I _C = 20 A _{dc} , I _{B1} = 2.0 A _{dc} , V _{BE(off)} = 5.0 V _{dc})	t _r	—	0.35	μs
Storage Time (V _{CC} = 80 V _{dc} , I _C = 20 A _{dc} , I _{B1} = I _{B2} = 2.0 A _{dc})	t _s	—	0.80	μs
Fall Time (V _{CC} = 80 V _{dc} , I _C = 20 A _{dc} , I _{B1} = I _{B2} = 2.0 A _{dc})	t _f	—	0.25	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) f_T = h_{FE} · f_{test}.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN-ON TIME

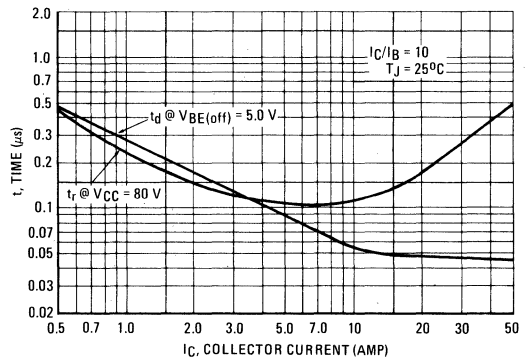


FIGURE 4 – THERMAL RESPONSE

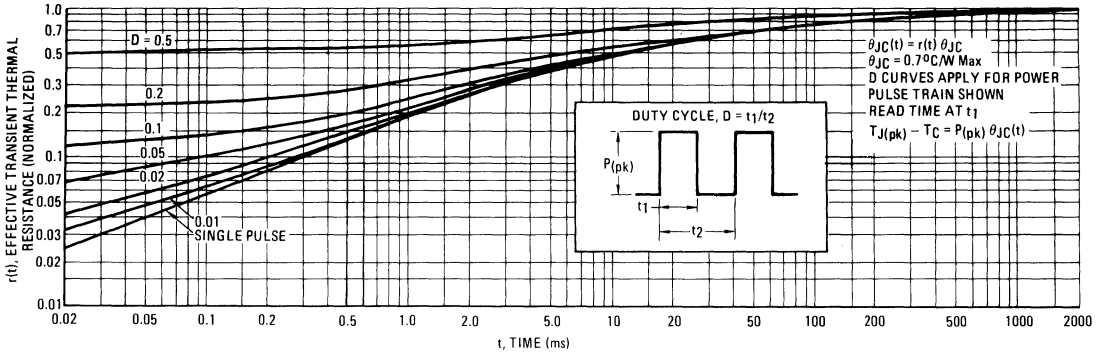
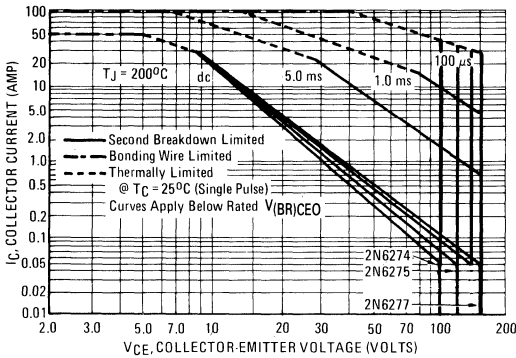


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

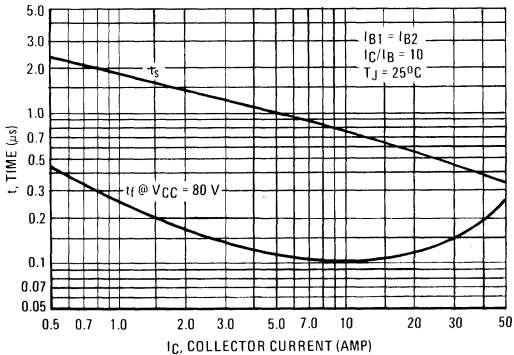


FIGURE 7 – CAPACITANCE

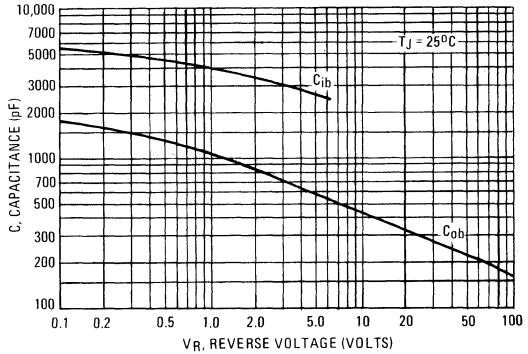


FIGURE 8 – DC CURRENT GAIN

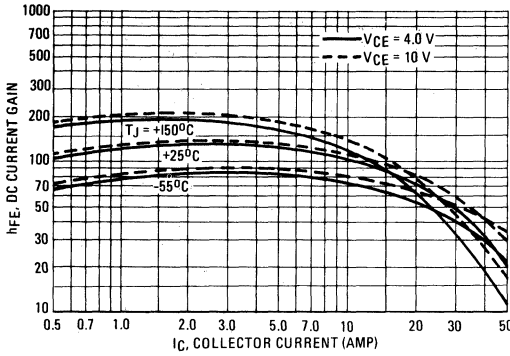


FIGURE 9 – COLLECTOR SATURATION REGION

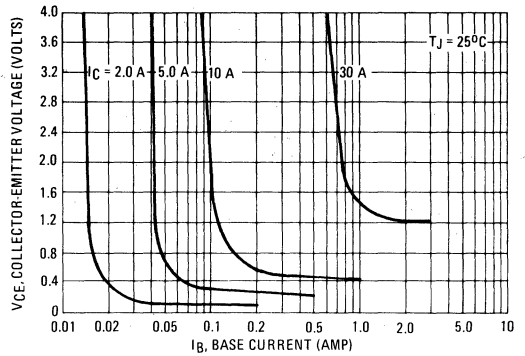


FIGURE 10 – "ON" VOLTAGES

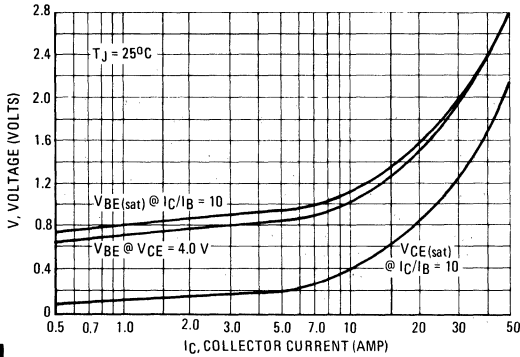


FIGURE 11 – TEMPERATURE COEFFICIENTS

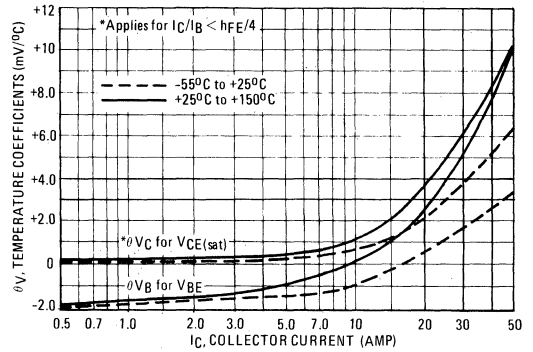


FIGURE 12 – COLLECTOR CUT-OFF REGION

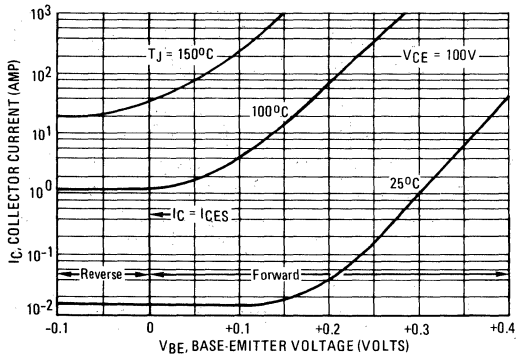
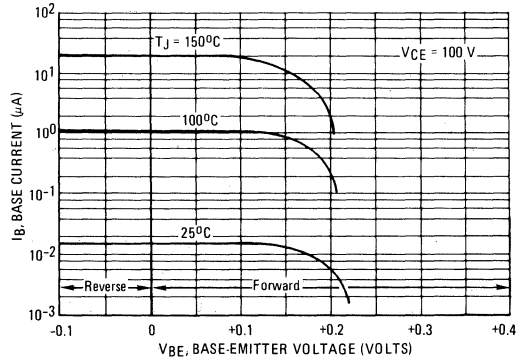


FIGURE 13 – BASE CUT-OFF REGION



NPN
2N6282 thru 2N6284
PNP
2N6285 thru 2N6287

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for general-purpose amplifier and low-frequency switching applications.

- High DC Current Gain @ $I_C = 10 \text{ Adc}$ –
 $h_{FE} = 2400 \text{ (Typ)} - 2N6282, 2N6283, 2N6284$
 $= 4000 \text{ (Typ)} - 2N6285, 2N6286, 2N6287$
- Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 60 \text{ Vdc (Min)} - 2N6282, 2N6285$
 $= 80 \text{ Vdc (Min)} - 2N6283, 2N6286$
 $= 100 \text{ Vdc (Min)} - 2N6284, 2N6287$
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON
20 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS

60, 80, 100 VOLTS
160 WATTS

***MAXIMUM RATINGS**

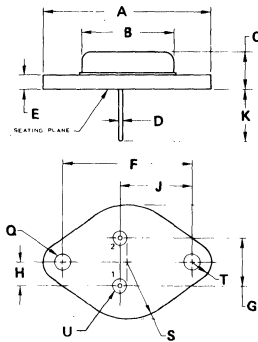
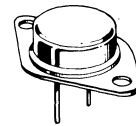
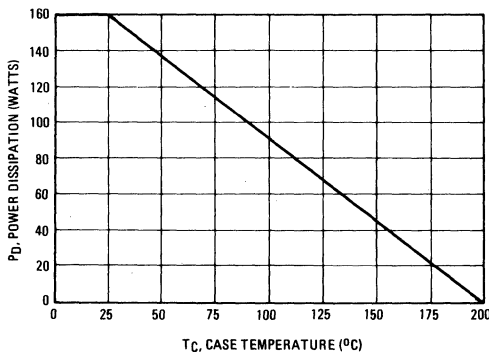
Rating	Symbol	2N6282 2N6285	2N6283 2N6286	2N6284 2N6287	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	20 40			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	160 0.915			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			$^\circ\text{C}$

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.09	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120

NOTES:

1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

CASE 1-04
TO-204AA

2N6282, 2N6283, 2N6284 NPN 2N6285, 2N6286, 2N6287 PNP

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ($I_C = 0.1 \text{ Adc}$, $I_B = 0$)	$V_{CE(sus)}$	60 80 100	—	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 50 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	— — —	1.0 1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	— —	0.5 5.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	2.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 20 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	h_{FE}	750 100	18,000 —	—
Collector-Emitter Saturation Voltage ($I_C = 10 \text{ Adc}$, $I_B = 40 \text{ mAdc}$) ($I_C = 20 \text{ Adc}$, $I_B = 200 \text{ mAdc}$)	$V_{CE(sat)}$	— —	2.0 3.0	Vdc
Base-Emitter On Voltage ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	$V_{BE(on)}$	—	2.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 20 \text{ Adc}$, $I_B = 200 \text{ mAdc}$)	$V_{BE(sat)}$	—	4.0	Vdc

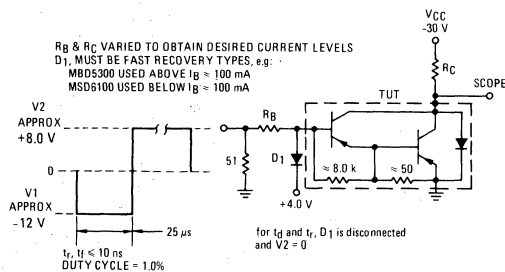
DYNAMIC CHARACTERISTICS

Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	$ h_{fe} $	4.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	— —	400 600	pF
Small-Signal Current Gain ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	300	—	—

* Indicates JEDEC Registered Data.

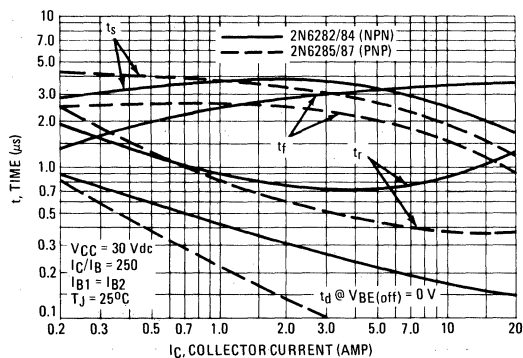
(1) Pulse test: Pulse Width = 300 μs , Duty Cycle = 2%

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



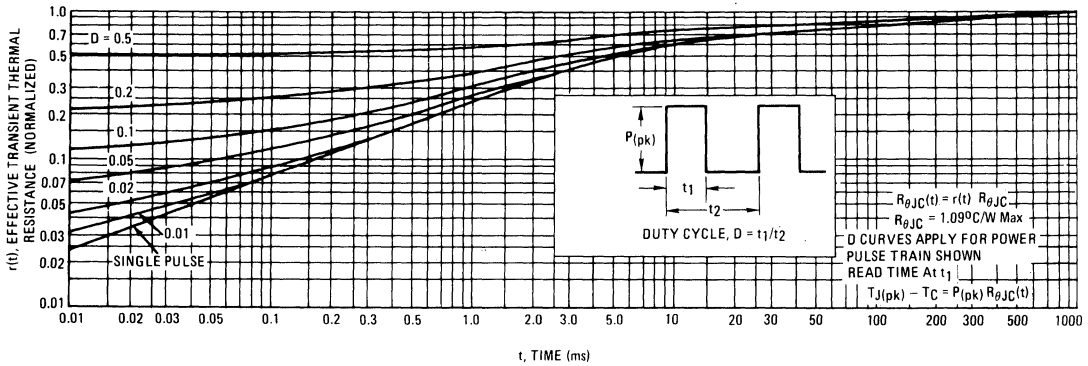
For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 — SWITCHING TIMES



2N6282, 2N6283, 2N6284 NPN
2N6285, 2N6286, 2N6287 PNP

FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6282, 2N6285

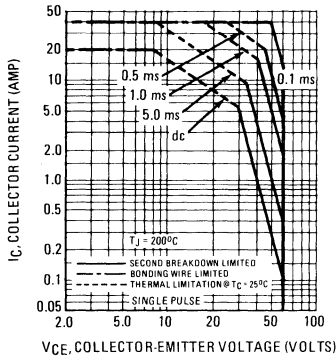


FIGURE 6 – 2N6283, 2N6286

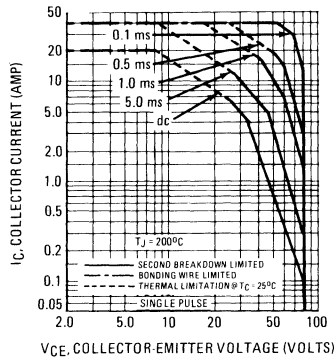
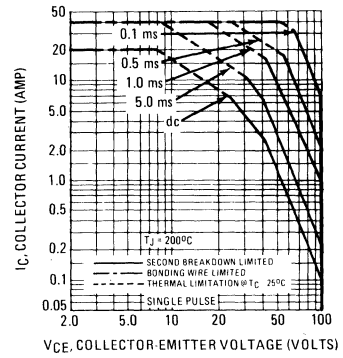


FIGURE 7 – 2N6284, 2N6287



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6 and 7 is based on $T_{J(pk)} = 200^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 – SMALL-SIGNAL CURRENT GAIN

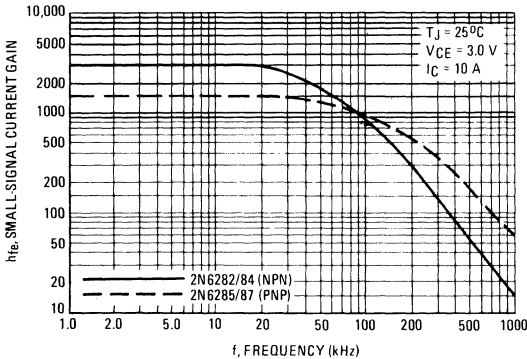
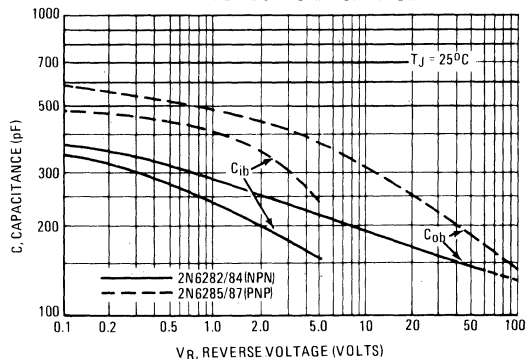


FIGURE 9 – CAPACITANCE



2N6282, 2N6283, 2N6284 NPN
2N6285, 2N6286, 2N6287 PNP

NPN
2N6282, 2N6283, 2N6284

PNP
2N6285, 2N6286, 2N6287

FIGURE 10 - DC CURRENT GAIN

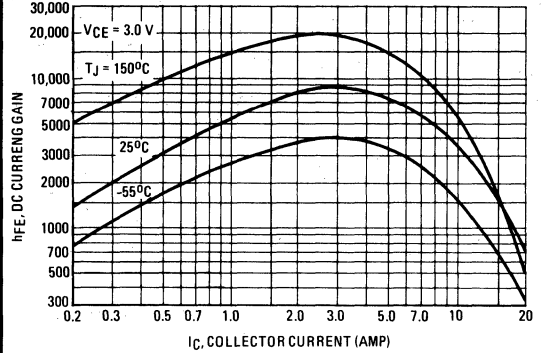
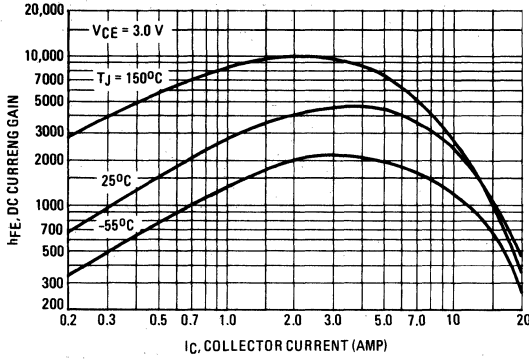


FIGURE 11 - COLLECTOR SATURATION REGION

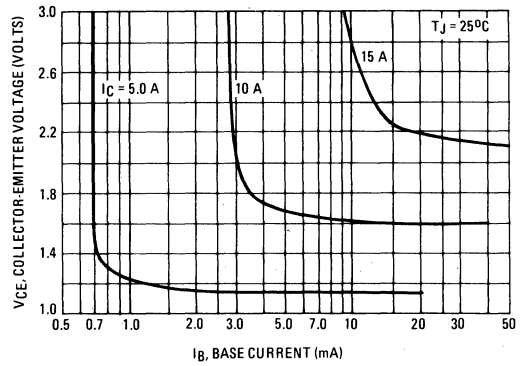
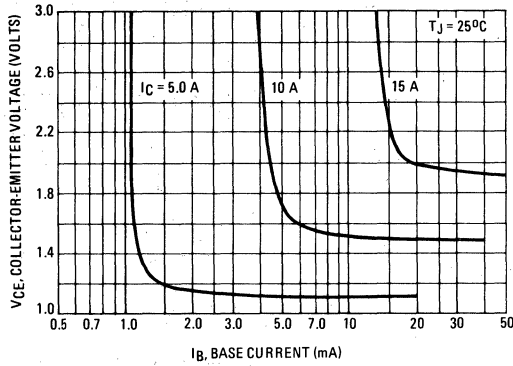
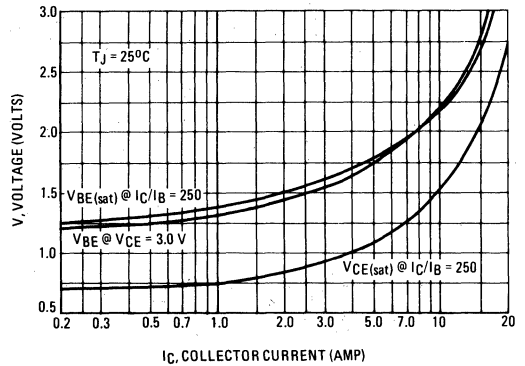
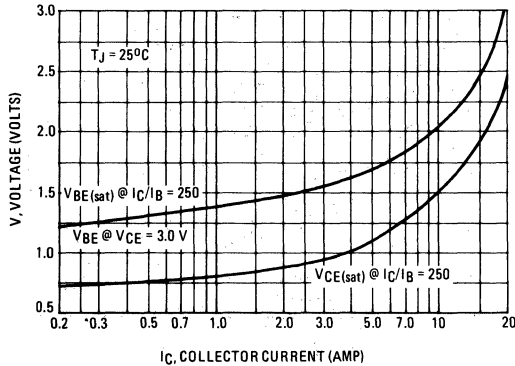


FIGURE 12 - "ON" VOLTAGES



3

2N6282, 2N6283, 2N6284 NPN
2N6285, 2N6286, 2N6287 PNP

NPN
2N6282, 2N6283, 2N6284

PNP
2N6285, 2N6286, 2N6287

FIGURE 13 – TEMPERATURE COEFFICIENTS

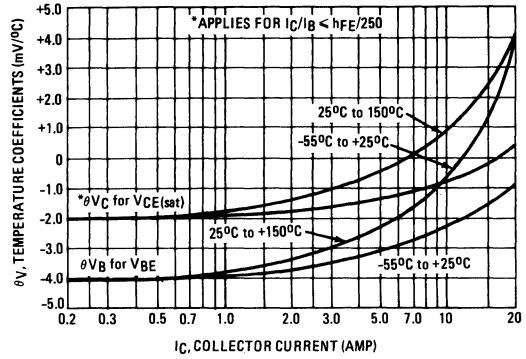
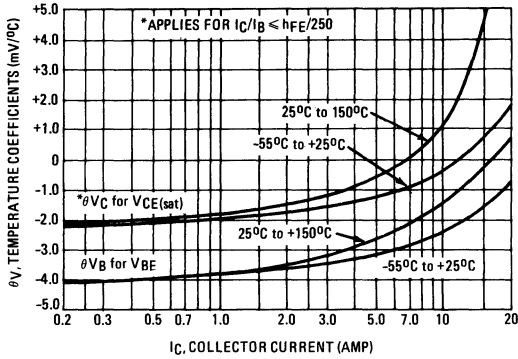


FIGURE 14 – COLLECTOR CUTOFF REGION

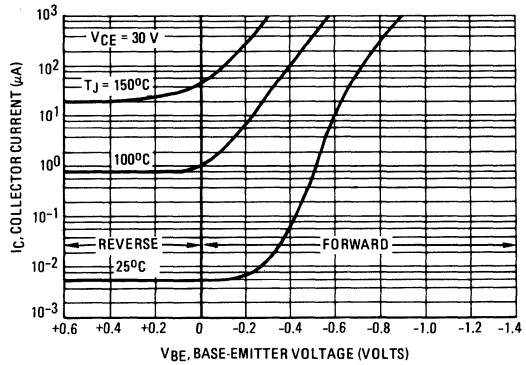
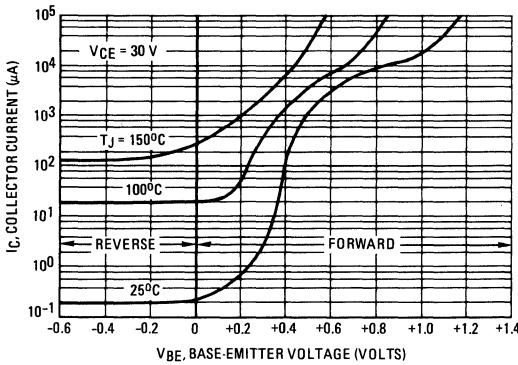
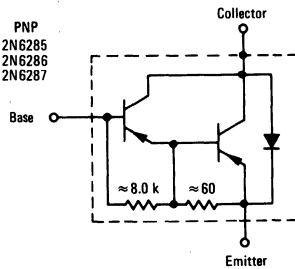
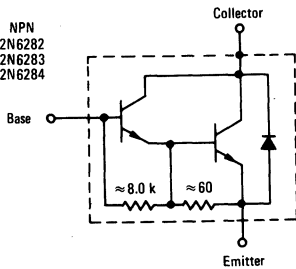


FIGURE 15 – DARLINGTON SCHEMATIC



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
2N6294, 2N6295
PNP
2N6296, 2N6297

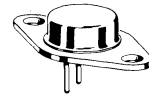
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for general-purpose amplifier, low-frequency switching and hammer driver applications.

- High DC Current Gain – $h_{FE} = 3000$ (Typ) @ $I_C = 2.0$ Adc
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)} = 2.0$ Vdc (Max) @ $I_C = 2.0$ Adc
- Collector-Emitter Sustaining Voltage $V_{CEO(sus)} = 60$ Vdc (Min) – 2N6294, 2N6296
 $= 80$ Vdc (Min) – 2N6295, 2N6297
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

4 AMPERES
DARLINGTON
COMPLEMENTARY SILICON
POWER TRANSISTORS

60, 80 VOLTS
50 WATTS



*** MAXIMUM RATINGS**

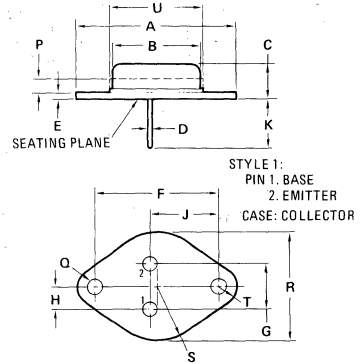
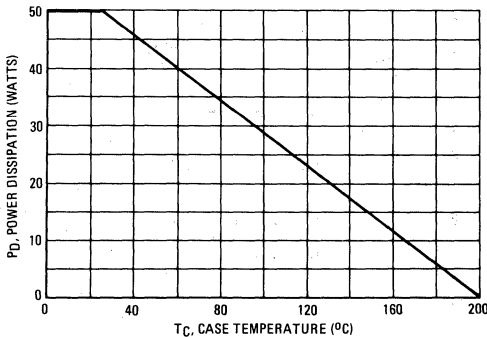
Rating	Symbol	2N6294 2N6296	2N6295 2N6297	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	4.0 8.0		A dc
Base Current	I_B	80		mA dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	50 0.286		Watts W/ $^\circ\text{C}$
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	$^\circ\text{C}/\text{W}$

* Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	—	0.360	—
P	—	1.27	—	0.050
Q	3.61	3.86	0.142	0.152
S	—	8.89	—	0.350
T	—	3.68	—	0.145
U	—	15.75	—	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

2N6294, 2N6295 NPN/2N6296, 2N6297 PNP

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ($I_C = 50 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	60 80	— —	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	— —	0.5 0.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	— — — —	0.5 0.5 5.0 5.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	h_{FE}	750 100	18000 —	—
Collector-Emitter Saturation Voltage ($I_C = 2.0 \text{ Adc}$, $I_B = 8.0 \text{ mAdc}$) ($I_C = 4.0 \text{ Adc}$, $I_B = 40 \text{ mAdc}$)	$V_{CE(sat)}$	— —	2.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 4.0 \text{ Adc}$, $I_B = 40 \text{ mAdc}$)	$V_{BE(sat)}$	—	4.0	Vdc
Base-Emitter On Voltage ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio ($I_C = 1.5 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	$ h_{fe} $	4.0	—	—
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	— —	120 200	pF
Small-Signal Current Gain ($I_C = 1.5 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	300	—	—

*Indicates JEDEC Registered Data

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

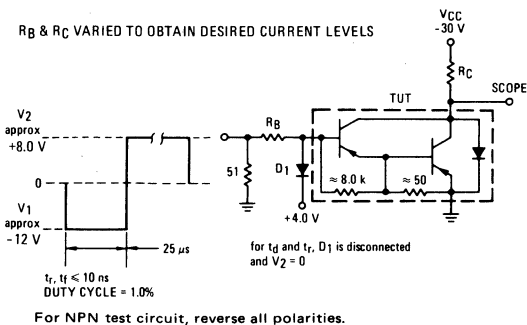
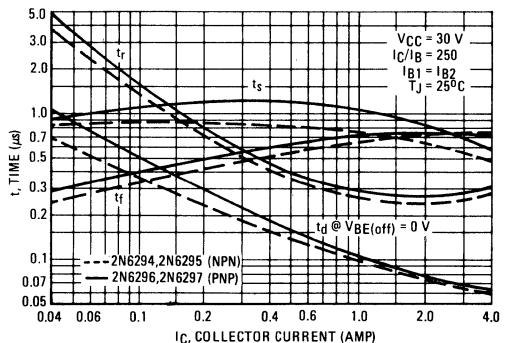


FIGURE 3 – SWITCHING TIMES



2N6294, 2N6295 NPN/2N6296, 2N6297 PNP

FIGURE 4 – THERMAL RESPONSE

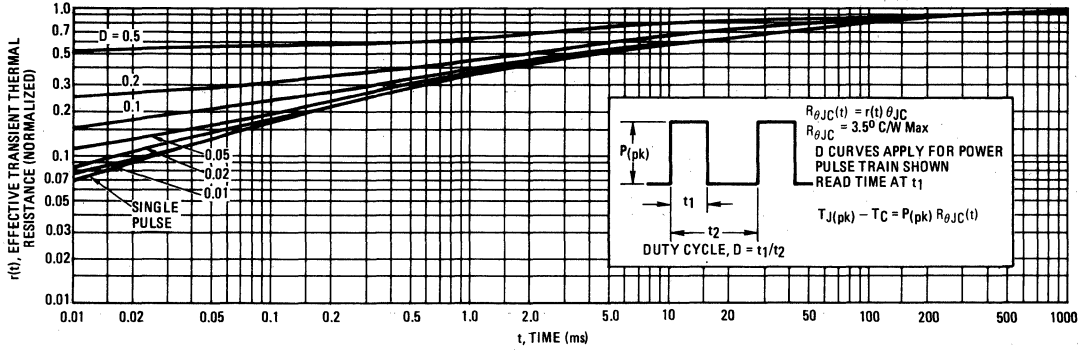
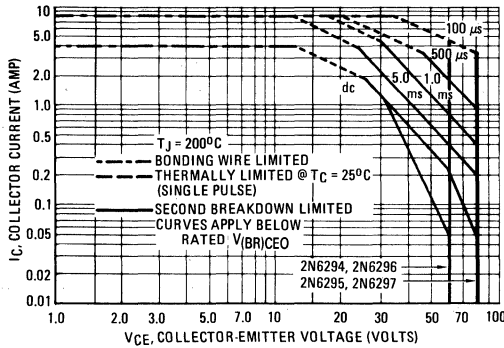


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

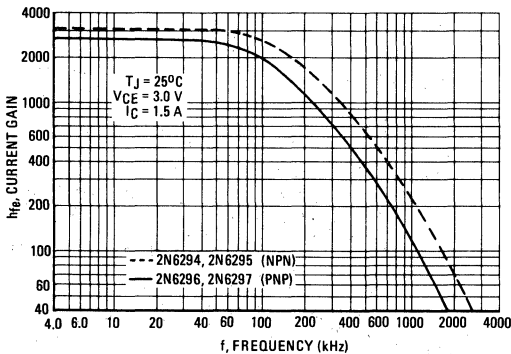
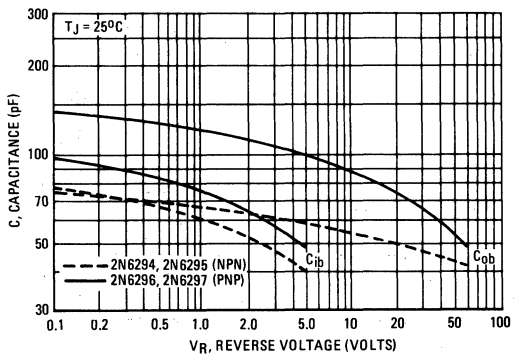


FIGURE 7 – CAPACITANCE



2N6294, 2N6295 NPN/2N6296, 2N6297 PNP

NPN
2N6294, 2N6295

PNP
2N6296, 2N6297

FIGURE 8 – DC CURRENT GAIN

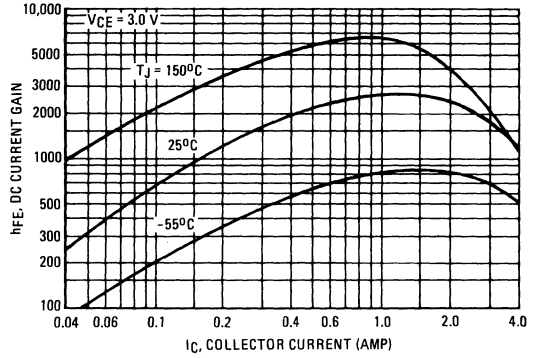
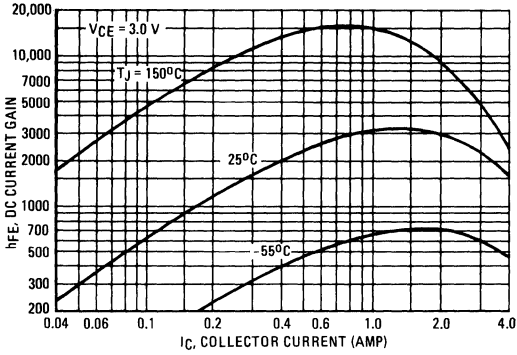


FIGURE 9 – COLLECTOR SATURATION REGION

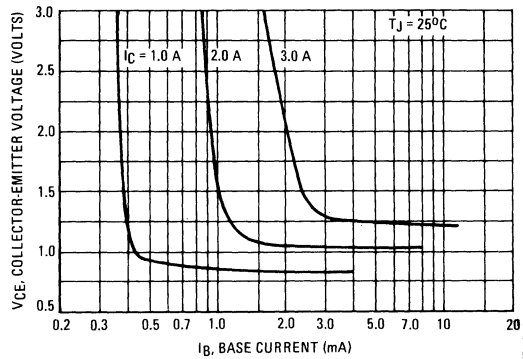
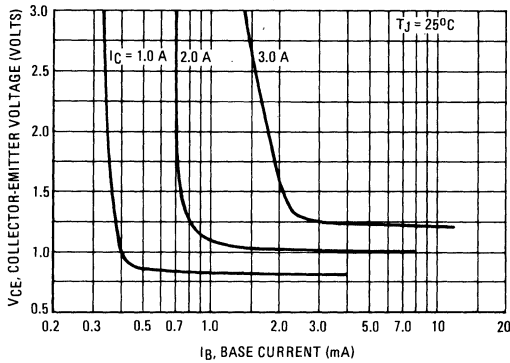
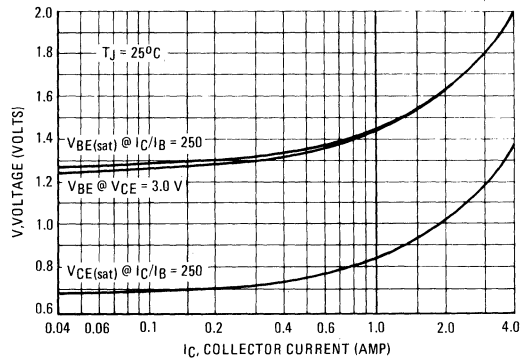
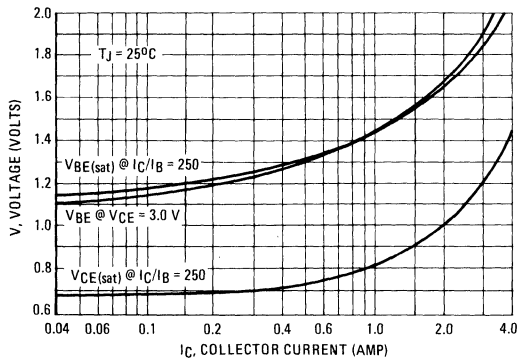


FIGURE 10 – "ON" VOLTAGES



2N6306
2N6307, 2N6308

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

... designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications in associated consumer products.

- High Collector-Base Voltage —
 $V_{CB} = 500 \text{ Vdc} - 2N6306$
 $= 600 \text{ Vdc} - 2N6307$
 $= 700 \text{ Vdc} - 2N6308$
- Excellent DC Current Gain @ $I_C = 3.0 \text{ Adc}$
 $h_{FE} = 15 - 75 - 2N6306, 2N6307$
 $= 12 - 60 - 2N6308$
- Low Collector-Emitter Saturation Voltage @ $I_C = 3.0 \text{ Adc}$
 $V_{CE(sat)} = 0.8 \text{ Vdc (Max)} - 2N6306$
 $= 1.0 \text{ Vdc (Max)} - 2N6307$
 $= 1.5 \text{ Vdc (Max)} - 2N6308$
- Current Gain Bandwidth Product —
 $f_T = 5.0 \text{ MHz (Min)} @ I_C = 0.3 \text{ Adc}$

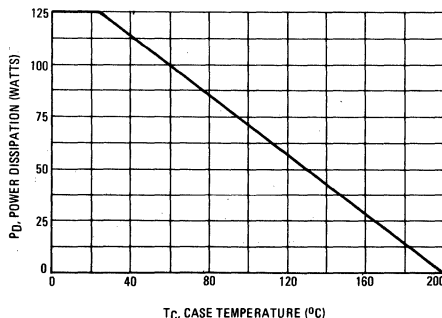
***MAXIMUM RATINGS**

Rating	Symbol	2N6306	2N6307	2N6308	Unit
Collector-Base Voltage	V_{CB}	500	600	700	Vdc
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Emitter-Base Voltage	V_{EB}	← 8.0 →			Vdc
Collector Current — Continuous Peak	I_C	← 8.0 → 16			Adc
Base Current	I_B	← 4.0 →			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 125 → 0.714			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			$^\circ\text{C}$

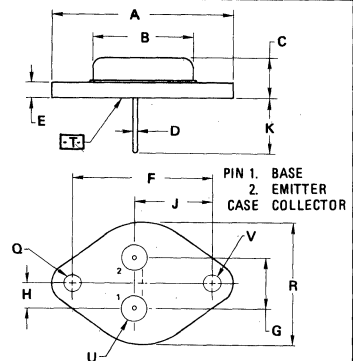
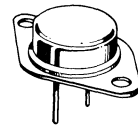
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.4	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING



8 AMPERE POWER TRANSISTORS
NPN SILICON
250-300-350 VOLTS
125 WATTS



NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. \square IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\phi \ 0.13 \ (0.005) \ (M) \ T \ V \ (M)$$

FOR LEADS:

$$\phi \ 0.13 \ (0.005) \ (M) \ T \ V \ (M) \ Q \ (M)$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	18.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

2N6306, 2N6307, 2N6308

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

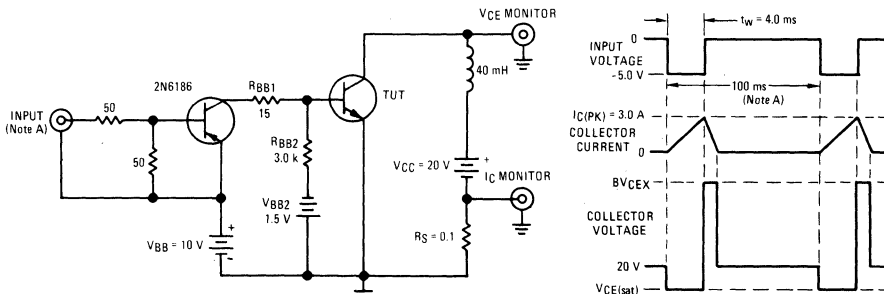
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 100 mA, I _B = 0)	V _{CE(sus)}	250 300 350	—	V _{dc}
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , I _B = 0)	I _{CEO}	—	0.5	mA _{dc}
Collector Cutoff Current (V _{CE} = 500 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 600 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 700 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 450 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C) (V _{CE} = 550 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C) (V _{CE} = 650 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C)	I _{CEX}	— — — — — —	0.5 0.5 0.5 2.5 2.5 2.5	mA _{dc}
Emitter Cutoff Current (V _{BE} = 8.0 Vdc, I _C = 0)	I _{EBO}	—	1.0	mA _{dc}
ON CHARACTERISTICS				
DC Current Gain (1) (I _C = 3.0 A, V _{CE} = 5.0 Vdc) (I _C = 8.0 A, V _{CE} = 5.0 Vdc)	h _{FE}	15 12 4.0 3.0	75 60 — —	—
Collector-Emitter Saturation Voltage (1) (I _C = 3.0 A, I _B = 0.6 A) (I _C = 8.0 A, I _B = 2.0 A) (I _C = 8.0 A, I _B = 2.67 A)	V _{CE(sat)}	— — — —	0.8 1.0 1.5 5.0 5.0	V _{dc}
Base-Emitter Saturation Voltage (1) (I _C = 8.0 A, I _B = 2.0 A) (I _C = 8.0 A, I _B = 2.67 A)	V _{BE(sat)}	— —	2.3 2.5	V _{dc}
Base-Emitter On Voltage (1) (I _C = 3.0 A, V _{CE} = 5.0 Vdc)	V _{BE(on)}	— —	1.3 1.5	V _{dc}
Second Breakdown Energy (Figure 2) (I _{C(PK)} = 3.0 A, L = 40 mH, R _{BE} = 3 kΩ, V _{BB2} = 1.5 Vdc)	E _{s/b}	—	180	mJ
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (2) (I _C = 0.3 A, V _{CE} = 10 Vdc, f _{test} = 1.0 MHz)	f _T	5.0	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	—	250	pF
SWITCHING CHARACTERISTICS				
Rise Time (V _{CC} = 125 Vdc, I _C = 3.0 A, I _B = 0.6 A)	t _r	—	0.6	μs
Storage Time (3) (V _{CC} = 125 Vdc, I _C = 3.0 A, I _{B1} = 0.6 A, I _{B2} = 1.5 A) Pulse Width = 25 μs Pulse Width = 5.0 μs	t _s	— —	1.6 0.8	μs
Fall Time (V _{CC} = 125 Vdc, I _C = 3.0 A, I _{B1} = 0.6 A, I _{B2} = 1.5 A)	t _f	—	0.4	μs

(1) Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle = 2.0%

(2) $f_T = |h_{fe}| \cdot f_{test}$

(3) "On" time is 25 μs. t_s decreases with shorter pulse widths, being approximately 50% of the values shown at a 5.0 μs pulse width.
*Indicates JEDEC Registered Data.

FIGURE 2 – SECOND BREAKDOWN ENERGY TEST CIRCUIT AND WAVEFORMS



Note A: Input pulse width is increased until I_{C(PK)} = 3.0 A.

FIGURE 3 – THERMAL RESPONSE

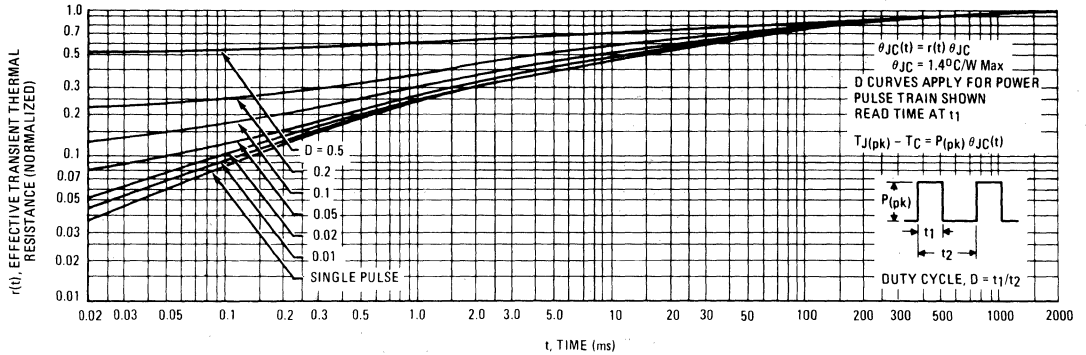
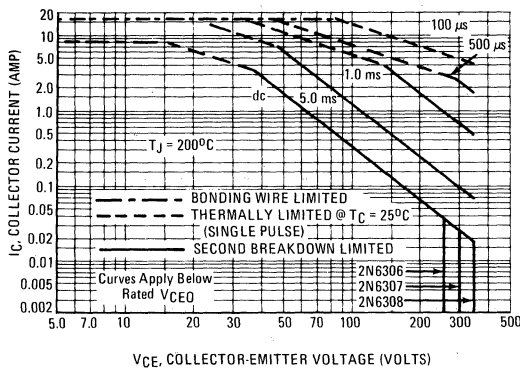


FIGURE 4 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 5 – SWITCHING TIMES TEST CIRCUIT

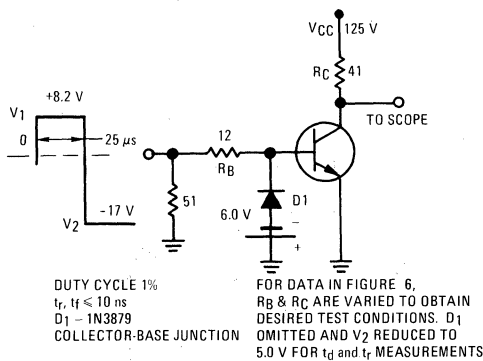


FIGURE 6 – TURN-ON AND TURN-OFF TIMES

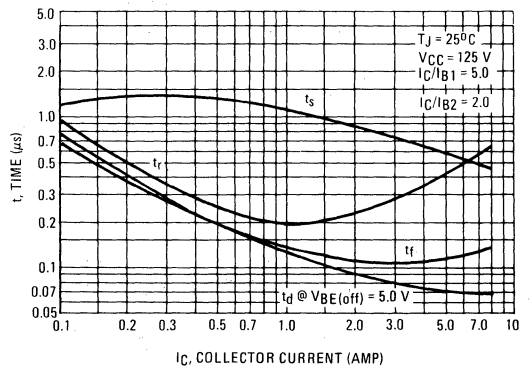


FIGURE 7 – DC CURRENT GAIN

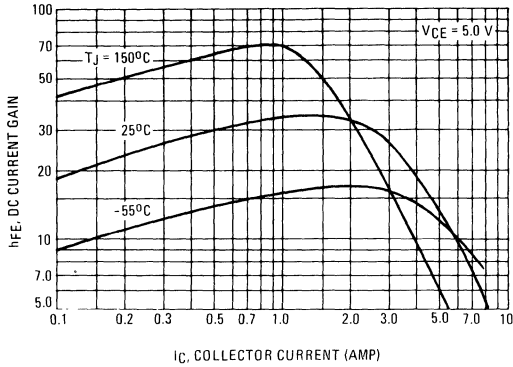


FIGURE 8 – COLLECTOR SATURATION REGION

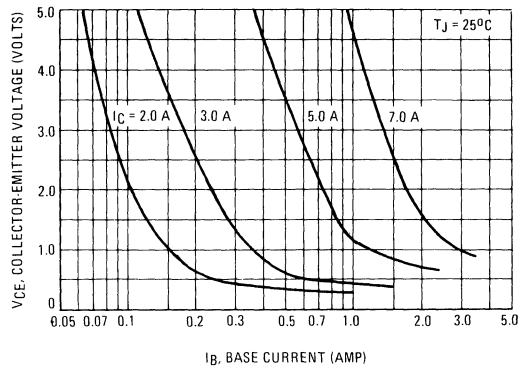


FIGURE 9 – "ON" VOLTAGES

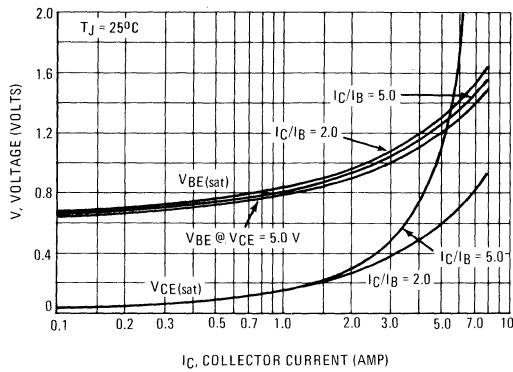


FIGURE 10 – TEMPERATURE COEFFICIENTS

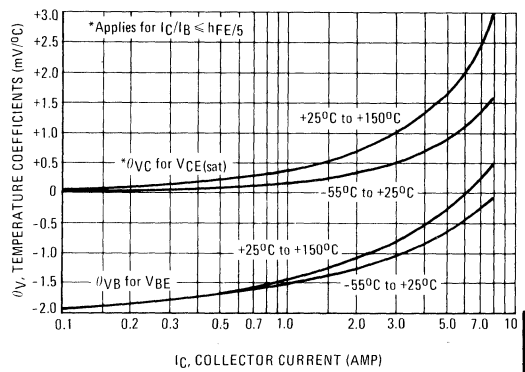


FIGURE 11 – COLLECTOR-CUTOFF REGION

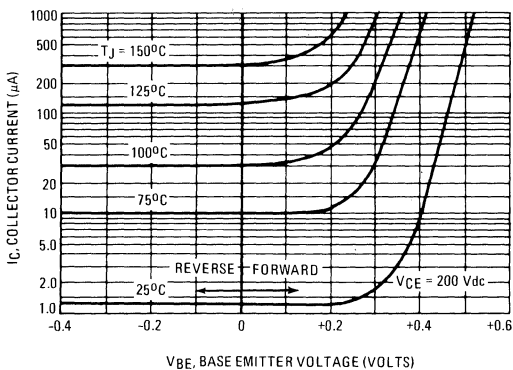
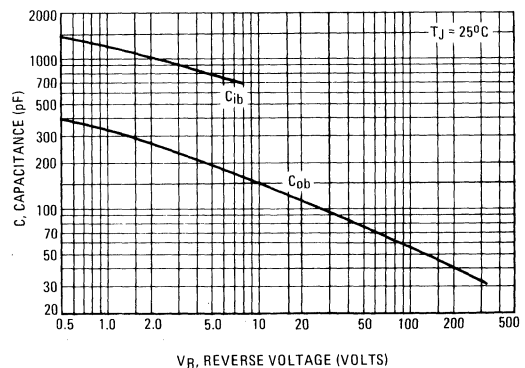


FIGURE 12 – CAPACITANCE



NPN
2N6315, 2N6316
PNP
2N6317, 2N6318

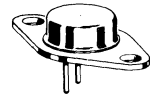
**COMPLEMENTARY SILICON
 MEDIUM-POWER TRANSISTORS**

... designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)} = 1.0 \text{ Vdc (Max) @ } I_C = 4.0 \text{ Adc}$
- Low Leakage Current – $I_{CEX} = 0.25 \text{ mAdc (Max)}$
- Excellent DC Current Gain – $h_{FE} = 20 \text{ (Min) @ } I_C = 2.5 \text{ Adc}$
- High Current Gain – Bandwidth Product – $f_T = 4.0 \text{ MHz @ } I_C = 0.25 \text{ Adc}$

7.0 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS

60-80 VOLTS
90 WATTS



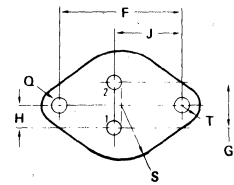
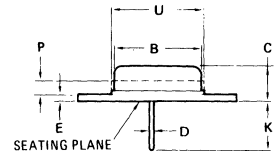
***MAXIMUM RATINGS**

Rating	Symbol	2N6315 2N6317	2N6316 2N6318	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	7.0		Adc
Peak		15		
Base Current	I_B	2.0		Adc
Total Device Dissipation – $T_C = 25^\circ\text{C}$	P_D	90		Watts
Derate above 25°C		0.515		W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.94	$^\circ\text{C/W}$

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE: COLLECTOR

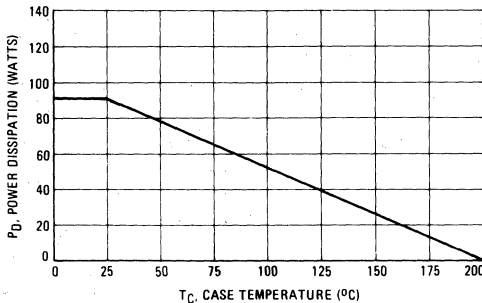
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and Notes Apply.

CASE 80-02
TO-213AA

3

FIGURE 1 – POWER DERATING



Safe Area Limits are indicated by Figure 13.

NPN 2N6315, 2N6316
PNP 2N6317, 2N6318

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 100 \text{ mAdc}$, $I_B = 0$)	2N6315,2N6317 2N6316,2N6318 $V_{CE(sus)}$	60 80	— —	Vdc	
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$)	2N6315,2N6317 2N6316,2N6318 I_{CEO}	— —	0.5 0.5	mAdc	
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	2N6315,2N6317 2N6316,2N6318 2N6315,2N6317 2N6316,2N6318 I_{CEX}	— — — —	0.25 0.25 2.0 2.0	mAdc	
Collector Cutoff Current ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$)	2N6315,2N6317 2N6316,2N6318 I_{CBO}	— —	0.25 0.25	mAdc	
Emitter Cutoff Current ($V_{EB} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	mAdc	
ON CHARACTERISTICS					
DC Current Gain (1) ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 2.5 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 7.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	35 20 4.0	— 100 —	—	
Collector-Emitter Saturation Voltage (1) ($I_C = 4.0 \text{ Adc}$, $I_B = 0.4 \text{ Adc}$) ($I_C = 7.0 \text{ Adc}$, $I_B = 1.75 \text{ Adc}$)	$V_{CE(sat)}$	— —	1.0 2.0	Vdc	
Base-Emitter Saturation Voltage (1) ($I_C = 7.0 \text{ Adc}$, $I_B = 1.75 \text{ Adc}$)	$V_{BE(sat)}$	—	2.5	Vdc	
Base-Emitter On Voltage (1) ($I_C = 2.5 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.5	Vdc	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2) ($I_C = 0.25 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 1.0 \text{ MHz}$)	f_T	4.0	—	MHz	
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	2N6317,2N6318 2N6315,2N6316 C_{ob}	— —	300 200	pF	
Small-Signal Current Gain ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	20	—	—	
SWITCHING CHARACTERISTICS					
Rise Time	(V _{CC} = 30 Vdc, I _C = 2.5 Adc, I _{B1} = I _{B2} = 0.25 Adc)	t _r	—	0.7	μs
Storage Time		t _s	—	1.0	μs
Fall Time		t _f	—	0.8	μs

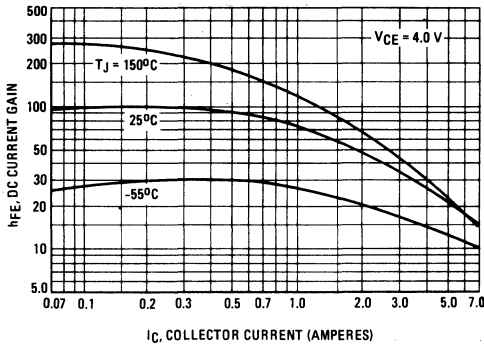
*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$

NPN 2N6315, 2N6316
PNP 2N6317, 2N6318

NPN
2N6315 and 2N6316



PNP
2N6317 and 2N6318

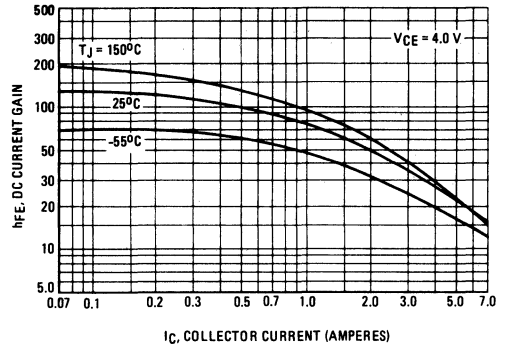


FIGURE 2 - DC CURRENT GAIN

FIGURE 3 - COLLECTOR SATURATION REGION

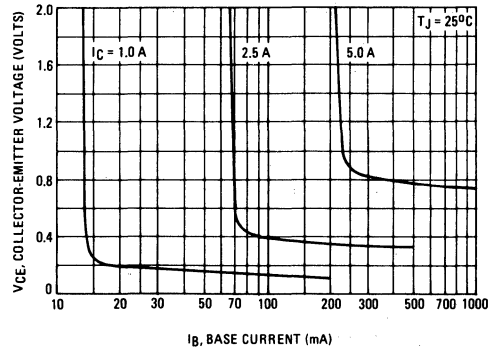
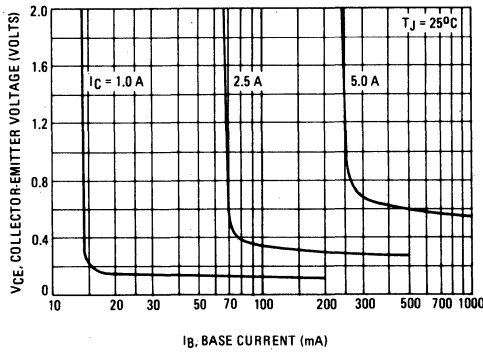
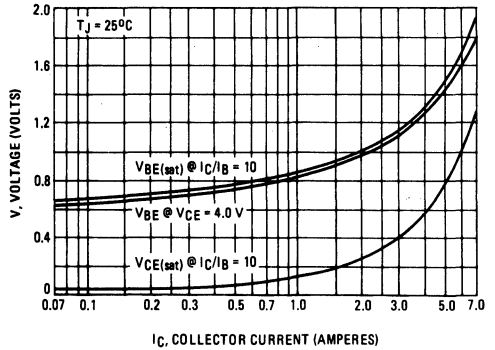
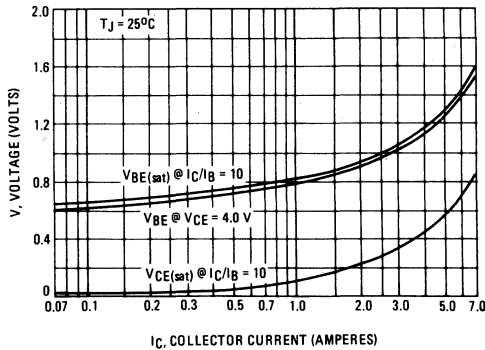


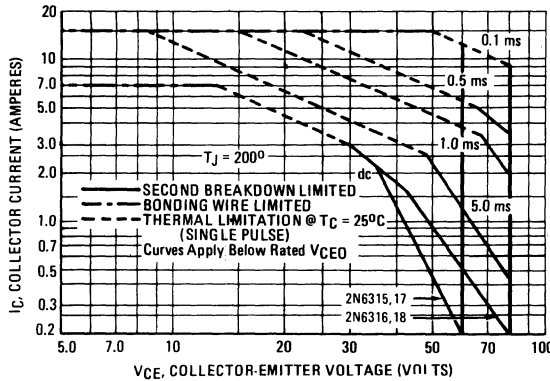
FIGURE 4 - "ON" VOLTAGES



3

NPN 2N6315, 2N6316
PNP 2N6317, 2N6318

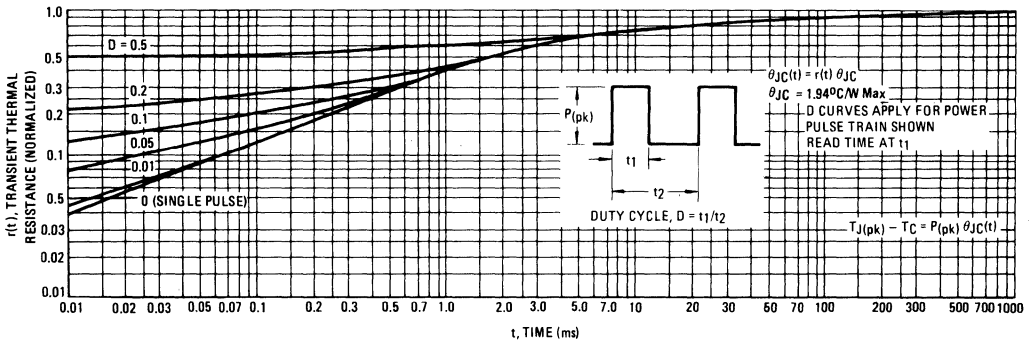
FIGURE 5 - ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 - THERMAL RESPONSE



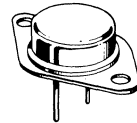
2N6338
thru
2N6341

HIGH-POWER NPN SILICON TRANSISTORS

... designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 100 \text{ Vdc (Min) - 2N6338}$
 $= 120 \text{ Vdc (Min) - 2N6339}$
 $= 140 \text{ Vdc (Min) - 2N6340}$
 $= 150 \text{ Vdc (Min) - 2N6341}$
- High DC Current Gain –
 $h_{FE} = 30-120 @ I_C = 10 \text{ Adc}$
 $= 12 \text{ (Min) } @ I_C = 25 \text{ Adc}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) } @ I_C = 10 \text{ Adc}$
- Fast Switching Times @ $I_C = 10 \text{ Adc}$
 $t_r = 0.3 \mu\text{s (Max)}$
 $t_s = 1.0 \mu\text{s (Max)}$
 $t_f = 0.25 \mu\text{s (Max)}$
- Complement to 2N6436-38

25 AMPERE
POWER TRANSISTORS
NPN SILICON
100, 120, 140, 150 VOLTS
200 WATTS



***MAXIMUM RATINGS**

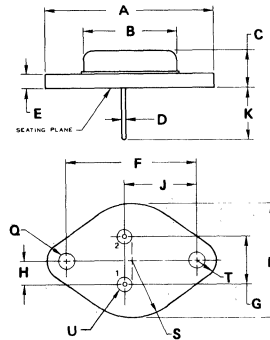
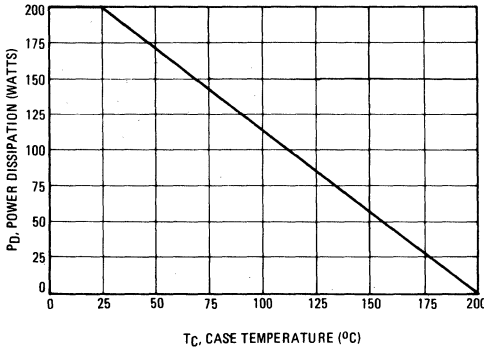
Rating	Symbol	2N6338	2N6339	2N6340	2N6341	Unit
Collector-Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter-Base Voltage	V_{EB}	6.0				Vdc
Collector Current – Continuous	I_C	25				Adc
Peak		50				
Base Current	I_B	10				Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	200				Watts
		1.14				$\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200				$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	$^\circ\text{C}/\text{W}$

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	28.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120

CASE 1-04

NOTES:

1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

2N6338 thru 2N6341

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 50 \text{ mA dc}, I_B = 0$)	2N6338 2N6339 2N6340 2N6341	$V_{CE0(sus)}$	100 120 140 150	— — — —	Vdc
Collector Cutoff Current ($V_{CE} = 50 \text{ Vdc}, I_B = 0$) ($V_{CE} = 60 \text{ Vdc}, I_B = 0$) ($V_{CE} = 70 \text{ Vdc}, I_B = 0$) ($V_{CE} = 75 \text{ Vdc}, I_B = 0$)	2N6338 2N6339 2N6340 2N6341	I_{CEO}	— — — —	50 50 50 50	$\mu\text{A dc}$
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CE0}, V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CE0}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)		I_{CEX}	— —	10 1.0	$\mu\text{A dc}$ mA dc
Collector Cutoff Current ($V_{CB} = \text{Rated } V_{CB}, I_E = 0$)		I_{CBO}	—	10	$\mu\text{A dc}$
Emitter Cutoff Current ($V_{BE} = 6.0 \text{ Vdc}, I_C = 0$)		I_{EBO}	—	100	$\mu\text{A dc}$

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 0.5 \text{ A dc}, V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 10 \text{ A dc}, V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 25 \text{ A dc}, V_{CE} = 2.0 \text{ Vdc}$)	h_{FE}	50 30 12	— 120 —	—
Collector-Emitter Saturation Voltage ($I_C = 10 \text{ A dc}, I_B = 1.0 \text{ A dc}$) ($I_C = 25 \text{ A dc}, I_B = 2.5 \text{ A dc}$)	$V_{CE(sat)}$	— —	1.0 1.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 10 \text{ A dc}, I_B = 1.0 \text{ A dc}$) ($I_C = 25 \text{ A dc}, I_B = 2.5 \text{ A dc}$)	$V_{BE(sat)}$	— —	1.8 2.5	Vdc
Base-Emitter On Voltage ($I_C = 10 \text{ A dc}, V_{CE} = 2.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.8	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product (2) ($I_C = 1.0 \text{ A dc}, V_{CE} = 10 \text{ Vdc}, f_{rest} = 10 \text{ MHz}$)	f_T	40	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz}$)	C_{ob}	—	300	pF

SWITCHING CHARACTERISTICS

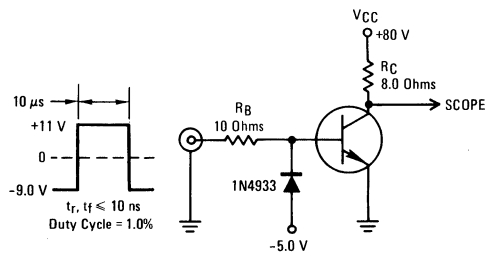
Rise Time ($V_{CC} \approx 80 \text{ Vdc}, I_C = 10 \text{ A dc}, I_{B1} = 1.0 \text{ A dc}, V_{BE(off)} = 6.0 \text{ Vdc}$)	t_r	—	0.3	μs
Storage Time ($V_{CC} \approx 80 \text{ Vdc}, I_C = 10 \text{ A dc}, I_{B1} = I_{B2} = 1.0 \text{ A dc}$)	t_s	—	1.0	μs
Fall Time ($V_{CC} \approx 80 \text{ Vdc}, I_C = 10 \text{ A dc}, I_{B1} = I_{B2} = 1.0 \text{ A dc}$)	t_f	—	0.25	μs

¹Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.

(2) $f_T = h_{FE} \cdot f_{rest}$.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN-ON TIME

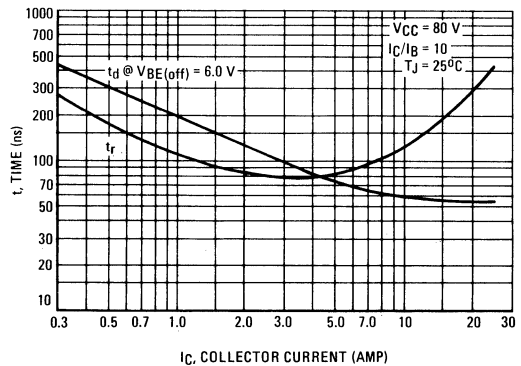


FIGURE 4 – THERMAL RESPONSE

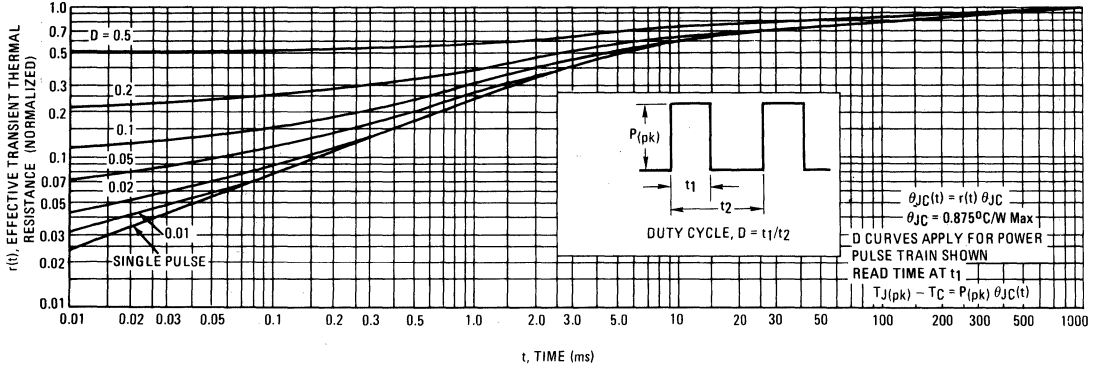
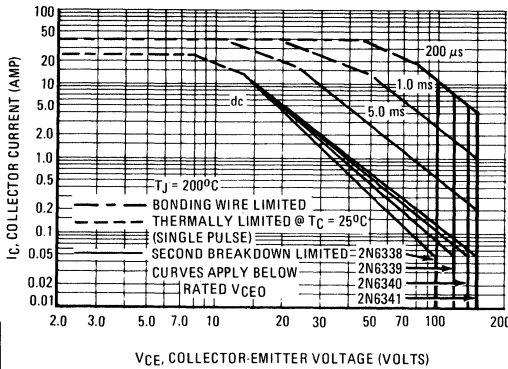


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

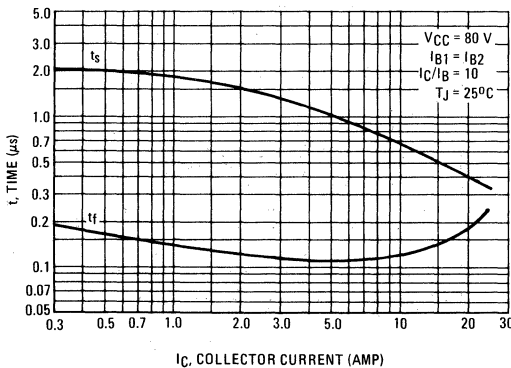
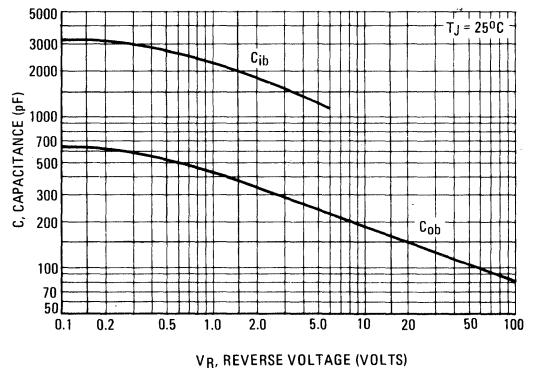


FIGURE 7 – CAPACITANCE



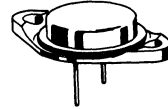
2N6377
thru
2N6379

HIGH-POWER PNP SILICON TRANSISTORS

... designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector Emitter Sustaining Voltage –
 $V_{CE(sus)} = 80 \text{ Vdc (Min) – 2N6377}$
 $= 100 \text{ Vdc (Min) – 2N6378}$
 $= 120 \text{ Vdc (Min) – 2N6379}$
- High DC Current Gain –
 $h_{FE} = 30-120 @ I_C = 20 \text{ Adc}$
 $= 10 \text{ (Min) } @ I_C = 50 \text{ Adc}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) } @ I_C = 20 \text{ Adc}$
- Fast Switching Times @ $I_C = 20 \text{ Adc}$
 $t_r = 0.35 \mu\text{s (Max)}$
 $t_s = 0.8 \mu\text{s (Max)}$
 $t_f = 0.25 \mu\text{s (Max)}$
- Complement to 2N6274-77

50 AMPERE
POWER TRANSISTORS
PNP SILICON
80, 100, 120 VOLTS
250 WATTS



*** MAXIMUM RATINGS**

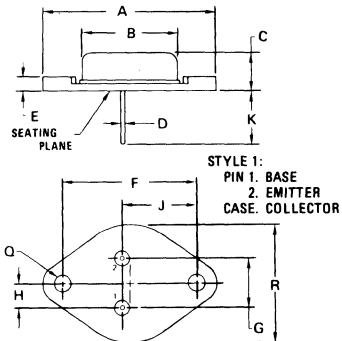
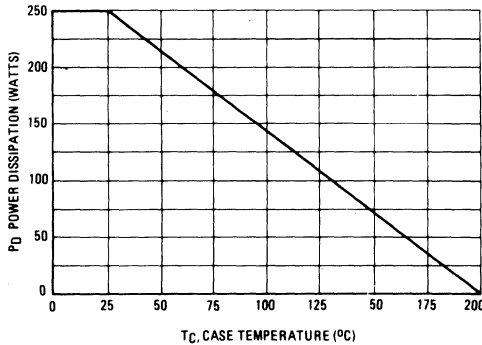
Rating	Symbol	2N6377	2N6378	2N6379	Unit
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Collector-Emitter Voltage	V_{CEO}	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 50 →			A dc
		← 100 →			
Base Current	I_B	← 20 →			A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 250 →			Watts
		← 1.43 →			
Operating and Storage Junction Temperature Range	$T_{J,Tstg}$	← -65 to +200 →			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ\text{C/W}$

* Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

2N6377 thru 2N6379

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
*OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 50 \text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	80 100 120	—	Vdc	
Collector Cutoff Current ($V_{CE} = 50 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 60 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 70 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	— — —	50 50 50	μAdc	
Collector Cutoff Current ($V_{CE} = 90\%$ Rated V_{CB} , $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 90\%$ Rated V_{CB} , $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	— —	10 1.0	μAdc mAdc	
Emitter Cutoff Current ($V_{EB} = 6.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	100	μAdc	
*ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 20 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 50 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	50 30 10	— 120 —	—	
Collector-Emitter Saturation Voltage ($I_C = 20 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$) ($I_C = 50 \text{ Adc}$, $I_B = 10 \text{ Adc}$)	$V_{CE(sat)}$	— —	1.2 3.0	Vdc	
Base-Emitter Saturation Voltage ($I_C = 20 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$) ($I_C = 50 \text{ Adc}$, $I_B = 10 \text{ Adc}$)	$V_{BE(sat)}$	— —	1.8 3.5	Vdc	
DYNAMIC CHARACTERISTICS					
*Current-Gain — Bandwidth Product (2) ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 10 \text{ MHz}$)	f_T	30	—	MHz	
*Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	—	1500	pF	
*SWITCHING CHARACTERISTICS (Figure 2)					
Rise Time	$(V_{CC} = 80 \text{ Vdc}$, $I_C = 20 \text{ Adc}$, $I_{B1} = I_{B2} = 2.0 \text{ Adc}$)	t_r	—	0.35	μs
Storage Time		t_s	—	0.80	μs
Fall Time		t_f	—	0.25	μs

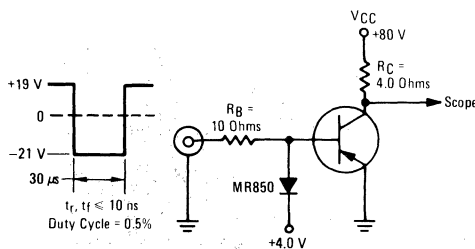
*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$

3

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



Note: For information on Figures 3 & 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 — TURN ON TIME

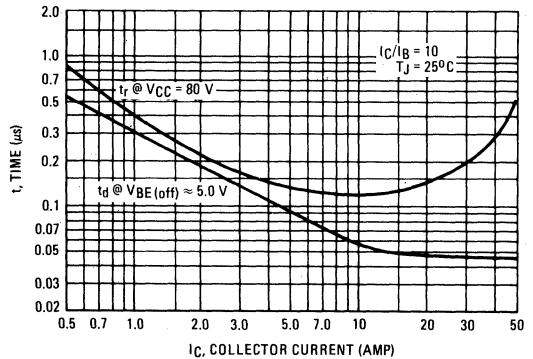


FIGURE 4 – THERMAL RESPONSE

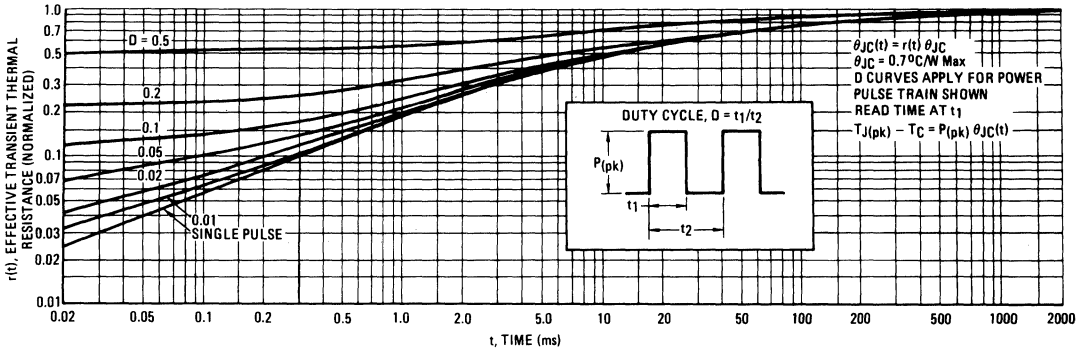
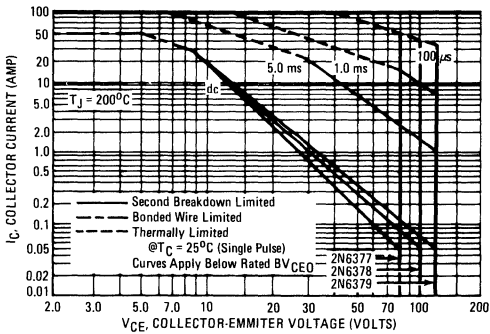


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

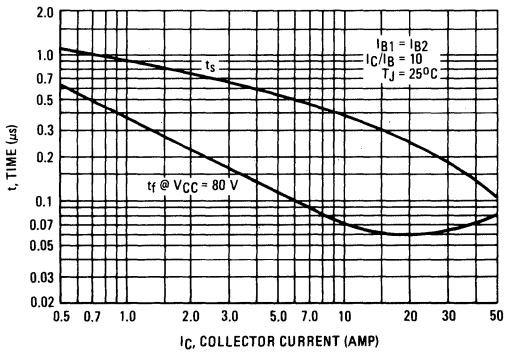


FIGURE 7 – CAPACITANCE

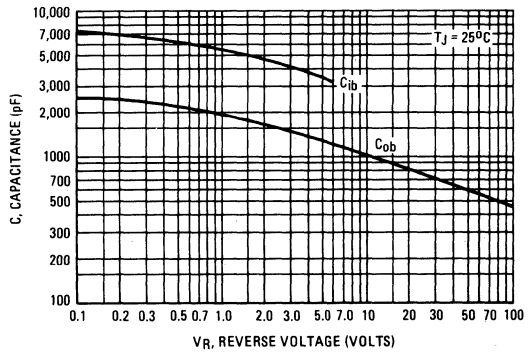


FIGURE 8 – DC CURRENT GAIN

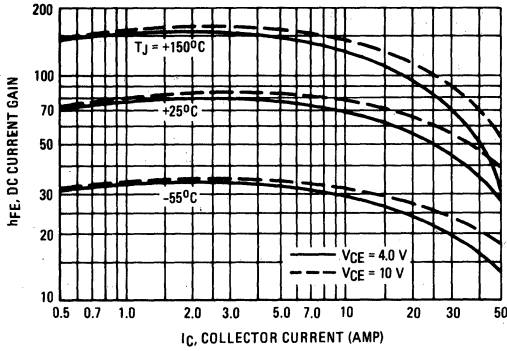


FIGURE 9 – COLLECTOR SATURATION REGION

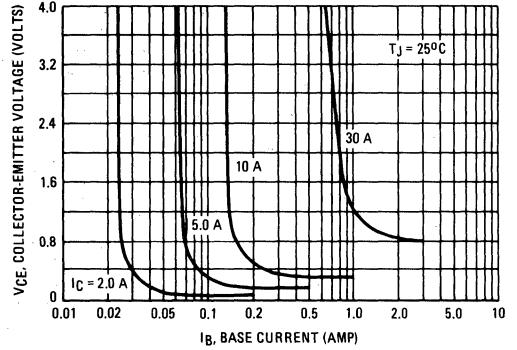


FIGURE 10 – "ON" VOLTAGES

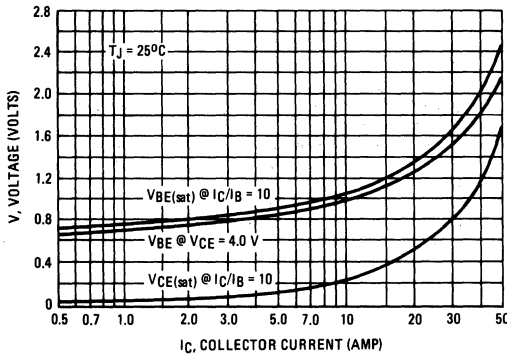


FIGURE 11 – TEMPERATURE COEFFICIENTS

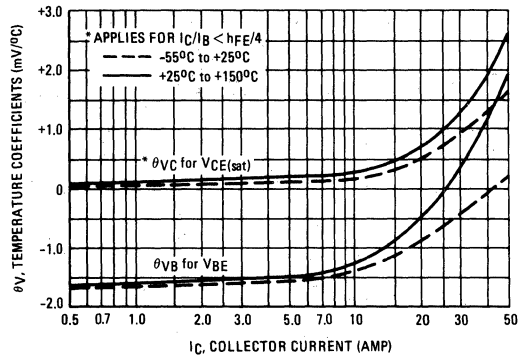


FIGURE 12 – COLLECTOR CUT-OFF REGION

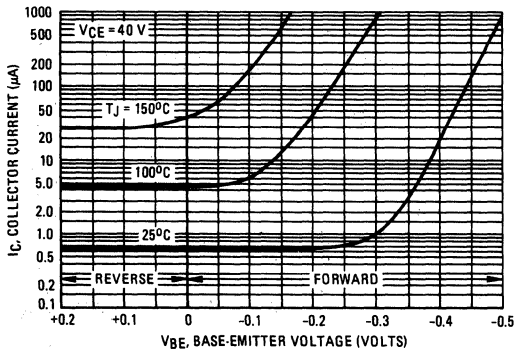
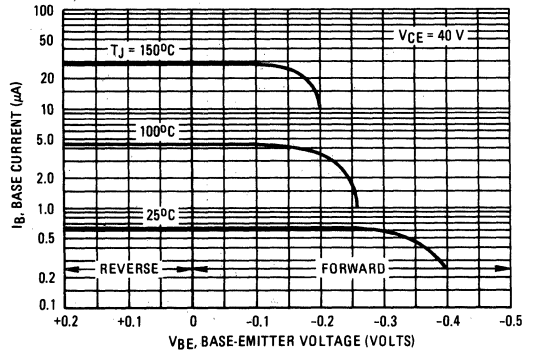


FIGURE 13 – BASE CUTOFF REGION



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
2N6383, 2N6384
2N6385
PNP
2N6648

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

... monolithic complementary silicon Darlington transistors designed for low and medium frequency power applications such as power switching, audio amplifiers, hammer drivers, and shunt and series regulators.

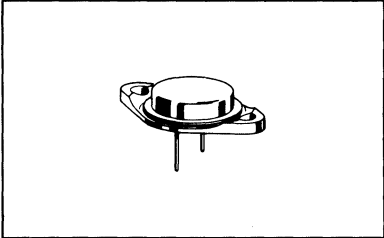
- High Gain Darlington Performance
- True Complementary Specifications

15 AMPERE PEAK
COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

40-60-80 VOLTS
100 WATTS

***MAXIMUM RATINGS**

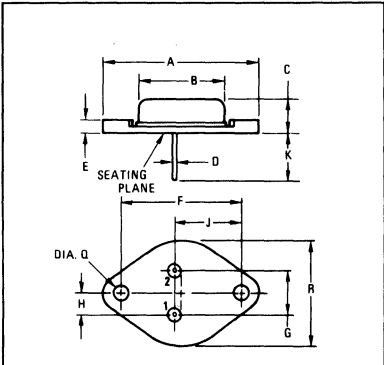
Rating	Symbol	2N6383 2N6648	2N6384	2N6385	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	40	60	80	Vdc
Collector-Emitter Voltage	V_{CEX}	40	60	80	Vdc
Collector-Emitter Voltage	V_{CBO}	40	60	80	Vdc
Emitter Base Voltage	V_{EBO}	5.0			Vdc
Collector Current – Continuous	I_C	10			Adc
Peak (1)**	I_{CM}	15			Adc
Base Current – Continuous	I_B	0.25			Adc
Total Power Dissipation @ $T_C = 25^\circ C$ (2) Derate above $25^\circ C$	P_D	100			Watts
		0.571			W/ $^\circ C$
Operating and Storage Junction Temperature Range (2)	T_J, T_{stg}	-65 to +200			$^\circ C$



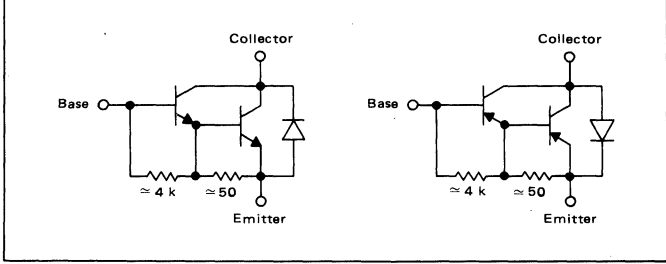
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes: 1/32" from Case for 5 Seconds	T_L	235	$^\circ C$

* Indicates JEDEC Registered Data.
 **Not JEDEC Registered.
 (1) Pulse Width = 50 ms, Duty Cycle \leq 10%.
 (2) Exceeds JEDEC Registration for 2N6648.
 JEDEC Registration gives $P_D = 70 W, T_J = 150^\circ C$.



STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	-	3.43	-	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.84	17.15	0.665	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	-	1.050

Collector connected to case.
 CASE 11 01
 (TO-3)

3

2N6383, 2N6384, 2N6385, NPN, 2N6648, PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (1) (I _C = 200 mAdc, I _B = 0)	2N6383, 2N6648 2N6384 2N6385	V _{CEO(sus)}	40 60 80	— — —	Vdc
Collector Cutoff Current (V _{CE} = Rated Value)		I _{CEO}	—	1.0	mAdc
*Collector Cutoff Current (V _{CE} = Rated V _{CEO(sus)} Value, V _{BE(off)} = 1.5 Vdc) (V _{CE} = Rated V _{CEO(sus)} Value, V _{BE(off)} = 1.5 Vdc, T _C = 150°C)		I _{CEV}	— —	0.3 3.0	mAdc
*Emitter Cutoff Current (V _{EB} = 5.0 Vdc, I _C = 0)		I _{EBO}	—	10	mAdc
Collector-Emitter Sustaining Voltage (1) (R _{BE} = 100 Ω, I _C = 200 mA)	2N6383, 2N6648 2N6384 2N6385	V _{CER(sus)}	40 60 80	— — —	Vdc
Collector-Emitter Sustaining Voltage (1) (V _{BE(off)} = 1.5 V, I _C = 200 mA)	2N6383, 2N6648 2N6384 2N6385	V _{CEV(sus)}	40 60 80	— — —	Vdc

ON CHARACTERISTICS (1)

*DC Current Gain (I _C = 5.0 Adc, V _{CE} = 3.0 Vdc) (I _C = 10 Adc, V _{CE} = 3.0 Vdc)		h _{FE}	1000 100	20,000 —	—
*Collector-Emitter Saturation Voltage (I _C = 5.0 Adc, I _B = 0.01 Adc) (I _C = 10 Adc, I _B = 0.1 Adc)		V _{CE(sat)}	— —	2.0 3.0	Vdc
*Base-Emitter On Voltage (I _C = 5.0 Adc, V _{CE} = 3.0 Vdc) (I _C = 10 Adc, V _{CE} = 3.0 Vdc)		V _{BE(on)}	— —	2.8 4.5	Vdc
Diode Forward Voltage (I _F = 10 Adc)		V _F	—	4.0	Vdc

*DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1.0 MHz)		C _{ob}	—	200	pF
*Magnitude of Common-Emitter Small-Signal Short-Circuit Current Transfer Ratio (I _C = 1.0 Adc, V _{CE} = 5.0 Vdc, f = 1.0 MHz)		h _{fe}	20	—	—
Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I _C = 1.0 Adc, V _{CE} = 5.0 Vdc, f = 1.0 kHz)		h _{fe}	1000	—	—

SECOND BREAKDOWN

Second Breakdown Collector Current with Base-Forward Biased	I _{S/B}	See Figures 8 and 9		
Second Breakdown Energy with Base Reverse-Biased (L = 12 mH, R _{BE} = 100 Ω, V _{BE(off)} = 1.5 Vdc, I _C = 4.5 Adc)	E _{S/B}	120	—	mJ

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

* Indicates JEDEC Registered Data.

FIGURE 1 - DC CURRENT GAIN

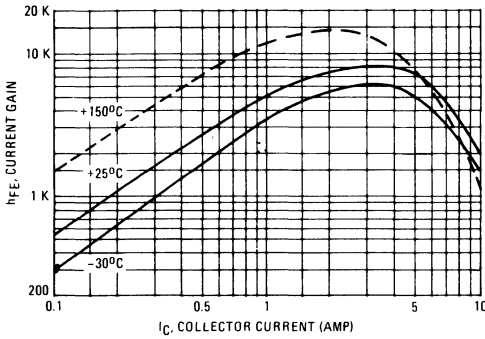


FIGURE 2 - COLLECTOR SATURATION REGION

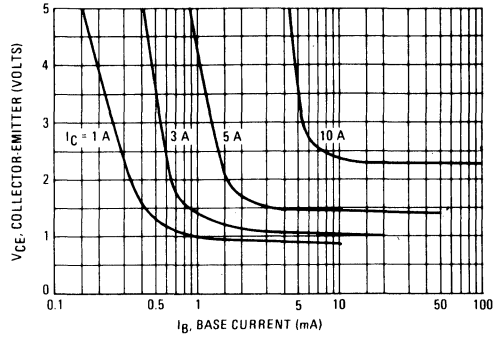


FIGURE 3 - COLLECTOR-EMITTER SATURATION VOLTAGE

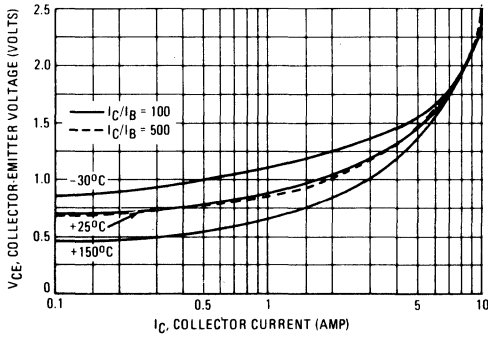


FIGURE 4 - BASE-EMITTER VOLTAGE

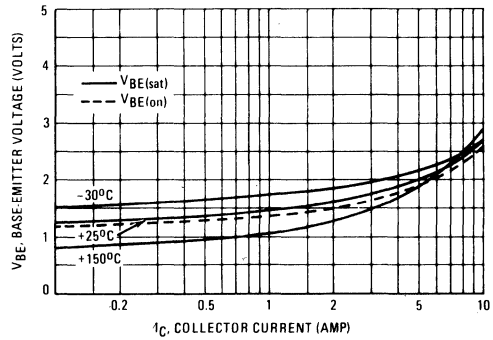


FIGURE 5 - SWITCHING TIME TEST CIRCUIT (Shown for NPN)

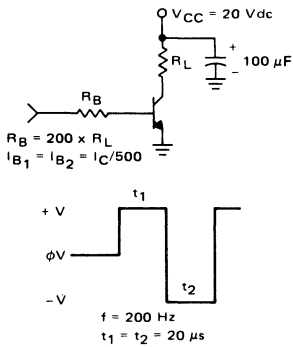


FIGURE 6 - SWITCHING TIMES

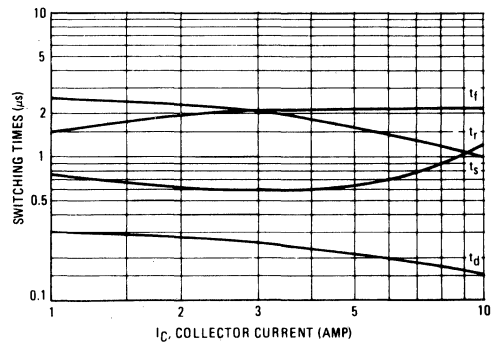
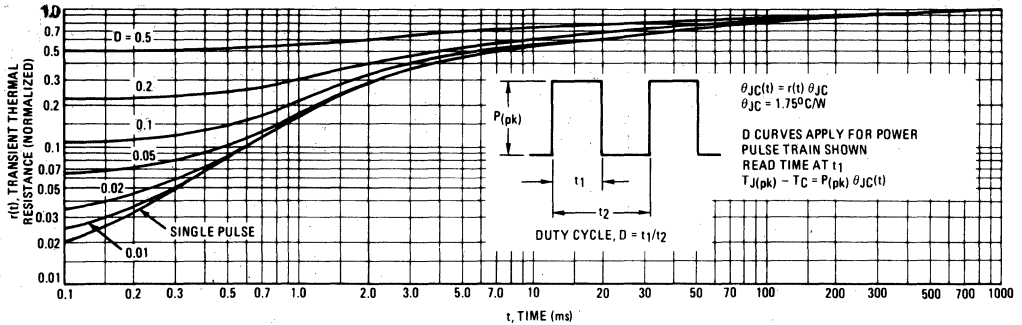


FIGURE 7 - THERMAL RESPONSE



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 8 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated

for temperature.

$T_J(pk)$ may be calculated from the data in Figure 7. At high case temperatures, see Figure 9, thermal limitations will reduce the current that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do derate the same as thermal limitations. Allowable current at the voltages shown on Figure 8 may be found at any case temperature by derating linearly to 200°C .

FORWARD BIASED SAFE OPERATING AREA

FIGURE 8 - $T_C = 25^\circ\text{C}$

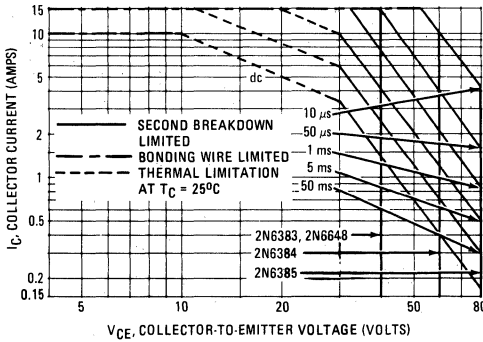


FIGURE 9 - $T_C = 100^\circ\text{C}$

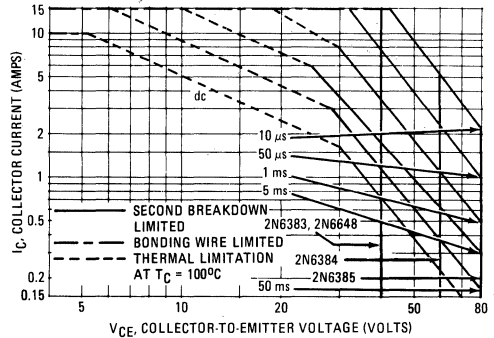
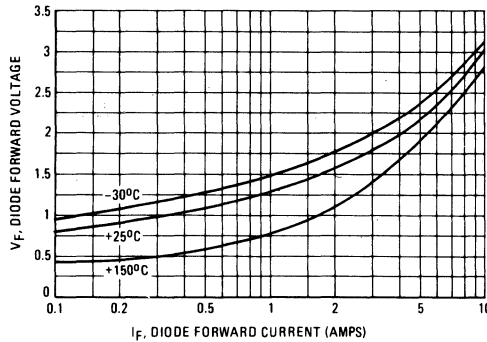


FIGURE 10 - CE DIODE CHARACTERISTICS



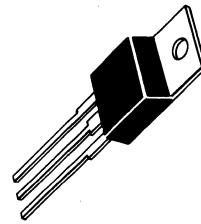
2N6386
2N6387
2N6388

**PLASTIC MEDIUM-POWER
 SILICON TRANSISTORS**

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
 $h_{FE} = 2500$ (Typ) @ $I_C = 4.0$ Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc
 $V_{CE(sus)} = 40$ Vdc (Min) – 2N6386
 $= 60$ Vdc (Min) – 2N6387
 $= 80$ Vdc (Min) – 2N6388
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 2.0$ Vdc (Max) @ $I_C = 3.0$ Adc – 2N6386
 $= 2.0$ Vdc (Max) @ $I_C = 5.0$ Adc – 2N6387, 2N6388
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON
8 AND 10 AMPERE
NPN SILICON
POWER TRANSISTORS
40-60-80 VOLTS
65 WATTS

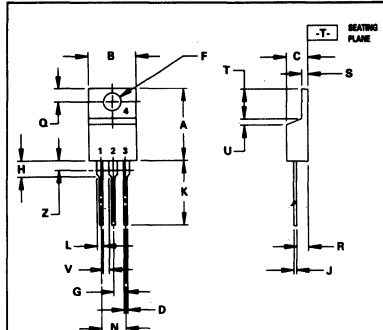
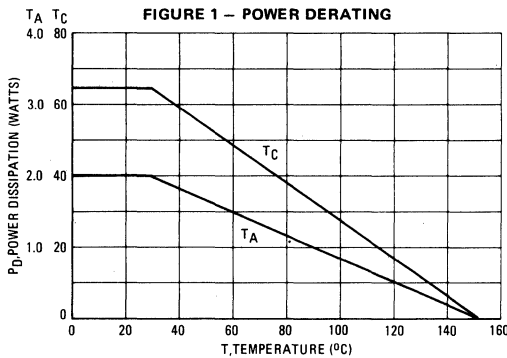


***MAXIMUM RATINGS**

Rating	Symbol	2N6386	2N6387	2N6388	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	8.0 15	10 15	10 15	Adc
Base Current	I_B	250			mAdc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	65			Watts $W/^\circ C$
Total Power Dissipation @ $T_A = 25^\circ C$ Derate above $25^\circ C$	P_D	2.0 0.016			Watts $W/^\circ C$
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +150			$^\circ C$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ C/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$



NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.29	0.380	0.405
C	4.67	4.82	0.180	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.065
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.065
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
 PIN 1: BASE
 2: COLLECTOR
 3: EMITTER
 4: COLLECTOR

CASE 221A-04
TO-220AB

2N6386 2N6387 2N6388 NPN

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	40 60 80	—	Vdc
Collector Cutoff Current ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 60 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 80 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	— — —	1.0 1.0 1.0	mA
Collector Cutoff Current ($V_{CE} = 40 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 60 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 40 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$) ($V_{CE} = 60 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$)	I_{CEX}	— — — — — —	300 300 300 3.0 3.0 3.0	μA mA
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	5.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 3.0 \text{ A}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 5.0 \text{ A}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 8.0 \text{ A}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 10 \text{ A}$, $V_{CE} = 3.0 \text{ Vdc}$)	h_{FE}	1000 1000 100 100	20000 20000 — —	—
Collector-Emitter Saturation Voltage ($I_C = 3.0 \text{ A}$, $I_B = 0.006 \text{ A}$) ($I_C = 5.0 \text{ A}$, $I_B = 0.01 \text{ A}$) ($I_C = 8.0 \text{ A}$, $I_B = 0.08 \text{ A}$) ($I_C = 10 \text{ A}$, $I_B = 0.1 \text{ A}$)	$V_{CE(sat)}$	— — — —	2.0 2.0 3.0 3.0	Vdc
Base-Emitter On Voltage ($I_C = 3.0 \text{ A}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 5.0 \text{ A}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 8.0 \text{ A}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 10 \text{ A}$, $V_{CE} = 3.0 \text{ Vdc}$)	$V_{BE(on)}$	— — — —	2.8 2.8 4.5 4.5	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain ($I_C = 1.0 \text{ A}$, $V_{CE} = 5.0 \text{ Vdc}$, $f_{test} = 1.0 \text{ MHz}$)	$ h_{fe} $	20	—	—
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	C_{ob}	—	200	pF
Small-Signal Current Gain ($I_C = 1.0 \text{ A}$, $V_{CE} = 5.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	1000	—	—

* Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT

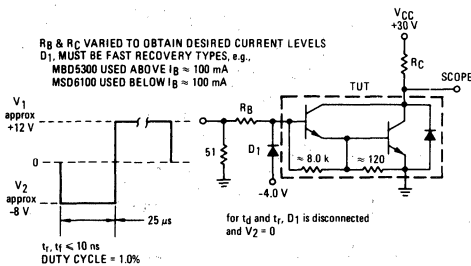


FIGURE 3 — SWITCHING TIMES

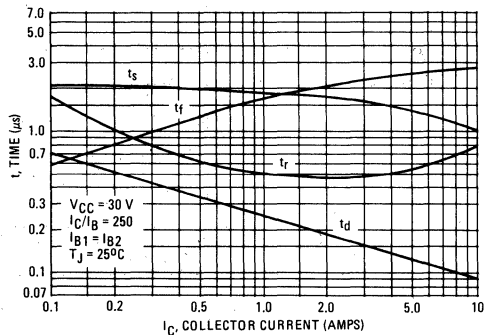


FIGURE 4 – THERMAL RESPONSE

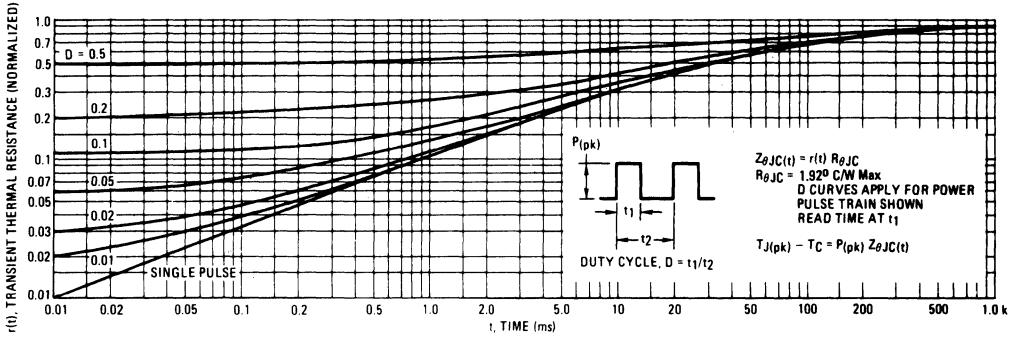
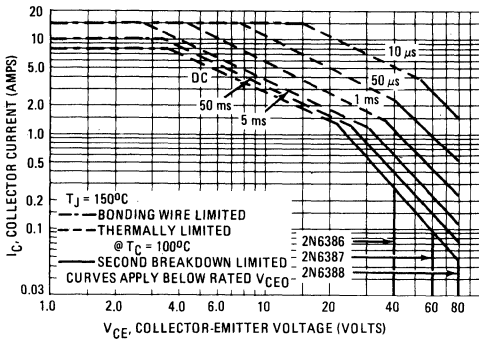


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

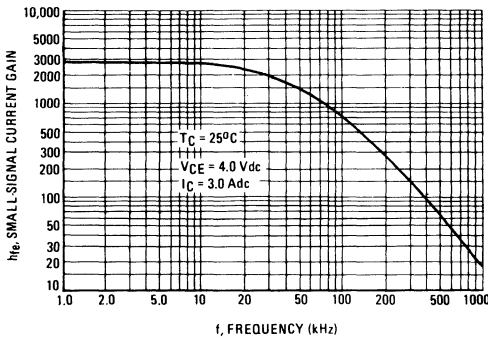


FIGURE 7 – CAPACITANCE

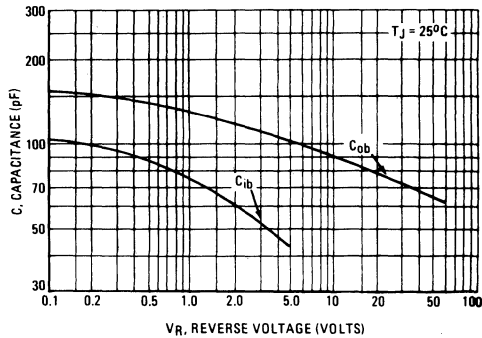


FIGURE 8 – DC CURRENT GAIN

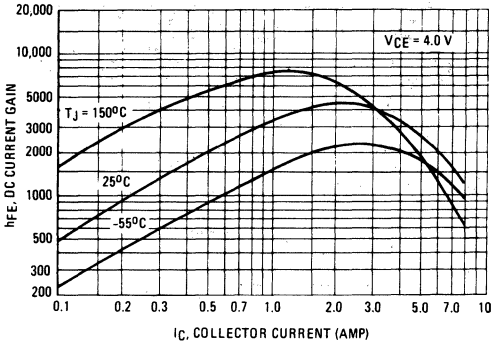


FIGURE 9 – COLLECTOR SATURATION REGION

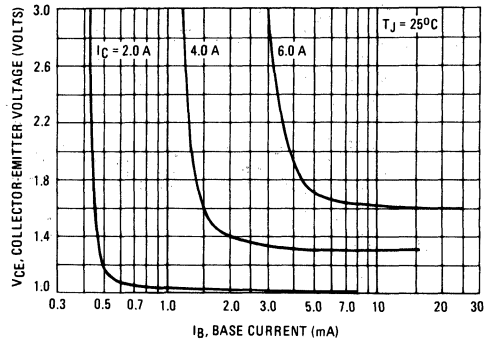


FIGURE 10 – "ON" VOLTAGES

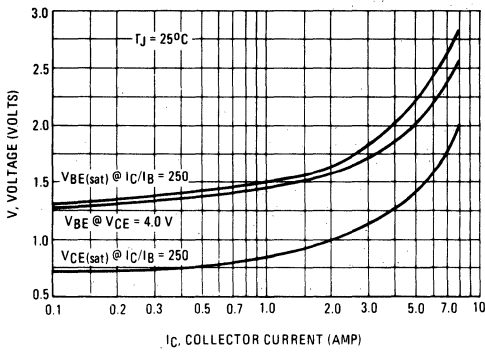


FIGURE 11 – TEMPERATURE COEFFICIENTS

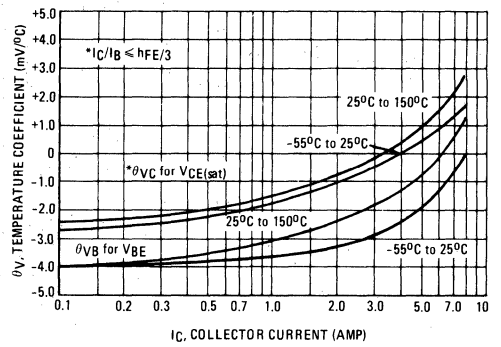


FIGURE 12 – COLLECTOR CUT-OFF REGION

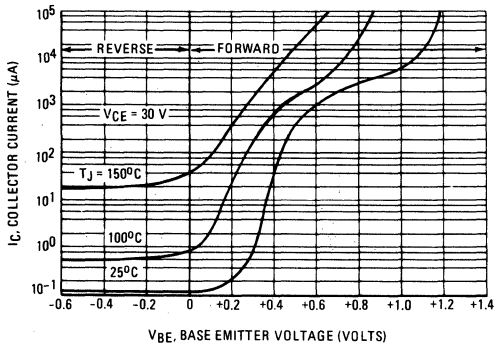
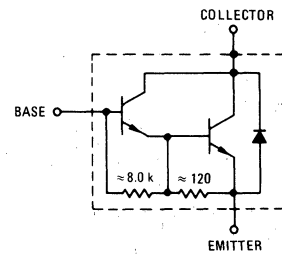


FIGURE 13 – DARLINGTON SCHEMATIC



3

2N6420 thru 2N6422
See Page 3-20

2N6436
2N6437, 2N6438

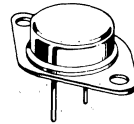
HIGH-POWER PNP SILICON TRANSISTORS

...designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector-Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 80 \text{ Vdc (Min) – 2N6436}$
 $= 100 \text{ Vdc (Min) – 2N6437}$
 $= 120 \text{ Vdc (Min) – 2N6438}$
- High DC Current Gain –
 $h_{FE} = 20-80 @ I_C = 10 \text{ Adc}$
 $= 12 \text{ (Min) } @ I_C = 25 \text{ Adc}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) } @ I_C = 10 \text{ Adc}$
- Fast Switching Times @ $I_C = 10 \text{ Adc}$
 $t_r = 0.3 \mu\text{s (Max)}$
 $t_s = 1.0 \mu\text{s (Max)}$
 $t_f = 0.25 \mu\text{s (Max)}$
- Complement to NPN 2N6338 thru 2N6341

25 AMPERE
POWER TRANSISTORS
PNP SILICON

80, 100, 120 VOLTS
200 WATTS



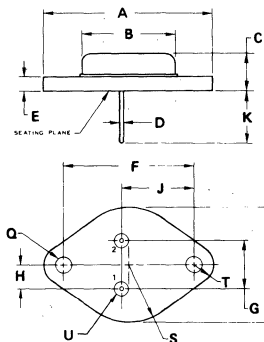
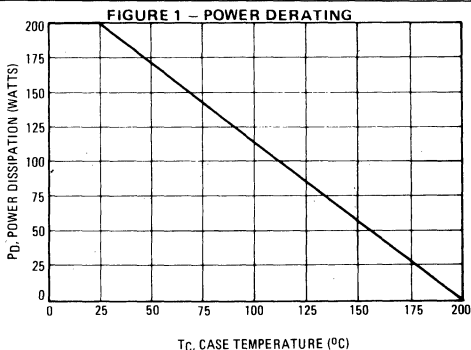
***MAXIMUM RATINGS**

Rating	Symbol	2N6436	2N6437	2N6438	Unit
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Collector-Emitter Voltage	V_{CEO}	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current – Continuous	I_C	← 25 →			A dc
Peak		← 50 →			
Base Current	I_B	← 10 →			A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	← 200 →			Watts
Derate above 25°C		← 1.14 →			W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data.



STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120

CASE1-04

NOTES:
 1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

2N6436, 2N6437, 2N6438

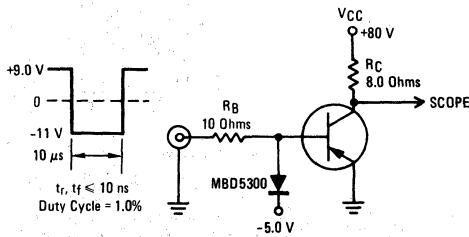
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I _C = 50 mA _{dc} , I _B = 0)	2N6436 2N6437 2N6438	V _{CEO(sus)}	80 100 120	— — —	V _{dc}
Collector Cutoff Current (V _{CE} = 40 V _{dc} , I _B = 0) (V _{CE} = 50 V _{dc} , I _B = 0) (V _{CE} = 60 V _{dc} , I _B = 0)	2N6436 2N6437 2N6438	I _{CEO}	— — —	50 50 50	μA _{dc}
Collector Cutoff Current (V _{CE} = 90 V _{dc} , V _{BE(off)} = -1.5 V _{dc}) (V _{CE} = 110 V _{dc} , V _{BE(off)} = -1.5 V _{dc}) (V _{CE} = 130 V _{dc} , V _{BE(off)} = -1.5 V _{dc}) (V _{CE} = 80 V _{dc} , V _{BE(off)} = -1.5 V _{dc} , T _C = 150°C) (V _{CE} = 100 V _{dc} , V _{BE(off)} = -1.5 V _{dc} , T _C = 150°C) (V _{CE} = 120 V _{dc} , V _{BE(off)} = -1.5 V _{dc} , T _C = 150°C)	2N6436 2N6437 2N6438 2N6436 2N6437 2N6438	I _{CEX}	— — — — — —	10 10 10 1.0 1.0 1.0	μA _{dc} mA _{dc}
Collector Cutoff Current (V _{CB} = 100 V _{dc} , I _E = 0) (V _{CB} = 120 V _{dc} , I _E = 0) (V _{CB} = 140 V _{dc} , I _E = 0)	2N6436 2N6437 2N6438	I _{CBO}	— — —	10 10 10	μA _{dc}
Emitter Cutoff Current (V _{EB} = 6.0 V _{dc} , I _C = 0)		I _{EBO}	—	100	μA _{dc}
ON CHARACTERISTICS					
DC Current Gain (1) (I _C = 0.5 A _{dc} , V _{CE} = 2.0 V _{dc}) (I _C = 10 A _{dc} , V _{CE} = 2.0 V _{dc}) (I _C = 25 A _{dc} , V _{CE} = 2.0 V _{dc})		h _{FE}	30 20 12	— 120 —	—
Collector-Emitter Saturation Voltage (1) (I _C = 10 A _{dc} , I _B = 1.0 A _{dc}) (I _C = 25 A _{dc} , I _B = 2.5 A _{dc})		V _{CE(sat)}	— —	1.0 1.8	V _{dc}
Base-Emitter Saturation Voltage (1) (I _C = 10 A _{dc} , I _B = 1.0 A _{dc}) (I _C = 25 A _{dc} , I _B = 2.5 A _{dc})		V _{BE(sat)}	— —	1.8 2.5	V _{dc}
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I _C = 1.0 A _{dc} , V _{CE} = 10 V _{dc} , f _{test} = 10 MHz)		f _T	40	—	MHz
Output Capacitance (V _{CE} = 10 V _{dc} , I _E = 0, f = 100 kHz)		C _{ob}	—	700	pF
SWITCHING CHARACTERISTICS					
Rise Time (V _{CC} = 80 V _{dc} , I _C = 10 A, V _{BE(off)} = 6.0 V _{dc} , I _{B1} = 1.0 A _{dc})		t _r	—	0.3	μs
Storage (V _{CC} = 80 V _{dc} , I _C = 10 A, V _{BE(off)} = 6.0 V _{dc} , I _{B1} = I _{B2} = 1.0 A _{dc})		t _s	—	1.0	μs
Fall Time (V _{CC} = 80 V _{dc} , I _C = 10 A, V _{BE(off)} = 6.0 V _{dc} , I _{B1} = I _{B2} = 1.0 A _{dc})		t _f	—	0.25	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN-ON TIME

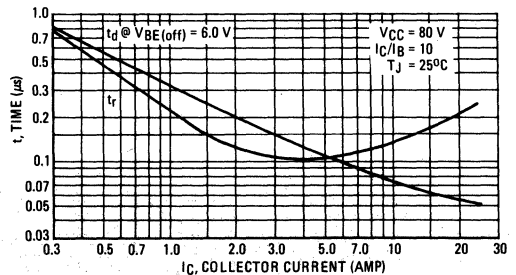


FIGURE 4 – THERMAL RESPONSE

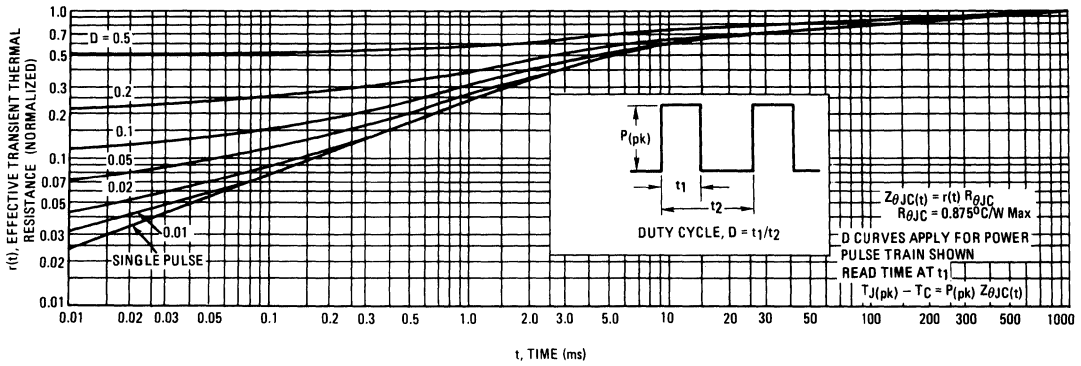
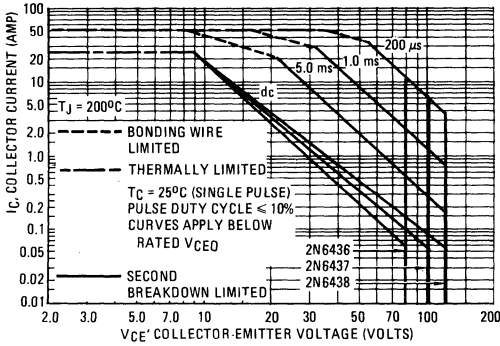


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{j(pk)} = 200^{\circ}\text{C}$; T_c is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{j(pk)} \leq 200^{\circ}\text{C}$. $T_{j(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

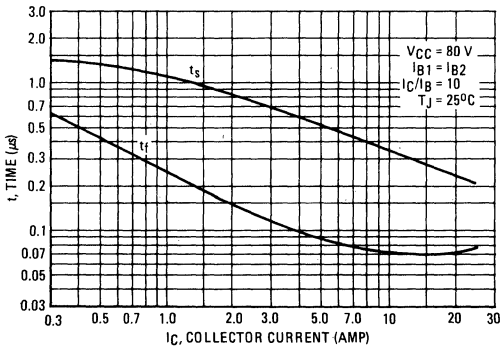


FIGURE 7 – CAPACITANCE

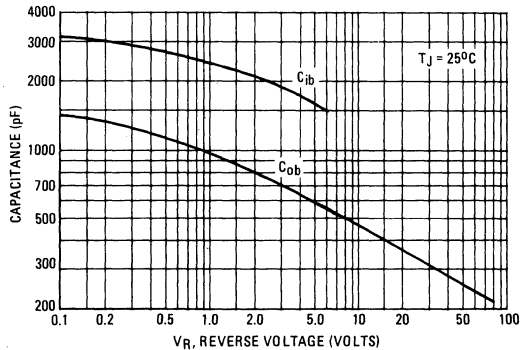


FIGURE 8 – DC CURRENT GAIN

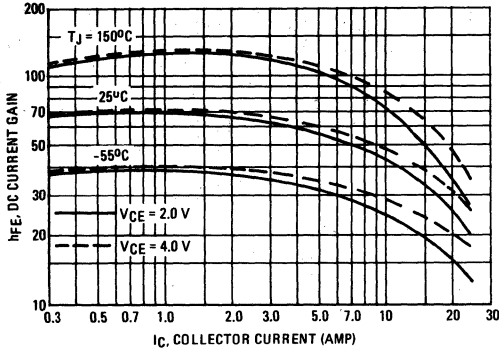


FIGURE 9 – COLLECTOR SATURATION REGION

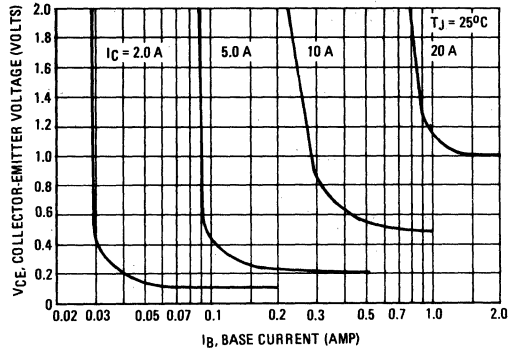


FIGURE 10 – "ON" VOLTAGE

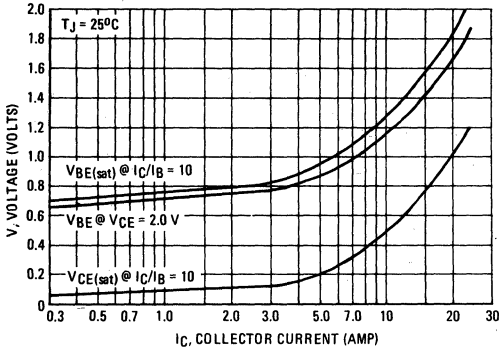


FIGURE 11 – TEMPERATURE COEFFICIENTS

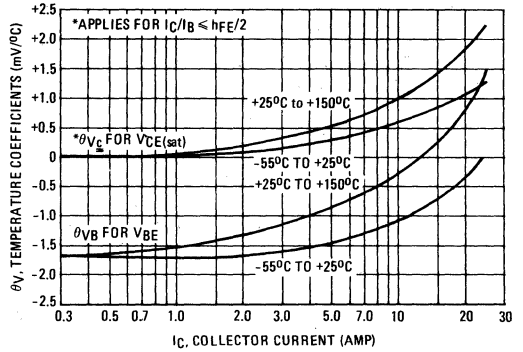


FIGURE 12 – COLLECTOR CUT-OFF REGION

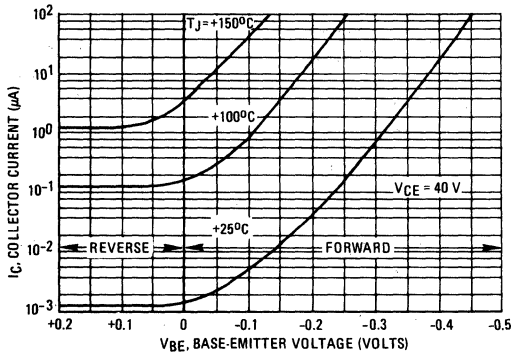
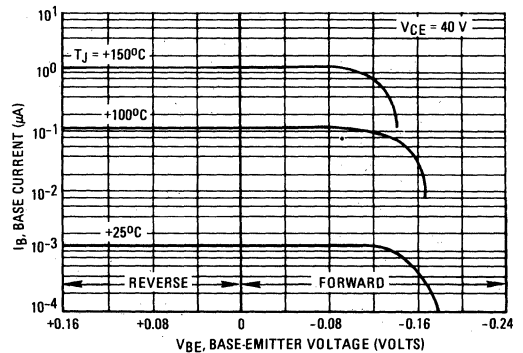


FIGURE 13 – BASE CUT-OFF REGION



NPN	PNP
2N6486	2N6489
2N6487	2N6490
2N6488	2N6491

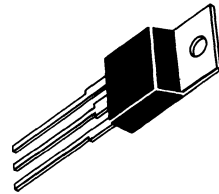
**COMPLEMENTARY SILICON PLASTIC
POWER TRANSISTORS**

... designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 15 Amperes
 $h_{FE} = 20-150 @ I_C = 5.0 \text{ Adc}$
 $= 5.0 \text{ (Min) } @ I_C = 15 \text{ Adc}$
- Collector-Emitter Sustaining Voltage –
 $V_{CEO} \text{ (sus)} = 40 \text{ Vdc (Min) - 2N6486, 2N6489}$
 $= 60 \text{ Vdc (Min) - 2N6487, 2N6490}$
 $= 80 \text{ Vdc (Min) - 2N6488, 2N6491}$
- High Current Gain – Bandwidth Product
 $f_T = 5.0 \text{ MHz (Min) } @ I_C = 1.0 \text{ Adc}$
- TO-220AB Compact Package
- TO-66 Leadform Also Available

**15 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS**

**40-60-80 VOLTS
75 WATTS**



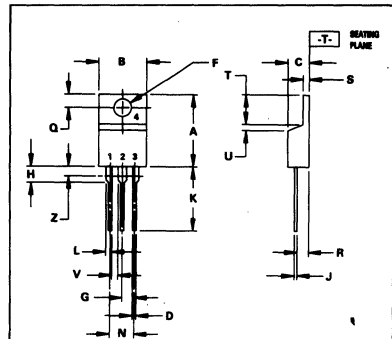
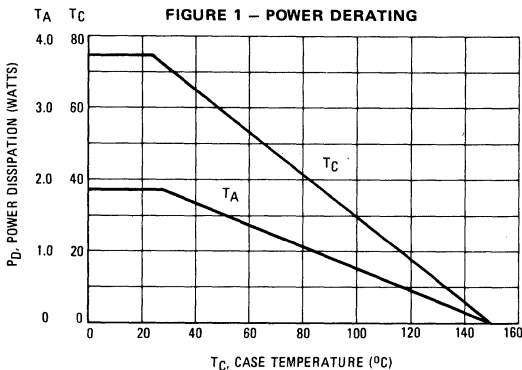
***MAXIMUM RATINGS**

Rating	Symbol	2N6486 2N6489	2N6487 2N6490	2N6488 2N6491	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	50	70	90	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous	I_C	15			Adc
Base Current	I_B	5.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75			Watts
		0.6			W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.8			Watts
		0.014			W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.90	3.35	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.75	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

**CASE 221A-04
TO-220AB**

2N6486 2N6487 2N6488 NPN

2N6489 2N6490 2N6491 PNP

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

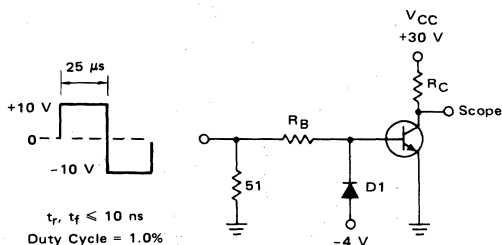
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mA dc}, I_B = 0$)	$V_{CE(sus)}$	40 60 80	— — —	Vdc
Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mA dc}, V_{BE} = 1.5 \text{ Vdc}$)	V_{CEX}	50 70 90	— — —	Vdc
Collector Cutoff Current ($V_{CE} = 20 \text{ Vdc}, I_B = 0$)	I_{CEO}	—	1.0	mAdc
($V_{CE} = 30 \text{ Vdc}, I_B = 0$)		—	1.0	
($V_{CE} = 40 \text{ Vdc}, I_B = 0$)		—	1.0	
Collector Cutoff Current ($V_{CE} = 45 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$)	I_{CEX}	—	500	μAdc
($V_{CE} = 65 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$)		—	500	
($V_{CE} = 85 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}$)		—	500	
($V_{CE} = 40 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)		—	5.0	mAdc
($V_{CE} = 60 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)		—	5.0	
($V_{CE} = 80 \text{ Vdc}, V_{EB(off)} = 1.5 \text{ Vdc}, T_C = 150^\circ\text{C}$)		—	5.0	
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 5.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 15 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	20 5.0	150 —	—
Collector-Emitter Saturation Voltage ($I_C = 5.0 \text{ Adc}, I_B = 0.5 \text{ Adc}$) ($I_C = 15 \text{ Adc}, I_B = 5.0 \text{ Adc}$)	$V_{CE(sat)}$	— —	1.3 3.5	Vdc
Base-Emitter On Voltage ($I_C = 5.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 15 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	— —	1.3 3.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) ($I_C = 1.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}, f_{test} = 1.0 \text{ MHz}$)	f_T	5.0	—	MHz
Small-Signal Current Gain ($I_C = 1.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}, f = 1.0 \text{ kHz}$)	h_{fe}	25	—	—

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $< 300 \mu\text{s}$, Duty Cycle $< 2.0\%$.

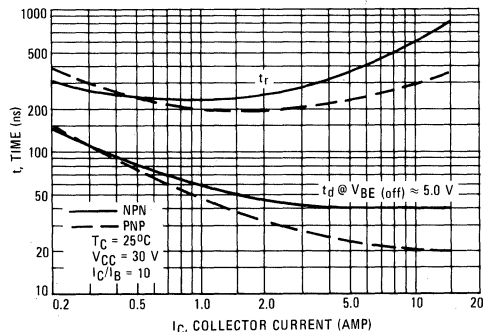
(2) $f_T = I_{hfe} \cdot f_{test}$.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



D1 must be fast recovery type, e.g.;
 MBD5300 used above $I_B \approx 100 \text{ mA}$
 MSD6100 used below $I_B \approx 100 \text{ mA}$

FIGURE 3 — TURN-ON TIME



2N6486 2N6487 2N6488 NPN
 2N6489 2N6490 2N6491 PNP

FIGURE 4 – THERMAL RESPONSE

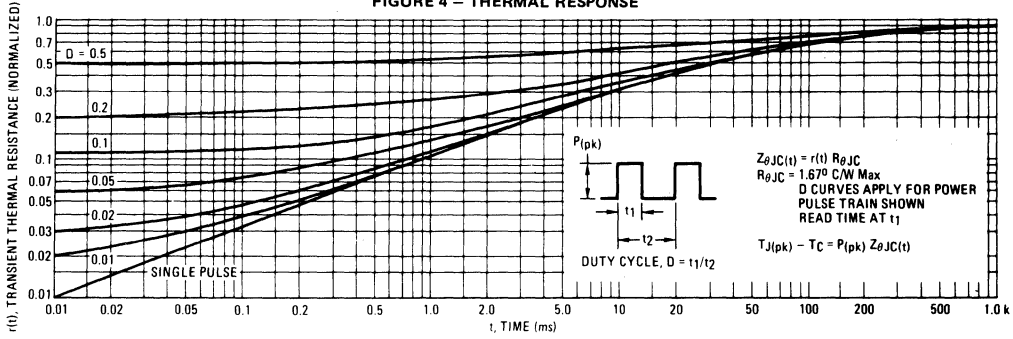
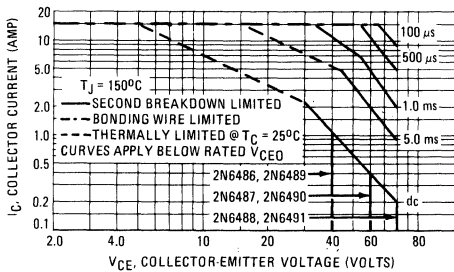


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – TURN-OFF TIME

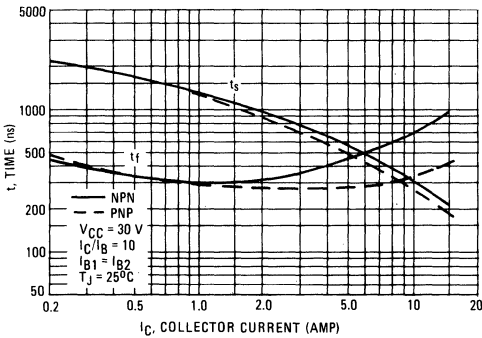
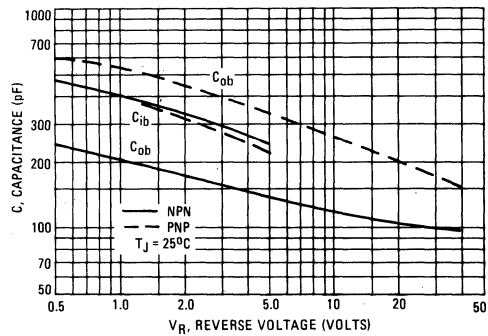


FIGURE 7 – CAPACITANCES



2N6486 2N6487 2N6488 NPN
 2N6489 2N6490 2N6491 PNP

NPN
 2N6486, 2N6487, 2N6488

PNP
 2N6489, 2N6490, 2N6491

FIGURE 8 - DC CURRENT GAIN

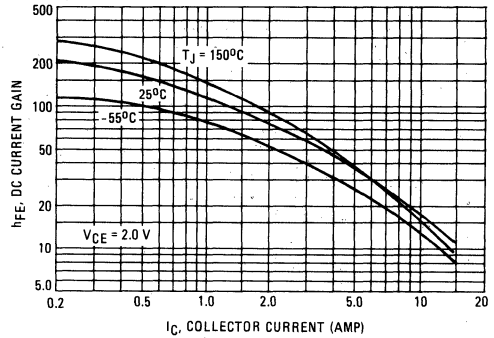
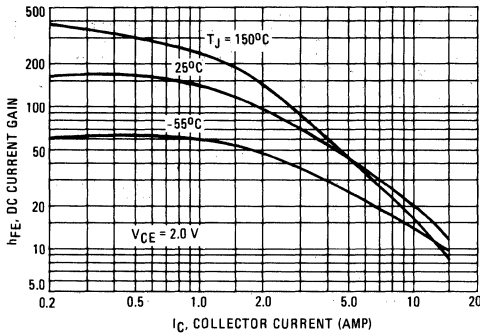


FIGURE 9 - COLLECTOR SATURATION REGION

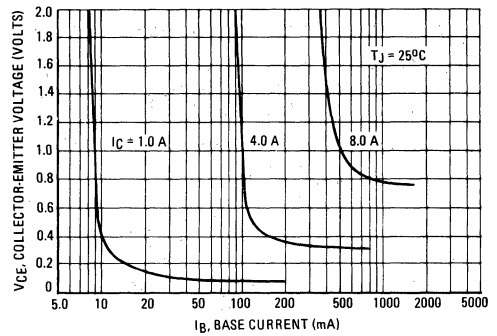
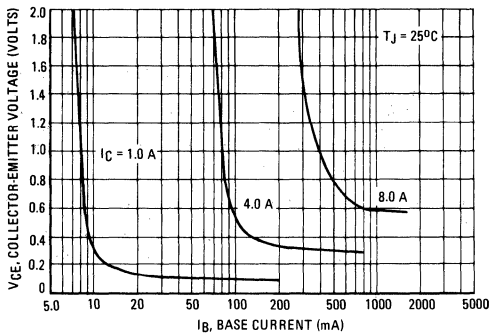
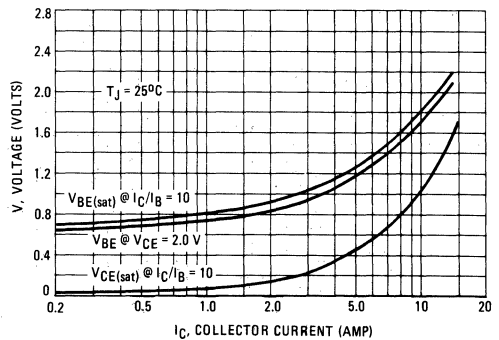
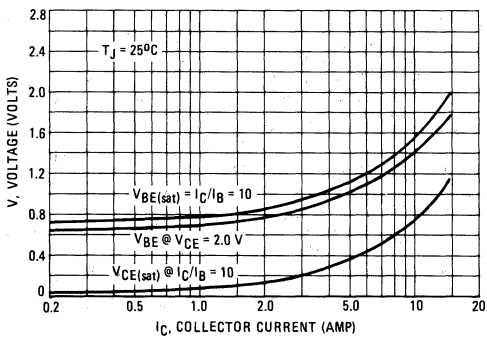


FIGURE 10 - "ON" VOLTAGES



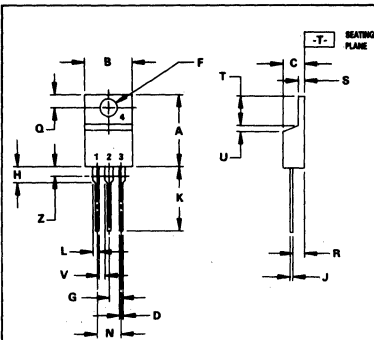
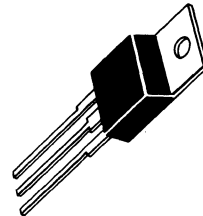
2N6497
2N6498

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

... designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications.

- High Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 250 \text{ Vdc (Min) - 2N6497}$
 $= 300 \text{ Vdc (Min) - 2N6498}$
- Excellent DC Current Gain –
 $h_{FE} = 10 - 75 @ I_C = 2.5 \text{ Adc}$
- Low Collector-Emitter Saturation Voltage @ $I_C = 2.5 \text{ Adc}$ –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) - 2N6497}$
 $= 1.25 \text{ Vdc (Max) - 2N6498}$

5 AMPERE
POWER TRANSISTORS
NPN SILICON
250 & 300 VOLTS
80 WATTS



NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DERMES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.60	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 221A-04
TO-220AB

3

***MAXIMUM RATINGS**

Rating	Symbol	2N6497	2N6498	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	Vdc
Collector-Base Voltage	V_{CB}	350	400	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →	← 6.0 →	Vdc
Collector Current – Continuous – Peak	I_C	← 5.0 →	← 10 →	A dc
Base Current	I_B	← 2.0 →	← 2.0 →	A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 80 →	← 0.64 →	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →	← -65 to +150 →	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data.

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 25 \text{ mAdc}$, $I_B = 0$)	2N6497 2N6498	$V_{CE(sus)}$	250 300	— —	Vdc
Collector Cutoff Current ($V_{CE} = 350 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 400 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 175 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 100^\circ\text{C}$) ($V_{CE} = 200 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 100^\circ\text{C}$)	2N6497 2N6498 2N6497 2N6498	I_{CEX}	— — — —	— — 10 10	mAdc
Emitter Cutoff Current ($V_{BE} = 6.0 \text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 2.5 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$) ($I_C = 5.0 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$)		h_{FE}	10 3.0	— —	—
Collector-Emitter Saturation Voltage ($I_C = 2.5 \text{ Adc}$, $I_B = 500 \text{ mAdc}$) ($I_C = 5.0 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$)	2N6497 2N6498 All Devices	$V_{CE(sat)}$	— —	— —	Vdc
Base-Emitter Saturation Voltage ($I_C = 2.5 \text{ Adc}$, $I_B = 500 \text{ mAdc}$) ($I_C = 5.0 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$)		$V_{BE(sat)}$	— —	— —	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product ($I_C = 250 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)		f_T	5.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 100 \text{ kHz}$)		C_{ob}	—	150	pF
SWITCHING CHARACTERISTICS					
Rise Time ($V_{CC} = 125 \text{ Vdc}$, $I_C = 2.5 \text{ Adc}$, $I_{B1} = 0.5 \text{ Adc}$)		t_r	—	0.4	μs
Storage Time ($V_{CC} = 125 \text{ Vdc}$, $I_C = 2.5 \text{ Adc}$, $V_{BE} = 5.0 \text{ Vdc}$, $I_{B1} = I_{B2} = 0.5 \text{ Adc}$)		t_s	—	1.4	μs
Fall Time ($V_{CC} = 125 \text{ Vdc}$, $I_C = 2.5 \text{ Adc}$, $I_{B1} = I_{B2} = 0.5 \text{ Adc}$)		t_f	—	0.45	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

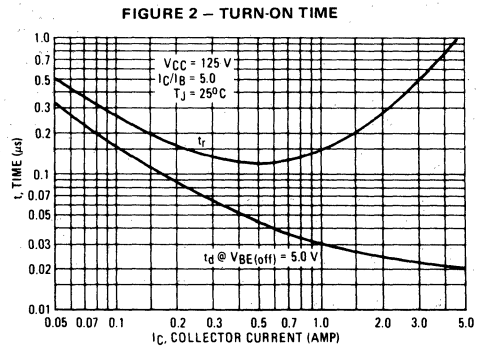
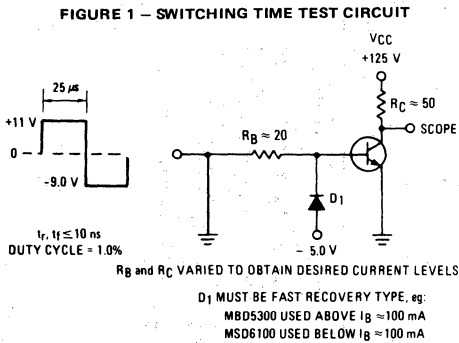


FIGURE 3 – THERMAL RESPONSE

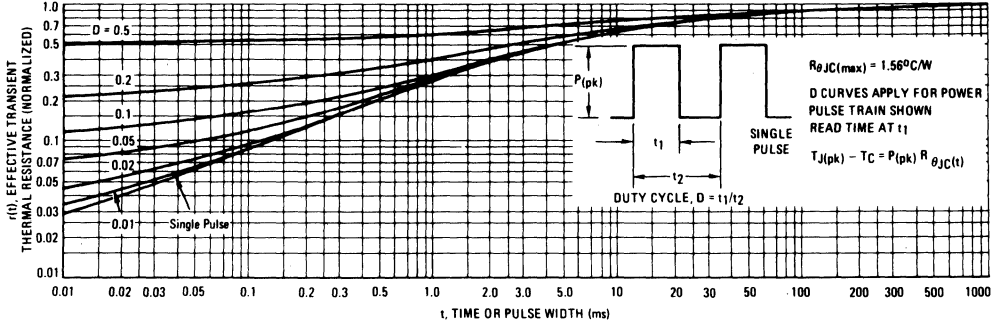
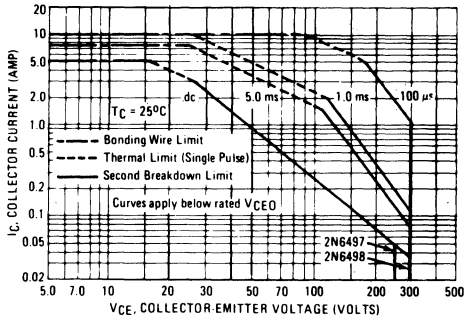


FIGURE 4 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 4 may be found at any case temperature by using the appropriate curve on Figure 6.

FIGURE 5 – TURN-OFF TIME

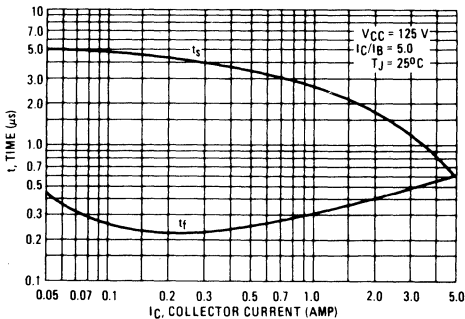


FIGURE 6 – POWER DERATING

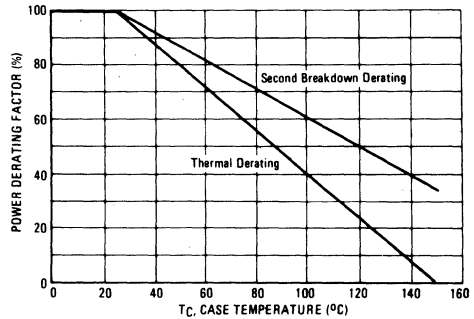


FIGURE 7 – DC CURRENT GAIN

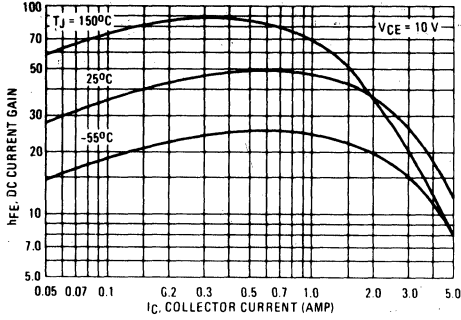


FIGURE 8 – COLLECTOR SATURATION REGION

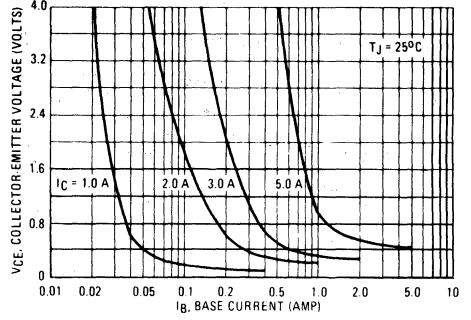


FIGURE 9 – "ON" VOLTAGES

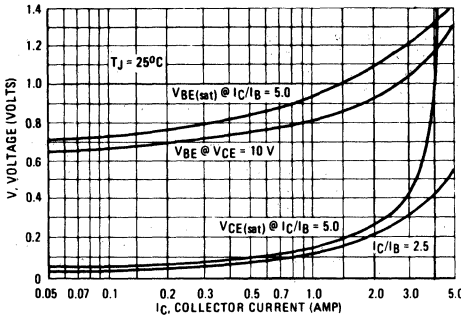


FIGURE 10 – TEMPERATURE COEFFICIENTS

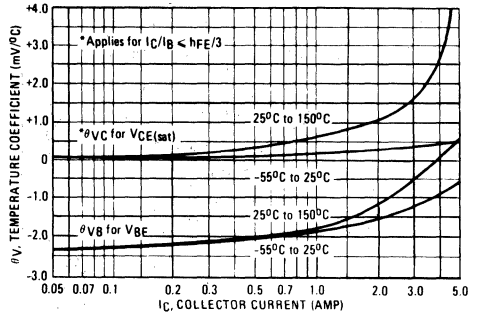


FIGURE 11 – COLLECTOR CUTOFF REGION

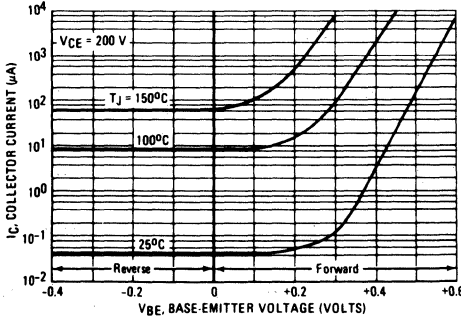
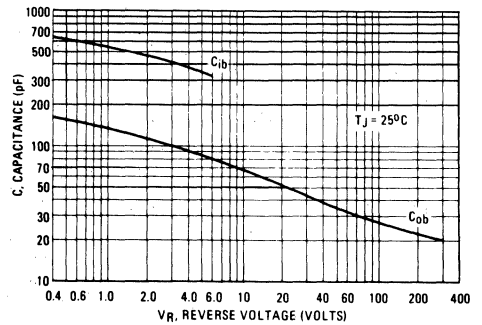


FIGURE 12 – CAPACITANCE



3

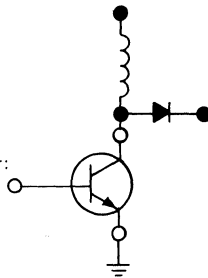
Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

This device is designed for high-voltage, high-speed, power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 200 volt line operated SWITCHMODE applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

- Specification Features –
- High Temperature Performance Specified for:
 - Reversed Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents



***MAXIMUM RATINGS**

Rating	Symbol	2N6543	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	8.0	Vdc
Collector Current – Continuous	I_C	5.0	Adc
– Peak (1)	I_{CM}	10	
Base Current – Continuous	I_B	5.0	Adc
– Peak (1)	I_{BM}	10	
Emitter Current – Continuous	I_E	10	Adc
– Peak (1)	I_{EM}	20	
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	100	Watts
@ $T_C = 100^\circ C$		57.2	
Derate above $25^\circ C$		0.57	W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ C$

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

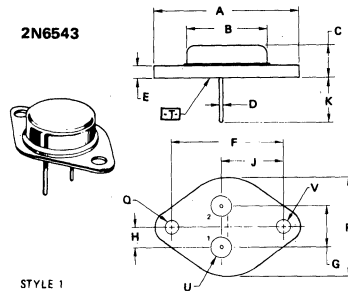
2N6543

5 AMPERE
NPN SILICON
POWER TRANSISTOR
400 VOLTS
100 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

2N6543



STYLE 1
 PIN 1 BASE
 2 EMITTER
 CASE COLLECTOR

NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. \square IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\text{MOUNTING HOLE Q: } \text{M} \pm 0.13 \text{ (0.005) } \text{V} \text{ T } \text{V} \text{ Q}$$

FOR LEADS:

$$\text{LEADS: } \text{M} \pm 0.13 \text{ (0.005) } \text{V} \text{ T } \text{V} \text{ Q } \text{Q}$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.87	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15	BSC	1.187	BSC
G	10.92	BSC	0.430	BSC
H	5.48	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	400	—	Vdc
Collector-Emitter Sustaining Voltage (Table 2, Figure 12) ($I_C = 2.6\text{ A}$, $V_{clamp} = \text{Rated } V_{CEX}$, $T_C = 100^\circ\text{C}$)	$V_{CEX(sus)}$	450	—	Vdc
($I_C = 5.0\text{ Adc}$, $V_{clamp} = \text{Rated } V_{CE0} - 100\text{ V}$, $T_C = 100^\circ\text{C}$)		300	—	
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	0.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 8.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased $t = 1.0\text{ s}$ (non-repetitive) ($V_{CE} = 100\text{ Vdc}$)	$I_{S/b}$	0.2	—	Adc
		(See Figure 11)		
Clamped Inductive SOA with base reverse biased	RBSOA	(See Figure 12)		

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 1.5\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$) ($I_C = 3.0\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$)	h_{FE}	12	60	—
		7.0	35	
Collector-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	1.0	Vdc
		—	5.0	
		—	2.0	
Base-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	1.4	Vdc
		—	1.4	

DYNAMIC CHARACTERISTICS

Current-Gain -- Bandwidth Product ($I_C = 200\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1.0\text{ MHz}$)	f_T	6.0	28	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ MHz}$)	C_{ob}	50	200	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 2)					
Delay Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 3.0\text{ A}$, $I_{B1} = I_{B2} = 0.6\text{ A}$, $t_p = 100\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.05	μs
Rise Time		t_r	—	0.7	μs
Storage Time		t_s	—	4.0	μs
Fall Time		t_f	—	0.8	μs
Inductive Load, Clamped (Table 2)					
Storage Time	Symbol	Typ	Max	Unit	
Storage Time	t_{sv}	—	4.0	μs	
Crossover Time	t_c	0.6	—	μs	
Fall Time	t_{fi}	—	0.8	μs	
Storage Time	t_{sv}	0.8	—	μs	
Crossover Time	t_c	0.3	—	μs	
Fall Time	t_{fi}	0.2	—	μs	

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

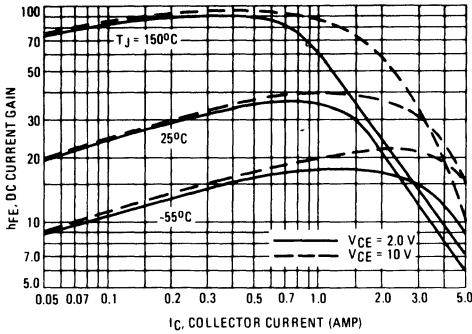


FIGURE 2 – COLLECTOR SATURATION REGION

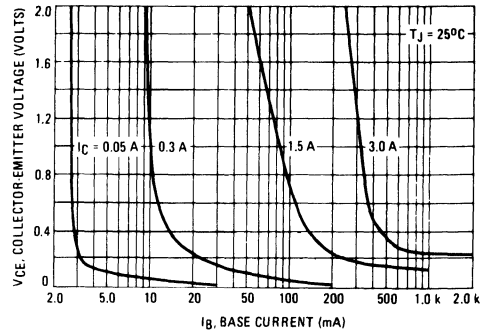


FIGURE 3 – "ON" VOLTAGE

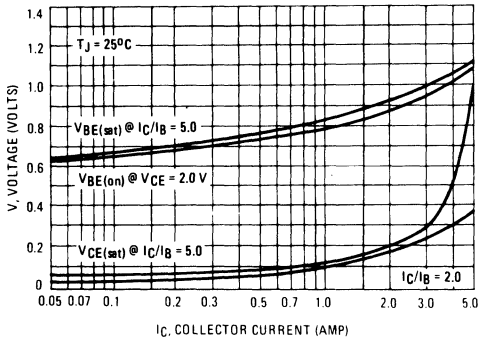


FIGURE 4 – TEMPERATURE COEFFICIENTS

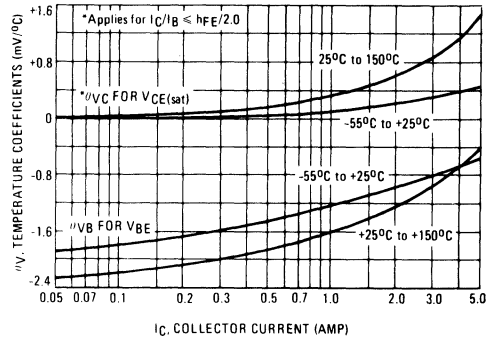


FIGURE 5 – COLLECTOR CUTOFF REGION

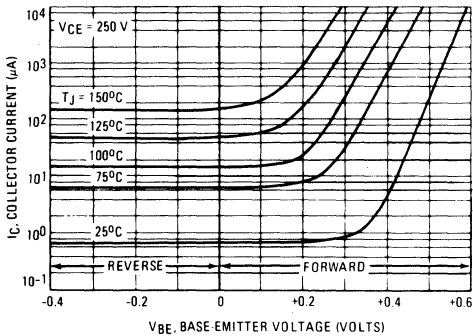


FIGURE 6 – CAPACITANCE

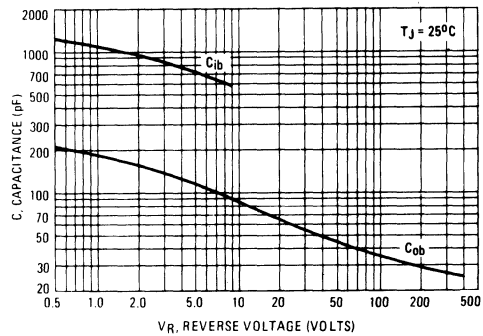


FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

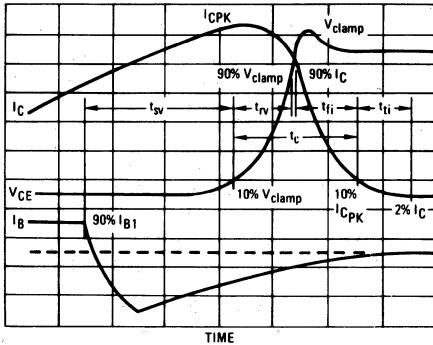


TABLE 1 – INDUCTIVE SWITCHING PERFORMANCE

IC (A)	TC (°C)	tsv (μs)	trv (μs)	tfi (μs)	ttr (μs)	tc (μs)
1.0	25	0.70	0.22	0.21	0.23	0.66
100	100	1.20	0.37	0.19	0.39	0.95
3.0	25	1.10	0.09	0.12	0.08	0.29
100	100	1.60	0.42	0.19	0.40	1.01
5.0	25	1.10	0.16	0.19	0.11	0.46
100	100	1.70	0.45	0.37	0.26	1.08

Note: All Data Recorded in the Inductive Switching Circuit Shown in Table 2.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- tsv = Voltage Storage Time, 90% IB1 to 10% Vclamp
- trv = Voltage Rise Time, 10–90% Vclamp
- tfi = Current Fall Time, 90–10% IC
- ttr = Current Tail, 10–2% IC
- tc = Crossover Time, 10% Vclamp to 10% IC

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{tr} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (tc and tsv) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

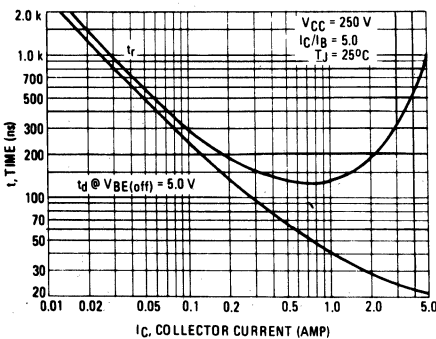


FIGURE 9 – TURN-OFF TIME

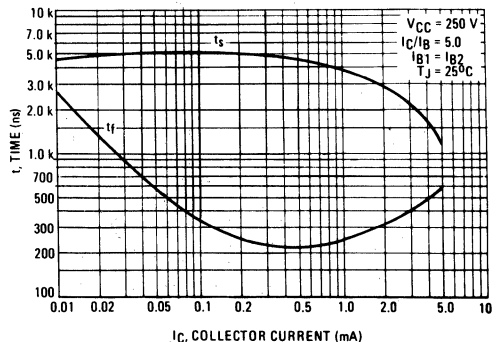


TABLE 2 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

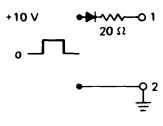
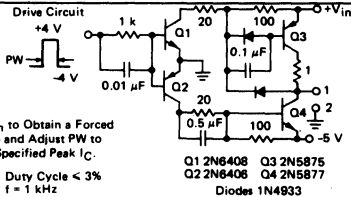
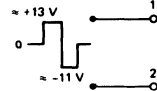
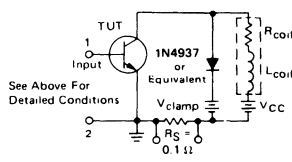
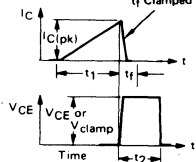
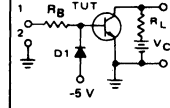
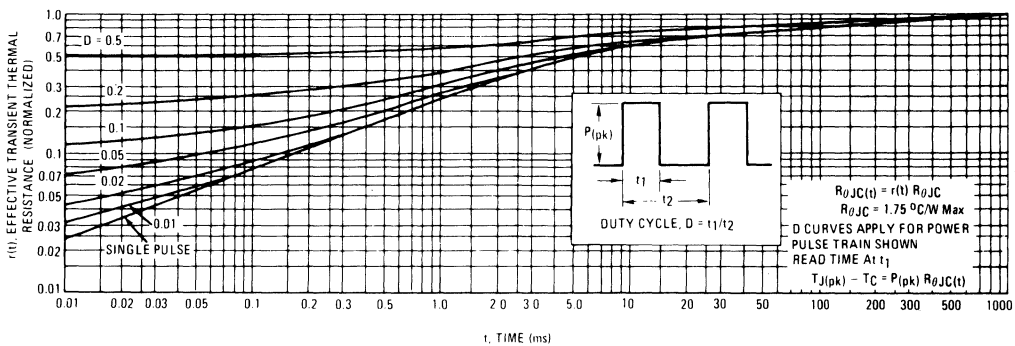
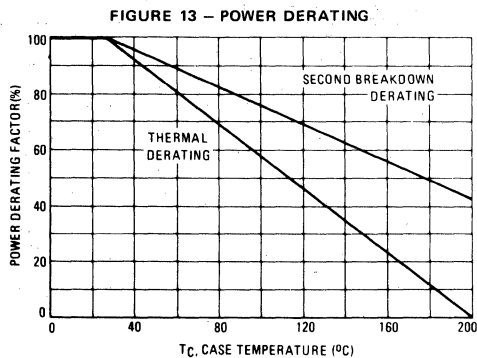
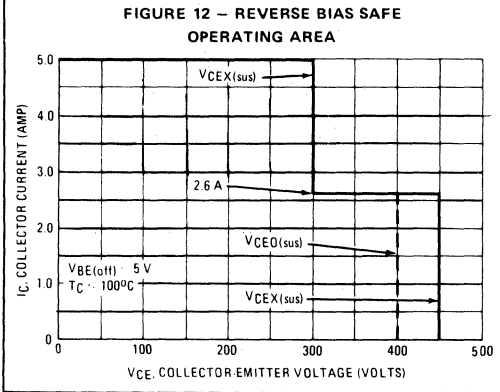
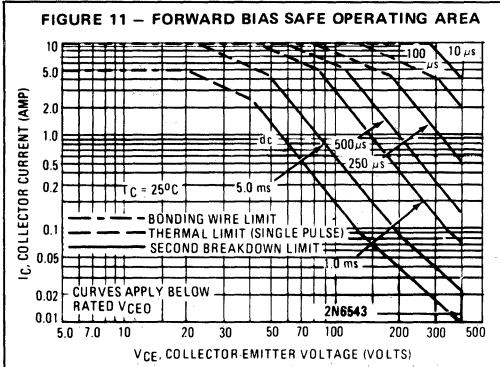
	V _{CEO(sus)}	V _{CEX(sus)} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>+10 V 20 Ω 0</p> <p>PW Varied to Attain I_C = 100 mA</p>	 <p>Drive Circuit +4 V 1 k 0.01 μF -4 V</p> <p>Set +V_{in} to Obtain a Forced h_{FE} = 5 and Adjust PW to Attain Specified Peak I_C. Duty Cycle < 3% f = 1 kHz</p> <p>Q1 2N6408 Q3 2N5875 Q2 2N6406 Q4 2N5877 Diodes 1N4933</p>	 <p>≈ +13 V 0 ≈ -11 V</p> <p>I_C = 3 A PW ≈ 100 μs t_r < 5 ns t_f < 50 ns Duty Cycle < 2%</p>
CIRCUIT VALUES	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} (Unclamped)</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>V_{clamp} = Rated V_{CEX} Value</p>	<p>V_{CC} = 260 V R_L = 83 Ω D1 = 1N5820 or Equiv. R_B = 20 Ω</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>TUT 1N4937 or Equivalent R_{coil} L_{coil} V_{CC} R_S = 0.1 Ω V_{clamp}</p> <p>See Above For Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>I_C I_{C(pk)} t₁ t₂ t₁ Clamped</p> <p>V_{CE} V_{CE} or V_{clamp}</p> <p>t₁ Adjusted to Obtain I_C t₁ ≈ $\frac{L_{coil}(I_{Cpk})}{V_{CC}}$ t₂ ≈ $\frac{L_{coil}(I_{Cpk})}{V_{clamp}}$</p> <p>Test Equipment Scope-Tektronics 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>  <p>TUT R_B D1 R_L V_{CC} -5 V</p>

FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC-VCE limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on Tc = 25°C; TJ(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when Tc ≥ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

TJ(pk) may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.

2N6545

Designers Data Sheet

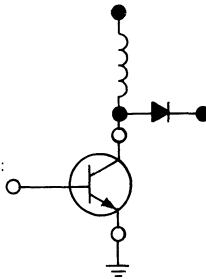
**SWITCHMODE SERIES
 NPN SILICON POWER TRANSISTOR**

The 2N6545 transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features —

- High Temperature Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



**8 AMPERE
 NPN SILICON
 POWER TRANSISTOR**

**400 VOLTS
 125 WATTS**

**Designer's Data for
 "Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

***MAXIMUM RATINGS**

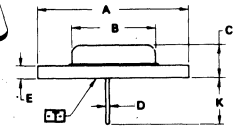
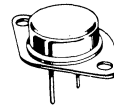
Rating	Symbol	2N6545	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	9.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
— Peak (1)	I_{CM}	16	
Base Current — Continuous	I_B	8.0	Adc
— Peak (1)	I_{BM}	16	
Emitter Current — Continuous	I_E	16	Adc
— Peak (1)	I_{EM}	32	
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	125	Watts
Derate above $25^\circ C$		71.5	
@ $T_C = 100^\circ C$		0.714	W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ C$

THERMAL CHARACTERISTICS

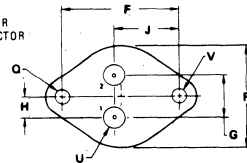
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ C$

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.



STYLE 1
 PIN 1, BASE
 2, EMITTER
 CASE COLLECTOR



- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. \square IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\pm \text{MIL } (0.005) \text{ T V } \text{M}$$

FOR LEADS:

$$\pm \text{MIL } (0.005) \text{ T V } \text{M}$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.06	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15	BSC	1.187	BSC
G	10.92	BSC	0.430	BSC
H	5.46	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

**CASE 1-05
 TO-204AA**

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
Collector-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE0}(\text{sus})$	400	—	Vdc
Collector-Emitter Sustaining Voltage ($I_C = 4.5\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{CEX}$, $T_C = 100^\circ\text{C}$)	$V_{CEX}(\text{sus})$	450	—	Vdc
($I_C = 8.0\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{CE0} - 100\text{ V}$, $T_C = 100^\circ\text{C}$)		300	—	
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(\text{off})} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(\text{off})} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	0.5 2.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 9.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased $t = 1.0\text{ s}$ (non-repetitive) ($V_{CE} = 100\text{ Vdc}$)	$I_{S/b}$	0.2	—	A
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ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 2.5\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$) ($I_C = 5.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$)	h_{FE}	12 7.0	60 35	—
Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 8.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE}(\text{sat})$	— — —	1.5 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE}(\text{sat})$	— —	1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain – Bandwidth Product ($I_C = 300\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f_{\text{test}} = 1.0\text{ MHz}$)	f_T	6.0	28	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 1.0\text{ MHz}$)	C_{ob}	75	300	pF

SWITCHING CHARACTERISTICS

Resistive Load					
Delay Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 5.0\text{ A}$, $I_{B1} = I_{B2} = 1.0\text{ A}$, $t_p = 100\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.05	μs
Rise Time		t_r	—	1.0	μs
Storage Time		t_s	—	4.0	μs
Fall Time		t_f	—	1.0	μs
Inductive Load, Clamped					
Storage Time	$(I_C = 5.0\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{CEX}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(\text{off})} = 5.0\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_s	—	4.0	μs
Fall Time		t_f	—	0.9	μs
Typical					
Storage Time	$(I_C = 5.0\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{CEX}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(\text{off})} = 5.0\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_s	—	1.2	μs
Fall Time		t_f	—	0.18	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = $300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

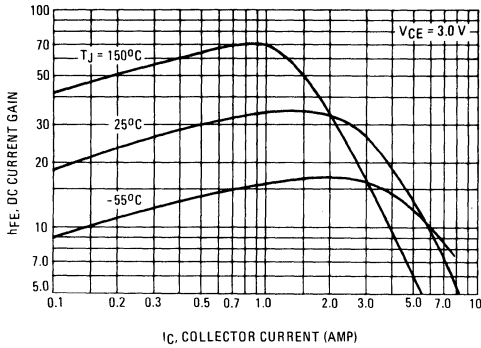


FIGURE 2 – COLLECTOR SATURATION REGION

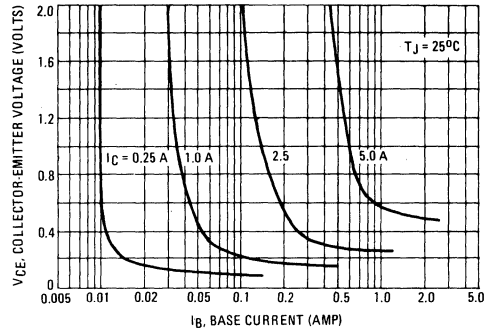


FIGURE 3 – "ON" VOLTAGE

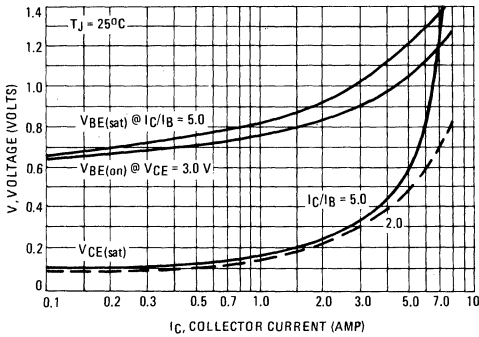


FIGURE 4 – TEMPERATURE COEFFICIENTS

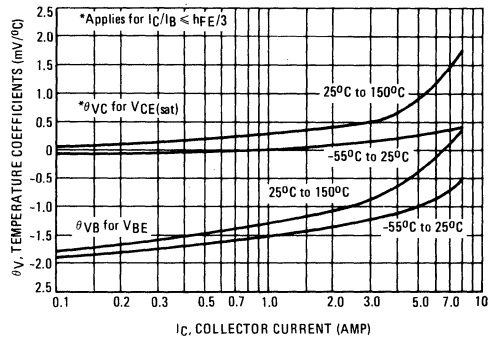


FIGURE 5 – TURN-ON TIME

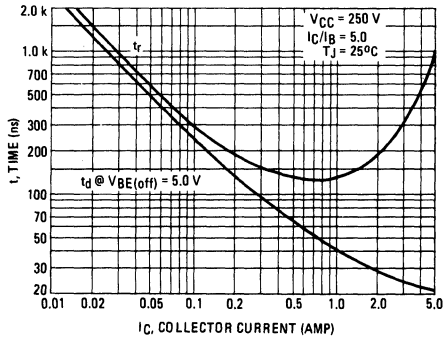


FIGURE 6 – TURN-OFF TIME

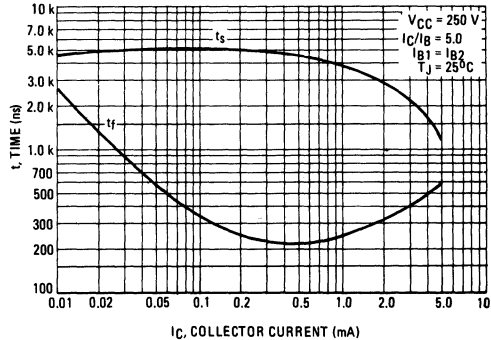


FIGURE 7 – FORWARD BIAS SAFE OPERATING AREA

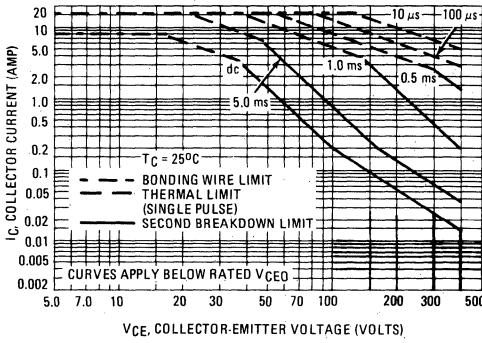


FIGURE 8 – REVERSE BIAS SAFE OPERATING AREA

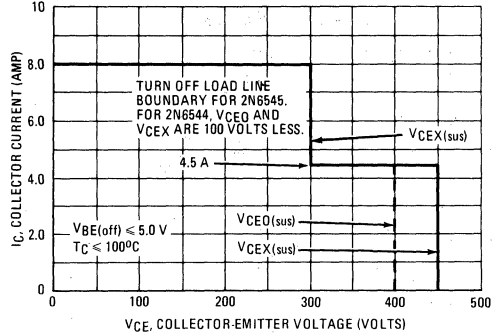
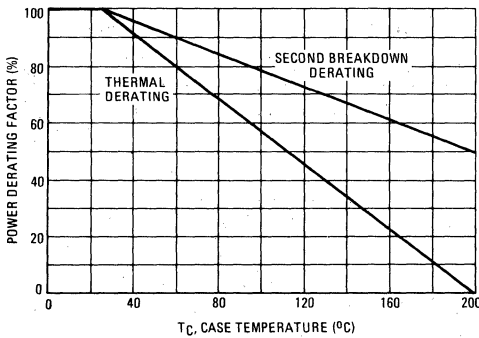


FIGURE 9 – POWER DERATING

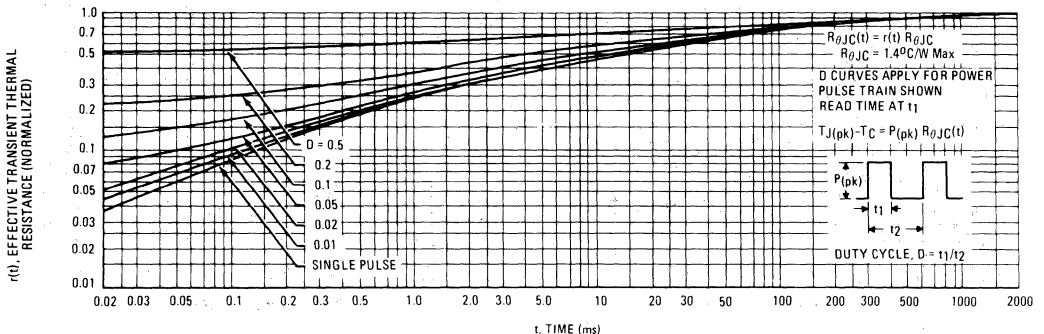


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7, may be found at any case temperature by using the appropriate curve on Figure 9.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. The reverse biased safe operating area (Figure 8) is the boundary the load line may traverse during turn-off.

FIGURE 10 – THERMAL RESPONSE



3

Designers Data Sheet

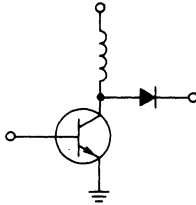
**SWITCHMODE SERIES
 NPN SILICON POWER TRANSISTORS**

The 2N6546 and 2N6547 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features –

- High Temperature Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



***MAXIMUM RATINGS**

Rating	Symbol	2N6546	2N6547	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	300	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	350	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	850	Vdc
Emitter Base Voltage	V_{EB}	9.0		Vdc
Collector Current – Continuous	I_C		15	Adc
– Peak (1)	I_{CM}		30	
Base Current – Continuous	I_B		10	Adc
– Peak (1)	I_{BM}		20	
Emitter Current – Continuous	I_E		25	Adc
– Peak (1)	I_{EM}		50	
Total Power Dissipation @ $T_C = 25^\circ C$	P_D		175	Watts
@ $T_C = 100^\circ C$			100	
Derate above $25^\circ C$			1.0	W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ C$

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle < 10%.

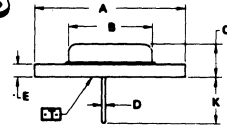
2N6546
2N6547

**15 AMPERE
 NPN SILICON
 POWER TRANSISTORS**

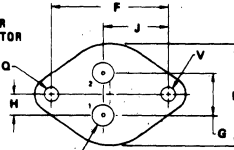
**300 and 400 VOLTS
 175 WATTS**

**Designer's Data for
 "Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



STYLE 1
 PIN 1 BASE
 PIN 2 EMITTER
 CASE COLLECTOR



NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. \overline{T} IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE \varnothing :

$$\varnothing \pm 0.13 (0.005) \varnothing T \sqrt{\varnothing}$$

FOR LEADS

$$\varnothing \pm 0.13 (0.005) \varnothing T \sqrt{\varnothing} \varnothing \varnothing$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	38.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

**CASE 1-05
 TO-204AA**

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE0(sus)}$	300 400	—	Vdc	
Collector-Emitter Sustaining Voltage ($I_C = 8.0\text{ A}$, $V_{clamp} = \text{Rated } V_{CEX}$, $T_C = 100^\circ\text{C}$)	$V_{CEX(sus)}$	350 450	—	Vdc	
($I_C = 15\text{ A}$, $V_{clamp} = \text{Rated } V_{CE0} - 100\text{ V}$, $T_C = 100^\circ\text{C}$)		200 300	—		
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$)	I_{CEV}	—	1.0	mAdc	
($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)		—	4.0		
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	5.0	mAdc	
Emitter Cutoff Current ($V_{EB} = 9.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	mAdc	
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased $t = 1.0\text{ s}$ (non-repetitive) ($V_{CE} = 100\text{ Vdc}$)	$I_{S/b}$	0.2	—	Adc	
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 5.0\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$)	h_{FE}	12	60	—	
($I_C = 10\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$)		6.0	30		
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2.0\text{ Adc}$)	$V_{CE(sat)}$	—	1.5	Vdc	
($I_C = 15\text{ Adc}$, $I_B = 3.0\text{ Adc}$)		—	5.0		
($I_C = 10\text{ Adc}$, $I_B = 2.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)		—	2.5		
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2.0\text{ Adc}$)	$V_{BE(sat)}$	—	1.6	Vdc	
($I_C = 10\text{ Adc}$, $I_B = 2.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)		—	1.6		
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product ($I_C = 500\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1.0\text{ MHz}$)	f_T	6.0	28	MHz	
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ MHz}$)	C_{ob}	125	500	pF	
SWITCHING CHARACTERISTICS					
Resistive Load					
Delay Time	$(V_{CC} = 250\text{ V}$, $I_C = 10\text{ A}$, $I_{B1} = I_{B2} = 2.0\text{ A}$, $t_p = 100\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.05	μs
Rise Time		t_r	—	1.0	μs
Storage Time		t_s	—	4.0	μs
Fall Time		t_f	—	0.7	μs
Inductive Load, Clamped					
Storage Time	$(I_C = 10\text{ A(pk)}$, $V_{clamp} = \text{Rated } V_{CEX}$, $I_{B1} = 2.0\text{ A}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_s	—	5.0	μs
Fall Time		t_f	—	1.5	μs
Typical					
Storage Time	$(I_C = 10\text{ A(pk)}$, $V_{clamp} = \text{Rated } V_{CEX}$, $I_{B1} = 2.0\text{ A}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_s	2.0	μs	
Fall Time		t_f	0.09	μs	

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

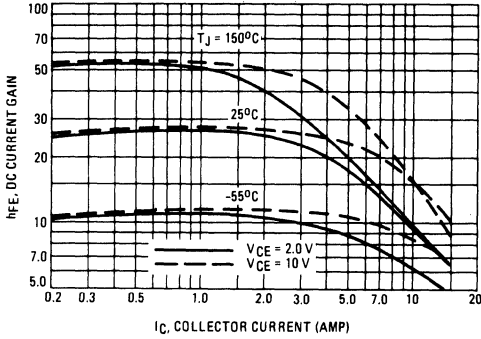


FIGURE 2 – COLLECTOR SATURATION REGION

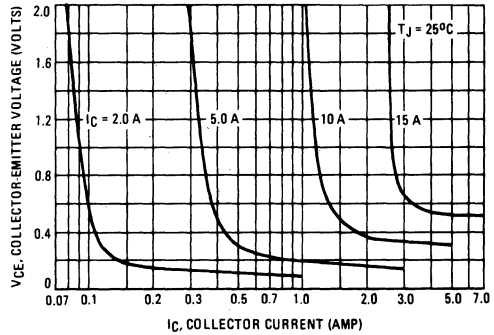


FIGURE 3 – "ON" VOLTAGE

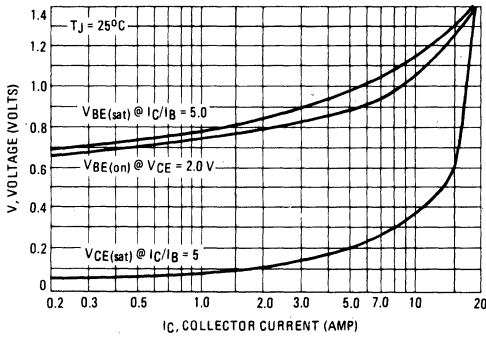


FIGURE 4 – TEMPERATURE COEFFICIENTS

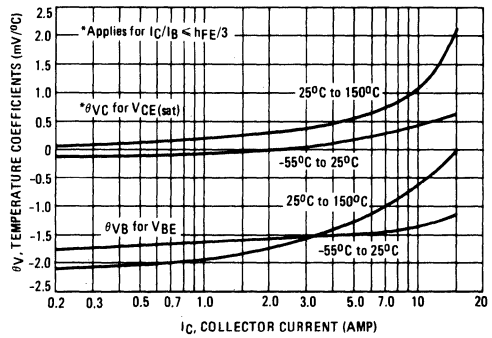


FIGURE 5 – TURN-ON TIME

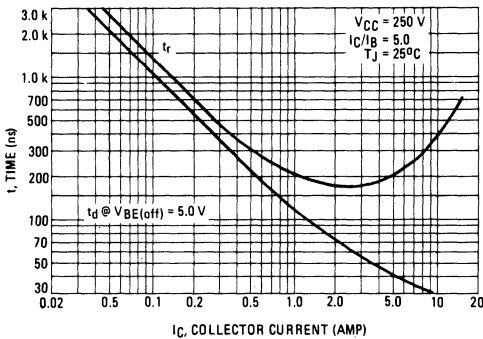
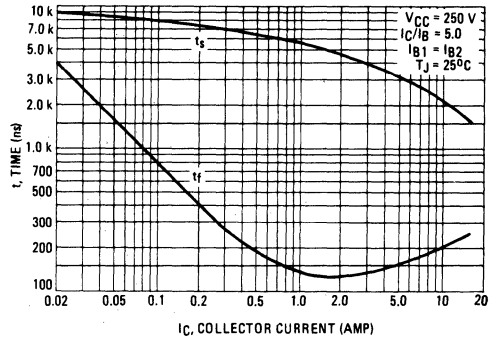


FIGURE 6 – TURN-OFF TIME



MAXIMUM RATED SAFE OPERATING AREAS

FIGURE 7 - FORWARD BIAS SAFE OPERATING AREA

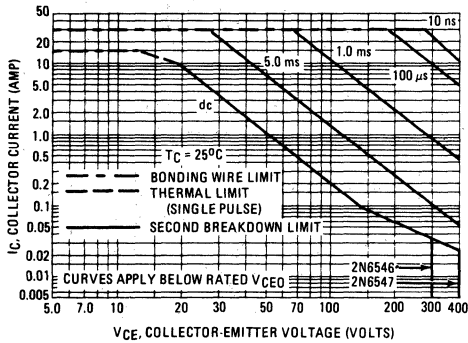


FIGURE 8 - REVERSE BIAS SAFE OPERATING AREA

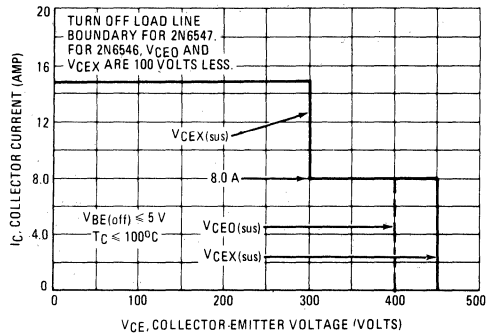
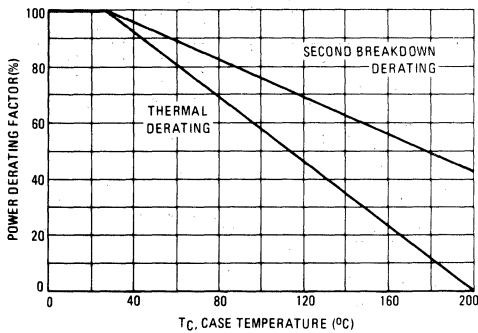


FIGURE 9 - POWER DERATING

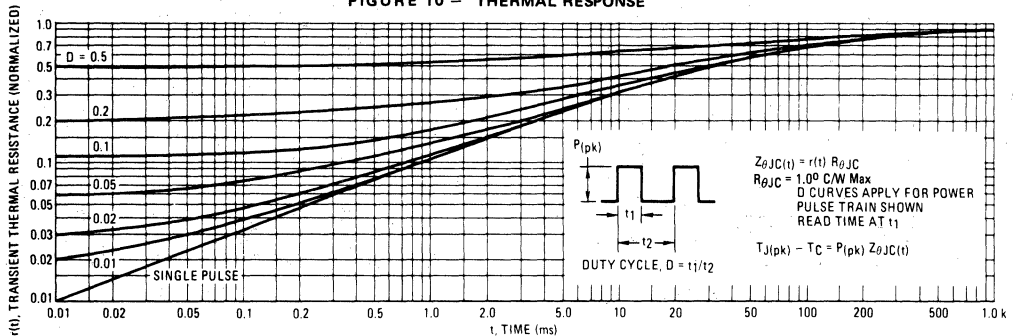


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 10 - THERMAL RESPONSE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6576
2N6577
2N6578

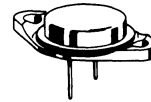
NPN SILICON POWER DARLINGTON TRANSISTORS

General-purpose EpiBase power Darlington transistors, suitable for linear and switching applications.

- Replacement for 2N3055 and Driver
- High Gain Darlington Performance
- Built-In Diode Protection for Reverse Polarity Protection
- Can Be Driven from Low-Level Logic
- Popular Voltage Range
- Operating Range – –65 to +200°C

15 AMPERE
POWER TRANSISTORS

NPN SILICON
DARLINGTON
60, 90, 120 VOLTS
120 WATTS



***MAXIMUM RATINGS**

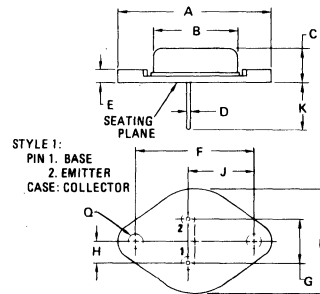
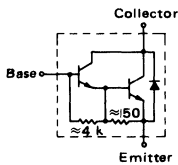
Rating	Symbol	2N6576	2N6577	2N6578	Unit
Collector-Emitter Voltage	V _{CEO(sus)}	60	90	120	Vdc
Collector-Base Voltage	V _{CB}	60	90	120	Vdc
Emitter-Base Voltage	V _{EB}	← 7.0 →			Vdc
Collector Current – Continuous	I _C	← 15 →			A dc
		← 30 →			
Base Current – Continuous	I _B	← 0.25 →			A dc
		← 0.50 →			
Emitter Current – Continuous	I _E	← 15.25 →			A dc
		← 30.5 →			
Total Power Dissipation @ T _C = 25°C	P _D	← 120 →			Watts
		← 0.685 →			
Operating and Storage Junction Temperature Range	T _J , T _{stg}	← -65 to +200 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.46	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for 10s.	T _L	265	°C

*Indicates JEDEC Registered Data

DARLINGTON SCHEMATIC



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

CASE 11-03
TO-3

2N6576, 2N6577, 2N6578

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage(1) ($I_C = 200 \text{ mAdc}, I_B = 0$)	$V_{CE(sus)}$	60 90 120	—	Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated Value}$)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current ($V_{CER} = \text{Rated } V_{CE(sus)} \text{ Value}, R_{BE} = 10 \text{ k}\Omega, T_C = 150^\circ\text{C}$)	I_{CER}	—	5.0	mAdc
Collector Cutoff Current $V_{CEX} = \text{Rated } V_{CE(sus)} \text{ Value}, V_{BE(off)} = 1.5 \text{ Vdc}$	I_{CEV}	—	5.0	mAdc
Collector Cutoff Current ($V_{CB} = \text{Rated Value}$)	I_{CBO}	—	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 15 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 10 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 4.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 0.4 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}$)	h_{FE}	100 500 2000 200	— 5,000 20,000 —	—
Collector-Emitter Saturation Voltage ($I_C = 15 \text{ Adc}, I_B = 0.15 \text{ Adc}$) ($I_C = 10 \text{ Adc}, I_B = 0.1 \text{ Adc}$)	$V_{CE(sat)}$	— —	4.0 2.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 15 \text{ Adc}, I_B = 0.15 \text{ Adc}$) ($I_C = 10 \text{ Adc}, I_B = 0.1 \text{ Adc}$)	$V_{BE(sat)}$	— —	4.5 3.5	Vdc
Collector-Emitter Diode Voltage Drop ($I_{EC} = 15 \text{ Adc}$)	V_F	—	4.5	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common-Emitter Small-Signal Short-Circuit Current Transfer Ratio ($I_C = 3.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}, f = 1.0 \text{ MHz}$)	$ h_{fe} $	10	200	—

SWITCHING CHARACTERISTICS

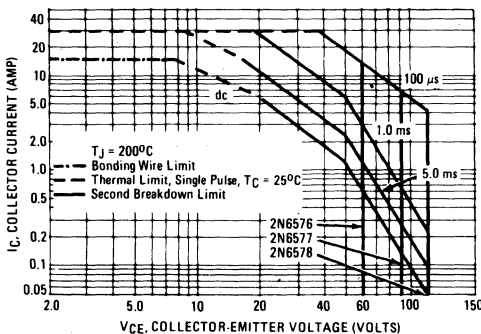
RESISTIVE LOAD (Figure 2)

Characteristic	Symbol	Min	Max	Unit
Delay Time	t_d	—	0.15	μs
Rise Time	t_r	—	1.0	μs
Storage Time	t_s	—	2.0	μs
Fall Time	t_f	—	7.0	μs

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 1 — RATED FORWARD BIASED SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%.

$T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – DC CURRENT GAIN

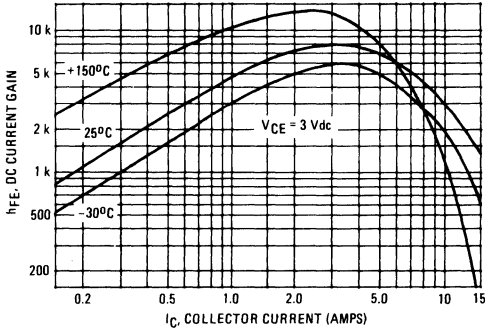


FIGURE 3 – COLLECTOR-SATURATION REGION

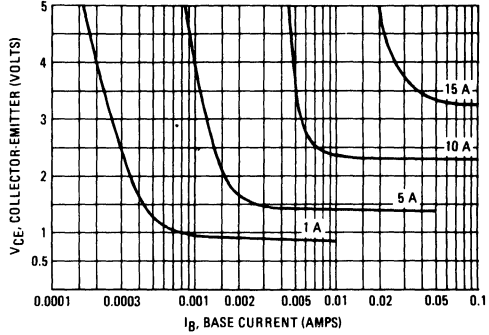


FIGURE 4 – COLLECTOR SATURATION VOLTAGE

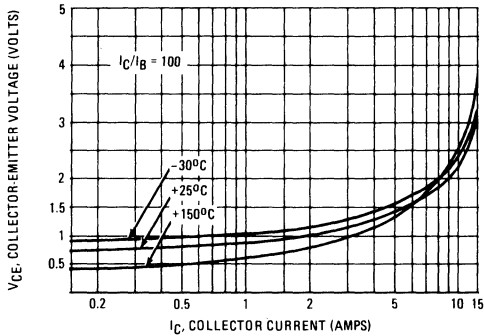


FIGURE 5 – BASE-EMITTER VOLTAGE

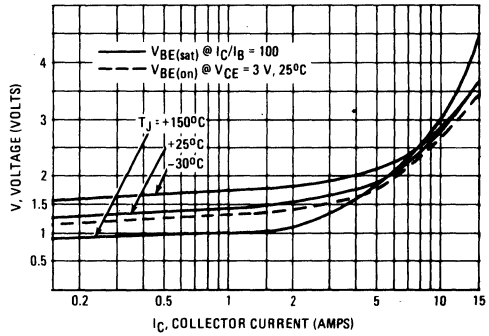
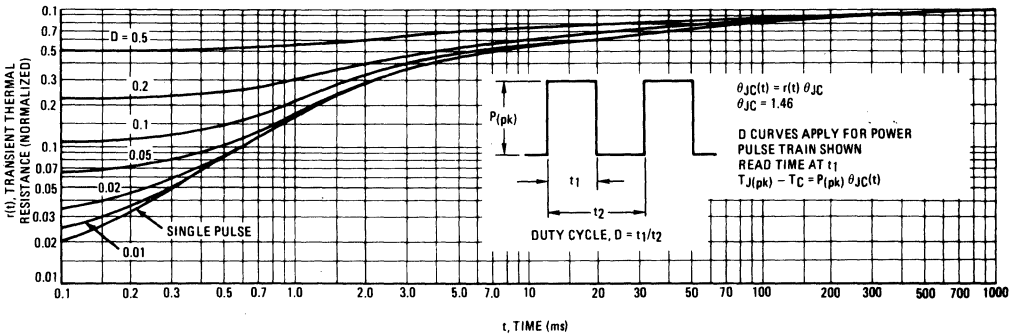


FIGURE 6 – THERMAL RESPONSE



Darlington Silicon Power Transistors

... designed for general-purpose amplifier and low speed switching applications.

- High DC Current Gain — $h_{FE} = 3500$ (Typ) @ $I_C = 4$ Adc
- Collector-Emitter Sustaining Voltage — @ 200 mAdc
 $V_{CE(sus)} = 60$ Vdc (Min) — 2N6667
 $= 80$ Vdc (Min) — 2N6668
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)} = 2$ Vdc (Max) @ $I_C = 5$ Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- Complementary to 2N6387, 2N6388

2N6667
2N6668

PNP SILICON
DARLINGTON
POWER TRANSISTORS

10 AMPERES
60-80 VOLTS
65 WATTS

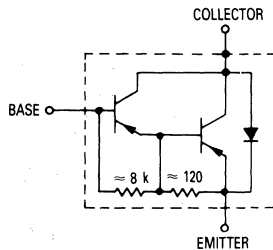
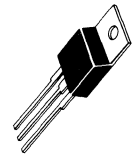


Figure 1. Darlington Schematic



CASE 221A-04
 TO-220AB

***MAXIMUM RATINGS**

Rating	Symbol	2N6667	2N6668	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous — Peak	I_C	10 15		Adc
Base Current	I_B	250		mAdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	65 0.52		watts $W/^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2 0.016		Watts $W/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

* Indicates JEDEC Registered Data

2N6667, 2N6668

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mAdc}$, $I_B = 0$)	2N6667 2N6668	$V_{CE(sus)}$	60 80	— —	Vdc
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 80 \text{ Vdc}$, $I_B = 0$)	2N6667 2N6668	I_{CEO}	— —	1 1	mAdc
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 60 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$)	2N6667 2N6668 2N6667 2N6668	I_{CEX}	— — — —	300 300 3 3	μAdc mAdc
Emitter Cutoff Current ($V_{BE} = 5 \text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	5	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 5 \text{ Adc}$, $V_{CE} = 3 \text{ Vdc}$) ($I_C = 10 \text{ Adc}$, $V_{CE} = 3 \text{ Vdc}$)	h_{FE}	1000 100	20000 —	—
Collector-Emitter Saturation Voltage ($I_C = 5 \text{ Adc}$, $I_B = 0.01 \text{ Adc}$) ($I_C = 10 \text{ Adc}$, $I_B = 0.1 \text{ Adc}$)	$V_{CE(sat)}$	— —	2 3	Vdc
Base-Emitter Saturation Voltage ($I_C = 5 \text{ Adc}$, $I_B = 0.01 \text{ Adc}$) ($I_C = 10 \text{ Adc}$, $I_B = 0.1 \text{ Adc}$)	$V_{BE(sat)}$	— —	2.8 4.5	Vdc

DYNAMIC CHARACTERISTICS

Small-Signal Current Gain ($I_C = 1 \text{ Adc}$, $V_{CE} = 5 \text{ Vdc}$, $f_{test} = 1 \text{ MHz}$)	$ h_{fe} $	20	—	—
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 1 \text{ MHz}$)	C_{ob}	—	200	pF
Small-Signal Current Gain ($I_C = 1 \text{ Adc}$, $V_{CE} = 5 \text{ Vdc}$, $f = 1 \text{ kHz}$)	h_{fe}	1000	—	—

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

R_B & R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
 D_1 , MUST BE FAST RECOVERY TYPES, e.g.,
 MBD5300 USED ABOVE $I_B \approx 100 \text{ mA}$
 MSD6100 USED BELOW $I_B \approx 100 \text{ mA}$

FOR t_d AND t_r , D_1 IS DISCONNECTED AND $V_2 = 0$
 t_r , $t_f \leq 10 \text{ ns}$
 DUTY CYCLE = 1%

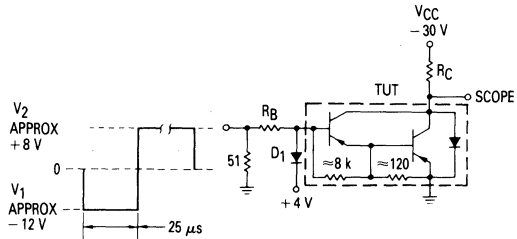


Figure 2. Switching Times Test Circuit

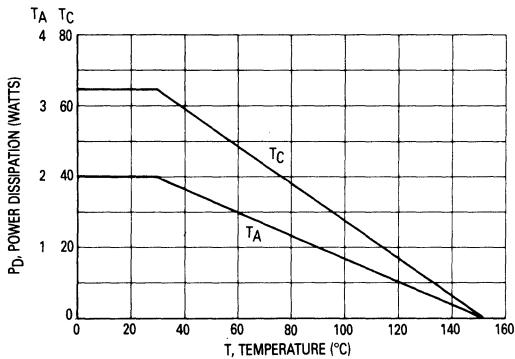


Figure 3. Power Derating

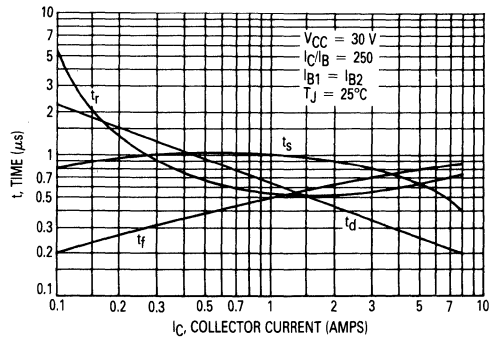


Figure 4. Typical Switching Times

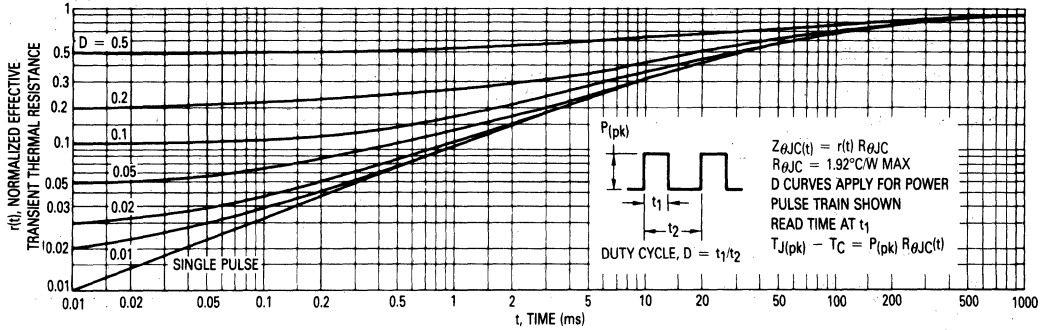


Figure 5. Thermal Response

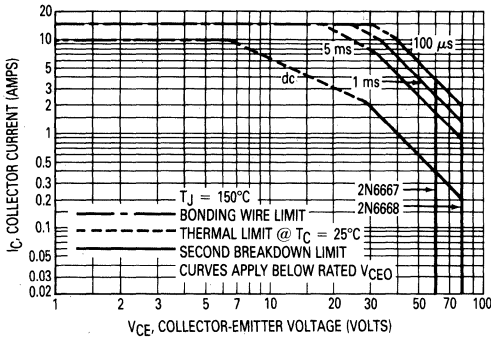


Figure 6. Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

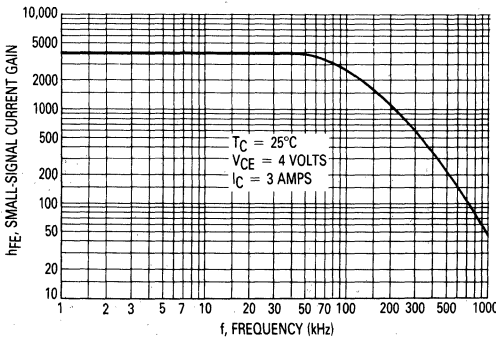


Figure 7. Typical Small-Signal Current Gain

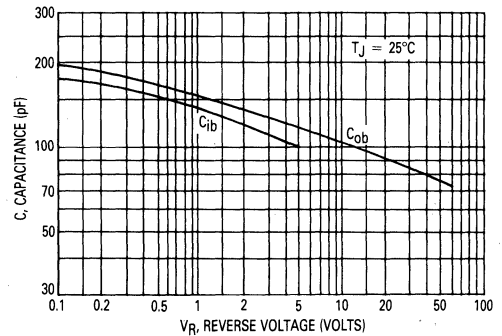


Figure 8. Typical Capacitance

3

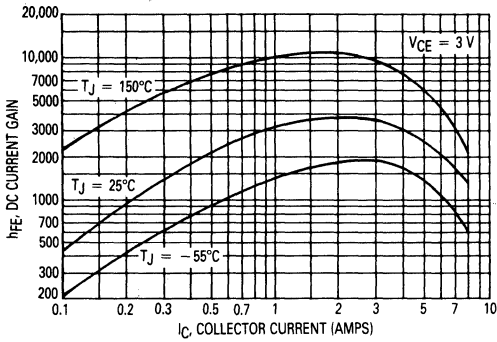


Figure 9. Typical DC Current Gain

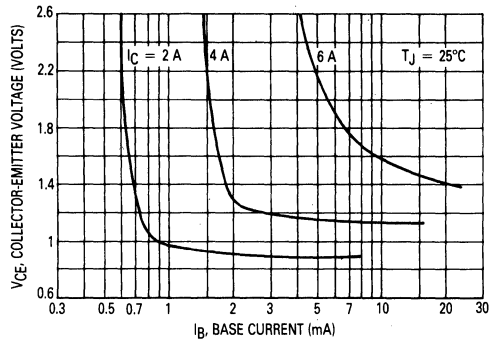


Figure 10. Typical Collector Saturation Region

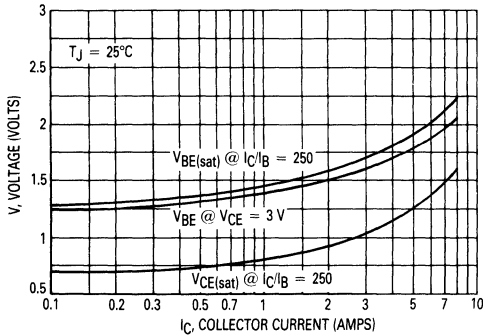


Figure 11. Typical "On" Voltages

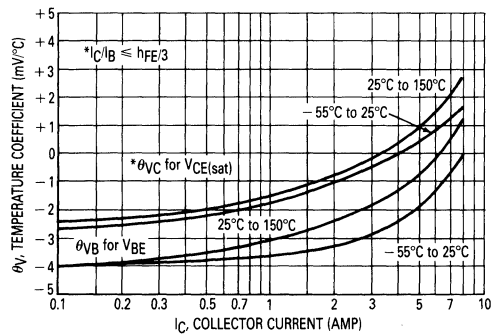


Figure 12. Typical Temperature Coefficients

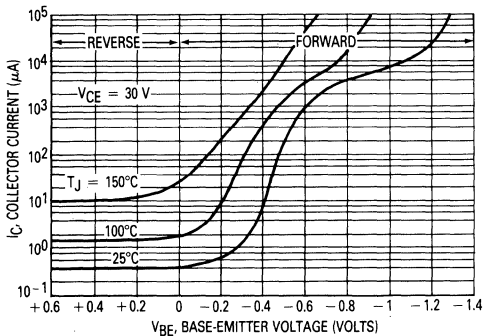


Figure 13. Typical Collector Cut-Off Region

OUTLINE DIMENSIONS

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.86	10.29	0.389	0.405
C	4.07	4.92	0.160	0.190
D	3.64	0.98	0.095	0.039
F	3.81	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.33	0.110	0.155
J	0.38	0.95	0.014	0.037
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	3.54	3.04	0.140	0.120
R	2.04	2.73	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.80	1.27	0.030	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

**CASE 221A-04
TO-220AB**

2N6648
See Page
3-209

NPN Silicon Power Transistors

The 2N6676, 2N6677, 2N6678, MJH6676, MJH6677, and MJH6678 transistors are designed for high voltage switching applications such as:

- Off-Line Supplies
 - Converter Circuits
 - Pulse Width Modulated Regulators
- Specification Features —
- High Voltage Capability
 - Fast Switching Speeds
 - Low Saturation Voltages
 - High SOA Ratings

2N6676
2N6677
2N6678
MJH6676
MJH6677
MJH6678

NPN SILICON
POWER TRANSISTORS

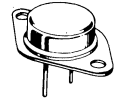
15 AMPERES
300, 350, 400 VOLTS
125 and 175 WATTS

MAXIMUM RATINGS

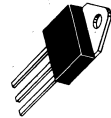
Rating	Symbol	2N6676 MJH6676	2N6677 MJH6677	2N6678 MJH6678	Unit
Collector-Emitter Voltage	V _{CEV}	450	550	650	Vdc
Collector-Emitter Voltage	V _{CEX}	350	400	450	Vdc
Collector-Emitter Voltage	V _{CEO}	300	350	400	Vdc
Emitter-Base Voltage	V _{EBO}	8			Vdc
Collector Current — Continuous	I _C	15			Adc
Collector Current — Peak	I _{CM}	20			
Base Current — Continuous	I _B	5			Adc
Maximum Lead Temperature At Distance > 1/16 in. (1.58 mm) from seating plane for 10 s max		235			°C

MAXIMUM THERMAL RATINGS

Rating	Symbol	2N6676 2N6677 2N6678	MJH6676 MJH6677 MJH6678	Unit
Thermal Resistance Junction to Case	R _{θJC}	1		°C/W
Power Dissipation T _C = 25°C Derate above 25°C	P _T	175 1	125 1	Watts W/°C
Operating and Storage Junction	T _J , T _{stg}	-65 to +200		°C



CASE 1-05
TO-204AA
2N6676
2N6677
2N6678



CASE 340-01
TO-218AC
MJH6676
MJH6677
MJH6678

2N6676, 2N6677, 2N6678
MJH6676, MJH6677, MJH6678

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}, V_{BE(\text{off})} = 1.5 \text{ Vdc}$ ($V_{CE} = \text{Rated } V_{CEV}, V_{BE(\text{off})} = 1.5 \text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	0.1	mA	
Emitter Cutoff Current ($V_{EB} = 8 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	2	mA	
Collector-Emitter Sustaining Voltage ($I_C = 200 \text{ mA}, I_B = 0$)	2N6676, MJH6676 2N6677, MJH6677 2N6678, MJH6678	$V_{CEO(\text{sus})}$	300 350 400	— — —	Vdc
Collector-Emitter Sustaining Voltage ($I_C = 15 \text{ A}, V_{CE(\text{pk})} = V_{\text{clamp}} = \text{Rated } V_{CEX}$)	2N6676, MJH6676 2N6677, MJH6677 2N6678, MJH6678	$V_{CEX(\text{sus})}$	350 400 450	— — —	Vdc

SECOND BREAKDOWN

Second Breakdown Collector with Base Forward Biased	$I_{S/b}$	See Figure 1
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 2

ON CHARACTERISTICS

DC Current Gain ($I_C = 15 \text{ A}, V_{CE} = 3 \text{ V}$)	h_{FE}	8	—	—
Base-Emitter Saturation Voltage ($I_C = 15 \text{ A}, I_B = 3 \text{ A}$)	$V_{BE(\text{sat})}$	—	1.5	Vdc
Collector-Emitter, Saturation Voltage ($I_C = 15 \text{ A}, I_B = 3 \text{ A}$) ($I_C = 15 \text{ A}, I_B = 3 \text{ A}, T_C = 100^\circ\text{C}$)	$V_{CE(\text{sat})}$	—	1.5 2	Vdc

DYNAMIC CHARACTERISTICS

Current Gain ($I_C = 1 \text{ A}, V_{CE} = 10 \text{ Vdc}, f = 5 \text{ MHz}$)	$ h_{fe} $	3	10	—
Output Capacitance ($I_C = 1 \text{ A}, V_{CB} = 10 \text{ Vdc}, f = 0.1 \text{ MHz}$)	C_{ob}	150	500	pF

SWITCHING CHARACTERISTICS

Resistive Load								
Delay Time	$V_{CC} = 200 \text{ V}, I_C = 15 \text{ A},$ $I_{B1} = I_{B2} = 3 \text{ A}, t_p = 20 \mu\text{s},$ Duty Cycle $\leq 2\%$ $V_{B2} = 6 \text{ V}, R_L = 13.5 \Omega$ (See Figure 3)	$T_C = 25^\circ\text{C}$	t_d	—	0.1	μs		
Rise Time			t_r	—	0.6			
Storage Time			t_s	—	2.5			
Fall Time			t_f	—	0.5			
Delay Time			t_d	—	0.4			
Rise Time		t_r	—	1				
Storage Time		t_s	—	4				
Fall Time		t_f	—	1				
Inductive Load								
Cross Over Time		$L = 50 \mu\text{H}$ $V_{CE(\text{pk})} = V_{\text{clamp}} = \text{Rated } V_{CEX}$ (See Figure 3)	$T_C = 25^\circ\text{C}$	t_c	—		0.5	μs
	$T_C = 100^\circ\text{C}$		—		0.8			

2N6676, 2N6677, 2N6678 MJH6676, MJH6677, MJH6678

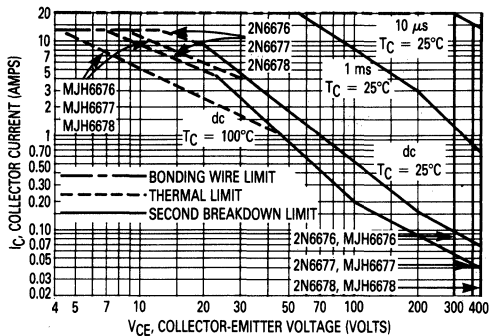


Figure 1. Maximum Rated Forward Biased Safe Operating Area

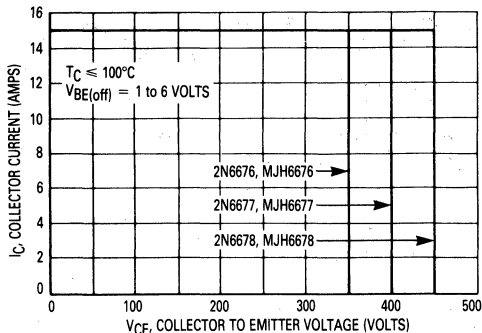


Figure 2. Maximum Rated Reverse Biased Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^\circ\text{C}$ and $T_C = 100^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 2 gives the RBSOA characteristics.

OUTLINE DIMENSIONS

3

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.130	0.210
V	3.81	4.19	0.151	0.165

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
⊕ 0.13 (0.005) ⊙ T V ⊙
FOR LEADS:
⊕ 0.13 (0.005) ⊙ T V ⊙ Q ⊙
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

**CASE 1-05
TO-204AA
(Formerly TO-3)
2N6676 thru 2N6678**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
F	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

**CASE 340-01
TO-218AC
MJH6676 thru MJH6678**

**2N6676, 2N6677, 2N6678
MJH6676, MJH6677, MJH6678**

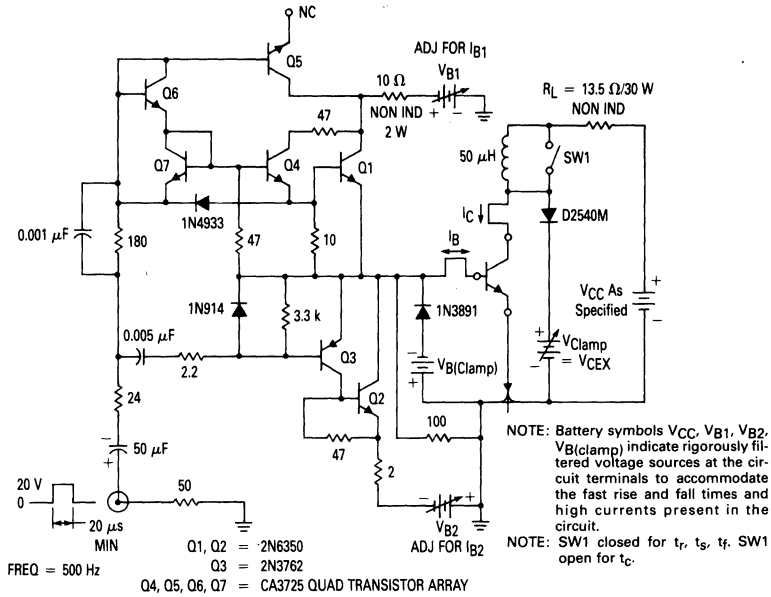
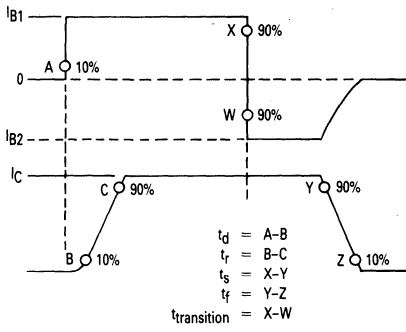


Figure 3. Switching Times Test Circuit



NOTE: TRANSITION TIME FROM 90% I_{B1} to 90% I_{B2} MUST BE LESS THAN 0.5 μs .

Figure 4. Switching Time Measurements

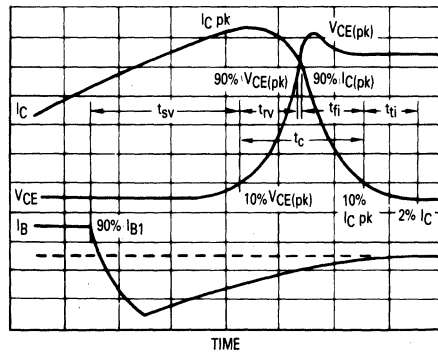


Figure 5. Inductive Switching Measurements

2N6833
2N6834

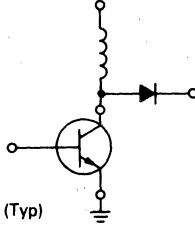
Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

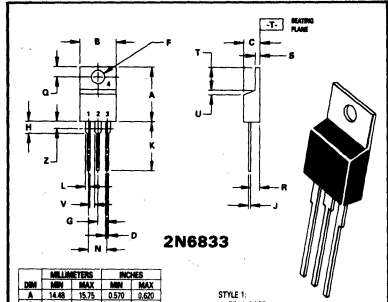
These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 50 ns Inductive Fall Time — 75°C (Typ)
 - 70 ns Inductive Crossover Time — 75°C (Typ)
 - 500 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +150°C
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents



5.0 AMPERE
NPN SILICON
POWER TRANSISTORS
450 VOLTS
80 and 125 WATTS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.46	15.75	0.570	0.620
B	9.98	10.20	0.390	0.405
C	4.07	4.82	0.160	0.190
D	0.94	0.98	0.037	0.039
E	1.81	3.73	0.071	0.147
F	2.42	3.06	0.095	0.120
G	1.90	3.83	0.075	0.150
H	0.46	0.71	0.018	0.028
I	1.15	1.29	0.045	0.051
J	12.70	14.27	0.500	0.562
K	1.15	1.29	0.045	0.051
L	4.83	5.33	0.190	0.210
M	2.54	3.04	0.100	0.120
N	2.04	2.79	0.080	0.110
O	1.15	1.29	0.045	0.051
P	5.07	6.47	0.200	0.255
Q	0.62	1.27	0.025	0.050
R	1.15	—	0.045	—
S	—	2.04	—	0.080

STYLE 1:
 PN 1 BASE
 2 COLLECTOR
 3 EMITTER
 4 COLLECTOR

NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MAXIMUM RATINGS

Rating	Symbol	2N6833	2N6834	Unit
Collector-Emitter Voltage*	V _{CEO(sus)}	450		Vdc
Collector-Emitter Voltage*	V _{CEV}	850		Vdc
Emitter Base Voltage*	V _{EB}	6.0		Vdc
Collector Current — Continuous*	I _C	5.0		Adc
— Peak (1)	I _{CM}	10		
Base Current — Continuous*	I _B	4.0		Adc
— Peak (1)	I _{BM}	8.0		
Total Power Dissipation @ T _C = 25°C*	P _D	80	125	Watts
— @ T _C = 100°C*		32	71.5	
Derate above 25°C*		0.64	0.714	W/°C
Operating and Storage Junction Temperature Range*	T _J , T _{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

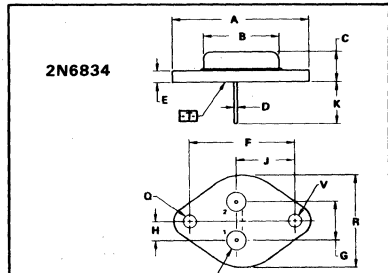
Characteristic	Symbol	2N6833	2N6834	Unit
Thermal Resistance, Junction to Case*	R _{θJC}	1.56	1.40	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds*	T _L	275		°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
 *Indicate JEDEC Registered Data

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

CASE 221A-04
TO-220AB



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.57	1.05	0.023	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.45 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	25.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA (Formerly TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450*	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25* 1.5*	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0*	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figures 15* and 16*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 17			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 1.5\text{ Adc}$, $I_B = 0.15\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	1.0 2.5* 2.5*	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.5* 1.5	Vdc
DC Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$) ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.5* 5.0	—	30* —	—

DYNAMIC CHARACTERISTICS (2)

Current Gain - Bandwidth Product ($V_{CE} = 10\text{ Vdc}$, $I_C = 0.25\text{ Adc}$, $f_{test} = 10\text{ MHz}$)	f_T	15*	—	75*	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	20*	—	200*	pF

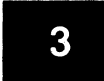
SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	($I_C = 3.0\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 0.4\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	($I_{B2} = 0.8\text{ Adc}$, $R_{B2} = 8.0\ \Omega$)	t_d	—	30	100*	ns
Rise Time			t_r	—	100	300*	
Storage Time			t_s	—	1000	3000*	
Fall Time			t_f	—	60	300*	
Storage Time			t_s	—	400	—	
Fall Time			t_f	—	130	—	
Inductive Load (Table 2)							
Storage Time	($I_C = 3.0\text{ Adc}$, $I_{B1} = 0.4\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	$(T_C = 100^\circ\text{C})$	t_{sv}	—	500	1600*	ns
Fall Time			t_{fi}	—	100	200*	
Crossover Time			t_c	—	120	250*	
Storage Time		$(T_C = 150^\circ\text{C})$	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	

(1) Pulse Test: PW - 300 μs , Duty Cycle $\leq 2\%$.

(2) $f_T = |h_{fe}| f_{test}$

*Indicates JEDEC Registered Limit



TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

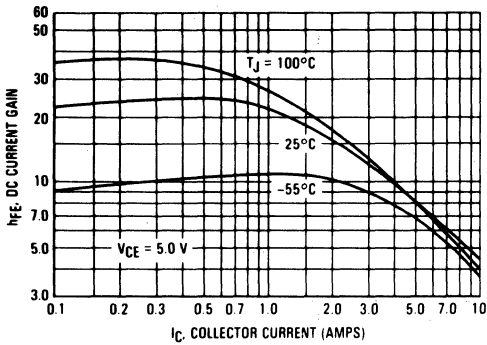


FIGURE 2 — COLLECTOR SATURATION REGION

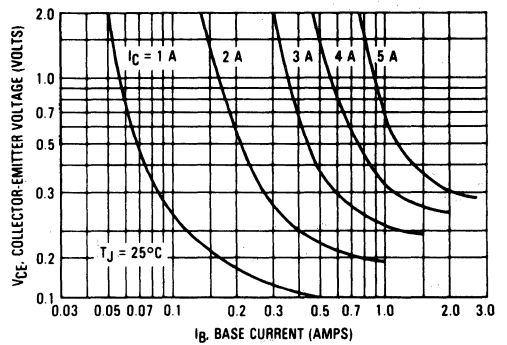


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

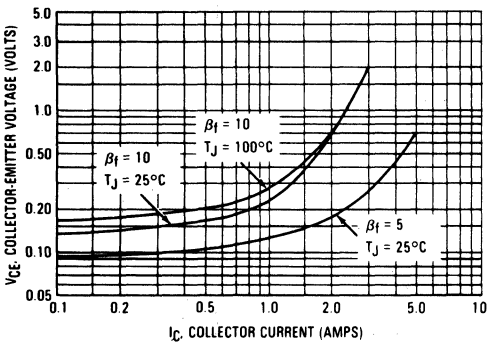


FIGURE 4 — BASE-EMITTER VOLTAGE

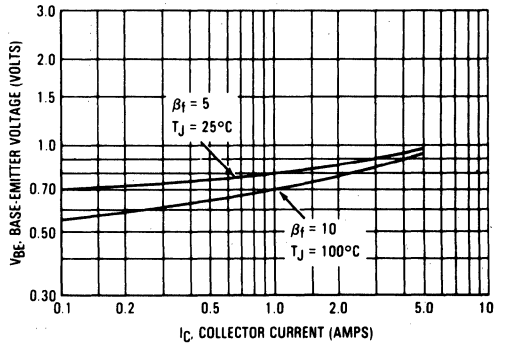


FIGURE 5 — COLLECTOR CUTOFF REGION

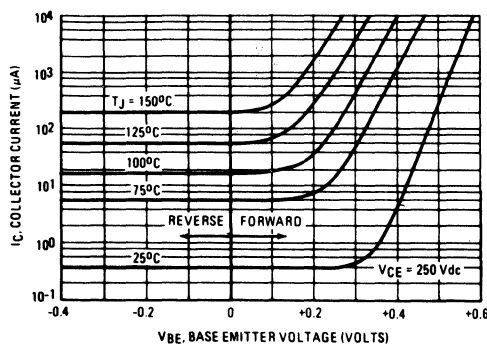
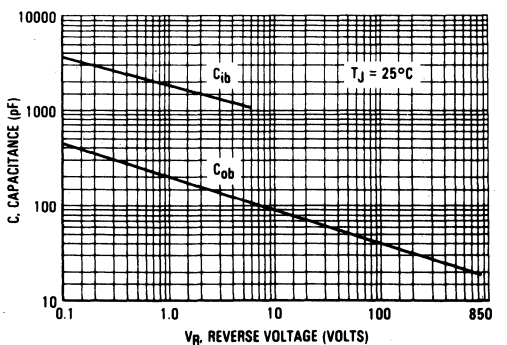


FIGURE 6 — CAPACITANCE



3

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

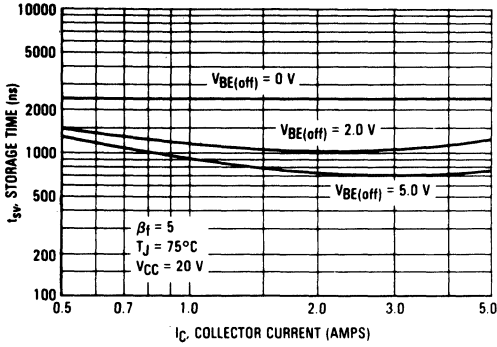


FIGURE 8 — STORAGE TIME

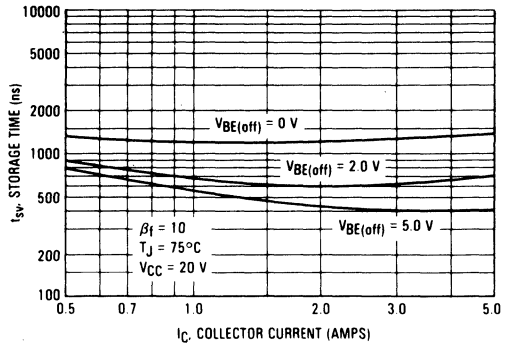


FIGURE 9 — COLLECTOR CURRENT FALL TIME

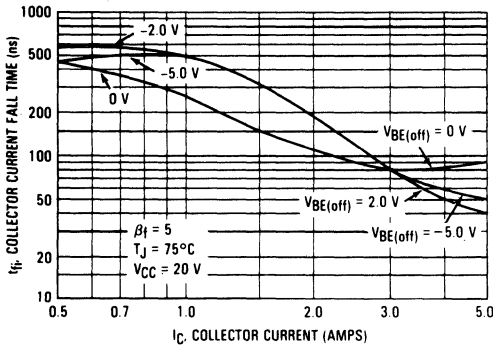


FIGURE 10 — COLLECTOR CURRENT FALL TIME

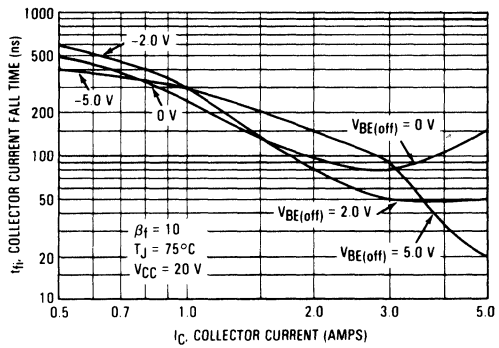


FIGURE 11 — CROSSOVER TIME

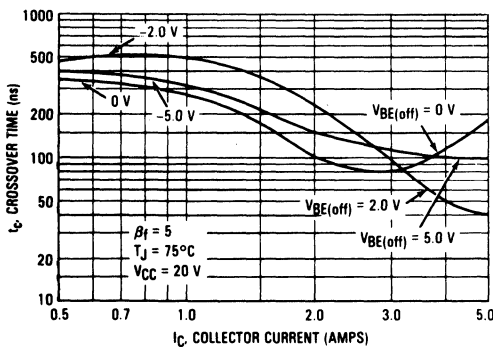


FIGURE 12 — CROSSOVER TIME

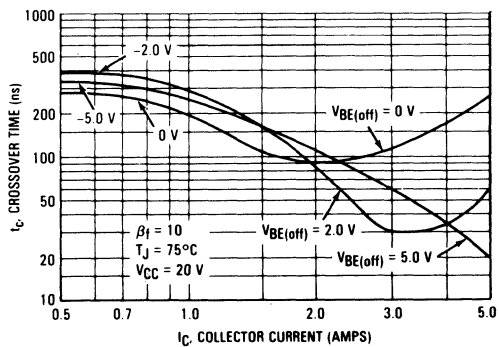


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

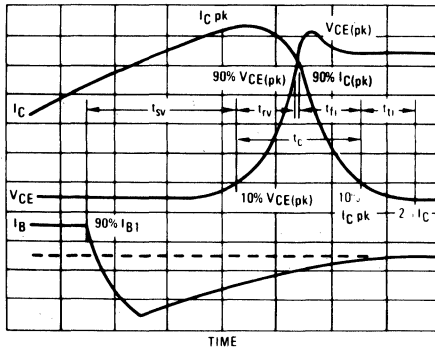
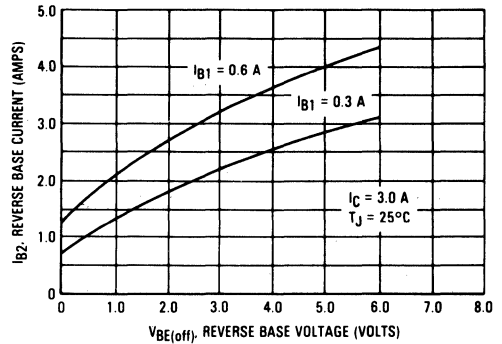


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA (2N6833)

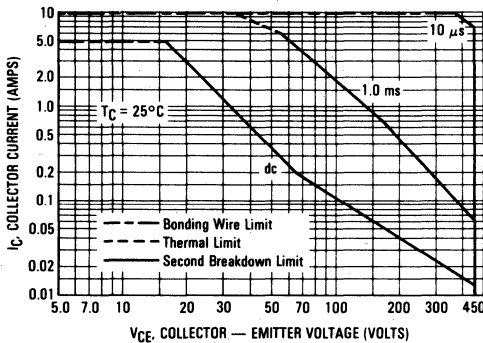
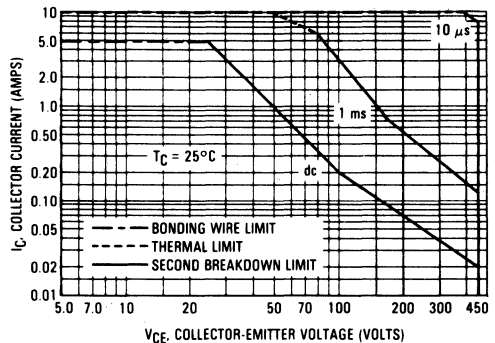


FIGURE 16 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA (2N6834)



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 15 and 16 are based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 15 and 16 may be found at any case temperature by using the appropriate curve on Figures 18 or 19.

$T_J(\text{pk})$ may be calculated from the data in Figures 20 or 21. At high case temperatures, thermal limitations will

reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable putting reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

FIGURE 17 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA

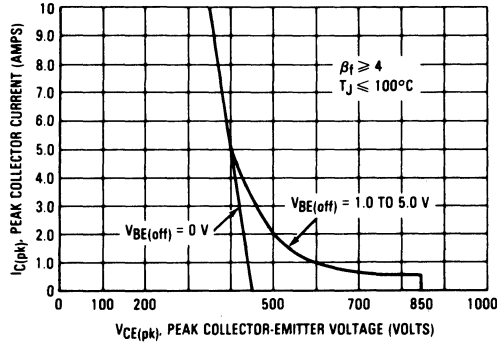


FIGURE 18 — POWER DERATING (2N6833)

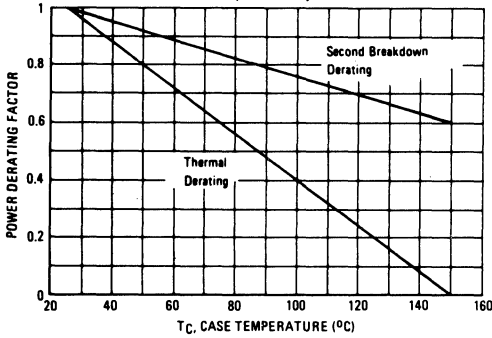


FIGURE 19 — POWER DERATING (2N6834)

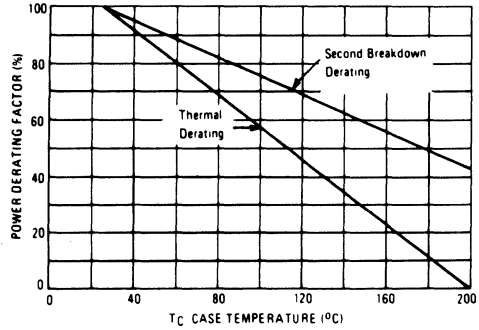
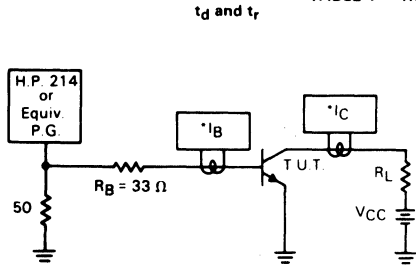
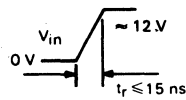


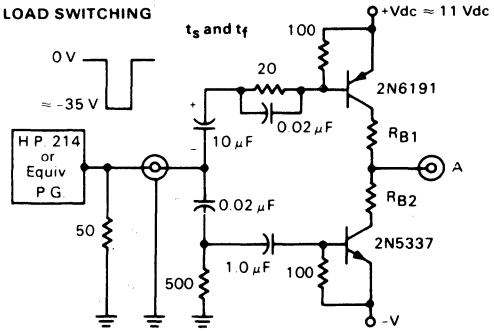
TABLE 1 — RESISTIVE LOAD SWITCHING



$V_{CC} = 250 \text{ Vdc}$
 $R_L = 83 \Omega$
 $I_C = 3.0 \text{ Adc}$
 $I_B = 0.4 \text{ Adc}$



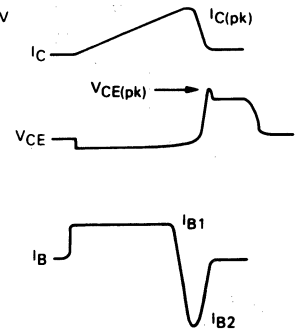
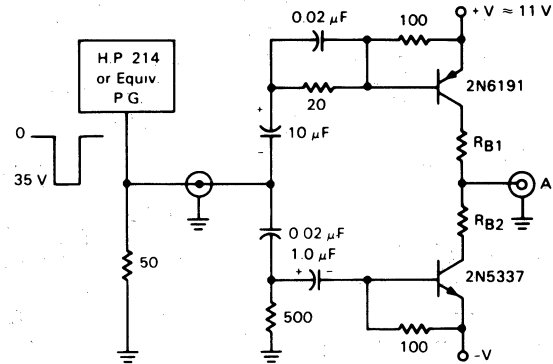
*Tektronix P-6042 or Equivalent



$V_{CC} = 250$
 $R_L = 83 \Omega$
 $I_C = 3.0 \text{ Adc}$
 $I_{B1} = 0.4 \text{ Adc}$
 $I_{B2} = 0.8 \text{ Adc}$
 $R_{B1} = 33 \Omega$
 $R_{B2} = 8.0 \Omega$
 For $V_{BE}(\text{off}) = 5.0 \text{ V}$ $R_{B2} = 0 \Omega$

*Note: Adjust -V to obtain desired $V_{BE}(\text{off})$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



$$T_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

V(BR)CEO
 L = 10 mH
 $R_{B2} = \infty$
 $V_{CC} = 20$ Volts

Inductive Switching
 L = 200 μ H
 $R_{B2} = 0$
 $V_{CC} = 20$ Volts
 R_{B1} selected for desired I_{B1}

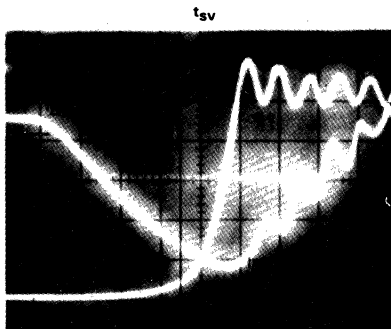
RBSOA
 L = 200 μ H
 $R_{B2} = 0$
 $V_{CC} = 20$ Volts
 R_{B1} selected for desired I_{B1}

*Tektronix
 P-6042 or
 Equivalent

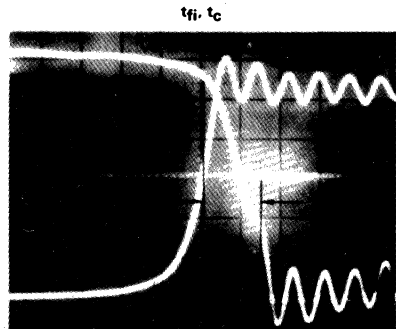
Scope - Tektronix
 7403 or
 Equivalent

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS



$I_{C(pk)} = 3.0$ Amps
 $I_{B1} = 0.4$ Amp
 $V_{BE(off)} = 5.0$ Volts
 $V_{CE(pk)} = 400$ Volts
 $T_C = 25^\circ C$
 Time Base =
 20 ns/cm



$I_{C(pk)} = 3.0$ Amps
 $I_{B1} = 0.4$ Amp
 $V_{BE(off)} = 5.0$ Volts
 $V_{CE(pk)} = 400$ Volts
 $T_C = 25^\circ C$
 Time Base =
 20 ns/cm

THERMAL RESPONSE

FIGURE 20 — 2N6833

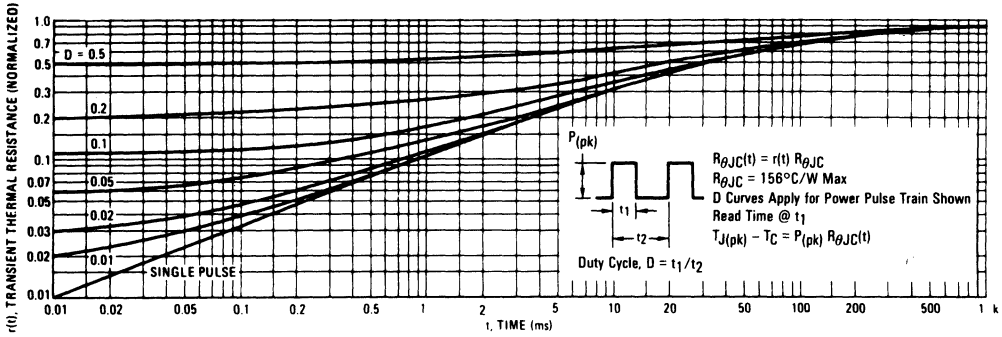
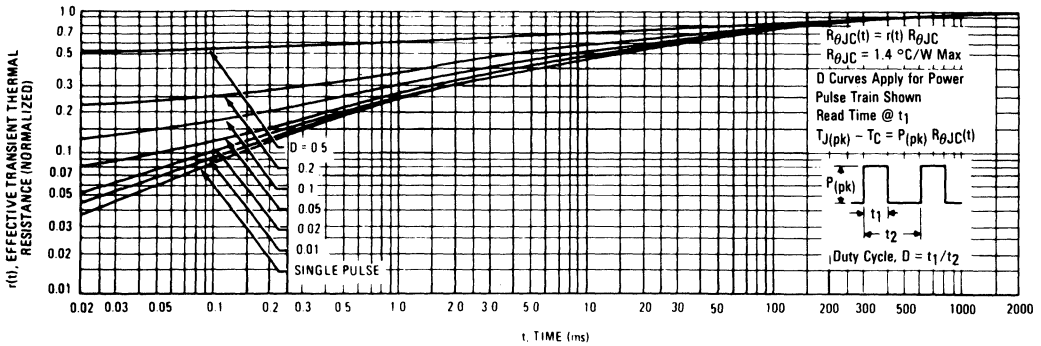


FIGURE 21 — 2N6834



2N6835

Designer's Data Sheet

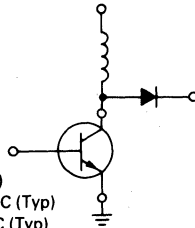
**SWITCHMODE III SERIES
 ULTRA-FAST NPN SILICON POWER TRANSISTORS**

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

- Switching Regulators
- Inverters
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times

90 ns Inductive Fall Time — 75°C (Typ)
 90 ns Inductive Crossover Time — 75°C (Typ)
 450 ns Inductive Storage Time — 75°C (Typ)

- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
 Reverse-Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents

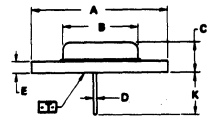
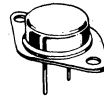


**8 AMPERE
 NPN SILICON
 POWER TRANSISTORS**

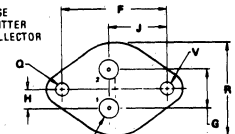
**450 VOLTS
 150 WATTS**

**Designer's Data for
 "Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR



- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. [E] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
 ⌀ .13 (0.005) T V ⊕ ⊙
 FOR LEADS:
 ⌀ .13 (0.005) ⊕ T V ⊕ ⊙ ⊕
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.03	0.039	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.87	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

**CASE 1-05
 TO-204AA Type
 (TO-3 Type)**

***MAXIMUM RATINGS**

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
— Peak (1)	I_{CM}	16	
Base Current — Continuous	I_B	6.0	Adc
— Peak (1)	I_{BM}	12	
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	150	Watts
@ $T_C = 100^\circ C$		85.5	
Derate above 25°C		0.86	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5.0 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

*Indicate JEDEC Registered Data

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25* 1.5*	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE(off)} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0*	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.40\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 0.66\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 0.66\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	1.2 2.5* 3.0*	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.66\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 0.66\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.5* 1.5	Vdc
DC Current Gain ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$) ($I_C = 8.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.5* 4.0*	—	30*	—

DYNAMIC CHARACTERISTICS (2)

Current Gain - Bandwidth Product ($V_{CE} = 10\text{ Vdc}$, $I_C = 0.25\text{ Adc}$, $f_{test} = 10\text{ MHz}$)	f_T	10*	—	75*	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	50*	—	350*	pF

SWITCHING CHARACTERISTICS**Resistive Load (Table 1)**

Delay Time	($I_C = 5.0\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 0.66\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	($I_{B2} = 1.3\text{ Adc}$, $R_{B2} = 4.0\ \Omega$)	t_d	—	20	50*	ns
Rise Time			t_r	—	85	250*	
Storage Time			t_s	—	1000	2500*	
Fall Time			t_f	—	70	250*	
Storage Time		($V_{BE(off)} = 5.0\text{ Vdc}$)	t_s	—	500	—	
Fall Time			t_f	—	100	—	

Inductive Load (Table 2)

Storage Time	($I_C = 5.0\text{ Adc}$, $I_{B1} = 0.66\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	($T_C = 100^\circ\text{C}$)	t_{sv}	—	700	1800*	ns
Fall Time			t_{fi}	—	80	200*	
Crossover Time		($T_C = 150^\circ\text{C}$)	t_c	—	150	250*	
Storage Time			t_{sv}	—	800	—	
Fall Time			t_{fi}	—	80	—	
Crossover Time			t_c	—	200	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.(2) $f_T = |s_{he}| f_{test}$

*Indicates JEDEC Registered Limit

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

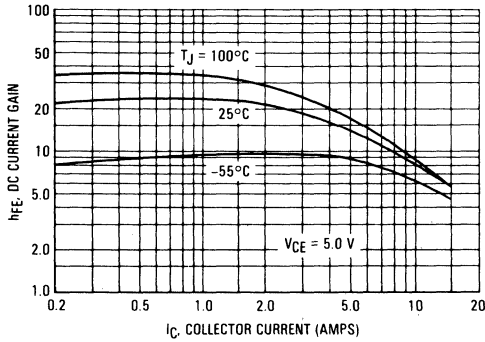


FIGURE 2 — COLLECTOR SATURATION REGION

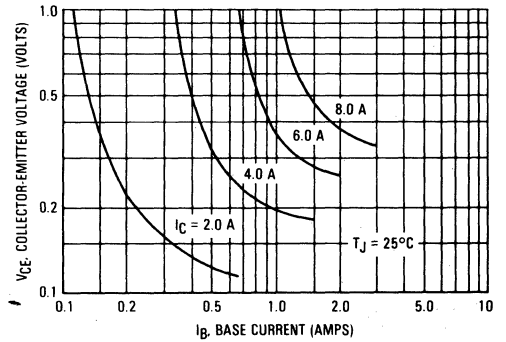


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

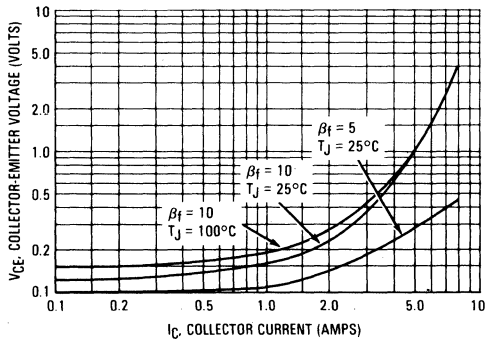


FIGURE 4 — BASE-EMITTER VOLTAGE

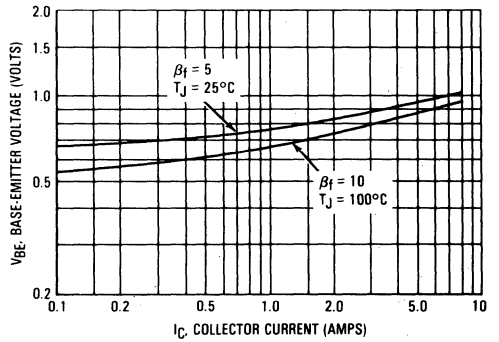


FIGURE 5 — COLLECTOR CUTOFF REGION

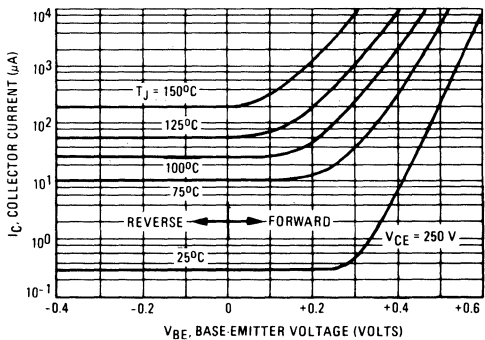
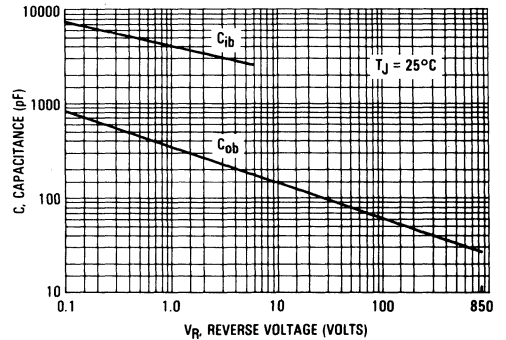


FIGURE 6 — CAPACITANCE



3

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

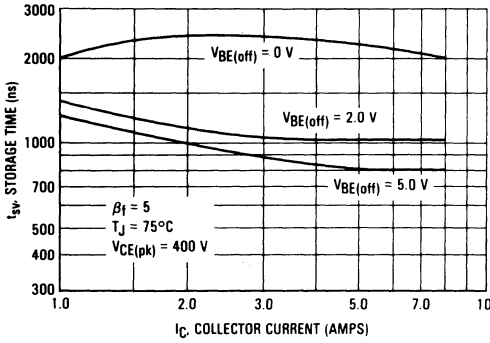


FIGURE 8 — STORAGE TIME

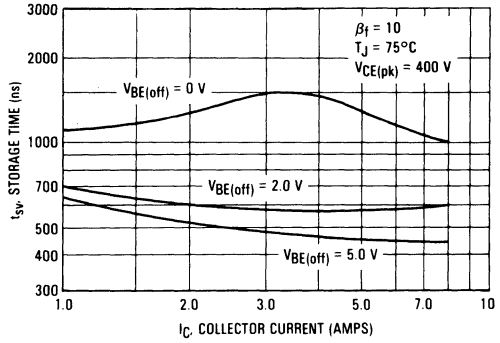


FIGURE 9 — COLLECTOR CURRENT FALL TIME

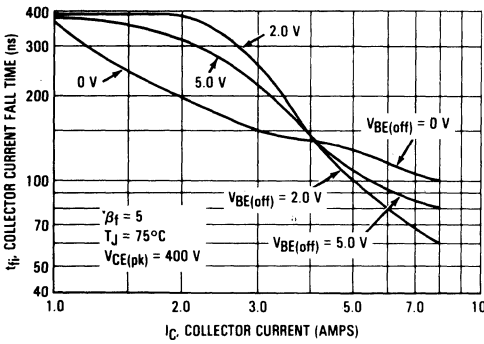


FIGURE 10 — COLLECTOR CURRENT FALL TIME

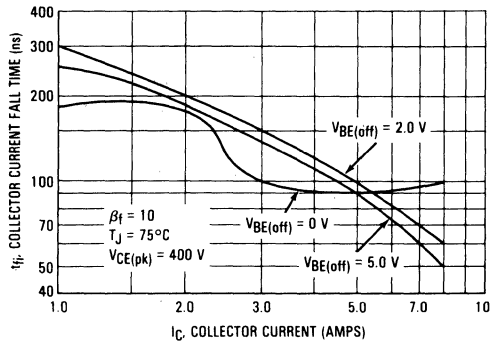


FIGURE 11 — CROSSOVER TIME

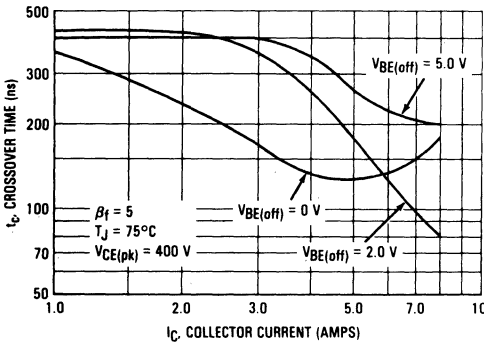


FIGURE 12 — CROSSOVER TIME

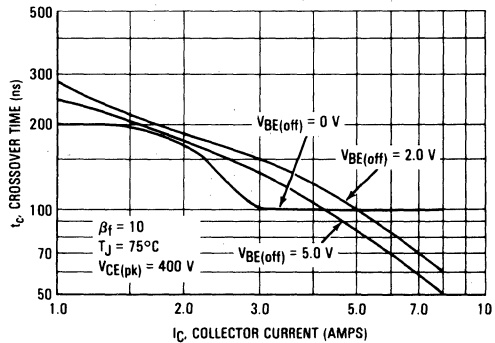


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

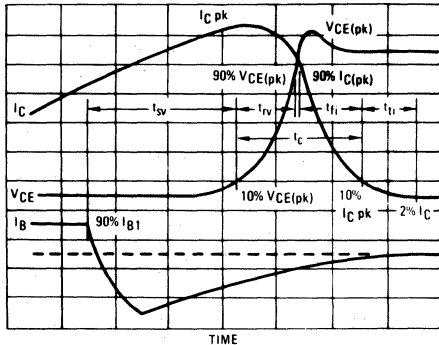
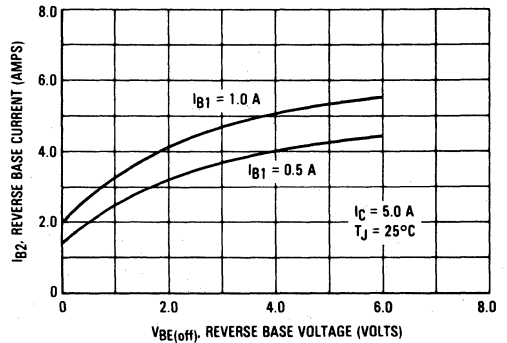


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

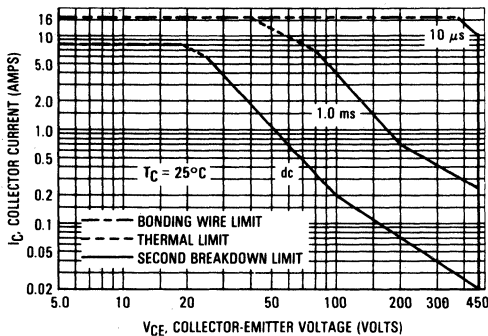
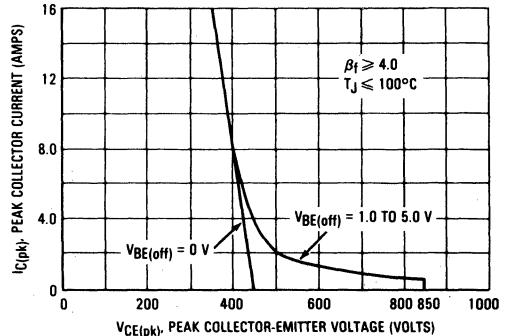


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce

the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

3

FIGURE 17 — THERMAL RESPONSE

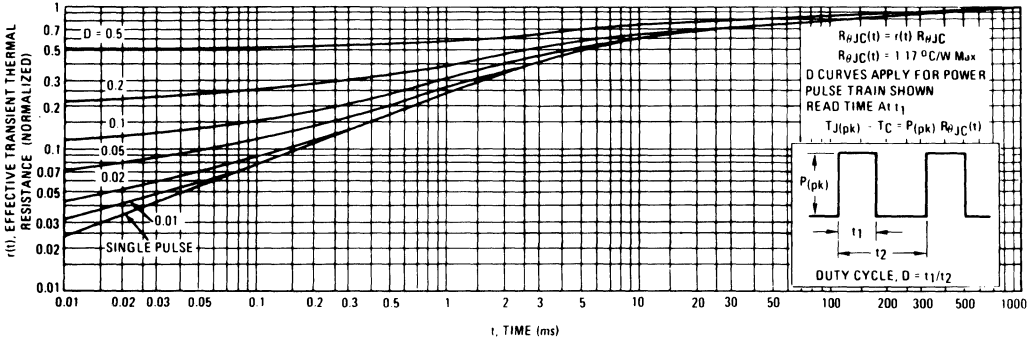


FIGURE 18 — POWER DERATING

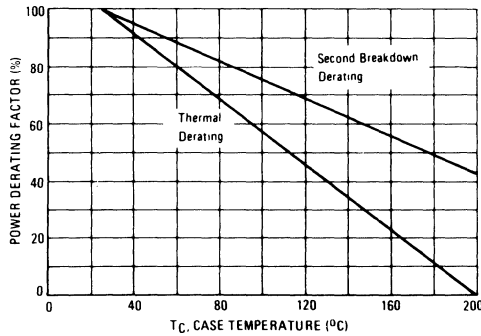
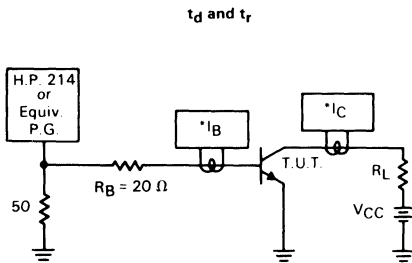
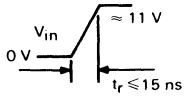


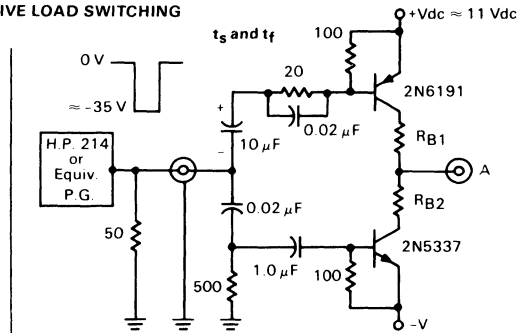
TABLE 1 — RESISTIVE LOAD SWITCHING



$V_{CC} = 250 \text{ Vdc}$
 $R_L = 50 \Omega$
 $I_C = 5.0 \text{ Adc}$
 $I_B = 0.5 \text{ Adc}$



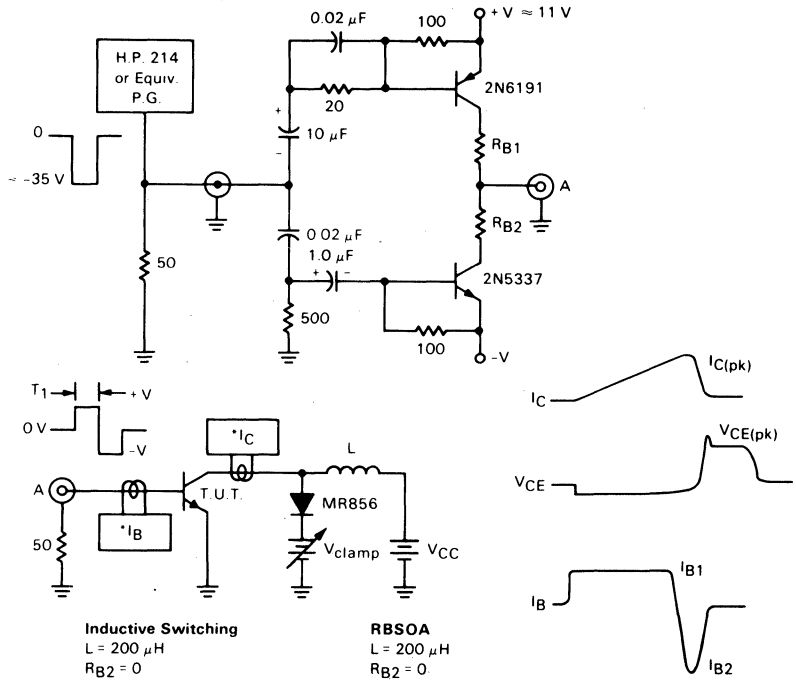
*Tektronix
 P-6042 or
 Equivalent



$V_{CC} = 250 \text{ Vdc}$ $I_{B1} = 0.5 \text{ Adc}$ $R_{B1} = 20 \Omega$
 $R_L = 50 \Omega$ $I_{B2} = 1.0 \text{ Adc}$ $R_{B2} = 4.0 \Omega$
 $I_C = 5.0 \text{ Adc}$ For $V_{BE(off)} = 5.0 \text{ V}$ $R_{B2} = 0 \Omega$

*Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



$$T_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$$

T₁ adjusted to obtain I_{C(pk)}

V(BR)CEO
 L = 10 mH
 R_{B2} = ∞
 V_{CC} = 20 Volts

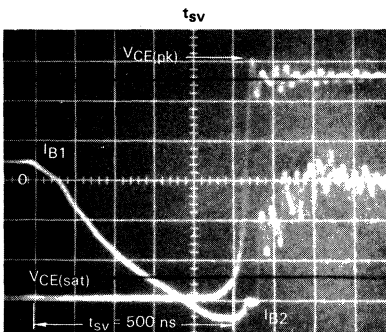
Inductive Switching
 L = 200 μH
 R_{B2} = 0
 V_{CC} = 20 Volts
 R_{B1} selected for desired I_{B1}

Scope - Tektronix
 7403 or
 Equivalent

RBSOA
 L = 200 μH
 R_{B2} = 0
 V_{CC} = 20 Volts
 R_{B1} selected for desired I_{B1}

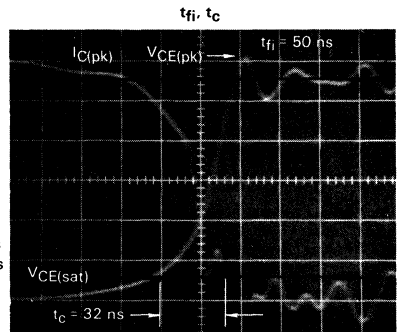
Note: Adjust -V to obtain desired V_{BE(off)} at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS



I_{C(pk)} = 5.0 Amps
 I_{B1} = 0.5 Amp
 V_{BE(off)} = 5.0 Volts
 V_{CE(pk)} = 400 Volts
 T_C = 25°C
 Time Base =
 100 ns/cm

I_{C(pk)} = 5.0 Amps
 I_{B1} = 0.5 Amp
 V_{BE(off)} = 5.0 Volts
 V_{CE(pk)} = 400 Volts
 T_C = 25°C
 Time Base =
 20 ns/cm



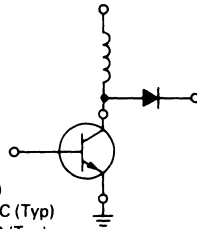
2N6836

Designer's Data Sheet

**SWITCHMODE III SERIES
 ULTRA-FAST NPN SILICON POWER TRANSISTORS**

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

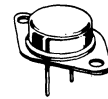
- Switching Regulators
- Inverters
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 30 ns Inductive Fall Time — 75°C (Typ)
 - 50 ns Inductive Crossover Time — 75°C (Typ)
 - 600 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents



15 AMPERE
NPN SILICON
POWER TRANSISTORS
450 VOLTS
175 WATTS

**Designer's Data for
 "Worst Case" Conditions**

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



***MAXIMUM RATINGS**

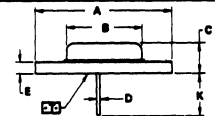
Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V _{CEO(sus)}	450	Vdc
Collector-Emitter Voltage	V _{CEV}	850	Vdc
Emitter Base Voltage	V _{EB}	6.0	Vdc
Collector Current — Continuous	I _C	15	A
— Peak (1)	I _{CM}	20	A
Base Current — Continuous	I _B	10	A
— Peak (1)	I _{BM}	15	A
Total Power Dissipation	P _D	175	Watts
@ T _C = 25°C		100	
@ T _C = 100°C		1.0	
Derate above 25°C			
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200	°C

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.0	°C/W
Maximum Lead Temperature for Soldering	T _L	275	°C
Purposes: 1/8" from Case for 5.0 Seconds			

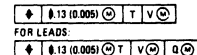
(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

*Indicate JEDEC Registered Data



STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. [T] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D:



4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	28.37	—	1.1150
B	—	21.08	—	0.8300
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	20.15	BSC	—	0.790
G	10.92	BSC	—	0.430
H	5.46	BSC	—	0.215
J	16.80	BSC	—	0.660
K	11.18	12.18	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	26.67	—	1.050
N	4.83	5.33	0.190	0.210
O	3.81	4.19	0.150	0.165

CASE 1-05
 TO-204AA Type
 (TO-3 Type)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25* 1.5*	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0*	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.7\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	1.2 2.5* 3.0*	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.5* 1.5	Vdc
DC Current Gain ($I_C = 10\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$) ($I_C = 15\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	8.0* 5.0	—	30*	—

DYNAMIC CHARACTERISTICS (2)

Current Gain - Bandwidth Product ($V_{CE} = 10\text{ Vdc}$, $I_C = 0.25\text{ Adc}$, $f_{test} = 10\text{ MHz}$)	f_T	10*	—	75*	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	50*	—	400*	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	$(I_C = 10\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 1.0\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	$(I_{B2} = 2.6\text{ Adc}$, $R_{B2} = 1.6\ \Omega)$	t_d	—	20	100*	ns
Rise Time			t_r	—	200	500*	
Storage Time			t_s	—	1200	3000*	
Fall Time		t_f	—	200	250*		
Storage Time		$(V_{BE(off)} = 5.0\text{ Vdc})$	t_s	—	650	—	
Fall Time	t_f		—	80	—		
Inductive Load (Table 2)							
Storage Time	$(I_C = 10\text{ Adc}$, $I_{B1} = 1.0\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	$(T_C = 100^\circ\text{C})$	t_{sv}	—	800	1500*	ns
Fall Time			t_{fi}	—	50	150*	
Crossover Time			t_c	—	90	200*	
Storage Time		$(T_C = 150^\circ\text{C})$	t_{sv}	—	1050	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.(2) $t_T = |s_{he}| f_{test}$.

*Indicates JEDEC Registered Limit

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

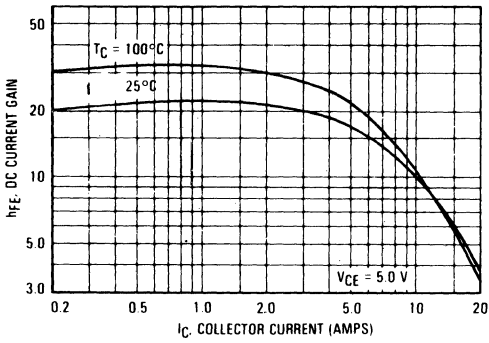


FIGURE 2 — COLLECTOR SATURATION REGION

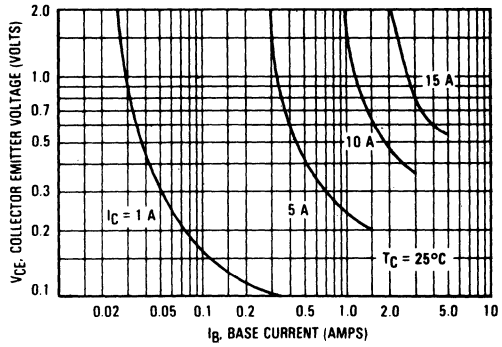


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

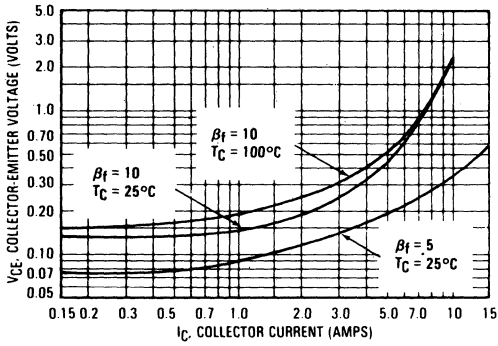


FIGURE 4 — BASE-EMITTER VOLTAGE

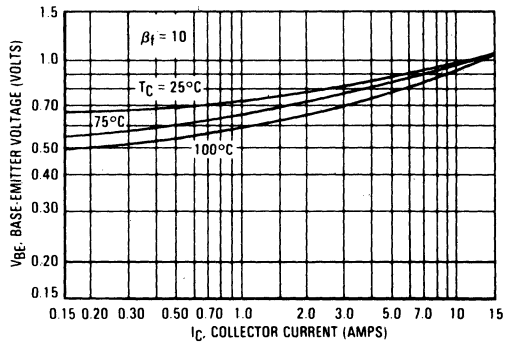


FIGURE 5 — COLLECTOR CUTOFF REGION

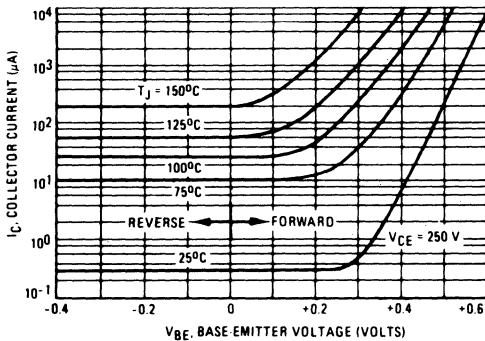
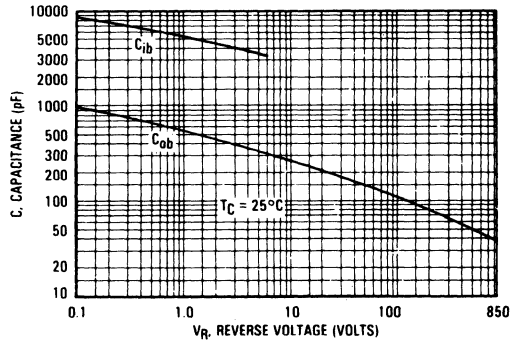


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

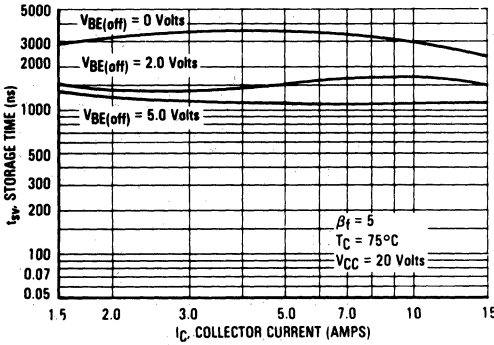


FIGURE 8 — STORAGE TIME

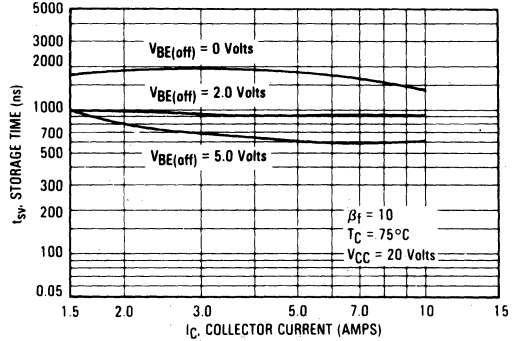


FIGURE 9 — COLLECTOR CURRENT FALL TIME

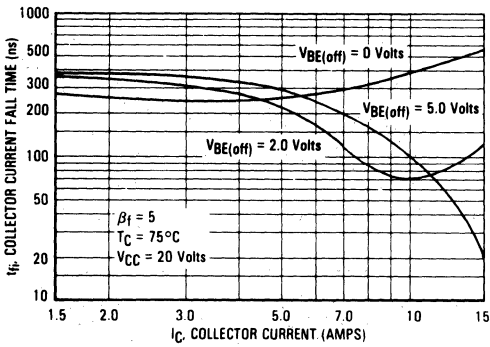


FIGURE 10 — COLLECTOR CURRENT FALL TIME

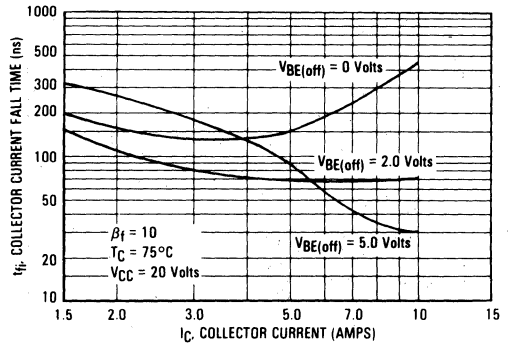


FIGURE 11 — CROSSOVER TIME

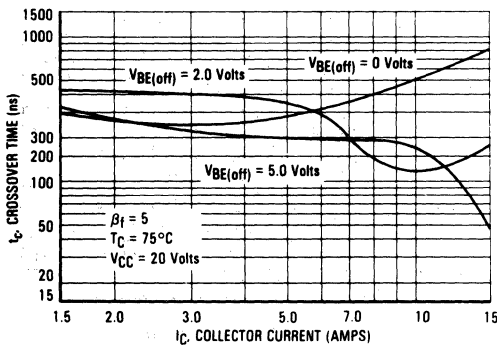
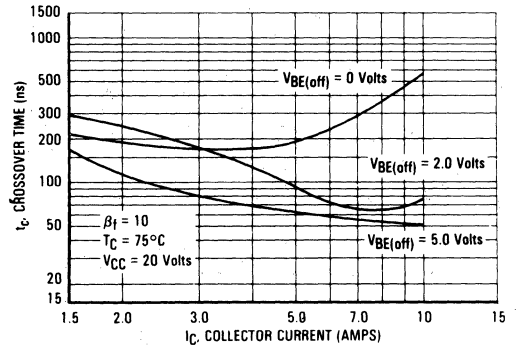


FIGURE 12 — CROSSOVER TIME



3

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

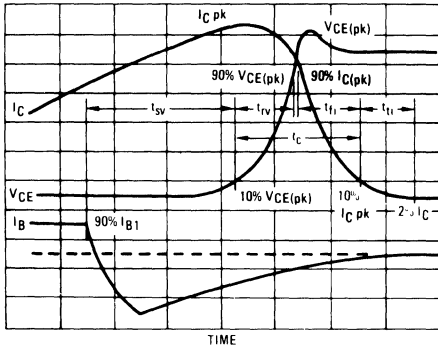
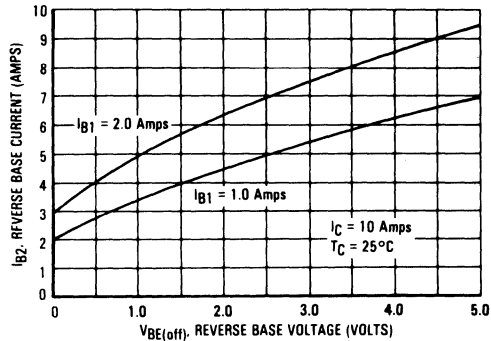


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

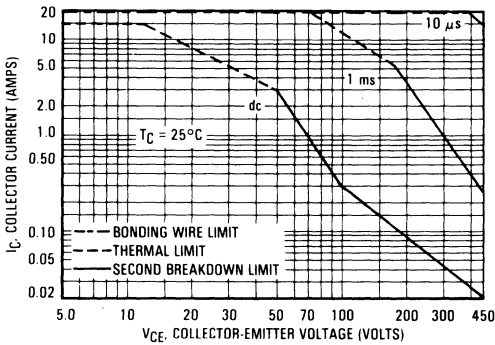
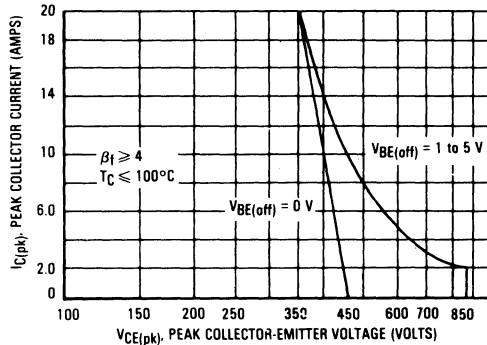


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25^\circ C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce

the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

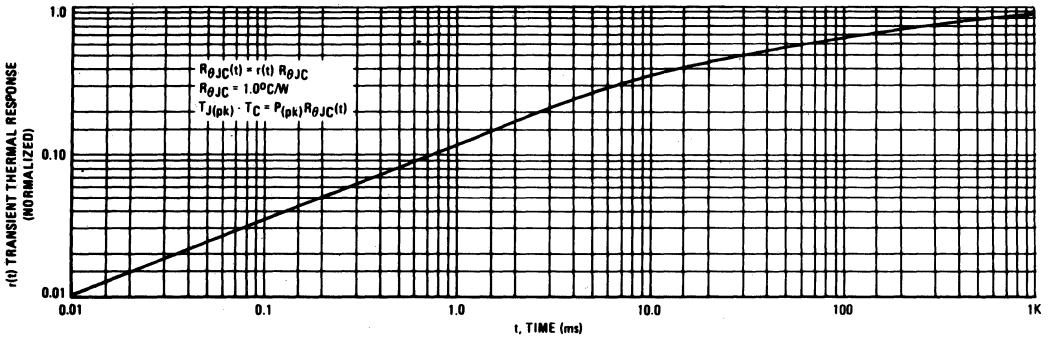


FIGURE 18 — POWER DERATING

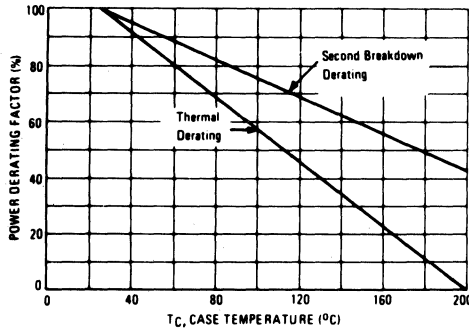
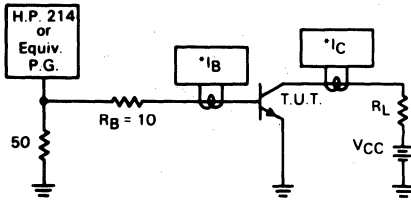
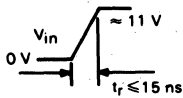


TABLE 1 — RESISTIVE LOAD SWITCHING

t_d and t_r

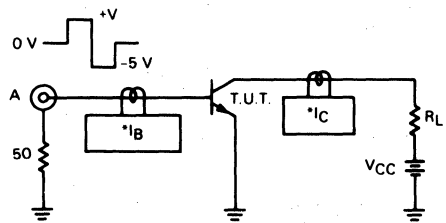
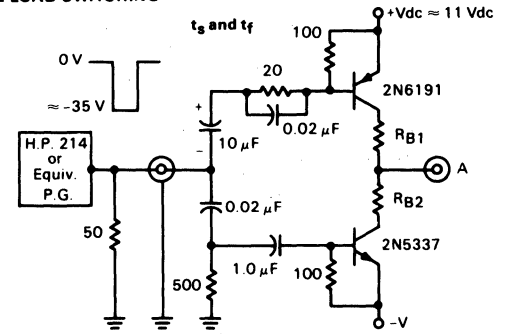


$V_{CC} = 250$ Vdc
 $R_L = 25$ Ω
 $I_C = 10$ Adc
 $I_B = 1.0$ Adc



*Tektronix
 P-6042 or
 Equivalent

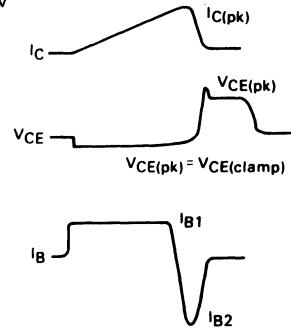
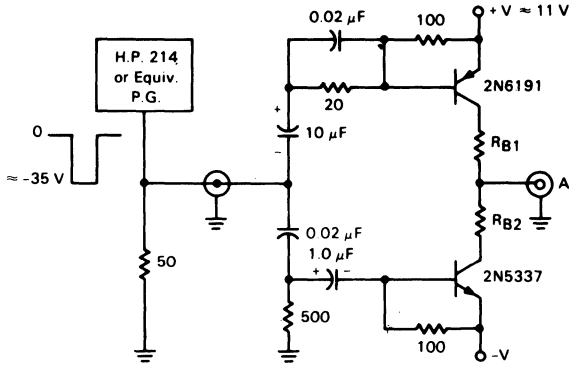
t_s and t_f



$V_{CC} = 250$ Vdc
 $R_L = 25$ Ω
 $I_C = 10$ Adc
 $I_{B1} = 1.0$ Adc
 $I_{B2} = 2.0$ Adc
 $R_{B1} = 10$ Ω
 $R_{B2} = 1.6$ Ω
 For $V_{BE}(\text{off}) = 5.0$ V $R_{B2} = 0$ Ω

*Note: Adjust -V to obtain desired $V_{RE}(\text{off})$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



$$T_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

V(BR)CEO
 $L = 10 \text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20 \text{ Volts}$

Inductive Switching
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

RBSOA
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

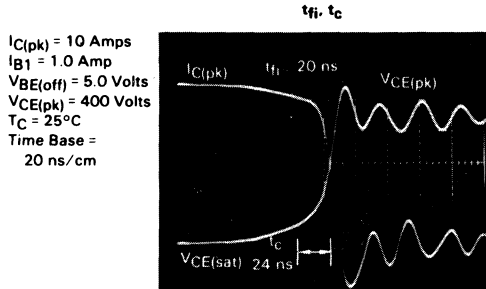
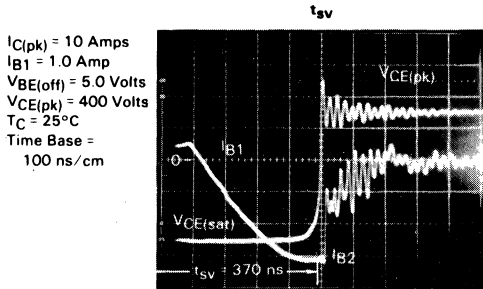
*Tektronix
P-6042 or
Equivalent

Scope - Tektronix
7403 or
Equivalent

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.



TYPICAL INDUCTIVE SWITCHING WAVEFORMS



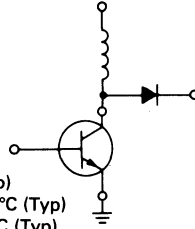
Designer's Data Sheet

SWITCHMODE III SERIES
ULTRA-FAST NPN SILICON POWER TRANSISTORS

This transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 30 ns Inductive Fall Time — 75°C (Typ)
 - 40 ns Inductive Crossover Time — 75°C (Typ)
 - 800 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range — 65 to +200°C
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents



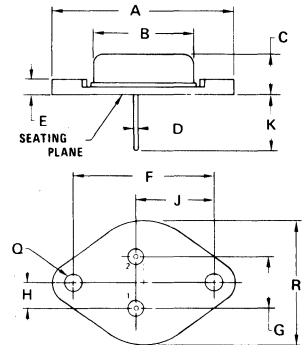
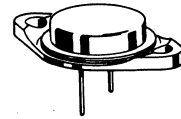
20 AMPERE

NPN SILICON
POWER TRANSISTORS

450 VOLTS
250 WATTS

Designer's Data for
"Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
 TO-204AE (Type) Modified TO-3

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage*	$V_{CE0(sus)}$	450	Vdc
Collector-Emitter Voltage*	V_{CEV}	850	Vdc
Emitter Base Voltage*	V_{EB}	6.0	Vdc
Collector Current — Continuous*	I_C	20	Adc
— Peak (1)	I_{CM}	30	
Base Current — Continuous*	I_B	15	Adc
— Peak (1)	I_{BM}	20	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ *	P_D	250	Watts
Derate above 25°C @ $T_C = 100^\circ\text{C}$		143	
		1.43	W/°C
Operating and Storage Junction* Temperature Range	T_J, T_{stg}	-65 to +200	°C

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering* Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
 *Indicate JEDEC Registered Data

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	— —	— —	0.25* 1.5*	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0*	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.2\text{ Adc}$) ($I_C = 15\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 15\text{ Adc}$, $I_B = 2.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.5 3.0* 3.0*	Vdc
Base-Emitter Saturation Voltage ($I_C = 15\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 15\text{ Adc}$, $I_B = 2.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5* 1.5	Vdc
DC Current Gain ($I_C = 15\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$) ($I_C = 20\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.5* 5.0	— —	30* —	—

DYNAMIC CHARACTERISTICS (2)

Current Gain — Bandwidth Product ($V_{CE} = 10\text{ Vdc}$, $I_C = 0.25\text{ Adc}$, $f_{test} = 10\text{ MHz}$)	f_T	10*	—	75*	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	100*	—	500*	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)								
Delay Time	$(I_C = 15\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 2.0\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	$(I_{B2} = 4.0\text{ Adc}$, $R_{B2} = 1.6\ \Omega)$	t_d	—	20	100*	ns	
Rise Time			t_r	—	200	500*		
Storage Time			t_s	—	1200	2700*		
Fall Time			t_f	—	200	350*		
Storage Time			$(V_{BE(off)} = 5.0\text{ Vdc})$	t_s	—	650		—
Fall Time				t_f	—	80		—
Inductive Load (Table 2)								
Storage Time	$(I_C = 15\text{ Adc}$, $I_{B1} = 2.0\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	$(T_C = 100^\circ\text{C})$	t_{sv}	—	800	2700*	ns	
Fall Time			t_{fi}	—	50	200*		
Crossover Time			t_c	—	90	250*		
Storage Time			$(T_C = 150^\circ\text{C})$	t_{sv}	—	1050		—
Fall Time				t_{fi}	—	70		—
Crossover Time				t_c	—	120		—

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.(2) $f_T = |h_{FE}| f_{test}$

*Indicates JEDEC Registered Limit

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

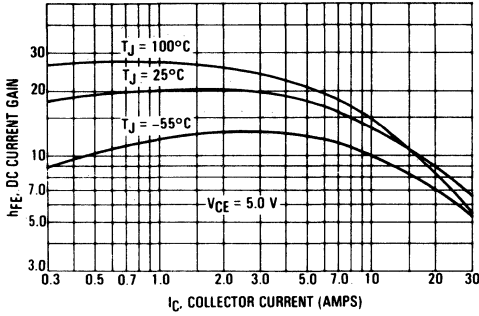


FIGURE 2 — COLLECTOR SATURATION REGION

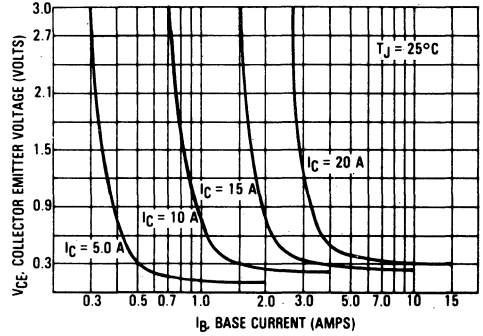


FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION

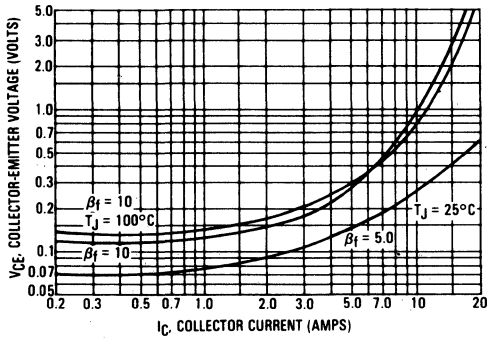


FIGURE 4 — BASE-EMITTER VOLTAGE

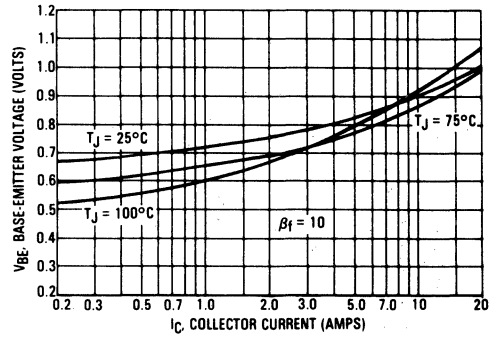


FIGURE 5 — COLLECTOR CUTOFF REGION

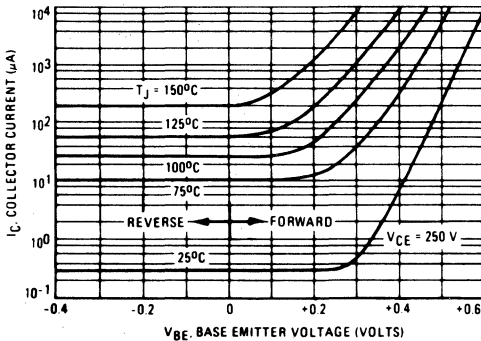
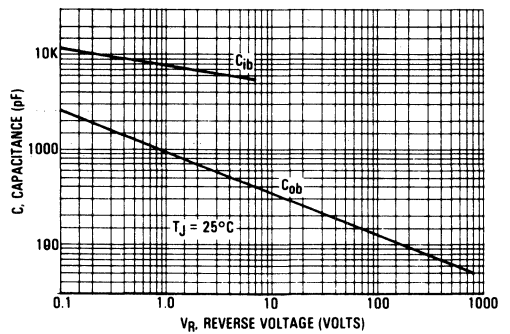


FIGURE 6 — CAPACITANCE



3

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

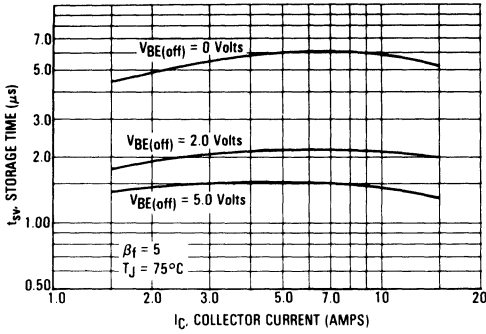


FIGURE 8 — STORAGE TIME

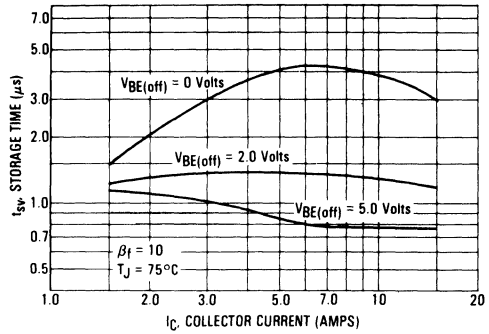


FIGURE 9 — COLLECTOR CURRENT FALL TIME

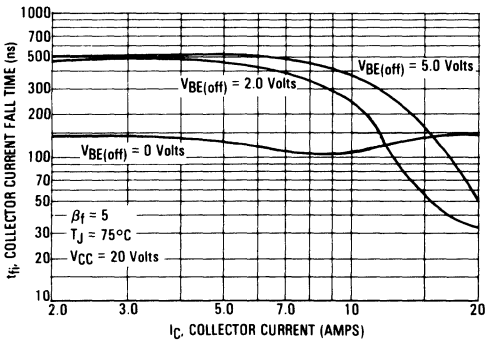


FIGURE 10 — COLLECTOR CURRENT FALL TIME

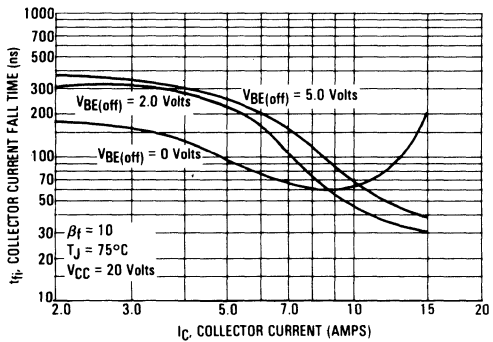


FIGURE 11 — CROSSOVER TIME

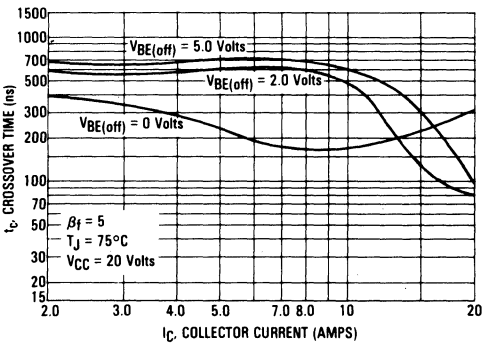


FIGURE 12 — CROSSOVER TIME

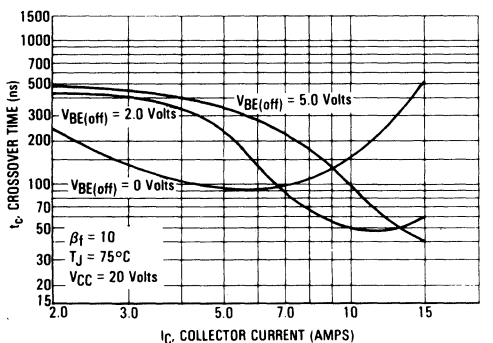


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

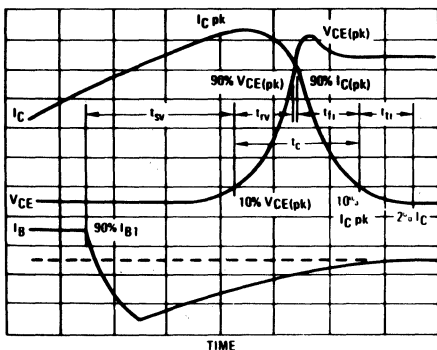
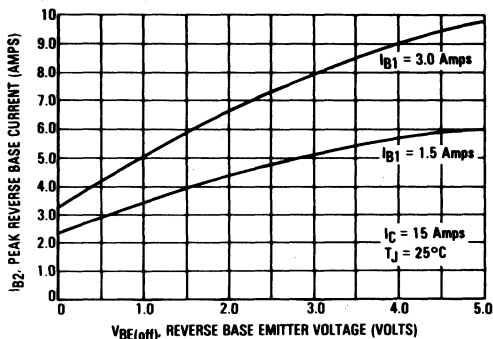


FIGURE 14 — REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

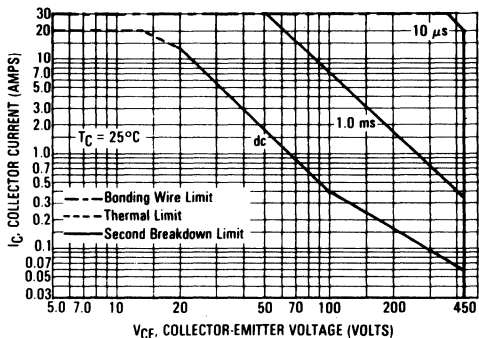
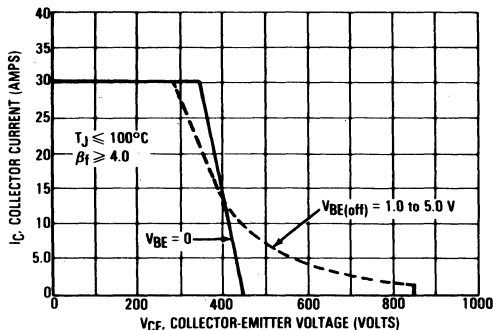


FIGURE 16 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_c - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25^\circ C$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_J(pk)$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will re-

duce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

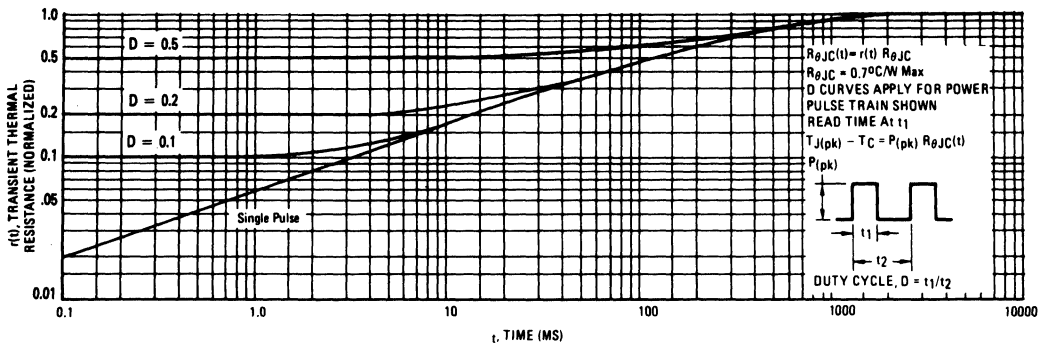


FIGURE 18 — POWER DERATING

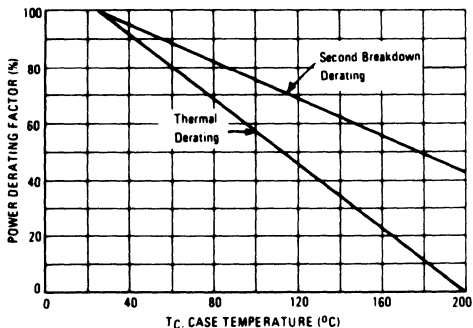
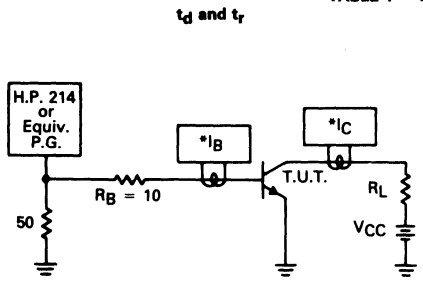
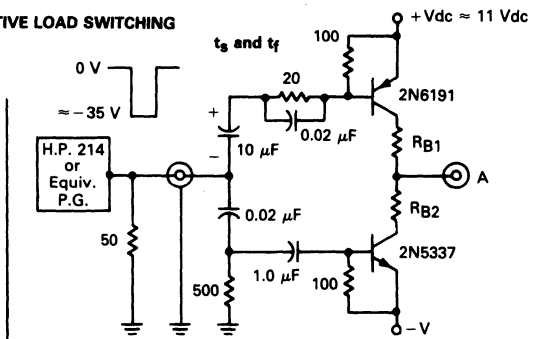


TABLE 1 — RESISTIVE LOAD SWITCHING



$V_{CC} = 250 \text{ Vdc}$
 $R_L = 16 \Omega$
 $I_C = 15 \text{ Adc}$
 $I_B = 2.0 \text{ Adc}$

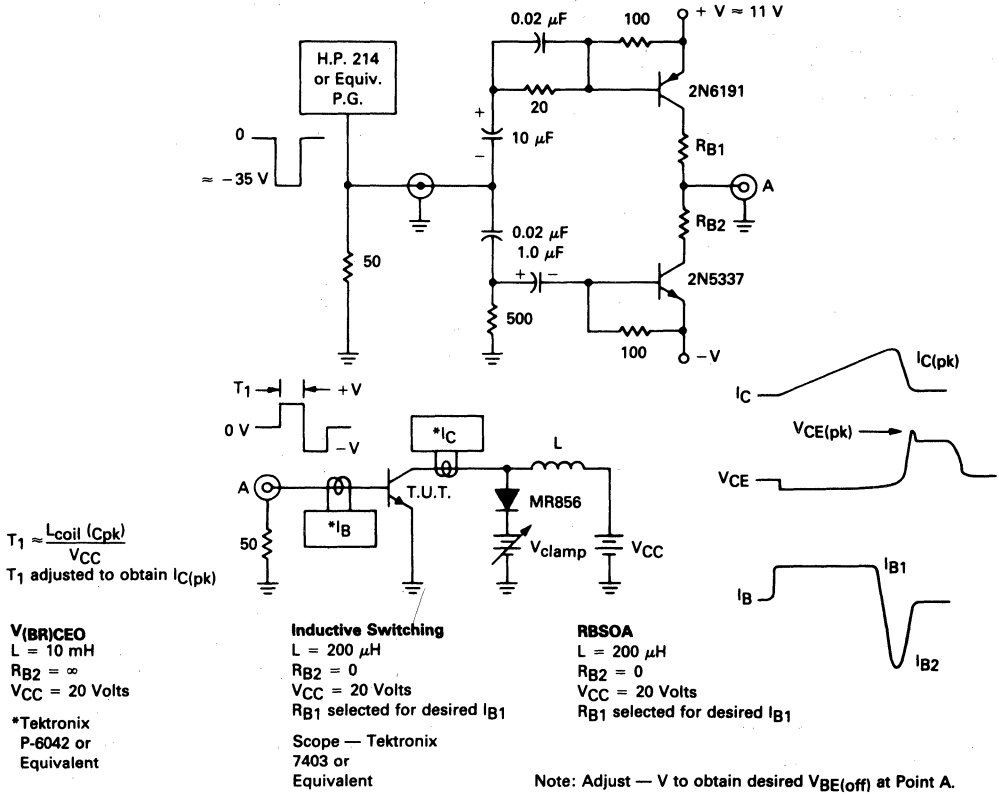
*Tektronix P-6042 or Equivalent



$V_{CC} = 250$ $I_{B1} = 2.0 \text{ Adc}$ $R_{B1} = 7.5 \Omega$
 $R_L = 16 \Omega$ $I_{B2} = 4.0 \text{ Adc}$ $R_{B2} = 1.6 \Omega$
 $I_C = 15 \text{ Adc}$ For $V_{BE(off)} = 5.0 \text{ V}$ $R_{B2} = 0 \Omega$

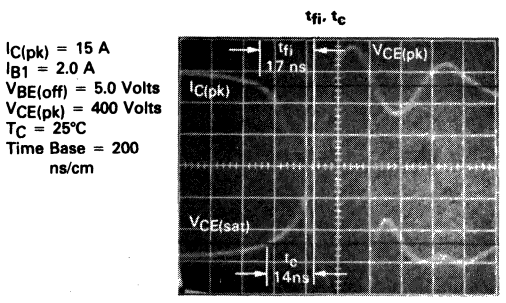
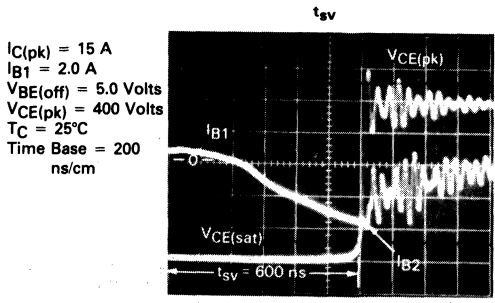
*Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



3

TYPICAL INDUCTIVE SWITCHING WAVEFORMS



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD135,-6,-10,-16
BD137,-6,-10,-16
BD139,-6,-10,-16

PLASTIC MEDIUM POWER
 SILICON NPN TRANSISTOR

... designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- Available in h_{FE} groups -6, -10, -16
- DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 0.15$ Adc
- BD 135, 137, 139 are complementary with BD 136, 138, 140

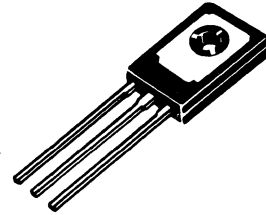
1.5 AMPERE
POWER TRANSISTOR

NPN SILICON

45, 60, 80 VOLTS
10 WATTS

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 135	45	Vdc
		BD 137	60	
		BD 139	80	
Collector-Base Voltage	V_{CBO}	BD 135	45	Vdc
		BD 137	60	
		BD 139	100	
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	A dc
Base Current	I_B		0.5	A dc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$	P_D		1.25	Watts
		Derate above 25°C	10	mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D		12.5	Watt
		Derate above 25°C	100	mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150	$^\circ\text{C}$



THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	100	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.03$ Adc, $I_B = 0$)	V_{CEO}^*	BD 135 BD 137 BD 139	45 60 80	—	Vdc
Collector Cutoff Current ($V_{CB} = 30$ Vdc, $I_E = 0$) ($V_{CB} = 30$ Vdc, $I_E = 0$, $T_C = 125^\circ\text{C}$)	I_{CBO}		—	0.1 10	$\mu\text{A dc}$
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	10	$\mu\text{A dc}$
DC Current Gain ($I_C = 0.005$ A, $V_{CE} = 2$ V) ($I_C = 0.15$ A, $V_{CE} = 2$ V)	h_{FE}^*		25 40	— 250	—
($I_C = 0.5$ A, $V_{CE} = 2$ V)			25	—	
Collector-Emitter Saturation Voltage* ($I_C = 0.5$ Adc, $I_B = 0.05$ Adc)	$V_{CE(sat)}^*$		—	0.5	Vdc
Base-Emitter On Voltage* ($I_C = 0.5$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}^*$		—	1	Vdc

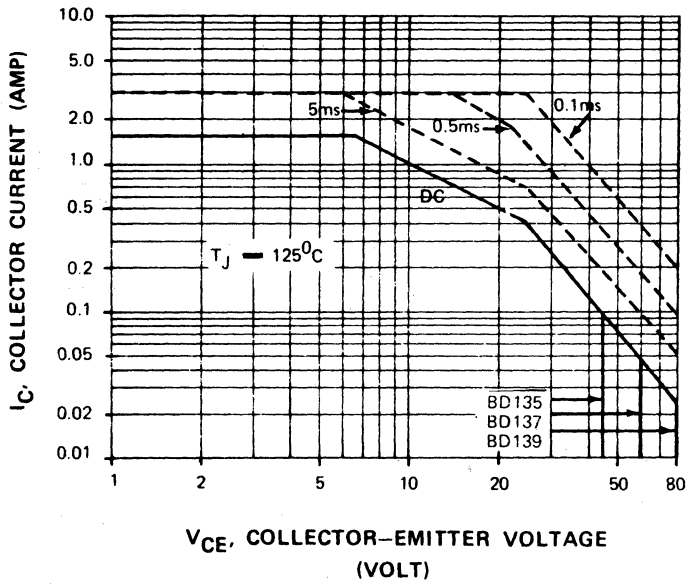
* Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.04	0.45	0.45
B	2.68	2.74	0.26	0.26
C	2.42	2.66	0.09	0.10
D	0.51	0.68	0.020	0.025
E	2.93	3.17	0.11	0.12
F	2.32	2.46	0.091	0.097
G	1.77	2.41	0.050	0.095
H	0.98	0.63	0.039	0.025
I	14.61	16.63	0.575	0.650
J	—	2.70	—	0.10
K	3.76	4.01	0.148	0.158
L	1.15	1.30	0.045	0.050
M	0.64	0.68	0.025	0.027
N	3.68	3.97	0.145	0.155
V	1.02	—	0.040	—

STYLE 1
 1. MET. MAIN TERMINAL
 2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010)
 DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



3

Available in HFE groups	Min.	Max.
(At $I_C = 0.15$ A, $V_{CE} = 2$ V) HFE group:		
-6	40	100
-10	63	160
-16	100	250

MOTOROLA
SEMICONDUCTOR
 TECHNICAL DATA

BD136,-6,-10,-16
BD138,-6,-10,-16
BD140,-6,-10,-16

PLASTIC MEDIUM POWER
 SILICON PNP TRANSISTOR

- ... designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.
- Available in h_{FE} groups -6, -10, -16
 - DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 0.15$ Adc
 - BD 136, 138, 140 are complementary with BD 135, 137, 139

1.5 AMPERE
POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
 10 WATTS

MAXIMUM RATINGS

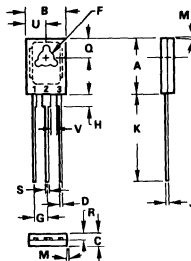
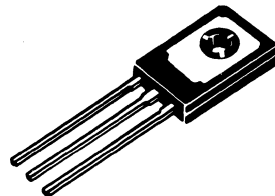
Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 136	45	Vdc
		BD 138	60	
		BD 140	80	
Collector-Base Voltage	V_{CBO}	BD 136	45	Vdc
		BD 138	60	
		BD 140	100	
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D		1.25	Watts
			10	mW/°C
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D		12.5	Watt
			100	mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.03$ Adc, $I_B = 0$)	BV_{CEO} *	BD 136 BD 138 BD 140	45 60 80	—	Vdc
Collector Cutoff Current ($V_{CB} = 30$ Vdc, $I_E = 0$) ($V_{CB} = 30$ Vdc, $I_E = 0$, $T_C = 125^\circ\text{C}$)	I_{CBO}		—	0.1 10	μAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	10	μAdc
DC Current Gain ($I_C = 0.005$ A, $V_{CE} = 2$ V) ($I_C = 0.15$ A, $V_{CE} = 2$ V)	h_{FE} *		25 40	— 250	—
($I_C = 0.5$ A, $V_{CE} = 2$ V)			25	—	
Collector-Emitter Saturation Voltage* ($I_C = 0.5$ Adc, $I_B = 0.05$ Adc)	$V_{CE(sat)}$ *		—	0.5	Vdc
Base-Emitter On Voltage* ($I_C = 0.5$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$ *		—	1	Vdc



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.00	11.54	0.400	0.455
B	3.50	7.24	0.295	0.300
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.92	2.96	0.081	0.097
H	1.27	2.41	0.060	0.095
J	0.29	0.63	0.015	0.025
K	14.61	16.63	0.575	0.660
M	P TYP			
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.68	0.025	0.026
U	2.68	3.93	0.105	0.155
V	1.02	—	0.040	—

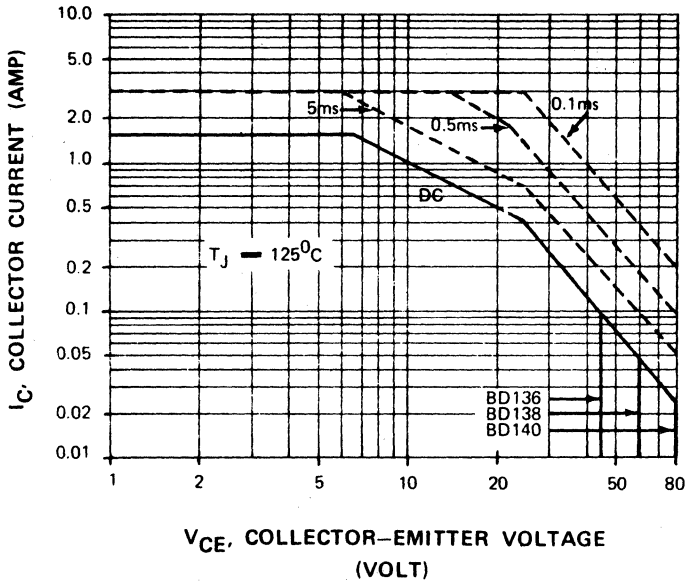
STYLE 1:
 PM1 - EMITTER
 2 - COLLECTOR
 3 - BASE

NOTES:
 1. MT - MAIN TERMINAL
 2. LEADS TRULY POSITIONED WITHIN 0.25mm (0.010")
 DIA TO DIM A & B AT MAXIMUM MATERIAL
 CONDITION

CASE 77-05
TO-126

* Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



Available in HFE groups (at $I_C = 0.15\text{ A}$, $V_{CE} = 2\text{ V}$) HFE group:	Min.	Max.
-6	40	100
-10	63	160
-16	100	250

BD157
BD158
BD159

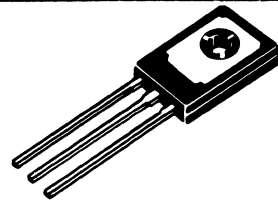
**PLASTIC MEDIUM POWER NPN
 SILICON TRANSISTOR**

... designed for power output stages for television, radio, phonograph and other consumer product applications.

- Suitable for Transformerless, Line-Operated Equipment
- Thermopad† Construction Provides High Power Dissipation Rating for High Reliability

**0.5 AMPERE
 POWER TRANSISTOR
 NPN SILICON**

250-300-350 VOLTS
 20 WATTS



***MAXIMUM RATINGS**

Rating	Symbol	BD 157	BD 158	BD 159	Unit
Collector-Emitter Voltage	V _{CEO}	250	300	350	Vdc
Collector-Base Voltage	V _{CB}	275	325	375	Vdc
Emitter-Base Voltage	V _{EB}	← 5.0 →			Vdc
Collector Current – Continuous Peak	I _C	← 0.5 → ← 1.0 →			Adc
Base Current	I _B	← 0.25 →			Adc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	← 20 → ← 0.16 →			Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	← -65 to +150 →			°C

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ _{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

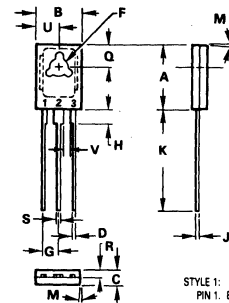
Characteristic	Symbol	Type	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (I _C = 1.0 mAdc, I _B = 0)	BV _{CEO}	BD 157 BD 158 BD 159	250 300 350	—	Vdc
Collector Cutoff Current (At rated voltage)	I _{CBO}		—	100	μAdc
Emitter Cutoff Current (V _{EB} = 5.0 Vdc, I _C = 0)	I _{EBO}		—	100	μAdc

ON CHARACTERISTICS

DC Current Gain (I _C = 50 mAdc, V _{CE} = 10 Vdc)	h _{FE}		30	240	—
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- NOTES:
 1. MT = MAIN TERMINAL
 2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS			INCHES		
	MIN	MAX	TYP	MIN	MAX	TYP
A	10.80	11.04	0.425	0.435		
B	7.50	7.74	0.295	0.305		
C	2.42	2.66	0.095	0.105		
D	0.51	0.65	0.020	0.025		
F	2.83	3.17	0.115	0.125		
G	2.32	2.46	0.091	0.097		
H	1.27	2.41	0.050	0.095		
J	0.39	0.63	0.015	0.025		
K	14.61	16.53	0.575	0.655		
M	± TYP			± TYP		
Q	3.76	4.01	0.148	0.158		
R	1.15	1.39	0.045	0.055		
S	0.64	0.88	0.025	0.035		
U	3.69	3.93	0.145	0.155		
V	1.02	—	0.040	—		

**CASE 77-05
 TO-126**

FIGURE 1 – POWER TEMPERATURE DERATING CURVE

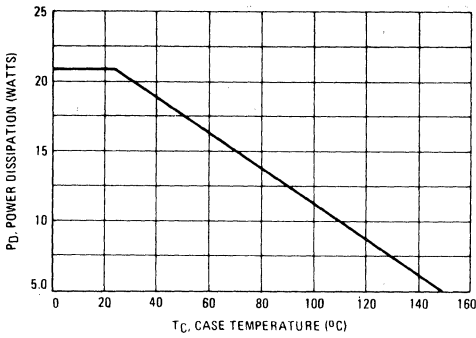


FIGURE 2 – "ON" VOLTAGES

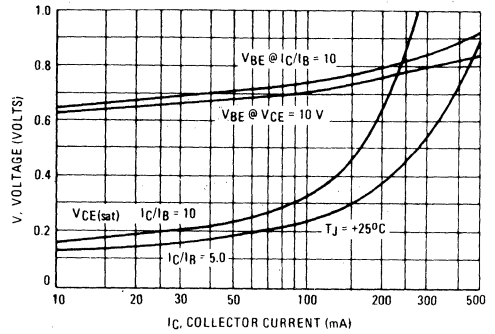
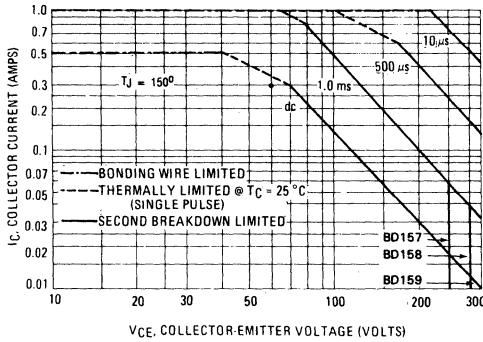
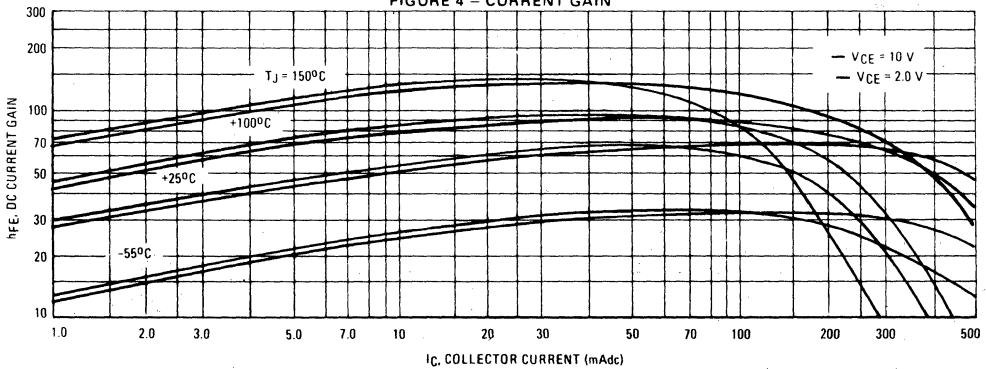


FIGURE 3 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C - V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 4 – CURRENT GAIN



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD165
BD167
BD169

**PLASTIC MEDIUM POWER
SILICON NPN TRANSISTOR**

... designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 0.15$ Adc
- BD 165, 167, 169 are complementary with BD 166, 168, 170

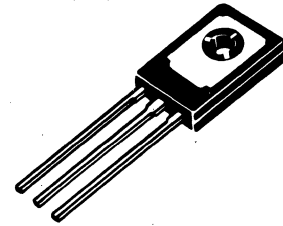
**1.5 AMPERE
POWER TRANSISTOR**

NPN SILICON

**45, 60, 80 VOLTS
20 WATTS**

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 165	45	Vdc
		BD 167	60	
		BD 169	80	
Collector-Base Voltage	V_{CBO}	BD 165	45	Vdc
		BD 167	60	
		BD 169	80	
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$	P_D		1.25	Watts
		Derate above 25°C	8	
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D		20	Watt
		Derate above 25°C	160	
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +150	$^\circ\text{C}$



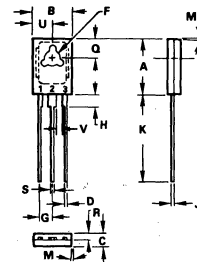
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	100	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$)	BV_{CEO}	BD 165	45	—	Vdc
		BD 167	60	—	
		BD 169	80	—	
Collector Cutoff Current ($V_{CB} = 45$ Vdc, $I_E = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	I_{CBO}	BD 165	—	0.1	mA
		BD 167	—	0.1	
		BD 169	—	0.1	
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mA
DC current Gain ($I_C = 0.15$ A, $V_{CE} = 2$ V) ($I_C = 0.5$ A, $V_{CE} = 2$ V)	h_{FE}		40	—	
			15	—	
Collector-Emitter Saturation Voltage* ($I_C = 0.5$ Adc, $I_B = 0.05$ Adc)	$V_{CE(sat)}$		—	0.5	Vdc
Base-Emitter On Voltage* ($I_C = 0.5$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$		—	0.95	Vdc
Current-Gain-Bandwidth Product ($I_C = 500$ mA, $V_{CE} = 2$ Vdc, $f = 1.0$ MHz)	f_T		6.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.90	11.94	0.429	0.469
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.59	2.83	0.102	0.112
H	1.27	1.51	0.050	0.059
J	0.38	0.63	0.015	0.025
K	14.67	16.03	0.577	0.629
M	2-TYP			
O	3.75	4.01	0.148	0.158
R	1.15	1.38	0.045	0.054
S	0.64	0.88	0.025	0.035
U	3.89	3.93	0.153	0.155
V	1.92	—	0.075	—

STYLE 1:
PN 1: EMITTER
2: COLLECTOR
3: BASE

NOTES:
1. MT - MAIN TERMINAL
2. LEADS: TRUE POSITIONED WITHIN 0.25mm (0.010") DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

**CASE 77-05
TO-126**

FIGURE 1 - P_n - T_c DERATING CURVE

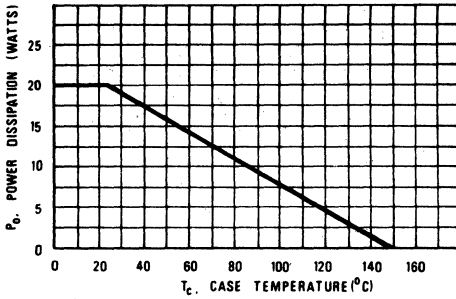
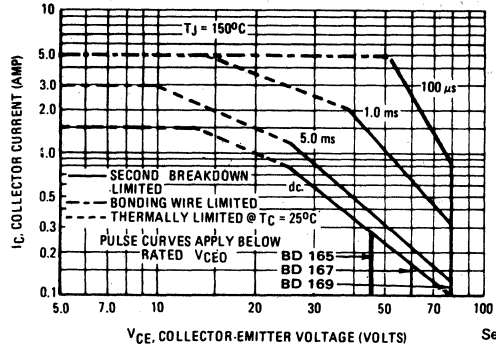


FIGURE 2 - SAFE OPERATING AREA



See Note 1

FIGURE 3 - COLLECTOR SATURATION REGION

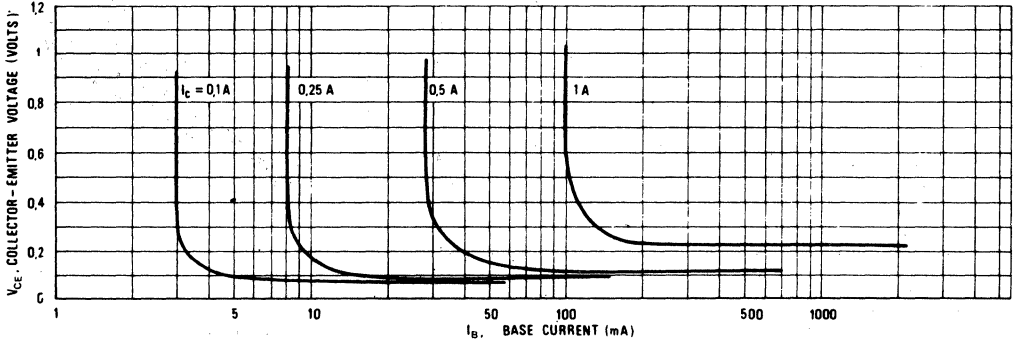


FIGURE 4 - CURRENT GAIN

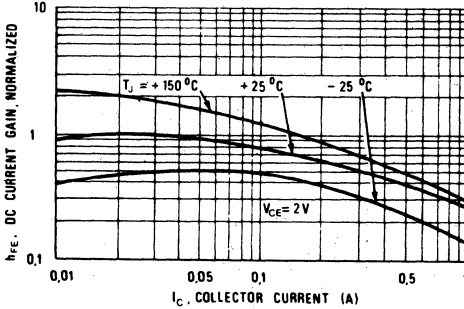
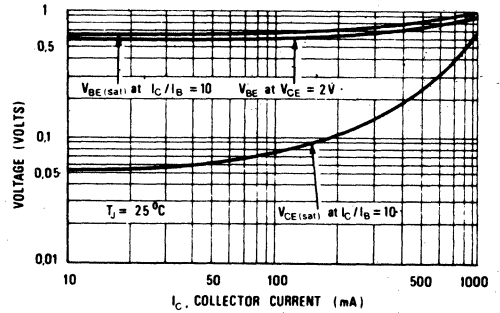


FIGURE 5 - "ON" VOLTAGE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

BD166 BD168 BD170

PLASTIC MEDIUM POWER SILICON PNP TRANSISTOR

... designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 0.15$ Adc
- BD 166, 168, 170 are complementary with BD 165, 167, 169

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 166	45	Vdc
		BD 168	60	
		BD 170	80	
Collector-Base Voltage	V_{CBO}	BD 166	45	Vdc
		BD 168	60	
		BD 170	80	
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	A dc
Base Current	I_B		0.5	A dc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D		1.25	Watts
			10	mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D		20	Watt
			160	mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	100	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

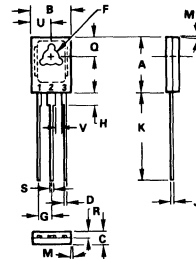
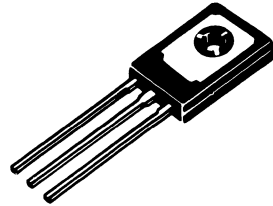
Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$)	BV_{CEO}	BD 166 BD 168 BD 170	45 60 80	—	Vdc
Collector Cutoff Current ($V_{CB} = 45$ Vdc, $I_E = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	I_{CBO}	BD 166 BD 168 BD 170	— — —	0.1 0.1 0.1	mA dc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mA dc
DC current Gain ($I_C = 0.15$ A, $V_{CE} = 2$ V) ($I_C = 0.5$ A, $V_{CE} = 2$ V)	h_{FE}		40 15	—	—
Collector-Emitter Saturation Voltage* ($I_C = 0.5$ Adc, $I_B = 0.05$ Adc)	$V_{CE(sat)}$		—	0.5	Vdc
Base-Emitter On Voltage* ($I_C = 0.5$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$		—	0.95	Vdc
Current-Gain-Bandwidth Product ($I_C = 500$ mA dc, $V_{CE} = 2$ Vdc, $f = 1.0$ MHz)	f_T		6.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$.

1.5 AMPERE POWER TRANSISTOR

PNP SILICON

45, 60, 80 VOLTS
20 WATTS



DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.28	0.83	0.011	0.033
K	14.61	16.63	0.575	0.655
M	2.79		0.110	
Q	3.75	4.01	0.148	0.158
R	1.15	1.29	0.045	0.051
S	0.64	0.68	0.025	0.027
U	3.69	3.92	0.145	0.155
V	1.02	—	0.040	—

STYLE 1
1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. M₁ - MAIN TERMINAL
2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010")
DIA TO DIM A & B AT MAXIMUM MATERIAL
CONDITION

CASE 77-05
TO-126

3

FIGURE 1 - P_D - T_C DERATING CURVE

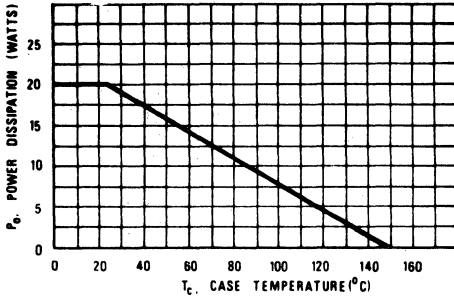


FIGURE 2 - SAFE OPERATING AREA

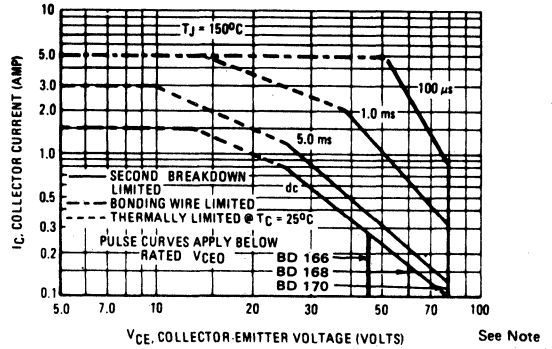


FIGURE 3 - COLLECTOR SATURATION REGION

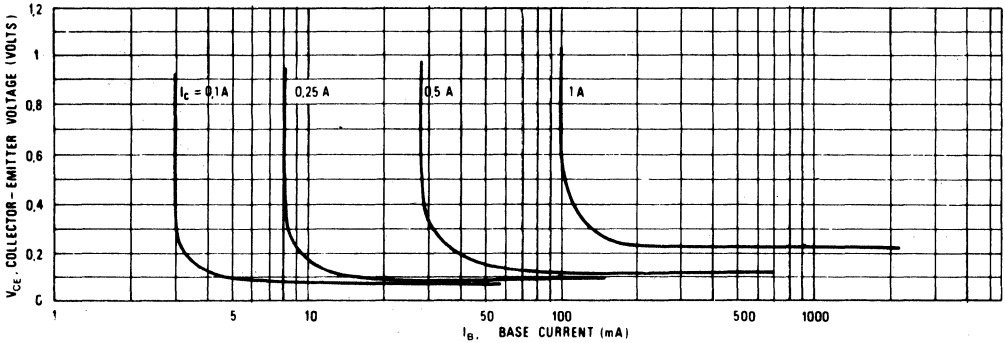


FIGURE 4 - CURRENT GAIN

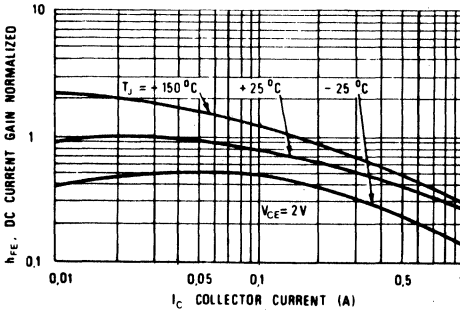
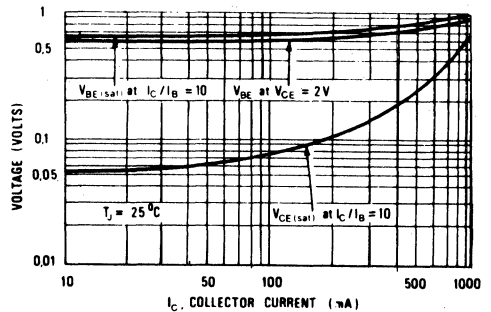


FIGURE 5 - "ON" VOLTAGE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD175,-6,-10,-16
BD177,-6,-10
BD179,-6,-10

**PLASTIC MEDIUM POWER
 SILICON NPN TRANSISTOR**

designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 0.15$ Adc
- BD 175, 177, 179 are complementary with BD 176, 178, 180
- Available in h_{FE} groups -6, -10, -16

**3 AMPERE
 POWER TRANSISTOR**

NPN SILICON

**45, 60, 80 VOLTS
 30 WATTS**

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 175 BD 177 BD 179	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 175 BD 177 BD 179	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		3.0	A dc
Base Current	I_B		1.0	A dc
Total Device Dissipation Derate above 25°C	P_D		30 240	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +150	°C

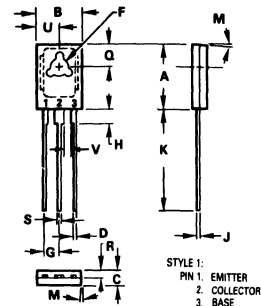
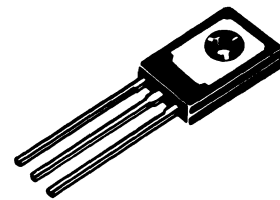
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$)	V_{CEO}	BD 175 BD 177 BD 179	45 60 80	—	Vdc
Collector Cutoff Current ($V_{CB} = 45$ Vdc, $I_E = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	I_{CBO}	BD 175 BD 177 BD 179	—	0.1 0.1 0.1	mA dc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mA dc
DC current Gain ($I_C = 0.15$ A, $V_{CE} = 2$ V) ($I_C = 1$ A, $V_{CE} = 2$ V)	h_{FE}	group -6 -10 -16	40 63 100	100 160 250	
Collector-Emitter Saturation Voltage* ($I_C = 1$ Adc, $I_B = 0.1$ Adc)	$V_{CE(sat)}$		—	0.8	Vdc
Base-Emitter On Voltage* ($I_C = 1$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$		—	1.3	Vdc
Current-Gain-Bandwidth Product ($I_C = 250$ mA dc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle $\leq 2.0\%$.

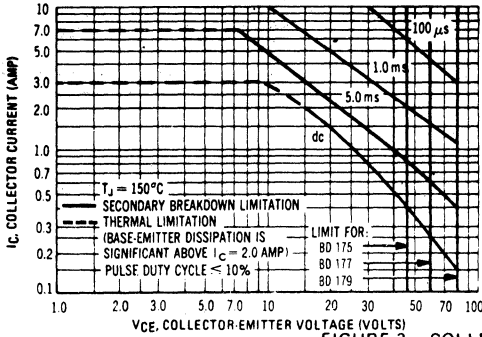


NOTES:
 1. MT = MAIN TERMINAL
 2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010)
 DIA. TO DIM A & B AT MAXIMUM MATERIAL
 CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.94	0.425	0.475
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.53	0.015	0.020
K	14.61	16.83	0.575	0.665
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.98	0.025	0.035
U	3.89	3.93	0.153	0.155
V	1.02	—	0.040	—

**CASE 77-05
 TO-126**

FIGURE 1 - ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C - V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 - COLLECTOR SATURATION REGION

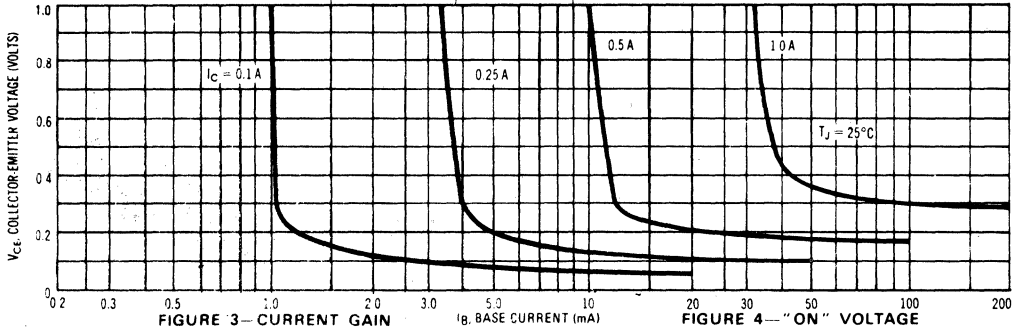


FIGURE 3 - CURRENT GAIN

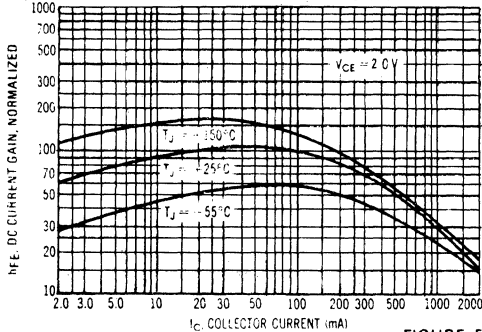


FIGURE 4 - "ON" VOLTAGE

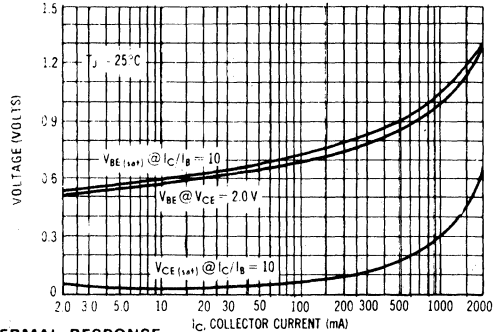
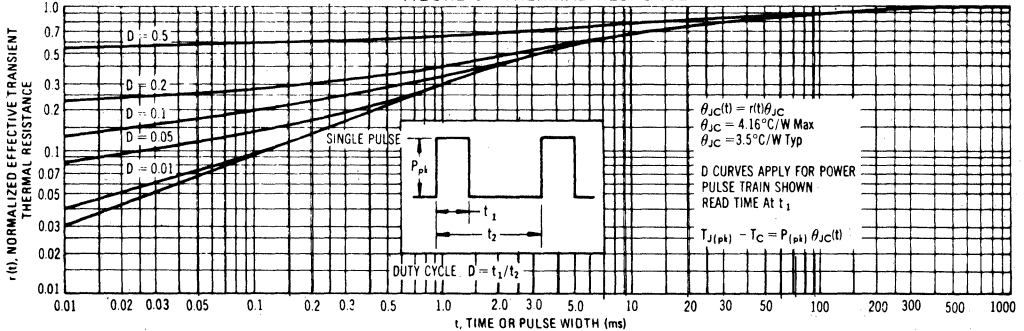


FIGURE 5 - THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD176,-6,-10,-16
BD178,-6,-10
BD180,-6,-10

**PLASTIC MEDIUM POWER
 SILICON PNP TRANSISTOR**

designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 0.15$ Adc
- BD 176, 178, 180 are complementary with BD 175, 177, 179
- Available in h_{FE} groups -6, -10, -16

**3 AMPERE
 POWER TRANSISTOR**

PNP SILICON

**45, 60, 80 VOLTS
 30 WATTS**

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 176	45	Vdc
		BD 178	60	
		BD 180	80	
Collector-Base Voltage	V_{CBO}	BD 176	45	Vdc
		BD 178	60	
		BD 180	80	
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		3.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation Derate above 25°C	P_D	$T_C = 25^\circ\text{C}$	30	Watts
			240	
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +150	°C

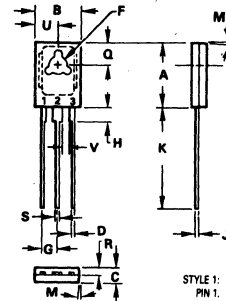
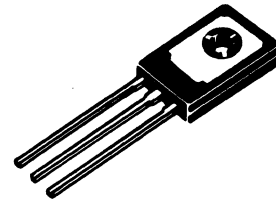
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$)	V_{CEO}^*	BD 176 BD 178 BD 180	45 60 80	—	Vdc
Collector Cutoff Current ($V_{CB} = 45$ Vdc, $I_E = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	I_{CBO}	BD 176 BD 178 BD 180	— — —	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mAdc
DC Current Gain ($I_C = 0.15$ A, $V_{CE} = 2$ V) ($I_C = 1$ A, $V_{CE} = 2$ V)	h_{FE}^*		40 63 100 15	100 160 250	
Collector-Emitter Saturation Voltage* ($I_C = 1$ Adc, $I_B = 0.1$ Adc)	$V_{CE(sat)}^*$		—	0.8	Vdc
Base-Emitter On Voltage* ($I_C = 1$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}^*$		—	1.3	Vdc
Current-Gain-Bandwidth Product ($I_C = 250$ mA, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle $\leq 2.0\%$.



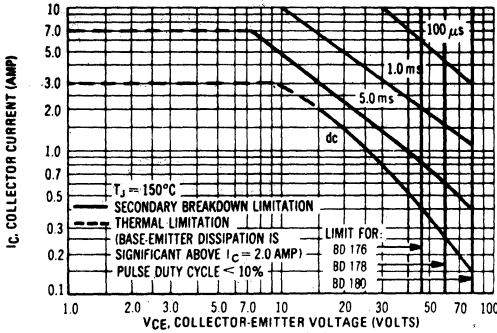
STYLE 1:
 PIN 1: EMITTER
 2: COLLECTOR
 3: BASE

NOTES:
 1. MT = MAIN TERMINAL.
 2. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.83	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	15.63	0.575	0.655
M	2 TYP		2 TYP	
Q	3.78	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

**CASE 77-05
 TO-126**

FIGURE 1 - ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C - V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 - COLLECTOR SATURATION REGION

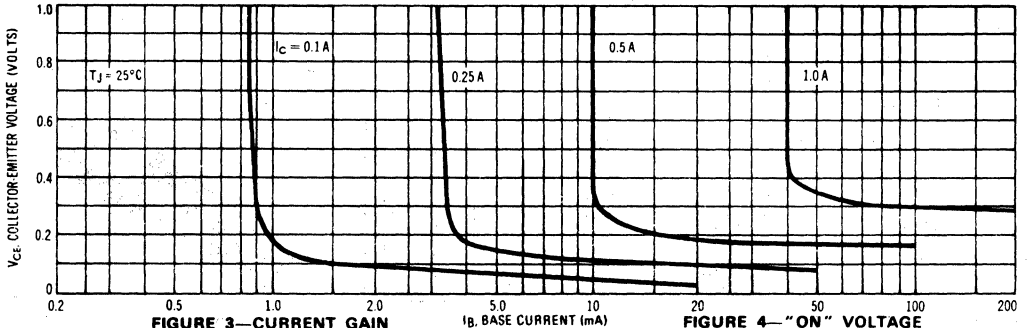


FIGURE 3 - CURRENT GAIN

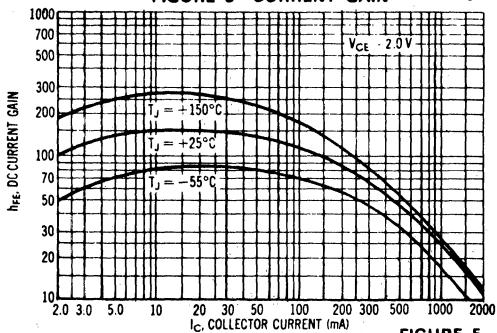


FIGURE 4 - "ON" VOLTAGE

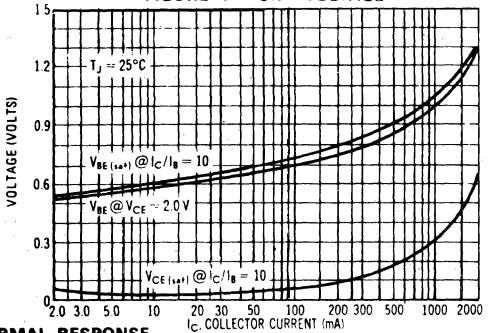
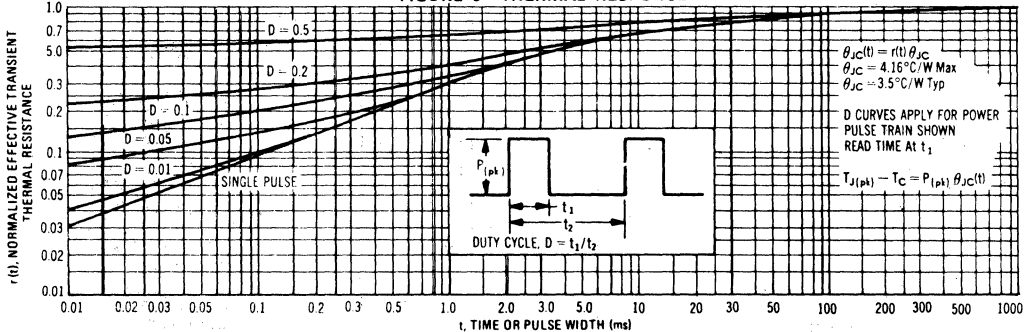


FIGURE 5 - THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD185
BD187
BD189

**PLASTIC MEDIUM POWER
 SILICON NPN TRANSISTOR**

... designed for use in 5 to 10 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 0.5$ Adc
- BD 185, 187, 189 are complementary with BD 186, 188, 190

**4 AMPERE
 POWER TRANSISTOR**

NPN SILICON

**30, 45, 60 VOLTS
 40 WATTS**

MARCH 1970—E-003

MAXIMUM RANGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 185 BD 187 BD 189	30 45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 185 BD 187 BD 189	40 55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		4.0	Adc
Base Current	I_B		2.0	Adc
Total Device Dissipation Derate above 25°C	P_D		40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +150	°C

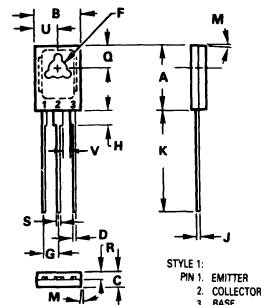
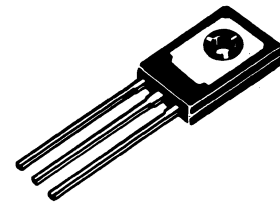
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$)	BV_{CEO}	BD 185 BD 187 BD 189	30 45 60	—	Vdc
Collector Cutoff Current ($V_{CB} = 40$ Vdc, $I_E = 0$) ($V_{CB} = 55$ Vdc, $I_E = 0$) ($V_{CB} = 70$ Vdc, $I_E = 0$)	I_{CBO}	BD 185 BD 187 BD 189	—	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mAdc
DC current Gain ($I_C = 0.5$ A, $V_{CE} = 2$ V) ($I_C = 2$ A, $V_{CE} = 2$ V)	h_{FE}		40 15	—	
Collector-Emitter Saturation Voltage* ($I_C = 2$ Adc, $I_B = 0.2$ Adc)	$V_{CE(sat)}$		—	1.0	Vdc
Base-Emitter On Voltage* ($I_C = 2$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$		—	1.5	Vdc
Current-Gain-Bandwidth Product ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		2.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle $\leq 2.0\%$.

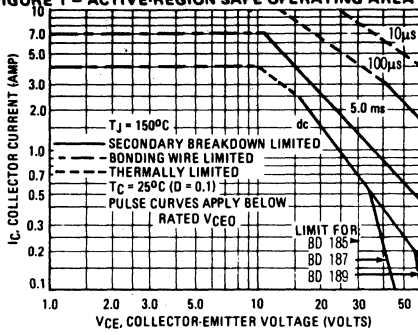


NOTES:
 1. MT - MAIN TERMINAL.
 2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.86	0.095	0.105
D	0.51	0.66	0.020	0.025
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.53	0.575	0.655
M	3" TYP		3" TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

**CASE 77-05
 TO-126**

FIGURE 1 - ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C - V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 - COLLECTOR SATURATION REGION

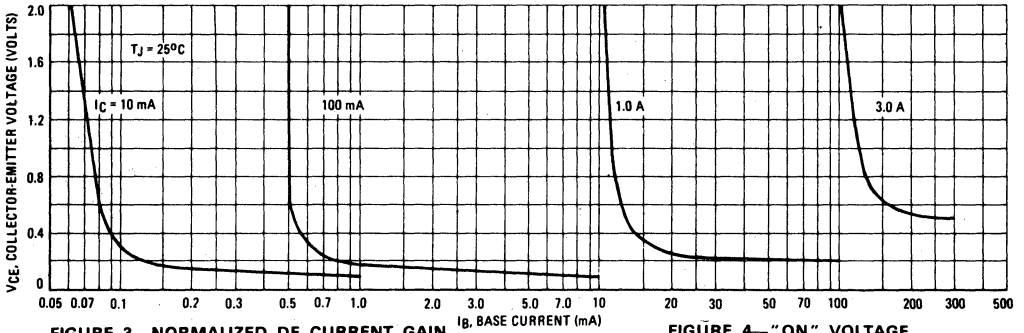


FIGURE 3 - NORMALIZED DC CURRENT GAIN

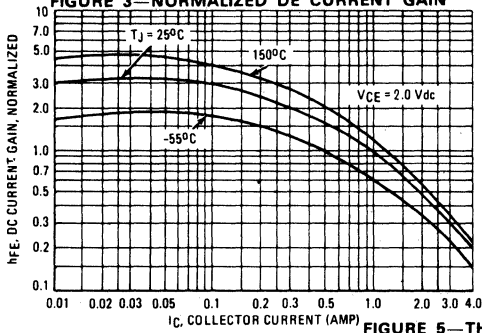


FIGURE 4 - "ON" VOLTAGE

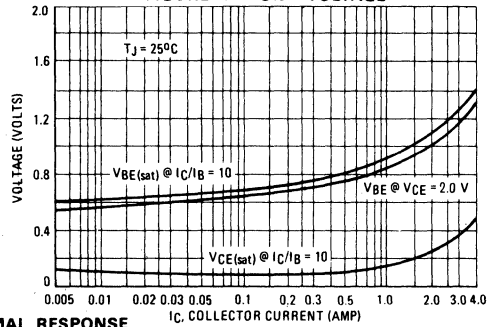
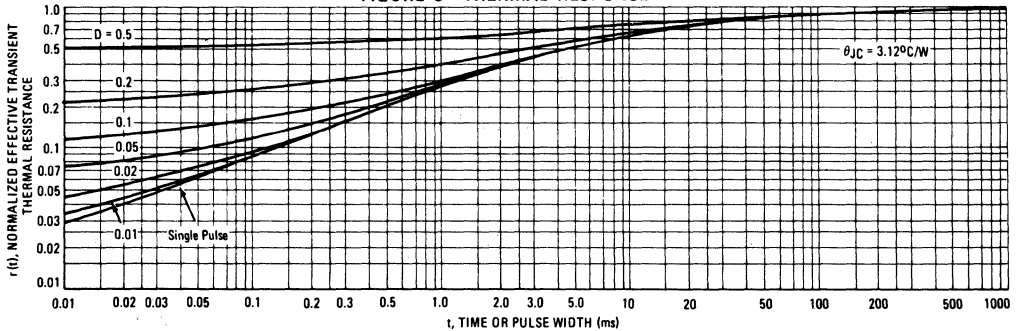


FIGURE 5 - THERMAL RESPONSE



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

BD186 BD188 BD190

PLASTIC MEDIUM POWER SILICON PNP TRANSISTOR

Designed for use in 5 to 10 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current— $h_{FE} = 40$ (Min) @ $I_C = 0.5$ Adc
- BD 186, 188, 190 are complementary with BD 185, 187, 189

MAXIMUM RANGES

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 186 BD 188 BD 190	30 45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 186 BD 188 BD 190	40 55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		4.0	Adc
Base Current	I_B		2.0	Adc
Total Device Dissipation Derate above 25°C	P_D		40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$)	BV_{CEO} *	BD 186 BD 188 BD 190	30 45 60	—	Vdc
Collector Cutoff Current ($V_{CB} = 40$ Vdc, $I_E = 0$) ($V_{CB} = 55$ Vdc, $I_E = 0$) ($V_{CB} = 70$ Vdc, $I_E = 0$)	I_{CBO}	BD 186 BD 188 BD 190	—	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mAdc
DC current Gain ($I_C = 0.5$ A, $V_{CE} = 2$ V) ($I_C = 2$ A, $V_{CE} = 2$ V)	h_{FE} *		40 15	—	
Collector-Emitter Saturation Voltage* ($I_C = 2.0$ Adc, $I_B = 0.2$ Adc)	$V_{CE(sat)}$ *		—	1.0	Vdc
Base-Emitter On Voltage* ($I_C = 2.0$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$ *		—	1.5	Vdc
Current-Gain-Bandwidth Product ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		2.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μ s. Duty Cycle $\leq 2.0\%$.

4 AMPERE POWER TRANSISTOR

PNP SILICON

30, 45, 60 VOLTS 40 WATTS

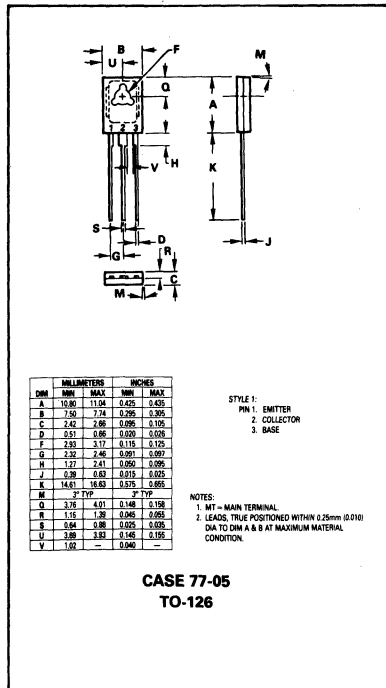
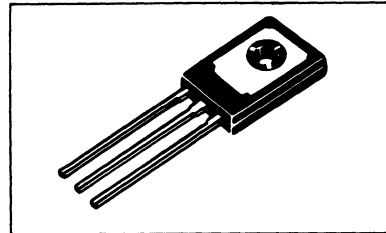
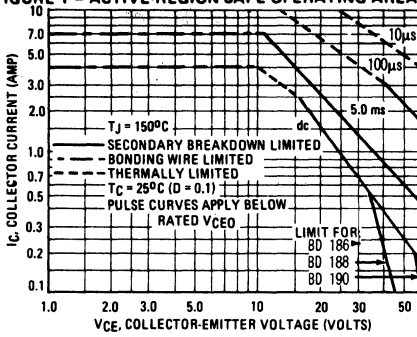


FIGURE 1 - ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C - V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 - COLLECTOR SATURATION REGION

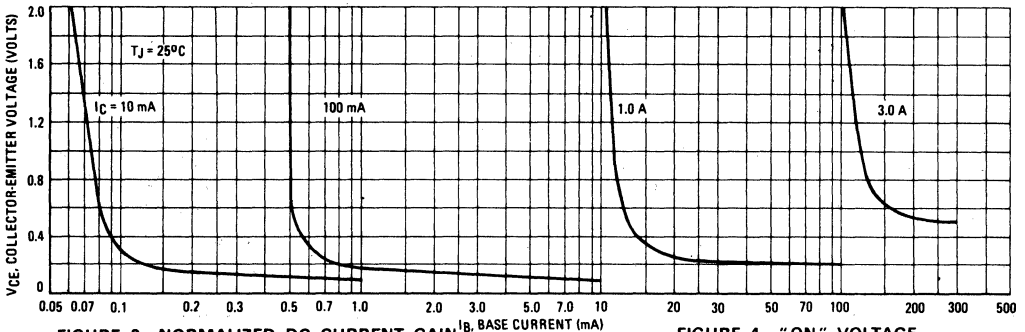


FIGURE 3 - NORMALIZED DC CURRENT GAIN

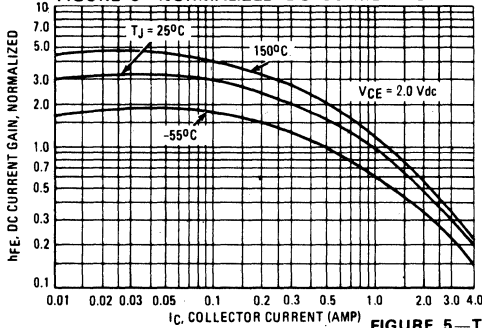


FIGURE 4 - "ON" VOLTAGE

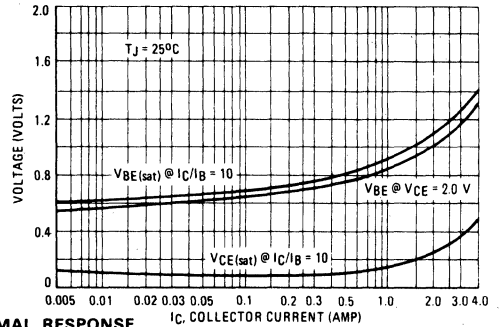
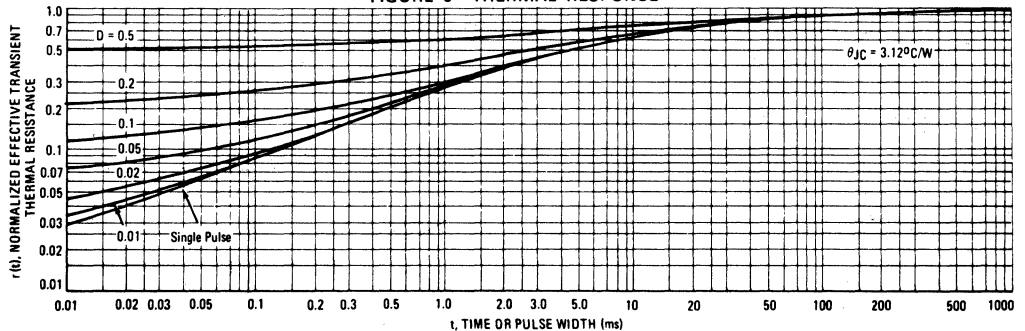


FIGURE 5 - THERMAL RESPONSE



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

BD205 BD207

PLASTIC HIGH POWER SILICON NPN TRANSISTOR

... designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain— $h_{FE} = 30$ (Min) @ $I_C = 2.0$ Adc
- BD 205, 207 are complementary with BD 206, 208

10 AMPERE POWER TRANSISTOR

NPN SILICON

45, 60 VOLTS
90 WATTS

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 205 BD 207	45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 205 BD 207	55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150	°C

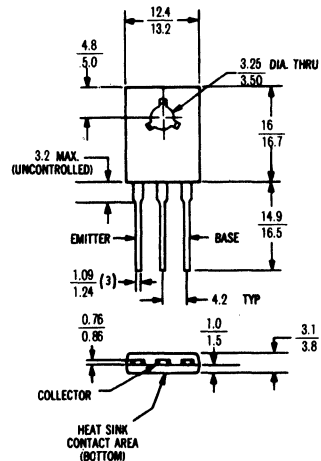
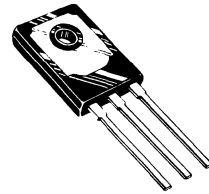
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.2$ Adc, $I_B = 0$)	BV_{CEO}	BD 205 BD 207	45 60	—	Vdc
Collector Cutoff Current ($V_{CB} = 55$ Vdc, $I_E = 0$) ($V_{CB} = 70$ Vdc, $I_E = 0$)	I_{CBO}	BD 205 BD 207	—	1.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	2.0	mAdc
DC current Gain ($I_C = 2$ A, $V_{CE} = 2$ V) ($I_C = 4$ A, $V_{CE} = 2$ V)	h_{FE}		30 15	—	
Collector-Emitter Saturation Voltage* ($I_C = 4$ Adc, $I_B = 0.4$ Adc)	$V_{CE(sat)}$		—	1.1	Vdc
Base-Emitter On Voltage* ($I_C = 4$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$		—	1.6	Vdc
Current-Gain-Bandwidth Product ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		1.5	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$.



When mounting the device, torque not to exceed 0.09 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.
All dimensions in millimeters

CASE 90

FIGURE 1 — ACTIVE REGION DC SAFE OPERATING AREA

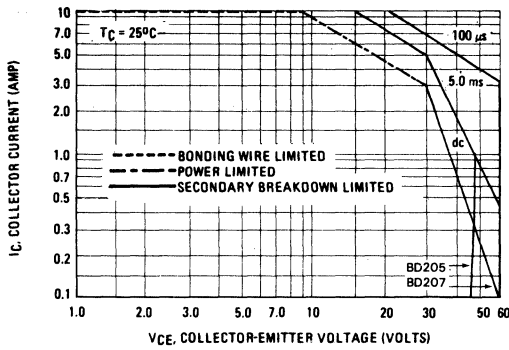


FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

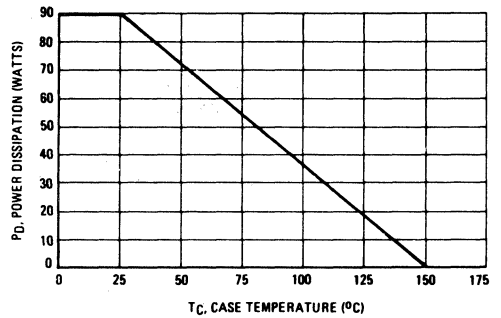


FIGURE 3 — "ON" VOLTAGES

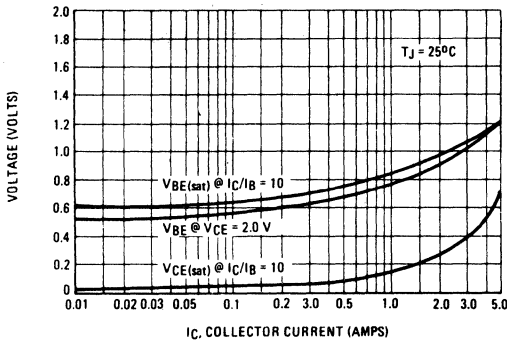


FIGURE 4 — CURRENT GAIN

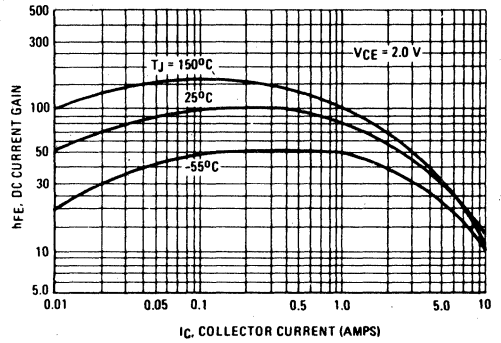
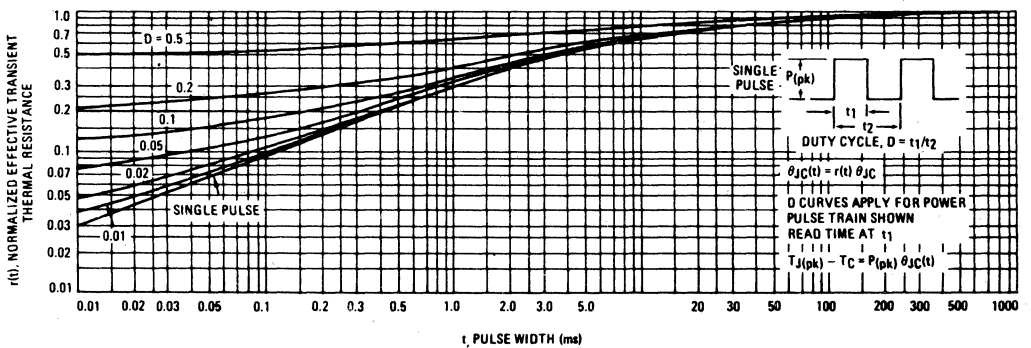


FIGURE 5 — THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD206
BD208

**PLASTIC HIGH POWER
 SILICON PNP TRANSISTOR**

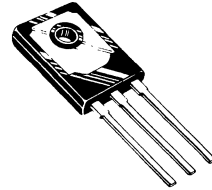
... designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current— $h_{FE} = 30$ (Min) @ $I_C = 2.0$ Adc
- BD 206, 208 are complementary with BD 205, 207

**10 AMPERE
 POWER TRANSISTOR**
PNP SILICON
45, 60 VOLTS
90 WATTS

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 206 BD 208	45 60	Vdc
Collector-Base Voltage	V_{CBO}	BD 206 BD 208	55 70	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150	°C



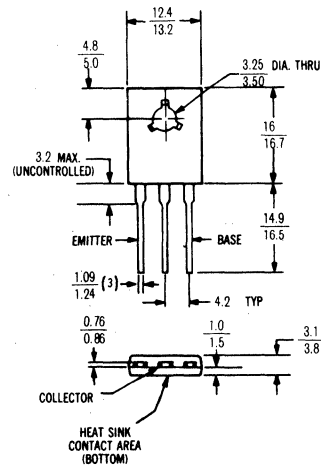
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.2$ Adc, $I_B = 0$)	V_{CEO}^*	BD 206 BD 208	45 60	—	Vdc
Collector Cutoff Current ($V_{CB} = 55$ Vdc, $I_E = 0$) ($V_{CB} = 70$ Vdc, $I_E = 0$)	I_{CBO}	BD 206 BD 208	—	1.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	2.0	mAdc
DC current Gain ($I_C = 2A, V_{CE} = 2$ V) ($I_C = 4A, V_{CE} = 2$ V)	h_{FE}		30 15	—	
Collector-Emitter Saturation Voltage* ($I_C = 4$ Adc, $I_B = 0.4$ Adc)	$V_{CE(sat)}^*$		—	1.1	Vdc
Base-Emitter On Voltage* ($I_C = 4$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}^*$		—	1.6	Vdc
Current-Gain-Bandwidth Product ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		1.5	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs . Duty Cycle $\leq 2.0\%$.



When mounting the device, torque not to exceed 0.09 m-kg.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.
 All dimensions in millimeters

CASE 90

FIGURE 1 — ACTIVE REGION DC SAFE OPERATING AREA

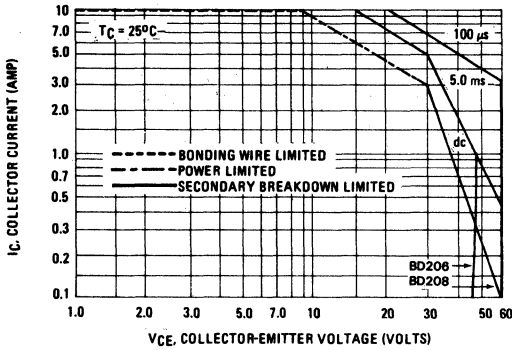


FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

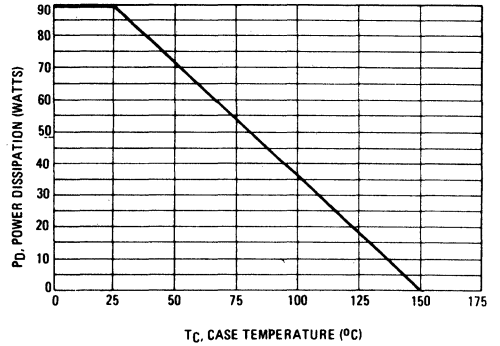


FIGURE 3 — "ON" VOLTAGES

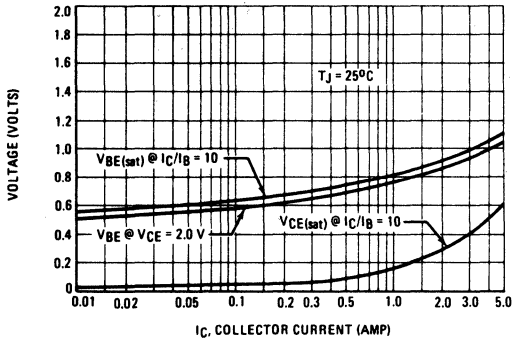


FIGURE 4 — CURRENT GAIN

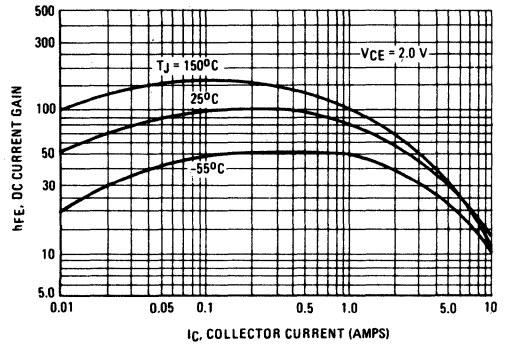
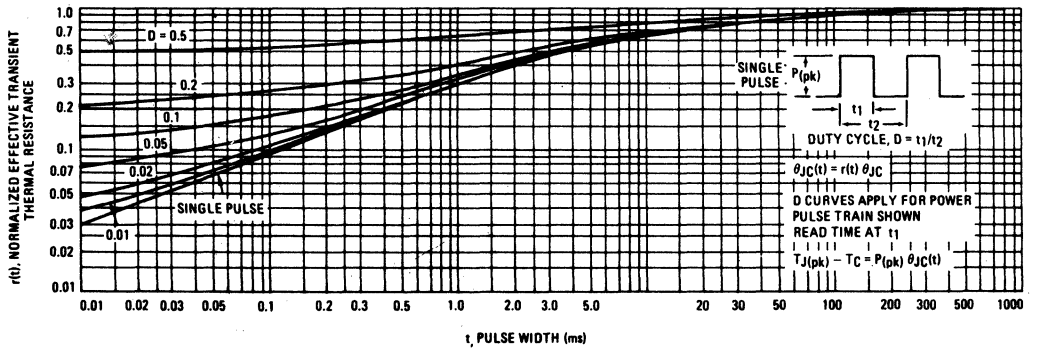


FIGURE 5 — THERMAL RESPONSE



3

BD232

NPN SILICON MEDIUM POWER TRANSISTORS

- For Power Output Stages and Line Driver in Television Receivers

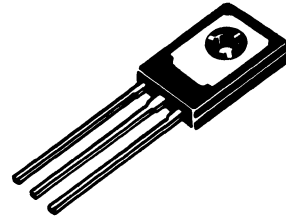
0.5 AMPERES

**NPN SILICON
 POWER TRANSISTOR**

**300 VOLTS
 20 WATTS**

MAXIMUM RATINGS

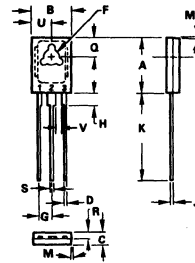
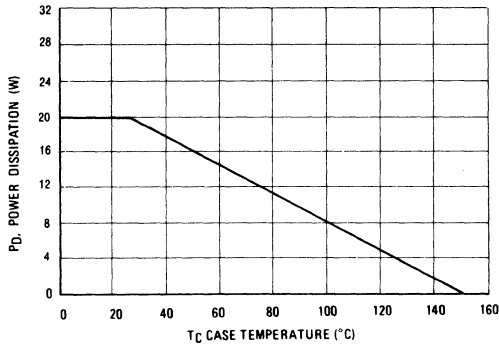
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Emitter Voltage	V_{CES}	500	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current - Continuous	I_C	0.5	Adc
Base Current	I_B	0.25	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$



THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^\circ\text{C}/\text{W}$

FIGURE 1 - POWER DERATING



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.433
B	2.60	2.74	0.102	0.108
C	2.52	2.66	0.100	0.105
D	0.51	0.66	0.020	0.026
F	2.80	3.17	0.110	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.90	0.93	0.035	0.037
K	14.61	16.63	0.575	0.654
M	± TYP			
Q	3.71	4.01	0.146	0.158
R	1.15	1.30	0.045	0.051
S	0.65	0.68	0.025	0.027
U	3.65	3.82	0.144	0.150
V	1.02	-	0.040	-

STYLE 1
 PIN 1 - EMITTER
 2 - COLLECTOR
 3 - BASE

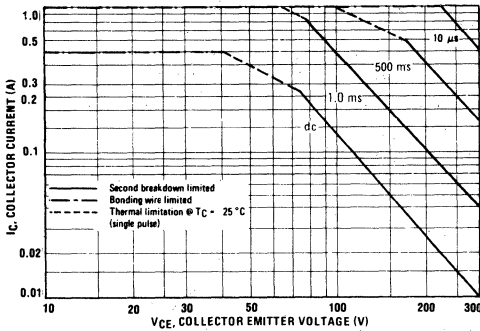
NOTES:
 1. M - MAIN TERMINAL
 2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010)
 DIM TO DIM A & B AT MAXIMUM MATERIAL
 CONDITION

**CASE 77-05
 TO-126**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

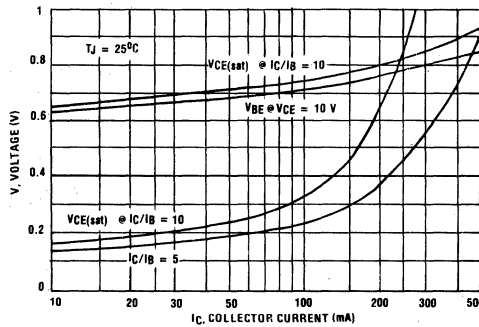
Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS (1)				
Collector-Emitter Sustaining Voltage ($I_C = 10 \text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	300	—	Vdc
Collector Cutoff Current ($V_{CE} = 500 \text{ Vdc}$, $V_{BE} = 0$)	I_{CES}	—	0.1	mAdc
Base-Emitter Voltage ($V_{CE} = 5 \text{ Vdc}$, $I_C = 150 \text{ mA}$)	V_{BE}	—	1.0	Vdc
DC Current Gain ($V_{CE} = 5 \text{ V}$, $I_C = 50 \text{ mA}$) ($V_{CE} = 5 \text{ V}$, $I_C = 150 \text{ mA}$)	h_{FE}	25 20	150	
Collector Emitter Saturation Voltage ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$)	$V_{CE(sat)}$	—	1.0	Vdc

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of figure 6 is based on $T_{J(pk)} = 150^\circ\text{C}$, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 3 – "ON" VOLTAGES



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD233
BD235
BD237

**PLASTIC MEDIUM POWER
 SILICON NPN TRANSISTOR**

... designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

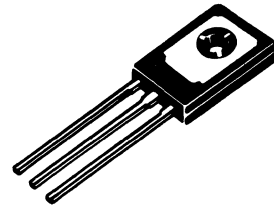
- DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 0.15$ Adc
- BD 233, 235, 237 are complementary with BD 234, 236, 238

**2 AMPERE
 POWER TRANSISTOR**

NPN SILICON
45, 60, 80 VOLTS
25 WATTS

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 233 BD 235 BD 237	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 233 BD 235 BD 237	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		2.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation $T_C = 25^\circ\text{C}$	P_D		25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		55 to +150	$^\circ\text{C}$



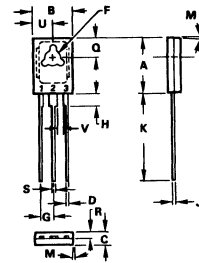
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	50	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$)	V_{CEO}	BD 233 BD 235 BD 237	45 60 80	—	Vdc
Collector Cutoff Current ($V_{CB} = 45$ Vdc, $I_C = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	I_{CBO}	BD 233 BD 235 BD 237	—	0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mAdc
DC current Gain ($I_C = 0.15$ A, $V_{CE} = 2$ V) ($I_C = 1$ A, $V_{CE} = 2$ V)	h_{FE1} h_{FE2}		40 26	—	
Collector-Emitter Saturation Voltage* ($I_C = 1$ Adc, $I_B = 0.1$ Adc)	$V_{CE(sat)}$		—	0.6	Vdc
Base-Emitter On Voltage* ($I_C = 1$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$		—	1.3	Vdc
Current-Gain-Bandwidth Product ($I_C = 250$ mA, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$.



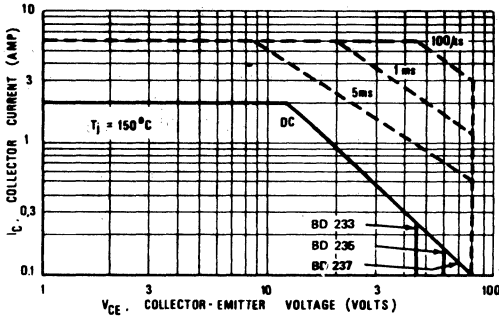
MILLIMETERS		INCHES		
MIN	MAX	MIN	MAX	
A	10.80	11.00	0.425	0.430
B	7.50	7.74	0.295	0.305
C	2.42	2.60	0.095	0.105
D	0.51	0.60	0.020	0.025
F	2.83	3.17	0.115	0.125
G	2.32	2.40	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.50	0.63	0.019	0.025
K	14.81	16.63	0.575	0.655
M	P-TYP			Q-TYP
Q	3.76	4.01	0.148	0.158
R	1.52	1.90	0.060	0.075
S	0.64	0.80	0.025	0.032
U	3.68	3.81	0.145	0.150
V	1.02	—	0.040	—

STYLE 1:
 PIN 1: EMITTER
 2: COLLECTOR
 3: BASE

NOTES:
 1. MT = MAIN TERMINAL.
 2. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010")
 DIA TO DIM A & B AT MAXIMUM MATERIAL
 CONDITION.

**CASE 77-05
 TO-126**

FIGURE 1 - ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C - V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 - COLLECTOR SATURATION REGION

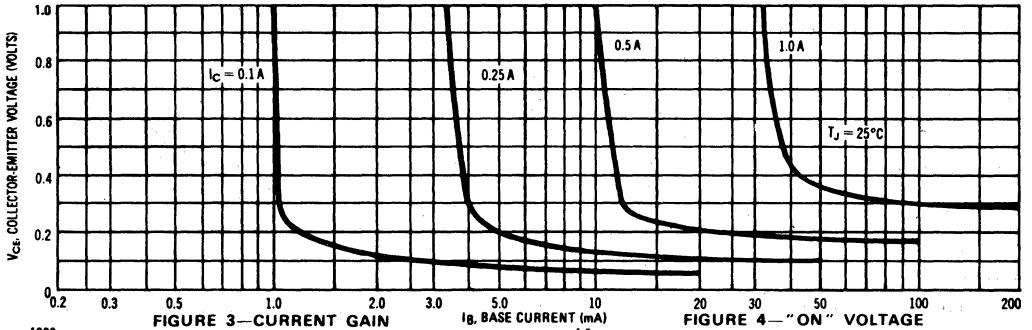


FIGURE 3 - CURRENT GAIN

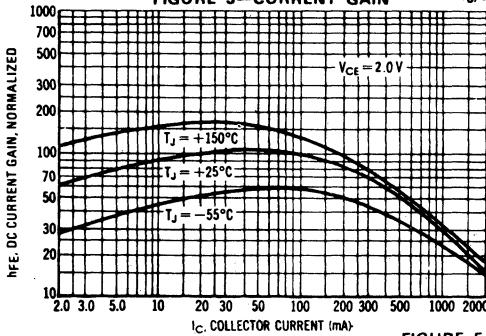


FIGURE 4 - "ON" VOLTAGE

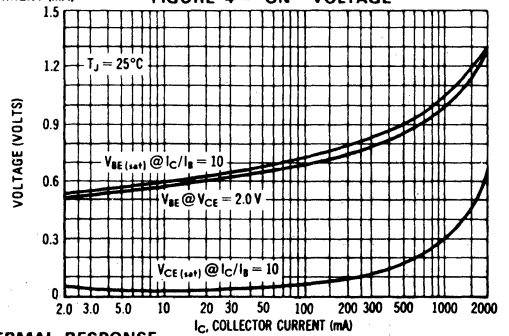
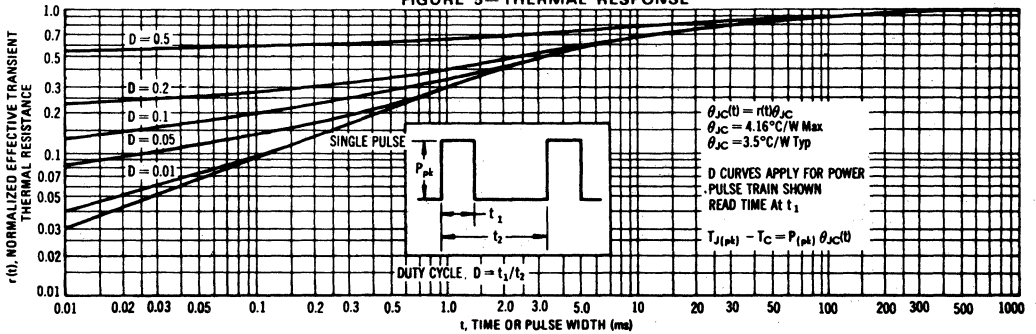


FIGURE 5 - THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
 TECHNICAL DATA

BD234
BD236
BD238

**PLASTIC MEDIUM POWER
 SILICON PNP TRANSISTOR**

designed for use in 5 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 0.15$ Adc
- BD 234, 236, 238 are complementary with BD 233, 235, 237

**2 AMPERE
 POWER TRANSISTOR**

PNP SILICON

**45, 60, 80 VOLTS
 25 WATTS**

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD 234 BD 236 BD 238	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD 234 BD 236 BD 238	45 60 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		2.0	Adc
Base Current	I_B		1.0	Adc
Total Device Dissipation $T_C = 25^\circ\text{C}$	P_D		25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150	$^\circ\text{C}$

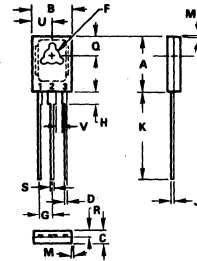
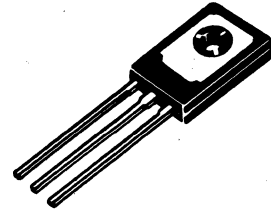
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$)	BV_{CEO}	BD 234 BD 236 BD 238	45 60 80	—	Vdc
Collector Cutoff Current ($V_{CB} = 45$ Vdc, $I_E = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	I_{CBO}	BD 234 BD 236 BD 238	—	0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mAdc
DC current Gain ($I_C = 0.15$ A, $V_{CE} = 2$ V) ($I_C = 1$ A, $V_{CE} = 2$ V)	h_{FE1} h_{FE2}		40 25	—	
Collector-Emitter Saturation Voltage* ($I_C = 1$ Adc, $I_B = 0.1$ Adc)	$V_{CE(sat)}$		—	0.6	Vdc
Base-Emitter On Voltage* ($I_C = 1$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$		—	1.3	Vdc
Current-Gain-Bandwidth Product ($I_C = 250$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$.



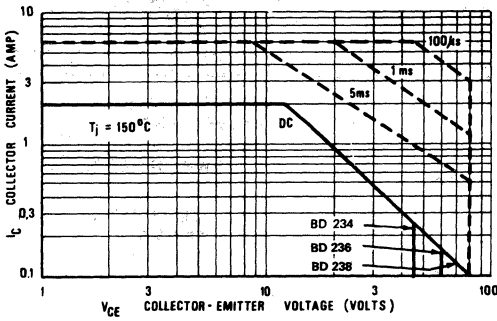
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.80	11.00	0.425	0.430
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.025
F	2.80	3.12	0.110	0.125
G	2.30	2.46	0.091	0.097
H	1.72	2.21	0.060	0.086
J	0.29	0.45	0.015	0.018
K	14.41	15.63	0.570	0.615
M			\varnothing TYP	\varnothing TYP
Q	3.76	4.01	0.148	0.158
R	1.15	1.35	0.045	0.055
S	0.84	0.98	0.035	0.039
V	3.80	3.95	0.149	0.155
W	1.02	—	0.040	—

STYLE 1:
 PIN 1: EMITTER
 2: COLLECTOR
 3: BASE

NOTES:
 1. M7 - MOUNTING TERMINAL
 2. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010")
 DIA TO DIM A & B AT MAXIMUM MATERIAL
 CONDITION.

**CASE 77-05
 TO-126**

FIGURE 1 - ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C - V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 - COLLECTOR SATURATION REGION

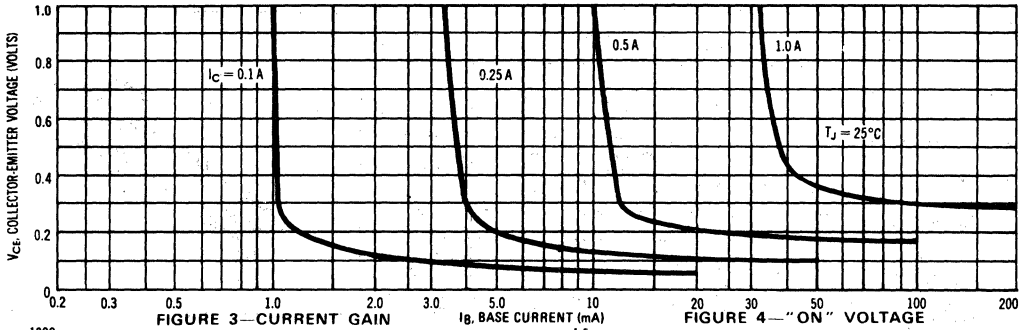


FIGURE 3 - CURRENT GAIN

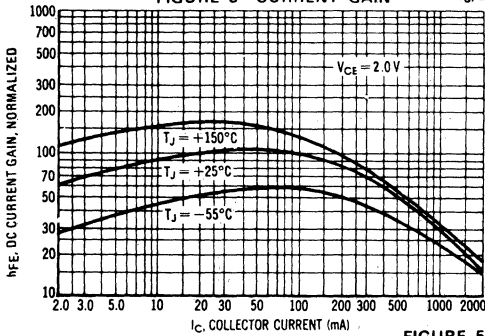


FIGURE 4 - "ON" VOLTAGE

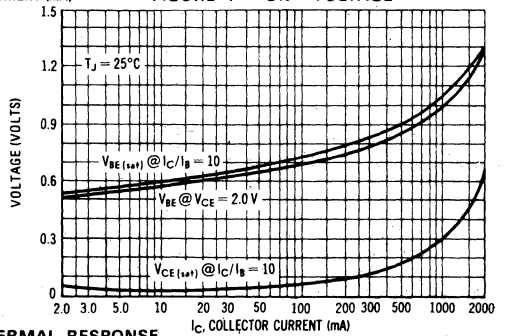
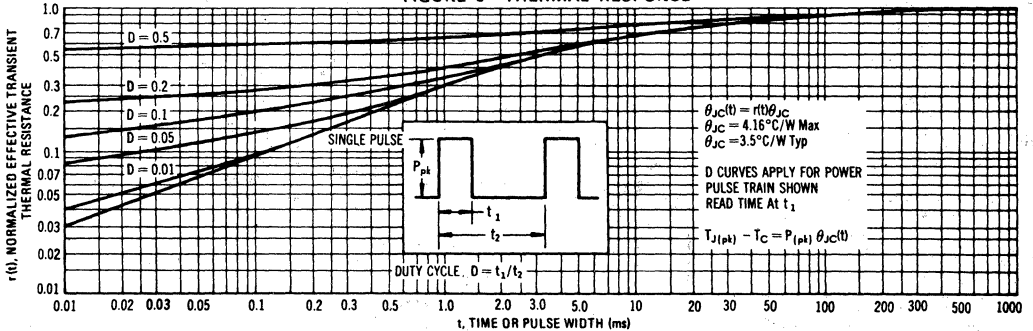


FIGURE 5 - THERMAL RESPONSE



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

... designed for use in general purpose amplifier and switching applications. Compact TO-220 AB package. TO-66 leadform also available ordered with "66" suffix.

MAXIMUM RATINGS

Rating	Symbol	BD239 BD240	BD239A BD240A	BD239B BD240B	BD239C BD240C	Unit
Collector-Emitter Voltage	V_{CE0}	45	60	80	100	Vdc
Collector-Emitter Voltage	V_{CB}	55	70	90	115	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous	I_C	2				Adc
Collector Current - Peak		4				Adc
Base Current	I_B	0.8				Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	30				Watts
		0.24				W/ $^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0				Watts
		0.016				W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (See Note 3)	E	32				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.167	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 30 \text{ mAdc}, I_B = 0$)	BD239, BD240 BD239A, BD240A BD239B, BD240B BD239C, BD240C	$V_{CE0(sus)}$	45 60 80 100	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}, I_B = 0$) ($V_{CE} = 60 \text{ Vdc}, I_B = 0$)	BD239A, BD240A BD239B, C, BD240B, C	I_{CE0}	- 0.3	mAdc
Collector Cutoff Current ($V_{CE} = 45 \text{ Vdc}, V_{EB} = 0$) ($V_{CE} = 60 \text{ Vdc}, V_{EB} = 0$) ($V_{CE} = 80 \text{ Vdc}, V_{EB} = 0$) ($V_{CE} = 100 \text{ Vdc}, V_{EB} = 0$)	BD239, BD240 BD239A, BD240A BD239B, BD240A BD239C, BD240C	I_{CES}	- 200 200 200	μAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)		I_{E0}	- 1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 0.2 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$)		h_{FE}	40 15	-
Collector-Emitter Saturation Voltage ($I_C = 1.0 \text{ Adc}, I_B = 200 \text{ mAdc}$)		$V_{CE(sat)}$	- 0.7	Vdc
Base-Emitter On Voltage ($I_C = 1.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$)		$V_{BE(on)}$	- 1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain - Bandwidth Product (2) ($I_C = 200 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f_{test} = 1 \text{ MHz}$)		f_T	3.0	MHz
Small-Signal Current Gain ($I_C = 0.2 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 1 \text{ kHz}$)		h_{fe}	20	-

(1) Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.

(2) $f_T = h_{FE} \cdot f_{test}$

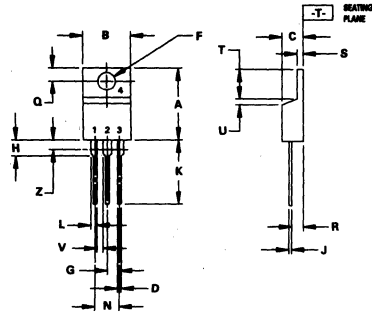
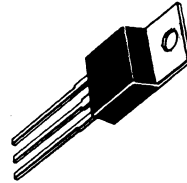
(3) This rating based on testing with $L_C = 20 \text{ mH}, R_{BE} = 100 \Omega, R_E = 0.1 \Omega, I_C = 1.8 \text{ A}$.

NPN
BD239
BD239A
BD239B
BD239C

PNP
BD240
BD240A
BD240B
BD240C

2 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

45, 60, 80, 100 VOLTS
30 WATTS



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS			INCHES		
	MIN	MAX		MIN	MAX	
A	14.48	16.75	0.570	0.620		
B	9.86	10.28	0.390	0.405		
C	4.07	4.82	0.160	0.190		
D	0.84	0.98	0.0325	0.0395		
F	3.81	3.73	0.142	0.147		
G	2.42	2.66	0.095	0.105		
H	2.80	3.93	0.110	0.155		
J	0.46	0.71	0.018	0.028		
K	12.70	14.27	0.500	0.562		
L	1.15	1.38	0.045	0.055		
N	4.83	5.33	0.190	0.210		
Q	2.54	3.04	0.100	0.120		
R	2.04	2.79	0.080	0.110		
S	1.15	1.38	0.045	0.055		
T	5.97	6.47	0.235	0.255		
U	0.80	1.27	0.030	0.050		
V	1.15	-	0.045	-		
Z	-	2.04	-	0.080		

STYLE 1:

1. PIN 1, BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

3

**BD239, BD239A, BD239B, BD239C NPN
BD240, BD240A, BD240B, BD240C PNP**

FIGURE 1 – DC CURRENT GAIN

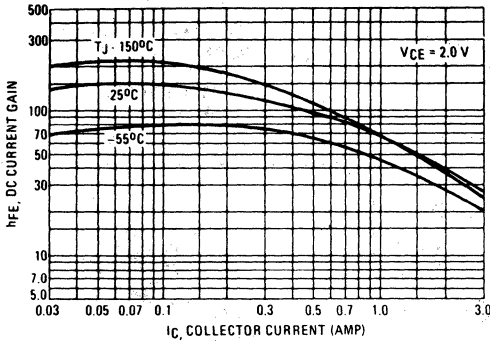


FIGURE 2 – TURN-OFF TIME

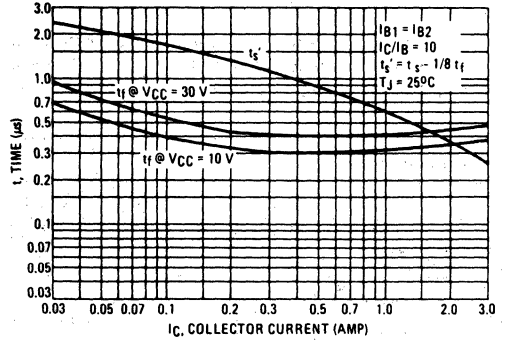


FIGURE 3 – SWITCHING TIME EQUIVALENT CIRCUIT

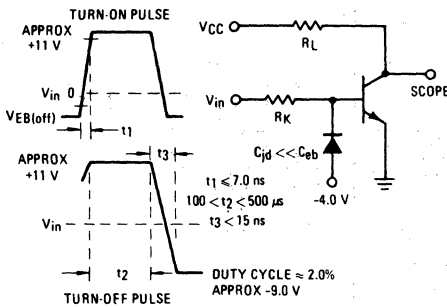


FIGURE 4 – TURN-ON TIME

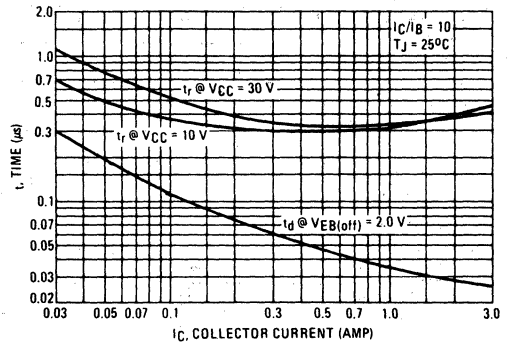
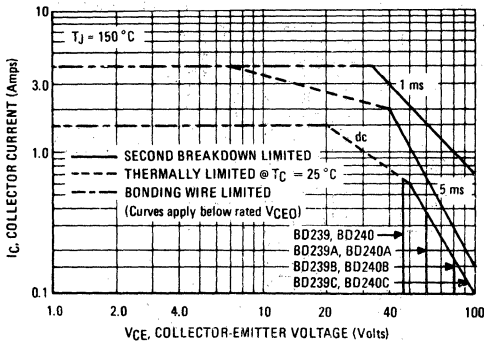


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

... designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage –
 $V_{CE} = 1.2 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- Collector-Emitter Sustaining Voltage –
 $V_{CEO} (\text{sus}) = 45 \text{ Vdc (Min.) BD241, BD242}$
 $= 60 \text{ Vdc (Min.) BD241A, BD242A}$
 $= 80 \text{ Vdc (Min.) BD241B, BD242B}$
 $= 100 \text{ Vdc (Min.) BD241C, BD242C}$
- High Current Gain – Bandwidth Product
 $f_T = 3.0 \text{ MHz (Min) @ } I_C = 500 \text{ mA dc}$
- Compact TO-220 AB Package
- TO-66 Leadform Also Available ordered with "-66" suffix.

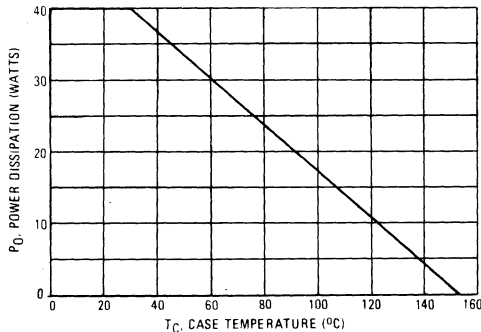
MAXIMUM RATINGS

Rating	Symbol	BD241 BD242	BD241A BD242A	BD241B BD242B	BD241C BD242C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Emitter Voltage	V_{CES}	55	70	90	115	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous	I_C	3.0				Adc
Collector Current - Peak		5.0				Adc
Base Current	I_B	1.0				Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40				Watts
		0.32				W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

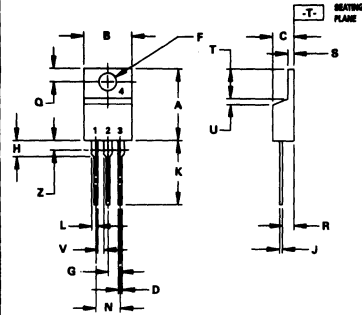
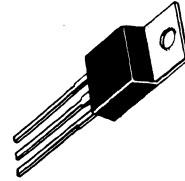
FIGURE 1 – POWER DERATING



NPN	PNP
BD241	BD242
BD241A	BD242A
BD241B	BD242B
BD241C	BD242C

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON

45, 60, 80, 100 VOLTS
40 WATTS



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.62	0.160	0.180
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.106
H	2.90	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.38	0.045	0.055
N	4.82	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.94	2.79	0.090	0.110
S	1.15	1.38	0.045	0.055
T	5.97	6.47	0.235	0.256
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

- STYLE 1:
1. PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

BD241, BD241A, BD241B, BD241C NPN BD242, BD242A, BD242B, BD242C PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit.
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ¹ ($I_C = 30\text{ mA}$, $I_B = 0$)	BD241, BD242 BD241A, BD242A BD241B, BD242B BD241C, BD242C	V_{CEO}	45 60 80 100	Vdc
Collector Cutoff Current ($V_{CE} = 30\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 60\text{ Vdc}$, $I_B = 0$)	BD241, BD241A, BD242, BD242A, BD241B, BD241C, BD242B, BD242C	I_{CEO}		mAdc 0.3 0.3
Collector Cutoff Current ($V_{CE} = 45\text{ Vdc}$, $V_{EB} = 0$) ($V_{CE} = 60\text{ Vdc}$, $V_{EB} = 0$) ($V_{CE} = 80\text{ Vdc}$, $V_{EB} = 0$) ($V_{CE} = 100\text{ Vdc}$, $V_{EB} = 0$)	BD241, BD242 BD241A, BD242A BD241B, BD242B BD241C, BD242C	I_{CES}		μAdc 200 200 200 200
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)		I_{EBO}		mAdc 1.0

ON CHARACTERISTICS¹

DC Current Gain ($I_C = 1.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) ($I_C = 3.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	h_{FE}	25 10		
Collector-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 600\text{ Adc}$)	$V_{CE(sat)}$		1.2	Vdc
Base-Emitter On Voltage ($I_C = 3.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	$V_{BE(on)}$		1.8	Vdc

DYNAMIC CHARACTERISTICS

Current Gain - Bandwidth Product ² ($I_C = 500\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1\text{ MHz}$)	f_T	3.0		MHz
Small-Signal Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ kHz}$)	h_{fe}	20		

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

² $f_T = |h_{fe}| \bullet f_{test}$

3

FIGURE 2 - SWITCHING TIME EQUIVALENT CIRCUIT

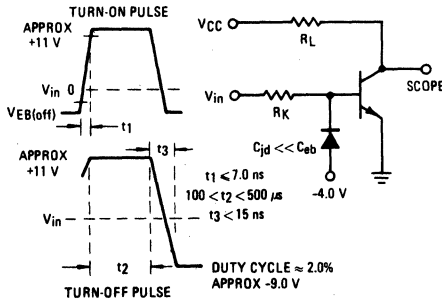
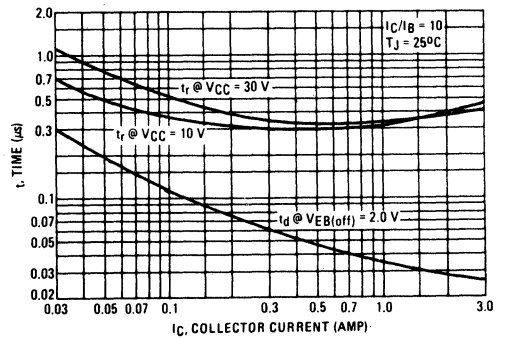


FIGURE 3 - TURN-ON TIME



**BD241, BD241A, BD241B, BD241C NPN
BD242, BD242A, BD242B, BD242C PNP**

FIGURE 4 – THERMAL RESPONSE

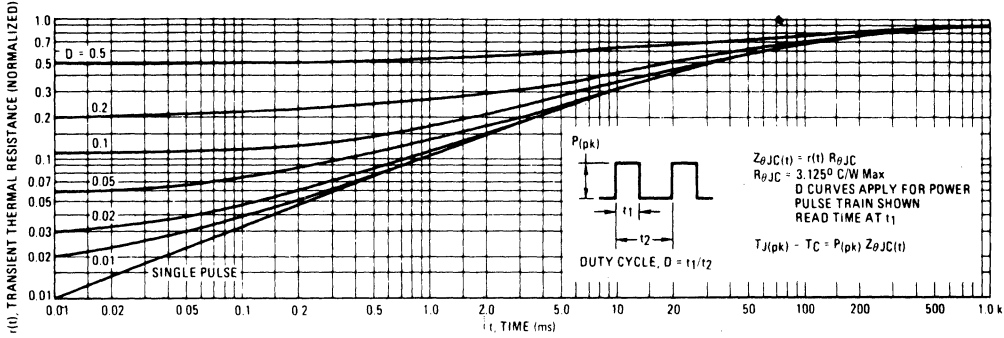
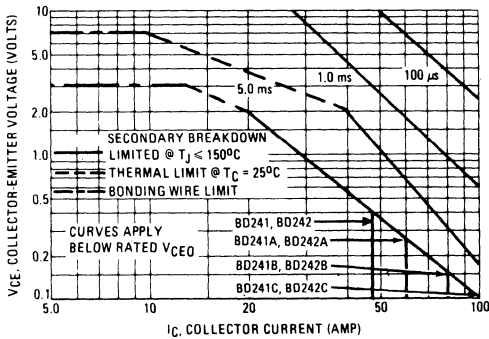


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 5 is based on $T_{j(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{j(pk)} \leq 150^{\circ}\text{C}$. $T_{j(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 6 – TURN-OFF TIME

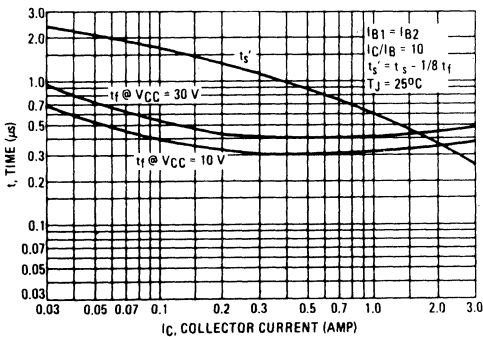
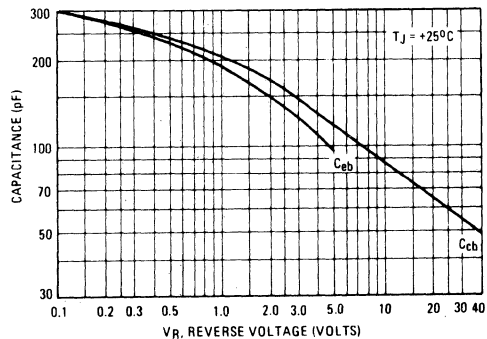


FIGURE 7 – CAPACITANCE



**BD241, BD241A, BD241B, BD241C NPN
BD242, BD242A, BD242B, BD242C PNP**

FIGURE 8 – DC CURRENT GAIN

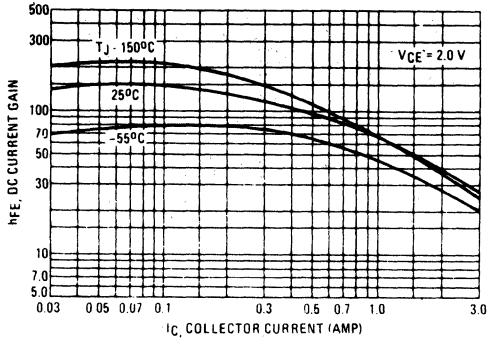


FIGURE 9 – COLLECTOR SATURATION REGION

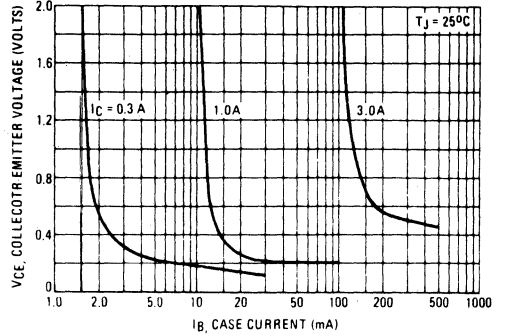


FIGURE 10 – "ON" VOLTAGES

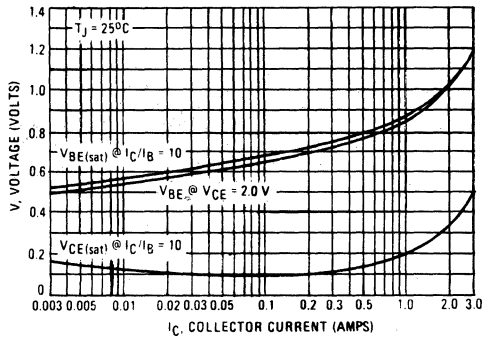


FIGURE 11 – TEMPERATURE COEFFICIENTS

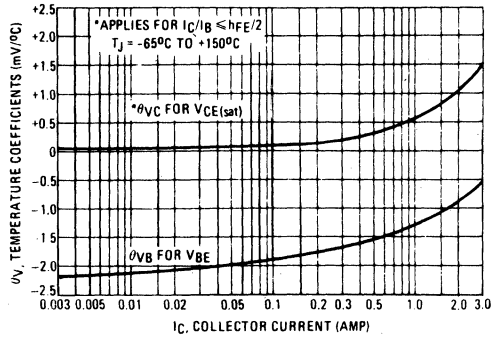


FIGURE 12 – COLLECTOR CUT-OFF REGION

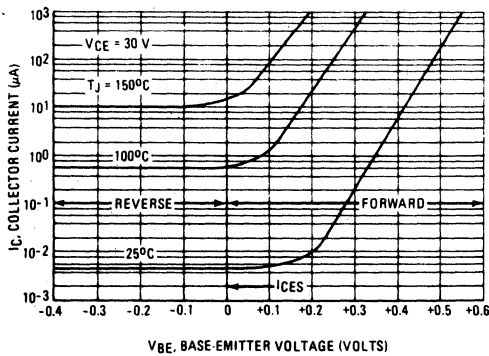
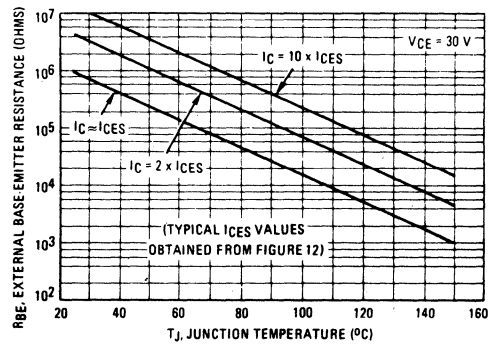


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



BD243
BD243A
BD243B
BD243C

BD244
BD244A
BD244B
BD244C

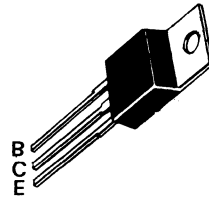
**COMPLEMENTARY SILICON PLASTIC
 POWER TRANSISTORS**

... designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.5 \text{ Vdc (Max) @ } I_C = 6.0 \text{ Adc}$
- Collector-Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 45 \text{ Vdc (Min) — BD243, BD244}$
 $= 60 \text{ Vdc (Min) — BD243A, BD244A}$
 $= 80 \text{ Vdc (Min) — BD243B, BD244B}$
 $= 100 \text{ Vdc (Min) — BD243C, BD244C}$
- High Current Gain – Bandwidth Product
 $f_T = 3.0 \text{ MHz (Min) @ } I_C = 500 \text{ mAdc}$
- Compact TO-220 AB Package

**6 AMPERE
 POWER TRANSISTORS
 COMPLEMENTARY SILICON**

**45-60-80-100 VOLTS
 65 WATTS**



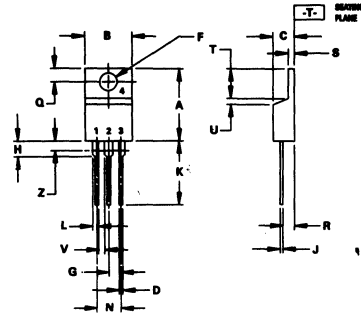
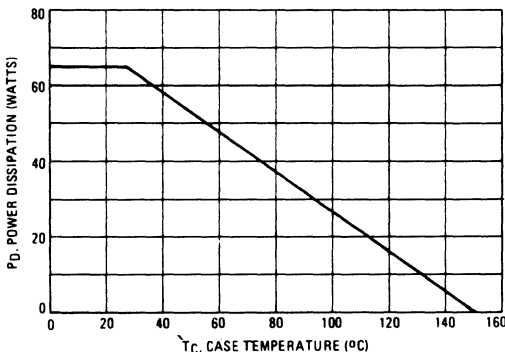
MAXIMUM RATINGS

Rating	Symbol	BD243 BD244	BD243A BD244A	BD243B BD244B	BD243C BD244C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current Continuous Peak	I_C	← 6 →				Adc
		← 10 →				
Base Current	I_B	← 2.0 →				Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 65 →				Watts
		← 0.52 →				
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →				$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ\text{C/W}$

FIGURE 1 – POWER DERATING



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.406
C	4.07	4.82	0.160	0.190
D	0.94	0.98	0.035	0.039
F	3.81	3.73	0.150	0.147
G	2.42	2.86	0.095	0.105
H	2.80	3.83	0.110	0.150
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	6.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
 PIN 1: BASE
 2: COLLECTOR
 3: EMITTER
 4: COLLECTOR

**CASE 221A-04
 TO-220AB**

BD243, 243A, 243B, 243C, BD244, 244A, 244B, 244C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I _C = 30 mAdc, I _B = 0)	BD243, BD244 BD243A, BD244A BD243B, BD244B BD243C, BD244C	V _{CEO(sus)}	45 60 80 100	— — — —	Vdc
Collector Cutoff Current (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 60 Vdc, I _B = 0)	BD243, BD243A, BD244, BD244A BD243B, BD243C, BD244B, BD244C	I _{CEO}	— —	0.7 0.7	mAdc
Collector Cutoff Current (V _{CE} = 45 Vdc, V _{EB} = 0) (V _{CE} = 60 Vdc, V _{EB} = 0) (V _{CE} = 80 Vdc, V _{EB} = 0) (V _{CE} = 100 Vdc, V _{EB} = 0)	BD243, BD244 BD243A, BD244A BD243B, BD244B BD243C, BD244C	I _{CES}	— — — —	400 400 400 400	μAdc
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)		I _{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I _C = 0.3 Adc, V _{CE} = 4.0 Vdc) (I _C = 3.0 Adc, V _{CE} = 4.0 Vdc)		h _{FE}	30 15	— —	—
Collector-Emitter Saturation Voltage (I _C = 6.0 Adc, I _B = 1 Adc)		V _{CE(sat)}	—	1.5	Vdc
Base-Emitter On Voltage (I _C = 6.0 Adc, V _{CE} = 4.0 Vdc)		V _{BE(on)}	—	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain - Bandwidth Product (2) (I _C = 500 mAdc, V _{CE} = 10 Vdc, f _{test} = 1 MHz)		f _T	3.0	—	MHz
Small-Signal Current Gain (I _C = 0.5 Adc, V _{CE} = 10 Vdc, f = 1 kHz)		h _{fe}	20	—	—

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) f_T = h_{fe} • f_{test}

3

FIGURE 2 - SWITCHING TIME TEST CIRCUIT

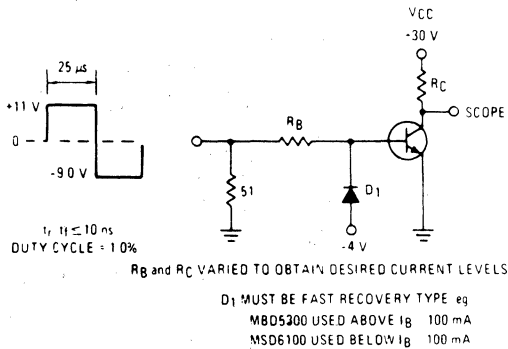


FIGURE 3 - TURN-ON TIME

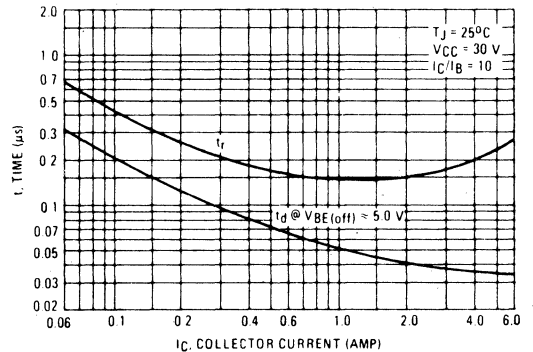


FIGURE 4 - THERMAL RESPONSE

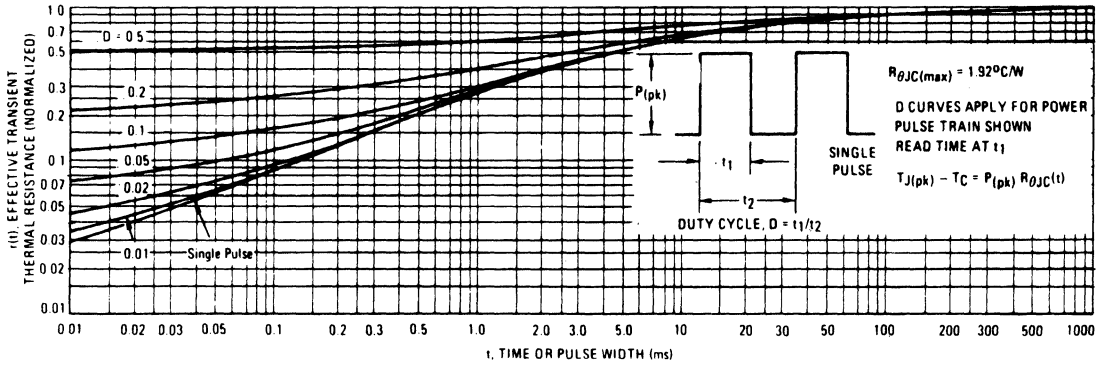
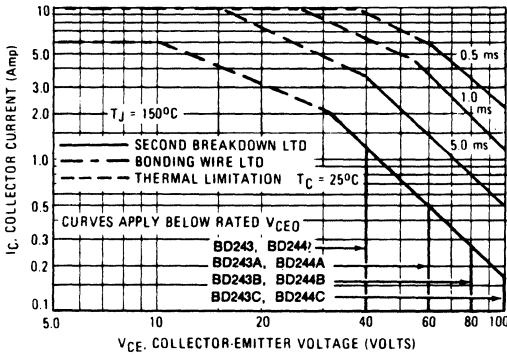


FIGURE 5 - ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor - average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ C$; T_c is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (See AN-415A).

FIGURE 6 - TURN-OFF TIME

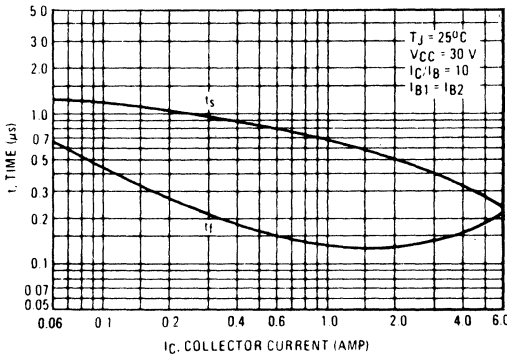
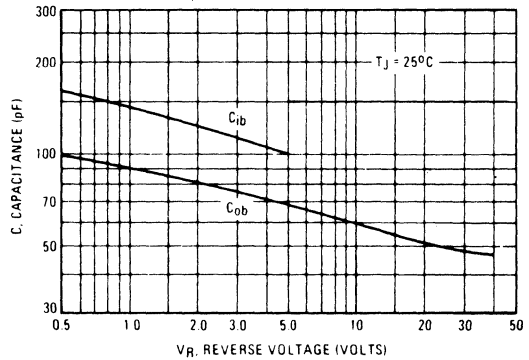
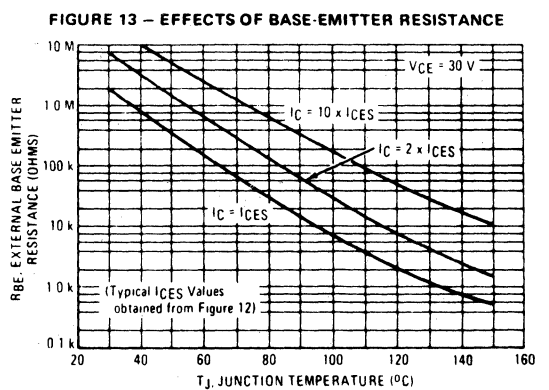
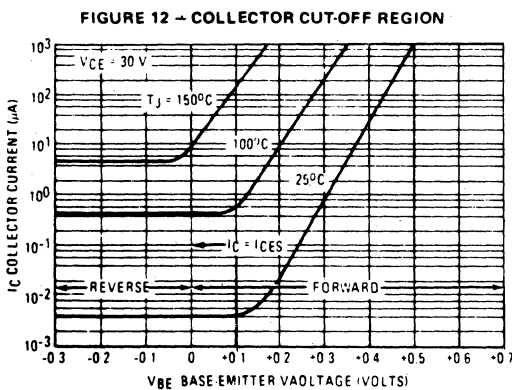
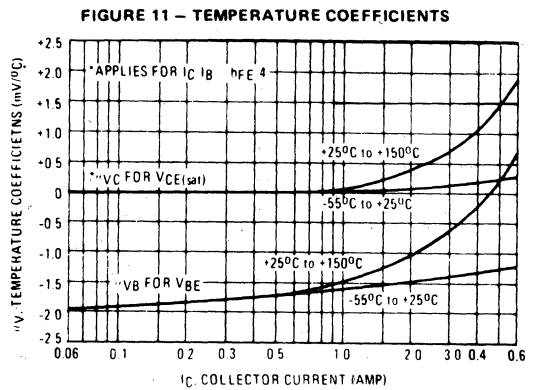
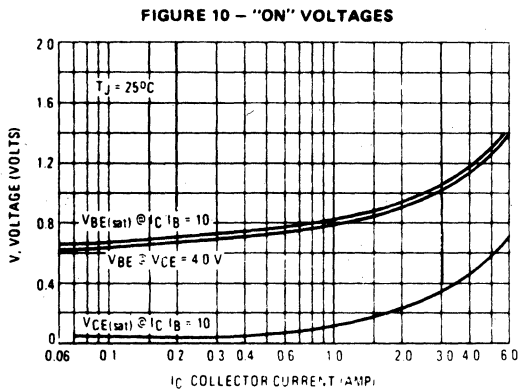
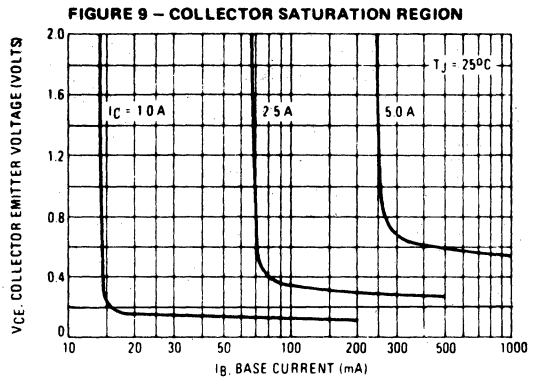
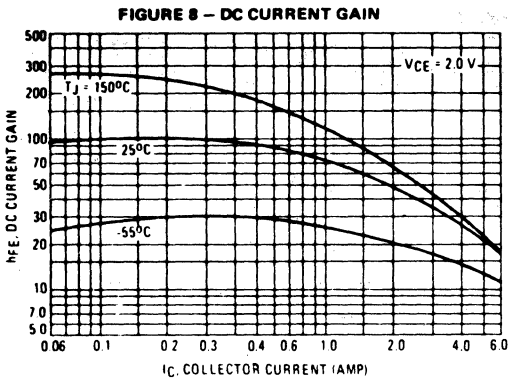


FIGURE 7 - CAPACITANCE





3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
BD311
PNP
BD312

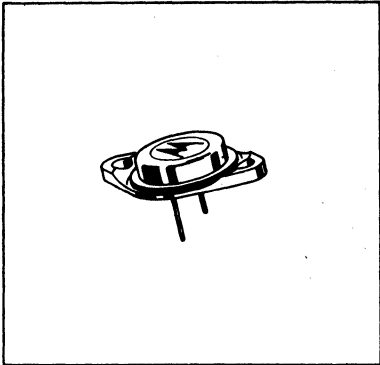
**COMPLEMENTARY SILICON
HIGH-POWER TRANSISTORS**

... designed for high quality amplifiers operating up to 60 Watts into 4 ohm load.

- High DC Current Gain
- Excellent Safe Operating Area
- High Current Gain – Bandwidth Product – Typical
 $f_T = 4.0 \text{ MHz} @ I_C = 0.5 \text{ A}$

**10 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS**

**60 VOLTS
115 WATTS**

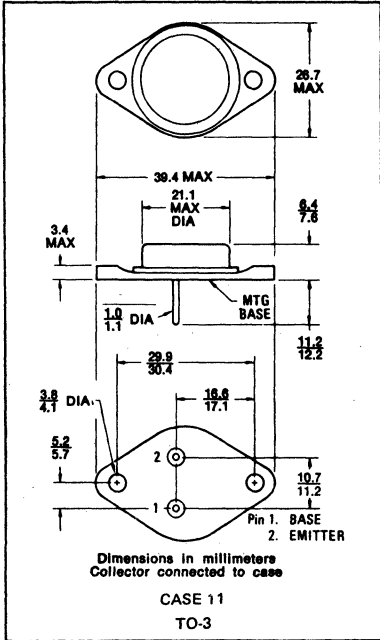
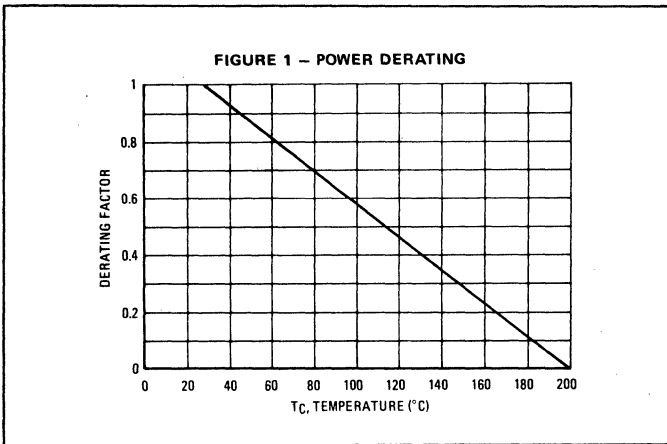


MAXIMUM RATINGS

Rating	Symbol	BD311/312	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	10	Adc
Peak		20	
Base Current	I_B	4.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	115	Watts
Derate above 25°C		0.658	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit.
Thermal Resistance, Junction to Case	θ_{JC}	1.52	$^\circ\text{C/W}$



BD311 NPN, BD312 PNP

ELECTRICAL CHARACTERISTICS* ($T_C = 25^\circ\text{C}$ unless otherwise noted)

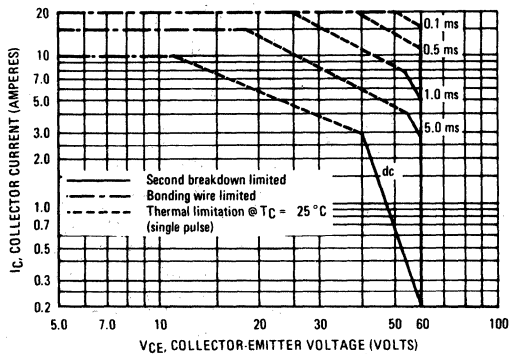
Characteristic	Symbol	Min.	Max.	Unit.
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ¹ ($I_C = 200\text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	60		Vdc
Collector-Base Cutoff Current ($V_{CB} = \text{Rated } V_{CB}$, $I_E = 0$)	I_{CBO}		1.0	mAdc
Emitter-Base Cutoff Current ($V_{BE} = 7.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}		1.0	mAdc
ON CHARACTERISTICS¹				
DC Current Gain ($I_C = 5.0\text{ Vdc}$, $V_{CE} = 4.0\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	h_{FE}	25 5		—
Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.5\text{ Adc}$)	$V_{CE(sat)}$		1.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.5\text{ Adc}$)	$V_{BE(sat)}$		1.8	Vdc
Base-Emitter On Voltage ($I_C = 5.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	$V_{BE(on)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS¹				
Current-Gain — Bandwidth Product ² ($I_C = 0.5\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1.0\text{ MHz}$)	f_T	4.0		MHz
SECOND BREAKDOWN				
Second Breakdown Collector Current ($V_{CE} = 39\text{ Vdc}$, $t = 0.5\text{ sec.}$) ($V_{CE} = 50\text{ Vdc}$, $t = 0.5\text{ sec.}$)	$I_{S/B}$	2.95 0.60		Adc

¹ Pulse test: Pulse width $< 300\ \mu\text{s}$, Duty Cycle $> 2\%$

² $f_T = |h_{fe}| \cdot f_{test}$

3

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate. Second breakdown pulse limits are valid for duty cycles to 10%.

At high case temperatures, thermal limitation may reduce the power that can be handled to values less than the limitations imposed by second breakdown.

BD311 NPN, BD312 PNP

PNP DEVICE
BD312

NPN DEVICE
BD311

FIGURE 3 - DC CURRENT GAIN

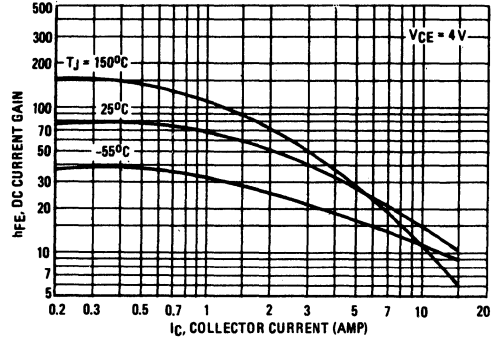
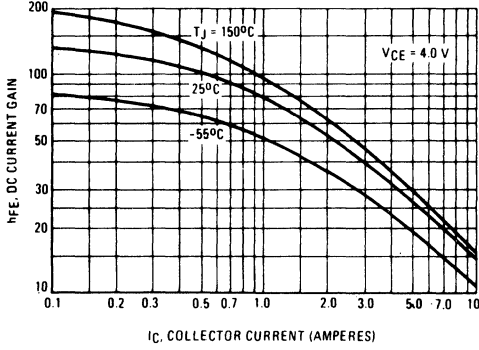
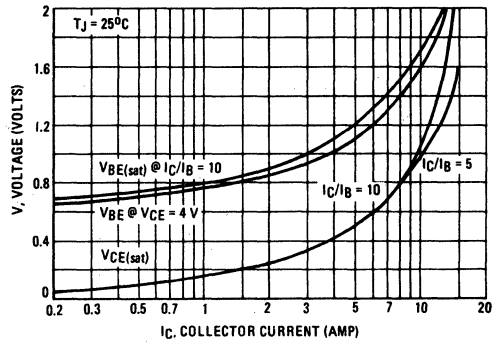
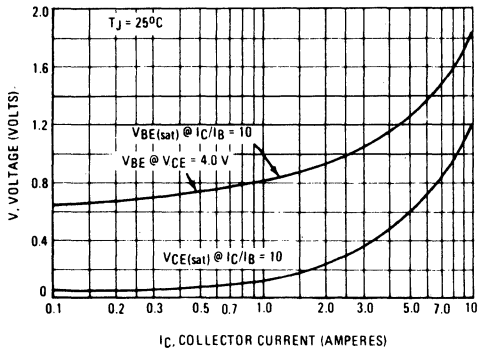


FIGURE 4 - "ON" VOLTAGES



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
BD315, BD316
PNP
BD317, BD318

**COMPLEMENTARY SILICON
HIGH-POWER TRANSISTORS**

... designed for high quality amplifiers operating up to 100 Watts into 4 ohm load with BD315, BD316 and into 8 ohm load with BD317, BD318.

- High DC Current Gain
- Excellent Safe Operating Area
- High Current Gain — Bandwidth Product — Typical
 $f_T = 2.0 \text{ MHz @ } I_C = 1.0 \text{ A}$

**16 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS**

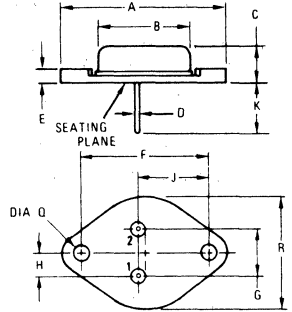
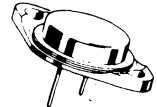
**80-100 VOLTS
200 WATTS**

MAXIMUM RATINGS

Rating	Symbol	BD315 BD316	BD317 BD318	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	16 20		A dc
Base Current — Continuous	I_B	5.0		A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	200 1.14		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	$^\circ\text{C/W}$



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE
1. DIM "Q" IS DIA

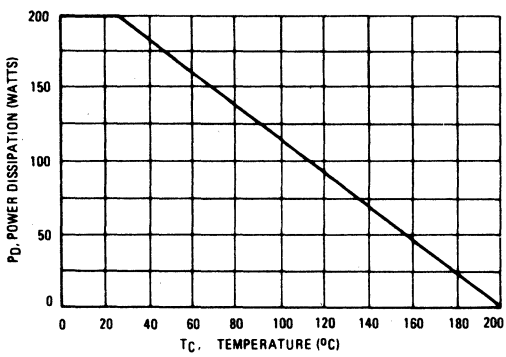
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

Collector connected to case

CASE 11 (TO-3)

3

FIGURE 1 — POWER DERATING



BD315, BD316, BD317, BD318

* ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

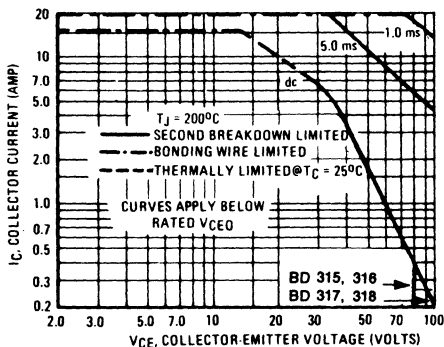
Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I _C = 200 mAdc, I _B = 0)	BD315, BD316 BD317, BD318	V _{CEO (100s)}	80 100	— —	Vdc
Collector-Base Cutoff Current (V _{CB} = Rated V _{CB} , I _E = 0)		I _{CBO}	—	1.0	mAdc
Emitter-Base Cutoff Current (V _{BE} = 7.0 Vdc, I _C = 0)		I _{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain I _C = 5.0 Adc, V _{CE} = 4.0 Vdc I _C = 8.0 Adc, V _{CE} = 4.0 Vdc I _C = 10 Adc, V _{CE} = 4.0 Vdc	BD317, BD318 BD315, BD316 All Types	h _{FE}	25 25 15	—	—
Collector-Emitter Saturation Voltage I _C = 8.0 Adc, I _B = 0.8 Adc		V _{CE (sat)}	—	1.0	Vdc
Base-Emitter Saturation Voltage I _C = 8.0 Adc, I _B = 0.8 Adc		V _{BE (sat)}	—	1.8	Vdc
Base-Emitter On Voltage (I _C = 8.0 Adc, V _{CE} = 2.0 Vdc)		V _{BE (on)}	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I _C = 1.0 Adc, V _{CE} = 20 Vdc, f _{test} = 0.5 MHz)		f _T	1.0	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle > 2.0%.

(2) f_T = |h_{FE}| • f_{test}.

3

FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_{J(pk)} = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided T_{J(pk)} < 200°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

PNP DEVICES
BD316 and BD318

NPN DEVICES
BD315 and BD317

FIGURE 3 — DC CURRENT GAIN

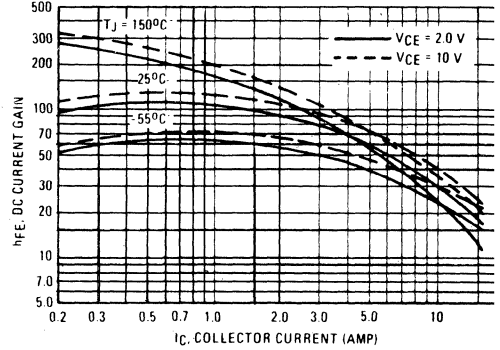
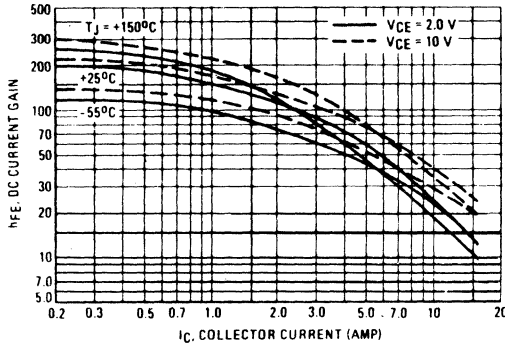
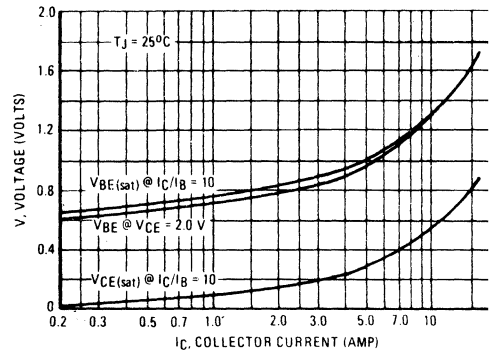
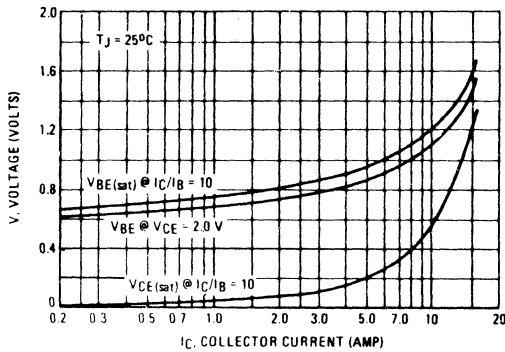


FIGURE 4 — "ON" VOLTAGES



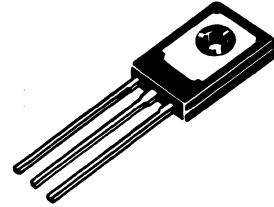
MOTOROLA
SEMICONDUCTOR
 TECHNICAL DATA

BD433, BD435
BD437, BD439
BD441

PLASTIC MEDIUM POWER SILICON
NPN TRANSISTOR

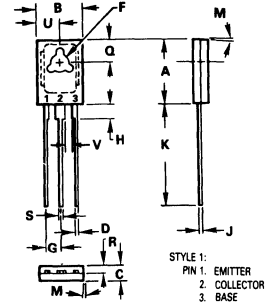
... for amplifier and switching applications Complementary types: BD434/436/438/440/442

4 AMPERE
POWER TRANSISTOR
NPN SILICON



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector Emitter Voltage	V_{CEO}	BD433 BD435 BD437 BD439 BD441	22 32 45 60 80	V _{dc}
Collector Base Voltage	V_{CBO}	BD433 BD435 BD437 BD439 BD441	22 32 45 60 80	V _{dc}
Emitter Base Voltage	V_{EBO}		5	V _{dc}
Collector current	I_C		4	A _{dc}
Base Current	I_B		1	A _{dc}
Total Device Dissipation $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D		36 288	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature range.	I_J, I_{stg}		-55 to +150	$^\circ\text{C}$



NOTES:
 1. MT = MAIN TERMINAL
 2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010)
 DIA TO DIM A & B AT MAXIMUM MATERIAL
 CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	2 TYP		2 TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-126

THERMAL CHARACTERISTICS

	Symbol	Max.	Unit
Thermal Resistance Junction to Case	θ_{JC}	3.5	$^\circ\text{C}/\text{W}$

BD433, BD435, BD437, BD439, BD441

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Collector Emitter Breakdown Voltage (I _C = 100 mA, I _B = 0)	BD433 BD435 BD437 BD439 BD441	BV _{CEO}	22 32 45 60 80		V _{dc}
Collector Base Breakdown Voltage (I _C = 100 μA, I _B = 0)	BD433 BD435 BD437 BD439 BD441	BV _{CBO}	22 32 45 60 80		V _{dc}
Emitter Base Breakdown Voltage (I _E = 100 μA, I _C = 0)		BV _{EBO}	5		V _{dc}
Collector Cutoff Current (V _{CB} = 22 V, I _E = 0) (V _{CB} = 32 V, I _E = 0) (V _{CB} = 45 V, I _E = 0) (V _{CB} = 60 V, I _E = 0) (V _{CB} = 80 V, I _E = 0)	BD433 BD435 BD437 BD439 BD441	I _{CBO}		0.1 0.1 0.1 0.1 0.1	mA _{dc}
Emitter Cutoff Current (V _{EB} = 5 V)		I _{EBO}		1	mA _{dc}
DC Current Gain (I _C = 10 mA, V _{CE} = 5 V)	BD433 BD435 BD437 BD439 BD441	H _{FE}	40 40 30 20 15		
DC Current Gain (I _C = 500 mA, V _{CE} = 1 V)	BD433 BD435 BD437 BD439 BD441	H _{FE}	85 85 85 40 40	475 475 375 475 475	
DC Current Gain (I _C = 2 A, V _{CE} = 1 V)	BD433 BD435 BD437 BD439 BD441	H _{FE}	50 50 40 25 15		
Collector Saturation Voltage (I _C = 2 A, I _B = 0.2 A) (I _C = 3 A, I _B = 0.3 A)	BD433 BD435 BD437 BD439 BD441	V _{CE (sat)}		0.5 0.5 0.7 0.8 0.8	V _{dc}
Base-Emitter on voltage (I _C = 2 A, V _{CE} = 1 V)	BD433/435/437 BD439/441	V _{BE(ON)}		1.1 1.5	V _{dc}
Current Gain Bandwidth Product (V _{CE} = 1 V, I _C = 250 mA, f = 1 MHz)		f _T	3		MHz

FIGURE 1 – COLLECTOR SATURATION REGION

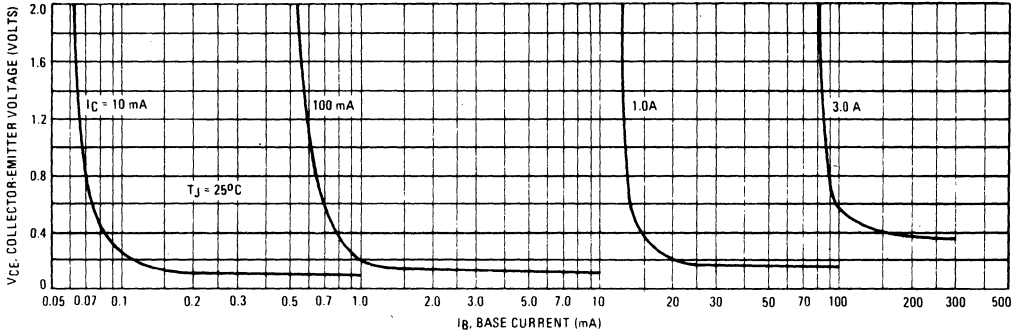


FIGURE 2 – CURRENT GAIN

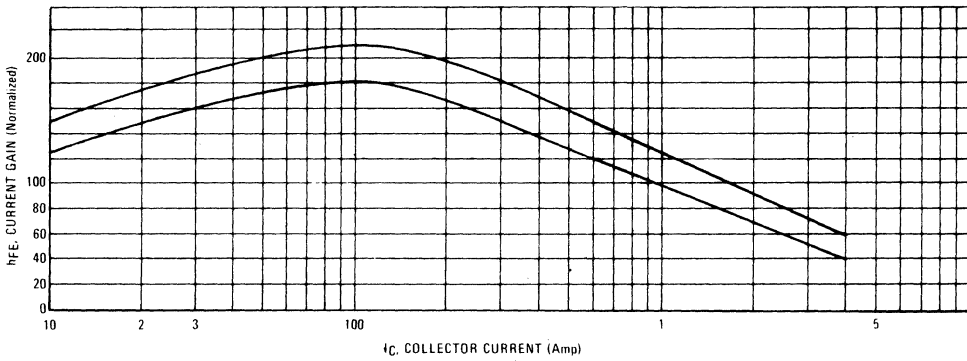


FIGURE 3 – "ON" VOLTAGE

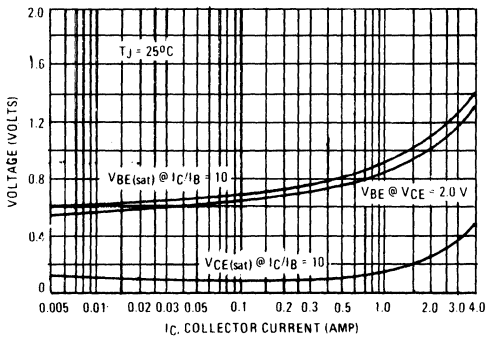
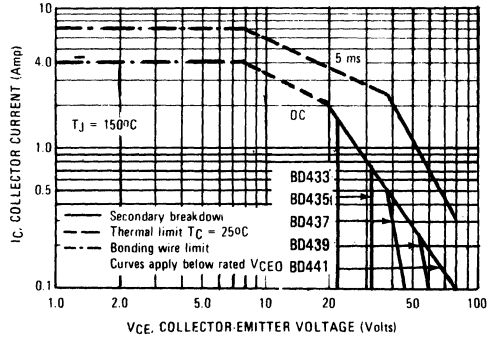


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



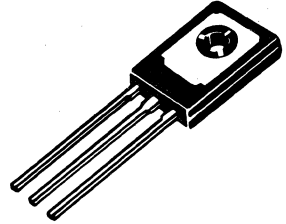
MOTOROLA
SEMICONDUCTOR
 TECHNICAL DATA

BD434, BD436
BD438, BD440
BD442

PLASTIC MEDIUM POWER SILICON
PNP TRANSISTOR

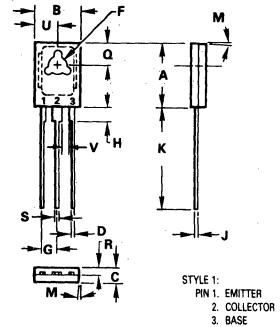
... for amplifier and switching applications Complementary types: BD433/435/437/439/441.

4 AMPERE
POWER TRANSISTOR
PNP SILICON



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector Emitter Voltage	V_{CEO}	BD434	22	Vdc
		BD436	32	
		BD438	45	
		BD440	60	
		BD442	80	
Collector Base Voltage	V_{CBO}	BD434	22	Vdc
		BD436	32	
		BD438	45	
		BD440	60	
		BD442	80	
Emitter Base Voltage	V_{EBO}		5	Vdc
Collector current	I_C		4	Adc
Base Current	I_B		1	Adc
Total Device Dissipation $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D		36	Watts mW/ $^\circ\text{C}$
			288	
Operating and Storage Junction Temperature range.	I_J, I_{stg}		-55 to +150	$^\circ\text{C}$



- NOTES:
 1. MT - MAIN TERMINAL.
 2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3" TYP		3" TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.89	3.93	0.145	0.155
V	1.02	-	0.040	-

CASE 77-05
TO-126

THERMAL CHARACTERISTICS

	Symbol	Max.	Unit
Thermal Resistance Junction to Case	θ_{JC}	3.5	$^\circ\text{C}/\text{W}$

BD434, BD436, BD438, BD440, BD442

ELECTRICAL CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Collector Emitter Breakdown Voltage ($I_C = 100\text{ mA}$, $I_B = 0$) BD434 BD436 BD438 BD440 BD442	BV_{CEO}	22 32 45 60 80			Vdc
Collector Base Breakdown Voltage ($I_C = 100\text{ }\mu\text{A}$, $I_B = 0$) BD434 BD436 BD438 BD440 BD442	BV_{CBO}	22 32 45 60 80			Vdc
Emitter Base Breakdown Voltage ($I_E = 100\text{ }\mu\text{A}$, $I_C = 0$)	BV_{EBO}	5			Vdc
Collector Cutoff Current ($V_{CB} = 22\text{ V}$, $I_E = 0$) ($V_{CB} = 32\text{ V}$, $I_E = 0$) ($V_{CB} = 45\text{ V}$, $I_E = 0$) ($V_{CB} = 60\text{ V}$, $I_E = 0$) ($V_{CB} = 80\text{ V}$, $I_E = 0$) BD434 BD436 BD438 BD440 BD442	CBO			0.1 0.1 0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}			1	mAdc
DC Current Gain ($I_C = 10\text{ mA}$, $V_{CE} = 5\text{ V}$) BD434 BD436 BD438 BD440 BD442	H_{FE}	40 40 30 20 15			
DC Current Gain ($I_C = 500\text{ mA}$, $V_{CE} = 1\text{ V}$) BD434 BD436 BD438 BD440 BD442	H_{FE}	85 85 85 40 40		475 475 375 475 475	
DC Current Gain ($I_C = 2\text{ A}$, $V_{CE} = 1\text{ V}$) BD434 BD436 BD438 BD440 BD442	H_{FE}	50 50 40 25 15			
Collector Saturation Voltage ($I_C = 2\text{ A}$, $I_B = 0.2\text{ A}$) BD434 BD436 BD438 BD440 BD442 ($I_C = 3\text{ A}$, $I_B = 0.3\text{ A}$)	$V_{CE(sat)}$			0.5 0.5 0.7 0.8 0.8	Vdc
Base-Emitter on voltage ($I_C = 2\text{ A}$, $V_{CE} = 1\text{ V}$) BD434/436/438 BD440/442	$V_{BE(ON)}$			1.1 1.5	Vdc
Current Gain Bandwidth Product ($V_{CE} = 1\text{ V}$, $I_C = 250\text{ mA}$, $f = 1\text{ MHz}$)	f_T	3			MHz

FIGURE 1 – COLLECTOR SATURATION REGION

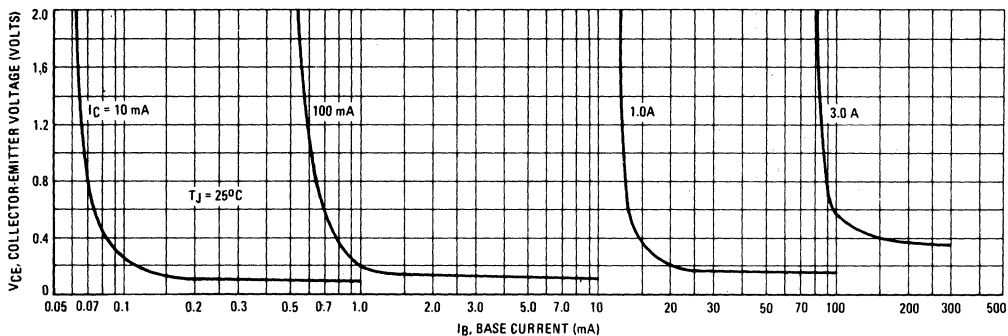


FIGURE 2 – CURRENT GAIN

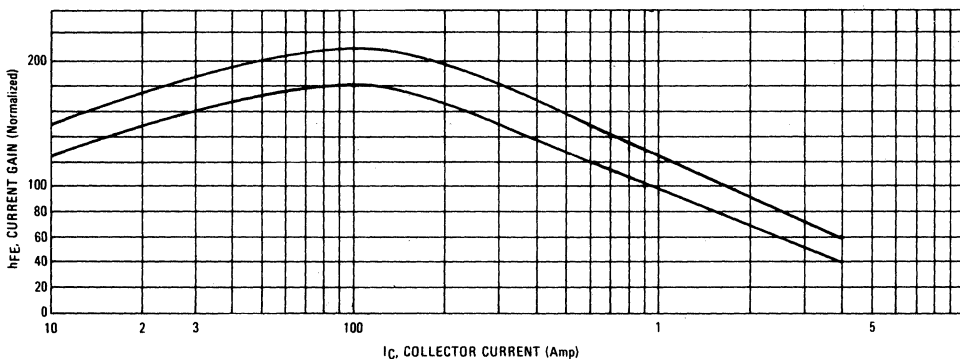


FIGURE 3 – "ON" VOLTAGE

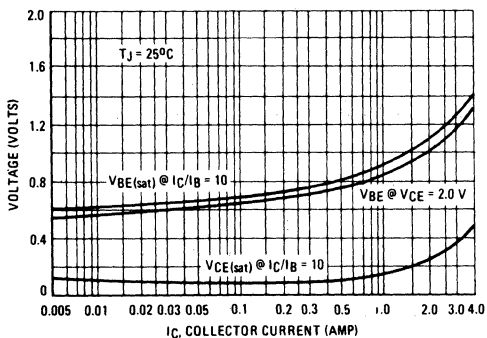
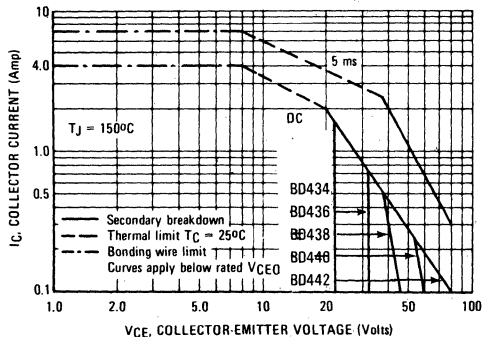


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



BD505
BD507
BD509

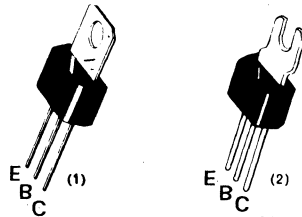
NPN SILICON ANNULAR TRANSISTORS

... designed for complementary symmetry audio circuits

- Excellent Current Gain Linearity — 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 0.7 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Adc}$
- Complements to PNP BD506, BD508, BD510
- Uniwatt[▲] Package for Excellent Thermal Properties —
 1.0 Watt @ $T_A = 25^\circ\text{C}$
 10.0 Watts @ $T_C = 25^\circ\text{C}$

NPN SILICON
AUDIO TRANSISTORS

20 - 30 - 40 VOLTS
 10 WATTS



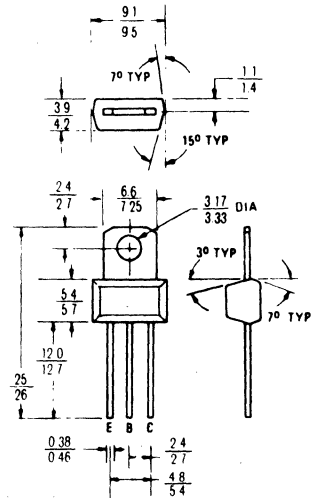
(1) Standard package: BD505, 507, 509
 (2) Tab formed for flat mounting: BD505-1, 507-1, 509-1
 Also available with leads formed to TO-5 configuration: BD505-5, 507-5, 509-5

MAXIMUM RATINGS

Rating	Symbol	BD505	BD507	BD509	Unit
Collector-Emitter Voltage	V_{CEO}	20	30	40	Vdc
Collector-Base Voltage	V_{CB}	30	40	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current - Continuous	I_C	2.0			Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0			Watt
		8.0			mW/°C
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10			Watts
		80			mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	125	°C/W



All dimensions in millimeters
 Collector connected
 to tab

CASE 152

BD505, BD507, BD509

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}$, $I_B = 0$)	BD505 BD507 BD509	BV _{CEO}	20	—	—	Vdc
			30	—	—	
			40	—	—	
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{Adc}$, $I_C = 0$)		5	—	—	Vdc	
Collector Cutoff Current (VCB = 20, 30, 40 Vdc, $I_E = 0$)	BD505 BD507 BD509	I _{CBO}	—	—	100	nAdc
			—	—	100	
			—	—	100	

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 250 \text{ mAdc}$, $V_{CE} = 2 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 2 \text{ Vdc}$)	h _{FE}	60	160	—	—
		40	90	—	
Collector-Emitter Saturation Voltage(1) ($I_C = 1.0 \text{ Adc}$, $I_B = 0.1 \text{ Adc}$)	V _{CE(sat)}	—	0.30	0.7	Vdc
Base-Emitter On Voltage (1) ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$)	V _{BE(on)}	—	0.91	1.2	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 50 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$, $f = 100 \text{ MHz}$)	f _T	50	250	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, $I_E = 0$, $f = 100 \text{ kHz}$)	C _{ob}	—	—	30	pF

(1) Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

FIGURE 1 — DC CURRENT GAIN

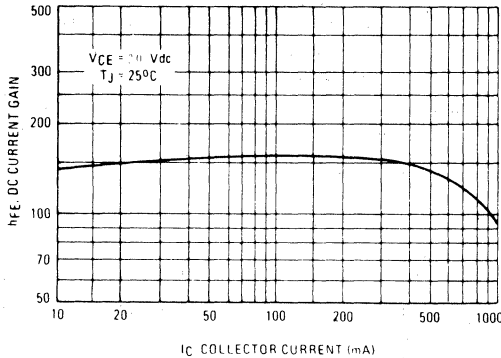


FIGURE 2 — "ON" VOLTAGES

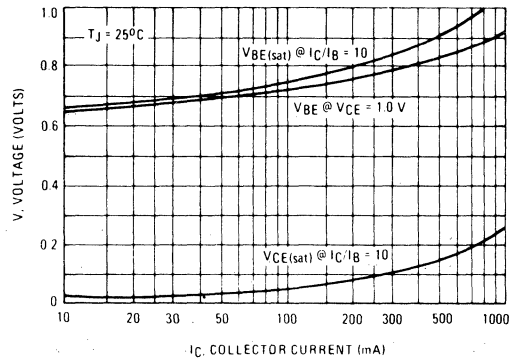
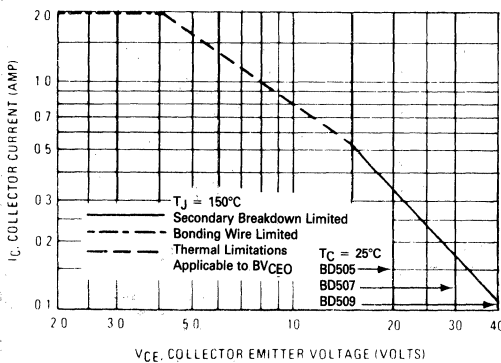


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

BD506
BD508
BD510

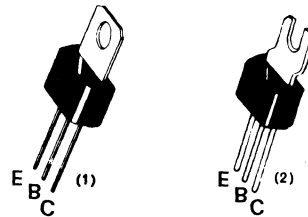
PNP SILICON
AUDIO TRANSISTORS

20 - 30 - 40 VOLTS
 10 WATTS

PNP SILICON ANNULAR[♦] TRANSISTORS

... designed for complementary symmetry audio circuits

- Excellent Current Gain Linearity — 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 0.7 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Adc}$
- Complements to NPN BD505, BD507, BD509
- Uniwatt[▲] Package for Excellent Thermal Properties —
 1.0 Watt @ $T_A = 25^\circ\text{C}$
 10.0 Watts @ $T_C = 25^\circ\text{C}$



(1) Standard package: BD506, 508, 510
 (2) Tab formed for flat mounting: BD506-1, 508-1, 510-1

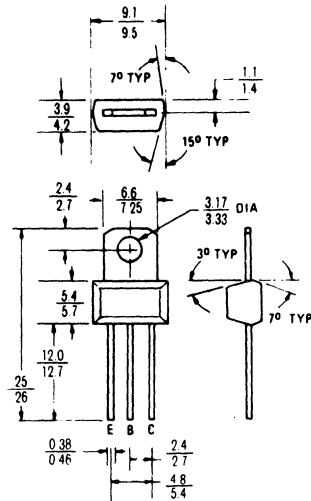
Also available with leads formed to TO-5 configuration: BD506-5, 508-5, 510-5

MAXIMUM RATINGS

Rating	Symbol	BD506	BD508	BD510	Unit
Collector-Emitter Voltage	V_{CEO}	20	30	40	Vdc
Collector-Base Voltage	V_{CB}	30	40	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current Continuous	I_C	2.0			Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0			Watt
		8.0			mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10			Watts
		80			mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	125	$^\circ\text{C/W}$



All dimensions in millimeters
 Collector connected
 to tab

CASE 152

BD506, BD508, BD510

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I _C = 1.0 mA, I _B = 0)	BD506 BD508 BD510	BV _{CEO}	20 30 40	— — —	Vdc
Emitter-Base Breakdown Voltage (I _E = 100 μA, I _C = 0)		BV _{EBO}	5.0	—	Vdc
Collector Cutoff Current (V _{CB} = 20, 30, 40 Vdc, I _E = 0)	BD506 BD508 BD510	I _{CBO}	— — —	— — —	nAdc

ON CHARACTERISTICS

DC Current Gain (1) (I _C = 250 mA, V _{CE} = 2.0 Vdc) (I _C = 1.0 A, V _{CE} = 2.0 Vdc)	h _{FE}	60 40	135 90	— —	—
Collector-Emitter Saturation Voltage(1) (I _C = 1.0 A, I _B = 0.1 A)	V _{CE(sat)}	—	0.40	0.7	Vdc
Base-Emitter On Voltage (1) (I _C = 1.0 A, V _{CE} = 1.0 Vdc)	V _{BE(on)}	—	0.92	1.2	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product (I _C = 50 mA, V _{CE} = 5.0 Vdc, f = 100 MHz)	f _T	50	180	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 100 kHz)	C _{ob}	—	—	30	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 1 — DC CURRENT GAIN

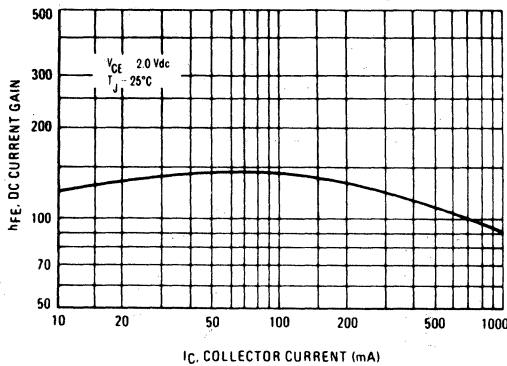


FIGURE 2 — "ON" VOLTAGES

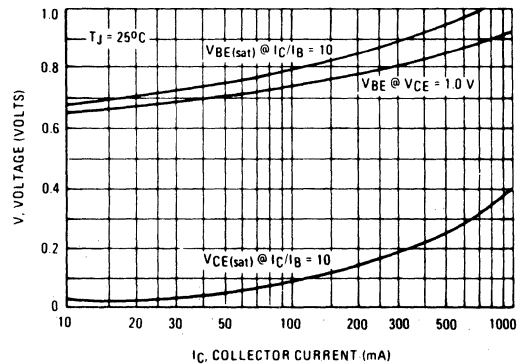
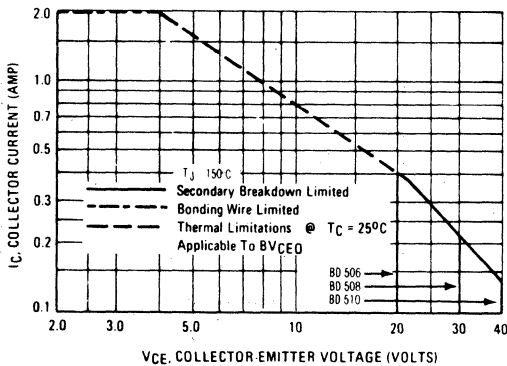


FIGURE 3 — DC SAFE OPERATING AREA



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The data of Figure 3 is based on T_J(pk) = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown

BD515
BD517
BD519

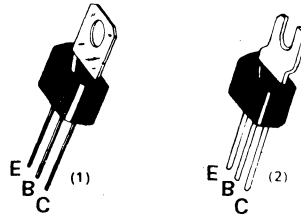
**NPN SILICON ANNULAR
AMPLIFIER TRANSISTORS**

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
 $V_{CE0} = 45 \text{ Vdc (Min) @ } I_C = 1 \text{ mAdc — BD515}$
 $60 \text{ Vdc (Min) @ } I_C = 1 \text{ mAdc — BD517}$
 $80 \text{ Vdc (Min) @ } I_C = 1 \text{ mAdc — BD519}$
- High Power Dissipation — $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$
- Complements to BD516, BD518, BD520

**NPN SILICON
AMPLIFIER TRANSISTORS**

45 - 60 - 80 VOLTS
10 WATTS



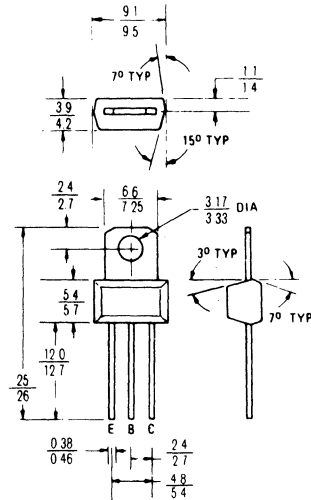
(1) Standard package: BD515, 517, 519
(2) Tab formed for flat mounting: BD515-1, 517-1, 519-1
Also available with leads formed to TO-5 configuration: BD515-5, 517-5, 519-5

MAXIMUM RATINGS

Rating	Symbol	BD515	BD517	BD519	Unit
Collector-Emitter Voltage	V_{CE0}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0			Vdc
Collector Current - Continuous	I_C	2.0			Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0			Watt mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10			Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	125	$^\circ\text{C/W}$



All dimensions in millimeters
Collector connected
to tab

CASE 152

BD515, BD517, BD519

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}$, $I_E = 0$)	BD515 BD517 BD519	BV_{CEO}	45 60 80	— — —	— — —	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{Adc}$, $I_C = 0$)		BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 30 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 40 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$)	BD515 BD517 BD519	I_{CBO}	— — —	— — —	100 100 100	nAdc
ON CHARACTERISTICS						
DC Current Gain (1) ($I_C = 10 \text{ mAdc}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 150 \text{ mAdc}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 2.0 \text{ Vdc}$)		h_{FE}	— 60 25	115 125 55	— 350 —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 500 \text{ mAdc}$, $I_B = 50 \text{ mAdc}$) ($I_C = 500 \text{ mAdc}$, $I_B = 25 \text{ mAdc}$)		$V_{CE(sat)}$	— —	0.18 0.24	0.5 —	Vdc
Base-Emitter On Voltage (1) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 2.0 \text{ Vdc}$)		$V_{BE(on)}$	—	0.74	1.0	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain-Bandwidth Product ($I_C = 200 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$, $f = 100 \text{ MHz}$)		f_T	50	160	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 100 \text{ kHz}$)		C_{ob}	—	6.0	12	pF

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$

FIGURE 1 — TYPICAL DC CURRENT GAIN

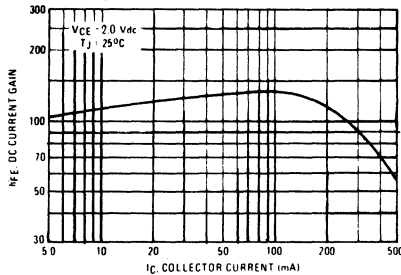


FIGURE 2 — "SATURATION" AND "ON" VOLTAGES

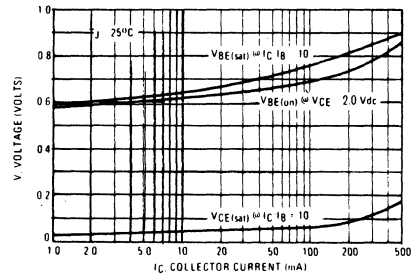


FIGURE 3 — DC SAFE OPERATING AREA

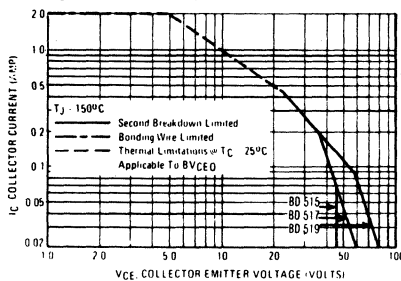
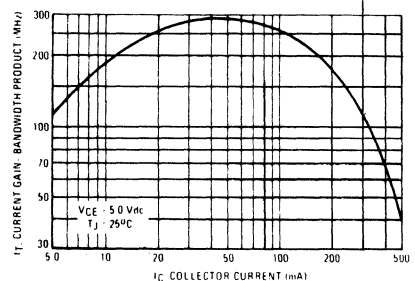


FIGURE 4 — CURRENT-GAIN — BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$. T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

BD516
BD518
BD520

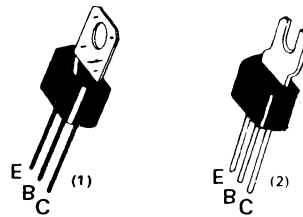
**PNP SILICON ANNULAR
 AMPLIFIER TRANSISTORS**

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
 $BV_{CEO} = 45 \text{ Vdc (Min) @ } I_C = 1 \text{ mAdc — BD516}$
 $60 \text{ Vdc (Min) @ } I_C = 1 \text{ mAdc — BD518}$
 $80 \text{ Vdc (Min) @ } I_C = 1 \text{ mAdc — BD520}$
- High Power Dissipation — $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$
- Complements to BD515, BD517, BD519

**PNP SILICON ANNULAR *
 AMPLIFIER TRANSISTORS**

45 - 60 - 80 VOLTS
 10 WATTS



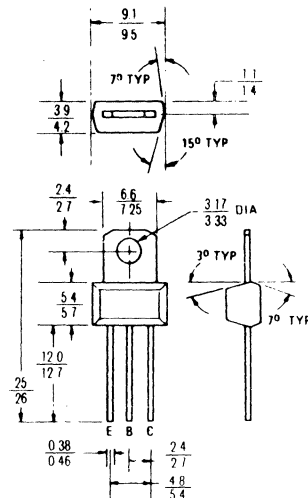
(1) Standard package: **BD516, 518, 520**
 (2) Tab formed for flat mounting: **BD516-1, 518-1, 520-1**
 Also available with leads formed to TO-5 configuration: **BD516-5, 518-5, 520-5**

MAXIMUM RATINGS

Rating	Symbol	BD516	BD518	BD520	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0			Vdc
Collector Current - Continuous	I_C	2.0			A dc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0			Watt
		8.0			mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10			Watts
		80			mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	125	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	125	$^\circ\text{C/W}$



All dimensions in millimeters
 Collector connected
 to tab

CASE 152

BD516, BD518, BD520

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}, I_B = 0$)	BD516 BD518 BD520	BV_{CEO}	45 60 80	— — —	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{Adc}, I_C = 0$)		BV_{EBO}	4.0	—	Vdc
Collector Cutoff Current ($V_{CB} = 30 \text{ Vdc}, I_E = 0$) ($V_{CB} = 40 \text{ Vdc}, I_E = 0$) ($V_{CB} = 60 \text{ Vdc}, I_E = 0$)	BD516 BD518 BD520	I_{CBO}	— — —	— — —	nAdc

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 10 \text{ mAdc}, V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 150 \text{ mAdc}, V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}, V_{CE} = 2.0 \text{ Vdc}$)		h_{FE}	— 60 25	150 130 80	— 350 —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 500 \text{ mAdc}, I_B = 50 \text{ mAdc}$) ($I_C = 500 \text{ mAdc}, I_B = 25 \text{ mAdc}$)		$V_{CE(sat)}$	— —	0.24 0.32	0.5 —	Vdc
Base-Emitter On Voltage (1) ($I_C = 500 \text{ mAdc}, V_{CE} = 2.0 \text{ Vdc}$)		$V_{BE(on)}$	—	0.78	1.0	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 200 \text{ mAdc}, V_{CE} = 5.0 \text{ Vdc}, f = 100 \text{ MHz}$)		f_T	50	125	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 100 \text{ kHz}$)		C_{ob}	—	10	15	pF

(1) Pulse Test Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 1 — DC CURRENT GAIN

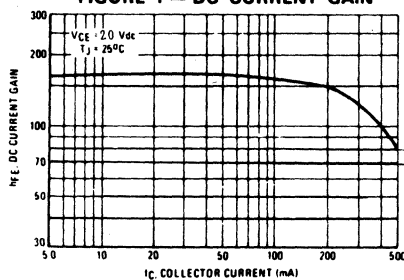


FIGURE 2 — "ON" VOLTAGES

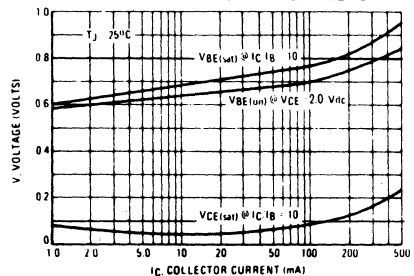


FIGURE 3 — DC SAFE OPERATING AREA

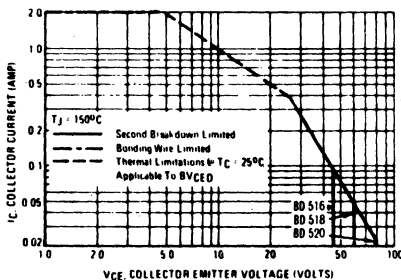
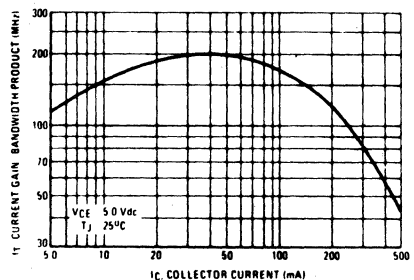


FIGURE 4 — CURRENT-GAIN-BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_J(pk) = 150^\circ\text{C}$. T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

BD525
BD527
BD529

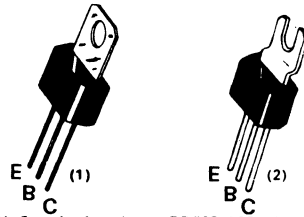
**NPN SILICON ANNULAR
 AMPLIFIER TRANSISTORS**

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
 $V_{CEO} = 60 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc — BD525}$
 $80 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc — BD527}$
 $100 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc — BD529}$
- High Power Dissipation — $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$
- Complements to PNP BD526, BD528, BD530

**NPN SILICON
 AMPLIFIER TRANSISTORS**

60 - 80 - 100 VOLTS
 10 WATTS



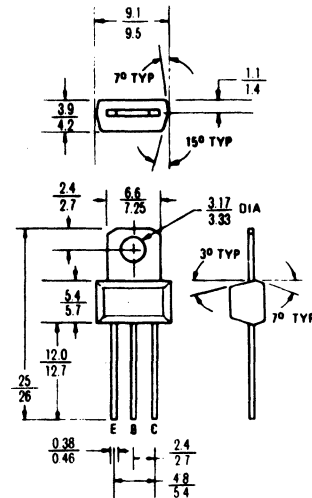
(1) Standard package: BD525, 527, 529
 (2) Tab formed for flat mounting: BD525-1, 527-1, 529-1
 Also available with leads formed to TO-5 configuration: BD525-5, 527-5, 529-5

MAXIMUM RATINGS

Rating	Symbol	BD525	BD527	BD529	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	4.0			Vdc
Collector Current - Continuous	I_C	2.0			Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0			Watt mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80			Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	125	$^\circ\text{C/W}$



All dimensions in millimeters
 Collector connected
 to tab

CASE 152

BD525, BD527, BD529

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I _C = 1.0 mA, I _B = 0)	BD525 BD527 BD529	BV _{CEO}	60 80 100	— — —	— — —	Vdc
Emitter-Base Breakdown Voltage (I _E = 100 μA, I _C = 0)		BV _{EBO}	4.0	—	—	Vdc
Collector Cutoff Current (V _{CB} = 40 Vdc, I _E = 0) (V _{CB} = 60 Vdc, I _E = 0) (V _{CB} = 80 Vdc, I _E = 0)	BD525 BD527 BD529	I _{CBO}	— — —	— — —	100 100 100	nA

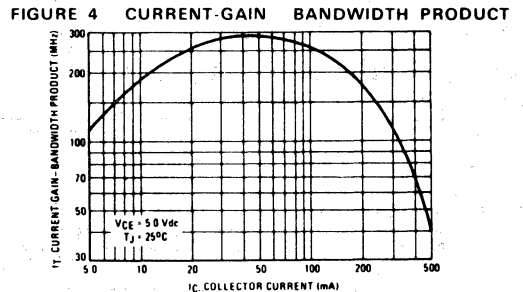
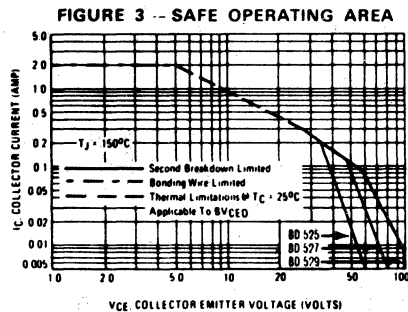
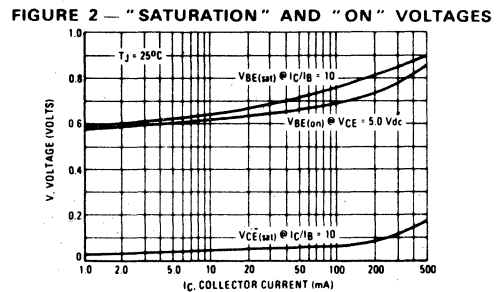
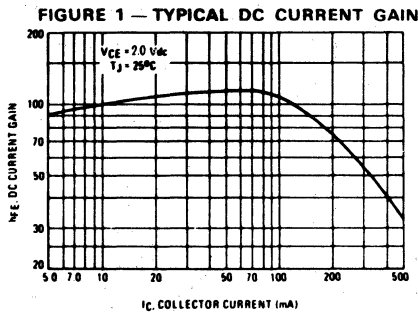
ON CHARACTERISTICS

DC Current Gain (1) (I _C = 50 mA, V _{CE} = 2.0 Vdc) (I _C = 250 mA, V _{CE} = 2.0 Vdc)		h _{FE}	60 30	115 95	— —	—
Collector-Emitter Saturation Voltage(1) (I _C = 250 mA, I _B = 10 mA) (I _C = 250 mA, I _B = 25 mA)		V _{CE(sat)}	— —	0.18 0.1	0.5 —	Vdc
Base-Emitter On Voltage (1) (I _C = 250 mA, V _{CE} = 5.0 Vdc)		V _{BE(on)}	—	0.74	1.0	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product (I _C = 250 mA, V _{CE} = 5.0 Vdc, f = 100 MHz)		f _T	50	150	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 100 kHz)		C _{ob}	—	6.0	12	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on T_{J(pk)} = 150°C. T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

BD526
BD528
BD530

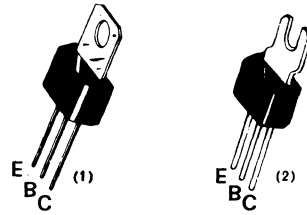
**PNP SILICON ANNULAR
AMPLIFIER TRANSISTORS**

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
 $BV_{CEO} = 60 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc — BD526}$
 $80 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc — BD528}$
 $100 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc — BD530}$
- High Power Dissipation — $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$
- Complements to NPN BD525, BD527, BD529

**PNP SILICON
AMPLIFIER TRANSISTORS**

60 - 80 - 100 VOLTS
10 WATTS



(1) Standard package: BD526, 528, 530
(2) Tab formed for flat mounting: BD526-1, 528-1, 530-1

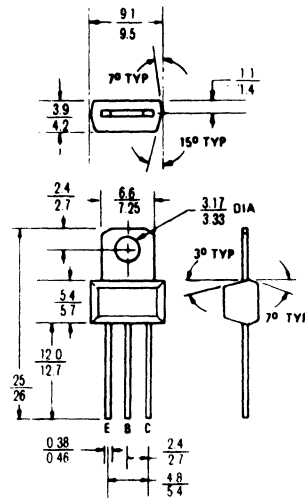
Also available with leads formed to TO-5 configuration: BD526-5, 528-5, 530-5

MAXIMUM RATINGS

Rating	Symbol	BD526	BD528	BD530	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	—	4.0	—	Vdc
Collector Current - Continuous	I_C	—	2.0	—	Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	—	1.0	—	Watt mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	—	10	—	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			$^\circ\text{C}$

HERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	125	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	125	$^\circ\text{C/W}$



All dimensions in millimeters
Collector connected to tab

CASE 152

BD526, BD528, BD530

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mA}$, $I_B = 0$)	BD526 BD528 BD530	BV_{CEO}	60 80 100	— — —	— — —	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{A}$, $I_C = 0$)		BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$)	BD526 BD528 BD530	I_{CBO}	— — —	— — —	100 100 100	nAdc

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 50 \text{ mA}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 250 \text{ mA}$, $V_{CE} = 2.0 \text{ Vdc}$)	h_{FE}	60 30	153 98	— —	—
Collector-Emitter Saturation Voltage(1) ($I_C = 250 \text{ mA}$, $I_B = 10 \text{ mA}$) ($I_C = 250 \text{ mA}$, $I_B = 25 \text{ mA}$)	$V_{CE(sat)}$	— —	0.22 0.15	0.5 —	Vdc
Base-Emitter On Voltage (1) ($I_C = 250 \text{ mA}$, $V_{CE} = 5.0 \text{ Vdc}$)	$V_{BE(on)}$	—	0.78	1.0	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 200 \text{ mA}$, $V_{CE} = 5.0 \text{ Vdc}$, $f = 100 \text{ MHz}$)	f_T	50	100	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 100 \text{ kHz}$)	C_{ob}	—	10	15	pF

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$

FIGURE 1 — DC CURRENT GAIN

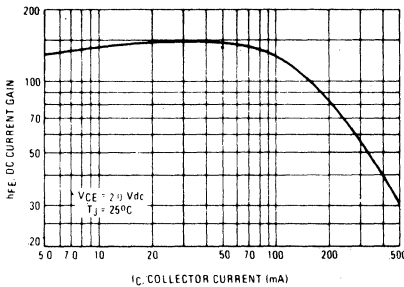


FIGURE 2 — "ON" VOLTAGES

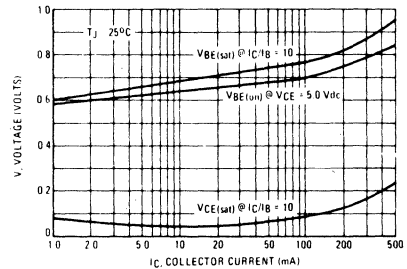


FIGURE 3 — DC SAFE OPERATING AREA

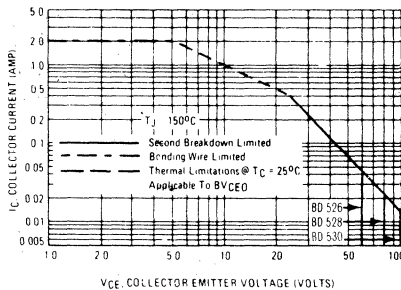
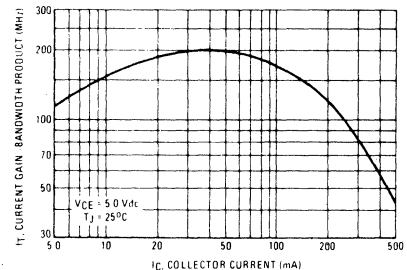


FIGURE 4 — CURRENT-GAIN-BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_J(pk) = 150^\circ\text{C}$. T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

... designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage –
 $V_{CE} = 0.8 \text{ Vdc (Max) @ } I_C = 2.0 \text{ Adc}$
- Collector-Emitter Sustaining Voltage –
 $V_{CEO} \text{ (sus)} = 45 \text{ Vdc (Min) BD533, BD534}$
 $= 60 \text{ Vdc (Min) BD535, BD536}$
 $= 80 \text{ Vdc (Min) BD537, BD538}$
- High Current Gain – Bandwidth Product
 $f_T = 3.0 \text{ MHz (Min) @ } I_C = 250 \text{ mA}$
- Compact TO-220 AB Package
- TO-66 Leadform Also Available ordered with “-66” suffix

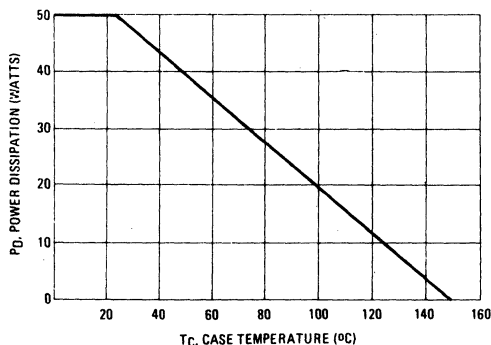
MAXIMUM RATINGS

Rating	Symbol	BD533 BD534	BD535 BD536	BD537 BD538	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current - Continuous	I_C	← 4.0 →			Adc
Peak		← 8.0 →			
Base Current	I_B	← 1.0 →			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 50 →			Watts
		← 0.4 →			
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	$^\circ\text{C/W}$

FIGURE 1 —POWER DERATING

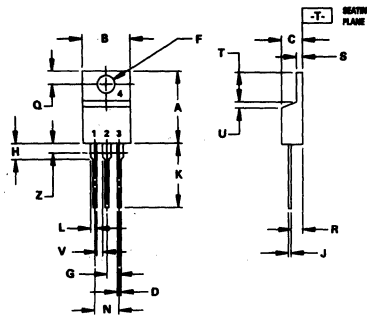
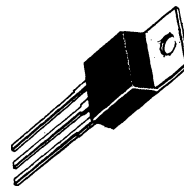


NPN
BD533
BD535
BD537

PNP
BD534
BD536
BD538

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON

45, 60, 80 VOLTS
50 WATTS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.89	10.28	0.390	0.405
C	4.67	4.92	0.180	0.190
D	0.64	0.88	0.025	0.035
F	3.81	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.82	0.110	0.150
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.87	6.47	0.230	0.255
U	0.90	1.27	0.030	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:
PIN 1: BASE
2: COLLECTOR
3: EMITTER
4: COLLECTOR

CASE 221A-04
TO-220AB

BD533, BD535, BD537 NPN
BD534, BD536, BD538 PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ¹ ($I_C = 0.1\text{ Adc}, I_B = 0$)	BD533, BD534 BD535, BD536 BD537, BD538	$V_{CEO(sus)}$	45 60 80	Vdc
Collector Cutoff Current ($V_{CB} = 45\text{ Vdc}, I_E = 0$) ($V_{CB} = 60\text{ Vdc}, I_E = 0$) ($V_{CB} = 80\text{ Vdc}, I_E = 0$)	BD533, BD534 BD535, BD536 BD537, BD538	I_{CBO}	0.1 0.1 0.1	mAdc
Collector Cutoff Current ($V_{CE} = 45\text{ Vdc}, V_{EB} = 0$) ($V_{CE} = 60\text{ Vdc}, V_{EB} = 0$) ($V_{CE} = 80\text{ Vdc}, V_{EB} = 0$)	BD533, BD534 BD535, BD536 BD537, BD538	I_{CES}	100 100 100	μAdc
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}, I_C = 0$)		I_{EBO}	1.0	mAdc
ON CHARACTERISTICS¹				
DC Current Gain ($I_C = 10\text{ mAdc}, V_{CE} = 5\text{ Vdc}$)	BD533, BD534 BD535, BD536 BD537, BD538	h_{FE}	20 20 15	
($I_C = 500\text{ mAdc}, V_{CE} = 2\text{ Vdc}$)			40	
($I_C = 2\text{ Adc}, V_{CE} = 2\text{ Vdc}$)	BD533, BD534 BD535, BD536 BD537, BD538		25 25 15	
Collector-Emitter Saturation Voltage ($I_C = 2.0\text{ Adc}, I_B = 0.2\text{ Adc}$)		$V_{CE(sat)}$	0.8	Vdc
Base-Emitter On Voltage ($I_C = 2.0\text{ Adc}, V_{CE} = 2.0\text{ Vdc}$)		$V_{BE(on)}$	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain - Bandwidth Product ² ($I_C = 250\text{ mAdc}, V_{CE} = 1\text{ Vdc}, f_{test} = 1\text{ MHz}$)		f_T	3.0	MHz

¹ Pulse test = Pulse width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

² $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 - SWITCHING TIME EQUIVALENT CIRCUIT

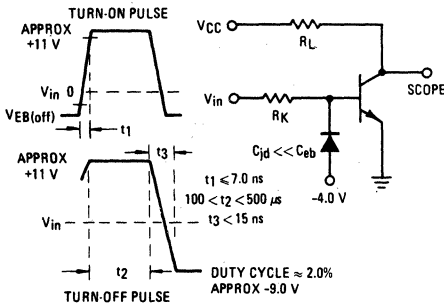
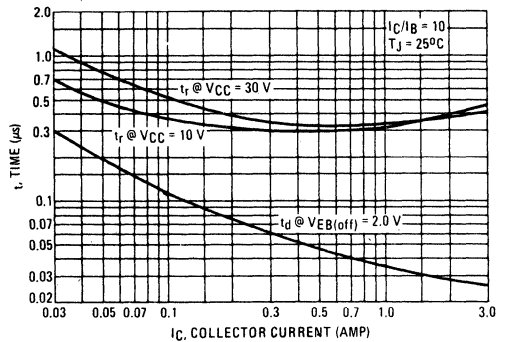


FIGURE 3 - TURN-ON TIME



BD533, BD535, BD537 NPN
BD534, BD536, BD538 PNP

FIGURE 4 – THERMAL RESPONSE

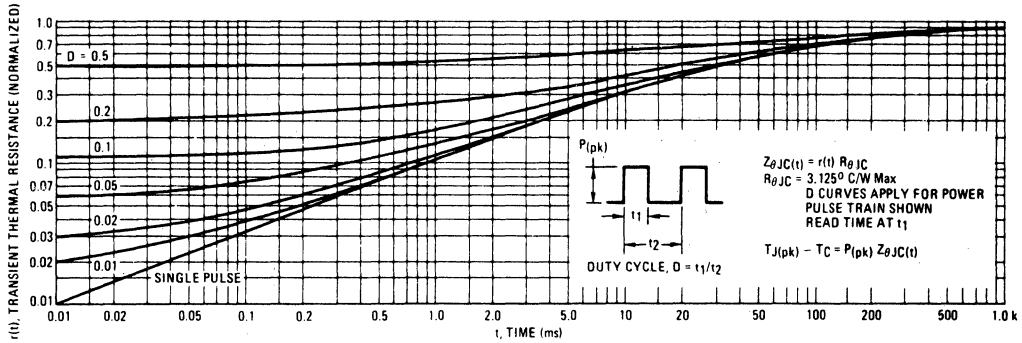
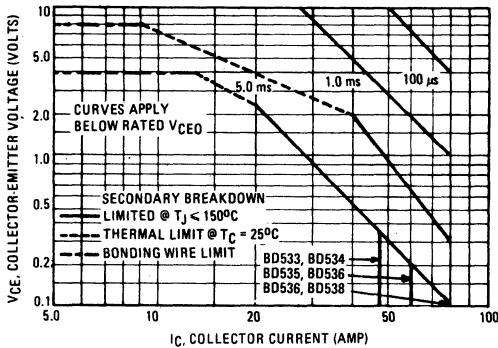


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{j(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{j(pk)} \leq 150^{\circ}\text{C}$. $T_{j(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A).

FIGURE 6 – TURN-OFF TIME

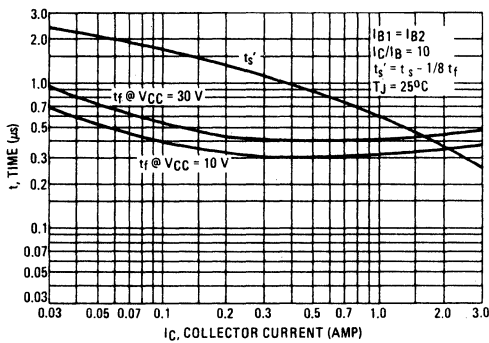
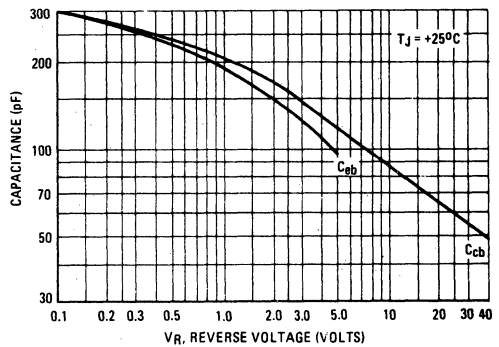


FIGURE 7 – CAPACITANCE



BD533, BD535, BD537 NPN
BD534, BD536, BD538 PNP

FIGURE 8 – DC CURRENT GAIN

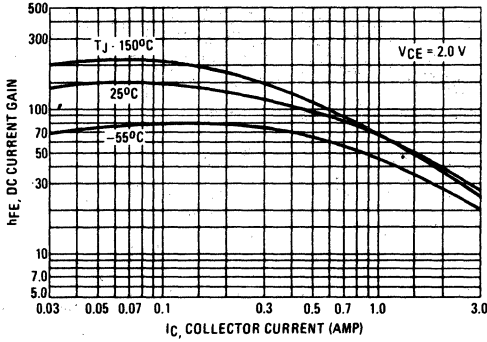


FIGURE 9 – COLLECTOR SATURATION REGION

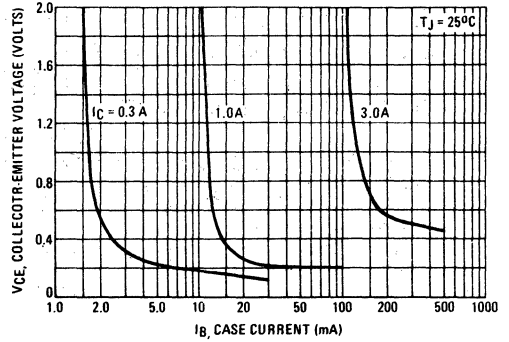


FIGURE 10 – "ON" VOLTAGES

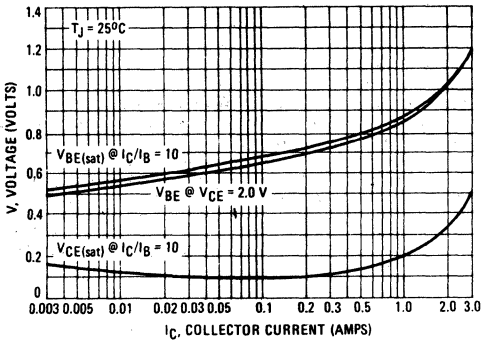


FIGURE 11 – TEMPERATURE COEFFICIENTS

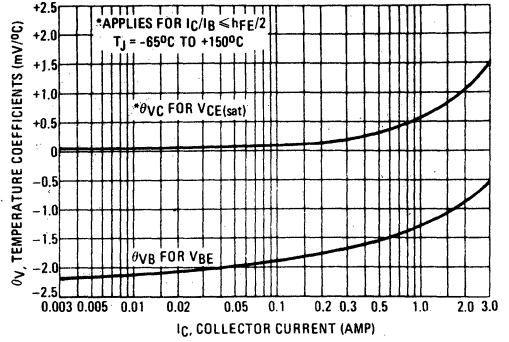


FIGURE 12 – COLLECTOR CUT-OFF REGION

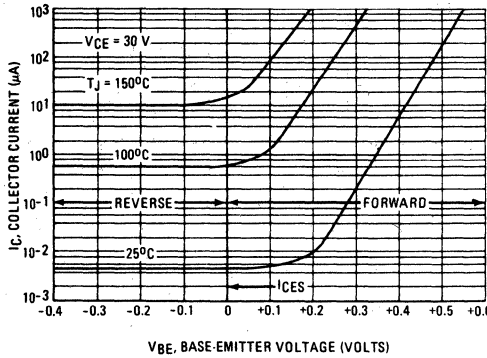
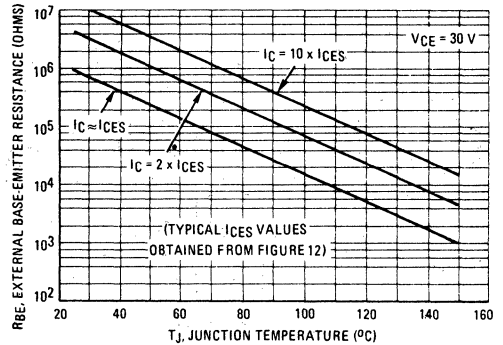


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



3

BD675, BD675A
BD677, BD677A
BD679, BD679A
BD681

PLASTIC MEDIUM-POWER
SILICON NPN DARLINGTONS

... for use as output devices in complementary general-purpose amplifier applications.

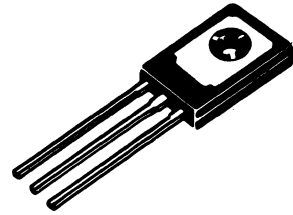
- High DC Current Gain –
 $h_{FE} = 750$ (Min) @ $I_C = 1.5$ and 2.0 Adc
- Monolithic Construction
- BD675, 675A, 677, 677A, 679, 679A, 681 are complementary with BD676, 676A, 678, 678A, 680, 680A, 682
- BD 677, 677A, 679, 679A are equivalent to MJE 800, 801, 802, 803

4.0 AMPERE
DARLINGTON
POWER TRANSISTORS
NPN SILICON

45, 60, 80, 100 VOLTS
40 WATTS

MAXIMUM RATINGS

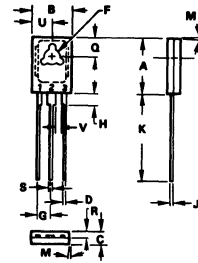
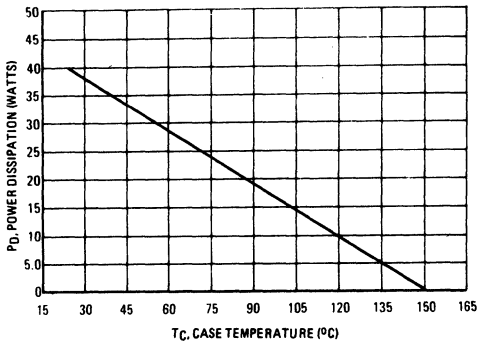
Rating	Symbol	BD675 BD675A	BD677 BD677A	BD679 BD679A	BD681	Unit
Collector-Emitter Voltage	V_{CE0}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	4.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40				Watts
Operating and Storage Junction Temperating Range	T_J, T_{stg}	-55 to +150				$^\circ\text{C}$



THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.13	$^\circ\text{C}/\text{W}$

FIGURE 1 – POWER TEMPERATURE DERATING



MILLIMETERS		INCHES		
MIN	MAX	MIN	MAX	
A	10.80	11.00	0.425	0.430
B	7.80	7.74	0.295	0.290
C	2.62	2.95	0.102	0.115
D	0.51	0.69	0.020	0.028
E	2.80	2.17	0.110	0.085
G	2.52	2.46	0.101	0.097
H	1.27	2.41	0.050	0.095
J	0.28	0.02	0.011	0.005
K	14.61	16.02	0.575	0.630
M	TYP		TYP	
Q	3.75	4.02	0.148	0.158
R	1.15	1.28	0.045	0.050
S	0.64	0.68	0.025	0.026
U	3.89	3.92	0.153	0.154
V	1.02	—	0.040	—

STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. BASE

NOTES:
 1. WET MAIN TERMINAL.
 2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

BD675, 675A, BD677, 677A, BD679, 679A, BD681

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) ($I_C = 50 \text{ mAdc}, I_B = 0$)	BD675, 675A BD677, 677A BD679, 679A BD681	BV_{CEO}	45 60 80 100	— — — —	Vdc
Collector Cutoff Current ($V_{CE} = \text{Half Rated } BV_{CEO}, I_B = 0$)		I_{CEO}	—	500	μAdc
Collector Cutoff Current ($V_{CB} = \text{Rated } BV_{CEO}, I_E = 0$) ($V_{CB} = \text{Rated } BV_{CEO}, I_E = 0, T_C = 100^\circ\text{C}$)		I_{CBO}	— —	0.2 2.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)		I_{EBO}	—	2.0	mAdc

ON CHARACTERISTICS

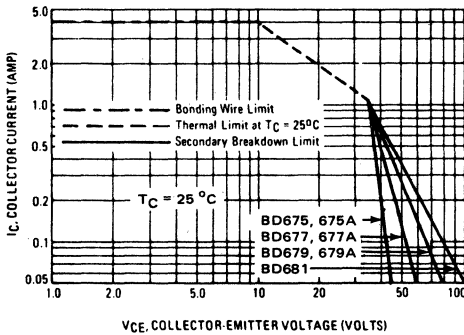
DC Current Gain(1) ($I_C = 1.5 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 2.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}$)	BD675, 677, 679, 681 BD 675A, 677A, 679A	h_{FE}	750 750	— —	—
Collector-Emitter Saturation Voltage(1) ($I_C = 1.5 \text{ Adc}, I_B = 30 \text{ mAdc}$) ($I_C = 2.0 \text{ Adc}, I_B = 40 \text{ mAdc}$)	BD 677, 679, 681 BD 675A, 677A, 679A	$V_{CE(sat)}$	— —	2.5 2.8	Vdc
Base-Emitter On Voltage(1) ($I_C = 1.5 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 2.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}$)	BD 677, 679, 681 BD 675A, 677A, 679A	$V_{BE(on)}$	— —	2.5 2.5	Vdc

DYNAMIC CHARACTERISTICS

Small-Signal Current Gain ($I_C = 1.5 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}, f = 1.0 \text{ MHz}$)	h_{fe}	1.0	—	—
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(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 - DC SAFE OPERATING AREA

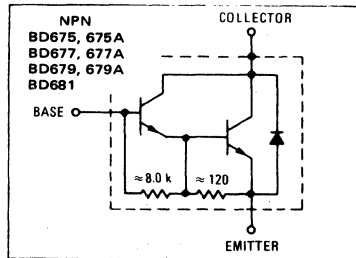


There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

V_{CE} , COLLECTOR-EMITTER VOLTAGE (VOLTS)

FIGURE 3 DARLINGTON CIRCUIT SCHEMATIC



BD676, BD676A
BD678, BD678A
BD680, BD680A
BD682

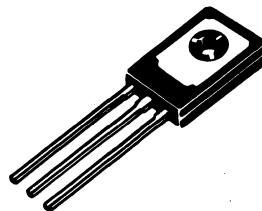
PLASTIC MEDIUM-POWER SILICON PNP DARLINGTONS

... for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain – $h_{FE} = 750$ (Min) @ $I_C = 1.5$ and 2.0 Adc
- Monolithic Construction
- BD676, 676A, 678, 678A, 680, 680A, 682 are complementary with BD675, 675A, 677, 677A, 679, 679A, 681
- BD 678, 678A, 680, 680A are equivalent to MJE 700, 701, 702, 703

4.0 AMPERE DARLINGTON POWER TRANSISTORS PNP SILICON

45, 60, 80, 100 VOLTS
40 WATTS



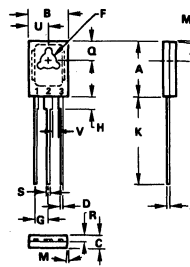
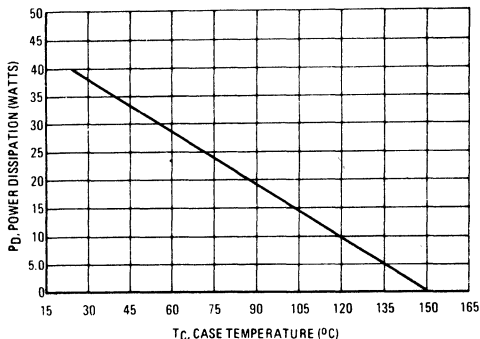
MAXIMUM RATING

Rating	Symbol	BD676 BD676A	BD678 BD678A	BD680 BD680A	BD682	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	4.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40				Watts
Operating and Storage Junction Temperating Range	T_J, T_{stg}	-55 to +150				$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.13	$^\circ\text{C}/\text{W}$

FIGURE 1 – POWER TEMPERATURE DERATING



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.50	11.50	0.413	0.453
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.52	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.49	0.63	0.019	0.025
K	14.47	16.62	0.570	0.655
M	TYP		TYP	
Q	3.76	4.07	0.148	0.159
R	1.15	1.20	0.045	0.047
S	0.64	0.60	0.025	0.024
V	3.68	3.93	0.145	0.155
W	1.02	—	0.040	—

STYLE 1:
 PN 1. EMITTER
 2. COLLECTOR
 3. BASE

NOTES:
 1. MT – MAIN TERMINAL.
 2. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05
TO-126

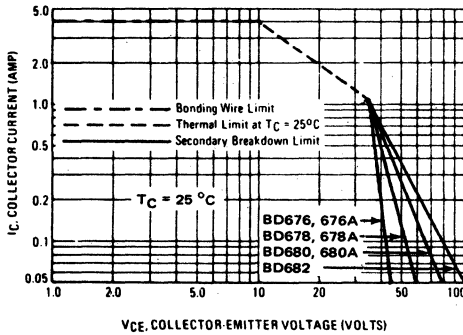
BD676, 676A, BD678, 678A, BD680, 680A, BD682

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) ($I_C = 50 \text{ mAdc}, I_B = 0$)	BD676, 676A BD678, 678A BD680, 680A BD682	BV_{CEO}	45 60 80 100	— — — —	Vdc
Collector Cutoff Current ($V_{CE} = \text{Half Rated } BV_{CEO}, I_B = 0$)		I_{CEO}	—	500	μAdc
Collector Cutoff Current ($V_{CB} = \text{Rated } BV_{CEO}, I_E = 0$) ($V_{CB} = \text{Rated } BV_{CEO}, I_E = 0, T_C = 100^\circ\text{C}$)		I_{CBO}	— —	0.2 2.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1) ($I_C = 1.5 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 2.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}$)	BD676, 678, 680, 682 BD 676A, 678A, 680A	h_{FE}	750 750	— —	—
Collector-Emitter Saturation Voltage(1) ($I_C = 1.5 \text{ Adc}, I_B = 30 \text{ mAdc}$) ($I_C = 2.0 \text{ Adc}, I_B = 40 \text{ mAdc}$)	BD 678, 680, 682 BD 676A, 678A, 680A	$V_{CE(sat)}$	— —	2.5 2.8	Vdc
Base-Emitter On Voltage(1) ($I_C = 1.5 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 2.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}$)	BD 678, 680, 682 BD 676A, 678A, 680A	$V_{BE(on)}$	— —	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 1.5 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}, f = 1.0 \text{ MHz}$)		h_{fe}	1.0	—	—

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

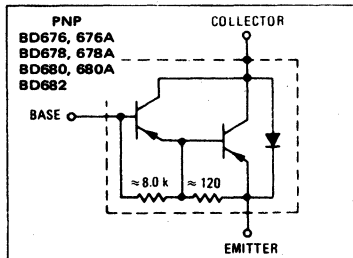
FIGURE 2 - DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 - DARLINGTON CIRCUIT SCHEMATIC

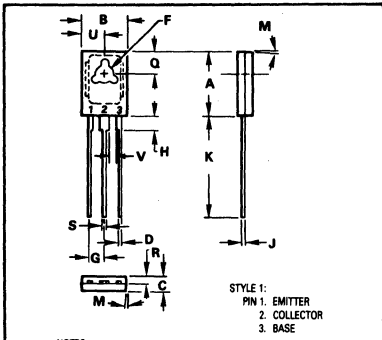
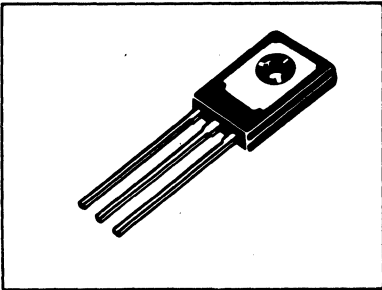


NPN	PNP
BD775	BD776
BD777	BD778
BD779	BD780

PLASTIC DARLINGTON COMPLEMENTARY SILICON ANNULAR POWER TRANSISTORS
 . . . designed for general purpose amplifier and high-speed switching applications such as hammer drivers for desk calculators.

- High DC Current Gain
 $h_{FE} = 1400$ (Typ) @ $I_C = 2.0$ Adc
- Collector-Emitter Sustaining Voltage – @ 10 mAdc
 V_{CEO} (sus) = 45 Vdc (Min) – BD775, 776
 = 60 Vdc (Min) – BD777, 778
 = 80 Vdc (Min) – BD779, 780
- Reverse Voltage Protection Diode
- Monolithic Construction with Built-in Base-Emitter output Resistor
- Thermopad II^Δ Construction with Hard Solder for High Reliability.

DARLINGTON 4-AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS
 45, 60, 80 VOLTS
 15 WATTS

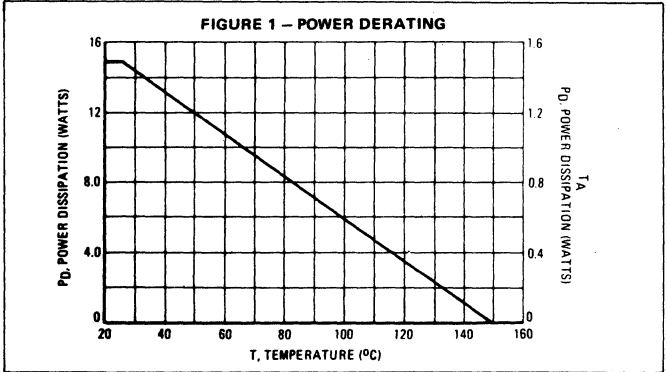


MAXIMUM RATINGS

Rating	Symbol	BD775 BD776	BD777 BD778	BD779 BD780	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}		5.0		Vdc
Collector Current – Continuous Peak	I_C		4.0 6.0		Adc
Base Current	I_B		100		mAdc
Total Device Dissipation $T_C = 25^\circ\text{C}$ – Derate above 25°C	P_D		15 0.12		Watts W/°C
Operating and Storage junction Temperature Range	T_J, T_{stg} T_J, T_{stg}		- 65 to + 150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	8.34	°C/W
Thermal Resistance, junction to Ambient	$R\theta_{JA}$	83.3	°C/W



NOTES:
 1. MT = MAIN TERMINAL
 2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.83	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.84	0.99	0.035	0.039
U	3.89	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-126

◇ Annular Semiconductors Patented by Motorola Inc.
 △ Trademark of Motorola Inc.

BD775, BD777, BD779 NPN
BD776, BD778, BD780 PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
OFF CHARACTERISTICS				
Collector-Emitter Collector-Emitter Sustaining Voltage (1) ($I_C = 10\text{ mAdc}$, $I_B = 0$) BD775, BD776 BD777, BD778 BD779, BD780	V_{CE0} (sus)	45 60 80		Vdc
Collector Cutoff Current ($V_{CE} = 20\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 30\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40\text{ Vdc}$, $I_B = 0$) BD775, BD776 BD777, BD778 BD779, BD780	I_{CE0}		100 100 100	μAdc
Collector Cutoff Current ($V_{CB} = \text{Rated}$, V_{CE0} (sus), $I_E = 0$) ($V_{CB} = \text{Rated}$, V_{CE0} (sus), $I_E = 0$, $I_C = 100^\circ\text{C}$)	I_{CBO}		1.0 100	μAdc
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}		1.0	μAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 2.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$)	H_{FE}	750		
Collector-Emitter Saturation Voltage ($I_C = 1.5\text{ Adc}$, $I_B = 6\text{ mAdc}$)	$V_{CE}(\text{Sat})$		1.5	Vdc
Base Emitter Saturation Voltage ($I_C = 1.5\text{ Adc}$, $I_B = 6\text{ mAdc}$)	$V_{BE}(\text{Sat})$		2.5	Vdc
Base-Emitter On Voltage ($I_C = 1.5\text{ Adc}$, $V_{CE} = 3\text{ Vdc}$)	$V_{BE}(\text{On})$		2.3	Vdc
Output Diode Voltage Drop ($I_{EC} = 2.0\text{ Adc}$)	V_{EC}		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain Bandwidth Product ($I_C = 1.0\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$)	f_T	20		MHz
	SYMBOL		TYP.	UNIT
Turn-On Time ($I_C = 250\text{ mA}$, $V_{CE} = 2\text{ V}$) BD775-777-779 BD776-778-780	t_{on}	25	250 250 150	ns
Turn Off Time ($I_C = 250\text{ mA}$, $V_{CE} = 2\text{ V}$) BD775-777-779 BD776-778-780	t_{off}		600 400	ns

3

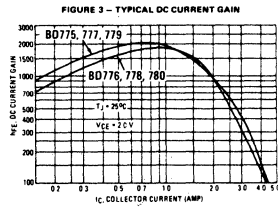
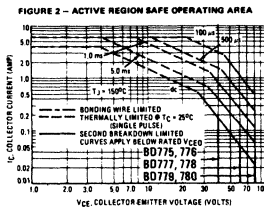
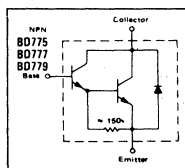
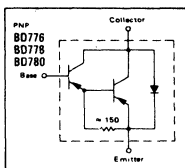


FIGURE 4 - DA RLINGTON CIRCUIT SCHEMATIC



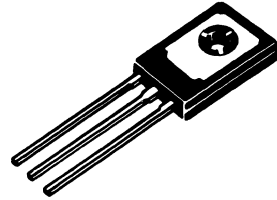
NPN
BD785, BD787
PNP
BD786, BD788

COMPLEMENTARY PLASTIC SILICON ANNULAR[♦]
POWER TRANSISTORS

... designed for low power audio amplifier and low current, high-speed switching applications.

- Low Collector-Emitter Sustaining Voltage –
 V_{CE0} (sus) 45 Vdc (Min) – BD785, BD786
 60 Vdc (Min) – BD787, BD788
- High Current-Gain – Bandwidth Product –
 $f_T = 50$ MHz (Min) @ $I_C = 100$ mAdc
- DC Current Gain Specified at 0.2, 1.0, 2.0 and 4.0 Adc
- Collector-Emitter Saturation Voltage Specified at 0.5, 1.0, 2.0 and 4.0 Adc

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
45, 60VOLTS
15 WATTS

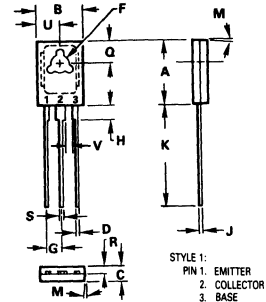


***MAXIMUM RATINGS**

Rating	Symbol	BD785 BD786	BD787 BD788	Unit
Collector-Emitter Voltage	V_{CE0}	45	60	Vdc
Collector-Base Voltage	V_{CB0}	60	80	Vdc
Emitter-Base Voltage	V_{EB0}	6.0		Vdc
Collector Current – Continuous	I_C	4.0		Adc
– Peak		8.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	15		Watts
Derate Above 25°C		0.12		W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

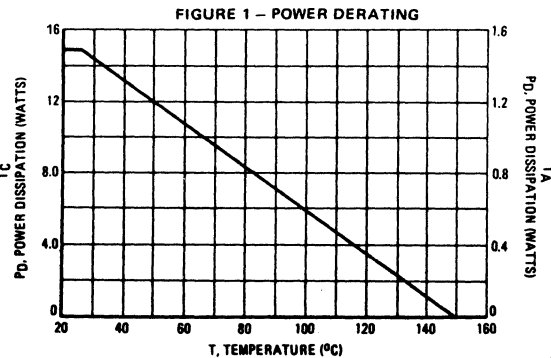
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	$^\circ\text{C/W}$



- NOTES:
 1. MT – MAIN TERMINAL
 2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010)
 DIA TO DIM A & B AT MAXIMUM MATERIAL
 CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3" TYP			
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-126



BD785, BD787 NPN
BD786, BD788 PNP

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 10 \text{ mAdc}$, $I_B = 0$) BD785, BD786 BD787, BD788	$V_{CE(sus)}$	45 60	— —	Vdc
Collector Cutoff Current ($V_{CE} = 20 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) BD785, BD786 BD787, BD788	I_{CEO}	— —	100 100	μAdc
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) BD785, BD786 BD787, BD788	I_{CEX}	— —	1.0 1.0	μAdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$) ($V_{CE} = 40 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 125^\circ\text{C}$) BD785, BD786 BD787, BD788	I_{CEX}	— —	0.1 0.1	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	μAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 200 \text{ mAdc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	h_{FE}	40 25 20 5.0	250 — — —	—
Collector-Emitter Saturation Voltage ($I_C = 500 \text{ mAdc}$, $I_B = 50 \text{ mAdc}$) ($I_C = 1.0 \text{ Adc}$, $I_B = 100 \text{ mAdc}$) ($I_C = 2.0 \text{ Adc}$, $I_B = 200 \text{ mAdc}$) ($I_C = 4.0 \text{ Adc}$, $I_B = 800 \text{ mAdc}$)	$V_{CE(sat)}$	— — — —	0.4 0.6 0.8 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 2.0 \text{ Adc}$, $I_B = 200 \text{ mAdc}$)	$V_{BE(sat)}$	—	2.0	Vdc
Base-Emitter on Voltage ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.8	Vdc

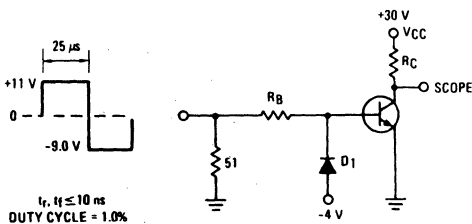
DYNAMIC CHARACTERISTICS

Current-Gain - Bandwidth Product ($I_C = 100 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 10 \text{ MHz}$)	f_T	50	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_C = 0$) $f = 0.1 \text{ MHz}$ BD785, BD787 BD786, BD788	C_{ob}	— —	50 70	pF
Small-Signal Current Gain ($I_C = 200 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	10	—	—

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$

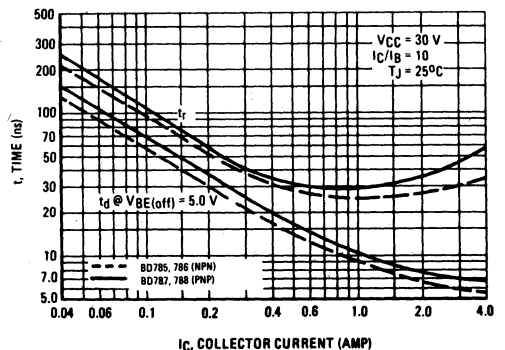
FIGURE 2 - SWITCHING TIME TEST CIRCUIT



D1 MUST BE FAST RECOVERY TYPE, eg:
 M805300 USED ABOVE $I_B \approx 100 \text{ mA}$
 MS06100 USED BELOW $I_B \approx 100 \text{ mA}$

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 - TURN-ON TIME



BD785, BD787 NPN
BD786, BD788 PNP

FIGURE 4 – THERMAL RESPONSE

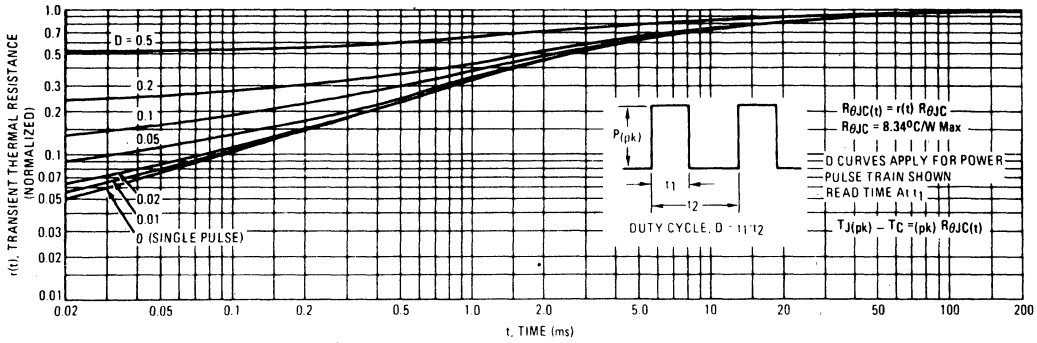
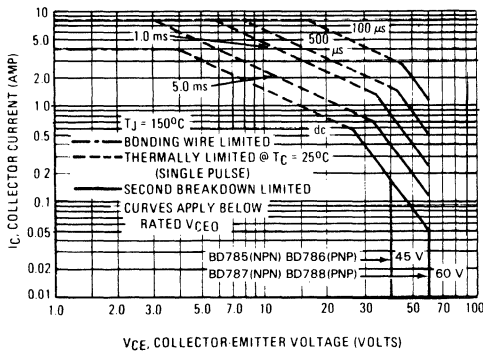


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 5 is based on $T_{j(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{j(pk)} \leq 150^{\circ}\text{C}$. $T_{j(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 6 – TURN-OFF TIME

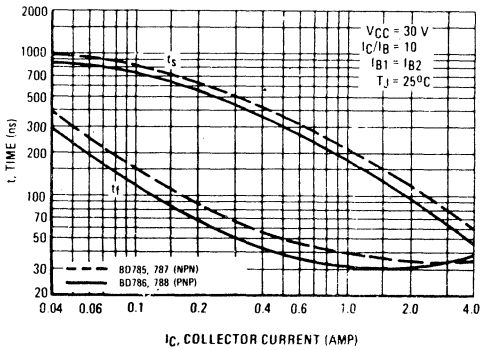
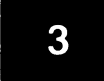
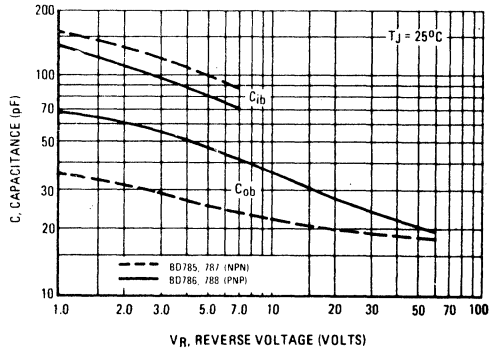


FIGURE 7 – CAPACITANCE



BD785, BD787 NPN
BD786, BD788 PNP

NPN
BD785, BD787

PNP
BD786, BD788

FIGURE 8 – DC CURRENT GAIN

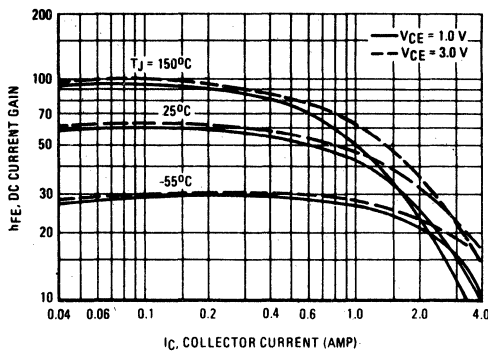
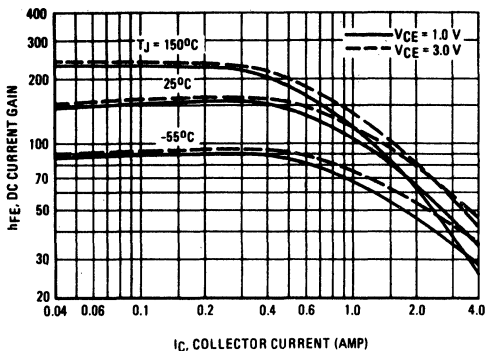
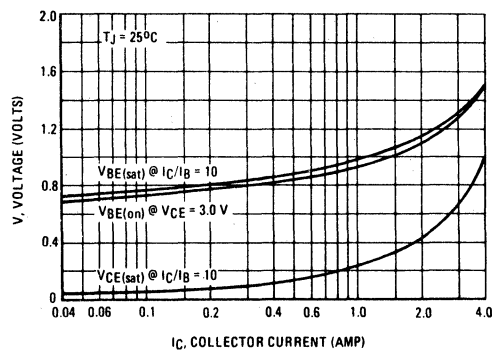
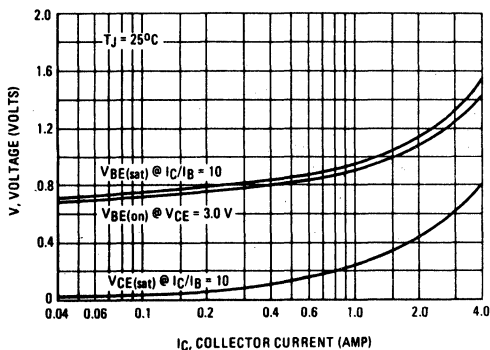
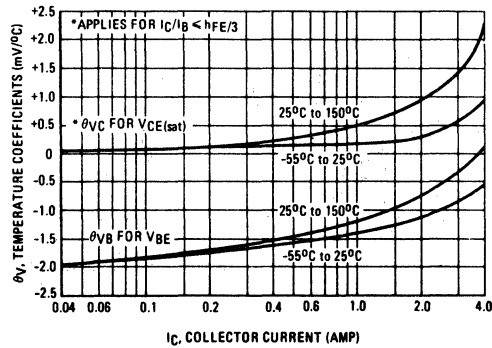
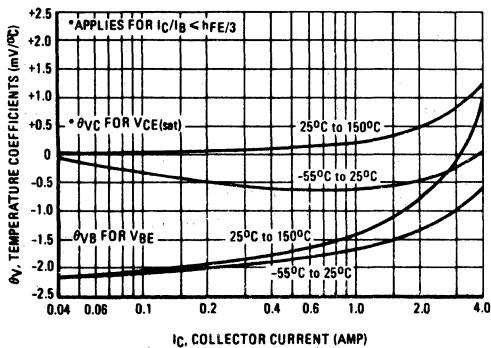


FIGURE 9 – "ON" VOLTAGES



3

FIGURE 10 – TEMPERATURE COEFFICIENTS



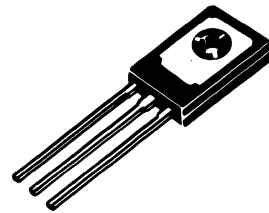
NPN
BD789, BD791
PNP
BD790, BD792

COMPLEMENTARY PLASTIC SILICON ANNULAR[♦]
POWER TRANSISTORS

... designed for low power audio amplifier and low-current, high speed switching applications.

- High Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 80 \text{ Vdc (Min) – BD789, BD790}$
 $= 100 \text{ Vdc (Min) – BD791, BD792}$
- High DC Current Gain @ $I_C = 200 \text{ mAdc}$
 $h_{FE} = 40\text{-}250$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.5 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$
- High Current Gain – Bandwidth Product –
 $f_T = 40 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
80, 100 VOLTS
15 WATTS

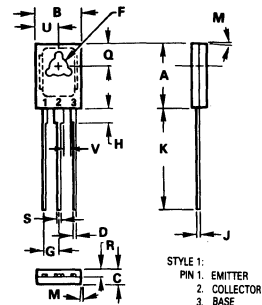
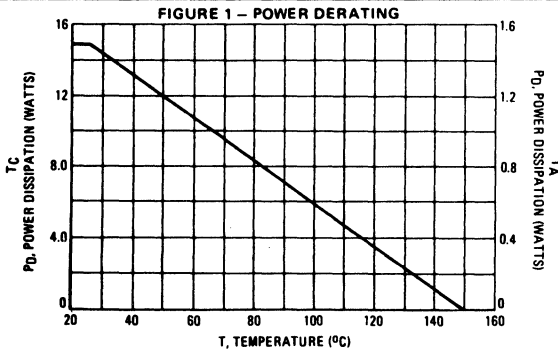


***MAXIMUM RATINGS**

Rating	Symbol	BD789 BD790	BD791 BD792	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current – Continuous	I_C	4.0		Adc
– Peak		8.0		
Base Current	I_B	1.0		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	15	0.12	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	$^\circ\text{C/W}$



- NOTES:
 1. M² – MAIN TERMINAL.
 2. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010)
 DIA TO DIM A & B AT MAXIMUM MATERIAL
 CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
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J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
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U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05
TO-126

BD789, BD791 NPN
BD790, BD792 PNP

***ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)**

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I _C = 10 mA _{dc} , I _B = 0)	BD789, BD790 BD791, BD792	V _{CEO(sus)}	80 100	— —	V _{dc}
Collector Cutoff Current (V _{CE} = 40 V _{dc} , I _B = 0) (V _{CE} = 50 V _{dc} , I _B = 0)	BD789, BD790 BD791, BD792	I _{CEO}	— —	100 100	μA _{dc}
Collector Cutoff Current (V _{CE} = 80 V _{dc} , V _{BE(off)} = 1.5 V _{dc}) (V _{CE} = 100 V _{dc} , V _{BE(off)} = 1.5 V _{dc}) (V _{CE} = 40 V _{dc} , V _{BE(off)} = 1.5 V _{dc} , T _C = 125°C) (V _{CE} = 50 V _{dc} , V _{BE(off)} = 1.5 V _{dc} , T _C = 125°C)	BD789, BD790 BD791, BD792 BD789, BD790 BD791, BD792	I _{CEX}	— — — —	1.0 1.0 0.1 0.1	μA _{dc} mA _{dc}
Emitter Cutoff Current (V _{EB} = 6.0 V _{dc} , I _C = 0)		I _{EBO}	—	1.0	μA _{dc}

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 200 mA _{dc} , V _{CE} = 3.0 V _{dc}) (I _C = 1.0 A _{dc} , V _{CE} = 3.0 V _{dc}) (I _C = 2.0 A _{dc} , V _{CE} = 3.0 V _{dc}) (I _C = 4.0 A _{dc} , V _{CE} = 3.0 V _{dc})	h _{FE}	40 20 10 5.0	— — — —	250 — — —	—
Collector-Emitter Saturation Voltage (I _C = 500 mA _{dc} , I _B = 50 mA _{dc}) (I _C = 1.0 A _{dc} , I _B = 100 mA _{dc}) (I _C = 2.0 A _{dc} , I _B = 200 mA _{dc}) (I _C = 4.0 A _{dc} , I _B = 800 mA _{dc})	V _{CE(sat)}	— — — —	— — — —	0.5 1.0 2.5 3.0	V _{dc}
Base-Emitter Saturation Voltage (I _C = 2.0 A _{dc} , I _B = 200 mA _{dc})	V _{BE(sat)}	—	—	1.8	V _{dc}
Base-Emitter On Voltage (I _C = 200 mA _{dc} , V _{CE} = 3.0 V _{dc})	V _{BE(on)}	—	—	1.5	V _{dc}

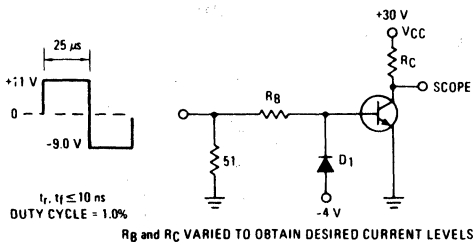
DYNAMIC CHARACTERISTICS

Current-Gain – Bandwidth Product (I _C = 100 mA _{dc} , V _{CE} = 10 V _{dc} , f = 10 MHz)	f _T	40	—	—	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _C = 0, f = 0.1 MHz)	C _{ob}	—	—	50 70	pF
Small-Signal Current Gain (I _C = 200 mA _{dc} , V _{CE} = 10 V _{dc} , f = 1.0 kHz)	h _{fe}	10	—	—	—

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

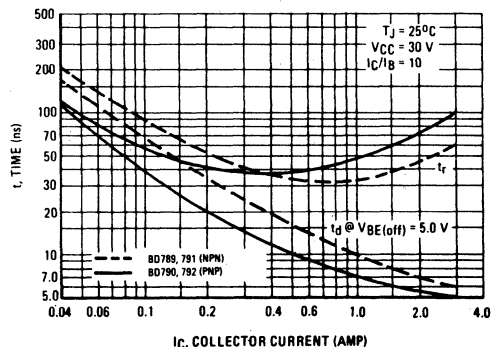
FIGURE 2 – SWITCHING TIME TEST CIRCUIT



D₁ MUST BE FAST RECOVERY TYPE, eg:
 M8D5300 USED ABOVE I_B = 100 mA
 MSD6100 USED BELOW I_B = 100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME



BD789, BD791 NPN
BD790, BD792 PNP

FIGURE 4 – THERMAL RESPONSE

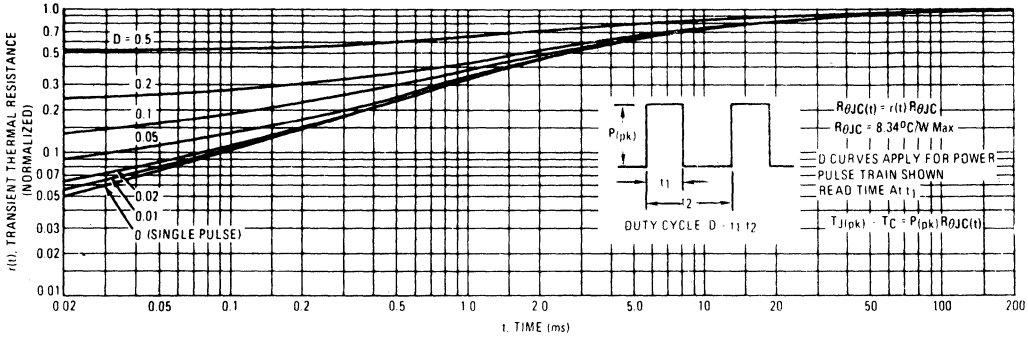
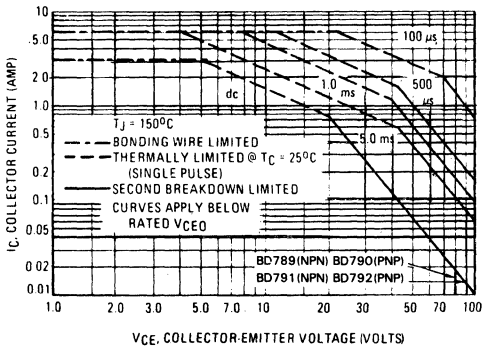


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C V_{CE} limits of the transistor that must be observed for reliable operation, i.e. the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415A)

FIGURE 6 – TURN-OFF TIME

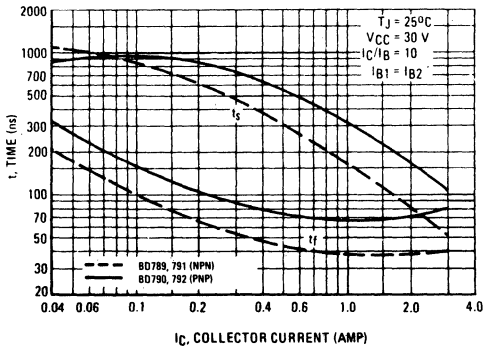
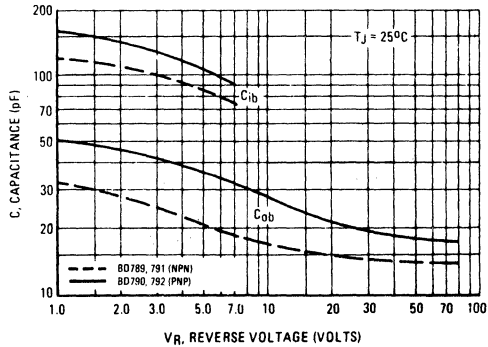


FIGURE 7 – CAPACITANCE



BD789, BD791 NPN
BD790, BD792 PNP

NPN
BD789, BD791

PNP
BD790, BD792

FIGURE 8 - DC CURRENT GAIN

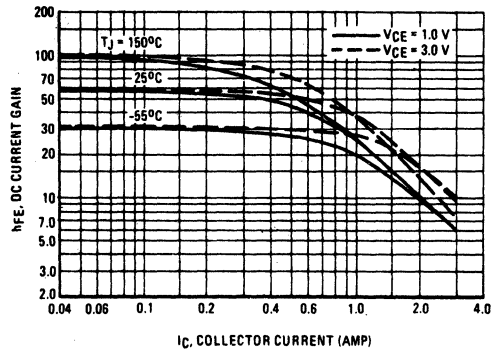
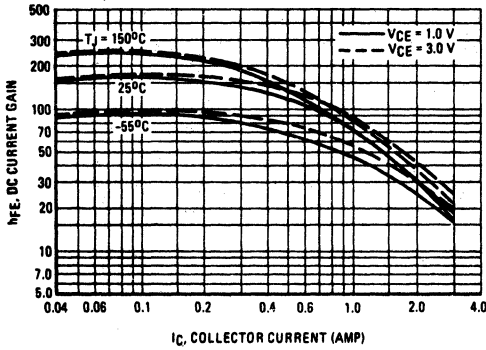


FIGURE 9 - "ON" VOLTAGES

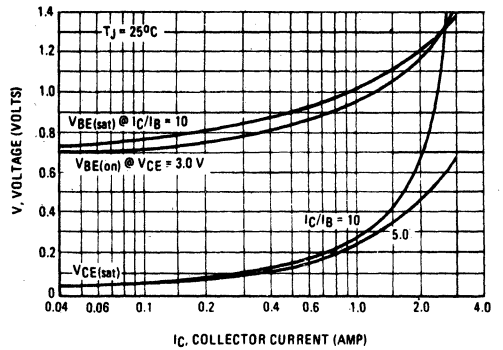
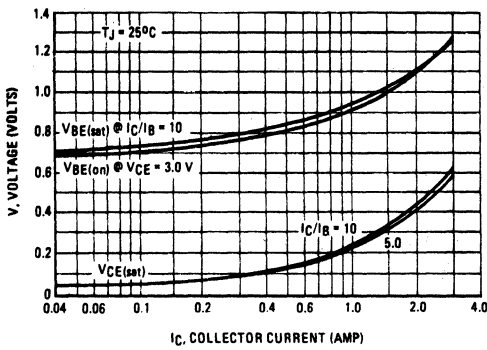
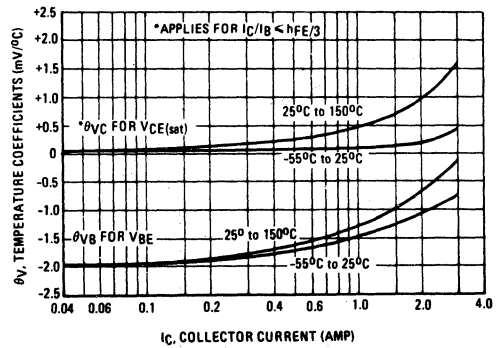
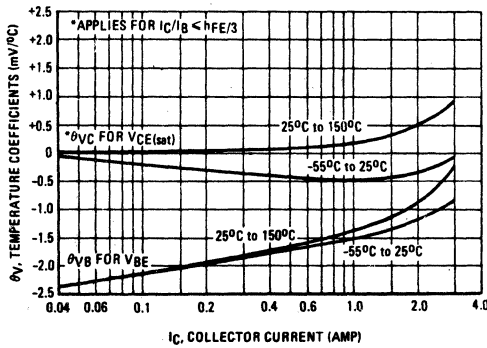


FIGURE 10 - TEMPERATURE COEFFICIENTS



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

BD795 BD797

BD799 BD801

PLASTIC HIGH POWER SILICON NPN TRANSISTOR

designed for use up to 30 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 1.0$ Adc
- BD 795, 797, 799, 801 are complementary with BD 796, 798, 800, 802

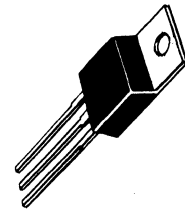
8 AMPERE POWER TRANSISTOR

NPN SILICON

45, 60, 80, 100 VOLTS
65 WATTS

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD795 BD797 BD799 BD801	45 60 80 100	Vdc
Collector-Base Voltage	V_{CBO}	BD795 BD797 BD799 BD801	45 60 80 100	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		8	Adc
Base Current	I_B		3	Adc
Total Device Dissipation $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D		65 522	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150	$^\circ\text{C}$



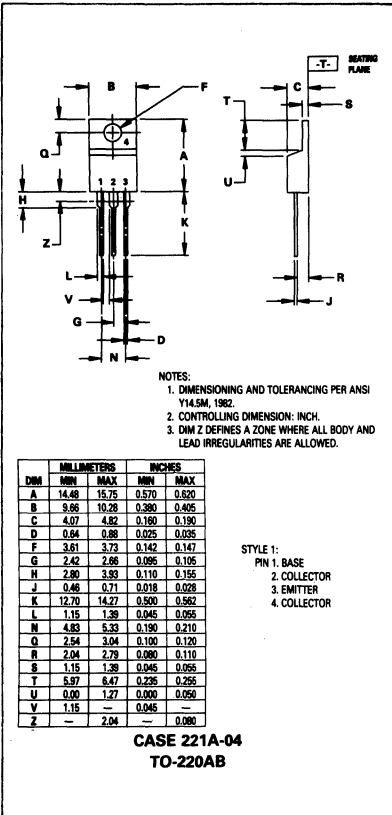
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.92	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

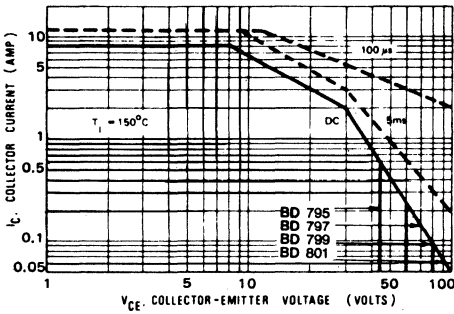
Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$) ($I_C = 0.05$ Adc, $I_B = 0$)	BV_{CEO}	BD795 BD797 BD799 BD801	45 60 80 100	—	Vdc
Collector Cutoff Current ($V_{CB} = 45$ Vdc, $I_E = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$) ($V_{CB} = 100$ Vdc, $I_E = 0$)	I_{CBO}	BD795 BD797 BD799 BD801	—	0.1 0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mAdc
DC current Gain ($I_C = 1$ A, $V_{CE} = 2$ V) ($I_C = 3$ A, $V_{CE} = 2$ V)	h_{FE}	BD 795/797 BD 799/801 BD 795/797 BD 799/801	40 30 25 15	—	
Collector-Emitter Saturation Voltage* ($I_C = 3$ Adc, $I_B = 0.3$ Adc)	$V_{CE(sat)}$		—	1.0	Vdc
Base-Emitter On Voltage* ($I_C = 3$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$		—	1.6	Vdc
Current-Gain-Bandwidth Product ($I_C = 0.25$ Adc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs . Duty Cycle $\leq 2.0\%$.



BD795, BD797, BD799, BD801

FIGURE 1 - ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C - V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 - COLLECTOR SATURATION REGION

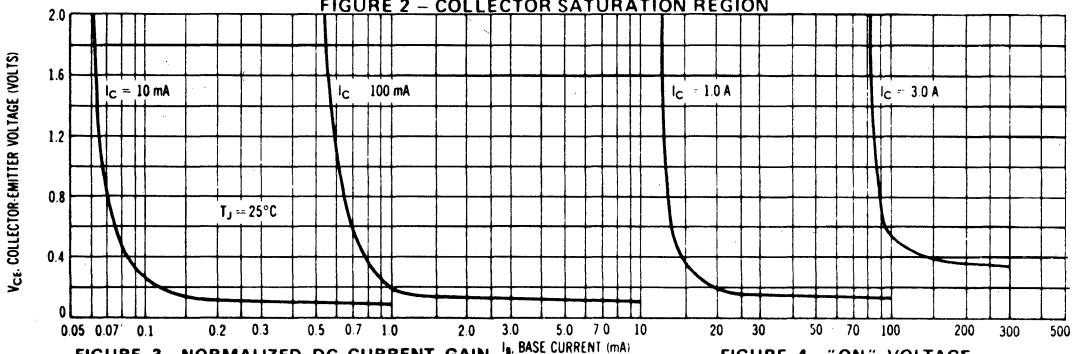


FIGURE 3 - NORMALIZED DC CURRENT GAIN

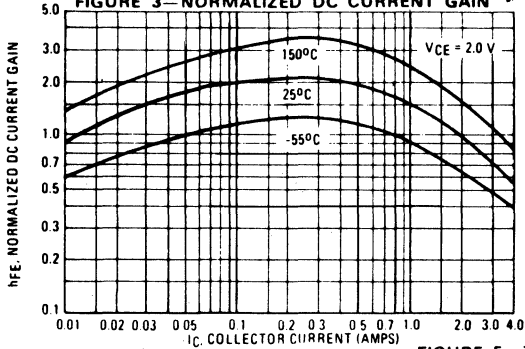


FIGURE 4 - "ON" VOLTAGE

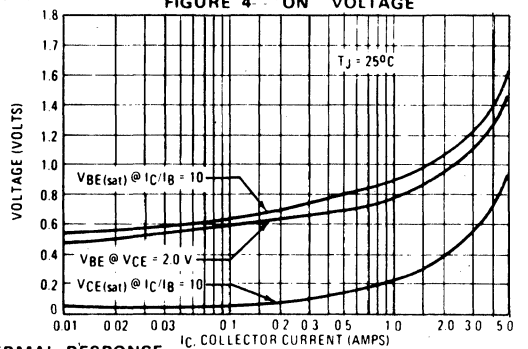
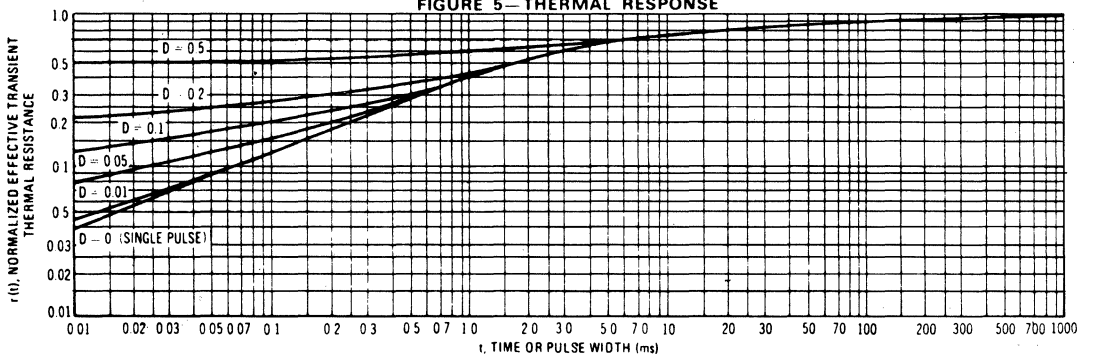


FIGURE 5 - THERMAL RESPONSE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD796
BD798

BD800
BD802

**PLASTIC HIGH POWER
SILICON PNP TRANSISTOR**

designed for use up to 30 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain— $h_{FE} = 40$ (Min) @ $I_C = 1.0$ Adc
- BD 796, 798, 800, 802 are complementary with BD 795, 797, 799, 801

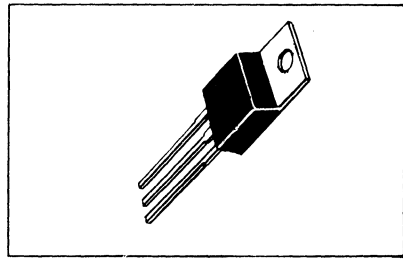
**8 AMPERE
POWER TRANSISTOR**

PNP SILICON

**45, 60, 80, 100 VOLTS
65 WATTS**

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD796 BD798 BD800 BD802	45 60 80 100	Vdc
Collector-Base Voltage	V_{CBO}	BD796 BD798 BD800 BD802	45 60 80 100	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		8	A dc
Base Current	I_B		3	A dc
Total Device Dissipation Derate above 25°C	P_D		65 522	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150	°C

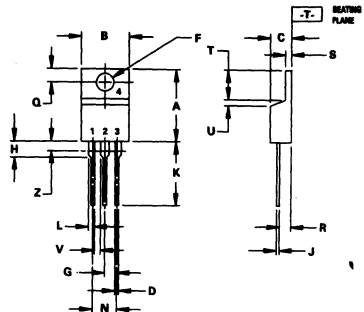


THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.92	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.1$ Adc, $I_B = 0$) ($I_C = 0.05$ Adc, $I_B = 0$)	V_{CEO}	BD796 BD798 BD800 BD802	45 60 80 100	—	Vdc
Collector Cutoff Current ($V_{CB} = 45$ Vdc, $I_E = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$) ($V_{CB} = 100$ Vdc, $I_E = 0$)	I_{CBO}	BD796 BD798 BD800 BD802	—	0.1 0.1 0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	1.0	mAdc
DC current Gain ($I_C = 1$ A, $V_{CE} = 2$ V) ($I_C = 3$ A, $V_{CE} = 2$ V)	h_{FE}	BD 796/798 BD 800/802 BD 796/788 BD 800/802	40 30 25 15	—	
Collector-Emitter Saturation Voltage* ($I_C = 3$ Adc, $I_B = 0.3$ Adc)	$V_{CE(sat)}$		—	1.0	Vdc
Base-Emitter On Voltage* ($I_C = 3$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$		—	1.6	Vdc
Current-Gain-Bandwidth Product ($I_C = 0.25$ Adc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		3.0	—	MHz



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.86	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
M	4.82	5.33	0.190	0.210
Q	2.54	3.84	0.100	0.150
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

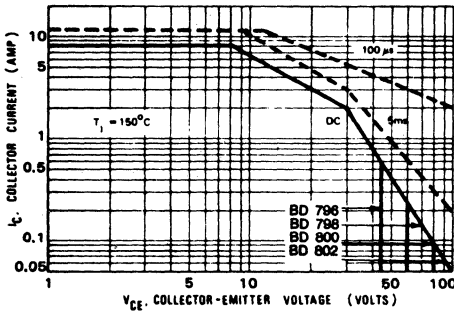
**CASE 221A-04
TO-220AB**

3

Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

BD796, BD798, BD800, BD802

FIGURE 1 - ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C - V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 - COLLECTOR SATURATION REGION

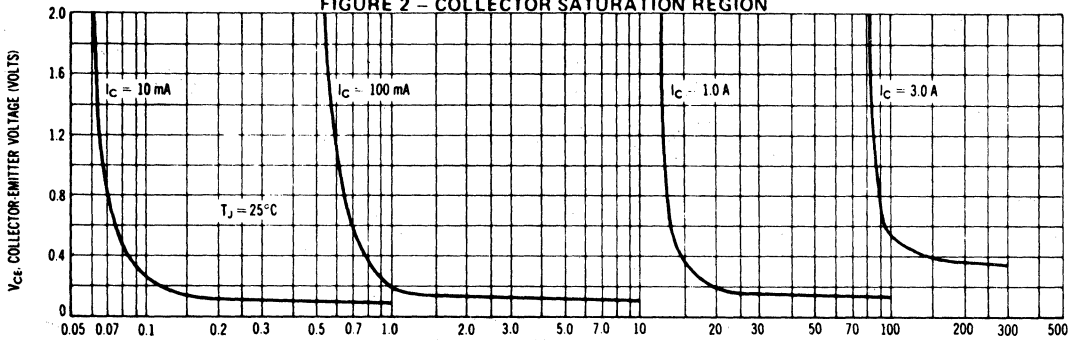


FIGURE 3 - NORMALIZED DC CURRENT GAIN

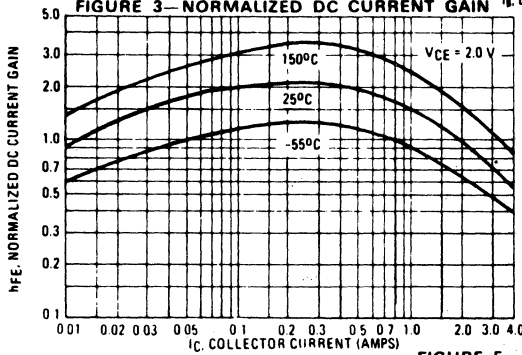


FIGURE 4 - "ON" VOLTAGE

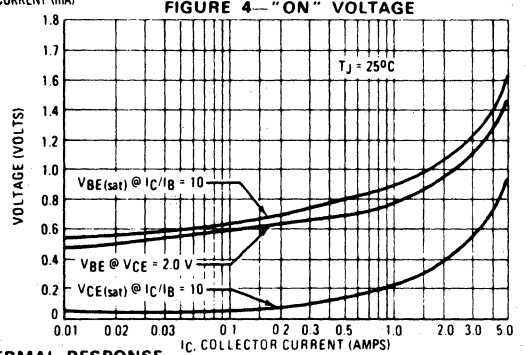
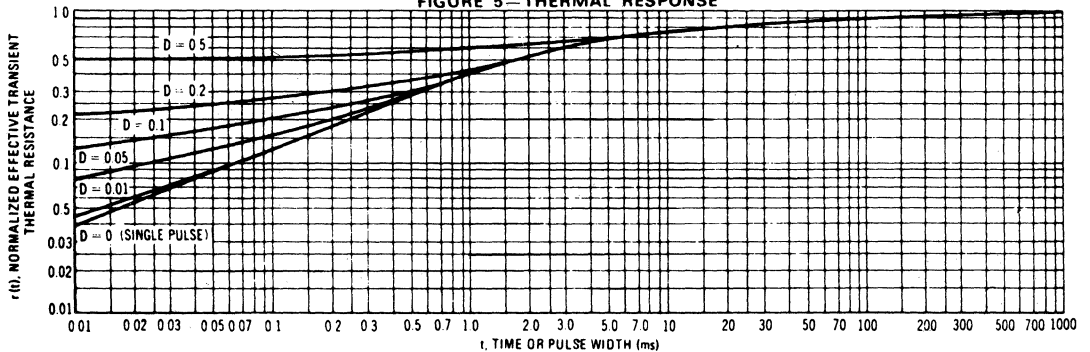


FIGURE 5 - THERMAL RESPONSE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD805
BD807
BD809

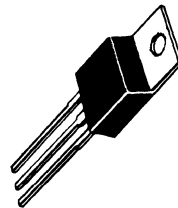
PLASTIC HIGH POWER
SILICON NPN TRANSISTOR

... designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current— $h_{FE} = 30$ (Min) @ $I_C = 2.0$ Adc
- BD 805, 807, 809 are complementary with BD 806, 808, 810

10 AMPERE
POWER TRANSISTOR
NPN SILICON

45, 60, 80 VOLTS
90 WATTS



MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD805 BD807 BD809	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD805 BD807 BD809	55 70 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	A dc
Base Current	I_B		6.0	A dc
Total Device Dissipation Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150	°C

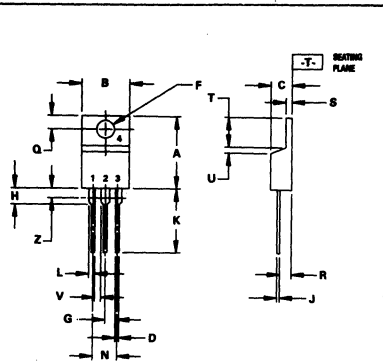
TERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.2$ Adc, $I_B = 0$)	BV_{CEO}	BD805 BD807 BD809	45 60 80	—	Vdc
Collector Cutoff Current ($V_{CB} = 55$ Vdc, $I_E = 0$) ($V_{CB} = 70$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	I_{CBO}	BD805 BD807 BD809	—	1.0 1.0 1.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	2.0	mAdc
DC current Gain ($I_C = 2$ A, $V_{CE} = 2$ V) ($I_C = 4$ A, $V_{CE} = 2$ V)	h_{FE}		30 15	—	
Collector-Emitter Saturation Voltage* ($I_C = 4$ Adc, $I_B = 0.4$ Adc)	$V_{CE(sat)}$		—	1.1	Vdc
Base-Emitter On Voltage* ($I_C = 4$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$		—	1.6	Vdc
Current Gain-Bandwidth Product ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		15	—	MHz

Pulse Test: Pulse Width $\leq 300 \mu\text{s}$ Duty Cycle $\leq 2.0\%$



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.67	4.82	0.180	0.190
D	0.64	0.86	0.025	0.035
F	3.81	3.73	0.142	0.147
Q	2.62	2.66	0.095	0.105
H	2.90	3.32	0.110	0.135
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.26	0.045	0.055
M	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.94	2.79	0.095	0.110
S	1.15	1.26	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 221A-04
TO-220AB

FIGURE 1 — ACTIVE REGION DC SAFE OPERATING AREA

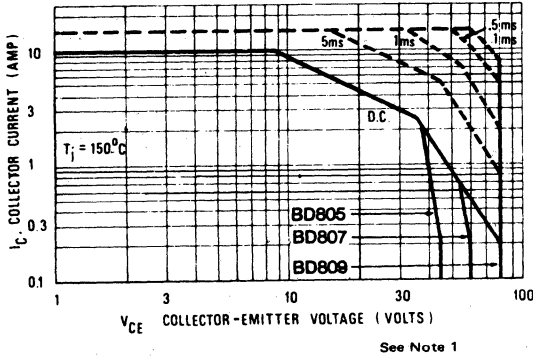


FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

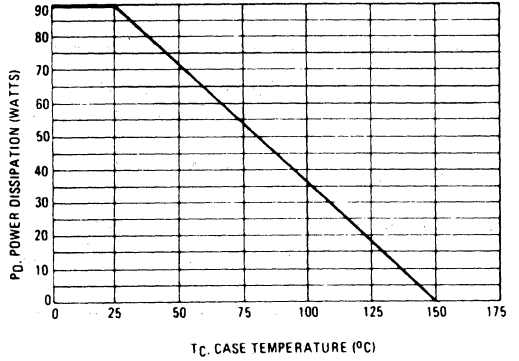


FIGURE 3 — "ON" VOLTAGES

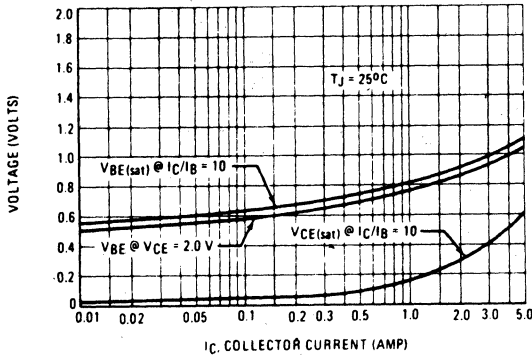


FIGURE 4 — CURRENT GAIN

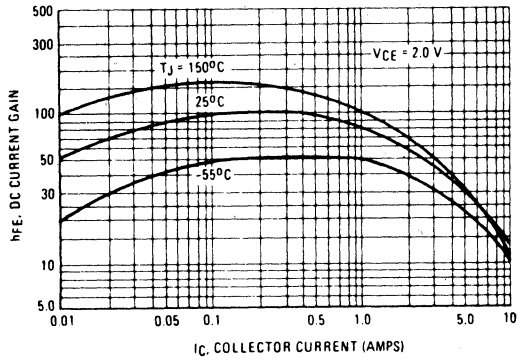
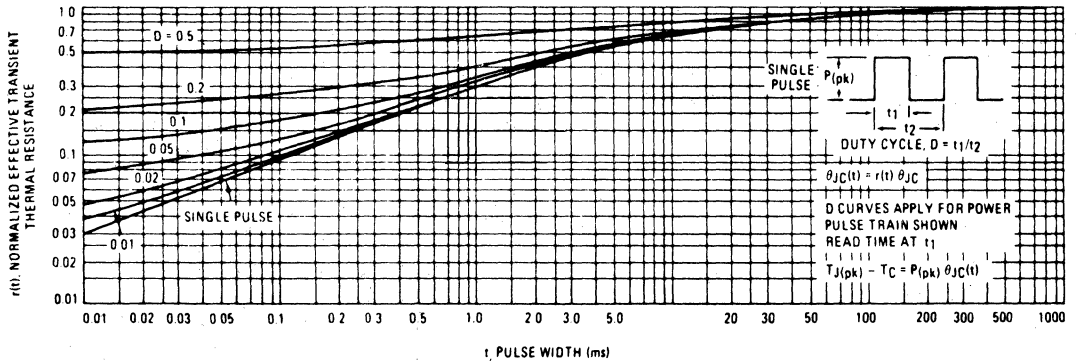


FIGURE 5 — THERMAL RESPONSE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C \cdot V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD806
BD808
BD810

**PLASTIC HIGH POWER
 SILICON PNP TRANSISTOR**

... designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current— $h_{FE} = 30$ (Min) @ $I_C = 2.0$ Adc
- BD 806, 808, 810 are complementary with BD 805, 807, 809

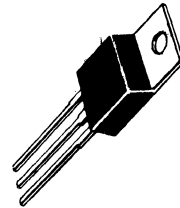
**10 AMPERE
 POWER TRANSISTOR**

PNP SILICON

**45, 60, 80 VOLTS
 90 WATTS**

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	V_{CEO}	BD806 BD808 BD810	45 60 80	Vdc
Collector-Base Voltage	V_{CBO}	BD806 BD808 BD810	55 70 80	Vdc
Emitter-Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		10.0	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-55 to +150	°C



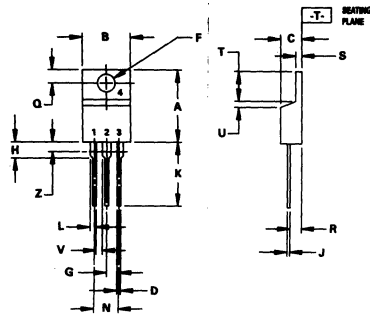
HERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ($I_C = 0.2$ Adc, $I_B = 0$)	BV_{CEO}	BD806 BD808 BD810	45 60 80	—	Vdc
Collector Cutoff Current ($V_{CB} = 55$ Vdc, $I_E = 0$) ($V_{CB} = 70$ Vdc, $I_E = 0$) ($V_{CB} = 80$ Vdc, $I_E = 0$)	I_{CBO}	BD806 BD808 BD810	—	1.0 1.0 1.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}		—	2.0	mAdc
DC current Gain ($I_C = 2A, V_{CE} = 2V$) ($I_C = 4A, V_{CE} = 2V$)	h_{FE}		30 15	—	
Collector-Emitter Saturation Voltage* ($I_C = 4$ Adc, $I_B = 0.4$ Adc)	$V_{CE(sat)}$		—	1.1	Vdc
Base-Emitter On Voltage* ($I_C = 4$ Adc, $V_{CE} = 2.0$ Vdc)	$V_{BE(on)}$		—	1.6	Vdc
Current-Gain-Bandwidth Product ($I_C = 1.0$ Adc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T		1.5	—	MHz

Pulse Test: Pulse Width $\leq 300 \mu\text{s}$. Duty Cycle $\leq 20\%$.



NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.86	10.28	0.390	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.98	0.025	0.039
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
O	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.87	6.47	0.230	0.255
U	0.90	1.27	0.030	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

**CASE 221A-04
 TO-220AB**

STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

FIGURE 1 - ACTIVE REGION DC SAFE OPERATING AREA

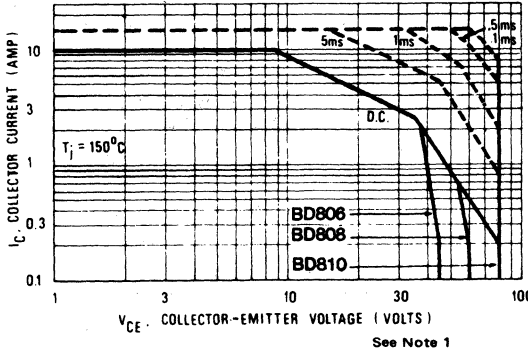


FIGURE 2 - POWER-TEMPERATURE DERATING CURVE

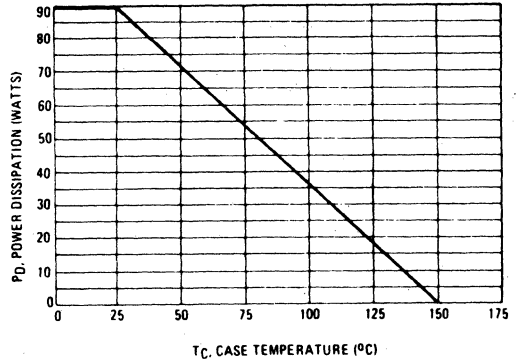


FIGURE 3 - "ON" VOLTAGES

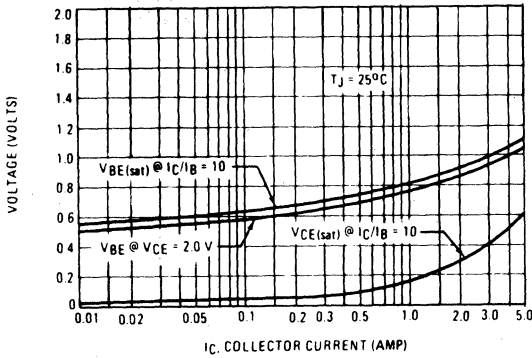


FIGURE 4 - CURRENT GAIN

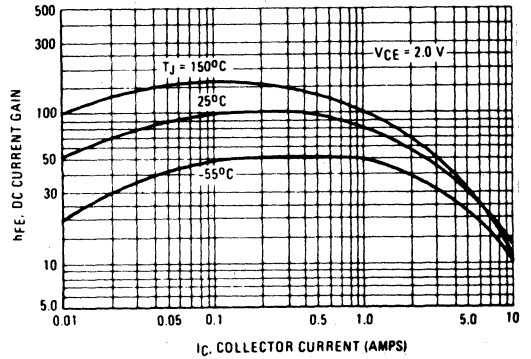
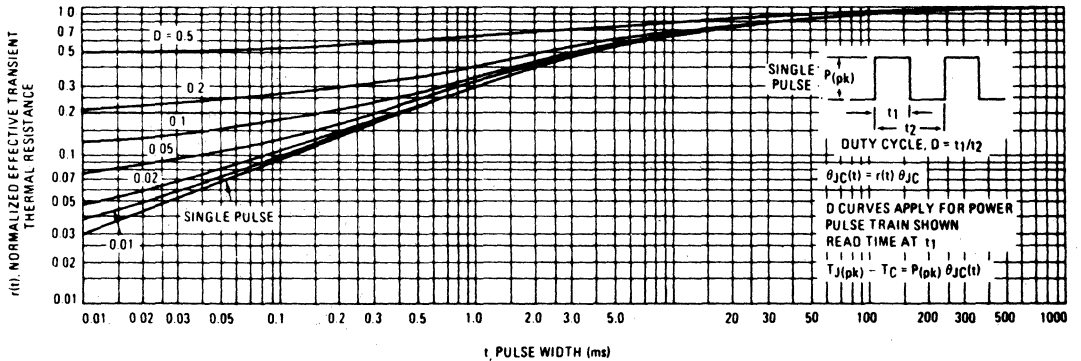


FIGURE 5 - THERMAL RESPONSE



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C \cdot V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BD895, BD895A
BD897, BD897A
BD899, BD899A
BD901

PLASTIC POWER SILICON NPN DARLINGTONS

... for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain —
 $h_{FE} = 750$ (Min) @ $I_C = 3.0$ and 4.0 Adc
- Monolithic Construction
- BD895, 895A, 897, 897A, 899, 899A, 901 are complementary with BD896, 896A, 898, 898A, 900, 900A, 902.
- Electrical equivalents to BD695A, 697, 697A, 699, 699A, 701.

DARLINGTON
8 AMPERE
NPN SILICON
POWER TRANSISTORS

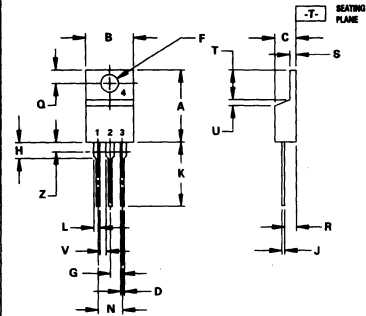
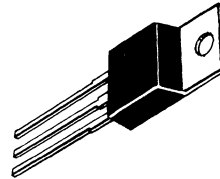
45-60-80-100 VOLTS
70 WATTS

MAXIMUM RATINGS

Rating	Symbol	BD895 BD895A	BD897 BD897A	BD899 BD899A	BD901	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	8.0				Aadc
Base Current	I_B	0.1				Aadc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	70				Watts
		0.56				W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150				$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.79	$^\circ\text{C}/\text{W}$



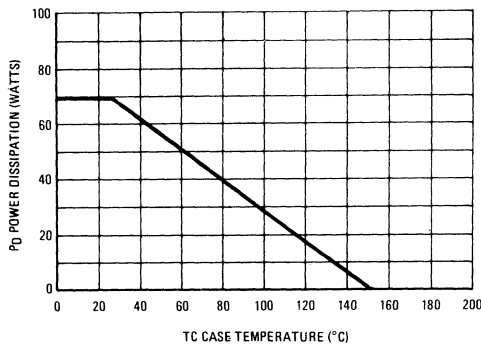
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.86	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
M	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.90	1.27	0.030	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

FIGURE 1 — POWER TEMPERATURE DERATING CURVE



BD895, BD895A, BD897, BD897A, BD899, BD899A, BD901

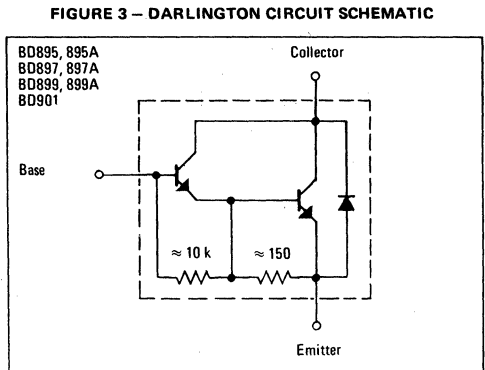
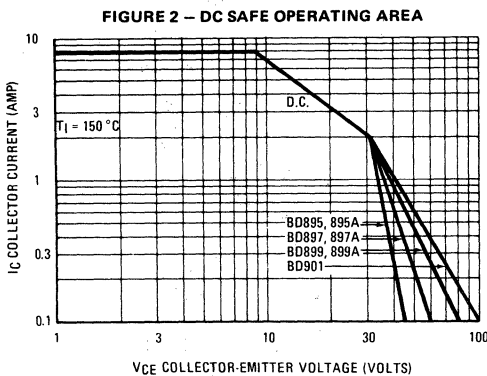
ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ¹ ($I_C = 100\text{ mAdc}$, $I_B = 0$)	BD895, 895A BD897, 897A BD899, 899A BD901	BV_{CEO}	45 60 80 100	— — — —	Vdc
Collector Cutoff Current ($V_{CE} = \text{Half Rated } BV_{CEO}$, $I_B = 0$)		I_{CEO}	—	500	μAdc
Collector Cutoff Current ($V_{CB} = \text{Rated } BV_{CEO}$, $I_E = 0$) ($V_{CB} = \text{Rated } BV_{CEO}$, $I_E = 0$, $T_C = 100^\circ\text{C}$)		I_{CBO}	—	0.2 2.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain ¹ ($I_C = 3.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$) ($I_C = 4.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$)	BD895, 897, 899, 901 BD895A, 897A, 899A	h_{FE}	750 750	— —	—
Collector-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 12\text{ mAdc}$) ($I_C = 4.0\text{ Adc}$, $I_B = 16\text{ mAdc}$)	BD895, 897, 899, 901 BD895A, 897A, 899A	$V_{CE(sat)}$	— —	2.5 2.8	Vdc
Base-Emitter On Voltage ¹ ($I_C = 3.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$) ($I_C = 4.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$)	BD895, 897, 899, 901 BD895A, 897A, 899A	$V_{BE(on)}$	— —	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$, $f = 1.0\text{ MHz}$)		h_{fe}	1.0	—	—

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must

not be subjected to greater dissipation than the curves indicate. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown (see AN-415).



MOTOROLA
SEMICONDUCTOR
 TECHNICAL DATA

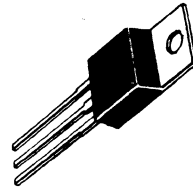
BD896, BD896A
BD898, BD898A
BD900, BD900A
BD902

PLASTIC MEDIUM-POWER
PNP TRANSISTORS

... for use as output devices in complementary general-purpose amplifier applications.

- High DC Current Gain –
 $h_{FE} = 750$ (Min) @ $I_C = 3.0$ and 4.0 Adc
- Monolithic Construction
- BD896A, 898, 898A, 900, 900A, 902 are complementary with BD895A, 897, 897A, 899, 899A, 901
- Electrical equivalents to BD696A, 698, 698A, 700, 700A, 702

DARLINGTON
8 AMPERE
SILICON
POWER TRANSISTORS
45-60-80-100 VOLTS
70 WATTS



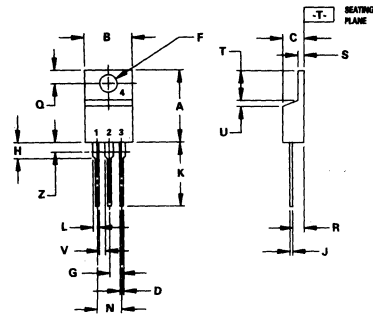
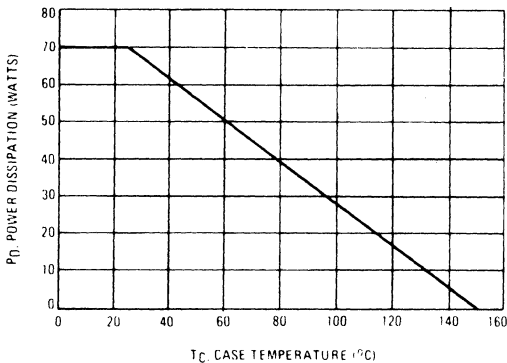
MAXIMUM RATINGS

Rating	Symbol	BD896 BD896A	BD898 BD898A	BD900 BD900A	BD902	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	8.0				A dc
Base Current	I_B	0.1				A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	70				Watts
		0.56				W/ $^\circ\text{C}$
Operating and Storage Junction Temperating Range	T_J, T_{stg}	-55 to +150				$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.79	$^\circ\text{C/W}$

FIGURE 1 – POWER TEMPERATURE DERATING CURVE



- NOTES:
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DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.26	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.81	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 221A-04
TO-220AB

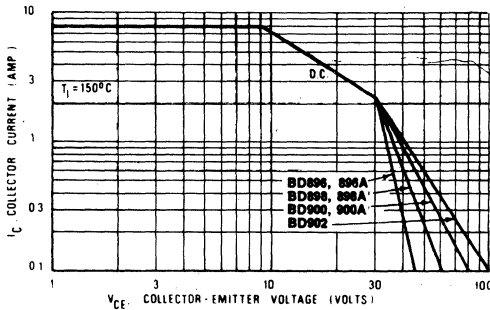
BD896, 896A, BD898, 898A, BD900, 900A, BD902

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ⁽¹⁾ ($I_C = 100 \text{ mAdc}$, $I_B = 0$)	BD896, 896A BD898, 898A BD900, 900A BD902	V_{CE0}	45 60 80 100	— — — —	Vdc
Collector Cutoff Current ($V_{CE} = \text{Half Rated } V_{CE0}$, $I_B = 0$)		I_{CEO}	—	500	μAdc
Collector Cutoff Current ($V_{CB} = \text{Rated } BV_{CE0}$, $I_E = 0$) ($V_{CB} = \text{Rated } BV_{CE0}$, $I_E = 0$, $T_C = 100^\circ\text{C}$)		I_{CBO}	—	0.2 2.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain ⁽¹⁾ ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	BD896, 898, 900, 902 BD896A, 898A, 900A	h_{FE}	750 750	— —	—
Collector-Emitter Saturation Voltage ($I_C = 3.0 \text{ Adc}$, $I_B = 12 \text{ mAdc}$) ($I_C = 4.0 \text{ Adc}$, $I_B = 16 \text{ mAdc}$)	BD896, 898, 900, 902 BD896A, 898A, 900A	$V_{CE(sat)}$	— —	2.5 2.8	Vdc
Base-Emitter On Voltage ⁽¹⁾ ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	BD896, 898, 900, 902 BD896A, 898A, 900A	$V_{BE(on)}$	— —	2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)		h_{fe}	1.0	—	—

⁽¹⁾Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

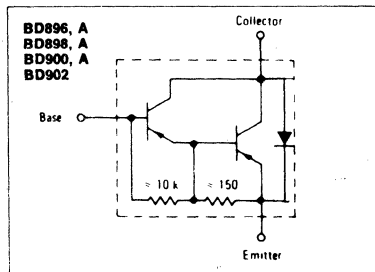
FIGURE 2 - DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 - DARLINGTON CIRCUIT SCHEMATIC



NPN
BDV65
BDV65A
BDV65B
BDV65C

PNP
BDV64
BDV64A
BDV64B
BDV64C

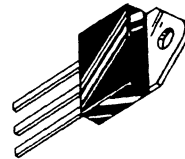
**COMPLEMENTARY SILICON PLASTIC
 POWER DARLINGTONS**

... for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain
 HFE = 1000 (min.) @ 5 Adc
- Monolithic Construction with Built-in
 Base Emitter Shunt Resistors

**DARLINGTONS
 10 AMPERES
 COMPLEMENTARY SILICON
 POWER TRANSISTORS**

**60-80-100-120 VOLTS
 125 WATTS**



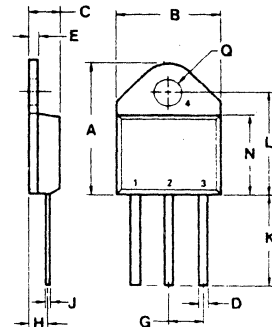
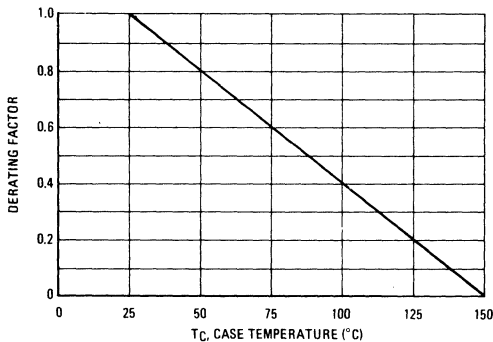
MAXIMUM RATINGS

Rating	Symbol	BDV 65 BDV 64	BDV 65A BDV 64A	BDV 65B BDV 64B	BDV 65C BDV 64C	Unit
Collector-Emitter Voltage	V _{CEO}	60	80	100	120	V _{dc}
Collector-Base Voltage	V _{CB}	60	80	100	120	V _{dc}
Emitter-Base Voltage	V _{EB}	5				V _{dc}
Collector Current	I _C					A _{dc}
- Continuous					10	
- Peak					20	
Base Current	I _B	0.5				A _{dc}
Total Device Dissipation @ T _c = 25°C	P _D	125				Watts
Derate above 25°C		1				W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1	°C/W

FIGURE 1 - POWER DERATING



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

**CASE 340-01
 (TO-218AC)**

NPN-BDV65A, B, C
PNP-BDV64A, B, C

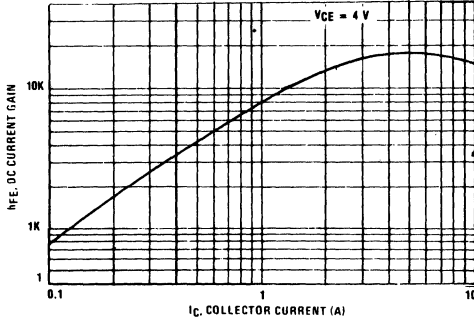
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 30 \text{ mAdc}$, $I_B = 0$)	BDV65 -BDV64 BDV65A-BDV64A BDV65B-BDV64B BDV65C-BDV64C	$V_{CE0} \text{ (sus)}$	60 80 100 120	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 50 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 60 \text{ Vdc}$, $I_B = 0$)	BDV65 -BDV64 BDV65A-BDV64A BDV65B-BDV64B BDV65C-BDV64C	I_{CEO}	1 1 1 1	mAdc
Collector Cutoff Current ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 120 \text{ Vdc}$, $I_E = 0$)	BDV65 -BDV64 BDV65A-BDV64A BDV65B-BDV64B BDV65C-BDV64C	I_{CBO}	.4 .4 .4 .4	mAdc
Collector Cutoff Current ($V_{CB} = 30 \text{ Vdc}$, $I_E = 0$, $T_C = 150^\circ\text{C}$) ($V_{CB} = 40 \text{ Vdc}$, $I_E = 0$, $T_C = 150^\circ\text{C}$) ($V_{CB} = 50 \text{ Vdc}$, $I_E = 0$, $T_C = 150^\circ\text{C}$) ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$, $T_C = 150^\circ\text{C}$)	BDV65 -BDV64 BDV65A-BDV64A BDV65B-BDV64B BDV65C-BDV64C	I_{CBO}	2 2 2 2	mAdc
Emitter Cutoff Current ($V_{BE} = 5 \text{ Vdc}$, $I_C = 0$)		I_{EBO}	5	mAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 5 \text{ Adc}$, $V_{CE} = 4 \text{ Vdc}$)		HFE	1000	
Collector-Emitter Saturation Voltage ($I_C = 5 \text{ Adc}$, $I_B = 0.02 \text{ Adc}$)		$V_{CE} \text{ (sat)}$	2	Vdc
Base-Emitter Saturation Voltage ($I_C = 5 \text{ Adc}$, $V_{CE} = 4 \text{ Vdc}$)		$V_{BE} \text{ (on)}$	2.5	Vdc

BDV65, BDV65A, BDV65B NPN
BDV64, BDV64A, BDV64B PNP

NPN

FIGURE 2 - DC CURRENT GAIN



PNP

FIGURE 3 - DC CURRENT GAIN

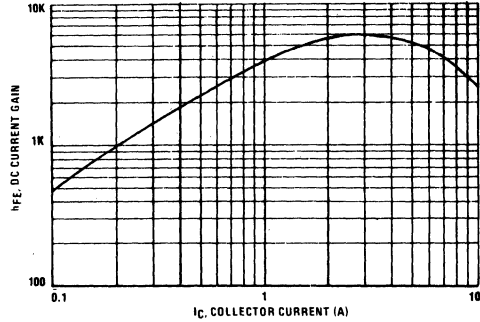


FIGURE 4 - "ON" VOLTAGES

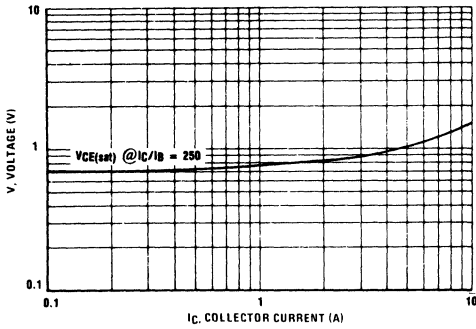


FIGURE 5 - "ON" VOLTAGES

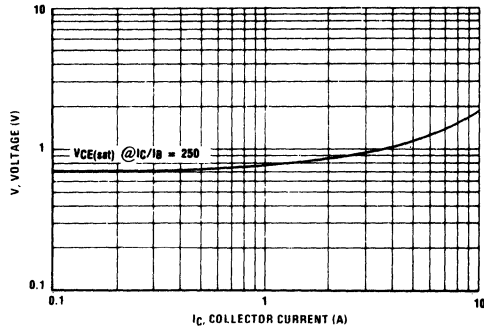
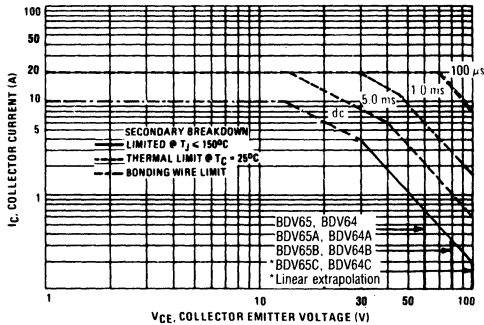


FIGURE 6 - ACTIVE REGION SAFE OPERATING AREA

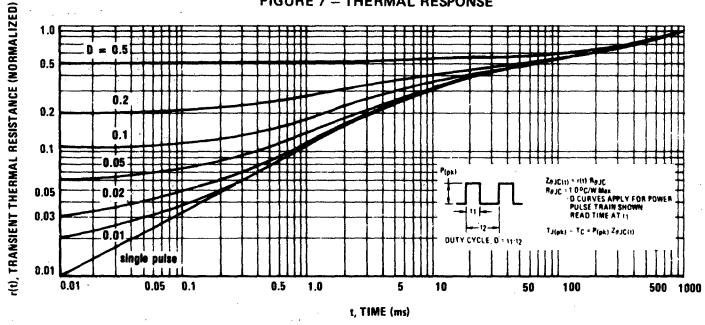


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 6 is based on $T_{J(pk)} = 150^\circ C$, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ C$. $T_{J(pk)}$ may be calculated from the data in figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN 415A)

BDV65, BDV65A, BDV65B NPN
BDV64, BDV64A, BDV64B PNP

FIGURE 7 – THERMAL RESPONSE



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

**NPN
BDW39
thru
BDW43**

**PNP
BDW44
thru
BDW48**

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for general purpose and low speed switching applications.

- High DC Current Gain – $h_{FE} = 2500$ (typ.) @ $I_C = 5.0$ Adc.

- Collector Emitter Sustaining Voltage @ 30 mAdc:

$V_{CE(sus)} =$ 45 Vdc (min.) – BDW39/BDW44
60 Vdc (min.) – BDW40/BDW45
80 Vdc (min.) – BDW41/BDW46
100 Vdc (min.) – BDW42/BDW47
120 Vdc (min.) – BDW43/BDW48

- Low Collector Emitter Saturation Voltage:

$V_{CE(sat)} =$ 2.0 Vdc (max.) @ $I_C = 5.0$ Adc
3.0 Vdc (max.) @ $I_C = 10.0$ Adc

- Monolithic Construction with Built-In Base Emitter Shunt resistors
- TO-220AB Compact Package
- TO-66 Lead form also available ordered with "-66" suffix.

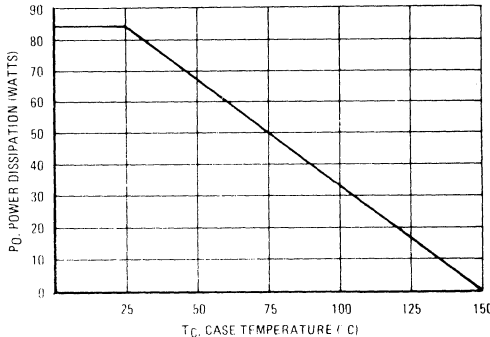
MAXIMUM RATINGS

Rating	Symbol	BDW39 BDW44	BDW40 BDW45	BDW41 BDW46	BDW42 BDW47	BDW43 BDW48	Unit
Collector-Emitter Voltage	V_{CE0}	45	60	80	100	120	V _{dc}
Collector-Base Voltage	V_{CB}	45	60	80	100	120	V _{dc}
Emitter-Base Voltage	V_{EB}	5.0					V _{dc}
Collector Current – Continuous	I_C	15					A _{dc}
Base Current	I_B	0.5					A _{dc}
Total Device Dissipation (@ $T_C = 25$ C Derate above 25 C	P_D	85			0.68		Watts W/C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to + 150					°C

THERMAL CHARACTERISTICS

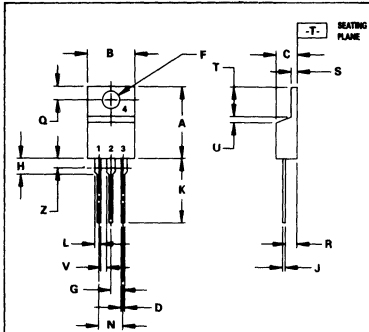
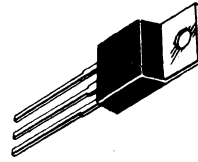
Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.47	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING CURVE



DARLINGTON 15 AMPERE

COMPLEMENTARY SILICON
POWER TRANSISTORS
45-60-80-100-120 VOLTS
85 WATTS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.29	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.86	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.029
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.60	1.27	0.020	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:
PN: 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

**BDW39, BDW40, BDW41, BDW42, BDW43 NPN
BDW44, BDW45, BDW46, BDW47, BDW48 PNP**

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Collector Emitter Sustaining Voltage ¹ ($I_C = 30 \text{ mAdc}, I_B = 0$)	$V_{CE(sus)}$	45 60 80 100 120		Vdc
Collector Cutoff Current ($V_{CE} = 22.5 \text{ Vdc}, I_B = 0$) ($V_{CE} = 30 \text{ Vdc}, I_B = 0$) ($V_{CE} = 40 \text{ Vdc}, I_B = 0$) ($V_{CE} = 50 \text{ Vdc}, I_B = 0$) ($V_{CE} = 60 \text{ Vdc}, I_B = 0$)	I_{CEO}		2 2 2 2 2	mAdc
Collector Cutoff Current ($V_{CB} = 45 \text{ Vdc}, I_E = 0$) ($V_{CB} = 60 \text{ Vdc}, I_E = 0$) ($V_{CB} = 80 \text{ Vdc}, I_E = 0$) ($V_{CB} = 100 \text{ Vdc}, I_E = 0$) ($V_{CB} = 120 \text{ Vdc}, I_E = 0$)	I_{CBO}		1 1 1 1 1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)	I_{EBO}		2	mAdc
ON CHARACTERISTICS¹				
DC Current Gain ($I_C = 5 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 10 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$) for all except BDW43/48 for BDW 43/48	h_{FE}	1000 250		250
Collector-Emitter Saturation Voltage ($I_C = 5 \text{ Adc}, I_B = 10 \text{ mAdc}$) ($I_C = 10 \text{ Adc}, I_B = 50 \text{ mAdc}$)	$V_{CE(sat)}$		2 3	Vdc
Base-Emitter On Voltage ($I_C = 10 \text{ Adc}, V_{CE} = 4 \text{ Vdc}$)	$V_{BE(on)}$		3	Vdc
SECOND BREAKDOWN²				
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$			Adc
BDW39/BDW40/BDW41/BDW42/BDW43	$\left\{ \begin{array}{l} V_{CE} = 28.4 \text{ Vdc} \\ V_{CE} = 40 \text{ Vdc} \\ V_{CE} = 22.5 \text{ Vdc} \\ V_{CE} = 36 \text{ Vdc} \end{array} \right.$	3 1.2 3.8 1.2		
BDW44/BDW45/BDW46/BDW47/BDW48				
DYNAMIC CHARACTERISTICS				
Magnitude of common emitter small signal short circuit current transfer ratio ($I_C = 3.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}, f = 1.0 \text{ MHz}$)	f_T	4.0		MHz
Output capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz}$) BDW39/BDW40/BDW41/BDW42/BDW43 BDW44/BDW45/BDW46/BDW47/BDW48	C_{ob}		200 300	PF
Small signal current gain $I_C = 3.0 \text{ Adc}, V_{CE} = 3.0 \text{ Vdc}, f = 1.0 \text{ kHz}$	h_{fe}	300		

Indicates JEDEC Registered Data.

¹ Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2.0 %.

² Pulse Test non repetitive: Pulse Width = 250 ms.

BDW39, BDW40, BDW41, BDW42, BDW43 NPN BDW44, BDW45, BDW46, BDW47, BDW48 PNP

FIGURE 2 - SWITCHING TIMES TEST CIRCUIT

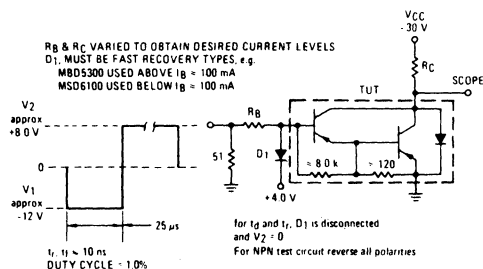


FIGURE 3 - SWITCHING TIMES

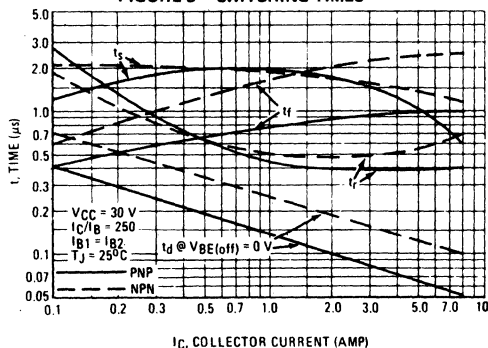
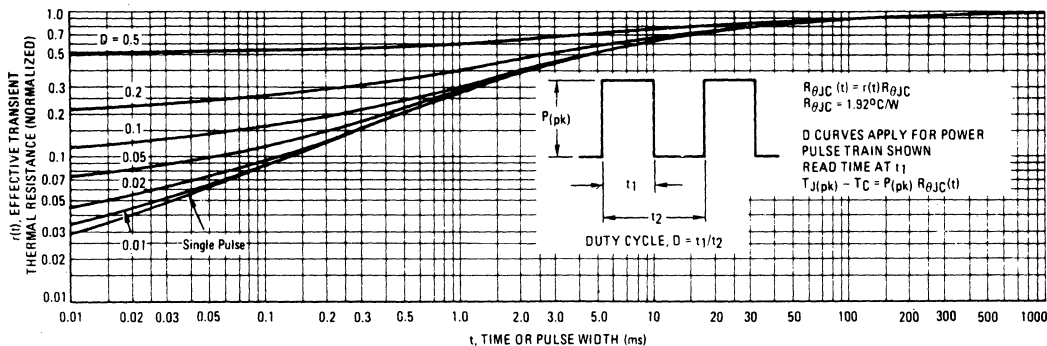


FIGURE 4 - THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 - BDW39 THRU BDW43

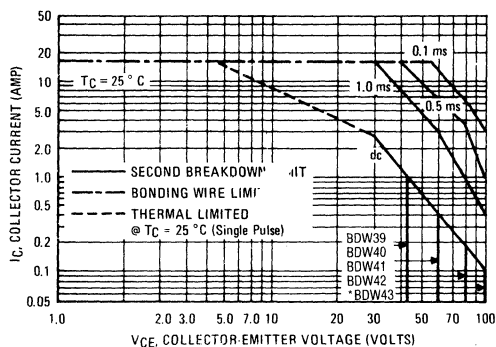
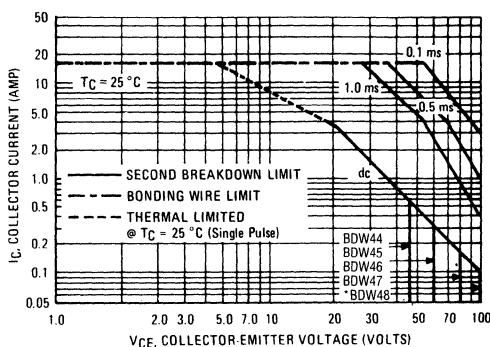


FIGURE 6 - BDW44 THRU BDW48



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Fig. 5 and 6 is based on $T_{J(pk)} =$

200°C ; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Fig. 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See an-415).

*Linear extrapolation

**BDW39, BDW40, BDW41, BDW42, BDW43 NPN
BDW44, BDW45, BDW46, BDW47, BDW48 PNP**

FIGURE 7 - SMALL-SIGNAL CURRENT GAIN

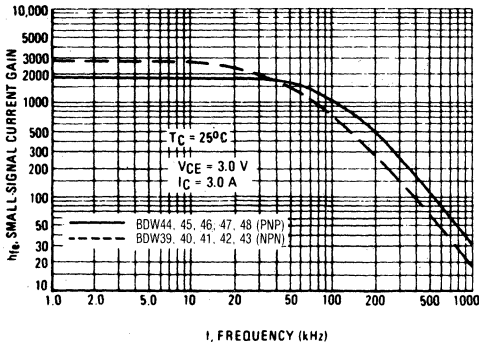
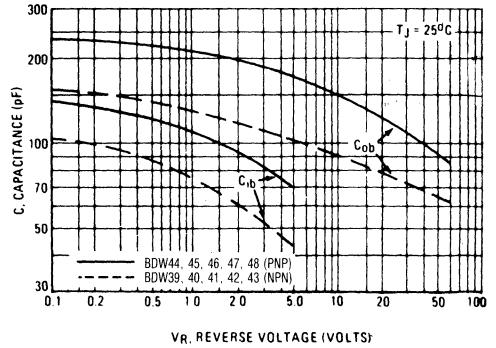


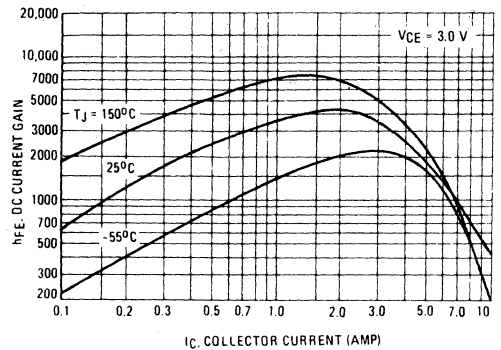
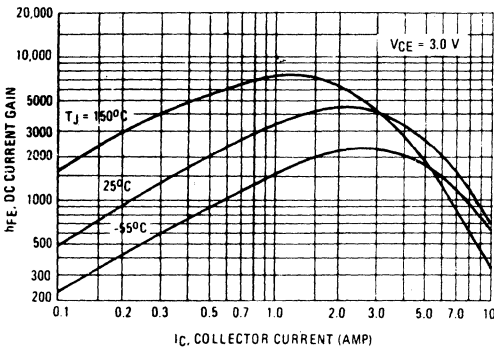
FIGURE 8 - CAPACITANCE



BDW39, 40, 41, 42, 43 (NPN)

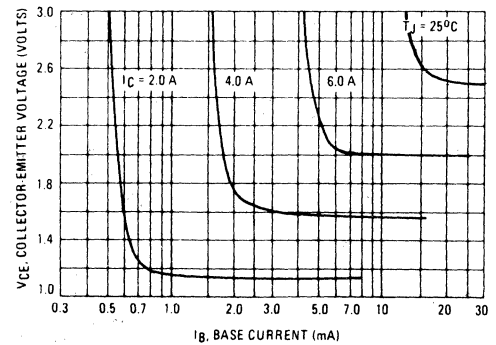
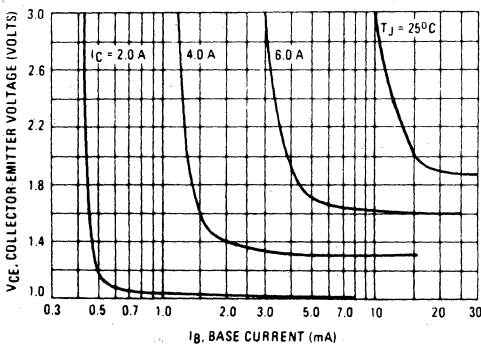
BDW44, 45, 46, 47, 48 (PNP)

FIGURE 9 - DC CURRENT GAIN



3

FIGURE 10 - COLLECTOR SATURATION REGION



**BDW39, BDW40, BDW41, BDW42, BDW43 NPN
BDW44, BDW45, BDW46, BDW47, BDW48 PNP**

BDW39, 40, 41, 42, 43 (NPN)

BDW44, 45, 46, 47, 48 (PNP)

FIGURE 11 – "ON" VOLTAGES

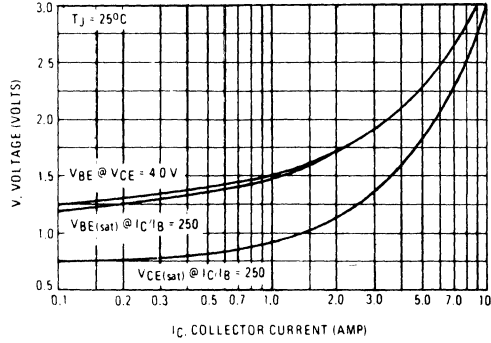
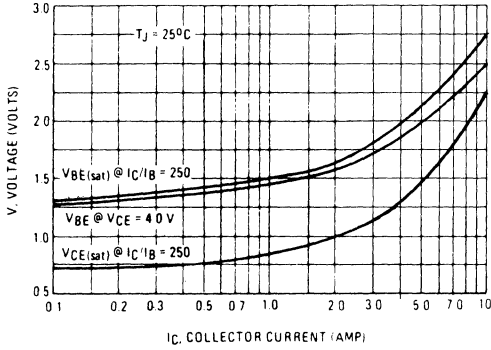


FIGURE 12 – TEMPERATURE COEFFICIENTS

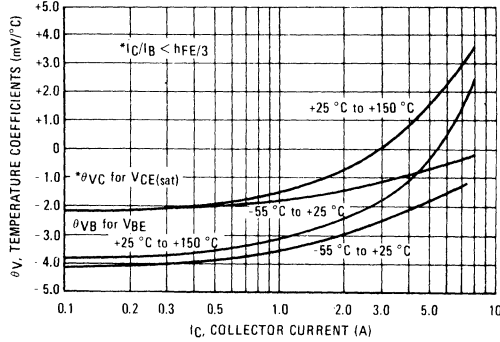
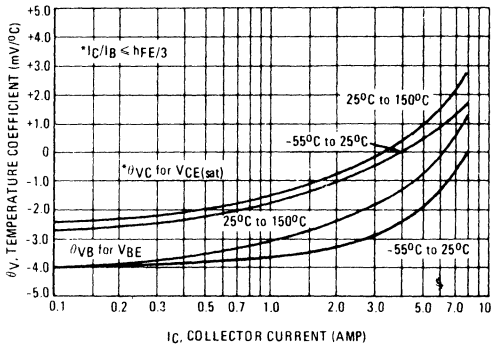
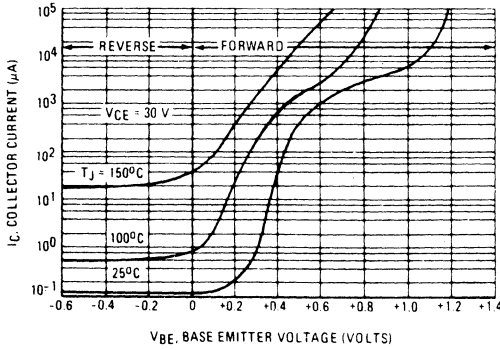
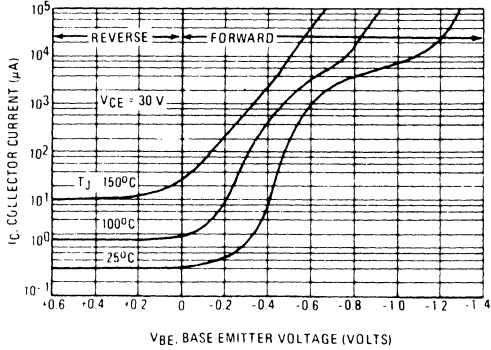
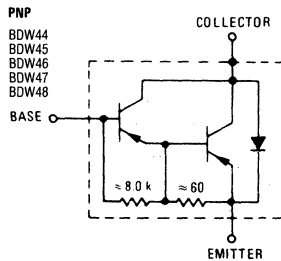
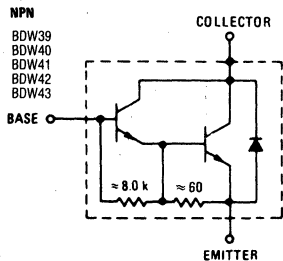


FIGURE 13 – COLLECTOR CUT-OFF REGION



BDW39, BDW40, BDW41, BDW42, BDW43 NPN
BDW44, BDW45, BDW46, BDW47, BDW48 PNP

FIGURE 14 – DARLINGTON SCHEMATIC



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for general purpose and low speed switching applications.

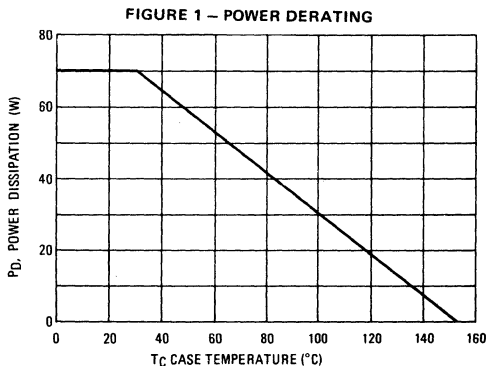
- High DC Current Gain - $h_{FE} = 2500$ (typ.) at $I_C = 4.0$ Adc
- Collector-Emitter Sustaining Voltage at 100 mAdc
 $V_{CE(sus)} = 45$ Vdc (min.) - BDX33, 34
 60 Vdc (min.) - BDX33A, 34A
 80 Vdc (min.) - BDX33B, 34B
 100 Vdc (min.) - BDX33C, 34C
- Low Collector-Emitter Saturation Voltage
 $V_{CE(sat)} = 2.5$ Vdc (max.) at $I_C = 4.0$ Adc - BDX33, 33A/34, 34A
 2.5 Vdc (max.) at $I_C = 3.0$ Adc - BDX33B, 33C/34B, 34C
- Monolithic Construction with Built-In Base-Emitter Shunt resistors
- TO-220AB Compact Package
- TO-66 Lead form also available ordered with "-66" suffix.

MAXIMUM RATINGS

Rating	Symbol	BDX33 BDX34	BDX33A BDX34A	BDX33B BDX34B	BDX33C BDX34C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous Peak	I_C	10 15				Adc
Base Current	I_B	0.25				Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	70 0.56				Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_{J}, T_{stg}	-65 to +150				$^\circ\text{C}$

THERMAL CHARACTERISTICS

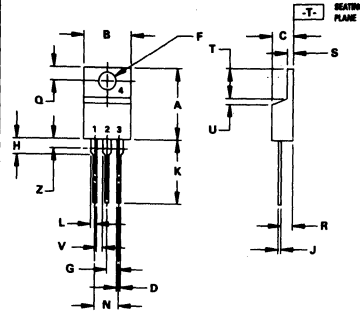
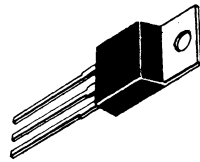
Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.78	$^\circ\text{C}/\text{W}$



NPN
BDX33
BDX33A
BDX33B
BDX33C

PNP
BDX34
BDX34A
BDX34B
BDX34C

**DARLINGTON
10 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
45-60-80-100 VOLTS
70 Watts**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.40	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.38	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

**CASE 221A-04
TO-220AB**

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

BDX33, BDX33A, BDX33B, BDX33C NPN
BDX34, BDX34A, BDX34B, BDX34C PNP

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ¹ (I _C = 100 mA _{dc} , I _B = 0)	BDX33/BDX34 BDX33A/BDX34A BDX33B/BDX34B BDX33C/BDX34C	V _{CEO(sus)}	45 60 80 100	V _{dc}
Collector-Emitter Sustaining Voltage ¹ (I _C = 100 mA _{dc} , I _B = 0, R _{BE} = 100)	BDX33/BDX34 BDX33A/BDX34A BDX33B/BDX34B BDX33C/BDX34C	V _{CER(sus)}	45 60 80 100	V _{dc}
Collector-Emitter Sustaining Voltage ¹ (I _C = 100 mA _{dc} , I _B = 0, V _{BE} = 1.5 V _{dc})	BDX33/BDX34 BDX33A/BDX34A BDX33B/BDX34B BDX33C/BDX34C	V _{CEx(sus)}	45 60 80 100	V _{dc}
Collector Cutoff Current (V _{CE} = ½ rated V _{CEO} , I _B = 0)	T _C = 25 °C T _C = 100 °C	I _{CEO}	0.5 10	mA _{dc}
Collector Cutoff Current (V _{CB} = rated V _{CB0} , I _E = 0)	T _C = 25 °C T _C = 100 °C	I _{CBO}	1 5	mA _{dc}
Emitter Cutoff Current (V _{BE} = 5.0 V _{dc} , I _C = 0)		I _{EBO}	10	mA _{dc}
ON CHARACTERISTICS				
DC Current Gain ¹ (I _C = 4.0 Adc, V _{CE} = 3.0 V _{dc}) (I _C = 3.0 Adc, V _{CE} = 3.0 V _{dc})	BDX33, 33A/34, 34A BDX33B, 33C/34B, 34C	h _{FE}	750 750	—
Collector-Emitter Saturation Voltage (I _C = 4.0 Adc, I _B = 8 mA _{dc}) (I _C = 3.0 Adc, I _B = 6 mA _{dc})	BDX33, 33A/34, 34A BDX33B, 33C/34B, 34C	V _{CE(sat)}	2.5 2.5	V _{dc}
Base-Emitter On Voltage (I _C = 4.0 Adc, V _{CE} = 3 V) (I _C = 3.0 Adc, V _{CE} = 3 V _{dc})	BDX33, 33A/34, 34A BDX33B, 33C/34B, 34C	V _{BE(on)}	2.5 2.5	V _{dc}
Diode Forward Voltage (I _C = 8 Adc)		V _F	4	V _{dc}
SECOND BREAKDOWN²				
Second Breakdown Collector Current With Base Forward Biased (V _{CE} = 25 V _{dc}) (V _{CE} = 20 V _{dc}) (V _{CE} = 36 V _{dc}) (V _{CE} = 33 V _{dc})	BDX33 Series BDX34 Series BDX33 Series BDX34 Series	I _{S/b}	2.8 3.5 1.0 1.0	Adc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (T _C = 1.0 Adc, V _{CE} = 5.0 V _{dc} , f = 1 MHz)		h _{FE}	1000	—
Current Gain-Bandwidth product (I _C = 1.0 Adc, V _{CE} = 5.0 V _{dc} , f = 1.0 MHz)		f _T	3	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 0.1 MHz)	BDX33 Series BDX34 Series	C _{ob}	200 300	pF

¹ Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2%

² Pulse Test non repetitive: Pulse Width = 0.25 s.

BDX33, BDX33A, BDX33B, BDX33C NPN
BDX34, BDX34A, BDX34B, BDX34C PNP

FIGURE 2 – THERMAL RESPONSE

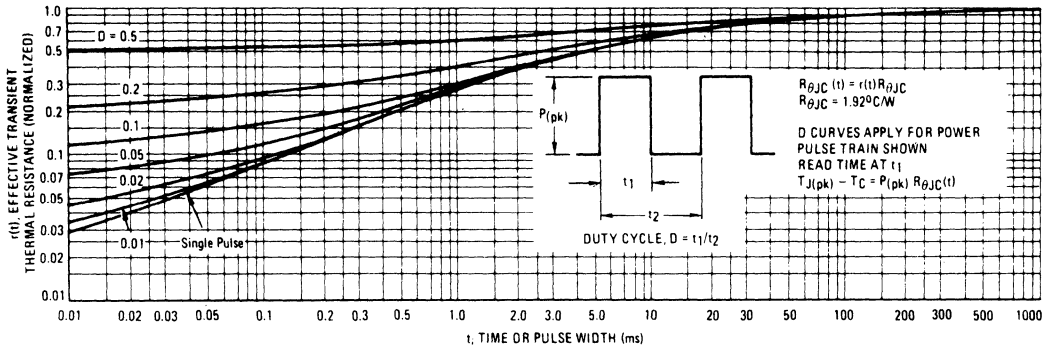
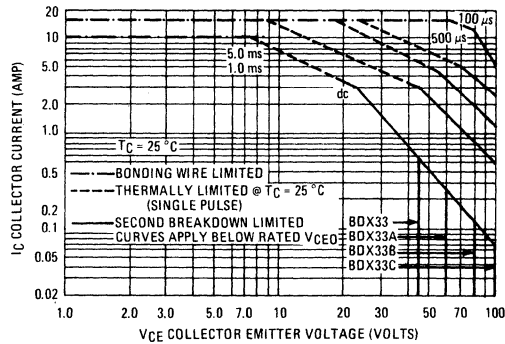
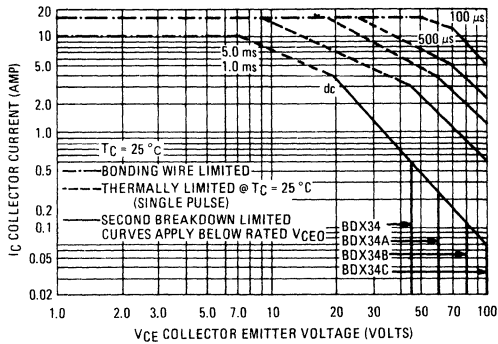


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Fig. 3 is based on $T_{J(pk)} = 150^\circ\text{C}$;

T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Fig. 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (see AN-415A).

FIGURE 4 – SMALL-SIGNAL CURRENT GAIN

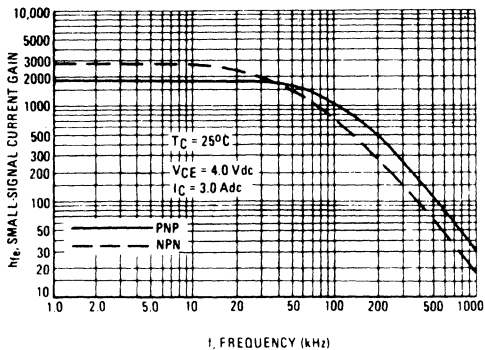
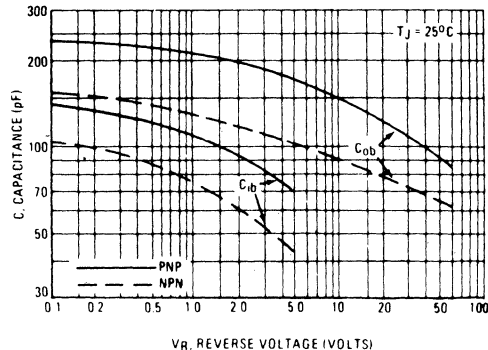


FIGURE 5 – CAPACITANCE



BDX33, BDX33A, BDX33B, BDX33C NPN
BDX34, BDX34A, BDX34B, BDX34C PNP

NPN
BDX33, 33A, 33B, 33C

PNP
BDX34, 34A, 34B, 34C

FIGURE 6 – DC CURRENT GAIN

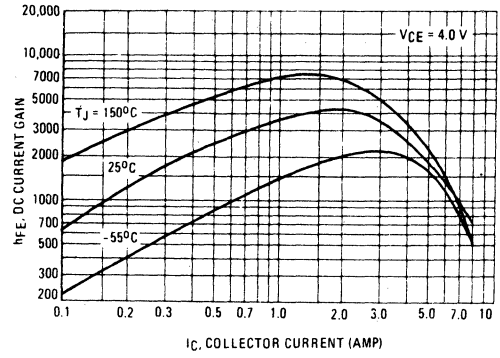
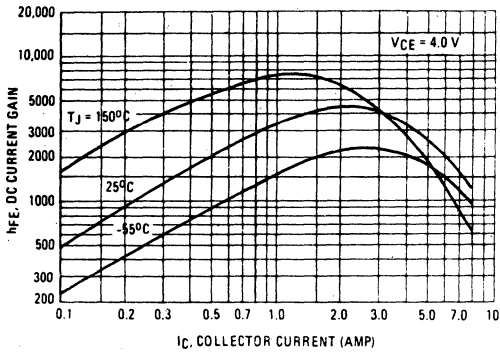


FIGURE 7 – COLLECTOR SATURATION REGION

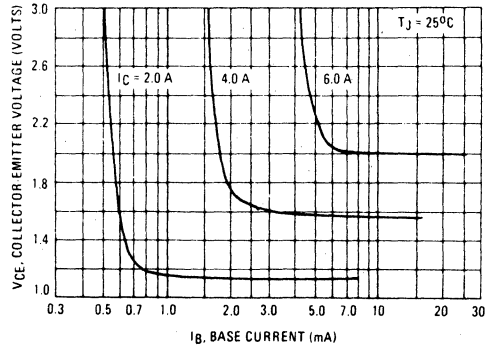
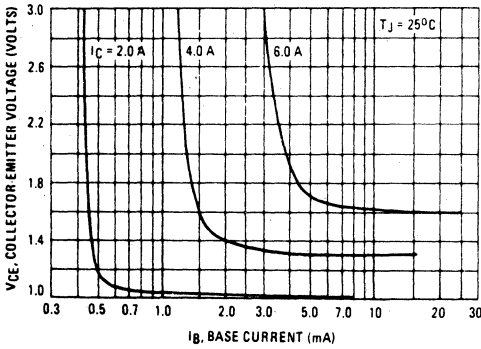
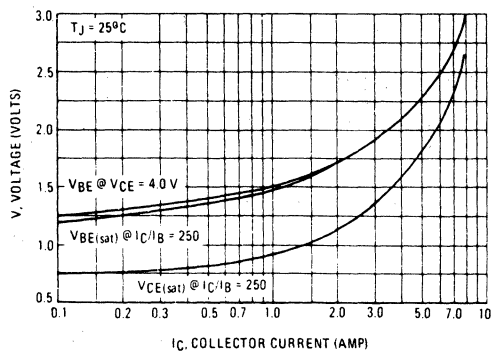
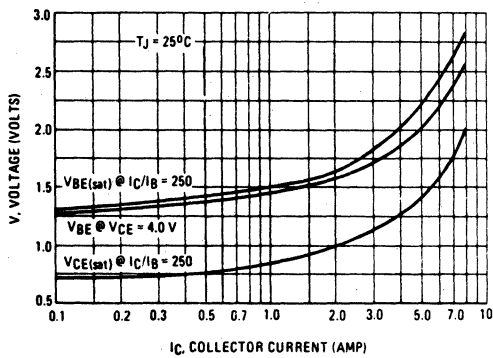


FIGURE 8 – "ON" VOLTAGES



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

**NPN
BDX53
BDX53A
BDX53B
BDX53C**

**PNP
BDX54
BDX54A
BDX54B
BDX54C**

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain —
 $h_{FE} = 2500$ (Typ) @ $I_C = 4.0$ Adc
- Collector-Emitter Sustaining Voltage — @ 100 mAdc
 $V_{CE(sus)} = 45$ Vdc (Min) — BDX53, 54
 $= 60$ Vdc (Min) — BDX53A, 54A
 $= 80$ Vdc (Min) — BDX53B, 54B
 $= 100$ Vdc (Min) — BDX53C, 54C
- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 2.0$ Vdc (Max) @ $I_C = 3.0$ Adc
 $= 4.0$ Vdc (Max) @ $I_C = 5.0$ Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package

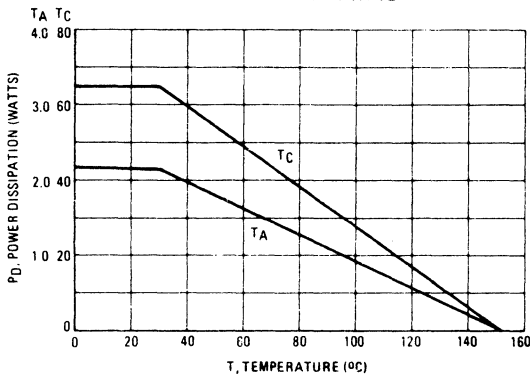
*MAXIMUM RATINGS

Rating	Symbol	BDX53 BDX54	BDX53A BDX54A	BDX53B BDX54B	BDX53C BDX54C	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	8				Adc
		12				
Base Current	I_B	0.2				Adc
Total Device Dissipation	P_D	60				Watts
		@ $T_C = 25^\circ\text{C}$ Derate above 25°C				
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				$^\circ\text{C}$

THERMAL CHARACTERISTICS

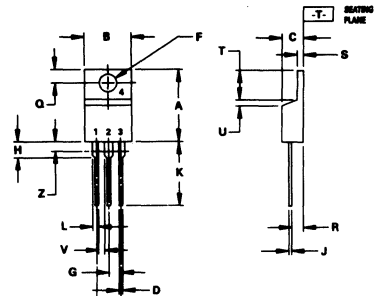
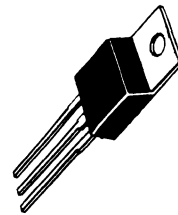
Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	$^\circ\text{C}/\text{W}$

FIGURE 1 — POWER DERATING



DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80-100 VOLTS
65 WATTS



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	5.88	10.28	0.230	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.81	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.48	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

BDX53, 53A, 53B, 53C NPN BDX54, 54A, 54B, 54C PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 100 mA, I _B = 0)	BDX53, BDX54 BDX53A, BDX54A BDX53B, BDX54B BDX53C, BDX54C	V _{CEO(sus)}	45 60 80 100	V _{dc}
Collector Cutoff Current (V _{CE} = 22 Vdc, I _B = 0) (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 40 Vdc, I _B = 0) (V _{CE} = 50 Vdc, I _B = 0)	BDX53, BDX54 BDX53A, BDX54A BDX53B, BDX54B BDX53C, BDX54C	I _{CEO}	— — — —	0.5 0.5 0.5 0.5 mA
Collector Cutoff Current (V _{CB} = 45 Vdc, I _E = 0) (V _{CB} = 60 Vdc, I _E = 0) (V _{CB} = 80 Vdc, I _E = 0) (V _{CB} = 100 Vdc, I _E = 0)	BDX53, BDX54 BDX53A, BDX54A BDX53B, BDX54B BDX53C, BDX54C	I _{CBO}	— — — —	0.2 0.2 0.2 0.2 mA
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)		I _{EBO}	—	2.0 mA
ON CHARACTERISTICS (1)				
DC Current Gain (I _C = 3.0 A, V _{CE} = 3.0 Vdc)		h _{FE}	750	—
Collector-Emitter Saturation Voltage (I _C = 3.0 A, I _B = 12 mA)		V _{CE(sat)}	— —	2.0 4.0 V _{dc}
Base-Emitter Saturation Voltage (I _C = 3.0 A, I _B = 12 mA)		V _{BE(sat)}	—	2.5 V _{dc}
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I _C = 3.0 A, V _{CE} = 4.0 Vdc, f = 1.0 MHz)		h _{fe}	4.0	—
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	BDX53, 53A, 53B, 53C BDX54, 54A, 54B, 54C	C _{ob}	— —	300 200 pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

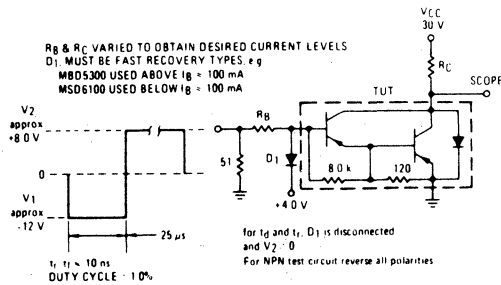
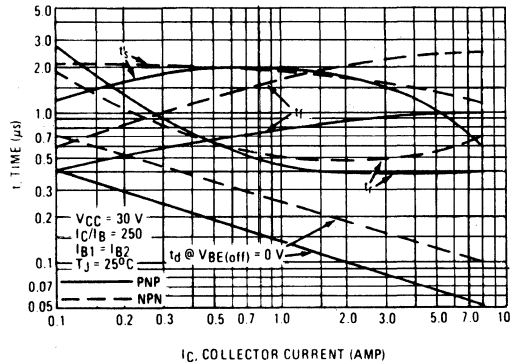


FIGURE 3 – SWITCHING TIMES



BDX53, 53A, 53B, 53C NPN
BDX54, 54A, 54B, 54C PNP

FIGURE 4 – THERMAL RESPONSE

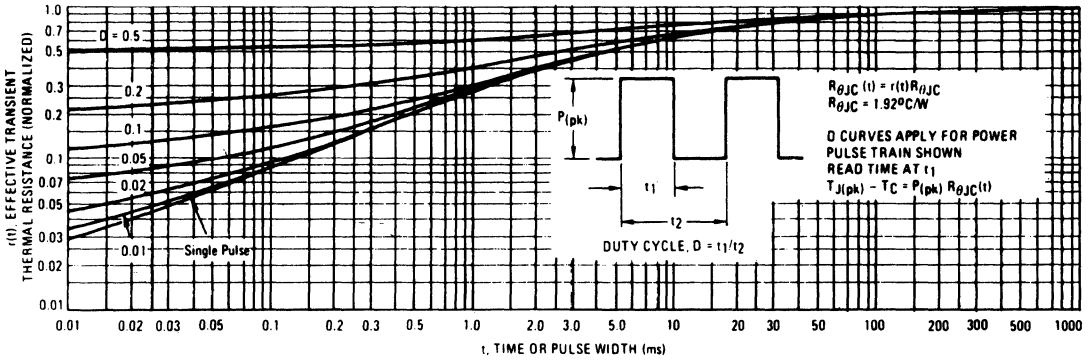
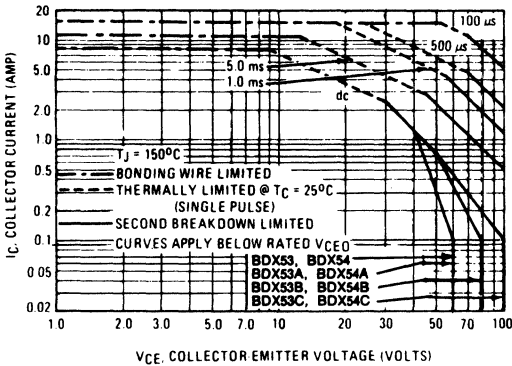


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (see AN-415A).

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

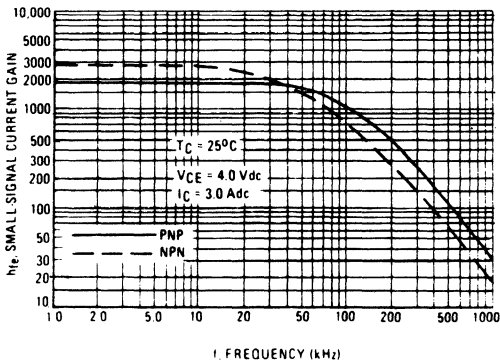
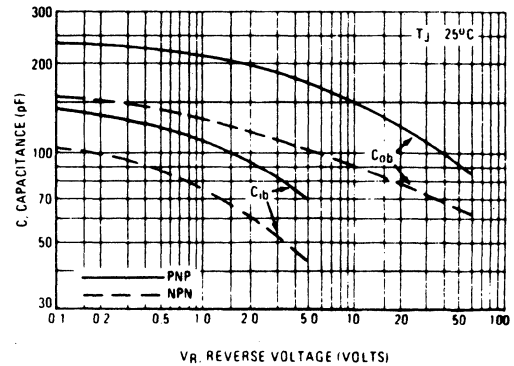


FIGURE 7 – CAPACITANCE



BDX53, 53A, 53B, 53C NPN
BDX54, 54A, 54B, 54C PNP

NPN
BDX53, BDX53A, BDX53B, BDX53C

PNP
BDX54, BDX54A, BDX54B, BDX54C

FIGURE 8 - DC CURRENT GAIN

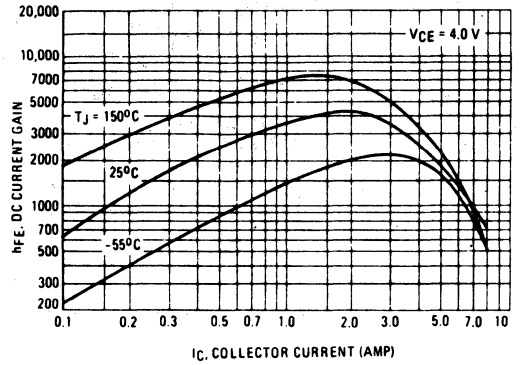
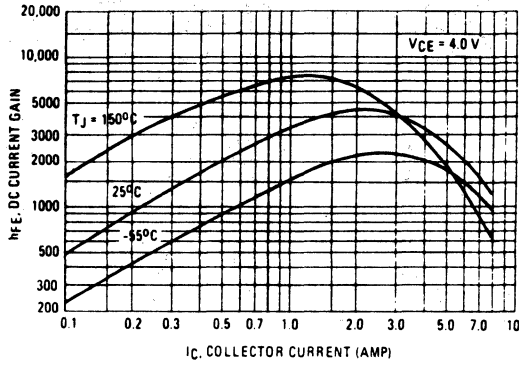
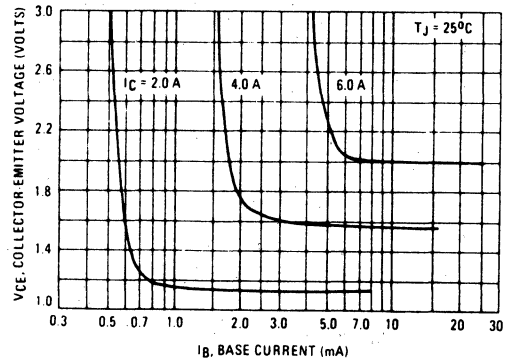
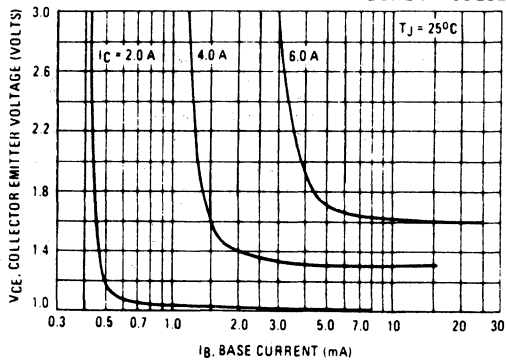
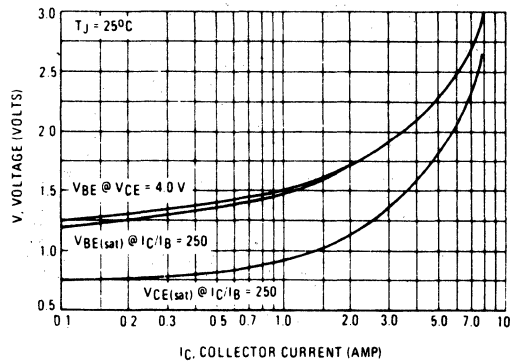
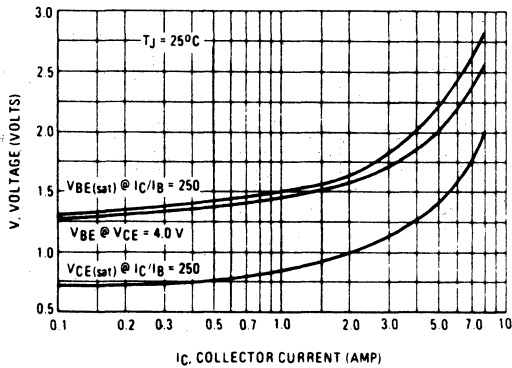


FIGURE 9 - COLLECTOR SATURATION REGION



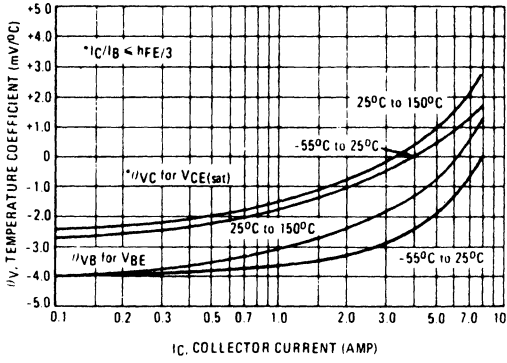
3

FIGURE 10 - "ON" VOLTAGES



BDX53, 53A, 53B, 53C NPN
BDX54, 54A, 54B, 54C PNP

NPN
BDX53, BDX53A, BDX53B, BDX53C



PNP
BDX54, BDX54A, BDX54B, BDX54C

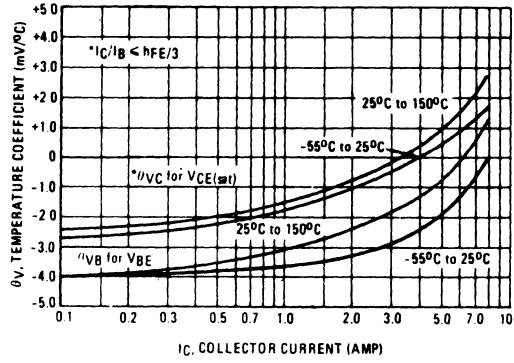


FIGURE 12 – COLLECTOR CUT-OFF REGION

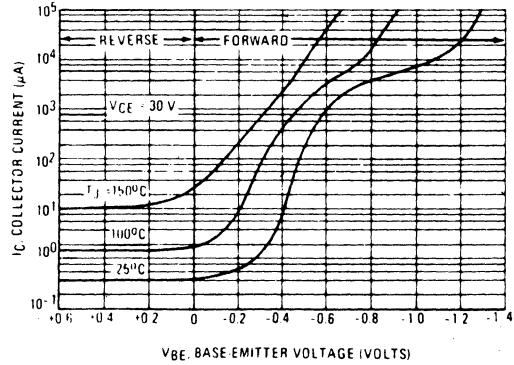
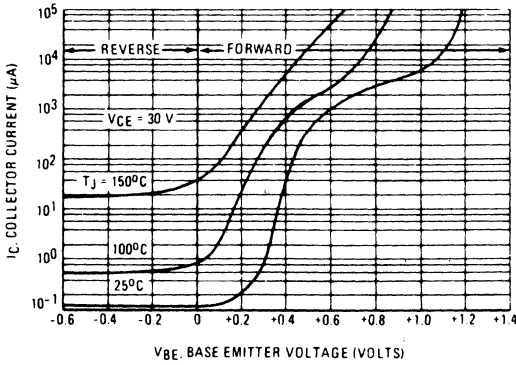
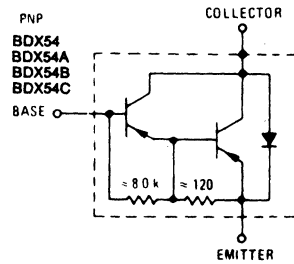
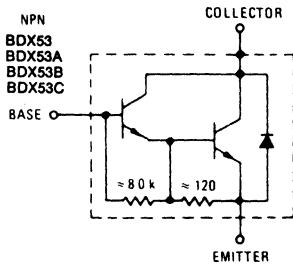


FIGURE 13 – DARLINGTON SCHEMATIC



BU204
BU205

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

... specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage – $V_{CEX} = 1300 \text{ Vdc} - \text{BU204}$
 $1500 \text{ Vdc} - \text{BU205}$
- Glassivated Base-Collector Junction
- Switching Times with Inductive Loads –
 $t_f = 0.65 \mu\text{s (Typ)} @ I_C = 2\text{A}$

2.5 AMPERE
NPN SILICON
POWER TRANSISTORS

1300 AND 1500 VOLTS
36 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

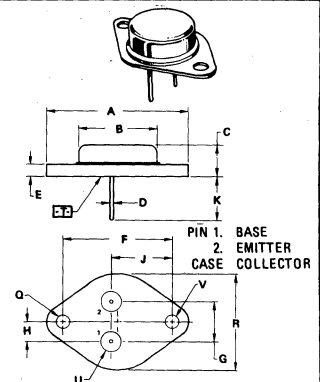
MAXIMUM RATINGS

Rating	Symbol	BU204	BU205	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	600	700	Vdc
Collector-Emitter Voltage	V_{CEX}	1300	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	2.5		Adc
– Peak (1)	I_{CM}	3		Adc
Base Current – Peak (1)	I_{BM}	2.5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	36		Watts
Derate above 25°C		10		$\text{W}/^\circ\text{C}$
@ $T_C = 90^\circ\text{C}$		0.4		$\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +115		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C}/\text{W}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D:

$\text{M} \pm 0.13 (0.005) \text{ T V } \text{M}$

FOR LEADS:

$\text{M} \pm 0.13 (0.005) \text{ T V } \text{M} \text{ M}$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.57	1.09	0.028	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.49 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-86

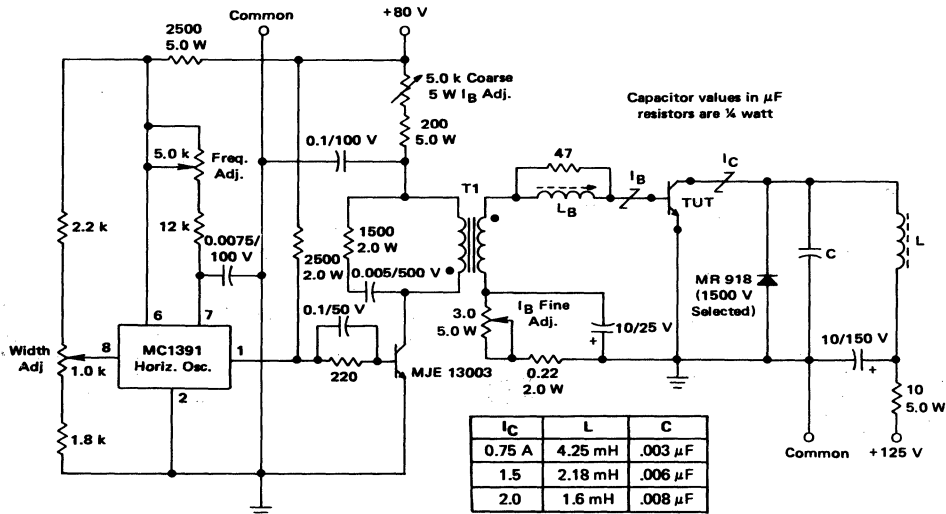
BU204, BU205

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage ($I_C = 100 \text{ mAdc}, I_B = 0$)	BU204 BU205	$V_{CEO(sus)}$	600 700	— —	Vdc
Collector Cutoff Current ($V_{CE} = 1300 \text{ Vdc}, V_{BE} = 0$) ($V_{CE} = 1500 \text{ Vdc}, V_{BE} = 0$)	BU204 BU205	I_{CES}	— —	1.0 1.0	mAdc
Emitter Base Voltage ($I_E = 10 \text{ mA}, I_C = 0$)		V_{EBO}	5.0	—	Vdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage ($I_C = 2.0 \text{ Adc}, I_B = 1.0 \text{ Adc}$)		$V_{CE(sat)}$	—	5.0	Vdc
Base Emitter Saturation Voltage ($I_C = 2.0 \text{ Adc}, I_B = 1.0 \text{ Adc}$)		$V_{BE(sat)}$	—	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased		$I_{S/B}$	See Figure 14		
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (1) ($I_C = 0.1 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}, f_{test} = 1.0 \text{ MHz}$)		f_T	—	4.0	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 1.0 \text{ MHz}$)		C_{ob}	—	50	pF
SWITCHING CHARACTERISTICS					
Fall Time ($I_C = 2.0 \text{ Adc}, I_{B1} = 1.0 \text{ Adc}, L_B = 25 \mu\text{H}$) (See Figure 1)		t_f	—	0.65	μs

(1) Pulse Test: Pulse Width < 300 μs , Duty Cycle = 2%.

FIGURE 1 — TEST CIRCUIT



DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminates "E" iron core. Primary Inductance — 39 mH. Secondary Inductance — 22 mH, Leakage Inductance with primary shorted — 2.0 μH , Primary 260 turns #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM} . Worst case component variations and maximum high voltage loading must also be taken into account.

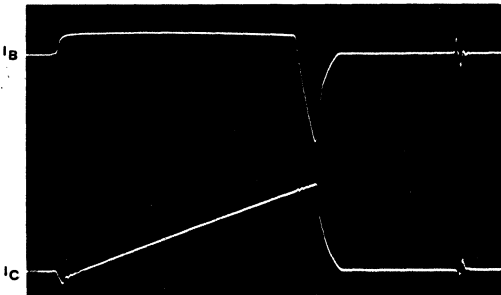
If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM} , I_{B1} , and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B , at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown

in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1} , and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1} h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM} . As L_B is increased, the curves become broader and flatter above the $I_{B1} h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE} , essentially moves the curves to the left or right according to the relation $I_{B1} h_{FE} = \text{constant}$. It then becomes obvious that, for a specified I_{CM} , an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1} . The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM} . These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

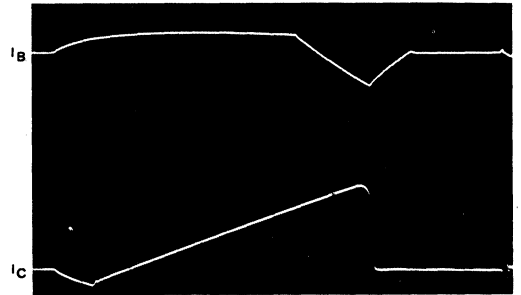
TEST CIRCUIT WAVEFORMS

FIGURE 2



(time)

FIGURE 3



(time)

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

3

FIGURE 4 – OPTIMIZING DRIVE @ $I_C = 0.75$ A

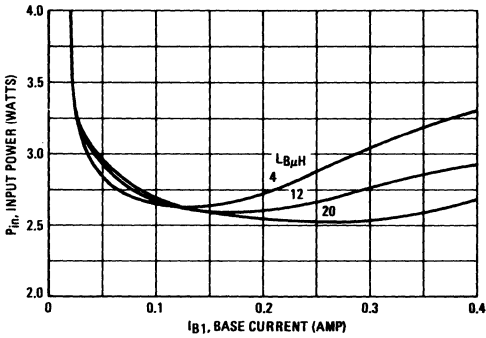


FIGURE 5 – OPTIMIZING DRIVE @ $I_C = 1.5$ A

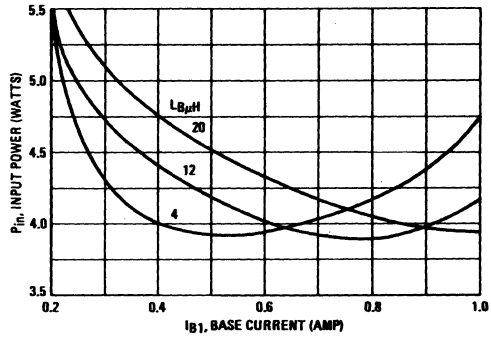


FIGURE 6 – OPTIMIZING DRIVE @ $I_C = 2.0$ A

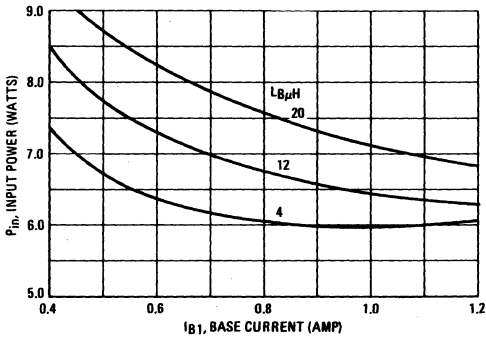


FIGURE 7 – SWITCHING BEHAVIOR versus TEMPERATURE

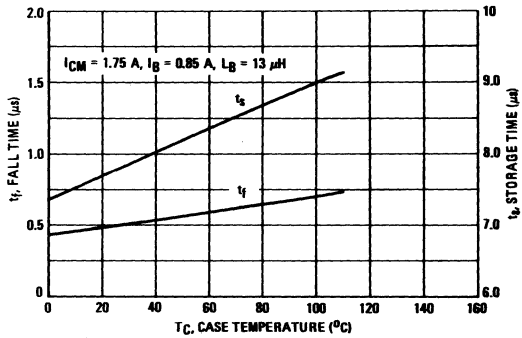


FIGURE 8 – OPTIMUM DRIVE CONDITIONS

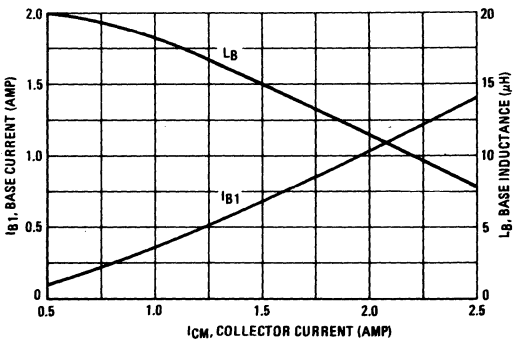


FIGURE 9 – SWITCHING BEHAVIOR versus I_{CM}

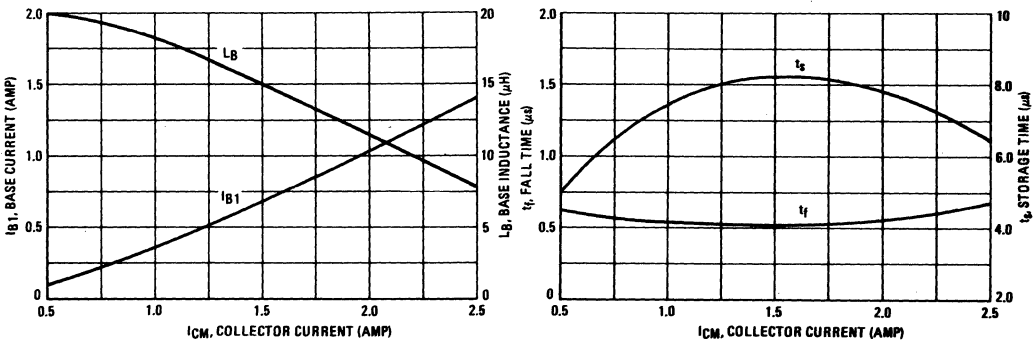


FIGURE 10 – THERMAL RESPONSE

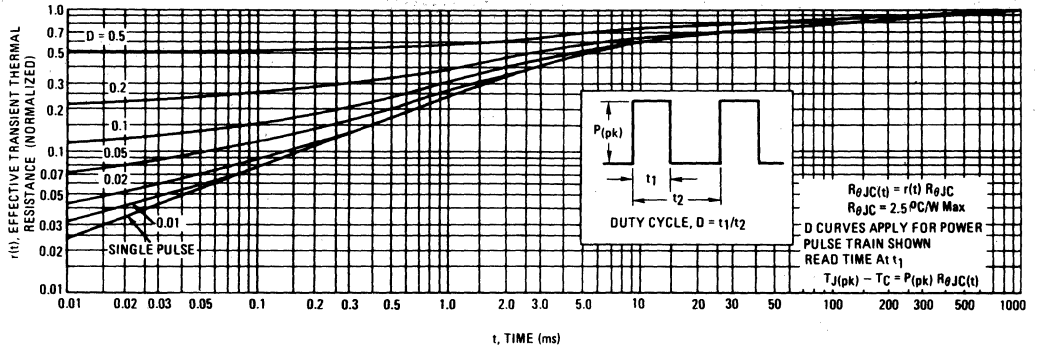


FIGURE 11 – COLLECTOR SATURATION REGION

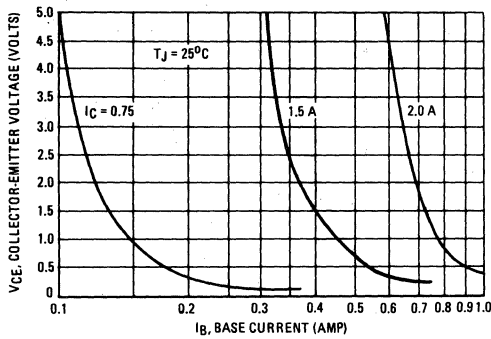


FIGURE 12 – DC CURRENT GAIN

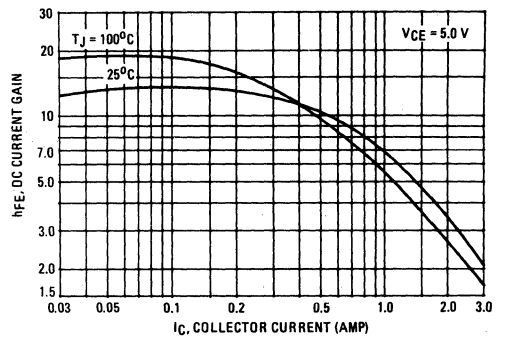


FIGURE 13 – "ON" VOLTAGES

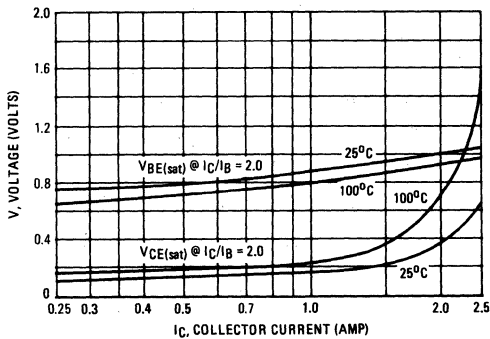
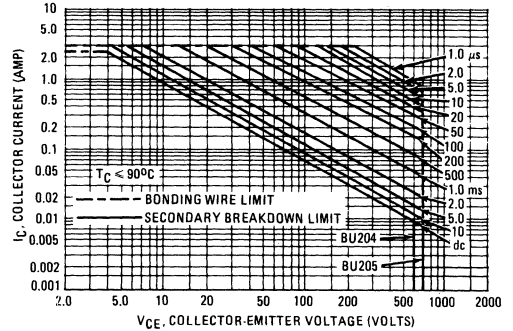


FIGURE 14 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA



BU207
BU208

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

... specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage –
 $V_{CEX} = 1300 \text{ Vdc} - \text{BU207}$
 $1500 \text{ Vdc} - \text{BU208}$
- Collector-Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 600 \text{ Vdc} - \text{BU207}$
 $700 \text{ Vdc} - \text{BU208}$
- Switching Times with Inductive Loads, $t_f = 0.4 \mu\text{s}$ (Typ) @
 $I_C = 4.5 \text{ A}$
- Optimum Drive Condition Curves
- Glass Base-Collector Junction

5 AMPERE
NPN SILICON
POWER TRANSISTORS
1300 AND 1500 VOLTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

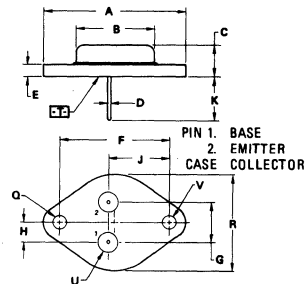
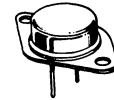
***MAXIMUM RATINGS**

Rating	Symbol	BU207	BU208	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	600	700	Vdc
Collector-Emitter Voltage	V_{CEX}	1300	1500	Vdc
Emitter Base Voltage	V_{EB}	5		Vdc
Collector Current – Continuous	I_C	5		Adc
Peak (1)	I_{CM}	7.5		
Base Current – Peak (1)	I_{BM}	4		Adc
Total Power Dissipation @ $T_C = 95^\circ\text{C}$ Derate above 95°C	P_D	12.5	0.625	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +115		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.6	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.



- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. [] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$\pm 0.13 (0.005) \text{ (M)} T \text{ (V)} \text{ (Q)}$

FOR LEADS:

$\pm 0.13 (0.005) \text{ (M)} T \text{ (V)} \text{ (Q)}$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	1.187 BSC		
G	10.92 BSC	0.430 BSC		
H	5.48 BSC	0.215 BSC		
J	16.89 BSC	0.665 BSC		
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	26.67	—	1.050	—
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

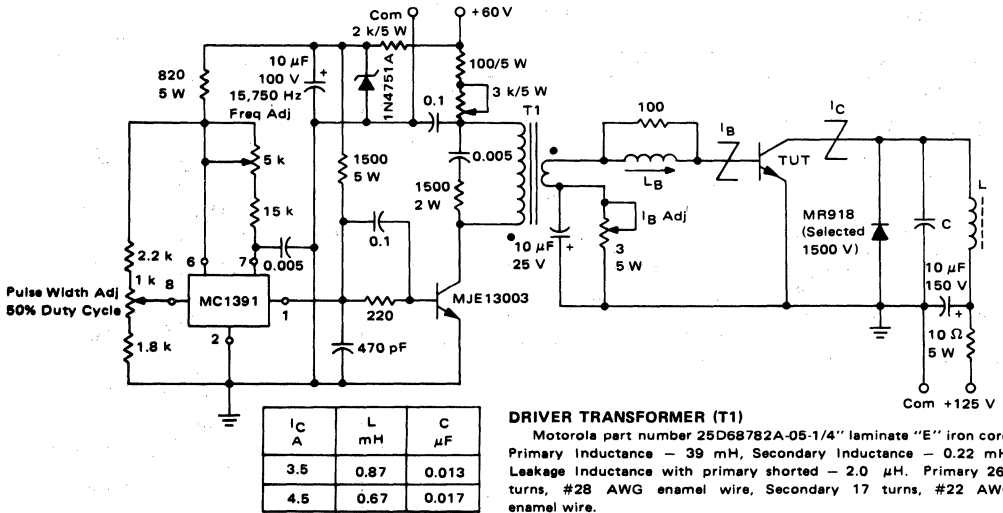
CASE 1-05

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage ($I_C = 100 \text{ mA}, I_B = 0$)	BU207 BU208 $V_{CE(sus)}$	600 700	— —	— —	Vdc
Collector Cutoff Current ($V_{CE} = 1300 \text{ Vdc}, V_{BE} = 0$) ($V_{CE} = 1500 \text{ Vdc}, V_{BE} = 0$)	BU207 BU208 I_{CES}	— —	— —	1.0 1.0	mAdc
Emitter Base Voltage ($I_E = 10 \text{ mA}, I_C = 0$)	V_{EBO}	5.0	—	—	Vdc
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 4.5 \text{ Adc}, V_{CE} = 5 \text{ Vdc}$)	h_{FE}	2.25	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 4.5 \text{ Adc}, I_B = 2 \text{ Adc}$)	$V_{CE(sat)}$	—	—	5	Vdc
Base Emitter Saturation Voltage ($I_C = 4.5 \text{ Adc}, I_B = 2 \text{ Adc}$)	$V_{BE(sat)}$	—	—	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14			
DYNAMIC CHARACTERISTICS					
Current-Gain - Bandwidth Product ($I_C = 0.1 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}, f_{test} = 1 \text{ MHz}$)	f_T	—	4.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz}$)	C_{ob}	—	125	—	pF
SWITCHING CHARACTERISTICS					
Fall Time ($I_C = 4.5 \text{ Adc}, I_B = 1.8 \text{ Adc}, L_B = 10 \mu\text{H}$, see Figure 1)	t_f	—	0.6	—	μs

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle \leq 2%.

FIGURE 1 - SWITCHING TIMES TEST CIRCUIT



BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM} . Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM} , I_{B1} , and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown

in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1} , and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1} h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM} . As L_B is increased, the curves become broader and flatter above the $I_{B1} h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor *initiation* of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE} , essentially moves the curves to the left or right according to the relation $I_{B1} h_{FE} = \text{constant}$. It then becomes obvious that, for a specified I_{CM} , an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1} . The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM} . These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

TEST CIRCUIT WAVEFORMS

FIGURE 2

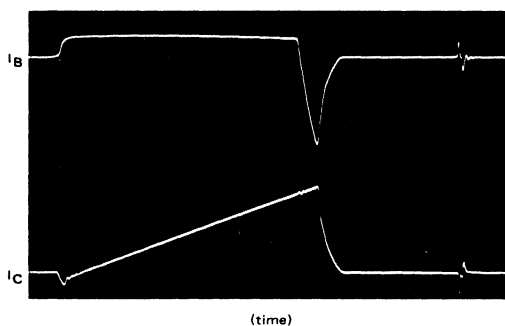
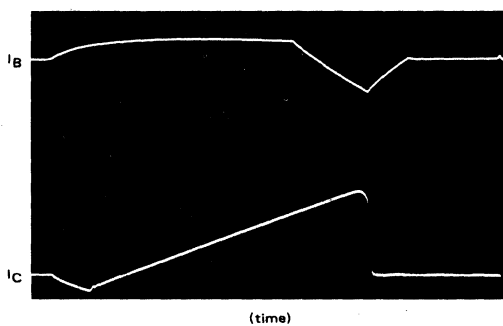


FIGURE 3



3

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 - OPTIMIZING DRIVE @ $I_C = 3.5 \text{ A}$

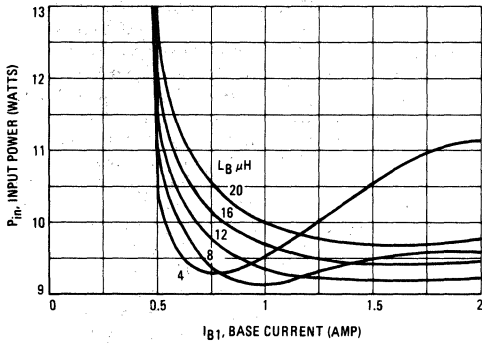


FIGURE 6 - SWITCHING BEHAVIOR versus TEMPERATURE
 $I_{CM} = 3.5 \text{ A}, I_B = 1.5 \text{ A}, L_B = 14 \mu\text{H}$

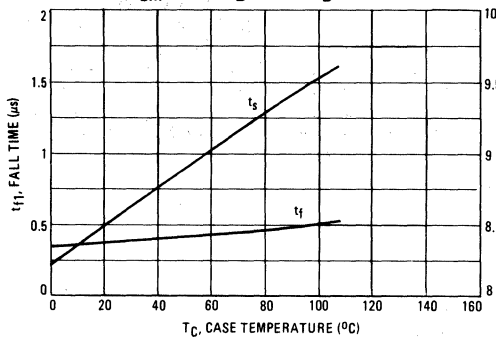


FIGURE 5 - OPTIMIZING DRIVE @ $I_C = 4.5 \text{ A}$

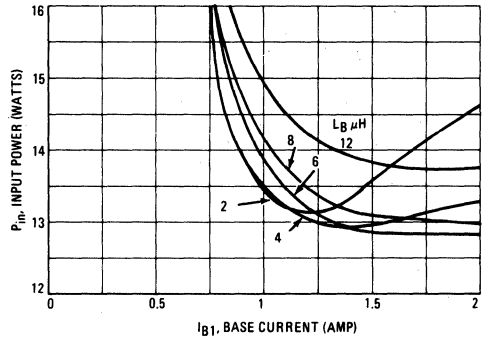


FIGURE 7 - SWITCHING BEHAVIOR versus TEMPERATURE
 $I_{CM} = 4.5 \text{ A}, I_B = 1.75 \text{ A}, L_B = 8 \mu\text{H}$

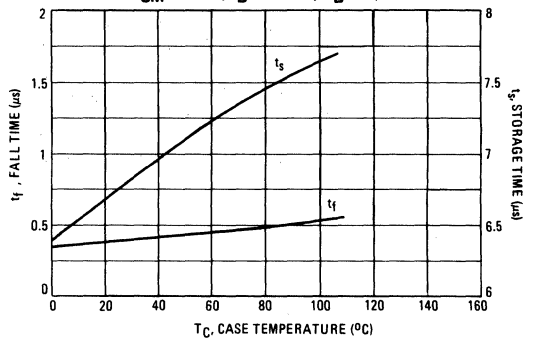


FIGURE 8 - OPTIMUM DRIVE CONDITIONS

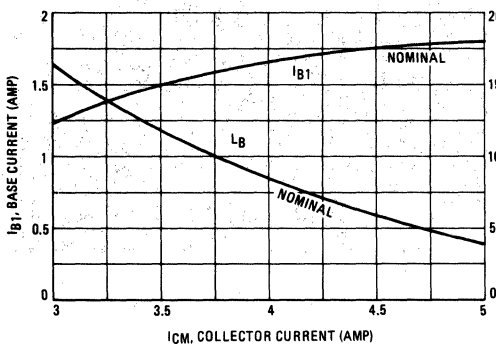
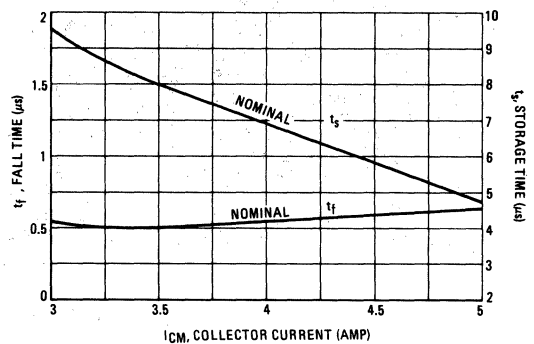


FIGURE 9 - SWITCHING BEHAVIOR versus I_{CM}



3

FIGURE 10 – THERMAL RESPONSE

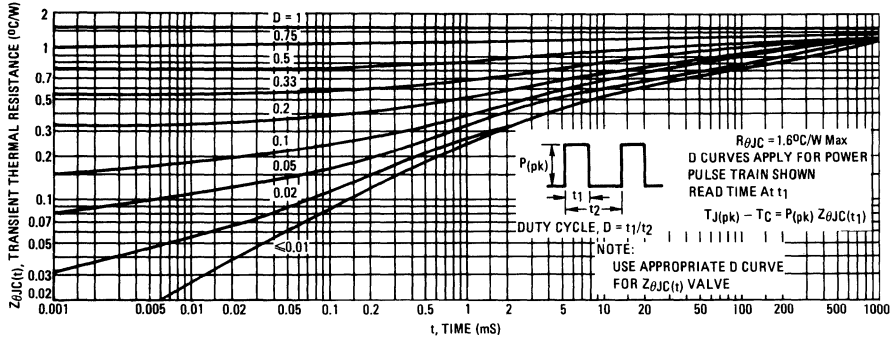


FIGURE 11 – COLLECTOR SATURATION REGION

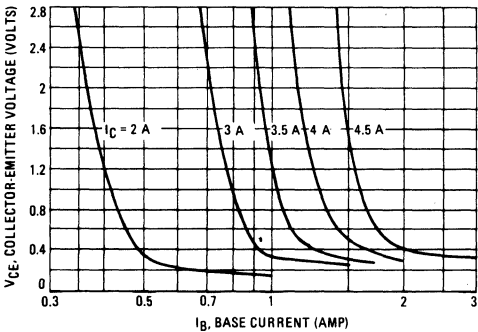


FIGURE 12 – DC CURRENT GAIN

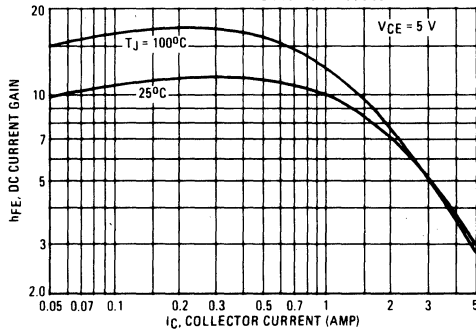


FIGURE 13 – "ON" VOLTAGES

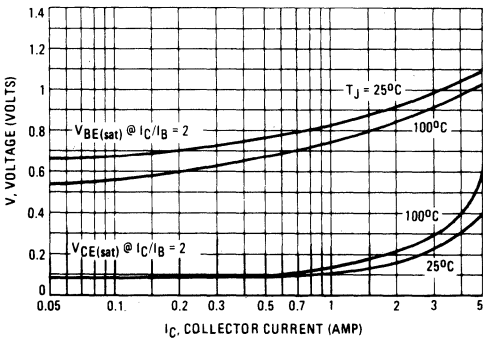
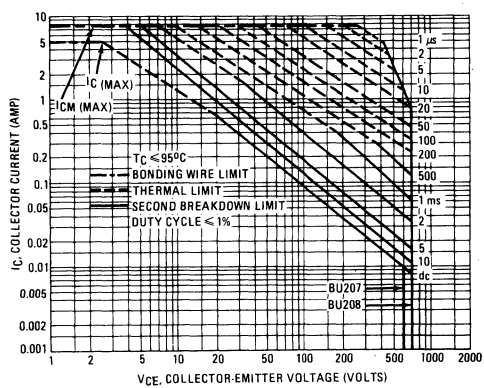


FIGURE 14 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA



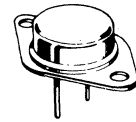
HORIZONTAL DEFLECTION TRANSISTOR

... designed for use in televisions.

- Collector-Emitter Voltages V_{CES} 1500/1700 Volts
- Fast Switching – 400 ns Typical Fall Time
- Low $V_{CE(sat)}$ 0.3 Vdc Typical at 4.5 Adc/2.25 Adc (BU208A)
- Low thermal Resistance $1^{\circ}\text{C}/\text{W}$ increased reliability
- Glass passivated (patented photoglass). Triple diffused Mesa Technology for long term stability.

6 AND 7 AMPERES
NPN SILICON
POWER TRANSISTORS

1500 to 1700 VOLTS



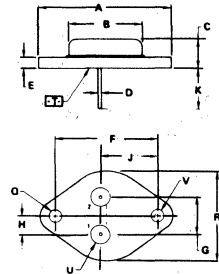
MAXIMUM RATINGS

Rating	Symbol	BU208A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector-Emitter Voltage	V_{CES}	1500	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current			Vdc
– Continuous	I_C	7 (5)	
– Peak	I_{CM}	15 (7.5)	
Base Current			A dc
– Continuous	I_B	4	
– Peak (Negative)	I_{BM}	3.5	
Total Power Dissipation at $T_C = 95^{\circ}\text{C}$ Derate above 95°C	P_D	20 (12.5) 1 (0.625)	Watts $\text{W}/^{\circ}\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +115	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0 (1.6)	$^{\circ}\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	$^{\circ}\text{C}$

NOTE: 1. Pulsed 5 ms, Duty Cycle \leq 10%.
 2. See page 3 for Additional Ratings on A Type.
 3. Figures in () are Standard Ratings Motorola Guarantees are Superior.



NOTES
 1. DIMENSIONS Q AND V ARE DATUMS
 2. T IS SEATING PLANE AND DATUM
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D
 $\text{M} \begin{matrix} \text{M} \\ \text{M} \end{matrix} \begin{matrix} \text{M} \\ \text{M} \end{matrix} \begin{matrix} \text{M} \\ \text{M} \end{matrix} \begin{matrix} \text{M} \\ \text{M} \end{matrix} \begin{matrix} \text{M} \\ \text{M} \end{matrix} \begin{matrix} \text{M} \\ \text{M} \end{matrix}$
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 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 (TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
-----------------	--------	------	------	------	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $L = 25\text{ mH}$)	$V_{CEO(sus)}$	700			Vdc
Collector Cutoff Current ¹ ($V_{CE} = \text{rated } V_{CES}$, $V_{BE} = 0$)	I_{CES}			1.0	mAdc
Emitter Base Voltage ¹ ($I_C = 0$, $I_E = 10\text{ mA}$) ($I_C = 0$, $I_E = 100\text{ mA}$)	V_{EBO}	5	7		Vdc

ON CHARACTERISTICS¹

DC Current Gain ($I_C = 4.5\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	2.25			
Collector-Emitter Saturation Voltage ($I_C = 4.5\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 4.5\text{ Adc}$, $I_B = 2\text{ Adc}$)	$V_{CE(sat)}$			5 1	Vdc
Base-Emitter Saturation Voltage ($I_C = 4.5\text{ Adc}$, $I_B = 2\text{ Adc}$)	$V_{BE(sat)}$			1.5	Vdc

DYNAMIC CHARACTERISTICS

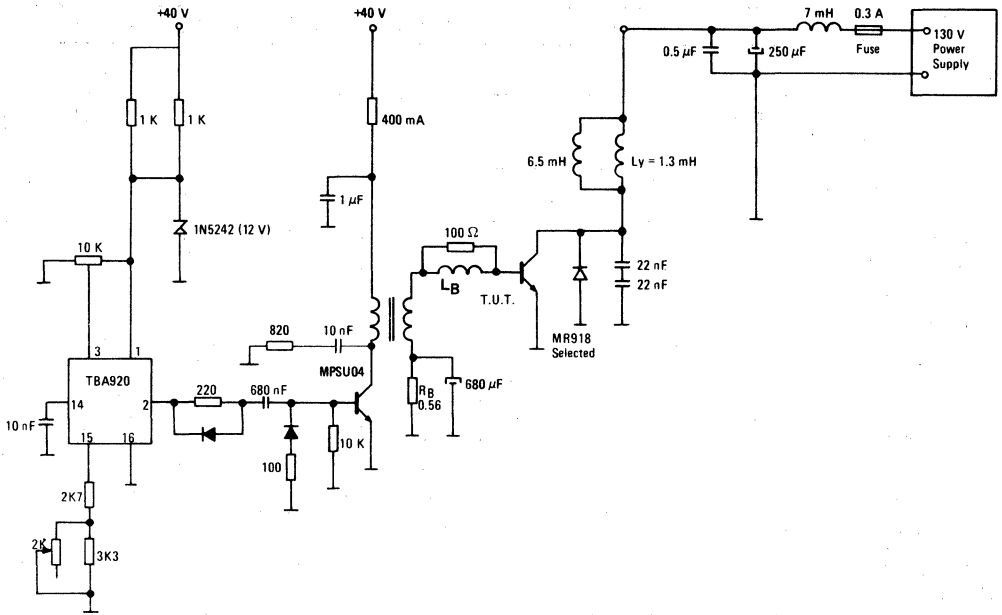
Current-Gain Bandwidth Product ($I_C = 0.1\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$, $f_{test} = 1\text{ MHz}$)	f_T		4		MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1\text{ MHz}$)	C_{ob}		125		pF

SWITCHING CHARACTERISTICS

Storage Time (see test circuit fig. 1) ($I_C = 4.5\text{ Adc}$, $I_{B1} = 1.8\text{ Adc}$, $L_B = 10\text{ }\mu\text{H}$)	t_s		8		μS
Fall time (see test circuit fig. 1) ($I_C = 4.5\text{ Adc}$, $I_{B1} = 1.8\text{ Adc}$, $L_B = 10\text{ }\mu\text{H}$)	t_f		0.4		μS

Pulse test: $PW = 300\text{ }\mu\text{S}$; Duty cycle $< 2\%$.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



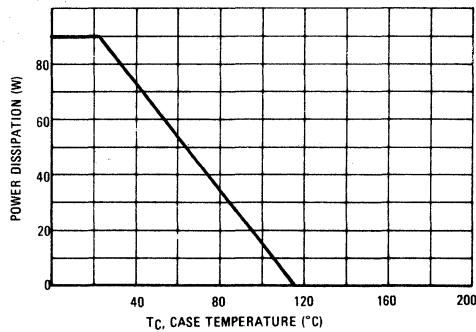
FLASHOVER PERFORMANCE

The BU208A is guaranteed to the following additional maximum ratings

I_C PEAK	10A	20 pulses maximum of
Followed by		Pulse Width $\leq 50 \mu s$. Duty cycle $\leq 50\%$.
V_{CES} PEAK	1650V	

3

FIGURE 2 – POWER DERATING



BASE DRIVE
The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM} . Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Fig. 3. This results in rapid, but only partial collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Fig. 4, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically since the equivalent circuit is complex, and since there are several important variables (I_{CM} , I_{B1} , and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B , at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B .

This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. For very low L_B a very narrow optimum is obtained. This occurs when $I_{B1} \cdot h_{FE} \cong I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM} . As L_B is increased, the curves become broader and flatter above the $I_{B1} \cdot h_{FE} = I_{CM}$ point as the turn off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE} , essentially moves the curves to the left, or right according to the relation $I_{B1} \cdot h_{FE} = \text{constant}$. It then becomes obvious that, for a specified I_{CM} , an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1} . The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Neither L_B nor I_{B1} are absolutely critical. Due to the high gain of Motorola devices it is suggested that in general a low value of I_{B1} be used to obtain optimum efficiency—eg. for BU208A with $I_{CM} = 4.5$ A use $I_{B1} \approx 1.5$ A, at $I_{CM} = 4$ A use $I_{B1} \approx 1.2$ A. These values are lower than for most competition devices but practical tests have showed comparable efficiency for Motorola devices even at the higher level of I_{B1} .

An L_B of 10 μH to 12 μH should give satisfactory operation of BU208A with I_{CM} of 4 to 4.5 A and I_{B1} between 1.2 and 2 A.

TEST CIRCUIT WAVEFORMS

FIGURE 3

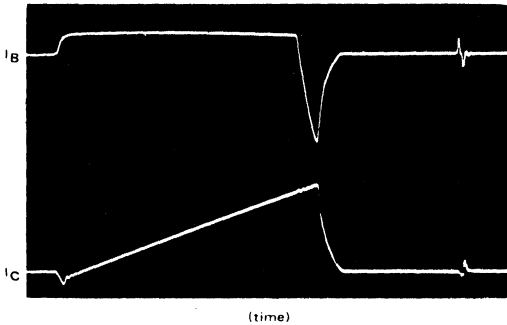
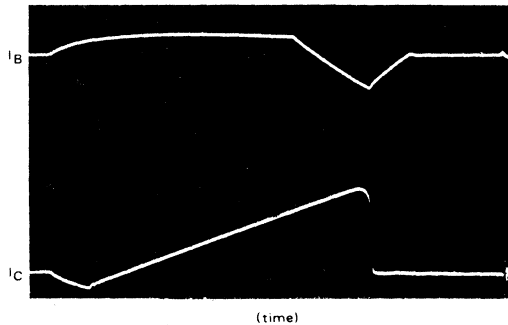


FIGURE 4



3

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive

power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected.

FIGURE 5 - DC CURRENT GAIN

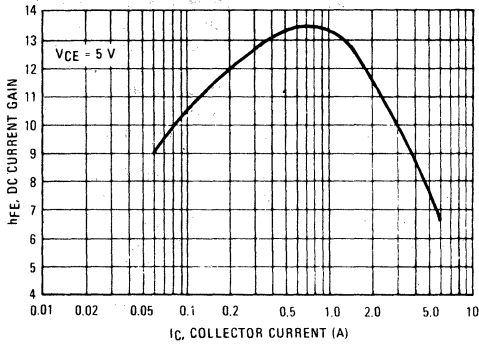


FIGURE 6 - COLLECTOR-EMITTER SATURATION VOLTAGE

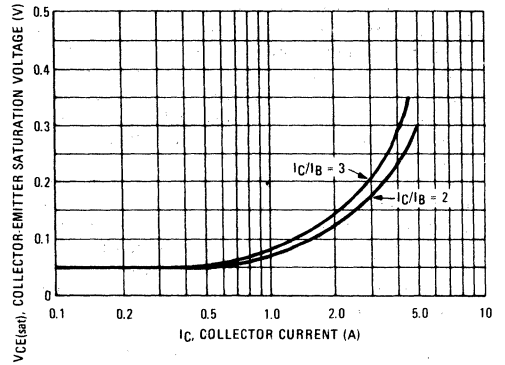


FIGURE 7 - BASE EMITTER SATURATION VOLTAGE

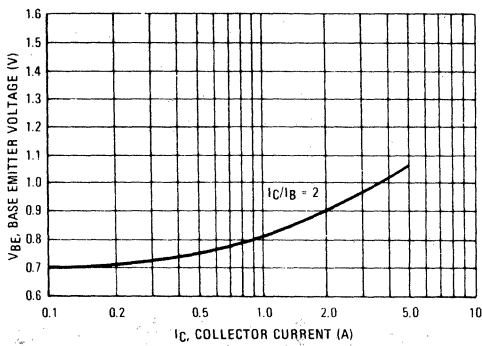


FIGURE 8 - COLLECTOR SATURATION REGION

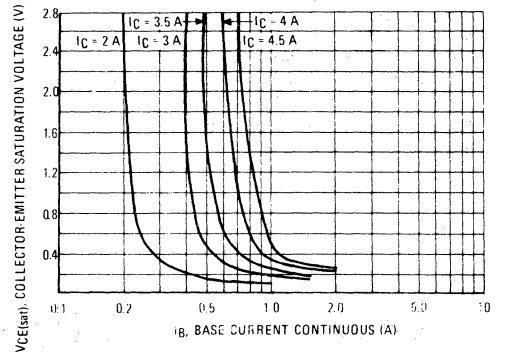
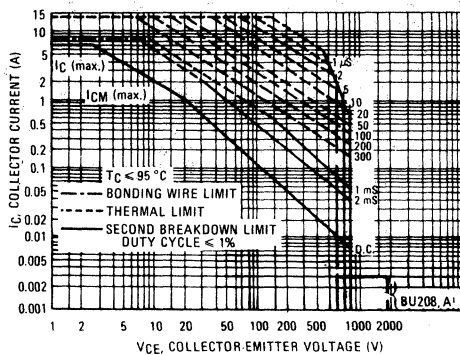


FIGURE 9 - MAXIMUM FORWARD BIAS SAFE OPERATING AREA



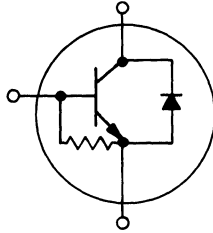
¹ Pulse width $\leq 20 \mu$ s. Duty cycle ≤ 0.25 . $R_{\theta E} \leq 100$ Ohms.

BU208D

NPN SILICON HORIZONTAL DEFLECTION TRANSISTOR WITH INTEGRATED DAMPER DIODE

... specifically designed for use in large screen color deflection circuits

- $V_{CES} = 1500 \text{ V}$;
 $V_{CEO(sus)} = 700 \text{ V (min)}$
- Low saturation:
 $V_{CE(sat)} = 1.0 \text{ V (max) @ } I_C = 4.5 \text{ Adc}$



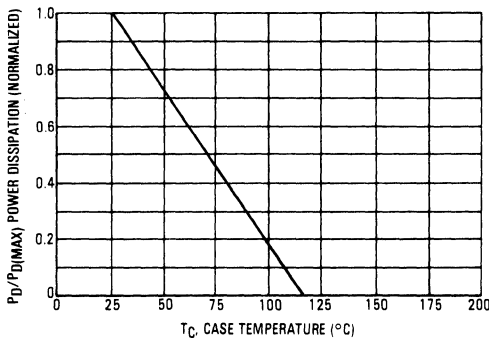
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	700	Vdc
Collector-Emitter Voltage ($R_{BE} = 0$)	V_{CES}	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	5.0	Adc
— Peak	I_{CM}	7.5	
Base Current — Peak	I_B	3.5	Adc
Total Device Dissipation $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	60 0.666	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 115	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	$^\circ\text{C/W}$

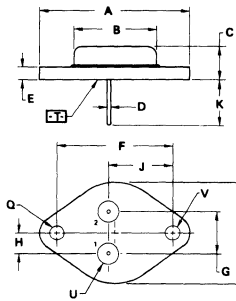
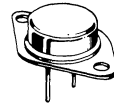
FIGURE 1 — POWER DERATING



5 AMPERES

**NPN SILICON
POWER TRANSISTORS**

**1500 VOLTS
60 WATTS**



NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. \square IS SEATING PLANE AND DATUM.

STYLE 1
PIN 1. BASE
CASE. EMITTER
COLLECTOR

3. POSITIONAL TOLERANCE FOR
MOUNTING HOLE Q:

$$\text{MOUNTING HOLE Q: } \text{M} \pm 0.13 (0.005) \text{ T V } \text{M}$$

FOR LEADS:

$$\text{FOR LEADS: } \text{M} \pm 0.13 (0.005) \text{ T V } \text{M } \text{M}$$

4. DIMENSIONS AND TOLERANCES PER
ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.38	0.055	0.070
F	30.15	BSC	—	1.187 BSC
G	10.92	BSC	—	0.430 BSC
H	5.46	BSC	—	0.215 BSC
J	16.89	BSC	—	0.665 BSC
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

**CASE 1-05
TO-204AA (Type)
(Formerly TO-3)**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 100\text{ mAdc}$, $I_B = 0$, $L = 25\text{ mH}$, $V_{\text{clamp}} = 800\text{ V}$)	$V_{\text{CEO(sus)}}$	700	—	Vdc
Collector Cutoff Current ($V_{\text{CE}} = 1500\text{ Vdc}$, $V_{\text{BE}} = 0$)	I_{CES}	—	1.0	mAdc
Emitter Cutoff Current ($V_{\text{EB}} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	300	mAdc
ON CHARACTERISTICS (1)				
Diode Forward Voltage ($I_F = 4.0\text{ A}$)	V_F	—	2.0	Vdc
Collector-Emitter Saturation Voltage ($I_C = 4.5\text{ Adc}$, $I_B = 2.0\text{ Adc}$)	$V_{\text{CE(sat)}}$	—	1.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 4.5\text{ Adc}$, $I_B = 2.0\text{ Adc}$)	$V_{\text{BE(sat)}}$	—	1.5	Vdc
SWITCHING CHARACTERISTICS (Inductive Load)				
Fall Time ($I_C(\text{end}) = 4.5\text{ Adc}$, $V_{\text{CC}} = 140\text{ Vdc}$, $I_B(\text{end}) = 1.8\text{ A}$, $L_C = 0.9\text{ mH}$, $L_B = 10\text{ }\mu\text{H}$)	t_f	—	0.6 (typ)	μs

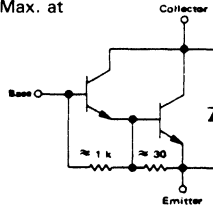
(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 3\%$.

BU323
BU323A

NPN SILICON POWER DARLINGTON TRANSISTOR

The BU323, BU323A are monolithic darlington transistors designed for automotive ignition, switching regulator and motor control applications.

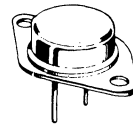
- V_{CE} Sat Specified at $-40^{\circ}\text{C} = 2\text{ V Max.}$ at $I_C = 6\text{ A.}$
- 550 mJ Energy Capability Tested in Automotive Ignition Circuit.
- Photoglass Passivation for Reliability and Stability.



16 AMPERE PEAK

POWER TRANSISTORS
DARLINGTON NPN SILICON

350 - 400 VOLTS
 175 WATTS



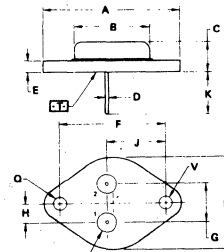
MAXIMUM RATINGS

Rating	Symbol	BU323	BU323A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Base Voltage	V_{CB0}	500	600	Vdc
Emitter-Base Voltage	V_{EB0}	8	8	Vdc
Collector Current - Continuous	I_C	10	10	Adc
Peak (1)		16	16	
Base Current - Continuous	I_B	3	3	Adc
Total Power Dissipation @ $T_C = 25^{\circ}\text{C}$	P_D	175	175	Watts
@ $T_C = 100^{\circ}\text{C}$		100	100	Watts
Derate above 25°C		1	1	W/ $^{\circ}\text{C}$
Operating and Storage Junction	T_J, T_{stg}	-65 to +200		$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	$^{\circ}\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^{\circ}\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.



- NOTES
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. [] IS SEATING PLANE AND DATUM
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\text{MOUNTING HOLE Q: } \text{M} \text{ } \text{L} \text{ } \text{V} \text{ } \text{O}$$

FOR LEADS:

$$\text{LEADS: } \text{M} \text{ } \text{L} \text{ } \text{V} \text{ } \text{O} \text{ } \text{R}$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	-	3.43	-	0.135
F	30.15 BSC	-	1.187 BSC	-
G	10.92 BSC	-	0.430 BSC	-
H	5.46 BSC	-	0.215 BSC	-
J	16.89 BSC	-	0.665 BSC	-
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

BU323, BU323A

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min.	Typ.	Max.	Unit	
OFF CHARACTERISTICS¹							
Collector-Emitter Sustaining Voltage (Figure 1) L = 10 mH ($I_C = 200\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	BU323 BU323A	$V_{\text{CEO(sus)}}$	350 400			Vdc	
Collector-Emitter Sustaining Voltage (Figure 1) ($I_C = 3\text{ A}$, $R_{\text{BE}} = 100\text{ Ohms}$, L = 500 μH) Unclamped	BU323 BU323A	$V_{\text{CER(sus)}}$	400 475			Vdc	
Collector Cutoff Current (Rated V_{CER} , $R_{\text{BE}} = 100\text{ Ohms}$)		I_{CER}			1	mAdc	
Collector Cutoff Current (Rated V_{CBO} , $I_E = 0$)		I_{CBO}			1	mAdc	
Emitter Cutoff Current ($V_{\text{EB}} = 6\text{ Vdc}$, $I_C = 0$)		I_{EBO}			40	mAdc	
ON CHARACTERISTICS¹							
DC Current Gain ($I_C = 3\text{ Adc}$, $V_{\text{CE}} = 6\text{ Vdc}$) ($I_C = 6\text{ Adc}$, $V_{\text{CE}} = 6\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 6\text{ Vdc}$)		h_{FE}	300 150 50	550 350 150	2000		
Collector-Emitter Saturation Voltage ($I_C = 3\text{ Adc}$, $I_B = 60\text{ mA}$) ($I_C = 6\text{ Adc}$, $I_B = 120\text{ mA}$) ($I_C = 10\text{ Adc}$, $I_B = 300\text{ mA}$) ($I_C = 6\text{ Adc}$, $I_B = 120\text{ mA}$, $T_C = -40^\circ\text{C}$)		$V_{\text{CE(sat)}}$			1.5 1.7 2.7 2.0	Vdc	
Base-Emitter Saturation Voltage ($I_C = 6\text{ Adc}$, $I_B = 120\text{ mA}$) ($I_C = 10\text{ Adc}$, $I_B = 300\text{ mA}$) ($I_C = 6\text{ Adc}$, $I_B = 120\text{ mA}$, $T_C = -40^\circ\text{C}$)		$V_{\text{BE(sat)}}$			2.2 3 2.4	Vdc	
Base-Emitter On Voltage ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 6\text{ Vdc}$)		$V_{\text{BE(on)}}$			2.5	Vdc	
Diode Forward Voltage ($I_F = 10\text{ Adc}$)		V_f		2	3.5	Vdc	
DYNAMIC CHARACTERISTICS							
Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)		C_{ob}		165	350	pF	
SWITCHING CHARACTERISTICS							
Storage Time	($V_{\text{CC}} = 12\text{ Vdc}$, $I_C = 6\text{ Adc}$, $I_{\text{B1}} = I_{\text{B2}} = 0.3\text{ Adc}$ Fig. 2		t_s		7.5	15	μs
Fall Time							
FUNCTIONAL TESTS							
Second Breakdown Collector Current with Base-Forward Biased		$I_{\text{S/B}}$		See Figure 10			
Pulsed Energy Test (See Figure 12)		$\frac{I_C^2 L}{2}$	550			mJ	

¹ Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

FIGURE 1 - SUSTAINING VOLTAGE TEST CIRCUIT

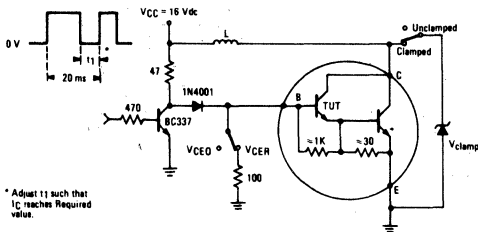


FIGURE 2 - SWITCHING TIMES TEST CIRCUIT

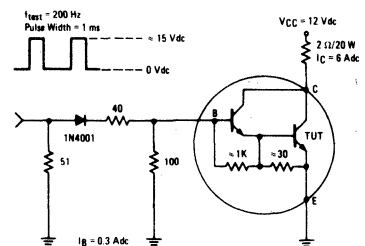


FIGURE 3 – DC CURRENT GAIN

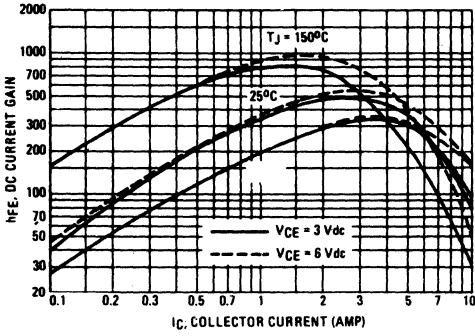


FIGURE 4 – COLLECTOR-SATURATION REGION

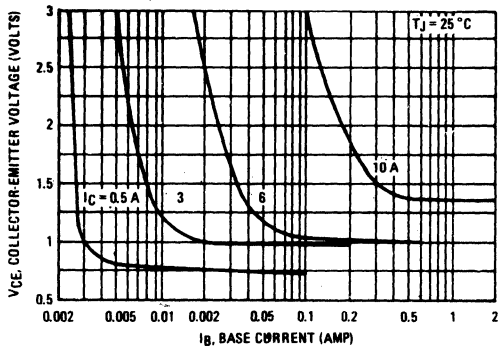


FIGURE 5 – COLLECTOR-EMITTER SATURATION VOLTAGE

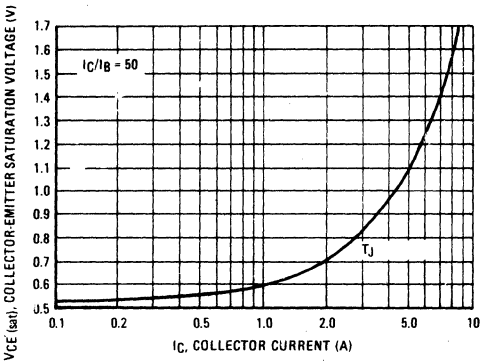


FIGURE 6 – BASE-EMITTER VOLTAGE

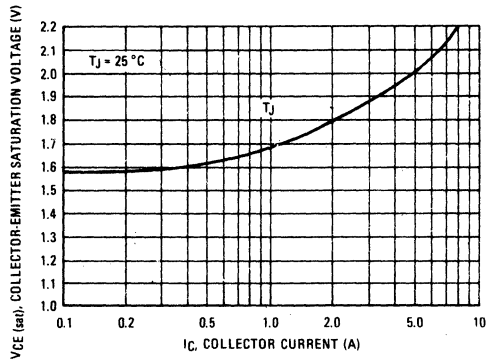


FIGURE 7 – TURN-OFF SWITCHING TIME

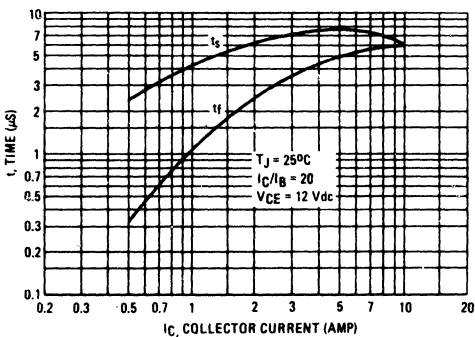
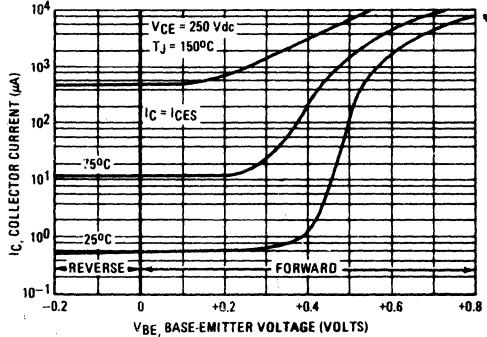


FIGURE 8 – COLLECTOR CUTOFF REGION



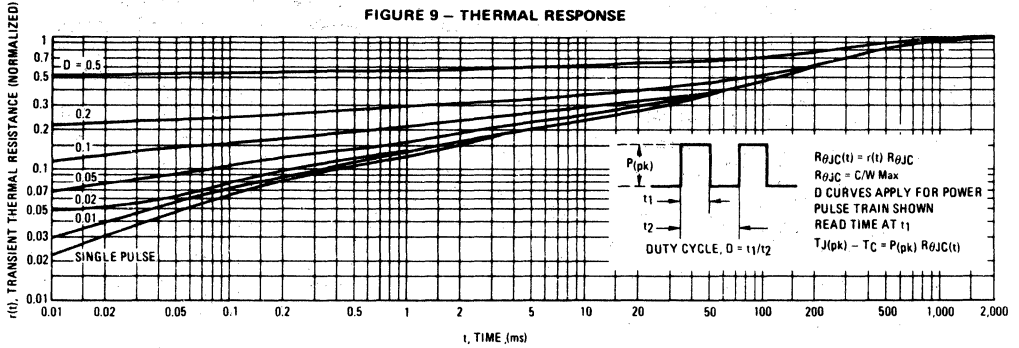
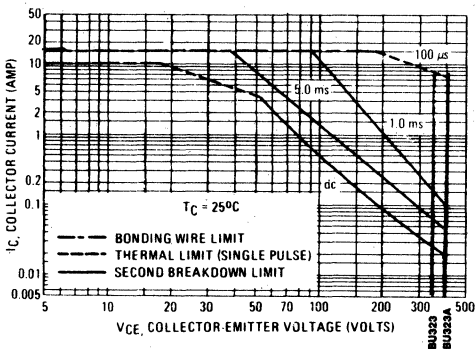


FIGURE 10 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING

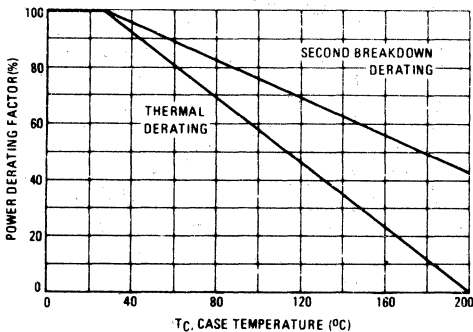
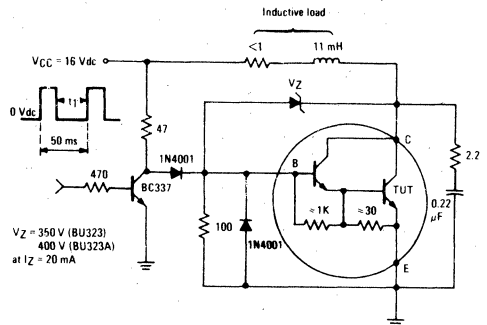


FIGURE 12 – IGNITION TEST CIRCUIT



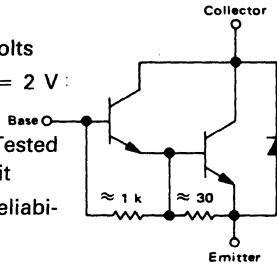
t_1 to be selected such that I_C reaches 10 Adc before switch-off.

NOTE: Figure 12 specifies energy handling capabilities in an automotive ignition circuit

BU323P
BU323AP

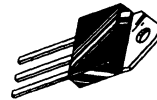
The BU323P, BU323AP are monolithic darlington transistors designed for automotive ignition, switching regulator and motor control applications.

- Collector-Emitter Sustaining Voltage - $V_{CE(sus)} = 475$ Vdc (Min. BU323AP)
- 125 Watts Capability at 50 Volts
- V_{CE} Sat Specified at $-40^{\circ}\text{C} = 2$ V Max. at $I_C = 6$ A
- 550 mJ Energy Capability Tested in Automotive Ignition Circuit
- Photoglass Passivation for Reliability and Stability



DARLINGTON
NPN SILICON
POWER TRANSISTORS

350 & 400 VOLTS
125 WATTS



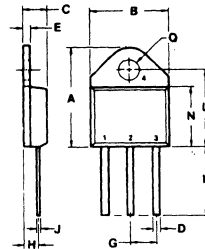
MAXIMUM RATINGS

Rating	Symbol	BU323P	BU323AP	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	200	250	Vdc
Collector-Emitter Voltage	V_{CEV}	300	350	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current - Continuous	I_C	50	40	Adc
- Peak (1)	I_{CM}	100	80	
- Overload	I_{OI}			
Base Current - Continuous	I_B	10	16	Adc
- Peak (1)	I_{BM}			
Total Power Dissipation - $T_C = 25^{\circ}\text{C}$	P_D	125		Watts
- $T_C = 100^{\circ}\text{C}$		100		Watts
Derate above 25°C		1		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: $\frac{1}{8}$ " from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.85	0.040	0.075
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.94	4.22	0.195	0.166

CASE 340-01
 (TO-18AC)

BU323P/BU323AP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS¹					
Collector-Emitter Sustaining Voltage (Figure 1) L = 10 mH ($I_C = 200\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	BU323P BU323AP $V_{\text{CEO(sus)}}$	350 400			Vdc
Collector-Emitter Sustaining Voltage (Figure 1) ($I_C = 3\text{ A}$, $R_{\text{BE}} = 100\text{ Ohms}$, L = 500 μH) Unclamped	BU323P BU323AP $V_{\text{CER(sus)}}$	400 475			Vdc
Collector Cutoff Current (Rated V_{CER} , $R_{\text{BE}} = 100\text{ Ohms}$)	I_{CER}			1	mA
Collector Cutoff Current (Rated V_{CBO} , $I_E = 0$)	I_{CBO}			1	mA
Emitter Cutoff Current ($V_{\text{EB}} = 6\text{ Vdc}$, $I_C = 0$)	I_{EBO}			40	mA

ON CHARACTERISTICS¹

DC Current Gain ($I_C = 3\text{ Adc}$, $V_{\text{CE}} = 6\text{ Vdc}$) ($I_C = 6\text{ Adc}$, $V_{\text{CE}} = 6\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 6\text{ Vdc}$)	h_{FE}	300 150 50	550 350 150	2000	
Collector-Emitter Saturation Voltage ($I_C = 3\text{ Adc}$, $I_B = 60\text{ mA}$) ($I_C = 6\text{ Adc}$, $I_B = 120\text{ mA}$) ($I_C = 10\text{ Adc}$, $I_B = 300\text{ mA}$) ($I_C = 6\text{ Adc}$, $I_B = 120\text{ mA}$, $T_C = -40^\circ\text{C}$)	$V_{\text{CE(sat)}}$			1.5 1.7 2.7 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 6\text{ Adc}$, $I_B = 120\text{ mA}$) ($I_C = 10\text{ Adc}$, $I_B = 300\text{ mA}$) ($I_C = 6\text{ Adc}$, $I_B = 120\text{ mA}$, $T_C = -40^\circ\text{C}$)	$V_{\text{BE(sat)}}$			2.2 3 2.4	Vdc
Base-Emitter On Voltage ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 6\text{ Vdc}$)	$V_{\text{BE(on)}}$			2.5	Vdc
Diode Forward Voltage ($I_F = 10\text{ Adc}$)	V_f		2	3.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}		165	350	pF
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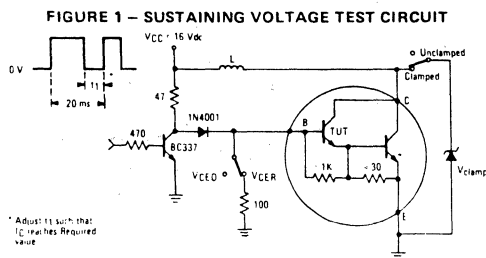
SWITCHING CHARACTERISTICS

Storage Time ($V_{\text{CC}} = 12\text{ Vdc}$, $I_C = 6\text{ Adc}$,	t_s	7.5	15	μs
Fall Time $I_{B1} = I_{B2} = 0.3\text{ Adc}$ Fig. 2				

FUNCTIONAL TESTS

Second Breakdown Collector Current with Base-Forward Biased	$I_{\text{S/B}}$		See Figure 10		
Pulsed Energy Test (See Figure 12)	$I_{\text{C}}^2 L$	550			mJ

¹ Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.



3-512

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

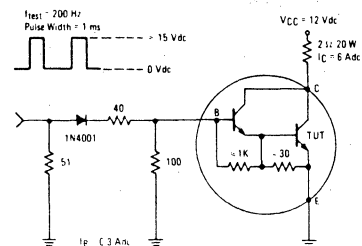


FIGURE 3 – DC CURRENT GAIN

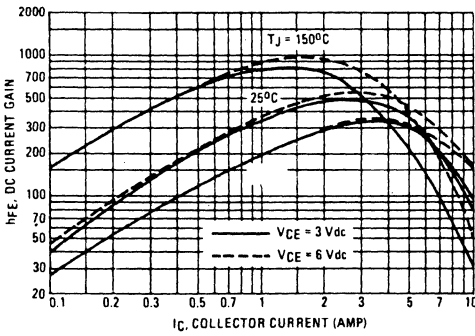


FIGURE 5 – COLLECTOR-EMITTER SATURATION VOLTAGE

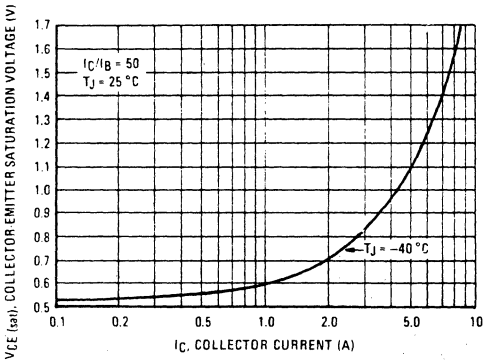


FIGURE 7 – TURN-OFF SWITCHING TIME

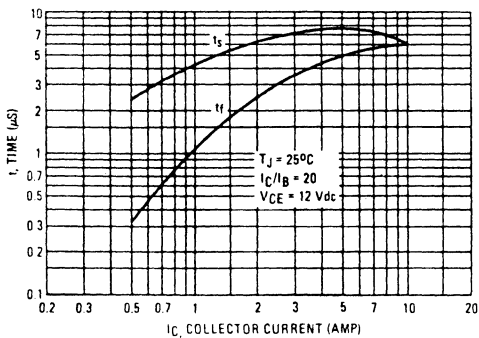


FIGURE 4 – COLLECTOR-SATURATION REGION

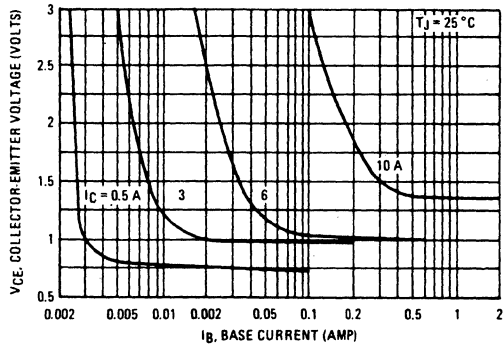


FIGURE 6 – BASE-EMITTER VOLTAGE

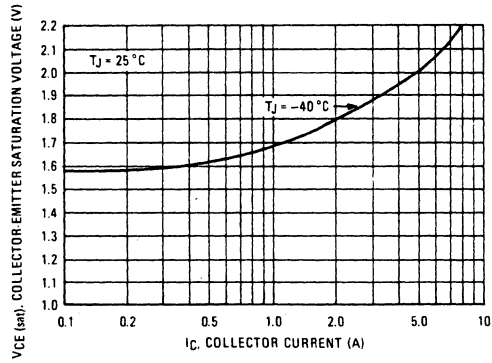
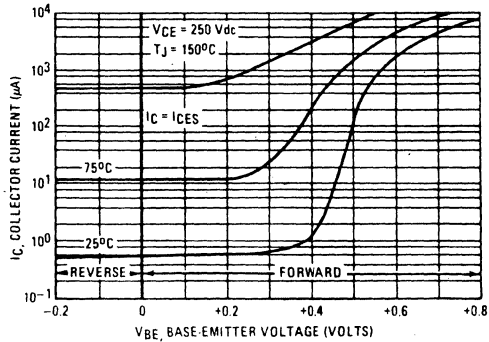


FIGURE 8 – COLLECTOR CUTOFF REGION



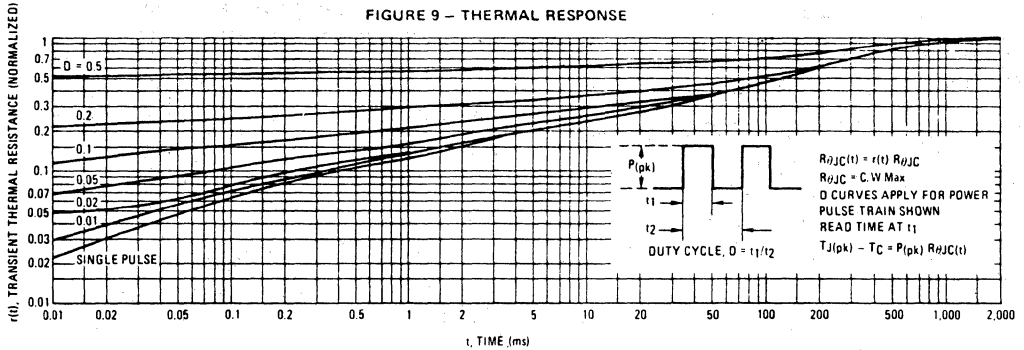
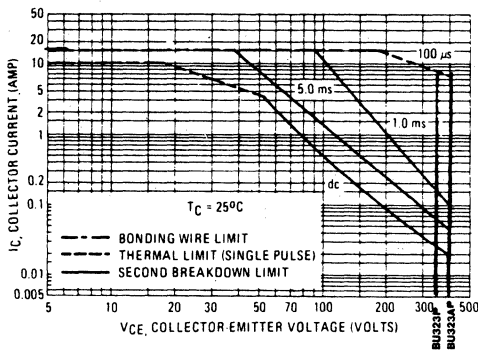


FIGURE 10 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_J(pk)$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

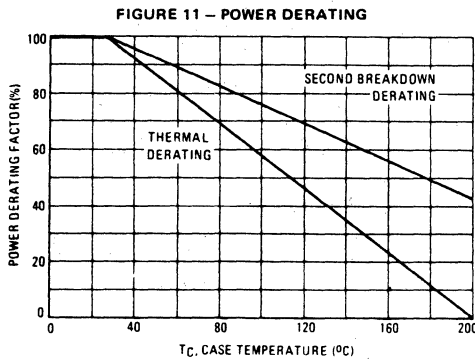
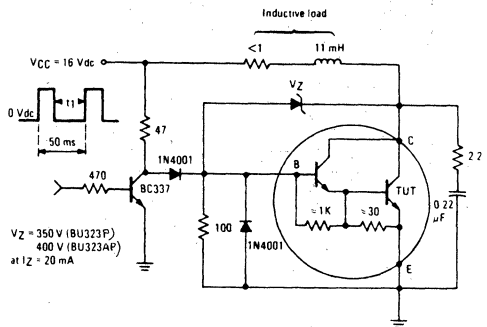


FIGURE 12 – IGNITION TEST CIRCUIT



t_1 to be selected such that I_C reaches 10 A dc before switch-off

NOTE: Figure 12 specifies energy handling capabilities in an automotive ignition circuit

BU326
BU326A

HIGH VOLTAGE NPN SILICON TRANSISTOR

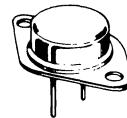
... Designed for use in the switch-mode power supplies of colour television receivers.

- Collector-Emitter Voltage $V_{CES} = 800\text{ V}$ and 900 V
- Collector-Current $I_C = 6\text{ A DC}$
- Low collector emitter saturation voltage
 $V_{CE(sat)} = 3\text{ V max. at } I_C = 4\text{ A}$
- Fall time at $I_C = 2.5\text{ A}$
 $T_F = 1\text{ }\mu\text{s max. at } T_C = 100\text{ }^\circ\text{C}$

6 AMPERES

NPN SILICON
POWER TRANSISTORS

375, 400 VOLTS
90 WATTS



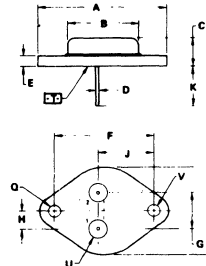
MAXIMUM RATINGS

Rating	Symbol	BU326	BU326A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	375	400	Vdc
Collector-Emitter Voltage	V_{CES}	800	900	Vdc
Emitter Base Voltage	V_{EB}	10		Vdc
Collector Current – Continuous	I_C	6		Adc
– Peak ¹	I_{CM}	8		
Base Current – Continuous	I_B	2		Adc
– Peak ¹	I_{BM}	3		
Reverse Base Current 20 ms max.	I_B	100		mA
– Peak during turn off	I_{BM}	3		A
Total Power Dissipation Derate above 25 °C	P_D	90		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.65	°C/W

¹ Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES

1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D.

⌀ ± 0.13 (0.005) T | v |

FOR LEADS

⌀ ± 0.13 (0.005) T | v | a |

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	8.25	7.52	0.320	0.300
D	0.97	1.09	0.038	0.043
E	-	3.43	-	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	4.82	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

BU326, BU326A

ELECTRICAL CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	BU326 BU326A	V_{CE0} (sus)	375 400		Vdc
Collector-Cutoff Current ($V_{CE} = 800\text{ V}$, $V_{BE} = 0$) ($V_{CE} = 900\text{ V}$, $V_{BE} = 0$)	BU326 BU326A	I_{CES}		1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 800\text{ V}$, $V_{BE} = 0$, $T_J = 125\text{ }^\circ\text{C}$) ($V_{CE} = 900\text{ V}$, $V_{BE} = 0$, $T_J = 125\text{ }^\circ\text{C}$)	BU326 BU326A	I_{CES}		2.0 2.0	mAdc
Emitter Cutoff Current ($V_{EB} = 10\text{ V}$, $I_C = 0$)		I_{EBO}		10	mAdc

ON CHARACTERISTICS¹

DC Current Gain ($I_C = 0.6\text{ A}$, $V_{CE} = 5\text{ V}$)		h_{FE}		30	—
Collector-Emitter Saturation Voltage ($I_C = 2.5\text{ A}$, $I_B = 0.25\text{ A}$) ($I_C = 4.0\text{ A}$, $I_B = 1.25\text{ A}$)		V_{CE} (sat)		10 3	Vdc
Base-Emitter Saturation Voltage ($I_C = 2.5\text{ A}$, $I_B = 0.25\text{ A}$) ($I_C = 4.0\text{ A}$, $I_B = 1.25\text{ A}$)		V_{BE} (sat)		1.4 1.6	Vdc

DYNAMIC CHARACTERISTICS

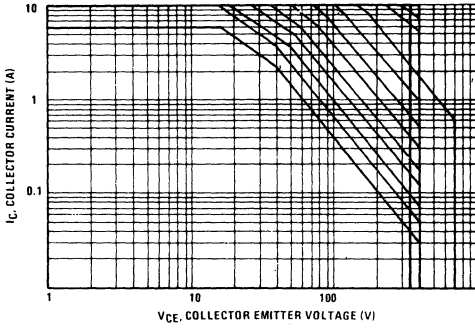
Current-Gain – Bandwidth Product ($I_C = 200\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1.0\text{ MHz}$)		f_T		6	MHz
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)					
Turn On Time	($I_C = 2.5\text{ A}$, $I_{B1} = 0.5\text{ A}$) ($I_{B2} = 1.0\text{ A}$, $V_{CC} = 250\text{ V}$)	t_{on}		0.5	μs
Storage Time		t_s		3.5	μs
Fall Time		t_f		0.3	μs
Fall Time	($I_C = 2.5\text{ A}$, $I_{B1} = 0.5\text{ A}$) ($I_{B2} = 1.0\text{ A}$, $V_{CC} = 250\text{ V}$, $T_C = 100\text{ }^\circ\text{C}$)	t_f		1.0	μs

¹ Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 2 – "ON" VOLTAGES

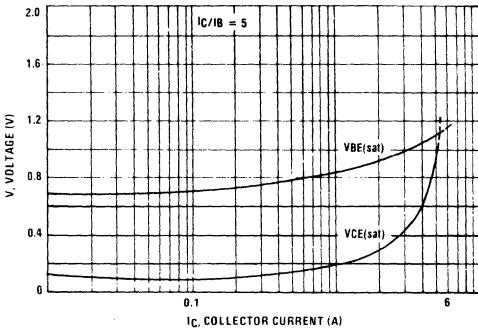


FIGURE 3 – DC CURRENT GAIN

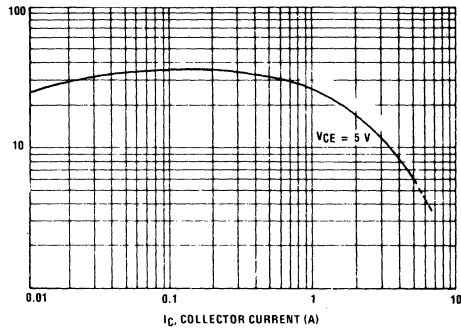


FIGURE 4 – RESISTIVE SWITCHING PERFORMANCE

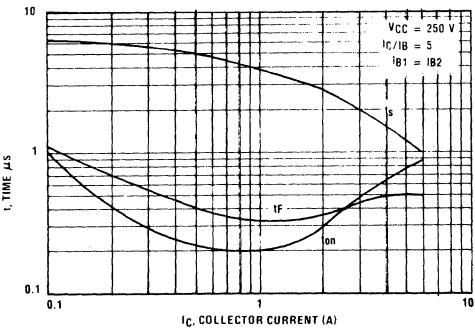
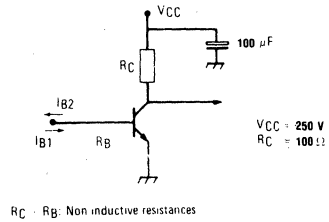


FIGURE 5 – SWITCHING TIMES TEST CIRCUIT



NPN Power Transistors

These devices are high voltage, high speed transistors for horizontal deflection output stages of TV's and CRT's.

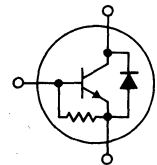
- High Voltage: $V_{CEV} = 330$ or 400 V
- Fast Switching Speed: $t_f = 750$ ns (max)
- Low Saturation Voltage: $V_{CE(sat)} = 1$ V (max) @ 5 A
- Packaged in Compact JEDEC TO-220AB
- "D" Suffix w/Integral Damper Diode

BU406,D
BU407,D

7 AMPERES
NPN SILICON
POWER TRANSISTORS
60 WATTS
150 and 200 VOLTS

MAXIMUM RATINGS

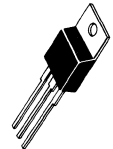
Rating	Symbol	BU406,D	BU407,D	Unit
Collector-Emitter Voltage	V_{CEO}	200	150	Vdc
Collector-Emitter Voltage	V_{CEV}	400	330	Vdc
Collector-Base Voltage	V_{CB0}	400	330	Vdc
Emitter Base Voltage	V_{EBO}	6		Vdc
Collector Current — Continuous	I_C	7		Adc
Peak Repetitive		10		
Peak (10 ms)		15		
Base Current	I_B	4		Adc
Total Device Dissipation, $T_C = 25^\circ\text{C}$ Derate above $T_C = 25^\circ\text{C}$	P_D	60		Watts W/°C
		0.48		
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 150		°C



"D" SUFFIX ONLY

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C



CASE 221A-04
TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ⁽¹⁾ ($I_C = 100$ mA, $I_B = 0$)	BU406,D BU407,D	$V_{CE0(sus)}$	200 150	— —	Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}, V_{BE} = 0$) ($V_{CE} = \text{Rated } V_{CE0} + 50$ Vdc, $V_{BE} = 0$) ($V_{CE} = \text{Rated } V_{CE0} + 50$ Vdc, $V_{BE} = 0, T_C = 150^\circ\text{C}$)		I_{CES}	— — —	— — —	5 0.1 1 mAdc
Emitter Cutoff Current ($V_{EB} = 6$ Vdc, $I_C = 0$)	BU406, BU407 BU406D, BU407D	I_{EBO}	— —	— —	1 400 mAdc
ON CHARACTERISTICS(1)					
Collector-Emitter Saturation Voltage ($I_C = 5$ Adc, $I_B = 0.5$ Adc)		$V_{CE(sat)}$	—	—	1 Vdc
Base-Emitter Saturation Voltage ($I_C = 5$ Adc, $I_B = 0.5$ Adc)		$V_{BE(sat)}$	—	—	1.2 Vdc
Forward Diode Voltage ($I_{EC} = 5$ Adc) "D" only		V_{EC}	—	—	2 Volts

(1) Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 1\%$.

(continued)

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{\text{test}} = 20 \text{ MHz}$)	f_T	10	—	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 1 \text{ MHz}$)	C_{ob}	—	80	—	pF
SWITCHING CHARACTERISTICS					
Inductive Load Crossover Time ($V_{CC} = 40 \text{ Vdc}$, $I_C = 5 \text{ Adc}$, $I_{B1} = I_{B2} = 0.5 \text{ Adc}$, $L = 150 \mu\text{H}$)	t_c	—	—	0.75	μs

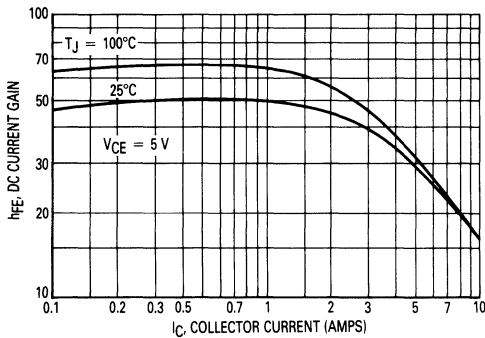


Figure 1. DC Current Gain

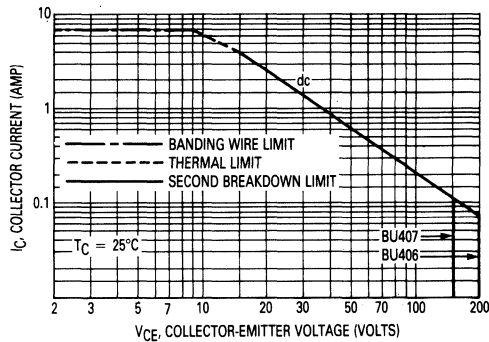


Figure 2. Maximum Rated Forward Bias Safe Operating Area

OUTLINE DIMENSIONS

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.86	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.106
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
 PIN 1: BASE
 2: COLLECTOR
 3: EMITTER
 4: COLLECTOR

**CASE 221A-04
TO-220AB**



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

BU426 BU426A

HIGH VOLTAGE NPN SILICON TRANSISTOR

... designed for use in the switched mode power supply of 90° and 110° colour television receivers.

- High Collector-Emitter Voltage
 $V_{CES} = 800\text{ V}, 900\text{ V}$
- Collector Current
 $I_C = 6\text{ A}$
- Low Collector Emitter Saturation Voltage
 $V_{CE(sat)} = 3\text{ Vdc}, @ I_C = 4\text{ A}, I_B = 1.25\text{ Adc}$
- Fall Time @ $I_C = 2.5\text{ A}, I_B(\text{end}) = 1\text{ A}$
 $t_f = 0.3\text{ }\mu\text{sec (typ)}$

6 AMPERES

TRIPLE DIFFUSED
NPN SILICON
POWER TRANSISTORS

800,900 VOLTS
113 WATTS

MAXIMUM RATINGS

Rating	Symbol	BU426	BU426A	Unit
Collector-Emitter Voltage	V_{CEO}	375	400	Vdc
Collector-Emitter Voltage $V_{BE} = 0$	V_{CES}	800	900	Vdc
Emitter-Base Voltage	V_{EB}	10		Vdc
Collector Current — Continuous	I_C	6		Adc
— Peak		12		
Base Current	I_B	2.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	113		Watts
Derate above 25°C		0.90		W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.1	$^\circ\text{C/W}$

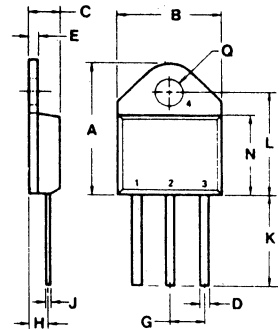
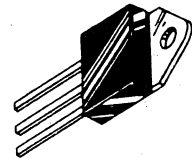
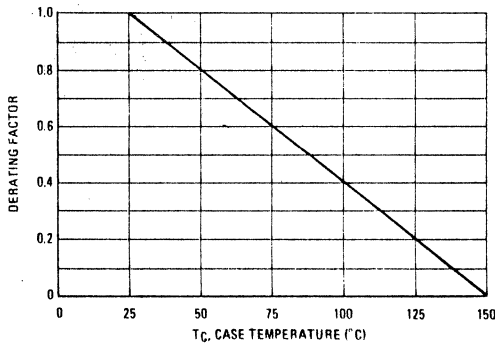


FIGURE 1 — POWER DERATING



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
(TO-218AC)

BU426
BU426A

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage See Figure 8 ($I_C = 100\text{ mA}$, $L = 25\text{ mH}$)	BU426 BU426A	V _{CEO}	375 400	— —	— —	V _{dc}
Collector-Cutoff Current ($V_{CES} = \text{Rated Value}$, $T_C = 25^\circ\text{C}$) ($V_{CES} = \text{Rated Value}$, $T_C = 125^\circ\text{C}$)		I _{CES}	— —	— —	1.0 2.0	mAdc
Emitter Cutoff Current ($V_{EB} = 10\text{ Vdc}$, $I_C = 0$)		I _{EBO}	—	—	10	mAdc

ON CHARACTERISTICS

DC Current Gain ($I_C = 0.6\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)		h _{FE}		30	—	—
Collector-Emitter Saturation Voltage ($I_C = 2.5\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 4\text{ Adc}$, $I_B = 1.25\text{ Adc}$)		V _{CE(sat)}	— — —	— — —	1.5 3	V _{dc}
Base-Emitter Saturation Voltage ($I_C = 4\text{ Adc}$, $I_B = 1.25\text{ Adc}$) ($I_C = 2.5\text{ Adc}$, $I_B = 0.5\text{ Adc}$)		V _{BE(sat)}	— —	— —	1.6 1.4	V _{dc}

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($I_C = 0.2\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f_{\text{test}} = 1.0\text{ MHz}$)		f _T		6		MHz
--	--	----------------	--	---	--	-----

SWITCHING CHARACTERISTICS (Resistive Load)

		MIN.	TYP.	MAX.	
Turn on Time	($I_C = 2.5\text{ A}$, $I_{B1} = 0.5\text{ A}$) ($I_{B2} = 1.0\text{ A}$, $V_{CC} = 250\text{ V}$)	t _{on}	0.2	0.6	μs
Storage Time		t _s	2	3.5	
Fall Time		t _f	0.5		
Fall Time	($I_C = 2.5\text{ A}$, $I_{B1} = 0.5\text{ A}$) ($I_{B2} = 1.0\text{ A}$, $V_{CC} = 250\text{ V}$, $T_C = 95^\circ\text{C}$)	t _f		0.75	μs
		t _f			

FIGURE 2 – DC CURRENT GAIN

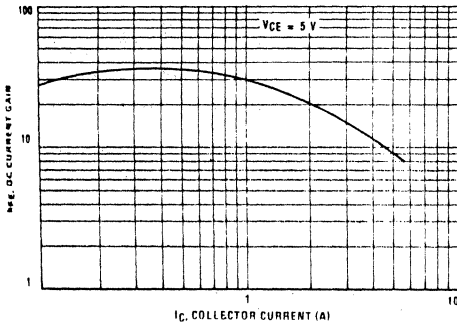


FIGURE 3 – "ON VOLTAGE"

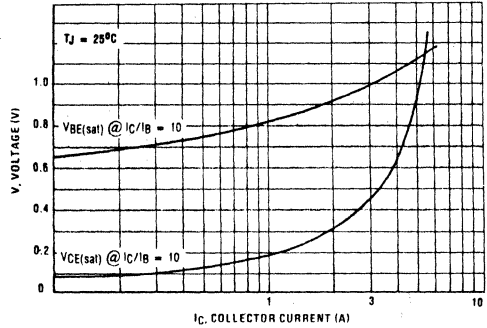


FIGURE 4 – TURN ON TIMES

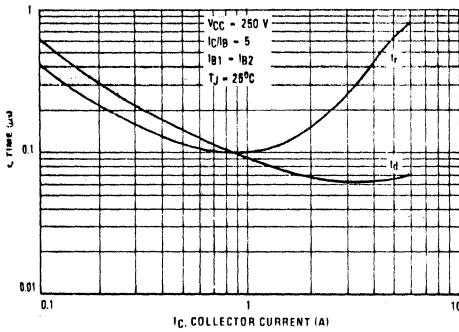


FIGURE 5 – TURN OFF TIMES

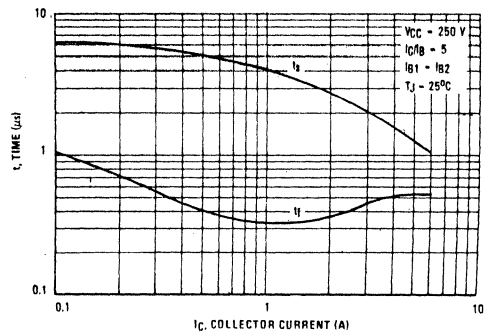
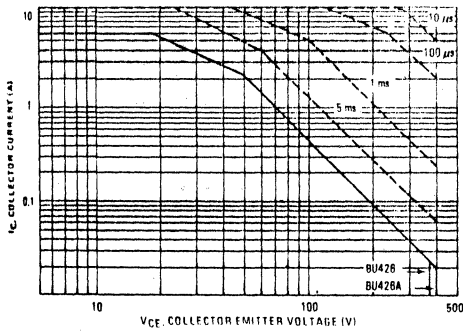


FIGURE 6 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C , V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 6 is based on $T_{J(pk)} = 150^\circ C$, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ C$. $T_{J(pk)}$ may be calculated from the data in figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN 415A)

FIGURE 7 - THERMAL RESPONSE

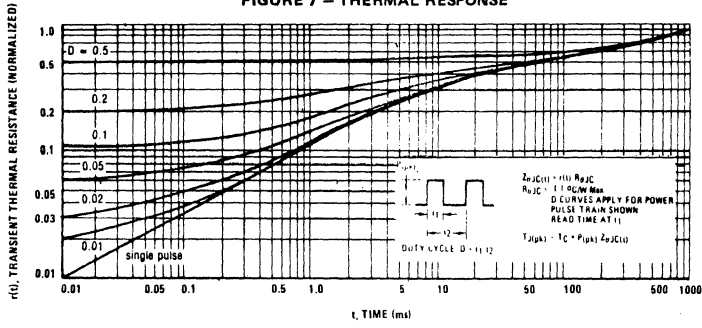
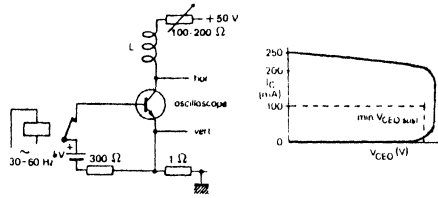


FIGURE 8 - SUSTAINING VOLTAGE TEST CIRCUIT



HORIZONTAL DEFLECTION TRANSISTOR

... specifically designed for use in large screen color deflection circuits

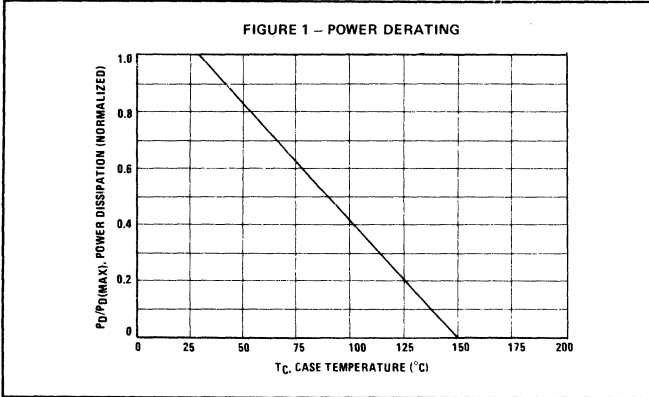
- $V_{CEX} = 1500\text{ V}$;
 $V_{CEO(sus)} = 700\text{ V (min.)}$
- Low saturation:
 $V_{CE(sat)} = 1\text{ V (max.) @ } I_C = 4.5\text{ Adc}$

MAXIMUM RATINGS

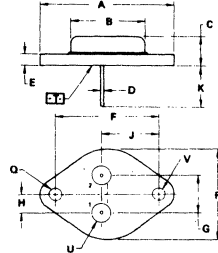
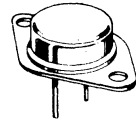
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector-Base Voltage	V_{CBO}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.0\text{ V}$)	V_{CEX}	1500	Vdc
Collector-Current – continuous	I_C	6	Adc
– peak ($p_w \leq 300\ \mu s$)	I_{CM}	16	Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	75	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.66	$^\circ\text{C/W}$



6 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
1500 VOLTS
75 WATTS



- NOTES:
 1 DIMENSIONS D AND V ARE DATUMS
 2 [] IS SEATING PLANE AND DATUM
 3 POSITIONAL TOLERANCE FOR MOUNTING HOLE D
 $\pm 0.13 (0.005) \text{ T V } \textcircled{C}$
 FOR LEADS:
 $\pm 0.13 (0.005) \text{ T V } \textcircled{C} \textcircled{C}$
 4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1975

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.37	-	1.550	-
B	21.08	-	0.830	-
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	-	3.43	-	0.135
F	30.15 BSC	-	1.187 BSC	-
G	10.92 BSC	-	0.430 BSC	-
H	5.46 BSC	-	0.215 BSC	-
J	16.89 BSC	-	0.665 BSC	-
K	11.18	12.19	0.440	0.480
Q	2.81	4.19	0.150	0.165
R	26.67	-	1.050	-
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
----------------	--------	------	------	------

OFF CHARACTERISTICS (1)

Collector-Emitter Sustaining Voltage ($I_C = 500\text{ mAdc}$, $I_B = 0$) $L = 10\text{ mH}$	$V_{CE(sus)}$	700		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 1000\text{ V}$, $I_E = 0$) ($V_{CE} = 1500\text{ V}$, $I_E = 0$)	I_{CBO}		0.02 1.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 1500\text{ V}$, $V_{BE} = -2\text{ V}$)	I_{CEX}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 100\text{ mA}$)	V_{EBO}	5		V
Emitter Cutoff Current ($V_{EB} = 4\text{ V}$)	I_{EBO}		10	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 4.5\text{ Adc}$, $V_{CE} = 5\text{ V}$)	h_{FE}	3.0		—
Collector-Emitter Saturation Voltage ($I_C = 4.5\text{ Adc}$, $I_B = 2\text{ A}$)	$V_{CE(sat)}$		1.0	Vdc
Base-Emitter On Voltage ($I_C = 4.5\text{ Adc}$, $V_{CE} = 2\text{ A}$)	$V_{BE(on)}$		1.3	Vdc

SWITCHING CHARACTERISTICS (Resistive Load)

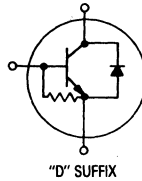
	($V_{CC} = 100\text{ Vdc}$, $I_C = 4.5\text{ A}$, $I_{B1} = 1.5\text{ A}$, $I_{B2} = 1.5\text{ A}$)		—		μs
Storage Time		t_s	—	1.2	
Fall Time		t_f	—	1.0	

(1) Pulse Test: Pulse Width = $300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

NPN Silicon Power Transistors Horizontal Deflection

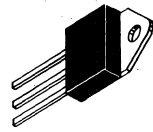
... specifically designed for use in large screen color deflection circuits.

- Glass Passivated (Patented Photoglass)
- Triple Diffused Mesa Technology for Long Term Stability
- Collector-Emitter Voltage — $V_{CE} = 1500$ Vdc
- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)} = 700$ Vdc
- Switching Times with Inductive Loads, $t_f = 0.5 \mu s$ (Typ) @ $I_C = 4.5$ A
- Optimum Drive Condition Curves
- Glass Base-Collector Junction
- TO-218 Package for Low Cost Mounting
- Available with Internal Flyback Diode, "D" Suffix



BU508
BU508D
BU508A
BU508AD

POWER TRANSISTORS
8 AMPERES
1500 VOLTS



CASE 340-01
TO-218 AC

MAXIMUM RATINGS

Rating	Symbol	All Parts	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector-Emmitter Voltage	V_{CES}	1500	Vdc
Emitter Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak ⁽¹⁾	I_C I_{CM}	8 15	Adc
Base Current — Continuous Peak ⁽¹⁾	I_B I_{BM}	4 6	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	125 1	Watts W/ $^\circ C$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 seconds	T_L	275	$^\circ C$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

BU508, BU508D, BU508A, BU508AD

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Emitter sustaining voltage ($I_C = 100 \text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	700	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 1500 \text{ Vdc}$, $V_{BE} = 0$, $T_C = 25^\circ\text{C}$) ($V_{CE} = 1500 \text{ Vdc}$, $V_{BE} = 0$, $T_C = 125^\circ\text{C}$)	I_{CES}	—	—	0.1 2	mA
Emitter Base Leakage ($V_{EB} = 6 \text{ V}$, $I_C = 0$)	BU508, A BU508D, AD I_{EBO}	—	—	10 300	mA

ON CHARACTERISTICS(1)

DC Current Gain ($I_C = 4.5 \text{ A}$, $V_{CE} = V_{dc}$)	h_{FE}	2.25	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 4.5 \text{ A}$, $I_B = 2 \text{ A}$)	BU508, D BU508A, AD $V_{CE(sat)}$	—	—	3 1	Vdc
Base Emitter Saturation Voltage ($I_C = 4.5 \text{ A}$, $I_B = 2 \text{ A}$)	$V_{BE(sat)}$	—	—	1.3	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 11			

DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product ($I_C = 0.1 \text{ A}$, $V_{CE} = 5 \text{ Vdc}$, $f_{test} = 1 \text{ MHz}$)	f_T	—	7	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	—	125	—	pF

SWITCHING CHARACTERISTICS

Fall Time ($I_C = 4.5 \text{ A}$, $I_B = 1.8 \text{ A}$, $dI_B/dt = 1 \text{ A}/\mu\text{s}$, $L_B = 10 \mu\text{H}$, see Figure 1)	t_s t_f		8 0.5		μs
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(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

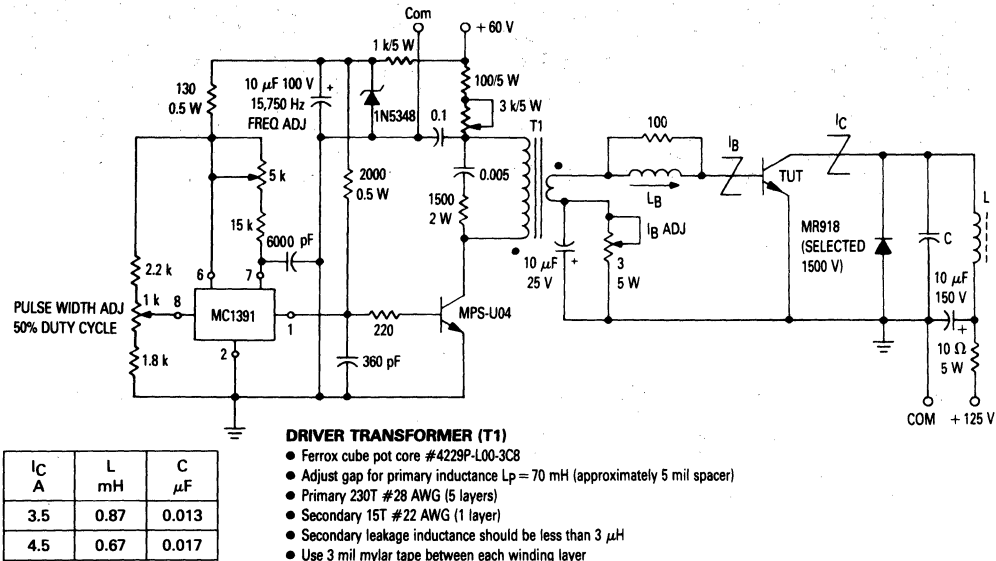


Figure 1. Switching Times Test Circuit

BASE DRIVE: The Key to Performance

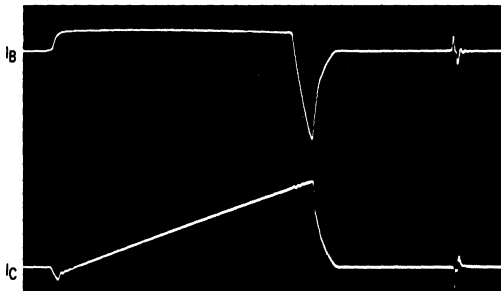
By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM} . Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM} , I_{B1} , and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B , at the desired conditions, for

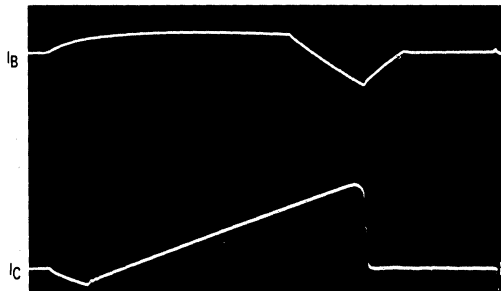
several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B . This kind of analysis shows the parameter which really matters is dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1} , and low values of L_B is due to switching losses as described above. For very low L_B a very narrow optimum is obtained. This occurs when $I_{B1} h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM} . As L_B is increased, the curves become broader and flatter above the $I_{B1} h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor *initiation* of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE} , essentially moves the curves to the left or right according to the relation $I_{B1} h_{FE} = \text{constant}$. It then becomes obvious that, for a specified I_{CM} , an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1} . The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Neither L_B nor I_{B1} are absolutely critical, and should be selected for the specific required condition. Similar curves relating to this discussion can be found on Motorola's data sheet for the BU207.

TEST CIRCUIT WAVEFORMS



(TIME)

Figure 2.



(TIME)

Figure 3.

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental impor-

tance. Once the required transistor-operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

3

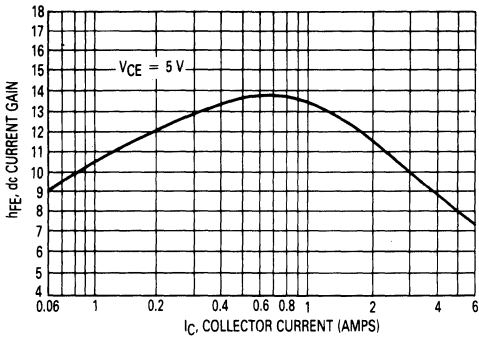


Figure 4. Typical dc Current Gain

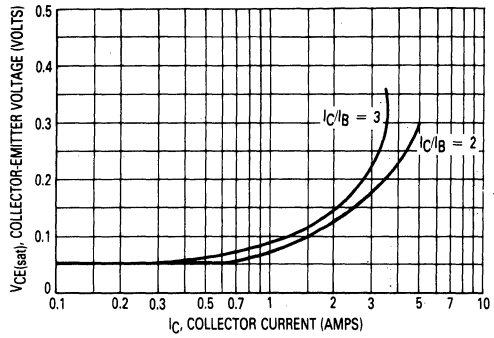


Figure 5. Typical Collector Saturation Voltage

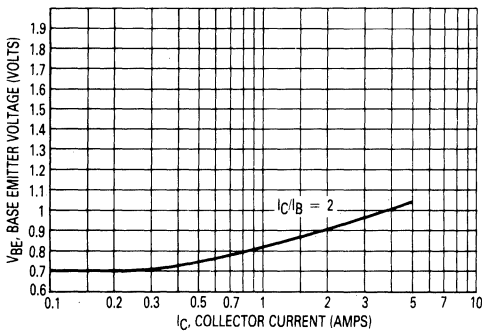


Figure 6. Typical Base Emitter Saturation Voltage

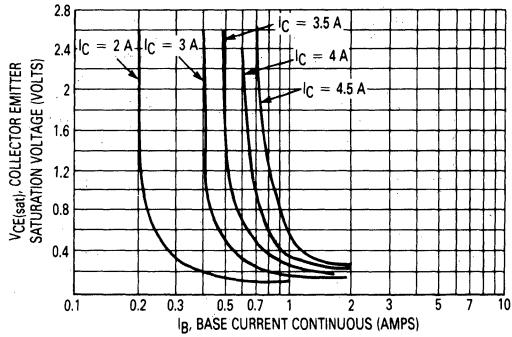


Figure 7. Typical Collector Saturation Region

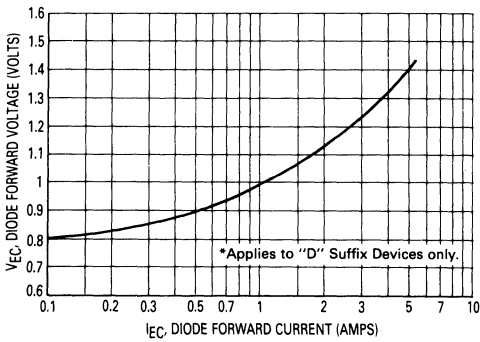


Figure 8. Typical Damper Diode Forward Voltage*

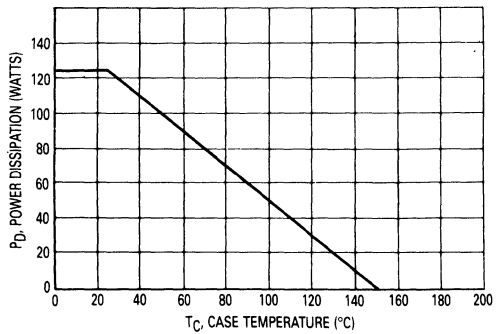


Figure 9. Power-Temperature Derating Curve

BU508, BU508D, BU508A, BU508AD

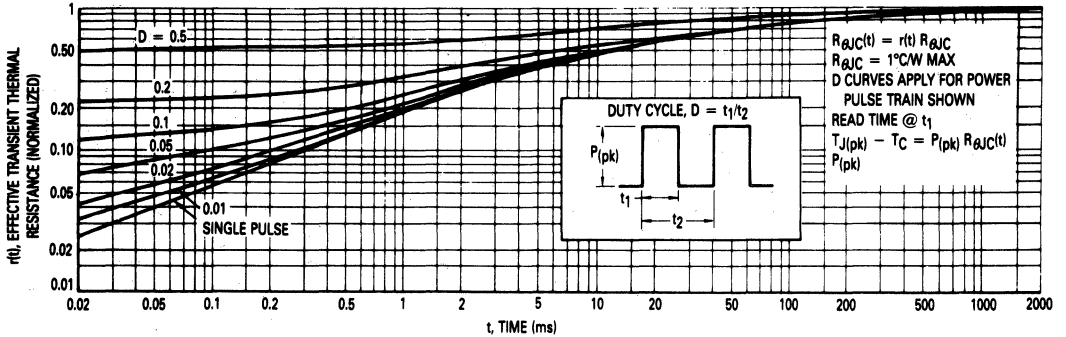


Figure 10. Thermal Response

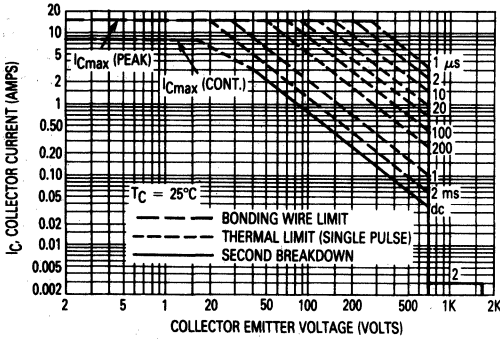
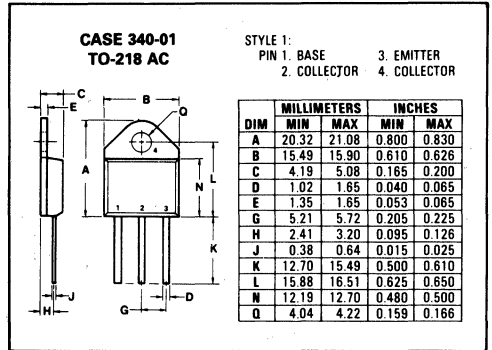


Figure 11. Maximum Forward Biased Safe Operating Area

Note (2) Operation in this area limited to Pulse Width < 20 μs ,
 Duty Cycle < 0.25, $R_{BE} < 100$ ohms



BU522
BU522A
BU522B

HIGH VOLTAGE SILICON POWER DARLINGTONS

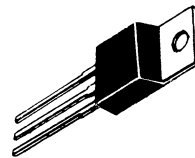
Power Transistor mainly intended for use as ignition circuit output transistor.

- Specified minimum sustaining voltage:
 $V_{CE(sus)} = 350 \text{ V (BU522)}$
 400 V (BU522A)
 425 V (BU522B)
- High S.O.A. capability:
 $V_{CE} = 350 \text{ V (BU522) at } I_C = 5 \text{ A}$
 $400 \text{ V (BU522A, BU522B)}$
- Low $V_{CE(sat)} = 2.0 \text{ V max. at } I_C = 4 \text{ A (BU522A, BU522B)}$

7 AMPERES

DARLINGTON
TRIPLE DIFFUSED
POWER TRANSISTORS
NPN SILICON

375, 425, 450 VOLTS
75 WATTS



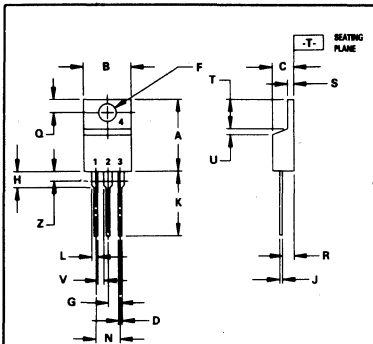
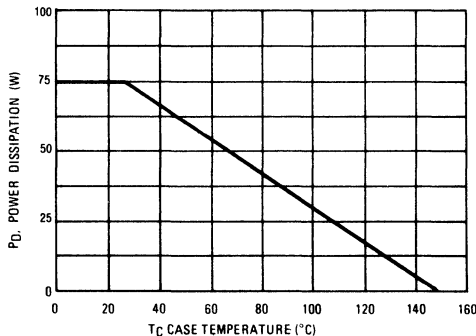
MAXIMUM RATINGS

Rating	Symbol	BU522	BU522A	BU522B	Unit
Collector-Emitter Voltage Sust.	$V_{CER(sus)}$	350	400	425	Vdc
Collector-Emitter Voltage	V_{CER}	375	425	450	Vdc
Collector-Base Voltage	V_{CBO}	400	450	475	Vdc
Emitter-Base Voltage	V_{EBO}		5.0	-	Vdc
Collector Current - Continuous	I_C		7.0		Adc
Base Current	I_B		2.0		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D		75	0.60	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}		-65 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	$^\circ\text{C/W}$

FIGURE 1 - POWER DERATING



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.56	10.28	0.380	0.406
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.82	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.87	6.47	0.232	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:
 PIN 1: BASE
 2: COLLECTOR
 3: EMITTER
 4: COLLECTOR

CASE 221A-04
TO-220AB

BU522, BU522A, BU522B

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (See Figure 2) (I _C = 1.0 A) See Figure 2	V _{CE(sus)}				Vdc
	BU522	350			
	BU522A	400			
	BU522B	425			
Collector Cutoff Current (Rated V _{CE} , R _{BE} = 270 Ω)	I _{CER}			1.0	mAdc
Collector Cutoff Current (Rated V _{CB0} , I _E = 0)	I _{CBO}			1.0	mAdc
Emitter Cutoff Current (V _{EB} = 5.0 Vdc, I _C = 0)	I _{EBO}			40	mAdc

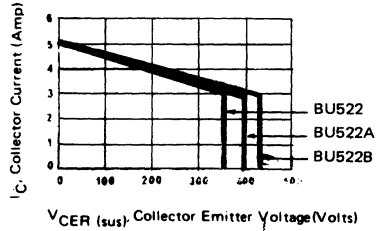
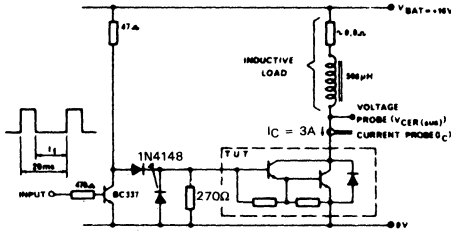
ON CHARACTERISTICS

DC Current Gain (I _C = 2.5 Adc, V _{CE} = 5 Vdc)	h _{FE}	250			—
Collector-Emitter Saturation Voltage (I _C = 4 Adc, I _B = 80 mAdc)	V _{CE(sat)}			2.5 2	Vdc
Base-Emitter Saturation Voltage (I _C = 4 Adc, I _B = 80 mAdc)	V _{BE(sat)}			2.5	Vdc

DYNAMIC CHARACTERISTICS

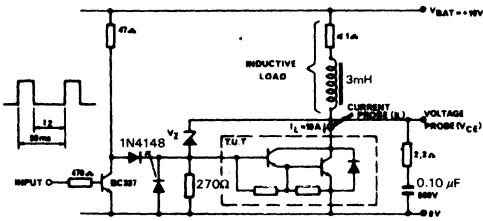
Current Gain – Bandwidth Product (I _C = 0.3 mAdc, V _{CE} = 5.0 Vdc, f _{test} = 1.0 MHz)	f _T		7.5		MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}		150		pF

FIGURE 2 - SUSTAINING VOLTAGE TEST $V_{CER} (sus)$



t_1 to be selected that I_C reaches 3 Adc before switch-off
Case temperature of the power transistor: $T_C = 25^\circ C$

Test conditions of the Collector-Base Clamping Circuit:



Clamping device characteristics:

$V_Z = 350 V (BU522)$
 $400 V (BU522A/B) \pm 1\%$ at $I_Z = 20 mA$

Clamping duration is around $45 \mu sec (BU522)$
 $40 \mu sec (BU522A/B)$

t_2 to be selected that I_L reaches 5 Adc before switch-off

Case temperature of the power transistor: $T_C = 25^\circ C$.

FIGURE 3 - S.O.A. TEST

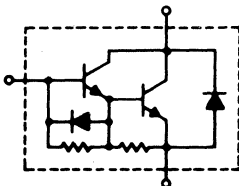
MOTOROLA SEMICONDUCTOR TECHNICAL DATA

BU806 BU807

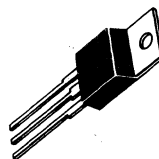
NPN DARLINGTON POWER TRANSISTORS

These Darlington transistors are high voltage, high speed devices for horizontal deflection circuits in TV's and CRT's.

- High Voltage: $V_{CEV} = 330$ or 400 V
- Fast Switching Speed:
 $t_c = 1.0 \mu s$ (max)
- Low Saturation Voltage:
 $V_{CE(sat)} = 1.5$ V (max)
- Packaged in JEDEC TO-220AB
- Dampener Diode V_F is specified.
 $V_F = 2.0$ V (max)



**8.0 AMPERE
DARLINGTON
NPN POWER
TRANSISTORS**
60 WATTS
150 and 200 VOLTS

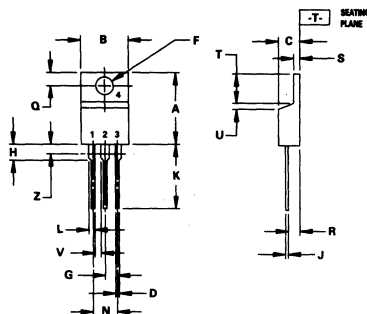


MAXIMUM RATINGS

Rating	Symbol	BU806	BU807	Unit
Collector-Emitter Voltage	V_{CEO}	200	150	Vdc
Collector-Emitter Voltage	V_{CEV}	400	330	Vdc
Collector-Base Voltage	V_{CBO}	400	330	Vdc
Emitter-Base Voltage	V_{EBO}	6.0		Vdc
Collector Current — Continuous	I_C	8.0		Adc
Collector Current — Peak		15		
Emitter-Collector Diode Current	I_F	10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation, $T_C = 25^\circ C$ Derate above $T_C = 25^\circ C$	P_D	60 0.48		Watts W/°C
Operating and Storage Junction Temperature Range	T_J , T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Lead Temperature for Soldering Purposes, 1/8" from Case for 5.0 Seconds	T_L	275	°C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.86	0.095	0.105
H	2.90	3.53	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.38	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.94	2.79	0.090	0.110
S	1.15	1.38	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:
PIN 1: BASE
2: COLLECTOR
3: EMITTER
4: COLLECTOR

CASE 221A-04
TO-220AB

BU806, BU807

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 100\text{ mAdc}$, $I_B = 0$)	BU806 BU807 $V_{CE(sus)}$	200 150	—	—	Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CBO}$, $V_{BE} = 0$)	I_{CES}	—	—	100	μAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $V_{BE(off)} = 6.0\text{ Vdc}$)	I_{CEV}	—	—	100	μAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	3.0	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 50\text{ mAdc}$)	$V_{CE(sat)}$	—	—	1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 50\text{ mAdc}$)	$V_{BE(sat)}$	—	—	2.4	Vdc
Emitter-Collector Diode Forward Voltage ($I_F = 4.0\text{ Adc}$)	V_F	—	—	2.0	Vdc

SWITCHING CHARACTERISTICS

Turn-On Time	(Resistive Load, $V_{CC} = 100\text{ Vdc}$, $I_C = 5.0\text{ Adc}$, $I_{B1} = 50\text{ mAdc}$, $I_{B2} = 500\text{ mAdc}$)	t_{on}	—	0.35	—	μs
Storage Time		t_s	—	0.55	—	μs
Fall Time		t_f	—	0.20	—	μs
Crossover Time ($I_C = 5.0\text{ Adc}$, $I_{B1} = 50\text{ mAdc}$, $V_{BE(off)} = 4.0\text{ Vdc}$, $V_{clamp} = 200\text{ Vdc}$, $L = 500\text{ }\mu\text{H}$)		t_c	—	0.40	1.0	μs

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$.

FIGURE 1 — DC CURRENT GAIN

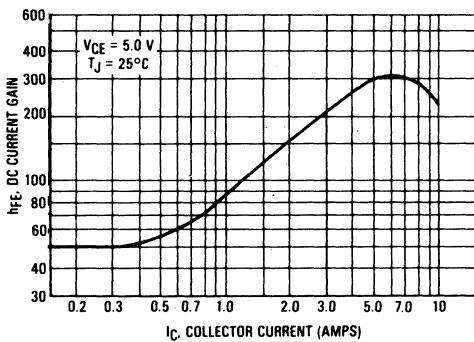
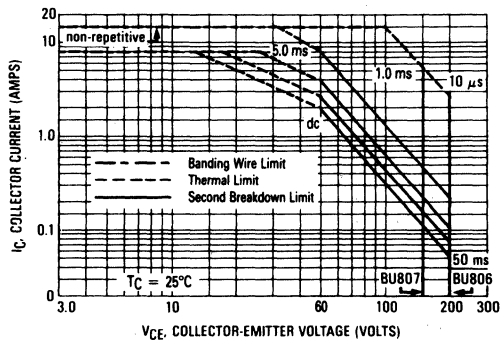


FIGURE 2 — SAFE OPERATING AREA (FSOA)



BUS36
BUS37

SWITCHMODE II^A SERIES
NPN SILICON POWER TRANSISTORS

The BUS36 and BUS37 transistors are designed for low voltage, high speed, power switching in inductive and resistive circuits where turn-off times are critical. They are particularly suited for battery-operated Switchmode applications and driver applications such as :

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

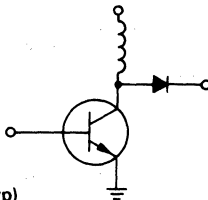
Fast Turn-Off Times

- 60 ns Inductive Fall Time – 25°C (Typ)
- 110 ns Inductive Crossover Time – 25°C (Typ)

Operating Temperature Range – 65 to + 175°C

100°C Performance Specified for :

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents (125°C)

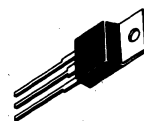


12 AMPERES
NPN SILICON
POWER TRANSISTORS

120 & 150 VOLTS
107 WATTS

Designer's Data for
"Worst Case" Conditions

The Designer's^A Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



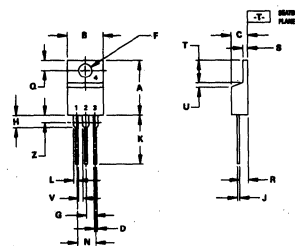
MAXIMUM RATINGS

Rating	Symbol	BUS36	BUS37	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	120	150	Vdc
Collector-Emitter Voltage	V_{CEV}	250	300	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous	I_C	12		Adc
– Peak (1)	I_{OL}	25		
– Overload		40		
Base Current – Continuous	I_B	7		Adc
– Peak (1)	I_{BM}	15		
Total Power Dissipation – $T_C = 25^\circ C$	P_D	107		Watts
Derate above 25°C – $T_C = 100^\circ C$		53		
		0.71		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to + 175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.



DIM	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	2.00	12.20	0.080	0.485
C	0.67	0.92	0.030	0.370
D	0.64	0.88	0.025	0.035
F	2.81	3.75	0.112	0.147
G	2.42	2.66	0.095	0.105
H	2.00	2.82	0.110	0.115
J	0.68	0.71	0.028	0.029
K	12.70	14.27	0.500	0.562
L	1.12	1.30	0.045	0.050
M	0.62	0.82	0.025	0.032
N	2.54	3.04	0.100	0.120
P	2.04	2.79	0.080	0.110
R	1.15	1.30	0.045	0.050
T	0.67	0.47	0.026	0.020
V	0.60	1.27	0.020	0.050
W	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

BUS36, BUS37

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) (IC = 50 mA, IB = 0) L = 25 mH	BUS36 BUS37	VCEO(sus)	120 150	— —	— —	Vdc
Collector Cutoff Current (VCEV = Rated Value, VBE(off) = 1.5 Vdc) (VCEV = Rated Value, VBE(off) = 1.5 Vdc, TC = 125°C)		ICEV	— —	— —	0.1 1.0	mAdc
Collector Cutoff Current	BUS36 : VCE = 60 V BUS37 : VCE = 75 V	ICEO	— —	— —	0.05 0.05	mAdc
Emitter Cutoff Current (VEB = 6 Vdc, IC = 0)		IEBO			0.1	mAdc
Emitter-base breakdown Voltage (IE = 50 mA - IC = 0)		BVEBO	8.0			Vdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	IS/b			See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	RBSOA			See Figure 13	

ON CHARACTERISTICS (1)

DC Current Gain (IC = 10 Adc, VCE = 2 Vdc) (IC = 0.5 Amp, VCE = 2 V)	hFE	30 50	— —	— —	—
Collector-Emitter Saturation Voltage (IC = 12 Amp, IB = 1.2 Amp) (IC = 12 Amp, IB = 1.2 Amp, TC = 100°C)	VCE(sat)	— —	— —	0.8 1.0	Vdc
Base-Emitter Saturation Voltage (IC = 12 Amp, IB = 1.2 Amp) (IC = 12 Amp, IB = 1.2 Amp, TC = 100°C)	VBE(sat)	— —	— —	1.8 1.8	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance (VCB = 10 Vdc, IE = 0, ftest = 100 kHz)	Cob	—	—	300	pF
Current Gain - Bandwidth Product (2) (IC = 1.0 Adc, VCE = 10 Vdc, ftest = 1.0 MHz)	fT	30	—	—	MHz

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	(VCC = 100 Vdc, IC = 12 A, IB1 = 1.2 A, tp = 30 μs, Duty Cycle ≤ 2%, VBE(off) = 5 V)	td	—	0.07	0.15	μs
Rise Time		tr	—	0.15	0.3	
Storage Time		ts	—	0.5	1.0	
Fall Time		tf	—	0.12	0.25	

Inductive Load, Clamped (Table 1)

Storage Time	(IC(pk) = 12 A, IB1 = 1.2 A, VBE(off) = 5 V, VCE(c1) = 100 V)	(TC = 25°C)	t _{sv}	—	0.5	—	μs
Fall Time			t _{fi}	—	0.06	—	
Storage Time		(TC = 100°C)	t _{sv}	—	0.6	1.0	
Fall Time			t _{fi}	—	0.15	0.30	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 - DC CURRENT GAIN

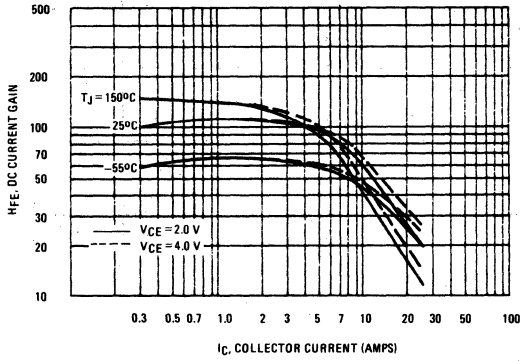


FIGURE 2 - COLLECTOR SATURATION REGION

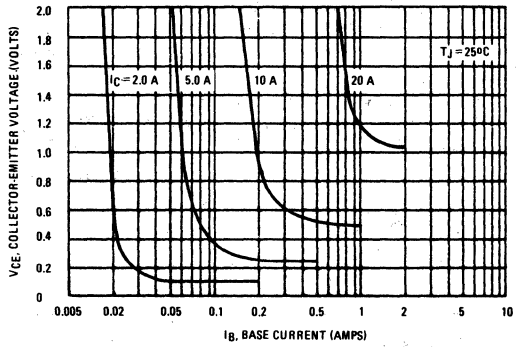


FIGURE 3 - COLLECTOR-EMITTER SATURATION VOLTAGE

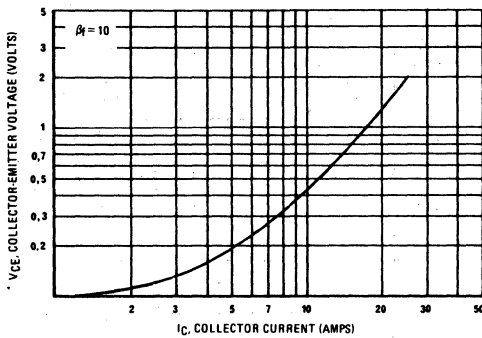


FIGURE 4 - BASE-EMITTER VOLTAGE

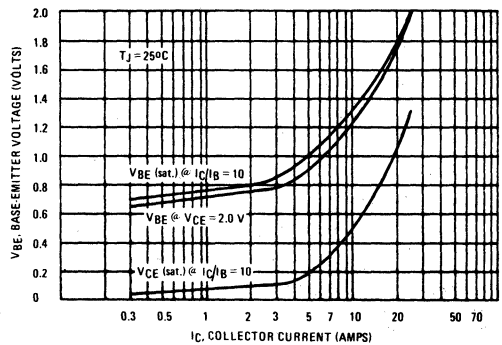


FIGURE 5 - COLLECTOR CUTOFF REGION

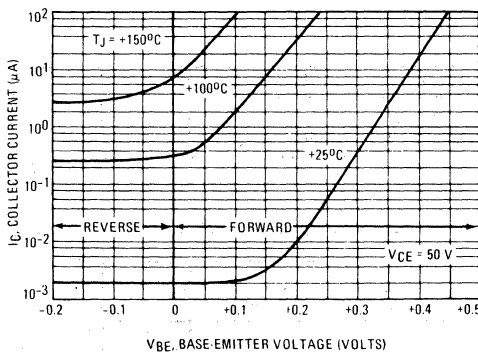
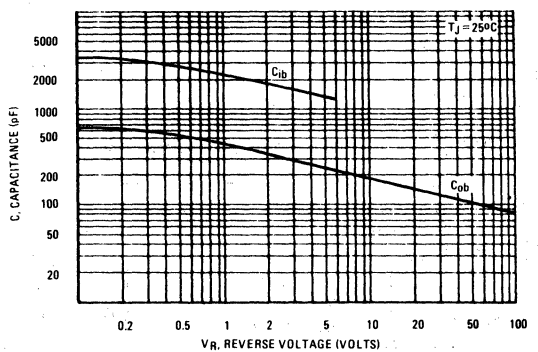


FIGURE 6 - CAPACITANCE



3

TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

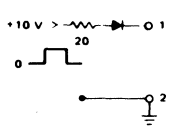
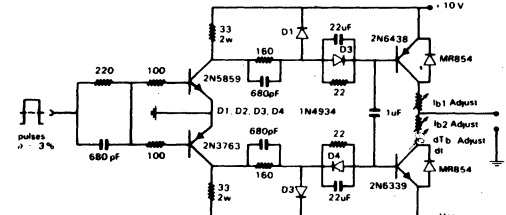
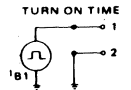
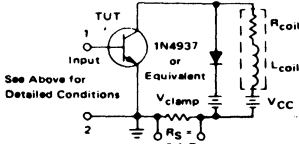
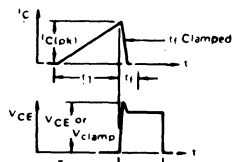
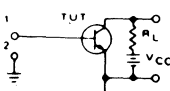
INPUT CONDITIONS	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
<p>$V_{CE0(sus)}$</p>  <p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>		 <p>TURN ON TIME</p> <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME</p> <p>Use inductive switching driver as the input to the resistive test circuit.</p>
<p>CIRCUIT VALUES</p> <p>$L_{coil} = 80 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$</p>	<p>$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$</p> <p>$V_{clamp} = 250 \text{ V}$ R_B adjusted to attain desired I_{B1}</p>	<p>$V_{CC} = 250 \text{ V}$ $R_L = 83 \Omega$ Pulse Width $10 \mu\text{s}$</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p> <p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$</p> <p>$t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$</p> <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

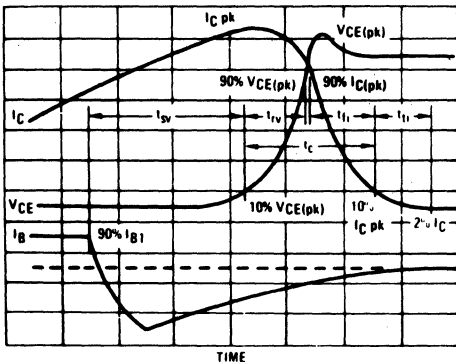
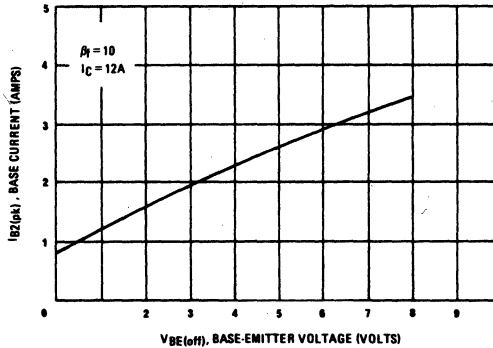


FIGURE 8 - PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
 - t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
 - t_{fi} = Current Fall Time, 90–10% I_C
 - t_{ti} = Current Tail, 10–2% I_C
 - t_c = Crossover Time, 10% V_{clamp} to 10% I_C
- An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME, T_{sv}

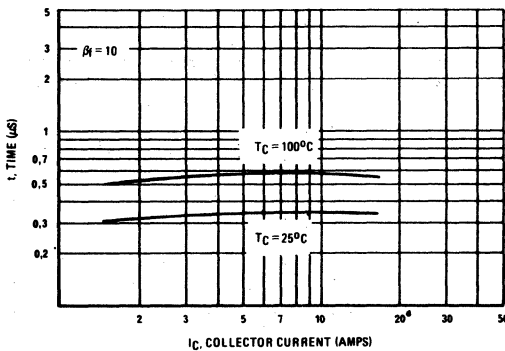


FIGURE 10 – FALL TIMES

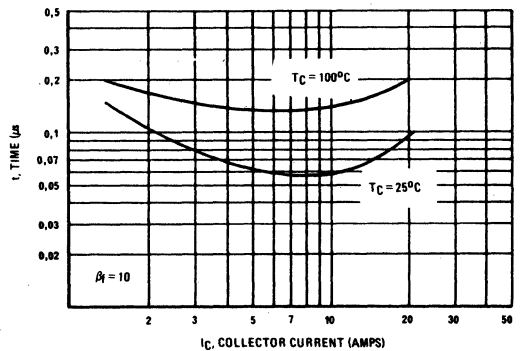


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

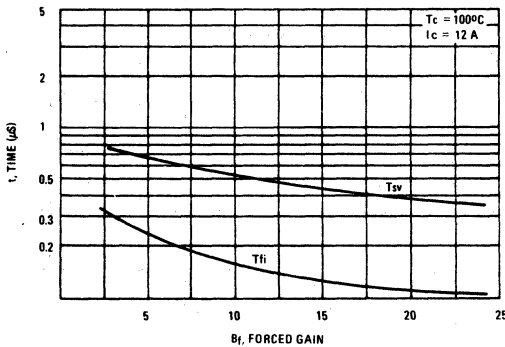
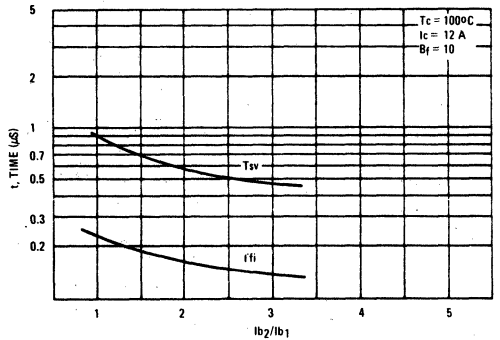


FIGURE 11b – TURN-OFF TIMES vs I_{b2}/I_{b1}



3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

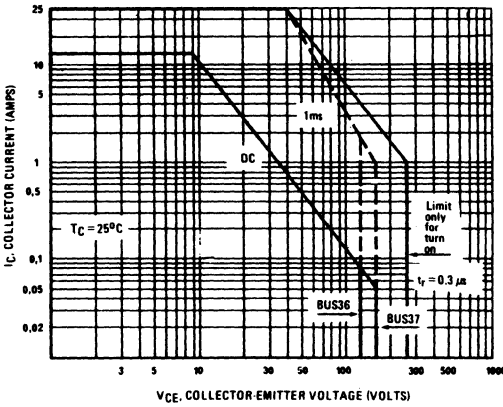


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

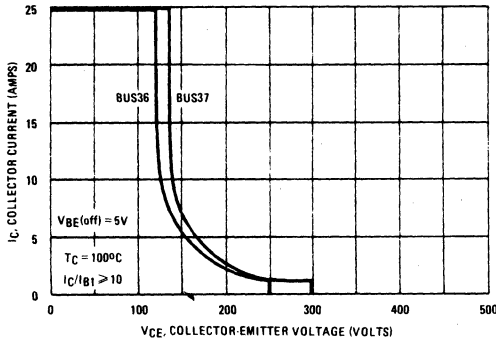
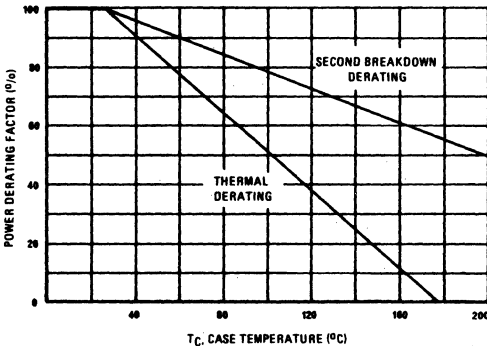


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

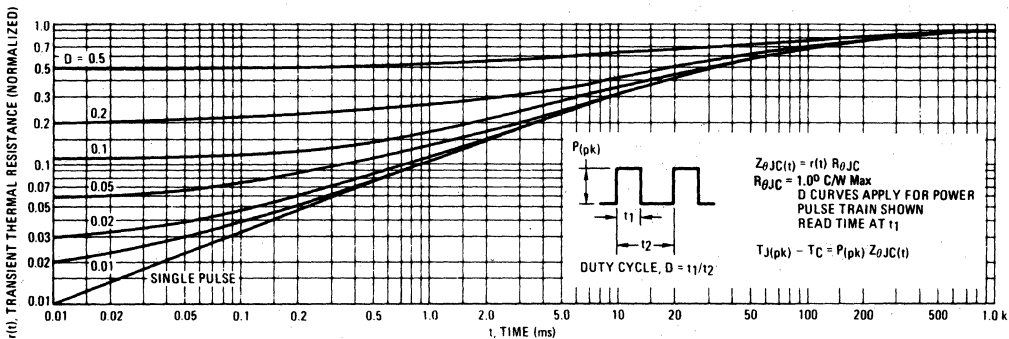
The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

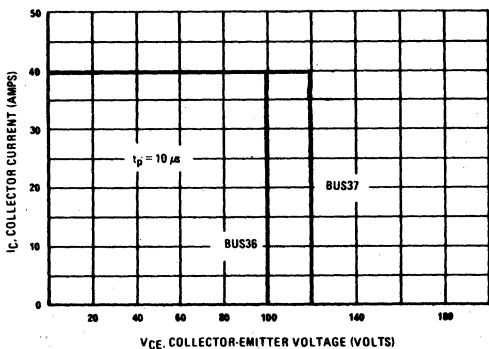
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load inductance shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped condition: so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

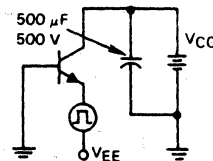
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 17) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 17 – OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C , t_p



3

BUS45P

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The BUS 45P transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

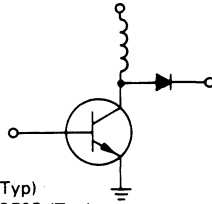
Fast Turn-Off Times

- 100 ns Inductive Fall Time—25°C (Typ)
- 150 ns Inductive Crossover Time—25°C (Typ)
- 400 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range – 65 to +150°C

100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

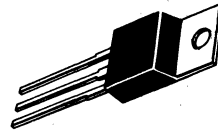


3 AMPERES
NPN SILICON
POWER TRANSISTORS

450 VOLTS
75 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



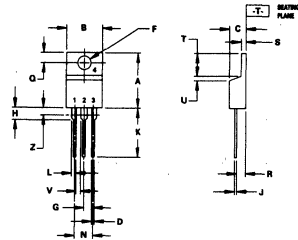
MAXIMUM RATINGS

Rating	Symbol	BUS 45P	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6	Vdc
Collector Current – Continuous	I_C	3	Adc
– Peak (1)	I_{CM}	5	
Base Current – Continuous	I_B	1.5	Adc
– Peak (1)	I_{BM}	3	
Total Power Dissipation – $T_C = 25^\circ C$	P_D	75	Watts
– $T_C = 100^\circ C$			
Derate above 25°C			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.



MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	5.96	10.29	0.235	0.405
C	4.87	4.82	0.190	0.190
D	0.94	0.98	0.035	0.035
F	3.91	3.71	0.150	0.145
G	2.42	2.88	0.095	0.105
H	2.90	3.93	0.110	0.155
J	0.48	0.71	0.019	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.28	0.045	0.050
M	4.80	5.00	0.190	0.200
Q	2.54	3.04	0.100	0.120
R	2.54	2.79	0.099	0.110
S	1.15	1.20	0.045	0.050
T	0.87	0.47	0.035	0.025
U	0.90	1.27	0.035	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

BUS45P

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (IC = 100 mA, IB = 0)	VCEO(sus)	450	—	—	Vdc
Collector Cutoff Current (VCEV = 850 V, VBE(off) = 1.5 Vdc) (VCEV = 850 V, VBE(off) = 1.5 Vdc, TC = 100°C)	ICEV	—	—	0.5 2.5	mAdc
Collector Cutoff Current (VCE = 850 V, RBE = 50 Ω, TC = 100°C)	ICER	—	—	3.0	mAdc
Emitter Cutoff Current (VEB = 6.0 Vdc, IC = 0)	IEBO	—	—	1.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain (IC = 2 Adc, VCE = 5.0 Vdc)	hFE	6	—	—	—
Collector-Emitter Saturation Voltage (IC = 2 Adc, IB = 0.5 Adc) (IC = 3 Adc, IB = 0.75 Adc) (IC = 2 Adc, IB = 0.5 Adc, TC = 100°C)	VCE(sat)	—	—	1.0 3.0 2.0	Vdc
Base-Emitter Saturation Voltage (IC = 2 Adc, IB = 0.5 Adc) (IC = 2 Adc, IB = 0.5 Adc, TC = 100°C)	VBE(sat)	—	—	1.5 1.5	Vdc

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	(VCC = 250 Adc, IC = 2 A, IB1 = 0.5 Adc, tp = 30 μs, Duty Cycle ≤ 2%, VBE(off) = 5.0 Vdc)	td	—	0.03	0.05	μs
Rise Time		tr	—	0.10	0.40	
Storage Time		ts	—	0.40	1.50	
Fall Time		tf	—	0.175	0.50	

Inductive Load, Clamped (Table 1)

Storage Time	(IC(pk) = 2 A, IB1 = 0.5 Adc, VBE(off) = 5.0 Vdc, VCE(pk) = 250 V)	(TJ = 100°C)	t _{sv}	—	0.70	2.0	μs
Crossover Time			tc	—	0.28	0.50	
Fall Time			t _{fi}	—	0.15	0.35	
Storage Time	(TJ = 25°C)	t _{sv}	—	0.40	—		
Crossover Time		tc	—	0.15	—		
Fall Time		t _{fi}	—	0.10	—		

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

$$\beta t = \frac{I_C}{I_B}$$

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The BUS 46P transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

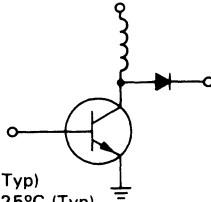
Fast Turn-Off Times

- 100 ns Inductive Fall Time—25°C (Typ)
- 150 ns Inductive Crossover Time—25°C (Typ)
- 400 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range -65 to +150°C

100°C Performance-Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



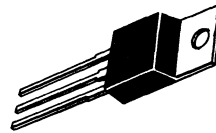
5 AMPERES

NPN SILICON
POWER TRANSISTORS

450 VOLTS
80 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



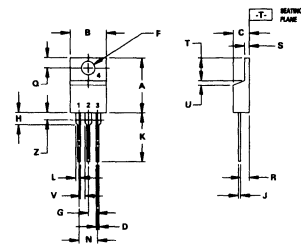
MAXIMUM RATINGS

Rating	Symbol	BUS 46P	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6	Vdc
Collector Current — Continuous	I_C	5	Adc
— Peak (1)	I_{CM}	8	
Base Current — Continuous	I_B	2	Adc
— Peak (1)	I_{BM}	4	
Total Power Dissipation — $T_C = 25^\circ\text{C}$	P_D	80	Watts
Derate above 25°C — $T_C = 100^\circ\text{C}$			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.



MILLIMETERS		INCHES	
MIN	MAX	MIN	MAX
A	14.68	15.75	0.620
B	9.68	10.28	0.380
C	4.07	4.82	0.160
D	0.94	0.98	0.035
F	3.61	3.73	0.142
G	2.42	2.68	0.095
H	2.90	3.03	0.115
J	0.46	0.71	0.018
K	12.75	14.27	0.500
L	1.15	1.20	0.045
N	4.83	5.30	0.190
Q	2.54	3.00	0.100
R	2.04	2.29	0.080
S	1.15	1.28	0.045
T	5.97	6.47	0.235
U	0.00	1.27	0.000
V	1.15	—	0.045
Z	—	2.04	—

STYLE 1: BASE
 PIN 1: COLLECTOR
 2: EMITTER
 3: COLLECTOR

NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
 2. CONTROLLING DIMENSION: INCH.
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CASE 221A-04
TO-220AB

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (IC = 100 mA, IB = 0)	VCEO(sus)	450	-	-	Vdc
Collector Cutoff Current (VCEV = 850 V, VBE(off) = 1.5 Vdc) (VCEV = 850 V, VBE(off) = 1.5 Vdc, TC = 100°C)	ICEV	-	-	0.5 2.5	mAdc
Collector Cutoff Current (VCE = 850 V, RBE = 50 Ω, TC = 100°C)	ICER	-	-	3.0	mAdc
Emitter Cutoff Current (VEB = 6.0 Vdc, IC = 0)	IEBO	-	-	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	IS/b			See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	RBSOA			See Figure 13	

ON CHARACTERISTICS (1)

DC Current Gain (IC = 3.0 Adc, VCE = 5.0 Vdc)	hFE	7.0	-	-	-
Collector-Emitter Saturation Voltage (IC = 3.0 Adc, IB = 0.6 Adc) (IC = 5.0 Adc, IB = 1.0 Adc) (IC = 3.0 Adc, IB = 0.6 Adc, TC = 100°C)	VCE(sat)	-	-	1.0 3.0 2.0	Vdc
Base-Emitter Saturation Voltage (IC = 3.0 Adc, IB = 0.6 Adc) (IC = 3.0 Adc, IB = 0.6 Adc, TC = 100°C)	VBE(sat)	-	-	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance (VCB = 10 Vdc, IE = 0, ftest = 100 KHz)	Cob	-	-	250	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	(VCC = 250 Adc, IC = 3.0 Adc, IB1 = 0.4 Adc, tp = 30 μs, Duty Cycle ≤ 2%, VBE(off) = 5.0 Vdc)	td	-	0.03	0.05	μs
Rise Time		tr	-	0.10	0.40	
Storage Time		ts	-	0.40	1.50	
Fall Time		tf	-	0.175	0.50	

Inductive Load, Clamped (Table 1)

Storage Time	(IC(pk) = 3.0 A, IB1 = 0.4 Adc, VBE(off) = 5.0 Vdc, VCE(pk) = 250 V)	(TJ = 100°C)	t _{sv}	-	0.70	2.0	μs
Crossover Time			tc	-	0.28	0.50	
Fall Time		tfj	-	0.15	0.30		
Storage Time		(TJ = 25°C)	t _{sv}	-	0.40	-	
Crossover Time			tc	-	0.15	-	
Fall Time			tfj	-	0.10	-	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

$$\beta_f = \frac{I_C}{I_B}$$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

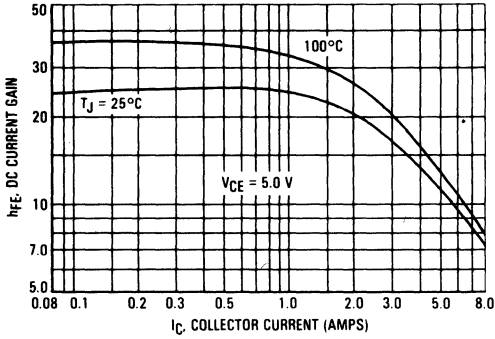


FIGURE 2 — COLLECTOR SATURATION REGION

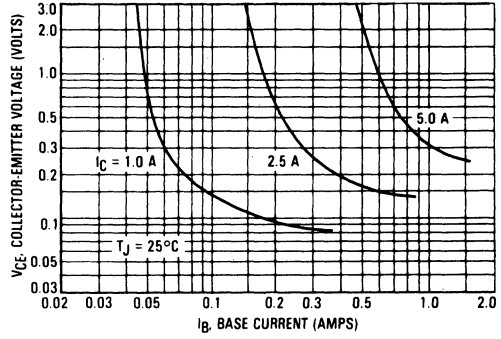


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

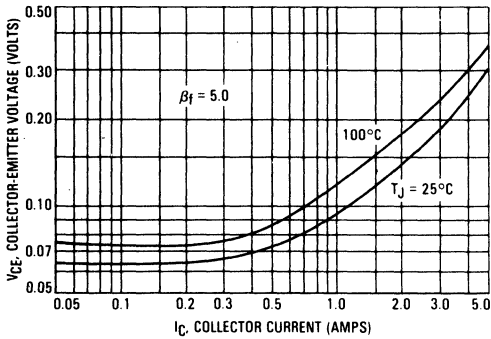


FIGURE 4 — BASE-EMITTER VOLTAGE

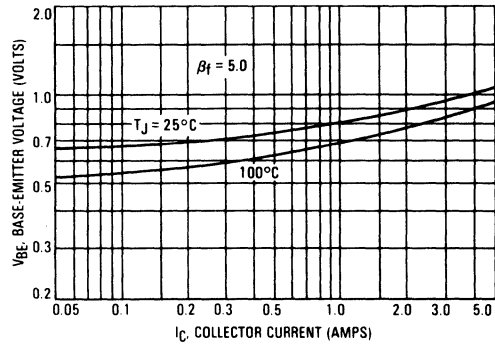


FIGURE 5 — COLLECTOR CUTOFF REGION

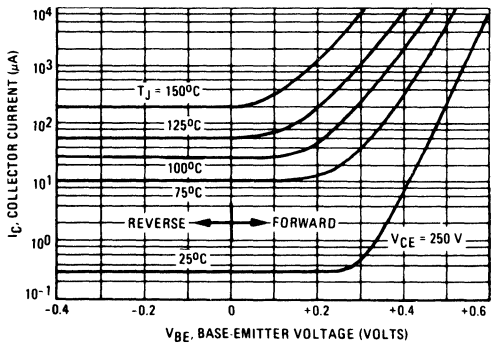


FIGURE 6 — CAPACITANCE

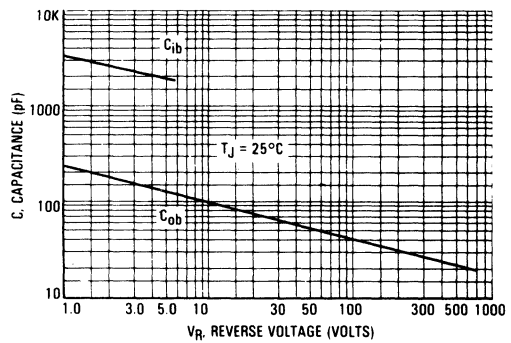


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CE0(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>	<p>Adjust R_1 to obtain I_{B1} For switching and RBSOA, $R_2 = 0$ For $BV_{CE0(sus)}$, $R_2 = \infty$</p>	<p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 80 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = 250 \text{ V}$ R_B adjusted to attain desired I_{B1}	$V_{CC} = 250 \text{ V}$ $R_L = 83 \Omega$ Pulse Width = $10 \mu\text{s}$
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> $t_{r1} \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_{r2} \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

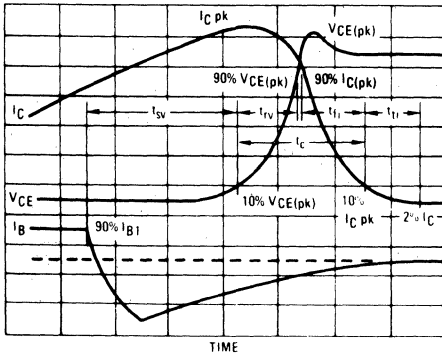
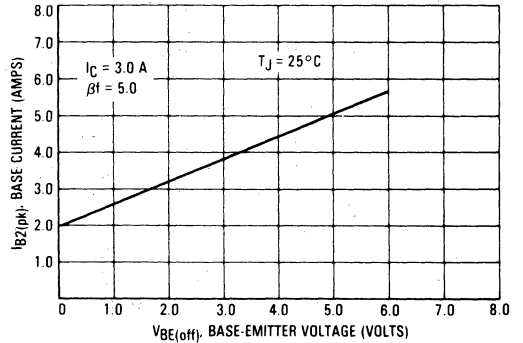


FIGURE 8 - PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

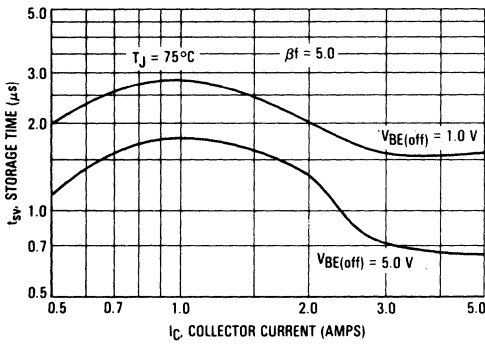


FIGURE 10 — CROSSOVER AND FALL TIMES

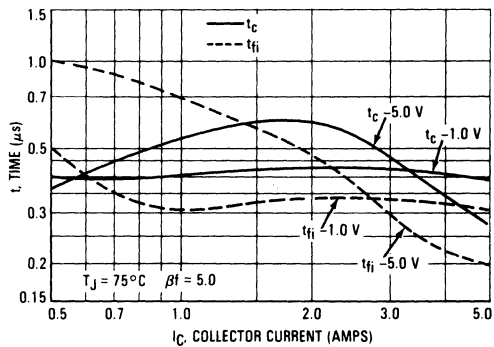
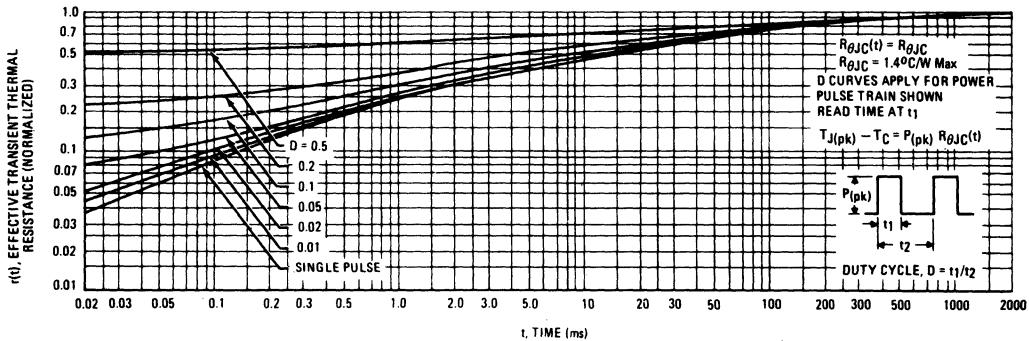


FIGURE 11 — THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

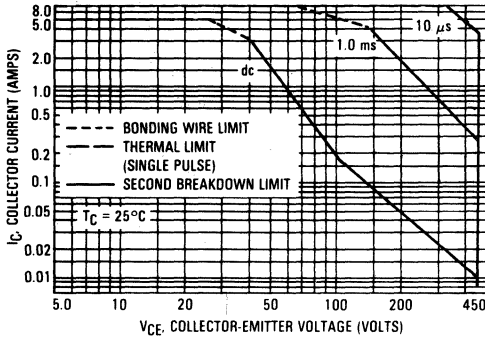


FIGURE 13 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

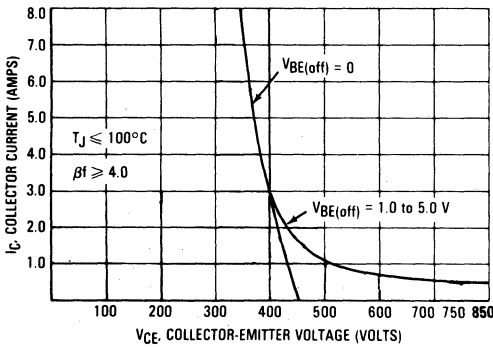
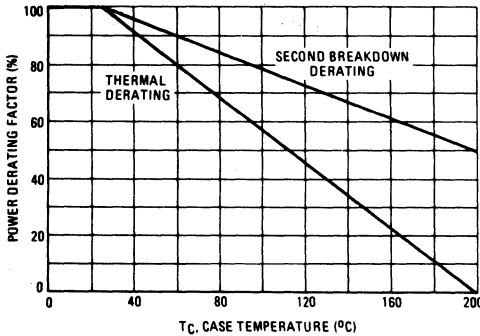


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

3

BUS47
BUS47A

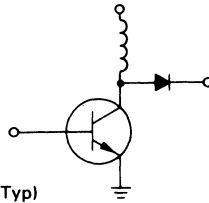
SWITCHMODE II[▲] SERIES
NPN SILICON POWER TRANSISTORS

The BUS 47 and BUS 47A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

60 ns Inductive Fall Time—25°C (Typ)
 120 ns Inductive Crossover Time—25°C (Typ)



Operating Temperature Range –65 to +200°C

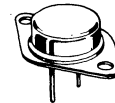
100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents (125°C)

9 AMPERES
NPN SILICON
POWER TRANSISTORS
400 AND 450 VOLTS (BVCEO)
150 WATTS
850 – 1000 V (BVCEES)

Designer's Data for
"Worst Case" Conditions

The Designer's[▲] Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



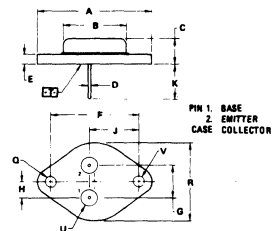
MAXIMUM RATINGS

Rating	Symbol	BUS 47	BUS 47A	Unit
Collector-Emitter Voltage	V _{CEO(sus)}	450	450	Vdc
Collector-Emitter Voltage	V _{CEV}	850	1000	Vdc
Emitter Base Voltage	V _{EB}	7		Vdc
Collector Current – Continuous	I _C	9		Adc
– Peak (1)	I _{CM}	18		
– Overload	I _{OI}	36		
Base Current – Continuous	I _B	5		Adc
– Peak (1)	I _{BM}	10		
Total Power Dissipation – T _C = 25°C	P _D	150		Watts
– T _C = 100°C		85.5		
Derate above 25°C		0.86		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS
 2. [E] IS SEATING PLANE AND DATUM
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D

FOR LEADS:
 [A] [B] [C] [D] [E] [F] [G] [H] [I] [J] [K] [L] [M] [N] [O] [P] [Q] [R] [S] [T] [U] [V] [W] [X] [Y] [Z]

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	77.06	–	0.830
C	0.35	1.92	0.250	0.300
D	0.97	1.06	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15	35.2	1.185	1.385
G	10.92	11.92	0.429	0.470
H	5.48	6.35	0.215	0.250
I	16.89	18.27	0.665	0.719
J	11.18	12.19	0.440	0.480
K	3.81	4.19	0.150	0.165
L	–	26.67	–	1.050
M	4.83	5.33	0.190	0.210
N	3.81	4.19	0.150	0.165

CASE 1-05 TO-3 TYPE

BUS47, BUS47A

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 200 mA, I _B = 0) L = 25 mH	BUS47 BUS47A	V _{CEO(sus)}	400 450	—	—	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 125°C)		I _{CEV}	— —	— —	0.15 1.5	mAdc
Collector Cutoff Current (V _{CE} = Rated V _{CEV} , R _{BE} = 10 Ω)	T _C = 25°C T _C = 125°C	I _{CER}	—	—	0.4 3.0	mAdc
Emitter Cutoff Current (V _{EB} = 5 Vdc, I _C = 0)		I _{EBO}	—	—	0.1	mAdc
Emitter-base breakdown Voltage (I _E = 50 mA - I _C = 0)		V _{VEBO}	7.0	—	—	Vdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figure 12
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 6 Adc, V _{CE} = 5 Vdc) (I _C = 5 Adc, V _{CE} = 5 V)	BUS47 BUS47A	h _{FE}	7	—	—	
Collector-Emitter Saturation Voltage (I _C = 6 Adc, I _B = 1.2 Adc) (I _C = 9 Adc, I _B = 1.8 Adc) (I _C = 6 Adc, I _B = 1.2 Adc, T _C = 100°C) (I _C = 5 Adc, I _B = 1 Adc) (I _C = 8 Adc, I _B = 1.6 Adc) (I _C = 5 Adc, I _B = 1 Adc, T _C = 100°C)	BUS47 BUS47A	V _{CE(sat)}	— — — — — —	— — — — — —	1.5 5.0 2.5 1.5 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I _C = 6 Adc, I _B = 1.2 Adc) (I _C = 6 Adc, I _B = 1.2 Adc, T _C = 100°C) (I _C = 5 Adc, I _B = 1 Adc) (I _C = 5 Adc, I _B = 1 Adc, T _C = 100°C)	BUS47 BUS47A	V _{BE(sat)}	— — — —	— — — —	1.6 1.6 1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 100 KHz)	C _{ob}	—	—	300	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	(V _{CC} = 250 Vdc, I _C = 6 A, I _{B1} = 1.2 A, t _p = 30 μs, Duty Cycle 2, V _{BE(off)} = 5 V)	t _d	—	0.05	0.2	μs
Rise Time		t _r	—	0.5	0.8	
Storage Time		t _s	—	1	2.0	
Fall Time		t _f	—	0.2	0.4	

Inductive Load, Clamped (Table 1)

Storage Time	(I _{C(pk)} = 6 A, I _{B1} = 1.2 A, V _{BE(off)} = 5 V, V _{CE(c1)} = 250 V)	BUS47	(T _C = 25°C)	t _{sv}	—	0.9	—	μs
Fall Time				t _{fi}	—	0.06	—	
Storage Time	(I _{C(pk)} = 5 A, I _{B1} = 1 A)	BUS47A	(T _C = 100°C)	t _{sv}	—	1.0	2.5	
Crossover Time				t _c	—	0.2	0.5	
Fall Time				t _{fi}	—	0.1	0.3	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 - DC CURRENT GAIN

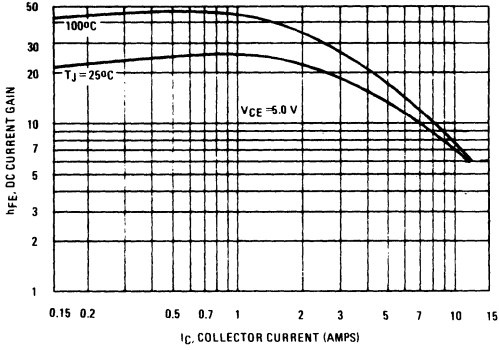


FIGURE 2 - COLLECTOR SATURATION REGION

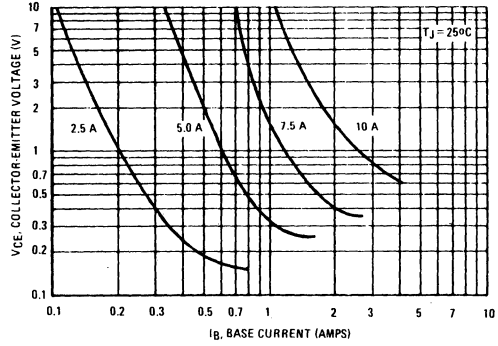


FIGURE 3 - COLLECTOR-EMITTER SATURATION VOLTAGE

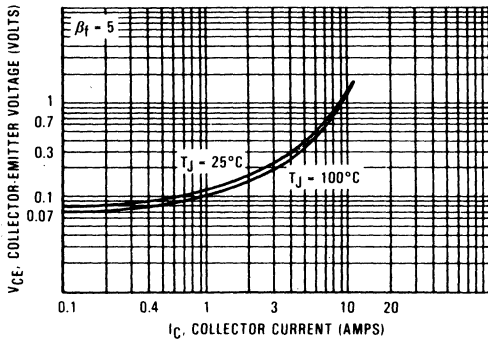


FIGURE 4 - BASE-EMITTER VOLTAGE

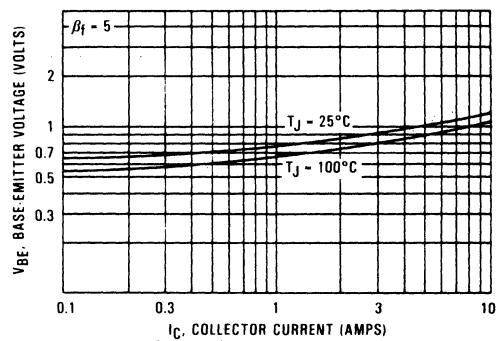


FIGURE 5 - COLLECTOR CUTOFF REGION

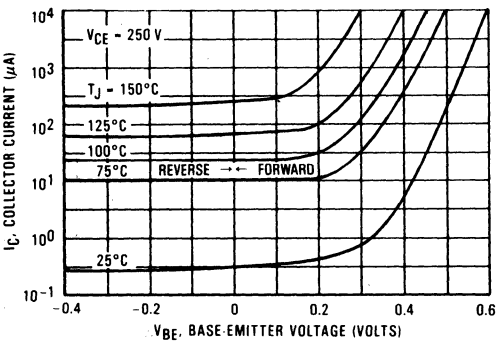


FIGURE 6 - CAPACITANCE

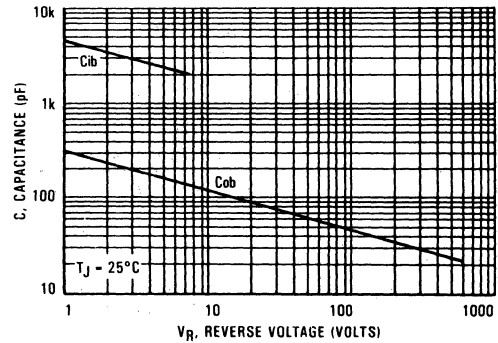
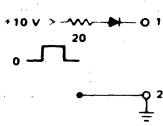
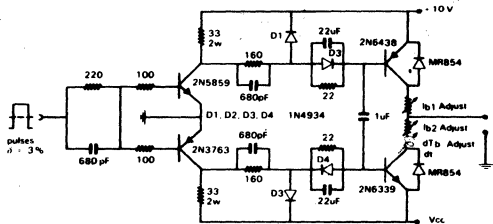
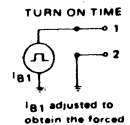
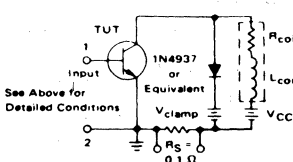
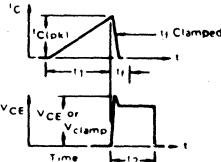
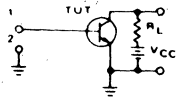


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CEO} (sus)	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>		 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit</p>
CIRCUIT VALUES	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}</p>	<p>V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

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FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

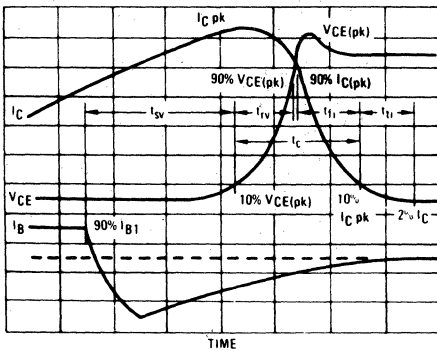
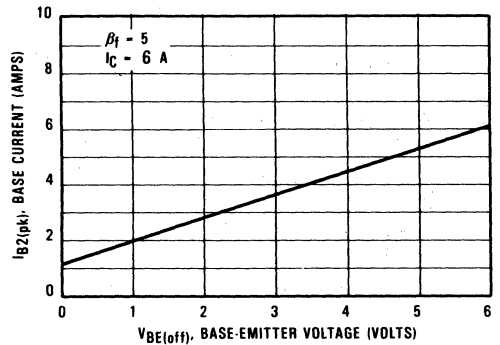


FIGURE 8 - PEAK-REVERSE CURRENT



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An enlarged portion of the inductive switching waveforms

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$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

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INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME

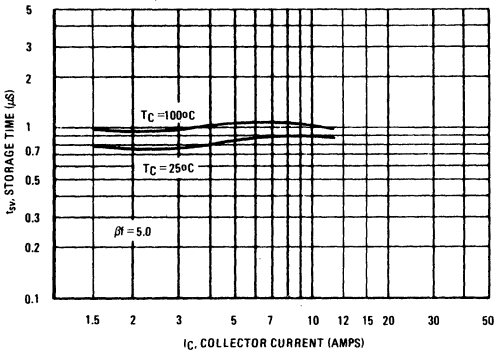


FIGURE 11a – TURN-OFF TIMES vs FORCED I_C

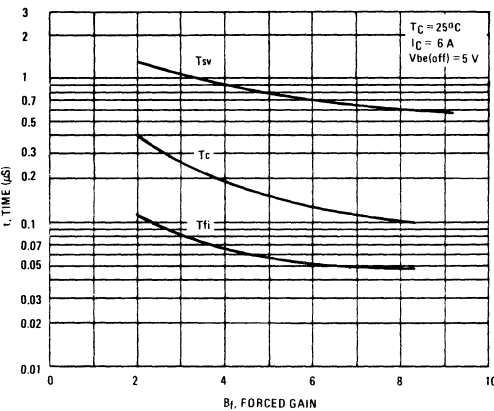


FIGURE 10 – CROSSOVER AND FALL TIMES

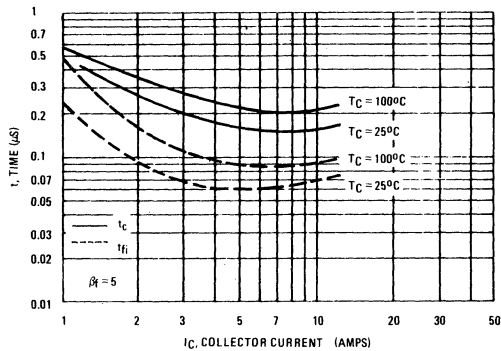
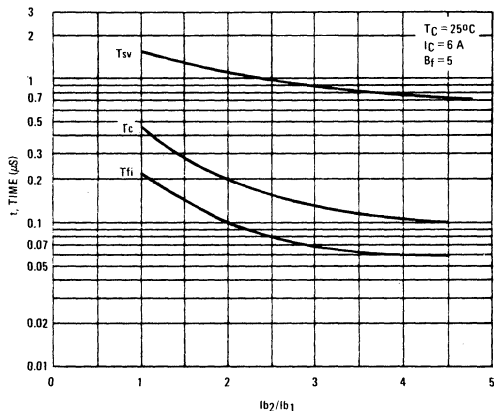


FIGURE 11b – TURN-OFF TIMES vs I_{B2}/I_{B1}



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FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

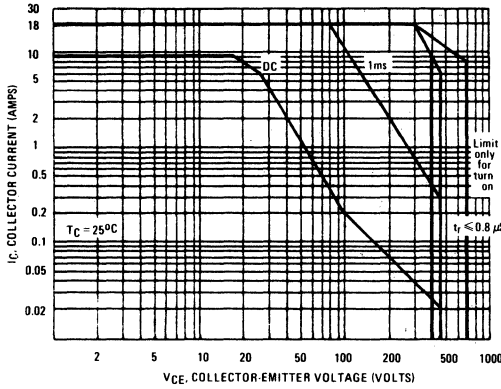


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

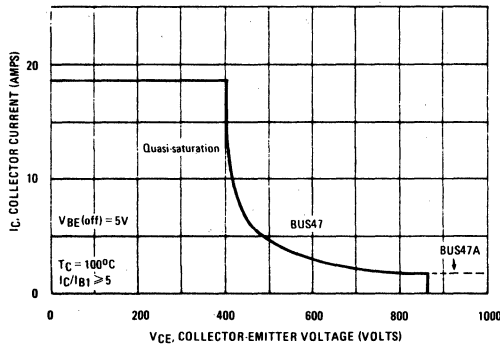
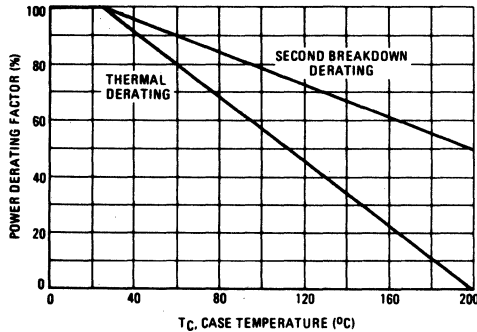


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

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There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

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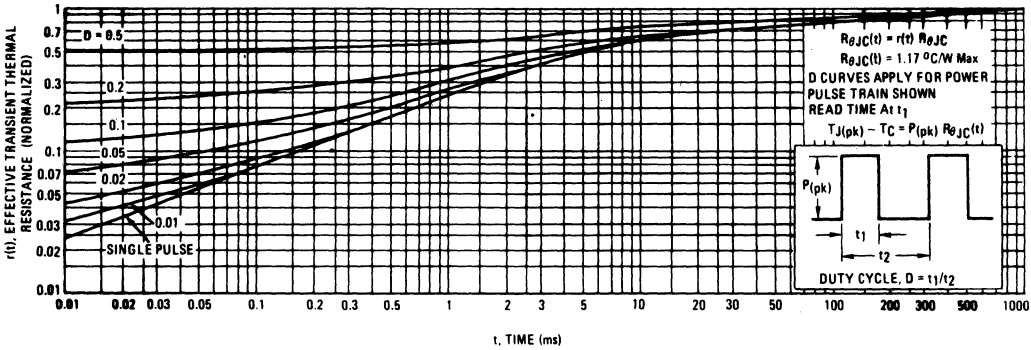
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For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

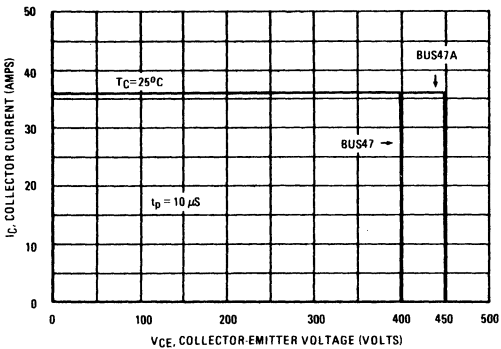
3

FIGURE 15 - THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 - RATED OVERLOAD SAFE OPERATING AREA (OLSOA)



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

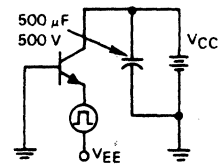
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 17) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 17 -- OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C , t_p



BUS47P
BUS47AP

SWITCHMODE II^A SERIES
NPN SILICON POWER TRANSISTORS

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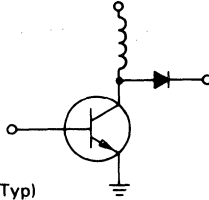
Fast Turn-Off Times

60 ns Inductive Fall Time—25°C (Typ)
 120 ns Inductive Crossover Time—25°C (Typ)

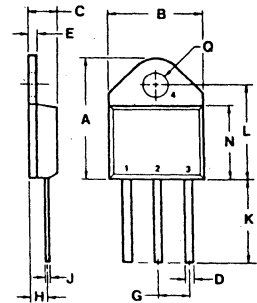
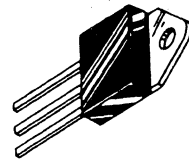
Operating Temperature Range -65 to +175°C

100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents (125°C)



9 AMPERES
NPN SILICON
POWER TRANSISTORS
400 AND 450 VOLTS (BVCEO)
128 WATTS
850 - 1000 V (BVCEES)



STYLE 1:
 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	BUS 47P	BUS 47AP	Unit
Collector-Emitter Voltage	V _{CEO(sus)}	400	450	Vdc
Collector-Emitter Voltage	V _{CEV}	850	1000	Vdc
Emitter Base Voltage	V _{EB}	7		Vdc
Collector Current — Continuous	I _C	9		Adc
— Peak (1)	I _{CM}	18		
— Overload		36		
Base Current — Continuous	I _B	5		Adc
— Peak (1)	I _{BM}	10		
Total Power Dissipation — T _C = 25°C	P _D	128		Watts
— T _C = 100°C		64.5		
Derate above 25°C		0.86		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

BUS47P, BUS47AP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (1)

Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 200\text{ mA}$, $I_B = 0$) $L = 25\text{ mH}$	BUS47P BUS47AP	$V_{CEO(sus)}$	400 450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 125^\circ\text{C}$)		I_{CEV}	—	—	0.15 1.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 10\ \Omega$)	$T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$	I_{CER}	—	—	0.4 3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 5\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	—	0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50\text{ mA}$ - $I_C = 0$)		B_{VEBO}	7.0	—	—	Vdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 6\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 5\text{ Adc}$, $V_{CE} = 5\text{ V}$)	BUS47P BUS47AP	h_{FE}	7	—	—	
Collector-Emitter Saturation Voltage ($I_C = 6\text{ Adc}$, $I_B = 1.2\text{ Adc}$) ($I_C = 9\text{ Adc}$, $I_B = 1.8\text{ Adc}$) ($I_C = 6\text{ Adc}$, $I_B = 1.2\text{ Adc}$, $T_C = 100^\circ\text{C}$) ($I_C = 5\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$) ($I_C = 5\text{ Adc}$, $I_B = 1\text{ Adc}$, $T_C = 100^\circ\text{C}$)	BUS47P BUS47AP	$V_{CE(sat)}$	—	—	1.5 5.0 2.5 1.5 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 6\text{ Adc}$, $I_B = 1.2\text{ Adc}$) ($I_C = 6\text{ Adc}$, $I_B = 1.2\text{ Adc}$, $T_C = 100^\circ\text{C}$) ($I_C = 5\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 5\text{ Adc}$, $I_B = 1\text{ Adc}$, $T_C = 100^\circ\text{C}$)	BUS47P BUS47AP	$V_{BE(sat)}$	—	—	1.6 1.6 1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 100\text{ KHz}$)	C_{ob}	—	—	300	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 6\text{ A}$, $I_{B1} = 1.2\text{ A}$, $t_p = 30\ \mu\text{s}$, Duty Cycle $\leq 2\%$, $V_{BE(off)} = 5\text{ V}$)	t_d	—	0.05	0.2	μs
Rise Time		t_r	—	0.5	0.8	
Storage Time		t_s	—	1	2.0	
Fall Time		t_f	—	0.2	0.4	

Inductive Load, Clamped (Table 1)

Storage Time	$I_{C(pk)} = 6\text{ A}$, $I_{B1} = 1.2\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $V_{CE(c1)} = 250\text{ V}$	BUS47P	$(T_C = 25^\circ\text{C})$	t_{sv}	—	0.9	—	μs
Fall Time				t_{fi}	—	0.06	—	
Storage Time	$I_{C(pk)} = 5\text{ A}$, $I_{B1} = 1\text{ A}$	BUS47AP	$(T_C = 100^\circ\text{C})$	t_{sv}	—	1.0	2.5	
Crossover Time				t_c	—	0.2	0.5	
Fall Time				t_{fi}	—	0.1	0.3	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 - DC CURRENT GAIN

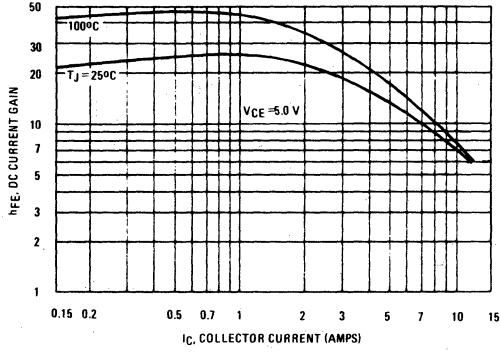


FIGURE 2 - COLLECTOR SATURATION REGION

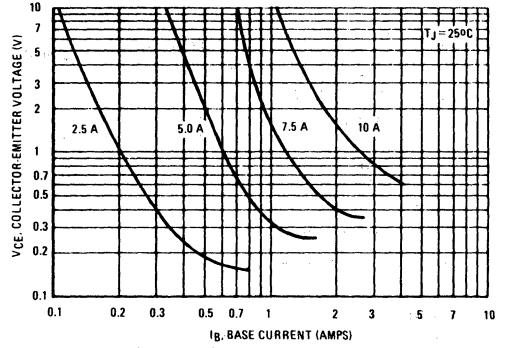


FIGURE 3 - COLLECTOR-EMITTER SATURATION VOLTAGE

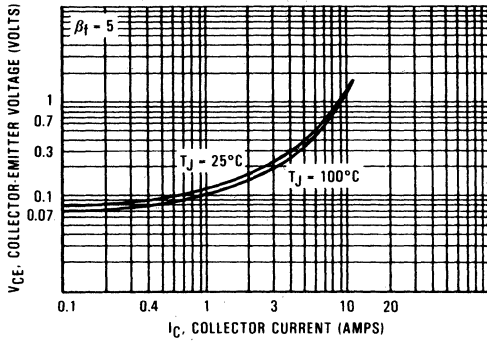


FIGURE 4 - BASE-EMITTER VOLTAGE

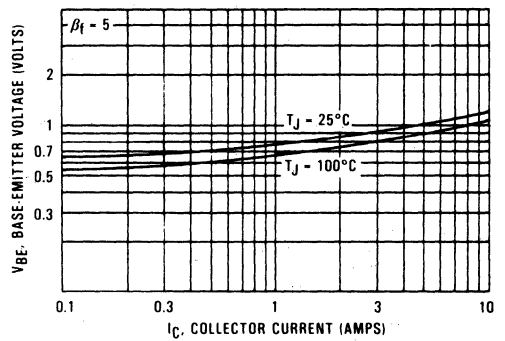


FIGURE 5 - COLLECTOR CUTOFF REGION

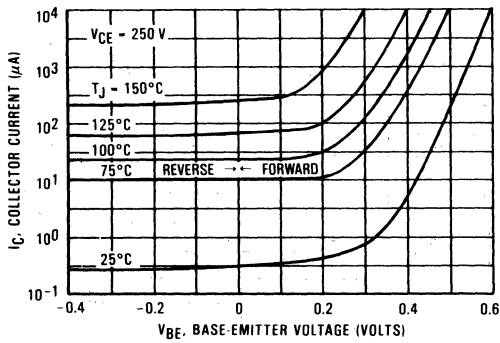
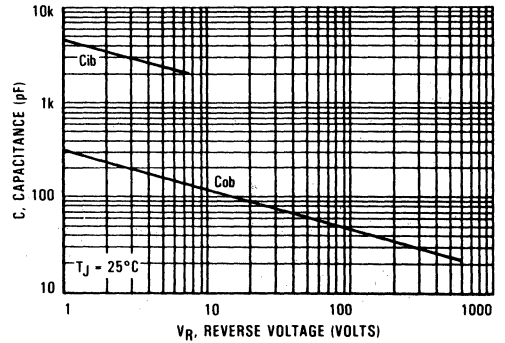


FIGURE 6 - CAPACITANCE



3

TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

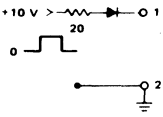
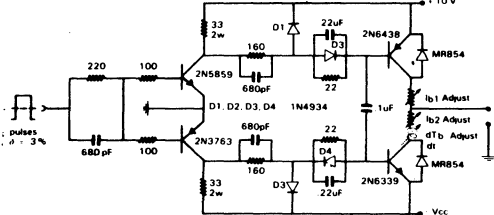
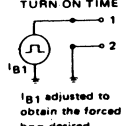
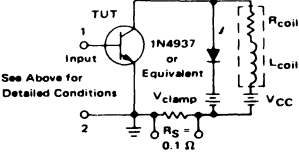
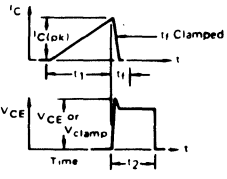
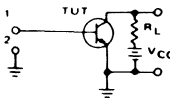
	VCE(sus)	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>		 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 80 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = 250 \text{ V}$ R_B adjusted to attain desired I_{B1}	$V_{CC} = 250 \text{ V}$ $R_L = 83 \Omega$ Pulse Width = $10 \mu\text{s}$
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

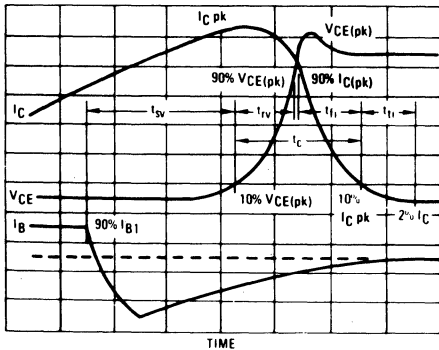
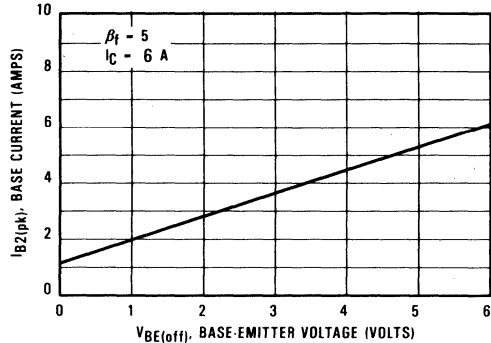


FIGURE 8 - PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
 - t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
 - t_{fi} = Current Fall Time, 90–10% I_C
 - t_{ti} = Current Tail, 10–2% I_C
 - t_c = Crossover Time, 10% V_{clamp} to 10% I_C
- An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME

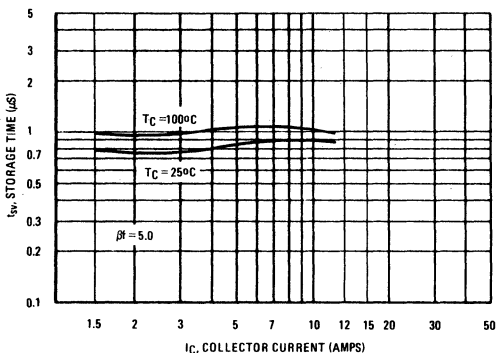


FIGURE 10 – CROSSOVER AND FALL TIMES

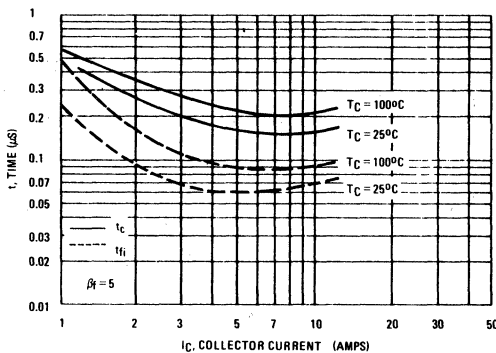


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

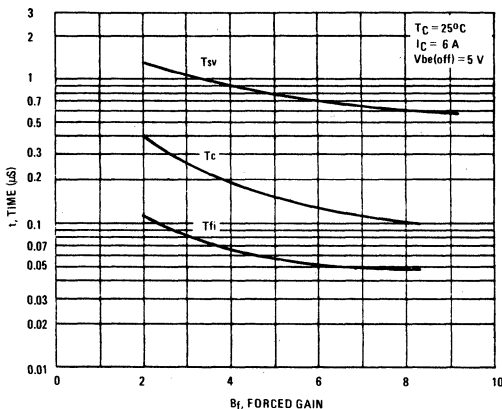
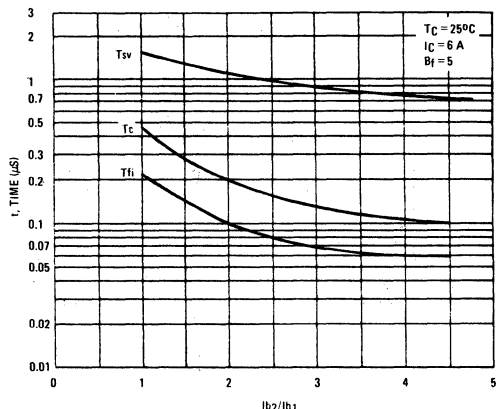


FIGURE 11b – TURN-OFF TIMES vs I_{B2}/I_{B1}



3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

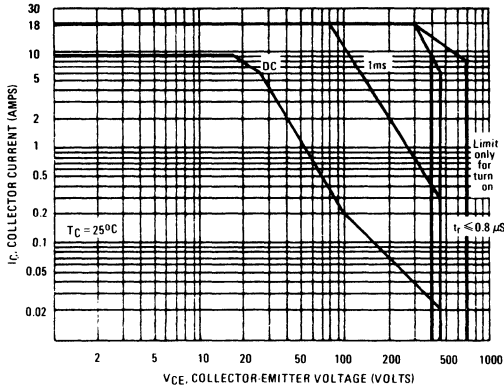


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

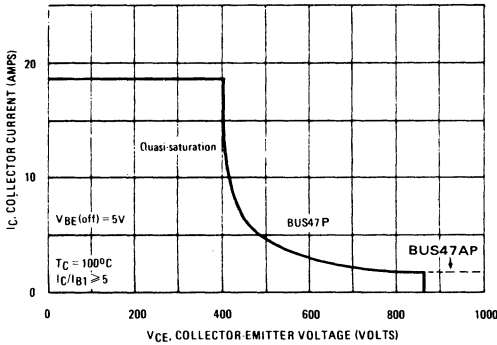
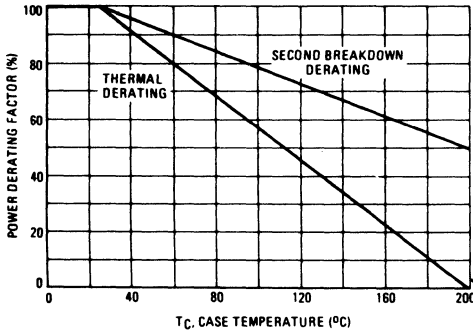


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

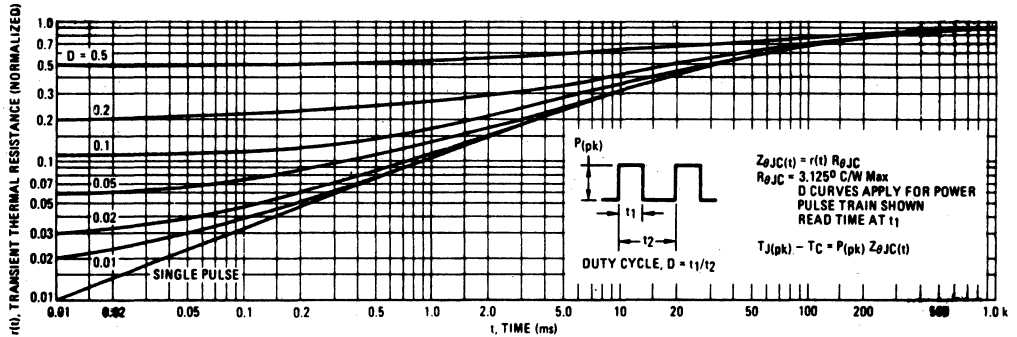
The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

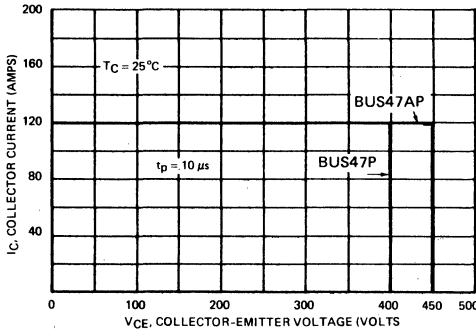
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)



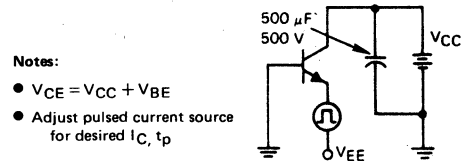
OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 17) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 17 – OVERLOAD SOA TEST CIRCUIT



BUS48
BUS48A

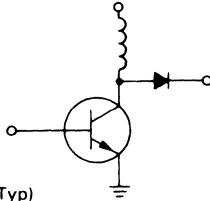
SWITCHMODE II^A SERIES
NPN SILICON POWER TRANSISTORS

The BUS 48 and BUS 48A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

60 ns Inductive Fall Time—25°C (Typ)
 120 ns Inductive Crossover Time—25°C (Typ)



Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

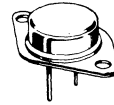
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents (125°C)

15 AMPERES
NPN SILICON
POWER TRANSISTORS

400 and 450 VOLTS (BVCEO)
850 - 1000 VOLTS (BVCEES)
175 WATTS

Designer's Data for
"Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



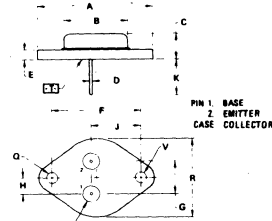
MAXIMUM RATINGS

Rating	Symbol	BUS 48	BUS 48A	Unit
Collector-Emitter Voltage	V _{CEO(sus)}	400	450	Vdc
Collector-Emitter Voltage	V _{CEV}	850	1000	Vdc
Emitter Base Voltage	V _{EB}	7		Vdc
Collector Current - Continuous	I _C	15		Adc
- Peak(1)	I _{CM}	30		
- Overload	I _{OL}	60		
Base Current - Continuous	I _B	5		Adc
- Peak(1)	I _{BM}	20		
Total Power Dissipation - T _C = 25°C	P _D	175		Watts
- T _C = 100°C		100		
Derate above 25°C		1.0		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



- NOTES
- 1 DIMENSIONS Q AND V ARE DATUMS
 - 2 IS SEATING PLANE AND DATUM
 - 3 POSITIONAL TOLERANCE FOR MOUNTING HOLE D
- FOR LEADS
- 4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	33.37	35.50	1.314	1.398
B	27.68	29.81	1.090	1.174
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	1.187 BSC		
G	10.97 BSC	0.430 BSC		
H	3.46 BSC	0.215 BSC		
J	18.89 BSC	0.685 BSC		
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	16.67	0.659		
N	4.83	5.33	0.190	0.210
O	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

BUS48, BUS48A

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (1)

Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 200\text{ mA}$, $I_B = 0$) $L = 25\text{ mH}$	BUS48 BUS48A	$V_{CE(sus)}$	400 450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 125^\circ\text{C}$)		I_{CEV}	—	—	0.2 2.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 10\ \Omega$)	$T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$	I_{CER}	—	—	0.5 3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 5\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	—	0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50\text{ mA}$ - $I_C = 0$)		B_{VEBO}	7.0	—	—	Vdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 10\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 8\text{ Adc}$, $V_{CE} = 5\text{ V}$)	BUS48 BUS48A	h_{FE}	8	—	—	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 15\text{ Adc}$, $I_B = 3\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$, $T_C = 100^\circ\text{C}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$) ($I_C = 12\text{ Adc}$, $I_B = 2.4\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	BUS48 BUS48A	$V_{CE(sat)}$	— — — — — —	— — — — — —	1.5 5.0 2.0 1.5 5.0 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$, $T_C = 100^\circ\text{C}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	BUS48 BUS48A	$V_{BE(sat)}$	— — — —	— — — —	1.6 1.6 1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 100\text{ KHz}$)	C_{ob}	—	—	350	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{B1} = 2.0\text{ A}$, $t_p = 30\ \mu\text{s}$, Duty Cycle $\leq 2\%$, $V_{BE(off)} = 5\text{ V}$)	t_d	—	0.1	0.2	μs
Rise Time		t_r	—	0.4	0.7	
Storage Time		t_s	—	1.3	2.0	
Fall Time		t_f	—	0.2	0.4	

Inductive Load, Clamped (Table 1)

Storage Time	$(I_C(pk) = 10\text{ A}$, $I_{B1} = 2.0\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $V_{CE(c1)} = 250\text{ V}$)	$(T_C = 25^\circ\text{C})$	t_{sv}	—	1.3	—	μs
Fall Time		$(T_C = 25^\circ\text{C})$	t_{fi}	—	0.06	—	
Storage Time	$(I_C(pk) = 10\text{ A}$, $I_{B1} = 2.0\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $V_{CE(c1)} = 250\text{ V}$)	$(T_C = 100^\circ\text{C})$	t_{sv}	—	1.5	2.5	
Crossover Time		$(T_C = 100^\circ\text{C})$	t_c	—	0.3	0.6	
Fall Time		$(T_C = 100^\circ\text{C})$	t_{fi}	—	0.17	0.35	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

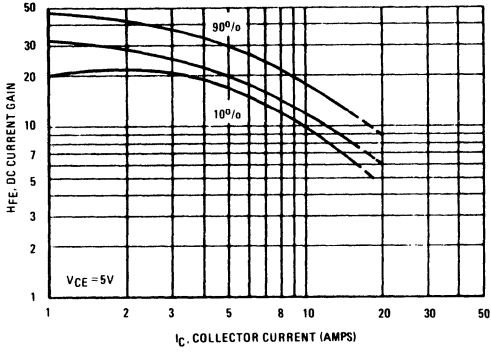


FIGURE 2 – COLLECTOR SATURATION REGION

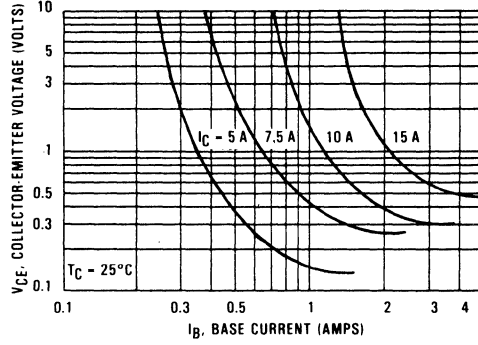


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

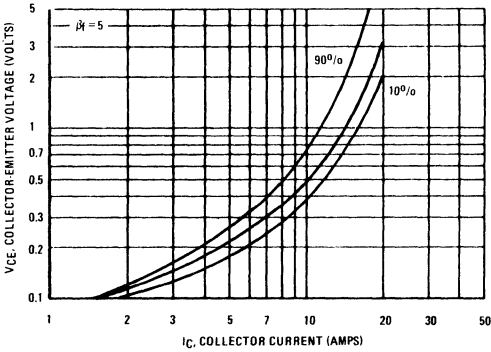


FIGURE 4 – BASE-EMITTER VOLTAGE

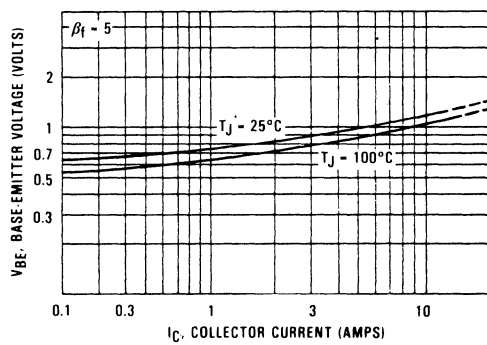


FIGURE 5 – COLLECTOR CUTOFF REGION

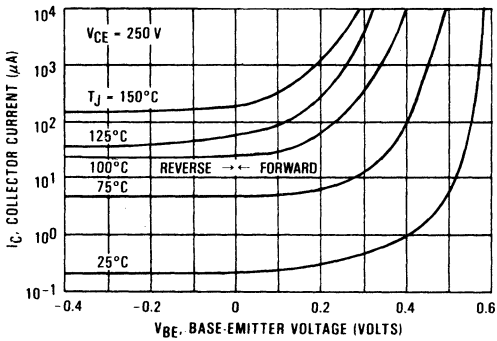


FIGURE 6 – CAPACITANCE

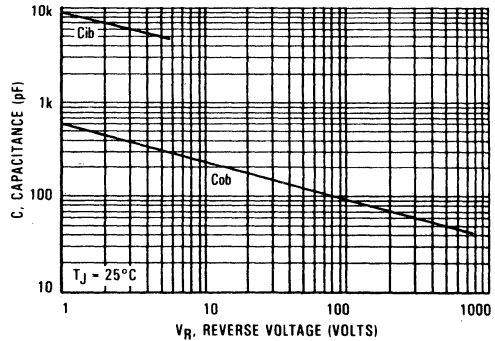


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

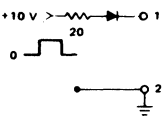
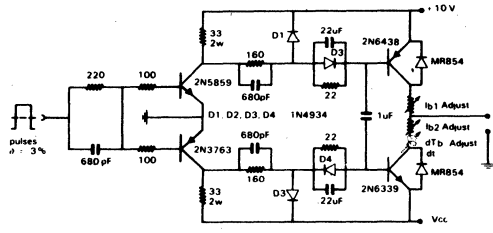
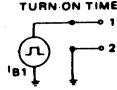
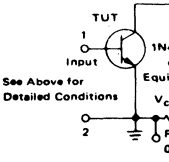
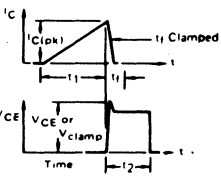
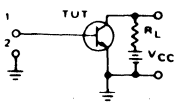
	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>		 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}</p>	<p>V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

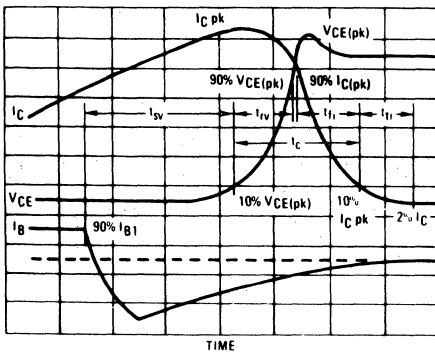
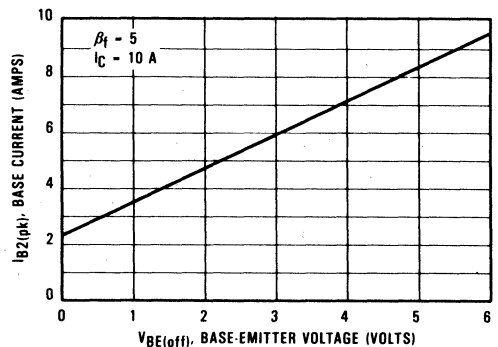


FIGURE 8 - PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
 - t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
 - t_{fi} = Current Fall Time, 90–10% I_C
 - t_{ti} = Current Tail, 10–2% I_C
 - t_c = Crossover Time, 10% V_{clamp} to 10% I_C
- An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME, T_{sv}

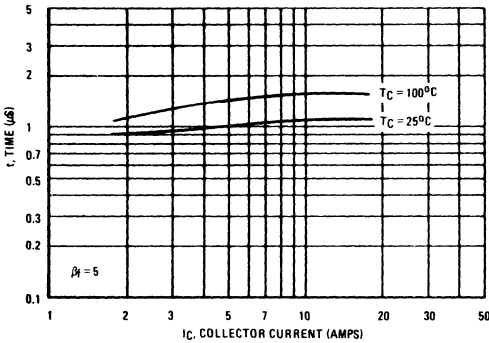


FIGURE 10 – CROSSOVER AND FALL TIMES

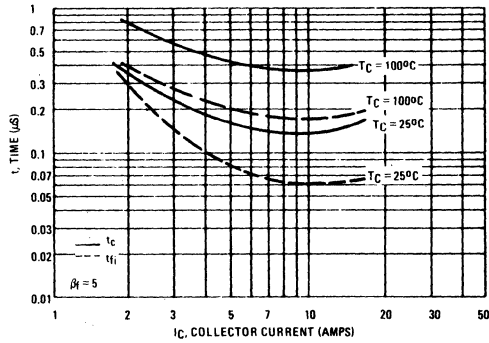


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

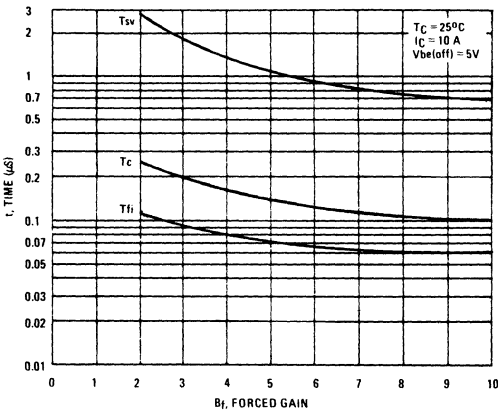
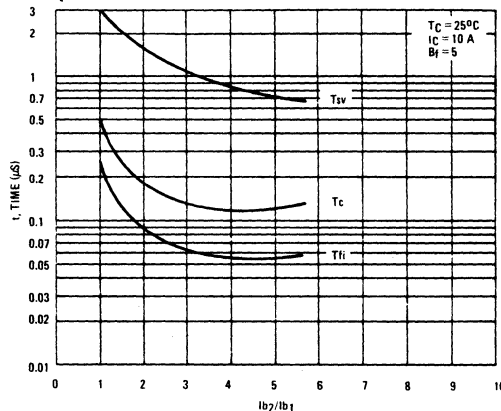


FIGURE 11b – TURN-OFF TIMES vs I_{B2}/I_{B1}



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

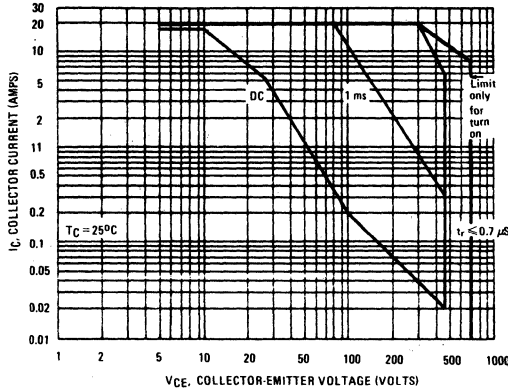


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

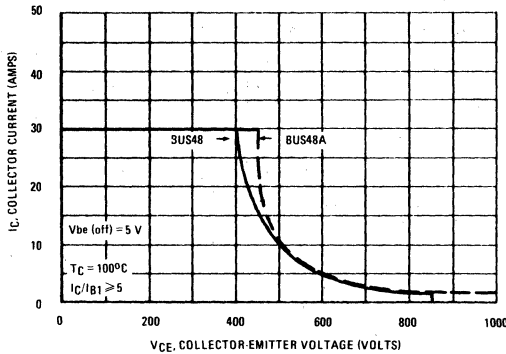
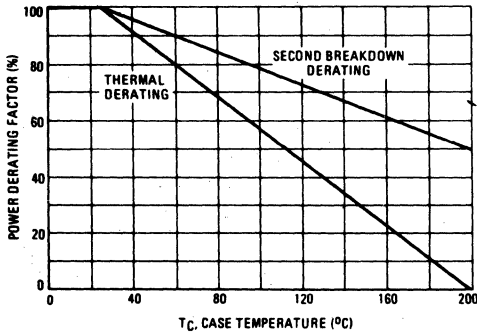


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

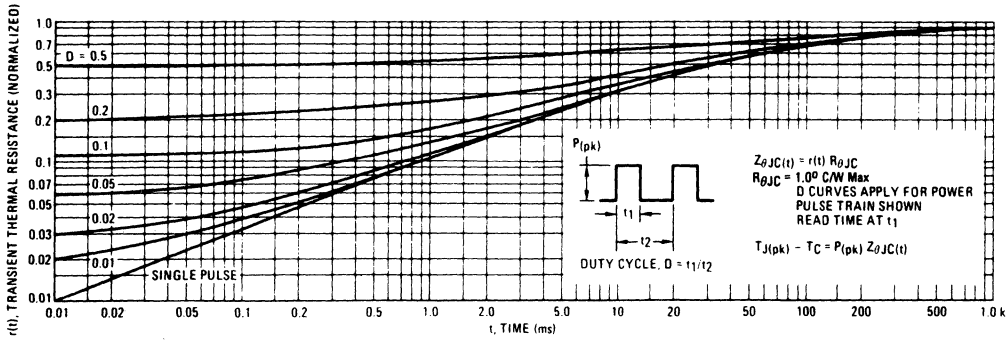
$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

3

FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)

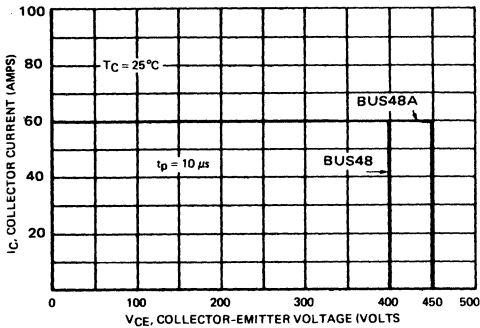
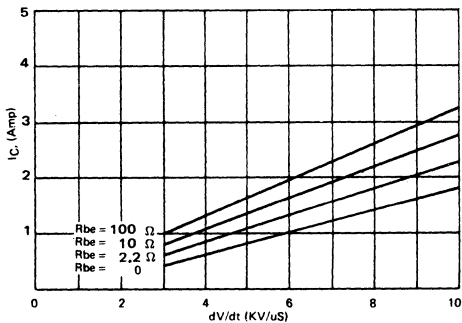


FIGURE 17 – $I_C = f(dV/dt)$



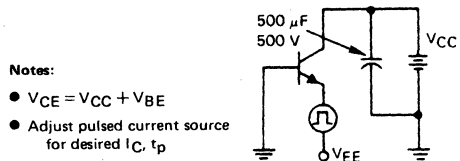
OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 18 – OVERLOAD SOA TEST CIRCUIT



BUS48P
BUS48AP

SWITCHMODE II^A SERIES
NPN SILICON POWER TRANSISTORS

The BUS 48P/BUS 48AP transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

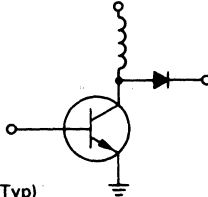
Fast Turn-Off Times

60 ns Inductive Fall Time—25°C (Typ)
 120 ns Inductive Crossover Time—25°C (Typ)

Operating Temperature Range -65 to +175°C

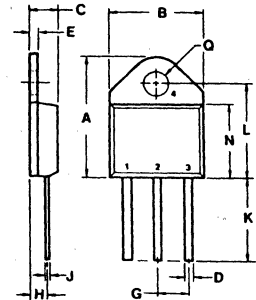
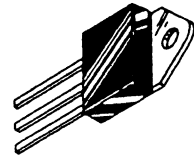
100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents (125°C)



15 AMPERES
NPN SILICON
POWER TRANSISTORS

400 and 450 VOLTS (BVCEO)
850 - 1000 VOLTS (BVCEV)
150 WATTS



STYLE 1:
 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	BUS 48P	BUS 48AP	Unit
Collector-Emitter Voltage	V _{CEO(sus)}	400	450	Vdc
Collector-Emitter Voltage	V _{CEV}	850	1000	Vdc
Emitter Base Voltage	V _{EB}	7		Vdc
Collector Current — Continuous	I _C	15		Adc
— Peak(1)	I _{CM}	30		
— Overload	I _{OI}	60		
Base Current — Continuous	I _B	5		Adc
— Peak (1)	I _{BM}	20		
Total Power Dissipation — T _C = 25°C	P _D	150		Watts
— T _C = 100°C		75		
Derate above 25°C		1.0		
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

BUS48P, BUS48AP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (1)

Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 200\text{ mA}$, $I_B = 0$) $L = 25\text{ mH}$	BUS48P BUS48AP	$V_{CE0(sus)}$	400 450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 125^\circ\text{C}$)		I_{CEV}	— —	— —	0.2 2.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 10\ \Omega$)	$T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$	I_{CER}	—	—	0.5 3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 5\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	—	0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50\text{ mA}$ - $I_C = 0$)		B_{VEBO}	7.0	—	—	Vdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	$RBSOA$	See Figure 13			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 10\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 8\text{ Adc}$, $V_{CE} = 5\text{ V}$)	BUS48 BUS48A	h_{FE}	8	—	—	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 15\text{ Adc}$, $I_B = 3\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$, $T_C = 100^\circ\text{C}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$) ($I_C = 12\text{ Adc}$, $I_B = 2.4\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	BUS48P BUS48AP	$V_{CE(sat)}$	— — — — — —	— — — — — —	1.5 5.0 2.0 1.5 5.0 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$, $T_C = 100^\circ\text{C}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 1.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	BUS48P BUS48AP	$V_{BE(sat)}$	— — — —	— — — —	1.6 1.6 1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 100\text{ KHz}$)	C_{ob}	—	—	350	μF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{B1} = 2.0\text{ A}$, $t_p = 30\ \mu\text{s}$, Duty Cycle 2%, $V_{BE(off)} = 5\text{ V}$)	t_d	—	0.1	0.2	μs
Rise Time		t_r	—	0.4	0.7	
Storage Time		t_s	—	1.3	2.0	
Fall Time		t_f	—	0.2	0.4	

Inductive Load, Clamped (Table 1)

Storage Time	$(I_C(pk) = 10\text{ A}$, $I_{B1} = 2.0\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $V_{CE(c1)} = 250\text{ V}$)	$(T_C = 25^\circ\text{C})$	t_{sv}	—	1.3	—	μs
Fall Time			t_{fi}	—	0.06	—	
Storage Time		$(T_C = 100^\circ\text{C})$	t_{sv}	—	1.5	2.5	
Crossover Time			t_c	—	0.3	0.6	
Fall Time			t_{fi}	—	0.17	0.35	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

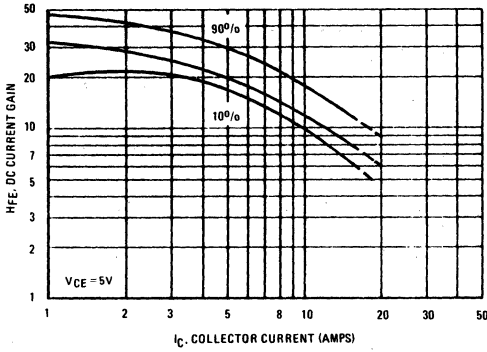


FIGURE 2 – COLLECTOR SATURATION REGION

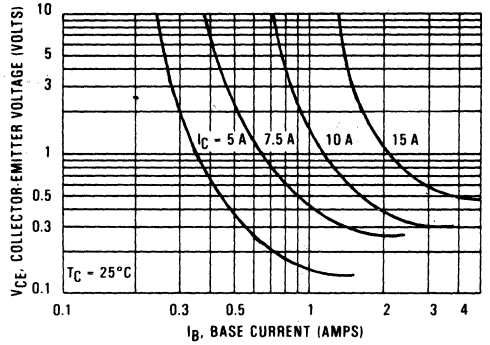


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

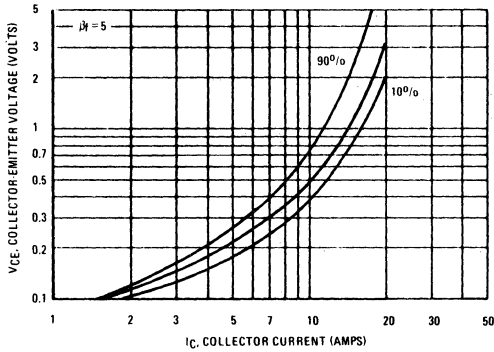


FIGURE 4 – BASE-EMITTER VOLTAGE

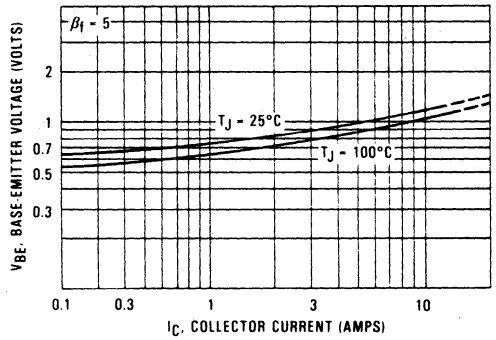


FIGURE 5 – COLLECTOR CUTOFF REGION

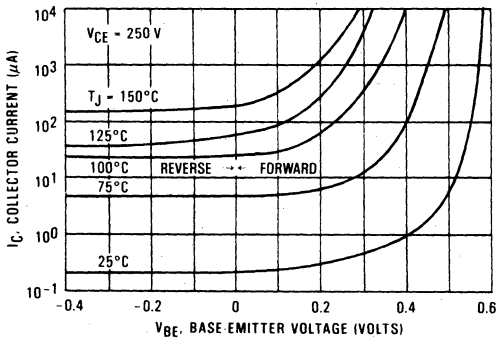
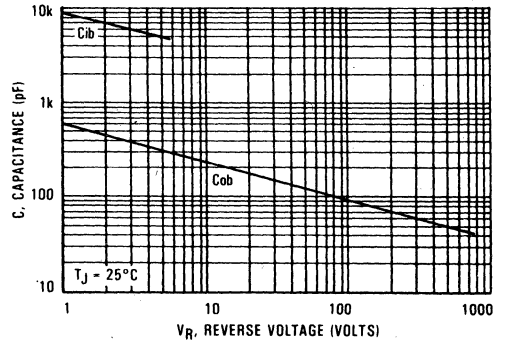


FIGURE 6 – CAPACITANCE



3

TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

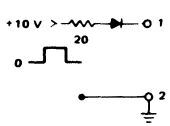
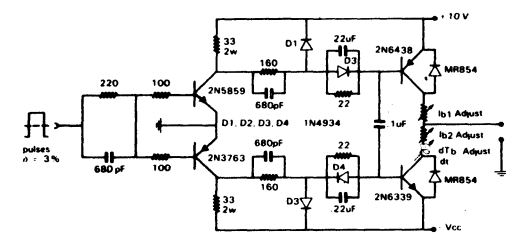
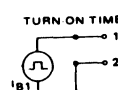
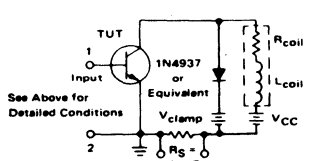
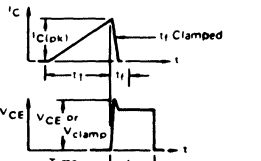
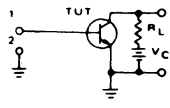
	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
<p>INPUT CONDITIONS</p>  <p>PW Varied to Attain I_C = 100 mA</p>			<p>TURN ON TIME</p>  <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME</p> <p>Use inductive switching driver as the input to the resistive test circuit.</p>
<p>CIRCUIT VALUES</p>	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}</p>	<p>V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs</p>
<p>TEST CIRCUITS</p>	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

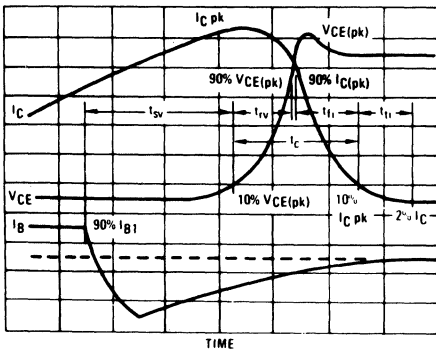
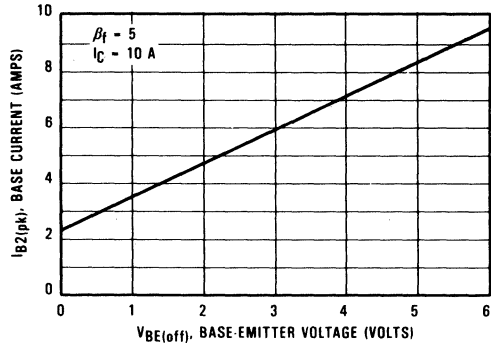


FIGURE 8 - PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
 - t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
 - t_{fi} = Current Fall Time, 90–10% I_C
 - t_{ti} = Current Tail, 10–2% I_C
 - t_c = Crossover Time, 10% V_{clamp} to 10% I_C
- An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME, T_{sv}

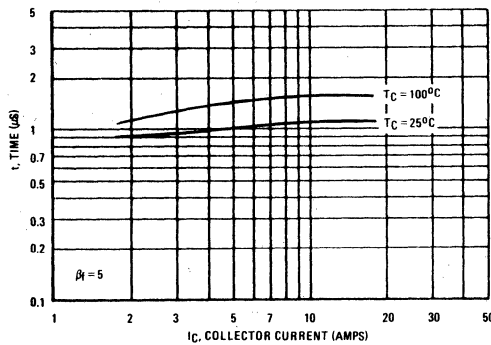


FIGURE 10 – CROSSOVER AND FALL TIMES

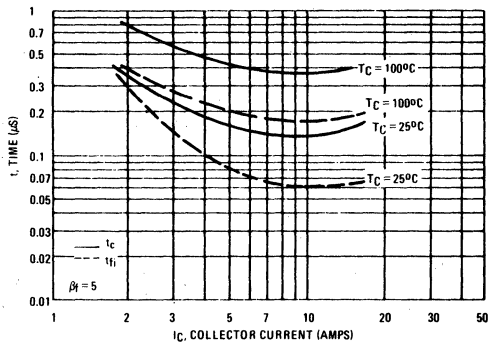


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

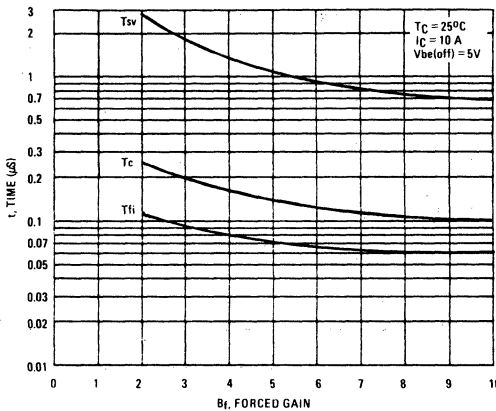
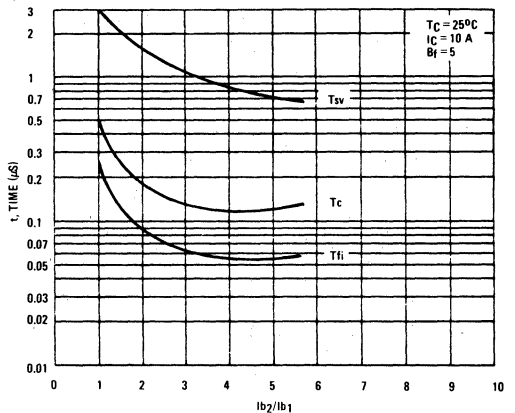


FIGURE 11b – TURN-OFF TIMES vs I_{B2}/I_{B1}



3

BUS48P, BUS48AP

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

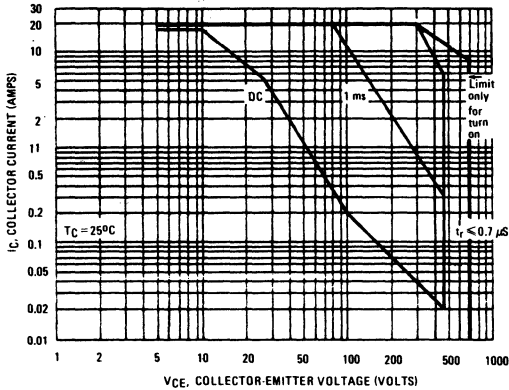


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

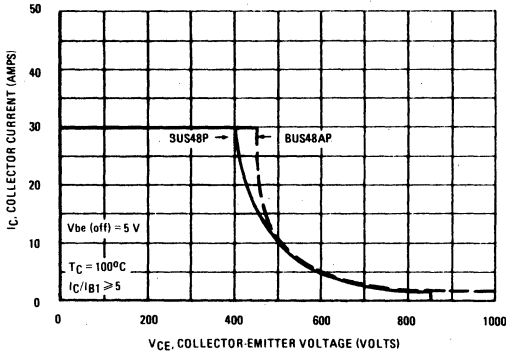
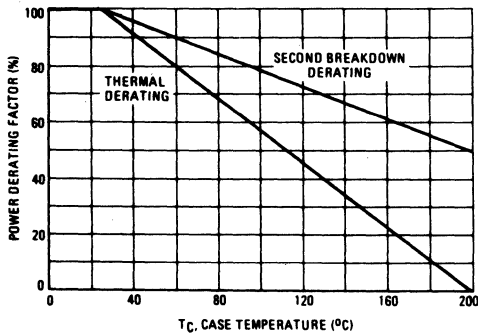


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

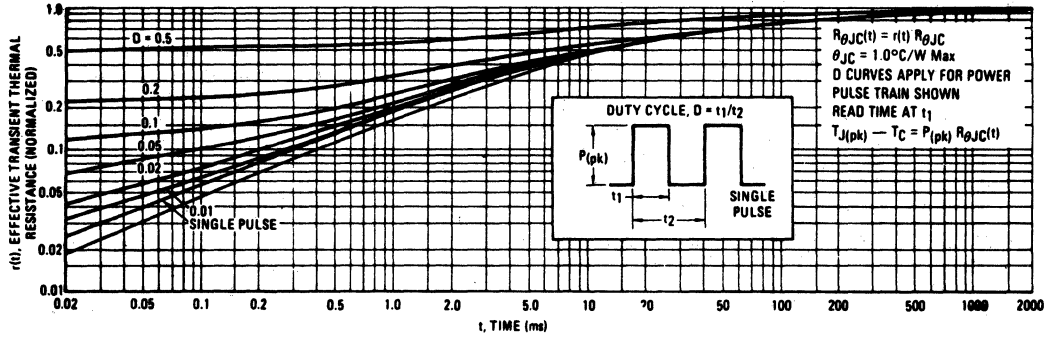
The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)

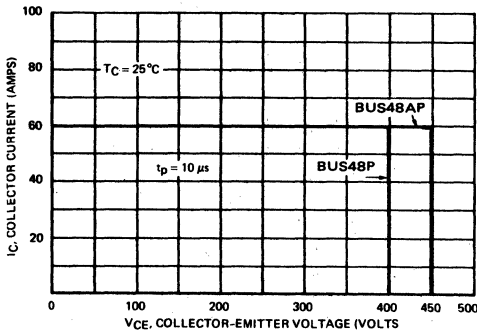
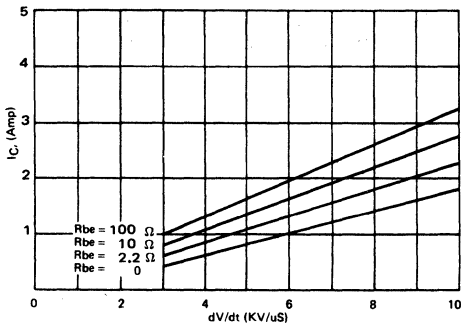


FIGURE 17 – $I_C = f(dV/dt)$



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

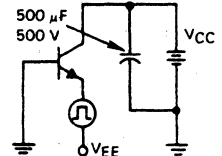
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 18 – OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p



BUS50

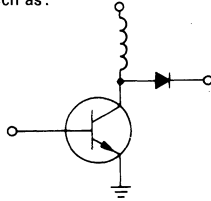
ADVANCED INFORMATION
SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The BUS50 transistor is designed for low voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for battery switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

Fast Turn-Off Times
 300 ns Inductive Fall Time -25°C (Typ)

Operating Temperature Range -65 to +200°C
 100°C Performance Specified for:
 Reverse-Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents (125°C)

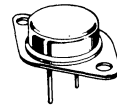


70 AMPERES
NPN SILICON
POWER TRANSISTORS

125 VOLTS (BVCEO)
 350 WATTS
 200 V (BVCEV)

Designer's Data for
"Worst Case" Conditions

The Designers' Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



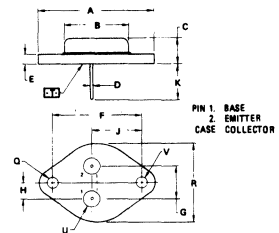
MAXIMUM RATINGS

Rating	Symbol	BUS50	Unit
Collector-Emitter Voltage	$V_{CE(OTUS)}$	125	Vdc
Collector-Emitter Voltage	V_{CEV}	200	Vdc
Emitter Base Voltage	V_{EB}	7	Vdc
Collector Current - Continuous	I_C	70	Adc
- Peak (1)	I_{CM}	140	
- Overload	I_{ol}		
Base Current - Continuous	I_B	20	Adc
- Peak (1)	I_{BM}		
Total Power Dissipation - $T_C = 25^\circ C$	P_D	350	Watts
- $T_C = 100^\circ C$		200	
Derate above 25°C		2	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.



- NOTES:
 1. DIMENSIONS G AND V ARE DATUMS.
 2. \square IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D.
 FOR LEADS
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1975.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.80	0.057	0.063
E	-	3.43	-	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 1-05 TO-3 TYPE

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit.
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 200\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 200\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		.2 2	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 125\text{ V}$)	I_{CEO}		1	mAdc
Emitter Cutoff Current ($V_{EB} = 7\text{ V}$)	I_{EBO}		.2	mAdc

ON CHARACTERISTICS¹

DC Current Gain ($I_C = 5\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 50\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 15		
Collector-Emitter Saturation Voltage ($I_C = 35\text{ A}$, $I_B = 2\text{ A}$) ($I_C = 70\text{ A}$, $I_B = 7\text{ A}$)	$V_{CE(sat)}$		1 1.2	Vdc
Base-Emitter Saturation Voltage ($I_C = 35\text{ A}$, $I_B = 2\text{ A}$) ($I_C = 70\text{ A}$, $I_B = 7\text{ A}$)	$V_{BE(sat)}$		1.8 2	Vdc

SWITCHING CHARACTERISTICS (Resistive Load) t_{on} and (Inductive Load) t_{sv} , t_f

Turn-on Time	$I_C = 70\text{ A}$, $I_{B1} = 7\text{ A}$ $V_{BEoff} = -5\text{ V}$ ($V_{CC} = 125\text{ V}$)	t_{on}	1.2	μs
Storage Time		t_{sv}	1.5	
Fall Time		t_f	.3	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

BUS51 BUS52

ADVANCED INFORMATION SWITCHMODE SERIES NPN SILICON POWER TRANSISTORS

The BUS51 and BUS52 transistors are designed for low voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for battery switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

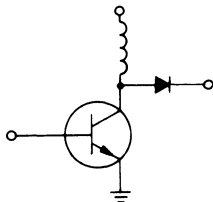
Fast Turn-Off Times

300 ns Inductive Fall Time -25°C (Typ)

Operating Temperature Range -65 to $+200^{\circ}\text{C}$

100 $^{\circ}\text{C}$ Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents (125°C)

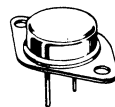


50 & 40 AMPERES NPN SILICON POWER TRANSISTORS

200 and 250 VOLTS (BVCEO)
350 WATTS
300-350 (BVCEC)

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



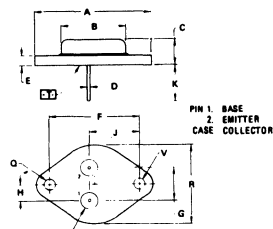
MAXIMUM RATINGS

Rating	Symbol	BUS51	BUS52	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	200	250	Vdc
Collector-Emitter Voltage	V_{CEV}	300	350	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current - Continuous	I_C	50	40	Adc
- Peak (1)	I_{CM}	100	80	
- Overload	I_{OI}			
Base Current - Continuous	I_B	10	16	Adc
- Peak (1)	I_{BM}			
Total Power Dissipation - $T_C = 25^{\circ}\text{C}$	P_D	350		Watts
- $T_C = 100^{\circ}\text{C}$		200		
Derate above 25°C		2		W/ $^{\circ}\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to $+200$		$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.5	$^{\circ}\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: $\frac{1}{8}$ " from Case for 5 Seconds	T_L	275	$^{\circ}\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.



- NOTES
1 DIMENSIONS D AND V ARE DATUMS
2 \square IS SEATING PLANE AND DATUM
3 POSITIONAL TOLERANCE FOR MOUNTING HOLE D
FOR LEADS
4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	38.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	-	3.43	-	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.13	0.440	0.480
Q	3.84	4.08	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 1-05 TO 3

BUS51, BUS52

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS¹					
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 200 mA, I _B = 0, L = 25 mH)	BUS51 BUS52	V _{CE(sus)}	200 250		V _{dc}
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 V _{dc}) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 V _{dc} , T _C = 125°C)		I _{CEV}		0.2 2.0	mAdc
Collector Cutoff Current (V _{CE0} = Rated Value)		I _{CE0}		1	mA
Emitter Cutoff Current (V _{EB} = 7 V _{dc} , I _C = 0)		I _{EB0}		2	mAdc

ON CHARACTERISTICS¹

DC Current Gain (I _C = 5 Adc, V _{CE} = 4 V _{dc}) (I _C = 50 Adc, V _{CE} = 4 V)	BUS51	h _{FE}	20 15		
DC Current Gain (I _C = 5 Adc, V _{CE} = 4 V _{dc}) (I _C = 40 Adc, V _{CE} = 4 V)	BUS52	h _{FE}	20 15		
Collector-Emitter Saturation Voltage (I _C = 30 Adc, I _B = 2 Adc) (I _C = 50 Adc, I _B = 5 Adc)	BUS51	V _{CE(sat)}		1 1.5	V _{dc}
(I _C = 25 Adc, I _B = 2 Adc) (I _C = 40 Adc, I _B = 4 Adc)	BUS52			1 1.5	
Base-Emitter Saturation Voltage (I _C = 30 Adc, I _B = 2 Adc) (I _C = 50 Adc, I _B = 5 Adc)	BUS51	V _{BE(sat)}		1.8 2	V _{dc}
(I _C = 25 Adc, I _B = 2 Adc) (I _C = 40 Adc, I _B = 4 Adc)	BUS52			1.8 2	

SWITCHING CHARACTERISTICS Resistive Load (Table 1)

Turn-on Time	I _{C(pk)} = 50 A I _{B1} = 5 A V _{BE(off)} = 5 V V _{CE(c1)} = 150 V I _{C(pk)} = 40 A I _{B1} = 4 A	BUS51	(T _C = 25°C)	t _{on}	1	μs
			(T _C = 100°C)			
		BUS52				

Inductive Load, Clamped (Table 1)

Storage Time	I _{C(pk)} = 50 A I _{B1} = 5 A V _{BE(off)} = 5 V V _{CE(c1)} = 150 V I _{C(pk)} = 40 A I _{B1} = 4 A	BUS51	(T _C = 25°C)	t _{sv}	2	μs
Fall Time				t _f	.3	
Storage Time		BUS52	(T _C = 100°C)	t _{sv}		
Crossover Time				t _c		
Fall Time				t _f		

¹ Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

SWITCHMODE II[▲] SERIES NPN SILICON POWER TRANSISTORS

The BUS97 and BUS97A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fast time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

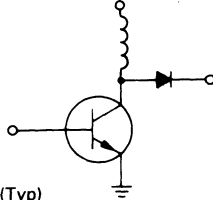
Fast Turn-Off Times

60 ns Inductive Fall Time—25°C (Typ)
120 ns Inductive Crossover Time—25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents (125°C)



BUS97 BUS97A

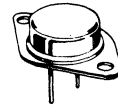
18 AMPERES
NPN SILICON
POWER TRANSISTOR

450 VOLTS

175 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



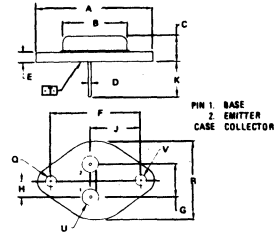
MAXIMUM RATINGS

Rating	Symbol	BUS97	BUS97A	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous	I_C	18		Adc
— Peak (1)	I_{CM}	30		
— Overload	I_{OL}	60		
Base Current — Continuous	I_B	5		Adc
— Peak (1)	I_{BM}	20		
Total Power Dissipation — $T_C = 25^\circ\text{C}$	P_D	175		Watts
— $T_C = 100^\circ\text{C}$		100		
Derate above 25°C		1.0		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES
1 DIMENSIONS Q AND V ARE DATUMS
2 [] IS SEATING PLANE AND DATUM
3 POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	29.31	—	1.150
B	—	21.00	—	0.830
C	6.35	7.62	0.250	0.300
D	0.91	1.00	0.036	0.040
E	1.00	1.78	0.039	0.070
F	30.15	BSC	1.187	BSC
G	19.92	BSC	0.785	BSC
H	14.46	BSC	0.570	BSC
J	16.80	BSC	0.661	BSC
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	26.67	—	1.050
N	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

BUS97, BUS97A

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (1)

Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 200\text{ mA}$, $I_B = 0$) $L = 25\text{ mH}$	BUS97 BUS97A	$V_{CEO(sus)}$	400 450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 125^\circ\text{C}$)		I_{CEV}	—	—	0.2 2.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 10\ \Omega$)	$T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$	I_{CER}	—	—	0.5 3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 5\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	—	0.1	mAdc
Emitter-base breakdown Voltage ($I_E = 50\text{ mA}$ - $I_C = 0$)			7			Vdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 12\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 10\text{ A}$, $V_{CE} = 5\text{ V}$)	BUS97 BUS97A	h_{FE}	7	—	—	
Collector-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 2.4\text{ A}$) ($I_C = 18\text{ A}$, $I_B = 6\text{ A}$) ($I_C = 12\text{ A}$, $I_B = 2.4\text{ A}$, $T_C = 100^\circ\text{C}$) ($I_C = 10\text{ A}$, $I_B = 2\text{ A}$) ($I_C = 15\text{ A}$, $I_B = 3\text{ A}$) ($I_C = 10\text{ A}$, $I_B = 2\text{ A}$, $T_C = 100^\circ\text{C}$)	BUS97 BUS97A	$V_{CE(sat)}$	— — — — — —	— — — — — —	1.5 3 2.5 1.5 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 12\text{ Adc}$, $I_B = 2.4\text{ Adc}$) ($I_C = 12\text{ Adc}$, $I_B = 2.4\text{ Adc}$, $T_C = 100^\circ\text{C}$) ($I_C = 10\text{ A}$, $I_B = 2\text{ Adc}$) ($I_C = 10\text{ A}$, $I_B = 2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	BUS97 BUS97A	$V_{BE(sat)}$	— — — —	— — — —	1.6 1.6 1.6 1.6	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 100\text{ KHz}$)	C_{ob}	—	—	350	pF
--	----------	---	---	-----	----

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 12\text{ A}$, $I_{B1} = 2.4\text{ A}$, $t_D = 30\ \mu\text{s}$, Duty Cycle $\leq 2\%$, $V_{BE(off)} = 5\text{ V}$)	t_d	—	0.1	0.2	μs
Rise Time		t_r	—	0.4	0.7	
Storage Time		t_s	—	1.3	2.0	
Fall Time		t_f	—	0.2	0.4	

Inductive Load, Clamped (Table 1)

Storage Time	$(I_C(pk) = 12\text{ A})$ BUS97 $I_{B1} = 2.4\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $V_{CE(C1)} = 250\text{ V}$	$(T_C = 25^\circ\text{C})$	t_{sv}	—	1.3	—	μs
Fall Time			t_{fi}	—	0.06	—	
Storage Time	$(I_C(pk) = 10\text{ A})$ BUS97A $I_{B1} = 2\text{ A}$	$(T_C = 100^\circ\text{C})$	t_{sv}	—	1.5	2.5	
Crossover Time			t_c	—	0.3	0.6	
Fall Time			t_{fi}	—	0.17	0.35	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

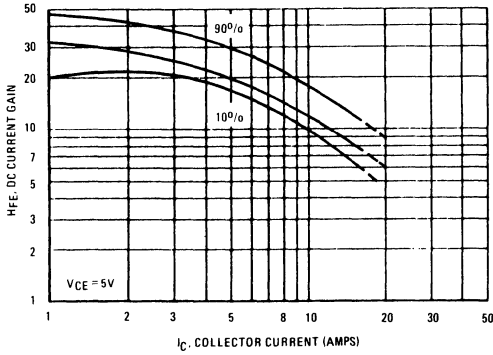


FIGURE 2 – COLLECTOR SATURATION REGION

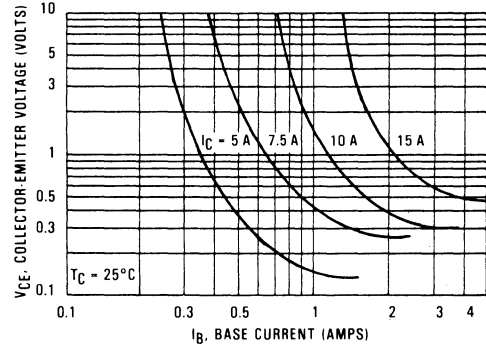


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

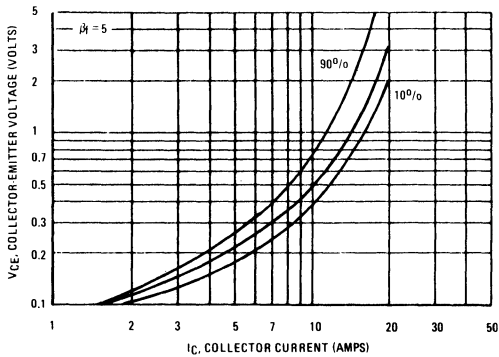


FIGURE 4 – BASE-EMITTER VOLTAGE

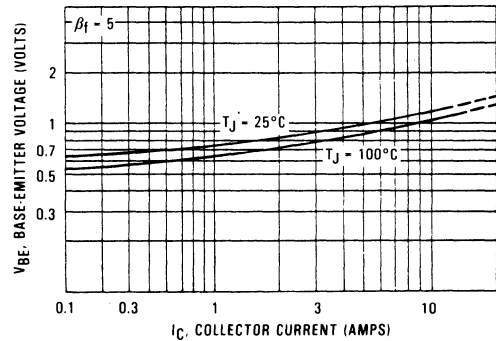


FIGURE 5 – COLLECTOR CUTOFF-REGION

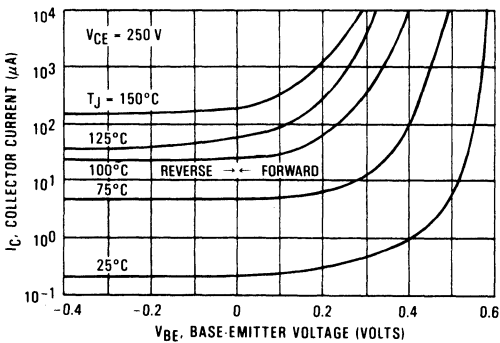


FIGURE 6 – CAPACITANCE

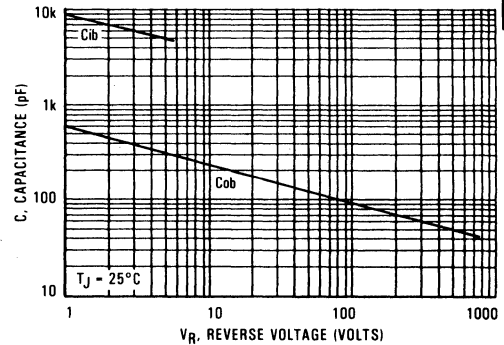


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

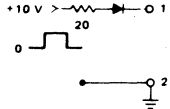
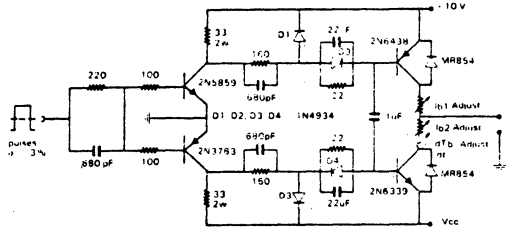
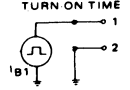
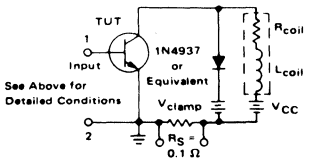
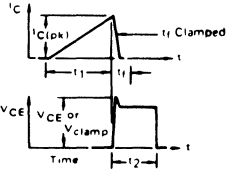
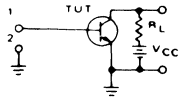
	V _{CEO} (sus)	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>		 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}</p>	<p>V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions R_S = 0.1 Ω</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

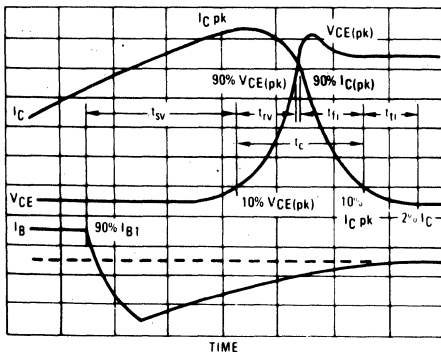
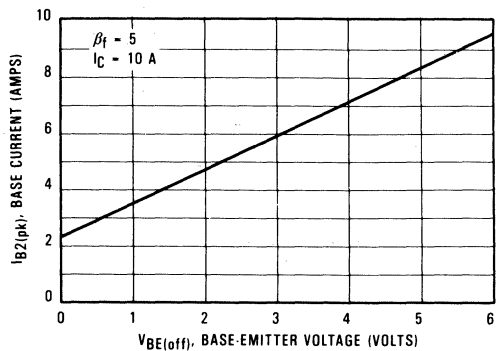


FIGURE 8 - PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 – STORAGE TIME, T_{sv}

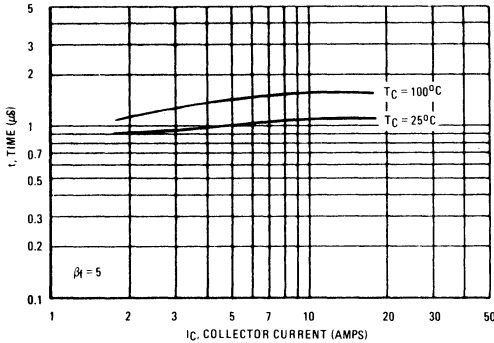


FIGURE 10 – CROSSOVER AND FALL TIMES

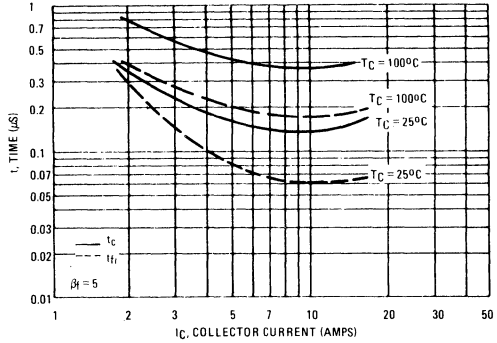


FIGURE 11a – TURN-OFF TIMES vs FORCED GAIN

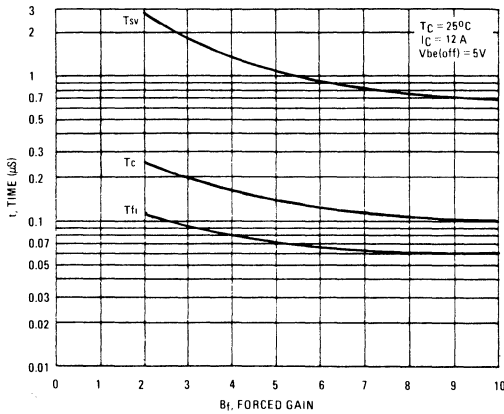
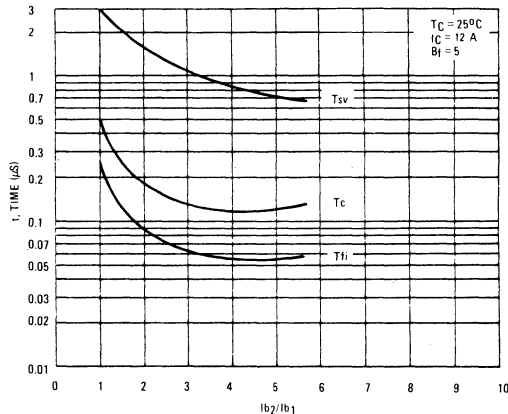


FIGURE 11b – TURN-OFF TIMES vs I_{b2}/I_{b1}



3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

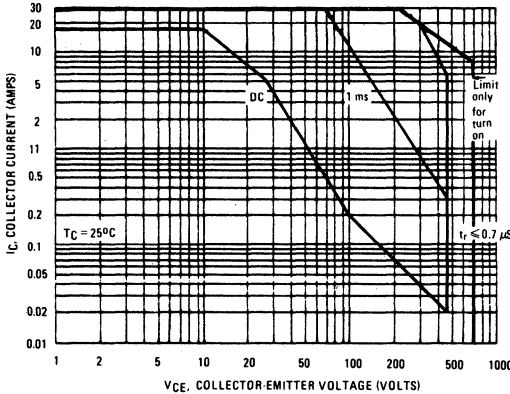


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

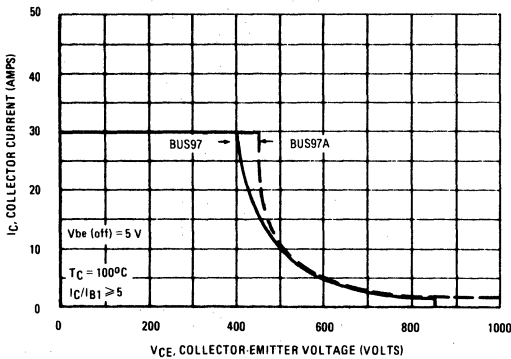
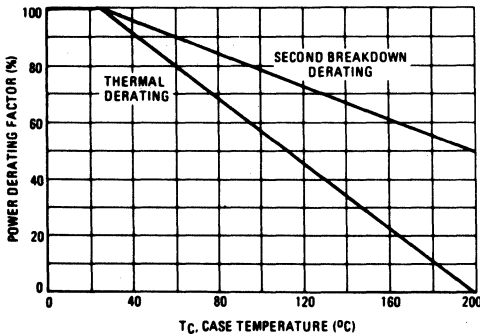


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

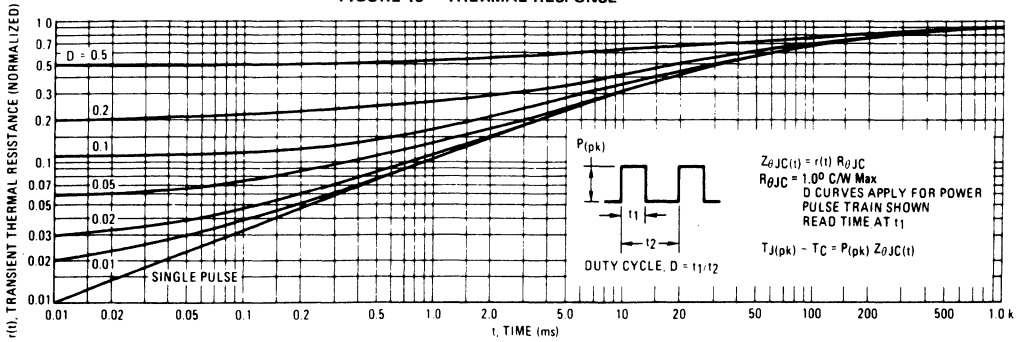
$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

3

FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)

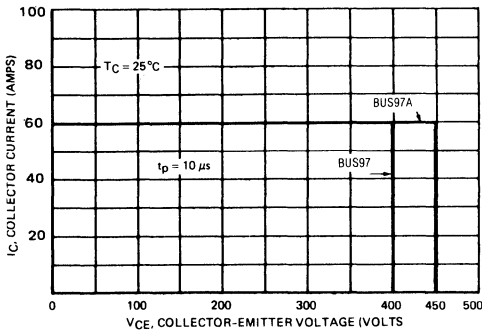
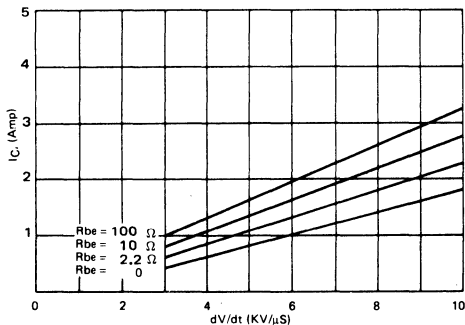


FIGURE 17 – $I_C = f(dV/dt)$



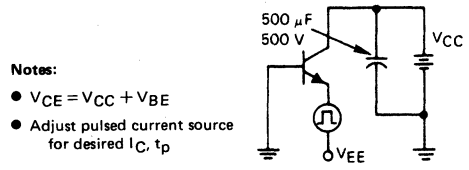
OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 18 – OVERLOAD SOA TEST CIRCUIT



SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The BUS 98 and BUS 98A transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

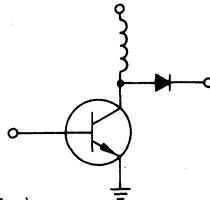
Fast Turn-Off Times

60 ns Inductive Fall Time – 25°C (Typ)
 120 ns Inductive Crossover Time – 25°C (Typ)

Operating Temperature Range – 65 to + 200°C

100°C Performance Specified for :

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents (125°C)



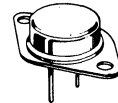
30 AMPERES

NPN SILICON
POWER TRANSISTORS

400 AND 450 VOLTS (BVCEO)
250 WATTS
850 – 1000 V (BVCEES)

Designer's Data for
"Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



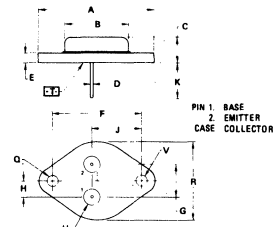
MAXIMUM RATINGS

Rating	Symbol	BUS 98	BUS98A	Unit
Collector-Emitter Voltage	V _{CEO(sus)}	400	450	Vdc
Collector-Emitter Voltage	V _{CEV}	850	1000	Vdc
Emitter Base Voltage	V _{EB}	7		Vdc
Collector Current – Continuous	I _C	30		Adc
– Peak (1)	I _{CM}	60		
– Overload	I _{ol}	120		
Base Current – Continuous	I _B	10		Adc
– Peak (1)	I _{BM}	30		
Total Power Dissipation – T _C = 25°C	P _D	250		Watts
Derate above 25°C		1.42		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	– 65 to + 200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. [T] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q.
 ⌀ ± 0.13 (0.005) Ⓢ T V Ⓢ
 FOR LEADS
 ⌀ ± 0.13 (0.005) Ⓢ T V Ⓢ Ⓢ
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1972.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3

BUS98, BUS98A

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (IC = 200 mA, IB = 0) L = 25 mH	BUS98 BUS98A	VCEO(sus) 400 450	— —	— —	Vdc
Collector Cutoff Current (VCEV = Rated Value, VBE(off) = 1.5 Vdc) (VCEV = Rated Value, VBE(off) = 1.5 Vdc, TC = 125°C)		ICEV	— —	— 4.0	mAdc
Collector Cutoff Current (VCE = Rated VCEV, RBE = 10 Ω) TC = 25°C TC = 125°C		ICER	— —	— 6.0	mAdc
Emitter Cutoff Current (VEB = 7 Vdc, IC = 0)		IEBO		0.2	mAdc
Emitter-base breakdown Voltage (IE = 100 mA - IC = 0)		VEBO	7.0		Vdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	IS/b		See Figure 12	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 13	

ON CHARACTERISTICS(1)

DC Current Gain (IC = 20 Adc, VCE = 5 Vdc) (IC = 16 Adc, VCE = 5 V)	BUS98 BUS98A	hFE	8	—	—
Collector-Emitter Saturation Voltage (IC = 20 Adc, IB = 4 Adc) (IC = 30 Adc, IB = 8 Adc) (IC = 20 Adc, IB = 4 Adc, TC = 100°C) (IC = 16 Adc, IB = 3.2 Adc) (IC = 24 Adc, IB = 5 Adc) (IC = 16 Adc, IB = 3.2 Adc, TC = 100°C)	BUS98 BUS98A	VCE(sat)	— — — — — —	— — — — — —	1.5 3.5 2.0 1.5 5.0 2.0
Base-Emitter Saturation Voltage (IC = 20 Adc, IB = 4 Adc) (IC = 20 Adc, IB = 4 Adc, TC = 100°C) (IC = 16 Adc, IB = 3.2 Adc) (IC = 16 Adc, IB = 3.2 Adc, TC = 100°C)	BUS98 BUS98A	VBE(sat)	— — — —	— — — —	1.6 1.6 1.6 1.6

DYNAMIC CHARACTERISTICS

Output Capacitance (VCB = 10 Vdc, IE = 0, ftest = 100 khz)	Cob	—	—	700	pF
---	-----	---	---	-----	----

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	(VCC = 250 Vdc, IC = 20A, IB1 = 4.0 A, tp = 30 μs, Duty Cycle ≤ 2%, VBE(off) = 5 V) (for BUS98A : IC = 16A, IB1 = 3.2A)	td	—	0.1	0.2	μs
Rise Time		tr	—	0.4	0.7	
Storage Time		ts	—	1.55	2.3	
Fall Time		tf	—	0.2	0.4	

Inductive Load, Clamped (Table 1)

Storage Time	IC(pk) = 20A IB1 = 4A] (BUS98)	(TC = 25°C)	tsv	—	1.55	—	μs
Fall Time			tfi	—	0.06	—	
Storage Time	VBE(off) = 5 V, VCE(c1) = 250 V) IC(pk) = 16A IB1 = 3.2A] (BUS98A)	(TC = 100°C)	tsv	—	1.8	2.8	
Crossover Time			tc	—	0.3	0.6	
Fall Time			tfi	—	0.17	0.35	

(1) Pulse Test : PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

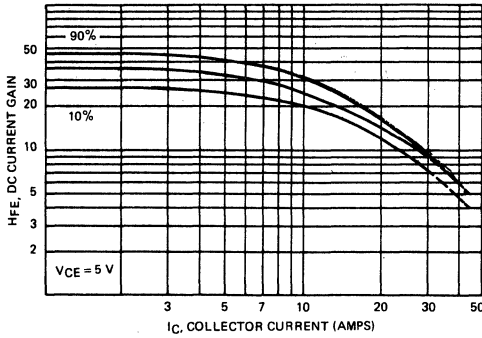


FIGURE 2 — COLLECTOR SATURATION REGION

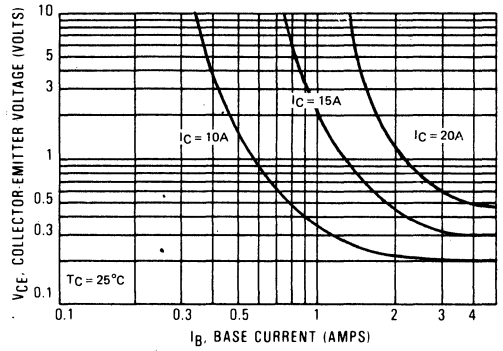


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

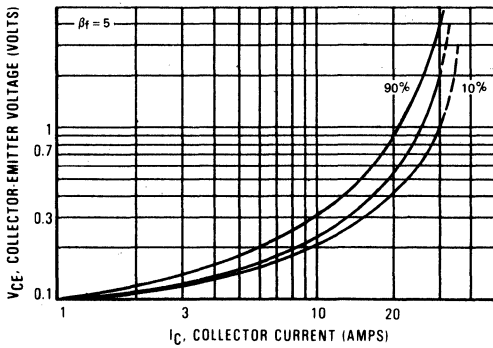


FIGURE 4 — BASE-EMITTER VOLTAGE

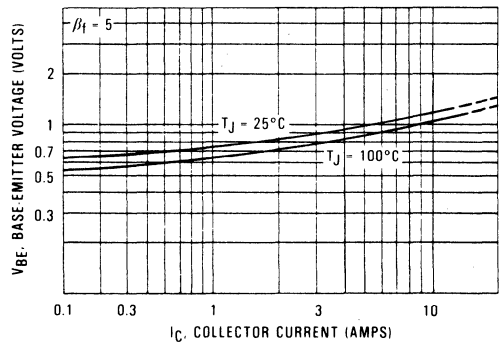


FIGURE 5 — COLLECTOR CUTOFF REGION

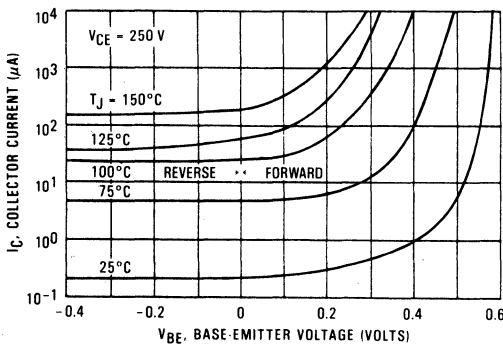
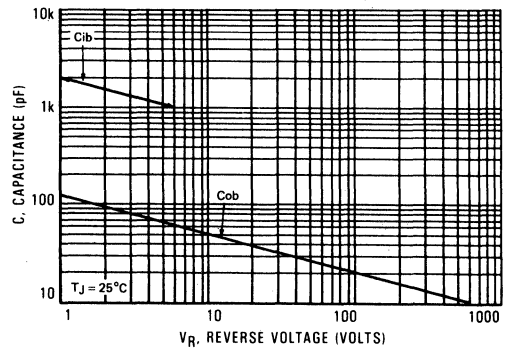


FIGURE 6 — CAPACITANCE



3

TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

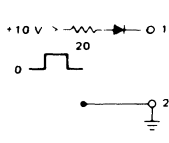
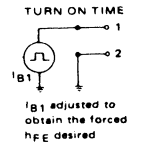
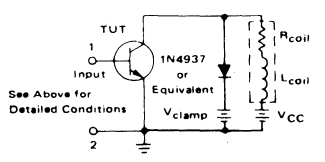
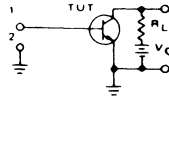
	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>	<p>ADJUST V_{C1} TO OBTAIN DESIRED I_{B1}</p> <p>ADJUST V_{C2} TO OBTAIN DESIRED I_{B2}</p>	 <p>TURN ON TIME</p> <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME</p> <p>Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	L _{coil} = 25 mH V _{CC} = 10 V R _{coil} = 0.7 Ω	L _{coil} 180 µH R _{coil} 0.05 Ω V _{CC} 20 V V _{clamp} 250 V	V _{CC} 250 V Pulse Width 10 µs
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

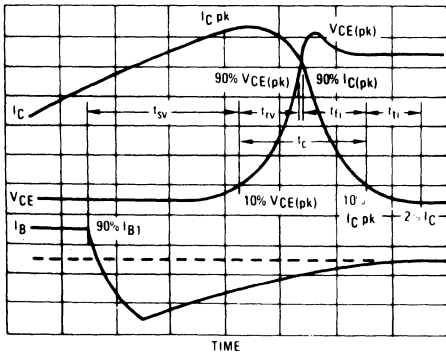
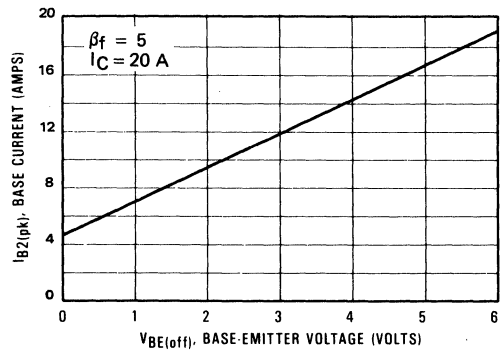


FIGURE 8 - PEAK-REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME, T_{sv}

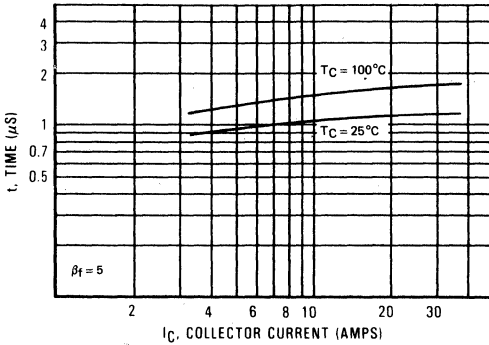


FIGURE 10 — CROSSOVER AND FALL TIMES

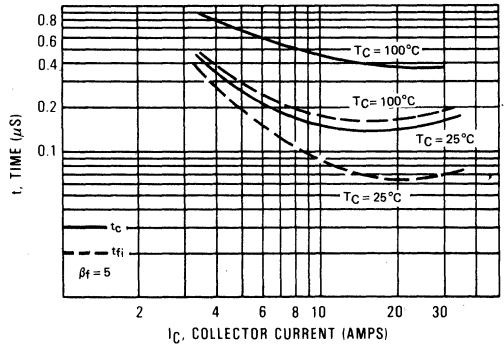


FIGURE 11a — TURN-OFF TIMES vs FORCED GAIN

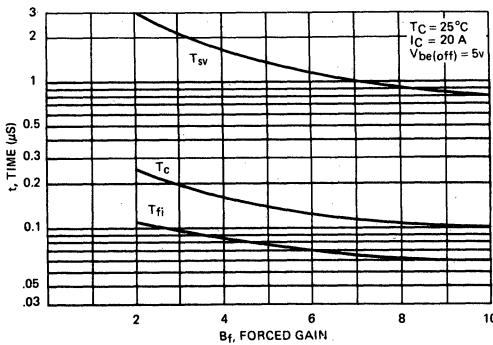
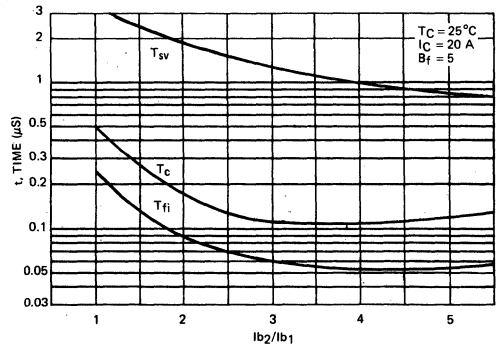


FIGURE 11b — TURN-OFF TM TIMES vs I_{b2}/I_{b1}



3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

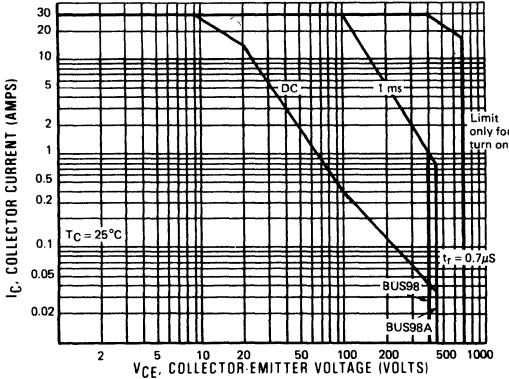
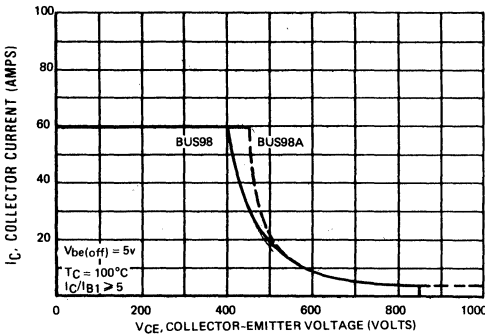


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA



REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 14 — POWER DERATING

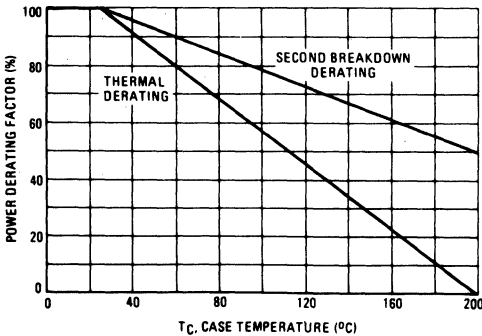
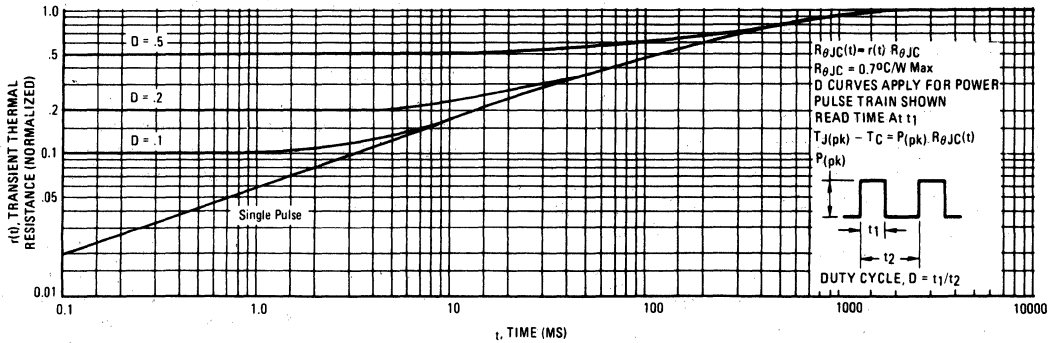


FIGURE 15 – THERMAL RESPONSE



OVERLOAD CHARACTERISTICS

FIGURE 16 – RATED OVERLOAD SAFE OPERATING AREA (OLSOA)

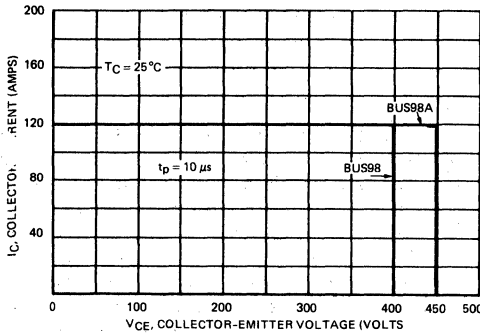
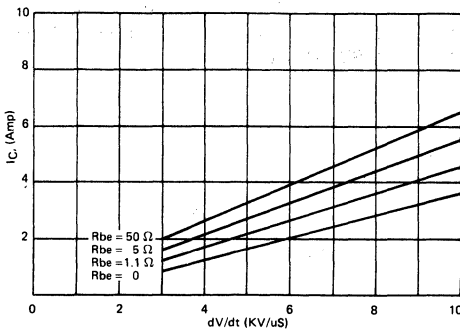


FIGURE 17 – $I_C = f(dV/dt)$



OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

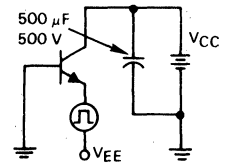
Maximum allowable collector-emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common-base circuit (Figure 18) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

FIGURE 18 – OVERLOAD SOA TEST CIRCUIT

Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C , t_p

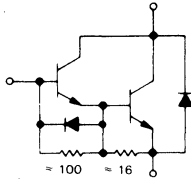


BUT13

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The BUT 13 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 300 nS Inductive Fall Time at 25°C (Typ)
 1.1 μS Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range - 65 to 200°C

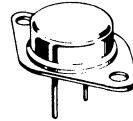


28 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS

600 VOLTS
175 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



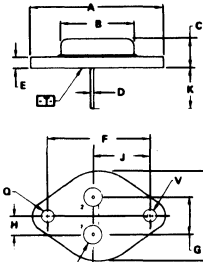
MAXIMUM RATINGS

Rating	Symbol	BUT13	Unit
Collector-Emitter Voltage	V _{CEO(sus)}	400	Vdc
Collector-Emitter Voltage	V _{CEV}	600	Vdc
Emitter Base Voltage	V _{EB}	10	Vdc
Collector Current			A dc
- Continuous	I _C	28	
- Peak (1)	I _{CM}	35	
Base Current			A dc
- Continuous	I _B	6	
- Peak (1)	I _{BM}	7.5	
Free Wheel Diode:			A dc
Forward current - Continuous	I _F	28	
- Peak	I _{FM}	35	
Total Power Dissipation @ T _C = 25°C	P _D	175	Watts
Derate above 25°C @ T _C = 100°C		100	W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	- 65 to + 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	Rθ _{JC}	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES
 1 DIMENSIONS D AND V ARE DATUMS
 2 [] IS SEATING PLANE AND DATUM
 3 POSITIONAL TOLERANCE FOR MOUNTING HOLE Ø
 4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

⌀ .13 (0.005) Ⓢ T V Ⓢ
 FOR LEADS
 ⌀ .13 (0.005) Ⓢ T V Ⓢ Ⓢ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.37		1.550	
B	21.08		0.830	
C	6.35	7.62	0.250	0.300
D	0.97	1.08	0.038	0.043
E		3.43		0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18 12.19	0.440 0.480		
Q	3.81 4.19	0.150 0.165		
R	26.67		1.050	
U	4.83 5.33	0.190 0.210		
V	3.81 4.19	0.150 0.165		

CASE 1-05 TO-3

BUT13

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (IC = 100 mA, IB = 0)	VCEO(sus)	400	–	–	Vdc
Collector Cutoff Current (VCEV = Rated Value, VBE(off) = 1.5 Vdc) (VCEV = Rated Value, VBE(off) = 1.5 Vdc, TC = 100 °C)	ICEV	–	–	0.1 2.0	mAdc
Emitter Cutoff Current (VEB = 2.0 V, IC = 0)	IEBO	–	–	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	IS/b	–	–	See Figure 16	–
Clamped Inductive SOA with Base Reverse Biased	RBSOA	–	–	See Figure 17	–

ON CHARACTERISTICS (1)

DC Current Gain (IC = 10 A, VCE = 5 V) (IC = 18 A, VCE = 5 V)	hFE	30 20	– –	– –	–
Collector-Emitter Saturation Voltage (IC = 10 A, IB = 0.5 A) (IC = 18 A, IB = 1.8 A) (IC = 22 A, IB = 2.2 A) (IC = 28 A, IB = 5.6 A)	VCE(sat)	– – – –	– – – –	2.0 2.5 3.0 5.0	Vdc
Base-Emitter Saturation Voltage (IC = 10 A, IB = 0.5 A) (IC = 18 A, IB = 1.8 A) (IC = 22 A, IB = 2.2 A)	VBE(sat)	– – –	– – –	2.5 3.0 3.3	Vdc
Diode Forward Voltage (IF = 22 A)	Vf	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	TC = 25°C	See Table 1 IC = 18 A	ts	–	1.1	2.6	μs
Fall Time			tf	–	0.3	0.8	μs
Storage Time	TC = 100°C	IB1 = 1.8 A VBE(off) = 5 V	ts	–	1.4	–	μs
Fall Time			tf	–	0.33	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

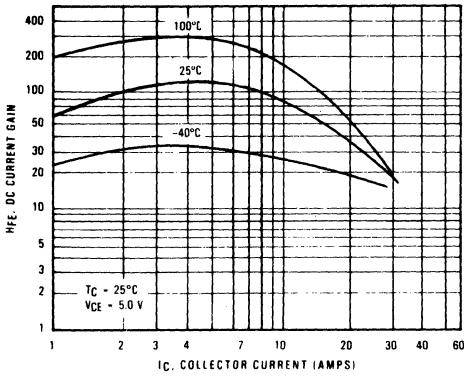


FIGURE 2 — COLLECTOR SATURATION REGION

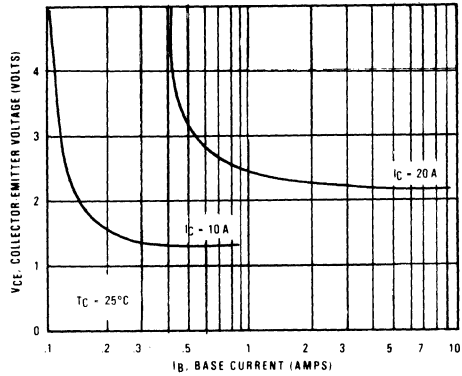


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

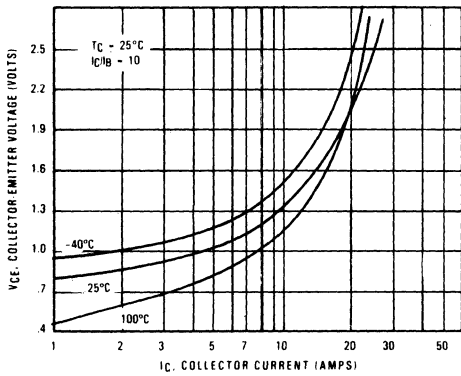


FIGURE 4 — BASE-EMITTER VOLTAGE

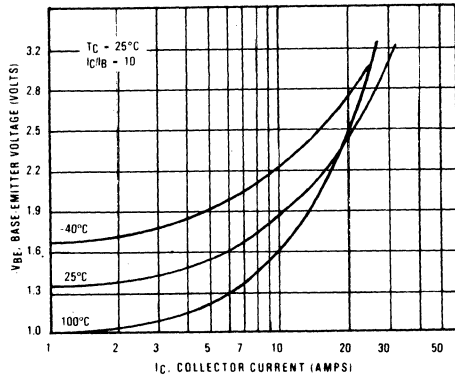


FIGURE 5 — THERMAL RESPONSE

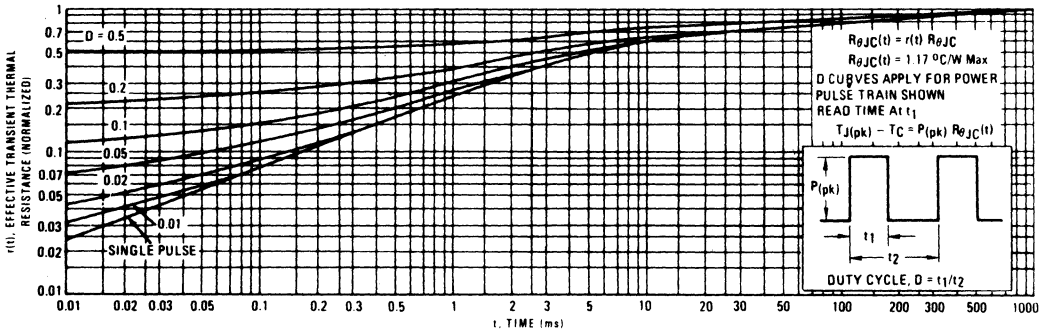


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	VCE(sus)	RBSOA AND INDUCTIVE SWITCHING	TEST CIRCUIT for FREE WHEEL DIODE
INPUT CONDITIONS	<p>5 V 20Ω</p> <p>PW Varied to Attain I_L 100mA</p>		
CIRCUIT VALUES	$L_{coil} = 10 \text{ mH}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CE(sus)}$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 10 \text{ V}$	
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>1) Adjusted to Obtain I_C $t_1 \approx L_{coil}(ICM) / V_{CC}$ $t_2 \approx L_{coil}(ICM) / V_{clamp}$</p> <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	

FIGURE 6 - FALL TIME vs IB2/IB1

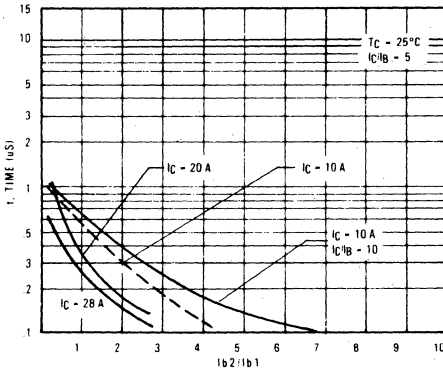


FIGURE 7 - TURN-OFF TIME vs IC

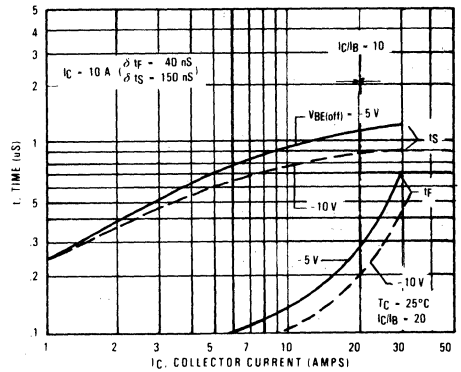


FIGURE 8 - STORAGE TIME vs FORCED GAIN

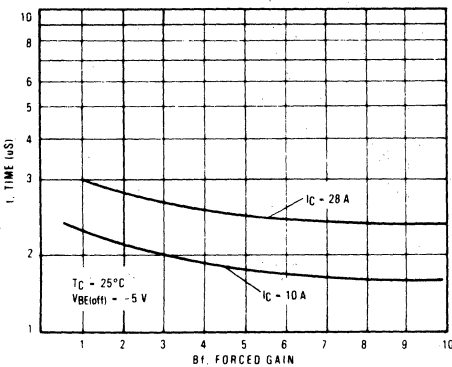
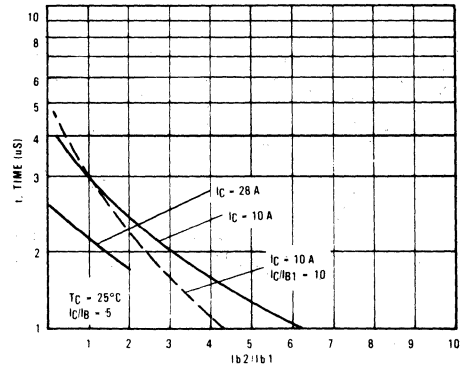


FIGURE 9 - STORAGE TIME vs IB2/IB1



3

FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 – FREE WHEEL DIODE MEASUREMENTS

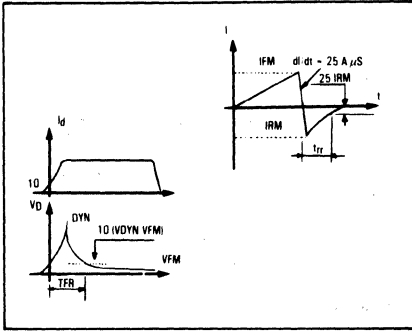


FIGURE 11 – FORWARD VOLTAGE

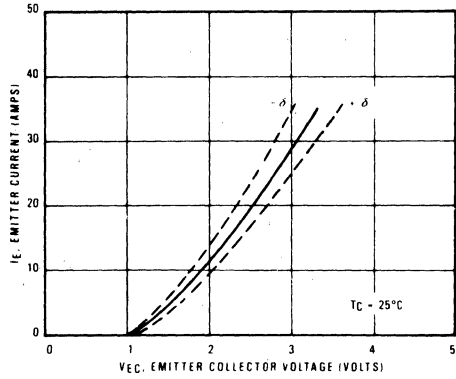


FIGURE 12 – FORWARD MODULATION VOLTAGE

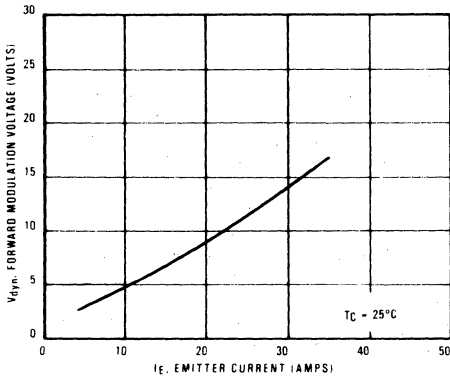


FIGURE 13 – PEAK REVERSE RECOVERY CURRENT

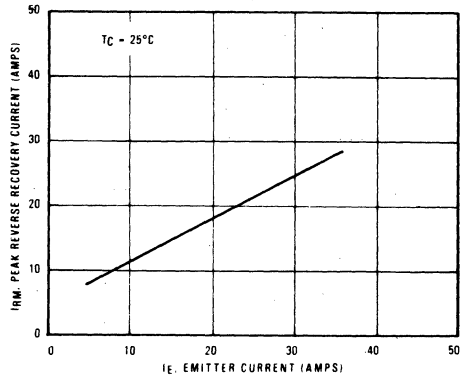


FIGURE 14 – FORWARD RECOVERY TIME

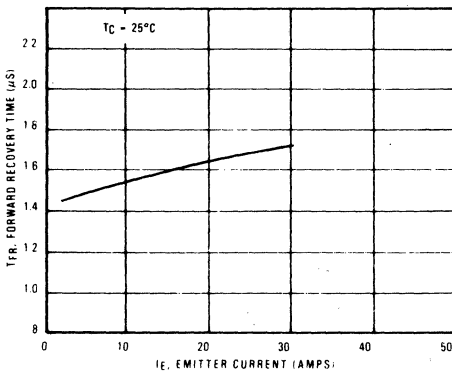
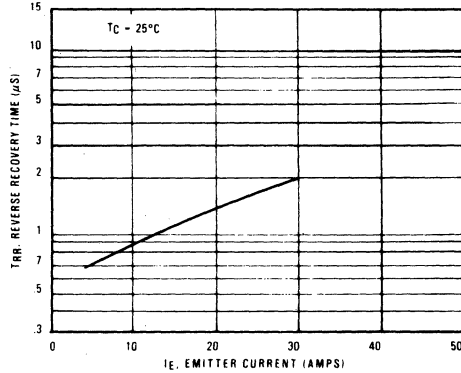


FIGURE 15 – REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 - SAFE OPERATING AREA

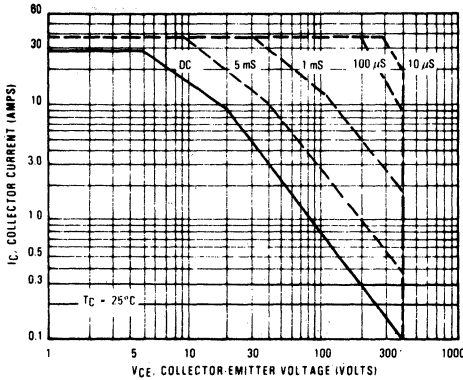
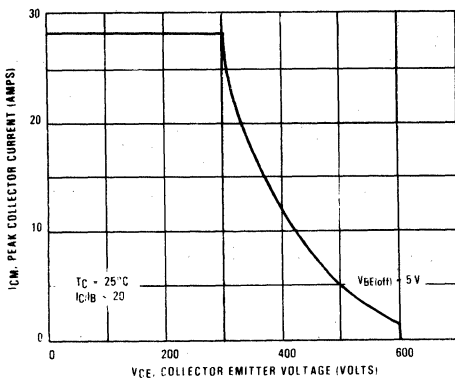


FIGURE 17 - REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC-VCE limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

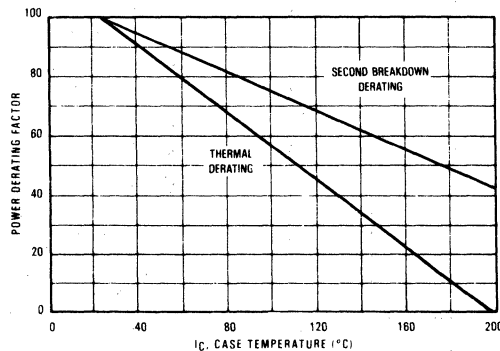
The data of Figure 16 is based on TC = 25°C; TJ(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when TC ≥ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

TJ(pk) may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

FIGURE 18 - POWER DERATING



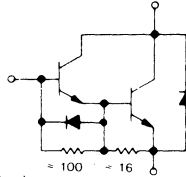
3

BUT14

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The BUT 14 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 300 nS Inductive Fall Time at 25°C (Typ)
 - 1.3 μS Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range - 65 to 200°C

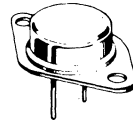


25 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS

850 VOLTS
175 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



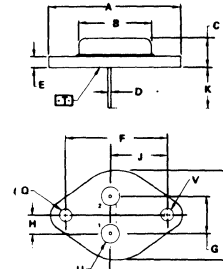
MAXIMUM RATINGS

Rating	Symbol	BUT14	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	500	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current			Adc
- Continuous	I_C	25	
- Peak (1)	I_{CM}	35	
Base Current			Adc
- Continuous	I_B	5	
- Peak (1)	I_{BM}	7.5	
Free Wheel Diode:			Adc
Forward current - Continuous	I_F	25	
- Peak	I_{FM}	35	
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	175	Watts
Derate above 25°C @ $T_C = 100^\circ C$		100	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 65 to + 200	°C

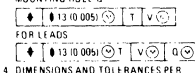
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES
 1 DIMENSIONS D AND V ARE DATUMS
 2 [] IS SEATING PLANE AND DATUM
 3 POSITIONAL TOLERANCE FOR MOUNTING HOLE G
 4 DIMENSIONS AND TOLERANCES PER ANSI #14.5, 1913



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	35.37		1.550	
B	21.08		0.830	
C	6.35	7.62	0.250	0.300
D	9.97	1.09	0.038	0.043
E		3.43		0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.48 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
D	3.81	4.19	0.150	0.165
R		28.61		1.093
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

BUT14

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (IC = 100 mA, IB = 0)	VCEO(sus)	500	–	–	Vdc
Collector Cutoff Current (VCEV = Rated Value, VBE(off) = 1.5 Vdc) (VCEV = Rated Value, VBE(off) = 1.5 Vdc, TC = 100°C)	ICEV	–	–	0.2 2.0	mAdc
Emitter Cutoff Current (VEB = 2.0 V, IC = 0)	IEBO	–	–	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	IS/b		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17	

ON CHARACTERISTICS (1)

DC Current Gain (IC = 8 A, VCE = 5 V) (IC = 16 A, VCE = 5 V)	hFE	30 15	– –	– –	
Collector-Emitter Saturation Voltage (IC = 8 A, IB = 0.4 A) (IC = 16 A, IB = 1.6 A) (IC = 20 A, IB = 2.0 A) (IC = 25 A, IB = 5 A)	VCE(sat)	– – – –	– – – –	2.0 3.0 3.5 5.0	Vdc
Base-Emitter Saturation Voltage (IC = 8 A, IB = 0.4 A) (IC = 16 A, IB = 1.6 A) (IC = 20 A, IB = 2 A)	VBE(sat)	– – –	– – –	2.5 2.9 3.3	Vdc
Diode Forward Voltage (IF = 20 A)	Vf	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	TC = 25°C	See Table 1 IC = 16 A	ts	–	1.3	2.8	μs
Fall Time			tf	–	0.3	0.8	μs
Storage Time	TC = 100°C	IB1 = 1.6 A VBE(off) = 5 V	ts	–	1.5	–	μs
Fall Time			tf	–	0.35	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

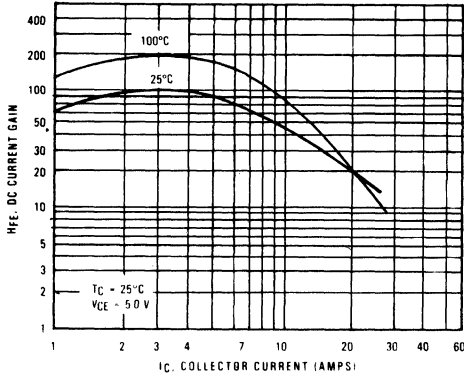


FIGURE 2 — COLLECTOR SATURATION REGION

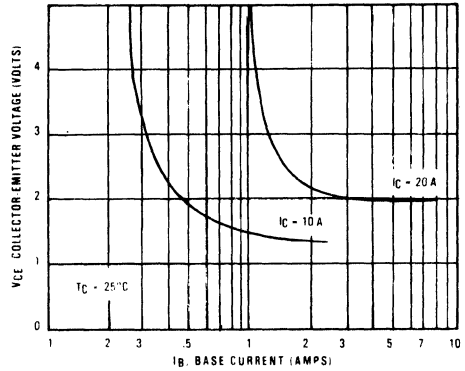


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

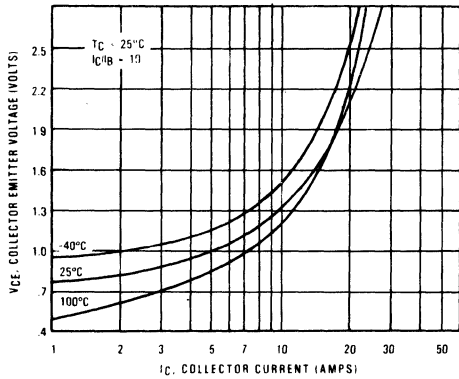


FIGURE 4 — BASE-EMITTER VOLTAGE

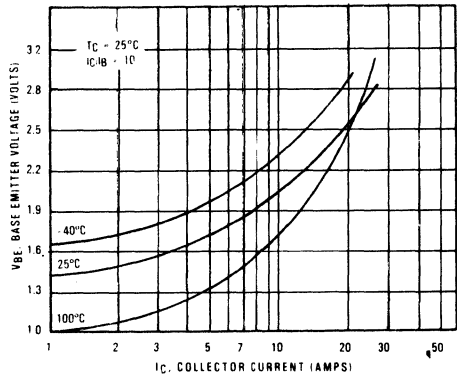


FIGURE 5 — THERMAL RESPONSE

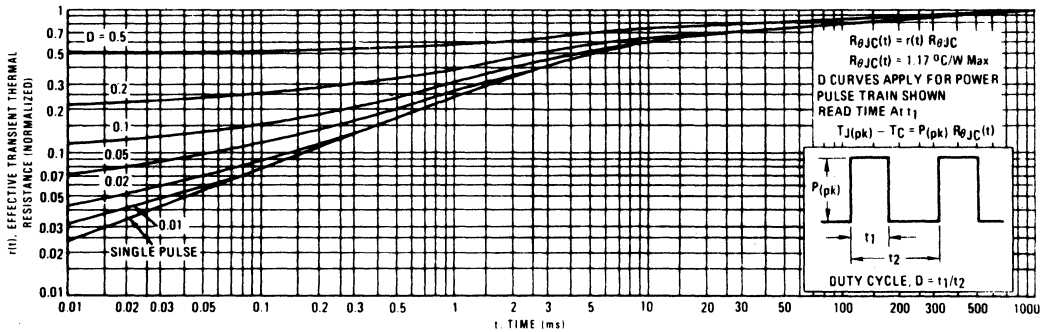


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

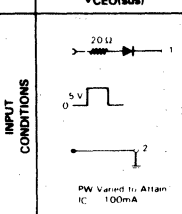
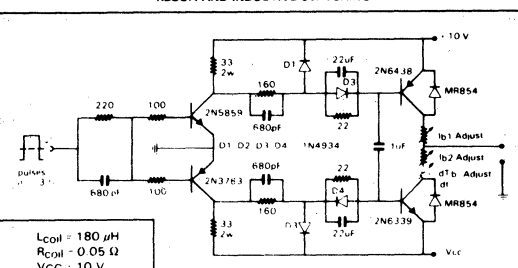
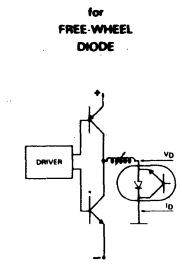
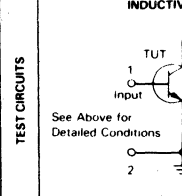
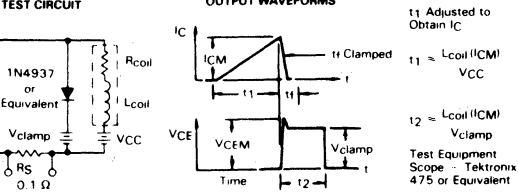
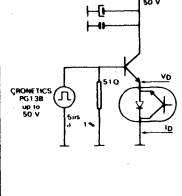
<p>INPUT CONDITIONS</p>  <p>$V_{CE0(sus)}$</p> <p>20Ω</p> <p>5 V</p> <p>0</p> <p>PW Varied to Attain $I_C = 100mA$</p>	<p>RBSOA AND INDUCTIVE SWITCHING</p>  <p>10 V</p> <p>33 2w</p> <p>180</p> <p>80pf</p> <p>2N6438</p> <p>MRB54</p> <p>22</p> <p>22uF</p> <p>1uF</p> <p>1N4934</p> <p>1b1 Adjust</p> <p>1b2 Adjust</p> <p>d1</p> <p>d1</p> <p>MRB54</p> <p>2N6339</p> <p>22uF</p> <p>33 2w</p> <p>15 W</p> <p>Vcc</p>	<p>TEST CIRCUIT for FREE-WHEEL DIODE</p>  <p>DRIVER</p> <p>VD</p> <p>IQ</p>
<p>CIRCUIT VALUES</p> <p>$L_{coil} = 10 mH$ $V_{CC} = 10V$</p> <p>$R_{coil} = 0.7 \Omega$</p> <p>$V_{clamp} = V_{CE0(sus)}$</p>	<p>$L_{coil} = 180 \mu H$</p> <p>$R_{coil} = 0.05 \Omega$</p> <p>$V_{CC} = 10 V$</p>	
<p>TEST CIRCUITS</p> <p>INDUCTIVE TEST CIRCUIT</p>  <p>1</p> <p>Input</p> <p>1N4937 or Equivalent</p> <p>R_{coil}</p> <p>L_{coil}</p> <p>V_{clamp}</p> <p>V_{CC}</p> <p>See Above for Detailed Conditions</p> <p>2</p> <p>R_S</p> <p>0.1 Ω</p>	<p>OUTPUT WAVEFORMS</p>  <p>I_C</p> <p>I_{CM}</p> <p>t_1 Clamped</p> <p>t_1</p> <p>t_2</p> <p>V_{CE}</p> <p>V_{CEM}</p> <p>V_{clamp}</p> <p>Time</p> <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 = L_{coil} / I_{CM} V_{CC}$</p> <p>$t_2 = L_{coil} / I_{CM} V_{clamp}$</p> <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>AV up to 50 V</p>  <p>CHROMICS PULSER set to 50 V</p> <p>5uF</p> <p>1510</p> <p>VD</p> <p>IQ</p>

FIGURE 6 - FALL TIME vs I_{B2}/I_{B1}

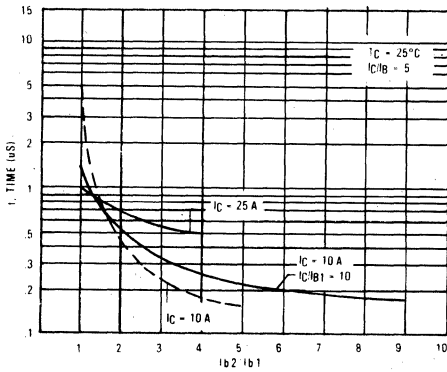


FIGURE 7 - TURN-OFF TIME vs I_C

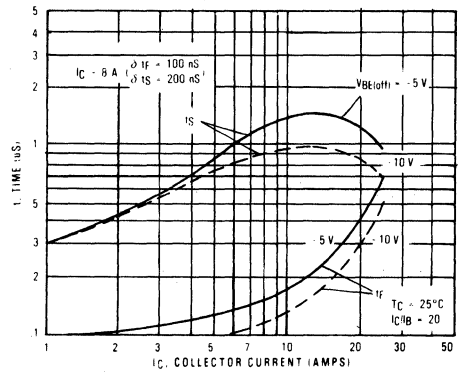


FIGURE 8 - STORAGE TIME vs FORCED GAIN

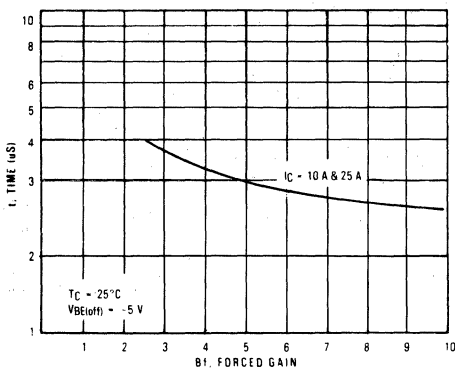
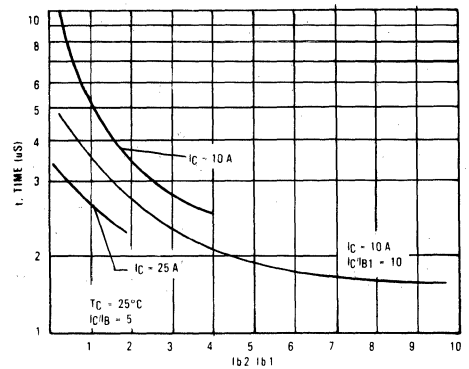


FIGURE 9 - STORAGE TIME vs I_{B2}/I_{B1}



FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 – FREE WHEEL DIODE MEASUREMENTS

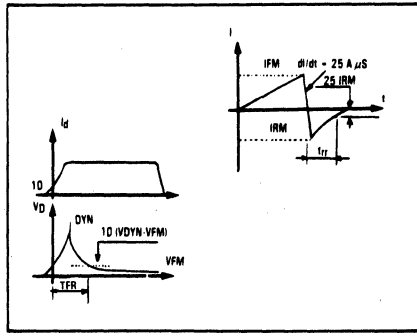


FIGURE 11 – FORWARD VOLTAGE

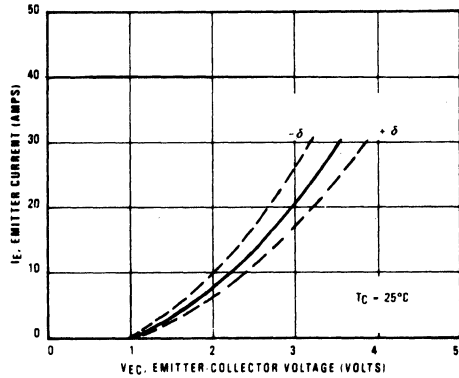


FIGURE 12 – FORWARD MODULATION VOLTAGE

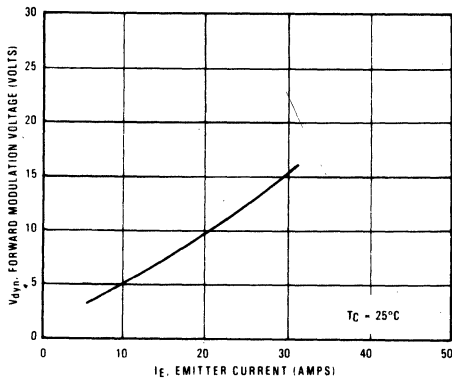


FIGURE 13 – PEAK REVERSE RECOVERY CURRENT

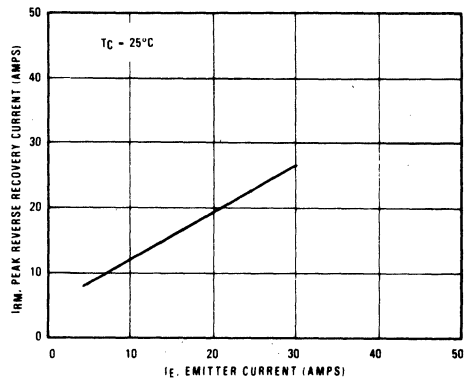


FIGURE 14 – FORWARD RECOVERY TIME

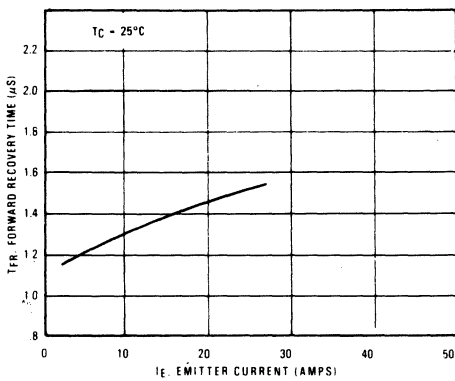
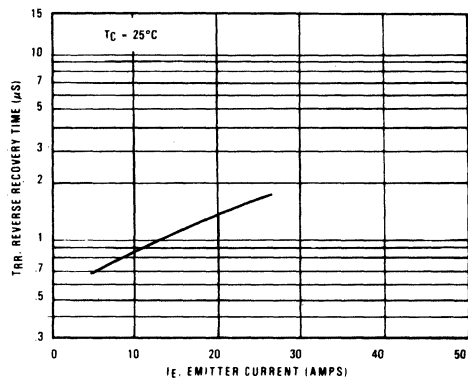
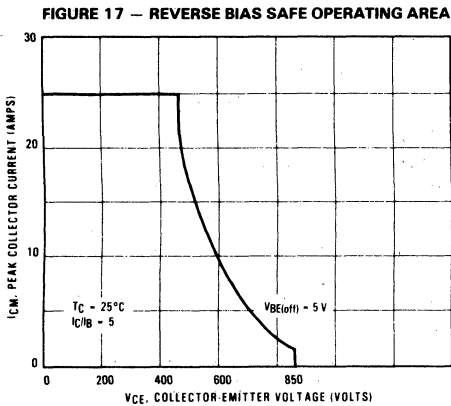
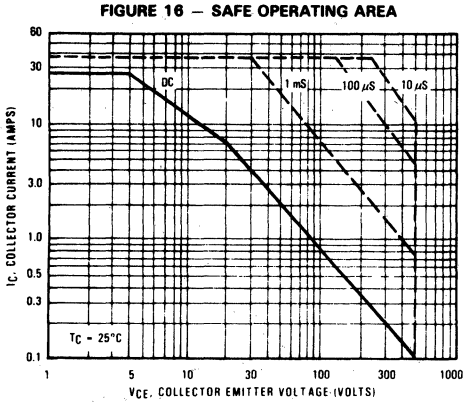


FIGURE 15 – REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

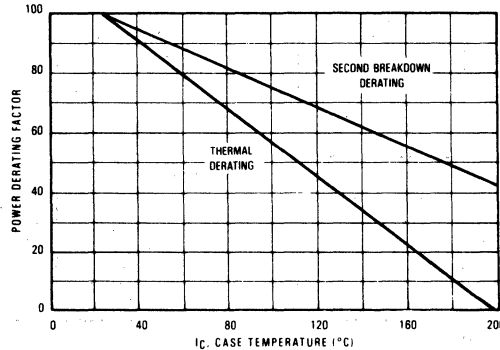
The data of Figure 16 is based on T_C = 25°C; T_{J(pk)} is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C ≥ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

T_{J(pk)} may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

FIGURE 18 – POWER DERATING

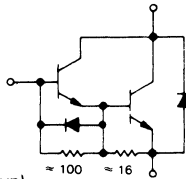


BUT15

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The BUT 15 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times



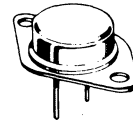
300 nS Inductive Fall Time at 25°C (Typ)
1.2 μS Inductive Storage Time at 25°C (Typ)

- Operating Temperature Range - 65 to 200°C

20 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS
1000 VOLTS
175 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



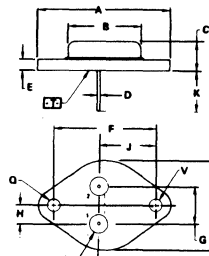
MAXIMUM RATINGS

Rating	Symbol	BUT15	Unit
Collector-Emitter Voltage	V _{CEO(sus)}	700	Vdc
Collector-Emitter Voltage	V _{CEV}	1000	Vdc
Emitter Base Voltage	V _{EB}	10	Vdc
Collector Current			Adc
- Continuous	I _C	20	
- Peak (1)	I _{CM}	25	
Base Current			Adc
- Continuous	I _B	5	
- Peak (1)	I _{BM}	10	
Free Wheel Diode:			Adc
Forward current - Continuous	I _F	20	
- Peak	I _{FM}	25	
Total Power Dissipation @ T _C = 25°C	P _D	175	Watts
Derate above 25°C @ T _C = 100°C		100	W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	- 65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES

- 1 DIMENSIONS Q AND V ARE DATUMS
- 2 [T] IS SEATING PLANE AND DATUM
- 3 POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
- 4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

⌀ 13 (0.005) (T) V (Q)

FOR LEADS

⌀ 13 (0.005) (T) V (Q) (Q)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	-	2.43	-	0.135
F	30.15 BSC	-	1.187 BSC	-
G	10.97 BSC	-	0.430 BSC	-
H	5.46 BSC	-	0.215 BSC	-
J	15.89 BSC	-	0.625 BSC	-
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.97	-	1.060
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (IC = 100 mA, IB = 0)	VCEO(sus)	700	–	–	Vdc
Collector Cutoff Current (VCEV = Rated Value, VBE(off) = 1.5 Vdc) (VCEV = Rated Value, VBE(off) = 1.5 Vdc, TC = 100 °C)	ICEV	–	–	0.1 2.0	mAdc
Emitter Cutoff Current (VEB = 2.0 V, IC = 0)	IEBO	–	–	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	IS/b		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17	

ON CHARACTERISTICS (1)

DC Current Gain (IC = 6 A, VCE = 5 V) (IC = 12 A, VCE = 5 V)	hFE	30 15	– –	– –	
Collector-Emitter Saturation Voltage (IC = 6 A, IB = 0.3 A) (IC = 12 A, IB = 1.2 A) (IC = 16 A, IB = 1.6 A) (IC = 20 A, IB = 4 A)	VCE(sat)	– – – –	– – – –	2.0 3.0 3.5 5.0	Vdc
Base-Emitter Saturation Voltage (IC = 6 A, IB = 0.3 A) (IC = 12 A, IB = 1.2 A) (IC = 16 A, IB = 1.6 A)	VBE(sat)	– – –	– – –	2.5 2.9 3.3	Vdc
Diode Forward Voltage (IF = 16 A)	Vf	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	TC = 25°C	See Table 1	ts	–	1.2	2.5	μs
Fall Time			tf	–	0.3	0.8	μs
Storage Time	TC = 100°C	IB1 = 1.2 A	ts	–	1.4	–	μs
Fall Time			tf	–	0.35	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

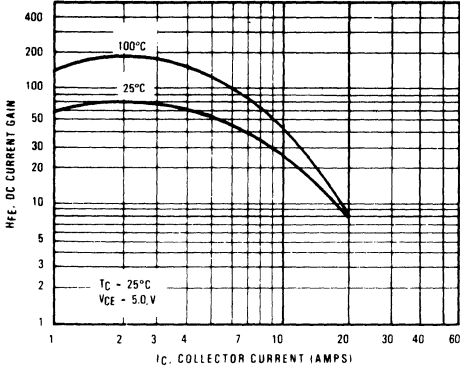


FIGURE 2 — COLLECTOR SATURATION REGION

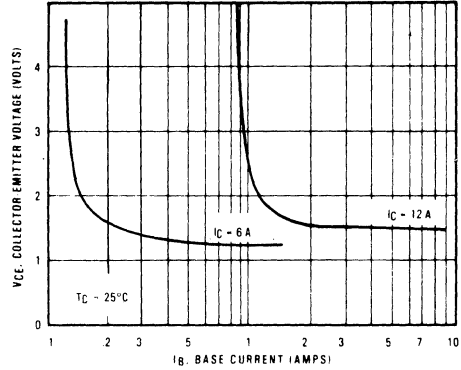


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

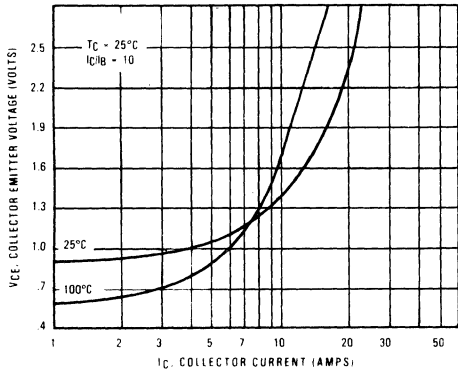


FIGURE 4 — BASE-EMITTER VOLTAGE

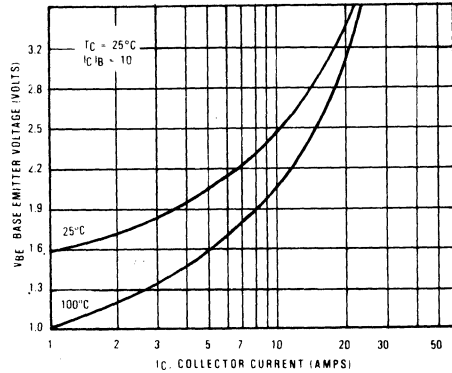


FIGURE 5 — THERMAL RESPONSE

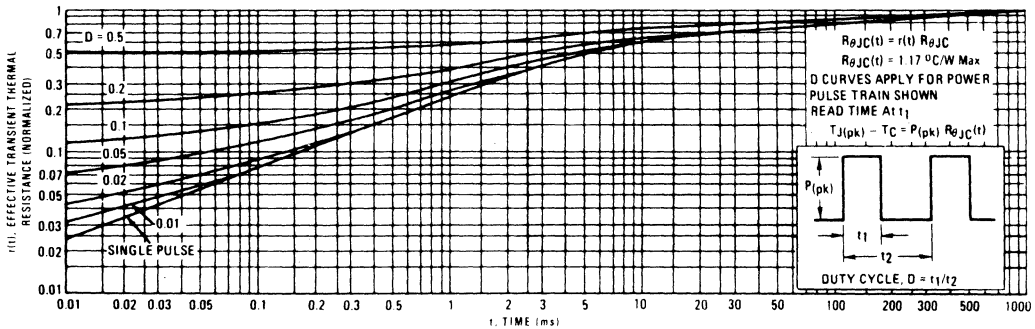


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

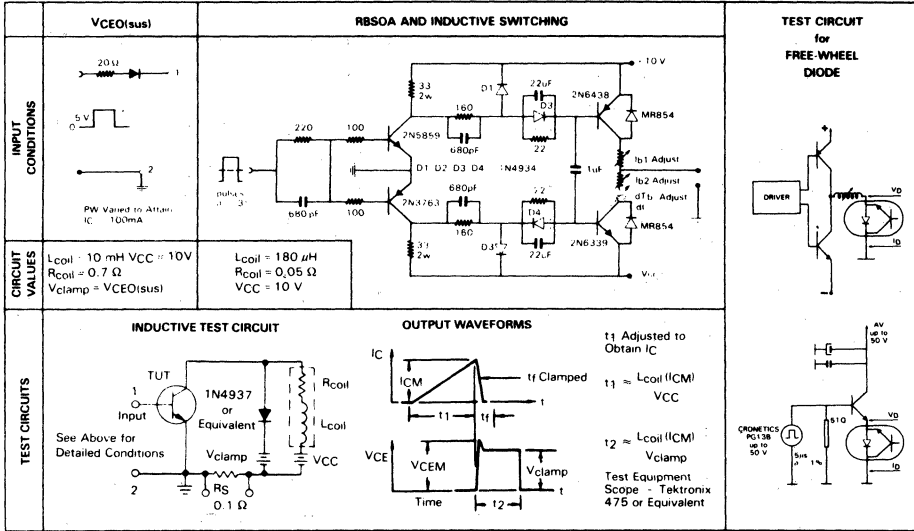


FIGURE 6 - FALL TIME vs IB2/IB1

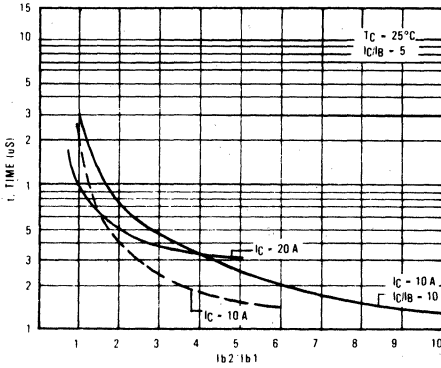


FIGURE 7 - TURN-OFF TIME vs IC

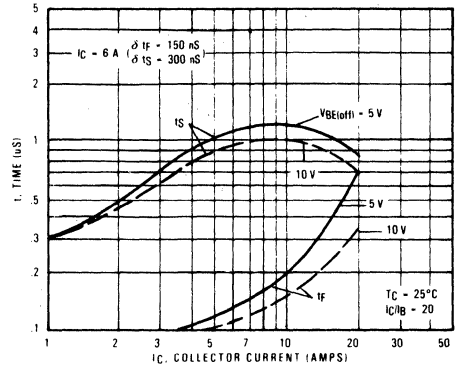


FIGURE 8 - STORAGE TIME vs FORCED GAIN

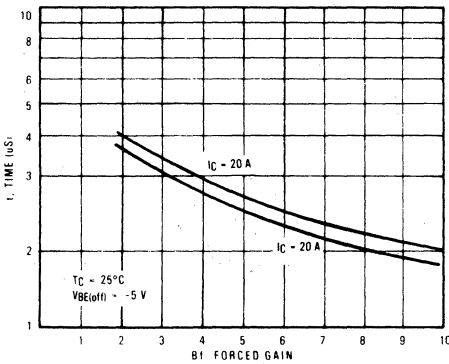
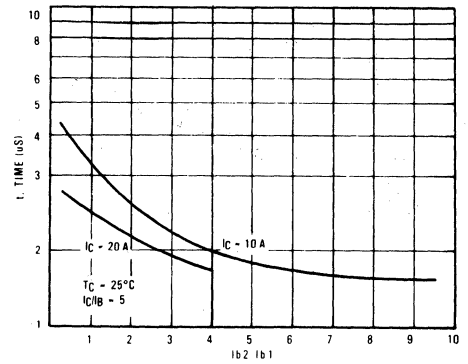


FIGURE 9 - STORAGE TIME vs IB2/IB1



3

FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 – FREE WHEEL DIODE MEASUREMENTS

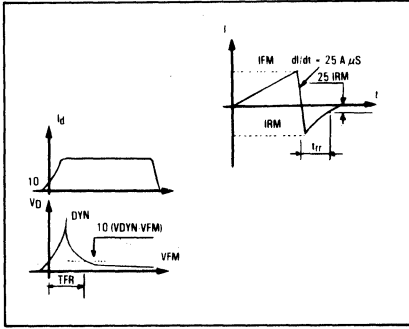


FIGURE 11 – FORWARD VOLTAGE

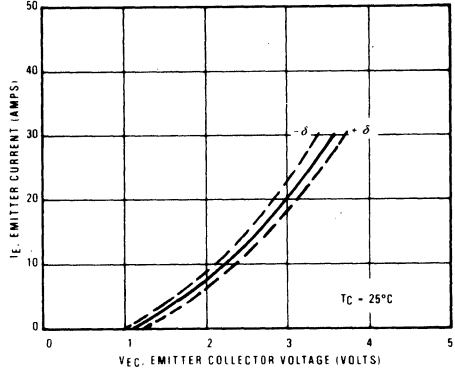


FIGURE 12 – FORWARD MODULATION VOLTAGE

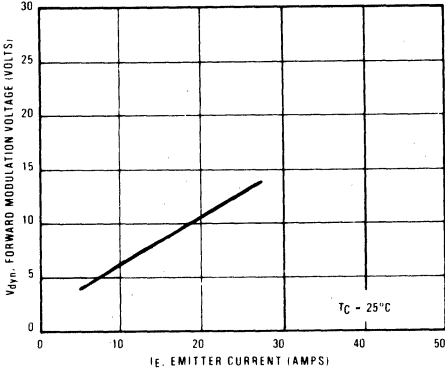


FIGURE 13 – PEAK REVERSE RECOVERY CURRENT

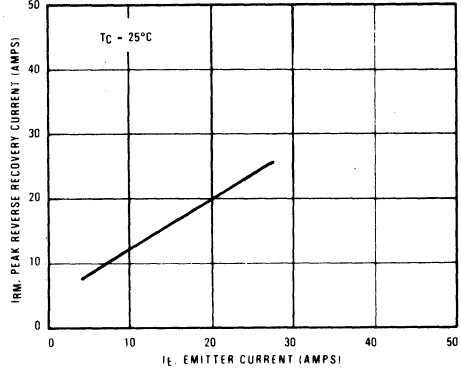


FIGURE 14 – FORWARD RECOVERY TIME

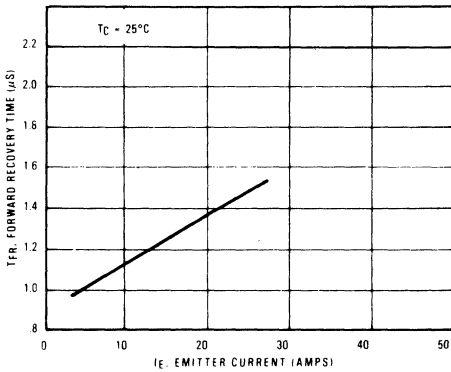
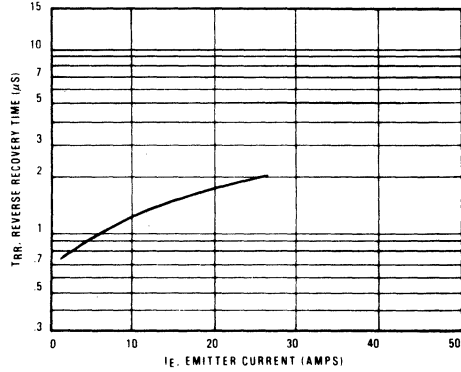


FIGURE 15 – REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

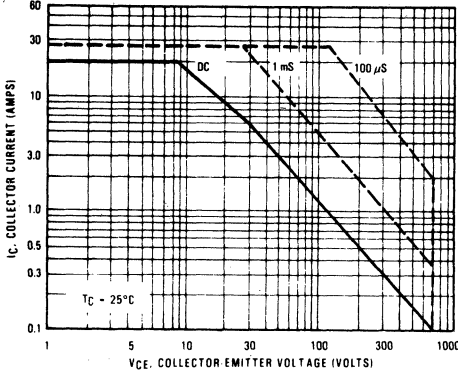


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA

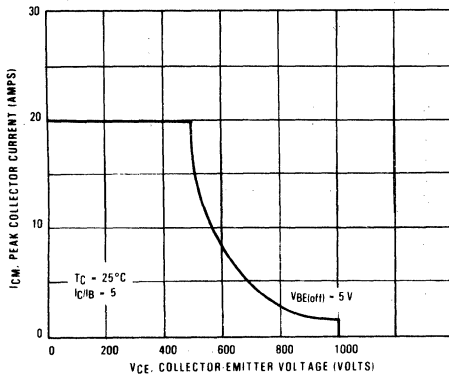
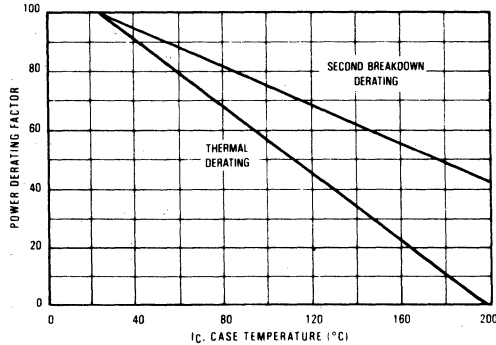


FIGURE 18 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC-VCE limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on TC = 25°C; TJ(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when TC ≥ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

TJ(pk) may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

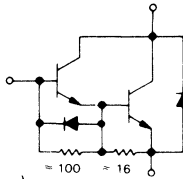
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

BUT16

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The BUT 16 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 2.0 μ s Inductive Fall Time at 100°C (Typ)
 - 0.8 μ s Inductive Storage Time at 100°C (Typ)
- Operating Temperature Range - 65 to 175°C

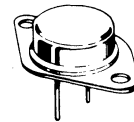


12 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS

1400 VOLTS
150 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



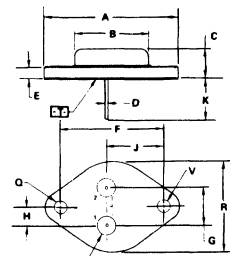
MAXIMUM RATINGS

Rating	Symbol	BUT16	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	1000	Vdc
Collector-Emitter Voltage	V_{CEV}	1400	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current			Adc
- Continuous	I_C	12	
- Peak (1)	I_{CM}	20	
Base Current			Adc
- Continuous	I_B	8	
- Peak (1)	I_{BM}	10	
Free Wheel Diode:			Adc
Forward current - Continuous	I_F	12	
- Peak	I_{FM}	20	
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	150	Watts
@ $T_C = 100^\circ C$		75	
Derate above 25°C			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 65 to +175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle \leq 10%.



- NOTES
- 1 DIMENSIONS Q AND V ARE DATUMS
 - 2 [] IS SEATING PLANE AND DATUM
 - 3 POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
 - FOR LEADS
 - 4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1937

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.37	-	1.550	-
B	21.08	-	0.830	-
C	6.35	7.62	0.250	0.300
D	0.97	1.05	0.038	0.043
E	-	3.43	-	0.135
F	30.15 BSC	-	1.187 BSC	-
G	10.93 BSC	-	0.430 BSC	-
H	5.46 BSC	-	0.215 BSC	-
J	16.83 BSC	-	0.665 BSC	-
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

BUT16

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (IC = 100 mA, IB = 0)	VCEO(sus)	1000	–	–	Vdc
Collector Cutoff Current (VCEV = Rated Value, VBE(off) = 1.5 Vdc) (VCEV = Rated Value, VBE(off) = 1.5 Vdc, TC = 100°C)	ICEV	–	–	0.1 2.0	mAdc
Emitter Cutoff Current (VEB = 2.0 V, IC = 0)	IEBO	–	–	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	IS/b			See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	RBSOA			See Figure 17	

ON CHARACTERISTICS (1)

DC Current Gain (IC = 4 A, VCE = 5 V) (IC = 8 A, VCE = 5 V)	hFE	20 5	– –	– –	
Collector-Emitter Saturation Voltage (IC = 12 A, IB = 6 A)	VCE(sat)	–	–	5.0	Vdc
Base-Emitter Saturation Voltage (IC = 8 A, IB = 1.6 A)	VBE(sat)	–	–	3.3	Vdc
Diode Forward Voltage (IF = 12 A)	Vf	–	–	4.0	Vdc

SWITCHING CHARACTERISTICS Inductive Load, Clamped (Table 1)

Storage Time	TC = 25°C	See Table 1	ts	–	–	3.3	μs
Fall Time			tf	–	–	1.5	μs
Storage Time	TC = 100°C	IB1 = 1.6 A	ts	–	2.0	–	μs
Fall Time			tf	–	0.8	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

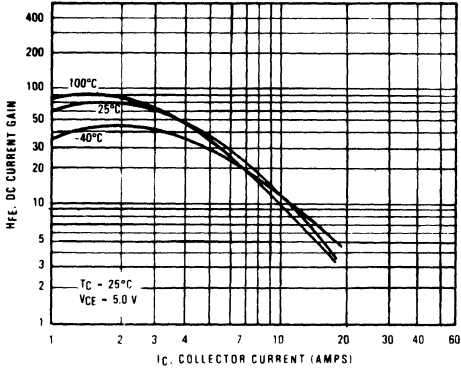


FIGURE 2 — COLLECTOR SATURATION REGION

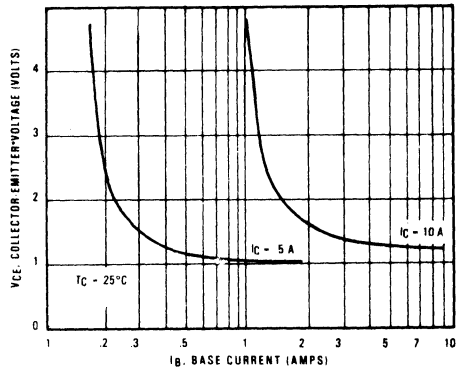


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

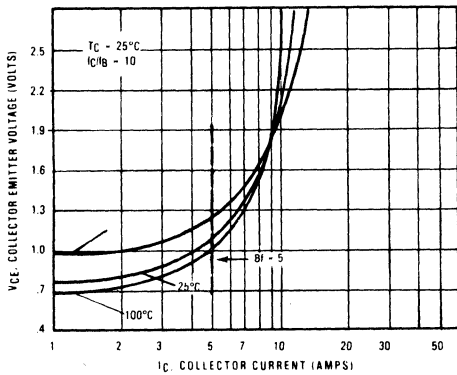


FIGURE 4 — BASE-EMITTER VOLTAGE

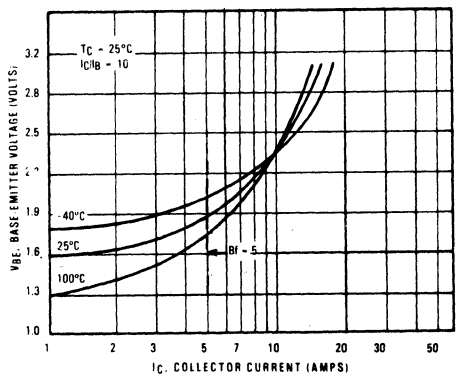


FIGURE 5 — THERMAL RESPONSE

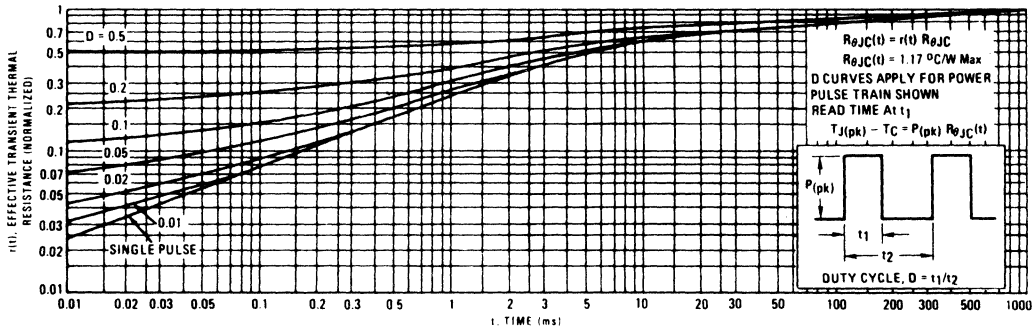


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	VCE0(us)	RBSOA AND INDUCTIVE SWITCHING	TEST CIRCUIT for FREE-WHEEL DIODE
INPUT CONDITIONS			
	<p>PW Varied to Attain IC = 100mA</p>		
CIRCUIT VALUES	<p>Lcoil = 10 mH VCC = 10V Rcoil = 0.7 Ω Vclamp = VCE0(us)</p>	<p>Lcoil = 180 μH Rcoil = 0.05 Ω VCC = 10 V</p>	
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>	<p>OUTPUT WAVEFORMS</p>	<p>TEST CIRCUIT</p>
	<p>See Above for Detailed Conditions</p>	<p>t1 Adjusted to Obtain IC t1 = Lcoil I(CM) / VCC t2 = Lcoil I(CM) / Vclamp Test Equipment Scope Tektronix 475 or Equivalent</p>	

FIGURE 6 - FALL TIME vs IB2/IB1

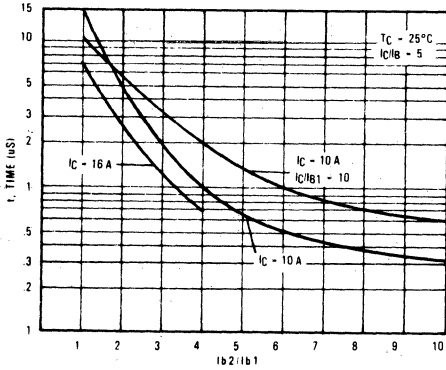


FIGURE 7 - TURN-OFF TIME vs IC

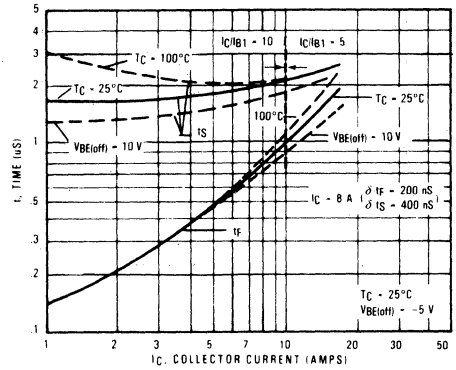


FIGURE 8 - STORAGE TIME vs FORCED GAIN

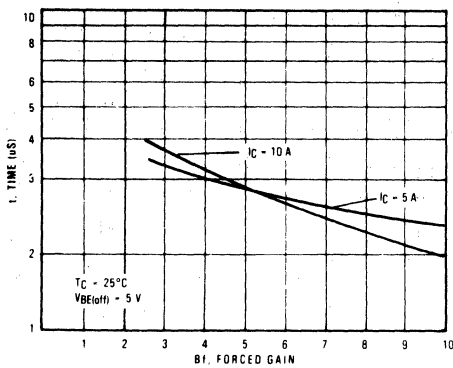
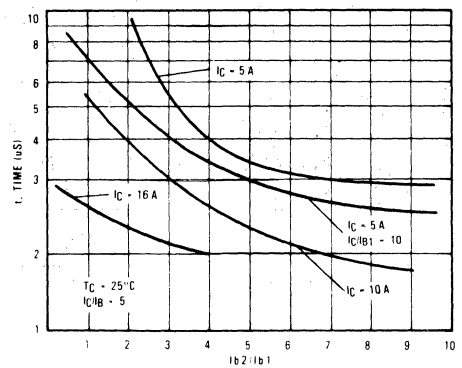


FIGURE 9 - STORAGE TIME vs IB2/IB1



3

FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 — FREE WHEEL DIODE MEASUREMENTS

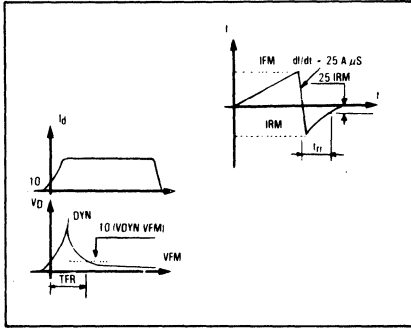


FIGURE 11 — FORWARD VOLTAGE

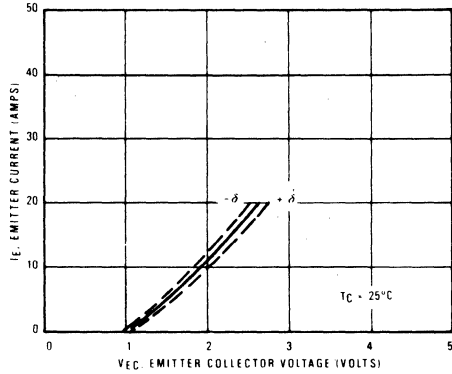


FIGURE 12 — FORWARD MODULATION VOLTAGE

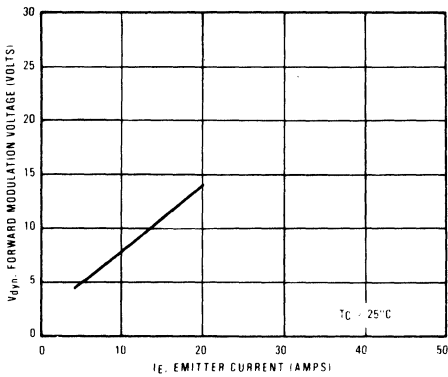


FIGURE 13 — PEAK REVERSE RECOVERY CURRENT

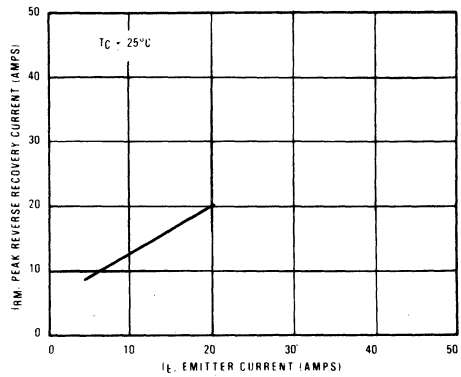


FIGURE 14 — FORWARD RECOVERY TIME

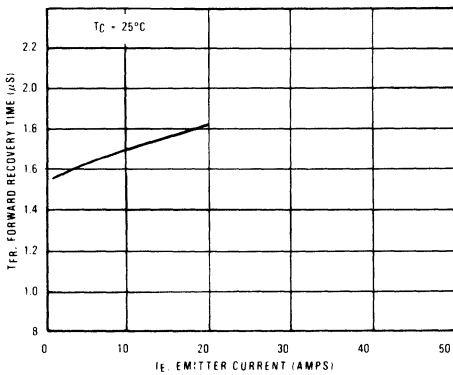
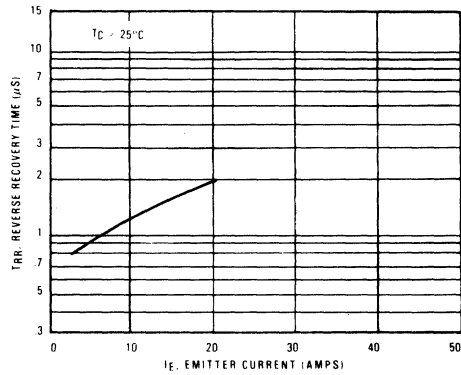


FIGURE 15 — REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

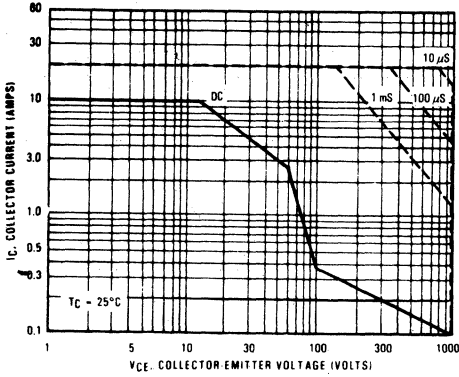


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA

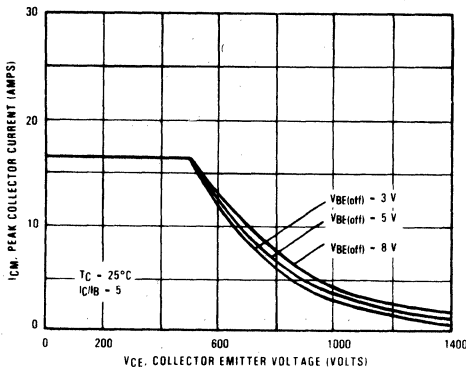
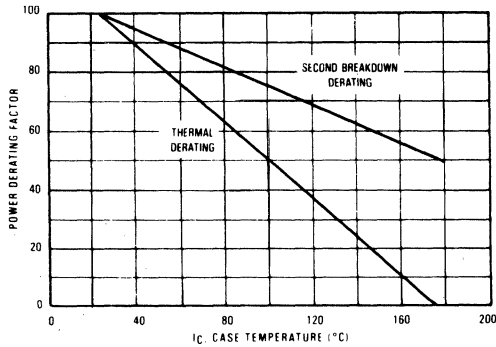


FIGURE 18 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUT33

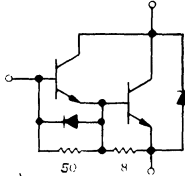
SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The BUT33 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn Off Times

800 nS Inductive Fall Time at 25°C (Typ)
 2.0 μS Inductive Storage Time at 25°C (Typ)

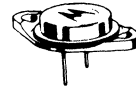
- Operating Temperature Range - 65 to 200°C



56 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS
600 VOLTS
250 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



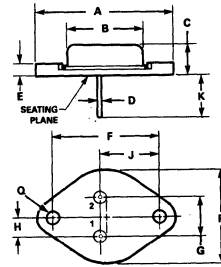
MAXIMUM RATINGS

Rating	Symbol	BUT33	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current	I_C	56	Adc
Continuous	I_{CM}	75	
Base Current	I_B	12	Adc
Continuous	I_{BM}	15	
Free Wheel Diode			
Forward current	I_F	56	Adc
Peak	I_{FM}	75	
Total Power Dissipation (at T_C 25°C)	P_D	250	Watts
Derate above 25°C (at T_C 100°C)		140	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms. Duty Cycle ≤ 10%.



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	38.37	1.510	1.550
B	18.30	21.08	0.720	0.830
C	6.35	7.65	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	24.89	26.67	0.980	1.050

CASE 197-01
 MODIFIED TO-3

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (IC = 100 mA, IB = 0)	VCEO(sus)	400	—	—	Vdc
Collector Cutoff Current (VCEV = Rated Value, VBE(off) = 1.5 Vdc) (VCEV = Rated Value, VBE(off) = 1.5 Vdc, TC = 100°C)	ICEV	—	—	0.2 4.0	mAdc
Emitter Cutoff Current (VEB = 2.0 V, IC = 0)	IEBO	—	—	350	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	IS/b		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17	

ON CHARACTERISTICS (1)

DC Current Gain (IC = 20 A, VCE = 5 V) (IC = 36 A, VCE = 5 V)	hFE	30 20	— —	— —	
Collector-Emitter Saturation Voltage (IC = 20 A, IB = 1 A) (IC = 36 A, IB = 3.6 A) (IC = 44 A, IB = 4.4 A) (IC = 56 A, IB = 11.2 A)	VCE(sat)	— — — —	— — — —	2.0 2.5 3.0 5.0	Vdc
Base-Emitter Saturation Voltage (IC = 20 A, IB = 1 A) (IC = 36 A, IB = 3.6 A) (IC = 44 A, IB = 4.4 A)	VBE(sat)	— — —	— — —	2.5 2.9 3.3	Vdc
Diode Forward Voltage (IF = 44 A)	Vf	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS
Inductive Load, Clamped (Table 1)

Storage Time	TC = 25°C	See Table 1	IC = 36 A	ts	—	2.0	3.3	μs
Fall Time			IB = 3.6 A	tf	—	0.8	1.6	μs
Storage Time	TC = 100°C		VBE(off) = 5 V	ts	—	2.2	—	μs
Fall Time				tf	—	0.8	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

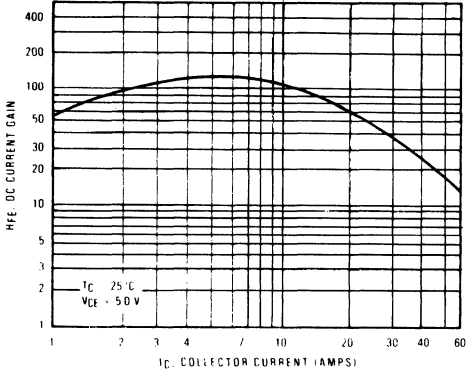


FIGURE 2 -- COLLECTOR SATURATION REGION

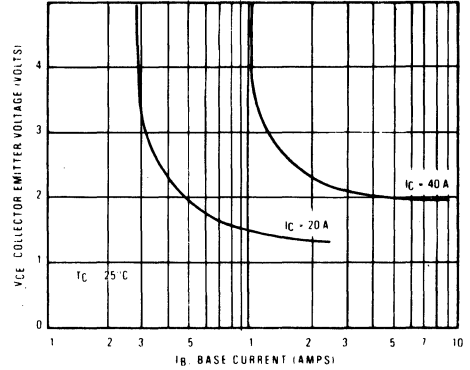


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

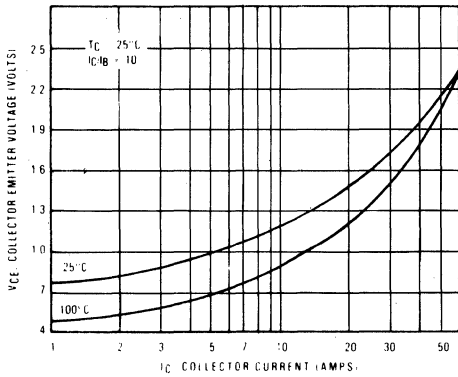


FIGURE 4 — BASE-EMITTER VOLTAGE

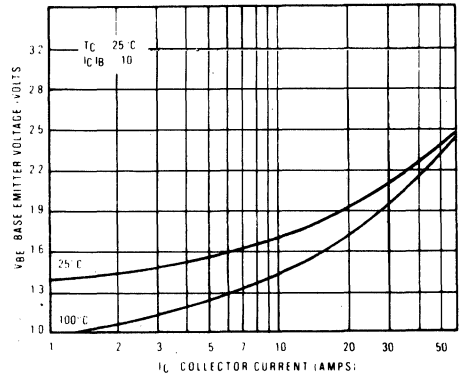


FIGURE 5 — THERMAL RESPONSE

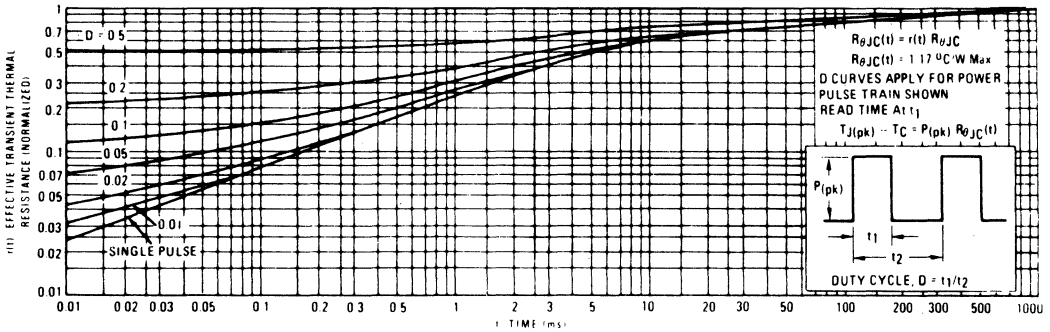


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

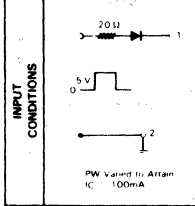
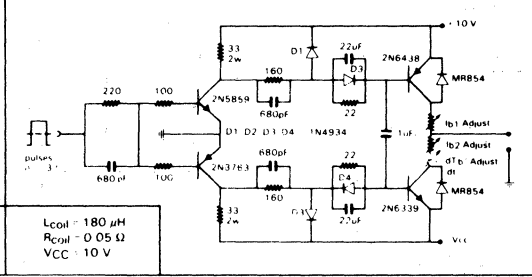
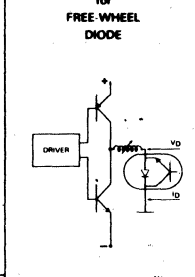
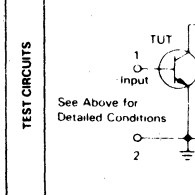
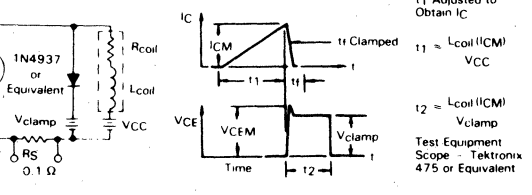
<p>INPUT CONDITIONS</p> 	<p>RBSOA AND INDUCTIVE SWITCHING</p> 	<p>TEST CIRCUIT for FREE-WHEEL DIODE</p> 
<p>CIRCUIT VALUES</p> <p>$L_{coil} = 10 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CE(sus)}$</p>	<p>$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 10 \text{ V}$</p>	
<p>TEST CIRCUITS</p> <p>INDUCTIVE TEST CIRCUIT</p> 	<p>OUTPUT WAVEFORMS</p> 	

FIGURE 6 - FALL TIME vs I_{B2}/I_{B1}

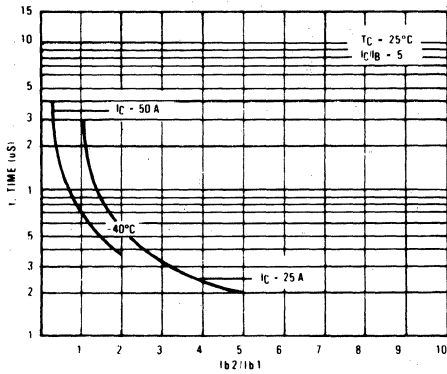


FIGURE 7 - TURN-OFF TIME vs I_C

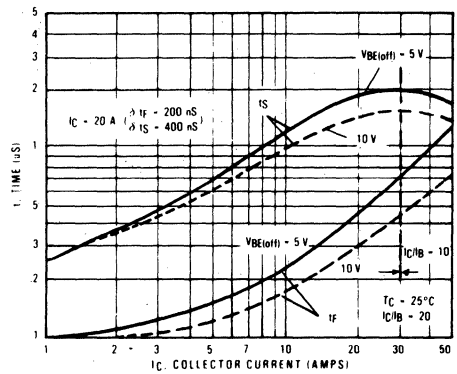


FIGURE 8 - STORAGE TIME vs FORCED GAIN

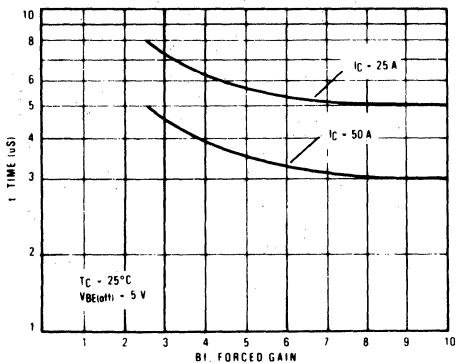
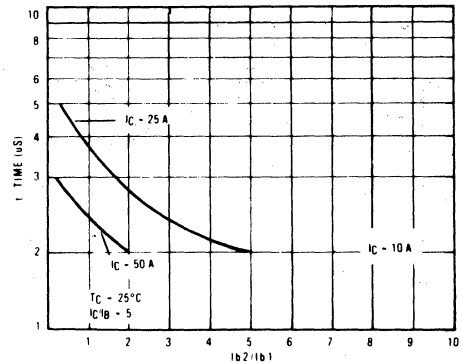


FIGURE 9 - STORAGE TIME vs I_{B2}/I_{B1}



FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 - FREE WHEEL DIODE MEASUREMENTS

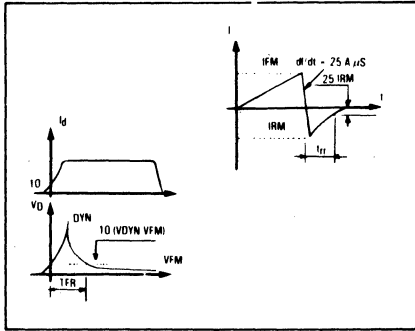


FIGURE 11 - FORWARD VOLTAGE

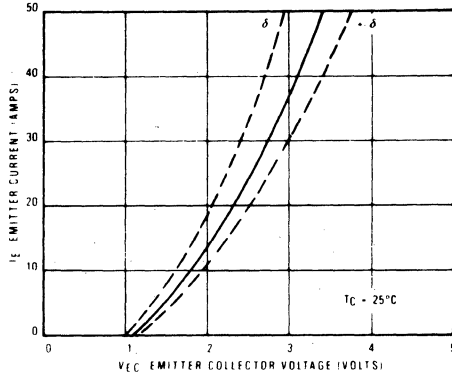


FIGURE 12 - FORWARD MODULATION VOLTAGE

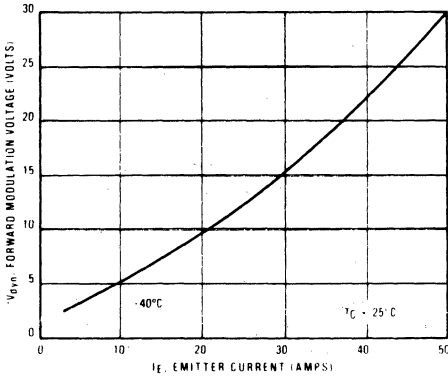


FIGURE 13 - PEAK REVERSE RECOVERY CURRENT

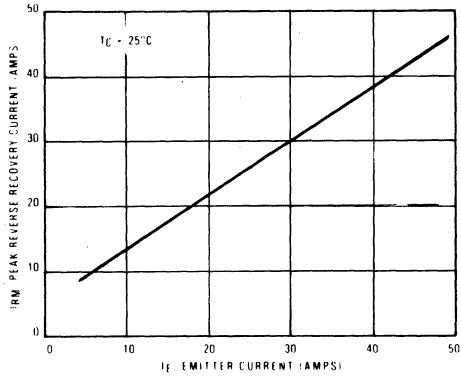


FIGURE 14 - FORWARD RECOVERY TIME

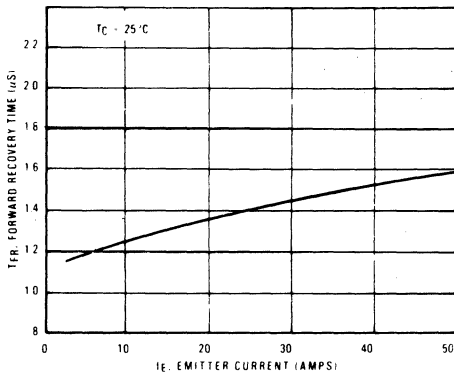
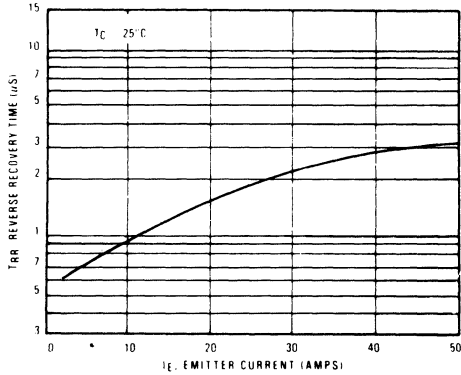


FIGURE 15 - REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 — SAFE OPERATING AREA

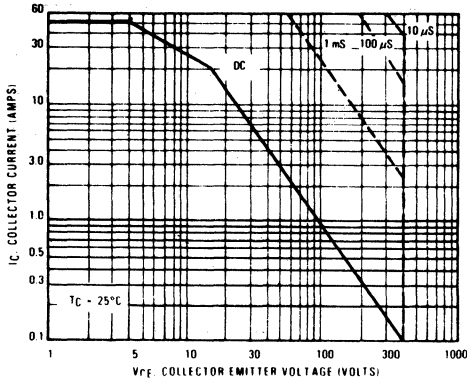


FIGURE 17 — REVERSE BIAS SAFE OPERATING AREA

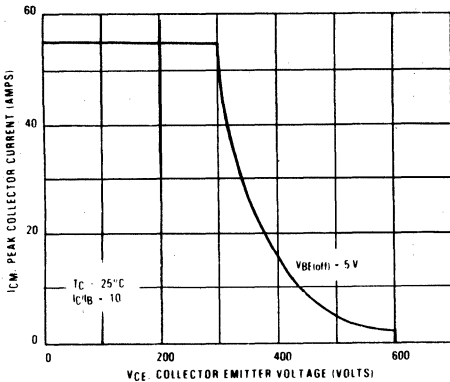
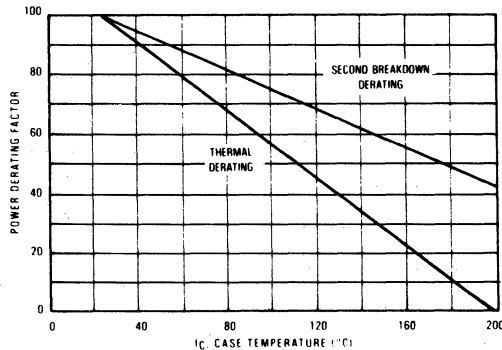


FIGURE 18 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

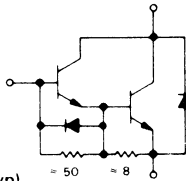
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

BUT34

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The BUT34 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 0.7 μ S Inductive Fall Time at 25°C (Typ)
 - 1.8 μ S Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range - 65 to 200°C



50 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS

850 VOLTS
250 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



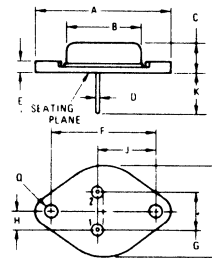
MAXIMUM RATINGS

Rating	Symbol	BUT34	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	500	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current			Adc
- Continuous	I_C	50	
- Peak (1)	I_{CM}	75	
Base Current			Adc
- Continuous	I_B	10	
- Peak (1)	I_{BM}	15	
Free Wheel Diode:			Adc
Forward current - Continuous	I_F	50	
- Peak	I_{FM}	75	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250	Watts
Derate above 25°C @ $T_C = 100^\circ\text{C}$		140	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle \leq 10%.



STYLE 1
 PIN 1 BASE
 2 EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.37	-	1.550	-
B	21.08	0.830		
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	-	3.43	-	0.135
F	29.90	30.40	1.177	1.197
G	10.87	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.84	17.15	0.665	0.675
K	11.18	12.15	0.440	0.480
O	3.84	4.09	0.151	0.161
R	-	26.67	-	1.050

CASE 197-01
 MODIFIED TO-3

BUT34

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Table 1) (IC = 100 mA, IB = 0)	VCEO(sus)	500	-	-	Vdc
Collector Cutoff Current (VCEV = Rated Value, VBE(off) = 1.5 Vdc) (VCEV = Rated Value, VBE(off) = 1.5 Vdc, TC = 100 °C)	ICEV	-	-	0.2 4.0	mAdc
Emitter Cutoff Current (VEB = 2.0 V, IC = 0)	IEBO	-	-	350	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	IS/b			See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	RBSOA			See Figure 17	

ON CHARACTERISTICS (1)

DC Current Gain (IC = 16 A, VCE = 5 V) (IC = 32 A, VCE = 5 V)	hFE	30 15	- -	- -	
Collector-Emitter Saturation Voltage (IC = 16 A, IB = 0.8 A) (IC = 32 A, IB = 3.2 A) (IC = 40 A, IB = 4 A) (IC = 50 A, IB = 10 A)	VCE(sat)	- - - -	- - - -	2.0 3.0 3.5 5.0	Vdc
Base-Emitter Saturation Voltage (IC = 16 A, IB = 0.8 A) (IC = 32 A, IB = 3.2 A) (IC = 40 A, IB = 4 A)	VBE(sat)	- - -	- - -	2.5 2.9 3.3	Vdc
Diode Forward Voltage (IF = 40 A)	Vf	-	-	4.0	Vdc

40°C

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	TC = 25°C	See Table 1 IC = 32 A	ts	-	1.8	3.0	μs
Fall Time			tf	-	0.7	1.5	μs
Storage Time	TC = 100°C	IB1 = 3.2 A	ts	-	2.2	-	μs
Fall Time			tf	-	0.8	-	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

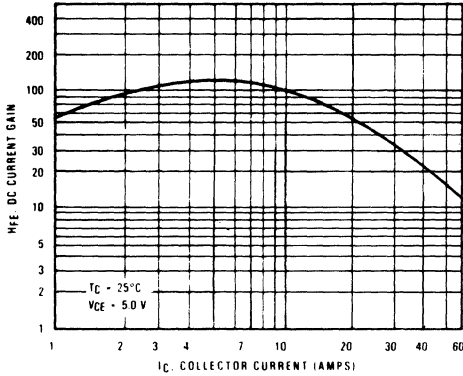


FIGURE 2 – COLLECTOR SATURATION REGION

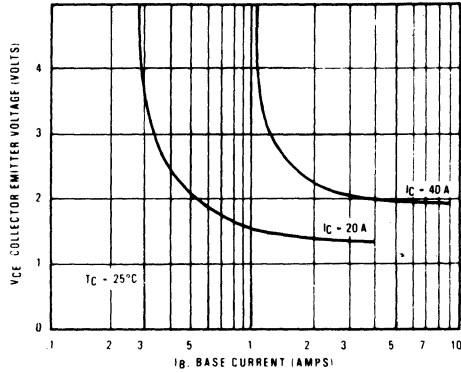


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

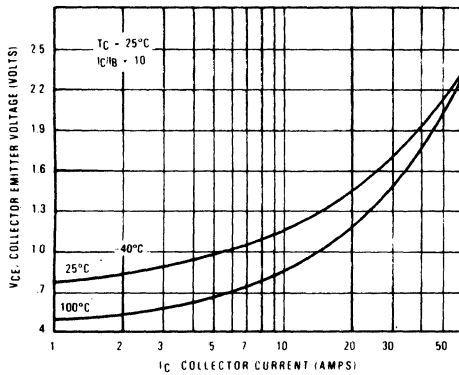


FIGURE 4 – BASE-EMITTER VOLTAGE

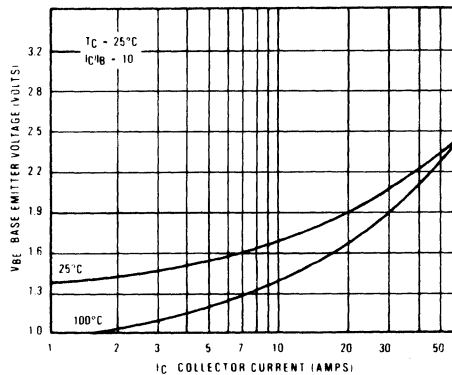


FIGURE 5 – THERMAL RESPONSE

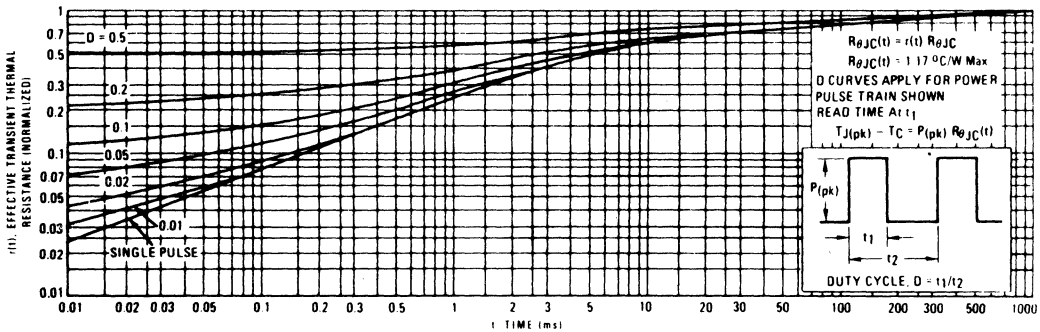


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

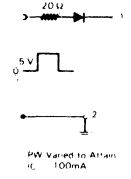
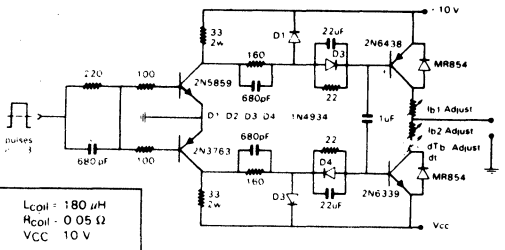
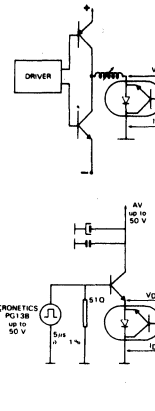
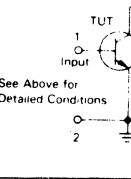
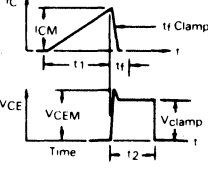
<p>INPUT CONDITIONS</p>  <p>PW Varied to Attain I_C I_C 100mA</p>	<p>RBSOA AND INDUCTIVE SWITCHING</p> 	<p>TEST CIRCUIT for FREE-WHEEL DIODE</p> 
<p>CIRCUIT VALUES</p> <p>$L_{coil} = 10 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CE(sus)}$</p>	<p>$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 10 \text{ V}$</p>	
<p>TEST CIRCUITS</p> <p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C $t_1 \approx L_{coil} (I_{CM}) / V_{CC}$ $t_2 \approx L_{coil} (I_{CM}) / V_{clamp}$</p> <p>Test Equipment Scope Tektronix 475 or Equivalent</p>	

FIGURE 6 - FALL TIME vs I_{B2}/I_{B1}

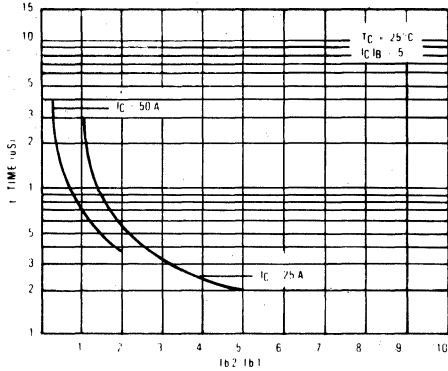


FIGURE 7 - TURN-OFF TIME vs I_C

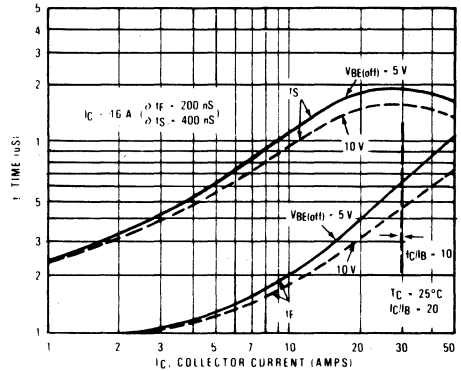


FIGURE 8 - STORAGE TIME vs FORCED GAIN

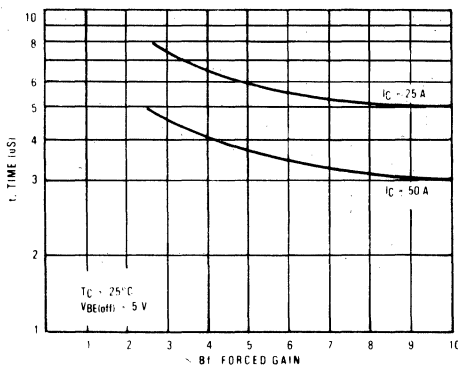
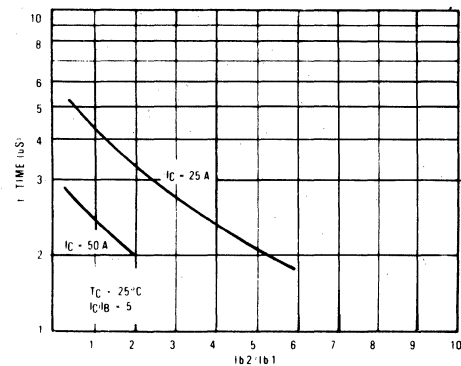


FIGURE 9 - STORAGE TIME vs I_{B2}/I_{B1}



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FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 – FREE WHEEL DIODE MEASUREMENTS

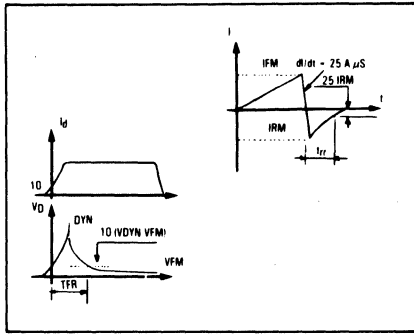


FIGURE 11 – FORWARD VOLTAGE

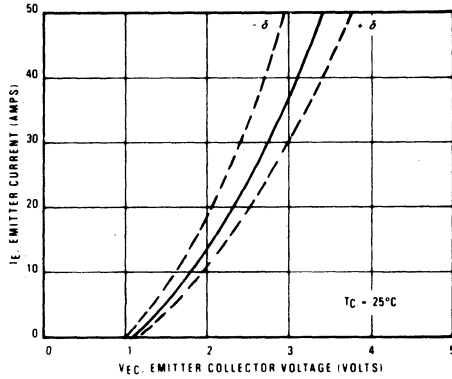


FIGURE 12 – FORWARD MODULATION VOLTAGE

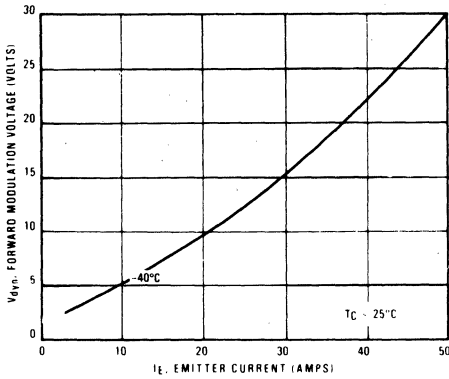


FIGURE 13 – PEAK REVERSE RECOVERY CURRENT

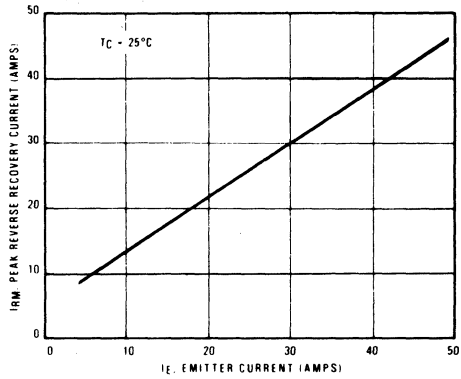


FIGURE 14 – FORWARD RECOVERY TIME

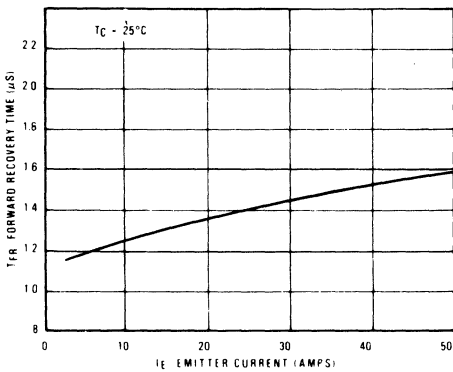
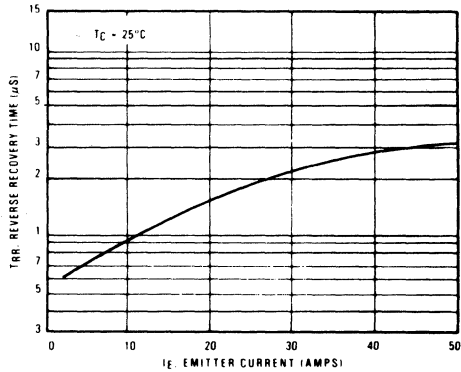


FIGURE 15 – REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 - SAFE OPERATING AREA

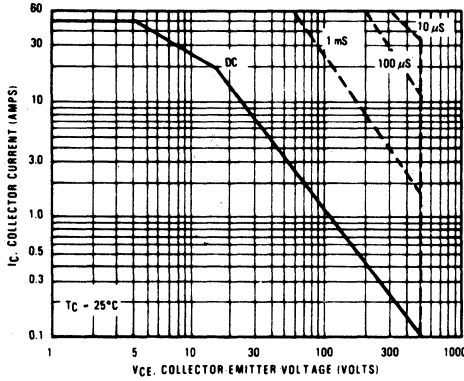
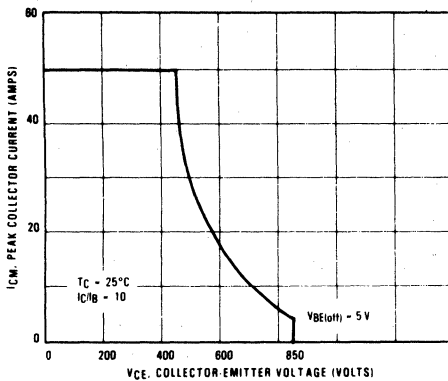


FIGURE 17 - REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC-VCE limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

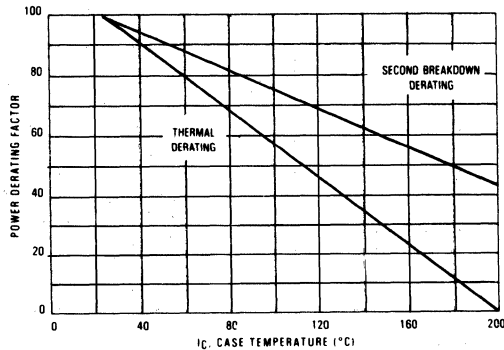
The data of Figure 16 is based on TC = 25°C; TJ(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when TC ≥ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

TJ(pk) may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

FIGURE 18 - POWER DERATING



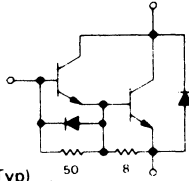
3

BUT35

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The BUT35 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
 - Switching Regulators
 - Inverters
 - Solenoid and Relay Drivers
 - Fast Turn-Off Times
- 550 nS Inductive Fall Time at 25°C (Typ)
 2.5 uS Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range - 65 to 200°C



40 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS
1000 VOLTS
250 WATTS

Designer's Data for
"Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



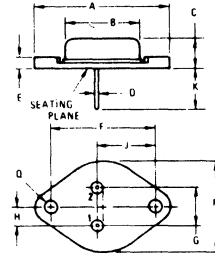
MAXIMUM RATINGS

Rating	Symbol	BUT35	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	700	Vdc
Collector-Emitter Voltage	V_{CEV}	1000	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current			Adc
- Continuous	I_C	40	
- Peak (1)	I_{CM}	50	
Base Current			Adc
- Continuous	I_B	10	
- Peak (1)	I_{BM}	20	
Free Wheel Diode:			Adc
Forward current	I_F	40	
Peak	I_{FM}	50	
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	250	Watts
Derate above 25°C @ $T_C = 100^\circ C$		140	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1
 PIN 1 BASE
 2 EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.37	1.550		
B	21.08	0.830		
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E		1.43		0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.58	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
D	3.84	4.29	0.151	0.169
R		26.67		1.050

CASE 197-01
 MODIFIED TO-3

BUT35

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (IC = 100 mA, IB = 0)	VCE(sus)	700	-	-	Vdc
Collector Cutoff Current (VCEV = Rated Value, VBE(off) = 1.5 Vdc) (VCEV = Rated Value, VBE(off) = 1.5 Vdc, TC = 100 °C)	ICEV	-	-	0.2 4.0	mAdc
Emitter Cutoff Current (VEB = 2.0 V, IC = 0)	IEBO	-	-	350	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	IS/b		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17	

ON CHARACTERISTICS (1)

DC Current Gain (IC = 12 A, VCE = 5 V) (IC = 24 A, VCE = 5 V)	hFE	30 15	- -	- -	
Collector Emitter Saturation Voltage (IC = 12 A, IB = 0.6 A) (IC = 24 A, IB = 2.4 A) (IC = 32 A, IB = 3.2 A) (IC = 40 A, IB = 8 A)	VCE(sat)	- - - -	- - - -	2.0 3.0 3.5 5.0	Vdc
Base-Emitter Saturation Voltage (IC = 12 A, IB = 0.6 A) (IC = 24 A, IB = 2.4 A) (IC = 32 A, IB = 3.2 A)	VBE(sat)	- - -	- - -	2.5 2.9 3.3	Vdc
Diode Forward Voltage (IF = 32 A)	Vf	-	-	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	TC = 25°C	See Table 1 IC = 24 A	ts	-	-	4.0	µs
Fall Time			tf	-	-	1.2	µs
Storage Time	TC = 100°C	IB1 = 2.4 A VBE(off) = 5 V	ts	-	2.8	-	µs
Fall Time			tf	-	0.65	-	µs

(1) Pulse Test: PW = 300 µs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

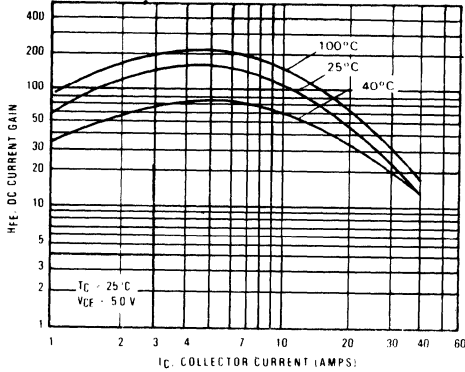


FIGURE 2 — COLLECTOR SATURATION REGION

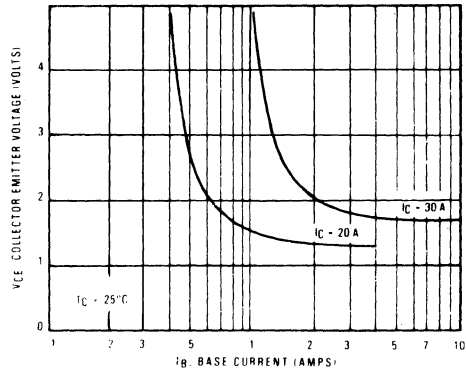


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

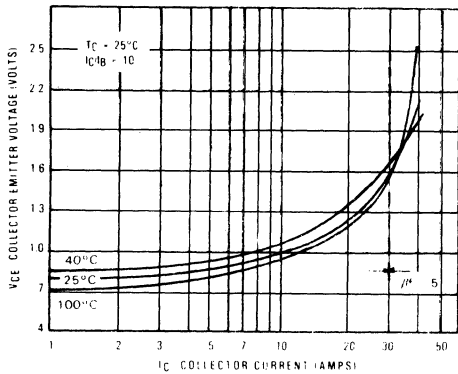


FIGURE 4 — BASE-EMITTER VOLTAGE

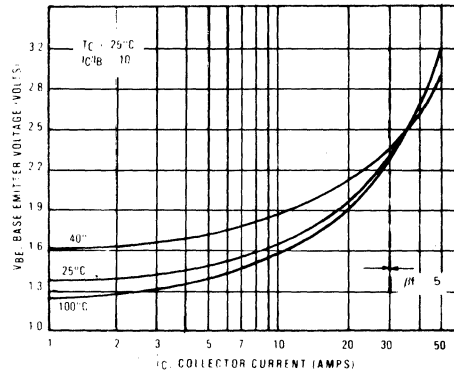


FIGURE 5 — THERMAL RESPONSE

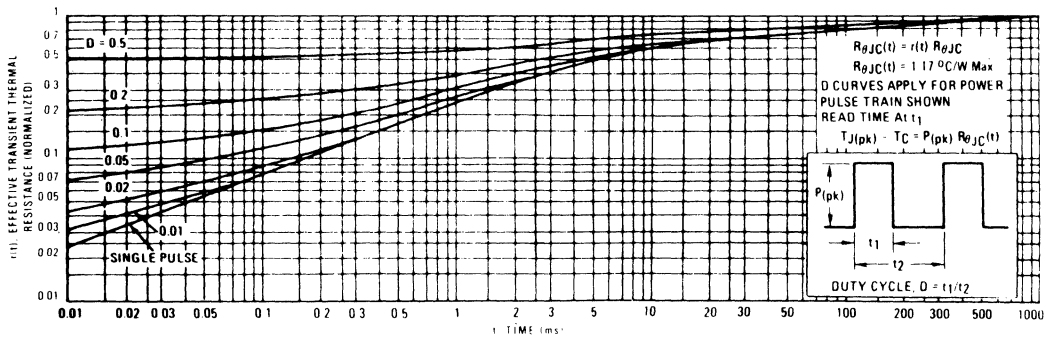


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

<p>VCE0(sus)</p> <p>INPUT CONDITIONS</p> <p>PW Varied to Attain IC IC = 100mA</p>	<p>RBSOA AND INDUCTIVE SWITCHING</p>	<p>TEST CIRCUIT for FREE-WHEEL DIODE</p>
<p>CIRCUIT VALUES</p> <p>L_{coil} = 10 mH V_{CC} = 10V R_{coil} = 0.7 Ω V_{clamp} VCE0(sus)</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 10 V</p>	
<p>TEST CIRCUITS</p> <p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t1 Adjusted to Obtain IC t1 = L_{coil}(ICM) / V_{CC} t2 = L_{coil}(ICM) / V_{clamp}</p> <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	

FIGURE 6 - FALL TIME vs IB2/IB1

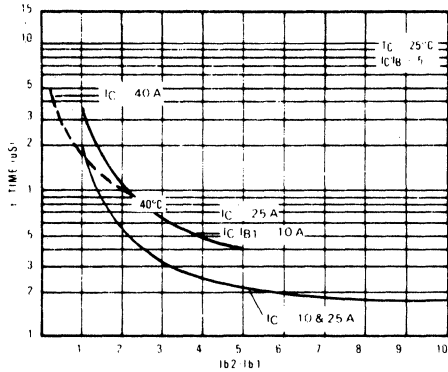


FIGURE 7 - TURN-OFF TIME vs IC

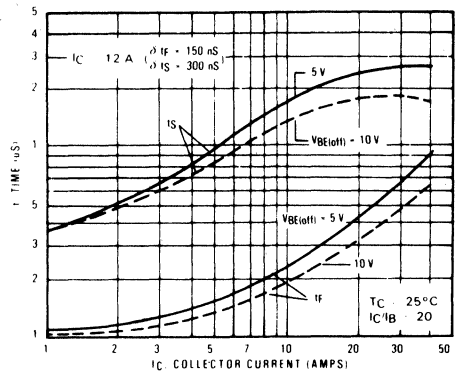


FIGURE 8 - STORAGE TIME vs FORCED GAIN

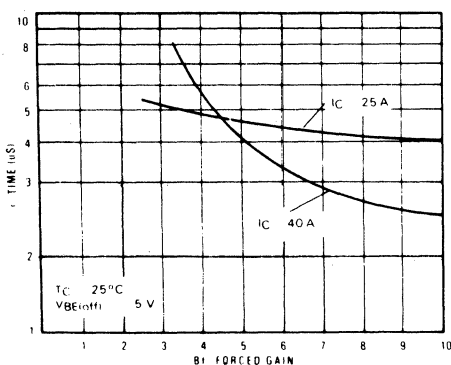
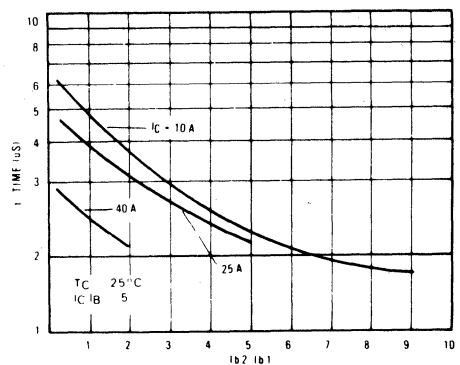


FIGURE 9 - STORAGE TIME vs Ib2/Ib1



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FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 – FREE WHEEL DIODE MEASUREMENTS

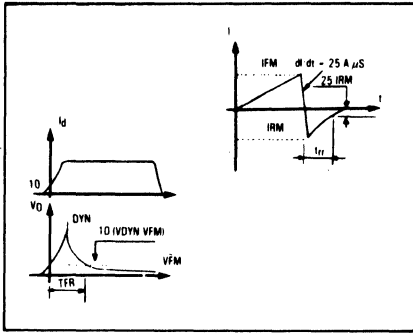


FIGURE 11 – FORWARD VOLTAGE

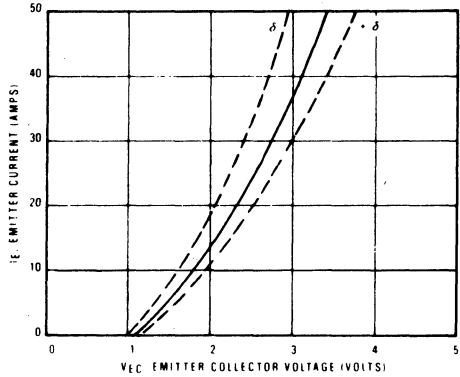


FIGURE 12 – FORWARD MODULATION VOLTAGE

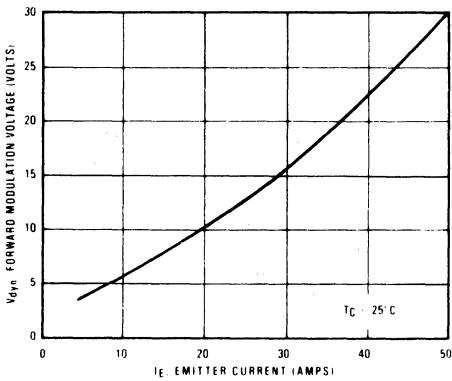


FIGURE 13 – PEAK REVERSE RECOVERY CURRENT

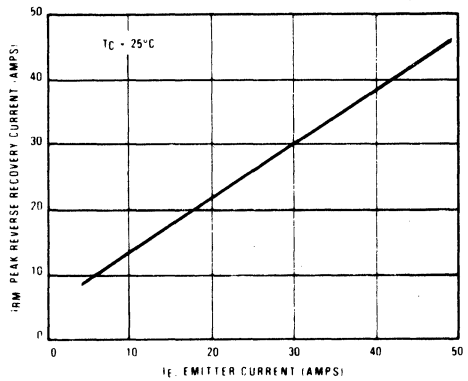


FIGURE 14 – FORWARD RECOVERY TIME

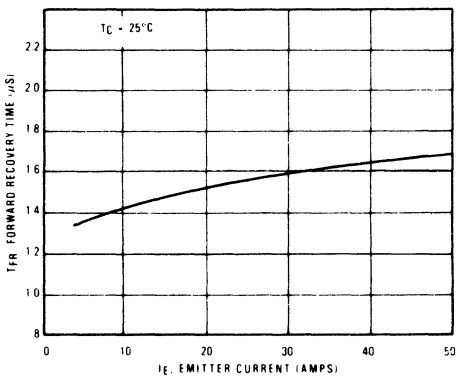
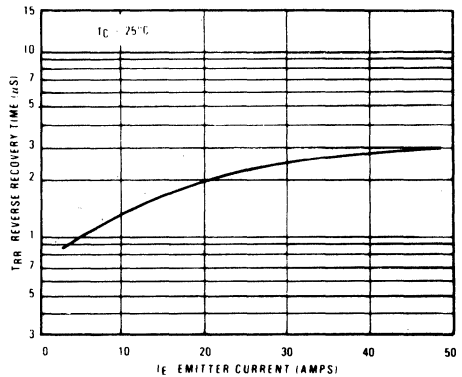


FIGURE 15 – REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 – SAFE OPERATING AREA

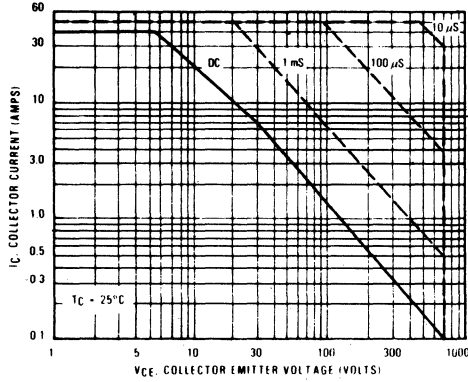
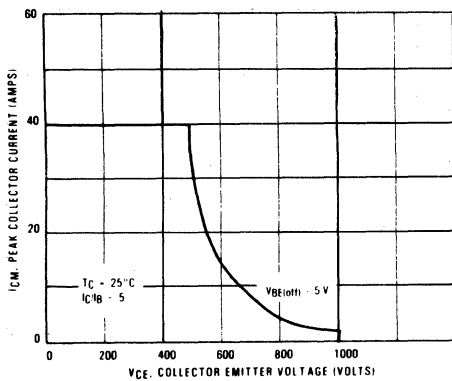


FIGURE 17 – REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

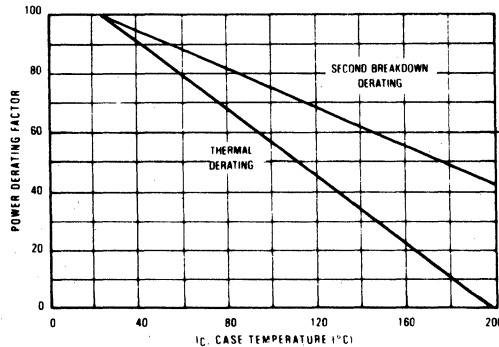
The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

FIGURE 18 – POWER DERATING

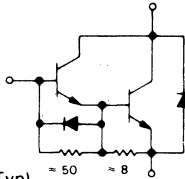


BUT36

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The BUT36 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times



1.7 μ S Inductive Fall Time at 100°C (Typ)
 4.5 μ S Inductive Storage Time at 100°C (Typ)

- Operating Temperature Range - 65 to 175°C

24 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS

1400 VOLTS
250 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.

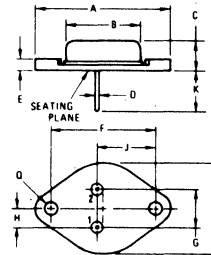


MAXIMUM RATINGS

Rating	Symbol	BUT36	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	1000	Vdc
Collector-Emitter Voltage	V_{CEV}	1400	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current			Adc
- Continuous	I_C	24	
- Peak (1)	I_{CM}	40	
Base Current			Adc
- Continuous	I_B	15	
- Peak (1)	I_{BM}	20	
Free Wheel Diode:			Adc
Forward current - Continuous	I_F	24	
- Peak	I_{FM}	40	
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	250	Watts
Derate above 25°C @ $T_C = 100^\circ C$		125	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C



STYLE 1:
 PIN 1 BASE
 2 EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	29.37	-	1.156
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	-	3.43	-	0.135
F	28.90	30.40	1.137	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.58	0.210	0.220
J	16.84	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	-	1.050

CASE 197-01
MODIFIED TO-3

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle \leq 10%.

BUT36

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (IC = 100 mA, IB = 0)	VCEO(sus)	1000	—	—	Vdc
Collector Cutoff Current (VCEV = Rated Value, VBE(off) = 1.5 Vdc) (VCEV = Rated Value, VBE(off) = 1.5 Vdc, TC = 100°C)	ICEV	—	—	0.2 4.0	mAdc
Emitter Cutoff Current (VEB = 2.0 V, IC = 0)	IEBO	—	—	350	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	IS/b		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17	

ON CHARACTERISTICS (1)

DC Current Gain (IC = 8 A, VCE = 5 V) (IC = 16 A, VCE = 5 V)	hFE	20 5	— —	— —	
Collector-Emitter Saturation Voltage (IC = 24 A, IB = 12 A)	VCE(sat)	—	—	5.0	Vdc
Base-Emitter Saturation Voltage (IC = 16 A, IB = 3.2 A)	VBE(sat)	—	—	3.3	Vdc
Diode Forward Voltage (IF = 24 A)	Vf	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	TC = 25°C	See Table 1	ts	—	—	6.0	μs
Fall Time			tf	—	—	2.5	μs
Storage Time	TC = 100°C	IB1 = 3.2 A	ts	—	4.5	—	μs
Fall Time			tf	—	1.7	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 - DC CURRENT GAIN

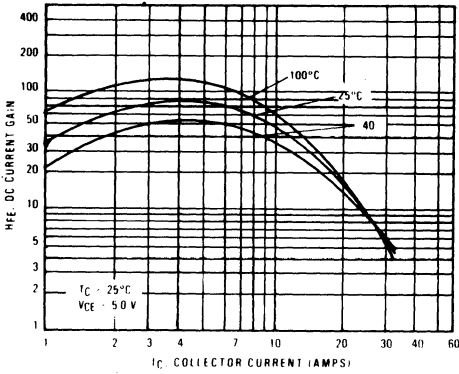


FIGURE 2 - COLLECTOR SATURATION REGION

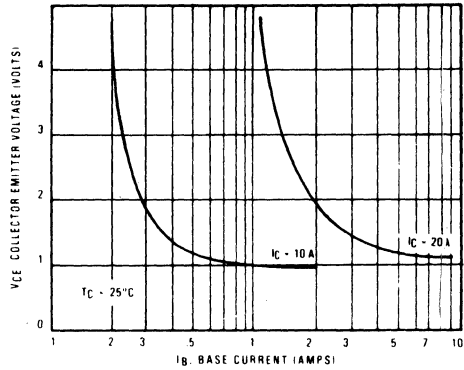


FIGURE 3 - COLLECTOR-EMITTER SATURATION VOLTAGE

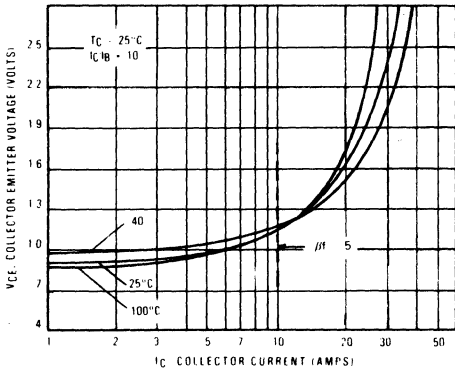


FIGURE 4 - BASE-EMITTER VOLTAGE

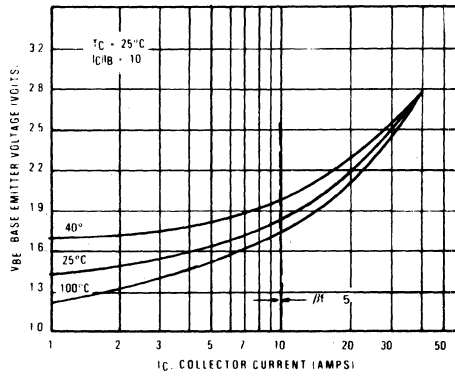


FIGURE 5 - THERMAL RESPONSE

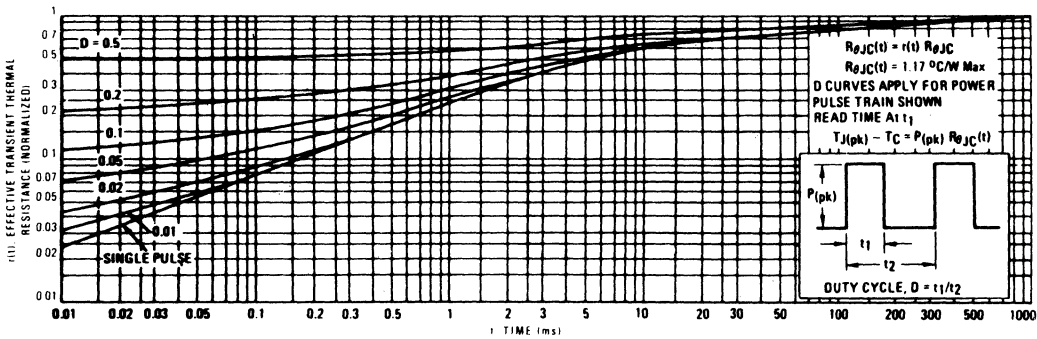


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

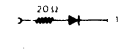
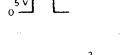
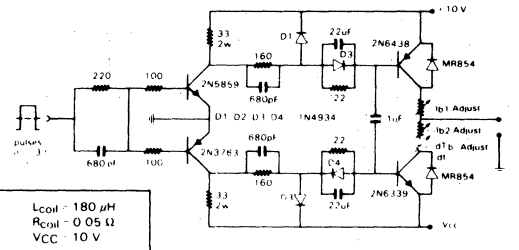
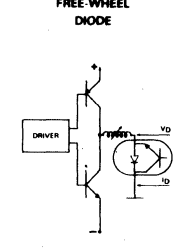
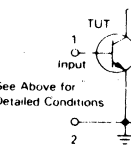
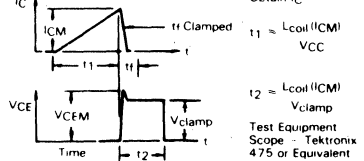
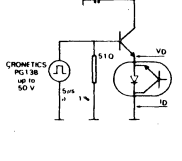
<p>VCE0(sus)</p>  <p>INPUT CONDITIONS</p>  <p>PW Varied to Attain IC = 100mA</p>	<p>RBSOA AND INDUCTIVE SWITCHING</p> 	<p>TEST CIRCUIT for FREE-WHEEL DIODE</p> 
<p>CIRCUIT VALUES</p> <p>L_{coil} = 10 mH V_{CC} = 10V R_{coil} = 0.7 Ω V_{clamp} = V_{CE0(sus)}</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 10 V</p>	
<p>TEST CIRCUITS</p> <p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain IC</p> <p>t₁ ≈ L_{coil} / (ICM - V_{CC})</p> <p>t₂ ≈ L_{coil} / (ICM - V_{clamp})</p> <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	 <p>CRONICS PCT 38 up to 50 V</p>

FIGURE 6 - FALL TIME vs IB2/IB1

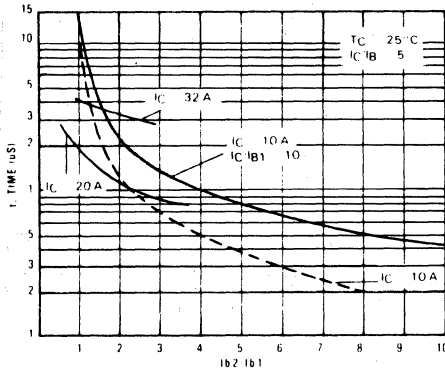


FIGURE 7 - TURN-OFF TIME vs IC

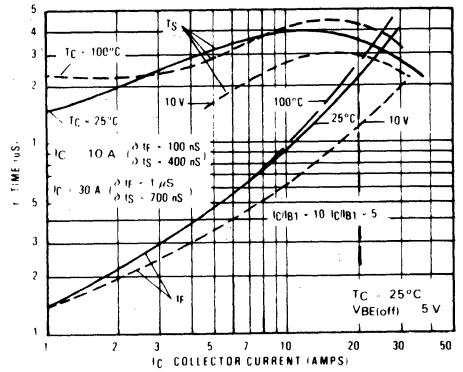


FIGURE 8 - STORAGE TIME vs FORCED GAIN

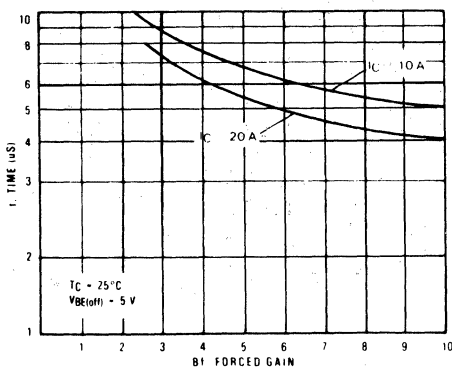
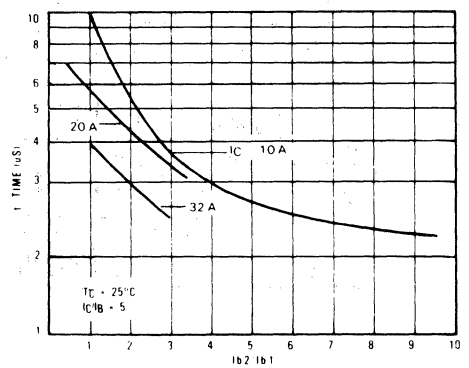


FIGURE 9 - STORAGE TIME vs IB2/IB1



3

FREE-WHEEL DIODE CHARACTERISTICS

FIGURE 10 – FREE WHEEL DIODE MEASUREMENTS

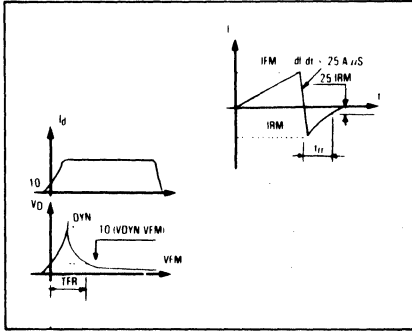


FIGURE 11 – FORWARD VOLTAGE

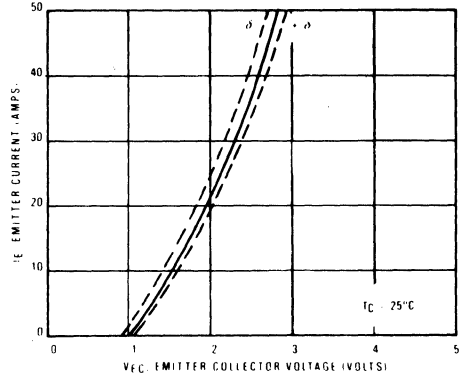


FIGURE 12 – FORWARD MODULATION VOLTAGE

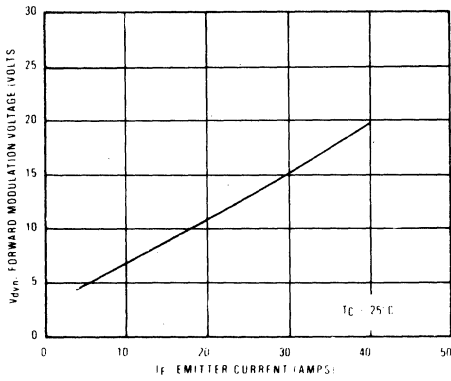


FIGURE 13 – PEAK REVERSE RECOVERY CURRENT

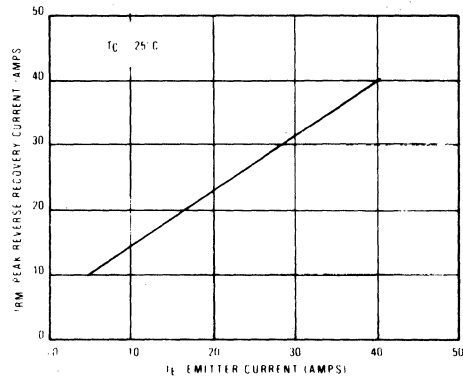


FIGURE 14 – FORWARD RECOVERY TIME

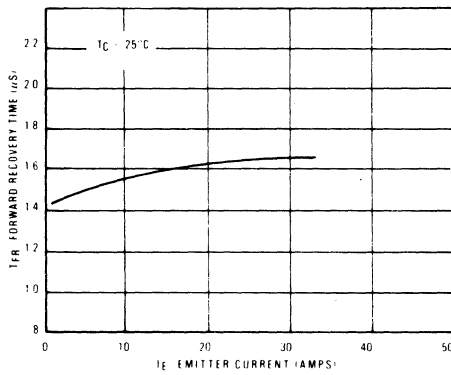
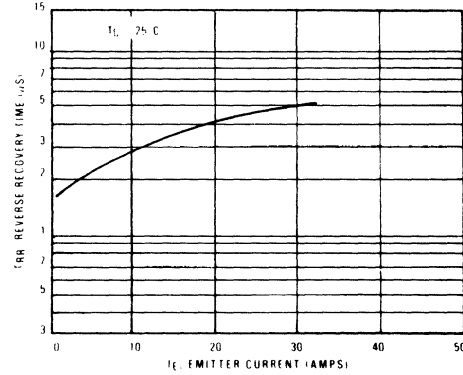


FIGURE 15 – REVERSE RECOVERY TIME



The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

FIGURE 16 – SAFE OPERATING AREA

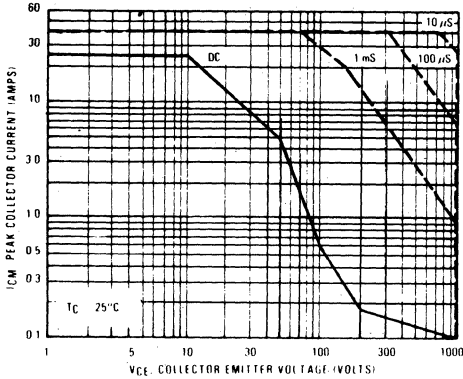


FIGURE 17 – REVERSE BIAS SAFE OPERATING AREA

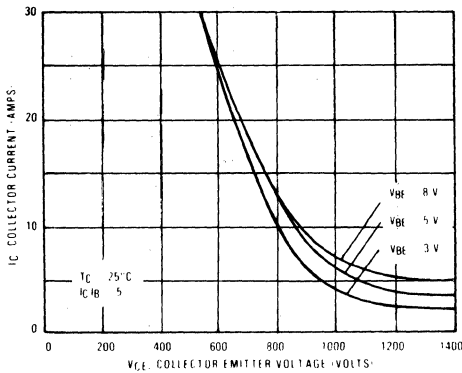
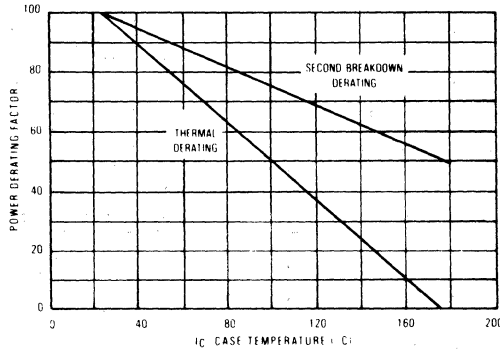


FIGURE 18 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_J(pk)$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

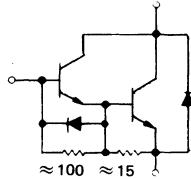
BUT50P

ADVANCE INFORMATION

SWITCHMODE^A SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

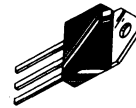
The BUT50P darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switch-mode applications such as :

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



8 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS

500 VOLTS - $V_{CEO(sus)}$
100 WATTS
850 VOLTS - V_{CES}



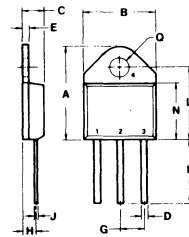
MAXIMUM RATINGS

Rating	Symbol	BUT50P	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	500	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	850	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	8	Vdc
Collector Current - Continuous	I_C	8	Adc
- Peak (1)	I_{CM}	16	
Base Current - Continuous	I_B	2	Adc
- Peak (1)	I_{BM}	4	
Free Wheel Diode :			Adc
Forward Current - continous	I_F	8	
- peak	I_{FM}	16	
Total Power Dissipation @ $T_C=25^\circ C$	P_D	100	Watts
@ $T_C=100^\circ C$		40	
Derate above $25^\circ C$.8	W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to + 150	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^\circ C/W$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.



STYLE 1
 1 BASE
 2 COLLECTOR
 3 EMITTER
 4 COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	.800	0.830
B	15.49	15.90	0.610	0.628
C	4.19	5.08	0.165	0.200
D	1.92	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
F	5.21	5.72	0.206	0.225
H	2.41	2.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	16.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
O	2.94	4.19	0.116	0.165

Case 340-01
TO-218AC

BUT50P

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	500	—	—	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	—	—	0.25 2.5	mAdc
Emitter Cutoff Current (V _{EB} = 8.0 V, I _C = 0)	I _{EBO}	—	—	175	mAdc

ON CHARACTERISTICS (1)

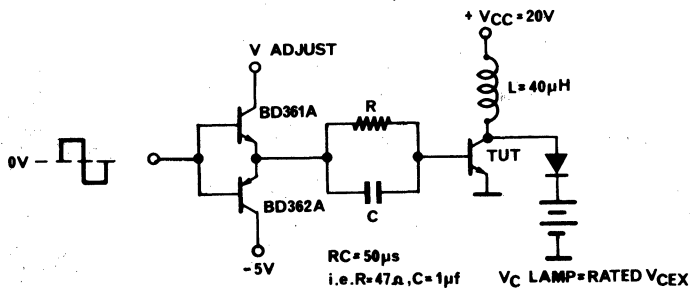
DC Current Gain (I _C = 2 Adc, V _{CE} = 5 V)	h _{FE}	30	—	—	—
Collector-Emitter Saturation Voltage (I _C = 5 Adc, I _B = 0.25 Adc) (I _C = 8 Adc, I _B = 1 Adc) (I _C = 5 Adc, I _B = 0.25 Adc, T _C = 100°C)	V _{CE(sat)}	—	—	2.0 3.0 2.5	Vdc
Base-Emitter Saturation Voltage (I _C = 5 Adc, I _B = 0.25 Adc) (I _C = 5 Adc, I _B = 0.25 Adc, T _C = 100°C)	V _{BE(sat)}	—	—	2.5 2.5	Vdc
Diode Forward Voltage (I _F = 5 Adc)	V _f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped

Storage Time	(I _C = 5 A, I _{B1} = 0.25 A, V _{be(off)} = 5 V)	t _s	—	0.75	—	μs
Fall Time		t _f	—	0.10	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%



SWITCHING TIMES TEST CIRCUIT

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

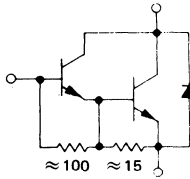
BUT51P

ADVANCE INFORMATION

SWITCHMODE^Δ SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

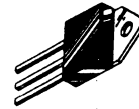
The BUT51P darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switch-mode applications such as :

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



15 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTORS

500 VOLTS - $V_{ce0(sus)}$
100 WATTS
850 VOLTS - V_{ces}



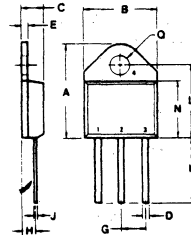
MAXIMUM RATINGS

Rating	Symbol	BUT51P	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	500	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	850	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	8	Vdc
Collector Current - Continuous	I_C	15	Adc
Collector Current - Peak (1)	I_{CM}	25	
Base Current - Continuous	I_B	2.5	Adc
Base Current - Peak (1)	I_{BM}	5	
Free Wheel Diode :			Adc
Forward Current - continuous	I_F	15	
Forward Current - peak	I_{FM}	25	
Total Power Dissipation @ $T_C=25^{\circ}C$	P_D	125	Watts
Derate above $25^{\circ}C$		50	
Derate above $25^{\circ}C$		1	W/ $^{\circ}C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to + 150	$^{\circ}C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	$^{\circ}C/W$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.



STYLE 1:
 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.00	.800	0.830
B	15.48	15.90	0.610	0.625
C	4.19	5.00	0.165	0.200
D	1.92	1.65	0.040	0.065
E	1.35	1.68	0.053	0.066
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.125
J	0.50	0.84	0.015	0.035
K	12.70	16.48	0.500	0.650
L	15.88	16.51	0.625	0.650
M	12.19	12.70	0.480	0.500
O	3.94	4.19	0.155	0.165

Case 340-01
TO-218AC

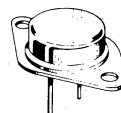
BUV10N

SWITCHMODE^Δ SERIES
NPN SILICON POWER TRANSISTOR

... designed for high current, high speed, high power applications.

- HFe min.: 20 at $I_C = 10$ A
- T_F max. = 0.45 μ s at $I_C = 15$ A
- Equivalent to BDY58

25 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
125 VOLTS
175 WATTS

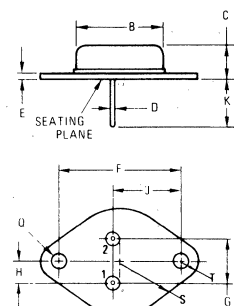


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	125	Vdc
Collector-Base Voltage	V_{CB0}	160	Vdc
Emitter-Base Voltage	V_{EB0}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	160	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	140	Vdc
Collector-Current – continuous	I_C	25	A dc
– peak ($p_w \leq 10$ ms)	I_{CM}	30	A pk
Base-Current continuous	I_B	6	A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	$^\circ\text{C/W}$

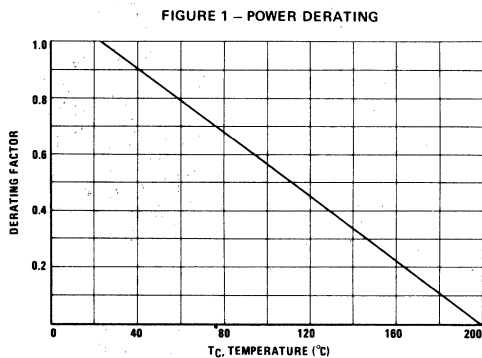


STYLE 1:
 PIN 1 BASE
 2 EMITTER
 CASE-COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
 (TO-3)



BUV10N

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage (I _C = 200 mA, I _B = 0, L = 25 mH)	V _{CE(sus)}	125		V _{dc}
Collector Cutoff Current at Reverse Bias: (V _{CE} = 160 V, V _{BE} = -1.5 V) (V _{CE} = 160 V, V _{BE} = -1.5 V, T _C = 125°C)	I _{CEX}		1.5 6	mAdc
Collector-Emitter Cutoff Current (V _{CE} = 100 V)	I _{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage (I _E = 50 mA)	V _{EBO}	7		V
Emitter-Cutoff Current (V _{EB} = 5 V)	I _{EBO}		0.5	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased (V _{CE} = 20 V, t = 0.5 s) (V _{CE} = 48 V, t = 0.5 s)	I _{S/b}	8.75 1.0		A _{dc}
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ON CHARACTERISTICS¹

DC Current Gain (I _C = 10 A, V _{CE} = 4 V) (I _C = 20 A, V _{CE} = 4 V)	h _{FE}	20 10	60	
Collector-Emitter Saturation Voltage (I _C = 10 A, I _B = 1 A) (I _C = 20 A, I _B = 2 A)	V _{CE(sat)}		1 2.0	V _{dc}
Base-Emitter Saturation Voltage (I _C = 10 A, I _B = 1 A)	V _{BE(sat)}		1.5	V _{dc}

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product (V _{CE} = 15 V, I _C = 1 A, f = 4 MHz)	f _T	10.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	I _C = 15 A, I _{B1} = I _{B2} = 1.5 A, (V _{CC} = 75 V, R _C = 5 Ω)	t _{on}	1.0	μs
Storage Time		t _s	1.55	
Fall Time		t _f	0.45	

¹ Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

BUV10N

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

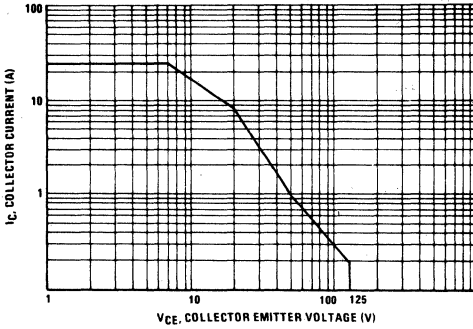


FIGURE 3 – "ON" VOLTAGES

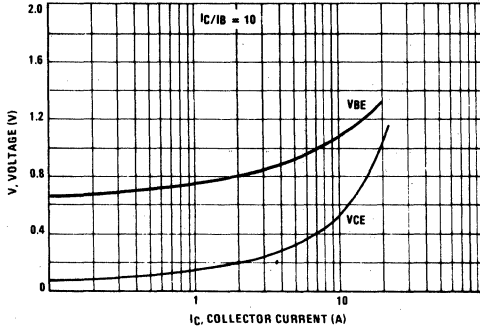
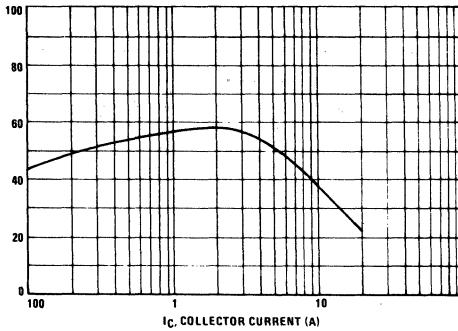


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

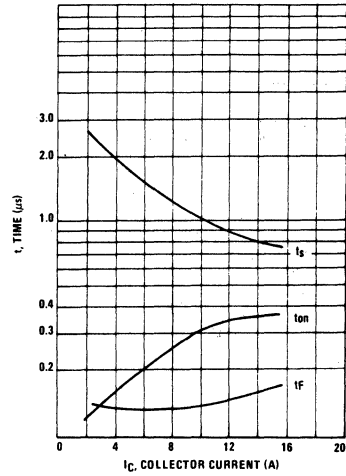
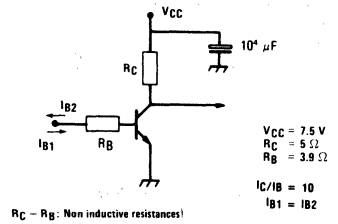


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

BUV11

SWITCHMODE^A SERIES
NPN SILICON POWER TRANSISTOR

... designed for high current, high speed, high power applications.

- High DC current gain: HFE min. = 20 at $I_C = 6$ A
- Low $V_{CE(sat)}$. $V_{CE(sat)}$ max. = 0.6 V at $I_C = 6$ A
- Very fast switching times:
 T_F max. = 0.8 μ s at $I_C = 12$ A

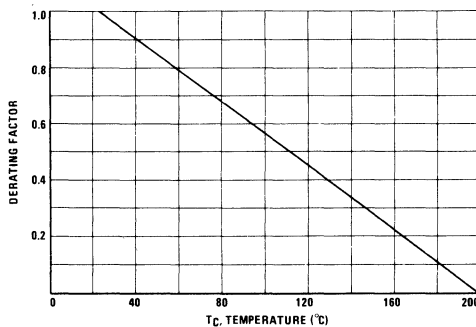
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	200	Vdc
Collector-Base Voltage	V_{CB0}	250	Vdc
Emitter-Base Voltage	V_{EB0}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	250	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	240	Vdc
Collector-Current — continuous	I_C	20	A _{dc}
— peak ($p_w \leq 10$ ms)	I_{CM}	25	A _{pk}
Base-Current continuous	I_B	4	A _{dc}
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

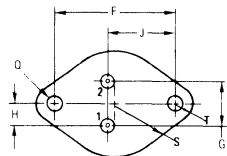
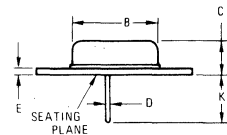
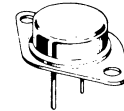
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C/W}$

FIGURE 1 — POWER DERATING



20 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
200 VOLTS
150 WATTS



STYLE 1:
 PIN 1. BASE
 PIN 2. EMITTER
 CASE. COLLECTOR
 STYLE 2:
 PIN 1. BASE
 PIN 2. COLLECTOR
 CASE. EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
 (TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 250\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 250\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.5 6	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 160\text{ V}$)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	5.0 0.15		A _{dc}
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 6\text{ A}$, $V_{CE} = 2\text{ V}$) ($I_C = 12\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 6\text{ A}$, $I_B = 0.6\text{ A}$) ($I_C = 12\text{ A}$, $I_B = 1.5\text{ A}$)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 1.5\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
--	-------	-----	--	-----

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 12\text{ A}$, $I_{B1} = I_{B2} = 1.5\text{ A}$, ($V_{CC} = 150\text{ V}$, $RC = 12.5\ \Omega$)	t_{on}	0.8	μs
Storage Time		t_s	1.8	
Fall Time		t_f	0.4	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

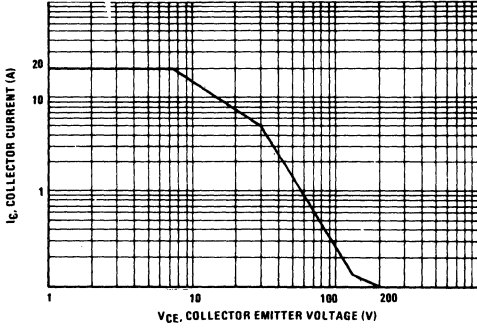


FIGURE 3 – "ON" VOLTAGES

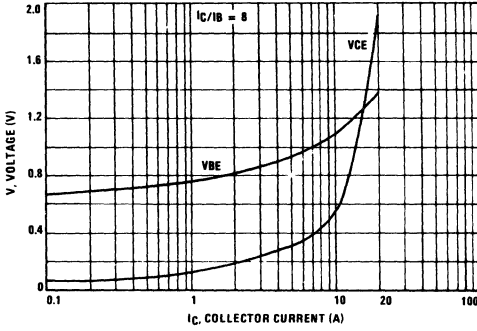
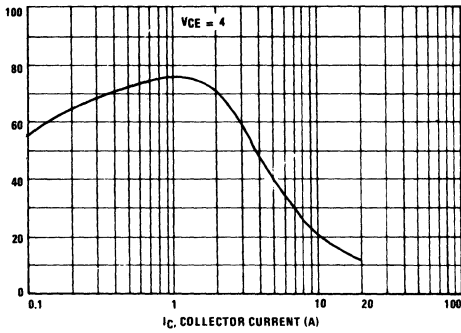


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC-VCE limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on TC = 25°C; TJ(pk) is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – SWITCHING TIMES VERSUS COLLECTOR CURRENT

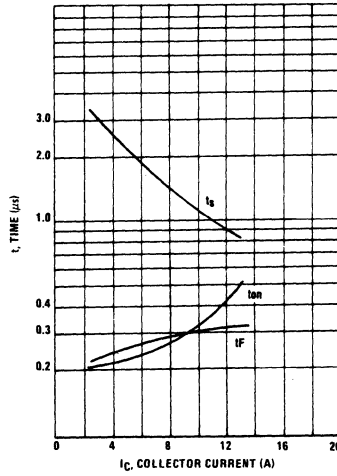
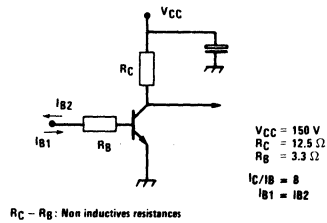


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT

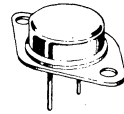


NPN SILICON POWER METAL TRANSISTOR

... designed for high speed, high current, high power applications.

- High DC Current gain — H_{FE} min 20 @ $I_C = 8$ A
- Very fast switching times
 t_F max. = 0.25 μ s @ $I_C = 15$ A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$ max. = 0.6 V, @ $I_C = 8$ A
- High V_{CEO} : 160 V.

**NPN SILICON
 POWER
 METAL TRANSISTOR**
20 AMPERES



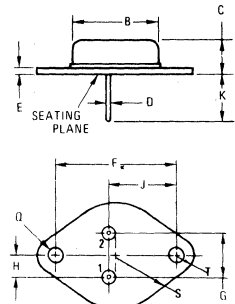
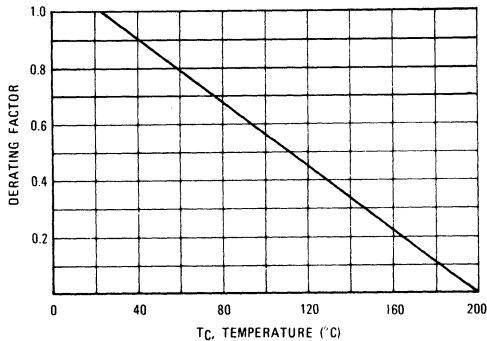
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	160	Vdc
Collector-Base Voltage	V_{CBO}	220	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	220	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	200	Vdc
Collector-Current — continuous	I_C	20	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	25	Apk
Base-Current continuous	I_B	5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C/W}$

FIGURE 1 — POWER DERATING



STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

STYLE 2:
 PIN 1: BASE
 2: COLLECTOR
 CASE: EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.84	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
 (TO 3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CEO(sus)}$	160		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 220\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 220\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.5 6.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 130\text{ V}$)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	5 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 8\text{ A}$, $V_{CE} = 2\text{ V}$) ($I_C = 15\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 0.8\text{ A}$) ($I_C = 15\text{ A}$, $I_B = 1.88\text{ A}$)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 15\text{ A}$, $I_B = 1.88\text{ A}$)	$V_{BE(sat)}$		1.8	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8		MHz
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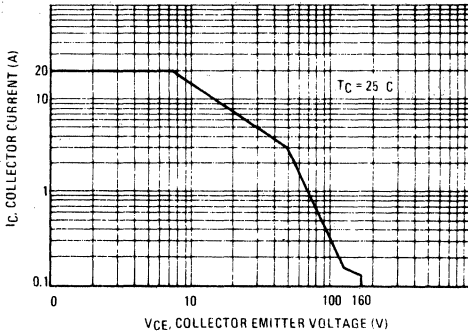
SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$(I_C = 15\text{ A}$, $I_{B1} = I_{B2} = 1.88\text{ A}$, $V_{CC} = 30\text{ V}$, $R_L \approx 2\Omega$)	t_{on}		1.2	μs
Storage Time		t_s		1.2	
Fall Time		t_f		0.25	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.



FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Average operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

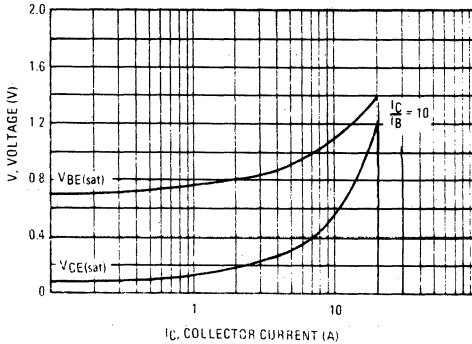


FIGURE 4 – DC CURRENT GAIN

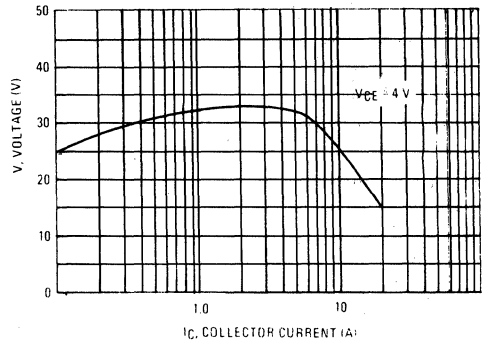


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

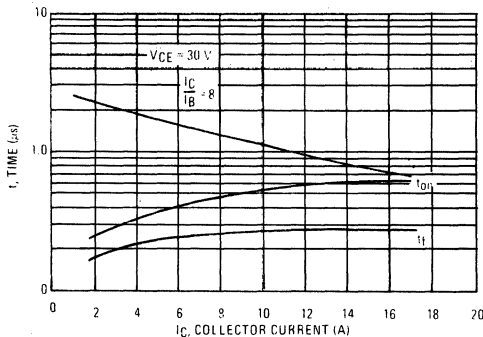
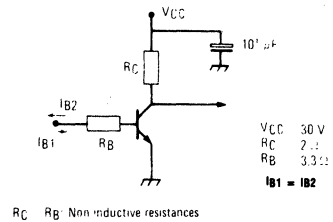


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

BUV12

SWITCHMODE^Δ SERIES
NPN SILICON POWER TRANSISTOR

... designed for high speed, high voltage, high power applications.

- High DC current gain:
 HFE min. = 20 at $I_C = 5\text{ A}$
- Very fast switching times:
 T_S max. = 1.5 μs at $I_C = 10\text{ A}$
 T_F max. = 0.5 μs at $I_C = 10\text{ A}$

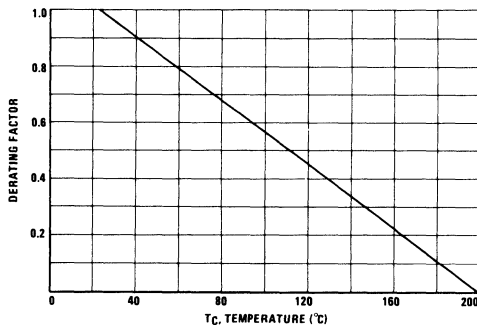
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector-Base Voltage	V_{CBO}	300	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5\text{ V}$)	V_{CEX}	300	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	290	Vdc
Collector-Current – continuous	I_C	20	Adc
– peak ($p_w \leq 10\text{ ms}$)	I_{CM}	25	Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

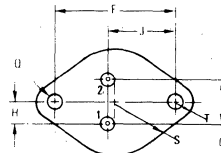
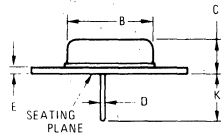
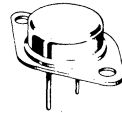
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C/W}$

FIGURE 1 – POWER DERATING



20 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
250 VOLTS
150 WATTS



STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR
 STYLE 2:
 PIN 1: BASE
 2: COLLECTOR
 CASE: EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.206	0.225
J	16.64	17.15	0.656	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1 03
 (TO 3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS¹				
Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CEO(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.5 6	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 200\text{ V}$)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	5.0 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 5\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 10\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 5\text{ A}$, $I_B = 0.5\text{ A}$) ($I_C = 10\text{ A}$, $I_B = 1.25\text{ A}$)	$V_{CE(sat)}$		1.0 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 1.25\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 10\text{ A}$, $I_{B1} = I_{B2} = 1.25\text{ A}$, ($V_{CC} = 150\text{ V}$, $R_C = 15\ \Omega$)	t_{on}	0.7	μs
Storage Time		t_s	1.5	
Fall Time		t_f	0.5	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

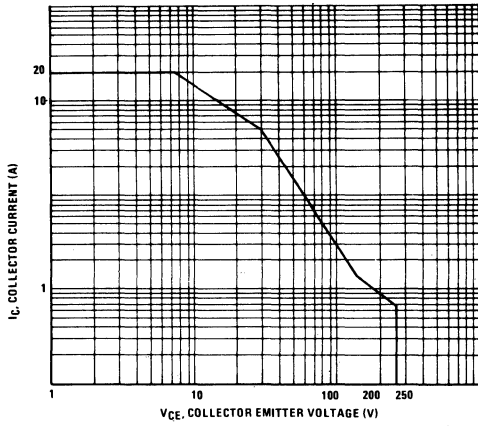


FIGURE 3 – "ON" VOLTAGES

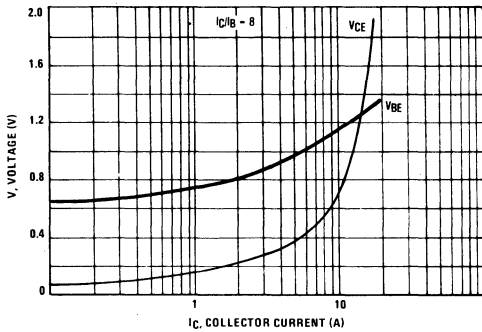
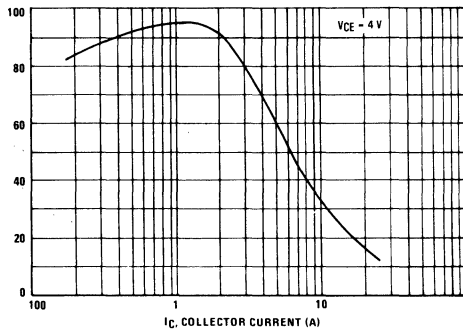


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC-VCE limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of figure 2 is based on TC = 25°C; TJ(pk) is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

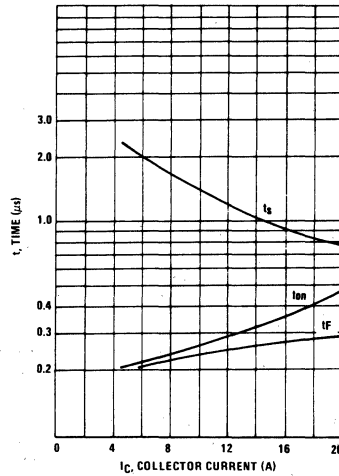
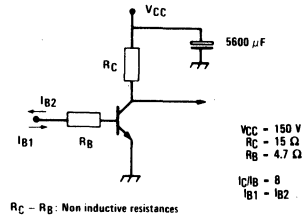


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



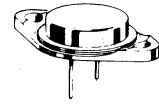
BUV20

SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTOR

... designed for high speed, high current, high power applications.

- High DC current gain:
 HFE min. = 20 at $I_C = 25$ A
 = 10 at $I_C = 50$ A
- Low $V_{CE(sat)}$:
 $V_{CE(sat)}$ max. = 0.6 V at $I_C = 25$ A
 = 1.2 V at $I_C = 50$ A
- Very fast switching times:
 $T_F = 0.25 \mu s$ at $I_C = 50$ A

50 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
125 VOLTS
250 WATTS

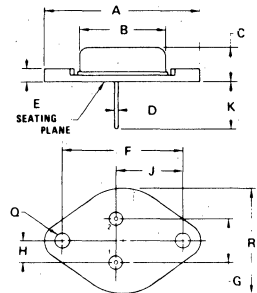


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	125	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	160	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	150	Vdc
Collector-Current — continuous	I_C	50	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	60	Apk
Base-Current continuous	I_B	10	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

THERMAL CHARACTERISTICS

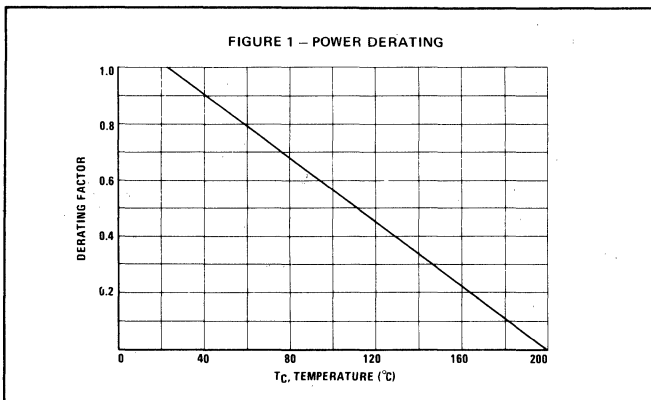
Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ C/W$



STYLE 1:
 PIN 1. BASE
 PIN 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	8.35	7.62	0.250	0.300
D	1.45	1.90	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
 MODIFIED TO 3



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 140\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 140\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 100\text{ V}$)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 20\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 40\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	12 1.5		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 25\text{ A}$, $V_{CE} = 2\text{ V}$) ($I_C = 50\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 25\text{ A}$, $I_B = 2.5\text{ A}$) ($I_C = 50\text{ A}$, $I_B = 5\text{ A}$)	$V_{CE(sat)}$		0.6 1.2	Vdc
Base-Emitter Saturation Voltage ($I_C = 50\text{ A}$, $I_B = 5\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 50\text{ A}$, $I_{B1} = I_{B2} = 5\text{ A}$, ($V_{CC} = 30\text{ V}$, $R_C = 0.6\ \Omega$)	t_{on}	1.5	μs
Storage Time		t_s	1.2	
Fall Time		t_f	0.25	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

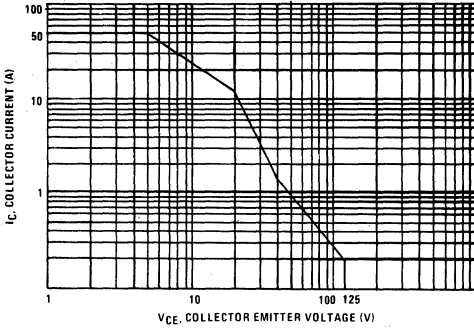


FIGURE 3 – "ON" VOLTAGES

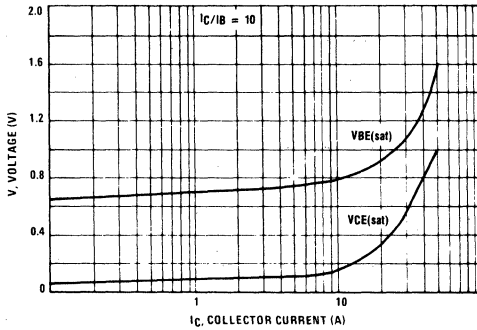
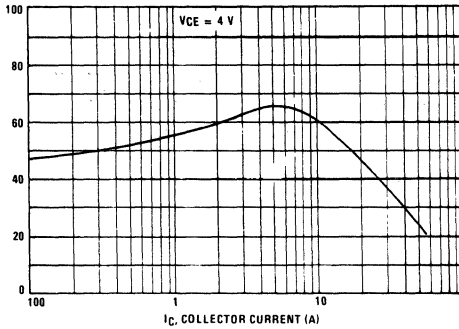


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

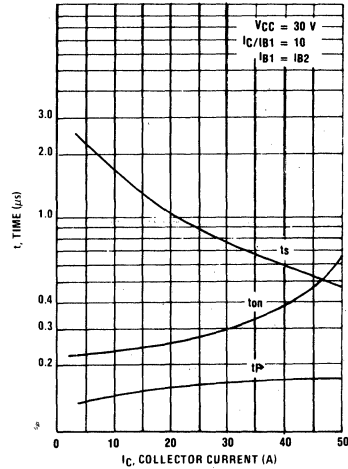
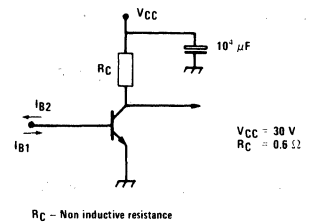


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

BUV21

SWITCHMODE^A SERIES
NPN SILICON POWER TRANSISTOR

... designed for high speed, high current, high power applications.

- High DC current gain:
 HFE min. = 20 at $I_C = 12\text{ A}$
- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 0.6 V at $I_C = 8\text{ A}$
- Very fast switching times:
 T_F max. = 0.4 μs at $I_C = 25\text{ A}$

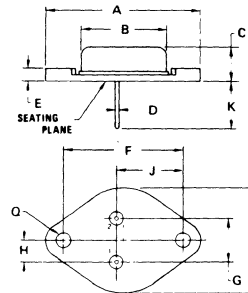
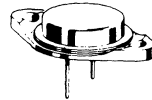
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	200	Vdc
Collector-Base Voltage	V_{CBO}	250	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5\text{ V}$)	V_{CEX}	250	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	240	Vdc
Collector-Current – continuous	I_C	40	Adc
– peak ($p_w \leq 10\text{ ms}$)	I_{CM}	50	Apk
Base-Current continuous	I_B	8	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ\text{C/W}$

40 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
200 VOLTS
250 WATTS

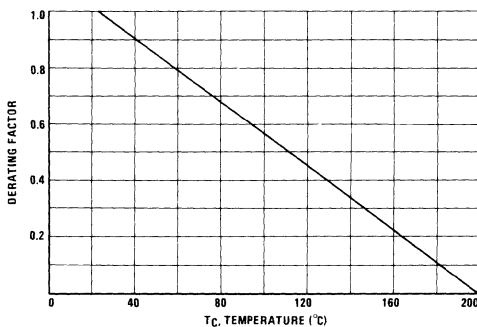


STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.90	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
 MODIFIED TO 3

FIGURE 1 – POWER DERATING



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 250\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 250\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 160\text{ V}$)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 20\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	12 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 12\text{ A}$, $V_{CE} = 2\text{ V}$) ($I_C = 25\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 1.2\text{ A}$) ($I_C = 25\text{ A}$, $I_B = 3\text{ A}$)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 25\text{ A}$, $I_B = 3\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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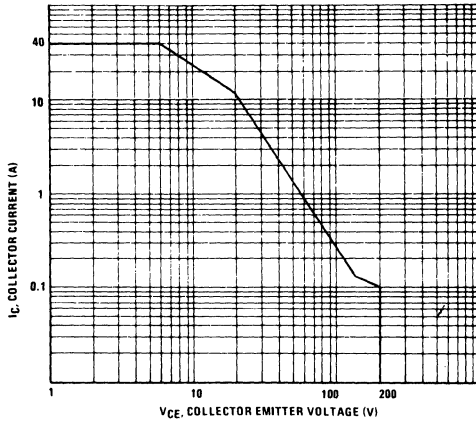
SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 25\text{ A}$, $I_{B1} = I_{B2} = 3\text{ A}$, ($V_{CC} = 100\text{ V}$, $R_C = 4\ \Omega$)	t_{on}	1.0	μs
Storage Time		t_s	1.8	
Fall Time		t_f	0.4	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

3

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC-VCE limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of figure 2 is based on $T_C = 25^\circ C$; $T_J(pk)$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

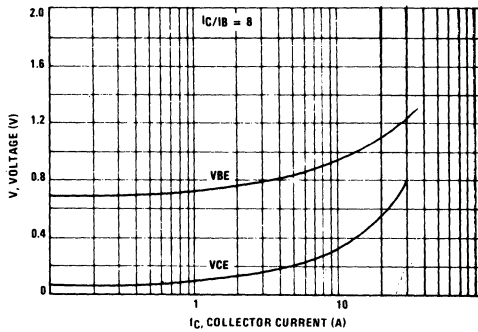


FIGURE 4 – DC CURRENT GAIN

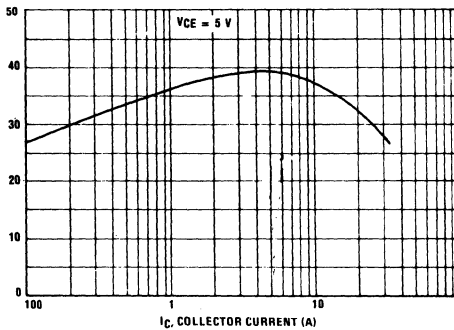


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

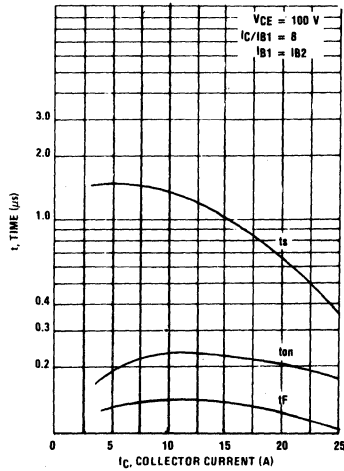
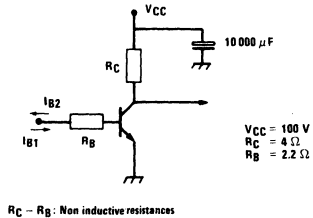


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



SWITCHMODE^A SERIES
NPN SILICON POWER TRANSISTOR

... designed for high speed, high current, high power and low cost applications.

- High DC current gain: HFE min. = 15 at $I_C = 20$ A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$ max. = 1.0 V at $I_C = 20$ A
 = 1.8 V at $I_C = 40$ A
- Very fast switching times:
 T_F max. = 0.2 μ s at $I_C = 40$ A

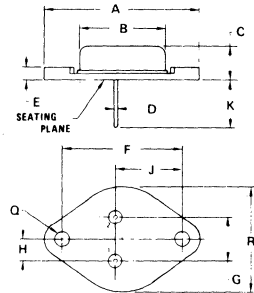
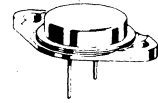
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	160	Vdc
Collector-Base Voltage	V_{CBO}	220	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	220	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	200	Vdc
Collector-Current — continuous	I_C	40	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	50	Apk
Base-Current continuous	I_B	10	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ\text{C/W}$

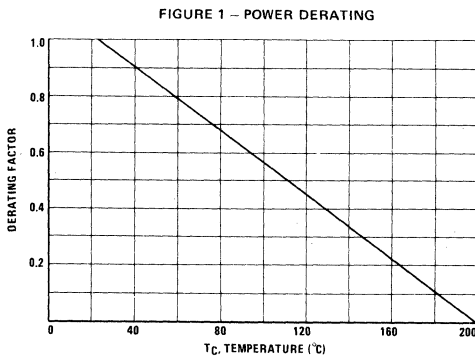
40 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
160 VOLTS
250 WATTS



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.560
B	18.30	21.06	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.05	0.151	0.161
R	24.89	26.67	0.980	1.060

CASE 197-01
 MODIFIED TO 3



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	160		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 220\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 220\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 130\text{ V}$)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 25\text{ V}$, $t = 0.5\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 0.5\text{ s}$)	$I_{S/b}$	10 0.3		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 20\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 40\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 10	60	
Collector-Emitter Saturation Voltage ($I_C = 20\text{ A}$, $I_B = 2\text{ A}$) ($I_C = 40\text{ A}$, $I_B = 5\text{ A}$)	$V_{CE(sat)}$		1.0 1.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 40\text{ A}$, $I_B = 5\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 40\text{ A}$, $I_{B1} = I_{B2} = 5\text{ A}$, ($V_{CC} = 30\text{ V}$, $R_C = 0.75\ \Omega$)	t_{on}		1.2	μs
Storage Time		t_s		1.0	
Fall Time		t_f		0.2	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

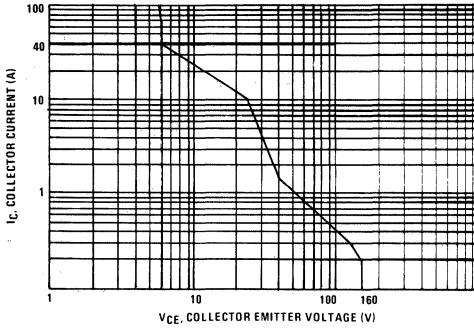


FIGURE 3 – "ON" VOLTAGES

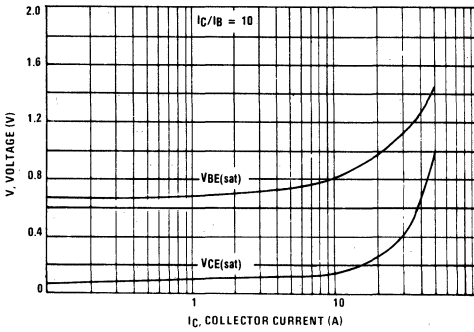
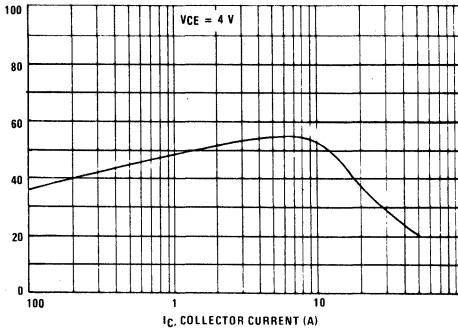


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$, $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

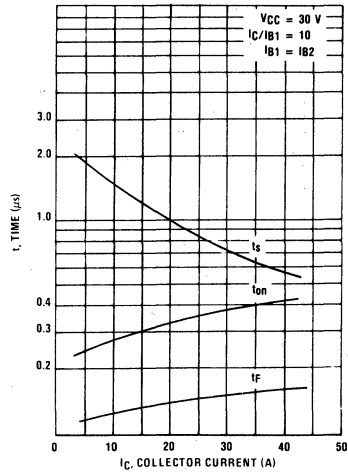
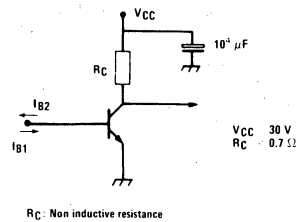


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



SWITCHMODE^A SERIES
NPN SILICON POWER TRANSISTOR

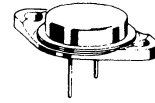
... designed for high current, high speed, high power applications.

- High DC current gain: HFE min. = 20 at $I_C = 10$ A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$ max. = 1.0 V at $I_C = 10$ A
- Very fast switching times:
 T_F max. = 0.35 μ s at $I_C = 20$ A

40 AMPERES

NPN SILICON
POWER
METAL TRANSISTOR

250 VOLTS
250 WATTS



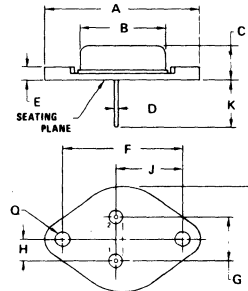
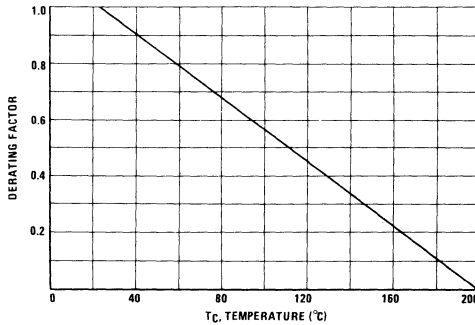
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	125	Vdc
Collector-Base Voltage	V_{CBO}	300	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	300	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	290	Vdc
Collector-Current — continuous	I_C	40	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	50	Apk
Base-Current continuous	I_B	8	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ\text{C/W}$

FIGURE 1 — POWER DERATING



STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	15.30	21.06	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.80	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 200\text{ V}$)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 20\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	12 0.15		Arc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 10\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 20\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	20 10	60	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 1\text{ A}$) ($I_C = 20\text{ A}$, $I_B = 2.5\text{ A}$)	$V_{CE(sat)}$		1.0 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 40\text{ A}$, $I_B = 4\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 20\text{ A}$, $I_{B1} = I_{B2} = 2.5\text{ A}$, ($V_{CC} = 100\text{ V}$, $R_C = 5\ \Omega$)	t_{on}	0.8	μs
Storage Time		t_s	1.1	
Fall Time		t_f	0.35	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

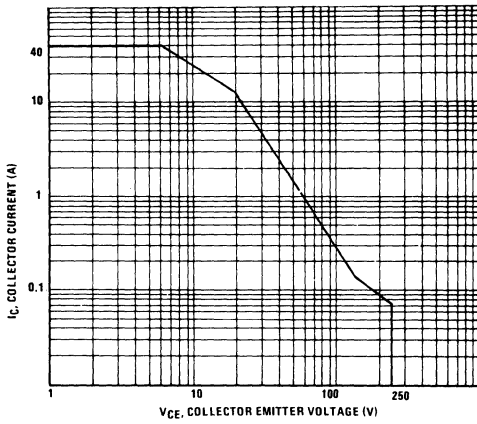


FIGURE 3 – "ON" VOLTAGES

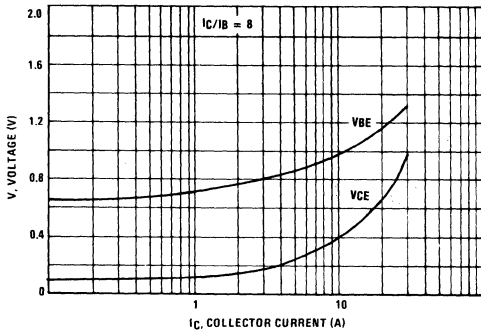
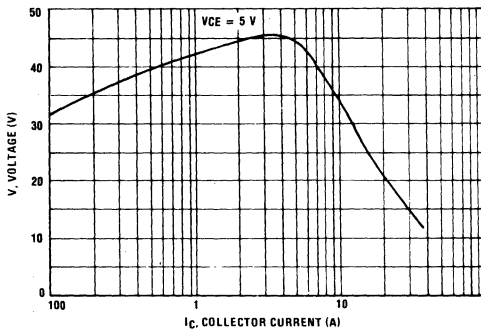


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ C$; $T_J(pk)$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

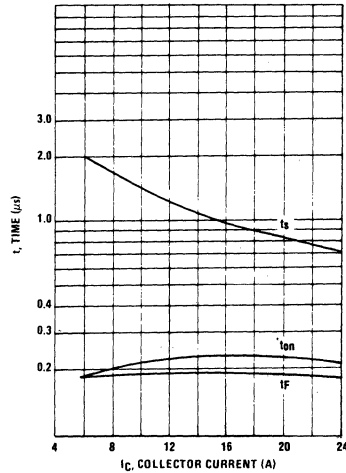
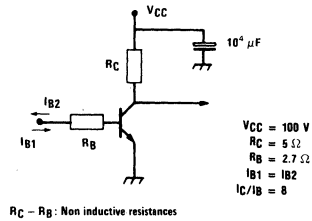


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



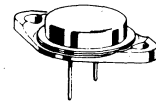
BUV23

SWITCHMODE^A SERIES
NPN SILICON POWER TRANSISTOR

... designed for high current, high speed, high power applications.

- High DC current gain: HFE min. = 15 at $I_C = 8$ A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 0.8 V at $I_C = 8$ A
- Very fast switching times:
 $T_F = 0.4 \mu s$ at $I_C = 16$ A

30 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
325 VOLTS
250 WATTS

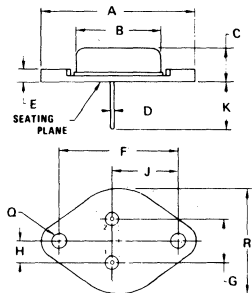


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	325	Vdc
Collector-Base Voltage	V_{CBO}	400	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	400	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	390	Vdc
Collector-Current — continuous	I_C	30	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	40	Apk
Base-Current continuous	I_B	6	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ C/W$

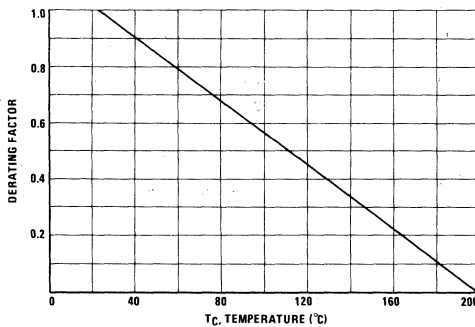


STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	-	3.43	-	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
 MODIFIED TO 3

FIGURE 1 — POWER DERATING



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	325		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 400\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 400\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 260\text{ V}$)	I_{CEO}		3.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 20\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	12 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 8\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 16\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 1.6\text{ A}$) ($I_C = 16\text{ A}$, $I_B = 3.2\text{ A}$)	$V_{CE(sat)}$		0.8 1.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 16\text{ A}$, $I_B = 3.2\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 16\text{ A}$, $I_{B1} = I_{B2} = 3.2\text{ A}$. ($V_{CC} = 100\text{ V}$, $R_C = 6.25\ \Omega$)	t_{on}	0.8	μs
Storage Time		t_s	1.8	
Fall Time		t_f	0.4	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 20\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

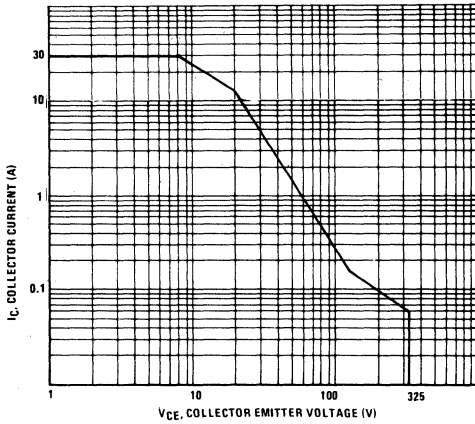


FIGURE 3 – "ON" VOLTAGES

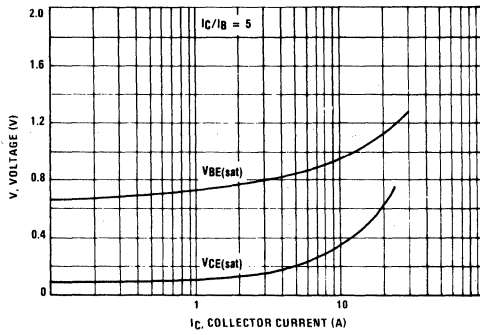
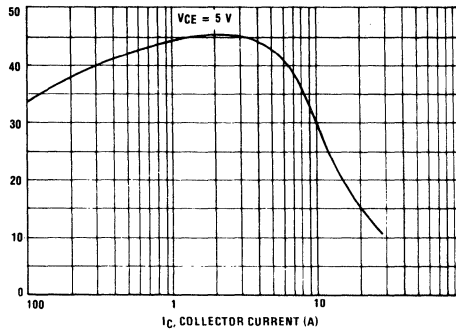


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of figure 2 is based on $T_C = 25^\circ C$; $T_J(\rho k)$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

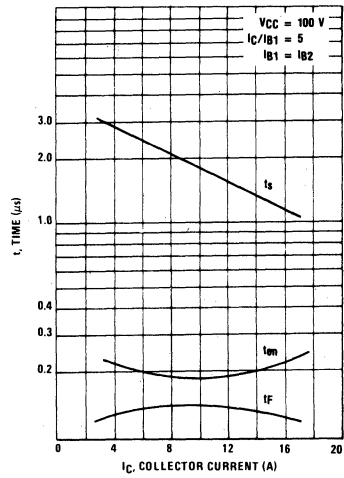
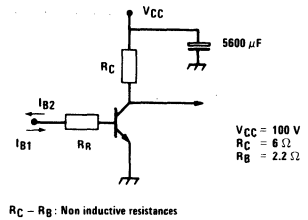


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



BUV24

SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTOR

... designed for high current, high speed, high power applications.

- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 1.0 V at $I_C = 12$ A
- Very fast switching times:
 T_F max. = 0.9 μ s at $I_C = 12$ A

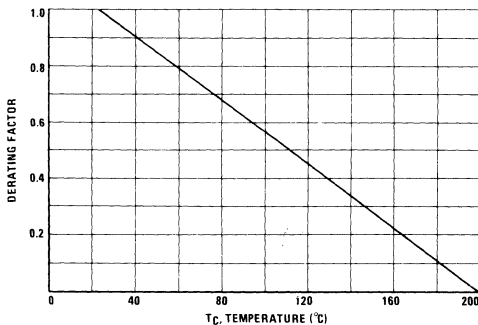
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sats)}$	400	Vdc
Collector-Base Voltage	V_{CBO}	450	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	450	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	440	Vdc
Collector-Current – continuous	I_C	20	Adc
– peak ($p_w \leq 10$ ms)	I_{CM}	30	Apk
Base-Current continuous	I_B	4	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

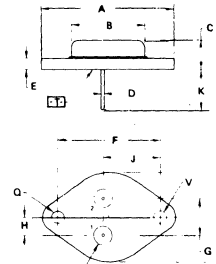
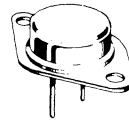
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^\circ\text{C/W}$

FIGURE 1 – POWER DERATING



20 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
400 VOLTS
250 WATTS



- NOTES
- DIMENSIONS D AND V ARE DATUMS
 - \square IS SEATING PLANE AND DATUM
 - POSITIONAL TOLERANCE FOR MOUNTING HOLE D
 - DIMENSIONS AND TOLERANCES PER ANSI Y14.5-1973
- FOR LEADS
- \blacktriangledown 13 (0.005) \odot \oplus \oplus \odot
 - \blacktriangledown 13 (0.005) \odot \oplus \oplus \odot

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.37		1.550	
B	21.08		0.830	
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	3.43		0.135	
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	26.67		1.050	
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	400		Vdc
Collector Cutoff Current at Reverse Biases: ($V_{CE} = 450\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 450\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		3.0 12.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 320\text{ V}$)	I_{CEO}		30	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 20\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	12 0.15		A
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 6\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 12\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage ($I_C = 6\text{ A}$, $I_B = 1.2\text{ A}$) ($I_C = 12\text{ A}$, $I_B = 2.4\text{ A}$)	$V_{CE(sat)}$		0.6 1.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 2.4\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 2\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 12\text{ A}$, $I_{B1} = I_{B2} = 2.4\text{ A}$, ($V_{CC} = 120\text{ V}$, $RC = 8.3\ \Omega$)	t_{on}		1.6	μs
Storage Time		t_s		3.0	
Fall Time		t_f		0.9	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

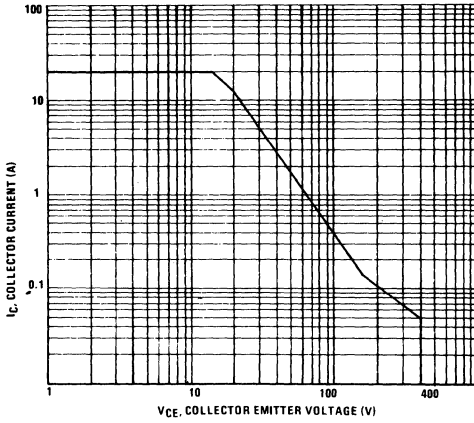


FIGURE 3 – "ON" VOLTAGES

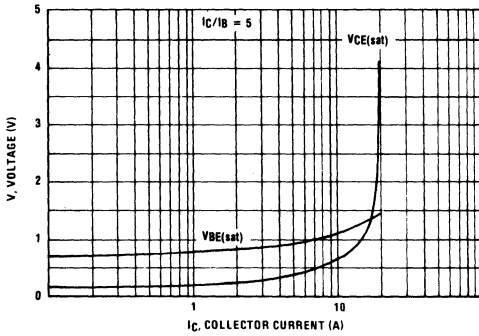
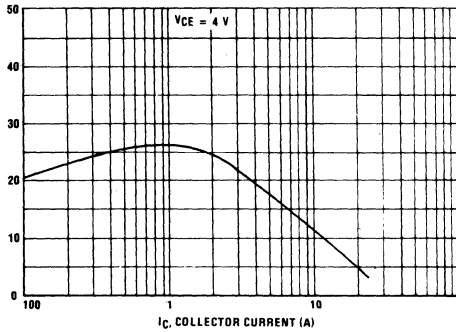


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC-VCE limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on TC = 25°C, TJ(pk) is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

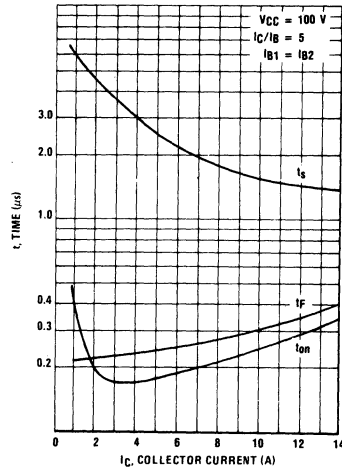
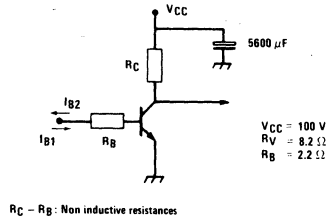


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



Designer's Data Sheet
NPN Silicon Power Transistors
Switchmode Series

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:

- Collector-Emitter Voltage — $V_{CEV} = 850$ and 1000
- Fast Turn-Off Times
 - 140 ns Inductive Fall Time — 100°C (Typ)
 - 170 & 250 ns Inductive Crossover Time — 100°C (Typ)
 - 1200 & 1800 ns Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Load
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents
- Extremely High RBSOA Capability

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-Emitter Voltage	BUW11/12	$V_{CEO(sus)}$	400	Vdc
	BUW11A/12A		450	
Collector-Emitter Voltage	BUW11/12	V_{CEV}	850	Vdc
	BUW11A/12A		1000	
Emitter-Base Voltage		V_{EB}	10	Vdc
Collector Current — Continuous	BUW11/11A	I_C	5	Adc
	BUW12/12A		8	
— Peak (1)	BUW11/11A	I_{CM}	10	
	BUW12/12A		20	
Base Current — Continuous	BUW11/11A	I_B	2	Adc
	BUW12/12A		4	
— Peak (1)	BUW11/11A	I_{BM}	4	
	BUW12/12A		8	
Total Power Dissipation @ $T_C = 25^{\circ}\text{C}$ @ $T_C = 100^{\circ}\text{C}$ Derate above $T_C = 25^{\circ}\text{C}$		P_D	125	Watts
			50	
			1	
Operating and Storage Junction Temperature Range		T_J, T_{stg}	-55 to +150	$^{\circ}\text{C}$

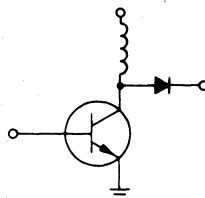
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$.1	$^{\circ}\text{C/W}$
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^{\circ}\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

BUW11,A
BUW12,A

POWER TRANSISTORS
5 and 8 AMPERES
400 and 450 VOLTS
125 WATTS



CASE 340-01
TO-218AC

BUW11,A • BUW12,A

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS(1)						
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0)	BUW11/12 BUW11A/12A	V _{CE0(sus)}	400 450	— —	— —	Vdc
Collector Cutoff Current (V _{CEV} = Rated V _{CEV} , V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated V _{CEV} , V _{BE(off)} = 1.5 Vdc, T _C = 100°C)		I _{CEV}	— —	— —	0.1 1	mAdc
Collector Cutoff Current (V _{CE} = Rated V _{CEV} , R _{BE} = 50 Ω, T _C = 100°C)		I _{CER}	—	—	1	mAdc
Emitter Cutoff Current (V _{EB} = 9 Vdc, I _C = 0)		I _{EBO}	—	—	0.1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figures 8 and 9
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figures 10 and 11

BUW11

ON CHARACTERISTICS(1)

Collector-Emitter Saturation Voltage (I _C = 1 Adc, I _B = 0.2 Adc) (I _C = 3 Adc, I _B = 0.6 Adc) (I _C = 3 Adc, I _B = 0.6 Adc, T _C = 100°C)	V _{CE(sat)}	— — —	— — —	1 1.5 2	Vdc
Base-Emitter Saturation Voltage (I _C = 3 Adc, I _B = 0.6 Adc) (I _C = 3 Adc, I _B = 0.6 Adc, T _C = 100°C)	V _{BE(sat)}	— —	— —	1.4 1.4	Vdc
DC Current Gain (I _C = 3 Adc, V _{CE} = 5 Vdc)	h _{FE}	6	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1 kHz)	C _{ob}	—	125	—	pF
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SWITCHING CHARACTERISTICS

Inductive Load (Table 1)							
Storage Time	I _C = 3 Adc, I _{B1} = 0.6 Adc, V _{BE(off)} = 5 Vdc, V _{CE(pk)} = 300 Vdc	(T _J = 100°C)	t _{sv}	—	1.2	1.5	μs
Fall Time			t _{fi}	—	0.14	0.3	
Crossover Time			t _c	—	0.25	0.5	
Resistive Load (Table 2)							
Delay Time	I _C = 3 Adc, V _{CC} = 250 Vdc, I _{B1} = 0.6 Adc, PW = 20 μs, Duty Cycle ≤ 2%	(I _{B2} = 0.6 Adc, R _{B2} = 4 Ω)	t _d	—	—	0.1	μs
Rise Time			t _r	—	—	0.8	
Storage Time			t _s	—	—	4	
Fall Time			t _f	—	—	0.8	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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BUW11A

ON CHARACTERISTICS(1)

Collector-Emitter Saturation Voltage ($I_C = 1 \text{ A dc}, I_B = 0.2 \text{ A dc}$) ($I_C = 2.5 \text{ A dc}, I_B = 0.5 \text{ A dc}$) ($I_C = 2.5 \text{ A dc}, I_B = 0.5 \text{ A dc}, T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	1 1.5 2	Vdc
Base-Emitter Saturation Voltage ($I_C = 2.5 \text{ A dc}, I_B = 0.5 \text{ A dc}$) ($I_C = 2.5 \text{ A dc}, I_B = 0.5 \text{ A dc}, T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.4 1.4	Vdc
DC Current Gain ($I_C = 2.5 \text{ A dc}, V_{CE} = 5 \text{ V dc}$)	h_{FE}	6	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10 \text{ V dc}, I_E = 0, f_{test} = 1 \text{ kHz}$)	C_{ob}	—	125	—	pF
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SWITCHING CHARACTERISTICS

Inductive Load (Table 1)							
Storage Time	$(I_C = 2.5 \text{ A dc}, I_{B1} = 0.5 \text{ A dc}, V_{BE(off)} = 5 \text{ V dc}, V_{CE(pk)} = 300 \text{ V dc})$	$(T_J = 100^\circ\text{C})$	t_{sv}	—	1.2	1.5	μs
Fall Time			t_{fi}	—	0.14	0.3	
Crossover Time			t_c	—	0.25	0.5	
Resistive Load (Table 2)							
Delay Time	$(I_C = 2.5 \text{ A dc}, V_{CC} = 250 \text{ V dc}, I_{B1} = 0.5 \text{ A dc}, PW = 20 \mu\text{s}, \text{Duty Cycle} \leq 2\%)$	$(I_{B2} = 0.5 \text{ A dc}, R_{B2} = 4 \Omega)$	t_d	—	—	0.1	μs
Rise Time			t_r	—	—	0.8	
Storage Time			t_s	—	—	4	
Fall Time			t_f	—	—	0.8	

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

BUW11,A • BUW12,A

ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BUW12					
ON CHARACTERISTICS(1)					
Collector-Emitter Saturation Voltage ($I_C = 3 \text{ Adc}, I_B = 0.6 \text{ Adc}$) ($I_C = 6 \text{ Adc}, I_B = 1.2 \text{ Adc}$) ($I_C = 6 \text{ Adc}, I_B = 1.2 \text{ Adc}, T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1 1.5 2	Vdc
Base-Emitter Saturation Voltage ($I_C = 6 \text{ Adc}, I_B = 1.2 \text{ Adc}$) ($I_C = 6 \text{ Adc}, I_B = 1.2 \text{ Adc}, T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain ($I_C = 6 \text{ Adc}, V_{CE} = 5 \text{ Vdc}$)	h_{FE}	6	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f_{test} = 1 \text{ kHz}$)	C_{ob}	—	125	—	pF
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SWITCHING CHARACTERISTICS

Inductive Load (Table 1)							
Storage Time	$I_C = 6 \text{ Adc},$ $I_{B1} = 1.2 \text{ Adc},$ $V_{BE(off)} = 5 \text{ Vdc},$ $V_{CE(pk)} = 300 \text{ Vdc}$	$(T_J = 100^\circ\text{C})$	t_{sv}	—	1.8	2.3	μs
Fall Time			t_{fi}	—	0.14	0.3	
Crossover Time			t_c	—	0.17	0.5	
Resistive Load (Table 2)							
Delay Time	$I_C = 6 \text{ Adc},$ $V_{CC} = 250 \text{ Vdc},$ $I_{B1} = 1.2 \text{ Adc},$ $PW = 20 \mu\text{s},$ Duty Cycle $\leq 2\%$	$(I_{B2} = 1.2 \text{ Adc},$ $R_{B2} = 4 \Omega)$	t_d	—	—	0.1	μs
Rise Time			t_r	—	—	0.8	
Storage Time			t_s	—	—	4	
Fall Time			t_f	—	—	0.8	

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

BUW12A

ON CHARACTERISTICS(1)

Collector-Emitter Saturation Voltage ($I_C = 3 \text{ Adc}, I_B = 0.6 \text{ Adc}$) ($I_C = 5 \text{ Adc}, I_B = 1 \text{ Adc}$) ($I_C = 5 \text{ Adc}, I_B = 1 \text{ Adc}, T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1 1.5 2	Vdc
Base-Emitter Saturation Voltage ($I_C = 5 \text{ Adc}, I_B = 1 \text{ Adc}$) ($I_C = 5 \text{ Adc}, I_B = 1 \text{ Adc}, T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain ($I_C = 5 \text{ Adc}, V_{CE} = 5 \text{ Vdc}$)	h_{FE}	6	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f_{test} = 1 \text{ kHz}$)	C_{ob}	—	125	—	pF
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SWITCHING CHARACTERISTICS

Inductive Load (Table 1)							
Storage Time	$I_C = 5 \text{ Adc},$ $I_{B1} = 1 \text{ Adc},$ $V_{BE(off)} = 5 \text{ Vdc},$ $V_{CE(pk)} = 300 \text{ Vdc}$	$(T_J = 100^\circ\text{C})$	t_{sv}	—	1.8	2.3	μs
Fall Time			t_{fi}	—	0.14	0.3	
Crossover Time			t_c	—	0.17	0.5	
Resistive Load (Table 2)							
Delay Time	$I_C = 5 \text{ Adc},$ $V_{CC} = 250 \text{ Vdc},$ $I_{B1} = 1 \text{ Adc},$ $PW = 20 \mu\text{s},$ Duty Cycle $\leq 2\%$	$(I_{B2} = 1 \text{ Adc},$ $R_{B2} = 4 \Omega)$	t_d	—	—	0.1	μs
Rise Time			t_r	—	—	0.8	
Storage Time			t_s	—	—	4	
Fall Time			t_f	—	—	0.8	

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

TYPICAL STATIC CHARACTERISTICS

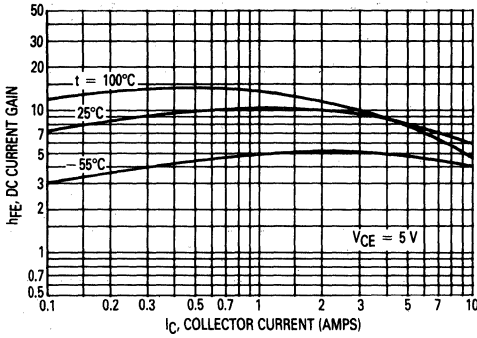


Figure 1. Typical DC Current Gain

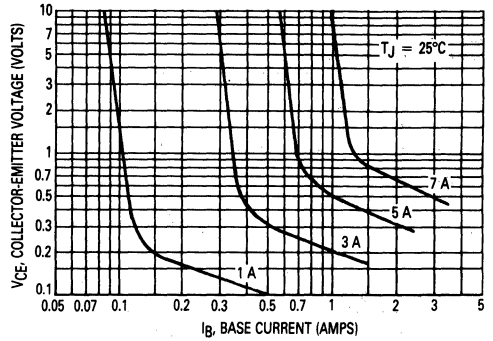


Figure 2. Typical Collector Saturation Region

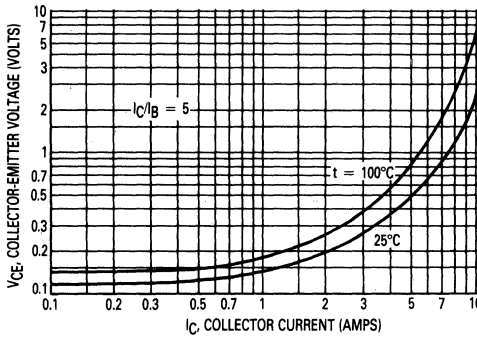


Figure 3. Typical Collector Saturation Region

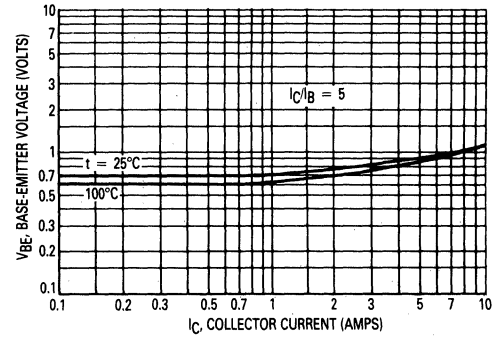


Figure 4. Typical Base-Emitter Voltage

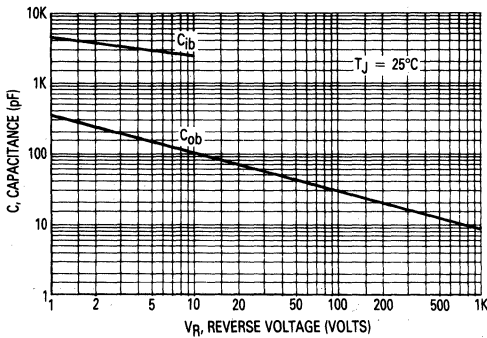


Figure 5. Typical Capacitance

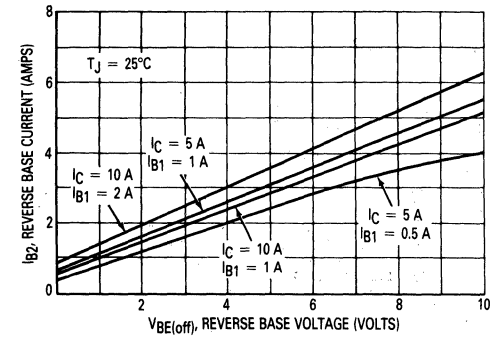


Figure 6. Peak Reverse Base Current

3

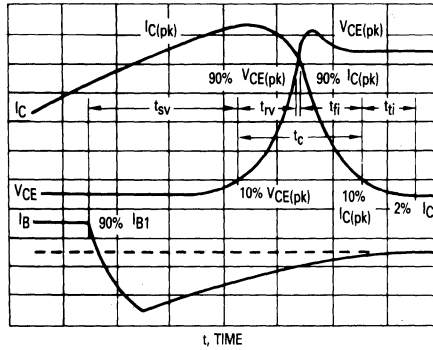
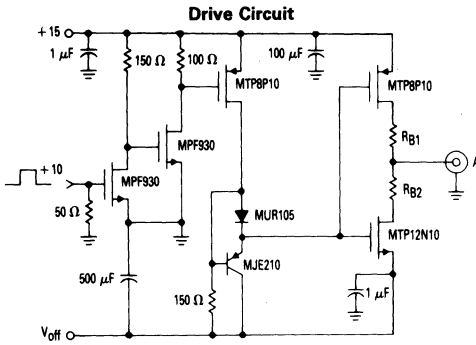


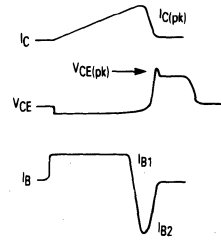
Figure 7. Inductive Switching Measurements

Table 1. Inductive Load Switching



V(BR)ICE(sus)
 $L = 10 \text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20 \text{ Volts}$
 $I_{C(pk)} = 100 \text{ mA}$
 $I_{B} = 0$

Inductive Switching
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}
 $I_{B} = 0$



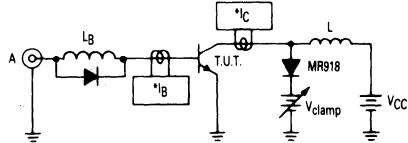
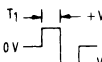
RBSOA
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}
 $I_{B} = 0$

*Tektronix AM503
 P6302 or Equivalent

Scope — Tektronix
 7403 or Equivalent

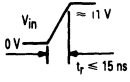
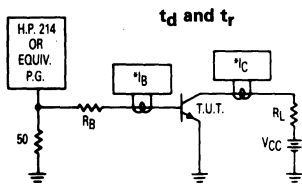
$$T_1 \approx \frac{L_{\text{coil}} (I_{C(pk)})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

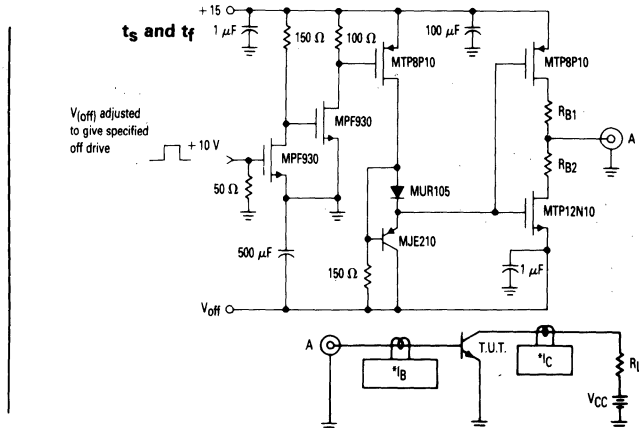


Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

Table 2. Resistive Load Switching



*Tektronix AM503
 P6302 or Equivalent



$V_{(off)}$ adjusted to give specified off drive

MAXIMUM FORWARD BIAS SAFE OPERATING AREA

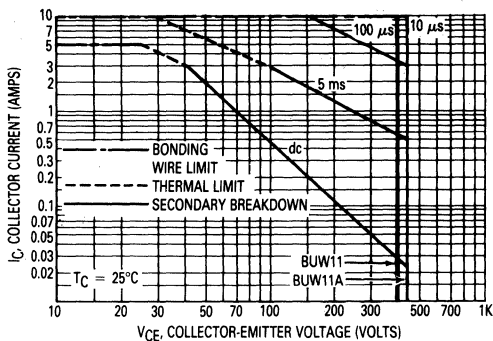


Figure 8. BUW11,A

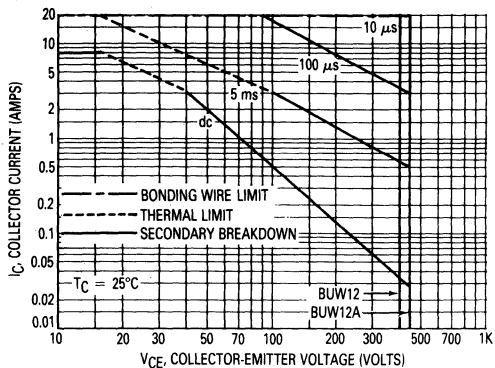


Figure 9. BUW12,A

MAXIMUM REVERSE BIAS SAFE OPERATING AREA

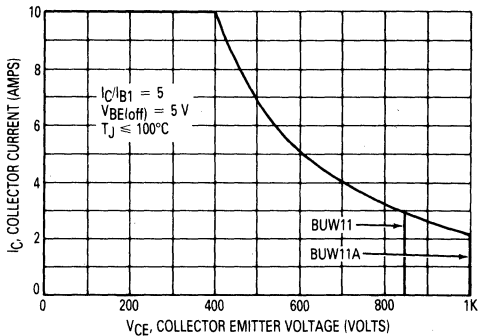


Figure 10. BUW11,A

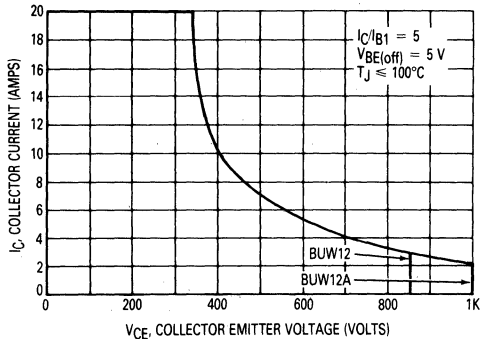


Figure 11. BUW12,A

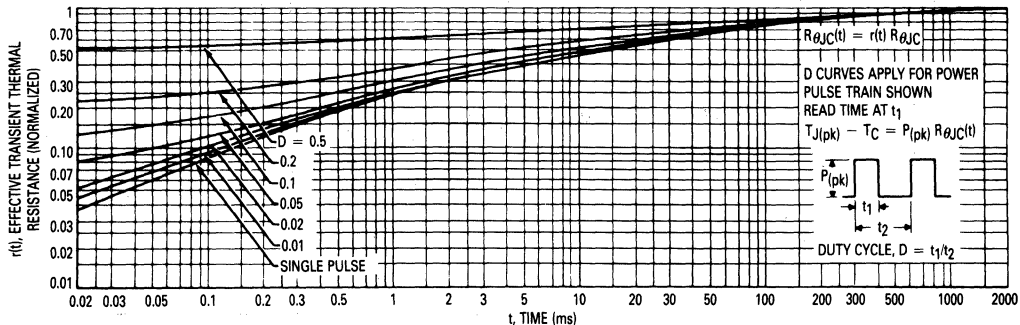


Figure 12. Thermal Response

3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 8 and 9 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 8 and 9 may be found at any case temperature by using the appropriate curve on Figure 13.

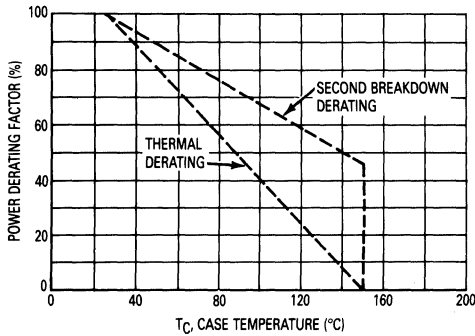


Figure 13. Power Derating

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figures 10 and 11 gives the RBSOA characteristics.

OUTLINE DIMENSIONS

STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.206	0.225
H	2.41	3.20	0.096	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

**CASE 340-01
TO-218AC**

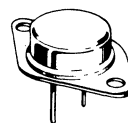
SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTOR

... designed for high speed, high voltage, high power applications.

- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 1.5 V at $I_C = 8$ A
- Very fast switching times:
 T_F max. = 0.8 μ s at $I_C = 8$ A

15 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR

325 VOLTS
150 WATTS

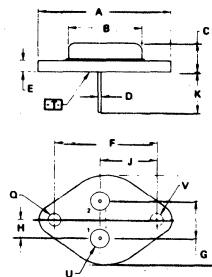


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	325	Vdc
Collector-Base Voltage	V_{CBO}	400	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5$ V)	V_{CEX}	400	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	390	Vdc
Collector-Current – continuous	I_C	15	Adc
– peak ($p_w \leq 10$ ms)	I_{CM}	20	Apk
Base-Current continuous	I_B	3	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C}/\text{W}$



NOTES

- 1 DIMENSIONS Q AND V ARE DATUMS
- 2 [] IS SEATING PLANE AND DATUM
- 3 POSITIONAL TOLERANCE FOR MOUNTING HOLE D

◆ $\frac{13}{10.005}$ (T) (V) (Q)

FOR LEADS

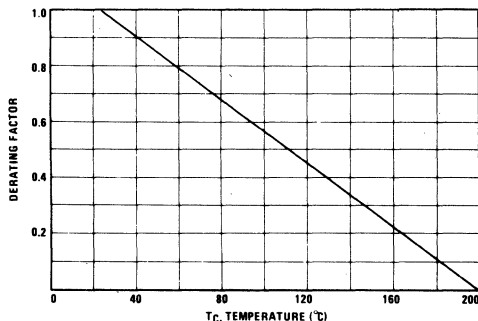
◆ $\frac{13}{10.005}$ (T) (V) (Q)

- 4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	0.35	7.62	0.250	0.300
D	0.97	1.08	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.48 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3

FIGURE 1 – POWER DERATING



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	325		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 400\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 400\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.5 6.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 260\text{ V}$)	I_{CEO}		1.5	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 140\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	5 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 4\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 8\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage ($I_C = 4\text{ A}$, $I_B = 0.8\text{ A}$) ($I_C = 8\text{ A}$, $I_B = 1.6\text{ A}$)	$V_{CE(sat)}$		0.8 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 1.6\text{ A}$)	$V_{BE(sat)}$		1.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 8\text{ A}$, $I_{B1} = I_{B2} = 1.6\text{ A}$, ($V_{CC} = 150\text{ V}$, $R_C = 18.7\ \Omega$)	t_{on}		1.2	μs
Storage Time		t_s		2.5	
Fall Time		t_f		0.8	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

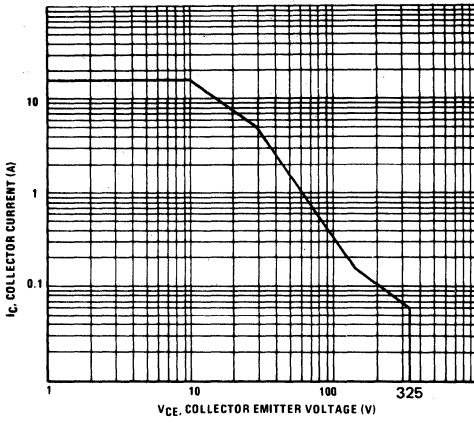


FIGURE 3 – "ON" VOLTAGES

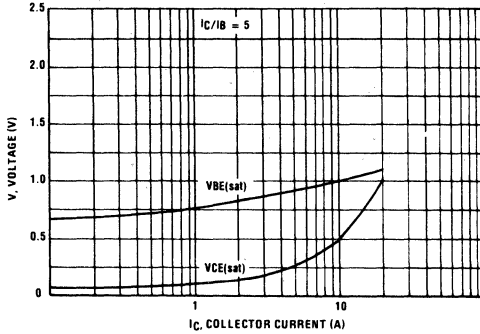
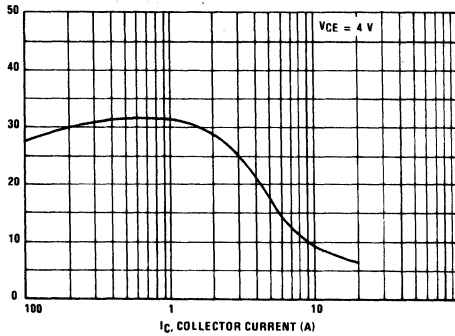


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

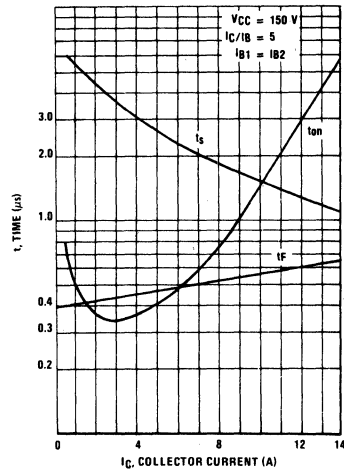
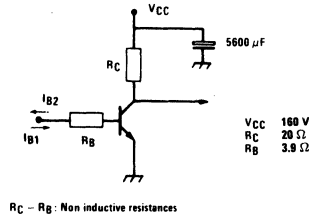


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

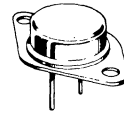
NPN SILICON POWER METAL TRANSISTOR

... designed for high speed, high current, high power application.

- High current gain – bandwidth product F_t min. = 8.0 MHz
 - High DC current gain H_{FE} min. 15 @ $I_C = 12$ A.
- Very fast switching times
 t_F max. = 0.25 μ s @ $I_C = 20$ A

**NPN SILICON
 POWER
 METAL TRANSISTOR**

30 AMPERES



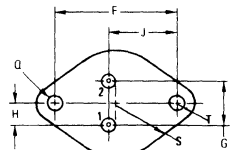
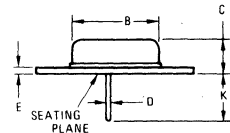
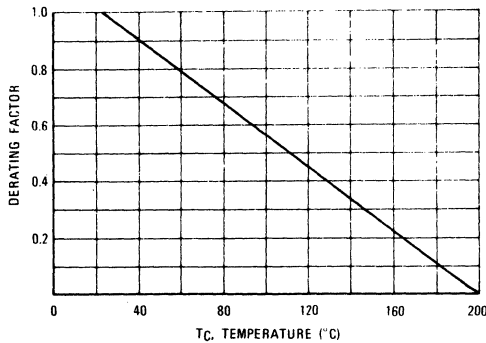
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	90	Vdc
Collector-Base Voltage	V_{CB0}	120	Vdc
Emitter-Base Voltage	V_{EB0}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -1.5$ V)	V_{CEX}	120	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\Omega$)	V_{CER}	110	Vdc
Collector-Current – continuous	I_C	30	Adc
– peak ($p_w < 10$ ms)	I_{CM}	40	Apk
Base-Current continuous	I_B	6	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	$^\circ\text{C/W}$

FIGURE 1 – POWER DERATING



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE-COLLECTOR

STYLE 2:
 PIN 1. BASE
 2. COLLECTOR
 CASE-EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
 (TO-3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	90		Vdc
Collector-Emitter Cutoff Current at Reverse Bias Voltage ($V_{CE} = 120\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 120\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)			1 5	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 70\text{ V}$)	I_{CEO}		1	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1	mAdc

SECOND BREAKDOWN.

Second Breakdown Collector Current with base forward biased ($V_{CE} = 45\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	1 4		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 12\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 20\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 1.2\text{ A}$) ($I_C = 20\text{ A}$, $I_B = 2.5\text{ A}$)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 20\text{ A}$, $I_B = 2.5\text{ A}$)	$V_{BE(sat)}$		2.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8		MHz
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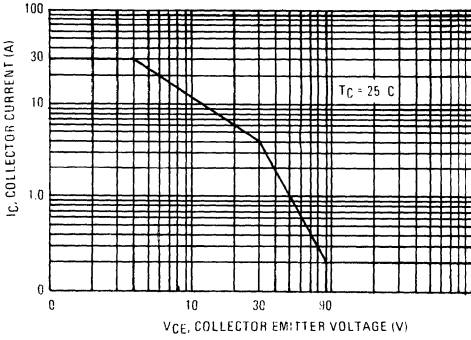
SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 20\text{ A}$, $I_{B1} = I_{B2} = 2.5\text{ A}$, $V_{CE} = 30\text{ V}$, $RC = 1.5\ \Omega$	t_{on}	1.2	μs
Storage Time		t_s	1.0	
Fall Time		t_f	0.25	

¹ Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

3

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC-VCE limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of figure 2 is based on TC = 25 °C; TJ(pk) is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 3 – "ON" VOLTAGES

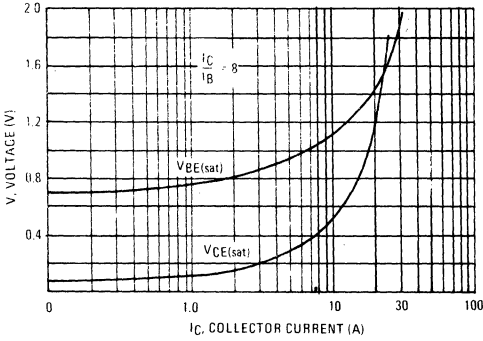


FIGURE 4 – DC CURRENT GAIN

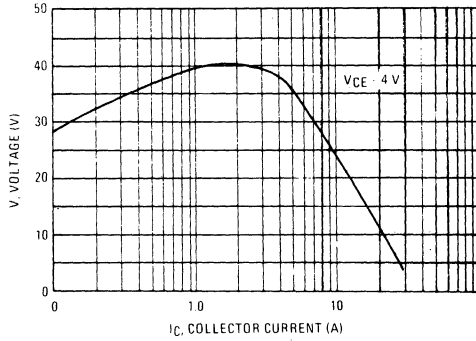


FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

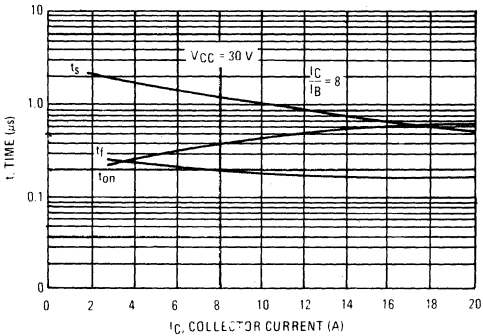
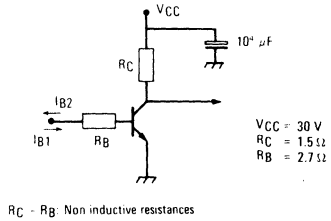


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



SWITCHMODE^A SERIES
NPN SILICON POWER TRANSISTOR

... designed for high speed, high current, high power applications.

- High D.C. current gain:
HFE min.: 15 at $I_C = 10\text{ A}$
- Very fast switching times:
 T_F max. = $0.25\ \mu\text{s}$ at $I_C = 15\text{ A}$

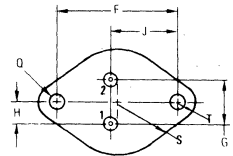
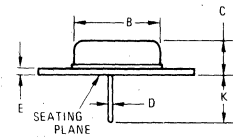
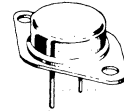
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	125	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5\text{ V}$)	V_{CEX}	160	Vdc
Collector-Emitter Voltage ($R_{BE} = 100\ \Omega$)	V_{CER}	150	Vdc
Collector-Current – continuous	I_C	20	A dc
– peak ($p_w \leq 10\text{ ms}$)	I_{CM}	28	A pk
Base-Current continuous	I_B	4	A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	$^\circ\text{C/W}$

20 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
125 VOLTS
120 WATTS



STYLE 1
 PIN 1 BASE
 2 EMITTER
 CASE-COLLECTOR

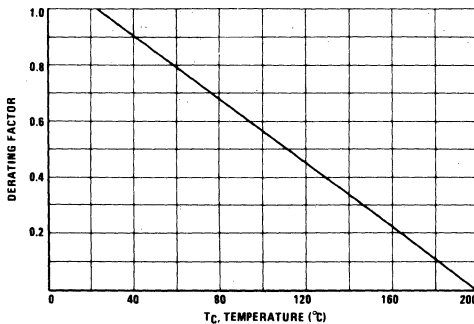
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	5.43	—	0.213
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
 (TO-3)

3

FIGURE 1 – POWER DERATING



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CEO(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 160\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 160\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 100\text{ V}$)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 50\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	4.0 1.0		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 10\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 15\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 1\text{ A}$) ($I_C = 15\text{ A}$, $I_B = 1.88\text{ A}$)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 15\text{ A}$, $I_B = 1.88\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
--	-------	-----	--	-----

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 15\text{ A}$, $I_{B1} = I_{B2} = 1.88\text{ A}$, ($V_{CC} = 30\text{ V}$, $R_C = 2\ \Omega$)	t_{on}	1.2	μs
Storage Time		t_s	1.0	
Fall Time		t_f	0.25	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

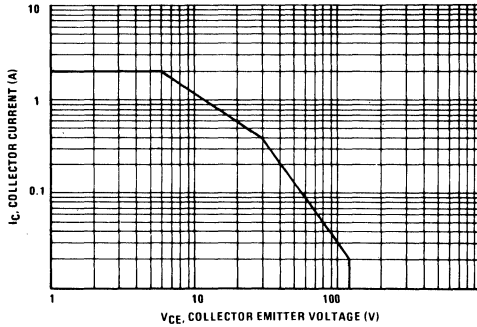


FIGURE 3 – "ON" VOLTAGES

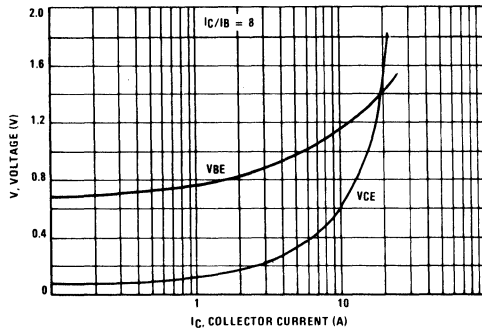
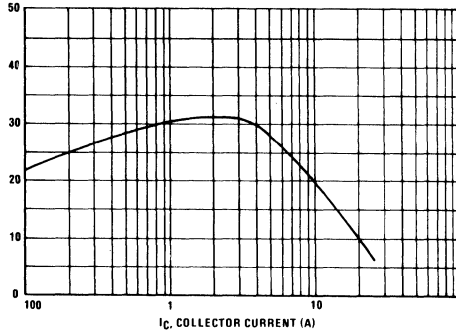


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC-VCE limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on TC = 25°C; TJ(pk) is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

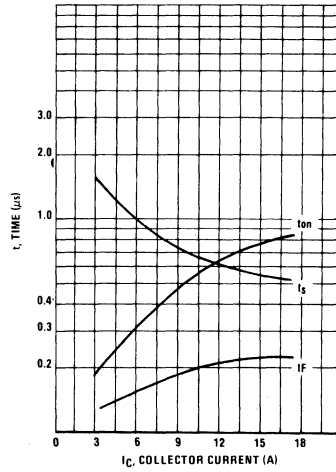
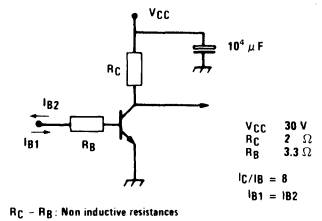


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



BUX41

SWITCHMODE^A SERIES
NPN SILICON POWER TRANSISTOR

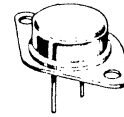
... designed for high speed, high current, high power applications.

- Very fast switching times:
 T_F max. = 0.4 μ s at $I_C = 8$ A

15 AMPERES

NPN SILICON
POWER
METAL TRANSISTOR

200 VOLTS
120 WATTS

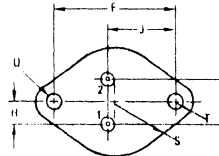
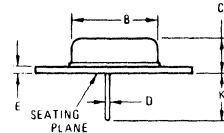


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	200	Vdc
Collector-Base Voltage	V_{CBO}	250	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5$ V)	V_{CEX}	250	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	240	Vdc
Collector-Current – continuous	I_C	15	A dc
– peak ($p_w \leq 10$ ms)	I_{CM}	20	A pk
Base-Current continuous	I_B	3	A dc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	$^\circ C/W$



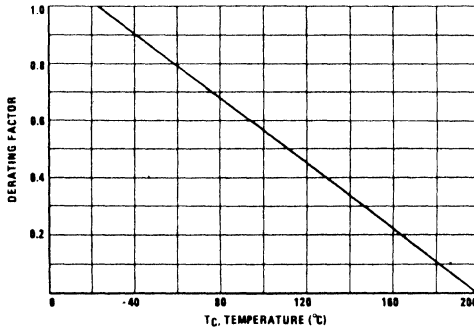
STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR
 STYLE 2:
 PIN 1. BASE
 2. COLLECTOR
 CASE-EMITTER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	-	22.23	-	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	-	3.43	-	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.206	0.225
J	16.64	17.15	0.655	0.675
K	7.92	-	0.312	-
Q	3.84	4.09	0.151	0.161
S	-	13.34	-	0.525
T	-	4.78	-	0.188

All JEDEC dimensions and notes apply

CASE 1-03
 (TO 3)

FIGURE 1 – POWER DERATING



BUX41

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 250\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 250\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 160\text{ V}$)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 135\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	4.0 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 5\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 8\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage ($I_C = 5\text{ A}$, $I_B = 0.5\text{ A}$) ($I_C = 8\text{ A}$, $I_B = 1\text{ A}$)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 1\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 8\text{ A}$, $I_{B1} = I_{B2} = 1\text{ A}$, ($V_{CC} = 150\text{ V}$, $R_C = 18.75\ \Omega$)	t_{on}	0.6	μs
Storage Time		t_s	1.5	
Fall Time		t_f	0.4	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

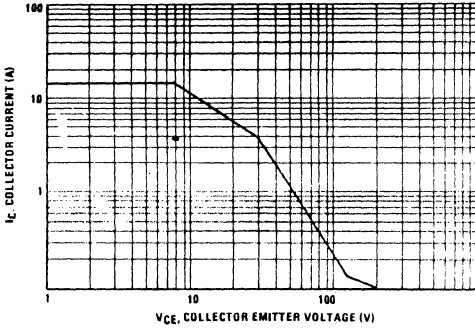


FIGURE 3 – "ON" VOLTAGES

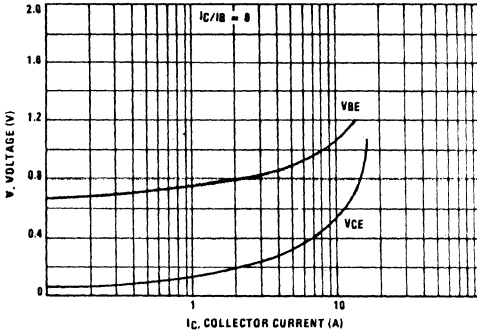
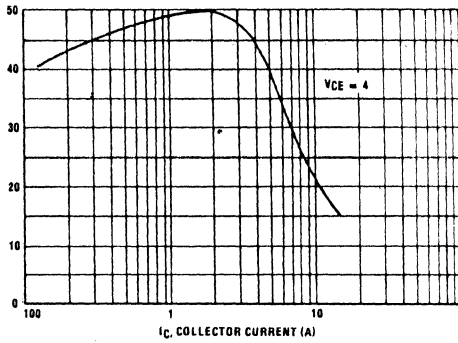


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of figure 2 is based on $T_C = 25^\circ C$; $T_J(pk)$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

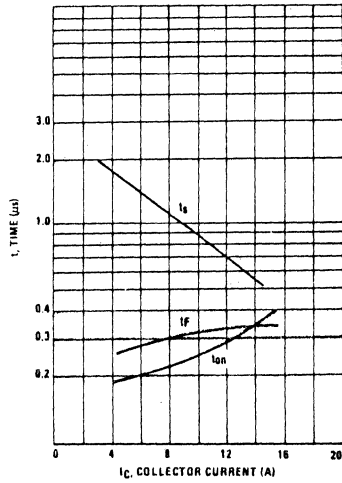
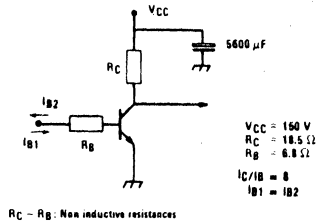


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTOR

... designed for high speed, high current, high power applications.

- High DC current gain:
HFE min. = 15 at $I_C = 8$ A
- Very fast switching times:
 T_F max. = 0.25 μ s at $I_C = 12$ A

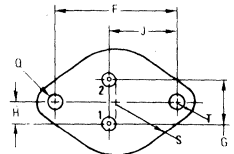
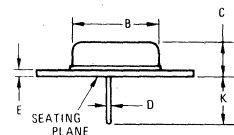
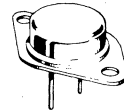
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	160	Vdc
Collector-Base Voltage	V_{CBO}	220	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5$ V)	V_{CEX}	220	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	200	Vdc
Collector-Current — continuous	I_C	18	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	25	Apk
Base-Current continuous	I_B	-3.6	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	$^\circ C/W$

18 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
160 VOLTS
120 WATTS



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE-COLLECTOR
 STYLE 2:
 PIN 1. BASE
 2. COLLECTOR
 CASE-EMITTER

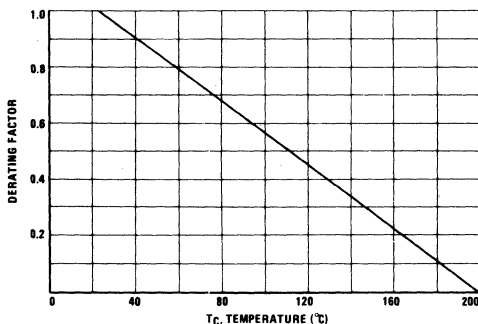
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.54	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

All JEDEC dimensions and notes apply

CASE 1-03
 (TO-3)

3

FIGURE 1 — POWER DERATING



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
----------------	--------	------	------	------

OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	160		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 220\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 220\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 130\text{ V}$)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 100\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	4 0.27		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 8\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 12\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage ($I_C = 8\text{ A}$, $I_B = 0.8\text{ A}$) ($I_C = 12\text{ A}$, $I_B = 1.5\text{ A}$)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 12\text{ A}$, $I_B = 1.5\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
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SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 12\text{ A}$, $I_{B1} = I_{B2} = 1.5\text{ A}$, ($V_{CC} = 30\text{ V}$, $R_C = 2.5\ \Omega$)	t_{on}		1.2	μs
Storage Time		t_s		1.2	
Fall Time		t_f		0.25	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA

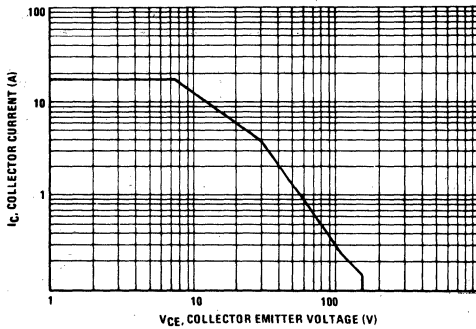


FIGURE 3 – "ON" VOLTAGES

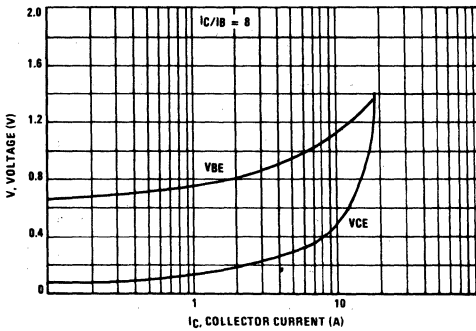
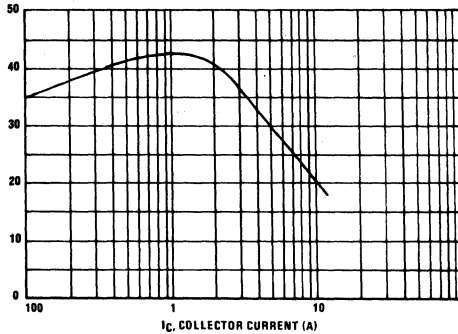


FIGURE 4 – DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ C$; $T_J(pk)$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 – RESISTIVE SWITCHING PERFORMANCE

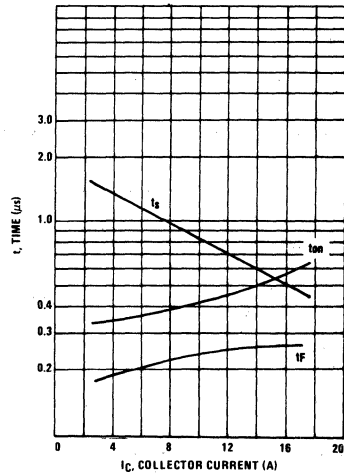
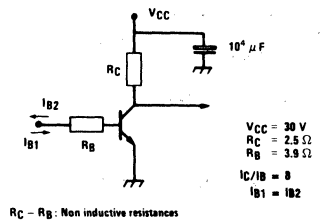


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT



3

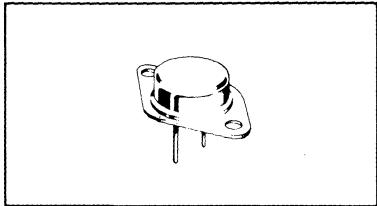
BUX42

SWITCHMODE^A SERIES
NPN SILICON POWER TRANSISTOR

... designed for high speed, high voltage, high power applications.

- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 1.2 V at $I_C = 4$ A
- Very fast switching times:
 T_F max. = 0.4 μ s at $I_C = 6$ A

12 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
250 VOLTS
120 WATTS

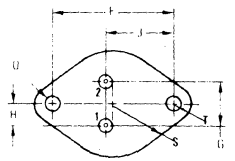
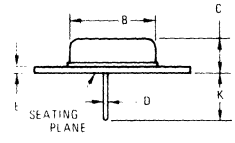
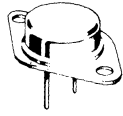


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector-Base Voltage	V_{CB0}	300	Vdc
Emitter-Base Voltage	V_{EB0}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5$ V)	V_{CEX}	300	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	290	Vdc
Collector-Current – continuous	I_C	12	Adc
– peak ($p_w \leq 10$ ms)	I_{CM}	15	Apk
Base-Current continuous	I_B	2.4	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

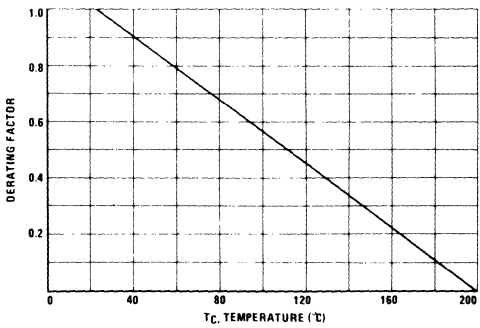
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	$^\circ C/W$



STYLE 1
 PIN 1 BASE
 2 EMITTER
 CASE COLLECTOR

FIGURE 1 – POWER DERATING



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	22	23	-	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	-	3.43	-	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.42	-	0.312	-
Q	3.84	4.09	0.151	0.161
S	-	13.34	-	0.525
T	-	4.78	-	0.188

All JEDEC dimensions and metrics apply

CASE 1 03
 (TO 3)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CE(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 200\text{ V}$)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 135\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	4.0 0.15		Adc
--	-----------	-------------	--	-----

ON CHARACTERISTICS¹

DC Current Gain ($I_C = 4\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 6\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	45	
Collector-Emitter Saturation Voltage ($I_C = 4\text{ A}$, $I_B = 0.4\text{ A}$) ($I_C = 6\text{ A}$, $I_B = 0.75\text{ A}$)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 6\text{ A}$, $I_B = 0.75\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
--	-------	-----	--	-----

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 6\text{ A}$, $I_{B1} = I_{B2} = 0.75\text{ A}$, ($V_{CC} = 150\text{ V}$, $R_C = 25\ \Omega$)	t_{on}	0.6	μs
Storage Time		t_s	2.0	
Fall Time		t_f	0.4	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 -- ACTIVE REGION SAFE OPERATING AREA

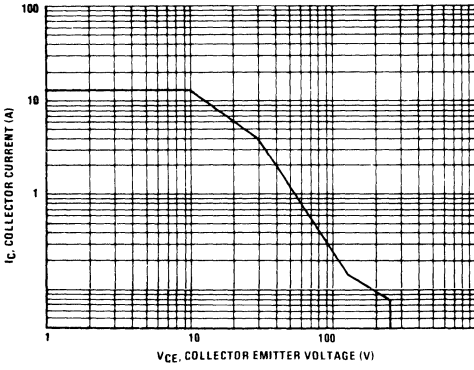


FIGURE 3 -- "ON" VOLTAGES

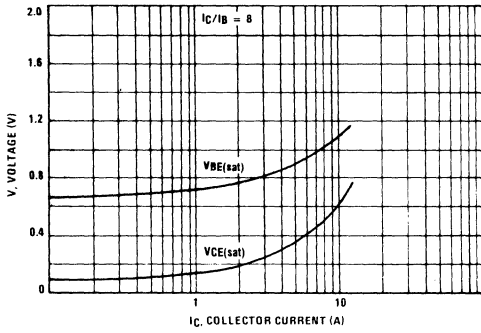
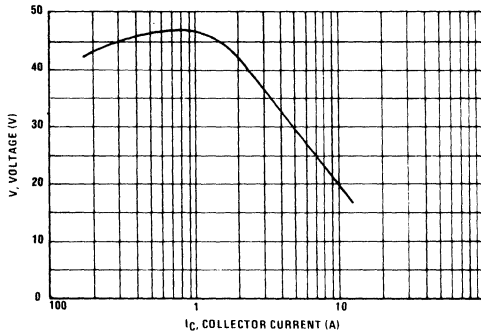


FIGURE 4 -- DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ C$; $T_J(pk)$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 -- RESISTIVE SWITCHING PERFORMANCE

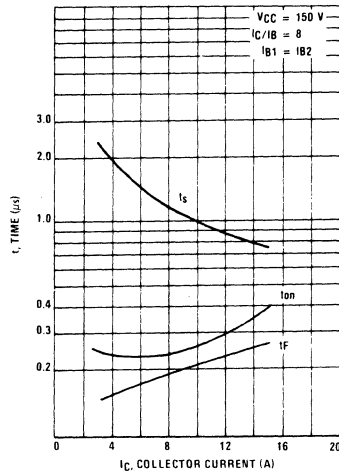
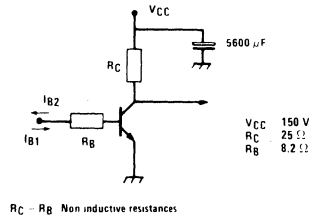


FIGURE 6 -- SWITCHING TIMES TEST CIRCUIT

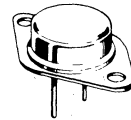


SWITCHMODE[▲] SERIES
NPN SILICON POWER TRANSISTOR

... designed for high speed, high voltage, high power applications.

- $V_{CE(sat)}$ max. = 1.6 V at $I_C = 6$ A
- Very fast switching times:
 T_F max. = 0.90 μ s at $I_C = 5$ A

10 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
325 VOLTS
120 WATTS

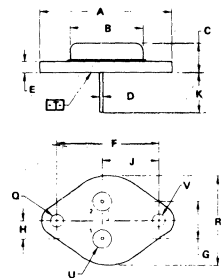


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	325	Vdc
Collector-Base Voltage	V_{CBO}	400	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector-Emitter Voltage ($V_{BE} = -2.5$ V)	V_{CEX}	400	Vdc
Collector-Emitter Voltage ($R_{BE} = 100 \Omega$)	V_{CER}	360	Vdc
Collector-Current — continuous	I_C	10	Adc
— peak ($p_w \leq 10$ ms)	I_{CM}	12	Apk
Base-Current continuous	I_B	2	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	$^\circ C$

THERMAL CHARACTERISTICS

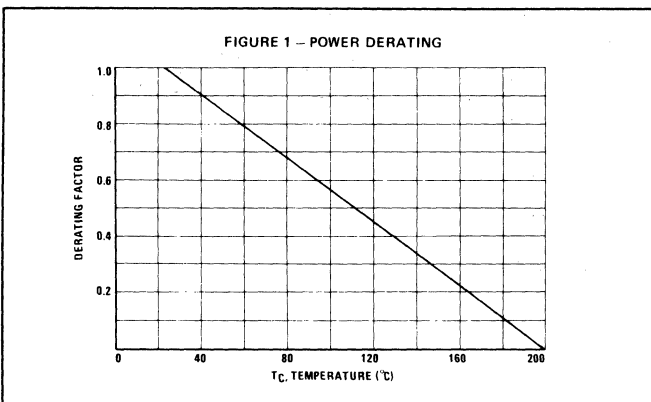
Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	$^\circ C/W$



NOTES
1 DIMENSIONS G AND V ARE DATUMS
2 [] IS SEATING PLANE AND DATUM
3 POSITIONAL TOLERANCE FOR MOUNTING HOLE D
 $\phi \pm 0.13 (0.005) \text{ T V } \textcircled{M}$
FOR LEADS
 $\phi \pm 0.13 (0.005) \text{ T V } \textcircled{M} \textcircled{D}$
4 DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.08	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.23	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05 TO-3



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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OFF CHARACTERISTICS¹

Collector-Emitter Sustaining Voltage ($I_C = 200\text{ mA}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{CEO(sus)}$	325		Vdc
Collector Cutoff Current at Reverse Bias: ($V_{CE} = 400\text{ V}$, $V_{BE} = -1.5\text{ V}$) ($V_{CE} = 400\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 125^\circ\text{C}$)	I_{CEX}		1.0 5.0	mAdc
Collector-Emitter Cutoff Current ($V_{CE} = 260\text{ V}$)	I_{CEO}		1.0	mAdc
Emitter-Base Reverse Voltage ($I_E = 50\text{ mA}$)	V_{EBO}	7		V
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}		1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ($V_{CE} = 30\text{ V}$, $t = 1\text{ s}$) ($V_{CE} = 135\text{ V}$, $t = 1\text{ s}$)	$I_{S/b}$	4.0 0.15		Adc
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ON CHARACTERISTICS¹

DC Current Gain ($I_C = 3\text{ A}$, $V_{CE} = 4\text{ V}$) ($I_C = 5\text{ A}$, $V_{CE} = 4\text{ V}$)	h_{FE}	15 8	60	
Collector-Emitter Saturation Voltage ($I_C = 3\text{ A}$, $I_B = 0.375\text{ A}$) ($I_C = 5\text{ A}$, $I_B = 1\text{ A}$)	$V_{CE(sat)}$		1.0 1.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 5\text{ A}$, $I_B = 1\text{ A}$)	$V_{BE(sat)}$		2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 1\text{ A}$, $f = 4\text{ MHz}$)	f_T	8.0		MHz
--	-------	-----	--	-----

SWITCHING CHARACTERISTICS (Resistive Load)

Turn on Time	$I_C = 5\text{ A}$, $I_{B1} = I_{B2} = 1\text{ A}$, ($V_{CC} = 150\text{ V}$, $R_C = 30\ \Omega$)	t_{on}	1.0	μs
Storage Time		t_s	2.2	
Fall Time		t_f	0.9	

¹ Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 2 - ACTIVE REGION SAFE OPERATING AREA

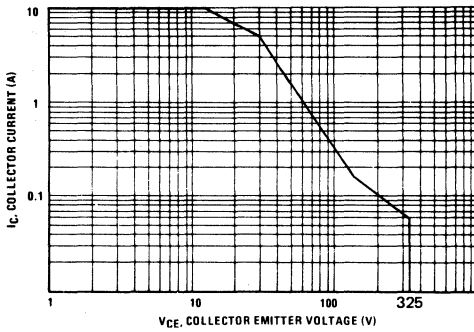


FIGURE 3 - "ON" VOLTAGES

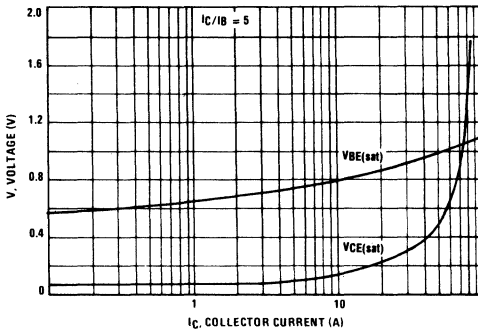
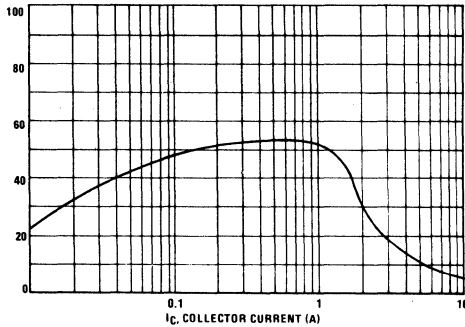


FIGURE 4 - DC CURRENT GAIN



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of figure 2 is based on $T_C = 25^\circ C$, $T_J(\rho k)$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

FIGURE 5 - RESISTIVE SWITCHING PERFORMANCE

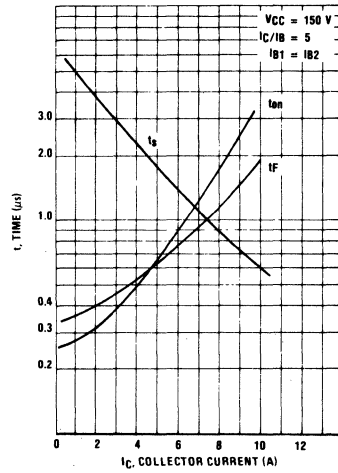
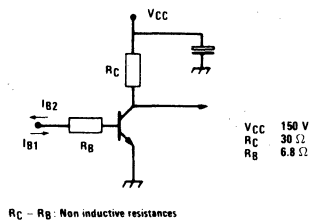


FIGURE 6 - SWITCHING TIMES TEST CIRCUIT



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BUX84
BUX85

SWITCHMODE
NPN SILICON POWER TRANSISTORS

The BUX 84/85 are designed for high voltage, high speed power switching applications like converters, inverters, switching regulators, motor control systems.

SPECIFICATIONS FEATURES:

- $V_{CE(sus)}$ { 400 V BUX 84
450 V BUX 85
- $V_{CES(sus)}$ { 800 V BUX 84
1000 V BUX 85
- Fall time = 0.3 us (typ) at $I_C = 1$ A
- $V_{CE(sat)} = 1$ V (max) at $I_C = 1$ A, $I_B = 0.2$ A

MAXIMUM RATINGS

Rating	Symbol	BUX 84	BUX 85	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CES}	800	1000	Vdc
Emitter Base Voltage	V_{EBO}	5		Vdc
Collector Current	I_C	2		Adc
- Continuous	I_{CM}	3.0		
- Peak (1)				
Base Current	I_B	0.75		Adc
- Continuous	I_{BM}	1.0		
- Peak (1)				
Reverse Base Current:				Adc
- Peak	I_{BM}	1		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	50		Watts
Derate above 25°C		400		mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 65 to +150		$^\circ\text{C}$

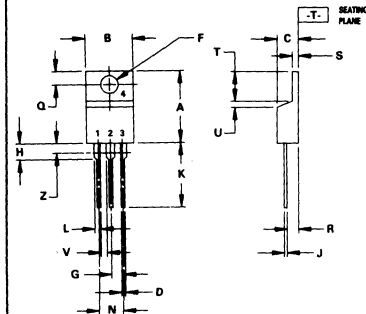
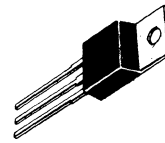
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient:	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Test. Pulse Width = 5 ms, Duty Cycle \leq 10%.

2 AMPERES
TRIPLE DIFFUSED
POWER TRANSISTORS
NPN SILICON

400 - 450 VOLTS
50 WATTS



NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION - INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.84	0.88	0.035	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.06	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

BUX84 BUX85

ELECTRICAL CHARACTERISTICS (TC = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (IC = 100 mAdc, (L = 25 mH) See fig. 1)	BUX 84 BUX 85	VCEO(sus) 400 450	- -	- -	Vdc
Collector Cutoff Current (VCEs = Rated Value) (VCEs = Rated Value, TC = 125 °C)	ICES	- -	- -	0.2 1.5	mAdc
Emitter Cutoff Current (VEB = 5 Vdc, IC = 0)	IEBO	-	-	1	mAdc

ON CHARACTERISTICS (1)

DC Current Gain (IC = 0.1 Adc, VCE = 5 V)	hFE	30	50	-	-
Collector-Emitter Saturation Voltage (IC = 0.3 Adc, IB = 30 mAdc) (IC = 1 Adc, IB = 200 mAdc)	VCE(sat)	- -	- -	0.8 1	Vdc
Base-Emitter Saturation Voltage (IC = 1 Adc, IB = 0.2 Adc)	VBE(sat)	-	-	1.1	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain - Bandwidth Product (IC = 500 mAdc, VCE = 10 Vdc, f = 1 MHz)	fT	4	-	-	MHz
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SWITCHING CHARACTERISTICS

Turn-on Time	VCC = 250 Vdc, IC = 1 A IB1 = 0.2 A, IB2 = 0.4 A See fig. 2 Same above cond. at TC = 95°C	ton	-	0.3	0.5	μs
Storage Time		ts	-	2	3.5	μs
Fall Time		tf	-	0.3	-	μs
Fall Time		tf	-	-	1.4	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 - TEST CIRCUIT FOR $V_{CE0\text{ sust}}$

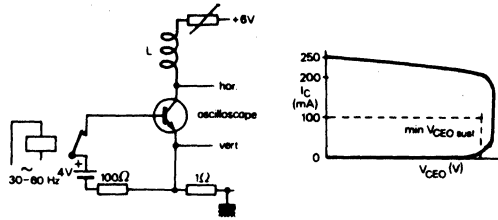
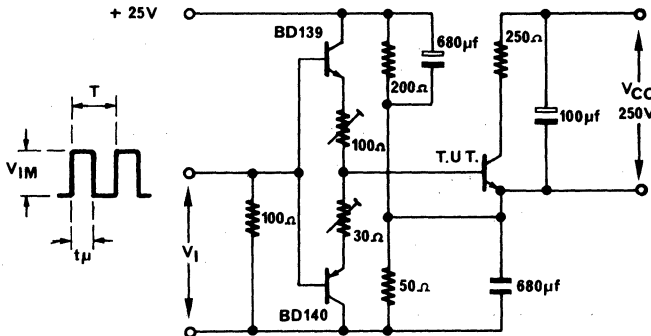
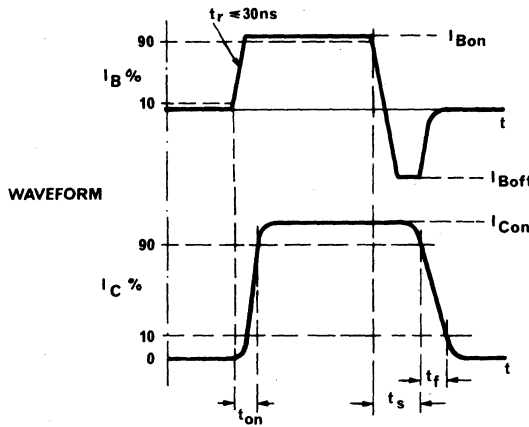


FIGURE 2 - SWITCHING TIMES / TEST CIRCUIT



NPN
D44E Series
PNP
D45E Series

**COMPLEMENTARY SILICON POWER
 DARLINGTON TRANSISTORS**

... for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)} = 2.0 \text{ V (Max) @ } 10 \text{ A}$
- High DC Current Gain — 1000 (Min) @ 5.0 Adc
- Complementary Pairs Simplifies Designs

DARLINGTON
10 AMPERE

**COMPLEMENTARY SILICON
 POWER TRANSISTORS**

40-80 VOLTS
50 WATTS

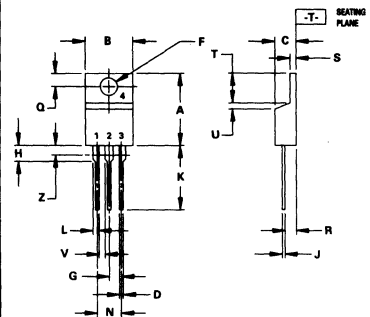
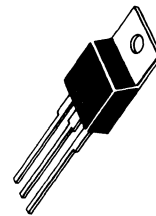
MAXIMUM RATINGS

Rating	Symbol	D44E or D45E			Unit
		1	2	3	
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter Base Voltage	V_{EB}	7.0			Vdc
Collector Current — Continuous Peak (1)	I_C	10 20			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_A = 25^\circ\text{C}$	P_D	50 1.67			Watts
Operating and Storage Junction Temperature Range	T_J , T_{stg}	-55 to 150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Width $\leq 6.0 \text{ ms}$, Duty Cycle $\leq 50\%$.



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

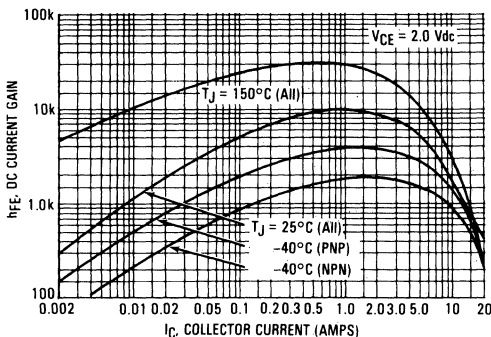
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.56	10.29	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.90	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.38	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.38	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 221A-04
TO-220AB

3

FIGURE 1 — TYPICAL DC CURRENT GAIN



D44E Series NPN, D45 Series PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CE0}, V_{BE} = 0$)	I_{CES}	—	—	10	μA
Emitter Cutoff Current ($V_{EB} = 7.0 \text{ Vdc}$)	I_{EBO}	—	—	1.0	μA
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 5.0 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}$)	h_{FE}	1000	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 5.0 \text{ Adc}, I_B = 10 \text{ mAdc}$) ($I_C = 10 \text{ Adc}, I_B = 20 \text{ mAdc}$)	$V_{CE(sat)}$	—	—	1.5 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0 \text{ Adc}, I_B = 10 \text{ mAdc}$)	$V_{BE(sat)}$	—	—	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance ($V_{CB} = 10 \text{ Vdc}, f_{test} = 1.0 \text{ MHz}$)	C_{CBO}	—	—	130 220	μF
	D44E Series	—	—	—	—
	D45E Series	—	—	—	—
SWITCHING CHARACTERISTICS					
Delay and Rise Times ($I_C = 10 \text{ Adc}, I_{B1} = 20 \text{ mAdc}$)	$t_d + t_r$	—	0.6	—	μs
Storage Time ($I_C = 10 \text{ Adc}, I_{B1} = I_{B2} = 20 \text{ mAdc}$)	t_s	—	2.0	—	μs
Fall Time ($I_C = 10 \text{ Adc}, I_{B1} = I_{B2} = 20 \text{ mAdc}$)	t_f	—	0.5	—	μs

SAFE OPERATING AREA INFORMATION

FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (NPN)

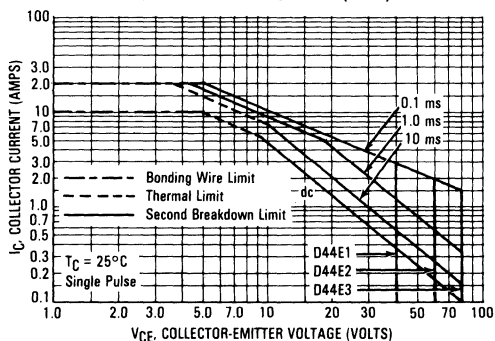
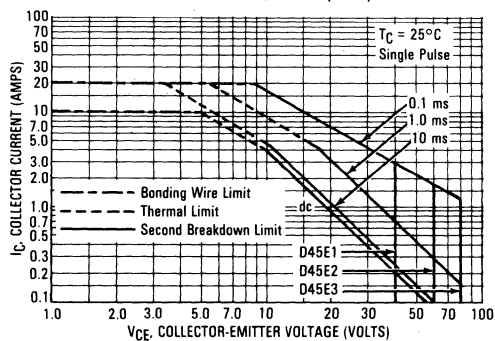


FIGURE 3 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (PNP)



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

NPN D44H Series PNP D45H Series

COMPLEMENTARY SILICON POWER TRANSISTORS

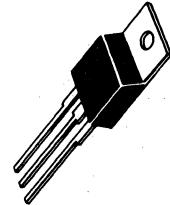
... for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 1.0 \text{ V (Max) @ } 8.0 \text{ A}$
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

10 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

30-80 VOLTS



MAXIMUM RATINGS

Rating	Symbol	D44H or D45H				Unit
		1,2	4,5	7,8	10,11	
Collector-Emitter Voltage	V_{CEO}	30	45	60	80	Vdc
Emitter Base Voltage	V_{EB}	5.0				Vdc
Collector Current — Continuous Peak (1)	I_C	10 20				Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_A = 25^\circ\text{C}$	P_D	50 1.67				Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ\text{C}$

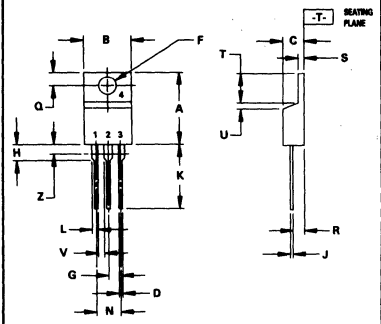
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Width $\leq 6.0 \text{ ms}$, Duty Cycle $\leq 50\%$.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
DC Current Gain ($V_{CE} = 1.0 \text{ Vdc}, I_C = 2.0 \text{ Adc}$)	D44H1,4,7,10 D45H1,4,7,10	h_{FE}	35	—	—
	D44H2,5,8,11 D45H2,5,8,11		60	—	—
($V_{CE} = 1.0 \text{ Vdc}, I_C = 4.0 \text{ Adc}$)	D44H1,4,7,10 D45H1,4,7,10		20	—	—
	D44H2,5,8,11 D45H2,5,8,11		40	—	—



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.90	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
M	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.78	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:
PIN 1: BASE
2: COLLECTOR
3: EMITTER
4: COLLECTOR

CASE 221A-04
TO-220AB

D44H Series NPN, D45H Series PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CE0}, V_{BE} = 0$)	I_{CES}	—	—	10	μA
Emitter Cutoff Current ($V_{EB} = 5.0 \text{ Vdc}$)	I_{EBO}	—	—	100	μA
ON CHARACTERISTICS					
Collector-Emitter Saturation Voltage ($I_C = 8.0 \text{ Adc}, I_B = 0.4 \text{ Adc}$) ($I_C = 8.0 \text{ Adc}, I_B = 0.8 \text{ Adc}$)	$V_{CE(sat)}$	— —	— —	1.0 1.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 8.0 \text{ Adc}, I_B = 0.8 \text{ Adc}$)	$V_{BE(sat)}$	—	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance ($V_{CB} = 10 \text{ Vdc}, f_{\text{test}} = 1.0 \text{ MHz}$)	C_{cb}	—	130 230	—	pF
Gain Bandwidth Product ($I_C = 0.5 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 20 \text{ MHz}$)	f_T	—	50 40	—	MHz
SWITCHING TIMES					
Delay and Rise Times ($I_C = 5.0 \text{ Adc}, I_{B1} = 0.5 \text{ Adc}$)	$t_d + t_r$	—	300 135	—	ns
Storage Time ($I_C = 5.0 \text{ Adc}, I_{B1} = I_{B2} = 0.5 \text{ Adc}$)	t_s	—	500 500	—	ns
Fall Time ($I_C = 5.0 \text{ Adc}, I_{B1} = I_{B2} = 0.5 \text{ Adc}$)	t_f	—	140 100	—	ns

FIGURE 1 — NORMALIZED DC CURRENT GAIN

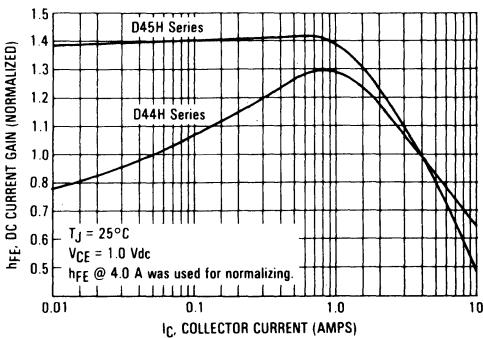
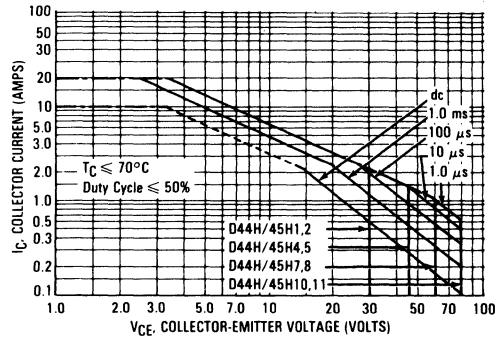


FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



NPN
D44VH Series
PNP
D45VH Series

COMPLEMENTARY SILICON POWER TRANSISTORS

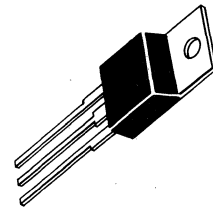
These complementary silicon power transistors are designed for high-speed switching applications, such as switching regulators and high frequency inverters. The devices are also well-suited for drivers for high power switching circuits.

- Fast Switching — $t_f = 90$ ns (Max)
- Key Parameters Specified @ 100°C
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)} = 1.0$ V (Max) @ 8.0 A
- Complementary Pairs Simplify Circuit Designs

15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

30, 45, 60 and 80 VOLTS
83 WATTS



MAXIMUM RATINGS

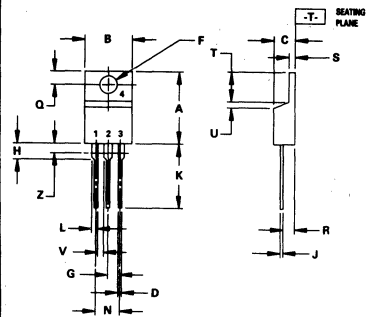
Rating	Symbol	D44VH or D45VH				Unit
		1	4	7	10	
Collector-Emitter Voltage	V_{CEO}	30	45	60	80	Vdc
Collector-Emitter Voltage	V_{CEV}	50	70	80	100	Vdc
Emitter Base Voltage	V_{EB}	7.0				Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	15 20				Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	83 1.67				Watts W/°C
Operating and Storage Junction Temperature Range	T_J , T_{stg}	-55 to 150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle $\leq 50\%$.

Note 1: All polarities are shown for NPN transistors. For PNP transistors, reverse polarities.
 Note 2: See MJE5220/5230 Series data sheet for characteristic curves.



NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.86	0.095	0.105
H	2.90	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 221A-04
TO-220AB

D44VH Series NPN, D45VH Series PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I _C = 25 mA _{dc} , I _B = 0)	V _{CEO(sus)}	30 45 60 80	— — — —	— — — —	V _{dc}
Collector-Emitter Cutoff Current (V _{CE} = Rated V _{CEV} , V _{BE(off)} = 4.0 V _{dc}) (V _{CE} = Rated V _{CEV} , V _{BE(off)} = 4.0 V _{dc} , T _C = 100°C)	I _{CEV}	— —	— —	10 100	μA _{dc}
Emitter Base Cutoff Current (V _{EB} = 7.0 V _{dc} , I _C = 0)	I _{EBO}	—	—	10	μA _{dc}

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 2.0 A _{dc} , V _{CE} = 1.0 V _{dc}) (I _C = 4.0 A _{dc} , V _{CE} = 1.0 V _{dc})	h _{FE}	35 20	— —	— —	—
Collector-Emitter Saturation Voltage (I _C = 8.0 A _{dc} , I _B = 0.4 A _{dc}) (I _C = 8.0 A _{dc} , I _B = 0.8 A _{dc}) (I _C = 15 A _{dc} , I _B = 3.0 A _{dc} , T _C = 100°C)	V _{CE(sat)}	— — —	— — —	0.4 1.0 0.8 1.5	V _{dc}
Base-Emitter Saturation Voltage (I _C = 8.0 A _{dc} , I _B = 0.4 A _{dc}) (I _C = 8.0 A _{dc} , I _B = 0.8 A _{dc}) (I _C = 8.0 A _{dc} , I _B = 0.4 A _{dc} , T _C = 100°C) (I _C = 8.0 A _{dc} , I _B = 0.8 A _{dc} , T _C = 100°C)	V _{BE(sat)}	— — — —	— — — —	1.2 1.0 1.1 1.5	V _{dc}

DYNAMIC CHARACTERISTICS

Current Gain Bandwidth Product (I _C = 0.1 A _{dc} , V _{CE} = 10 V _{dc} , f = 20 MHz)	f _T	—	50	—	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _C = 0, f _{test} = 1.0 MHz)	C _{cb}	— —	120 275	— —	pF

SWITCHING CHARACTERISTICS

Delay Time	(V _{CC} = 20 V _{dc} , I _C = 8.0 A _{dc} , I _{B1} = I _{B2} = 0.8 A _{dc})	t _d	—	—	50	ns
Rise Time		t _r	—	—	250	
Storage Time		t _s	—	—	700	
Fall Time		t _f	—	—	90	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

HIGH VOLTAGE NPN SILICON TRANSISTORS

... designed for medium to high voltage inverters, converters, regulators and switching circuits.

- High Collector-Emitter Voltage –
 $V_{CE0} = 200$ Volts – MJ410
 300 Volts – MJ411
- DC Current Gain Specified @ 1.0 and 2.5 Adc
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.8$ Vdc @ $I_C = 1.0$ Adc

5 AMPERE
POWER TRANSISTORS
NPN SILICON
200-300 VOLTS
100 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJ410	MJ411	Unit
Collector-Emitter Voltage	V_{CE0}	200	300	Vdc
Collector-Base Voltage	V_{CB}	200	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	5.0		Adc
Peak		10		
Base Current	I_B	2.0		Adc
Total Device Dissipation @ $T_C = 75^\circ\text{C}$	P_D	100		Watts
Derate above 75°C		1.33		$\text{W}/^\circ\text{C}$
Operating Junction Temperature Range	T_J	-65 to +150		$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.75	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

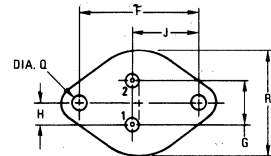
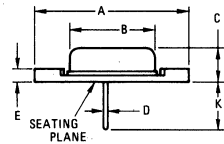
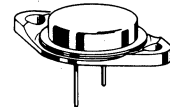
Collector-Emitter Sustaining Voltage ($I_C = 100$ mAdc, $I_B = 0$)	MJ410 MJ411	$V_{CE0(sus)}$	200 300	–	Vdc
Collector Cutoff Current ($V_{CE} = 200$ Vdc, $I_B = 0$)	MJ410	I_{CEO}	–	0.25	mAdc
($V_{CE} = 300$ Vdc, $I_B = 0$)	MJ411		–	0.25	
Collector Cutoff Current ($V_{CE} = 200$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 125^\circ\text{C}$)	MJ410	I_{CEX}	–	0.5	mAdc
($V_{CE} = 300$ Vdc, $V_{EB(off)} = 1.5$ Vdc, $T_C = 125^\circ\text{C}$)	MJ411		–	0.5	
Emitter Cutoff Current ($V_{EB} = 5.0$ Vdc, $I_C = 0$)		I_{EBO}	–	5.0	mAdc

ON CHARACTERISTICS

DC Current Gain ($I_C = 1.0$ Adc, $V_{CE} = 5.0$ Vdc)		h_{FE}	30	90	–
($I_C = 2.5$ Adc, $V_{CE} = 5.0$ Vdc)			10	–	
Collector-Emitter Saturation Voltage ($I_C = 1.0$ Adc, $I_B = 0.1$ Adc)		$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0$ Adc, $I_B = 0.1$ Adc)		$V_{BE(sat)}$	–	1.2	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 200$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)		f_T	2.5	–	MHz
--	--	-------	-----	---	-----

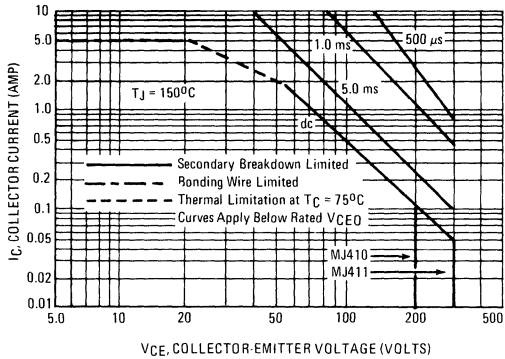


STYLE 1:
 PIN 1: BASE
 CASE: COLLECTOR
 NOTE:
 2. EMITTER
 1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	28.67	–	1.050

CASE 11-01
 TO-3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 2 – DC CURRENT GAIN

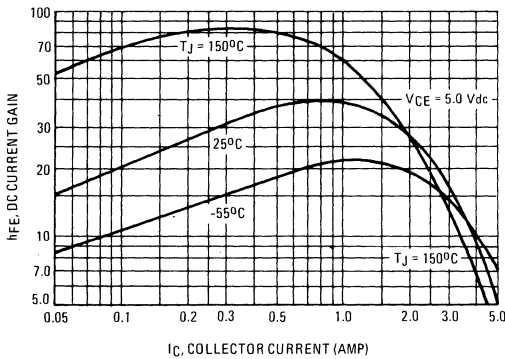


FIGURE 3 – "ON" VOLTAGES

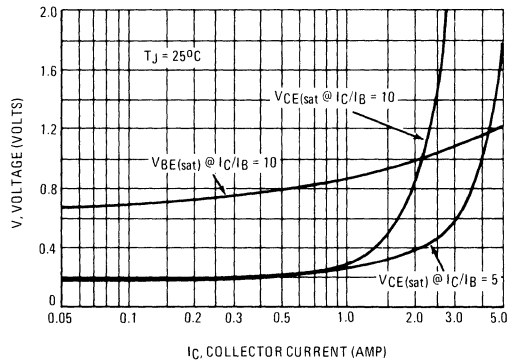


FIGURE 4 – SUSTAINING VOLTAGE TEST LOAD LINE

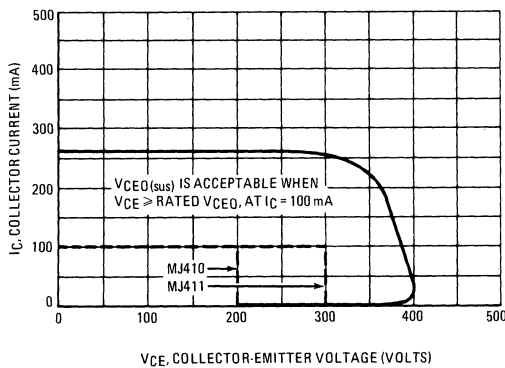
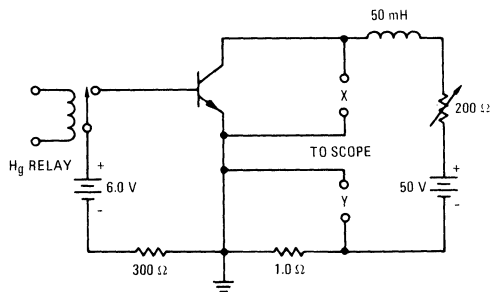


FIGURE 5 – SUSTAINING VOLTAGE TEST CIRCUIT



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

MJ413 MJ423 MJ431

HIGH-VOLTAGE NPN SILICON TRANSISTORS

... designed for medium-to-high voltage inverters, converters, regulators and switching circuits.

- High Voltage — $V_{CEX} = 400$ Vdc
- Gain Specified to 3.5 Amp
- High Frequency Response to 2.5 MHz

10 AMPERE
POWER TRANSISTORS
NPN SILICON

400 VOLTS
125 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJ413	MJ423	MJ431	Unit
Collector-Emitter Voltage	V_{CEX}	400	400	400	Vdc
Collector-Base Voltage	V_{CB}	400	400	400	Vdc
Emitter-Base Voltage	V_{EB}	5.0	5.0	5.0	Vdc
Collector Current — Continuous	I_C	10	10	10	Adc
Base Current	I_B	2.0	2.0	2.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	125 1.0			Watts w/ $^\circ\text{C}$
Operation Junction Temperature Range	T_J	-65 to +150			$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +200			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ⁽¹⁾ ($I_C = 100$ mA, $I_B = 0$)	$V_{BR}/CEO(sus)$	325	—	Vdc
Collector Cutoff Current ($V_{CE} = 400$ Vdc, $V_{EB}(off) = 1.5$ Vdc)	I_{CEX}	—	0.25	mA
($V_{CE} = 400$ Vdc, $V_{EB}(off) = 1.5$ Vdc, $T_C = 125^\circ\text{C}$)		—	2.5	mA
		—	0.5	mA
		—	5.0	mA
Emitter Cutoff Current ($V_{BE} = 5.0$ Vdc, $I_C = 0$)	I_{EBO}	—	5.0	mA
		—	2.0	mA

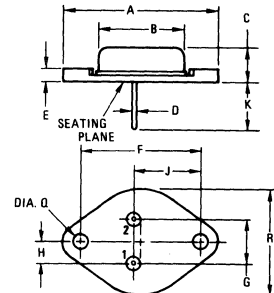
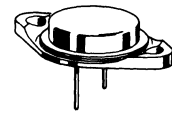
ON CHARACTERISTICS

DC Current Gain ⁽¹⁾ ($I_C = 0.5$ Adc, $V_{CE} = 5.0$ Vdc)	MJ413	h_{FE}	20	80	—
($I_C = 1.0$ Adc, $V_{CE} = 5.0$ Vdc)			15	—	
($I_C = 1.0$ Adc, $V_{CE} = 5.0$ Vdc)	MJ423		30	90	
($I_C = 2.5$ Adc, $V_{CE} = 5.0$ Vdc)			10	—	
($I_C = 2.5$ Adc, $V_{CE} = 5.0$ Vdc)	MJ431		15	35	
($I_C = 3.5$ Adc, $V_{CE} = 5.0$ Vdc)			10	—	
Collector-Emitter Saturation Voltage ⁽¹⁾ ($I_C = 0.5$ Adc, $I_B = 0.05$ Adc)	MJ413	$V_{CE(sat)}$	—	0.8	Vdc
($I_C = 1.0$ Adc, $I_B = 0.10$ Adc)	MJ423		—	0.8	
($I_C = 2.5$ Adc, $I_B = 0.5$ Adc)	MJ431		—	0.7	
Base-Emitter Saturation Voltage ⁽¹⁾ ($I_C = 0.5$ Adc, $I_B = 0.05$ Adc)	MJ413	$V_{BE(sat)}$	—	1.25	Vdc
($I_C = 1.0$ Adc, $I_B = 0.1$ Adc)	MJ423		—	1.25	
($I_C = 2.5$ Adc, $I_B = 0.5$ Adc)	MJ431		—	1.5	

DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product ($I_C = 200$ mA, $V_{CE} = 10$ Vdc, $f = 1.0$ MHz)	f_T	2.5	—	MHz
--	-------	-----	---	-----

(1) $PW \leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

CASE 11-01
TO-3

FIGURE 1 — ACTIVE-REGION SAFE-OPERATING AREA

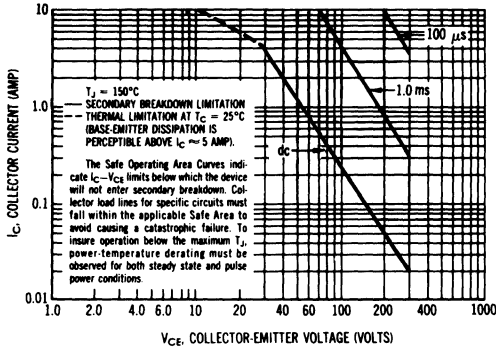


FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

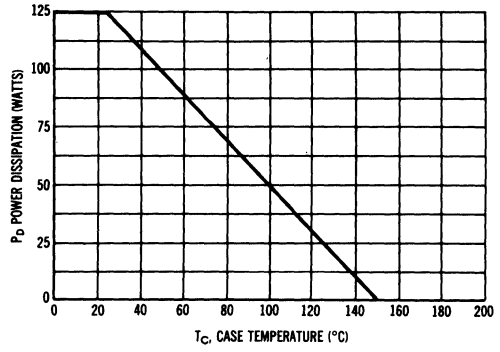


FIGURE 3 — SUSTAINING VOLTAGE TEST LOAD LINE

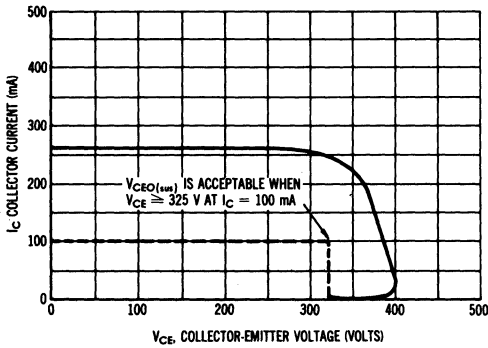


FIGURE 4 — SUSTAINING VOLTAGE TEST CIRCUIT

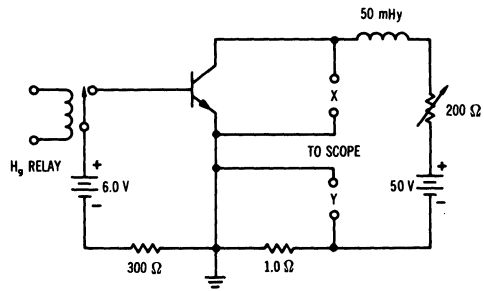


FIGURE 5 — CURRENT GAIN

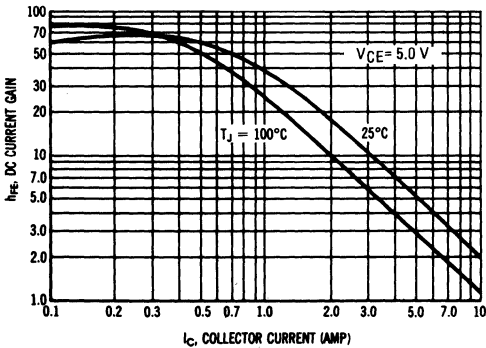
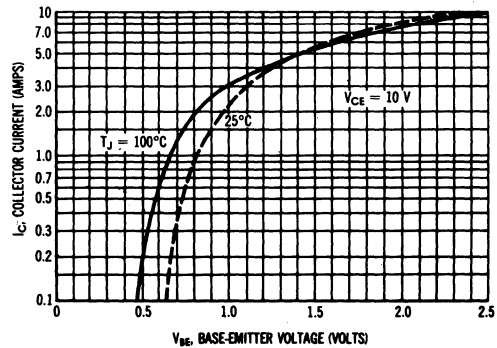


FIGURE 6 — TRANSCONDUCTANCE



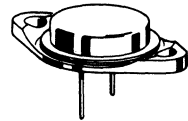
HIGH-POWER NPN SILICON TRANSISTOR

... for use as an output device in complementary audio amplifiers to 100-Watts music power per channel.

- High DC Current Gain – $h_{FE} = 25-100 @ I_C = 7.5 \text{ A}$
- Excellent Safe Operating Area
- Complement to the PNP MJ4502

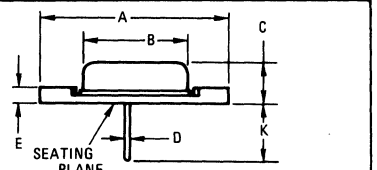
**30 AMPERE
 POWER TRANSISTOR**

NPN SILICON
100 VOLTS
200 WATTS

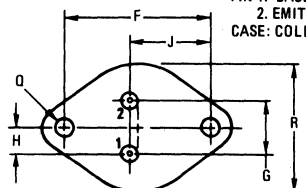


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CE}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Collector-Emitter Voltage	V_{CEO}	90	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	200 1.14	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE: COLLECTOR



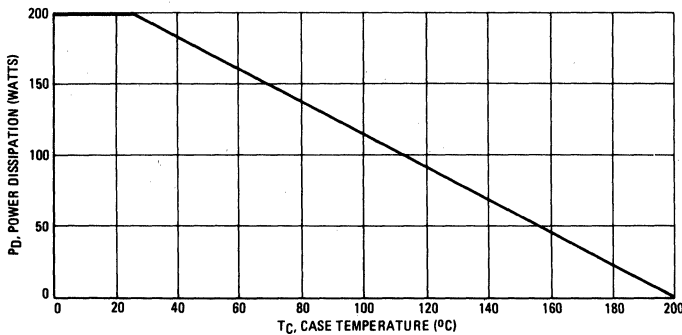
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

NOTE:
 1. DIM "Q" IS DIA. CASE 11-01
 TO-3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	$^\circ\text{C}/\text{W}$

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ⁽¹⁾ ($I_C = 200 \text{ mA dc}$, $R_{BE} = 100 \text{ Ohms}$)	BV_{CER}	100	—	Vdc
Collector-Emitter Sustaining Voltage ⁽¹⁾ ($I_C = 200 \text{ mA dc}$)	$V_{CEO(sus)}$	90	—	Vdc
Collector-Base Cutoff Current ($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$, $T_C = 150^\circ\text{C}$)	I_{CBO}	—	1.0 5.0	mA dc
Emitter-Base Cutoff Current ($V_{BE} = 4.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	mA dc
ON CHARACTERISTICS ⁽¹⁾				
DC Current Gain ⁽¹⁾ ($I_C = 7.5 \text{ A dc}$, $V_{CE} = 2.0 \text{ Vdc}$)	h_{FE}	25	100	—
Base-Emitter "On" Voltage ($I_C = 7.5 \text{ A dc}$, $V_{CE} = 2.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.3	Vdc
Collector-Emitter Saturation Voltage ($I_C = 7.5 \text{ A dc}$, $I_B = 0.75 \text{ A dc}$)	$V_{CE(sat)}$	—	0.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 7.5 \text{ A dc}$, $I_B = 0.75 \text{ A dc}$)	$V_{BE(sat)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain - Bandwidth Product ($I_C = 1.0 \text{ A dc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	f_T	2.0	—	MHz

⁽¹⁾ Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 - DC CURRENT GAIN

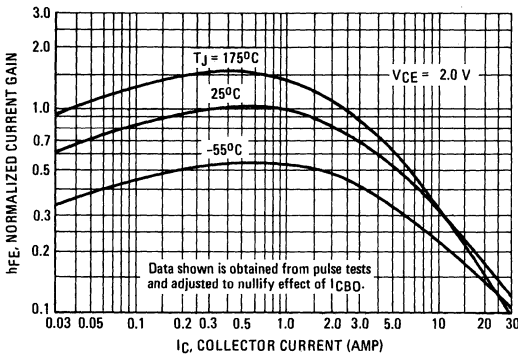


FIGURE 3 - "ON" VOLTAGES

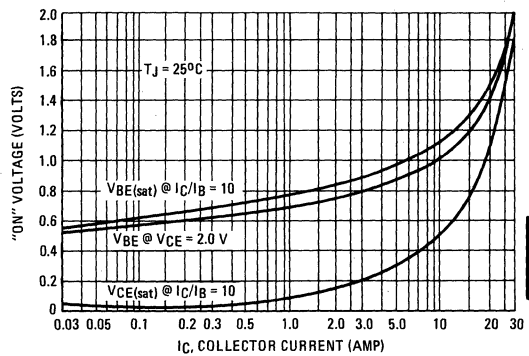
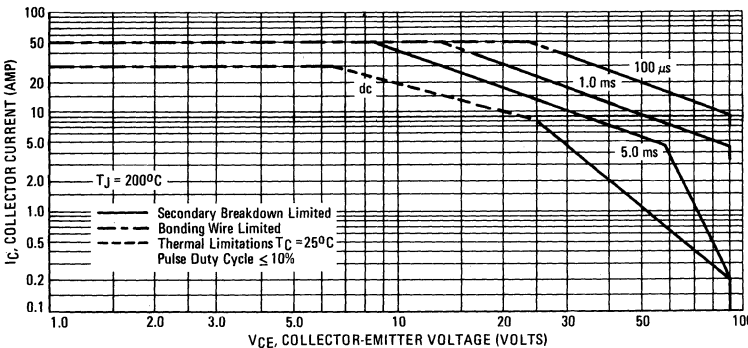


FIGURE 4 - ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

**PNP
MJ900, MJ901
NPN
MJ1000, MJ1001**

MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

... for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – $h_{FE} = 6000$ (Typ) @ $I_C = 3.0$ Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

**8.0 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON**

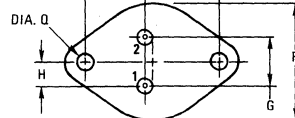
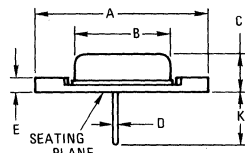
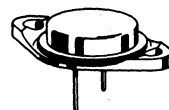
**60-80 VOLTS
90 WATTS**

MAXIMUM RATINGS

Rating	Symbol	MJ900 MJ1000	MJ901 MJ1001	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	8.0		Adc
Base Current	I_B	0.1		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	90	0.515	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.94	$^\circ\text{C}/\text{W}$



STYLE 1:

PIN 1. BASE

2. EMITTER

CASE: COLLECTOR

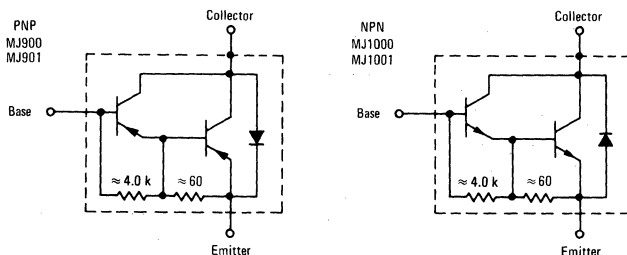
NOTE:

1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

Collector connected to case.
CASE 11-01
(TO-3)

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC



MJ900, MJ901 PNP/MJ1000, MJ1001 NPN

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I _C = 100 mA _{dc} , I _B = 0)	V _{(BR)CEO}	60 80	—	V _{dc}
Collector Emitter Leakage Current (V _{CB} = 60 V _{dc} , R _{BE} = 1.0 k ohm) MJ900, MJ1000 (V _{CB} = 80 V _{dc} , R _{BE} = 1.0 k ohm) MJ901, MJ1001 (V _{CB} = 60 V _{dc} , R _{BE} = 1.0 k ohm, T _C = 150°C) MJ900, MJ1000 (V _{CB} = 80 V _{dc} , R _{BE} = 1.0 k ohm, T _C = 150°C) MJ901, MJ1001	I _{CER}	—	1.0 1.0 5.0 5.0	mA _{dc}
Emitter Cutoff Current (V _{BE} = 5.0 V _{dc} , I _C = 0)	I _{EBO}	—	2.0	mA _{dc}
Collector-Emitter Leakage Current (V _{CE} = 30 V _{dc} , I _B = 0) MJ900, MJ1000 (V _{CE} = 40 V _{dc} , I _B = 0) MJ901, MJ1001	I _{CEO}	—	500 500	μA _{dc}
ON CHARACTERISTICS				
DC Current Gain(1) (I _C = 3.0 A _{dc} , V _{CE} = 3.0 V _{dc}) (I _C = 4.0 A _{dc} , V _{CE} = 3.0 V _{dc})	h _{FE}	1000 750	—	—
Collector-Emitter Saturation Voltage(1) (I _C = 3.0 A _{dc} , I _B = 12 mA _{dc}) (I _C = 8.0 A _{dc} , I _B = 40 mA _{dc})	V _{CE(sat)}	—	2.0 4.0	V _{dc}
Base-Emitter Voltage(1) (I _C = 3.0 A _{dc} , V _{CE} = 3.0 V _{dc})	V _{BE}	—	2.5	V _{dc}

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

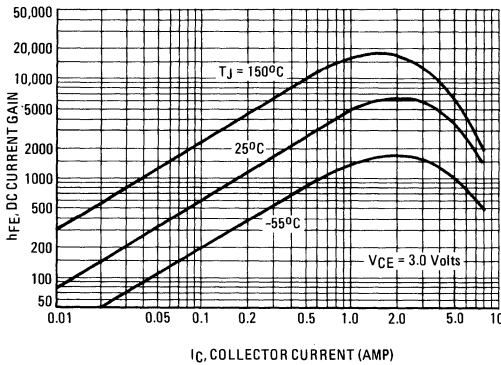
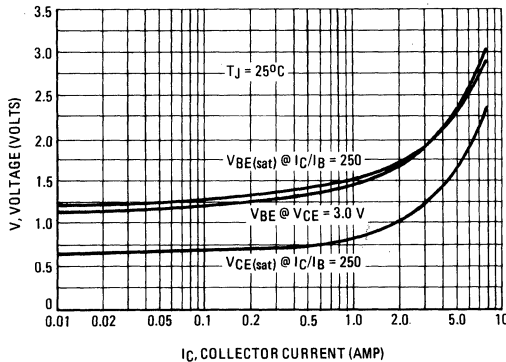


FIGURE 4 – “ON” VOLTAGES



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor

FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

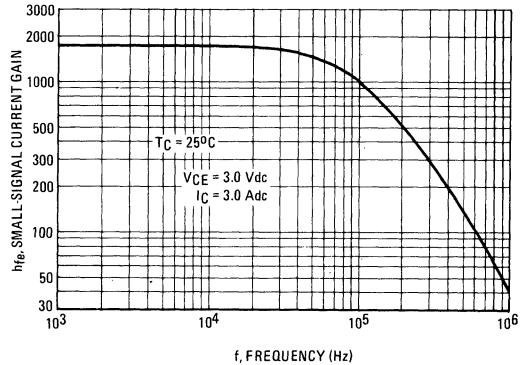
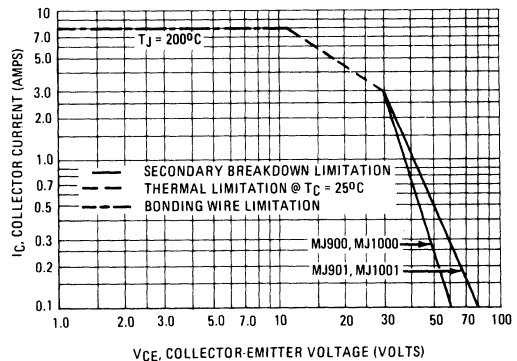


FIGURE 5 – DC SAFE OPERATING AREA



must not be subjected to greater dissipation than the curves indicate. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

PNP
MJ2500, MJ2501
NPN
MJ3000, MJ3001

MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

... for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain - $h_{FE} = 4000$ (Typ) @ $I_C = 5.0$ Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

10 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON

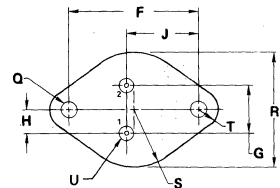
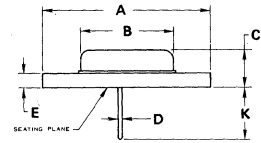
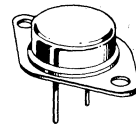
60-80 VOLTS
150 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJ2500 MJ3000	MJ2501 MJ3001	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	10		A dc
Base Current	I_B	0.2		A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	150		Watts
		0.857		W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C}/\text{W}$



STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

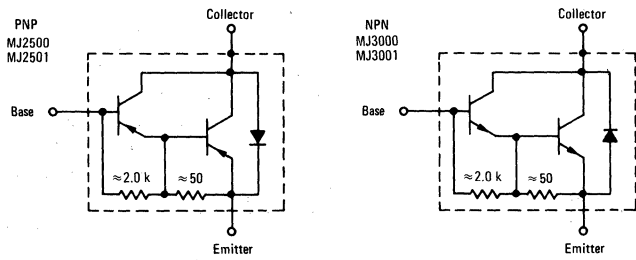
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	2.54	3.05	0.100	0.120

CASE1-04

NOTES:
 1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

3

FIGURE 1 - DARLINGTON CIRCUIT SCHEMATIC



MJ2500, MJ2501 PNP/MJ3000, MJ3001 NPN

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage(1) ($I_C = 100 \text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	60 80	—	Vdc
Collector-Emitter Leakage Current ($V_{EB} = 60 \text{ Vdc}$, $R_{BE} = 1.0 \text{ k ohm}$) ($V_{EB} = 80 \text{ Vdc}$, $R_{BE} = 1.0 \text{ k ohm}$) ($V_{EB} = 60 \text{ Vdc}$, $R_{BE} = 1.0 \text{ k ohm}$, $T_C = 150^\circ\text{C}$) ($V_{EB} = 80 \text{ Vdc}$, $R_{BE} = 1.0 \text{ k ohm}$, $T_C = 150^\circ\text{C}$)	I_{CER}	— — — —	1.0 1.0 5.0 5.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	2.0	mAdc
Collector-Emitter Leakage Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	— —	1.0 1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 5.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	h_{FE}	1000	—	—
Collector-Emitter Saturation Voltage ($I_C = 5.0 \text{ Adc}$, $I_B = 20 \text{ mAdc}$) ($I_C = 10 \text{ Adc}$, $I_B = 50 \text{ mAdc}$)	$V_{CE(sat)}$	— —	2.0 4.0	Vdc
Base-Emitter Voltage ($I_C = 5.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	V_{BE}	—	3.0	Vdc

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 – DC CURRENT GAIN

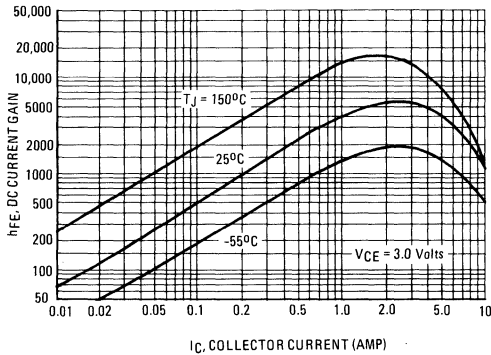


FIGURE 4 – "ON" VOLTAGES

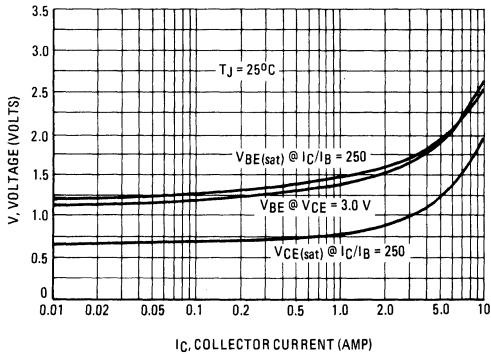


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

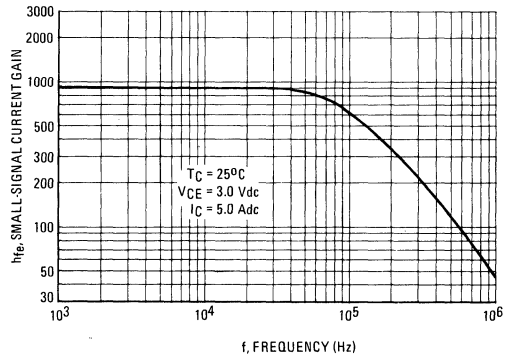
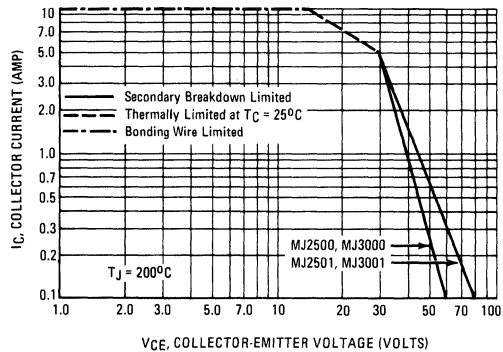


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must

not be subjected to greater dissipation than the curves indicate. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

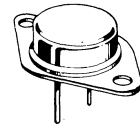
MJ3029

NPN SILICON HIGH-VOLTAGE TRANSISTOR

... designed for TV horizontal and vertical deflection amplifier circuits.

- High Collector-Emitter Sustaining Voltage — $V_{CEO(sus)} = 250$ Vdc (Min) MJ3029
- Fast Fall Time in Horizontal Deflection
- Excellent Gain Linearity for Vertical Deflection — $h_{fe} @ 0.4$ Adc, $h_{fe} @ 0.3$ Adc = 0.95 (Min)

5 AMPERE
POWER TRANSISTOR
NPN SILICON
250-325 VOLTS
125 WATTS

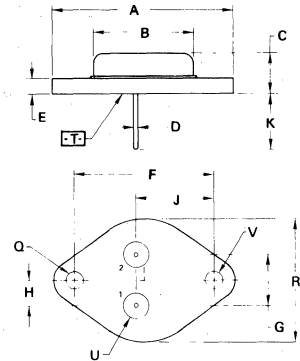


MAXIMUM RATINGS

Rating	Symbol	MJ3029	Unit
Collector-Emitter Voltage	V_{CEO}	250	Vdc
Collector-Emitter Voltage	V_{CER}	500	Vdc
Collector-Emitter Voltage	V_{CEX}	—	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	5.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	125 1.0	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	$^\circ\text{C}/\text{W}$



NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. \square IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\phi \pm 0.13 (0.005) \text{ (M)} \text{ (T)} \text{ (V)} \text{ (M)}$$

FOR LEADS:

$$\phi \pm 0.13 (0.005) \text{ (M)} \text{ (T)} \text{ (V)} \text{ (M)} \text{ (Q)} \text{ (M)}$$

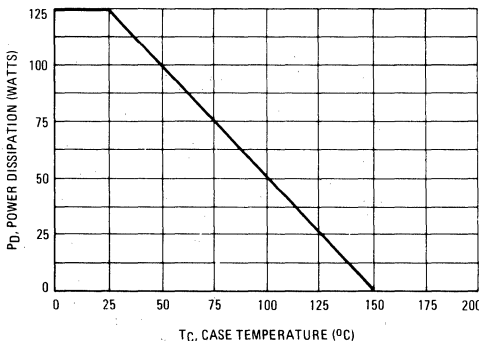
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

STYLE 1
 PIN 1 BASE
 2 EMITTER
 CASE COLLECTOR

CASE 1-05

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage(1) (I _C = 0.1 Adc, I _B = 0)	MJ3029	V _{CEO(sus)}	250	—	Vdc
Collector Cutoff Current (V _{CE} = 500 Vdc, R _{BE} = 1.5 k Ohms)	MJ3029	I _{CER}	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I _C = 0.3 Adc, V _{CE} = 5.0 Vdc)(1) (I _C = 0.4 Adc, V _{CE} = 5.0 Vdc)(1)	h _{FE 1}	25	—	—	
	h _{FE 2}	30	—	—	
Gain Linearity	h _{FE 2} h _{FE 1}	0.95	—	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

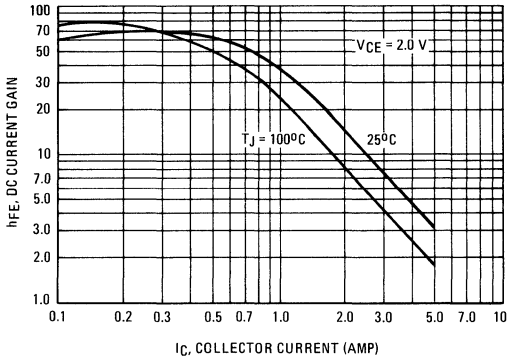
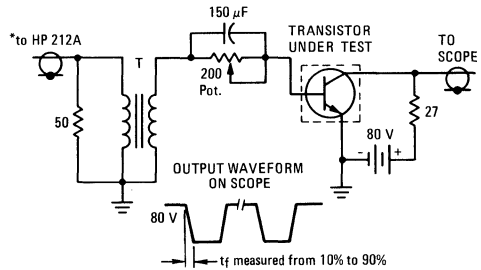
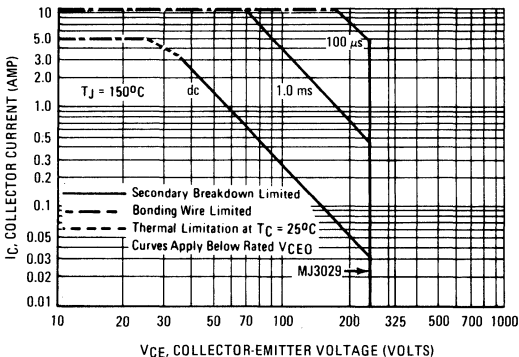


FIGURE 3 – TEST FOR FALL TIME



*HP 212A: Set for 10 μs wide pulses at 2000 pulses per sec. (500 μs intervals). Adjust for I_{B1} = 0.8 A.
Bias: Adjust to 1.5 V on a VTVM across the 200 Ω Pot.
T: Pulse Transformer: Motorola Part No. 25D68782A01.

FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 4 is based on T_{J(pk)} = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided T_{J(pk)} ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJ3040
MJ3041
MJ3042

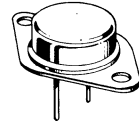
HIGH VOLTAGE SILICON POWER
DARLINGTONS

... developed for line operated amplifier, series pass and switching regulator applications.

- Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 300 \text{ Vdc (Min) – MJ3040, MJ3041}$
 $= 350 \text{ Vdc (Min) – MJ3042}$
- High DC Current Gain –
 $h_{FE} = 100 \text{ (Min) @ } I_C = 2.5 \text{ Adc – MJ3040}$
 $= 250 \text{ (Min) @ } I_C = 2.5 \text{ Adc – MJ3041, MJ3042}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 2.2 \text{ Vdc (Max) @ } I_C = 2.5 \text{ Adc}$
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON
10 AMPERE
POWER TRANSISTORS
NPN SILICON

300, 350 VOLTS
175 WATTS



MAXIMUM RATINGS

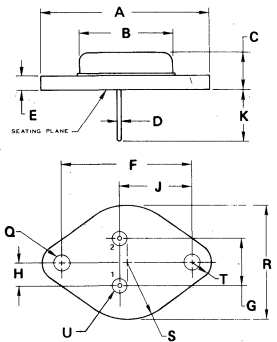
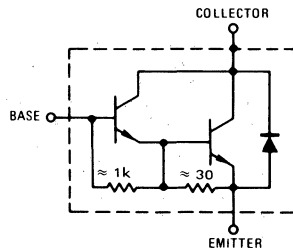
Rating	Symbol	MJ3040	MJ3041	MJ3042	Unit
Collector-Base Voltage	V_{CB}	400	400	500	Vdc
Collector-Emitter Voltage	V_{CE}	300	300	350	Vdc
Emitter-Base Voltage	V_{EB}	← 8.0 →			Vdc
Collector Current – Continuous	I_C	← 10 →			A dc
– Peak (1)		← 15 →			
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 175 →			Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$

(1) Pulse Width = 5.0 ms, Duty Cycle \leq 10%.

DARLINGTON SCHEMATIC



STYLE 1

PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120

CASE1-04

NOTES:

1. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-3 OUTLINE SHALL APPLY.

MJ3040, MJ3041, MJ3042

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

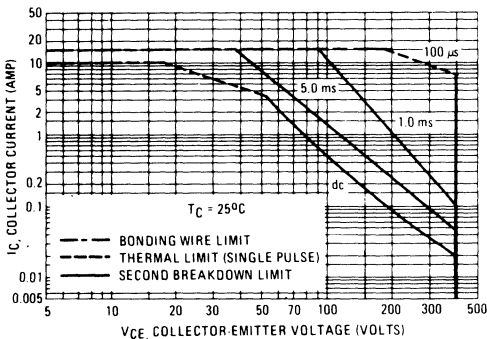
OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 100 \text{ mAdc}$, $I_B = 0$)	MJ3040, MJ3041 MJ3042	$V_{CE(sus)}$	300 350	— —	Vdc
Collector Cutoff Current ($V_{CB} = 400 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 500 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 400 \text{ Vdc}$, $I_E = 0$, $T_C = 100^\circ\text{C}$) ($V_{CB} = 500 \text{ Vdc}$, $I_E = 0$, $T_C = 100^\circ\text{C}$)	MJ3040, MJ3041 MJ3042 MJ3040, MJ3041 MJ3042	I_{CBO}	— — — —	— 1.0 1.0 5.0 5.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	40	mAdc

ON CHARACTERISTICS

DC Current Gain ($I_C = 2.5 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 5.0 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$)	MJ3040 MJ3041, MJ3042 MJ3040 MJ3041, MJ3042	h_{FE}	100 250 25 50	— — — —	—
Collector-Emitter Saturation Voltage ($I_C = 2.5 \text{ Adc}$, $I_B = 50 \text{ mAdc}$) ($I_C = 5.0 \text{ Adc}$, $I_B = 400 \text{ mAdc}$)		$V_{CE(sat)}$	— —	2.2 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0 \text{ Adc}$, $I_B = 400 \text{ mAdc}$)		$V_{BE(sat)}$	—	3.0	Vdc
Base-Emitter On Voltage ($I_C = 2.5 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$)		$V_{BE(on)}$	—	2.5	Vdc

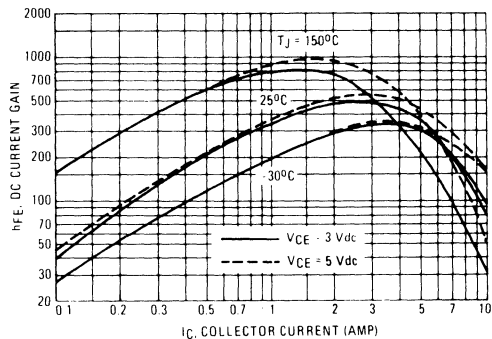
FIGURE 1 — FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor — average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 — DC CURRENT GAIN



MOTOROLA
SEMICONDUCTOR
 TECHNICAL DATA

PNP
MJ4030
MJ4031
MJ4032

NPN
MJ4033
MJ4034
MJ4035

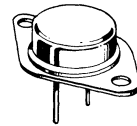
MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

... for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – $h_{FE} = 3500$ (Typ) @ $I_C = 10$ Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor

16 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON

60-100 VOLTS
150 WATTS

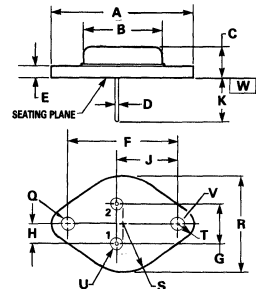


MAXIMUM RATINGS

Rating	Symbol	MJ4030 MJ4033	MJ4031 MJ4034	MJ4032 MJ4035	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current	I_C	16			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	150 0.857			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C}/\text{W}$



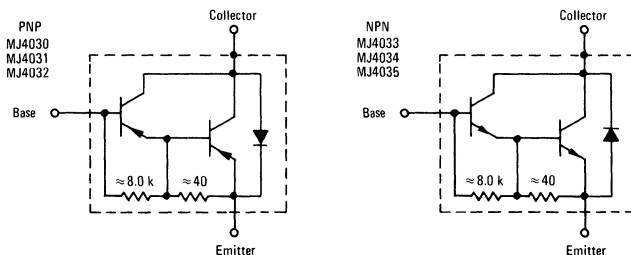
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.666 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—		26.67 — 1.050	
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

- STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR
- NOTES:
 1. DIAMETER V AND SURFACE W ARE DATUMS.
 2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\pm \phi 0.25$ (0.010) M W | V Q
 3. POSITIONAL TOLERANCE FOR LEADS:
 $\pm \phi 0.30$ (0.012) M W | V Q Q

CASE 1-04
TO-204AA

3

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC



PNP MJ4030, MJ4031, MJ4032 NPN MJ4033, MJ4034, MJ4035

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage(1) (I _C = 100 mA, I _B = 0)	V _{(BR)CEO}	60 80 100	— — —	Vdc
Collector Emitter Leakage Current (V _{CB} = 60 Vdc, R _{BE} = 1.0 k ohm) (V _{CB} = 80 Vdc, R _{BE} = 1.0 k ohm) (V _{CB} = 100 Vdc, R _{BE} = 1.0 k ohm) (V _{CB} = 60 Vdc, R _{BE} = 1.0 k ohm, T _C = 150°C) (V _{CB} = 80 Vdc, R _{BE} = 1.0 k ohm, T _C = 150°C) (V _{CB} = 100 Vdc, R _{BE} = 1.0 k ohm, T _C = 150°C)	I _{CEr}	— — — — — —	— 1.0 1.0 1.0 5.0 5.0 5.0	mA _{dc}
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	—	5.0	mA _{dc}
Collector-Emitter Leakage Current (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 40 Vdc, I _B = 0) (V _{CE} = 50 Vdc, I _B = 0)	I _{CEQ}	— — —	— 3.0 3.0 3.0	mA _{dc}
ON CHARACTERISTICS(1)				
DC Current Gain (I _C = 10 A _{dc} , V _{CE} = 3.0 Vdc)	h _{FE}	1000	—	—
Collector-Emitter Saturation Voltage (I _C = 10 A _{dc} , I _B = 40 mA _{dc}) (I _C = 16 A _{dc} , I _B = 80 mA _{dc})	V _{CE(sat)}	— —	2.5 4.0	Vdc
Base-Emitter Voltage (I _C = 10 A _{dc} , V _{CE} = 3.0 Vdc)	V _{BE}	—	3.0	Vdc

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

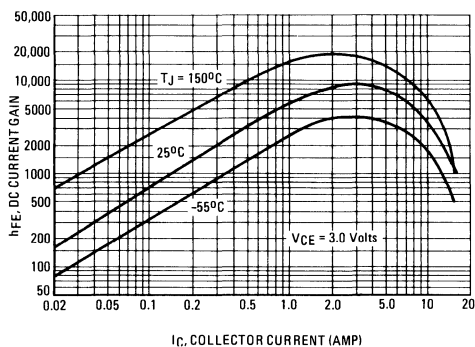


FIGURE 4 – “ON” VOLTAGES

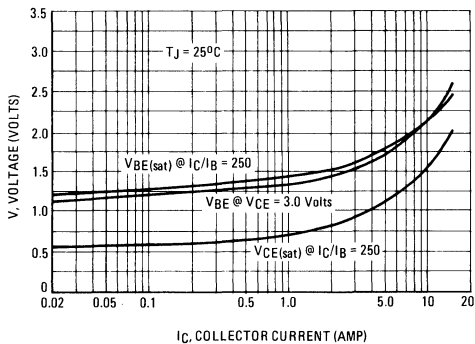


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

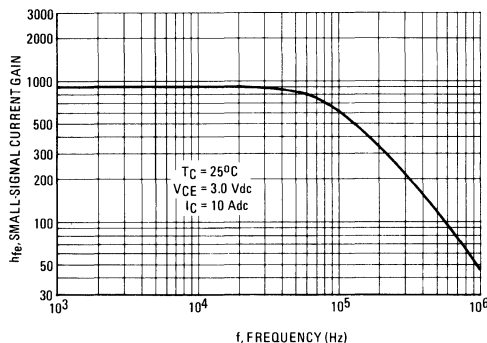
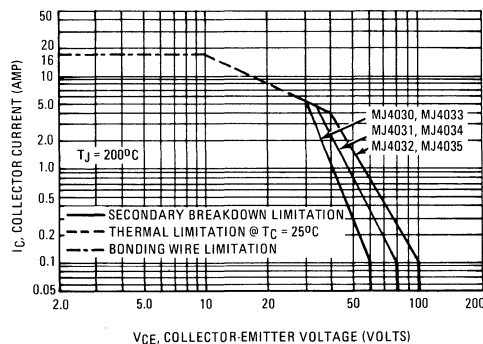


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor

must not be subjected to greater dissipation than the curves indicate. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

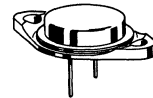
HIGH-POWER PNP SILICON TRANSISTOR

... for use as an output device in complementary audio amplifiers to 100-Watts music power per channel.

- High DC Current Gain – $h_{FE} = 25-100 @ I_C = 7.5 \text{ A}$
- Excellent Safe Operating Area
- Complement to the NPN MJ802

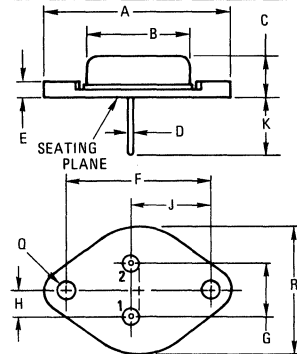
**30 AMPERE
 POWER TRANSISTOR**

PNP SILICON
100 VOLTS
200 WATTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CE}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Collector-Emitter Voltage	V_{CEO}	90	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	200 1.14	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$



STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR
 NOTE: 1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.99	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

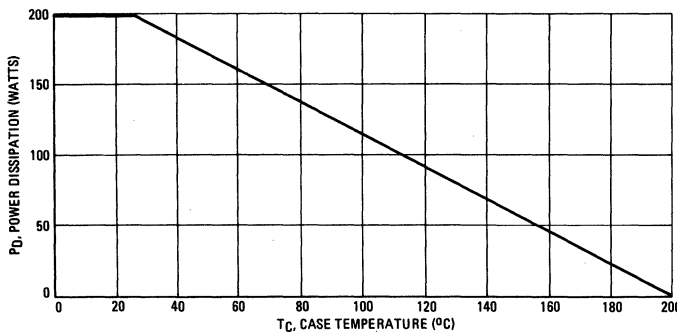
**CASE 11-01
 TO-204AA**

3

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	$^\circ\text{C}/\text{W}$

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ⁽¹⁾ ($I_C = 200\text{ mA dc}$, $R_{BE} = 100\text{ Ohms}$)	$V_{(BR)CER}$	100	—	Vdc
Collector-Emitter Sustaining Voltage ⁽¹⁾ ($I_C = 200\text{ mA dc}$)	$V_{CEO(sus)}$	90	—	Vdc
Collector-Base Cutoff Current ($V_{CB} = 100\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 100\text{ Vdc}$, $I_E = 0$, $T_C = 150^\circ\text{C}$)	I_{CBO}	—	1.0 5.0	mA dc
Emitter-Base Cutoff Current ($V_{BE} = 4.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	mA dc
ON CHARACTERISTICS ⁽¹⁾				
DC Current Gain ($I_C = 7.5\text{ A dc}$, $V_{CE} = 2.0\text{ Vdc}$)	h_{FE}	25	100	—
Base-Emitter "On" Voltage ($I_C = 7.5\text{ A dc}$, $V_{CE} = 2.0\text{ Vdc}$)	$V_{BE(on)}$	—	1.3	Vdc
Collector-Emitter Saturation Voltage ($I_C = 7.5\text{ A dc}$, $I_B = 0.75\text{ A dc}$)	$V_{CE(sat)}$	—	0.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 7.5\text{ A dc}$, $I_B = 0.75\text{ A dc}$)	$V_{BE(sat)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain - Bandwidth Product ($I_C = 1.0\text{ A dc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ MHz}$)	f_T	2.0	—	MHz

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 – DC CURRENT GAIN

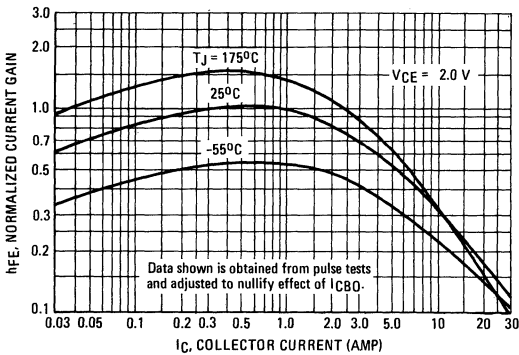


FIGURE 3 – "ON" VOLTAGES

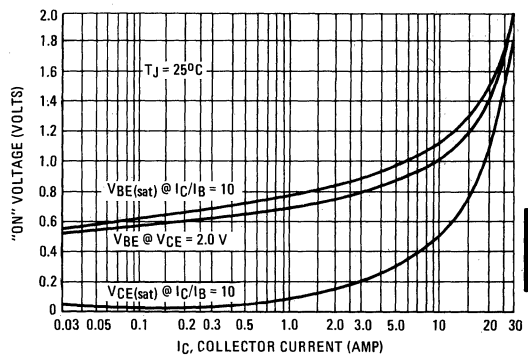
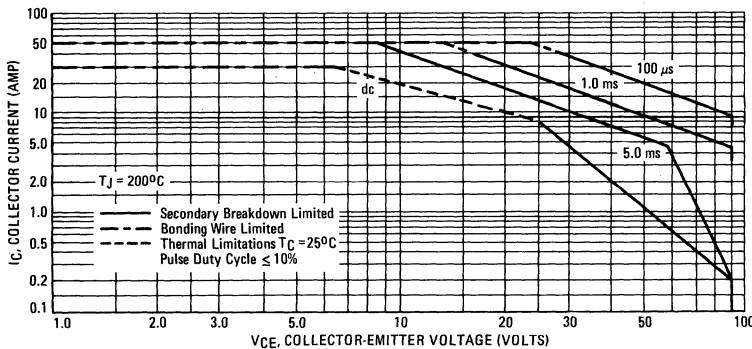


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.



MJ4646
MJ4647

PNP SILICON POWER TRANSISTORS

... designed for high-voltage amplifier and saturated switching applications at collector currents to one Ampere. Ideally suited for applications of dc-to-dc converters, relay and hammer drivers, motor controls, and servo and pulse amplifiers. High-voltage ratings permit direct-line operation.

- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = < 1.5 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$
- High Collector-Emitter Breakdown Voltage —
 $V_{(BR)CEO} = 300 \text{ and } 400 \text{ Vdc (Min)}$
- DC Current Gain Specified — 10 mAdc to 500 mAdc

1.0 AMPERE
POWER TRANSISTORS
PNP SILICON
200-300-400 VOLTS
5 WATTS

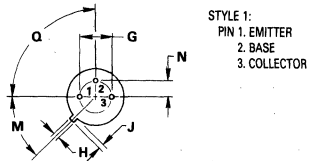
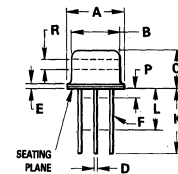


MAXIMUM RATINGS

Rating	Symbol	MJ4646	MJ4647	Unit
Collector-Emitter Voltage	V_{CEO}	300	400	Vdc
Collector-Base Voltage	V_{CB}	300	400	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	0.5	1.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	5.0	28.6	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 65 to +200		°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	θ_{JC}	35	°C/W
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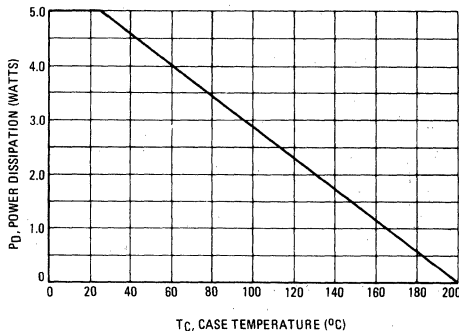
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	—	45° NOM	—	45° NOM
P	—	1.27	—	0.050
Q	—	90° NOM	—	90° NOM
R	2.54	—	0.100	—

All JEDEC Dimensions and Notes Apply.

CASE 79-02
TO-205AD

3

FIGURE 1 — POWER DERATING



MJ4646, MJ4647

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I _C = 10 mAdc, I _B = 0)	V _{(BR)CEO}	300 400	— —	— —	Vdc
Collector-Base Breakdown Voltage (I _C = 100 μAdc, I _E = 0)	V _{(BR)CBO}	300 400	— —	— —	Vdc
Emitter-Base Breakdown Voltage (I _E = 100 μAdc, I _C = 0)	V _{(BR)EBO}	5.0	—	—	Vdc
Collector Cutoff Current (V _{CE} = 200 Vdc, V _{BE(off)} = 0.5 Vdc)	I _{CEX}	—	—	10	μAdc

ON CHARACTERISTICS

DC Current Gain (I _C = 10 mAdc, V _{CE} = 10 Vdc) (I _C = 100 mAdc, V _{CE} = 10 Vdc) (1) (I _C = 500 mAdc, V _{CE} = 10 Vdc) (1)	h _{FE}	20 25 20	— — —	— — —	—
Collector-Emitter Saturation Voltage (I _C = 500 mAdc, I _B = 100 mAdc)	V _{CE(sat)}	— —	0.6 0.75	1.2 1.5	Vdc

DYNAMIC CHARACTERISTICS

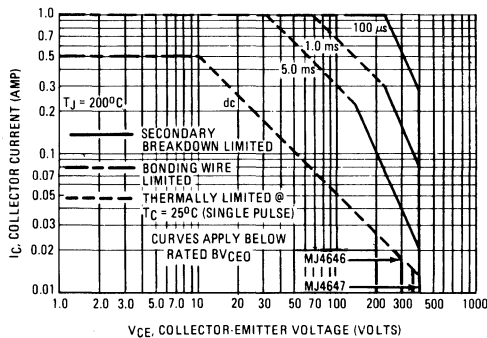
Current-Gain-Bandwidth Product (I _C = 70 mAdc, V _{CE} = 20 Vdc, f = 20 MHz)	f _T	40 30	— —	— —	MHz
Output Capacitance (V _{CB} = 20 Vdc, I _E = 0, f = 100 kHz)	C _{ob}	— —	— —	60	pF

SWITCHING CHARACTERISTICS

Delay Time	(V _{CC} = 100 Vdc, I _C = 500 mAdc,	t _d	—	—	100	ns
Rise Time	I _{B1} = 50 mAdc, V _{BE(off)} = 5.0 Vdc)	t _r	—	—	100	ns
Turn-Off Time	(V _{CC} = 100 Vdc, I _C = 500 mAdc, I _{B1} = I _{B2} = 50 mAdc, Pulse Width = 1.0 μs)	t _{off}	—	—	720	ns

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_{J(pk)} = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided T_{J(pk)} ≤ 200°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Designers Data Sheet

SWITCHMODE SERIES
PNP SILICON POWER TRANSISTOR

The MJ6503 transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

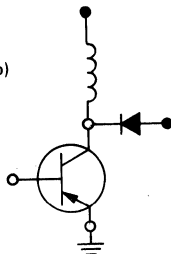
Fast Turn-Off Times

- 100 ns Inductive Fall Time @ 25°C (Typ)
- 125 ns Inductive Crossover Time @ 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



MAXIMUM RATINGS

Rating	Symbol	MJ6503	Unit
Collector-Emitter Voltage	V_{CEO}	400	Vdc
Collector-Emitter Voltage	V_{CEV}	450	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current - Continuous	I_C	8.0	Adc
Peak (1)	I_{CM}	16	
Base Current - Continuous	I_B	4.0	Adc
Peak (1)	I_{BM}	8.0	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	125	Watts
Derate above 25°C @ $T_C = 100^\circ\text{C}$		71.5	
		0.714	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

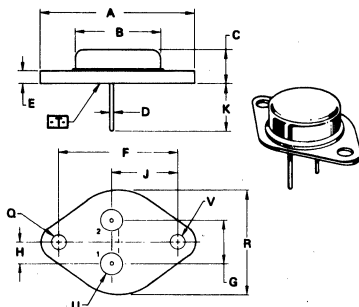
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering	T_L	275	°C
Purposes: 1/8" from Case for 5 Seconds			

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

8 AMPERE
PNP SILICON
POWER TRANSISTOR
400 VOLTS
125 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. \square IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
 $\phi \pm 0.13 (0.005) \text{ } \oplus \text{ } \square \text{ } \ominus \text{ } \square \text{ } \ominus \text{ } \square$
- FOR LEADS:
 $\phi \pm 0.13 (0.005) \text{ } \oplus \text{ } \square \text{ } \ominus \text{ } \square \text{ } \ominus \text{ } \square$
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.87	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	-	1.187 BSC	-
G	10.92 BSC	-	0.430 BSC	-
H	5.46 BSC	-	0.215 BSC	-
J	16.89 BSC	-	0.665 BSC	-
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

STYLE 1
 PIN 1: BASE
 2: EMITTER
 CASE COLLECTOR

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 10\text{ mA}$, $I_B = 0$)	$V_{CE0(sus)}$	400	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	—	—	0.5	mAdc
		—	—	2.5	
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 2.0\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	15	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 4\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 3.0\text{ Adc}$) ($I_C = 4\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	1.5	Vdc
		—	—	5.0	
		—	—	2.5	
Base-Emitter Saturation Voltage ($I_C = 4\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 4\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.5	Vdc
		—	—	1.5	

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	100	—	400	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 4.0\text{ A}$, $I_{B1} = 1.0\text{ A}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2\%$)	t_d	—	0.025	0.1	μs
Rise Time		t_r	—	0.100	0.5	μs
Storage Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 4.0\text{ A}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2\%$)	t_s	—	0.60	2.0	μs
Fall Time		t_f	—	0.11	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	$(I_C = 4\text{ A(pk)}$, $V_{CE(pk)} = 250\text{ Vdc}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	0.8	3.0	μs
Crossover Time		t_c	—	0.4	1.5	μs
Fall Time		t_{fi}	—	0.1	—	μs
Storage Time		t_{sv}	—	0.5	—	μs
Crossover Time	$(I_C = 4\text{ A(pk)}$, $V_{CE(pk)} = 250\text{ Vdc}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_c	—	0.125	—	μs
Fall Time		t_{fi}	—	0.1	—	μs

(1) Pulse Test: PW = 300 μs , Duty Cycle $\leq 2\%$



DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

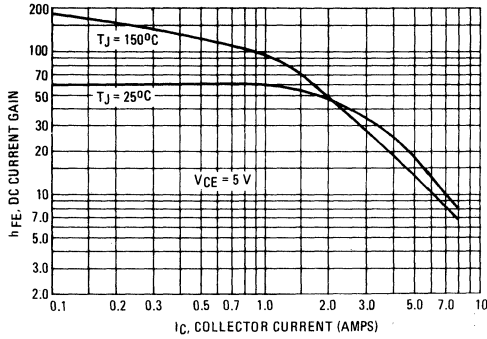


FIGURE 2 – COLLECTOR SATURATION REGION

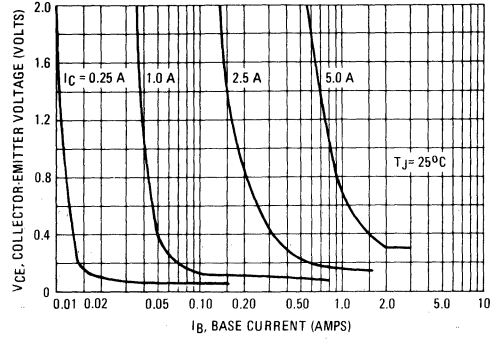


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

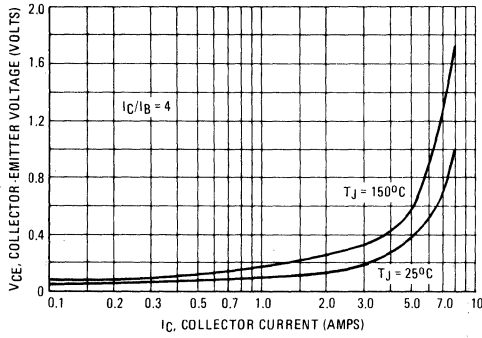


FIGURE 4 – BASE-EMITTER VOLTAGE

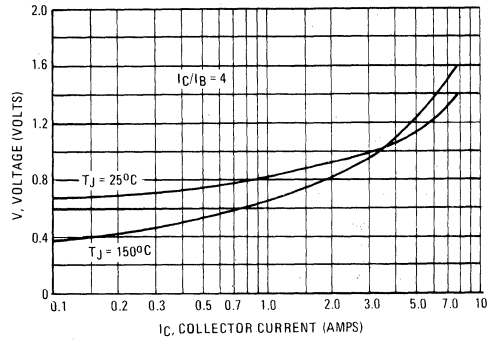


FIGURE 5 – COLLECTOR CUTOFF REGION

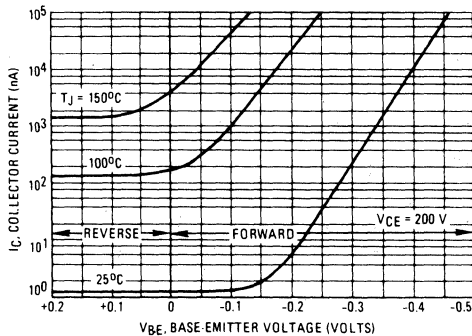
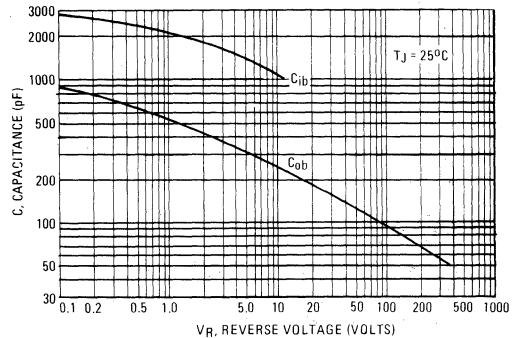


FIGURE 6 – CAPACITANCE



3

TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

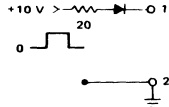
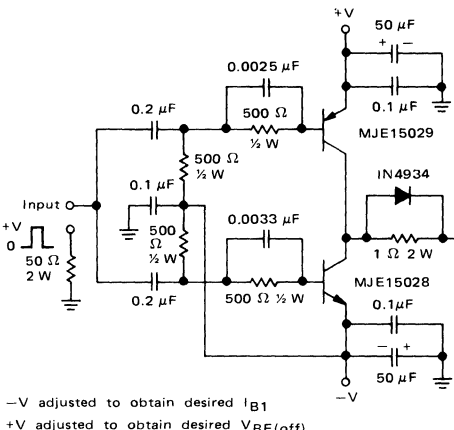
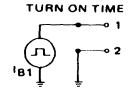
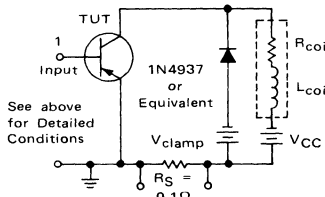
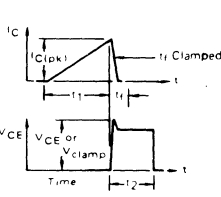
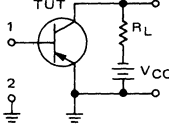
	V _{CE(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>+10 V > 20 0</p> <p>PW Varied to Attain I_C = 100 mA</p>	 <p>-V adjusted to obtain desired I_{B1} +V adjusted to obtain desired V_{BE(off)}</p>	 <p>TURN ON TIME TURN OFF TIME I_{B1} adjusted to obtain the forced h_{FE} desired Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>V_{clamp} = 250 V R_B adjusted to attain I_{B1}</p>	<p>V_{CC} = 250 V R_L = 62 Ω Pulse Width = 10 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 



FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

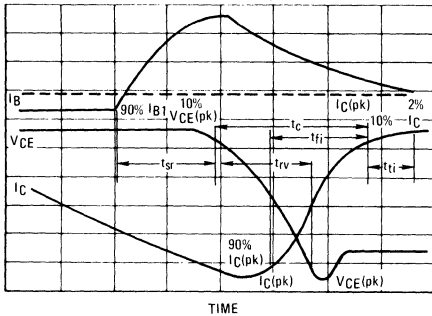
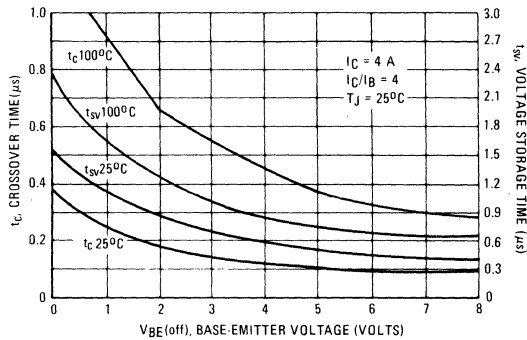


FIGURE 8 - INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$
- t_{rv} = Voltage Rise Time, 10–90% $V_{CE(pk)}$
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 9 – TURN-ON SWITCHING TIMES

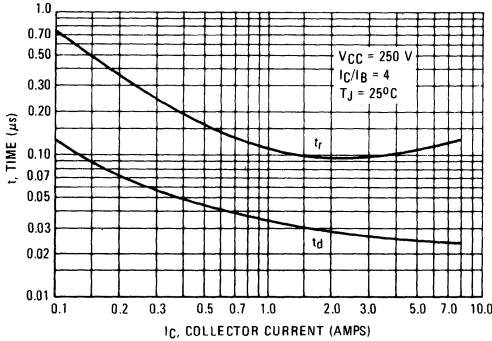


FIGURE 10 – TURN-OFF SWITCHING TIMES

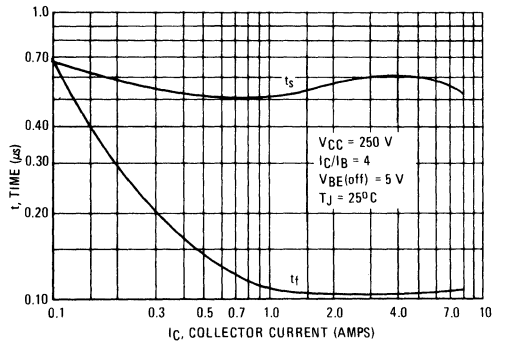
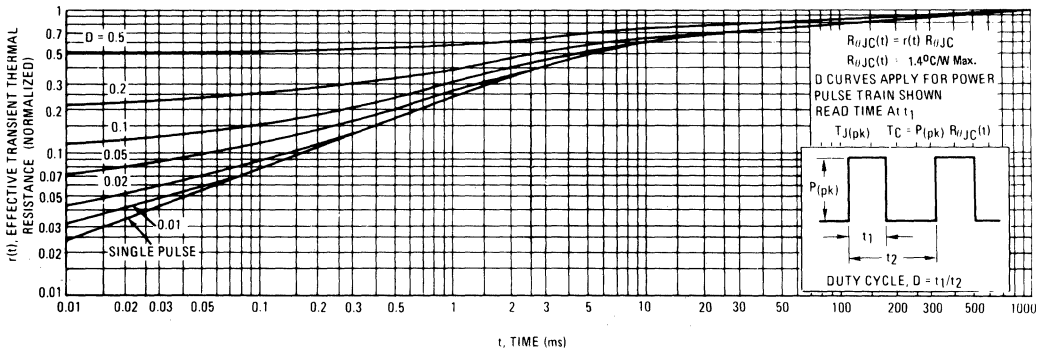


FIGURE 11 – THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

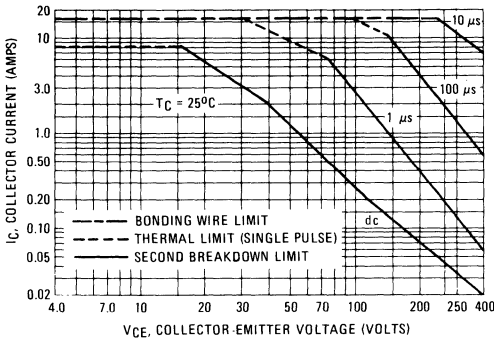


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA

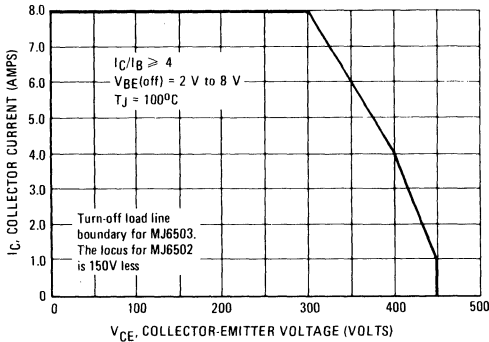
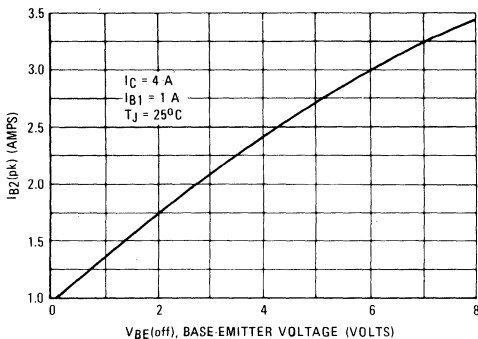


FIGURE 14 PEAK REVERSE BASE CURRENT



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

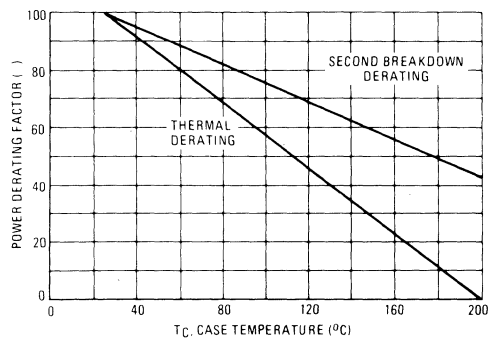
The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

FIGURE 15 POWER DERATING



MJ8501

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTOR

The MJ8501 transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

- 300 ns Inductive Fall Time – 25°C (Typ)
- 500 ns Inductive Crossover Time – 25°C (Typ)
- 900 ns Inductive Storage Time – 25°C (Typ)

Operating Temperature Range –65 to +200°C

100°C Performance Specified for:

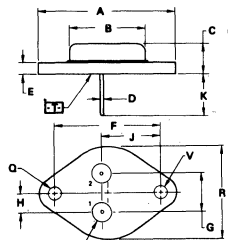
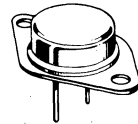
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

2.5 AMPERE
NPN SILICON
POWER TRANSISTOR

800 VOLTS
125 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
 2. [E] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q.

⊕ ±0.13 (0.005) ⊕ T V ⊕ Q ⊕

FOR LEADS:

⊕ ±0.13 (0.005) ⊕ T V ⊕ Q ⊕

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	38.37	—	1.550
B	—	21.06	—	0.830
C	6.35	7.82	0.250	0.300
D	0.87	1.09	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC	—	1.187 BSC	—
G	19.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MJ8501	Unit
Collector-Emitter Voltage	V _{CEO}	800	V _{dc}
Collector-Emitter Voltage	V _{CEV}	1400	V _{dc}
Emitter Base Voltage	V _{EB}	8.0	V _{dc}
Collector Current – Continuous	I _C	2.5	Adc
Peak (1)	I _{CM}	5.0	
Base Current – Continuous	I _B	2.0	Adc
Peak (1)	I _{RM}	4.0	
Total Power Dissipation @ T _C = 25°C	P _D	125	Watts
@ T _C = 100°C		71	
Derate above 25°C		0.71	W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.4	°C/W
Maximum Lead Temperature for Soldering	T _L	275	°C
Purposes: 1/8" from Case for 5 Seconds			

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ8501 $V_{CE0(sus)}$	800	—	—	Vdc	
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	—	—	0.25 5.0	mAdc	
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5.0	mAdc	
Emitter Cutoff Current ($V_{EB} = 7.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc	
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12				
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13				
ON CHARACTERISTICS (1)						
DC Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.5	—	—	—	
Collector-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.33\text{ Adc}$) ($I_C = 2.5\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 1.0\text{ Adc}$, $I_B = 0.33\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	2.0 5.0 3.0	Vdc	
Base-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.33\text{ Adc}$) ($I_C = 1.0\text{ Adc}$, $I_B = 0.33\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.5 1.5	Vdc	
DYNAMIC CHARACTERISTICS						
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	50	—	250	pF	
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(VCC = 500 Vdc, IC = 1.0 A, IB1 = 0.33 A, VBE(off) = 5.0 Vdc, tp = 50 μs, Duty Cycle < 2.0%)	td	—	0.045	0.20	μs
Rise Time		tr	—	0.2	2.0	μs
Storage Time		ts	—	1.0	4.0	μs
Fall Time		tf	—	0.5	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(IC = 1.0 A(pk), Vclamp = 500 Vdc, IB1 = 0.33 A, VBE(off) = 5 Vdc, TC = 100°C)	tsv	—	1.3	4.0	μs
Crossover Time		tc	—	0.6	2.0	μs
Storage Time	(IC = 1.0 A(pk), Vclamp = 500 Vdc, IB1 = 0.33 A, VBE(off) = 5 Vdc, TC = 25°C)	tsv	—	0.9	—	μs
Crossover Time		tc	—	0.5	—	μs
Fall Time		tfi	—	0.3	—	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle < 2%.



FIGURE 1 – DC CURRENT GAIN

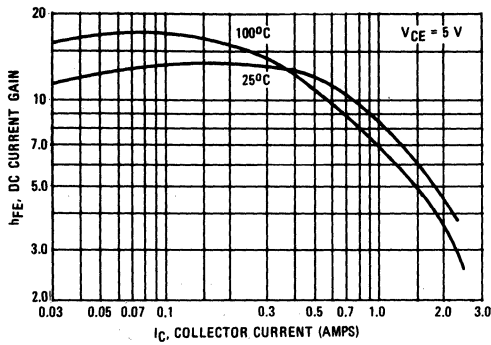


FIGURE 2 – COLLECTOR SATURATION REGION

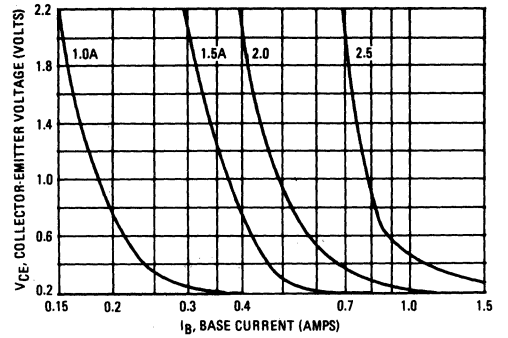


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

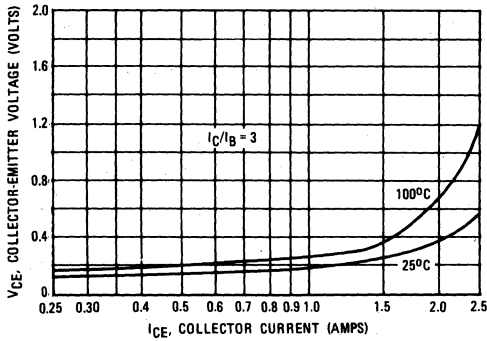


FIGURE 4 – BASE-EMITTER VOLTAGE

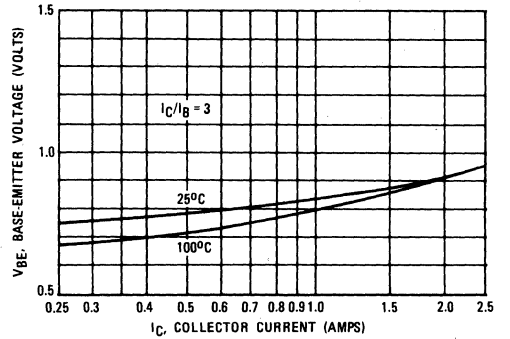


FIGURE 5 – COLLECTOR CUTOFF REGION

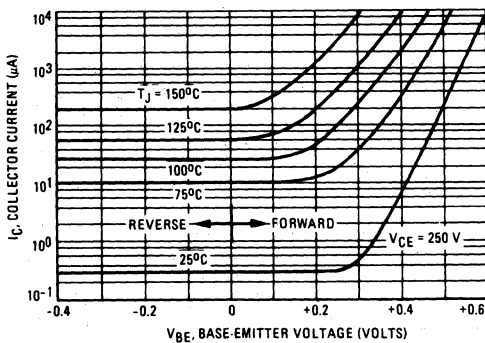
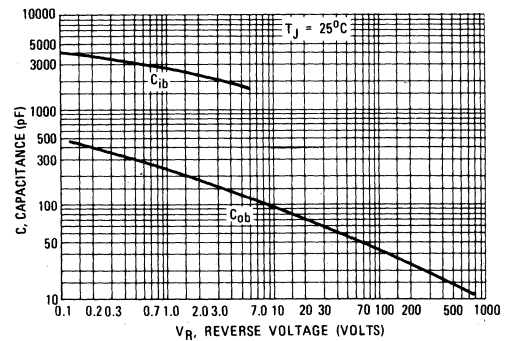


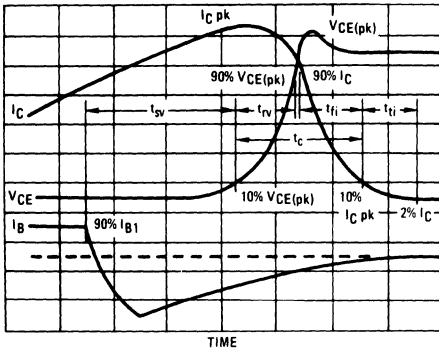
FIGURE 6 – CAPACITANCE



3

SWITCHING TIMES NOTE

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$
- t_{rv} = Voltage Rise Time, 10–90% $V_{CE(pk)}$
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

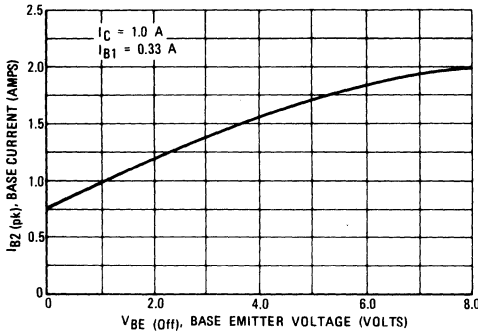
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 8 – PEAK REVERSE BASE CURRENT



RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN - ON SWITCHING TIMES

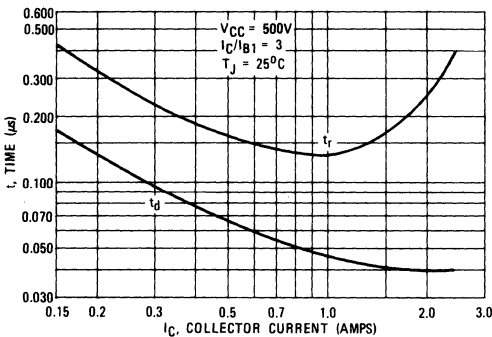


FIGURE 10 – TURN - OFF SWITCHING TIMES

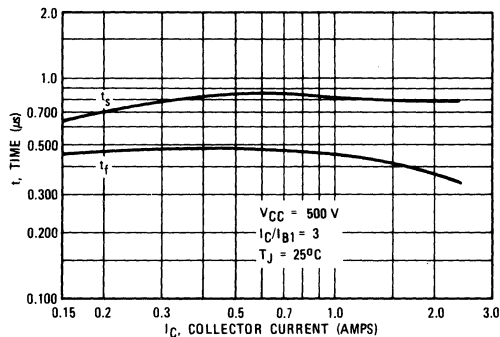
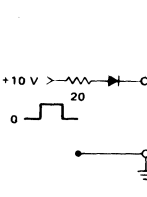
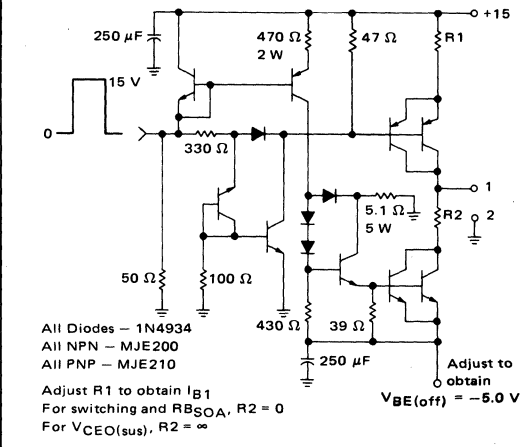
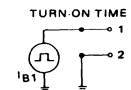
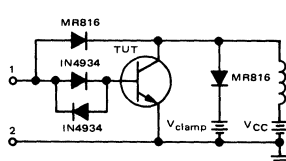
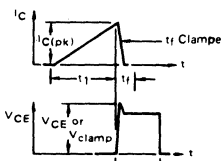
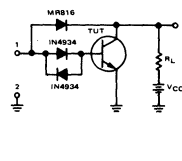


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>	 <p>All Diodes - 1N4934 All NPN - MJE200 All PNP - MJE210</p> <p>Adjust R1 to obtain I_{B1} For switching and R_{BSOA}, R2 = 0 For V_{CEO(sus)}, R2 = ∞</p> <p>Adjust to obtain V_{BE(off)} = -5.0 V</p>	 <p>TURN-ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>V_{clamp} = 500 V</p>	<p>V_{CC} = 500 V R_L = 500 Ω Pulse Width = 50 µs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> 	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

3

FIGURE 11 - THERMAL RESPONSE

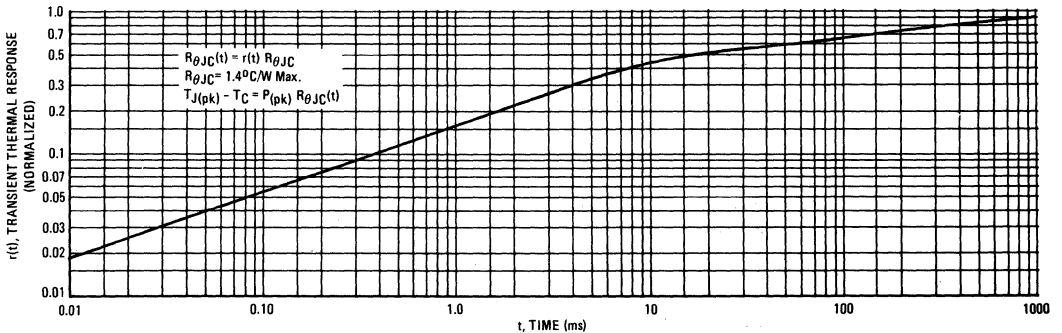


FIGURE 12 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA

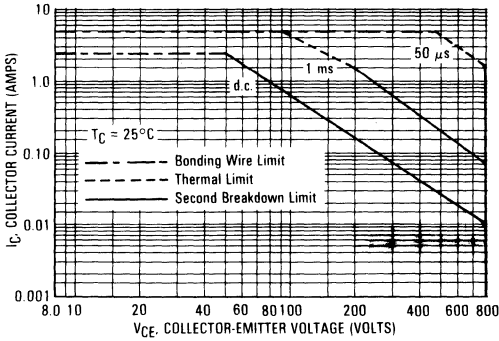


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA

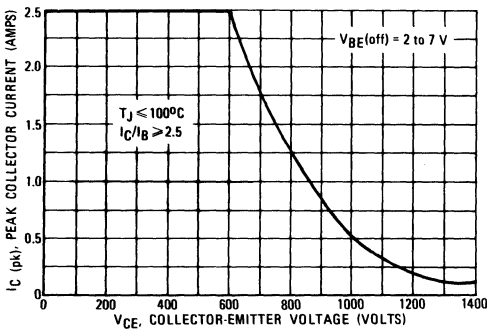
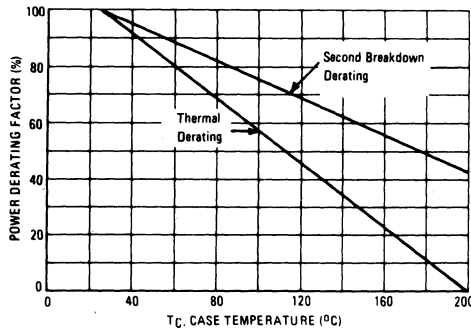


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ8502 and MJ8503 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

- 150 ns Inductive Fall Time—25°C (Typ)
- 400 ns Inductive Crossover Time—25°C (Typ)
- 1200 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range —65 to +200°C
100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

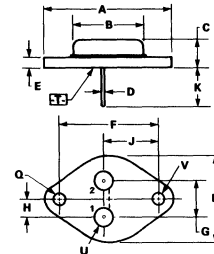
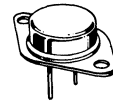
5.0 AMPERE

NPN SILICON
POWER TRANSISTORS

700 and 800 VOLTS
150 WATTS

Designer's Data for
"Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



- NOTES:
1. DIMENSIONS A AND V ARE DATUMS.
2. [T] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE:
 $\pm 0.13 (0.005) \text{ } \textcircled{M} \text{ } \textcircled{T} \text{ } \textcircled{V} \text{ } \textcircled{Q}$
FOR LEADS:
 $\pm 0.13 (0.005) \text{ } \textcircled{M} \text{ } \textcircled{T} \text{ } \textcircled{V} \text{ } \textcircled{Q} \text{ } \textcircled{Q}$
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1, BASE
2, EMITTER
CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.666 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MJ8502	MJ8503	Unit
Collector-Emitter Voltage	V_{CEO}	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous	I_C	5.0	5.0	Adc
Peak (1)	I_{CM}	10	10	
Base Current — Continuous	I_B	4.0	4.0	Adc
Peak (1)	I_{BM}	8.0	8.0	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	150	Watts
@ $T_C = 100^\circ\text{C}$		86	86	
Derate above 25°C		0.85	0.85	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.16	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ8502 MJ8503	$V_{CEO(sus)}$	700 800	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)		I_{CEV}	— —	— —	mAdc 5.0
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)		I_{CER}	—	—	5.0 mAdc
Emitter Cutoff Current ($V_{EB} = 7.0\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	—	1.0 mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12
Clamped Inductive SOA with Base Reverse Biased	RB SOA	See Figure 13

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 1.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.5	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 2.5\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 2.5\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 2.5\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 2.5\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	60	—	300	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$(V_{CC} = 500\text{ Vdc}$, $I_C = 2.5\text{ A}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.040	0.20	μs
Rise Time		t_r	—	0.125	2.0	μs
Storage Time		t_s	—	1.2	4.0	μs
Fall Time		t_f	—	0.65	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	$(I_C = 2.5\text{ A(pk)}$, $V_{clamp} = 500\text{ Vdc}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	1.6	5.0	μs
Crossover Time		t_c	—	0.60	2.0	μs
Storage Time		t_{sv}	—	1.2	—	μs
Crossover Time		t_c	—	0.4	—	μs
Fall Time		t_{fi}	—	0.15	—	μs

(1) Pulse Test: PW - 300 μs , Duty Cycle $\leq 2\%$.

FIGURE 1 – DC CURRENT GAIN

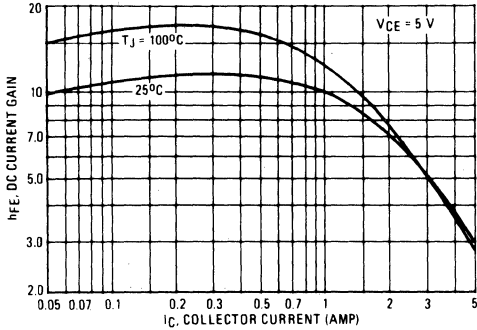


FIGURE 2 – COLLECTOR SATURATION REGION

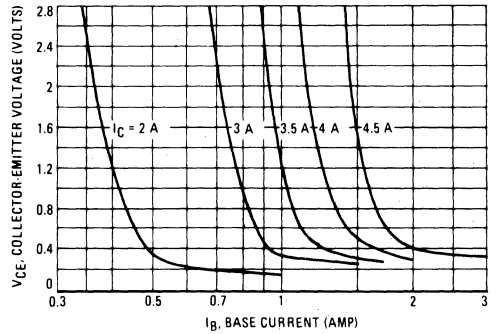


FIGURE 3 – COLLECTOR-EMITTER SATURATION REGION

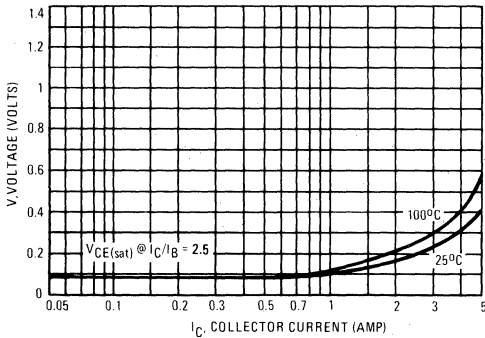


FIGURE 4 – BASE-EMITTER VOLTAGE

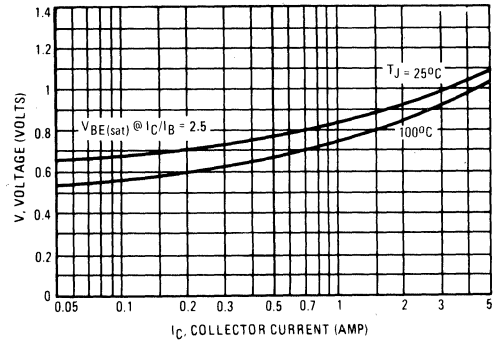


FIGURE 5 – COLLECTOR CUTOFF REGION

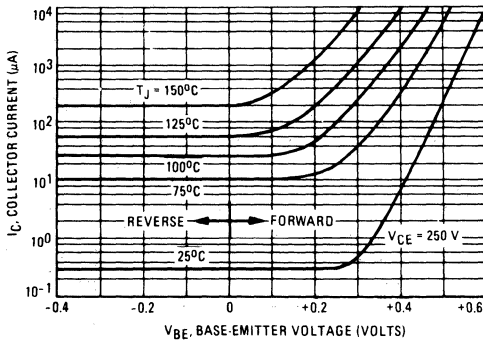
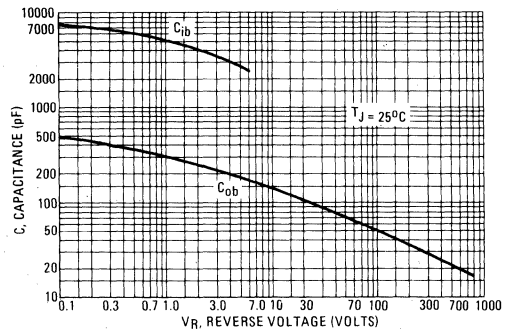


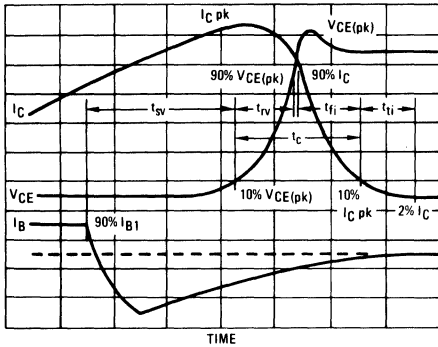
FIGURE 6 – CAPACITANCE



3

SWITCHING TIMES NOTE

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$
- t_{rv} = Voltage Rise Time, 10–90% $V_{CE(pk)}$
- t_{ff} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

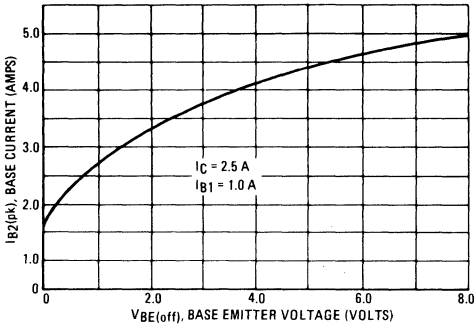
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{ff} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 8 – PEAK REVERSE BASE CURRENT



RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON SWITCHING TIMES

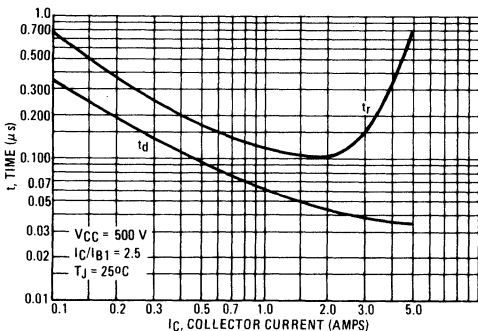


FIGURE 10 – TURN-OFF SWITCHING TIMES

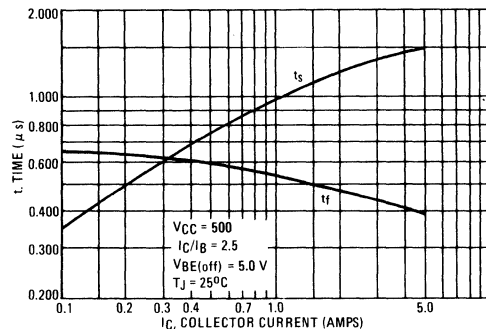
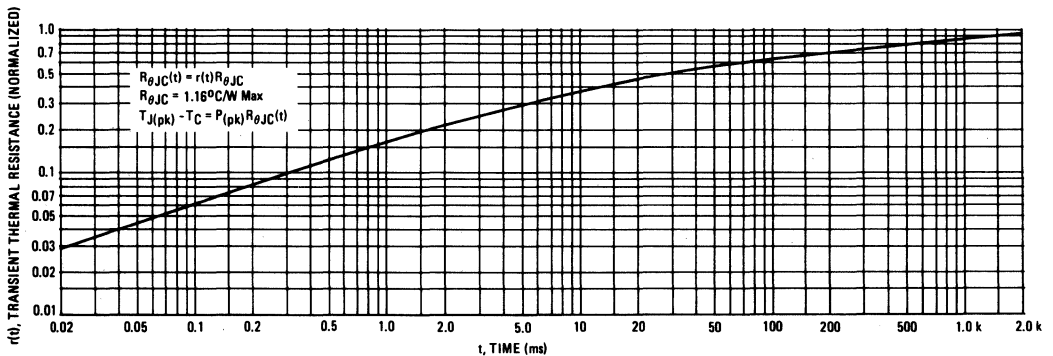


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

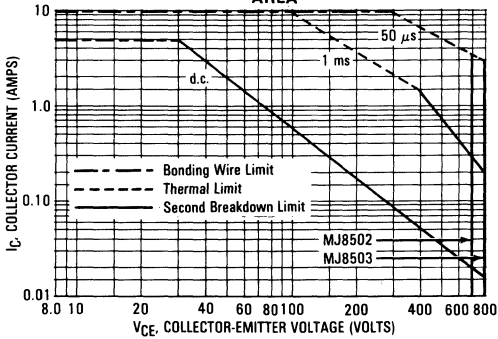
	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>+10 V \rightarrow 20 \rightarrow 1 0 \rightarrow 20 \rightarrow 2</p> <p>PW Varied to Attain $I_C = 100$ mA</p>	<p>All Diodes - 1N4934 All NPN - MJE200 All PNP - MJE210</p> <p>Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For V_{CEO(sus)}, R2 = ∞</p> <p>Adjust to obtain $V_{BE(off)} = -5.0$ V</p>	<p>TURN ON TIME I_{B1}</p> <p>I_{B1} adjusted to obtain the forced hFE desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>$L_{coil} = 80$ mH $V_{CC} = 10$ V $R_{coil} = 0.7$ Ω</p>	<p>$L_{coil} = 180$ μH $R_{coil} = 0.05$ Ω $V_{CC} = 20$ V</p> <p>$V_{clamp} = 500$ V</p>	<p>$V_{CC} = 500$ V $R_L = 200$ Ω Pulse Width = 50 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$</p> <p>$t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$</p> <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

FIGURE 11 - THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

FIGURE 12 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA



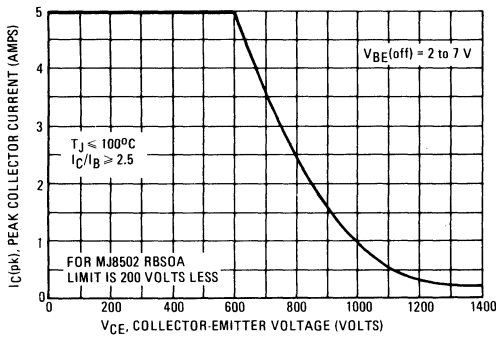
FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

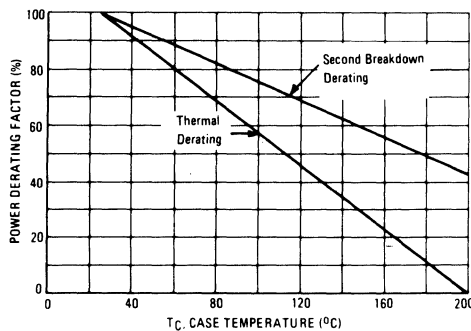
FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



MJ8504
MJ8505

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ8504 and MJ8505 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

- 75 ns Inductive Fall Time -25°C (typ)
- 150 ns Inductive Crossover Time -25°C (typ)
- 1.25 μs Inductive Storage Time -25°C (typ)

Operating Temperature Range -65 to +200°C

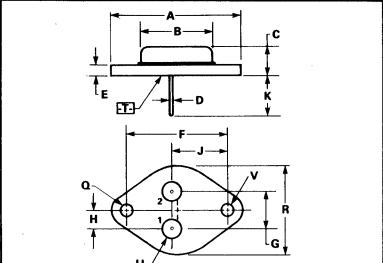
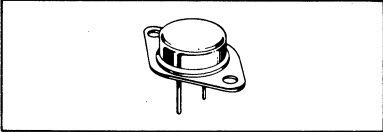
100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

10 AMPERE
NPN SILICON
POWER TRANSISTORS
 700 and 800 VOLTS
 175 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



- NOTES:
1. DIMENSIONS Q AND Y ARE DATUMS.
 2. [T] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE:
 $\pm 0.13 (0.005) \text{ } \textcircled{T} \text{ } \textcircled{V} \text{ } \textcircled{Q}$
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.
- FOR LEADS:
 $\pm 0.13 (0.005) \text{ } \textcircled{T} \text{ } \textcircled{V} \text{ } \textcircled{Q} \text{ } \textcircled{Q}$

STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	38.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.08	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MJ8504	MJ8505	Unit
Collector-Emitter Voltage	V _{CEO}	700	800	V _{dc}
Collector-Emitter Voltage	V _{CEV}	1200	1400	V _{dc}
Emitter Base Voltage	V _{EB}	8.0	8.0	V _{dc}
Collector Current - Continuous	I _C	10	10	A _{dc}
Peak (1)	I _{CM}	15	15	A _{dc}
Base Current - Continuous	I _B	8	8	A _{dc}
Peak (1)	I _{BM}	12	12	A _{dc}
Total Power Dissipation @ T _C = 25°C	P _D	175	175	Watts
@ T _C = 100°C		100	100	
Derate above 25°C		1.0	1.0	W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.0	°C/W
Maximum Lead Temperature for Soldering	T _L	275	°C
Purposes: 1/8" from Case for 5 Seconds			

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ8504 MJ8505	$V_{CEO(sus)}$	700 800	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)		I_{CEV}	— —	— 0.25 5.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)		I_{CER}	—	—	5.0 mAdc
Emitter Cutoff Current ($V_{EB} = 7.0\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	—	1.0 mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 1.5\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.5	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 4.0\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 2.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	90	—	450	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)					
Delay Time	$(V_{CC} = 500\text{ Vdc}$, $I_C = 5.0\text{ A}$, $I_{B1} = 2.0\text{ A}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.050	0.20 μs
Rise Time		t_r	—	0.175	2.0 μs
Storage Time		t_s	—	1.25	4.0 μs
Fall Time		t_f	—	0.60	2.0 μs
Inductive Load, Clamped (Table 1)					
Storage Time	$(I_C = 5.0\text{ A(pk)}$, $V_{clamp} = 500\text{ Vdc}$, $I_{B1} = 2.0\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	1.75	5.5 μs
Crossover Time		t_c	—	0.400	2.0 μs
Storage Time	$(I_C = 5.0\text{ A(pk)}$, $V_{clamp} = 500\text{ Vdc}$, $I_{B1} = 2.0\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_{sv}	—	1.25	— μs
Crossover Time		t_c	—	0.150	— μs
Fall Time		t_{fi}	—	0.075	— μs

(1) Pulse Test: PW - 300 μs , Duty Cycle $\leq 2\%$.

FIGURE 1 – DC CURRENT GAIN

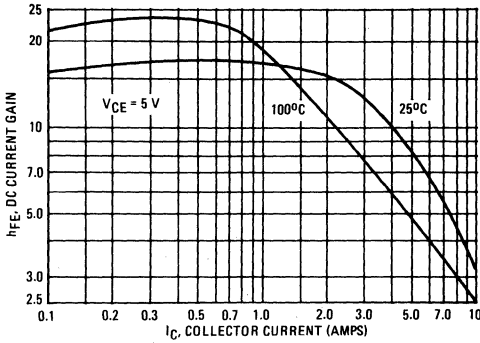


FIGURE 2 – COLLECTOR SATURATION REGION

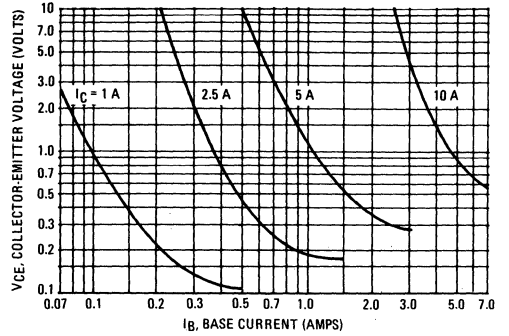


FIGURE 3 – COLLECTOR-EMITTER SATURATION REGION

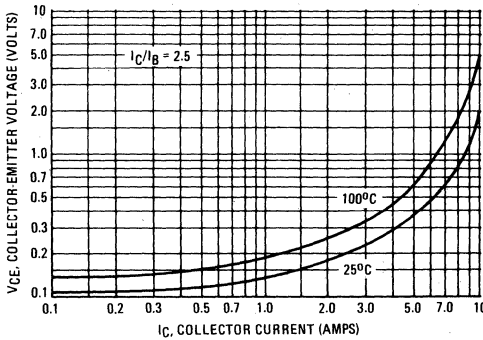


FIGURE 4 – BASE-EMITTER VOLTAGE

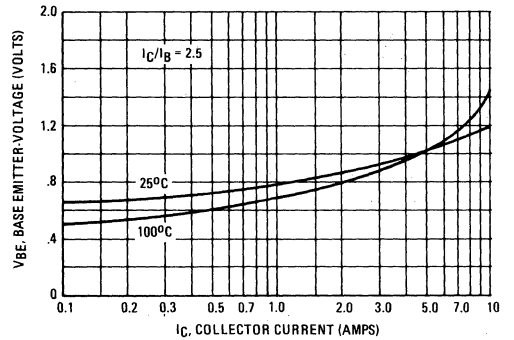


FIGURE 5 – COLLECTOR CUTOFF REGION

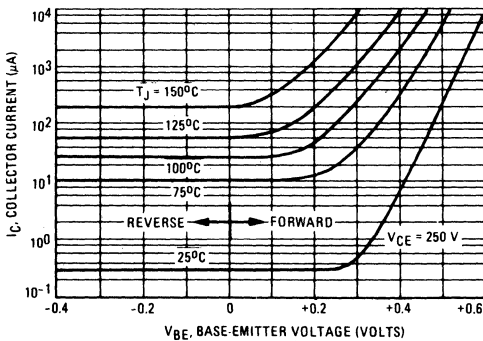
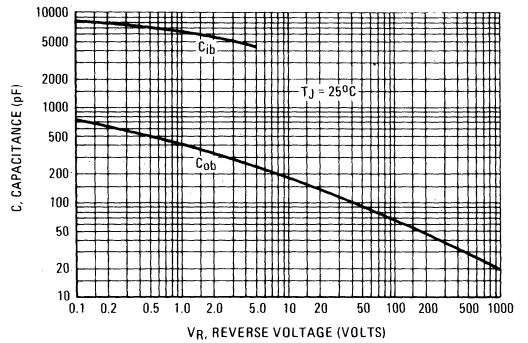


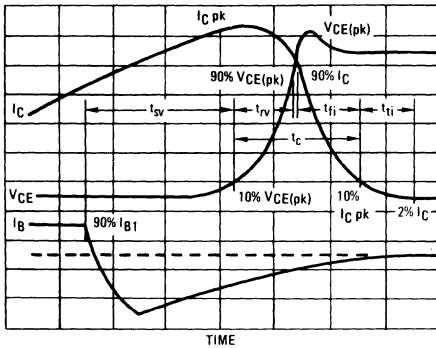
FIGURE 6 – CAPACITANCE



3

SWITCHING TIMES NOTE

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In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

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- t_{rv} = Voltage Rise Time, 10–90% $V_{CE}(pk)$
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% $V_{CE}(pk)$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

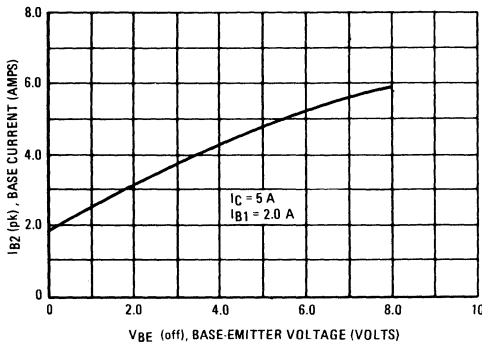
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$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 8 – PEAK REVERSE BASE CURRENT



RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON SWITCHING TIMES

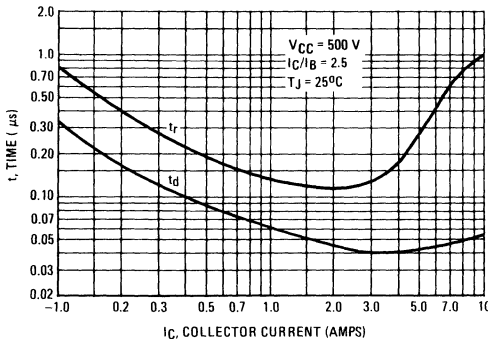


FIGURE 10 – TURN-OFF SWITCHING TIMES

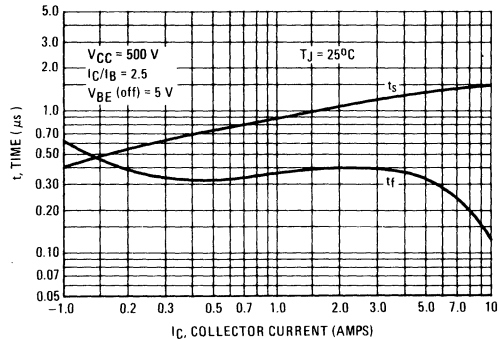
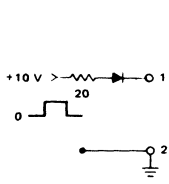
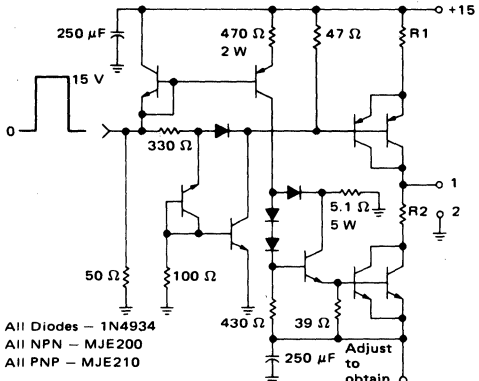
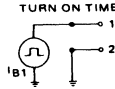
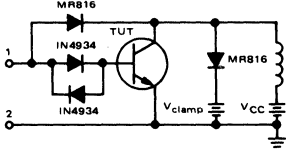
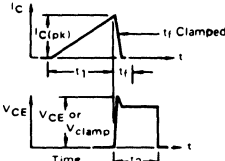
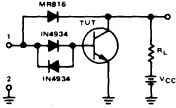
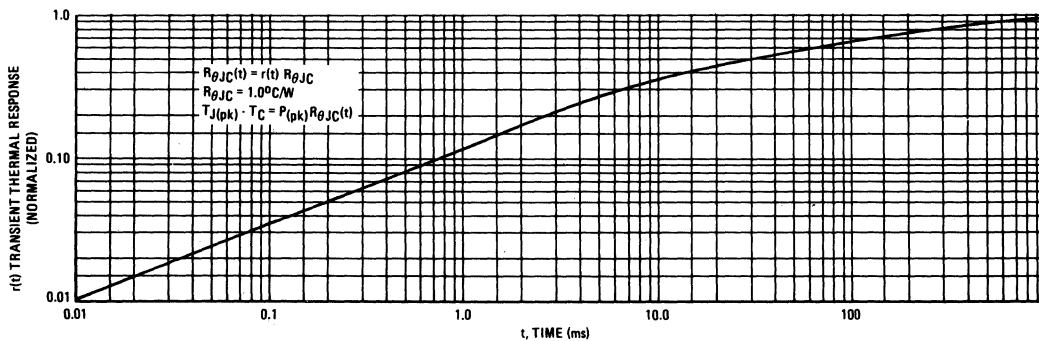


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CE0(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
<p>INPUT CONDITIONS</p>  <p>PW Varied to Attain $I_C = 100 \text{ mA}$</p>		 <p>All Diodes - 1N4934 All NPN - MJE200 All PNP - MJE210</p> <p>Adjust R1 to obtain I_{B1} For switching and RBSOA, $R_2 = 0$ For $V_{CE0(sus)}$, $R_2 = \infty$</p>	 <p>TURN ON TIME I_{B1}</p> <p>I_{B1} adjusted to obtain the forced hFE desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
<p>CIRCUIT VALUES</p> <p>$L_{coil} = 80 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$</p>		<p>$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$</p> <p>$V_{clamp} = 500 \text{ V}$</p>	<p>$V_{CC} = 500 \text{ V}$ $R_L = 100 \Omega$ Pulse Width = $50 \mu\text{s}$</p>
<p>TEST CIRCUITS</p>	<p>INDUCTIVE TEST CIRCUIT</p> 	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$</p> <p>$t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$</p> <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

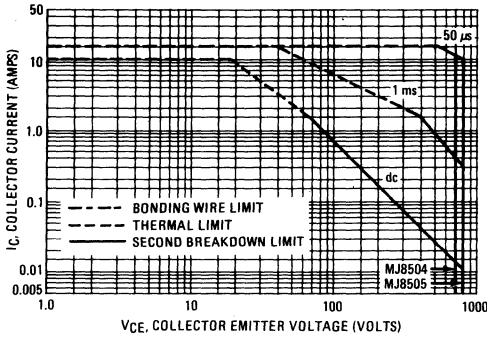
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FIGURE 11 - THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA



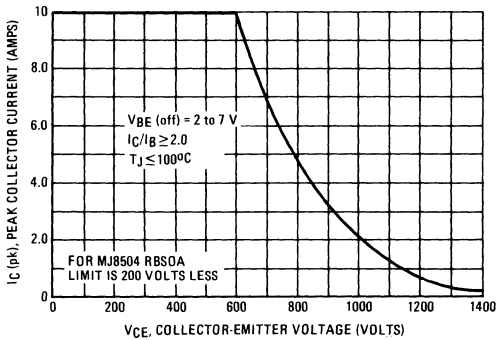
FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

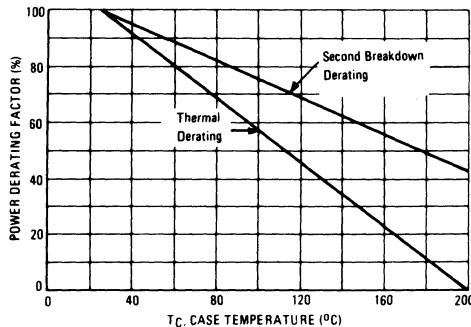
FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



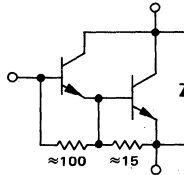
Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10000 and MJ10001 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

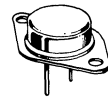
100°C Performance Specified for:
 Reversed Biased SOA with Inductive Loads
 Switching Times With Inductive Loads —
 210 ns Inductive Fall Time (Typ)
 Saturation Voltages
 Leakage Currents



20 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
350 and 400 VOLTS
175 WATTS

Designer's Data for
"Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



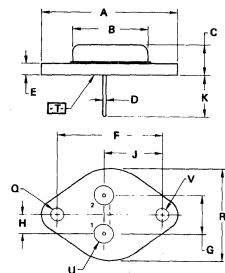
MAXIMUM RATINGS

Rating	Symbol	MJ10000	MJ10001	Unit
Collector-Emitter Voltage	V_{CEO}	350	400	Vdc
Collector-Emitter Voltage	V_{CEX}	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous	I_C	20		A dc
— Peak (1)	I_{CM}	30		
Base Current — Continuous	I_B	2.5		A dc
— Peak (1)	I_{BM}	5		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	P_D	175		Watts
Derate above 25°C		100		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	38.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	6.46 BSC		0.215 BSC	
J	15.88 BSC		0.625 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	26.67		1.050	
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 250\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	$V_{\text{CEO(sus)}}$	350 400	— —	— —	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) $I_C = 2\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^{\circ}\text{C}$	$V_{\text{CEX(sus)}}$	400 450 275 325	— — — —	— — — —	Vdc
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$) ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$, $T_C = 150^{\circ}\text{C}$)	I_{CEV}	— —	— —	0.25 5	mAdc
Collector Cutoff Current ($V_{\text{CE}} = \text{Rated } V_{\text{CEV}}$, $R_{\text{BE}} = 50\ \Omega$, $T_C = 100^{\circ}\text{C}$)	I_{CER}	—	—	5	mAdc
Emitter Cutoff Current ($V_{\text{EB}} = 8\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	150	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{\text{S/b}}$	See Figure 11			Adc
ON CHARACTERISTICS (2)					
DC Current Gain ($I_C = 5\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$)	h_{FE}	50 40	— —	600 400	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$) ($I_C = 20\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$, $T_C = 100^{\circ}\text{C}$)	$V_{\text{CE(sat)}}$	— — —	— — —	1.9 3 2	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$) ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$, $T_C = 100^{\circ}\text{C}$)	$V_{\text{BE(sat)}}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage (1) ($I_F = 10\text{ Adc}$)	V_f	—	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 1.0\text{ Adc}$, $V_{\text{CE}} = 10\text{ Vdc}$, $f_{\text{test}} = 1\text{ MHz}$)	$ h_{\text{fe}} $	10	—	—	—
Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	100	—	325	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time ($V_{\text{CC}} = 250\text{ Vdc}$, $I_C = 10\text{ A}$,	t_d	—	0.12	0.2	μs
Rise Time $I_{\text{B1}} = 400\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $t_p = 50\ \mu\text{s}$,	t_r	—	0.20	0.6	μs
Storage Time Duty Cycle $\leq 2\%$.)	t_s	—	1.5	3.5	μs
Fall Time	t_f	—	1.1	2.4	μs
Inductive Load, Clamped (Table 1)					
Storage Time ($I_C = 10\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 400\text{ mA}$,	t_{sv}	—	3.5	5.5	μs
Crossover Time $V_{\text{BE(off)}} = 5\text{ Vdc}$, $T_C = 100^{\circ}\text{C}$)	t_c	—	1.5	3.7	μs
Storage Time ($I_C = 10\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 400\text{ mA}$,	t_{sv}	—	1.0	—	μs
Crossover Time $V_{\text{BE(off)}} = 5\text{ Vdc}$, $T_C = 25^{\circ}\text{C}$)	t_c	—	0.7	—	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

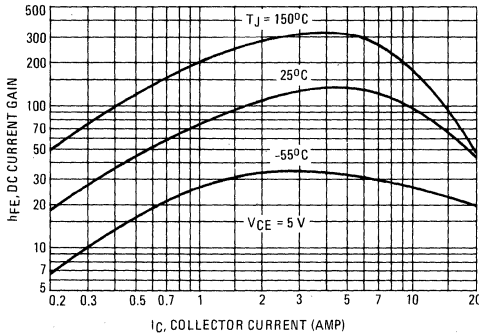


FIGURE 2 – COLLECTOR SATURATION REGION

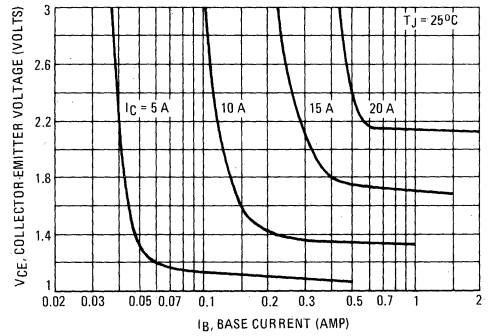


FIGURE 3 – COLLECTOR EMITTER SATURATION VOLTAGES

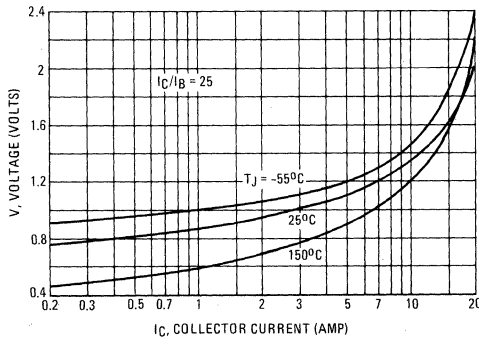


FIGURE 4 – BASE-EMITTER VOLTAGE

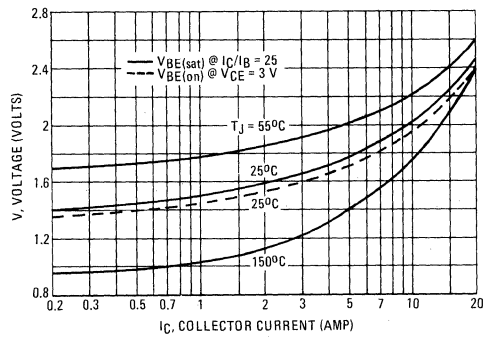


FIGURE 5 – COLLECTOR CUTOFF REGION

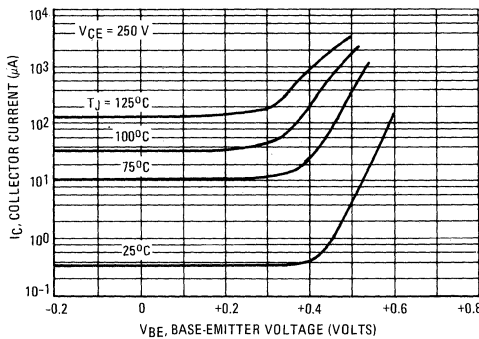
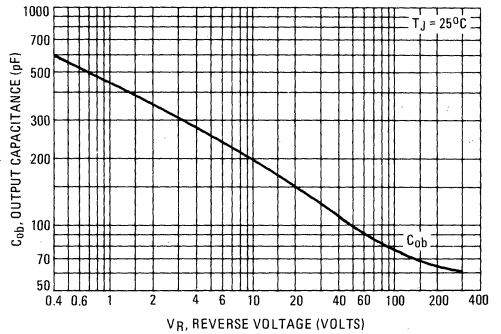
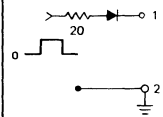
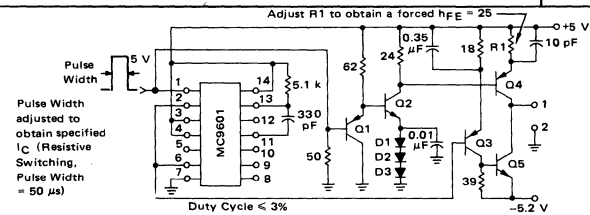
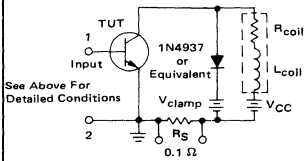
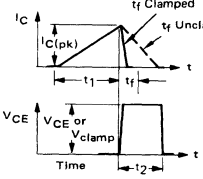
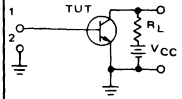


FIGURE 6 – OUTPUT CAPACITANCE



3

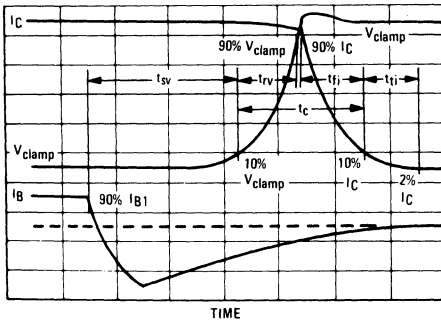
TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CE0(sus)}	V _{CEX(sus)} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 250 mA</p>	 <p>Duty Cycle ≤ 3%</p>	<p>Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914</p>
CIRCUIT VALUES	<p>L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = V_{CE0(sus)}</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value</p>	<p>V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above For Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope-Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

SWITCHING TIMES NOTE



FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fj} = Current Fall Time, 90–10% I_C
- t_{tj} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

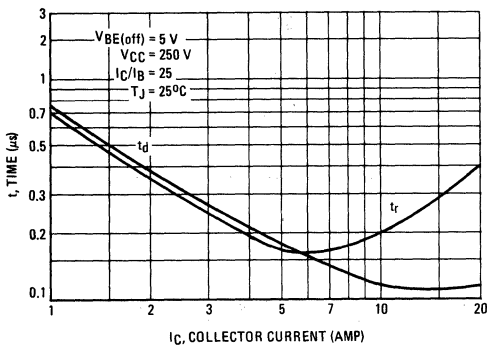


FIGURE 9 – TURN-OFF TIME

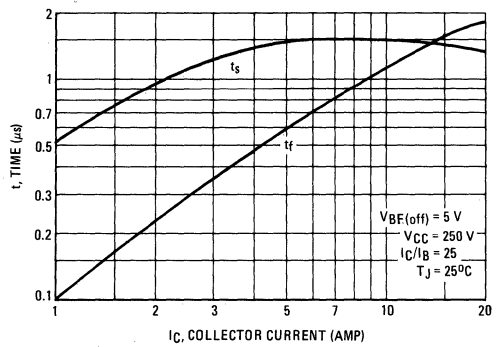
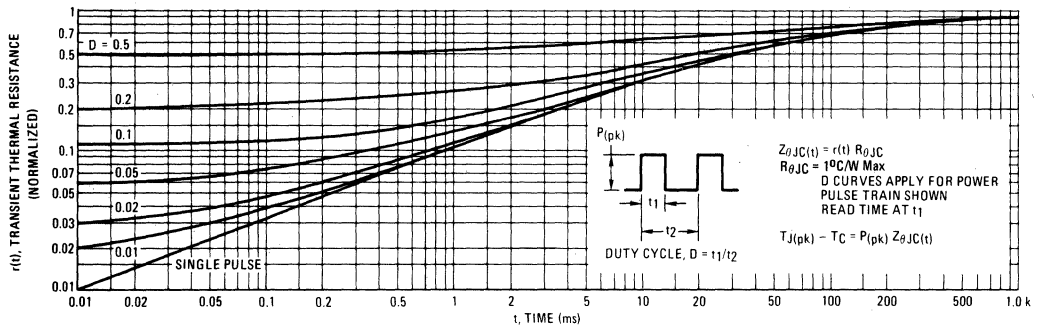


FIGURE 10 – THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

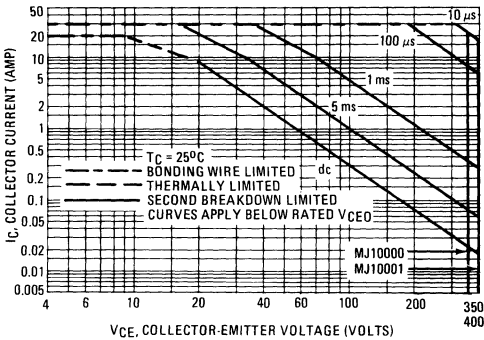


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA

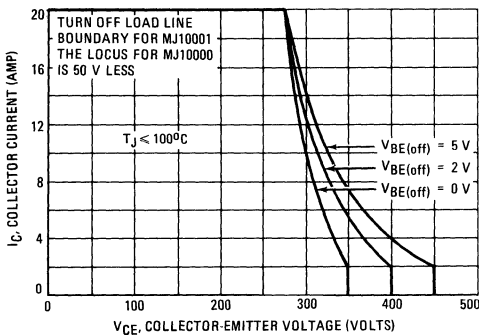
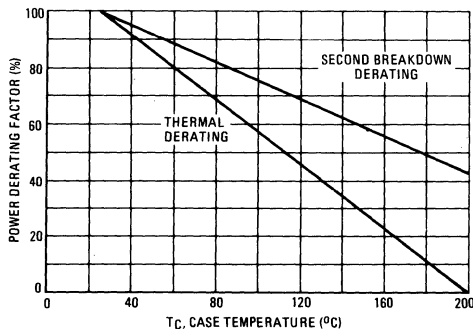


FIGURE 13 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(\text{sus})}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

Designers Data Sheet

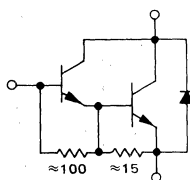
SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10002 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

100°C Performance Specified for:

- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads – 140 ns Inductive Fall Time (Typ)
- Saturation Voltages
- Leakage Currents



10 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS

350 VOLTS
150 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

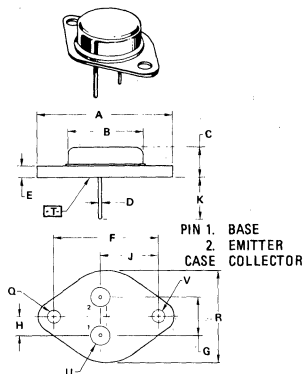
MAXIMUM RATINGS

Rating	Symbol	MJ10002	Unit
Collector-Emitter Voltage	V _{CEO}	350	Vdc
Collector-Emitter Voltage	V _{CEX}	400	Vdc
Collector-Emitter Voltage	V _{CEV}	450	Vdc
Emitter Base Voltage	V _{EB}	8.0	Vdc
Collector Current – Continuous	I _C	10	Adc
Collector Current – Peak (1)	I _{CM}	20	
Base Current – Continuous	I _B	2.5	Adc
Base Current – Peak (1)	I _{BM}	5.0	
Total Power Dissipation @ T _C = 25°C	P _D	150	Watts
@ T _C = 100°C		100	
Derate above 25°C		0.86	W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. [E] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
 ⌀ .13 (0.005) M T V Q
 FOR LEADS:
 ⌀ .13 (0.005) M T V Q Q Q
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.08	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15	BSC	1.187	BSC
G	10.92	BSC	0.430	BSC
H	5.46	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.13	0.440	0.480
Q	3.81	4.18	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.18	0.150	0.165

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS (2)						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 250\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$) MJ10002	$V_{\text{CEO(sus)}}$	350	–	–	Vdc	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) ($I_C = 1.0\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$) MJ10002	$V_{\text{CEX(sus)}}$	400	–	–	Vdc	
($I_C = 5.0\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$) MJ10002		275	–	–		
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$) ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	–	–	0.25 5.0	mAdc	
Collector Cutoff Current ($V_{\text{CE}} = \text{Rated } V_{\text{CEV}}$, $R_{\text{BE}} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	–	–	5.0	mAdc	
Emitter Cutoff Current ($V_{\text{EB}} = 8.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	–	175	mAdc	
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased	$I_{\text{S/b}}$	See Figure 11			Adc	
ON CHARACTERISTICS (2)						
DC Current Gain ($I_C = 2.5\text{ Adc}$, $V_{\text{CE}} = 5.0\text{ Vdc}$) ($I_C = 5.0\text{ Adc}$, $V_{\text{CE}} = 5.0\text{ Vdc}$)	h_{FE}	40 30	– –	500 300	–	
Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 250\text{ mA}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 250\text{ mA}$, $T_C = 100^\circ\text{C}$)	$V_{\text{CE(sat)}}$	– – –	– – –	1.9 2.9 2.0	Vdc	
Base-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 250\text{ mA}$) ($I_C = 5.0\text{ Adc}$, $I_B = 250\text{ mA}$, $T_C = 100^\circ\text{C}$)	$V_{\text{BE(sat)}}$	– –	– –	2.5 2.5	Vdc	
Diode Forward Voltage (1) ($I_F = 5.0\text{ Adc}$)	V_f	–	3.0	5.0	Vdc	
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain ($I_C = 1.0\text{ Adc}$, $V_{\text{CE}} = 10\text{ Vdc}$, $f_{\text{test}} = 1.0\text{ MHz}$)	$ h_{\text{fe}} $	10	–	–	–	
Output Capacitance ($V_{\text{CB}} = 50\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	60	–	275	pF	
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	$(V_{\text{CC}} = 250\text{ Vdc}$, $I_C = 5.0\text{ A}$, $I_{\text{B1}} = 250\text{ mA}$, $V_{\text{BE(off)}} = 5.0\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$).	t_d	–	0.05	0.2	μs
Rise Time		t_r	–	0.25	0.6	μs
Storage Time		t_s	–	1.2	3.0	μs
Fall Time		t_f	–	0.6	1.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	$(I_C = 5.0\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 250\text{ mA}$, $V_{\text{BE(off)}} = 5.0\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	–	2.1	5.0	μs
Crossover Time		t_c	–	1.3	3.3	μs
Storage Time	$(I_C = 5.0\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 250\text{ mA}$, $V_{\text{BE(off)}} = 5.0\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_{sv}	–	0.92	–	μs
Crossover Time		t_c	–	0.5	–	μs



- (1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.
- (2) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

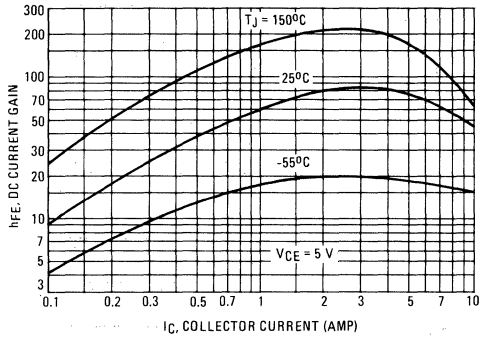


FIGURE 2 – COLLECTOR SATURATION REGION

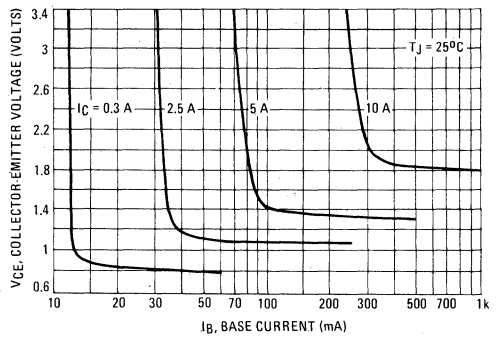


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

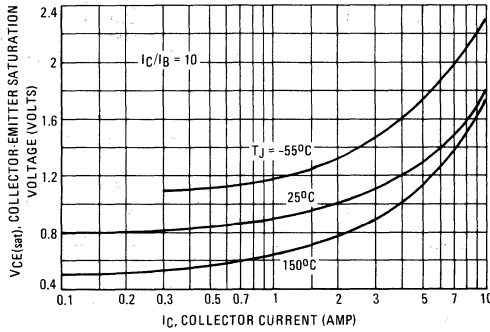


FIGURE 4 – BASE-EMITTER VOLTAGE

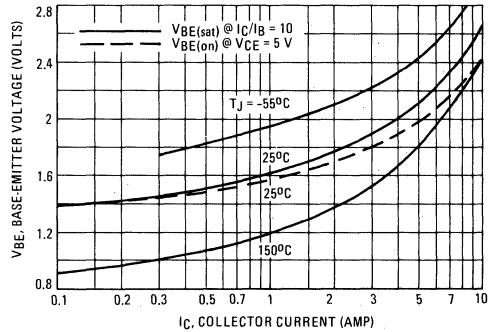


FIGURE 5 – COLLECTOR CUT-OFF REGION

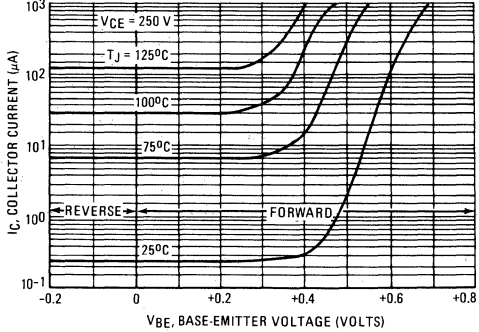
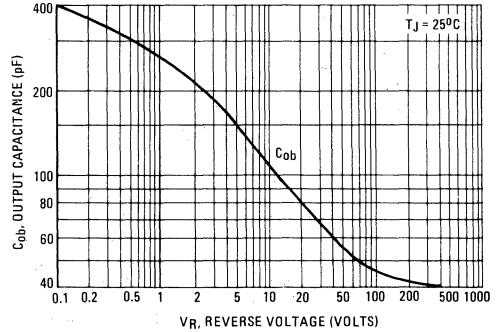


FIGURE 6 – OUTPUT CAPACITANCE



3

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

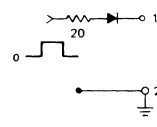
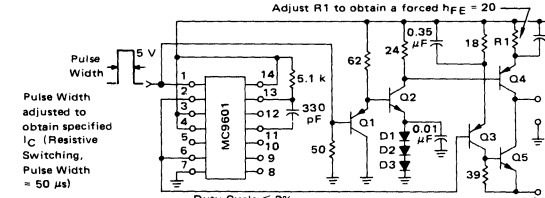
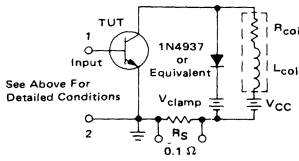
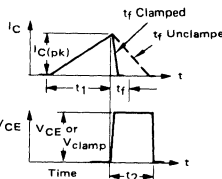
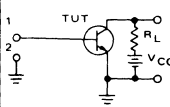
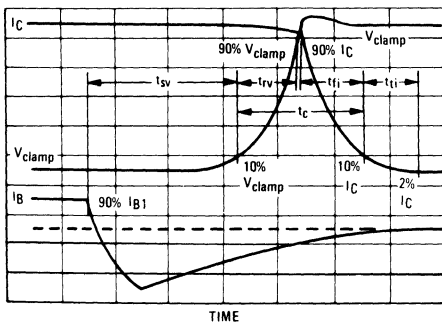
INPUT CONDITIONS	V _{CE0(sus)}	RESISTIVE SWITCHING
 <p>PW Varied to Attain I_C = 250 mA</p>	<p>V_{CE0(sus)} AND INDUCTIVE SWITCHING</p>  <p>Duty Cycle ≤ 3%</p>	<p>RESISTIVE SWITCHING</p> <p>Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914</p>
<p>CIRCUIT VALUES</p> <p>L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = V_{CE0(sus)}</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value</p>	<p>V_{CC} = 250 V R_L = 50 Ω Pulse Width = 50 μs</p>
<p>TEST CIRCUITS</p> <p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above For Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 = \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 = \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope-Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fj} = Current Fall Time, 90–10% I_C
- t_{tj} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

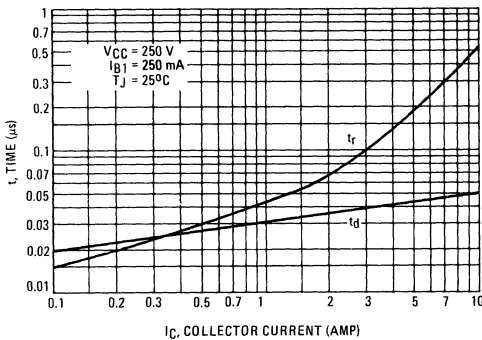


FIGURE 9 – TURN-OFF TIME

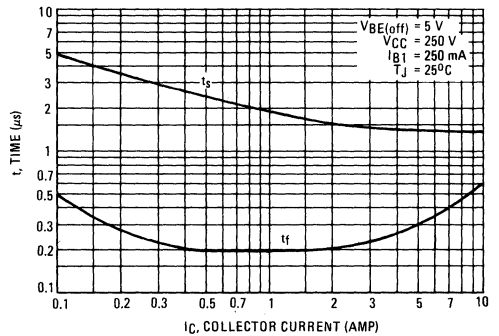
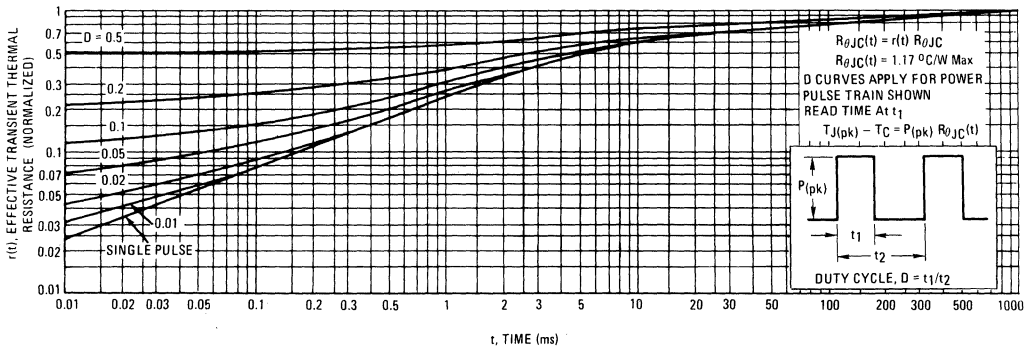


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – ACTIVE-REGION SAFE OPERATING AREA

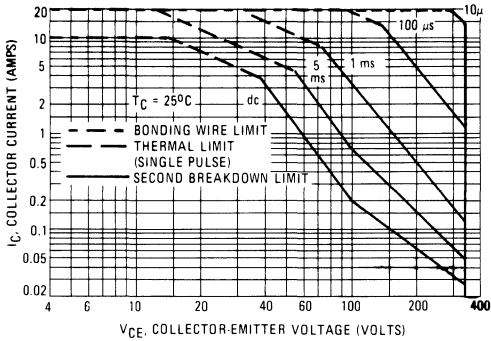
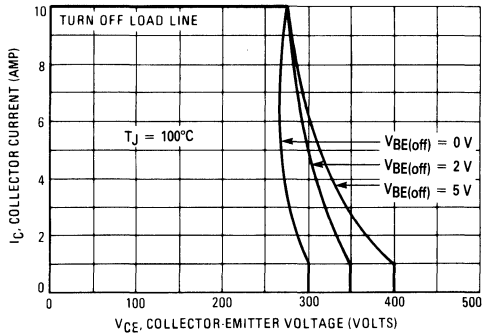


FIGURE 12 – REVERSE BIASED SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

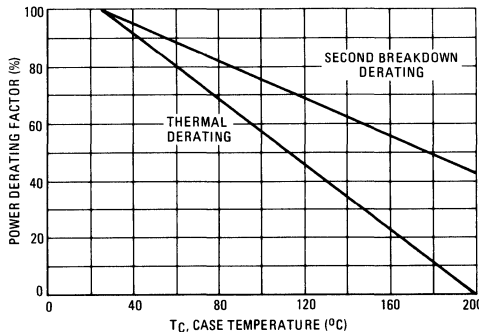
The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



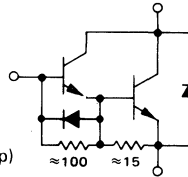
Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The MJ10004 and MJ10005 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
 - Inverters
 - Solenoid and Relay Drivers
 - Motor Controls
 - Deflection Circuits
- Fast Turn-Off Times

40 ns Inductive Fall Time - 25°C (Typ)
 650 ns Inductive Storage Time - 25°C (Typ)
 Operating Temperature Range -65 to +200°C
 100°C Performance Specified for:
 Reversed Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents



20 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS

350 and 400 VOLTS
175 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.

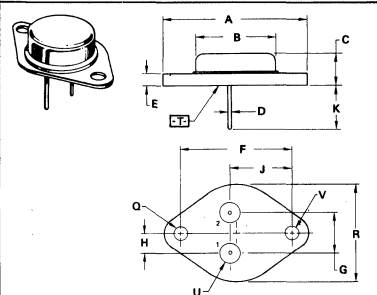
MAXIMUM RATINGS

Rating	Symbol	MJ10004	MJ10005	Unit
Collector-Emitter Voltage	V _{CEO}	350	400	Vdc
Collector-Emitter Voltage	V _{CEX}	400	450	Vdc
Collector-Emitter Voltage	V _{CEV}	450	500	Vdc
Emitter Base Voltage	V _{EB}		8.0	Vdc
Collector Current - Continuous	I _C	20		Adc
- Peak (1)	I _{CM}	30		
Base Current - Continuous	I _B	2.5		Adc
- Peak (1)	I _{BM}	5.0		
Total Power Dissipation @ T _C = 25°C	P _D	175		Watts
Derate above 25°C		100		
@ T _C = 100°C		1.0		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. T₁ IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\pm \phi .13 (0.005) \text{ T } \text{V} \text{ (M)}$$

FOR LEADS:

$$\pm \phi .13 (0.005) \text{ (M) T } \text{V} \text{ (M) Q } \text{(M)}$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.09	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC 1.187 BSC			
G	10.92 BSC 0.430 BSC			
H	9.46 BSC 0.215 BSC			
J	16.89 BSC 0.665 BSC			
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.87	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 250\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	MJ10004 MJ10005	$V_{\text{CEO(sus)}}$	350 400	– –	– –	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) ($I_C = 2.0\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$)	MJ10004 MJ10005	$V_{\text{CEX(sus)}}$	400 450	– –	– –	Vdc
($I_C = 10\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$)	MJ10004 MJ10005		275 325	– –	– –	
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$) ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)		I_{CEV}	– –	– –	0.25 5.0	mAdc
Collector Cutoff Current ($V_{\text{CE}} = \text{Rated } V_{\text{CEV}}$, $R_{\text{BE}} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)		I_{CER}	–	–	5.0	mAdc
Emitter Cutoff Current ($V_{\text{EB}} = 2.0\text{ Vdc}$, $I_C = 0$)		I_{EBO}	–	–	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{\text{S/b}}$	See Figure 11			
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ON CHARACTERISTICS (2)

DC Current Gain ($I_C = 5.0\text{ Adc}$, $V_{\text{CE}} = 5.0\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 5.0\text{ Vdc}$)	h_{FE}	50 40	– –	600 400	–
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$) ($I_C = 20\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$, $T_C = 100^\circ\text{C}$)	$V_{\text{CE(sat)}}$	– – –	– – –	1.9 3.0 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$) ($I_C = 10\text{ Adc}$, $I_B = 400\text{ mAdc}$, $T_C = 100^\circ\text{C}$)	$V_{\text{BE(sat)}}$	– –	– –	2.5 2.5	Vdc
Diode Forward Voltage (1) ($I_F = 10\text{ Adc}$)	V_f	–	3.0	5.0	Vdc

DYNAMIC CHARACTERISTICS

Small-Signal Current Gain ($I_C = 1.0\text{ Adc}$, $V_{\text{CE}} = 10\text{ Vdc}$, $f_{\text{test}} = 1.0\text{ MHz}$)	$ h_{\text{fe}} $	10	–	–	–
Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	100	–	325	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$(V_{\text{CC}} = 250\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{\text{B1}} = 400\text{ mA}$, $V_{\text{BE(off)}} = 5.0\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2\%$).	t_d	–	0.12	0.2	μs
Rise Time		t_r	–	0.2	0.6	μs
Storage Time		t_s	–	0.6	1.5	μs
Fall Time		t_f	–	0.15	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	$(I_C = 10\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 400\text{ mA}$, $V_{\text{BE(off)}} = 5.0\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	–	1.0	2.5	μs
Crossover Time		t_c	–	0.4	1.5	μs
Storage Time		t_{sv}	–	0.65	–	μs
Crossover Time		t_c	–	0.2	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: $\text{PW} = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS

FIGURE 1 - DC CURRENT GAIN

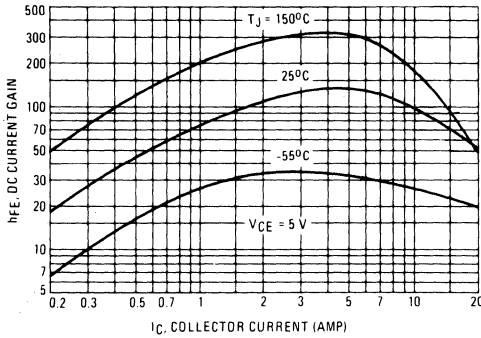


FIGURE 2 - COLLECTOR SATURATION REGION

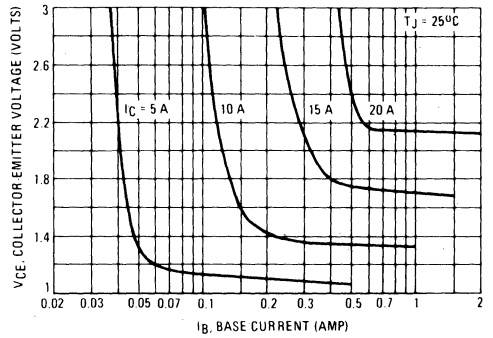


FIGURE 3 - COLLECTOR-EMITTER SATURATION VOLTAGE

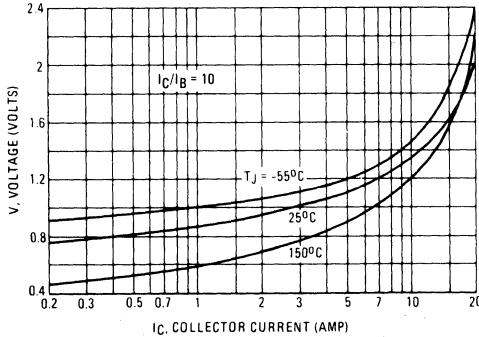


FIGURE 4 - BASE-EMITTER VOLTAGE

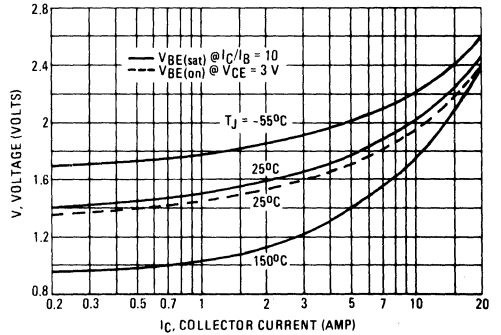


FIGURE 5 - COLLECTOR CUTOFF REGION

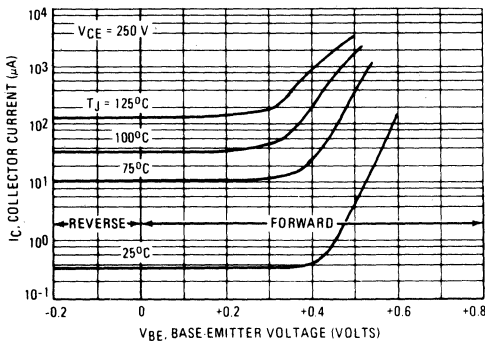


FIGURE 6 - OUTPUT CAPACITANCE

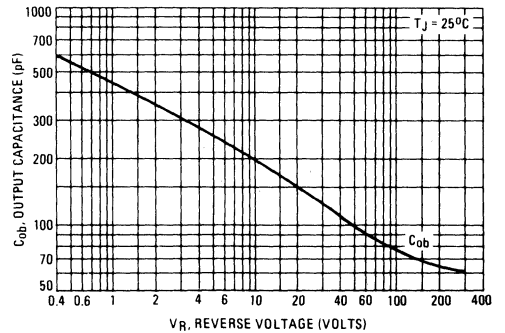


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

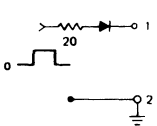
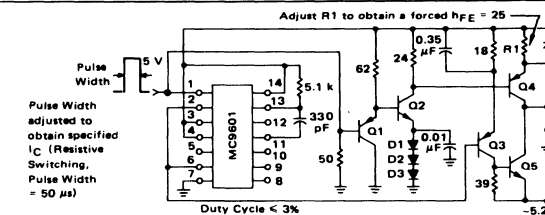
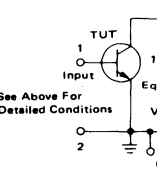
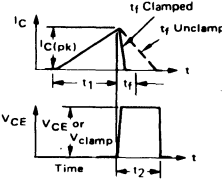
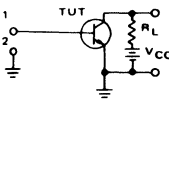
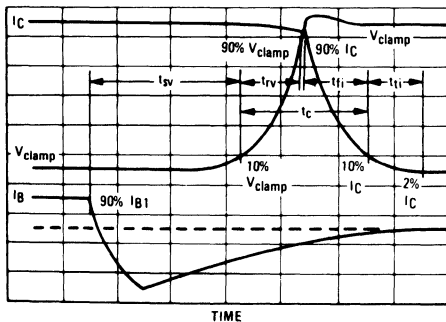
V _{CEO(sus)}	V _{CEX(sus)} AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
<p>INPUT CONDITIONS</p>  <p>PW Varied to Attain I_C = 250 mA</p>	<p>Adjust R1 to obtain a forced h_{FE} = 25</p>  <p>Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 μs)</p> <p>Duty Cycle < 3%</p>		<p>RESISTIVE SWITCHING</p> <p>Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914</p>
<p>CIRCUIT VALUES</p> <p>L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = V_{CEO(sus)}</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value</p>		<p>V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 μs</p>
<p>TEST CIRCUITS</p> <p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above For Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> <p>t₁ ≈ $\frac{L_{coil} (I_{Cpk})}{V_{CC}}$</p> <p>t₂ ≈ $\frac{L_{coil} (I_{Cpk})}{V_{clamp}}$</p> <p>Test Equipment Scope Tektronix 475 or Equivalent</p>		<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

TYPICAL CHARACTERISTICS

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rV} + t_{fI} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sV}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 - TURN-ON TIME

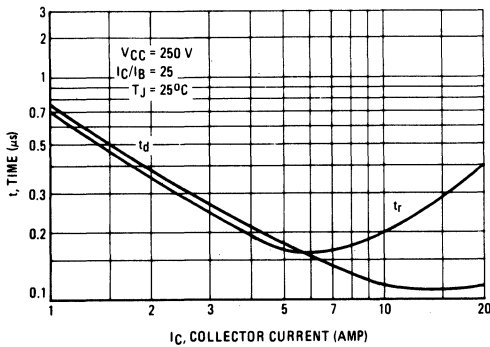


FIGURE 9 - TURN-OFF TIME

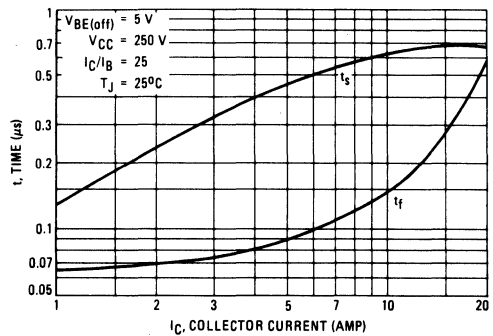
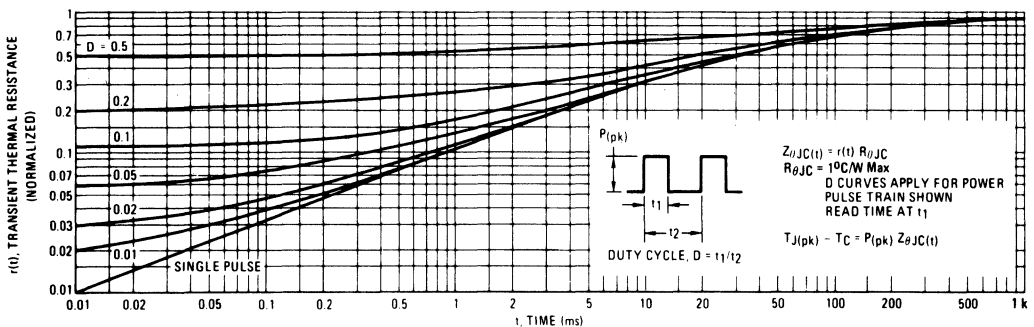


FIGURE 10 - THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

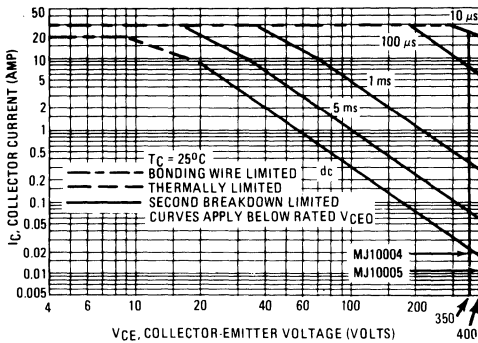


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA

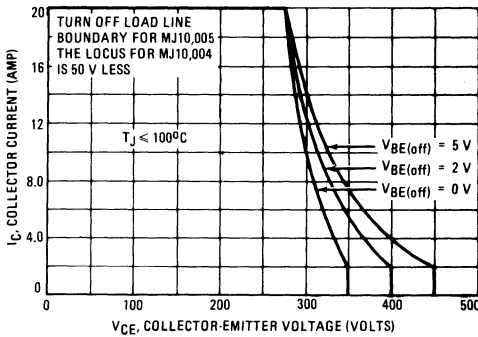
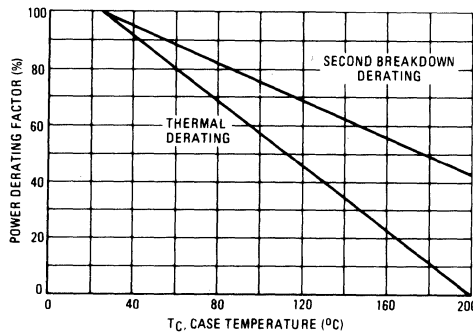


FIGURE 13 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(\text{SUS})}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The MJ10006 and MJ10007 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

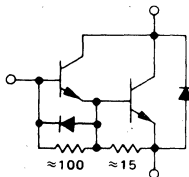
- Switching Regulators
 - Inverters
 - Solenoid and Relay Drivers
 - Motor Controls
 - Deflection Circuits
- Fast Turn-Off Times

30 ns Inductive Fall Time – 25°C (Typ)
 500 ns Inductive Storage Time – 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



10 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS

350 AND 400 VOLTS
150 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

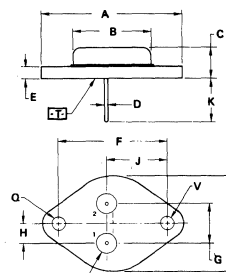
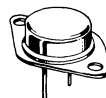
MAXIMUM RATINGS

Rating	Symbol	MJ10006	MJ10007	Unit
Collector-Emitter Voltage	V _{CEO}	350	400	V _{dc}
Collector-Emitter Voltage	V _{CEX}	400	450	V _{dc}
Collector-Emitter Voltage	V _{CEV}	450	500	V _{dc}
Emitter Base Voltage	V _{EB}	8.0		V _{dc}
Collector Current – Continuous	I _C	10		A _{dc}
– Peak (1)	I _{CM}	20		
Base Current – Continuous	I _B	2.5		A _{dc}
– Peak (1)	I _{BM}	5.0		
Total Power Dissipation @ T _C = 25°C	P _D	150		Watts
Derate above 25°C @ T _C = 100°C		100		
		0.86		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle < 10%.



STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. [T] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE IS:
 ⌀ ±0.13 (0.005) Ⓢ T V Ⓢ
 FOR LEADS:
 ⌀ ±0.13 (0.005) Ⓢ T V Ⓢ Ⓢ
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.08	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.39 BSC		0.645 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 250\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	MJ10006 MJ10007 $V_{\text{CEO(sus)}}$	350 400	— —	— —	Vdc	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) ($I_C = 1\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$)	MJ10006 MJ10007 $V_{\text{CEX(sus)}}$	400 450	— —	— —	Vdc	
($I_C = 5\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$)	MJ10006 MJ10007	275 325	— —	— —		
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$)	I_{CEV}	—	—	0.25	mAdc	
($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)		—	—	5.0		
Collector Cutoff Current ($V_{\text{CE}} = \text{Rated } V_{\text{CEV}}$, $R_{\text{BE}} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5.0	mAdc	
Emitter Cutoff Current ($V_{\text{EB}} = 2\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc	
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased	$I_{\text{S/b}}$	See Figure 11				
ON CHARACTERISTICS (2)						
DC Current Gain ($I_C = 2.5\text{ Adc}$, $V_{\text{CE}} = 5.0\text{ Vdc}$)	h_{FE}	40	—	500	—	
($I_C = 5.0\text{ Adc}$, $V_{\text{CE}} = 5.0\text{ Vdc}$)		30	—	300		
Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 250\text{ mAdc}$)	$V_{\text{CE(sat)}}$	—	—	1.9	Vdc	
($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$)		—	—	2.9		
($I_C = 5.0\text{ Adc}$, $I_B = 250\text{ mAdc}$, $T_C = 100^\circ\text{C}$)		—	—	2.0		
Base-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 250\text{ mAdc}$)	$V_{\text{BE(sat)}}$	—	—	2.5	Vdc	
($I_C = 5.0\text{ Adc}$, $I_B = 250\text{ mAdc}$, $T_C = 100^\circ\text{C}$)		—	—	2.5		
Diode Forward Voltage (1) ($I_F = 5.0\text{ Adc}$)	V_f	—	3.0	5	Vdc	
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain ($I_C = 1.0\text{ Adc}$, $V_{\text{CE}} = 10\text{ Vdc}$, $f_{\text{test}} = 1.0\text{ MHz}$)	$ h_{\text{fe}} $	10	—	—	—	
Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	60	—	275	pF	
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	($V_{\text{CC}} = 250\text{ Vdc}$, $I_C = 5.0\text{ A}$, $I_{\text{B1}} = 250\text{ mA}$, $V_{\text{BE(off)}} = 5.0\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.05	0.2	μs
Rise Time		t_r	—	0.25	0.6	μs
Storage Time		t_s	—	0.5	1.5	μs
Fall Time		t_f	—	0.06	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	($I_C = 5.0\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 250\text{ mA}$, $V_{\text{BE(off)}} = 5.0\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	0.8	2.0	μs
Crossover Time		t_c	—	0.6	1.5	μs
Storage Time	($I_C = 5.0\text{ A(pk)}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $I_{\text{B1}} = 250\text{ mA}$, $V_{\text{BE(off)}} = 5.0\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_{sv}	—	0.5	—	μs
Crossover Time		t_c	—	0.3	—	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs , Duty Cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS

FIGURE 1 - DC CURRENT GAIN

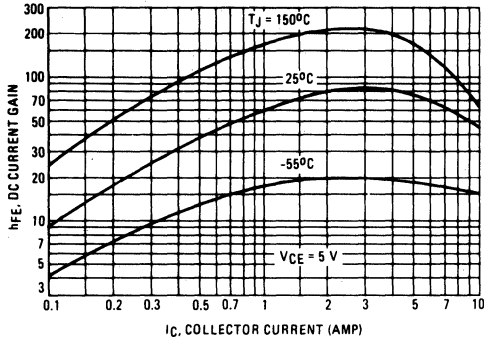


FIGURE 2 - COLLECTOR SATURATION REGION

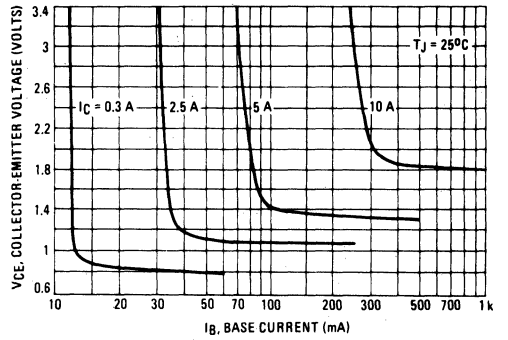


FIGURE 3 - COLLECTOR-EMITTER SATURATION VOLTAGE

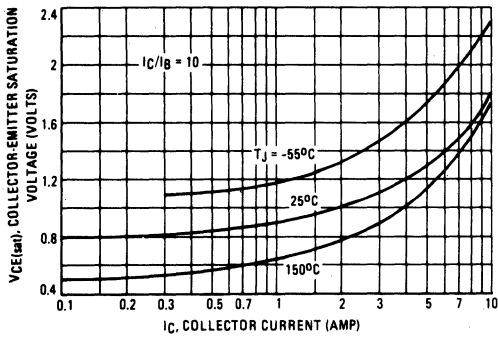


FIGURE 4 - BASE-EMITTER VOLTAGE

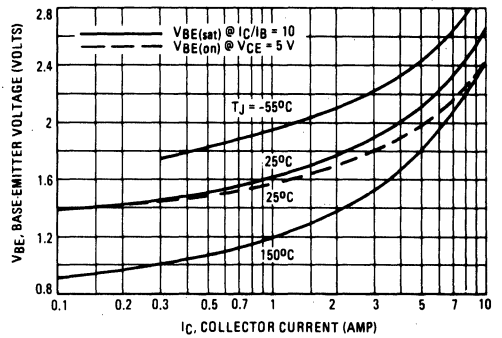


FIGURE 5 - COLLECTOR CUTOFF REGION

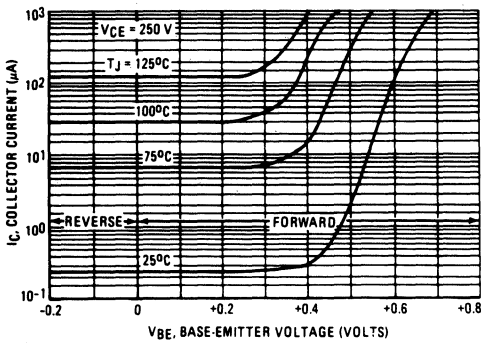
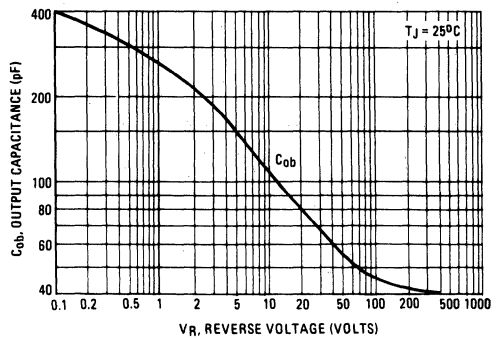


FIGURE 6 - OUTPUT CAPACITANCE



3

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

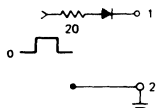
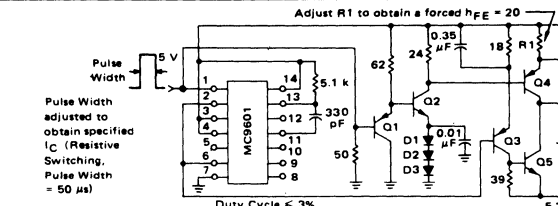
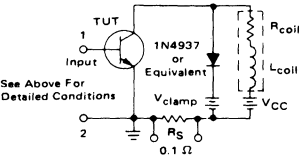
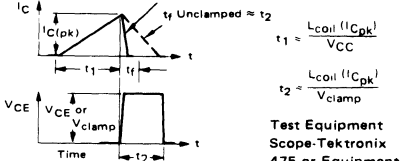
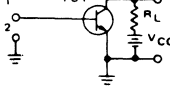
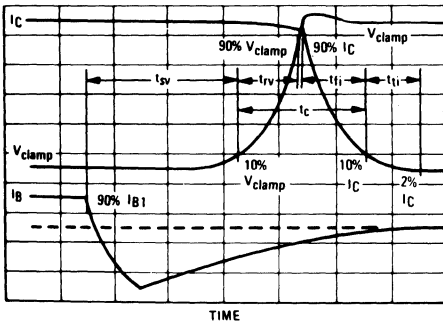
	$V_{CE0}(us)$	$V_{CEX}(us)$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain $I_C = 250$ mA</p>	 <p>Adjust R1 to obtain a forced $h_{FE} = 20$</p> <p>Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 μs)</p> <p>Duty Cycle $\leq 3\%$</p>	<p>Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE210 D1 1N914 D2 1N914 D3 1N914</p>
CIRCUIT VALUES	<p>$L_{coil} = 10$ mH $V_{CC} = 10$ V $R_{coil} = 0.7$ Ω $V_{clamp} = V_{CE0}(us)$</p>	<p>$L_{coil} = 180$ μH $R_{coil} = 0.05$ Ω $V_{CC} = 20$ V $f_o = 500$ kHz $V_{clamp} = \text{Rated } V_{CEX}$ Value</p>	<p>$V_{CC} = 250$ V $R_L = 50$ Ω Pulse Width = 50 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above For Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> $t_1 = \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 = \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope: Tektronix 475 or Equipment</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

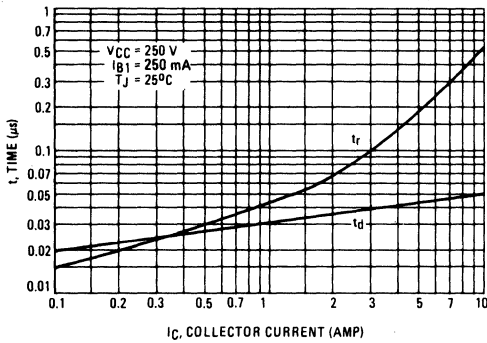


FIGURE 9 – TURN-OFF TIME

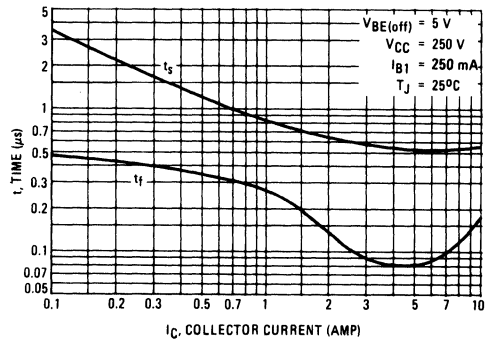
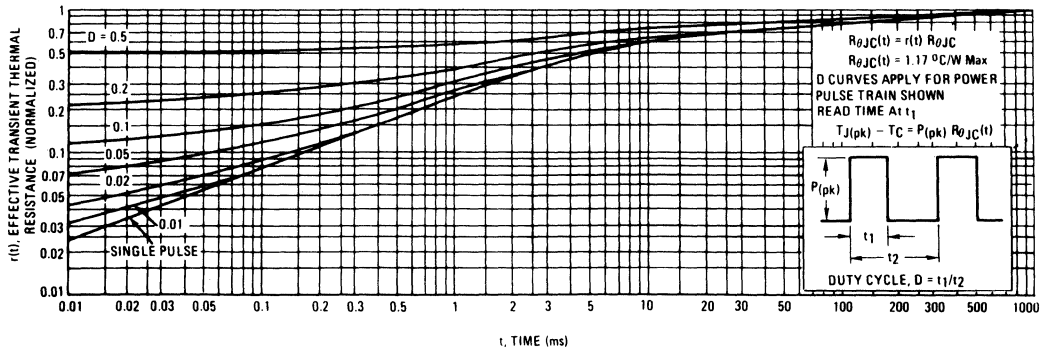


FIGURE 10 – THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

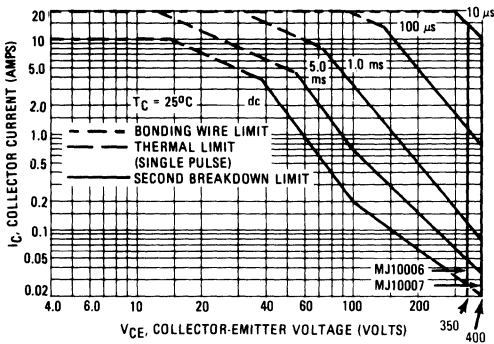


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA

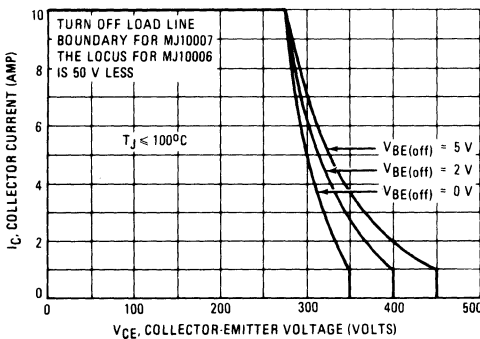
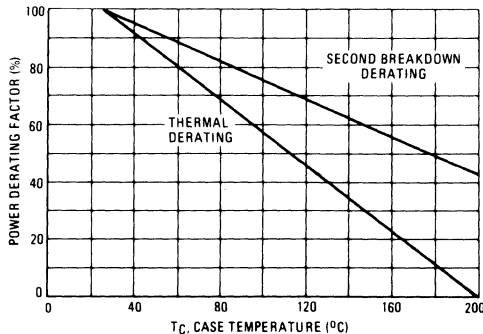


FIGURE 13 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

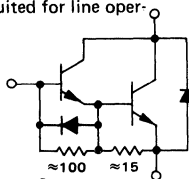
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The MJ10008 and MJ10009 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times



1.6 μ s (max) Inductive Crossover Time — 10 A, 100°C
 3.5 μ s (max) Inductive Storage Time — 10 A, 100°C

Operating Temperature Range — -65 to +200°C

100°C Performance Specified for:

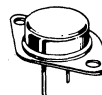
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

20 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS

450 and 500 VOLTS
175 WATTS

Designer's Data for
"Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



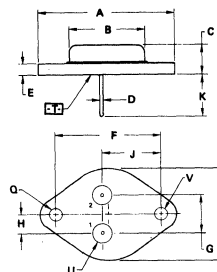
MAXIMUM RATINGS

Rating	Symbol	MJ10008	MJ10009	Unit
Collector-Emitter Voltage	V _{CEO}	450	500	Vdc
Collector-Emitter Voltage	V _{CEX}	450	500	Vdc
Collector-Emitter Voltage	V _{CEV}	650	700	Vdc
Emitter Base Voltage	V _{EB}	8		Vdc
Collector Current — Continuous	I _C	20		Adc
— Peak (1)	I _{CM}	30		
Base Current — Continuous	I _B	2.5		Adc
— Peak (1)	I _{BM}	5		
Total Power Dissipation @ T _C = 25°C	P _D	175		Watts
@ T _C = 100°C		100		
Derate above 25°C		1		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.



STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS			INCHES		
	MIN	MAX		MIN	MAX	
A	—	39.37	—	1.550		
B	—	21.08	—	0.830		
C	6.35	7.62	0.250	0.300		
D	0.97	1.03	0.038	0.043		
E	1.40	1.78	0.055	0.070		
F	30.15 BSC		1.187 BSC			
G	10.92 BSC		0.430 BSC			
H	5.48 BSC		0.215 BSC			
J	16.89 BSC		0.665 BSC			
K	11.18	12.75	0.440	0.500		
L	3.81	4.18	0.150	0.165		
R	—	26.67	—	1.050		
U	4.83	5.33	0.190	0.210		
V	3.81	4.19	0.150	0.165		

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	MJ10008 MJ10009	$V_{\text{CEO(sus)}}$	450 500	— —	— —	Vdc
Collector-Emitter Sustaining Voltage (Table 1, Figure 12) ($I_C = 2\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$, $V_{\text{BE(off)}} = 5\text{ V}$)	MJ10008 MJ10009	$V_{\text{CEX(sus)}}$	450 500	— —	— —	Vdc
($I_C = 10\text{ A}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEX}}$, $T_C = 100^\circ\text{C}$, $V_{\text{BE(off)}} = 5\text{ V}$)	MJ10008 MJ10009		325 375	— —	— —	
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$) ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)		I_{CEV}	— —	— —	0.25 5	mAdc
Collector Cutoff Current ($V_{\text{CE}} = \text{Rated } V_{\text{CEV}}$, $R_{\text{BE}} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)		I_{CER}	—	—	5	mAdc
Emitter Cutoff Current ($V_{\text{EB}} = 2\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	—	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{\text{S/b}}$	See Figure 11			
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ON CHARACTERISTICS (2)

DC Current Gain ($I_C = 5\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 5\text{ Vdc}$)	h_{FE}	40 30	— —	400 300	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 500\text{ mAdc}$) ($I_C = 20\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 500\text{ mAdc}$, $T_C = 100^\circ\text{C}$)	$V_{\text{CE(sat)}}$	— — —	— — —	2 3.5 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 500\text{ mAdc}$) ($I_C = 10\text{ Adc}$, $I_B = 500\text{ mAdc}$, $T_C = 100^\circ\text{C}$)	$V_{\text{BE(sat)}}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage (1) ($I_F = 10\text{ Adc}$)	V_f	—	3	5	Vdc

DYNAMIC CHARACTERISTICS

Small-Signal Current Gain ($I_C = 1\text{ Adc}$, $V_{\text{CE}} = 10\text{ Vdc}$, $f_{\text{test}} = 1\text{ MHz}$)	$ h_{\text{fe}} $	8	—	—	—
Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	100	—	325	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$V_{\text{CC}} = 250\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{\text{B1}} = 500\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $t_p = 25\ \mu\text{s}$ Duty Cycle $\leq 2\%$.	t_d	—	0.12	0.25	μs
Rise Time		t_r	—	0.5	1.5	μs
Storage Time		t_s	—	0.8	2.0	μs
Fall Time		t_f	—	0.2	0.6	μs
Inductive Load, Clamped (Table 1)						
Storage Time	$I_C = 10\text{ A(pk)}$, $V_{\text{clamp}} = 250\text{ V}$, $I_{\text{B1}} = 500\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	1.5	3.5	μs
Crossover Time		t_c	—	0.36	1.6	μs
Storage Time	$I_C = 10\text{ A(pk)}$, $V_{\text{clamp}} = 250\text{ V}$, $I_{\text{B1}} = 500\text{ mA}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$)	t_{sv}	—	0.8	—	μs
Crossover Time		t_c	—	0.18	—	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: $\text{PW} = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

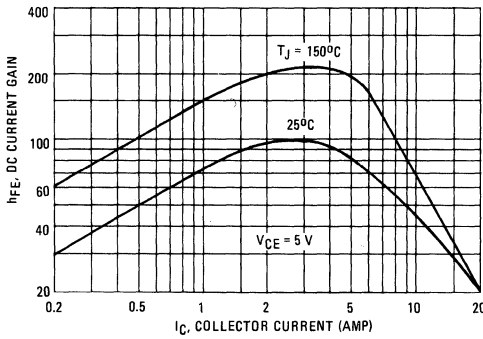


FIGURE 2 – COLLECTOR SATURATION REGION

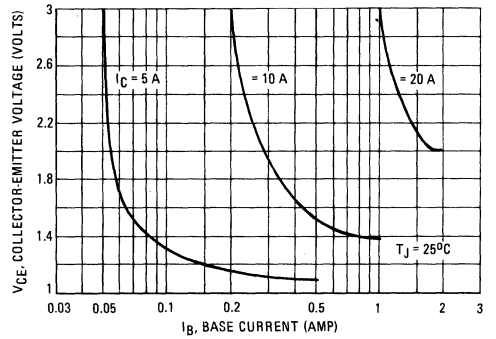


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

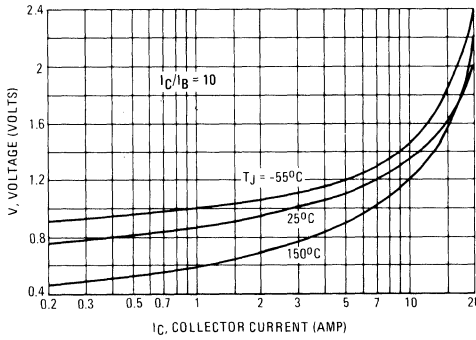


FIGURE 4 – BASE-EMITTER VOLTAGE

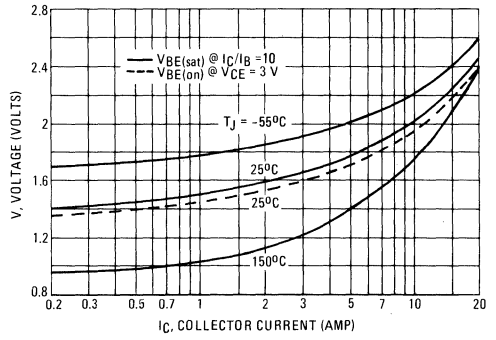


FIGURE 5 – COLLECTOR CUTOFF REGION

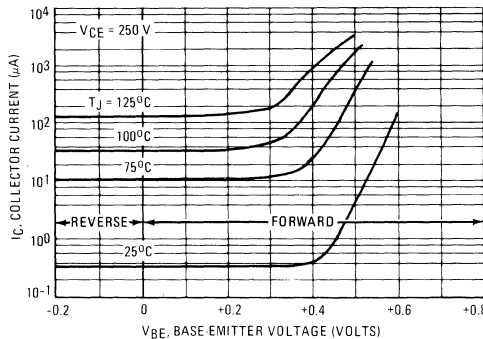
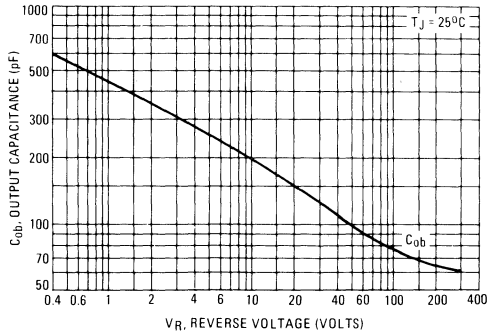


FIGURE 6 – OUTPUT CAPACITANCE



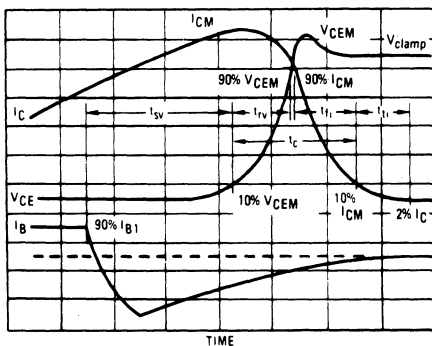
3

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CE0(sus)}	V _{CEX(sus)} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain I_C = 100 mA</p>	<p>DRIVER SCHEMATIC</p> <p>For inductive loads pulse width is adjusted to obtain specified I_C</p>	<p>TURN-ON TIME</p> <p>I_{B1} adjusted to obtain the forced β_{FE} desired</p> <p>TURN-OFF TIME</p> <p>Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = V_{CE0(sus)}</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value</p>	<p>V_{CC} = 250 V R_L = 25 Ω Pulse Width = 25 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above For Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope – Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

*Adjust -V such that V_{BE(off)} = 5 V except as required for RB SOA (Figure 12).

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

– continued –



TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

Typical inductive switching waveforms are shown in Figure 7. In general, $t_{rV} + t_{fI} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at $T_C = 25^\circ\text{C}$ and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sV}) which are guaranteed at $T_C = 100^\circ\text{C}$.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 - TURN-ON TIME

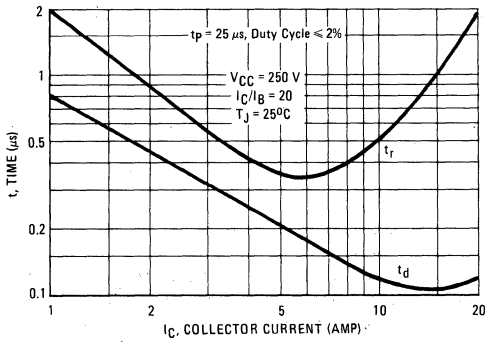


FIGURE 9 - TURN-OFF TIME

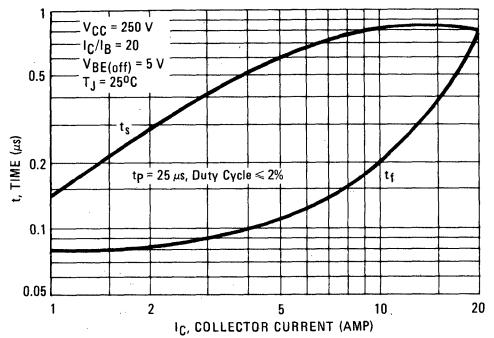
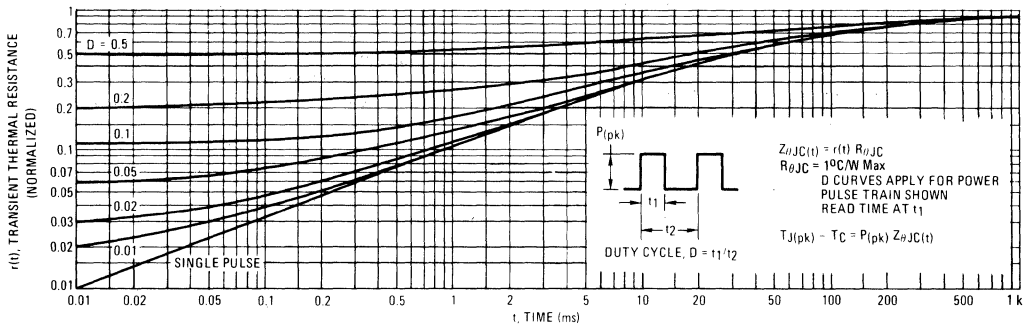


FIGURE 10 - THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

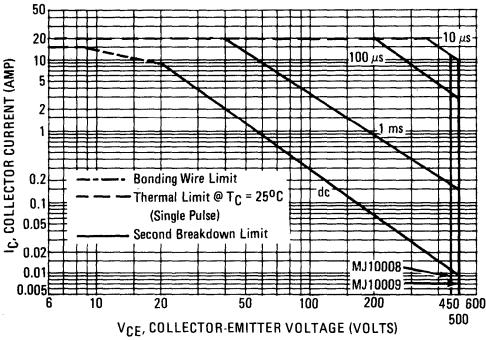


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA (MJ10009)

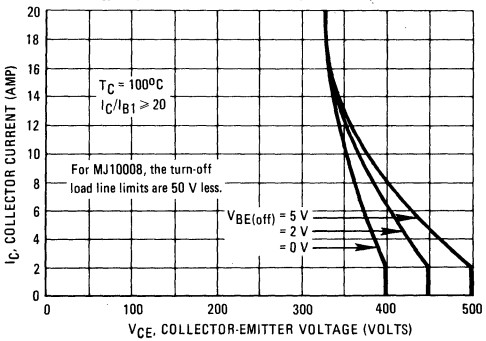
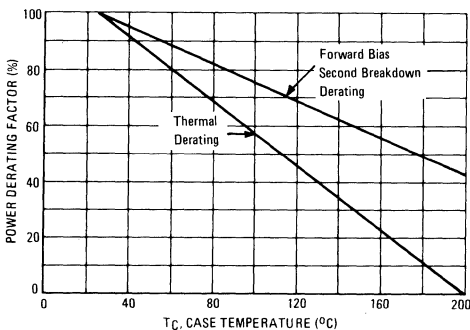


FIGURE 13 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

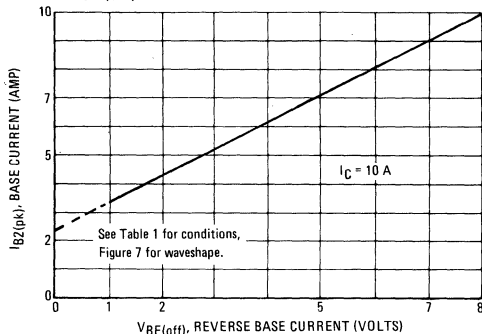
The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics. See Table 1 for circuit conditions.

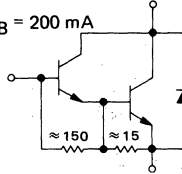
FIGURE 14 – REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



DARLINGTON
HORIZONTAL DEFLECTION TRANSISTOR

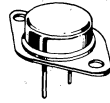
... specifically designed for use in deflection circuits.

- $V_{CE(sat)} = 3.0$ Volts (Max) @ $I_C = 4.0$ Amps, $I_B = 200$ mA
- Built-In Damper Diode
- $V_{CEX} = 1400$ Volts
- Glassivated Base-Collector Junction
- Safe Operating Area @ $50 \mu s = 25$ A, 200 V



8.0 AMPERE
NPN SILICON
DARLINGTON
POWER TRANSISTOR

1400 VOLTS
80 WATTS



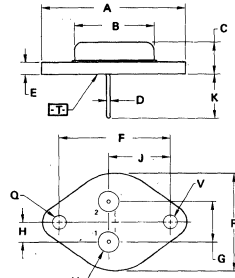
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEX}	1400	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	8.0	A dc
Peak (1)	I_{CM}	16	
Base Current — Continuous	I_B	2.0	A dc
Peak (1)	I_{BM}	4.0	
Emitter Current — Continuous	I_E	10	A dc
Peak (1)	I_{EM}	20	
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	80	Watts
Derate above $25^\circ C$		0.6	W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes: 1.8" from Case for 5 Seconds	T_L	275	$^\circ C$

(1) Pulse Test: Pulse Width = 1.0 ms, Duty Cycle \leq 10%.

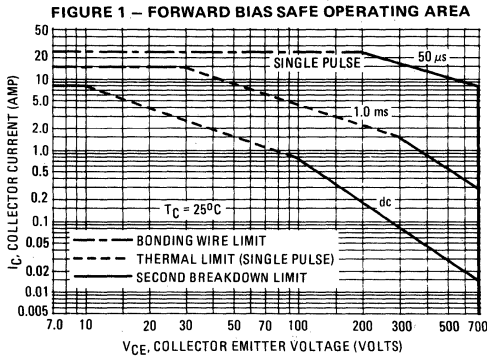


STYLE 1
PIN 1. BASE
2. EMITTER
3. COLLECTOR

- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
 ± 0.13 (0.005) \ominus T V \ominus
FOR LEADS:
 ± 0.13 (0.005) \ominus T V \ominus \oplus Q
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.560
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15	BSC	1.187	BSC
G	10.92	BSC	0.430	BSC
H	5.48	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage ($I_C = 100 \text{ mA dc}, I_B = 0$)	$V_{CE(sus)}$	700	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 1400 \text{ Vdc}, V_{BE} = 0$)	I_{CES}	—	—	0.25	mA dc
Emitter Cutoff Current ($V_{BE} = 4.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	—	50	mA dc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage ($I_C = 3.5 \text{ A dc}, I_B = 0.15 \text{ A dc}$) ($I_C = 4.0 \text{ A dc}, I_B = 0.2 \text{ A dc}$)	$V_{CE(sat)}$	— —	— —	3.0 3.0	Vdc
Base Emitter Saturation Voltage ($I_C = 3.5 \text{ A dc}, I_B = 0.15 \text{ A dc}$) ($I_C = 4.0 \text{ A dc}, I_B = 0.2 \text{ A dc}$)	$V_{BE(sat)}$	— —	— —	2.0 2.0	Vdc
Forward Diode Voltage ($I_F = 4.0 \text{ A dc}$)	V_f	—	1.2	2.0	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 1			
SWITCHING CHARACTERISTICS					
Fall Time (See Figure 2) ($I_C = 4.0 \text{ A dc}, I_{B1} = 0.2 \text{ A dc}$)	t_f	—	0.65	1.0	μs

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle = 2%.

FIGURE 2 – FALL TIME TEST CIRCUIT

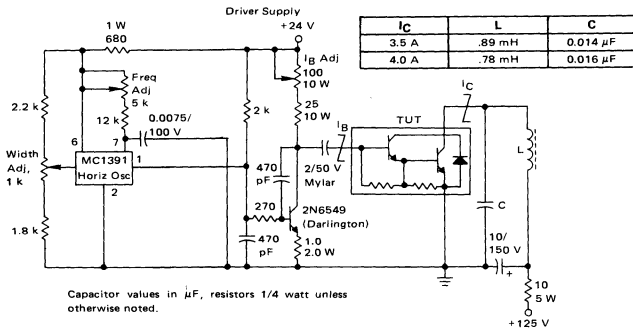
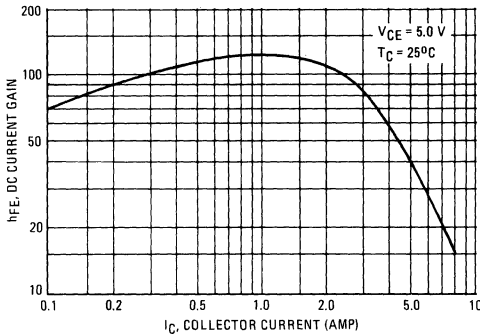


FIGURE 3 – DC CURRENT GAIN



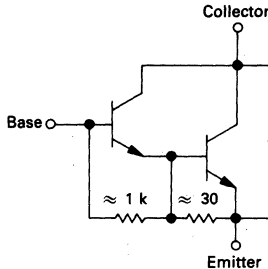
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ10012
MJH10012

NPN SILICON POWER DARLINGTON TRANSISTOR

The MJ10012 and MJH10012 are high-voltage, high-current Darlington transistors designed for automotive ignition, switching regulator and motor control applications.

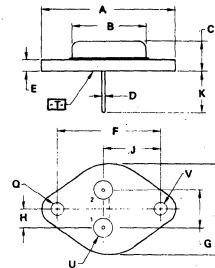
- Collector-Emitter Sustaining Voltage — $V_{CE(sus)} = 400 \text{ Vdc (Min)}$
- 175 Watts Capability at 50 Volts
- Automotive Functional Tests



10 AMPERE

POWER TRANSISTORS
DARLINGTON NPN SILICON

400 VOLTS
 175 AND 118 WATTS



MJ10012



STYLE 1
 PIN 1. BASE
 PIN 2. EMITTER
 CASE. COLLECTOR

- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. () IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q.
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	35.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.91	1.08	0.036	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC 1.187 BSC			
G	10.92 BSC 0.429 BSC			
H	5.46 BSC 0.215 BSC			
J	16.80 BSC 0.662 BSC			
K	11.18	12.18	0.440	0.480
L	3.81	4.18	0.151	0.165
M	26.67 1.050			
Q	4.83	5.33	0.190	0.210
V	3.81	4.18	0.151	0.165

CASE 1-05
TO-204AA

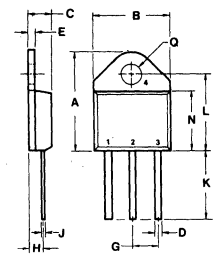
MAXIMUM RATINGS

Rating	Symbol	MJ10012	MJH10012	Unit
Collector-Emitter Voltage	V_{CEO}	400		Vdc
Collector-Emitter Voltage ($R_{BE} = 27 \Omega$)	V_{CER}	550		Vdc
Collector-Base Voltage	V_{CBO}	600		Vdc
Emitter-Base Voltage	V_{EBO}	8.0		Vdc
Collector Current — Continuous	I_C	10		Adc
Collector Current — Peak (1)		15		Adc
Base Current	I_B	2.0		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175	118	Watts
@ $T_C = 100^\circ\text{C}$		100	47.5	Watts
Derate above 25°C		1.0	1.05	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	-55 to +150	$^\circ\text{C}$

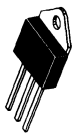
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle $\leq 10\%$.



MJH10012



- STYLE 1:
 PIN 1. BASE
 PIN 2. COLLECTOR
 PIN 3. EMITTER
 PIN 4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.628
C	4.18	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.48	16.51	0.625	0.650
M	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Figure 1) ($I_C = 200\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	$V_{\text{CEO(sus)}}$	400	—	—	Vdc
Collector-Emitter Sustaining Voltage (Figure 1) ($I_C = 200\text{ mA}$, $R_{\text{BE}} = 27\text{ Ohms}$, $V_{\text{clamp}} = \text{Rated } V_{\text{CER}}$)	$V_{\text{CER(sus)}}$	425	—	—	Vdc
Collector Cutoff Current (Rated V_{CER} , $R_{\text{BE}} = 27\text{ Ohms}$)	I_{CER}	—	—	1.0	mAdc
Collector Cutoff Current (Rated V_{CBO} , $I_E = 0$)	I_{CBO}	—	—	1.0	mAdc
Emitter Cutoff Current ($V_{\text{EB}} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	40	mAdc

ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 3.0\text{ Adc}$, $V_{\text{CE}} = 6.0\text{ Vdc}$) ($I_C = 6.0\text{ Adc}$, $V_{\text{CE}} = 6.0\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 6.0\text{ Vdc}$)	h_{FE}	300 100 20	550 350 150	— 2000 —	—
Collector-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$) ($I_C = 6.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2.0\text{ Adc}$)	$V_{\text{CE(sat)}}$	— — —	— — —	1.5 2.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 6.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2.0\text{ Adc}$)	$V_{\text{BE(sat)}}$	— —	— —	2.5 3.0	Vdc
Base-Emitter On Voltage ($I_C = 10\text{ Adc}$, $V_{\text{CE}} = 6.0\text{ Vdc}$)	$V_{\text{BE(on)}}$	—	—	2.8	Vdc
Diode Forward Voltage ($I_F = 10\text{ Adc}$)	V_f	—	2.0	3.5	Vdc

DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	—	165	350	pF

SWITCHING CHARACTERISTICS						
Storage Time	($V_{\text{CC}} = 12\text{ Vdc}$, $I_C = 6.0\text{ Adc}$, $I_{\text{B1}} = I_{\text{B2}} = 0.3\text{ Adc}$) Figure 2	t_s	—	7.5	15	μs
Fall Time		t_f	—	5.2	15	μs

FUNCTIONAL TESTS					
Second Breakdown Collector Current with Base-Forward Biased	$I_{\text{S/B}}$	See Figure 10			—
Pulsed Energy Test (See Figure 12)	$\frac{I_C^2 L}{2}$	—	—	180	mJ

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.



FIGURE 1 – SUSTAINING VOLTAGE TEST CIRCUIT

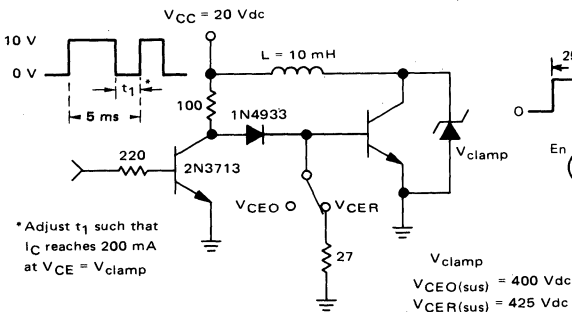


FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

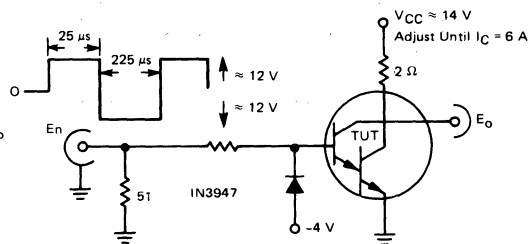


FIGURE 3 – DC CURRENT GAIN

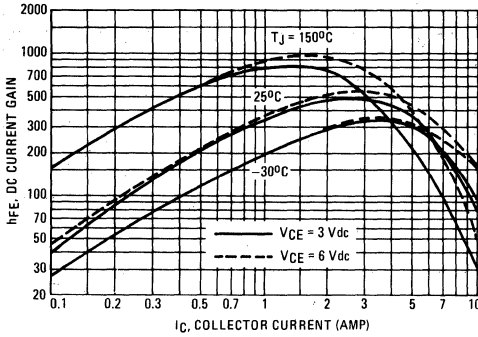


FIGURE 4 – COLLECTOR-SATURATION REGION

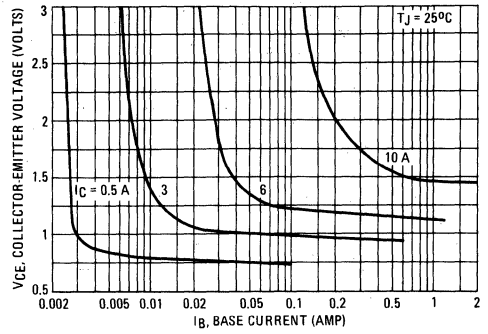


FIGURE 5 – COLLECTOR-EMITTER SATURATION VOLTAGE

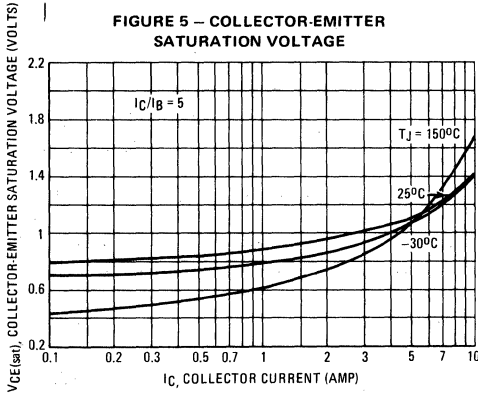


FIGURE 6 – BASE-EMITTER VOLTAGE

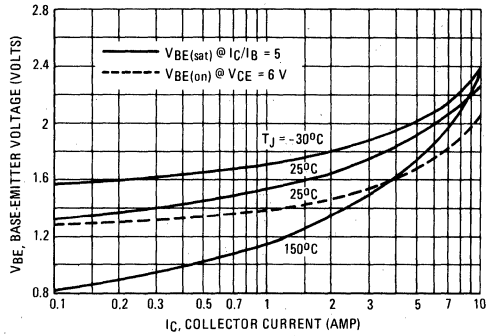


FIGURE 7 – TURN-OFF SWITCHING TIME

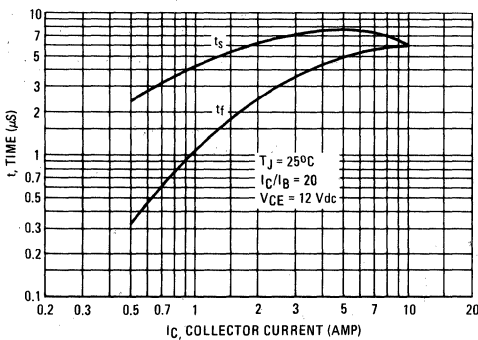
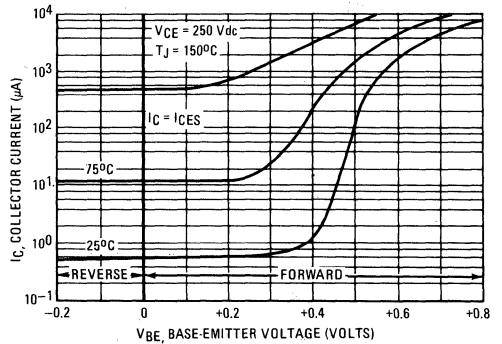


FIGURE 8 – COLLECTOR CUTOFF REGION



3

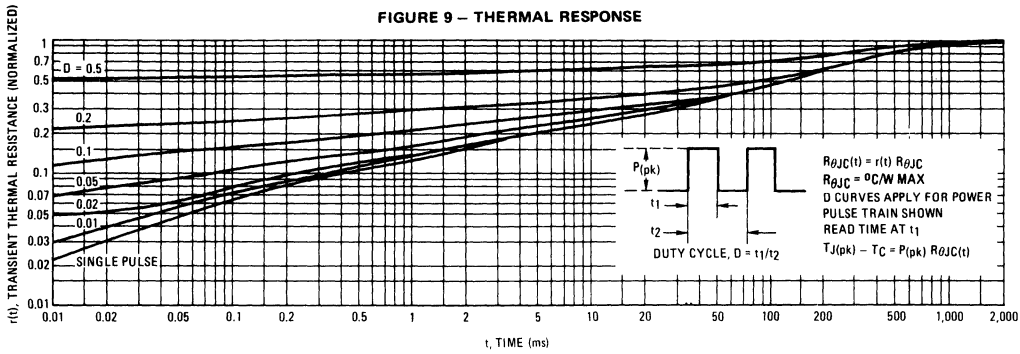
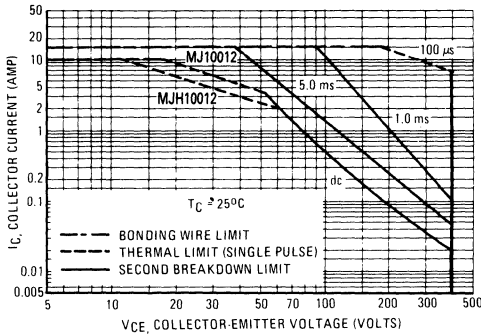


FIGURE 10 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^{\circ}\text{C}$; $T_{j(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^{\circ}\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{j(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING

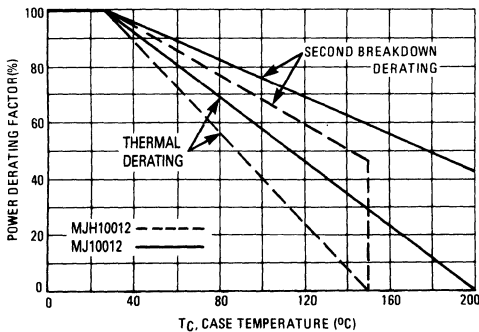
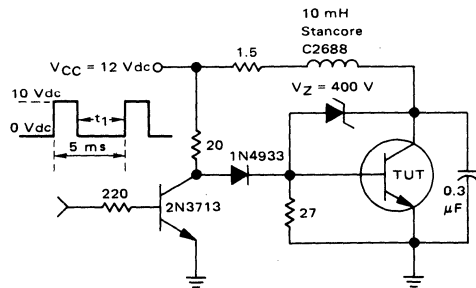


FIGURE 12 – USAGE TEST CIRCUIT



t_1 to be selected such that I_C reaches 6 Adc before switch-off.

NOTE:

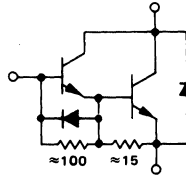
"Usage Test," Figure 12 specifies energy handling capabilities in an automotive ignition circuit.

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTOR

The MJ10014 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- Switching Regulators
 - Inverters
 - Solenoid and Relay Drivers
 - Motor Controls
 - Deflection Circuits
- Fast Turn-Off Times
 - 250 ns Inductive Fall Time—25°C (Typ)
 - 500 ns Inductive Crossover Time—25°C (Typ)
 - 1.4 μs Inductive Storage Time—25°C (Typ)
 - Operating Temperature Range: -65 to +200°C
 - 100°C Performance Specified for:
 - Reversed Biased SOA With Inductive Loads
 - Switching Times With Inductive Loads
 - Saturation Voltages
 - Leakage Currents



10 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR

600 VOLTS
175 WATTS

Designers Data for
"Worst-Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristic boundaries—are given to facilitate "worst-case" design.

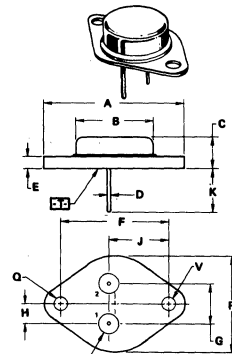
MAXIMUM RATINGS

Rating	Symbol	MJ10014	Unit
Collector-Emitter Voltage	V _{CEO}	600	Vdc
Collector-Emitter Voltage	V _{CEV}	700	Vdc
Emitter Base Voltage	V _{EB}	8	Vdc
Collector Current — Continuous	I _C	10	Adc
— Peak (1)	I _{CM}	15	
Base Current — Continuous	I _B	7	Adc
— Peak (1)	I _{BM}	10	
Total Power Dissipation @ T _C = 25°C	P _D	175	Watts
@ T _C = 100°C		100	
Derate above 25°C		1	W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%



- NOTES: U
1. DIMENSIONS D AND V ARE DATUMS.
 2. [] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D:
 $\text{⌀ } \frac{1}{16} \text{ (0.005) } \text{Ⓜ } \text{T } \text{V } \text{Ⓜ}$
 - FOR LEADS:
 $\text{⌀ } \frac{1}{16} \text{ (0.005) } \text{Ⓜ } \text{T } \text{V } \text{Ⓜ } \text{Ⓜ}$
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.27	—	1.550
B	—	21.88	—	0.860
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
M	—	26.67	—	1.050
N	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	600	—	—	Vdc
MJ10014					
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	—	—	0.3 5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5	mAdc
Emitter Cutoff Current ($V_{EB} = 2\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			

ON CHARACTERISTICS (2)

DC Current Gain ($I_C = 5\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	20 10	— —	500 250	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— —	— —	2.5 2.6	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	3 3	Vdc
Diode Forward Voltage (1) ($I_F = 10\text{ Adc}$)	V_f	—	3	5	Vdc

DYNAMIC CHARACTERISTICS

Small-Signal Current Gain ($I_C = 1\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1\text{ MHz}$)	$ h_{fe} $	10	—	—	—
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 100\text{ kHz}$)	C_{ob}	100	—	350	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{B1} = 400\text{ mA}$, $V_{BE(off)} = 5\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2\%$).	t_d	—	0.02	0.2	μs
Rise Time		t_r	—	0.9	2	μs
Storage Time		t_s	—	0.95	4	μs
Fall Time		t_f	—	0.22	1	μs
Inductive Load, Clamped (Table 1)						
Storage Time	$(I_C = 10\text{ A(pk)}$, $V_{clamp} = 250\text{ Vdc}$, $I_{B1} = 1\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_s	—	2.3	6	μs
Crossover Time		t_c	—	1	3	μs
Storage Time	$(I_C = 10\text{ A(pk)}$, $V_{clamp} = 250\text{ Vdc}$, $I_{B1} = 1\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_s	—	1.4	—	μs
Crossover Time		t_c	—	0.5	—	μs
Fall Time		t_{fi}	—	0.25	—	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

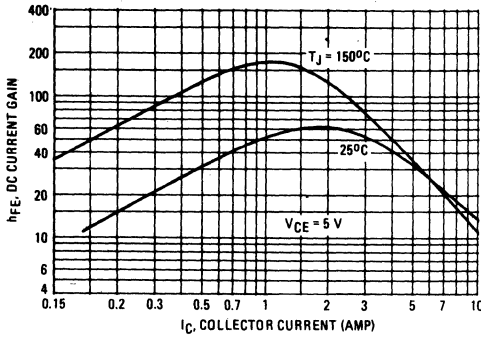


FIGURE 2 – COLLECTOR SATURATION REGION

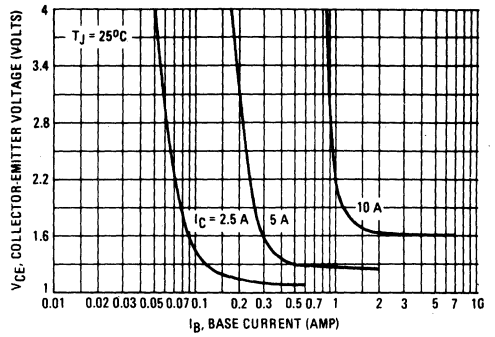


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

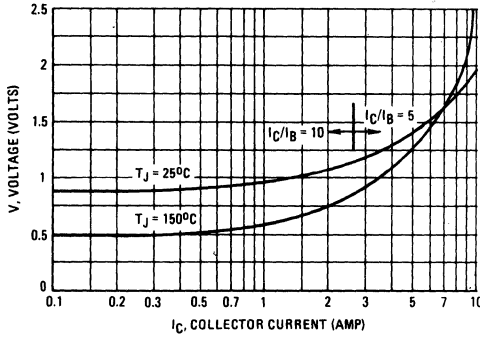


FIGURE 4 – BASE-EMITTER VOLTAGE

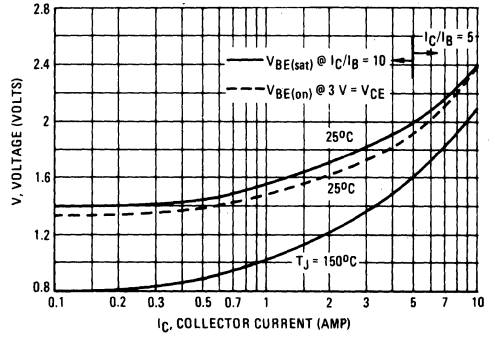


FIGURE 5 – COLLECTOR CUTOFF REGION

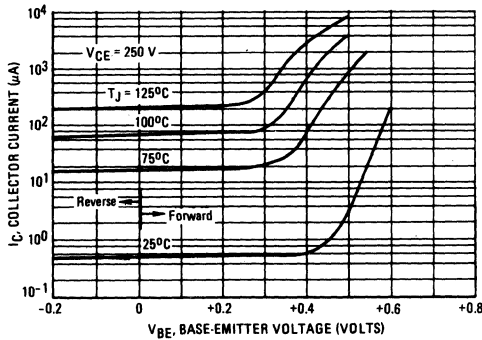
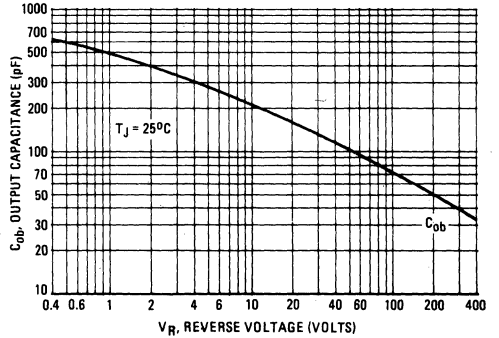


FIGURE 6 – OUTPUT CAPACITANCE



3

TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain I_C = 250 mA</p>	<p>Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 μs)</p> <p>Duty Cycle ≤ 3%</p>	<p>Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914</p>
CIRCUIT VALUES	<p>L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = V_{CEO(sus)}</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p>	<p>V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> <p>t₁ ≈ $\frac{L_{coil}(I_{Cpk})}{V_{CC}}$</p> <p>t₂ ≈ $\frac{L_{coil}(I_{Cpk})}{V_{clamp}}$</p> <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

SWITCHING TIME NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10-90% V_{clamp}
- t_{fi} = Current Fall Time, 90-10% I_C
- t_{ti} = Current Tail, 10-2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

- continued -

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

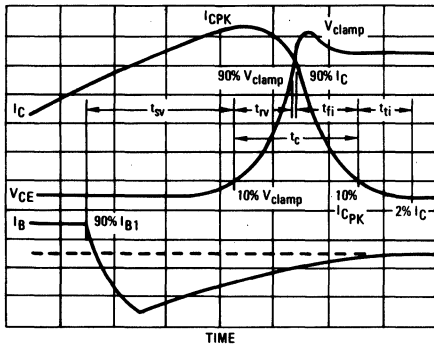
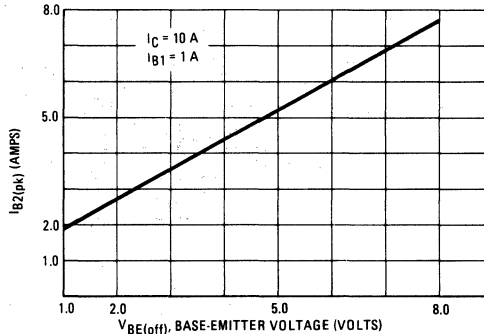


FIGURE 8 - PEAK REVERSE CURRENT



TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rV} + t_{fI} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 - TURN-ON TIME

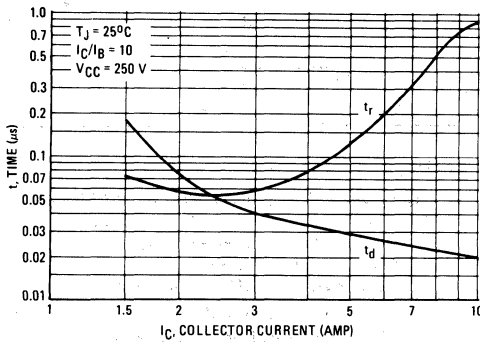


FIGURE 10 - TURN-OFF TIME

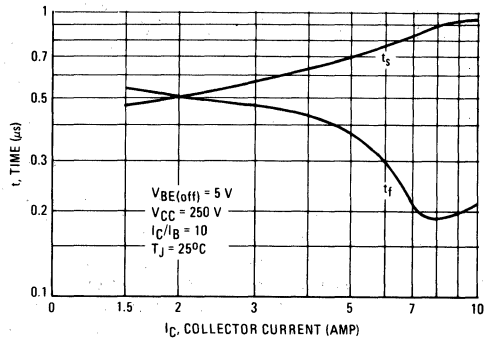
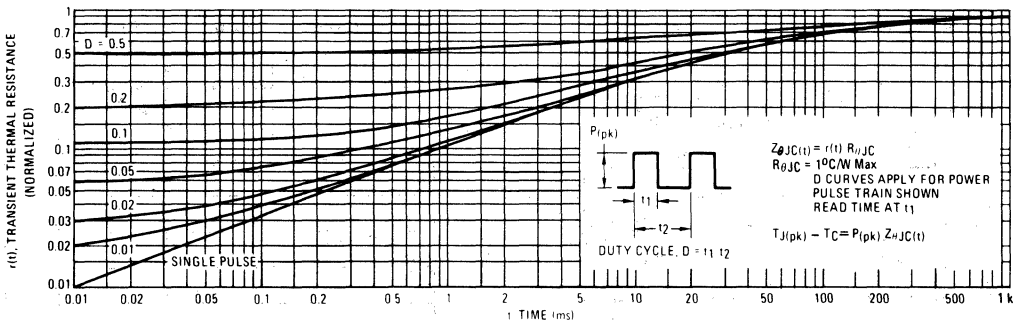


FIGURE 11 - THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

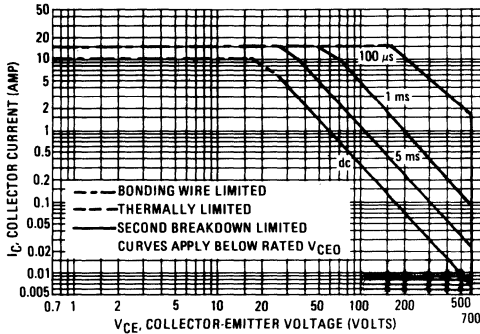


FIGURE 13 – REVERSE BIAS SWITCHING SAFE OPERATING AREA

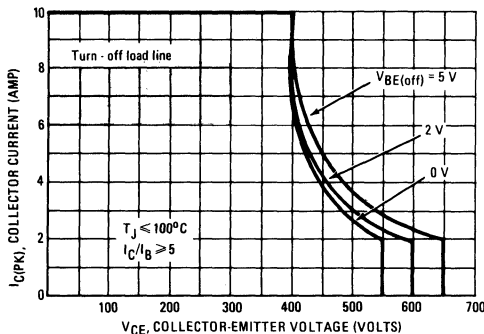
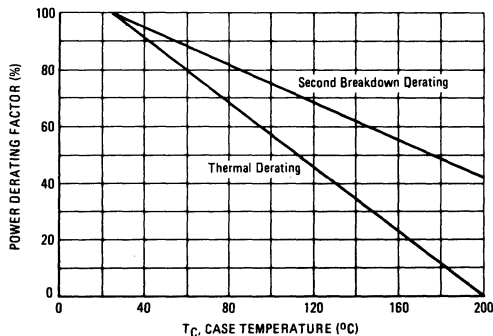


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

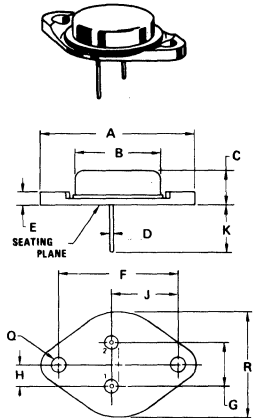
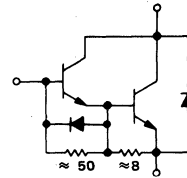
SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The MJ10015 and MJ10016 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Motor Controls
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 1.0 μ s (max) Inductive Crossover Time – 20 Amps
 - 2.5 μ s (max) Inductive Storage Time – 20 Amps
- Operating Temperature Range –65 to +200°C
- Performance Specified for
 - Reversed Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

50 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS

400 and 500 VOLTS
250 WATTS



STYLE 1:
 PIN 1. BASE
 PIN 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.90	0.057	0.075
E	—	3.43	—	0.135
F	28.90	30.40	1.127	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

MAXIMUM RATINGS

Rating	Symbol	MJ10015	MJ10016	Unit
Collector-Emitter Voltage	V_{CEO}	400	500	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current – Continuous	I_C	50		Adc
– Peak (1)	I_{CM}	75		Adc
Base Current – Continuous	I_B	10		Adc
– Peak (1)	I_{BM}	15		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250		Watts
@ $T_C = 100^\circ\text{C}$		143		
Derate above 25°C		1.43		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	MJ10015 MJ10016 $V_{\text{CEO(sus)}}$	400 500	— —	— —	Vdc
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$)	I_{CEV}	—	—	0.25	mAdc
Emitter Cutoff Current ($V_{\text{EB}} = 2.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	350	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{\text{S/b}}$	See Figure 7			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 8			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 20\text{ Adc}$, $V_{\text{CE}} = 5.0\text{ Vdc}$) ($I_C = 40\text{ Adc}$, $V_{\text{CE}} = 5.0\text{ Vdc}$)	h_{FE}	25 10	— —	— —	—
Collector-Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 50\text{ Adc}$, $I_B = 10\text{ Adc}$)	$V_{\text{CE(sat)}}$	— —	— —	2.2 5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 1.0\text{ Adc}$)	$V_{\text{BE(sat)}}$	—	—	2.75	Vdc
Diode Forward Voltage (2) ($I_F = 20\text{ Adc}$)	V_f	—	2.5	5.0	Vdc

DYNAMIC CHARACTERISTIC

Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	—	—	750	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)					
Delay Time	$(V_{\text{CC}} = 250\text{ Vdc}$, $I_C = 20\text{ A}$, $I_{\text{B1}} = 1.0\text{ Adc}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $t_p = 25\text{ }\mu\text{s}$ Duty Cycle $\leq 2\%$).	t_d	—	0.14	0.3
Rise Time		t_r	—	0.3	1.0
Storage Time		t_s	—	0.8	2.5
Fall Time		t_f	—	0.3	1.0
Inductive Load, Clamped (Table 1)					
Storage Time	$(I_C = 20\text{ A(pk)}$, $V_{\text{clamp}} = 250\text{ V}$, $I_{\text{B1}} = 1.0\text{ A}$, $V_{\text{BE(off)}} = 5.0\text{ Vdc}$)	t_{sv}	—	1.0	2.5
Crossover Time		t_c	—	0.36	1.0

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

(2) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.



TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

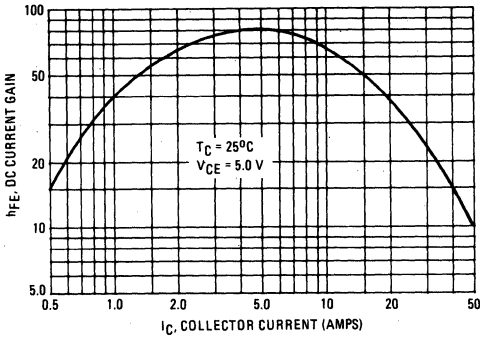


FIGURE 2 – COLLECTOR-EMITTER SATURATION VOLTAGE

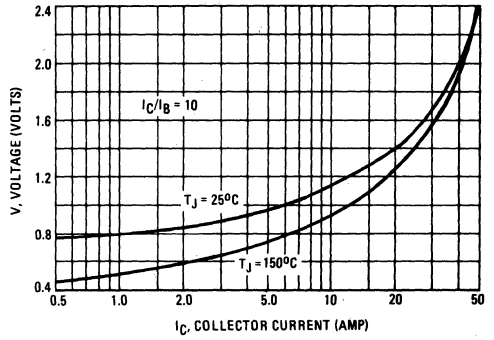


FIGURE 3 – BASE-EMITTER SATURATION VOLTAGE

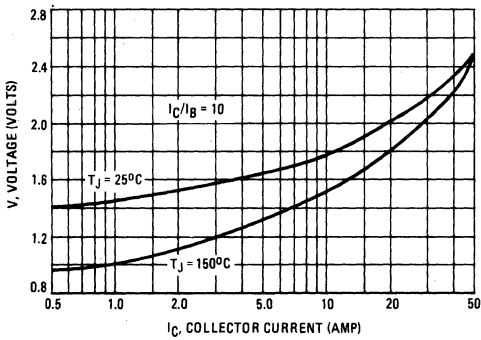


FIGURE 4 – COLLECTOR CUTOFF REGION

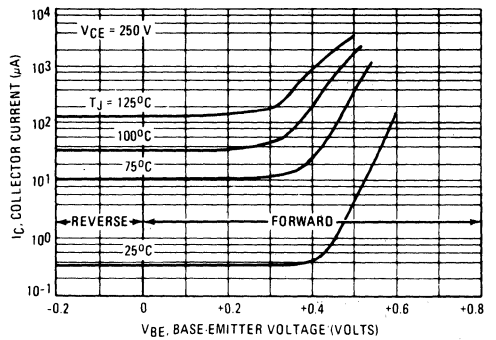


FIGURE 5 – OUTPUT CAPACITANCE

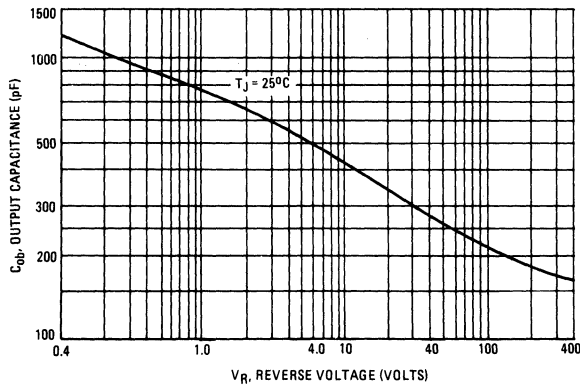
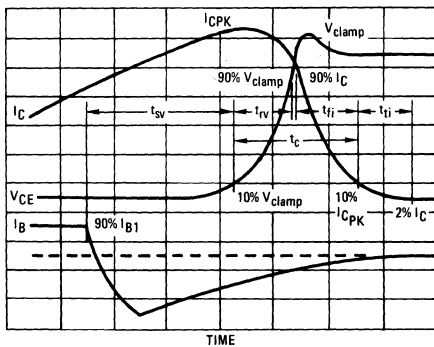


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CE0} (sus)	V _{CEX} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>5 V 0</p> <p>20 Ω</p> <p>PW Varied to Attain I_C = 100 mA</p>	<p>Adjust R1 to obtain a forced h_FE = 20</p> <p>Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 25 μs)</p> <p>Duty Cycle < 3%</p>	<p>TURN-ON TIME</p> <p>I_{B1} adjusted to obtain the forced h_FE desired</p> <p>TURN-OFF TIME</p> <p>Use inductive switching circuit as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 10 mH V_{CC} = 10 V</p> <p>R_{coil} = 0.7 Ω</p> <p>V_{clamp} = V_{CE0}(sus)</p>	<p>L_{coil} = 180 μH</p> <p>R_{coil} = 0.05 Ω</p> <p>V_{CC} = 20 V</p> <p>Q1 2N2907 Q5 MJE200</p> <p>Q2 2N2222 D1 1N914</p> <p>Q3 2N3762 D2 1N914</p> <p>Q4 MJE210 D3 1N914</p>	<p>V_{CC} = 250 V</p> <p>R_L = 12.5 Ω</p> <p>Pulse Width = 25 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> <p>t₁ ≈ $\frac{L_{coil}(I_{Cpk})}{V_{CC}}$</p> <p>t₂ ≈ $\frac{L_{coil}(I_{Cpk})}{V_{clamp}}$</p> <p>Test Equipment Scope – Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

*Adjust -V such that V_{BE(off)} = 5 V except as required for RB SOA (Figure B).

FIGURE 6 – INDUCTIVE SWITCHING MEASUREMENTS



t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
 t_{RV} = Voltage Rise Time, 10–90% V_{clamp}
 t_{FJ} = Current Fall Time, 90–10% I_C
 t_{TI} = Current Tail, 10–2% I_C
 t_C = Crossover Time, 10% V_{clamp} to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

SWITCHING TIMES NOTE

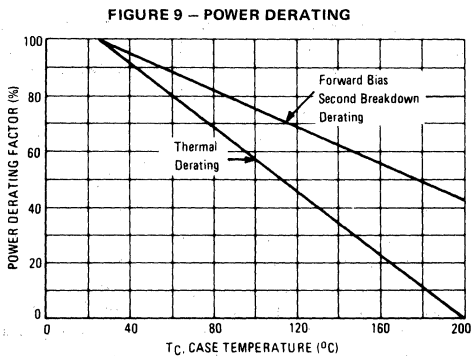
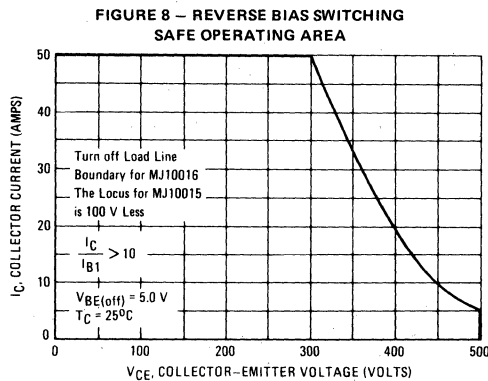
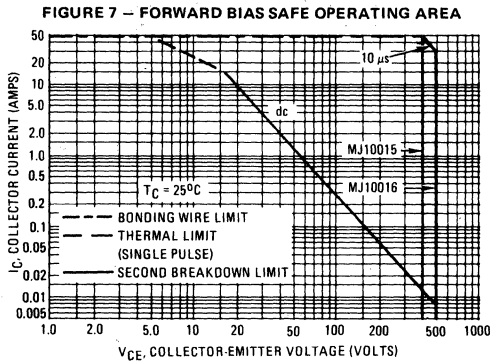
In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

In general, t_{RV} + t_{FJ} ≈ t_C. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_C and t_{SV}) which are guaranteed.



The Safe Operating Area figures shown in Figures 7 and 8 are specified ratings for these devices under the test conditions shown.



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

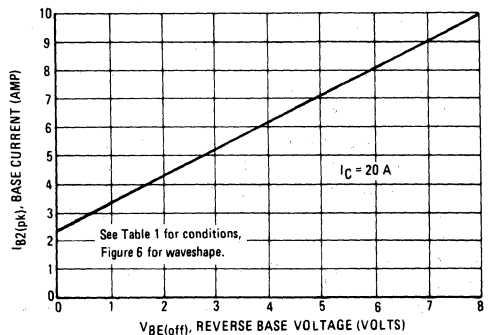
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the complete RBSOA characteristics.

FIGURE 10 – TYPICAL REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



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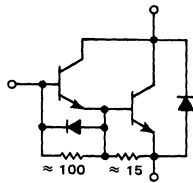
MJ10020
MJ10021

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The MJ10020 and MJ10021 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 150 ns Inductive Fall Time at 25°C (Typ)
 - 750 ns Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
 - Reversed Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents



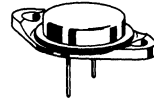
60 AMPERE

NPN SILICON
POWER DARLINGTON
TRANSISTORS

200 and 250 VOLTS
 250 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



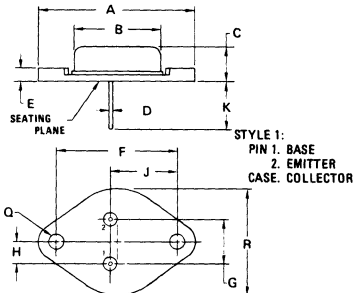
MAXIMUM RATINGS

Rating	Symbol	MJ10020	MJ10021	Unit
Collector-Emitter Voltage	V _{CEO}	200	250	Vdc
Collector-Emitter Voltage	V _{CEV}	300	350	Vdc
Emitter Base Voltage	V _{EB}	8.0		Vdc
Collector Current - Continuous	I _C	60		Adc
Collector Current - Peak (1)	I _{CM}	100		
Base Current - Continuous	I _B	20		Adc
Base Current - Peak (1)	I _{BM}	30		
Total Power Dissipation @ T _C = 25°C	P _D	250		Watts
Derate above 25°C @ T _C = 100°C		143		
		1.43		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.750	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	-	3.43	-	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ10020 MJ10021	$V_{CE(sus)}$	200 250	— —	— —	Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)		I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)		I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)		I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$				See Figure 13
Clamped Inductive SOA with Base Reverse Biased		RBSOA				See Figure 14
ON CHARACTERISTICS (1)						
DC Current Gain ($I_C = 15\text{ Adc}$, $V_{CE} = 5.0\text{ V}$)		h_{FE}	75	—	1000	—
Collector-Emitter Saturation Voltage ($I_C = 30\text{ Adc}$, $I_B = 1.2\text{ Adc}$) ($I_C = 60\text{ Adc}$, $I_B = 4.0\text{ Adc}$) ($I_C = 30\text{ Adc}$, $I_B = 1.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)		$V_{CE(sat)}$	— — —	— — —	2.2 4.0 2.4	Vdc
Base-Emitter Saturation Voltage ($I_C = 30\text{ Adc}$, $I_B = 1.2\text{ Adc}$) ($I_C = 30\text{ Adc}$, $I_B = 1.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)		$V_{BE(sat)}$	— —	— —	3.0 3.5	Vdc
Diode Forward Voltage ($I_F = 30\text{ Adc}$)		V_f	—	2.5	5.0	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)		C_{ob}	175	—	700	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	$(V_{CC} = 175\text{ Vdc}$, $I_C = 30\text{ A}$, $I_{B1} = 1.2\text{ Adc}$, $V_{BE(off)} = 5.0\text{ V}$, $t_p = 25\ \mu\text{s}$ Duty Cycle $\leq 2.0\%$).	t_d	—	0.02	0.2	μs
Rise Time		t_r	—	0.30	1.0	μs
Storage Time		t_s	—	1.0	3.5	μs
Fall Time		t_f	—	0.07	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	$(I_{CM} = 30\text{ A(pk)}$, $V_{CEM} = 200\text{ V}$, $I_{B1} = 1.2\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	1.2	3.5	μs
Crossover Time		t_c	—	0.45	2.0	μs
Storage Time	$(I_{CM} = 30\text{ A(pk)}$, $V_{CEM} = 200\text{ V}$, $I_{B1} = 1.2\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $T_C = 25^\circ\text{C}$)	t_{sv}	—	0.75	—	μs
Crossover Time		t_c	—	0.25	—	μs
Fall Time		t_{fi}	—	0.15	—	μs

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

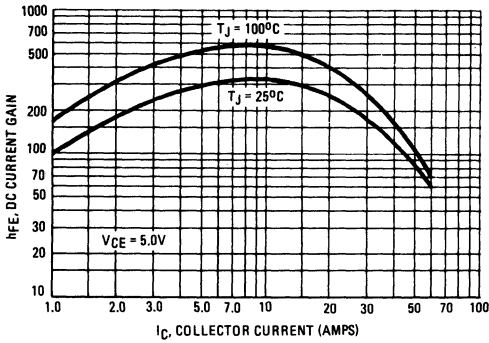


FIGURE 2 – COLLECTOR SATURATION REGION

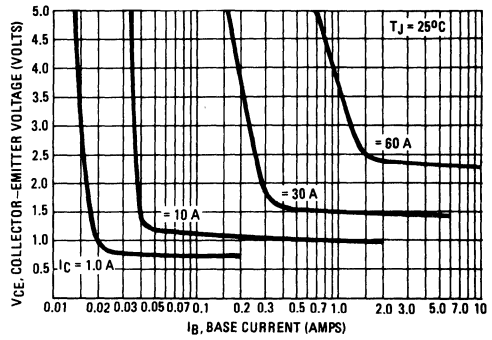


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

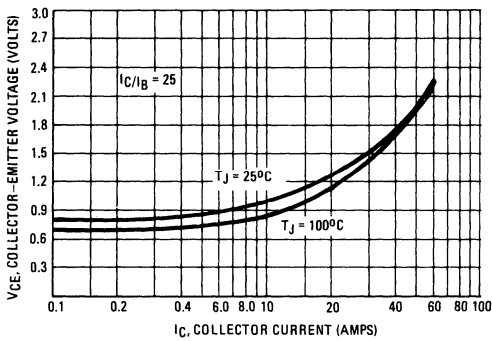


FIGURE 4 – BASE-EMITTER VOLTAGE

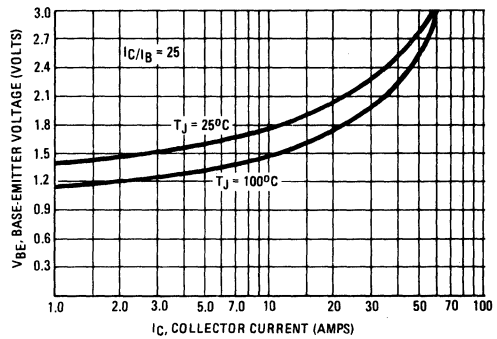


FIGURE 5 – COLLECTOR CUTOFF REGION

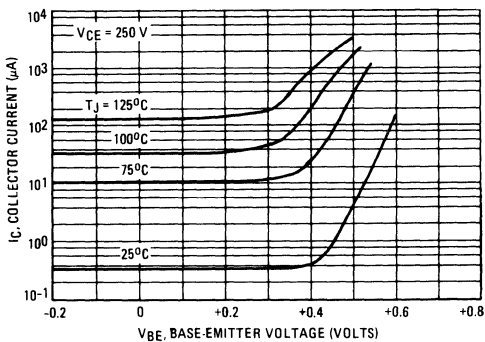


FIGURE 6 – OUTPUT CAPACITANCE

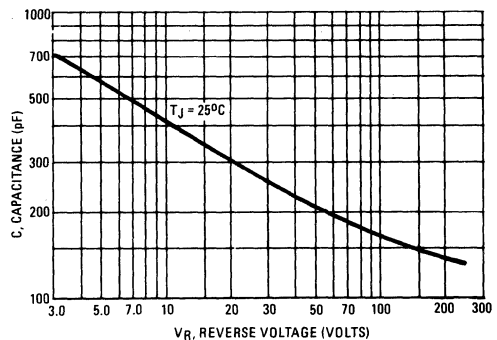


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

<p>INPUT CONDITIONS</p> <p>20 Ω 5 V PW Varied to Attain $I_C = 100 \text{ mA}$</p>	<p>RBSOA AND INDUCTIVE SWITCHING</p> <p>Adjust R1 to obtain a forced $hFE = \dots$</p> <p>Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 25 μs)</p> <p>Duty Cycle $\leq 3\%$</p>	<p>RESISTIVE SWITCHING</p> <p>TURN ON TIME TURN-OFF TIME Use inductive switching circuit as the input to the resistive test circuit.</p>
<p>CIRCUIT VALUES</p> <p>$L_{\text{coil}} = 10 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{\text{coil}} = 0.7 \Omega$ $V_{\text{clamp}} = V_{CE(\text{off})}$</p>	<p>$L_{\text{coil}} = 180 \mu\text{H}$ $R_{\text{coil}} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$</p> <p>Q1 2N2907 Q5 MJE15028 Q2 2N2222 D1 1N914 Q3 2N3762 D2 1N914 Q4 MJE15029 D3 1N914</p>	<p>$V_{CC} = 175 \text{ V}$ $R_L = 5.6 \Omega$ Pulse Width = 25 μs</p>
<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 \approx \frac{L_{\text{coil}}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{\text{coil}}(I_{CM})}{V_{\text{clamp}}}$</p> <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

*Adjust - V such that $V_{BE(\text{off})} = 5 \text{ V}$ except as required for RBSOA (Figure 14).

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

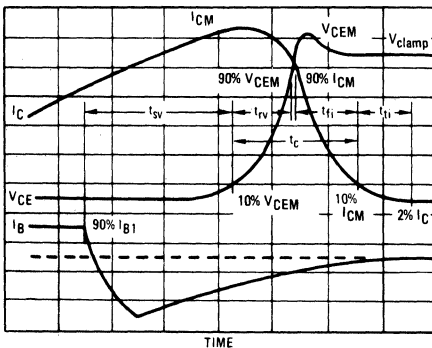


FIGURE 8 - TYPICAL PEAK REVERSE BASE CURRENT

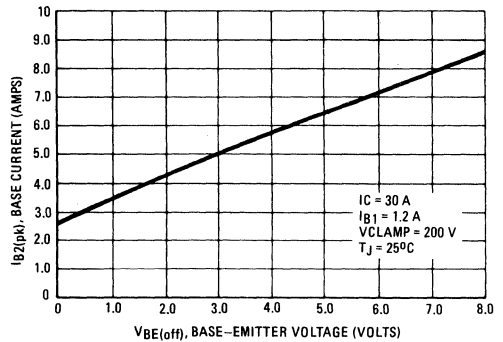
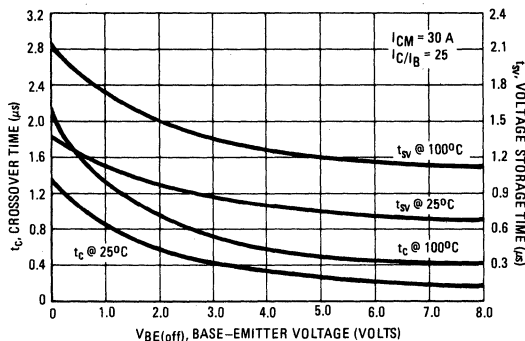


FIGURE 9 - TYPICAL INDUCTIVE SWITCHING TIMES



3

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{rv} = Voltage Rise Time, 10 – 90% V_{CEM}
- t_{fi} = Current Fall Time, 90 – 10% I_{CM}
- t_{ti} = Current Tail, 10 – 2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

FIGURE 10 – TYPICAL TURN-ON SWITCHING TIMES

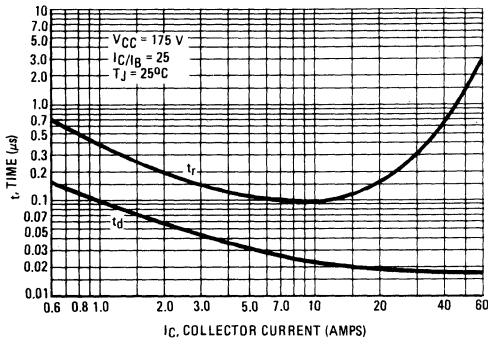


FIGURE 11 – TYPICAL TURN-OFF SWITCHING TIMES

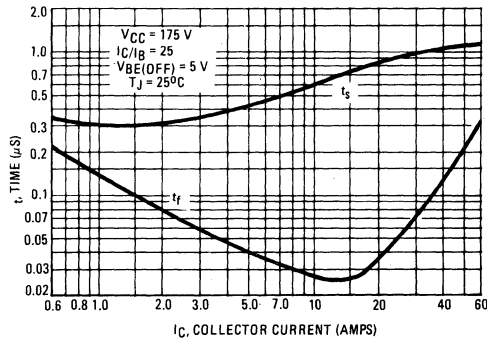
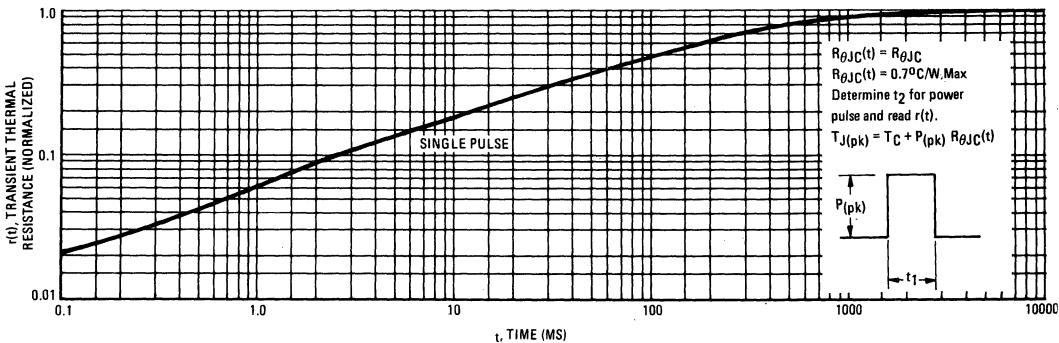


FIGURE 12 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 13 and 14, are specified for these devices under the test conditions shown.

FIGURE 13 - MAXIMUM FORWARD BIAS SAFE OPERATING AREA

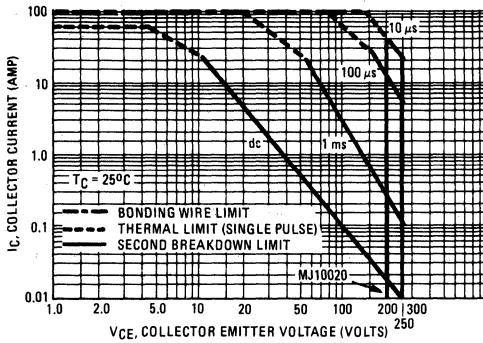
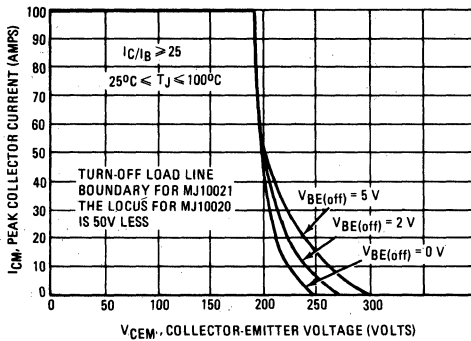


FIGURE 14 - MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

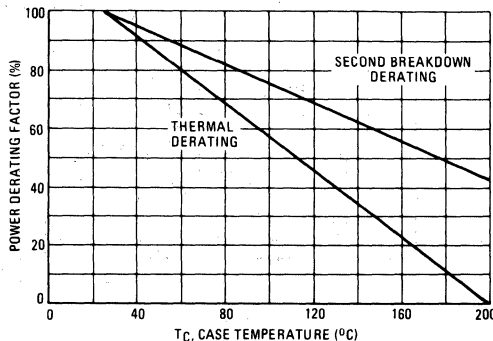
The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

FIGURE 15 - POWER DERATING



3

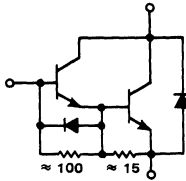
MJ10022
MJ10023

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON
WITH BASE-EMITTER SPEEDUP DIODE

The MJ10022 and MJ10023 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 150 ns Inductive Fall Time @ 25°C (Typ)
 300 ns Inductive Storage Time @ 25°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
 Reversed Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents



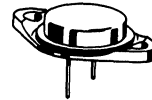
40 AMPERE

NPN SILICON
POWER DARLINGTON
TRANSISTORS

350 and 400 VOLTS
250 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



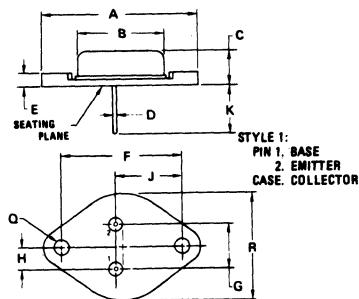
MAXIMUM RATINGS

Rating	Symbol	MJ10022	MJ10023	Unit
Collector-Emitter Voltage	V _{CEO}	350	400	V _{dc}
Collector-Emitter Voltage	V _{CEV}	450	600	V _{dc}
Emitter Base Voltage	V _{EB}	8.0		V _{dc}
Collector Current — Continuous	I _C	40		A _{dc}
— Peak (1)	I _{CM}	80		
Base Current — Continuous	I _B	20		A _{dc}
— Peak (1)	I _{BM}	40		
Total Power Dissipation @ T _C = 25°C	P _D	250		Watts
@ T _C = 100°C		143		
Derate above 25°C		1.43		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ10022 MJ10023	$V_{CE0(sus)}$	350 400	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)		I_{CEV}	— —	— —	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)		I_{CER}	—	—	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)		I_{EBO}	—	—	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 13	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 14	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 10\text{ Adc}$, $V_{CE} = 5.0\text{ V}$)	h_{FE}	50	—	600	—
Collector-Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 40\text{ Adc}$, $I_B = 5.0\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.2 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 1.2\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 1.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage ($I_F = 20\text{ Adc}$)	V_f	—	2.5	5.0	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	150	—	600	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$(V_{CC} = 250\text{ Vdc}$, $I_C = 20\text{ A}$, $I_{B1} = 1.0\text{ Adc}$, $V_{BE(off)} = 5.0\text{ V}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.03	0.2	μs
Rise Time		t_r	—	0.4	1.2	μs
Storage Time		t_s	—	0.9	2.5	μs
Fall Time		t_f	—	0.3	0.9	μs
Inductive Load, Clamped (Table 1)						
Storage Time	$(I_{CM} = 20\text{ A}$, $V_{CEM} = 250\text{ V}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	1.9	4.4	μs
Crossover Time		t_c	—	0.6	2.0	μs
Fall Time		t_{fi}	—	0.3	—	μs
Storage Time	$(I_{CM} = 20\text{ A}$, $V_{CEM} = 250\text{ V}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $T_C = 25^\circ\text{C}$)	t_{sv}	—	1.0	—	μs
Crossover Time		t_c	—	0.3	—	μs
Fall Time		t_{fi}	—	0.15	—	μs

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

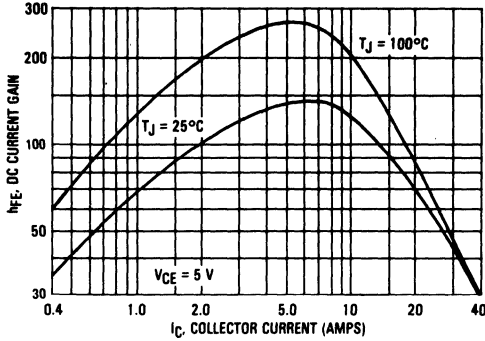


FIGURE 2 — COLLECTOR SATURATION REGION

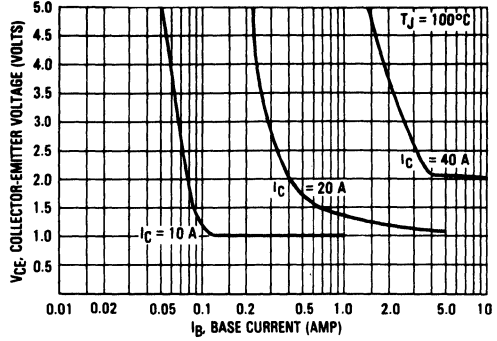


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

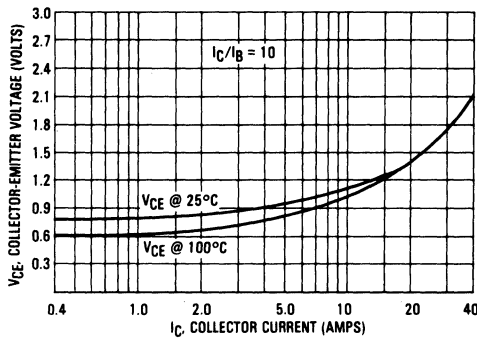


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

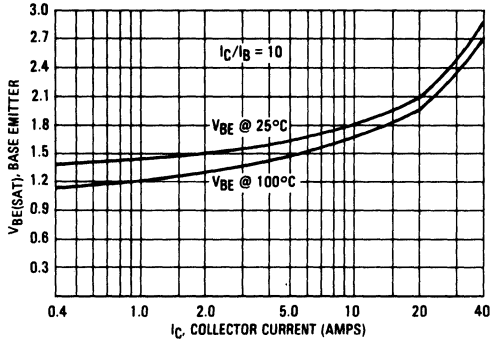


FIGURE 5 — COLLECTOR CUTOFF REGION

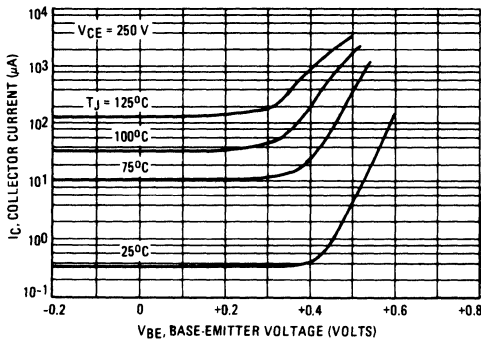


FIGURE 6 — C_{ob} OUTPUT CAPACITANCE

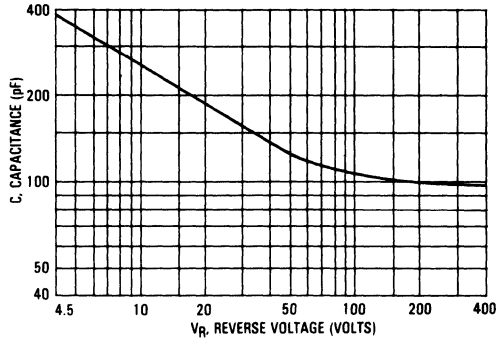


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CE0(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>20 Ω 5 V 0 PW Varied to Attain I_C = 100 mA</p>	<p>Adjust R1 to obtain a forced h_{FE} = 20 Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 25 μs) Duty Cycle < 3%</p>	<p>TURN-ON TIME</p> <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN-OFF TIME</p> <p>Use inductive switching circuit as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = V_{CE0(sus)}</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>Q1 2N2907 Q5 MJE15028 Q2 2N2222 D1 1N914 Q3 2N3762 D2 1N914 Q4 MJE15029 D3 1N914</p>	<p>V_{CC} = 250 V R_L = 12.5 Ω Pulse Width = 25 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t₃ Adjusted to Obtain I_C</p> <p>t₁ = $\frac{L_{coil}(I_{CM})}{V_{CC}}$ t₂ = $\frac{L_{coil}(I_{CM})}{V_{clamp}}$</p> <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

*Adjust - V such that V_{BE(off)} = 5 V except as required for RBSOA (Figure 14).

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

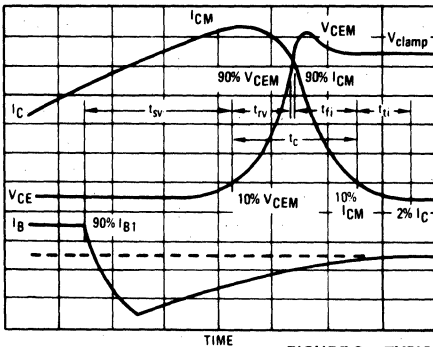


FIGURE 8 - TYPICAL PEAK REVERSE BASE CURRENT

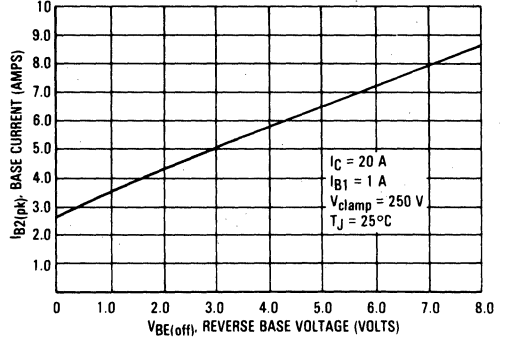
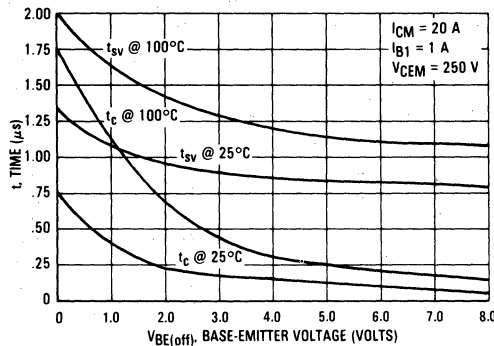


FIGURE 9 - TYPICAL INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{rv} = Voltage Rise Time, 10—90% V_{CEM}
- t_{fi} = Current Fall Time, 90—10% I_{CM}
- t_{ti} = Current Tail, 10—2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C t_c f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 10 — TYPICAL TURN-ON SWITCHING TIMES

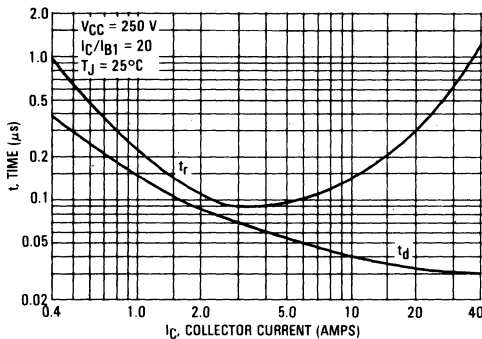


FIGURE 11 — TYPICAL TURN-OFF SWITCHING TIMES

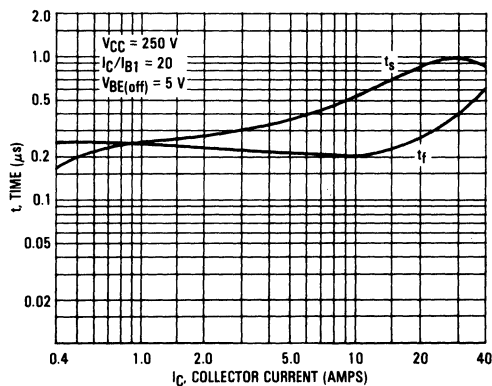
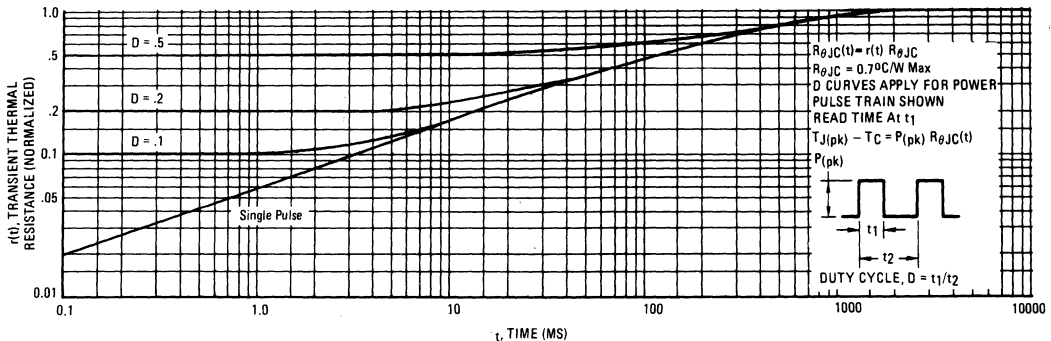


FIGURE 12 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

FIGURE 13 - MAXIMUM FORWARD BIAS SAFE OPERATING AREA

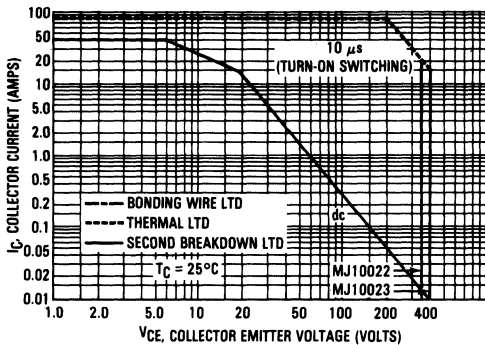
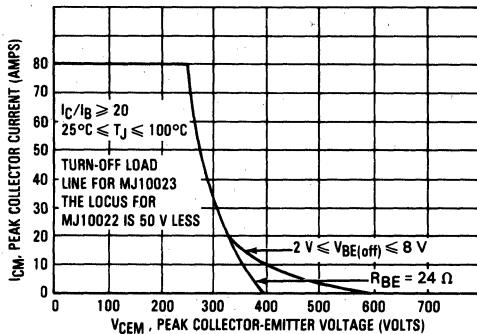


FIGURE 14 - MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

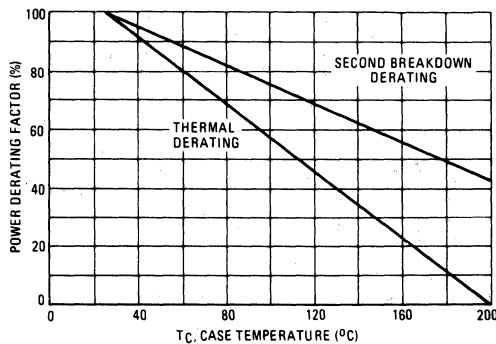
The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

FIGURE 15 - POWER DERATING



3

MJ10024
MJ10025

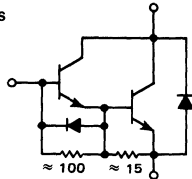
Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The MJ10024 and MJ10025 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents



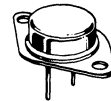
20 AMPERE

NPN SILICON
POWER DARLINGTON
TRANSISTORS

750 and 850 VOLTS
250 WATTS

Designer's Data for
"Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



MAXIMUM RATINGS

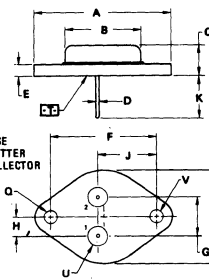
Rating	Symbol	MJ10024	MJ10025	Unit
Collector-Emitter Voltage	V_{CEO}	750	850	Vdc
Collector-Emitter Voltage	V_{CEV}	1000	1200	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous	I_C	20		Adc
— Peak (1)	I_{CM}	40		
Base Current — Continuous	I_B	10		Adc
— Peak (1)	I_{BM}	20		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250		Watts
@ $T_C = 100^\circ\text{C}$		143		
Derate above 25°C		1.43		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

STYLE 1
 PIN 1. BASE
 2. SWITTER
 CASE COLLECTOR



- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. \square IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
 ϕ .13 (0.005) \odot T V \odot
 FOR LEADS:
 ϕ .13 (0.005) \odot T V \odot \odot \odot
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.065	0.070
F	30.15 BSC		1.187 BSC	
G	10.52 BSC		0.430 BSC	
H	5.48 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.18	0.440	0.480
Q	3.81	4.18	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.18	0.150	0.165

CASE 1-05

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ10024 MJ10025	$V_{CEO(sus)}$	750 850	— —	Vdc	
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)		I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)		I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)		I_{EBO}	—	—	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 14		
Clamped Inductive SOA with base reverse biased	RBSOA		See Figure 15		

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ V}$)	h_{FE}	50	—	600	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 5.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.2 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage ($I_F = 10\text{ Adc}$)	V_f	—	1.25	4.0	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	110	—	500	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	($V_{CC} = 250\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{B1} = 1.0\text{ Adc}$, $V_{BE(off)} = 5.0\text{ V}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.03	0.3	μs
Rise Time		t_r	—	0.6	1.8	
Storage Time		t_s	—	2.0	5.0	
Fall Time		t_f	—	0.6	1.8	
Inductive Load, Clamped (Table 1)						
Storage Time	($I_{CM} = 10\text{ A}$, $V_{CEM} = 250\text{ V}$, $I_{B1} = 1.0\text{ A}$, $V_{BE(off)} = 5\text{ V}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	2.9	7.0	μs
Crossover Time		t_c	—	1.0	3.3	
Storage Time	($I_{CM} = 10\text{ A}$, $V_{CEM} = 250\text{ V}$, $I_{B1} = 1.0\text{ A}$, $R_{BE} = 24\ \Omega$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	21	50	μs
Crossover Time		t_c	—	9.0	25	
Storage Time	($I_{CM} = 10\text{ A}$, $V_{CEM} = 250\text{ V}$, $V_{BE(off)} = 5.0\text{ V}$, I_{B1} Baker Clamped [1 Ampere Source], $T_C = 100^\circ\text{C}$)	t_{sv}	—	2.2	—	μs
Crossover Time		t_c	—	0.5	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$

3

FIGURE 1 — DC CURRENT GAIN

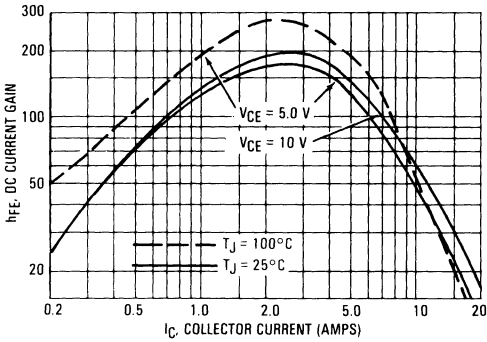


FIGURE 2 — COLLECTOR SATURATION REGION

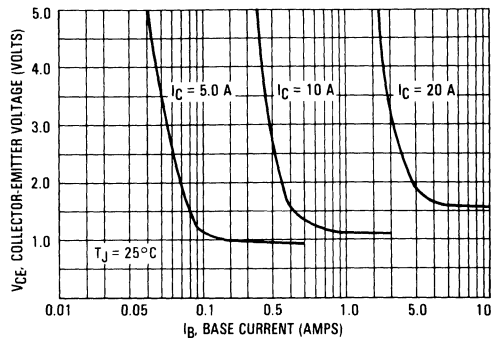


FIGURE 3 — COLLECTOR SATURATION VOLTAGE

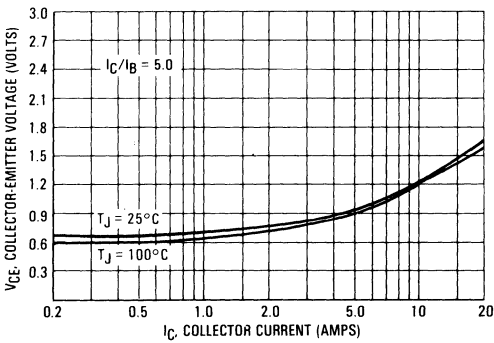


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

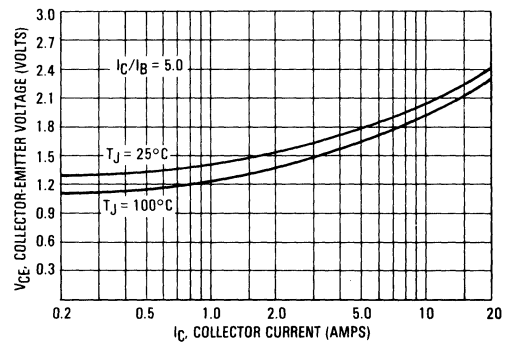


FIGURE 5 — COLLECTOR CUTOFF REGION

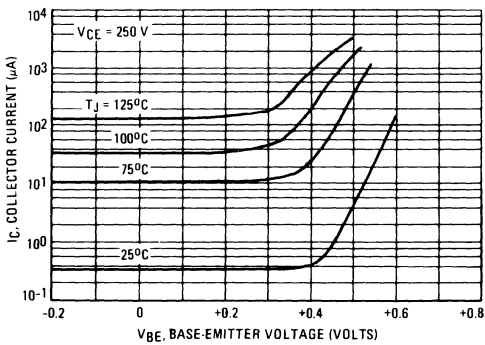


FIGURE 6 — C_{ob} OUTPUT CAPACITANCE

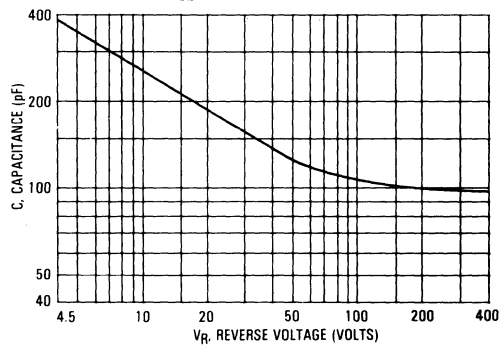


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

INPUT CONDITIONS		RBSOA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
<p>5 V 0 20 Ω 1 2 PW Varied to Attain $I_C = 100 \text{ mA}$</p>		<p>Adjust R1 to obtain a forced $h_{FE} = 10$</p> <p>Duty Cycle $\leq 3\%$</p>		<p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN-OFF TIME Use inductive switching circuit as the input to the resistive test circuit.</p>
<p>CIRCUIT VALUES</p> <p>$L_{coil} = 10 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CE(off)}$</p>		<p>$L_{coil} = 100 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$</p>		<p>Q1 2N2907 Q5 MJE1502B Q2 2N2222 D1 1N914 Q3 2N3762 D2 1N914 Q4 MJE1502B D3 1N914</p> <p>$V_{CC} = 250 \text{ V}$ $R_L = 25 \Omega$ Pulse Width = 25 μs</p>
<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>		<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> <p>$t_1 \approx \frac{L_{coil} (I_{CM})}{V_{CC}}$</p> <p>$t_2 \approx \frac{L_{coil} (I_{CM})}{V_{clamp}}$</p> <p>Test Equipment Scope – Tektronix 475 or Equivalent</p>		<p>RESISTIVE TEST CIRCUIT</p>

*Adjust – V such that $V_{BE(off)} = 5 \text{ V}$ except as required for RBSOA (Figure 14).

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

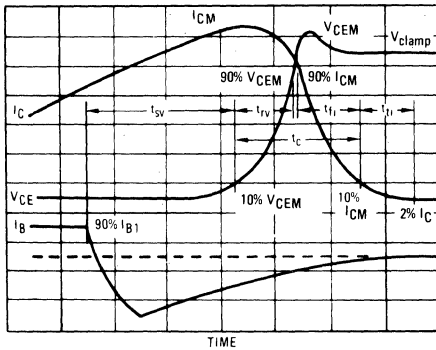


FIGURE 8 – TYPICAL PEAK REVERSE BASE CURRENT

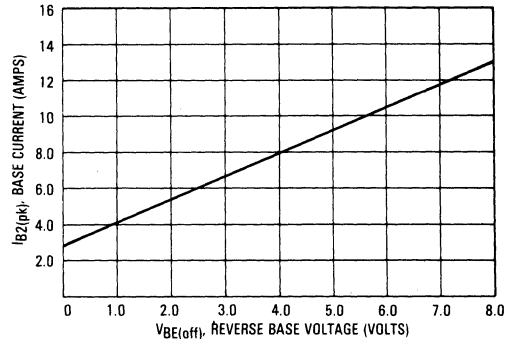


FIGURE 9 – TYPICAL INDUCTIVE SWITCHING TIMES

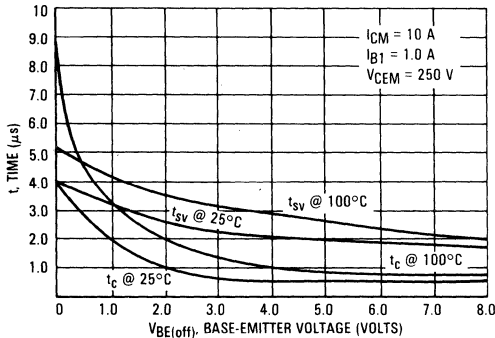
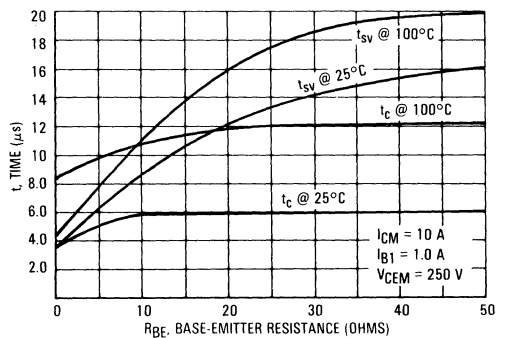


FIGURE 10 – TYPICAL INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

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- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{RV} = Voltage Rise Time, 10—90% V_{CEM}
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- t_{ti} = Current Tail, 10—2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{RV} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{SV}) which are guaranteed at 100°C.

FIGURE 11 — TYPICAL TURN-ON SWITCHING TIMES

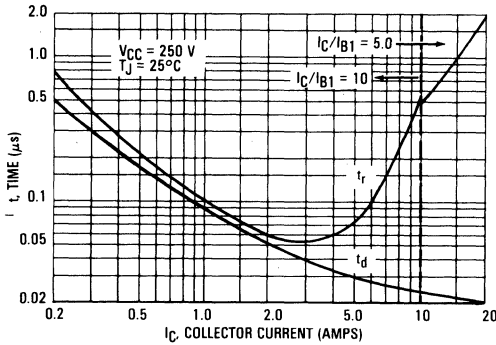


FIGURE 12 — TYPICAL TURN-OFF SWITCHING TIMES

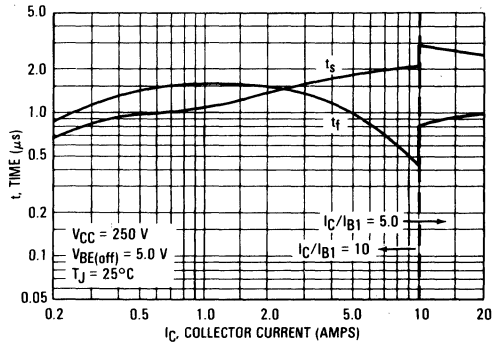
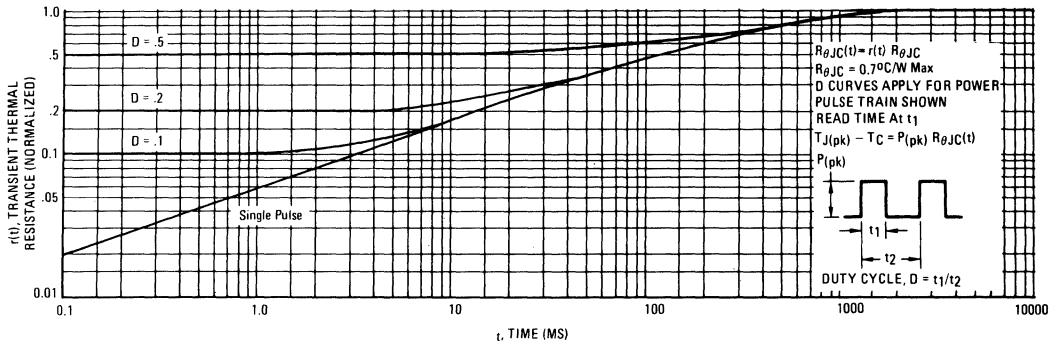


FIGURE 13 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 14 and 15 are specified for these devices under the test conditions shown.

FIGURE 14 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

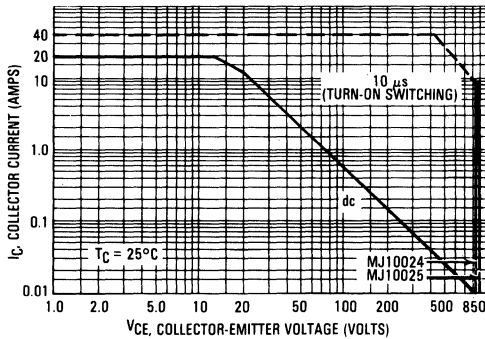
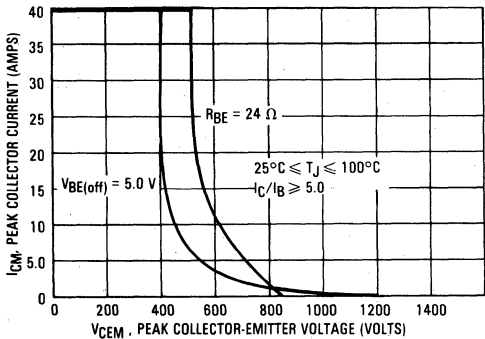


FIGURE 15 — MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

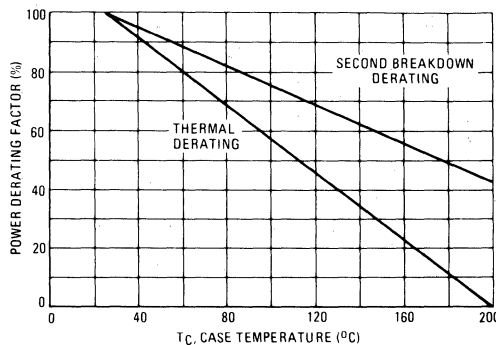
The data of Figure 14 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 14 may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

FIGURE 16 — POWER DERATING

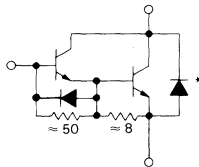
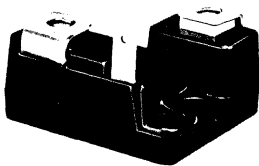
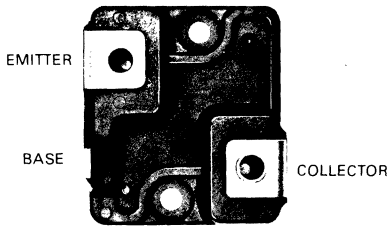


3

Designer's Data Sheet

**25 kVA ENERGY MANAGEMENT SERIES
 SWITCHMODE DARLINGTON TRANSISTORS
 25, 50 and 100 Ampere Operating Current**

These Darlington transistors are designed for industrial service under practical operating environments requiring fast switching speed for highly efficient systems operating at high frequency such as inverters, PWM controllers and other high frequency systems operating from 120, 230 and 460 V lines.



*Emitter-Collector Diode is a fast recovery high power diode.
 Note: The 8 ohm resistor is not included in the MJ10044 and MJ10047.

MAXIMUM RATINGS

Mechanical Ratings			
Rating	Value	Unit	
Mounting Torque (To heat sink with 6-32 Screw) (Note 1)	8.0	in.-lb	
Lead Torque (Lead to bus with 5 mm Screw) (Note 2)	20	in.-lb	
Per Unit Weight	41	grams	

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.5	$^{\circ}C/W$
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Mica Insulators available as separate items.
 0.003" thick. Motorola Part Number 14CSB12387B003.

Notes:

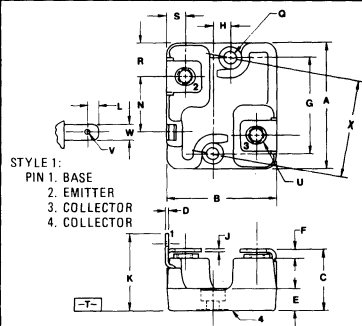
1. A Belleville washer of 0.281" O.D., 0.138" I.D., 0.013" thick and 43 pounds flat is recommended.
2. The maximum penetration of the screw should be limited to 0.50".
3. To adapt the collector and emitter terminals to quick connect terminals, AMP 250 Series Faston tab P/N 61499-1 is suggested.
4. The mounting holes of this package are compatible with TO-204 (formerly TO-3) mounting holes.

MJ10041
MJ10044
MJ10047

**25, 50, and 100 AMPERE
 NPN SILICON
 POWER DARLINGTON
 TRANSISTOR
 250, 450 and 850 VOLTS
 250 WATTS**

**Designer's Data for
 "Worst-Case" Conditions**

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst-case" design.



NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
 $\pm \varnothing 0.25 (0.010) \text{ (M)} \text{ T A } \text{ (B)} \text{ (C)}$
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
4. CONTROLLING DIMENSION: INCH EXCEPT FOR METRICALLY THREADED INSERTS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.11	40.13	1.540	1.580
B	33.93	34.95	1.336	1.376
C	—	20.32	—	0.800
D	0.68	0.83	0.027	0.033
E	8.30	8.81	0.327	0.347
F	—	4.44	—	0.175
G	29.67 BSC		1.168 BSC	
H	5.08 BSC		0.200 BSC	
J	0.93	1.09	0.037	0.043
K	—	25.40	—	1.000
L	2.92	3.30	0.115	0.130
N	17.14	13.39	0.675	0.685
Q	3.73	3.88	0.147	0.153
R	10.41	10.79	0.410	0.425
S	5.84	6.35	0.230	0.250
U	M5.8 (METRIC THRD)			
V	1.27	1.52	0.050	0.060
W	4.69	4.85	0.185	0.191
X	30.15 BSC		1.187 BSC	

CASE 353-01

MJ10041, MJ10044, MJ10047

MAXIMUM RATINGS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	MJ10041	MJ10044	MJ10047	Unit
Collector-Emitter Voltage ($I_B = 0$)	V_{CEO}	850	450	250	Vdc
Collector-Emitter Voltage ($R_{BE} = 10$ Ohms)	V_{CER}	900	500	300	Vdc
Collector-Base Voltage	V_{CB}	900	500	300	Vdc
Emitter-Base Voltage	V_{EB}	8.0			Vdc
Collector Current — Operating ($T_C = 115^\circ\text{C}$) ($T_C = 85^\circ\text{C}$) ($T_C = 85^\circ\text{C}$)	$I_{C(op)}$	25 — —	— 50 —	— — 100*	A
Collector Current — Continuous — Peak Repetitive — Peak Nonrepetitive	I_C	37.5 75 125	75 150 250	100 300 500	A
Base Current — Continuous — Peak Nonrepetitive	I_B	25 50			A
Total Device Dissipation Derate above $T_C = 25^\circ\text{C}$ For 1-minute overload	P_D	250 2.0 333			Watts W/ $^\circ\text{C}$ Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}	-55 to +150 -55 to 200			$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 125$ mAdc)	MJ10041 MJ10044 MJ10047	$V_{CEO(sus)}$	850 450 250	— — —	Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CB}, V_{BE(off)} = 1.5$ Vdc) ($V_{CE} = \text{Rated } V_{CB}, V_{BE(off)} = 1.5$ Vdc, $T_C = 150^\circ\text{C}$)		I_{CEV}	— —	2.0 10	mA
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CER}, R_{BE} = 10 \Omega, T_C = 100^\circ\text{C}$)		I_{CER}	—	10	mA
Emitter Cutoff Current ($V_{EB} = 4.0$ Vdc, $I_C = 0$)	MJ10041 MJ10044 MJ10047	I_{EBO}	— —	500 2.5	mA

SAFE OPERATING AREA

Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figures 32, 34 & 36
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figures 33, 35 & 37
Overload Safe Operating Area	OLSOA	See Figures 38, 39, 40, 41, 42 & 43

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0, f_{test} = 1.0$ kHz)	C_{ob}	—	2000	pF
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(1) Pulse Test. Pulse width of 300 μs , duty cycle $\leq 2.0\%$.

*This rating is with a 50% duty cycle, and is limited by power dissipation. Higher operating currents are allowable at lower duty cycles.

MJ10041, MJ10044, MJ10047

ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
MJ10041				
DC Current Gain ($I_C = 25 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 25 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$)	h_{FE}	25 40	— —	
Collector-Emitter Saturation Voltage ($I_C = 25 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$) ($I_C = 37.5 \text{ Adc}$, $I_B = 7.5 \text{ Adc}$) ($I_C = 25 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	2.0 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 25 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$) ($I_C = 25 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	3.0 3.0	Vdc
MJ10044				
DC Current Gain ($I_C = 50 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 50 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$)	h_{FE}	50 60	— —	
Collector-Emitter Saturation Voltage ($I_C = 50 \text{ Adc}$, $I_B = 1.67 \text{ Adc}$) ($I_C = 75 \text{ Adc}$, $I_B = 6.0 \text{ Adc}$) ($I_C = 50 \text{ Adc}$, $I_B = 1.67 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	2.0 3.3 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 50 \text{ Adc}$, $I_B = 1.67 \text{ Adc}$) ($I_C = 50 \text{ Adc}$, $I_B = 1.67 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	3.0 3.0	Vdc
MJ10047				
DC Current Gain ($I_C = 100 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 100 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$)	h_{FE}	75 90	— —	
Collector-Emitter Saturation Voltage ($I_C = 100 \text{ Adc}$, $I_B = 2.75 \text{ Adc}$) ($I_C = 100 \text{ Adc}$, $I_B = 2.75 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— —	2.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 100 \text{ Adc}$, $I_B = 2.75 \text{ Adc}$) ($I_C = 100 \text{ Adc}$, $I_B = 2.75 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	3.5 3.5	Vdc

(1) Pulse Test: Pulse width of 300 μs , duty cycle $\leq 2.0\%$.

3

ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit	
SWITCHING CHARACTERISTICS						
MJ10041						
Resistive Load						
Delay Time	$(V_{CC} = 300 \text{ Vdc}$, $I_C = 25 \text{ A}$, $I_{B1} = 2.5 \text{ A}$, $V_{BE(OFF)} = 5.0 \text{ V}$, $t_D = 50 \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.03	μs	
Rise Time		t_r	—	1.2		
Storage Time		t_s	—	3.3		
Fall Time		t_f	—	1.5		
Inductive Load, Clamped						
Storage Time	$(I_{CM} = 25 \text{ A}$, $V_{CEM} = 300 \text{ V}$, $V_{BE(OFF)} = 5.0 \text{ V}$, $I_{B1} = 2.5 \text{ A}$)	$T_J = 100^\circ\text{C}$	t_{sv}	—	5.0	μs
Crossover Time			t_c	—	3.0	
Storage Time		$T_J = 25^\circ\text{C}$	t_{sv}	—	3.5	
Crossover Time			t_c	—	1.5	

MJ10041, MJ10044, MJ10047

ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit		
SWITCHING CHARACTERISTICS							
MJ10044							
Resistive Load							
Delay Time	$(V_{CC} = 250\text{ Vdc}, I_C = 50\text{ A}, I_{B1} = 1.67\text{ A}, V_{BE(OFF)} = 5.0\text{ V}, t_p = 50\ \mu\text{s}, \text{Duty Cycle} \leq 2.0\%)$	t_d	—	0.03	0.25	μs	
Rise Time		t_r	—	0.9	3.0		
Storage Time		t_s	—	1.5	3.8		
Fall Time		t_f	—	0.4	1.3		
Inductive Load, Clamped							
Storage Time	$(I_{CM} = 50\text{ A}, V_{CEM} = 250\text{ V}, V_{BE(OFF)} = 5.0\text{ V}, I_{B1} = 1.67\text{ A})$	$T_J = 100^\circ\text{C}$	t_{sv}	—	2.5	7.5	μs
Crossover Time		t_c	—	0.8	3.0		
Storage Time	$T_J = 25^\circ\text{C}$	t_{sv}	—	1.5	3.8		
Crossover Time	t_c	—	0.5	1.5			
MJ10047							
Resistive Load							
Delay Time	$(V_{CC} = 150\text{ Vdc}, I_C = 100\text{ A}, I_{B1} = 2.75\text{ A}, V_{BE(OFF)} = 5.0\text{ V}, t_p = 50\ \mu\text{s}, \text{Duty Cycle} \leq 2.0\%)$	t_d	—	0.035	0.25	μs	
Rise Time		t_r	—	1.2	4.0		
Storage Time		t_s	—	1.4	4.0		
Fall Time		t_f	—	0.25	1.0		
Inductive Load, Clamped							
Storage Time	$(I_{CM} = 100\text{ A}, V_{CEM} = 150\text{ V}, V_{BE(OFF)} = 5.0\text{ V}, I_{B1} = 2.75\text{ A})$	$T_J = 100^\circ\text{C}$	t_{sv}	—	2.8	8.0	μs
Crossover Time		t_c	—	1.4	4.0		
Storage Time	$T_J = 25^\circ\text{C}$	t_{sv}	—	2.2	6.5		
Crossover Time	t_c	—	1.0	3.0			
C-E DIODE CHARACTERISTICS							
Power Dissipation ($I_B = 0$)	P_D	—	—	125	W		
Single Cycle Surge Current (60 Hz)	I_{FSM}	—	—	250	Apk		
Forward Voltage (1)	V_F	—	—	—	Vdc		
($I_F = 25\text{ Adc}$)	MJ10041	—	2.7	5.0			
($I_F = 50\text{ Adc}$)	MJ10044	—	1.7	5.0			
($I_F = 100\text{ Adc}$)	MJ10047	—	2.5	5.0			
Reverse Recovery Time	t_{rr}	—	—	—	μs		
($I_F = 25\text{ Adc}, di/dt = 25\text{ A}/\mu\text{s}$)	MJ10041	—	0.2	1.0			
($I_F = 50\text{ Adc}, di/dt = 50\text{ A}/\mu\text{s}$)	MJ10044	—	0.4	1.0			
($I_F = 100\text{ Adc}, di/dt = 100\text{ A}/\mu\text{s}$)	MJ10047	—	0.4	1.0			
Reverse Recovery Current	$I_{RM(rec)}$	—	—	—	A		
($I_F = 25\text{ A}, di/dt = 25\text{ A}/\mu\text{s}$)	MJ10041	—	3.5	12.5			
($I_F = 50\text{ A}, di/dt = 50\text{ A}/\mu\text{s}$)	MJ10044	—	10	25			
($I_F = 100\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$)	MJ10047	—	25	50			
Forward Turn-On Time (Compliance Voltage = 250 V)	t_{on}	—	—	—	μs		
($I_F = 25\text{ Adc}$)	MJ10041	—	0.1	1.0			
($I_F = 50\text{ Adc}$)	MJ10044	—	0.1	0.5			
($I_F = 100\text{ Adc}$)	MJ10047	—	0.4	1.0			

(1) Pulse Test: Pulse width of 300 μs , duty cycle $\leq 2.0\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

MJ10041

FIGURE 1 — DC CURRENT GAIN

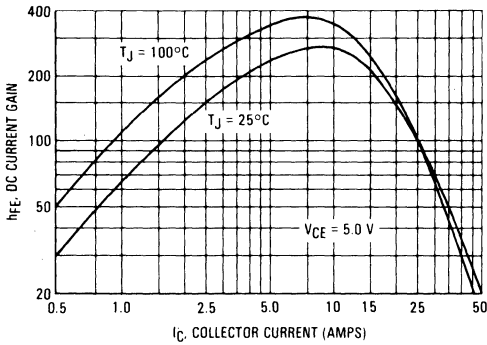
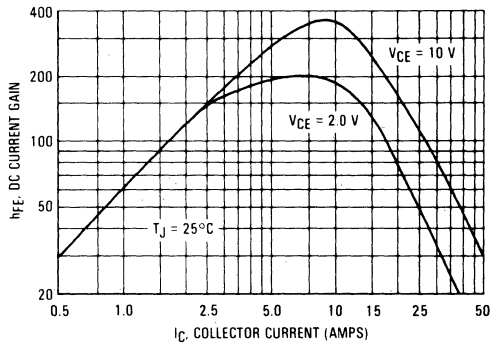


FIGURE 2 — DC CURRENT GAIN



MJ10044

FIGURE 3 — DC CURRENT GAIN

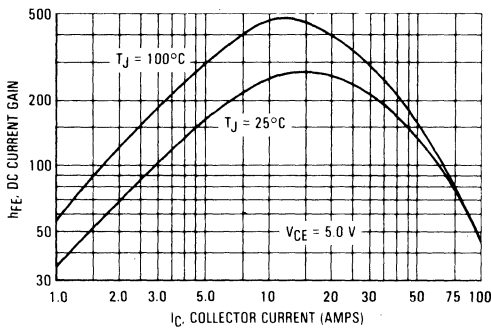
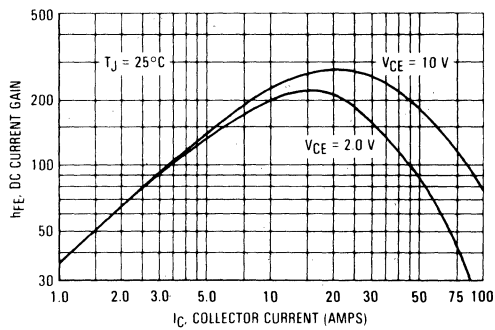


FIGURE 4 — DC CURRENT GAIN



MJ10047

FIGURE 5 — DC CURRENT GAIN

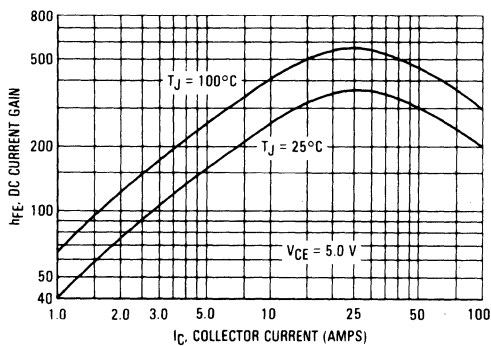
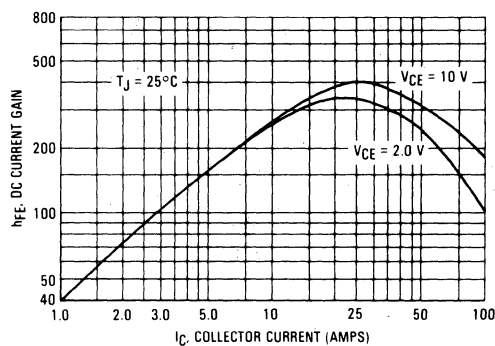


FIGURE 6 — DC CURRENT GAIN



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10041

FIGURE 7 — DC CURRENT GAIN

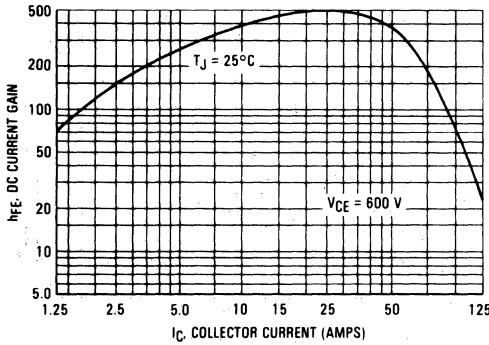
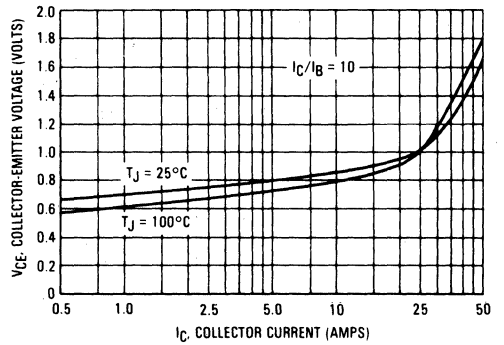


FIGURE 8 — COLLECTOR SATURATION VOLTAGE



MJ10044

FIGURE 9 — DC CURRENT GAIN

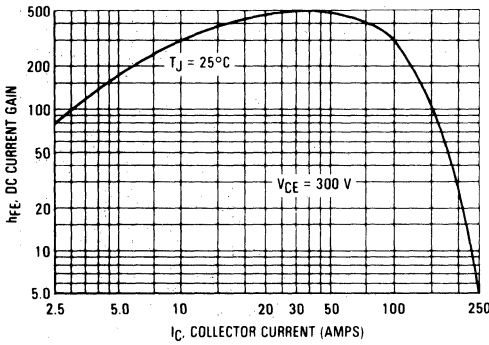
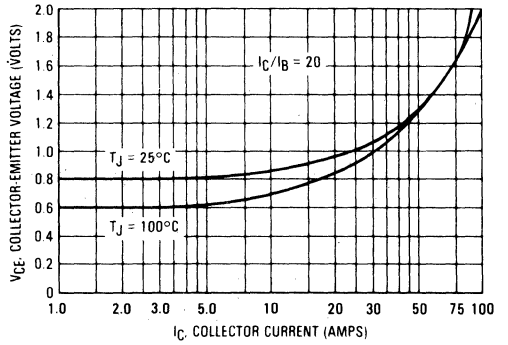


FIGURE 10 — COLLECTOR SATURATION REGION



MJ10047

FIGURE 11 — DC CURRENT GAIN

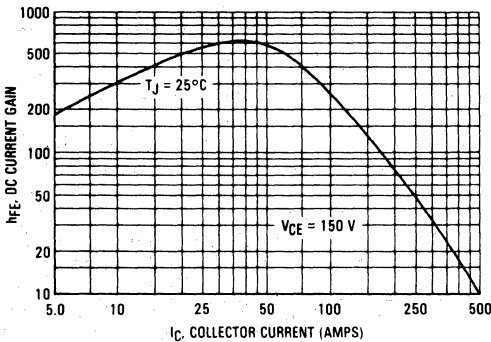
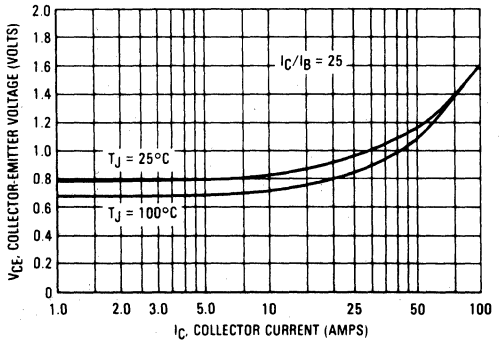


FIGURE 12 — COLLECTOR SATURATION REGION



3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10041

FIGURE 13 — BASE-EMITTER SATURATION VOLTAGE

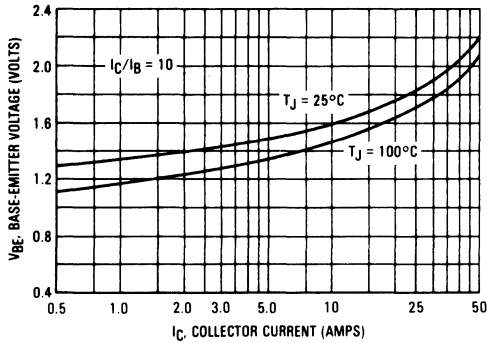
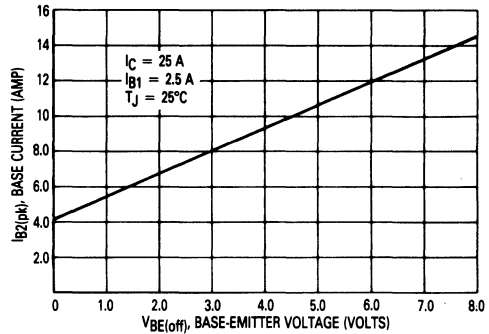


FIGURE 14 — PEAK REVERSE BASE CURRENT



MJ10044

FIGURE 15 — BASE-EMITTER SATURATION VOLTAGE

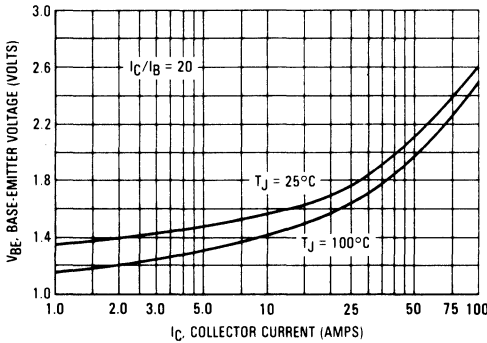
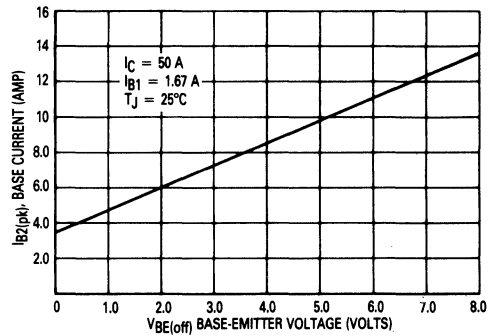


FIGURE 16 — PEAK REVERSE BASE CURRENT



MJ10047

FIGURE 17 — BASE-EMITTER SATURATION VOLTAGE

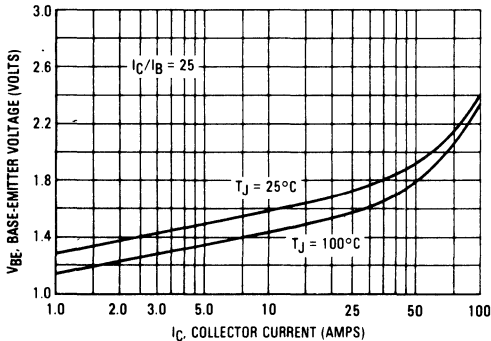
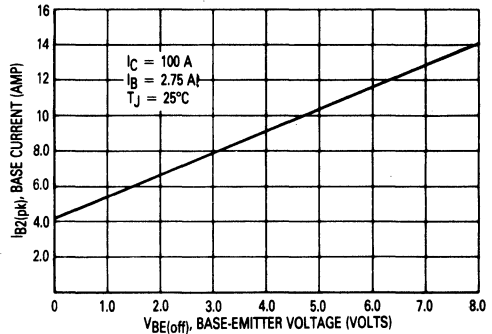


FIGURE 18 — PEAK REVERSE BASE CURRENT



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10041

FIGURE 19 — TYPICAL INDUCTIVE SWITCHING TIMES

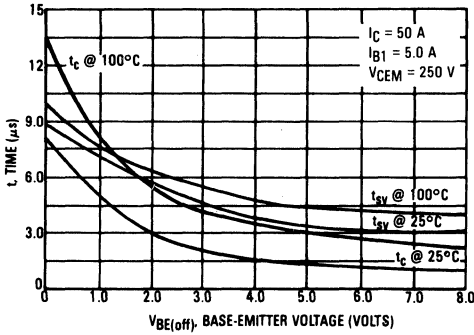
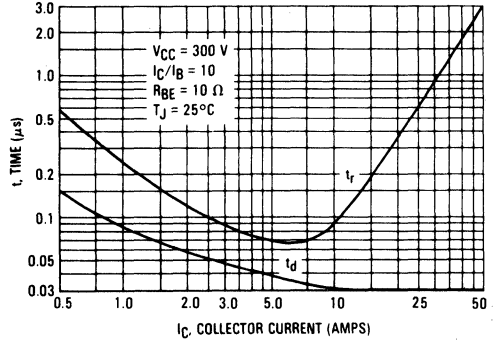


FIGURE 20 — TYPICAL TURN-ON SWITCHING TIMES



MJ10044

FIGURE 21 — TYPICAL INDUCTIVE SWITCHING TIMES

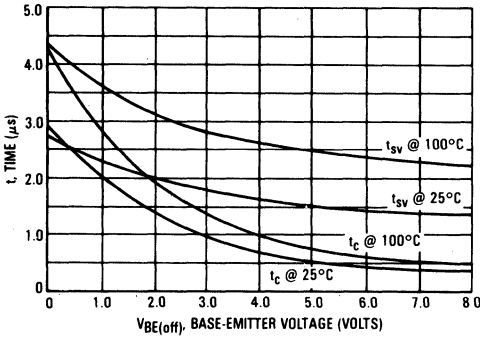
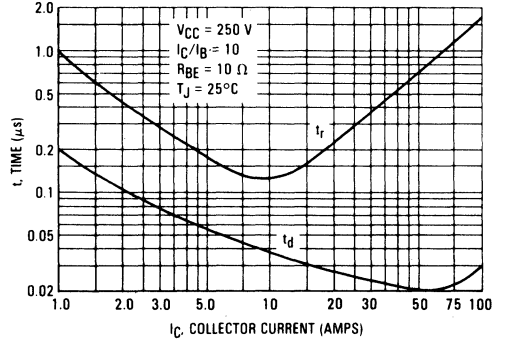


FIGURE 22 — TYPICAL TURN-ON SWITCHING TIMES



MJ10047

FIGURE 23 — TYPICAL INDUCTIVE SWITCHING TIMES

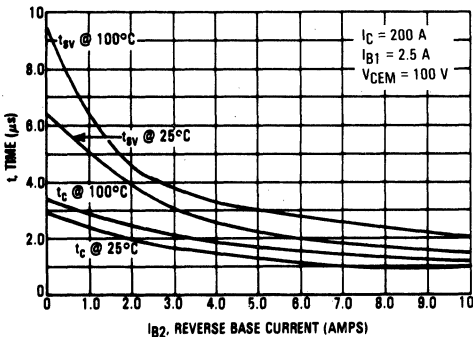
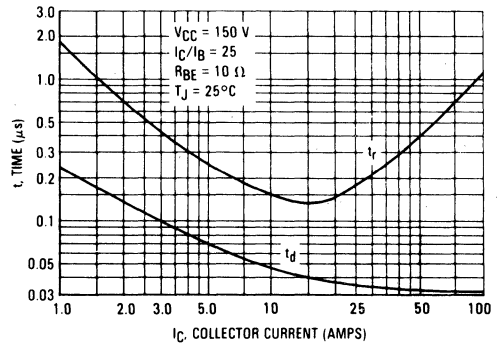


FIGURE 24 — TYPICAL TURN-ON SWITCHING TIMES



3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 25 — TYPICAL TURN-OFF SWITCHING TIMES
MJ10041

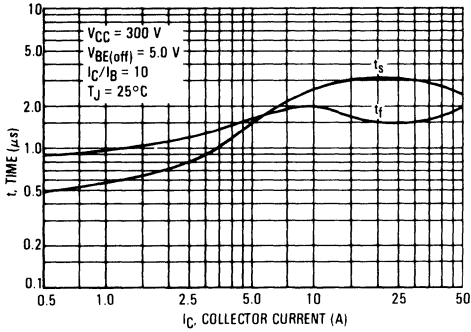


FIGURE 26 — EMITTER-COLLECTOR DIODE
FORWARD VOLTAGE

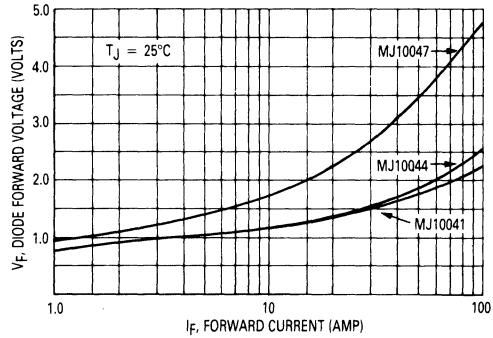


FIGURE 27 — TYPICAL TURN-OFF SWITCHING TIMES
MJ10044

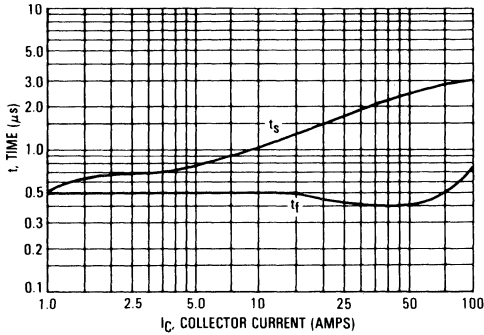


FIGURE 28 — POWER DERATING

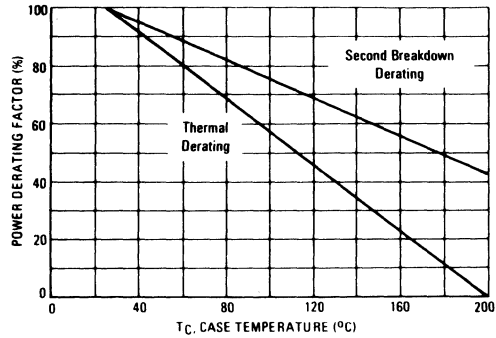


FIGURE 29 — TYPICAL TURN-OFF SWITCHING TIMES
MJ10047

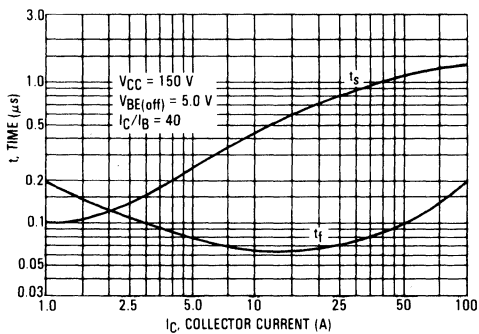


TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS		<p>DRIVER SCHEMATIC</p> <p>For inductive loads pulse width is adjusted to obtain specified I_C</p>	<p>TURN ON TIME</p> <p>I_{B1} adjusted to obtain the forced hFE desired</p> <p>TURN-OFF TIME</p> <p>Use inductive switching circuit as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 10 mH V_{CC} = 10 V</p> <p>R_{coil} = 0.7 Ω</p> <p>V_{clamp} = V_{CEO(sus)}</p>	<p>L_{coil} = 5.0 μH</p> <p>V_{CC} = 20 V</p>	<p>V_{CC} = 150 to 300 V</p> <p>Pulse Width = 50 μs</p> <p>Adjust R_L for I_{CM}</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> <p>t₁ ~ $\frac{L_{coil} (I_{CM})}{V_{CC}}$</p> <p>t₂ ~ $\frac{L_{coil} (I_{CM})}{V_{clamp}}$</p> <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

*Adjust — V such that V_{BE(off)} = 5.0 V except as required for RBSOA.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCH-MODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
- t_{fi} = Current Fall Time, 90–10% I_{CM}
- t_{ti} = Current Tail, 10–2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching wave-

form is shown in Figure 30 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = \frac{1}{2} V_{CC} I_C (t_c) f$$

In general, t_{rv} + t_{fi} = t_c. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 30 — INDUCTIVE SWITCHING MEASUREMENTS

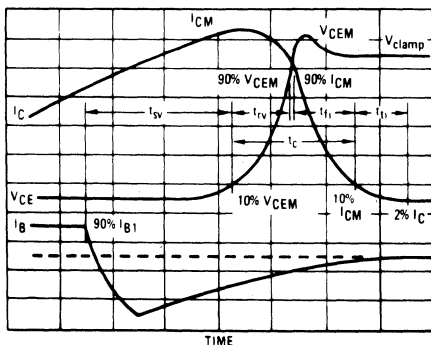
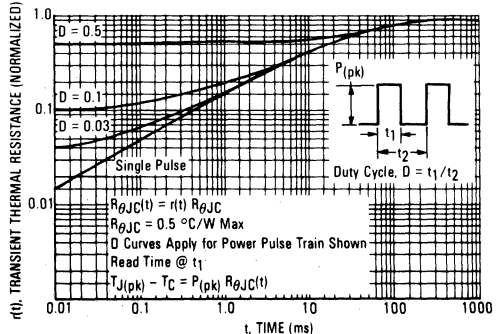


FIGURE 31 — THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

MJ10041

FIGURE 32 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

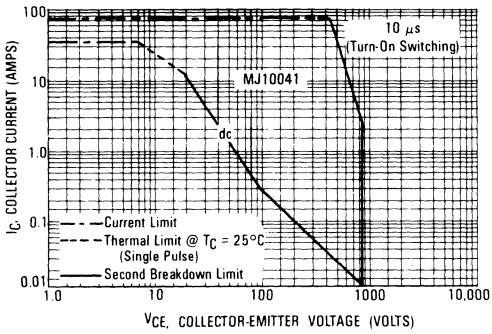
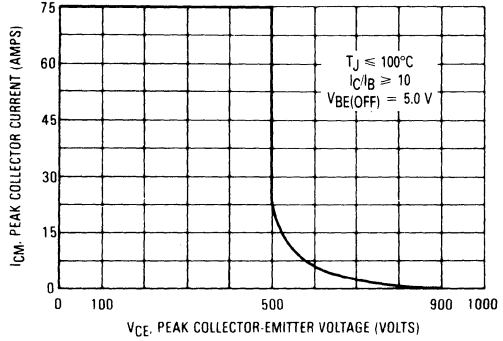


FIGURE 33 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



MJ10044

FIGURE 34 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

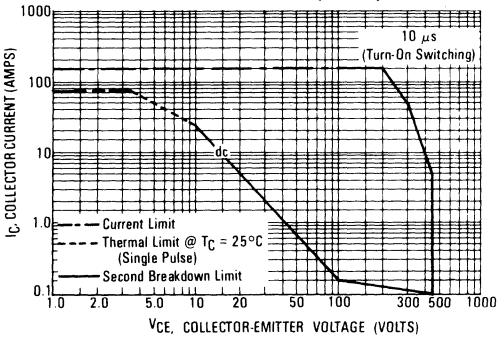
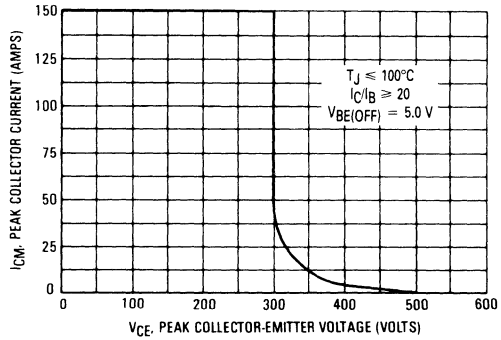


FIGURE 35 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



MJ10047

FIGURE 36 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

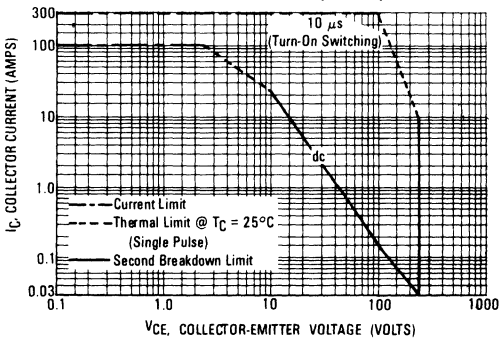
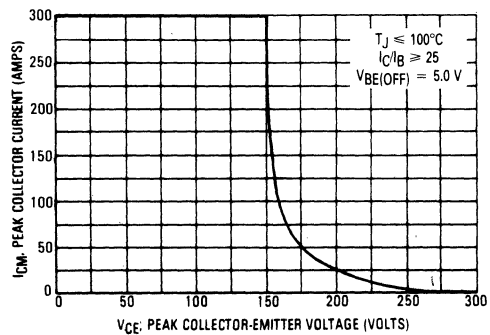


FIGURE 37 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



3

OVERLOAD CHARACTERISTICS

MJ10041

FIGURE 38 — OVERLOAD SAFE OPERATING AREA
TYPE I (OLSOA)

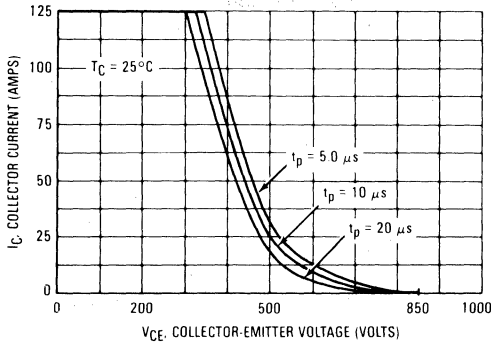
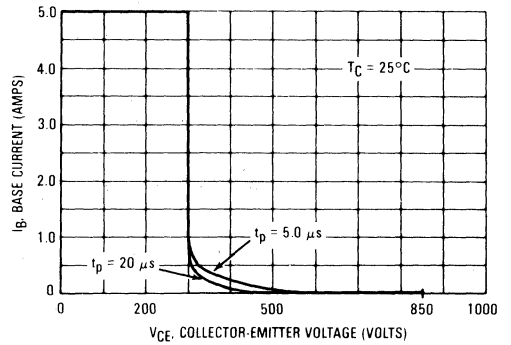


FIGURE 39 — OVERLOAD SAFE OPERATING AREA
TYPE II (OLSOA)



MJ10044

FIGURE 40 — OVERLOAD SAFE OPERATING AREA
TYPE I (OLSOA)

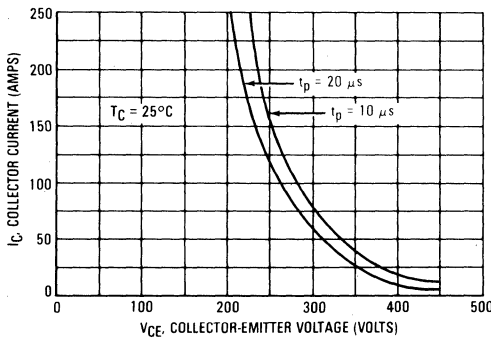
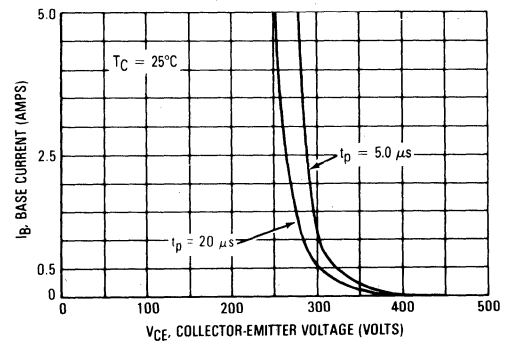


FIGURE 41 — OVERLOAD SAFE OPERATING AREA
TYPE II (OLSOA)



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MJ10047

FIGURE 42 — OVERLOAD SAFE OPERATING AREA
TYPE I (OLSOA)

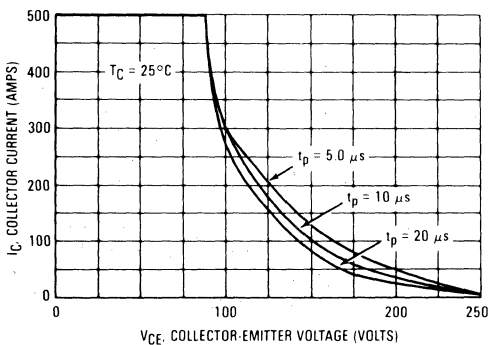
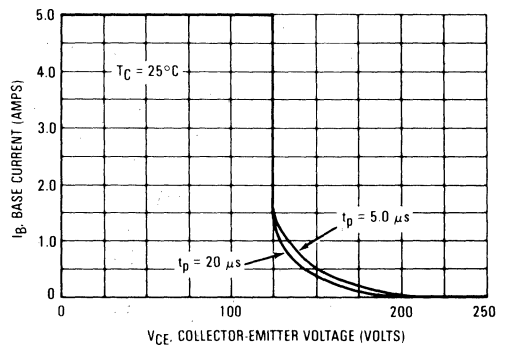


FIGURE 43 — OVERLOAD SAFE OPERATING AREA
TYPE II (OLSOA)



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 32, 34, and 36 are based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on these figures may be found at any case temperature by using the appropriate curve on Figure 28.

$T_{J(pk)}$ may be calculated from the data in Figure 31. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figures 33, 35 and 37 give the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in these figures adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figures 38, 40 and 42 depict the Type I OLSOA rating for these devices. Maximum allowable collector-emitter voltage versus collec-

tor current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, these figures define the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 44) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

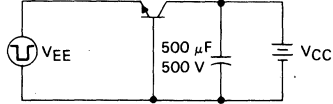
This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figures 39, 41 and 43 are measured in the circuit shown in Figure 45, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NON-REPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for these devices is 100 occurrences. Another factor is the form of turn-off bias. For these devices, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5.0\text{ V}$ (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

OVERLOAD SAFE OPERATING TEST CIRCUITS

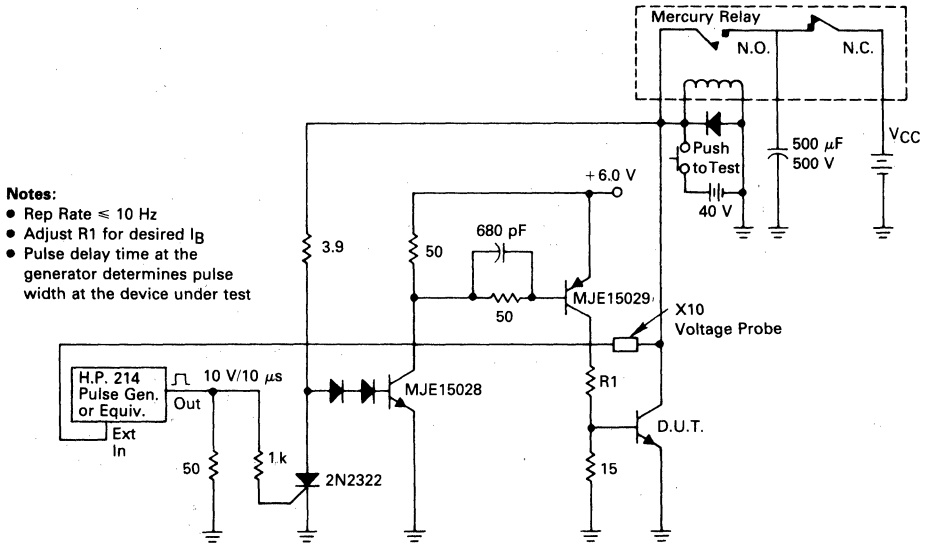
FIGURE 44 — OVERLOAD SOA TEST CIRCUIT TYPE I (OLSOA)



Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

FIGURE 45 — OVERLOAD SOA TEST CIRCUIT TYPE II (OLSOA)



Notes:

- Rep Rate ≤ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test

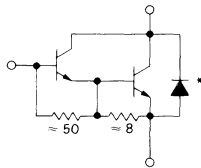
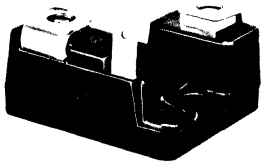
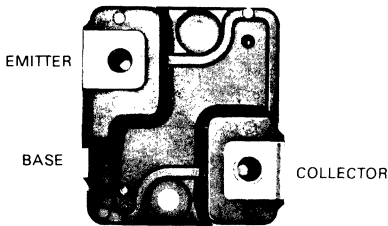
3

MJ10042
MJ10045
MJ10048

Designer's Data Sheet

25 KVA ENERGY MANAGEMENT SERIES
SWITCHMODE DARLINGTON TRANSISTORS
25, 50 and 100 Ampere Operating Current

These Darlington transistors are designed for industrial service under practical operating environments found in switching high power inductive loads off 120, 230 and 460 Volt lines.



*Emitter-Collector Diode is a high power diode.

MAXIMUM RATINGS

Mechanical Ratings			
Rating	Value	Unit	
Mounting Torque (To heat sink with 6-32 Screw) (Note 1)	8.0	in.-lb	
Lead Torque (Lead to bus with 5 mm Screw) (Note 2)	20	in.-lb	
Per Unit Weight	41	grams	

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case, $R_{\theta JC}$	0.5	$^{\circ}C/W$
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Mica Insulators available as separate items.
 0.003" thick. Motorola Part Number 14CSB12387B003.

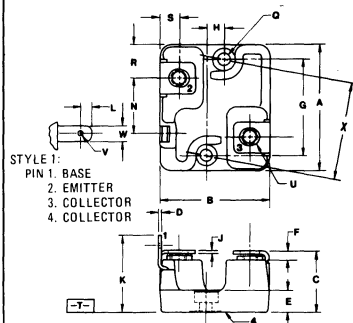
Notes:

1. A Belleville washer of 0.281" O.D., 0.138" I.D., 0.013" thick and 43 pounds flat is recommended.
2. The maximum penetration of the screw should be limited to 0.50".
3. To adapt the collector and emitter terminals to quick connect terminals, AMP 250 Series Faston tab P/N 61499-1 is suggested.
4. The mounting holes of this package are compatible with TO-204 (formerly TO-3) mounting holes.

25, 50, and 100 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
250, 450 and 850 VOLTS
250 WATTS

Designer's Data for
"Worst-Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristics boundaries—are given to facilitate "worst-case" design.



NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
 $\pm \begin{matrix} \text{A} & \text{B} & \text{C} & \text{D} & \text{E} & \text{F} \end{matrix} \begin{matrix} \text{A} & \text{B} & \text{C} & \text{D} & \text{E} & \text{F} \end{matrix}$
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
4. CONTROLLING DIMENSION: INCH EXCEPT FOR METRICALLY THREADED INSERTS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.11	40.13	1.540	1.580
B	33.93	34.95	1.336	1.376
C	—	20.32	—	0.800
D	0.68	0.83	0.027	0.033
E	8.30	8.81	0.327	0.347
F	—	4.44	—	0.175
G	29.67	BSC	1.168	BSC
H	5.08	BSC	0.200	BSC
J	0.93	1.09	0.037	0.043
K	—	25.40	—	1.000
L	2.92	3.30	0.115	0.130
N	17.14	17.39	0.675	0.685
Q	3.73	3.88	0.147	0.153
R	10.41	10.79	0.410	0.425
S	5.84	6.35	0.230	0.250
U	M5	8 (METRIC THRD)		
V	1.27	1.52	0.050	0.060
W	4.69	4.85	0.185	0.191
X	38.15	BSC	1.187	BSC

CASE 353-01

MJ10042, MJ10045, MJ10048

MAXIMUM RATINGS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	MJ10042	MJ10045	MJ10048	Unit
Collector-Emitter Voltage ($I_B = 0$)	V_{CEO}	850	450	250	Vdc
Collector-Emitter Voltage ($R_{BE} = 10\ \Omega$)	V_{CER}	900	500	300	Vdc
Collector-Base Voltage	V_{CB}	900	500	300	Vdc
Emitter-Base Voltage	V_{EB}	8.0			Vdc
Collector Current — Operating ($T_C = 115^\circ\text{C}$) ($T_C = 85^\circ\text{C}$) ($T_C = 85^\circ\text{C}$)	$I_{C(op)}$	25 — —	— 50 —	— — 100*	A
Collector Current — Continuous — Peak Repetitive — Peak Nonrepetitive	I_C	37.5 75 125	75 150 250	100 300 500	A
Base Current — Continuous — Peak Nonrepetitive	I_B	25 50			A
Total Device Dissipation Derate above $T_C = 25^\circ\text{C}$ For 1-minute overload	P_D	250 2.0 333			Watts W/ $^\circ\text{C}$ Watts
Operating Junction and Storage Temperature Range For 1-minute overload	T_J, T_{stg}	-55 to +150 -55 to 200			$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 125\ \text{mAdc}$)	MJ10042 MJ10045 MJ10048	$V_{CEO(sus)}$	850 450 250	— — —	Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CB}, V_{BE(off)} = 1.5\ \text{Vdc}$) ($V_{CE} = \text{Rated } V_{CER}, V_{BE(off)} = 1.5\ \text{Vdc}, T_C = 150^\circ\text{C}$)		I_{CEV}	— —	2.0 10	mA
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CER}, R_{BE} = 10\ \Omega, T_C = 100^\circ\text{C}$)		I_{CER}	—	10	mA
Emitter Cutoff Current ($V_{EB} = 4.0\ \text{Vdc}, I_C = 0$)		I_{EBO}	—	350	mA

SAFE OPERATING AREA

Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figures 32, 34 & 36
Clamped Inductive SOA with Base Reverse-Biased	RESOA	See Figures 33, 35 & 37
Overload Safe Operating Area	OLSOA	See Figures 38, 39, 40, 41, 42 & 43

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\ \text{Vdc}, I_E = 0, f_{test} = 1.0\ \text{kHz}$)	C_{ob}	—	2000	pF
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(1) Pulse Test. Pulse width of 300 μs , duty cycle $\leq 2.0\%$.

* This rating is with a 50% duty cycle, and is limited by power dissipation. Higher operating currents are allowable at lower duty cycles.

MJ10042, MJ10045, MJ10048

ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
MJ10042				
DC Current Gain ($I_C = 25 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 25 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$)	h_{FE}	35 40	— —	
Collector-Emitter Saturation Voltage ($I_C = 25 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$) ($I_C = 37.5 \text{ Adc}$, $I_B = 7.5 \text{ Adc}$) ($I_C = 25 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(\text{sat})}$	— — —	2.0 5.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 25 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$) ($I_C = 25 \text{ Adc}$, $I_B = 2.0 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(\text{sat})}$	— —	3.0 3.0	Vdc
MJ10045				
DC Current Gain ($I_C = 50 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 50 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$)	h_{FE}	50 60	— —	
Collector-Emitter Saturation Voltage ($I_C = 50 \text{ Adc}$, $I_B = 1.67 \text{ Adc}$) ($I_C = 75 \text{ Adc}$, $I_B = 6.0 \text{ Adc}$) ($I_C = 50 \text{ Adc}$, $I_B = 1.67 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(\text{sat})}$	— — —	2.0 3.3 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 50 \text{ Adc}$, $I_B = 1.67 \text{ Adc}$) ($I_C = 50 \text{ Adc}$, $I_B = 1.67 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(\text{sat})}$	— —	3.0 3.0	Vdc
MJ10048				
DC Current Gain ($I_C = 100 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 100 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$)	h_{FE}	75 90	— —	
Collector-Emitter Saturation Voltage ($I_C = 100 \text{ Adc}$, $I_B = 2.75 \text{ Adc}$) ($I_C = 100 \text{ Adc}$, $I_B = 2.75 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(\text{sat})}$	— —	2.0 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 100 \text{ Adc}$, $I_B = 2.75 \text{ Adc}$) ($I_C = 100 \text{ Adc}$, $I_B = 2.75 \text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(\text{sat})}$	— —	3.0 3.0	Vdc

(1) Pulse Test: Pulse width of 300 μs , duty cycle $\leq 2.0\%$.

MJ10042, MJ10045, MJ10048

ELECTRICAL CHARACTERISTICS (Continued) ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
SWITCHING CHARACTERISTICS						
MJ10042						
Resistive Load						
Delay Time	$V_{CC} = 300\text{ Vdc}$, $I_C = 25\text{ A}$, $I_{B1} = 2.0\text{ A}$, $R_{BE} = 10\ \Omega$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$	t_d	—	0.03	0.25	μs
Rise Time		t_r	—	1.2	5.0	
Storage Time		t_s	—	35	100	
Fall Time		t_f	—	8.5	35	
Inductive Load, Clamped						
Storage Time	$I_{CM} = 25\text{ A}$, $V_{CEM} = 350\text{ V}$, $R_{BE} = 10\ \Omega$, $I_{B1} = 2.0\text{ A}$	$T_J = 100^\circ\text{C}$	t_{sv}	—	50	μs
Crossover Time			t_c	—	20	
Storage Time	$T_J = 25^\circ\text{C}$	t_{sv}	—	35	100	μs
Crossover Time		t_c	—	10	35	
MJ10045						
Resistive Load						
Delay Time	$V_{CC} = 250\text{ Vdc}$, $I_C = 50\text{ A}$, $I_{B1} = 1.67\text{ A}$, $R_{BE} = 10\ \Omega$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$	t_d	—	0.03	0.25	μs
Rise Time		t_r	—	0.9	3.0	
Storage Time		t_s	—	10	25	
Fall Time		t_f	—	3.0	10	
Inductive Load, Clamped						
Storage Time	$I_{CM} = 50\text{ A}$, $V_{CEM} = 250\text{ V}$, $R_{BE} = 10\ \Omega$, $I_{B1} = 1.67\text{ A}$	$T_J = 100^\circ\text{C}$	t_{sv}	—	15	μs
Crossover Time			t_c	—	4.0	
Storage Time	$T_J = 25^\circ\text{C}$	t_{sv}	—	10	25	μs
Crossover Time		t_c	—	2.7	10	
MJ10048						
Resistive Load						
Delay Time	$V_{CC} = 150\text{ Vdc}$, $I_C = 100\text{ A}$, $I_{B1} = 2.75\text{ A}$, $R_{BE} = 10\ \Omega$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$	t_d	—	0.035	0.25	μs
Rise Time		t_r	—	1.2	4.0	
Storage Time		t_s	—	6.3	20	
Fall Time		t_f	—	2.5	8.0	
Inductive Load, Clamped						
Storage Time	$I_{CM} = 100\text{ A}$, $V_{CEM} = 150\text{ V}$, $R_{BE} = 10\ \Omega$, $I_{B1} = 2.75\text{ A}$	$T_J = 100^\circ\text{C}$	t_{sv}	—	9.0	μs
Crossover Time			t_c	—	3.3	
Storage Time	$T_J = 25^\circ\text{C}$	t_{sv}	—	6.5	20	μs
Crossover Time		t_c	—	2.3	8.0	
C-E DIODE CHARACTERISTICS						
Power Dissipation ($I_B = 0$)		P_D	—	—	125	W
Single Cycle Surge Current (60 Hz)		I_{FSM}	—	—	250	Apk
Forward Voltage (1)		V_F	—	—	—	Vdc
($I_F = 25\text{ Adc}$)	MJ10042		—	—	1.5	
($I_F = 50\text{ Adc}$)	MJ10045		—	—	1.5	
($I_F = 100\text{ Adc}$)	MJ10048		—	—	2.0	
Reverse Recovery Time ($d_i/d_t = 25\text{ A}/\mu\text{s}$)		t_{rr}	—	—	—	μs
($I_F = 25\text{ Adc}$)	MJ10042		—	4.0	12	
($I_F = 50\text{ Adc}$)	MJ10045		—	3.3	10	
($I_F = 100\text{ Adc}$)	MJ10048		—	2.5	8.0	
Forward Turn-On Time (Compliance Voltage = 250 V)		t_{on}	—	—	—	μs
($I_F = 25\text{ Adc}$)	MJ10042		—	0.3	1.2	
($I_F = 50\text{ Adc}$)	MJ10045		—	0.3	1.0	
($I_F = 100\text{ Adc}$)	MJ10048		—	1.0	3.5	

(1) Pulse Test: Pulse width of 300 μs , duty cycle $\leq 2.0\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

MJ10042

FIGURE 1 — DC CURRENT GAIN

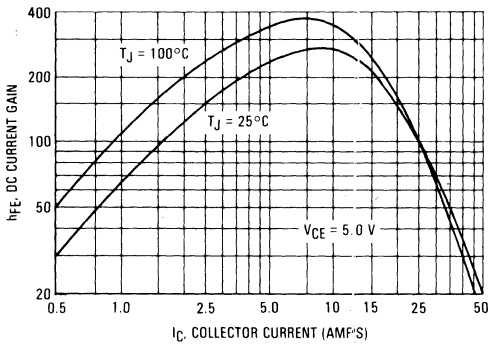
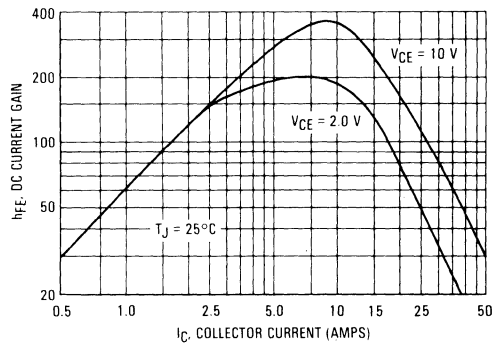


FIGURE 2 — DC CURRENT GAIN



MJ10045

FIGURE 3 — DC CURRENT GAIN

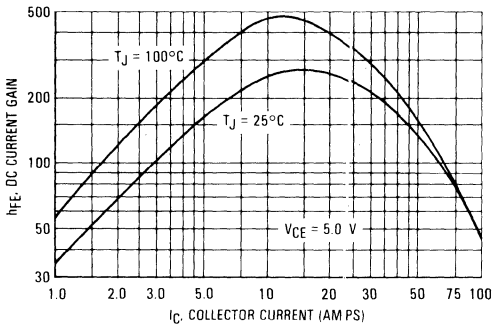
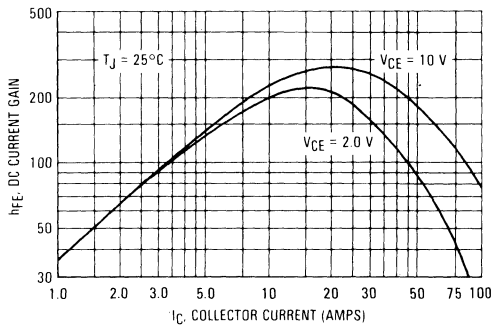


FIGURE 4 — DC CURRENT GAIN



MJ10048

FIGURE 5 — DC CURRENT GAIN

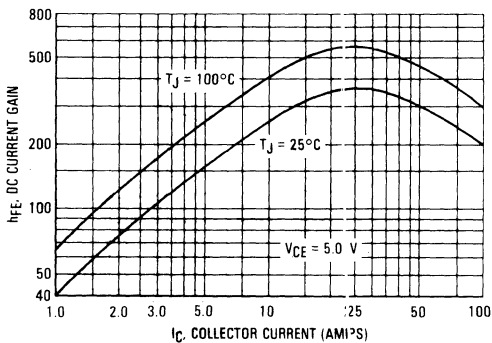
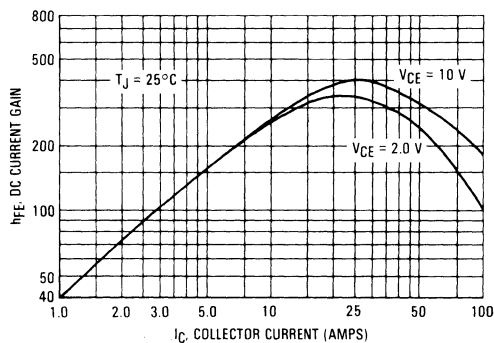


FIGURE 6 — DC CURRENT GAIN



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10042

FIGURE 7 — DC CURRENT GAIN

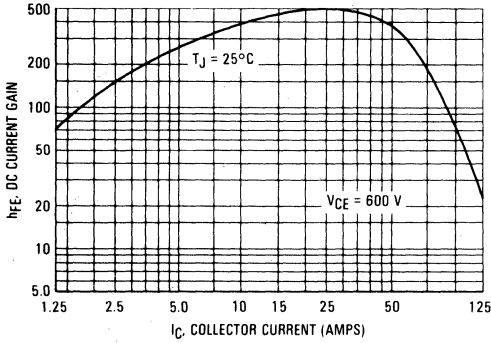
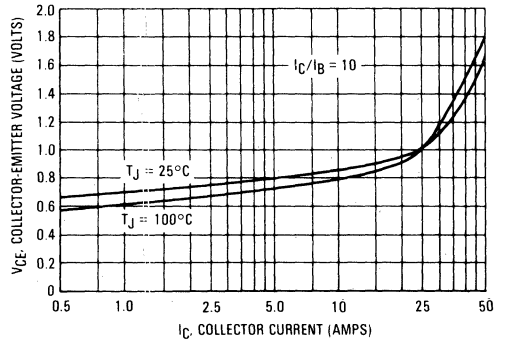


FIGURE 8 — COLLECTOR SATURATION VOLTAGE



MJ10045

FIGURE 9 — DC CURRENT GAIN

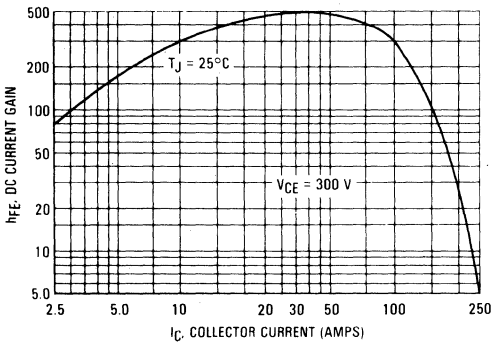
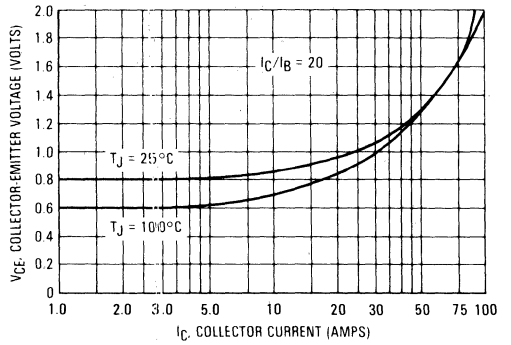


FIGURE 10 — COLLECTOR SATURATION REGION



MJ10048

FIGURE 11 — DC CURRENT GAIN

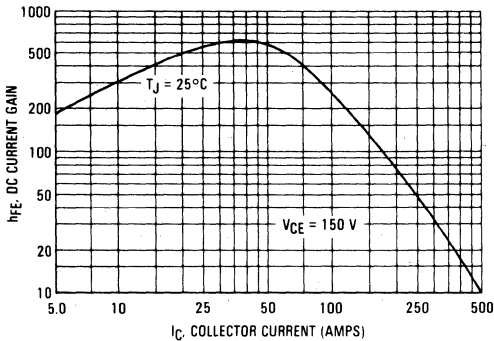
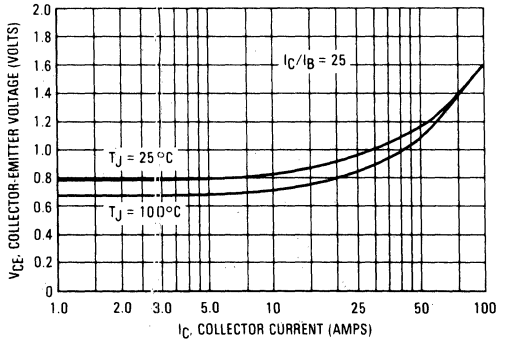


FIGURE 12 — COLLECTOR SATURATION REGION



3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10042

FIGURE 13 — BASE-EMITTER SATURATION VOLTAGE

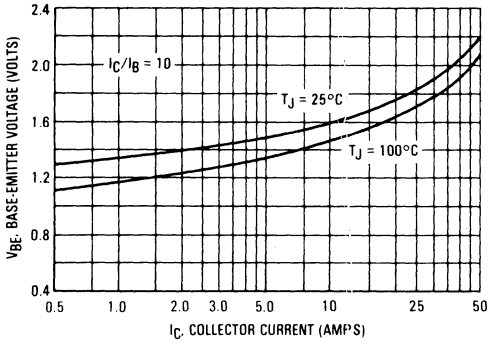
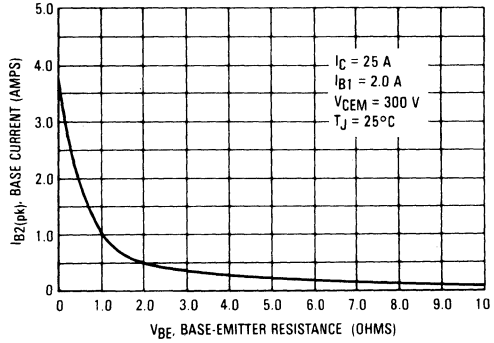


FIGURE 14 — TYPICAL PEAK REVERSE BASE CURRENT



MJ10045

FIGURE 15 — BASE-EMITTER SATURATION VOLTAGE

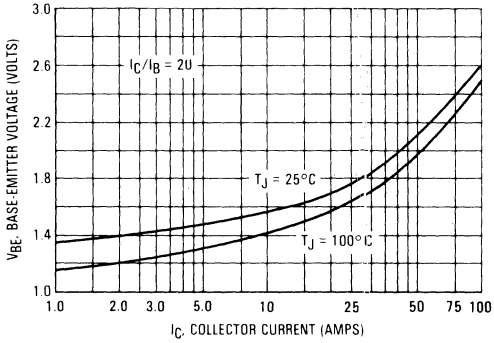
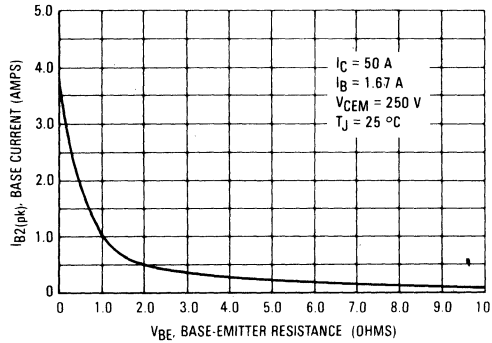


FIGURE 16 — TYPICAL PEAK REVERSE BASE CURRENT



MJ10048

FIGURE 17 — BASE-EMITTER SATURATION VOLTAGE

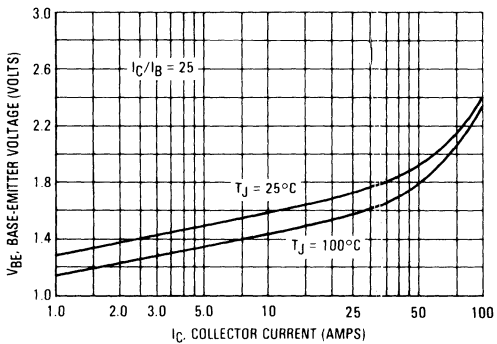
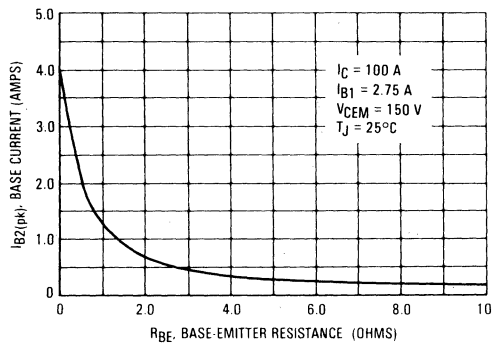


FIGURE 18 — TYPICAL PEAK REVERSE BASE CURRENT



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

MJ10042

FIGURE 19 — TYPICAL INDUCTIVE SWITCHING TIMES

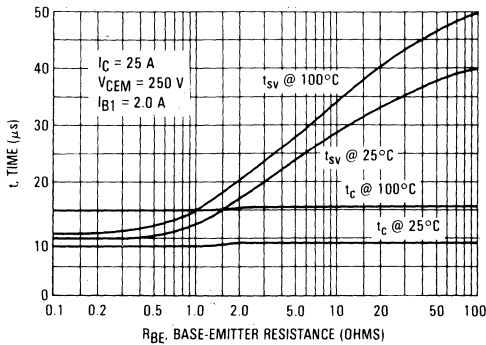
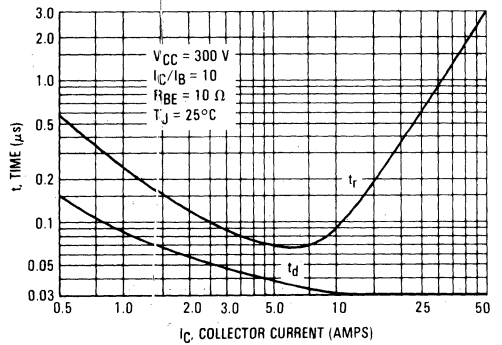


FIGURE 20 — TYPICAL TURN-ON SWITCHING TIMES



MJ10045

FIGURE 21 — TYPICAL INDUCTIVE SWITCHING TIMES

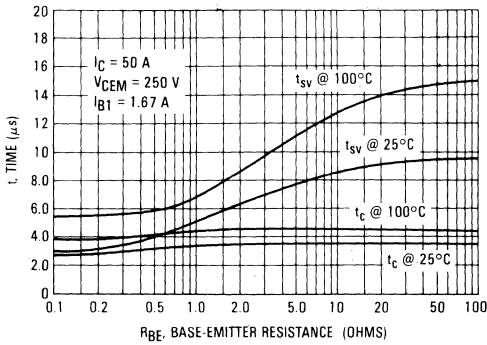
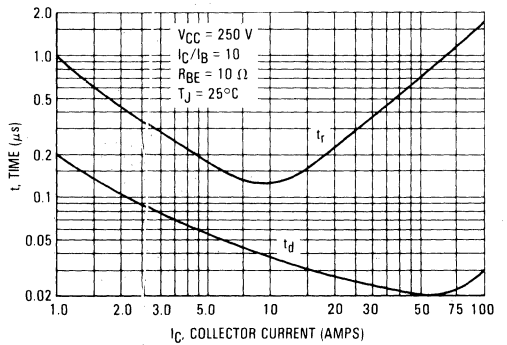


FIGURE 22 — TYPICAL TURN-ON SWITCHING TIMES



MJ10048

FIGURE 23 — TYPICAL INDUCTIVE SWITCHING TIMES

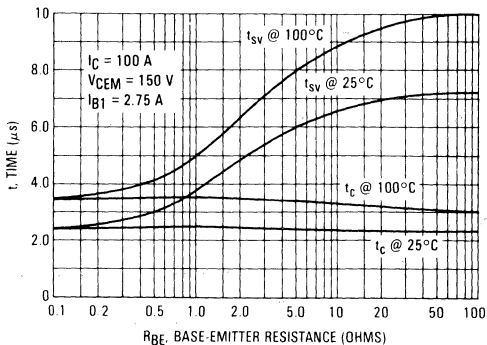
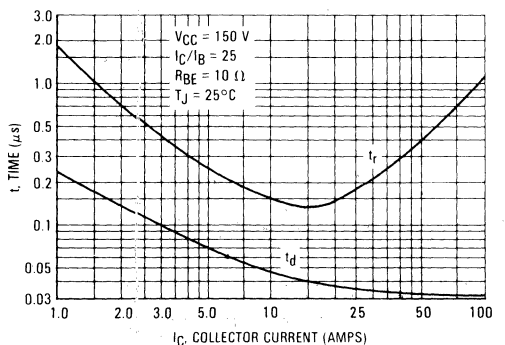


FIGURE 24 — TYPICAL TURN-ON SWITCHING TIMES



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 25 — TYPICAL TURN-OFF SWITCHING TIMES
MJ10042

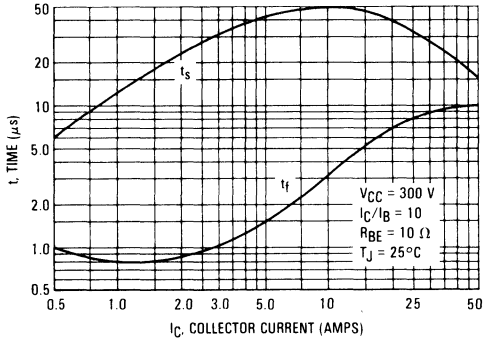


FIGURE 26 — EMITTER-COLLECTOR DIODE
FORWARD VOLTAGE

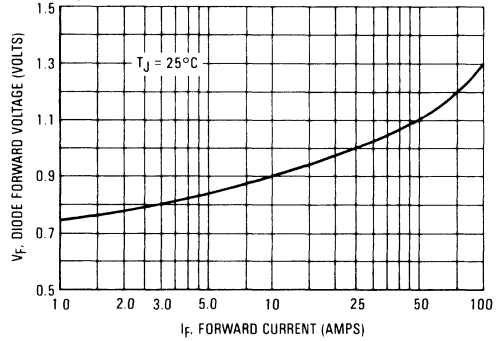


FIGURE 27 — TYPICAL TURN-OFF SWITCHING TIMES
MJ10045

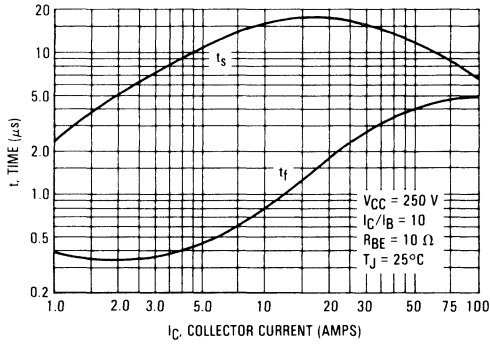


FIGURE 28 — POWER DERATING

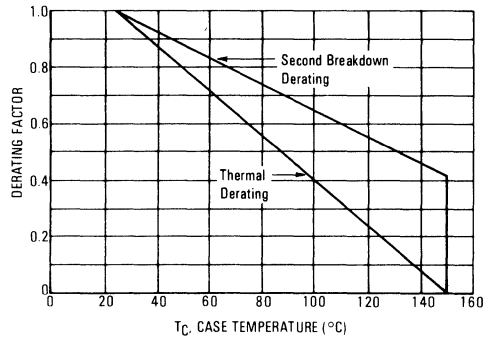


FIGURE 29 — TYPICAL TURN-OFF SWITCHING TIMES
MJ10048

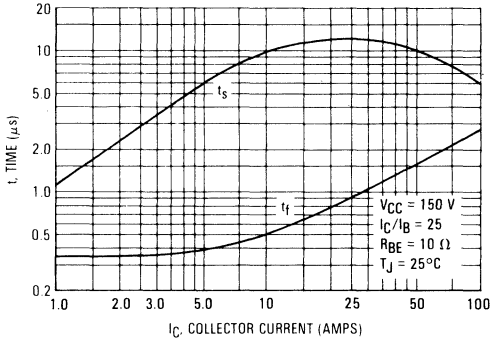


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CE(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS		<p>DRIVER SCHEMATIC</p> <p>For inductive loads pulse width is adjusted to obtain specified I_C</p>	<p>TURN ON TIME</p> <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME</p> <p>Use inductive switching circuit as the input to the resistive test circuit.</p>
CIRCUIT VALUES	$L_{coil} = 10 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.1 \Omega$ $V_{clamp} = V_{CE(sus)}$	$L_{coil} = 5.0 \mu\text{H}$ $V_{CC} = 20 \text{ V}$	$V_{CC} = 150 \text{ to } 300 \text{ V}$ Pulse Width = $50 \mu\text{s}$ Adjust R_L for I_{CM}
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ <p>Test Equipment Scope – Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

*Adjust $-V$ such that $V_{BE(off)} = 5.0 \text{ V}$ except as required for RBSOA.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and motor controls, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
- t_{fi} = Current Fall Time, 90–10% I_{CM}
- t_{ti} = Current Tail, 10–2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform

is shown in Figure 30 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 30 – INDUCTIVE SWITCHING MEASUREMENTS

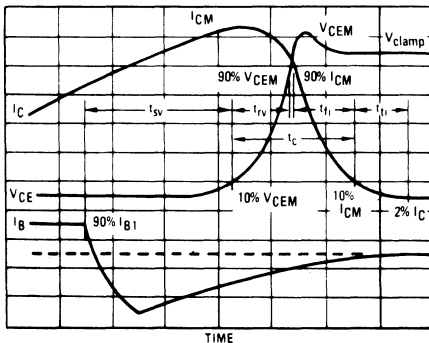
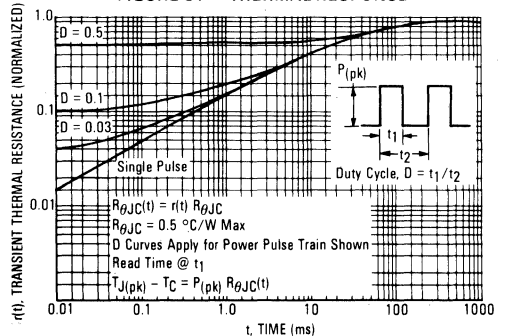


FIGURE 31 – THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

MJ10042

FIGURE 32 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

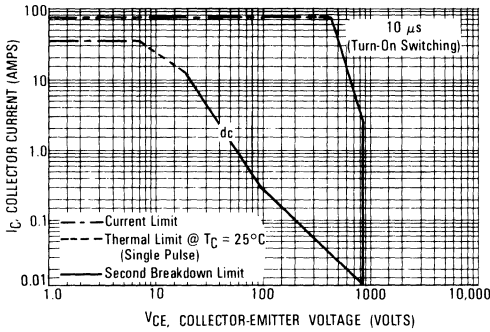
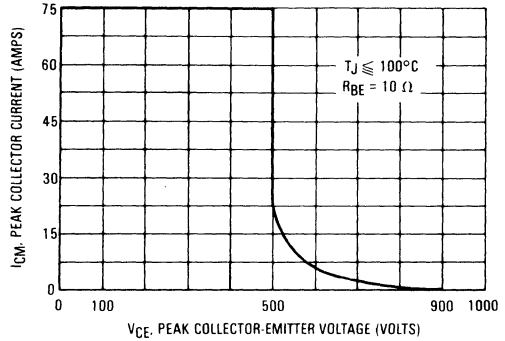


FIGURE 33 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



MJ10045

FIGURE 34 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

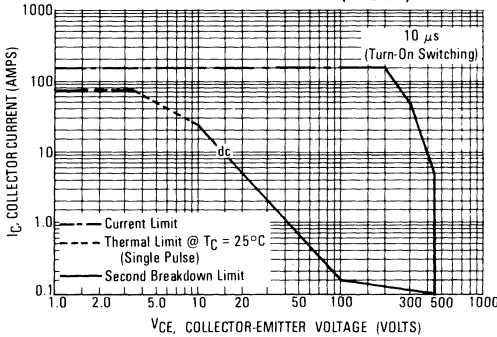
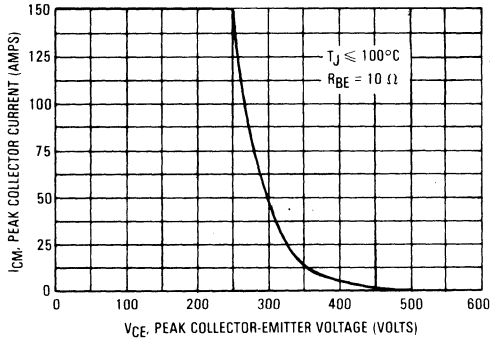


FIGURE 35 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



MJ10048

FIGURE 36 — MAXIMUM RATED FORWARD-BIAS SAFE OPERATING AREA (FBSOA)

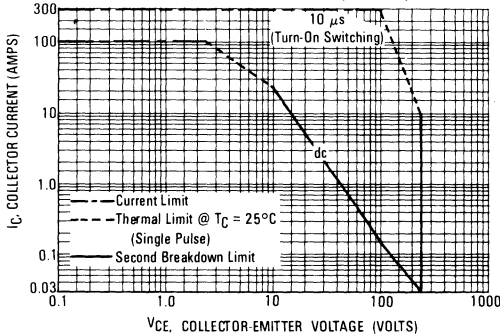
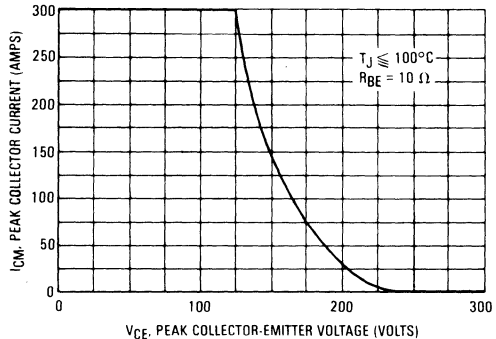


FIGURE 37 — MAXIMUM RATED REVERSE-BIAS SAFE OPERATING AREA (RBSOA)



3

OVERLOAD CHARACTERISTICS

MJ10042

FIGURE 38 — OVERLOAD SAFE OPERATING AREA
TYPE I (OLSOA)

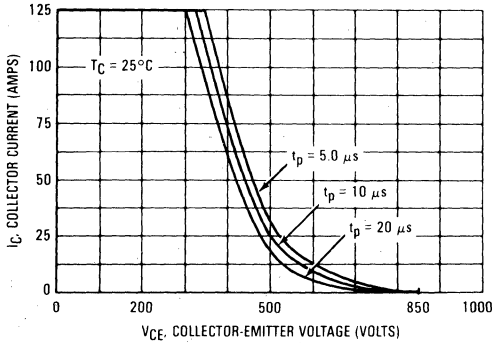
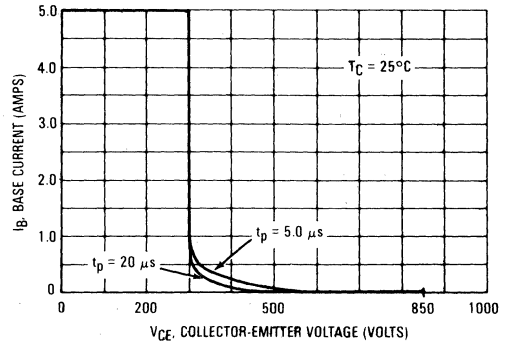


FIGURE 39 — OVERLOAD SAFE OPERATING AREA
TYPE II (OLSOA)



MJ10045

FIGURE 40 — OVERLOAD SAFE OPERATING AREA
TYPE I (OLSOA)

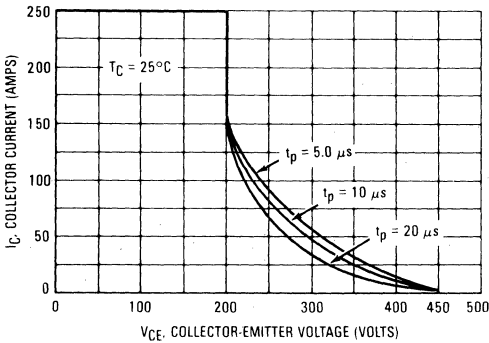
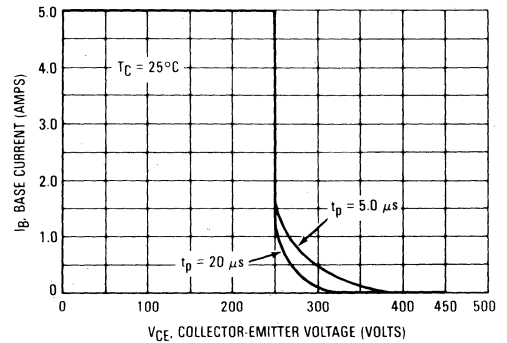


FIGURE 41 — OVERLOAD SAFE OPERATING AREA
TYPE II (OLSOA)



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MJ10048

FIGURE 42 — OVERLOAD SAFE OPERATING AREA
TYPE I (OLSOA)

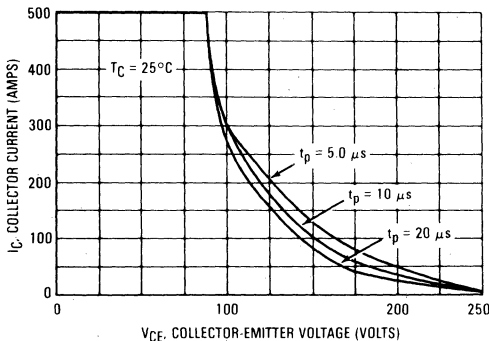
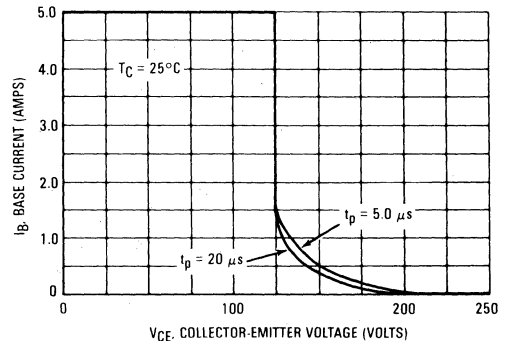


FIGURE 43 — OVERLOAD SAFE OPERATING AREA
TYPE II (OLSOA)



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 32, 34 and 36 are based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on these figures may be found at any case temperature by using the appropriate curve on Figure 28.

$T_{J(pk)}$ may be calculated from the data in Figure 31. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse-Bias Safe Operating Area and represents the voltage-current condition allowable during reverse-biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figures 33, 35 and 37 give the RBSOA characteristics.

OVERLOAD SAFE OPERATING AREA

The forward-bias safe operating area (FBSOA) specification given in these figures adequately describes transistor capability for normal repetitive operation. When short circuit or fault conditions occur, these transistor specifications are not always adequate. A specification called overload safe operating area (OLSOA) has been developed to describe the transistor's ability to survive under fault conditions. OLSOA is specified under two types of conditions.

TYPE I OLSOA

Type I OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known. Figures 38, 40 and 42 depict the Type I OLSOA rating for these devices. Maximum allowable collector-

emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, these figures define the maximum time which can be allowed for fault detection and shutdown of base drive.

Type I OLSOA is measured in a common-base circuit (Figure 44) which allows precise definition of collector-emitter voltage and collector current. This is the same circuit that is used to measure forward-bias safe operating area.

TYPE II OLSOA

Type II OLSOA applies when maximum collector current is not limited by circuit design, but is limited only by the gain of the transistor. Therefore, collector current does not appear on the Type II OLSOA curve. This curve defines a safe region of operation from the information that is usually available to the designer.

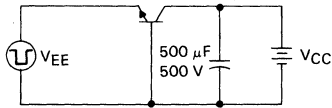
This information is normally base drive, bus voltage and time. In terms of the OLSOA curve, bus voltage is assumed to be worst-case collector-emitter voltage, and time is defined to be the same pulse width that was described for Type I OLSOA. Using these variables, maximum collector-emitter voltage versus base drive is plotted for several values of pulse width. A safe region of operation is thus determined by the circuit parameters. Type II OLSOA, as shown in Figures 39, 41 and 43 are measured in the circuit shown in Figure 45, and measurement is made as follows: Base current is applied while the collector is open, allowing a highly overdriven saturated condition. Next, a stiff voltage source is applied to the collector. The rising voltage at the collector of the transistor triggers a delay function. At the end of this delay, base drive is removed. The delay time is the variable on the Type II OLSOA curve. The storage time of the transistor is thereby factored into the rating.

There are several additional aspects to be considered regarding OLSOA. The first consideration is that OLSOA is strictly a NON-REPETITIVE rating. It is intended to describe the survivability of the transistor during an accidental overload and is not intended to describe a stress level which can be sustained indefinitely. The number of nonrepetitive faults for which OLSOA is defined for these devices is 100 occurrences. Another factor is the form of turn-off bias. For these devices, turn-off bias has relatively little effect on its OLSOA capability. This observation is valid from $I_{B2} = 0$ (soft) to $V_{BE(off)} = 5\text{ V}$ (stiff).

OLSOA is subject to the same derating with temperature as normal FBSOA. The second breakdown derating curve is applied to the allowable current at any given voltage, using the same procedure that is followed with pulsed FBSOA.

OVERLOAD SAFE OPERATING TEST CIRCUITS

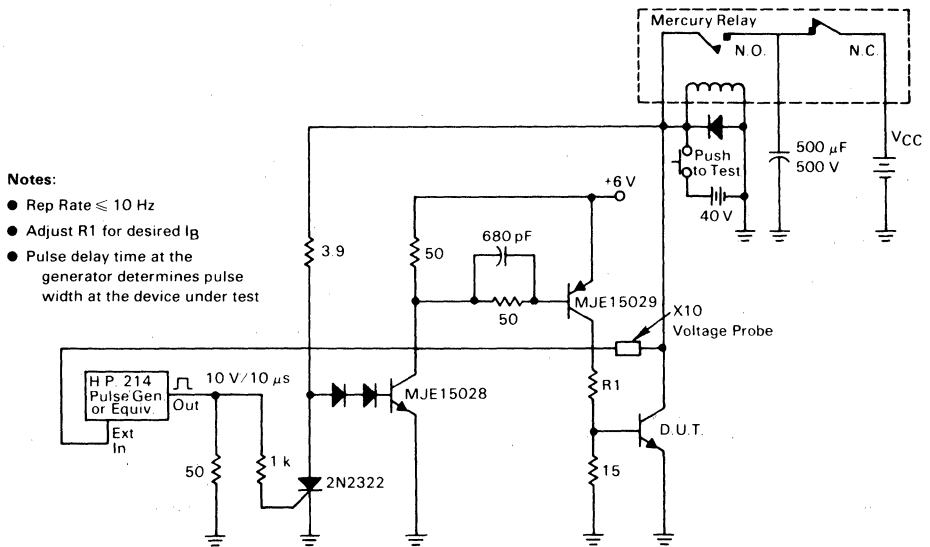
FIGURE 44 — OVERLOAD SOA TEST CIRCUIT TYPE I (OLSOA)



Notes:

- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

FIGURE 45 — OVERLOAD SOA TEST CIRCUIT TYPE II (OLSOA)



Notes:

- Rep Rate ≤ 10 Hz
- Adjust R1 for desired I_B
- Pulse delay time at the generator determines pulse width at the device under test

3

PNP	NPN
MJ11011	MJ11012
MJ11013	MJ11014
MJ11015	MJ11016

HIGH-CURRENT COMPLEMENTARY SILICON TRANSISTORS

... for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain - $h_{FE} = 1000$ (Min) @ $I_C = 20$ Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor
- Junction Temperature to +200°C

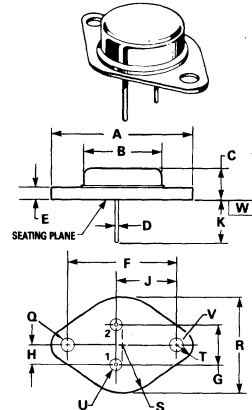
30 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON
60-120 VOLTS
200 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJ11011 MJ11012	MJ11013 MJ11014	MJ11015 MJ11016	Unit
Collector-Emitter Voltage	V_{CEO}	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector Current	I_C	30			A dc
Base Current	I_B	1			A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C @ $T_C = 100^\circ\text{C}$	P_D	200 115			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.87	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes for ≤ 10 Seconds.	T_L	275	$^\circ\text{C}$



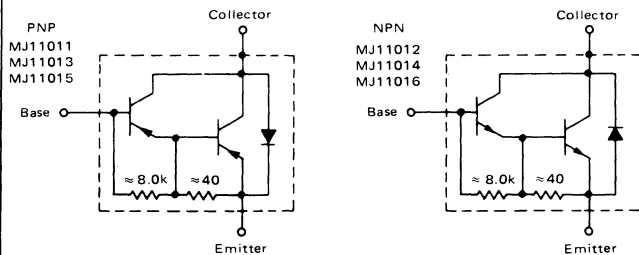
- NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
 2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\pm \phi 0.25$ (0.010) M | W | V Q
 3. POSITIONAL TOLERANCE FOR LEADS:
 $\pm \phi 0.30$ (0.012) M | W | V Q Q

STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.666 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA

FIGURE 1 — DARLINGTON CIRCUIT SCHEMATIC



PNP MJ11011, MJ11013, MJ11015 NPN MJ11012, MJ11014, MJ11016

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage(1) (I _C = 100 mA, I _B = 0)	V _{(BR)CEO}	60 90 120	— — —	V _{dc}
Collector Emitter Leakage Current (V _{CE} = 60 Vdc, R _{BE} = 1 k ohm) (V _{CE} = 90 Vdc, R _{BE} = 1 k ohm) (V _{CE} = 120 Vdc, R _{BE} = 1 k ohm) (V _{CE} = 60 Vdc, R _{BE} = 1 k ohm, T _C = 150°C) (V _{CE} = 90 Vdc, R _{BE} = 1 k ohm, T _C = 150°C) (V _{CE} = 120 Vdc, R _{BE} = 1 k ohm, T _C = 150°C)	I _{CER}	— — — — — —	1 1 1 5 5 5	mA _{dc}
Emitter Cutoff Current (V _{BE} = 5 Vdc, I _C = 0)	I _{EBO}	—	5	mA _{dc}
Collector-Emitter Leakage Current (V _{CE} = 50 Vdc, I _B = 0)	I _{CEO}	—	1	mA _{dc}
ON CHARACTERISTICS(1)				
DC Current Gain (I _C = 20 A, V _{CE} = 5 Vdc) (I _C = 30 A, V _{CE} = 5 Vdc)	h _{FE}	1000 200	— —	—
Collector-Emitter Saturation Voltage (I _C = 20 A, I _B = 200 mA) (I _C = 30 A, I _B = 300 mA)	V _{CE(sat)}	—	3 4	V _{dc}
Base-Emitter Saturation Voltage (I _C = 20 A, I _B = 200 mA) (I _C = 30 A, I _B = 300 mA)	V _{BE(sat)}	—	3.5 5	V _{dc}
DYNAMIC CHARACTERISTICS				
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I _C = 10 A, V _{CE} = 3 Vdc, f = 1 MHz)	h _{fg}	4	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — DC CURRENT GAIN (1)

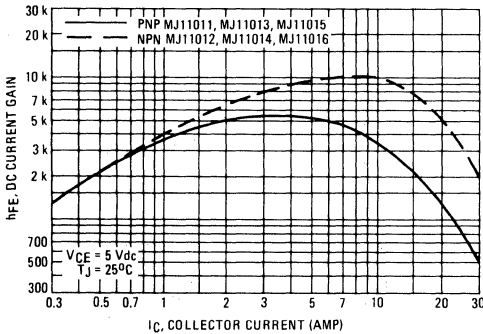
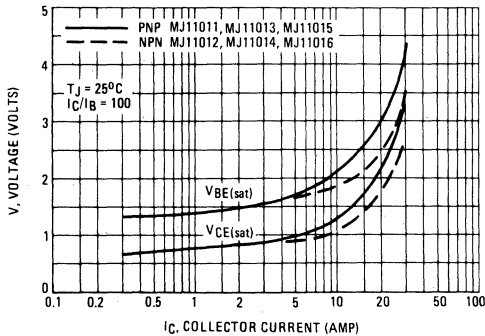


FIGURE 4 — "ON" VOLTAGES (1)



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor

FIGURE 3 — SMALL-SIGNAL CURRENT GAIN

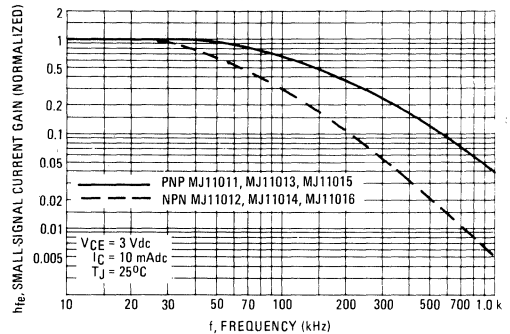
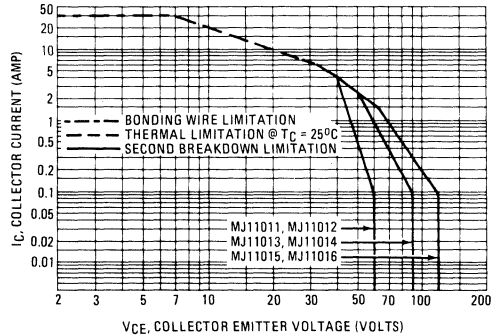


FIGURE 5 — ACTIVE REGION DC SAFE OPERATING AREA



must not be subjected to greater dissipation than the curves indicate. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

NPN **NPN**
MJ11017 **MJ11018**
MJ11019 **MJ11020**
MJ11021 **MJ11022**

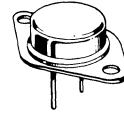
**COMPLEMENTARY DARLINGTON
 SILICON POWER TRANSISTORS**

... designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High dc Current Gain @ 10 Adc — $h_{FE} = 400$ Min (All Types)
- Collector-Emitter Sustaining Voltage
 $V_{CE(sus)} = 150$ Vdc (Min) — MJ11018, 17
 $= 200$ Vdc (Min) — MJ11020, 19
 $= 250$ Vdc (Min) — MJ11022, 21
- Low Collector-Emitter Saturation
 $V_{CE(sat)} = 1.0$ V (Typ) @ $I_C = 5.0$ A
 $= 1.8$ V (Typ) @ $I_C = 10$ A
- Monolithic Construction
- 100% SOA Tested @ $V_{CE} = 44$ V, $I_C = 4.0$ A, $t = 250$ ms.

15 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON

150, 200, 250 VOLTS
175 WATTS



MAXIMUM RATINGS

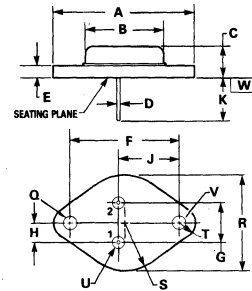
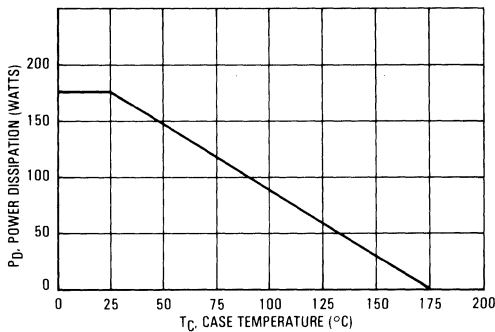
Rating	Symbol	MJ11018 MJ11017	MJ11020 MJ11019	MJ11022 MJ11021	Unit
Collector-Emitter Voltage	V_{CE0}	150	200	250	Vdc
Collector-Base Voltage	V_{CB}	150	200	250	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	15 30			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above 25°C	P_D	175 1.16			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J T_{stg}	-65 to +175 -65 to +200			$^\circ\text{C}$ $^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.86	$^\circ\text{C}/\text{W}$

(1) Pulse Test: Pulse Width 5.0 ms, Duty Cycle $\leq 10\%$

FIGURE 1 — POWER DERATING



NOTES:

1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\pm \phi 0.25 (0.010) \text{ (M) } | \text{ W } | \text{ (M) } | \text{ V } | \text{ (M)}$
3. POSITIONAL TOLERANCE FOR LEADS:
 $\pm \phi 0.30 (0.012) \text{ (M) } | \text{ W } | \text{ (M) } | \text{ Q } | \text{ (M)}$

STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA

PNP MJ11017, MJ11019, MJ11021
NPN MJ11018, MJ11020, MJ11022

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 0.1 \text{ Adc}$, $I_B = 0$)	$V_{CE(sus)}$	MJ11017, MJ11018 200	—	Vdc
MJ11019, MJ11020 250		—		
MJ11021, MJ11022		—		
Collector Cutoff Current ($V_{CE} = 75$, $I_B = 0$)	I_{CEO}	MJ11017, MJ11018	—	mAdc
($V_{CE} = 100$, $I_B = 0$)		MJ11019, MJ11020	1.0	
($V_{CE} = 125$, $I_B = 0$)		MJ11021, MJ11022	1.0	
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_J = 150^\circ\text{C}$)	I_{CEV}	—	0.5	mAdc
—		—	5.0	
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	2.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 10 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 15 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$)	h_{FE}	400	15,000	—
—		100	—	
Collector-Emitter Saturation Voltage ($I_C = 10 \text{ Adc}$, $I_B = 100 \text{ mA}$) ($I_C = 15 \text{ Adc}$, $I_B = 150 \text{ mA}$)	$V_{CE(sat)}$	—	2.0	Vdc
—		—	3.4	
Base-Emitter On Voltage $I_C = 10 \text{ A}$, $V_{CE} = 5.0 \text{ Vdc}$	$V_{BE(on)}$	—	2.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 15 \text{ Adc}$, $I_B = 150 \text{ mA}$)	$V_{BE(sat)}$	—	3.8	Vdc

DYNAMIC CHARACTERISTICS

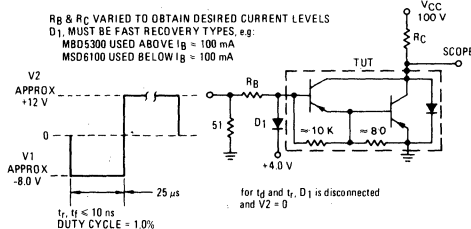
Magnitude of Common Emitter Small Signal Short Circuit Forward Current Transfer Ratio ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	$[h_{fe}]$	3.0	—	—
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$) MJ11018, MJ11020, MJ11022 MJ11017, MJ11019, MJ11021	C_{ob}	—	400	pF
—		—	600	
Small-Signal Current Gain ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	100	—	—

SWITCHING CHARACTERISTICS

Characteristics	Symbol	Typical		Unit
		NPN	PNP	
Delay Time	t_d	150	75	ns
Rise Time	t_r	1.2	0.5	μs
Storage Time	t_s	4.4	2.7	μs
Fall Time	t_f	10.0	2.5	μs

(1) Pulsed Test: Pulse Width = 300 μs . Duty Cycle $\leq 2\%$.

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

PNP MJ11017, MJ11019, MJ11021
NPN MJ11018, MJ11020, MJ11022

FIGURE 3 — THERMAL RESPONSE

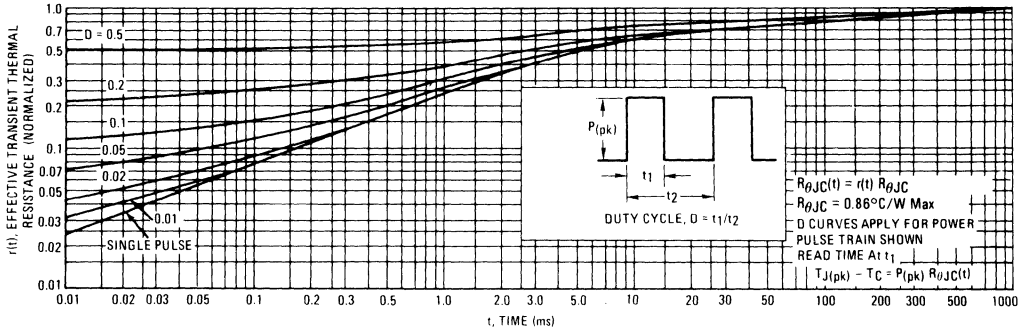
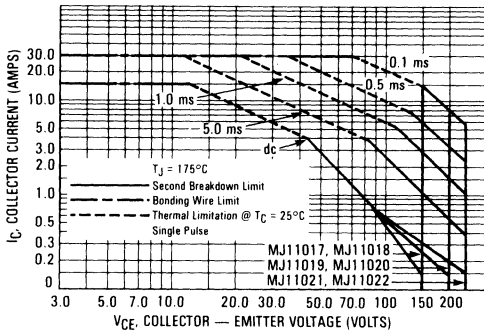


FIGURE 4 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (FBSOA)

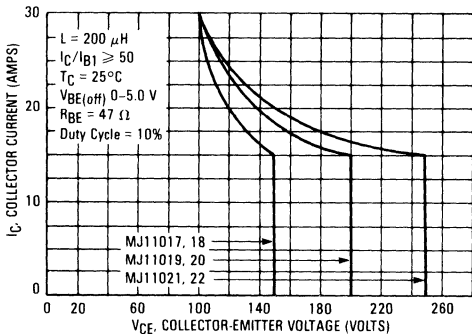


FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 175^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 175^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 5 — MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives RBSOA characteristics.

FIGURE 6 — DC CURRENT GAIN

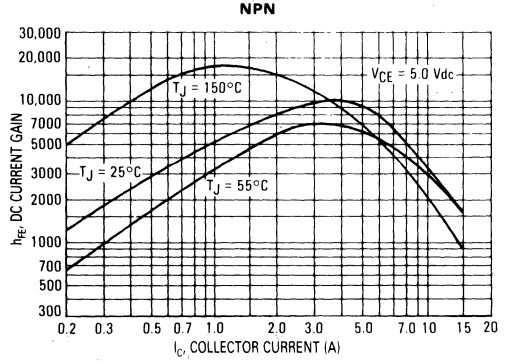
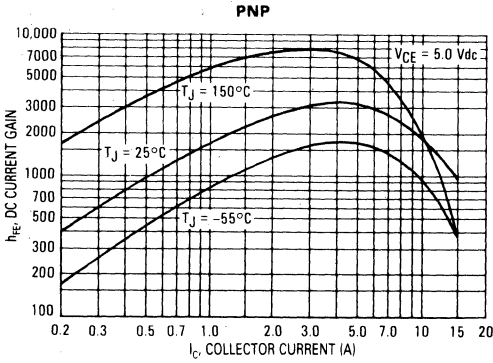


FIGURE 7 — COLLECTOR SATURATION REGION

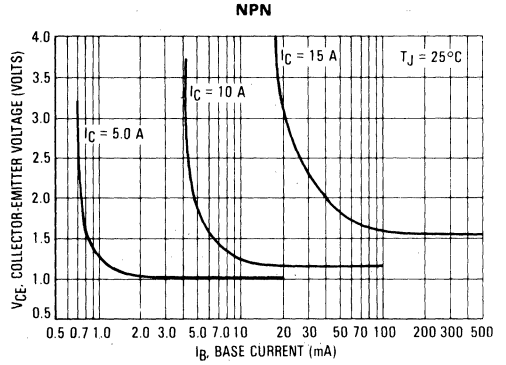
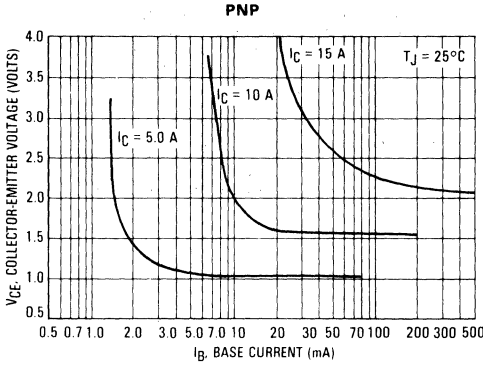
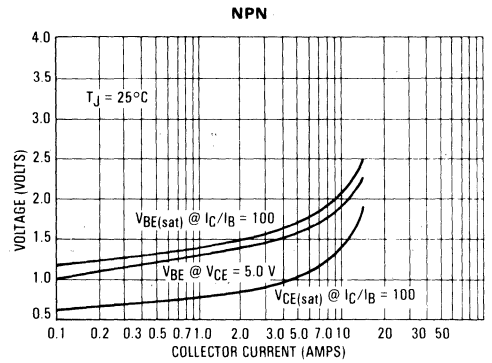
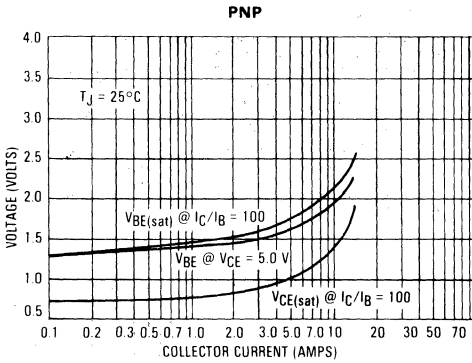


FIGURE 8 — "ON" VOLTAGES



NPN	PNP
MJ11028	MJ11029
MJ11030	MJ11031
MJ11032	MJ11033

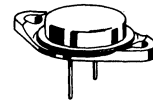
HIGH-CURRENT COMPLEMENTARY SILICON TRANSISTORS

... for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — $h_{FE} = 1000$ (Min) @ $I_C = 25$ Adc
 $h_{FE} = 400$ (Min) @ $I_C = 50$ Adc
- Curves to 100 A (Pulsed)
- Diode Protection to Rated I_C
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor
- Junction Temperature to +200°C

50 AMPERE
COMPLEMENTARY SILICON
DARLINGTON
POWER TRANSISTOR

60-120 VOLTS
300 WATTS



MAXIMUM RATINGS

Rating	Symbol	MJ11028 MJ11029	MJ11030 MJ11031	MJ11032 MJ11033	Unit
Collector-Emitter Voltage	V_{CE0}	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector Current—Continuous	I_C	50			Adc
Peak	I_{CM}	100			
Base Current—Continuous	I_B	2			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C @ $T_C = 100^\circ\text{C}$	P_D	300			Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Maximum Lead Temperature for Soldering Purposes for ≤ 10 seconds	T_L	275	$^\circ\text{C}$
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.584	$^\circ\text{C}$

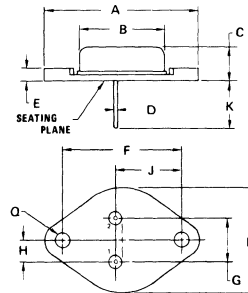
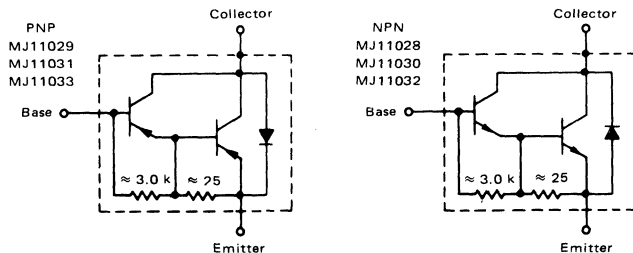


FIGURE 1 — DARLINGTON CIRCUIT SCHEMATIC



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	18.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	28.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

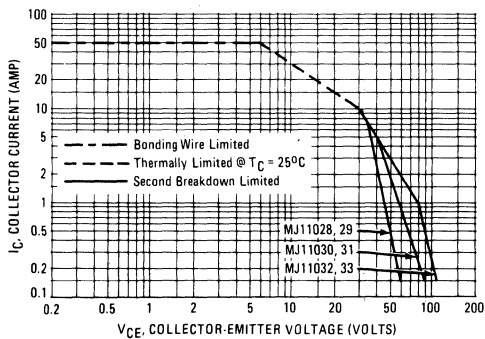
NPN MJ11028, MJ11030, MJ11032
PNP MJ11029, MJ11031, MJ11033

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 100 \text{ mAdc}$, $I_B = 0$)	MJ11028 MJ11029 MJ11030 MJ11031 MJ11032 MJ11033	$V_{(BR)CEO}$	60 90 120	Vdc
Collector-Emitter Leakage Current ($V_{CE} = 60 \text{ Vdc}$, $R_{BE} = 1 \text{ k ohm}$) ($V_{CE} = 90 \text{ Vdc}$, $R_{BE} = 1 \text{ k ohm}$) ($V_{CE} = 120 \text{ Vdc}$, $R_{BE} = 1 \text{ k ohm}$) ($V_{CE} = 60 \text{ Vdc}$, $R_{BE} = 1 \text{ k ohm}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 90 \text{ Vdc}$, $R_{BE} = 1 \text{ k ohm}$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 120 \text{ Vdc}$, $R_{BE} = 1 \text{ k ohm}$, $T_C = 150^\circ\text{C}$)	MJ11028 MJ11029 MJ11030 MJ11031 MJ11032 MJ11033 MJ11028 MJ11029 MJ11030 MJ11031 MJ11032 MJ11033 MJ11028 MJ11029 MJ11030 MJ11031 MJ11032 MJ11033	I_{CER}	— — — — — —	mAdc
Emitter Cutoff Current ($V_{BE} = 5 \text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	5 mAdc
Collector-Emitter Leakage Current ($V_{CE} = 50 \text{ Vdc}$, $I_B = 0$)		I_{CEO}	—	2 mAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 25 \text{ Adc}$, $V_{CE} = 5 \text{ Vdc}$) ($I_C = 50 \text{ Adc}$, $V_{CE} = 5 \text{ Vdc}$)		h_{FE}	1 k 400	18 k —
Collector-Emitter Saturation Voltage ($I_C = 25 \text{ Adc}$, $I_B = 250 \text{ mAdc}$) ($I_C = 50 \text{ Adc}$, $I_B = 500 \text{ mAdc}$)		$V_{CE(sat)}$	— —	2.5 3.5 Vdc
Base-Emitter Saturation Voltage ($I_C = 25 \text{ Adc}$, $I_B = 200 \text{ mAdc}$) ($I_C = 50 \text{ Adc}$, $I_B = 300 \text{ mAdc}$)		$V_{BE(sat)}$	— —	3.0 4.5 Vdc

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 3 – DC CURRENT GAIN

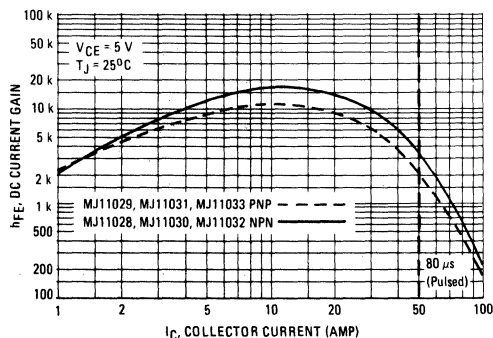
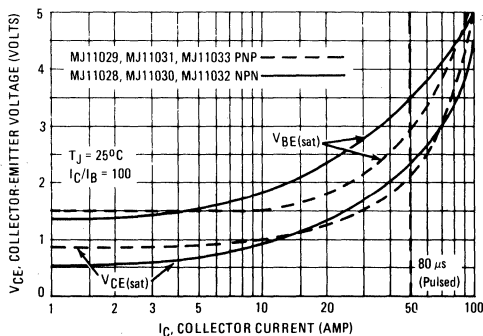


FIGURE 4 – "ON" VOLTAGE



MJ12002

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

... specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage –
 $V_{CEX} = 1500$ Volts
- Glassivated Base-Collector Junction
- Forward Bias Safe Operating Area @ $50 \mu s = 15 A, 300 V$
- Switching Times with Inductive Loads –
 $t_f = 0.65 \mu s$ (Typ) @ $I_C = 2.0 A$

2.5 AMPERE
NPN SILICON
POWER TRANSISTOR

1500 VOLTS
75 WATTS

Designer's Data for
"Worst Case" Conditions

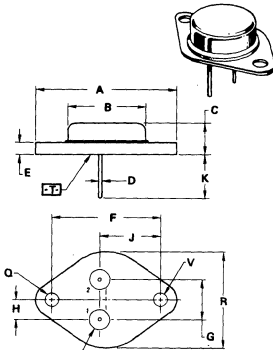
The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	2.5	Adc
Base Current – Continuous	I_B	2.0	Adc
Emitter Current – Continuous	I_E	4.5	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ @ $T_C = 100^\circ C$	P_D	75 30	Watts Watts
Derate above $25^\circ C$		0.6	$W/^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ C$



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\pm 0.13 (0.005) \text{ T } | \text{ V } \text{ (M)}$$

FOR LEADS:

$$\pm 0.13 (0.005) \text{ (M) T } | \text{ V } \text{ (M) } | \text{ Q } \text{ (M)}$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	19.87 BSC		0.783 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

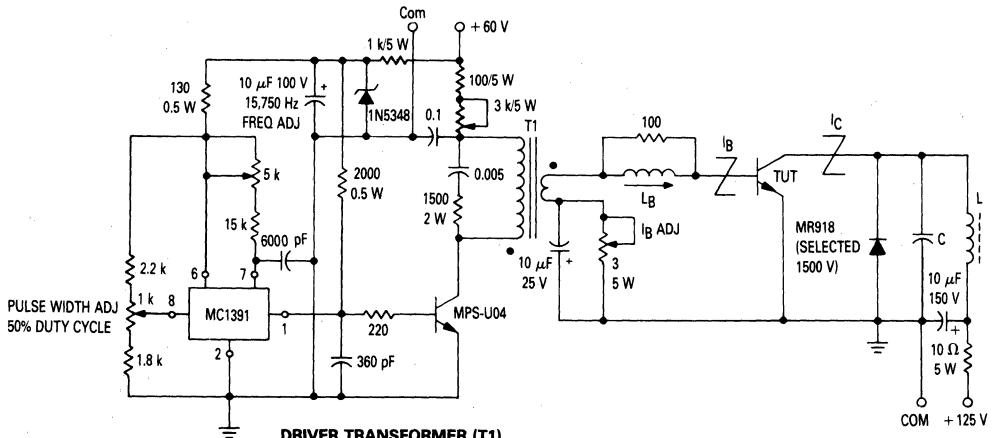
STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage ($I_C = 50 \text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	750	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 1500 \text{ Vdc}$, $V_{BE} = 0$)	I_{CES}	—	—	1.0	mA
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	0.1	mA
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage ($I_C = 2.0 \text{ A}$, $I_B = 1.8 \text{ A}$)	$V_{CE(sat)}$	—	—	5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 2.0 \text{ A}$, $I_B = 1.8 \text{ A}$)	$V_{BE(sat)}$	—	—	1.5	Vdc
Second Breakdown Collector Current with Base-Forward Biased	$I_{S/B}$	—	See Figure 14	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	—	50	—	pF
Current Gain – Bandwidth Product (1) ($I_C = 0.1 \text{ A}$, $V_{CE} = 5.0 \text{ Vdc}$, $f_{test} = 1.0 \text{ MHz}$)	f_T	—	4.0	—	MHz
SWITCHING CHARACTERISTICS					
Fall Time ($I_C = 2.0 \text{ A}$, $I_{B1} = 1.0 \text{ A}$, $L_B = 12 \mu\text{H}$, See Figure 1)	t_f	—	0.65	1.0	μs

(1) Pulse Test: Pulse Width $< 300 \mu\text{s}$, Duty Cycle = 2%.

Figure 1. Switching Times Test Circuit



DRIVER TRANSFORMER (T1)

- Ferroxcube pot core #4229P-L00-3C8
- Adjust gap for primary inductance $L_p = 70 \text{ mH}$ (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than $3 \mu\text{H}$
- Use 3 mil mylar tape between each winding layer

I_C	L	C
0.75 A	4.25 mH	.003 μF
1.5	2.18 mH	.006 μF
2.0	1.6 mH	.008 μF

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM} . Worst case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM} , I_{B1} , and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B , at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown

in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1} , and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1} h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM} . As L_B is increased, the curves become broader and flatter above the $I_{B1} h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE} , essentially moves the curves to the left or right according to the relation $I_{B1} h_{FE} = \text{constant}$. It then becomes obvious that, for a specified I_{CM} , an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1} . The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM} . These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

TEST CIRCUIT WAVEFORMS

FIGURE 2

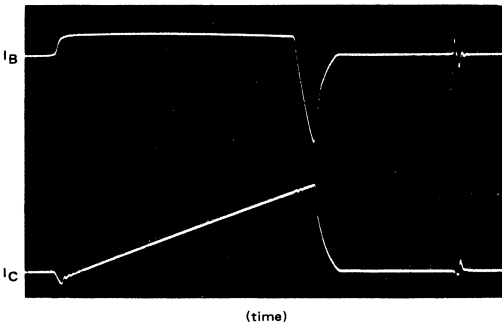
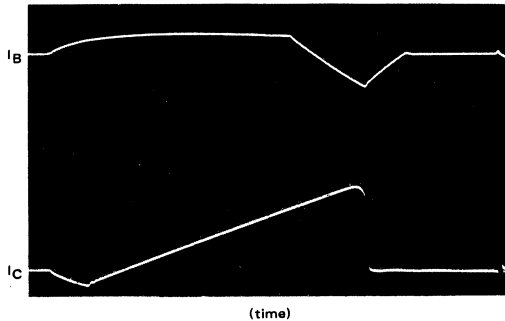


FIGURE 3



TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 – OPTIMIZING DRIVE @ $I_C = 0.75$ A

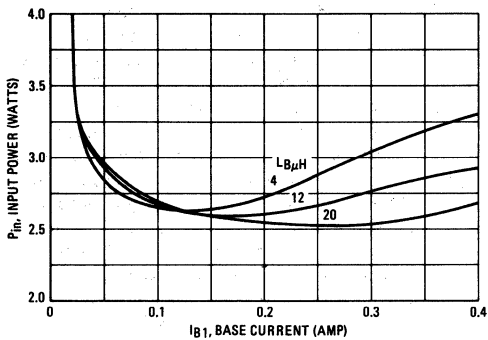


FIGURE 5 – OPTIMIZING DRIVE @ $I_C = 1.5$ A

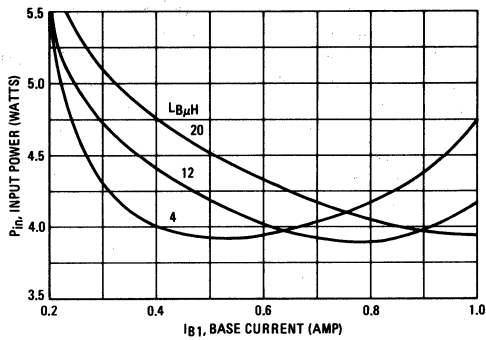


FIGURE 6 – OPTIMIZING DRIVE @ $I_C = 2.0$ A

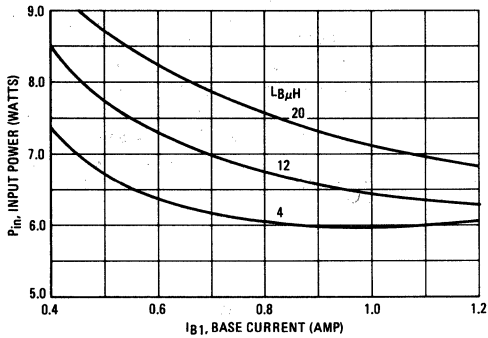


FIGURE 7 – SWITCHING BEHAVIOR versus TEMPERATURE

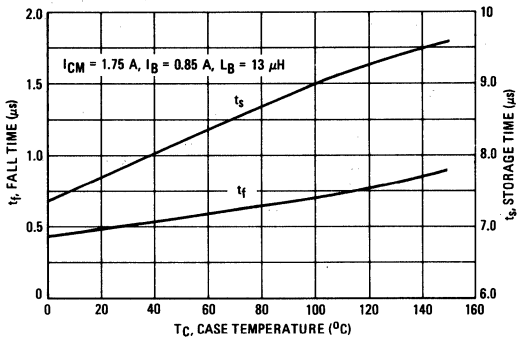


FIGURE 8 – OPTIMUM DRIVE CONDITIONS

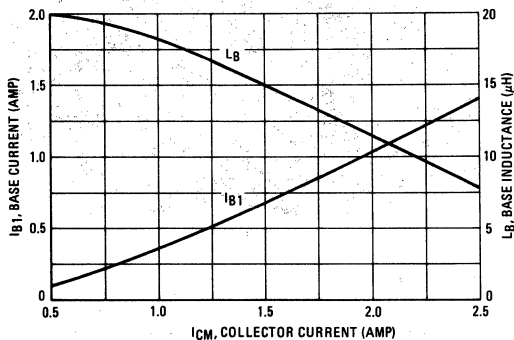
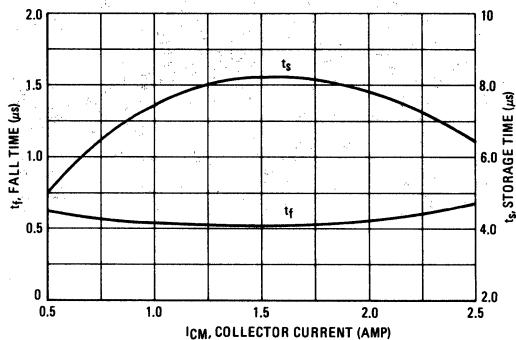


FIGURE 9 – SWITCHING BEHAVIOR versus I_{CM}



3

FIGURE 10 – THERMAL RESPONSE

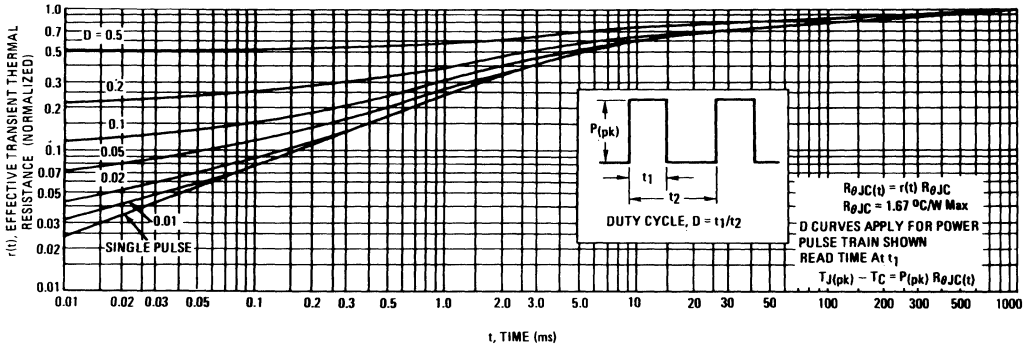


FIGURE 11 – COLLECTOR SATURATION REGION

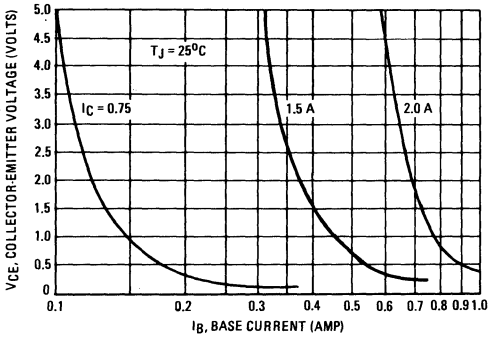


FIGURE 12 – DC CURRENT GAIN

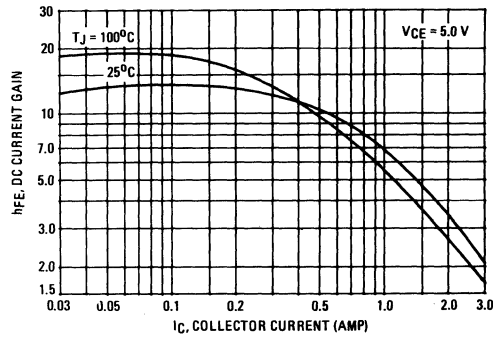


FIGURE 13 – "ON" VOLTAGES

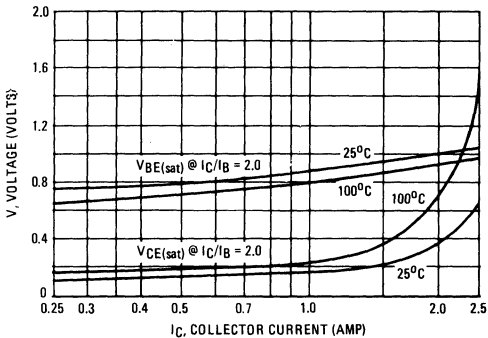
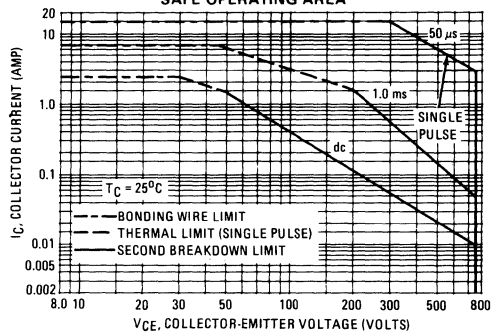


FIGURE 14 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA



NOTE:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 μs SB curve is beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

HORIZONTAL DEFLECTION TRANSISTOR

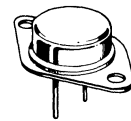
... specifically designed for use in CRT deflection circuits.

- Collector-Emitter Voltage — $V_{CEX} = 1500$ Volts
- Glassivated Base-Collector Junction
- Forward Bias Safe Operating Area @ $50 \mu s = 20$ A, 300 V
- Switching Times with Inductive Loads —
 $t_f = 0.5 \mu s$ (Typ) @ $I_C = 3.0$ A

4 AMPERE

NPN SILICON
POWER TRANSISTOR

1500 VOLTS
100 WATTS

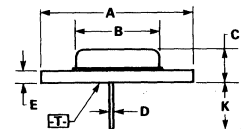


MAXIMUM RATINGS

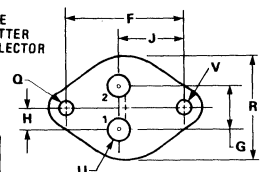
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector-Current — Continuous	I_C	4.0	Adc
Base Current — Continuous	I_B	3.0	Adc
Emitter Current — Continuous	I_E	7.0	Adc
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	100	Watts
$T_C = 100^\circ C$		40	Watts
Derate above $25^\circ C$		0.8	W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes. 1/8" from Case for 5 Seconds	T_L	275	$^\circ C$



STYLE 1:
 PIN 1, BASE
 2, EMITTER
 CASE-COLLECTOR



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
 2. T_1 IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
 ± 0.13 (0.005) M T V M

FOR LEADS:

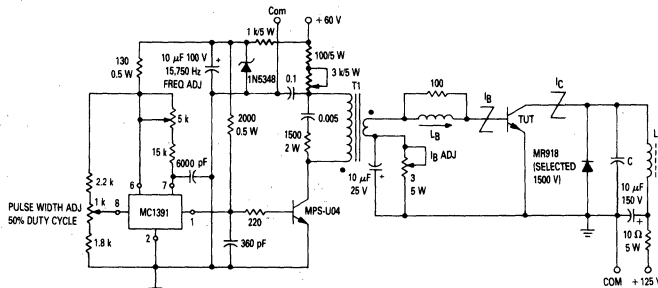
± 0.13 (0.005) M T V M Q M

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.37	—	1.550	—
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

FIGURE 1 — TEST CIRCUIT



DRIVER TRANSFORMER (T1)

- Ferroxcube pot core #4229P-L00-3C8
- Adjust gap for primary inductance $L_p = 70$ mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than 3 μH
- Use 3 mil mylar tape between each winding layer

I_C A	L mH	C μF
3.0	1.00	0.012

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage ($I_C = 50 \text{ mAdc}, I_B = 0$)	$V_{CE(sus)}$	750	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 1500 \text{ Vdc}, V_{BE} = 0$)	I_{CES}	—	—	1.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	—	1.0	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage ($I_C = 3.0 \text{ Adc}, I_B = 1.2 \text{ Adc}$)	$V_{CE(sat)}$	—	—	5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0 \text{ Adc}, I_B = 1.2 \text{ Adc}$)	$V_{BE(sat)}$	—	—	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 5			—
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product ($I_C = 0.1 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}, f_{test} = 1.0 \text{ MHz}$)	f_T	—	4	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz}$)	C_{ob}	—	90	—	pF
SWITCHING CHARACTERISTICS					
Fall Time ($I_C = 3.0 \text{ Adc}, I_{B1} = 1.2 \text{ Adc}, L_B = 8.0 \mu\text{H}$, See Figure 1)	t_f	—	0.5	1.0	μs

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle = 2%.

FIGURE 2 – DC CURRENT GAIN

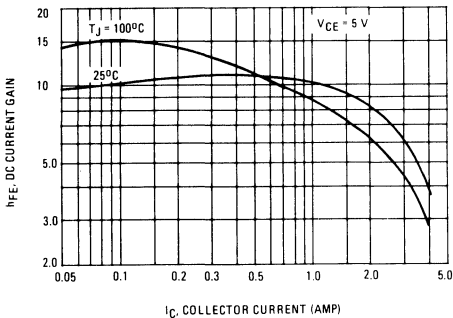


FIGURE 3 – COLLECTOR SATURATION REGION

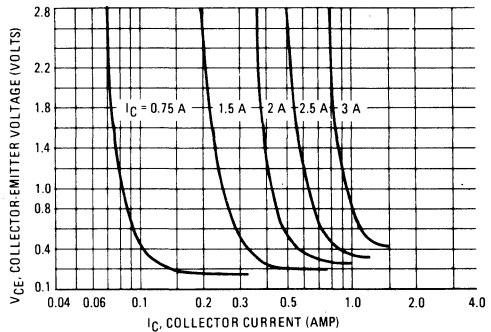


FIGURE 4 – "ON" VOLTAGES

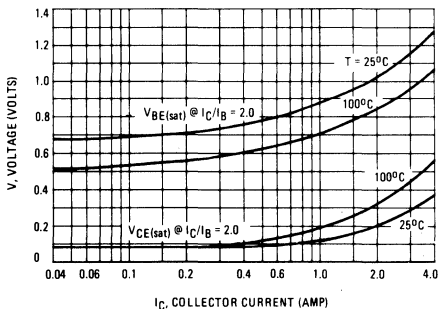
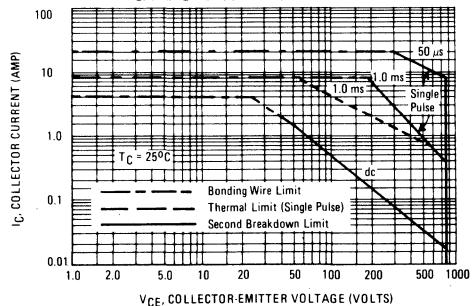


FIGURE 5 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA



NOTE:
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The $50 \mu\text{s}$ and 1 ms curves are beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

... specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage – $V_{CEX} = 1500$ Vdc
- Glassivated Base-Collector Junction
- Safe Operating Area @ $50 \mu s = 20$ A, 400 V
- Switching Times with Inductive Loads –
 $t_f = 0.4 \mu s$ (Typ) @ $I_C = 4.5$ A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	5.0	Adc
Base Current – Continuous	I_B	4.0	Adc
Emitter Current – Continuous	I_E	9.0	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ @ $T_C = 100^\circ C$ Derate above $25^\circ C$	P_D	100 40 0.8	Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ C$

THERMAL CHARACTERISTICS

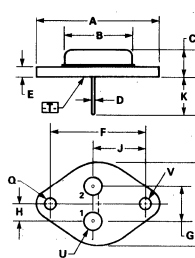
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ C$

Designer's Data for "Worst Case" Conditions

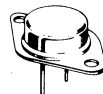
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

5.0 AMPERE
NPN SILICON
POWER TRANSISTORS

1500 VOLTS
100 WATTS



MJ12004

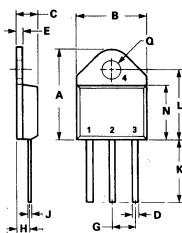


STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

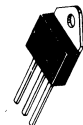
- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. [] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q
FOR LEADS:
 ± 0.13 (0.005) [] T | V [] Q []
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5,
1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.69	0.038	0.063
E	1.40	1.78	0.055	0.070
F	30.15	BSC	1.187	BSC
G	10.92	BSC	0.430	BSC
H	5.46	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.151	0.165
M	—	26.67	—	1.050
N	4.83	5.33	0.190	0.210
O	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA



MJH12004



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES		
	MIN	MAX	MIN	MAX	
A	20.32	21.08	0.800	0.830	
B	15.49	15.90	0.610	0.626	
C	4.19	5.08	0.165	0.200	
D	1.02	1.65	0.040	0.065	
E	1.25	1.65	0.050	0.065	
F	5.21	5.72	0.205	0.225	
G	H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025	
K	12.70	15.49	0.500	0.610	
L	15.89	16.51	0.625	0.650	
M	12.19	12.70	0.480	0.500	
N	4.04	4.22	0.159	0.166	

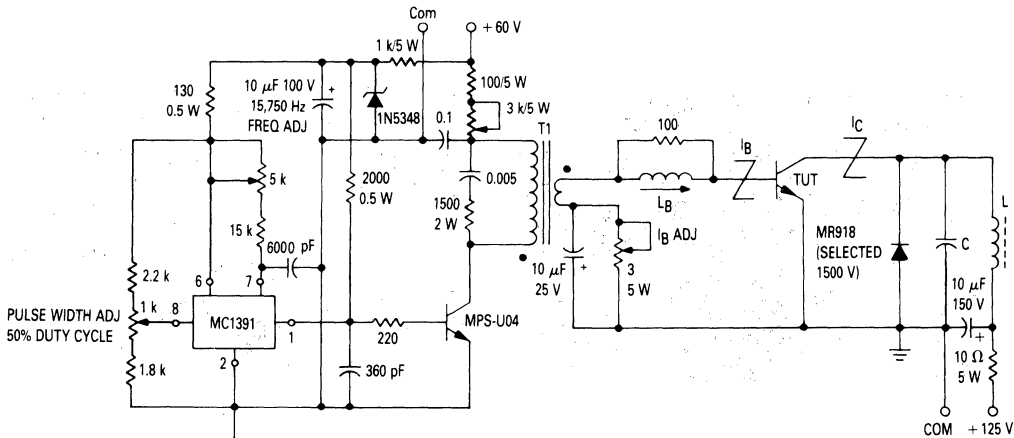
CASE 340-01
TO-218AC

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage ($I_C = 50 \text{ mAdc}, I_B = 0$)	$V_{CE(sus)}$	750	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 1500 \text{ Vdc}, V_{BE} = 0$)	I_{CES}	—	—	1.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	—	1.0	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage ($I_C = 4.5 \text{ Adc}, I_B = 1.8 \text{ Adc}$) ($I_C = 3.5 \text{ Adc}, I_B = 1.5 \text{ Adc}$)	$V_{CE(sat)}$	—	—	5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 4.5 \text{ Adc}, I_B = 1.8 \text{ Adc}$) ($I_C = 3.5 \text{ Adc}, I_B = 1.5 \text{ Adc}$)	$V_{BE(sat)}$	—	—	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14			
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product ($I_C = 0.1 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}, f_{test} = 1 \text{ MHz}$)	f_T	—	4	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz}$)	C_{ob}	—	125	—	pF
SWITCHING CHARACTERISTICS					
Fall Time ($I_C = 4.5 \text{ Adc}, I_{B1} = 1.8 \text{ Adc},$ $L_B = 8.0 \mu\text{H}, \text{ See Figure 1}$)	t_f	$T_C = 25^\circ\text{C}$ — $T_C = 100^\circ\text{C}$	0.4 — 0.6	1.0 — —	μs

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle = 2%.

Figure 1. Switching Times Test Circuit



DRIVER TRANSFORMER (T1)

- Ferroxcube pot core #4229P-L00-3C8
- Adjust gap for primary inductance $L_p = 70 \text{ mH}$ (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than $3 \mu\text{H}$
- Use 3 mil mylar tape between each winding layer

I_C A	L mH	C μF
3.5	0.87	0.013
4.5	0.67	0.017

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM} . Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM} , I_{B1} , and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B , at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown

in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1} , and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1} h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM} . As L_B is increased, the curves become broader and flatter above the $I_{B1} h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE} , essentially moves the curves to the left or right according to the relation $I_{B1} h_{FE} = \text{constant}$. It then becomes obvious that, for a specified I_{CM} , an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1} . The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM} . These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

3

TEST CIRCUIT WAVEFORMS

FIGURE 2

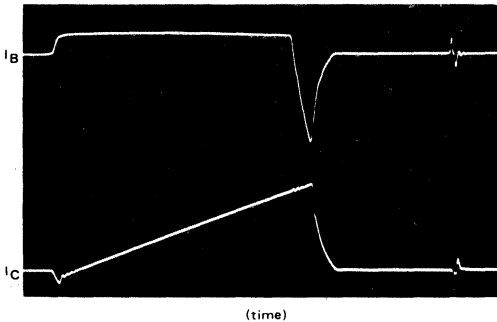
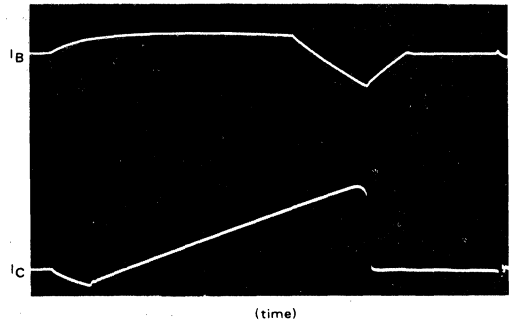


FIGURE 3



TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 – OPTIMIZING DRIVE @ 3.5 A

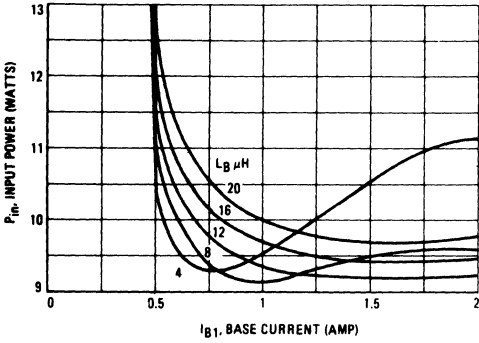


FIGURE 6 – SWITCHING BEHAVIOR versus TEMPERATURE
 $I_{CM} = 3.5$ A, $I_B = 1.5$ A, $L_B = 14 \mu H$

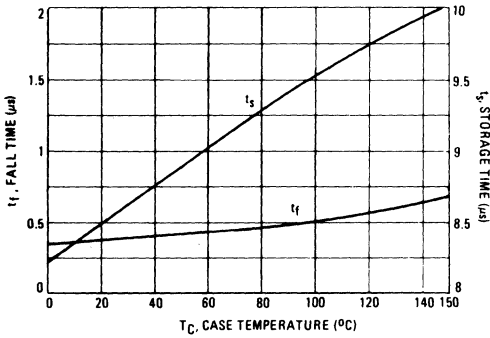


FIGURE 8 – OPTIMUM DRIVE CONDITIONS

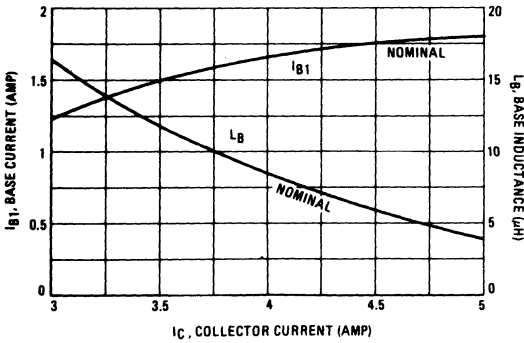


FIGURE 5 – OPTIMIZING DRIVE @ 4.5 A

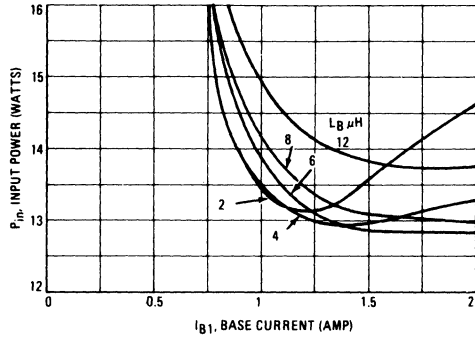


FIGURE 7 – SWITCHING BEHAVIOR versus TEMPERATURE
 $I_{CM} = 4.5$ A, $I_B = 1.75$ A, $L_B = 8 \mu H$

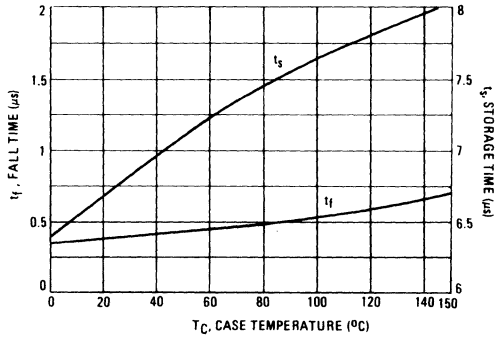
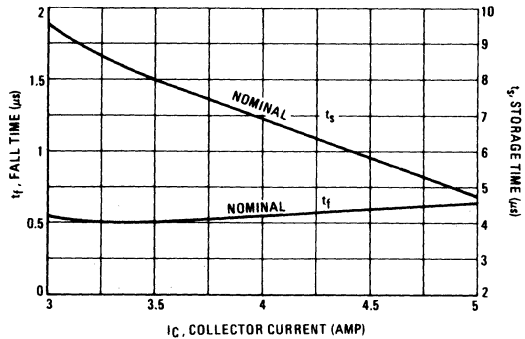


FIGURE 9 – SWITCHING BEHAVIOR versus I_{CM}



3

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 10 — DC CURRENT GAIN

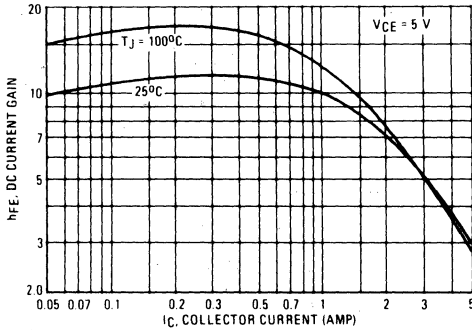
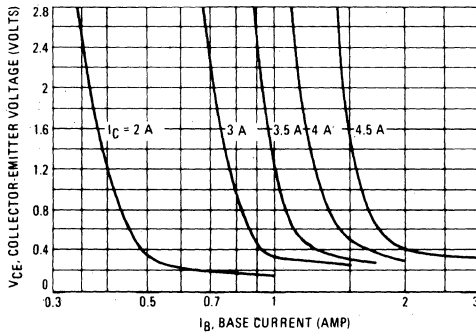
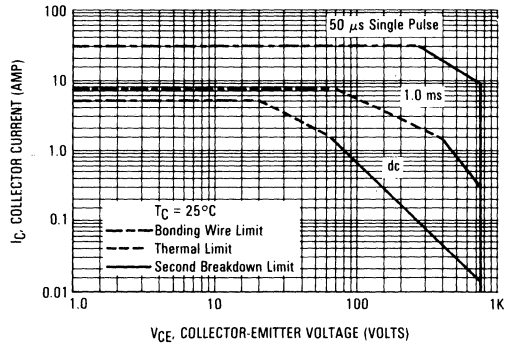


FIGURE 12 — COLLECTOR SATURATION REGION



SAFE OPERATING AREA INFORMATION

FIGURE 11 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

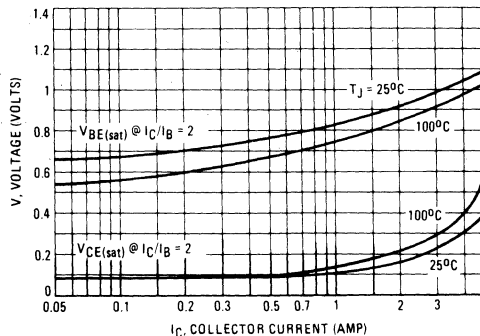


NOTE:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC—VCE limits of the transistor must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 µs SB curve is beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

FIGURE 13 — "ON" VOLTAGES



THERMAL RESPONSE

FIGURE 14 — MJ12004

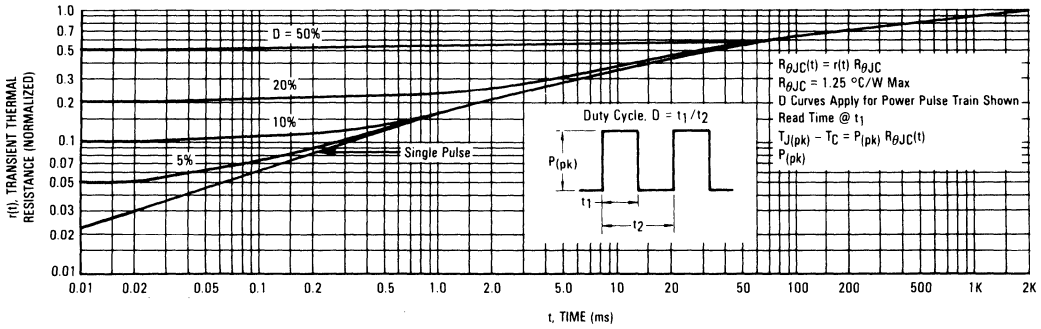
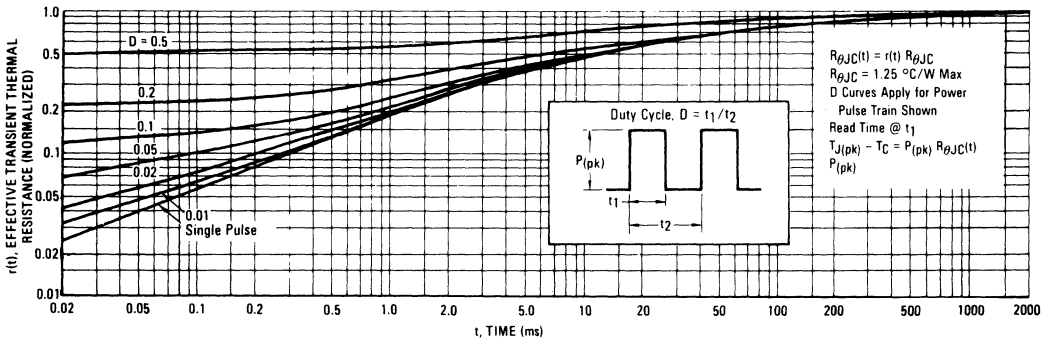


FIGURE 15 — MJH12004



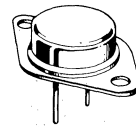
HORIZONTAL DEFLECTION TRANSISTOR

... specifically designed for use in deflection circuits.

- $V_{CEX} = 1500$ V
- Glassivated Base-Collector Junction
- Safe Operating Area @ $50 \mu s = 20$ A, 400 V

8 AMPERE
NPN SILICON
POWER TRANSISTOR

1500 VOLTS
100 WATTS

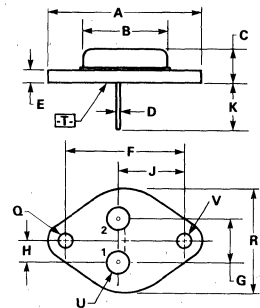


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	8.0	A dc
Base Current — Continuous	I_B	4.0	A dc
Emitter Current — Continuous	I_E	12	A dc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	100 0.8	Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ C$

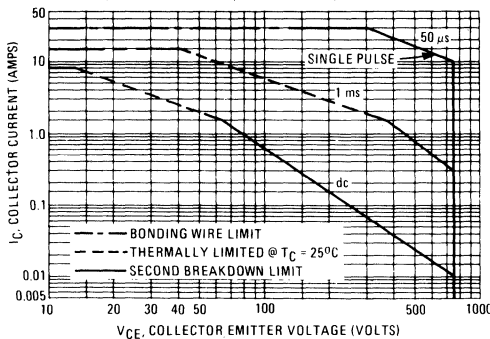
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ C$



- NOTES:
- DIMENSIONS Q AND V ARE DATUMS.
 - \square IS SEATING PLANE AND DATUM.
 - POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
 $\pm 0.13 (0.005) \text{ M } \text{ T } \text{ V } \text{ M}$
 FOR LEADS:
 $\pm 0.13 (0.005) \text{ M } \text{ T } \text{ V } \text{ M } \text{ Q } \text{ M}$
 - DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

FIGURE 1 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



STYLE 1:
 PIN 1, BASE
 2, EMITTER
 CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.46 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($V_C = 50\text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	750	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 1500\text{ Vdc}$, $V_{BE} = 0$)	I_{CES}	—	—	0.25	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	0.1	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$)	$V_{CE(sat)}$	—	—	5.0	Vdc
Base Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$)	$V_{BE(sat)}$	—	—	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	—	—	See Figure 1	
SWITCHING CHARACTERISTICS					
Fall Time ($I_C = 5.0\text{ Adc}$, $I_{B1} = 1.0\text{ Adc}$, $L_B = 8.0\text{ }\mu\text{H}$)	t_f	—	0.4	1.0	μs

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle = 2%.

FIGURE 2 – DC CURRENT GAIN

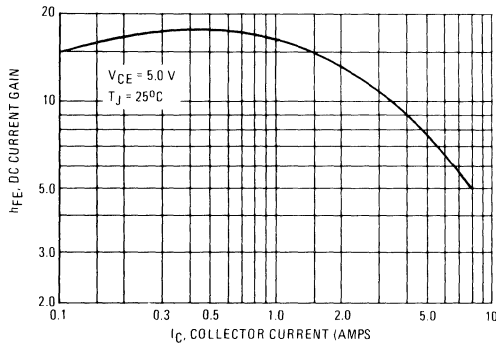
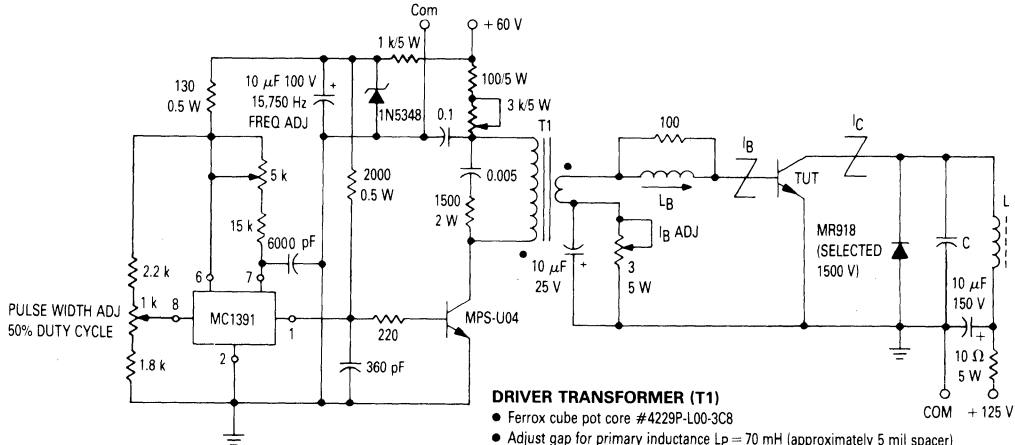


FIGURE 3 – SWITCHING TIMES TEST CIRCUIT



DRIVER TRANSFORMER (T1)

- Ferrous cube pot core #4229P-L00-3C8
- Adjust gap for primary inductance $L_p = 70\text{ mH}$ (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
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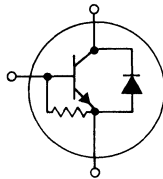
I_C A	L mH	C μF
5.0	0.575	0.018

Designers Data Sheet

**NPN HORIZONTAL DEFLECTION TRANSISTOR
 WITH INTEGRATED DAMPER DIODE**

... specifically designed for use in large-screen color-deflection circuits.

- Collector-Emitter Voltage — $V_{CEX} = 1500$ Vdc
- Glassivated Base-Collector Junction
- Safe Operating Area @ $50 \mu s = 20$ A, 400 V
- Switching Times with Inductive Loads —
 $t_f = 0.4 \mu s$ (Typ) @ $I_C = 5.0$ A
- C-E Diode Forward Voltage Specified



MAXIMUM RATINGS

Rating	Symbol	MJ12005D	Unit
Collector-Emitter Voltage	V_{CEO}	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
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Emitter Current — Continuous	I_E	12	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ @ $T_C = 100^\circ C$	P_D	100 40	Watts
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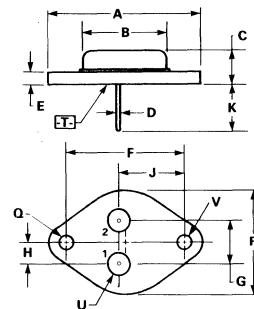
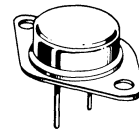
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Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

8.0 AMPERE
NPN SILICON
POWER TRANSISTORS

1500 VOLTS
100 WATTS



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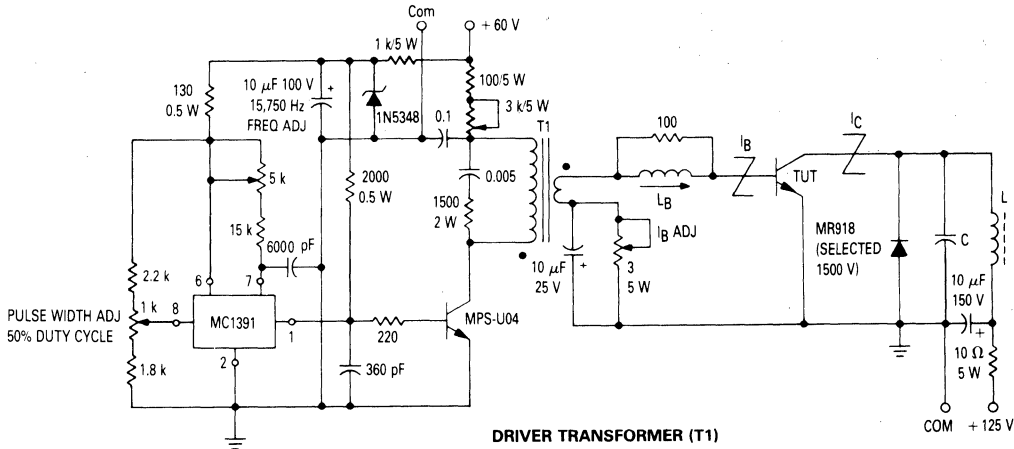
CASE 1-05
TO-204AA

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Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	200	mAdc
ON CHARACTERISTICS (1)					
Diode Forward Voltage ($I_F = 8.0\text{ Amps}$)	$V_{F(VEC)}$	—	—	2.5	Vdc
Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 8.0\text{ Adc}$, $I_B = 2.5\text{ Adc}$)	$V_{CE(sat)}$	—	—	5.0 5.0	Vdc
Base Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 8.0\text{ Adc}$, $I_B = 2.5\text{ Adc}$)	$V_{BE(sat)}$	—	—	1.5 1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14			
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product ($I_C = 0.1\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$, $f_{test} = 1.0\text{ MHz}$)	f_T	—	4.0	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	—	150	—	pF
SWITCHING CHARACTERISTICS					
Fall Time ($I_C = 5.0\text{ Adc}$, $I_{B1} = 1.5\text{ Adc}$, $I_B = 8.0\text{ }\mu\text{H}$, See Figure 1)	t_f	—	0.4 0.6	1.0 —	μs

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle = 2.0%.

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



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- Secondary leakage inductance should be less than $3\text{ }\mu\text{H}$
- Use 3 mil mylar tape between each winding layer

I_C A	L mH	C μF
5.0	0.57	0.018
7.0	0.45	0.025

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM} . Worst-case component variations and maximum high voltage loading must also be taken into account.

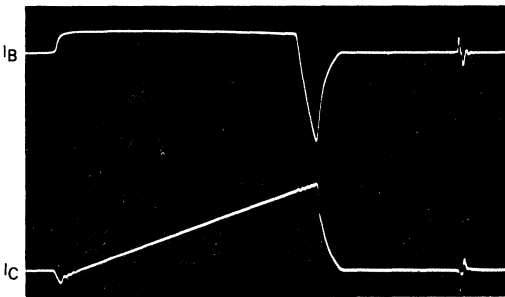
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Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM} , I_{B1} , and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B , at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values

of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1} , and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1} h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM} . As L_B is increased, the curves become broader and flatter above the $I_{B1} h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE} , essentially moves the curves to the left or right according to the relation $I_{B1} h_{FE} = \text{constant}$. It then becomes obvious that, for a specified I_{CM} , an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1} . The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM} . These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

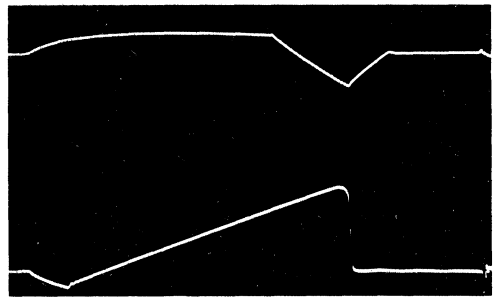
TEST CIRCUIT WAVEFORMS

FIGURE 2



(time)

FIGURE 3



(time)

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

3

FIGURE 4 — OPTIMIZING DRIVE @ 5.0 A

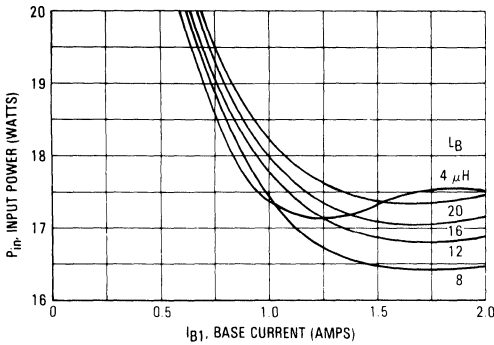


FIGURE 5 — OPTIMIZING DRIVE @ 7.0 A

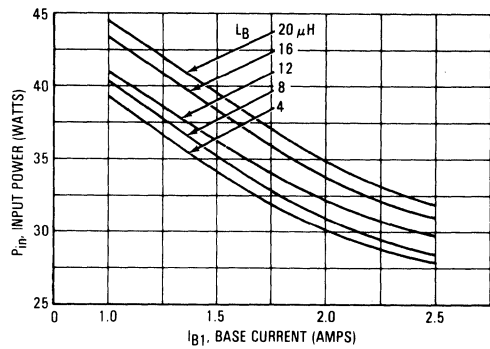


FIGURE 6 — SWITCHING BEHAVIOR versus TEMPERATURE

$I_{CM} = 5.0$ A, $I_B = 1.5$ A, $L_B = 8.0$ μ H

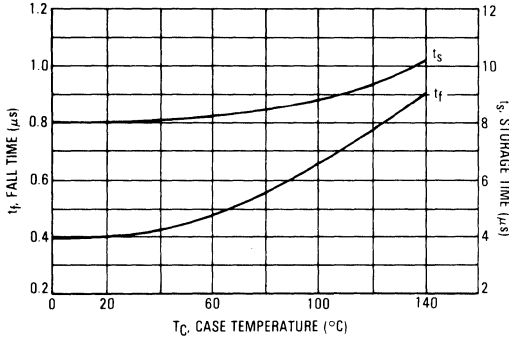


FIGURE 7 — SWITCHING BEHAVIOR versus TEMPERATURE

$I_{CM} = 7.0$ A, $I_B = 2.0$ A, $L_B = 4.0$ μ H

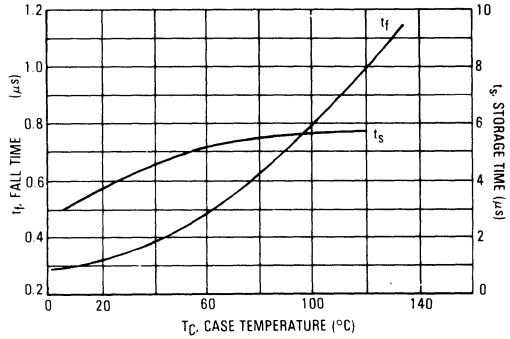


FIGURE 8 — OPTIMUM DRIVE CONDITIONS

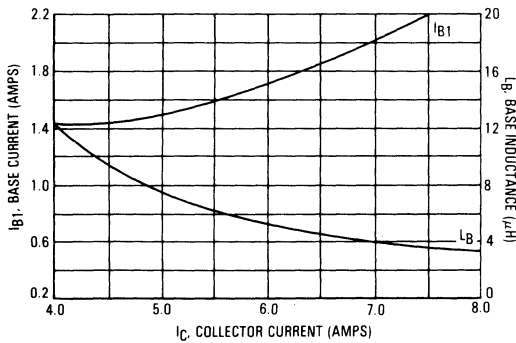


FIGURE 9 — SWITCHING BEHAVIOR versus I_{CM} AT 25°C

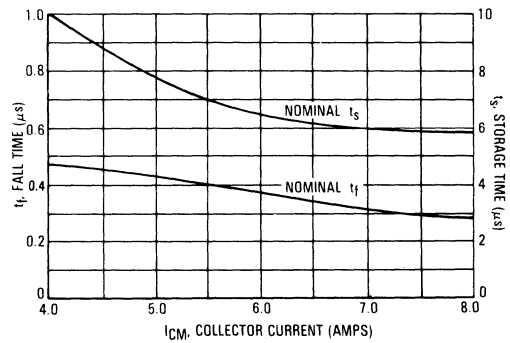


FIGURE 10 — THERMAL RESPONSE

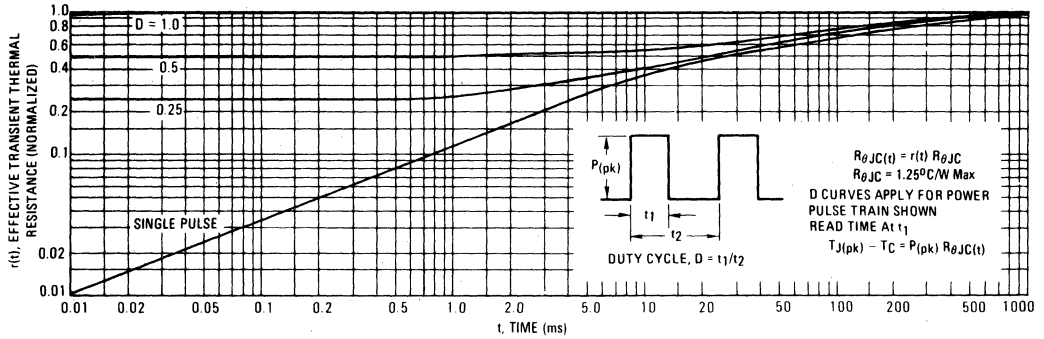


FIGURE 11 — COLLECTOR SATURATION REGION

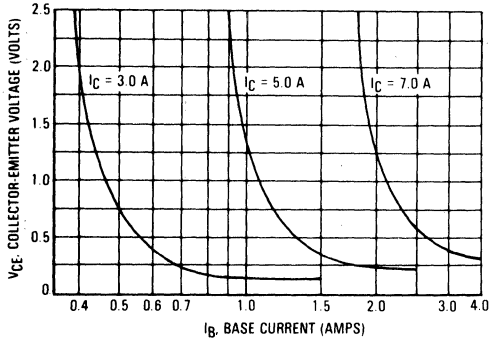


FIGURE 12 — DC CURRENT GAIN versus COLLECTOR CURRENT

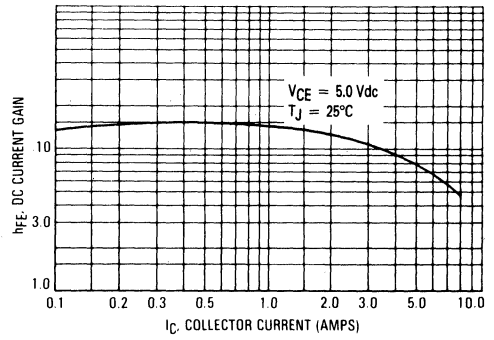
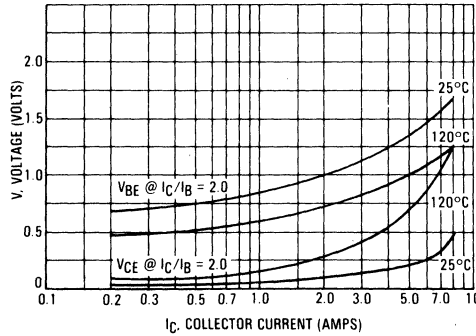
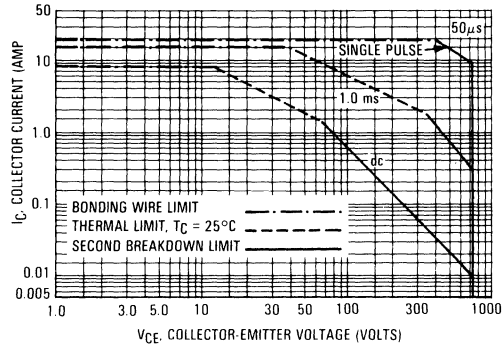


FIGURE 13 — "ON" VOLTAGES



3

**FIGURE 14 — MAXIMUM FORWARD BIAS
SAFE OPERATING AREA**



NOTE:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 μs SB curve is beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without falling.

HORIZONTAL DEFLECTION TRANSISTOR

... specifically designed for use in CRT deflection circuits.

- Collector-Emitter Voltage – $V_{CEX} = 950$ Volts
- Glassivated Base-Collector Junction
- Forward Bias Safe Operating Area @ $50 \mu s = 30$ A, 300 V
- Switching Times with Inductive Loads –
 $t_f = 0.5 \mu s$ (Typ) @ $I_C = 5.0$ A

MAXIMUM RATINGS

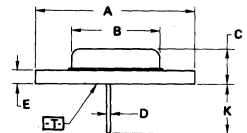
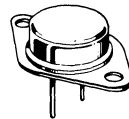
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	400	Vdc
Collector-Emitter Voltage	V_{CEX}	950	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector-Current – Continuous	I_C	10	Adc
Base Current – Continuous	I_B	5.0	Adc
Emitter Current – Continuous	I_E	15	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ $T_C = 100^\circ C$	P_D	100 40	Watts Watts
Derate above $25^\circ C$		0.8	$W/^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ C$

THERMAL CHARACTERISTICS

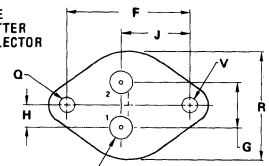
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ C$

10 AMPERE
NPN SILICON
POWER TRANSISTOR

950 VOLTS
100 WATTS



STYLE 1:
PIN 1: BASE
2: EMITTER
CASE-COLLECTOR



- NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
 2. \square IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$\phi \pm 0.13$ (0.005) M	T	V	Ⓞ
FOR LEADS:			
$\phi \pm 0.13$ (0.005) M	T	V	Ⓞ

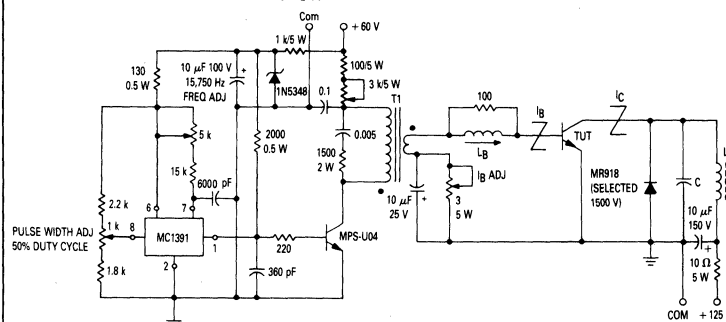
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.87	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30	15 BSC	1.187	BSC
G	10.92	BSC	0.430	BSC
H	5.46	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

3

FIGURE 1 – TEST CIRCUIT



DRIVER TRANSFORMER (T1)

- Ferroxcube pot core #4229P-L00-3CB
- Adjust gap for primary inductance $L_p = 70$ mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than $3 \mu H$
- Use 3 mil mylar tape between each winding layer

I_C A	L mH	C μF
5.0	0.57	0.039

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage ($I_C = 50 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	400	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 950 \text{ Vdc}$, $V_{BE} = 0$)	I_{CES}	—	—	1.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage ($I_C = 5.0 \text{ Adc}$, $I_B = 1.2 \text{ Adc}$)	$V_{CE(sat)}$	—	—	5.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0 \text{ Adc}$, $I_B = 1.2 \text{ Adc}$)	$V_{BE(sat)}$	—	—	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 5			—
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product ($I_C = 0.1 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$, $f_{test} = 1.0 \text{ MHz}$)	f_T	—	6.0	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	—	150	—	pF
SWITCHING CHARACTERISTICS					
Fall Time ($I_C = 5.0 \text{ Adc}$, $I_{B1} = 1.2 \text{ Adc}$, $L_B = 8.0 \mu\text{H}$, See Figure 1)	t_f	—	0.5	1.0	μs

(1) Pulse Test: Pulse Width < 300 μs , Duty Cycle = 2%.

FIGURE 2 – DC CURRENT GAIN

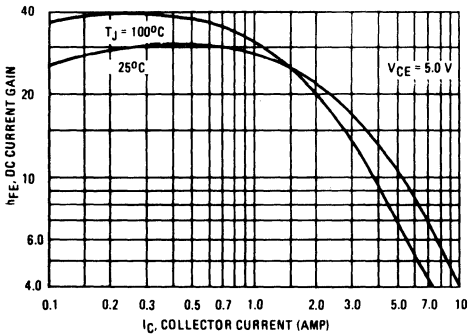


FIGURE 4 – "ON" VOLTAGES

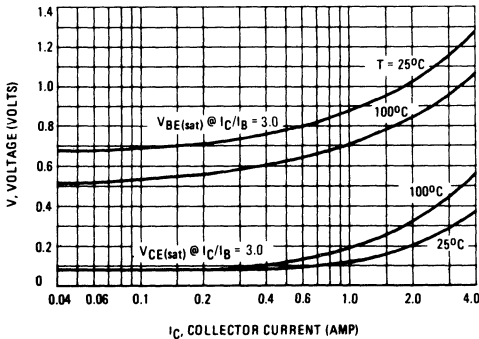


FIGURE 3 – COLLECTOR SATURATION REGION

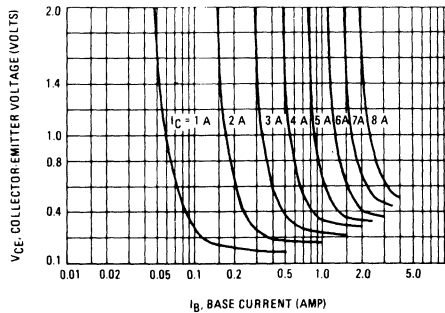
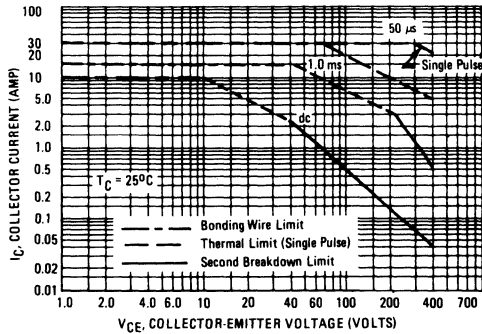


FIGURE 5 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA



NOTE:
 There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
 The 50 μs and 1 ms curves are beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.



MJ12020
MJ12021
MJ12022

Designer's Data Sheet

HIGH PERFORMANCE NPN DEFLECTION TRANSISTORS

These transistors are designed for high resolution video systems, such as, high density graphic displays, data terminals, video scanners . . . wherever high frequency deflection is required.

- Fast Turn-Off Times
- Maximum Storage and Fall Times Specified at 100°C
- Operating Junction Temperature Range -65°C to +200°C
- High f_T of 15 MHz

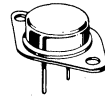
5.0, 8.0 and 15 AMPERE

NPN SILICON DEFLECTION POWER TRANSISTORS

850 VOLTS
125, 150 and 175 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



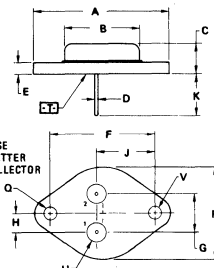
MAXIMUM RATINGS

Rating	Symbol	MJ12020	MJ12021	MJ12022	Unit
Collector-Emitter Voltage	V _{CEO}	450			Vdc
Collector-Emitter Voltage	V _{CEV}	850			Vdc
Emitter Base Voltage	V _{EB}	6.0			Vdc
Collector Current — Continuous	I _C	5.0	8.0	15	Adc
— Peak (1)	I _{CM}	10	16	20	
Base Current — Continuous	I _B	4.0	6.0	10	Adc
— Peak (1)	I _{BM}	8.0	12	15	
Total Power Dissipation @ T _C = 25°C	P _D	125	150	175	Watts
@ T _C = 100°C		71.5	85.5	100	
Derate above 25°C		0.714	0.86	1.0	W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200			°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	R _{θJC}	1.4	1.17	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275			°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

- NOTES:
1. DIMENSIONS D AND V ARE DATUMS.
2. [] IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D:
⊕ 0.13 (0.005) ⊙ T V ⊙ ⊙
FOR LEADS:
⊕ 0.13 (0.005) ⊙ T V ⊙ ⊙ ⊙
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	28.37	—	1.150
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.87	1.08	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.48 BSC	—	0.215 BSC	—
J	18.29 BSC	—	0.685 BSC	—
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.151	0.165
M	—	26.87	—	1.059
N	4.83	5.33	0.190	0.210
O	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA (TO-3)

MJ12020, MJ12021, MJ12022

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	450	—	—	Vdc
Collector Cutoff Current (V _{CEV} = 850 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = 850 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current (V _{CE} = 850 Vdc, R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V _{EB} = 6.0 Vdc, I _C = 0)	I _{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figures 19, 21 or 23			
Turn-Off SOA with Base Reverse Biased	RBSOA	See Figures 20, 22 or 24			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage (I _C = 3.0 Adc, I _B = 0.6 Adc) MJ12020 (I _C = 5.0 Adc, I _B = 1.0 Adc) MJ12021 (I _C = 10 Adc, I _B = 2.0 Adc) MJ12022	V _{CE(sat)}	—	—	1.2	Vdc
Base Emitter Saturation Voltage (I _C = 3.0 Adc, I _B = 0.6 Adc) MJ12020 (I _C = 5.0 Adc, I _B = 1.0 Adc) MJ12021 (I _C = 10 Adc, I _B = 2.0 Adc) MJ12022	V _{BE(sat)}	—	—	1.5	Vdc
DC Current Gain (I _C = 5.0 Adc, V _{CE} = 5.0 Vdc) MJ12020 (I _C = 8.0 Adc, V _{CE} = 5.0 Vdc) MJ12021 (I _C = 15 Adc, V _{CE} = 5.0 Vdc) MJ12022	h _{FE}	5.0	—	—	—

DYNAMIC CHARACTERISTICS

Current Gain Bandwidth Product (I _C = 0.3 Adc, V _{CE} = 10 Vdc, f = 1.0 MHz) MJ12020 (I _C = 1.0 Adc, V _{CE} = 10 Vdc, f = 1.0 MHz) MJ12021 (I _C = 1.3 Adc, V _{CE} = 10 Vdc, f = 1.0 MHz) MJ12022	f _T	15	—	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 kHz) MJ12020 MJ12021 MJ12022	C _{ob}	—	—	200 350 400	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

MJ12020, MJ12021, MJ12022

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit	
SWITCHING CHARACTERISTICS							
MJ12020							
Inductive Switching, Clamped Drive							
Storage Time	$(I_C = 3.0 \text{ Adc}, I_B = 0.6 \text{ Adc}, V_{CC} = 40 \text{ Vdc}, V_{BE(\text{off})} = 4.0 \text{ Vdc}, \text{Pulse Width} = 8.0 \mu\text{s}, \text{Duty Cycle} \leq 2\%)$ See Table 1	$T_J = 25^\circ\text{C}$	t_s	—	440	1200	ns
Fall Time			t_f	—	130	300	
Storage Time		$T_J = 100^\circ\text{C}$	t_s	—	550	1500	
Fall Time			t_f	—	200	500	
Inductive Switching, Series Base Inductance							
Fall Time	$(I_C = 3.0 \text{ Adc}, I_B = 0.6 \text{ Adc}, L_B = 24 \mu\text{H})$ See Table 2		t_f	—	175	—	ns
MJ12021							
Inductive Switching, Clamped Drive							
Storage Time	$(I_C = 5.0 \text{ Adc}, I_B = 1.0 \text{ Adc}, V_{CC} = 60 \text{ Vdc}, V_{BE(\text{off})} = 4.0 \text{ Vdc}, \text{Pulse Width} = 8.0 \mu\text{s}, \text{Duty Cycle} \leq 2\%)$ See Table 1	$T_J = 25^\circ\text{C}$	t_s	—	550	1200	ns
Fall Time			t_f	—	100	300	
Storage Time		$T_J = 100^\circ\text{C}$	t_s	—	750	1600	
Fall Time			t_f	—	180	500	
Inductive Switching, Series Base Inductance							
Fall Time	$(I_C = 5.0 \text{ Adc}, I_B = 1.0 \text{ Adc}, L_B = 24 \mu\text{H})$ See Table 2		t_f	—	300	—	ns
MJ12022							
Inductive Switching, Clamped Drive							
Storage Time	$(I_C = 10 \text{ Adc}, I_B = 2.0 \text{ Adc}, V_{CC} = 120 \text{ Vdc}, V_{BE(\text{off})} = 4.0 \text{ Vdc}, \text{Pulse Width} = 8.0 \mu\text{s}, \text{Duty Cycle} \leq 2\%)$ See Table 1	$T_J = 25^\circ\text{C}$	t_s	—	820	1800	ns
Fall Time			t_f	—	100	300	
Storage Time		$T_J = 100^\circ\text{C}$	t_s	—	1100	2500	
Fall Time			t_f	—	130	400	
Inductive Switching, Series Base Inductance							
Fall Time	$(I_C = 10 \text{ Adc}, I_B = 2.0 \text{ Adc}, L_B = 24 \mu\text{H})$ See Table 2		t_f	—	350	—	ns

TYPICAL ELECTRICAL CHARACTERISTICS

MJ12020

FIGURE 1 — DC CURRENT GAIN

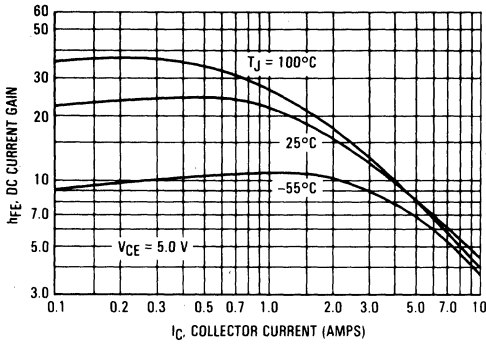
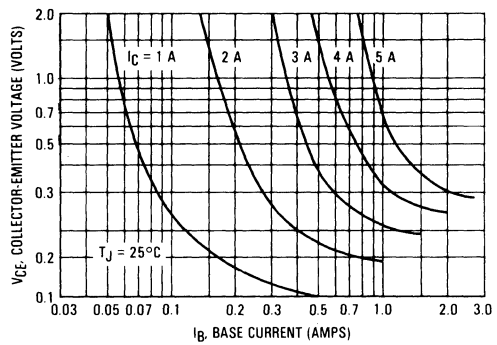


FIGURE 2 — COLLECTOR SATURATION REGION



MJ12021

FIGURE 3 — DC CURRENT GAIN

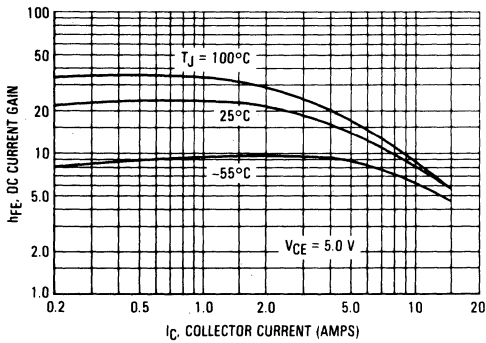
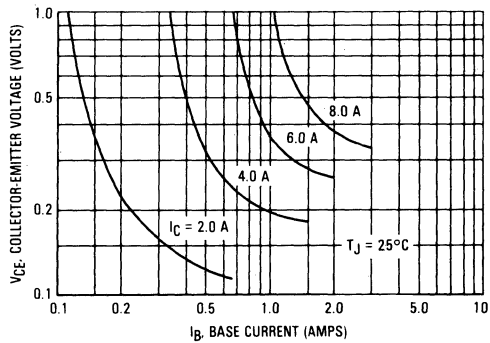


FIGURE 4 — COLLECTOR SATURATION REGION



MJ12022

FIGURE 5 — DC CURRENT GAIN

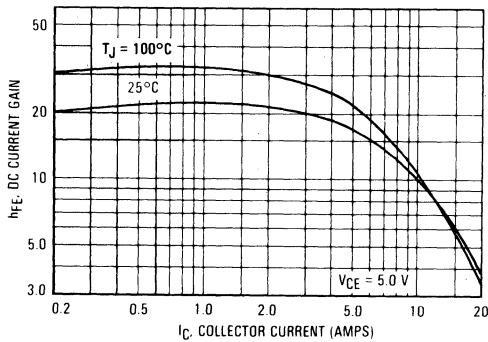
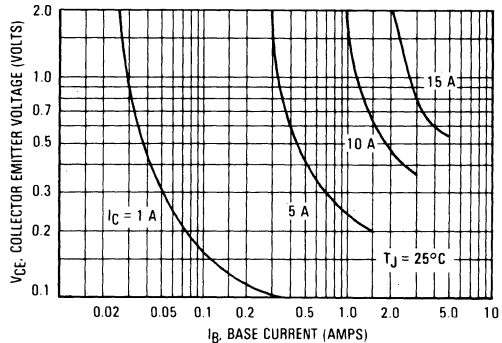


FIGURE 6 — COLLECTOR SATURATION REGION



TYPICAL ELECTRICAL CHARACTERISTICS

MJ12020

FIGURE 7 — COLLECTOR-EMITTER SATURATION VOLTAGE

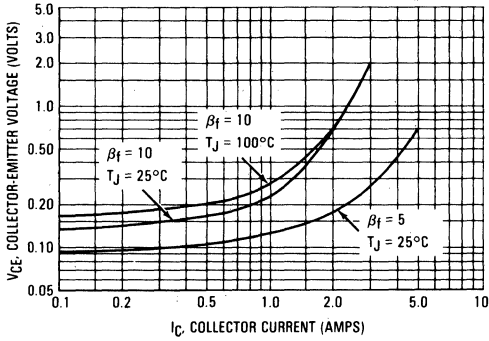
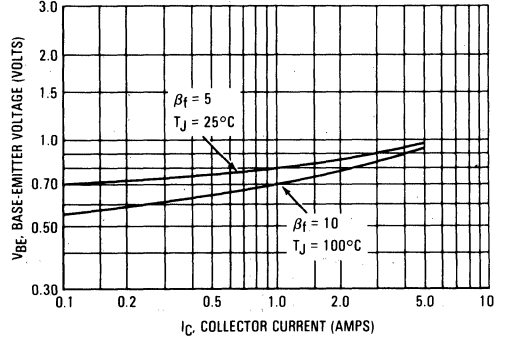


FIGURE 8 — BASE-EMITTER VOLTAGE



MJ12021

FIGURE 9 — COLLECTOR-EMITTER SATURATION VOLTAGE

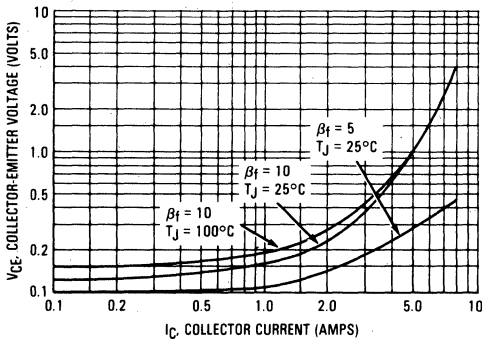
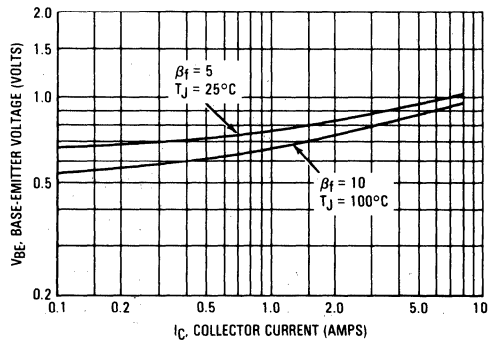


FIGURE 10 — BASE-EMITTER VOLTAGE



MJ12022

FIGURE 11 — COLLECTOR-EMITTER SATURATION VOLTAGE

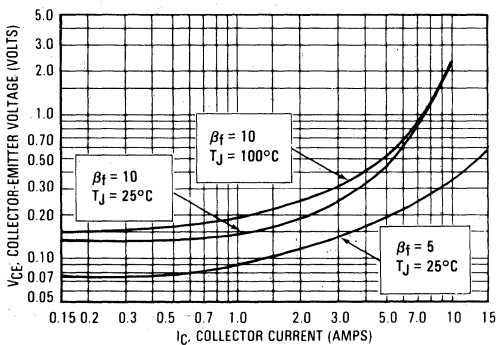
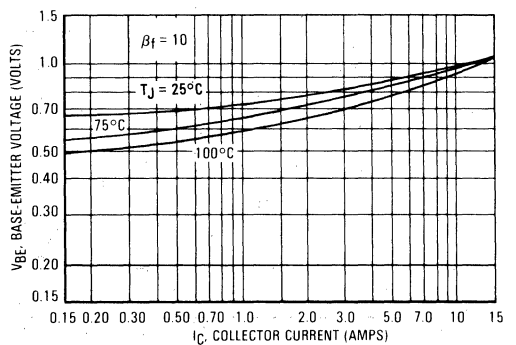


FIGURE 12 — BASE-EMITTER VOLTAGE



3

TYPICAL DYNAMIC CHARACTERISTICS

MJ12020

FIGURE 13 — STORAGE TIME

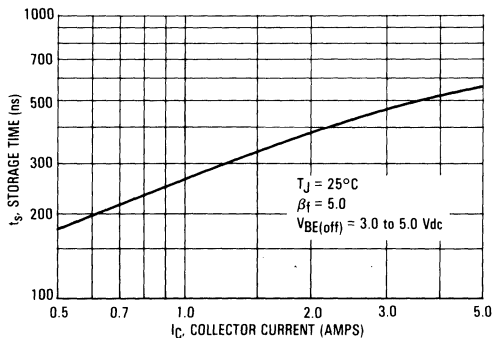
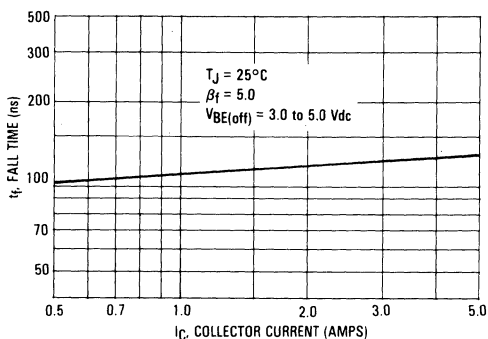


FIGURE 14 — FALL TIME



MJ12021

FIGURE 15 — STORAGE TIME

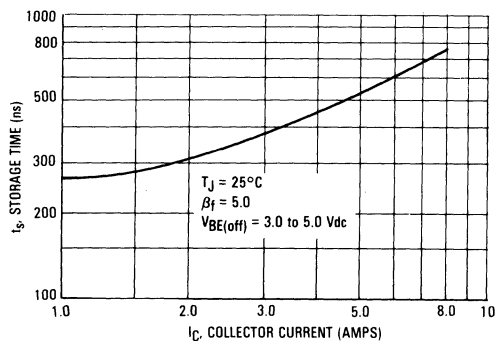
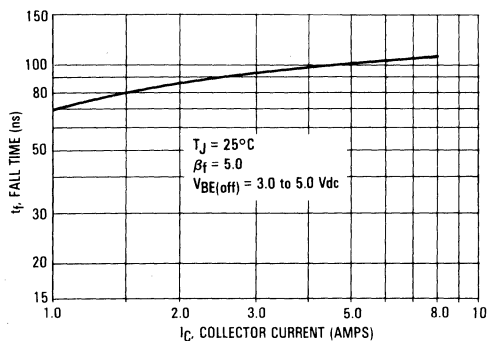


FIGURE 16 — FALL TIME



MJ12022

FIGURE 17 — STORAGE TIME

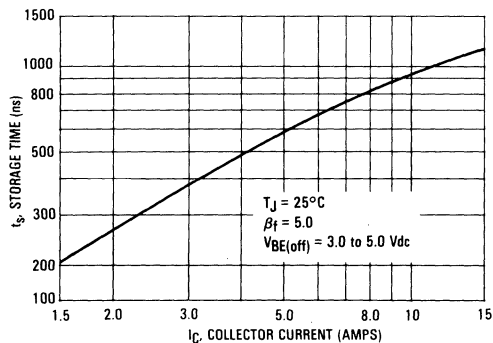
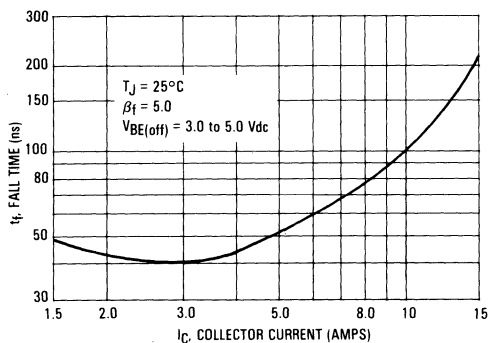


FIGURE 18 — FALL TIME



SAFE OPERATING AREA INFORMATION

MJ12020

FIGURE 19 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

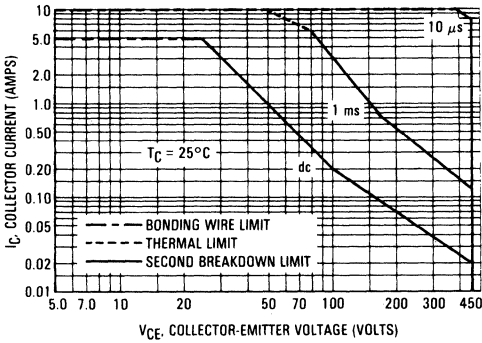
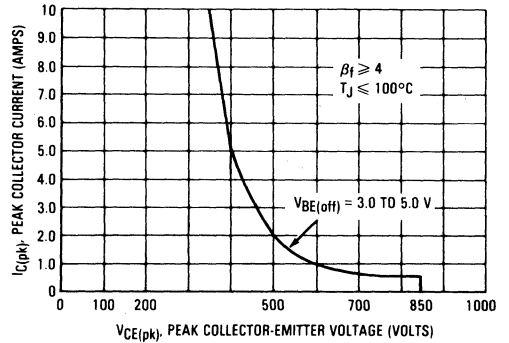


FIGURE 20 — MAXIMUM RATED TURN-OFF SAFE OPERATING AREA



MJ12021

FIGURE 21 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

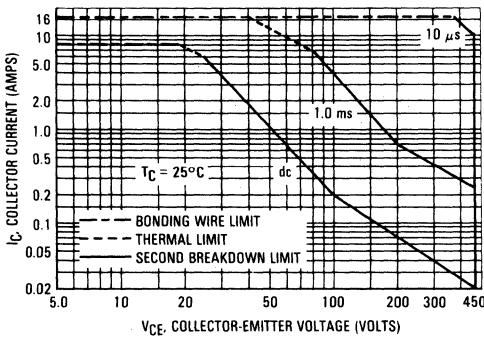
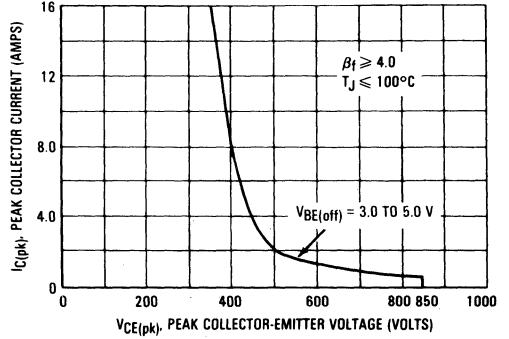


FIGURE 22 — MAXIMUM RATED TURN-OFF SAFE OPERATING AREA



MJ12022

FIGURE 23 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

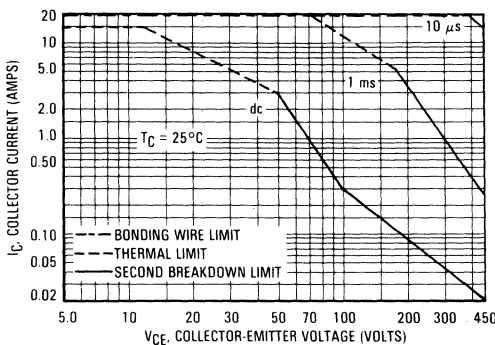
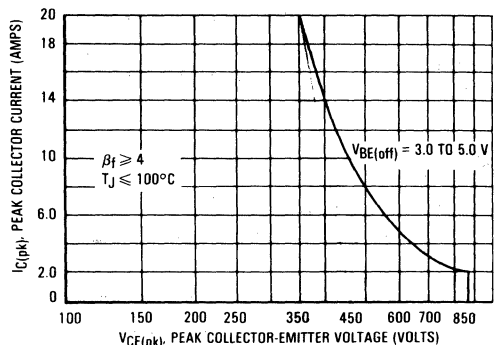


FIGURE 24 — MAXIMUM RATED TURN-OFF SAFE OPERATING AREA



3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

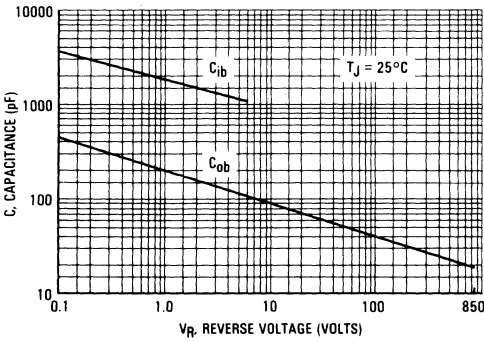
The data of Figures 19, 21 and 23 are based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 19, 21 and 23 may be found at any case temperature by using the appropriate curve on Figure 28.

$T_{J(pk)}$ may be calculated from the data in Figures 29, 30 or 31. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

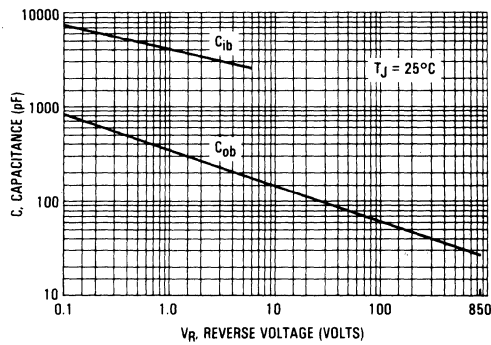
TURN-OFF

In deflection circuits, high voltage and high current normally do not occur simultaneously during turn-off with the base-emitter reverse biased. The safe level of operating these devices is specified as the Turn-Off Safe Operating Area, and represents the area the lead line may traverse during reverse biased turn off. For reliable operation, all abnormal operating conditions should be checked for operation within this area.

**FIGURE 25 — CAPACITANCE VARIATION
MJ12020**



**FIGURE 26 — CAPACITANCE VARIATION
MJ12021**



**FIGURE 27 — CAPACITANCE VARIATION
MJ12022**

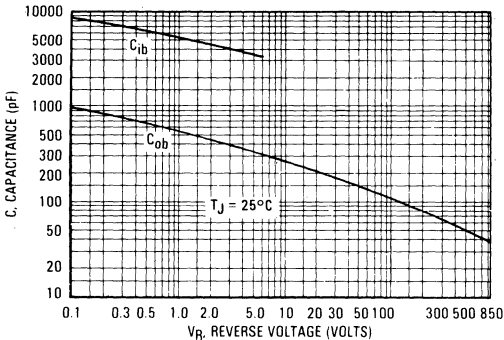
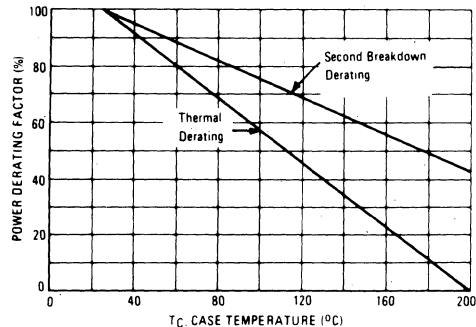


FIGURE 28 — POWER DERATING



THERMAL RESPONSE

FIGURE 29 — MJ12020

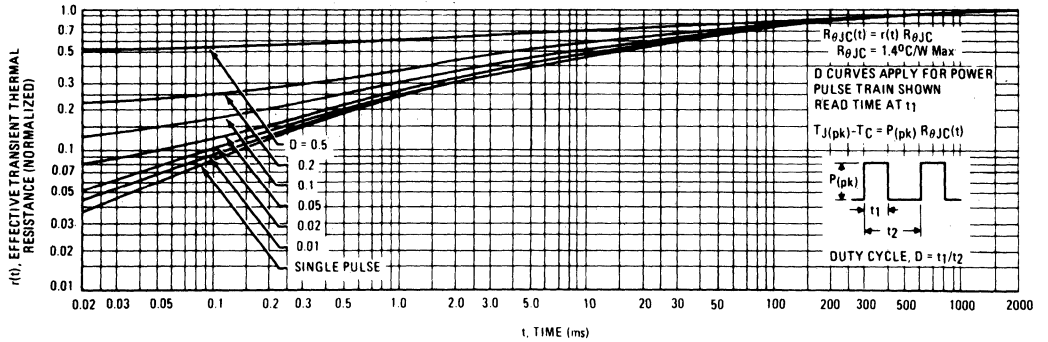


FIGURE 30 — MJ12021

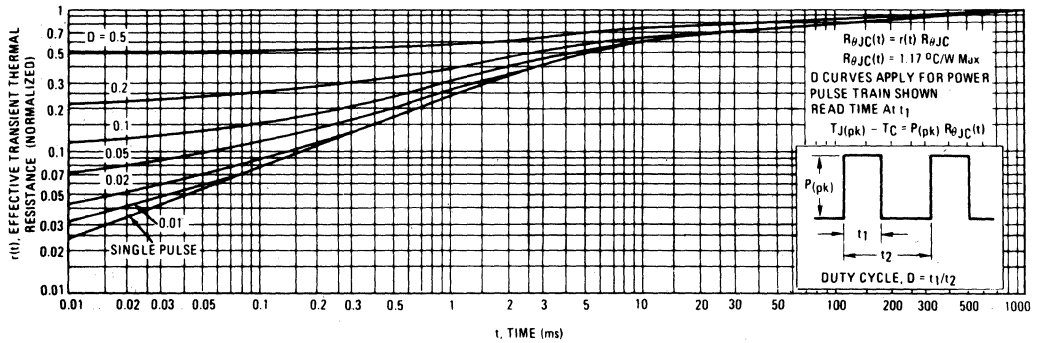


FIGURE 31 — MJ12022

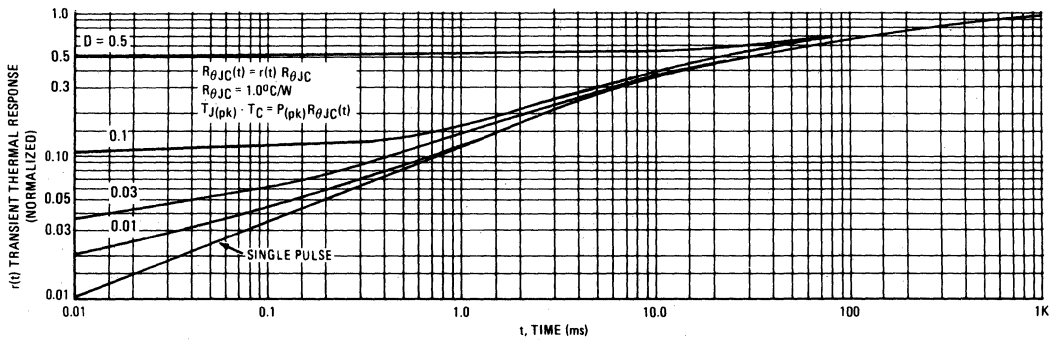
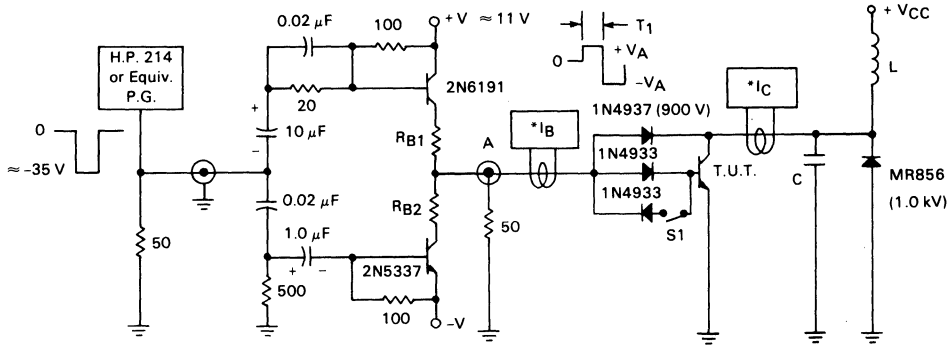


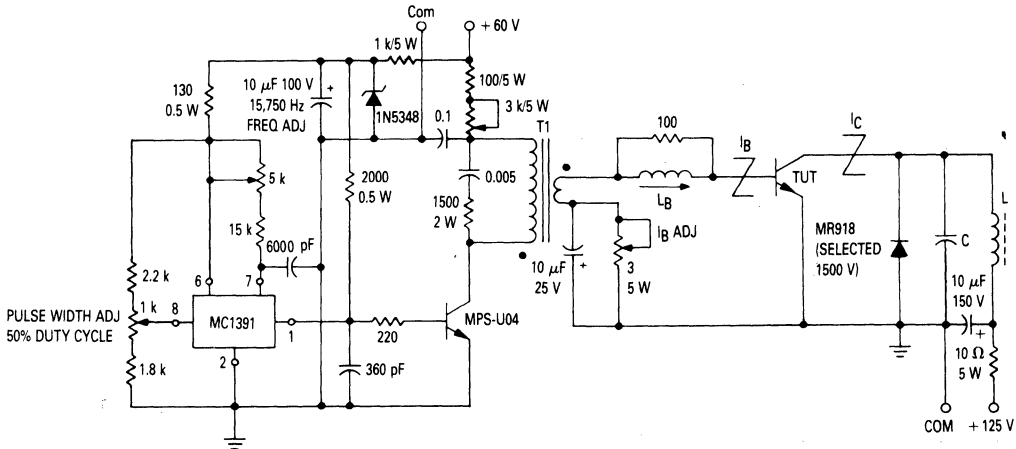
TABLE 1 — TEST CONDITIONS FOR DYNAMIC PERFORMANCE



T₁ adjusted to obtain I_{C(pk)}
 -V_A adjusted to obtain V_{BE(off)}

V _{CE0} (sus) L = 10 mH R _{B2} = ∞ V _{CC} = 20 Vdc S1 — Open *Tektronix P-6042 or Equivalent	Inductive Switching, Clamped Drive			Turn-Off SOA		
	MJ12020	MJ12021	MJ12022	MJ12020	MJ12021	MJ12022
	C = 0.003 μF V _{CC} = 40 Vdc	C = 0.020 μF V _{CC} = 60 Vdc	C = 0.036 μF V _{CC} = 120 Vdc	C = 0.003 μF V _{CC} = 20 Vdc	C = 0.020 μF V _{CC} = 35 Vdc	C = 0.037 μF V _{CC} = 55 Vdc
	L = 100 μH, S1 — Closed R _{B2} = 0, R _{B1} selected for required I _{B1} Scope — Tektronix 7403 or Equivalent			L = 100 μH R _{B2} = 0, R _{B1} selected for required I _{B1} S1 — Closed		

TABLE 2 — TEST CIRCUIT FOR INDUCTIVE SWITCHING WITH BASE INDUCTANCE



DRIVER TRANSFORMER (T1)

- Ferroxcube pot core #4229P-100-3C8
- Adjust gap for primary inductance L_p = 70 mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than 3 μH
- Use 3 mil mylar tape between each winding layer

Device	V _{CC} (Volts)	I _{C(pk)} (Amp)	C (μF)
MJ12020	20	3.0	0.003
MJ12021	35	5.0	0.020
MJ12022	55	10	0.036

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ13014 and MJ13015 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

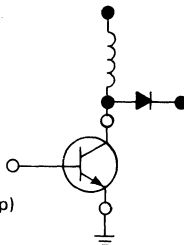
Fast Turn - Off Times:

- 60 ns Inductive Fall Time @ 25°C (Typ)
- 120 ns Inductive Crossover Time @ 25°C (Typ)
- 800 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



10 AMPERE

NPN SILICON
POWER TRANSISTORS

350 AND 400 VOLTS
 150 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.

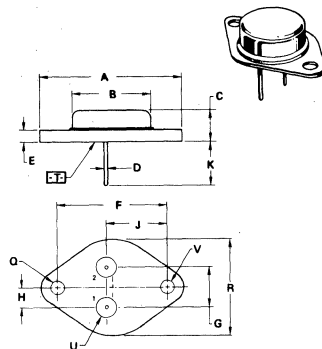
MAXIMUM RATINGS

Rating	Symbol	MJ13014	MJ13015	Unit
Collector-Emitter Voltage	V_{CE0}	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	550	600	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current - Continuous	I_C	10		Acd
Collector Current - Peak (1)	I_{CM}	20		
Base Current - Continuous	I_B	5.0		Acd
Base Current - Peak (1)	I_{BM}	10		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150		Watts
Derate above 25°C @ $T_C = 100^\circ\text{C}$		85.5		
		0.86		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.



- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. \square IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

$$\text{MOUNTING HOLE Q: } \text{M} \text{ } \text{N} \text{ } \text{O} \text{ } \text{P} \text{ } \text{Q} \text{ } \text{R} \text{ } \text{S} \text{ } \text{T} \text{ } \text{U} \text{ } \text{V} \text{ } \text{W} \text{ } \text{X} \text{ } \text{Y} \text{ } \text{Z}$$

FOR LEADS:

$$\text{FOR LEADS: } \text{M} \text{ } \text{N} \text{ } \text{O} \text{ } \text{P} \text{ } \text{Q} \text{ } \text{R} \text{ } \text{S} \text{ } \text{T} \text{ } \text{U} \text{ } \text{V} \text{ } \text{W} \text{ } \text{X} \text{ } \text{Y} \text{ } \text{Z}$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.06	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	19.82 BSC		0.780 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

MJ13014, MJ13015

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0)	MJ13014 MJ13015	V _{CEO(sus)}	350 400	— —	— —	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 150°C)		I _{CEV}	— —	— —	0.5 2.5	mAdc
Collector Cutoff Current (V _{CE} = Rated V _{CEV} , R _{BE} = 50 Ω, T _C = 100°C)		I _{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V _{EB} = 6.0 Vdc, I _C = 0)		I _{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	I _{S/b}	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 2.5 Adc, V _{CE} = 5 Vdc)	h _{FE}	12	—	40	—
Collector-Emitter Saturation Voltage (I _C = 5 Adc, I _B = 1.0 Adc) (I _C = 10 Adc, I _B = 2.0 Adc) (I _C = 5 Adc, I _B = 1.0 Adc, T _C = 100°C)	V _{CE(sat)}	— — —	— — —	1.4 5.0 2.4	Vdc
Base-Emitter Saturation Voltage (I _C = 5 Adc, I _B = 1.0 Adc) (I _C = 5 Adc, I _B = 1.0 Adc, T _C = 100°C)	V _{BE(sat)}	— —	— —	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1.0 kHz)	C _{ob}	50	—	350	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 250 Vdc, I _C = 5.0 A, I _{B1} = 1.0 A, t _p = 25 μs, Duty Cycle ≈ 2%)	t _d	—	0.01	0.1	μs
Rise Time		t _r	—	0.085	0.5	μs
Storage Time	(V _{CC} = 250 Vdc, I _C = 5.0 A, I _{B1} = 1.0 A, V _{BE(off)} = 5.0 Vdc, t _p = 25 μs, Duty Cycle ≈ 2%)	t _s	—	0.8	2.0	μs
Fall Time		t _f	—	0.095	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I _C = 5 A (pk), V _{clamp} = 250 Vdc, I _{B1} = 1.0 A, V _{BE(off)} = 5 Vdc, T _C = 100°C)	t _{sv}	—	1.5	3.5	μs
Crossover Time		t _c	—	0.25	1.0	μs
Fall Time		t _{fi}	—	0.12	—	μs
Storage Time	(I _C = 5 A (pk), V _{clamp} = 250 Vdc, I _{B1} = 1.0 A, V _{BE(off)} = 5 Vdc, T _C = 25°C)	t _{sv}	—	0.8	—	μs
Crossover Time		t _c	—	0.12	—	μs
Fall Time		t _{fi}	—	0.06	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

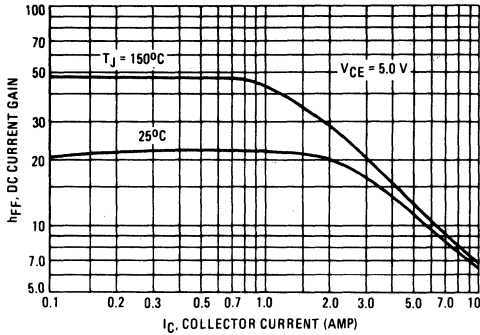


FIGURE 2 – COLLECTOR SATURATION REGION

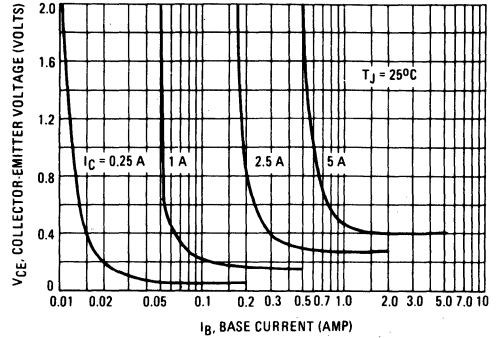


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

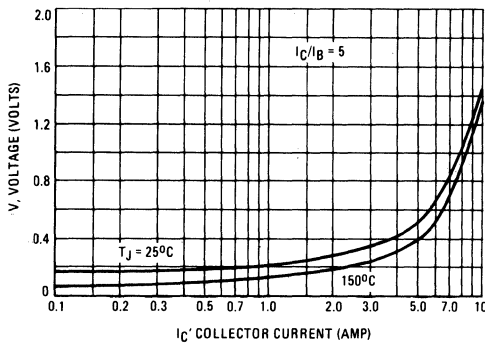
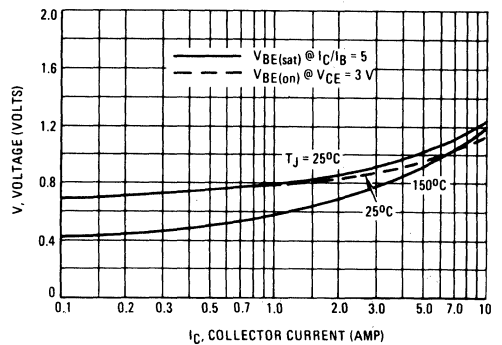


FIGURE 4 – BASE-EMITTER VOLTAGE



3

FIGURE 5 – COLLECTOR CUTOFF REGION

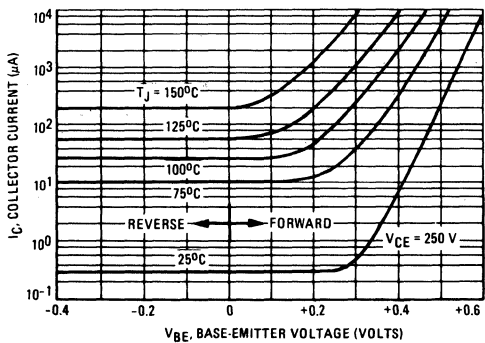


FIGURE 6 – CAPACITANCE

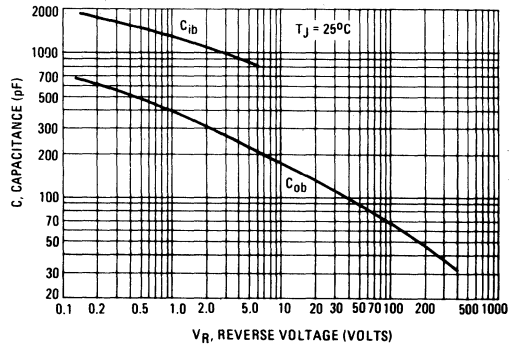


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

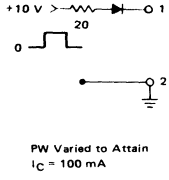
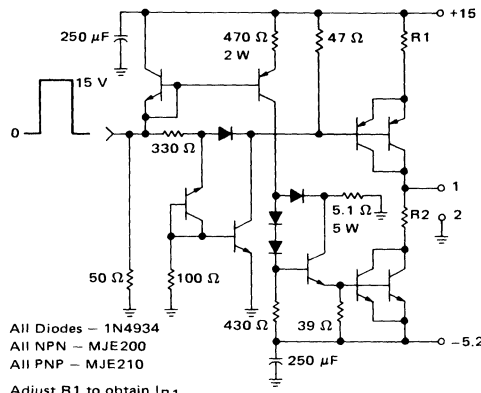
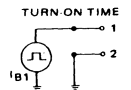
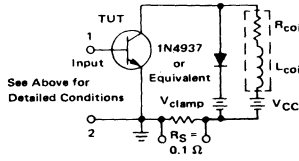
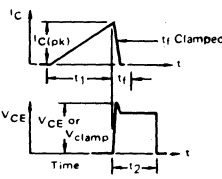
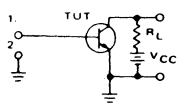
	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>	 <p>All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210</p> <p>Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For V_{CEO(sus)}, R2 = ∞</p>	 <p>TURN-ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}</p>	<p>V_{CC} = 250 V R_L = 50 Ω Pulse Width = 10 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope – Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

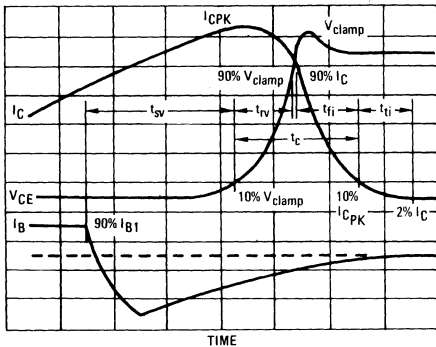
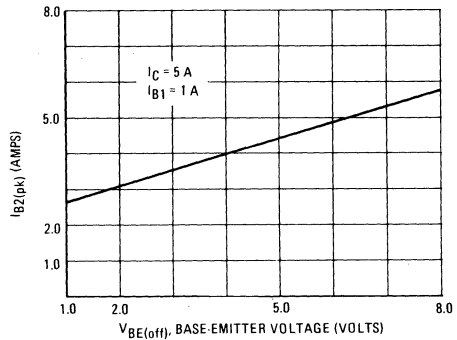


FIGURE 8 – PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_B to 10% V_{clamp}
 - t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
 - t_{fi} = Current Fall Time, 90–10% I_C
 - t_{ti} = Current Tail, 10–2% I_C
 - t_c = Crossover Time, 10% V_{clamp} to 10% I_C
- An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

FIGURE 9 – TURN-ON SWITCHING TIMES

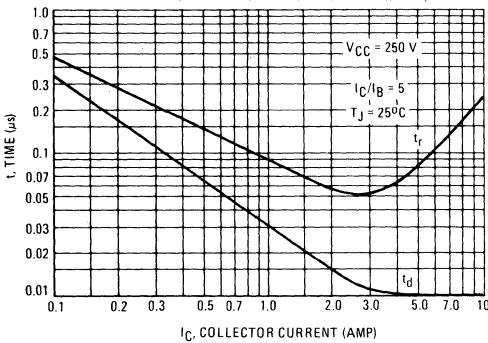


FIGURE 10 – TURN-OFF TIME

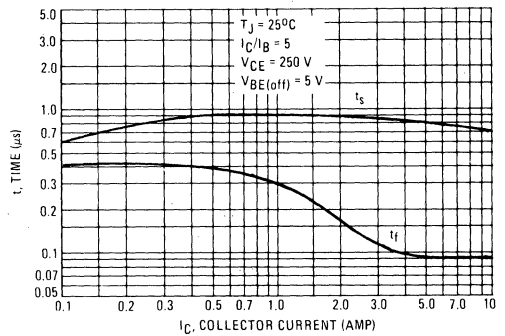
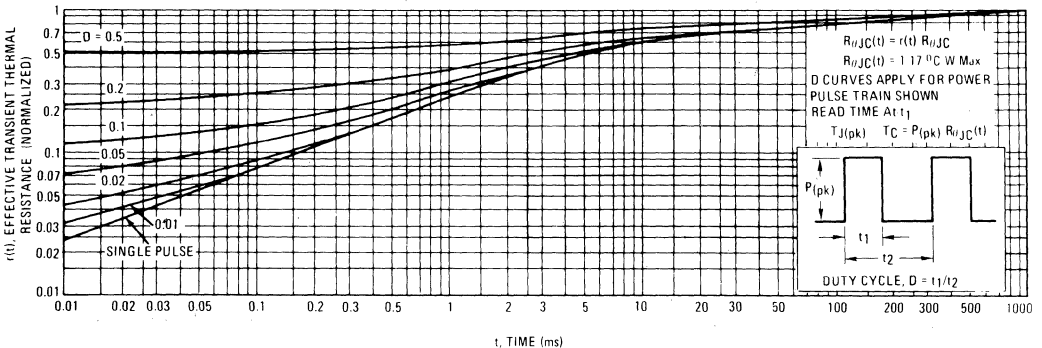


FIGURE 11 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

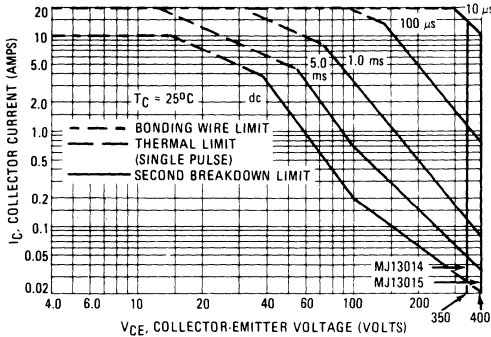


FIGURE 13 – REVERSE BIAS SWITCHING SAFE OPERATING AREA

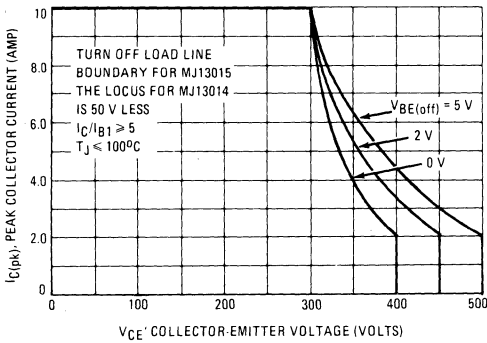
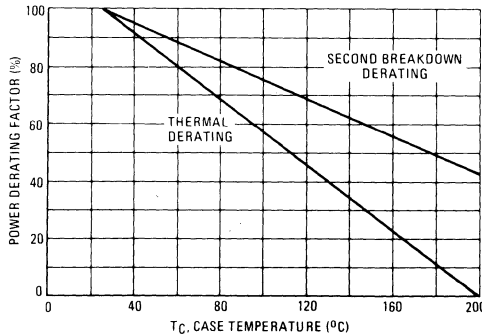


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

Designer's Data Sheet

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The MJ13070 and MJ13071 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

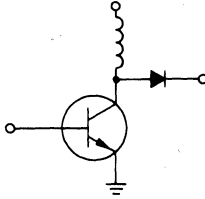
Fast Turn-Off Times

- 100 ns Inductive Fall Time @ 25°C (Typ)
- 150 ns Inductive Crossover Time @ 25°C (Typ)
- 400 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



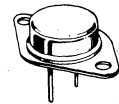
5 AMPERE

NPN SILICON
POWER TRANSISTORS

400 AND 450 VOLTS
125 WATTS

Designer's Data for
"Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



MAXIMUM RATINGS

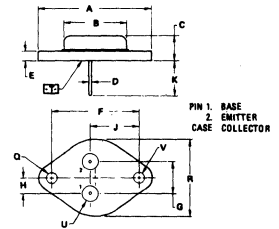
Rating	Symbol	MJ13070	MJ13071	Unit
Collector-Emitter Voltage	V _{CEO}	400	450	Vdc
Collector-Emitter Voltage	V _{CEV}	650	750	Vdc
Emitter Base Voltage	V _{EB}	6.0		Vdc
Collector Current — Continuous	I _C	5.0		Adc
— Peak (1)	I _{CM}	8.0		
Base Current — Continuous	I _B	2.0		Adc
— Peak (1)	I _{BM}	4.0		
Total Power Dissipation @ T _C = 25°C	P _D	125		Watts
Derate above 25°C @ T _C = 100°C		71.5		
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3



- NOTES:
 1. DIMENSIONS D AND V ARE DATUMS.
 2. \square IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Ø.
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

⊕ 0.13 (0.005) ⊖ T | V ⊕
 FOR LEADS:
 ⊕ 0.13 (0.005) ⊖ T | V ⊕ ⊕

MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX
A	-	29.37	-	1.150
B	-	21.08	-	0.830
C	0.35	7.62	0.250	0.300
D	0.97	1.99	0.038	0.073
E	1.40	1.78	0.055	0.070
F	30.15 BSC	-	1.187 BSC	-
G	15.92 BSC	-	0.626 BSC	-
H	5.46 BSC	-	0.215 BSC	-
J	16.85 BSC	-	0.663 BSC	-
K	11.18 12.15	0.440 0.480	-	-
L	3.81	4.19	0.150	0.165
M	-	26.87	-	1.060
N	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ13070 MJ13071 $V_{CE(sus)}$	400 450	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	— —	— —	0.5 2.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.0 3.0 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	250	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	($V_{CC} = 250\text{ Adc}$, $I_C = 3.0\text{ Adc}$, $I_{B1} = 0.4\text{ Adc}$, $t_p = 30\ \mu\text{s}$, Duty Cycle $\leq 2\%$, $V_{BE(off)} = 5.0\text{ Vdc}$)	t_d	—	0.03	0.05	μs
Rise Time		t_r	—	0.10	0.40	
Storage Time		t_s	—	0.40	1.50	
Fall Time		t_f	—	0.175	0.50	

Inductive Load, Clamped (Table 1)							
Storage Time	($I_{C(pk)} = 3.0\text{ A}$, $I_{B1} = 0.4\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 250\text{ V}$)	(T _J = 100°C)	t_{sv}	—	0.70	2.0	μs
Crossover Time			t_c	—	0.28	0.50	
Fall Time		t_{fi}	—	0.15	0.30		
Storage Time		(T _J = 25°C)	t_{sv}	—	0.40	—	
Crossover Time			t_c	—	0.15	—	
Fall Time			t_{fi}	—	0.10	—	

(1) Pulse Test: PW - 300 μs . Duty Cycle $\leq 2\%$.

$$\beta_f = \frac{I_C}{I_B}$$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

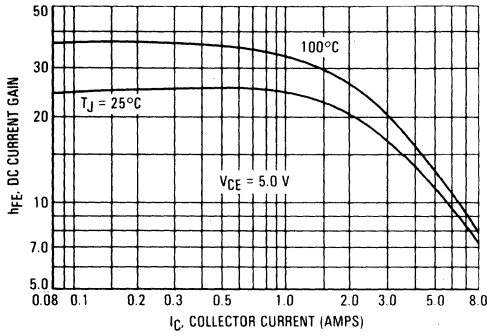


FIGURE 2 — COLLECTOR SATURATION REGION

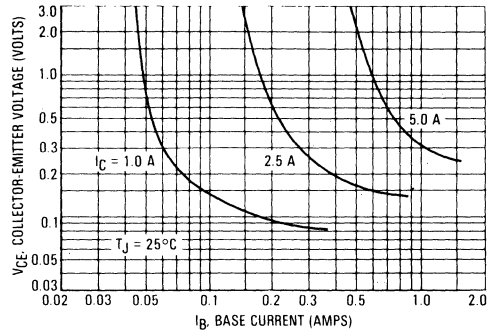


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

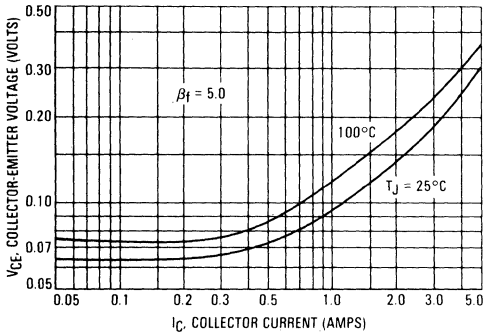


FIGURE 4 — BASE-EMITTER VOLTAGE

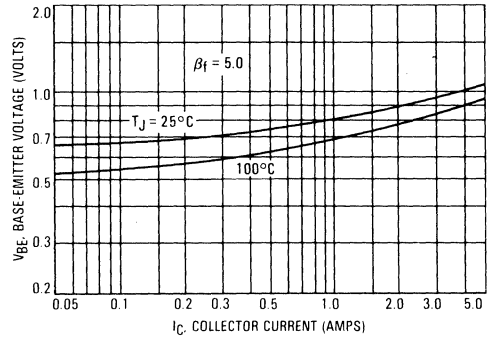


FIGURE 5 — COLLECTOR CUTOFF REGION

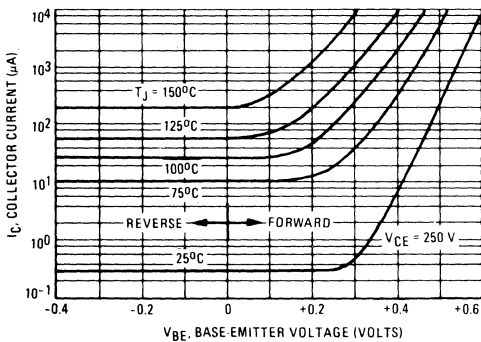


FIGURE 6 — CAPACITANCE

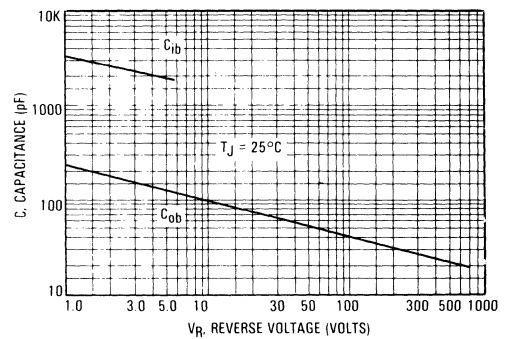


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

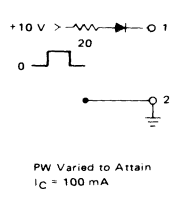
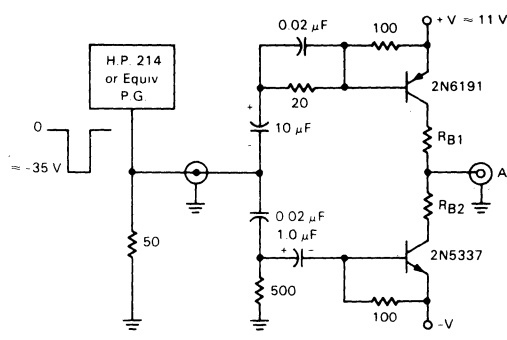
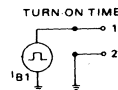
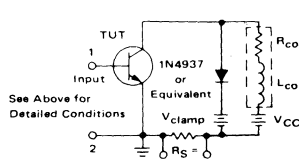
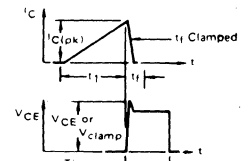
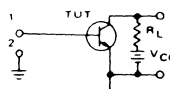
	$V_{CE0(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
<p>INPUT CONDITIONS</p>  <p>PW Varied to Attain $I_C = 100$ mA</p>		 <p>Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For $V_{CE0(sus)}$, R2 = ∞</p>	<p>TURN ON TIME</p>  <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
<p>CIRCUIT VALUES</p> <p>$L_{coil} = 80$ mH $V_{CC} = 10$ V $R_{coil} = 0.7$ Ω</p>		<p>$L_{coil} = 180$ μH $R_{coil} = 0.05$ Ω $V_{CC} = 20$ V</p> <p>$V_{clamp} = 250$ V R_B adjusted to attain desired I_{B1}</p>	<p>$V_{CC} = 250$ V $R_L = 83$ Ω Pulse Width = 10 μs</p>
<p>TEST CIRCUITS</p>	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope – Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 



FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

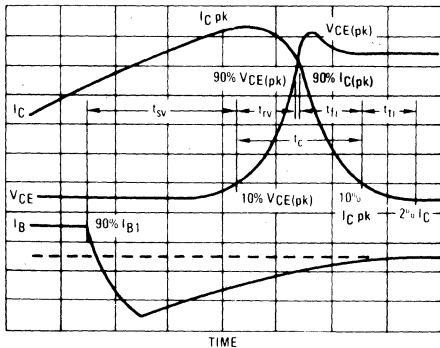
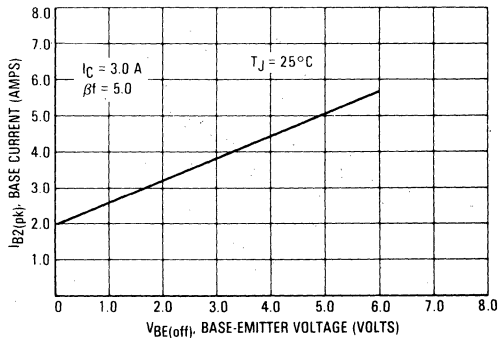


FIGURE 8 – PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
 - t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
 - t_{fi} = Current Fall Time, 90–10% I_C
 - t_{ti} = Current Tail, 10–2% I_C
 - t_c = Crossover Time, 10% V_{clamp} to 10% I_C
- An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

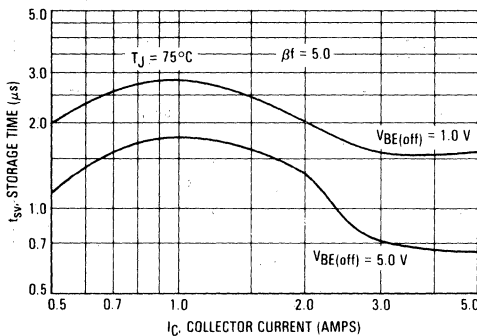


FIGURE 10 — CROSSOVER AND FALL TIMES

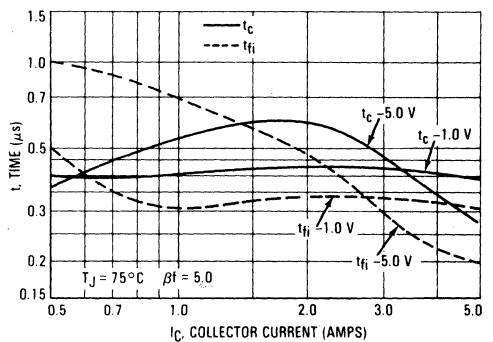
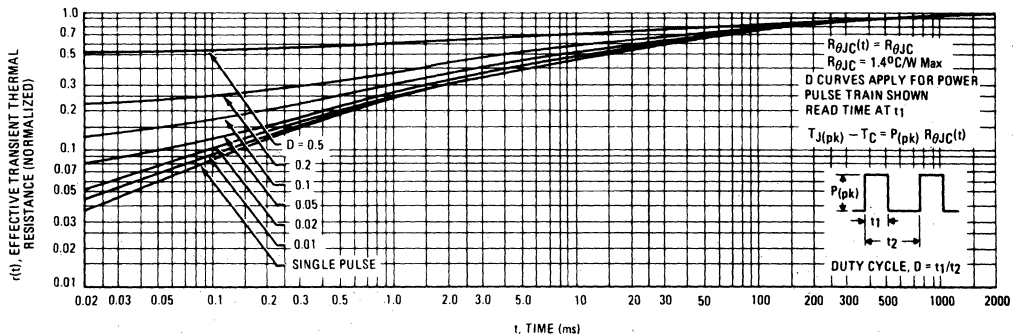


FIGURE 11 — THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

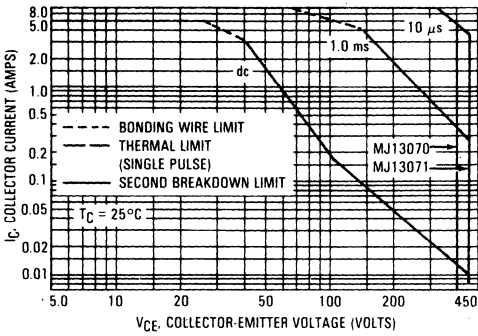


FIGURE 13 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

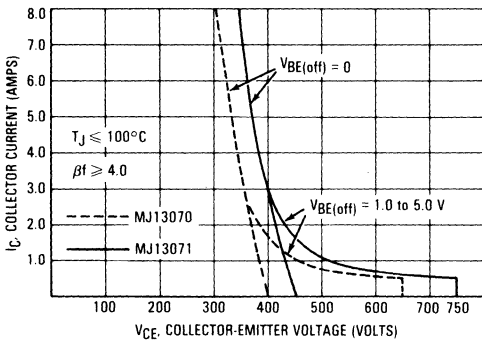
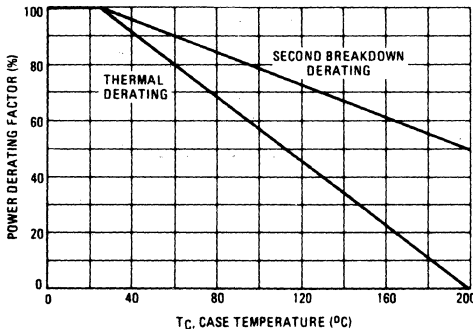


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

Designer's Data Sheet

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The MJ13080 and MJ13081 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

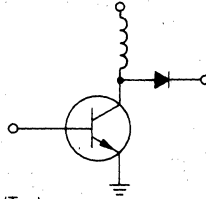
Fast Turn-Off Times

- 100 ns Inductive Fall Time @ 25°C (Typ)
- 150 ns Inductive Crossover Time @ 25°C (Typ)
- 400 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



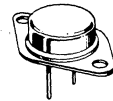
8 AMPERE

NPN SILICON
POWER TRANSISTORS

400 AND 450 VOLTS
150 WATTS

Designer's Data for
"Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



MAXIMUM RATINGS

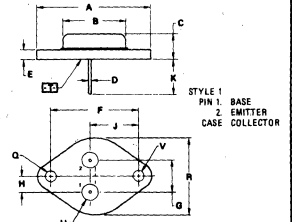
Rating	Symbol	MJ13080	MJ13081	Unit
Collector-Emitter Voltage	V _{CEO}	400	450	Vdc
Collector-Emitter Voltage	V _{CEV}	650	750	Vdc
Emitter Base Voltage	V _{EB}		6.0	Vdc
Collector Current — Continuous	I _C		8.0	Adc
— Peak (1)	I _{CM}		12	
Base Current — Continuous	I _B		3.0	Adc
— Peak (1)	I _{BM}		6.0	
Total Power Dissipation @ T _C = 25°C	P _D	150		Watts
@ T _C = 100°C		85.5		
Derate above 25°C		0.86		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3



- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. [] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q.

FOR LEADS:
 ⌀ .13 (0.005) T | v ⊕
 ⌀ .13 (0.005) T | v ⊕ ⊕

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1975.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.37	1.550		
B	21.98	0.850		
C	6.35	0.250	0.250	0.300
D	0.97	0.038	0.043	
E	1.40	0.055	0.010	
F	30.15 BSC	1.181 BSC		
G	10.52 BSC	0.410 BSC		
H	5.40 BSC	0.215 BSC		
J	16.25 BSC	0.645 BSC		
K	11.18	0.440	0.440	0.480
L	3.81	0.150	0.165	
M	26.67	1.050		
N	4.83	0.190	0.210	
V	3.81	0.150	0.165	

CASE 1-05
TO-204AA

MJ13080, MJ13081

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0)	MJ13080 MJ13081 V _{CEO(sus)}	400 450	— —	— —	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	— —	— —	0.5 2.5	mAdc
Collector Cutoff Current (V _{CE} = Rated V _{CEV} , R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V _{EB} = 6.0 Vdc, I _C = 0)	I _{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figure 12		
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13		

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 5.0 Adc, V _{CE} = 3.0 Vdc)	h _{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage (I _C = 5.0 Adc, I _B = 1.0 Adc) (I _C = 8.0 Adc, I _B = 1.6 Adc) (I _C = 5.0 Adc, I _B = 1.0 Adc, T _C = 100°C)	V _{CE(sat)}	— — —	— — —	1.0 3.0 2.0	Vdc
Base-Emitter Saturation Voltage (I _C = 5.0 Adc, I _B = 1.0 Adc) (I _C = 5.0 Adc, I _B = 1.0 Adc, T _C = 100°C)	V _{BE(sat)}	— —	— —	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1.0 kHz)	C _{ob}	—	—	300	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 250 Vdc, I _C = 5.0 Adc, I _{B1} = 0.7 Adc, t _p = 30 μs, Duty Cycle ≤ 2%, V _{BE(off)} = 5.0 Vdc)	t _d	—	0.025	0.05	μs
Rise Time		t _r	—	0.10	0.50	
Storage Time		t _s	—	0.50	1.50	
Fall Time		t _f	—	0.15	0.50	

Inductive Load, Clamped (Table 1)							
Storage Time	(I _{C(pk)} = 5.0 A, I _{B1} = 0.7 Adc, V _{BE(off)} = 5.0 Vdc, V _{CE(pk)} = 250 V)	(T _J = 100°C)	t _{sv}	—	0.75	2.20	μs
Crossover Time			t _c	—	0.22	0.40	
Fall Time		t _{fi}	—	0.175	0.35		
Storage Time		(T _J = 25°C)	t _{sv}	—	0.40	—	
Crossover Time			t _c	—	0.15	—	
Fall Time			t _{fi}	—	0.10	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

$$\beta_f = \frac{I_C}{I_B}$$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

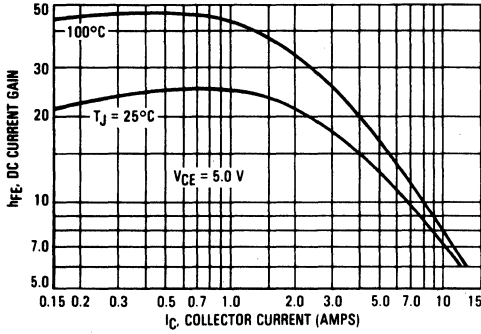


FIGURE 2 — COLLECTOR SATURATION REGION

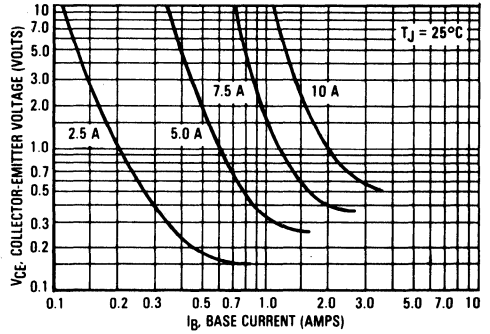


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

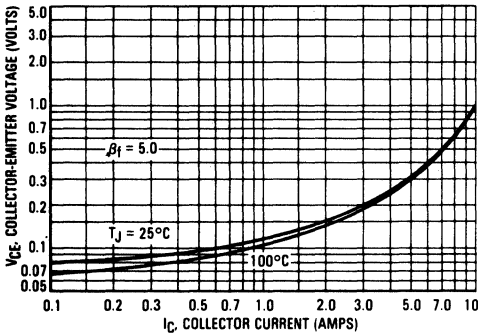


FIGURE 4 — BASE-EMITTER VOLTAGE

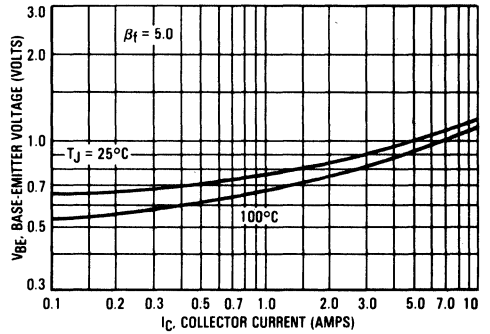


FIGURE 5 — COLLECTOR CUTOFF REGION

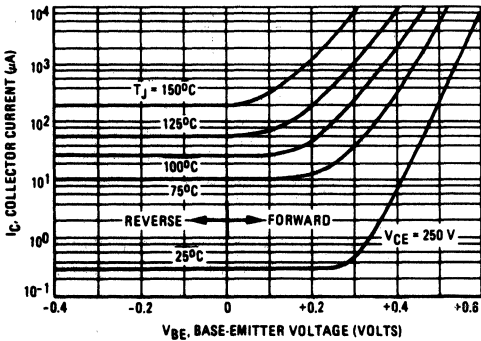


FIGURE 6 — CAPACITANCE

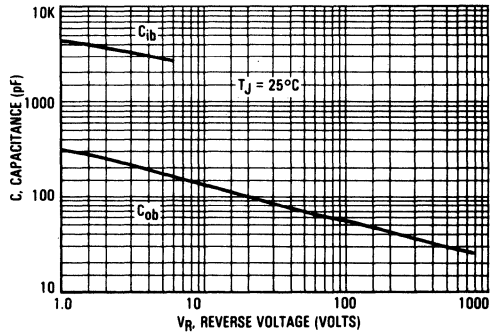
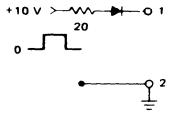
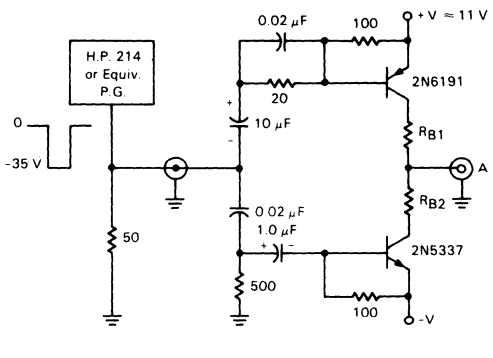
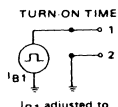
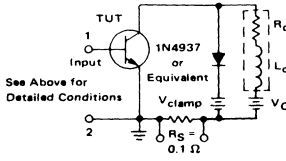
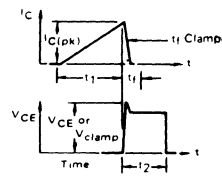
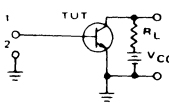


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

INPUT CONDITIONS	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
 <p>PW Varied to Attain I_C = 100 mA</p>	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	 <p>Adjust R1 to obtain I_{B1} For switching and R_{BSOA}. R2 = 0 For V_{CEO(sus)}. R2 = ∞</p> <p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced hFE desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment: Scope – Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 	

3

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

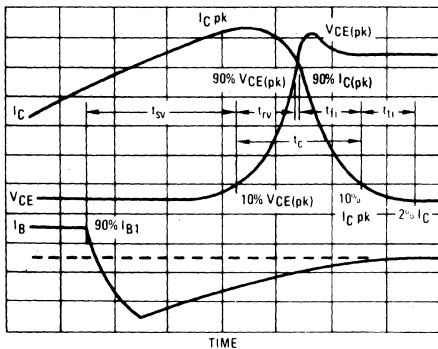
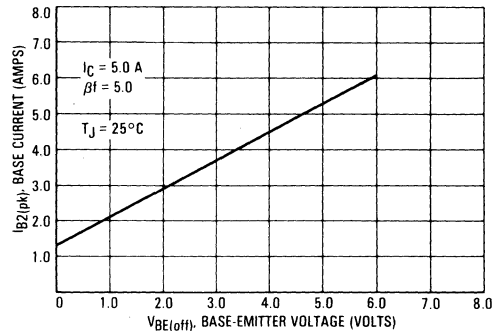


FIGURE 8 – PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

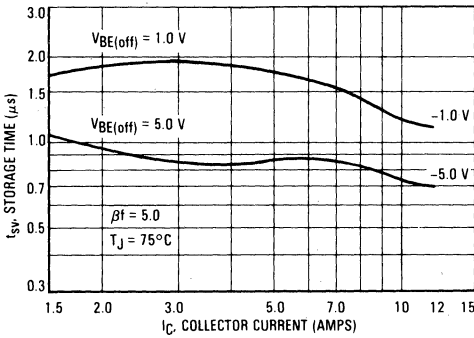


FIGURE 10 — CROSSOVER AND FALL TIMES

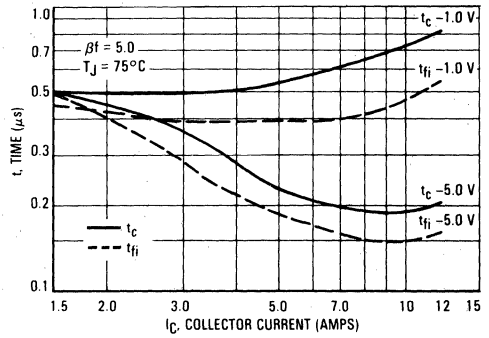
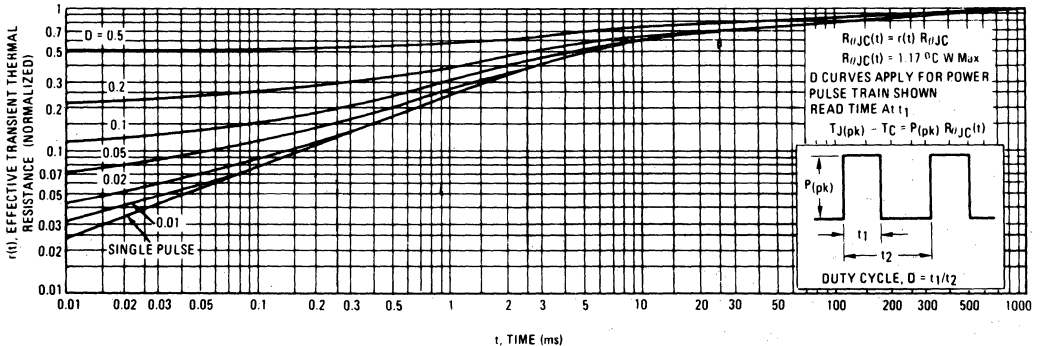


FIGURE 11 — THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

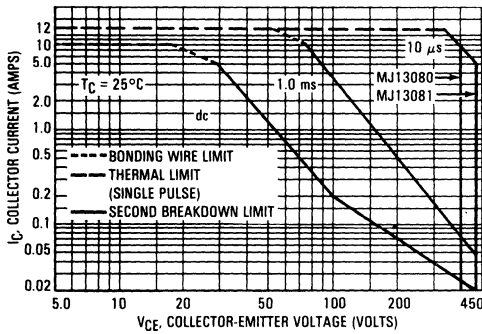


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

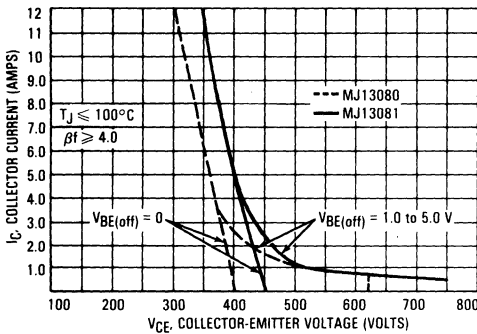
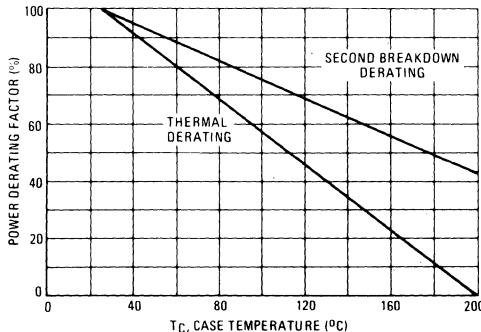


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

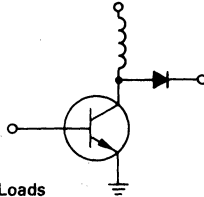
Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

100°C Performance Specified for:
 Reverse-Biased SOA with Inductive Loads
 Switching Times with Inductive Loads —
 150 ns Inductive Fall Time (Typ)
 Saturation Voltages
 Leakage Currents



MAXIMUM RATINGS

Rating	Symbol	MJ13090	MJ13091	MJH13090	MJH13091	Unit
Collector-Emitter Voltage	V _{CEO(sus)}	400	450	400	450	Vdc
Collector-Emitter Voltage	V _{CEV}	650	750	650	750	Vdc
Emitter-Base Voltage	V _{EB}	6.0				Vdc
Collector Current						Adc
— Continuous	I _C	15				
— Peak (1)	I _{CM}	20				
Base Current						Adc
— Continuous	I _B	5.0				
— Peak (1)	I _{BM}	10				
Total Device Dissipation	P _D					Watts
@ T _C = 25°C		175		125		
@ T _C = 100°C		100		50		
Derate above 25°C		1.0		1.0		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to 200		-55 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.0	°C/W
Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds.	T _L	275	°C

(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.

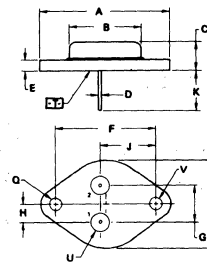
Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

15 AMPERE

NPN SILICON
POWER
TRANSISTORS

400 AND 450 VOLTS
125 and 175 WATTS



MJ13090
MJ13091

STYLE 1
 PIN 1. BASE
 PIN 2. EMITTER
 CASE. COLLECTOR

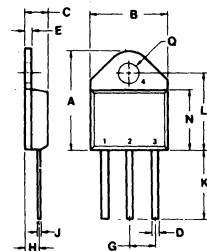
NOTES:

1. DIMENSIONS D AND V ARE DATUMS.
2. □ IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE: $\phi \pm 0.13 (0.005) \text{ (M) T V } \text{ (M)}$
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS			INCHES		
	MIN	MAX	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550	—	—
B	—	27.08	—	1.066	—	—
C	6.35	7.62	0.250	0.300	—	—
D	0.57	1.08	0.028	0.043	—	—
E	1.40	1.78	0.055	0.070	—	—
F	30.15 BSC	—	1.187 BSC	—	—	—
G	10.92 BSC	—	0.430 BSC	—	—	—
H	5.46 BSC	—	0.215 BSC	—	—	—
J	16.88 BSC	—	0.665 BSC	—	—	—
K	11.18	12.19	0.441	0.480	—	—
L	3.81	4.19	0.151	0.165	—	—
M	—	26.67	—	1.050	—	—
U	4.83	5.33	0.190	0.210	—	—
V	3.81	4.19	0.151	0.165	—	—

CASE 1-05
TO-204AA

MJH13090
MJH13091



1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

DIM	MILLIMETERS			INCHES		
	MIN	MAX	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830	—	—
B	15.49	15.90	0.610	0.628	—	—
C	4.19	5.08	0.165	0.200	—	—
D	1.02	1.65	0.040	0.065	—	—
E	1.35	1.65	0.053	0.065	—	—
G	5.21	5.72	0.206	0.225	—	—
H	2.41	3.20	0.095	0.126	—	—
J	0.38	0.64	0.015	0.025	—	—
K	12.70	15.49	0.500	0.610	—	—
L	15.88	16.51	0.625	0.650	—	—
N	12.19	12.70	0.480	0.500	—	—
O	4.04	4.22	0.159	0.166	—	—

CASE 340-01
TO-218AC

MJ13090, MJ13091, MJH13090, MJH13091

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0) MJ13090, MJH13090 MJ13091, MJH13091	V _{CEO(sus)}	400 450	— —	— —	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	—	—	0.5 2.5	mAdc
Collector Cutoff Current (V _{CE} = Rated V _{CEV} , R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V _{EB} = 6.0 Vdc, I _C = 0)	I _{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figures 12 and 13		
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 14		

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 10 Adc, V _{CE} = 3.0 Vdc)	h _{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage (I _C = 10 Adc, I _B = 2.0 Adc) (I _C = 15 Adc, I _B = 3.0 Adc) (I _C = 10 Adc, I _B = 2.0 Adc, T _C = 100°C)	V _{CE(sat)}	—	—	1.0 3.0 2.0	Vdc
Base-Emitter Saturation Voltage (I _C = 10 Adc, I _B = 2.0 Adc) (I _C = 10 Adc, I _B = 2.0 Adc, T _C = 100°C)	V _{BE(sat)}	—	—	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1.0 kHz)	C _{ob}	—	—	350	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	(V _{CC} = 250 Vdc, I _C = 10 Adc, I _{B1} = 1.25 Adc, t _p = 30 μs, Duty Cycle ≤ 2%, V _{BE(off)} = 5.0 Vdc)	t _d	—	0.03	0.05	μs	
Rise Time		t _r	—	0.13	0.50		
Storage Time		t _s	—	0.55	2.50		
Fall Time		t _f	—	0.10	0.50		
Inductive Load, Clamped (Table 1)							
Storage Time	(I _{C(pk)} = 10 A, I _{B1} = 1.25 Adc, V _{BE(off)} = 5.0 Vdc, V _{CE(pk)} = 250 V)	(T _J = 100°C)	t _{sv}	—	0.80	3.00	μs
Crossover Time			t _c	—	0.175	0.40	
Fall Time		t _{fi}	—	0.15	0.30		
Storage Time		(T _J = 25°C)	t _{sv}	—	0.50	—	
Crossover Time			t _c	—	0.15	—	
Fall Time			t _{fi}	—	0.10	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

$$*\beta_f = \frac{I_C}{I_B}$$

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

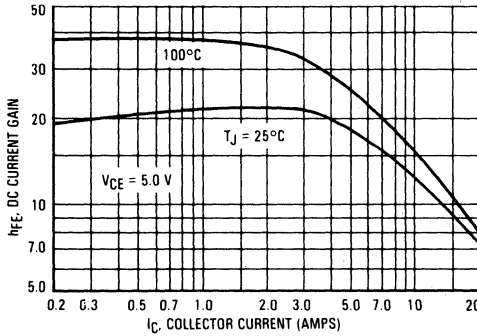


FIGURE 2 — COLLECTOR SATURATION REGION

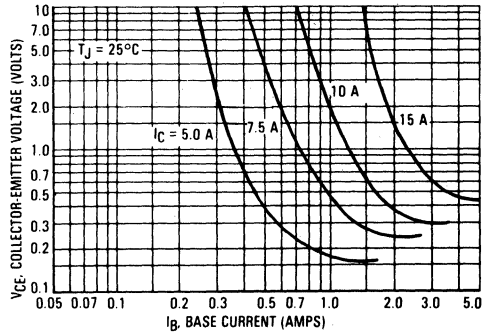


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

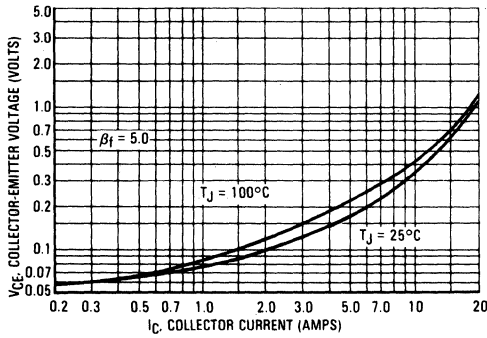


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

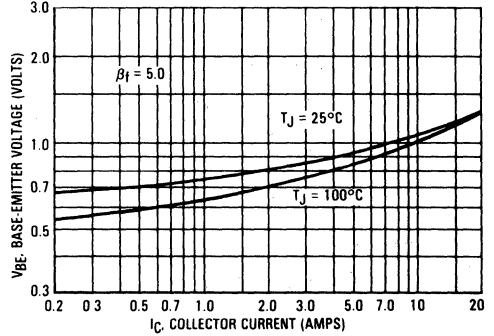


FIGURE 5 — COLLECTOR CUTOFF REGION

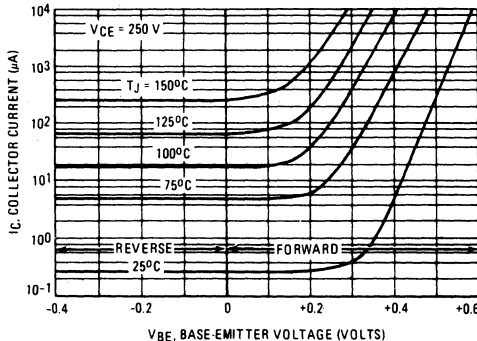
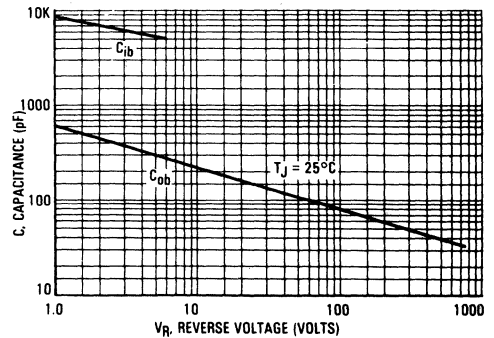
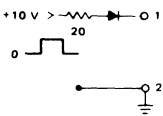
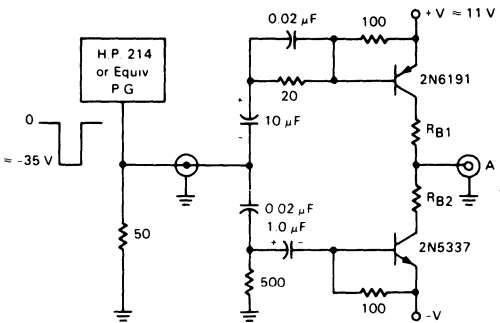
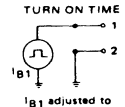
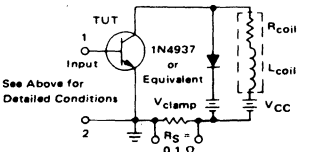
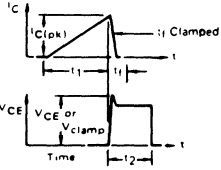
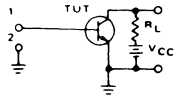


FIGURE 6 — CAPACITANCE



MJ13090, MJ13091, MJH13090, MJH13091

TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>	 <p>Connect Point A to base of TUT Adjust -V to obtain desired V_{BE(off)} at Point A Adjust R1 to obtain I_{B1} For switching and R_{BSOA}, R2 = 0 For V_{CEO(sus)} R2 = ∞</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>V_{clamp} = 250 V R_{B1} adjusted to attain desired I_{B1}</p>	<p>V_{CC} = 250 V R_L = 25 Ω Pulse Width = 30 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

3

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

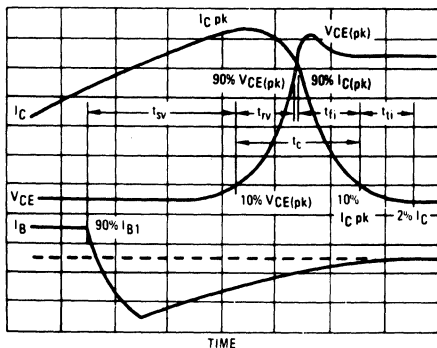
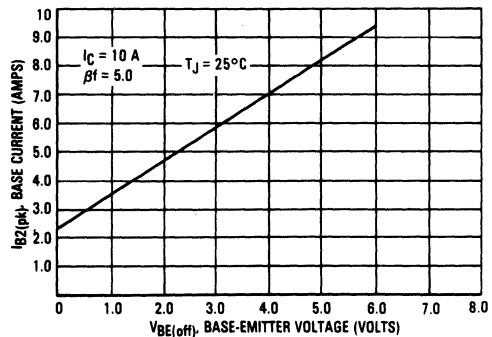


FIGURE 8 - PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10—90% V_{clamp}
- t_{fi} = Current Fall Time, 90—10% I_C
- t_{ti} = Current Tail, 10—2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

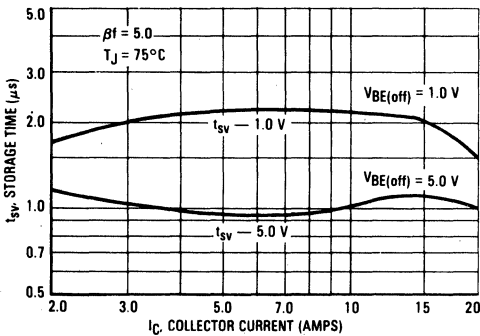


FIGURE 10 — CROSSOVER AND FALL TIMES

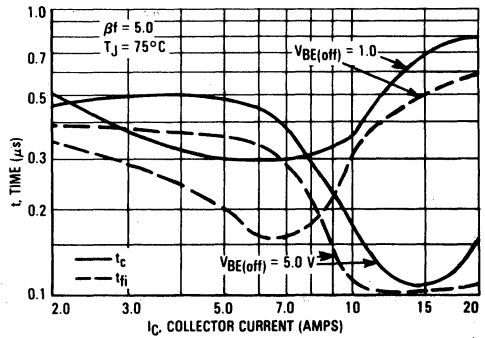
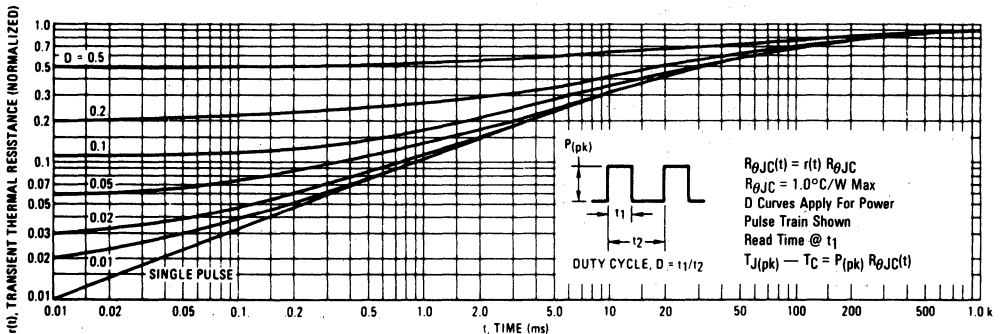


FIGURE 11 — THERMAL RESPONSE

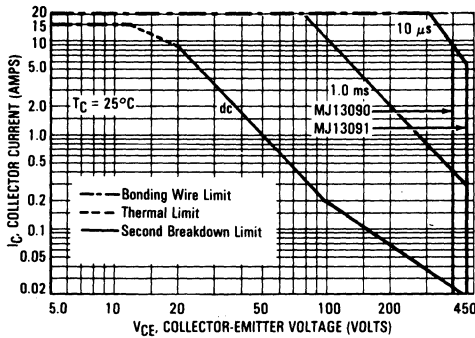


3

MJ13090, MJ13091, MJH13090, MJH13091

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

**FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA
MJ13090 and MJ13091**



**FIGURE 13 — FORWARD BIAS SAFE OPERATING AREA
MJH13090 and MJH13091**

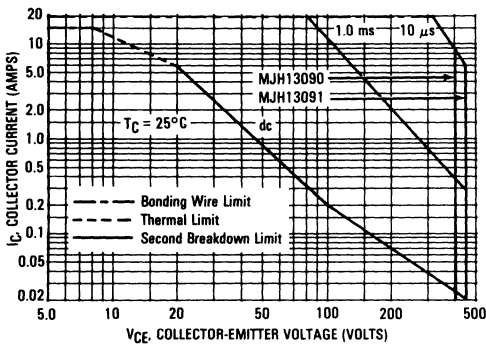
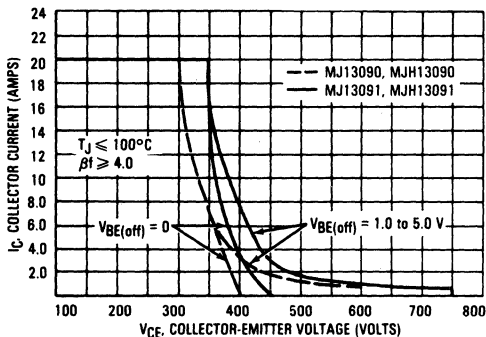


FIGURE 14 — REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

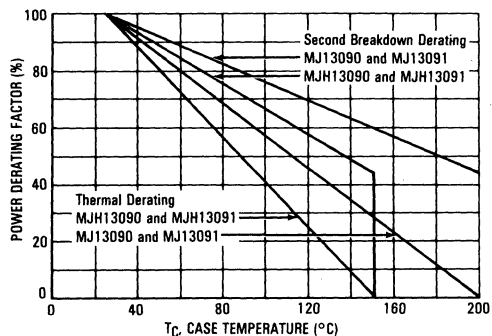
The data of Figures 12 and 13 are based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 12 and 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives RBSOA characteristics.

FIGURE 15 — POWER DERATING



Designer's Data Sheet

**SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTOR**

The MJ13101 transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

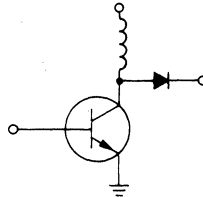
Fast Turn-Off Times

- 30 ns Inductive Fall Time @ 25°C (Typ)
- 50 ns Inductive Crossover Time @ 25°C (Typ)
- 900 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



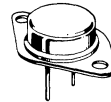
20 AMPERE

**NPN SILICON
POWER TRANSISTOR**

**450 VOLTS
175 WATTS**

**Designer's Data for
"Worst Case" Conditions**

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



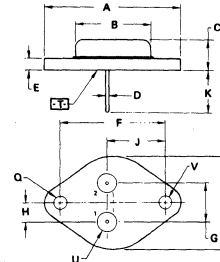
MAXIMUM RATINGS

Rating	Symbol	MJ13101	Unit
Collector-Emitter Voltage	V_{CEO}	450	Vdc
Collector-Emitter Voltage	V_{CEV}	750	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	20	Adc
— Peak (1)	I_{CM}	30	
Base Current — Continuous	I_B	10	Adc
— Peak (1)	I_{BM}	15	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175	Watts
Derate above 25°C @ $T_C = 100^\circ\text{C}$		1.0	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. □ IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
 FOR LEADS: $\pm 0.13 (0.005) \text{ T } \text{V } \text{O}$
 FOR CASE: $\pm 0.13 (0.005) \text{ T } \text{V } \text{O } \text{O}$
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

DIM	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.60	—	0.850
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.45 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.18	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.18	0.150	0.165

**CASE 1-05
TO-204AA**

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.5 2.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 15\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$)	h_{FE}	8.0	—	40	—
Collector-Emitter Saturation Voltage ($I_C = 15\text{ Adc}$, $I_B = 3.0\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 4.0\text{ Adc}$) ($I_C = 15\text{ Adc}$, $I_B = 3.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	1.0 3.0 2.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 15\text{ Adc}$, $I_B = 3.0\text{ Adc}$) ($I_C = 15\text{ Adc}$, $I_B = 3.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	450	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$V_{CC} = 250\text{ Vdc}$, $I_C = 15\text{ Adc}$, $I_{B1} = 2.0\text{ Adc}$, $t_p = 30\ \mu\text{s}$, Duty Cycle $\leq 2\%$, $V_{BE(off)} = 5.0\text{ Vdc}$	t_d	—	0.02	0.05	μs
Rise Time		t_r	—	0.13	0.50	
Storage Time		t_s	—	0.90	3.5	
Fall Time		t_f	—	0.10	0.50	

Inductive Load, Clamped (Table 1)							
Storage Time	$I_{C(pk)} = 15\text{ A}$, $I_{B1} = 2.0\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 250\text{ V}$	$(T_J = 100^\circ\text{C})$	t_{sv}	—	1.25	4.0	μs
Crossover Time			t_c	—	0.15	0.50	
Fall Time			t_{fi}	—	0.13	0.40	
Storage Time		$(T_J = 25^\circ\text{C})$	t_{sv}	—	0.90	—	
Crossover Time			t_c	—	0.05	—	
Fall Time			t_{fi}	—	0.03	—	

(1) Pulse Test: PW - 300 μs , Duty Cycle $\leq 2\%$.

* $\beta_f = \frac{I_C}{I_B}$



DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

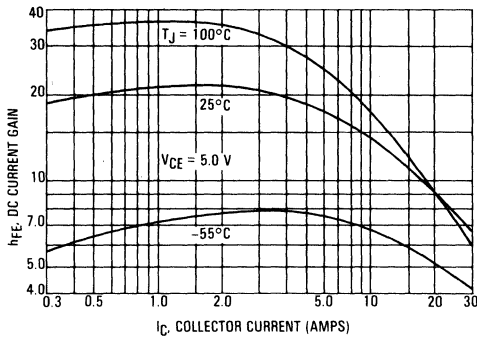


FIGURE 2 — COLLECTOR SATURATION REGION

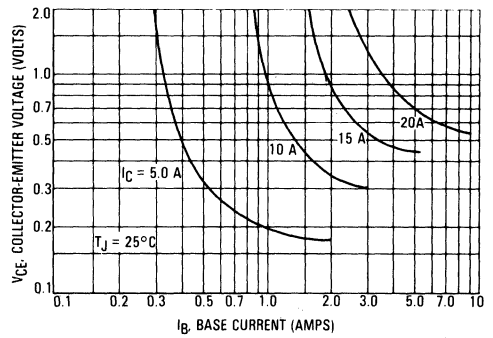


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

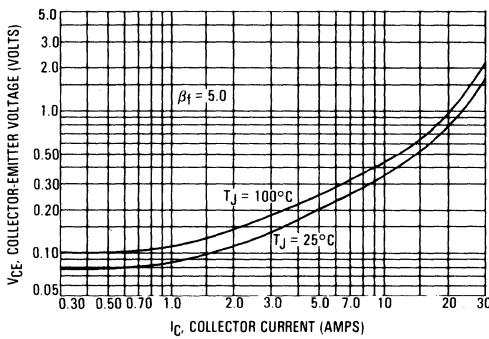


FIGURE 4 — BASE-EMITTER VOLTAGE

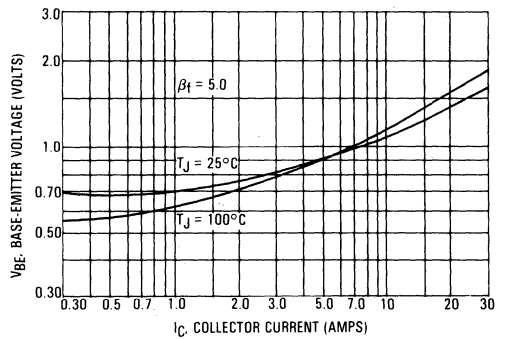


FIGURE 5 — COLLECTOR CUTOFF REGION

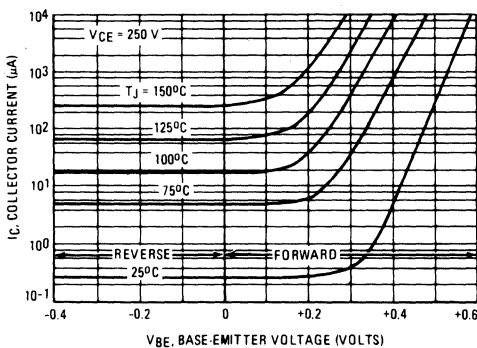
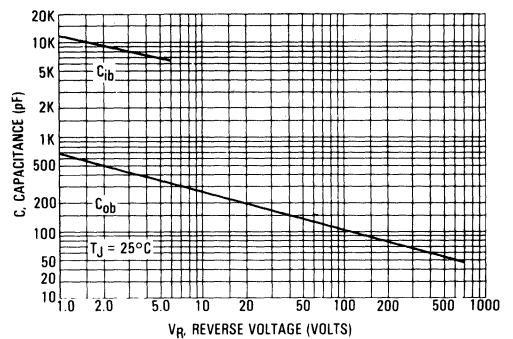


FIGURE 6 — CAPACITANCE



3

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

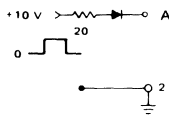
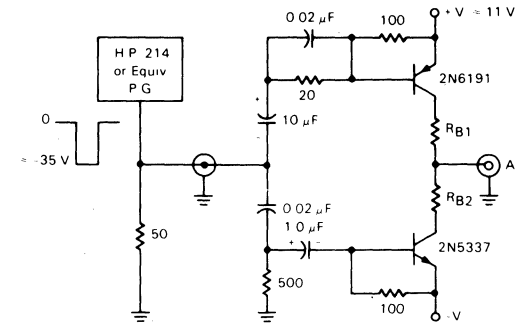
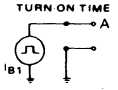
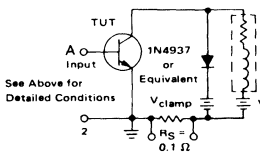
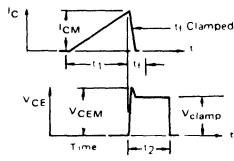
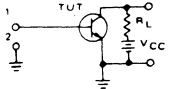
	V _{CE0} (sus)	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>	 <p>Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For V_{CE0}(sus), R2 = ∞</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_FE desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	L _{coil} = 80 mH V _{CC} = 10 V R _{coil} = 0.7 Ω	L _{coil} = 180 μH R _{coil} = 0.05 Ω V _{CC} = 20 V V _{clamp} = 250 V R _B adjusted to attain desired I _{B1}	V _{CC} = 250 V R _L = 16.6 Ω Pulse Width = 30 μs
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C t₁ ≈ $\frac{L_{coil} (I_{CM})}{V_{CC}}$ t₂ ≈ $\frac{L_{coil} (I_{CM})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 



FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

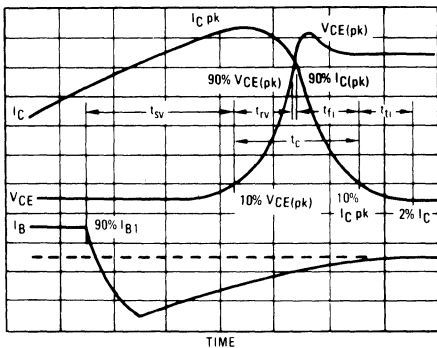
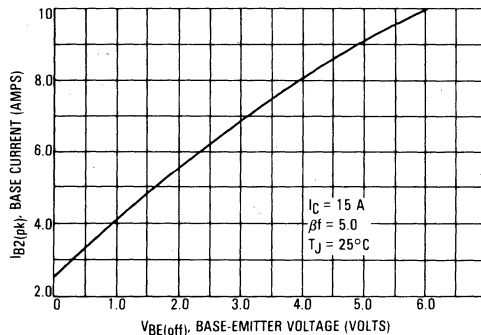


FIGURE 8 – PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
 - t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
 - t_{fi} = Current Fall Time, 90–10% I_C
 - t_{ti} = Current Tail, 10–2% I_C
 - t_c = Crossover Time, 10% V_{clamp} to 10% I_C
- An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

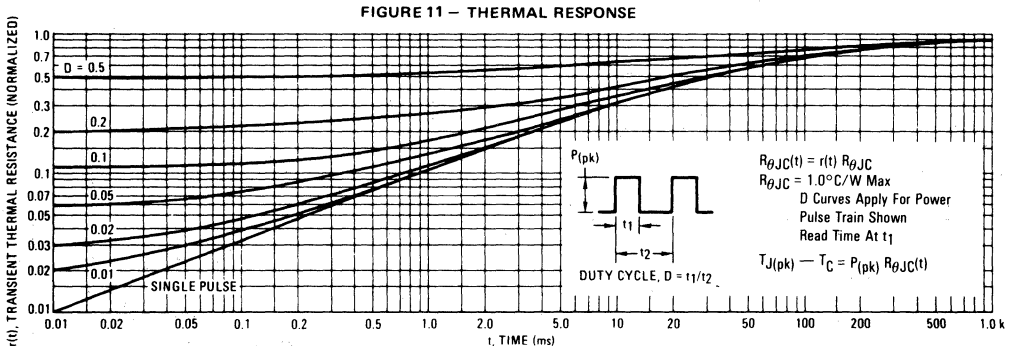
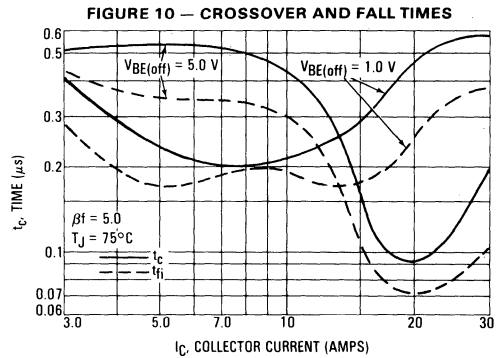
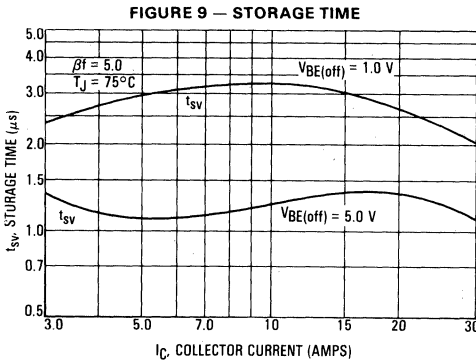
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING



3

The Safe Operating Area figures shown in figure 12 and 13 are specified for these devices under the test conditions shown

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA

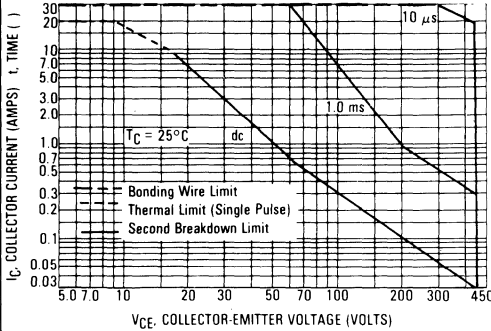


FIGURE 13 — REVERSE BIAS SAFE OPERATING AREA

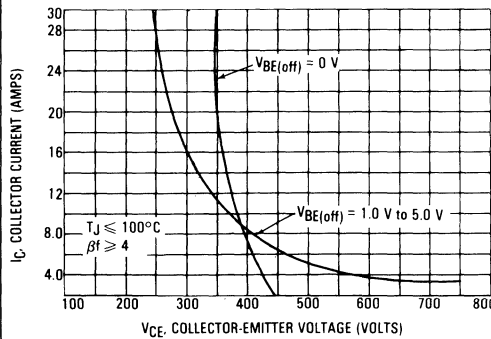
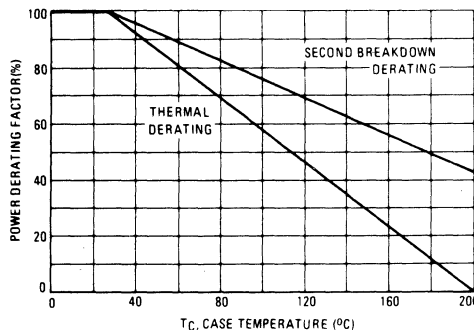


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate IC—VCE limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on Tc = 25°C; Tj(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when Tc ≥ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14

Tj(pk) may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ13330 and MJ13331 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

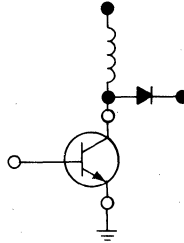
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Time

- 75 ns Inductive Fall Time—25°C (Typ)
- 150 ns Inductive Crossover Time—25°C (Typ)
- 900 ns Inductive Storage Time—25°C (Typ)
- Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



MAXIMUM RATINGS

Rating	Symbol	MJ13330	MJ13331	Unit
Collector-Emitter Voltage	V _{CEO}	200	250	V _{dc}
Collector-Emitter Voltage	V _{CEV}	400	450	V _{dc}
Emitter Base Voltage	V _{EB}	6		V _{dc}
Collector Current - Continuous	I _C	20		A _{dc}
Collector Current - Peak (1)	I _{CM}	30		A _{dc}
Base Current - Continuous	I _B	10		A _{dc}
Base Current - Peak (1)	I _{BM}	20		A _{dc}
Total Power Dissipation @ T _C = 25°C	P _D	175		Watts
@ T _C = 100°C		100		
Derate above 25°C		1		W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

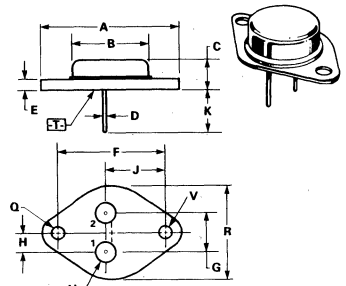
20 AMPERE

NPN SILICON
POWER TRANSISTORS

200 and 250 VOLTS
175 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



NOTES:

1. DIMENSIONS Q AND V ARE DATUMS.
2. \overline{T} IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
 $\pm 0.13 (0.005) \text{ (M) T | V } \text{ (M)}$

FOR LEADS:

1. $\pm 0.13 (0.005) \text{ (M) T | V } \text{ (M) Q } \text{ (M)}$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1:

1. BASE
2. EMITTER
- CASE COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA

Similar device types with higher V_{CEO} ratings are: MJ13332 (350 V) thru MJ13335 (500 V).

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE0(sus)}$	200 250	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	—	—	0.25 5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5	mAdc
Emitter Cutoff Current ($V_{EB} = 6\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	0.5	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 13			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 5\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	15 8.0	—	75 40	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.5\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 5\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.8\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	1.5 3.5 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.5\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.8\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.8 1.8	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 300\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1\text{ MHz}$)	f_T	5	—	40	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 100\text{ kHz}$)	C_{ob}	100	—	400	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$(V_{CC} = 175\text{ Vdc}$, $I_C = 10\text{ A}$, $I_{B1} = 1.5\text{ Adc}$, $V_{BE(off)} = 5\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2\%$)	t_d	—	0.08	0.20	μs
Rise Time		t_r	—	0.55	1.0	μs
Storage Time		t_s	—	0.70	3.5	μs
Fall Time		t_f	—	0.11	0.7	μs
Inductive Load, Clamped (Table 1)						
Storage Time	$(I_C = 10\text{ A(pk)}$, $V_{clamp} = 200\text{ Vdc}$, $I_{B1} = 1.8\text{ Adc}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	1.35	4.5	μs
Crossover Time		t_c	—	0.45	1.8	μs
Storage Time	$(I_C = 10\text{ A(pk)}$, $V_{clamp} = 200\text{ Vdc}$, $I_{B1} = 1.5\text{ Adc}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_{sv}	—	0.90	—	μs
Crossover Time		t_c	—	0.15	—	μs
Fall Time		t_{fi}	—	0.075	—	μs

(1) Pulse Test: PW = 300 μs , Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

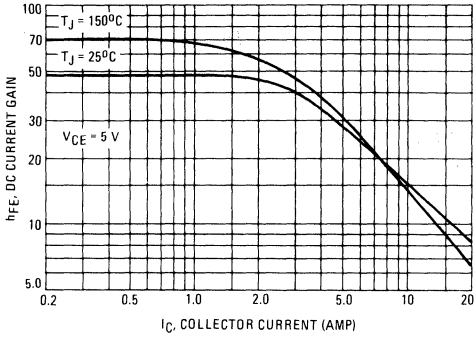


FIGURE 2 – COLLECTOR SATURATION REGION

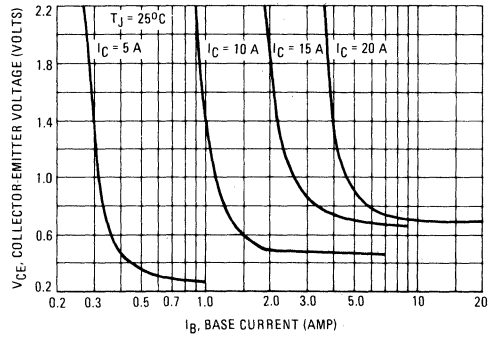


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

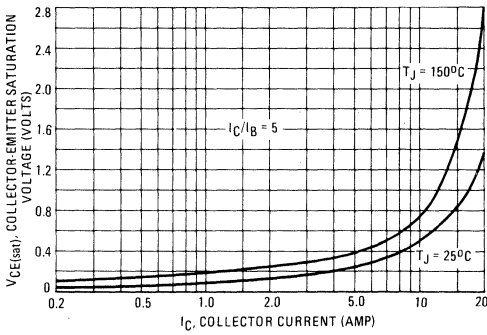
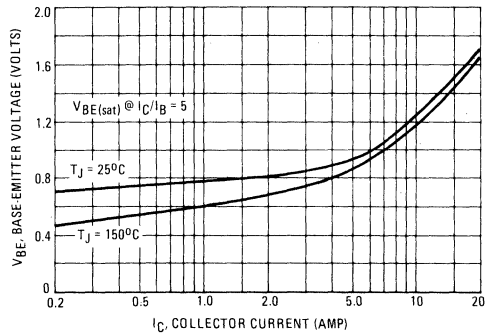


FIGURE 4 – BASE-EMITTER VOLTAGE



3

FIGURE 5 – COLLECTOR CUTOFF REGION

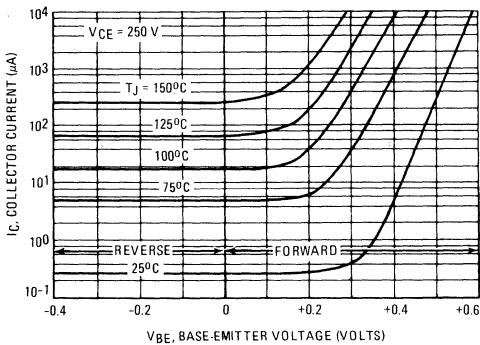
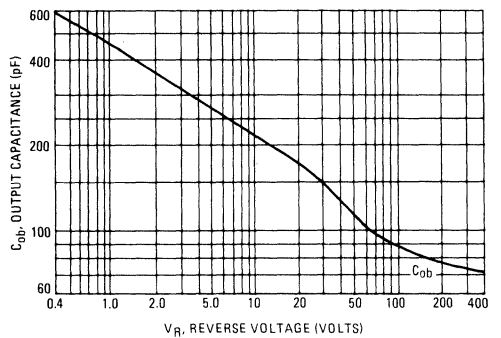
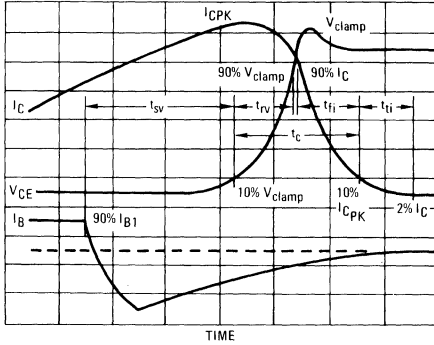


FIGURE 6 – OUTPUT CAPACITANCE



SWITCHING TIMES NOTE

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, $90\% I_{B1}$ to $10\% V_{clamp}$

t_{rv} = Voltage Rise Time, $10-90\% V_{clamp}$

t_{fi} = Current Fall Time, $90-10\% I_C$

t_{ti} = Current Tail, $10-2\% I_C$

t_c = Crossover Time, $10\% V_{clamp}$ to $10\% I_C$

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

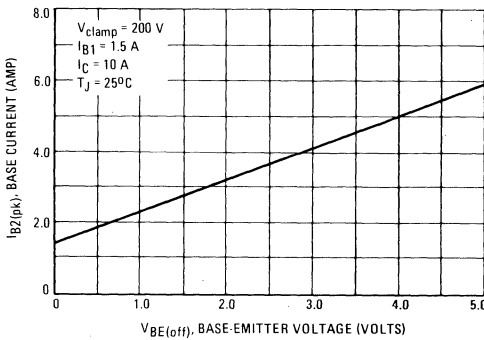
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at $25^\circ C$ and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at $100^\circ C$.

FIGURE 8 – REVERSE BASE CURRENT versus BASE EMITTER VOLTAGE



RESISTIVE SWITCHING

FIGURE 9 – TURN-ON TIME

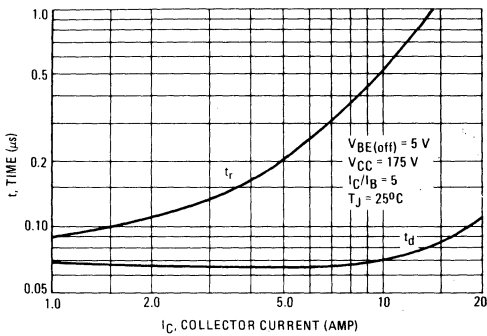


FIGURE 10 – TURN-OFF TIME

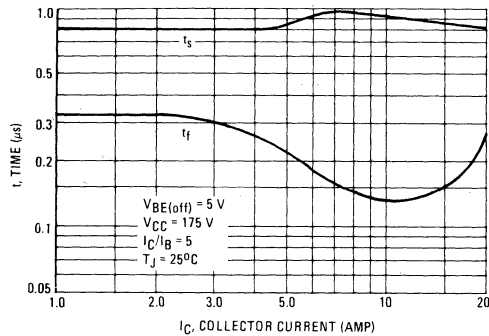
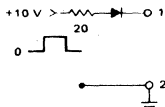
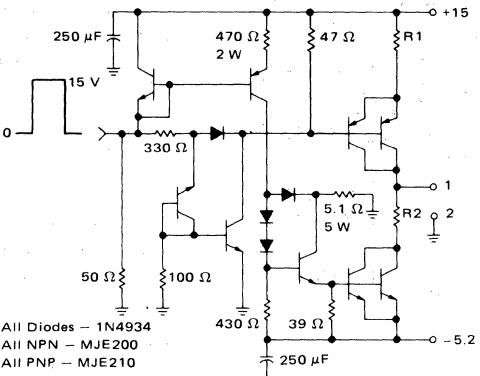
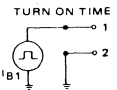
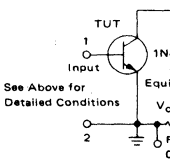
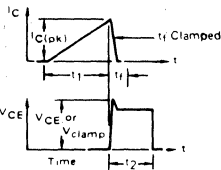
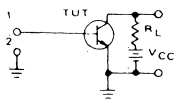
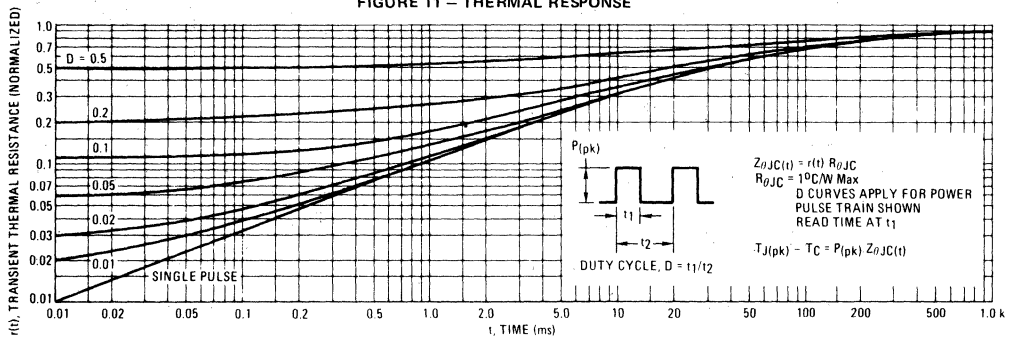


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>	 <p>All Diodes - 1N4934 All NPN - MJE200 All PNP - MJE210 Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For V_{CEO(sus)}, R2 = ∞</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	L _{coil} = 80 mH V _{CC} = 10 V R _{coil} = 0.7 Ω	L _{coil} = 180 μH R _{coil} = 0.05 Ω V _{CC} = 20 V V _{clamp} = 200 V	V _{CC} = 175 V R _L = 17.5 Pulse Width = 25 μs
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>  <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$</p> <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

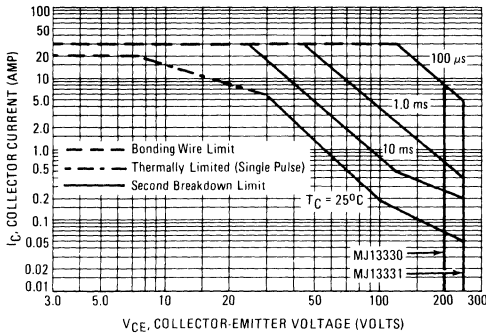
3

FIGURE 11 - THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA



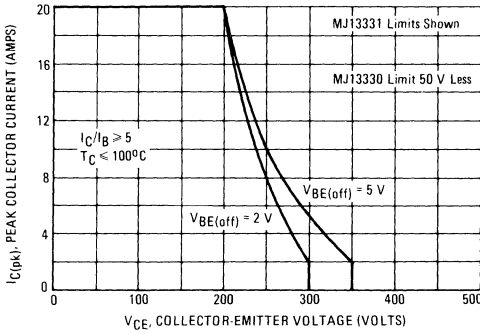
FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

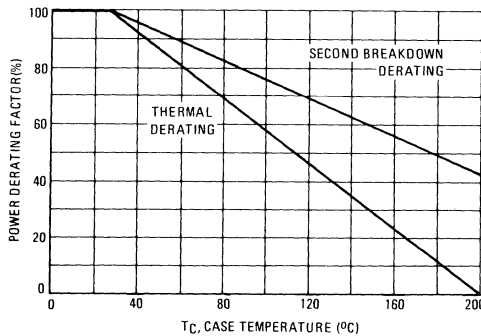
FIGURE 13 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJ13333 and MJ13335 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

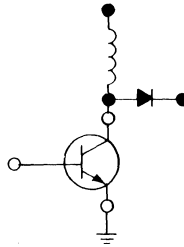
Fast Turn-Off Times

200 ns Inductive Fall Time—25°C (Typ)
 1.8 μs Inductive Storage Time—25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

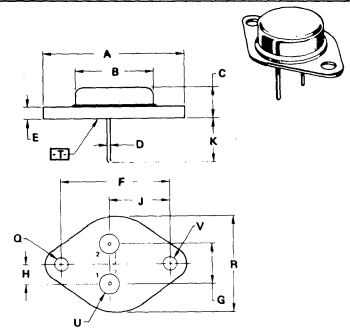


20 AMPERE
NPN SILICON
POWER TRANSISTORS

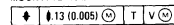
400-500 VOLTS
175 WATTS

Designer's Data for
"Worst Case" Conditions

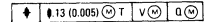
The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



- NOTES:**
1. DIMENSIONS Q AND V ARE DATUMS.
 2. [E] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:



FOR LEADS:



4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	—	1.187 BSC	—
G	10.92 BSC	—	0.430 BSC	—
H	5.48 BSC	—	0.215 BSC	—
J	16.89 BSC	—	0.665 BSC	—
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MJ13333	MJ13335	Unit
Collector-Emitter Voltage	V_{CEO}	400	500	Vdc
Collector-Emitter Voltage	V_{CEV}	700	800	Vdc
Emitter Base Voltage	V_{EB}	—	6.0	Vdc
Collector Current — Continuous	I_C	20	—	Adc
Peak (1)	I_{CM}	30	—	Adc
Base Current — Continuous	I_B	10	—	Adc
Peak (1)	I_{BM}	15	—	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175	—	Watts
Derate above 25°C	—	100	—	W/ $^\circ\text{C}$
@ $T_C = 100^\circ\text{C}$	—	1.0	—	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering	T_L	275	$^\circ\text{C}$
Purposes: 1/8" from Case for 5 Seconds	—	—	—

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Similar device types available with lower V_{CEO} ratings, see the MJ13330 (200 V) and MJ13331 (250 V).

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJ13335 MJ13333	$V_{CE0(sus)}$	500 400	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^{\circ}\text{C}$)		I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^{\circ}\text{C}$)		I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	10	—	60	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 6.7\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2.0\text{ Adc}$, $T_C = 100^{\circ}\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.8 5.0 2.4	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 2.0\text{ Adc}$, $T_C = 100^{\circ}\text{C}$)	$V_{BE(sat)}$	— —	— —	1.8 1.8	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	125	—	500	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 250 Vdc, I _C = 10 A, I _{B1} = 2.0 A, V _{BE(off)} = 5.0 Vdc, t _p = 10 μs, Duty Cycle < 2.0%)	t _d	—	0.02	0.1	μs
Rise Time		t _r	—	0.3	0.7	μs
Storage Time		t _s	—	1.6	4.0	μs
Fall Time		t _f	—	0.3	0.7	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I _C = 10 A(pk), V _{clamp} = 250 Vdc, I _{B1} = 2.0 A, V _{BE(off)} = 5 Vdc, T _C = 100°C)	t _{sv}	—	2.5	5.0	μs
Crossover Time		t _c	—	0.8	2.0	μs
Storage Time	(I _C = 10 A(pk), V _{clamp} = 250 Vdc, I _{B1} = 2.0 A, V _{BE(off)} = 5 Vdc, T _C = 25°C)	t _{sv}	—	1.8	—	μs
Crossover Time		t _c	—	0.4	—	μs
Fall Time		t _{fi}	—	0.2	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle < 2%.



FIGURE 1 – DC CURRENT GAIN

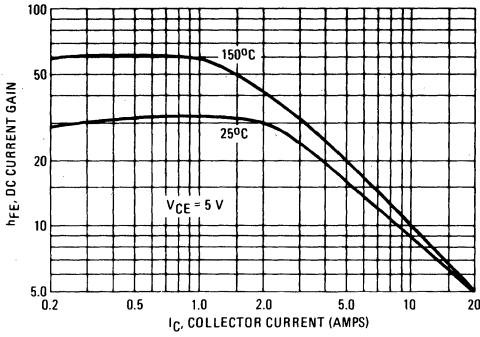


FIGURE 2 – COLLECTOR SATURATION REGION

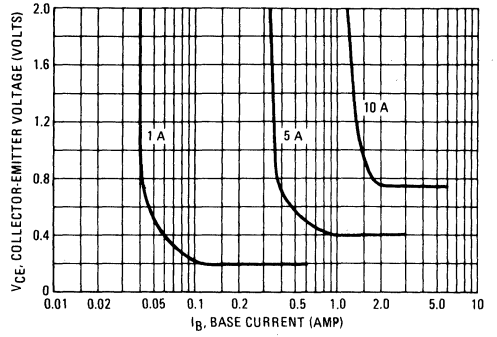


FIGURE 3 – COLLECTOR-EMITTER SATURATION REGION

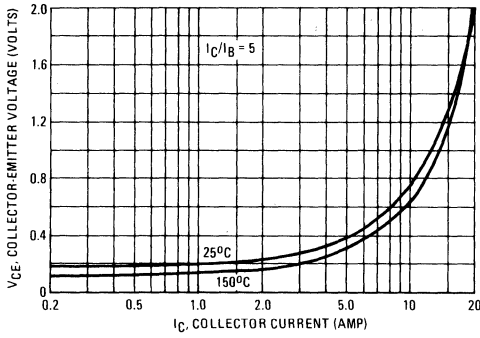
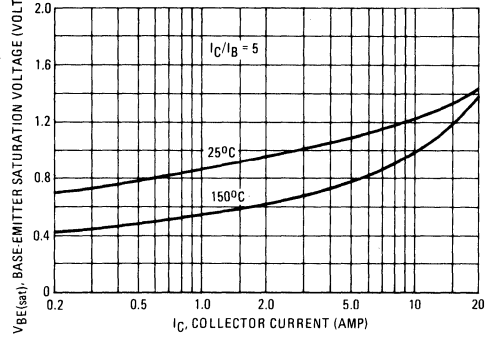


FIGURE 4 – BASE-EMITTER VOLTAGE



3

FIGURE 5 – COLLECTOR CUTOFF REGION

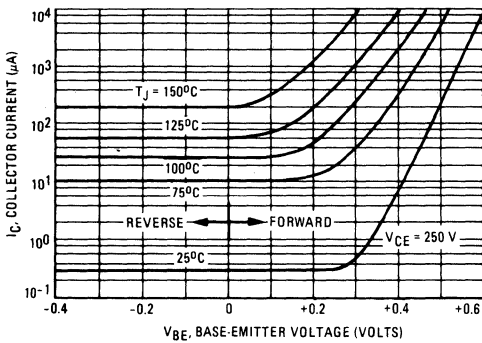
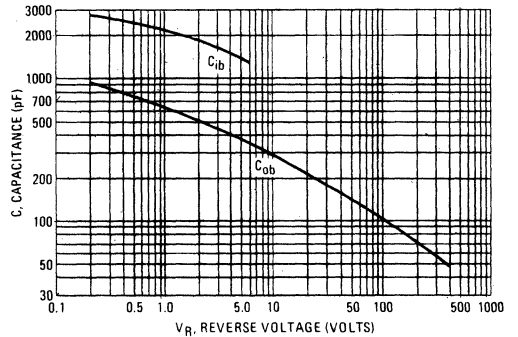
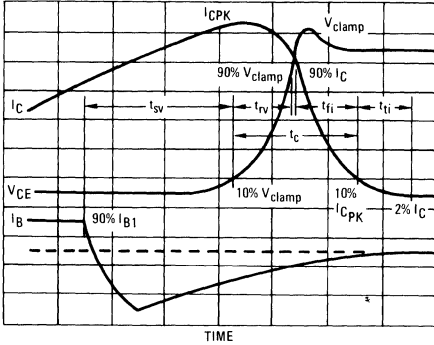


FIGURE 6 – CAPACITANCE



SWITCHING TIMES NOTE

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

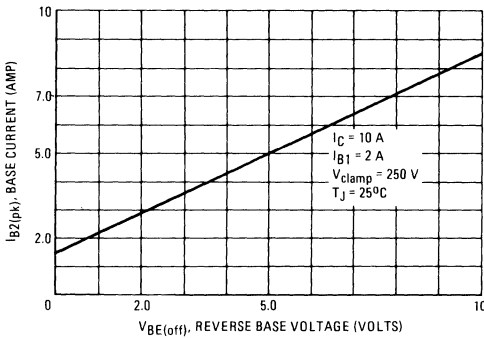
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 8 – REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON SWITCHING TIMES

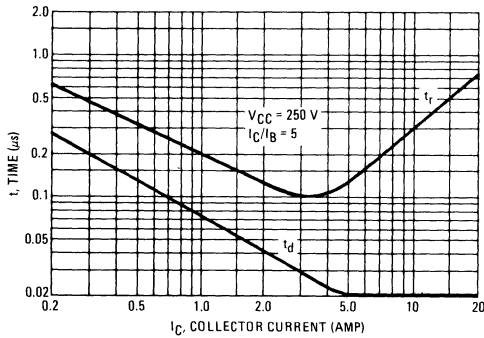


FIGURE 10 – TURN-OFF SWITCHING TIMES

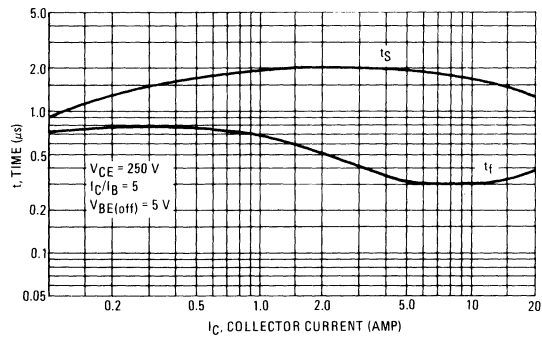


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>+10 V 20 PW Varied to Attain I_C = 100 mA</p>	<p>All Diodes - 1N4934 All NPN - MJE200 All PNP - MJE210</p> <p>Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For V_{CEO(sus)}, R2 = ∞</p>	<p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}</p>	<p>V_{CC} = 250 V R_L = 50 Ω Pulse Width = 10 µs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

FIGURE 11 - THERMAL RESPONSE

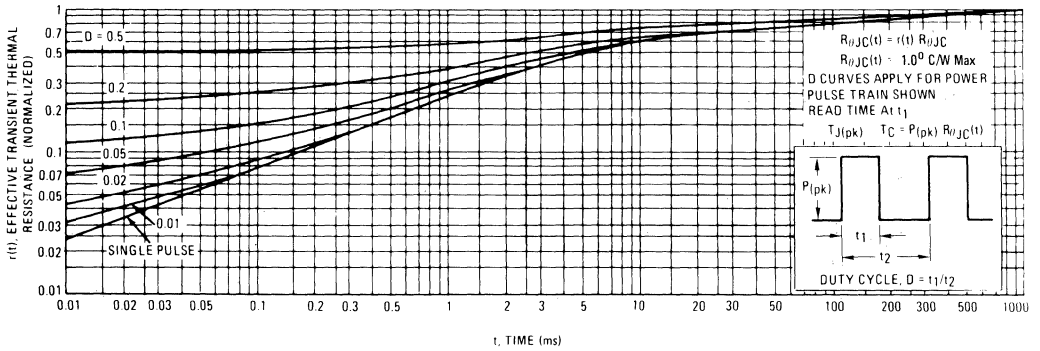


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

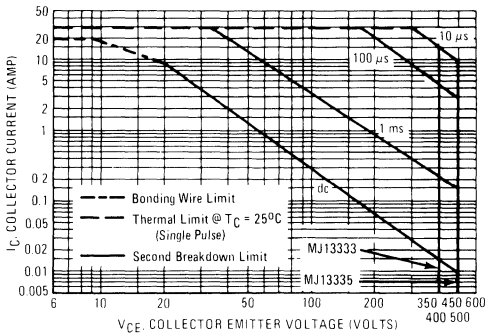


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA

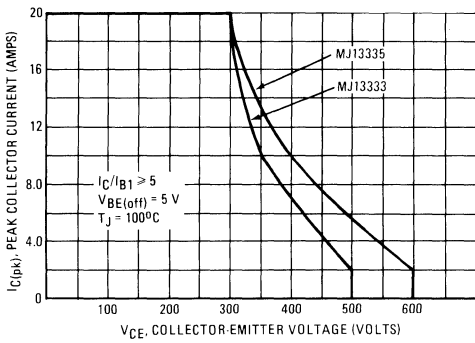
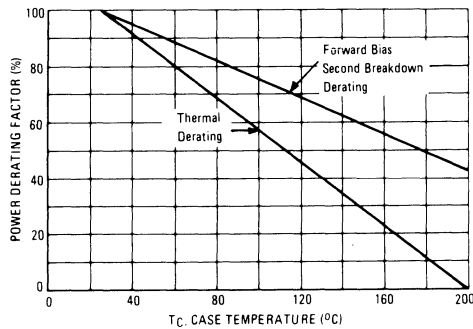


FIGURE 14 – POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

HIGH-CURRENT COMPLEMENTARY SILICON POWER TRANSISTORS

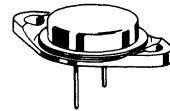
... designed for use in high-power amplifier and switching circuit applications.

- High Current Capability – I_C Continuous = 60 Amperes
- DC Current Gain – $h_{FE} = 15-100$ @ $I_C = 50$ Adc
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)} = 2.5$ Vdc (Max) @ $I_C = 50$ Adc

60 AMPERES

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
300 WATTS

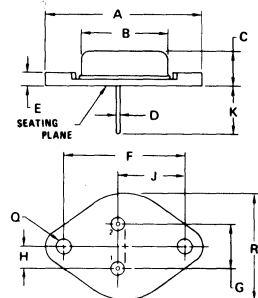


MAXIMUM RATINGS

Rating	Symbol	MJ14000 MJ14001	MJ14002 MJ14003	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CBO}	60	80	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector Current – Continuous	I_C	60		A dc
Base Current – Continuous	I_B	15		A dc
Emitter Current – Continuous	I_E	75		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	300		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.584	$^\circ\text{C/W}$

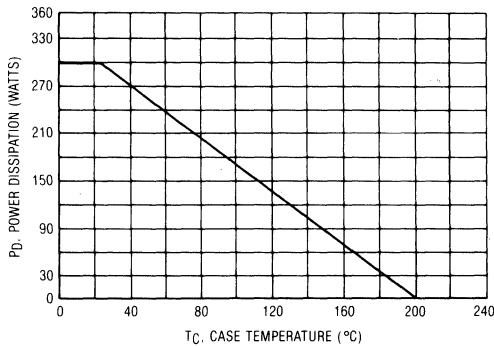


STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	28.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

FIGURE 1 – POWER DERATING



NPN MJ14000, MJ14002
PNP MJ14001, MJ14003

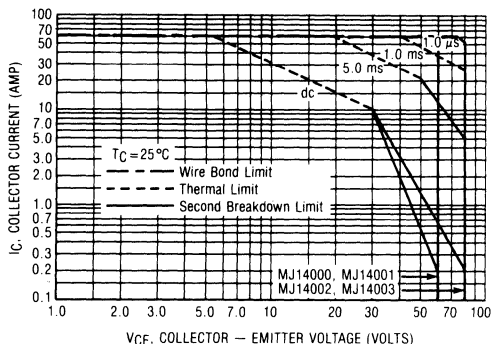
ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	60 80	— —	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	— —	1.0 1.0	mA
Collector Cutoff Current ($V_{CE} = 60 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ V}$) ($V_{CE} = 80 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ V}$)	I_{CEX}	— —	1.0 1.0	mA
Collector Cutoff Current ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	— —	1.0 1.0	mA
Emitter Cutoff Current ($V_{BE} = 5 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	mA
ON CHARACTERISTICS				
DC Current Gain (1) ($I_C = 25 \text{ Adc}$, $V_{CE} = 3.0 \text{ V}$) ($I_C = 50 \text{ Adc}$, $V_{CE} = 3.0 \text{ V}$) ($I_C = 60 \text{ Adc}$, $V_{CE} = 3.0 \text{ V}$)	h_{FE}	30 15 5	— 100 —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 25 \text{ Adc}$, $I_B = 2.5 \text{ Adc}$) ($I_C = 50 \text{ Adc}$, $I_B = 5.0 \text{ Adc}$) ($I_C = 60 \text{ Adc}$, $I_B = 12 \text{ Adc}$)	$V_{CE(sat)}$	— — —	1 2.5 3	Vdc
Base-Emitter Saturation Voltage (1) ($I_C = 25 \text{ Adc}$, $I_B = 2.5 \text{ Adc}$) ($I_C = 50 \text{ Adc}$, $I_B = 5.0 \text{ Adc}$) ($I_C = 60 \text{ Adc}$, $I_B = 12 \text{ Adc}$)	$V_{BE(sat)}$	— — —	2 3 4	Vdc
DYNAMIC CHARACTERISTICS				
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	—	2000	pF

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

3

FIGURE 2 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

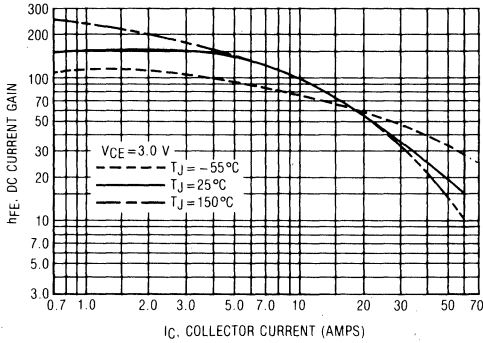
The data of Figure 2 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

NPN MJ14000, MJ14002
PNP MJ14001, MJ14003

TYPICAL ELECTRICAL CHARACTERISTICS

NPN
MJ14000, MJ14002

FIGURE 3 — DC CURRENT GAIN



PNP
MJ14001, MJ14003

FIGURE 4 — DC CURRENT GAIN

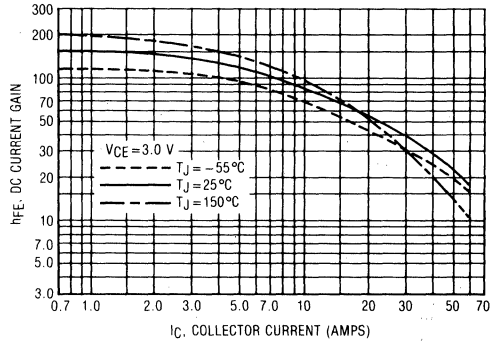


FIGURE 5 — COLLECTOR SATURATION REGION

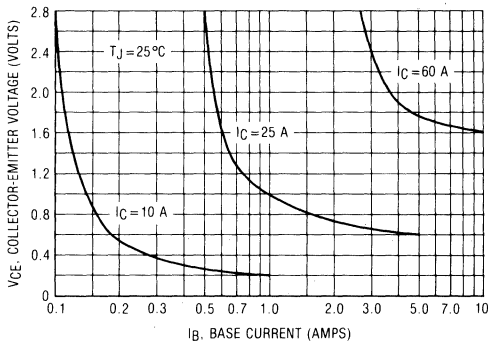


FIGURE 6 — COLLECTOR SATURATION REGION

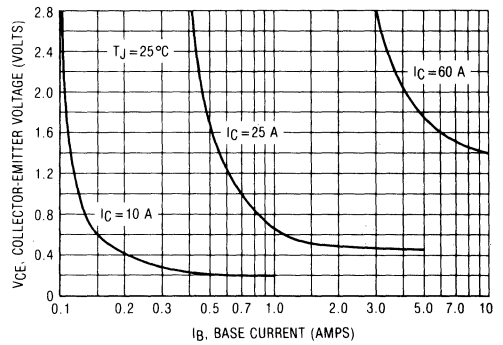


FIGURE 7 — "ON" VOLTAGES

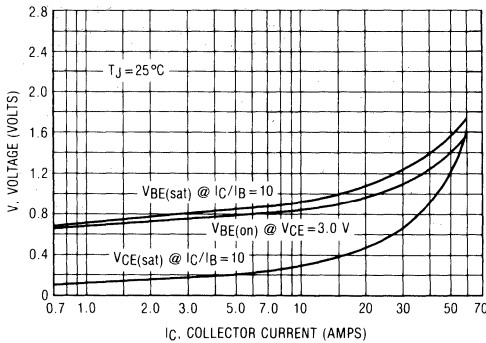
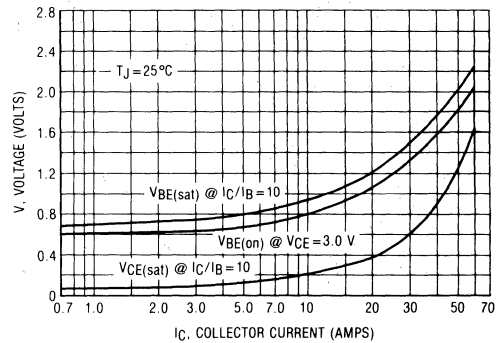


FIGURE 8 — "ON" VOLTAGES



3

NPN MJ14000, MJ14002
PNP MJ14001, MJ14003

FIGURE 9 – TURN-ON SWITCHING TIMES

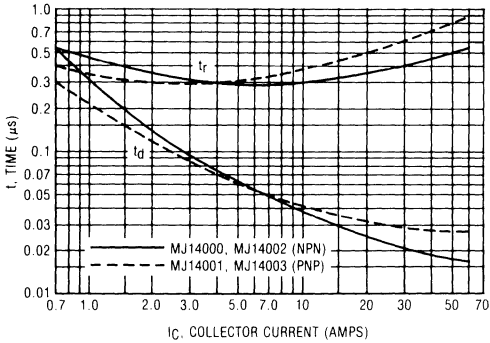


FIGURE 10 - TURN-OFF SWITCHING TIMES

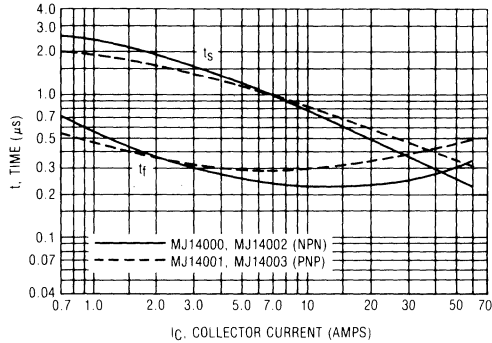


FIGURE 11 – CAPACITANCE VARIATION

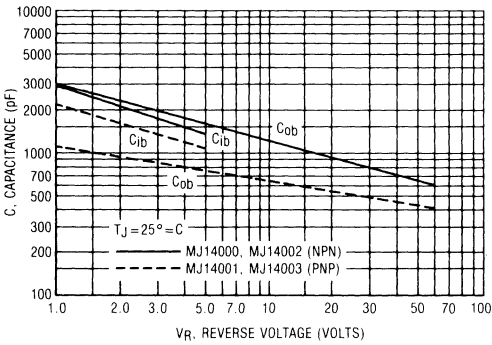
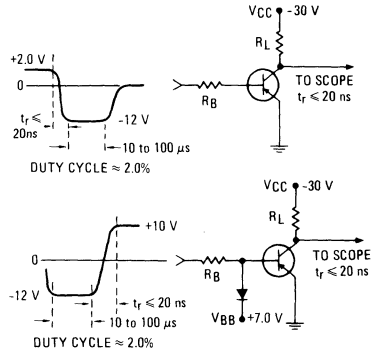
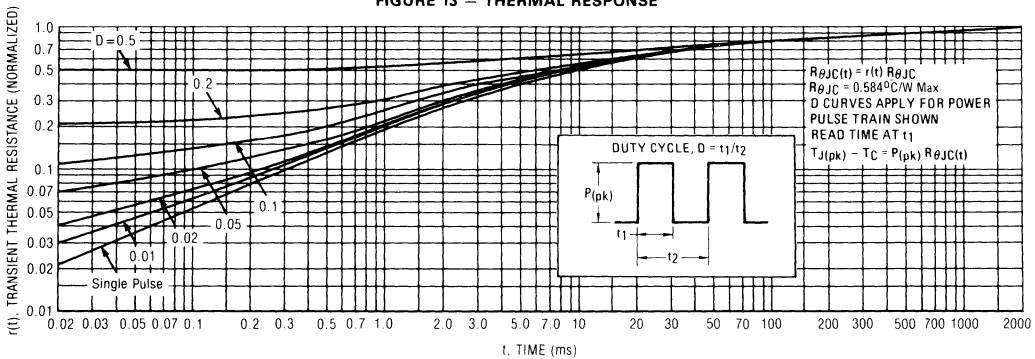


FIGURE 12 – SWITCHING TEST CIRCUIT



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
 INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
 FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

FIGURE 13 – THERMAL RESPONSE



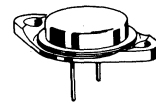
COMPLEMENTARY SILICON POWER TRANSISTORS

The MJ15001 and MJ15002 are EpiBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) –
 200 W @ 40 V
 50 W @ 100 V
- For Low Distortion Complementary Designs
- High DC Current Gain –
 $h_{FE} = 25$ (Min) @ $I_C = 4$ Adc

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON

140 VOLTS
200 WATTS

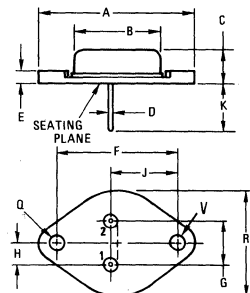


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	140	Vdc
Collector-Base Voltage	V_{CBO}	140	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current – Continuous	I_C	15	Aadc
Base Current – Continuous	I_B	5	Aadc
Emitter Current – Continuous	I_E	20	Aadc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	200 1.14	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for $\leq 10\text{s}$.	T_L	265	$^\circ\text{C}$



- NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
 2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\boxed{\text{M}} \text{ } \boxed{0.25} \text{ (0.010)} \text{ } \boxed{\text{M}} \text{ } \boxed{\text{T}} \text{ } \boxed{\text{V}} \text{ } \boxed{\text{M}}$
 3. POSITIONAL TOLERANCE FOR LEADS:
 $\boxed{\text{M}} \text{ } \boxed{0.30} \text{ (0.012)} \text{ } \boxed{\text{M}} \text{ } \boxed{\text{T}} \text{ } \boxed{\text{V}} \text{ } \boxed{\text{M}} \text{ } \boxed{\text{Q}} \text{ } \boxed{\text{M}}$
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973. STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

NPN MJ15001
PNP MJ15002

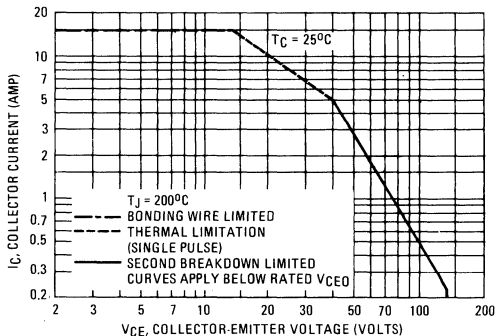
ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	140	—	Vdc
Collector Cutoff Current ($V_{CE} = 140 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 140 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	—	100 2	μAdc mAdc
Collector Cutoff Current ($V_{CE} = 140 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	250	μAdc
Emitter Cutoff Current ($V_{EB} = 5 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 40 \text{ Vdc}$, $t = 1 \text{ s}$ (non-repetitive)) ($V_{CE} = 100 \text{ Vdc}$, $t = 1 \mu\text{s}$ (non-repetitive))	$I_{S/b}$	5 0.5	— —	Adc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 4 \text{ Adc}$, $V_{CE} = 2 \text{ Vdc}$)	h_{FE}	25	150	—
Collector-Emitter Saturation Voltage ($I_C = 4 \text{ Adc}$, $I_B = 0.4 \text{ Adc}$)	$V_{CE(sat)}$	—	1	Vdc
Base-Emitter On Voltage ($I_C = 4 \text{ Adc}$, $V_{CE} = 2 \text{ Vdc}$)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 0.5 \text{ MHz}$)	f_T	2	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f_{test} = 1 \text{ MHz}$)	C_{ob}	—	1000	pF

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.



FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN MJ15001
PNP MJ15002

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

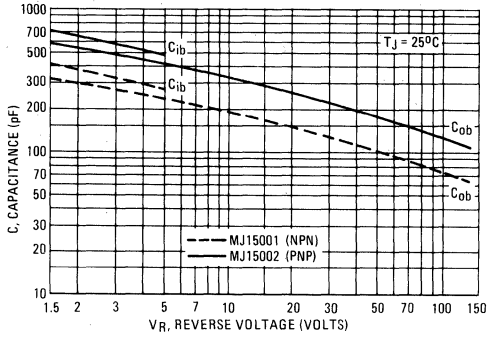


FIGURE 3 – CURRENT-GAIN – BANDWIDTH PRODUCT

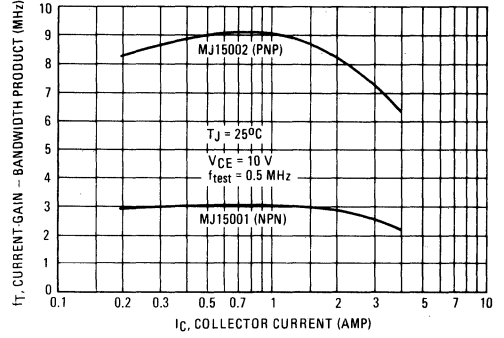
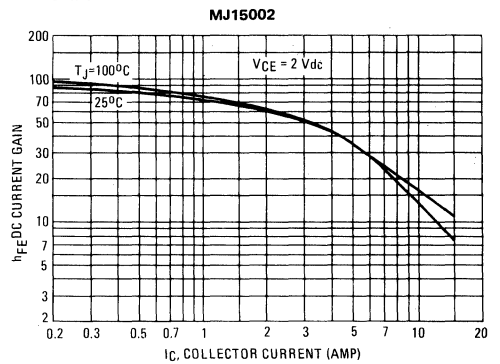
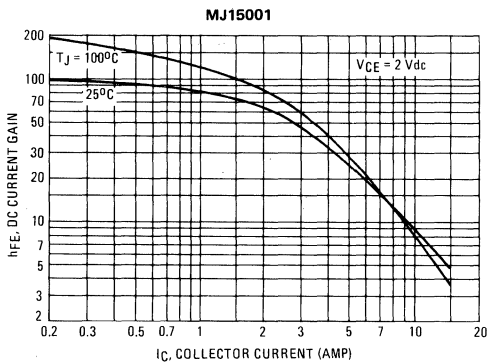
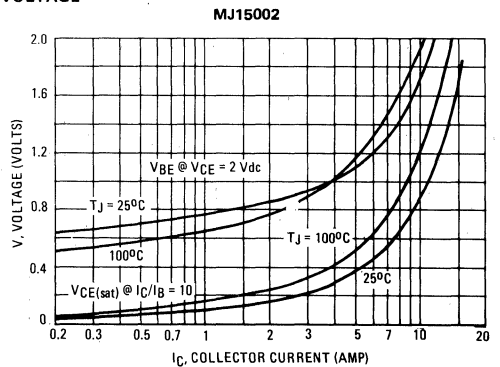
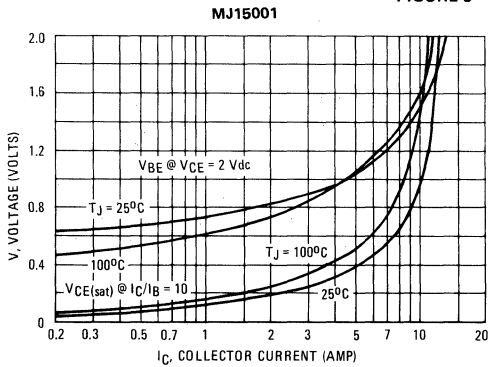


FIGURE 4 – DC CURRENT GAIN



3

FIGURE 5 – "ON" VOLTAGE



NPN
MJ15003
PNP
MJ15004

COMPLEMENTARY SILICON POWER TRANSISTORS

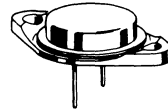
The MJ15003 and MJ15004 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) – 250 W @ 50 V
- For Low Distortion Complementary Designs
- High DC Current Gain – $h_{FE} = 25$ (Min) @ $I_C = 5$ Adc

20 AMPERE

POWER TRANSISTORS
COMPLEMENTARY SILICON

140 VOLTS
250 WATTS

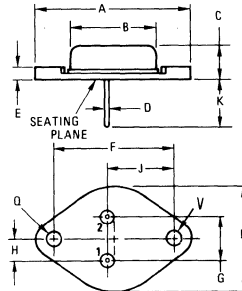


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	140	Vdc
Collector-Base Voltage	V_{CBO}	140	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current – Continuous	I_C	20	Adc
Base Current – Continuous	I_B	5	Adc
Emitter Current – Continuous	I_E	25	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	250 1.43	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for $\leq 10s$.	T_L	265	$^\circ\text{C}$



- NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
 2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\text{HOLE Q: } \text{Ø } 0.25 (0.010) \text{ M } \text{T } \text{V } \text{M}$
 3. POSITIONAL TOLERANCE FOR LEADS:
 $\text{LEADS: } \text{Ø } 0.30 (0.012) \text{ M } \text{T } \text{V } \text{M } \text{Q } \text{M}$
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973. STYLE 1:

PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	-	3.43	-	0.135
F	30.15 BSC	-	1.187 BSC	-
G	10.92 BSC	-	0.430 BSC	-
H	5.46 BSC	-	0.215 BSC	-
J	16.89 BSC	-	0.665 BSC	-
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	-	26.67	-	1.050
V	3.84	4.09	0.151	0.161

CASE 11-01
TO-204AA

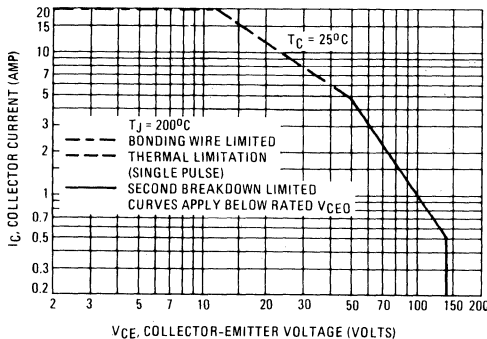
NPN MJ15003, PNP MJ15004

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 200 mA, I _B = 0)	V _{CEO(sus)}	140	—	Vdc
Collector Cutoff Current (V _{CE} = 140 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CE} = 140 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 150°C)	I _{CEX}	—	100	μAdc
Collector Cutoff Current (V _{CE} = 140 Vdc, I _B = 0)	I _{CEO}	—	2	mAdc
Collector Cutoff Current (V _{CE} = 140 Vdc, I _B = 0)	I _{CEO}	—	250	μAdc
Emitter Cutoff Current (V _{EB} = 5 Vdc, I _C = 0)	I _{EBO}	—	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V _{CE} = 50 Vdc, t = 1 s (non-repetitive)) (V _{CE} = 100 Vdc, t = 1 s (non-repetitive))	I _{S/b}	5	—	Adc
		1	—	
ON CHARACTERISTICS				
DC Current Gain (I _C = 5 Adc, V _{CE} = 2 Vdc)	h _{FE}	25	150	
Collector-Emitter Saturation Voltage (I _C = 5 Adc, I _B = 0.5 Adc)	V _{CE(sat)}	—	1	Vdc
Base-Emitter On Voltage (I _C = 5 Adc, V _{CE} = 2 Vdc)	V _{BE(on)}	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I _C = 0.5 Adc, V _{CE} = 10 Vdc, f _{test} = 0.5 MHz)	f _T	2	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1 MHz)	C _{ob}	—	1000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_{J(pk)} = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN MJ15003, PNP MJ15004

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

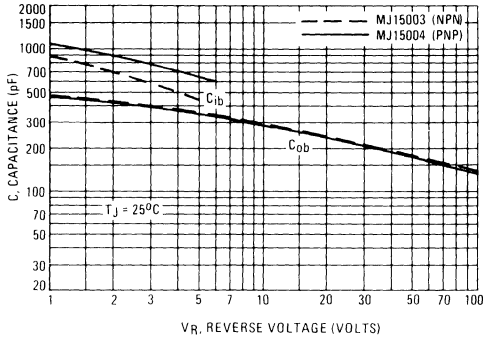


FIGURE 3 – CURRENT GAIN – BANDWIDTH PRODUCT

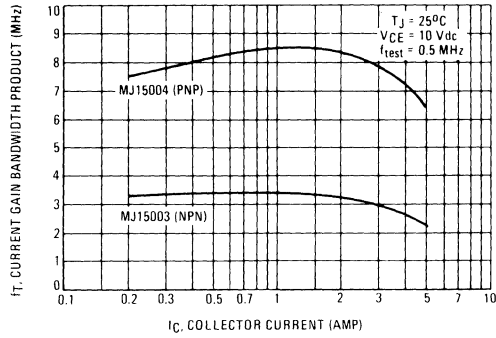


FIGURE 4 – DC CURRENT GAIN

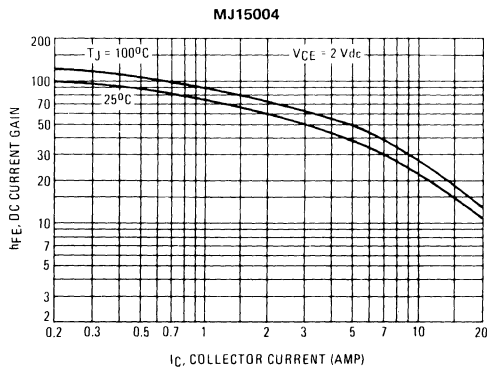
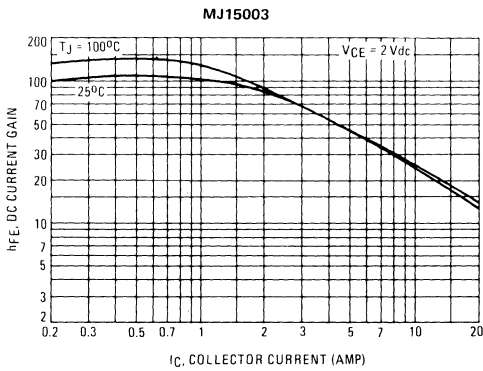
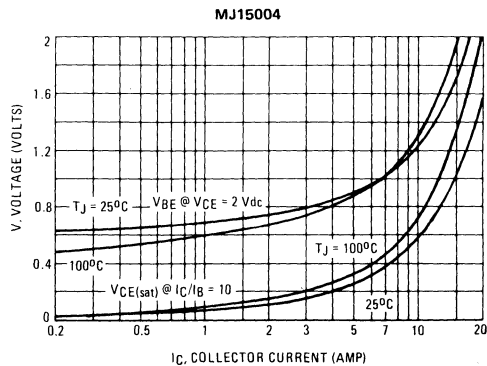
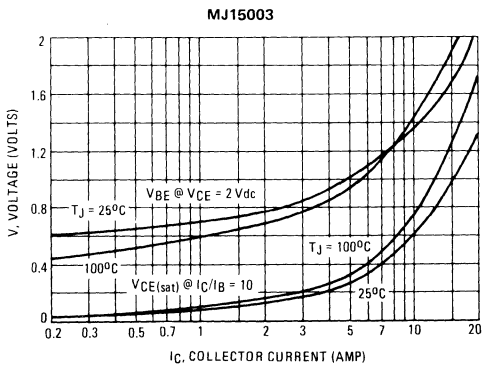


FIGURE 5 – "ON" VOLTAGE



3

NPN
MJ15011
PNP
MJ15012

Advance Information

COMPLEMENTARY SILICON POWER TRANSISTORS

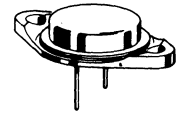
The MJ15011 and MJ15012 are PowerBase power transistors designed for high-power audio, disk head positioners, and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc-to-dc converters or inverters.

- High Safe Operating Area (100% Tested)
1.2 A @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
hFE = 20 (Min) @ 2 A, 2 V
VCE(sat) = 2.5 V (Max) @ IC = 4 A, IB = 0.4 A
- For Low Distortion Complementary Designs

10 AMPERE

**COMPLEMENTARY
 POWER TRANSISTORS**

**250 VOLTS
 200 WATTS**



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	VCEO	250	Vdc
Collector-Emitter Voltage	VCEX	250	Vdc
Emitter-Base Voltage	VEB	5	Vdc
Collector Current — Continuous	IC	10	A dc
— Peak (1)	ICM	15	A dc
Base Current — Continuous	IB	2	A dc
— Peak (1)	IBM	5	A dc
Emitter Current — Continuous	IE	12	A dc
— Peak (1)	IEM	20	A dc
Total Power Dissipation @ TC = 25°C	PD	200	Watts
Derate above 25°C		1.14	W/°C
Operating and Storage Junction Temperature Range	TJ, Tstg	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	RθJC	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes	TL	265	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

- NOTES:
1. DIAMETERS Q, V AND SURFACE T ARE DATUMS.
 2. POSITIONAL TOLERANCE FOR HOLE Q:
⊕ 0.25 (0.010) ⊕ T V ⊕
 3. POSITIONAL TOLERANCE FOR LEADS:
⊕ 0.30 (0.012) ⊕ T V ⊕ Q ⊕
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973. STYLE 1.

PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	30.16	BSC	1.187	BSC
G	10.92	BSC	0.430	BSC
H	5.46	BSC	0.215	BSC
J	16.89	BSC	0.665	BSC
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050
V	3.84	4.09	0.151	0.161

**CASE 11-01
 TO-204AA**

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

NPN MJ15011, PNP MJ15012

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 100\text{ mA}$)	$V_{(BR)CEO}$	250	—	Vdc
Collector Cutoff Current ($V_{CE} = 200\text{ Vdc}$)	I_{CEO}	—	1	mAdc
Collector Cutoff Current ($V_{CE} = 250\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$)	I_{CEX}	—	500	μAdc
Emitter Cutoff Current ($V_{BE} = 5\text{ Vdc}$)	I_{EBO}	—	500	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 2\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$) ($I_C = 4\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$)	h_{FE}	20 5	100 —	—
Collector-Emitter Saturation Voltage ($I_C = 2\text{ Adc}$, $I_B = 0.2\text{ Adc}$) ($I_C = 4\text{ Adc}$, $I_B = 0.4\text{ Adc}$)	$V_{CE(sat)}$	— —	0.8 2.5	Vdc
Base-Emitter On Voltage ($I_C = 4\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $f = 1\text{ MHz}$)	C_{ob}	—	750	pF
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 40\text{ Vdc}$, $t = 0.5\text{ s}$) ($V_{CE} = 100\text{ Vdc}$, $t = 0.5\text{ s}$)	$I_{S/b}$	5 1.4	— —	Adc

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

FIGURE 1 — DC CURRENT GAIN

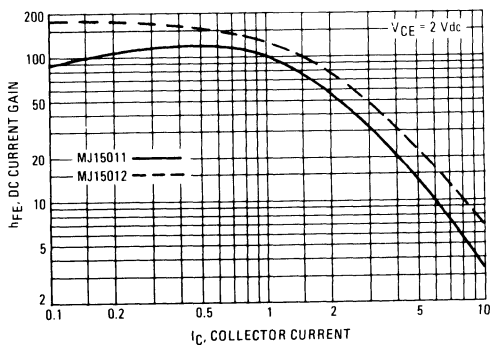
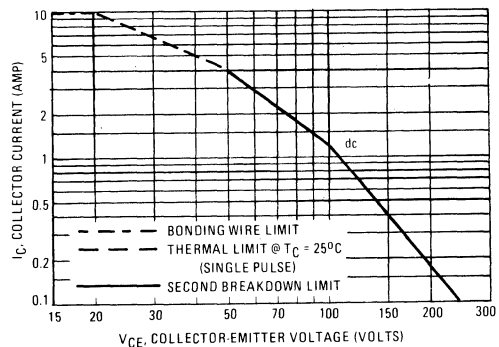


FIGURE 2 — ACTIVE REGION SAFE OPERATING AREA



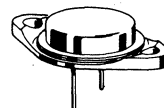
SILICON POWER TRANSISTORS

The MJ15022 and MJ15024 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) –
2 A @ 80 V
- High DC Current Gain –
 $h_{FE} = 15$ (Min) @ $I_C = 8$ Adc

16 AMPERE
SILICON
POWER TRANSISTORS

200 and 250 VOLTS
250 WATTS



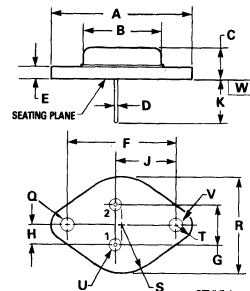
MAXIMUM RATINGS

Rating	Symbol	MJ15022	MJ15024	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Base Voltage	V_{CBO}	350	400	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector-Emitter Voltage	V_{CEX}	400		Vdc
Collector Current – Continuous	I_C	16		Aadc
Peak (1)		30		
Base Current – Continuous	I_B	5		Aadc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250		Watts
Derate above 25°C		1.43		W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	$^\circ\text{C}/\text{W}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.



STYLE 1:
 1. PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

NOTES:

- DIAMETER V AND SURFACE W ARE DATUMS.
- POSITIONAL TOLERANCE FOR HOLE Q:
 $\pm \phi 0.25$ (0.010) W V Q
- POSITIONAL TOLERANCE FOR LEADS:
 $\pm \phi 0.30$ (0.012) W V Q U

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA

NPN MJ15022, MJ15024

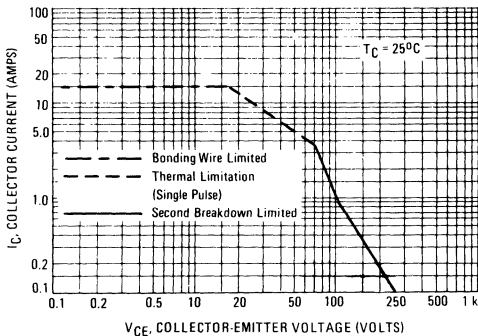
ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 100 \text{ mAdc}$, $I_B = 0$)	MJ15022 MJ15024	$V_{CE0(sus)}$	200 250	—
Collector Cutoff Current ($V_{CE} = 200 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 250 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$)	MJ15022 MJ15024	I_{CEX}	— —	250 250
Collector Cutoff Current ($V_{CE} = 150 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 200 \text{ Vdc}$, $I_B = 0$)	MJ15022 MJ15024	I_{CEO}	— —	$\mu\text{A dc}$ 500 500
Emitter Cutoff Current ($V_{CE} = 5 \text{ Vdc}$, $I_B = 0$)		I_{EBO}	—	500 $\mu\text{A dc}$
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 50 \text{ Vdc}$, $t = 0.5 \text{ s}$ (non-repetitive)) ($V_{CE} = 80 \text{ Vdc}$, $t = 0.5 \text{ s}$ (non-repetitive))		$I_{S/b}$	5 2	— — A dc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 8 \text{ A dc}$, $V_{CE} = 4 \text{ Vdc}$) ($I_C = 16 \text{ A dc}$, $V_{CE} = 4 \text{ Vdc}$)		h_{FE}	15 5	60 —
Collector-Emitter Saturation Voltage ($I_C = 8 \text{ A dc}$, $I_B = 0.8 \text{ A dc}$) ($I_C = 16 \text{ A dc}$, $I_B = 3.2 \text{ A dc}$)		$V_{CE(sat)}$	— —	1.4 4.0 Vdc
Base-Emitter On Voltage ($I_C = 8 \text{ A dc}$, $V_{CE} = 4 \text{ Vdc}$)		$V_{BE(on)}$	—	2.2 Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product ($I_C = 1 \text{ A dc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 1 \text{ MHz}$)		f_T	4	— MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f_{test} = 1 \text{ MHz}$)		C_{ob}	—	500 μF

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

3

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

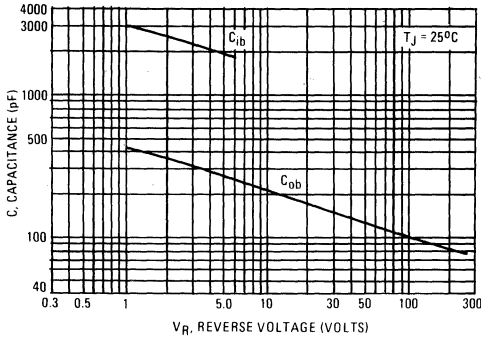


FIGURE 3 – CURRENT-GAIN-BANDWIDTH PRODUCT

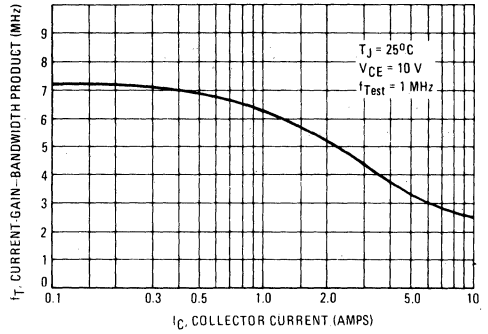


FIGURE 4 – DC CURRENT GAIN

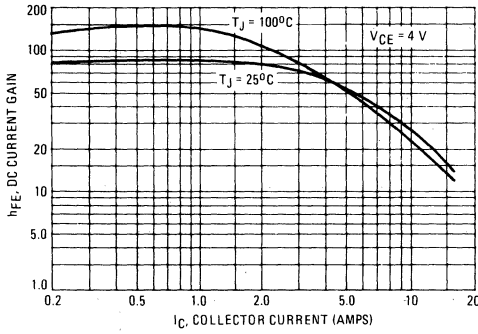


FIGURE 5 – "ON" VOLTAGE

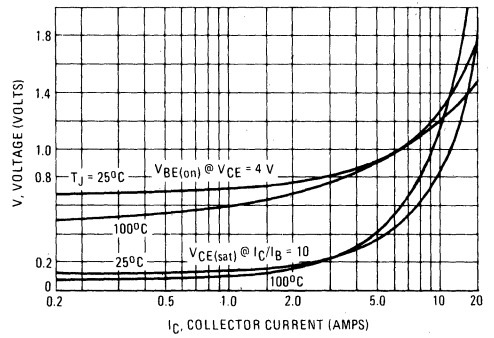
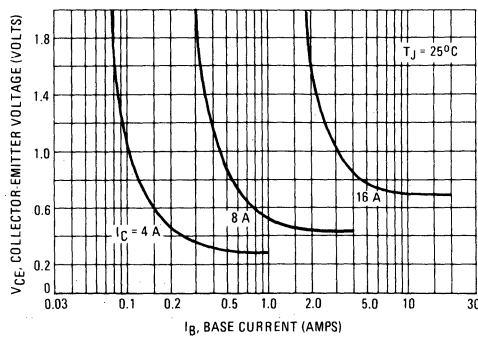


FIGURE 6 – COLLECTOR SATURATION REGION



3

PNP
MJ15023
MJ15025

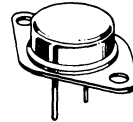
SILICON POWER TRANSISTORS

The MJ15023 and MJ15025 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) –
2 A @ 80 V
- High DC Current Gain –
 $h_{FE} = 15$ (Min) @ $I_C = 8$ Adc

16 AMPERE
SILICON
POWER TRANSISTORS

200 and 250 VOLTS
250 WATTS



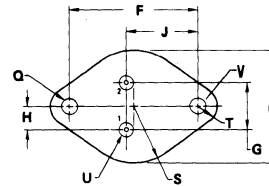
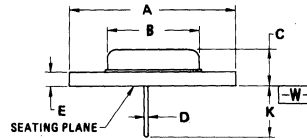
MAXIMUM RATINGS

Rating	Symbol	MJ15023	MJ15025	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Base Voltage	V_{CBO}	350	400	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector-Emitter Voltage	V_{CEX}	400		Vdc
Collector Current – Continuous	I_C	16		Adc
Peak (1)		30		
Base Current – Continuous	I_B	5		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250		Watts
Derate above 25°C		1.43		W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	$^\circ\text{C}/\text{W}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.



STYLE 1:
 PIN 1: BASE
 PIN 2: EMITTER
 CASE: COLLECTOR
 NOTE:
 1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

CASE 1-04
TO-204AA

MJ15023, MJ15025

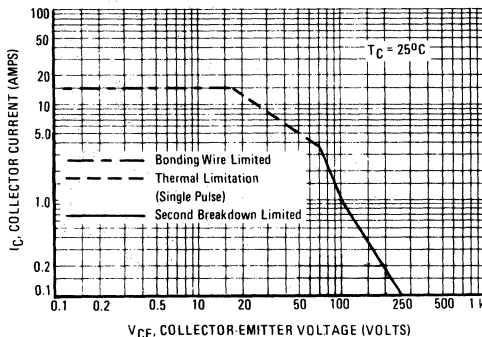
ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 100 \text{ mA}$, $I_B = 0$)	MJ15023 MJ15025	$V_{CE(sus)}$	200 250	—
Collector Cutoff Current ($V_{CE} = 200 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = 250 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$)	MJ15023 MJ15025	I_{CEX}	— —	250 250
Collector Cutoff Current ($V_{CE} = 150 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 200 \text{ Vdc}$, $I_B = 0$)	MJ15023 MJ15025	I_{CEO}	— —	500 500
Emitter Cutoff Current ($V_{CE} = 5 \text{ Vdc}$, $I_B = 0$)	Both	I_{EBO}	—	500
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 50 \text{ Vdc}$, $t = 0.5 \text{ s}$ (non-repetitive)) ($V_{CE} = 80 \text{ Vdc}$, $t = 0.5 \text{ s}$ (non-repetitive))		$I_{S/b}$	5 2	— —
ON CHARACTERISTICS				
DC Current Gain ($I_C = 8 \text{ Adc}$, $V_{CE} = 4 \text{ Vdc}$) ($I_C = 16 \text{ Adc}$, $V_{CE} = 4 \text{ Vdc}$)		h_{FE}	15 5	60 —
Collector-Emitter Saturation Voltage ($I_C = 8 \text{ Adc}$, $I_B = 0.8 \text{ Adc}$) ($I_C = 16 \text{ Adc}$, $I_B = 3.2 \text{ Adc}$)		$V_{CE(sat)}$	— —	1.4 4.0
Base-Emitter On Voltage ($I_C = 8 \text{ Adc}$, $V_{CE} = 4 \text{ Vdc}$)		$V_{BE(on)}$	—	2.2
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product ($I_C = 1 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 1 \text{ MHz}$)		f_T	4	—
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f_{test} = 1 \text{ MHz}$)		C_{ob}	—	600

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

3

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

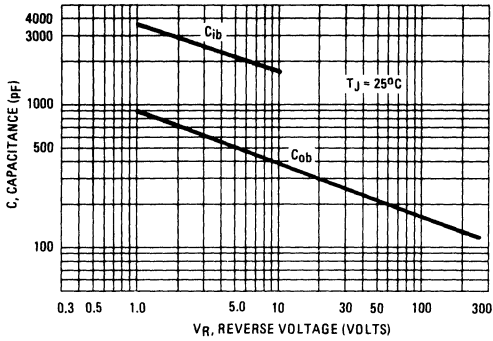


FIGURE 3 – CURRENT-GAIN-BANDWIDTH PRODUCT

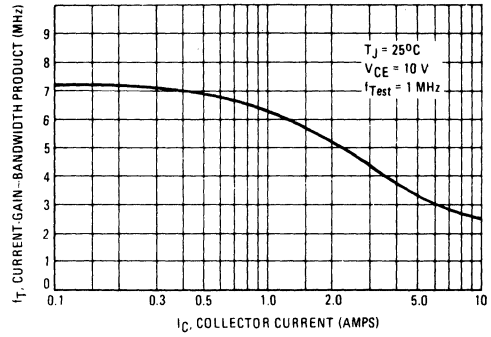


FIGURE 4 – DC CURRENT GAIN

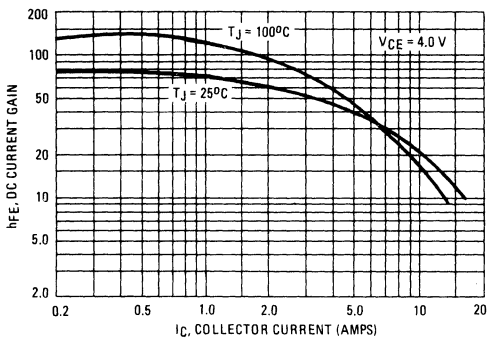
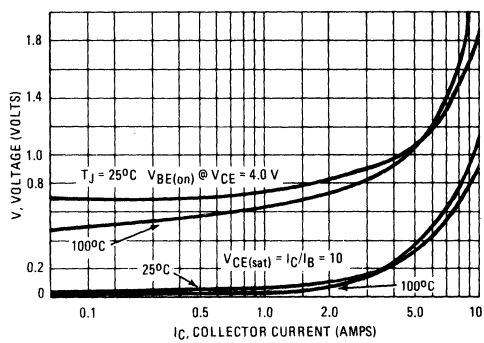


FIGURE 5 – "ON" VOLTAGE



Designers Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16004 is a selected high-gain version of the MJ16002 for applications where drive current is limited.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 50 ns Inductive Fall Time — 75°C (Typ)
 - 70 ns Inductive Crossover Time — 75°C (Typ)
 - 500 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range —65 to +200°C
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

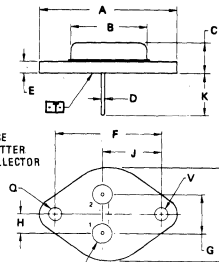
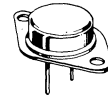
5 AMPERE

NPN SILICON
POWER TRANSISTORS

450 VOLTS
125 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 1
 PIN 1 BASE
 2 EMITTER
 CASE COLLECTOR

- NOTES:
1. DIMENSIONS G AND V ARE DATUMS.
 2. [T] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D:

$$\pm 0.13 (0.005) \text{ (T) V (O) (O)}$$

FOR LEADS:

$$\pm 0.13 (0.005) \text{ (T) V (O) (O)}$$

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	39.37	-	1.550
B	-	21.08	-	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	1.187 BSC		
G	10.92 BSC	0.430 BSC		
H	5.46 BSC	0.215 BSC		
J	16.89 BSC	0.665 BSC		
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.150	0.165
R	-	26.67	-	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	5.0	Adc
— Peak (1)	I_{CM}	10	Adc
Base Current — Continuous	I_B	4.0	Adc
— Peak (1)	I_{BM}	8.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	125	Watts
@ $T_C = 100^\circ\text{C}$		71.5	
Derate above 25°C		0.714	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

MJ16002

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE0(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 1.5\text{ Adc}$, $I_B = 0.2\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.0 2.5 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	5.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	200	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	($I_C = 3.0\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 0.4\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	($I_{B2} = 0.8\text{ Adc}$, $R_{B2} = 8.0\ \Omega$)	t_d	—	30	100	ns
Rise Time			t_r	—	100	300	
Storage Time			t_s	—	1000	3000	
Fall Time			t_f	—	60	300	
Storage Time			t_s	—	400	—	
Fall Time			t_f	—	130	—	
	($V_{BE(off)} = 5.0\text{ Vdc}$)						

Inductive Load (Table 2)

Storage Time	($I_C = 3.0\text{ Adc}$, $I_{B1} = 0.4\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	($T_J = 100^\circ\text{C}$)	t_{sv}	—	500	1600	ns
Fall Time			t_{fi}	—	100	200	
Crossover Time			t_c	—	120	250	
Storage Time			t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	
		($T_J = 150^\circ\text{C}$)					

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

$$* \beta_{ef} = \frac{I_C}{I_{B1}}$$

MJ16004

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 1.5\text{ Adc}$, $I_B = 0.15\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	1.0 2.5 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.5 1.5	Vdc
DC Current Gain ($I_C = 5.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	200	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	$(I_C = 3.0\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 0.3\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	$(I_{B2} = 0.6\text{ Adc}$, $R_{B2} = 8.0\ \Omega$)	t_d	—	30	100	ns
Rise Time			t_r	—	130	300	
Storage Time			t_s	—	800	2700	
Fall Time			t_f	—	80	350	
Storage Time			t_{s1}	—	250	—	
Fall Time		$(V_{BE(off)} = 5.0\text{ Vdc})$	t_{f1}	—	60	—	

Inductive Load (Table 2)

Storage Time	$(I_C = 3.0\text{ Adc}$, $I_{B1} = 0.3\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	$(T_J = 100^\circ\text{C})$	t_{sv}	—	400	1300	ns
Fall Time			t_{fi}	—	80	150	
Crossover Time			t_c	—	90	200	
Storage Time		$(T_J = 150^\circ\text{C})$	t_{sv}	—	450	—	
Fall Time			t_{fi}	—	100	—	
Crossover Time			t_c	—	110	—	

(1) Pulse Test: PW - 300 μs , Duty Cycle $\leq 2\%$.

$$*\beta_f = \frac{I_C}{I_{B1}}$$

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

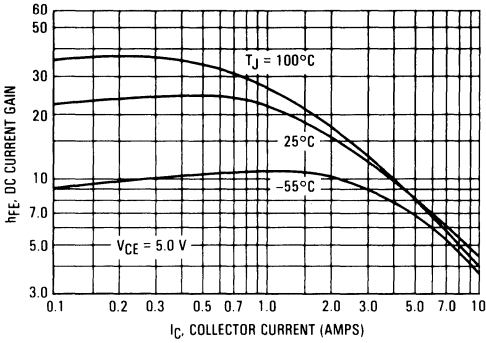


FIGURE 2 — COLLECTOR SATURATION REGION

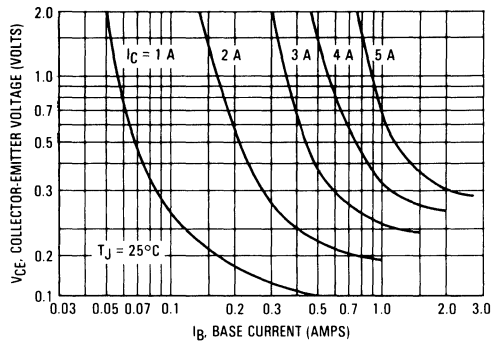


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

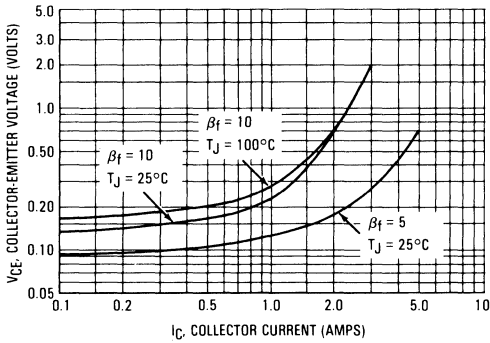


FIGURE 4 — BASE-EMITTER VOLTAGE

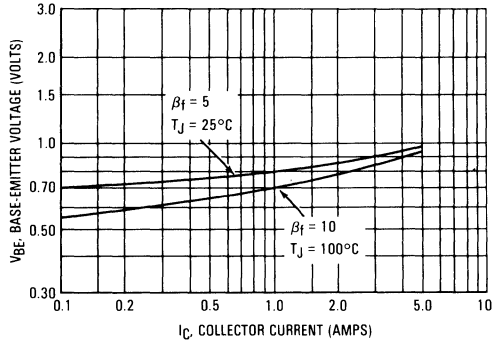


FIGURE 5 — COLLECTOR CUTOFF REGION

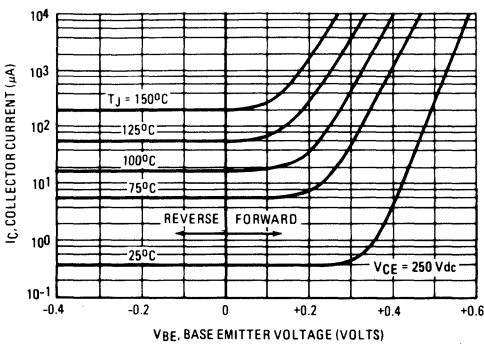
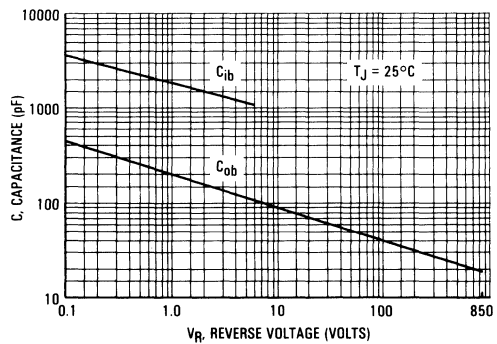


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

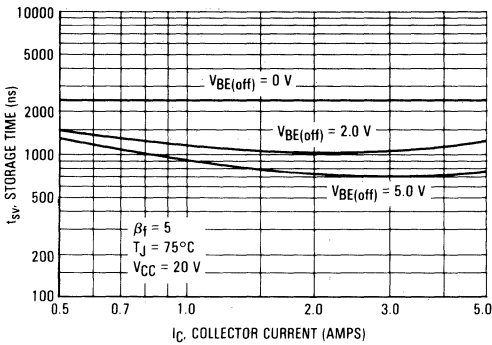


FIGURE 8 — STORAGE TIME

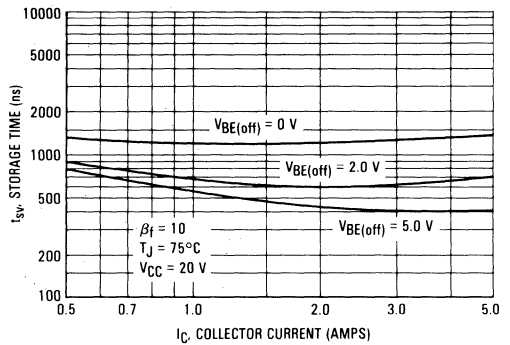


FIGURE 9 — COLLECTOR CURRENT FALL TIME

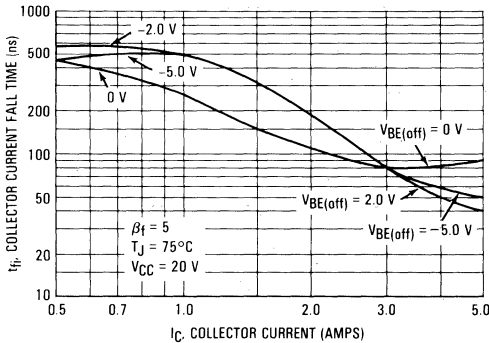


FIGURE 10 — COLLECTOR CURRENT FALL TIME

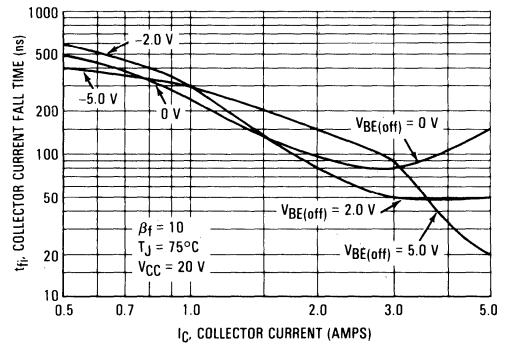


FIGURE 11 — CROSSOVER TIME

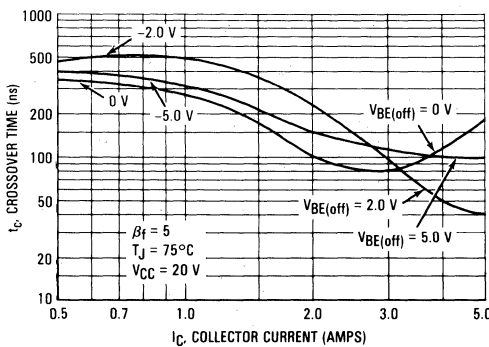
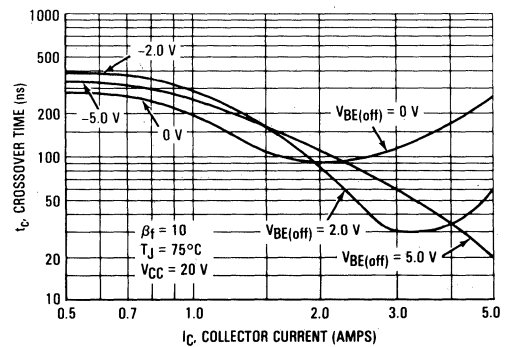


FIGURE 12 — CROSSOVER TIME



3

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

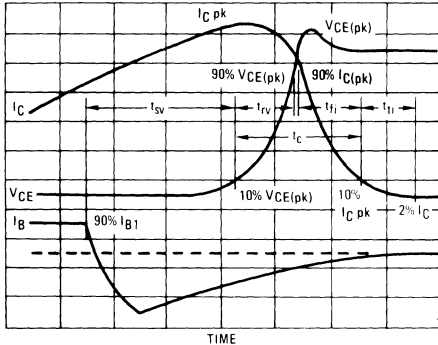
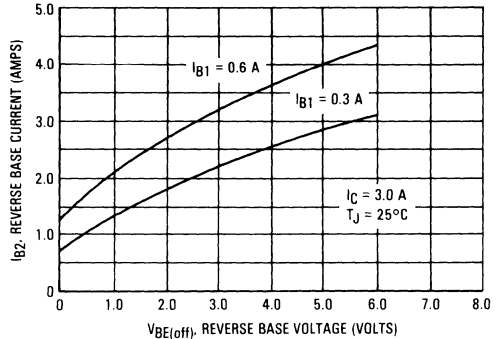


FIGURE 14 — PEAK REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

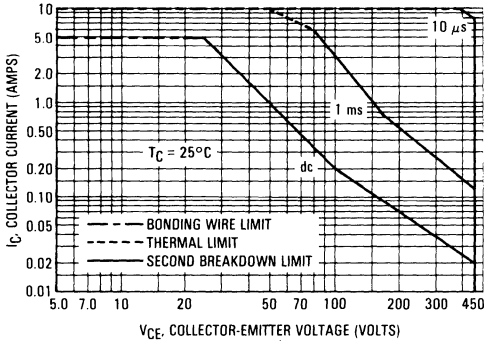
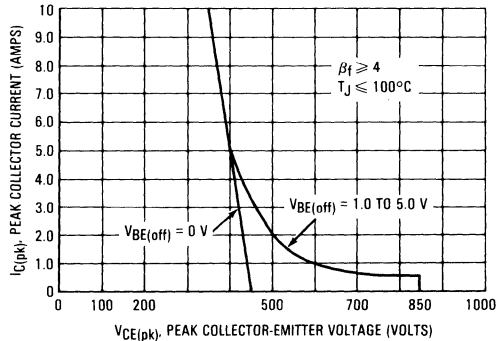


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25^\circ C$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_J(pk)$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce

the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

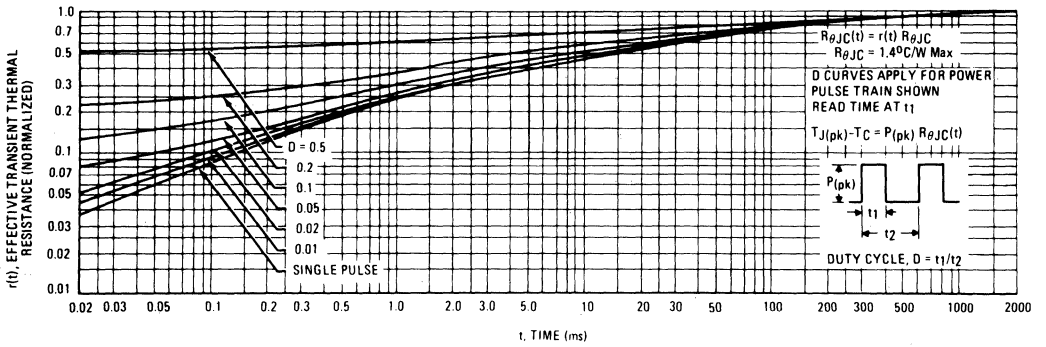


FIGURE 18 — POWER DERATING

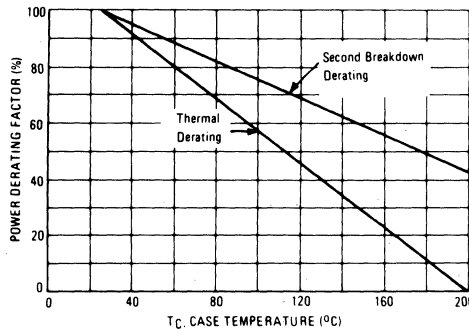
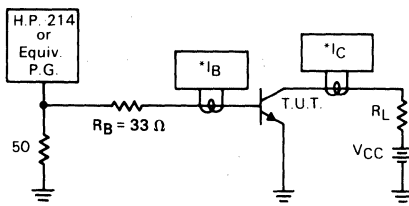
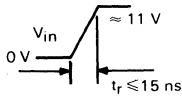


TABLE 1 — RESISTIVE LOAD SWITCHING

t_d and t_r

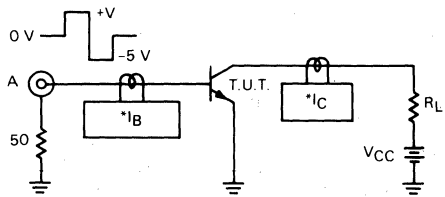
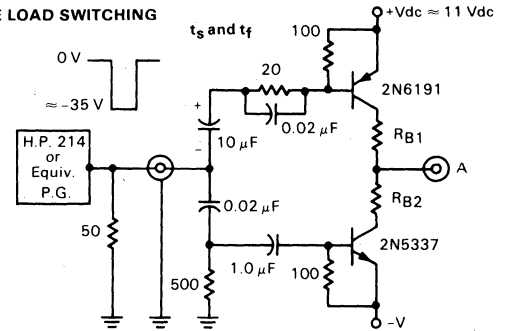


$V_{CC} = 250 \text{ Vdc}$
 $R_L = 83 \Omega$
 $I_C = 3.0 \text{ Adc}$
 $I_B = 0.3 \text{ Adc}$



*Tektronix P-6042 or Equivalent

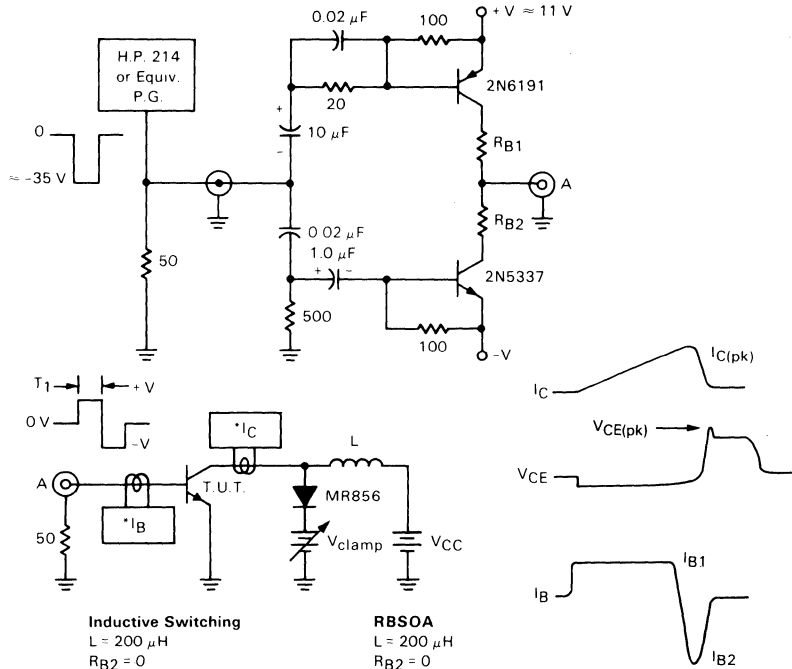
t_s and t_f



$V_{CC} = 250$
 $R_L = 83 \Omega$
 $I_C = 3.0 \text{ Adc}$
 $I_{B1} = 0.3 \text{ Adc}$
 $I_{B2} = 0.6 \text{ Adc}$
 $R_{B1} = 33 \Omega$
 $R_{B2} = 8.0 \Omega$
 For $V_{BE(\text{off})} = 5.0 \text{ V}$ $R_{B2} = 0 \Omega$

*Note: Adjust -V to obtain desired $V_{BE(\text{off})}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



$$T_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

VCE0(sus)
 $L = 10 \text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20 \text{ Volts}$

Inductive Switching
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

RBSOA
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

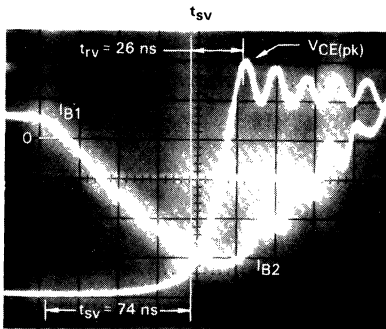
*Tektronix
 P-6042 or
 Equivalent

Scope - Tektronix
 7403 or
 Equivalent

Note: Adjust $-V$ to obtain desired $V_{BE(off)}$ at Point A.

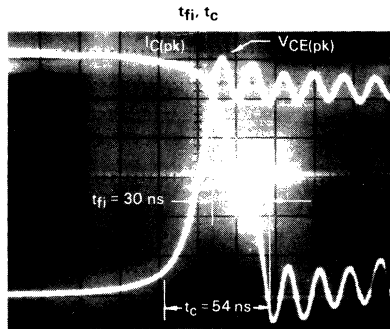


TYPICAL INDUCTIVE SWITCHING WAVEFORMS



$I_{C(pk)} = 3.0 \text{ Amps}$
 $I_{B1} = 0.3 \text{ Amp}$
 $V_{BE(off)} = 5.0 \text{ Volts}$
 $V_{CE(pk)} = 300 \text{ Volts}$
 $T_C = 25^\circ\text{C}$
 Time Base =
 20 ns/cm

$I_{C(pk)} = 3.0 \text{ Amps}$
 $I_{B1} = 0.3 \text{ Amp}$
 $V_{BE(off)} = 5.0 \text{ Volts}$
 $V_{CE(pk)} = 300 \text{ Volts}$
 $T_C = 25^\circ\text{C}$
 Time Base =
 20 ns/cm



Designer's Data Sheet
NPN Silicon Power Transistors
1 kV Switchmode III Series

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:

- Collector-Emitter Voltage — $V_{CEV} = 1000$ Vdc
- Fast Turn-Off Times
 100 ns Inductive Fall Time — 100°C (Typ)
 120 ns Inductive Crossover Time — 100°C (Typ)
 500 ns Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
 Reverse-Biased SOA with Inductive Load
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents
- Extended FBSOA Rating Using Ultra-fast Rectifiers
- Extremely High RBSOA Capability

MAXIMUM RATINGS

Rating	Symbol	MJ16002A	MJH16002A	Unit
Collector-Emitter Voltage	V_{CEO}	500		Vdc
Collector-Emitter Voltage	V_{CEV}	1000		Vdc
Emitter-Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous	I_C	5		Adc
Collector Current — Peak ⁽¹⁾	I_{CM}	10		
Base Current — Continuous	I_B	4		Adc
Base Current — Peak ⁽¹⁾	I_{BM}	8		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	125	100	Watts
@ $T_C = 100^\circ\text{C}$		71.5	40	
Derate above $T_C = 25^\circ\text{C}$		0.714	0.833	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	-55 to 150	°C

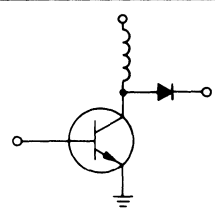
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.40	1.25	°C/W
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275		°C

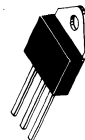
(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

POWER TRANSISTORS
5 AMPERES
500 VOLTS
125 and 100 WATTS



CASE 1-05
TO-204AA
MJ16002A



CASE 340-01
TO-218AC
MJH16002A

MJ16002A, MJH16002A

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)					
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	500	—	—	Vdc
Collector Cutoff Current (V _{CEV} = 1000 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = 1000 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	—	0.003 0.020	0.15 1.0	mAdc
Collector Cutoff Current (V _{CE} = 850 Vdc, R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	0.020	1.0	mAdc
Emitter Cutoff Current (V _{EB} = 6 Vdc, I _C = 0)	I _{EBO}	—	—	0.15	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figure 14a or 14b			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 15			

ON CHARACTERISTICS(1)

Collector-Emitter Saturation Voltage (I _C = 1.5 Adc, I _B = 0.2 Adc) (I _C = 3 Adc, I _B = 0.4 Adc) (I _C = 3 Adc, I _B = 0.4 Adc, T _C = 100°C)	V _{CE(sat)}	—	0.3 0.5 0.6	0.7 1 1.5	Vdc
Base-Emitter Saturation Voltage (I _C = 3 Adc, I _B = 0.4 Adc) (I _C = 3 Adc, I _B = 0.4 Adc, T _C = 100°C)	V _{BE(sat)}	—	1 1	1.5 1.5	Vdc
DC Current Gain (I _C = 5 Adc, V _{CE} = 5 Vdc)	h _{FE}	5	8	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1 kHz)	C _{ob}	—	—	200	pF
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SWITCHING CHARACTERISTICS

Inductive Load (Table 1)							
Storage Time	I _C = 3 Adc, I _{B1} = 0.4 Adc, V _{BE(off)} = 5 Vdc, V _{CE(pk)} = 400 Vdc	(T _J = 100°C)	t _{sv}	—	500	1600	ns
Fall Time			t _{fi}	—	100	200	
Crossover Time			t _c	—	120	250	
Storage Time		(T _J = 150°C)	t _{sv}	—	600	—	
Fall Time			t _{fi}	—	120	—	
Crossover Time			t _c	—	160	—	
Resistive Load (Table 2)							
Delay Time	I _C = 3 Adc, V _{CC} = 250 Vdc, I _{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ≤ 2%	(I _{B2} = 0.8 Adc, R _{B2} = 8 Ω)	t _d	—	30	100	ns
Rise Time			t _r	—	100	300	
Storage Time			t _s	—	1000	3000	
Fall Time		t _f	—	60	300		
Storage Time		(V _{BE(off)} = 5 Vdc)	t _s	—	400	—	
Fall Time			t _f	—	130	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

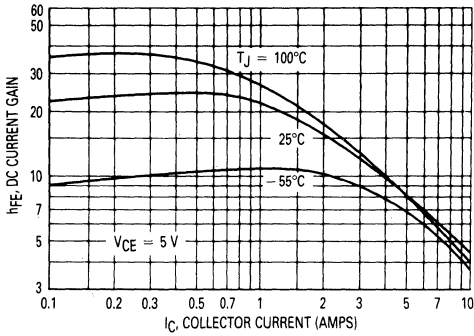


Figure 1. DC Current Gain

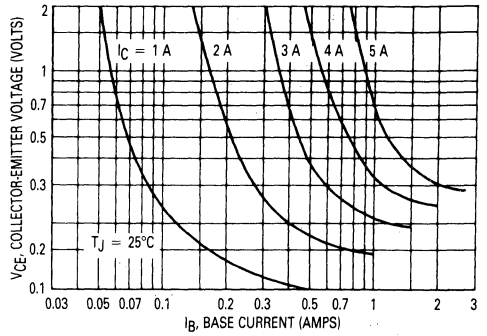


Figure 2. Collector Saturation Region

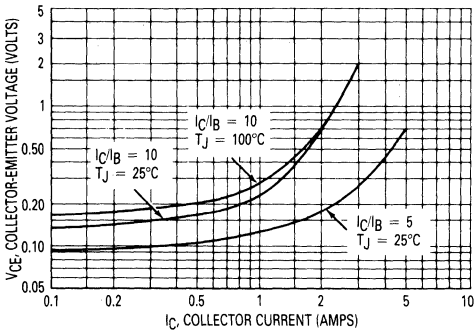


Figure 3. Collector-Emitter Saturation Region

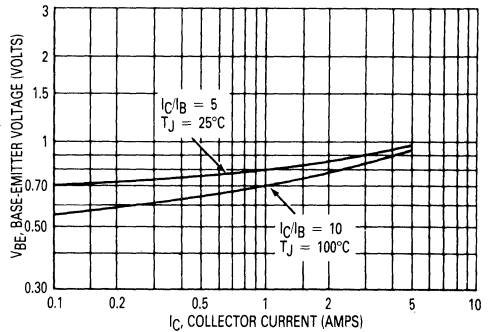


Figure 4. Base-Emitter Saturation Region

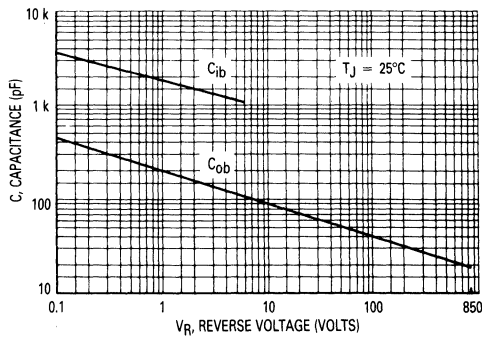


Figure 5. Capacitance

3

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

$I_C/I_{B1} = 5, T_C = 75^\circ\text{C}, V_{CE(pk)} = 400\text{ V}$

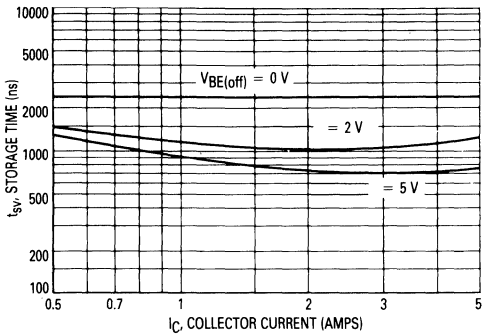


Figure 6. Storage Time

$I_C/I_{B1} = 10, T_C = 75^\circ\text{C}, V_{CE(pk)} = 400\text{ V}$

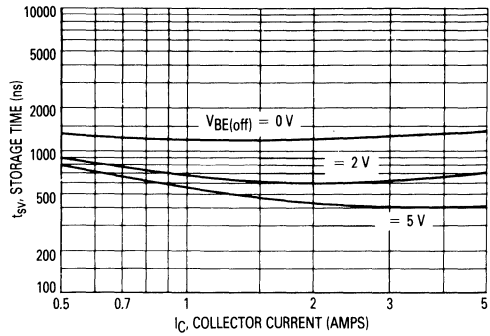


Figure 7. Storage Time

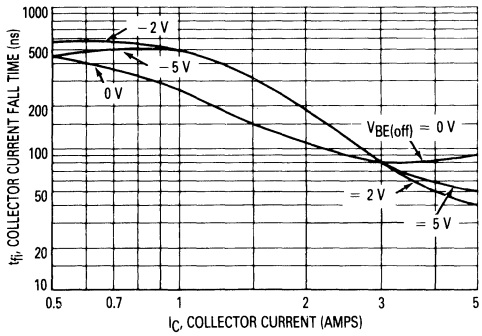


Figure 8. Collector Current Fall Time

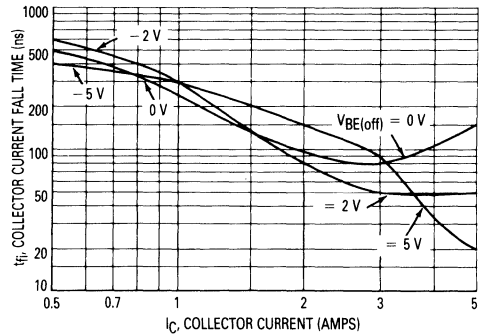


Figure 9. Collector Current Fall Time

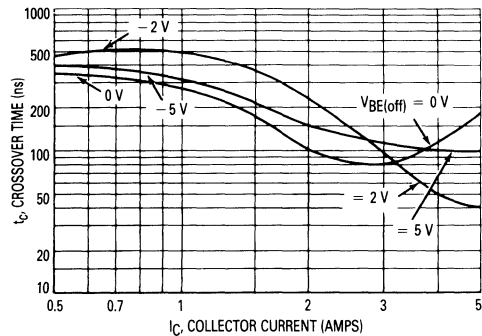


Figure 10. Crossover Time

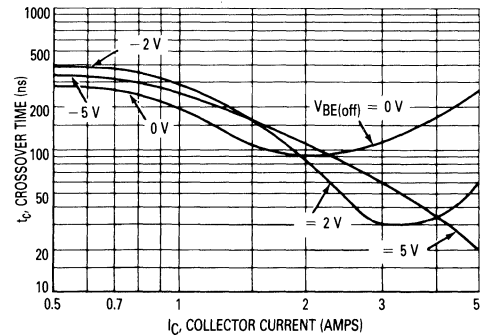
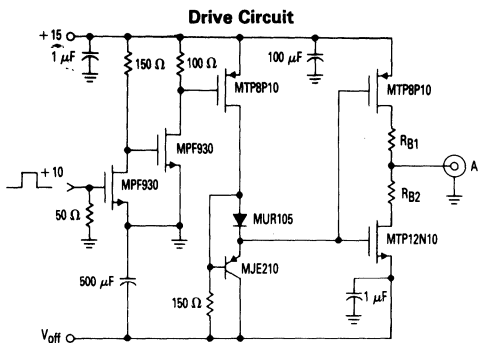


Figure 11. Crossover Time

Table 1. Inductive Load Switching



*Tektronix AM503
P6302 or Equivalent

Scope — Tektronix
7403 or Equivalent

$$T_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

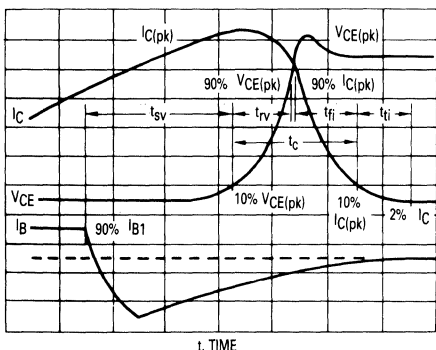


Figure 12. Inductive Switching Measurements

$V_{CE0(max)}$
 $L = 10 \text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20 \text{ Volts}$
 $I_{C(pk)} = 100 \text{ mA}$

Inductive Switching

$L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

RBSOA

$L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

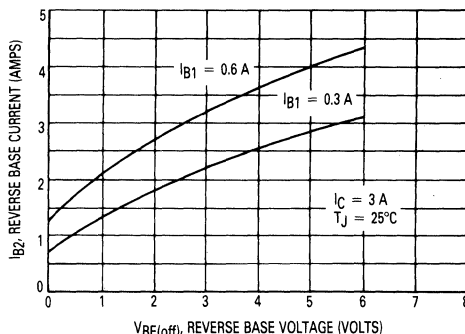
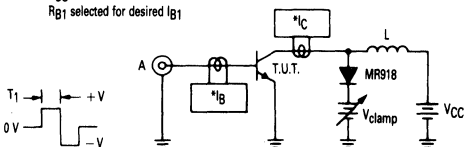
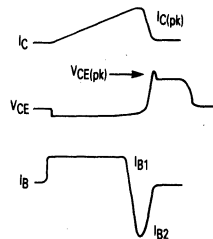
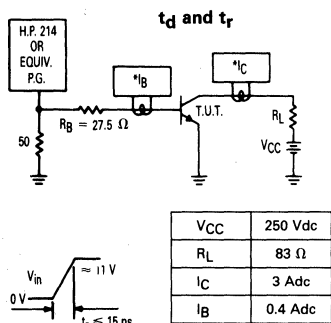


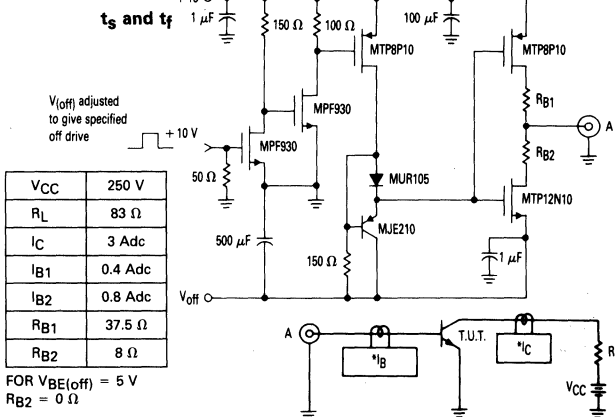
Figure 13. Peak Reverse Base Current

Table 2. Resistive Load Switching



*Tektronix AM503
P6302 or Equivalent

V_{CC}	250 Vdc
R_L	83 Ω
I_C	3 Adc
I_{B1}	0.4 Adc

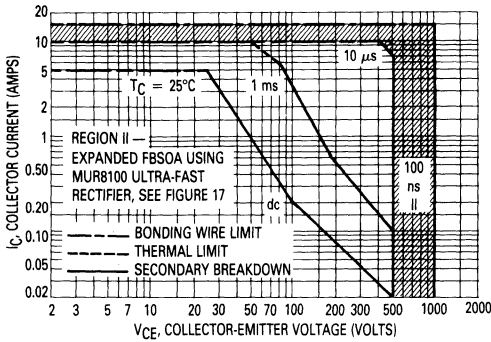


$V_{(off)}$ adjusted to give specified off drive

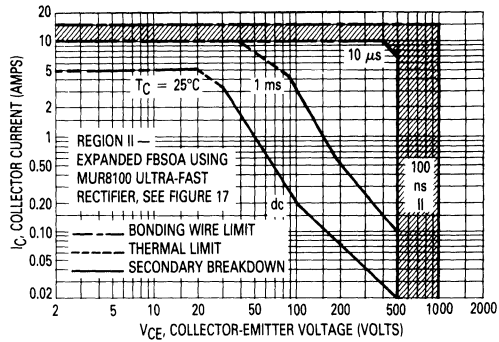
V_{CC}	250 V
R_L	83 Ω
I_C	3 Adc
I_{B1}	0.4 Adc
I_{B2}	0.8 Adc
R_{B1}	37.5 Ω
R_{B2}	8 Ω

FOR $V_{BE(off)} = 5 \text{ V}$
 $R_{B2} = 0 \Omega$

GUARANTEED OPERATING AREA INFORMATION



a. MJ16002A



b. MJH16002A

Figure 14. Maximum Rated Forward Biased Safe Operating Area

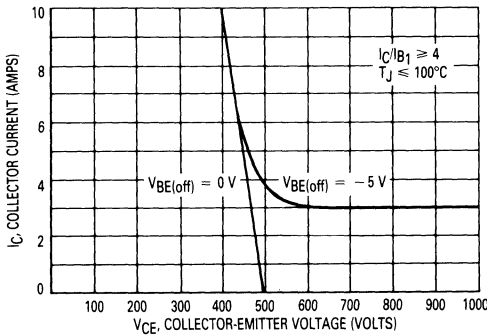


Figure 15. Maximum Reverse Biased Safe Operating Area

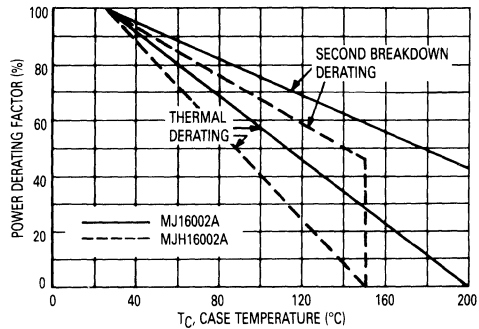


Figure 16. Power Derating

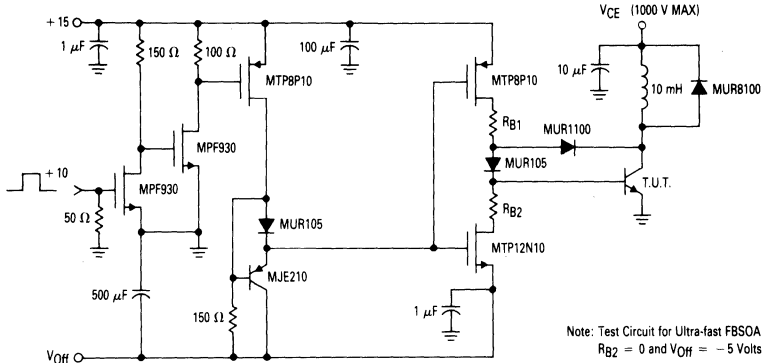


Figure 17. Switching Safe Operating Area

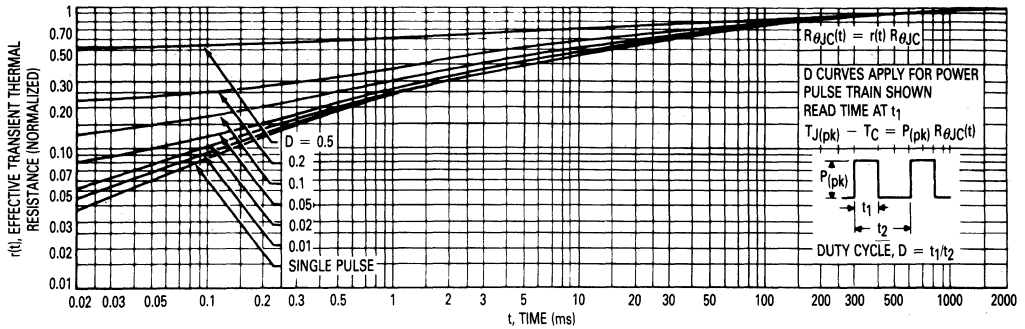


Figure 18. Thermal Response

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 14a or 14b is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 14a or 14b may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE III DESIGN CONSIDERATIONS

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector-emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{CE0(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN-ON —

Safe turn-on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra-fast recovery rectifiers, and are valid for turn-on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{CE0(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn-on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

3. TURN-OFF —

A bipolar transistor's ability to withstand turn-off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

3

SWITCHMODE III DESIGN CONSIDERATIONS (Cont.)

4. OPERATION ABOVE V(BR)CEO(sus) —

When bipolars are operated above collector-emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn-on, as a stiff negative bias is needed for safe turn-off. Any hiccup in the base-drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

5. RBSOA —

Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA

results in several types of circuits (see Application Note AN951).

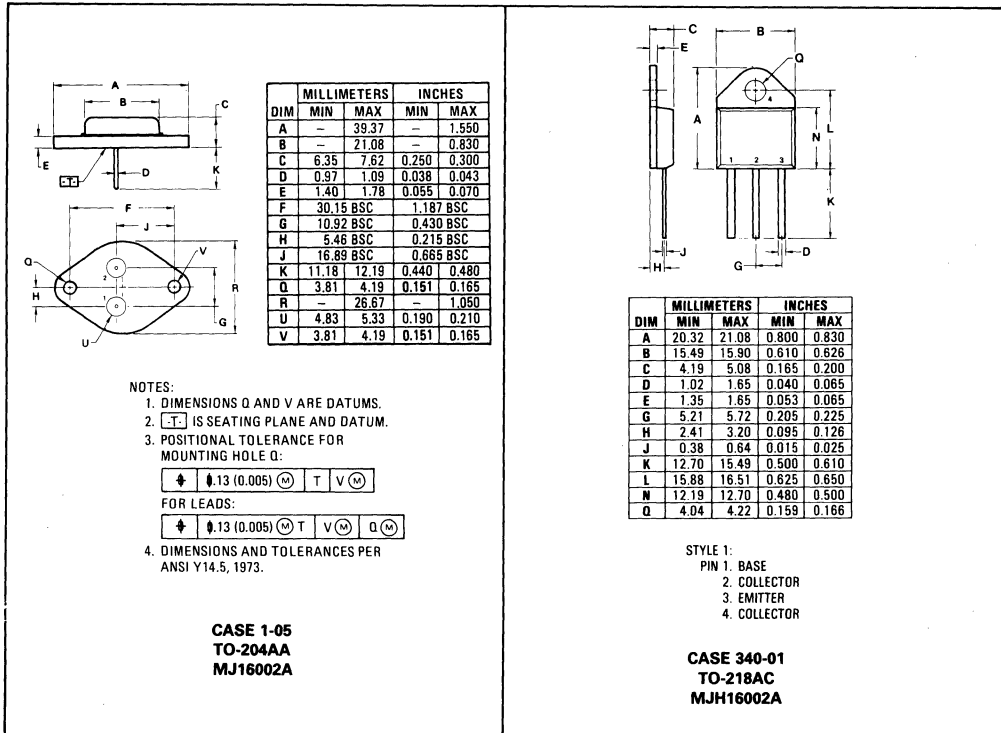
6. DESIGN SAMPLES —

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR4100 types are well-suited for higher drive requirements (see Article Reprint AR131).

OUTLINE DIMENSIONS



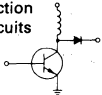
Designers Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16008 and MJH16008 are selected high gain versions of the MJ16006 and MJH16006 for applications where drive current is limited.

Typical Applications: Features:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 70 ns Inductive Fall Time - 100°C (Typ)
 - 100 ns Inductive Crossover Time - 100°C (Typ)
 - 500 ns Inductive Storage Time - 100°C (Typ)
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Load
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents



MAXIMUM RATINGS

Rating	Symbol	MJ16006 MJ16008	MJH16006 MJH16008	Unit
Collector-Emitter Voltage	V _{CEO}	450	450	Vdc
Collector-Emitter Voltage	V _{CEV}	850	850	Vdc
Emitter-Base Voltage	V _{EB}	6.0	6.0	Vdc
Collector Current				Adc
— Continuous	I _C	8.0	8.0	
— Peak (1)	I _{CM}	16	16	
Base Current				Adc
— Continuous	I _B	6.0	6.0	
— Peak (1)	I _{BM}	12	12	
Total Device Dissipation	P _D			Watts
@ T _C = 25°C		150	125	
@ T _C = 100°C		85.5	50	
Derate above 25°C		0.86	1.0	W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to 200	-55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.17	1.0 °C/W
Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds.	T _L	275	°C

(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.

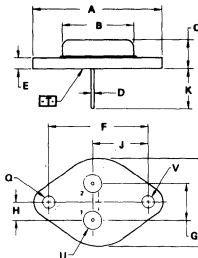
Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit Curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

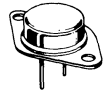
8.0 AMPERE

**NPN SILICON
POWER TRANSISTORS**

**450 VOLTS
125 AND 150 WATTS**



**MJ16006
MJ16008**



STYLE 1
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

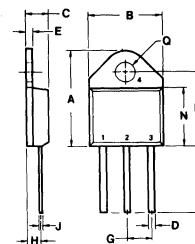
- NOTES:
 1. DIMENSIONS G AND V ARE DATUMS.
 2. [] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Ø.
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	39.37	1.550		
B	21.08	0.830		
C	6.35	7.62	0.250	0.300
D	0.31	1.08	0.010	0.043
E	1.40	1.78	0.055	0.070
F	30.15	1.187	BSC	
G	10.92	0.430	BSC	
H	5.46	0.215	BSC	
J	16.89	0.665	BSC	
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

± 13 (0.005) T V ⊕

FOR LEADS: ± 13 (0.005) T V ⊕ ⊕

**CASE 1-05
TO-204AA**



**MJH16006
MJH16008**



1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	29.32	21.08	0.900	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.125
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
D	4.04	4.22	0.158	0.168

**CASE 340-01
TO-218AC**

MJ16006, MJ16008, MJH16006, MJH16008

MJ16006 MJH16006

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit		
OFF CHARACTERISTICS (1)							
Collector-Emitter Sustaining Voltage (Table 2) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	450	—	—	Vdc		
Collector Cutoff Current (V _{CEV} = 850 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = 850 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	—	—	0.25 1.5	mAdc		
Collector Cutoff Current (V _{CE} = 850 Vdc, R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	—	2.5	mAdc		
Emitter Cutoff Current (V _{EB} = 6.0 Vdc, I _C = 0)	I _{EBO}	—	—	1.0	mAdc		
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figure 15					
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16					
ON CHARACTERISTICS (1)							
Collector-Emitter Saturation Voltage (I _C = 3.0 Adc, I _B = 0.4 Adc) (I _C = 5.0 Adc, I _B = 0.66 Adc) (I _C = 5.0 Adc, I _B = 0.66 Adc, T _C = 100°C)	V _{CE(sat)}	—	—	2.5 3.0 3.0	Vdc		
Base-Emitter Saturation Voltage (I _C = 5.0 Adc, I _B = 0.66 Adc) (I _C = 5.0 Adc, I _B = 0.66 Adc, T _C = 100°C)	V _{BE(sat)}	—	—	1.5 1.5	Vdc		
DC Current Gain (I _C = 8.0 Adc, V _{CE} = 5.0 Vdc)	h _{FE}	5.0	—	—	—		
DYNAMIC CHARACTERISTICS							
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1.0 kHz)	C _{ob}	—	—	350	pF		
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(I _C = 5.0 Adc, V _{CC} = 250 Vdc, I _{B1} = 0.66 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I _{B2} = 1.3 Adc, R _{B2} = 4.0 Ω)	t _d	—	20	50	ns
Rise Time			t _r	—	85	250	
Storage Time			t _s	—	1000	2500	
Fall Time			t _f	—	70	250	
Storage Time			t _s	—	500	—	
Fall Time			t _f	—	100	—	
Inductive Load (Table 2)							
Storage Time	(I _C = 5.0 Adc, I _{B1} = 0.66 Adc, V _{BE(off)} = 5.0 Vdc, V _{CE(pk)} = 400 Vdc)	(T _J = 100°C)	t _{sv}	—	700	1800	ns
Fall Time			t _{fi}	—	80	200	
Crossover Time			t _c	—	150	250	
Storage Time			t _{sv}	—	800	—	
Fall Time			t _{fi}	—	80	—	
Crossover Time			t _c	—	200	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

MJ16006, MJ16008, MJH16006, MJH16008

MJ16008 MJH16008

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	450	—	—	Vdc
Collector Cutoff Current (V _{CEV} = 850 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = 850 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current (V _{CE} = 850 Vdc, R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V _{EB} = 6.0 Vdc, I _C = 0)	I _{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage (I _C = 3.0 Adc, I _B = 0.3 Adc) (I _C = 5.0 Adc, I _B = 0.5 Adc) (I _C = 5.0 Adc, I _B = 0.5 Adc, T _C = 100°C)	V _{CE(sat)}	—	—	2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage (I _C = 5.0 Adc, I _B = 0.5 Adc) (I _C = 5.0 Adc, I _B = 0.5 Adc, T _C = 100°C)	V _{BE(sat)}	—	—	1.5 1.5	Vdc
DC Current Gain (I _C = 8.0 Adc, V _{CE} = 5.0 Vdc)	h _{FE}	7.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1.0 kHz)	C _{ob}	—	—	350	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	(I _C = 5.0 Adc, V _{CC} = 250 Vdc, I _{B1} = 0.5 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I _{B2} = 1.0 Adc, R _{B2} = 4.0 Ω)	t _d	—	20	50	ns
Rise Time			t _r	—	100	250	
Storage Time			t _s	—	900	2200	
Fall Time		t _f	—	70	250		
Storage Time		t _s	—	400	—		
Fall Time		t _f	—	50	—		
Inductive Load (Table 2)							
Storage Time	(I _C = 5.0 Adc, I _{B1} = 0.5 Adc, V _{BE(off)} = 5.0 Vdc, V _{CE(pk)} = 400 Vdc)	(T _J = 100°C)	t _{sv}	—	500	1400	ns
Fall Time			t _{fi}	—	70	150	
Crossover Time			t _c	—	100	200	
Storage Time		t _{sv}	—	600	—		
Fall Time		t _{fi}	—	100	—		
Crossover Time		t _c	—	150	—		

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

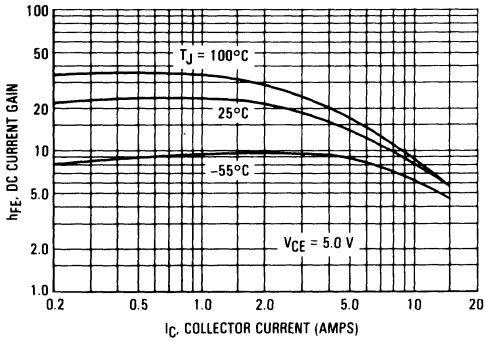


FIGURE 2 — COLLECTOR SATURATION REGION

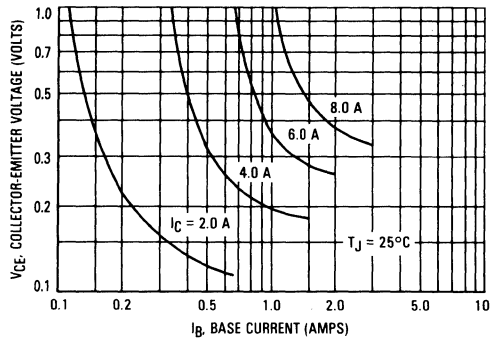


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

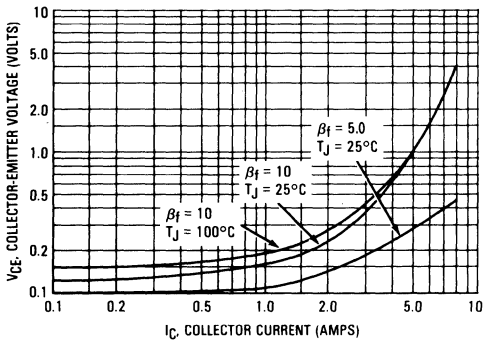


FIGURE 4 — BASE-EMITTER VOLTAGE

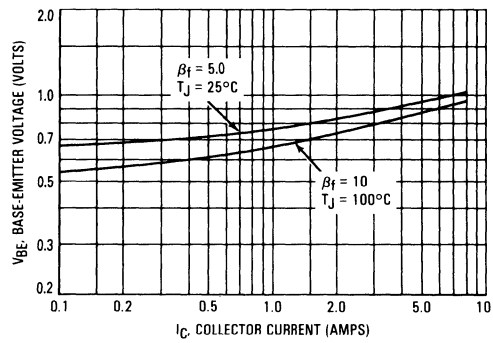


FIGURE 5 — COLLECTOR CUTOFF REGION

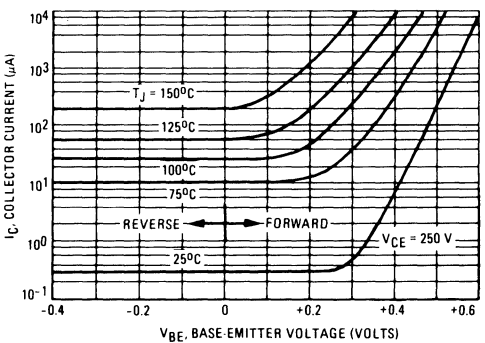
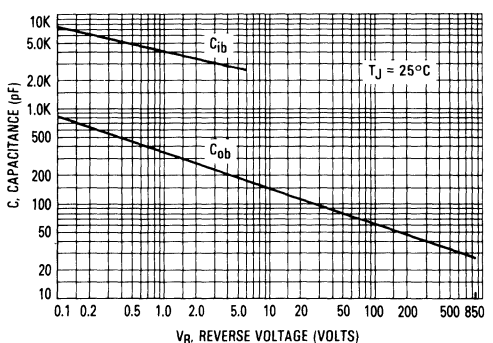


FIGURE 6 — CAPACITANCE



TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

FIGURE 7 — STORAGE TIME

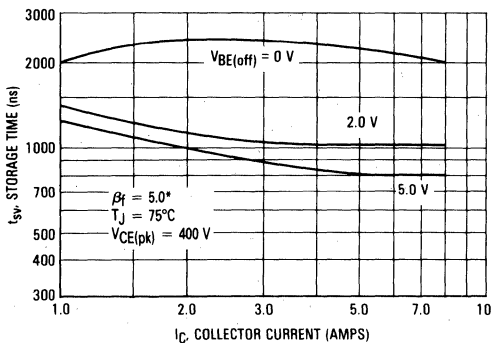


FIGURE 8 — STORAGE TIME

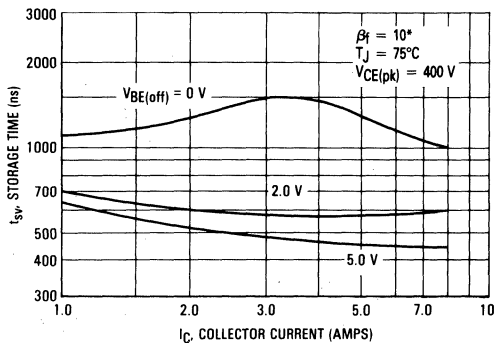


FIGURE 9 — COLLECTOR CURRENT FALL TIME

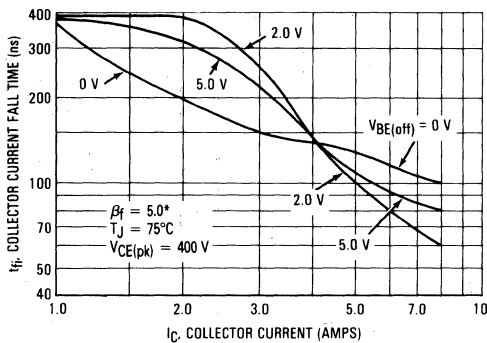


FIGURE 10 — COLLECTOR CURRENT FALL TIME

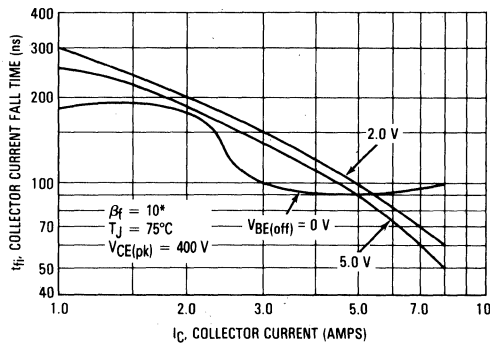


FIGURE 11 — CROSSOVER TIME

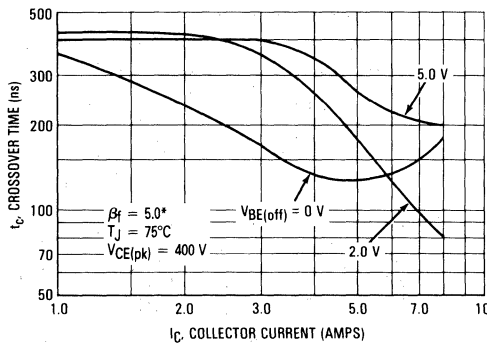
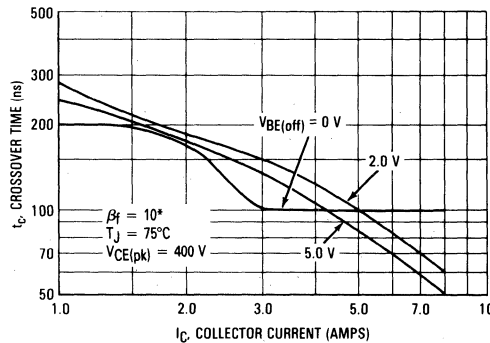


FIGURE 12 — CROSSOVER TIME



$^* \beta_f = \frac{I_C}{I_{B1}}$

3

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

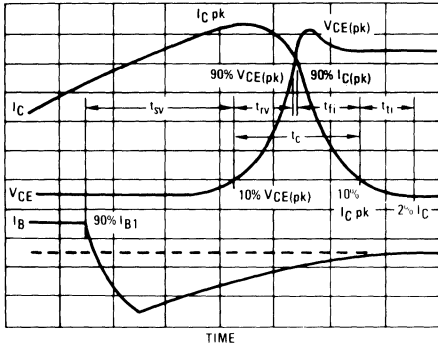


FIGURE 14 — PEAK REVERSE BASE CURRENT

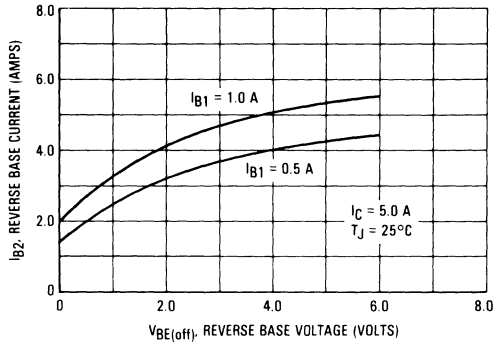
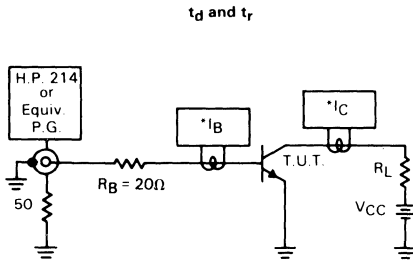
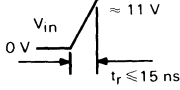


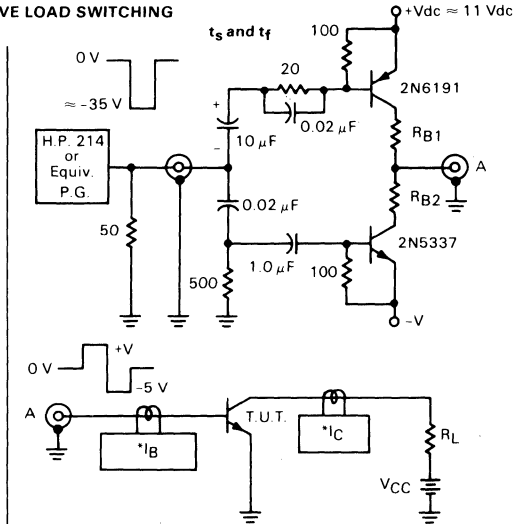
TABLE 1 — RESISTIVE LOAD SWITCHING



$V_{CC} = 250 \text{ Vdc}$
 $R_L = 50 \Omega$
 $I_C = 5.0 \text{ Adc}$
 $I_B = 0.5 \text{ Adc}$



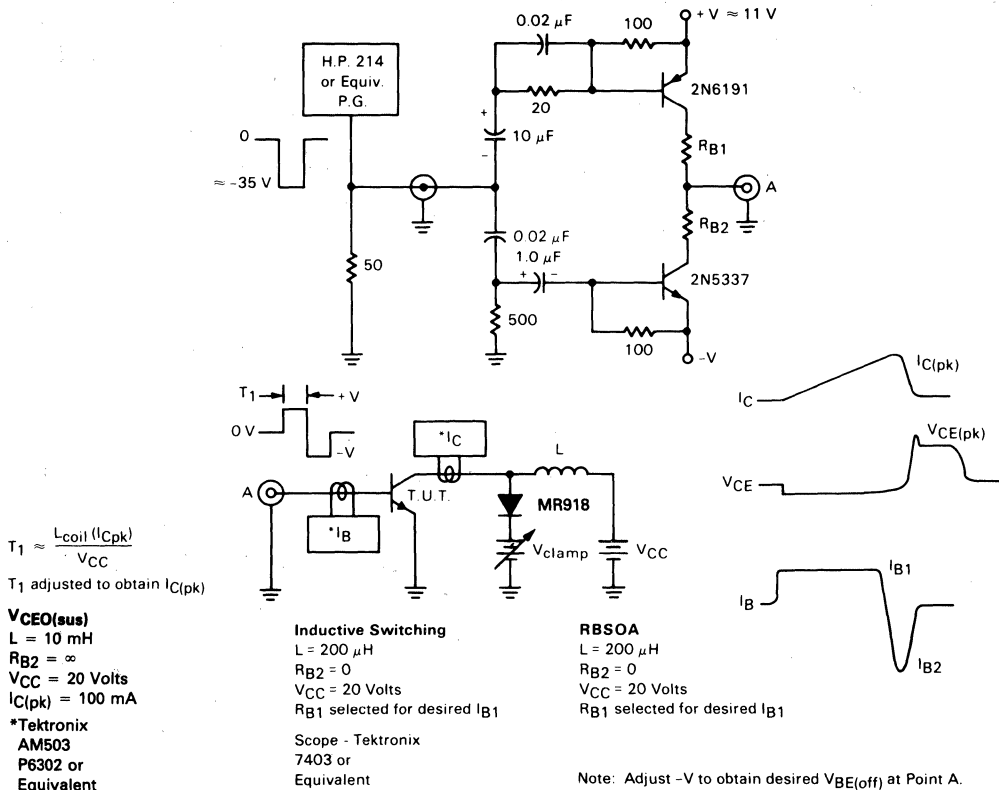
*Tektronix
 AM503
 P6302 or
 Equivalent



$V_{CC} = 250$
 $R_L = 50 \Omega$
 $I_C = 5.0 \text{ Adc}$
 $I_{B1} = 0.5 \text{ Adc}$
 $I_{B2} = 1.0 \text{ Adc}$
 For $V_{BE(off)} = 5.0 \text{ V}$ $R_{B2} = 0 \Omega$

Note: Adjust $-V$ to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 and 15A are based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 and 15A may be found at any case temperature by using the appropriate curve on Figure 17.

$T_J(pk)$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will re-

duce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA, MJ16006 & MJ16008

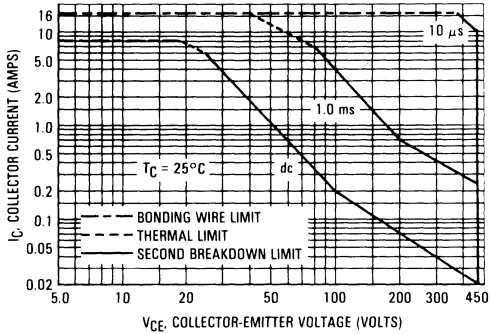


FIGURE 15A — SAFE OPERATING AREA, MJH16006 & MJH16008

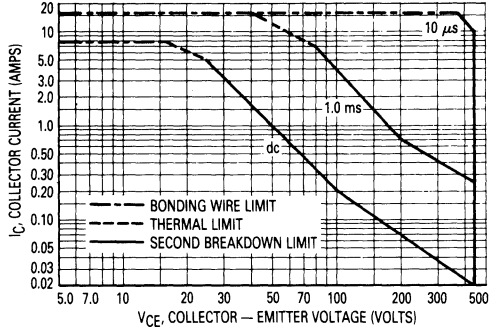


FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA

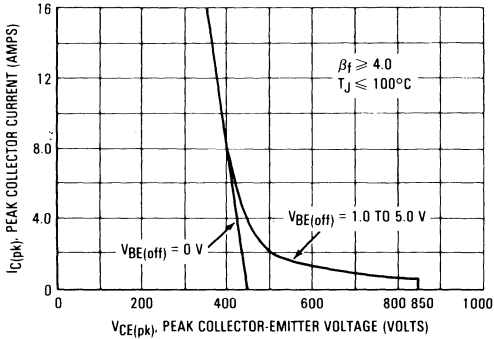


FIGURE 17 — POWER DERATING

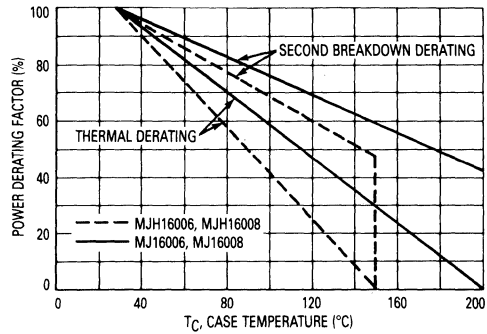
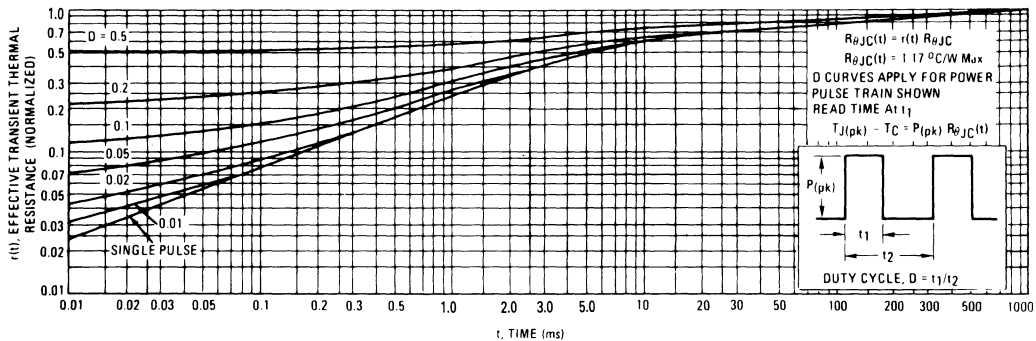


FIGURE 18 — THERMAL RESPONSE



Designer's Data Sheet
NPN Silicon Power Transistors
1 kV Switchmode III Series

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

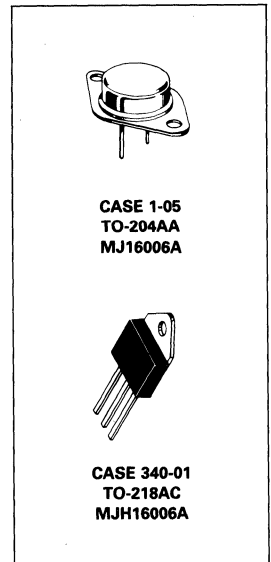
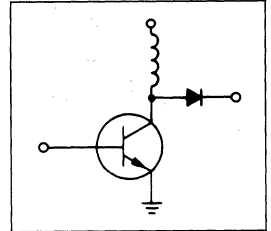
Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:

- Collector-Emitter Voltage — $V_{CEV} = 1000$ Vdc
- Fast Turn-Off Times
 - 80 ns Inductive Fall Time — 100°C (Typ)
 - 120 ns Inductive Crossover Time — 100°C (Typ)
 - 800 ns Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Load
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents
- Extended FBSOA Rating Using Ultra-fast Rectifiers
- Extremely High RBSOA Capability

POWER TRANSISTORS
8 AMPERES
500 VOLTS
125 and 150 WATTS



MAXIMUM RATINGS

Rating	Symbol	MJ16006A	MJH16006A	Unit
Collector-Emitter Voltage	V_{CEO}	500		Vdc
Collector-Emitter Voltage	V_{CEV}	1000		Vdc
Emitter-Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous	I_C	8		Adc
— Peak ⁽¹⁾	I_{CM}	16		
Base Current — Continuous	I_B	6		Adc
— Peak ⁽¹⁾	I_{BM}	12		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	125	Watts
@ $T_C = 100^\circ\text{C}$		85	50	
Derate above $T_C = 25^\circ\text{C}$		0.86	1	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	-55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	1	°C/W
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MJ16006A, MJH16006A

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)					
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	500	—	—	Vdc
Collector Cutoff Current (V _{CEV} = 1000 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = 1000 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	— —	0.003 0.020	0.15 1.0	mAdc
Collector Cutoff Current (V _{CE} = 1000 Vdc, R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	0.020	1.0	mAdc
Emitter Cutoff Current (V _{EB} = 6 Vdc, I _C = 0)	I _{EBO}	—	0.005	0.15	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figure 14a or 14b			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 15			

ON CHARACTERISTICS(1)

Collector-Emitter Saturation Voltage (I _C = 3 Adc, I _B = 0.6 Adc) (I _C = 5 Adc, I _B = 1 Adc) (I _C = 5 Adc, I _B = 1 Adc, T _C = 100°C)	V _{CE(sat)}	— — —	0.35 0.50 0.60	0.7 1 1.5	Vdc
Base-Emitter Saturation Voltage (I _C = 5 Adc, I _B = 1 Adc) (I _C = 5 Adc, I _B = 1 Adc, T _C = 100°C)	V _{BE(sat)}	— —	1 1	1.5 1.5	Vdc
DC Current Gain (I _C = 8 Adc, V _{CE} = 5 Vdc)	h _{FE}	5	8	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1 kHz)	C _{ob}	—	—	350	pF
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SWITCHING CHARACTERISTICS

Inductive Load (Table 1)							
Storage Time	(I _C = 5 Adc, I _{B1} = 0.66 Adc, V _{BE(off)} = 5 Vdc, V _{CE(pk)} = 400 Vdc)	(T _J = 100°C)	t _{sv}	—	800	2000	ns
Fall Time			t _{fi}	—	80	200	
Crossover Time			t _c	—	120	300	
Storage Time		(T _J = 150°C)	t _{sv}	—	1000	—	
Fall Time			t _{fi}	—	90	—	
Crossover Time			t _c	—	150	—	
Resistive Load (Table 2)							
Delay Time	(I _C = 5 Adc, V _{CC} = 250 Vdc, I _{B1} = 0.66 Adc, PW = 30 μs, Duty Cycle ≤ 2%)	(I _{B2} = 1.3 Adc, R _{B2} = 4 Ω)	t _d	—	25	100	ns
Rise Time			t _r	—	400	700	
Storage Time			t _s	—	1400	3000	
Fall Time		t _f	—	175	400		
Storage Time		(V _{BE(off)} = 5 Vdc)	t _s	—	475	—	
Fall Time			t _f	—	100	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

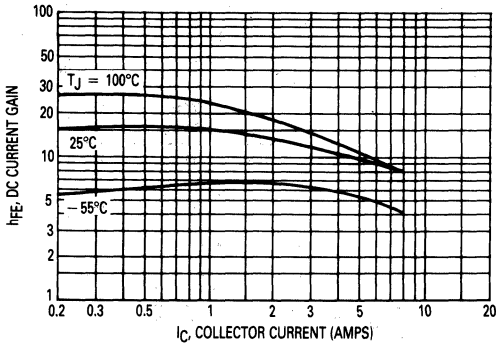


Figure 1. DC Current Gain

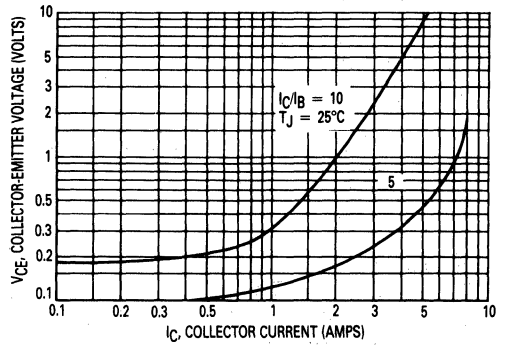


Figure 2. Collector-Emitter Saturation Region

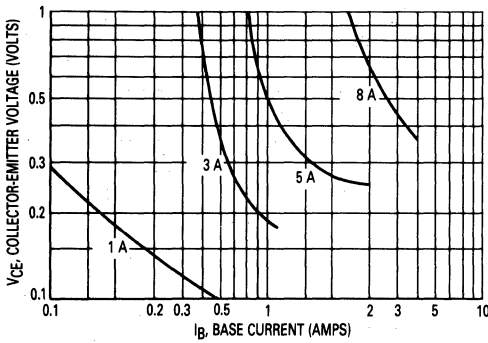


Figure 3. Collector-Emitter Saturation Region

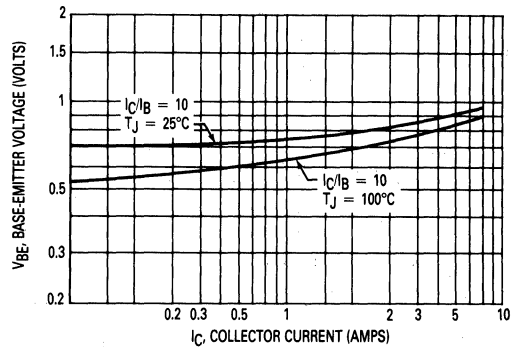


Figure 4. Base-Emitter Saturation Region

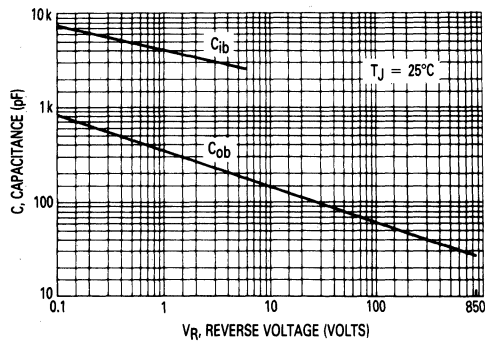


Figure 5. Capacitance

3

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

$I_C/I_{B1} = 5, T_C = 75^\circ\text{C}, V_{CE(pk)} = 400\text{ V}$

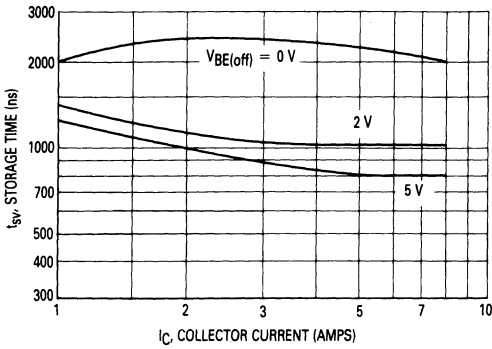


Figure 6. Storage Time

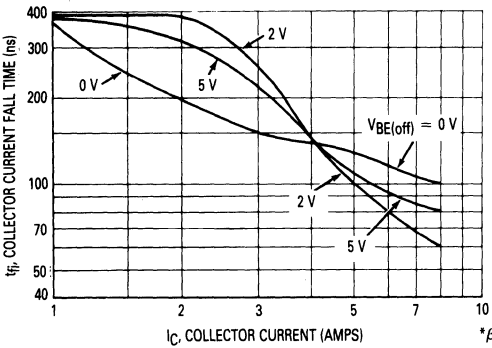


Figure 8. Collector Current Fall Time

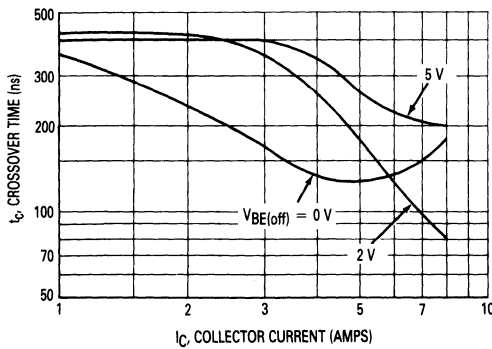


Figure 10. Crossover Time

$I_C/I_{B1} = 10, T_C = 75^\circ\text{C}, V_{CE(pk)} = 400\text{ V}$

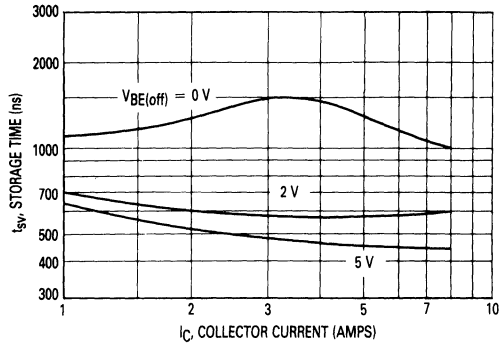


Figure 7. Storage Time

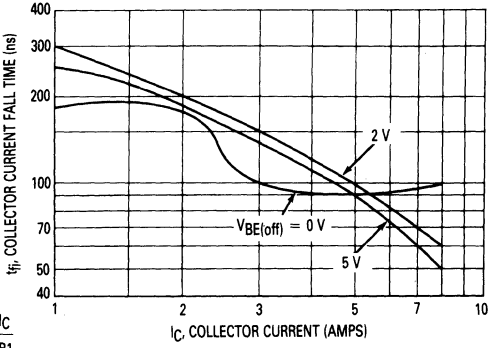


Figure 9. Collector Current Fall Time

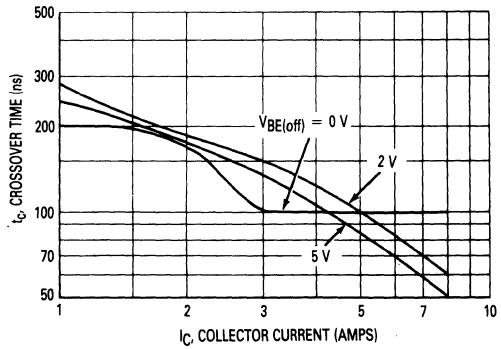
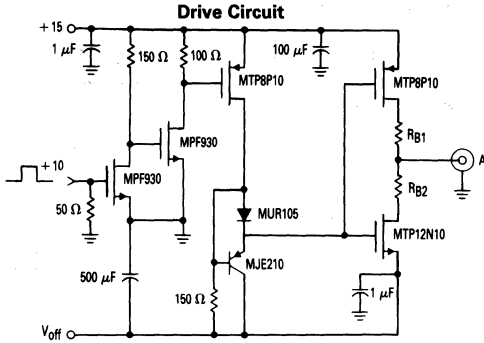


Figure 11. Crossover Time



Table 1. Inductive Load Switching



*Tektronix AM503
P6302 or Equivalent

Scope — Tektronix
7403 or Equivalent

$$T_1 \approx \frac{L_{coil} (I_{C(pk)})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

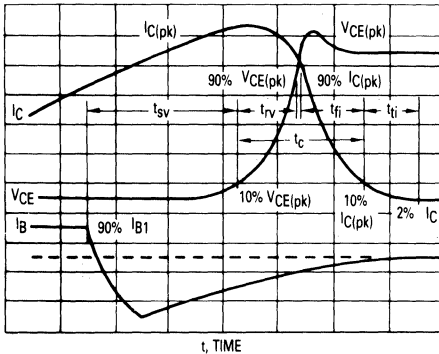


Figure 12. Inductive Switching Measurements

$V_{CE(oss)}$
 $L = 10 \text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20 \text{ Volts}$

Inductive Switching

$L = 750 \text{ } \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

RBSOA

$L = 750 \text{ } \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

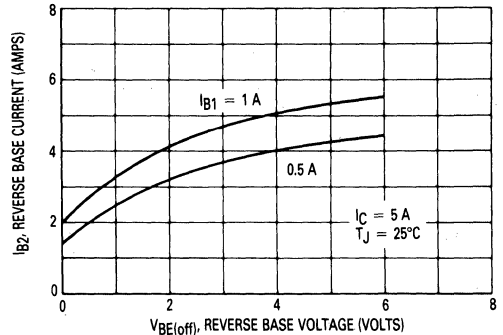
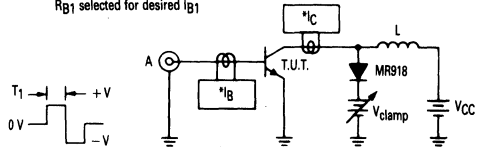
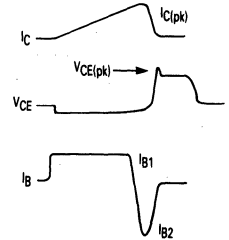
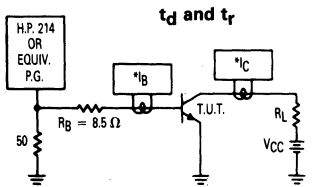


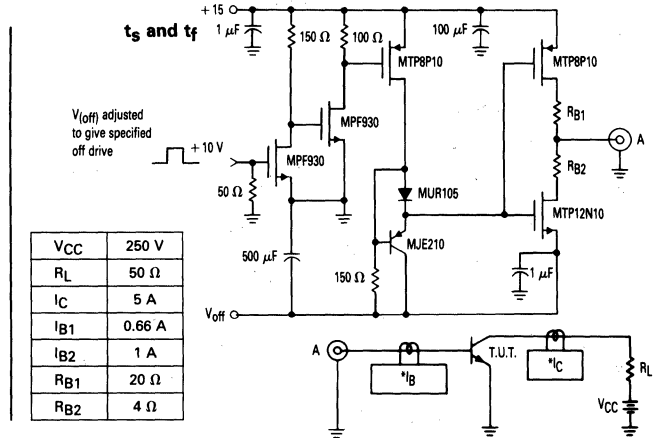
Figure 13. Peak Reverse Base Current

Table 2. Resistive Load Switching



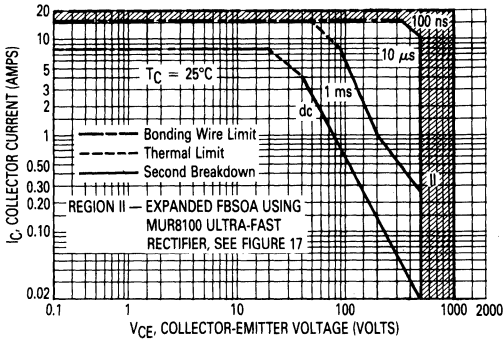
V_{CC}	250 V
R_L	50 Ω
I_C	5 A
I_B	0.66 A

*Tektronix AM503
P6302 or Equivalent

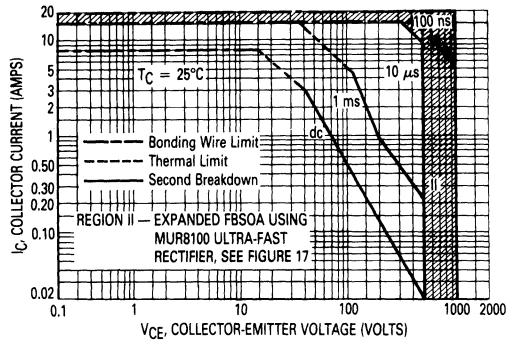


V_{CC}	250 V
R_L	50 Ω
I_C	5 A
I_{B1}	0.66 A
I_{B2}	1 A
R_{B1}	20 Ω
R_{B2}	4 Ω

GUARANTEED SAFE OPERATING AREA LIMITS



a. MJ16006A



b. MJH16006A

Figure 14. Maximum Rated Forward Biased Safe Operating Area

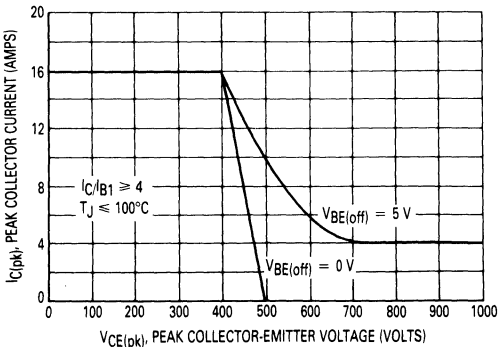


Figure 15. Maximum Reverse Biased Safe Operating Area

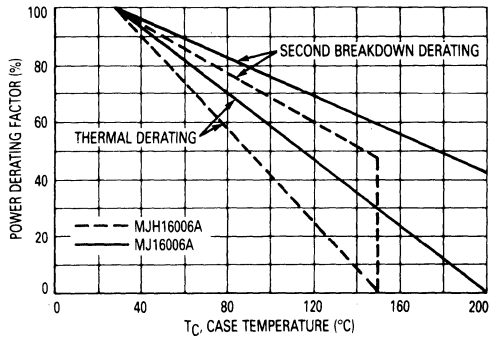
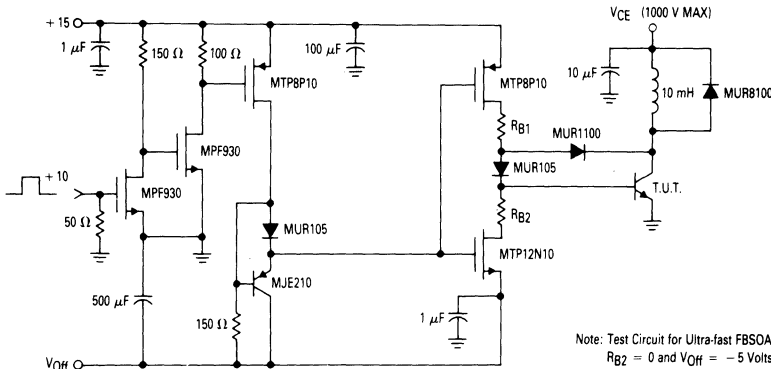


Figure 16. Power Derating



Note: Test Circuit for Ultra-fast FBSOA
R_{B2} = 0 and V_{OH} = -5 Volts

Figure 17. Switching Safe Operating Area

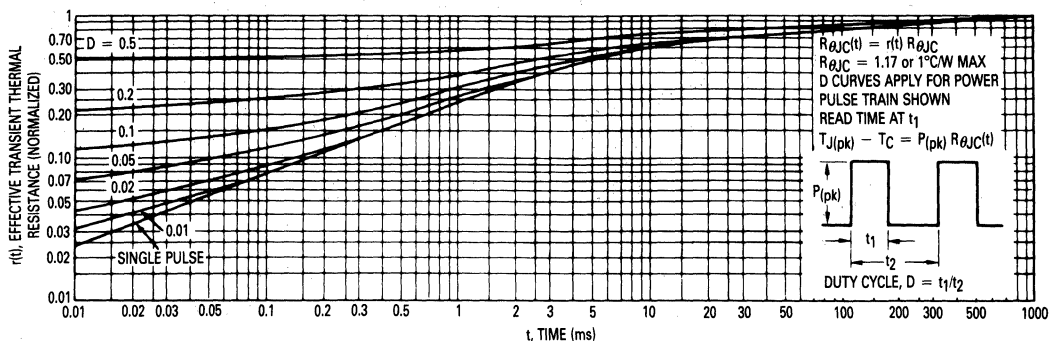


Figure 18. Thermal Response

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 14a and 14b is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 14a and 14b may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE III DESIGN CONSIDERATIONS

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector-emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{CE(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN-ON —

Safe turn-on load line excursions are bounded by pulsed FBSOA curves. The $10\ \mu\text{s}$ curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra-fast recovery rectifiers, and are valid for turn-on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{CE(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn-on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

3. TURN-OFF —

A bipolar transistor's ability to withstand turn-off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

3

SWITCHMODE III DESIGN CONSIDERATIONS (Cont.)

4. OPERATION ABOVE $V_{CEO(sus)}$ —

When bipolars are operated above collector-emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn-on, as is a stiff negative bias needed for safe turn-off. Any hiccup in the base-drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

5. RBSOA —

Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only

for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

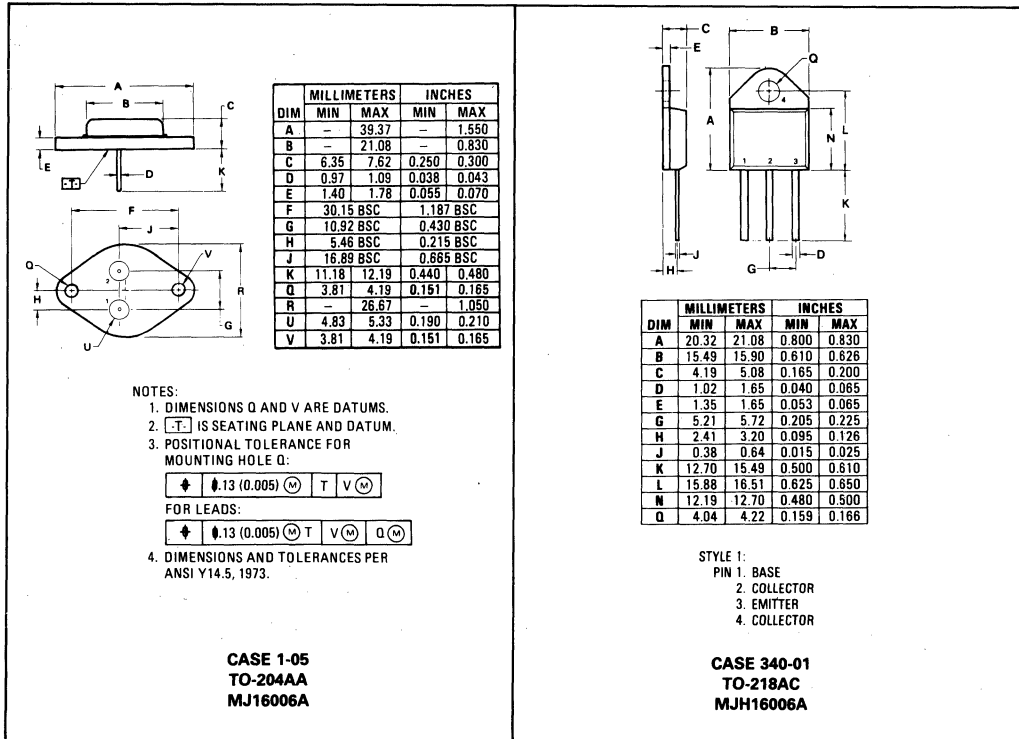
6. DESIGN SAMPLES —

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR4100 types are well-suited for higher drive requirements (see Article Reprint AR131).

OUTLINE DIMENSIONS



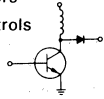
Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16012 and MJH16012 are selected high gain versions of the MJ16010 and MJH16010 for applications where drive current is limited.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits



Features:

- Fast Turn-Off Times — $T_C = 100^\circ\text{C}$
 50 ns Inductive Fall Time (Typ)
 90 ns Inductive Crossover Time (Typ)
 800 ns Inductive Storage Time (Typ)
- 100°C Performance Specified for:
 Reverse-Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents

MAXIMUM RATINGS

Rating	Symbol	MJ16010 MJ16012	MJH16010 MJH16012	Unit
Collector-Emitter Voltage	V_{CEO}	450		Vdc
Collector-Emitter Voltage	V_{CEV}	850		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	15		Adc
— Peak (1)	I_{CM}	20		Adc
Base Current — Continuous	I_B	10		Adc
— Peak (1)	I_{BM}	15		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$ Derate above 25°C	P_D	175 100 1.0	135 53.8 1.11	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	0.93	$^\circ\text{C}/\text{W}$
Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	T_L	275		$^\circ\text{C}$

(1) Pulse Test: Pulse Width $\leq 5.0 \mu\text{s}$, Duty Cycle $\geq 10\%$.

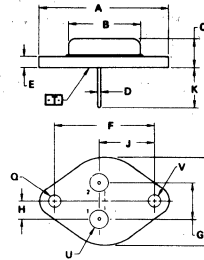
Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

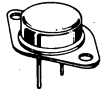
15 AMPERE

NPN SILICON
POWER TRANSISTORS

450 VOLTS
135 AND 175 WATTS



MJ16010
MJ16012

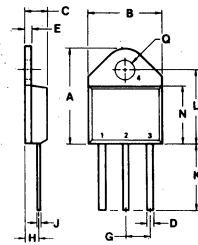


STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

- NOTES:
 1. DIMENSIONS Q AND V ARE DATUMS.
 2. [T] IS SEATING PLANE AND DATUM.
 3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
 Ⓢ ±0.13 (0.005) Ⓢ T V Ⓢ
 FOR LEADS:
 Ⓢ ±0.13 (0.005) Ⓢ T V Ⓢ Ⓢ
 4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	35.37	—	1.550	—
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC	1.187 BSC	—	—
G	10.92 BSC	0.430 BSC	—	—
H	5.48 BSC	0.215 BSC	—	—
J	16.89 BSC	0.665 BSC	—	—
K	11.18	12.19	0.440	0.480
L	3.81	4.19	0.151	0.165
M	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

CASE 1-05
TO-204AA



MJH16010
MJH16012



1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	2.20	0.095	0.176
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	15.51	0.625	0.650
M	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

MJ16010, MJ16012, MJH16010, MJH16012

MJ16010 MJH16010

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.7\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.3\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.3\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.3\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.3\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain ($I_C = 15\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	5.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	400	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	
Delay Time	$(I_C = 10\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 1.3\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	$(I_{B2} = 2.6\text{ Adc}$, $R_B = 1.6\ \Omega$)	t_d	—	20	—	ns
Rise Time			t_r	—	200	—	
Storage Time	$(V_{BE(off)} = 5.0\text{ Vdc})$	t_s	—	1200	—		
Fall Time		t_f	—	200	—		
Storage Time		t_s	—	650	—		
Fall Time		t_f	—	80	—		

Inductive Load (Table 2)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	
Storage Time	$(I_C = 10\text{ Adc}$, $I_{B1} = 1.3\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	$(T_C = 100^\circ\text{C})$	t_{sv}	—	800	1800	ns
Fall Time			t_{fi}	—	50	200	
Crossover Time	$(T_C = 150^\circ\text{C})$	t_c	—	90	250		
Storage Time		t_{sv}	—	1050	—		
Fall Time		t_{fi}	—	70	—		
Crossover Time		t_c	—	120	—		

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.

MJ16012
MJH16012

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.5 1.5	Vdc
DC Current Gain ($I_C = 15\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	400	pF
--	----------	---	---	-----	----

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	$(I_C = 10\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 1.0\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	$(I_{B2} = 2.0\text{ Adc}$, $R_B = 1.6\ \Omega$)	t_d	—	20	—	ns
Rise Time			t_r	—	200	—	
Storage Time			t_s	—	900	—	
Fall Time			t_f	—	150	—	
Storage Time			t_{sv}	—	500	—	
Fall Time			t_{fv}	—	40	—	

Inductive Load (Table 2)

Storage Time	$(I_C = 10\text{ Adc}$, $I_{B1} = 1.0\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$)	$(T_C = 100^\circ\text{C})$	t_{sv}	—	650	1500	ns
Fall Time			t_{fi}	—	30	150	
Crossover Time			t_c	—	50	200	
Storage Time			t_{sv}	—	850	—	
Fall Time			t_{fi}	—	30	—	
Crossover Time			t_c	—	70	—	

(1) Pulse Test: Pulse Width = $300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

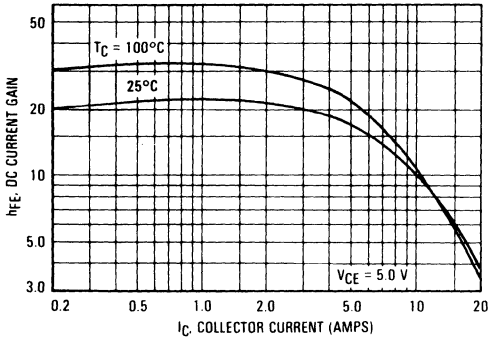


FIGURE 2 — COLLECTOR SATURATION REGION

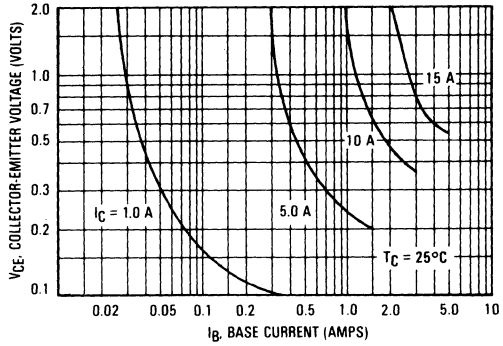


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

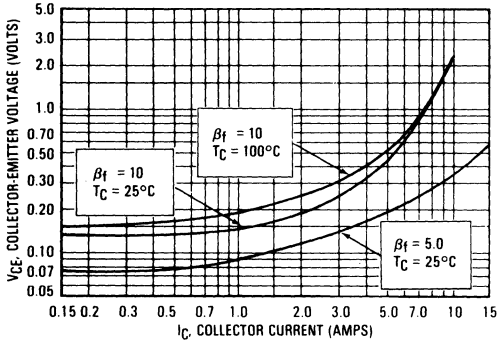


FIGURE 4 — BASE-EMITTER VOLTAGE

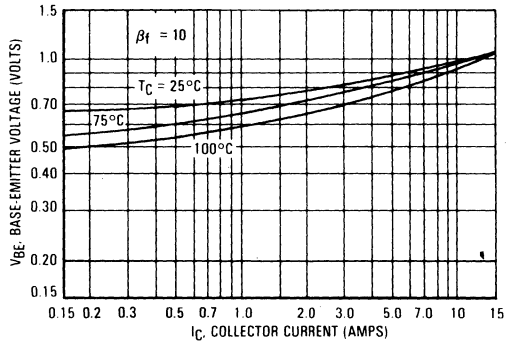


FIGURE 5 — COLLECTOR CUTOFF REGION

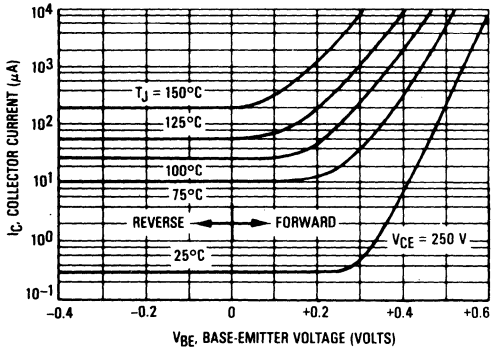
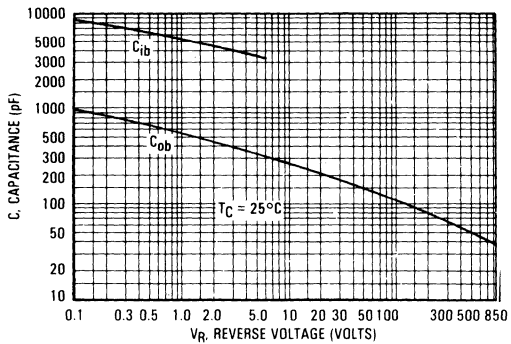


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

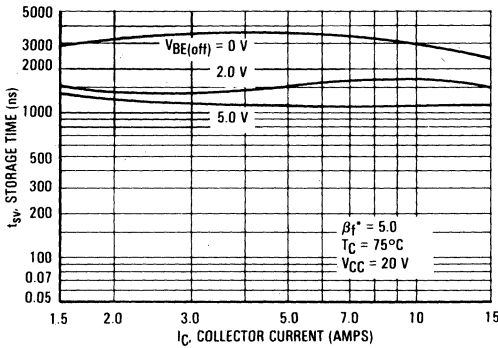


FIGURE 8 — STORAGE TIME

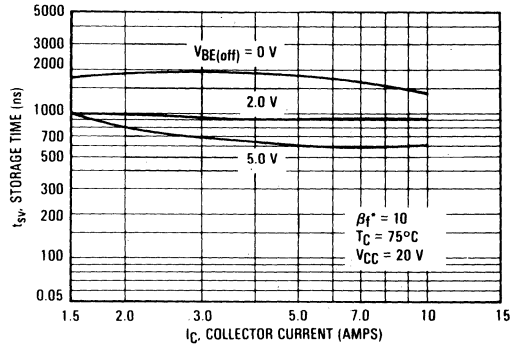


FIGURE 9 — COLLECTOR CURRENT FALL TIME

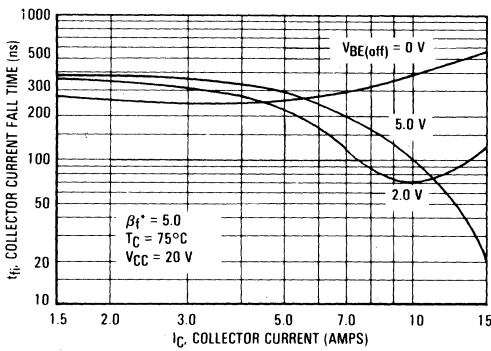


FIGURE 10 — COLLECTOR CURRENT FALL TIME

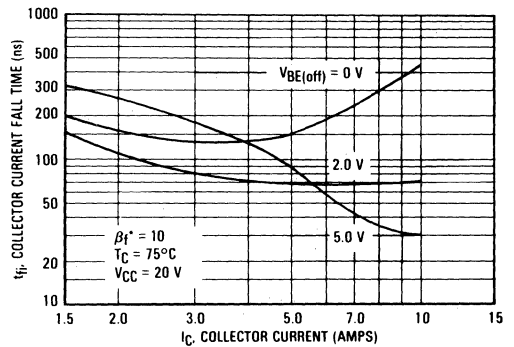


FIGURE 11 — CROSSOVER TIME

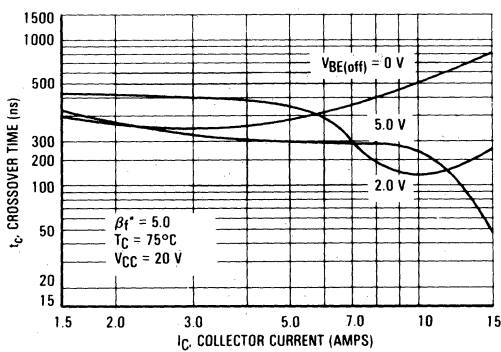
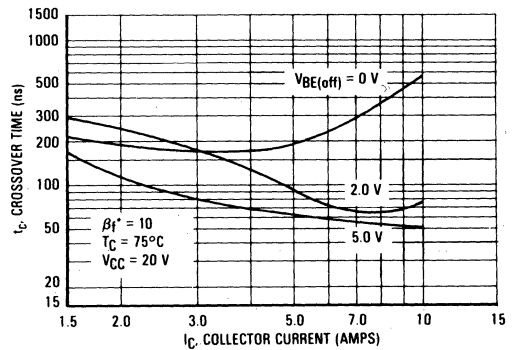


FIGURE 12 — CROSSOVER TIME



$$* \beta_f = \frac{I_C}{I_{B1}}$$

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

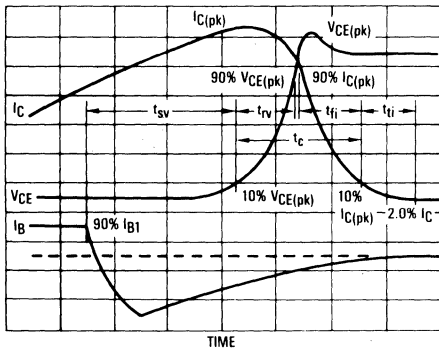
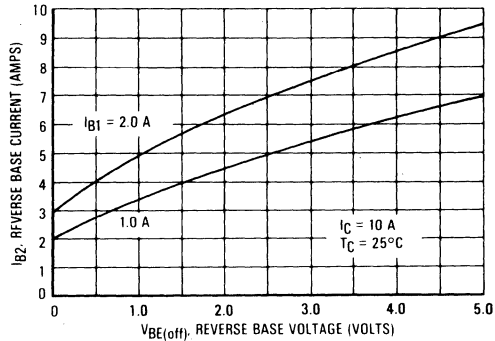
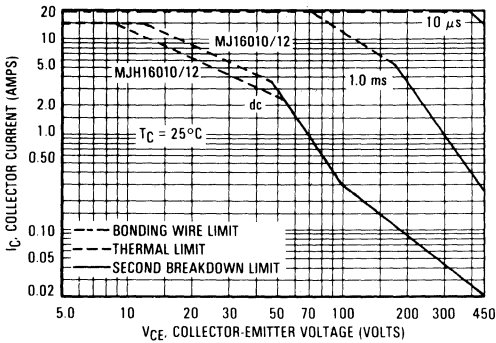


FIGURE 14 — PEAK REVERSE BASE CURRENT



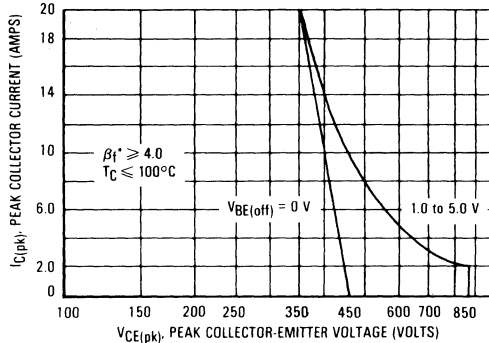
GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



$$\beta_f = \frac{I_C}{I_{B1}}$$

FIGURE 16 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25^\circ C$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_J(pk)$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will re-

duce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

MJ16010, MJ16012, MJH16010, MJH16012

FIGURE 17 — THERMAL RESPONSE

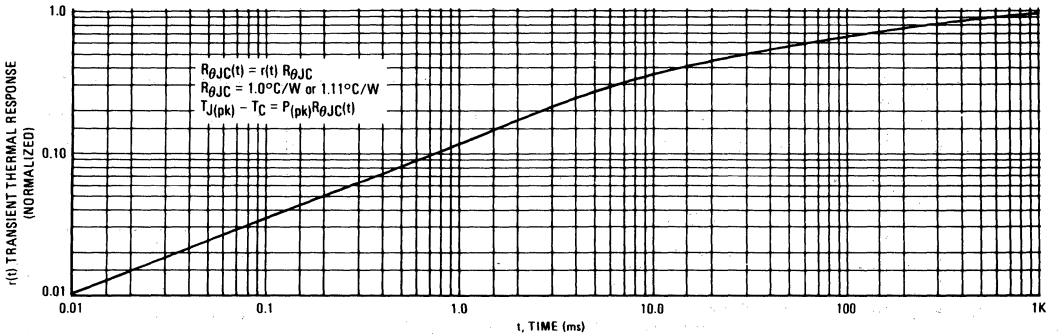


FIGURE 18 — POWER DERATING

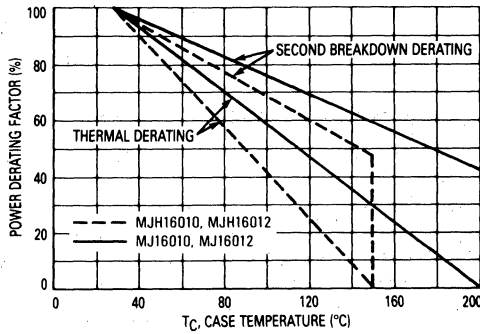
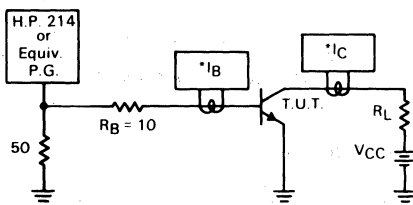
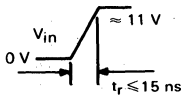


TABLE 1 — RESISTIVE LOAD SWITCHING

t_d and t_r

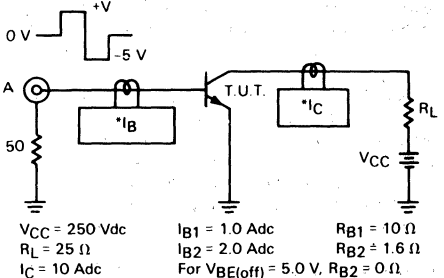
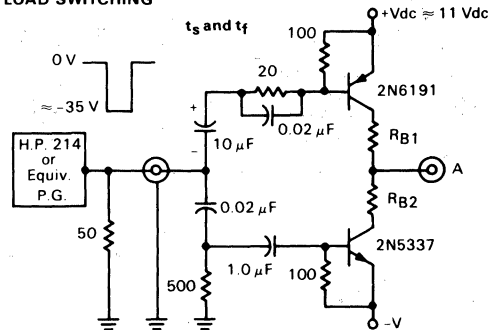


$V_{CC} = 250 \text{ Vdc}$
 $R_L = 25 \Omega$
 $I_C = 10 \text{ Adc}$
 $I_B = 1.0 \text{ Adc}$



*Tektronix AM503
 P6302 or Equivalent

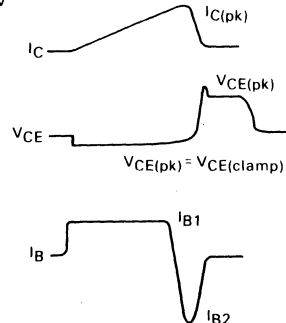
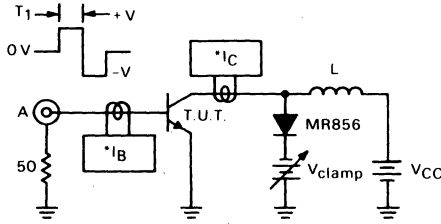
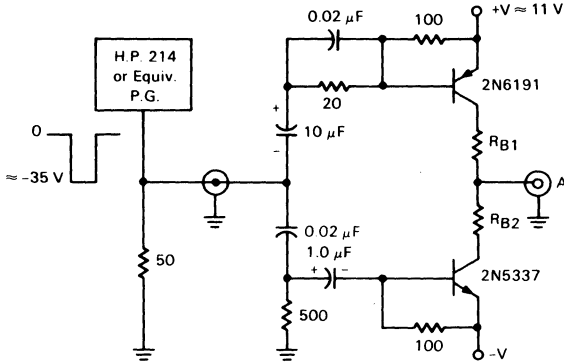
t_s and t_f



$V_{CC} = 250 \text{ Vdc}$
 $R_L = 25 \Omega$
 $I_C = 10 \text{ Adc}$
 $I_{B1} = 1.0 \text{ Adc}$
 $I_{B2} = 2.0 \text{ Adc}$
 $R_{B1} = 10 \Omega$
 $R_{B2} = 1.6 \Omega$
 For $V_{BE(off)} = 5.0 \text{ V}$, $R_{B2} = 0 \Omega$

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



$$T_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

VCEO(sus)
 $L = 10 \text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20 \text{ V}$ Its

Inductive Switching
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ V}$
 R_{B1} selected for desired I_{B1}

RBSOA
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ V}$
 R_{B1} selected for desired I_{B1}

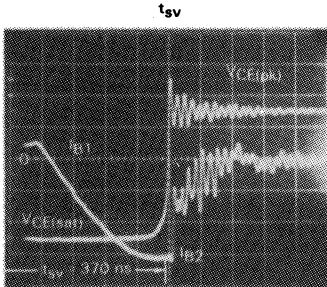
*Tektronix AM503
 P6302 or Equivalent

Scope — Tektronix
 7403 or Equivalent

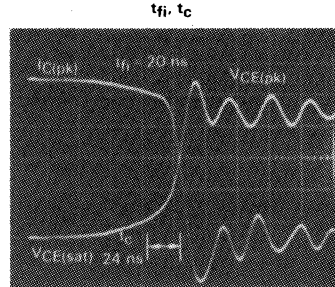
Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

$I_{C(pk)} = 10 \text{ A}$
 $I_{B1} = 1.0 \text{ A}$
 $V_{BE(off)} = 5.0 \text{ V}$
 $V_{CE(pk)} = 400 \text{ V}$
 $T_C = 25^\circ\text{C}$
 Time Base =
 100 ns/cm



$I_{C(pk)} = 10 \text{ A}$
 $I_{B1} = 1.0 \text{ A}$
 $V_{BE(off)} = 5.0 \text{ V}$
 $V_{CE(pk)} = 400 \text{ V}$
 $T_C = 25^\circ\text{C}$
 Time Base =
 20 ns/cm



Designer's Data Sheet
NPN Silicon Power Transistors
1 kV Switchmode III Series

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:

- Collector-Emitter Voltage — $V_{CEV} = 1000$ Vdc
- Fast Turn-Off Times
 - 50 ns Inductive Fall Time — 100°C (Typ)
 - 90 ns Inductive Crossover Time — 100°C (Typ)
 - 900 ns Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Load
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents
- Extended FBSOA Rating Using Ultra-fast Rectifiers
- Extremely High RBSOA Capability

MAXIMUM RATINGS

Rating	Symbol	MJ16010A	MJH16010A	Unit
Collector-Emitter Voltage	V_{CEO}	500		Vdc
Collector-Emitter Voltage	V_{CEV}	1000		Vdc
Emitter-Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous	I_C	15		Adc
— Peak ⁽¹⁾	I_{CM}	20		
Base Current — Continuous	I_B	10		Adc
— Peak ⁽¹⁾	I_{BM}	15		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175	135	Watts
@ $T_C = 100^\circ\text{C}$		100	54	
Derate above $T_C = 25^\circ\text{C}$		1	1.09	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	-55 to 150	°C

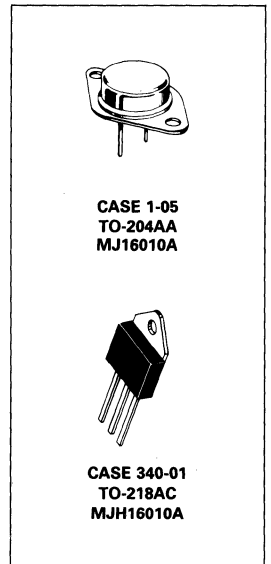
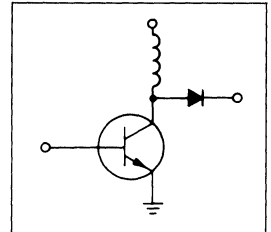
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	0.92	°C/W
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

POWER TRANSISTORS
15 AMPERES
500 VOLTS
125 and 175 WATTS



MJ16010A, MJH16010A

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)					
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	500	—	—	Vdc
Collector Cutoff Current (V _{CEV} = 1000 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = 1000 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	— —	0.003 0.020	0.15 1.0	mAdc
Collector Cutoff Current (V _{CE} = 1000 Vdc, R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	0.020	1.0	mAdc
Emitter Cutoff Current (V _{EB} = 6 Vdc, I _C = 0)	I _{EBO}	—	0.005	0.15	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figure 14a or 14b			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 15			

ON CHARACTERISTICS(1)

Collector-Emitter Saturation Voltage (I _C = 5 Adc, I _B = 1 Adc) (I _C = 10 Adc, I _B = 2 Adc) (I _C = 10 Adc, I _B = 2 Adc, T _C = 100°C)	V _{CE(sat)}	— — —	0.25 0.45 0.60	0.7 1 1.5	Vdc
Base-Emitter Saturation Voltage (I _C = 10 Adc, I _B = 2 Adc) (I _C = 10 Adc, I _B = 2 Adc, T _C = 100°C)	V _{BE(sat)}	— —	1.2 1.2	1.5 1.5	Vdc
DC Current Gain (I _C = 15 Adc, V _{CE} = 5 Vdc)	h _{FE}	5	8	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1 kHz)	C _{ob}	—	—	400	pF
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SWITCHING CHARACTERISTICS

Inductive Load (Table 1)							
Storage Time	(I _C = 10 Adc, I _{B1} = 1.3 Adc, V _{BE(off)} = 5 Vdc, V _{CE(pk)} = 400 Vdc)	(T _J = 100°C)	t _{sv}	—	900	2000	ns
Fall Time			t _{fi}	—	50	250	
Crossover Time			t _c	—	90	300	
Storage Time		(T _J = 150°C)	t _{sv}	—	1100	—	
Fall Time			t _{fi}	—	70	—	
Crossover Time			t _c	—	120	—	
Resistive Load (Table 2)							
Delay Time	(I _C = 10 Adc, V _{CC} = 250 Vdc, I _{B1} = 1.3 Adc, PW = 30 μs, Duty Cycle ≤ 2%)	(I _{B2} = 2.6 Adc, R _{B2} = 1.6 Ω)	t _d	—	25	100	ns
Rise Time			t _r	—	325	600	
Storage Time			t _s	—	1300	3000	
Fall Time		(V _{BE(off)} = 5 Vdc)	t _f	—	175	400	
Storage Time			t _s	—	700	—	
Fall Time			t _f	—	80	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

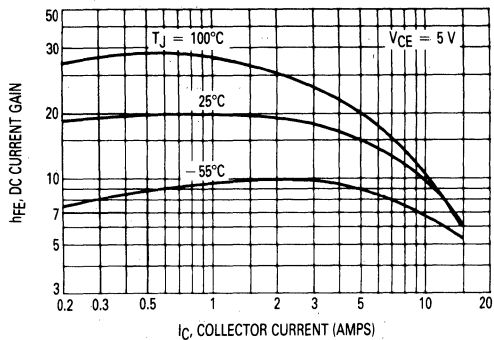


Figure 1. DC Current Gain

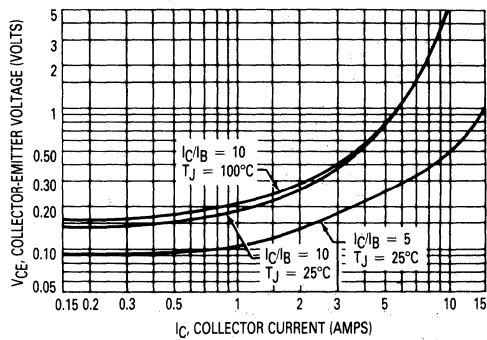


Figure 2. Collector-Emitter Saturation Region

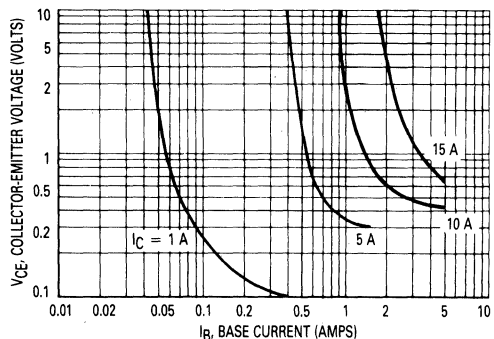


Figure 3. Collector-Emitter Saturation Region

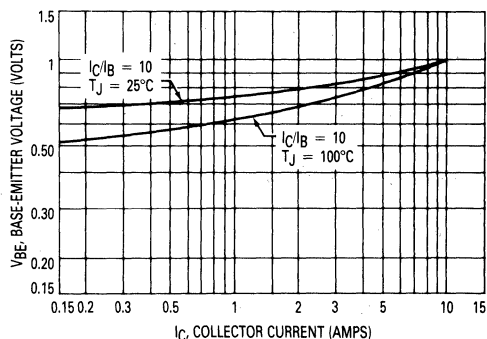


Figure 4. Base-Emitter Saturation Region

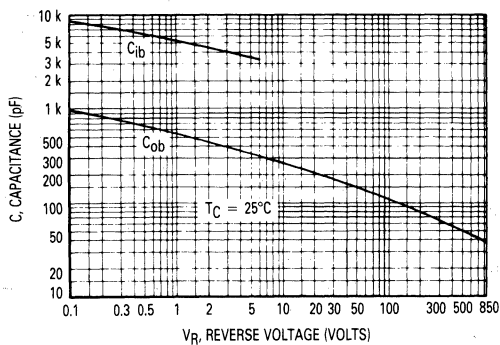


Figure 5. Capacitance

3

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

$I_C/I_{B1} = 5, T_C = 75^\circ\text{C}, V_{CE(pk)} = 400\text{ V}$

$I_C/I_{B1} = 10, T_C = 75^\circ\text{C}, V_{CE(pk)} = 400\text{ V}$

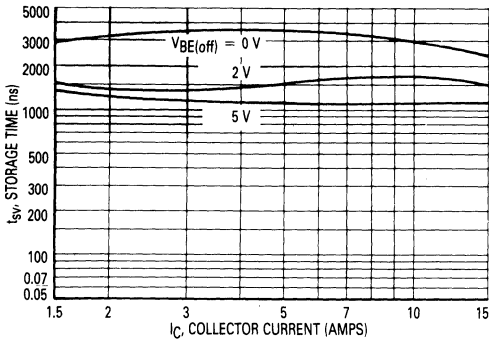


Figure 6. Storage Time

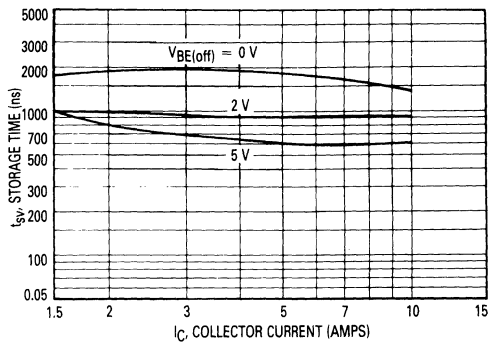


Figure 7. Storage Time

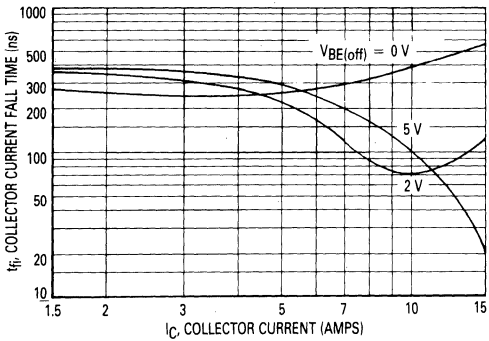


Figure 8. Collector Current Fall Time

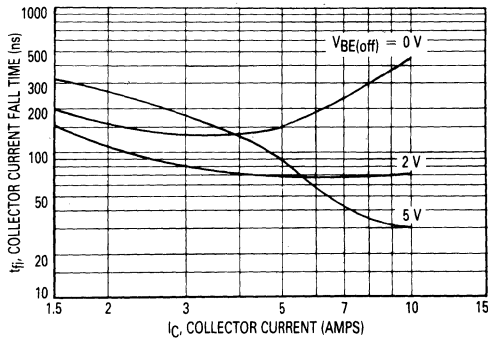


Figure 9. Collector Current Fall Time

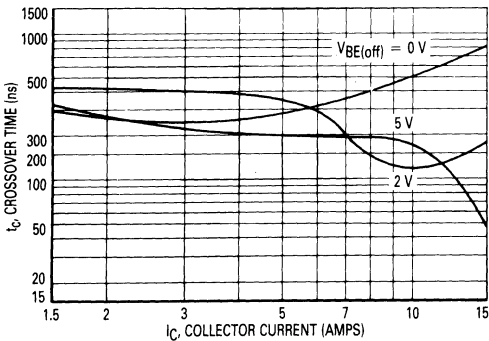


Figure 10. Crossover Time

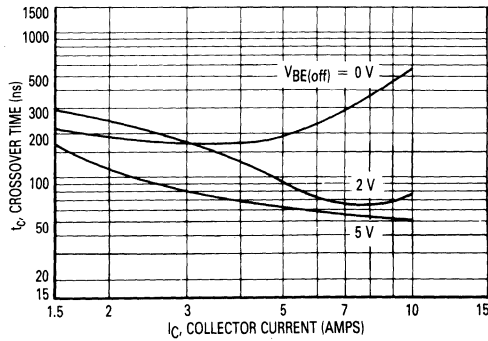
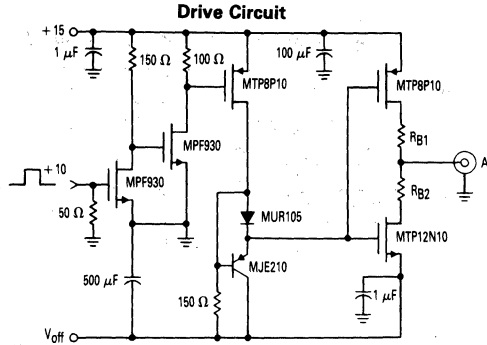


Figure 11. Crossover Time

Table 1. Inductive Load Switching



*Tektronix AM503
P6302 or Equivalent

Scope - Tektronix
7403 or Equivalent

$$T_1 \approx \frac{L_{coil} (I_{C(pk)})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

$V_{CE0(sus)}$
 $L = 10 \text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20 \text{ Volts}$
 $I_{C(pk)} = 100 \text{ mA}$

Inductive Switching
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

RBSOA
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

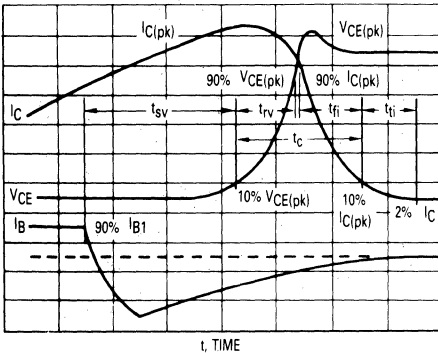
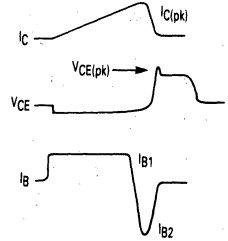


Figure 12. Inductive Switching Measurements

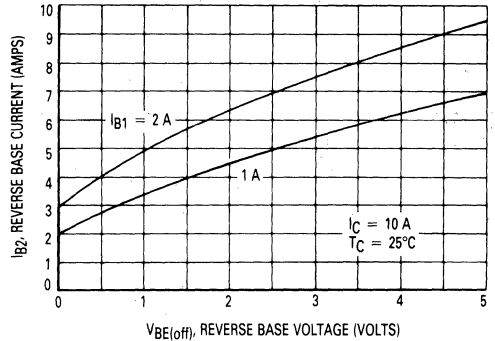
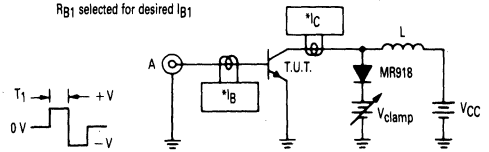
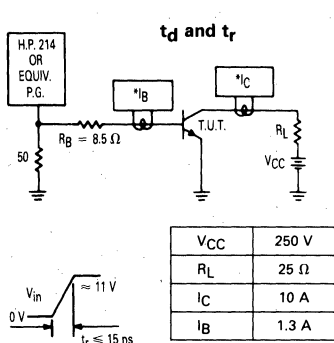
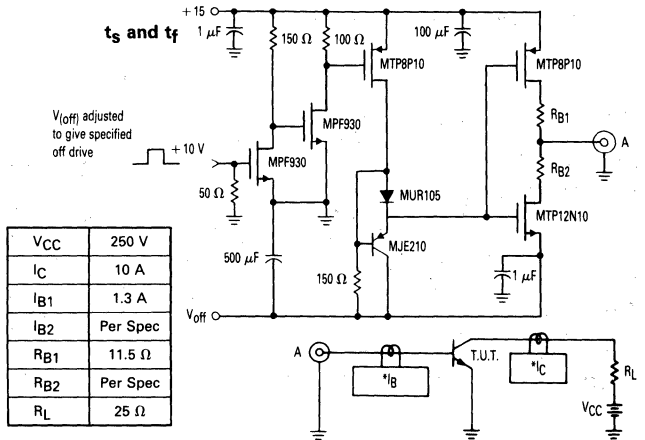


Figure 13. Peak Reverse Base Current

Table 2. Resistive Load Switching



V_{CC}	250 V
R_L	25 Ω
I_C	10 A
I_B	1.3 A

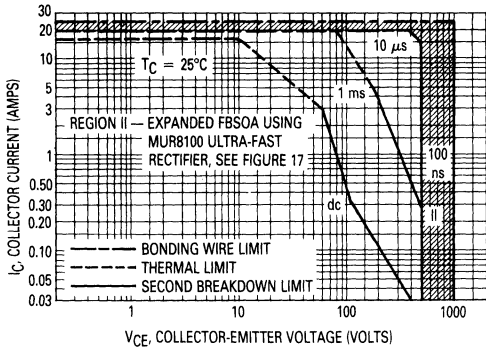


V_{CC}	250 V
I_C	10 A
I_{B1}	1.3 A
I_{B2}	Per Spec
R_{B1}	11.5 Ω
R_{B2}	Per Spec
R_L	25 Ω

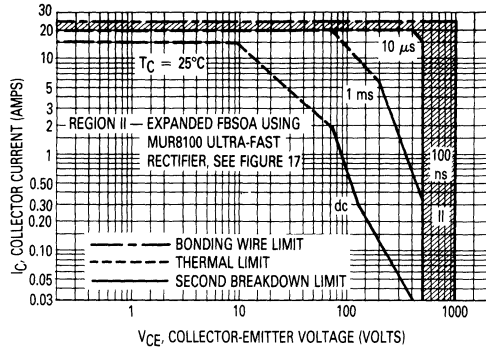
*Tektronix AM503
P6302 or Equivalent

MJ16010A, MJH16010A

GUARANTEED OPERATING AREA INFORMATION



a. MJ16010A



b. MJH16010A

Figure 14. Maximum Rated Forward Biased Safe Operating Area

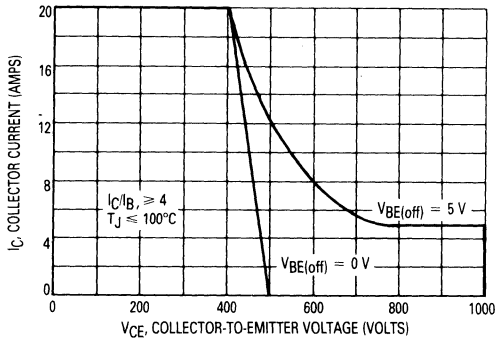


Figure 15. Maximum Reverse Biased Safe Operating Area

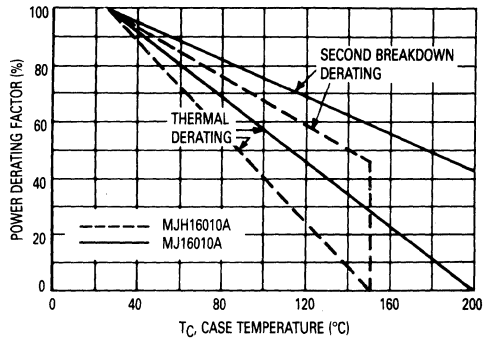


Figure 16. Power Derating

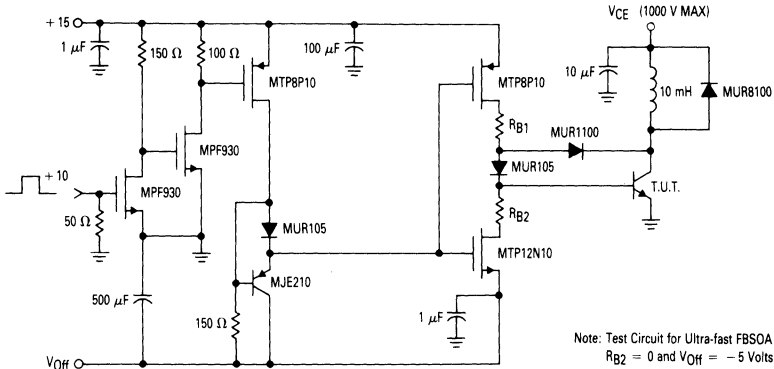


Figure 17. Switching Safe Operating Area

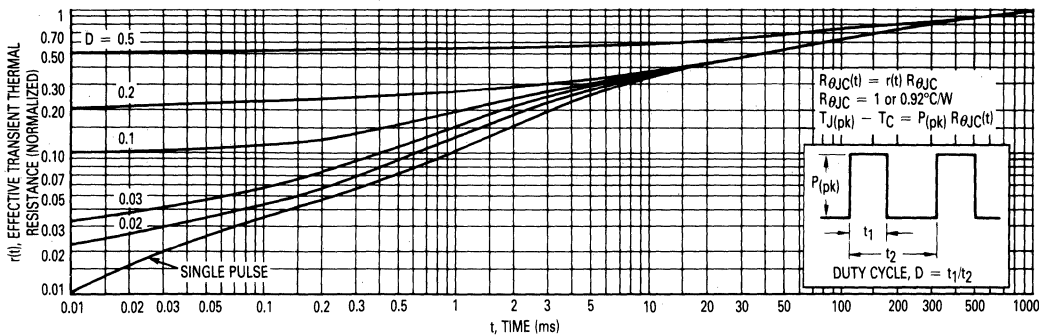


Figure 18. Thermal Response

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 14a and 14b is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 14a and 14b may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE III DESIGN CONSIDERATIONS

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector-emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{CE(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN-ON —

Safe turn-on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra-fast recovery rectifiers, and are valid for turn-on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{CE(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn-on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

3. TURN-OFF —

A bipolar transistor's ability to withstand turn-off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

3

SWITCHMODE III DESIGN CONSIDERATIONS (Cont.)

4. OPERATION ABOVE $V_{CE0(sus)}$ —

When bipolars are operated above collector-emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn-on, as is a stiff negative bias needed for safe turn-off. Any hiccup in the base-drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

5. RBSOA —

Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA

results in several types of circuits (see Application Note AN951).

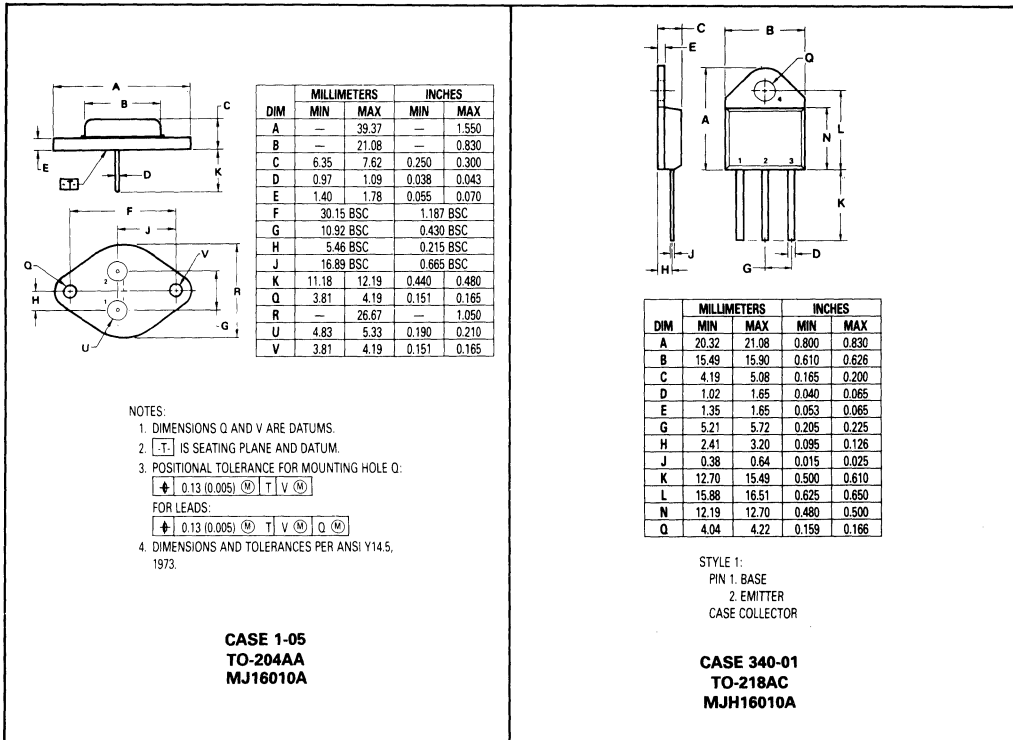
6. DESIGN SAMPLES —

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR4100 types are well-suited for higher drive requirements (see Article Reprint AR131).

OUTLINE DIMENSIONS



MJ16014
MJ16016

Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications. The MJ16016 is a selected high-gain version of the MJ16014 for applications where drive current is limited.

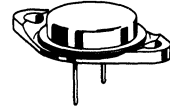
Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 40 ns Inductive Fall Time — 75°C (Typ)
 - 40 ns Inductive Crossover Time — 75°C (Typ)
 - 800 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

20 AMPERE

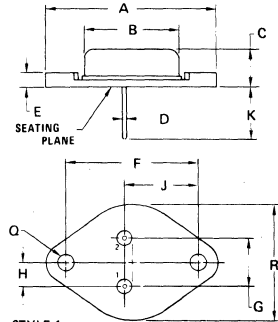
NPN SILICON
POWER TRANSISTORS

450 VOLTS
250 WATTS



Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V _{CEO}	450	Vdc
Collector-Emitter Voltage	V _{CEV}	850	Vdc
Emitter Base Voltage	V _{EB}	6.0	Vdc
Collector Current — Continuous	I _C	20	Adc
— Peak (1)	I _{CM}	30	
Base Current — Continuous	I _B	10	Adc
— Peak (1)	I _{BM}	20	
Total Power Dissipation @ T _C = 25°C	P _D	250	Watts
@ T _C = 100°C		143	
Derate above 25°C		1.43	W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

MJ16014

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	450	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 850\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current ($V_{CE} = 850\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.3\text{ Adc}$) ($I_C = 15\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 15\text{ Adc}$, $I_B = 2.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 15\text{ Adc}$, $I_B = 2.0\text{ Adc}$) ($I_C = 15\text{ Adc}$, $I_B = 2.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.5 1.5	Vdc
DC Current Gain ($I_C = 20\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	5.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	500	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	$I_C = 15\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 2.0\text{ Adc}$, $PW = 30\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$	$(I_{B2} = 4.0\text{ Adc}$, $R_B = 1.6\ \Omega)$	t_d	—	20	50	ns
Rise Time			t_r	—	200	500	
Storage Time			t_s	—	1200	2700	
Fall Time			t_f	—	200	350	
Storage Time			t_{sv}	—	650	—	
Fall Time			t_{fv}	—	80	—	
Inductive Load (Table 2)							
Storage Time	$I_C = 15\text{ Adc}$, $I_{B1} = 2.0\text{ Adc}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$	$(T_C = 100^\circ\text{C})$	t_{sv}	—	800	2700	ns
Fall Time			t_{fv}	—	50	200	
Crossover Time			t_c	—	90	250	
Storage Time			t_{sv}	—	1050	—	
Fall Time			t_{fv}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: PW = 300 μs , Duty Cycle $\leq 2\%$.

* $\beta_1 = \frac{I_C}{I_{B1}}$



MJ16016

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Table 2) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	450	—	—	Vdc
Collector Cutoff Current (V _{CEV} = 850 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = 850 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V _{CE} = 850 Vdc, R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V _{EB} = 6.0 Vdc, I _C = 0)	I _{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage (I _C = 10 Adc, I _B = 1.0 Adc) (I _C = 15 Adc, I _B = 1.5 Adc) (I _C = 15 Adc, I _B = 1.5 Adc, T _C = 100°C)	V _{CE(sat)}	— — —	— — —	2.5 3.0 3.0	Vdc
Base-Emitter Saturation Voltage (I _C = 15 Adc, I _B = 1.5 Adc) (I _C = 15 Adc, I _B = 1.5 Adc, T _C = 100°C)	V _{BE(sat)}	— —	— —	1.5 1.5	Vdc
DC Current Gain (I _C = 20 Adc, V _{CE} = 5.0 Vdc)	h _{FE}	7.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1.0 kHz)	C _{ob}	—	—	500	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	I _C = 15 Adc, V _{CC} = 250 Vdc, I _{B1} = 1.5 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%	I _{B2} = 3.0 Adc, R _B = 1.6 Ω	t _d	—	20	50	ns
Rise Time			t _r	—	200	500	
Storage Time			t _s	—	900	2200	
Fall Time			t _f	—	100	250	
Storage Time			t _s	—	500	—	
Fall Time	t _f	—	40	—			

Inductive Load (Table 2)

Storage Time	I _C = 15 Adc, I _{B1} = 1.5 Adc, V _{BE(off)} = 5.0 Vdc, V _{CE(pk)} = 400 Vdc	T _C = 100°C	t _{sv}	—	750	2500	ns
Fall Time			t _{fi}	—	30	150	
Crossover Time			t _c	—	50	200	
Storage Time	T _C = 150°C	t _{sv}	—	900	—		
Fall Time		t _{fi}	—	30	—		
Crossover Time		t _c	—	70	—		

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

*β_f = I_C / I_{B1}

TYPICAL STATIC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

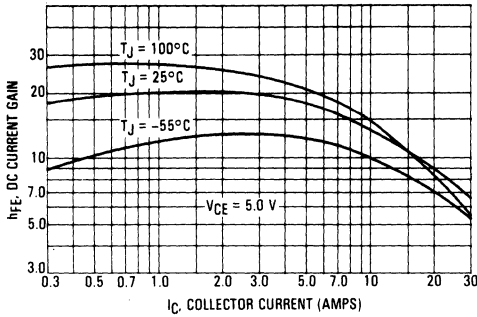


FIGURE 2 — COLLECTOR SATURATION REGION

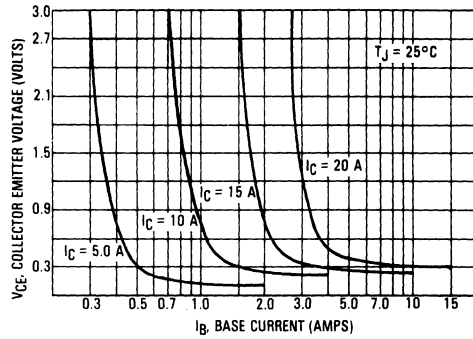


FIGURE 3 — COLLECTOR-EMITTER SATURATION REGION

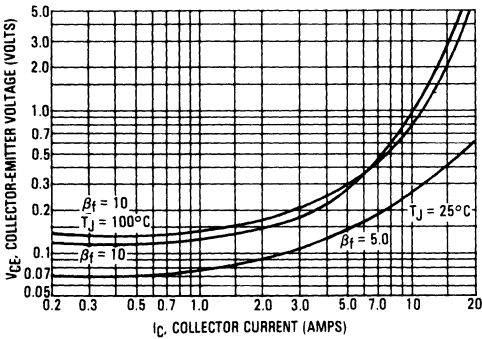


FIGURE 4 — BASE-EMITTER VOLTAGE

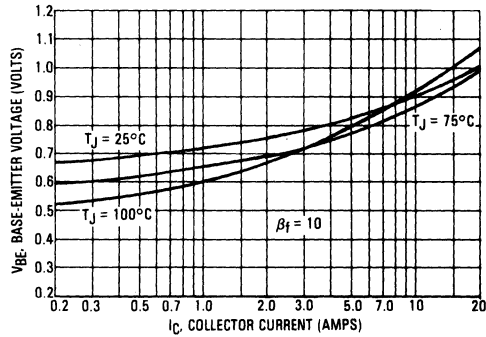


FIGURE 5 — COLLECTOR CUTOFF REGION

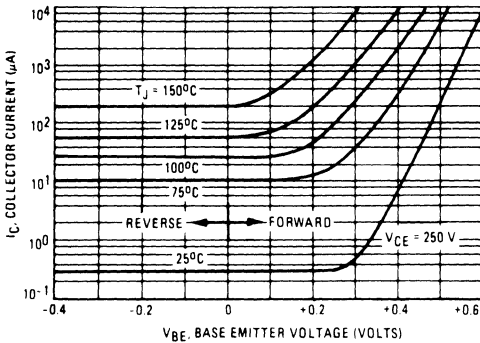
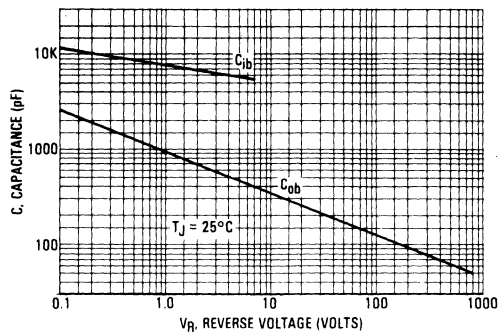


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

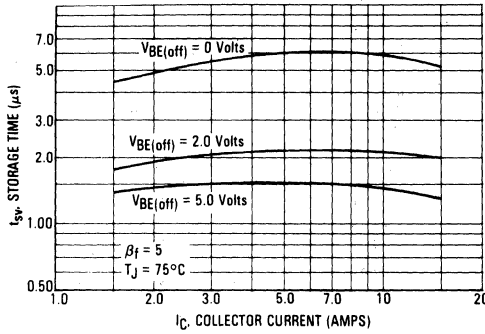


FIGURE 8 — STORAGE TIME

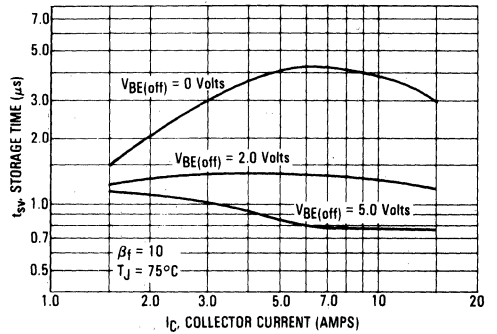


FIGURE 9 — COLLECTOR CURRENT FALL TIME

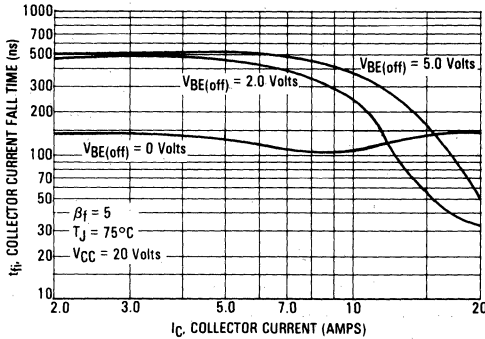


FIGURE 10 — COLLECTOR CURRENT FALL TIME

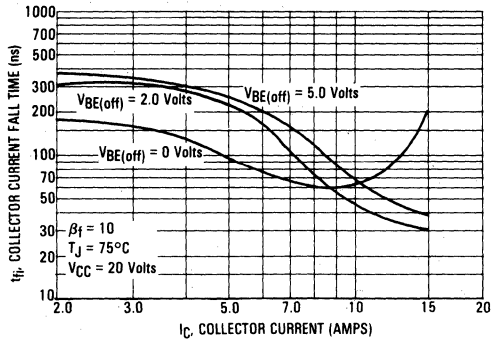


FIGURE 11 — CROSSOVER TIME

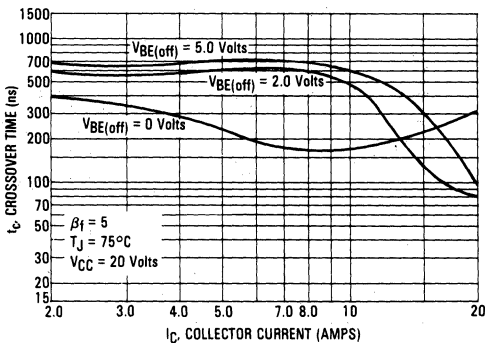


FIGURE 12 — CROSSOVER TIME

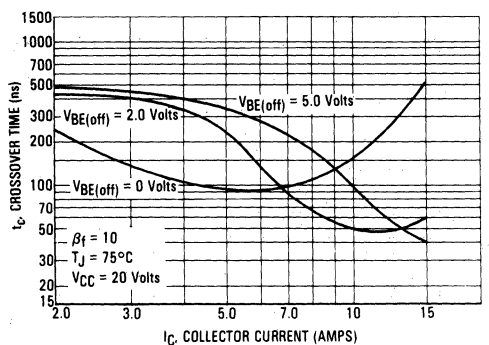


FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

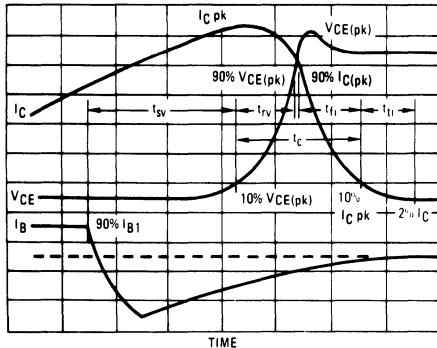
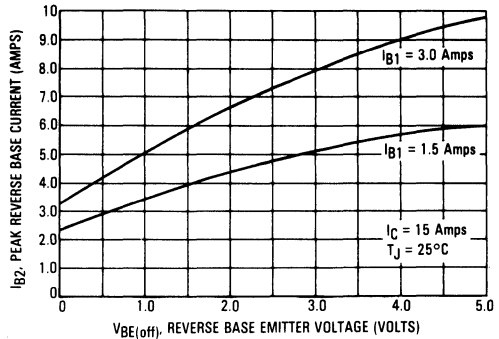


FIGURE 14 — REVERSE BASE CURRENT



GUARANTEED SAFE OPERATING AREA LIMITS

FIGURE 15 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

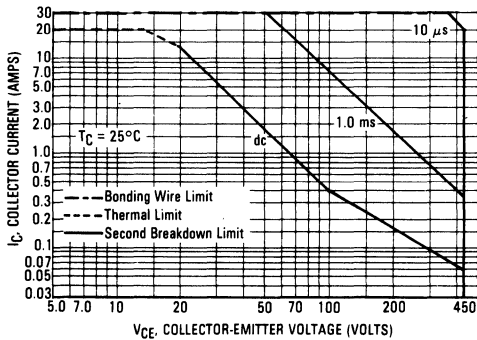
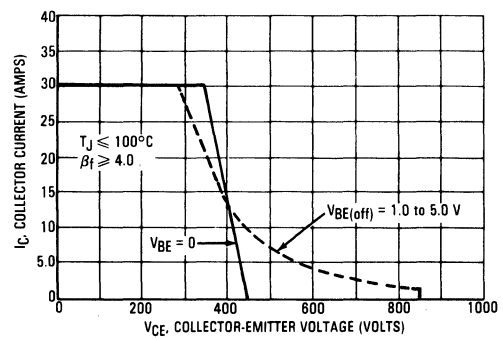


FIGURE 16 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce

the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

FIGURE 17 — THERMAL RESPONSE

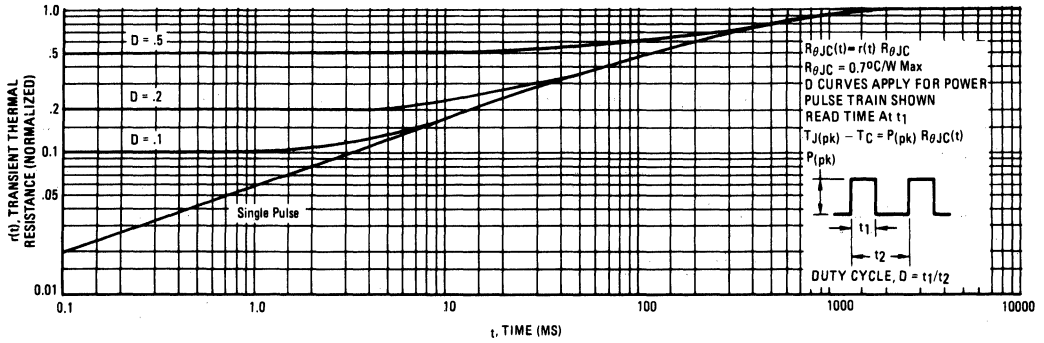


FIGURE 18 — POWER DERATING

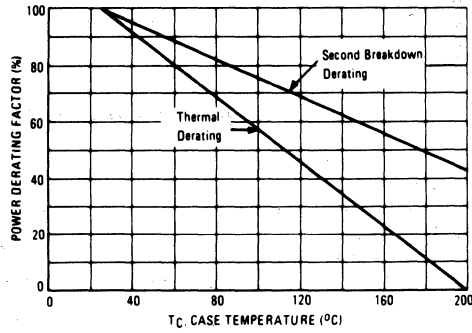
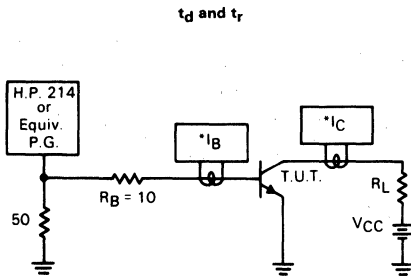
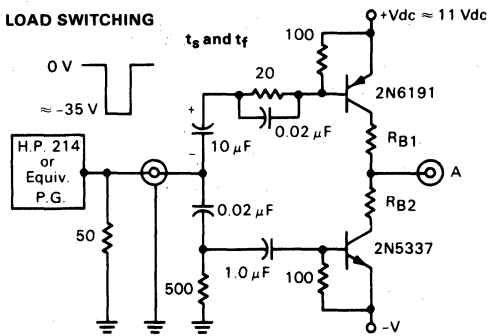


TABLE 1 — RESISTIVE LOAD SWITCHING



$V_{CC} = 250 \text{ Vdc}$
 $R_L = 16 \Omega$
 $I_C = 15 \text{ A}$
 $I_B = 1.5 \text{ A}$

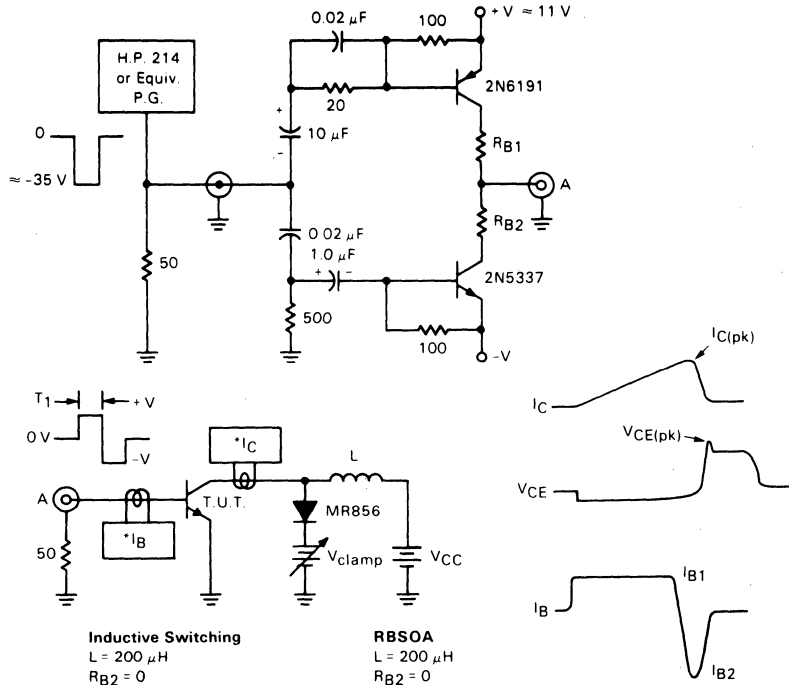
*Tektronix
 P-6042 or
 Equivalent



$V_{CC} = 250$
 $R_L = 16 \Omega$
 $I_C = 15 \text{ A}$
 $I_{B1} = 1.5 \text{ A}$
 $I_{B2} = 3.0 \text{ A}$
 $R_{B1} = 7.5 \Omega$
 $R_{B2} = 1.6 \Omega$
 For $V_{BE(off)} = 5.0 \text{ V}$ $R_{B2} = 0 \Omega$

*Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 - INDUCTIVE LOAD SWITCHING



$$T_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

V_{CEO(sus)}
 L = 10 mH
 $R_{B2} = \infty$
 $V_{CC} = 20$ Volts

Inductive Switching
 L = 200 μ H
 $R_{B2} = 0$
 $V_{CC} = 20$ Volts
 R_{B1} selected for desired I_{B1}

RBSOA
 L = 200 μ H
 $R_{B2} = 0$
 $V_{CC} = 20$ Volts
 R_{B1} selected for desired I_{B1}

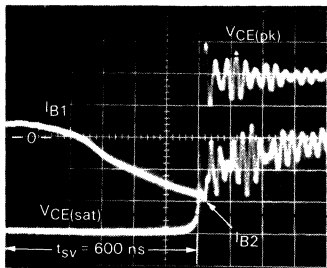
*Tektronix
 P-6042 or
 Equivalent

Scope - Tektronix
 7403 or
 Equivalent

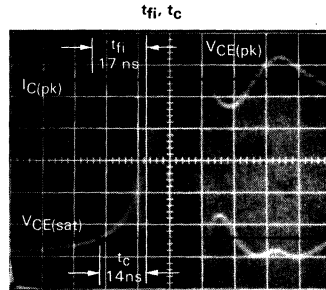
Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

$I_{C(pk)} = 15$ A
 $I_{B1} = 1.5$ A
 $V_{BE(off)} = 5.0$ Volts
 $V_{CE(pk)} = 400$ Volts
 $T_C = 25^\circ$ C
 Time Base = 100 ns/cm



$I_{C(pk)} = 15$ A
 $I_{B1} = 1.5$ A
 $V_{BE(off)} = 5.0$ Volts
 $V_{CE(pk)} = 400$ Volts
 $T_C = 25^\circ$ C
 Time Base = 10 ns/cm



Designer's Data Sheet
NPN Silicon Power Transistors
1.5 kV Switchmode III Series

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

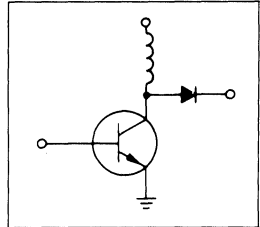
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:

- Collector-Emitter Voltage — $V_{CEV} = 1500$ Vdc
- Fast Turn-Off Times
 - 80 ns Inductive Fall Time — 100°C (Typ)
 - 110 ns Inductive Crossover Time — 100°C (Typ)
 - 4.5 μ s Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Load
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

MJ16018
MJH16018

POWER TRANSISTORS
10 AMPERES
800 VOLTS
125 and 175 WATTS



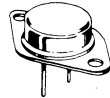
MAXIMUM RATINGS

Rating	Symbol	MJ16018	MJH16018	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	800		Vdc
Collector-Emitter Voltage	V_{CEV}	1500		Vdc
Emitter-Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous	I_C	10		Adc
— Peak ⁽¹⁾	I_{CM}	15		
Base Current — Continuous	I_B	8		Adc
— Peak ⁽¹⁾	I_{BM}	12		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	PD	175	125	Watts
@ $T_C = 100^\circ\text{C}$		100	50	
Derate above $T_C = 25^\circ\text{C}$		1	1	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 200	-55 to 150	°C

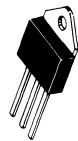
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	1	°C/W
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 μ s, Duty Cycle \leq 10%.



CASE 1-05
TO-204AA
MJ16018



CASE 340-01
TO-218AC
MJH16018

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS(1)

Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 50\text{ mA}$, $I_B = 0$)	$V_{CE0(sus)}$	800	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 1500\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 1500\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current ($V_{CE} = 1500\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 6\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	0.1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 13			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 14			

ON CHARACTERISTICS(1)

Collector-Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 5\text{ Adc}$) ($I_C = 5\text{ Adc}$, $I_B = 2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	—	—	1 5 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 5\text{ Adc}$, $I_B = 2\text{ Adc}$) ($I_C = 5\text{ Adc}$, $I_B = 2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	—	—	1.5 1.5	Vdc
DC Current Gain ($I_C = 5\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	4	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1\text{ kHz}$)	C_{ob}	—	—	450	pF
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SWITCHING CHARACTERISTICS

Inductive Load (Table 1)							
Storage Time	Baker Clamped ($I_C = 5\text{ Adc}$, $I_{B1} = 2\text{ Adc}$, $V_{BE(off)} = 2\text{ Vdc}$, $V_{CE(pk)} = 400\text{ Vdc}$, $PW = 25\ \mu\text{s}$)	$(T_J = 25^\circ\text{C})$	t_{sv}	—	4000	8000	ns
Fall Time			t_{fi}	—	60	200	
Crossover Time			t_c	—	90	300	
Storage Time		$(T_J = 100^\circ\text{C})$	t_{sv}	—	4500	9000	
Fall Time			t_{fi}	—	80	250	
Crossover Time			t_c	—	110	375	
Resistive Load (Table 1)							
Delay Time	$(I_C = 5\text{ Adc}$, $V_{CC} = 250\text{ Vdc}$, $I_{B1} = 2\text{ Adc}$, $I_{B2} = 2\text{ Adc}$, $R_{B2} = 3\ \Omega$, $PW = 25\ \mu\text{s}$, Duty Cycle $\leq 2\%$)		t_d	—	85	200	ns
Rise Time			t_r	—	900	2000	
Storage Time			t_s	—	4500	9000	
Fall Time			t_f	—	200	400	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

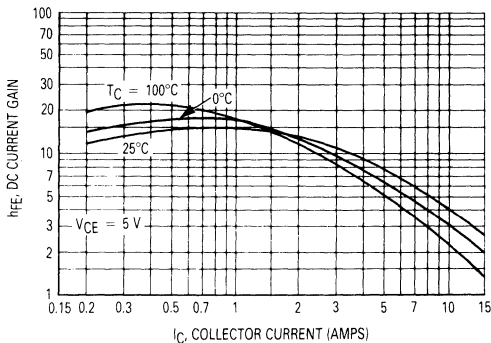


Figure 1. DC Current Gain

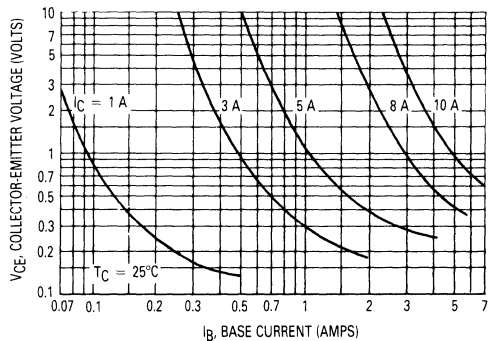


Figure 2. Collector Saturation Region



TYPICAL STATIC CHARACTERISTICS

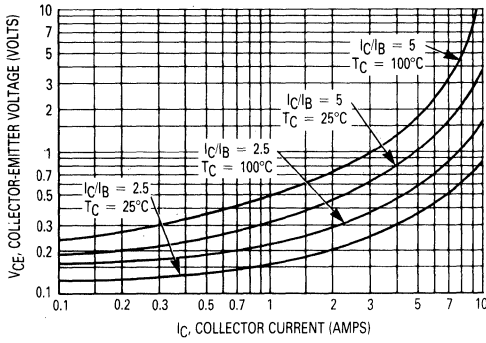


Figure 3. Collector-Emitter Saturation Region

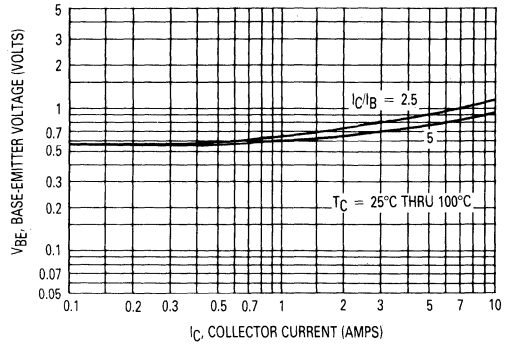


Figure 4. Base-Emitter Saturation Region

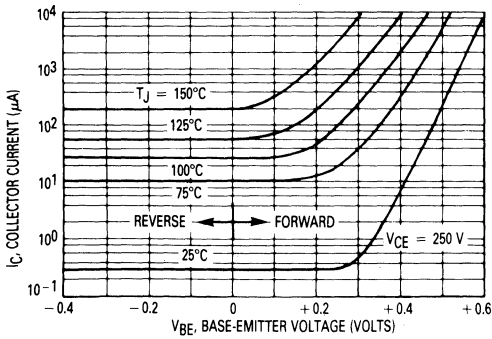


Figure 5. Collector Cutoff Region

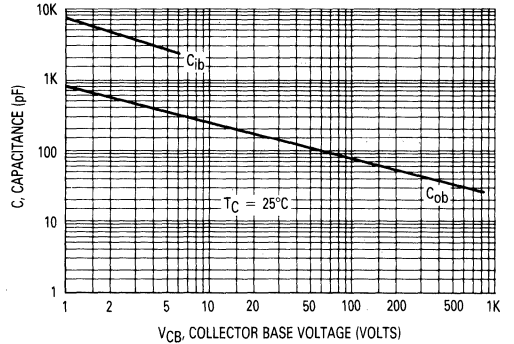


Figure 6. Typical Capacitance

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

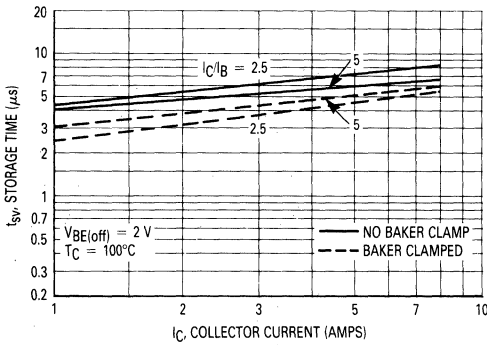


Figure 7. Storage Time

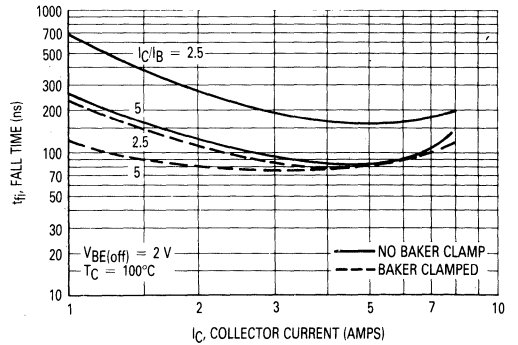


Figure 8. Inductive Switching Fall Time

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TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

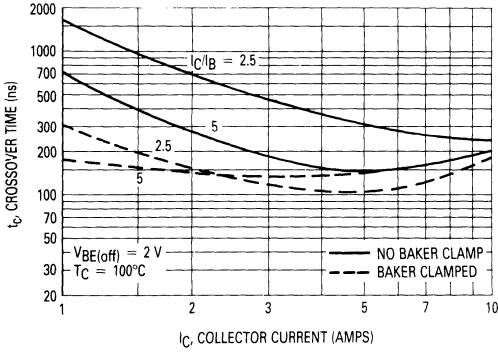


Figure 9. Inductive Switching Crossover Time

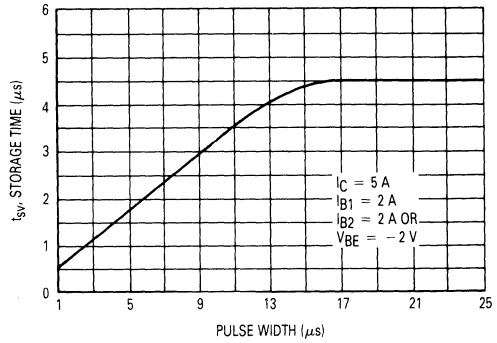


Figure 10. (t_{sv}) Storage Time versus I_{B1} Pulse Width

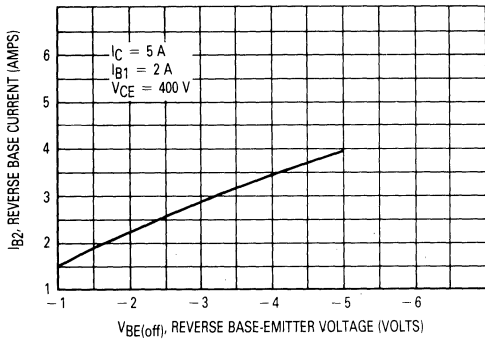


Figure 11. Reverse Base Current versus Off Voltage

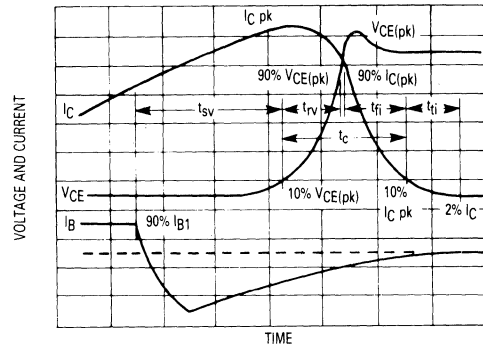


Figure 12. Inductive Switching Measurements

3

GUARANTEED SAFE OPERATING AREA LIMITS

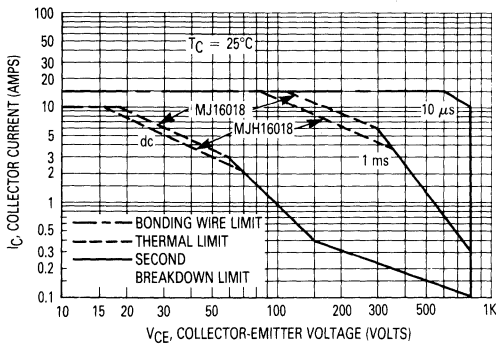


Figure 13. Maximum Forward Bias Safe Operating Area

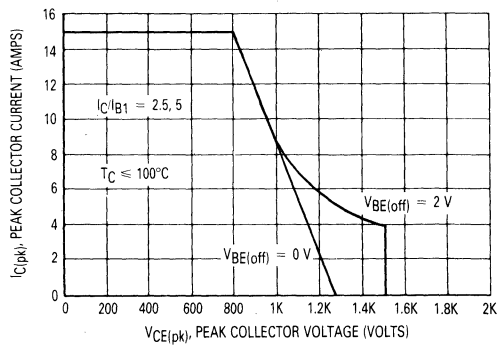


Figure 14. Maximum Reverse Bias Safe Operating Area

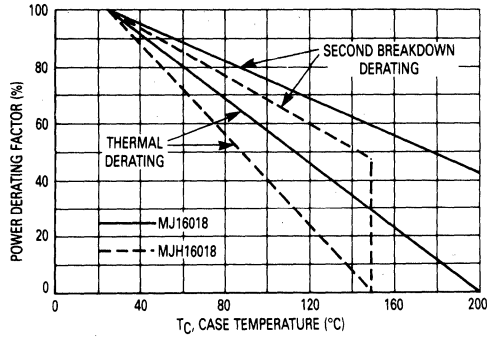


Figure 15. Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 16. At high case temperatures, thermal limitations will

reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

3

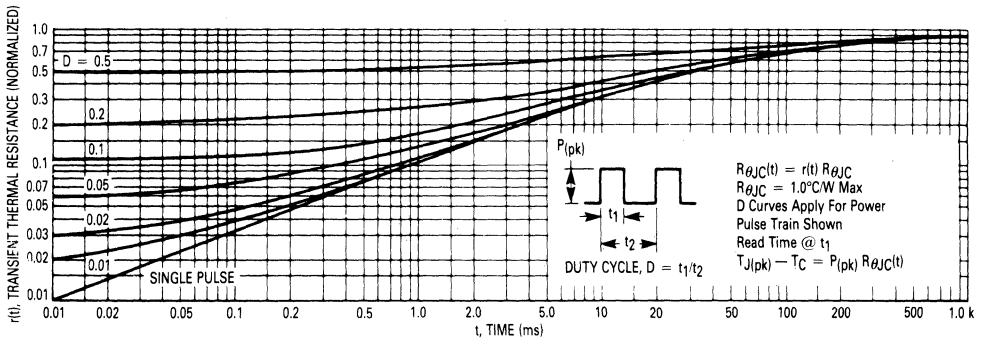
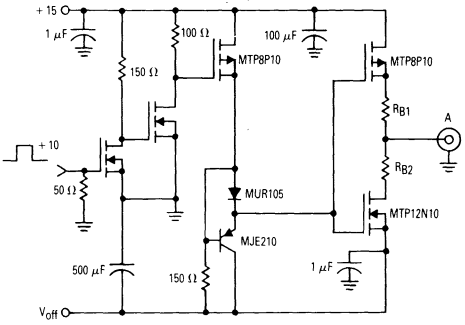
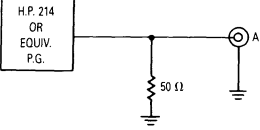
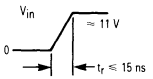
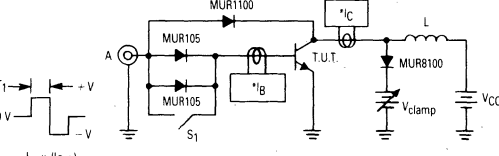
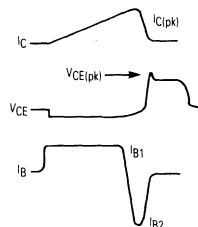
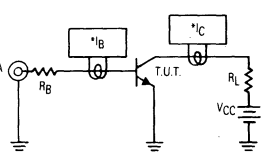


Figure 16. Thermal Response

Table 1. Test Conditions for Dynamic Performance

Input Conditions	V _{CEO} (sus)	RBSOA	Inductive Switching	Resistive Switching
<p style="text-align: center;">Drive Circuit</p>  <p style="text-align: center;">Note: Adjust V_{off} to obtain desired V_{BE(off)} at Point A.</p>				<p style="text-align: center;">For t_d and t_r:</p>   <p style="text-align: center;">For t_s and t_f: Use Inductive Switching Drive Circuit</p>
	<p style="text-align: center;">Circuit Values</p> <p>L = 10 mH R_{B2} = ∞ V_{CC} = 20 Volts I_(pk) = 50 mA S₁ Closed</p>	<p style="text-align: center;">Circuit Values</p> <p>L = 200 µH R_{B2} = 0 V_{CC} = 20 Volts R_{B1} selected for desired I_{B1} S₁ Closed</p>	<p style="text-align: center;">Circuit Values</p> <p>L = 200 µH R_{B2} = 0 when V_{BE(off)} is specified or selected for desired I_{B2} V_{CC} ≈ 20 Volts, Adjusted to obtain desired I_C R_{B1} selected for desired I_{B1} S₁ = Open for baker clamp condition</p>	<p style="text-align: center;">Circuit Values</p> <p>for t_d and t_r V_{CC} = 250 Volts R_B selected for desired I_{B1} R_L selected for desired I_C for t_s and t_f V_{CC} = 250 Volts R_B = 0 R_{B1} & R_{B2} selected for I_{B1} & I_{B2} R_L selected for desired I_C</p>
	<p style="text-align: center;">Test Circuit</p>  <p style="text-align: center;">T₁ = $\frac{L_{soil} I_{C(pk)}}{V_{CC}}$ T₁ adjusted to obtain I_{C(pk)}</p> <p style="text-align: center;">*Tektronix AM503 P6302 or Equivalent</p> <p style="text-align: center;">Scope — Tektronix 7403 or Equivalent</p> 			 <p style="text-align: center;">*Tektronix AM503 P6302 or Equivalent</p>



Complementary Power Transistors

DKA For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Electrically Similar to Popular TIP29 and TIP30 Series

MAXIMUM RATINGS

Rating	Symbol	MJD29 MJD30	MJD29C MJD30C	Unit
Collector-Emitter Voltage	V_{CE0}	40	100	Vdc
Collector-Base Voltage	V_{CB}	40	100	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak	I_C	1 3		Adc
Base Current	I_B	0.4		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	15 0.12		Watts W/ $^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.56 0.012		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.3	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	$^\circ\text{C}/\text{W}$
Lead Temperature for Soldering Purposes	T_L	260	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 30 \text{ mAdc}, I_B = 0$)	MJD29, MJD30 MJD29C, MJD30C	$V_{CE0(sus)}$	40 100	—	Vdc
Collector Cutoff Current ($V_{CE} = 40 \text{ Vdc}, I_B = 0$) ($V_{CE} = 60 \text{ Vdc}, I_B = 0$)	MJD29, MJD30 MJD29C, MJD30C	I_{CEO}	—	50	μAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CE0}, V_{EB} = 0$)		I_{CES}	—	20	μAdc
Emitter Cutoff Current ($V_{BE} = 5 \text{ Vdc}, I_C = 0$)		I_{EBO}	—	1	mAdc

* These ratings are applicable when surface mounted on the minimum pad size recommended.
 (1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

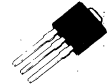
(continued)

NPN
MJD29,C
PNP
MJD30,C

SILICON
POWER TRANSISTORS
1 AMPERE
40 and 100 VOLTS
15 WATTS

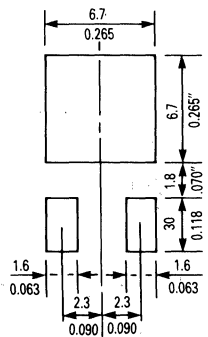


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES
RECOMMENDED FOR
SURFACE MOUNTED
APPLICATIONS



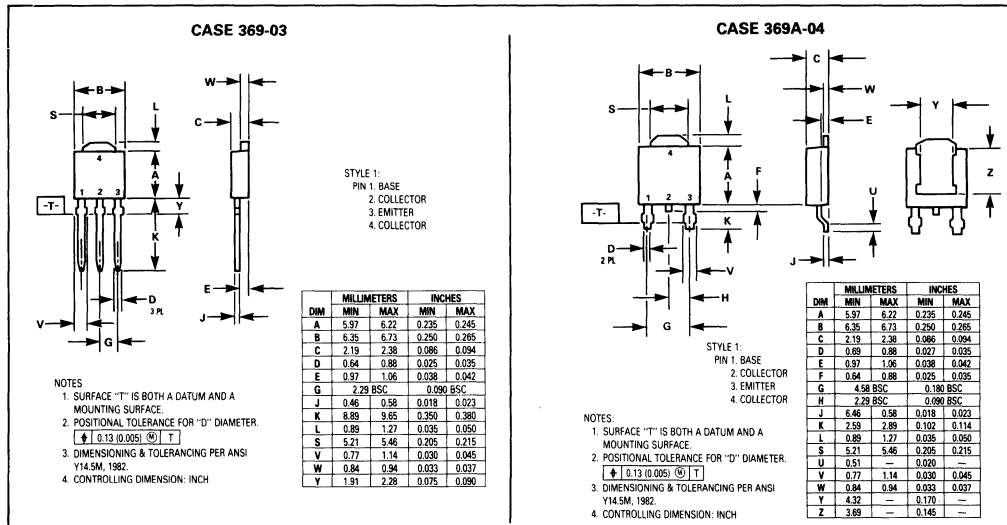
MJD29,C NPN, MJD30,C PNP

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 0.2 \text{ Adc}$, $V_{CE} = 4 \text{ Vdc}$) ($I_C = 1 \text{ Adc}$, $V_{CE} = 4 \text{ Vdc}$)	h_{FE}	40 15	— 75	—
Collector-Emitter Saturation Voltage ($I_C = 1 \text{ Adc}$, $I_B = 125 \text{ mAdc}$)	$V_{CE(sat)}$	—	0.7	Vdc
Base-Emitter On Voltage ($I_C = 1 \text{ Adc}$, $V_{CE} = 4 \text{ Vdc}$)	$V_{BE(on)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) ($I_C = 200 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 1 \text{ MHz}$)	f_T	3	—	MHz
Small-Signal Current Gain ($I_C = 0.2 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1 \text{ kHz}$)	$ h_{fe} $	20	—	—

- (1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.
 (2) $f_T = |h_{fe}| \cdot f_{test}$

OUTLINE DIMENSIONS



Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD29-1)

MJD29,C NPN, MJD30,C PNP

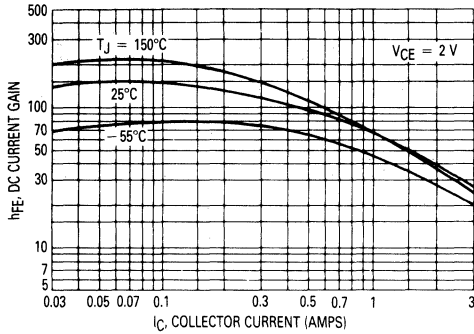


Figure 1. DC Current Gain

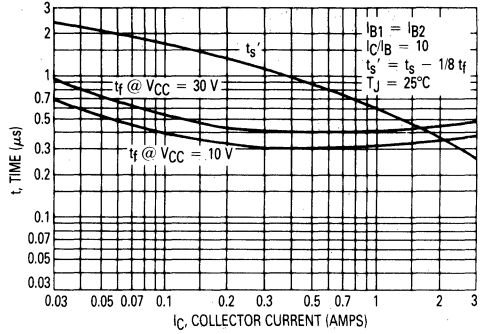


Figure 2. Turn-Off Time

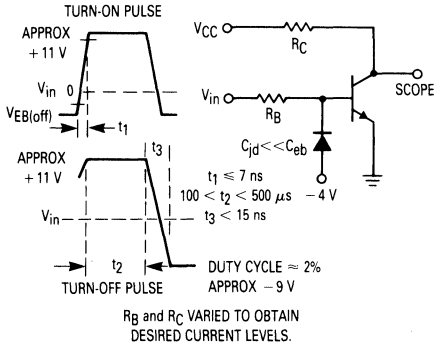


Figure 3. Switching Time Equivalent Circuit

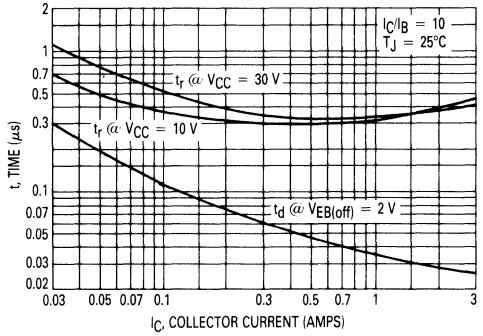


Figure 4. Turn-On Time

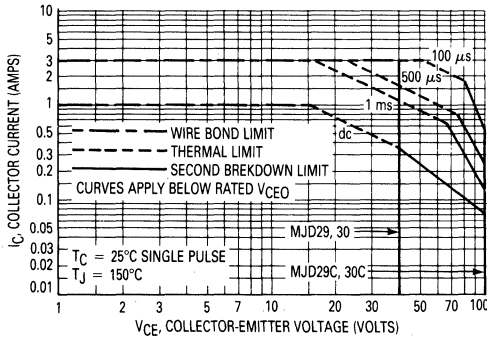


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

MJD29,C NPN, MJD30,C PNP

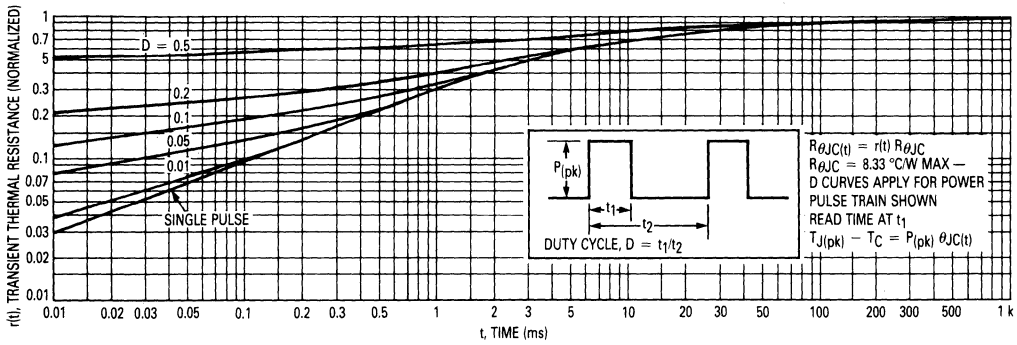


Figure 6. Thermal Response

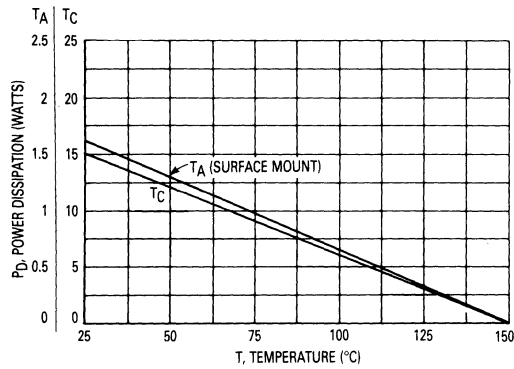


Figure 7. Power Derating

Complementary Power Transistors

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Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Electrically Similar to Popular TIP31 and TIP32 Series

MAXIMUM RATINGS

Rating	Symbol	MJD31 MJD32	MJD31C MJD32C	Unit
Collector-Emitter Voltage	V_{CE0}	40	100	Vdc
Collector-Base Voltage	V_{CB}	40	100	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak	I_C	3 5		A _{dc}
Base Current	I_B	1		A _{dc}
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	15 0.12		Watts W/ $^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.56 0.012		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.3	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	$^\circ\text{C/W}$
Lead Temperature for Soldering Purposes	T_L	260	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 30 \text{ mA}_{dc}, I_B = 0$)	MJD31, MJD32 MJD31C, MJD32C	$V_{CE0(sus)}$	40 100	—	Vdc
Collector Cutoff Current ($V_{CE} = 40 \text{ Vdc}, I_B = 0$) ($V_{CE} = 60 \text{ Vdc}, I_B = 0$)	MJD31, MJD32 MJD31C, MJD32C	I_{CEO}	—	50	μA_{dc}
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CE0}, V_{EB} = 0$)		I_{CES}	—	20	μA_{dc}
Emitter Cutoff Current ($V_{BE} = 5 \text{ Vdc}, I_C = 0$)		I_{EBO}	—	1	mA_{dc}

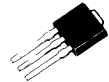
* These ratings are applicable when surface mounted on the minimum pad size recommended. (continued)
 (1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

NPN
MJD31,C
PNP
MJD32,C

SILICON
POWER TRANSISTORS
3 AMPERES
40 and 100 VOLTS
15 WATTS

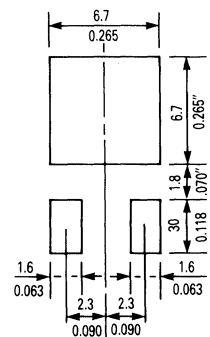


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES
RECOMMENDED FOR
SURFACE MOUNTED
APPLICATIONS



MJD31,C NPN, MJD32,C PNP

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 1 \text{ Adc}, V_{CE} = 4 \text{ Vdc}$) ($I_C = 3 \text{ Adc}, V_{CE} = 4 \text{ Vdc}$)	h_{FE}	25 10	— 50	—
Collector-Emitter Saturation Voltage ($I_C = 3 \text{ Adc}, I_B = 375 \text{ mAdc}$)	$V_{CE(sat)}$	—	1.2	Vdc
Base-Emitter On Voltage ($I_C = 3 \text{ Adc}, V_{CE} = 4 \text{ Vdc}$)	$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) ($I_C = 500 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f_{test} = 1 \text{ MHz}$)	f_T	3	—	MHz
Small-Signal Current Gain ($I_C = 0.5 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 1 \text{ kHz}$)	$ h_{fe} $	20	—	—

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.
 (2) $f_T = |h_{fe}| \cdot f_{test}$

OUTLINE DIMENSIONS

CASE 369-03

STYLE 1:
 PIN 1: BASE
 2: COLLECTOR
 3: EMITTER
 4: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC	—	0.090 BSC	—
J	0.46	0.58	0.018	0.023
K	0.89	0.95	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

NOTES
 1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
 2. POSITIONAL TOLERANCE FOR "D" DIAMETER:
 $\left[\begin{array}{c} \text{M} \\ \text{0.13 (0.005)} \end{array} \right] \text{ T}$
 3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 4. CONTROLLING DIMENSION: INCH

CASE 369A-04

STYLE 1:
 PIN 1: BASE
 2: COLLECTOR
 3: EMITTER
 4: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.89	0.025	0.035
G	4.98 BSC	—	0.195 BSC	—
H	2.29 BSC	—	0.090 BSC	—
J	6.46	6.58	0.018	0.023
K	2.99	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.92	—	0.170	—
Z	3.89	—	0.145	—

NOTES
 1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
 2. POSITIONAL TOLERANCE FOR "D" DIAMETER:
 $\left[\begin{array}{c} \text{M} \\ \text{0.13 (0.005)} \end{array} \right] \text{ T}$
 3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 4. CONTROLLING DIMENSION: INCH

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD31-1)



TYPICAL CHARACTERISTICS

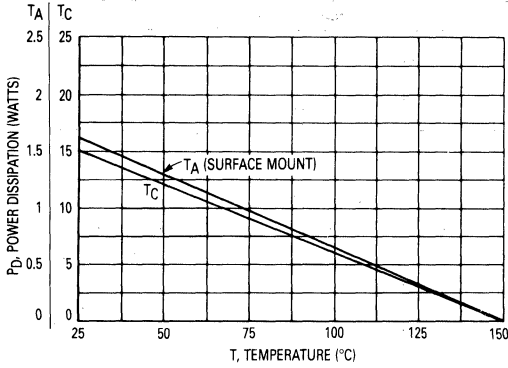
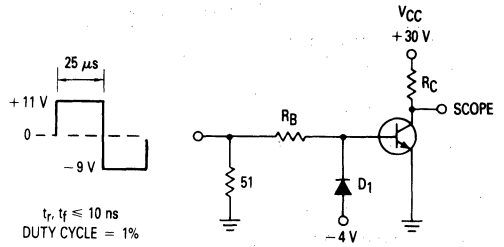


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
 MBD5300 USED ABOVE $I_B \approx 100$ mA
 MSD6100 USED BELOW $I_B \approx 100$ mA
 REVERSE ALL POLARITIES FOR PNP

Figure 2. Switching Time Test Circuit

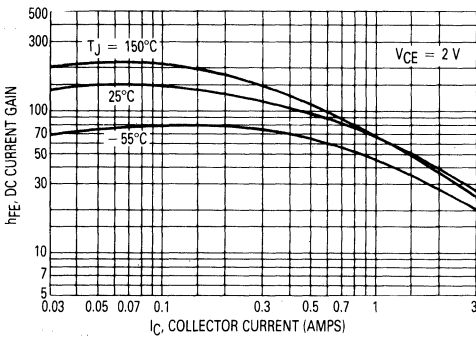


Figure 3. DC Current Gain

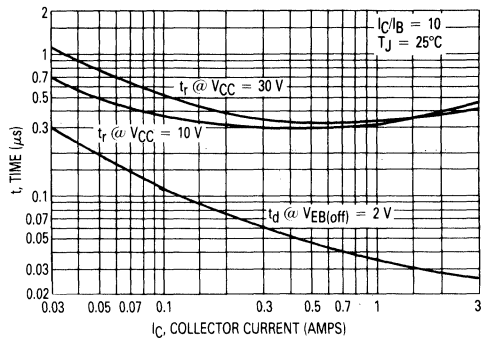


Figure 4. Turn-On Time

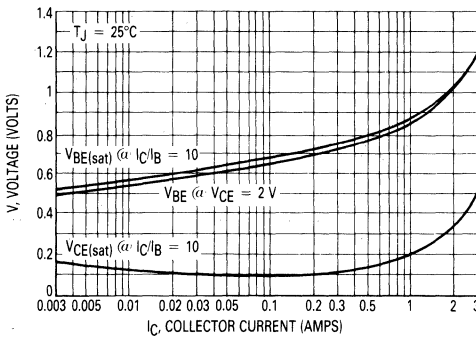


Figure 5. "On" Voltages

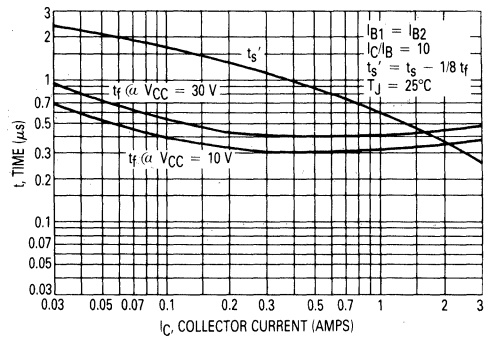


Figure 6. Turn-Off Time

3

MJD31,C NPN, MJD32,C PNP

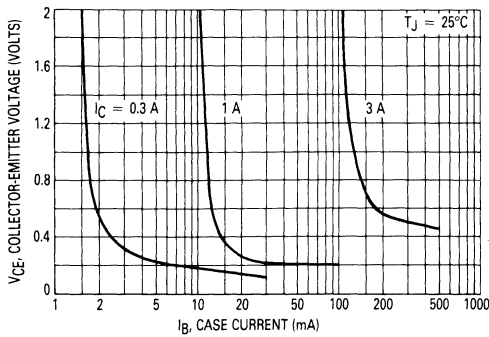


Figure 7. Collector Saturation Region

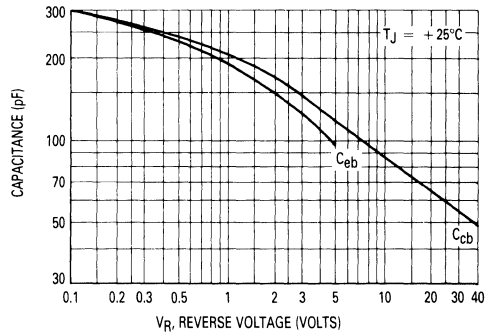


Figure 8. Capacitance

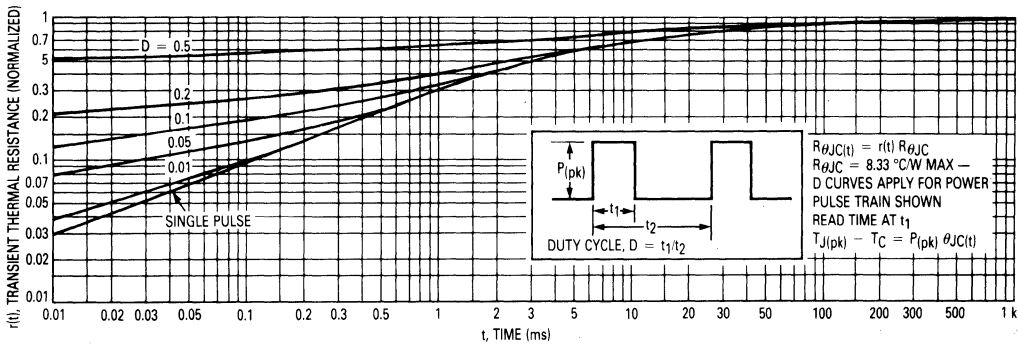


Figure 9. Thermal Response

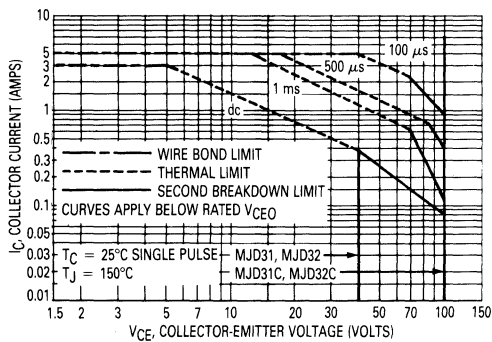


Figure 10. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Complementary Power Transistors

DKA For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Electrically Similar to Popular TIP41 and TIP42 Series
- Monolithic Construction With Built-in Base-Emitter Resistors

NPN
MJD41C
PNP
MJD42C

SILICON
POWER TRANSISTORS
6 AMPERES
100 VOLTS
20 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJD41C MJD42C	Unit
Collector-Emitter Voltage	V _{CEO}	100	Vdc
Collector-Base Voltage	V _{CB}	100	Vdc
Emitter-Base Voltage	V _{EB}	5	Vdc
Collector Current — Continuous Peak	I _C	6 10	Adc
Base Current	I _B	2	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	20 0.16	Watts W/°C
Total Power Dissipation* @ T _A = 25°C Derate above 25°C	P _D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	6.25	°C/W
Thermal Resistance, Junction to Ambient*	R _{θJA}	71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

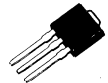
Collector-Emitter Sustaining Voltage (1) (I _C = 30 mA, I _B = 0)	V _{CEO(sus)}	100	—	Vdc
Collector Cutoff Current (V _{CE} = 60 Vdc, I _B = 0)	I _{CEO}	—	50	μAdc
Collector Cutoff Current (V _{CE} = 100 Vdc, V _{EB} = 0)	I _{CES}	—	10	μAdc
Emitter Cutoff Current (V _{BE} = 5 Vdc, I _C = 0)	I _{EBO}	—	0.5	mAdc

* These ratings are applicable when surface mounted on the minimum pad size recommended.
 (1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

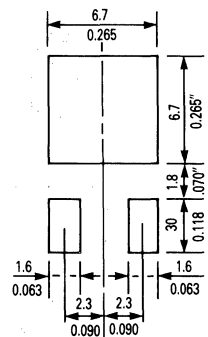


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



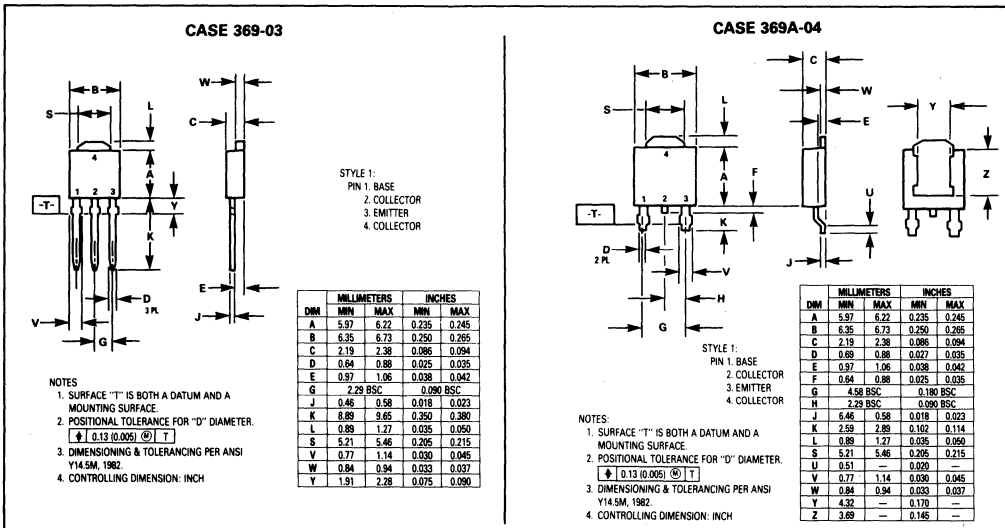
MJD41C NPN, MJD42C PNP

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 0.3 \text{ Adc}, V_{CE} = 4 \text{ Vdc}$) ($I_C = 3 \text{ Adc}, V_{CE} = 4 \text{ Vdc}$)	h_{FE}	30 15	— 75	—
Collector-Emitter Saturation Voltage ($I_C = 6 \text{ Adc}, I_B = 600 \text{ mAdc}$)	$V_{CE(sat)}$	—	1.5	Vdc
Base-Emitter On Voltage ($I_C = 6 \text{ Adc}, V_{CE} = 4 \text{ Vdc}$)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) ($I_C = 500 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f_{test} = 1 \text{ MHz}$)	f_T	3	—	MHz
Small-Signal Current Gain ($I_C = 0.5 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 1 \text{ kHz}$)	$ h_{fe} $	20	—	—

- (1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.
 (2) $f_T = |h_{fe}| \cdot f_{test}$

OUTLINE DIMENSIONS



Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD41C-1)

MJD41C NPN, MJD42C PNP

TYPICAL CHARACTERISTICS

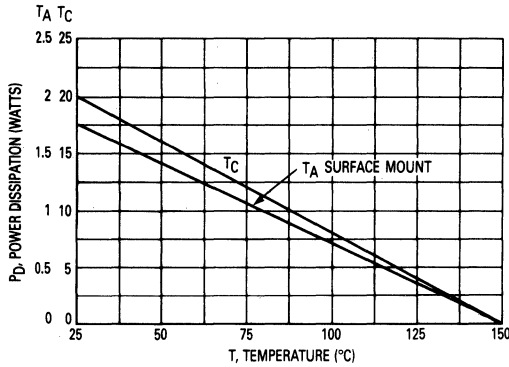
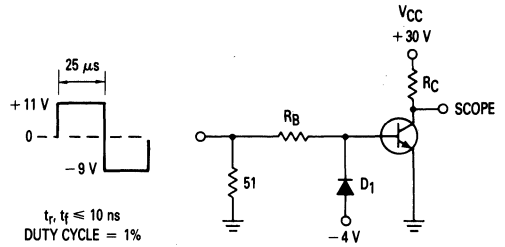


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
 MBD5300 USED ABOVE $I_B \approx 100$ mA
 MSD6100 USED BELOW $I_B \approx 100$ mA
 REVERSE ALL POLARITIES FOR PNP

Figure 2. Switching Time Test Circuit

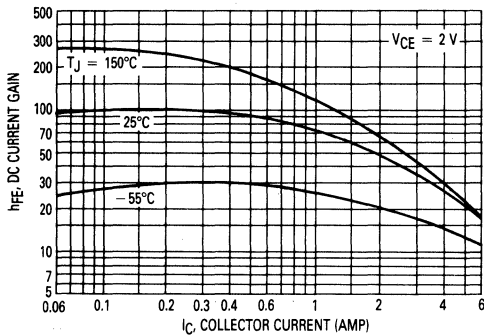


Figure 3. DC Current Gain

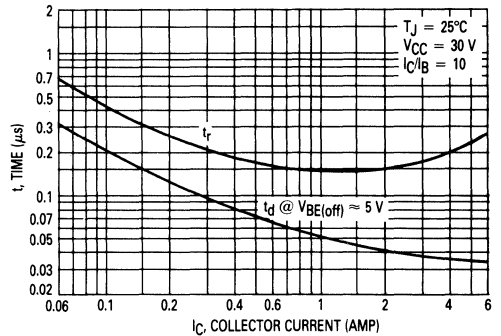


Figure 4. Turn-On Time

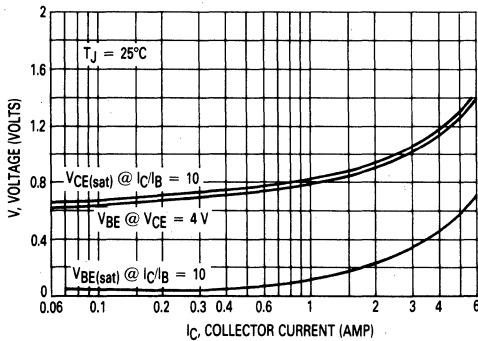


Figure 5. "On" Voltages

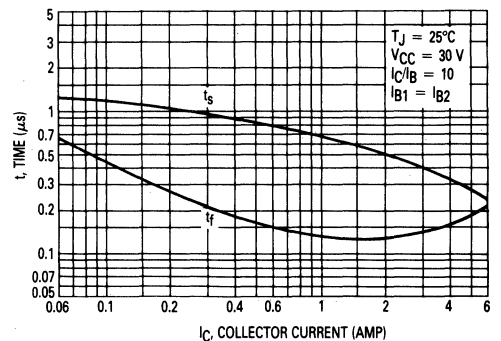


Figure 6. Turn-Off Time

MJD41C NPN, MJD42C PNP

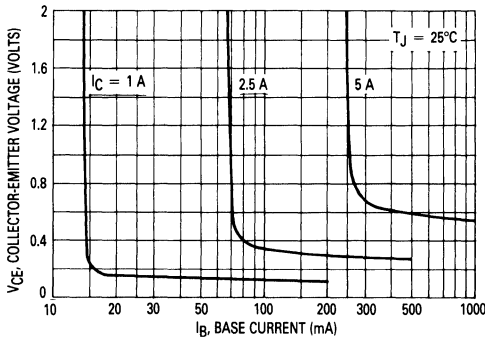


Figure 7. Collector Saturation Region

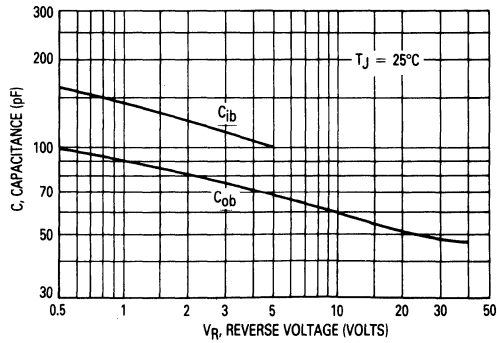


Figure 8. Capacitance

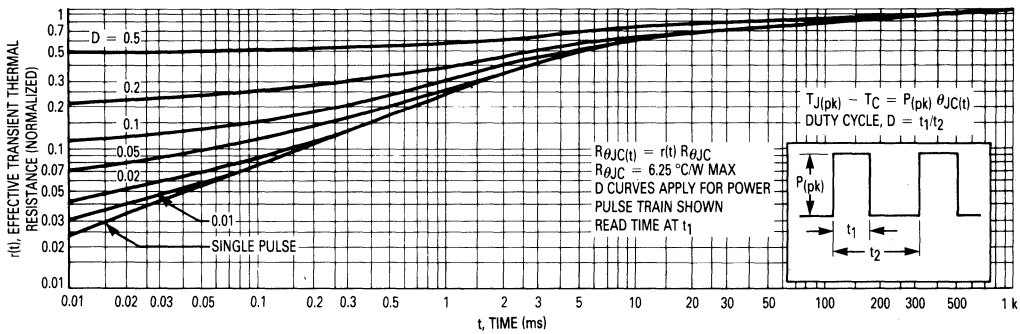


Figure 9. Thermal Response

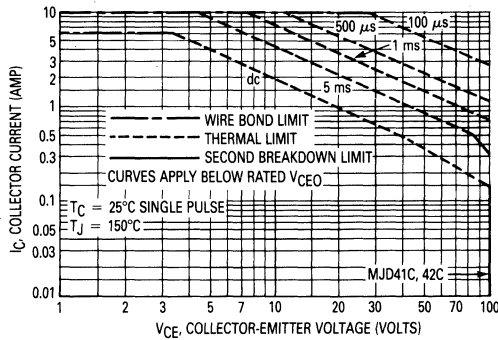


Figure 10. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



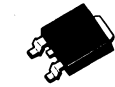
Complementary Power Transistors DPAK For Surface Mount Applications

... for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

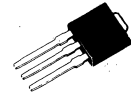
- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel for Surface Mount ("RL" Suffix)
- Electrically Similar to Popular D44H/D45H Series
- Low Collector Emitter Saturation Voltage — $V_{CE(sat)} = 1$ Volt Max @ 8 Amperes
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

NPN
MJD44H11
PNP
MJD45H11

SILICON
POWER TRANSISTORS
8 AMPERES
80 VOLTS
20 WATTS



CASE 369A-04



CASE 369-03

MAXIMUM RATINGS

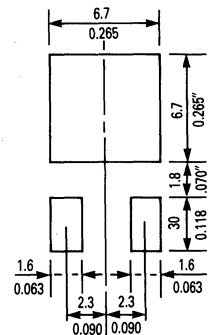
Rating	Symbol	D44H11 or D45H11	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous	I_C	8	Adc
Peak		16	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20	Watts W/°C
		0.16	
Total Power Dissipation (1) @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.75	Watts W/°C
		0.014	
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	°C/W
Lead Temperature for Soldering	T_L	260	°C

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MJD44H11 NPN, MJD45H11 PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (I _C = 30 mA, I _B = 0)	V _{CEO(sus)}	80	—	—	Vdc
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , V _{BE} = 0)	I _{CES}	—	—	10	μA
Emitter Cutoff Current (V _{EB} = 5 Vdc)	I _{EBO}	—	—	50	μA

ON CHARACTERISTICS

Collector-Emitter Saturation Voltage (I _C = 8 Adc, I _B = 0.4 Adc)	V _{CE(sat)}	—	—	1	Vdc
Base-Emitter Saturation Voltage (I _C = 8 Adc, I _B = 0.8 Adc)	V _{BE(sat)}	—	—	1.5	Vdc
DC Current Gain (V _{CE} = 1 Vdc, I _C = 2 Adc)	h _{FE}	60	—	—	—
DC Current Gain (V _{CE} = 1 Vdc, I _C = 4 Adc)		40	—	—	—

DYNAMIC CHARACTERISTICS

Collector Capacitance (V _{CB} = 10 Vdc, f _{test} = 1 MHz)	MJD44H11 MJD45H11	C _{cb}	—	130 230	—	pF
Gain Bandwidth Product (I _C = 0.5 Adc, V _{CE} = 10 Vdc, f = 20 MHz)	MJD44H11 MJD45H11	f _T	—	50 40	—	MHz

SWITCHING TIMES

Delay and Rise Times (I _C = 5 Adc, I _{B1} = 0.5 Adc)	MJD44H11 MJD45H11	t _d + t _r	—	300 135	—	ns
Storage Time (I _C = 5 Adc, I _{B1} = I _{B2} = 0.5 Adc)	MJD44H11 MJD45H11	t _s	—	500 500	—	ns
Fall Time (I _C = 5 Adc, I _{B1} = I _{B2} = 0.5 Adc)	MJD44H11 MJD45H11	t _f	—	140 100	—	ns

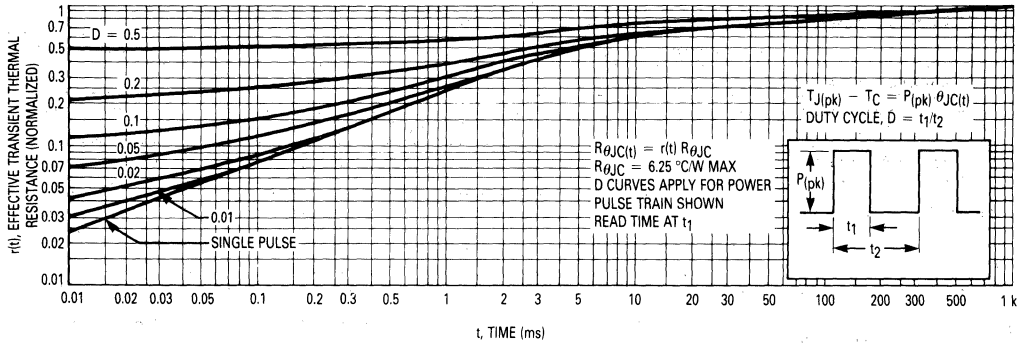


Figure 1. Thermal Response

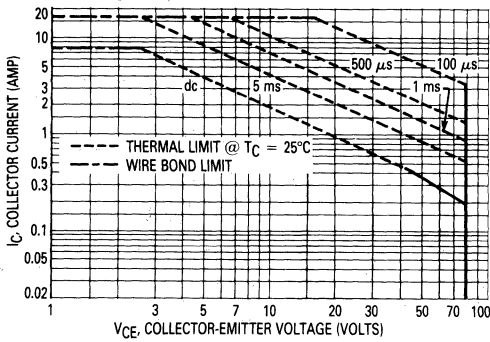


Figure 2. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

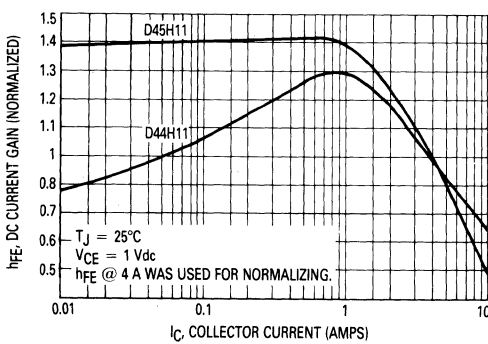


Figure 3. Normalized DC Current Gain

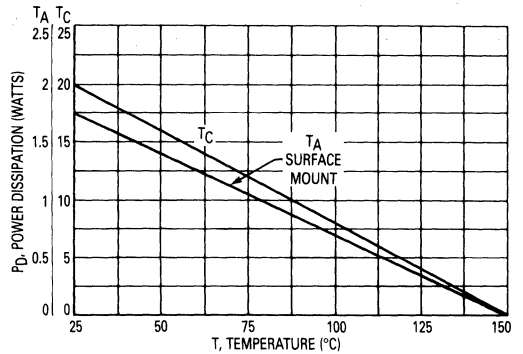
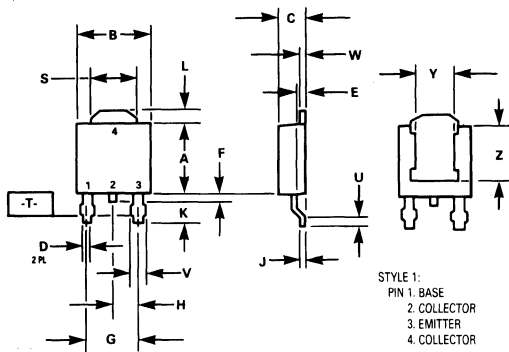


Figure 4. Power Derating

3

MJD44H11 NPN, MJD45H11 PNP

OUTLINE DIMENSIONS



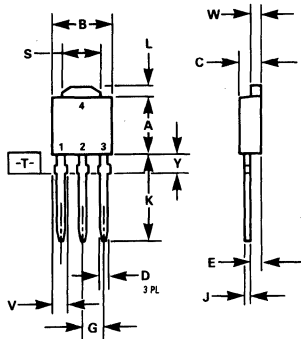
STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 369A-04

NOTES:

1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
 $\pm 0.13 (0.005) \text{ (M) T}$
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—



NOTES:

1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
 $\pm 0.13 (0.005) \text{ (M) T}$
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 369-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD44H11-1)

High Voltage Power Transistors

DPAK For Surface Mount Applications

Designed for line operated audio output amplifier, switchmode power supply drivers and other switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Electrically Similar to Popular TIP47, and TIP50
- 250 and 400 V (Min) — $V_{CE(sus)}$
- 1 A Rated Collector Current

MAXIMUM RATINGS

Rating	Symbol	MJD47	MJD50	Unit
Collector-Emitter Voltage	V_{CEO}	250	400	Vdc
Collector-Base Voltage	V_{CB}	350	500	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak	I_C	1	2	Adc
Base Current	I_B	0.6		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	15	0.12	Watts W $^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.56	0.0125	Watts W $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	$^\circ\text{C/W}$
Lead Temperature for Soldering Purpose	T_L	260	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 30 \text{ mAdc}, I_B = 0$)	MJD47 MJD50	$V_{CE(sus)}$	250 400	—	Vdc
Collector Cutoff Current ($V_{CE} = 150 \text{ Vdc}, I_B = 0$) ($V_{CE} = 300 \text{ Vdc}, I_B = 0$)	MJD47 MJD50	I_{CEO}	— —	0.2 0.2	mAdc

* When surface mounted on minimum pad sizes recommended.
 (1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

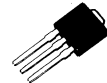
(continued)

MJD47
MJD50

NPN SILICON
POWER TRANSISTORS
1 AMPERE
250, 400 VOLTS
15 WATTS

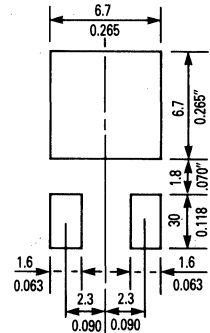


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MJD47, MJD50

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS — continued

Collector Cutoff Current ($V_{CE} = 350\text{ Vdc}, V_{BE} = 0$) ($V_{CE} = 500\text{ Vdc}, V_{BE} = 0$)	MJD47 MJD50	I_{CES}	— —	0.1 0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5\text{ Vdc}, I_C = 0$)		I_{EBO}	—	1	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 0.3\text{ Adc}, V_{CE} = 10\text{ Vdc}$) ($I_C = 1\text{ Adc}, V_{CE} = 10\text{ Vdc}$)	h_{FE}	30 10	150 —	—
Collector-Emitter Saturation Voltage ($I_C = 1\text{ Adc}, I_B = 0.2\text{ Adc}$)	$V_{CE(sat)}$	—	1	Vdc
Base-Emitter On Voltage ($I_C = 1\text{ Adc}, V_{CE} = 10\text{ Vdc}$)	$V_{BE(on)}$	—	1.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ($I_C = 0.2\text{ Adc}, V_{CE} = 10\text{ Vdc}, f = 2\text{ MHz}$)	f_T	10	—	MHz
Small-Signal Current Gain ($I_C = 0.2\text{ Adc}, V_{CE} = 10\text{ Vdc}, f = 1\text{ kHz}$)	h_{fe}	25	—	—

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

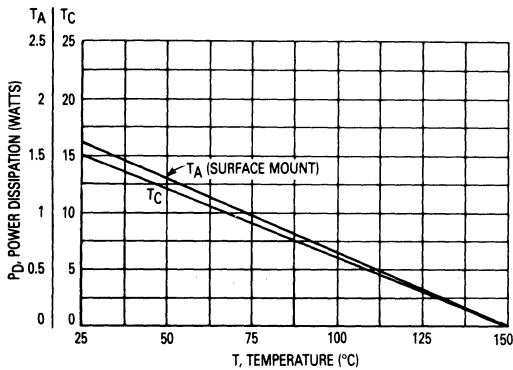


Figure 1. Power Derating

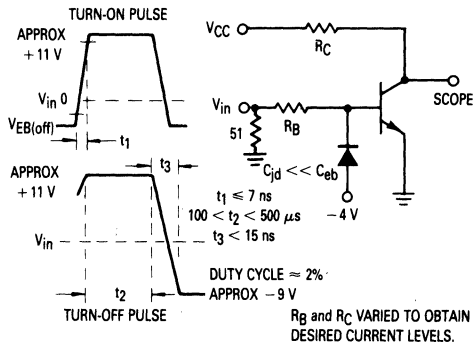


Figure 2. Switching Time Equivalent Circuit

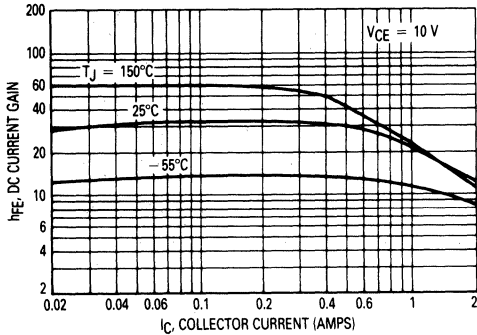


Figure 3. DC Current Gain

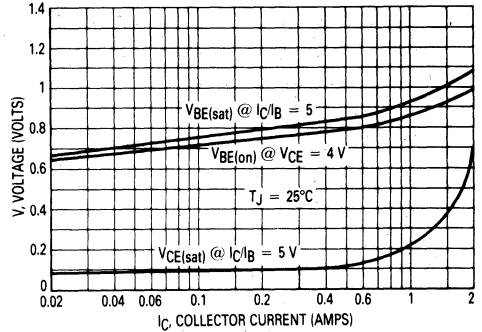


Figure 4. "On" Voltages

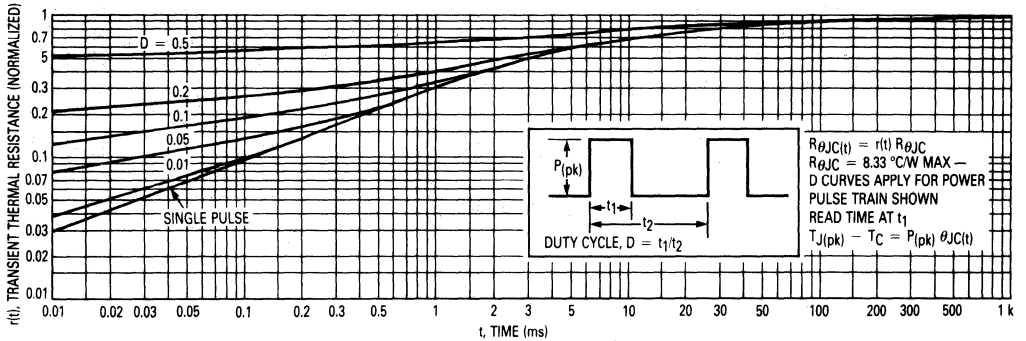


Figure 5. Thermal Response

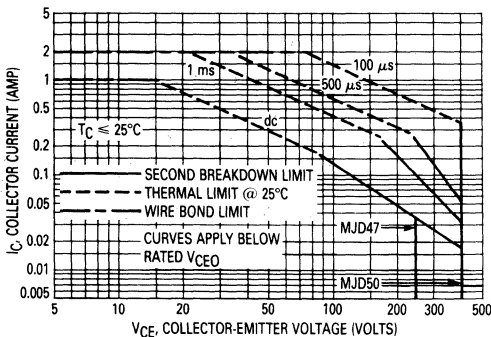


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

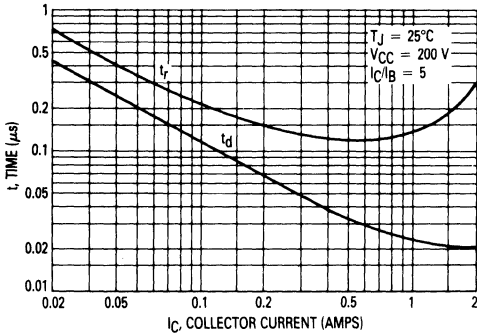


Figure 7. Turn-On Time

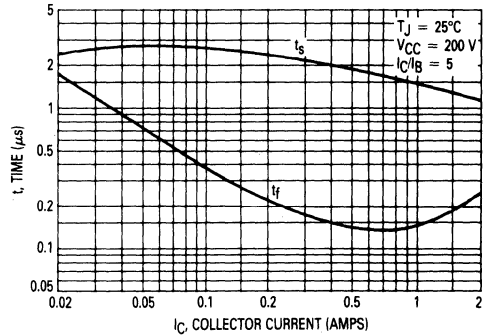


Figure 8. Turn-Off Time

OUTLINE DIMENSIONS

CASE 369-03

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.32	0.235	0.246
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.88	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.94	0.94	0.037	0.037
Y	1.91	2.28	0.075	0.090

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER: $\pm 0.13 (0.005) \text{ @ } T$
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

CASE 369A-04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.32	0.235	0.246
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.68	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	6.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.88	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.94	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.146	—

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER: $\pm 0.13 (0.005) \text{ @ } T$
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD47-1)

Complementary Darlington Power Transistors

DPAK For Surface Mount Applications

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Surface Mount Replacements for TIP110-TIP117 Series
- Monolithic Construction With Built-in Base-Emitter Shunt Resistors
- High DC Current Gain — $h_{FE} = 2500$ (Typ) @ $I_C = 2$ Adc
- Complementary Pairs Simplifies Designs

MAXIMUM RATINGS

Rating	Symbol	MJD112 MJD117	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	2 4	Adc
Base Current	I_B	50	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20 0.16	Watts W/ $^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.75 0.014	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 30$ mAdc, $I_B = 0$)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current ($V_{CE} = 50$ Vdc, $I_B = 0$)	I_{CEO}	—	20	μAdc
Collector Cutoff Current ($V_{CB} = 100$ Vdc, $I_E = 0$)	I_{CBO}	—	20	μAdc
Emitter Cutoff Current ($V_{BE} = 5$ Vdc, $I_C = 0$)	I_{EBO}	—	2	mAdc

* These ratings are applicable when surface mounted on the minimum pad sizes recommended.
 (1) Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.

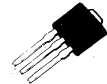
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NPN
MJD112
PNP
MJD117

SILICON
POWER TRANSISTORS
2 AMPERES
100 VOLTS
20 WATTS

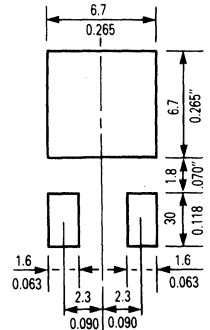


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MJD112 NPN, MJD117 PNP

*ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued				
Collector-Cutoff Current ($V_{CE} = 80\text{ Vdc}$, $V_{BE(\text{off})} = 1.5\text{ Vdc}$) ($V_{CE} = 80\text{ Vdc}$, $V_{BE(\text{off})} = 1.5\text{ Vdc}$, $T_C = 125^\circ\text{C}$)	I_{CEX}	—	10 500	μAdc
Collector-Cutoff Current ($V_{CB} = 80\text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	10	μAdc
Emitter-Cutoff Current ($V_{BE} = 5\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	2	mAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 3\text{ Vdc}$) ($I_C = 2\text{ Adc}$, $V_{CE} = 3\text{ Vdc}$) ($I_C = 4\text{ Adc}$, $V_{CE} = 3\text{ Vdc}$)	h_{FE}	500 1000 200	— 12,000 —	—
Collector-Emitter Saturation Voltage ($I_C = 2\text{ Adc}$, $I_B = 8\text{ mAdc}$) ($I_C = 4\text{ Adc}$, $I_B = 40\text{ mAdc}$)	$V_{CE(\text{sat})}$	— —	2 3	Vdc
Base-Emitter Saturation Voltage ($I_C = 4\text{ Adc}$, $I_B = 40\text{ mAdc}$)	$V_{BE(\text{sat})}$	—	4	Vdc
Base-Emitter On Voltage ($I_C = 2\text{ Adc}$, $V_{CE} = 3\text{ Vdc}$)	$V_{BE(\text{on})}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product ($I_C = 0.75\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ MHz}$)	f_T	25	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	— —	200 100	pF
	MJD117 MJD112			

*Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

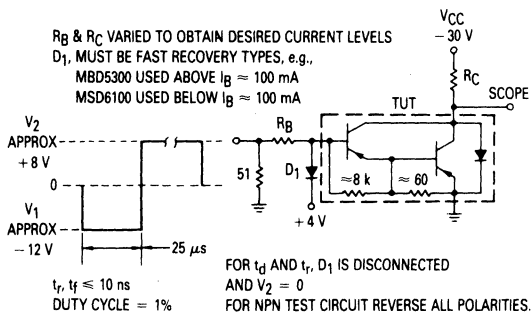


Figure 1. Switching Times Test Circuit

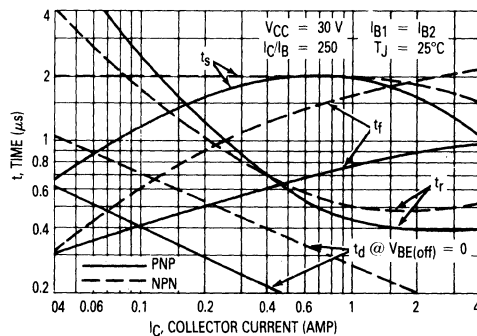


Figure 2. Switching Times

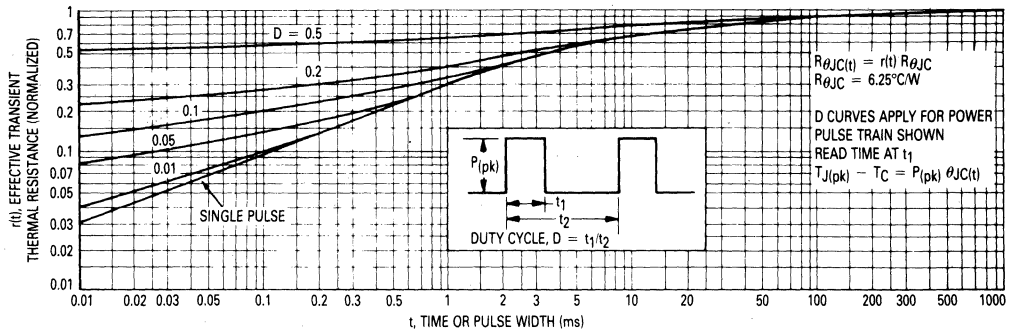


Figure 3. Thermal Response

ACTIVE-REGION SAFE-OPERATING AREA

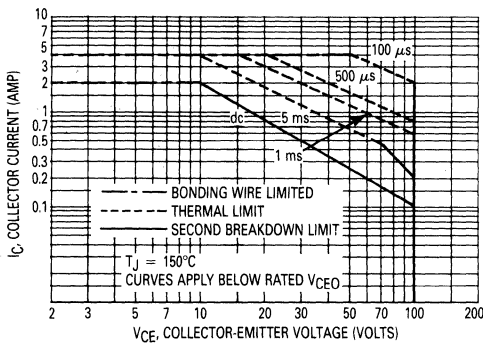


Figure 4. Maximum Rated Forward Biased Safe Operating Area

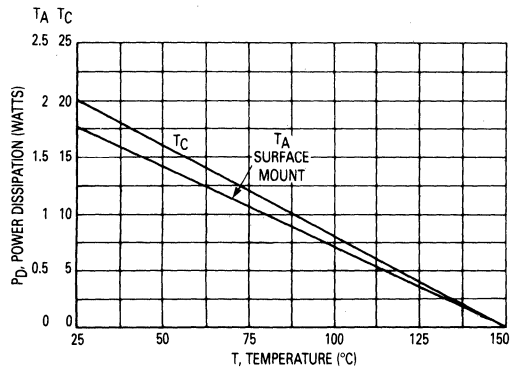


Figure 5. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

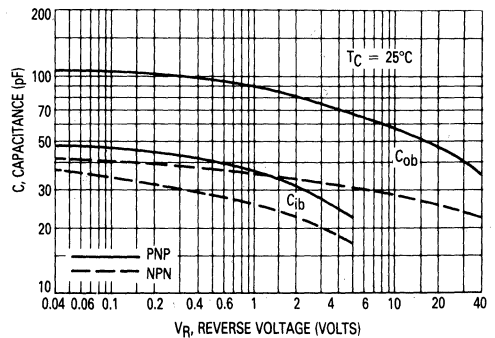


Figure 6. Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS

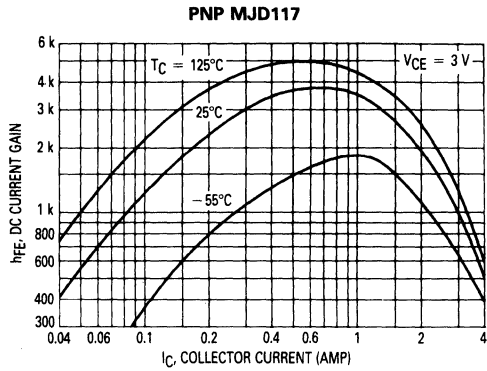
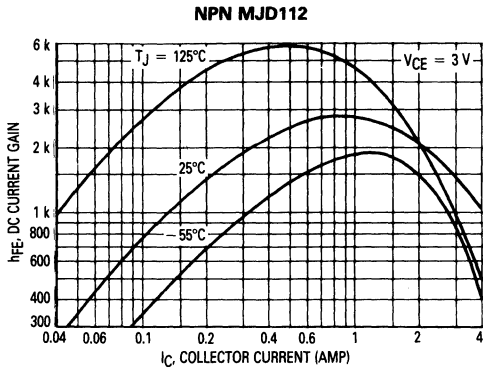


Figure 7. DC Current Gain

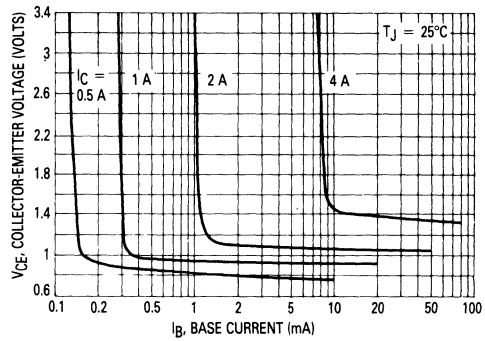
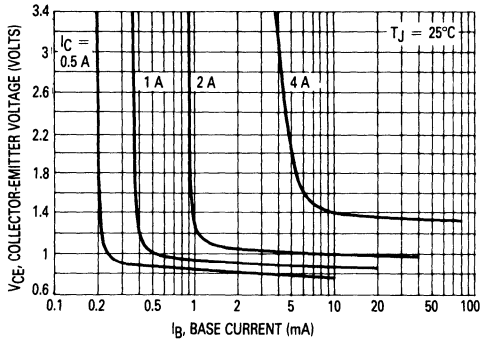


Figure 8. Collector Saturation Region

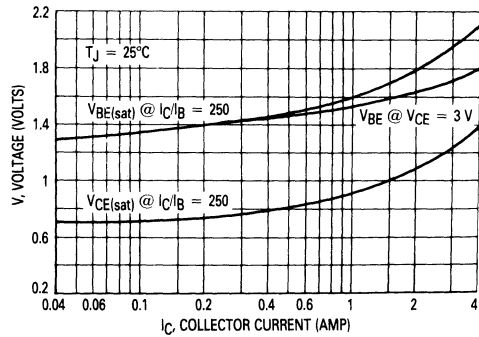
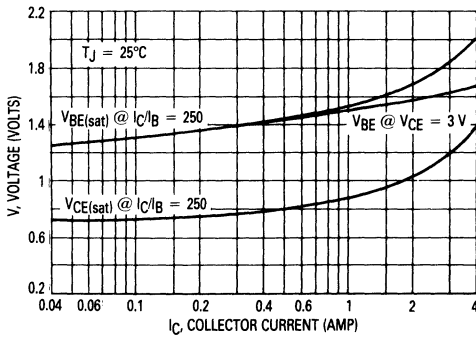


Figure 9. "On" Voltages

MJD112 NPN, MJD117 PNP

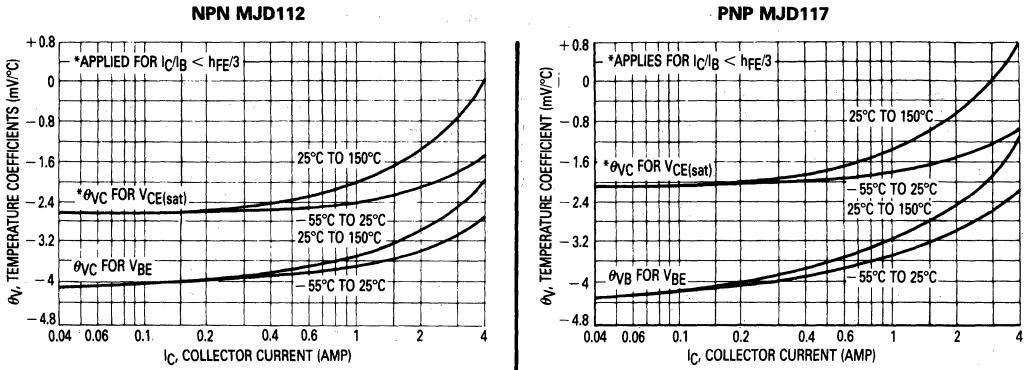


Figure 10. Temperature Coefficients

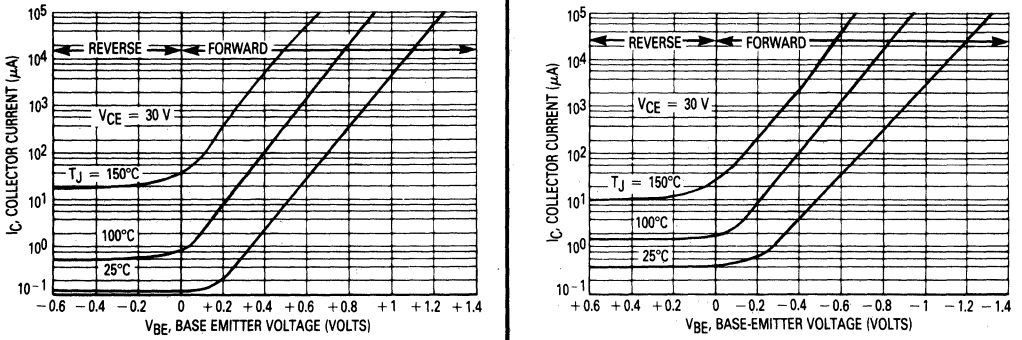


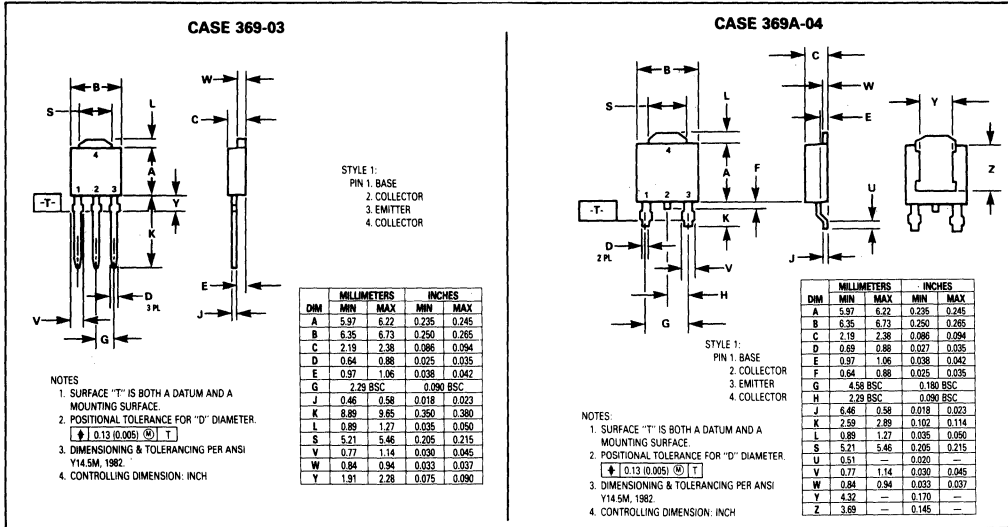
Figure 11. Collector Cut-Off Region

3



Figure 12. Darlington Schematic

OUTLINE DIMENSIONS



Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD112-1)

Complementary Darlington Power Transistors DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("1" Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel ("RL" Suffix)
- Surface Mount Replacements for 2N6040-2N6045 Series, TIP120-TIP122 Series, and TIP125-TIP127 Series
- Monolithic Construction With Built-in Base-Emitter Shunt Resistors
- High DC Current Gain — $h_{FE} = 2500$ (Typ) @ $I_C = 4$ Adc
- Complementary Pairs Simplifies Designs

MAXIMUM RATINGS

Rating	Symbol	MJD122 MJD127	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	8 16	Adc
Base Current	I_B	120	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20 0.16	Watts W/ $^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.75 0.014	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 30$ mAdc, $I_B = 0$)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current ($V_{CE} = 50$ Vdc, $I_B = 0$)	I_{CEO}	—	10	μAdc

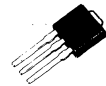
* These ratings are applicable when surface mounted on the minimum pad sizes recommended. (continued)

NPN
MJD122
PNP
MJD127

SILICON
POWER TRANSISTORS
8 AMPERES
100 VOLTS
20 WATTS

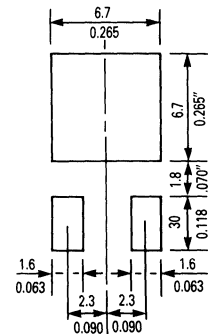


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MJD122 NPN, MJD127 PNP

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued				
Collector Cutoff Current ($V_{CE} = 100\text{ Vdc}$, $V_{BE(\text{off})} = 1.5\text{ Vdc}$) ($V_{CE} = 100\text{ Vdc}$, $V_{BE(\text{off})} = 1.5\text{ Vdc}$, $T_C = 125^\circ\text{C}$)	I_{CEX}	—	10 500	μAdc
Collector Cutoff Current ($V_{CB} = 100\text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current ($V_{BE} = 5\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	2	mAdc

ON CHARACTERISTICS

DC Current Gain ($I_C = 4\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$) ($I_C = 8\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$)	h_{FE}	1000 100	12,000 —	—
Collector-Emitter Saturation Voltage ($I_C = 4\text{ Adc}$, $I_B = 16\text{ mAdc}$) ($I_C = 8\text{ Adc}$, $I_B = 80\text{ mAdc}$)	$V_{CE(\text{sat})}$	— —	2 4	Vdc
Base-Emitter Saturation Voltage (1) ($I_C = 8\text{ Adc}$, $I_B = 80\text{ mAdc}$)	$V_{BE(\text{sat})}$	—	4.5	Vdc
Base-Emitter On Voltage ($I_C = 4\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$)	$V_{BE(\text{on})}$	—	2.8	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 3\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$, $f = 1\text{ MHz}$)	$ h_{fe} $	4	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	— —	300 200	pF
Small-Signal Current Gain ($I_C = 3\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$, $f = 1\text{ kHz}$)	h_{fe}	300	—	—

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

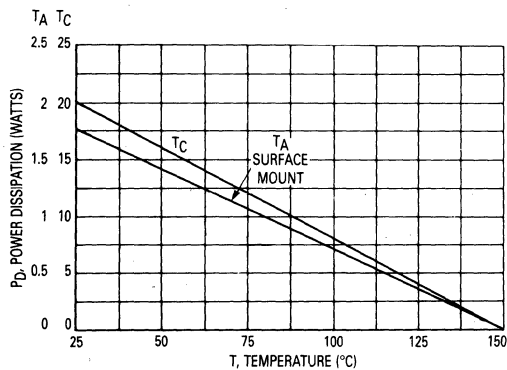


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

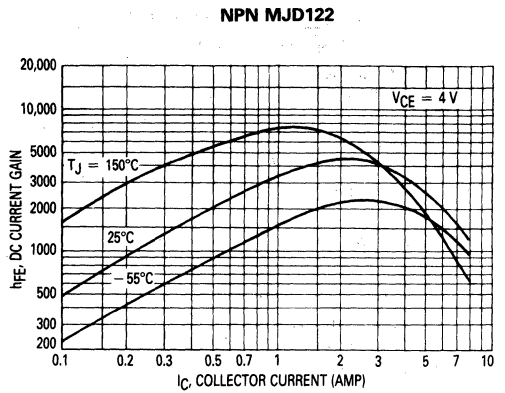
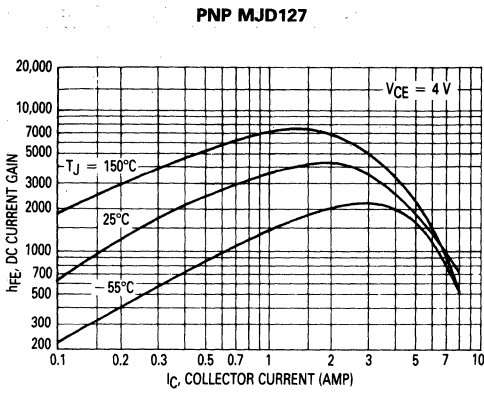


Figure 2. DC Current Gain

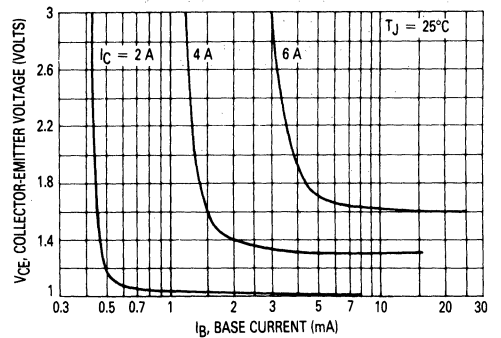
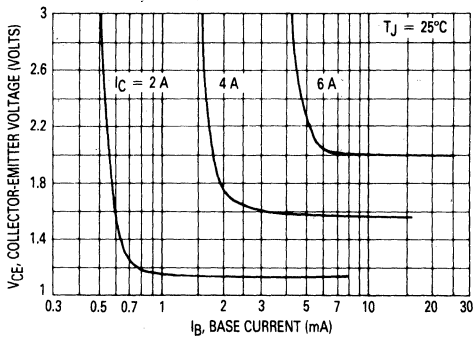


Figure 3. Collector Saturation Region

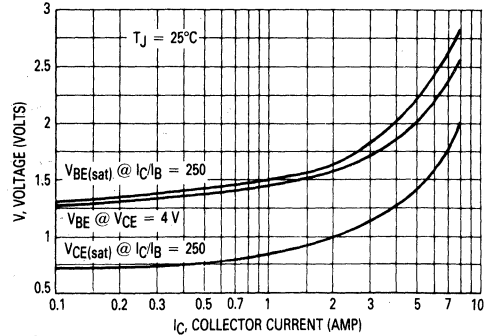
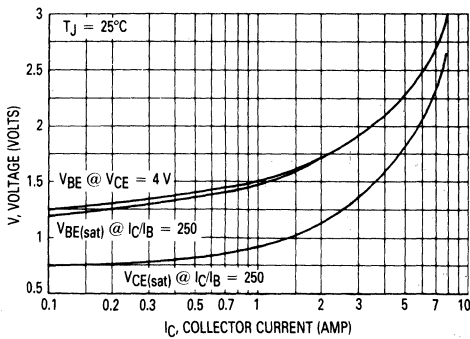
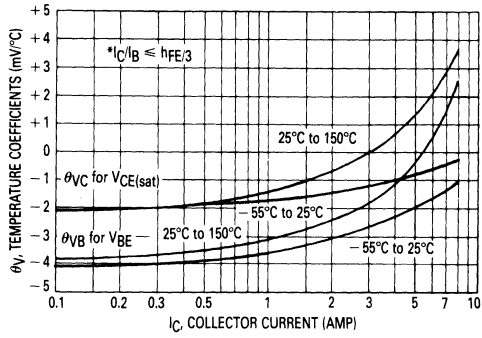


Figure 4. "On" Voltages

MJD122 NPN, MJD127 PNP

TYPICAL ELECTRICAL CHARACTERISTICS

PNP MJD127



NPN MJD122

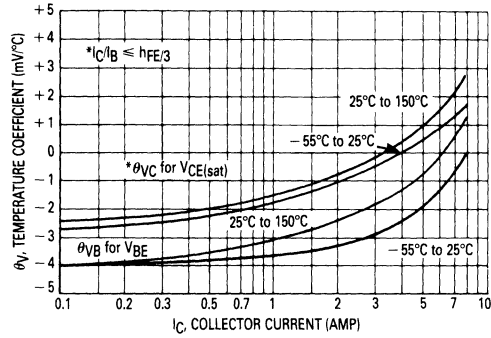


Figure 5. Temperature Coefficients

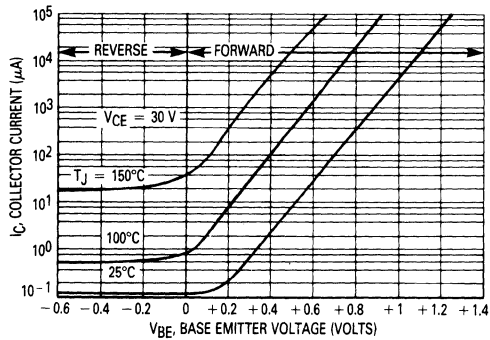
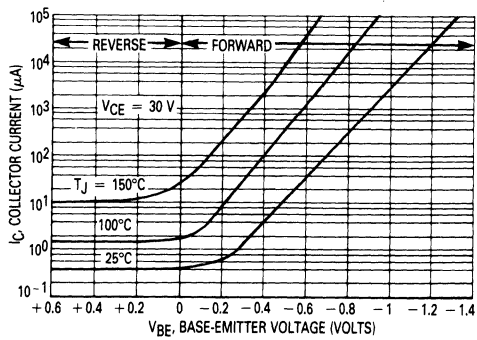


Figure 6. Collector Cut-Off Region

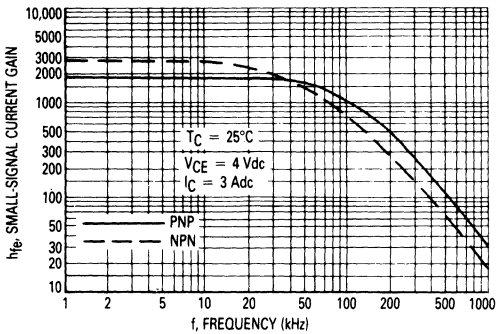


Figure 7. Small-Signal Current Gain

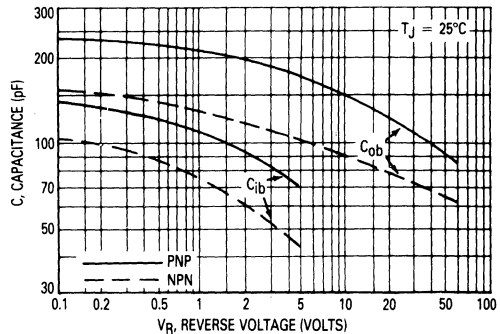


Figure 8. Capacitance

MJD122 NPN, MJD127 PNP

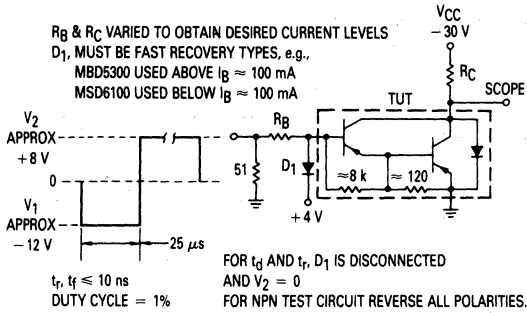


Figure 9. Switching Times Test Circuit

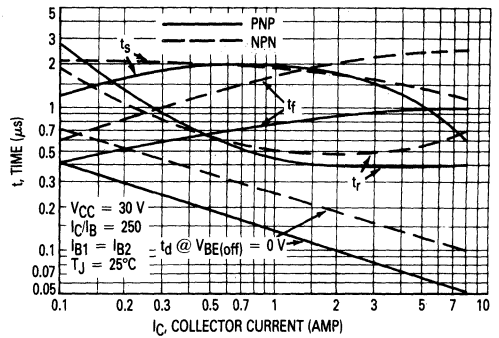


Figure 10. Switching Times

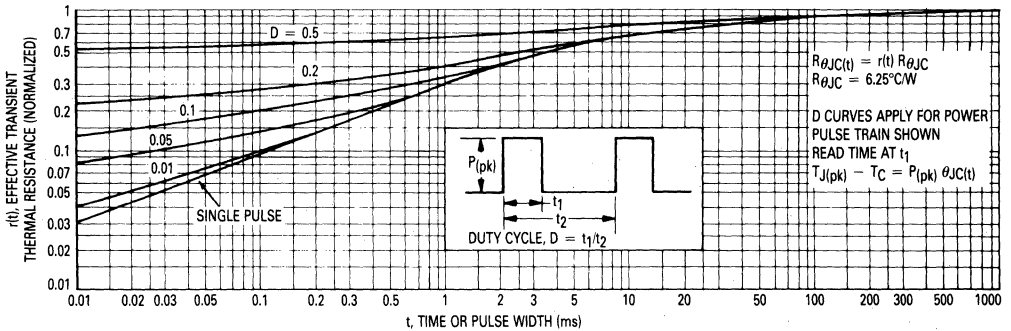


Figure 11. Thermal Response

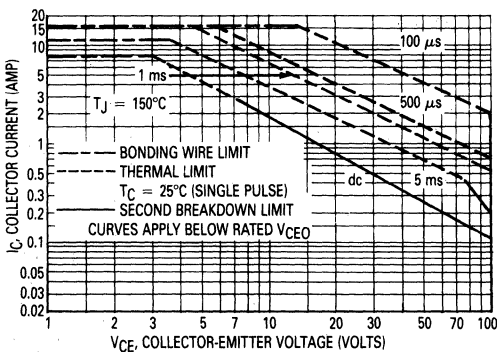


Figure 12. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

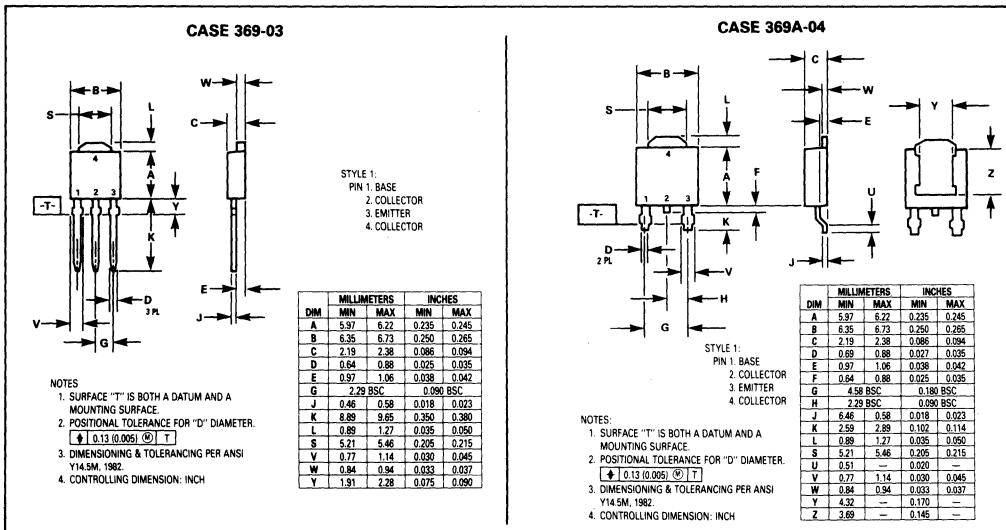
The data of Figure 12 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJD122 NPN, MJD127 PNP



Figure 13. Darlington Schematic

OUTLINE DIMENSIONS



Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD122-1)



Complementary
Plastic Power Transistors
NPN/PNP Silicon
DPAK For Surface Mount Applications

... designed for low voltage, low-power, high-gain audio amplifier applications.

- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)} = 25 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain — $h_{FE} = 70 \text{ (Min) @ } I_C = 500 \text{ mAdc}$
 $= 45 \text{ (Min) @ } I_C = 2 \text{ Adc}$
 $= 10 \text{ (Min) @ } I_C = 5 \text{ Adc}$
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$
 $= 0.75 \text{ Vdc (Max) @ } I_C = 2 \text{ Adc}$
- High Current-Gain — Bandwidth Product — $f_T = 65 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- Annular Construction for Low Leakage — $I_{CBO} = 100 \text{ nAdc @ Rated } V_{CB}$

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	40	Vdc
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Emitter-Base Voltage	V_{EB}	8	Vdc
Collector Current — Continuous Peak	I_C	5 10	Adc
Base Current	I_B	1	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	12.5 0.1	Watts W/°C
Total Device Dissipation @ $T_A = 25^\circ\text{C}^*$ Derate above 25°C	P_D	1.4 0.011	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W
Junction to Ambient*	$R_{\theta JA}$	89.3	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 10 \text{ mAdc}, I_B = 0$)	$V_{CEO(sus)}$	25	—	Vdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}, I_E = 0$) ($V_{CB} = 40 \text{ Vdc}, I_E = 0, T_J = 125^\circ\text{C}$)	I_{CBO}	—	100 100	nAdc μAdc
Emitter Cutoff Current ($V_{BE} = 8 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	100	nAdc

* When surface mounted on minimum pad sizes recommended.
 (1) Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

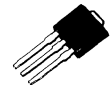
(continued)

NPN
MJD200
PNP
MJD210

SILICON
POWER TRANSISTORS
5 AMPERES
25 VOLTS
12.5 WATTS

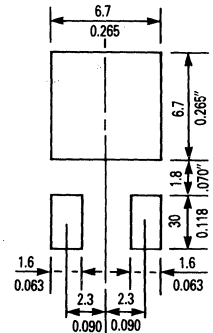


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES
RECOMMENDED FOR
SURFACE MOUNTED
APPLICATIONS



MJD200 NPN, MJD210 PNP

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 1 \text{ Vdc}$) ($I_C = 2 \text{ Adc}$, $V_{CE} = 1 \text{ Vdc}$) ($I_C = 5 \text{ Adc}$, $V_{CE} = 2 \text{ Vdc}$)	h_{FE}	70 45 10	— 180 —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 500 \text{ mAdc}$, $I_B = 50 \text{ mAdc}$) ($I_C = 2 \text{ Adc}$, $I_B = 200 \text{ mAdc}$) ($I_C = 5 \text{ Adc}$, $I_B = 1 \text{ Adc}$)	$V_{CE(sat)}$	— — —	0.3 0.75 1.8	Vdc
Base-Emitter Saturation Voltage (1) ($I_C = 5 \text{ Adc}$, $I_B = 1 \text{ Adc}$)	$V_{BE(sat)}$	—	2.5	Vdc
Base-Emitter On Voltage (1) ($I_C = 2 \text{ Adc}$, $V_{CE} = 1 \text{ Vdc}$)	$V_{BE(on)}$	—	1.6	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product (2) ($I_C = 100 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 10 \text{ MHz}$)	f_T	65	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	— —	80 120	pF
	MJD200 MJD210			

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

(2) $f_T = |h_{FE}| \cdot f_{test}$

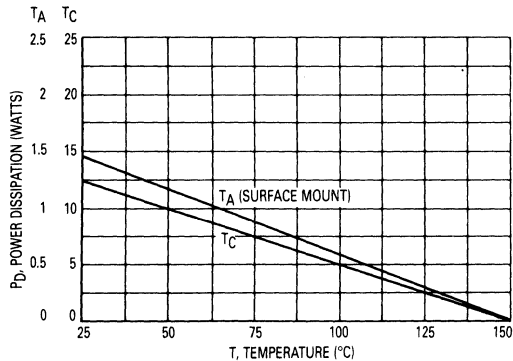


Figure 1. Power Derating

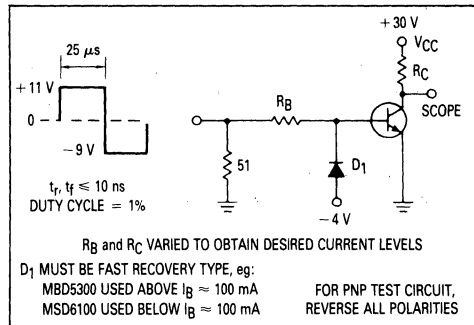


Figure 2. Switching Time Test Circuit

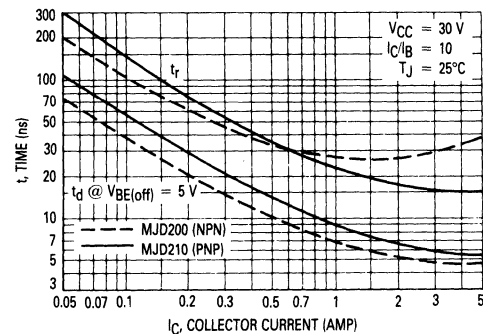


Figure 3. Turn-On Time

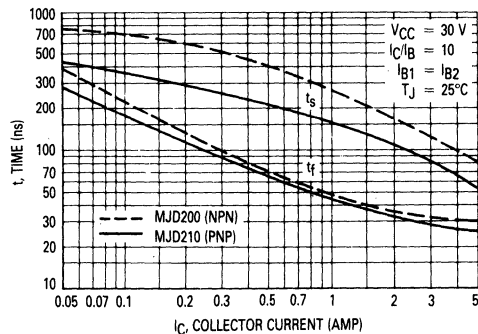


Figure 4. Turn-Off Time

MJD200 NPN, MJD210 PNP

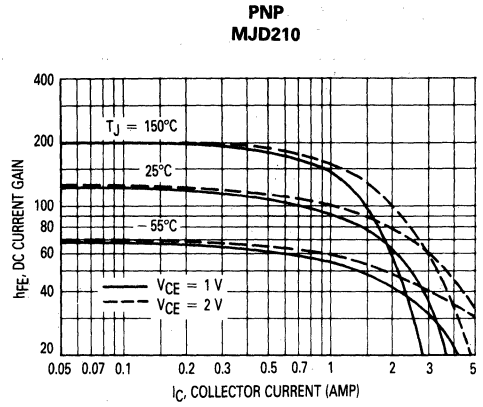
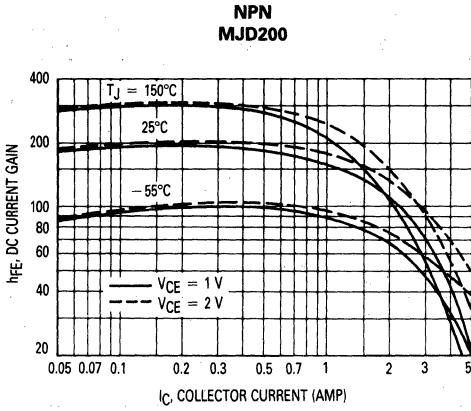


Figure 5. DC Current Gain

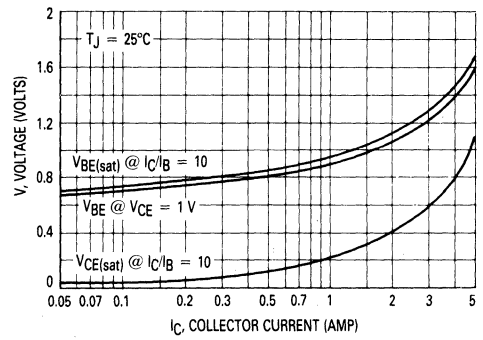
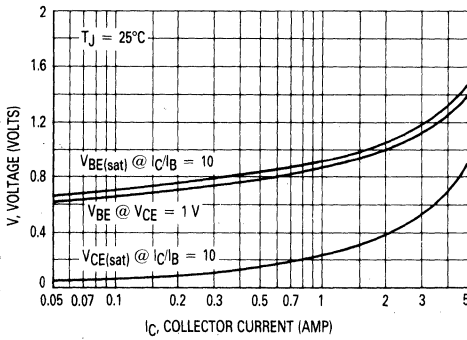


Figure 6. "On" Voltage

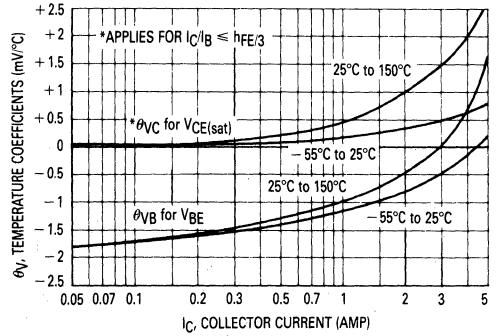
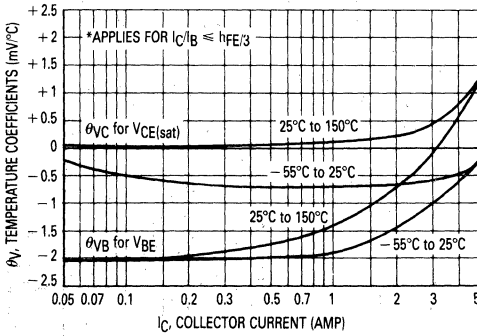


Figure 7. Temperature Coefficients

MJD200 NPN, MJD210 PNP

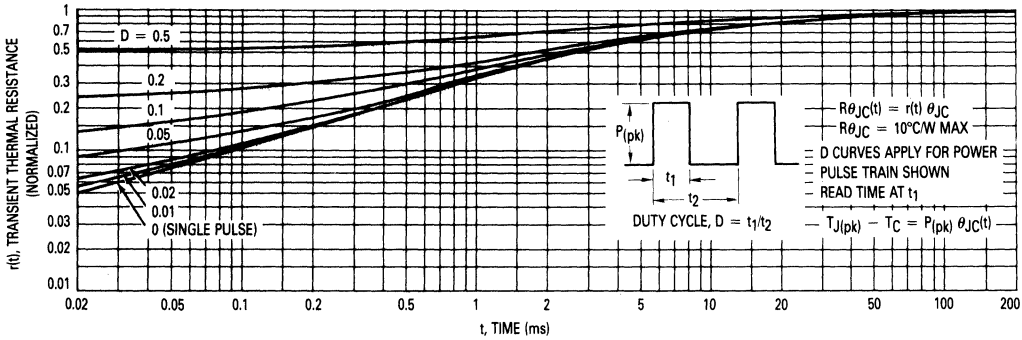


Figure 8. Thermal Response

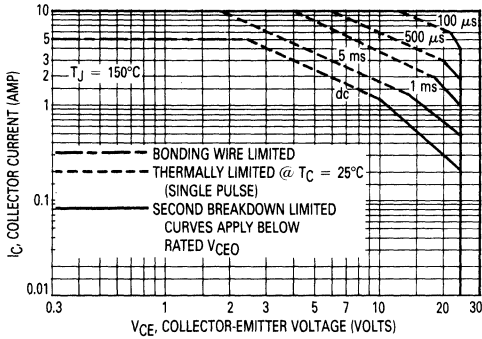


Figure 9. Active Region Safe Operating Area

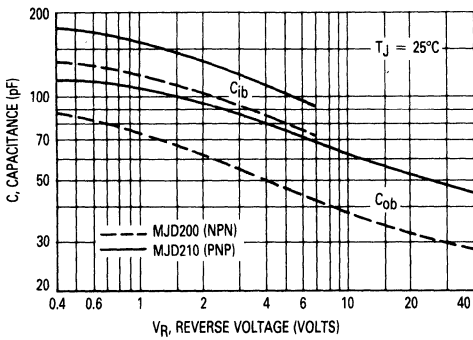
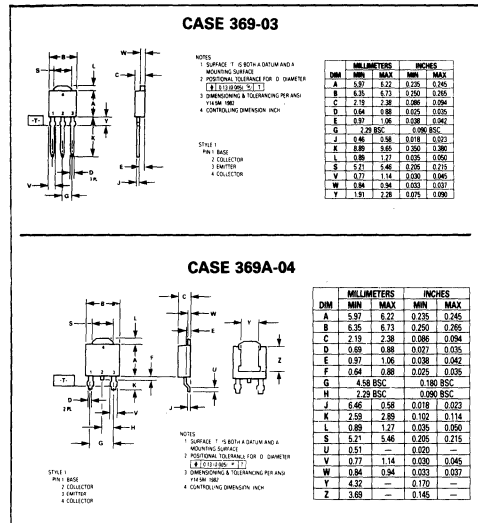


Figure 10. Capacitance

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

OUTLINE DIMENSIONS



Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD200-1)

High Voltage Power Transistors DPAK For Surface Mount Applications

Designed for line operated audio output amplifier, switchmode power supply drivers and other switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Electrically Similar to Popular MJE340 and MJE350
- 300 V (Min) — $V_{CEO(sus)}$
- 0.5 A Rated Collector Current

NPN
MJD340

PNP
MJD350

SILICON
POWER TRANSISTORS
0.5 AMPERE
300 VOLTS
15 WATTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	3	Vdc
Collector Current — Continuous — Peak	I_C	0.5 0.75	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	15 0.12	Watts $W^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.56 0.012	Watts $W^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	$^\circ\text{C/W}$
Lead Temperature for Soldering Purpose	T_L	260	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 1 \text{ mAdc}, I_B = 0$)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current ($V_{CB} = 300 \text{ Vdc}, I_E = 0$)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 3 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	0.1	mAdc

ON CHARACTERISTICS (1)

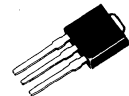
DC Current Gain ($I_C = 50 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$)	h_{FE}	30	240	—
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* When surface mounted on minimum pad sizes recommended.
 (1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

(continued)

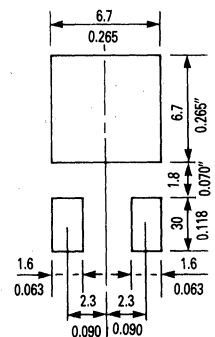


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



TYPICAL CHARACTERISTICS

MJD340

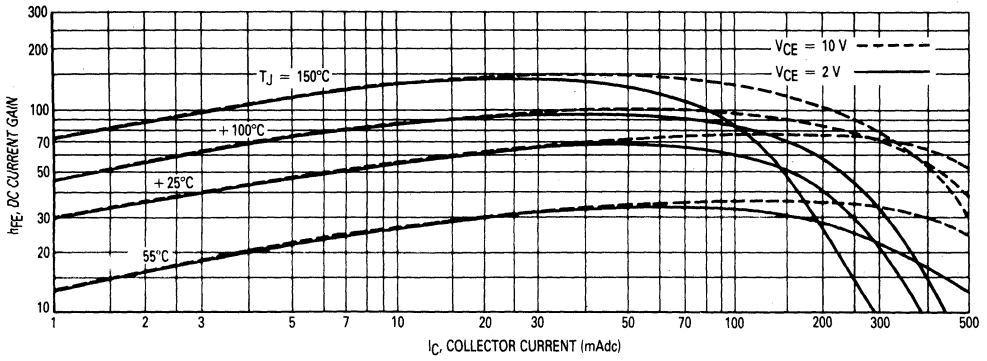


Figure 1. DC Current Gain

MJD340

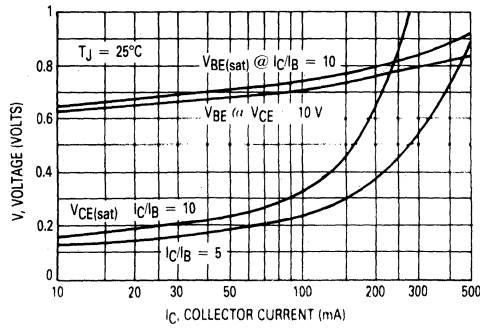


Figure 2. "On" Voltages

MJD350

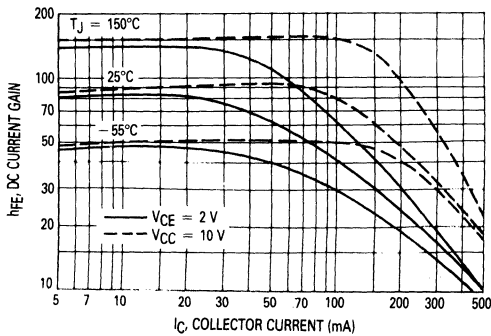


Figure 3. DC Current Gain

MJD350

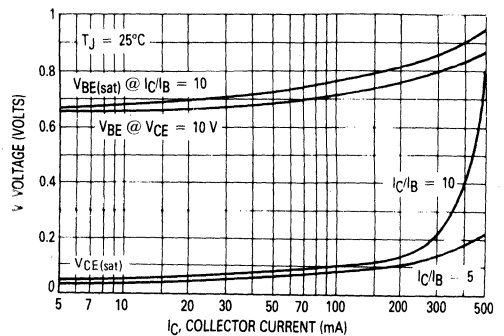


Figure 4. "On" Voltages

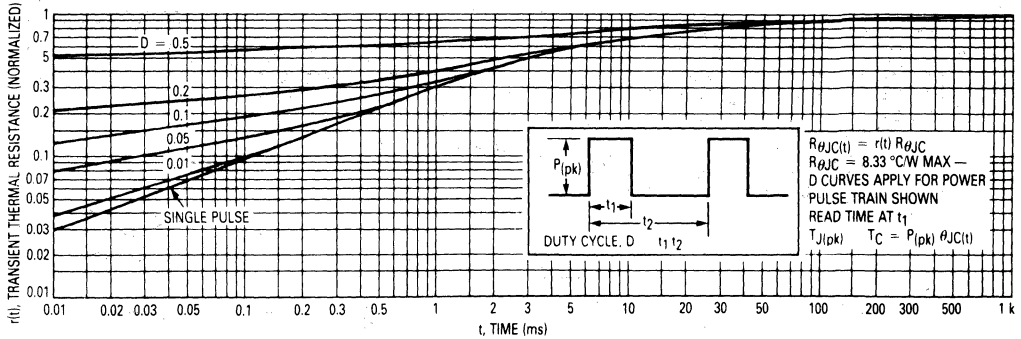


Figure 5. Thermal Response

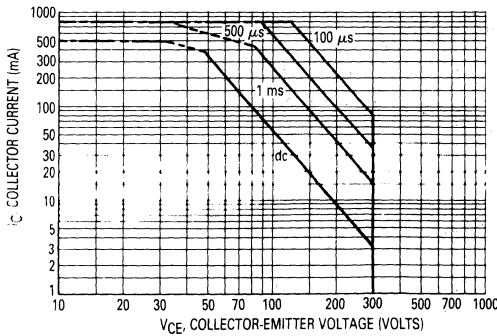


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{j(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{j(pk)} \leq 150^\circ\text{C}$. $T_{j(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

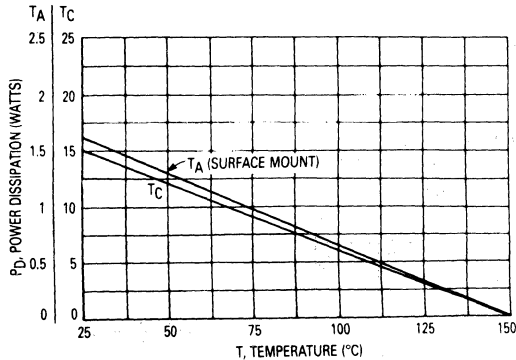
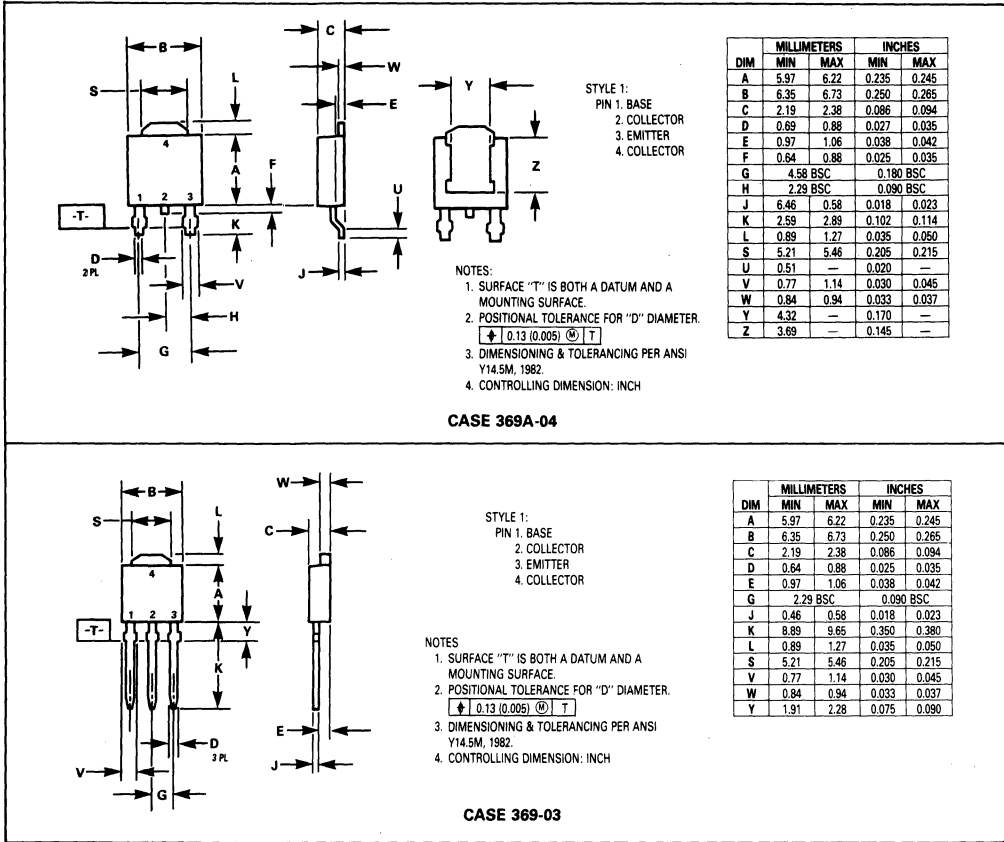


Figure 7. Power Derating

OUTLINE DIMENSIONS



Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD340-1)

Complementary Power Transistors DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("1" Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel ("RL" Suffix)
- Electrically Similar to MJE2955 and MJE3055
- DC Current Gain Specified to 10 Amperes
- High Current Gain-Bandwidth Product — $f_T = 2 \text{ MHz (Min) @ } I_C = 500 \text{ mA dc}$

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CE0}	60	Vdc
Collector-Base Voltage	V_{CB}	70	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_{D\dagger}$	20 0.16	Watts W°C
Total Power Dissipation (1) @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.75 0.014	Watts W°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$

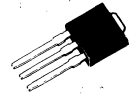
(1) These ratings are applicable when surface mounted on the minimum pad sizes recommended.
 † Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

PNP
MJD2955
NPN
MJD3055

SILICON
POWER TRANSISTORS
10 AMPERES
60 VOLTS
20 WATTS

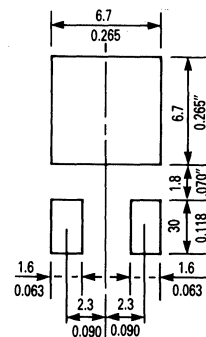


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



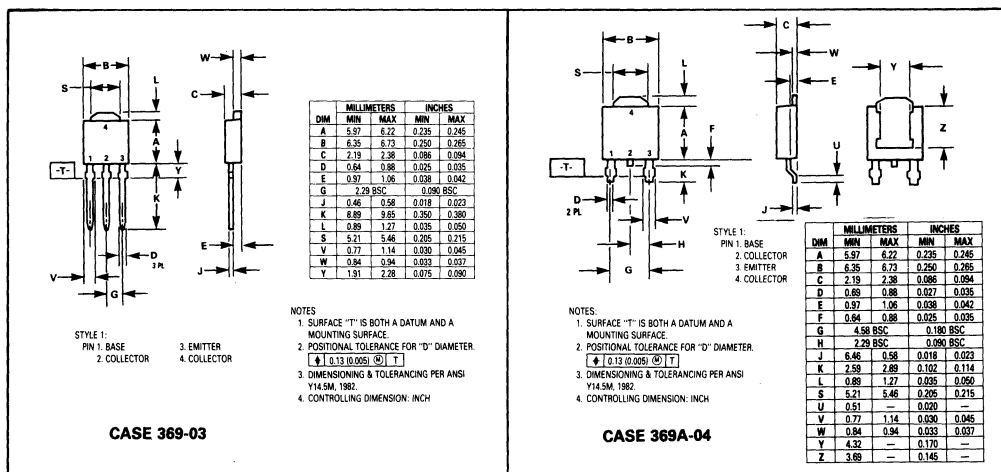
MJD2955 PNP, MJD3055 NPN

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 30 mA, I _B = 0)	V _{CEO(sus)}	60	—	Vdc
Collector Cutoff Current (V _{CE} = 30 Vdc, I _B = 0)	I _{CEO}	—	50	μAdc
Collector Cutoff Current (V _{CE} = 70 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 70 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C)	I _{CEX}	—	0.02 2	mA mAdc
Collector Cutoff Current (V _{CB} = 70 Vdc, I _E = 0) (V _{CB} = 70 Vdc, I _E = 0, T _C = 150°C)	I _{CBO}	—	0.02 2	mA mAdc
Emitter Cutoff Current (V _{BE} = 5 Vdc, I _C = 0)	I _{EBO}	—	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I _C = 4 Adc, V _{CE} = 4 Vdc) (I _C = 10 Adc, V _{CE} = 4 Vdc)	h _{FE}	20 5	100 —	—
Collector-Emitter Saturation Voltage (1) (I _C = 4 Adc, I _B = 0.4 Adc) (I _C = 10 Adc, I _B = 3.3 Adc)	V _{CE(sat)}	—	1.1 8	Vdc
Base-Emitter On Voltage (1) (I _C = 4 Adc, V _{CE} = 4 Vdc)	V _{BE(on)}	—	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I _C = 500 mA, V _{CE} = 10 Vdc, f = 500 kHz)	f _T	2	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD3055-1)

TYPICAL CHARACTERISTICS

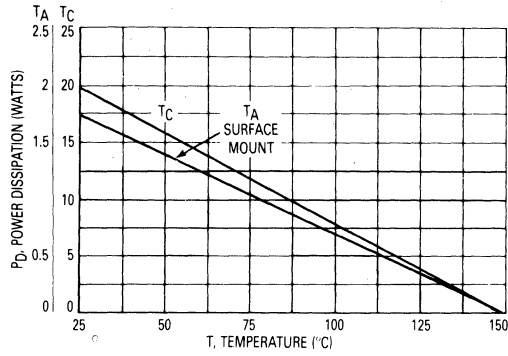


Figure 1. Power Derating

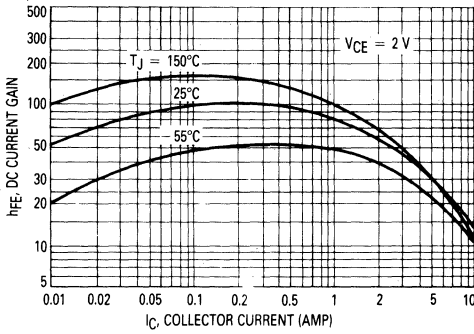


Figure 2. DC Current Gain

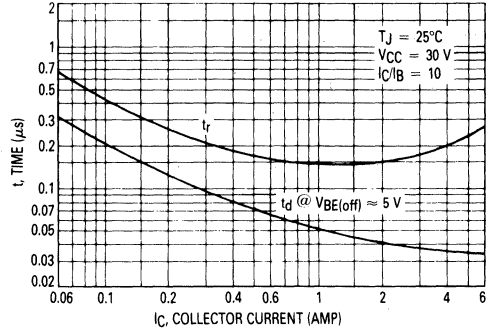


Figure 3. Turn-On Time

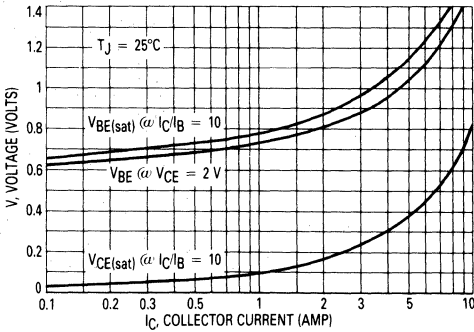


Figure 4. "On" Voltages, MJD3055

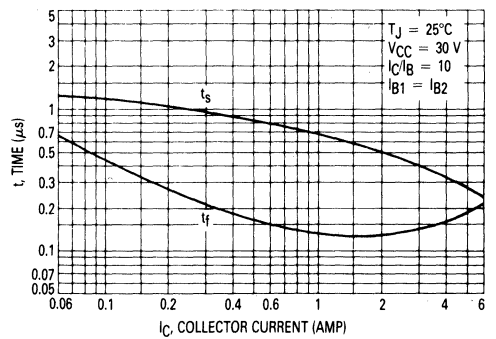


Figure 5. Turn-Off Time

3

MJD2955 PNP, MJD3055 NPN

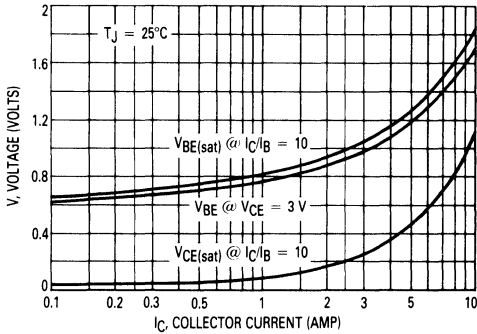


Figure 6. "On" Voltages, MJD2955

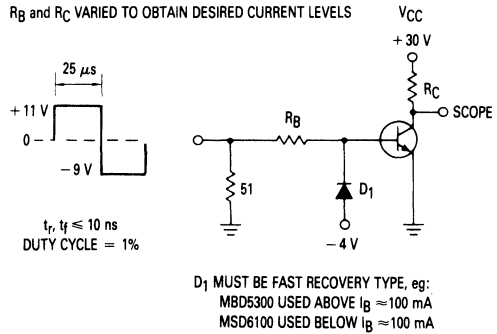


Figure 7. Switching Time Test Circuit

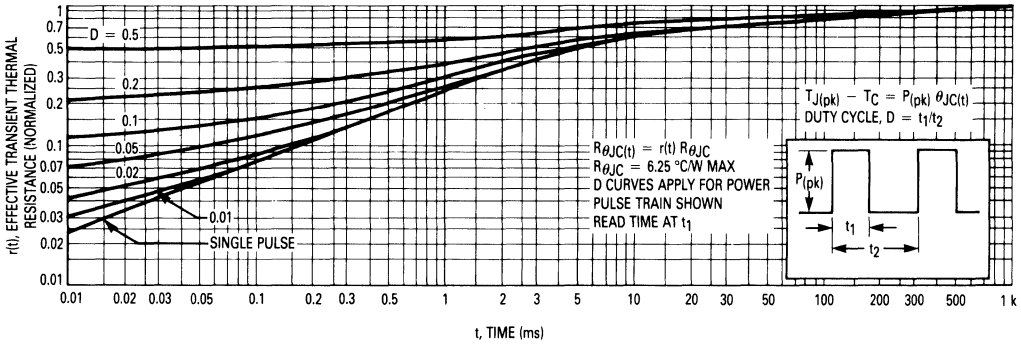


Figure 8. Thermal Response

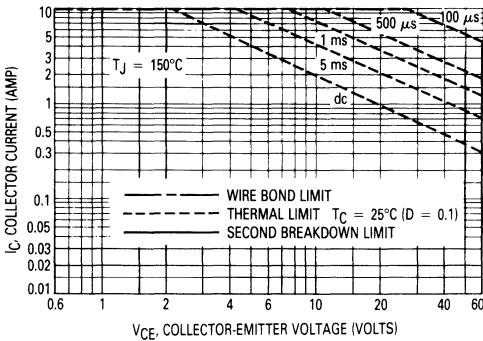


Figure 9. Maximum Forward Bias Safe Operating Area

FORWARD BIAS SAFE OPERATING AREA INFORMATION

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Complementary Darlington Power Transistors

DPAK For Surface Mount Applications

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, convertors, and power amplifiers.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("1" Suffix)
- Available on 16 mm Tape and Reel for Automatic Handling ("RL" Suffix)
- Surface Mount Replacements for 2N6034-2N6039 Series
- Monolithic Construction With Built-in Base-Emitter Shunt Resistors
- High DC Current Gain — $h_{FE} = 2500$ (Typ) @ $I_C = 4$ Adc
- Complementary Pairs Simplifies Designs

MAXIMUM RATINGS

Rating	Symbol	MJD6036 MJD6039	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	4 8	Adc
Base Current	I_B	100	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20 0.16	Watts $W/^\circ\text{C}$
Total Power Dissipation (1) @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.75 0.014	Watts $W/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$

*ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 30$ mAdc, $I_B = 0$)	$V_{CEO(sus)}$	80	—	Vdc
Collector-Cutoff Current ($V_{CE} = 40$ Vdc, $I_B = 0$)	I_{CEO}	—	10	μAdc

(1) These ratings are applicable when surface mounted on the minimum pad sizes recommended. (continued)

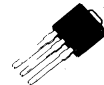
* Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.

PNP
MJD6036
NPN
MJD6039

SILICON
POWER TRANSISTORS
4 AMPERES
80 VOLTS
20 WATTS

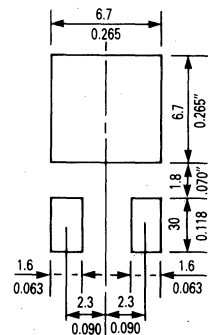


CASE 369A-04



CASE 369-03

**MINIMUM PAD SIZES
 RECOMMENDED FOR
 SURFACE MOUNTED
 APPLICATIONS**



MJD6036 PNP, MJD6039 NPN

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 1 \text{ Adc}$, $V_{CE} = 4 \text{ Vdc}$) ($I_C = 2 \text{ Adc}$, $V_{CE} = 4 \text{ Vdc}$)	h_{FE}	1000 500	— —	—
Collector-Emitter Saturation Voltage ($I_C = 2 \text{ Adc}$, $I_B = 8 \text{ mAdc}$)	$V_{CE(sat)}$	—	2.5	Vdc
Base-Emitter On Voltage ($I_C = 2 \text{ Adc}$, $V_{CE} = 4 \text{ Vdc}$)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain ($I_C = 0.75 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1 \text{ kHz}$)	$ h_{fe} $	25	—	—
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	— —	200 100	pF
	MJD6036 MJD6039			

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

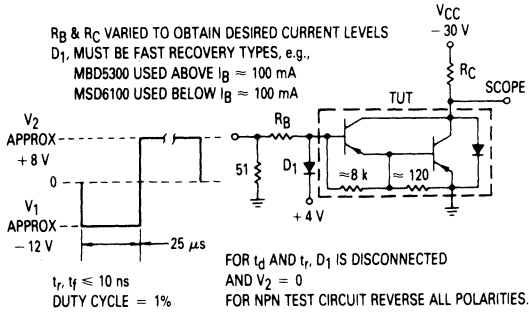


Figure 1. Switching Times Test Circuit

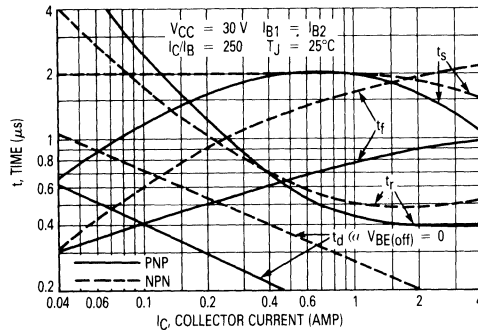


Figure 2. Switching Times

TYPICAL ELECTRICAL CHARACTERISTICS

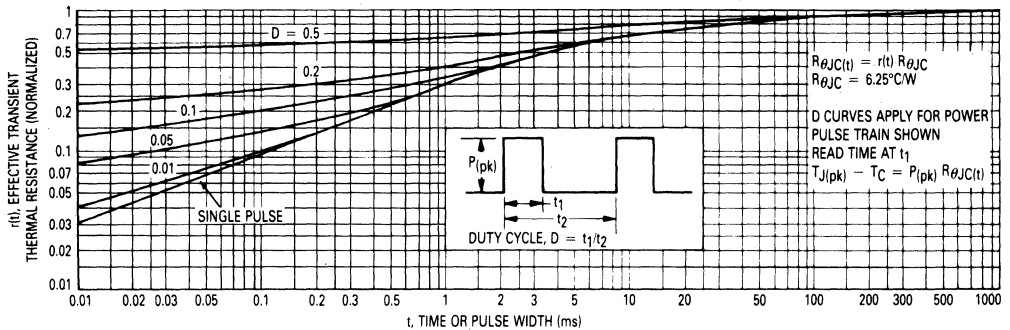


Figure 3. Thermal Response

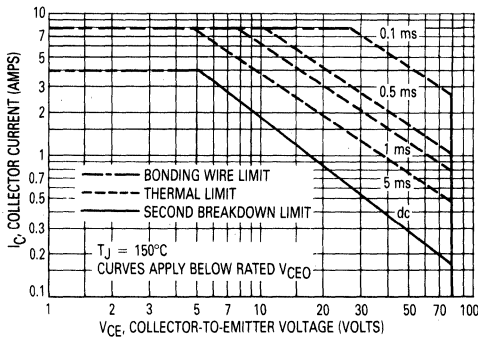


Figure 4. Maximum Rated Forward Biased Safe Operating Area

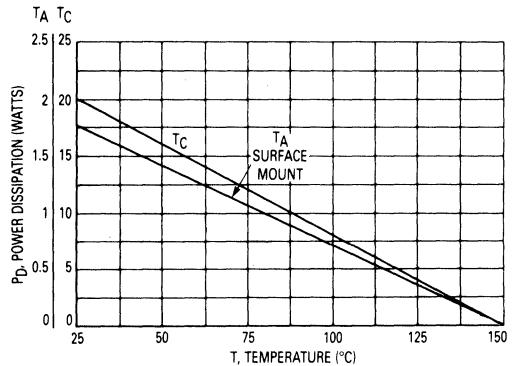


Figure 5. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 6 and 7 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

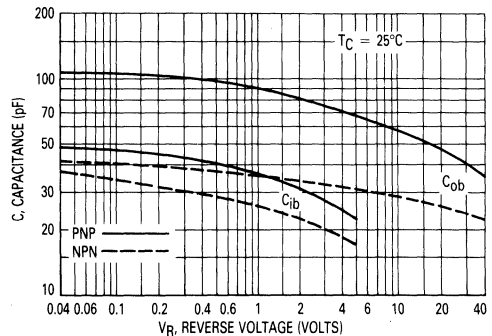


Figure 6. Capacitance

3

MJD6036 PNP, MJD6039 NPN

TYPICAL ELECTRICAL CHARACTERISTICS

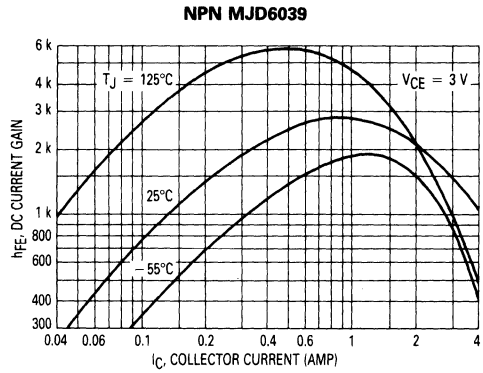
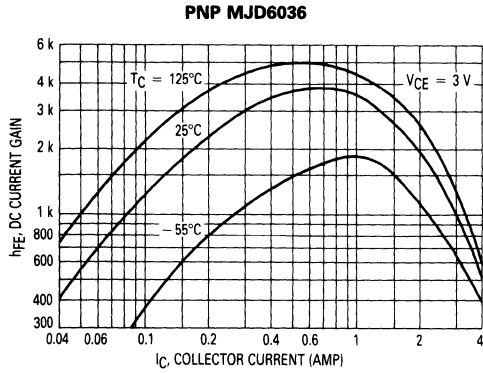


Figure 7. DC Current Gain

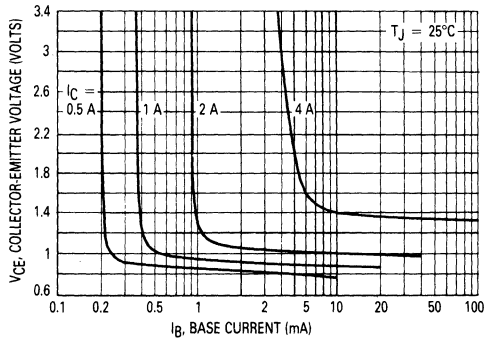
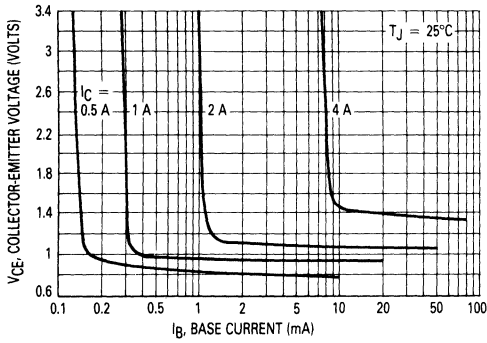


Figure 8. Collector Saturation Region

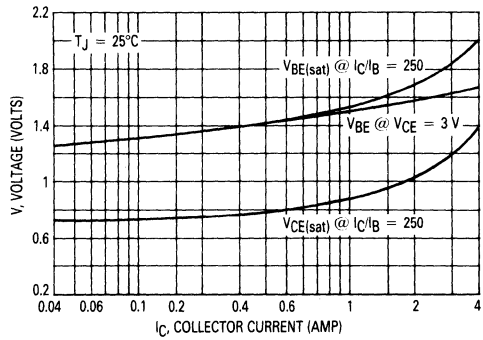
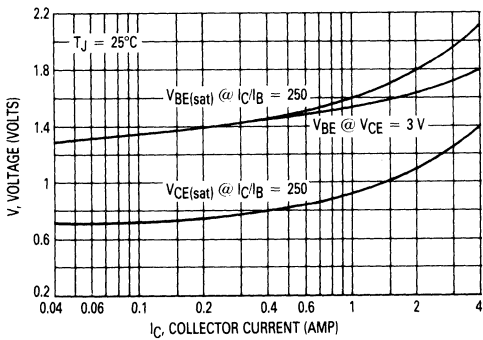


Figure 9. "On" Voltages

MJD6036 PNP, MJD6039 NPN

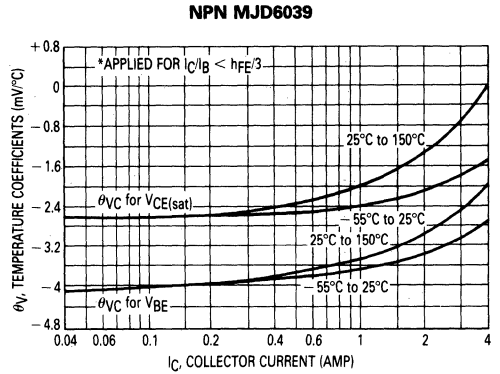
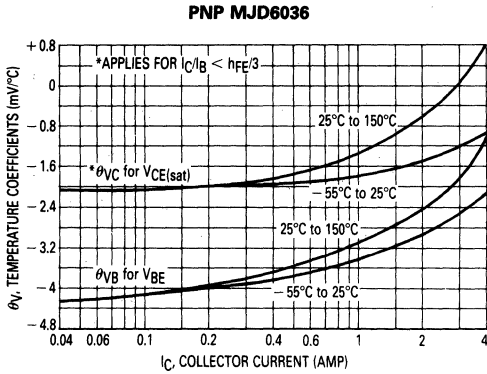


Figure 10. Temperature Coefficients

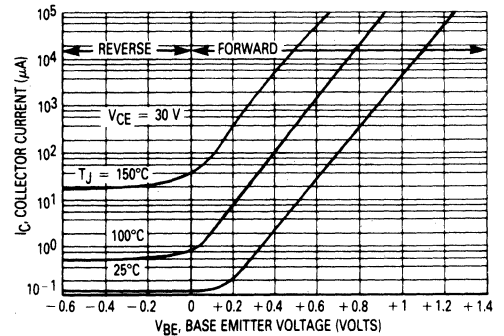
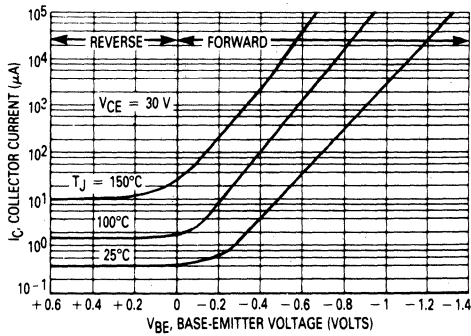


Figure 11. Collector Cut-Off Region

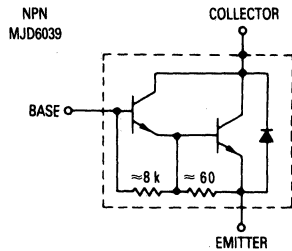
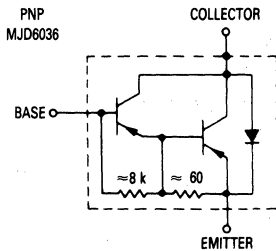
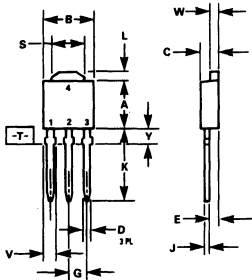


Figure 12. Darlington Schematic

OUTLINE DIMENSIONS

CASE 369-03

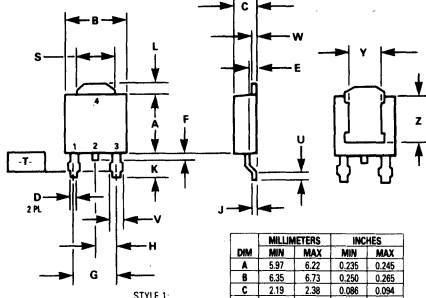


STYLE 1:
PIN 1, BASE
2, COLLECTOR
3, EMITTER
4, COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.85	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.29	0.075	0.090

- NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
 2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
 $\downarrow 0.13 (0.005) \text{ (M) T}$
 3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 4. CONTROLLING DIMENSION: INCH

CASE 369A-04



STYLE 1:
PIN 1, BASE
2, COLLECTOR
3, EMITTER
4, COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	6.58	0.254	0.260
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

- NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
 2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
 $\downarrow 0.13 (0.005) \text{ (M) T}$
 3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 4. CONTROLLING DIMENSION: INCH

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD6036-1)

Designer's Data Sheet
High Voltage Switchmode Series
DPAK For Surface Mount Applications

This device is designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 220 V SWITCHMODE applications such as switching regulators, inverters, motor controls, solenoid/relay drivers and deflection circuits.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Reverse Biased SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and $100^\circ\text{C} \dots t_C @ 1 \text{ A}$, 100°C is 290 ns (Typ)
- 700 V Blocking Capability
- Switching and SOA Applications Information
- Electrically Similar to the Popular MJE13003

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous	I_C	1.5	Adc
— Peak (1)	I_{CM}	3	
Base Current — Continuous	I_B	0.75	Adc
— Peak (1)	I_{BM}	1.5	
Emitter Current — Continuous	I_E	2.25	Adc
— Peak (1)	I_{EM}	4.5	
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (2)	P_D	1.56	Watts
Derate above 25°C		0.0125	$\text{W}/^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	15	Watts
Derate above 25°C		0.12	$\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient (2)	$R_{\theta JA}$	80	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes	T_L	260	$^\circ\text{C}$

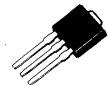
(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.
 (2) When surface mounted on minimum pad sizes recommended.

MJD13003

NPN SILICON
POWER TRANSISTOR
1.5 AMPERES
400 VOLTS
15 WATTS

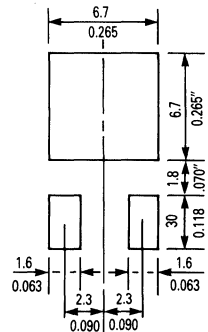


CASE 369A-04



CASE 369-03

MINIMUM PAD SIZES
RECOMMENDED FOR
SURFACE MOUNTED
APPLICATIONS



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage ($I_C = 10\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.1 2	mAdc
Emitter Cutoff Current ($V_{EB} = 9\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 11			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 12			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$) ($I_C = 1\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$)	h_{FE}	8 5	— —	40 25	—
Collector-Emitter Saturation Voltage ($I_C = 0.5\text{ Adc}$, $I_B = 0.1\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.25\text{ Adc}$) ($I_C = 1.5\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.25\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — — —	— — — —	0.5 1 3 1	Vdc
Base-Emitter Saturation Voltage ($I_C = 0.5\text{ Adc}$, $I_B = 0.1\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.25\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.25\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— — —	— — —	1 1.2 1.1	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product ($I_C = 100\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ MHz}$)	f_T	4	10	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	—	21	—	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$V_{CC} = 125\text{ Vdc}$, $I_C = 1\text{ A}$, $I_{B1} = I_{B2} = 0.2\text{ A}$, $t_D = 25\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$	t_d	—	0.05	0.1	μs
Rise Time		t_r	—	0.5	1	μs
Storage Time		t_s	—	2	4	μs
Fall Time		t_f	—	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Storage Time	$I_C = 1\text{ A}$, $V_{clamp} = 300\text{ Vdc}$, $I_{B1} = 0.2\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$	t_{sv}	—	1.7	4	μs
Crossover Time		t_c	—	0.29	0.75	μs
Fall Time		t_{fi}	—	0.15	—	μs

(1) Pulse Test: Pulse Width = $300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

OUTLINE DIMENSIONS

CASE 369-03

NOTES

- SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
- POSITIONAL TOLERANCES FOR "D" DIAMETER: $\phi 0.13(0.005) [M]$
- DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.84	0.88	0.033	0.035
E	0.87	1.06	0.038	0.042
G	2.29	RSC	0.090	RSC
H	0.46	0.58	0.018	0.023
K	8.89	9.85	0.350	0.390
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.51	—	—	—
W	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.81	2.28	0.072	0.090

STYLE 1:
PIN 1: BASE
2: COLLECTOR
3: EMITTER
4: COLLECTOR

CASE 369A-04

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.84	0.88	0.033	0.035
E	0.87	1.06	0.038	0.042
G	4.54	RSC	0.180	RSC
H	2.29	RSC	0.090	RSC
J	6.46	0.58	0.018	0.023
K	2.19	2.89	0.100	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.51	—	—	—
W	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	2.89	—	0.145	—

NOTES

- SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
- POSITIONAL TOLERANCE FOR "D" DIAMETER: $\phi 0.13(0.005) [M]$
- DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH

STYLE 1:
PIN 1: BASE
2: COLLECTOR
3: EMITTER
4: COLLECTOR

Case 369-03 may be ordered by adding a "-1" suffix to the device title (i.e. MJD13003-1)

3-971

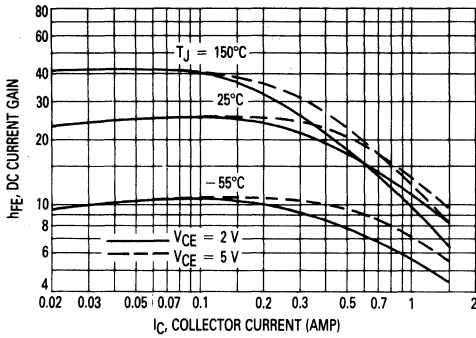


Figure 1. DC Current Gain

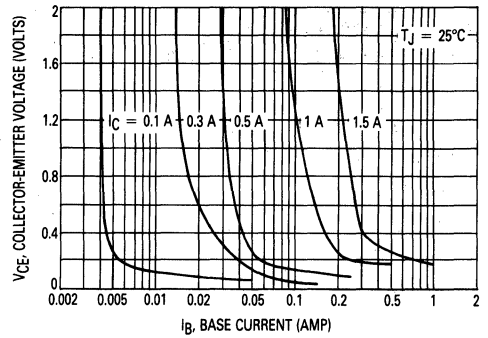


Figure 2. Collector Saturation Region

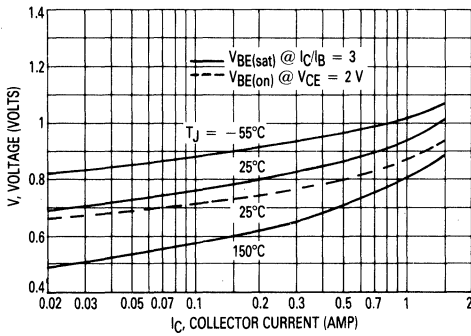


Figure 3. Base-Emitter Voltage

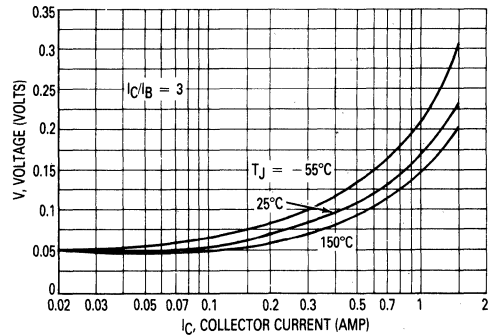


Figure 4. Collector-Emitter Saturation Region

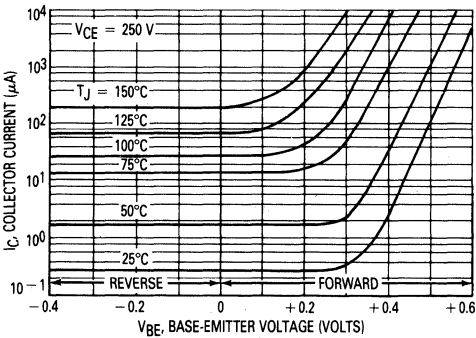


Figure 5. Collector Cutoff Region

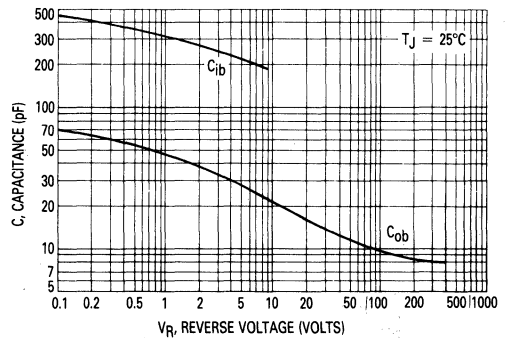


Figure 6. Capacitance

3

Table 1. Test Conditions For Dynamic Performance

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING			RESISTIVE SWITCHING
TEST CIRCUITS			
CIRCUIT VALUES	<p>COIL DATA: FERROXCUBE CORE #6656 FULL BOBBIN (~200 TURNS) #20</p>	<p>GAP FOR 30 mH/2 A $L_{coil} = 50 \text{ mH}$</p>	<p>$V_{CC} = 20 \text{ V}$ $V_{clamp} = 300 \text{ Vdc}$</p>
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p> <p>t_1 ADJUSTED TO OBTAIN I_C</p> $t_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$ <p>TEST EQUIPMENT SCOPE-TEKTRONICS 475 OR EQUIVALENT</p>		

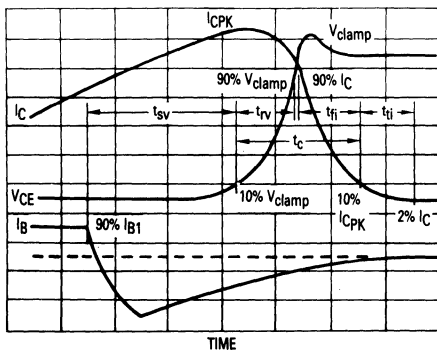


Figure 7. Inductive Switching Measurements

Table 2. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{RV} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching wave-

forms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the equation:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{RV} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{SV}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

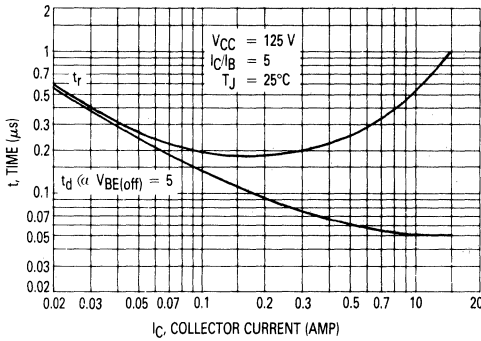


Figure 8. Turn-On Time

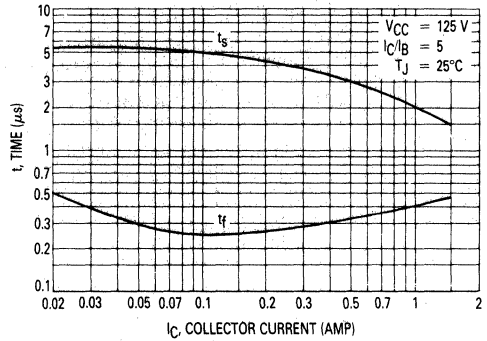


Figure 9. Turn-Off Time

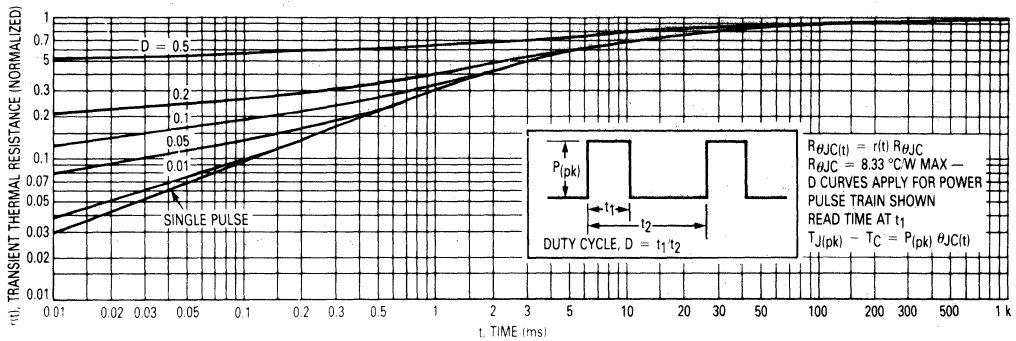


Figure 10. Thermal Response

3

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

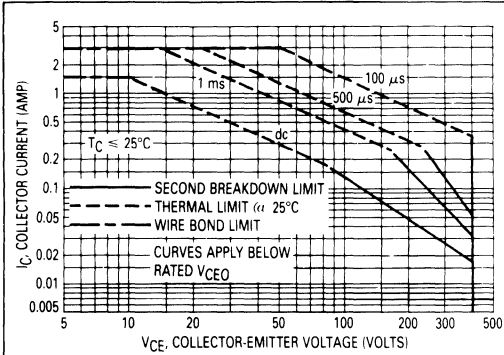


Figure 11. Active Region Safe Operating Area

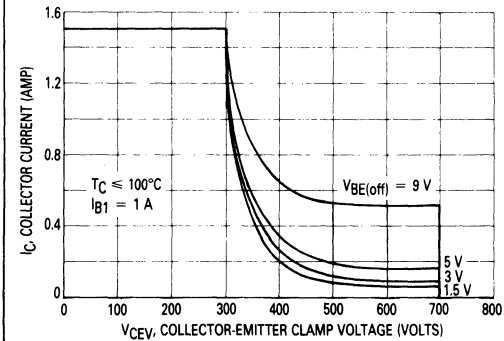


Figure 12. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by applying curves on Figure 13.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

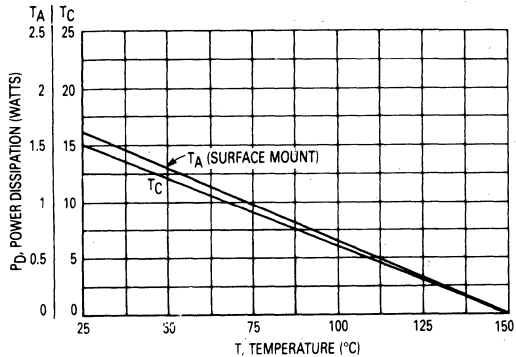


Figure 13. Power Derating

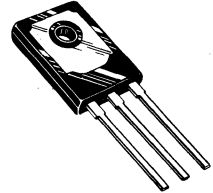
MEDIUM-POWER PNP SILICON TRANSISTOR

... for use as an output device in complementary audio amplifiers up to 20-Watts music power per channel.

- High DC Current Gain – $h_{FE} = 25-100$ @ $I_C = 2.0$ A
- Thermopad High-Efficiency Compact Package
- Complementary to NPN MJE205

5 AMPERE
POWER TRANSISTOR
PNP SILICON

50 VOLTS
65 WATTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	5.0	Adc
Base Current	I_B	2.5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D(1)$	65 0.522	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.92	$^\circ\text{C}/\text{W}$

(1) Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

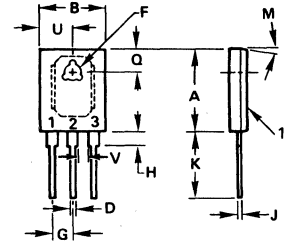
OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage (2) ($I_C = 100$ mA, $I_B = 0$)	BV_{CEO}	50	—	Vdc
Collector Cutoff Current ($V_{CB} = 50$ Vdc, $I_E = 0$) ($V_{CB} = 50$ Vdc, $I_E = 0$, $T_C = 150^\circ\text{C}$)	I_{CBO}	—	0.1 2.0	mA
Emitter Cutoff Current ($V_{BE} = 4.0$ Vdc, $I_C = 0$)	I_{EBO}	—	1.0	mA

ON CHARACTERISTICS

DC Current Gain ($I_C = 2.0$ Adc, $V_{CE} = 2.0$ Vdc)	h_{FE}	25	100	—
Base-Emitter Voltage ($I_C = 2.0$ Adc, $V_{CE} = 2.0$ Vdc)	V_{BE}	—	1.2	Vdc

(2) Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$.

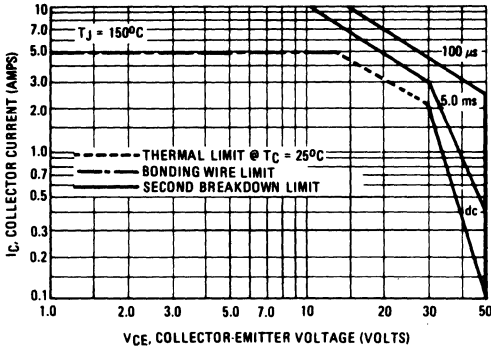


STYLE 2:
 PIN 1. EMITTER
 2. COLLECTOR
 3. BASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	90 TYP		90 TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	—	0.080	—

CASE 90-05
TO-225AB

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 1 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – "ON" VOLTAGES

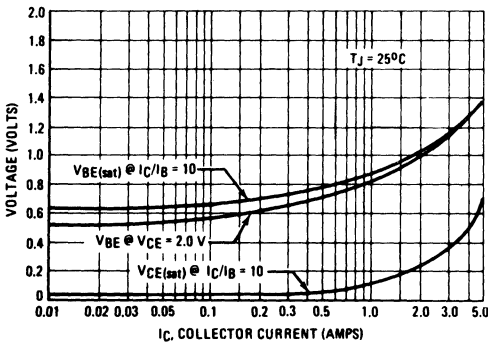


FIGURE 3 – DC CURRENT GAIN

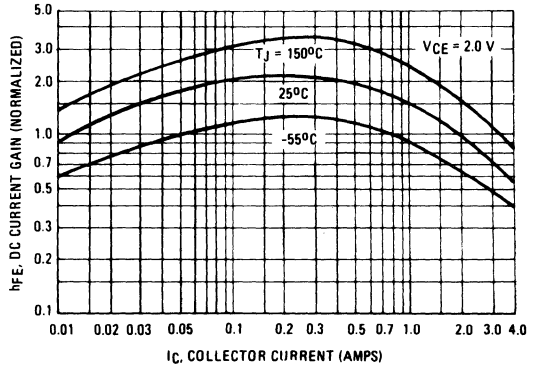
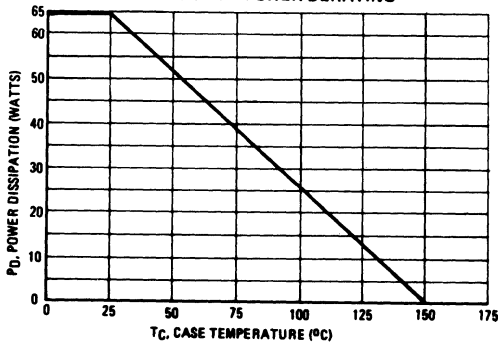


FIGURE 4 – POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
MJE170 thru MJE172
NPN
MJE180 thru MJE182

**COMPLEMENTARY PLASTIC SILICON
 POWER TRANSISTORS**

... designed for low power audio amplifier and low current, high speed switching applications.

- Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 40 \text{ Vdc} - \text{MJE170, MJE180}$
 $= 60 \text{ Vdc} - \text{MJE171, MJE181}$
 $= 80 \text{ Vdc} - \text{MJE172, MJE182}$
- DC Current Gain –
 $h_{FE} = 30 \text{ (Min) @ } I_C = 0.5 \text{ Adc}$
 $= 12 \text{ (Min) @ } I_C = 1.5 \text{ Adc}$
- Current-Gain – Bandwidth Product –
 $f_T = 50 \text{ MHz (Min) @ } I_C = 100 \text{ mA dc}$
- Annular Construction for Low Leakages –
 $I_{CBO} = 100 \text{ nA (Max) @ Rated } V_{CB}$

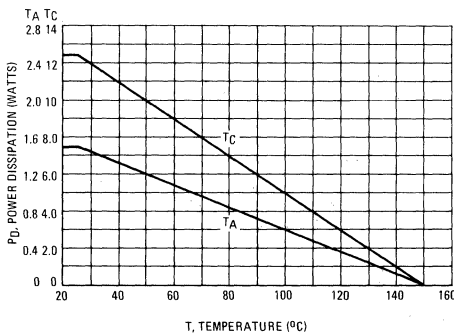
MAXIMUM RATINGS

Rating	Symbol	MJE170 MJE180	MJE171 MJE181	MJE172 MJE182	Unit
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 3.0 → ← 6.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	← 1.5 → ← 0.012 →			Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 12.5 → ← 0.1 →			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			$^\circ\text{C}$

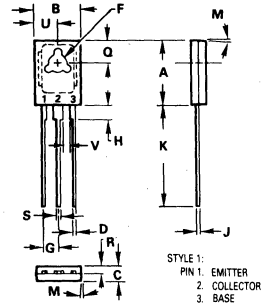
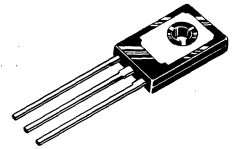
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	$^\circ\text{C/W}$

FIGURE 1 – POWER DERATING



3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
40-60-80 VOLTS
12.5 WATTS



NOTES:
 1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP			
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

MJE170, MJE171, MJE172, PNP MJE180, MJE181, MJE182 NPN

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I _C = 10 mA _{dc} , I _B = 0)	V _{CEO(sus)}	40	—	V _{dc}
	MJE170, MJE180	60	—	
	MJE171, MJE181	80	—	
	MJE172, MJE182	—	—	
Collector Cutoff Current (V _{CB} = 60 V _{dc} , I _E = 0)	I _{CBO}	—	0.1	μA _{dc}
(V _{CB} = 80 V _{dc} , I _E = 0)	MJE170, MJE180	—	0.1	
(V _{CB} = 100 V _{dc} , I _E = 0)	MJE171, MJE181	—	0.1	
(V _{CB} = 60 V _{dc} , I _E = 0, T _C = 150°C)	MJE172, MJE182	—	0.1	
(V _{CB} = 80 V _{dc} , I _E = 0, T _C = 150°C)	MJE170, MJE180	—	0.1	mA _{dc}
(V _{CB} = 100 V _{dc} , I _E = 0, T _C = 150°C)	MJE171, MJE181	—	0.1	
(V _{CB} = 100 V _{dc} , I _E = 0, T _C = 150°C)	MJE172, MJE182	—	0.1	
Emitter Cutoff Current (V _{BE} = 7.0 V _{dc} , I _C = 0)	I _{EBO}	—	0.1	μA _{dc}

ON CHARACTERISTICS

DC Current Gain (I _C = 100 mA _{dc} , V _{CE} = 1.0 V _{dc}) (I _C = 500 mA _{dc} , V _{CE} = 1.0 V _{dc}) (I _C = 1.5 A _{dc} , V _{CE} = 1.0 V _{dc})	h _{FE}	50 30 12	250 — —	—
Collector-Emitter Saturation Voltage (I _C = 500 mA _{dc} , I _B = 50 mA _{dc}) (I _C = 1.5 A _{dc} , I _B = 150 mA _{dc}) (I _C = 3.0 A _{dc} , I _B = 600 mA _{dc})	V _{CE(sat)}	— — —	0.3 0.9 1.7	V _{dc}
Base-Emitter Saturation Voltage (I _C = 1.5 A _{dc} , I _B = 150 mA _{dc}) (I _C = 3.0 A _{dc} , I _B = 600 mA _{dc})	V _{BE(sat)}	— —	1.5 2.0	V _{dc}
Base-Emitter On Voltage (I _C = 500 mA _{dc} , V _{CE} = 1.0 V _{dc})	V _{BE(on)}	—	1.2	V _{dc}

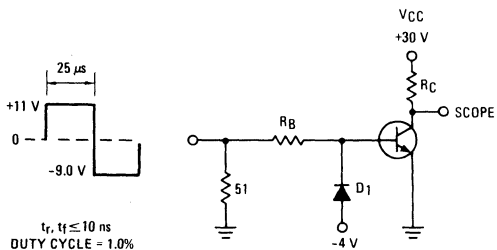
DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product (1) (I _C = 100 mA _{dc} , V _{CE} = 10 V _{dc} , f _{test} = 10 MHz)	f _T	50	—	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 0.1 MHz)	C _{ob}	—	60 40	pF
	MJE170/MJE172	—	60	
	MJE180/MJE182	—	40	

(1) f_T = |h_{fe}| • f_{test}

3

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D₁ MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

For PNP test circuit, reverse all polarities.

FIGURE 3 — TURN-ON TIME

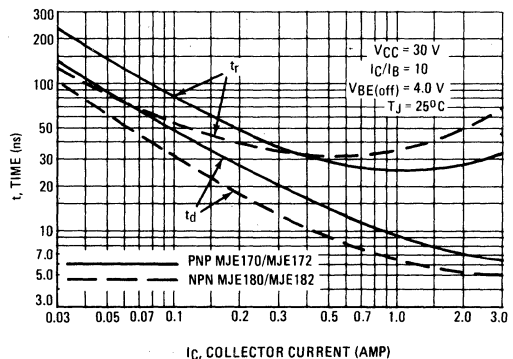
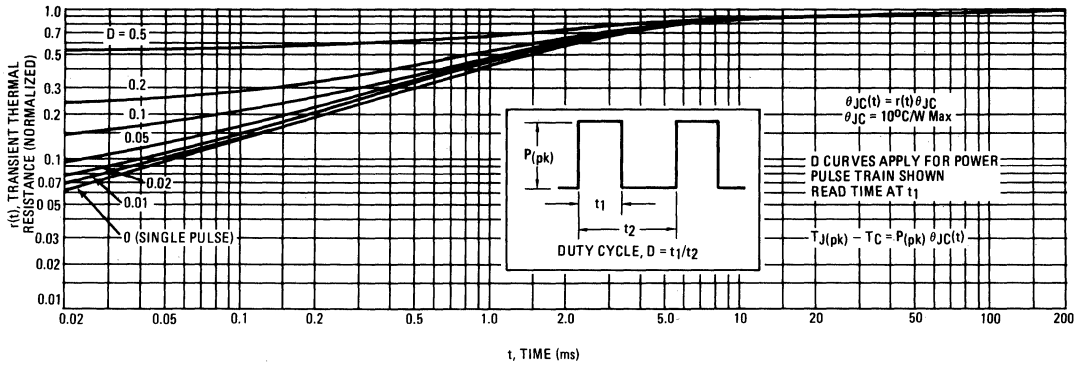


FIGURE 4 - THERMAL RESPONSE



ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 - MJE170, MJE171, MJE172

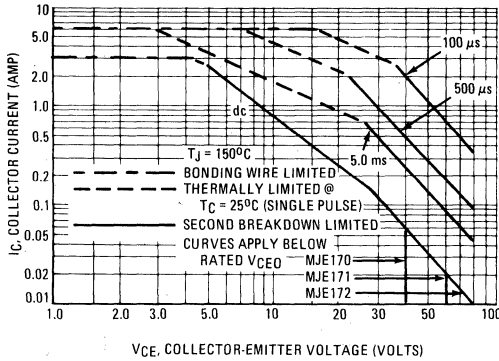
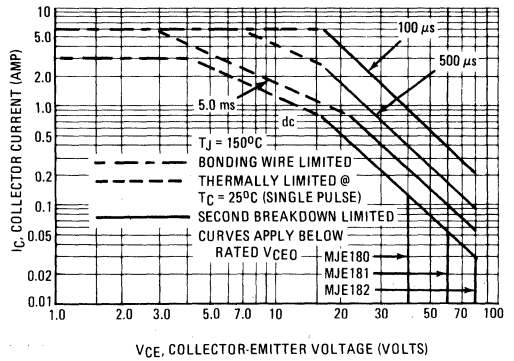


FIGURE 6 - MJE180, MJE181, MJE182



There are two limitations on the power handling ability of a transistor - average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figures 5 and 6 is based on $T_J(pk) = 150^\circ\text{C}$; T_C is

variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(pk) < 150^\circ\text{C}$. $T_J(pk)$ may be calculated from the data in Figure 4. At high case temperature, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 - TURN-OFF TIME

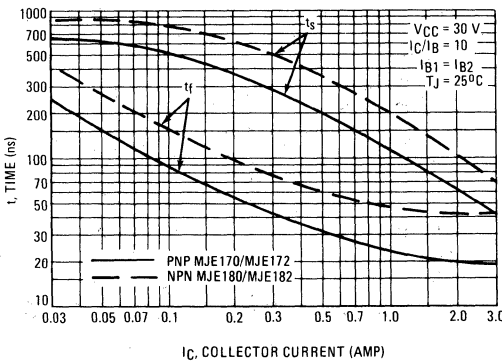
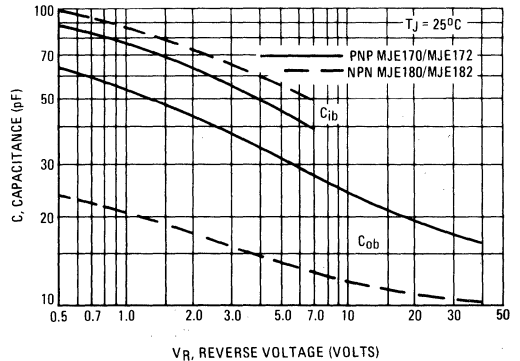


FIGURE 8 - CAPACITANCE



MJE170, MJE171, MJE172, PNP MJE180, MJE181, MJE182 NPN

PNP
MJE170, MJE171, MJE172

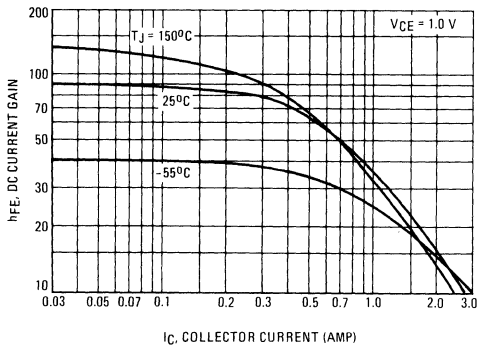


FIGURE 9 - DC CURRENT GAIN

NPN
MJE180, MJE181, MJE182

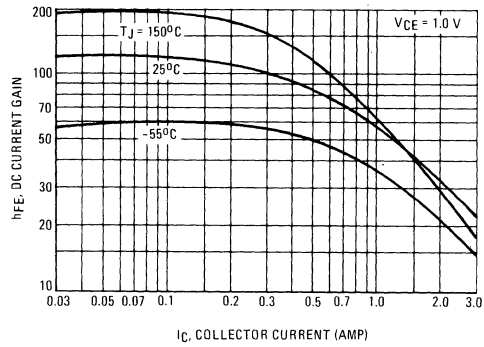


FIGURE 10 - "ON" VOLTAGES

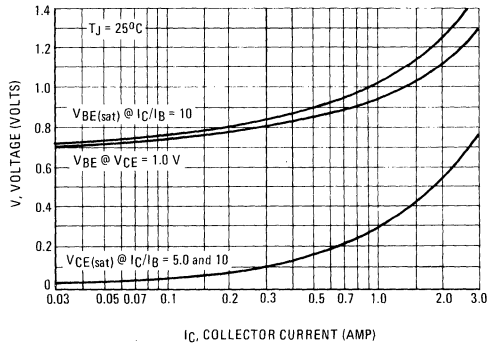
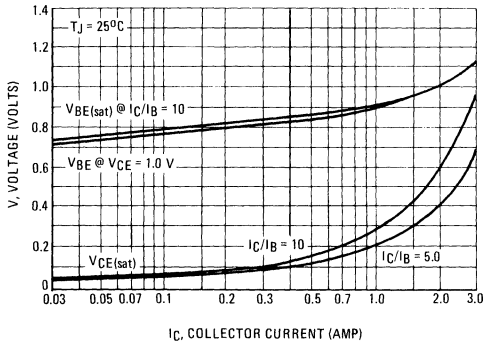
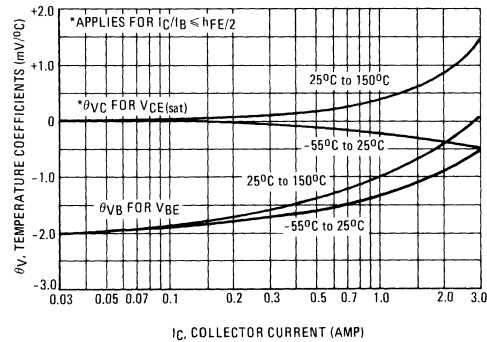
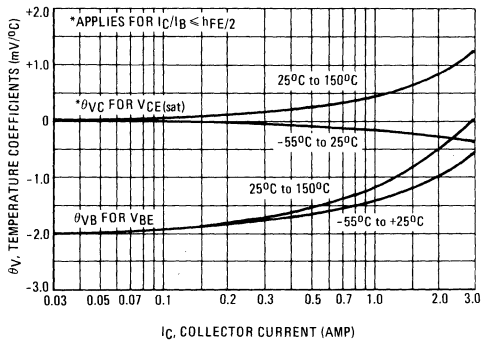


FIGURE 11 - TEMPERATURE COEFFICIENTS



3

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

**NPN
MJE200
PNP
MJE210**

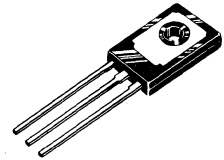
COMPLEMENTARY SILICON POWER PLASTIC TRANSISTORS

... designed for low voltage, low-power, high-gain audio amplifier applications.

- Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 25 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain – $h_{FE} = 70 \text{ (Min) @ } I_C = 500 \text{ mAdc}$
= 45 (Min) @ $I_C = 2.0 \text{ Adc}$
= 10 (Min) @ $I_C = 5.0 \text{ Adc}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$
= 0.75 Vdc (Max) @ $I_C = 2.0 \text{ Adc}$
- High Current-Gain – Bandwidth Product –
 $f_T = 65 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- Annular Construction for Low Leakage – $I_{CBO} = 100 \text{ nAdc @ Rated } V_{CB}$

**5 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON**

**25 VOLTS
15 WATTS**



MAXIMUM RATINGS

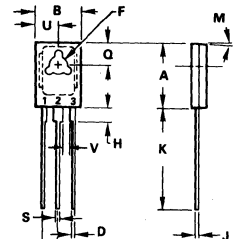
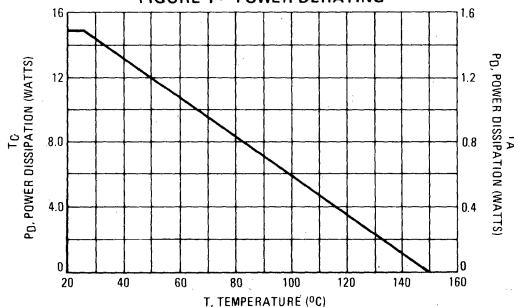
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	40	Vdc
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Emitter-Base Voltage	V_{EB}	8.0	Vdc
Collector Current – Continuous Peak	I_C	5.0 10	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	15 0.12	Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5 0.012	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	$^\circ\text{C/W}$

3

FIGURE 1 – POWER DERATING



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:

- LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.89	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

MJE200, NPN MJE210 PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 10 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	25	—	Vdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 40 \text{ Vdc}$, $I_E = 0$, $T_J = 125^\circ\text{C}$)	I_{CBO}	—	100	nAdc
		—	100	μAdc
Emitter Cutoff Current ($V_{BE} = 8.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	100	nAdc

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 5.0 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$)	h_{FE}	70	—	—
		45	180	—
		10	—	—
Collector-Emitter Saturation Voltage (1) ($I_C = 500 \text{ mAdc}$, $I_B = 50 \text{ mAdc}$) ($I_C = 2.0 \text{ Adc}$, $I_B = 200 \text{ mAdc}$) ($I_C = 5.0 \text{ Adc}$, $I_B = 1.0 \text{ Adc}$)	$V_{CE(sat)}$	—	0.3	Vdc
		—	0.75	
		—	1.8	
Base-Emitter Saturation Voltage (1) ($I_C = 5.0 \text{ Adc}$, $I_B = 1.0 \text{ Adc}$)	$V_{BE(sat)}$	—	2.5	Vdc
Base-Emitter On Voltage (1) ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.6	Vdc

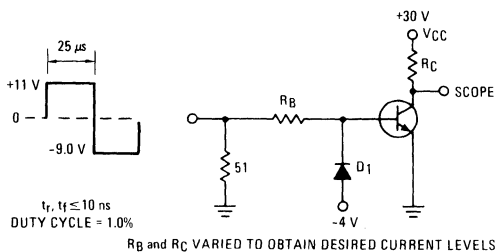
DYNAMIC CHARACTERISTICS

Current-Gain — Bandwidth Product (2) ($I_C = 100 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 10 \text{ MHz}$)	f_T	65	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	MJE200	80	μF
		MJE210	120	

(1) Pulse test: Pulse Width = 300 μs , Duty Cycle $\approx 2.0\%$.

(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 — SWITCHING TIME TEST CIRCUIT



D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx 100 \text{ mA}$
MSD6100 USED BELOW $I_B \approx 100 \text{ mA}$

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 — TURN-ON TIME

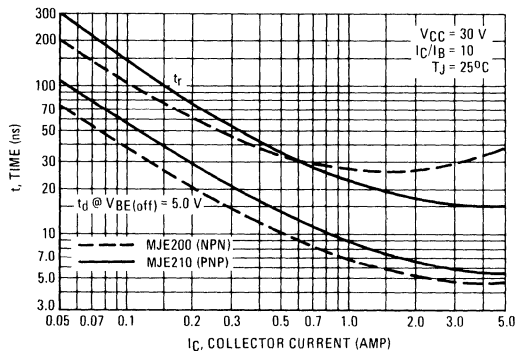


FIGURE 4 – THERMAL RESPONSE

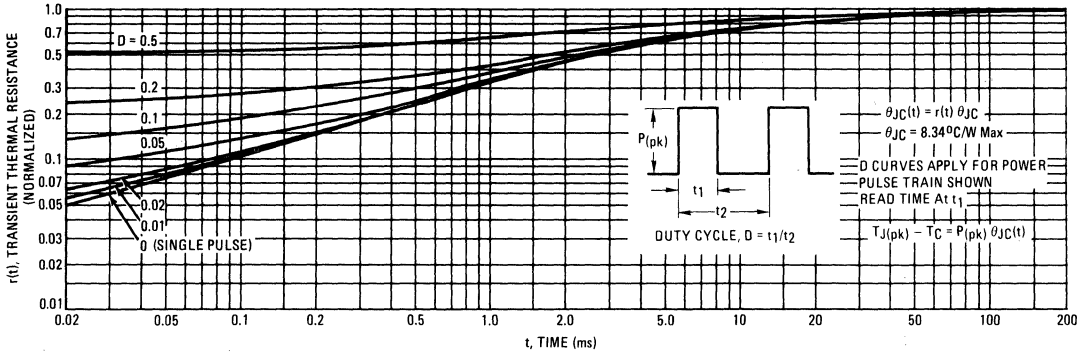
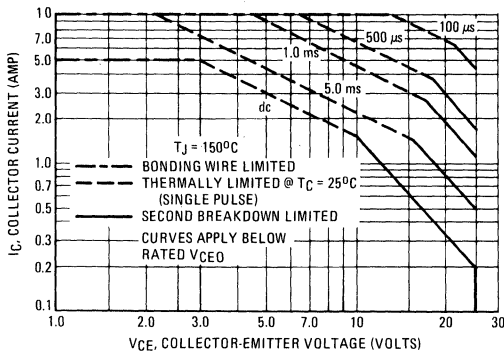


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

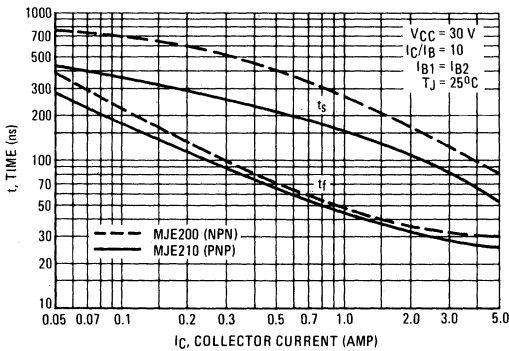
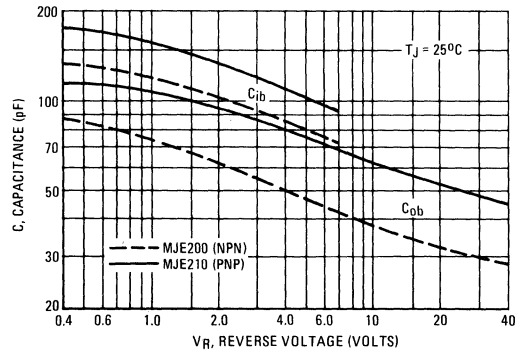


FIGURE 7 – CAPACITANCE



MJE200, NPN MJE210 PNP

NPN
MJE200

PNP
MJE210

FIGURE 8 - DC CURRENT GAIN

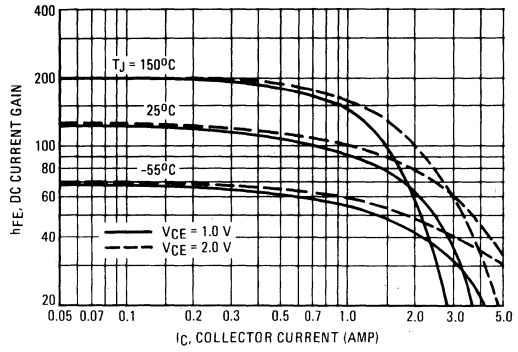
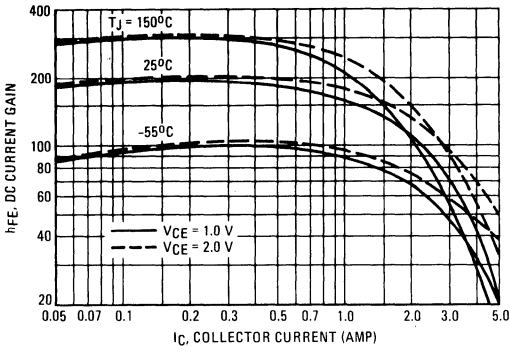


FIGURE 9 - "ON" VOLTAGE

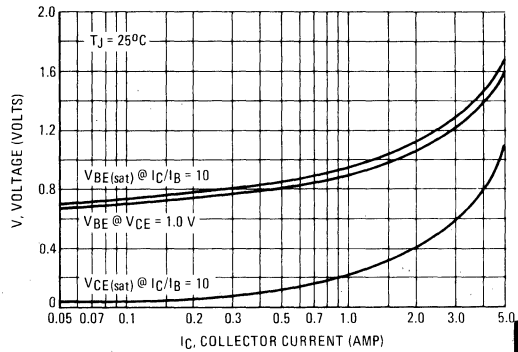
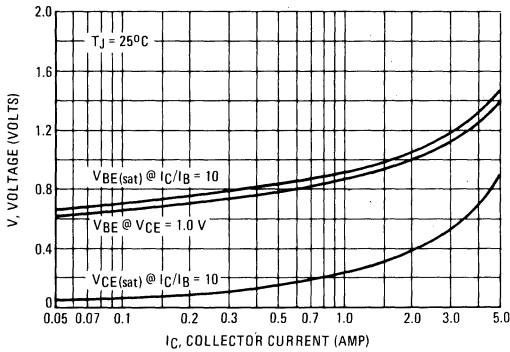
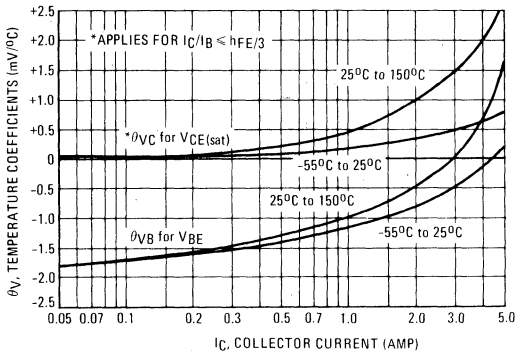
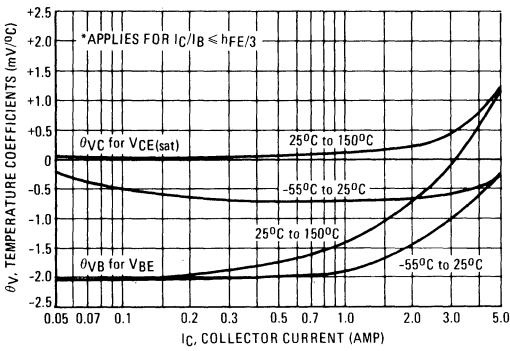


FIGURE 10 - TEMPERATURE COEFFICIENTS



NPN
MJE240, MJE241
MJE243, MJE244
PNP
MJE250 thru MJE254

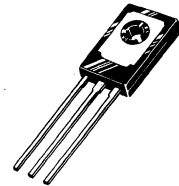
COMPLEMENTARY SILICON POWER PLASTIC TRANSISTORS

... designed for low power audio amplifier and low-current, high-speed switching applications.

- High Collector-Emitter Sustaining Voltage —
 $V_{CE(sus)} = 80 \text{ Vdc (Min) — MJE240, MJE250/2}$
 $= 100 \text{ Vdc (Min) — MJE243/4, MJE253/4}$
- High DC Current Gain @ $I_C = 200 \text{ mAdc}$
 $h_{FE} = 40\text{--}200 \text{ — MJE240, MJE250}$
 $= 40\text{--}120 \text{ — MJE241,243, MJE251,253}$
 $= 25 \text{ (Min) — MJE244, MJE252,54}$
- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$
- High Current Gain Bandwidth Product —
 $f_T = 40 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- Annular Construction for Low Leakages
 $I_{CBO} = 100 \text{ nAdc (Max) @ Rated } V_{CB}$

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON

80, 100 VOLTS
15 WATTS



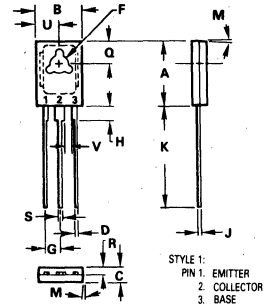
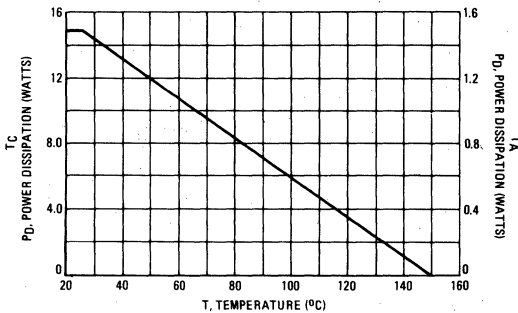
MAXIMUM RATINGS

Rating	Symbol	MJE240 MJE241 MJE250 MJE251 MJE252	MJE243 MJE244 MJE253 MJE254	Unit
Collector-Emitter Voltage	V_{CE}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}		7.0	Vdc
Collector Current — Continuous	I_C	4.0	8.0	Adc
Peak				
Base Current	I_B	1.0		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	15		Watts
Derate above 25°C		0.12		$\text{W}/^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.5		Watts
Derate above 25°C		0.012		$\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	$^\circ\text{C}/\text{W}$

FIGURE 1 — POWER DERATING



NOTES:

- LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3" TYP		3" TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	2.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

MJE240, MJE241, MJE243, MJE244, NPN, MJE250 thru MJE254, PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I _C = 10 mA, I _B = 0)	MJE240, MJE241, MJE250, MJE251, MJE252 MJE243, MJE244 MJE253, MJE254	V _{CEO(sus)}	80 100	— —	V _{dc}
Collector Cutoff Current (V _{CB} = 80 V _{dc} , I _E = 0)	MJE240, MJE241, MJE250, MJE251, MJE252	I _{CBO}	—	0.1	μA _{dc}
(V _{CB} = 100 V _{dc} , I _E = 0)	MJE243, MJE244, MJE253, MJE254		—	0.1	
(V _{CE} = 80 V _{dc} , I _E = 0, T _C = 125°C)	MJE240, MJE241, MJE250, MJE251, MJE252		—	0.1	mA _{dc}
(V _{CE} = 100 V _{dc} , I _E = 0, T _C = 125°C)	MJE243, MJE244 MJE253, MJE254		—	0.1	
Emitter Cutoff Current (V _{BE} = 7.0 V _{dc} , I _C = 0)		I _{EBO}	—	0.1	μA _{dc}

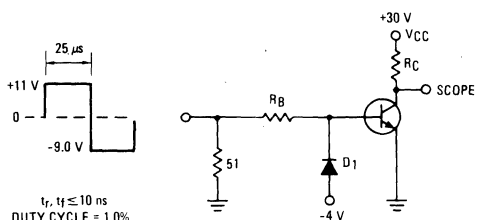
ON CHARACTERISTICS

DC Current Gain (I _C = 200 mA, V _{CE} = 1.0 V _{dc})	MJE240, MJE250 MJE241, MJE251, MJE243, MJE253 MJE252, MJE244, MJE254	h _{FE}	40 40 40 25	200 120 180 —	—
(I _C = 1.0 A, V _{CE} = 1.0 V _{dc})	MJE241, MJE251, MJE243, MJE253		20 15	— —	
(I _C = 1.0 A, V _{CE} = 1.0 V _{dc})	MJE252 MJE244, MJE254		10 15	— —	
(I _C = 2.0 A, V _{CE} = 1.0 V _{dc})	MJE240, MJE250		15	—	
Collector-Emitter Saturation Voltage (I _C = 500 mA, I _B = 50 mA)	All Types	V _{CE(sat)}	—	0.3	V _{dc}
(I _C = 1.0 A, I _B = 100 mA)	MJE241, MJE251, MJE243, MJE253		—	0.6	
(I _C = 2.0 A, I _B = 200 mA)	MJE252, MJE244, MJE254 MJE240, MJE250		—	0.8	
Base-Emitter Saturation Voltage (I _C = 2.0 A, I _B = 200 mA)		V _{BE(sat)}	—	1.8	V _{dc}
Base-Emitter On Voltage (I _C = 500 mA, V _{CE} = 1.0 V _{dc})		V _{BE(on)}	—	1.5	V _{dc}

DYNAMIC CHARACTERISTICS

Current-Gain – Bandwidth Product (I _C = 100 mA, V _{CE} = 10 V _{dc} , f _{test} = 10 MHz)		f _T	40	—	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 0.1 MHz)	MJE240/MJE244 MJE250/MJE254	C _{ob}	—	50 70	pF

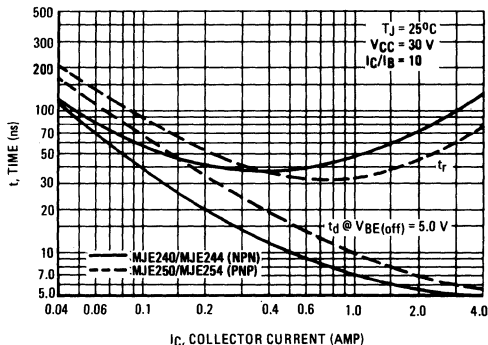
FIGURE 2 – SWITCHING TIME TEST CIRCUIT



D₁ MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B = 100 mA
MSD6100 USED BELOW I_B = 100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME



**MJE240, MJE241, MJE243, MJE244, NPN,
MJE250 thru MJE254, PNP**

FIGURE 4 – THERMAL RESPONSE

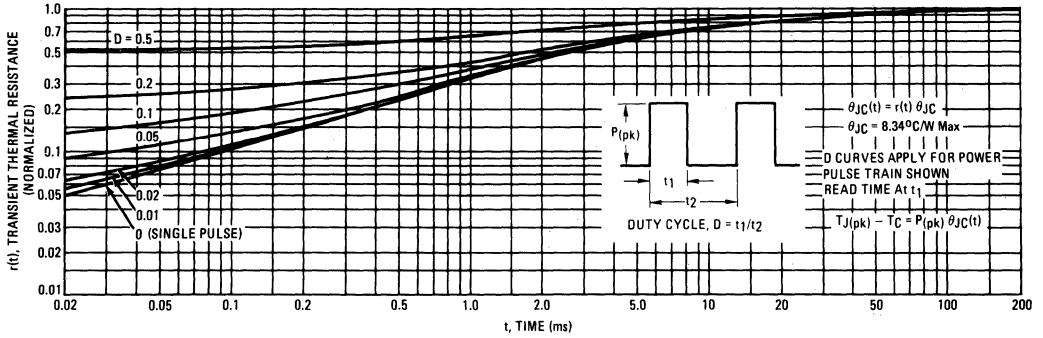
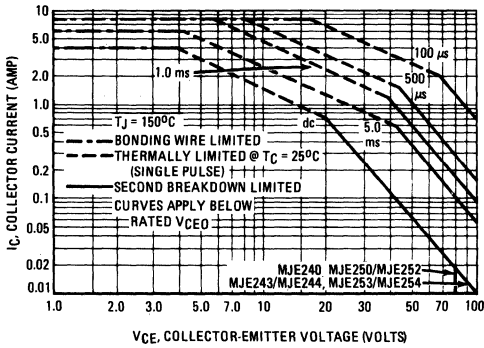


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

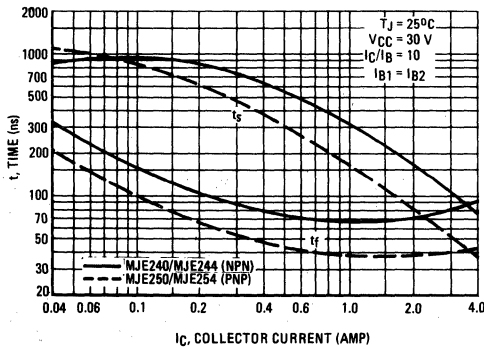
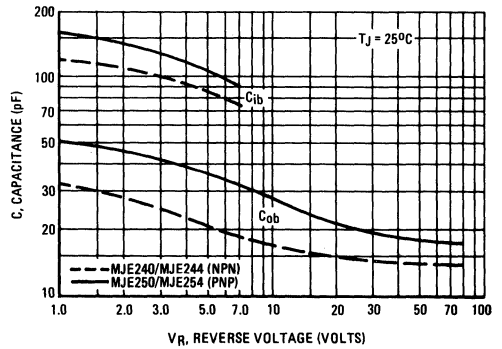


FIGURE 7 – CAPACITANCE



**MJE240, MJE241, MJE243, MJE244, NPN,
MJE250 thru MJE254, PNP**

**NPN
MJE240 thru MJE244**

**PNP
MJE250 thru MJE254**

FIGURE 8 – DC CURRENT GAIN

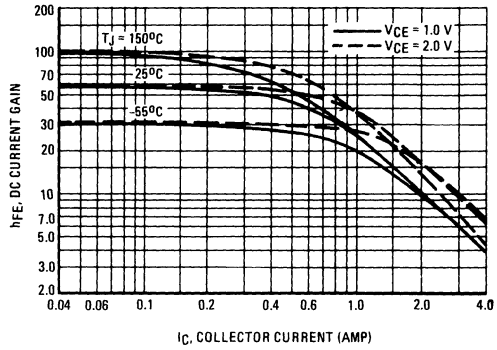
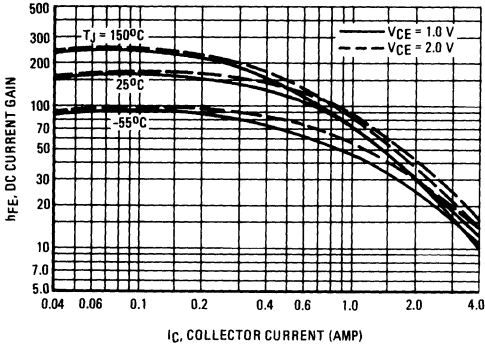


FIGURE 9 – "ON" VOLTAGES

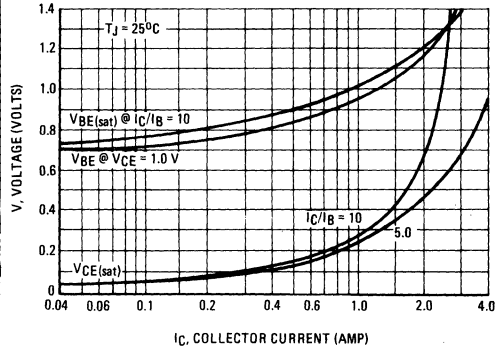
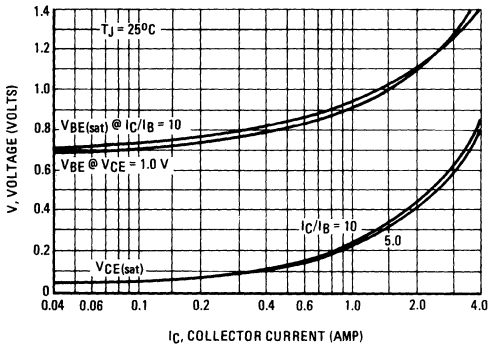
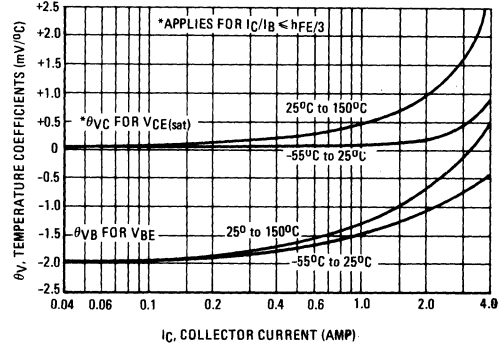
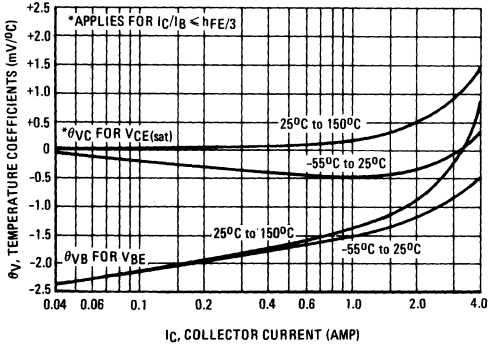


FIGURE 10 – TEMPERATURE COEFFICIENTS



3

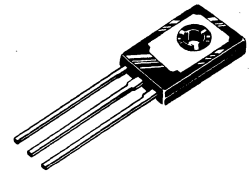
MJE340

**PLASTIC MEDIUM POWER NPN
 SILICON TRANSISTOR**

... useful for high-voltage general purpose applications.

- Suitable for Transformerless, Line-Operated Equipment
- Thermopad Construction Provides High Power Dissipation Rating for High Reliability

**0.5 AMPERE
 POWER TRANSISTOR
 NPN SILICON
 300 VOLTS
 20 WATTS**



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CE0}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mA dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20 0.16	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

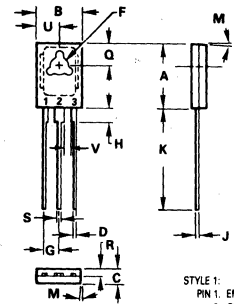
Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 1.0 \text{ mA dc}, I_E = 0$)	$V_{CE0(sus)}$	300	—	Vdc
Collector Cutoff Current ($V_{CB} = 300 \text{ Vdc}, I_E = 0$)	I_{CBO}	—	100	$\mu\text{A dc}$
Emitter Cutoff Current ($V_{EB} = 3.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	100	$\mu\text{A dc}$

ON CHARACTERISTICS

DC Current Gain ($I_C = 50 \text{ mA dc}, V_{CE} = 10 \text{ Vdc}$)	h_{FE}	30	240	—
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STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. BASE

NOTES:
 1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010)
 DIA TO DIM A & B AT MAXIMUM MATERIAL
 CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3" TYP		3" TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

FIGURE 1 – POWER TEMPERATURE DERATING

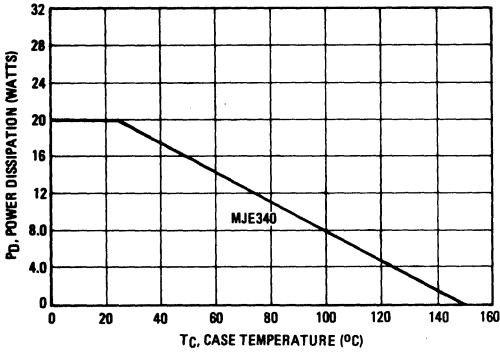
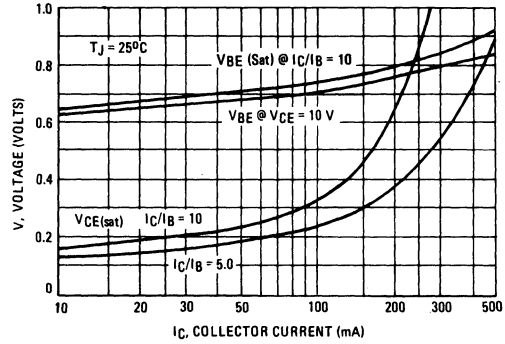
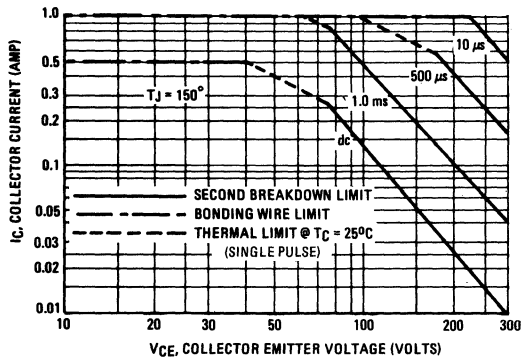


FIGURE 2 – "ON" VOLTAGES



ACTIVE-REGION SAFE OPERATING AREA

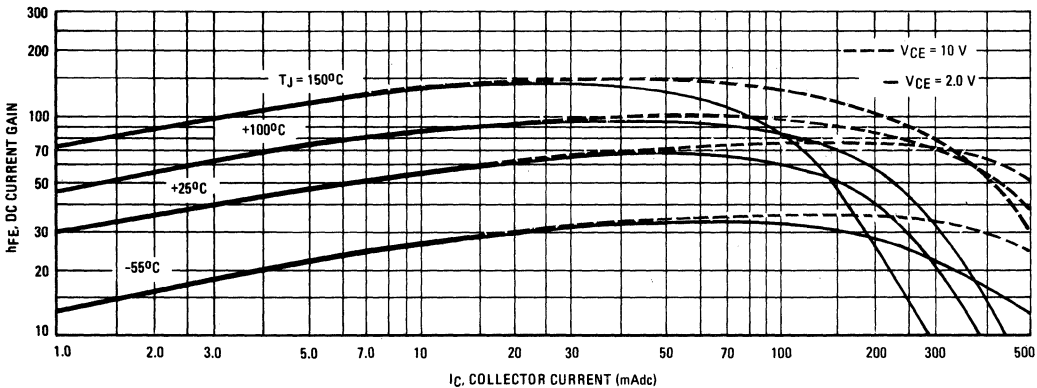
FIGURE 3 – MJE340



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 – DC CURRENT GAIN



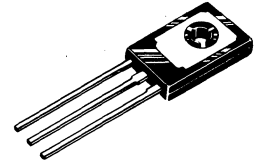
**PLASTIC NPN SILICON
MEDIUM-POWER TRANSISTORS**

...useful for medium voltage applications requiring high f_T such as converters and extended range amplifiers.

**0.5 AMPERE
POWER TRANSISTORS
NPN SILICON
150-200 VOLTS
20 WATTS**

MAXIMUM RATINGS

Rating	Symbol	MJE341	MJE344	Unit
Collector-Emitter Voltage	V_{CEO}	150	200	Vdc
Collector-Base Voltage	V_{CB}	175	200	Vdc
Emitter-Base Voltage	V_{EB}	3.0	5.0	Vdc
Collector Current — Continuous	I_C	500		mAdc
Base Current	I_B	250		mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20	0.16	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$



THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^\circ\text{C}/\text{W}$

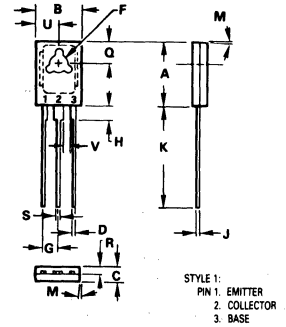
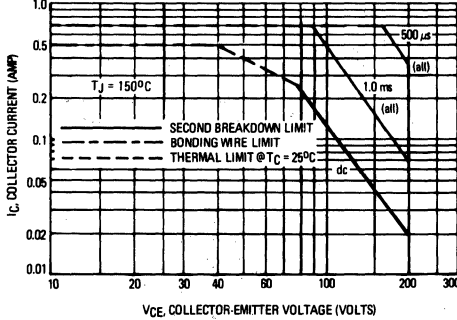


FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.29	0.045	0.051
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

MJE341, MJE344

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($I_C = 1.0 \text{ mAdc}$, $I_B = 0$)	MJE341 MJE344	$V_{CE(sus)}$	150 200	— —	Vdc
Collector Cutoff Current ($V_{CE} = 150 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 200 \text{ Vdc}$, $I_B = 0$)	MJE341 MJE344	I_{CEO}	— —	1.0 1.0	mAdc
Collector Cutoff Current ($V_{CB} = 175 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 200 \text{ Vdc}$, $I_E = 0$)	MJE341 MJE344	I_{CBO}	— —	0.3 0.1	mAdc
Emitter Cutoff Current ($V_{EB} = 3.0 \text{ Vdc}$, $I_C = 0$) ($V_{EB} = 5.0 \text{ Vdc}$, $I_C = 0$)	MJE341 MJE344	I_{EBO}	— —	0.1 0.1	mAdc

ON CHARACTERISTICS

DC Current Gain ($I_C = 10 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$) ($I_C = 50 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$) ($I_C = 150 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$)	MJE341 MJE341 MJE344 MJE341	h_{FE}	20 25 30 20	— 200 300 —	—
Collector-Emitter Saturation Voltage ($I_C = 50 \text{ mAdc}$, $I_B = 5.0 \text{ mAdc}$) ($I_C = 150 \text{ mAdc}$, $I_B = 15 \text{ mAdc}$)	MJE344 MJE341	$V_{CE(sat)}$	— —	1.0 2.3	Vdc
Base-Emitter On Voltage ($I_C = 50 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$)		$V_{BE(on)}$	—	1.0	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 50 \text{ mAdc}$, $V_{CE} = 25 \text{ Vdc}$, $f = 10 \text{ MHz}$)	f_T	15	—	MHz
Output Capacitance ($V_{CB} = 20 \text{ Vdc}$, $I_E = 0$, $f = 100 \text{ kHz}$)	C_{ob}	—	15	pF
Small-Signal Current Gain ($I_C = 50 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	25	—	—

FIGURE 2 — DC CURRENT GAIN

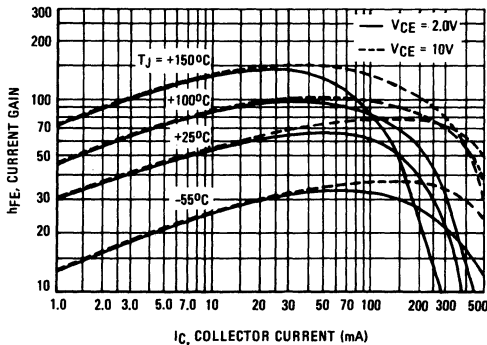
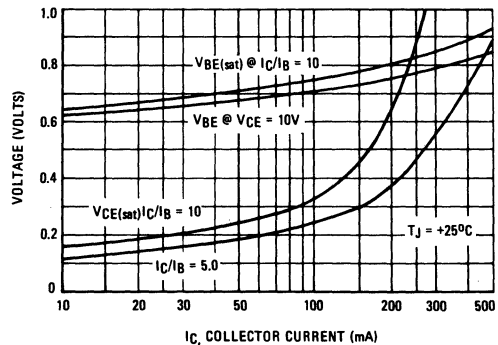


FIGURE 3 — "ON" VOLTAGES



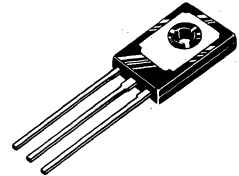
**PLASTIC MEDIUM POWER PNP
 SILICON TRANSISTOR**

... designed for use in line-operated applications such as low power, line-operated series pass and switching regulators requiring PNP capability.

- High Collector-Emitter Sustaining Voltage –
 $V_{CE0(sus)} = 300 \text{ Vdc @ } I_C = 1.0 \text{ mAdc}$
- Excellent DC Current Gain –
 $h_{FE} = 30-240 @ I_C = 50 \text{ mAdc}$
- Plastic Thermopad Package:

**0.5 AMPERE
 POWER TRANSISTOR
 PNP SILICON**

**300 VOLTS
 20 WATTS**



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

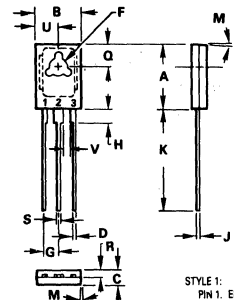
Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 1.0 \text{ mAdc}, I_B = 0$)	$V_{CE0(sus)}$	300	–	Vdc
Collector Cutoff Current ($V_{CB} = 300 \text{ Vdc}, I_E = 0$)	I_{CBO}	–	100	μAdc
Emitter Cutoff Current ($V_{EB} = 3.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	–	100	μAdc

ON CHARACTERISTICS

DC Current Gain ($I_C = 50 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$)	h_{FE}	30	240	–
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STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. BASE

NOTES:

- LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.096
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	2 TYP		2 TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	–	0.040	–

CASE 77-05

FIGURE 1 – DC CURRENT GAIN

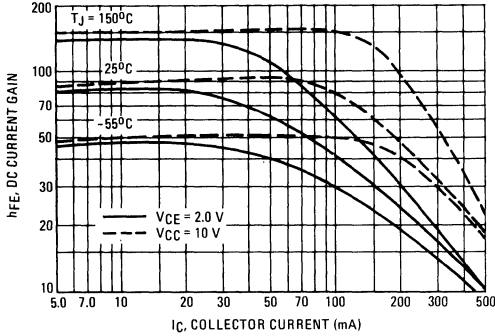


FIGURE 2 – "ON" VOLTAGES

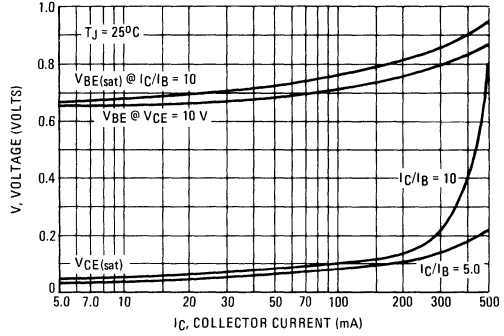


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA

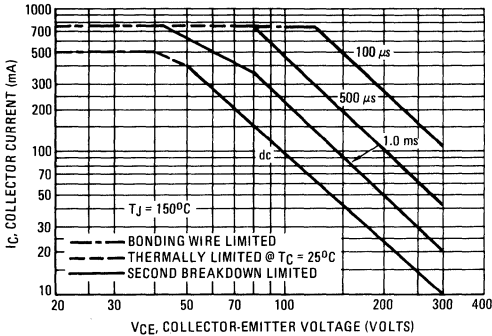
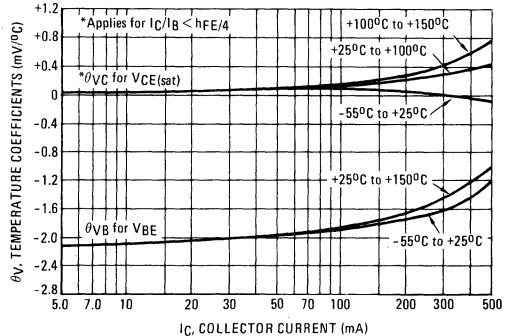


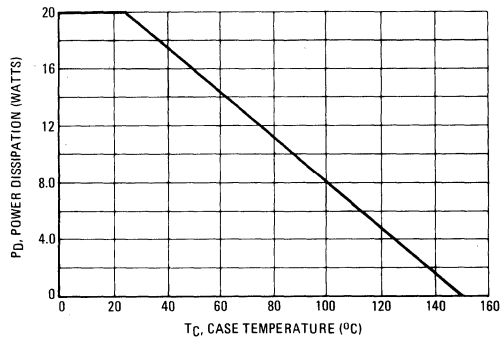
FIGURE 4 – TEMPERATURE COEFFICIENTS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 5 – POWER DERATING



**PLASTIC MEDIUM-POWER PNP
 SILICON TRANSISTOR**

... designed for use in general-purpose amplifiers and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain – $h_{FE} = 25$ (Min) @ $I_C = 1.0$ Adc
- Complementary to NPN MJE520

**3 AMPERE
 POWER TRANSISTOR
 PNP SILICON**

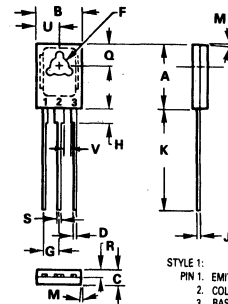
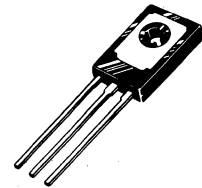
**30 VOLTS
 25 WATTS**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	3.0	A dc
– Peak		7.0	
Base Current – Continuous	I_B	2.0	A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	25 0.2	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	$^\circ\text{C}/\text{W}$



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 100$ mA dc, $I_B = 0$)	$V_{CEO(sus)}$	30	—	Vdc
Collector-Base Cutoff Current ($V_{CB} = 30$ Vdc, $I_E = 0$)	I_{CBO}	—	100	μA dc
Emitter-Base Cutoff Current ($V_{EB} = 4.0$ Vdc, $I_C = 0$)	I_{EBO}	—	100	μA dc

ON CHARACTERISTICS

DC Current Gain ($I_C = 1.0$ A dc, $V_{CE} = 1.0$ Vdc)	h_{FE}	25	—	—
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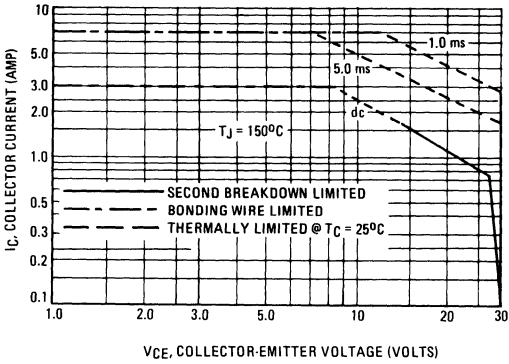
(1) Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$.

NOTES:
 1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – DC CURRENT GAIN

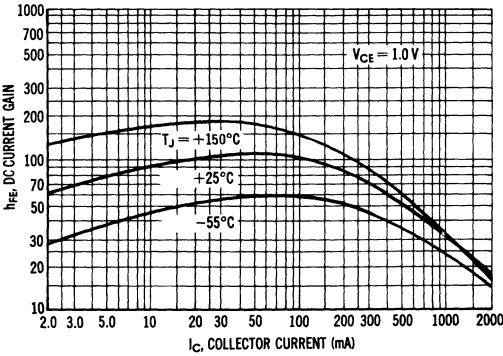


FIGURE 3 – "ON" VOLTAGE

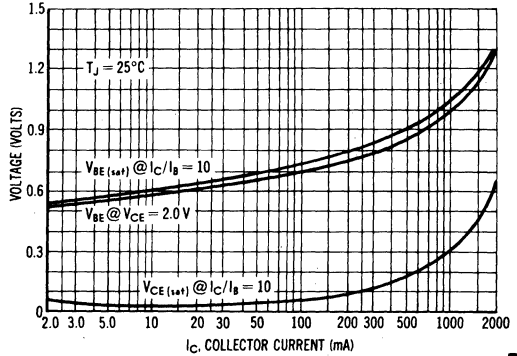
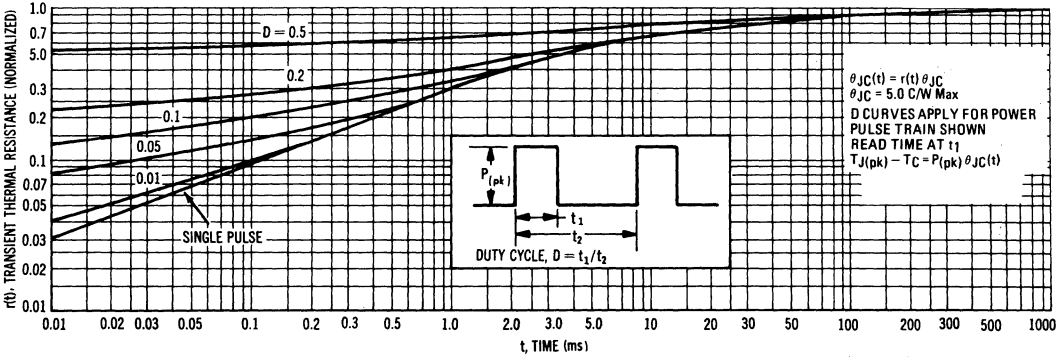


FIGURE 4 – THERMAL RESPONSE



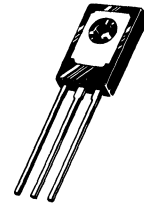
**PLASTIC MEDIUM-POWER PNP
 SILICON TRANSISTORS**

... designed for use in general-purpose amplifier and switching circuits. Recommended for use in 5 to 20 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain – $h_{FE} = 40$ (Min) @ $I_C = 1.0$ Adc
- MJE371 is Complementary to NPN MJE521

**4 AMPERE
 POWER TRANSISTORS
 PNP SILICON**

**40 VOLTS
 40 WATTS**



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	4.0	Adc
– Peak		8.0	
Base Current – Continuous	I_B	2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40 320	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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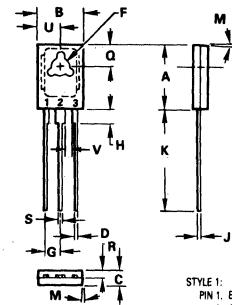
OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 100$ mA dc, $I_B = 0$)	$V_{CEO(sus)}$	40	–	Vdc
Collector-Base Cutoff Current ($V_{CB} = 40$ Vdc, $I_E = 0$)	I_{CBO}	–	100	μA dc
Emitter-Base Cutoff Current ($V_{EB} = 4.0$ Vdc, $I_C = 0$)	I_{EBO}	–	100	μA dc

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 1.0$ Adc, $V_{CE} = 1.0$ Vdc)	h_{FE}	40	–	–
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(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$ Duty Cycle $\leq 2.0\%$.



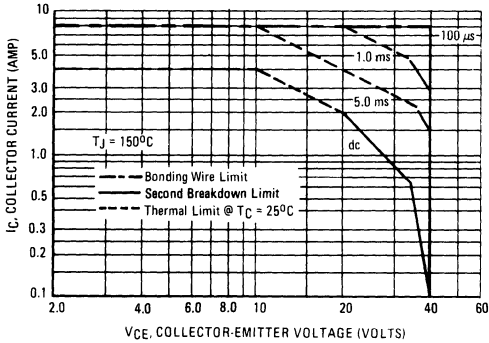
STYLE 1:
 PIN 1, EMITTER
 2, COLLECTOR
 3, BASE

NOTES:
 1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	2 TYP		2 TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	–	0.040	–

CASE 77-05

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – DC CURRENT GAIN

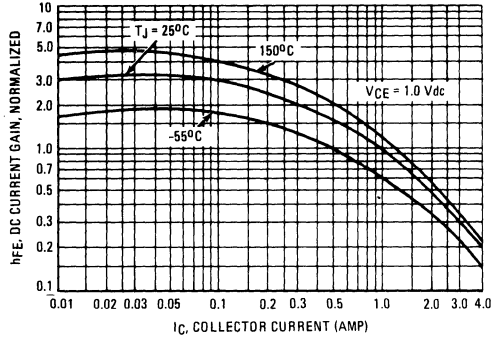


FIGURE 3 – "ON" VOLTAGE

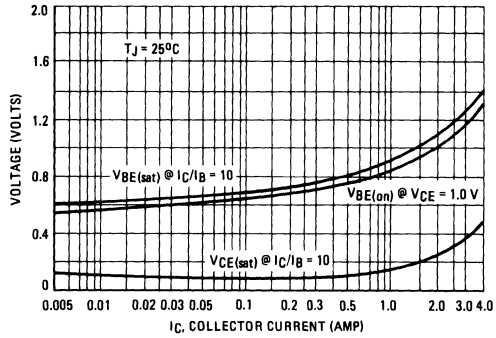
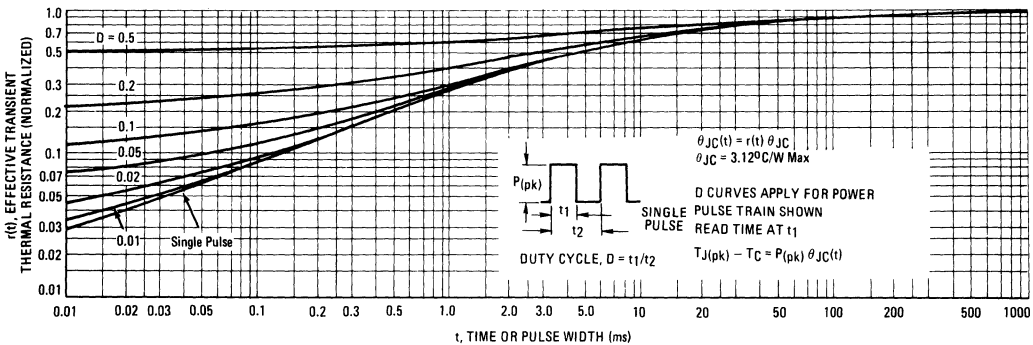


FIGURE 4 – THERMAL RESPONSE



**PLASTIC MEDIUM-POWER NPN
 SILICON TRANSISTOR**

... designed for use in general-purpose amplifier and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain – $h_{FE} = 25$ (Min) @ $I_C = 1.0$ Adc
- Complementary to PNP MJE370

**3 AMPERE
 POWER TRANSISTOR
 NPN SILICON**

**30 VOLTS
 25 WATTS**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	3.0	A dc
– Peak		7.0	
Base Current – Continuous	I_B	2.0	A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	25 0.2	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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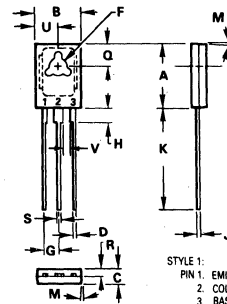
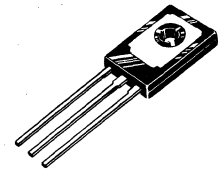
OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 100$ mAdc, $I_B = 0$)	$V_{CEO(sus)}$	30	–	Vdc
Collector-Base Cutoff Current ($V_{CB} = 30$ Vdc, $I_E = 0$)	I_{CBO}	–	100	$\mu\text{A dc}$
Emitter-Base Cutoff Current ($V_{EB} = 4.0$ Vdc, $I_C = 0$)	I_{EBO}	–	100	$\mu\text{A dc}$

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 1.0$ Adc, $V_{CE} = 1.0$ Vdc)	h_{FE}	25	–	–
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(1) Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2.0\%$.

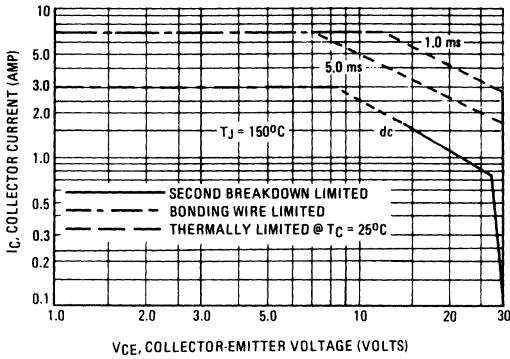


NOTES:
 1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.69	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	Ø TYP		Ø TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	–	0.040	–

CASE 77-05

FIGURE 1 ACTIVE-REGION SAFE OPERATING AREA



The data of Figure 1 based on $T_J(pk) = 150^\circ C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $(T_{Jpk}) \leq 150^\circ C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

FIGURE 2 - DC CURRENT GAIN

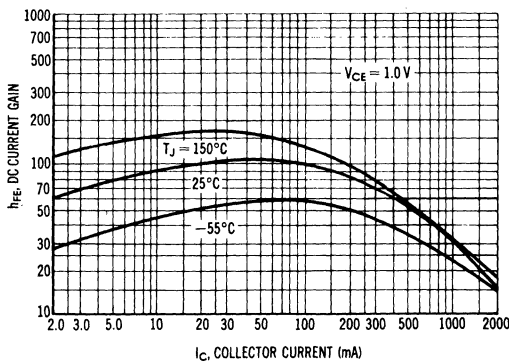


FIGURE 3 - "ON" VOLTAGE

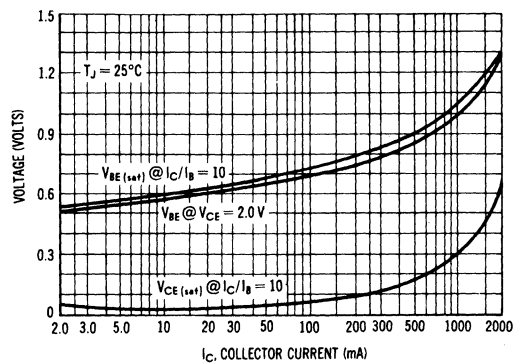
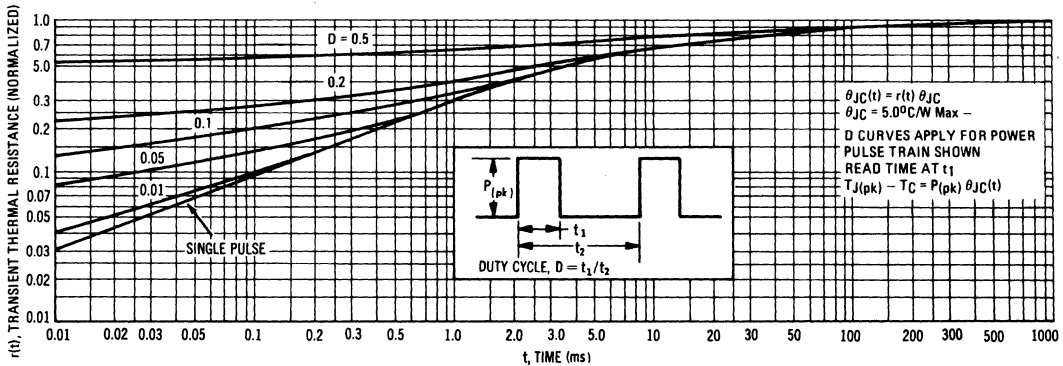


FIGURE 4 - THERMAL RESPONSE



PLASTIC DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
 $h_{FE} = 2000$ (Typ) @ $I_C = 2.0$ Adc
- Monolithic Construction with Built-in Base-Emitter Resistors to Limit Leakage Multiplication
- Choice of Packages –
MJE700 and MJE800 series
TO220AB, MJE700T and MJE800T

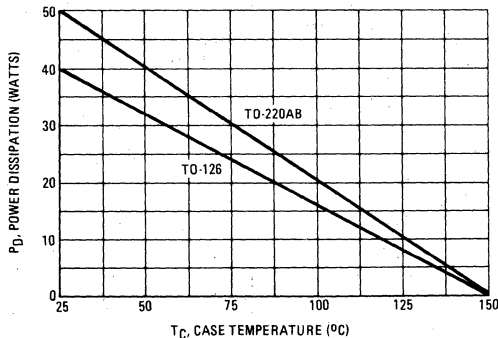
MAXIMUM RATINGS

Rating	Symbol	MJE700,T MJE701 MJE800,T MJE801	MJE702 MJE703 MJE802 MJE803	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	0.1		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	CASE 77	TO-220	Watts $W/^\circ\text{C}$
		40	50	
		0.32	0.40	
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case CASE 77 TO-220	$R_{\theta JC}$	3.13 2.50	$^\circ\text{C/W}$

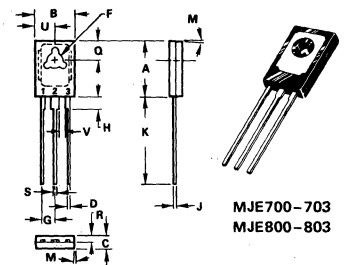
FIGURE 1 – POWER DERATING



4.0 AMPERE

DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

40 WATT
50 WATT

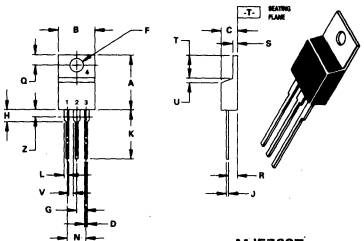


STYLE 1:
PIN 1: EMITTER
2: COLLECTOR
3: BASE

MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX
A	15.00	15.04	0.591	0.592
B	7.50	7.74	0.295	0.305
C	2.42	2.68	0.095	0.105
D	0.51	0.66	0.020	0.025
F	2.93	3.17	0.115	0.125
G	0.32	2.66	0.012	0.105
H	1.27	2.41	0.050	0.095
J	0.32	0.63	0.012	0.025
K	14.61	16.63	0.575	0.655
M	TYP			
Q	3.76	4.01	0.148	0.158
R	1.15	1.29	0.045	0.050
S	0.64	0.68	0.025	0.025
U	3.89	3.93	0.153	0.155
V	1.01	—	—	0.040

NOTES:
1. LEADS: TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

CASE 77-05



MJE700T
MJE800T

STYLE 1:
PIN 1: BASE
2: COLLECTOR
3: EMITTER
4: COLLECTOR

MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	6.86	10.28	0.269	0.405
C	4.87	4.82	0.190	0.190
D	0.64	0.68	0.025	0.025
F	3.81	3.73	0.149	0.147
G	2.42	2.66	0.095	0.105
H	2.86	3.83	0.113	0.150
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.29	0.045	0.050
M	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	1.04	2.78	0.040	0.110
S	1.15	1.29	0.045	0.050
T	6.97	6.47	0.274	0.255
U	0.50	1.27	0.020	0.050
V	1.15	—	—	0.045
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

PNP MJE700,T thru MJE703 NPN MJE800,T thru MJE803

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I _C = 50 mA, I _B = 0)	V _{(BR)CEO}	60 80	— —	V _{dc}
Collector Cutoff Current (V _{CE} = 60 V _{dc} , I _B = 0) (V _{CE} = 80 V _{dc} , I _B = 0)	I _{CEO}	— —	100 100	μA _{dc}
Collector Cutoff Current (V _{CB} = Rated BV _{CEO} , I _E = 0) (V _{CB} = Rated BV _{CEO} , I _E = 0, T _C = 100°C)	I _{CBO}	— —	100 500	μA _{dc}
Emitter Cutoff Current (V _{BE} = 5.0 V _{dc} , I _C = 0)	I _{EBO}	—	2.0	mA _{dc}
ON CHARACTERISTICS				
DC Current Gain (1) (I _C = 1.5 A _{dc} , V _{CE} = 3.0 V _{dc}) (I _C = 2.0 A _{dc} , V _{CE} = 3.0 V _{dc}) (I _C = 4.0 A _{dc} , V _{CE} = 3.0 V _{dc})	h _{FE}	MJE700,T MJE702, MJE800,T MJE802 MJE701, MJE703, MJE801, MJE803 All devices	750 750 100	—
Collector-Emitter Saturation Voltage (1) (I _C = 1.5 A _{dc} , I _B = 30 mA _{dc}) (I _C = 2.0 A _{dc} , I _B = 40 mA _{dc}) (I _C = 4.0 A _{dc} , I _B = 40 mA _{dc})	V _{CE(sat)}	MJE700,T MJE702, MJE800,T MJE802 MJE701, MJE703, MJE801, MJE803 All devices	— — —	V _{dc}
Base-Emitter On Voltage (1) (I _C = 1.5 A _{dc} , V _{CE} = 3.0 V _{dc}) (I _C = 2.0 A _{dc} , V _{CE} = 3.0 V _{dc}) (I _C = 4.0 A _{dc} , V _{CE} = 3.0 V _{dc})	V _{BE(on)}	MJE700,T MJE702, MJE800,T MJE802 MJE701, MJE703, MJE801, MJE803 All devices	— — —	V _{dc}
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I _C = 1.5 A _{dc} , V _{CE} = 3.0 V _{dc} , f = 1.0 MHz)	h _{fe}	1.0	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT

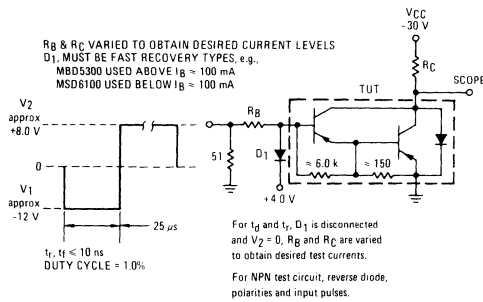


FIGURE 3 — SWITCHING TIMES

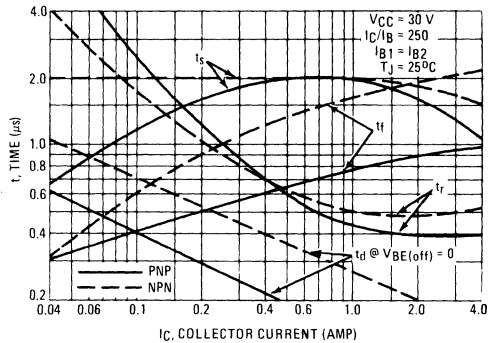
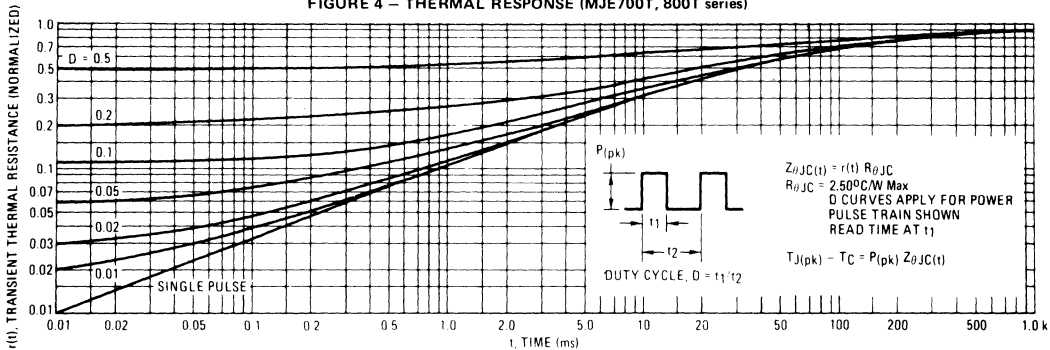
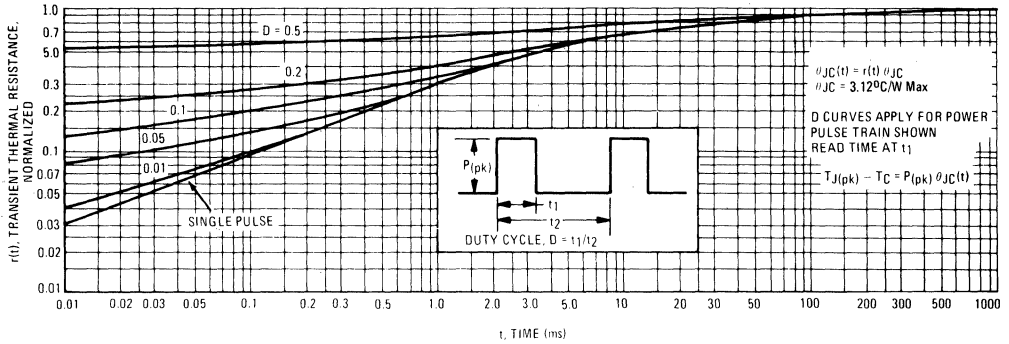


FIGURE 4 — THERMAL RESPONSE (MJE700T, 800T series)



PNP MJE700,T thru MJE703
NPN MJE800,T thru MJE803

FIGURE 5 – THERMAL RESPONSE (MJE700, 800 series)



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 6 – MJE700 series

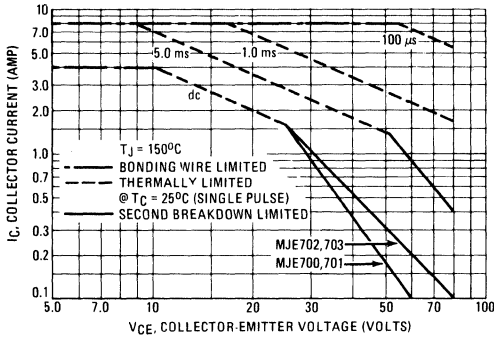
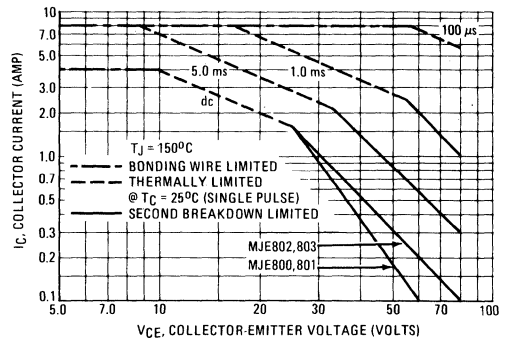


FIGURE 7 – MJE800 series



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 6 and 7 are based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4 or 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 – MJE700T

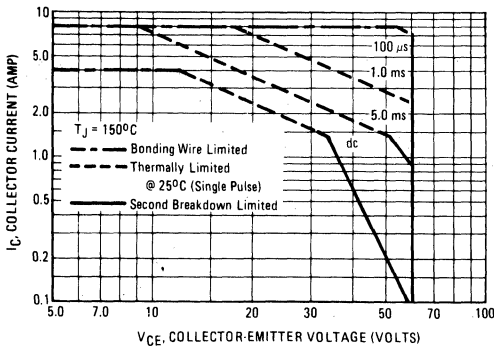
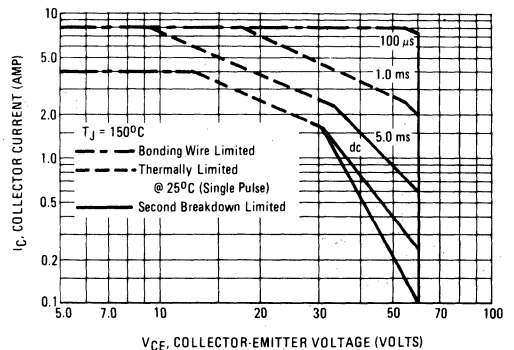


FIGURE 9 – MJE800T



PNP MJE700,T thru MJE703
NPN MJE800,T thru MJE803

PNP
MJE700,T series

NPN
MJE800,T series

FIGURE 10 – DC CURRENT GAIN

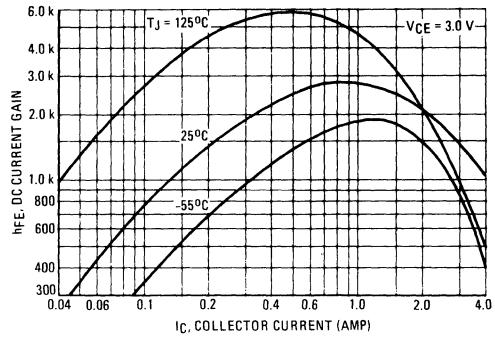
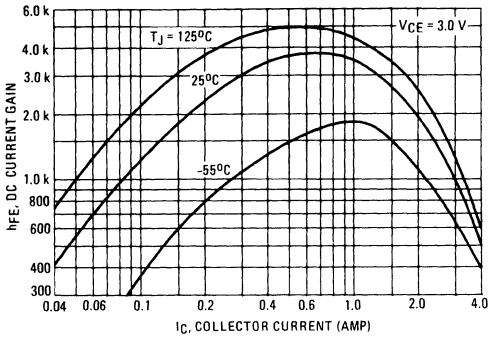


FIGURE 11 – COLLECTOR SATURATION REGION

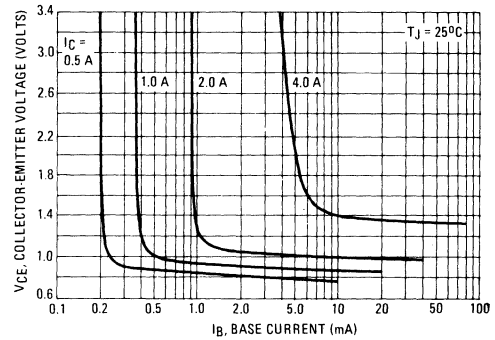
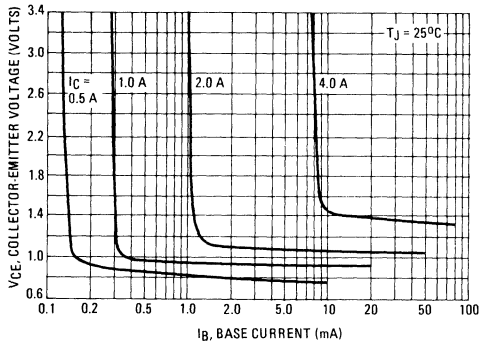
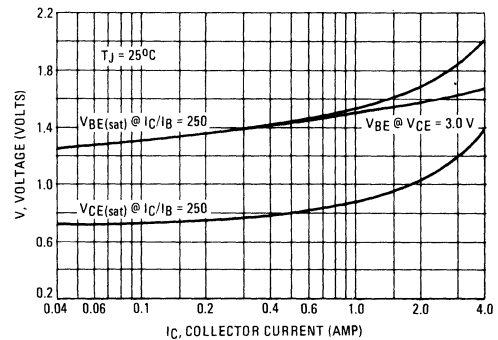
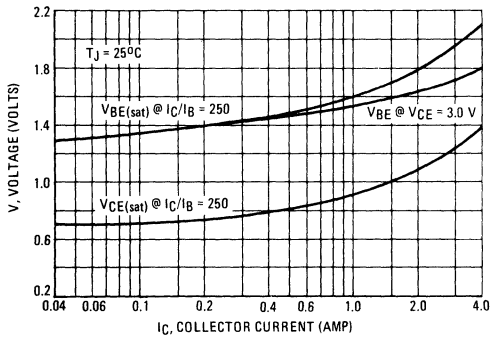


FIGURE 12 – "ON" VOLTAGES



Designer's Data Sheet
NPN Silicon Power Transistor
Switchmode III Series

This transistor is designed for high-voltage, power switching in inductive circuits where RBSOA and breakdown voltage are critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Fluorescent Lamp Ballasts
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Features:

- High V_{CEV} Capability (1800 Volts)
- Low Saturation Voltage
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	900	Vdc
Collector-Emitter Voltage	V_{CEV}	1800	Vdc
Emitter Base Voltage	V_{EB}	9	Vdc
Collector Current — Continuous Peak ⁽¹⁾	I_C	2	Adc
	I_{CM}	5	
Base Current — Continuous Peak ⁽¹⁾	I_B	1.5	Adc
	I_{BM}	2.5	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C @ $T_C = 100^\circ\text{C}$	P_D	80	Watts
		32	
		0.64	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

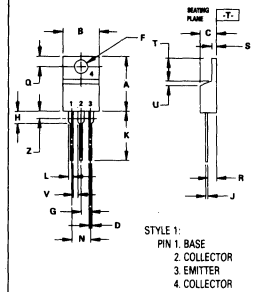
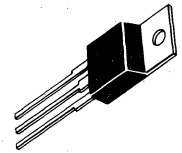
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

MJE1320

POWER TRANSISTOR
2 AMPERES
900 VOLTS
80 WATTS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.56	10.29	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
O	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
(TO-220AB)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($I_C = 50\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	900	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.25 2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 9\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	0.25	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 13			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 14			

ON CHARACTERISTICS(1)

DC Current Gain ($V_{CE} = 5\text{ Vdc}$)	$I_C = 2\text{ Adc}$ $I_C = 1\text{ Adc}$	h_{FE}	2.5 3	4.5 7	— —	— —
Collector-Emitter Saturation Voltage ($I_C = 1\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 2\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.5\text{ Adc}$, $T_C = 100^\circ\text{C}$)		$V_{CE(sat)}$	— — —	0.18 0.3 0.3	1 2.5 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 1\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 2\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.5\text{ Adc}$, $T_C = 100^\circ\text{C}$)		$V_{BE(sat)}$	— — —	0.2 0.9 0.15	1.5 2.8 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1\text{ MHz}$)	C_{ob}	—	80	—	pF
--	----------	---	----	---	----

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	$V_{CC} = 250\text{ Vdc}$, $I_C = 1\text{ A}$ $I_{B1} = I_{B2} = 0.5\text{ Adc}$ $t_p = 25\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$	t_d	—	0.1	—	μs	
Rise Time		t_r	—	0.8	—	μs	
Storage Time		t_s	—	4	—	μs	
Fall Time		t_f	—	0.8	—	μs	
Inductive Load, Clamped (Table 2)							
Storage Time	$I_C = 1\text{ A}$, $V_{clamp} = 400\text{ Vdc}$, $V_{BE(off)} = 2\text{ Vdc}$, $I_{B1} = 0.5\text{ Adc}$	$T_C = 25^\circ\text{C}$	t_{sv}	—	2.8	—	μs
Crossover Time			t_c	—	2.2	—	μs
Storage Time		$T_C = 100^\circ\text{C}$	t_{sv}	—	3.7	10.5	μs
Crossover Time			t_c	—	3.5	10	μs
Fall Time							

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

TYPICAL STATIC CHARACTERISTICS

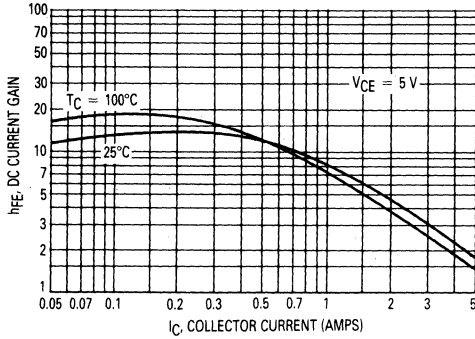


Figure 1. DC Current Gain

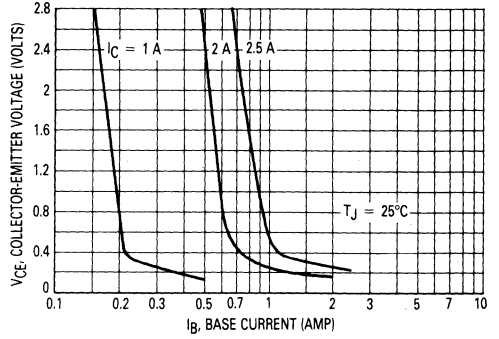


Figure 2. Collector Saturation Region

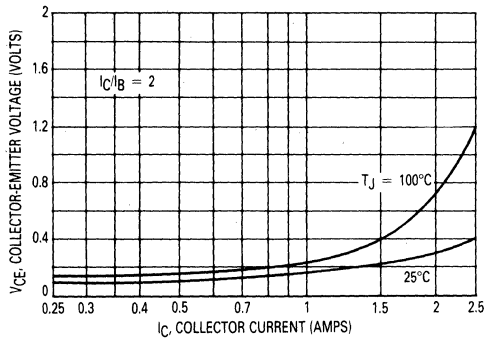


Figure 3. Collector Emitter Saturation Voltage

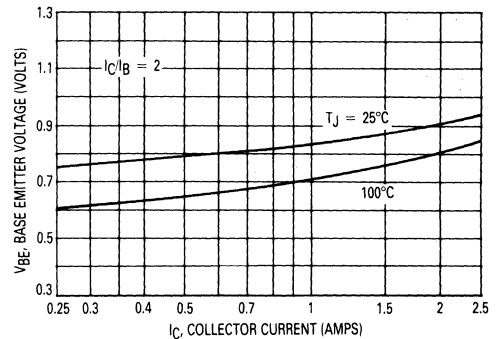


Figure 4. Base Emitter Saturation Voltage

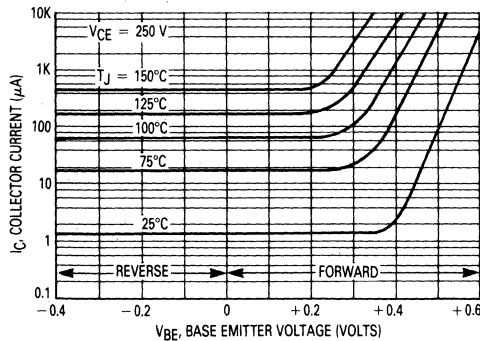


Figure 5. Collector Cutoff Region

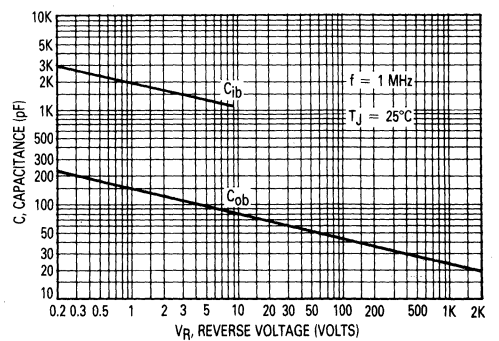


Figure 6. Capacitance Variation

TYPICAL DYNAMIC CHARACTERISTICS

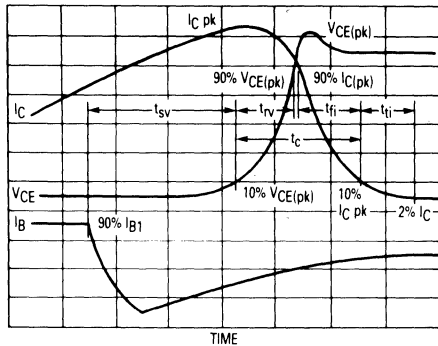


Figure 7. Inductive Switching Measurements

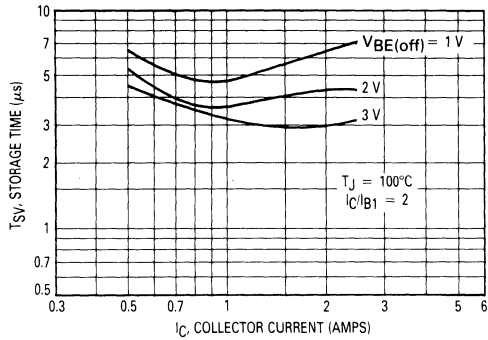


Figure 8. Inductive Storage Time

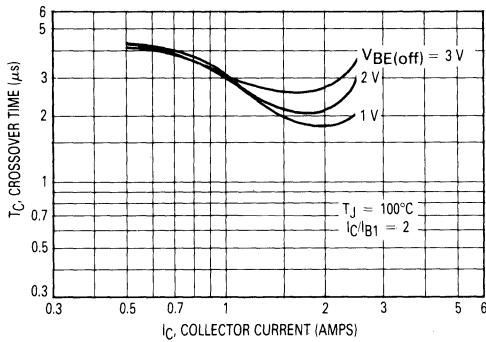


Figure 9. Inductive Crossover Time

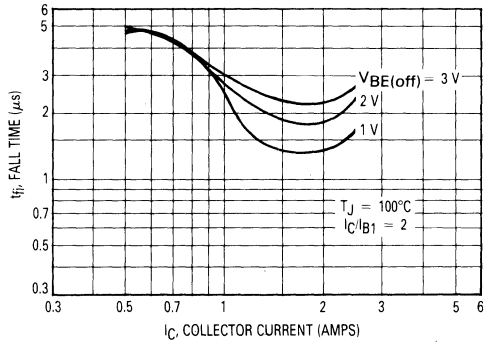
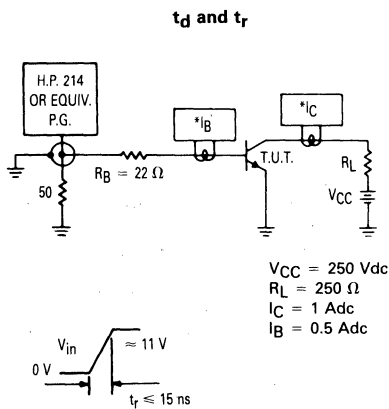


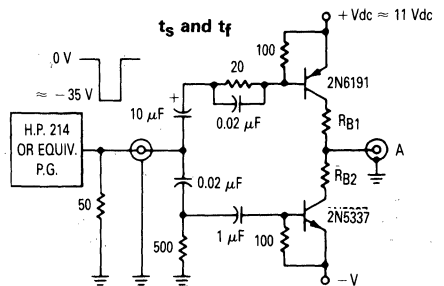
Figure 10. Inductive Fall Time

Table 1. Resistive Load Switching



$V_{CC} = 250 \text{ Vdc}$
 $R_L = 250 \Omega$
 $I_C = 1 \text{ Adc}$
 $I_B = 0.5 \text{ Adc}$

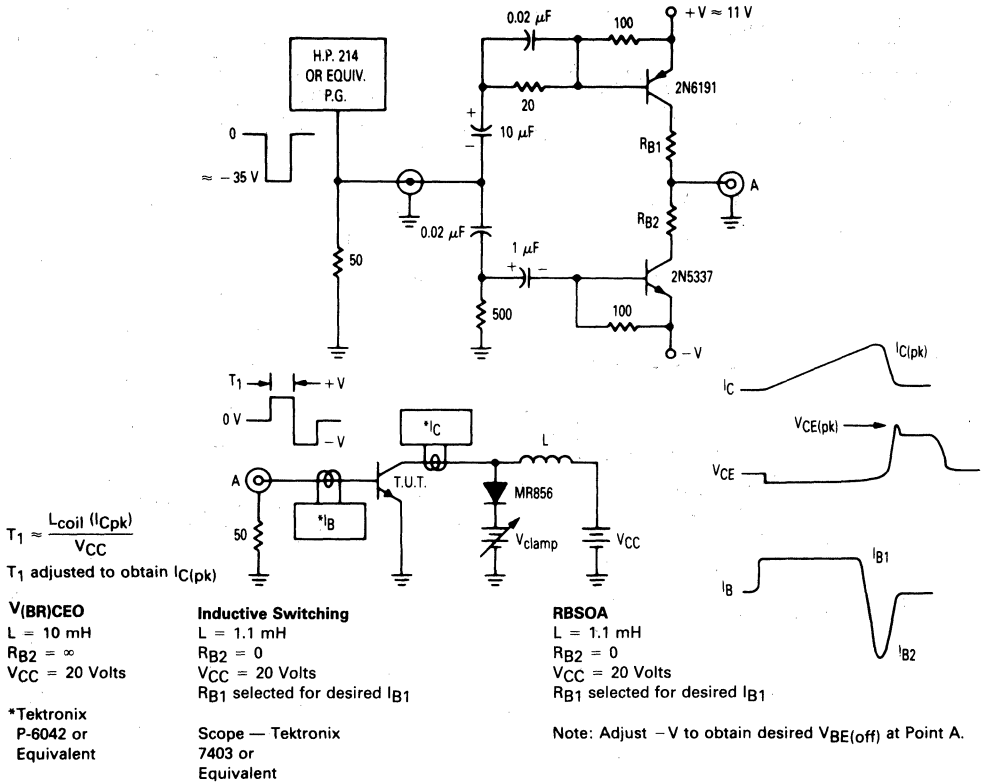
*Tektronix AM503
 P6302 or Equivalent



$V_{CC} = 250 \text{ Vdc}$ $I_{B1} = 0.5 \text{ Adc}$ $R_{B1} = 22 \Omega$
 $R_L = 250 \Omega$ $I_{B2} = 0.5 \text{ Adc}$ $R_{B2} = 10 \Omega$
 $I_C = 1 \text{ Adc}$ For $V_{BE(off)} = 5 \text{ V}$ $R_{B2} = 0 \Omega$

Note: Adjust $-V$ to obtain desired $V_{BE(off)}$ at point A.

Table 2. Inductive Load Switching



3

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_J(pk)$ may be calculated from the data in Figure 14. At high case temperatures, thermal limitations will

reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

GUARANTEED SAFE OPERATING AREA

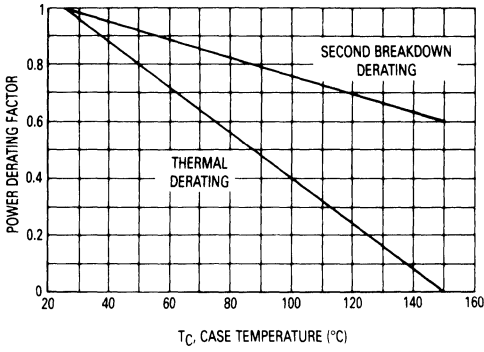


Figure 11. Power Derating

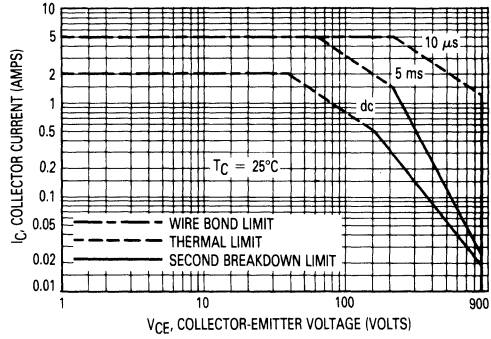


Figure 12. Maximum Rated Forward Bias Safe Operating Area

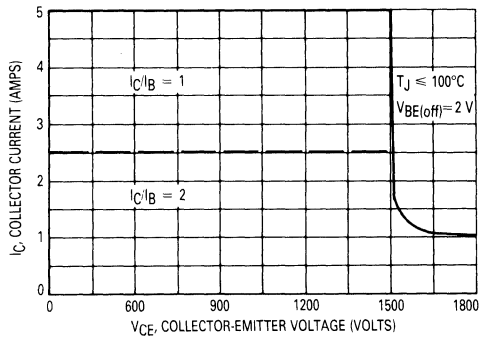


Figure 13. Maximum Rated Reverse Bias Safe Operating Area

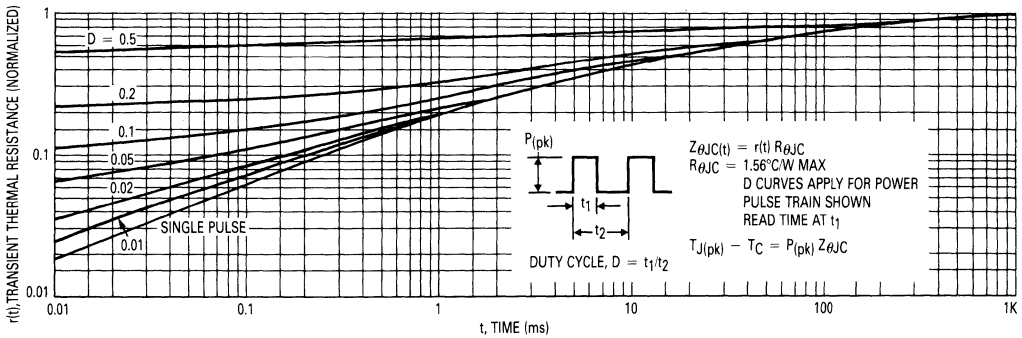


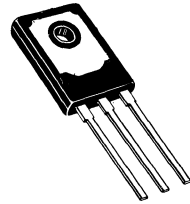
Figure 14. Thermal Response

SILICON
MEDIUM-POWER TRANSISTORS

... designed for use in power amplifier and switching applications.

- High Collector Current –
 $I_C = 15 \text{ A dc}$
- High DC Current Gain –
 $h_{FE} = 10 \text{ (Min) @ } I_C = 15 \text{ A dc}$

15 AMPERE
POWER TRANSISTORS
SILICON
40-60 VOLTS
90 WATTS



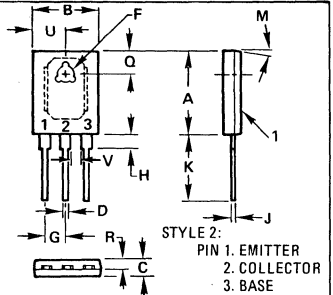
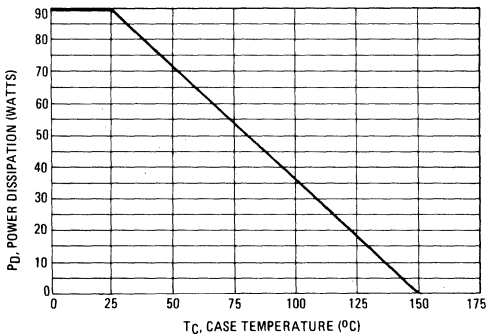
MAXIMUM RATINGS

Rating	Symbol	MJE1660	MJE1661	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Base Voltage	V_{CB}	40	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current-Continuous	I_C	15		A dc
Base Current	I_B	5.0		A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	90	0.72	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	$^\circ\text{C}/\text{W}$

FIGURE 1 – POWER TEMPERATURE DERATING CURVE



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	90 TYP		90 TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	-	0.080	-

CASE 90-05
TO-225AB

When mounting the device, torque not to exceed 8.0 in.-lb.

If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

MJE1660, MJE1661 NPN

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 200 \text{ mA}$, $I_B = 0$)	MJE 1660 MJE 1661	$V_{CE(sus)}$	40 60	—	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$)		I_{CEO}	—	1.0	mA
Collector Cutoff Current ($V_{CE} = 40 \text{ Vdc}$, $V_{BE} = 0$) ($V_{CE} = 60 \text{ Vdc}$, $V_{BE} = 0$)	MJE 1660 MJE 1661	I_{CES}	— —	0.7 0.7	mA
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$)	MJE 1660 MJE 1661	I_{CBO}	— —	0.7 0.7	mA
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_E = 0$)		I_{EBO}	—	1.0	mA

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 5.0 \text{ A}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 15 \text{ A}$, $V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	20 10	100 —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 15 \text{ A}$, $I_B = 1.5 \text{ A}$)	$V_{CE(sat)}$	—	1.8	Vdc
Base-Emitter on Voltage (1) ($I_C = 15 \text{ A}$, $V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	—	2.5	Vdc

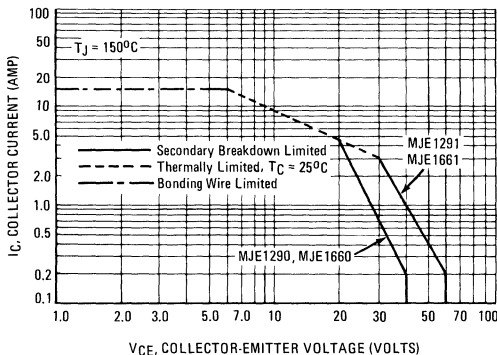
DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 1.0 \text{ A}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	f_T	3.0	—	MHz
Small-Signal Current Gain ($I_C = 1.0 \text{ A}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	25	—	—

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$. Duty Cycle $\leq 2.0\%$.

3

FIGURE 2 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C - V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

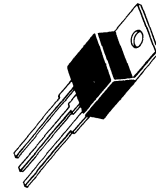
NPN SILICON HIGH-VOLTAGE TRANSISTOR

... useful for general-purpose, high voltage applications requiring high f_T .

- Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 350 \text{ Vdc (Min) @ } I_C = 2.5 \text{ mAdc}$
- DC Current Gain –
 $h_{FE} = 40 \text{ (Min) @ } I_C = 100 \text{ mAdc – MJE2361T}$
- Current-Gain-Bandwidth Product –
 $f_T = 10 \text{ MHz (Typ) @ } I_C = 50 \text{ mAdc}$

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON

350 VOLTS
30 WATTS

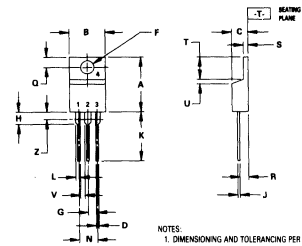
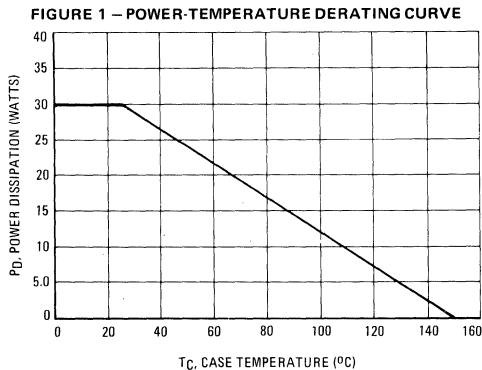


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	350	Vdc
Collector-Base Voltage	V_{CB}	375	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous	I_C	0.5	Adc
Base Current	I_B	0.25	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	30 0.24	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.167	$^\circ\text{C/W}$



NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.38	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.38	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.90	1.27	0.030	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
 PIN 1: BASE
 2: COLLECTOR
 3: EMITTER
 4: COLLECTOR

CASE 221A-04
TO-220AB

MJE2360T , MJE2361T

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage(1) ($I_C = 2.5 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	350	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 250 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	—	0.25	mAdc
Collector Cutoff Current ($V_{CE} = 375 \text{ Vdc}$, $V_{EB(off)} = 1.5 \text{ Vdc}$)	I_{CEX}	—	—	0.5	mAdc
Collector Cutoff Current ($V_{CB} = 375 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	—	0.1	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	0.1	mAdc

ON CHARACTERISTICS (1)

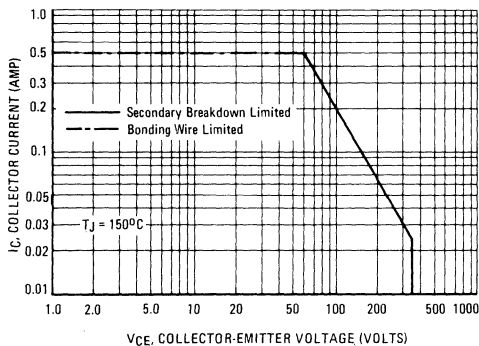
DC Current Gain ($I_C = 50 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$)	MJE2360T	h_{FE}	25	—	200	—
	MJE2361T		50	—	250	
($I_C = 100 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$)	MJE2360T		15	—	—	
	MJE2361T		40	—	—	
Collector-Emitter Saturation Voltage ($I_C = 100 \text{ mAdc}$, $I_B = 10 \text{ mAdc}$)	$V_{CE(sat)}$	—	—	1.5	Vdc	
Base-Emitter On Voltage ($I_C = 100 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$)	$V_{BE(on)}$	—	—	1.0	Vdc	

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 50 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	f_T	—	10	—	MHz
Output Capacitance ($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$, $f = 100 \text{ kHz}$)	C_{ob}	—	20	—	pF

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 2 — DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C - V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

NPN MJE2801, MJE2801T PNP MJE2901

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

... for use as an output device in complementary audio amplifiers up to 35-Watts music power per channel.

- High DC Current Gain — $h_{FE} = 25-100 @ I_C = 3.0 \text{ A}$
- Choice of Packages — MJE2801, 2901 — TO-225AB
MJE2801T — TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	5.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ MJE2801, 2901 MJE2801T	P_{DT}	90 75	Watts
Derate above 25°C MJE2801, 2901 MJE2801T		0.72 0.6	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case MJE2801, 2901 MJE2801T	θ_{JC}	1.39 1.67	$^\circ\text{C}/\text{W}$

† Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage (1) ($I_C = 200 \text{ mAdc}, I_B = 0$)	$V_{(BR)CEO}$	60	—	Vdc
Collector-Cutoff Current ($V_{CB} = 60 \text{ Vdc}, I_E = 0$) ($V_{CB} = 60 \text{ Vdc}, I_E = 0, T_C = 150^\circ\text{C}$)	I_{CBO}	—	0.1 2.0	mAdc
Emitter Cutoff Current ($V_{BE} = 4.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	1.0	mAdc

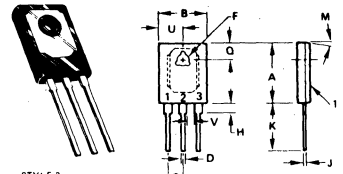
ON CHARACTERISTICS

DC Current Gain ($I_C = 3.0 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$)	h_{FE}	25	100	—
Base-Emitter Voltage ($I_C = 3.0 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$)	V_{BE}	—	1.4	Vdc

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60 VOLTS
75, 90 WATTS

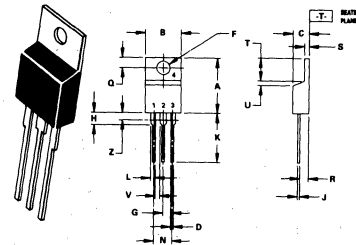


STYLE 2
PIN 1 EMITTER
2 COLLECTOR
3 BASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22	BSC	0.166	BSC
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	90 TYP		90 TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	—	0.080	—

MJE2801
MJE2901

CASE 90-05
TO-225AB



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.60	10.76	0.380	0.420
C	4.07	4.82	0.160	0.190
D	3.68	3.98	0.145	0.155
E	3.41	3.73	0.134	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.03	0.110	0.119
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.10	1.36	0.040	0.054
M	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.75	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
V	0.20	1.27	0.008	0.050
W	1.15	—	0.045	—
Z	—	2.04	—	0.080

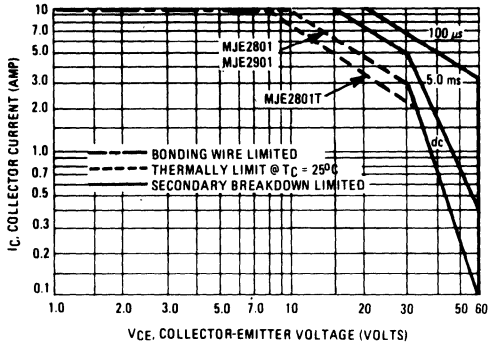
STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MJE2801/MJE2801T NPN, MJE2901 PNP

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150^\circ\text{C}$. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – DC CURRENT GAIN

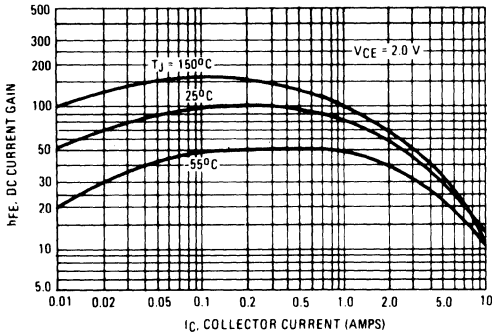


FIGURE 3 – POWER DERATING

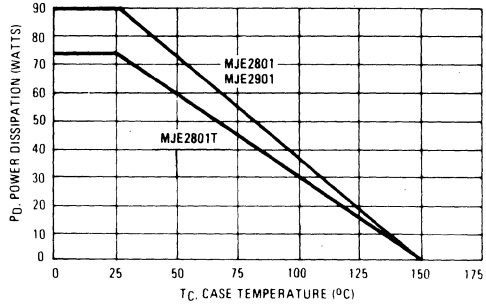
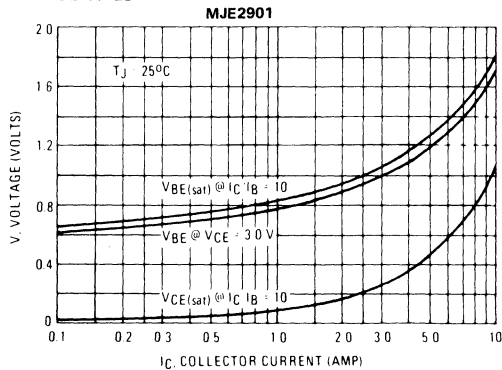
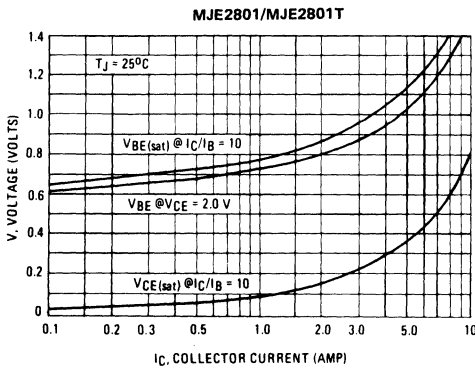


FIGURE 4 – "ON" VOLTAGES



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP
MJE2955, MJE2955T
NPN
MJE3055, MJE3055T

COMPLEMENTARY SILICON PLASTIC
POWER TRANSISTORS

... designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 10 Amperes
- High Current Gain – Bandwidth Product –
 $f_T = 2.0 \text{ MHz (Min) @ } I_C = 500 \text{ mAdc}$
- Choice of Packages – MJE3055, MJE2955 – TO-225AB (TO-127)
MJE3055T, MJE2955T – TO-220AB

MAXIMUM RATINGS

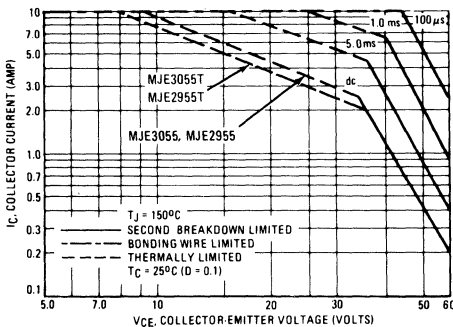
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	70	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	10	Aadc
Base Current	I_B	6.0	Aadc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DT}		Watts
MJE3055, MJE2955		90	W/ $^\circ\text{C}$
MJE3055T, MJE2955T		75	W/ $^\circ\text{C}$
Derate above 25°C			
MJE3055, MJE2955		0.72	W/ $^\circ\text{C}$
MJE3055T, MJE2955T		0.6	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	$^\circ\text{C/W}$
MJE3055, MJE2955		1.39	
MJE3055T, MJE2955T		1.67	

† Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



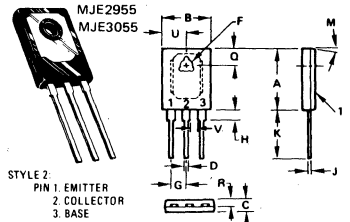
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C , V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{j(pk)} = 150^\circ\text{C}$. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{j(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown (See AN 415A).

10 AMPERE

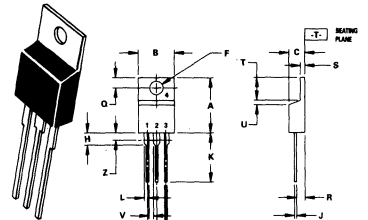
COMPLEMENTARY SILICON
POWER TRANSISTORS

60 VOLTS
75, 90 WATTS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22	BSC	0.166	BSC
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	90 TYP		30 TYP	
N	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	-	0.080	-

CASE 90-05
TO-225AB



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.48	15.75	0.650	0.620
B	6.96	15.08	0.270	0.595
C	4.07	4.82	0.160	0.190
D	0.54	0.68	0.021	0.027
F	3.81	3.73	0.150	0.147
G	7.42	7.86	0.292	0.310
H	0.90	0.93	0.035	0.037
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.38	0.045	0.055
M	4.83	5.33	0.190	0.210
N	2.54	3.04	0.100	0.120
R	2.04	2.78	0.080	0.110
S	1.15	1.38	0.045	0.055
T	5.87	6.41	0.231	0.252
U	6.90	1.77	0.270	0.070
V	1.15	-	0.045	-
Z	-	2.04	-	0.080

STYLE 1:
PIN 1: BASE
PIN 2: EMITTER
PIN 4: COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MJE2955, MJE2955T, PNP, MJE3055, MJE3055T, NPN

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 200 mA _{dc} , I _B = 0)	V _{CEO(sus)}	60	—	V _{dc}
Collector Cutoff Current (V _{CE} = 30 V _{dc} , I _B = 0)	I _{CEO}	—	700	μA _{dc}
Collector Cutoff Current (V _{CE} = 70 V _{dc} , V _{EB(off)} = 1.5 V _{dc}) (V _{CE} = 70 V _{dc} , V _{EB(off)} = 1.5 V _{dc} , T _C = 150°C)	I _{CEX}	—	1.0 5.0	mA _{dc}
Collector Cutoff Current (V _{CB} = 70 V _{dc} , I _E = 0) (V _{CB} = 70 V _{dc} , I _E = 0, T _C = 150°C)	I _{CBO}	—	1.0 10	mA _{dc}
Emitter Cutoff Current (V _{BE} = 5.0 V _{dc} , I _C = 0)	I _{EBO}	—	5.0	mA _{dc}
ON CHARACTERISTICS				
DC Current Gain (1) (I _C = 4.0 A _{dc} , V _{CE} = 4.0 V _{dc}) (I _C = 10 A _{dc} , V _{CE} = 4.0 V _{dc})	h _{FE}	20 5.0	100 —	—
Collector-Emitter Saturation Voltage (1) (I _C = 4.0 A _{dc} , I _B = 0.4 A _{dc}) (I _C = 10 A _{dc} , I _B = 3.3 A _{dc})	V _{CE(sat)}	—	1.1 8.0	V _{dc}
Base-Emitter On Voltage (1) (I _C = 4.0 A _{dc} , V _{CE} = 4.0 V _{dc})	V _{BE(on)}	—	1.8	V _{dc}
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I _C = 500 mA _{dc} , V _{CE} = 10 V _{dc} , f = 500 kHz)	f _T	2.0	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

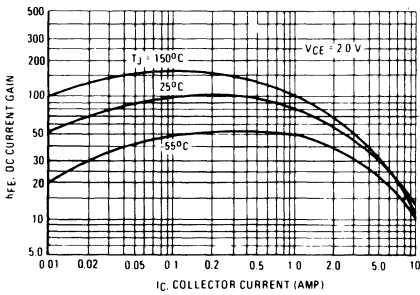
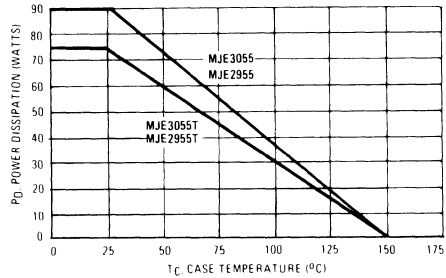
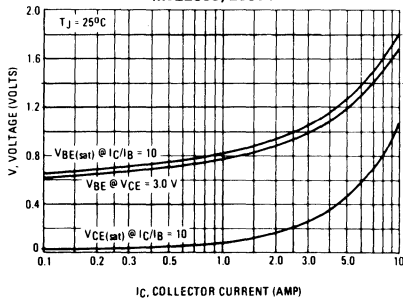


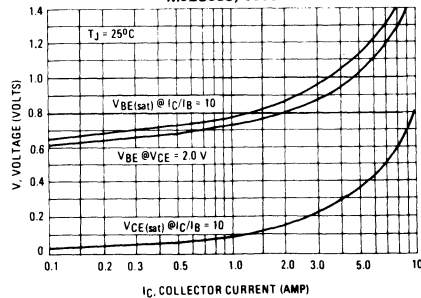
FIGURE 3 – POWER DERATING



MJE2955, 2955T FIGURE 4 – "ON" VOLTAGES



MJE3055, 3055T



NPN
MJE3300, MJE3301
PNP
MJE3310

PLASTIC DARLINGTON COMPLEMENTARY SILICON ANNULAR POWER TRANSISTORS

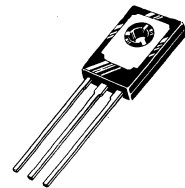
... designed for general-purpose amplifier and high-speed switching applications.

- High DC Current Gain – $h_{FE} = 2000$ (Typ) @ $I_C = 1.0$ Adc
- Collector-Emitter Sustaining Voltage – @ 10 mAdc
 $V_{CE(sus)} = 40$ Vdc (Min) – MJE3310/MJE3300
 $= 60$ Vdc (Min) – MJE3301
- Reverse Voltage Protection Diode
- Pinout Compatible with TO-220 Package
- Monolithic Construction with Built-In Base-Emitter Output Resistor
- Thermopad II Construction With Hard Solder for High Reliability

DARLINGTON
4-AMPERE

COMPLEMENTARY SILICON
POWER TRANSISTORS

40, 60 VOLTS
15 WATTS



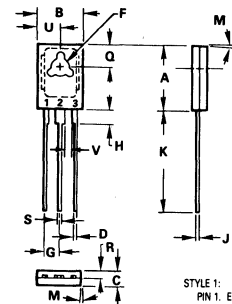
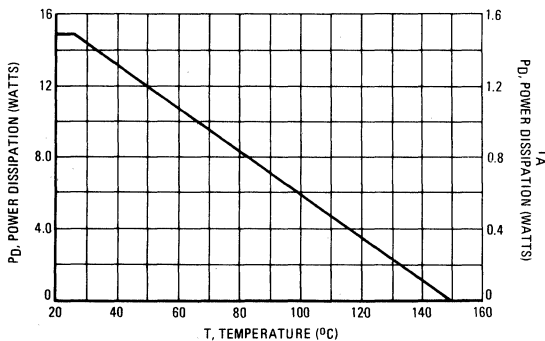
MAXIMUM RATINGS

Rating	Symbol	MJE3310 MJE3300	MJE3301	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Base Voltage	V_{CB}	40	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	4.0		Adc
Peak		6.0		
Base Current	I_B	100		mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	15		Watts
Derate above 25°C		0.12		$\text{W}/^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.5		Watts
Derate above 25°C		0.012		$\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83.3	$^\circ\text{C}/\text{W}$

FIGURE 1 – POWER DERATING



STYLE 1:
PIN 1: EMITTER
PIN 2: COLLECTOR
PIN 3: BASE

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	15.63	0.575	0.615
M	3" TYP		3" TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.89	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

MJE3300, MJE3301 NPN

MJE3310 PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ⁽¹⁾ (I _C = 10 mAdc, I _B = 0)	V _{CEO(sus)}	40 60 —	— —	Vdc
Collector-Cutoff Current (V _{CE} = 20 Vdc, I _B = 0) (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 40 Vdc, I _B = 0)	I _{CEO}	— — —	100 100 —	μAdc
Collector Cutoff Current (V _{CB} = Rated V _{CEO(sus)} , I _E = 0) (V _{CB} = Rated V _{CEO(sus)} , I _E = 0, T _C = 100°C)	I _{CBO}	— —	1.0 100	μAdc
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	—	1.0	μAdc
ON CHARACTERISTICS				
DC Current Gain (I _C = 1.0 Adc, V _{CE} = 2.0 Vdc) (I _C = 1.5 Adc, V _{CE} = 2.0 Vdc)	h _{FE}	1000 750	— —	—
Collector-Emitter Saturation Voltage (I _C = 1.5 Adc, I _B = 6.0 mAdc)	V _{CE(sat)}	—	1.5	Vdc
Base-Emitter Saturation Voltage (I _C = 1.5 Adc, I _B = 6.0 mAdc)	V _{BE(sat)}	—	2.5	Vdc
Base-Emitter On Voltage (I _C = 1.5 Adc, V _{CE} = 2.0 Vdc)	V _{BE(on)}	—	2.5	Vdc
Output Diode Voltage Drop (I _{EC} = 2.0 Adc)	V _{EC}	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I _C = 1.0 Adc, V _{CE} = 2.0 Vdc)	f _T	20	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA

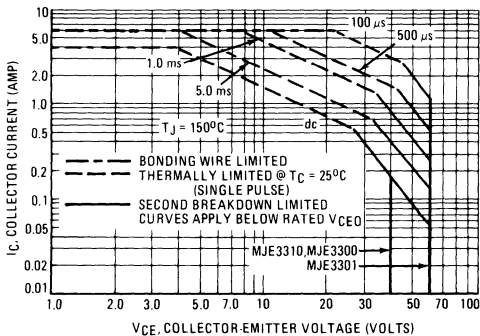


FIGURE 3 – TYPICAL DC CURRENT GAIN

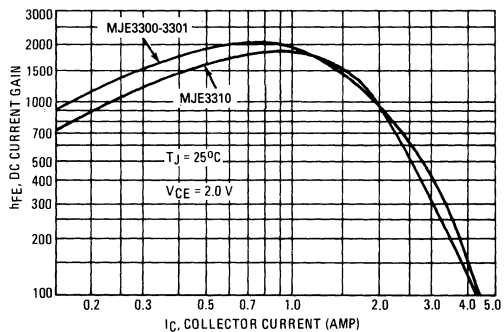
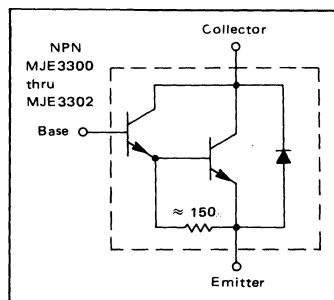
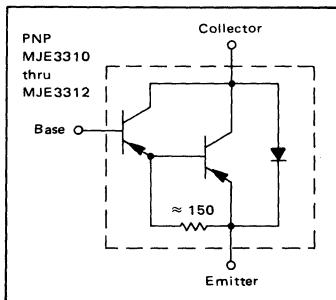


FIGURE 4 – DARLINGTON CIRCUIT SCHEMATIC



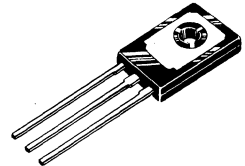
NPN SILICON HIGH-VOLTAGE POWER TRANSISTORS

... designed for use in line-operated equipment requiring high f_T .

- High DC Current Gain –
 $h_{FE} = 40-160 @ I_C = 20 \text{ mAdc}$
- Current-Gain-Bandwidth Product –
 $f_T = 15 \text{ MHz (Min) @ } I_C = 10 \text{ mAdc}$
- Low Output Capacitance –
 $C_{ob} = 10 \text{ pF (Max) @ } f = 1.0 \text{ MHz}$

0.3 AMPERE
POWER TRANSISTORS
NPN SILICON

250-350 VOLTS
15 WATTS



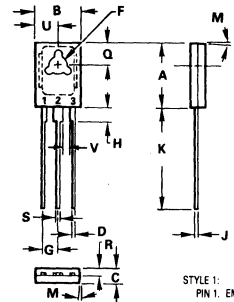
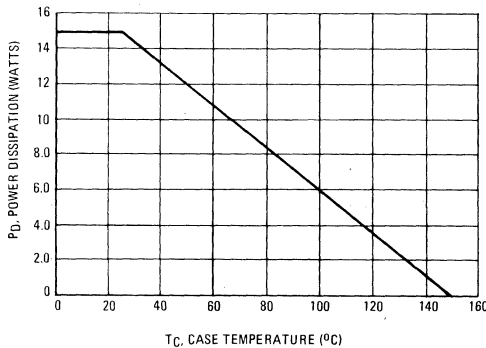
MAXIMUM RATINGS

Rating	Symbol	MJE3439	MJE3440	Unit
Collector-Emitter Voltage	V_{CEO}	350	250	Vdc
Collector-Base Voltage	V_{CB}	450	350	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →		Vdc
Collector Current – Continuous	I_C	← 0.3 →		Adc
Base Current	I_B	← 150 →		mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 15 →		Watts
		← 0.12 →		W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.33	$^\circ\text{C/W}$

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



NOTES:
 1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3 rd TYP		3 rd TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.89	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

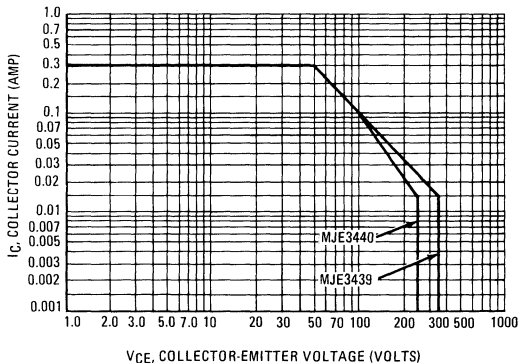
MJE3439, MJE3440

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I _C = 5.0 mA _{dc} , I _B = 0) (I _C = 50 mA _{dc} , I _B = 0)	MJE3439 MJE3440	V _{CEO(sus)}	350 250	V _{dc}
Collector Cutoff Current (V _{CE} = 300 V _{dc} , I _B = 0) (V _{CE} = 200 V _{dc} , I _B = 0)	MJE3439 MJE3440	I _{CEO}	– 20 50	μA _{dc}
Collector Cutoff Current (V _{CE} = 450 V _{dc} , V _{EB(off)} = 1.5 V _{dc}) (V _{CE} = 300 V _{dc} , V _{EB(off)} = 1.5 V _{dc})	MJE3439 MJE3440	I _{CEX}	– 500 500	μA _{dc}
Collector Cutoff Current (V _{CB} = 350 V _{dc} , I _E = 0) (V _{CB} = 250 V _{dc} , I _E = 0)	MJE3439 MJE3440	I _{CBO}	– 20 20	μA _{dc}
Emitter Cutoff Current (V _{BE} = 5.0 V _{dc} , I _C = 0)		I _{EBO}	– 20	μA _{dc}
ON CHARACTERISTICS				
DC Current Gain (I _C = 2.0 mA _{dc} , V _{CE} = 10 V _{dc}) (I _C = 20 mA _{dc} , V _{CE} = 10 V _{dc})		h _{FE}	30 50	–
Collector-Emitter Saturation Voltage (I _C = 50 mA _{dc} , I _B = 4.0 mA _{dc})		V _{CE(sat)}	– 0.5	V _{dc}
Base-Emitter Saturation Voltage (I _C = 50 mA _{dc} , I _B = 4.0 mA _{dc})		V _{BE(sat)}	– 1.3	V _{dc}
Base-Emitter On Voltage (I _C = 50 mA _{dc} , V _{CE} = 10 V _{dc})		V _{BE(on)}	– 0.8	V _{dc}
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I _C = 10 mA _{dc} , V _{CE} = 10 V _{dc} , f = 5.0 MHz)		f _T	15	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 1.0 MHz)		C _{ob}	– 10	pF
Small-Signal Current Gain (I _C = 5.0 mA _{dc} , V _{CE} = 10 V _{dc} , f = 1.0 kHz)		h _{fe}	25	–

3

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C-V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
MJE4340	MJE4350
MJE4341	MJE4351
MJE4342	MJE4352
MJE4343	MJE4353

HIGH-VOLTAGE — HIGH POWER TRANSISTORS

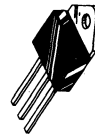
... designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage —

	NPN	PNP
V _{CEO(sus)} = 100 Vdc —	MJE4340	MJE4350
= 120 Vdc —	MJE4341	MJE4351
= 140 Vdc —	MJE4342	MJE4352
= 160 Vdc —	MJE4343	MJE4353
- High DC Current Gain — @ I_C = 8.0 Adc
h_{FE} = 35 (Typ)
- Low Collector-Emitter Saturation Voltage —
V_{CE(sat)} = 2.0 Vdc (Max) @ I_C = 8.0 Adc

16 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON

100-160 VOLTS



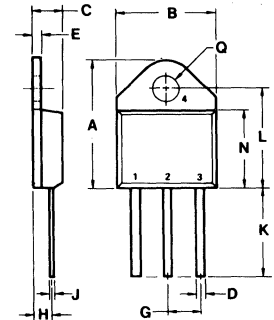
MAXIMUM RATINGS

Rating	Symbol	MJE4340	MJE4341	MJE4342	MJE4343	Unit
		MJE4350	MJE4351	MJE4352	MJE4353	
Collector-Emitter Voltage	V _{CEO}	100	120	140	160	Vdc
Collector-Base Voltage	V _{CB}	100	120	140	160	Vdc
Emitter-Base Voltage	V _{EB}	← 7.0 →				Vdc
Collector Current — Continuous Peak (1)	I _C	← 16 → ← 20 →				Adc
Base Current — Continuous	I _B	← 5.0 →				Adc
Total Device Dissipation @ T _C = 25°C	P _D	← 125 →				Watts
Operating and Storage Junction Temperature Range	T _{J, Tstg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.0	°C/W

(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.



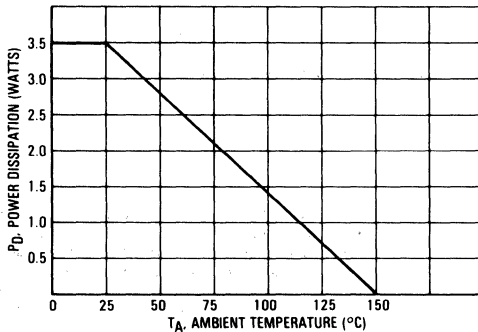
STYLE 1:
 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
 TO-218AC

3

FIGURE 1 — POWER DERATING
 REFERENCE: AMBIENT TEMPERATURE



MJE4340 thru MJE4343NPN, MJE4350 thru MJE4353PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 200\text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	100	—	Vdc
MJE4340, MJE4350		120	—	
MJE4341, MJE4351		140	—	
MJE4342, MJE4352		160	—	
MJE4343, MJE4353		—	—	
Collector-Emitter Cutoff Current ($V_{CE} = 50\text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	750	μAdc
($V_{CE} = 60\text{ Vdc}$, $I_B = 0$)		—	750	
($V_{CE} = 70\text{ Vdc}$, $I_B = 0$)		—	750	
($V_{CE} = 80\text{ Vdc}$, $I_B = 0$)		—	750	
Collector-Emitter Cutoff Current ($V_{CE} = \text{Rated } V_{CB}$, $V_{EB(off)} = 1.5\text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CB}$, $V_{EB(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEX}	—	1.0	mAdc
		—	5.0	
Collector-Base Cutoff Current ($V_{CB} = \text{Rated } V_{CB}$, $I_E = 0$)	I_{CBO}	—	750	μAdc
Emitter-Base Cutoff Current ($V_{BE} = 7.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	1.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 8.0\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$) ($I_C = 16\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	h_{FE}	15	35 (Typ)	—
		8.0	15 (Typ)	
Collector-Emitter Saturation Voltage ($I_C = 8.0\text{ Adc}$, $I_B = 800\text{ mA}$) ($I_C = 16\text{ Adc}$, $I_B = 2.0\text{ Adc}$)	$V_{CE(sat)}$	—	2.0	Vdc
		—	3.5	
Base-Emitter Saturation Voltage ($I_C = 16\text{ Adc}$, $I_B = 2.0\text{ Adc}$)	$V_{BE(sat)}$	—	3.9	Vdc
Base-Emitter On Voltage ($I_C = 16\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	$V_{BE(on)}$	—	3.9	Vdc

DYNAMIC CHARACTERISTICS

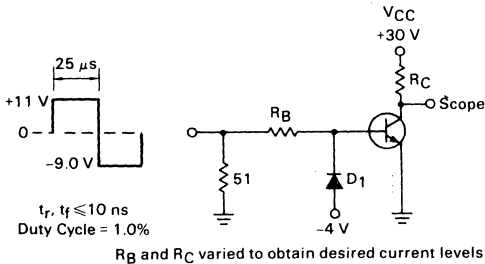
Current-Gain—Bandwidth Product (2) ($I_C = 1.0\text{ Adc}$, $V_{CE} = 20\text{ Vdc}$, $f_{test} = 0.5\text{ MHz}$)	f_T	1.0	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	—	800	pF

(1) Pulse Test: Pulse Width $\leq 30\mu\text{ s}$, Duty Cycle $\geq 2.0\%$.

(2) $f_T = |h_{fe}| \bullet f_{test}$

3

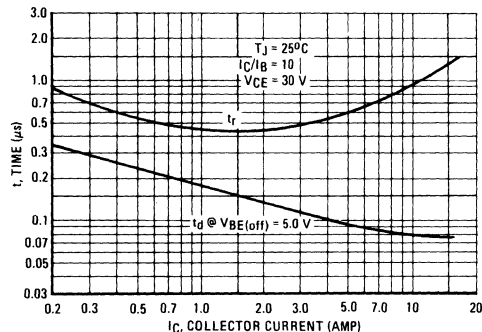
FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



D_1 must be fast recovery type, eg:
MBD5300 used above $I_B \approx 100\text{ mA}$
MSD6100 used below $I_B \approx 100\text{ mA}$

Note: Reverse polarities to test PNP devices.

FIGURE 3 — TYPICAL TURN-ON TIME



TYPICAL CHARACTERISTICS

FIGURE 4 — TURN-OFF TIME

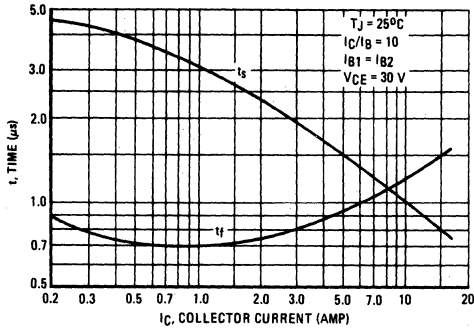
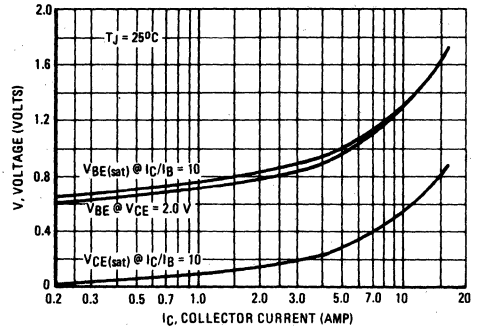


FIGURE 5 — ON VOLTAGES



DC CURRENT GAIN

FIGURE 6 — MJE4340 SERIES (NPN)

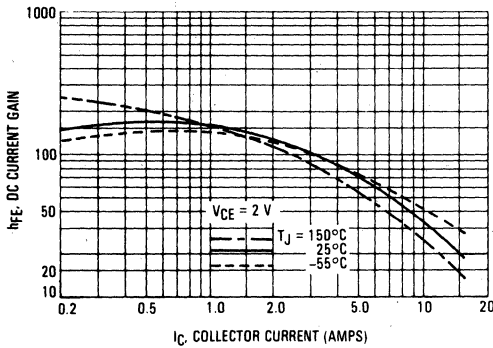


FIGURE 7 — MJE4350 SERIES (PNP)

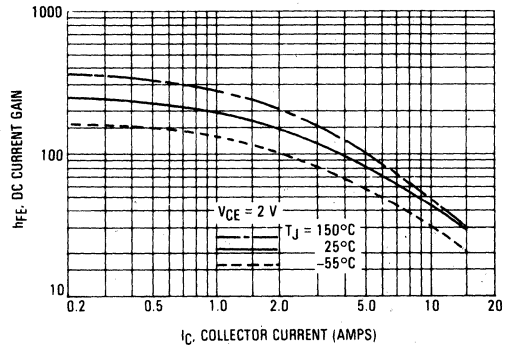
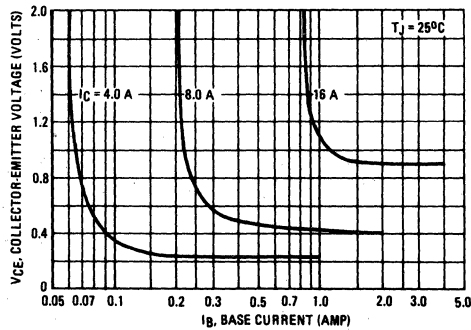


FIGURE 8 — COLLECTOR SATURATION REGION



MJE4340 thru MJE4343NPN, MJE4350 thru MJE4353PNP

FIGURE 9 — THERMAL RESPONSE

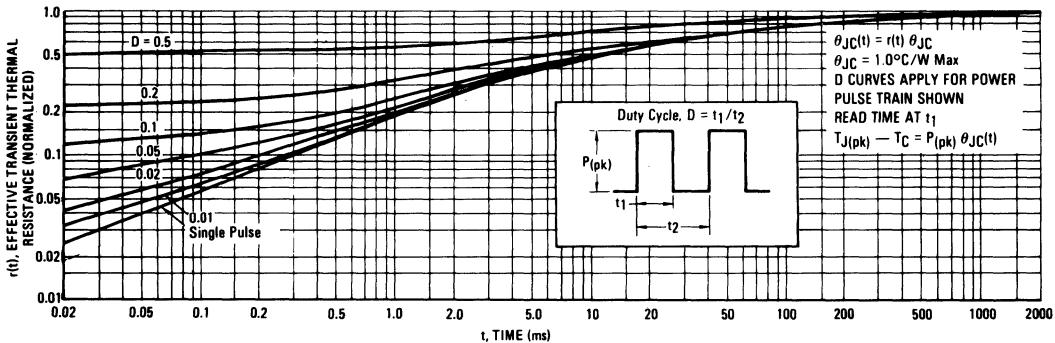
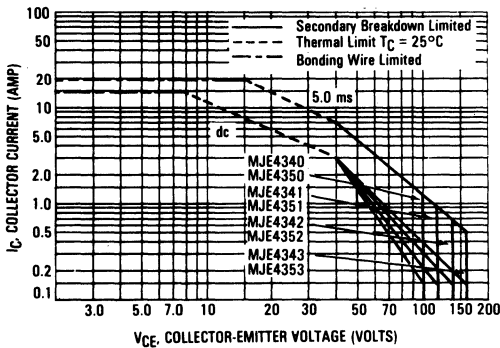


FIGURE 10 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



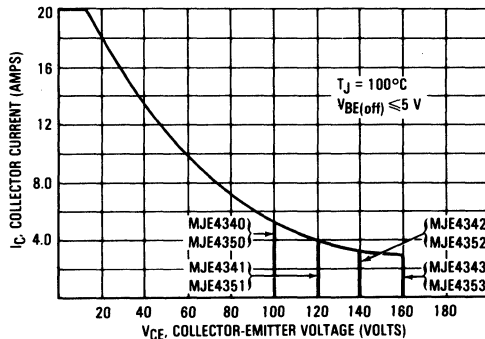
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^{\circ}\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^{\circ}\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 11 gives RBSOA characteristics.

FIGURE 11 — MAXIMUM REVERSE BIAS SAFE OPERATING AREA



NPN Silicon Power Darlington Transistors

The MJE5740, 41, 42 Darlington transistors are designed for high-voltage power switching in inductive circuits. They are particularly suited for operation in applications such as:

- Small Engine Ignition
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

MJE5740
MJE5741
MJE5742

**POWER DARLINGTON
TRANSISTORS**
8 AMPERES
300, 350, 400 VOLTS
80 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJE5740	MJE5741	MJE5742	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	800	Vdc
Emitter Base Voltage	V_{EB}	8			Vdc
Collector Current — Continuous	I_C	8			Adc
— Peak (1)	I_{CM}	16			
Base Current — Continuous	I_B	2.5			Adc
— Peak (1)	I_{BM}	5			
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2			Watts
		16			mW/°C
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	80			Watts
		640			mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle = 10%.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS (2)

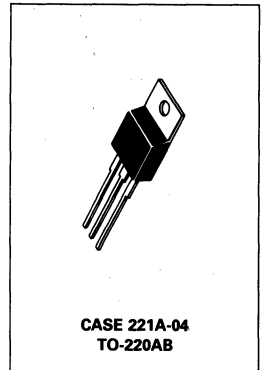
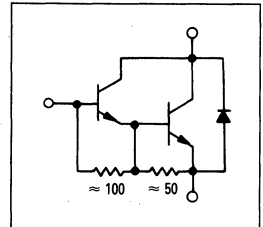
Collector-Emitter Sustaining Voltage ($I_C = 50\text{ mA}, I_B = 0$)	MJE5740 MJE5741 MJE5742	$V_{CEO(sus)}$	300 350 400	— — —	— — —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}, V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}, V_{BE(off)} = 1.5\text{ Vdc}, T_C = 100^\circ\text{C}$)		I_{CEV}	— —	— —	1 5	mAdc
Emitter Cutoff Current ($V_{EB} = 8\text{ Vdc}, I_C = 0$)		I_{EBO}	—	—	75	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 6
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 7

(2) Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

(continued)



MJE5740, MJE5741, MJE5742

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 0.5 \text{ Adc}, V_{CE} = 5 \text{ Vdc}$) ($I_C = 4 \text{ Adc}, V_{CE} = 5 \text{ Vdc}$)	hFE	50 200	100 400	— —	—
Collector-Emitter Saturation Voltage ($I_C = 4 \text{ Adc}, I_B = 0.2 \text{ Adc}$) ($I_C = 8 \text{ Adc}, I_B = 0.4 \text{ Adc}$) ($I_C = 4 \text{ Adc}, I_B = 0.2 \text{ Adc}, T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2 3 2.2	Vdc
Base-Emitter Saturation Voltage ($I_C = 4 \text{ Adc}, I_B = 0.2 \text{ Adc}$) ($I_C = 8 \text{ Adc}, I_B = 0.4 \text{ Adc}$) ($I_C = 4 \text{ Adc}, I_B = 0.2 \text{ Adc}, T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— — —	— — —	2.5 3.5 2.4	Vdc
Diode Forward Voltage (2) ($I_F = 5 \text{ Adc}$)	V_f	—	—	2.5	Vdc

SWITCHING CHARACTERISTICS

Typical Resistive Load (Table 1)						
Delay Time	$V_{CC} = 250 \text{ Vdc}, I_{C(pk)} = 6 \text{ A}$ $I_{B1} = I_{B2} = 0.25 \text{ A}, t_p = 25 \mu\text{s}$, Duty Cycle $\leq 1\%$	t_d	—	0.04	—	μs
Rise Time		t_r	—	0.5	—	μs
Storage Time		t_s	—	8	—	μs
Fall Time		t_f	—	2	—	μs
Inductive Load, Clamped (Table 1)						
Voltage Storage Time	$I_{C(pk)} = 6 \text{ A}, V_{CE(pk)} = 250 \text{ Vdc}$ $I_{B1} = 0.06 \text{ A}, V_{BE(off)} = 5 \text{ Vdc}$	t_{sv}	—	4	—	μs
Crossover Time		t_c	—	2	—	μs

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

(2) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

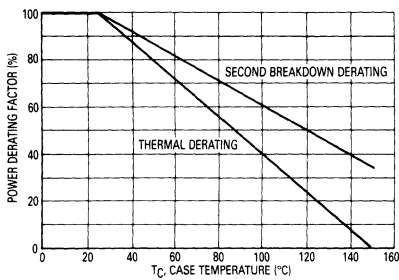


Figure 1. Power Derating

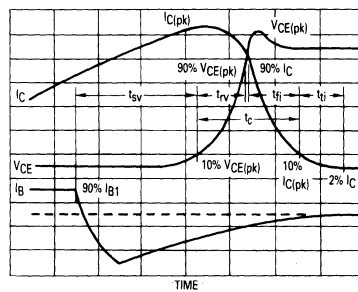


Figure 2. Inductive Switching Measurements

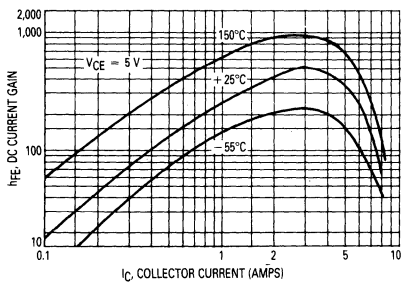


Figure 3. DC Current Gain

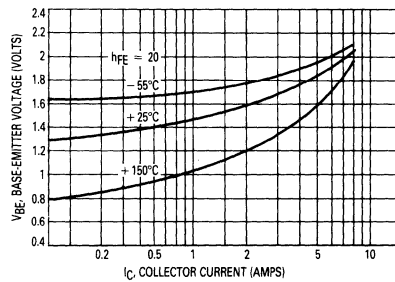


Figure 4. Base-Emitter Voltage

Table 1. Test Conditions for Dynamic Performance

Reverse Bias Safe Operating Area and Inductive Switching		Resistive Switching
<p>Test Circuits</p> <p>DUTY CYCLE $\leq 10\%$ $t_r, t_f \leq 10$ ns</p> <p>NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}</p>	<p>Circuit Values</p> <p>COIL DATA: FERROXCUBE CORE #6656 FULL BOBBIN (~16 TURNS) #16</p> <p>GAP FOR 200 μH/20 A $L_{coil} = 200 \mu$H</p> <p>$V_{CC} = 30$ V $V_{CE(pk)} = 250$ Vdc $I_{C(pk)} = 6$ A</p>	<p>Test Waveforms</p> <p>Output Waveforms</p> <p>t_1 ADJUSTED TO OBTAIN I_C</p> $t_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$ <p>TEST EQUIPMENT SCOPE — TEKTRONIX 475 OR EQUIVALENT</p>
		<p>Resistive Switching</p> <p>$V_{CC} = 250$ V D1 = 1N5820 OR EQUIV.</p>
		<p>Test Waveforms</p> <p>$t_r, t_f < 10$ ns DUTY CYCLE = 1% R_B AND R_C ADJUSTED FOR DESIRED I_B AND I_C</p>

3

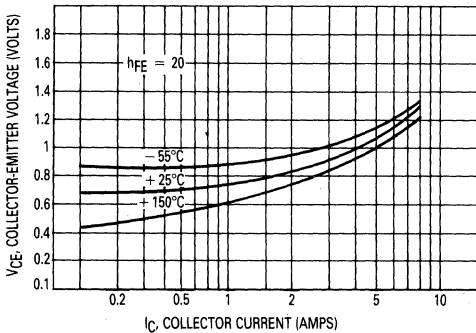
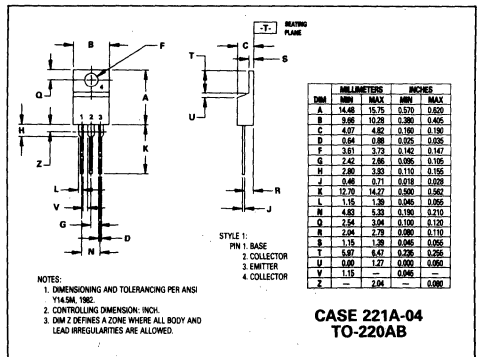


Figure 5. Collector Saturation Voltage

OUTLINE DIMENSIONS



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 1.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives the complete RBSOA characteristics.

The Safe Operating Area figures shown in Figures 6 and 7 are specified ratings for these devices under the test conditions shown.

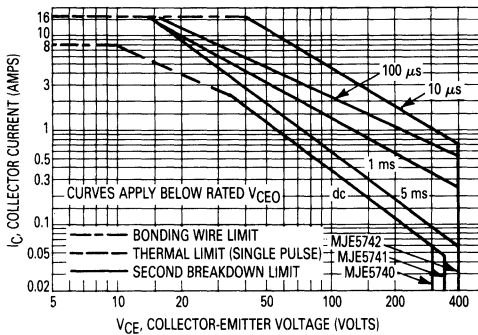


Figure 6. Forward Bias Safe Operating Area

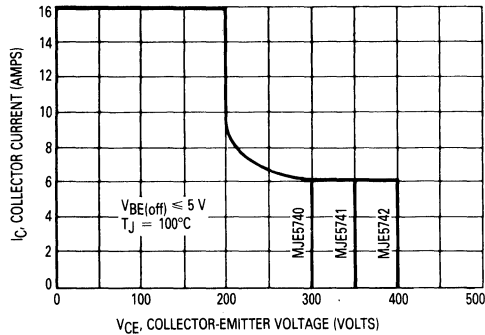


Figure 7. Reverse Bias Safe Operating Area

RESISTIVE SWITCHING PERFORMANCE

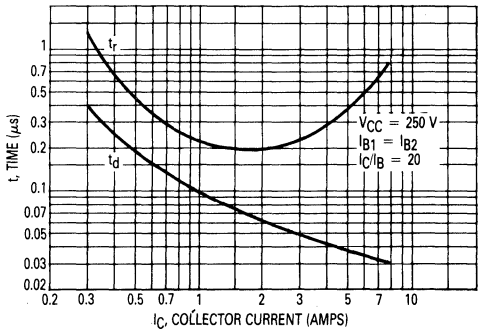


Figure 8. Turn-On Time

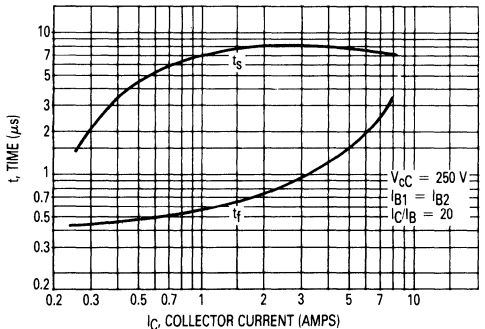


Figure 9. Turn-Off Time

MJE5850
MJE5851
MJE5852

Designers Data Sheet

SWITCHMODE SERIES
PNP SILICON POWER TRANSISTORS

The MJE5850, MJE5851 and the MJE5852 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

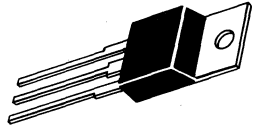
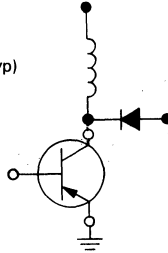
Fast Turn-Off Times

100 ns Inductive Fall Time @ 25°C (Typ)
 125 ns Inductive Crossover Time @ 25°C (Typ)

Operating Temperature Range -65 to +150°C

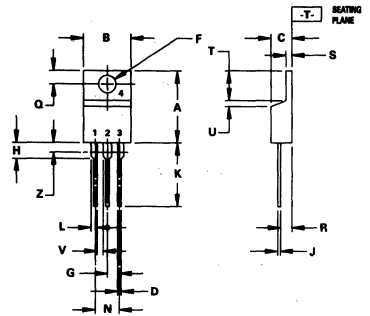
100°C Performance Specified for:

- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.26	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.86	0.095	0.115
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
O	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MJE 5850	MJE 5851	MJE 5852	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	300	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	350	400	450	Vdc
Emitter Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous	I_C	8.0			Adc
Peak (1)	I_{CM}	16			
Base Current — Continuous	I_B	4.0			Adc
Peak (1)	I_{BM}	8.0			
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	80			Watts
Derate above 25°C		0.640			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to 150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

MJE5850, MJE5851, MJE5852

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (I _C = 10 mA, I _B = 0)	MJE5850 MJE5851 MJE5852	V _{CEO(sus)}	300 350 400	— — —	Vdc	
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)		I _{CEV}	— —	— —	0.5 2.5	mAdc
Collector Cutoff Current (V _{CE} = Rated V _{CEV} , R _{BE} = 50 Ω, T _C = 100°C)		I _{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V _{EB} = 6.0 Vdc, I _C = 0)		I _{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased Clamped Inductive SOA with base reverse biased	I _{S/b} RBSOA	See Figure 12 See Figure 13
---	---------------------------	--------------------------------

*ON CHARACTERISTICS

DC Current Gain (I _C = 2.0 Adc, V _{CE} = 5 Vdc) (I _C = 5.0 Adc, V _{CE} = 5 Vdc)	h _{FE}	15 5	— —	— —	—
Collector-Emitter Saturation Voltage (I _C = 4.0 Adc, I _B = 1.0 Adc) (I _C = 8.0 Adc, I _B = 3.0 Adc) (I _C = 4.0 Adc, I _B = 1.0 Adc, T _C = 100°C)	V _{CE(sat)}	— — —	— — —	— 2.0 5.0 2.5	Vdc
Base-Emitter Saturation Voltage (I _C = 4.0 Adc, I _B = 1.0 Adc) (I _C = 4.0 Adc, I _B = 1.0 Adc, T _C = 100°C)	V _{BE(sat)}	— —	— —	— 1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1.0 kHz)	C _{ob}	—	270	—	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 250 Vdc, I _C = 4.0 A, I _{B1} = 1.0 A,	t _d	—	0.025	0.1	μs
Rise Time	t _p = 50 μs, Duty Cycle ≤ 2%)	t _r	—	0.100	0.5	μs
Storage Time	(V _{CC} = 250 Vdc, I _C = 4.0 A, I _{B1} = 1.0 A,	t _s	—	0.60	2.0	μs
Fall Time	V _{BE(off)} = 5 Vdc, t _p = 50 μs, Duty Cycle ≤ 2%)	t _f	—	0.11	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I _{CM} = 4 A, V _{CEM} = 250 V, I _{B1} = 1.0 A,	t _{sv}	—	0.8	3.0	μs
Crossover Time	V _{BE(off)} = 5 Vdc, T _C = 100°C)	t _c	—	0.4	1.5	μs
Fall Time		t _{fi}	—	0.1	—	μs
Storage Time	(I _{CM} = 4 A, V _{CEM} = 250 V, I _{B1} = 1.0 A,	t _{sv}	—	0.5	—	μs
Crossover Time	V _{BE(off)} = 5 Vdc, T _C = 25°C)	t _c	—	0.125	—	μs
Fall Time		t _{fi}	—	0.1	—	μs

* Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

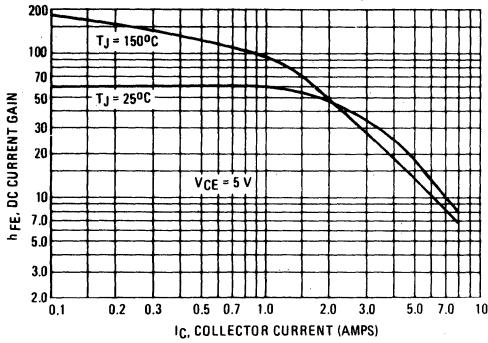


FIGURE 2 – COLLECTOR SATURATION REGION

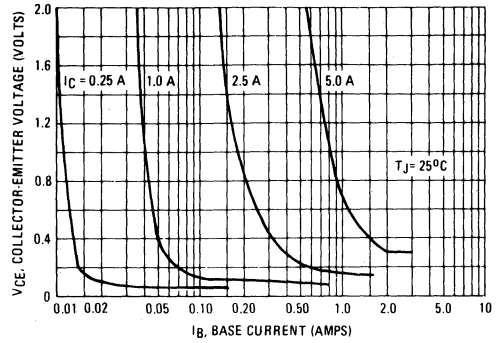


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

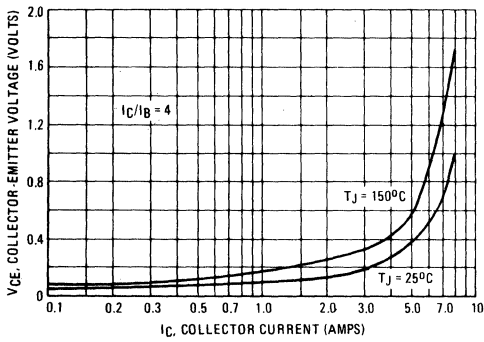


FIGURE 4 – BASE-EMITTER VOLTAGE

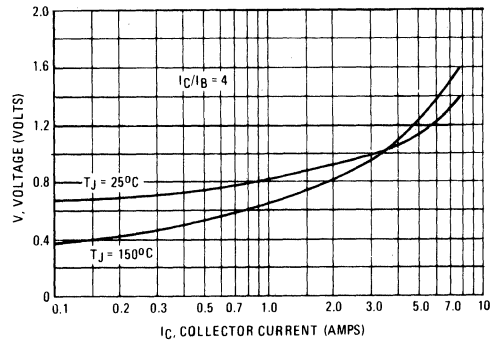


FIGURE 5 – COLLECTOR CUTOFF REGION

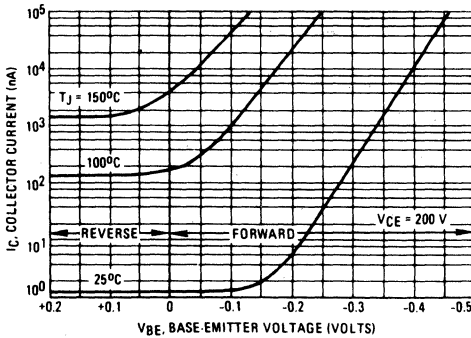
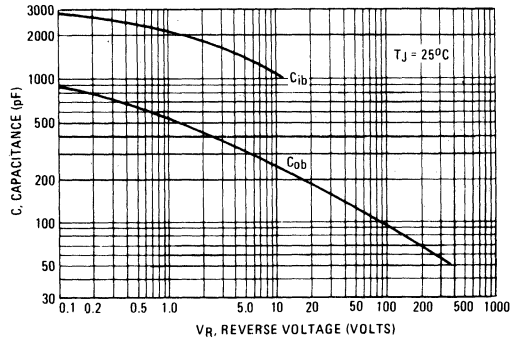


FIGURE 6 – CAPACITANCE



3

TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

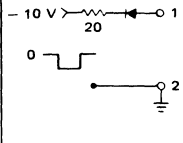
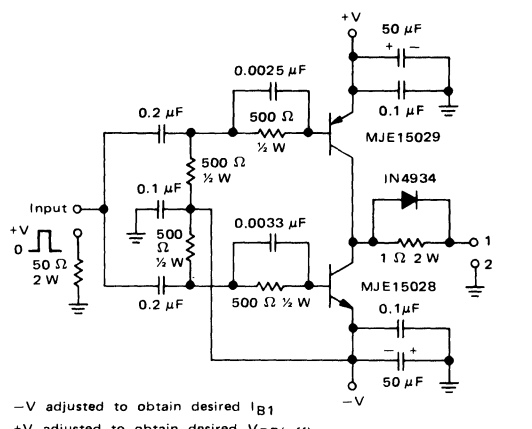
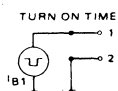
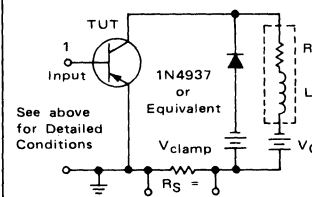
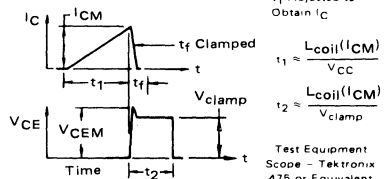
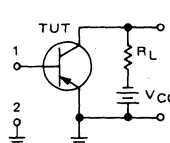
	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
<p>INPUT CONDITIONS</p>  <p>PW Varied to Attain I_C = 100 mA</p>	 <p>-V adjusted to obtain desired I_{B1} +V adjusted to obtain desired V_{BE(off)}</p>	<p>TURN ON TIME</p>  <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit</p>	
<p>CIRCUIT VALUES</p> <p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>V_{clamp} = 250 V R_B adjusted to attain I_{B1}</p>	<p>V_{CC} = 250 V R_L = 62 Ω Pulse Width = 10 μs</p>	
<p>TEST CIRCUITS</p> <p>INDUCTIVE TEST CIRCUIT</p>  <p>See above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 	

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS

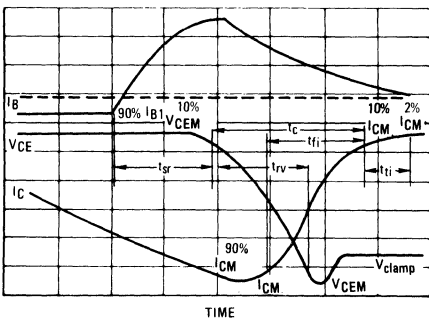
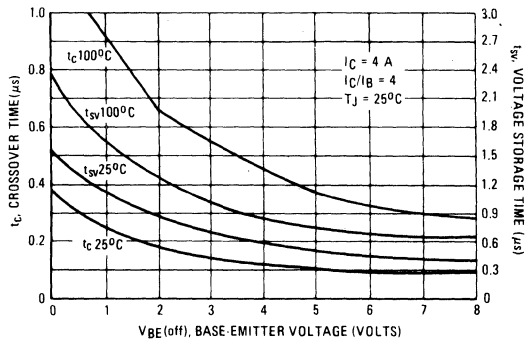


FIGURE 8 - INDUCTIVE SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
 - t_{RV} = Voltage Rise Time, 10–90% V_{CEM}
 - t_{fi} = Current Fall Time, 90–10% I_{CM}
 - t_{ij} = Current Tail, 10–2% I_{CM}
 - t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}
- An enlarged portion of the inductive switching waveform

is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C t_c f$$

In general, $t_{RV} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{SV}) which are guaranteed at 100°C.

FIGURE 9 – TURN-ON SWITCHING TIMES

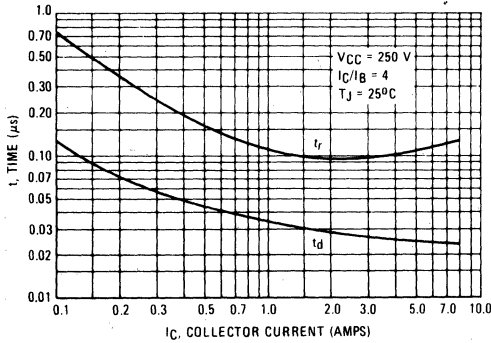


FIGURE 10 – TURN-OFF SWITCHING TIMES

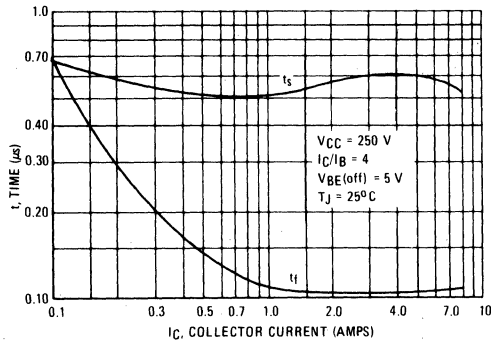
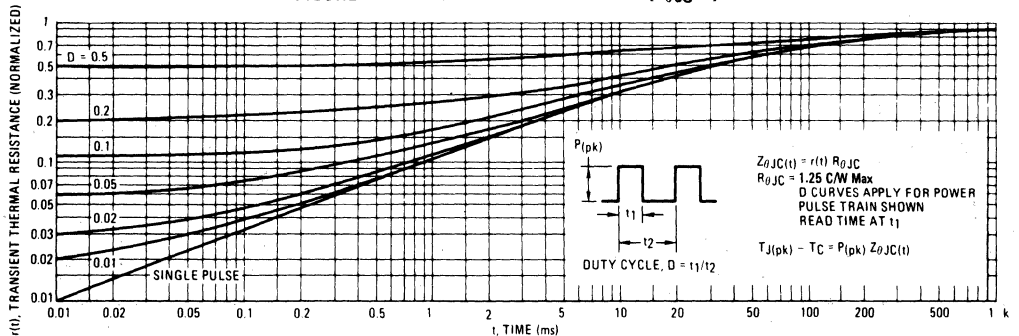


FIGURE 11 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – MAXIMUM FORWARD BIAS SAFE OPERATING AREA

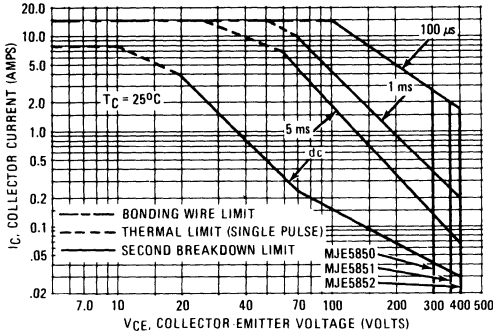


FIGURE 13 – RBSOA, MAXIMUM REVERSE BIAS SAFE OPERATING AREA

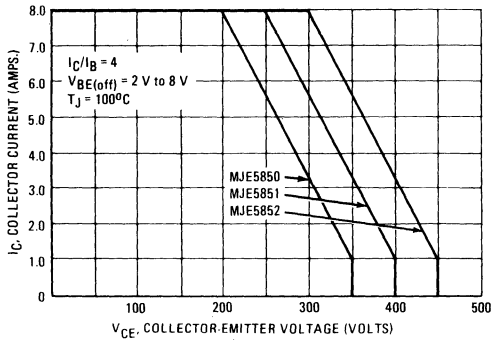
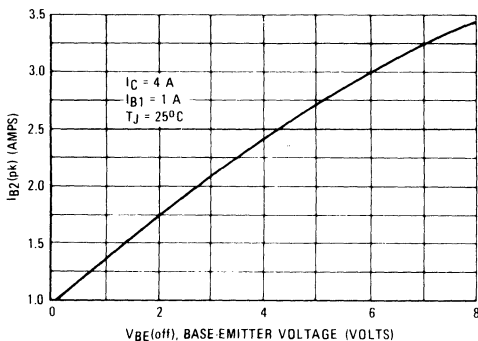


FIGURE 14 PEAK REVERSE BASE CURRENT



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

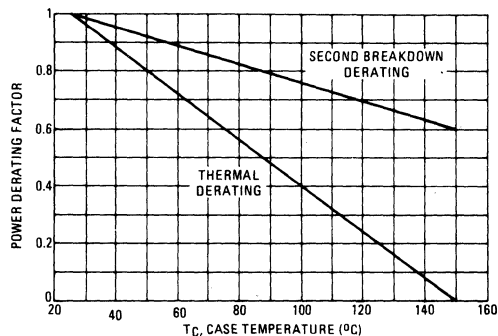
The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_J(\text{pk})$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

FIGURE 15 – FORWARD BIAS POWER DERATING



MJE8500
MJE8501

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE8500 and MJE8501 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

- 300 ns Inductive Fall Time – 25°C (Typ)
- 500 ns Inductive Crossover Time – 25°C (Typ)
- 900 ns Inductive Storage Time – 25°C (Typ)

Operating Temperature Range –65 to +125°C

100°C Performance Specified for:

- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

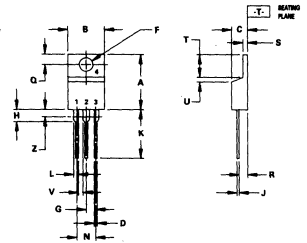
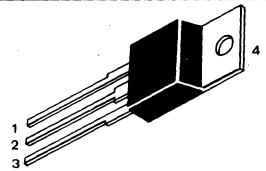
2.5 AMPERE

NPN SILICON
POWER TRANSISTORS

700 and 800 VOLTS
65 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.40	15.75	0.570	0.620
B	3.96	10.20	0.390	0.405
C	4.07	4.62	0.160	0.180
D	0.94	0.98	0.035	0.039
F	3.61	3.73	0.142	0.147
G	2.42	2.65	0.095	0.105
H	2.60	3.03	0.110	0.120
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.20	0.045	0.050
M	4.80	5.20	0.190	0.210
N	3.84	3.96	0.150	0.156
P	2.04	2.70	0.080	0.110
Q	1.15	1.20	0.045	0.050
T	6.67	6.67	0.265	0.265
U	0.90	1.27	0.030	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:
 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	MJE8500	MJE8501	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current – Continuous	I_C	2.5	2.5	Adc
Peak (1)	I_{CM}	5.0	5.0	
Base Current – Continuous	I_B	2.0	2.0	Adc
Peak (1)	I_{BM}	4.0	4.0	
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	65	65	Watts
@ $T_C = 100^\circ C$		17	17	
Derate above 25°C		0.65	0.65	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +125		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.54	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

MJE8500, MJE8501

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	MJE8500 MJE8501	$V_{CEO(sus)}$	700 800	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)		I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)		I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current ($V_{EB} = 7.0\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	7.5	—	—	—	
Collector-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.33\text{ Adc}$) ($I_C = 2.5\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 1.0\text{ Adc}$, $I_B = 0.33\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	— — —	2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.33\text{ Adc}$) ($I_C = 1.0\text{ Adc}$, $I_B = 0.33\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	— —	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	50	—	250	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	$(V_{CC} = 500\text{ Vdc}$, $I_C = 1.0\text{ A}$, $I_{B1} = 0.33\text{ A}$, $V_{BE(off)} = 5.0\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$)	t_d	—	0.045	0.20	μs
Rise Time		t_r	—	0.2	2.0	μs
Storage Time		t_s	—	1.0	4.0	μs
Fall Time		t_f	—	0.5	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	$(I_C = 1.0\text{ A(pk)}$, $V_{clamp} = 500\text{ Vdc}$, $I_{B1} = 0.33\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	—	1.3	4.0	μs
Crossover Time		t_c	—	0.6	2.0	μs
Storage Time	$(I_C = 1.0\text{ A(pk)}$, $V_{clamp} = 500\text{ Vdc}$, $I_{B1} = 0.33\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 25^\circ\text{C}$)	t_{sv}	—	0.9	—	μs
Crossover Time		t_c	—	0.5	—	μs
Fall Time		t_{fi}	—	0.3	—	μs

(1) Pulse Test: PW - 300 μs , Duty Cycle $\leq 2\%$.

FIGURE 1 – DC CURRENT GAIN

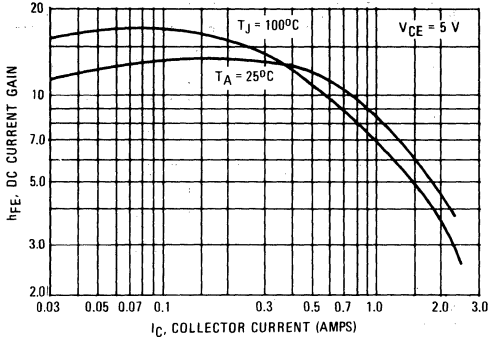


FIGURE 2 – COLLECTOR SATURATION REGION

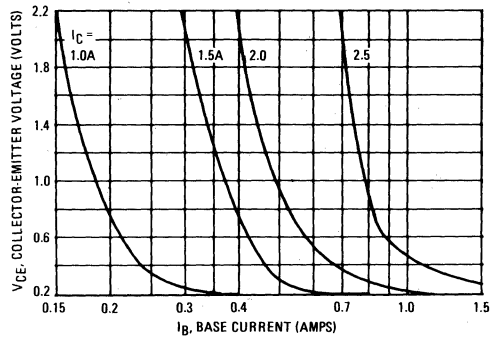


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

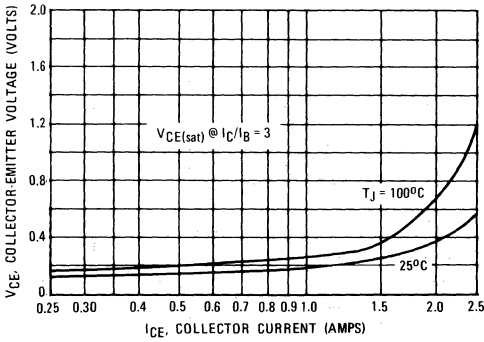


FIGURE 4 – BASE-EMITTER VOLTAGE

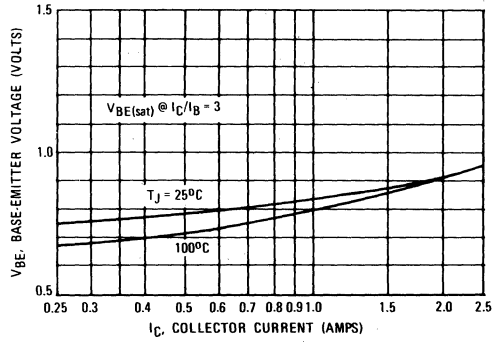


FIGURE 5 – COLLECTOR CUTOFF REGION

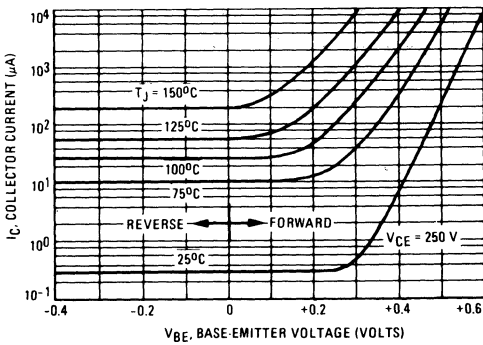


FIGURE 6 – CAPACITANCE

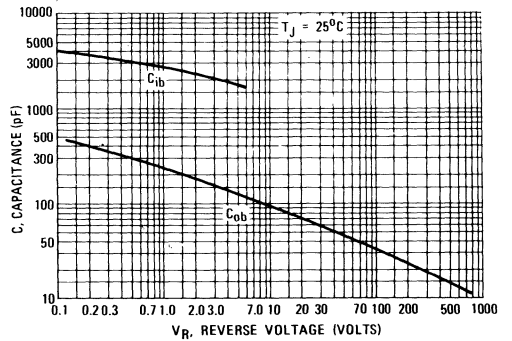


FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

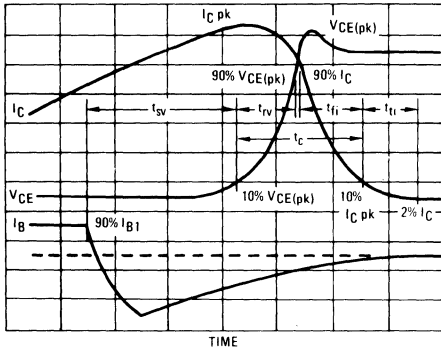
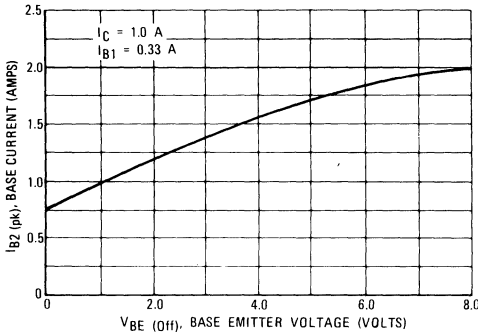


FIGURE 8 – PEAK REVERSE BASE CURRENT



TYPICAL RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN - ON SWITCHING TIMES

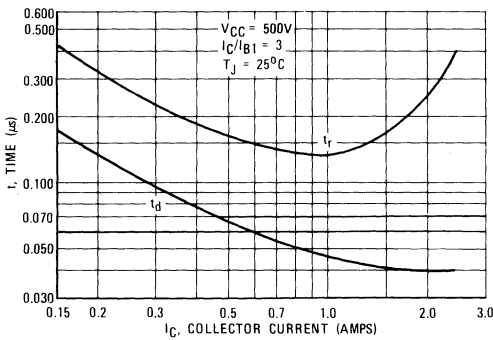
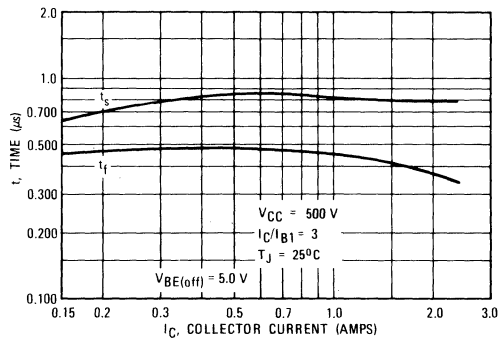


FIGURE 10 – TURN - OFF SWITCHING TIMES



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, $90\% I_{B1}$ to $10\% V_{CE}$ (pk)
- t_{rv} = Voltage Rise Time, $10-90\% V_{CE}$ (pk)
- t_{fi} = Current Fall Time, $90-10\% I_C$
- t_{ti} = Current Tail, $10-2\% I_C$
- t_c = Crossover Time, $10\% V_{CE}$ (pk) to $10\% I_C$

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

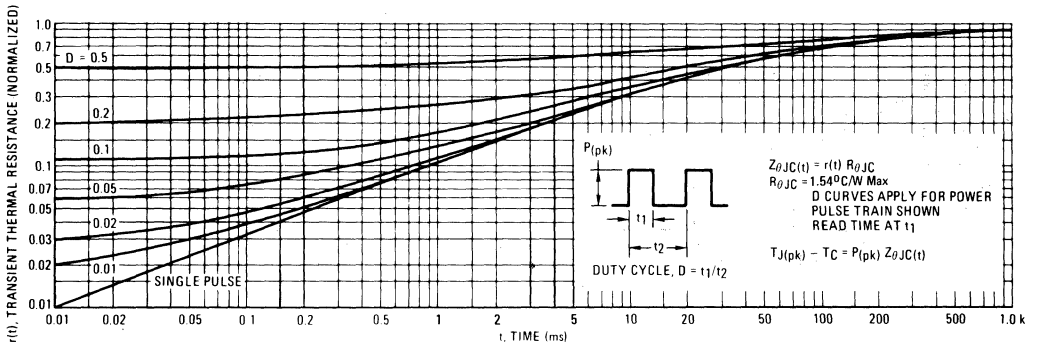
As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C .

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain I_C = 100 mA</p>	<p>All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and R_{BSOA}, R2 = 0 For BV_{CEO(sus)}, R2 = ∞ V_{BE(off)} = 5.0 V</p>	<p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p> <p>V_{clamp} = 500 V</p>	<p>V_{CC} = 500 V R_L = 500 Ω Pulse Width = 10 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p>	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope – Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

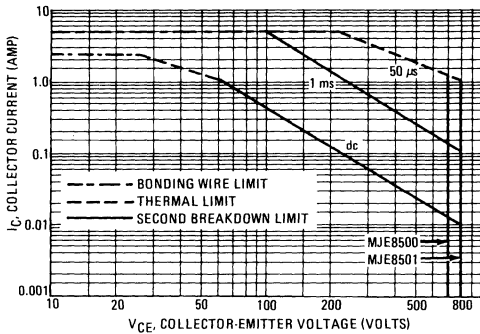
3

FIGURE 11 – THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA



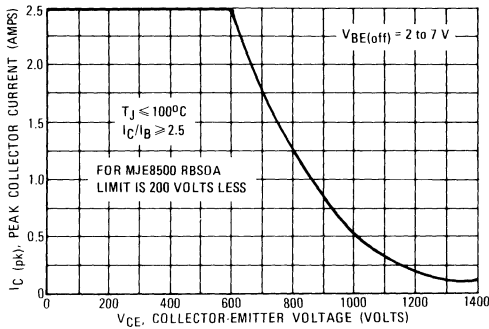
FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

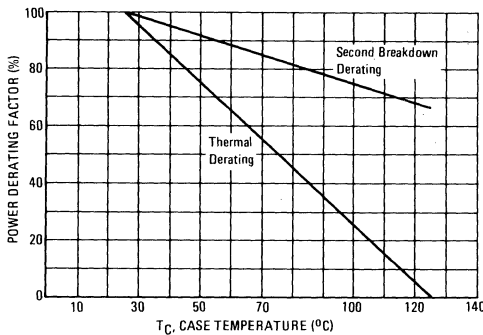
FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE8502 and MJE8503 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times

- 150 ns Inductive Fall Time—25°C (Typ)
- 400 ns Inductive Crossover Time—25°C (Typ)
- 1200 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range —65 to +125°C

100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

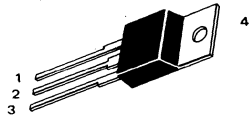
5.0 AMPERE

NPN SILICON
POWER TRANSISTORS

700 and 800 VOLTS
80 WATTS

Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



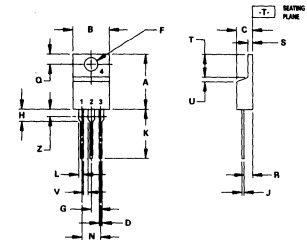
MAXIMUM RATINGS

Rating	Symbol	MJE8502	MJE8503	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	700	800	Vdc
Collector-Emitter Voltage	V_{CEV}	1200	1400	Vdc
Emitter Base Voltage	V_{EB}	8.0	8.0	Vdc
Collector Current — Continuous	I_C	5.0	5.0	Adc
Peak (1)	I_{CM}	10	10	
Base Current — Continuous	I_B	4.0	4.0	Adc
Peak (1)	I_{BM}	8.0	8.0	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	80	80	Watts
@ $T_C = 100^\circ\text{C}$		21	21	
Derate above 25°C		0.80	0.80	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +125		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



DIM	MILLIMETRIC		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	5.96	10.28	0.235	0.405
C	4.07	4.82	0.160	0.190
D	0.94	0.98	0.035	0.035
E	5.51	7.73	0.217	0.304
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
M	4.80	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.54	2.79	0.100	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.90	1.27	0.035	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
 1. PN 1 BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MJE8502, MJE8503

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0)	MJE8502 MJE8503	V _{CEO(sus)}	700 800	— —	— —	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)		I _{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current (V _{CE} = Rated V _{CEV} , R _{BE} = 50 Ω, T _C = 100°C)		I _{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V _{EB} = 7.0 Vdc, I _C = 0)		I _{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	I _{S/b}	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 1.0 Adc, V _{CE} = 5.0 Vdc)	h _{FE}	7.5	—	—	—
Collector-Emitter Saturation Voltage (I _C = 2.5 Adc, I _B = 1.0 Adc) (I _C = 5.0 Adc, I _B = 2.0 Adc) (I _C = 2.5 Adc, I _B = 1.0 Adc, T _C = 100°C)	V _{CE(sat)}	— — —	— — —	2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage (I _C = 2.5 Adc, I _B = 1.0 Adc) (I _C = 2.5 Adc, I _B = 1.0 Adc, T _C = 100°C)	V _{BE(sat)}	— —	— —	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1.0 kHz)	C _{ob}	60	—	300	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	[V _{CC} = 500 Vdc, I _C = 2.5 A, I _{B1} = 1.0 A, V _{BE(off)} = 5.0 Vdc, t _p = 50 μs, Duty Cycle ≤ 2.0%]	t _d	—	0.040	0.20	μs
Rise Time		t _r	—	0.125	2.0	μs
Storage Time		t _s	—	1.2	4.0	μs
Fall Time		t _f	—	0.65	2.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	[I _C = 2.5 A(pk), V _{clamp} = 500 Vdc, I _{B1} = 1.0 A, V _{BE(off)} = 5 Vdc, T _C = 100°C]	t _{sv}	—	1.6	5.0	μs
Crossover Time		t _c	—	0.60	2.0	μs
Storage Time	[I _C = 2.5 A(pk), V _{clamp} = 500 Vdc, I _{B1} = 1.0 A, V _{BE(off)} = 5 Vdc, T _C = 25°C]	t _{sv}	—	1.2	—	μs
Crossover Time		t _c	—	0.4	—	μs
Fall Time		t _{fi}	—	0.15	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 - DC CURRENT GAIN

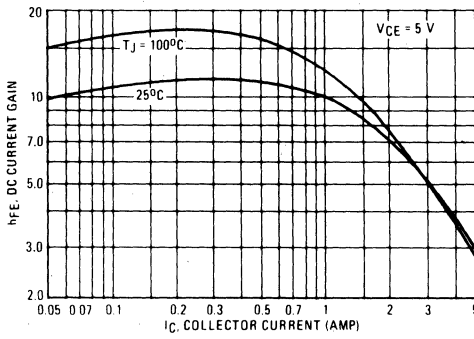


FIGURE 2 - COLLECTOR SATURATION REGION

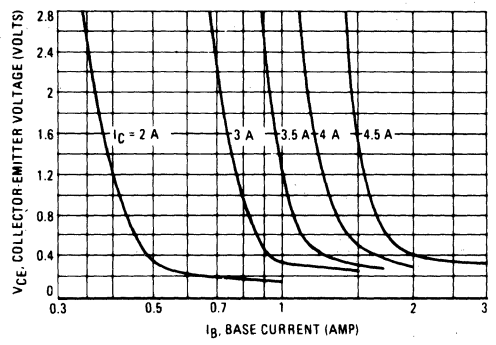


FIGURE 3 - COLLECTOR-EMITTER SATURATION REGION

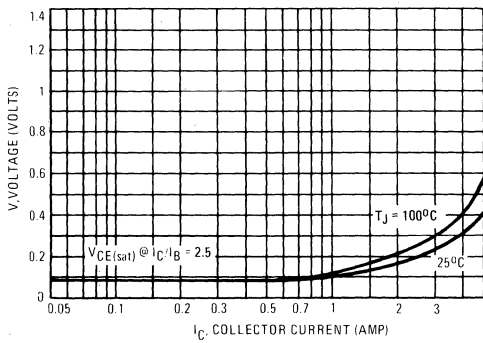


FIGURE 4 - BASE-EMITTER VOLTAGE

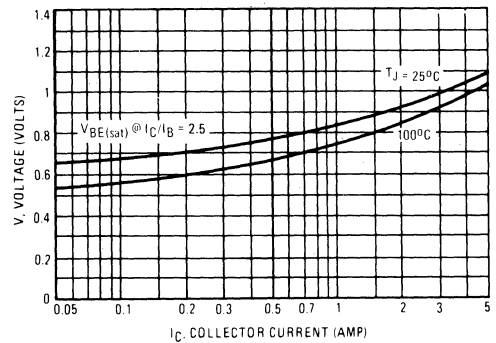


FIGURE 5 - COLLECTOR CUTOFF REGION

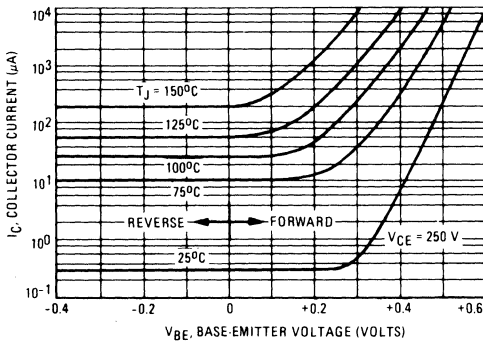
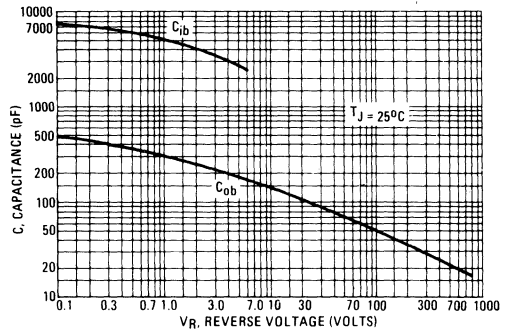
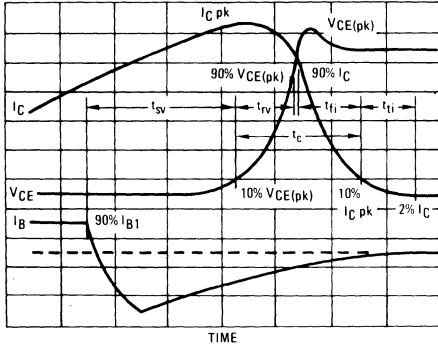


FIGURE 6 - CAPACITANCE



SWITCHING TIMES NOTE

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_B to 10% $V_{CE(pk)}$
- t_{rv} = Voltage Rise Time, 10–90% $V_{CE(pk)}$
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

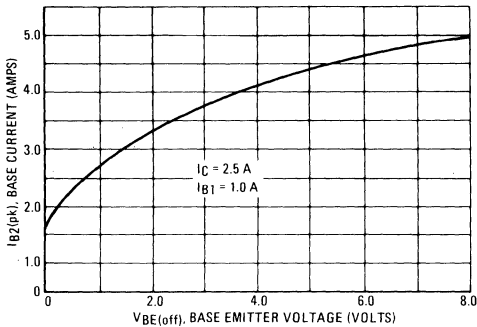
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 8 – PEAK REVERSE BASE CURRENT



TYPICAL RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON SWITCHING TIMES

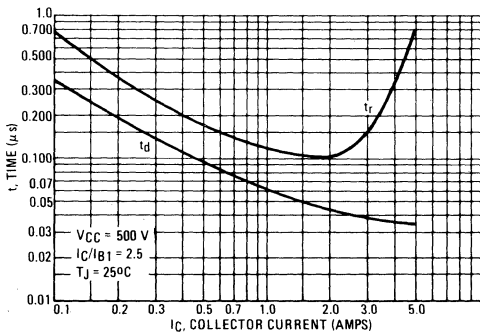


FIGURE 10 – TURN-OFF SWITCHING TIMES

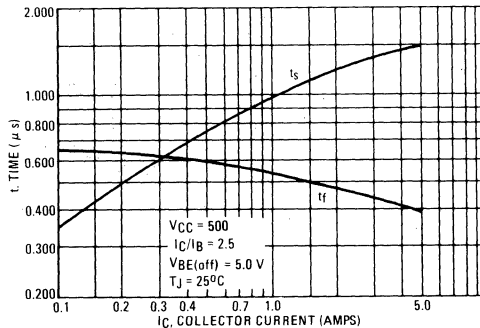
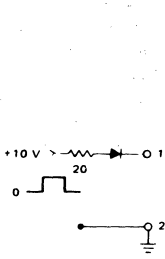
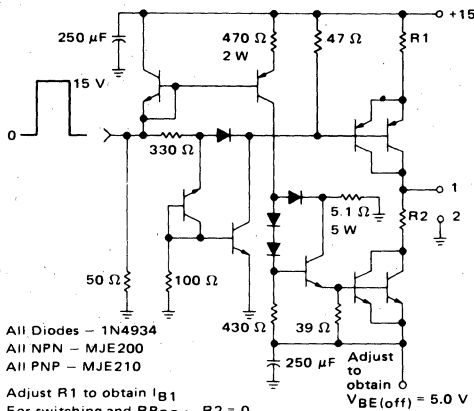
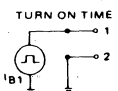
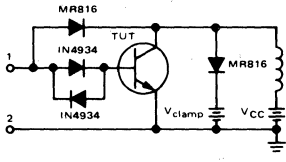
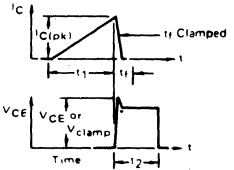
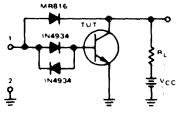
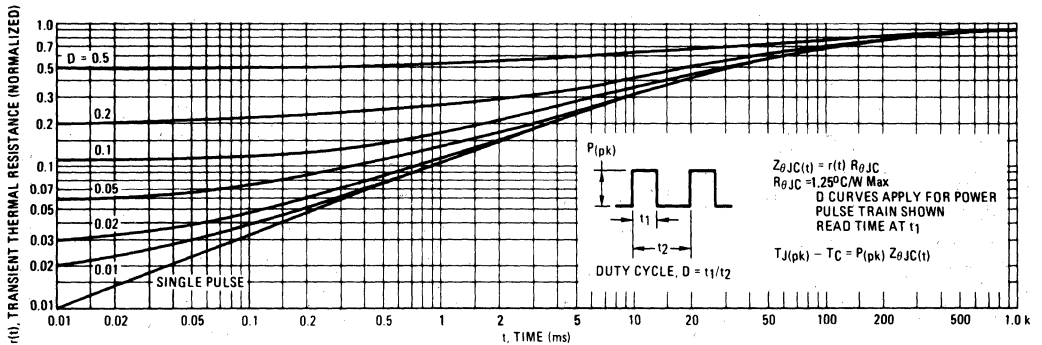


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I_C = 100 mA</p>	 <p>All Diodes - 1N4934 All NPN - MJE200 All PNP - MJE210 Adjust R1 to obtain I_{B1} For switching and R_{BSOA}, R2 = 0 For BV_{CEO(sus)}, R2 = ∞ Adjust to obtain V_{BE(off)} = 5.0 V</p>	 <p>TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 500 V</p>	<p>V_{CC} = 500 V R_L = 200 Ω Pulse Width = 10 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> 	<p>OUTPUT WAVEFORMS</p>  <p>t₁ Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

3

FIGURE 11 - THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

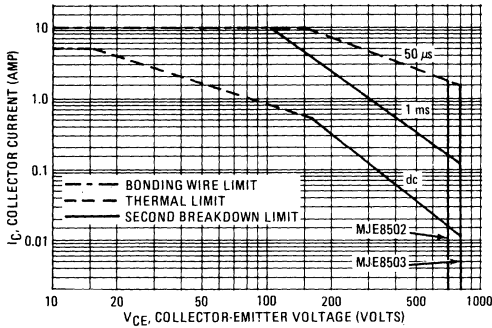


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA

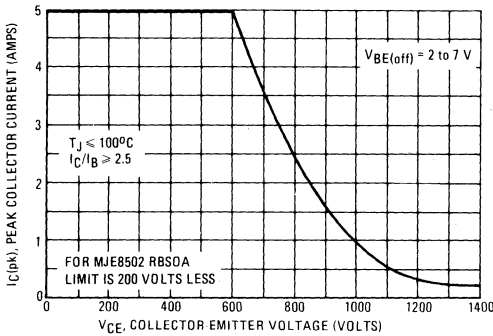
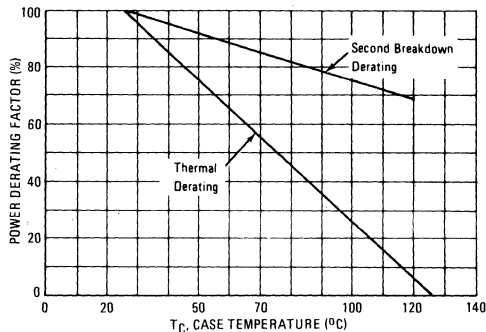


FIGURE 14 – POWER DERATING



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(pk)$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

HORIZONTAL DEFLECTION TRANSISTOR

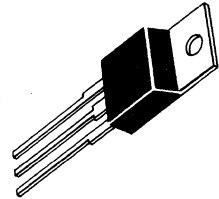
... specifically designed for use in small screen black and white deflection circuits.

- Collector-Emitter Voltage – $V_{CEX} = 1500$ Volts
- Glassivated Base-Collector Junction
- Switching Times with Inductive Loads –
 $t_f = 0.65 \mu s$ (Typ) @ $I_C = 2.0$ A

2.5 AMPERE

NPN SILICON
POWER TRANSISTOR

1500 VOLTS
65 WATTS

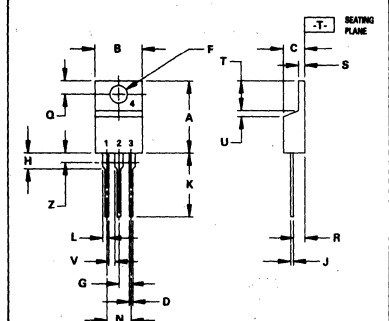


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	2.5	Adc
Base Current – Continuous	I_B	2.0	Adc
Emitter Current – Continuous	I_E	4.5	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	65	Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +125	$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.54	$^\circ C/W$



NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

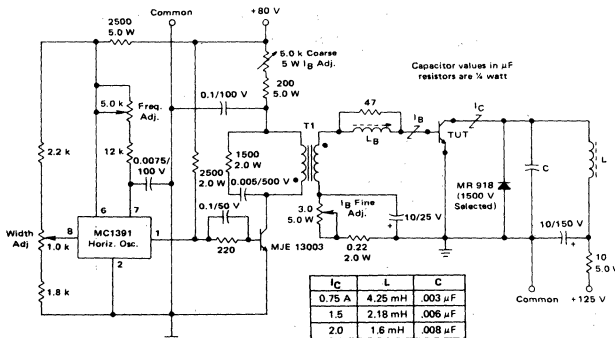
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.91	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.94	2.79	0.090	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 221A-04
TO-220AB

3

FIGURE 1 – TEST CIRCUIT



I_C	L	C
0.75 A	4.25 mH	.003 μF
1.5	2.18 mH	.006 μF
2.0	1.6 mH	.008 μF

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance – 39 mH. Secondary Inductance – 22 mH. Leakage Inductance with primary shorted – 2.0 μH . Primary 260 turns #28 AWG enamel wire. Secondary 17 turns, #22 AWG enamel wire.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I _C = 50 mAdc, I _B = 0)	V _{CEO(sus)}	750	—	—	Vdc
Collector Cutoff Current (V _{CE} = 1500 Vdc, V _{BE} = 0)	I _{CES}	—	—	1.0	mAdc
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	—	—	0.1	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I _C = 2.0 Adc, I _B = 1.8 Adc)	V _{CE(sat)}	—	—	5.0	Vdc
Base-Emitter Saturation Voltage (I _C = 2.0 Adc, I _B = 1.8 Adc)	V _{BE(sat)}	—	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	—	50	—	pF
Current Gain – Bandwidth Product (1) (I _C = 0.1 Adc, V _{CE} = 5.0 Vdc, f _{test} = 1.0 MHz)	f _T	—	4.0	—	MHz
SWITCHING CHARACTERISTICS					
Fall Time (I _C = 2.0 Adc, I _{B1} = 1.0 Adc, L _B = 12 μH)	t _f	—	0.65	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 2 – DC CURRENT GAIN

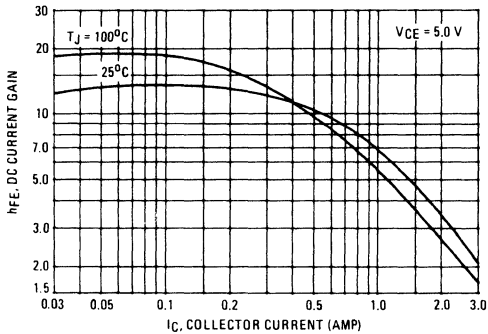


FIGURE 3 – "ON" VOLTAGE

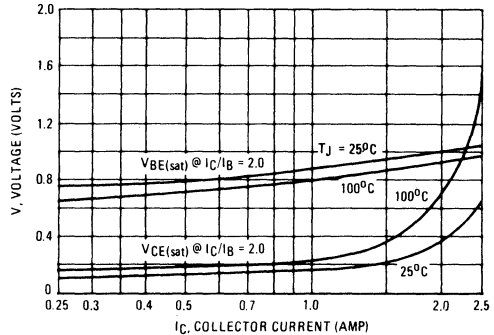
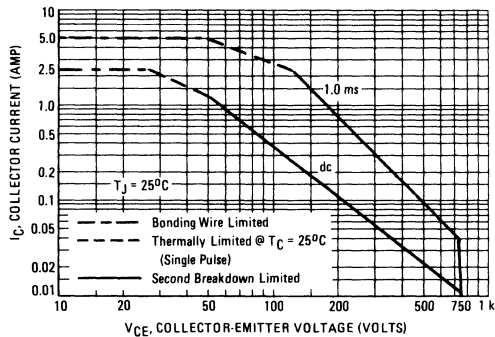


FIGURE 4 – SAFE OPERATING AREA



Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- Reverse Biased SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and 100°C ... t_c @ 1 A, 100°C is 290 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

MAXIMUM RATINGS

Rating	Symbol	MJE13002	MJE13003	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current – Continuous	I_C	1.5		Adc
– Peak (1)	I_{CM}	3		
Base Current – Continuous	I_B	0.75		Adc
– Peak (1)	I_{BM}	1.5		
Emitter Current – Continuous	I_E	2.25		Adc
– Peak (1)	I_{EM}	4.5		
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.4		Watts
Derate above 25°C		11.2		mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	40		Watts
Derate above 25°C		320		mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

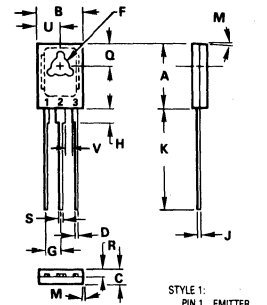
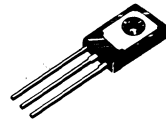
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	89	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

1.5 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
40 WATTS



STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. BASE

NOTES:
 1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA TO DIM A & B AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.94	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.32	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.53	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3" TYP		3" TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-05

MJE13002, MJE13003

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS (1)

Collector-Emitter Sustaining Voltage (I _C = 10 mA, I _B = 0)	MJE13002 MJE13003	V _{CEO(sus)}	300 400	— —	— —	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)		I _{CEV}	— —	— —	1 5	mAdc
Emitter Cutoff Current (V _{EB} = 9 Vdc, I _C = 0)		I _{EBO}	—	—	1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	I _{S/b}	See Figure 11			
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 12			

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 0.5 Adc, V _{CE} = 2 Vdc) (I _C = 1 Adc, V _{CE} = 2 Vdc)	h _{FE}	8 5	— —	40 25	—
Collector-Emitter Saturation Voltage (I _C = 0.5 Adc, I _B = 0.1 Adc) (I _C = 1 Adc, I _B = 0.25 Adc) (I _C = 1.5 Adc, I _B = 0.5 Adc) (I _C = 1 Adc, I _B = 0.25 Adc, T _C = 100°C)	V _{CE(sat)}	— — — —	— — — —	0.5 1 3 1	Vdc
Base-Emitter Saturation Voltage (I _C = 0.5 Adc, I _B = 0.1 Adc) (I _C = 1 Adc, I _B = 0.25 Adc) (I _C = 1 Adc, I _B = 0.25 Adc, T _C = 100°C)	V _{BE(sat)}	— — —	— — —	1 1.2 1.1	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain – Bandwidth Product (I _C = 100 mAdc, V _{CE} = 10 Vdc, f = 1 MHz)	f _T	4	10	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	—	21	—	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 125 Vdc, I _C = 1 A, I _{B1} = I _{B2} = 0.2 A, t _p = 25 μs, Duty Cycle < 1%)	t _d	—	0.05	0.1	μs
Rise Time		t _r	—	0.5	1	μs
Storage Time		t _s	—	2	4	μs
Fall Time		t _f	—	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Storage Time	(I _C = 1 A, V _{clamp} = 300 Vdc, I _{B1} = 0.2 A, V _{BE(off)} = 5 Vdc, T _C = 100°C)	t _{sv}	—	1.7	4	μs
Crossover Time		t _c	—	0.29	0.75	μs
Fall Time		t _{fi}	—	0.15	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – DC CURRENT GAIN

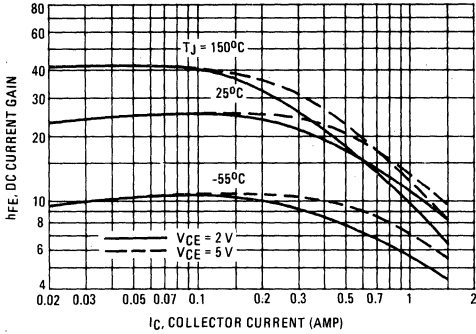


FIGURE 2 – COLLECTOR SATURATION REGION

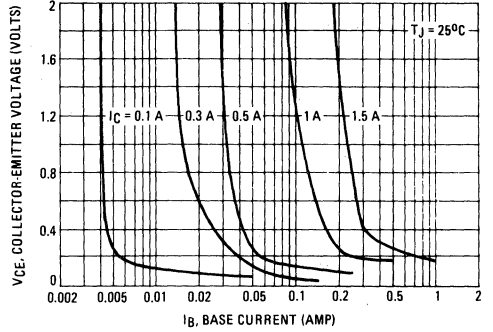


FIGURE 3 – BASE-EMITTER VOLTAGE

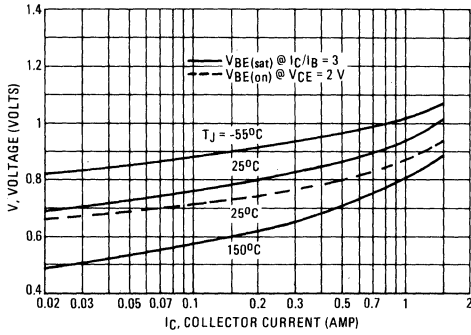


FIGURE 4 – COLLECTOR-EMITTER SATURATION REGION

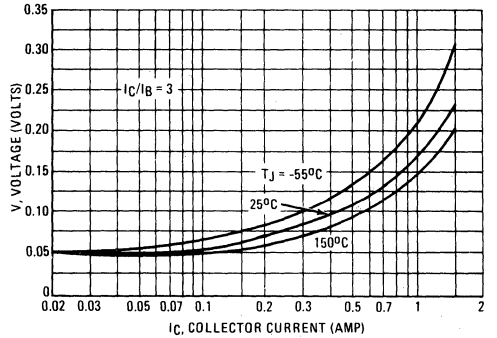


FIGURE 5 – COLLECTOR CUTOFF REGION

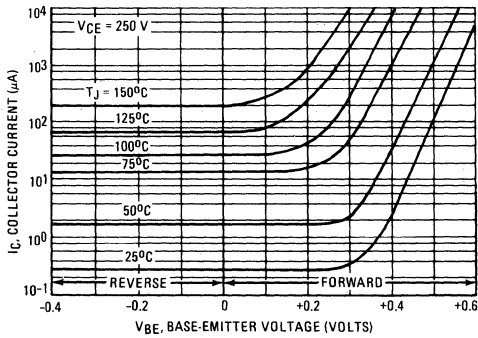


FIGURE 6 – CAPACITANCE

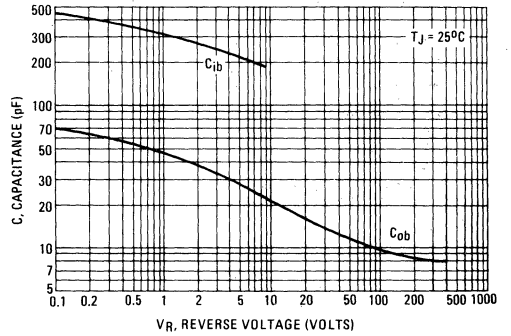


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
TEST CIRCUITS	<p>Duty Cycle < 10% $t_r, t_f < 10$ ns</p> <p>NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}</p>	
	CIRCUIT VALUES	<p>Coil Data: Ferroxcube Core #6656 Full Bobbin (~200 Turns) #20</p> <p>GAP for 30 mH/2A $L_{coil} = 50$ mH</p> <p>$V_{CC} = 20$ V $V_{clamp} = 300$ Vdc</p>
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope-Tektronics 475 or Equivalent</p>	<p>$t_r, t_f < 10$ ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C</p>

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

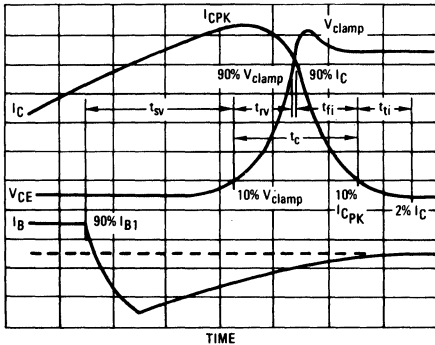


TABLE 2 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} μ s	t_{rv} μ s	t_{fi} μ s	t_{ti} μ s	t_c μ s
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

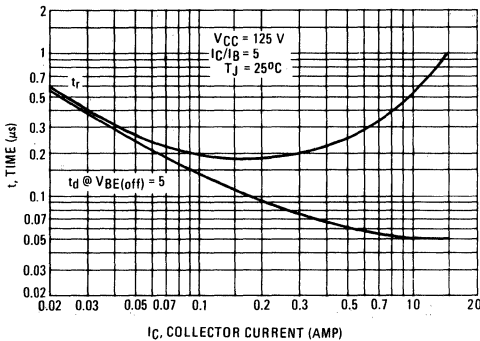


FIGURE 9 – TURN-OFF TIME

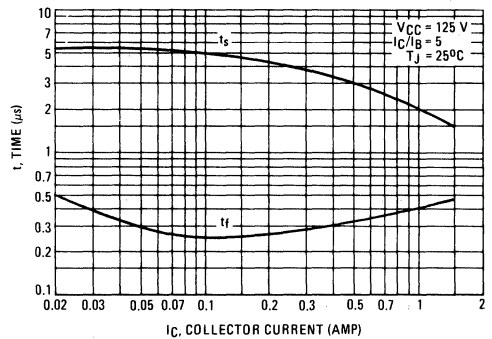
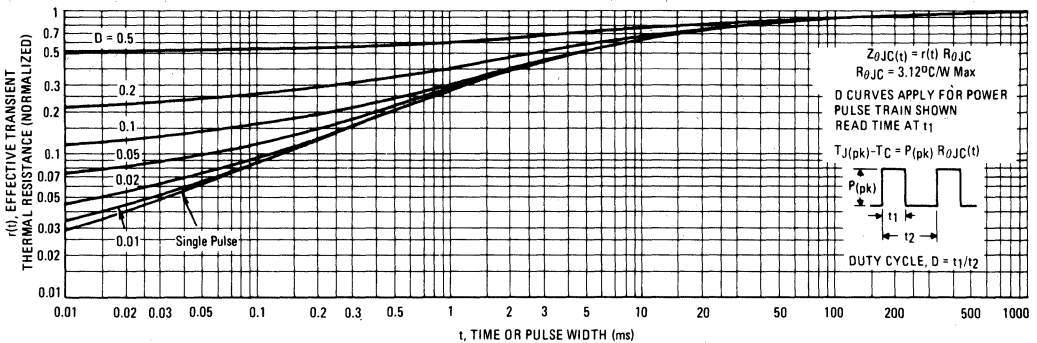


FIGURE 10 – THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 — FORWARD BIAS SAFE OPERATION AREA

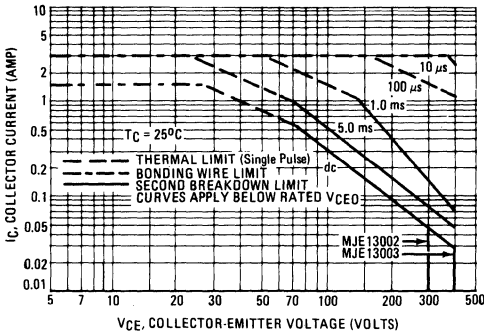


FIGURE 12 — REVERSE BIAS SAFE OPERATING AREA

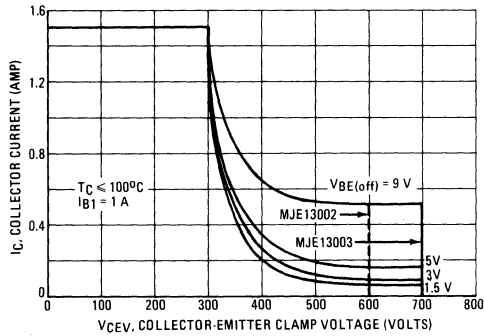
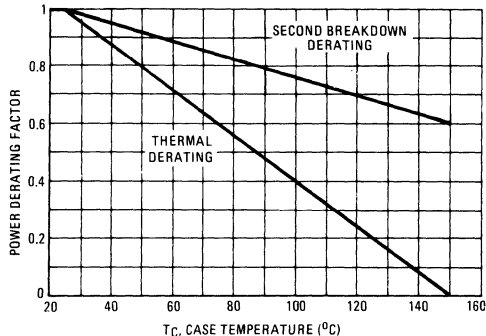


FIGURE 13 — FORWARD BIAS POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

MJE13004
MJE13005

Designers Data Sheet

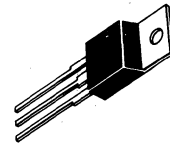
SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulator's, Inverters, Motor Controls, Solenoid / Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 2 to 4 Amp, 25 and 100°C
 ... t_c @ 3A, 100°C is 180 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information.

4 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
75 WATTS



MAXIMUM RATINGS

Rating	Symbol	MJE13004	MJE13005	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current – Continuous	I_C	4		Adc
– Peak (1)	I_{CM}	8		Adc
Base Current – Continuous	I_B	2		Adc
– Peak (1)	I_{BM}	4		Adc
Emitter Current – Continuous	I_E	6		Adc
– Peak (1)	I_{EM}	12		Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2		Watts
		16		mW/°C
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75		Watts
		600		mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

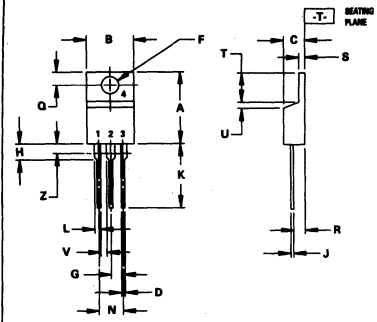
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.68	10.26	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.84	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.86	0.095	0.195
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
O	2.54	3.04	0.100	0.120
R	2.94	2.79	0.090	0.110
S	1.15	1.28	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- STYLE 1:**
1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 221A-04
TO-220AB

MJE13004, MJE13005

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I _C = 10 mA, I _B = 0)	MJE13004 MJE13005 V _{CEO(sus)}	300 400	— —	— —	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	— —	— —	1 5	mAdc
Emitter Cutoff Current (V _{EB} = 9 Vdc, I _C = 0)	I _{EBO}	—	—	1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	I _{S/b}		See Figure 11		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 12		

*ON CHARACTERISTICS

DC Current Gain (I _C = 1 Adc, V _{CE} = 5 Vdc) (I _C = 2 Adc, V _{CE} = 5 Vdc)	h _{FE}	10 8	— —	60 40	—
Collector-Emitter Saturation Voltage (I _C = 1 Adc, I _B = 0.2 Adc) (I _C = 2 Adc, I _B = 0.5 Adc) (I _C = 4 Adc, I _B = 1 Adc) (I _C = 2 Adc, I _B = 0.5 Adc, T _C = 100°C)	V _{CE(sat)}	— — — —	— — — —	0.5 0.6 1 1	Vdc
Base-Emitter Saturation Voltage (I _C = 1 Adc, I _B = 0.2 Adc) (I _C = 2 Adc, I _B = 0.5 Adc) (I _C = 2 Adc, I _B = 0.5 Adc, T _C = 100°C)	V _{BE(sat)}	— — —	— — —	1.2 1.6 1.5	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain – Bandwidth Product (I _C = 500 mAdc, V _{CE} = 10 Vdc, f = 1 MHz)	f _T	4	—	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	—	65	—	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 2)					
Delay Time	(V _{CC} = 125 Vdc, I _C = 2 A, I _{B1} = I _{B2} = 0.4 A, t _p = 25 μs, Duty Cycle ≤ 1%)	t _d	—	0.025	0.1 μs
Rise Time		t _r	—	0.3	0.7 μs
Storage Time		t _s	—	1.7	4 μs
Fall Time		t _f	—	0.4	0.9 μs
Inductive Load, Clamped (Table 2, Figure 13)					
Voltage Storage Time	(I _C = 2 A, V _{clamp} = 300 Vdc, I _{B1} = 0.4 A, V _{BE(off)} = 5 Vdc, T _C = 100°C)	t _{sv}	—	0.9	4 μs
Crossover Time		t _c	—	0.32	0.9 μs
Fall Time		t _{fi}	—	0.16	— μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – DC CURRENT GAIN

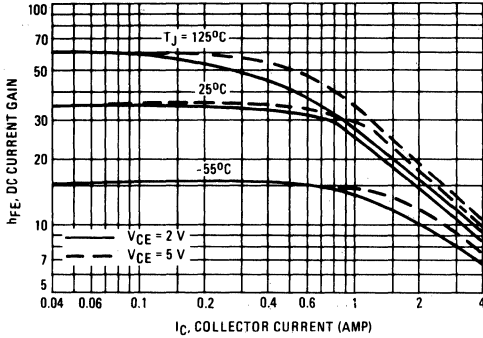


FIGURE 2 – COLLECTOR SATURATION REGION

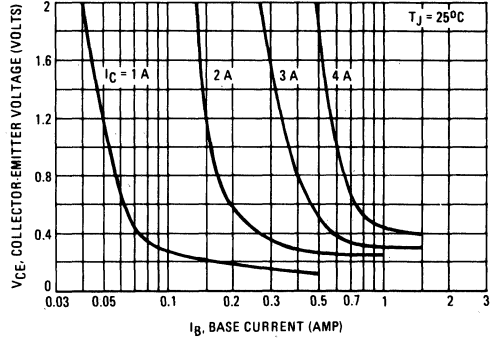


FIGURE 3 – BASE-EMITTER VOLTAGE

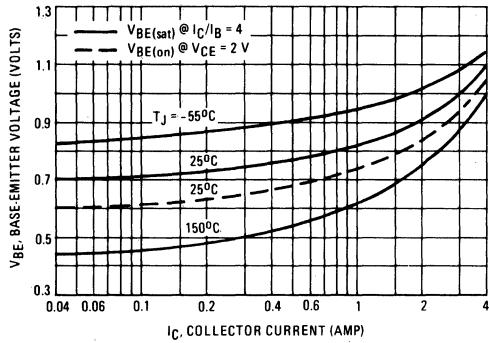


FIGURE 4 – COLLECTOR-EMITTER SATURATION VOLTAGE

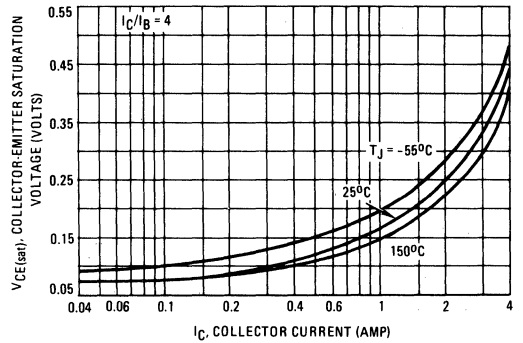


FIGURE 5 – COLLECTOR CUTOFF REGION

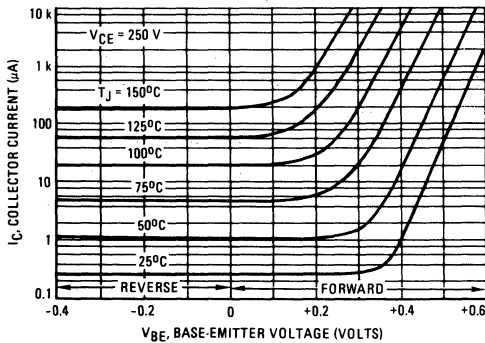


FIGURE 6 – CAPACITANCE

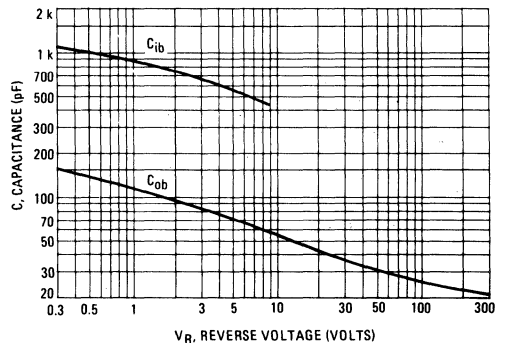
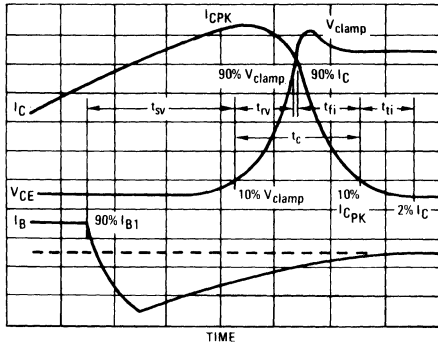


FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

TABLE 1 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
2	25	600	70	100	80	180
	100	900	110	240	130	320
3	25	650	60	140	60	200
	100	950	100	330	100	350
4	25	550	70	160	100	220
	100	850	110	350	160	390

NOTE: All Data recorded in the inductive Switching Circuit in Table 2.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

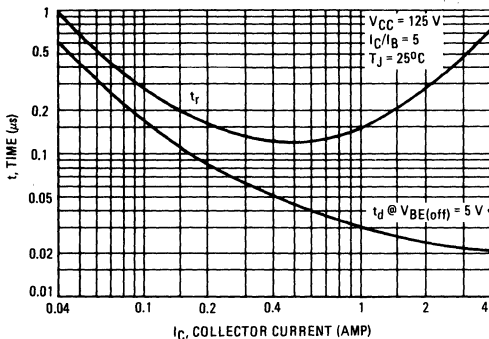


FIGURE 9 – TURN-OFF TIME

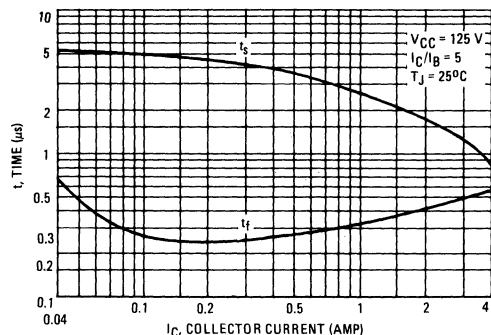
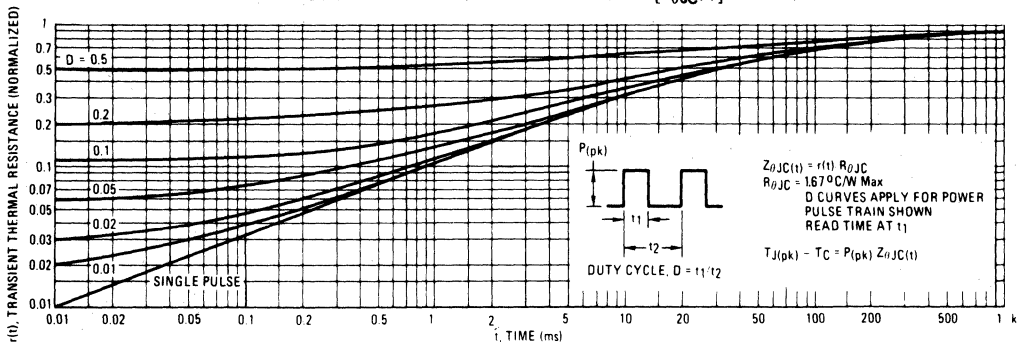


TABLE 2 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
TEST CIRCUITS	<p>Duty Cycle < 10% $t_r, t_f < 10$ ns</p> <p>NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}</p>	
CIRCUIT VALUES	<p>Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16</p> <p>GAP for 200 μH/20A $L_{coil} = 200$ μH</p> <p>$V_{CC} = 20$ V $V_{clamp} = 300$ Vdc</p>	<p>$V_{CC} = 125$ V $R_C = 62$ Ω D1 = 1N5820 or Equiv. $R_B = 22$ Ω</p>
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>$t_r, t_f < 10$ ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C</p>

3

FIGURE 10 - TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]



The Safe Operating Area Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

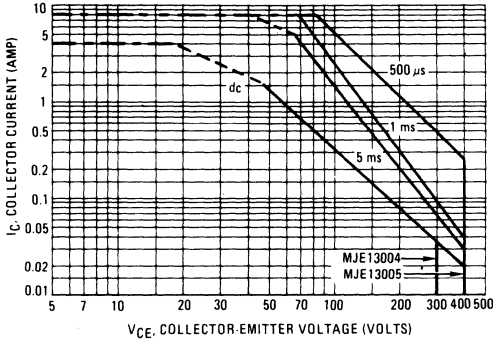


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA

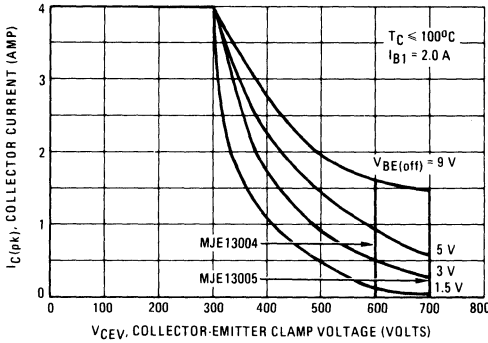
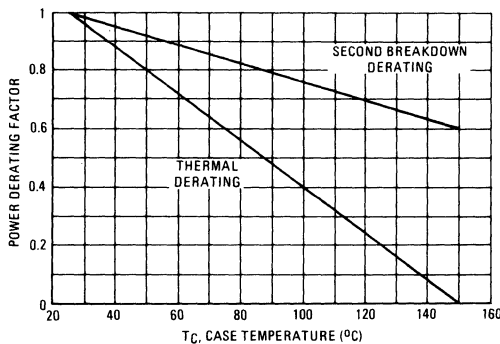


FIGURE 13 – FORWARD BIAS POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_J(\text{pk})$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

MJE13006 MJE13007

Designers Data Sheet

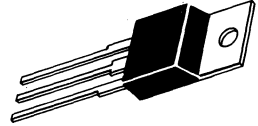
SWITCHMODE SERIES NPN SILICON POWER TRANSISTORS

The MJE13006 and MJE13007 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 3 to 8 Amp, 25 and 100°C
... t_c @ 5A, 100°C is 136 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

8 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
80 WATTS



Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

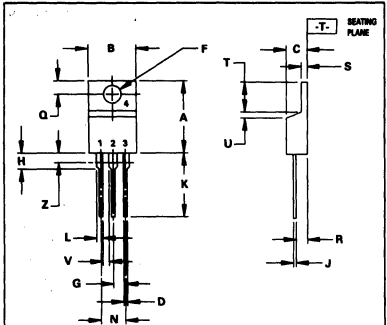
MAXIMUM RATINGS

Rating	Symbol	MJE13006	MJE13007	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous	I_C	8		Adc
— Peak (1)	I_{CM}	16		
Base Current — Continuous	I_B	4		Adc
— Peak (1)	I_{BM}	8		
Emitter Current — Continuous	I_E	12		Adc
— Peak (1)	I_{EM}	24		
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2	16	Watts $\text{mW}/^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	80	640	Watts $\text{mW}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.94	0.98	0.025	0.025
F	3.91	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
M	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.90	1.27	0.030	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

MJE13006, MJE13007

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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*OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (I _C = 10 mA, I _B = 0)	MJE13006 MJE13007	V _{CEO(sus)}	300 400	— —	— —	V _{dc}
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 V _{dc}) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 V _{dc} , T _C = 100°C)		I _{CEV}	— —	— —	1 5	mAdc
Emitter Cutoff Current (V _{EB} = 9 V _{dc} , I _C = 0)		I _{EBO}	—	—	1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	I _{S/b}	—	—	—	See Figure 1
Clamped Inductive SOA with Base Reverse Biased	—	—	—	—	See Figure 2

*ON CHARACTERISTICS

DC Current Gain (I _C = 2 Adc, V _{CE} = 5 V _{dc}) (I _C = 5 Adc, V _{CE} = 5 V _{dc})	h _{FE}	8 5	— —	60 30	—
Collector-Emitter Saturation Voltage (I _C = 2 Adc, I _B = 0.4 Adc) (I _C = 5 Adc, I _B = 1 Adc) (I _C = 8 Adc, I _B = 2 Adc) (I _C = 5 Adc, I _B = 1 Adc, T _C = 100°C)	V _{CE(sat)}	— — — —	— — — —	1 2 3 3	V _{dc}
Base-Emitter Saturation Voltage (I _C = 2 Adc, I _B = 0.4 Adc) (I _C = 5 Adc, I _B = 1 Adc) (I _C = 5 Adc, I _B = 1 Adc, T _C = 100°C)	V _{BE(sat)}	— — —	— — —	1.2 1.6 1.5	V _{dc}

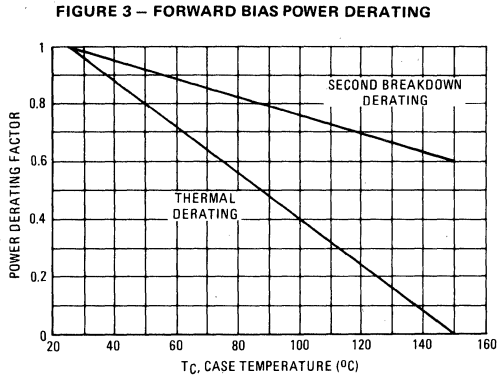
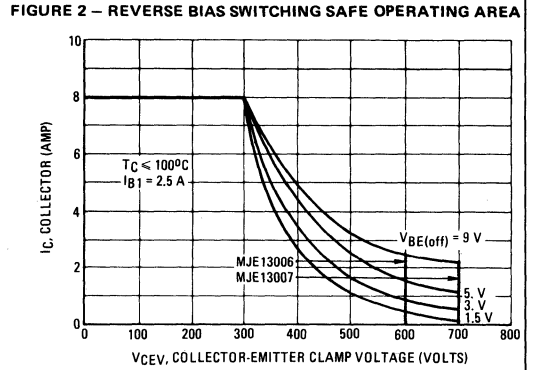
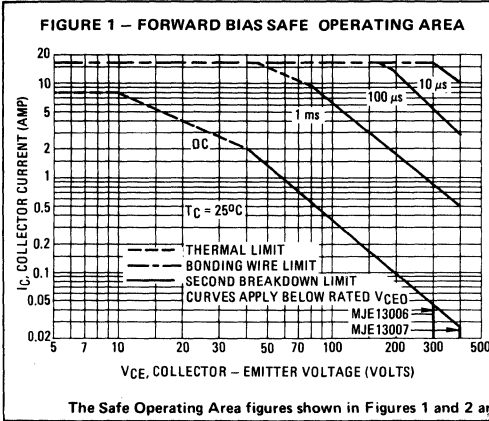
DYNAMIC CHARACTERISTICS

Current-Gain – Bandwidth Product (I _C = 500 mAdc, V _{CE} = 10 V _{dc} , f = 1 MHz)	f _T	4	—	—	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 0.1 MHz)	C _{ob}	—	110	—	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)					
Delay Time	(V _{CC} = 125 V _{dc} , I _C = 5 A, I _{B1} = I _{B2} = 1 A, t _p = 25 μs, Duty Cycle ≤ 1%)	t _d	—	0.05	0.1 μs
Rise Time		t _r	—	0.8	1.5 μs
Storage Time		t _s	—	1	3 μs
Fall Time		t _f	—	0.15	0.7 μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time	(I _C = 5 A, V _{clamp} = 300 V _{dc} ,	t _{ev}	—	0.86	2.3 μs
Crossover Time	I _{B1} = 1 A, V _{BE(off)} = 5 V _{dc} , T _C = 100°C)	t _c	—	0.14	0.7 μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

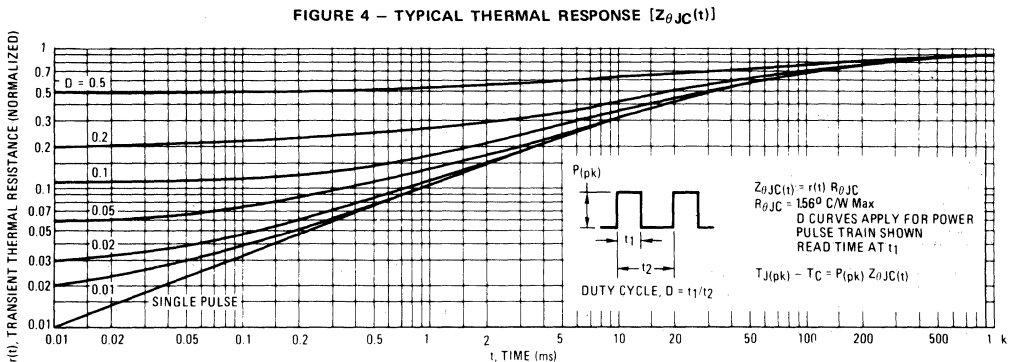


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_J(\text{pk})$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.



3

FIGURE 5 – DC CURRENT GAIN

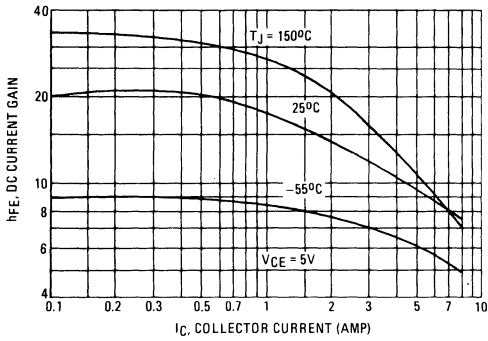


FIGURE 6 – COLLECTOR SATURATION REGION

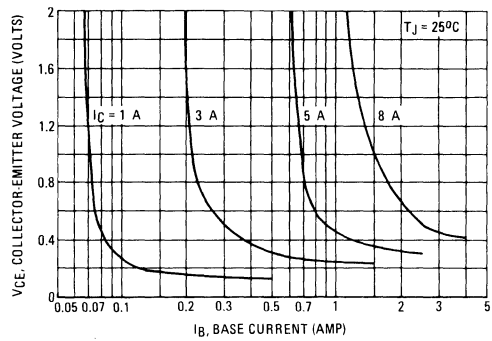


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE

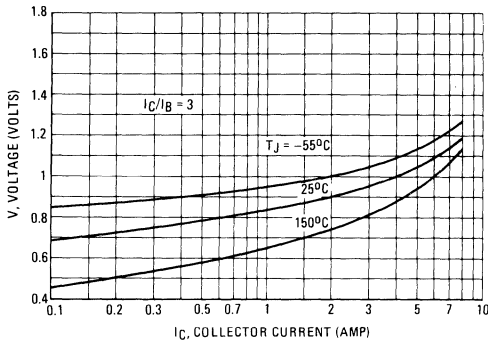


FIGURE 8 – COLLECTOR-EMITTER SATURATION VOLTAGE

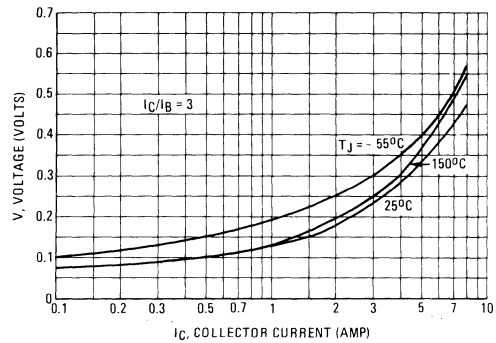


FIGURE 9 – COLLECTOR CUTOFF REGION

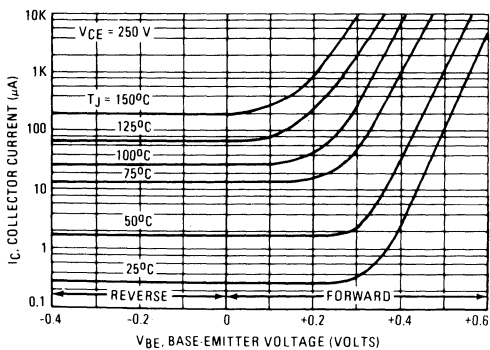


FIGURE 10 – CAPACITANCE

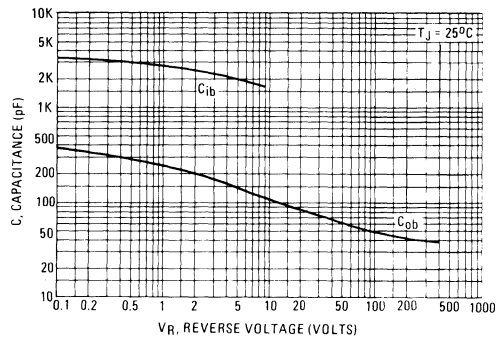


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	<p>Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16</p> <p>GAP for 200 μH/20A L_{coil} = 200 μH</p> <p>V_{CC} = 20 V V_{clamp} = 300 V</p>	<p>V_{CC} = 125 V R_C = 25 Ω D1 = 1N5820 or Equiv. R_B = 10 Ω</p>
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil} (I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{CM})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C</p>

APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at I_C = I_{leakage} ≈ 0 in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use

condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737A, AN-767, and AN-752.



VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

- (1) The device thermal limitations are not exceeded.
- (2) The turn-on time does not exceed 10 μ s (see standard pulsed forward SOA curves in Figure 1).
- (3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy

handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

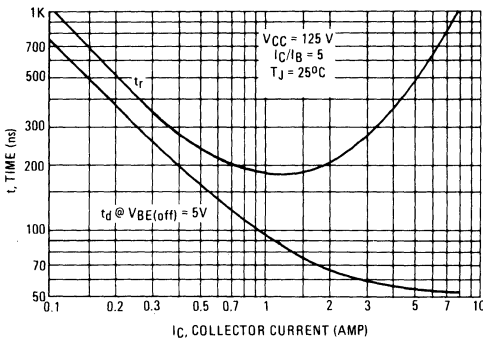


FIGURE 12 – TURN-OFF TIME

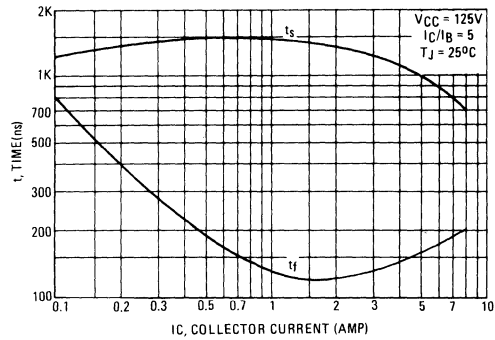


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

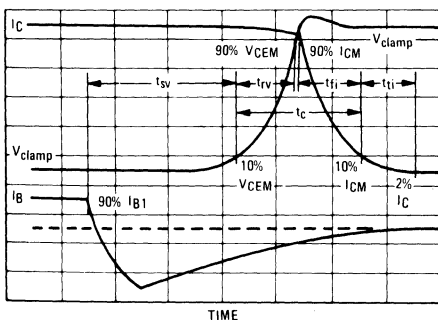


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS (at 300 V and 8A with $I_{B1} = 1.6A$ and $V_{BE(off)} = 5V$)

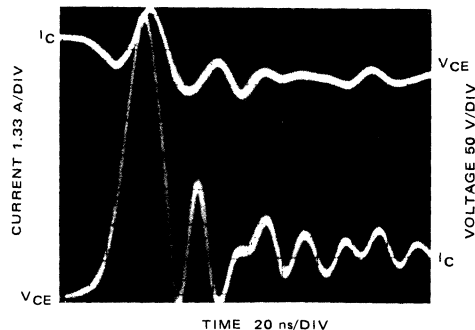
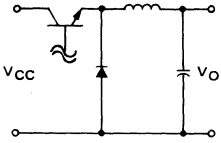
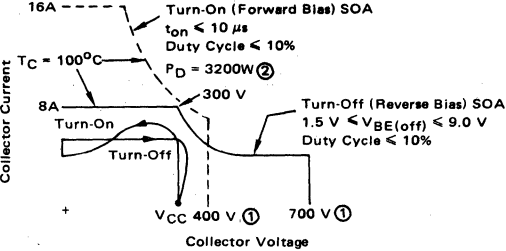
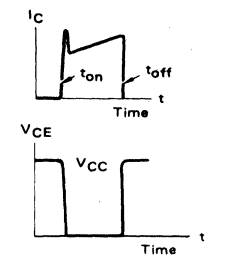
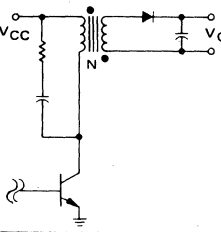
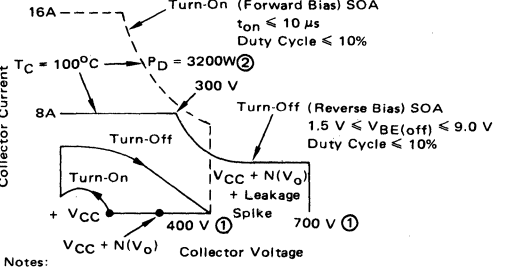
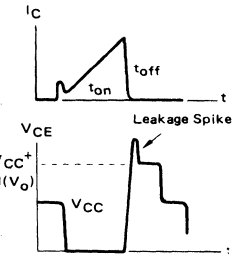
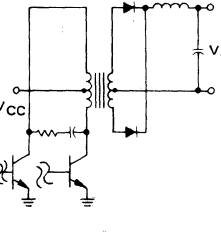
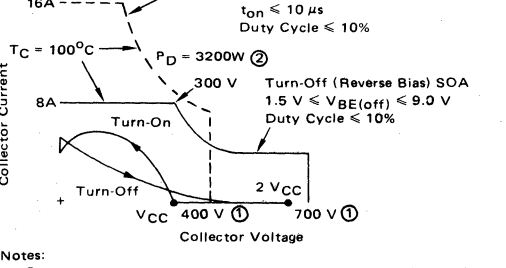
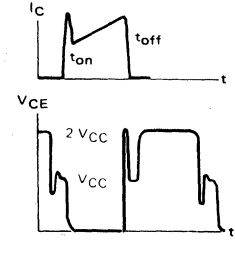
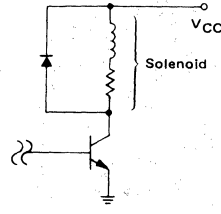
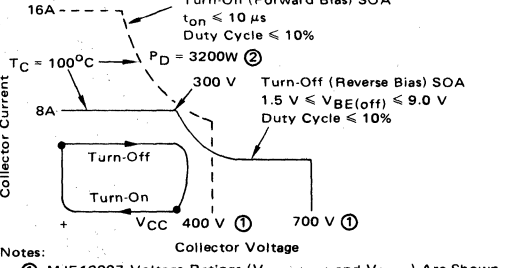
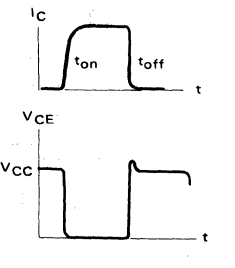


TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
<p>A</p> <p>SERIES SWITCHING REGULATOR</p> 	 <p>Notes:</p> <ol style="list-style-type: none"> ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13006 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure. 	
<p>B</p> <p>RINGING CHOKE INVERTER</p> 	 <p>Notes:</p> <ol style="list-style-type: none"> ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure 	
<p>C</p> <p>PUSH-PULL INVERTER/CONVERTER</p> 	 <p>Notes:</p> <ol style="list-style-type: none"> ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure. 	
<p>D</p> <p>SOLENOID DRIVER</p> 	 <p>Notes:</p> <ol style="list-style-type: none"> ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure. 	

3

TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I _C AMP	T _C °C	t _{sv} ns	t _{rv} ns	t _{fi} ns	t _{tj} ns	t _c ns
3	25	730	115	100	110	200
	100	1000	150	100	150	250
5	25	600	60	23	4	85
	100	860	84	50	10	136
8	25	650	25	26	4	42
	100	880	52	80	20	160

NOTE: All Data recorded in the inductive Switching Circuit in Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
- t_{fi} = Current Fall Time, 90–10% I_{CM}
- t_{tj} = Current Tail, 10–2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

Typical inductive switching waveforms are shown in Figure 14. In general, t_{rv} + t_{fi} ≈ t_c. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.



MJE13008
MJE13009

Designers Data Sheet

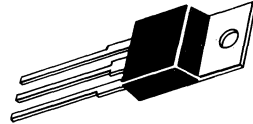
SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE13008 and MJE13009 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CE(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 3 to 12 Amp, 25 and 100 μs ... t_C @ 8 A, 100 $^\circ\text{C}$ is 120 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

12 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
100 WATTS



Designer's Data for
"Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

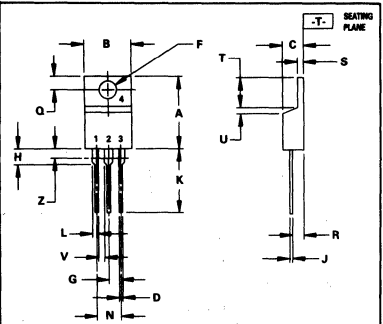
MAXIMUM RATINGS

Rating	Symbol	MJE13008	MJE13009	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous	I_C	12		Adc
— Peak (1)	I_{CM}	24		
Base Current — Continuous	I_B	6		Adc
— Peak (1)	I_{BM}	12		
Emitter Current — Continuous	I_E	18		Adc
— Peak (1)	I_{EM}	36		
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25 $^\circ\text{C}$	P_D	2	16	Watts mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25 $^\circ\text{C}$	P_D	100	800	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.85	10.28	0.390	0.405
C	4.07	4.92	0.160	0.190
D	0.64	0.88	0.025	0.035
E	3.61	3.73	0.142	0.147
F	2.42	2.66	0.095	0.105
G	2.80	3.93	0.110	0.155
H	0.46	0.71	0.018	0.028
I	12.70	14.27	0.500	0.562
J	1.15	1.39	0.045	0.055
K	4.83	5.33	0.190	0.210
L	2.54	3.04	0.100	0.120
M	2.04	2.79	0.080	0.110
N	1.15	1.39	0.045	0.055
O	5.97	6.47	0.235	0.255
P	0.00	1.27	0.000	0.050
Q	1.15	—	0.045	—
R	—	2.04	—	0.080

- STYLE 1:
 PIN 1: BASE
 2: COLLECTOR
 3: EMITTER
 4: COLLECTOR

CASE 221A-04
TO-220AB

MJE13008, MJE13009

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

*OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (I _C = 10 mA, I _B = 0)	MJE13008 MJE13009 V _{CEO(sus)}	300 400	–	–	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	–	–	1 5	mAdc
Emitter Cutoff Current (V _{EB} = 9 Vdc, I _C = 0)	I _{EBO}	–	–	1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	I _{S/b}	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased	–	See Figure 2			

*ON CHARACTERISTICS

DC Current Gain (I _C = 5 Adc, V _{CE} = 5 Vdc) (I _C = 8 Adc, V _{CE} = 5 Vdc)	h _{FE}	8 6	–	40 30	–
Collector-Emitter Saturation Voltage (I _C = 5 Adc, I _B = 1 Adc) (I _C = 8 Adc, I _B = 1.6 Adc) (I _C = 12 Adc, I _B = 3 Adc) (I _C = 8 Adc, I _B = 1.6 Adc, T _C = 100°C)	V _{CE(sat)}	–	–	1 1.5 3 2	Vdc
Base-Emitter Saturation Voltage (I _C = 5 Adc, I _B = 1 Adc) (I _C = 8 Adc, I _B = 1.6 Adc) (I _C = 8 Adc, I _B = 1.6 Adc, T _C = 100°C)	V _{BE(sat)}	–	–	1.2 1.6 1.5	Vdc

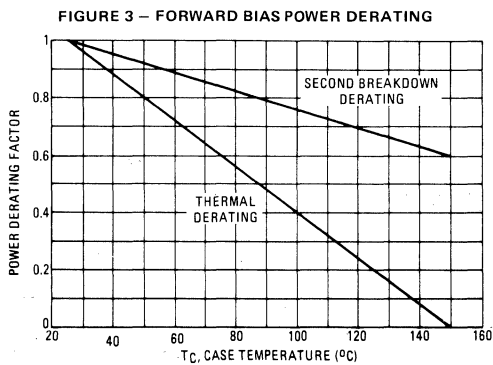
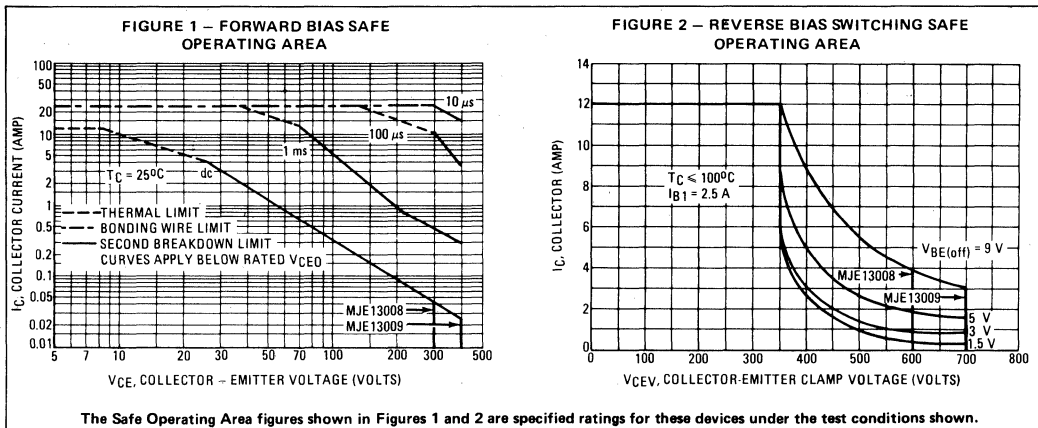
DYNAMIC CHARACTERISTICS

Current-Gain – Bandwidth Product (I _C = 500 mAdc, V _{CE} = 10 Vdc, f = 1 MHz)	f _T	4	–	–	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	–	180	–	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)					
Delay Time	V _{CC} = 125 Vdc, I _C = 8 A, I _{B1} = I _{B2} = 1.6 A, t _p = 25 μs, Duty Cycle ≤ 1%	t _d	–	0.06	0.1 μs
Rise Time		t _r	–	0.45	1 μs
Storage Time		t _s	–	1.3	3 μs
Fall Time		t _f	–	0.2	0.7 μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time	I _C = 8 A, V _{clamp} = 300 Vdc, I _{B1} = 1.6 A, V _{BE(off)} = 5 Vdc, T _C = 100°C)	t _{sv}	–	0.92	2.3 μs
Crossover Time		t _c	–	0.12	0.7 μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

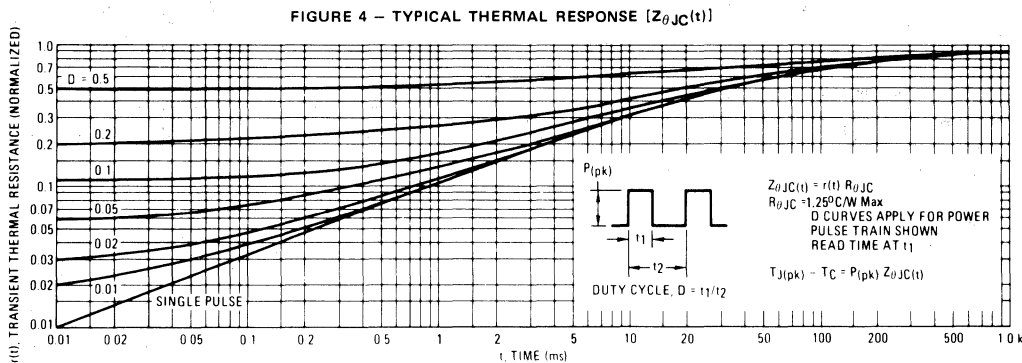


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^{\circ}C$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^{\circ}C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_J(pk)$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.



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FIGURE 5 - DC CURRENT GAIN

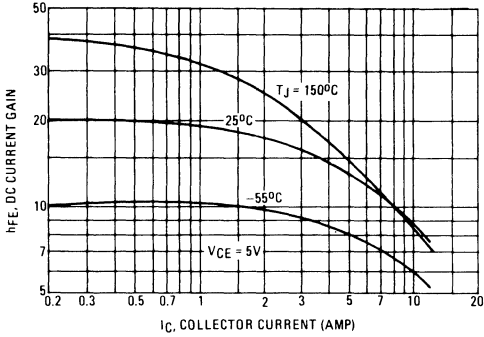


FIGURE 6 - COLLECTOR SATURATION REGION

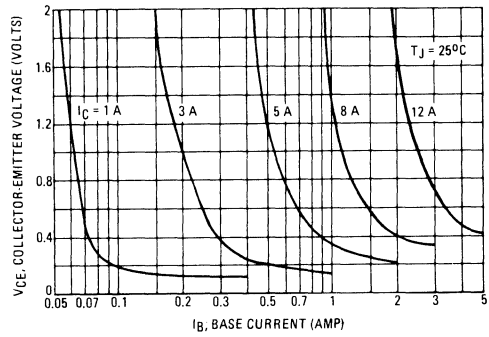


FIGURE 7 - BASE-EMITTER SATURATION VOLTAGE

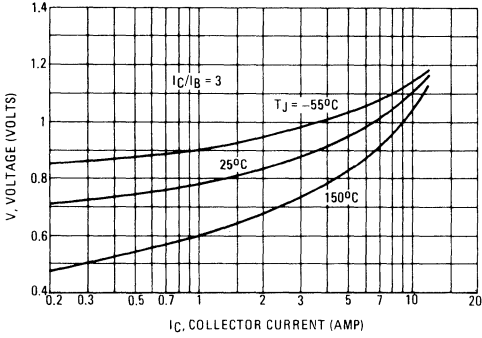


FIGURE 8 - COLLECTOR-EMITTER SATURATION VOLTAGE

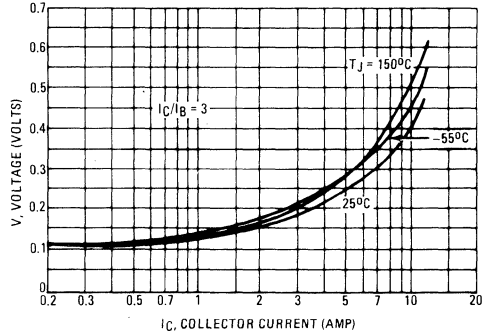


FIGURE 9 - COLLECTOR CUTOFF REGION

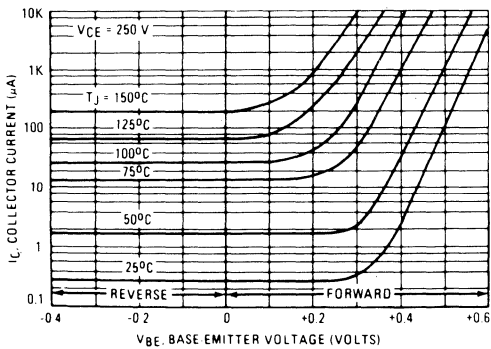


FIGURE 10 - CAPACITANCE

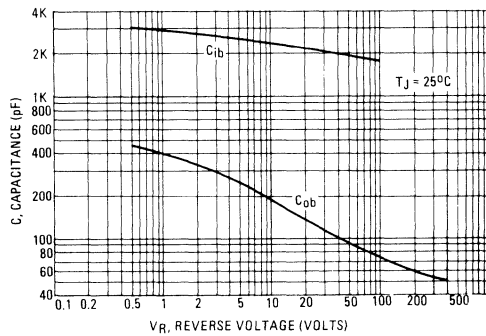


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
TEST CIRCUITS	<p>Duty Cycle \leq 10% $t_r, t_f \leq$ 10 ns</p> <p>NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}</p>	
CIRCUIT VALUES	<p>Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16</p> <p>GAP for 200 μH/20A $L_{coil} = 200 \mu$H</p> <p>$V_{CC} = 20$ V $V_{clamp} = 300$ Vdc</p>	<p>$V_{CC} = 125$ V $R_C = 15 \Omega$ D1 = 1N5820 or Equiv $R_B = 5.6 \Omega$</p>
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ <p>Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>$t_r, t_f < 10$ ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C</p>

APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use

condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737A, AN-752, AN-767.

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

- (1) The device thermal limitations are not exceeded.
- (2) The turn-on time does not exceed 10 μ s (see standard pulsed forward SOA curves in Figure 1).
- (3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy

handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 8 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_f). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

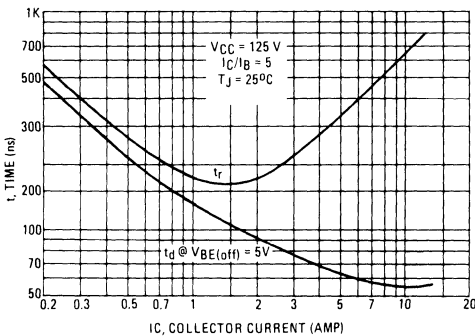


FIGURE 12 – TURN-OFF TIME

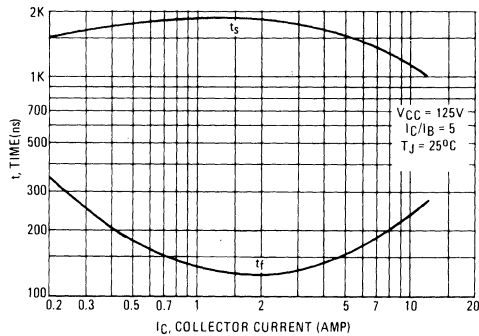


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

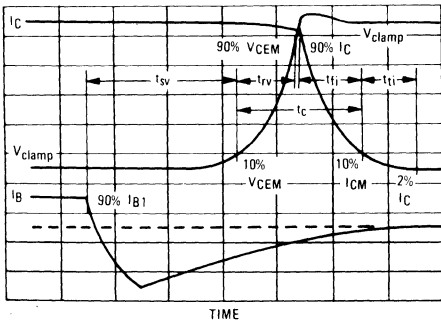


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS (at 300 V and 12 A with $I_{B1} = 2.4$ A and $V_{BE(off)} = 5$ V)

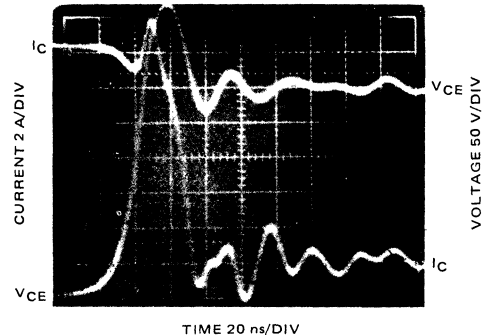
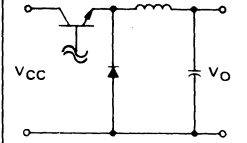
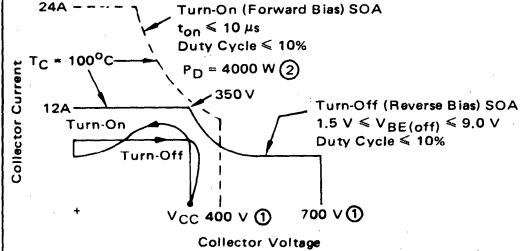
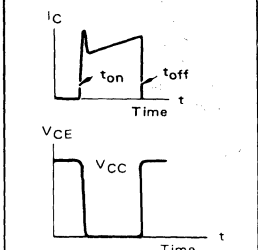
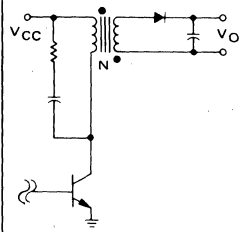
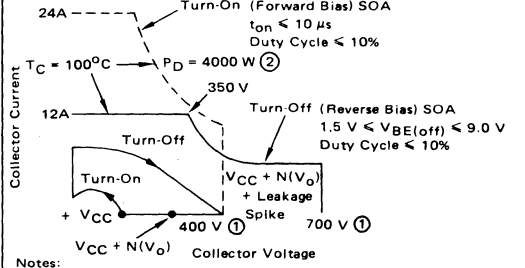
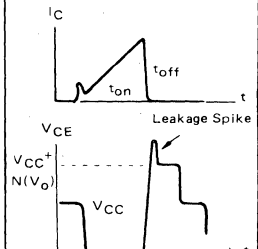
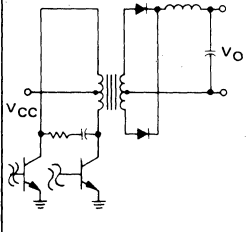
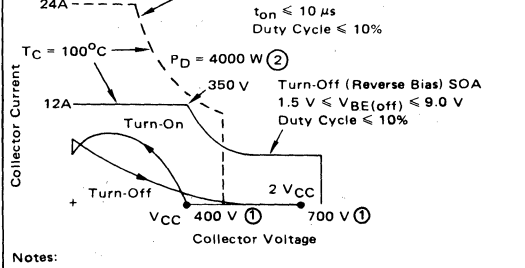
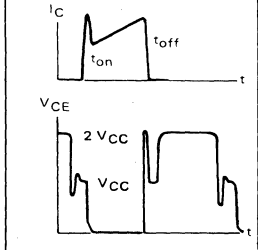
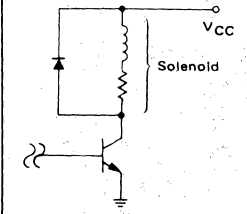
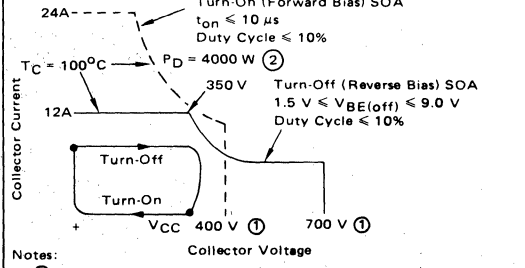
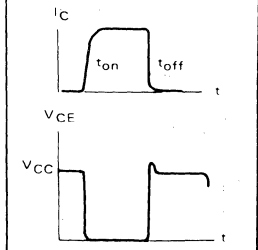


TABLE 2 - APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
<p>SERIES SWITCHING REGULATOR</p>  <p>A</p>	 <p>Notes:</p> <ul style="list-style-type: none"> ① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure. 	
<p>RINGING CHOKE INVERTER</p>  <p>B</p>	 <p>Notes:</p> <ul style="list-style-type: none"> ① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure 	
<p>PUSH-PULL INVERTER/CONVERTER</p>  <p>C</p>	 <p>Notes:</p> <ul style="list-style-type: none"> ① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure. 	
<p>SOLENOID DRIVER</p>  <p>D</p>	 <p>Notes:</p> <ul style="list-style-type: none"> ① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure. 	

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TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I _C AMP	T _C °C	t _{sv} ns	t _{rv} ns	t _{fi} ns	t _{ti} ns	t _c ns
3	25	770	100	150	200	240
	100	1000	230	160	200	320
5	25	630	72	26	10	100
	100	820	100	55	30	180
8	25	720	55	27	2	77
	100	920	70	50	8	120
12	25	640	20	17	2	41
	100	800	32	24	4	54

NOTE: All Data recorded in the inductive switching circuit in Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
- t_{fi} = Current Fall Time, 90–10% I_{CM}
- t_{ti} = Current Tail, 10–2% I_{CM}
- t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

Typical inductive switching waveforms are shown in Figure 14. In general, t_{rv} + t_{fi} ≈ t_c. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

SWITCHMODE II SERIES NPN SILICON POWER TRANSISTORS

The MJE13070 and MJE13071 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

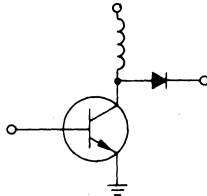
Fast Turn-Off Times

- 100 ns Inductive Fall Time @ 25°C (Typ)
- 150 ns Inductive Crossover Time @ 25°C (Typ)
- 400 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range -65 to +150°C

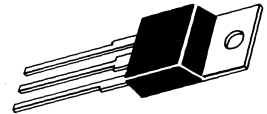
100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



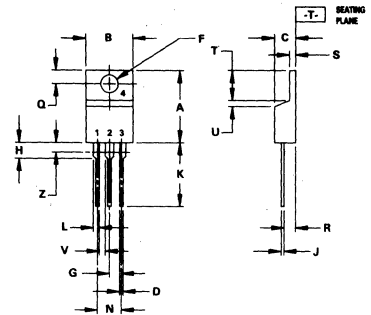
MJE13070 MJE13071

**5 AMPERE
NPN SILICON
POWER TRANSISTORS**
400 AND 450 VOLTS
80 WATTS



Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.62	0.160	0.190
D	0.84	0.98	0.025	0.035
E	3.81	3.72	0.142	0.147
F	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
O	2.54	3.04	0.100	0.120
Q	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.90	1.27	0.060	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1: BASE
2: COLLECTOR
3: EMITTER
4: COLLECTOR

CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MJE13070	MJE13071	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	750	Vdc
Emitter Base Voltage	V_{EB}		6.0	Vdc
Collector Current — Continuous	I_C		5.0	Adc
— Peak (1)	I_{CM}		8.0	
Base Current — Continuous	I_B		2.0	Adc
— Peak (1)	I_{BM}		4.0	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D		80	Watts
Derate above 25°C @ $T_C = 100^\circ\text{C}$			32	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

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MJE13070, MJE13071

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (1)

Collector-Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0)	MJE13070 MJE13071 V _{CEO(sus)}	400 450	— —	— —	V _{dc}
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 V _{dc}) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 V _{dc} , T _C = 100°C)	I _{CEV}	— —	— —	0.5 2.5	mAdc
Collector Cutoff Current (V _{CE} = Rated V _{CEV} , R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V _{EB} = 6.0 V _{dc} , I _C = 0)	I _{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 3.0 Adc, V _{CE} = 5.0 V _{dc})	h _{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage (I _C = 3.0 Adc, I _B = 0.6 Adc) (I _C = 5.0 Adc, I _B = 1.0 Adc) (I _C = 3.0 Adc, I _B = 0.6 Adc, T _C = 100°C)	V _{CE(sat)}	— — —	— — —	1.0 3.0 2.0	V _{dc}
Base-Emitter Saturation Voltage (I _C = 3.0 Adc, I _B = 0.6 Adc) (I _C = 3.0 Adc, I _B = 0.6 Adc, T _C = 100°C)	V _{BE(sat)}	— —	— —	1.5 1.5	V _{dc}

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f _{test} = 1.0 kHz)	C _{ob}	—	—	250	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 250 V _{dc} , I _C = 3.0 Adc, I _{B1} = 0.4 Adc, t _p = 30 μs, Duty Cycle ≤ 2%, V _{BE(off)} = 5.0 V _{dc})	t _d	—	0.03	0.05	μs
Rise Time		t _r	—	0.10	0.40	
Storage Time		t _s	—	0.40	1.50	
Fall Time		t _f	—	0.175	0.50	

Inductive Load, Clamped (Table 1)

Storage Time	(I _{C(pk)} = 3.0 A, I _{B1} = 0.4 Adc, V _{BE(off)} = 5.0 V _{dc} , V _{CE(pk)} = 250 V)	(T _J = 100°C)	t _{sv}	—	0.70	2.0	μs
Crossover Time			t _c	—	0.28	0.50	
Fall Time	(T _J = 25°C)	t _{fi}	—	0.15	0.30		
Storage Time		t _{sv}	—	0.40	—		
Crossover Time		t _c	—	0.15	—		
Fall Time			t _{fi}	—	0.10	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

$$\beta_f = \frac{I_C}{I_B}$$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

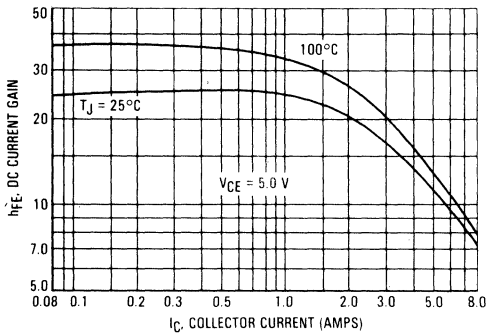


FIGURE 2 — COLLECTOR SATURATION REGION

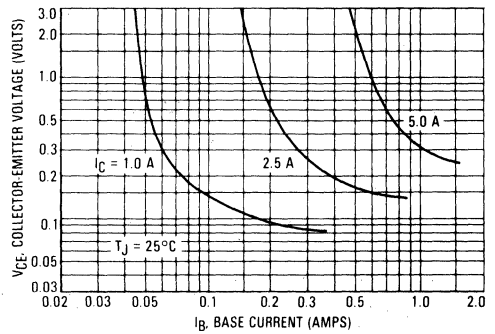


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

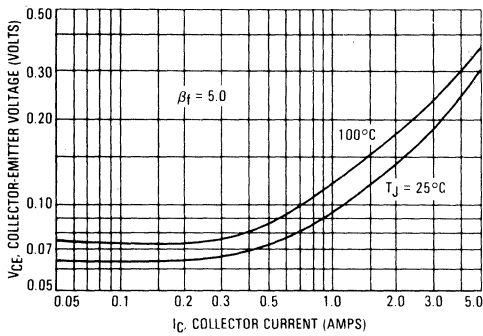


FIGURE 4 — BASE-EMITTER VOLTAGE

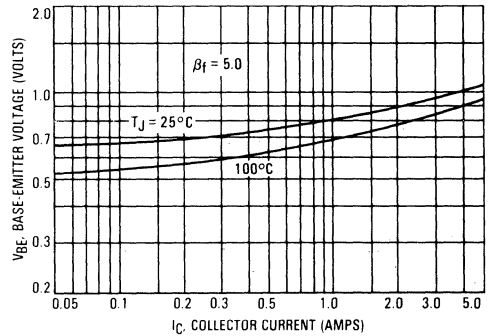


FIGURE 5 — COLLECTOR CUTOFF REGION

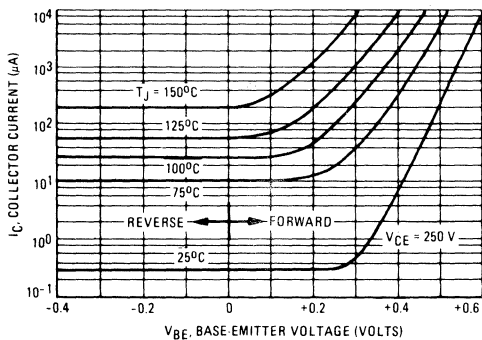


FIGURE 6 — CAPACITANCE

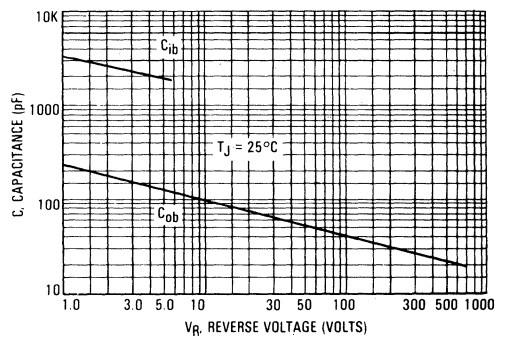


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V _{CE0(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain I_C = 100 mA</p>	<p>Adjust R_{B1} to obtain I_{B1} For switching and R_{BSOA}, R₂ = 0 For BV_{CE0(sus)}, R₂ = ∞</p>	<p>TURN ON TIME I_{B1}</p> <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	L _{coil} = 80 mH V _{CC} = 10 V R _{coil} = 0.7 Ω	L _{coil} = 180 μH R _{coil} = 0.05 Ω V _{CC} = 20 V V _{clamp} = 250 V R _{B1} adjusted to attain desired I _{B1}	V _{CC} = 250 V R _L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>See Above for Detailed Conditions</p>	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ <p>Test Equipment Scope – Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>



FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

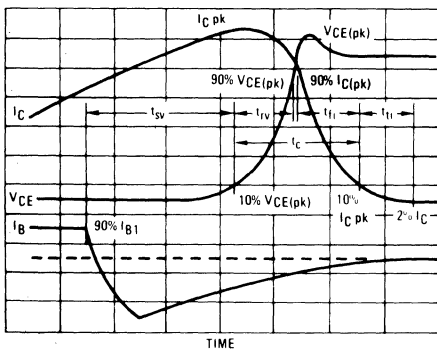
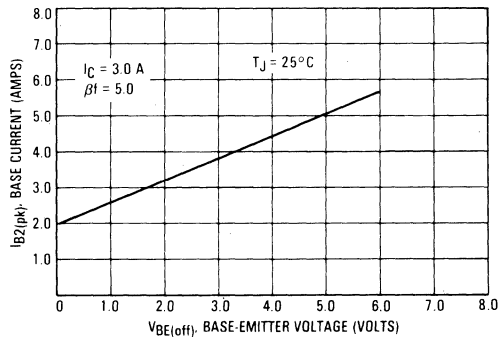


FIGURE 8 – PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms

is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

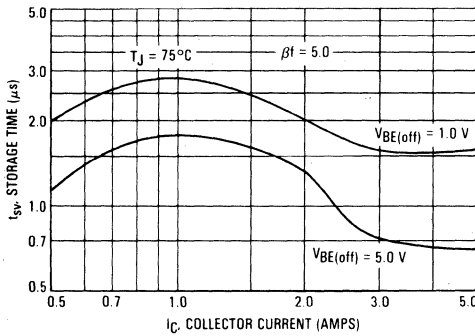


FIGURE 10 — CROSSOVER AND FALL TIMES

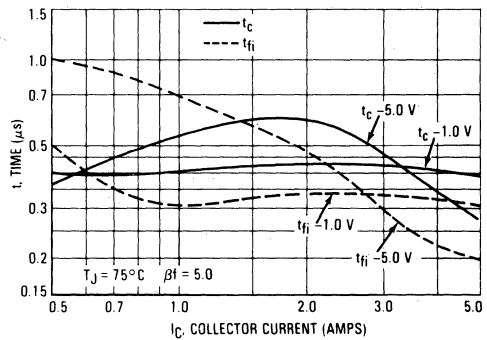
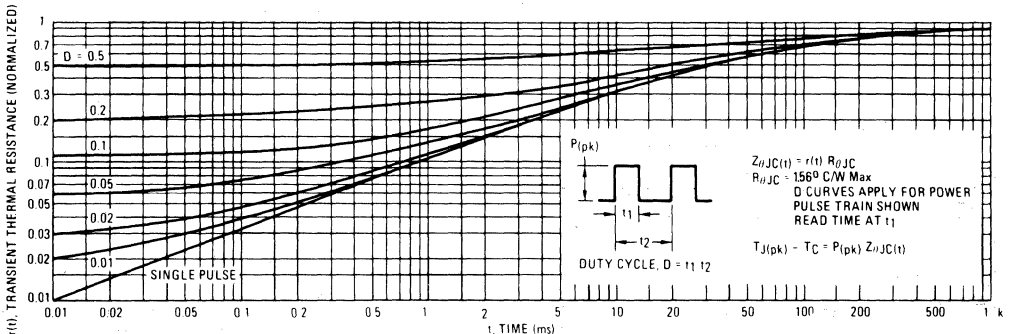


FIGURE 11 — THERMAL RESPONSE



3

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA

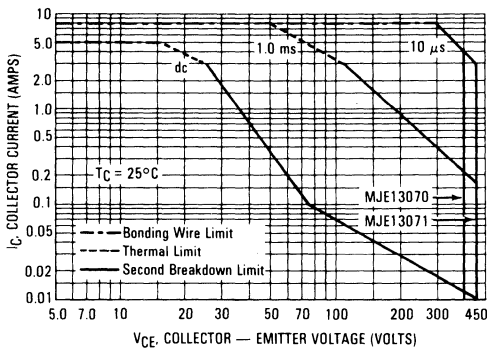


FIGURE 13 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

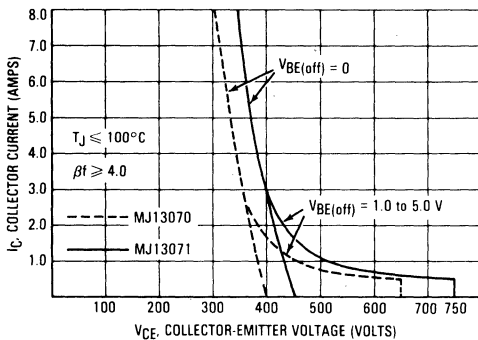
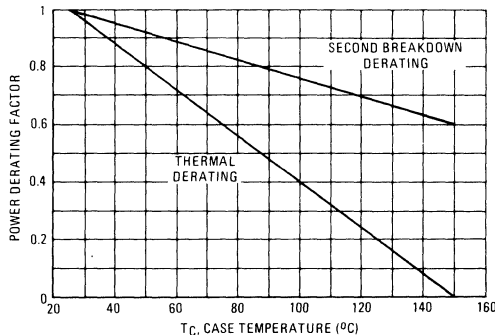


FIGURE 14 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

NPN **PNP**
MJE15028 **MJE15029**
MJE15030 **MJE15031**

**COMPLEMENTARY SILICON PLASTIC
POWER TRANSISTORS**

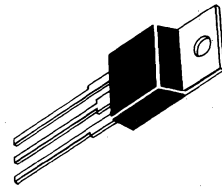
... designed for use as high-frequency drivers in audio amplifiers.

- DC Current Gain Specified to 4.0 Amperes
 $h_{FE} = 40(\text{Min}) @ I_C = 3.0 \text{ Adc}$
 $= 20(\text{Min}) @ I_C = 4.0 \text{ Adc}$
- Collector-Emitter Sustaining Voltage –
 $V_{CE(sus)} = 120 \text{ Vdc (Min)} - \text{MJE15028, MJE15029}$
 $= 150 \text{ Vdc (Min)} - \text{MJE15030, MJE15031}$
- High Current Gain – Bandwidth Product
 $f_T = 30 \text{ MHz (Min)} @ I_C = 500 \text{ mAdc}$
- TO-220AB Compact Package
- TO-66 Leadform Also Available

8 AMPERE

**POWER TRANSISTORS
COMPLEMENTARY SILICON**

**120-150 VOLTS
50 WATTS**



MAXIMUM RATINGS

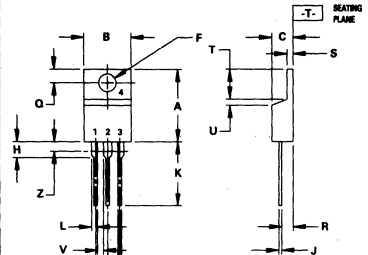
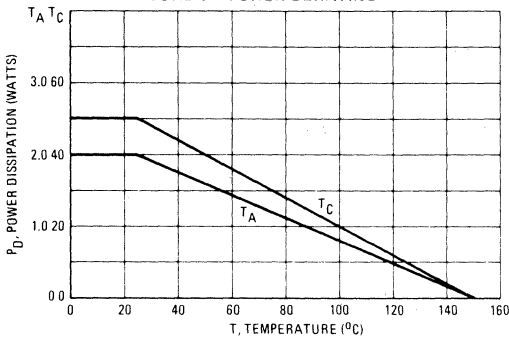
Rating	Symbol	MJE15028 MJE15029	MJE15030 MJE15031	Unit
Collector-Emitter Voltage	V_{CEO}	120	150	Vdc
Collector-Base Voltage	V_{CB}	120	150	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →		Vdc
Collector Current – Continuous – Peak	I_C	← 8.0 → ← 16 →		Adc
Base Current	I_B	← 2.0 →		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 50 → ← 0.40 →		Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	← 2.0 → ← 0.016 →		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

3

FIGURE 1 – POWER DERATING



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.98	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
O	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

**CASE 221A-04
TO-220AB**

NPN MJE15028, MJE15030
PNP MJE15029, MJE15031

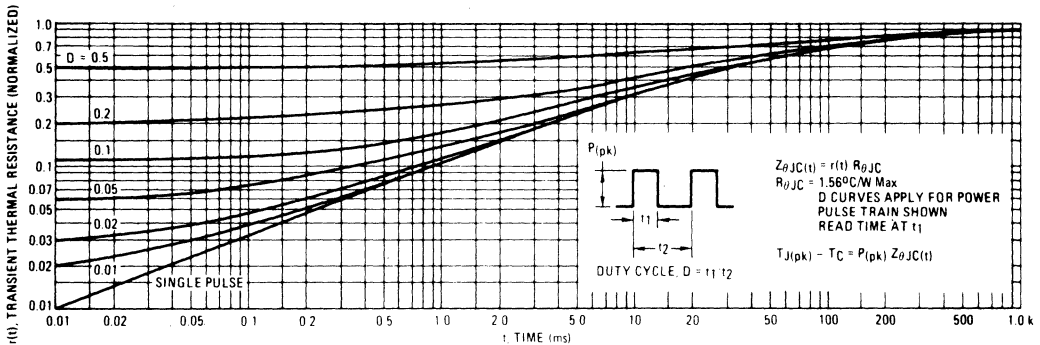
ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 10 \text{ mAdc}$, $I_B = 0$)	MJE15028, MJE15029 MJE15030, MJE15031	$V_{CE(sus)}$	120 150	– –	Vdc
Collector Cutoff Current ($V_{CE} = 120 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 150 \text{ Vdc}$, $I_B = 0$)	MJE15028, MJE15029 MJE15030, MJE15031	I_{CEO}	– –	0.1 0.1	mAdc
Collector Cutoff Current ($V_{CB} = 120 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 150 \text{ Vdc}$, $I_E = 0$)	MJE15028, MJE15029 MJE15030, MJE15031	I_{CBO}	– –	10 10	μAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)		I_{EBO}	–	10	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 0.1 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 2.0 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$) ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$)		h_{FE}	40 40 40 20	– – – –	–
DC Current Gain Linearity (V_{CE} From 2.0V to 20V, I_C From 0.1A to 3A) (NPN TO PNP)		h_{FE}		Typ 2 3	
Collector-Emitter Saturation Voltage ($I_C = 1.0 \text{ Adc}$, $I_B = 0.1 \text{ Adc}$)		$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter On Voltage ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 2.0 \text{ Vdc}$)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 10 \text{ MHz}$)		f_T	30	–	MHz

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

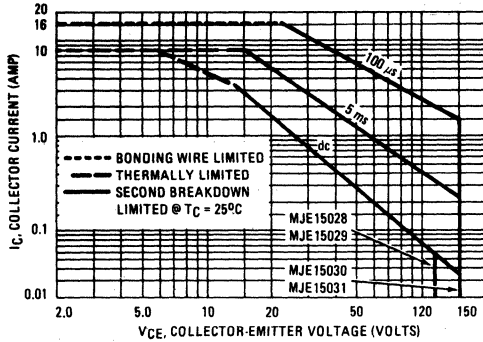
(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – THERMAL RESPONSE



NPN MJE15028, MJE15030
PNP MJE15029, MJE15031

FIGURE 3 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 – REVERSE-BIAS SWITCHING SAFE OPERATING AREA

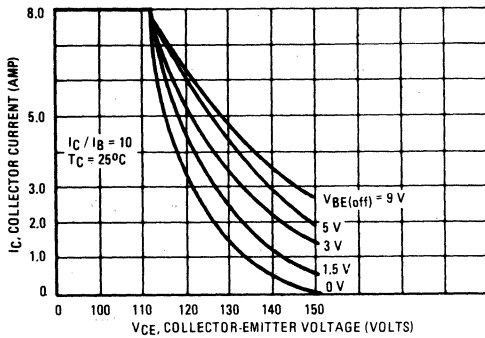


FIGURE 5 – CAPACITANCES

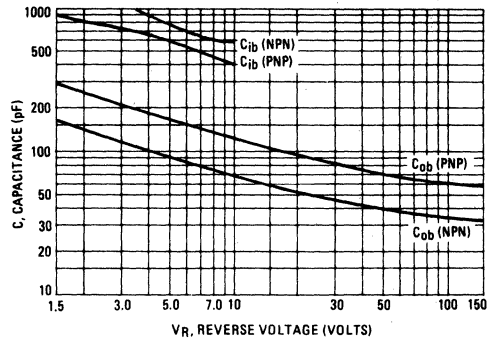


FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

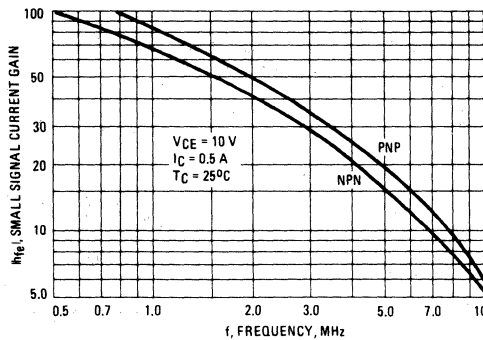
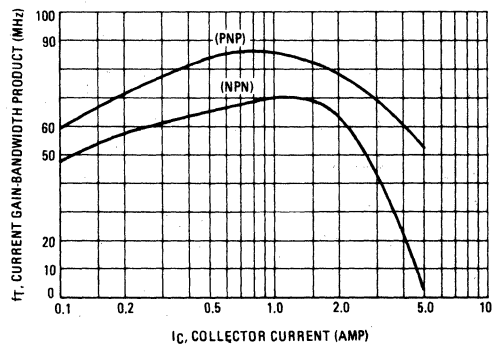


FIGURE 7 – CURRENT GAIN-BANDWIDTH PRODUCT



3

NPN MJE15028, MJE15030
PNP MJE15029, MJE15031

FIGURE 8 – DC CURRENT GAIN

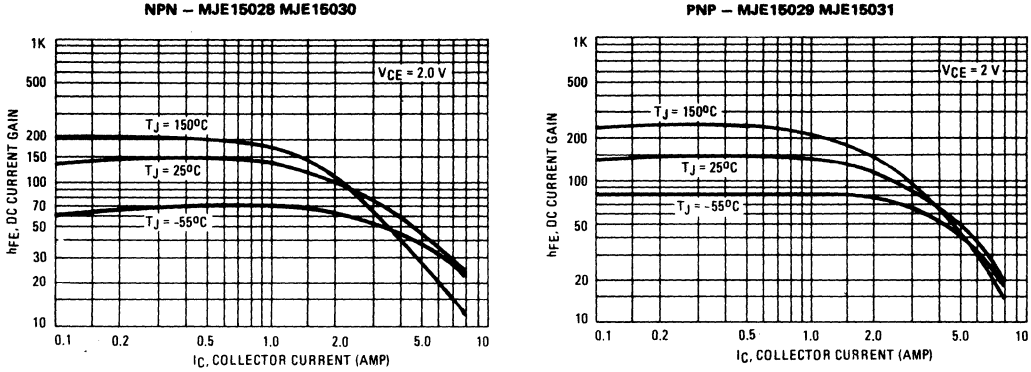


FIGURE 9 – "ON" VOLTAGE

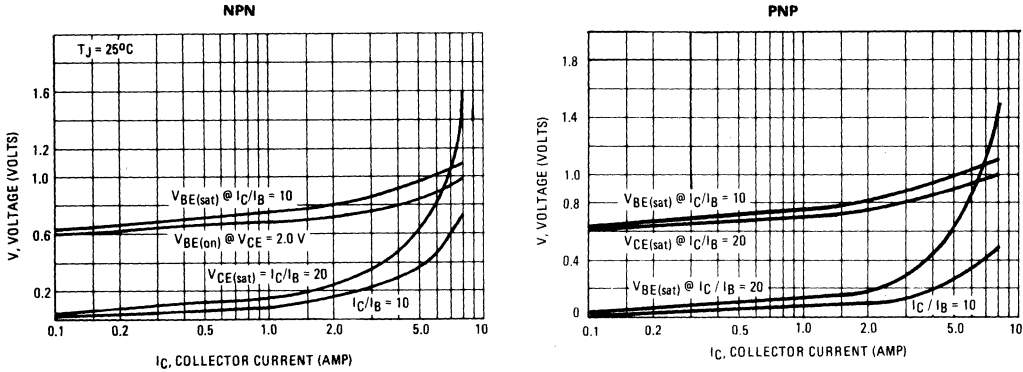


FIGURE 10 – TURN-ON TIMES

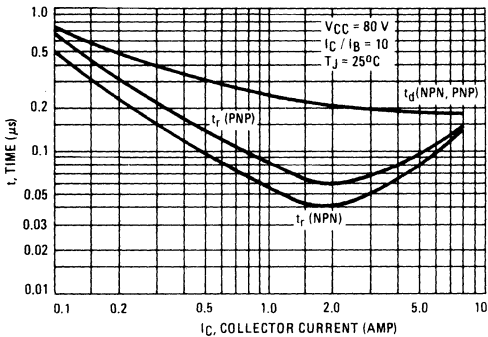
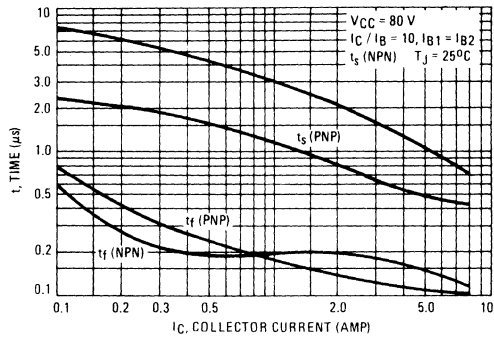


FIGURE 11 – TURN-OFF TIMES



MJE16002
MJE16004
MJH16002
MJH16004

Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed switching of inductive circuits where fall time and RBSOA are critical. They are particularly well-suited for line-operated switch-mode applications.

The MJE16004 and MJH16004 are high-gain versions of the MJE16002 and MJH16002 for applications where drive current is limited.

Typical Applications:

- Switching Regulators
- High Resolution Deflection Circuits
- Inverters
- Motor Drives
- Fast Switching Speeds
 - 50 ns Inductive Fall Time @ 75°C (Typ)
 - 70 ns Crossover Time @ 75°C (Typ)
- 100°C Performance Specified for:
 - Reverse-Biased SOA
 - Inductive Switching Times
 - Saturation Voltages
 - Leakage Currents

MAXIMUM RATINGS

Rating	Symbol	MJE16002 MJE16004	MJH16002 MJH16004	Unit
Collector-Emitter Voltage	V _{CEO(sus)}	450		Vdc
Collector-Emitter Voltage	V _{CEV}	850		Vdc
Emitter-Base Voltage	V _{EB}	6.0		Vdc
Collector Current — Continuous	I _C	5.0		Adc
— Peak (1)	I _{CM}	10		
Base Current — Continuous	I _B	4.0		Adc
— Peak (1)	I _{BM}	8.0		
Total Power Dissipation @ T _C = 25°C	P _D	80	100	Watts
Derate above T _C = 25°C		32	40	
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.56	1.25	°C/W
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

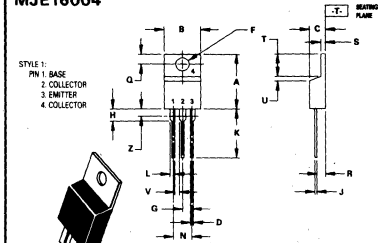
Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

5.0 AMPERE
NPN SILICON
POWER TRANSISTORS

450 VOLTS
80 and 100 WATTS

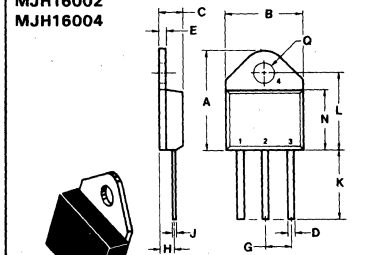
MJE16002
MJE16004



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.46	15.75	0.570	0.600
B	3.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.94	0.98	0.037	0.039
F	3.81	3.73	0.147	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.30	0.110	0.130
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.560
L	1.15	1.38	0.045	0.055
N	4.82	5.20	0.190	0.205
O	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.38	0.045	0.055
T	5.07	6.41	0.200	0.250
U	0.60	1.27	0.024	0.050
V	1.18	—	0.046	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MJH16002
MJH16004



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.95	0.053	0.076
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
O	4.04	4.22	0.158	0.166

CASE 340-01
TO-218AC

MJE16002, MJE16004, MJH16002, MJH16004

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS (1)

Collector-Emitter Sustaining Voltage (Table 2) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	450	—	—	Vdc
Collector Cutoff Current (V _{CEV} = 850 Vdc, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = 850 Vdc, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	—	—	0.25 1.5	mAdc
Collector Cutoff Current (V _{CE} = 850 Vdc, R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V _{EB} = 6.0 Vdc, I _C = 0)	I _{EBO}	—	—	1.0	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}		See Figure 17 or 18		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 19		

ON CHARACTERISTICS (1)

Collector-Emitter Saturation Voltage (I _C = 1.5 Adc, I _B = 0.2 Adc) MJE16002/MJH16002 (I _C = 1.5 Adc, I _B = 0.15 Adc) MJE16004/MJH16004 (I _C = 3.0 Adc, I _B = 0.4 Adc) MJE16002/MJH16002 (I _C = 3.0 Adc, I _B = 0.3 Adc) MJE16004/MJH16004 (I _C = 3.0 Adc, I _B = 0.4 Adc, T _C = 100°C) MJE16002/MJH16002 (I _C = 3.0 Adc, I _B = 0.3 Adc, T _C = 100°C) MJE16004/MJH16004	V _{CE(sat)}	—	—	1.0 1.0 2.5 2.5 2.5 2.5	Vdc
Base-Emitter Saturation Voltage (I _C = 3.0 Adc, I _B = 0.4 Adc) MJE16002/MJH16002 (I _C = 3.0 Adc, I _B = 0.3 Adc) MJE16004/MJH16004 (I _C = 3.0 Adc, I _B = 0.4 Adc, T _C = 100°C) MJE16002/MJH16002 (I _C = 3.0 Adc, I _B = 0.3 Adc, T _C = 100°C) MJE16004/MJH16004	V _{BE(sat)}	—	—	1.5 1.5 1.5 1.5	Vdc
DC Current Gain (I _C = 5.0 Adc, V _{CE} = 5.0 Vdc) MJE16002/MJH16002 MJE16004/MJH16004	h _{FE}	5.0 7.0	—	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1.0 kHz)	C _{ob}	—	—	200	pF
---	-----------------	---	---	-----	----

SWITCHING CHARACTERISTICS

Resistive Load (Table 1) MJE16002/MJH16002							
Delay Time	(I _C = 3.0 Adc, V _{CC} = 250 Vdc, I _{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I _{B2} = 0.8 Adc, R _{B2} = 8.0 Ω)	t _d	—	30	100	ns
Rise Time			t _r	—	100	300	
Storage Time			t _s	—	1000	3000	
Fall Time			t _f	—	60	300	
Storage Time			t _s	—	400	—	
Fall Time			t _f	—	130	—	
Resistive Load (Table 1) MJE16004/MJH16004							
Delay Time	(I _C = 3.0 Adc, V _{CC} = 250 Vdc, I _{B1} = 0.3 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I _{B2} = 0.6 Adc, R _{B2} = 8.0 Ω)	t _d	—	30	100	ns
Rise Time			t _r	—	130	300	
Storage Time			t _s	—	800	2700	
Fall Time			t _f	—	80	350	
Storage Time			t _s	—	250	—	
Fall Time			t _f	—	60	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

*β_{eff} = I_C / I_{B1}

SWITCHING CHARACTERISTICS (continued)

Characteristics		Symbol	Min	Typ	Max	Unit	
Inductive Load (Table 2) MJE16002/MJH16002							
Storage Time	$I_C = 3.0 \text{ Adc}$, $I_{B1} = 0.4 \text{ Adc}$	$(T_J = 100^\circ\text{C})$	t_{sv}	—	500	1600	ns
Fall Time			t_{fi}	—	100	200	
Crossover Time			t_c	—	120	250	
Storage Time	$V_{BE(off)} = 5.0 \text{ Vdc}$, $V_{CE(pk)} = 400 \text{ Vdc}$	$(T_J = 150^\circ\text{C})$	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	
Inductive Load (Table 2) MJE16004/MJH16004							
Storage Time	$I_C = 3.0 \text{ Adc}$, $I_{B1} = 0.3 \text{ Adc}$	$(T_J = 100^\circ\text{C})$	t_{sv}	—	400	1300	ns
Fall Time			t_{fi}	—	80	150	
Crossover Time			t_c	—	90	200	
Storage Time	$V_{BE(off)} = 5.0 \text{ Vdc}$, $V_{CE(pk)} = 400 \text{ Vdc}$	$(T_J = 150^\circ\text{C})$	t_{sv}	—	450	—	
Fall Time			t_{fi}	—	100	—	
Crossover Time			t_c	—	110	—	

(1) Pulse Test: PW - 300 μs , Duty Cycle $\leq 2\%$.

$\beta_f = \frac{I_C}{I_{B1}}$

FIGURE 1 — DC CURRENT GAIN

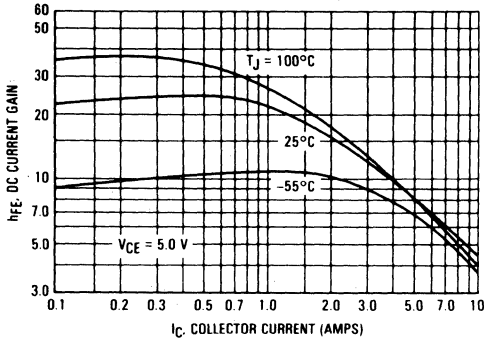


FIGURE 2 — COLLECTOR SATURATION REGION

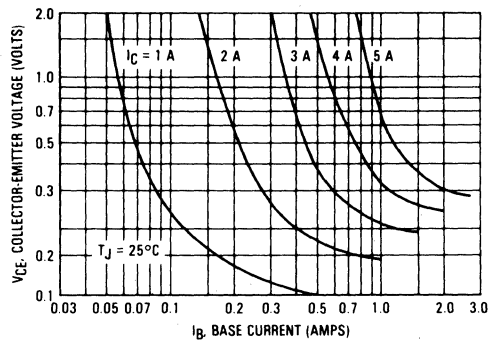


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

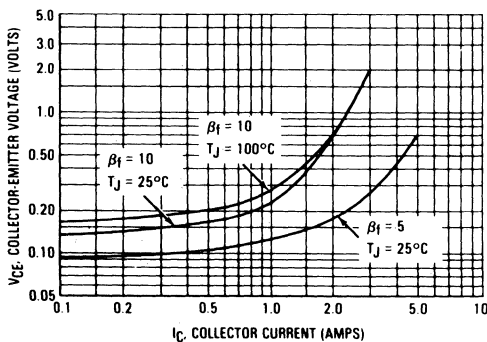
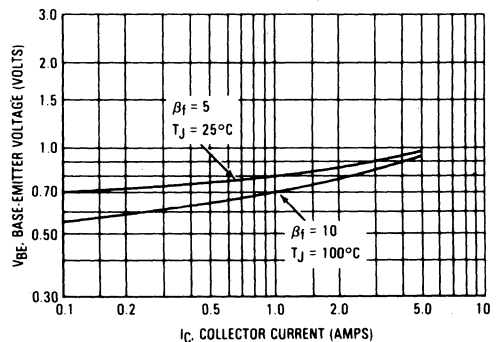


FIGURE 4 — BASE-EMITTER VOLTAGE



TYPICAL STATIC CHARACTERISTICS (continued)

FIGURE 5 — COLLECTOR CUTOFF REGION

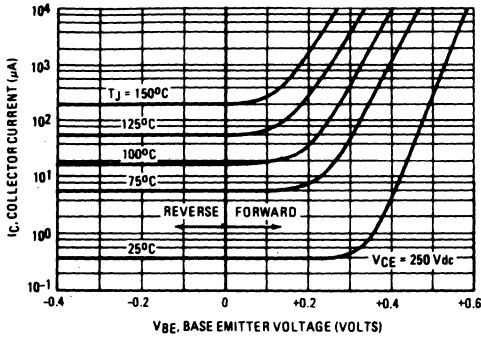
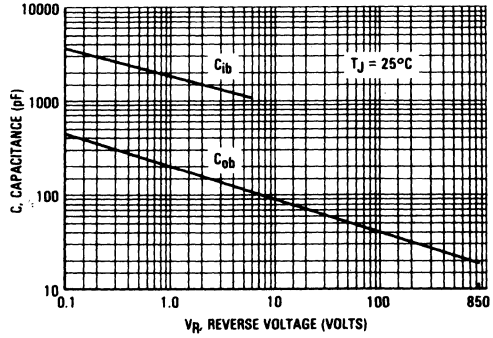


FIGURE 6 — CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 — STORAGE TIME

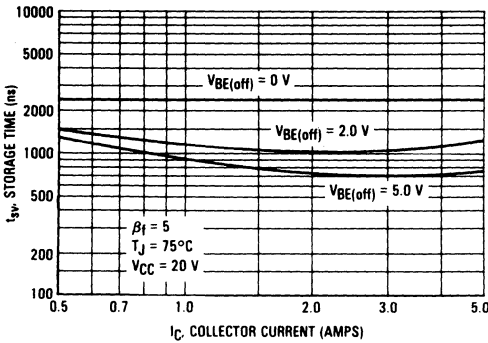


FIGURE 8 — STORAGE TIME

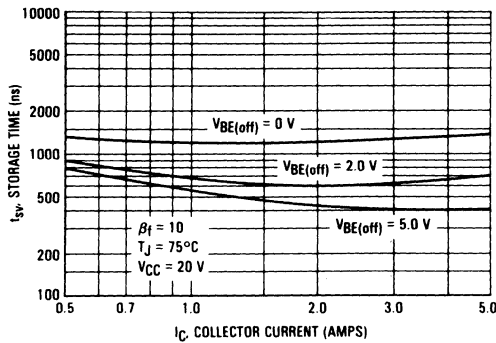


FIGURE 9 — COLLECTOR CURRENT FALL TIME

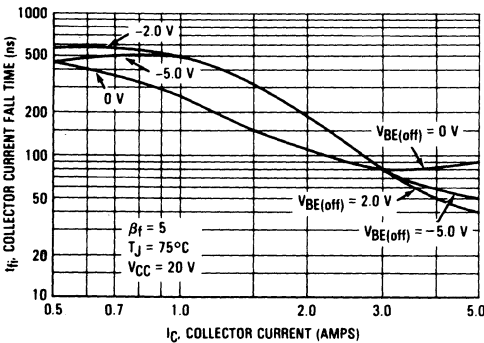
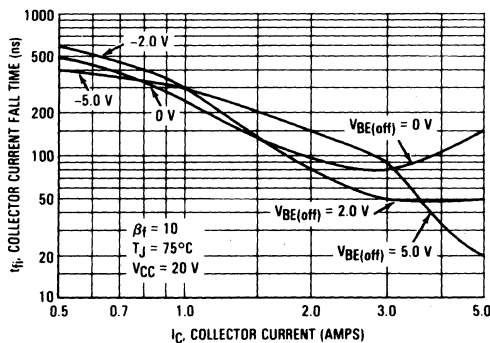


FIGURE 10 — COLLECTOR CURRENT FALL TIME



TYPICAL DYNAMIC CHARACTERISTICS (continued)

FIGURE 11 — CROSSOVER TIME

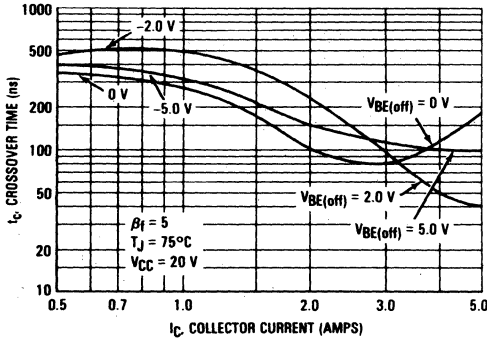
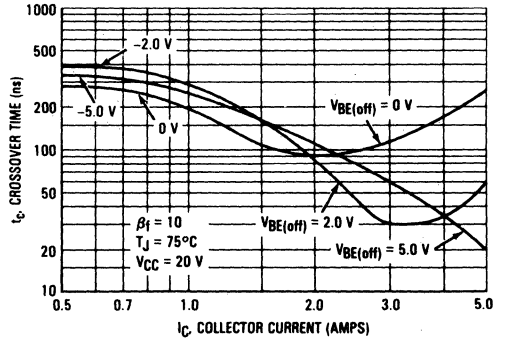


FIGURE 12 — CROSSOVER TIME



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

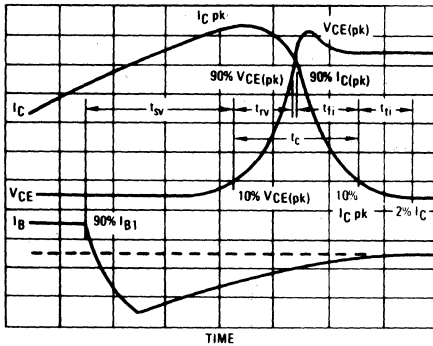


FIGURE 14 — PEAK REVERSE BASE CURRENT

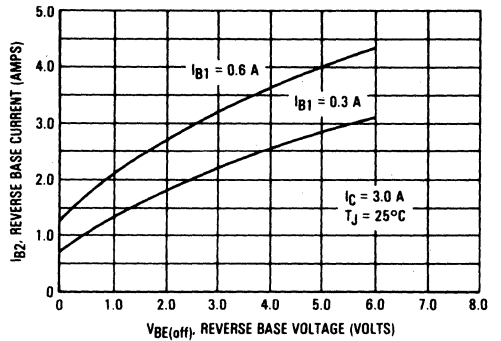
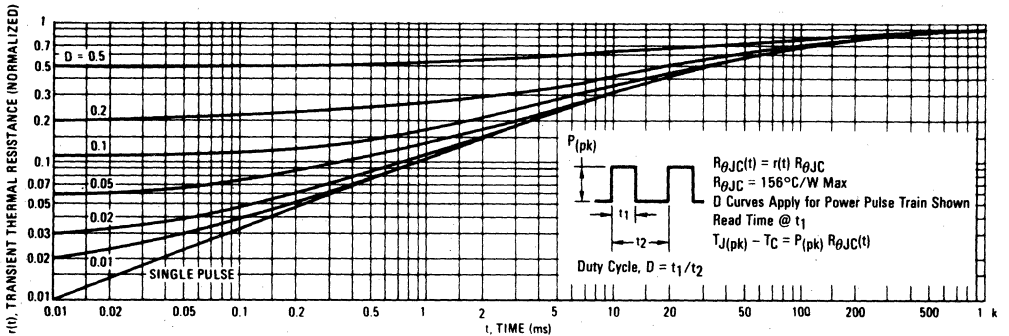


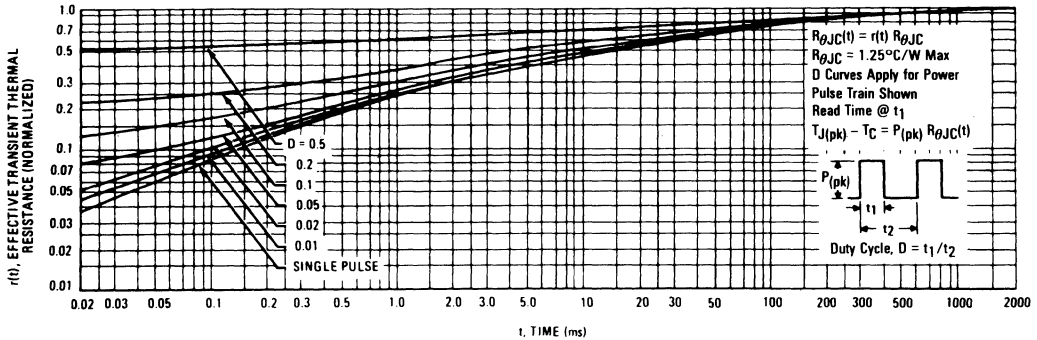
FIGURE 15 — THERMAL RESPONSE (MJE16002 and MJE16004)



3

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 16 — THERMAL RESPONSE (MJH16002 and MJH16004)



SAFE OPERATING AREA INFORMATION

FIGURE 17 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (MJE16002 and MJE16004)

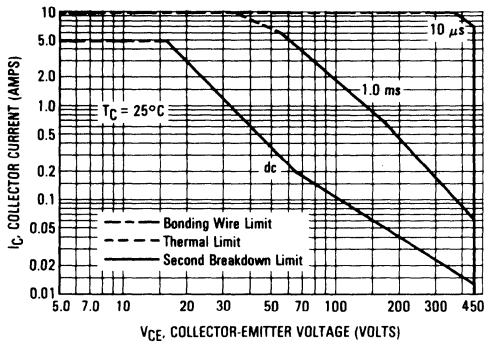


FIGURE 18 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (MJH16002 and MJH16004)

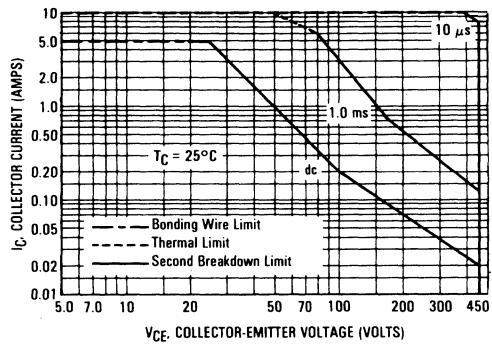


FIGURE 19 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

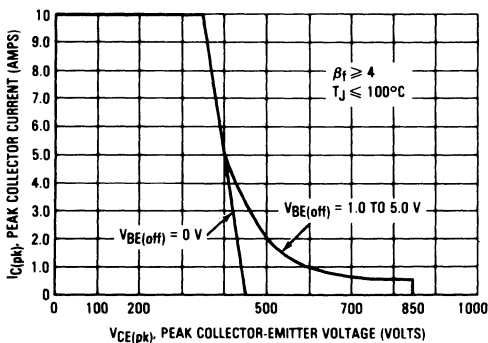
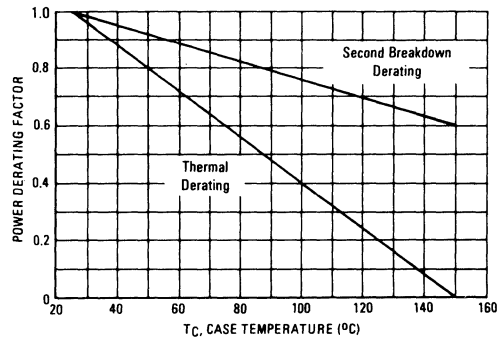


FIGURE 20 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 17 and 18 are based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 17 and 18 may be found at any case temperature by using the appropriate curve on Figure 20.

$T_{J(pk)}$ may be calculated from the data in Figures 15 or 16. At high case temperatures, thermal limitations will

reduce the power that can be handled to values less than the limitations imposed by second breakdown.

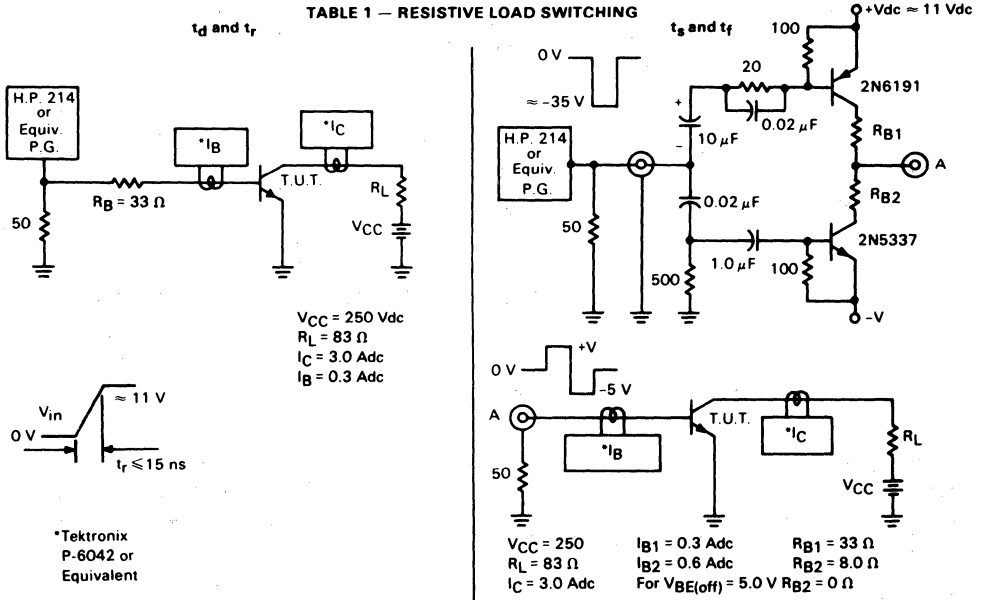
REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneous during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable putting reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 19 gives the RBSOA characteristics.

3

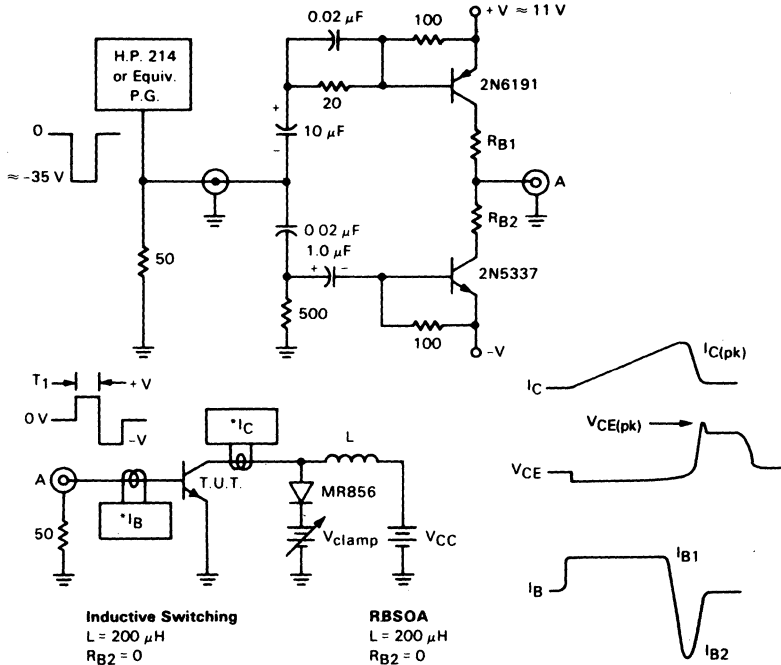
t_d and t_r

TABLE 1 — RESISTIVE LOAD SWITCHING



*Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TABLE 2 — INDUCTIVE LOAD SWITCHING



$$T_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

BV_{CEO}
 $L = 10 \text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20 \text{ Volts}$

Inductive Switching
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

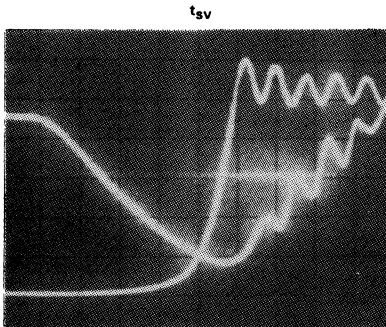
RBSOA
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

*Tektronix
 P-6042 or
 Equivalent

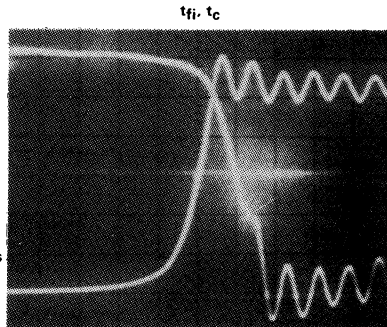
Scope - Tektronix
 7403 or
 Equivalent

Note: Adjust -V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS



$I_{C(pk)} = 3.0 \text{ Amps}$
 $I_{B1} = 0.3 \text{ Amp}$
 $V_{BE(off)} = 5.0 \text{ Volts}$
 $V_{CE(pk)} = 300 \text{ Volts}$
 $T_C = 25^\circ\text{C}$
 Time Base =
 20 ns/cm



$I_{C(pk)} = 3.0 \text{ Amps}$
 $I_{B1} = 0.3 \text{ Amp}$
 $V_{BE(off)} = 5.0 \text{ Volts}$
 $V_{CE(pk)} = 300 \text{ Volts}$
 $T_C = 25^\circ\text{C}$
 Time Base =
 20 ns/cm

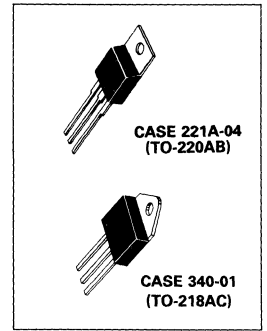
Designer's Data Sheet
NPN Silicon Power Transistors
Switchmode III Series

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 150 ns Inductive Fall Time: 25°C (Typ)
 - 150 ns Inductive Crossover Time: 25°C (Typ)
 - 500 ns Inductive Storage Time: 25°C (Typ)
- Operating Temperature Range: -65 to +150°C
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

MJE16032
MJE16034
MJH16032
MJH16034

POWER TRANSISTORS
3 AMPERES
750 and 850 VOLTS
80 and 125 WATTS



MAXIMUM RATINGS

Rating	Symbol	MJE16032 MJH16032	MJE16034 MJH16034	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	750	850	Vdc
Collector-Emitter Voltage	V_{CEV}	1500		Vdc
Emitter Base Voltage	V_{EB}	9		Vdc
Collector Current — Continuous	I_C	3		Adc
— Peak ⁽¹⁾	I_{CM}	6		
Base Current — Continuous	I_B	2		Adc
— Peak ⁽¹⁾	I_{BM}	4		
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C
		MJE16032 MJE16034	MJH16032 MJH16034	
Total Power Dissipation @ $T_C = +25^\circ\text{C}$	P_D	80	125	Watts
@ $T_C = +100^\circ\text{C}$		32	50	
Derate above 25°C		0.64	1	W/°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

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MJE16032, MJE16034, MJH16032, MJH16034

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	1	$^{\circ}\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275		$^{\circ}\text{C}$

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Table 2) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	750 850	— —	— —	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^{\circ}\text{C}$)	I_{CEV}	— —	0.005 0.020	0.25 2.5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^{\circ}\text{C}$)	I_{CER}	—	0.020	2.5	mAdc
Emitter Cutoff Current ($V_{EB} = 9\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	0.002	0.25	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 17			

ON CHARACTERISTICS(1)

DC Current Gain ($V_{CE} = 5\text{ Vdc}$)	h_{FE}	10 4	15 7	— —	— —
Collector-Emitter Saturation Voltage ($I_C = 1\text{ Adc}$, $I_B = 0.33\text{ Adc}$) ($I_C = 3\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.33\text{ Adc}$, $T_C = 100^{\circ}\text{C}$)	$V_{CE(sat)}$	— — —	0.15 1 0.5	1 2.5 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 1\text{ Adc}$, $I_B = 0.33\text{ Adc}$) ($I_C = 1\text{ Adc}$, $I_B = 0.33\text{ Adc}$, $T_C = 100^{\circ}\text{C}$)	$V_{BE(sat)}$	— —	0.8 0.7	1.5 1.5	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1\text{ MHz}$)	C_{ob}	—	80	—	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)							
Delay Time	$(V_{CC} = 400\text{ Vdc}$, $I_C = 2\text{ A}$ $I_{B1} = 333\text{ mA}$, $V_{BE(off)} = 5\text{ Vdc}$, $t_p = 50\ \mu\text{s}$, Duty Cycle \leq 2%)	t_d	—	0.06	0.2	μs	
Rise Time		t_r	—	0.15	1	μs	
Storage Time		t_s	—	1.5	2	μs	
Fall Time		t_f	—	0.15	1.5	μs	
Inductive Load, Clamped (Table 2)							
Storage Time	$(I_C = 2\text{ A}$, $V_{clamp} = 400\text{ Vdc}$, $V_{BE(off)} = 5\text{ Vdc}$, $I_{B1} = 333\text{ mA}$)	$T_C = 100^{\circ}\text{C}$	t_{sv}	—	0.5	1.5	μs
Crossover Time		$T_C = 25^{\circ}\text{C}$	t_c	—	0.2	1	μs
Storage Time		$T_C = 100^{\circ}\text{C}$	t_{sv}	—	0.5	—	μs
Crossover Time		$T_C = 25^{\circ}\text{C}$	t_c	—	0.15	—	μs
Fall Time			t_{fi}	—	0.15	—	μs

(1) Pulse Test: PW = 300 μs , Duty Cycle \leq 2%.

TYPICAL STATIC CHARACTERISTICS

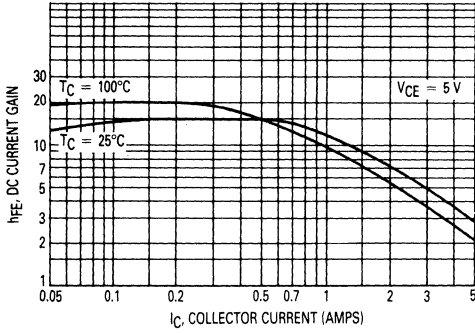


Figure 1. DC Current Gain

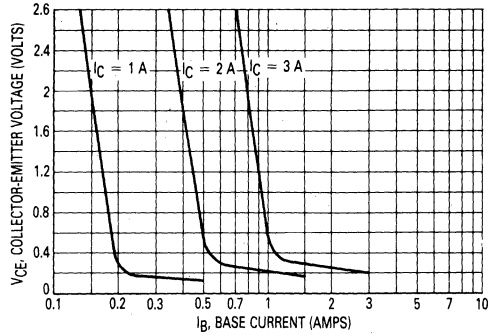


Figure 2. Collector Saturation Region

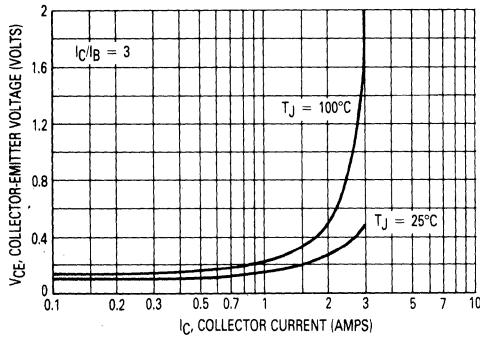


Figure 3. Collector-Emitter Saturation Voltage

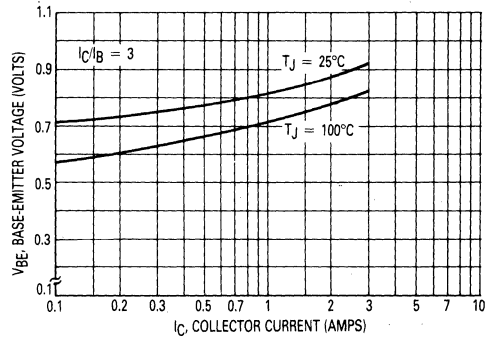


Figure 4. Base-Emitter Saturation Voltage

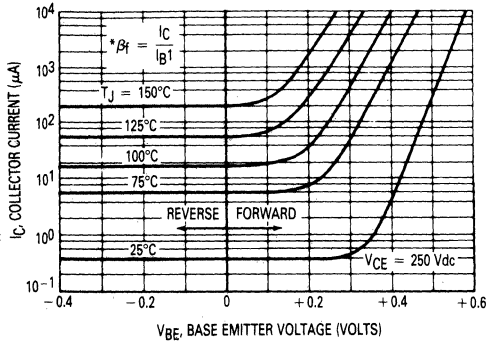


Figure 5. Collector Cutoff Region

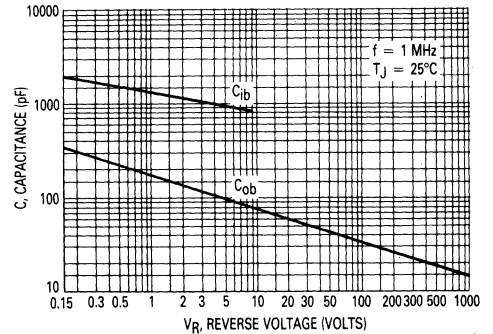


Figure 6. Capacitance Variation

TYPICAL DYNAMIC CHARACTERISTICS

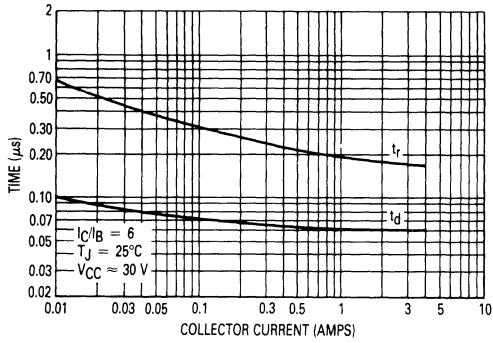


Figure 7. Resistive Turn-On Time

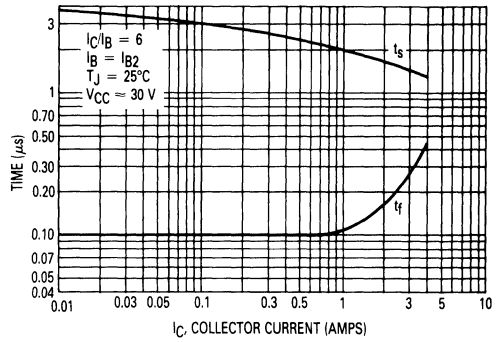


Figure 8. Resistive Turn-Off Time

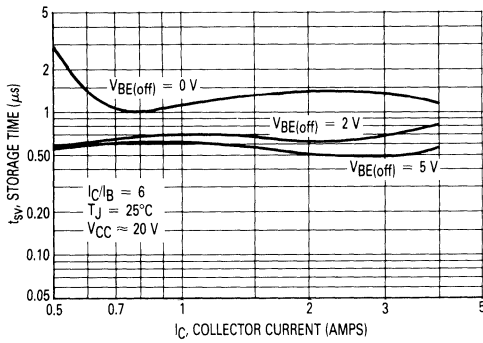


Figure 9. Inductive Storage Time
T_J = 25°C

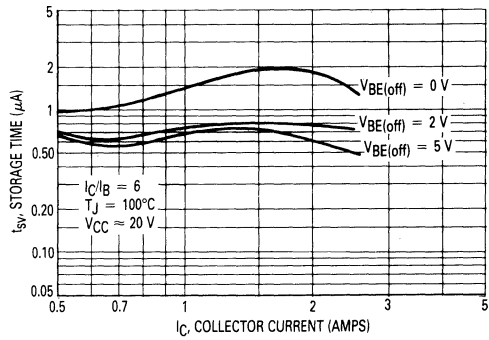


Figure 10. Inductive Storage Time
T_J = 100°C

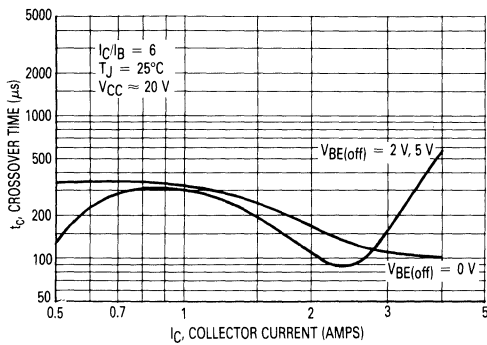


Figure 11. Inductive Crossover Time
T_J = 25°C

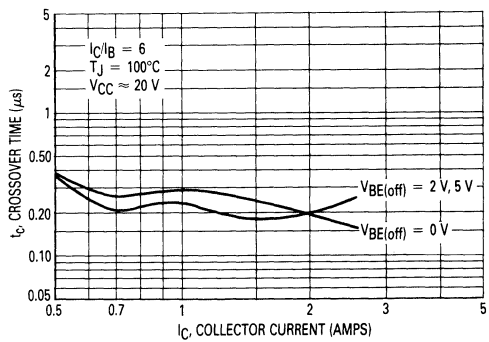


Figure 12. Inductive Crossover Time
T_J = 100°C

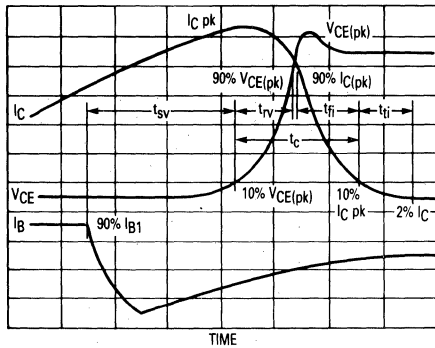


Figure 13. Inductive Switching Measurements

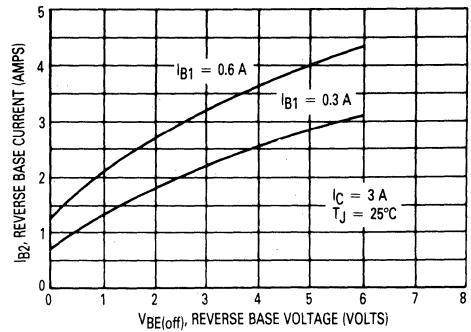
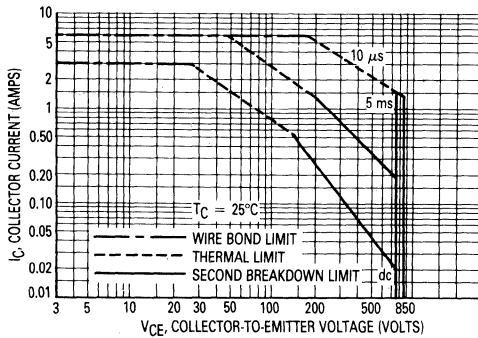
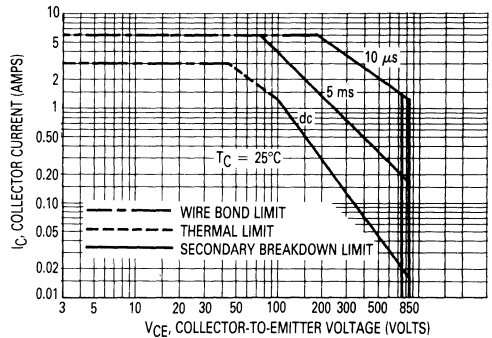


Figure 14. Peak Reverse Base Current

GUARANTEED SAFE OPERATING AREA LIMITS



a. MJE16032, MJE16034



b. MJH16032, MJH16034

Figure 15. Maximum Rated Forward Bias Safe Operating Area

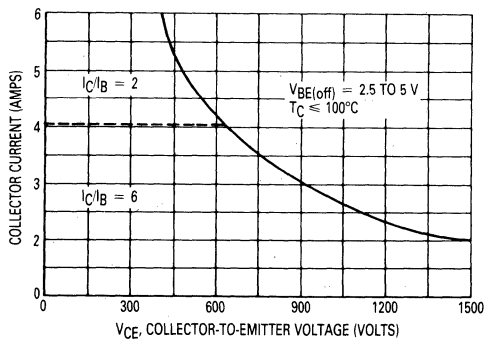


Figure 16. Maximum Rated Reverse Bias Safe Operating Area

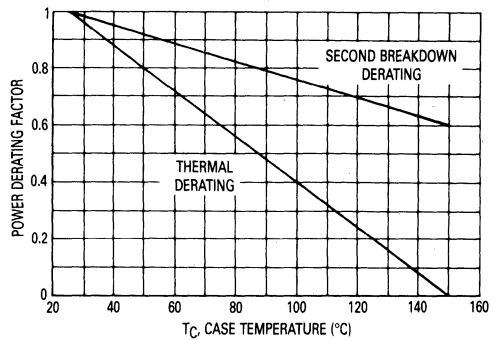


Figure 17. Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will re-

duce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

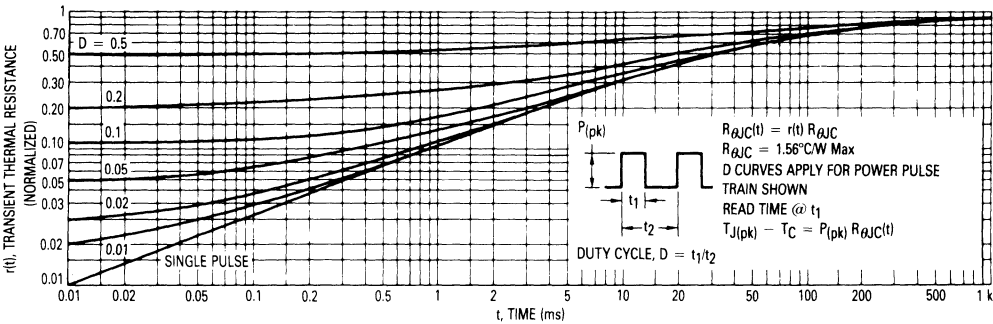
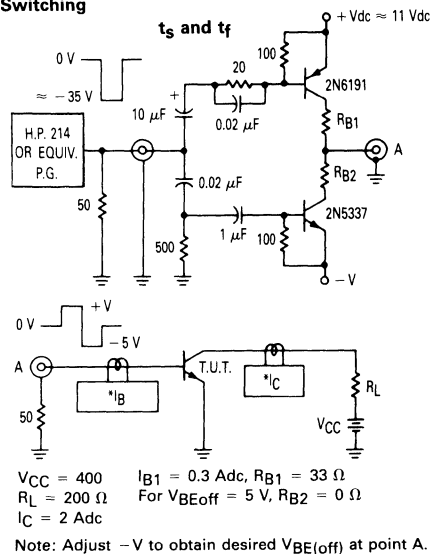
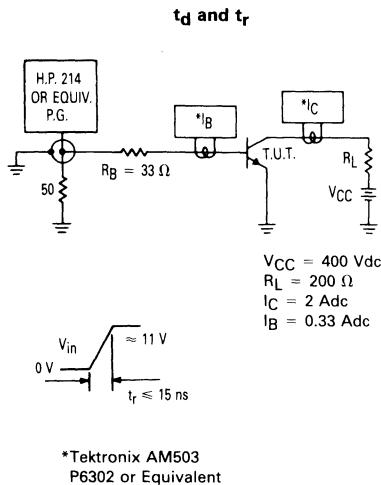


Figure 18. Thermal Response

Table 1. Resistive Load Switching

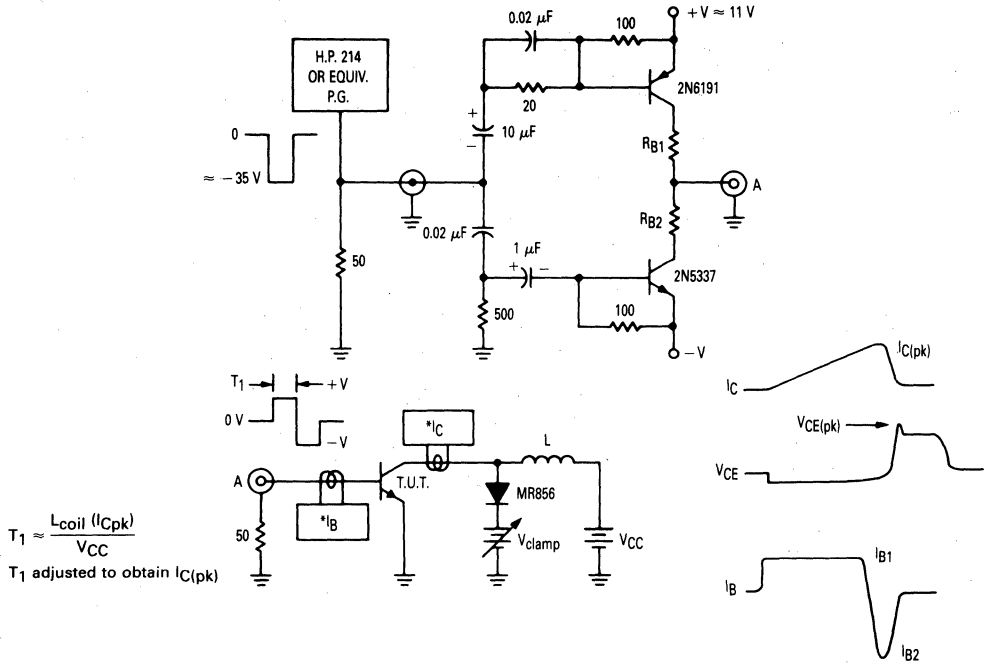


*Tektronix AM503 P6302 or Equivalent

Note: Adjust $-V$ to obtain desired $V_{BE(off)}$ at point A.



Table 2. Inductive Load Switching



V(BR)CEO
 $L = 10 \text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20 \text{ Volts}$

*Tektronix
 AM503
 P6302 or Equivalent

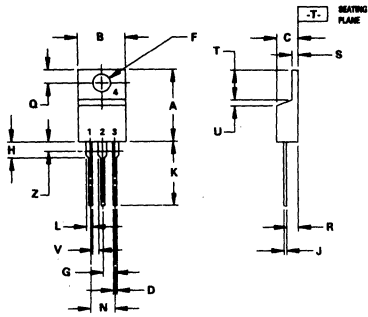
Inductive Switching
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

Scope — Tektronix
 7403 or
 Equivalent

RBSOA
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 20 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

Note: Adjust $-V$ to obtain desired $V_{BE(off)}$ at Point A.

OUTLINE DIMENSIONS

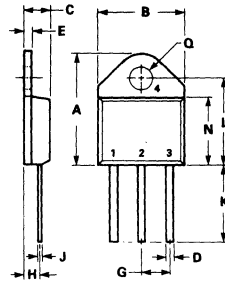


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.84	0.88	0.0325	0.035
F	3.51	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.87	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
(TO-220AB)

- STYLE 1:
 PIN 1: BASE
 2: COLLECTOR
 3: EMITTER
 4: COLLECTOR



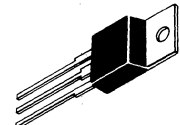
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
(TO-218AC)

Designer's Data Sheet
NPN Silicon Power Transistors
Switchmode III Series

MJE16080
MJE16081

POWER TRANSISTORS
8 AMPERES
400 and 450 VOLTS
80 WATTS



CASE 221A-04
 (TO-220AB)

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 10 ns Inductive Fall Time – 100°C (Typ)
 - 80 ns Inductive Crossover Time – 100°C (Typ)
 - 900 ns Inductive Storage Time – 100°C (Typ)
- Operating Temperature Range – 65 to +150°C
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents

MAXIMUM RATINGS

Rating	Symbol	MJE16080	MJE16081	Unit
Collector-Emitter Voltage	$V_{CE0(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	800	850	Vdc
Emitter Base Voltage	V_{EB}	9		Vdc
Collector Current — Continuous Peak(1)	I_C	8		Adc
	I_{CM}	16		
Base Current — Continuous Peak(1)	I_B	4		Adc
	I_{BM}	8		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C @ $T_C = 100^\circ\text{C}$	P_D	80		Watts
		32		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

MJE16080, MJE16081

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0)	MJE16080 MJE16081 V _{CEO(sus)}	400 450	— —	— —	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 100°C)	I _{CEV}	— —	0.020 —	0.25 2.5	mAdc
Emitter Cutoff Current (V _{EB} = 9 Vdc, I _C = 0)	I _{EBO}	—	0.05	50	μAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	I _{S/b}	See Figure 13				
Clamped Inductive SOA with Base Reverse Biased	RB _{SOA}	See Figure 14				

ON CHARACTERISTICS⁽¹⁾

DC Current Gain (V _{CE} = 5 Vdc)	I _C = 1.0 Adc I _C = 8 Adc	h _{FE}	15 5	25 10	— —	— —
Collector-Emitter Saturation Voltage (I _C = 2 Adc, I _B = 0.25 Adc) (I _C = 5 Adc, I _B = 0.625 Adc) (I _C = 8 Adc, I _B = 1.6 Adc) (I _C = 5 Adc, I _B = 0.625 Adc, T _C = 100°C)	V _{CE(sat)}	— — — —	0.2 0.4 0.6 0.5	0.5 1.2 1.5 1.5	Vdc	
Base-Emitter Saturation Voltage (I _C = 2 Adc, I _B = 0.25 Adc) (I _C = 5 Adc, I _B = 0.625 Adc) (I _C = 5 Adc, I _B = 0.625 Adc, T _C = 100°C)	V _{BE(sat)}	— — —	0.9 1 1	1.2 1.5 1.5	Vdc	

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1 MHz)	C _{ob}	—	120	—	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 125 Vdc, I _C = 5 A I _{B1} = I _{B2} = 0.625 Adc t _p = 25 μs, Duty Cycle ≤ 2%)	t _d	—	0.07	0.15	μs
Rise Time		t _r	—	0.03	0.08	μs
Storage Time		t _s	—	0.5	2	μs
Fall Time		t _f	—	0.2	0.5	μs
Inductive Load, Clamped (Table 2)						
Storage Time	(I _C = 5 A, V _{clamp} = 350 Vdc, V _{BE(off)} = 5 Vdc, I _{B1} = 0.625 Adc) T _C = 100°C	t _{sv}	—	0.90	2	μs
Crossover Time		t _c	—	0.08	0.20	μs
Storage Time		t _{fi}	—	0.01	0.10	μs
Fall Time						

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

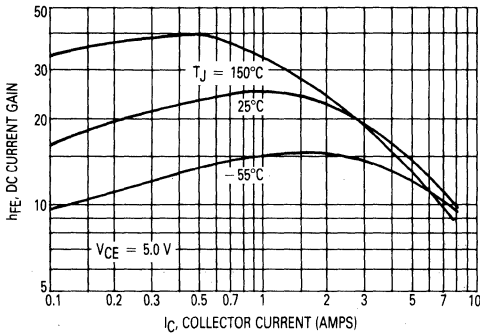


Figure 1. DC Current Gain

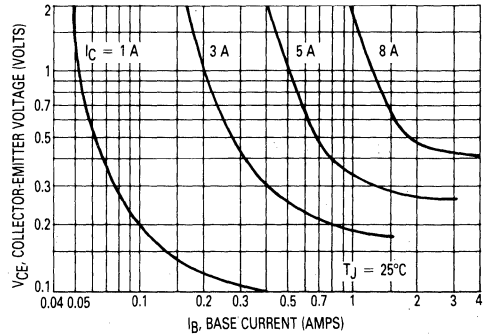


Figure 2. Collector Saturation Region

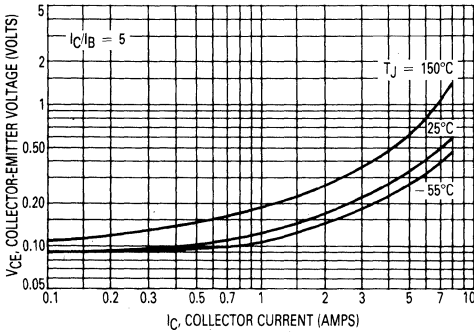


Figure 3. Collector-Emitter Saturation Voltage

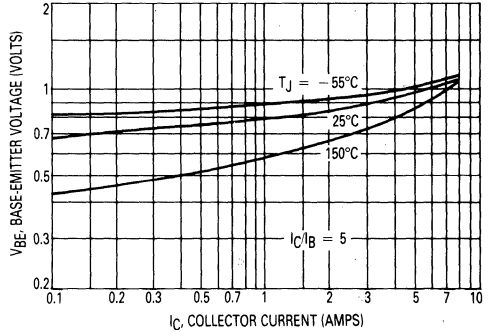


Figure 4. Base-Emitter Saturation Voltage

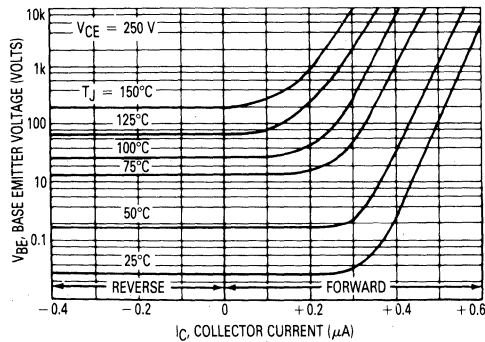


Figure 5. Collector Cutoff Region

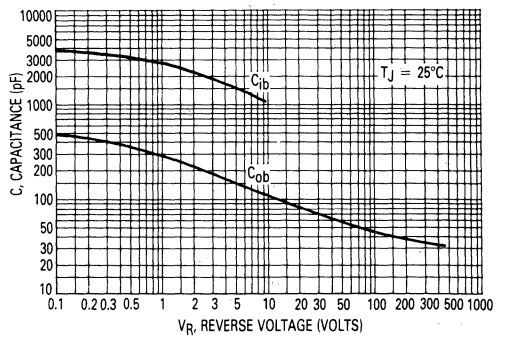


Figure 6. Capacitance Variation

3

TYPICAL DYNAMIC CHARACTERISTICS

$T_J = 25^\circ\text{C}$

$T_J = 100^\circ\text{C}$

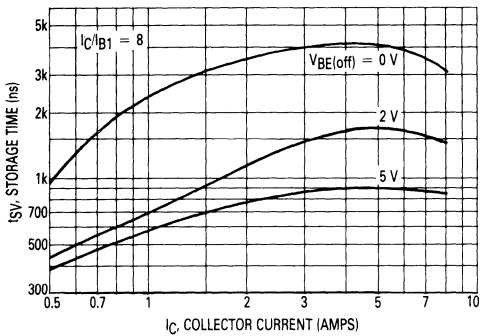


Figure 7. Inductive Storage Time

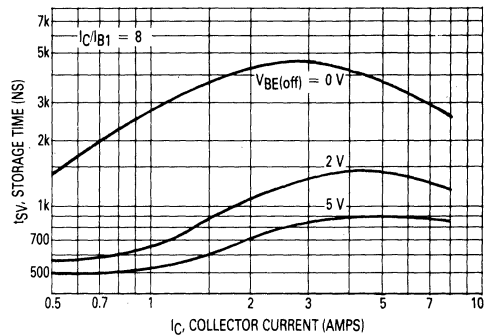


Figure 8. Inductive Storage Time

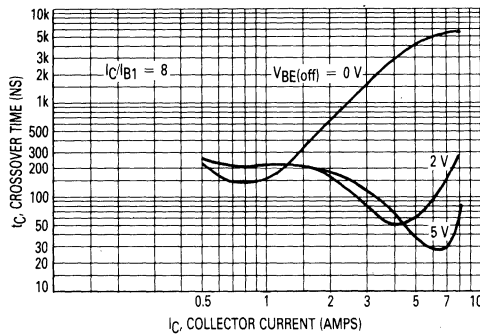


Figure 9. Inductive Crossover Time

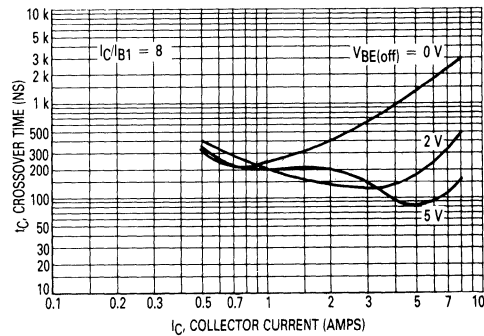


Figure 10. Inductive Crossover Time

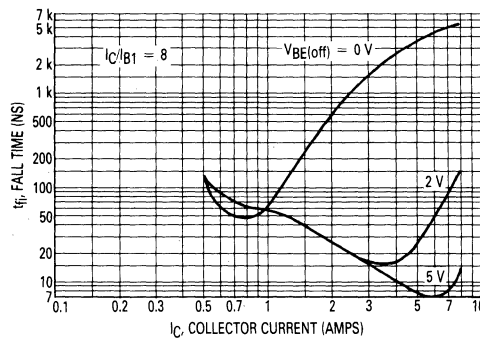


Figure 11. Inductive Fall Time

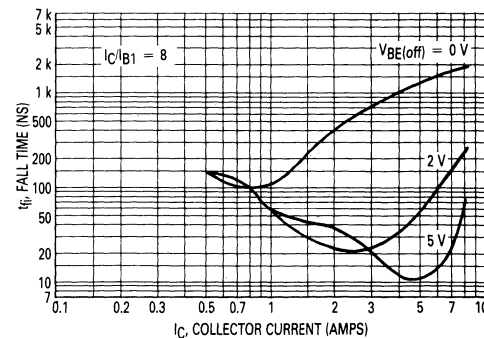


Figure 12. Inductive Fall Time

GUARANTEED SAFE OPERATING AREA LIMITS

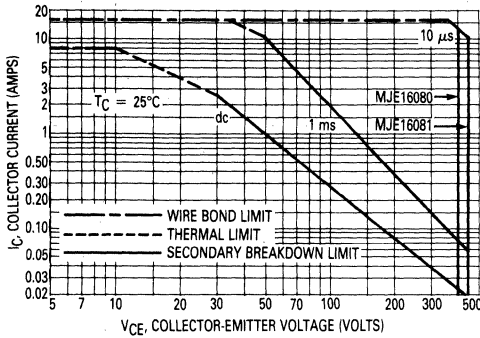


Figure 13. Maximum Rated Forward Bias Safe Operating Area

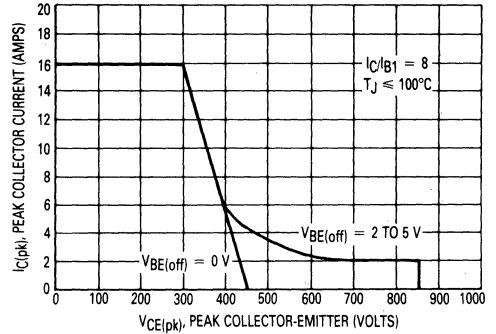


Figure 14. Maximum Rated Reverse Bias Safe Operating Area

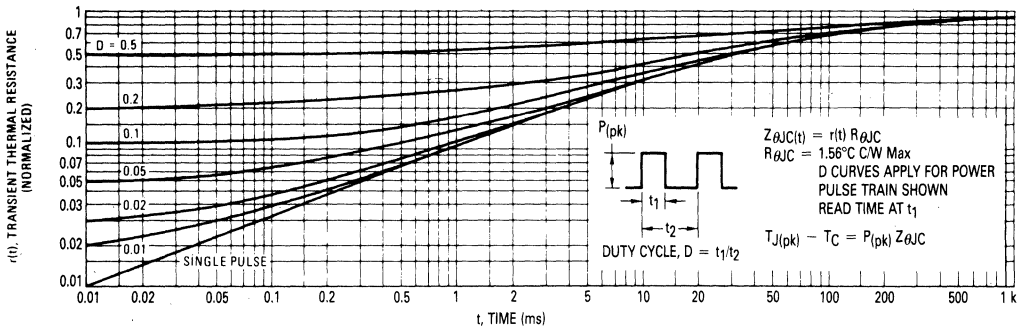


Figure 15. Typical Thermal Response [$Z_{\theta JC}(t)$]

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 16.

$T_J(pk)$ may be calculated from the data in Figure 15. At high case temperatures, thermal limitations will re-

duce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

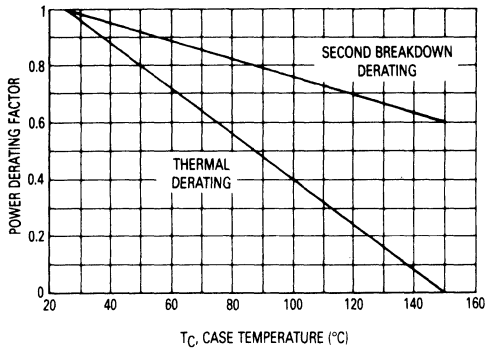


Figure 16. Power Derating

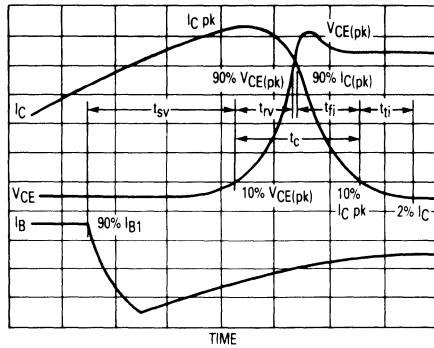


Figure 17. Inductive Switching Measurements

Table 1. Resistive Load Switching

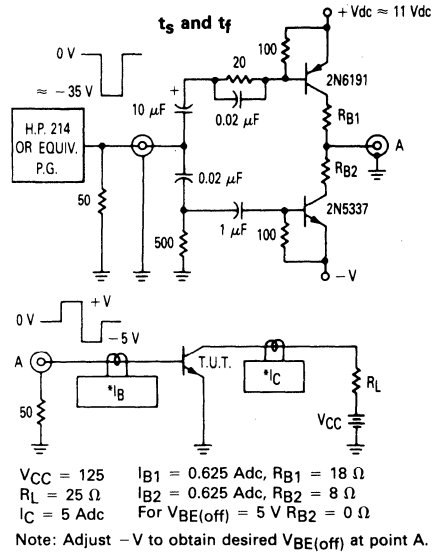
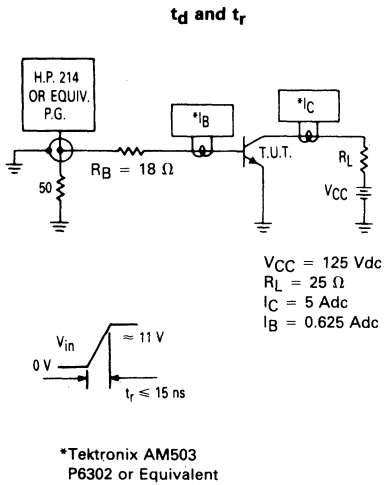
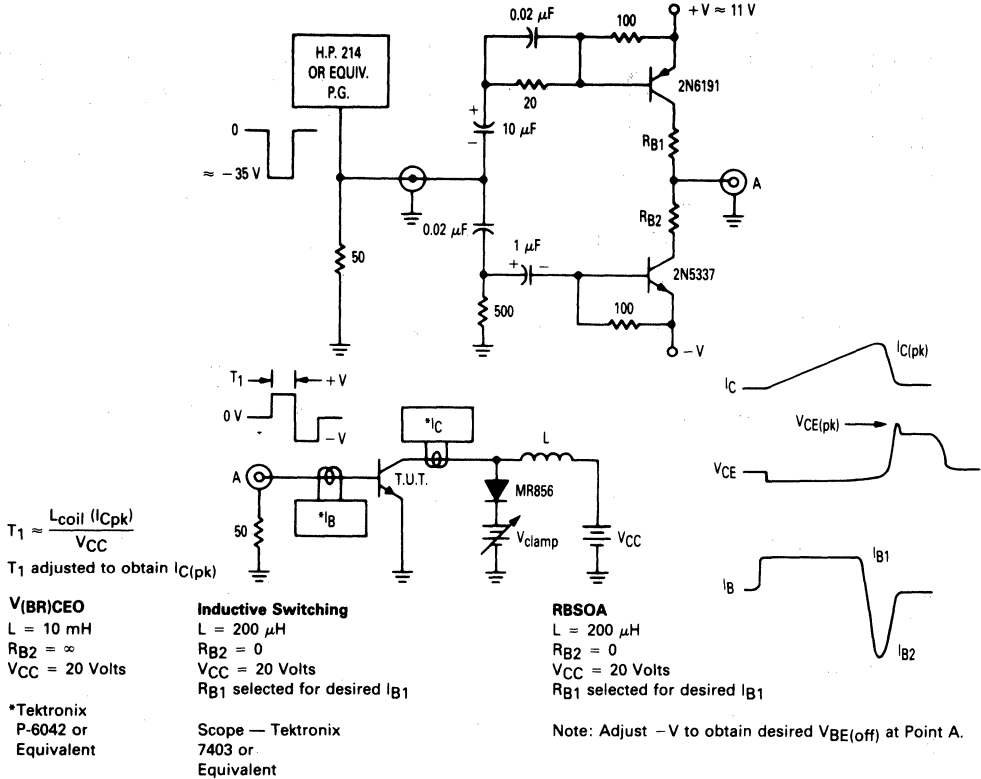
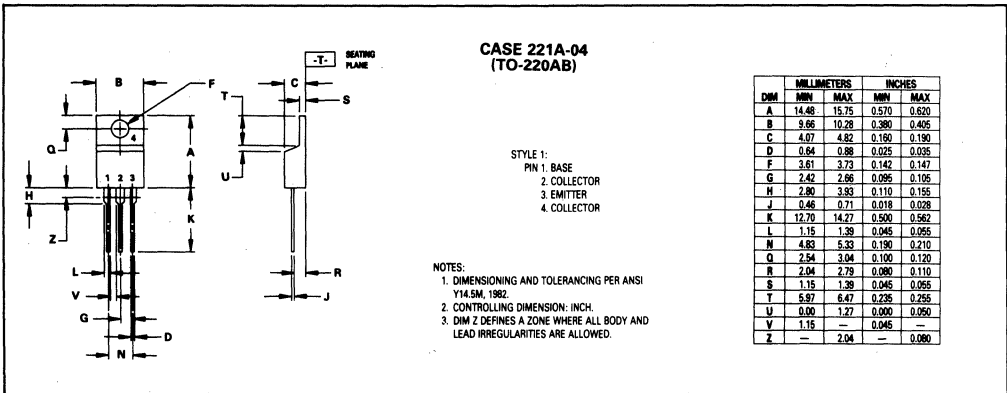


Table 2. Inductive Load Switching



3



MOTOROLA
SEMICONDUCTOR
 TECHNICAL DATA

NPN	PNP
MJH6282	MJH6285
MJH6283	MJH6286
MJH6284	MJH6287

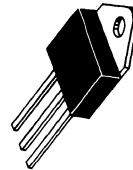
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for general-purpose amplifier and low-speed switching motor control applications.

- Similar to the Popular NPN 2N6282, 2N6283, 2N6284 and the PNP 2N6285, 2N6286, 2N6287
- Rugged RBSOA Characteristics
- Monolithic Construction with Built-In Collector-Emitter Diode

**DARLINGTON
 20 AMPERE
 COMPLEMENTARY SILICON
 POWER TRANSISTORS**

**60, 80, 100 VOLTS
 160 WATTS**



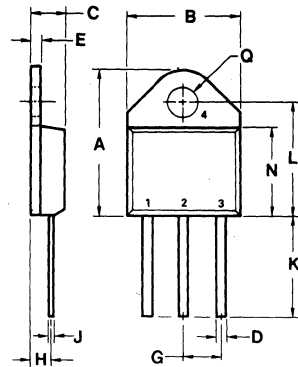
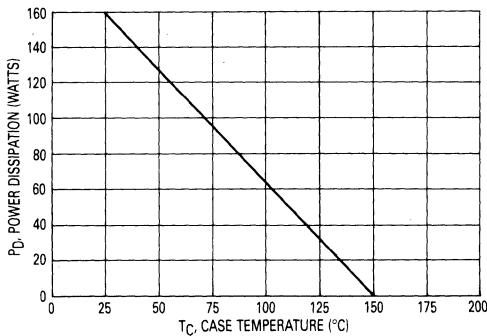
MAXIMUM RATINGS

Rating	Symbol	MJH6282 MJH6285	MJH6283 MJH6286	MJH6284 MJH6287	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	20 40			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	160 1.28			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.78	$^\circ\text{C}/\text{W}$

FIGURE 1 — POWER DERATING



STYLE 1:

- PIN 1. BASE
- COLLECTOR
- EMITTER
- COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.85	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
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K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

**CASE 340-01
 TO-218AC**

MJH6282, MJH6283, MJH6284 NPN
MJH6285, MJH6286, MJH6287 PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($I_C = 0.1 \text{ Adc}$, $I_B = 0$)	MJH6282, MJH6285 MJH6283, MJH6286 MJH6284, MJH6287	$V_{CE(sus)}$	60 80 100	— — —	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 50 \text{ Vdc}$, $I_B = 0$)	MJH6282, MJH6285 MJH6283, MJH6286 MJH6284, MJH6287	I_{CEO}	— — —	1.0 1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_C = 150^\circ\text{C}$)		I_{CEX}	— —	0.5 5.0	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	2.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 20 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	h_{FE}	750 100	18,000 —	—
Collector-Emitter Saturation Voltage ($I_C = 10 \text{ Adc}$, $I_B = 40 \text{ mAdc}$) ($I_C = 20 \text{ Adc}$, $I_B = 200 \text{ mAdc}$)	$V_{CE(sat)}$	— —	2.0 3.0	Vdc
Base-Emitter On Voltage ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	$V_{BE(on)}$	—	2.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 20 \text{ Adc}$, $I_B = 200 \text{ mAdc}$)	$V_{BE(sat)}$	—	4.0	Vdc

DYNAMIC CHARACTERISTICS

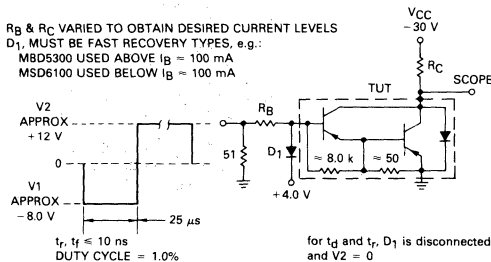
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	$ h_{fe} $	4.0	—	MHz	
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	MJH6282, 83, 84 MJH6285, 86, 87	C_{ob}	— —	400 600	pF
Small-Signal Current Gain ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	300	—	—	

SWITCHING CHARACTERISTICS

	Resistive Load	Symbol	Typical		Unit
			NPN	PNP	
Delay Time	$V_{CC} = 30 \text{ Vdc}$, $I_C = 10 \text{ Adc}$ $I_{B1} = I_{B2} = 100 \text{ mA}$ Duty Cycle = 1.0%	t_d	0.1	0.1	μs
Rise Time		t_r	0.3	0.3	
Storage Time		t_s	1.0	1.0	
Fall Time		t_f	3.5	2.0	

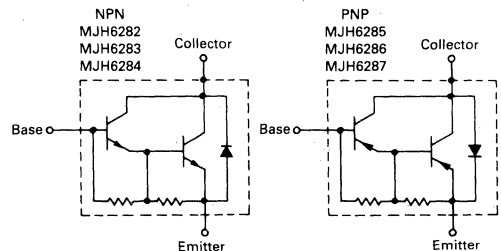
(1) Pulse test: Pulse Width = 300 μs , Duty Cycle = 2.0%.

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

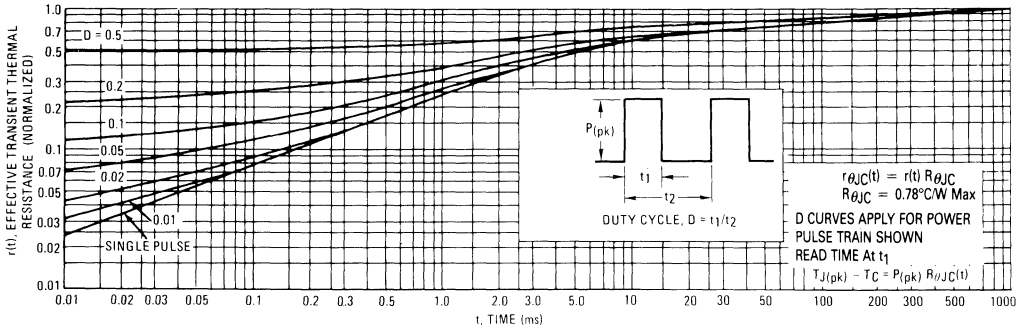
FIGURE 3 — DARLINGTON SCHEMATIC



3

**MJH6282, MJH6283, MJH6284 NPN
MJH6285, MJH6286, MJH6287 PNP**

FIGURE 4 — THERMAL RESPONSE



FBSOA, FORWARD BIAS SAFE OPERATING AREA

FIGURE 5 — MJH6282, MJH6285

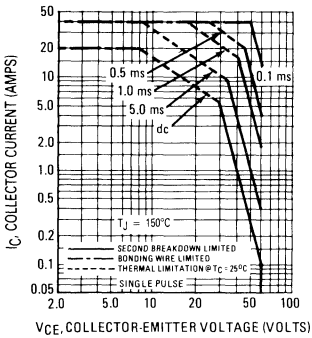


FIGURE 6 — MJH6283, MJH6286

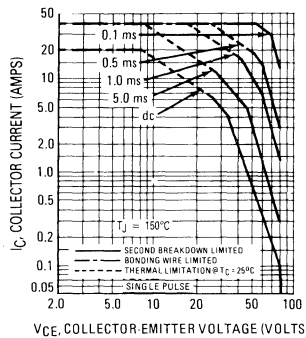


FIGURE 7 — MJH6284, MJH6287

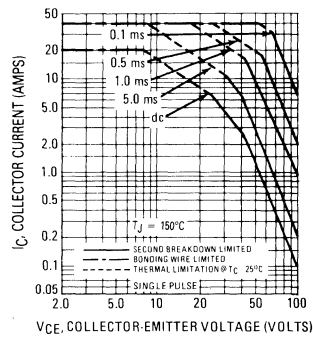
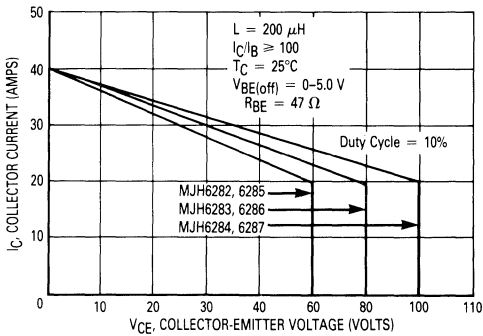


FIGURE 8 — MAXIMUM RBSOA, REVERSE BIAS SAFE OPERATING AREA



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5, 6 and 7 is based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJH6282, MJH6283, MJH6284 NPN
MJH6285, MJH6286, MJH6287 PNP

FIGURE 9 — DC CURRENT GAIN

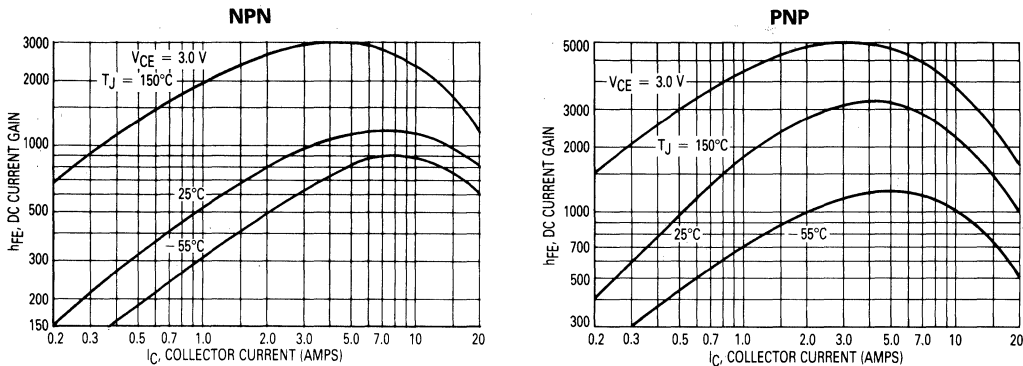


FIGURE 10 — COLLECTOR SATURATION REGION

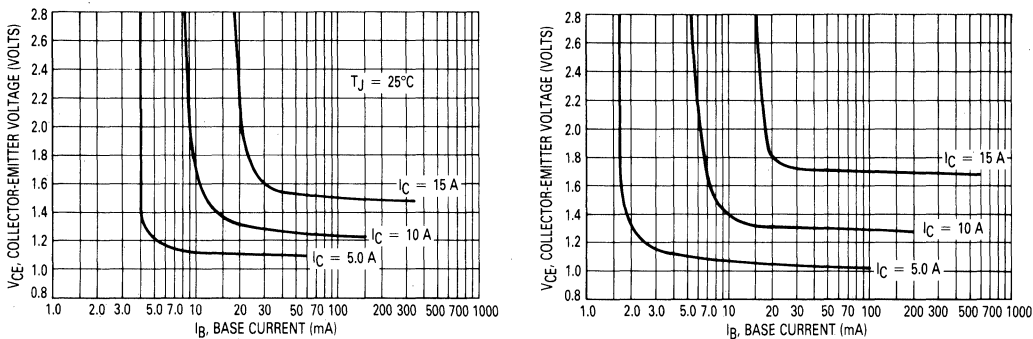
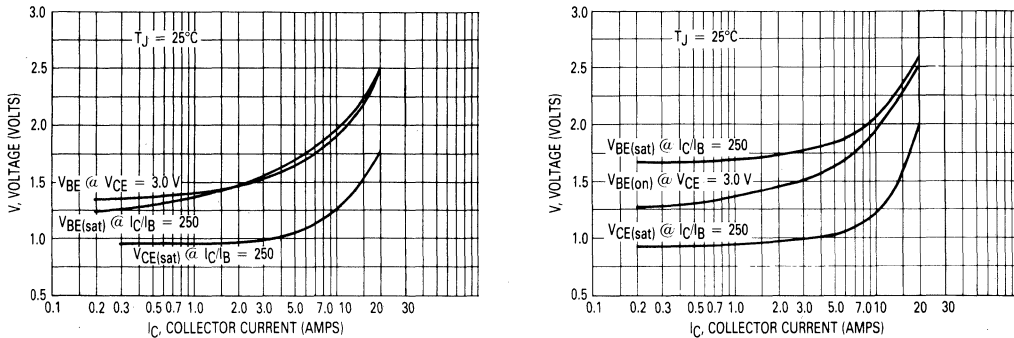


FIGURE 11 — "ON" VOLTAGES



3

PNP	NPN
MJH11017	MJH11018
MJH11019	MJH11020
MJH11021	MJH11022

**COMPLEMENTARY DARLINGTON
SILICON POWER TRANSISTORS**

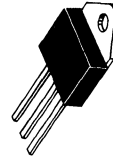
... designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High DC Current Gain @ 10 Adc — $h_{FE} = 400$ Min (All Types)
- Collector-Emitter Sustaining Voltage
 $V_{CE(sus)} = 150$ Vdc (Min) — MJH11018, 17
 $= 200$ Vdc (Min) — MJH11020, 19
 $= 250$ Vdc (Min) — MJH11022, 21
- Low Collector-Emitter Saturation Voltage
 $V_{CE(sat)} = 1.2$ V (Typ) @ $I_C = 5.0$ A
 $= 1.8$ V (Typ) @ $I_C = 10$ A
- Monolithic Construction

15 AMPERE

**DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON**

150, 200, 250 VOLTS
150 WATTS



MAXIMUM RATINGS

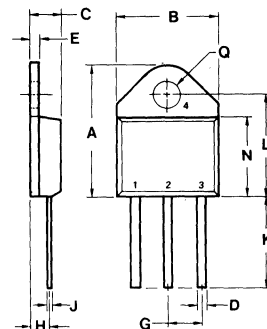
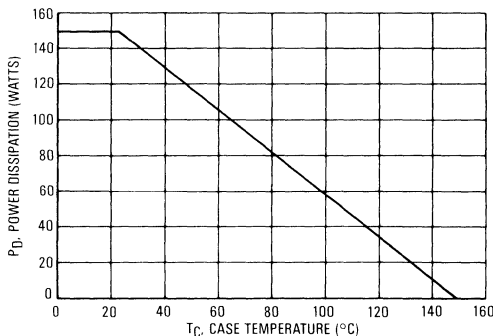
Rating	Symbol	MJH			Unit
		11018 11017	11020 11019	11022 11021	
Collector-Emitter Voltage	V_{CEO}	150	200	250	Vdc
Collector-Base Voltage	V_{CB}	150	200	250	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous — Peak (1)	I_C	15 30			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above 25°C	P_D	150 1.2			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.83	$^\circ\text{C}/\text{W}$

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle $\leq 10\%$

FIGURE 1 — POWER DERATING



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.48	15.90	0.610	0.628
C	4.19	5.08	0.165	0.200
D	1.02	1.85	0.040	0.075
E	1.35	1.85	0.053	0.075
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

**CASE 340-01
(TO-218AC)**

MJH11017, MJH11019, MJH11021 PNP MJH11018, MJH11020, MJH11022 NPN

ELECTRICAL CHARACTERISTICS (T_C = 25°C Unless Otherwise Noted)

Characteristics	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I _C = 0.1 Adc, I _B = 0)	MJH11017, MJH11018 MJH11019, MJH11020 MJH11021, MJH11022	V _{CEO(sus)}	150 200 250	— — —	Vdc
Collector Cutoff Current (V _{CE} = 75 Vdc, I _B = 0) (V _{CE} = 100 Vdc, I _B = 0) (V _{CE} = 125 Vdc, I _B = 0)	MJH11017, MJH11018 MJH11019, MJH11020 MJH11021, MJH11022	I _{CEO}	— — —	1.0 1.0 1.0	mAdc
Collector Cutoff Current (V _{CE} = Rated V _{CB} , V _{BE(off)} = 1.5 Vdc) (V _{CE} = Rated V _{CB} , V _{BE(off)} = 1.5 Vdc, T _J = 150°C)		I _{CEV}	— —	0.5 5.0	mAdc
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)		I _{EBO}	—	2.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 10 Adc, V _{CE} = 5.0 Vdc) (I _C = 15 Adc, V _{CE} = 5.0 Vdc)	h _{FE}	400 100	15,000 —	—
Collector-Emitter Saturation Voltage (I _C = 10 Adc, I _B = 100 mA) (I _C = 15 Adc, I _B = 150 mA)	V _{CE(sat)}	— —	2.5 4.0	Vdc
Base-Emitter On Voltage (I _C = 10 A, V _{CE} = 5.0 Vdc)	V _{BE(on)}	—	2.8	Vdc
Base-Emitter Saturation Voltage (I _C = 15 Adc, I _B = 150 mA)	V _{BE(sat)}	—	3.8	Vdc

DYNAMIC CHARACTERISTICS

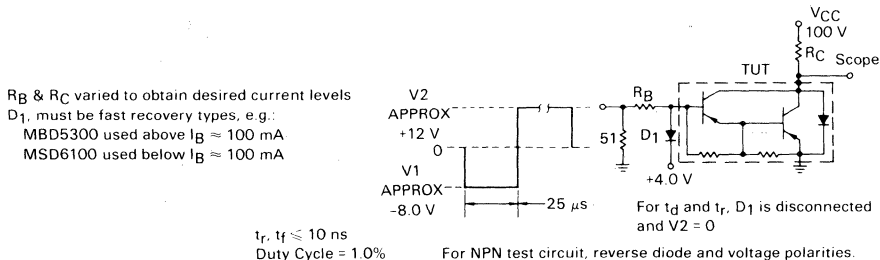
Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio (I _C = 10 Adc, V _{CE} = 3.0 Vdc, f = 1.0 MHz)	[h _{fe}]	3.0	—	—
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	— —	400 600	pF
Small-Signal Current Gain (I _C = 10 Adc, V _{CE} = 3.0 Vdc, f = 1.0 kHz)	h _{fe}	100	—	—

SWITCHING CHARACTERISTICS

Characteristics	Symbol	Typical		Unit
		NPN	PNP	
Delay Time	t _d	150	75	ns
Rise Time	t _r	1.2	0.5	μs
Storage Time	t _s	4.4	2.7	μs
Fall Time	t _f	2.5	2.5	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT



**MJH11017, MJH11019, MJH11021 PNP
MJH11018, MJH11020, MJH11022 NPN**

FIGURE 3 — THERMAL RESPONSE

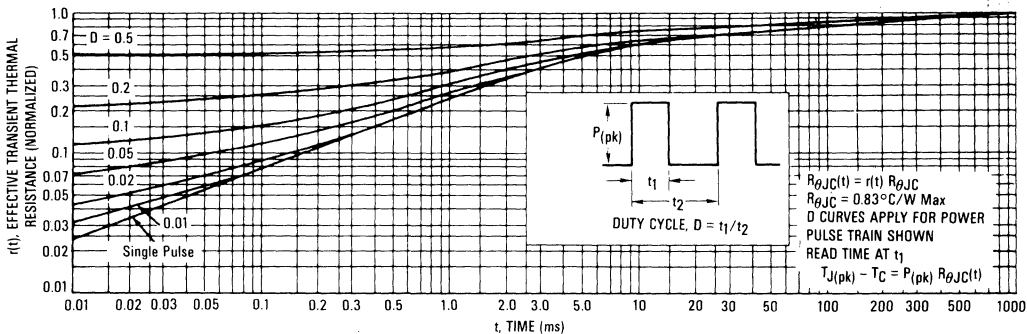
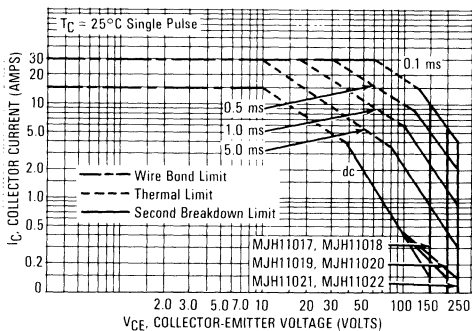


FIGURE 4 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (FBSOA)

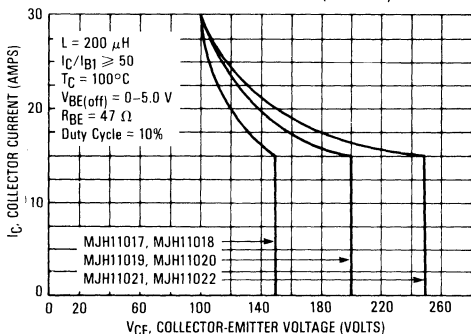


FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 5 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA (RBSOA)



REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives RBSOA characteristics.

MJH11017, MJH11019, MJH11021 PNP
MJH11018, MJH11020, MJH11022 NPN

FIGURE 6 — DC CURRENT GAIN

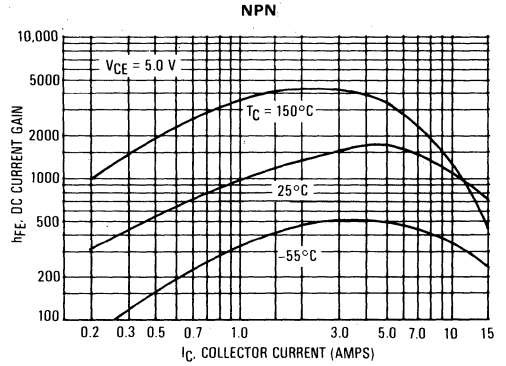
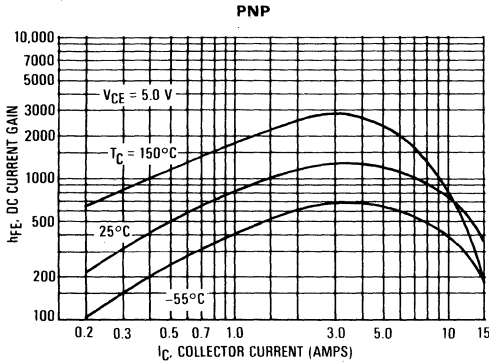


FIGURE 7 — COLLECTOR SATURATION REGION

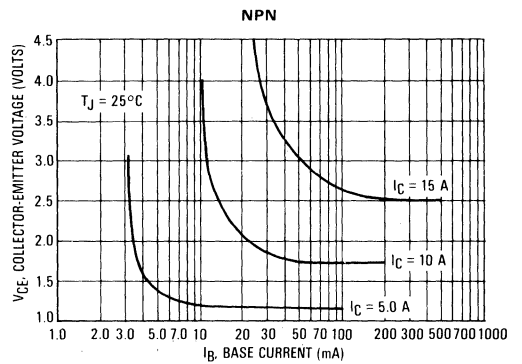
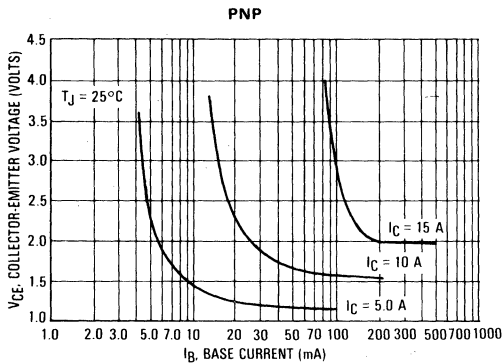
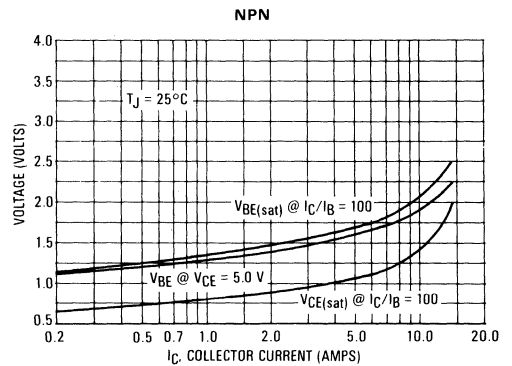
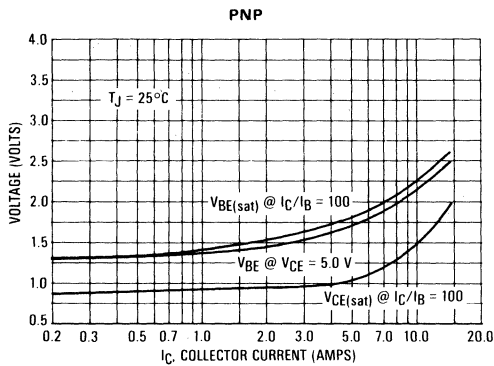


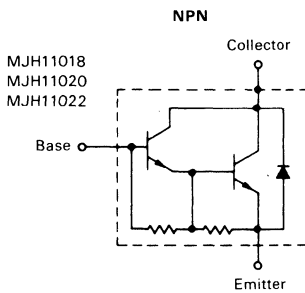
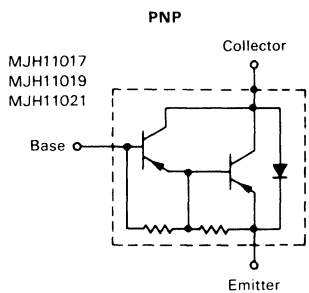
FIGURE 8 — "ON" VOLTAGES



3

MJH11017, MJH11019, MJH11021 PNP
MJH11018, MJH11020, MJH11022 NPN

FIGURE 9 — DARLINGTON SCHEMATIC



**MJH13090
MJH13091
See Page 3-816**

**MJH16010
MJH16012
See Page 3-890**

**MJH16002
MJH16004
See Page 3-1090**

**MJH16010A
See Page 3-898**

**MJH16002A
See Page 3-866**

**MJH16018
See Page 3-914**

**MJH16006
MJH16008
See Page 3-874**

**MJH16032
MJH16034
See Page 3-1098**

**MJH16006A
See Page 3-882**

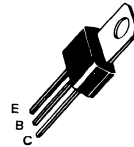
MPS-U01
MPS-U01A

NPN SILICON ANNULAR TRANSISTORS

... designed for complementary symmetry audio circuits to 10 Watts output.

- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)} = 0.5 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Adc}$
- Complements to PNP MPS-U51 and MPS-U51A
- Uniwatt Package for Excellent Thermal Properties – 1.0 Watt @ $T_A = 25^\circ\text{C}$

NPN SILICON
AUDIO TRANSISTORS



MAXIMUM RATINGS

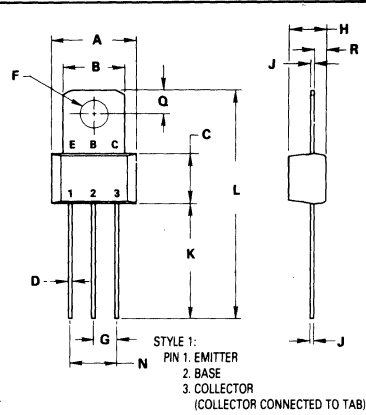
Rating	Symbol	MPS-U01	MPS-U01A	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Base Voltage	V_{CB}	40	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	2.0		A dc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0	8.0	Watt mW/°C
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10	80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA(1)}$	125	°C/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

Uniwatt packages can be To-5 lead formed by adding -5 to the device title and tab formed by flush mounting by adding -1 to the device title.



NOTE:
 1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MPS-U01, MPS-U01A

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 10\text{ mAdc}$, $I_B = 0$)	MPS-U01 MPS-U01A $V_{(BR)CEO}$	30 40	— —	Vdc
Collector-Base Breakdown Voltage ($I_C = 100\ \mu\text{Adc}$, $I_E = 0$)	MPS-U01 MPS-U01A $V_{(BR)CBO}$	40 50	— —	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100\ \mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	5.0	—	Vdc
Collector Cutoff Current ($V_{CB} = 30\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 40\text{ Vdc}$, $I_E = 0$)	MPS-U01 MPS-U01A I_{CBO}	— —	0.1 0.1	μAdc
Emitter Cutoff Current ($V_{BE} = 3.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	0.1	μAdc
ON CHARACTERISTICS(1)				
DC Current Gain ($I_C = 10\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 100\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 1.0\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	55 60 50	— — —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.1\text{ Adc}$)	$V_{CE(sat)}$	—	0.5	Vdc
Base-Emitter On Voltage ($I_C = 1.0\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$)	$V_{BE(on)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product ($I_C = 50\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 20\text{ MHz}$)	f_T	50	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$)	C_{ob}	—	20	pF

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 1 — DC CURRENT GAIN

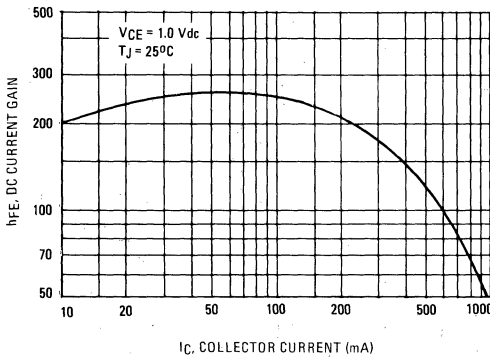


FIGURE 2 — "ON" VOLTAGES

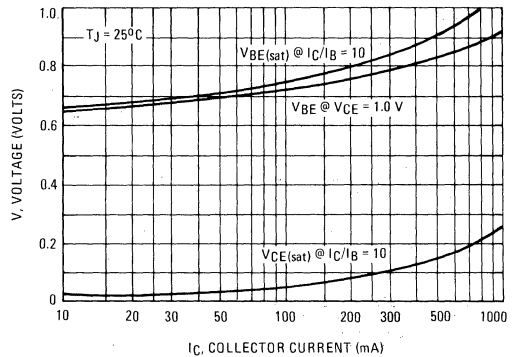
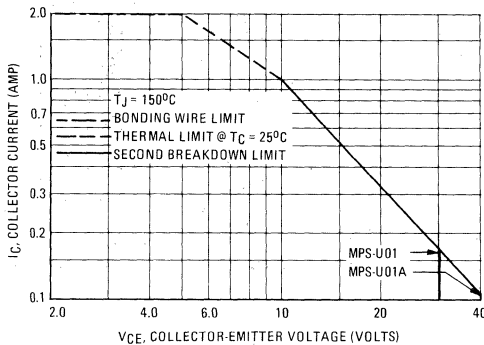


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

**NPN SILICON ANNULAR
 AMPLIFIER TRANSISTOR**

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Power Dissipation – $P_D = 10 \text{ W} @ T_C = 25^\circ\text{C}$
- Complement to PNP MPS-U52

**NPN SILICON
 AMPLIFIER TRANSISTOR**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	800	mA dc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

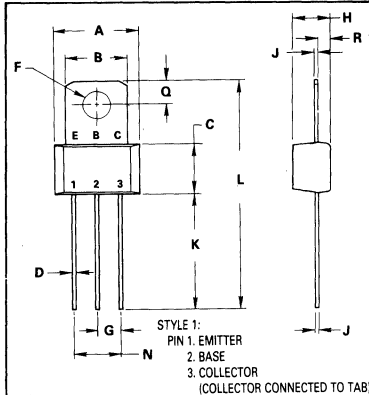
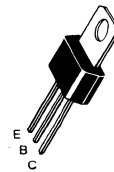
Characteristic	Symbol	Min	Max	Unit
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mA dc}, I_B = 0$)	$V_{(BR)CEO}$	40	-	Vdc
Collector-Base Breakdown Voltage ($I_C = 100 \mu\text{A dc}, I_E = 0$)	$V_{(BR)CBO}$	60	-	Vdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}, I_E = 0$)	I_{CBO}	-	100	nA dc

ON CHARACTERISTICS

DC Current Gain ($I_C = 10 \text{ mA dc}, V_{CE} = 10 \text{ Vdc}$) ($I_C = 150 \text{ mA dc}, V_{CE} = 10 \text{ Vdc}$) ($I_C = 500 \text{ mA dc}, V_{CE} = 10 \text{ Vdc}$)	h_{FE}	50 50 30	- 300 -	
Collector-Emitter Saturation Voltage ($I_C = 150 \text{ mA dc}, I_B = 15 \text{ mA dc}$)	$V_{CE(sat)}$	-	0.4	Vdc
Base-Emitter Saturation Voltage ($I_C = 150 \text{ mA dc}, I_B = 15 \text{ mA dc}$)	$V_{BE(sat)}$	-	1.3	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 20 \text{ mA dc}, V_{CE} = 20 \text{ Vdc}, f = 100 \text{ MHz}$)	f_T	100	-	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 100 \text{ kHz}$)	C_{ob}	-	20	pF



NOTE:
 1. LEADS WITHIN 0.15 mm (0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	3.30	7.24	0.260	0.286
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC 0.100 BSC			
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC 0.200 BSC			
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

FIGURE 1 – NORMALIZED DC CURRENT GAIN

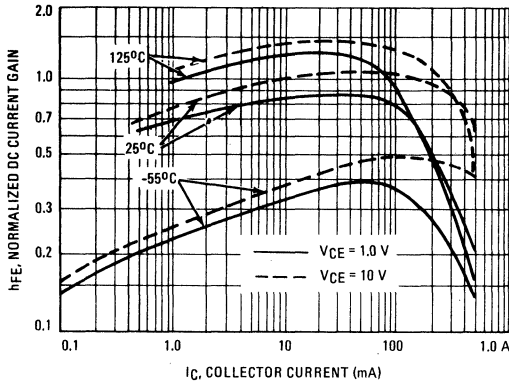


FIGURE 2 – COLLECTOR-EMITTER SATURATION VOLTAGE versus BASE CURRENT

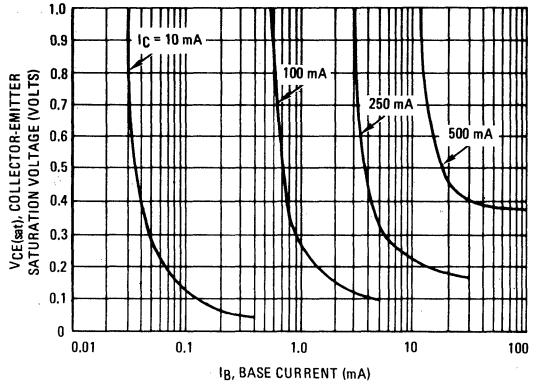


FIGURE 3 – BASE-EMITTER VOLTAGE versus COLLECTOR CURRENT

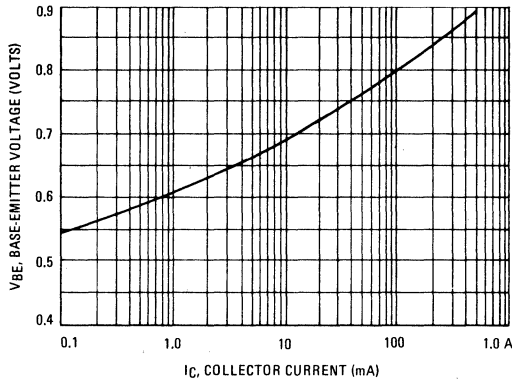


FIGURE 4 – CAPACITANCE versus VOLTAGE

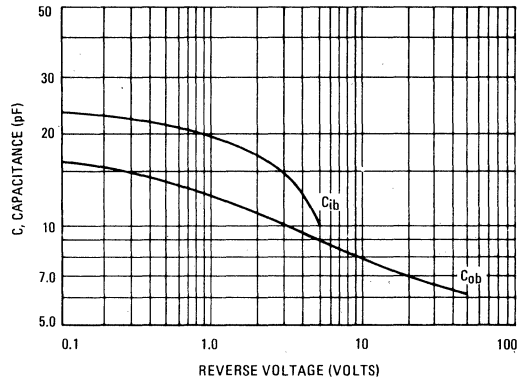


FIGURE 5 – CURRENT-GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

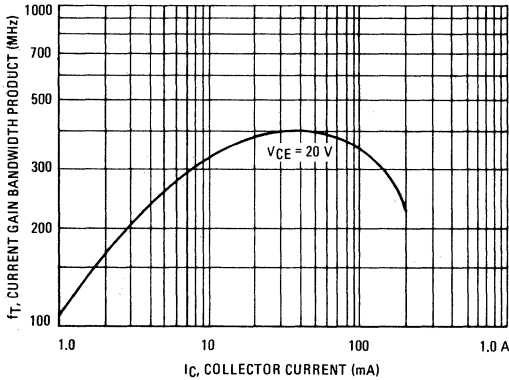
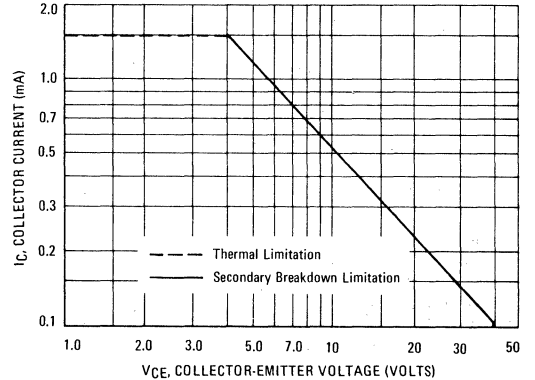


FIGURE 6 – ACTIVE REGION DC SAFE OPERATING AREA



3

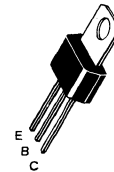
MPS-U03
MPS-U04

**NPN SILICON ANNULAR
HIGH VOLTAGE AMPLIFIER TRANSISTORS**

... designed for horizontal drive applications, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage –
 $V_{(BR)CEO} = 180 \text{ Vdc (Min) @ } I_C = 1 \text{ mAdc} \text{ — MPS-U04}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.5 \text{ Vdc (Max) @ } I_C = 200 \text{ mAdc}$
- High Power Dissipation –
 $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$

**NPN SILICON
AMPLIFIER
TRANSISTORS**

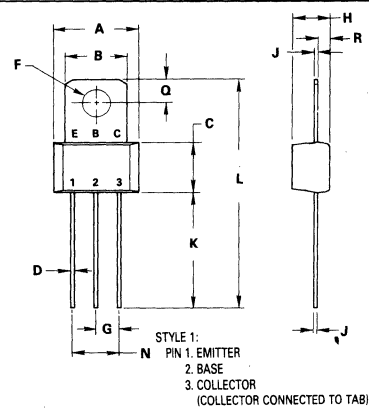


MAXIMUM RATINGS

Rating	Symbol	MPS-U03	MPS-U04	Unit
Collector-Emitter Voltage	V_{CEO}	120	180	Vdc
Collector-Base Voltage	V_{CB}	120	180	Vdc
Emitter-Base Voltage	V_{EB}		5	Vdc
Collector Current	I_C		1	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate Above 25°C	P_D	1	8	Watts mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above 25°C	P_D	10	80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		$^\circ\text{C}$
Solder Temperature, 1/16" From Case for 10 Seconds	—	260		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C/W}$



NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MPS-U03, MPS-U04

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}$, $I_E = 0$)	$V_{(BR)CEO}$	120 180	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 100 \mu\text{Adc}$, $I_E = 0$)	$V_{(BR)CBO}$	120 180	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	5.0	—	Vdc
Collector Cutoff Current ($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 150 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	— —	0.1 0.1	μAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 10 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$)	h_{FE}	40	—	—
Collector-Emitter Saturation Voltage ($I_C = 200 \text{ mAdc}$, $I_B = 20 \text{ mAdc}$)	$V_{CE(sat)}$	—	0.5	Vdc
Base-Emitter On Voltage ($I_C = 200 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.0	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 50 \text{ mAdc}$, $V_{CE} = 20 \text{ Vdc}$, $f = 20 \text{ MHz}$)	f_T	35	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 100 \text{ kHz}$)	C_{ob}	—	12	pF
Input Capacitance ($V_{BE} = 0.5 \text{ Vdc}$, $I_C = 0$, $f = 100 \text{ kHz}$)	C_{ib}	—	110	pF

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

3

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN – BANDWIDTH PRODUCT

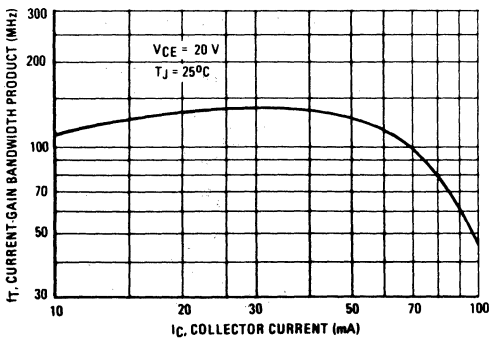
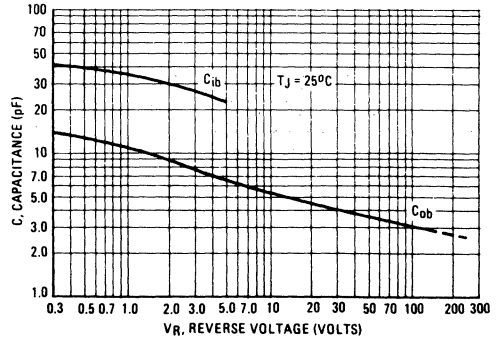


FIGURE 2 – CAPACITANCE



TYPICAL CHARACTERISTICS (Continued)

FIGURE 3 – DC CURRENT GAIN

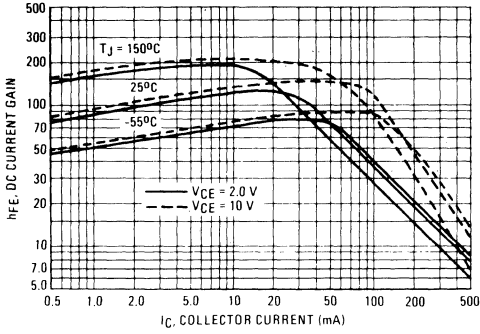


FIGURE 4 – "ON" VOLTAGE

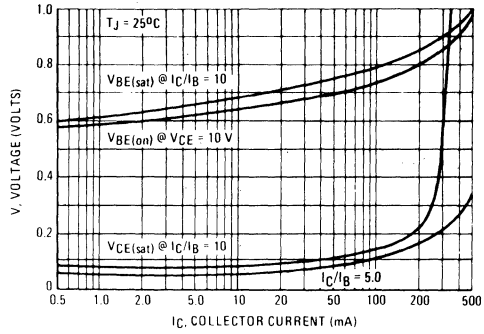


FIGURE 5 – COLLECTOR SATURATION REGION

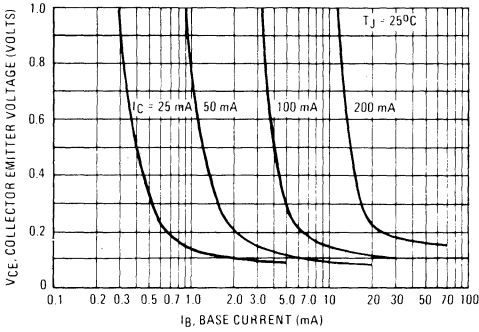


FIGURE 6 – TEMPERATURE COEFFICIENTS

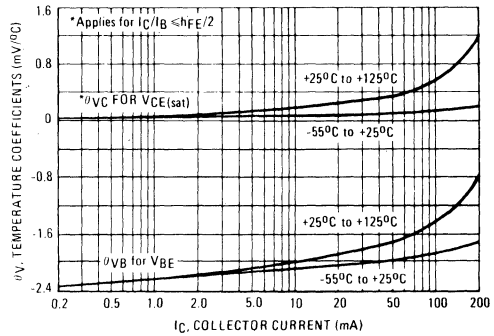


FIGURE 7 – COLLECTOR CHARACTERISTICS

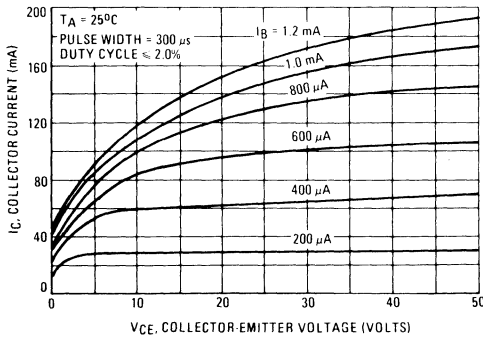
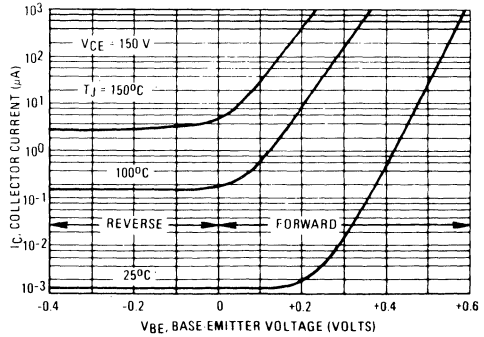


FIGURE 8 – COLLECTOR CUTOFF REGION



TYPICAL CHARACTERISTICS (Continued)

FIGURE 9 – THERMAL RESPONSE

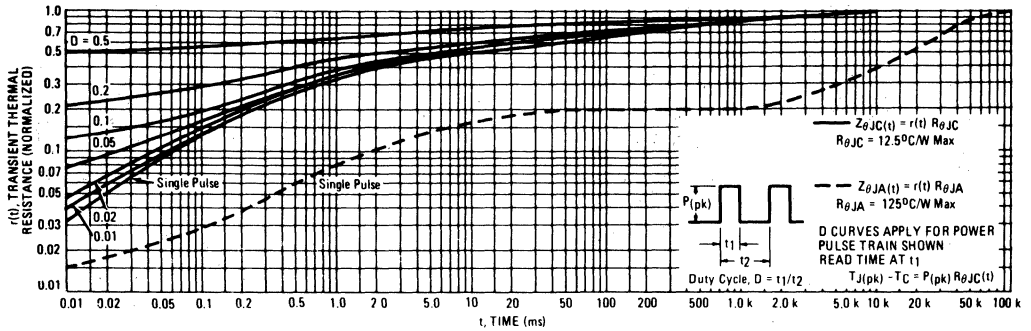
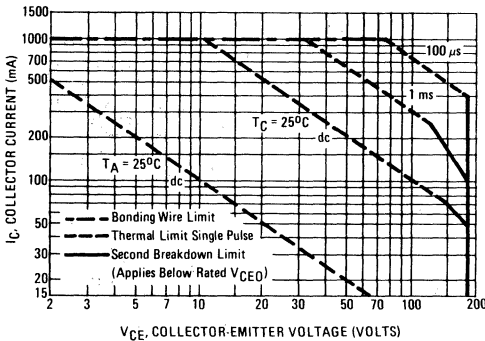


FIGURE 10 – ACTIVE REGION SAFE-OPERATING AREA

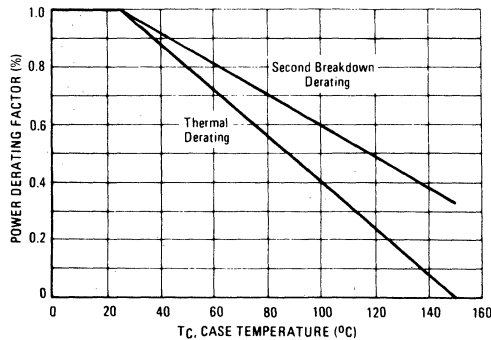


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING



3

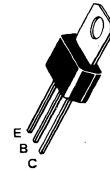
MPS-U05
MPS-U06

**NPN SILICON ANNULAR
 AMPLIFIER TRANSISTORS**

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage –
 $V_{(BR)CEO} = 60 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc} - \text{MPS-U05}$
 $80 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc} - \text{MPS-U06}$
- High Power Dissipation – $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$
- Complements to PNP MPS-U55 and MPS-U56

**NPN SILICON
 AMPLIFIER TRANSISTORS**

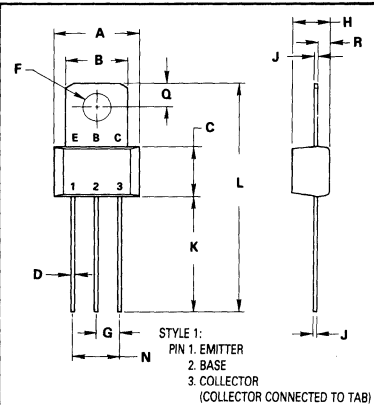


MAXIMUM RATINGS

Rating	Symbol	MPS-U05	MPS-U06	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	2.0		Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0	8.0	Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10	80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	$^\circ\text{C/W}$



NOTE:
 1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

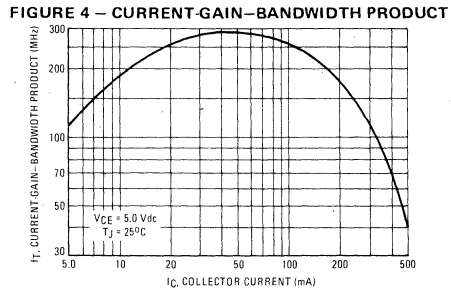
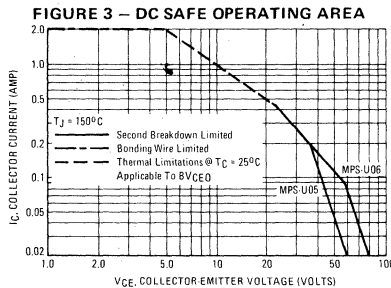
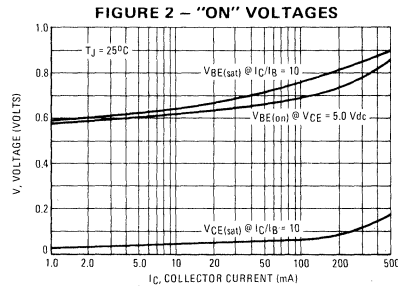
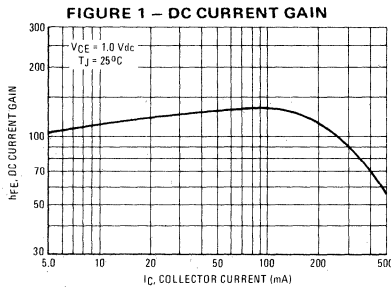
CASE 152-02

MPS-U05, MPS-U06

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	60 80	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	— —	— —	100 100	nAdc
ON CHARACTERISTICS					
DC Current Gain (1) ($I_C = 50 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 250 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$)	h_{FE}	80 60 —	125 100 55	— — —	—
Collector-Emitter Saturation Voltage(1) ($I_C = 250 \text{ mAdc}$, $I_B = 10 \text{ mAdc}$) ($I_C = 250 \text{ mAdc}$, $I_B = 25 \text{ mAdc}$)	$V_{CE(sat)}$	— —	0.18 0.1	0.4 —	Vdc
Base-Emitter On Voltage (1) ($I_C = 250 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$)	$V_{BE(on)}$	—	0.74	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (1) ($I_C = 250 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$, $f = 100 \text{ MHz}$)	f_T	50	150	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 100 \text{ kHz}$)	C_{ob}	—	6.0	12	pF

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

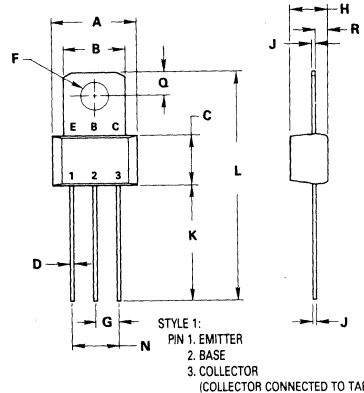
MPS-U07

**NPN SILICON ANNULAR
AMPLIFIER TRANSISTOR**

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage – $V_{(BR)CEO} = 100 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc}$
- High Power Dissipation – $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$
- Complement to PNP MPS-U57

**NPN SILICON
AMPLIFIER TRANSISTOR**



NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	2.0	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ⁽¹⁾ ($I_C = 1.0 \text{ mAdc}, I_B = 0$)	$V_{(BR)CEO}$	100	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{Adc}, I_C = 0$)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 80 \text{ Vdc}, I_E = 0$)	I_{CBO}	—	—	100	nAdc

ON CHARACTERISTICS

DC Current Gain (1) ($I_C = 50 \text{ mAdc}, V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 250 \text{ mAdc}, V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}, V_{CE} = 1.0 \text{ Vdc}$)	h_{FE}	60 30 —	110 65 33	— — —	—
Collector-Emitter Saturation Voltage (1) ($I_C = 250 \text{ mAdc}, I_B = 10 \text{ mAdc}$) ($I_C = 250 \text{ mAdc}, I_B = 25 \text{ mAdc}$)	$V_{CE(sat)}$	— —	0.18 0.1	0.4 —	Vdc
Base-Emitter On Voltage (1) ($I_C = 250 \text{ mAdc}, V_{CE} = 5.0 \text{ Vdc}$)	$V_{BE(on)}$	—	0.76	1.2	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product (1) ($I_C = 250 \text{ mAdc}, V_{CE} = 5.0 \text{ Vdc}, f = 100 \text{ MHz}$)	f_T	50	150	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 100 \text{ kHz}$)	C_{ob}	—	6.0	12	pF

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 1 – DC CURRENT GAIN

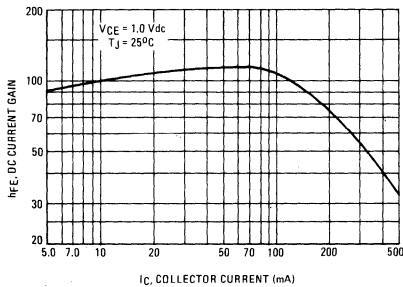


FIGURE 2 – "ON" VOLTAGES

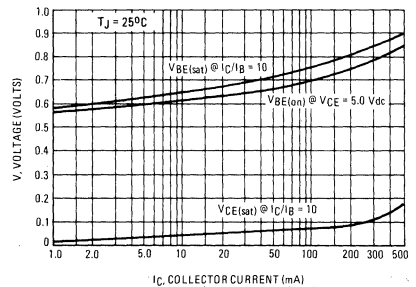


FIGURE 3 – DC SAFE OPERATING AREA

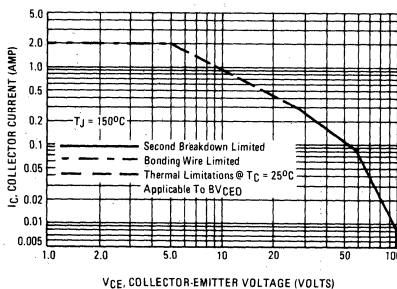
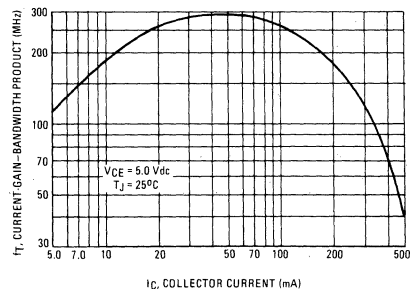


FIGURE 4 – CURRENT-GAIN-BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_J(pk) = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

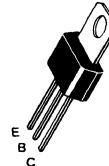
MPS-U10

NPN SILICON ANNULAR TRANSISTOR

... designed for high-voltage video and luminance output stages in TV receivers.

- High Collector-Emitter Breakdown Voltage –
 $V_{(BR)CEO} = 300 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc}$
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.75 \text{ Vdc (Max) @ } I_C = 30 \text{ mAdc}$
- Low Collector-Base Capacitance –
 $C_{cb} = 3.0 \text{ pF (Max) @ } V_{CB} = 20 \text{ Vdc}$

**NPN SILICON
 HIGH VOLTAGE
 AMPLIFIER
 TRANSISTOR**



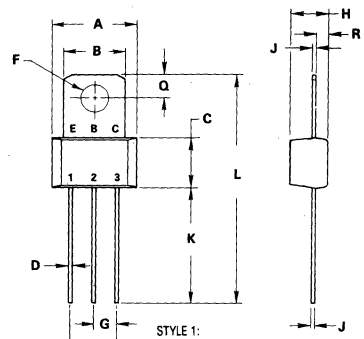
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous	I_C	0.5	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_{J,Tstg}$	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA(1)}$	125	$^\circ\text{C/W}$

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



NOTE:
 1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0 \text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	300	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 100 \mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	300	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{A}$, $I_C = 0$)	$V_{(BR)EBO}$	6.0	—	Vdc
Collector Cutoff Current ($V_{CB} = 200 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	0.2	μA
Emitter Cutoff Current ($V_{BE} = 6.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	0.1	μA

ON CHARACTERISTICS

DC Current Gain ($I_C = 1.0 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$) ($I_C = 10 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$) ($I_C = 30 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$)	h_{FE}	25 40 40	— — —	—
Collector-Emitter Saturation Voltage ($I_C = 30 \text{ mA}$, $I_B = 3.0 \text{ mA}$)	$V_{CE(sat)}$	—	0.75	Vdc
Base-Emitter On Voltage ($I_C = 30 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$)	$V_{BE(on)}$	—	0.85	Vdc

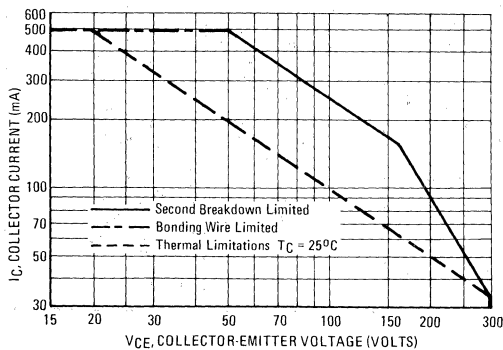
DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product (1) ($I_C = 10 \text{ mA}$, $V_{CE} = 20 \text{ Vdc}$, $f = 100 \text{ MHz}$)	f_T	45	—	MHz
Collector-Base Capacitance ($V_{CB} = 20 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	C_{cb}	—	3.0	pF

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

3

FIGURE 1 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C – V_{CE} limits below which the device will not enter second breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J , power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – DC CURRENT GAIN

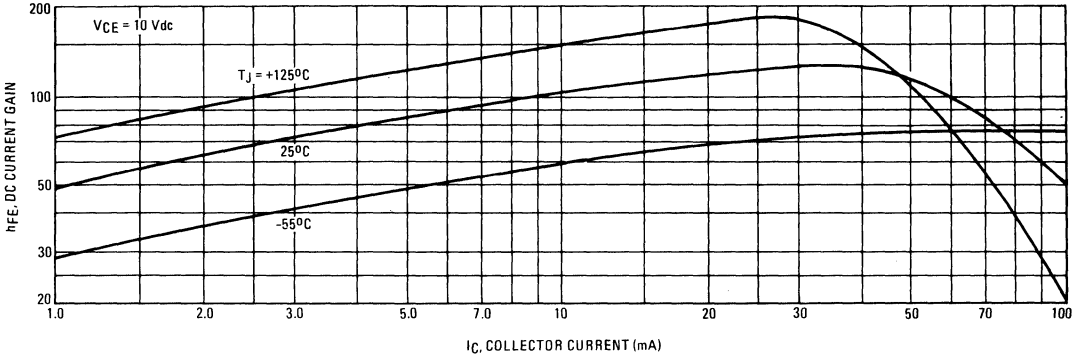


FIGURE 3 – CAPACITANCES

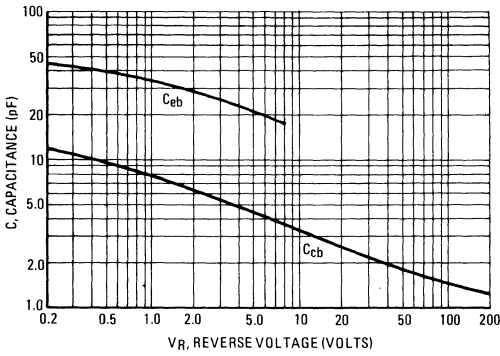


FIGURE 4 – CURRENT-GAIN-BANDWIDTH PRODUCT

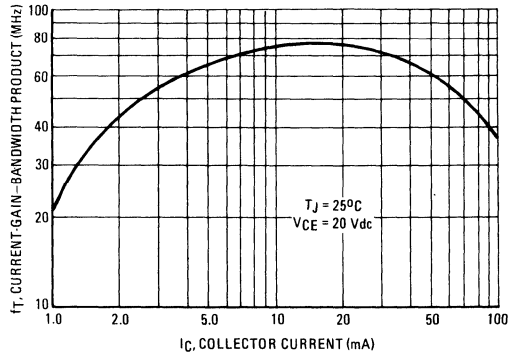
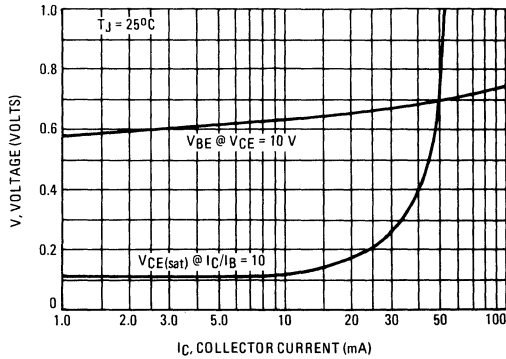


FIGURE 5 – "ON" VOLTAGES

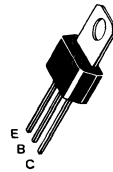


**NPN SILICON DARLINGTON
AMPLIFIER TRANSISTOR**

... designed for amplifier and driver applications.

- High DC Current Gain –
 $h_{FE} = 25,000$ (Min) @ $I_C = 200$ mAdc
 $15,000$ (Min) @ $I_C = 500$ mAdc
- Collector-Emitter Breakdown Voltage –
 $V_{(BR)CES} = 40$ Vdc (Min) @ $I_C = 100$ μ Adc
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.5$ Vdc @ $I_C = 1.0$ Adc
- Monolithic Construction for High Reliability
- Complement to PNP MPS-U95

**NPN SILICON
DARLINGTON
TRANSISTOR**



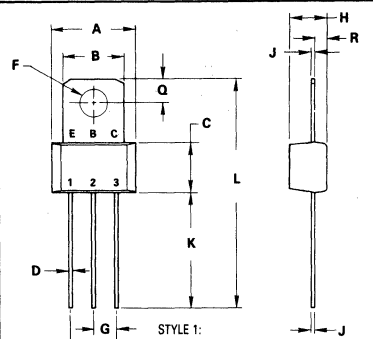
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(1)}$	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	12	Vdc
Collector Current	I_C	2.0	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C}/\text{W}$

(1) Due to the monolithic construction of this device, breakdown voltages of both transistor elements are identical. $V_{(BR)CES}$ is tested in lieu of $V_{(BR)CEO}$ in order to avoid errors caused by noise pickup. The voltage measured during the $V_{(BR)CES}$ test is the $V_{(BR)CEO}$ of the output transistor.



NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MPS-U45

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage ($I_C = 100 \mu\text{A}$, $V_{BE} = 0$)	$V_{(BR)CES}$	40	—	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 100 \mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \mu\text{A}$, $I_C = 0$)	$V_{(BR)EBO}$	12	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 30 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	—	100	nA
Emitter Cutoff Current ($V_{EB} = 10 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	100	nA

ON CHARACTERISTICS(1)

DC Current Gain ($I_C = 200 \text{ mA}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 500 \text{ mA}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 1.0 \text{ A}$, $V_{CE} = 5.0 \text{ Vdc}$)	h_{FE}	25,000 15,000 4,000	65,000 35,000 12,000	150,000 — —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0 \text{ A}$, $I_B = 2.0 \text{ mA}$)	$V_{CE(sat)}$	—	1.2	1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0 \text{ A}$, $I_B = 2.0 \text{ mA}$)	$V_{BE(sat)}$	—	1.85	2.0	Vdc
Base-Emitter On Voltage ($I_C = 1.0 \text{ A}$, $V_{CE} = 5.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.7	2.0	Vdc

DYNAMIC CHARACTERISTICS

Small-Signal Current Gain (1) ($I_C = 200 \text{ mA}$, $V_{CE} = 5.0 \text{ Vdc}$, $f = 100 \text{ MHz}$)	$ h_{fe} $	1.0	3.2	—	—
Collector Base Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	C_{cb}	—	2.5	6.0	pF

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

3

Uni-watt darlington transistors can be used in any number of low power applications, such as relay drivers, motor control and as general purpose amplifiers. As an audio amplifier these devices, when used as a complementary pair, can drive 3.5 watts into a 3.2 ohm speaker using a 14 volt supply with less than one per cent distortion. Because of the high gain the base drive requirement is as low as 1 mA in this application. They are also useful as power drivers for high current application such as voltage regulators.

FIGURE 1 – DC CURRENT GAIN

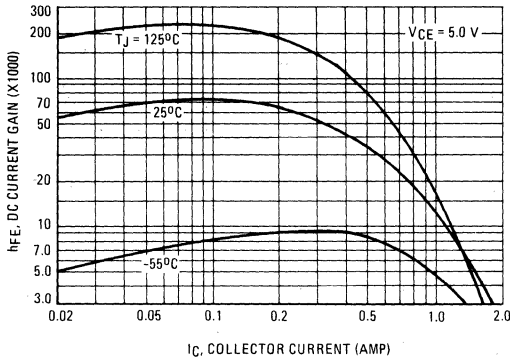


FIGURE 2 – SMALL-SIGNAL CURRENT GAIN

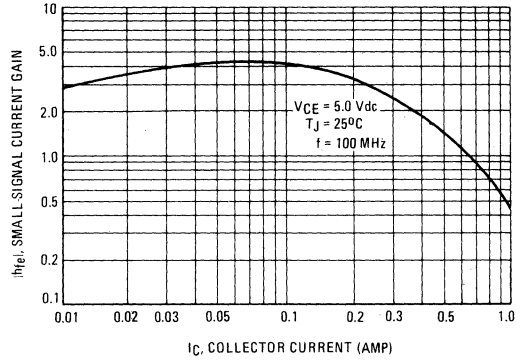


FIGURE 3 – "ON" VOLTAGES

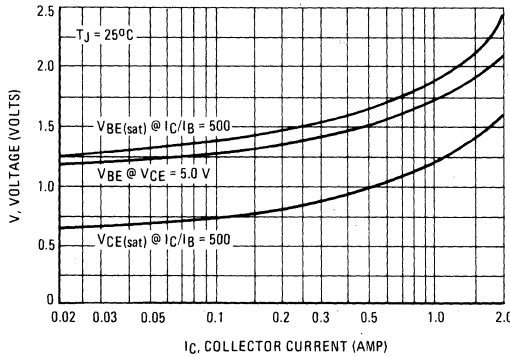
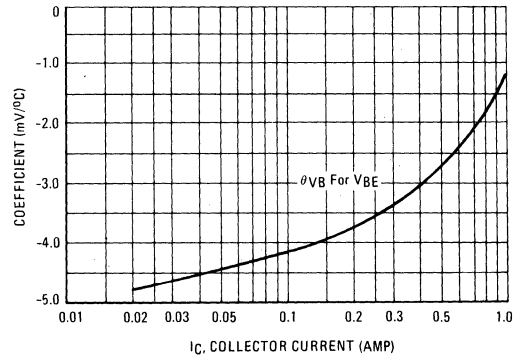
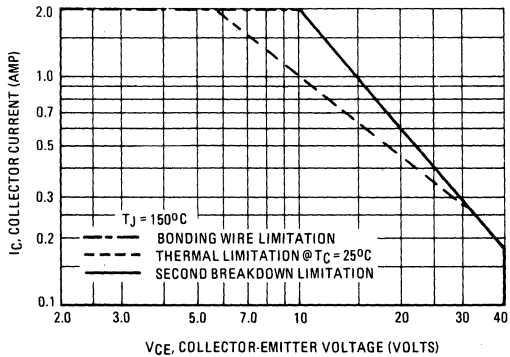


FIGURE 4 – TEMPERATURE COEFFICIENT



3

FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on T_{J(pk)} = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

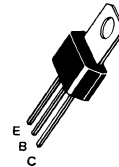
MPS-U51
MPS-U51A

PNP SILICON ANNULAR TRANSISTORS

... designed for complementary symmetry audio circuits to 5 Watts output.

- Excellent Current Gain Linearity – 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)} = 0.7 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Adc}$
- Complements to NPN MPS-U01 and MPS-U01A
- Uniwatt Package for Excellent Thermal Properties – 1.0 Watt @ $T_A = 25^\circ\text{C}$

PNP SILICON
AUDIO TRANSISTORS

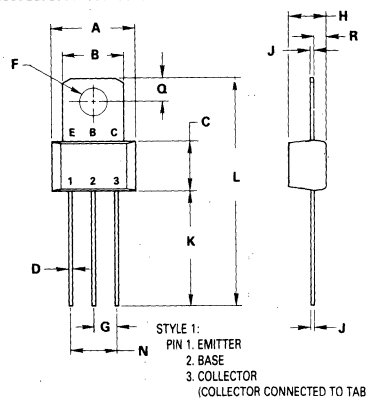


MAXIMUM RATINGS

Rating	Symbol	MPS-U51	MPS-U51A	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Base Voltage	V_{CB}	40	50	Vdc
Emitter-Base Voltage	V_{EB}		5.0	Vdc
Collector Current – Continuous	I_C		2.0	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0	8.0	Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10	80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	$^\circ\text{C/W}$



NOTE:
 1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MPS-U51, MPS-U51A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I _C = 1.0 mA, I _B = 0)	MPS-U51 MPS-U51A	V _{(BR)CEO}	30 40	— —	Vdc
Collector-Base Breakdown Voltage (I _C = 100 μA, I _E = 0)	MPS-U51 MPS-U51A	V _{(BR)CBO}	40 50	— —	Vdc
Emitter-Base Breakdown Voltage (I _E = 100 μA, I _C = 0)		V _{(BR)EBO}	5.0	—	Vdc
Collector Cutoff Current (V _{CB} = 30 Vdc, I _E = 0) (V _{CB} = 40 Vdc, I _E = 0)	MPS-U51 MPS-U51A	I _{CBO}	— —	0.1 0.1	μA
Emitter Cutoff Current (V _{BE} = 3.0 Vdc, I _C = 0)		I _{EBO}	—	0.1	μA
ON CHARACTERISTICS(1)					
DC Current Gain (I _C = 10 mA, V _{CE} = 1.0 Vdc) (I _C = 100 mA, V _{CE} = 1.0 Vdc) (I _C = 1.0 A, V _{CE} = 1.0 Vdc)		h _{FE}	55 60 50	— — —	—
Collector-Emitter Saturation Voltage (I _C = 1.0 A, I _B = 0.1 A)		V _{CE(sat)}	—	0.7	Vdc
Base-Emitter On Voltage (I _C = 1.0 A, V _{CE} = 1.0 Vdc)		V _{BE(on)}	—	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I _C = 50 mA, V _{CE} = 10 Vdc, f = 20 MHz)		f _T	50	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 100 kHz)		C _{ob}	—	30	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

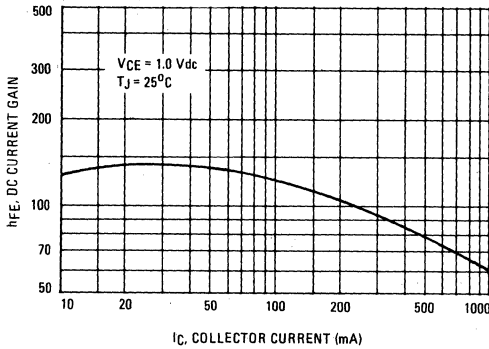


FIGURE 2 — "ON" VOLTAGES

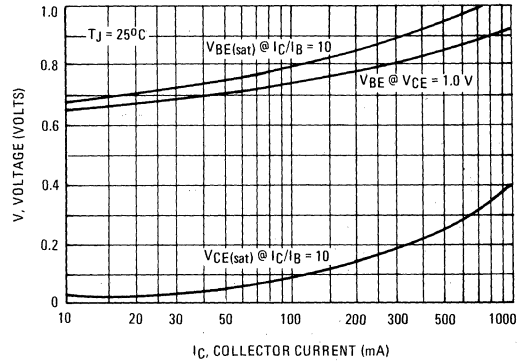
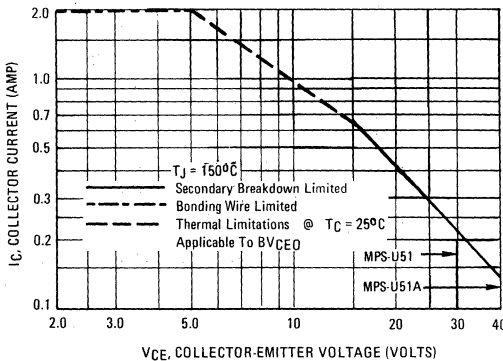


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on T_{J(pk)} = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MPS-U52

PNP SILICON ANNULAR TRANSISTOR

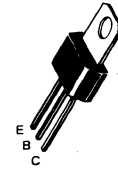
... designed for general-purpose amplifier and driver applications.

- Complement to NPN MPS-U02

**PNP SILICON
AMPLIFIER TRANSISTOR**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current - Continuous	I_C	1.5	A dc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}^{(1)}$	-55 to +150	°C



THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}^{(1)}$	125	C/W

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}, I_B = 0$)	$V_{(BR)CEO}$	40	-	Vdc
Collector-Base Breakdown Voltage ($I_C = 100 \mu\text{Adc}, I_E = 0$)	$V_{(BR)CBO}$	60	-	Vdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}, I_E = 0$)	I_{CBO}	-	100	nAdc

ON CHARACTERISTICS (2)

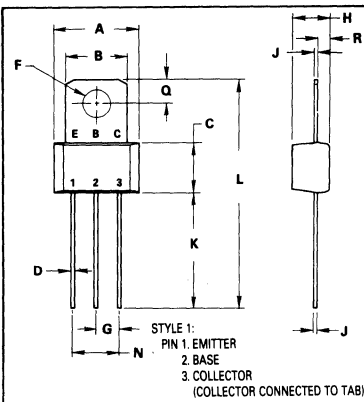
DC Current Gain ($I_C = 10 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$) ($I_C = 150 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}$)	h_{FE}	50 50 30	- 300 -	-
Collector-Emitter Saturation Voltage ($I_C = 150 \text{ mAdc}, I_B = 15 \text{ mAdc}$)	$V_{CE(sat)}$	-	0.4	Vdc
Base-Emitter Saturation Voltage ($I_C = 150 \text{ mAdc}, I_B = 15 \text{ mAdc}$)	$V_{BE(sat)}$	-	1.3	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product (2) ($I_C = 20 \text{ mAdc}, V_{CE} = 20 \text{ Vdc}, f = 100 \text{ MHz}$)	f_T	100	-	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 100 \text{ kHz}$)	C_{ob}	-	24	pF

(1) $R_{\theta JA}$ is measured with device soldered into a typical printed circuit board

(2) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$



NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

FIGURE 1 – DC CURRENT GAIN

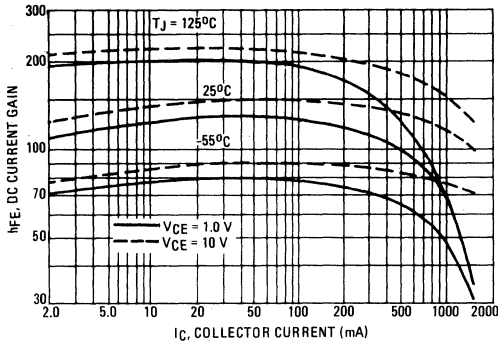


FIGURE 2 – "ON" VOLTAGES

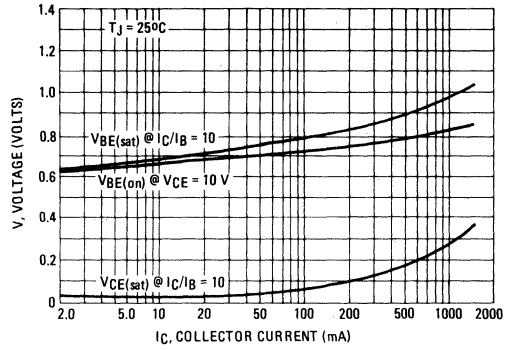


FIGURE 3 – COLLECTOR SATURATION REGION

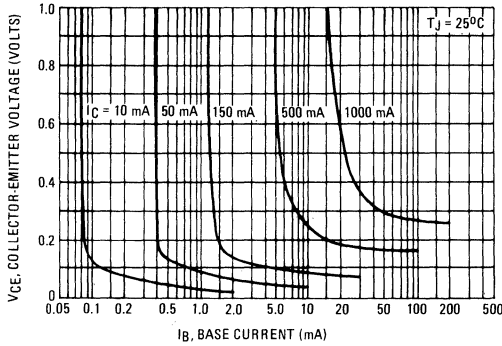


FIGURE 4 – DC SAFE OPERATING AREA

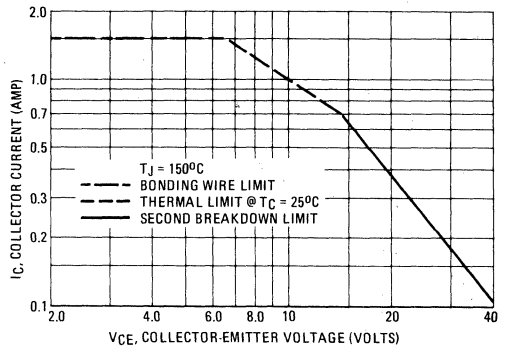


FIGURE 5 – CURRENT-GAIN BANDWIDTH PRODUCT

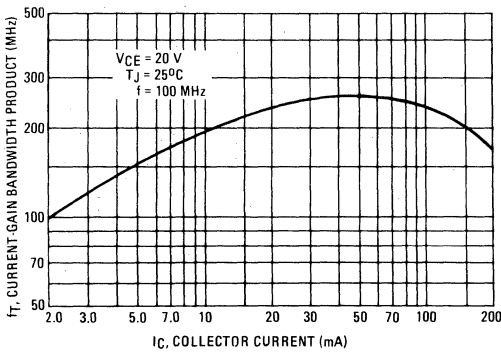
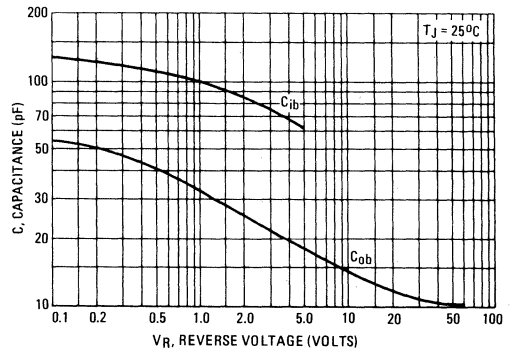


FIGURE 6 – CAPACITANCE



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

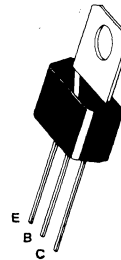
MPS-U55
MPS-U56

**PNP SILICON ANNULAR
AMPLIFIER TRANSISTORS**

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage –
 $V_{(BR)CEO} = 60 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc — MPS-U55}$
 $80 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc — MPS-U56}$
- High Power Dissipation – $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$
- Complements to NPN MPS-U05 and MPS-U06

**PNP SILICON
AMPLIFIER TRANSISTORS**



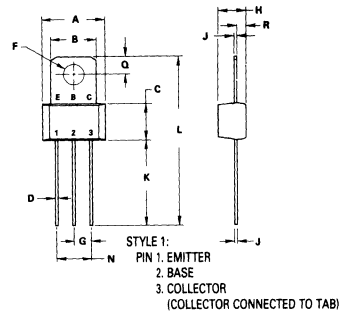
MAXIMUM RATINGS

Rating	Symbol	MPS-U55	MPS-U56	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	2.0		Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0	8.0	Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10	80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA(1)}$	125	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C/W}$

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MPS-U55, MPS-U56

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ⁽¹⁾ (I _C = 1.0 mA, I _B = 0)	V _{(BR)CEO}	60 80	—	—	Vdc
Emitter-Base Breakdown Voltage (I _E = 100 μA, I _C = 0)	V _{(BR)EBO}	4.0	—	—	Vdc
Collector Cutoff Current (V _{CB} = 40 Vdc, I _E = 0) (V _{CB} = 60 Vdc, I _E = 0)	I _{CBO}	— —	—	100 100	nA _{dc}
ON CHARACTERISTICS					
DC Current Gain (1) (I _C = 50 mA, V _{CE} = 1.0 Vdc) (I _C = 250 mA, V _{CE} = 1.0 Vdc) (I _C = 500 mA, V _{CE} = 1.0 Vdc)	h _{FE}	80 50 —	160 130 80	— — —	—
Collector-Emitter Saturation Voltage(1) (I _C = 250 mA, I _B = 10 mA) (I _C = 250 mA, I _B = 25 mA)	V _{CE(sat)}	— —	0.22 0.15	0.5 —	Vdc
Base-Emitter On Voltage (1) (I _C = 250 mA, V _{CE} = 5.0 Vdc)	V _{BE(on)}	—	0.78	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain-Bandwidth Product (1) (I _C = 250 mA, V _{CE} = 5.0 Vdc, f = 100 MHz)	f _T	50	100	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 100 kHz)	C _{ob}	—	10	15	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

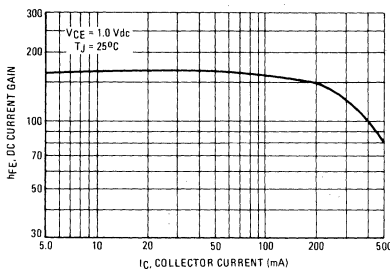


FIGURE 2 — "ON" VOLTAGES

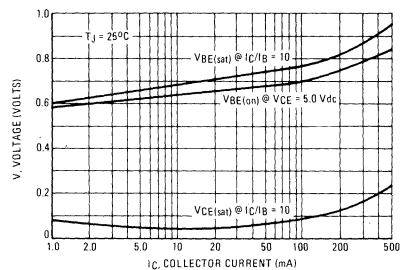


FIGURE 3 — ACTIVE-REGION SAFE OPERATING AREA

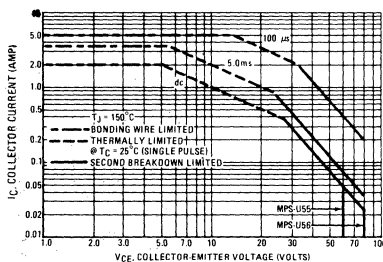
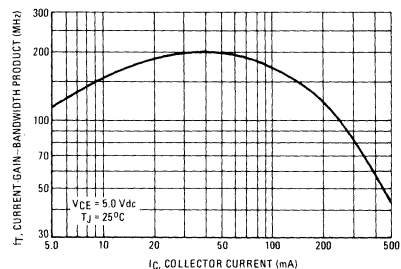


FIGURE 4 — CURRENT-GAIN-BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on T_{J(pk)} = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

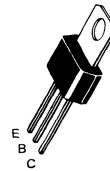
MPS-U57

**PNP SILICON ANNULAR
 AMPLIFIER TRANSISTOR**

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage –
 $V_{(BR)CEO} = 100 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc}$
- High Power Dissipation – $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$
- Complement to NPN MPS-U07

**AMPLIFIER TRANSISTOR
 PNP SILICON**

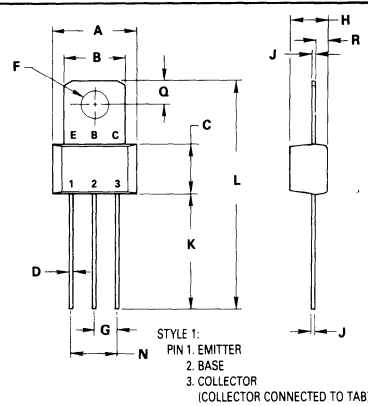


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	2.0	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	$^\circ\text{C/W}$



NOTE:
 1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0 \text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	100	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_C = 100 \mu\text{Adc}$, $I_E = 0$)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	—	100	nAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 50 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 250 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$)	h_{FE}	60 30 —	140 65 30	— — —	—
Collector-Emitter Saturation Voltage ($I_C = 250 \text{ mAdc}$, $I_B = 10 \text{ mAdc}$) ($I_C = 250 \text{ mAdc}$, $I_B = 25 \text{ mAdc}$)	$V_{CE(sat)}$	— —	0.24 0.15	0.5 —	Vdc
Base-Emitter On Voltage ($I_C = 250 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$)	$V_{BE(on)}$	—	0.78	1.2	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product (1) ($I_C = 250 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$, $f = 100 \text{ MHz}$)	f_T	50	100	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 100 \text{ kHz}$)	C_{ob}	—	10	15	pF

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

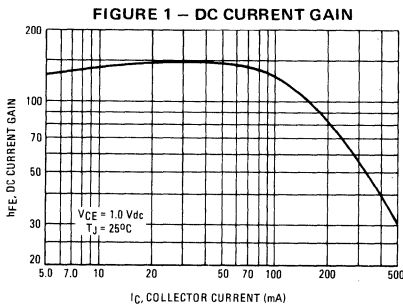


FIGURE 1 - DC CURRENT GAIN

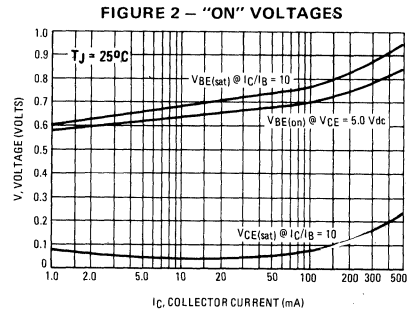


FIGURE 2 - "ON" VOLTAGES

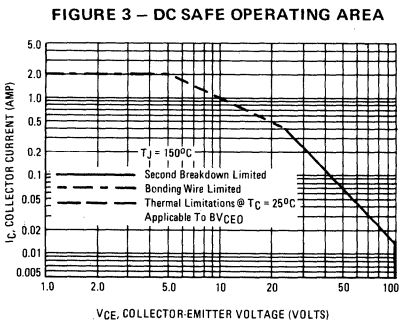
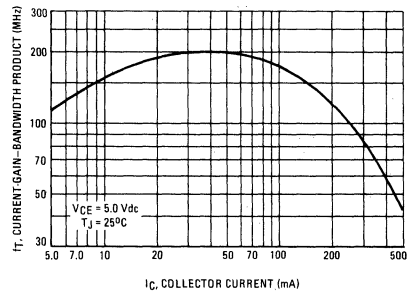


FIGURE 3 - DC SAFE OPERATING AREA

FIGURE 4 - CURRENT-GAIN-BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MPS-U60

PNP SILICON ANNULAR TRANSISTOR

... designed for general-purpose applications requiring high break-down voltages, low saturation voltages and low capacitance.

- Complement to NPN Type MPS-U10

**PNP SILICON
HIGH VOLTAGE
TRANSISTOR**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current - Continuous	I_C	500	mA _{dc}
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}(1)$	125	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage (2) ($I_C = 1.0 \text{ mA}_{dc}, I_B = 0$)	$V_{(BR)CEO}$	300	-	Vdc
Collector-Base Breakdown Voltage ($I_C = 100 \mu\text{A}_{dc}, I_E = 0$)	$V_{(BR)CBO}$	300	-	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \mu\text{A}_{dc}, I_C = 0$)	$V_{(BR)EBO}$	5.0	-	Vdc
Collector Cutoff Current ($V_{CB} = 200 \text{ Vdc}, I_E = 0$)	I_{CBO}	-	0.2	μA_{dc}
Emitter Cutoff Current ($V_{BE} = 3.0 \text{ Vdc}, I_C = 0$)	I_{EBO}	-	0.1	μA_{dc}

ON CHARACTERISTICS

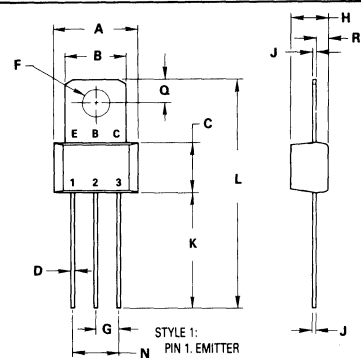
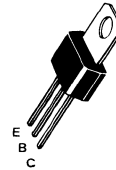
DC Current Gain (2) ($I_C = 1.0 \text{ mA}_{dc}, V_{CE} = 10 \text{ Vdc}$) ($I_C = 10 \text{ mA}_{dc}, V_{CE} = 10 \text{ Vdc}$) ($I_C = 30 \text{ mA}_{dc}, V_{CE} = 10 \text{ Vdc}$)	h_{FE}	25 30 30	-	-
Collector-Emitter Saturation Voltage ($I_C = 20 \text{ mA}_{dc}, I_B = 2.0 \text{ mA}_{dc}$)	$V_{CE(sat)}$	-	0.75	Vdc
Base-Emitter Saturation Voltage ($I_C = 20 \text{ mA}_{dc}, I_B = 2.0 \text{ mA}_{dc}$)	$V_{BE(sat)}$	-	0.9	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain - Bandwidth Product (2) ($I_C = 10 \text{ mA}_{dc}, V_{CE} = 20 \text{ Vdc}, f = 100 \text{ MHz}$)	f_T	60	-	MHz
Collector-Base Capacitance ($V_{CB} = 20 \text{ Vdc}, I_E = 0, f = 1.0 \text{ MHz}$)	C_{cb}	-	8.0	pF

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

(2) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.



STYLE 1:
1. PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm (0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

FIGURE 1 – DC CURRENT GAIN

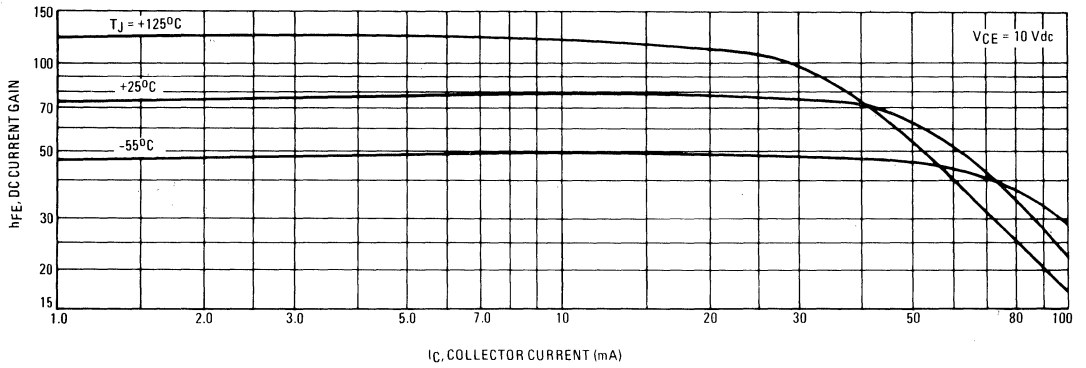


FIGURE 2 – CAPACITANCES

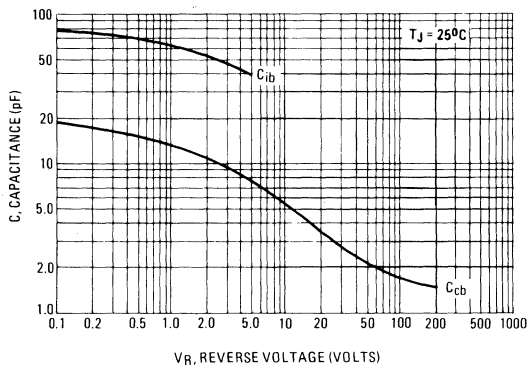


FIGURE 3 – CURRENT-GAIN-BANDWIDTH PRODUCT

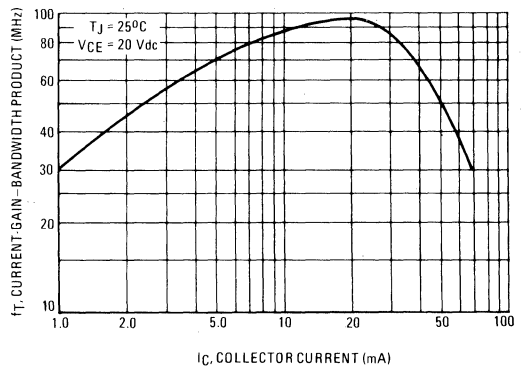


FIGURE 4 – "ON" VOLTAGES

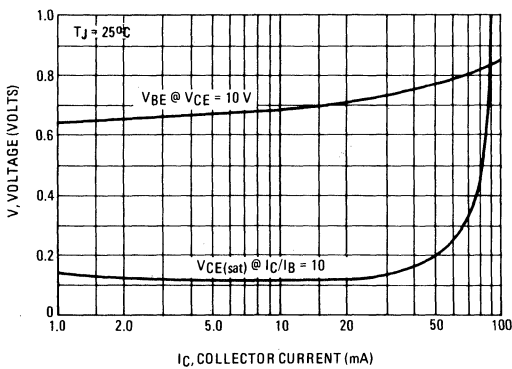
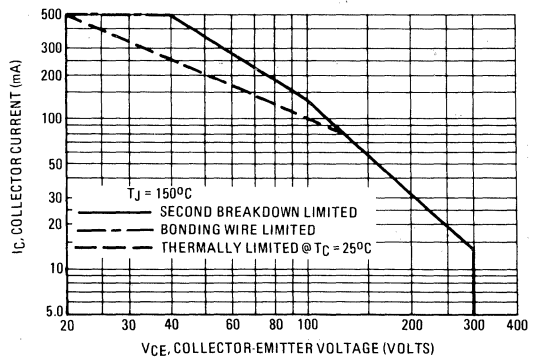


FIGURE 5 – DC SAFE OPERATING AREA



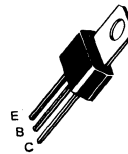
3

**PNP SILICON DARLINGTON
 AMPLIFIER TRANSISTOR**

... designed for amplifier and driver applications.

- High DC Current Gain –
 $h_{FE} = 25,000$ (Min) @ $I_C = 200$ mAdc
 $15,000$ (Min) @ $I_C = 500$ mAdc
- Collector-Emitter Breakdown Voltage –
 $V_{(BR)CES} = 40$ Vdc (Min) @ $I_C = 100$ μ Adc
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.5$ Vdc @ $I_C = 1.0$ Adc
- Monolithic Construction for High Reliability
- Complement to NPN MPS-U45

**PNP SILICON
 DARLINGTON
 TRANSISTOR**



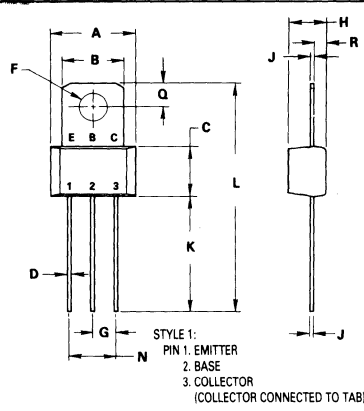
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}^{(1)}$	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current -Continuous	I_C	2.0	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	Watt mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10 80	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA(2)}$	125	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^\circ\text{C}/\text{W}$

- (1) Due to the monolithic construction of this device, breakdown voltages of both transistor elements are identical, $V_{(BR)CES}$ is tested in lieu of $V_{(BR)CEO}$ in order to avoid errors caused by noise pickup. The voltage measured during the $V_{(BR)CES}$ test is the $V_{(BR)CEO}$ of the output transistor.
 (2) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



NOTE:
 1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.86	0.213	0.233
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
Q	5.08 BSC		0.200 BSC	
N	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ($I_C = 100 \mu\text{Adc}$, $V_{BE} = 0$)	$V_{(BR)CES}$	40	—	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 100 \mu\text{Adc}$, $I_E = 0$)	$V_{(BR)CBO}$	50	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	10	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 30 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	—	100	nAdc
Emitter Cutoff Current ($V_{EB} = 8.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	100	nAdc

ON CHARACTERISTICS(1)

DC Current Gain ($I_C = 200 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$)	h_{FE}	25,000 15,000 4,000	43,000 41,000 35,000	150,000 — —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0 \text{ Adc}$, $I_B = 2.0 \text{ mAdc}$)	$V_{CE(sat)}$	—	1.0	1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0 \text{ Adc}$, $I_B = 2.0 \text{ mAdc}$)	$V_{BE(sat)}$	—	1.85	2.0	Vdc
Base-Emitter On Voltage ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.7	2.0	Vdc

DYNAMIC CHARACTERISTICS

Small-Signal Current Gain (1) ($I_C = 200 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$, $f = 100 \text{ MHz}$)	$ h_{fe} $	0.5	1.6	—	—
Collector Base Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	C_{cb}	—	2.5	12	pF

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Uni watt Darlington transistors can be used in any number of low power applications, such as relay drivers, motor control and as general purpose amplifiers. As an audio amplifier these devices, when used as a complementary pair, can drive 3.5 watts into a 3.2 ohm speaker using a 14 volt supply with less than one percent distortion. Because of the high gain the base drive requirement is as low as 1 mA in this application. They are also useful as power drivers for high current application such as voltage regulators.

FIGURE 1 – DC CURRENT GAIN

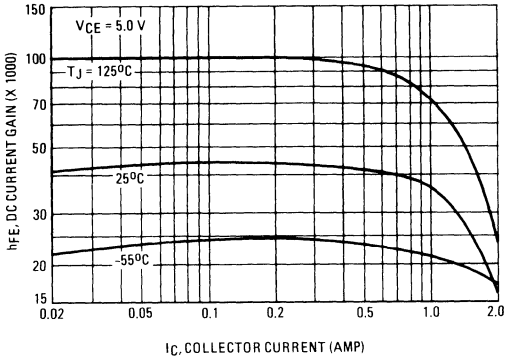


FIGURE 2 – SMALL-SIGNAL CURRENT GAIN

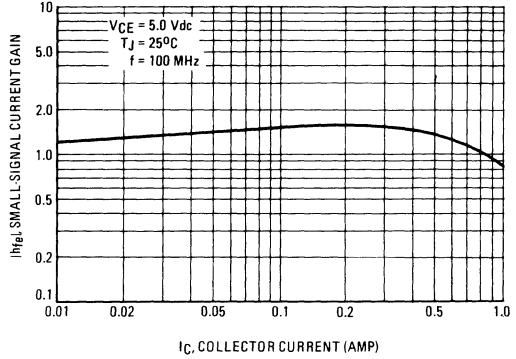


FIGURE 3 – "ON" VOLTAGES

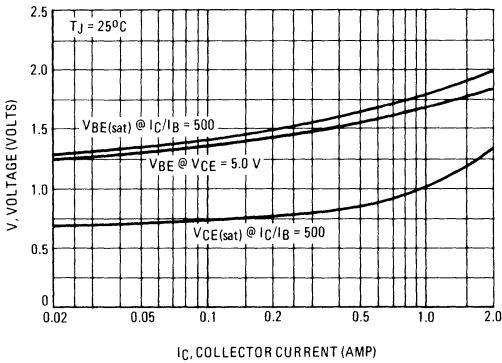


FIGURE 4 – TEMPERATURE COEFFICIENT

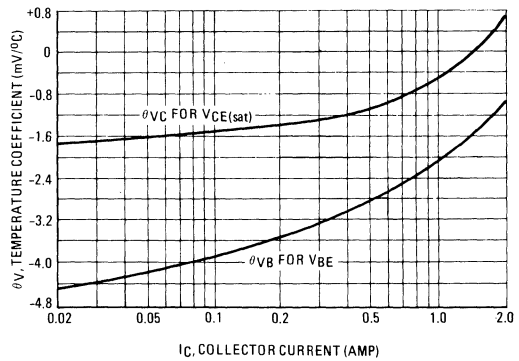
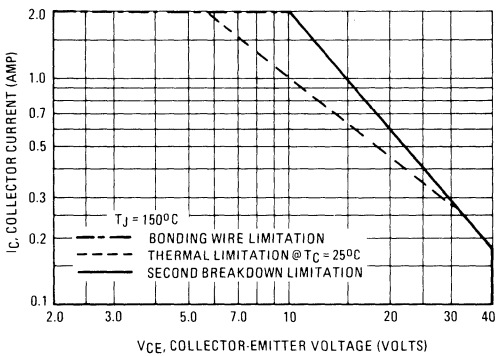


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on T_{J(pk)} = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

NPN
TIP29
TIP29A
TIP29B
TIP29C

PNP
TIP30
TIP30A
TIP30B
TIP30C

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

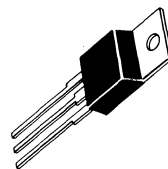
... designed for use in general purpose amplifier and switching applications. Compact TO-220 AB package. TO-66 leadform also available.

1 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON

40-60-80-100 VOLTS
30 WATTS

MAXIMUM RATINGS

Rating	Symbol	TIP29 TIP30	TIP29A TIP30A	TIP29B TIP30B	TIP29C TIP30C	Unit
Collector-Emitter Voltage	V_{CE0}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current - Continuous Peak	I_C	← 1.0 →				Adc
		← 3.0 →				
Base Current	I_B	← 0.4 →				Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 30 →				Watts W/ $^\circ\text{C}$
		← 0.24 →				
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	← 2.0 →				Watts W/ $^\circ\text{C}$
		← 0.016 →				
Unclamped Inductive Load Energy (See Note 3)	E	← 32 →				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →				$^\circ\text{C}$



THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.167	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 30 \text{ mA}, I_B = 0$)	TIP29, TIP30 TIP29A, TIP30A TIP29B, TIP30B TIP29C, TIP30C	$V_{CE0(sus)}$	40 60 80 100	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}, I_B = 0$) ($V_{CE} = 60 \text{ Vdc}, I_B = 0$)	TIP29, TIP29A, TIP30, TIP30A TIP29B, TIP29C, TIP30B, TIP30C	I_{CEO}	— — 0.3	mAdc
Collector Cutoff Current ($V_{CE} = 40 \text{ Vdc}, V_{EB} = 0$) ($V_{CE} = 60 \text{ Vdc}, V_{EB} = 0$) ($V_{CE} = 80 \text{ Vdc}, V_{EB} = 0$) ($V_{CE} = 100 \text{ Vdc}, V_{EB} = 0$)	TIP29, TIP30 TIP29A, TIP30A TIP29B, TIP30B TIP29C, TIP30C	I_{CES}	— — 200 200	μAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}, I_C = 0$)		I_{EBO}	— 1.0	mAdc

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 0.2 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	40 15	— 75	—
Collector-Emitter Saturation Voltage ($I_C = 1.0 \text{ Adc}, I_B = 125 \text{ mA}$)	$V_{CE(sat)}$	—	0.7	Vdc
Base-Emitter On Voltage ($I_C = 1.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.3	Vdc

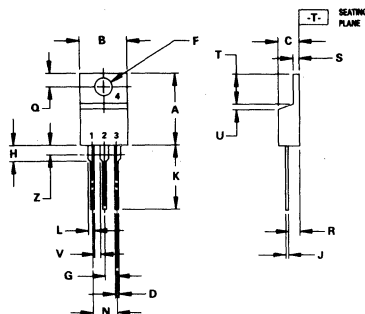
DYNAMIC CHARACTERISTICS

Current Gain - Bandwidth Product (2) ($I_C = 200 \text{ mA}, V_{CE} = 10 \text{ Vdc}, f_{test} = 1 \text{ MHz}$)	f_T	3.0	—	MHz
Small-Signal Current Gain ($I_C = 0.2 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 1 \text{ kHz}$)	h_{fe}	20	—	—

(1) Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.

(2) $f_T = h_{FE} \cdot f_{test}$

(3) This rating based on testing with $L_C = 20 \text{ mH}$, $R_{BE} = 100 \Omega$, $V_{CC} = 10 \text{ V}$, $I_C = 1.8 \text{ A}$, P.R.F. = 10 Hz.



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.406
C	4.07	4.82	0.160	0.190
D	0.94	0.96	0.025	0.035
F	3.91	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
V	0.00	1.27	0.000	0.050
W	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

STYLE 1:

- PIN 1: BASE
- COLLECTOR
- EMITTER
- COLLECTOR

TIP29, TIP29A, TIP29B, TIP29C, NPN, TIP30, TIP30A, TIP30B, TIP30C, PNP

FIGURE 1 – DC CURRENT GAIN

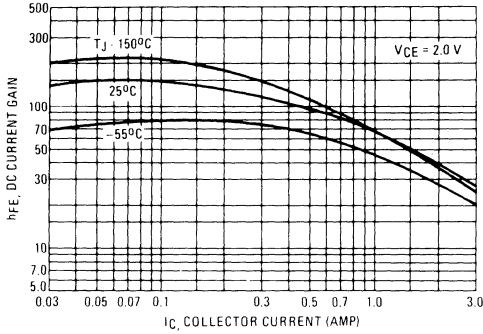


FIGURE 2 – TURN-OFF TIME

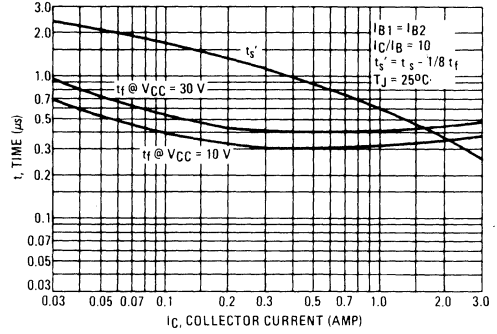


FIGURE 3 – SWITCHING TIME EQUIVALENT CIRCUIT

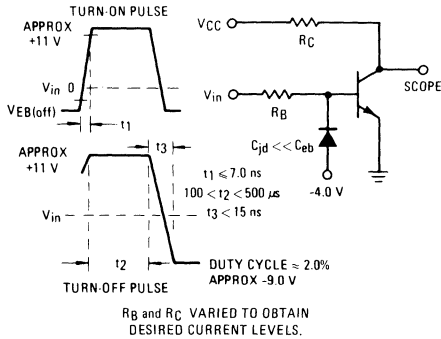


FIGURE 4 – TURN-ON TIME

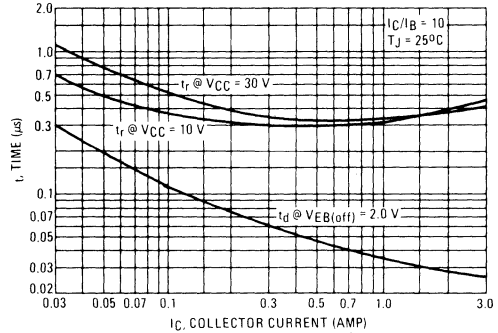
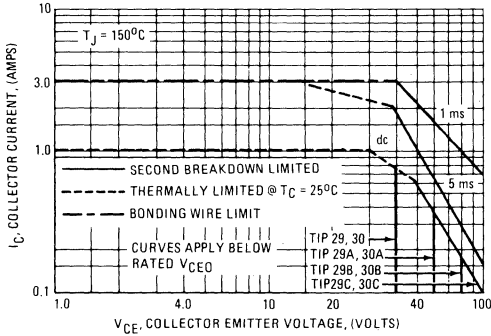


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN
TIP31
TIP31A
TIP31B
TIP31C

PNP
TIP32
TIP32A
TIP32B
TIP32C

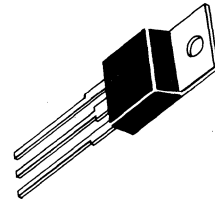
**COMPLEMENTARY SILICON PLASTIC
POWER TRANSISTORS**

... designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.2 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- Collector-Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 40 \text{ Vdc (Min) – TIP31, TIP 32}$
 $= 60 \text{ Vdc (Min) – TIP31A, TIP32A}$
 $= 80 \text{ Vdc (Min) – TIP31B, TIP32B}$
 $= 100 \text{ Vdc (Min) – TIP31C, TIP32C}$
- High Current Gain – Bandwidth Product
 $f_T = 3.0 \text{ MHz (Min) @ } I_C = 500 \text{ mAdc}$
- Compact TO-220 AB Package
- TO-66 Leadform Also Available

**3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON**

**40-60-80-100 VOLTS
40 WATTS**



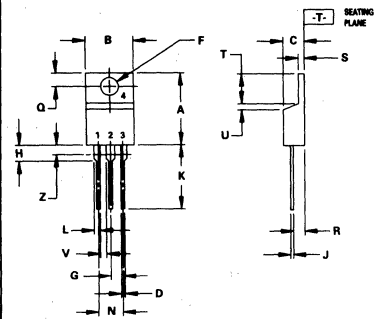
***MAXIMUM RATINGS**

Rating	Symbol	TIP31 TIP32	TIP31A TIP32A	TIP31B TIP32B	TIP31C TIP32C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous Peak	I_C	3.0				A dc
		5.0				A dc
Base Current	I_B	1.0				A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40				Watts
		0.32				W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0				Watts
		0.016				W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (1)	E	32				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

(1) $I_C = 1.8 \text{ A}$, $L = 20 \text{ mH}$, P.R.F. = 10 Hz, $V_{CC} = 10 \text{ V}$, $R_{BE} = 100 \Omega$.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.90	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.38	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.75	0.080	0.110
S	1.15	1.38	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 1:
PIN 1: BASE
2: COLLECTOR
3: EMITTER
4: COLLECTOR

**CASE 221A-04
TO-220AB**

TIP31, TIP31A, TIP31B, TIP31C, NPN, TIP32, TIP32A, TIP32B, TIP32C, PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 30 mA, I _B = 0)	TIP31, TIP32 TIP31A, TIP32A TIP31B, TIP32B TIP31C, TIP32C	V _{CEO(sus)}	40 60 80 100	Vdc
Collector Cutoff Current (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 60 Vdc, I _B = 0)	TIP31, TIP31A, TIP32, TIP32A TIP31B, TIP31C, TIP32B, TIP32C	I _{CEO}	— 0.3 0.3	mA
Collector Cutoff Current (V _{CE} = 40 Vdc, V _{EB} = 0) (V _{CE} = 60 Vdc, V _{EB} = 0) (V _{CE} = 80 Vdc, V _{EB} = 0) (V _{CE} = 100 Vdc, V _{EB} = 0)	TIP31, TIP32 TIP31A, TIP32A TIP31B, TIP32B TIP31C, TIP32C	I _{CES}	— 200 200 200	μA
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)		I _{EBO}	—	1.0 mA
ON CHARACTERISTICS (1)				
DC Current Gain (I _C = 1.0 A, V _{CE} = 4.0 Vdc) (I _C = 3.0 A, V _{CE} = 4.0 Vdc)		h _{FE}	25 10	—
Collector-Emitter Saturation Voltage (I _C = 3.0 A, I _B = 375 mA)		V _{CE(sat)}	—	1.2 Vdc
Base-Emitter On Voltage (I _C = 3.0 A, V _{CE} = 4.0 Vdc)		V _{BE(on)}	—	1.8 Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (2) (I _C = 500 mA, V _{CE} = 10 Vdc, f _{test} = 1 MHz)		f _T	3.0	— MHz
Small-Signal Current Gain (I _C = 0.5 A, V _{CE} = 10 Vdc, f = 1 kHz)		h _{fe}	20	—

- (1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
 (2) f_T = |h_{fe}| • f_{test}

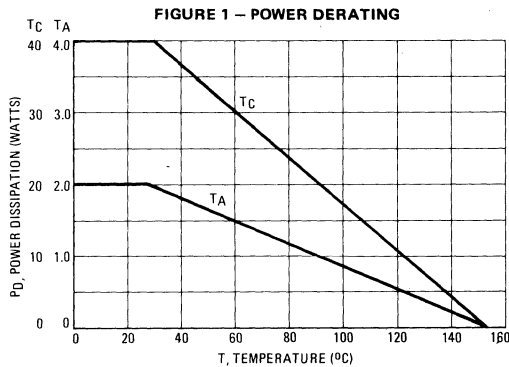


FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

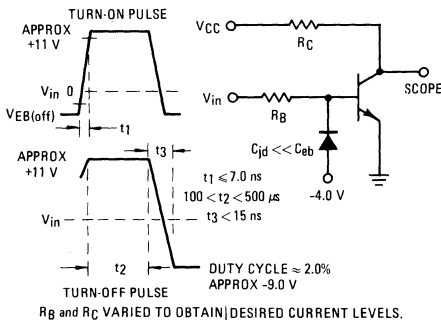
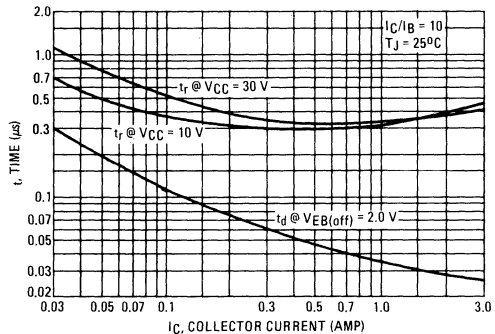


FIGURE 3 – TURN-ON TIME



TIP31, TIP31A, TIP31B, TIP31C, NPN, TIP32, TIP32A, TIP32B, TIP32C, PNP

FIGURE 4 – THERMAL RESPONSE

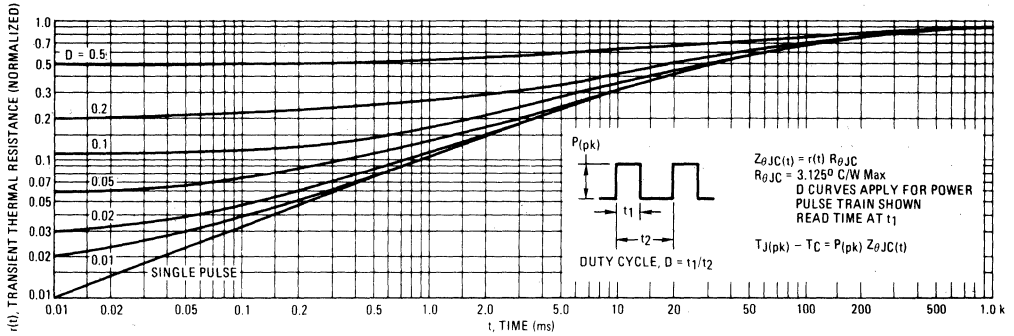
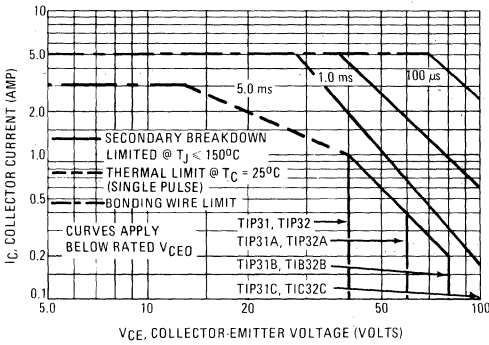


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

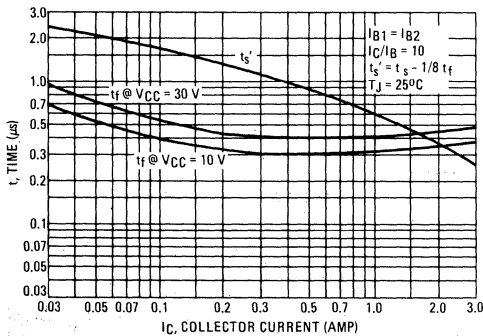
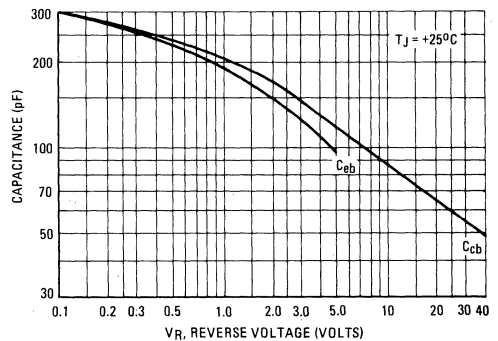


FIGURE 7 – CAPACITANCE



3

TIP31, TIP31A, TIP31B, TIP31C, NPN, TIP32, TIP32A, TIP32B, TIP32C, PNP

FIGURE 8 – DC CURRENT GAIN

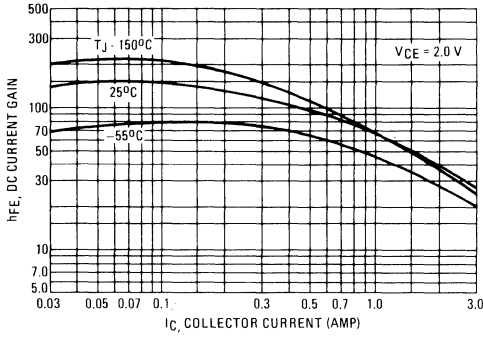


FIGURE 9 – COLLECTOR SATURATION REGION

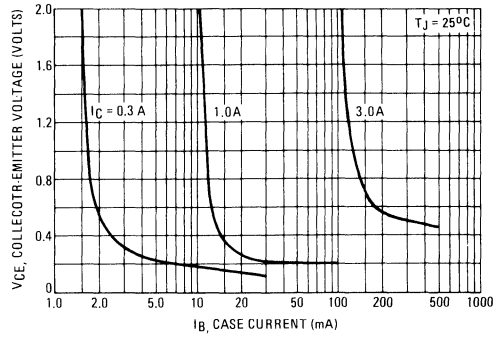


FIGURE 10 – "ON" VOLTAGES

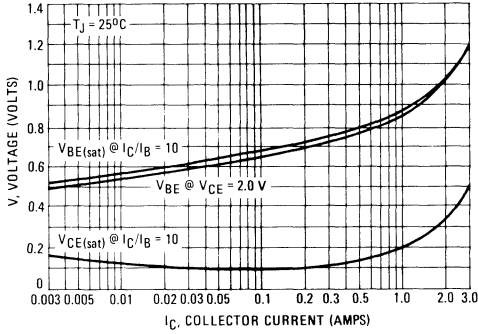


FIGURE 11 – TEMPERATURE COEFFICIENTS

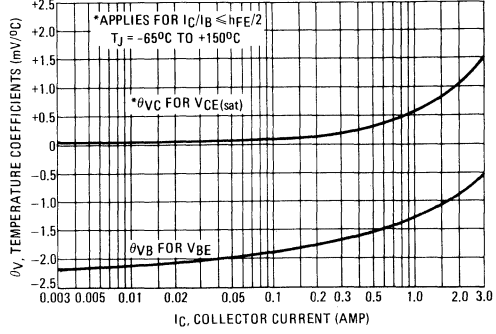


FIGURE 12 – COLLECTOR CUT-OFF REGION

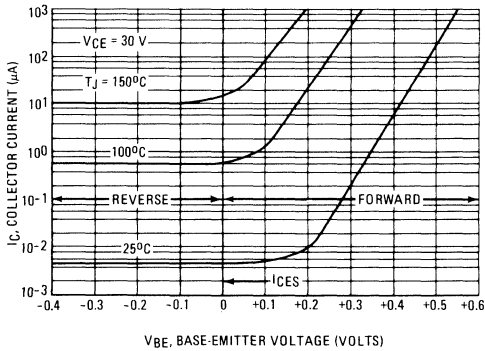
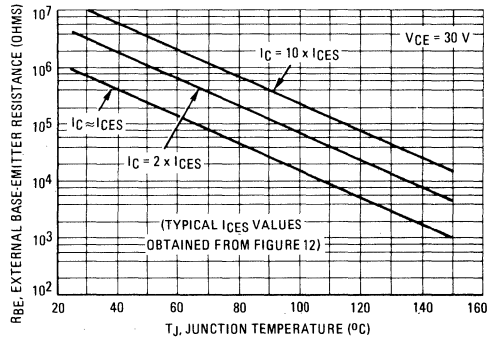


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

NPN
TIP33
TIP33A
TIP33B
TIP33C

PNP
TIP34
TIP34A
TIP34B
TIP34C

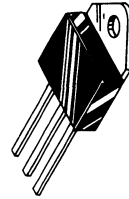
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

... for general-purpose power amplifier and switching applications.

- 10 A Collector Current
- Low Leakage Current — $I_{CEO} = 0.7 \text{ mA}$ @ 30 and 60 V
- Excellent dc Gain — $h_{FE} = 40 \text{ Typ}$ @ 3.0 A
- High Current Gain Bandwidth Product — $h_{fe} = 3.0 \text{ min}$ @ $I_C = 0.5 \text{ A}$, $f = 1.0 \text{ MHz}$

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

40-100 VOLTS
80 WATTS



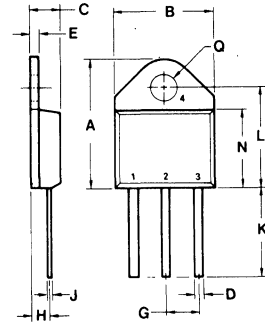
MAXIMUM RATINGS

Rating	Symbol	TIP33 TIP34	TIP33A TIP34A	TIP33B TIP34B	TIP33C TIP34C	Unit
Collector-Emitter Voltage	V_{CEO}	40 V	60 V	80 V	100 V	Vdc
Collector-Base Voltage	V_{CB}	40 V	60 V	80 V	100 V	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current — Continuous	I_C	10				Adc
Peak (1)		15				
Base Current — Continuous	I_B	3.0				Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	80				Watts
		0.64				
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	$^\circ\text{C}/\text{W}$
Junction-To-Free-Air Thermal Resistance	$R_{\theta JA}$	35.7	$^\circ\text{C}/\text{W}$

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle $\leq 10\%$.



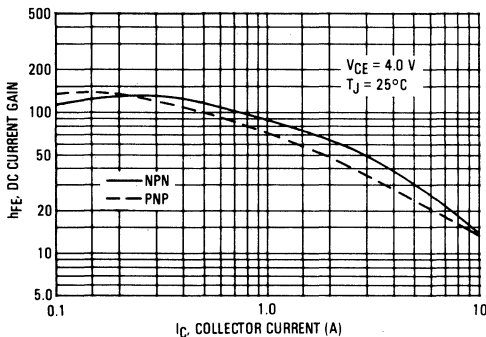
STYLE 1:
1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

3

FIGURE 1 — DC CURRENT GAIN



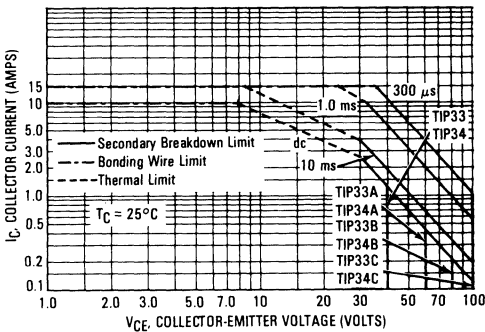
TIP33, TIP33A, TIP33B, TIP33C, TIP34, TIP34A, TIP34B, TIP34C

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 30\text{ mA}$, $I_B = 0$)	TIP33, TIP34 TIP33A, TIP34A TIP33B, TIP34B TIP33C, TIP34C	$V_{CE(sus)}$	40 60 80 100	— — — —	Vdc
Collector-Emitter Cutoff Current ($V_{CE} = 30\text{ V}$, $I_B = 0$) ($V_{CE} = 60\text{ V}$, $I_B = 0$)	TIP33, TIP33A, TIP34, TIP34A TIP33B, TIP33C, TIP34B, TIP34C	I_{CEO}	— —	— 0.7 0.7	mA
Collector-Emitter Cutoff Current ($V_{CE} = \text{Rated } V_{CE}$, $V_{EB} = 0$)		I_{CES}	—	0.4	mA
Emitter-Base Cutoff Current ($V_{EB} = 5.0\text{ V}$, $I_C = 0$)		I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 1.0\text{ A}$, $V_{CE} = 4.0\text{ V}$) ($I_C = 3.0\text{ A}$, $V_{CE} = 4.0\text{ V}$)		h_{FE}	40 20	— 100	—
Collector-Emitter Saturation Voltage ($I_C = 3.0\text{ A}$, $I_B = 0.3\text{ A}$) ($I_C = 10\text{ A}$, $I_B = 2.5\text{ A}$)		$V_{CE(sat)}$	— —	1.0 4.0	Vdc
Base-Emitter On Voltage ($I_C = 3.0\text{ A}$, $V_{CE} = 4.0\text{ V}$) ($I_C = 10\text{ A}$, $V_{CE} = 4.0\text{ V}$)		$V_{BE(on)}$	— —	1.6 3.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 0.5\text{ A}$, $V_{CE} = 10\text{ V}$, $f = 1.0\text{ kHz}$)		h_{fe}	20	—	—
Current-Gain—Bandwidth Product (2) ($I_C = 0.5\text{ A}$, $V_{CE} = 10\text{ V}$, $f = 1.0\text{ MHz}$)		f_T	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.
 (2) $f_T = [h_{fe}] \cdot f_{test}$

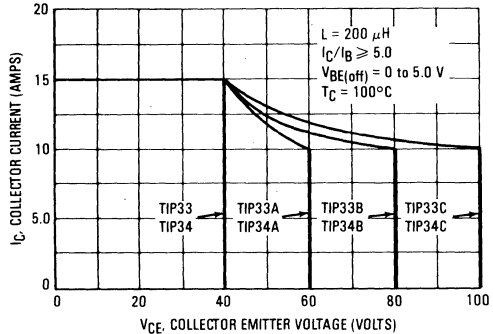
FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



FORWARD BIAS

The Forward Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during forward bias. The data is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%, and must be derated thermally for $T_C > 25^\circ\text{C}$.

FIGURE 3 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



REVERSE BIAS

The Reverse Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during reverse biased turn-off. This rating is verified under clamped conditions so the device is never subjected to an avalanche mode.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

NPN	PNP
TIP35	TIP36
TIP35A	TIP36A
TIP35B	TIP36B
TIP35C	TIP36C

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

... for general-purpose power amplifier and switching applications.

- 25 A Collector Current
- Low Leakage Current — $I_{CEO} = 1.0 \text{ mA}$ @ 30 and 60 V
- Excellent dc Gain — $h_{FE} = 40 \text{ Typ}$ @ 15 A
- High Current Gain Bandwidth Product — $(h_{fe} = 3.0 \text{ min})$ @ $I_C = 1.0 \text{ A}$, $f = 1.0 \text{ MHz}$

25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

40-100 VOLTS
125 WATTS

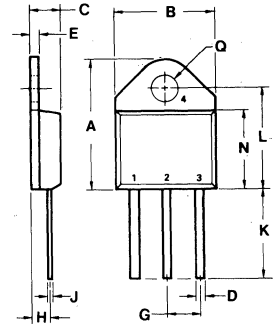
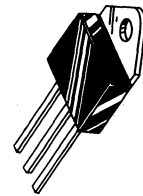
MAXIMUM RATINGS

Rating	Symbol	TIP35 TIP36	TIP35A TIP36A	TIP35B TIP36B	TIP35C TIP36C	Unit
Collector-Emitter Voltage	V_{CEO}	40 V	60 V	80 V	100 V	Vdc
Collector-Base Voltage	V_{CB}	40 V	60 V	80 V	100 V	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current — Continuous Peak (1)	I_C	25				Adc
Base Current — Continuous	I_B	5.0				Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	125				Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				$^\circ\text{C}$
Unclamped Inductive Load	E_{SB}	90				mJ

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C}/\text{W}$
Junction-To-Free-Air Thermal Resistance	$R_{\theta JA}$	35.7	$^\circ\text{C}/\text{W}$

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle $\leq 10\%$.



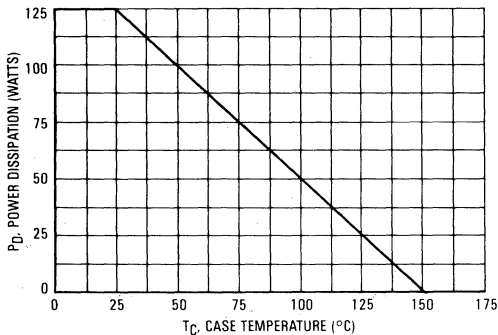
STYLE 1:

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.206	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

FIGURE 1 — POWER DERATING



TIP35, TIP35A, TIP35B, TIP35C, NPN, TIP36, TIP36A, TIP36B, TIP36C, PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

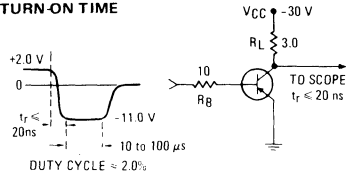
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 30 mA, I _B = 0)	V _{CE(sus)}	40 60 80 100	—	V _{dc}
Collector-Emitter Cutoff Current (V _{CE} = 30 V, I _B = 0)	I _{CEO}	—	1.0	mA
(V _{CE} = 60 V, I _B = 0)		—	1.0	
Collector-Emitter Cutoff Current (V _{CE} = Rated V _{CEO} , V _{EB} = 0)	I _{CES}	—	0.7	mA
Emitter-Base Cutoff Current (V _{EB} = 5.0 V, I _C = 0)	I _{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain (I _C = 1.5 A, V _{CE} = 4.0 V)	h _{FE}	25 15	— 75	—
(I _C = 15 A, V _{CE} = 4.0 V)				
Collector-Emitter Saturation Voltage (I _C = 15 A, I _B = 1.5 A)	V _{CE(sat)}	—	1.8 4.0	V _{dc}
(I _C = 25 A, I _B = 5.0 A)				
Base-Emitter On Voltage (I _C = 15 A, V _{CE} = 4.0 V)	V _{BE(on)}	—	2.0 4.0	V _{dc}
(I _C = 25 A, V _{CE} = 4.0 V)				
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I _C = 1.0 A, V _{CE} = 10 V, f = 1.0 kHz)	h _{fe}	25	—	—
Current-Gain—Bandwidth Product (2) (I _C = 1.0 A, V _{CE} = 10 V, f = 1.0 MHz)	f _T	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

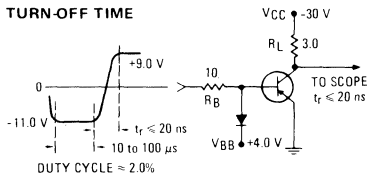
(2) f_T = [h_{fe}] · f_{test}

FIGURE 2 — SWITCHING TIME EQUIVALENT TEST CIRCUITS

TURN-ON TIME



TURN-OFF TIME



FOR CURVES OF FIGURES 3 & 4, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES.

FIGURE 3 — TURN-ON TIME

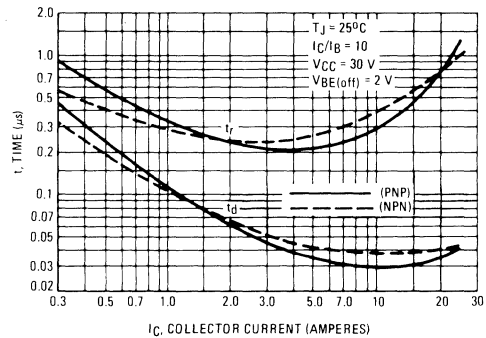


FIGURE 4 — TURN-OFF TIME

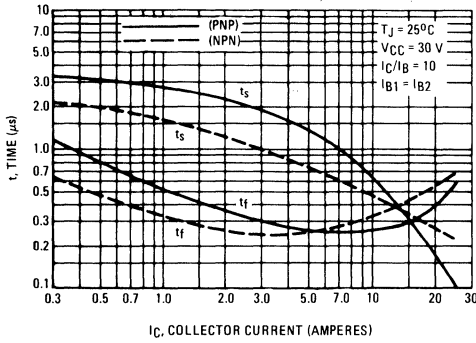
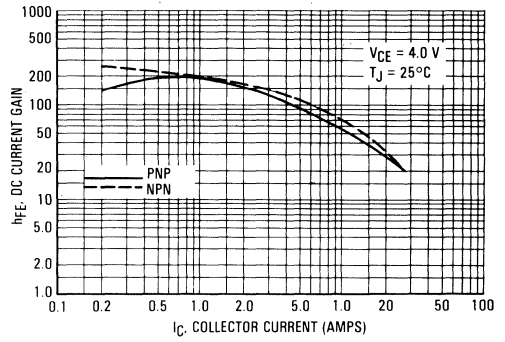


FIGURE 5 — DC CURRENT GAIN

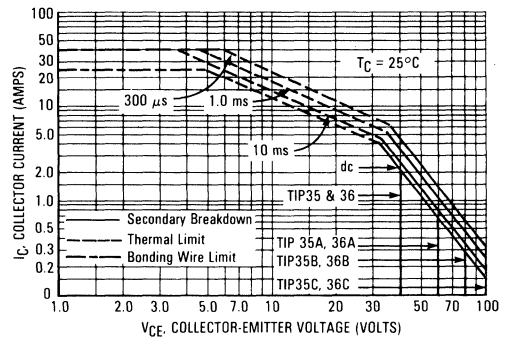


FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on T_C = 25°C; T_{J(pk)} is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C ≥ 25°C. Second breakdown limitations do not derate the same as thermal limitations.

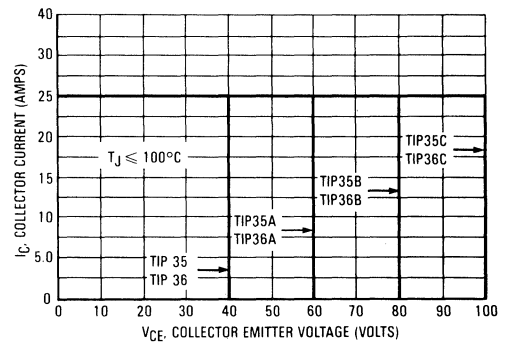
FIGURE 6 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



REVERSE BIAS

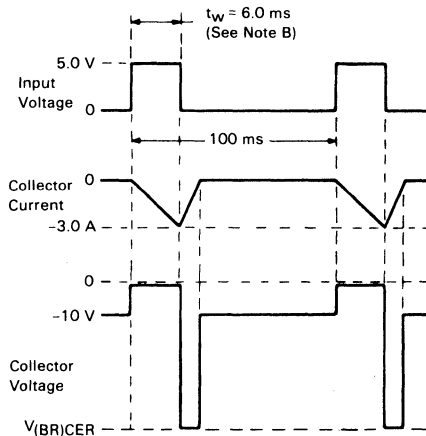
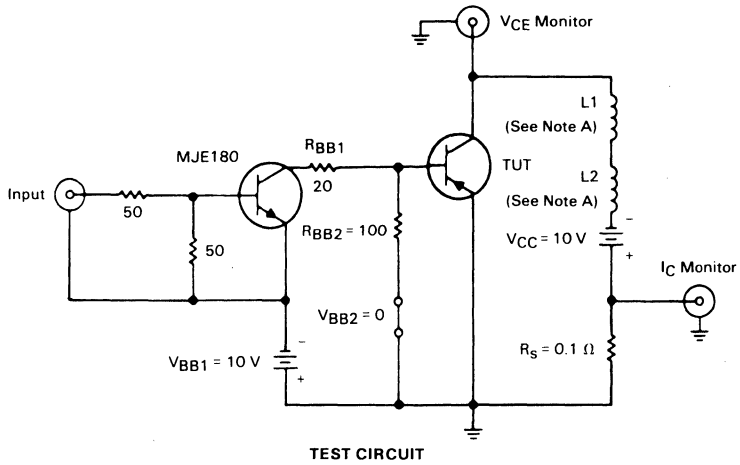
For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.

FIGURE 7 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



3

FIGURE 8 — INDUCTIVE LOAD SWITCHING



VOLTAGE AND CURRENT WAVEFORMS

NOTES:

- A. L1 and L2 are 10 mH, 0.11 Ω , Chicago Standard Transformer Corporation C-2688, or equivalent.
- B. Input pulse width is increased until $I_{CM} = -3.0$ A.
- C. For NPN, reverse all polarities.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

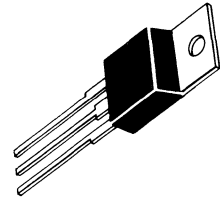
NPN TIP41 TIP41A TIP41B TIP41C	PNP TIP42 TIP42A TIP42B TIP42C
--	--

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

... designed for use in general purpose amplifier and switching applications.

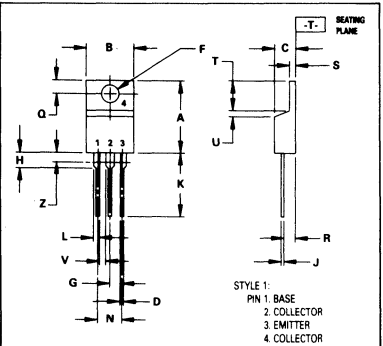
- Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.5 \text{ Vdc (Max) @ } I_C = 6.0 \text{ Adc}$
- Collector-Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 40 \text{ Vdc (Min) – TIP41, TIP42}$
 $= 60 \text{ Vdc (Min) – TIP41A, TIP42A}$
 $= 80 \text{ Vdc (Min) – TIP41B, TIP42B}$
 $= 100 \text{ Vdc (Min) – TIP41C, TIP42C}$
- High Current Gain – Bandwidth Product
 $f_T = 3.0 \text{ MHz (Min) @ } I_C = 500 \text{ mAdc}$
- Compact TO-220AB Package
- TO-66 Leadform Also Available

**6 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
40-60-80-100 VOLTS
65 WATTS**



*MAXIMUM RATINGS

Rating	Symbol	TIP41 TIP42	TIP41A TIP42A	TIP41B TIP42B	TIP41C TIP42C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous Peak	I_C	6				Adc
		10				
Base Current	I_B	2.0				Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	65				Watts W/ $^\circ\text{C}$
		0.52				
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0				Watts W/ $^\circ\text{C}$
		0.016				
Unclamped Inductive Load Energy (1)	E	62.5				mJ
Operating and Storage Junction Temperature Range	$T_{J,Tstg}$	-65 to +150				$^\circ\text{C}$



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.
 - DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

**CASE 221A-04
TO-220AB**

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

(1) $I_C = 2.5 \text{ A}$, $L = 20 \text{ mH}$, P.R.F. = 10 Hz, $V_{CC} = 10 \text{ V}$, $R_{BE} = 100 \Omega$.

TIP41, TIP41A, TIP41B, TIP41C, NPN, TIP42, TIP42A, TIP42B, TIP42C, PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I _C = 30 mA, I _B = 0)	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	V _{CEO(sus)}	40 60 80 100	— — — —	V _{dc}
Collector Cutoff Current (V _{CE} = 30 V _{dc} , V _{EB} = 0) (V _{CE} = 60 V _{dc} , I _B = 0)	TIP41, TIP41A, TIP42, TIP42A TIP41B, TIP41C, TIP42B, TIP42C	I _{CEO}	— —	0.7 0.7	mA _{dc}
Collector Cutoff Current (V _{CE} = 40 V _{dc} , V _{EB} = 0) (V _{CE} = 60 V _{dc} , V _{EB} = 0) (V _{CE} = 80 V _{dc} , V _{EB} = 0) (V _{CE} = 100 V _{dc} , V _{EB} = 0)	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	I _{CES}	— — — —	400 400 400 400	μA _{dc}
Emitter Cutoff Current (V _{BE} = 5.0 V _{dc} , I _C = 0)		I _{EBO}	—	1.0	mA _{dc}
ON CHARACTERISTICS (1)					
DC Current Gain (I _C = 0.3 A _{dc} , V _{CE} = 4.0 V _{dc}) (I _C = 3.0 A _{dc} , V _{CE} = 4.0 V _{dc})		h _{FE}	30 15	— 75	—
Collector-Emitter Saturation Voltage (I _C = 6.0 A _{dc} , I _B = 600 mA _{dc})		V _{CE(sat)}	—	1.5	V _{dc}
Base-Emitter On Voltage (I _C = 6.0 A _{dc} , V _{CE} = 4.0 V _{dc})		V _{BE(on)}	—	2.0	V _{dc}
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I _C = 500 mA _{dc} , V _{CE} = 10 V _{dc} , f _{test} = 1 MHz)		f _T	3.0	—	MHz
Small-Signal Current Gain (I _C = 0.5 A _{dc} , V _{CE} = 10 V _{dc} , f = 1 kHz)		h _{fe}	20	—	—

(1) Pulse Test: Pulswidth ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) f_T = |h_{fe}| • f_{test}

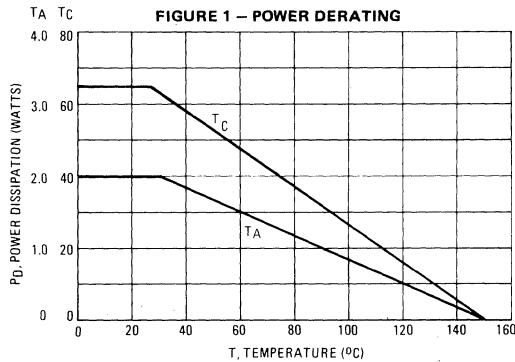


FIGURE 2 — SWITCHING TIME TEST CIRCUIT

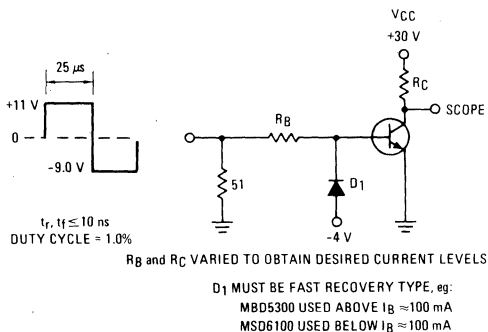


FIGURE 3 — TURN-ON TIME

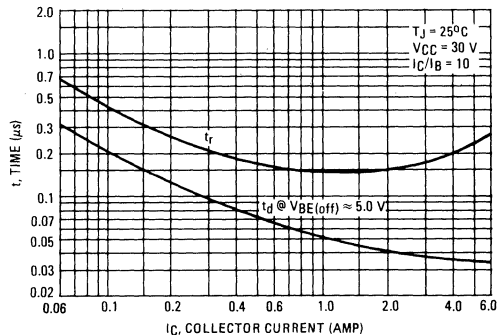


FIGURE 4 – THERMAL RESPONSE

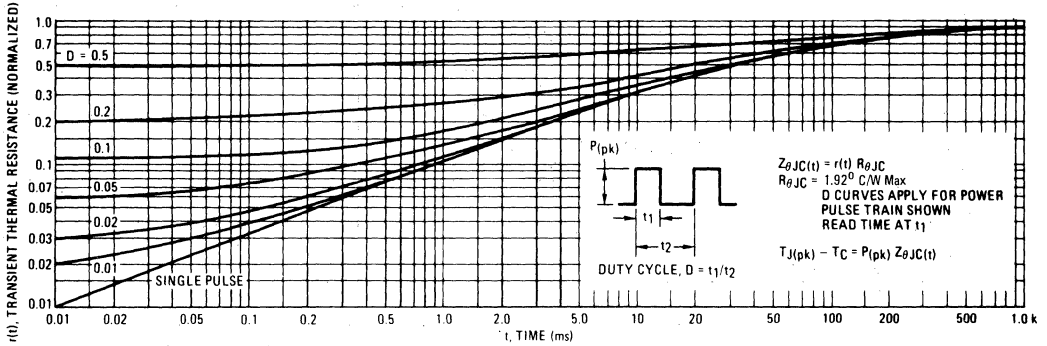
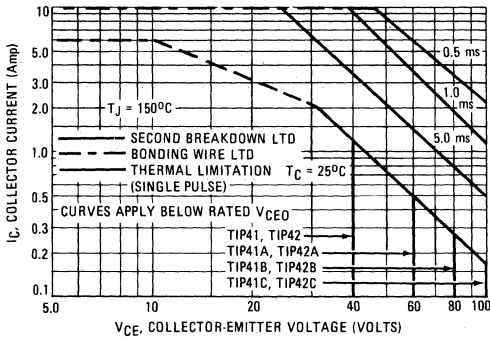


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

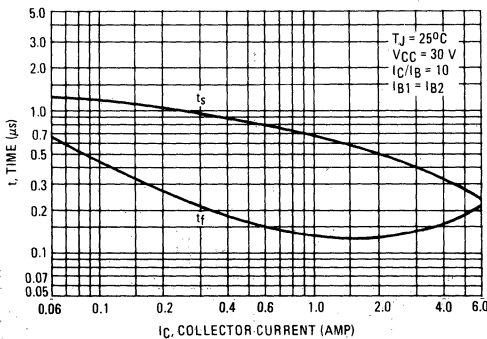
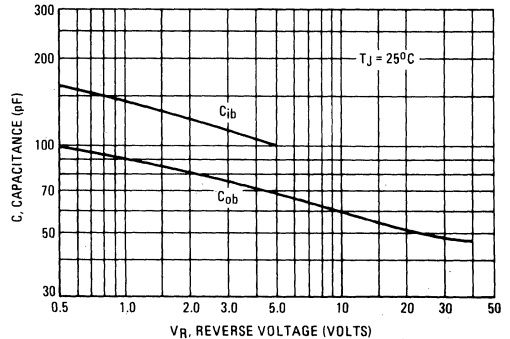


FIGURE 7 – CAPACITANCE



TIP41, TIP41A, TIP41B, TIP41C, NPN, TIP42, TIP42A, TIP42B, TIP42C, PNP

FIGURE 8 – DC CURRENT GAIN

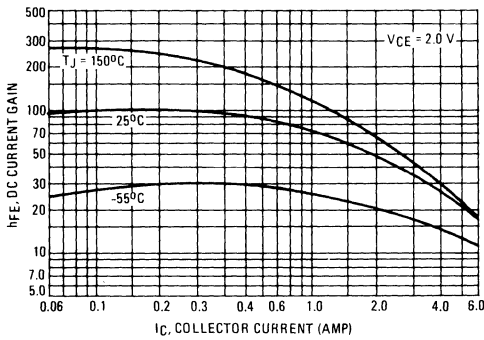


FIGURE 9 – COLLECTOR SATURATION REGION

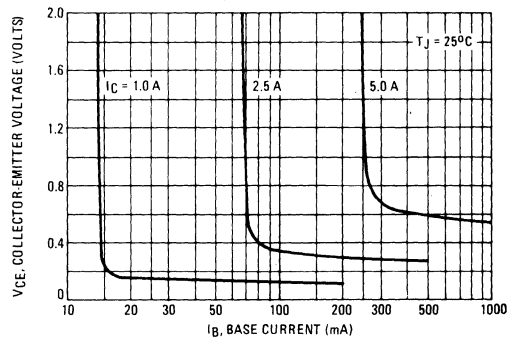


FIGURE 10 – "ON" VOLTAGES

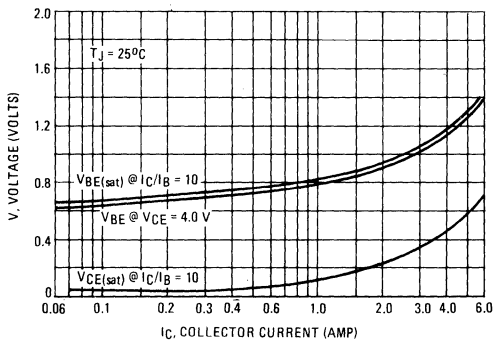


FIGURE 11 – TEMPERATURE COEFFICIENTS

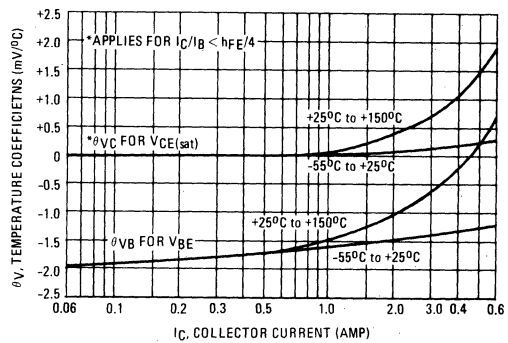


FIGURE 12 – COLLECTOR CUT-OFF REGION

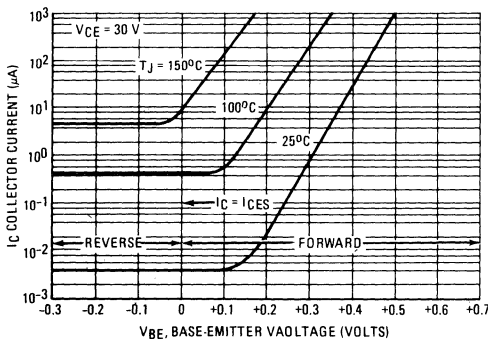
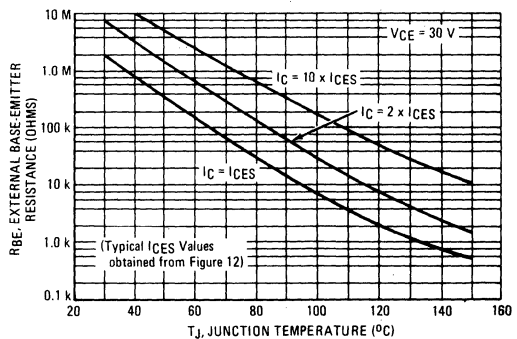


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

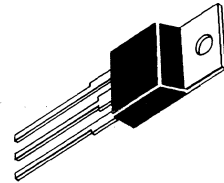
... designed for line operated audio output amplifier, Switchmode power supply drivers and other switching applications.

- 250 V to 400 V (Min) - $V_{CE0(sus)}$
- 1 A Rated Collector Current
- Popular TO-220 Plastic Package
- TO-66 Leadform Available

1.0 AMPERE

POWER TRANSISTORS
NPN SILICON

250-300-350-400 VOLTS
40 WATTS



MAXIMUM RATINGS

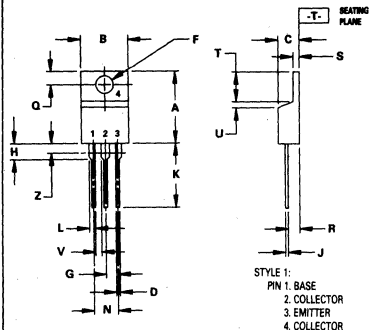
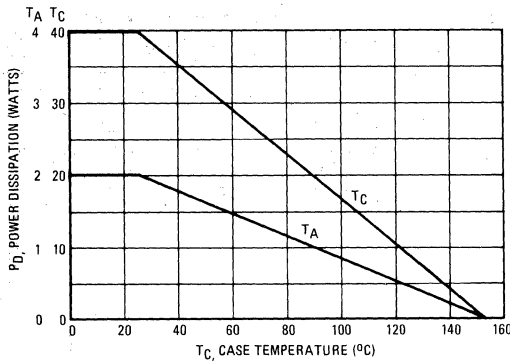
Rating	Symbol	TIP47	TIP48	TIP49	TIP50	Unit
Collector-Emitter Voltage	V_{CE0}	250	300	350	400	Vdc
Collector-Base Voltage	V_{CB}	350	400	450	500	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →				Vdc
Collector Current—Continuous Peak	I_C	← 1.0 →				Adc
		← 2.0 →				
Base Current	I_B	← 0.6 →				Adc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	← 40 →				Watts W/ $^\circ C$
		← 0.32 →				
Total Power Dissipation @ $T_A = 25^\circ C$ Derate above $25^\circ C$	P_D	← 2.0 →				Watts W/ $^\circ C$
		← 0.016 →				
Unclamped Inducting Load Energy (See Figure 8)	E	← 20 →				mJ
Operating and Storage Junction Temperature Range	$T_{J,Tstg}$	← -65 to +150 →				$^\circ C$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	$^\circ C/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$

3

FIGURE 1 — POWER DERATING



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
M	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

TIP47, TIP48, TIP49, TIP50 NPN

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I _C = 30 mAdc, I _B = 0)	TIP47 TIP48 TIP49 TIP50	V _{CEO(sus)}	250 300 350 400	— — — —	Vdc
Collector Cutoff Current (V _{CE} = 150 Vdc, I _B = 0) (V _{CE} = 200 Vdc, I _B = 0) (V _{CE} = 250 Vdc, I _B = 0) (V _{CE} = 300 Vdc, I _B = 0)	TIP47 TIP48 TIP49 TIP50	I _{CEO}	— — — —	1.0 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V _{CE} = 350 Vdc, V _{BE} = 0) (V _{CE} = 400 Vdc, V _{BE} = 0) (V _{CE} = 450 Vdc, V _{BE} = 0) (V _{CE} = 500 Vdc, V _{BE} = 0)	TIP47 TIP48 TIP49 TIP50	I _{CES}	— — — —	1.0 1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)		I _{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I _C = 0.3 Adc, V _{CE} = 10 Vdc) (I _C = 1.0 Adc, V _{CE} = 10 Vdc)		h _{FE}	30 10	150 —	—
Collector-Emitter Saturation Voltage (I _C = 1.0 Adc, I _B = 0.2 Adc)		V _{CE(sat)}	—	1.0	Vdc
Base-Emitter On Voltage (I _C = 1.0 Adc, V _{CE} = 10 Vdc)		V _{BE(on)}	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (I _C = 0.2 Adc, V _{CE} = 10 Vdc, f = 2.0 MHz)		f _T	10	—	MHz
Small-Signal Current Gain (I _C = 0.2 Adc, V _{CE} = 10 Vdc, f = 1.0 kHz)		h _{fe}	25	—	—

(1) Pulse Test: Pulsethickness ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

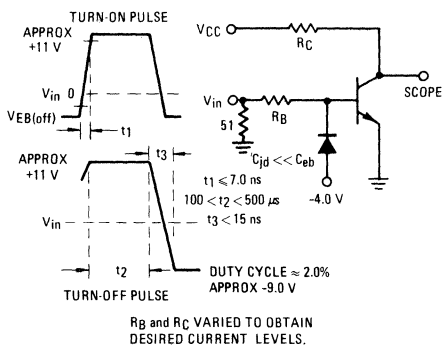


FIGURE 3 – TURN-ON TIME

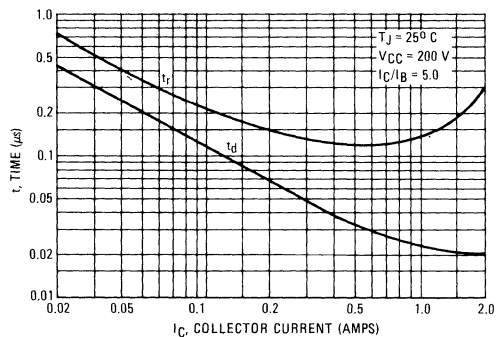


FIGURE 4 – THERMAL RESPONSE

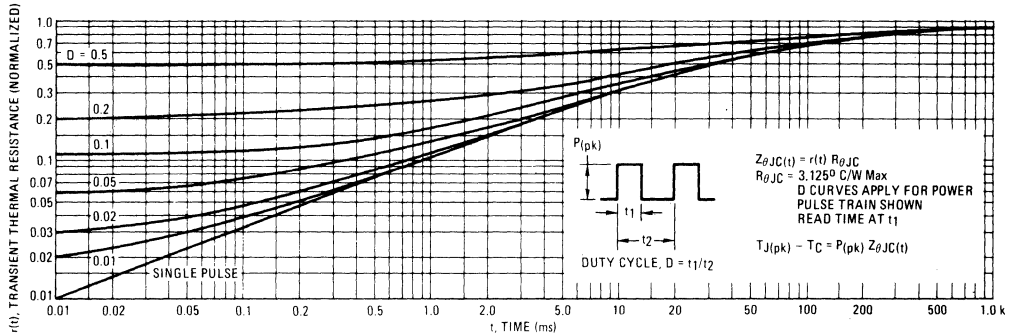
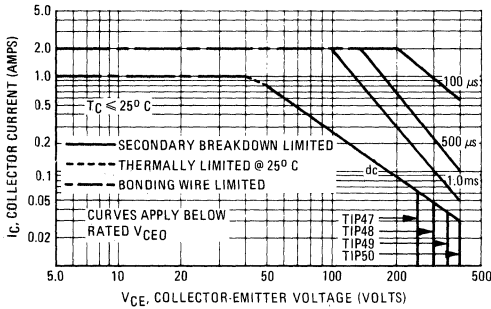


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

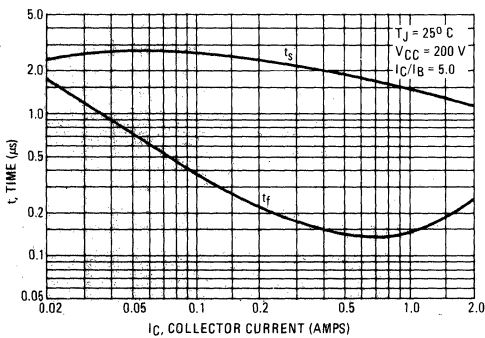
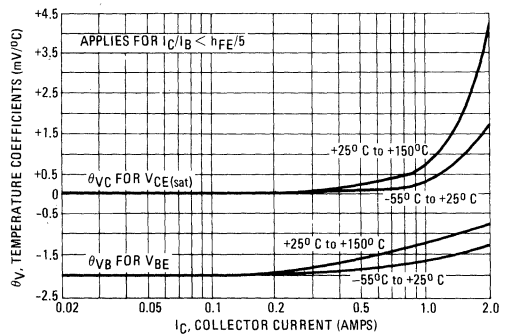
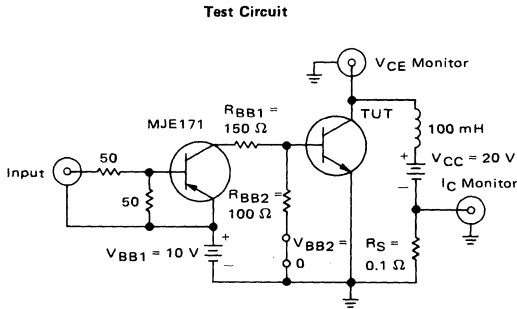


FIGURE 7 – TEMPERATURE COEFFICIENTS



TIP47, TIP48, TIP49, TIP50 NPN

FIGURE 8 – INDUCTIVE LOAD SWITCHING



Note A: Input pulse width is increased until $I_{CM} = 0.63$ A.

Voltage and Current Waveforms

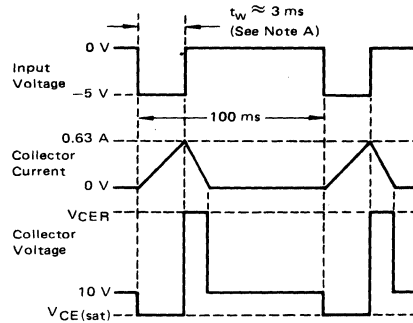


FIGURE 9 – DC CURRENT GAIN

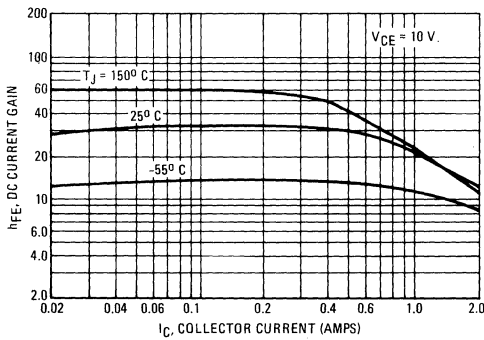
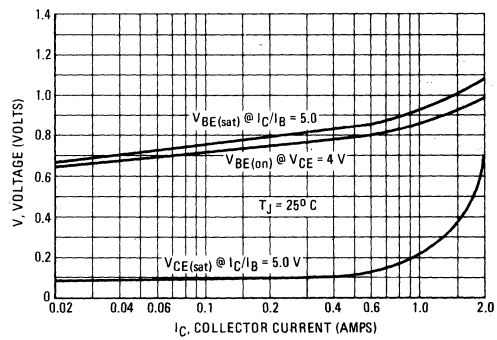


FIGURE 10 – "ON" VOLTAGES



MOTOROLA SEMICONDUCTOR TECHNICAL DATA

NPN
TIP100
TIP101
TIP102

PNP
TIP105
TIP106
TIP107

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
 $h_{FE} = 2500$ (Typ) @ $I_C = 4.0$ Adc
- Collector-Emitter Sustaining Voltage – @ 30 mAdc
 $V_{CE(sus)} = 60$ Vdc (Min) – TIP100, TIP105
 $= 80$ Vdc (Min) – TIP101, TIP106
 $= 100$ Vdc (Min) – TIP102, TIP107
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 2.0$ Vdc (Max) @ $I_C = 3.0$ Adc
 $= 2.5$ Vdc (Max) @ $I_C = 8.0$ Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

*MAXIMUM RATINGS

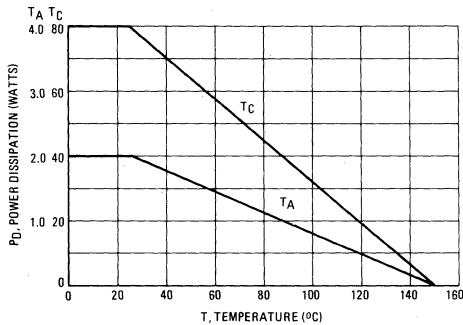
Rating	Symbol	TIP100, TIP105	TIP101, TIP106	TIP102, TIP107	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous	I_C	← 8.0 →			Adc
Peak		← 15 →			
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	← 80 →			Watts
		← 0.64 →			Watts/ $^\circ\text{C}$
Unclamped Inductive Load Energy (1)	E	← 30 →			mJ
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	← 2.0 →			Watts
		← 0.016 →			Watts/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

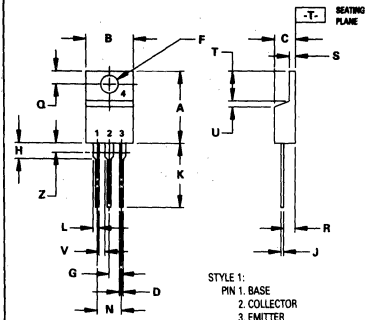
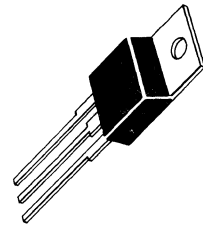
(1) $I_C = 1.1$ A, $L = 50$ mH, P.R.F. = 10 Hz, $V_{CC} = 20$ V, $R_{BE} = 100 \Omega$.

FIGURE 1 – POWER DERATING



DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80-100 VOLTS
80 WATTS



STYLE 1:
PM 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.86	10.28	0.390	0.406
C	4.07	4.93	0.160	0.194
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
O	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

TIP100, TIP101, TIP102 NPN/TIP105, TIP106, TIP107 PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) ($I_C = 30 \text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	60 80 100	— — —	Vdc	
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40 \text{ Vdc}$, $I_B = 0$) ($V_{CE} = 50 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	— — —	50 50 50	μA	
	Collector Cutoff Current ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 80 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	— — —	50 50 50	μA
		Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	8.0
ON-CHARACTERISTICS (1)					
DC Current Gain ($I_C = 3.0 \text{ A}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 8.0 \text{ A}$, $V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	1000 200	20,000 —	—	
Collector-Emitter Saturation Voltage ($I_C = 3.0 \text{ A}$, $I_B = 6.0 \text{ mA}$) ($I_C = 8.0 \text{ A}$, $I_B = 80 \text{ mA}$)	$V_{CE(sat)}$	— —	2.0 2.5	Vdc	
Base-Emitter On Voltage ($I_C = 8.0 \text{ A}$, $V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	—	2.8	Vdc	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain ($I_C = 3.0 \text{ A}$, $V_{CE} = 4.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	$ h_{fe} $	4.0	—	—	
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	— —	300 200	μF	

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

3

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

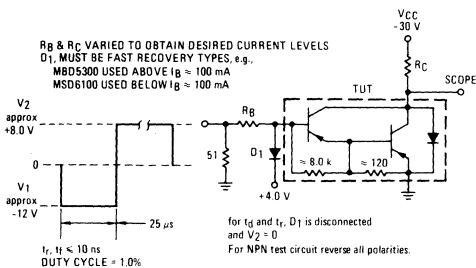


FIGURE 3 – SWITCHING TIMES

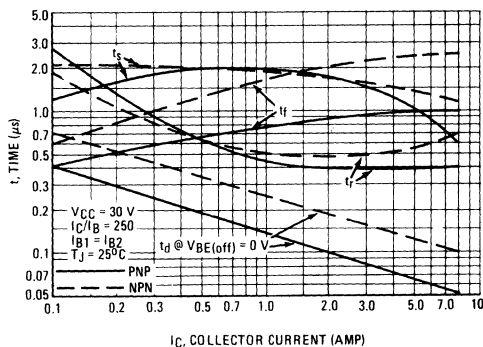


FIGURE 4 – THERMAL RESPONSE

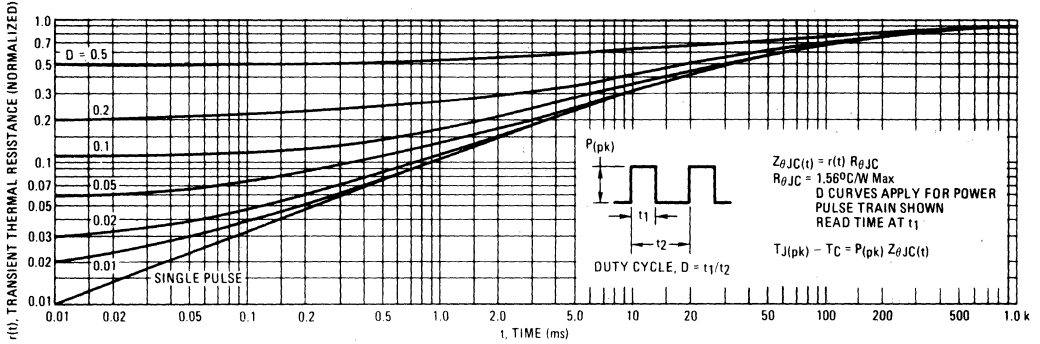
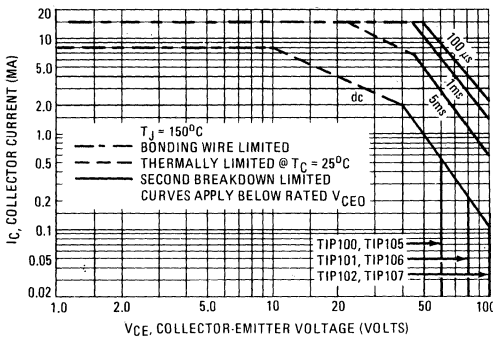


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 7 – CAPACITANCE

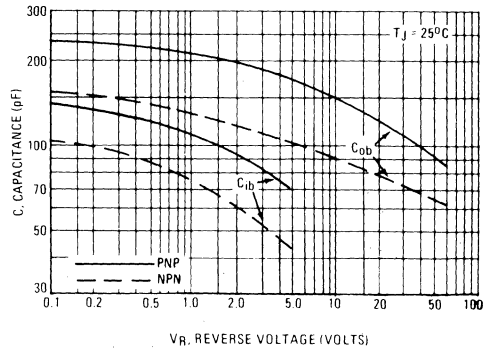
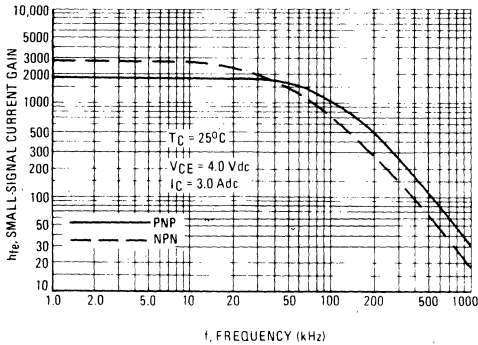
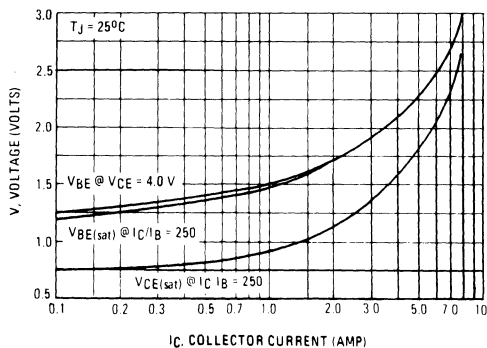
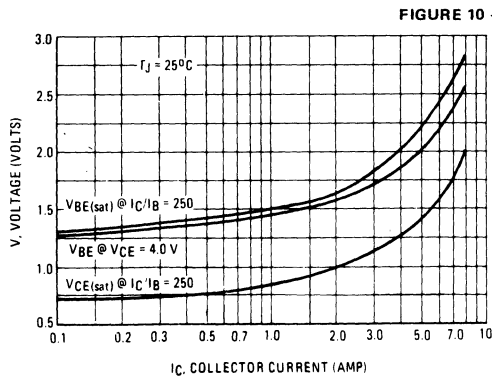
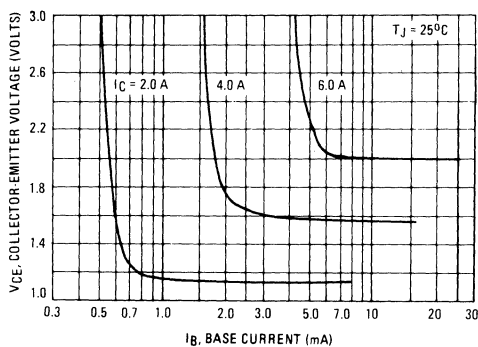
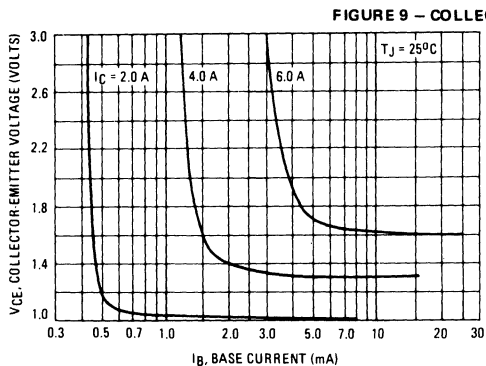
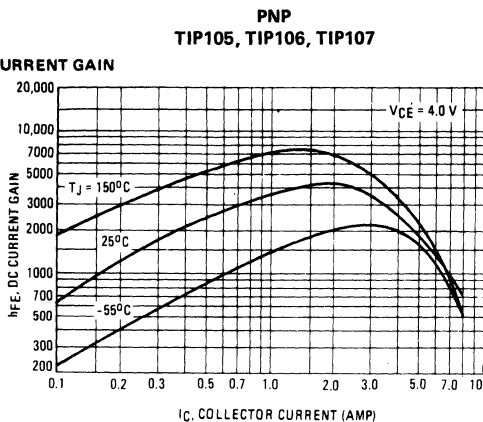
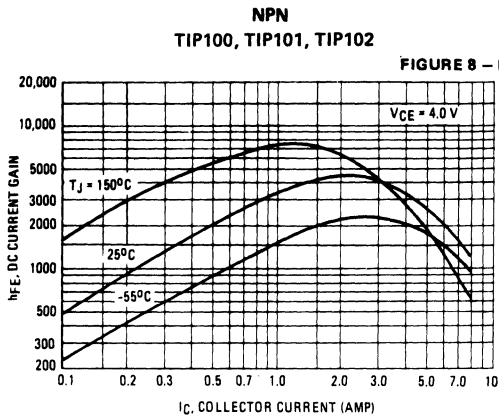


FIGURE 6 – SMALL-SIGNAL CURRENT GAIN



TIP100, TIP101, TIP102 NPN/TIP105, TIP106, TIP107 PNP



NPN
TIP110
TIP111
TIP112

PNP
TIP115
TIP116
TIP117

**PLASTIC MEDIUM-POWER
 COMPLEMENTARY SILICON TRANSISTORS**

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
 $h_{FE} = 2500$ (Typ) @ $I_C = 1.0$ Adc
- Collector-Emitter Sustaining Voltage – @ 30 mA dc
 $V_{CE(sus)} = 60$ Vdc (Min) – TIP110, TIP115
 $= 80$ Vdc (Min) – TIP111, TIP116
 $= 100$ Vdc (Min) – TIP112, TIP117
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 2.5$ Vdc (Max) @ $I_C = 2.0$ Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

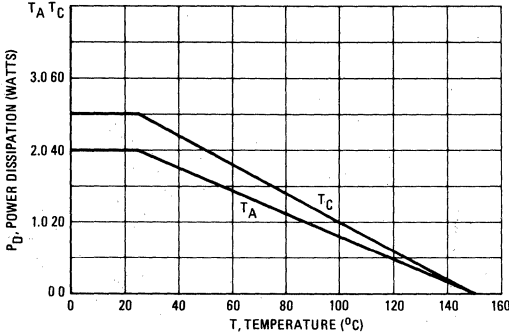
***MAXIMUM RATINGS**

Rating	Symbol	TIP110, TIP115	TIP111, TIP116	TIP112, TIP117	Unit
Collector-Emitter Voltage	V_{CE0}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous	I_C	← 2.0 →			A dc
Collector Current – Peak		← 4.0 →			A dc
Base Current	I_B	← 50 →			mA dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	← 50 →			Watts
Derate above 25°C		← 0.4 →			W/°C
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	← 2.0 →			Watts
Derate above 25°C		← 0.016 →			W/°C
Unclamped Inductive Load Energy – Figure 13	E	← 25 →			mJ
Operating and Storage Junction,	T_J, T_{stg}	← -65 to +150 →			°C

THERMAL CHARACTERISTICS

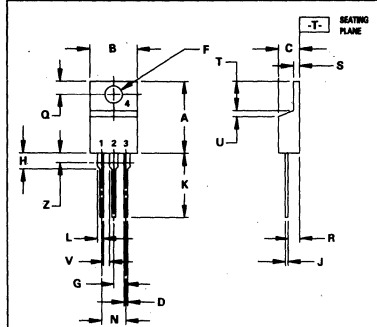
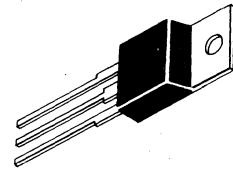
Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 – POWER DERATING



**DARLINGTON
 2 AMPERE
 COMPLEMENTARY SILICON
 POWER TRANSISTORS**

**60-80-100 VOLTS
 50 WATTS**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
- STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.406
C	4.07	4.82	0.160	0.190
D	0.84	0.88	0.0325	0.0325
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
M	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

**CASE 221A-04
 TO-220AB**

TIP110, TIP111, TIP112, NPN, TIP115, TIP116, TIP117, PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I _C = 30 mA, I _B = 0)	V _{CEO(sus)}	60 80 100	— — —	Vdc
Collector Cutoff Current (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 40 Vdc, I _B = 0) (V _{CE} = 50 Vdc, I _B = 0)	I _{CEO}	— — —	2.0 2.0 2.0	mA
Collector Cutoff Current (V _{CB} = 60 Vdc, I _E = 0) (V _{CB} = 80 Vdc, I _E = 0) (V _{CB} = 100 Vdc, I _E = 0)	I _{CBO}	— — —	1.0 1.0 1.0	mA
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	—	2.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain (I _C = 1.0 A, V _{CE} = 4.0 Vdc) (I _C = 2.0 A, V _{CE} = 4.0 Vdc)	h _{FE}	1000 500	— —	—
Collector-Emitter Saturation Voltage (I _C = 2.0 A, I _B = 8.0 mA)	V _{CE(sat)}	—	2.5	Vdc
Base-Emitter On Voltage (I _C = 2.0 A, V _{CE} = 4.0 Vdc)	V _{BE(on)}	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I _C = 0.75 A, V _{CE} = 10 Vdc, f = 1.0 MHz)	h _{fe}	25	—	—
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	— —	200 100	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

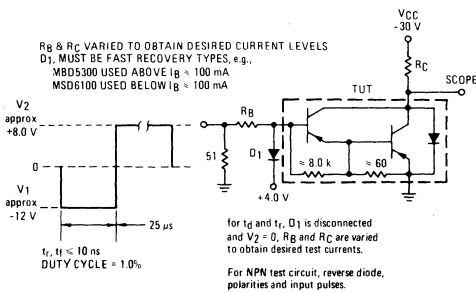


FIGURE 3 – SWITCHING TIMES

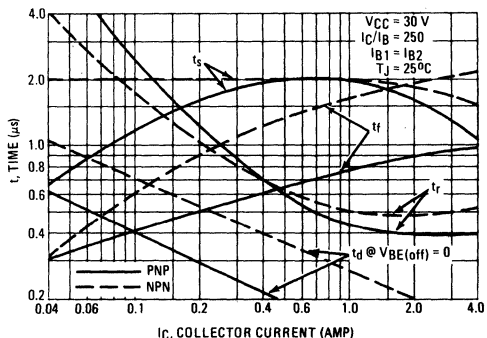
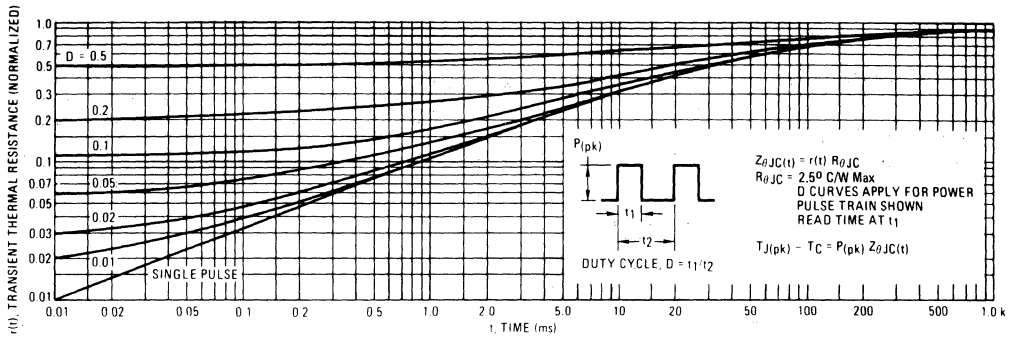


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 5 – TIP115, 116, 117

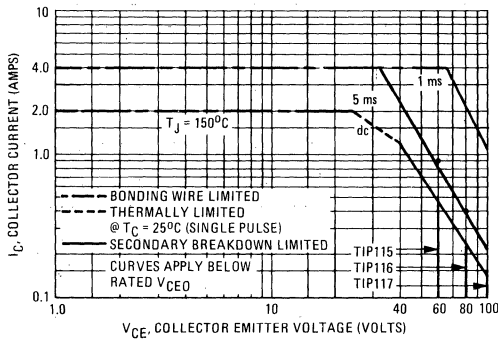


FIGURE 6 – TIP110, 111, 112

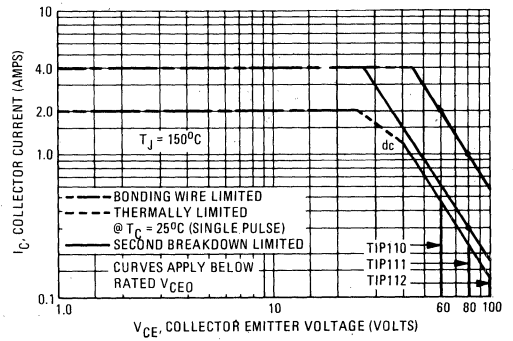
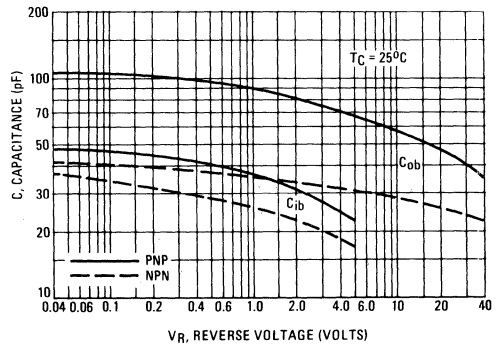


FIGURE 7 – CAPACITANCE



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

**NPN
TIP120
TIP121
TIP122**

**PNP
TIP125
TIP126
TIP127**

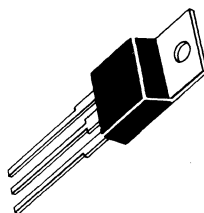
PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

... designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
 $h_{FE} = 2500$ (Typ) @ $I_C = 4.0$ Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc
 $V_{CE(sus)} = 60$ Vdc (Min) – TIP120, TIP125
 $= 80$ Vdc (Min) – TIP121, TIP126
 $= 100$ Vdc (Min) – TIP122, TIP127
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 2.0$ Vdc (Max) @ $I_C = 3.0$ Adc
 $= 4.0$ Vdc (Max) @ $I_C = 5.0$ Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON 5 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

**60-80-100 VOLTS
65 WATTS**



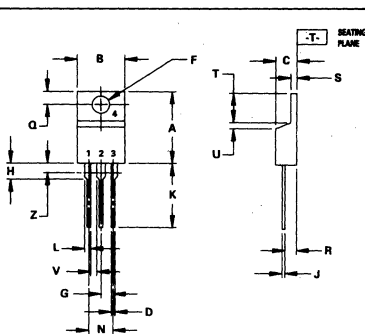
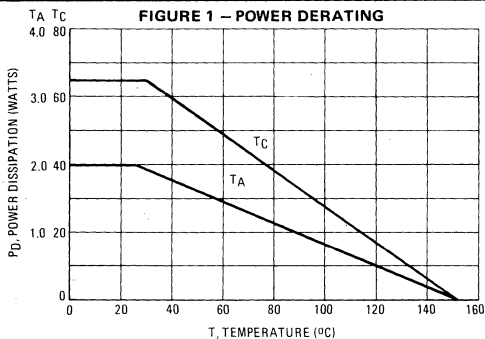
*MAXIMUM RATINGS

Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous	I_C	← 5.0 →			Adc
Peak		← 8.0 →			
Base Current	I_B	← 120 →			mAdc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	← 65 →			Watts
Derate above 25°C		← 0.52 →			
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	← 2.0 →			Watts
Derate above 25°C		← 0.016 →			
Unclamped Inductive Load Energy (1)	E	← 50 →			mJ
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	← -65 to +150 →			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

(1) $I_C = 1$ A, $L = 100$ mH, P.R.F. = 10 Hz, $V_{CC} = 20$ V, $R_{BE} = 100 \Omega$.



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.56	10.29	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.50	0.110	0.135
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
O	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

**CASE 221A-04
TO-220AB**

TIP120, TIP121, TIP122, NPN, TIP125, TIP126, TIP127, PNP

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I _C = 100 mAdc, I _B = 0)	TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	V _{CEO(sus)}	60 80 100	— — —	Vdc
Collector Cutoff Current (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 40 Vdc, I _B = 0) (V _{CE} = 50 Vdc, I _B = 0)	TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	I _{CEO}	— — —	0.5 0.5 0.5	mAdc
Collector Cutoff Current (V _{CB} = 60 Vdc, I _E = 0) (V _{CB} = 80 Vdc, I _E = 0) (V _{CB} = 100 Vdc, I _E = 0)	TIP120, TIP125 TIP121, TIP126 TIP122, TIP127	I _{CBO}	— — —	0.2 0.2 0.2	mAdc
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)		I _{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I _C = 0.5 Adc, V _{CE} = 3.0 Vdc) (I _C = 3.0 Adc, V _{CE} = 3.0 Vdc)		h _{FE}	1000 1000	— —	—
Collector-Emitter Saturation Voltage (I _C = 3.0 Adc, I _B = 12 mAdc) (I _C = 5.0 Adc, I _B = 20 mAdc)		V _{CE(sat)}	— —	2.0 4.0	Vdc
Base-Emitter On Voltage (I _C = 3.0 Adc, V _{CE} = 3.0 Vdc)		V _{BE(on)}	—	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I _C = 3.0 Adc, V _{CE} = 4.0 Vdc, f = 1.0 MHz)		h _{fe}	4.0	—	—
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	TIP125, TIP126, TIP127 TIP120, TIP121, TIP122	C _{ob}	— —	300 200	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

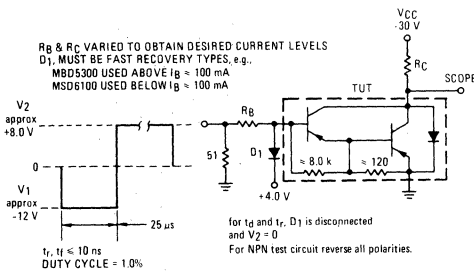
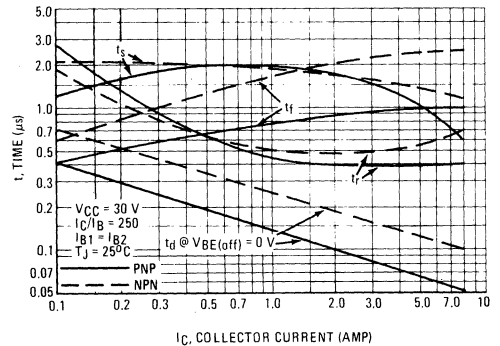


FIGURE 3 – SWITCHING TIMES



TIP120, TIP121, TIP122, NPN, TIP125, TIP126, TIP127, PNP

FIGURE 4 – THERMAL RESPONSE

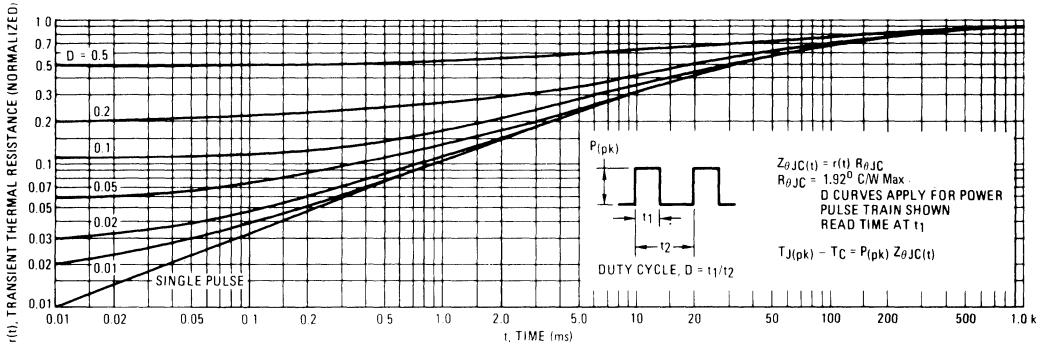
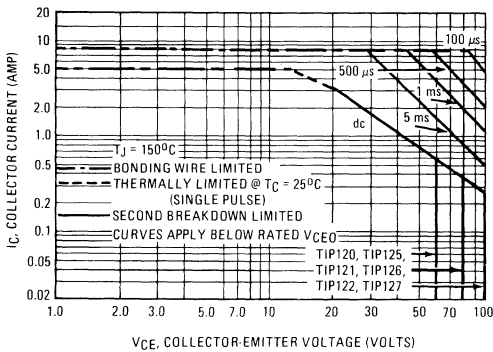


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

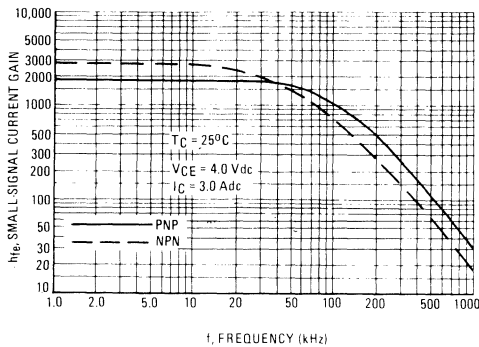
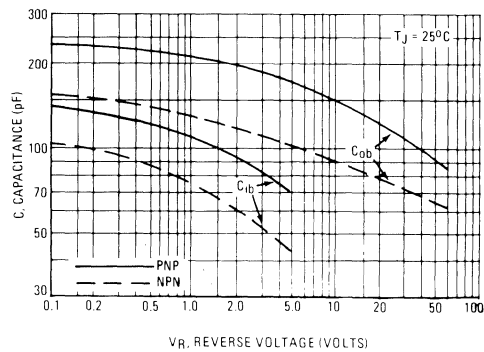
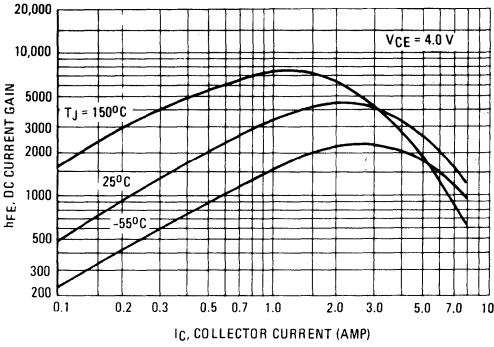


FIGURE 7 – CAPACITANCE



TIP120, TIP121, TIP122, NPN, TIP125, TIP126, TIP127, PNP

NPN
TIP120, TIP121, TIP122



PNP
TIP125, TIP126, TIP127

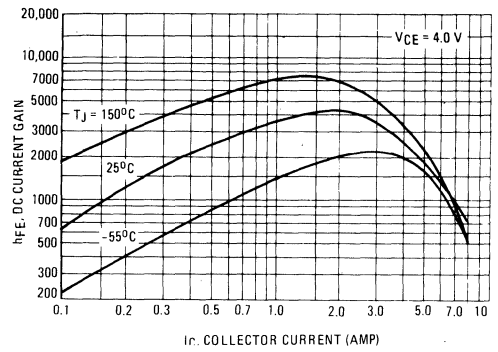


FIGURE 9 – COLLECTOR SATURATION REGION

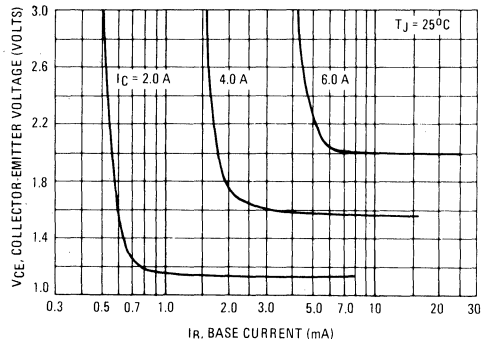
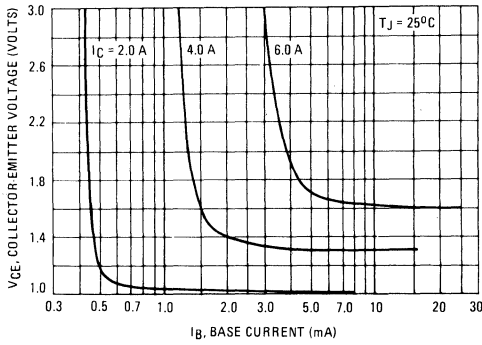
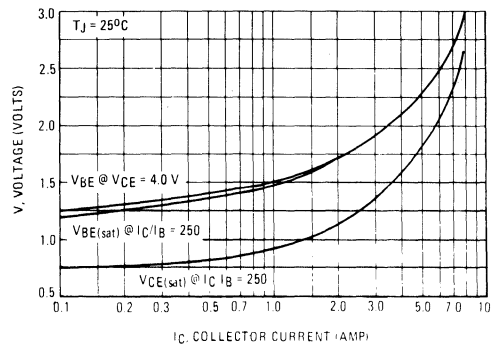
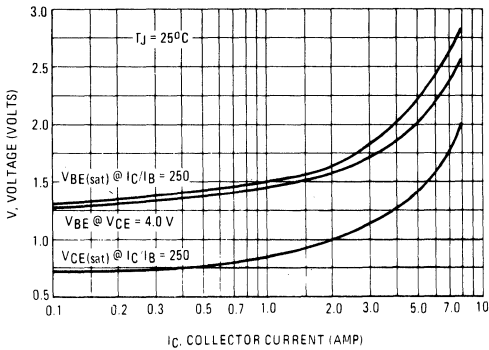


FIGURE 10 – "ON" VOLTAGES



3

NPN
TIP140
TIP141
TIP142

PNP
TIP145
TIP146
TIP147

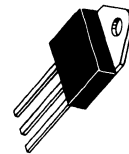
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain — Min $h_{FE} = 1000$ @ $I_C = 5$ A, $V_{CE} = 4$ V
- Collector-Emitter Sustaining Voltage — @ 30 mA
 $V_{CE(sus)} = 60$ Vdc (Min) — TIP140, TIP145
 80 Vdc (Min) — TIP141, TIP146
 100 Vdc (Min) — TIP142, TIP147
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor

10 AMPERE DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

60-100 VOLTS
125 WATTS



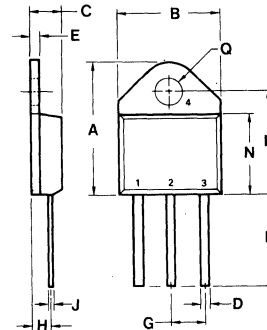
MAXIMUM RATINGS

Rating	Symbol	TIP140 TIP145	TIP141 TIP146	TIP142 TIP147	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak (1)	I_C	10 15			Adc
Base Current — Continuous	I_B	0.5			Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	125			Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C}/\text{W}$
Thermal Resistance, Case to Ambient	$R_{\theta JA}$	35.7	$^\circ\text{C}/\text{W}$

(1) 5 ms, $\leq 10\%$ Duty Cycle

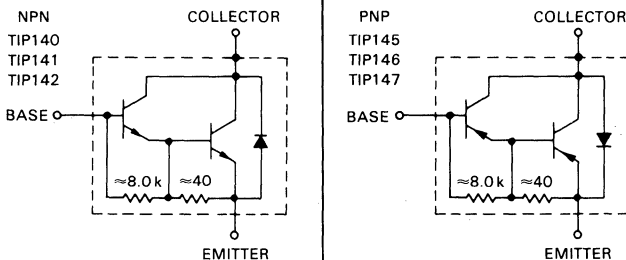


- STYLE 1:
 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	3.94	4.19	0.155	0.165

CASE 340-01
TO-218AC

DARLINGTON SCHEMATICS



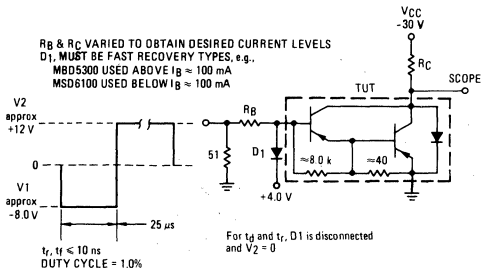
TIP140, TIP141, TIP142 NPN, TIP145, TIP146, TIP147 PNP

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1) ($I_C = 30\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	60 80 100	— — —	— — —	Vdc	
Collector Cutoff Current ($V_{CE} = 30\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 50\text{ Vdc}$, $I_B = 0$)	I_{CEO}	— — —	— — —	2.0 2.0 2.0	mA	
Collector Cutoff Current ($V_{CB} = 60\text{ V}$, $I_E = 0$) ($V_{CB} = 80\text{ V}$, $I_E = 0$) ($V_{CB} = 100\text{ V}$, $I_E = 0$)	I_{CBO}	— — —	— — —	1.0 1.0 1.0	mA	
Emitter Cutoff Current $V_{BE} = 5.0\text{ V}$	I_{EBO}	—	—	2.0	mA	
ON CHARACTERISTICS (1)						
DC Current Gain ($I_C = 5.0\text{ A}$, $V_{CE} = 4.0\text{ V}$) ($I_C = 10\text{ A}$, $V_{CE} = 4.0\text{ V}$)	h_{FE}	1000 500	— —	— —	—	
Collector-Emitter Saturation Voltage ($I_C = 5.0\text{ A}$, $I_B = 10\text{ mA}$) ($I_C = 10\text{ A}$, $I_B = 40\text{ mA}$)	$V_{CE(sat)}$	— —	— —	2.0 3.0	Vdc	
Base-Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 40\text{ mA}$)	$V_{BE(sat)}$	—	—	3.5	Vdc	
Base-Emitter On Voltage ($I_C = 10\text{ A}$, $V_{CE} = 4.0\text{ Vdc}$)	$V_{BE(on)}$	—	—	3.0	Vdc	
SWITCHING CHARACTERISTICS						
Resistive Load (See Figure 1)						
Delay Time	($V_{CC} = 30\text{ V}$, $I_C = 5.0\text{ A}$, $I_B = 20\text{ mA}$, Duty Cycle $\leq 2.0\%$, $I_{B1} = I_{B2}$, R_C & R_B Varied, $T_J = 25^\circ\text{C}$)	t_d	—	0.15	—	μs
Rise Time		t_r	—	0.55	—	μs
Storage Time		t_s	—	2.5	—	μs
Fall Time		t_f	—	2.5	—	μs

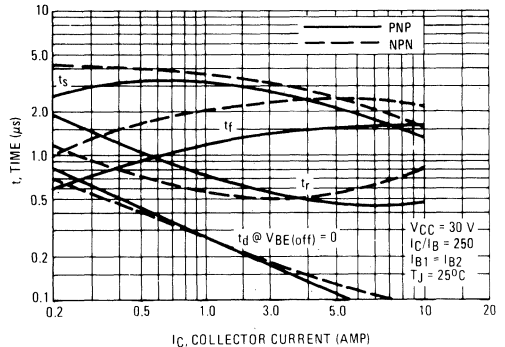
(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

FIGURE 2 — SWITCHING TIMES



TIP140, TIP141, TIP142 NPN, TIP145, TIP146, TIP147 PNP

TYPICAL CHARACTERISTICS

NPN
TIP140, TIP141, TIP142

PNP
TIP145, TIP146, TIP147

FIGURE 3 — DC CURRENT GAIN versus COLLECTOR CURRENT

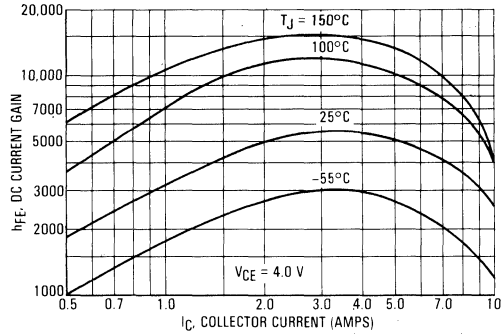
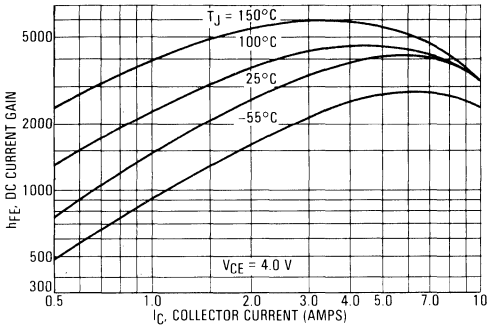


FIGURE 4 — COLLECTOR-EMITTER SATURATION VOLTAGE

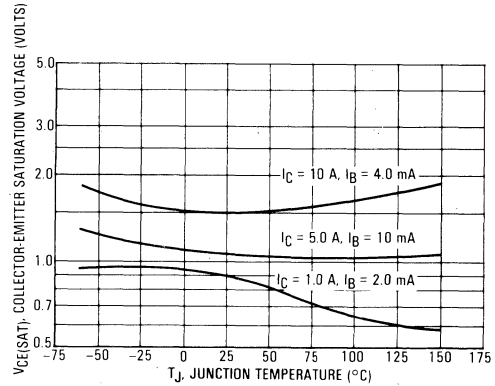
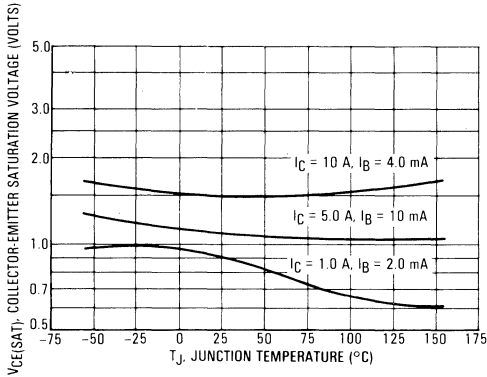
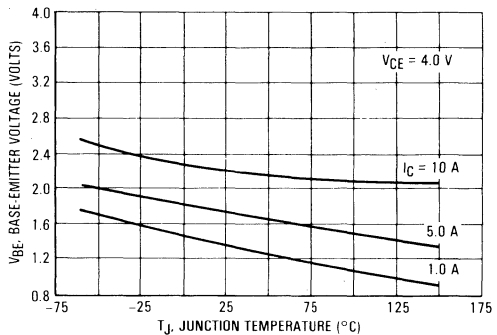
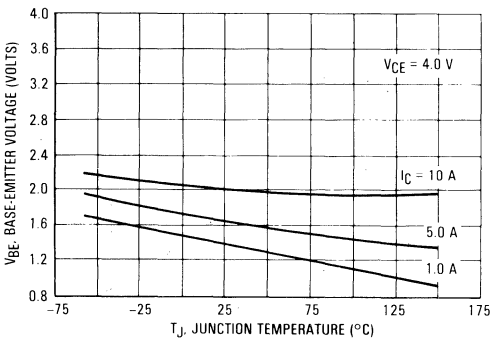


FIGURE 5 — BASE-EMITTER VOLTAGE



TIP140, TIP141, TIP142 NPN, TIP145, TIP146, TIP147 PNP

ACTIVE-REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the

curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 — ACTIVE-REGION SAFE OPERATING AREA

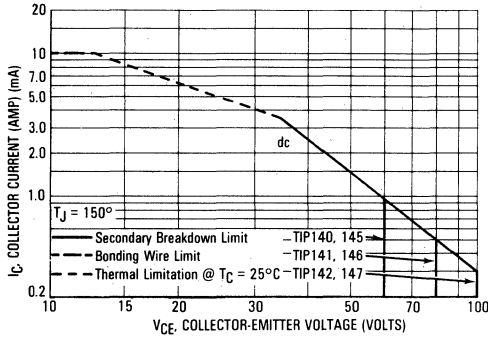


FIGURE 7 — UNCLAMPED INDUCTIVE LOAD

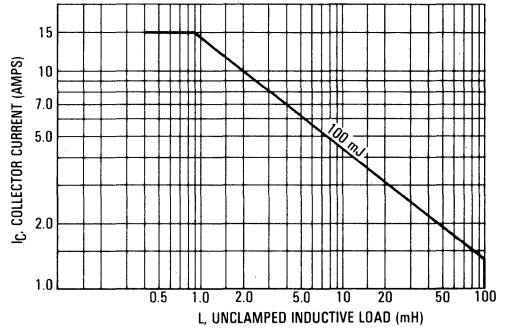
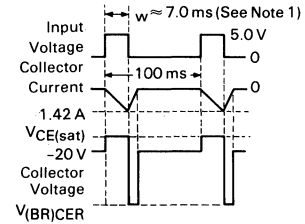
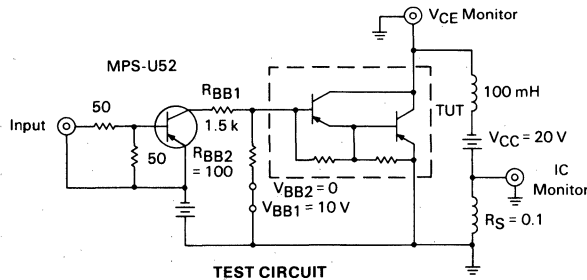


FIGURE 8 — INDUCTIVE LOAD



NOTE 1: Input pulse width is increased until $I_{CM} = 1.42 \text{ A}$.
NOTE 2: For NPN test circuit reverse polarities.

VOLTAGE AND CURRENT WAVEFORMS

FIGURE 9 — MAGNITUDE OF COMMON EMITTER SMALL-SIGNAL SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO

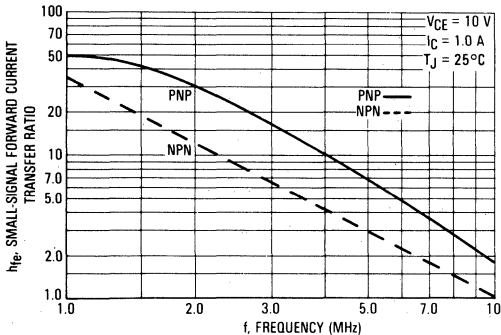
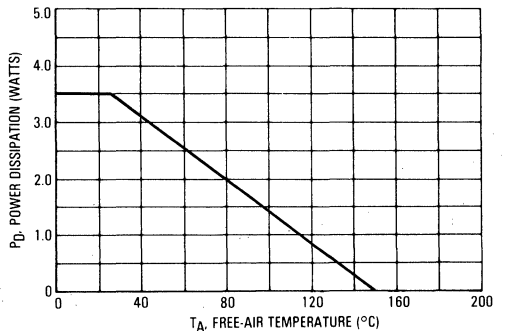


FIGURE 10 — FREE-AIR TEMPERATURE POWER DERATING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
TIP3055
PNP
TIP2955

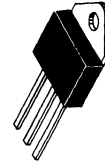
COMPLEMENTARY SILICON POWER TRANSISTORS

... designed for general-purpose switching and amplifier applications.

- DC Current Gain — $h_{FE} = 20-70 @ I_C = 4.0 \text{ Adc}$
- Collector-Emitter Saturation Voltage — $V_{CE(sat)} = 1.1 \text{ Vdc (Max)}$ @ $I_C = 4.0 \text{ Adc}$
- Excellent Safe Operating Area

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON

60 VOLTS
90 WATTS



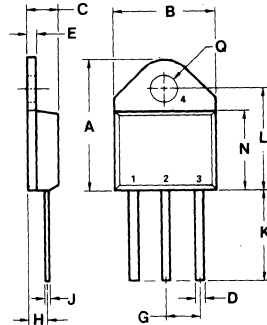
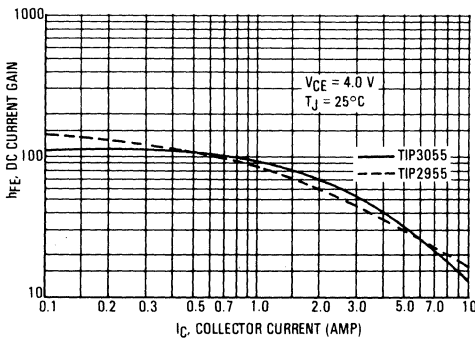
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Emitter Voltage	V_{CER}	70	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current	I_B	7.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	90 0.72	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.39	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	35.7	$^\circ\text{C}/\text{W}$

FIGURE 1 — DC CURRENT GAIN



STYLE 1:

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	6.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
(TO-218AC)

TIP3055NPN, TIP2955PNP

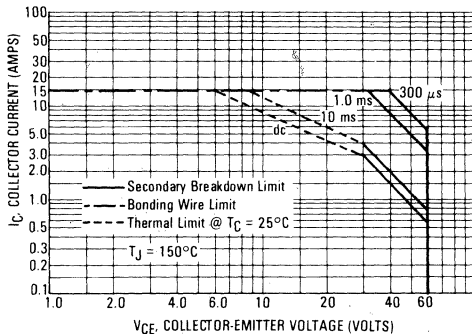
ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) ($I_C = 30 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	60	—	Vdc
Collector Cutoff Current ($V_{CE} = 70 \text{ Vdc}$, $R_{BE} = 100 \text{ Ohms}$)	I_{CER}	—	1.0	mAdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current ($V_{CE} = 100 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$)	I_{CEV}	—	5.0	mAdc
Emitter Cutoff Current ($V_{BE} = 7.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 10 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	h_{FE}	20 5.0	70 —	—
Collector-Emitter Saturation Voltage ($I_C = 4.0 \text{ Adc}$, $I_B = 400 \text{ mAdc}$) ($I_C = 10 \text{ Adc}$, $I_B = 3.3 \text{ Adc}$)	$V_{CE(sat)}$	— —	1.1 3.0	Vdc
Base-Emitter On Voltage ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	—	1.8	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 30 \text{ Vdc}$, $t = 1.0 \text{ s}$; Nonrepetitive)	$I_{s/b}$	3.0	—	Adc
DYNAMIC CHARACTERISTICS				
Current Gain—Bandwidth Product ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	f_T	2.5	—	MHz
Small-Signal Current Gain ($V_{CE} = 4.0 \text{ Vdc}$, $I_C = 1.0 \text{ Adc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	15	—	kHz

(1) Pulse Test: Pulse Width = $300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Note: For additional design curves, refer to electrical characteristics curves of 2N3055.

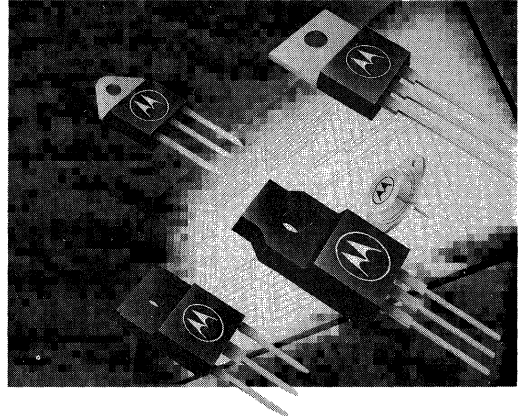
FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature.





1

**Alphanumeric Index
and Cross Reference**

2

Selector Guide

3

Data Sheets



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