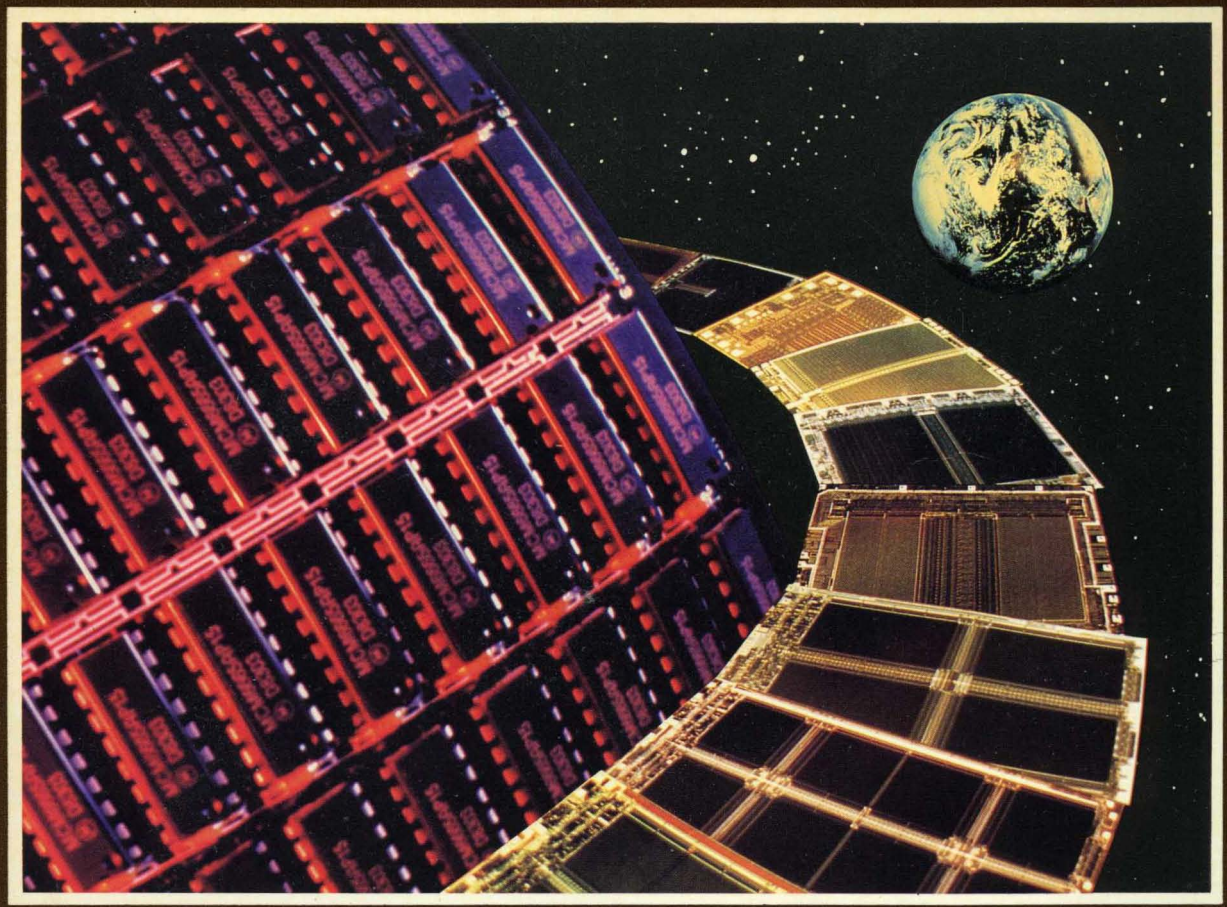
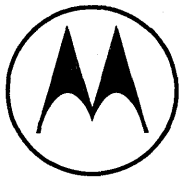
DL113
Rev 3

MOTOROLA



MEMORY DATA



MOTOROLA

MEMORIES

Prepared by
Technical Information Center

Motorola has developed a very broad range of reliable memories for virtually any digital data processing system application. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, a selector guide is included to simplify the task of choosing the best combination of circuits for optimum system architecture.

The information in this book has been carefully checked; no responsibility, however, is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent rights of the manufacturer.

New Motorola memories are being introduced continually. For the latest releases, and additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

Series D

Printed in U.S.A.
May 1984

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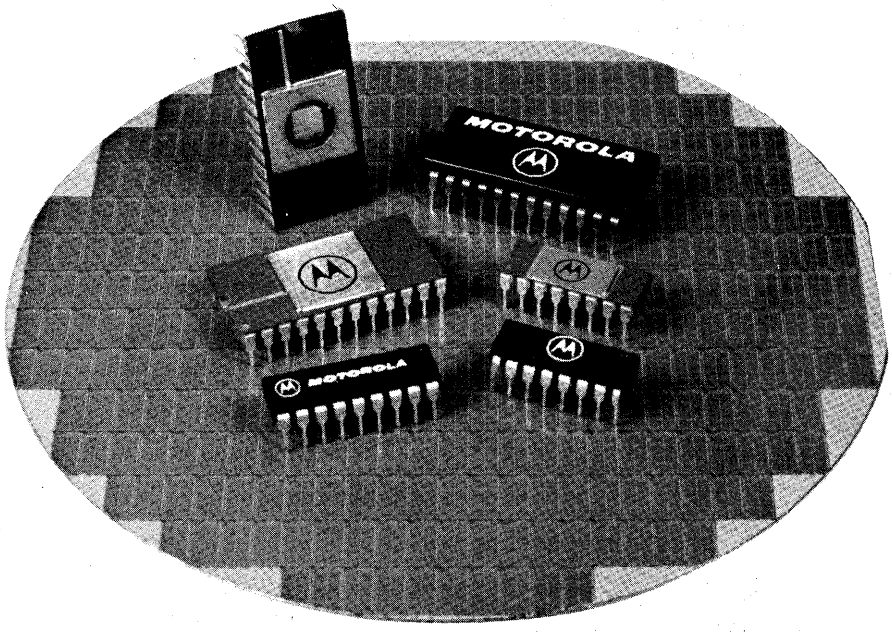
Selector Guide



MOTOROLA MEMORIES

Motorola has developed a very broad range of reliable MOS and bipolar memories for virtually any digital data processing system application.

New Motorola memories are being introduced continually. **This selector guide lists all those available as of May 1984.** For later releases, additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

Data sheets may be obtained from your in-plant VSMF Data Center, distributors, Motorola sales office or by writing to:

Literature Distribution Center
Motorola Semiconductor Products Inc.
P.O. Box 20912
Phoenix, AZ 85036

Notes:

Operating temperature ranges:
MOS – 0°C to 70°C
ECL – 0°C to 75°C
TTL – Military –55°C to +125°C, Commercial 0°C to 75°C

*To be introduced.
(Not all speed selections shown)

[1]300 mil package

[2]Character generators include shifted and unshifted characters, ASCII alphanumeric control, math, Japanese, British, German, European and French symbols.

[3]Standard Patterns for MOS ROMs:
MCM68A316EP91 – Universal Code Coverter and Character Generator
MCM68A332P2 – Sine/Cosine Look-Up Table
MCM68364P35-3 – Log/Antilog Look-Up Table
MCM65516P43M – MC146805 Monitor Program

[4]+5 volt for all read operations, except for programming, where +25 volts are required.

[5]Registered Outputs – 20 ns max clock to output
35 ns max address to clock setup time

[6]600 mil package

[7]Asynchronous register

[8]Synchronous register

[9]Typical access

RAMs

MOS DYNAMIC RAMs

Organization	Part Number	Access Time (ns Max)	Power Supplies	No. of Pins
16384 × 1	MCM4116BP15	150	+12, ±5 V	16
16384 × 1	MCM4116BP20	200	+12, ±5 V	16
16384 × 1	MCM4116BP25	250	+12, ±5 V	16
16384 × 1	MCM4517P10	100	+5 V	16
16384 × 1	MCM4517P12	120	+5 V	16
16384 × 1	MCM4517P15	150	+5 V	16
65536 × 1	MCM6665AP15	150	+5 V	16
65536 × 1	MCM6665AP20	200	+5 V	16
65536 × 1	MCM6665BP15	150	+5 V	16
65536 × 1	MCM6665BP20	200	+5 V	16
262,144 × 1	MCM6256P10*	100	+5 V	16
262,144 × 1	MCM6256P12*	120	+5 V	16
262,144 × 1	MCM6256P15*	150	+5 V	16
262,144 × 1	MCM6257P10*	100	+5 V	16
262,144 × 1	MCM6257P12*	120	+5 V	16
262,144 × 1	MCM6257P15*	150	+5 V	16

MOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
128 × 8	MCM6810	450	24
128 × 8	MCM68A10	360	24
128 × 8	MCM68B10	250	24
1024 × 4	MCM2114P20	200	18
1024 × 4	MCM2114P25	250	18
1024 × 4	MCM2114P30	300	18
1024 × 4	MCM2114P45	450	18
2048 × 8	MCM2016HP45	45	24
2048 × 8	MCM2016HN45	45	24[1]
2048 × 8	MCM2016HY45	45	24[1]
2048 × 8	MCM2016HP55	55	24
2048 × 8	MCM2016HN55	55	24[1]
2048 × 8	MCM2016HY55	55	24[1]
2048 × 8	MCM2016HP70	70	24
2048 × 8	MCM2016HN70	70	24[1]
2048 × 8	MCM2016HY70	70	24[1]
16384 × 1	MCM2167HP35	35	20
16384 × 1	MCM2167HL35	35	20
16384 × 1	MCM2167HZ35	35	20
16384 × 1	MCM2167HP45	45	20
16384 × 1	MCM2167HL45	45	20
16384 × 1	MCM2167HZ45	45	20
16384 × 1	MCM2167HP70	70	20
16384 × 1	MCM2167HL70	70	20
16384 × 1	MCM2167HZ70	70	20

RAMs (Continued)

CMOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
4096 × 1	MCM6147P55	55	18
4096 × 1	MCM6147P70	70	18
4096 × 1	MCM61L47P55	55	18
4096 × 1	MCM61L47P70	70	20
4096 × 4	MCM6168HP35*	35	20
4096 × 4	MCM6168HP45*	45	20
4096 × 4	MCM6168HP55*	55	20
4096 × 4	MCM6169HP35*	35	22
4096 × 4	MCM6169HP45*	45	22
4096 × 4	MCM6169HP55*	55	22
2048 × 8	MCM6116P12	120	24
2048 × 8	MCM6116P15	150	24
2048 × 8	MCM6116P20	200	24
2048 × 8	MCM61L16P12	120	24
2048 × 8	MCM61L16P15	150	24
2048 × 8	MCM61L16P20	200	24

ECL 10K, 10KH RAMs (Open Emitter)

Organization	Part Number	Access Time (ns max)	Pins
8 × 2	MCM10143	15.5	24
16 × 4	MC10H145	6	16
16 × 4	MCM10145	15	16
64 × 1	MCM10148	15	16
128 × 1	MCM10147	15	16
256 × 1	MCM10144	26	16
256 × 1	MCM10152	15	16
1024 × 1	MCM10146	29	16
1024 × 1	MCM10415-20	20	16
1024 × 1	MCM10415-15	15	16
1024 × 1	MCM10415-10*	10	16
256 × 4	MCM10422-15*	15	24
256 × 4	MCM10422-10*	10	24
4096 × 1	MCM10470-25*	25	18
4096 × 1	MCM10470-15*	15	18
1024 × 4	MCM10474-25*	25	24
1024 × 4	MCM10474-15*	15	24
16384 × 1	MCM10480-20*	20	20
4096 × 4	MCM10484-20*	20	28

RAMs (Continued)

ECL 100K RAMs (Open Emitter)

Organization	Part Number	Access Time (ns max)	Pins
1024 x 1	MCM100415-10*	10	16
256 x 4	MCM100422-10*	10	24
4096 x 1	MCM100470-15*	15	18
1024 x 4	MCM100474-15*	15	24
16384 x 1	MCM100480-20*	20	20
4096 x 4	MCM100484-20*	20	28

TTL RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
1024 x 1	MCM93415	45	O.C.	16
1024 x 1	MCM93425	45	3-State	16
256 x 4	MCM93L422	60	3-State	22
256 x 4	MCM93L422A	45	3-State	22
256 x 4	MCM93422	45	3-State	22
256 x 4	MCM93422A	35	3-State	22

ROMs

MOS CHARACTER GENERATORS[2] (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
128 x (7 x 5)	MCM6670P	350	18
128 x (7 x 5)	MCM6674P	350	18
128 x (9 x 7)	MCM66700P	350	24
128 x (9 x 7)	MCM66710P	350	24
128 x (9 x 7)	MCM66714P	350	24
128 x (9 x 7)	MCM66720P	350	24
128 x (9 x 7)	MCM66730P	350	24
128 x (9 x 7)	MCM66734P	350	24
128 x (9 x 7)	MCM66740P	350	24
128 x (9 x 7)	MCM66750P	350	24
128 x (9 x 7)	MCM66760P	350	24
128 x (9 x 7)	MCM66770P	350	24
128 = (9 x 7)	MCM66780P	350	24
128 x (9 x 7)	MCM66790P	350	24

ROMs (Continued)

MOS Binary ROMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
2048 × 8	MCM68A316EP	350	24
2048 × 8	MCM68A316EP91[3]	350	24
4096 × 8	MCM68A332P	350	24
4096 × 8	MCM68A332P2[3]	350	24
8192 × 8	MCM68364P20	200	24
8192 × 8	MCM68364P25	250	24
8192 × 8	MCM68364P35	350	24
8192 × 8	MCM68364P35-3[3]	350	24
8192 × 8	MCM68365P25	250	24
8192 × 8	MCM68365P35	350	24
8192 × 8	MCM68366P25	250	24
8192 × 8	MCM68366P35	350	24
8192 × 8	MCM68367P	450	24
8192 × 8	MCM68368P	450	24
8192 × 8	MCM68369P20	200	28
8192 × 8	MCM68369P25	250	28
8192 × 8	MCM68369P30	300	28
8192 × 8	MCM68370P20	200	28
8192 × 8	MCM68370P25	250	28
8192 × 8	MCM68370P30	300	28
8192 × 10	MCM68380P	300[9]	24
16384 × 8	MCM63128P15	150	28
16384 × 8	MCM63128P20	200	28
32768 × 8	MCM63256P15	150	28
32768 × 8	MCM63256P20	200	28

CMOS ROMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
2048 × 8	MCM65516P43	430	18
2048 × 8	MCM65516P43M[3]	430	18
2048 × 8	MCM65516P55	550	18
32768 × 8	MCM65256P35	350	28

EPROMs

MOS EPROMs

Organization	Part Number	Access Time (ns max)	Power Supplies[4]	No. of Pins
8192 × 8	MCM68764C35	350	+5 V, 25 V	24
8192 × 8	MCM68764C	450	+5 V, 25 V	24
8192 × 8	MCM68766C30	300	+5 V, 25 V	24
8192 × 8	MCM68766C35	350	+5 V, 25 V	24
8192 × 8	MCM68766C40	400	+5 V, 25 V	24
8192 × 8	MCM68766C	450	+5 V, 25 V	24

ROM/EEPROMs

MOS

Organization		Part Number	Access Time (ns max)	No. of Pins
ROM	EEPROM			
14K × 8	2K × 8	MCM6836E16	270	28
14K × 8	2K × 8 plus 256 redundant bytes	MCM6836R16	270	28

DUAL-PORT RAM

MOS

Organization	Part Number	Access Time (ns max)	No. of Pins
256 × 8	MCM68HC34*	240	40

PROMs

ECL PROMs

Organization	Part Number	Access Time (ns max)	No. of Pins
32 × 8	MCM10139	20	16
256 × 4	MCM10149	25	16
256 × 4	MCM10149A*	15	16

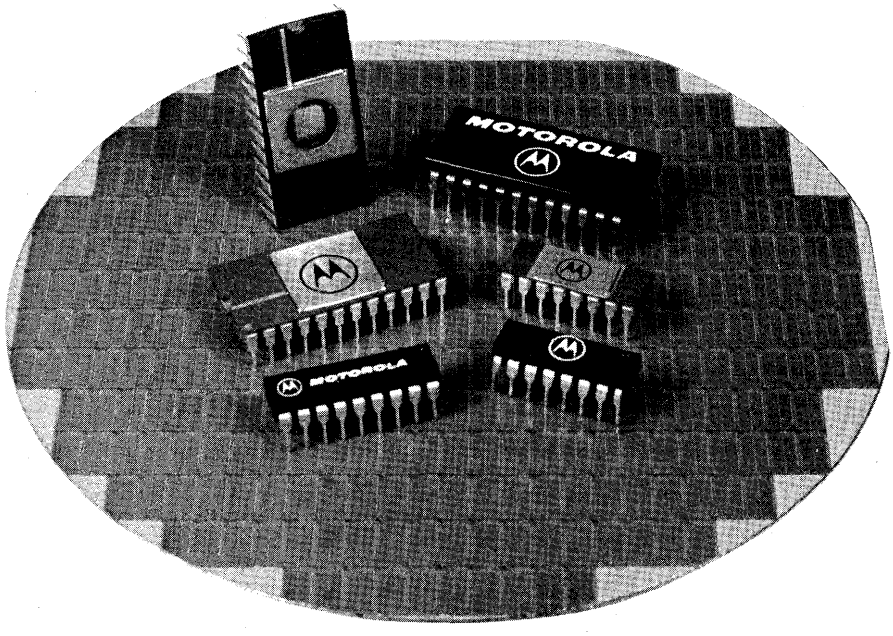
TTL PROMs (3-State Outputs)

Organization	Part Number	Access Time (ns max)	No. of Pins
32 × 8	MCM27S19*	25	16
512 × 4	MCM7621	70	16
512 × 4	MCM7621A	60	16
512 × 8	MCM7641	70	24
512 × 8	MCM7641A	60	24
512 × 8	MCM7649	60	20
512 × 8	MCM7649A	50	20
512 × 8	MCM27S29A*	35	20
512 × 8	MCM27S31A*	35	24
512 × 8	MCM27S25A*	See Note 5	24
512 × 8	MCM27S27A*	See Note 5	22
1024 × 4	MCM7643	70	18
1024 × 4	MCM7643A	50	18
1024 × 8	MCM7681	70	24
1024 × 8	MCM7681A	50	24
1024 × 8	MCM27S181*	35	24[6]
1024 × 8	MCM27S281*	35	24[1]
1024 × 8	MCM27S35A[7]*	See Note 5	24
1024 × 8	MCM27S37A[8]*	See Note 5	24
2048 × 4	MCM7685	70	18
2048 × 4	MCM7685A	55	18
2048 × 8	MCM76161	70	24
2048 × 8	MCM76161A	60	24
2048 × 8	MCM27S191*	35	24[6]
2048 × 8	MCM27S291*	35	24[1]
2048 × 8	MCM27S45A*[7]	See Note 5	24
2048 × 8	MCM27S47A*[8]	See Note 5	24
4096 × 4	MCM76165	50	20
4096 × 4	MCM76165A	35	20

BUBBLE

Organization	Part Number	Access Time (Average)	No. of Pins
262,144 × 1	MBM2256	7.0 ms	16
1,048,576 × 1	MBM2011A	11.5 ms	16

MOS Dynamic RAMs



MOTOROLA

MCM4116B

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4116B is a 16,384-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words and fabricated using Motorola's highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs.

By multiplexing row and column address inputs, the MCM4116B requires only seven address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The data output of the MCM4116B is controlled by the column address strobe and remains valid from access time until the column address strobe returns to the high state. This output scheme allows higher degrees of system design flexibility such as common input/output operation and two dimensional memory selection by decoding both row address and column address strobes.

The MCM4116B incorporates a one-transistor cell design and dynamic storage techniques, with each of the 128 row addresses requiring a refresh cycle every 2 milliseconds.

- Flexible Timing with Read-Modify-Write, RAS-Only Refresh, and Page-Mode Capability
- Industry Standard 16-Pin Package
- 16,384 X 1 Organization
- ±10% Tolerance on All Power Supplies
- All Inputs are Fully TTL Compatible
- Three-State Fully TTL-Compatible Output
- Common I/O Capability When Using "Early Write" Mode
- On-Chip Latches for Addresses and Data In
- Low Power Dissipation — 426 mW Active, 20 mW Standby (Max)
- Fast Access Time Options: 150 ns — MCM4116BP-15, BC-15
  200 ns — MCM4116BP-20, BC-20
  250 ns — MCM4116BP-25, BC-25
  300 ns — MCM4116BP-30, BC-30
- Easy Upgrade from 16-Pin 4K RAMs

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in},V_{out}	-0.5 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

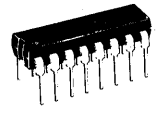
NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

MOS

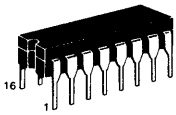
(N-CHANNEL)

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

DRAM

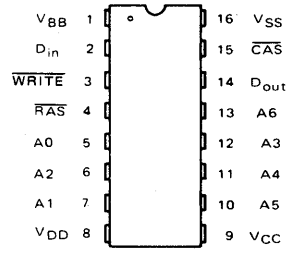


P SUFFIX
PLASTIC PACKAGE
CASE 648



C SUFFIC
FRIT-SEAL PACKAGE
CASE 620

PIN ASSIGNMENT



PIN NAMES

A0–A6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{in}	Data In
D_{out}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{BB}	Power (-5 V)
V_{CC}	Power (+5 V)
V_{DD}	Power (+12 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	Vdc	1
	V_{CC}	4.5	5.0	5.5	Vdc	1, 2
	V_{SS}	0	0	0	Vdc	1
	V_{BB}	-4.5	-5.0	-5.5	Vdc	1
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	–	7.0	Vdc	1
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4	–	7.0	Vdc	1
Logic 0 Voltage, all inputs	V_{IL}	-1.0	–	0.8	Vdc	1

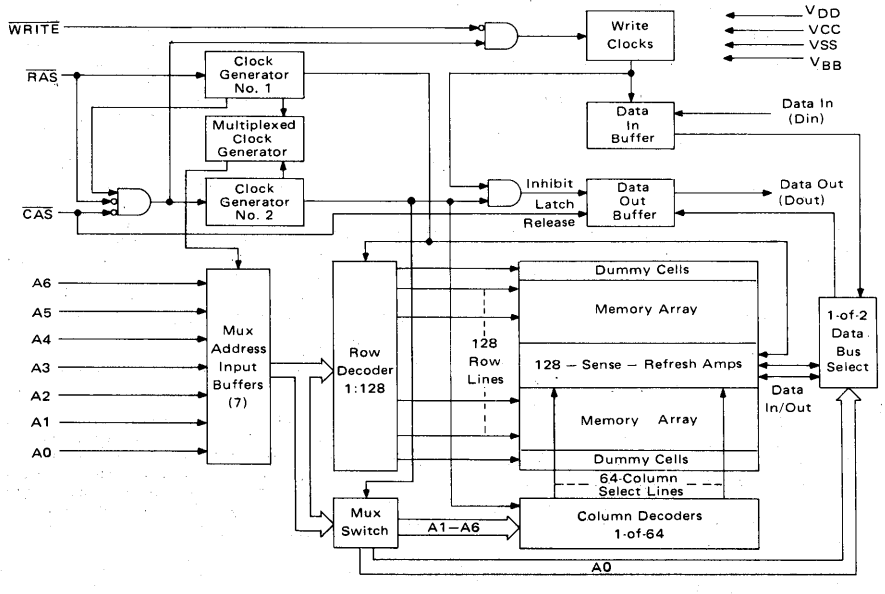
DC CHARACTERISTICS (V_{DD} = 12 V ±10%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

Characteristic	Symbol	Min	Max	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}	–	35	mA	4
V_{CC} Power Supply Current	I_{CC}	–	–	mA	5
Average V_{BB} Power Supply Current	$I_{BB1,3}$	–	200	µA	
Standby V_{BB} Power Supply Current	I_{BB2}	–	100	µA	
Standby V_{DD} Power Supply Current	I_{DD2}	–	1.5	mA	6
Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles	I_{DD3}	–	27	mA	4
Input Leakage Current (any input)	$I_{I(L)}$	–	10	µA	
Output Leakage Current	$I_{O(L)}$	–	10	µA	6, 7
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4	–	Vdc	2
Output Logic 0 Voltage @ I_{out} = 4.2 mA	V_{OL}	–	0.4	Vdc	

NOTES:

1. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
2. Output voltage will swing from V_{SS} to V_{CC} under open circuit conditions. For purposes of maintaining data in power-down mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations. V_{OH}(min) specification is not guaranteed in this mode.
3. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate.
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. Output is disabled (open-circuit) when $\overline{CAS}$ is at a logic 1.
7. $0 V \leq V_{out} \leq +5.5 V$.
8. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$.

BLOCK DIAGRAM



AC OPERATING CONDITIONS AND CHARACTERISTICS (See Notes 3, 9, 14)
(Read, Write, and Read-Modify-Write Cycles)

RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 12 V ±10%, V_{CC} = 5.0 V ±10%, V_{BB} = −5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

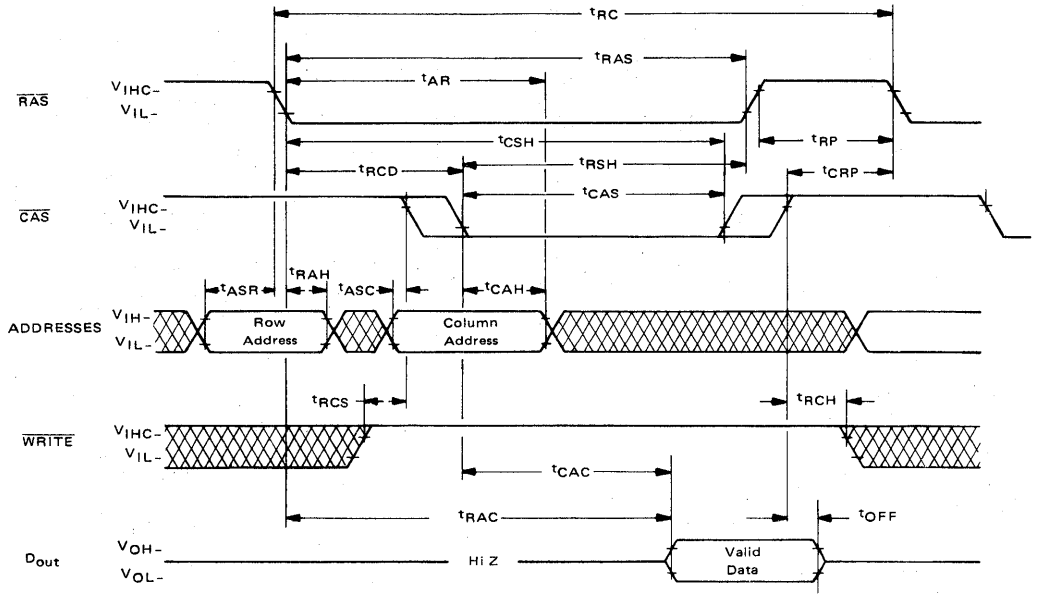
Parameter	Symbol	MCM4116B-15		MCM4116B-20		MCM4116B-25		MCM4116B-30		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	375	–	375	–	410	–	480	–	ns	
Read Write Cycle Time	t_{RWC}	375	–	375	–	515	–	660	–	ns	
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	–	250	–	300	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	100	–	135	–	165	–	200	ns	11, 12
Output Buffer and Turn-off Delay	t_{OFF}	0	50	0	50	0	60	0	60	ns	17
Row Address Strobe Precharge Time	t_{RP}	100	–	120	–	150	–	180	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	150	10,000	200	10,000	250	10,000	300	10,000	ns	
Column Address Strobe Pulse Width	t_{CAS}	100	10,000	135	10,000	165	10,000	200	10,000	ns	
Row to Column Strobe Lead Time	t_{RCD}	20	50	25	65	35	85	60	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	20	–	25	–	35	–	60	–	ns	
Column Address Setup Time	t_{ASC}	−10	–	−10	–	−10	–	−10	–	ns	
Column Address Hold Time	t_{CAH}	45	–	55	–	75	–	100	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	95	–	120	–	160	–	200	–	ns	
Transition Time (Rise and Fall)	t_T	3.0	35	3.0	50	3.0	50	3.0	50	ns	14
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Write Command Hold Time	t_{WCH}	45	–	55	–	75	–	100	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	95	–	120	–	160	–	200	–	ns	
Write Command Pulse Width	t_{WP}	45	–	55	–	75	–	100	–	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	60	–	80	–	100	–	180	–	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	60	–	80	–	100	–	180	–	ns	
Data in Setup Time	t_{DS}	0	–	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	45	–	55	–	75	–	100	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	95	–	120	–	160	–	200	–	ns	
Column to Row Strobe Precharge Time	t_{CRP}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100	–	135	–	165	–	200	–	ns	
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	–	2.0	ms	
$\overline{WRITE}$ Command Setup Time	t_{WCS}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	70	–	95	–	125	–	180	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	120	–	160	–	210	–	280	–	ns	16
$\overline{CAS}$ Precharge Time (Page mode cycle only)	t_{CP}	60	–	80	–	100	–	100	–	ns	
Page Mode Cycle Time	t_{PC}	170	–	225	–	275	–	325	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	150	–	200	–	250	–	300	–	ns	

Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A5), D_{in}	C_{I1}	4.0	5.0	pF	9
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8.0	10	pF	9
Output Capacitance (D_{out})	C_o	5.0	7.0	pF	7, 9

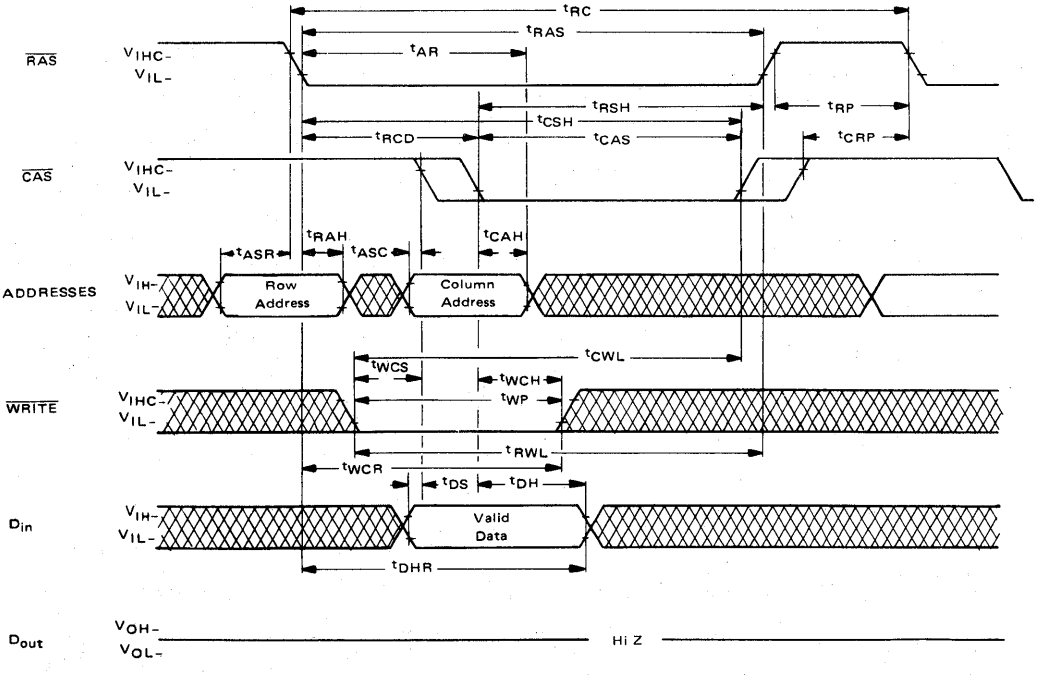
NOTES: (continued)

9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} + t_T \leq t_{RCD}$ (max).
11. Assumes that $t_{RCD} + t_T \geq t_{RCD}$ (max).
12. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Assumes that $t_{CRP} > 50$ ns.

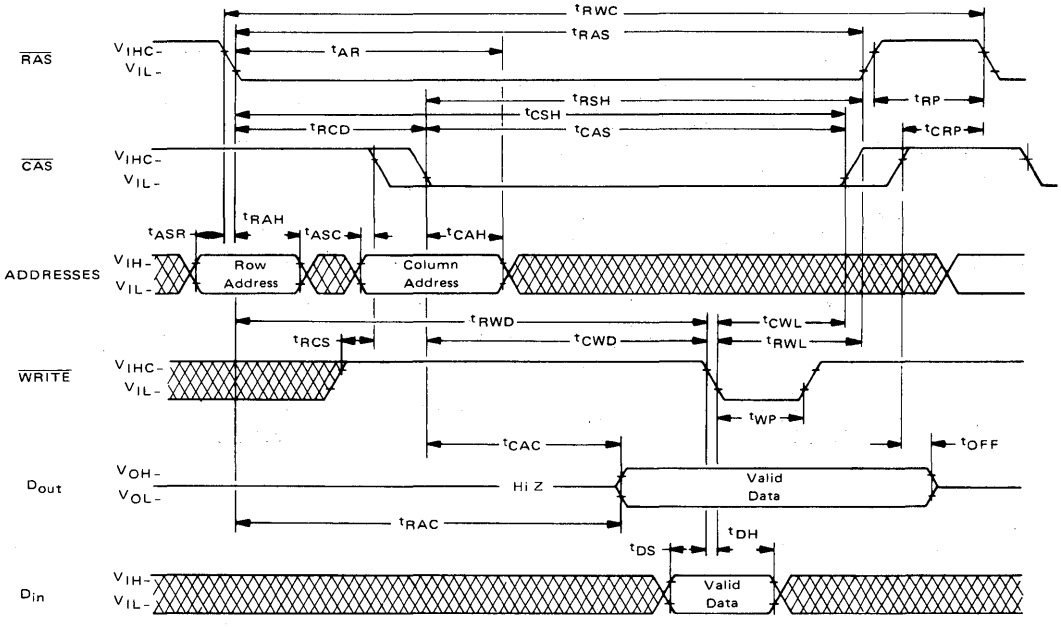
READ CYCLE TIMING



WRITE CYCLE TIMING

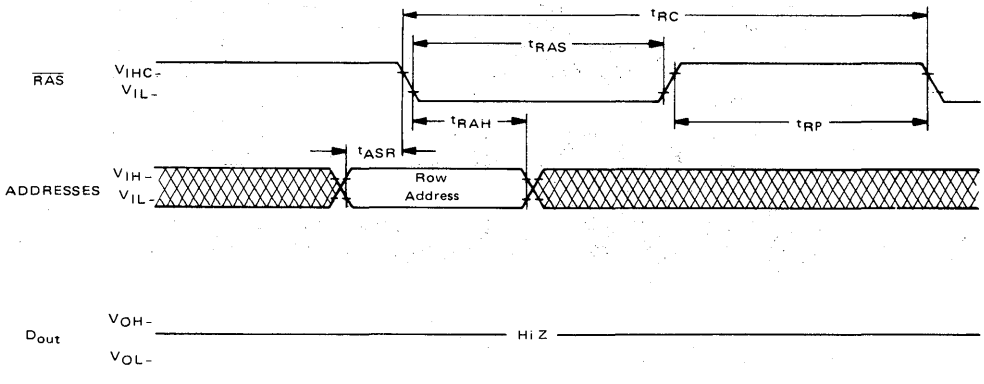


READ-WRITE/READ-MODIFY-WRITE CYCLE

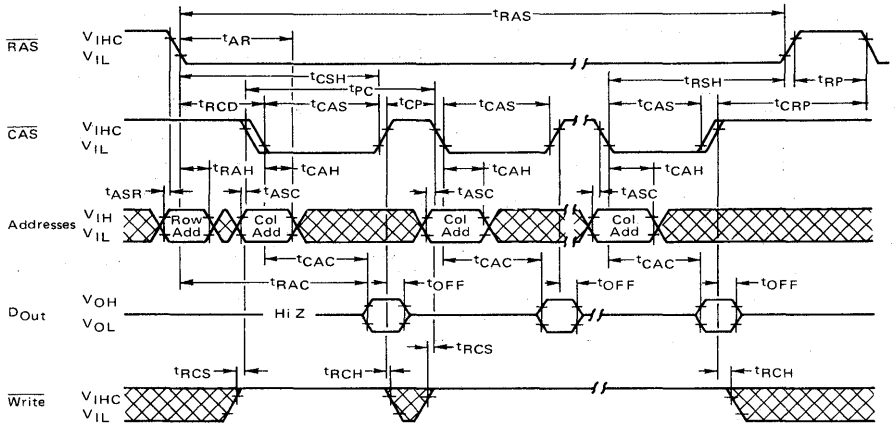


RAS ONLY REFRESH TIMING

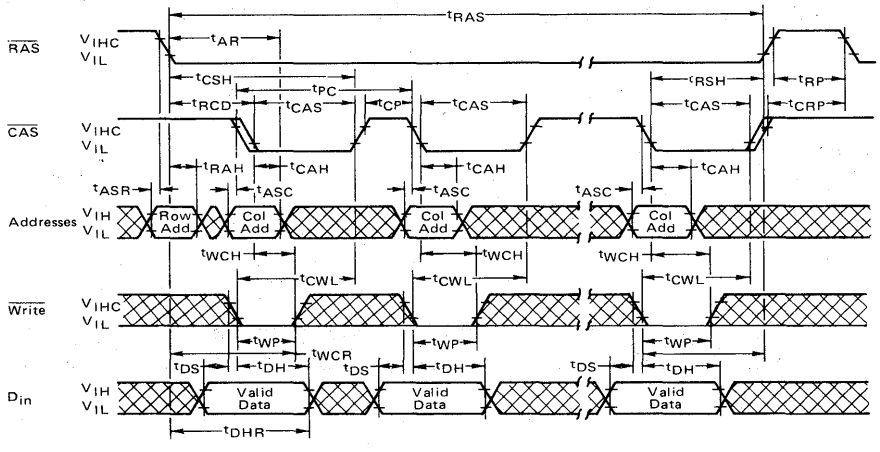
Note: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care



PAGE MODE READ CYCLE

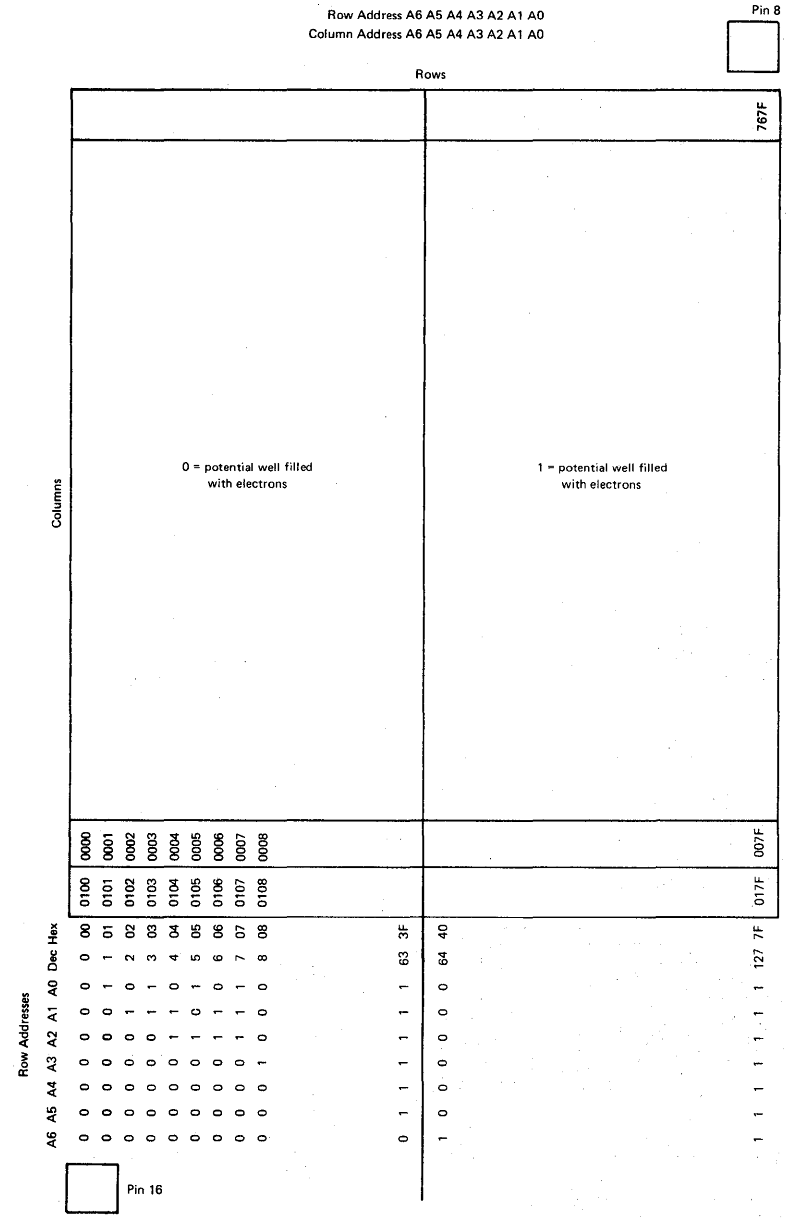


PAGE MODE WRITE CYCLE



MCM4116B BIT ADDRESS MAP

Row Address A6 A5 A4 A3 A2 A1 A0
Column Address A6 A5 A4 A3 A2 A1 A0



Column Addresses

Hex	Dec	A6	A5	A4	A3	A2	A1	A0
76	118	1	1	1	0	1	1	0
77	119	1	1	1	0	1	1	1
16	22	0	0	1	0	1	1	0
17	23	0	0	1	0	1	1	1
14	20	0	0	1	0	1	0	0
15	21	0	0	1	0	1	0	1
12	18	0	0	1	0	0	1	0
13	19	0	0	1	0	0	1	1
10	16	0	0	1	0	0	0	0
11	17	0	0	1	0	0	0	1
1E	30	0	0	1	1	1	1	0
1F	31	0	0	1	1	1	1	1
1C	28	0	0	1	1	1	0	0
1D	29	0	0	1	1	1	0	1
1A	26	0	0	1	1	0	1	0
1B	27	0	0	1	1	0	1	1
18	24	0	0	1	1	0	0	0
19	25	0	0	1	1	0	0	1
0E	14	0	0	0	1	1	1	0
0F	15	0	0	0	1	1	1	1
0C	12	0	0	0	1	1	0	0
0D	13	0	0	0	1	1	0	1
0A	10	0	0	0	1	0	1	0
0B	11	0	0	0	1	0	1	1
08	8	0	0	0	1	0	0	0
09	9	0	0	0	1	0	0	1
06	6	0	0	0	0	1	1	0
07	7	0	0	0	0	1	1	1
04	4	0	0	0	0	1	0	0
05	5	0	0	0	0	1	0	1
02	2	0	0	0	0	0	1	0
03	3	0	0	0	0	0	1	1
00	0	0	0	0	0	0	0	0
01	1	0	0	0	0	0	0	1

MOTOROLA

MCM4517

16,384-BIT DYNAMIC RAM

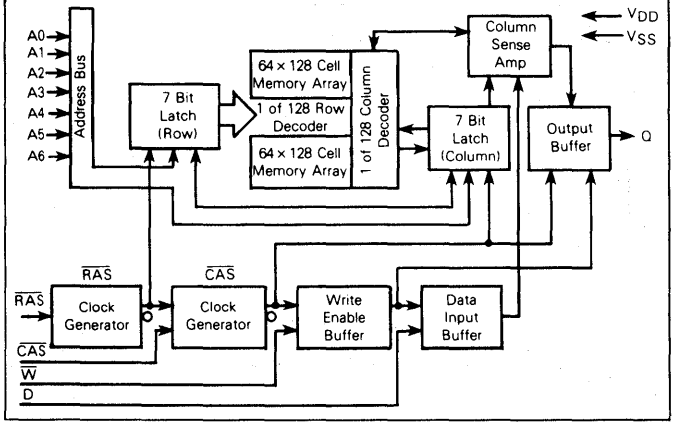
The MCM4517 is a 16,384-bit, high-speed, dynamic Random-Access Memory. Organized as 16,384 one-bit words and fabricated using HMOS high-performance, N-channel, silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM4517 requires only seven address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM4517 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 16,384 Words of 1 Bit
- Single +5 Volt Operation
- Fast 100 ns Operation
- Low Power Dissipation:
  170 mW Maximum (Active)
  14 mW Maximum (Standby)
- Maximum Access Time
  MCM4517-10 – 100 ns
  MCM4517-12 – 120 ns
  MCM4517-15 – 150 ns
  MCM4517-20 – 200 ns
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Output Capability
- 64K Compatible 128-cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatibility from the 16K RAM (MCM4116) to the 64K RAM (MCM6664)
- Allows Undershoot V_{IL} min = −2 V
- Hidden $\overline{RAS}$ Only Refresh Capability

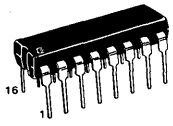
BLOCK DIAGRAM



MOS

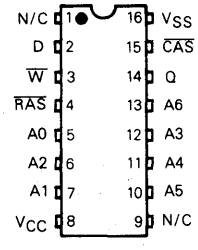
(N-CHANNEL, SILICON-GATE)

16,384-BIT
DYNAMIC RAM



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



PIN NAMES	
A0-A6	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

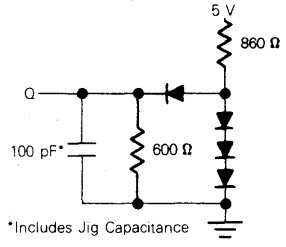
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	−2 to +7	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 – OUTPUT LOAD



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	–	$V_{CC}+1$	V	1
Logic 0 Voltage, All Inputs	V_{IL}	−2.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Units	Notes
V_{CC} Supply Current (Standby)	I_{CC1}	–	1.8	2.5	mA	5
V_{CC} Supply Current (Operating) 4517-10, t_{RC}=235 4517-12, t_{RC}=270 4517-15, t_{RC}=320 4517-20, t_{RC}=350	I_{CC2}	 – – – –	 22 20 18 16	 31 28 25 23	mA	4
V_{CC} Supply Current (RAS-Only Cycle) 4517-10, t_{RC}=235 4517-12, t_{RC}=270 4517-15, t_{RC}=320 4517-20, t_{RC}=350	I_{CC3}	 – – – –	 14 12 11 10	 23 21 19 18	mA	4
V_{CC} Standby Current (Standby, Output Enable) ($\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH})	I_{CC4}	–	2	5	mA	
V_{CC} Supply Current (Page Mode Cycle Only) 4517-10, t_{RC}=235 4517-12, t_{RC}=270 4517-15, t_{RC}=320 4517-20, t_{RC}=350	I_{CC5}	 – – – –	 17 15 13 10	 23 21 18 15	mA	
Input Leakage Current (Any Input) ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{I(L)}$	–	–	10	µA	
Output Leakage Current ($0 \le V_{out} \le 5.5$) ($\overline{CAS}$ at Logic 1)	$I_{O(L)}$	–	–	10	µA	
Output Logic 1 Voltage@I_{out}= −4 mA	V_{OH}	2.4	–	–	V	
Output Logic 0 Voltage@I_{out}=4 mA	V_{OL}	–	–	0.4	V	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

(See Notes 2, 3, 9, 14 and Figure 1)

Parameter	Symbol	MCM4517-10		MCM4517-12		MCM4517-15		MCM4517-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	235	–	270	–	320	–	360	–	ns	8, 9
Read-Modify-Write Cycle Time	t_{RWC}	285	–	320	–	410	–	440	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	100	–	120	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	55	–	65	–	80	–	120	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	45	0	50	0	60	0	70	ns	18
Row Address Strobe Precharge Time	t_{RP}	110	–	120	–	135	–	150	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	115	10000	140	10000	175	10000	200	10000	ns	19
Column Address Strobe Pulse Width	t_{CAS}	55	10000	65	10000	95	10000	120	10000	ns	19
Row to Column Strobe Lead Time	t_{RCD}	25	45	25	55	25	70	30	80	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	25	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	15	–	15	–	20	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	60	–	70	–	90	–	140	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	6

AC OPERATING CONDITIONS AND CHARACTERISTICS (Continued)

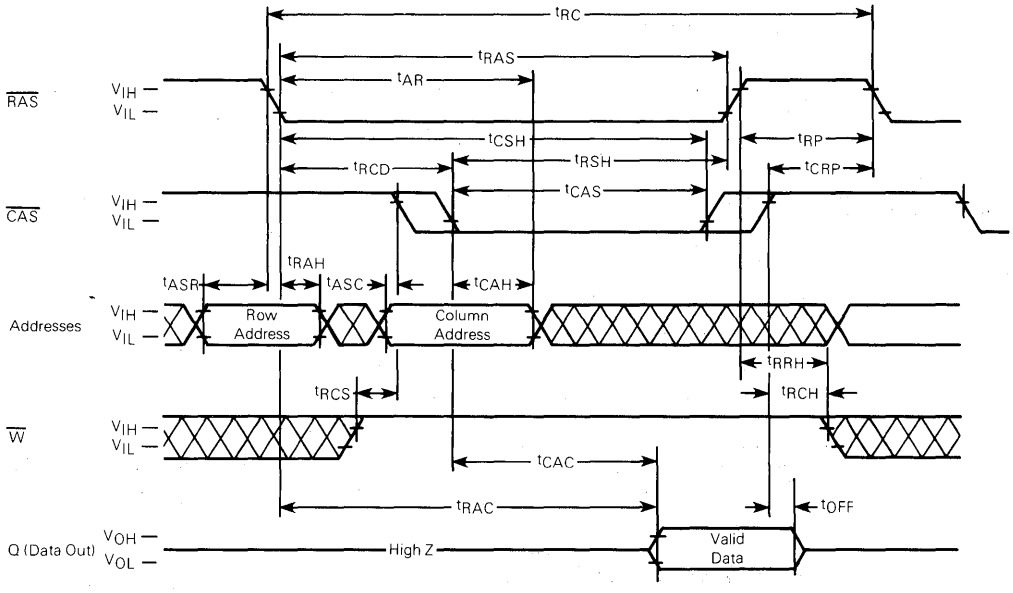
Parameter	Symbol	MCM4517-10		MCM4517-12		MCM4517-15		MCM4517-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	20	–	25	–	35	–	40	–	ns	14
Write Command Hold Time	t_{WCH}	25	–	30	–	45	–	60	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	70	–	85	–	115	–	140	–	ns	
Write Command Pulse Width	t_{WP}	25	–	30	–	50	–	50	–	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	60	–	65	–	110	–	110	–	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	45	–	50	–	100	–	100	–	ns	
Data in Setup Time	t_{DS}	0	–	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	25	–	30	–	45	–	60	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	70	–	85	–	115	–	140	–	ns	
Column to Row Strobe Precharge Time	t_{CRP}	0	–	0	–	0	–	0	–	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	70	–	85	–	105	–	120	–	ns	
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	–	2.0	ms	
Write Command Setup Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	55	–	65	–	80	–	100	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	100	–	120	–	150	–	160	–	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	165	–	200	–	ns	
$\overline{CAS}$ Precharge, Non Page Mode	t_{CPN}	50	–	55	–	70	–	90	–	ns	
RMW Cycle $\overline{RAS}$ Pulse Width	t_{RRW}	135	10000	160	10000	195	10000	220	10000	ns	
RMW Cycle $\overline{CAS}$ Pulse Width	t_{CRW}	95	10000	110	10000	130	10000	140	10000	ns	
Page Mode Cycle Time	t_{PC}	125	–	145	–	190	–	260	–	ns	
Page Mode Cycle Time (Read-Modify-Write)	t_{PCM}	175	–	200	–	280	–	360	–	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CP}	60	–	70	–	85	–	105	–	ns	
$\overline{RAS}$ Pulse Width (Page Mode Cycle Only)	t_{RPM}	115	10000	140	10000	175	10000	235	10000	ns	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = +5 V. Periodically sampled rather than 100% tested.)

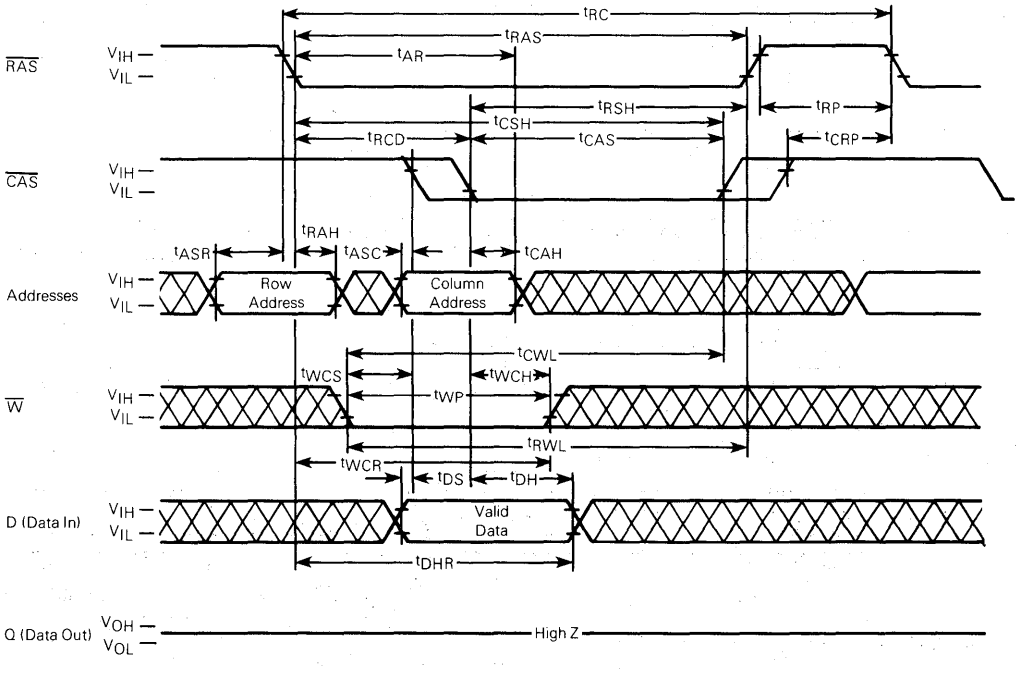
Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A6), D_{in}	C_{I1}	4.0	5.0	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	5.0	7.0	pF	7

NOTES:
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = i\Delta t/\Delta V$
8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (Max)
11. Assumes that $t_{RCD} \geq t_{RCD}$ (Max)
12. Measured with a current load equivalent to 2 TTL loads (+200 μA, −4 mA) and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. Addresses, data-in and $\overline{WRITE}$ are don't care. Data-out depends on the state of $\overline{CAS}$. If $\overline{CAS}$ remains low, the previous output will remain valid. $\overline{CAS}$ is allowed to make an active to inactive transition during the $\overline{RAS}$-only refresh cycle. When $\overline{CAS}$ is brought high, the output will assume a high-impedance state.
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
19. For read and write cycles only.

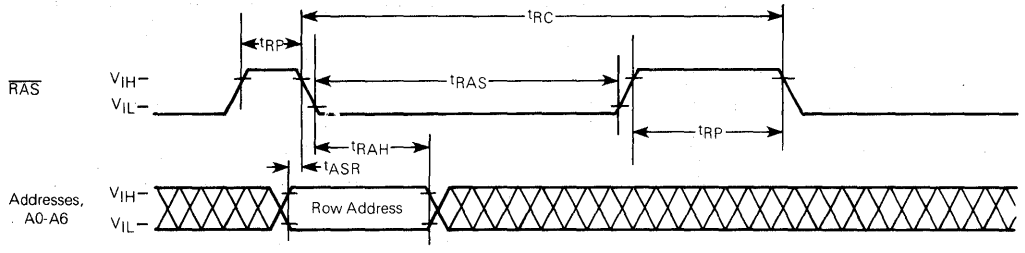
READ CYCLE TIMING



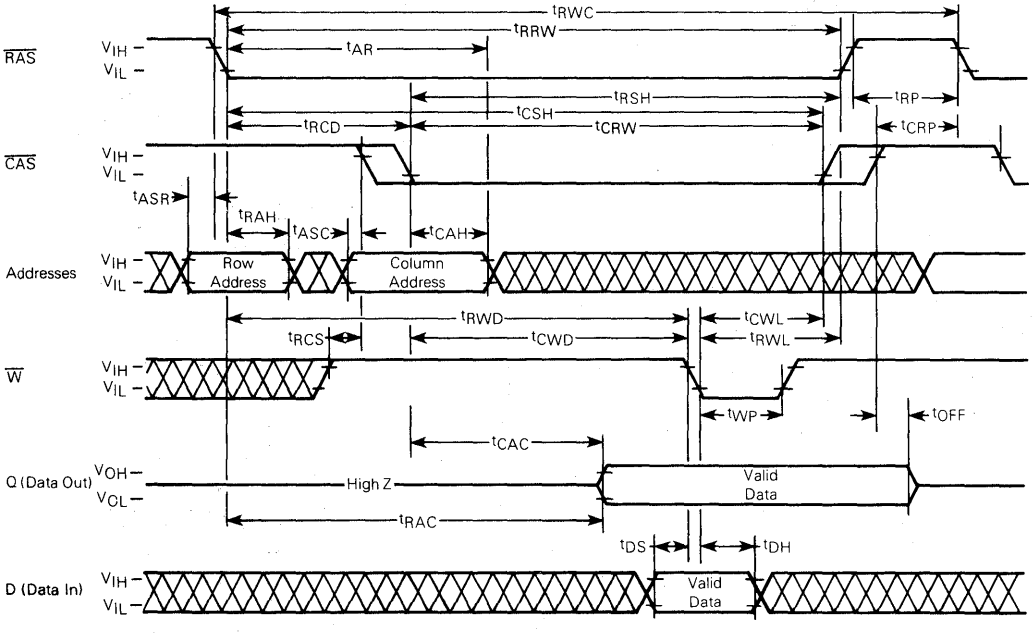
WRITE CYCLE TIMING



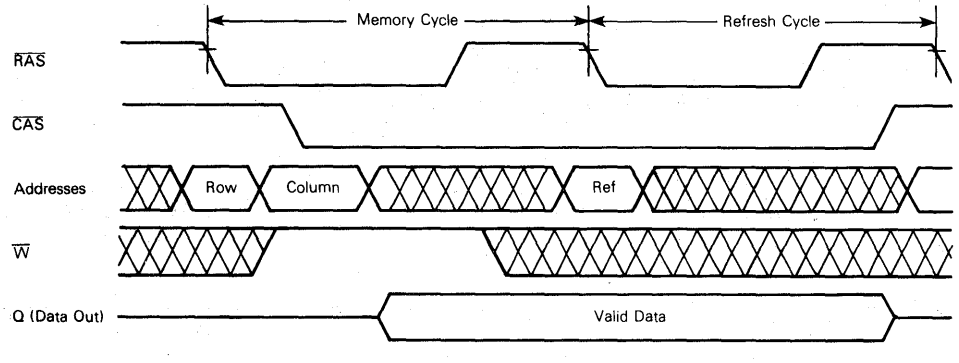
RAS-ONLY REFRESH CYCLE
(Data-In and Write are Don't Care, CAS is HIGH)



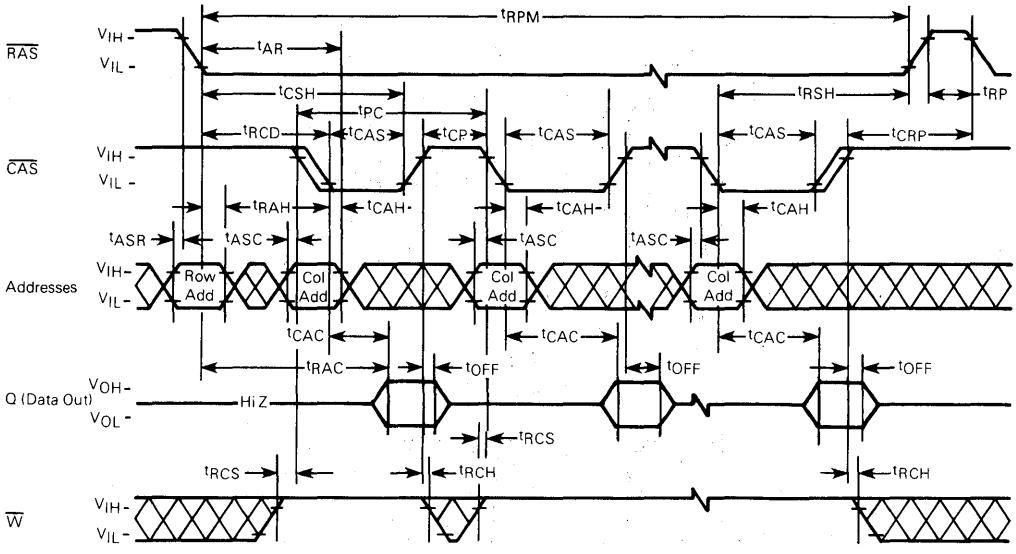
READ-WRITE/READ-MODIFY-WRITE CYCLE



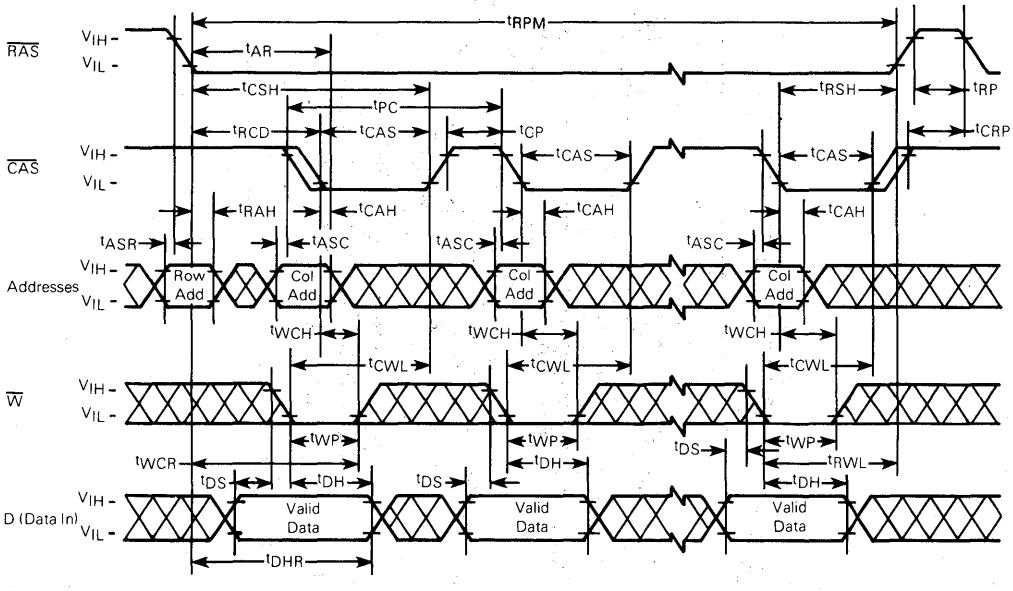
HIDDEN RAS-ONLY REFRESH CYCLE



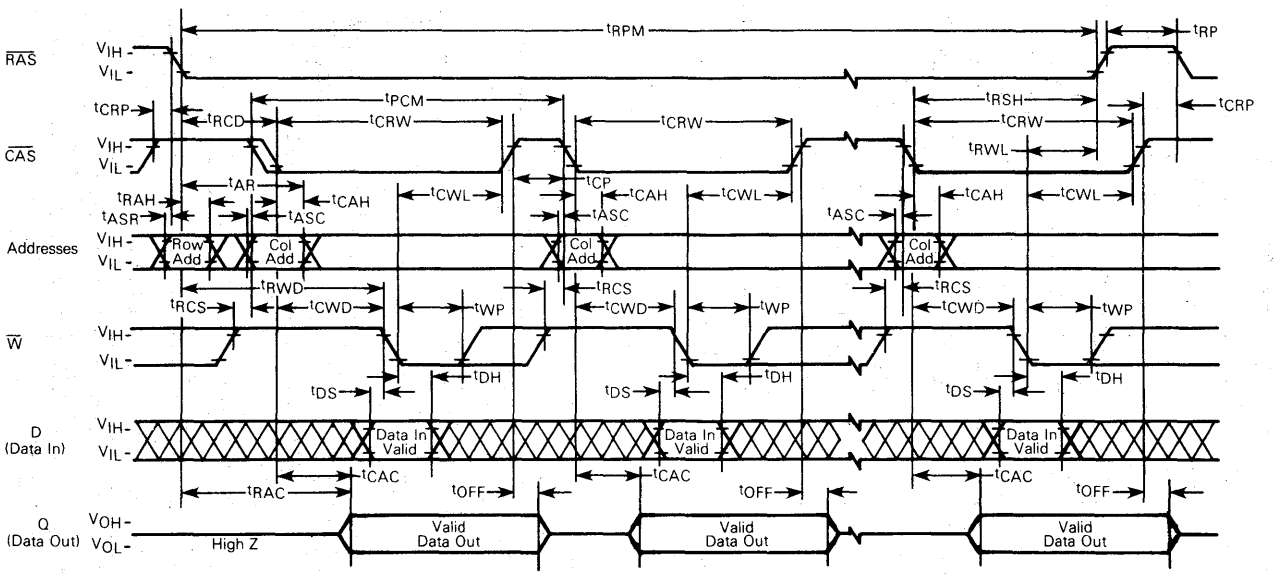
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



PAGE MODE READ-MODIFY-WRITE CYCLE



MOTOROLA

MCM6665A

MOS
(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

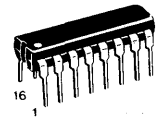
64K BIT DYNAMIC RAM

The MCM6665A is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, this new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6665A requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

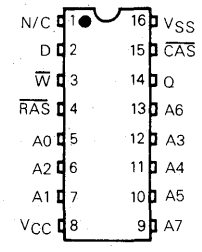
All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665A incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation (± 10%)
- Full Power Supply Range Capabilities
- Maximum Access Time
  MCM6665A-15 = 150 ns
  MCM6665A-20 = 200 ns
- Low Power Dissipation
  302.5 mW Maximum (Active) (MCM6665A-15)
  22 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)
- Fast Page Mode Cycle Time
- Low Soft Error Rate <0.1% per 1000 Hours (See Soft Error Testing)



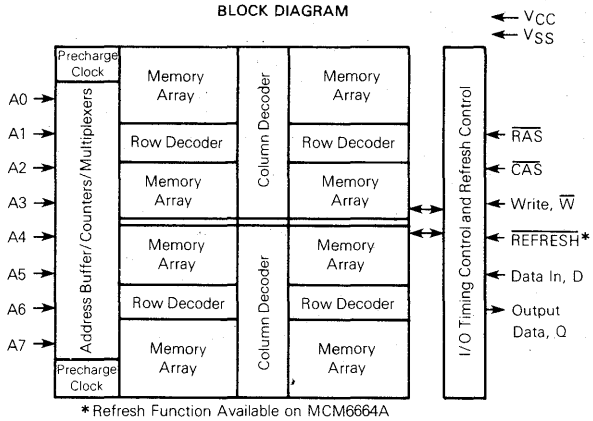
P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



PIN NAMES	
A0-A7	Address Input
D	Data In
Q	Data Out
W	Read/Write Input
RAS	Row Address Strobe
CAS	Column Address Strobe
VCC	Power (+5 V)
VSS	Ground

BLOCK DIAGRAM



*Refresh Function Available on MCM6664A

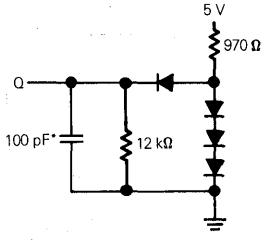
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (except V_{CC})	V_{in}, V_{out}	−2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	–	V_{CC}+1	V	1
Logic 0 Voltage, All Inputs	V_{IL}	−1.0*	–	0.8	V	1

*The device will withstand undershoots to the −2 volt level with a maximum pulse width of 20 ns at the −1.5 volt level. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (Standby)	I_{CC2}	–	4.0	mA	5
V_{CC} Power Supply Current 6665A-15, t_{RC} = 270 ns 6665A-20, t_{RC} = 330 ns	I_{CC1}	– –	55 50	mA	4
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles 6665A-15, t_{RC} = 270 ns 6665A-20, t_{RC} = 330 ns	I_{CC3}	– –	45 40	mA	4
V_{CC} Power Supply Current During Page Mode Cycle for t_{RAS} = 10 μsec 6665A-15, t_{PC} = t_{RP} = 145 ns 6665A-20, t_{PC} = t_{RP} = 200 ns	I_{CC4}	– –	40 35	mA	4
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{I(L)}$	–	10	μA	–
Output Leakage Current ($\overline{CAS}$ at logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{O(L)}$	–	10	μA	–
Output Logic 1 Voltage @ I_{out} = −4 mA	V_{OH}	2.4	–	V	–
Output Logic 0 Voltage @ I_{out} = 4 mA	V_{OL}	–	0.4	V	–

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A7), D	C_{I1}	3	5	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	6	8	pF	7
Output Capacitance (Q), ($\overline{CAS}$ = V_{IH} to disable output)	C_O	5	7	pF	7

NOTES:
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is guaranteed
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta t}{\Delta V}$

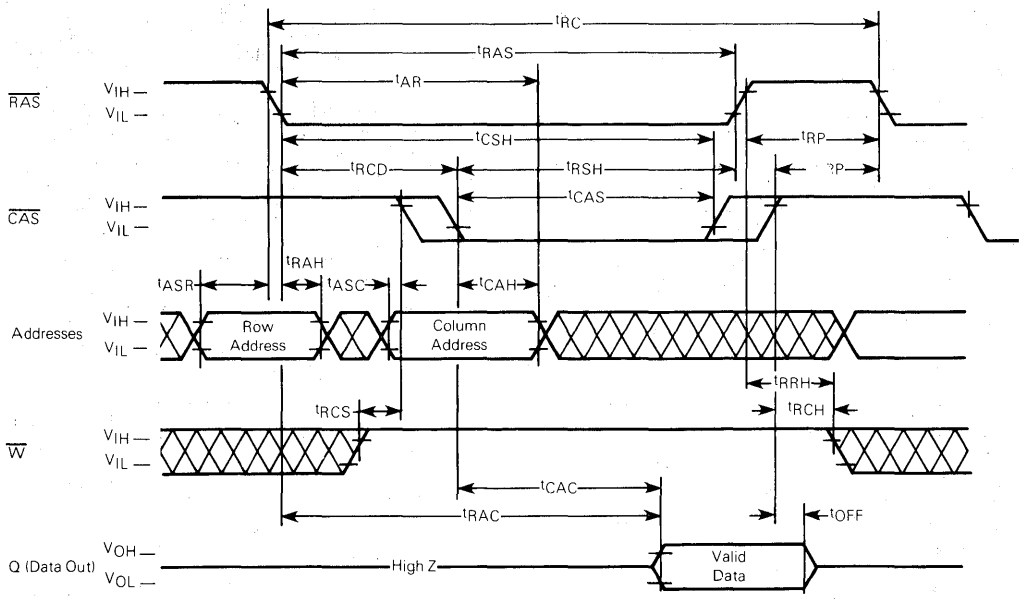
AC OPERATING CONDITIONS AND CHARACTERISTICS (Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted; See Notes 2, 3, 6, and Figure 1)

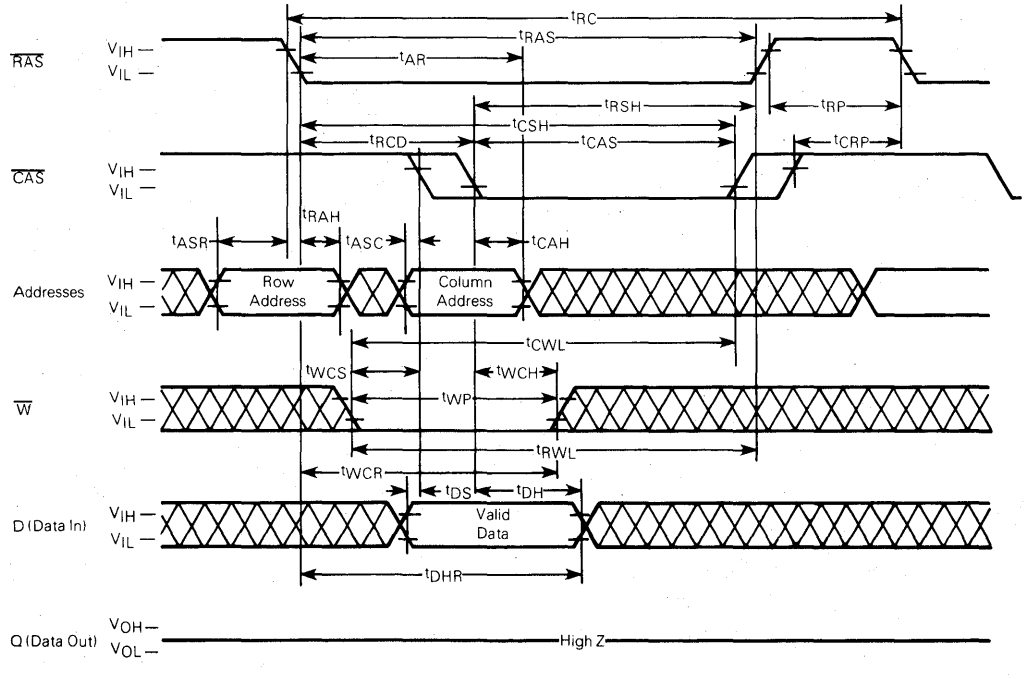
Parameter	Symbol	6665A-15		6665A-20		Units	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	270	–	330	–	ns	8, 9
Read Write Cycle Time	t_{RWC}	280	–	330	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	75	–	100	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	40	ns	18
Row Address Strobe Precharge Time	t_{RP}	100	–	120	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	150	10000	200	10000	ns	–
Column Address Strobe Pulse Width	t_{CAS}	75	10000	100	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	30	75	30	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	ns	–
Row Address Hold Time	t_{RAH}	20	–	25	–	ns	–
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	–
Column Address Hold Time	t_{CAH}	35	–	45	–	ns	–
Column Address Hold Time Referenced to RAS	t_{AR}	95	–	120	–	ns	17
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	6
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	–
Read Command Hold Time	t_{RCH}	0	–	0	–	ns	14
Read Command Hold Time Referenced to RAS	t_{RRH}	0	–	0	–	ns	14
Write Command Hold Time	t_{WCH}	35	–	45	–	ns	–
Write Command Hold Time Referenced to RAS	t_{WCR}	95	–	120	–	ns	17
Write Command Pulse Width	t_{WP}	35	–	45	–	ns	–
Write Command to Row Strobe Lead Time	t_{RWL}	45	–	55	–	ns	–
Write Command to Column Strobe Lead Time	t_{CWL}	45	–	55	–	ns	–
Data in Setup Time	t_{DS}	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	35	–	45	–	ns	15
Data in Hold Time Referenced to RAS	t_{DHR}	95	–	120	–	ns	17
Column to Row Strobe Precharge Time	t_{CRP}	−10	–	−10	–	ns	–
RAS Hold Time	t_{RSH}	75	–	100	–	ns	–
Refresh Period	t_{RFSH}	–	2.0	–	2.0	ms	–
WRITE Command Setup Time	t_{WCS}	−10	–	−10	–	ns	16
CAS to WRITE Delay	t_{CWD}	45	–	55	–	ns	16
RAS to WRITE Delay	t_{RWD}	120	–	155	–	ns	16
CAS Hold Time	t_{CSH}	150	–	200	–	ns	–
CAS Precharge Time (Page Mode Cycle Only)	t_{CP}	60	–	80	–	ns	–
Page Mode Cycle Time	t_{PC}	145	–	200	–	ns	–

8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
9. AC measurements $t_T = 5.0$ ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. t_{AR} min $\leq t_{AR} = t_{RCD} + t_{CAH}$
    t_{DHR} min $\leq t_{DHR} = t_{RCD} + t_{DH}$
    t_{WCR} min $\leq t_{WCR} = t_{RCD} + t_{WCH}$
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

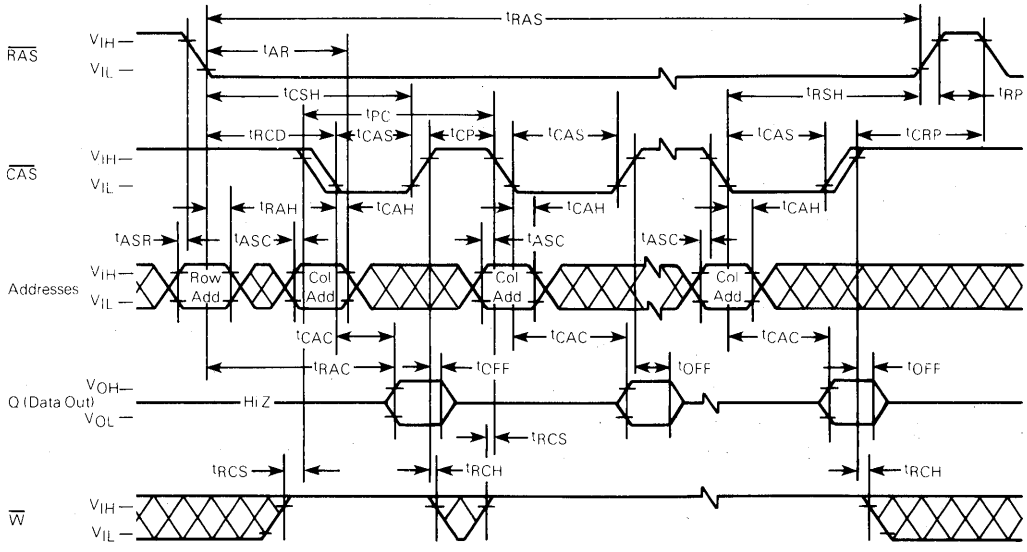
READ CYCLE TIMING



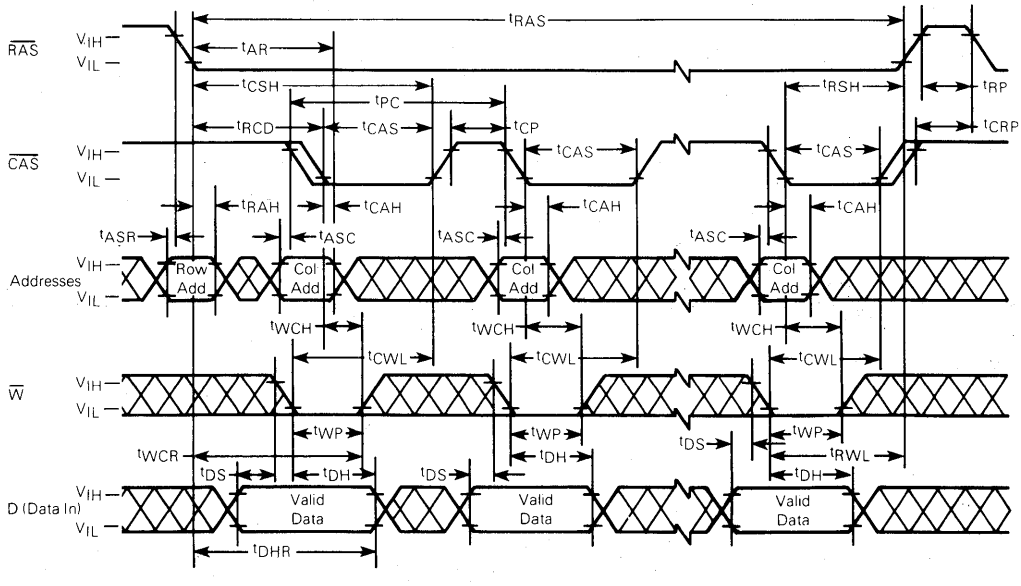
WRITE CYCLE TIMING



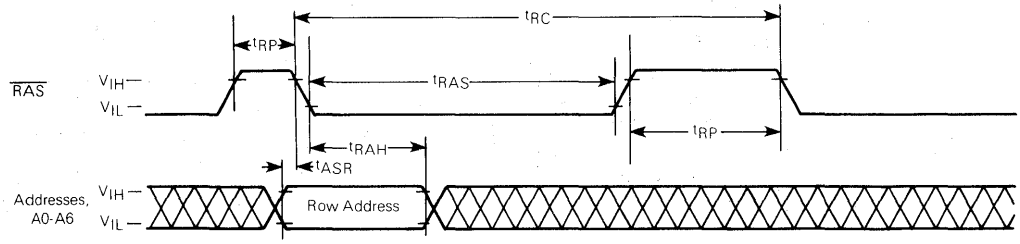
PAGE MODE READ CYCLE



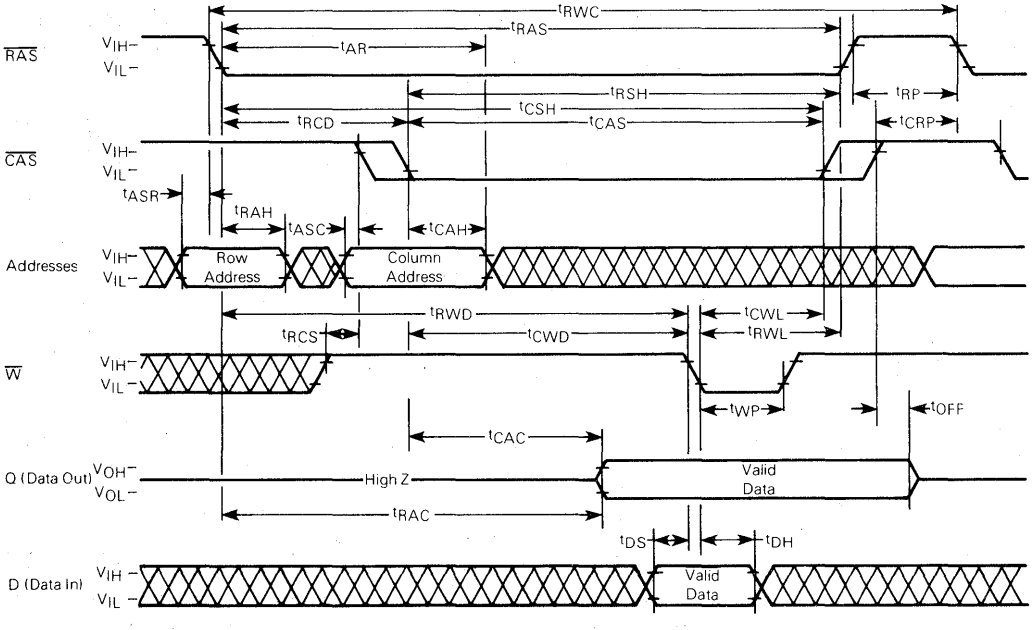
PAGE MODE WRITE CYCLE



RAS-ONLY REFRESH CYCLE
(Data-in and Write are Don't Care, CAS is HIGH)



READ-WRITE/READ-MODIFY-WRITE CYCLE



TYPICAL CHARACTERISTICS

FIGURE 2 — $\overline{RAS}$ ACCESS TIME versus SUPPLY VOLTAGE

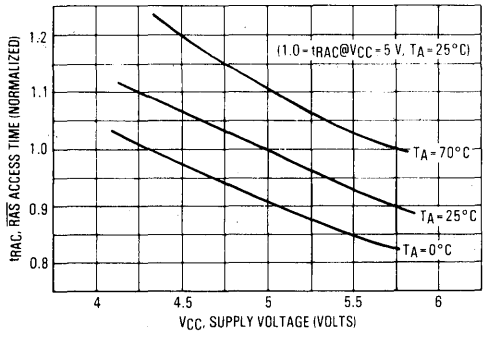


FIGURE 3 — $\overline{CAS}$ ACCESS TIME versus SUPPLY VOLTAGE

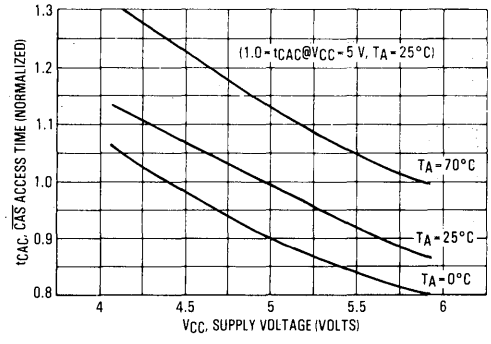


FIGURE 4 — $\overline{RAS}$ ACCESS TIME versus AMBIENT TEMPERATURE

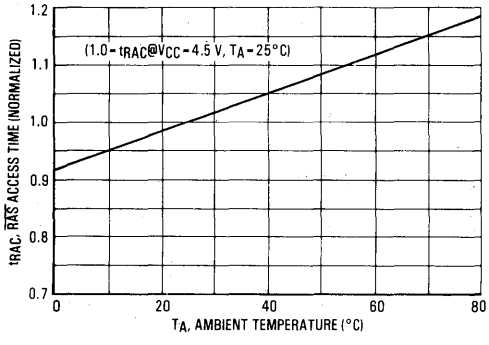


FIGURE 5 — $\overline{CAS}$ ACCESS TIME versus AMBIENT TEMPERATURE

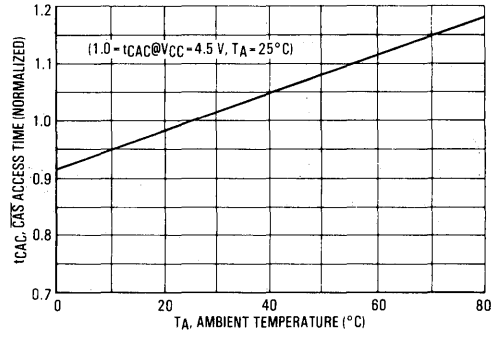


FIGURE 6 — $\overline{RAS}$, $\overline{W}$ INPUT LEVEL versus SUPPLY VOLTAGE

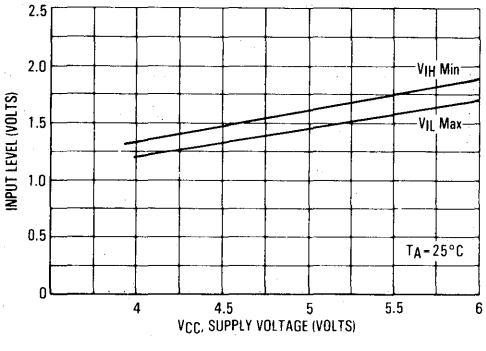
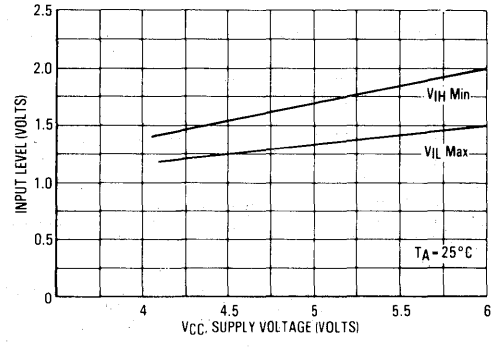


FIGURE 7 — $\overline{CAS}$, $\overline{W}$ INPUT LEVEL versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – I_{CC1} SUPPLY CURRENT versus CYCLE RATE

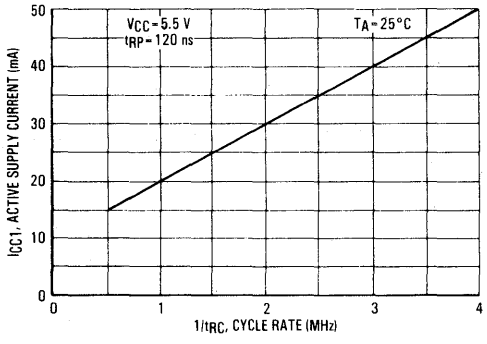


FIGURE 9 – I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

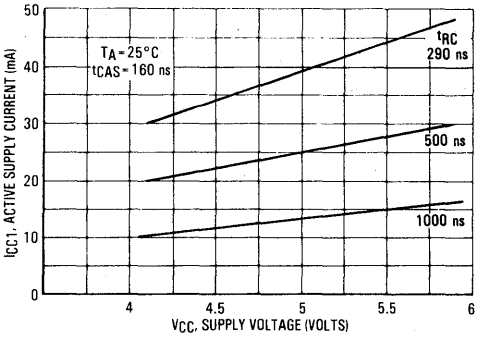


FIGURE 10 – I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

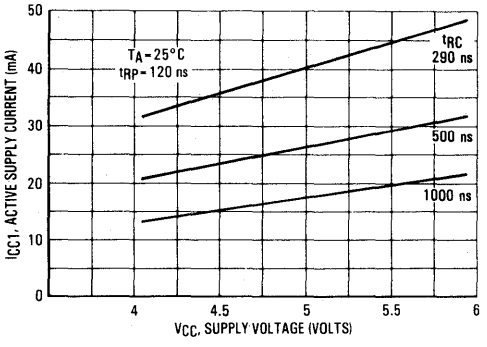


FIGURE 11 – I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min t_{RP})

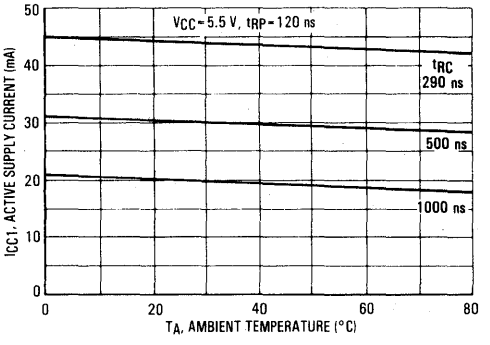


FIGURE 12 – I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min $\overline{RAS}$)

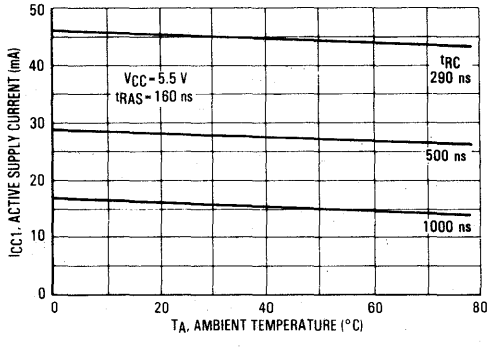
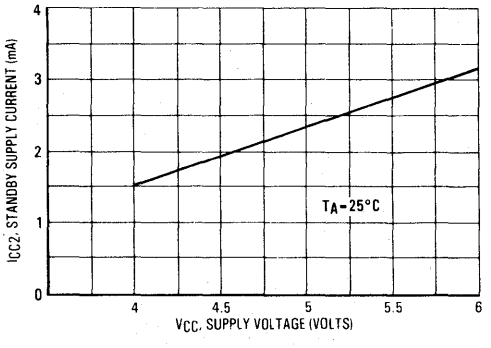


FIGURE 13 – I_{CC2} SUPPLY CURRENT versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 14 – I_{CC2} STANDBY CURRENT versus AMBIENT TEMPERATURE

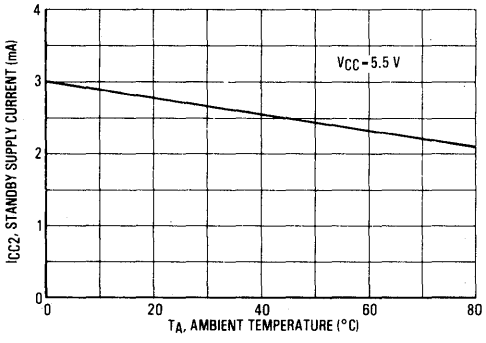


FIGURE 15 – I_{CC3} SUPPLY CURRENT versus CYCLE RATE

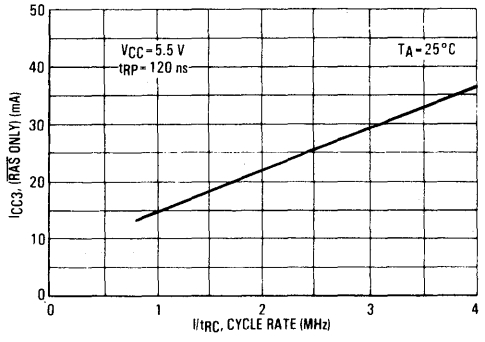


FIGURE 16 – ADDRESS INPUT LEVEL versus SUPPLY VOLTAGE

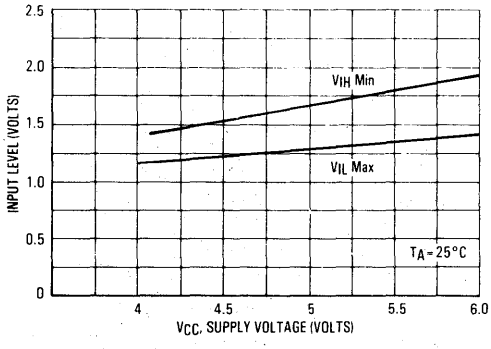
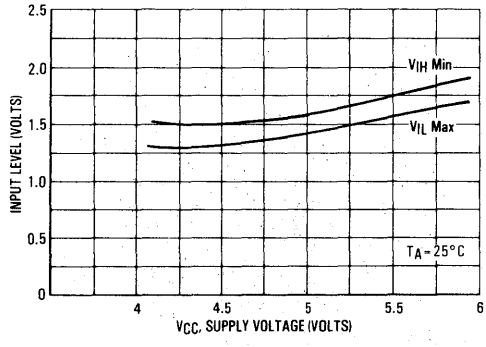


FIGURE 17 – DATA INPUT LEVEL versus SUPPLY VOLTAGE



SOFT ERROR TESTING

The storage cell depletion regions as well as the sense amplifier and its associated bit lines are susceptible to charge collection of electrons from an alpha "hit." However, the susceptibility of these vulnerable regions varies. Depleted storage cells are vulnerable at all times, whereas the sense amplifiers and associated bit lines are susceptible only during the small portion of the memory cycle just prior to sensing. Hence, an increase in the frequency of dynamic RAM access will cause a corresponding increase in the soft error rate.

To take this memory access dependency into account, the total soft error rate profile includes a cycle time component. The soft error rate due to bit line hits at the system's memory cycle rate is added to the soft error rate due to storage cell hits which are not frequency dependent. Figure 18 illustrates the impact that frequency of access has on the MCM6664A/MCM6665A overall soft error rate.

Under normal operating conditions, the die will be exposed to radiation levels of less than 0.01 alpha/cm^2/hr. Accelerated soft error testing data is generated from at least three high-intensity sources having an Alpha Flux Density range of 1×10^5 to 6×10^5 (alpha/cm^{2}hr) placed over uncoated die. Figure 19 shows the soft error rate for a given alpha flux density at a cycle rate of 100 kHz. The accelerated data of Figures 18 and 19 project that the soft error rate for package level radiation will be less than 0.1%/1000 hours.

SYSTEM LIFE OPERATING TEST CONDITIONS

1) Cycle time: 1 microsecond for read, write and refresh cycles
2) Refresh Rate: 1 millisecond
3) Voltage: 5.0 V
4) Temperature: 30° C ±2° C (ambient temperature inside enclosure)
5) Elevation: Approximately 620 feet above mean sea level
6) Data Patterns: Write the entire memory space sequentially with all "1"s and then perform continuous sequential reads for 6 hours. Next, write the entire memory space with all "0"s sequentially and then perform continuous sequential reads for 6 hours. Next, go back to the all "1"s pattern and repeat the sequences all over again.

FIGURE 18 — ACCELERATED SOFT ERROR versus CYCLE TIME

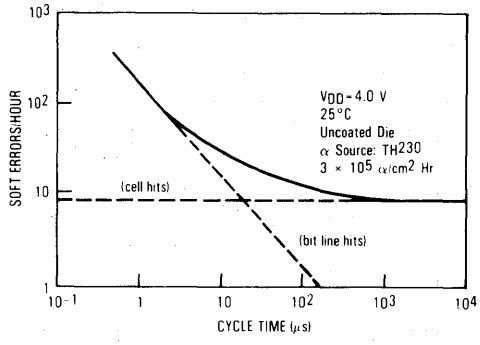
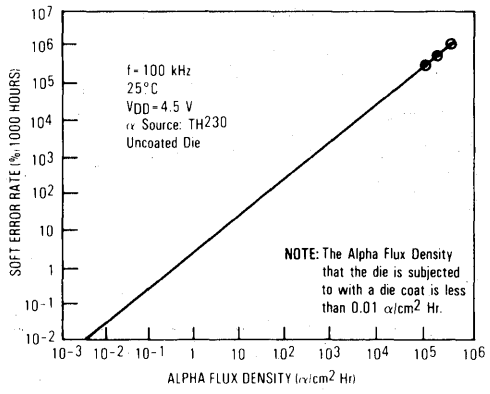


FIGURE 19 — SOFT ERROR RATE versus ALPHA FLUX DENSITY



CURRENT WAVEFORMS

FIGURE 20 — $\overline{RAS}$/$\overline{CAS}$ CYCLE

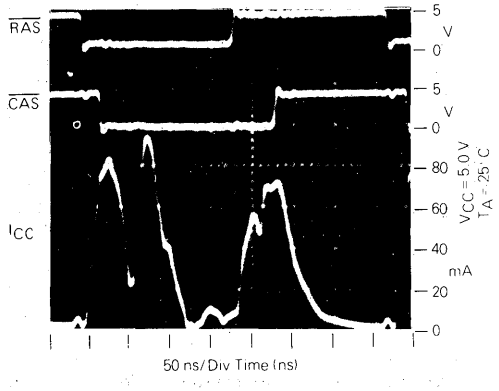


FIGURE 21 — LONG $\overline{RAS}$/$\overline{CAS}$ CYCLE

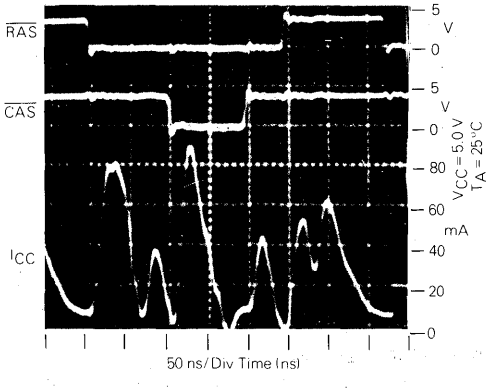


FIGURE 22 — $\overline{RAS}$ ONLY CYCLE

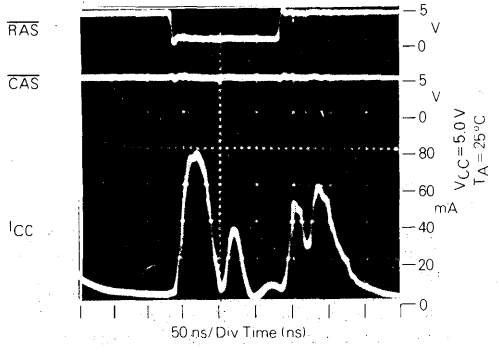


FIGURE 23 — PAGE MODE CYCLE

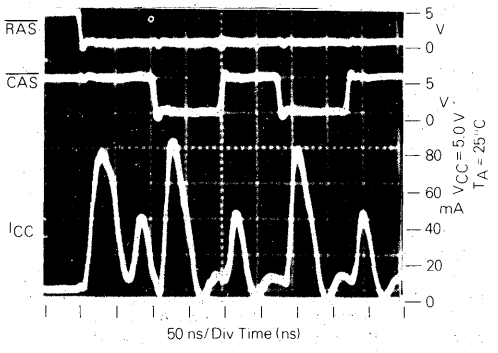
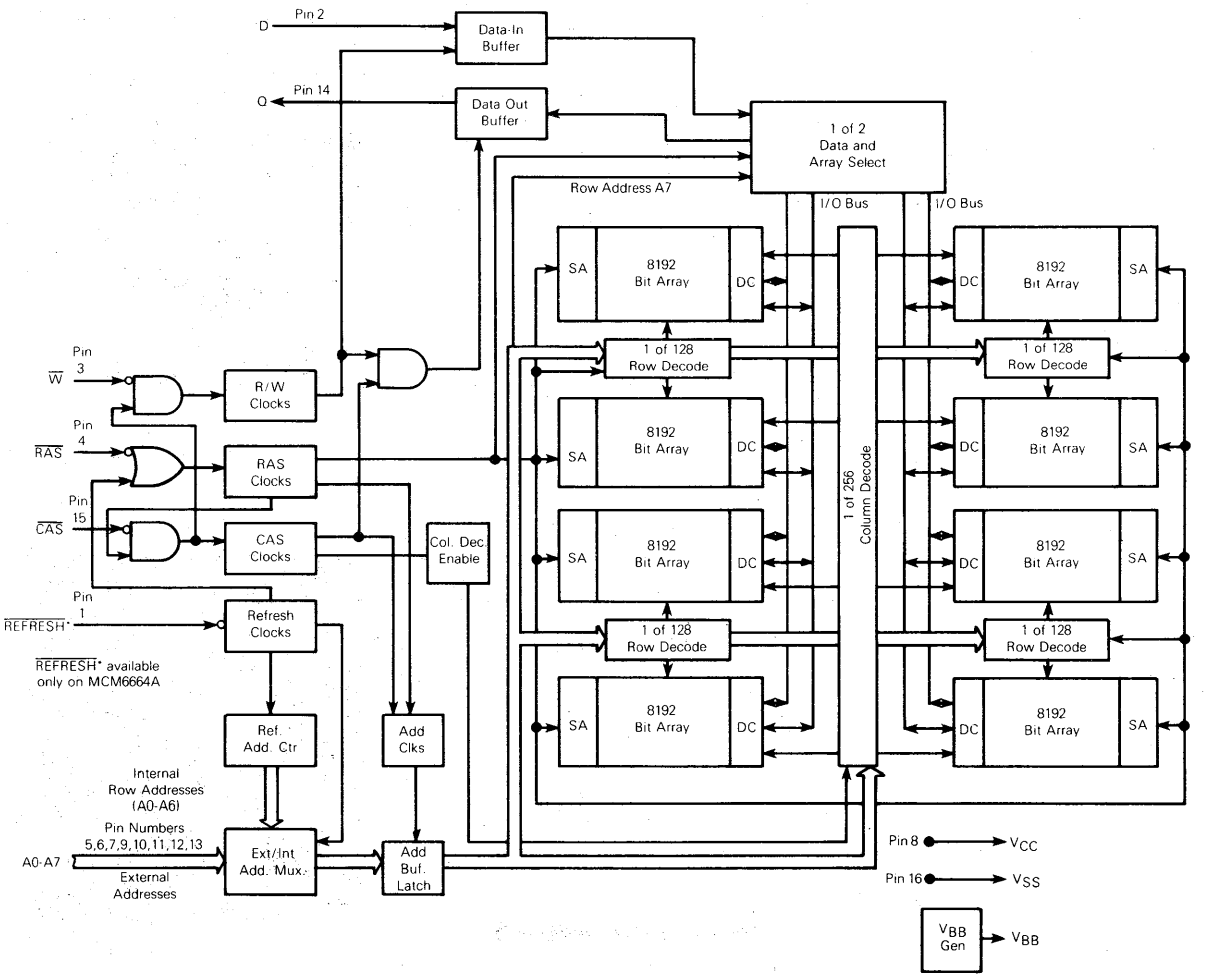


FIGURE 24 — FUNCTIONAL BLOCK DIAGRAM



DEVICE INITIALIZATION

Since the 64K dynamic RAM is a single supply 5 V only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up an initial pause of 100 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 2 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation. See Figures 25, 26 for power on characteristics of the RAM for two conditions (clocks active, clocks inactive).

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinguishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive-going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe and the column address strobe. A total of sixteen address bits will decode one of the 65,536 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 64K RAM: one is called the page mode cycle (described later) where an 8-bit column address field is presented on the input pins and latched by the $\overline{CAS}$ clock, and the other is the $\overline{RAS}$ only refresh cycle (described later) where a 7-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. In the latter case, the most significant bit on Row Address A7 (pin 9) is not required for refresh. See bit address map for the topology of the cells and their address selection.

NORMAL READ CYCLE

A read cycle is referred to as normal read cycle to differentiate if from a page-mode-read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at

CURRENT WAVEFORMS

FIGURE 25 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{RAS}$, $\overline{CAS}$ = V_{CC}

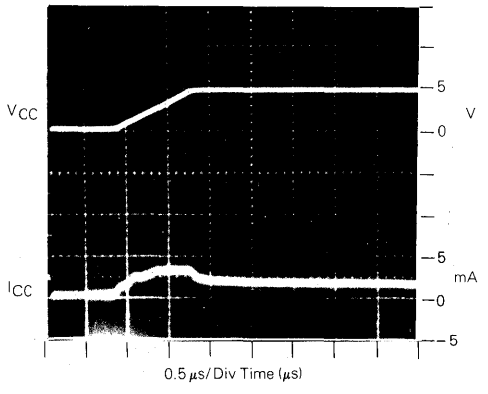
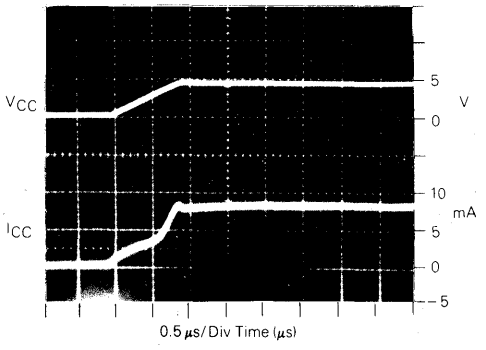


FIGURE 26 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{RAS}$, $\overline{CAS}$ = V_{SS}



the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available, as noted in the functional block diagram, Figure 24. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. The $\overline{CAS}$ clock can remain active for a maximum of 10 ns (t_{CRP}) into the next cycle. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as a early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisifed before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds $- [t_{RWL} + t_{RP} + 2T_t]$.

At the start of a write cycle, the data out is in a three-state condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers as noted in Functional Block Diagram. The three-state condition (high impedance) of the Data Out Pin during a write cycle can be effectively utilized in a system that has a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle is accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, the following parameters (t_{RWD}, t_{CWD}) play an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{RWD} and t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows faster successive data operations at the 256 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 64K dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 8-bit column address field. There are two controlling factors that limit the access to all 256 column locations in one $\overline{RAS}$ clock active operation. These are the refresh interval of the device (2 ms/128 = 15.6 microseconds) and the maximum active time specification for the $\overline{RAS}$ clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the $\overline{RAS}$ clock on time is the limiting factor of the number of sequential page accesses possible. Ten microseconds will provide approximately (10 microseconds/page mode cycle time) 50 successive page accesses for every row address selected before the $\overline{RAS}$ clock is reset.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. The page mode cycles illustrated show a series of sequential reads separated by a series of sequential writes. This is just one mode of operation. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

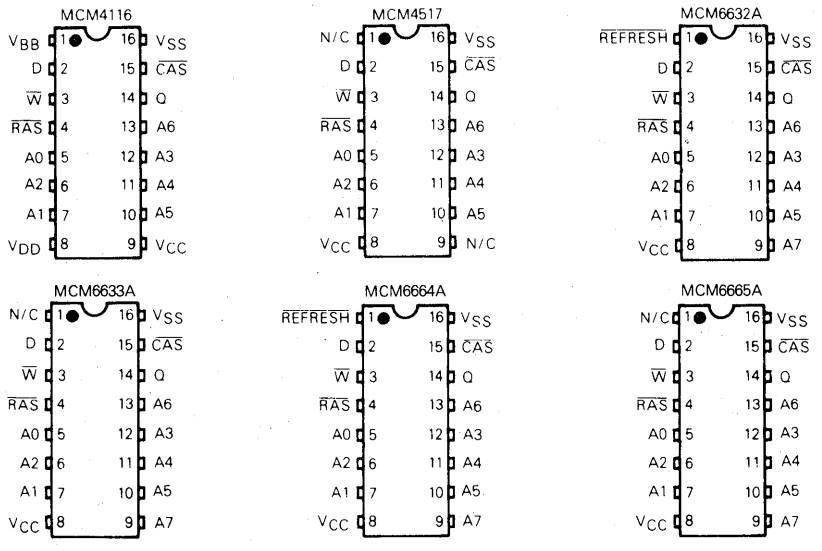
REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to

degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 2 ms. This is accomplished by sequentially cycling through the 128 row address locations every 2 ms, or at least one row every 15.6 microseconds. A normal read or write operation to the RAM will serve to refresh all the bits (256) associated with that particular row decoded.

$\overline{RAS}$ Only Refresh – When the memory component is in standby the $\overline{RAS}$ only refresh scheme is employed. This refresh method performs a $\overline{RAS}$ only cycle on all 128 row addresses every 2 ms. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and should be inactive or at a V_{IH} level to conserve power.

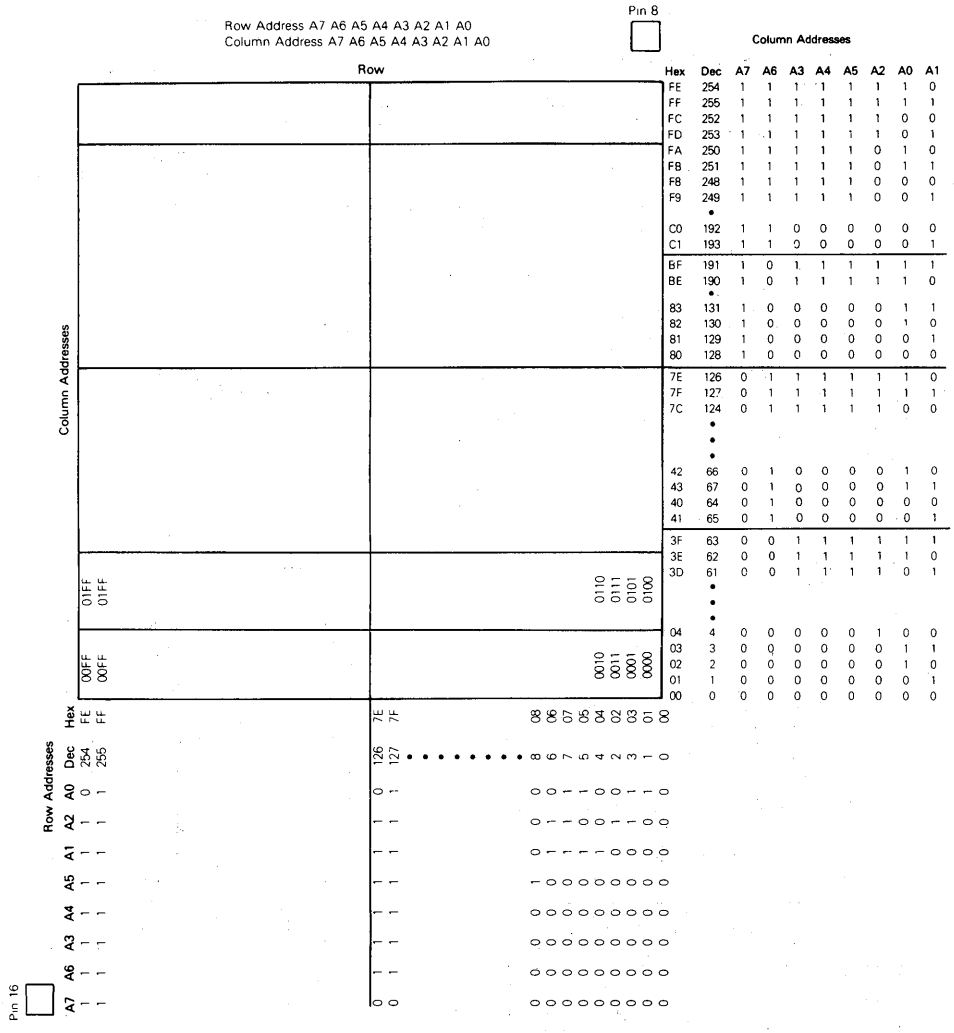
PIN ASSIGNMENT COMPARISON



PIN VARIATIONS

PIN NUMBER	MCM4116	MCM4517	MCM6632A	MCM6663A	MCM6664A	MCM6665A
1	V_{BB} (−5 V)	N/C	REFRESH	N/C	REFRESH	N/C
8	V_{DD} (+12 V)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
9	V_{CC} (+5 V)	N/C	A7	A7	A7	A7

MCM6665A BIT ADDRESS MAP



Data Stored = $D_{in} \oplus A_{0X} \oplus A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	True
0	1	Inverted
1	0	Inverted
1	1	True

MOTOROLA

MCM6665B

Advance Information

MOS
(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

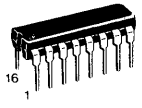
64K BIT DYNAMIC RAM

The MCM6665B is a 65,536-bit, high-speed, dynamic Random-Access Memory. It is organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, and is a yield-enhanced version of our popular MCM6665A, featuring a smaller die size and redundancy. As with any new mask set revision to a Dynamic RAM, it is recommended that the system performance be reevaluated using the new memory.

By multiplexing row- and column-address inputs, the MCM6665B requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

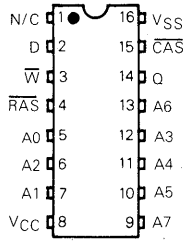
All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665B incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation (±10%)
- Maximum Access Time
  MCM6665BP15 = 150 ns
  MCM6665BP20 = 200 ns
- Low Power Dissipation
  302.5 mW Maximum (Active) (MCM6665B-15)
  22 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)
- Fast Page Mode Cycle Time



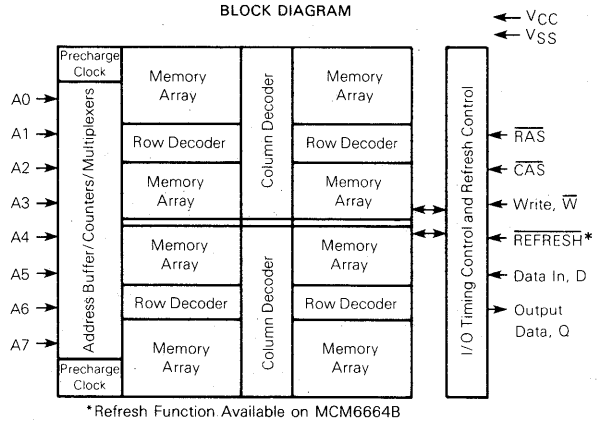
P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



PIN NAMES	
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



*Refresh Function Available on MCM6664B

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

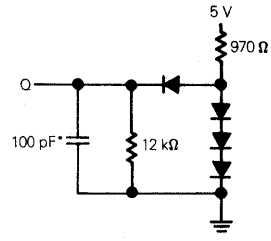
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (except V_{CC})	V_{in}, V_{out}	−2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	–	V_{CC}+1	V	1
Logic 0 Voltage, All Inputs	V_{IL}	−1.0*	–	0.8	V	1

*The device will withstand undershoots to the −2 volt level with a maximum pulse width of 20 ns at the −1.5 volt level. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (Standby)	I_{CC2}	–	4.0	mA	5
V_{CC} Power Supply Current 6665B-15, t_{RC} = 270 ns 6665B-20, t_{RC} = 330 ns	I_{CC1}	– –	55 50	mA	4
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles 6665B-15, t_{RC} = 270 ns 6665B-20, t_{RC} = 330 ns	I_{CC3}	– –	45 40	mA	4
V_{CC} Power Supply Current During Page Mode Cycle for t_{RAS} = 10 μsec 6665B-15, $t_{PC} = t_{RP}$ = 145 ns 6665B-20, $t_{PC} = t_{RP}$ = 200 ns	I_{CC4}	– –	40 35	mA	4
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{I(L)}$	–	10	μA	–
Output Leakage Current ($\overline{CAS}$ at logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{O(L)}$	–	10	μA	–
Output Logic 1 Voltage @ I_{out} = −4 mA	V_{OH}	2.4	–	V	–
Output Logic 0 Voltage @ I_{out} = 4 mA	V_{OL}	–	0.4	V	–

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A7), D	C_{I1}	3	5	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	6	8	pF	7
Output Capacitance (Q), ($\overline{CAS}$ = V_{IH} to disable output)	C_O	5	7	pF	7

NOTES:
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 μs is required after power-up followed by an 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the faster cycle rate with the output open.
5. $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta t}{\Delta V}$

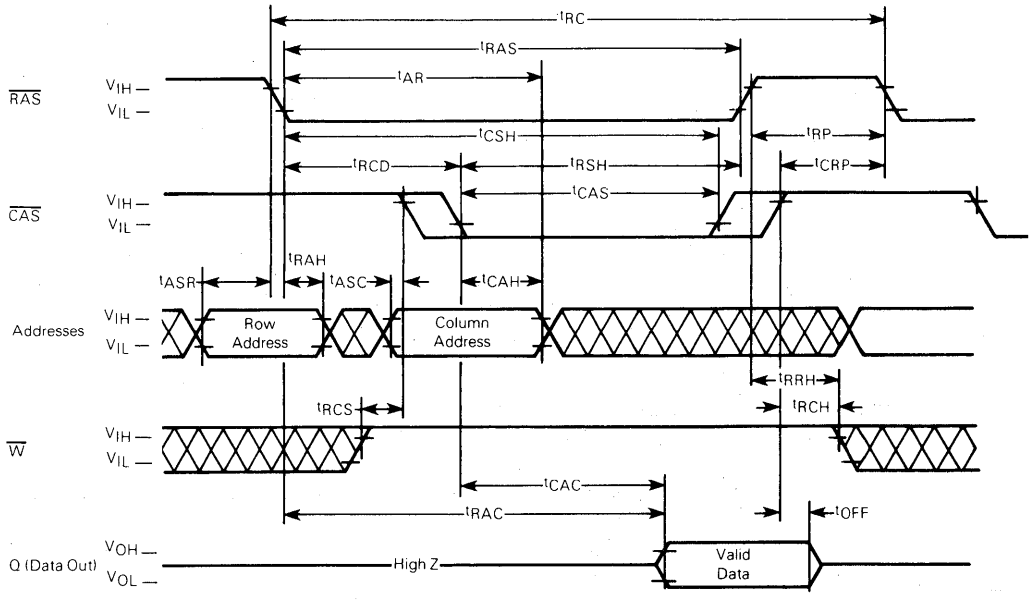
AC OPERATING CONDITIONS AND CHARACTERISTICS (Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted, See Notes 2, 3, 6, and Figure 1)

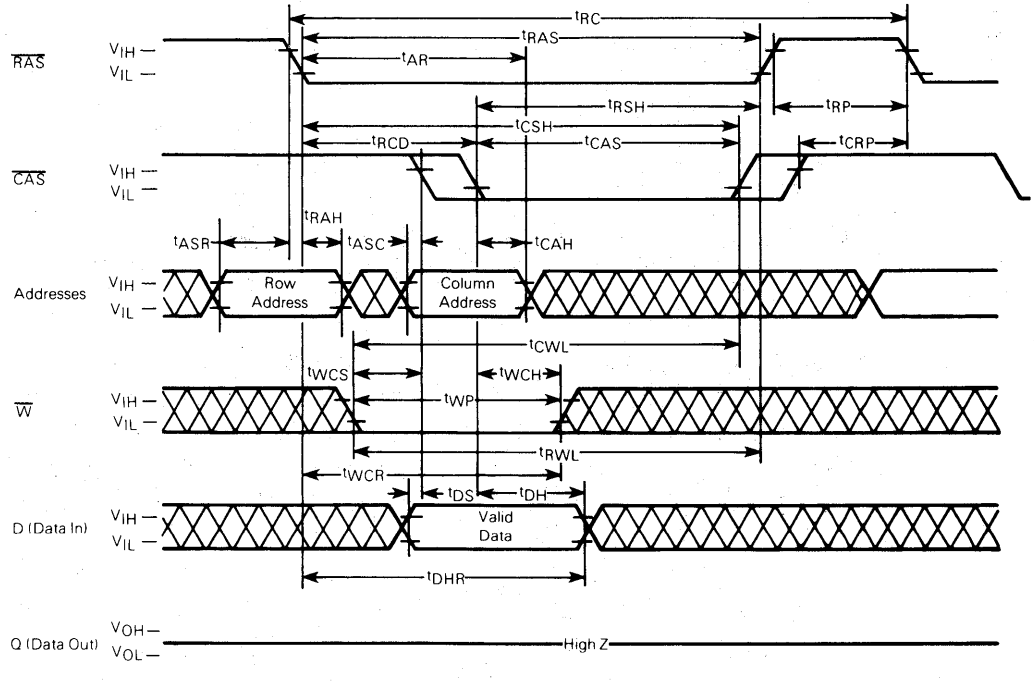
Parameter	Symbol	6665B-15		6665B-20		Units	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	270	–	330	–	ns	8, 9
Read Write Cycle Time	t_{RWC}	280	–	345	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	75	–	100	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	40	ns	18
Row Address Strobe Precharge Time	t_{RP}	100	–	120	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	150	10000	200	10000	ns	–
Column Address Strobe Pulse Width	t_{CAS}	75	10000	100	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	30	75	35	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	ns	–
Row Address Hold Time	t_{RAH}	20	–	25	–	ns	–
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	–
Column Address Hold Time	t_{CAH}	35	–	45	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	95	–	120	–	ns	17
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	6
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	–
Read Command Hold Time	t_{RCH}	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	14
Write Command Hold Time	t_{WCH}	35	–	45	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	95	–	120	–	ns	17
Write Command Pulse Width	t_{WP}	35	–	45	–	ns	–
Write Command to Row Strobe Lead Time	t_{RWL}	45	–	55	–	ns	–
Write Command to Column Strobe Lead Time	t_{CWL}	45	–	55	–	ns	–
Data in Setup Time	t_{DS}	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	35	–	45	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	95	–	120	–	ns	17
Column to Row Strobe Precharge Time	t_{CRP}	−10	–	−10	–	ns	–
$\overline{RAS}$ Hold Time	t_{RSH}	75	–	100	–	ns	–
Refresh Period	t_{RFSH}	–	2.0	–	2.0	ms	–
$\overline{WRITE}$ Command Setup Time	t_{WCS}	−10	–	−10	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	45	–	55	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	120	–	155	–	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	150	–	200	–	ns	–
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CP}	60	–	80	–	ns	–
Page Mode Cycle Time	t_{PC}	145	–	200	–	ns	–

8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
9. AC measurements $t_T = 5.0$ ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. t_{AR} min $\leq t_{AR} = t_{RCD} + t_{CAH}$
    t_{DHR} min $\leq t_{DHR} = t_{RCD} + t_{DH}$
    t_{WCR} min $\leq t_{WCR} = t_{RCD} + t_{WCH}$
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

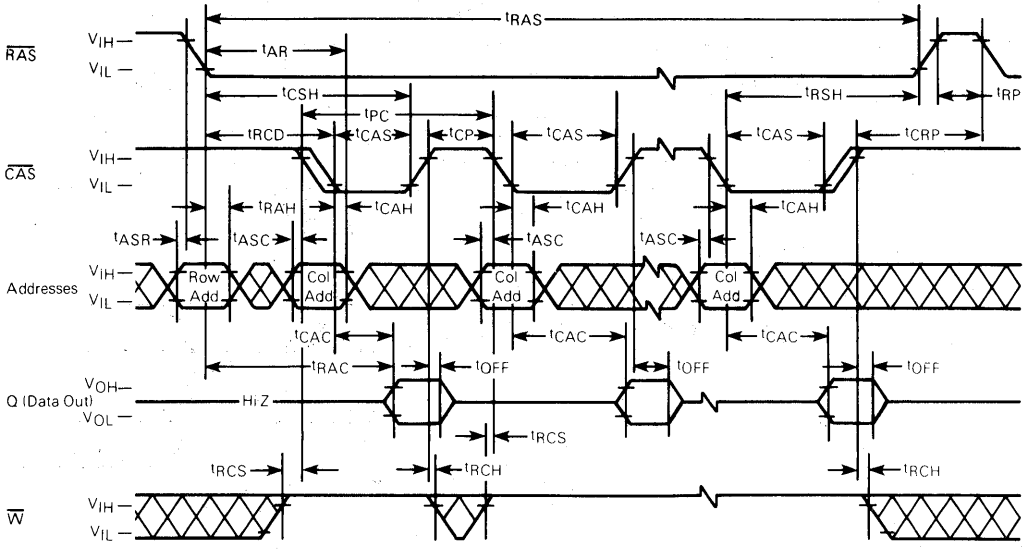
READ CYCLE TIMING



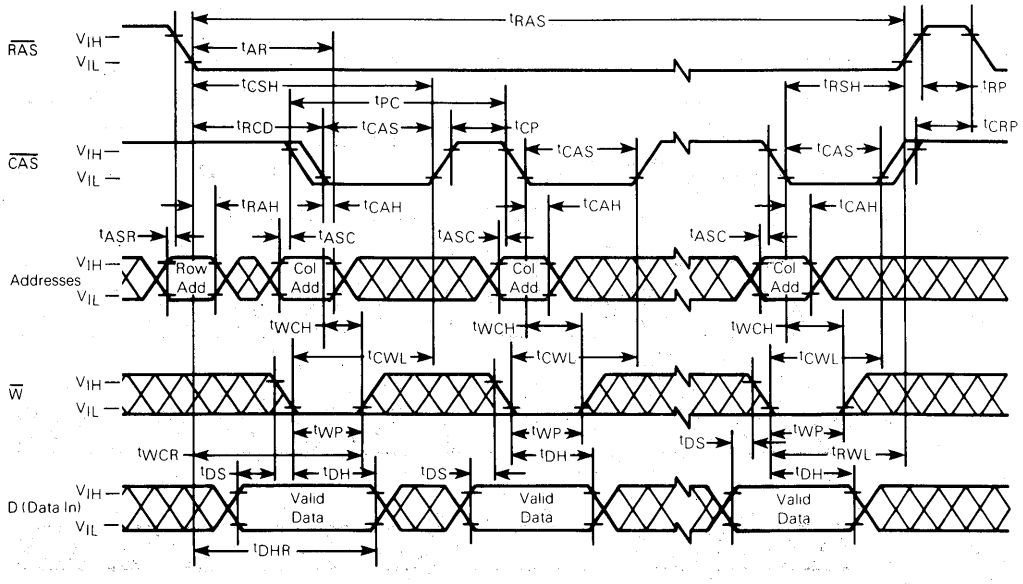
WRITE CYCLE TIMING



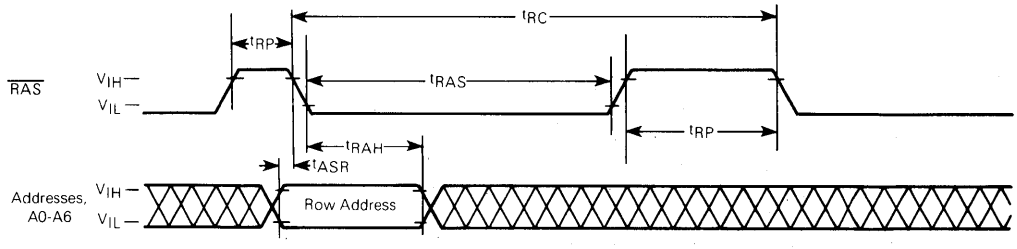
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



RAS-ONLY REFRESH CYCLE
(Data-in and Write are Don't Care, CAS is HIGH)



READ-WRITE/READ-MODIFY-WRITE CYCLE

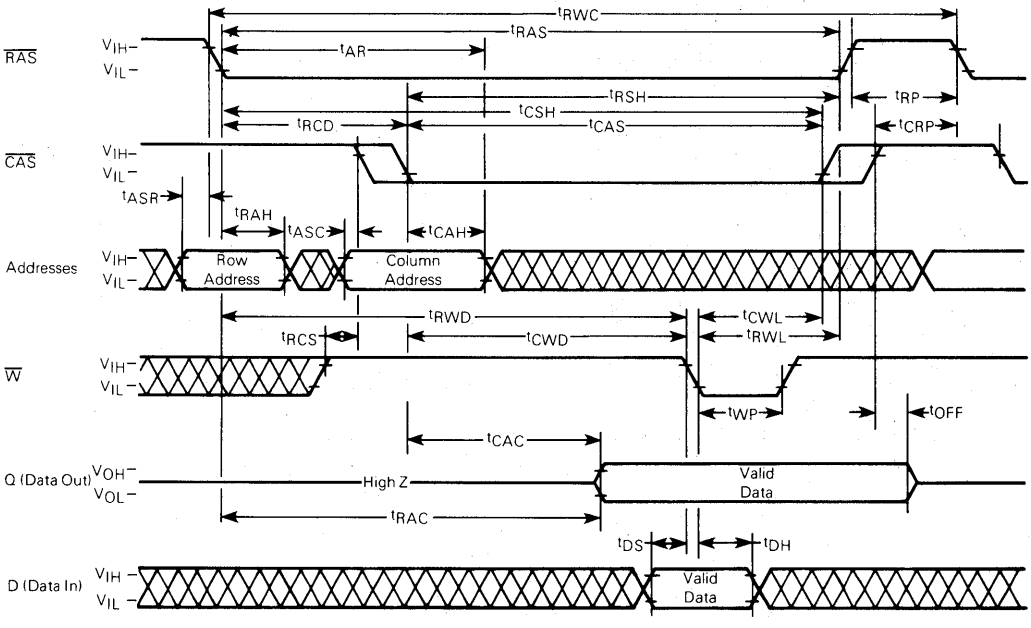
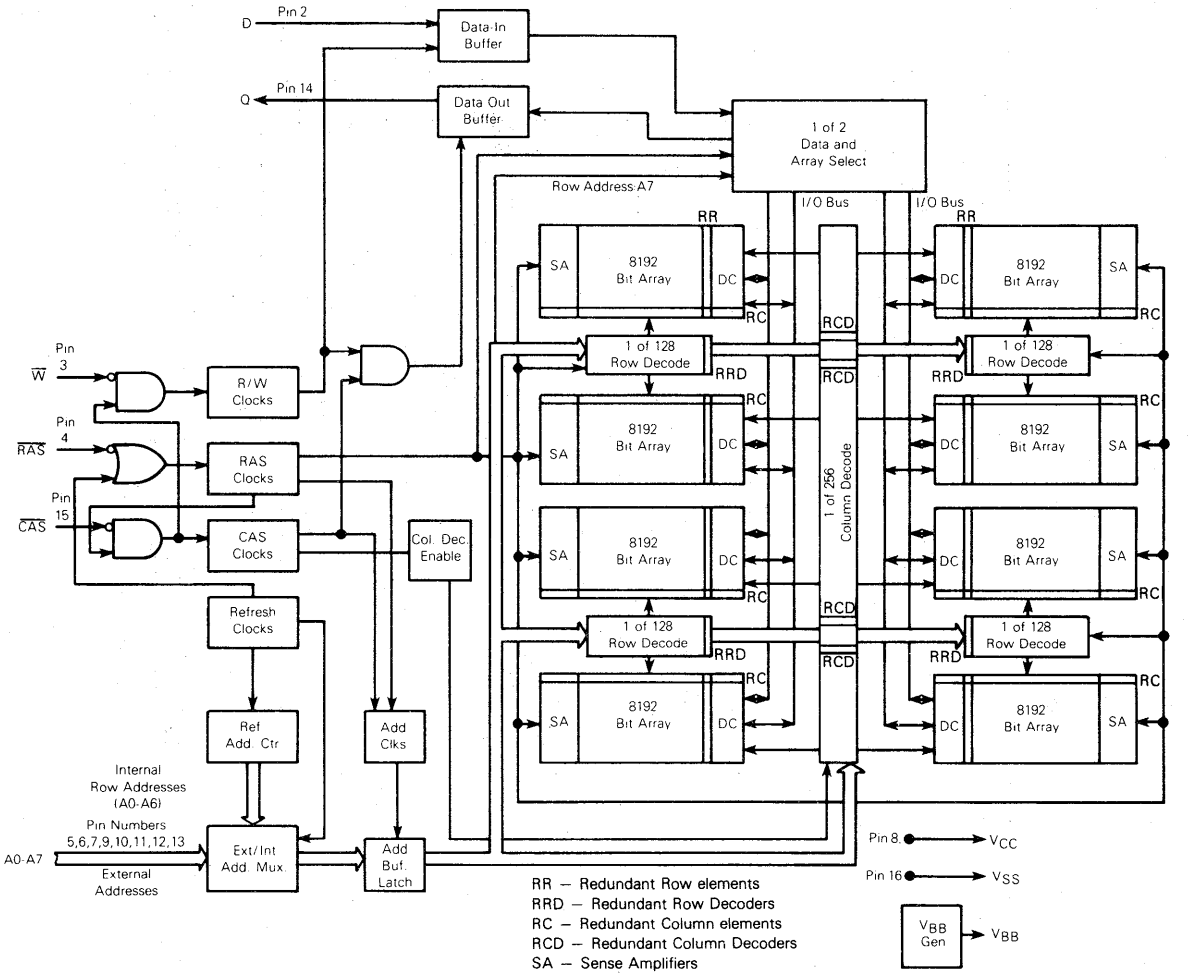


FIGURE 2 — FUNCTIONAL BLOCK DIAGRAM



DEVICE INITIALIZATION

Since the 64K dynamic RAM is a single supply 5 V only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up an initial pause of 100 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 2 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinguishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive-going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe and the column address strobe. A total of sixteen address bits will decode one of the 65,536 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 64K RAM: one is called the page mode cycle (described later) where an 8-bit column address field is presented on the input pins and latched by the $\overline{CAS}$ clock, and the other is the $\overline{RAS}$ only refresh cycle (described later) where a 7-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. In the latter case, the most significant bit on Row Address A7 (pin 9) is not required for refresh. See bit address map for the topology of the cells and their address selection.

NORMAL READ CYCLE

A read cycle is referred to as normal read cycle to differentiate if from a page-mode-read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available, as noted in the functional block diagram, Figure 2. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. The $\overline{CAS}$ clock can remain active for a maximum of 10 ns (t_{CRP}) into the next cycle. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as a early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisifed before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds – [t_{RWL} + t_{RP} + 2T_t].

At the start of a write cycle, the data out is in a three-state condition and remains inactive throughout the cycle. The data out remains three-state because the active transition.

of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers as noted in Functional Block Diagram. The three-state condition (high impedance) of the Data Out Pin during a write cycle can be effectively utilized in a system that has a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYLES

As the name implies, both a read and a write cycle is accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, the following parameters (t_{RWD}, t_{CWD}) play an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{RWD} and t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows faster successive data operations at the 256 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 64K dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 8-bit column address field. There are two controlling factors that limit the access to all 256 column locations in one $\overline{RAS}$ clock active operation. These are the refresh interval of the device (2 ms/128 = 15.6 microseconds) and the maximum active time specification for the $\overline{RAS}$ clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the $\overline{RAS}$ clock on time is the limiting factor of the number of sequential page accesses possible. Ten microseconds will provide approximately (10 microseconds/page mode cycle time) 50 successive page accesses for every row address selected before the $\overline{RAS}$ clock is reset.

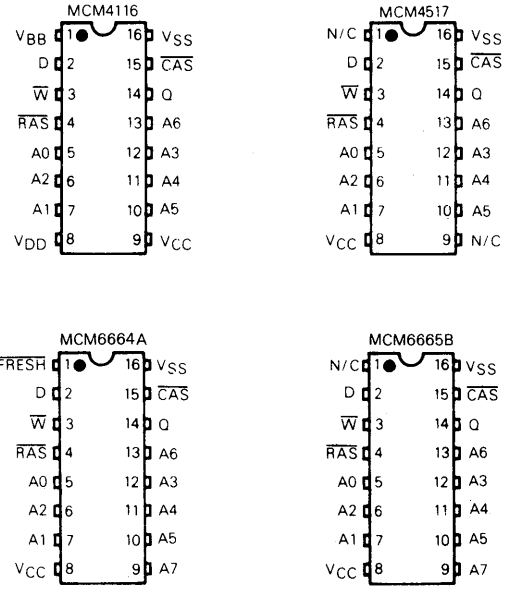
The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. The page mode cycles illustrated show a series of sequential reads separated by a series of sequential writes. This is just one mode of operation. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 2 ms. This is accomplished by sequentially cycling through the 128 row address locations every 2 ms, or at least one row every 15.6 microseconds. A normal read or write operation to the RAM will serve to refresh all the bits (256) associated with that particular row decoded.

$\overline{RAS}$ Only Refresh – When the memory component is in standby the $\overline{RAS}$ only refresh scheme is employed. This refresh method performs a $\overline{RAS}$ only cycle on all 128 row addresses every 2 ms. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and should be inactive or at a V_{IH} level to conserve power.

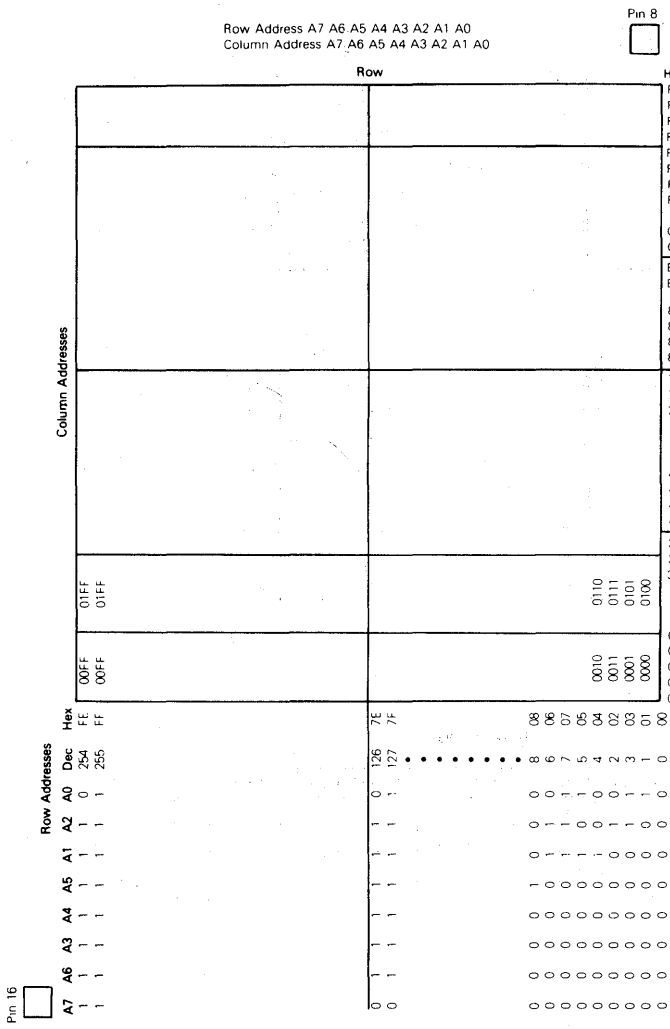
PIN ASSIGNMENT COMPARISON



PIN VARIATIONS

PIN NUMBER	MCM4116	MCM4517	MCM6664A	MCM6665B
1	V_{BB} (−5 V)	N/C	REFRESH	N/C
8	V_{DD} (+12 V)	V_{CC}	V_{CC}	V_{CC}
9	V_{CC} (+5 V)	N/C	A7	A7

MCM6665B BIT ADDRESS MAP



Hex	Dec	A7	A6	A3	A4	A5	A2	A0	A1
FE	254	1	1	1	1	1	1	1	0
FF	255	1	1	1	1	1	1	1	1
FC	252	1	1	1	1	1	1	0	0
FD	253	1	1	1	1	1	1	0	1
FA	250	1	1	1	1	1	0	1	0
FB	251	1	1	1	1	1	0	1	1
F8	248	1	1	1	1	1	0	0	0
F9	249	1	1	1	1	1	0	0	1
	•								
C0	192	1	1	0	0	0	0	0	0
C1	193	1	1	0	0	0	0	0	1
BF	191	1	0	1	1	1	1	1	1
BE	190	1	0	1	1	1	1	1	0
	•								
83	131	1	0	0	0	0	0	1	1
82	130	1	0	0	0	0	0	1	0
81	129	1	0	0	0	0	0	0	1
80	128	1	0	0	0	0	0	0	0
7E	126	0	1	1	1	1	1	1	0
7F	127	0	1	1	1	1	1	1	1
7C	124	0	1	1	1	1	1	0	0
	•								
	•								
	•								
42	66	0	1	0	0	0	0	1	0
43	67	0	1	0	0	0	0	1	1
40	64	0	1	0	0	0	0	0	0
41	65	0	1	0	0	0	0	0	1
3F	63	0	0	1	1	1	1	1	1
3E	62	0	0	1	1	1	1	1	0
3D	61	0	0	1	1	1	1	0	1
	•								
	•								
	•								
04	4	0	0	0	0	0	0	1	0
03	3	0	0	0	0	0	0	1	1
02	2	0	0	0	0	0	0	1	0
01	1	0	0	0	0	0	0	0	1
00	0	0	0	0	0	0	0	0	0

Data Stored = $D_{in} \oplus A_{0X} \oplus A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	True
0	1	Inverted
1	0	Inverted
1	1	True

MOTOROLA

MCM6665C

Product Preview

64K BIT DYNAMIC RAM

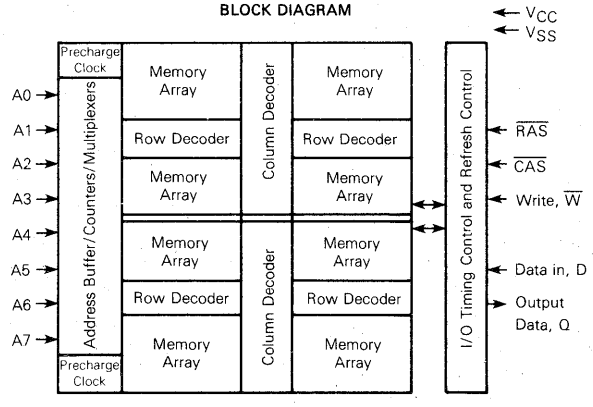
The MCM6665C is a 65,536-bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, this new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6665C requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$, allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665C incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation (±10%)
- Full Power Supply Range Capabilities
- Maximum Access Time
  - MCM6665C-12 = 120 ns
  - MCM6665C-15 = 150 ns
  - MCM6665C-20 = 200 ns
- Low Power Dissipation
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- Hidden Refresh Available
- $\overline{CAS}$ Controlled Ouput
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)
- Fast Page Mode Cycle Time
- Laser Redundancy

BLOCK DIAGRAM



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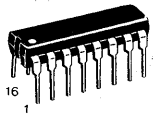
MOS

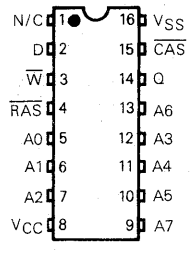
(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



PIN NAMES	
A0-A7	Address Input
D	Data In
Q	Data Out
W	Read/Write Input
RAS	Row Address Strobe
CAS	Column Address Strobe
VCC	Power (+ 5 V)
VSS	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltages to this high-impedance circuit.

DRAM

MOTOROLA

MCM6256

Product Preview

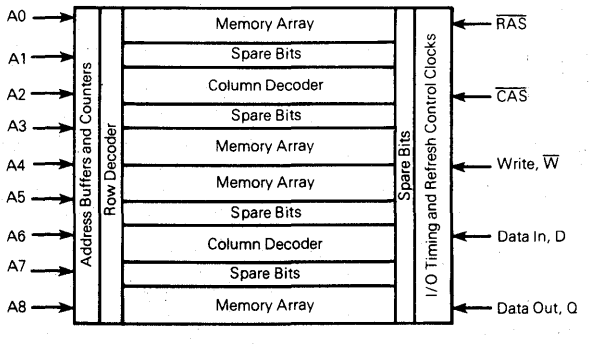
256K-BIT DYNAMIC RAM

The MCM6256 is a 262,144 bit, high-speed, dynamic Random Access Memory. Organized as 262,144 one-bit words and fabricated using Motorola's High-performance silicon-gate MOS (HMOS) technology, this new single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability. The MCM6256 has the capability of using redundancy and is manufactured using advanced direct-step on wafer photolithographic equipment.

By multiplexing row and column address inputs, the MCM6256 requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by $\overline{CAS}$ allowing greater system flexibility.

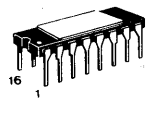
All inputs and outputs, including clocks, are fully TTL compatible. The MCM6256 incorporates a one transistor cell design and dynamic storage techniques. In addition to the $\overline{RAS}$-only refresh mode, a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh is available. The MCM6256 has an extended "page mode" feature which allows column accesses of up to 512 bits within the selected row.

- Organized as 262,144 Words of 1 Bit
- Single +5 Volt Operation (±10%)
- Maximum Access Time:
  MCM6256-10 = 100 ns
  MCM6256-12 = 120 ns
  MCM6256-15 = 150 ns
- Low Power Dissipation:
  70 mA maximum (Active) MCM6256-10
  4.5 mA maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{RAS}$-Only Refresh Mode
- Automatic ($\overline{CAS}$ before $\overline{RAS}$) Refresh Mode
- Extended Page Mode Capability
  50 ns Page Access Time — MCM6256-10
  100 ns Page Cycle Time — MCM6256-10

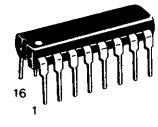


MOS
(N-CHANNEL, SILICON-GATE)

262,144 BIT DYNAMIC RANDOM ACCESS MEMORY

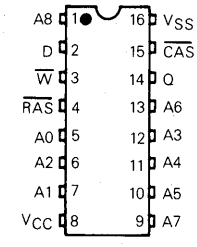


L SUFFIX
CERAMIC PACKAGE
CASE 690



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



PIN NAMES	
A0-A8	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MOTOROLA

MCM6257

Product Preview

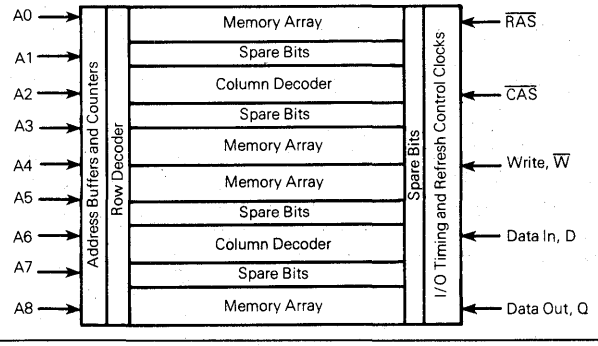
256K-BIT DYNAMIC RAM

The MCM6257 is a 262,144 bit, high-speed, dynamic Random Access Memory. Organized as 262,144 one-bit words and fabricated using Motorola's High-performance silicon-gate MOS (HMOS) technology, this new single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability. The MCM6257 has the capability of using redundancy and is manufactured using advanced direct-step on wafer photolithographic equipment.

By multiplexing row and column address inputs, the MCM6257 requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by $\overline{CAS}$ allowing greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6257 incorporates a one transistor cell design and dynamic storage techniques. In addition to the $\overline{RAS}$-only refresh mode, a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh is available. Another special feature of the MCM6257 is nibble mode, allowing the user to serially access up to 4 bits of data at a high data rate. Nibble mode addressing is controlled by the addresses on pin 1 (A8 row and A8 column).

- Organized as 262,144 Words of 1 Bit
- Single +5 Volt Operation (±10%)
- Maximum Access Time:
  MCM6257-10 = 100 ns
  MCM6257-12 = 120 ns
  MCM6257-15 = 150 ns
- Low Power Dissipation:
  70 mA maximum (Active) MCM6257-10
  4.5 mA maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{RAS}$-Only Refresh Mode
- Automatic ($\overline{CAS}$ before $\overline{RAS}$) Refresh Mode
- Fast Nibble Mode on Read and Write Cycles
  20 ns Access Time
  50 ns Cycle Time



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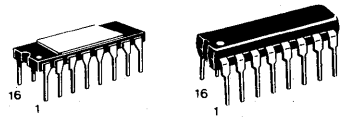
MOS
(N-CHANNEL, SILICON-GATE)

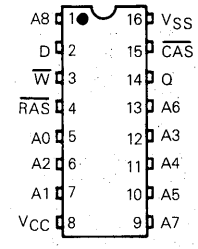
262,144 BIT DYNAMIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 690

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



PIN NAMES	
A0-A8	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

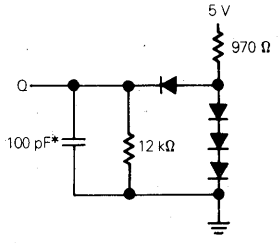
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{CC}, V_{in}, V_{out}	−1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature (Ceramic)	T_{stg1}	−65 to +150	°C
Storage Temperature (Plastic)	T_{stg2}	−55 to +125	°C
Power Dissipation	P_D	1.0	W
Data Out Current (Short Circuit)	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	MCM6257-10, -12, -15	V_{CC}	4.5	5.0	5.5	V	1
		V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs		V_{IH}	2.4	–	V_{CC}+1	V	1
Logic 0 Voltage, All Inputs		V_{IL}	−1.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current					
MCM6257-10, t_{RC} = 200 ns		–	70		
MCM6257-12, t_{RC} = 230 ns	I_{CC1}	–	65	mA	4
MCM6257-15, t_{RC} = 260 ns		–	57		
V_{CC} Power Supply Current (Output Not Loaded)					
Standby	I_{CC2}	–	4.5	mA	5
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles					
MCM6257-10, t_{RC} = 200 ns		–	60		
MCM6257-12, t_{RC} = 230 ns	I_{CC3}	–	55	mA	4
MCM6257-15, t_{RC} = 260 ns		–	50		
V_{CC} Power Supply Current During Automatic ($\overline{CAS}$ Before $\overline{RAS}$) Refresh					
MCM6257-10, t_{RC} = 200 ns		–	65		
MCM6257-12, t_{RC} = 230 ns	I_{CC4}	–	60	mA	4
MCM6257-15, t_{RC} = 260 ns		–	55		
V_{CC} Power Supply Current During Nibble Mode					
MCM6257-10, t_{NC} = 50 ns		–	25		
MCM6257-12, t_{NC} = 65 ns	I_{CC5}	–	23	mA	4
MCM6257-15, t_{NC} = 80 ns		–	20		
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$) (Any Input)	$I_{I(L)}$	–	10	μA	–
Output Leakage Current ($\overline{CAS}$ at logic 1, $0 \le V_{out} \le 5.5$)	$I_{O(L)}$	–	10	μA	–
Output Logic 1 Voltage @ I_{out} = −5 mA	V_{OH}	2.4	–	V	–
Output Logic 0 Voltage @ I_{out} = 4.2 mA	V_{OL}	–	0.4	V	–

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A8), D	C_{I1}	–	7	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	–	10	pF	7
Output Capacitance (Q), ($\overline{CAS}$ = V_{IH} to disable output)	C_O	–	7	pF	7

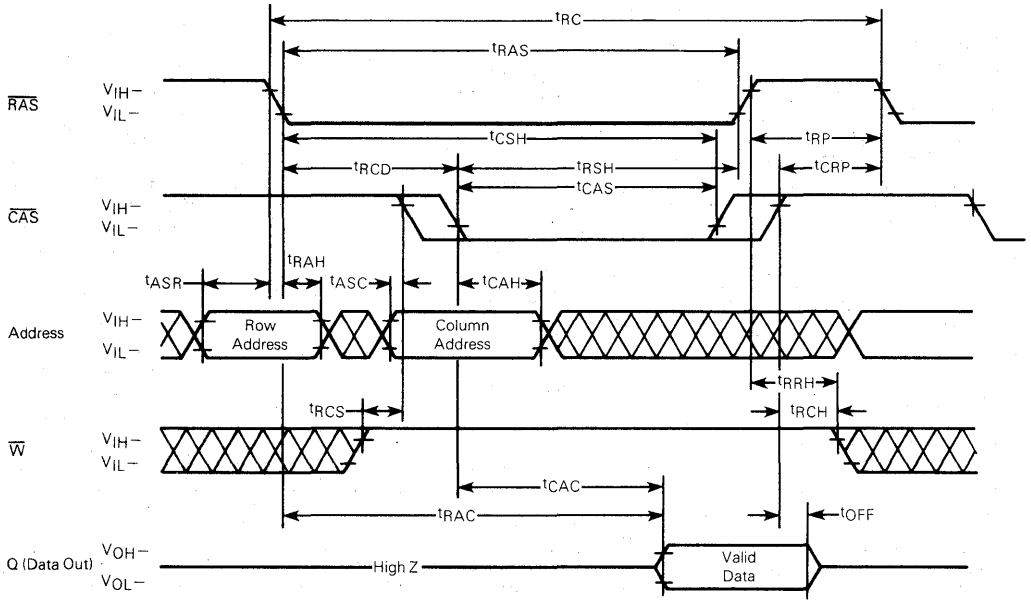
AC OPERATING CONDITIONS AND CHARACTERISTICS (Read Cycles)
(Full operating voltage and temperature range unless otherwise noted. See Notes 2, 3, 6, and Figure 1)

READ CYCLE

Parameter	Symbol		MCM6257-10		MCM6257-12		MCM6257-15		Units	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	210	–	230	–	260	–	ns	8, 9
Access Time from Row Address Strobe	t_{RELQV}	t_{RAC}	–	100	–	120	–	150	ns	10, 12
Access Time from Column Address Strobe	t_{CELQV}	t_{CAC}	–	50	–	60	–	75	ns	11, 12
Row Address Strobe Pulse Width	t_{RELREH}	t_{RAS}	110	10000	120	10000	150	10000	ns	–
Column Address Strobe Pulse Width	t_{CELCEH}	t_{CAS}	60	10000	60	10000	75	10000	ns	–
Refresh Period	t_{RVRV}	t_{RFSH}	–	4	–	4	–	4	ms	–
Row Address Strobe Precharge Time	t_{REHREL}	t_{RP}	90	–	100	–	100	–	ns	–
Column to Row Strobe Precharge Time	t_{CEHREL}	t_{CRP}	15	–	20	–	20	–	ns	–
Row to Column Strobe Lead Time	t_{RELCEL}	t_{RCD}	20	50	22	60	25	75	ns	13
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	60	–	60	–	75	–	ns	–
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	100	–	120	–	150	–	ns	–
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	12	–	15	–	ns	–
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	–
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	20	–	25	–	ns	–
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	2
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	–
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	20	–	20	–	20	–	ns	14
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	25	0	30	0	30	ns	17

NOTES:
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation guaranteed. To ensure proper initialization of the internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta t}{\Delta V}$
8. The specifications for t_{RC} (min), t_{RWC} (min), and nibble cycle time (t_{NC}) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
9. AC measurements are made with $t_T = 5.0$ ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
11. Assumes that $t_{RCD} > t_{RCD}$ (max).
12. Measured with a current load equivalent to 2 TTL (–200 μA, +4 mA) loads and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V).
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

READ CYCLE TIMING



AC OPERATING CONDITIONS AND CHARACTERISTICS (Write and Read-Modify-Write Cycles)
(Full operating voltage and temperature range unless otherwise noted. See Notes 2, 3, 6, and Figure 1)

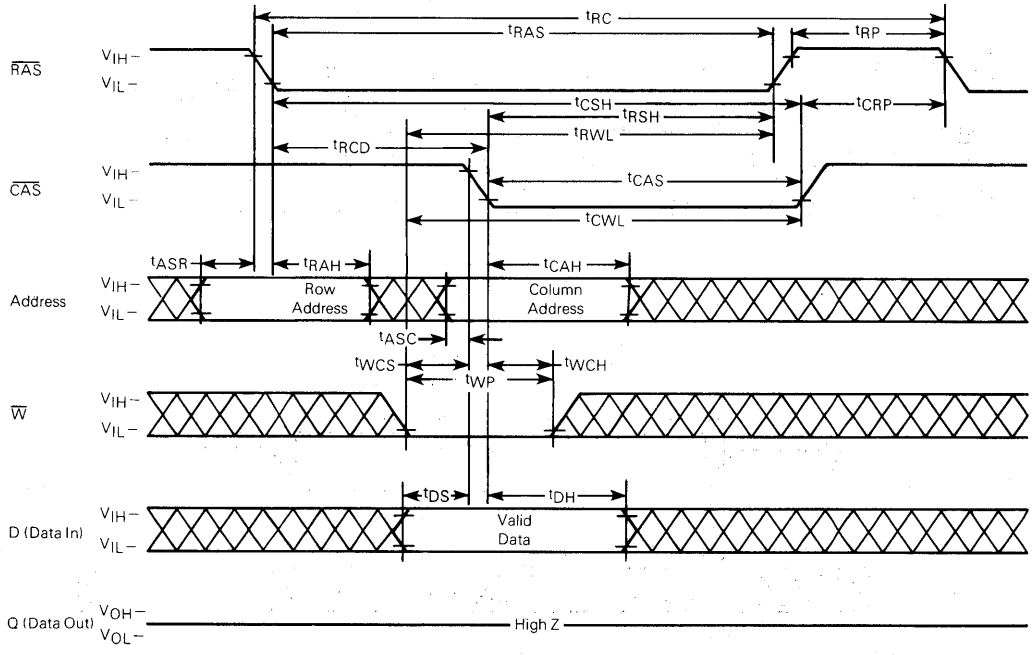
WRITE CYCLE

Parameter	Symbol		MCM6257-10		MCM6257-12		MCM6257-15		Units	Note
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	16
Write Command Hold Time	t_{CELWH}	t_{WCH}	15	–	20	–	25	–	ns	–
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	20	–	25	–	ns	–
Write Command to Row Strobe Lead Time	t_{WLREH}	t_{RWL}	40	–	50	–	60	–	ns	–
Write Command to Column Strobe Lead Time	t_{WLCEH}	t_{CWL}	20	–	30	–	40	–	ns	–
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{CELDX}	t_{DH}	15	–	20	–	25	–	ns	15

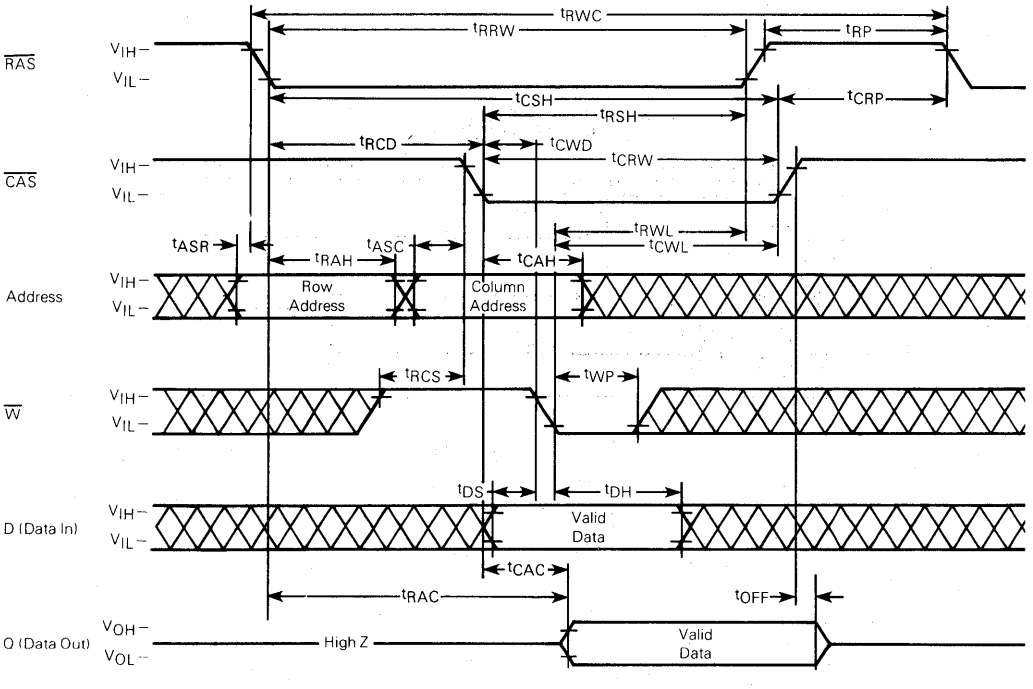
READ-MODIFY-WRITE CYCLE

Parameter	Symbol		MCM6257-10		MCM6257-12		MCM6257-15		Unit	Note
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RWC}	210	–	230	–	260	–	ns	8, 9
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CELWL}	t_{CWD}	15	–	20	–	25	–	ns	16
RMW Cycle $\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RRW}	110	10000	120	10000	150	10000	ns	–
RMW Cycle $\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CRW}	60	10000	60	10000	75	10000	ns	–

EARLY WRITE CYCLE



READ-MODIFY-WRITE OR LATE WRITE CYCLE

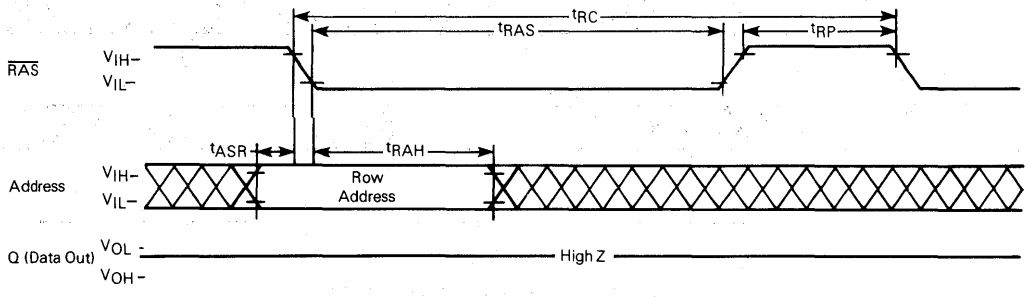


AC OPERATING CONDITIONS AND CHARACTERISTICS (Refresh Cycles)
(Full Operating Voltage and Temperature Range Unless Otherwise Noted.)

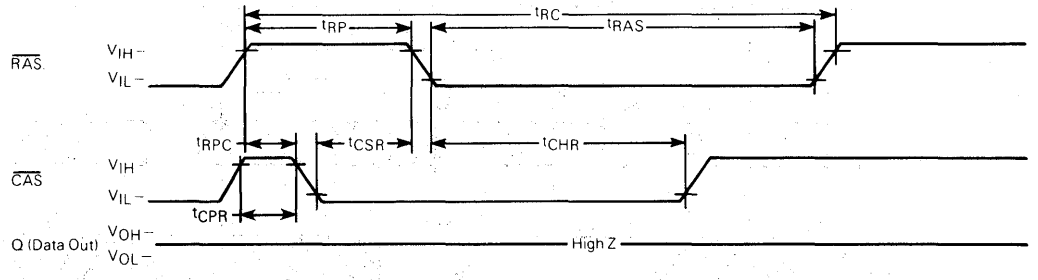
REFRESH CYCLE

Parameter	Symbol		MCM6257-10		MCM6257-12		MCM6257-15		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Column Address Strobe Setup Time for Auto Refresh	t_{CELREL}	t_{CSR}	20	–	25	–	30	–	ns
Column Address Strobe Hold Time for Auto Refresh	t_{RELCEH}	t_{CHR}	20	–	25	–	30	–	ns
Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	20	–	20	–	20	–	ns
$\overline{CAS}$ Precharge Time Before Automatic Refresh Cycle	t_{CEHCEL}	t_{CPR}	20	–	25	–	30	–	ns

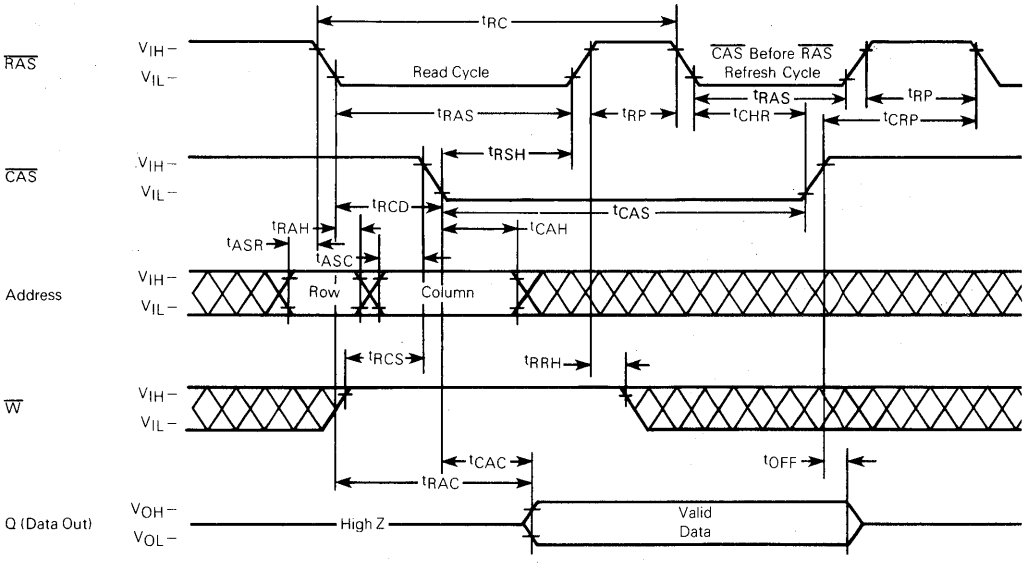
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{CAS}$ = V_{IH}, D and $\overline{W}$ are Don't Care)



AUTOMATIC ($\overline{CAS}$ BEFORE $\overline{RAS}$) REFRESH CYCLE
(D and $\overline{W}$ are Don't Care)



HIDDEN REFRESH CYCLE

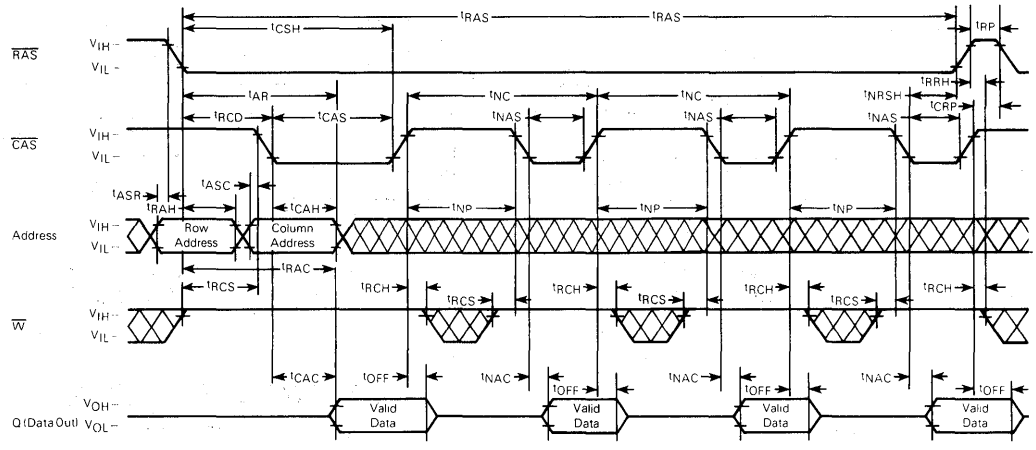


AC OPERATING CONDITIONS AND CHARACTERISTICS (Nibble Mode Cycle)
(Full Operating Voltage and Temperature Range Unless Otherwise Noted.)

NIBBLE MODE CYCLE

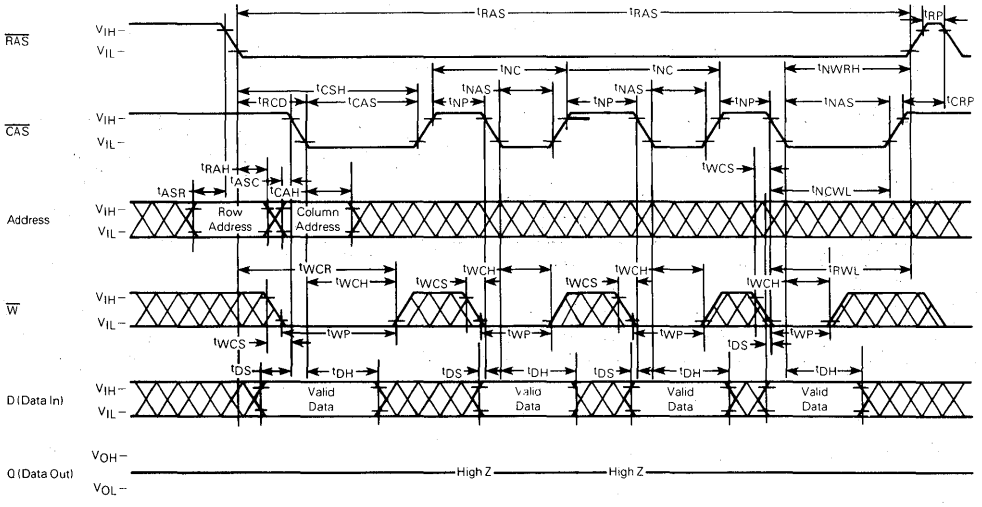
Parameter	Symbol		MCM6257-10		MCM6257-12		MCM6257-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Nibble Mode Cycle Time	t_{CELCEL}	t_{NC}	50	–	65	–	80	–	ns	8, 9
Nibble Mode Access Time	t_{CELQV}	t_{NAC}	–	20	–	30	–	40	ns	12
Nibble Mode Setup Time ($\overline{CAS}$ Pulse Width)	t_{CELCEH}	t_{NAS}	20	–	30	–	40	–	ns	–
Nibble Mode Precharge Time	t_{CEHCEL}	t_{NP}	20	–	25	–	30	–	ns	–
Nibble Mode $\overline{RAS}$ Hold Time	t_{CELREH}	t_{NRSH}	20	–	30	–	40	–	ns	–
Nibble Mode $\overline{CAS}$ Hold Time	t_{REHCEX}	t_{NCSH}	20	–	20	–	20	–	ns	–
Nibble Mode $\overline{WRITE}$ to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{NCWL}	20	–	30	–	40	–	ns	–
Nibble Mode Write $\overline{RAS}$ Hold Time	t_{CELREH}	t_{NWRH}	40	–	50	–	60	–	ns	–

NIBBLE MODE READ CYCLE*

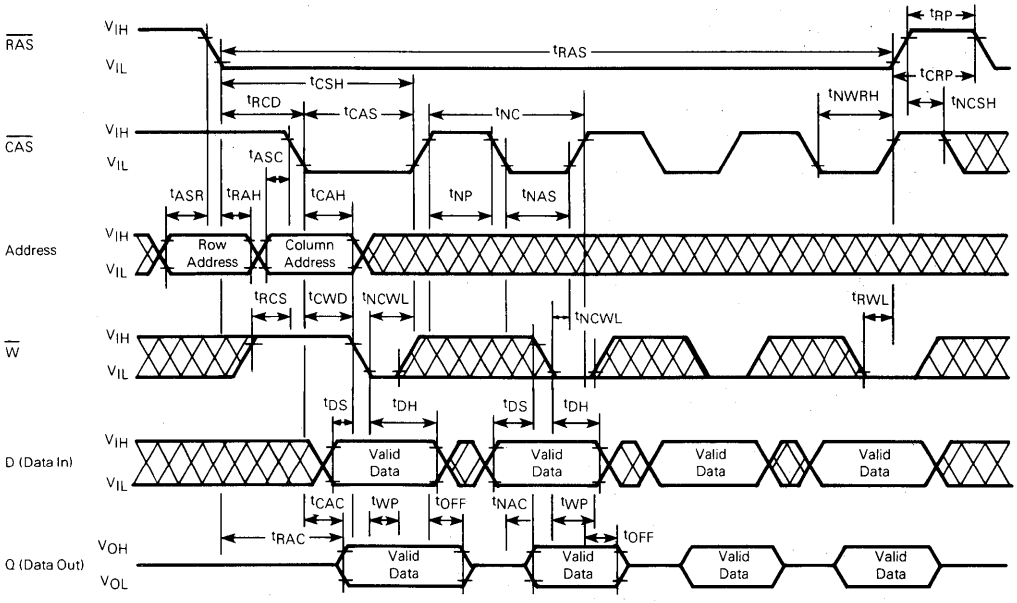


*Pin 1 at Row Time and Column Time Determine the Starting Address of the Nibble Cycle

NIBBLE MODE WRITE CYCLE (EARLY WRITE)



NIBBLE MODE READ-MODIFY-WRITE CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinguishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 256K RAM, one is called the $\overline{RAS}$ only refresh cycle (described later) where an 8-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A8 (pin 1) is not required for refresh. The other variation, which is called nibble mode, allows the user to address up to 4 bits of data (serially) at a very high data rate. (See **NIBBLE MODE CYCLES** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a nibble mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as a early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds – $[t_{RWL} + t_{RP} + 2T_t]$.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle is accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, t_{CWD} plays an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 ms. This is accomplished by sequentially cycling through the 256 row address locations every 4 ms, (i.e, at least one row every 15.6 microseconds like the 64K dynamic RAM). A normal read or write operation to the RAM will serve to refresh all the bits (1024) associated with that particular row decoded.

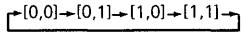
$\overline{RAS}$-Only Refresh – One method to ensure data retention is to employ the $\overline{RAS}$-only refresh scheme. In this refresh method, the system must perform a $\overline{RAS}$-only cycle or all 256 row addresses every 4 ms. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

AUTOMATIC ($\overline{CAS}$ BEFORE $\overline{RAS}$) REFRESH

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedence state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

NIBBLE MODE CYCLES

Nibble Mode Operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at a high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycle. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).

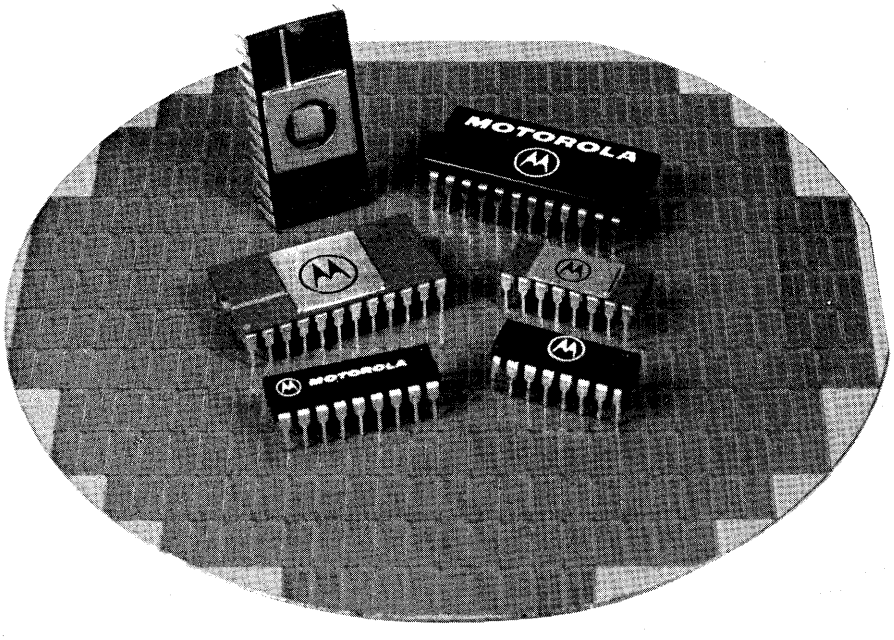


Pin one (A8) determines the starting point of the circular 4-bit nibble. Row A8 and Column A8 provide the two binary bits needed to select one of four bits. The user can start the nibble mode at any one of the four bits, from then on, successive bits come out in a binary fashion; 00→01→10→11 with Row A8 being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

MOS Static RAMs

SRAM



MOTOROLA

MCM6810

128 × 8-BIT STATIC RANDOM ACCESS MEMORY

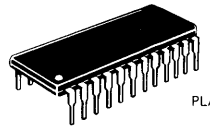
The MCM6810 is a byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing random storage in byte increments. Memory expansion is provided through multiple Chip Select inputs.

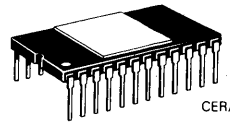
- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bidirectional Three-State Data Input/Output
- Six Chip Select Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 450 ns — MCM6810
  360 ns — MCM68A10
  250 ns — MCM68B10

MOS
(N-CHANNEL, SILICON-GATE)

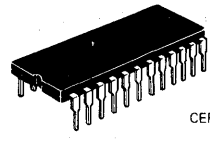
128 × 8-BIT STATIC RANDOM ACCESS MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 709



L SUFFIX
CERAMIC PACKAGE
CASE 716



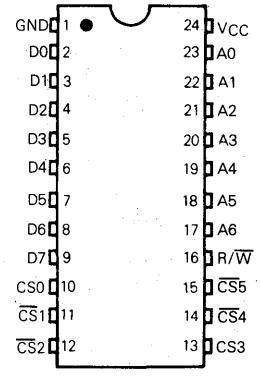
S SUFFIX
CERDIP PACKAGE
CASE 623

SRAM

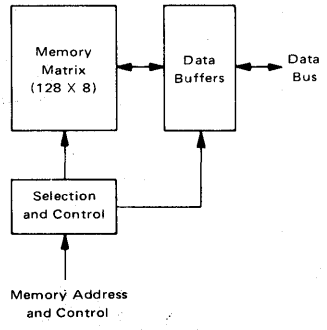
ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
Ceramic L Suffix	1.0	0°C to 70°C	MCM6810L
	1.0	−40°C to 85°C	MCM6810CL
	1.5	0°C to 70°C	MCM68A10L
	1.5	−40°C to 85°C	MCM68A10CL
	2.0	0°C to 70°C	MCM68B10L
Plastic P Suffix	1.0	0°C to 70°C	MCM6810P
	1.0	−40°C to 85°C	MCM6810CP
	1.5	0°C to 70°C	MCM68A10P
	1.5	−40°C to 85°C	MCM68A10CP
	2.0	0°C to 70°C	MCM68B10P
Cerdip S Suffix	1.0	0°C to 70°C	MCM6810S
	1.0	−40°C to 85°C	MCM6810CS
	1.5	0°C to 70°C	MCM68A10S
	1.5	−40°C to 85°C	MCM68A10CS
	2.0	0°C to 70°C	MCM68B10S

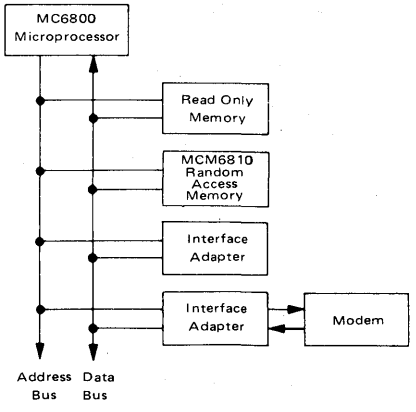
PIN ASSIGNMENT



MCM6810 RANDOM ACCESS MEMORY
BLOCK DIAGRAM



M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MCM6810, MCM68A10, MCM68B10 MCM6810C, MCM68A10C	T_A	T_L to T_H 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance Ceramic Plastic Cerdip	θ_{JA}	 60 120 65	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{PORT} \equiv$ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

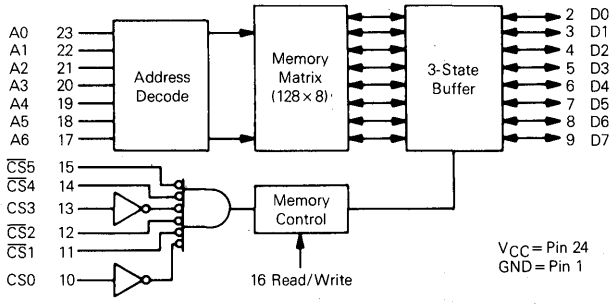
$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

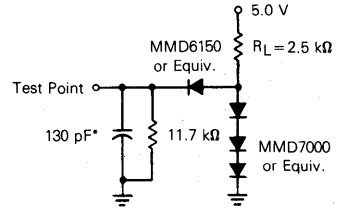
BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	$V_{SS}+2.0$	V_{CC}	V
Input Low Voltage	V_{IL}	$V_{SS}-0.3$	$V_{SS}+0.8$	V
Input Current (A_n, R/$\overline{W}$, $\overline{CS}_n$) (V_{in} = 0 to 5.25 V)	I_{in}	–	2.5	μA
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	V
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	V
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	ITSI	–	10	μA
Supply Current (1.0 MHz)	I_{CC}	–	80	mA
(V_{CC} = 5.25 V, All Other Pins Grounded) (1.5, 2.0 MHz)		–	100	
Input Capacitance (A_n, R/$\overline{W}$, CS_n, $\overline{CS}_n$) (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}	–	7.5	pF
Output Capacitance (D_n) (V_{out} = 0, T_A = 25°C, f = 1.0 MHz, CSO = 0)	C_{out}	–	12.5	pF

AC TEST LOAD



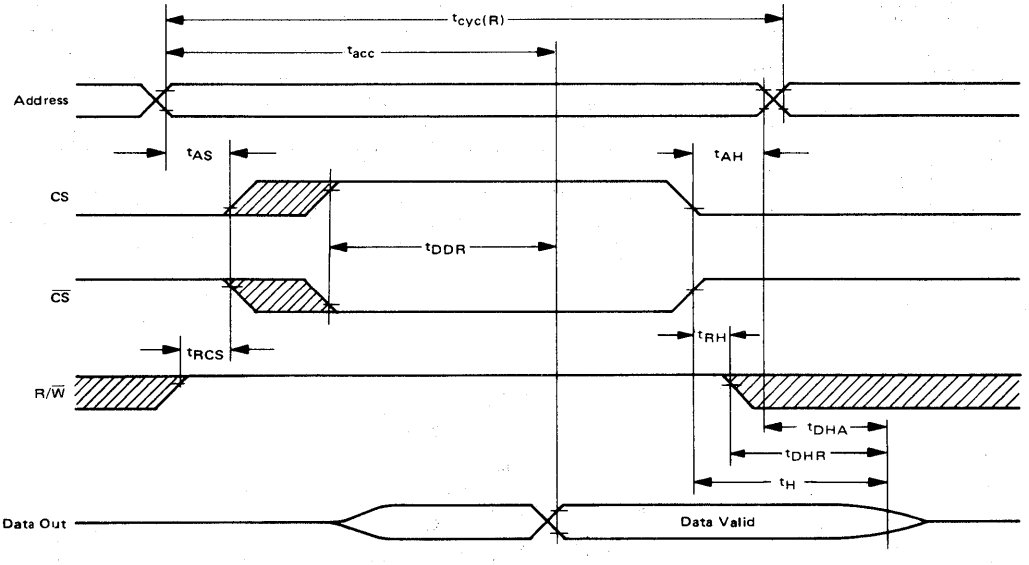
*Includes Jig Capacitance

AC OPERATING CONDITIONS AND CHARACTERISTICS

READ CYCLE (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Characteristic	Symbol	MCM6810		MCM68A10		MCM68B10		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	450	–	360	–	250	–	ns
Access Time	t_{acc}	–	450	–	360	–	250	ns
Address Setup Time	t_{AS}	20	–	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	0	–	ns
Data Delay Time (Read)	t_{DDR}	–	230	–	220	–	180	ns
Read to Select Delay Time	t_{RCS}	0	–	0	–	0	–	ns
Data Hold from Address	t_{DHA}	10	–	10	–	10	–	ns
Output Hold Time	t_H	10	–	10	–	10	–	ns
Data Hold from Read	t_{DHR}	10	80	10	60	10	60	ns
Read Hold from Chip Select	t_{RH}	0	–	0	–	0	–	ns

READ CYCLE TIMING



NOTES:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.
3. CS and $\overline{CS}$ have same timing.

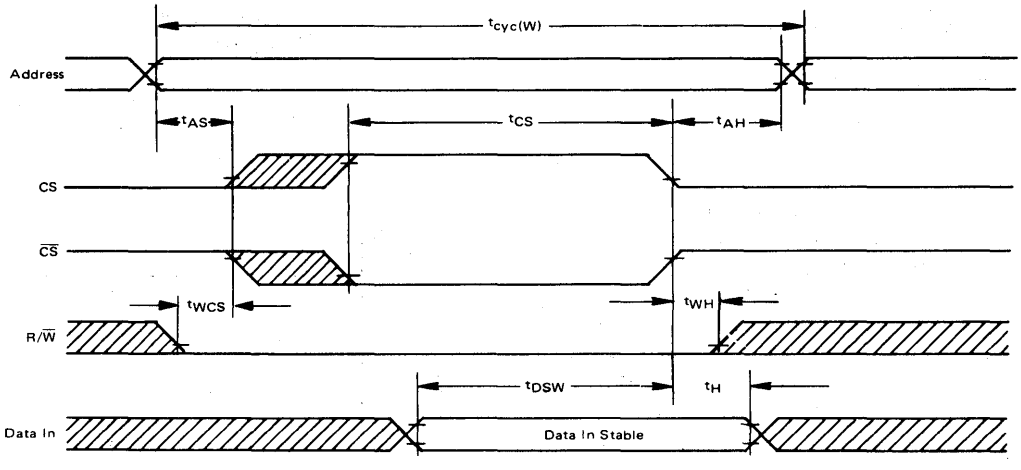
= Don't Care

WRITE CYCLE (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Characteristic	Symbol	MCM6810		MCM68A10		MCM68B10		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	450	–	360	–	250	–	ns
Address Setup Time	t_{AS}	20	–	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	0	–	ns
Chip Select Pulse Width	t_{CS}	300	–	250	–	210	–	ns
Write to Chip Select Delay Time	t_{WCS}	0	–	0	–	0	–	ns
Data Setup Time (Write)	t_{DSW}	190	–	80	–	60	–	ns
Input Hold Time	t_H	10	–	10	–	10	–	ns
Write Hold Time from Chip Select	t_{WH}	0	–	0	–	0	–	ns

SRAM

WRITE CYCLE TIMING



NOTES:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.
3. CS and $\overline{CS}$ have same timing.

= Don't Care

MOTOROLA

MCM2114

4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM2114 is a 4096-bit random access memory fabricated with high density, high reliability N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL, and requires no clocks or refreshing because of fully static operation. Data access is particularly simple, since address setup times are not required. The output data has the same polarity as the input data.

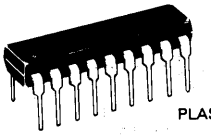
The MCM2114 is designed for memory applications where simple interfacing is the design objective. The MCM2114 is assembled in 18-pin dual-in-line packages with the industry standard pin-out. A separate chip select ($\overline{S}$) lead allows easy selection of an individual package when the three-state outputs are OR-tied.

- Single +5 Volt Supply
- 1024 Words by 4-Bit Organization
- Fully Static: Cycle Time = Access Time
- No Clock or Timing Strobe Required
- Maximum Access Time
  - 200 ns — MCM2114-20
  - 250 ns — MCM2114-25
  - 300 ns — MCM2114-30
  - 450 ns — MCM2114-45
- Power Dissipation: 100 mA Maximum (Active)
- Common Data Input and Output
- Three-State Outputs for OR-Ties
- Industry Standard 18-Pin Configuration
- Fully TTL Compatible

MOS

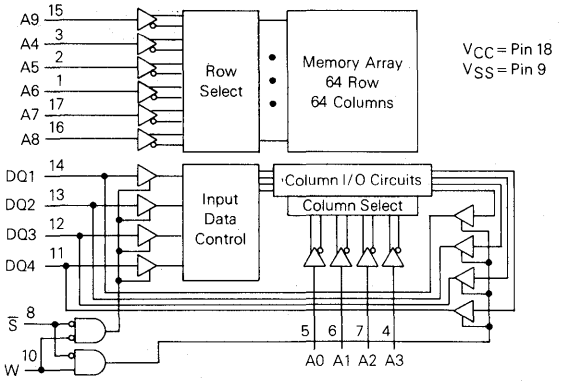
(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY

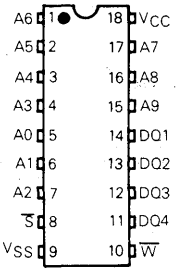


P SUFFIX
PLASTIC PACKAGE
CASE 707

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0-A9	Address Input
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
DQ1-DQ4	Data Input Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	−0.5 to +7.0	V
DC Output Current	5.0	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0	0	0	
Logic 1 Voltage, All Inputs	V_{IH}	2.0	–	6.0	V
Logic 0 Voltage, All Inputs	V_{IL}	−0.5	–	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	MCM2114			Unit
		Min	Typ	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{LI}	–	–	10	μA
I/O Leakage Current ($\overline{S}$ = 2.4 V, V_{DQ} = 0.4 V to V_{CC})	$\|I_{LO}\|$	–	–	10	μA
Power Supply Current (V_{in} = 5.5 V, I_{DQ} = 0 mA, T_A = 25°C)	I_{CC1}	–	80	95	mA
Power Supply Current (V_{in} = 5.5 V, I_{DQ} = 0 mA, T_A = 0°C)	I_{CC2}	–	–	100	mA
Output Low Current (V_{OL} = 0.4 V)	I_{OL}	2.1	6.0	–	mA
Output High Current (V_{OH} = 2.4 V)	I_{OH}	–	−1.4	−1.0	mA

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Input/Output Capacitance (V_{DQ} = 0 V)	$C_{I/O}$	5.0	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and termpature range unless otherwise noted.)

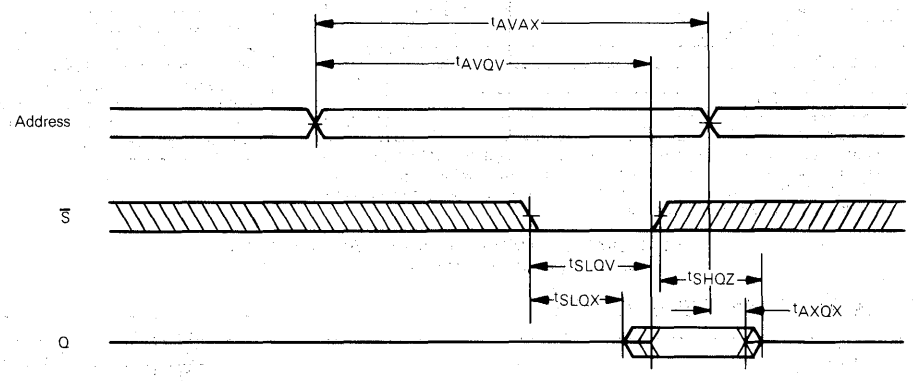
Input Pulse Levels.....0.8 Volt and 2.4 Volts
Input Rise and Fall Times.....10 ns
Input and Output Timing Levels.....1.5 Volts
Output Load.....1 TTL Gate and C_L = 100 pF

READ (NOTE 1), WRITE (NOTE 2) CYCLES

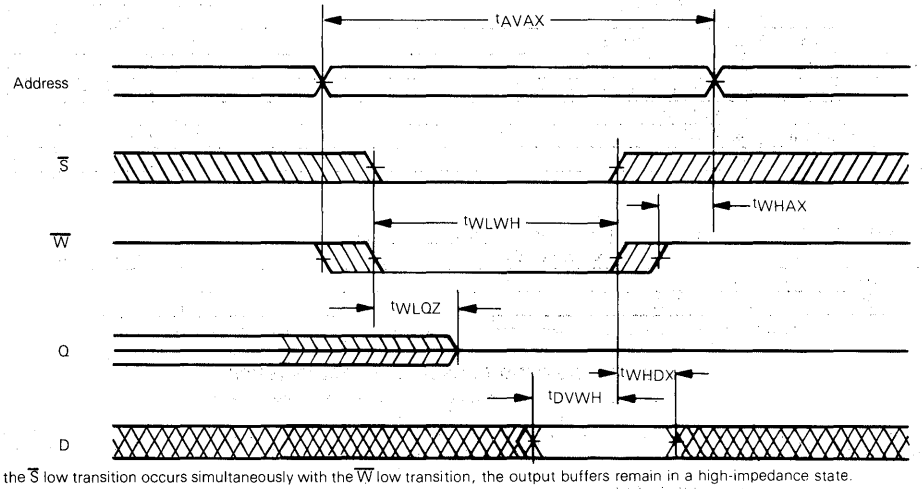
Parameter	Symbol	MCM2114-20		MCM2114-25		MCM2114-30		MCM2114-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care	t_{AVAX}	200	–	250	–	300	–	450	–	ns
Address Valid to Output Valid	t_{AVQV}	–	200	–	250	–	300	–	450	ns
Chip Select Low to Output Valid	t_{SLQV}	–	70	–	85	–	100	–	120	ns
Chip Select Low to Output Don't Care	t_{SLQX}	20	–	20	–	20	–	20	–	ns
Chip Select High to Output High Z	t_{SHQZ}	–	60	–	70	–	80	–	100	ns
Address Don't Care to Output Don't Care	t_{AXQX}	50	–	50	–	50	–	50	–	ns
Write Low to Write High	t_{WLWH}	120	–	135	–	150	–	200	–	ns
Write High to Address Don't Care	t_{WHAX}	0	–	0	–	0	–	0	–	ns
Write Low to Output High Z	t_{WLQZ}	–	60	–	70	–	80	–	100	ns
Data Valid to Write High	t_{DVWH}	120	–	135	–	150	–	200	–	ns
Write High to Data Don't Care	t_{WHDX}	0	–	0	–	0	–	0	–	ns

NOTES: 1. A Read occurs during the overlap of a low $\overline{S}$ and a high $\overline{W}$.
2. A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

READ CYCLE TIMING ($\overline{W}$ HELD HIGH)



WRITE CYCLE TIMING (NOTE 3)



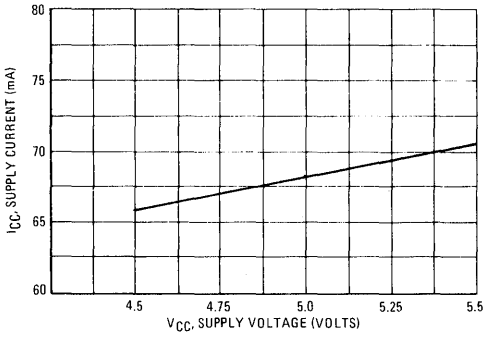
3. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transition, the output buffers remain in a high-impedance state.

WAVEFORMS

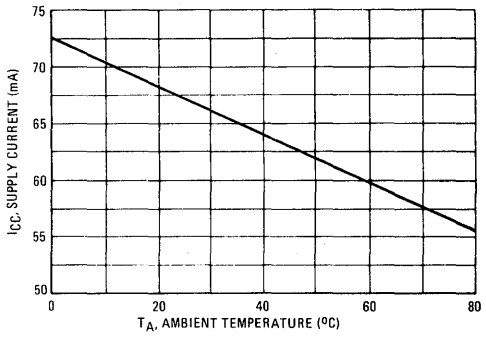
Waveform Symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

TYPICAL CHARACTERISTICS

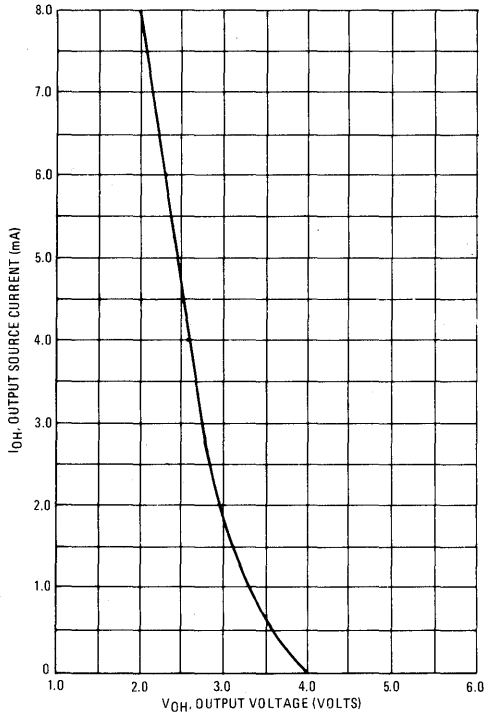
SUPPLY CURRENT versus SUPPLY VOLTAGE



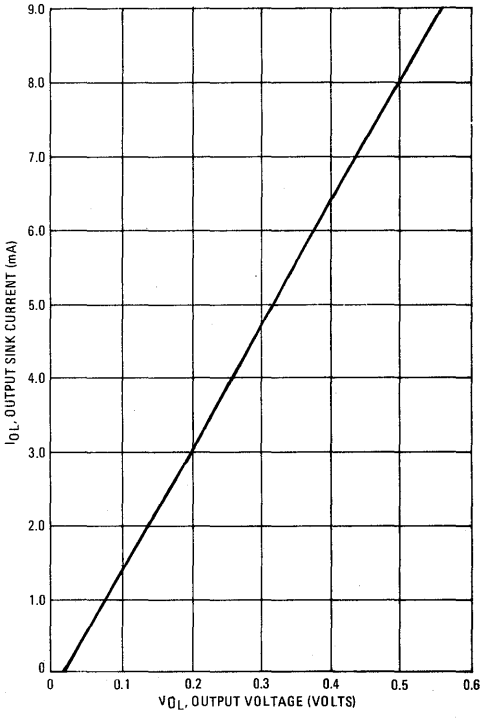
SUPPLY CURRENT versus AMBIENT TEMPERATURE



OUTPUT SOURCE CURRENT versus OUTPUT VOLTAGE

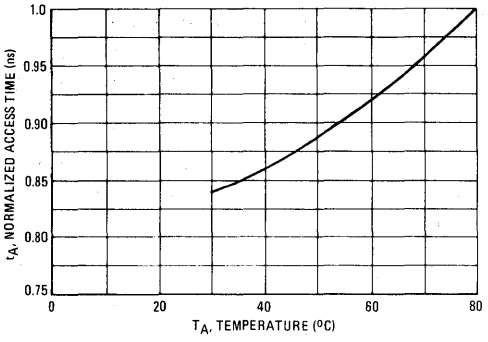


OUTPUT SINK CURRENT versus OUTPUT VOLTAGE

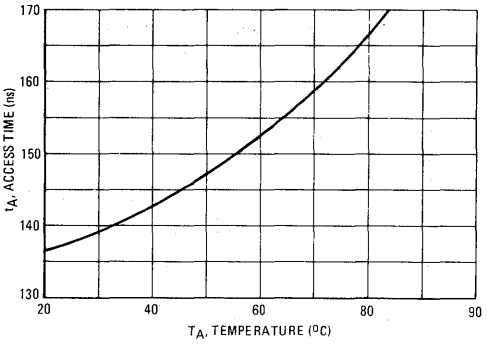


SRAM

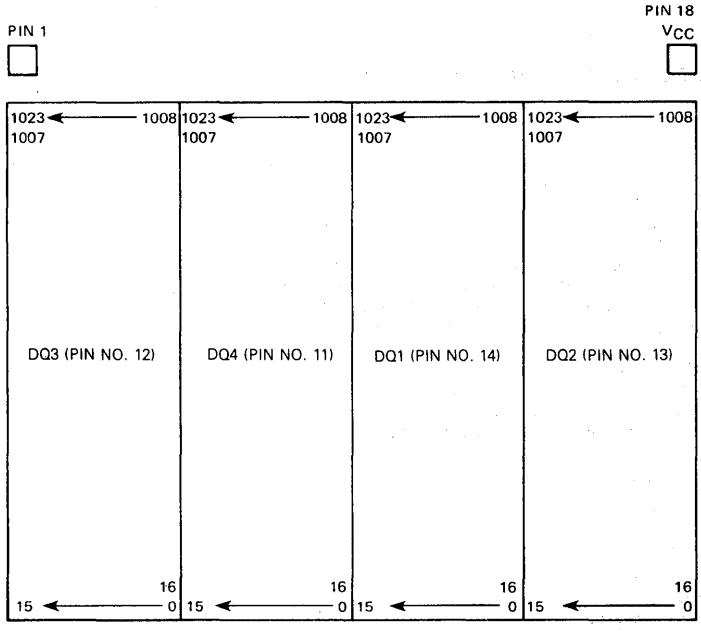
NORMALIZED ACCESS TIME versus TEMPERATURE



TYPICAL ACCESS TIME versus TEMPERATURE



MCM2114 BIT MAP



To determine the precise location on the die of a word in memory, reassign address numbers to the address pins as in the table below. The bit locations can then be determined directly from the bit map.

PIN NUMBER	REASSIGNED ADDRESS NUMBER	PIN NUMBER	REASSIGNED ADDRESS NUMBER
1	A6	6	A1
2	A5	7	A2
3	A4	15	$\overline{A9}$
4	A3	16	$\overline{A8}$
5	A0	17	$\overline{A7}$

MOTOROLA

MCM6147

4K BIT STATIC RANDOM ACCESS MEMORY

The MCM6147 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit, fabricated using Motorola's high performance CMOS silicon gate technology (HCMOS). It uses a design approach which provides the simple timing features associated with fully static memories and the reduced power associated with CMOS memories. This means low power without the need for clocks, nor reduced data rates due to cycle times that exceed access times.

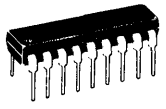
Chip Enable ($\overline{E}$) controls the power-down feature. It is not a clock, but rather a chip control that affects power consumption. After $\overline{E}$ goes high, initiating deselect mode, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high.

The MCM6147 is in an 18-pin dual in-line package with the industry standard pin out. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

- Single +5 V Supply
- Fully Static Memory — No Clock or Timing Strobe Required
- Maximum Access Time
  - MCM6147-55 = 55 ns
  - MCM6147-70 = 70 ns
- Automatic Power Down
- Low Power Dissipation
  - 35 mA Maximum (Active)
  - 12 mA Maximum (Standby — TTL Levels)
  - 800 μA Maximum (Standby)
  - 100 μA Maximum (Standby — MCM61L47)
- Low Standby Power Version Available
- Directly TTL Compatible — All Inputs and Output
- Separate Data Input and Three-State Output
- Equal Access and Cycle Time
- High Density 18-Pin Package

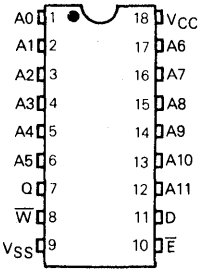
HCMOS
(COMPLEMENTARY MOS)

4,096 × 1 BIT STATIC RANDOM ACCESS MEMORY

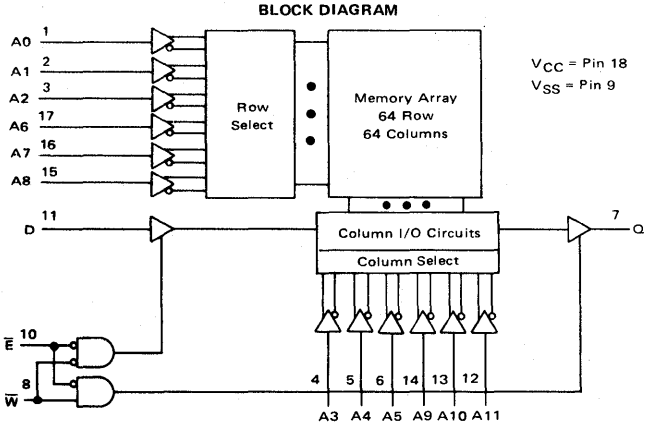


P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENTS



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address
$\overline{E}$	Chip Enable
D	Data In
Q	Data Out
$\overline{W}$	Write
V_{CC}	Power (+5 V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS(See note)

Rating	Value	Unit
Temperature Under Bias	−10 to +85	°C
Voltage on Any Pin with Respect to V_{CC}	−0.5 to +7.0	V
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V
Logic 1 Voltage, All Inputs	V_{IH}	2.0	–	6.0	V
Logic 0, Voltage, All Inputs	V_{IL}	−0.3	–	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	MCM61L47-55			MCM6147-55			MCM61L47-70			MCM6147-70			Unit
		Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{IL}	–	0.01	1.0	–	0.01	1.0	–	0.01	1.0	–	0.01	1.0	μA
Output Leakage Current ($\overline{E}$ = 2.0 V, V_{out} = 0 to 5.5 V)	I_{OL}	–	0.1	1.0	–	0.1	1.0	–	0.1	1.0	–	0.1	1.0	μA
Power Supply Current ($\overline{E}$ = V_{IL}, Output Open)	I_{CC}	–	15	35	–	15	35	–	15	35	–	15	35	mA
Standby Current ($\overline{E}$ = V_{IH})	I_{SB}	–	5	12	–	5	12	–	5	12	–	5	12	mA
Standby Current ($\overline{E}$ = V_{CC} − 0.2 V) (0.2 V ≥ V_{in} ≥ V_{CC} − 0.2 V)	I_{SB1}	–	25	100	–	200	800	–	25	100	–	200	800	μA
Input Low Voltage	V_{IL}	−0.3	–	0.8	−0.3	–	0.8	−0.3	–	0.8	−0.3	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	6.0	2.0	–	6.0	2.0	–	6.0	2.0	–	6.0	V
Output Low Voltage (I_{OL} = 12.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
Output High Voltage** (I_{OH} = −8.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V

*Typical values are for T_A = 25°C and V_{CC} = +5.0 V.

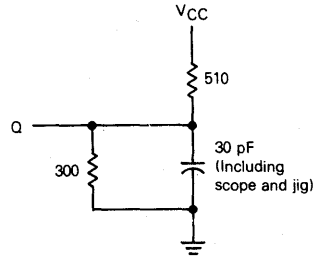
**Also, output voltages are compatible with Motorola's new High-Speed CMOS Logic Family, if the same power supply voltage is used.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	7.0	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

FIGURE 1 – OUTPUT LOAD



AC OPERATING CONDITIONS AND CHARACTERISTICS

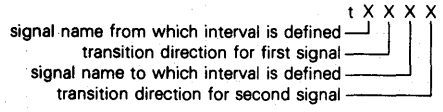
(Full operating voltage and temperature unless otherwise noted)

Input Pulse Levels .....0 Volt to 3.5 Volts
Input Rise and Fall Times .....10 ns
Input and Output Timing Reference Levels .....1.5 Volts
Output Load .....See Figure 1

READ, WRITE CYCLES

Parameter	Symbol	MCM61L47-55 MCM6147-55		MCM61L47-70 MCM6147-70		Unit
		Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Chip Enable is Held Active)	t_{AVAX}	55	–	70	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	55	–	70	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	–	55	–	70	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	–	55	–	70	ns
Address Valid to Output Invalid	t_{AVQX}	5	–	5	–	ns
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	10	–	ns
Chip Enable High to Output High Z	t_{EHQZ}	0	40	0	40	ns
Chip Selection to Power-Up Time	t_{PU}	0	–	0	–	ns
Chip Deselection to Power-Down Time	t_{PD}	0	30	0	30	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	0	–	ns
Chip Enable Low to Write High	t_{ELWH}	45	–	55	–	ns
Address Valid to Write High	t_{AVWH}	45	–	55	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	0	–	0	–	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	35	–	40	–	ns
Write High to Address Don't Care	t_{WHAX}	10	–	15	–	ns
Data Valid to Write High	t_{DVWH}	25	–	30	–	ns
Write High to Data Don't Care (Data Hold)	t_{WHDX}	10	–	10	–	ns
Write Low to Output High Z	t_{WLQZ}	0	30	0	35	ns
Write High to Output Valid	t_{WHQV}	0	–	0	–	ns

TIMING PARAMETER ABBREVIATIONS

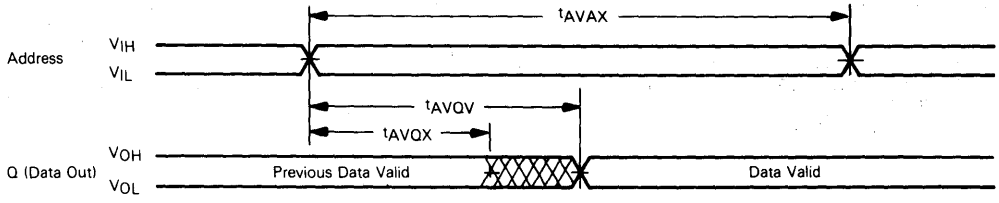


The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

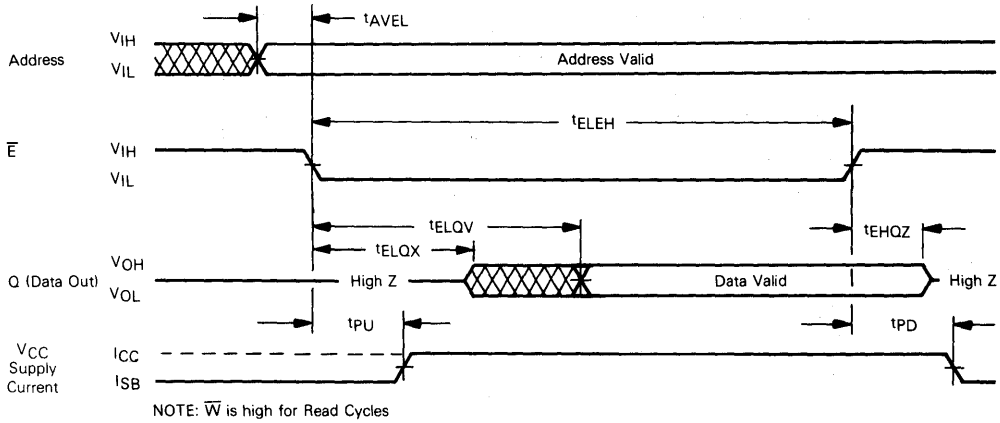
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE TIMING 1
($\overline{E}$ Held Low)

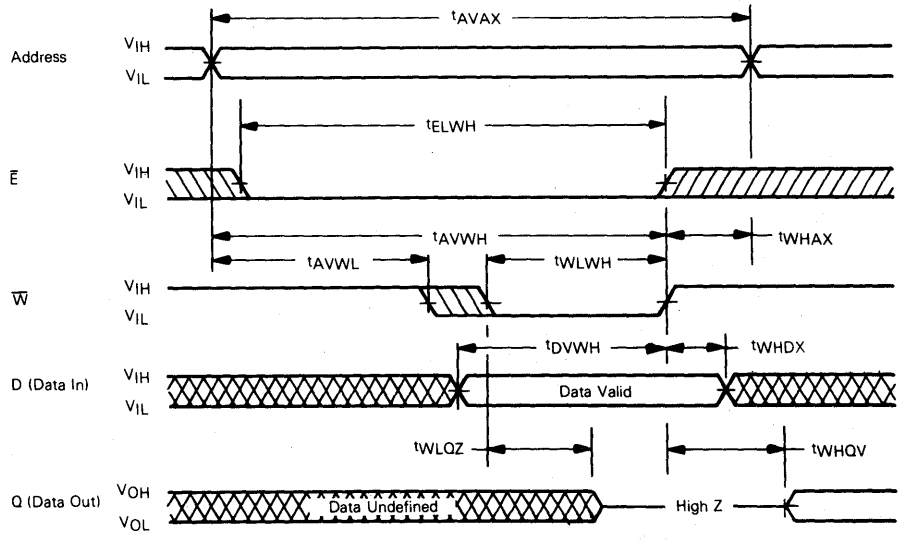


READ CYCLE TIMING 2



NOTE: $\overline{W}$ is high for Read Cycles

WRITE CYCLE TIMING



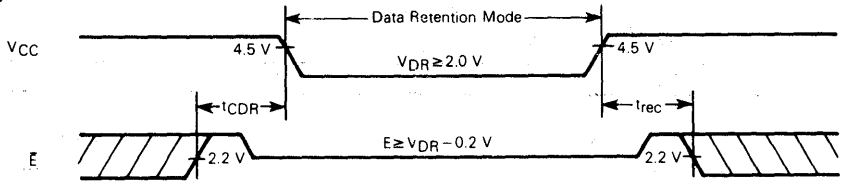
Data Out = Data In

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C) (MCM61L47 Only)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention	$\overline{E} \geq V_{CC} - 0.2$ V $V_{in} \geq V_{CC} - 0.2$ V or $V_{in} \leq 0.2$ V	V_{DR}	2.0	–	–	V
Data Retention Current	$V_{CC} = 3.0$ V, $\overline{E} \geq 2.8$ V $V_{in} \geq 2.8$ V or $V_{in} \leq 0.2$ V	I_{CCDR}	–	–	40	μA
Chip Disable to Data Retention Time	See Retention Waveform	t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	*t_{AVAX}	–	–	ns

*t_{AVAX} = Read Cycle Time.

LOW V_{CC} DATA RETENTION WAVEFORM



SRAM

MOTOROLA

MCM2016H

Advance Information

FAST 16K BIT STATIC RAM

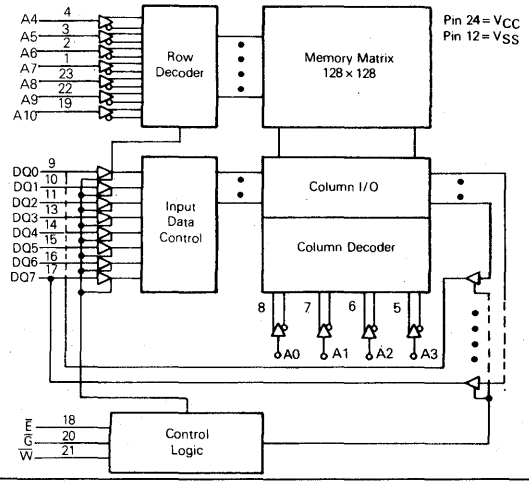
The MCM2016H is a 16,384-bit Static Random Access Memory organized as 2048 words by 8 bits, fabricated using Motorola's High-performance silicon-gate MOS (HMOS) technology. It uses an innovative design approach which combines the ease-of-use features of fully static operation (no external clocks or timing strobes required) with the reduced standby power dissipation associated with clocked memories. To the user this means low standby power dissipation without the need for address setup and hold times, nor reduced data rates due to cycle times that are no longer than access times. Perfect for cache and sub-100 ns buffer memory systems, this high speed static RAM is intended for applications that demand superior performance and reliability.

Chip Enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after chip enable ($\overline{E}$) goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as the chip enable ($\overline{E}$) remains high. This feature provides significant system-level power savings.

The MCM2016H is in a 24-pin dual-in-line 300 mil wide package with the industry standard JEDEC approved pinout. A 24 pin dual-in-line 600 mil wide package is also available.

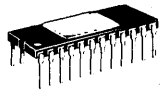
- Single +5 Volt Operation (±10%)
- Fully Static: No Clock or Timing Strobe Required
- Fast Access Time: MCM2016H-45 – 45 ns (max)
  MCM2016H-55 – 55 ns (max)
  MCM2016H-70 – 70 ns (max)
- Power Dissipation: 120 mA Maximum (Active)
  20 mA Maximum (Standby)
- Three-State Output

BLOCK DIAGRAM

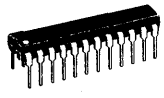


MOS
(N-CHANNEL, SILICON-GATE)

2,048×8 BIT STATIC RANDOM ACCESS MEMORY



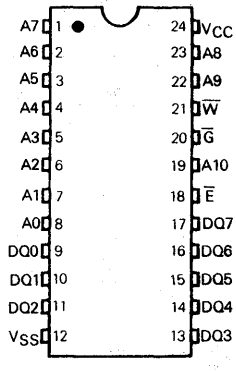
Y SUFFIX
CERAMIC PACKAGE
CASE 716



P SUFFIX
PLASTIC PACKAGE
CASE 724

SRAM

PIN ASSIGNMENTS



PIN NAMES	
A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power (+5 V)
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	−0.5 to +7.0	V
DC Output Current	20	mA
Power Dissipation	1.2	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage**	V_{IH}	2.0	3.0	6.0	V
	V_{IL}	−0.5*	0	0.8	V

*The device will withstand undershoots to the −2.5 volt level with a maximum pulse width of 50 ns. This is periodically sampled rather than 100% tested.

**50 ns maximum address rise and fall times, while the chip is selected.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{CC} = 5.5 V, V_{in} = GND to V_{CC})	I_{LI}	−10	10	μA
Output Leakage Current ($\overline{E}=V_{IH}$ or $\overline{G}=V_{IH}$, $V_{I/O}$ = GND to V_{CC})	I_{LO}	−50	50	μA
Operating Power Supply Current ($\overline{E}=V_{IL}$, $I_{I/O}$ = 0 mA)	I_{CC1}	—	120	mA
Standby Power Supply Current ($\overline{E}=V_{IH}$)	I_{SB}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA) See Figure 1	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA) See Figure 1	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance except $\overline{E}$, DQ	C_{in}	3	5	pF
Input/Output Capacitance and $\overline{E}$ Input Capacitance	$C_{I/O}$	5	7	pF

MODE SELECTION

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	V_{CC} Current	DQ
Standby	H	X	X	I_{SB}	High Z
Read	L	L	H	I_{CC}	Q
Write Cycle (1)	L	X	L	I_{CC}	D
Write Cycle (2)	L	X	L	I_{CC}	D

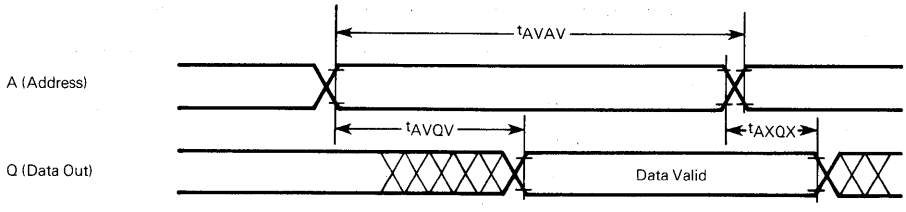
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels ..... 0 and 3.0 Volts
Input Rise and Fall Times ..... 5 ns
Input and Output Timing Reference Levels ..... 0.8 and 2.0 Volts
Output Load ..... See Figure 2

READ CYCLE #1 (Address Controlled) $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{W} = V_{IH}$

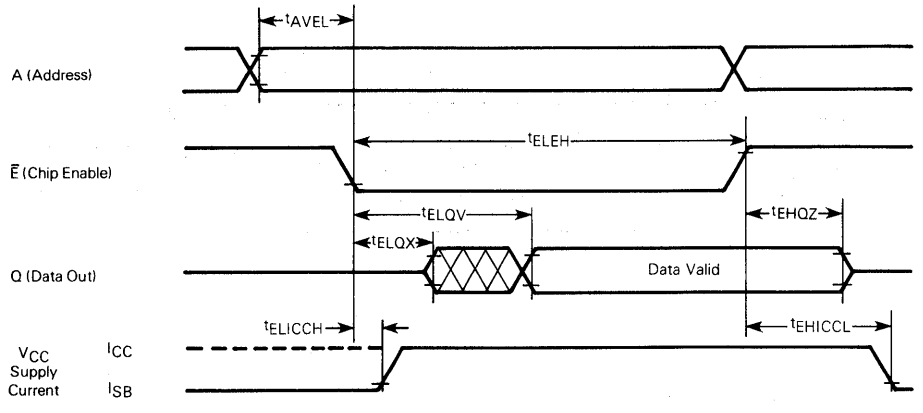
Parameter	Symbol		MCM2016H-45		MCM2016H-55		MCM2016H-70		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Output Valid (Address Access Time)	t_{AVQV}	t_{AA}	–	45	–	55	–	70	ns
Address Valid to Address Valid (Read Cycle Time)	t_{AVAV}	t_{RC}	45	–	55	–	70	–	ns
Address Invalid to Output Invalid (Output Hold Time)	t_{AXQX}	t_{OH}	5	–	5	–	5	–	ns



SRAM

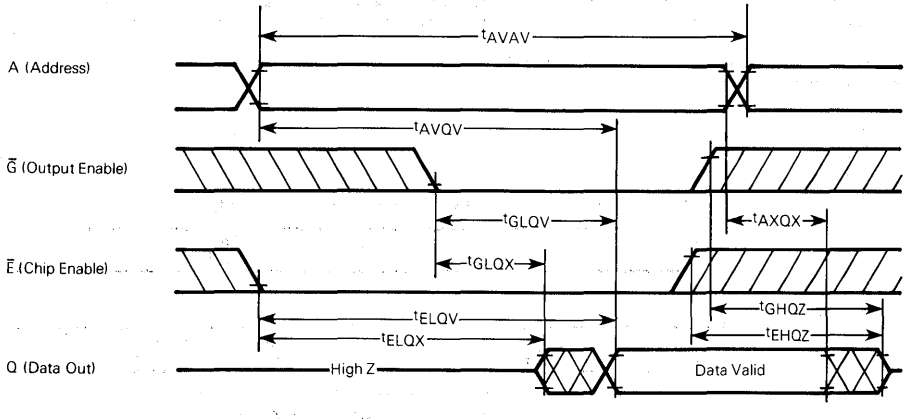
READ CYCLE #2 (Chip Enable Controlled) $\overline{G} = V_{IL}$, $\overline{W} = V_{IH}$

Parameter	Symbol		MCM2016H-45		MCM2016H-55		MCM2016H-70		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Chip Enable Low to Output Valid (Chip Enable Access Time)	t_{ELQV}	t_{ACS}	–	45	–	55	–	70	ns
Chip Enable Low to Chip Enable High (Read Cycle Time)	t_{ELEH}	t_{RC}	45	–	55	–	70	–	ns
Address Valid to Chip Enable Low (Address Setup to Enable Active)	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns
Chip Enable Low to Output Invalid (Chip Enable to Output Active)	t_{ELQX}	t_{LZ}	5	–	5	–	5	–	ns
Chip Enable High to Output High Z (Chip Disable to Output Disable)	t_{EHQZ}	t_{HZ}	0	20	0	20	0	20	ns
Chip Enable Low to Power Up	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	ns
Chip Enable High to Power Down	t_{EHICCL}	t_{PD}	–	20	–	20	–	20	ns



READ CYCLE #3 $\overline{W} = V_{IH}$

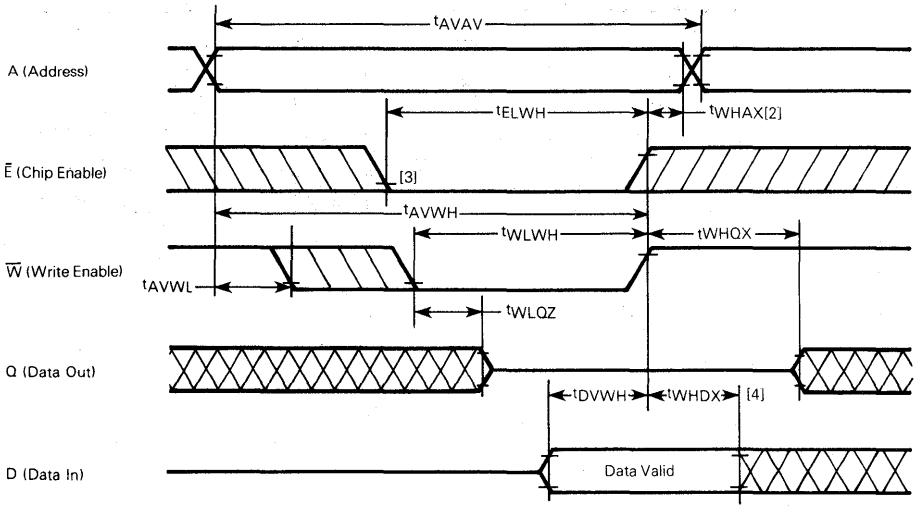
Parameter	Symbol		MCM2016H-45		MCM2016H-55		MCM2016H-70		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Chip Enable Low to Output Valid (Chip Enable Access Time)	t_{ELQV}	t_{ACS}	–	45	–	55	–	70	ns
Address Valid to Output Valid (Address Access Time)	t_{AVQV}	t_{AA}	–	45	–	55	–	70	ns
Address Valid to Address Valid (Read Cycle Time)	t_{AVAV}	t_{RC}	45	–	55	–	70	–	ns
Address Invalid to Output Invalid (Output Hold Time)	t_{AXQX}	t_{OH}	5	–	5	–	5	–	ns
Chip Enable Low to Output Invalid (Chip Enable to Output Active)	t_{ELQX}	t_{LZ}	5	–	5	–	5	–	ns
Chip Enable High to Output High Z (Chip Disable to Output Disable)	t_{EHQZ}	t_{HZ}	0	20	0	20	0	20	ns
Output Enable Low to Output Valid (Output Enable Access Time)	t_{GLQV}	t_{OE}	–	20	–	35	–	45	ns
Output Enable Low to Output Invalid (Output Enable to Output Active)	t_{GLQX}	t_{LX}	0	–	0	–	0	–	ns
Output Enable High to Output High Z (Output Disable to Output Disable)	t_{GHQZ}	t_{HZ}	0	20	0	20	0	30	ns



WRITE CYCLE #1 (Write Controlled Notes 1 and 3, $\overline{G} = V_{IL}$

Parameter	Symbol		MCM2016H-45		MCM2016H-55		MCM2016H-70		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Address Valid (Write Cycle Time)	t_{AVAV}	t_{WC}	45	–	55	–	70	–	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	t_{WP}	20	–	25	–	30	–	ns
Chip Enable Low to Write High (Chip Enable to End of Write)	t_{ELWH}	t_{EW}	40	–	50	–	65	–	ns
Data Valid to Write High (Data Setup to End of Write)	t_{DVWH}	t_{DW}	20	–	25	–	30	–	ns
Write High to Data Don't Care (Data Hold After End of Write)	t_{WHDX}	t_{DH}	0	–	10	–	10	–	ns
Address Valid to Write High (Address Setup to End of Write)	t_{AVWH}	t_{AW}	40	–	50	–	65	–	ns
Address Valid to Write Low (Address Setup to Beginning of Write)	t_{AVWL}	t_{AS}	0	–	0	–	0	–	ns
Write High to Address Don't Care (Address Hold After End of Write)	t_{WHAX}	t_{WR}	0	–	0	–	0	–	ns
Write Low to Output High Z (Write Enable to Output Disable)	t_{WLQZ}	t_{WZ}	0	20	0	20	0	20	ns
Write High to Output Don't Care (Output Active After End of Write)	t_{WHQX}	t_{OW}	0	10	0	10	0	10	ns

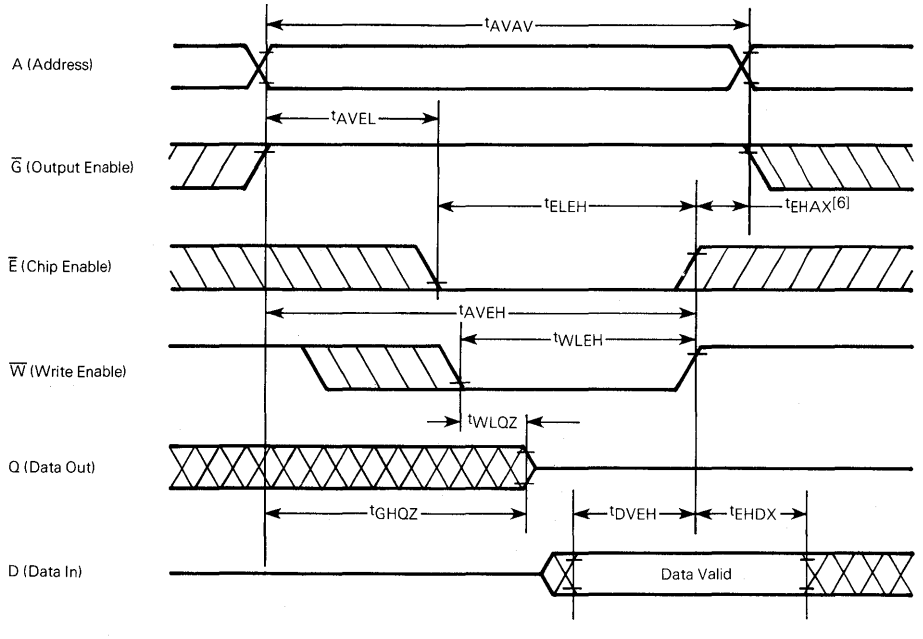
NOTES:
1. Write enable ($\overline{W}$) must be high during all address transitions.
2. t_{WHAX} is measured from the earlier of chip enable ($\overline{E}$) or write enable ($\overline{W}$) going high to the end of write cycle.
3. If the chip enable ($\overline{E}$) low transition occurs simultaneously with the write enable ($\overline{W}$) transition, the output remains in a high impedance state.
4. If chip enable ($\overline{E}$) is low during this period, DQ pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.



WRITE CYCLE #2 (Chip Enable Controlled) Note 5

Parameter	Symbol		MCM2016H-45		MCM2016H-55		MCM2016H-70		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Address Valid (Write Cycle Time)	t_{AVAV}	t_{WC}	45	–	55	–	70	–	ns
Write Low to Chip Enable High (Write Pulse Width)	t_{WLEH}	t_{WP}	20	–	20	–	20	–	ns
Chip Enable Low to Chip Enable High (Chip Enable to End of Write)	t_{ELEH}	t_{EW}	45	–	55	–	70	–	ns
Data Valid to Chip Enable High (Data Setup to End of Write)	t_{DVEH}	t_{DW}	20	–	20	–	20	–	ns
Chip Enable High to Data Don't Care (Data Hold After End of Write)	t_{EHDX}	t_{DH}	5	–	5	–	5	–	ns
Address Valid to Chip Enable High (Address Setup to End of Write)	t_{AVEH}	t_{AW}	45	–	55	–	70	–	ns
Address Valid to Chip Enable Low (Address Setup to Chip Enable)	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns
Chip Enable High to Address Don't Care (Address Hold After End of Write)	t_{EHAX}	t_{WR}	0	–	0	–	0	–	ns
Write Low to Output High Z (Write Enable to Output Disable)	t_{WLQZ}	t_{HZ}	0	20	0	20	0	20	ns

NOTES:
5. Write enable ($\overline{W}$) must be high during all address transitions.
6. t_{EHAX} is measured from the earlier of chip enable ($\overline{E}$) or write enable ($\overline{W}$) going high to the end of write cycle.
7. If the chip enable ($\overline{E}$) low transition occurs simultaneously with the write enable ($\overline{W}$) transition, the output remains in a high impedance state.
8. If chip enable ($\overline{E}$) is low during this period, DQ pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.



SRAM

FIGURE 1 — DC OUTPUT LOAD

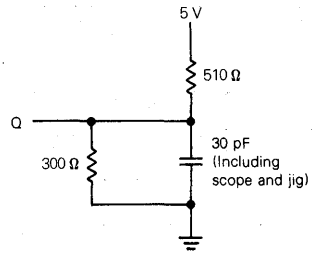
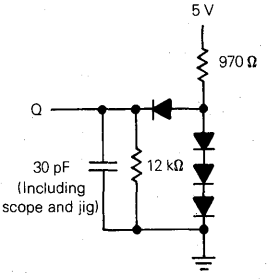


FIGURE 2 — AC OUTPUT LOAD



MOTOROLA

MCM2167H

Advance Information

MOS
(N-CHANNEL, SILICON-GATE)

16,384-BIT STATIC RANDOM ACCESS MEMORY

SRAM

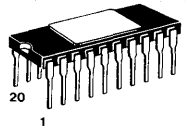
FAST 16K BIT STATIC RAM

The MCM2167H is a 16,384-bit Static Random Access Memory organized as 16,384 words by 1 bit, fabricated using Motorola's High-performance silicon-gate MOS (HMOS) technology. It uses an innovative design approach which combines the ease-of-use features of fully static operation (no external clocks or timing strobes required) with the reduced standby power dissipation associated with clocked memories. To the user this means low standby power dissipation without the need for address setup and hold times, nor reduced data rates due to cycle times that are no longer than access times. Perfect for cache and sub-100 ns buffer memory systems, this high speed static RAM is intended for applications demanding superior performance and reliability.

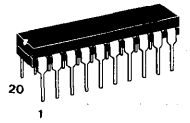
Chip Enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after Chip Enable ($\overline{E}$) goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as the Chip Enable ($\overline{E}$) remains high. This feature provides significant system-level power savings.

The MCM2167H is in a 20 pin dual-in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

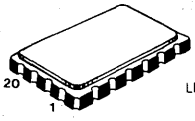
- Single +5 V Operation (±10%)
- Fully Static Memory — No Clock or Timing Strobe Required
- Fast Access Time: MCM2167H-35 — 35 ns Max.
  MCM2167H-45 — 45 ns Max.
  MCM2167H-55 — 55 ns Max.
- Power Dissipation: 120 mA Maximum (Active)
  20 mA Maximum (Standby)
- Three-State Output



L SUFFIX
CERAMIC PACKAGE
CASE 729

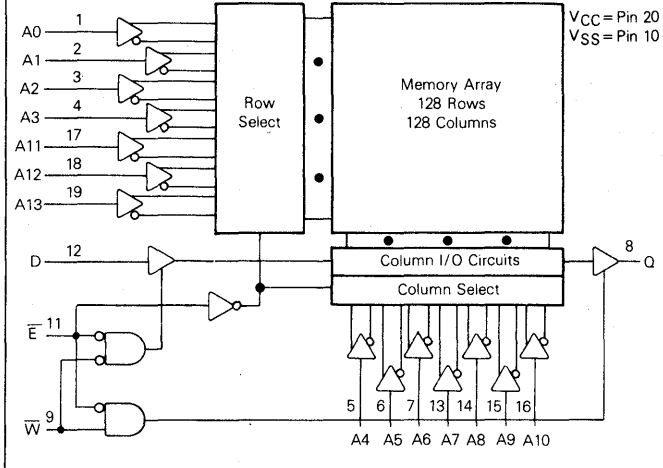


P SUFFIX
PLASTIC PACKAGE
CASE 738

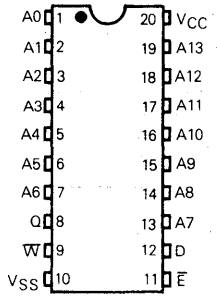


Z SUFFIX
LEADLESS CHIP CARRIER
CASE 752B

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0-A13	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	−0.5 to +7.0	V
DC Output Current	20	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage**	V_{IH}	2.0	3.0	6.0	V
	V_{IL}	−0.5*	0	0.8	V

*The device will withstand undershoots to −2.5 volt level with a maximum pulse width of 50 ns. This is periodically sampled rather than 100% tested.

**50 ns maximum address rise and fall times, while the chip is selected.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{CC}=5.5 V, V_{in}=GND to V_{CC})	I_{LI}	−10	10	μA
Output Leakage Current ($\overline{E}=V_{IH}$, $V_{I/O}$=GND to V_{CC}, V_{CC}=5.5 V)	I_{LO}	−50	50	μA
Operating Power Supply Current ($\overline{E}=V_{IL}$, $I_{I/O}$=0 mA)	I_{CC1}	—	120	mA
Standby Power Supply Current ($\overline{E}=V_{IH}$)	I_{SB}	—	20	mA
Output Low Voltage (I_{OL}=8.0 mA) See Figure 1	V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA) See Figure 1	V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, T_A=25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance except, $\overline{E}$, DQ	C_{in}	3	5	pF
Input/Output Capacitance and $\overline{E}$ Input Capacitance	$C_{I/O}$	3	7	pF

MODE SELECTION

Mode	$\overline{E}$	$\overline{W}$	V_{CC} Current	Q
Standby	H	X	I_{SB}	High Z
Read	L	H	I_{CC}	Data Out
Write Cycle (1)	L	L	I_{CC}	High Z
Write Cycle (2)	L	L	I_{CC}	High Z

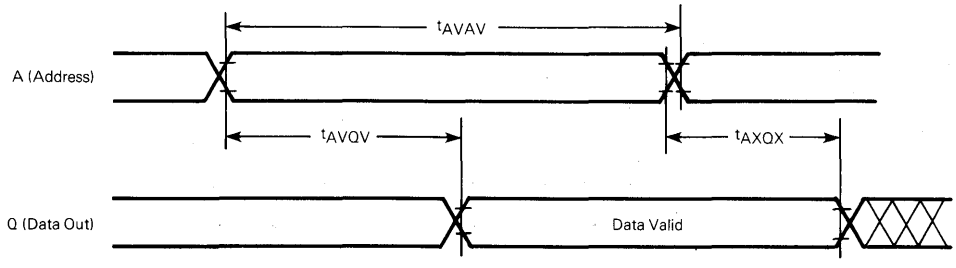
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

Input Pulse Levels ..... 0 and 3.0 Volts
Input Rise and Fall Times ..... 5 ns
Input and Output Timing Reference Levels ..... 0.8 and 2.0 Volts
Output Load ..... See Figure 2

READ CYCLE #1 (Address Controlled) $\overline{E} = V_{IL}$, $\overline{W} = V_{IH}$

Parameter	Symbol		MCM2167H-35		MCM2167H-45		MCM2167H-55		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Output Valid (Address Access Time)	t_{AVQV}	t_{AA}	–	35	–	45	–	55	ns
Address Valid to Address Valid (Read Cycle Time)	t_{AVAV}	t_{RC}	35	–	45	–	55	–	ns
Address Invalid to Output Invalid (Output Hold Time)	t_{AXQX}	t_{OH}	3	–	3	–	3	–	ns

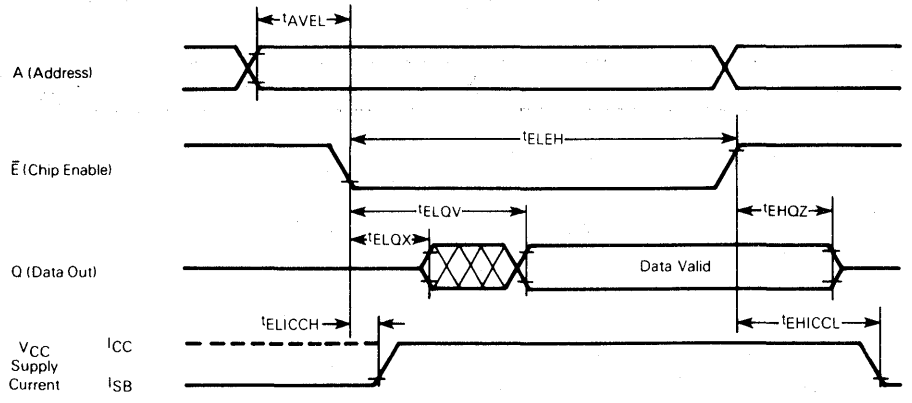


SRAM

READ CYCLE #2 (Chip Enable Controlled) Notes 1 and 2

Parameter	Symbol		MCM2167H-35		MCM2167H-45		MCM2167H-55		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Chip Enable Low to Output Valid (Chip Enable Access Time)	t_{ELQV}	t_{ACS}	–	35	–	45	–	55	ns
Chip Enable Low to Chip Enable High (Read Cycle Time)	t_{ELEH}	t_{RC}	35	–	45	–	55	–	ns
Address Valid to Chip Enable Low (Address Setup to Enable Active)	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns
Chip Enable Low to Output Invalid (Chip Enable to Output Active)	t_{ELQX}	t_{LZ}	5	–	5	–	5	–	ns
Chip Enable High to Output High Z (Chip Disable to Output Disable)	t_{EHQZ}	t_{HZ}	0	25	0	25	0	30	ns
Chip Enable Low to Power Up	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	ns
Chip Enable High to Power Down	t_{EHICCL}	t_{PD}	–	35	–	45	–	55	ns

NOTES:
1. Write Enable ($\overline{W}$) is high for read cycle.
2. Address valid prior to or coincident with Chip Enable ($\overline{E}$) transition low.

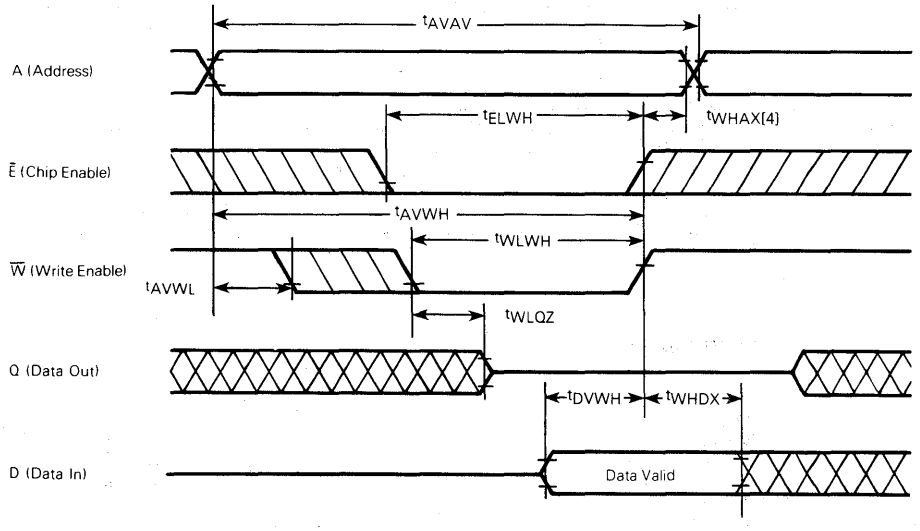


SRAM

WRITE CYCLE #1 (Write Controlled) Note 3

Parameter	Symbol		MCM2167H-35		MCM2167H-45		MCM2167H-55		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Address Valid (Write Cycle Time)	t_{AVAV}	t_{WC}	35	–	45	–	55	–	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	t_{WP}	20	–	20	–	25	–	ns
Chip Enable Low to Write High (Chip Enable to End of Write)	t_{ELWH}	t_{EW}	35	–	45	–	55	–	ns
Data Valid to Write High (Data Setup to End of Write)	t_{DVWH}	t_{DW}	15	–	15	–	20	–	ns
Write High to Data Don't Care (Data Hold After End of Write)	t_{WHDX}	t_{DH}	0	–	0	–	0	–	ns
Address Valid to Write High (Address Setup to End of Write)	t_{AVWH}	t_{AW}	35	–	45	–	55	–	ns
Address Valid to Write Low (Address Setup to Beginning of Write)	t_{AVWL}	t_{AS}	5	–	5	–	10	–	ns
Write High to Address Don't Care (Address Hold After End of Write)	t_{WHAX}	t_{WR}	0	–	0	–	0	–	ns
Write Low to Output High Z (Write Enable to Output Disable)	t_{WLQZ}	t_{WZ}	0	20	0	20	0	25	ns
Write High to Output Don't Care (Output Active After End of Write)	t_{WHQX}	t_{OW}	0	25	0	25	0	30	ns

NOTES:
3. Either Chip Enable ($\overline{E}$) or Write Enable ($\overline{W}$) must be high during all address transitions.
4. t_{WHAX} is measured from the earlier of Chip Enable ($\overline{E}$) or Write Enable ($\overline{W}$) going high to the end of write cycle.



WRITE CYCLE #2 (Chip Enable Controlled) Note 5

Parameter	Symbol		MCM2167H-35		MCM2167H-45		MCM2167H-55		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Address Valid (Write Cycle Time)	t_{AVAV}	t_{WC}	35	–	45	–	55	–	ns
Write Low to Chip Enable High (Write Pulse Width)	t_{WLEH}	t_{WP}	20	–	20	–	20	–	ns
Chip Enable Low to Chip Enable High (Chip Enable to End of Write)	t_{ELEH}	t_{EW}	35	–	45	–	55	–	ns
Data Valid to Chip Enable High (Data Setup to End of Write)	t_{DVEH}	t_{DW}	15	–	15	–	20	–	ns
Chip Enable High to Data Don't Care (Data Hold After End of Write)	t_{EHDX}	t_{DH}	5	–	5	–	5	–	ns
Address Valid to Chip Enable High (Address Setup to End of Write)	t_{AVEH}	t_{AW}	35	–	45	–	55	–	ns
Chip Enable High to Address Don't Care (Address Hold After End of Write)	t_{EHAX}	t_{WR}	0	–	0	–	0	–	ns

NOTES:
5. Either Chip Enable ($\overline{E}$) or Write Enable ($\overline{W}$) must be high during all address transitions.
6. t_{EHAX} is measured from the earlier of Chip Enable ($\overline{E}$) or Write Enable ($\overline{W}$) going high to the end of write cycle.

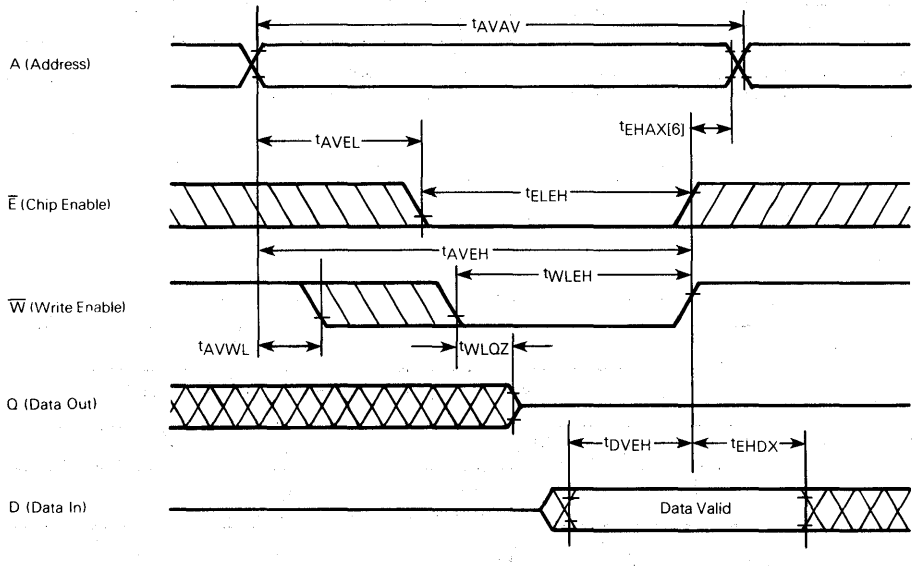


FIGURE 1 — DC OUTPUT LOAD

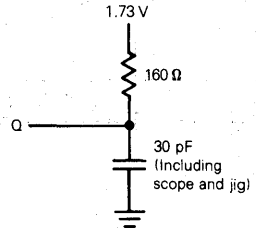
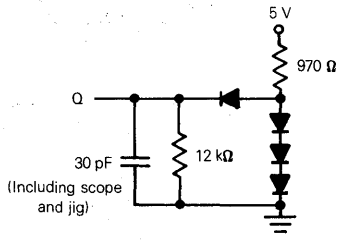


FIGURE 2 — AC OUTPUT LOAD



MOTOROLA

MCM6116

16K BIT STATIC RANDOM ACCESS MEMORY

The MCM6116 is a 16,384-bit Static Random Access Memory organized as 2048 words by 8 bits, fabricated using Motorola's high-performance silicon-gate CMOS (HCMOS) technology. It uses a design approach which provides the simple timing features associated with fully static memories and the reduced power associated with CMOS memories. This means low standby power without the need for clocks, nor reduced data rates due to cycle times that exceed access time.

Chip Enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after Chip Enable ($\overline{E}$) goes high, the part automatically reduces its power requirements and remains in this low-power standby as long as the Chip Enable ($\overline{E}$) remains high. The automatic power-down feature causes no performance degradation.

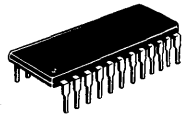
The MCM6116 is in a 24-pin dual-in-line package with the industry standard JEDEC approved pinout and is pinout compatible with the industry standard 16K EPROM/ROM.

- Single +5 V Supply
- 2048 Words by 8-Bit Operation
- HCMOS Technology
- Fully Static: No Clock or Timing Strobe Required
- Maximum Access Time: MCM6116-12 – 120 ns
  MCM6116-15 – 150 ns
  MCM6116-20 – 200 ns
- Power Dissipation: 70 mA Maximum (Active)
  15 mA Maximum (Standby-TTL Levels)
  2 mA Maximum (Standby)
- Low Power Version Also Available – MCM61L16
- Low Voltage Data Retention (MCM61L16 Only): 50 μA Maximum

HCMOS
(COMPLEMENTARY MOS)

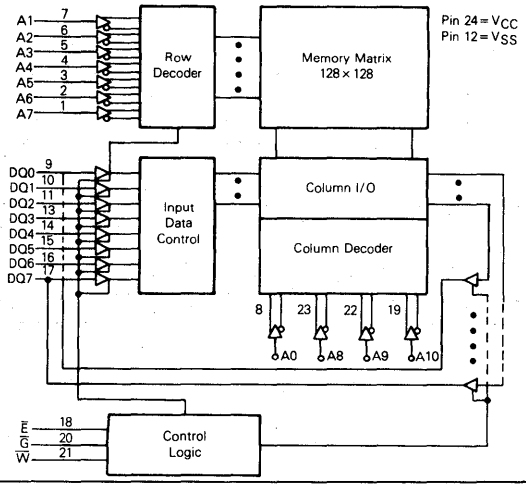
2,048 × 8 BIT STATIC RANDOM ACCESS MEMORY

SRAM

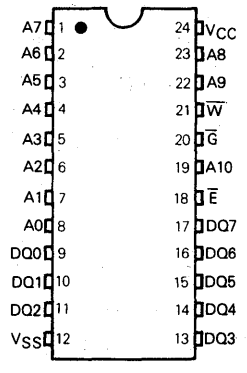


P SUFFIX
PLASTIC PACKAGE
CASE 709

BLOCK DIAGRAM



PIN ASSIGNMENTS



PIN NAMES	
A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power (+5 V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	−1.0 to +7.0	V
DC Output Current	20	mA
Power Dissipation	1.2	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature ranges unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−1.0*	–	0.8	V

*The device will withstand undershoots to the −1.0 volt level with a maximum pulse width of 50 ns at the −0.3 volt level. This is periodically sampled rather than 100% tested.

RECOMMENDED OPERATING CHARACTERISTICS

Parameter	Symbol	MCM6116			MCM61L16			Unit
		Min	Typ*	Max	Min	Typ*	Max	
Input Leakage Current (V_{CC} = 5.5 V, V_{in} = GND to V_{CC})	$\|I_{LI}\|$	–	–	1	–	–	1	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} $V_{I/O}$ = GND to V_{CC})	$\|I_{LO}\|$	–	–	1	–	–	1	μA
Operating Power Supply Current ($\overline{E}$ = V_{IL}, $I_{I/O}$ = 0 mA)	I_{CC}	–	35	70	–	35	55	mA
Average Operating Current Minimum cycle, duty = 100%	I_{CC2}	–	35	70	–	35	55	mA
Standby Power ($\overline{E}$ = V_{IH})	I_{SB}	–	5	15	–	5	12	mA
Supply Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≥ V_{CC} − 0.2 V or V_{in} ≤ 0.2 V)	I_{SB1}	–	20	2000	–	4	100	μA
Output Low Voltage (I_{OL} = 2.1 mA)	V_{OL}	–	–	0.4	–	–	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)**	V_{OH}	2.4	–	–	2.4	–	–	V

*V_{CC} = 5 V, T_A = 25°C

**Also, output voltages are compatible with Motorola's new high-speed CMOS logic family if the same power supply voltage is used.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance except $\overline{E}$	C_{in}	3	5	pF
Input/Output Capacitance and $\overline{E}$ Input Capacitance	$C_{I/O}$	5	7	pF

MODE SELECTION

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	V_{CC} Current	DQ
Standby	H	X	X	I_{SB}, I_{SB1}	High Z
Read	L	L	H	I_{CC}	Q
Write Cycle (1)	L	H	L	I_{CC}	D
Write Cycle (2)	L	L	L	I_{CC}	D

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

Input Pulse Levels ..... 0 Volt to 3.5 Volts
Input Rise and Fall Times ..... 10 ns
Input and Output Timing Reference Levels ..... 1.5 Volts
Output Load ..... 1 TTL Gate and C_L = 100 pF

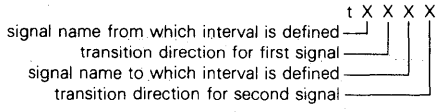
READ CYCLE

Parameter	Symbol	MCM6116-12 MCM61L16-12		MCM6116-15 MCM61L16-15		MCM6116-20 MCM61L16-20		Unit
		Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Chip Enable is Held Active)	t_{AVAX}	120	–	150	–	200	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	120	–	150	–	200	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	–	120	–	150	–	200	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	–	120	–	150	–	200	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	15	–	15	–	ns
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	15	–	15	–	ns
Chip Enable High to Output High Z	t_{EHQZ}	0	40	0	50	0	60	ns
Output Enable to Output Valid	t_{GLQV}	–	80	–	100	–	120	ns
Output Enable to Output Invalid	t_{GLQX}	10	–	15	–	15	–	ns
Output Enable to Output High Z	t_{GLQZ}	0	40	0	50	0	60	ns
Address Invalid to Output Invalid	t_{AXQX}	10	–	15	–	15	–	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	0	–	0	–	ns
Chip Enable to Power-Up Time	t_{PU}	0	–	0	–	0	–	ns
Chip Disable to Power-Down Time	t_{PD}	–	30	–	30	–	30	ns

WRITE CYCLE

Parameter	Symbol	MCM6116-12 MCM61L16-12		MCM6116-15 MCM61L16-15		MCM6116-20 MCM61L16-20		Unit
		Min	Max	Min	Max	Min	Max	
Chip Enable Low to Write High	t_{ELWH}	70	–	90	–	120	–	ns
Address Valid to Write High	t_{AVWH}	105	–	120	–	140	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	20	–	20	–	20	–	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	70	–	90	–	120	–	ns
Write High to Address Don't Care	t_{WHAX}	5	–	10	–	10	–	ns
Data Valid to Write High	t_{DVWH}	35	–	40	–	60	–	ns
Write High to Data Don't Care (Data Hold)	t_{WHDX}	5	–	10	–	10	–	ns
Write Low to Output High Z	t_{WLQZ}	0	50	0	60	0	60	ns
Write High to Output Valid	t_{WHQV}	5	–	10	–	10	–	ns
Output Disable to Output High Z	t_{GHQZ}	0	40	0	50	0	60	ns

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:

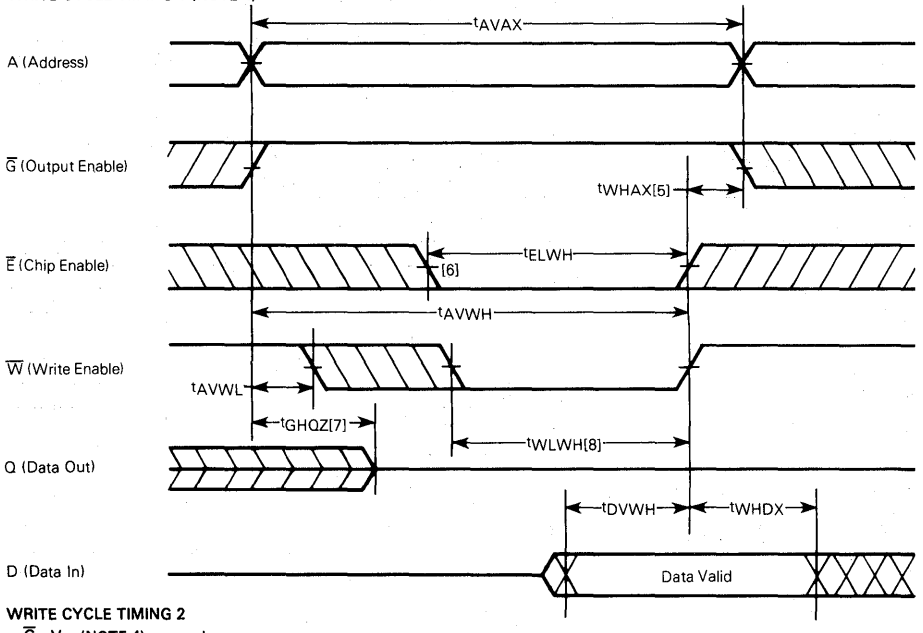
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

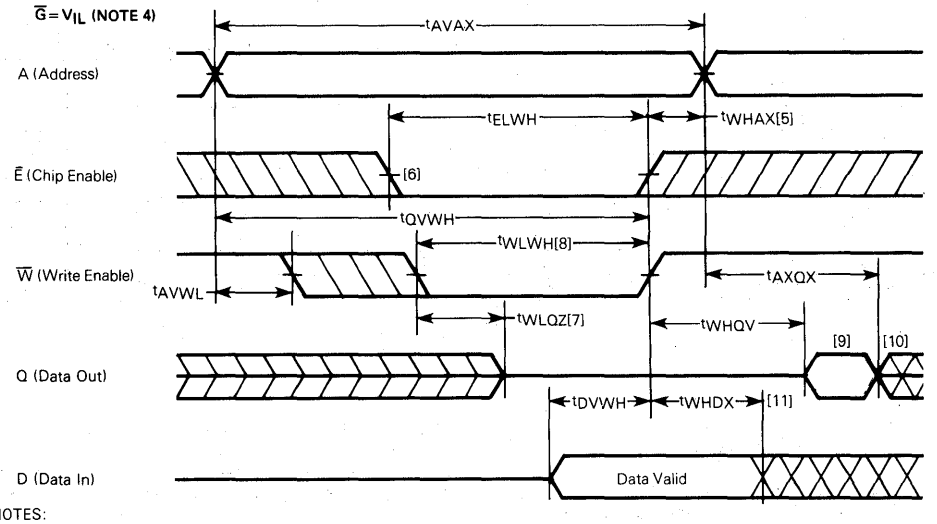
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

SRAM

WRITE CYCLE TIMING 1 (NOTE 4)



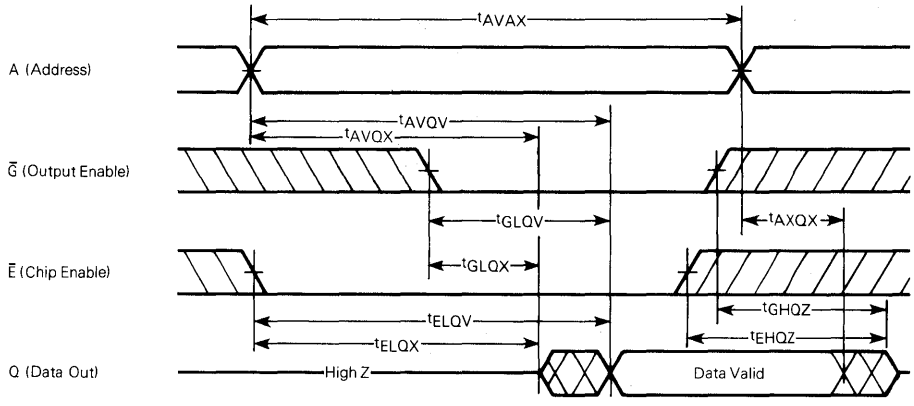
WRITE CYCLE TIMING 2
$\overline{G} = V_{IL}$ (NOTE 4)



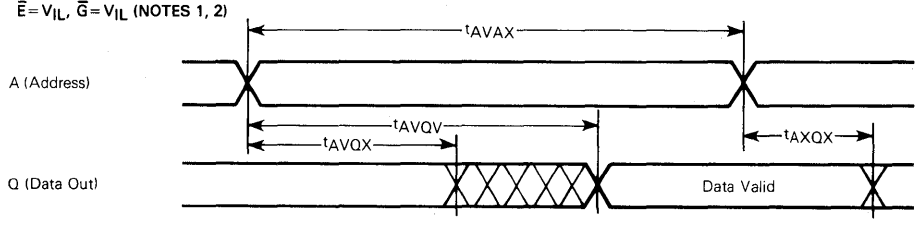
NOTES:

4. Write Enable ($\overline{W}$) must be high during all address transitions.
5. t_{WHAX} is measured from the earlier of Chip Enable ($\overline{E}$) or Write Enable ($\overline{W}$) going high to the end of write cycle.
6. If the Chip Enable ($\overline{E}$) low transition occurs simultaneously with the Write Enable ($\overline{W}$) low transitions or after the Write Enable ($\overline{W}$) transition, the output remains in a high impedance state.
7. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
8. A write occurs during the overlap of a low Chip Enable ($\overline{E}$) and a low Write Enable ($\overline{W}$).
9. Q (Data Out) is the same phase as write data of this write cycle.
10. Q (Data Out) is the read of the next address.
11. If Chip Enable ($\overline{E}$) is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

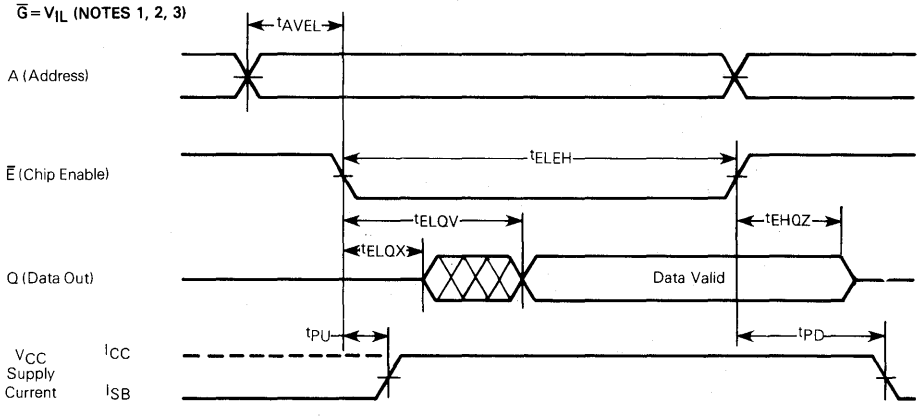
READ CYCLE TIMING 1 (NOTES 1 AND 2)



READ CYCLE TIMING 2
$\overline{E}=V_{IL}$, $\overline{G}=V_{IL}$ (NOTES 1, 2)



READ CYCLE TIMING 3
$\overline{G}=V_{IL}$ (NOTES 1, 2, 3)



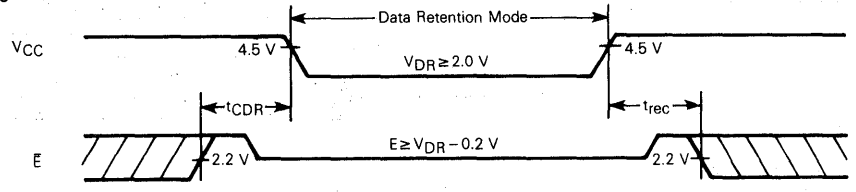
NOTES:
1. Write Enable ($\overline{W}$) is High for Read Cycle.
2. When Chip Enable ($\overline{E}$) is Low, the address input must not be in the high impedance state.
3. Address Valid prior to or coincident with Chip Enable ($\overline{E}$) transition Low.

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C) (MCM61L16 Only)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention	$\overline{E} \geq V_{CC} - 0.2$ V $V_{in} \geq V_{CC} - 0.2$ V or $V_{in} \leq 0.2$ V	V_{DR}	2.0	–	–	V
Data Retention Current	V_{CC} = 3.0 V, $\overline{E} \geq 2.8$ V $V_{in} \geq 2.8$ V or $V_{in} \leq 0.2$ V	I_{CCDR}	–	–	50	μA
Chip Disable to Data Retention Time	See Retention Waveform	t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	*t_{AVAX}	–	–	ns

*t_{AVAX} = Read Cycle Time.

LOW V_{CC} DATA RETENTION WAVEFORM



SRAM

MOTOROLA

MCM6168H

Product Preview

HCMOS
(COMPLEMENTARY MOS)

4,096 × 4 BIT
STATIC RANDOM
ACCESS MEMORY

SRAM

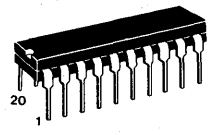
4K × 4 BIT STATIC RANDOM ACCESS MEMORY

The MCM6168H is a 16,384-bit Static Random Access Memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation High-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other sub-100 ns applications.

The Chip Enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature reduces system power requirements without degrading access performance.

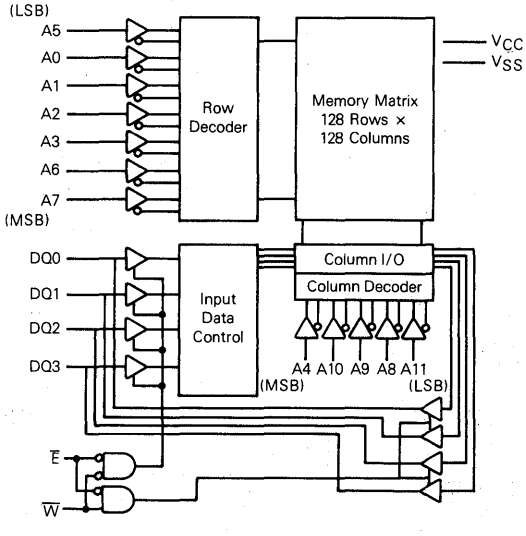
The MCM6168H is available in a 300 mil, 20 pin plastic dual in-line package with the JEDEC standard pinout.

- Single 5 V Supply
- 4K × 4 Bit Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time
- Low Power Operation: 50 mA Max. (Active)
  5 mA Max. (Standby—TTL Levels)
  2 mA Max. (Standby—Full Rail)

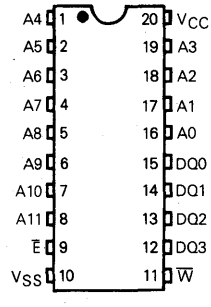


P SUFFIX
PLASTIC PACKAGE
CASE 738

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

MCM6169H

Product Preview

4K × 4 BIT STATIC RANDOM ACCESS MEMORY

The MCM6169H is a 16,384-bit Static Random Access Memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation High-performance silicon-gate CMOS (HCMOS III) technology. Employed design techniques provide the simple timing features of static memories (no external clocks or timing strobes required), combined with the lower power consumption and resultant reliability of CMOS circuitry. High speed access design makes this part suitable for cache and other sub-100 ns applications.

The Chip Enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature reduces system power requirements without degrading access performance.

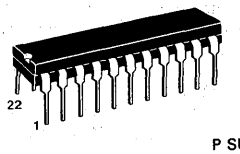
Output Enable ($\overline{G}$) is another feature which has been added to the device to allow the user very fast access to the data.

The MCM6169H is available in a 300 mil, 22 pin plastic dual in-line package.

- Single 5 V Supply
- 4K × 4 Bit Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Time
- Low Power Dissipation

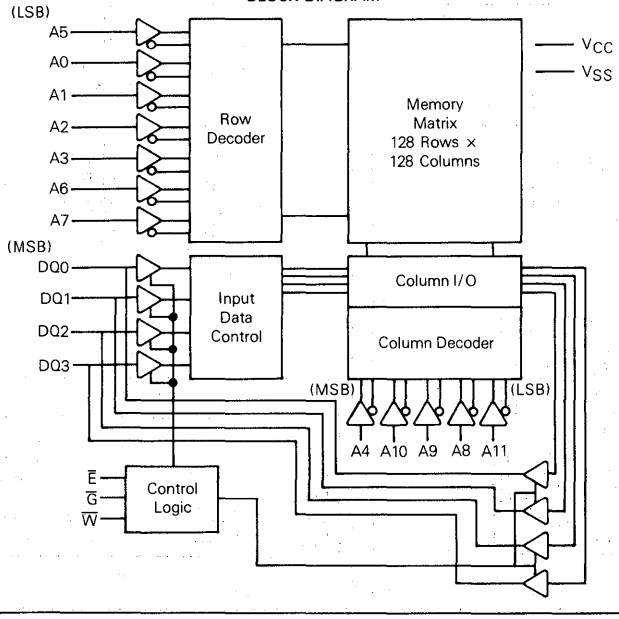
HCMOS
(COMPLEMENTARY MOS)

4,096 × 4 BIT STATIC RANDOM ACCESS MEMORY

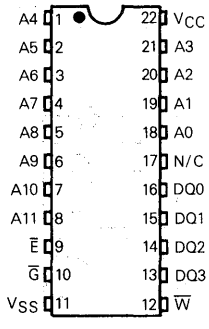


P SUFFIX
PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ3	Data Input/Output
V_{CC}	Power (+5 V)
V_{SS}	Ground
N/C	No Connect

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

MCM6164H

Product Preview

64K BIT STATIC RANDOM ACCESS MEMORY

The MCM6164H is a 65,536 bit Static Random Access Memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation High-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability.

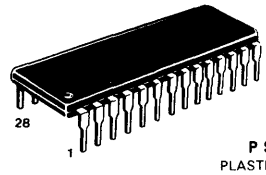
The Chip Enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of positive- and negative-logic Chip Enable pins provides more system design flexibility than single Chip Enable devices.

The MCM6164H is available in a 600 mil, 28 pin plastic dual in-line package with the JEDEC standard pinout.

- Single 5 V Supply
- 8K × 8 Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time
- Low Power Dissipation

HCMOS
(COMPLEMENTARY MOS)

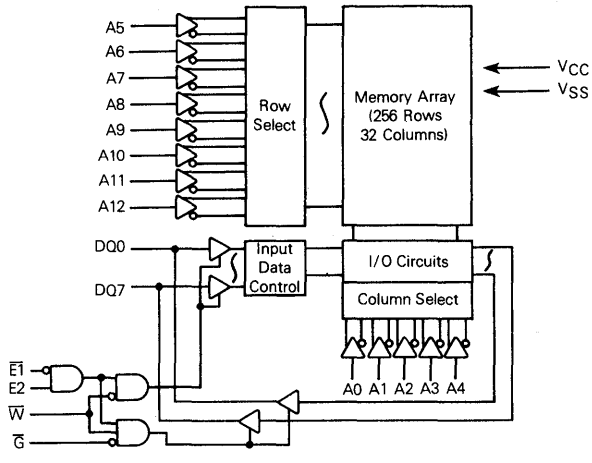
8192 × 8 BIT
STATIC
RANDOM ACCESS MEMORY



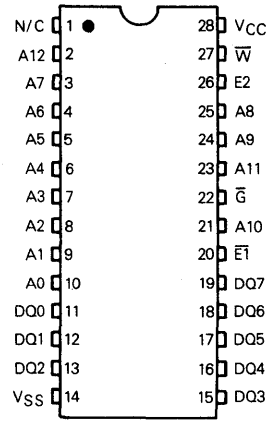
P SUFFIX
PLASTIC PACKAGE
CASE 710

SRAM

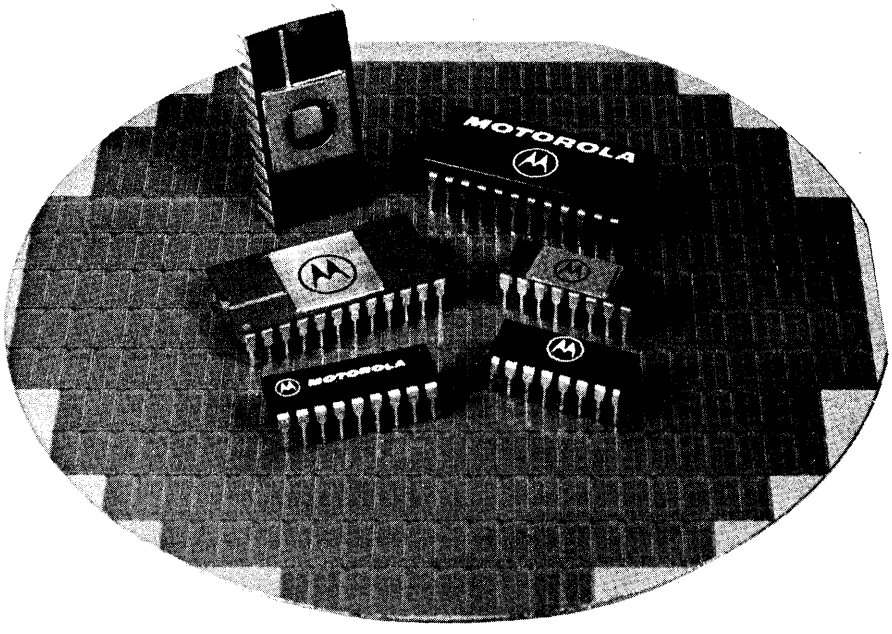
BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground



MOS EPROMs

MOTOROLA

MCM68764

64K-BIT UV ERASABLE PROM

The MCM68764 is a 65,536-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically, or for replacing 64K ROMs for fast turnaround time. The transparent window on the package allows the memory content to be erased with ultraviolet light.

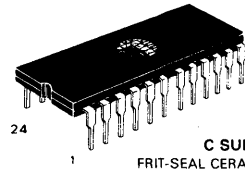
For ease of use, the device operates from a single power supply and has a static power-down mode. Pin-for-pin mask programmable ROMs are available for large volume production runs of systems initially using the MCM68764.

- Single +5 V Power Supply
- Automatic Power-down Mode (Standby) with Chip Enable
- Organized as 8192 Bytes of 8 Bits
- Low Power Dissipation
  - 85 mA Active Maximum
  - 20 mA Standby Maximum
- Fully TTL Compatible
- Maximum Access Time = 450 ns MCM68764
  - 350 ns MCM68764-35
- Standard 24-Pin DIP for EPROM Upgradability
- Pin Compatible to MCM68365 Mask Programmable ROM
- Fast Programming Algorithm Possible

MOS

(N-CHANNEL, SILICON-GATE)

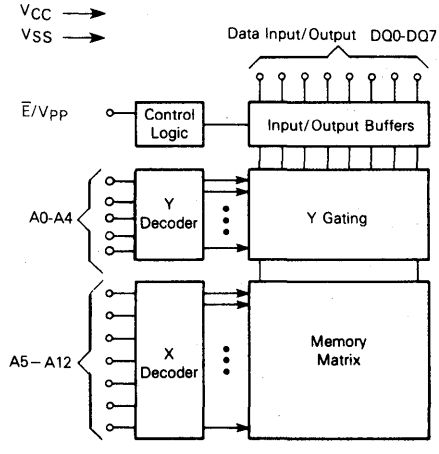
8192 × 8-BIT UV ERASABLE PROGRAMMABLE READ ONLY MEMORY



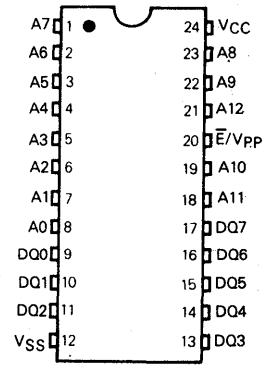
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623A

EPROM

BLOCK DIAGRAM



PIN ASSIGNMENT



Pin Names	
A	Address
DQ	Data Input/Output
E/VPP	Chip Enable/Program
VCC	+5 V
VSS	Ground

DS-9815-R3

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Operating Temperature Range	0 to +70	°C
Storage Temperature	−65 to +125	°C
All Input or Output Voltages with Respect to V_{SS}	+6 to −0.3	V
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to −0.3	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

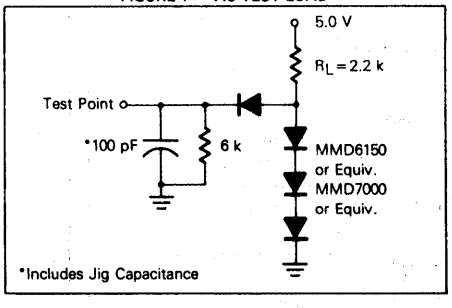
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MODE SELECTION

Mode	Pin Number			
	9-11, 13-17, DQ	12 V_{SS}	20 $\overline{E}/V_{PP}$	24 V_{CC}
Read	Data out	V_{SS}	V_{IL}	V_{CC}
Output Disable	High-Z	V_{SS}	V_{IH}	V_{CC}
Standby	High-Z	V_{SS}	V_{IH}	V_{CC}
Program	Data in	V_{SS}	Pulsed V_{ILP} to V_{IHP}	V_{CC}

EPROM

FIGURE 1 — AC TEST LOAD



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V) Except $\overline{E}/V_{PP}$	C_{in}	4.0	6.0	pF
Input Capacitance $\overline{E}/V_{PP}$	C_{in}	60	100	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

RECOMMENDED DC OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage	MCM68764C, MCM68764C35	V_{CC}	4.75	5.0	5.25	V
Input High Voltage		V_{IH}	2.0	–	V_{CC} + 1.0	V
Input Low Voltage		V_{IL}	−0.1	–	0.8	V

DC OPERATING CHARACTERISTICS

Characteristic	Condition	Symbol	MCM68764			Units
			Min	Typ	Max	
Address Input Sink Current	V_{in} = 5.25 V	I_{in}	–	–	10	μA
Output Leakage Current	V_{out} = 5.25 V	I_{LO}	–	–	10	μA
$\overline{E}/V_{PP}$ Input Sink Current	$\overline{E}/V_{PP}$ = 0.4	I_{EL}	–	–	100	μA
	$\overline{E}/V_{PP}$ = 2.4	$I_{EH} = I_{PL}$	–	–	100	μA
V_{CC} Supply Current (Standby, Outputs Open)	$\overline{E}/V_{PP} = V_{IH}$	I_{CC1}	–	–	20	mA
V_{CC} Supply Current (Active, Outputs Open).	$\overline{E}/V_{PP} = V_{IL}$	I_{CC2}	–	–	85	mA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}	–	–	0.45	V
Output High Voltage	I_{OH} = −400 μA	V_{OH}	2.4	–	–	V

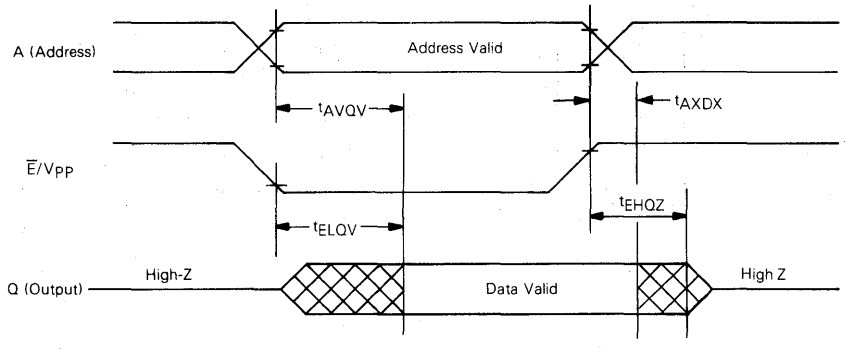
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels ..... 0.8 Volt and 2.2 Volts
Input Rise and Fall Times ..... 20 ns
Input Timing Levels ..... 1.0 Volt and 2.0 Volts
Output Timing Levels ..... 0.8 Volt and 2.0 Volts
Output Load ..... See Figure 1

Characteristic	Symbol		MCM68764C35		MCM68764C		Units
	Standard	Alternate	Min	Max	Min	Max	
Addres Valid to Output Valid ($\overline{E} = V_{IL}$)	t_{AVQV}	t_{ACC}	–	350	–	450	ns
Chip Enable to Output Valid	t_{ELQV}	t_{CE}	–	350	–	450	ns
Chip Disable to Output High Z	t_{EHQZ}	t_{DF}	0	100	0	100	ns
Data Hold from Address ($\overline{E} = V_{IL}$)	t_{AXDX}	t_{OH}	0	–	0	–	ns

READ MODE TIMING DIAGRAM



EPROM

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

($T_A = 25 \pm 5°C$)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Voltage for All Addresses and Data	V_{IH}	2.2	–	V_{CC} + 1	V
Input Low Voltage for All Addresses and Data	V_{IL}	−0.1	–	0.8	V
Program Pulse Input High Voltage	V_{IHP}	24	25	26	V
Program Pulse Input Low Voltage	V_{ILP}	2.0	V_{CC}	6.0	V

PROGRAMMING OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	V_{in} = 5.25 V	I_{LI}	–	–	10	μA
V_{PP} Program Pulse Supply Current (V_{PP} = 25 V ± 1 V)	–	I_{PH}	–	–	30	mA
V_{PP} Supply Current (V_{PP} = 2.4 V)	–	I_{PL} = I_{EH}	–	–	100	μA
V_{CC} Supply Current (V_{PP} = 5.0 V)	–	I_{CC}	–	–	85	mA

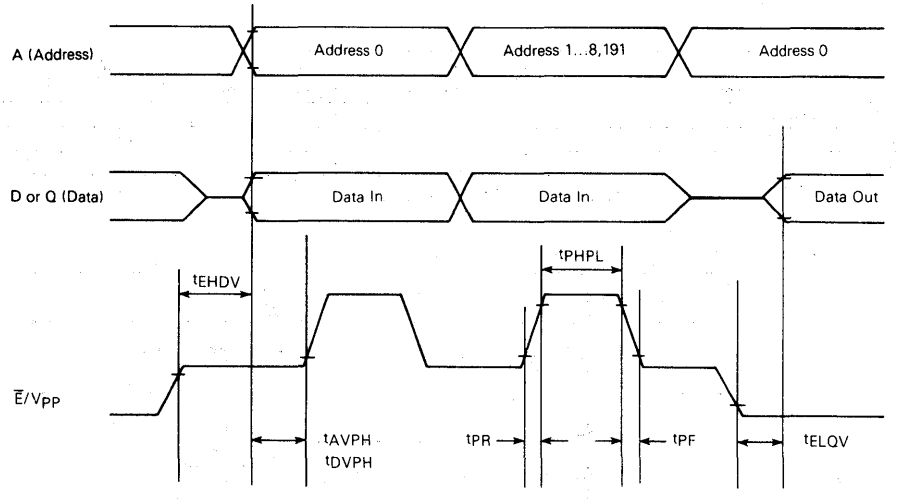
AC PROGRAMMING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol		Min	Max	Unit
	Standard	Alternate			
Address Setup Time	t_{AVPH}	t_{AS}	2.0	–	μs
Data Setup Time	t_{DVPH}	t_{DS}	2.0	–	μs
Chip Enable to Valid Data	t_{ELQV}	t_{CE}	450	–	ns
Chip Disable to Data In	t_{EHDV}	t_{CDD}	2.0	–	μs
Program Pulse Width	t_{PHPL}	t_{PW}	1.9	2.1	ms
Program Pulse Rise Time	t_{PR}	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	t_{PF}	0.5	2.0	μs
Cumulative Programming Time Per Word*	t_{CP}	t_{CP}	12	50	ms

*If less than 25 two millisecond pulses are required to verify programming, then 5 additional two millisecond pulses are required to ensure proper operating margins (i.e., 2 ms + 5 × 2 ms = 12 ms minimum t_{CP}).

EPROM

PROGRAMMING OPERATION TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

Before programming, the memory should be submitted to a full erase operation to ensure that every bit is in the "1" state (represented by Output High). Data is entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet erasure.

To set the memory up for Program Mode, the $\overline{E}/V_{PP}$ input (Pin 20) should be between +2.0 and +6.0 V, which will three-state the outputs and allow data to be setup on the DQ terminals. The V_{CC} voltage is the same as for the Read operation. Only "0's" will be programmed when "0's" and "1's" are entered in the 8-bit data word.

After address and data setup, 25-volt programming pulse (V_{IH} to V_{IHP}) is applied to the $\overline{E}/V_{PP}$ input. The program pulse width is 2 ms and the maximum program pulse amplitude is 26 V.

Multiple MCM68764s may be programmed in parallel by connecting like inputs and applying the program pulse to the $\overline{E}/V_{PP}$ inputs. Different data may be programmed into multiple MCM68764s connected in parallel by selectively applying the programming pulse only to the MCM68764s to be programmed.

READ OPERATION

After access time, data is valid at the outputs in the Read mode. A single input ($\overline{E}/V_{PP}$) enables the outputs and puts the chip in active or standby mode. With $\overline{E}/V_{PP}$ = "0" the outputs are enabled and the chip is in active mode; with $\overline{E}/V_{PP}$ = "1" the outputs are three-stated and the chip is in standby mode. During standby mode, the power dissipation is reduced.

Multiple MCM68764s may share a common data bus with like outputs OR-tied together. In this configuration, only one $\overline{E}/V_{PP}$ input should be low and no other device outputs should be active on the same bus. This will prevent data contention on the bus.

ERASING INSRUCTIONS

The MCM68764 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 angstroms. The recommended integrated dose (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM68764 should be positioned about one inch away from the UV-tubes.

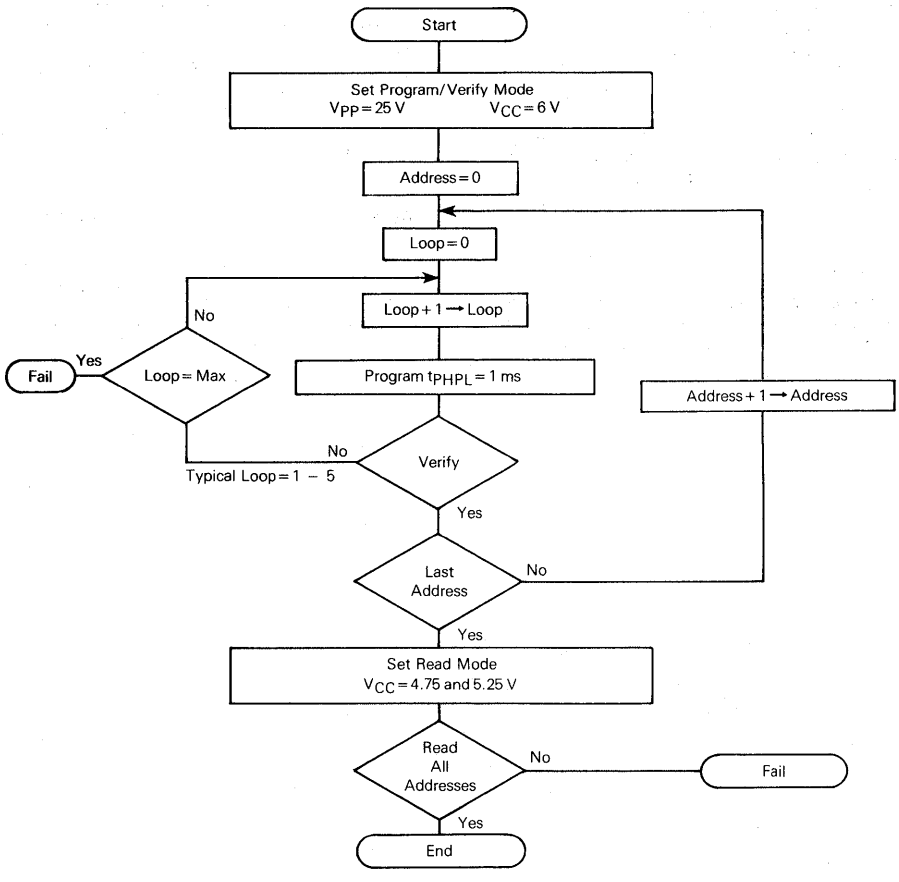
RECOMMENDED OPERATING PROCEDURES

After erasure and reprogramming of the EPROM, it is recommended that the quartz window be covered with an opaque self-adhesive cover. It is important that the self-adhesive cover not leave any residue on the quartz if it is removed to allow another erasure.

FAST PROGRAMMING ALGORITHM

This device is capable of the fast programming algorithm as shown by the following flow chart. This algorithm allows for faster programming time with increased operating margins and improved reliability of data storage.

FAST PROGRAMMING ALGORITHM FLOW CHART



MOTOROLA

MCM68766

8192 × 8-BIT UV ERASABLE PROM

The MCM68766 is a 65,536-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically, or for replacing 64K ROMs for fast turnaround time. The transparent window on the package allows the memory content to be erased with ultraviolet light.

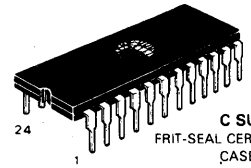
For ease of use, the device operates from a single power supply that has an output enable control and is pin-for-pin compatible with the MCM68366 mask programmable ROMs, which are available for large volume production runs of systems initially using the MCM68766.

- Single +5 V Power Supply
- Organized as 8192 Bytes of 8 Bits
- Fully TTL Compatible
- Maximum Access Time = 450 ns MCM68766
  400 ns MCM68766-40
  350 ns MCM68766-35
  300 ns MCM68766-30
- Standard 24-Pin DIP for EPROM Upgradability
- Pin Compatible to MCM68366 Mask Programmable ROM
- Low Power Dissipation — 85 mA Active Maximum
- Fast Programming Algorithm Possible

MOS

(N-CHANNEL, SILICON-GATE)

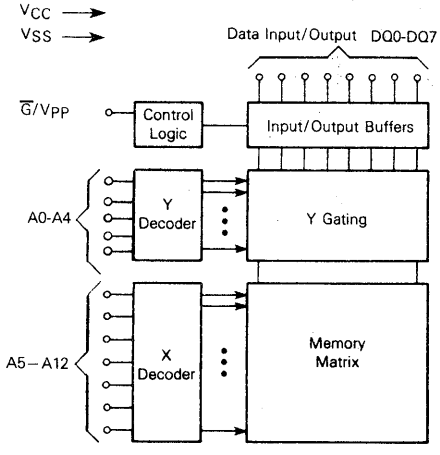
8192 × 8-BIT UV ERASABLE PROGRAMMABLE READ ONLY MEMORY



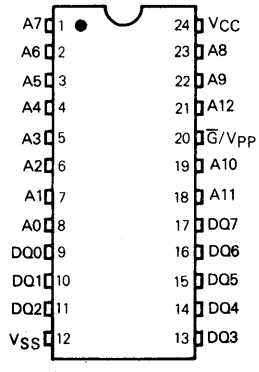
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623A

EPROM

BLOCK DIAGRAM



PIN ASSIGNMENT



Pin Names	
A	Address
DQ	Data Input/Output
G/VPP	Output Enable/Program
VCC	+5 V Power Supply
VSS	Ground

ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Operating Temperature Range	0 to +70	°C
Storage Temperature	−65 to +125	°C
All Input or Output Voltages with Respect to V_{SS}	+6 to −0.3	Vdc
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to −0.3	Vdc

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

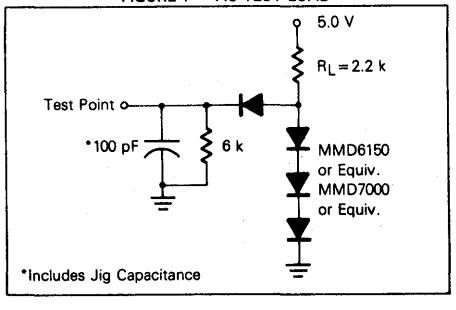
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MODE SELECTION

Mode	Pin Number			
	9-11, 13-17, DQ	12 V_{SS}	20 $\overline{G}/V_{PP}$	24 V_{CC}
Read	Data Out	V_{SS}	V_{IL}	V_{CC}
Output Disable	High-Z	V_{SS}	V_{IH}	V_{CC}
Program	Data In	V_{SS}	Pulsed V_{ILP} to V_{IHP}	V_{CC}

EPROM

FIGURE 1 — AC TEST LOAD



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V) Except $\overline{G}/V_{PP}$	C_{in}	4.0	6.0	pF
Input Capacitance ($\overline{G}/V_{PP}$)	C_{in}	60	100	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

RECOMMENDED DC OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage	MCM68766C, C35, C40	V_{CC}	4.75	5.0	5.25	V
	MCM68766C30-10, C35-10		4.50	5.0	5.50	
Input High Voltage		V_{IH}	2.0	–	V_{CC} + 1.0	V
Input Low Voltage		V_{IL}	−0.1	–	0.8	V

DC OPERATING CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Units
Address Input Sink Current	V_{in} = 5.25 V	I_{in}	–	–	10	μA
Output Leakage Current	V_{out} = 5.25 V	I_{LO}	–	–	10	μA
$\overline{G}/V_{PP}$ Input Sink Current	$\overline{G}/V_{PP}$ = 0.4 V	I_{GL}	–	–	100	μA
	$\overline{G}/V_{PP}$ = 2.4 V	$I_{GH} = I_{PL}$	–	–	100	μA
V_{CC} Supply Current (Outputs Open)	$\overline{G}/V_{PP} = V_{IL}$	I_{CC}	–	–	85	mA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}	–	–	0.45	V
Output High Voltage	I_{OH} = −400 μA	V_{OH}	2.4	–	–	V

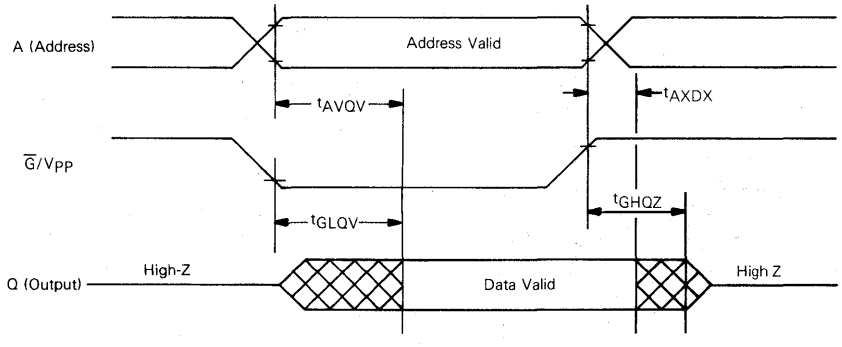
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels.....0.8 Volt and 2.2 Volts
Input Rise and Fall Times.....20 ns
Input Timing Levels.....1.0 Volt and 2.0 Volts
Output Timing Levels.....0.8 Volt and 2.0 Volts
Output Load.....See Figure 1

Characteristic	Symbol		MCM68766C 30		MCM68766C 35		MCM68766C 40		MCM68766C		Units
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max	
Address Valid to Output Valid ($\overline{G} = V_{IL}$)	t_{AVQV}	t_{ACC}	–	300	–	350	–	400	–	450	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}	–	120	–	150	–	150	–	150	ns
Output Disable to Output High Z	t_{GHQZ}	t_{DF}	0	100	0	100	0	100	0	100	ns
Data Hold from Address ($\overline{G} = V_{IL}$)	t_{AXDX}	t_{OH}	0	–	0	–	0	–	0	–	ns

READ MODE TIMING DIAGRAM



EPROM

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

($T_A = 25 \pm 5°C$)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Voltage for All Addresses and Data	V_{IH}	2.2	–	V_{CC} + 1	V
Input Low Voltage for All Addresses and Data	V_{IL}	−0.1	–	0.8	V
Program Pulse Input High Voltage	V_{IHP}	24	25	26	V
Program Pulse Input Low Voltage	V_{ILP}	2.0	V_{CC}	6.0	V

PROGRAMMING OPERATION DC CHARACTERISTICS

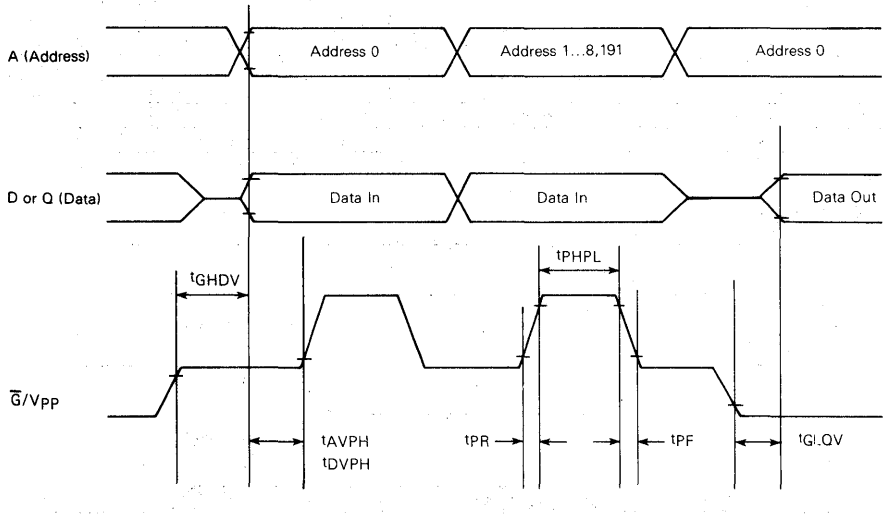
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	V_{in} = 5.25 V	I_{LI}	–	–	10	μA
V_{PP} Program Pulse Supply Current (V_{PP} = 25 V ±1 V)	–	I_{PH}	–	–	30	mA
V_{PP} Supply Current (V_{PP} = 2.4 V)	–	I_{PL} = I_{GH}	–	–	100	μA
V_{CC} Supply Current (V_{PP} = 5 V)	–	I_{CC}	–	–	85	mA

AC PROGRAMMING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol		Min	Max	Unit
	Standard	Alternate			
Address Setup Time	t_{AVPH}	t_{AS}	2.0	–	μs
Data Setup Time	t_{DVPH}	t_{DS}	2.0	–	μs
Output Enable to Valid Data	t_{GLQV}	t_{OE}	150	–	ns
Output Disable to Data In	t_{GHDV}	t_{ODD}	2.0	–	μs
Program Pulse Width	t_{PHPL}	t_{PW}	1.9	2.1	ms
Program Pulse Rise Time	t_{PR}	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	t_{PF}	0.5	2.0	μs
Cumulative Programming Time Per Word*	t_{CP}	t_{CP}	12	50	ms

*If less than 25, two-millisecond pulses are required to verify programming then 5 additional two-millisecond pulses are required to ensure proper operating margins (i.e., 2 ms + 5 × 2 ms = 12 ms minimum t_{CP}).

PROGRAMMING OPERATION TIMING DIAGRAM



EPROM

PROGRAMMING INSTRUCTIONS

Before programming, the memory should be submitted to a full erase operation to ensure that every bit is in the "1" state (represented by Output High). Data is entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for Program Mode, the $\overline{G}/V_{PP}$ input (Pin 20) should be between +2.0 and +6.0 V, which will three-state the outputs and allow data to be set up on the DQ terminals. The V_{CC} voltage is the same as for the Read operation. Only "0's" will be programmed when "0's" and "1's" are entered in the 8-bit data word.

After address and data setup, 25-volt programming pulse (V_{IH} to V_{IHP}) is applied to the $\overline{G}/V_{PP}$ input. The program pulse width is 2 ms and the maximum program pulse amplitude is 26 V.

Multiple MCM68766s may be programmed in parallel by connecting like inputs and applying the program pulse to the $\overline{G}/V_{PP}$ inputs. Different data may be programmed into multiple MCM68766s connected in parallel by selectively applying the programming pulse only to the MCM68766s to be programmed.

READ OPERATION

After access time, data is valid at the outputs in the Read mode. With $\overline{G}/V_{PP}$ = "0" the outputs are enabled; with $\overline{G}/V_{PP}$ = "1" the outputs are three-stated.

Multiple MCM68766s may share a common data bus with like outputs OR-tied together. In this configuration only one $\overline{G}/V_{PP}$ input should be low and no other device outputs should be active on the same bus. This will prevent data contention on the bus.

ERASING INSRUCTIONS

The MCM68766 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 angstroms. The recommended integrated dose (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM68766 should be positioned about one inch away from the UV-tubes.

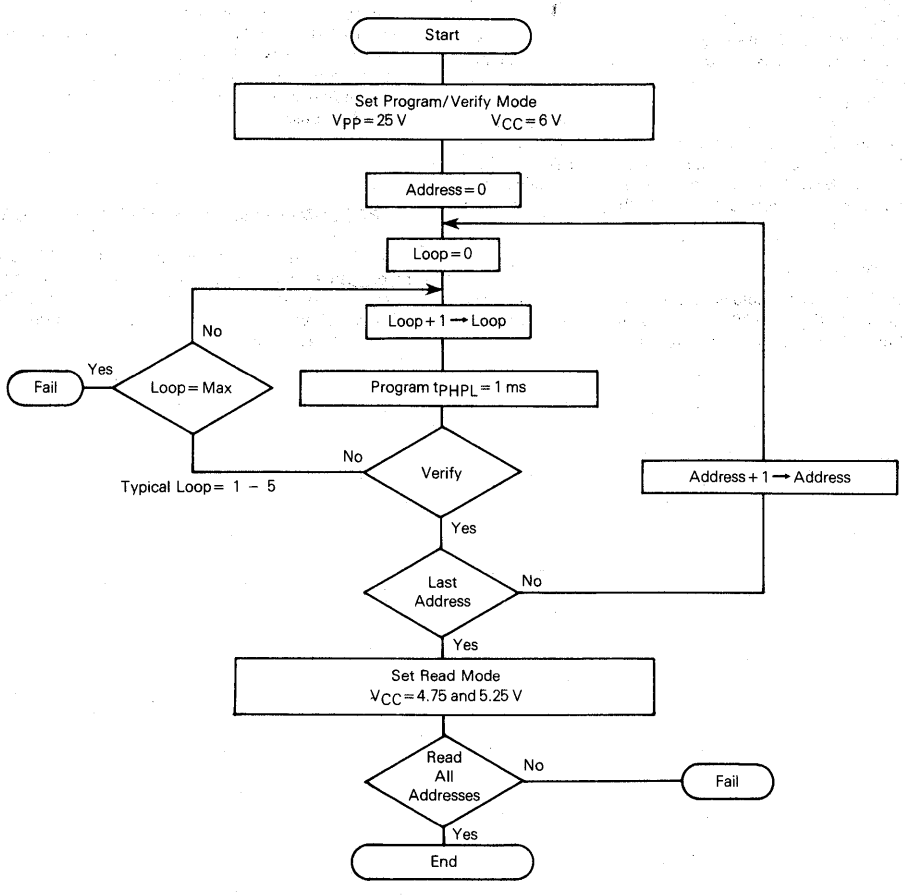
RECOMMENDED OPERATING PROCEDURES

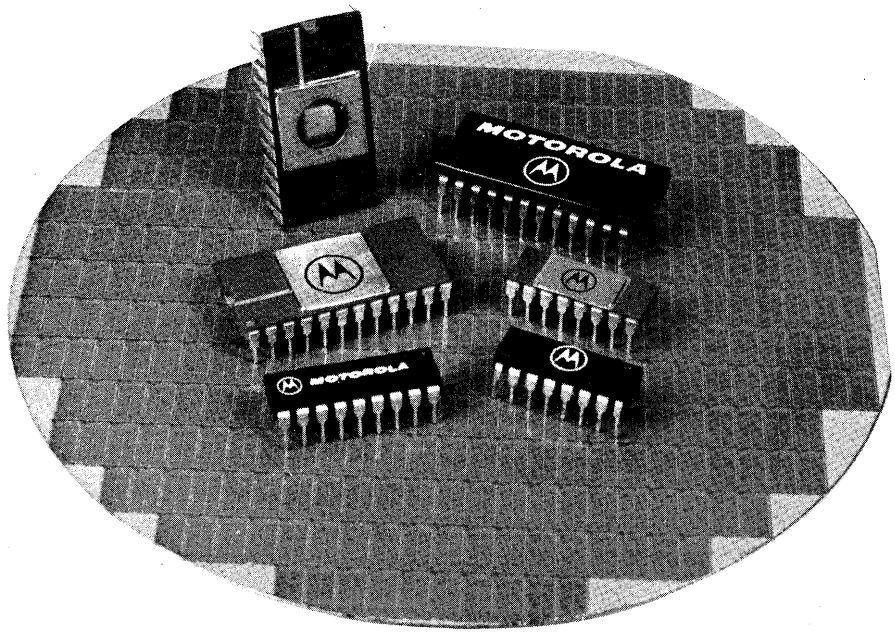
After erasure and reprogramming of the EPROM, it is recommended that the quartz window be covered with an opaque self-adhesive cover. It is important that the self-adhesive cover not leave any residue on the quartz if it is removed to allow another erasure.

FAST PROGRAMMING ALGORITHM

This device is capable of the fast programming algorithm as shown by the following flow chart. This algorithm allows for faster programming time with increased operating margins and improved reliability of data storage.

FAST PROGRAMMING ALGORITHM FLOW CHART





MOS EEPROMs

EEPROM

MOTOROLA

MCM2833

Product Preview

32K-BIT ELECTRICALLY ERASABLE PROM

The MCM2833 is a 32,768-bit Electrically Erasable Programmable Read Only Memory (E^2PROM) designed for handling data in applications requiring both nonvolatile memory and in-system reprogramming.

The MCM2833 saves time and money because of the in-system erase and reprogram capability. The device operates from a single +5 V power supply in the read, write, and erase mode. Word erase and write can be controlled entirely by TTL signal levels.

To ease system design, the high voltage needed by the device for write and erase cycles is generated internally.

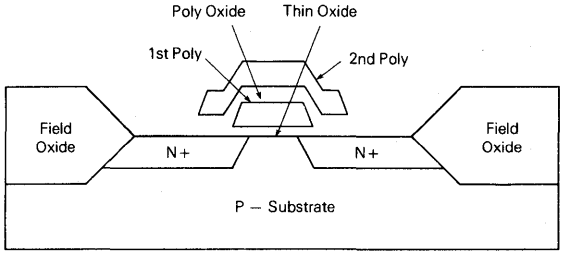
Another ease-of-use feature is the choice of erase modes (bulk, byte, row, or column) to optimize system erase/write time. For microprocessor compatibility, on-chip latches are provided for addresses, data, and controls, allowing the microprocessor to perform other tasks while the MCM2833 is erasing or programming (writing) itself.

The MCM2833 is fabricated using Motorola's FETMOS technology (Floating-gate Electron Tunneling MOS), which has the advantages of good data retention, good endurance, and conventional processing.

The device pinout is part of Motorola's industry standard byte wide Nonvolatile Memory family, providing cost-effective density upgrades.

- Single +5 V Power Supply
- Organized as 4096 Bytes of 8 Bits
- Fast Access Time of 150 ns (MCM2833-15) and 200 ns (MCM2833-20)
- Low Power Dissipation
  125 mA Maximum (Active)
  35 mA Maximum (Standby)
- In-System Automatic Erase/Write Capability
- Data Protected During Power-Up and Power-Down
- 10,000 Erase/Program Cycles per Byte
- Data Integrity of 10 Years
- 9 ms for Byte Erase or Write
- Latched Address, Data, and Controls for Write/Erase
- Chip Enable and Output Enable for Two Line Bus Control
- 28-Pin JEDEC Standard Pinout

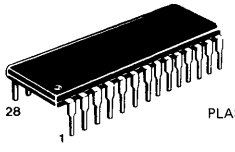
FETMOS
(Floating-Gate Electron Tunneling MOS)



HMOS

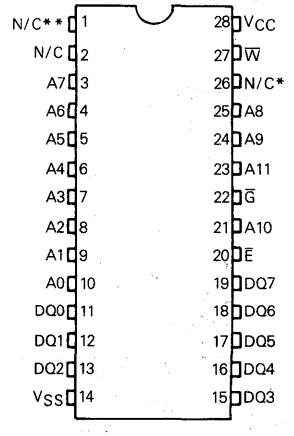
(N-CHANNEL, SILICON GATE)

4096 × 8-BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT



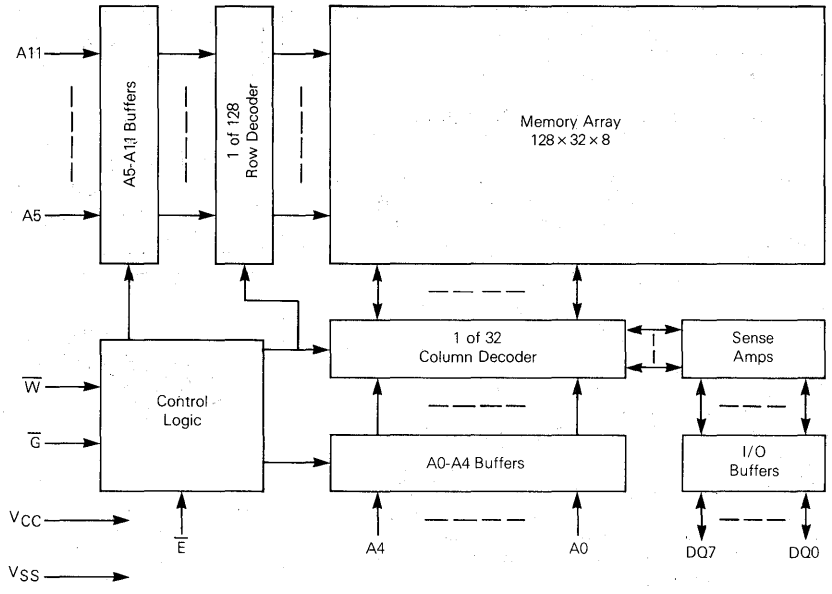
*For normal operation, pin 26 can be tied to V_{SS} or left floating.
**For normal operation, pin 1 can be tied to V_{SS} or V_{CC}.

PIN NAMES	
A	Address
DQ	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
N/C	No Connect
V_{CC}	+5 V Power Supply
V_{SS}	Ground

EEPROM

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MCM2833 BLOCK DIAGRAM



MODE SELECTION

	Mode	Pin Number and Function				Notes
		Pin 11-13 15-19 DQ0-DQ7	Pin 20 $\overline{E}$	Pin 22 $\overline{G}$	Pin 27 $\overline{W}$	
	Read	Data Out	V_{IL}	V_{IL}	V_{IH}	–
	Standby	High Z	V_{IH}	Don't Care	Don't Care	–
	Output Disable	High Z	V_{IL}	V_{IH}	V_{IH}	–
	Write	Data In	V_{IL}	V_{IH}	V_{IL}	–
	Write or Erase Inhibit	High Z	V_{IH}	Don't Care	Don't Care	–
	Word Erase (I)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	–
Special Modes	Word Erase (II)	V_{IH}	V_{IL}	V_{IH}	V_{IHH}	–
Special Modes	Page Erase (Row)	V_{IH}	V_{IL}	V_{IHH}	V_{IHH}	1
Special Modes	Page Erase (Column)	V_{IH}	V_{IL}	V_{IHH}	V_{IH}	2
Special Modes	Bulk Erase	V_{IH}	V_{IL}	V_{IHH}	V_{IL}	–

V_{IHH} = 11 V to 17 V

NOTES:
1. Row Page Erase Mode: There are 128 rows containing 32 bytes each. Individual rows are selected with addresses A5-A11 (A0-A4 are don't care).
2. Column Page Erase Mode: There are 32 columns containing 128 bytes each. Individual columns are selected with addresses A0-A4 (A5-A11 are don't care).

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Operating Temperature Range	0 to +70	°C
Storage Temperature	−65 to +100	°C
Input or Output Voltages with Respect to V_{SS} (Except $\overline{G}$, $\overline{W}$)	+6 to −0.4	V
Input Voltages with Respect to V_{SS} for $\overline{G}$ and $\overline{W}$	18 to −0.4	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

RECOMMENDED DC OPERATING CONDITIONS READ, WRITE, OR ERASE

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage	MCM2833-15, -20	V_{CC}	4.50	5.0	5.50	V
	MCM2833-15-5, -20-5	V_{CC}	4.75	5.0	5.25	V
Input High Voltage		V_{IH}	2.0	–	6.0	V
	($\overline{G}$ Pin 22 and $\overline{W}$ Pin 27)	V_{IHH}	11.0	–	17.0	V
Input Low Voltage*		V_{IL}	−0.1	–	0.8	V

*The device will withstand undershoots to the −0.4 V level for a maximum duration of 10 ns.

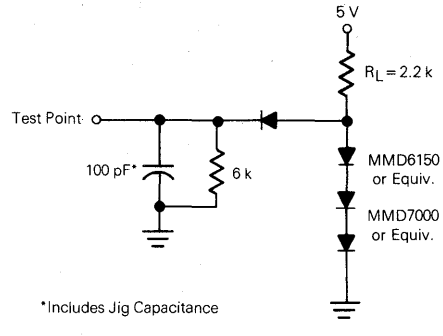
DC OPERATING CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current (A0-A11, $\overline{E}$)	$V_{in} = V_{CC}$ Max	I_{in1}	–	–	10	μA
Input Leakage Current ($\overline{G}$,$\overline{W}$)	$V_{in} = 17$ V	I_{in2}	–	–	10	μA
Output Leakage Current DQ0-DQ7)	$V_{out} = V_{CC}$ Max, $\overline{G} = V_{IH}$	I_{LO1}	–	–	10	μA
Output Leakage Current (DQ0-DQ7)	$V_{out} = 0.4$ V, $\overline{G} = V_{IH}$	I_{LO2}	–	–	10	μA
V_{CC} Supply Current, Standby	$\overline{E} = V_{IH}$, $\overline{G} = V_{IL}$	I_{CC1}	–	–	35	mA
V_{CC} Supply Current, Active (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{W} = V_{IH}$	I_{CC2}	–	–	120	mA
V_{CC} Supply Current, Active (Erase/Write)	See Mode Selection Table	I_{CC3}	–	–	130	mA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}	–	–	0.4	V
Output High Voltage	I_{OH} = −400 μA	V_{OH}	2.4	–	–	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	5	10	pF
Output Capacitance	C_{out}	–	10	pF

FIGURE 1 — AC TEST LOAD



EEPROM

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

AC Test Conditions

Input Transition Times: 5 ns ≤ $t_r = t_f$ ≤ 10 ns
Input Pulse Transition Levels: 0.45 Volts (V_{IL}) to 2.4 Volts (V_{IH})
Output Load: See Figure 1

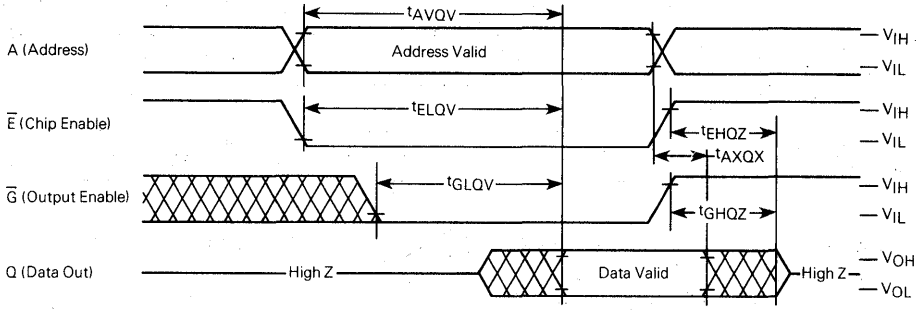
Test Timing Measurement
Reference Levels ..... Input 1 V and 2 V
Output 0.8 V and 2 V

READ OPERATION ($\overline{W} = V_{IH}$)

Parameter	Condition	Symbol	MCM2833-15		MCM2833-20		Unit	Notes
			Min	Max	Min	Max		
Address Valid to Output Valid (Address Access Time)	$\overline{E} = \overline{G} = V_{IL}$	t_{AVQV}	–	150	–	200	ns	–
Output Enable to Output Valid (Output Enable Access Time)		t_{GLQV}	–	70	–	75	ns	–
Chip Enable to Output Valid (Chip Enable Access Time)		t_{ELQV}	–	150	–	200	ns	–
Output Disable to Output High Z	$\overline{E} = V_{IL}$	t_{GHQZ}	0	60	0	60	ns	3
Chip Disable to Output High Z	$\overline{G} = V_{IL}$	t_{EHQZ}	0	60	0	60	ns	3
Address Invalid to Output Invalid		t_{AXQV}	0	–	0	–	ns	–

NOTE:
3. The parameters t_{GHQZ} and t_{EHQZ} may define the time at which the outputs achieve the open or High Z state and are not referenced to a level.

READ MODE TIMING DIAGRAM

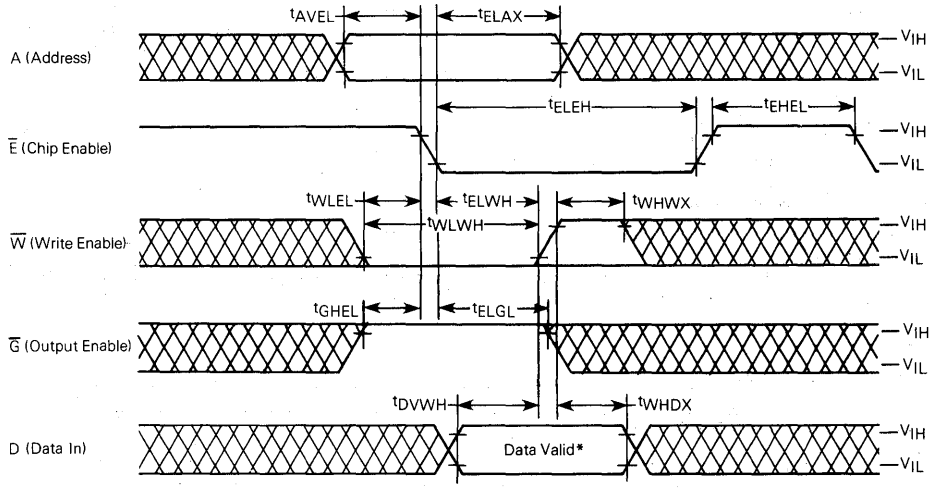


EEPROM

AC WRITE OR ERASE CHARACTERISTICS [$\overline{G} = V_{IH}$ During Write or Word Erase (I)]

Parameter		Symbol	Min	Max	Unit
Address Valid to Chip Enable (Address Setup Time)		t_{AVEL}	0	–	ns
Write Enable to Chip Enable		t_{WLEL}	0	–	ns
Chip Enable to Address Don't Care		t_{ELAX}	150	–	ns
Write High to Data Don't Care		t_{WHDX}	20	–	ns
Data Valid to Write High		t_{DVWH}	100	–	ns
Write Enable Pulse Width		t_{WLWH}	150	–	ns
Write Enable Hold Time		t_{ELWH}	150	–	ns
Chip Disable to Chip Enable (Enable Latch Setup Time)		t_{EHEL}	350	–	ns
Write or Erase Time	(MCM2833-15, -20)	t_{ELEH}	9	25	ms
(Chip Enable Pulse Width)	(MCM2833-15-5, -20-5)	t_{ELEH}	25	50	ms
Data Latch Time		t_{WHWX}	50	–	ns
Output Enable to Chip Enable		t_{GHEL}	0	–	ns
Output Enable Hold Time		t_{ELGL}	150	–	ns

WORD ERASE (I) OR WRITE WAVEFORMS



*Data in during Word Erase (I) (DQ0-DQ7) = V_{IH}

EEPROM

FUNCTIONAL DESCRIPTION

All inputs for the operating modes are TTL levels with the exception of bulk and page erase.

READ MODE

The MCM2833 uses 2-line control architecture for read operation to avoid bus contention problems. Data is available at the Data outputs of the selected device at t_{AVQV} with Chip Enable ($\overline{E}$), and Output Enable ($\overline{G}$) at V_{IL} or, at t_{GLQV} with Chip Enabled ($\overline{E}$), and address stable. In the read mode the device can be accessed similar to a static RAM. This can be done by holding Chip Enable active low and supplying the next address locations in a ripple through fashion with the next access determined by t_{AVQV}. The outputs of two or more EEPROMs may be Or-tied to the same data bus. Only one EEPROM should have its outputs selected to prevent data bus contention between two devices in this configuration. The outputs of other EEPROMs should be deselected with the Output Enable ($\overline{G}$) or Chip Enable ($\overline{E}$) input at a high TTL level.

STANDBY MODE

The Standby mode of the MCM2833 is achieved by applying a TTL high signal (V_{IH}) to Chip Enable ($\overline{E}$) input. When the device is in the Standby mode, the outputs are in the high impedance state, independent of the Output Enable ($\overline{G}$) input. When the MCM2833 is placed in the Standby mode, the active power dissipation is reduced by 72%.

WRITE OR ERASE

After each erasure, all bits of the selected byte(s) are in the "1" state. Data is introduced by selectively programming (writing) "0s" into the desired bit locations. Although only "0s" will be programmed (written), both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by electrical erasure.

Write or Erase Mode selection is controlled by applying the required sequence of signals to the device. The Output Enable ($\overline{G}$), Write Enable ($\overline{W}$), and A0-A11 address inputs are latched on the falling edge of Chip Enable ($\overline{E}$). DQ0-DQ7 are latched on the rising edge of Write Enable ($\overline{W}$). To enter new address, control ($\overline{G}$ and $\overline{W}$), and/or data, the Chip Enable ($\overline{E}$) signal must be clocked to V_{IH} for >350 ns (t_{EHEL}), otherwise, the previous address and data may stay latched and inhibit the entry of the new information.

WRITE OR ERASE INHIBIT

Programming (writing) or erasure of multiple EEPROMs in parallel is easily accomplished. Except for Chip Enable ($\overline{E}$), all like inputs of the parallel devices may be common. A high level on the Chip Enable ($\overline{E}$) input inhibits the EEPROM from being programmed (written) or erased.

WRITE OR ERASE VERIFY

To determine that the word(s) was correctly programmed (written) or erased, a normal read operation can be performed. A read following after a write or erase cycle will require that Chip Enable ($\overline{E}$) goes to V_{IH} and is held for >350 ns (t_{EHEL}) and that Write Enable ($\overline{W}$) is at a "1" and Output Enable ($\overline{G}$) at a "0" when Chip Enable ($\overline{E}$) goes to V_{IL} at the beginning of a read cycle. The data addressed will be valid on output lines at t_{ELQV} access time after Chip Enable ($\overline{E}$) goes low.

EEPROM

AC CHARACTERISTICS, SPECIAL ERASE MODE

Mode		Symbol	Min	Max	Unit
Address Valid to Chip Enable (Address Setup Time)		t_{AVEL}	0	–	ns
Output Disable to Chip Enable		t_{GHEL}	0	–	ns
Data Valid to Chip Enable		t_{DHEL}	0	–	ns
Write Enable to Chip Enable		t_{WLEL}	0	–	ns
Chip Enable to Address Don't Care		t_{ELAX}	150	–	ns
Chip Enable to Output Enable Don't Care		t_{ELGX}	150	–	ns
Chip Enable to Data In Don't Care		t_{ELDX}	150	–	ns
Chip Enable to Write Enable Don't Care		t_{ELWX}	150	–	ns
Chip Disable to Chip Enable (Enable Latch Setup Time)		t_{EHEL}	350	–	ns
Write or Erase Time	(MCM2833-15, -20)	t_{ELEH}	9	25	ms
(Chip Enable Pulse Width)	(MCM2833-15-5, -20-5)	t_{ELEH}	25	50	ms
Write Disable to Chip Enable		t_{WHEL}	0	–	ns
Data Latch Time		t_{WHWX}	50	–	ns
Data In High to Write High		t_{DHWH}	100	–	ns
Write High to Data Don't Care		t_{WHDX}	20	–	ns

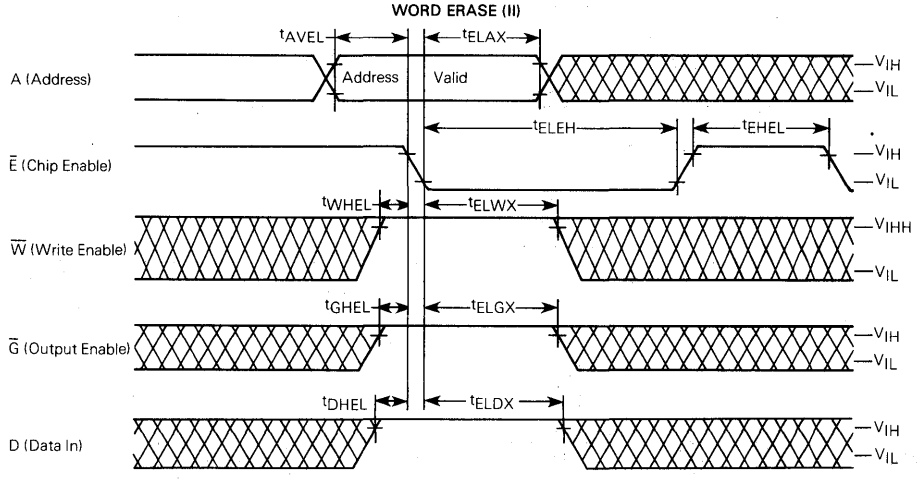
SPECIAL MODE SECTION

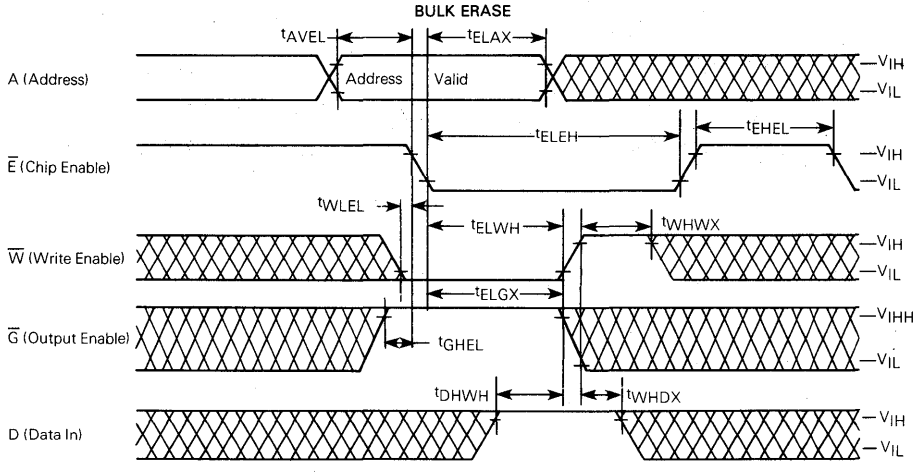
SPECIAL MODE SELECTIONS (V_{IHH} = 11 V to 17 V)

Special Modes	Pin Number and Function				Notes
	11-13, 15-19 DQ0-DQ7	Pin 20 $\overline{E}$	Pin 22 $\overline{G}$	Pin 27 $\overline{W}$	
Word Erase (II)	V_{IH}	V_{IL}	V_{IH}	V_{IHH}	–
Page Erase (Row)	V_{IH}	V_{IL}	V_{IHH}	V_{IHH}	4
Page Erase (Column)	V_{IH}	V_{IL}	V_{IHH}	V_{IH}	5
Bulk Erase	V_{IH}	V_{IL}	V_{IHH}	V_{IL}	–

NOTES:

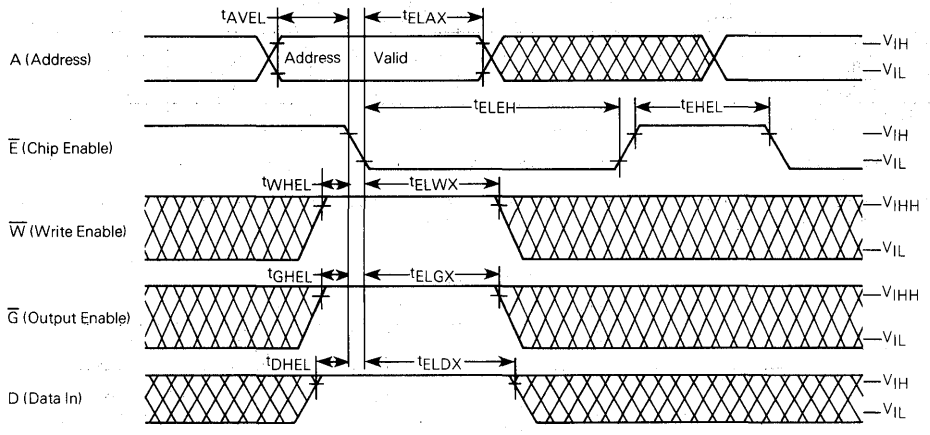
4. Row Page Erase Mode: There are 128 rows containing 32 bytes each. Individual rows are selected with addresses A5-A11 (A0-A4 are don't care).
5. Column Page Erase Mode: There are 32 columns containing 128 bytes each. Individual columns are selected with addresses A0-A4 (A5-A11 are don't care).



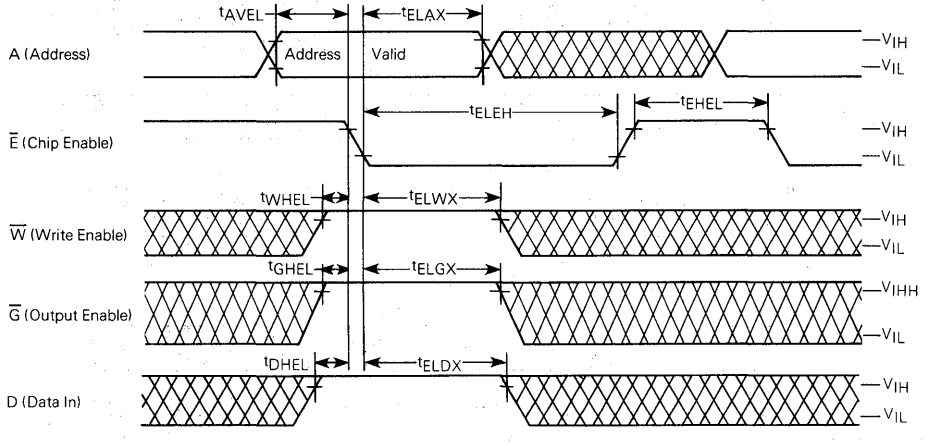


EEPROM

ROW PAGE ERASE
(A0-A4 = Don't Care)



COLUMN PAGE ERASE
(A5-A11 = Don't Care)



EEPROM

MOTOROLA

MCM2864

Product Preview

SMART 64K-BIT ELECTRICALLY ERASABLE PROM

The MCM2864 is a 65,536-bit Smart Electrically Erasable Programmable Read Only Memory (E^2PROM) designed for handling data in applications requiring both nonvolatile memory and in-system reprogramming.

The MCM2864 improves processor throughput by reducing the system overhead due to its in-system transparent erase-before-write capability. The device operates from a single +5 V power supply in the read and smart write mode. Word read and write can be controlled entirely by TTL signal levels.

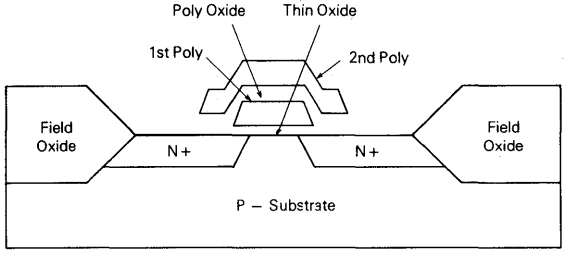
To ease system design, the high voltage needed by the device for the smart write cycle is generated internally. Another ease-of-use feature is the choice of erase modes (bulk, byte, row, or column) to optimize system erase/write time. For microprocessor compatibility, on-chip latches are provided for addresses, data, and controls allowing the microprocessor to perform other tasks while the MCM2864 is programming itself by the provision of a RDY/$\overline{BUSY}$ function to indicate status.

The MCM2864 is fabricated using Motorola's FETMOS technology (Floating-gate Electron Tunneling MOS), which has the advantages of good data retention, good endurance, and conventional processing.

The device pinout is part of Motorola's industry standard byte wide Nonvolatile Memory family, providing cost-effective density upgrades.

- Single +5 Volt Power Supply
- Organized as 8192 Bytes of 8 Bits
- Fast Access Time of 200 ns Maximum
- Low Power Dissipation
- In-System Automatic and Transparent Erase Before Write
- RDY/$\overline{BUSY}$ Function to Indicate Status
- Data Protected During Power Up and Power Down
- 10,000 Write Cycles Per Byte
- Data Integrity of 10 Years
- Latched Address, Data, and Controls During Write
- Chip Enable and Output Enable for Two Line Bus Control
- 10 ms for Byte Write and Internally Timed
- 28-Pin JEDEC Standard Pinout
- Internal Automatic Erase/Write Verify

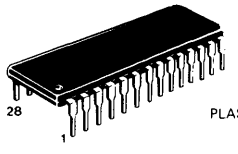
FETMOS
(Floating-Gate Electron Tunneling MOS)



HMOS

(N-CHANNEL, SILICON GATE)

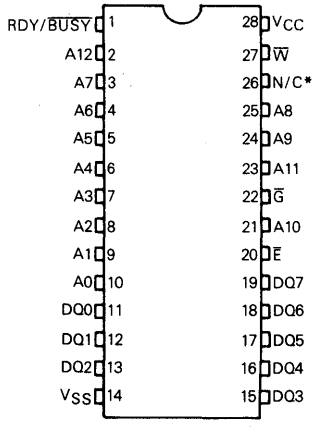
8192 × 8-BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 710

L SUFFIX CERAMIC PACKAGE ALSO AVAILABLE — CASE 719

PIN ASSIGNMENT

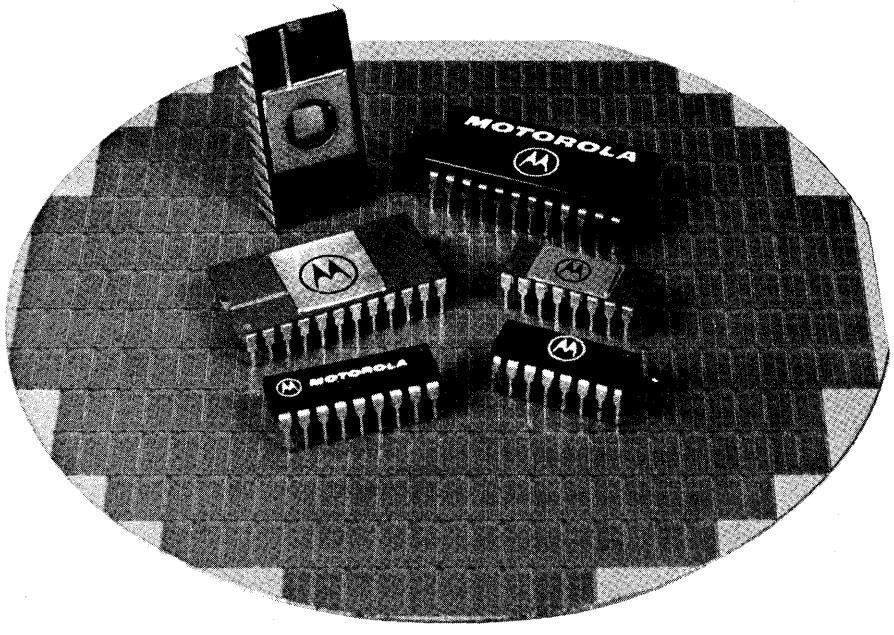


*For normal operation, pin 26 can be tied to V_{SS} or V_{CC}.

PIN NAMES

A	Address
DQ	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
RDY/$\overline{BUSY}$	Ready/Busy
N/C	No Connect
V_{CC}	+5 V Power Supply
V_{SS}	Ground

EEPROM



MOS ROMs

ROM

MOTOROLA

MCM6670
MCM6674

MOS

(N-CHANNEL, SILICON GATE)

128c X 7 X 5 CHARACTER GENERATOR

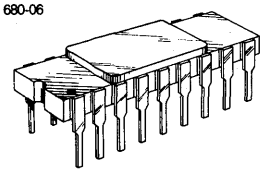
The MCM6670 is a mask-programmable horizontal-scan (row select) character generator containing 128 characters in a 5 X 7 matrix. A 7-bit address code is used to select one of the 128 available characters, and a 3-bit row select code chooses the appropriate row to appear at the outputs. The rows are sequentially displayed, providing a 7-word sequence of 5 parallel bits per word for each character selected by the address inputs.

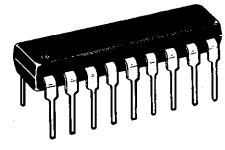
The MCM6674 is a preprogrammed version of the MCM6670. The complete pattern of this device is contained in this data sheet.

- Fully Static Operation
- TTL Compatibility
- Single ±10% +5 Volt Power Supply
- 18-Pin Package
- Diagonal Corner Power Supply Pins
- Fast Access Time, 350 ns (max)

128c x 7 x 5 HORIZONTAL-SCAN CHARACTER GENERATOR

L SUFFIX
CERAMIC PACKAGE
CASE 680-06





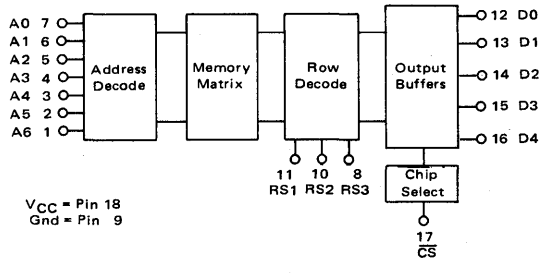
P SUFFIX
PLASTIC PACKAGE
CASE 707-02

ABSOLUTE MAXIMUM RATINGS (See Note 1)

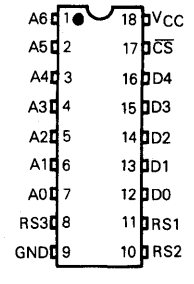
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ROM

DC OPERATING CONDITIONS AND CHARACTERISITCS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	V_{CC}	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 2.0 V or $\overline{CS}$ = 0.8 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	–	130	mAdc

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	5.0	pF
Output Capacitance	C_{out}	5.0	pF

ROM

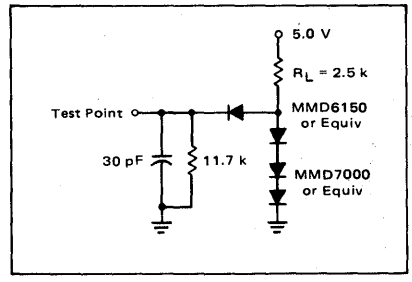
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 30 pF

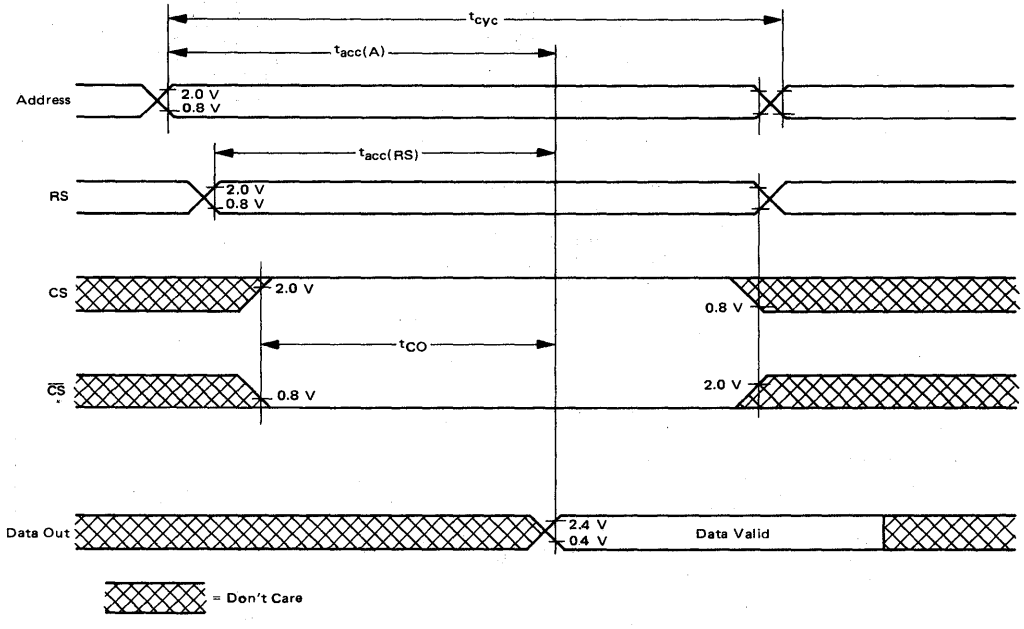
AC TEST LOAD



AC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Address Access Time	$t_{acc(A)}$	–	350	ns
Row Select Access Time	$t_{acc(RS)}$	–	350	ns
Chip Select to Output Delay	t_{CO}	–	150	ns

TIMING DIAGRAM



ROM

CUSTOM PROGRAMMING FOR MCM6670

By the programming of a single photomask, the customer may specify the content of the MCM6670. Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the following forms, in order of preference:

1. Hexadecimal coding using IBM Punch Cards (Figures 3 and 4).
2. Hexadecimal coding using ASCII Paper Tape Punch (Figure 5).

Programming of the MCM6670 can be achieved by using the following sequence:

1. Create the 128 characters in a 5 x 7 font using the format shown in Figure 1. Note that information at output D4 appears in column one, D3 in column two, thru D0 information in column five. The dots filled in and programmed as a logic "1" will appear at the outputs as V_{OH}; the dots left blank will be at V_{OL}. R0 is always programmed to be blank (V_{OL}). (Blank formats appear at the end of this data sheet for your convenience; they are not to be submitted to Motorola, however.)

2. Convert the characters to hexadecimal coding treating dots as ones and blanks as zeros, and enter this information in the blocks to the right of the character font format. The information for D4 must be a hex one or zero, and is entered in the left block. The information for D3 thru D0 is entered in the right block, with D3 the most significant bit for the hex coding, and D0 the least significant.

3. Transfer the hexadecimal figures either to punched cards (Figure 3) or to paper tape (Figure 5).

4. Transmit this data to Motorola, along with the customer name, customer part number and revision, and an indication that the source device is the MCM6670.

5. Information should be submitted on an organizational data form such as that shown in Figure 2.

FIGURE 1 – CHARACTER FORMAT

ROW SELECT TRUTH TABLE

RS3	RS2	RS1	OUTPUT
0	0	0	R0
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	R4
1	0	1	R5
1	1	0	R6
1	1	1	R7

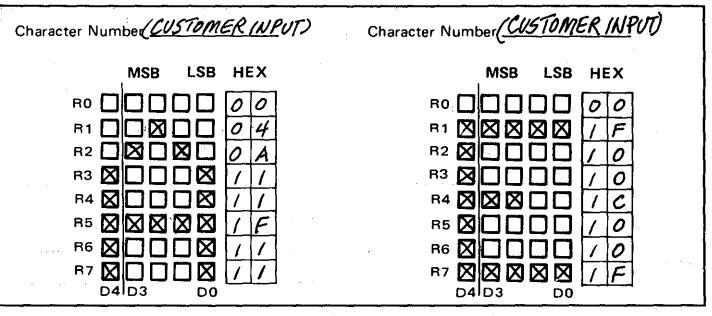


FIGURE 2 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM6670 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

Chip-Select Options:

	Active High 1	Active Low 0	No-Connect
CS	☐	☐	☐

ROM

FIGURE 3 – CARD PUNCH FORMAT

Columns

1-9	Blank
10-25	Hex coding for first character
26	Slash (/)
27-42	Hex coding for second character
43	Slash (/)
44-59	Hex coding for third character
60	Slash (/)
61-76	Hex coding for fourth character
77-78	Blank
79-80	Card number (starting 01; thru 32)

Column 10 on the first card contains either a zero or a one to program D4 of row R0 for the first character. Column 11 contains the hex character for D3 thru D0. Columns 12 and 13 contain the information to program R1. The entire first character is coded in columns 10 thru 25. Each card contains the coding for four characters; 32 cards are required to program the entire 128 characters. The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part. Figure 3 provides an illustration of the correct format.

FIGURE 4 – EXAMPLE OF CARD PUNCH FORMAT
(First 12 Characters of MCM6670P4)

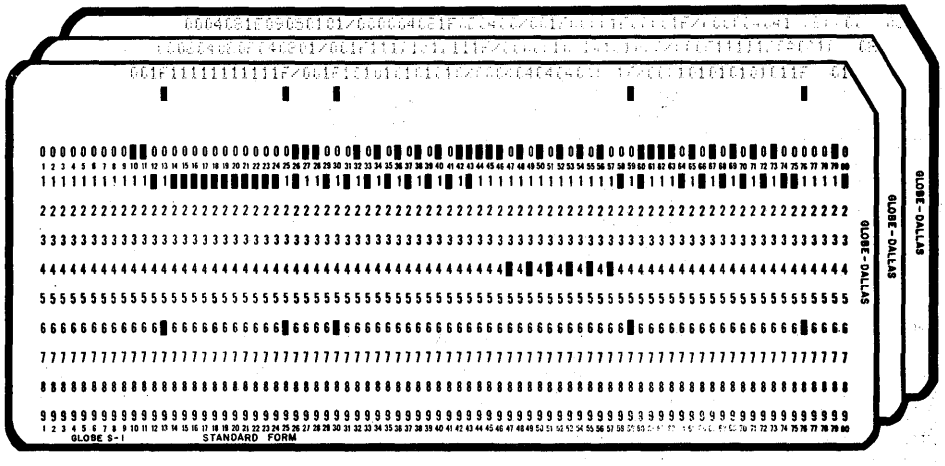


FIGURE 5 – PAPER TAPE FORMAT

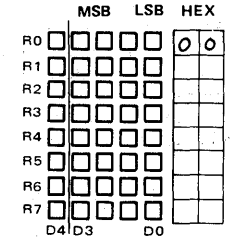
Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M ⩽ 64)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2114	Remaining 31 lines of hex figures, each line followed by a Carriage Return and Line Feed

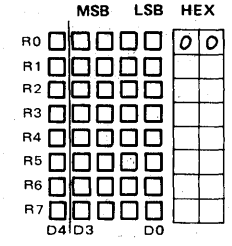
Blank Tape

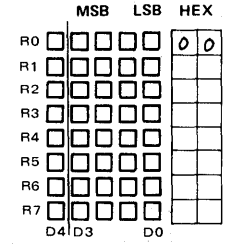
Frames 1 to M are left to the customer for internal identification, where M ⩽ 64. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

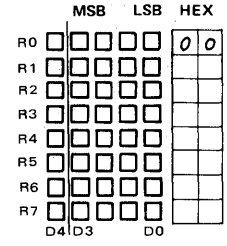
Frame M + 3 contains a zero or a one to program D4 of row R0 for the first character. Frame M + 4 contains the hex character for D3 thru D0, completing the programming information for R0. Frames M + 5 and M + 6 contain the information to program R1. The entire first character is coded in Frames M + 3 thru M + 18. Four complete characters are programmed with each line. A total of 32 lines program all 128 characters (32 x 4). The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part.

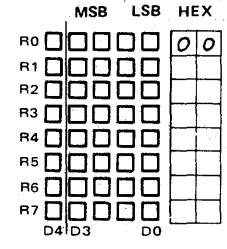
ROM

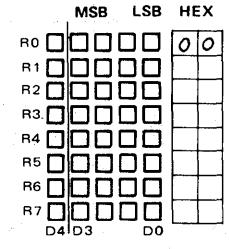


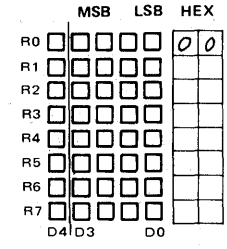


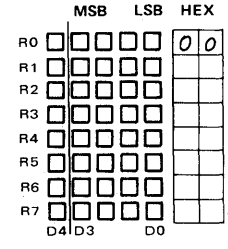


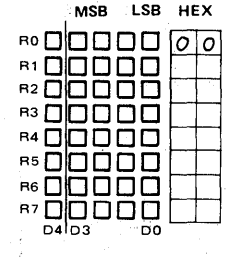


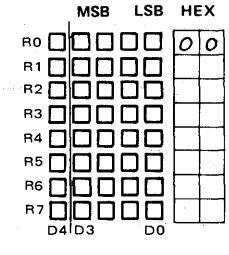


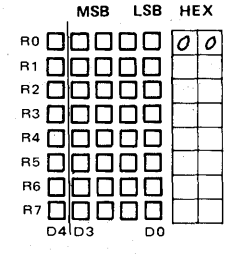


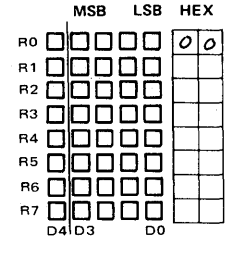


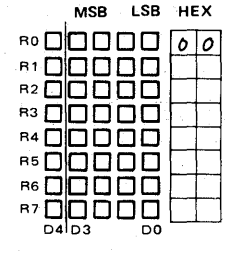


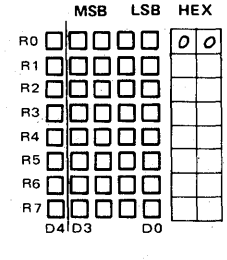


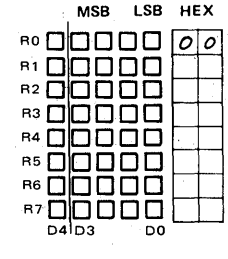


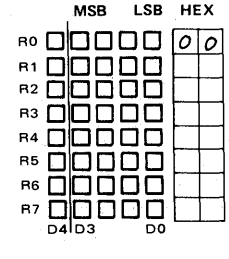












The formats below are given for your convenience in preparing character information for MCM6670 programming. THESE FORMATS ARE NOT TO BE USED TO TRANSMIT THE INFORMATION TO MOTOROLA. Refer to the Custom Programming instructions for detailed procedures.

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

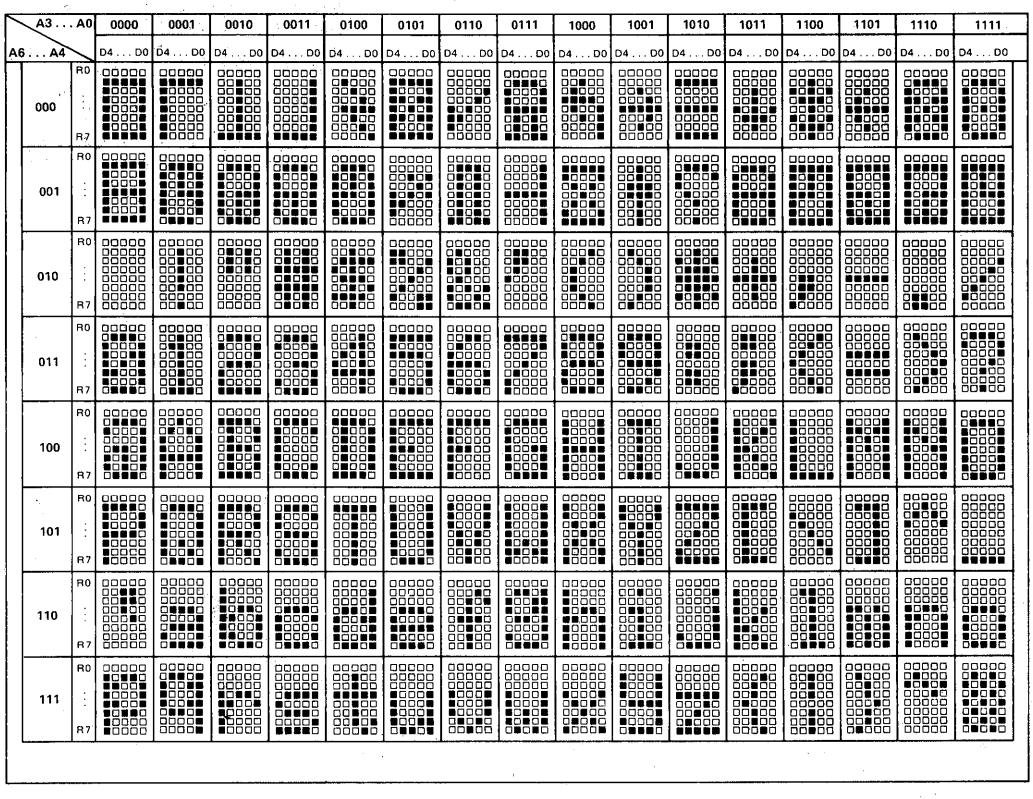
Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

FIGURE 6 – MCM6674 PATTERN



MOTOROLA

MCM66700 MCM66710 MCM66714 MCM66720 MCM66730 MCM66734 MCM66740 MCM66750 MCM66751 MCM66760 MCM66770 MCM66780 MCM66790

8192-BIT READ ONLY MEMORIES
ROW SELECT CHARACTER GENERATORS

The MCM66700 is a mask-programmable 8192-bit horizontal-scan (row select) character generator. It contains 128 characters in a 7 X 9 matrix, and has the capability of shifting certain characters that normally extend below the baseline such as j, y, g, p, and q. Circuitry is supplied internally to effectively lower the whole matrix for this type of character—a feature previously requiring external circuitry.

A seven-bit address code is used to select one of the 128 available characters. Each character is defined as a specific combination of logic 1s and 0s stored in a 7 X 9 matrix. When a specific four-bit binary row select code is applied, a word of seven parallel bits appears at the output. The rows can be sequentially selected, providing a nine-word sequence of seven parallel bits per word for each character selected by the address inputs. As the row select inputs are sequentially addressed, the devices will automatically place the 7 X 9 character in one of two preprogrammed positions on the 16-row matrix, with the positions defined by the four row select inputs. Rows that are not part of the character are automatically blanked.

The devices listed are preprogrammed versions of the MCM66700. They contain various sets of characters to meet the requirements of diverse applications. The complete patterns of these devices are contained in this data sheet.

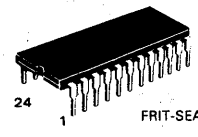
- Fully Static Operation
- Fully TTL Compatible with Three-State Outputs
- CMOS and MPU Compatible, Single ±10% 5 Volt Supply
- Shifted Character Capability
  (Except MCM66720, MCM66730, and MCM66734)
- Maximum Access Time = 350 ns
- 4 Programmable Chip Selects (0, 1, or X)
- Pin-for-Pin Replacement for the MCM6570, Including All Standard Patterns

MOS

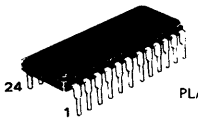
(N-CHANNEL, SILICON-GATE)

8K READ ONLY MEMORIES

HORIZONTAL-SCAN CHARACTER GENERATORS WITH SHIFTED CHARACTERS

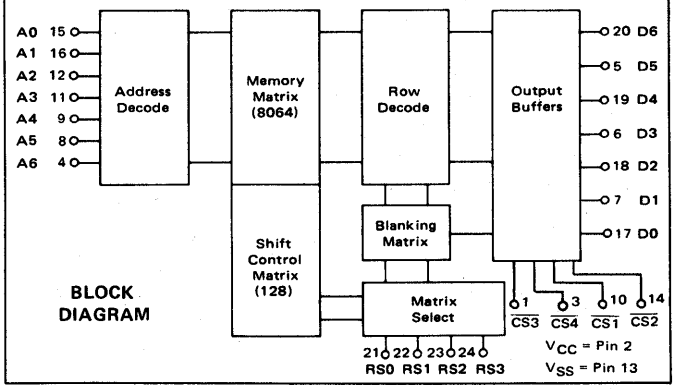


C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623-04



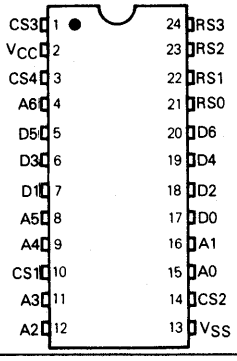
P SUFFIX
PLASTIC PACKAGE
CASE 709-02

ROM



BLOCK DIAGRAM

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note 1, Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC}	-0.3 to 7.0	Vdc
Input Voltage	V_{in}	-0.3 to 7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher-than-recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input Logic "1" Voltage	V_{IH}	2.0	–	V_{CC}	Vdc
Input Logic "0" Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5 Vdc, V_{CC} = 4.5 Vdc)	I_{IH}	–	–	2.5	μAdc
Output Low Voltage (Blank) (I_{OL} = 1.6 mAdc)	V_{OL}	0	–	0.4	Vdc
Output High Voltage (Dot) (I_{OH} = -205 μAdc)	V_{OH}	2.4	–	–	Vdc
Power Supply Current	I_{CC}	–	–	80	mAdc
Power Dissipation	P_D	–	200	440	mW

CAPACITANCE (Periodically sampled rather than 100% tested)

Input Capacitance (f = 1.0 MHz)	C_{in}	–	4.0	7.0	pF
Output Capacitance (f = 1.0 MHz)	C_{out}	–	4.0	7.0	pF

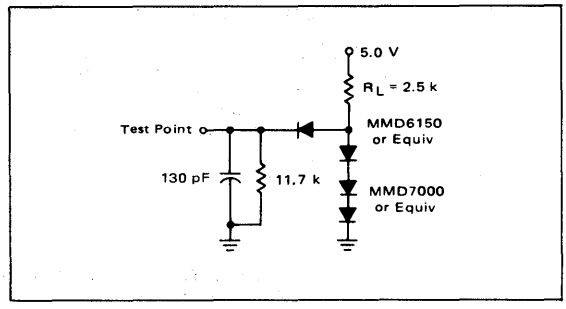
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 130 pF

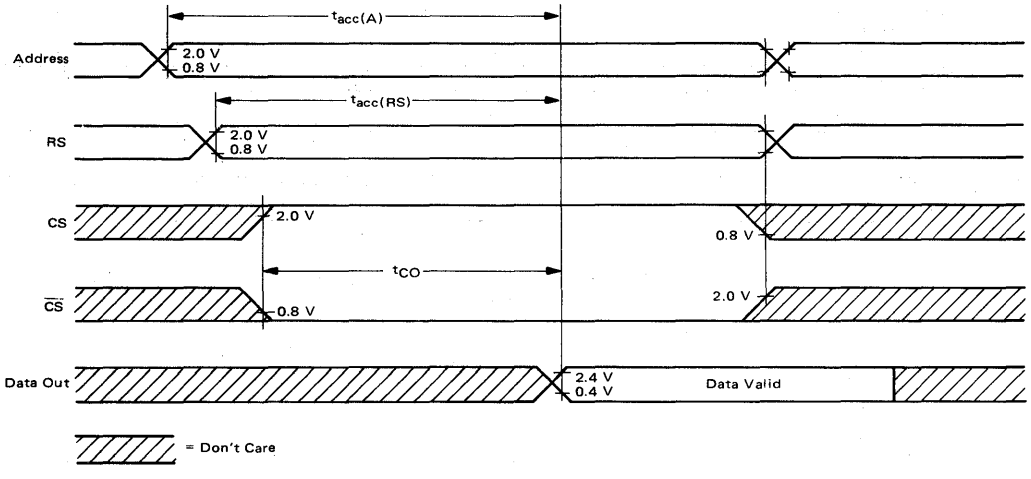
AC TEST LOAD



AC CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Address Access Time	$t_{acc(A)}$	250	350	ns
Row Select Access Time	$t_{acc(RS)}$	250	350	ns
Chip Select to Output Delay	t_{CO}	100	150	ns

TIMING DIAGRAM



ROM

MEMORY OPERATION (Using Positive Logic)

Most positive level = 1, most negative level = 0.

Address

To select one of the 128 characters, apply the appropriate binary code to the Address inputs (A0 through A6).

Row Select

To select one of the rows of the addressed character to appear at the seven output lines, apply the appropriate binary code to the Row Select inputs (RS0 through RS3).

Shifted Characters

These devices have the capability of displaying characters that descend below the bottom line (such as lowercase letters j, y, g, p, and q). Internal circuitry effectively drops the whole matrix for this type of character. Any character can be programmed to occupy either of the two positions in a 7 X 16 matrix. (Shifted characters are not available on MCM66720, MCM66730, or MCM66734.)

Output

For these devices, an output dot is defined as a logic 1 level, and an output blank is defined as a logic 0 level.

Programmable Chip Select

The MCM66700 has four Chip Select inputs that can be programmed with a 1, 0, or don't care (not connected). A don't care must always be the highest chip select pin or pins. All standard patterns have Don't Care Chip Select—except MCM66751.

DISPLAY FORMAT

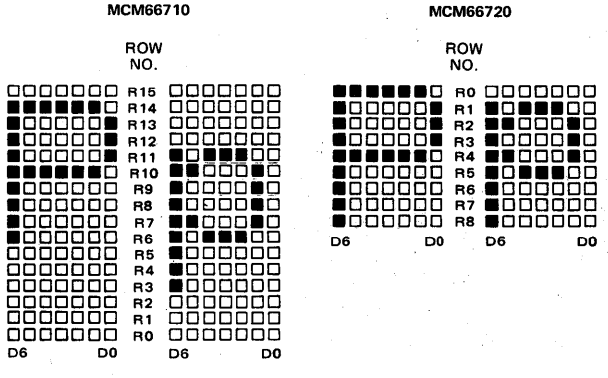
Figure 1 shows the relationship between the logic levels at the row select inputs and the character row at the outputs. The MCM66700 allows the user to locate the basic 7 X 9 font anywhere in the 7 X 16 array. In addition, a shifted font can be placed anywhere in the same 7 X 16 array. For example, the basic MCM66710 font is established in rows R14 through R6. All other rows are automatically blanked. The shifted font is established in rows R11 through R3, with all other rows blanked. Thus, while any one character is contained in a 7 X 9 array, the MCM66710 requires a 7 X 12 array on the CRT screen to contain both normal and descending characters. Other uses of the shift option may require as much as the full 7 X 16 array, or as little as the basic 7 X 9 array (when no shifting occurs, as in the MCM66720).

The MCM66700 can be programmed to be scanned either from bottom to top or from top to bottom. This is achieved through the option of assigning row numbers in ascending or descending count, as long as both the basic font and the shifted font are the same. For example, an up counter will scan the MCM66710 from bottom to top, whereas an up counter will scan the MCM66714 from top to bottom (see Figures 7 and 8 for row designation).

FIGURE 1 – ROW SELECT INPUT CODE AND SAMPLE CHARACTERS FOR MCM66710 AND MCM66720

ROW SELECT TRUTH TABLE

RS3	RS2	RS1	RS0	OUTPUT
0	0	0	0	R0
0	0	0	1	R1
0	0	1	0	R2
0	0	1	1	R3
0	1	0	0	R4
0	1	0	1	R5
0	1	1	0	R6
0	1	1	1	R7
1	0	0	0	R8
1	0	0	1	R9
1	0	1	0	R10
1	0	1	1	R11
1	1	0	0	R12
1	1	0	1	R13
1	1	1	0	R14
1	1	1	1	R15



ROM

CUSTOM PROGRAMMING FOR MCM66700

By the programming of a single photomask, the customer may specify the content of the MCM66700. Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the following forms, in order of preference:*

1. Hexadecimal coding using IBM Punch Cards (Figures 3 and 4)
2. Hexadecimal coding using ASCII Paper Tape Punch (Figure 5)

Programming of the MCM66700 can be achieved by using the follow sequence:

1. Create the 128 characters in a 7 X 9 font using the format shown in Figure 2. Note that information at output D6 appears in column one, D5 in column two, through D0 information in column seven. The dots filled in and programmed as a logic 1 will appear at the outputs as V_{OH}; the dots left blank will be at V_{OL}. (Blank formats appear at the end of this data sheet for your convenience; they are not to be submitted to Motorola, however.)

2. Indicate which characters are shifted by filling in the extra square (dot) in the top row, at the left (column S).

3. Convert the characters to hexadecimal coding treating dots as 1s and blanks as 0s, and enter this information in the blocks to the right of the character font format. High order bits are at the left, in columns S and D3. For the bottom eight rows, the bit in Column S must be 0, so these locations have been omitted. For the top row, the bit in Column S will be 0 for an unshifted character, and 1 for a shifted character.

4. Transfer the hexadecimal figures either to punched cards (Figure 3) or to paper tape (Figure 5).

5. Assign row numbers to the unshifted font. These must be nine sequential numbers (values 0 through 15) assigned consecutively to the rows. The shifted font is similarly placed in any position in the 16 rows.

6. Provide, in writing, the information indicated in Figure 6 (a copy of Figure 10 may be used for this purpose). Submit this information to Motorola together with the punched cards or paper tape.

FIGURE 2 – CHARACTER FORMAT

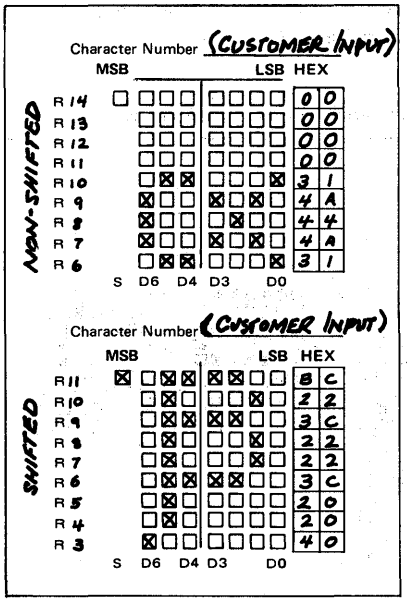


FIGURE 3 – CARD PUNCH FORMAT

Columns	
1 – 10	Blank
11	Asterisk (*)
12 – 29	Hex coding for first character
30	Slash (/)
31 – 48	Hex coding for second character
49	Slash (/)
50 – 67	Hex coding for third character
68	Slash (/)
69 – 76	Blank
77 – 78	Card number (starting 01; through 43)
79 – 80	Blank

Column 12 on the first card contains the hexadecimal equivalent of column S and D6 through D4 for the top row of the first character. Column 13 contains D3 through D0. Columns 14 and 15 contain the information for the next row. The entire first character is coded in columns 12 through 29. Each card contains the coding for three characters. 43 cards are required to program the entire 128 characters, the last card containing only two characters. The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part. As an example, the first nine characters of the MCM66710 are correctly coded and punched in Figure 4.

*NOTE: Motorola can accept magnetic tape and truth table formats. For further information contact your local Motorola sales representative.

ROM

FIGURE 4 – EXAMPLE OF CARD PUNCH FORMAT
(First 9 Characters of MCM66710)

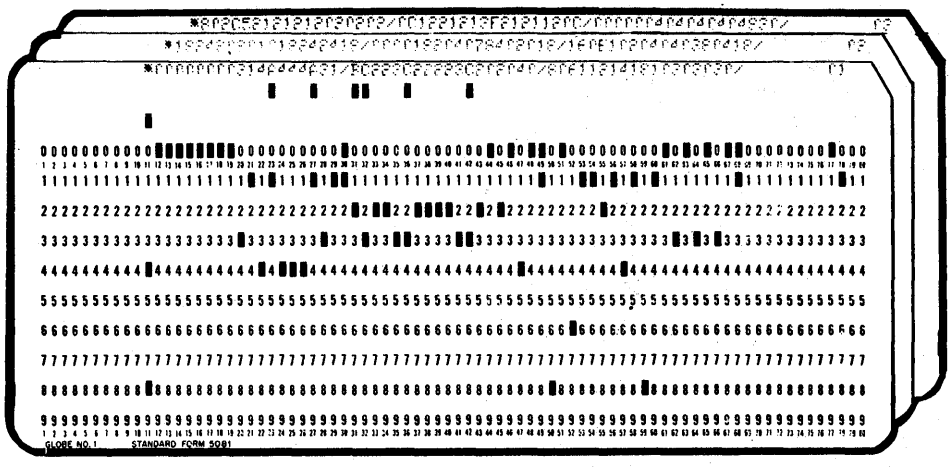


FIGURE 5 – PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M ≤ 64)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2378	Remaining 35 lines of hex figures, each line followed by a Carriage Return and Line Feed

Blank Tape

Frames 1 to M are left to the customer for internal identification, where M ≤ 64. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Frame M + 3 contains the hexadecimal equivalent of column S and D6 thru D4 for the top row of the first character. Frame M + 4 contains D3 thru D0. Frames M + 5 and M + 6 program the second row of the first character. Frames M + 3 to M + 66 comprise the first line of the printout. The line is terminated with a CR and LF.

The remaining 35 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 36 lines of data contain 36 x 64 or 2304 hex figures. Since 18 hex figures are required to program each 7 x 9 character, the full 128 (2304 ÷ 18) characters are programmed.

FIGURE 6 – FORMAT FOR ORGANIZATIONAL DATA

ORGANIZATIONAL DATA
MCM66700 MOS READ ONLY MEMORY

Customer _____

Customer Part No. _____ Rev. _____

Row Number for top row of non-shifted font _____

Row Number for bottom row of non-shifted font _____

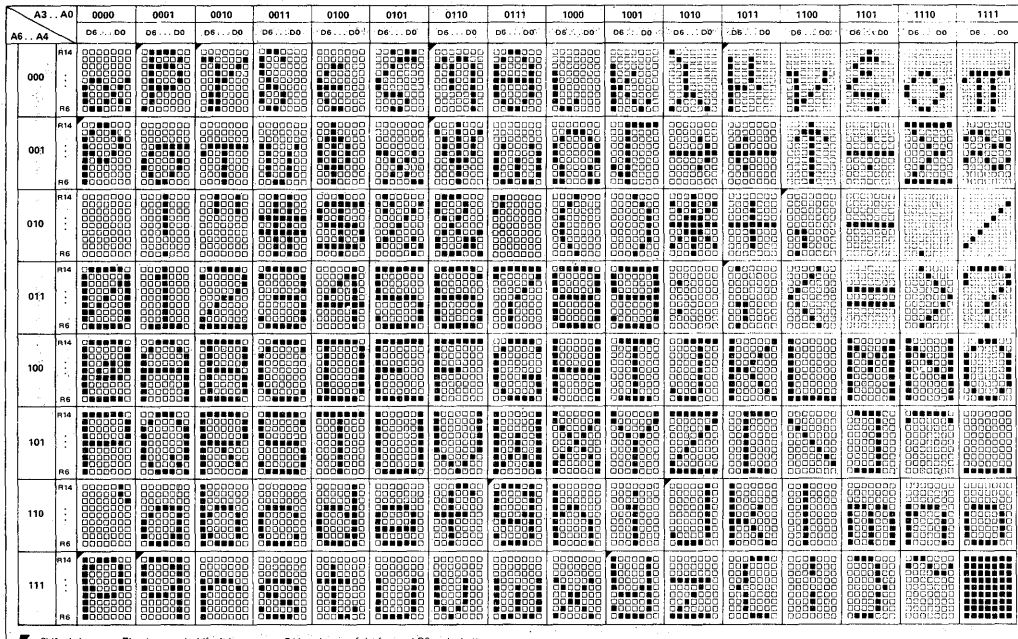
Row Number for top row of shifted font _____

Programmable Chip Select information: 1 = Active High 0 = Active Low X = Don't Care (Not Connected)

CS1____ CS2____ CS3____ CS4____

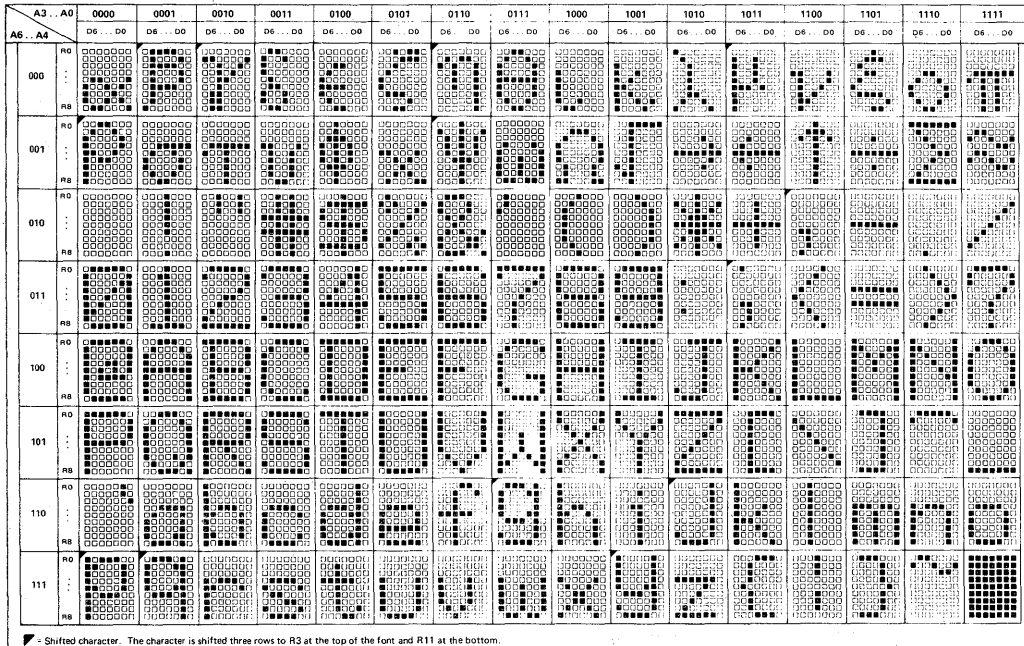
ROM

FIGURE 7 – MCM66710 PATTERN



◤ = Shifted character. The character is shifted three rows to R11 at the top of the font and R3 at the bottom.

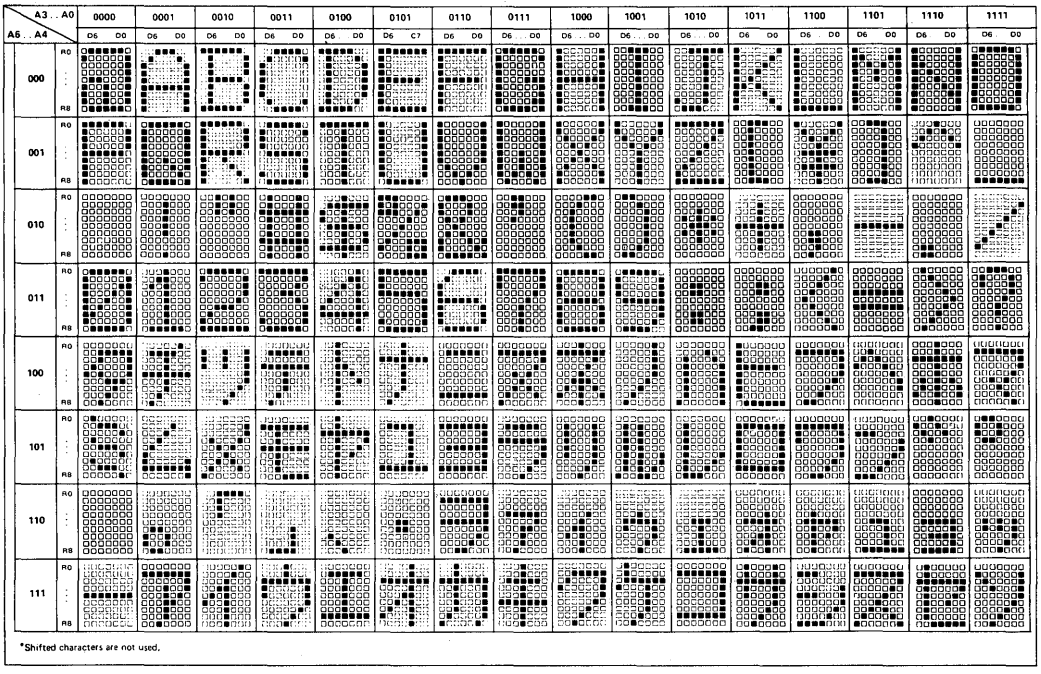
FIGURE 8 – MCM66714 PATTERN



◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

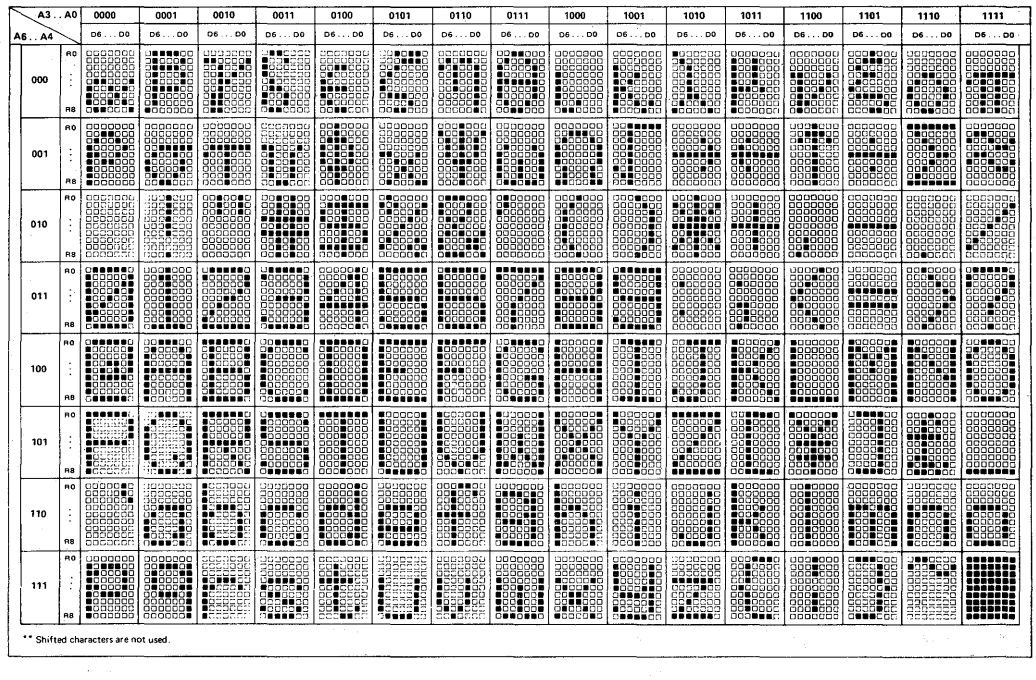
ROM

FIGURE 9 – MCM66734 PATTERN*



*Shifted characters are not used.

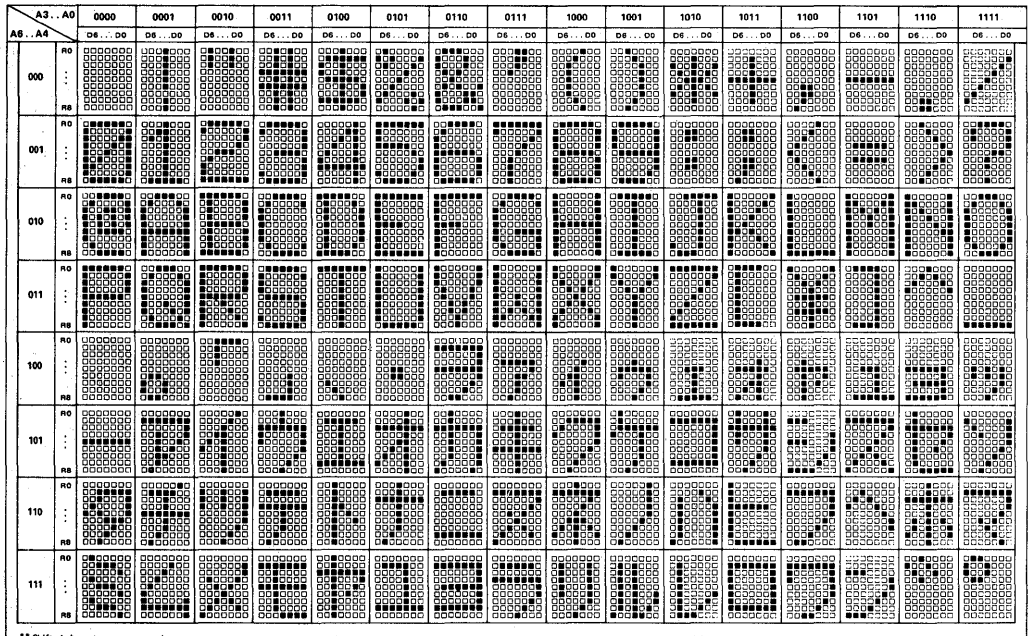
FIGURE 10 – MCM66720 PATTERN**



** Shifted characters are not used.

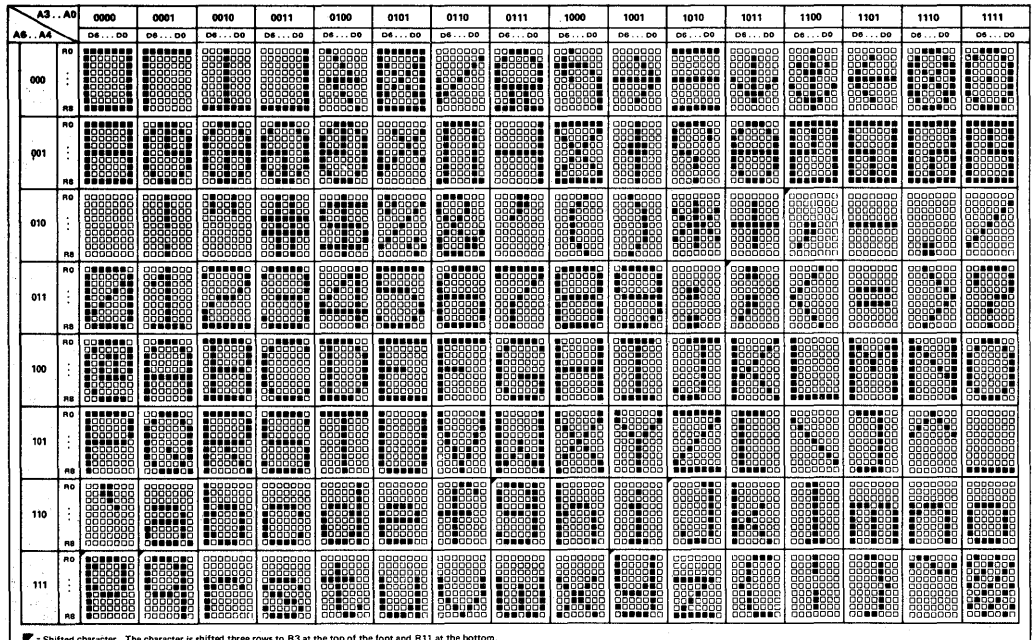
ROM

FIGURE 11 – MCM66730 PATTERN**



** Shifted characters are not used.

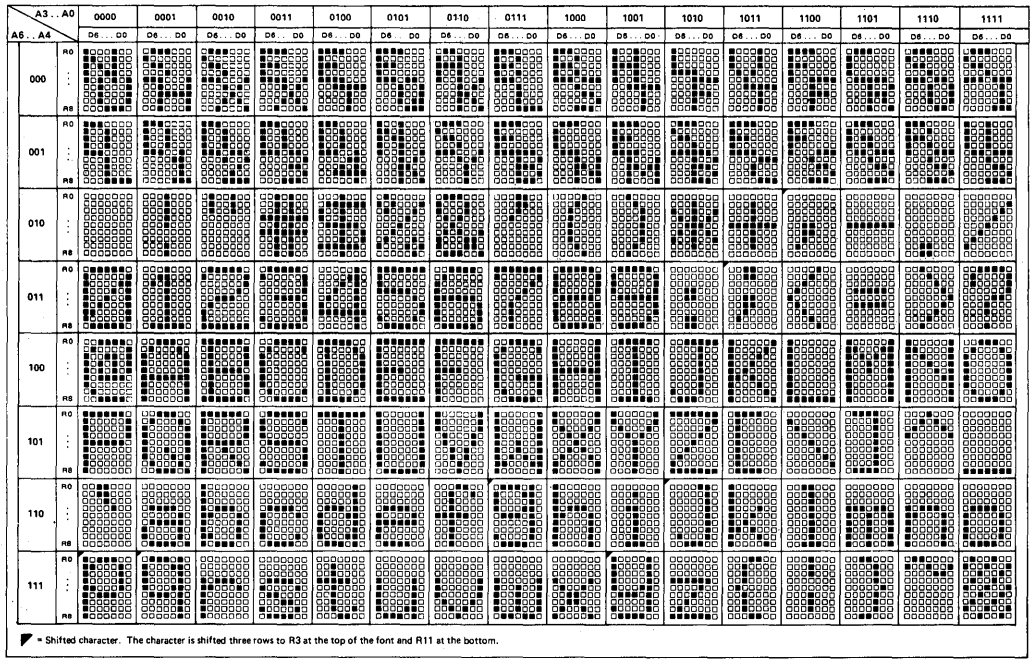
FIGURE 12 – MCM66740 PATTERN



◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

ROM

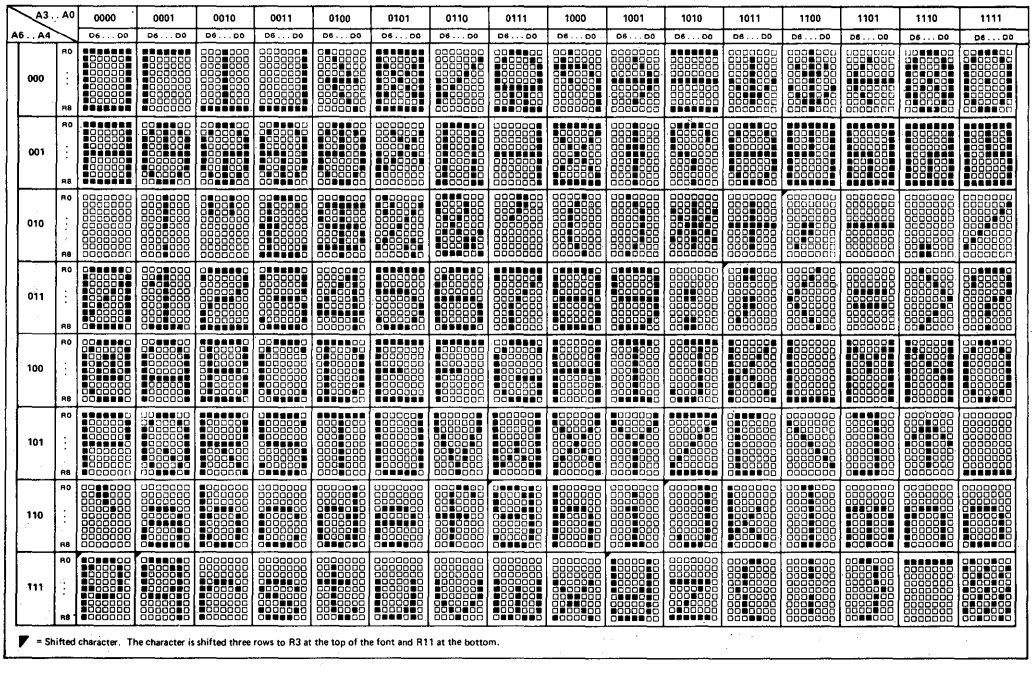
FIGURE 13 – MCM66750 PATTERN



◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

MCM66751 – Same as MCM66750 except CS1 = 0, CS2 = 0, CS3 = X, and CS4 = X.

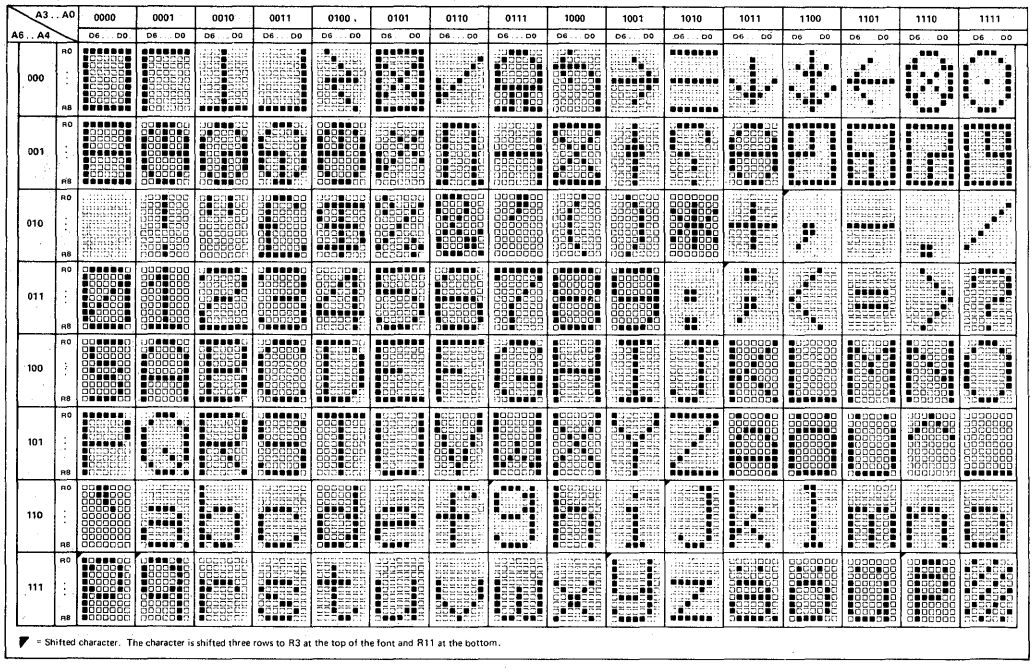
FIGURE 14 – MCM66760 PATTERN



◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

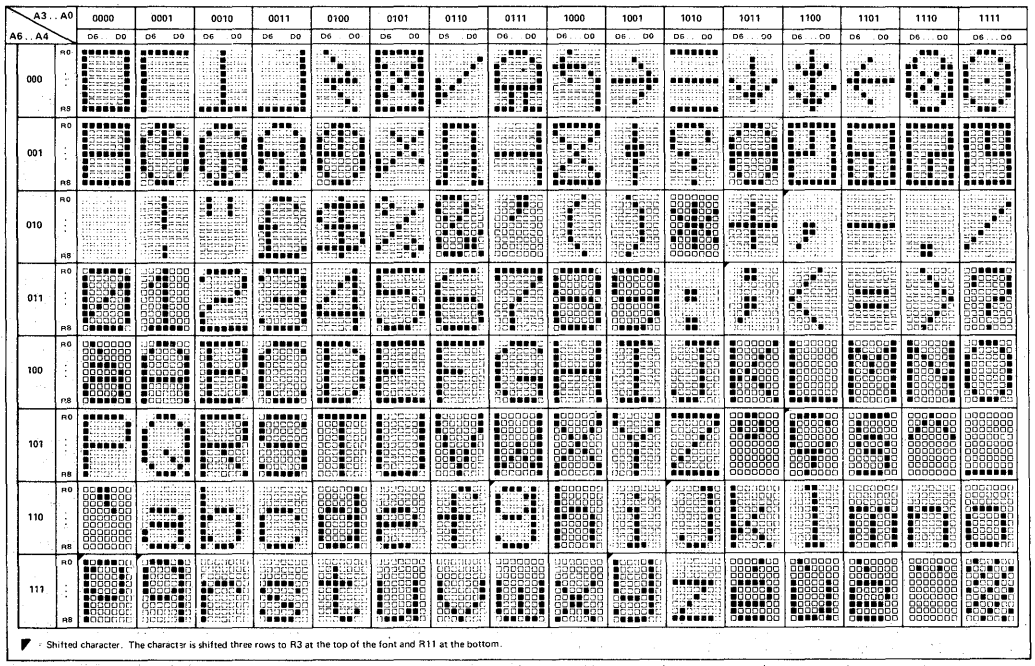
ROM

FIGURE 15 – MCM66770 PATTERN



▛ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

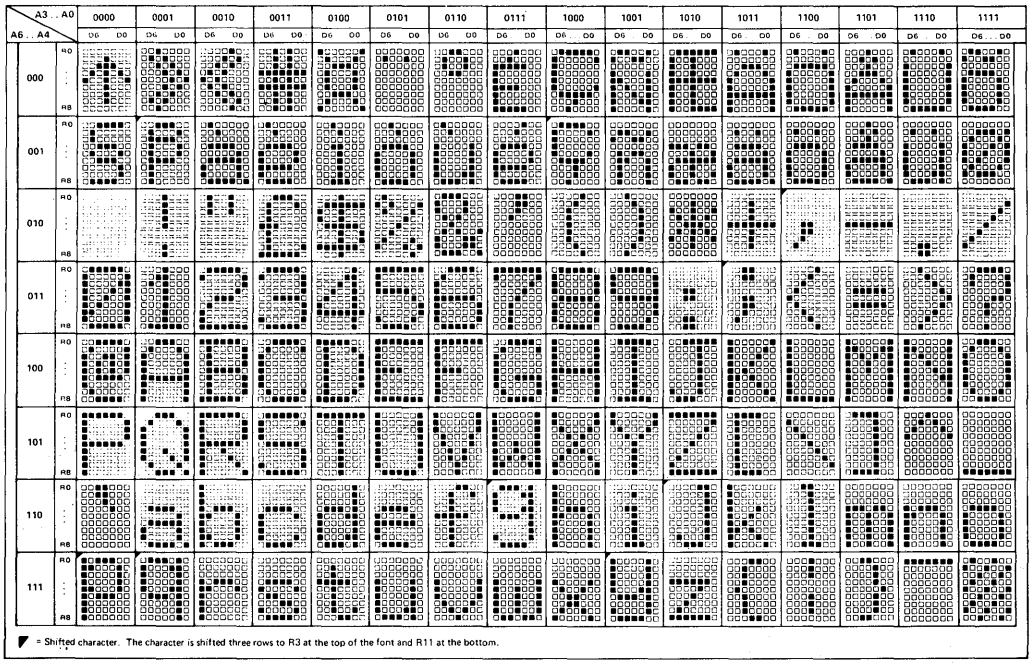
FIGURE 16 – MCM66780 PATTERN



▛ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

ROM

FIGURE 17 – MCM66790 PATTERN

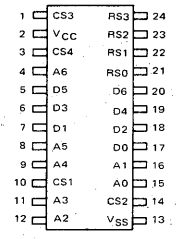


◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

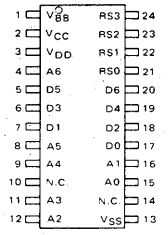
ROM

MCM6570 Series	MCM66700 Equivalent	Description
MCM6571	MCM66710	ASCII, shifted
MCM6571A	MCM66714	ASCII, shifted
MCM6572	MCM66720	ASCII
MCM6573	MCM66730	Japanese
MCM6573A	MCM66734	Japanese
MCM6574	MCM66740	Math Symbols
MCM6575	MCM66750	Alphanumeric Control
MCM6576	MCM66760	British, shifted
MCM6577	MCM66770	German, shifted
MCM6578	MCM66780	French, shifted
MCM6579	MCM66790	European, shifted

MCM66700 Series Pin Assignment



MCM6570 Series Pin Assignment

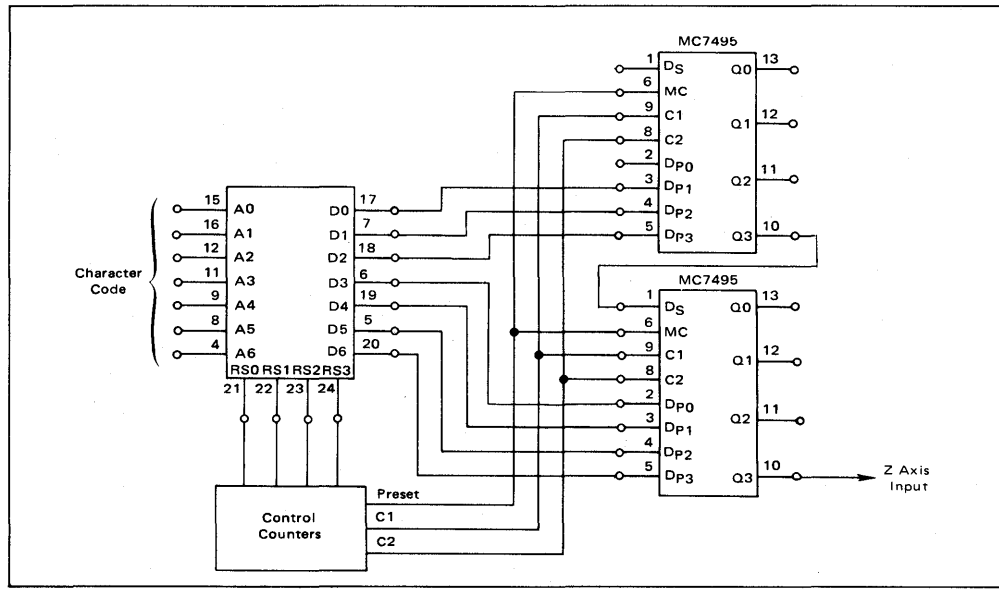


APPLICATIONS INFORMATION

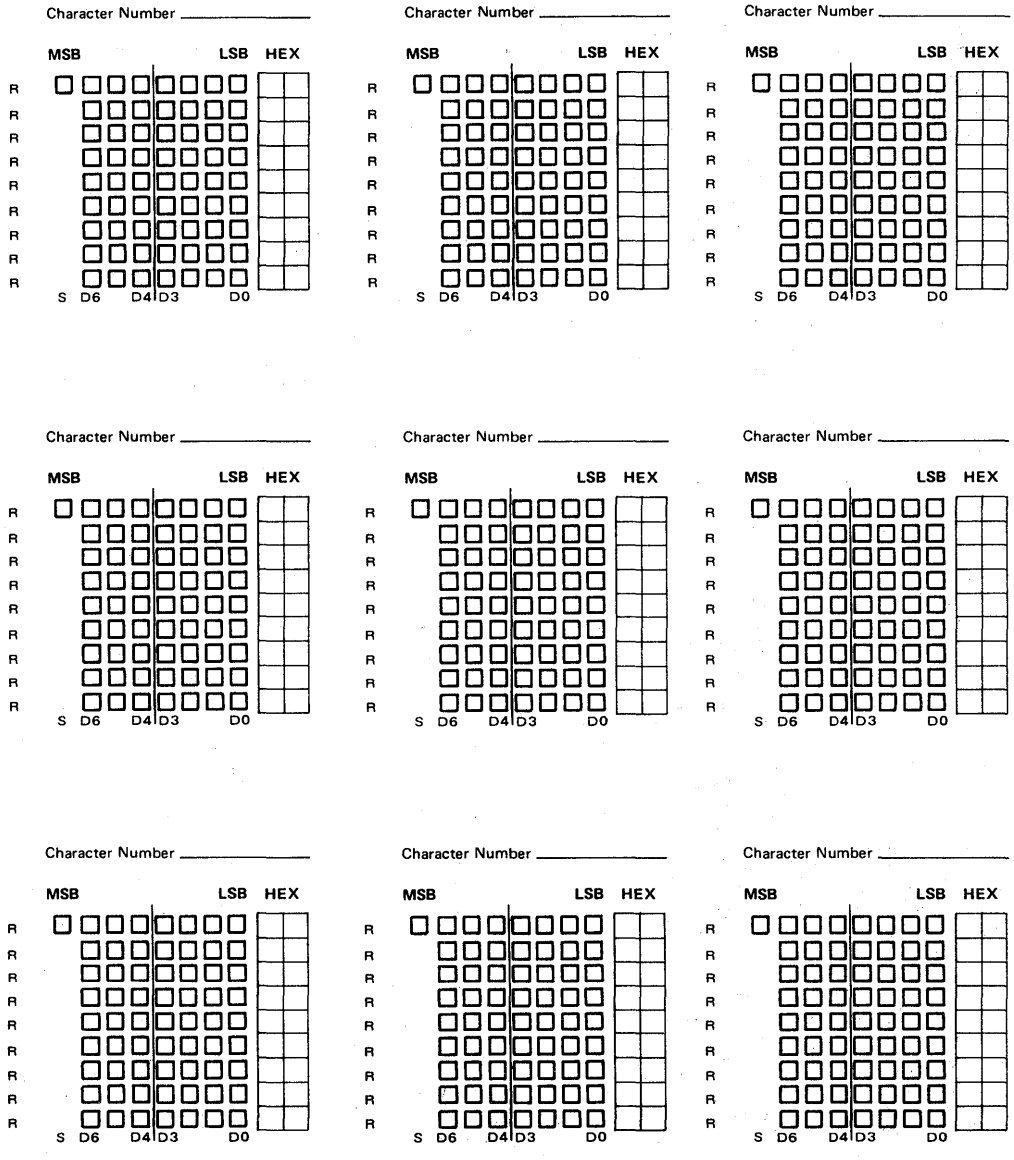
One important application for the MCM66700 series is in CRT display systems (Figure 18). A set of buffer shift registers or random access memories applies a 7-bit character code to the input of the character generator, which then supplies one row of the character according to the count at the four row select inputs. As each row is available, it is put into the TTL MC7495 shift registers. The parallel information in these shift registers is clocked serially out to the Z-axis where it modulates the raster to form the character.

The MCM66700 series require one power supply of +5.0 volts. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit spikes or glitches on their outputs when the ac power is switched on and off.

FIGURE 18 – CRT DISPLAY APPLICATION USING MCM66710



The formats below are given for your convenience in preparing character information for MCM66700 programming. **THESE FORMATS ARE NOT TO BE USED TO TRANSMIT THE INFORMATION TO MOTOROLA.** Refer to the Custom Programming instructions for detailed procedures.



MOTOROLA

MCM65516

2048 × 8 BIT READ ONLY MEMORY

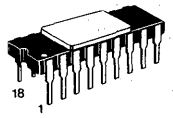
The MCM65516 is a complementary MOS mask programmable byte organized read only memory (ROM). The MCM65516 is organized as 2048 bytes of 8 bits, designed for use in multiplex bus systems. It is fabricated using Motorola's high performance silicon gate CMOS technology, which offers low-power operation from a single 5.0 volt supply.

The memory is compatible with CMOS microprocessors that share address and data lines. Compatibility is enhanced by pins 13, 14, 16, and 17 which give the user the versatility of selecting the active levels of each. Pin 17 allows the user to choose active high, active low, or a third option of programming which is termed the "MOTEL" mode. If this mode is selected by the user, it provides direct compatibility with either the Motorola MC146805E2 or Intel 8085 type microprocessor series. In the MOTEL operation the ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle. This unique operational feature makes the ROM an extremely versatile device.

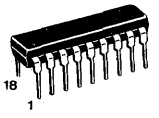
- 2K × 8 CMOS ROM
- 3 to 6 Volt Supply
- Access Time
  - 430 ns (5 V) MCM65516-43
  - 550 ns (5 V) MCM65516-55
- Low Power Dissipation
  - 15 mA Maximum (Active)
  - 30 μA Maximum (Standby)
- Multiplex Bus Directly Compatible With CMOS Microprocessors (MC146805E2, NSC800)
- Pins 13, 14, 16, and 17 are Mask Programmable
- MOTEL Mask Option Also Insures Direct Compatibility with NMOS Microprocessors Like MC6803, MC6801, 8085, and 8086
- Standard 18 Pin Package

CMOS
(COMPLEMENTARY MOS)

2048 × 8 BIT MULTIPLEXED BUS READ ONLY MEMORY

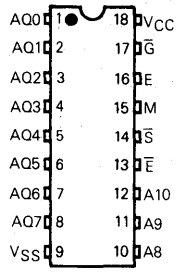


L SUFFIX
CERAMIC PACKAGE
CASE 680



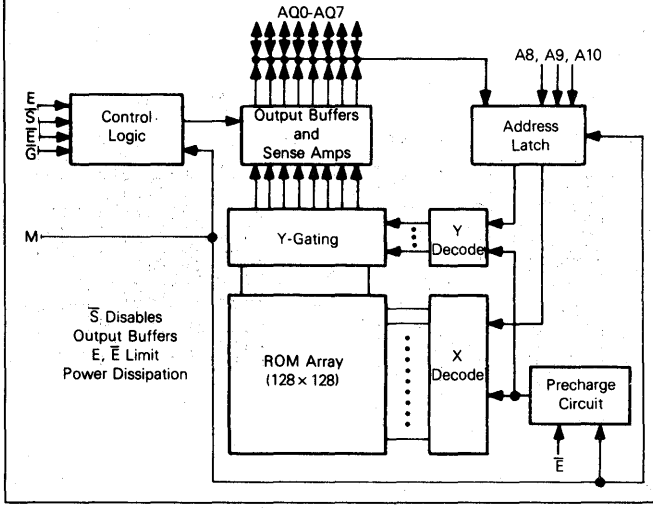
P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENTS



PIN NAMES	
AQ0-AQ7	Address/Data Output
A8-A10	Address
M	Multiplex Address Strobe
E	Chip Enable
S	Chip Select
G	Data Strobe (Output Enable)

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ROM

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	$V_{CC}-2.0$	–	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V

RECOMMENDED OPERATING CHARACTERISTICS

Characteristic	Symbol	MCM65516-43		MCM65516-55		Unit	Test Condition
		Min	Max	Min	Max		
Output High Voltage Source Current −1.6 mA	V_{OH}	$V_{CC}-0.4$ V	–	$V_{CC}-0.4$ V	–	V	
Output Low Voltage Sink Current +1.6 mA	V_{OL}	–	0.4	–	0.4	V	
Supply Current (Operating)	I_{CC1}	–	15	–	15	mA	$C_L=130$ pF, $V_{in}=V_{IH}$ to V_{IL}, $t_{cyc}=1.0$ μs
Supply Current (DC Active)	I_{CC2}	–	100	–	100	μA	$V_{in}=V_{CC}$ to GND
Standby Current	I_{SB}	–	30	–	50	μA	$V_{in}=V_{CC}$ to GND
Input Leakage	I_{in}	−10	+10	−10	+10	μA	
Output Leakage	I_{OL}	−10	+10	−10	+10	μA	

CAPACITANCE ($f=1.0$ MHz, $T_A=25°C$, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	5	pF
Output Capacitance	C_{out}	12.5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

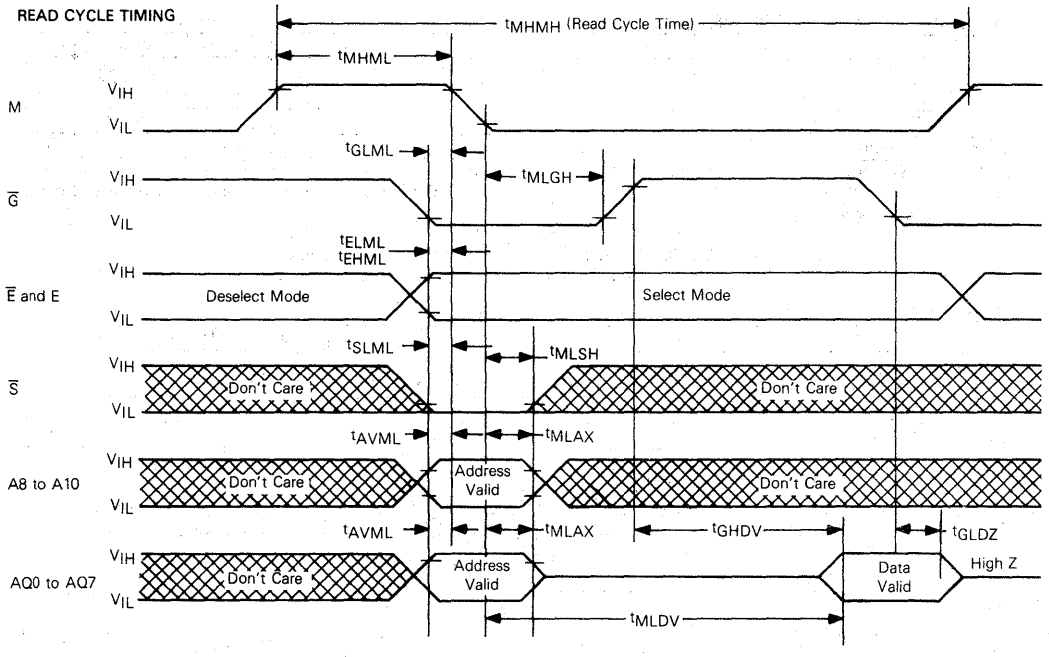
READ CYCLE

$C_L=130$ pF

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MCM65516-43		MCM65516-55		Unit
		Min	Max	Min	Max	
Address Strobe Access Time	t_{MLDV}	–	430	–	550	ns
Read Cycle Time	t_{MHMH}	–	750	–	1000	ns
Multiplex Address Strobe High to Multiplex Address Strobe Low (Pulse Width)	t_{MHML}	150	–	175	–	ns
Data Strobe Low to Multiplex Address Strobe Low	t_{GLML}	50	–	50	–	ns
Multiplex Address Strobe Low to Data Strobe High	t_{MLGH}	100	–	160	–	ns
Address Valid to Multiplex Address Strobe Low	t_{AVML}	50	–	50	–	ns
Chip Select Low to Multiplex Address Strobe Low	t_{SLML}	50	–	50	–	ns
Multiplex Address Strobe Low to Chip Select High	t_{MLSH}	50	–	80	–	ns
Chip Enable Low/High to Multiplex Address Strobe Low	t_{ELML} t_{EHMH}	50 50	– –	50 50	– –	ns
Multiplex Address Strobe Low to Address Don't Care	t_{MLAX}	50	–	80	–	ns
Data Strobe High to Data Valid	t_{GHDV}	175	–	200	–	ns
Data Strobe Low to High Z	t_{GLDZ}	–	160	–	160	ns

ROM



FUNCTIONAL DESCRIPTION

The 2K × 8 bit CMOS ROM (MCM65516) shares address and data lines and, therefore, is compatible with the majority of CMOS microprocessors in the industry. The package size is reduced from 24 pins for standard NMOS ROMs to 18 pins due to the multiplexed bus approach. The savings in package size and external bus lines adds up to tighter board packing density which is handy for battery powered hand carried CMOS systems. This ROM is designed with the intention of having very low active as well as standby currents. The active power dissipation of 150 mW (at V_{CC} = 5 V freq = 1 MHz) and standby power of 250 μW (at V_{CC} = 5 V) add up to low power for battery operation. The typical access time of the ROM is 280 ns making it acceptable for operation with today's existing CMOS microprocessors.

An example of this operation is shown in Figure 1. Shown is a typical connection with either the Motorola MC146805E2 CMOS microprocessor (M6800 series) or the National NSC800 which is an 8085 or Z80 based system. The main difference between the systems is that the data strobe (DS) on the MC146805E2 and the read bar ($\overline{RD}$) on the 8085 both control the output of data from the ROM but are of opposite polarity. The Motorola 2K × 8 ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle. This is termed the MOTEL mode of operation. This unique operational feature makes the ROM an extremely versatile part. Further operational features are explained in the following section.

Operational Features

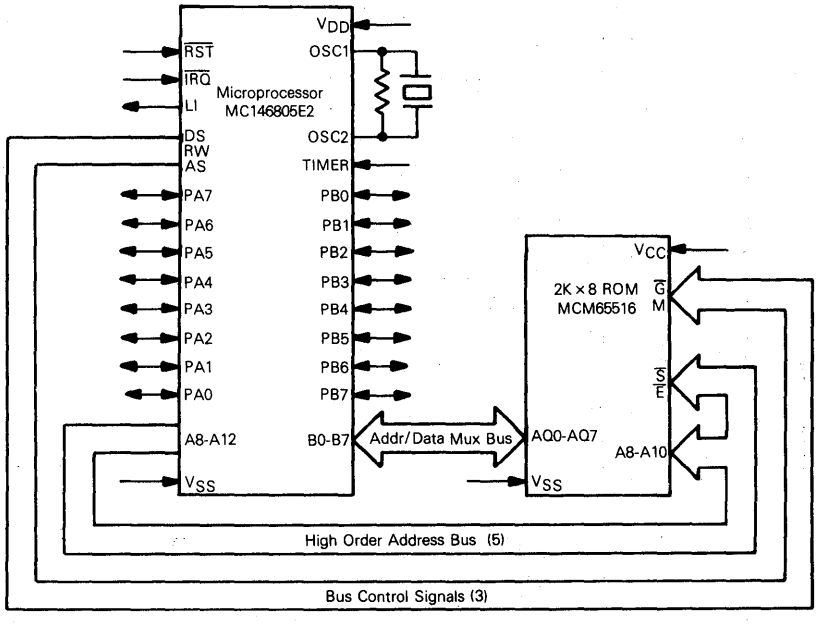
In order to operate in a multiplexed bus sytem the ROM latches, for one cycle, the address and chip select input information on the trailing edge of address strobe (M) so the address signals can be taken off the bus.

Since they are latched, the address and chip select signals have a setup and hold time referenced to the negative edge of address strobe. Address strobe has a minimum pulse width requirement since the circuit is internally precharged during this time and is setup for the next cycle on the trailing edge of address strobe. Access time is measured from the negative edge of address strobe.

The part is equipped with a data strobe input (G) which controls the output of data onto the bus lines after the addresses are off the bus. The data strobe has three potential modes of operation which are programmable with the ROM array. The first mode is termed the MOTEL mode of operation. In this mode, the circuit can work with either the Motorola or Intel type microprocessor series. The difference between the two series for a ROM peripheral is only the polarity of the data strobe signal. Therefore, in the MOTEL mode the ROM recognizes the state of the data strobe signal at the trailing edge of address strobe (requires a setup and hold time), latches the state into the circuit after address strobe, and turns on the data outputs when an opposite polarity signal appears on the data strobe input. In this manner the data strobe input can work with either polarity signal but that signal must toggle during a cycle to output data on the bus lines. If the data strobe remains at a d.c. level the outputs will remain off. The data strobe input has two other programmable modes of operation and those are the standard static select modes (high or low) where a d.c. input not synchronous with the address strobe will turn the outputs on or off.

The chip enable and chip select inputs are all programmable with the ROM array to either a high or low select. The chip select acts as an additional address and is latched on the address strobe trailing edge. On deselect the chip select merely turns off the output drivers acting as an output disable. It does not power down the chip. The chip enable inputs, however, do put the chip in a power down standby mode but they are not latched with address strobe and must be maintained in a d.c. state for a full cycle.

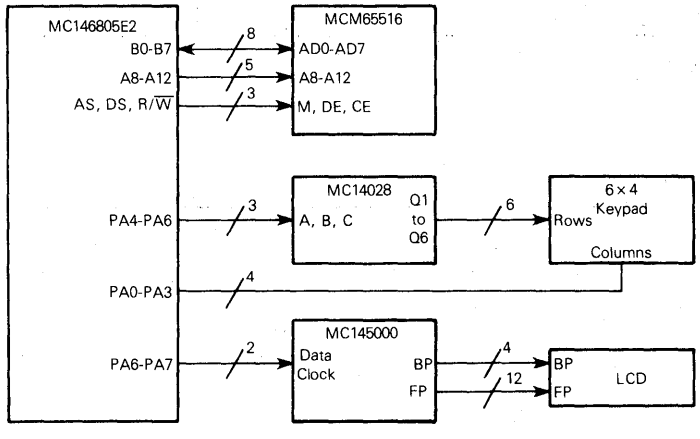
FIGURE 1
TYPICAL MINIMUM SYSTEM — MOTOROLA



INTRODUCTION

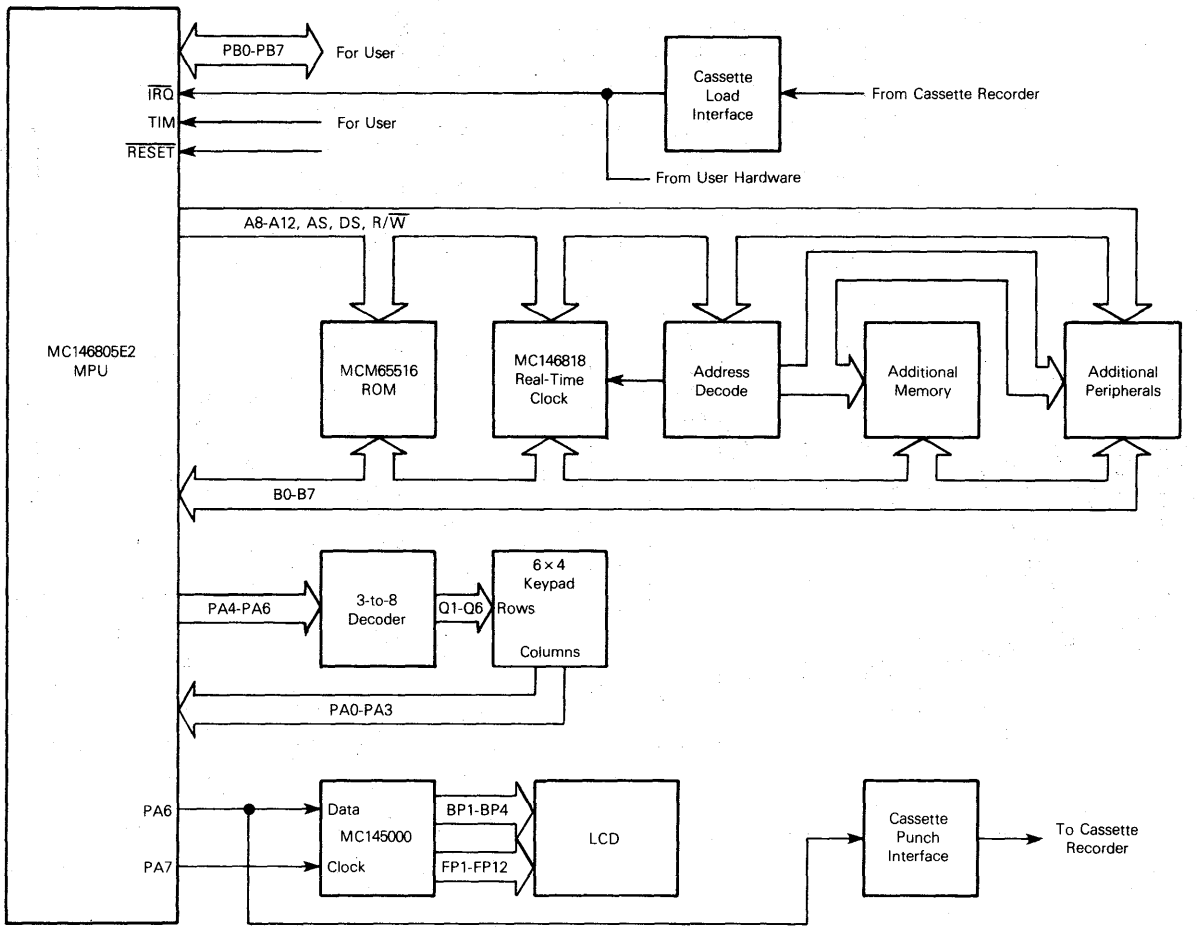
CBUG05 is a debug monitor program written for the MC146805E2 Microprocessor Unit and contained in the MCM65516 2K x 8 CMOS ROM. CBUG05 allows for rapid development and evaluation of hardware and M6805 Family type software, using memory and register examine/change commands as well as breakpoint and single instruction trace commands. CBUG05 also includes software to set and display time, using an optional MC146818 Real-Time Clock (RTC), and routines to punch and load an optional cassette interface. Figure 2 shows a minimum system which only requires the MPU, ROM, keypad inputs and display output interfaces. Port A of the MC146805E2 MPU is required for the I/O; however, Port B and all other MC146805E2 MPU features remain available to the user. A possible expanded system is shown in Figure 3. If additional information is required, please refer to Application Note AN-823 — "CBUG05 Debug Monitor Program for MC146805E2 Microprocessor Unit."

FIGURE 2 — MINIMUM CBUG05 SYSTEM



ROM

FIGURE 3 — EXPANDED CBUG05 SYSTEM



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM65516 the customer may specify the content of the memory and the method of enabling the outputs, or selection of the "MOTEL" option (Pin 17).

Information on the general options of the MCM65516 should be submitted on an Organizational Data form such as that shown in the below figure.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs
   One 16K (MCM2716, or TMS2716).
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character code. Motorola's R.O.M.S. format.

FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only

Quote: _____

Part No.: _____

Specif. No.: _____

Programmable Pin Options:

	13	14	16	17
Active High	☐	☐	☐	☐
Active Low	☐	☐	☐	☐

MOTEL ☐

ROM

MOTOROLA

MCM68A316E

MOS

(N-CHANNEL, SILICON-GATE)

2048 X 8 BIT
READ ONLY MEMORY

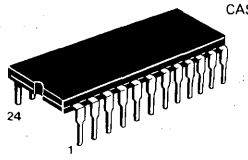
2048 X 8 BIT READ ONLY MEMORY

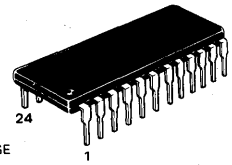
The MCM68A316E is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refeshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

- Fully Static Operation
- Three-State Data Output
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ±10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns
- Plug-in Compatible with 2316E
- Pin Compatible with 2708 and TMS2716 EPROMs

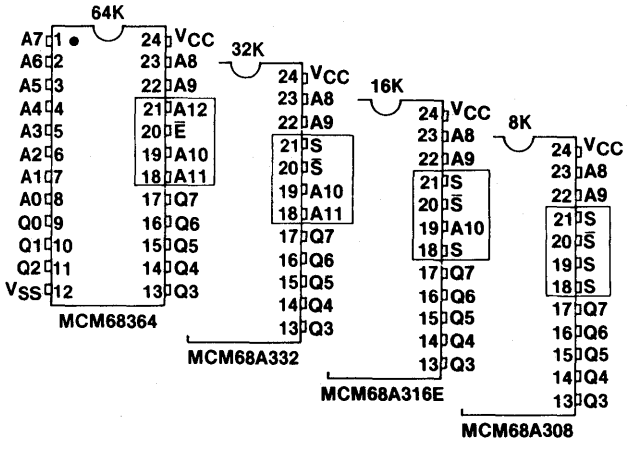
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623





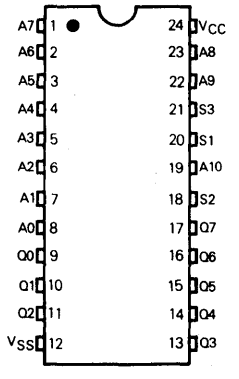
P SUFFIX
PLASTIC PACKAGE
CASE 709

MOTOROLA'S PIN-COMPATIBLE ROM FAMILY



INDUSTRY STANDARD PINOUTS

PIN ASSIGNMENT



PIN NAMES	
A0-A10	Address Inputs
S1-S3	Chip Selects
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

ROM

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	-2.5	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	Vdc
Output Leakage Current (Three-State) (S = 0.8 V or $\overline{S}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	-10	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	130	mAdc

ABSOLUTE MAXIMUM RATINGS (See Note 1)

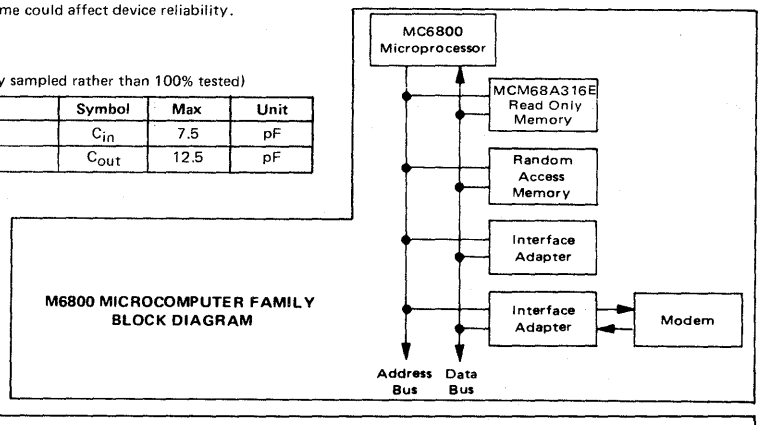
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

CAPACITANCE

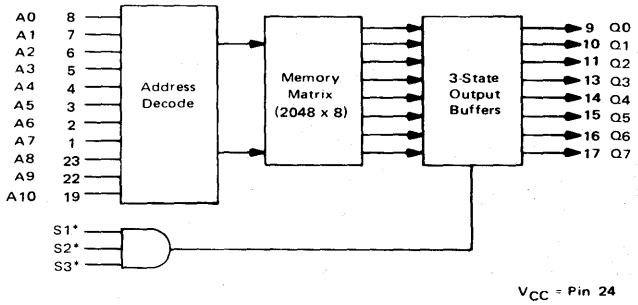
(f = 2.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF



M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

BLOCK DIAGRAM

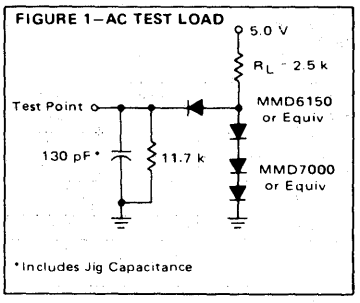


* Active level defined by the user.

V_{CC} = Pin 24
Gnd = Pin 12

ROM

FIGURE 1—AC TEST LOAD



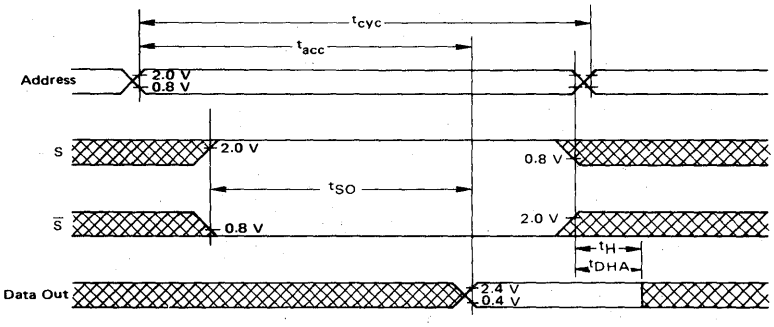
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.
All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Access Time	t_{acc}	–	350	ns
Chip Select to Output Delay	t_{SO}	–	150	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Deselection	t_H	10	150	ns

TIMING DIAGRAM



ROM

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A316E, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A316E should be submitted on an Organizational Data form such as that shown in Figure 2. ("No-Connect" must always be the highest order Chip Select(s).)

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROM (TMS2716 or MCM2716)
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character code. Motorola's R.O.M.S. format.

FIGURE 2 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A316E MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

Chip Select:	Active High	Active Low	No Connect
S1	☐	☐	☐
S2	☐	☐	☐
S3	☐	☐	☐

ROM

MOTOROLA

MCM68A332

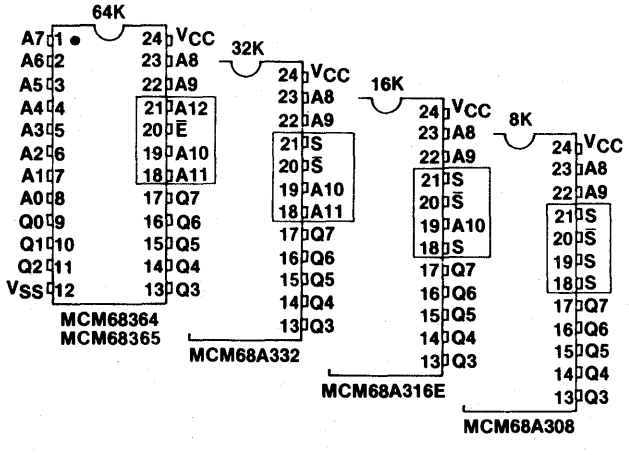
4096 X 8-BIT READ ONLY MEMORY

The MCM68A332 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

- Fully Static Operation
- Three-State Data Output for OR-Ties
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ±10% 5-Volt Power Supply
- Fully TTL Compatible
- Maximum Access Time = 350 ns
- Directly Compatible with 4732
- Preprogrammed MCM68A332-2 Available

MOTOROLA'S PIN-COMPATIBLE ROM FAMILY

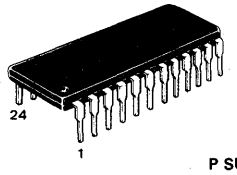


INDUSTRY STANDARD PINOUTS

MOS

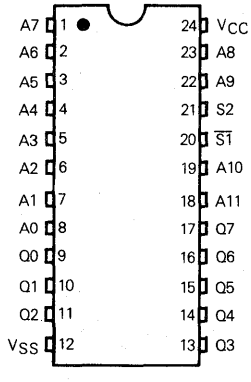
(N-CHANNEL, SILICON-GATE)

4096 X 8-BIT
READ ONLY MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 709

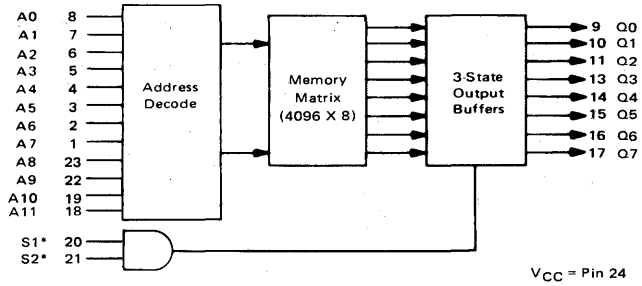
PIN ASIGNMENT



PIN NAMES	
A0-A11	Address Inputs
$\overline{S1}$, S2	Programmable Chip Selects
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

ROM

BLOCK DIAGRAM



* Active level defined by the user.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved.)	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	−2.5	2.5	μAdc
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	Vdc
Output Leakage Current (Three-State) (S = 0.8 V or $\overline{S}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	−10	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	80	mAdc

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

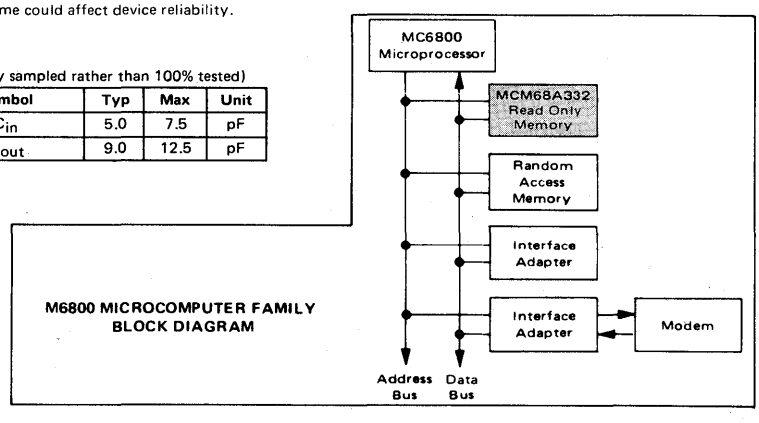
NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

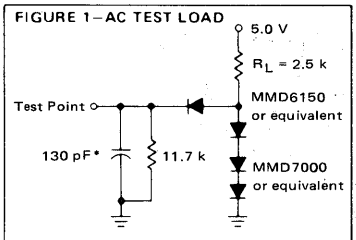
Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	5.0	7.5	pF
Output Capacitance	C_{out}	9.0	12.5	pF



M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

ROM

FIGURE 1–AC TEST LOAD



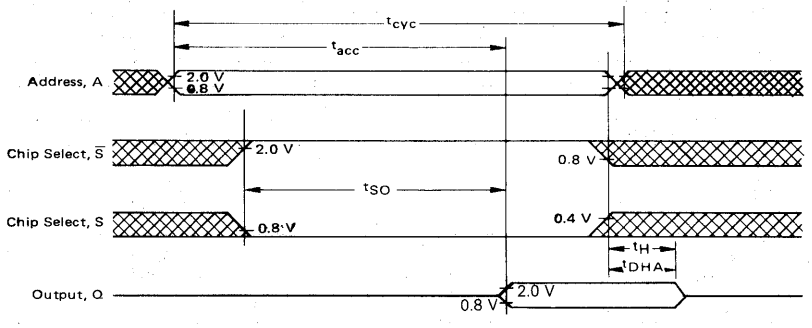
*Includes jig capacitance

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.
All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Access Time	t_{acc}	–	350	ns
Chip Select to Output Delay	t_{SO}	–	150	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Deselection	t_H	10	150	ns

TIMING DIAGRAM



Waveform Symbol	Input	Output	Waveform Symbol	Input	Output	Waveform Symbol	Input	Output
———	MUST BE VALID	WILL BE VALID	▨	DON'T CARE ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN	⟋⟍	–	HIGH IMPEDANCE

ROM

MCM68A332 CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A332, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A332 should be submitted on an Organizational Data form such as that shown in Figure 2. (A "No-Connect" or "Don't Care" must always be the highest order Chip Select(s).)

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs—two 16K (MCM2716 or TMS2716)
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character Code. Motorola;s R.O.M.S. format.

PRE-PROGRAMMED MCM68A332P2

The −2 standard ROM pattern contains sine-lookup and arctan-lookup tables.

Locations 0000 through 2001 contain the sine values. The sine's first quadrant is divided into 1000 parts with sine values corresponding to these angles stored in the ROM. Sin $\pi/2$ is included and is rounded to 0.9999.

The arctan values contain angles in radians corresponding to the arc tangents of 0 through 1 in steps of 0.001 and are contained in locations 2048 through 4049.

Locations 2002 through 2047 and 4050 through 4095 are zero filled.

All values are represented in absolute decimal format with four digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the two least significant digits in the upper byte. The decimal point is assumed to be to the left of the most significant digit.

Example: $\sin\left(\frac{1}{1000}\ \frac{\pi}{2}\right) = 0.0016$ decimal

Address	Contents
0002	0000 0000
0003	0001 0110

FIGURE 2 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A332 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only

Quote _____

Part No. _____

Specif. No. _____

Chip Select Options:	Active High	Active Low	No-Connect
S1	☐	☐	☐
S2	☐	☐	☐

ROM

MOTOROLA

MCM68364

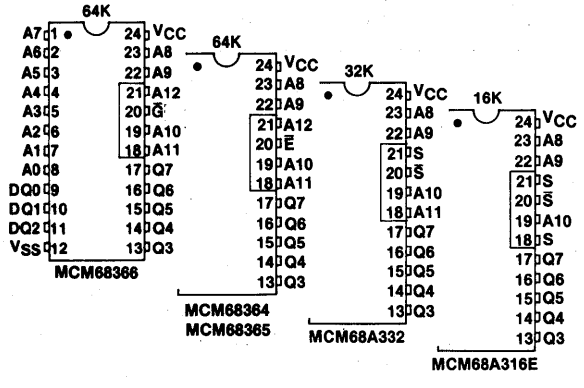
64K-BIT READ ONLY MEMORY

The MCM68364 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, and is TTL compatible. The addresses are latched with the Chip Enable input – no external latches required.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Single ±10% 5-Volt Power Supply
- Automatic Power Down
- Low Power Dissipation
  - 150 mW active (typical)
  - 35 mW standby (typical)
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- TTL Compatible
- Maximum Access Time
  - 200 ns – MCM68364-20
  - 250 ns – MCM68364-25
  - 300 ns – MCM68364-30
- Pin Compatible with 8K – MCM68A308, 16K – MCM68A316E, and 32K – MCM68A332 Mask-Programmable ROMs
- Pin Compatible with 24-pin 64K EPROM MCM68764

MOTOROLA'S PIN COMPATIBLE ROM FAMILY

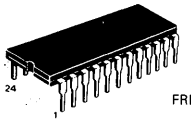


INDUSTRY STANDARD PIN-OUTS

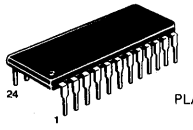
MOS

(N-CHANNEL, SILICON-GATE)

8192 × 8-BIT
READ ONLY MEMORY

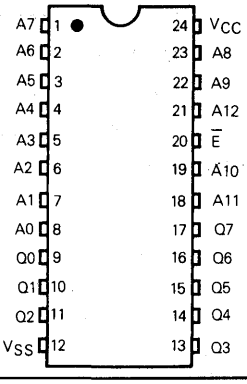


C SUFFIX
FRIT-SEAL PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT

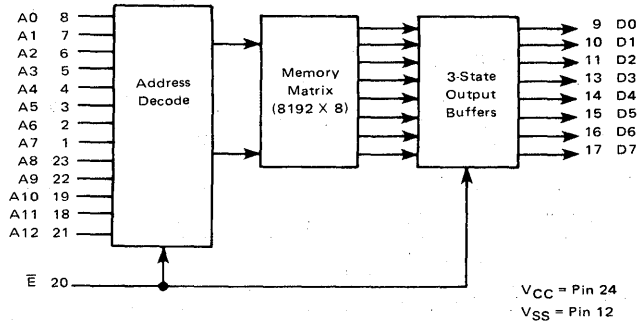


PIN NAMES	
A0-A12	Address
$\overline{E}$	Chip Enable
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ROM

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{in}	−0.5 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved, $\overline{E} = V_{IH}$)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V

DC OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	-10	—	10	μA
Output High Voltage (I_{OH} = -220 μA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	—	—	0.4	V
Output Leakage Current (Three-State) ($\overline{E}$ = 2.0 V, V_{out} = 0 V to 5.5 V)	I_{LO}	-10	—	10	μA
Supply Current — Active* (Minimum Cycle Rate)	I_{CC}	—	25	40	mA
Supply Current — Standby ($\overline{E}$ = V_{IH})	I_{SB}	—	7	10	mA

*Current is proportional to cycle rate.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	8	pF
Output Capacitance	C_{out}	15	pF

ROM

AC OPERATING CONDITIONS AND CHARACTERISTICS

Read Cycle

RECOMMENDED AC OPERATING CONDITIONS

(T_A = 0 to 70°C, V_{CC} = 5.0 V ±10%. All timing with $t_r = t_f = 20$ ns, loads of Figure 1)

Parameter	Symbol		MCM68364-20		MCM68364-25		MCM68364-30		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Chip Enable Low to Chip Enable Low of Next Cycle (Cycle Time)	t_{ELEL}	t_{CYC}	300	–	375	–	450	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	t_{EW}	200	–	250	–	300	–	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	t_{EA}	–	200	–	250	–	300	ns
Chip Enable High to Output High Z (Off Time)	t_{EHQZ}	t_{EHZ}	10	60	–	60	–	75	ns
Chip Enable Low to Address Don't Care (Hold)	t_{ELAX}	t_{AH}	60	–	60	–	75	–	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns
Chip Enable Precharge Time	t_{EHEL}	t_{EP}	100	–	125	–	150	–	ns

TIMING DIAGRAM

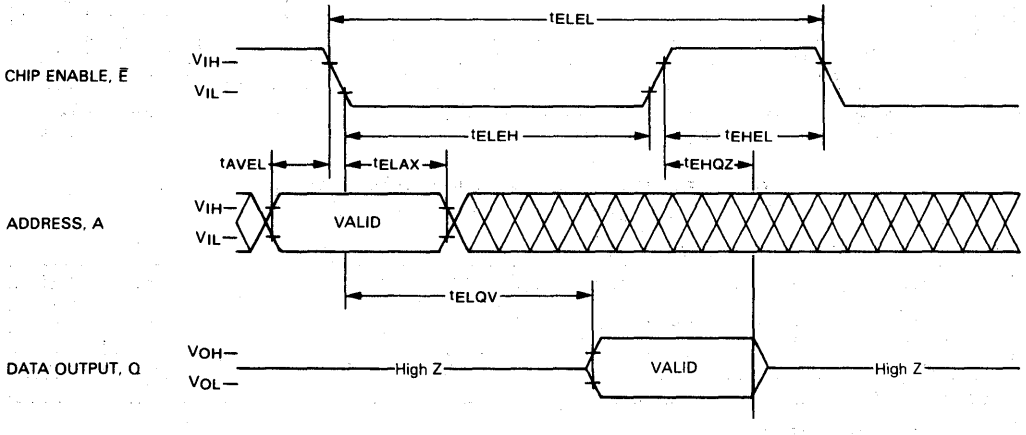
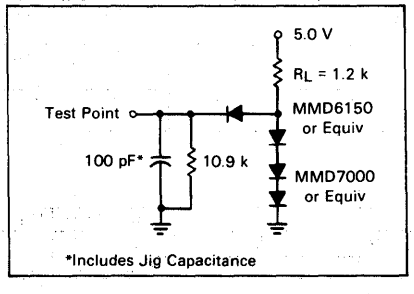


FIGURE 1 – AC TEST LOAD



WAVEFORMS

Waveform Symbol	Input	Output
———	MUST BE VALID	WILL BE VALID
▨	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
▨	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
▨	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
———		HIGH IMPEDANCE

ROM

PRODUCT DESCRIPTION

This Motorola MOS Read Only Memory (ROM), the MCM68364, is a clocked or edge enabled device. It makes use of virtual ground ROM cells and clocked peripheral circuitry, allowing a better speed-power product.

The MCM68364 has a period during which the non-static periphery must undergo a precharge. Therefore, the cycle time is slightly longer than the access time. It is essential that the precharge requirements are met to ensure proper address latching and avoid invalid output data. Once the address hold time has been met, new address information can be supplied in preparation for the next cycle.

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68364, the customer may specify the contents of the memory.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs – one 64K (MCM68764), two 32K, or four 16K (MCM2716 or TMS2716).
2. Magnetic Tape – 9 Track, 800 bpi, odd parity written in EBCDIC character code. Motorola's R.O.M.S. format.

PRE-PROGRAMMED MCM68364P25-3

The –3 standard ROM pattern contains log (base 10) and antilog (base 10) lookup tables for the 64K ROM.

Locations 0000 through 3599 contain log base 10 values. The arguments for the log table range from 1.00 through 9.99 incrementing in steps of 1/100. Each log value is represented by an eight-digit decimal number with decimal point assumed to be to the left of the most significant digit.

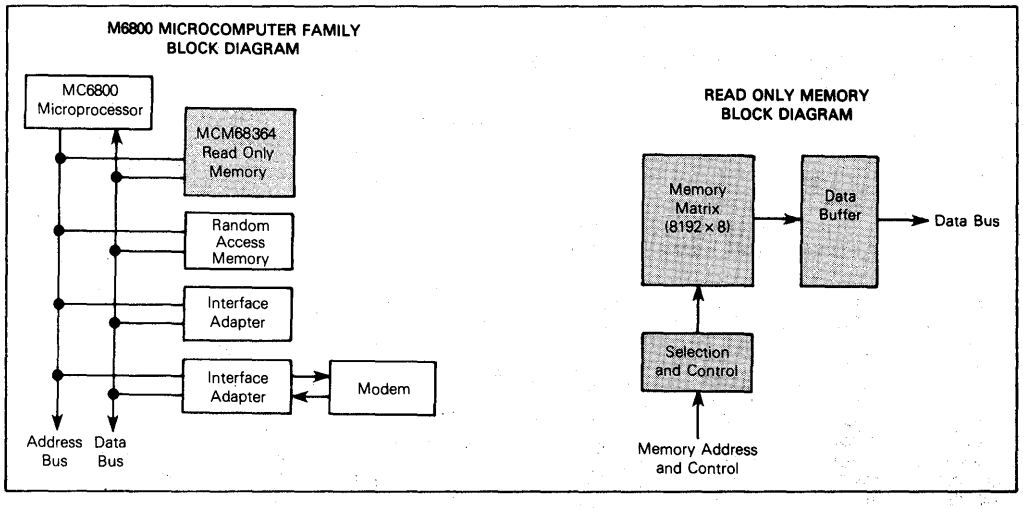
Antilog (base 10) are stored in locations 4096 through 8095. The arguments range from .000 through .999 incrementing in steps of 1/1000. Each antilog value is represented by an eight-digit decimal number with decimal point assumed to be to the right of the most significant digit.

Locations 3600 through 4095 and 8096 through 8191 are zero filled.

All values are represented in absolute decimal format with eight digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the remaining six digits in the three consecutive locations.

Example:
$\log_{10}(1.01) = .00432137$ decimal

Address	Contents	
4	0000	0000
5	0100	0011
6	0010	0001
7	0011	0111



ROM

MOTOROLA

MCM68365

64K BIT READ ONLY MEMORY

The MCM68365 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL, and needs no clocks or refreshing due to its static operation.

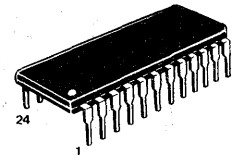
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The active level of the Chip Enable input and the memory content are defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Fully Static Operation
- Automatic Power Down
- Low Power Dissipation — 125 mW Active (Typical)
  25 mW Standby (Typical)
- Single ±10% 5-Volt Power Supply
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Enable
- TTL Compatible
- Maximum Access Time — 250 ns — MCM68365-25
  300 ns — MCM68365-30
  350 ns — MCM68365-35
- Pin Compatible with 16K — MCM68A316E and 32K — MCM68A332, 64K — MCM68364, MC68366 Mask-Programmable ROMs

MOS

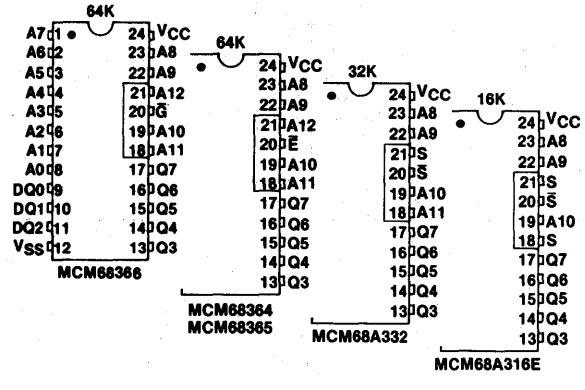
(N-CHANNEL, SILICON-GATE)

8192 × 8-BIT
READ ONLY MEMORY

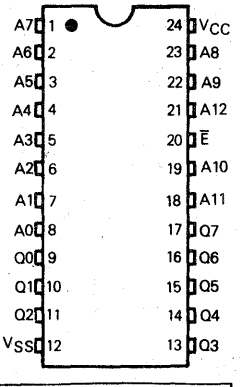


P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN COMPATIBLE ROM FAMILY
(INDUSTRY STANDARD PIN-OUTS)



PIN ASSIGNMENT

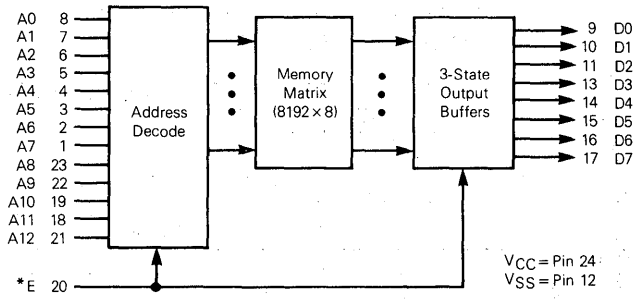


PIN NAMES	
A0-A12	Address
E	Chip Enable
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ROM

BLOCK DIAGRAM



*Active level defined by the user.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−1.0 to +7.0	V
Input Voltage	V_{in}	−1.0 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V	–
Input High Voltage	V_{IH}	2.0	–	5.5	V	–
Input Low Voltage	V_{IL}	−0.5	–	0.8		

DC OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	−10	–	10	μA	1
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	–	V	–
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	–	–	0.4	V	–
Output Leakage Current (Three-State) ($\overline{E}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	−10	–	10	μA	2
Supply Current — Active (V_{CC} = 5.5 V)	I_{CC}	–	25	60	mA	3
Supply Current — Standby (V_{CC} = 5.5 V)	I_{SB}	–	4	15	mA	4

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

Notes: 1. Measured a) forcing V_{CC} on one input pin at a time while all others are grounded, and
b) maintaining 0.0 V on one pin at a time while all others are at V_{CC} = 4.5 V and 5.5 V.
2. Measured a) with A0-A12 = V_{SS} and forcing 0.4 V on one output at a time while all others are held at 2.4 V, and
b) with A0-A12 = V_{SS} and forcing 2.4 V on one output at a time while all others are held at 0.4 V (V_{CC} = 4.5 V and 5.5 V)
3. Measured with the Chip Enabled ($\overline{E}$ = V_{IL}) addresses cycling, and the output unloaded.
4. Measured with the Chip Disabled ($\overline{E}$ = V_{IH}) and the outputs unloaded.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

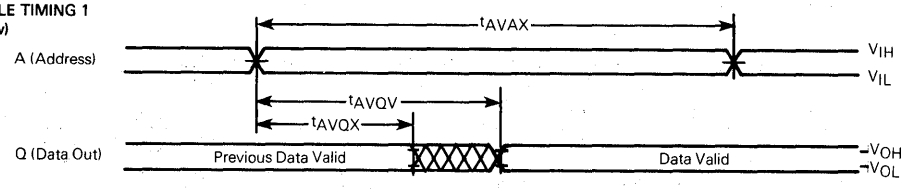
READ CYCLE (See Notes 5, 6)

Parameter	Symbol		MCM68365-25		MCM68365-30		MCM68365-35		Units
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Chip Enable is held Active)	t_{AVAX}	t_{CYC}	250	–	300	–	350	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	t_{EW}	250	–	300	–	350	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	t_{AA}	–	250	–	300	–	350	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	t_{EA}	–	250	–	300	–	350	ns
Address Valid to Output Invalid	t_{AVQX}	t_{DHA}	20	–	20	–	20	–	ns
Chip Enable Low to Output Invalid	t_{ELQX}	t_{ELZ}	10	–	10	–	10	–	ns
Chip Enable High to Output High-Z	t_{EHQZ}	t_{EHZ}	10	80	10	80	10	80	ns
Chip Selection to Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{EHICCL}	t_{PD}	–	100	–	100	–	120	ns

Notes: 5. Chip Enable ($\overline{E}$) is represented as active low for illustrative purposes.

6. AC Test Conditions
   Input Transition Times: 5 ns ≤ $t_r = t_f$ ≤ 20 ns
   Temperature: T_A = 0°C to 70°C
   Load Shown in Figure 1
   V_{CC} = 5.0 V ± 10%
   Input Pulse Levels: V_{IL} = −0.5 V to 0.8 V
   V_{IH} = 2.0 V to V_{CC}
   Measurement Levels: Input = 1.5 V
   Output Low = 0.8 V
   Output High = 2.0 V

READ CYCLE TIMING 1
($\overline{E}$ Held Low)



READ CYCLE TIMING 2

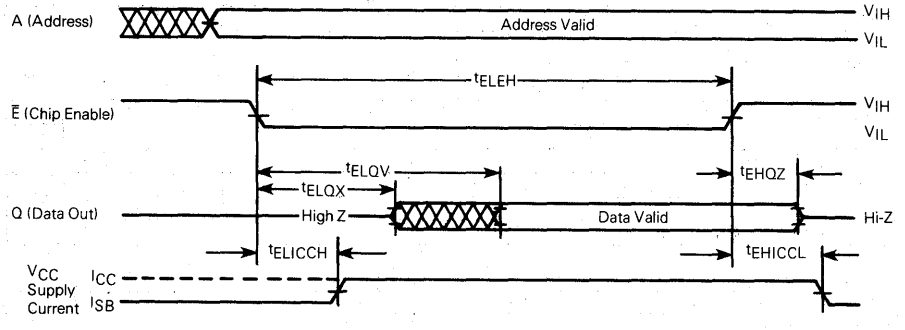
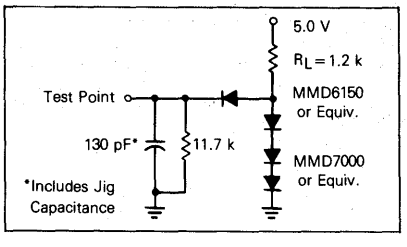


FIGURE 1 — AC TEST LOAD



ROM

FIGURE 2 — ADDRESS ACCESS TIME VERSUS TEMPERATURE

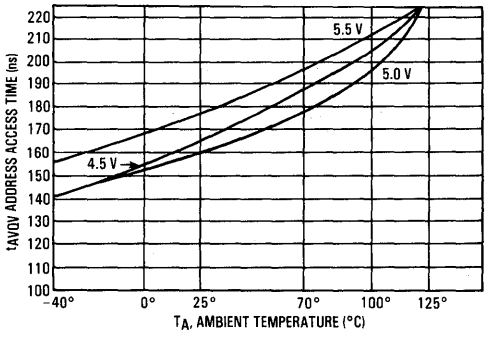


FIGURE 3 — I_{CC} SUPPLY CURRENT VERSUS TEMPERATURE

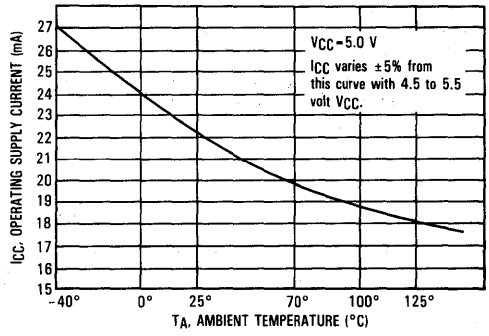
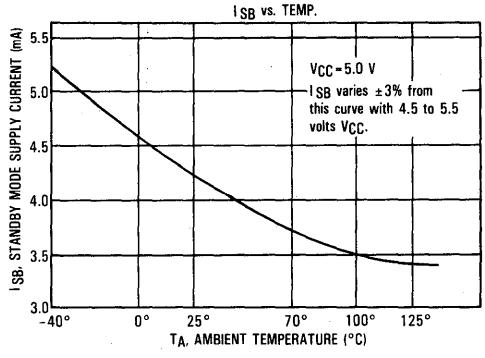


FIGURE 4 — I_{SB} STANDBY CURRENT VERSUS TEMPERATURE



PRE-PROGRAMMED MCM68365P35-3, P30-3, P25-3

The −3 standard ROM pattern contains log (base 10) and antilog (base 10) lookup tables for the 64K ROM.

Locations 0000 through 3599 contain log base 10 values. The arguments for the log table range from 1.00 through 9.99 incrementing in steps of 1/100. Each log value is represented by an eight-digit decimal number with decimal point assumed to be to the left of the most-significant digit.

Antilog (base 10) are stored in locations 4096 through 8095. The arguments range from 0.000 through 0.999 incrementing in steps of 1/1000. Each antilog value is represented by an eight-digit decimal number with decimal point assumed to be to the right of the most-significant digit.

Locations 3600 through 4095 and 8096 through 8191 are zero filled.

All values are represented in absolute decimal format with eight digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the remaining six digits in the three consecutive locations.

Example: $\log_{10}(1.01) = 0.00432137$ decimal

Address	Contents	
4	0000	0000
5	0100	0011
6	0010	0001
7	0011	0111

ROM

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68365, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68365 should be submitted on an Organizational Data form such as that shown in Figure 5.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs – One 64K or two 32K.
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character code. Motorola R.O.M.S. format.

FIGURE 5 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68365 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No: _____

Specif. No: _____

Enable Options:

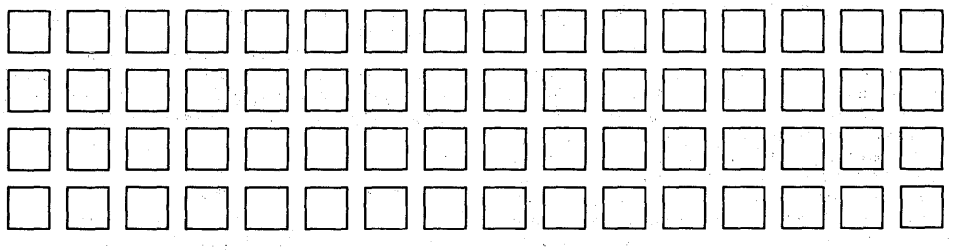
	Active High	Active Low
Chip Enable	☐	☐

Device Marking Requirements

The customer marking requirements are restricted to these limits:

1) Four lines maximum (including date code)

2) Not more than 16 characters per line



ROM

MOTOROLA

MCM68366

64K BIT READ ONLY MEMORY

The MCM68366 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and needs no clocks or refreshing due to its static operation.

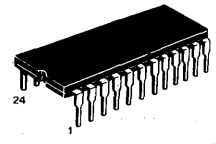
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The active level of the Output Enable input and the memory content is defined by the user. The Output Enable input deselects the output.

- Fully Static Operation
- Fast Data Valid Time for High Speed Microprocessors
- Low Power Dissipation — 125 mW Active (Typical)
- Single ±10% 5-Volt Power Supply
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- Mask Programmable Output Enable
- TTL Compatible
- Maximum Access Time — 150 ns from Output Enable
  250 ns from Address — MCM68366-25
  300 ns from Address — MCM68366-30
  350 ns from Address — MCM68366-35
- Pin Compatible with 8K, 16K, and 32K — Mask-Programmable ROMs
- Pin Compatible with MCM68766 64K EPROM

MOS

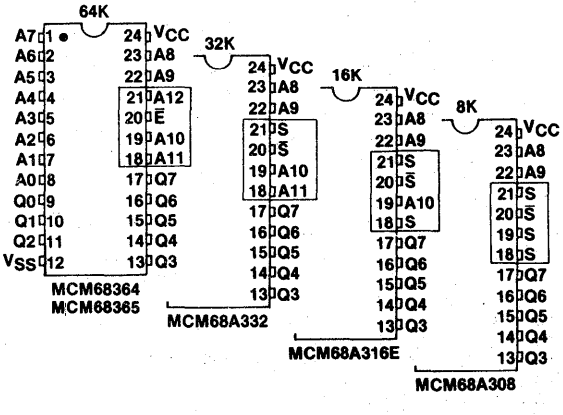
(N-CHANNEL, SILICON-GATE)

8192 × 8-BIT
READ ONLY MEMORY

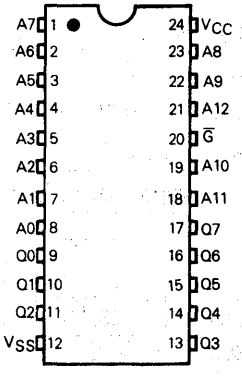


P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN COMPATIBLE ROM FAMILY
(INDUSTRY STANDARD PIN-OUTS)



PIN ASSIGNMENT

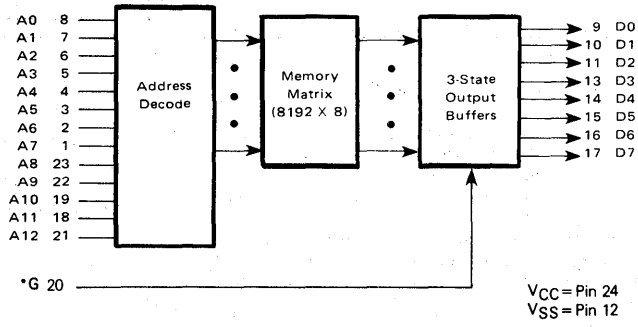


PIN NAMES	
A0-A12	Address
G	Output Enable
Q0-Q7	Data Output
VCC	+5 V Power Supply
VSS	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ROM

BLOCK DIAGRAM



*Active Level Defined by the User

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−1.0 to +7.0	V
Input Voltage	V_{in}	−1.0 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V	–
Input High Voltage	V_{IH}	2.0	–	5.5	V	–
Input Low Voltage	V_{IL}	−0.5	–	0.8		

DC OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	−10	–	10	μA	1
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	–	V	–
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	–	–	0.4	V	–
Output Leakage Current (Three-State) ($\overline{G}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	−10	–	10	μA	2
Supply Current (V_{CC} = 5.5 V)	I_{CC}	–	25	60	mA	3

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

Notes: 1. Measured a) forcing V_{CC} on one input pin at a time, while all others are grounded, and
b) maintaining 0.0 V on one pin at a time, while all others are at V_{CC} = 4.5 V and 5.5 V.
2. Measured a) with A0-A12 = V_{SS} and forcing 0.4 V on one output at a time while all others are held at 2.4 V, and
b) with A0-A12 = V_{SS} and forcing 2.4 V on one output at a time while all others are held at 0.4 V (V_{CC} = 4.5 V and 5.5 V).
3. Measured with the Output Enabled ($\overline{G}$ = V_{IL}), addresses cycling and the outputs unloaded.

ROM

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

READ CYCLE (See Notes 4, 5)

Parameter	Symbol		MCM68366-25		MCM68366-30		MCM68366-35		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Output Enable is Held Active)	t_{AVAX}	t_{CYC}	250	–	300	–	350	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	t_{AA}	–	250	–	300	–	350	ns
Output Enable Low to Output Valid (Access) (Note 6)	t_{GLQV}	t_{GA}	–	150	–	150	–	150	ns
Address Valid to Output Invalid	t_{AVQX}	t_{DHA}	10	–	10	–	10	–	ns
Output Enable Low to Output Invalid	t_{GLQX}	t_{GLZ}	10	–	10	–	10	–	ns
Output Enable High to Output High Z	t_{GHQZ}	t_{GHZ}	0	80	0	80	0	80	ns
Address Valid to Output Enable Low (Note 7)	t_{AVGL}	t_{AS}	100	–	150	–	200	–	ns

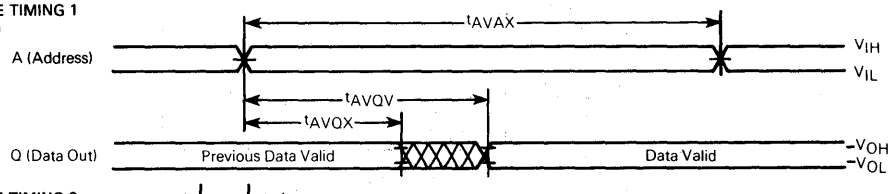
Notes: 4. Output Enable ($\overline{G}$) is represented as active low for illustrative purposes.

5. AC Test Conditions
   Input Transition Times: 5 ns ≤ $t_r = t_f$ ≤ 20 ns
   Temperature: T_A = 0°C to 70°C
   Load Shown in Figure 1
   V_{CC} = 5.0 V ± 10%
   Input Pulse Levels: V_{IL} = −0.5 V to 0.8 V
   V_{IH} = 2.0 V to V_{CC}
   Measurement Levels: Input = 1.5 V
   Output Low = 0.8 V
   Output High = 2.0 V

6. t_{GLQV} = 120 ns is also available.

7. A faster minimum time is allowed, but the timing must then be referenced to t_{AVQV} and t_{AVQX}.

READ CYCLE TIMING 1
($\overline{G}$ Held Low)



READ CYCLE TIMING 2

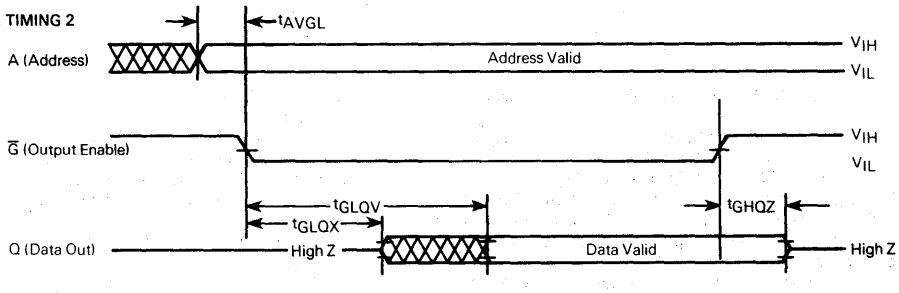
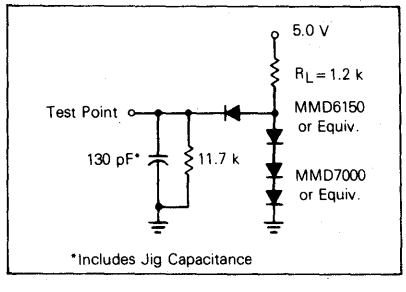


FIGURE 1 — AC TEST LOAD



ROM

FIGURE 2 – ADDRESS ACCESS TIME VERSUS TEMPERATURE

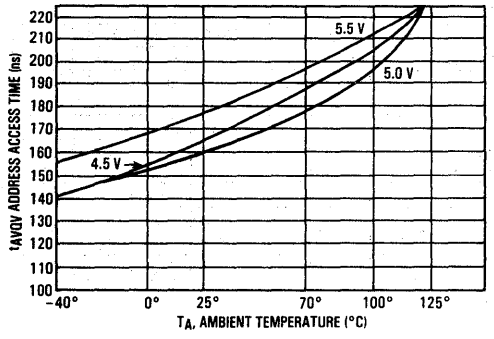


FIGURE 3 – I_{CC} SUPPLY CURRENT VERSUS TEMPERATURE

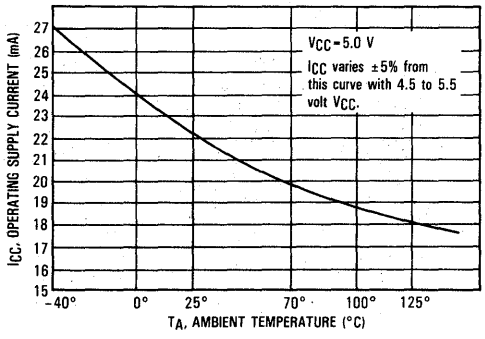
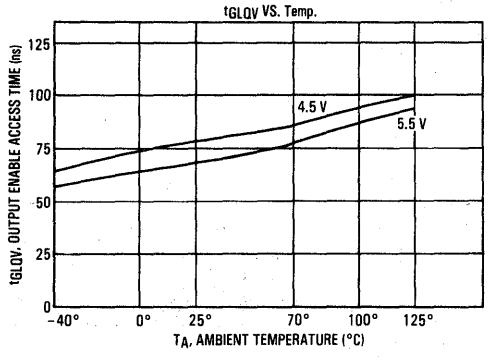


FIGURE 4 – OUTPUT ENABLE ACCESS VERSUS TEMPERATURE



PRE-PROGRAMMED MCM68366P35-3, P30-3, P25-3

The –3 standard ROM pattern contains log (base 10) and antilog (base 10) lookup tables for the 64K ROM.

Locations 0000 through 3599 contain log base 10 values. The arguments for the log table range from 1.00 through 9.99 incrementing in steps of 1/100. Each log value is represented by an eight-digit decimal number with decimal point assumed to be to the left of the most-significant digit.

Antilog (base 10) are stored in locations 4096 through 8095. The arguments range from 0.000 through 0.999 incrementing in steps of 1/1000. Each antilog value is represented by an eight-digit decimal number with decimal point assumed to be to the right of the most-significant digit.

Locations 3600 through 4095 and 8096 through 8191 are zero filled.

All values are represented in absolute decimal format with eight digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the remaining six digits in the three consecutive locations.

Example: $\log_{10}(1.01) = 0.00432137$ decimal

Address	Contents	
4	0000	0000
5	0100	0011
6	0010	0001
7	0011	0111

ROM

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68366, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68366 should be submitted on an Organizational Data form such as that shown in Figure 5.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs — one 64K or two 32K.
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character Code. Motorola's R.O.M.S. format.

FIGURE 5 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68366 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No: _____

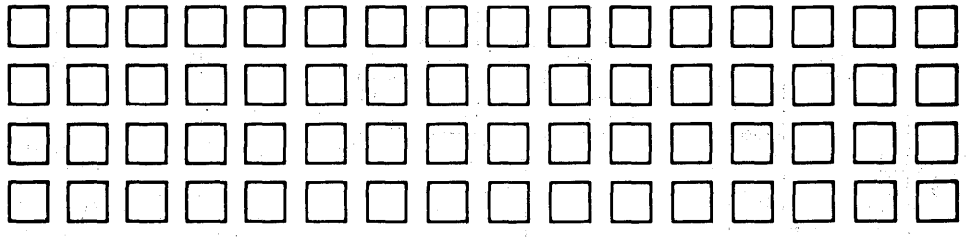
Specif. No: _____

Enable Options:

	Active High	Active Low
Output Enable	☐	☐

Device Marking Requirements

The customer marking requirements are resetricted to these limits:
1) Four lines maximum (including date code)
2) Not more than 16 characters per line



ROM

MOTOROLA

MCM68367

Advance Information

MOS

(N-CHANNEL, SILICON-GATE)

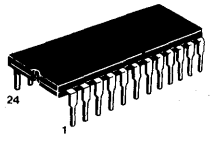
8192 × 8-BIT READ ONLY MEMORY (PAGE MODE)

64K BIT READ ONLY MEMORY

The MCM68367 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and needs no clocks or refreshing due to its static operation.

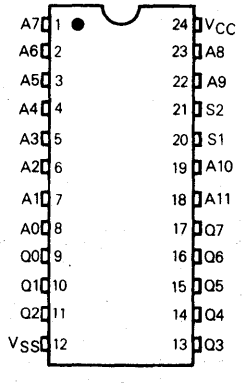
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. This 8K × 8-bit ROM is organized into two 4K pages that are accessed by two user defined address codes. The active level of the Chip Select inputs and the memory content are defined by the user. The Chip Select inputs deselect the output.

- Fully Static Operation
- Fast Data Valid Time for High Speed Microprocessors
- Page-Mode Organized Memory
- Low Power Dissipation — 125 mW Active (Typical)
- Single ±5% 5-Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Selects
- TTL Compatible



P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT

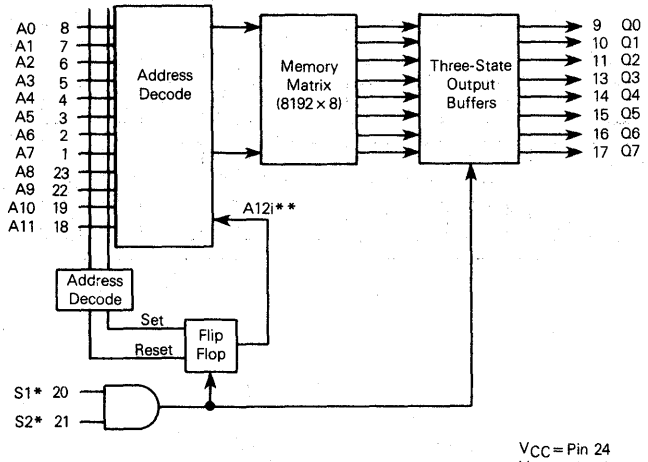


PIN NAMES

A0-A11	Address
S1, S2	Chip Select
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FIGURE 1 — BLOCK DIAGRAM



* Active Level Defined by User
** A12i — High Order Address Not User Accessible

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ROM

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−1.0 to +7.0	V
Input Voltage	V_{in}	−1.0 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Note: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.75	5.0	5.25	V	–
Input High Voltage	V_{IH}	2.2	–	V_{CC}	V	–
Input Low Voltage	V_{IL}	−0.5	–	0.8		

DC OPERATING CHARACTERISTICS

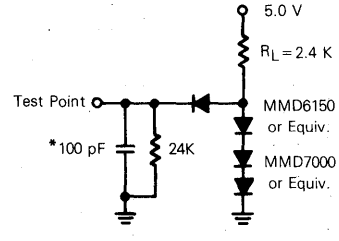
Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Input Current (V_{in} = 0 to 5.25 V, V_{CC} = 4.75 to 5.25 V)	I_{in}	−10	–	10	μA	2
Output High Voltage (I_{OH} = −100 μA)	V_{OH}	2.4	–	–	V	–
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V	–
Output Leakage Current (Three-State) (S1, S2 = 0.8 V, V_{out} = 0.4 to 2.4 V, V_{CC} = 4.75 to 5.25 V)	I_{LO}	−10	–	10	μA	3
Supply Current (V_{CC} = 5.25 V)	I_{CC}	–	25	100	mA	4

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

Notes: 2. Measured a) forcing V_{CC} on one input pin at a time, while all others are grounded (V_{SS}), and
b) maintaining 0.0 V (V_{SS}) on one pin at a time, while all others are at V_{CC} = 4.75 V and 5.25 V.
3. Measured a) with A0-A11 = V_{SS} and forcing 0.4 V on one output at a time while all others are held at 2.4 V, and
b) with A0-A11 = V_{SS} and forcing 2.4 V on one output at a time while all others are held at 0.4 V (V_{CC} = 4.75 V and 5.25 V).
4. Measured with the chip selected (S1, S2 active), addresses cycling and the outputs unloaded.

FIGURE 2 — AC TEST LOAD



*Includes Jig Capacitance

ROM

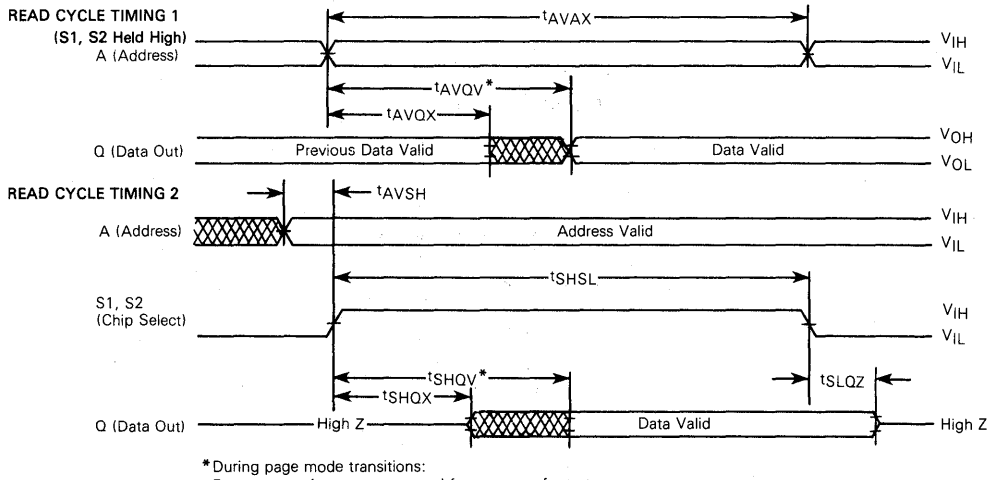
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

READ CYCLE (See Notes 5, 6)

Parameter	Symbol		Min	Max	Unit	Notes
	Standard	Alternate				
Address Valid to Address Don't Care (Cycle Time when Chip Select is Held Active)	t_{AVAX}	t_{CYC}	840	–	ns	–
Address Valid to Output Valid	t_{AVQV}	t_{AA}	–	450	ns	7
Chip Select to Output Valid	t_{SHQV}	t_{SA}	–	450	ns	7
Address Valid to Chip Select High	t_{AVSH}	t_{AS}	–	–	ns	8
Address Valid to Output Invalid	t_{AVQX}	t_{DHA}	10	–	ns	–
Chip Select to Output Invalid	t_{SHQX}	t_{SLZ}	10	–	ns	–
Chip Deselect to Output High Z	t_{SLQZ}	t_{SHZ}	0	150	ns	–
Address Valid to Output Valid During Page Transition Cycle	t_{AVQVP}	t_{AAP}	–	800	ns	9
Chip Select High to Output Valid During Page Transition Cycle	t_{SHQVP}	t_{SAP}	–	800	ns	9
Chip Select High to Chip Select Low	t_{SHSL}	t_{SW}	450	–	ns	10

Notes:
5. Chip selects S1 and S2 are represented as active high for illustrative purposes.
6. All times are guaranteed with worse case DC levels.
   Input transition times: $t_r = t_f = 15$ ns max.
   Temperature: $T_A = 0°C$ to $70°C$
   Load Shown in Figure 2
   $V_{CC} = 5.0\ V \pm 5\%$
   Input Pulse Levels: $V_{IL} = 0.8\ V$ or $-0.5\ V$
   $V_{IH} = 2.2\ V$ or $5.25\ V$
   Measurement Levels: Input = 1.5 V
   Output Low = 0.8 V
   Output High = 2.0 V
7. Except during page transition cycle.
8. $t_{AVSH} = t_{AVQV} - t_{SHQV}$
9. During a page transition, outputs are valid only for the new page. For example: "FF8" when applied in page 1 will give valid output only for page 0 (FF8). It is recommended that page 0 and page 1 have the same data for addresses FF8 and FF9.
10. During page transition cycle.



*During page mode transitions:
For t_{AVQV} refer to t_{AVQVP} and for t_{SHQV} refer to t_{SHQVP}.

ROM

FUNCTIONAL DESCRIPTION

The MCM68367 is an 8K × 8 bit "page mode" Read Only Memory (ROM) segmented into two 4K byte pages for use in systems with limited addressing capability. With this configuration, the MCM68367 looks like a 4K × 8 bit ROM from the bus operation standpoint and has the added advantage of two chip selects. The added chip select is gained by giving up the upper order address line (A12), which is normally required by an 8K × 8 ROM. To switch pages, the user inputs a certain address combination (which has been predetermined by the user and programmed into the device during wafer fabrication), which sets or resets an internal flip flop. This will cause the high order address bit A12i to be set to a logic 0 or 1 (page 0 or 1 respectively). The ROM will stay in this page until it gets the specified address combination for resetting the flip flop and toggling A12i.

Both chip selects must be active for at least 450 ns during the "page change" cycles to enable the flip flop. Also, when the device is powered up, it can come up in either page, so the user must provide one of his prechosen address combinations onto the bus to get into the desired page. After this occurs the device will stay in the page until the other programmed address combination occurs. For example, if the user wants page 0 (the lower half of the 8K memory, actually 4K) and his chosen page mode pair is FF8 and FF9 (hex), he must provide FF8 to the address line and have both chip selects active for at least 450 ns. To get to page 1, he must provide FF9.

There are eight possible pairs of address combinations which the customer can chose from and must be specified when inputting active levels of the chip selects and the bit pattern to Motorola. (See Figure 3 for the possible pairs.)

It is suggested that the data word (data output) for the predetermined decoding addresses (in this example FF8 and FF9) be set the same in both pages. That is, the output of data for FF8 in page 0 (0FF8) should be the same as FF8 in page 1 (1FF8), likewise FF9. The reason for this is that both memory word locations will be accessed in the same cycle when changing pages.

As an aid in understanding the functional operation of this device, please consult the block diagram of Figure 1.

Example of Operation:
(Mask programmable page mode pair: FF8 and FF9)

1. Power Up	Page undefined
2. Address = FF8	Part is now in page 0
3. Address = 000-3FF	Sequencing through 1K bytes on page 0
4. Address = FF9	Change to page 1
5. Address = 000-3FF	Sequencing through 1K bytes on page 1

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68367, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68367 should be submitted on an Organizational Data form such as that shown in Figure 3.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs — one 64K, two 32K.
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character Code. Motorola's R.O.M.S. format.

FIGURE 3 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68367 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No: _____

Specif. No: _____

Chip Select Options:

	Active High	Active Low
Chip Select S1	☐	☐
Chip Select S2	☐	☐

Mask Programmable Page Mode Pairs:

Page 0 A12i = 0	Page 1 A12i = 1
FF0	FF1 ☐
FF2	FF3 ☐
FF4	FF5 ☐
FF6	FF7 ☐
FF8	FF9 ☐
FFA	FFB ☐
FFC	FFD ☐
FFE	FFF ☐

MOTOROLA

MCM68368

Advance Information

64K BIT READ ONLY MEMORY

The MCM68368 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL, and needs no clocks or refreshing due to its static operation.

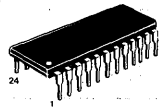
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The MCM68368 is organized into 8K × 8 with 12 address lines and a paging system which segments the memory into eight 1K banks. The active level of the Chip Select inputs and the memory content is defined by the user.

- Fully Static Operation
- Fast Data Valid Time for High Speed Microprocessors
- Bank Select Operation for Use in Address Limited Systems
- Low Power Dissipation — 200 mW Active (Typical)
- Single ±10% 5 Volt Power Supply
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Selects
- TTL Compatible
- Maximum Access Time — 200 ns from Selection
  450 ns from Address
- Pin Compatible with 8K, 16K, and 32K — Mask Programmable ROMs
- Pin Compatible with MCM68766 64K EPROM

MOS

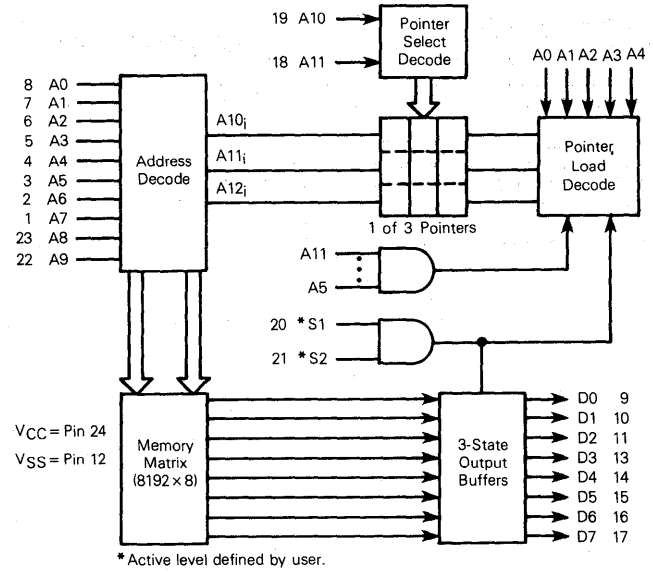
(N-CHANNEL, SILICON-GATE)

8192 × 8-BIT READ ONLY MEMORY (BANK SELECT)



P SUFFIX
PLASTIC PACKAGE
CASE 709

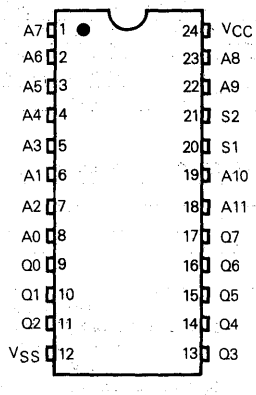
BLOCK DIAGRAM



*Active level defined by user.

NOTE: An i subscript denotes an internal address line only.

PIN ASSIGNMENT



PIN NAMES	
A0-A11	Address
S1, S2	Chip Selects
Q0-Q7	Data Output
VCC	+5 V Power Supply
VSS	Ground

ROM

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	−1.0 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Supply Voltage (V_{CC} Must be Applied at Least 100 μs Before Proper Device Operation is Achieved)	V_{CC}	4.5	5.0	5.5	V	–
Input High Voltage	V_{IH}	2.0	–	V_{CC}+1	V	–
Input Low Voltage	V_{IL}	−0.5	–	0.8		

OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Input Current (V_{in}=0 to 5.5 V)	I_{in}	−10	–	10	μA	1
Output High Voltage (I_{OH}= −205 μA)	V_{OH}	2.4	–	–	V	–
Output Low Voltage (I_{OL}= 3.2 mA)	V_{OL}	–	–	0.4	V	–
Output Leakage Current (Three-State) (S1 or S2=Not Selected, V_{out}=0.4 V to 2.4 V)	I_{LO}	−10	–	10	μA	2
Supply Current (V_{CC}=5.5 V)	I_{CC}	–	–	80	mA	3

CAPACITANCE (f=1.0 MHz, T_A=25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

NOTES:
1. Measured a) forcing V_{CC} on one input pin at a time, while all others are grounded (V_{SS}), and
   b) maintaining 0.0 V (V_{SS}) on one pin at a time, while all others are at V_{CC}=4.5 V and 5.5 V.
2. Measured a) with A0-A11=V_{SS} and forcing 0.4 V on one output at a time while all others are held at 2.4 V, and
   b) with A0-A11=V_{SS} and forcing 2.4 V on one output at a time while all others are held at 0.4 V (V_{CC}=4.5 V and 5.5 V).
3. Measured with the chip selected (S1, S2=true), addresses cycling and the outputs unloaded.

AC OPERATING CONDITIONS AND CHARACTERISTICS

READ CYCLE (See Notes 4, 5)

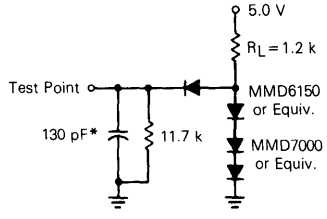
Parameter	Symbol		MCM68368		Unit	Notes
	Standard	Alternate	Min	Max		
Address Valid to Address Don't Care (Cycle Time when Chip Selects are Held Active)	t_{AVAX}	t_{CYC}	450	–	ns	–
Address Valid to Output Valid (Access)	t_{AVQV}	t_{AA}	–	450	ns	–
Chip Select High to Output Valid (Access)	t_{SHQV}	t_{AS}	–	200	ns	–
Address Valid to Output Invalid	t_{AVQX}	t_{DHA}	10	–	ns	–
Chip Select High to Output Invalid	t_{SHQX}	t_{SLZ}	10		ns	–
Chip Select Low to Output High Z	t_{SLQZ}	t_{SHZ}	0	175	ns	–
Address Valid to Chip Select High	t_{AVSH}	t_{AS}	250	–	ns	6

Notes: 4. S1, S2 represented as active high for illustrative purposes.

5. AC Test Conditions
   Input transition times: 5 ns ≤ $t_r = t_f$ ≤ 20 ns.
   Temperature: T_A = 0°C to 70°C
   Load Shown in Figure 1
   V_{CC} = 5.0 V ± 10%
   Input Pulse Levels: V_{IL} = −0.5 V to 0.8 V
   V_{IH} = 2.0 V to V_{CC}
   Measurement Levels: Input = 1.5 V
   Output High = 2.0 V
   Output Low = 0.8 V

6. A faster minimum time is allowed, but the timing must then be referenced to t_{AVQV} and t_{AVQX}.

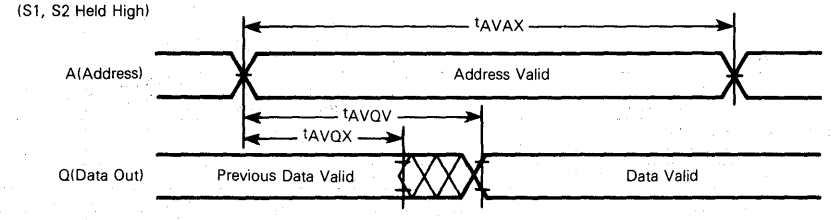
FIGURE 1 — AC TEST LOAD



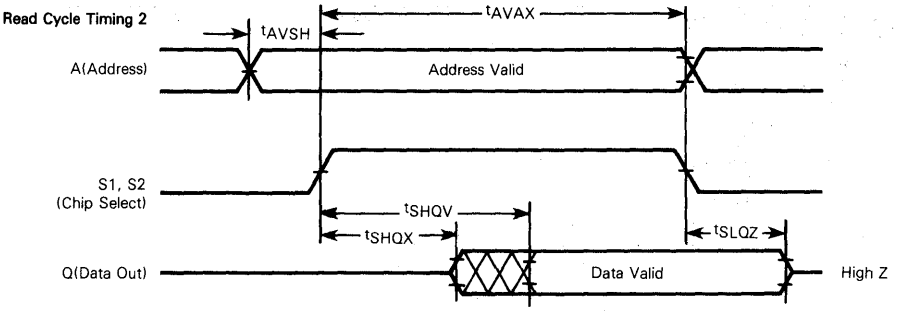
*Includes Jig Capacitance

ROM

Read Cycle Timing 1
(S1, S2 Held High)



Read Cycle Timing 2



FUNCTIONAL DESCRIPTION (Reference Block Diagram)

The MCM68368 is organized into 8K × 8 bit bytes. Twelve address lines are available and 4K bytes can be addressed at a time. A paging system is used which segments the memory into eight 1K banks. The upper 1K banks are always resident and the other 7 banks are accessed through pointers. The pointers contain three bits which define the internal 3 upper address bits ($A12_i$, $A11_i$, $A10_i$). Note that these 3 bits are not directly accessable to the user. There are a total of 3 pointers.

The pointers are loaded as follows: A11 through A5 are set to logic 1s; A4 and A3 select the pointer (see Table 1). A2, A1, A0 are the contents loaded to the pointer which determine which bank is to be selected (see Table 2).

TABLE 1

A4	A3	Pointer
0	0	0
0	1	1
1	0	2
1	1	X (No Pointer Will Be Loaded)

TABLE 2

A2	A1	A0	Bank
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 (Resident)

Example 1: Suppose FF3 (Hexadecimal) is addressed

A11	A10	A9	A8	A7	A5	A4	A3	A2	A1	A0
1	1	1	1	1	1	1	0	0	1	1

This will load the information for selecting bank 3 (A2 = 0, A1 = 1, A0 = 1) into pointer 2 (A4 = 1, A3 = 0). Note that the outputs seen from this address will be from the resident bank, not from bank 3. This means that when A11 through A5 are logic 1s that this is a write only condition for the pointer. Also, when A11 and A10 = 1, the internal address bits $A12_i$, $A11_i$, $A10_i$ are set to logic 1s which denotes the resident bank.

The banks are accessed as follows: A11 and A10 determine which pointer is used to choose the bank (see Table 3), A9-A0 determine the address in the bank.

TABLE 3

A11	A10	Pointer
0	0	0
0	1	1
1	0	2
1	1	None (Resident Bank Only)

Example 2: Suppose that on the following cycle, after that of Example 1, the address 900 (hex) is loaded to the ROM.

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	1	0	0	0	0	0	0	0	0
2		1		0				0			

Pointer 2 will be chosen (A11 = 1, A10 = 0). Thus, bank 3 is accessed because the code for the particular bank was contained in pointer 2. The address 100 is accessed in bank 3.

Chip Select (Reference Block Diagram)

This device utilizes two chip selects to create four different select codes. The selects serve as two gating functions: (1) both selects must be active true to enable the outputs; otherwise, the outputs are in a high impedance state (see AC Operating Conditions and Waveforms); (2) both selects must be active to write to a pointer; thus, the device cannot be deselected while loading contents into the pointers.

MOTOROLA

MCM68369

Advance Information

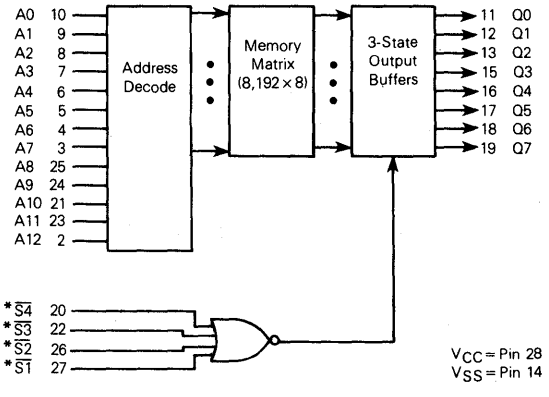
64K BIT READ ONLY MEMORY

The MCM68369 is a MOS mask programmable byte-oriented, Read-Only Memory (ROM). The MCM68369 is organized as 8K × 8 and is fabricated using Motorola's high performance N-channel silicon gate technology. This device is designed to provide maximum circuit density and reliability with the highest possible performance. It remains fully compatible with TTL inputs and outputs while maintaining low power dissipation and wide operating margins. The MCM68369 also contains circuitry for current surge suppression which maintains the chip in an internal deselect mode until V_{CC} approaches 2.5 volts, at which time the chip is internally selected.

The active level of the Chip Selects, along with the memory contents, are defined by the user.

- Single + 5 Volt (± 10%) Supply
- Fully Static Periphery — No Clocking Required on Chip Selects
- Power Dissipation
  80 mA Active (Maximum) (Unloaded)
- Program Layer Late in Process for Quick Turnaround Time
- Maximum Access from Address
  100 ns — MCM68369P20
  120 ns — MCM68369P25
  150 ns — MCM68369P30
- Maximum Access from Chip Select
  80 ns — MCM68369P20
  100 ns — MCM68369P25
  120 ns — MCM68369P30
- The Active Level of All Four Chip Selects are Mask Programmable, with a Don't Care Mask Option on Chip Selects S1 and S2
- 28-Pin JEDEC Standard Package and Pinout

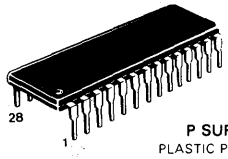
BLOCK DIAGRAM



*Active level defined by the user.

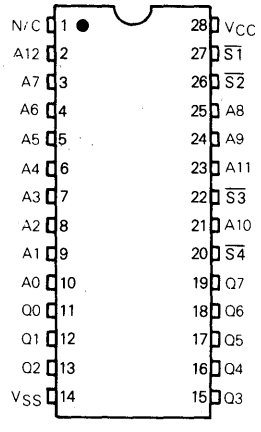
NMOS
(N-CHANNEL, SILICON GATE)

8192 × 8 BIT
READ ONLY MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT



PIN NAMES

A0-A12	Address
$\overline{S1}$, $\overline{S2}$, $\overline{S3}$, $\overline{S4}$	Chip Selects
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

ROM

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	−1.0 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V	–
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V	–
Input Low Voltage	V_{IL}	−0.5	–	0.8		

DC OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	−10	–	10	μA	1
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	–	V	–
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	–	–	0.4	V	–
Output Leakage Current (Output three-stated) ($\overline{S1}$ to $\overline{S4}$ ≥ 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	−10	–	10	μA	2,4
Supply Current – Active (V_{CC} = 5.5 V)	I_{CC}	–	–	80	mA	3,4

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	8	pF
Output Capacitance	C_{out}	15	pF

Notes:
1. Measured a) with the chip powered up forcing V_{CC} on one input pin at a time while all others are grounded, and
   b) maintaining 0.0 V on one pin at a time while all others are at V_{CC}.
2. Measured a) with A0-A12 = V_{SS} and forcing 0.4 V on one output at a time while all others are held at 2.4 V, and
   b) with A0-A12 = V_{SS} and forcing 2.4 V on one output at a time while all others are held at 0.4 V (V_{CC} = 4.5 V and 5.5 V).
3. Measured with the Chip Selected ($\overline{S} = V_{IL}$), addresses cycling (t_{AVAX} = 300 ns), and the outputs unloaded.
4. Chip Select ($\overline{S}$) is represented by active low for illustrative purposes.
   (The active level of the Chip Select is defined by the user.)

AC OPERATING CONDITIONS AND CHARACTERISTICS

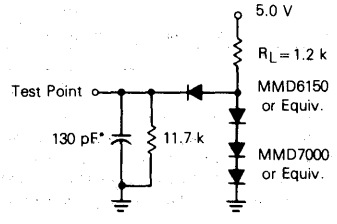
(Full operating voltage and temperature range unless otherwise noted.)

READ CYCLE (See Notes 4, 5)

Parameter	Symbol		MCM68369-20		MCM68369-25		MCM68369-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Address Valid to Address Don't Care	t_{AVAX}	t_{CYC}	200	–	250	–	300	–	ns	–
Address Valid to Output Valid (Access)	t_{AVQV}	t_{AA}	–	200	–	250	–	300	ns	–
Address Valid to Output Invalid	t_{AVQX}	t_{DHA}	20	–	20	–	20	–	ns	–
Chip Select Low to Output Valid	t_{SLQV}	t_{SA}	–	100	–	120	–	150	ns	–
Chip Select Low to Output Invalid	t_{SLQX}	t_{SLZ}	10	–	10	–	10	–	ns	–
Chip Select High to Output High Z	t_{SHQZ}	t_{SHZ}	–	80	–	80	–	80	ns	–

Notes: 5. AC Test Conditions:
Input Transition Times: 5 ns ≤ $t_r = t_f$ ≤ 20 ns.
Temperature: T_A = 0°C to 70°C
Load Shown in Figure 1
V_{CC} = 5.0 V ± 10%
Input Pulse Levels: V_{IL} = −0.5 V to 0.8 V
V_{IH} = 2.0 V to V_{CC}
Measurement Levels: Input = 1.5 V.
Output High = 2.0 V.
Output Low = 0.8 V.

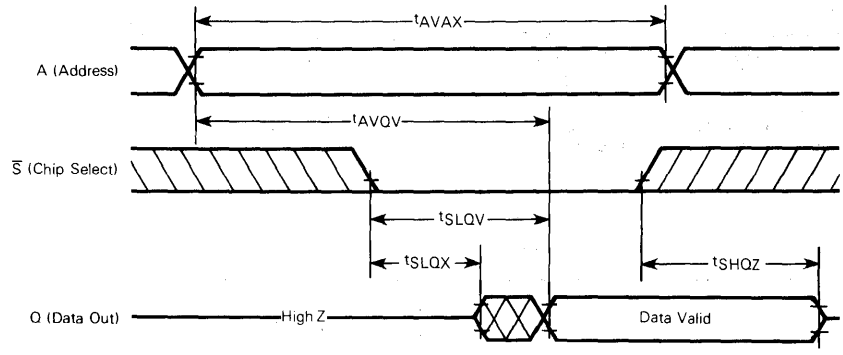
FIGURE 1 — AC TEST LOAD



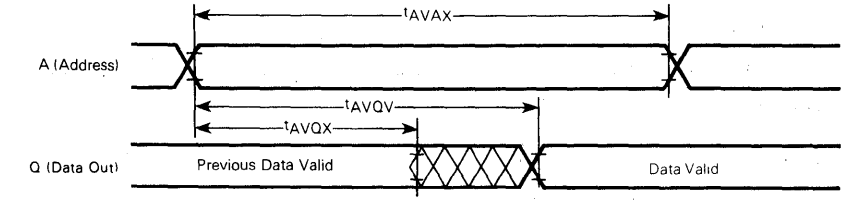
*Includes Jig Capacitance.

ROM

READ CYCLE TIMING 1 (Note 6)



READ CYCLE TIMING 2
$\overline{S} = V_{IL}$



Note 6. Addresses valid prior to or coincident with Chip Select ($\overline{S}$) transition low.

ROM

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68369, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68369 should be submitted on an Organizational Data form such as that shown in Figure 2.

Information for customer memory contents may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs — one 64K or two 32K.
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character Code. Motorola's R.O.M.S. format.

FIGURE 2 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68369 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No: _____

Specif. No: _____

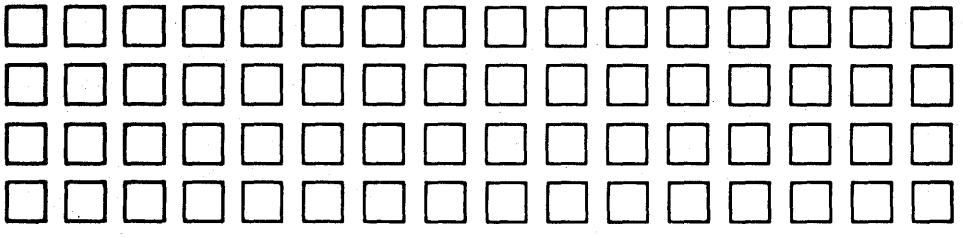
Enable Options:	Active High	Active Low	Don't Care
S4 Pin 20	☐	☐	—
S3 Pin 22	☐	☐	—
S2 Pin 26	☐	☐	☐
S1 Pin 27	☐	☐	☐

Device Marking Requirements

The customer marking requirements are restricted to these limits:

1) Four lines maximum (including date code)

2) Not more than 16 characters per line



ROM

MOTOROLA

MCM68370

Advance Information

64K BIT READ ONLY MEMORY

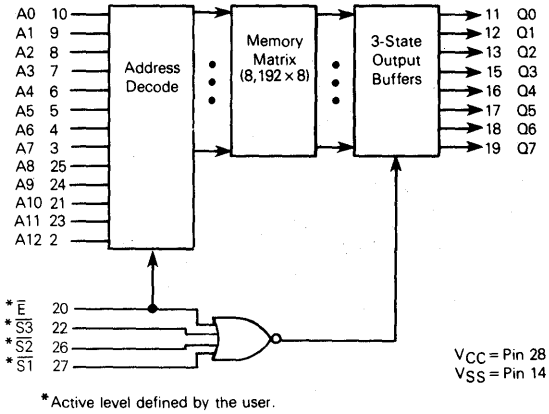
The MCM68370 is a MOS mask programmable byte-oriented, Read Only Memory (ROM). The MCM68370 is organized as 8K × 8 and is fabricated using Motorola's high performance N-channel silicon gate technology. This device is designed to provide maximum circuit density and reliability with the highest possible performance. It remains fully compatible with TTL inputs and outputs while maintaining low power dissipation and wide operating margins. The MCM68370 also contains circuitry for current surge suppression which maintains the chip in an internal deselect mode until V_{CC} approaches 2.5 volts, at which time the chip is internally selected.

The active levels of the Chip Enable and the Chip Selects, along with the memory contents, are defined by the user.

The Chip Enable input controls the automatic power down feature which deselects the outputs and reduces the power consumption.

- Single + 5 Volt (± 10%) Supply
- Fully Static Periphery — No Clocking Required on Chip Enable
- Power Dissipation
  80 mA Active (Maximum) (Unloaded)
  15 mA Standby (Maximum)
- Program Layer Late in Process for Quick Turnaround Time
- Maximum Access from Address and Chip Enable
  200 ns — MCM68370P20
  250 ns — MCM68370P25
  300 ns — MCM68370P30
- Maximum Access from Chip Select
  100 ns — MCM68370P20
  120 ns — MCM68370P25
  150 ns — MCM68370P30
- The Active Level of Chip Enable and Chip Selects is Mask Programmable, with a Don't Care Mask Option on Chip Selects $\overline{S1}$ and $\overline{S2}$
- 28-Pin JEDEC Standard Package and Pinout

BLOCK DIAGRAM

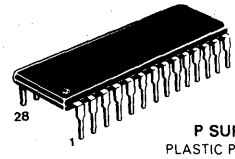


*Active level defined by the user.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

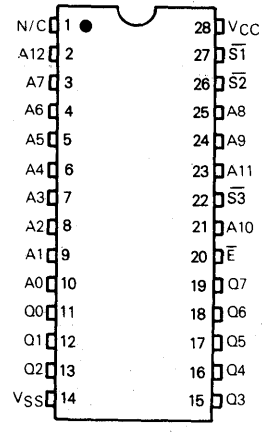
NMOS
(N-CHANNEL, SILICON GATE)

8,192 × 8 BIT
READ ONLY MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT



PIN NAMES	
A0-A12	Address
$\overline{E}$	Chip Enable
$\overline{S1}$, $\overline{S2}$, $\overline{S3}$	Chip Selects
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

ROM

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage Relative to VSS	V_{CC}	−1.0 to +7.0	V
Voltage on Any Pin Relative to VSS	V_{in}, V_{out}	−1.0 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V	–
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V	–
Input Low Voltage	V_{IL}	−0.5	–	0.8		

DC OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	−10	–	10	μA	1
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	–	V	–
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	–	–	0.4	V	–
Output Leakage Current (Output High Z; V_{out} = 0.4 V to 2.4 V) $\overline{E} \geq 2.0$ V, $\overline{S}$ = Don't Care $\overline{S} \geq 2.0$ V, $\overline{E}$ = Don't Care	I_{LO}	−10	–	10	μA	2, 5
Supply Current – Active (V_{CC} = 5.5 V)	I_{CC}	–	35	80	mA	3, 5
Supply Current – Standby (V_{CC} = 5.5 V)	I_{SB}	–	6	15	mA	4, 5

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	8	pF
Output Capacitance	C_{out}	15	pF

Notes:
1. Measured a) with the chip powered up forcing V_{CC} on one input pin at a time while all others are grounded, and
   b) maintaining 0.0 V on one pin at a time while all others are at V_{CC}.
2. Measured a) with A0-A12 = V_{SS} and forcing 0.4 V on one output at a time while all others are held at 2.4 V, and
   b) with A0-A12 = V_{SS} and forcing 2.4 V on one output at a time while all others are held at 0.4 V
   (V_{CC} = 4.5 V and 5.5 V).
3. Measured with the Chip Enabled ($\overline{E}$ = V_{IL}), addresses cycling (t_{AVAX} = 300 ns), and the outputs unloaded.
4. Measured with the Chip Disabled ($\overline{E}$ = V_{IH}) and the outputs unloaded.
5. Chip Enable ($\overline{E}$) and Chip Select ($\overline{S}$) are represented by active low for illustrative purposes.
   (The active level of the Chip Enable and the Chip Select are defined by the user.)

AC OPERATING CONDITIONS AND CHARACTERISTICS

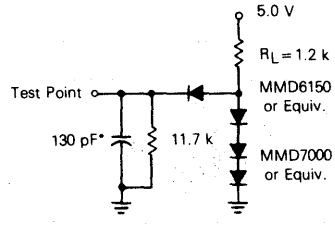
(Full operating voltage and temperature range unless otherwise noted.)

READ CYCLE (See Notes 5, 6)

Parameter	Symbol		MCM68370-20		MCM68370-25		MCM68370-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Address Valid to Address Don't Care (Cycle Time when Chip Enable is Held Active)	t_{AVAX}	t_{CYC}	200	–	250	–	300	–	ns	–
Chip Enable Low to Chip Enable High	t_{ELEH}	t_{EW}	200	–	250	–	300	–	ns	–
Address Valid to Output Valid (Access)	t_{AVQV}	t_{AA}	–	200	–	250	–	300	ns	–
Chip Enable Low to Output Valid (Access)	t_{ELQV}	t_{EA}	–	200	–	250	–	300	ns	–
Address Valid to Output Invalid	t_{AVQX}	t_{DHA}	20	–	20	–	20	–	ns	–
Chip Enable Low Output Invalid	t_{ELQX}	t_{ELZ}	20	–	20	–	20	–	ns	–
Chip Enable High to Output High Z	t_{EHQZ}	t_{EHZ}	–	80	–	80	–	80	ns	–
Chip Select Low to Output Valid	t_{SLQV}	t_{SA}	–	100	–	120	–	150	ns	–
Chip Select Low to Output Invalid	t_{SLQX}	t_{SLZ}	10	–	10	–	10	–	ns	–
Chip Select High to Output High Z	t_{SHQZ}	t_{SHZ}	–	80	–	80	–	80	ns	–

Note: 6. AC Test Conditions
Input Transition Times: 5 ns≤t_r = t_f≤20 ns
Temperature: T_A = 0°C to 70°C
Load Shown in Figure 1
V_{CC} = 5.0 V ± 10%
Input Pulse Levels: V_{IL} = −0.5 V to 0.8 V
V_{IH} = 2.0 V to V_{CC}
Measurement Levels: Input = 1.5 V
Output High = 2.0 V
Output Low = 0.8 V

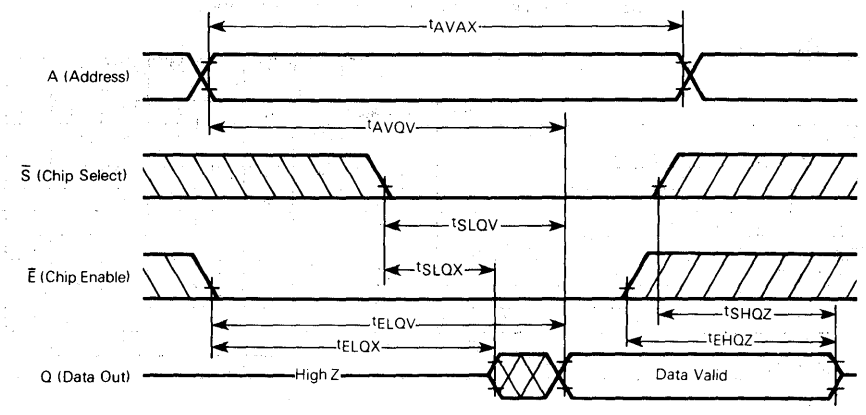
FIGURE 1 — AC TEST LOAD



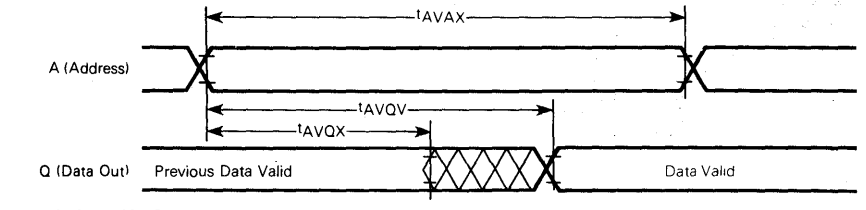
*Includes Jig Capacitance

ROM

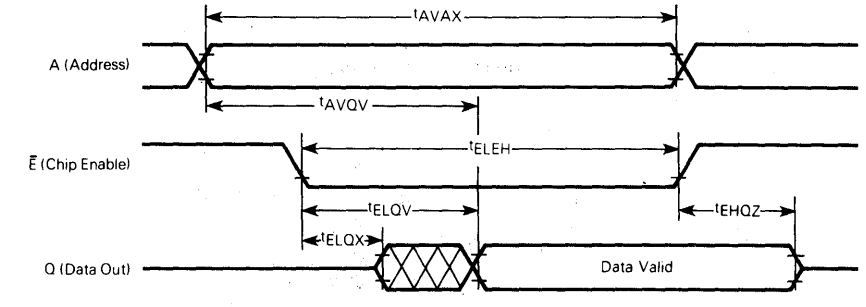
READ CYCLE TIMING 1



READ CYCLE TIMING 2
$\overline{E} = V_{IL}$, $\overline{S} = V_{IL}$



READ CYCLE TIMING 3
$\overline{S} = V_{IL}$ (Note 7)



Note: 7. Addresses valid prior to or coincident with Chip Enable ($\overline{E}$) transition low.

ROM

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68370, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68370 should be submitted on an Organizational Data form such as that shown in Figure 2.

Information for custom memory contents may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs — one 64K or two 32K.
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character Code. Motorola's R.O.M.S. format.

FIGURE 2 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68370 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No: _____

Specif. No: _____

Enable Options:	Active High	Active Low	Don't Care
E (Chip Enable, Pin 20)	☐	☐	—
S3 (Chip Select, Pin 22)	☐	☐	—
S2 (Chip Select, Pin 26)	☐	☐	☐
S1 (Chip Select, Pin 27)	☐	☐	☐

Device Marking Requirements

The customer marking requirements are restricted to these limits:
1) Four lines maximum (including date code)
2) Not more than 16 characters per line.

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ROM

MOTOROLA

MCM68380

Product Preview

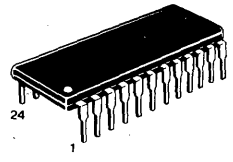
80K BIT READ ONLY MEMORY

The MCM68380 is an 81,920 bit mask-programmable read only memory with 4 banks organized as 2048 by 10 bit words, designed to operate as program memory for systems using a General Instrument CP1600 series microprocessor. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, and is TTL compatible. It has 16 bi-directional pins, DB0 through DB15, for a 16 bit address into the device and a 16 bit data out of the device. Three mode control pins, BC1, BC2, and BDIR, enable proper chip select logic.

- Address and Data Use a Common 16-Bit Three-State Bus
- 5-Bit Programmable Memory Map Using Upper Order Address (DB11-DB15) to Place 8K ROM Page Within 65K Word Memory Space
- External Address Status and Internal Data Output State is Latched with the Help of Control Strobes (BC1, BC2, and BDIR)
- Designed to Operate with Reduced External Logic in a Practical Microprocessor Application
- 300 ns Typical Data Access Time
- TTL Compatible I/O
- Single 5 Volt ± 10% Power Supply
- Totally Automated Custom Programming

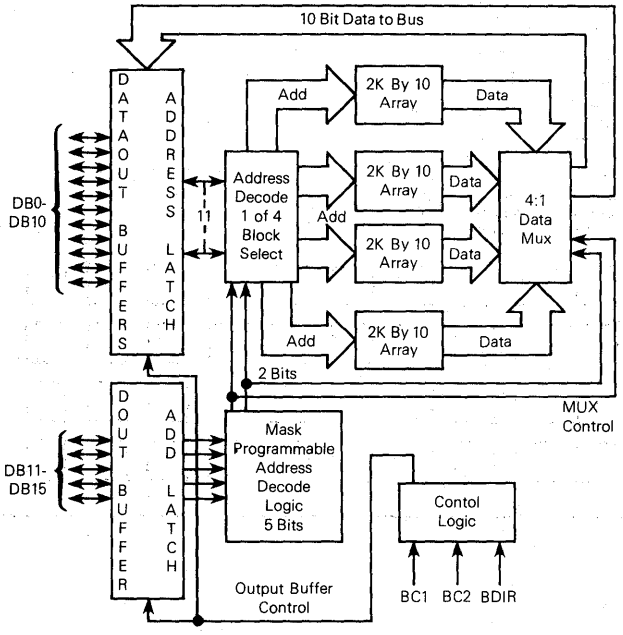
MOS
(N-CHANNEL, SILICON-GATE)

8192 × 10-BIT
READ ONLY MEMORY

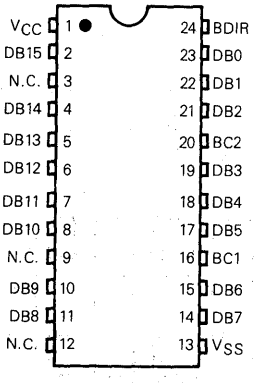


P SUFFIX
PLASTIC PACKAGE
CASE 709

BLOCK DIAGRAM
80K — ROM



PIN ASSIGNMENT



Pin Names	
DB0-DB15	Common Address/Data Out
BC1, BC2, BDIR	Bus Mode Control and Chip Read/Select Logic Enable
V_{CC}	+5 V Power Supply
V_{SS}	Ground

ROM

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (with Respect to V_{SS})	V_{CC}	−0.3 to +7.0	V
Input Voltage (with Respect to V_{SS})	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V

DC OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Output High Voltage (Source Current = −100 μA)	V_{OH}	2.4	–	V
Output Low Voltage (Sink Current= +1.6 mA)	V_{OL}	–	0.4	V
Supply Current (Operating) (V_{CC} = Max)	I_{CC}	–	100	mA
Input Leakage (V_{in} = 0 V to V_{CC})	I_{in}	−10	+10	μA
Output Leakage	I_{LO}	−10	+10	μA

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	5	pF
Output Capacitance	C_{out}	12.5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels ..... 0 Volt and 2.3 Volts
Input Rise and Fall Times ..... 20 ns
Input Timing Levels ..... 1.5 Volts
Output Timing Levels ..... 0.8 Volt and 2.0 Volts
Output Load ..... See Figure 1

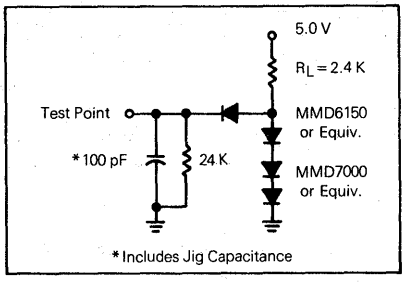
OPERATING CHARACTERISTICS

Parameter	Symbol	MCM68380 Min	MCM68380 Max	Unit	Notes
Address Setup	t_{AS}	300	–	ns	
Address Overlap (Address Hold)	t_{AH}	65	–	ns	
Data Turn On Delay	t_{DO}	–	350	ns	1
Data Hold	t_{DH}	80	–	ns	1
Control Code Stable	t_{CCS}	885	–	ns	
NACT Code Stable	t_{NACT}	885	–	ns	
Data Float Delay	t_{FL}	–	300	ns	1
Control Signals Skew	t_{CSS}	–	40	ns	

NOTES: 1. One TTL load and 100 pF.

ROM

FIGURE 1 — AC TEST LOAD



OPERATING DESCRIPTION

From initialization, the ROM waits for the first address code; i.e., BAR. For this address code and all subsequent address sequences, the ROM reads the 16 bit external bus and latches the value into its address register.

The ROM contains a programmable memory location for its own 8K page, and if a valid address is detected, the particular address located will transfer its contents to the chip output buffers. If the control code following the address cycle was a read, the ROM will output the 10 bits of addressed data and drive logic zero on the top six bits of the bus.

RESPONSES

A. **No Action.** Waiting state. Signals may be propagating internally, but I/O pins are in a high-impedance state and are not being read.

B. **Ignored by ROM.** Basically same response as A.

C. **Output and Input.** Output buffers drive I/O pins (if there is a valid add map from address previously loaded), and whatever appears on the I/O pins is loaded into the address register. If there is not a valid add map from address previously loaded, I/O pins are in a high-impedance state and whatever appears on the I/O pins is loaded into the address register.

D. **Data to Bus.** Output buffers drive I/O pins according to data in output register (if there is a valid add map). I/O pins are not read. Address previously loaded into address register remains unchanged. If there is not a valid add map from address previously loaded, I/O pins are in a high-impedance state and are not read.

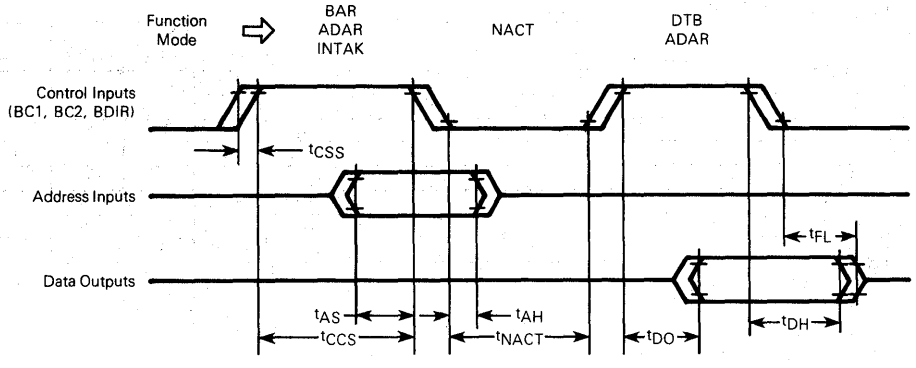
E. **Bus to Address Register.** Output buffers are in high-impedance state. Address present on I/O pins is loaded into address register.

TRUTH TABLE

INPUT CONTROL SIGNALS

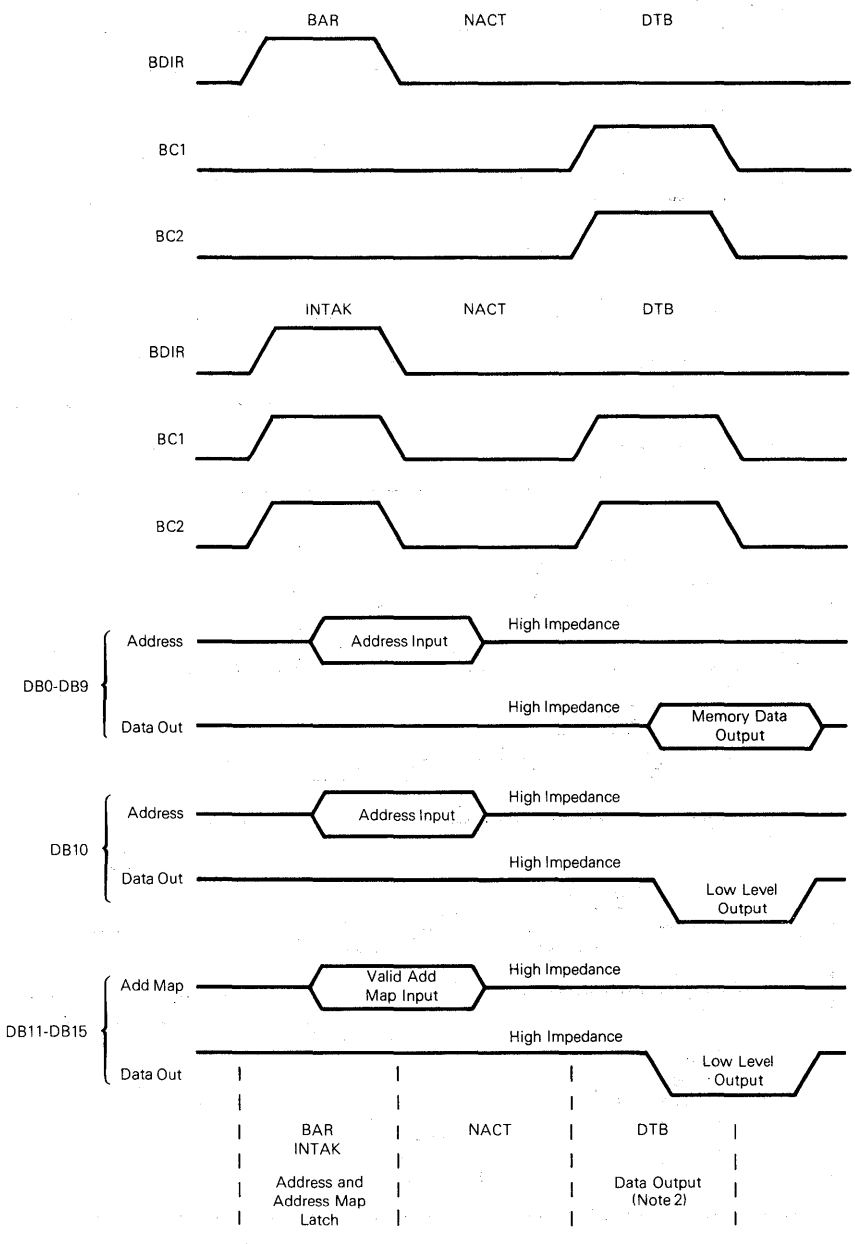
Responses	BDIR	BC1	BC2	Equivalent Signal	Decoded Function
A	0	0	0	NACT	No Action, D0-D15 = High Impedance
B	0	0	1	IAB	No Action
C	0	1	0	ADAR	Address Data to Address Register, D0-D15 = High Impedance
D	0	1	1	DTB (Read)	Data To Bus, D0-D15 = Input
E	1	0	0	BAR	Bus to Address Register
B	1	0	1	DWS	No Action
B	1	1	0	DW	No Action
E	1	1	1	INTAK	Interrupt Acknowledge

TIMING WAVEFORMS

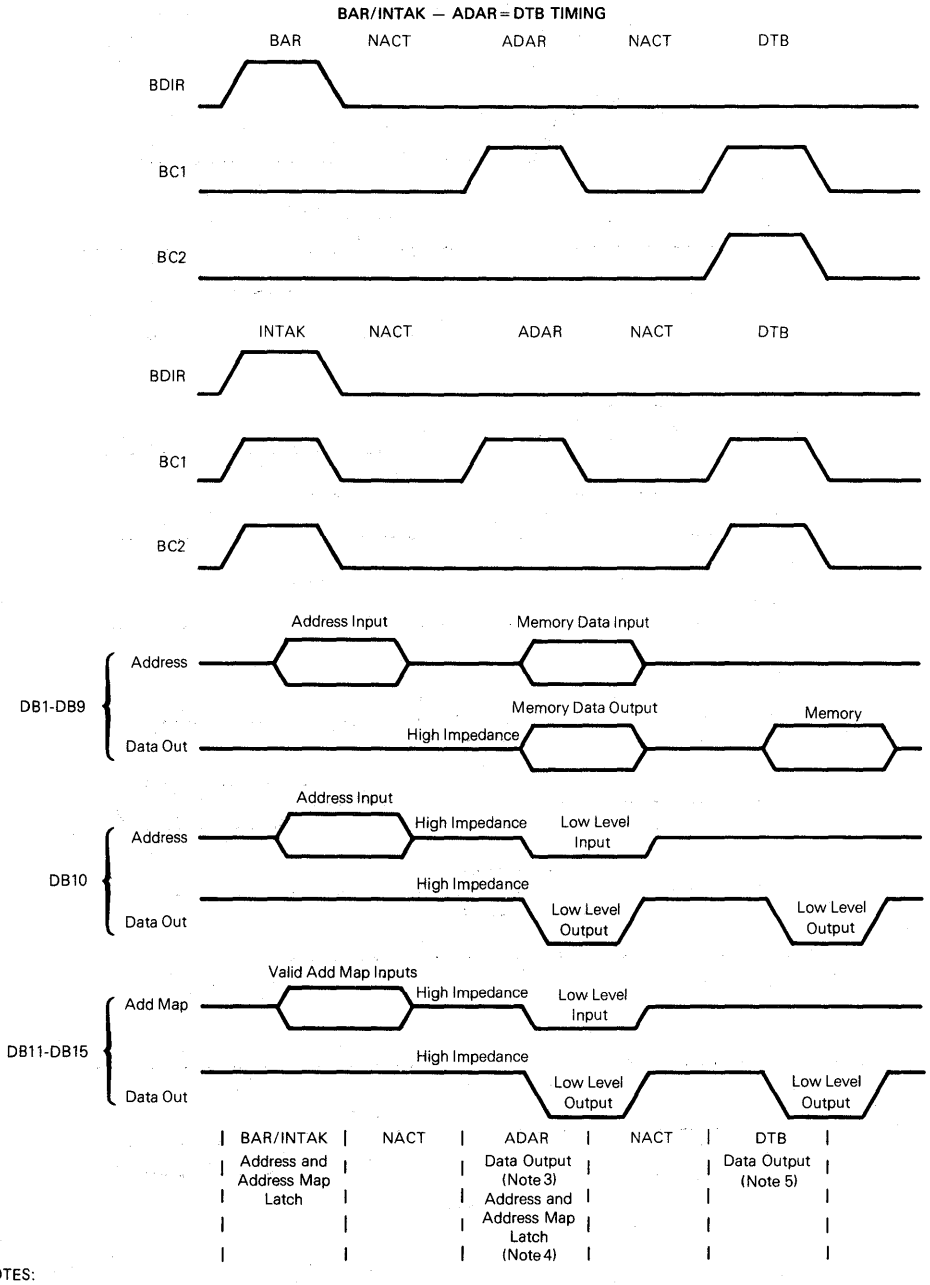


ROM

BAR/INTAK — DTB TIMING



ROM



NOTES:

2. If there are no valid address map inputs during BAR or INTAK instruction, I/O pins are in high-impedance state and are not read during DTB instruction.
3. If there are no valid address map inputs during BAR or INTAK instruction, I/O pins are in high-impedance and whatever appears on the I/O pins is loaded into the address register during ADAR instruction.
4. If there are valid address map inputs during BAR or INTAK instruction, memory data are outputted and whatever appears on the I/O pins is loaded into the address register.
5. If there are valid address map inputs during ADAR instruction, memory data are outputted, but if there are no valid address map inputs during ADAR instruction, I/O pins are in high-impedance and are not read during DTB instructions.

ROM

MOTOROLA

MCM63128

Advance Information

128K BIT READ ONLY MEMORY

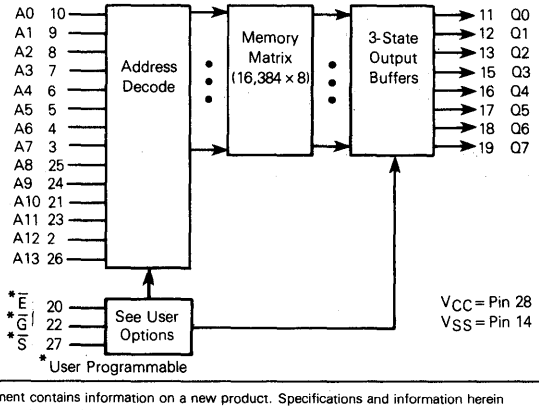
The MCM63128 is a MOS mask programmable, byte-oriented, Read-Only Memory (ROM). The MCM63128 is organized as 16K × 8 and is fabricated using Motorola's high performance N-channel silicon gate technology (HMOS). This device is designed to provide maximum circuit density and reliability with the highest possible performance. It remains fully compatible with TTL inputs and outputs while maintaining low power dissipation and wide operating margins. The MCM63128 also contains circuitry for current surge suppression which maintains the chip in an internal deselect mode until V_{CC} approaches 2.5 volts, at which time the chip is internally selected.

There are numerous logical NOR or NAND combinations between Chip Enable ($\overline{E}$), Chip Select ($\overline{S}$), and Output Enable ($\overline{G}$) that three state the device. This feature is selected by the user and placed into effect with the mask programming. The active level of the Chip Enable ($\overline{E}$), Chip Select ($\overline{S}$), and the Output Enable ($\overline{G}$), along with the memory contents, are defined by the user.

The Chip Enable input controls the automatic power down feature which deselects the outputs and reduces the power consumption.

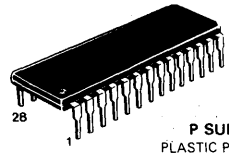
- Single + 5 Volt (±10%) Supply
- Fully Static Periphery — No Clocking Required on Chip Enable
- Power Dissipation
  100 mA Active (Maximum) (Unloaded)
  15 mA Standby (Maximum)
- Program Layer Late in Process for Quick Turnaround Time
- Maximum Access from Address and Chip Enable
  150 ns — MCM63128P15
  200 ns — MCM63128P20
- Maximum Access from Output Enable
  60 ns — MCM63128P15
  80 ns — MCM63128P20
- Active Level for Chip Enable, Chip Select, and Output Enable are User Selectable.
- 28-Pin JEDEC Standard Package and Pinout

BLOCK DIAGRAM



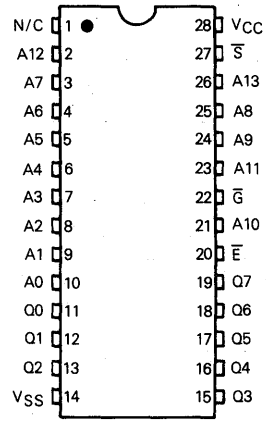
This document contains information on a new product. Specifications and information herein are subject to change without notice.

HMOS
(N-CHANNEL, SILICON GATE)
16,384 × 8 BIT
READ ONLY MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT



PIN NAMES	
A0-A13	Address
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{S}$	Chip Select
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

ROM

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage Relative to VSS	V_{CC}	−1.0 to +7.0	V
Voltage on Any Pin Relative to VSS	V_{in}, V_{out}	−1.0 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V	–
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V	–
Input Low Voltage	V_{IL}	−0.5	–	0.8		

DC OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	−10	–	10	μA	1
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	–	V	–
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	–	–	0.4	V	–
Output Leakage Current (Output High Z; V_{out} = 0.4 V to 2.4 V) $\overline{E} \geq 2.0$ V, $\overline{S} = \overline{G}$ = Don't Care $\overline{S} = \overline{G} \geq 2.0$ V, $\overline{E}$ = Don't Care	I_{LO}	−10	–	10	μA	2, 5
Supply Current – Active (V_{CC} = 5.5 V)	I_{CC}	–	–	100	mA	3, 5
Supply Current – Standby (V_{CC} = 5.5 V)	I_{SB}	–	–	15	mA	4, 5

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	8	pF
Output Capacitance	C_{out}	15	pF

ROM

Notes:
1. Measured a) with the chip powered up forcing V_{CC} on one input pin at a time while all others are grounded, and
   b) maintaining 0.0 V on one pin at a time while all others are at V_{CC}.
2. Measured a) with A0-A13 = V_{SS} and forcing 0.4 V on one output at a time while all others held at 2.4 V, and
   b) with A0-A13 = V_{SS} and forcing 2.4 V on one output at a time while all others are held at 0.4 V (V_{CC} = 4.5 V and 5.5 V).
3. Measured with the Chip Enabled ($\overline{E} = V_{IL}$), addresses cycling (t_{AVAX} = 150 ns), and the outputs unloaded.
4. Measured with the Chip Disabled ($\overline{E} = V_{IH}$) and the outputs unloaded.
5. Chip enable ($\overline{E}$), Chip Select ($\overline{S}$), and Output Enable ($\overline{G}$) are represented by active low for illustrative purposes. (The active level of the Chip Enable, Chip Select and Output Enable are defined by the user.)

AC OPERATING CONDITIONS AND CHARACTERISTICS

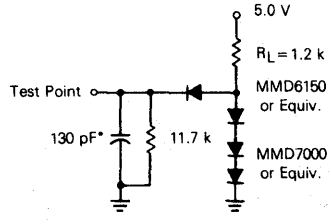
(Full operating voltage and temperature range unless otherwise noted.)

READ CYCLE (See Notes 5, 6)

Parameter	Symbol		MCM63128-15		MCM63128-20		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Address Valid to Address Don't Care (Cycle Time when Chip Enable is Held Active)	t_{AVAX}	t_{CYC}	150	–	200	–	ns	–
Chip Enable Low to Chip Enable High	t_{ELEH}	t_{EW}	150	–	200	–	ns	–
Address Valid to Output Valid (Access)	t_{AVQV}	t_{AA}	–	150	–	200	ns	–
Chip Enable Low to Output Valid (Access)	t_{ELQV}	t_{EA}	–	150	–	200	ns	–
Address Valid to Output Invalid	t_{AVQX}	t_{DHA}	20	–	20	–	ns	–
Chip Enable Low to Output Invalid	t_{ELQX}	t_{ELZ}	20	–	20	–	ns	–
Chip Enable High to Output High Z	t_{EHQZ}	t_{EHZ}	–	60	–	80	ns	–
Output Enable Low to Output Valid	t_{GLQV}	t_{GA}	–	60	–	80	ns	–
Output Enable Low to Output Invalid	t_{GLQX}	t_{GLZ}	10	–	10	–	ns	–
Output Enable High to Output High Z	t_{GHQZ}	t_{GHZ}	–	60	–	80	ns	–
Chip Select Low to Output Valid	t_{SLQV}	t_{SA}	–	60	–	80	ns	–
Chip Select Low to Output Invalid	t_{SLQX}	t_{SLZ}	10	–	10	–	ns	–
Chip Select High to Output High Z	t_{SHQZ}	t_{SHZ}	–	60	–	80	ns	–

Note: 6. AC Test Conditions
Input transition times: 5 ns ≤ $t_r = t_f$ ≤ 20 ns.
Temperature: T_A = 0°C to 70°C
Load Shown in Figure 1
V_{CC} = 5.0 V ± 10%
Input Pulse Levels: V_{IL} = −0.5 V to 0.8 V
V_{IH} = 2.0 V to V_{CC}
Measurement Levels: Input = 1.5 V
Output High = 2.0 V
Output Low = 0.8 V

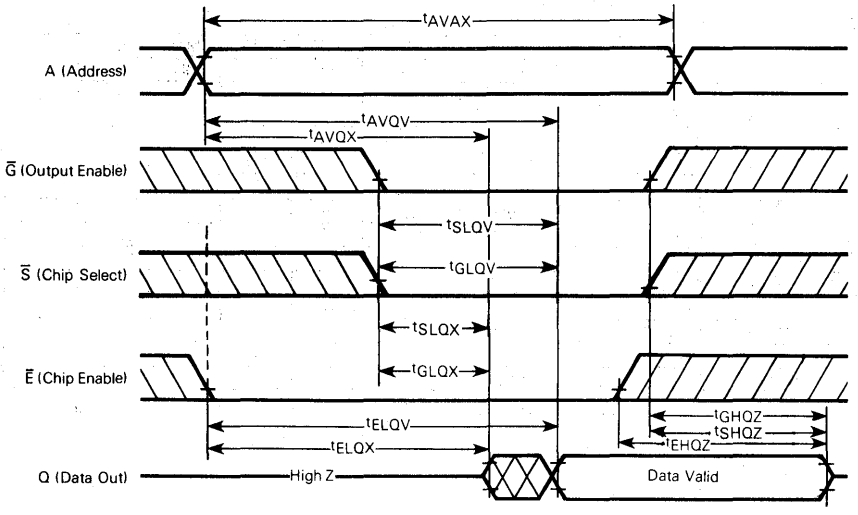
FIGURE 1 — AC TEST LOAD



*Includes Jig Capacitance

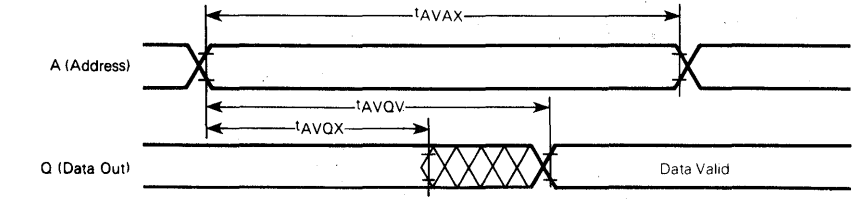
ROM

READ CYCLE TIMING 1 (Note 7)



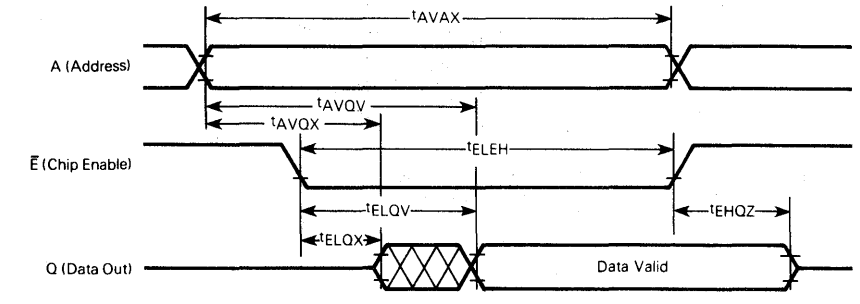
READ CYCLE TIMING 2

$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{S} = V_{IL}$ (Note 7)



READ CYCLE TIMING 3

$\overline{G} = V_{IL}$, $\overline{S} = V_{IL}$ (Notes 7, 8)



Notes: 7. When Chip Enable ($\overline{E}$) is Low, the address input must be valid.
8. Addresses valid prior to or coincident with Chip Enable ($\overline{E}$) transition low.

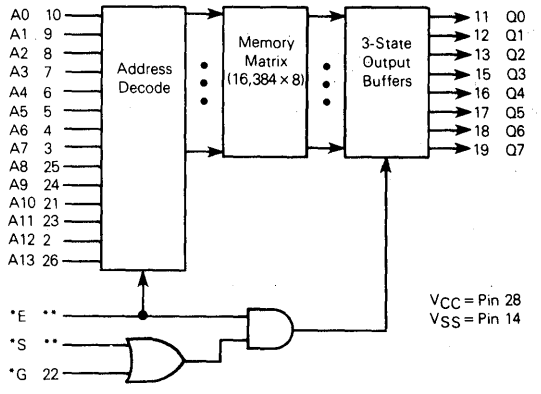
ROM

USER OPTIONS

OPTION 1

User Selections

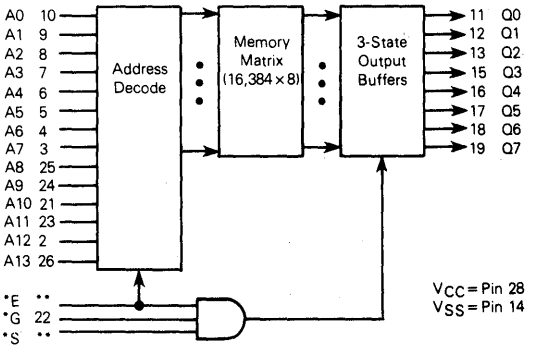
Function	Pin	Active Level (High)	Active Level (Low)
G[9]	22	1	0
E[10, 11]	20, 27	1	0
S[11]	20, 27	1	0



OPTION 2

User Selections

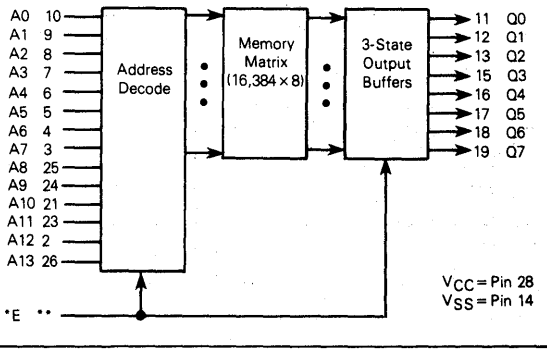
Function	Pin	Active Level (High)	Active Level (Low)
G[9]	22	1	0
E[10, 11]	20, 27	1	0
S[11]	20, 27	1	0



OPTION 3

User Selections

Function	Pin	Active Level (High)	Active Level (Low)
E[12]	20, 27	1	0



* Active level defined by the user

** Pin defined by user

Notes:

9. No Option on Pin.
10. Chip Enable (E) controls Power up and Power Down.
11. Chip Enable (E) and Chip Select (S) may not have the same Pin Assignment.
12. Either Pin 20 and Pin 22 will be Don't Care or Pin 22 and Pin 27 will be Don't Care but the one remaining pin controls Power Up and Power Down (E).

ROM

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM63128, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM63128 should be submitted on an Organizational Data form such as that shown in Figure 2.

Information for custom memory contents may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs — one 128K, two 64K, or four 32K.
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character Code. Motorola's R.O.M.S. format.

FIGURE 2 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM63128 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No: _____

Specif. No: _____

Enable Options: (Please Refer to User Options)

	Active High	Active Low	Pin 20	Pin 22	Pin 27
Chip Enable	☐	☐	☐		☐
Chip Select	☐	☐	☐		☐
Output Enable	☐	☐		☐	
Don't Care			☐	☐	☐

User Option 1 ☐

User Option 2 ☐

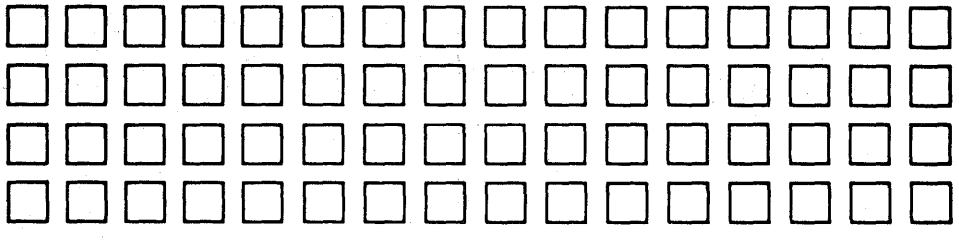
User Option 3 ☐

Device Marking Requirements

The customer marking requirements are restricted to these limits:

1) Four lines maximum (including date code)

2) Not more than 16 characters per line



ROM

MOTOROLA

MCM63256

Advance Information

256K BIT READ ONLY MEMORY

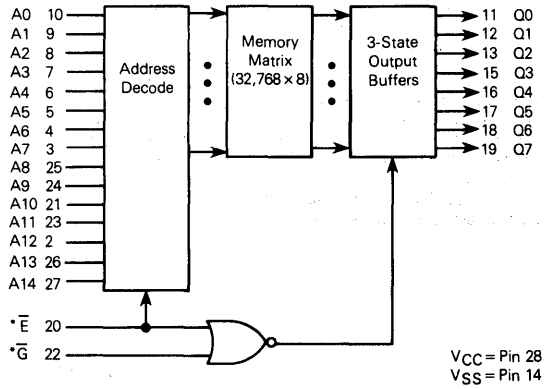
The MCM63256 is a MOS mask programmable byte-oriented, Read-Only Memory (ROM). The MCM63256 is organized as 32K × 8 and is fabricated using Motorola's High performance N-channel silicon gate technology (HMOS). This device is designed to provide maximum circuit density and reliability with the highest possible performance. It remains fully compatible with TTL inputs and outputs while maintaining low power dissipation and wide operating margins. The MCM63256 also contains circuitry for current surge suppression which maintains the chip in an internal deselect mode until V_{CC} approaches 2.5 volts, at which time the chip is internally selected.

The active level of the Chip Enable and the Output Enable, along with the memory contents, are defined by the user. The user can also define the pinout assignment for address (A14) to either pin 27 or pin 1.

The Chip Enable input controls the automatic power down feature which deselects the outputs and reduces the power consumption.

- Single + 5 Volt (±10%) Supply
- Fully Static Periphery — No Clocking Required on Chip Enable
- Power Dissipation
  100 mA Active (Maximum) (Unloaded)
  15 mA Standby (Maximum)
- Program Layer Late in Process for Quick Turnaround Time
- Maximum Access from Address and Chip Enable
  150 ns — MCM63256P15
  200 ns — MCM63256P20
- Maximum Access from Output Enable
  60 ns — MCM63256P15
  80 ns — MCM63256P20
- Address (A14) is User Selectable for Either Pin 27 or Pin 1
- Active Level for Chip Enable and Output Enable is User Selectable
- 28-Pin JEDEC Standard Package and Pinout

BLOCK DIAGRAM

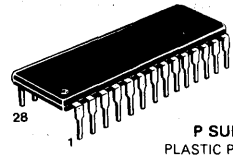


*Active level defined by the user.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

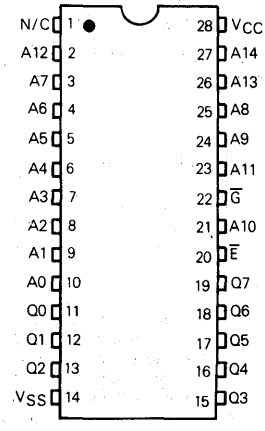
HMOS
(N-CHANNEL, SILICON GATE)

32,768 × 8 BIT
READ ONLY MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT



PIN NAMES

A0-A14	Address
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

ROM

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	−1.0 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V	–
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V	–
Input Low Voltage	V_{IL}	−0.5	–	0.8		

DC OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	−10	–	10	μA	1
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	–	V	–
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	–	–	0.4	V	–
Output Leakage Current (Output High Z; V_{out} = 0.4 V to 2.4 V) 1. $\overline{E} \geq 2.0$ V, $\overline{G}$ = Don't Care 2. $\overline{G} \geq 2.0$ V, $\overline{E}$ = Don't Care	I_{LO}	−10	–	10	μA	2, 5
Supply Current – Active (V_{CC} = 5.5 V)	I_{CC}	–	–	100	mA	3, 5
Supply Current – Standby (V_{CC} = 5.5 V)	I_{SB}	–	–	15	mA	4, 5

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	8	pF
Output Capacitance	C_{out}	15	pF

NOTES: 1. Measured a) with the chip powered up forcing V_{CC} on one input pin at a time while all others are grounded, and
b) maintaining 0.0 V on one pin at a time while all others are at V_{CC}.
2. Measured a) with A0-A14 = V_{SS} and forcing 0.4 V on one output at a time while all others are held at 2.4 V, and
b) with A0-A14 = V_{SS} and forcing 2.4 V on one output at a time while all others are held at 0.4 V (V_{CC} = 4.5 V and 5.5 V).
3. Measured with the Chip Enabled ($\overline{E} = V_{IL}$), addresses cycling (t_{AVAX} = 150 ns), and the outputs unloaded.
4. Measured with the Chip Disabled ($\overline{E} = V_{IH}$) and the outputs unloaded.
5. Chip Enable ($\overline{E}$) and Output Enable ($\overline{G}$) are represented by active low for illustrative purposes.
(The active level of the Chip enable and the Output Enable are defined by the user.)

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

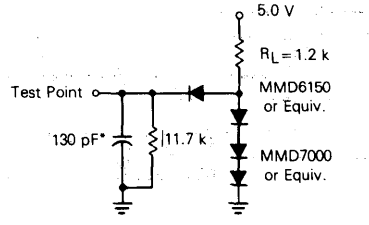
READ CYCLE (See Notes 5, 6)

Parameter	Symbol		MCM63256-15		MCM63256-20		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Address Valid to Address Don't Care (Cycle Time when Chip Enable is Held Active)	t_{AVAX}	t_{CYC}	150	–	200	–	ns	–
Chip Enable Low to Chip Enable High	t_{ELEH}	t_{EW}	150	–	200	–	ns	–
Address Valid to Output Valid (Access)	t_{AVQV}	t_{AA}	–	150	–	200	ns	–
Chip Enable Low to Output Valid (Access)	t_{ELQV}	t_{EA}	–	150	–	200	ns	–
Address Valid to Output Invalid	t_{AVQX}	t_{DHA}	20	–	20	–	ns	–
Chip Enable Low to Output Invalid	t_{ELQX}	t_{ELZ}	20	–	20	–	ns	–
Chip Enable High to Output High Z	t_{EHQZ}	t_{EHZ}	–	60	–	80	ns	–
Output Enable Low to Output Valid	t_{GLQV}	t_{GA}	–	60	–	80	ns	–
Output Enable Low to Output Invalid	t_{GLQX}	t_{GLZ}	10	–	10	–	ns	–
Output Enable High to Output High Z	t_{GHQZ}	t_{GHZ}	–	60	–	80	ns	–

Note: 6. AC Test Conditions

Input transition times: 5 ns ≤ $t_r = t_f$ ≤ 20 ns.
Temperature: T_A = 0°C to 70°C
Load Shown in Figure 1
V_{CC} = 5.0 V ± 10%
Input Pulse Levels: V_{IL} = – 0.5 V to 0.8 V
V_{IH} = 2.2 V to V_{CC}
Measurement Levels: Input = 1.5 V
Output Low = 0.8 V
Output High = 2.0 V

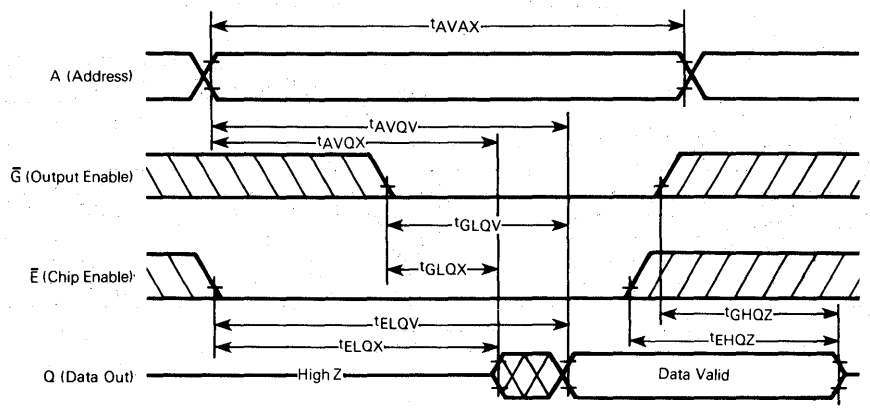
FIGURE 1 — AC TEST LOAD



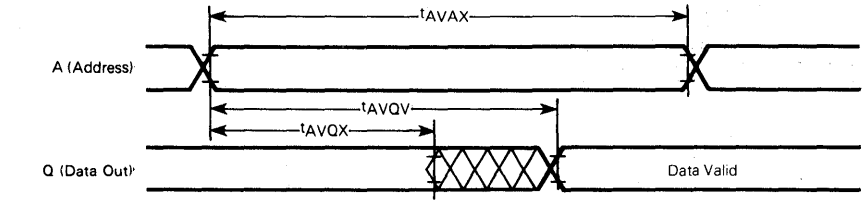
*Includes Jig Capacitance

ROM

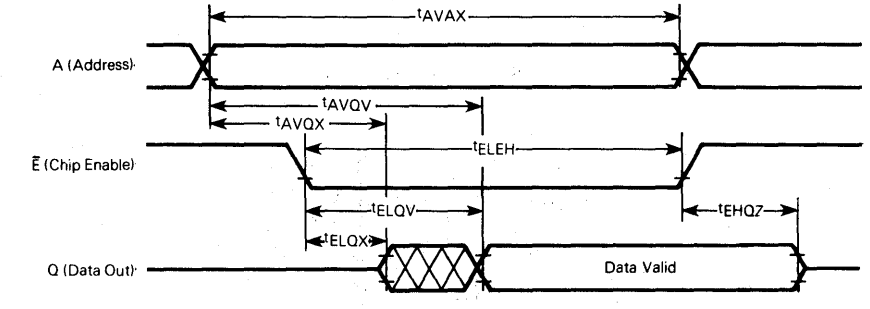
READ CYCLE TIMING 1 (Note 7)



READ CYCLE TIMING 2
$\overline{E}=V_{IL}$, $\overline{G}=V_{IL}$ (Note 7)



READ CYCLE TIMING 3
$\overline{G}=V_{IL}$ (Notes 7, 8)



Notes:
7. When Chip Enable ($\overline{E}$) is Low, the address input must be valid.
8. Addresses valid prior to or coincident with Chip Enable ($\overline{E}$) transition low.

ROM

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM63256, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM63256 should be submitted on an Organizational Data form such as that shown in Figure 2.

Information for custom memory contents may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs – one 256K, two 128K, or four 64K.
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character Code. Motorola's R.O.M.S. format.

FIGURE 2 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM63256 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No: _____

Specif. No: _____

Enable Options:

	Active High	Active Low
Chip Enable (Pin 20)	☐	☐
Output Enable (Pin 22)	☐	☐

Pinout Options:

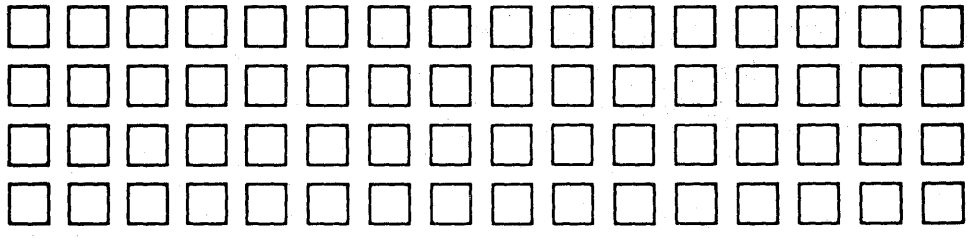
	Pin 27	Pin 1
Address A14	☐	☐

Device Marking Requirements

The customer marking requirements are restricted to these limits:

1) Four lines maximum (including date code)

2) Not more than 16 characters per line



ROM

MOTOROLA

MCM65256

Product Preview

256K BIT READ ONLY MEMORY

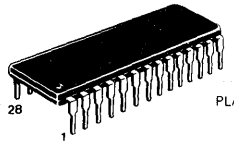
The MCM65256 is a complementary MOS mask-programmable byte-organized Read Only Memory (ROM). The MCM65256 is organized as 32,768 bytes of 8 bits and is fabricated using Motorola's High performance silicon gate CMOS technology (HCMOS). This device is designed to provide maximum circuit density and reliability with highest possible performance while maintaining low-power dissipation and wide operating margins. The MCM65256 offers low-power operation from a single +5 volt supply and is fully TTL compatible on all inputs and outputs.

The active level of the Chip Enable and the Output Enable, along with the memory contents, are defined by the user. The Chip Enable input deselects the outputs and puts the chip in a power-down mode. The user can also define the pinout assignment for Address (A14) to either pin 27 or pin 1.

- Single +5 Volt ± 10% Power Supply
- Fully Static Periphery — No Clocking Required on Chip Enable
- Maximum Access Time from Address and Chip Enable is 350 ns
- Automatic Power Down
- Low Power Dissipation
  - 50 mA Maximum (Active, Unloaded, 1 μs Cycle Rate) — Decreases with Increasing Cycle Time
  - 5 mA Maximum (Standby, TTL Inputs)
  - 50 μA Maximum (Standby, Full Rail Inputs)
- Program Layer Late in Process for Fast Turnaround Time
- Address (A14) is User Selectable for Either Pin 27 or Pin 1
- Active Level for Chip Enable and Output Enable Are User Selectable
- 28 Pin JEDEC Standard Package and Pinout

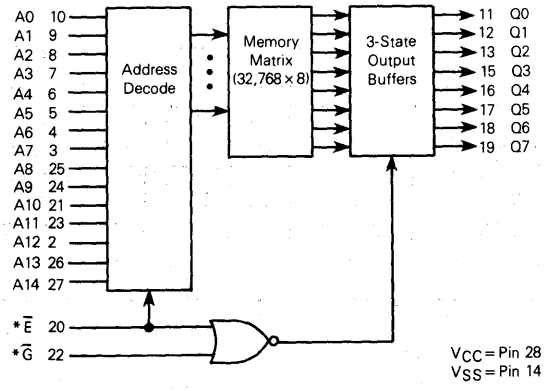
HCMOS
(COMPLEMENTARY MOS)

32,768 × 8 BIT
READ ONLY MEMORY



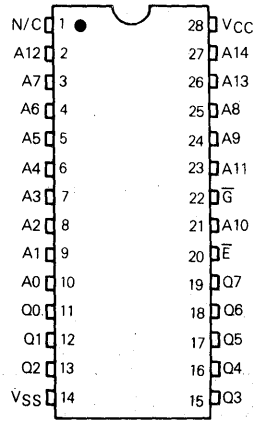
P SUFFIX
PLASTIC PACKAGE
CASE 710

BLOCK DIAGRAM



*Active level defined by the user.

PIN ASSIGNMENT



PIN NAMES

A0-A14	Address
Ē	Chip Enable
Ḡ	Output Enable
Q0-Q7	Data Output
VCC	+5 V Power Supply
VSS	Ground

ROM

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage Relative to V_{SS}	V_{CC}	−0.3 to +7.0	V
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Power Dissipation	P_D	1.0	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V	–
Input High Voltage	V_{IH}	2.2	–	V_{CC}	V	–
Input Low Voltage	V_{IL}	−0.3	–	0.8		

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	−10	–	10	μA	1
Output High Voltage (I_{OH} = −400 μA)	V_{OH}	2.4	–	–	V	–
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.4	V	–
Output Leakage Current (Output High Z; V_{out} = 0.4 V to 2.4 V) $\overline{E} \geq 2.2$ V, $\overline{G}$ = Don't Care $\overline{G} \geq 2.2$ V, $\overline{E}$ = Don't Care	I_{LO}	−10	–	10	μA	2, 5
Supply Current – Active (V_{CC} = 5.5 V) (1 μs Cycle Rate)	I_{CC}	–	–	50	mA	3, 5
Supply Current – Standby ($\overline{E} = V_{CC}$)	I_{SB1}	–	–	50	μA	4
Supply Current – Standby ($\overline{E} = V_{IH}$, Outputs Unloaded)	I_{SB2}	–	–	5	mA	5

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	10	pF
Output Capacitance	C_{out}	15	pF

Notes: 1. Measured a) with the chip powered up forcing V_{CC} on one input pin at a time while all others are grounded, and
b) maintaining 0.0 V on one pin at a time while all others are at V_{CC}.
2. Measured a) with A0-A14 = V_{SS} and forcing 0.4 V on one output at a time while all others are held at 2.4 V, and
b) with A0-A14 = V_{SS} and forcing 2.4 V on one output at a time while all others are held at 0.4 V (V_{CC} = 4.5 V and 5.5 V).
3. Measured with the Chip Enabled ($\overline{E} = V_{IL}$), addresses cycling (t_{AVAX} = 1 μs), and the outputs unloaded.
4. Measured with the Chip Disabled ($\overline{E} = V_{CC}$) and the outputs unloaded.
5. Chip Enable ($\overline{E}$) and Output Enable ($\overline{G}$) are represented by active low for illustrative purposes.
(The active level of the Chip Enable and the Output Enable are defined by the user.)

AC OPERATING CONDITIONS AND CHARACTERISTICS

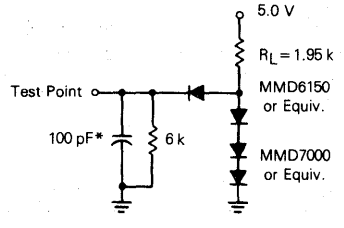
(Full operating voltage and temperature range unless otherwise noted.)

READ CYCLE (See Notes 5, 6)

Parameter	Symbol		MCM65256-35		Unit	Notes
	Standard	Alternate	Min	Max		
Address Valid to Address Don't Care (Cycle Time when Chip Enable is Held Active)	t_{AVAX}	t_{CYC}	350	–	ns	–
Chip Enable Low to Chip Enable High	t_{ELEH}	t_{EW}	350	–	ns	–
Address Valid to Output Valid (Access)	t_{AVQV}	t_{AA}	–	350	ns	–
Chip Enable Low to Output Valid (Access)	t_{ELQV}	t_{EA}	–	350	ns	–
Address Valid to Output Invalid	t_{AVQX}	t_{DHA}	20	–	ns	–
Chip Enable Low to Output Invalid	t_{ELQX}	t_{ELZ}	20	–	ns	–
Chip Enable High to Output High Z	t_{EHQZ}	t_{EHZ}	–	80	ns	–
Output Enable Low to Output Valid	t_{GLQV}	t_{GA}	–	100	ns	–
Output Enable Low to Output Invalid	t_{GLQX}	t_{GLZ}	10	–	ns	–
Output Enable High to Output High Z	t_{GHQZ}	t_{GHZ}	–	80	ns	–

Note: 6. AC Test Conditions
Input transition times: 5 ns ≤ $t_r = t_f$ ≤ 20 ns
Temperature: T_A = 0°C to 70°C
Load shown in Figure 1
V_{CC} = 5.0 V ± 10%
Input Pulse Levels: V_{IL} = −0.5 V to 0.8 V
V_{IH} = 2.2 V to V_{CC}
Measurement Levels: Input = 1.5 V
Output Low = 0.8 V
Output High = 2.0 V

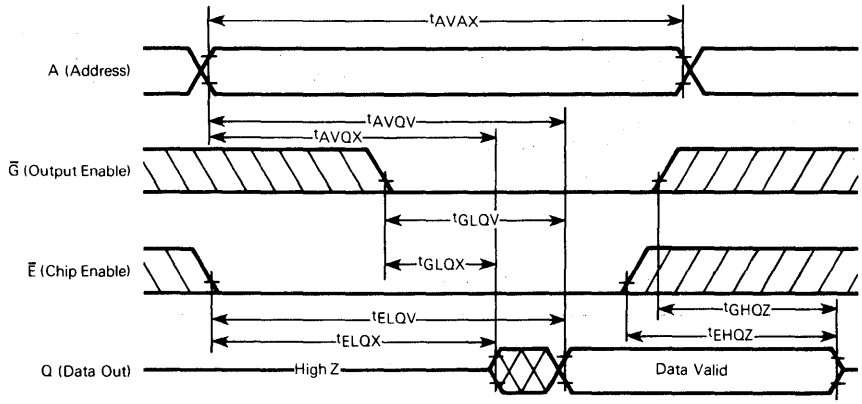
FIGURE 1 — AC TEST LOAD



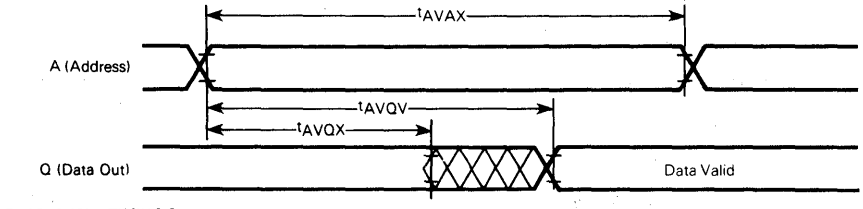
*Includes Jig Capacitance

ROM

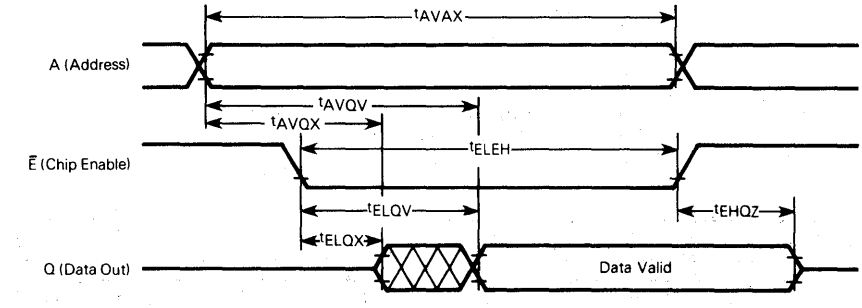
READ CYCLE TIMING 1 (Note 7)



READ CYCLE TIMING 2
$\overline{E}=V_{IL}$, $\overline{G}=V_{IL}$ (Note 7)



READ CYCLE TIMING 3
$\overline{G}=V_{IL}$ (Notes 7, 8)



Notes: 7. When Chip Enable ($\overline{E}$) is Low, the address input must be valid.
8. Addresses valid prior to or coincident with Chip Enable ($\overline{E}$) transition low.

ROM

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM65256, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM65256 should be submitted on an Organizational Data form such as that shown in Figure 2.

Information for custom memory contents may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs — one 256K, two 128K, or four 64K.
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character Code. Motorola's R.O.M.S. format.

FIGURE 2 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM65256 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No: _____

Specif. No: _____

Enable Options:

	Active High	Active Low
Chip Enable (Pin 20)	☐	☐
Output Enable (Pin 22)	☐	☐

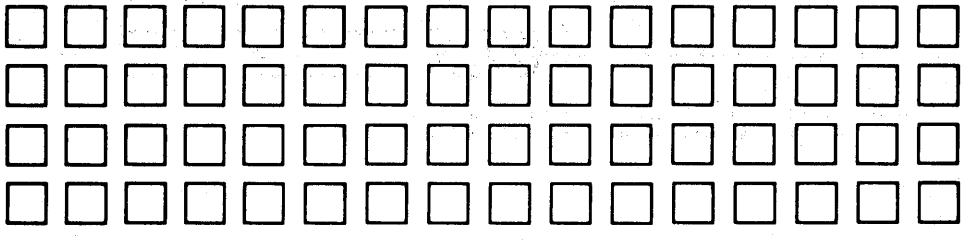
Pinout Options:

	Pin 27	Pin 1
Address A14	☐	☐

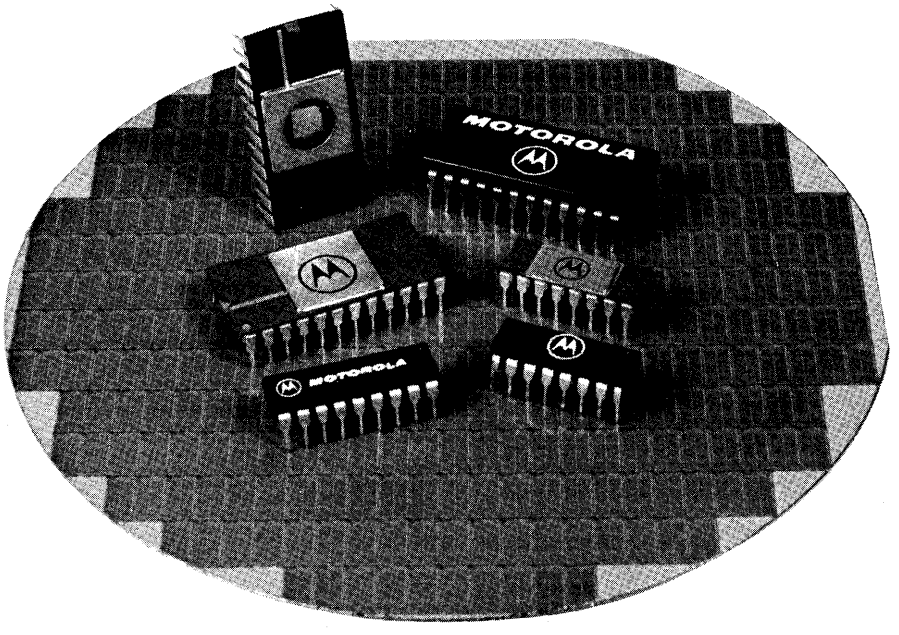
Device Marking Requirements

The customer marking requirements are restricted to these limits:

1) Four lines maximum (including date code)
2) Not more than 16 characters per line



ROM



Other MOS Memories

MOTOROLA

MCM68HC34

Advance Information

HCMOS
(HIGH DENSITY CMOS SILICON-GATE)

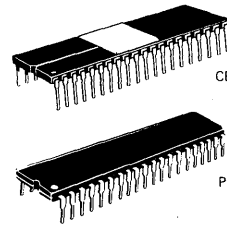
DUAL-PORT RAM MEMORY UNIT

DUAL-PORT RAM MEMORY UNIT

The MCM68HC34 is a dual-port RAM memory (DPM) unit which enables two processors, arbitrarily referred to as "A" and "B", operating on two separate buses to exchange data without interfering with devices on the other bus. It contains 256 bytes of dual-port RAM which is the medium actually used for the interchange of data.

The dual-port memory unit contains six semaphore registers that provide a means for controlling access to the dual-port RAM or any other shared resources. It also contains interrupt registers which provide a means for the processors to interrupt each other.

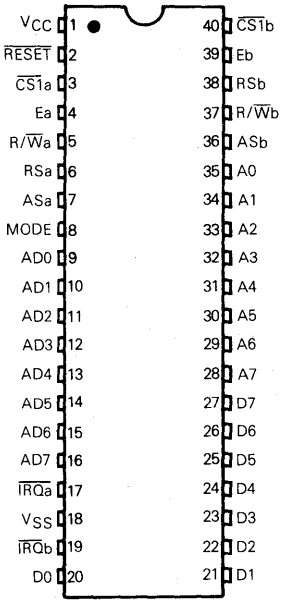
- High-Speed CMOS (HCMOS) Structure
- Six Read/Write Semaphore Registers
- 256 Bytes of Dual-Port RAM
- Eight Address Lines



L SUFFIX
CERAMIC PACKAGE
CASE 715

P SUFFIX
PLASTIC PACKAGE
CASE 711

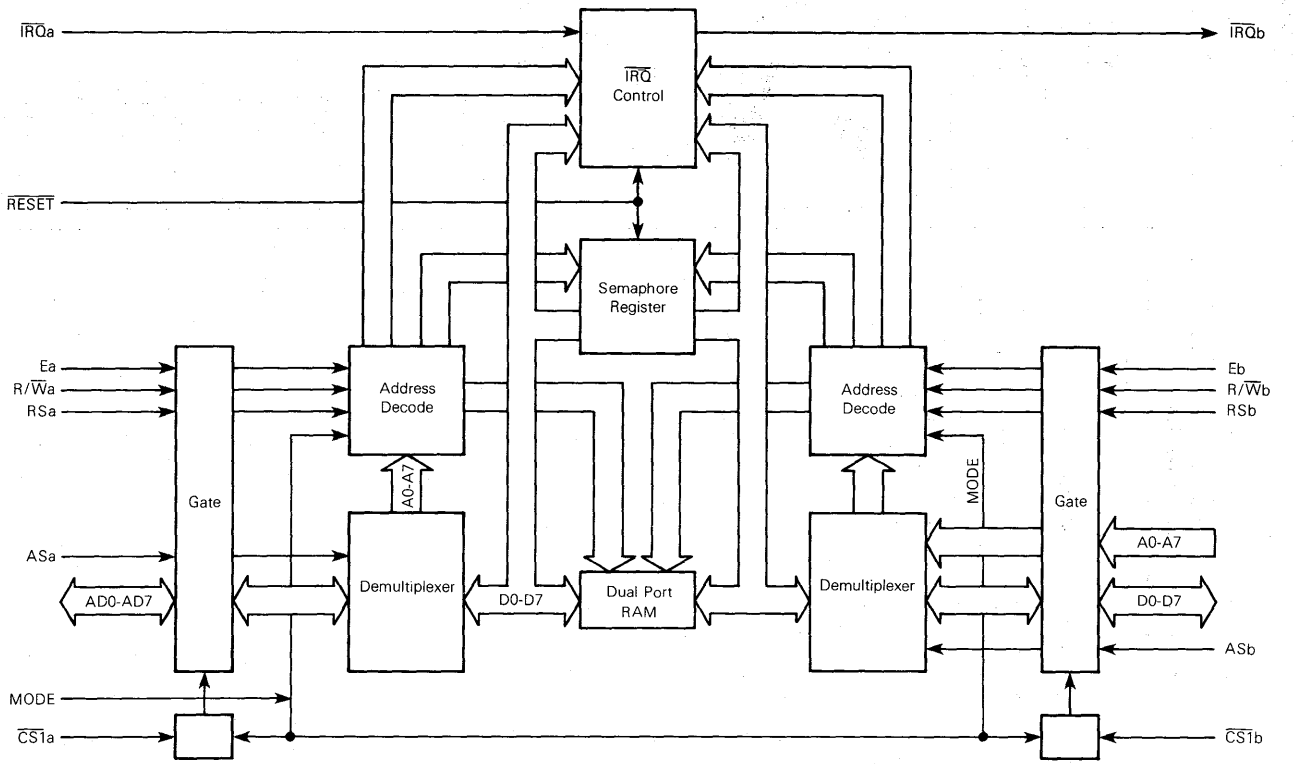
PIN ASSIGNMENT



Other

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FIGURE 1 — BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

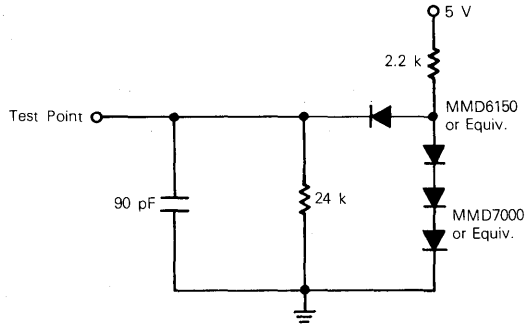
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 7.0	V
Input Voltage, All Inputs	V_{in}	V_{SS} −0.3 to V_{CC} +0.5	V
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance			
Ceramic	θ_{JA}	50	°C/W
Plastic		100	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Unused inputs must be tied to an appropriate logic level (either V_{CC} or V_{SS}) to reduce leakage currents and increase reliablity.

FIGURE 2 — BUS TIMING LOAD



DC ELECTRICAL CHARACTERISTCS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Input High Voltage (see Note 1)	V_{IH}	2.0	V_{CC} +0.3	V
Input Low Voltage (see Note 2)	V_{IL}	V_{SS} −0.3	0.8	V
Input Current (V_{in} = 0 to V_{CC})	I_{in}	—	1.0	μA
Output Leakage Current	I_{OZ}	—	10.0	μA
Output High Voltage (I_{Load} = −100 μA) (I_{Load} = < 10.0 μA)	V_{OH}	2.4 V_{CC} −0.1	— —	V
Output Low Voltage (I_{Load} = 1.6 mA) (I_{Load} = < 10.0 μA)	V_{OL}	— —	0.4 0.1	V
Current Drain — Outputs Unloaded Standby — CEa and CEb at V_{SS} Operating — Ea, Eb = 1 MHz, Both Sides Active	I_{DDS} I_{DD}	— —	0.1 30	mA mA
Input Capacitance	C_{in}	—	10	pF
Output Capacitance (AD0-AD7 and D0-D7)	C_{out}	—	12	pF

NOTES:
1. Input high voltage as stated is for all inputs except MODE. In the case of MODE, input high voltage is tied to V_{CC}.
2. Input low voltage as stated is for all inputs except MODE. In the case of MODE, input low voltage is tied to V_{SS} or is floating. If floating, the voltage will be internally pulled to V_{SS}.

Other

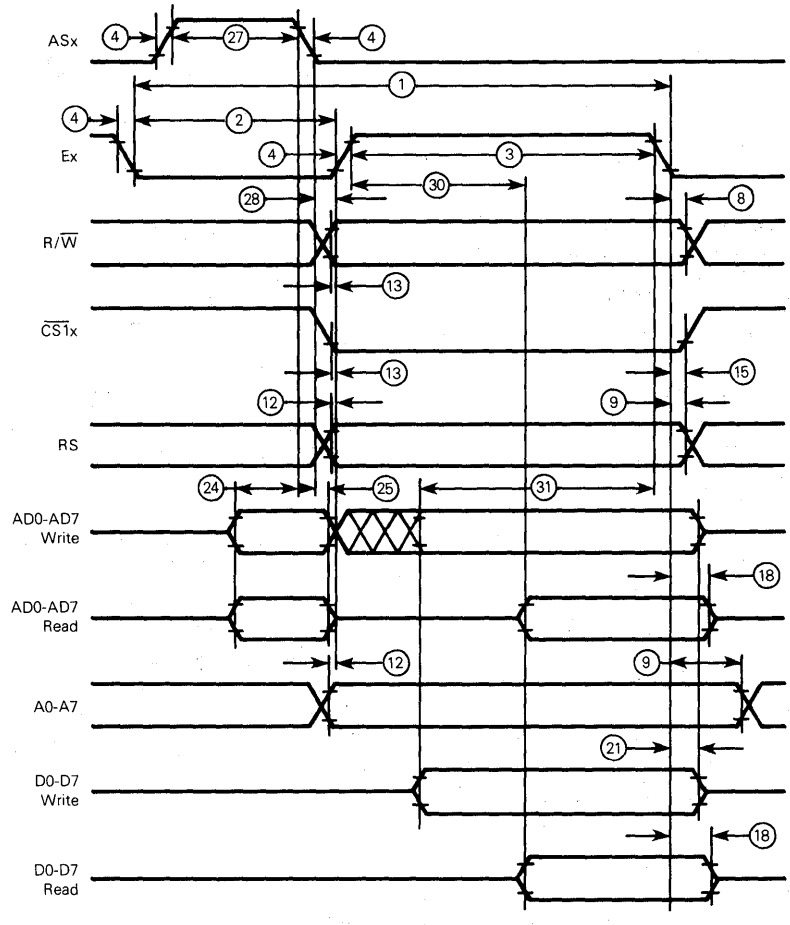
BUS TIMING (See Notes 1 and 2 and Figure 2)

Ident Number	Characteristics	Symbol	Min	Max	Unit
1	Cycle Time	t_{cyc}	800	–	ns
2	Pulse Width, E Low	P_{WEL}	300	–	ns
3	Pulse Width, E High	P_{WEH}	325	–	ns
4	Input Rise and Fall Time	t_r, t_f	–	30	ns
8	Read/Write Hold Time	t_{RWH}	10	–	ns
9	Non-Multiplexed Address, RS Hold Time	t_{AH}	10	–	ns
12	Non-Multiplexed Address, RS Valid Time to Eb	t_{AV}	20	–	ns
13	R/$\overline{W}$, Chip Select Setup Time	t_{RWS}	20	–	ns
15	Chip Select Hold Time	t_{CH}	0	–	ns
18	Read Data Hold Time	t_{DHR}	20	75	ns
21	Write Data Hold Time	t_{DHW}	10	–	ns
24	Address Setup Time for Latch	t_{ASL}	20	–	ns
25	Address Hold Time for Latch	t_{AHL}	20	–	ns
27	Pulse Width, AS High	PW_{ASH}	110	–	ns
28	Address Strobe to E Delay	t_{ASED}	20	–	ns
30	Read Data Delay Time	t_{DDR}	–	240	ns
31	Write Data Setup Time	t_{DSW}	100	–	ns

NOTES:

1. Timing numbers relative to one side only. No numbers are intended to be cross-referenced from one side to the other.
2. Measurement points shown for ac timing are 0.8 V and 2.0 V, unless otherwise specified.

BUS TIMING DIAGRAMS



Other

SIGNAL DESCRIPTION

The following paragraphs cont
the input and output signals.

V_{CC} AND V_{SS}

These pins supply power to the DPM. V_{CC} is +5 volts ±5% and V_{SS} is 0 volts or ground.

E CLOCK INPUTS (Ea AND Eb)

These are the input clocks from the respective processors and are positive during the latter portion of the bus cycle.

REGISTER SELECT INPUTS (RSa AND RSb)

These inputs function as register select inputs. A high on the RSa for side A or RSb for side B input allows selection of the semaphore and interrupt registers respectively for side A and side B by the lower three address bits. A low on RSa or RSb selects 256 bytes of RAM from side A or side B respectively.

CHIP SELECT INPUTS ($\overline{CS1}$a AND $\overline{CS1}$b)

These inputs function as chip select inputs for their respective sides. $\overline{CS1}$a must be low to select side A and $\overline{CS1}$b must be low to select side B. If $\overline{CS1}$a is high, side A is deselected. If $\overline{CS1}$b is high, side B is deselected.

MODE SELECT (MODE)

In normal operation, this pin should always be connected to V_{CC} (MODE = 1). Each side has three states controlled by RSa and $\overline{CS1}$a for side A and RSb and $\overline{CS1}$b for side B.

If $\overline{CS1}$a is high, side A cannot be accessed. If $\overline{CS1}$a is low, side A accesses either 256 bytes of RAM or the six semaphore registers and the two interrupt registers depending on the level of RSa. If RSa is low, 256 bytes of RAM are accessed and if RSa is high, the six semaphores and two interrupt registers are accessed.

The six semaphore and two interrupt registers are redundantly mapped in the 256 byte mode. That is, only the low order three bits select one of eight registers and the upper five bits of address are not decoded. Refer to Table 1.

TABLE 1 — SIDE A CONTROL SIGNAL OPERATION

Mode	$\overline{CS1}$a	RSa	Operation
1	0	0	Access 256 Byte RAM Side A
1	0	1	Access Semaphore/$\overline{IRQ}$ Side A on Lower Three Bits of Address
1	1	X	Side A Not Selected

The three states for side B in the 256 byte mode are controlled in the manner as side A using RSb and $\overline{CS1}$b except that side B uses separated address and data inputs. Refer to Table 2.

TABLE 2 — SIDE B CONTROL SIGNAL OPERATION

		RSb	Operation
		0	Access 256 Byte RAM Side B
		1	Access Semaphore/$\overline{IRQ}$ Side B on Lower Three Bits of Address
1	1	X	Side B Not Selected

INTERRUPT REQUEST OUTPUTS ($\overline{IRQ}$a AND $\overline{IRQ}$b)

These pins are active low open-drain outputs. A write to address F9 from one side asserts an interrupt, if not masked. On the other side, a write to address F9 sets this pin low.

B SIDE ADDRESS BUS INPUTS (A0-A7) AND B SIDE BIDIRECTIONAL DATA BUS (D0-D7)

When the B side is run from a multiplexed bus processor, the B side address pins are connected to the B side data pins, respectively (A0 to D0, A1 to D1, etc.).

SYSTEM RESET INPUT ($\overline{RESET}$)

A low level on this input causes the semaphore registers to be set to the states shown in Table 5 under **SEMAPHORE REGISTERS** and clears both bits of both $\overline{IRQ}$ registers to zeros. The RAM data is unaffected by $\overline{RESET}$.

ADDRESS STROBE INPUTS (ASa AND ASb)

The ASa input demultiplexes the eight low order address lines from the data lines on the A side. The falling edge of ASa latches the A side address within the DPM. The ASb input is used in the same manner when the B side is connected to a multiplexed bus. It must be connected to a high level when the B side is connected to a non-multiplexed bus.

A SIDE MULTIPLEXED ADDRESS/ BIDIRECTIONAL DATA BUS (AD0-AD7)

The A side can only be used with a multiplexed address/data bus. The A side addresses are on these lines during the time ASa is high. The lines are used as bidirectional data lines during the time Ea is high.

DUAL-PORT RAM

The dual-port memory unit contains 256 bytes of dual-port RAM that is accessed from either processor. It is selected in either case by eight address lines, register select, and chip select inputs. The direction of data transfer is controlled by the respective read/write (R/$\overline{W}$a or R/$\overline{W}$b) line. The dual-port RAM enables the processors to exchange data without interfering with devices on the other bus.

Simultaneous accesses by both sides of different locations of dual-port RAM will cause no ambiguities. Simultaneous reads by both sides of the same dual-port RAM location gives the proper data to both sides. On a simultaneous write and read of the same location, the data written is put into RAM but the data read is undefined. Simultaneous writes to

the same RAM location result in undefined data being stored. Thus, simultaneous writes and simultaneous write and read to the same location should be avoided. The semaphore registers provide a tool for determining when the shared RAM is available.

SEMAPHORE REGISTERS

The dual-port memory unit contains six read/write semaphore registers. Only two bits of each register are used. Bit 7 is the semaphore (SEM) bit and bit 6 is the ownership (OWN) bit. The remaining six bits will read all zeros.

Each semaphore register is able to arbitrate simultaneous accesses to it. The semaphore register bits provide a mechanism for controlling accesses to the shared RAM but there are no hardware controls of the dual-port RAM by the semaphore registers.

Table 3 is the truth table for when a semaphore register is accessed by one of the processors. When a semaphore register is written, the actual data written is disregarded but the SEM bit is set to zero. When the register is read, the resulting SEM bit is one (for the next read). The data obtained from the read is interpreted as: SEM bit equals zero — resource available, SEM bit equals one — resource not available.

TABLE 3 — ONE PROCESSOR SEMAPHORE BIT TRUTH TABLE

Original SEM Bit	R/$\overline{W}$	Data Read	Resulting SEM Bit
0	R	0*	1
1	R	1*	1
0	$\overline{W}$	—	0
1	$\overline{W}$	—	0

*0 = Resource Available
1 = Resource Not Available

Table 4 shows the truth table if both processors read or read and write the same semaphore register at the same time. The A processor always reads the actual SEM bit. The B processor reads the SEM bit except during the simultaneous read of a clear SEM bit. This insures that during a simultaneous read, only the A processor reads a clear SEM bit and therefore has priority to the shared RAM.

TABLE 4 — SIMULTANEOUS ACCESS OF OF SEMAPHORE REGISTER TRUTH TABLE

Original	A Processor		B Processor		Resulting
SEM Bit	R/$\overline{W}$	Data Read	R/$\overline{W}$	Data Read	SEM Bit
0	R	0*	R	1*	1
1	R	1*	$\overline{W}$	—	0
1	$\overline{W}$	—	R	1*	0
1	R	1*	R	1*	1

*0 = Resource Available
1 = Resource Not Available

The ownership bit is a read-only bit that indicates which processor last set the SEM bit. The OWN bit is set to a one whenever the SEM bit is set from zero to one. The OWN bit as read by one processor is the complement of the bit read by the other processor.

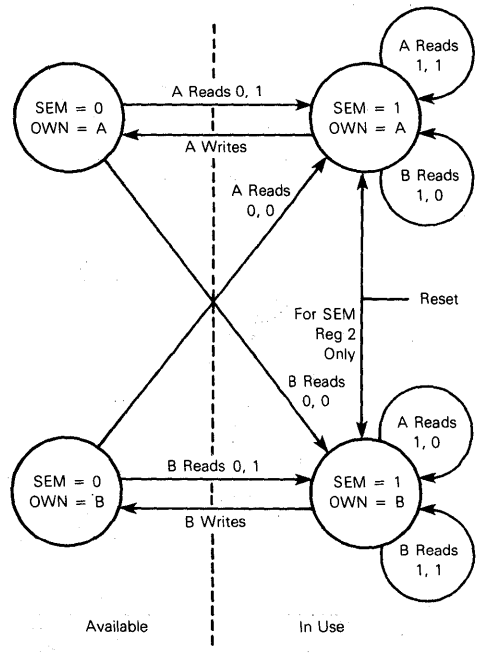
The reset state of the semaphore registers is defined in Table 5. The A processor owns all of the semaphore registers except the second semaphore register which is owned by the B processor.

TABLE 5 — RESET STATE OF SEMAPHORE REGISTERS

Semaphore Register Number	A Processor		B Processor	
	SEM Bit	OWN Bit	SEM Bit	OWN Bit
1	1	1	1	0
2	1	0	1	1
3	1	1	1	0
4	1	1	1	0
5	1	1	1	0
6	1	1	1	0

A state diagram for a semaphore register is shown in Figure 3.

FIGURE 3 — STATE DIAGRAM FOR SEMAPHORE REGISTER



NOTES:
1. Writes to a semaphore register are valid only if SEM = 1 and OWN = 1.
2. When A and B simultaneously read a semaphore register, the hardware handles it as a read by A followed by a read by B.

INTERRUPT REGISTERS

The dual-port memory unit contains two addressable locations at F8 and F9 on both sides that control the interrupt ($\overline{IRQ}$) operation between the processors. Although there is only one hardware register for each side, for purposes of explanation the register accessed at location F8 is referred to

Other

as the IRQX status register and the register accessed at location F9 is referred to as the IRQX control register (refer to Table 6). The registers each consisting of two bits have identical bit arrangements. Bit 6 is the enable bit and bit 7 is the flag bit. The other six bits are not used and always read as zero. When $\overline{RESET}$ is asserted, both bits are cleared to zero.

Table 7 summarizes the bits involved when reading or writing to the status or control registers at F8 or F9. The enable bits on either side (A or B) track the data that is written into the status register from that side. Writes to the control register do not alter data. The actual data written is disregarded but the action sets the flag bit in the other side's register and asserts an interrupt signal if enabled.

The following describes how the B side interrupt is asserted from the A side. The A side interrupt is controlled in a similar manner.

When the enable bit in the IRQb status register is set (bit 6 = 1), a write to IRQa control register sets the flag bit in the IRQb status register (bit 7 = 1) and causes an interrupt on the B side by setting the IRQb pin low. Reading the IRQb status register reads the state of the B side enable and flag bits. Reading the IRQb control register also reads the enable and flag bits but in addition, clears the B side flag bit (bit 7 = 0) and clears the B side interrupt by removing the low condition on the IRQb pin.

The enable bit in the IRQb status register (bit 6) is changed by writing the proper data to bit 6 of the IRQb status register. If the B side enable bit is zero, interrupts are prevented on the B side. However, a write to the IRQa control register still sets the B side flag bit.

INTERNAL REGISTER ADDRESSES

Table 8 shows the address of the RAM, $\overline{IRQ}$, and semaphore registers. The addresses to these registers are the same whether accessed from the A or B side. The address and data buses are multiplexed on the A side. The B side has separate address and data buses. The B side can be used on a multiplexed bus by connecting the corresponding address and data bit pins together (A0 to D0, A1 to D1, etc.) and using the B side address strobe input pin.

TABLE 6 — IRQ REGISTERS

Location	Register Name	Bit 7	Bit 6	Bits 5 to 0
A Side F8	IRQa Status	Flag	Enable	Not Used
A Side F9	IRQa Control	Flag	Enable	Not Used
B Side F8	IRQb Status	Flag	Enable	Not Used
B Side F9	IRQb Control	Flag	Enable	Not Used

TABLE 7 — INTERRUPT OPERATION

Operation	Action Taken
A Reads IRQa Status at F8	Read EA and FA
A Writes IRQa Status at F8	Writes to EA
A Reads IRQa Control at F9	Read EA and FA; Clear FA
A Writes IRQa Control at F9	Set FB; Assert IRQB if Enabled
B Reads IRQb Status at F8	Read EB and FB
B Writes IRQb Status at F8	Writes to EB
B Reads IRb Control at F9	Read EB and FB; Clear FB
B Writes IRQb Control at F9	Set FA; Assert IRQA if Enabled

F8 and F9 are Address Locations
EA and FA are A Side Enable and Flag Bits
EB and FB are B Side Enable and Flag Bits

TABLE 8 — REGISTER LOCATIONS

RS	Address	Register Name
0	00-FF	Dual Ported RAM
1	00-07	IRQ and Semaphore
1	08-0F	IRQ and Semaphore
1	10-17	IRQ and Semaphore
1	18-1F	IRQ and Semaphore
1	• • •	IRQ and Semaphore
1	E0-E7	IRQ and Semaphore
1	E8-EF	IRQ and Semaphore
1	F0-F7	IRQ and Semaphore
1	F8-FF	IRQ and Semaphore

Where:
X is 0 through F of the upper four bits of the address (note that only the lower three bits of the address are decoded):
X0 and X8 IRQa or IRQb Status
X1 and X9 IRQa or IRQb Control
X2 and XA Semaphore 1
X3 and XB Semaphore 2
X4 and XC Semaphore 3
X5 and XD Semaphore 4
X6 and XE Semaphore 5
X7 and XF Semaphore 6

Other

MOTOROLA

MCM6836E16
MCM6836R16

Advance Information

128K-BIT COMBINATION ROM/EEPROM MEMORY UNIT

The MCM6836E16/MCM6836R16 Combination ROM/EEPROM Memory (CREEM) is a 16K byte combination memory device with 14K bytes of mask programmable ROM and 2K bytes of electrically erasable programmable ROM (EEPROM). It is designed for handling data in applications requiring nonvolatile memory and in-system reprogramming to a portion of the memory. The MCM6836 saves time and money because of the in-system erase and reprogram capability of its 2K bytes of EEPROM. The industry standard pinout in a 28-pin dual-in-line package makes the MCM6836( )16 compatible with 128K-bit ROMs and EPROMs.

For easy use, the MCM6836( )16 device operates in the read mode from a single power supply and has a static power down mode. The MCM6836R16 version has a 256 byte user programmable redundancy EEPROM on chip. It can be programmed by the user to replace any page of 256 bytes of memory in the mask ROM or EEPROM sections.

The following are some of the major features of the MCM6836( )16.

- 128K-Bit ROM/EEPROM Combination Memory Organized as 16,384 × 8 Bytes
- Lowest Order 2K Bytes are Bulk Erasable EEPROM
- Remaining 14K Bytes are Mask Programmed ROM
- Packaged in Standard 28-Pin DIP
- Pin Compatible with 128K-Bit ROMs and EEPROMs
- In the Read Operating Mode Only +5 V Power Supply is Required
- +21 Vdc Programming Power Supply
- Bulk Erase
- 256 Bytes of Spare Memory are Included on Chip (MCM6836R16 Only)
- Seven Operating Modes: Read, Standby, Program, Erase, Verify, Replace (MCM6836R16 Only), and Erase-of-Replace (MCM6836R16 Only)

ORDERING INFORMATION (T_A = 0°C to 70°C)

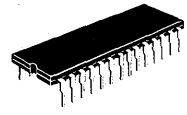
Package Type	Order Number
Cerdip	MCM6836E16S
S Suffix	MCM6836R16S
Plastic	MCM6836E16P
P Suffix	MCM6836R16P

This document contains information on a new product. Specifications and information herein are subject to change without notice.

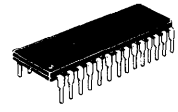
HMOS

HIGH-DENSITY N-CHANNEL PROCESS

128K-BIT COMBINATION ROM/EEPROM MEMORY

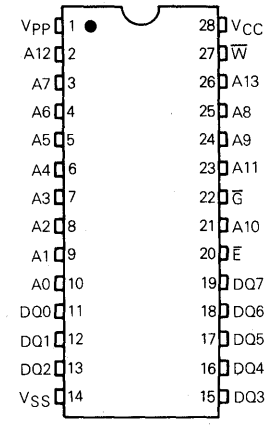


S SUFFIX
CERDIP PACKAGE
CASE 733



P SUFFIX
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT



Pin Names

A0-A13	Address
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write
DQ0-DQ7	Data
V_{PP}	Program Voltage
V_{CC}	+5 V Power Supply
V_{SS}	Ground

Other

FIGURE 1 — MCM6836( )16 EEPROM MEMORY UNIT BLOCK DIAGRAM

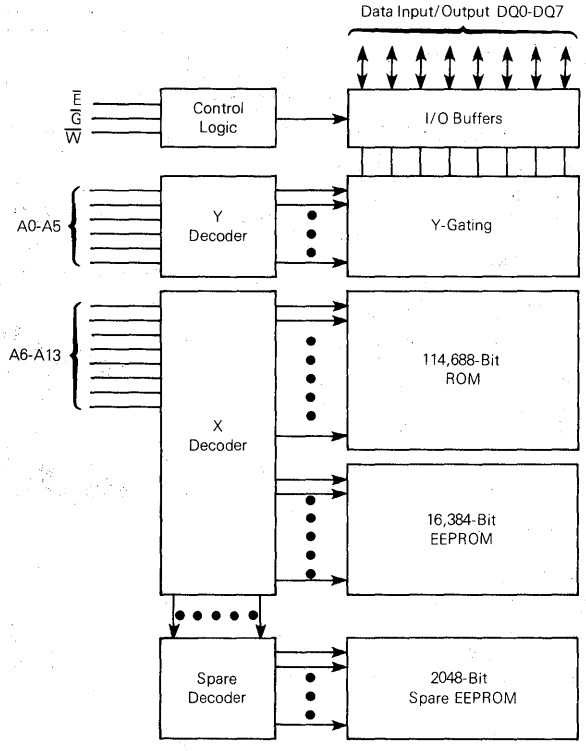
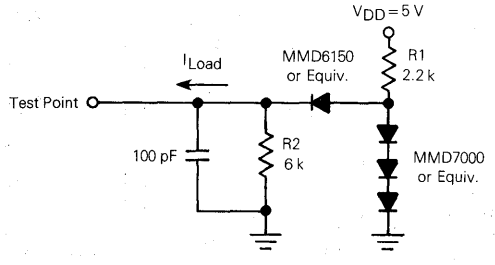


FIGURE 2 — AC TEST LOAD



Other

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Programming Voltage	V_{PP}	−0.3 to +22	V
Input Voltage			
Mode Programming Pin	V_{IHH}	−0.3 to +19	V
All Other Inputs	V_{in}	−0.3 to +7	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance			
Cerdip	θ_{JA}	60	°C/W
Plastic		100	

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts − Chip Internal Power

$P_{PORT} \equiv$ Port Power Dissipation, Watts − User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

OPERATING DC ELECTRICAL CHARACTERISTICS ($V_{CC} = V_{PP} = 5.0$ V ± 10%, $V_{SS} = 0$ Vdc, $T_A = 0°$ to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Output High Voltage ($I_{Load} = -400\ \mu A$)	V_{OH}	2.4	–	V
Output Low Voltage ($I_{Load} = 2.1$ mA)	V_{OL}	–	0.4	V
Input High Voltage	V_{IH}	2.0	V_{CC}	V
Input Low Voltage All Inputs (Except V_{PP})	V_{IL}	−0.1	0.8	V
Input High Voltage V_{PP} (Normal Operating Mode)	V_{IH}	V_{CC}	V_{CC}	V
Supply Current Measured at $T_A = 0°C$ in Read Mode Operation ($V_{CC} = 4.5$ to 5.5 V)	I_{CC}	–	100	mA
Input Low Current ($V_{IL} = 0$)	I_{IL}	–	−10	μA
Input High Current ($V_{IH} = 5.25$ V)	I_{IH}	–	10	μA
Hi-Z Output Leakage Current Low ($V_{out} = 0.4$ V)	I_{OZL}	–	−10	μA
Hi-Z Output Leakage Current High ($V_{out} = 5.5$ V)	I_{OZH}	–	10	μA
Capacitance				
Output ($V_{out} = 0$)	C_{out}	–	12	pF
Input ($V_{in} = 0$)	C_{in}	–	10	pF
V_{PP} Current	I_{PP}	–	12	mA
Supply Current During Standby, Measured at $T_A = 0°C$ ($V_{CC} = 4.5$ to 5.5 V, $\overline{E} \geq V_{IH}$, $\overline{G} \geq V_{IH}$)	$I_{CC(SB)}$	–	25	mA

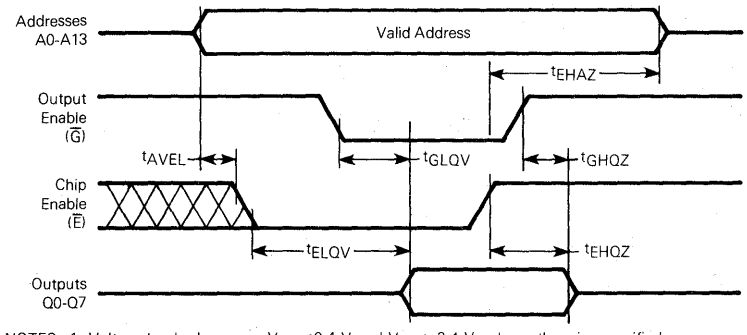
NOTES: 1. In normal read operation, if the V_{PP} pin is connected to V_{CC}, then the total I_{CC} current will be the sum of the total supply and the V_{PP} current.

2. In all cases, V_{CC} and V_{IHH} must be applied simultaneously with or prior to V_{PP}, V_{CC} and V_{IHH} must be switched off simultaneously with or after V_{PP}.

READ MODE AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Max	Unit
Access Time (From Chip Enable)	t_{ELQV}	–	250	ns
Access Time (From Output Enable)	t_{GLQV}	–	100	ns
Address Hold Time (From Chip Enable)	t_{EHAZ}	0	–	ns
Address Setup Time	t_{AVEL}	0	–	ns
Disable Time (From Output Enable)	t_{GHQZ}	0	80	ns
Disable Time (From Chip Enable)	t_{EHQZ}	10	80	ns

READ MODE TIMING DIAGRAM



NOTES: 1. Voltage levels shown are $V_{OL} \leq 0.4$ V and $V_{OH} \geq 2.4$ V unless otherwise specified.
2. Timing level measurement points are 0.8 V and 2.0 V unless otherwise specified.
3. $\overline{G}$ may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of $\overline{E}$ without impact on t_{ELQV}.

PROGRAMMING OPERATION DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = 25°C unless otherwise noted)

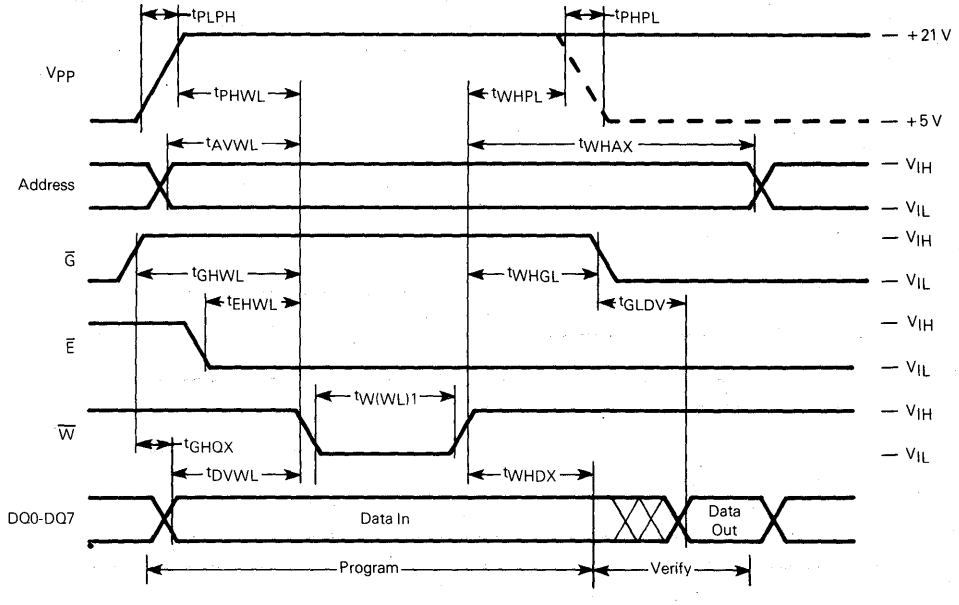
Characteristic	Symbol	Min	Typ	Max	Unit
Programming Voltage (V_{PP} Pin)	V_{PP}	20	21	22	V
Input High Voltage For Data	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	–0.1	–	0.8	V
Address, $\overline{E}$, $\overline{G}$, and $\overline{W}$ Sink Current (V_{in} = 5.25 V/0.4 V)	I_{leak}	–	–	10	μA
V_{PP} Supply Current (V_{PP} = 21 ± 1 V, $\overline{W}$ = V_{IH})	I_{PP1}	–	–	10	mA
V_{PP} Programming Pulse Supply Current (V_{PP} = 21 ± 1 V, $\overline{W}$ = V_{IL})	I_{PP2}	–	–	10	mA
V_{CC} Supply Current	I_{CC}	–	–	115	mA

Other

PROGRAMMING OPERATION AC TIMING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, V_{PP} = 21 ± 1 V, T_A = 25°C)

Characteristic	Symbol	Min	Max	Unit
V_{PP} Rise Time	t_{PLPH}	50	–	ns
V_{PP} Fall Time	t_{PHPL}	50	–	ns
V_{PP} Setup Time	t_{PHWL}	2.0	–	µs
V_{PP} Hold Time	t_{WHPL}	2.0	–	µs
Address Setup Time	t_{AVWL}	2.0	–	µs
Address Hold Time	t_{WHAX}	2.0	–	µs
Output Enable High to Program Pulse	t_{GHWL}	2.0	–	µs
Output Enable Hold Time	t_{WHGL}	2.0	–	µs
Chip Enable Setup Time	t_{EHWL}	2.0	–	µs
Output Disable to Hi-Z Output	t_{GHQX}	0.1	100	ns
Data Setup Time	t_{DVWL}	2.0	–	µs
Data Hold Time	t_{WHDX}	2.0	–	µs
Program Pulse Width	$t_{W(WL)1}$	1.0	10	ms
Output Enable to Valid Data	t_{GLDV}	–	200	ns

PROGRAMMING OPERATION TIMING DIAGRAM



Other

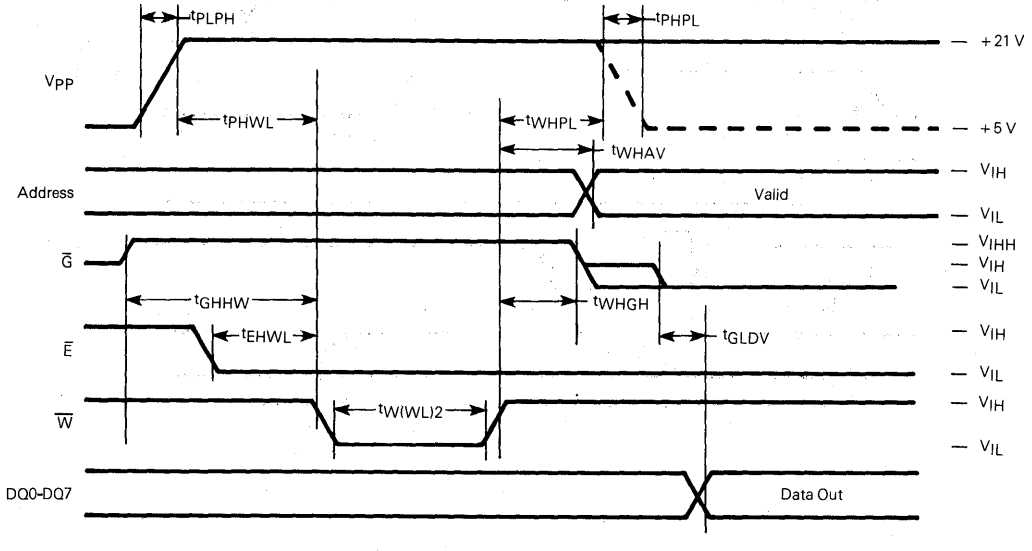
ERASE OPERATION DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, V_{PP} = 21 ± 1 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current for Any Input @ V_{in}	I_{leak}	–	–	10	μA
V_{CC} Supply Current (Outputs Open, $\overline{W} = V_{IL}$)	I_{CC}	–	–	115	mA
V_{PP} Supply Current ($\overline{W} = V_{IL}$)	I_{PP}	–	5	10	mA
Input Low Level	V_{IL}	−0.1	–	0.8	V
Input High Level	V_{IH}	2.0	–	V_{CC}	V
Input Mode Select High	V_{IHH}	12	15	19	V

ERASE OPERATION AC TIMING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, V_{PP} = 21 ± 1 Vdc, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{PP} Rise Time	t_{PLPH}	50	–	–	ns
V_{PP} Fall Time	t_{PHPL}	50	–	–	ns
V_{PP} Setup Time	t_{PHWL}	2.0	–	–	μs
V_{PP} Hold Time	t_{WHPL}	2.0	–	–	μs
Address Delay Time	t_{WHAV}	2.0	–	–	μs
Output Enable Setup Time	t_{GHHWL}	2.0	–	–	μs
Output Enable Hold Time	t_{WHGH}	2.0	–	–	μs
Chip Enable Setup Time	t_{EHWL}	2.0	–	–	μs
Erase Pulse Width	$t_{W(WL)2}$	1.0	10	100	ms
Output Enable to Invalid Data	t_{GLDV}	–	–	200	ns

ERASE OPERATION TIMING DIAGRAM

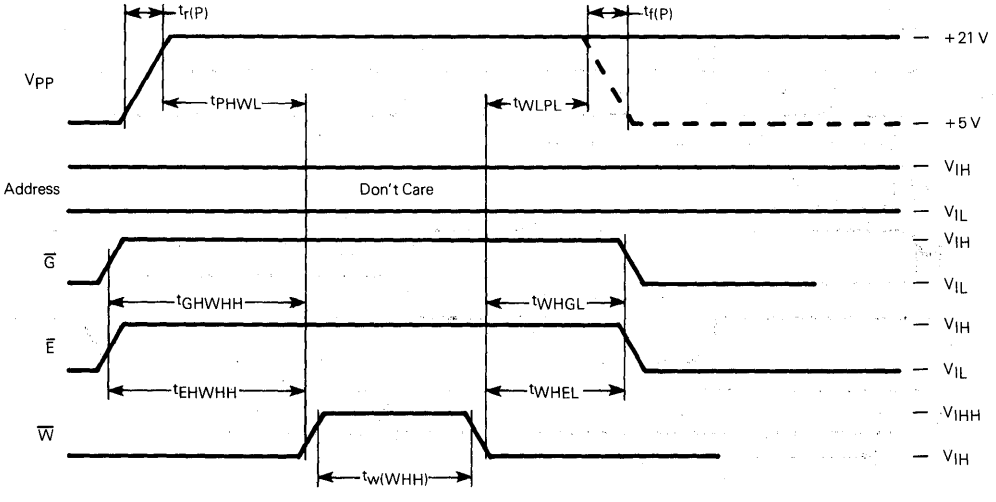


Other

ERASE-OF-REPLACE OPERATION AC TIMING CHARACTERISTICS (V_{CC} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, V_{PP} = 21 ± 1 Vdc, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{PP} Rise Time	$t_{r(P)}$	50	–	–	ns
V_{PP} Fall Time	$t_{f(P)}$	50	–	–	ns
V_{PP} Setup Time	t_{PHWL}	2.0	–	–	μs
V_{PP} Hold Time	t_{WLPL}	2.0	–	–	μs
Output Enable Setup Time	t_{GHWHH}	2.0	–	–	μs
Output Enable Hold Time	t_{WHGL}	2.0	–	–	μs
Chip Enable Setup Time	t_{EHWHH}	2.0	–	–	μs
Chip Enable Hold Time	t_{WHEL}	2.0	–	–	μs
Erase-of-Replace Pulse Width	$t_{w(WHH)}$	10	–	–	ms

ERASE-OF-REPLACE OPERATION TIMING DIAGRAM

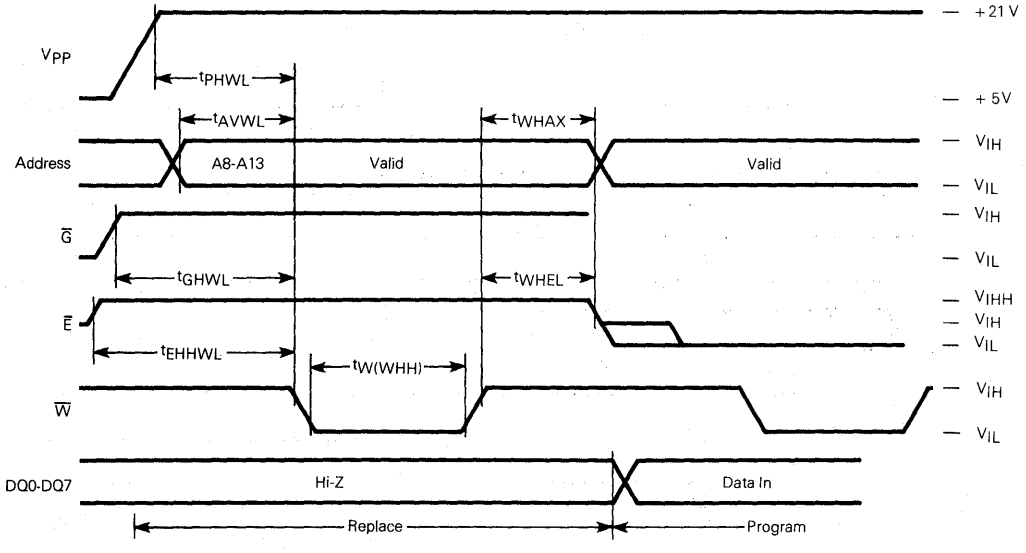


Other

REPLACE OPERATION AC TIMING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, V_{PP} = 21 ± 1 Vdc, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{PP} Setup Time	t_{PHWL}	2.0	–	–	μs
Address Setup Time	t_{AVWL}	2.0	–	–	μs
Address Hold Time	t_{WHAX}	2.0	–	–	μs
Output Enable Setup Time	t_{GHWL}	2.0	–	–	μs
Chip Enable Setup Time	t_{EHHWL}	2.0	–	–	μs
Chip Enable Hold Time	t_{WHEH}	2.0	–	–	μs
Replace Pulse Width	$t_{W(WL)3}$	50	100	–	ms

REPLACE OPERATION TIMING DIAGRAM



Other

FUNCTIONAL DESCRIPTION

INTRODUCTION

The MCM6836( )16 Combination ROM/EEPROM (CREEM) is a 128K bit memory device containing 2K bytes of EEPROM and 14K bytes of mask programmed ROM. The EEPROM is located in the lower 2K byte section of memory, at addresses $0000 to $07FF, and the mask ROM is located in the upper 14K byte section of memory at addresses $0800 to $3FFF. The MCM6836R16 contains an additional 256 bytes of spare memory. This redundant memory allows for the replacement of a 256 byte block of memory in either mask ROM or EEPROM. The MCM6836E16, without redundancy, is also available. The MCM6836( )16 is contained in a standard 28-pin dual in-line package.

The MCM6836( )16 incorporates several operating modes which make the device easy to use and test. These modes which are illustrated in Figure 3 include: Read, Standby, Program, Erase, Verify, Replace, and Erase-Of-Replace (Replace and Erase-Of-Replace modes are used in the MCM6836R16 only). The pin voltages (signals) required for each mode are also illustrated in Figure 3 and a functional description of each operating mode is provided below. The read and standby modes allow the device to be used as a conventional ROM, the program mode allows programming of individual bytes in the EEPROM, and the erase mode allows the entire EEPROM contents to be erased to the logic high state in approximately 10 milliseconds.

In the MCM6836R16, the replace mode allows substitution of any 256-byte page in the mask ROM or EEPROM memory space with an erased page of EEPROM which can then be programmed. The substitution is performed as a single block of memory, and on-chip logic determines if mask ROM or EEPROM has been replaced. If EEPROM has been replaced, the redundant memory and the memory it has replaced are erased when the standard EEPROM is erased. If the substitution is for mask ROM, the spare memory is erased only by the erase replace mode which has unique control functions. This allows the spare memory to contain the same characteristics as the normal memory for which it is substituted.

OPERATING MODES

The MCM6836E16/MCM6836R16 (CREEM) incorporates five common operating modes, plus two more modes for the MCM6836R16, which make the device easy to use and test. The following paragraphs provide a detailed discussion of each of these modes. In addition, Figure 3 provides a chart illustrating how the various pins are affected during each of the operating modes.

NOTE

It is possible to erase spare EEPROM even if it is used as ROM (or isn't being used) when the following erroneous pin connections are made: E and $G = V_{IHH}$, $V_{PP} = V_{PP}$, and $W = V_{IL}$.

Read Mode – this mode allows the MCM6836( )16 to be used like any conventional mask ROM. In order to read the device in this mode, E and $\overline{G}$ must be held low (V_{IL}), V_{PP} is connected to V_{CC}, and a valid address accessed for data output. The W pin can be in either state (don't care). Some characteristics of the read mode are:

1. Data is available 250 nanoseconds after valid addresses or after the falling edge of $\overline{E}$.
2. Data is valid 100 nanoseconds after the trailing edge of $\overline{G}$ provided $\overline{E}$ and stable addresses have been present for 150 nanoseconds or more.
3. Current is less than 100 milliamperes at 0°C.

Standby Mode – In this mode the MCM6836( )16 is disabled. In order to enter this mode, $\overline{E}$ and $\overline{G}$ must be at a logic high level (V_{IH}), and V_{PP} must be connected to V_{CC}. The $\overline{W}$ and address line can be at any state ("don't care") and the data bus will be in the high-impedance state. (Hi-Z). Some characteristics of the standby mode are:

1. Data outputs are high impedance.
2. Current is reduced 75% to less than 25 milliamperes at 0°C.

Program Mode – In this mode, individual bytes (memory locations) in the EEPROM may be programmed in approximately 10 milliseconds. (A memory location must be erased to the all ones state before it can be programmed.) In order to enter this mode and program the EEPROM, $\overline{E}$ must be at a logic low (V_{IL}), $\overline{G}$ at a logic high (V_{IH}), and V_{PP} must be held at +21 Vdc. A 10 millisecond negative-going pulse on $\overline{W}$ will then allow the input data to be programmed into the addresses accessed in the EEPROM. Some characteristics of the program mode are:

1. Although only zeros are programmed into the device, both ones and zeros can be present in the data word.
2. Requires +21 Vdc programming voltage supply.

FIGURE 3 – OPERATING MODES AND CONTROL VOLTAGES

	$\overline{E}$	$\overline{G}$	V_{PP}	$\overline{W}$	Address	Data
Read	V_{IL}	V_{IL}	V_{CC}	X	Valid	D_{out}
Standby	V_{IH}	V_{IH}	V_{CC}	X	X	Hi-Z
Program	V_{IL}	V_{IH}	V_{PP}	⎍ V_{IH}	Valid	D_{in}
Erase	V_{IL}	V_{IHH}	V_{PP}	⎍ V_{IH}	X	Hi-Z
Verify	V_{IL}	V_{IL}	V_{PP}	V_{IH}	Valid	D_{out}
Replace#	V_{IHH}	V_{IH}	V_{PP}	⎍ V_{IH}	Valid	Hi-Z
Erase-of-Replace#	V_{IH}	V_{IH}	V_{PP}	⎍ V_{IHH}	X	Hi-Z

# Indicates used in MCM6836R only.

NOTE: It is possible to erase spare EPROM even if it is used as ROM (or isn't being used) when the following erroneous pin connections are made: $\overline{E}$ and $\overline{G} = V_{IHH}$, $V_{PP} = V_{PP}$, and $\overline{W} = V_{IL}$.

Erase Mode – This mode allows the contents of the EEPROM to be erased to all ones. In order to enter this mode and erase the EEPROM, $\overline{E}$ must be held low (V_{IL}), $\overline{G}$ must be held at V_{IHH}, and V_{PP} must be held at +21 Vdc. A 10 millisecond negative-going pulse on $\overline{W}$ will then erase the EEPROM to the all ones state. Address lines can be in any state and the data bus will be in the high-impedance state (Hi-Z). Some characteristics of the erase mode are:

1. Bulk erase returns the entire EEPROM array to all ones.
2. A +21 Vdc programming voltage supply is required.

Verify Mode – In this mode the contents of the EEPROM can be verified as all ones after erasure and the contents of the data byte can be verified after programming. In order to enter this mode and verify EEPROM and/or data byte contents, $\overline{E}$ and $\overline{G}$ must be held at V_{IL}, and V_{PP} must be held at +21 Vdc. The $\overline{W}$ line must be held high (V_{IH}) and a valid address must be applied to the address lines accessing the EEPROM locations (to obtain data output). Some characteristics of the verify mode are:

1. Allows quick verification of the data byte which was written during the previous cycle.
2. Verification may be performed after each program or erase cycle.
3. Verification is accomplished by performing a read cycle with V_{PP} at +21 Vdc and $\overline{W}$ held at V_{IH}.

Replace Mode (MCM6836R16 only) – The replace mode allows for substitution of any 256 byte page in the mask ROM or EEPROM memory with an erased page of EEPROM which can then be programmed. The substitution is performed as a single block of memory and on-chip logic determines if mask ROM or EEPROM is to be replaced. If EEPROM is replaced, the redundant memory and the memory it has replaced is erased when the standard EEPROM is erased. If the substitution is for mask ROM, the spare memory can be erased only in the erase-of-replace mode, which has unique control functions. Thus, the spare memory assumes the same characteristics as the normal memory for which it was substituted.

To replace a block of memory, $\overline{E}$ must be held at V_{IHH}, $\overline{G}$ must be held at V_{IH}, and V_{PP} must be held at +21 Vdc. Then, a 100 millisecond negative-going pulse on $\overline{W}$ will substitute the spare memory when the beginning address of the section of memory to be replaced is set on address lines A8-A13.

The replace operation programs special EEPROM devices which: (1) program replacement addresses into a spare row decoder, (2) determine if the address space is in mask ROM or EEPROM, (3) enable the spare memory, and (4) prevent "overprogramming" the replacement address. Data is then programmed into the spare memory by using the program mode. If this section of memory is addressed during the read or program mode, a signal is generated that disables all normal row decoders.

Some characteristics of the replace mode are:

1. Substitutes 256 bytes of spare EEPROM for 256 bytes of either mask ROM or EEPROM.
2. Performed as a single block of memory.
3. On-chip logic determines if mask ROM or EEPROM is to be replaced.
4. When in the replace mode, special EEPROM devices are programmed which:
   A. Program replacement addresses into a spare row decoder,
   B. Determine if the address space is in mask ROM or EEPROM,
   C. Enable the spare memory, and
   D. Prevent "overprogramming" the replacement address.

Data is then programmed into spare memory using the program mode.

Erase-Of-Replace Mode (MCM6836R16 only) – This mode is used, when spare memory (redundancy) is being used, to erase the replace mask ROM. To erase the spare memory to all ones, $\overline{E}$ and $\overline{G}$ must be held at V_{IH}, and V_{PP} must be held at +21 Vdc. Then, a 10 millisecond positive-going (to V_{IHH}) pulse on $\overline{W}$ will erase the spare memory to the all ones state. This mode also erases the programmed address to the redundancy EEPROM. During the erase-of-replace mode, the address lines can be at any state and the data bus is in the high-impedance state. Some characteristics of the erase-of-replace mode are:

1. Returns the device to its original condition by erasing the replace circuitry, spare decoder, and spare memory.
2. Needed only for a device which contains redundancy as a user option.
3. False erasure of redundancy memory is unlikely due to unique control function ($\overline{W}$ pulse).

NOTE

The erase-of-replace mode need only be used if spare memory is being used to replace a section of mask ROM. This operation erases the replacement circuitry, spare decoder, and spare memory after which the device is returned to its original condition.

FUNCTIONAL PIN DESCRIPTION

V_{PP}

This pin is used as the +21 Vdc input voltage during EEPROM programming and erasing operations. It is connected to V_{CC} in the normal operating read and standby modes. V_{PP} should not, in any case, be applied before the device has been powered by V_{CC} or after V_{CC} has been removed from the device.

WRITE ($\overline{W}$)

The active low state (V_{IL}) of this input pin is used to program and erase the EEPROM. It is also used as a mode select pin for the erase-of-replace mode when V_{IHH} is applied to its input. In the normal read and standby operating modes, this pin is a "don't care".

CHIP ENABLE ($\overline{E}$)

The active low state (V_{IL}) of this input pin is used as a chip select signal for the read, program, erase, and verify operating modes. It is also used as a mode select input signal for the replace mode when V_{IHH} is applied. It is used as a mode select signal for the standby and erase-of-replace modes when V_{IH} is applied.

OUTPUT ENABLE ($\overline{G}$)

The active low state (V_{IL}) of this input pin is used in conjunction with $\overline{E}$ to enable the output buffer of this device. It is also used as a mode select signal for the erase mode when V_{IHH} is applied.

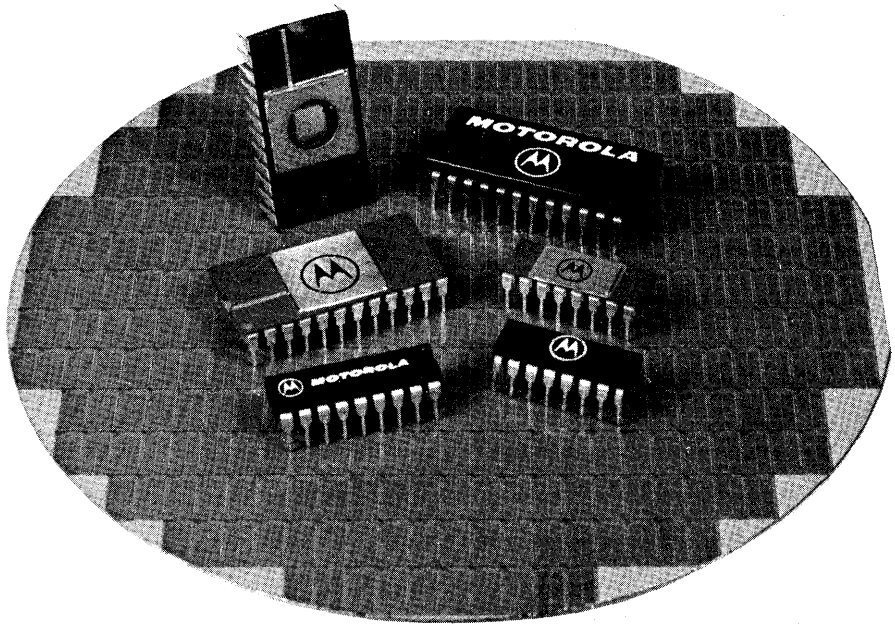
DATA BUS (DQ0-DQ7)

These eight pins provide a bidirectional data link to the system bus.

ADDRESS INPUTS (A0-A13)

These 14 address inputs allow any of the 14K bytes of mask ROM and 2K bytes of EEPROM to be uniquely selected in the read mode. Addresses $0000 to $07FF are designated as EEPROM, and addresses $0800 to $3FFF are designated as the mask programmable ROM. These address inputs are also used to select an address byte for programming, verifying, and replacing.

TTL RAMs



MOTOROLA

MCM93415

1024-BIT RANDOM ACCESS MEMORY

TTL
1024 X 1 BIT
RANDOM ACCESS MEMORY

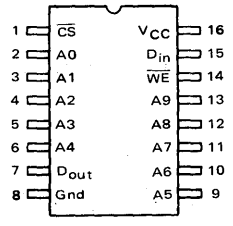
The MCM93415 is a 1024-bit Read/Write RAM organized 1024 words by 1 bit.

The MCM93415 is designed for buffer control storage and high performance main memory applications, and has a typical access time of 35 ns.

The MCM93415 has full decoding on-chip, separate data input and data output lines, and an active low chip select. The device is fully compatible with standard DTL and TTL logic families and features an uncommitted collector output for ease of memory expansion.

- Uncommitted Collector Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed –
  - Access Time – 35 ns Typical
  - Chip Select – 15 ns Typical
- Power Dissipation Decreases with Increasing Temperature
- Power Dissipation 0.5 mW/Bit Typical
- Organized 1024 Words X 1 Bit

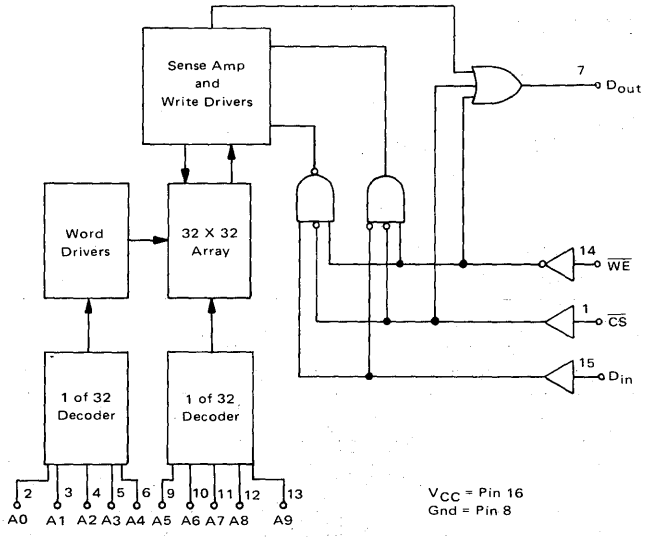
PIN ASSIGNMENT



Pin Designation

$\overline{CS}$	Chip Select
A0 – A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MCM93415 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of Chip Select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ held low and the chip selected, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held high and the chip selected. Data in the specified location is presented at D_{out} and is non-inverted.

Uncommitted collector outputs are provided to allow wired-OR applications. In any application an external pull-up resistor of R_L value must be used to provide a high at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}(Min)}{I_{OL} - FO(1.6)} \leqslant R_L \leqslant \frac{V_{CC}(Min) - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output High Level at Output Node
I_{OL} = Output Low Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA High/1.6 mA Low.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	
Ceramic Package (D and F Suffix)	-55°C to +165°C
Plastic Package (P Suffix)	-55°C to +125°C
Operating Junction Temperature, T_J	
Ceramic Package (D and F Suffix)	< 165°C
Plastic Package (P Suffix)	< 125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage (dc)	-0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	-0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	-12 mA to +5.0 mA

TRUTH TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{in}	Open Collector	Mode
H	X	X	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

GUARANTEED OPERATING RANGES (Note 2)

Part Number	Supply Voltage (V_{CC}) Min	Nom	Max	Ambient Temperature (T_A)
MCM93415DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM93415FM, DM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

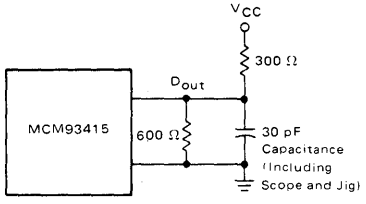
Symbol	Characteristic	Limits Min	Max	Unit	Conditions	
V_{OL}	Output Low Voltage		0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	2.1		Vdc	Guaranteed Input High Voltage for All Inputs	
V_{IL}	Input Low Voltage		0.8	Vdc	Guaranteed Input Low Voltage for All Inputs	
I_{IL}	Input Low Current		-400	μAdc	V_{CC} = Max, V_{in} = 0.4 V	
I_{IH}	Input High Current		40	μAdc	V_{CC} = Max, V_{in} = 4.5 V	
			1.0	mAdc	V_{CC} = Max, V_{in} = 5.25 V	
I_{CEX}	Output Leakage Current		100	μAdc	V_{CC} = Max, V_{out} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		-1.5	Vdc	V_{CC} = Max, I_{in} = -10 mA	
I_{CC}	Power Supply Current		130	mAdc	T_A = Max	V_{CC} = Max, All Inputs Grounded
			155	mAdc	T_A = 0°C	
			170	mAdc	T_A = Min	

AC OPERATING CONDITIONS AND CHARACTERISTICS

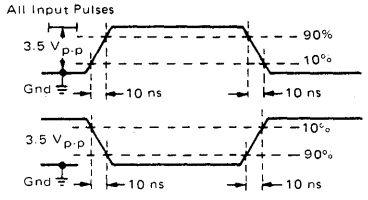
(Full operating voltage and temperature unless otherwise noted)

AC TEST LOAD AND WAVEFORM

Loading Condition



Input Pulses



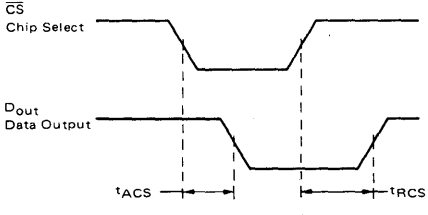
Symbol	Characteristic (Notes 2, 3)	MCM93415DC,PC Min	MCM93415DC,PC Max	MCM93415DM,FM Min	MCM93415DM,FM Max	Unit	Conditions
READ MODE	DELAY TIMES					ns	
t_{ACS}	Chip Select Time		35		45		See Test Circuit
t_{RCS}	Chip Select Recovery Time		35		50		and Waveforms
t_{AA}	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
t_{WS}	Write Disable Time		35		45		See Test Circuit
t_{WR}	Write Recovery Time		40		50		and Waveforms
	INPUT TIMING REQUIREMENTS					ns	
t_W	Write Pulse Width (to guarantee write)	30		40			See Test Circuit
t_{WSD}	Data Setup Time Prior to Write	5		5			and Waveforms
t_{WHD}	Data Hold Time After Write	5		5			
t_{WSA}	Address Setup Time (at t_W = Min)	10		15			
t_{WHA}	Address Hold Time	10		10			
t_{WSCS}	Chip Select Setup Time	5		5			
t_{WHCS}	Chip Select Hold Time	5		5			

NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola Sales Representative if extended temperature or modified operating conditions are desired.

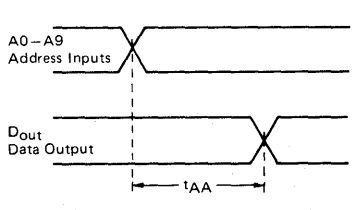
NOTE 3: The AC limits are guaranteed to be the worst case bit in the memory.

READ OPERATION TIMING DIAGRAM

Propagation Delay from Chip Select

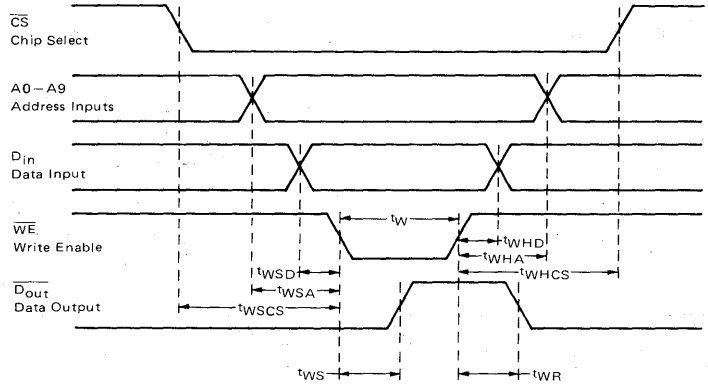


Propagation Delay from Address Inputs



(All Time Measurements Referenced to 1.5 V)

WRITE CYCLE TIMING



(All Time Measurements Referenced to 1.5 V)

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown	Still	
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W
P Suffix	65°C/W	100°C/W	25°C/W

MOTOROLA

MCM93422
MCM93L422

1024-BIT RANDOM ACCESS MEMORY

The MCM93422/MCM93L422 are 1024-bit Read/Write RAMs, organized 256 words by 4 bits, designed for high performance main memory and control storage applications.

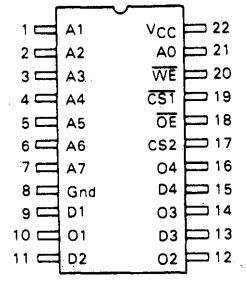
They have full decoding on-chip, separate data input and data output lines, an active low-output enable, write enable, and two chip selects, one active high, one active low. These memories are fully compatible with standard TTL logic families. A three-state output is provided to drive bus-organized systems and/or highly capacitive loads.

- Three-State Outputs
- TTL Inputs and Outputs
- Non-Inverting Data Outputs
- High Speed —
  Access Time — 30 ns Typical
  Chip Select — 15 ns Typical
- Power Dissipation — 0.26 mW/Bit Typical
- Standard 22-Pin, 400 Mil Wide Package
- Power Dissipation Decreases with Increasing Temperature
- Organized 256 Words × 4 Bits
- Two Chip Select Lines for Memory Expansion

TTL
256 × 4-BIT
RANDOM ACCESS MEMORY

MCM93422 — THREE-STATE
MCM93L422 — THREE-STATE

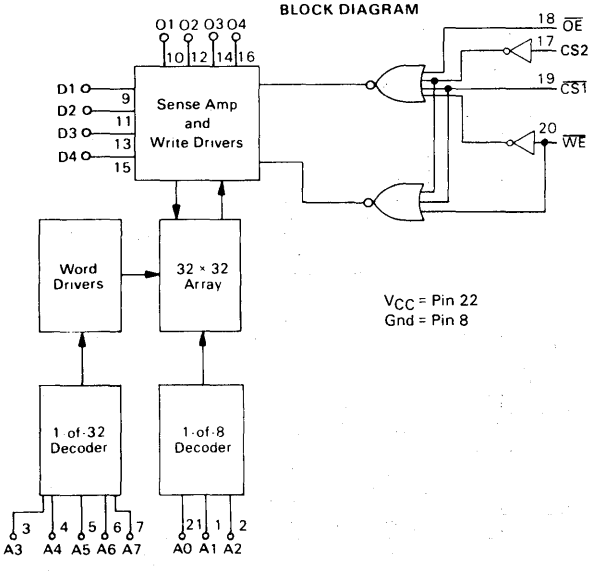
PIN ASSIGNMENT



Pin Description

$\overline{CS1}$, CS2	Chip Selects
A0-A7	Address Inputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
D1-D4	Data Inputs
O1-O4	Data Outputs

BLOCK DIAGRAM



V_{CC} = Pin 22
Gnd = Pin 8

FUNCTIONAL DESCRIPTION

The MCM93422/MCM93L422 are fully decoded 1024-bit random access memories organized 256 words by 4 bits. Word selections are achieved by means of an 8-bit address, A0–A7.

The Chip Select ($\overline{CS1}$ and CS2) inputs provide for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 20). With $\overline{WE}$ and $\overline{CS1}$ held low and the CS2 held high, the data at D_n is written into the addressed location. To read, $\overline{WE}$ and CS2 are held high and $\overline{CS1}$ is held low. Data in the specified location is presented at the output (O1–O4) and is non-inverted.

The three-state outputs of the MCM93422/MCM93L422 provide drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus-organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in a high-impedance state.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	
Ceramic Package (D Suffix)	−65°C to +150°C
Plastic Package (P Suffix)	−55°C to +125°C
Operating Junction Temperature, T_J	
Ceramic Package (D Suffix)	<165°C
Plastic Package (P Suffix)	<125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)	−0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	−0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	−12 mA to +5.0 mA

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

GUARANTEED OPERATING RANGES

Part Number	Supply Voltage (V_{CC})			Ambient Temperature (T_A)
	Min	Nom	Max	
MCM93422DC, PC MCM93L422DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range)

Symbol	Characteristic		Limits Min	Limits Max	Units	Conditions	
V_{OL}	Output Low Voltage		—	0.45	Vdc	V_{CC} = Min, I_{OL} = 8.0 mA	
V_{IH}	Input High Voltage		2.1	—	Vdc	Guaranteed Input High Voltage for all Inputs	
V_{IL}	Input Low Voltage		—	0.8	Vdc	Guaranteed Input Low Voltage for all Inputs	
I_{IL}	Input Low Current		—	−300	μAdc	V_{CC} = Max, V_{in} = 0.4 V	
I_{IH}	Input High Current		— —	40 1.0	μAdc mAdc	V_{CC} = Max, V_{in} = 4.5 V V_{CC} = Max, V_{in} = 5.25 V	
I_{off}	Output Current (High Z)			50 −50	μAdc	V_{CC} = Max, V_{out} = 2.4 V V_{CC} = Max, V_{out} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground		—	−70	mAdc	V_{CC} = Max (Note 2)	
V_{OH}	Output High Voltage		2.4	—	Vdc	V_{CC} = Min, I_{OH} = −5.2 mA	
V_{IK}	Input Diode Clamp Voltage		—	−1.5	Vdc	V_{CC} = Max, I_{in} = −10 mA	
I_{CC}	Power Supply Current	MCM93422	— —	130 155	mAdc mAdc	T_A = Max T_A = Min	V_{CC} = Max, All Inputs Grounded
		MCM93L422	— —	75 80	mAdc mAdc	T_A = Max T_A = Min	

TRUTH TABLE

Inputs					Output	Mode
$\overline{OE}$	$\overline{CS1}$	CS2	$\overline{WE}$	D1-D4	O1-O4	
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	X	X	X	X	High Z	Output Disabled
L	L	H	H	X	O1-O4	Read

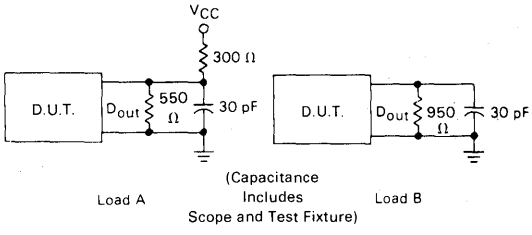
H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

AC OPERATING CONDITIONS AND CHARACTERISTICS

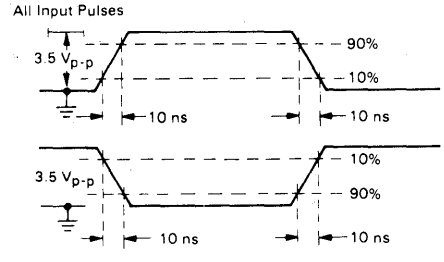
(Full operating voltage and temperature range)

AC TEST LOAD AND WAVEFORMS

Loading Conditions



Input Pulses

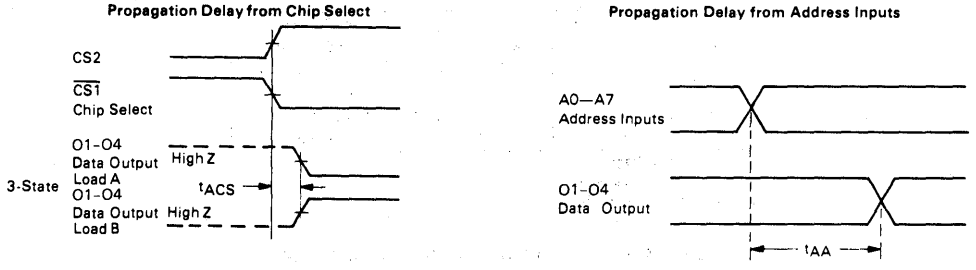


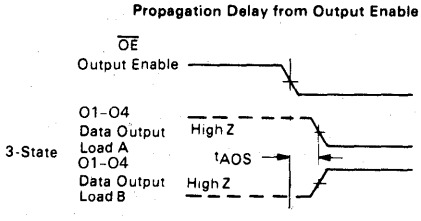
Symbol	Characteristic (Notes 2, 3, 4, 5)	MCM93422DC,PC		MCM93L422DC,PC		Units	Conditions
		Min	Max	Min	Max		
READ MODE	DELAY TIMES					ns	
t_{ACS}	Chip Select Time	—	30	—	35		See Test Circuit
t_{ZRCS}	Chip Select to High Z	—	30	—	35		and Waveforms
t_{AOS}	Output Enable Time	—	30	—	35		
T_{ZROS}	Output Enable to High Z	—	30	—	35		
t_{AA}	Address Access Time	—	45	—	60		
WRITE MODE	DELAY TIMES					ns	See Test Circuit
t_{ZWS}	Write Disable to High Z	—	35	—	40		and Waveform
t_{WR}	Write Recovery Time	—	40	—	45		
	INPUT TIMING REQUIREMENTS					ns	
t_W	Write Pulse Width (to guarantee write)	30	—	45	—		See Test Circuit
t_{WSD}	Date Setup Time Prior to Write	5.0	—	5.0	—		and Waveforms
t_{WHD}	Data Hold Time After Write	5.0	—	5.0	—		
t_{WSA}	Address Setup Time (at t_W = Min)	10	—	10	—		
t_{WHA}	Address Hold Time	5.0	—	5.0	—		
t_{WSCS}	Chip Select Setup Time	5.0	—	5.0	—		
t_{WHCS}	Chip Select Hold Time	5.0	—	5.0	—		

NOTE 2: Output short circuit conditions must not exceed 1 second duration.
3: The maximum address access time is guaranteed to be the worst-case bit in the memory.
4: Load A used to measure transitions between logic levels and from High Z state to logic Low state.
Load B used to measure transitions between High Z state to logic High state.
Load C used to measure transitions from either logic High or Low state to High Z state.
5: All time measurements are referenced to +1.5 Vdc except transitions into the High Z state where outputs are referenced to a delta of 0.5 Vdc from the logic level using Load C.

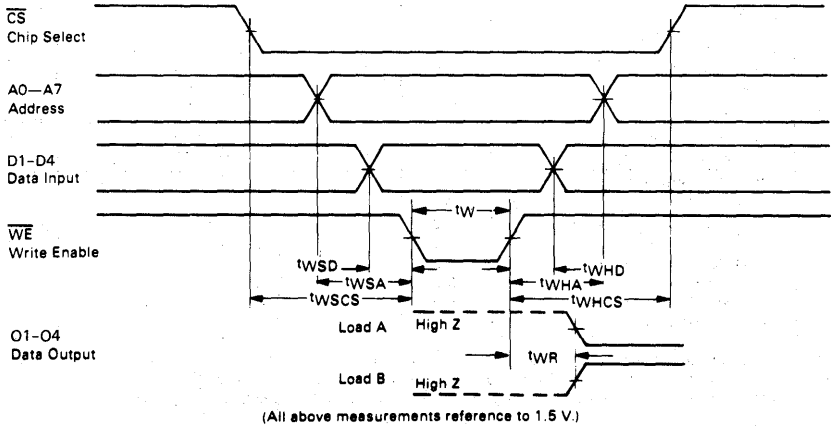
READ OPERATION TIMING DIAGRAM

(All Time Measurements Referenced to 1.5 V)



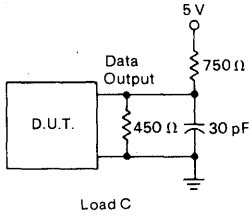


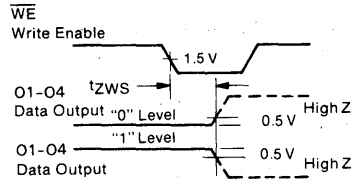
WRITE CYCLE TIMING



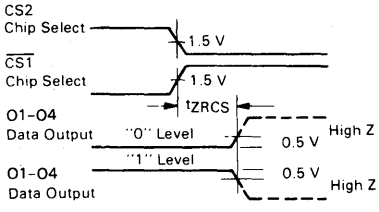
(All above measurements reference to 1.5 V.)

WRITE ENABLE TO HIGH Z DELAY

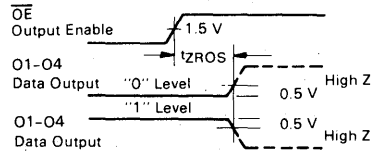




Propagation Delay from Chip Select to High Z



Propagation Delay from Output Enable to High Z



(All t_{ZXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C.)

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown*	Still	
D Suffix	50°C/W	85°C/W	15°C/W
P Suffix	50°C/W	85°C/W	15°C/W

*500 linear ft. per minute blown air

MOTOROLA

MCM93425

1024-BIT RANDOM ACCESS MEMORY

TTL
1024 X 1 BIT
RANDOM ACCESS MEMORY

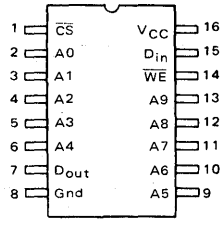
The MCM93425 is a 1024-bit Read/Write RAM, organized 1024 words by 1 bit.

The MCM93425 is designed for high performance main memory and control storage applications and has a typical address time of 35 ns.

The MCM93425 has full decoding on-chip, separate data input and data output lines, and an active low-chip select and write enable. The device is fully compatible with standard DTL and TTL logic families. A three-state output is provided to drive bus-organized systems and/or highly capacitive loads.

- Three-State Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed –
  - Access Time – 35 ns Typical
  - Chip Select – 15 ns Typical
- Power Dissipation – 0.5 mW/Bit Typical
- Power Dissipation Decreases With Increasing Temperature

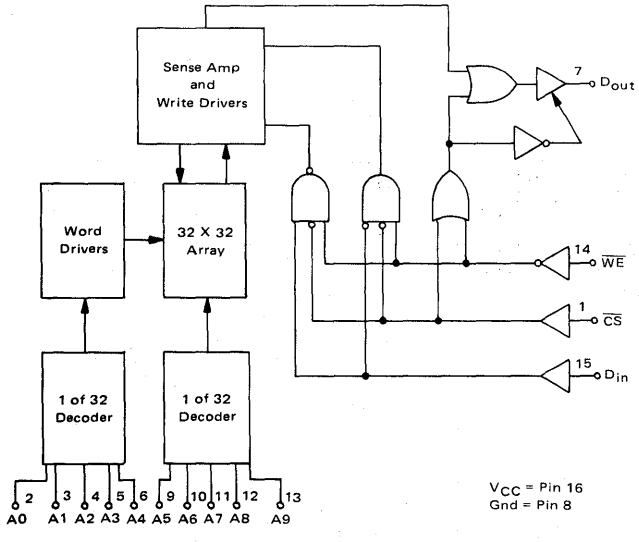
PIN ASSIGNMENT



Pin Description

$\overline{CS}$	Chip Select
A0 - A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

BLOCK DIAGRAM



NOTE: Logic driving sense amp/write drivers depicts negative-only write used on C4m.

FUNCTIONAL DESCRIPTION

The MCM93425 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A0–A9.

The Chip Select ($\overline{CS}$) input provides for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held high and $\overline{CS}$ held low. Data in the specified location is presented at D_{out} and is non-inverted.

The three-state output provides drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high-impedance state.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	
Ceramic Package (D and F Suffix)	−55°C to +165°C
Plastic Package (P Suffix)	−55°C to +125°C
Operating Junction Temperature, T_J	
Ceramic Package (D and F Suffix)	< 165°C
Plastic Package (P Suffix)	< 125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)	−0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	−0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	−12 mA to +5.0 mA

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

TRUTH TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}	Mode
H	X	X	High Z	Not Selected
L	L	L	High Z	Write "0"
L	L	H	High Z	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

GUARANTEED OPERATING RANGES (Notes 2 and 3)

Part Number	Supply Voltage (V_{CC}) Min	Nom	Max	Ambient Temperature (T_A)
MCM93425DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM93425FM, DM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

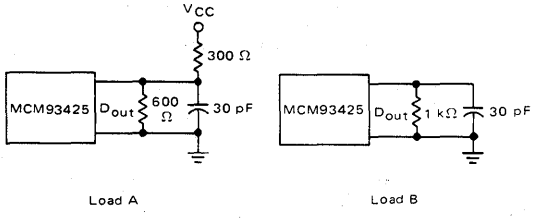
Symbol	Characteristic		Limits Min	Max	Units	Conditions	
V_{OL}	Output Low Voltage			0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA	
V_{IH}	Input High Voltage		2.1		Vdc	Guaranteed Input High Voltage for all Inputs	
V_{IL}	Input Low Voltage			0.8	Vdc	Guaranteed Input Low Voltage for all Inputs	
I_{IL}	Input Low Current			−400	μAdc	V_{CC} = Max, V_{in} = 0.4 V	
I_{IH}	Input High Current			40	μAdc	V_{CC} = Max, V_{in} = 4.5 V	
				1.0	mAdc	V_{CC} = Max, V_{in} = 5.25 V	
I_{off}	Output Current (High Z)			50	μAdc	V_{CC} = Max, V_{out} = 2.4 V	
				−50		V_{CC} = Max, V_{out} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground			−100	mAdc	V_{CC} = Max	
V_{OH}	Output High Voltage	MCM93425DC, PC	2.4		Vdc	I_{OH} = −10.3 mA, V_{CC} = 5.0 V ± 5%	
		MCM93425FM, DM	2.4		Vdc	I_{OH} = −5.2 mA	
V_{CD}	Input Diode Clamp Voltage			−1.5	Vdc	V_{CC} = Max, I_{in} = −10 mA	
I_{CC}	Power Supply Current			130	mAdc	T_A = Max	V_{CC} = Max, All Inputs Grounded
				155	mAdc	T_A = 0°C	
				170	mAdc	T_A = Min	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

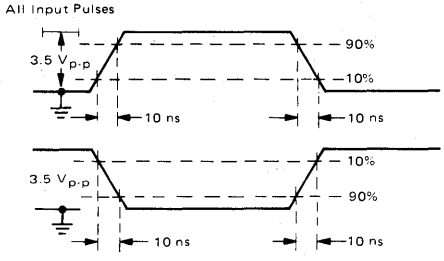
AC TEST LOAD AND WAVEFORMS

Loading Conditions



Load A Load B

Input Pulses



Symbol	Characteristic (Notes 2, 4)	MCM93425DC, PC Min	MCM93425DC, PC Max	MCM93425DM, FM Min	MCM93425DM, FM Max	Units	Conditions
READ MODE	DELAY TIMES					ns	
t_{ACS}	Chip Select Time		35		45		See Test Circuit
t_{ZRCS}	Chip Select to High Z		35		50		and Waveforms
t_{AA}	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
t_{ZWS}	Write Disable to High Z		35		45		See Test Circuit
t_{WR}	Write Recovery Time		40		50		and Waveforms
	INPUT TIMING REQUIREMENTS					ns	
t_W	Write Pulse Width (to guarantee write)	30		40			See Test Circuit
t_{WSD}	Data Setup Time Prior to Write	5		5			and Waveforms
t_{WHD}	Data Hold Time After Write	5		5			
t_{WSA}	Address Setup Time (at t_W = Min)	10		15			
t_{WHA}	Address Hold Time	10		10			
t_{WSCS}	Chip Select Setup Time	5		5			
t_{WHCS}	Chip Select Hold Time	5		5			

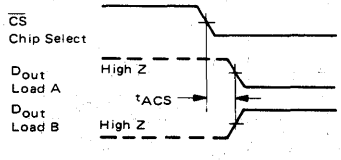
NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola Sales Representative if extended temperature or modified operating conditions are desired.

NOTE 3: Output short circuit conditions must not exceed 1 second duration.

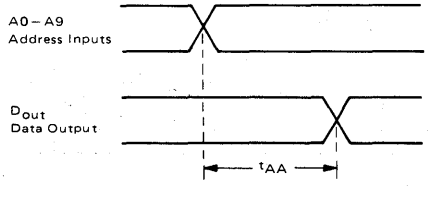
NOTE 4: The maximum address access time is guaranteed to be the worst case bit in the memory.

READ OPERATION TIMING DIAGRAM

Propagation Delay from Chip Select

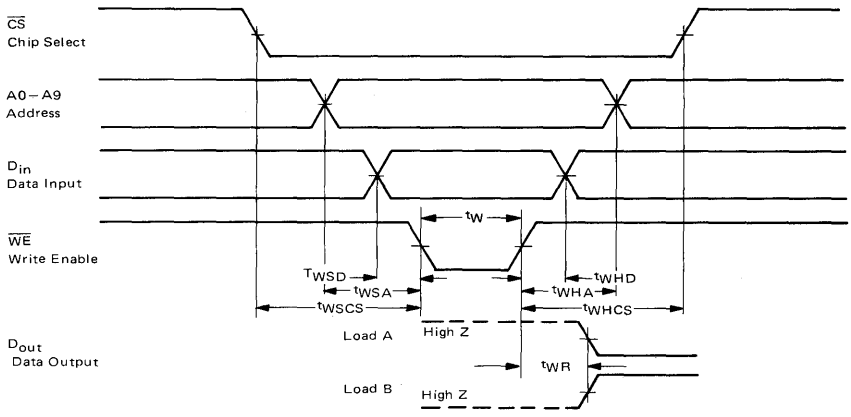


Propagation Delay from Address Inut



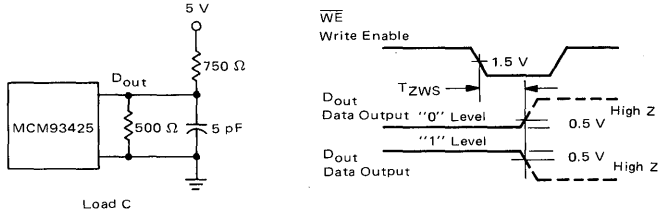
(All time measurements referenced to 1.5 V)

WRITE CYCLE TIMING

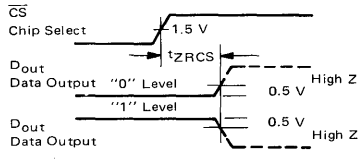


(All above measurements reference to 1.5 V)

WRITE ENABLE TO HIGH Z DELAY



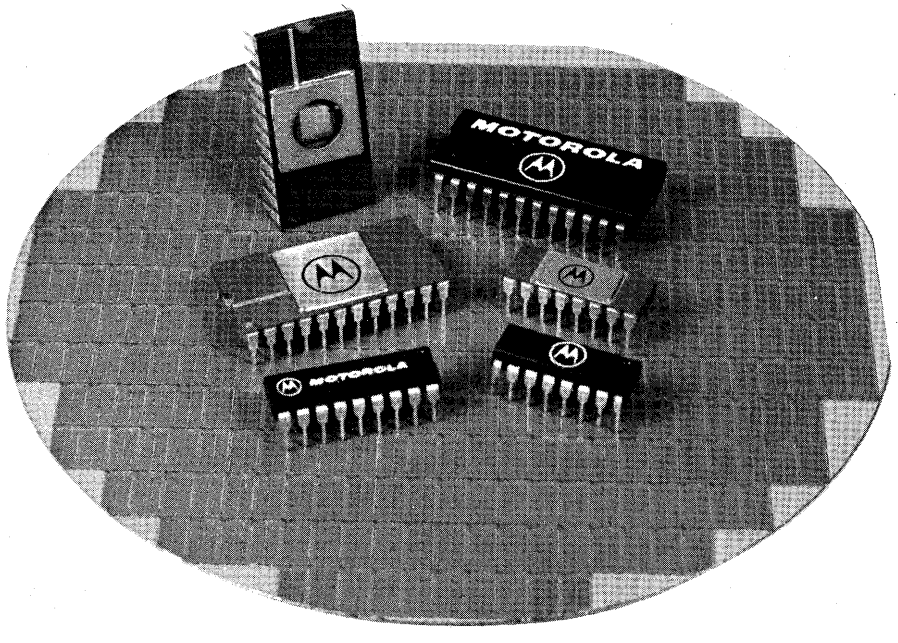
Propagation Delay from Chip Select to High Z



(All t_{ZXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C)

Package	θ_{JA} (Junction to Ambient) Blown	θ_{JA} (Junction to Ambient) Still	θ_{JC} (Junction to Case)
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W
P Suffix	65°C/W	100°C/W	25°C/W

TTL PROMs



MOTOROLA

MCM7621
MCM7621A

TTL

2048-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7621,A — 512 × 4 THREE-STATE

TTL PROM

2048-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7621 and MCM7621A, together with various other 76xx series TTL PROMS, have common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available with three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

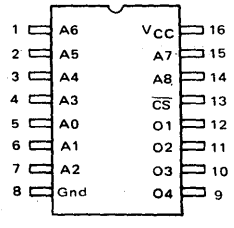
All pinouts are compatible to industry-standard PROMs and ROMs.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable — Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current — 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive — 16 mA Sink, 2.0 mA Source
- Fast Access Time — Guaranteed for Worst-Case N^2 Sequencing, Over Commercial Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

PIN ASSIGNMENT

MCM7621DC/ADC
MCM7621PC/APC



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Operating Output Voltage	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM7621xxx	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

GUARANTEED OPERATING RANGE (T_A = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	—	—	Vdc
Input Low Voltage	V_{IL}	—	—	0.8	Vdc

DC OPERATING CONDITIONS AND CHARACTERISTICS

Symbol	Parameter	Test Conditions	Three-State Output Min	Three-State Output Typ	Three-State Output Max	Unit
I_{IH}	Address/Enable "1"	$V_{IH} = V_{CC}$ Max	—	—	40	μAdc
I_{IL}	Input Current "0"	V_{IL} = 0.45 V	—	-0.1	-0.25	mAdc
V_{OH}	Output Voltage "1"	I_{OH} = -2.0 mA, V_{CC} Min	2.4	3.4	—	Vdc
V_{OL}	"0"	I_{OL} = +16 mA, V_{CC} Min	—	0.35	0.45	Vdc
I_{OHE}	Output Disabled "1"	V_{OH} = +5.25 V, V_{CC} Max	—	—	40	μAdc
I_{OLE}	Current "0"	V_{OL} = +0.3 V, V_{CC} Max	—	—	-40	μAdc
V_{IK}	Input Clamp Voltage	I_{in} = -18 mA	—	—	-1.2	Vdc
I_{OS}	Output Short Circuit Current	V_{CC} Max, V_{out} = 0.0 V One Output Only for 1.0 s Max	-15	—	-70	mAdc
I_{CC}	Power Supply Current	V_{CC} Max All Inputs Grounded	—	60	100	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

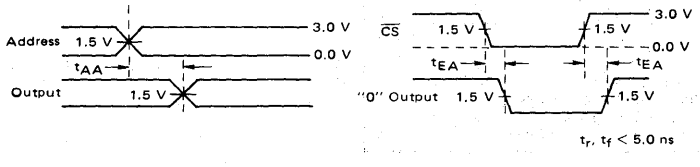
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

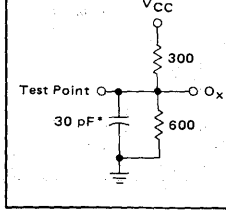
		MCM7621 0 to +75°C		MCM7621A 0 to +75°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	60	ns
Chip Enable Access Time	t_{EA}	15	25	15	25	ns

NOTE: AC limits guaranteed for worst case N^2 sequential with maximum test frequency of 5.0 MHz.

TIMING DIAGRAM



AC TEST LOAD



*Includes Scope and Test Fixture Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

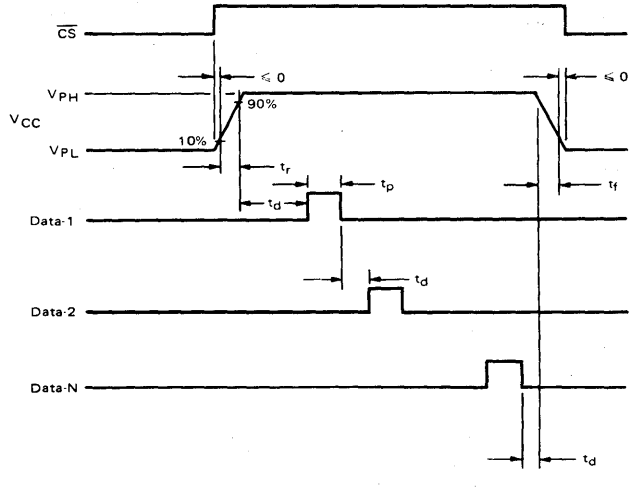
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input high (V_{IH}) to the $\overline{CS}$ input. $\overline{CS}$ input must remain at V_{IH} for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occured.

TABLE 1 — PROGRAMMING SPECIFICATIONS

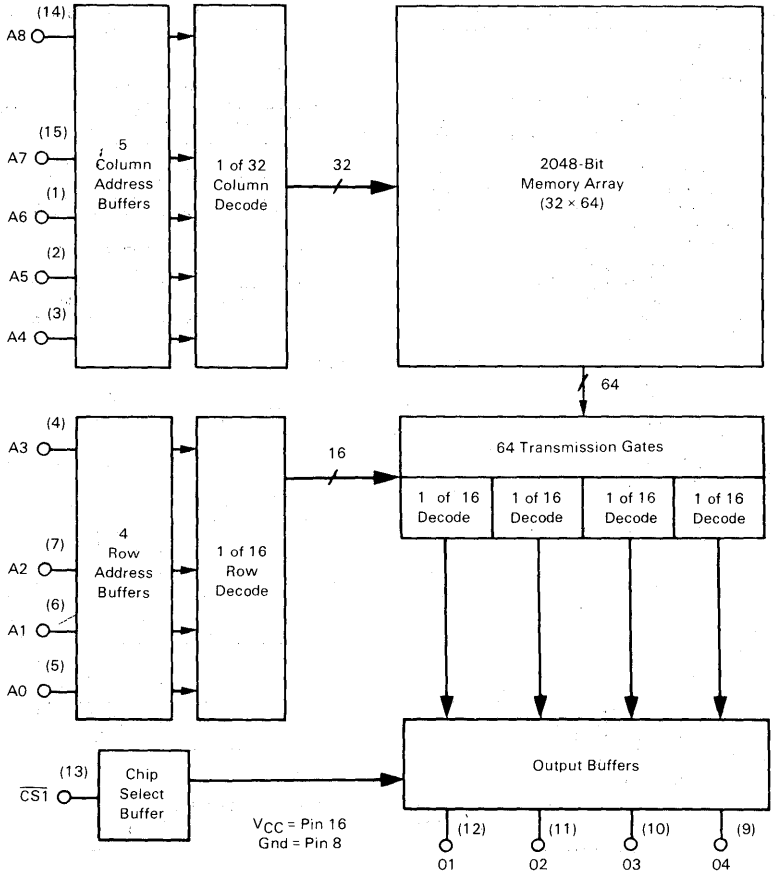
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} V_{PL}	Programming/Verify Voltage to V_{CC}	11.75 4.5	12.0 4.5	12.25 5.5	V V
I_{CCP}	Programming Voltage Current Limit with V_{PH} Applied	600	600	650	mA
t_r t_f	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μs μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width	100	—	1000	μs
DC	Programming Duty Cycle	—	50	90	%
 V_{OPE} V_{OPD}	Output Voltage Enable Disable (2)	 10.0 4.5	 10.5 5.0	 11.0 5.5	 V V
I_{OPE}	Output Voltage Enable Current	2.0	4.0	10	mA
T_A	Ambient Temperature	—	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 — TYPICAL PROGRAMMING WAVEFORMS



MCM7621/21A BLOCK DIAGRAM



MOTOROLA

MCM7641
MCM7641A

TTL PROM

TTL

4096-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7641,A — 512 × 8 THREE-STATE

4096-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7641 and MCM7641A, together with various other 76xx series TTL PROMS, comprise a complete and compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

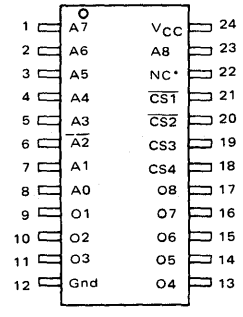
All pinouts are compatible to industry-standard PROMs and ROMs.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable — Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current — 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive — 16 mA Sink, 2.0 mA Source
- Fast Access Time — Guaranteed for Worst-Case N^2 Sequencing, Over Commercial Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

PIN ASSIGNMENT

MCM7641DC/ADC
MCM7641PC/APC



*No Connection

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Operating Output Voltage	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM7641xxx	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

GUARANTEED OPERATING RANGE (T_A = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	—	—	Vdc
Input Low Voltage	V_{IL}	—	—	0.8	Vdc

DC OPERATING CONDITIONS AND CHARACTERISTICS Three-State Output

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
I_{IH}	Address/Enable	"1"	$V_{IH} = V_{CC}$ Max	—	—	40	μAdc
I_{IL}	Input Current	"0"	V_{IL} = 0.45 V	—	-0.1	-0.25	mAdc
V_{OH}	Output Voltage	"1"	I_{OH} = -2.0 mA, V_{CC} Min	2.4	3.4	—	Vdc
V_{OL}		"0"	I_{OL} = +16 mA, V_{CC} Min	—	0.35	0.45	Vdc
I_{OHE}	Output Disabled	"1"	V_{OH} = +5.25 V, V_{CC} Max	—	—	40	μAdc
I_{OLE}	Current	"0"	V_{OL} = +0.3 V, V_{CC} Max	—	—	-40	μAdc
V_{IK}	Input Clamp Voltage		I_{in} = -18 mA	—	—	-1.2	Vdc
I_{OS}	Output Short Circuit Current		V_{CC} Max, V_{out} = 0.0 V One Output Only for 1.0 s Max	-15	—	-70	mAdc
I_{CC}	Power Supply Current		V_{CC} Max All Inputs Grounded	—	60	140	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

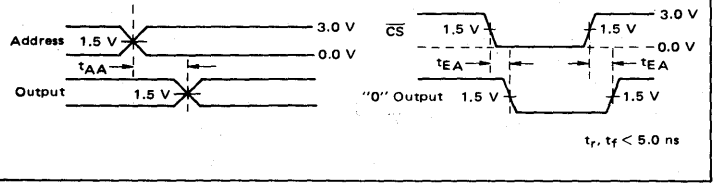
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

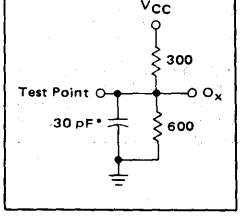
		MCM7641		MCM7641A		
		0 to +75°C		0 to +75°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	60	ns
Chip Enable Access Time	t_{EA}	30	40	30	40	ns

NOTE: AC limits guaranteed for worst case N^2 sequential with maximum test frequency of 5.0 MHz.

TIMING DIAGRAM



AC TEST LOAD



*Includes Scope and Test Fixture Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

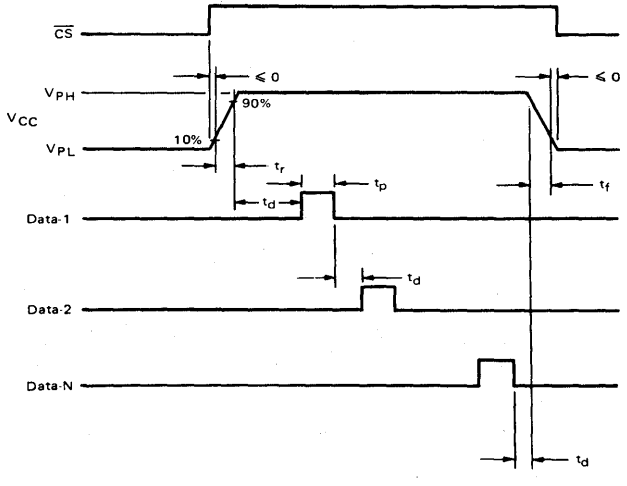
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input high (V_{IH}) to the $\overline{CS}$ input. $\overline{CS}$ input must remain at V_{IH} for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occured.

TABLE 1 — PROGRAMMING SPECIFICATIONS

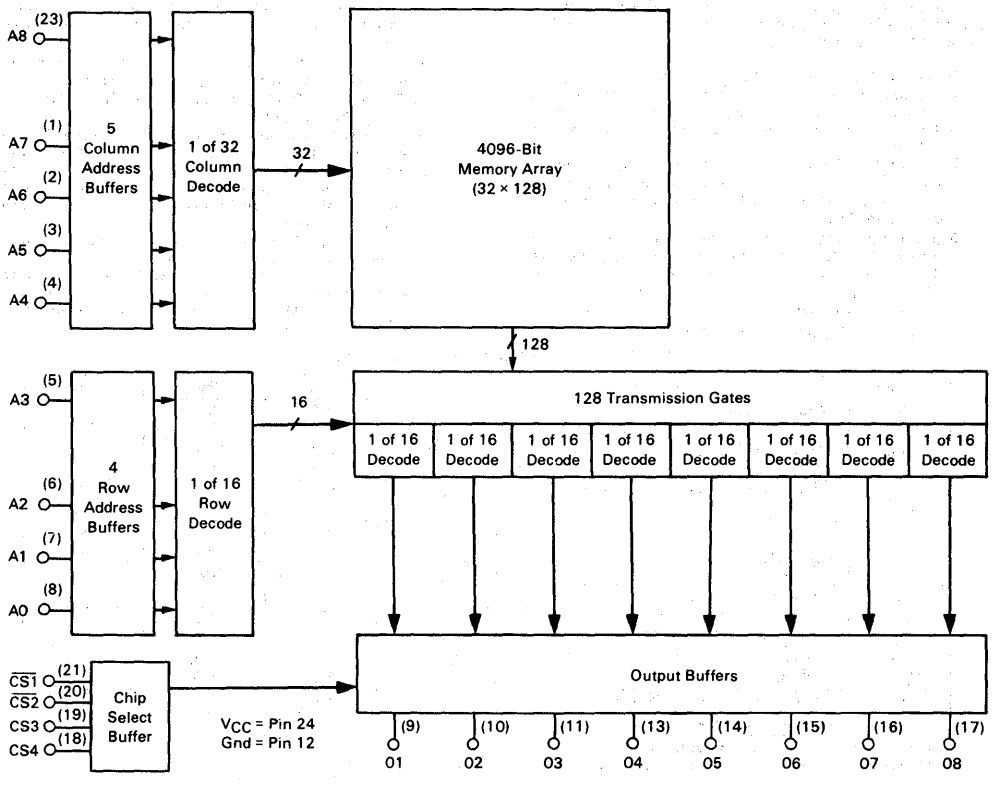
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} V_{PL}	Programming/Verify Voltage to V_{CC}	11.75 4.5	12.0 4.5	12.25 5.5	V V
I_{CCP}	Programming Voltage Current Limit with V_{PH} Applied	600	600	650	mA
t_r t_f	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μs μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width	100	—	1000	μs
DC	Programming Duty Cycle	—	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable Disable (2)	10.0 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	2.0	4.0	10	mA
T_A	Ambient Temperature	—	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 — TYPICAL PROGRAMMING WAVEFORMS



MCM7641/41A BLOCK DIAGRAM



MOTOROLA

MCM7643
MCM7643A

TTL

4096-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7643,A — 1024 × 4 THREE-STATE

4096-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7643 and MCM7643A, together with various other 76xx series TTL PROMS, comprise a complete and compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

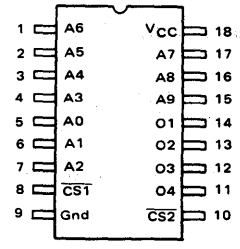
All pinouts are compatible to industry-standard PROMs and ROMs.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable — Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current — 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive — 16 mA Sink, 2.0 mA Source
- Fast Access Time — Guaranteed for Worst-Case N^2 Sequencing, Over Commercial Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

PIN ASSIGNMENT

MCM7643DC/ADC
MCM7643PC/APC



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Operating Output Voltage	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM7643xxx	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

GUARANTEED OPERATING RANGE (T_A = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	—	—	Vdc
Input Low Voltage	V_{IL}	—	—	0.8	Vdc

DC OPERATING CONDITIONS AND CHARACTERISTICS

Symbol	Parameter		Test Conditions	Three-State Output Min	Typ	Max	Unit
I_{IH}	Address/Enable	"1"	V_{IH} = V_{CC} Max	—	—	40	μAdc
I_{IL}	Input Current	"0"	V_{IL} = 0.45 V	—	-0.1	-0.25	mAdc
V_{OH}	Output Voltage	"1"	I_{OH} = -2.0 mA, V_{CC} Min	2.4	3.4	—	Vdc
V_{OL}		"0"	I_{OL} = +16 mA, V_{CC} Min	—	0.35	0.45	Vdc
I_{OHE}	Output Disabled	"1"	V_{OH} = +5.25 V, V_{CC} Max	—	—	40	μAdc
I_{OLE}	Current	"0"	V_{OL} = +0.3 V, V_{CC} Max	—	—	-40	μAdc
V_{IK}	Input Clamp Voltage		I_{in} = -18 mA	—	—	-1.2	Vdc
I_{OS}	Output Short Circuit Current		V_{CC} Max, V_{out} = 0.0 V One Output Only for 1.0 s Max	-15	—	-70	mAdc
I_{CC}	Power Supply Current		V_{CC} Max All Inputs Grounded	—	100	140	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

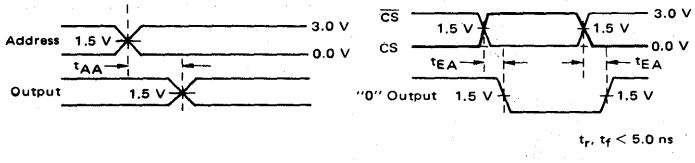
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

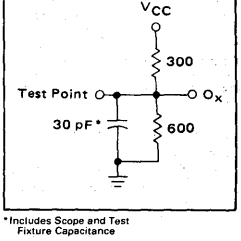
		MCM7643 0 to +75°C		MCM7643A 0 to +75°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	50	70	40	50	ns
Chip Enable Access Time	t_{EA}	25	30	25	30	ns

NOTE: AC limits guaranteed for worst case N^2 sequential with maximum test frequency of 5.0 MHz.

TIMING DIAGRAM



AC TEST LOAD



*Includes Scope and Test Fixture Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

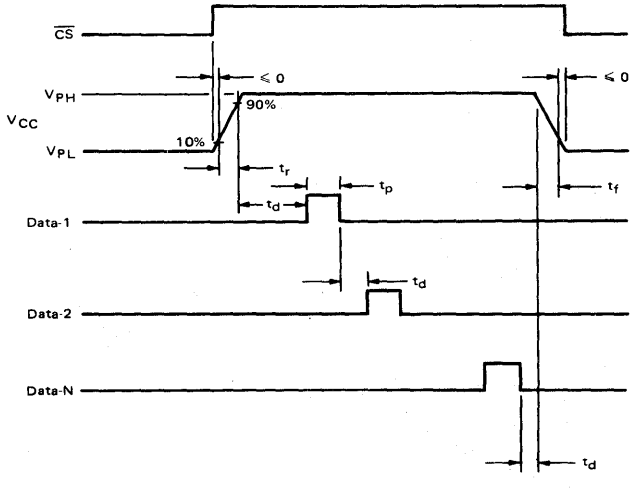
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input high (V_{IH}) to the $\overline{CS}$ input. $\overline{CS}$ input must remain at V_{IH} for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occured.

TABLE 1 — PROGRAMMING SPECIFICATIONS

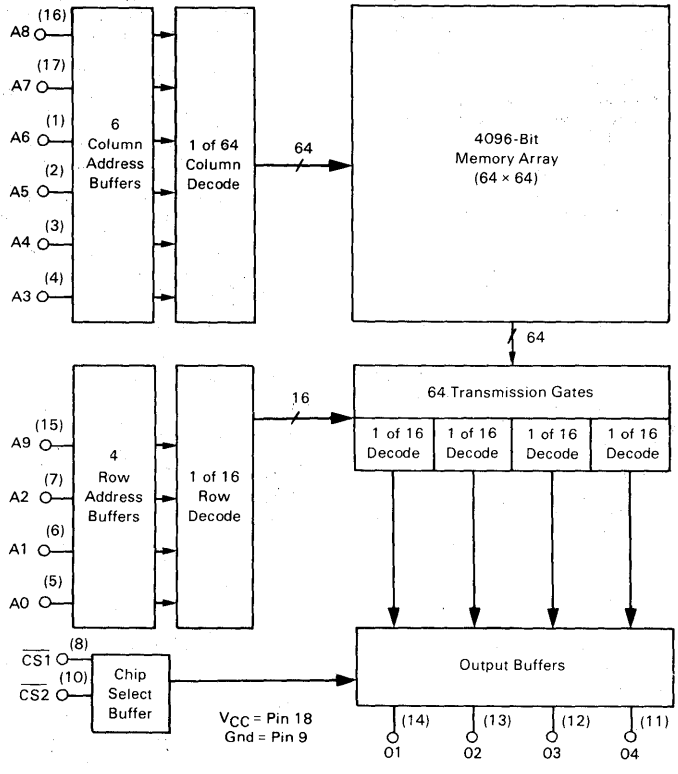
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} V_{PL}	Programming/Verify Voltage to V_{CC}	11.75 4.5	12.0 4.5	12.25 5.5	V V
I_{CCP}	Programming Voltage Current Limit with V_{PH} Applied	600	600	650	mA
t_r t_f	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μs μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width	100	—	1000	μs
DC	Programming Duty Cycle	—	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable Disable (2)	10.0 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	2.0	4.0	10	mA
T_A	Ambient Temperature	—	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS



MCM7643/43A BLOCK DIAGRAM



MOTOROLA

MCM7649
MCM7649A

TTL

4096-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7649, A — 512 × 8 THREE-STATE

4096-BIT PROGRAMMABLE READ ONLY MEMORY

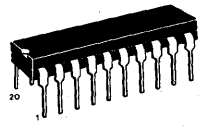
The MCM7649 and MCM7649A, together with various other 76xx series TTL PROMs, comprise a complete and compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with three-state outputs. All bits are manufactured storing a Logic "1" (outputs high), and can be selectively programmed for Logic "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

All pinouts are compatible to industry-standard PROMs and ROMs.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

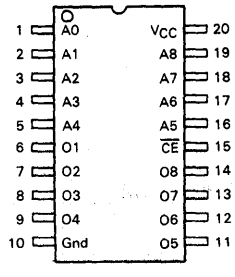
- Common DC Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable — Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current — 250 μA Logic "0", 25 μA Logic "1"
  Full Output Drive — 16 mA Sink, 2.0 mA Source
- Pin-Compatible with Industry-Standard PROMs and ROMs
- Fast Access Time — Guaranteed for Worst-Case N^2 Sequencing, Over Commercial Temperature and Voltage Ranges
  MCM7649 60 ns Maximum
  MCM7649A 45 ns Maximum



P SUFFIX
PLASTIC PACKAGE
CASE 738-02

PIN ASSIGNMENT

MCM7649PC/APC



PIN DESIGNATION

A0-A8	Address Inputs
O1-O8	Data Outputs
$\overline{CE}$	Chip Enable

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Operating Output Voltage	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM7649xxx	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

GUARANTEED OPERATING RANGE (T_A = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	—	—	Vdc
Input Low Voltage	V_{IL}	—	—	0.8	Vdc

DC OPERATING CONDITIONS AND CHARACTERISTICS Three-State Output

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
I_{IH}	Address/Enable	"1"	V_{IH} = V_{CC} Max	—	—	25	μAdc
I_{IL}	Input Current	"0"	V_{IL} = 0.45 V	—	-0.1	-0.25	mAdc
V_{OH}	Output Voltage	"1"	I_{OH} = -2.0 mA, V_{CC} Min	2.4	3.4	—	Vdc
V_{OL}		"0"	I_{OL} = +16 mA, V_{CC} Min	—	0.35	0.50	Vdc
I_{OHE}	Output Disabled	"1"	V_{OH} = +5.25 V, V_{CC} Max	—	—	40	μAdc
I_{OLE}	Current	"0"	V_{OL} = +0.3 V, V_{CC} Max	—	—	-40	μAdc
V_{IK}	Input Clamp Voltage		I_{in} = -18 mA	—	—	-1.2	Vdc
I_{OS}	Output Short Circuit Current		V_{CC} Max, V_{out} = 0.0 V One Output Only for 1.0 s Max	-20	—	-100	mAdc
I_{CC}	Power Supply Current		V_{CC} Max All Inputs Grounded	—	120	170	mAdc

CAPACITANCE (T_A = 25°C, periodically sampled rather than 100% tested.)

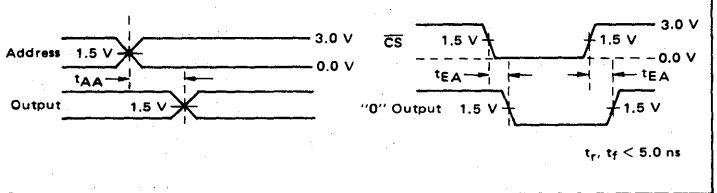
Parameter	Test Conditions	Symbol	Typ	Unit
Input Capacitance	V_{CC} = 5.0 V, V_{in} = 2.0 V, f = 1.0 MHz	C_{in}	8.0	pF
Output Capacitance	V_{CC} = 5.0 V, V_{in} = 2.0 V, f = 1.0 MHz	C_{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

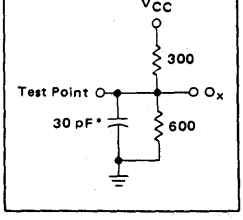
		MCM7649		MCM7649A		
		0 to +75°C		0 to +75°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	40	60	35	45	ns
Chip Enable Access Time	t_{EA}	30	40	25	35	ns

NOTE: AC limits guaranteed for worst case N^2 sequential with maximum test frequency of 5.0 MHz.

TIMING DIAGRAM



AC TEST LOAD



*Includes Scope and Test Fixture Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

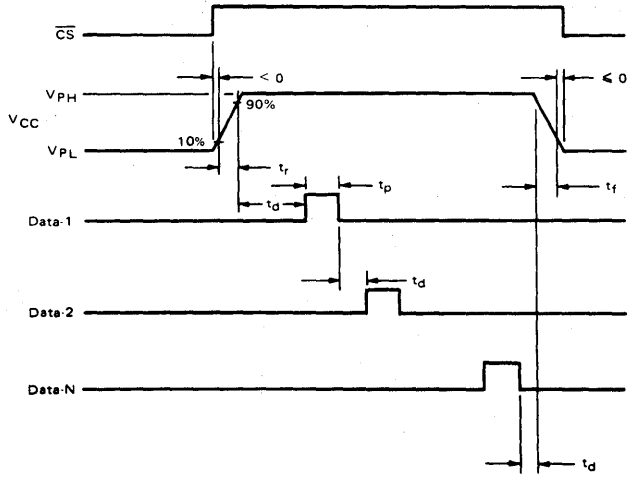
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input high (V_{IH}) to the $\overline{CS}$ input. $\overline{CS}$ input must remain at V_{IH} for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a Logic "0" (V_{IL}) to the $\overline{CS}$ input.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

TABLE 1 — PROGRAMMING SPECIFICATIONS

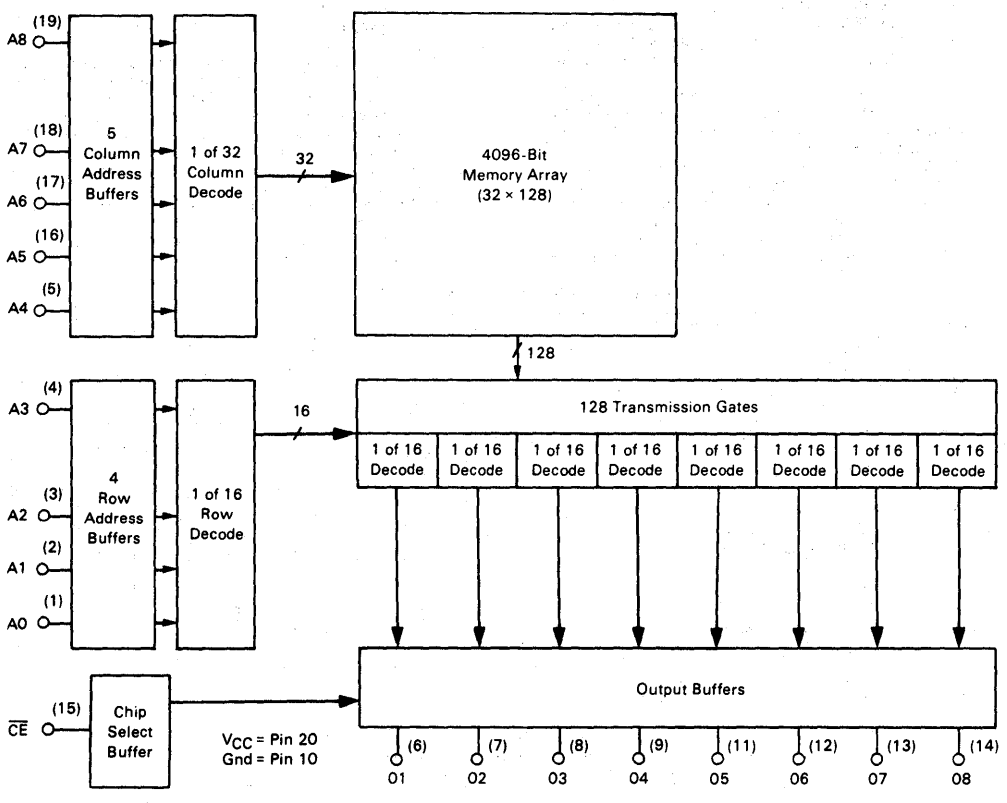
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} V_{PL}	Programming/Verify Voltage to V_{CC}	11.75 4.5	12.0 4.5	12.25 5.5	V V
I_{CCP}	Programming Voltage Current Limit with V_{PH} Applied	600	600	650	mA
t_r t_f	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μs μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width	100	—	1000	μs
DC	Programming Duty Cycle	—	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable Disable (2)	10.0 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	2.0	4.0	10	mA
T_A	Ambient Temperature	—	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 — TYPICAL PROGRAMMING WAVEFORMS



MCM7649/49A BLOCK DIAGRAM



MOTOROLA

MCM7681
MCM7681A

TTL

8192-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7681,A — 1024 × 8 THREE-STATE

TTL PROM

8192-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7681 and MCM7681A, together with various other 76xx series TTL PROMS, comprise a complete and compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

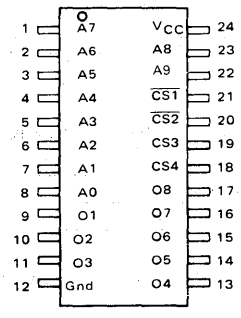
Pinouts are compatible to industry-standard PROMs and ROMs. In addition, the MCM7681 is a pin compatible replacement for the 512 × 8 with Pin 22 connected as A9 on the 1024 × 8.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable — Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current — 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive — 16 mA Sink, 2.0 mA Source
- Fast Access Time — Guaranteed for Worst-Case N^2 Sequencing, Over Commercial Temperature Ranges and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

PIN ASSIGNMENT

MCM7681DC/ADC
MCM7681PC/APC



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Operating Output Voltage	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM7681xxx	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

GUARANTEED OPERATING RANGE (T_A = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	—	—	Vdc
Input Low Voltage	V_{IL}	—	—	0.8	Vdc

DC OPERATING CONDITIONS AND CHARACTERISTICS

Symbol	Parameter		Test Conditions	Three-State Output Min	Typ	Max	Unit
I_{IH}	Address/Enable	"1"	$V_{IH} = V_{CC}$ Max	—	—	40	μAdc
I_{IL}	Input Current	"0"	V_{IL} = 0.45 V	—	-0.1	-0.25	mAdc
V_{OH}	Output Voltage	"1"	I_{OH} = -2.0 mA, V_{CC} Min	2.4	3.4	—	Vdc
V_{OL}		"0"	I_{OL} = +16 mA, V_{CC} Min	—	0.35	0.45	Vdc
I_{OHE}	Output Disabled	"1"	V_{OH} = +5.25 V, V_{CC} Max	—	—	40	μAdc
I_{OLE}	Current	"0"	V_{OL} = +0.3 V, V_{CC} Max	—	—	-40	μAdc
V_{IK}	Input Clamp Voltage		I_{in} = -18 mA	—	—	-1.2	Vdc
I_{OS}	Output Short Circuit Current		V_{CC} Max, V_{out} = 0.0 V One Output Only for 1.0 s Max	-15	—	-70	mAdc
I_{CC}	Power Supply Current		V_{CC} Max All Inputs Grounded	—	110	150	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

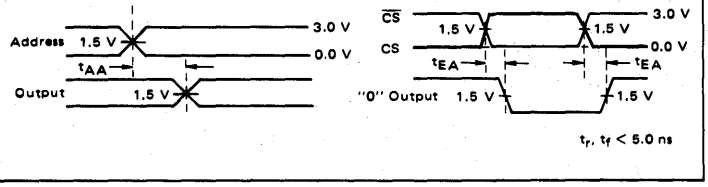
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

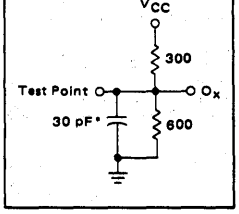
		MCM7681 0 to +75°C		MCM7681A 0 to +75°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	—	70	—	50	ns
Chip Enable Access Time	t_{EA}	30	40	30	40	ns

NOTE: AC limits guaranteed for worst case N^2 sequential with maximum test frequency of 5.0 MHz.

TIMING DIAGRAM



AC TEST LOAD



*Includes Scope and Test Fixture Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

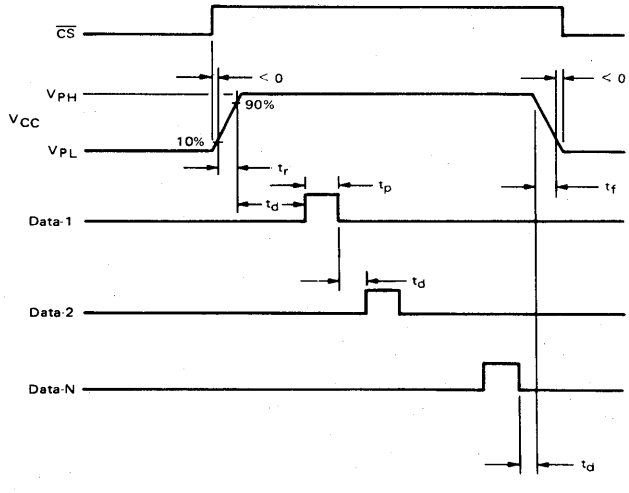
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input high (V_{IH}) to the $\overline{CS}$ input. $\overline{CS}$ input must remain at V_{IH} for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occured.

TABLE 1 — PROGRAMMING SPECIFICATIONS

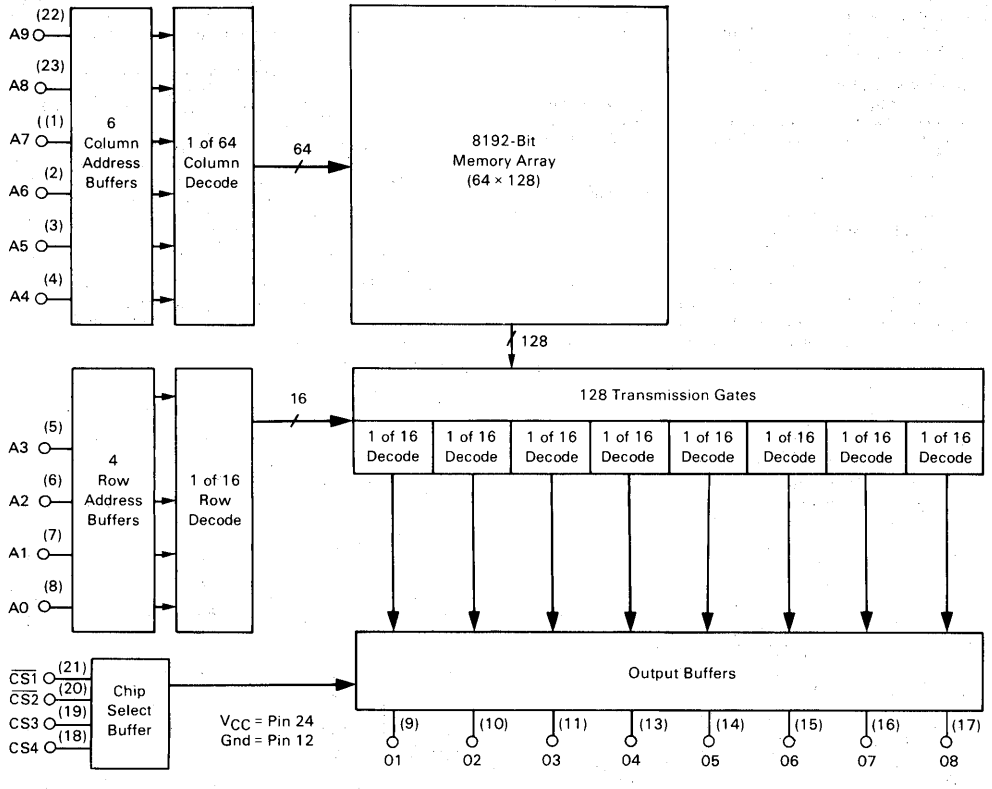
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} V_{PL}	Programming/Verify Voltage to V_{CC}	11.75 4.5	12.0 4.5	12.25 5.5	V V
I_{CCP}	Programming Voltage Current Limit with V_{PH} Applied	600	600	650	mA
t_r t_f	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μs μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width	100	—	1000	μs
DC	Programming Duty Cycle	—	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable Disable (2)	10.0 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	2.0	4.0	10	mA
T_A	Ambient Temperature	—	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 — TYPICAL PROGRAMMING WAVEFORMS



MCM7681/81A BLOCK DIAGRAM



MOTOROLA

MCM7685
MCM7685A

TTL

8192-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7685,A — 2048 × 4 THREE-STATE

TTL PROM

8192-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7685 and MCM7685A, together with various other 76xx series TTL PROMS, comprise a complete and compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable PROMs and are available in commonly used organizations, with three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

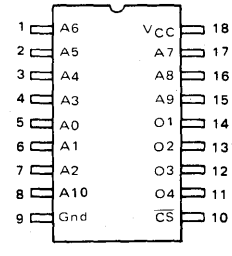
Pinouts are compatible to industry-standard PROMs and ROMs. The MCM7685 is a pin compatible replacement for the 1024 × 4 organization with Pin 8 connected as A10 on the 2048 × 4.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable — Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current -- 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive — 16 mA Sink, 2.0 mA Source
- Fast Access Time — Guaranteed for Worst-Case N^2 Sequencing, Commercial Temperature Ranges and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

PIN ASSIGNMENT

MCM7685DC/ADC
MCM7685PC/APC



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Operating Output Voltage	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM7685xxx	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

GUARANTEED OPERATING RANGE (T_A = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	—	—	Vdc
Input Low Voltage	V_{IL}	—	—	0.8	Vdc

DC OPERATING CONDITIONS AND CHARACTERISTICS

Symbol	Parameter		Test Conditions	Three-State Output Min	Typ	Max	Unit
I_{IH}	Address/Enable	"1"	V_{IH} = V_{CC} Max	—	—	40	μAdc
I_{IL}	Input Current	"0"	V_{IL} = 0.45 V	—	-0.1	-0.25	mAdc
V_{OH}	Output Voltage	"1"	I_{OH} = -2.0 mA, V_{CC} Min	2.4	3.4	—	Vdc
V_{OL}		"0"	I_{OL} = +16 mA, V_{CC} Min	—	0.35	0.45	Vdc
I_{OHE}	Output Disabled	"1"	V_{OH} = +5.25 V, V_{CC} Max	—	—	40	μAdc
I_{OLE}	Current	"0"	V_{OL} = +0.3 V, V_{CC} Max	—	—	-40	μAdc
V_{IK}	Input Clamp Voltage		I_{in} = -18 mA	—	—	-1.2	Vdc
I_{OS}	Output Short Circuit Current		V_{CC} Max, V_{out} = 0.0 V One Output Only for 1.0 s Max	-15	—	-70	mAdc
I_{CC}	Power Supply Current		V_{CC} Max All Inputs Grounded	—	80	150	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

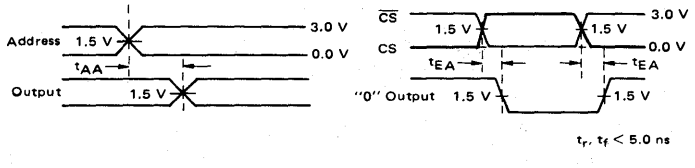
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

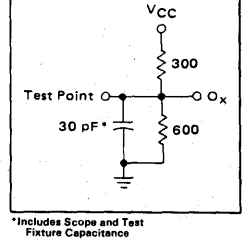
		MCM7685 0 to +75°C		MCM7685A 0 to +75°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	40	55	ns
Chip Enable Access Time	t_{EA}	30	40	30	40	ns

NOTE: AC limits guaranteed for worst case N^2 sequential with maximum test frequency of 5.0 MHz.

TIMING DIAGRAM



AC TEST LOAD



*Includes Scope and Test Fixture Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

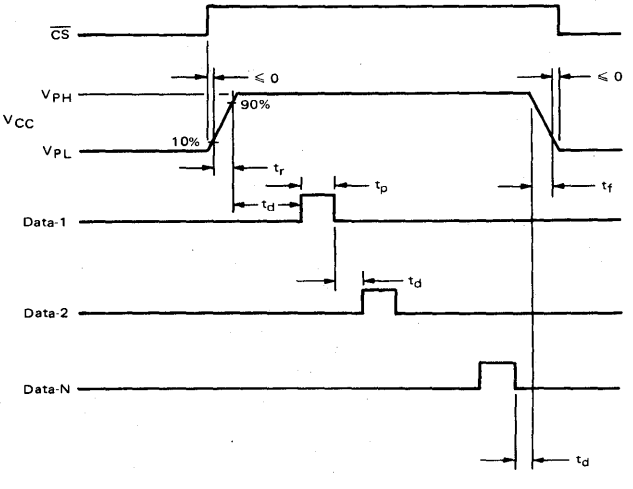
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input high (V_{IH}) to the $\overline{CS}$ input. $\overline{CS}$ input must remain at V_{IH} for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occured.

TABLE 1 — PROGRAMMING SPECIFICATIONS

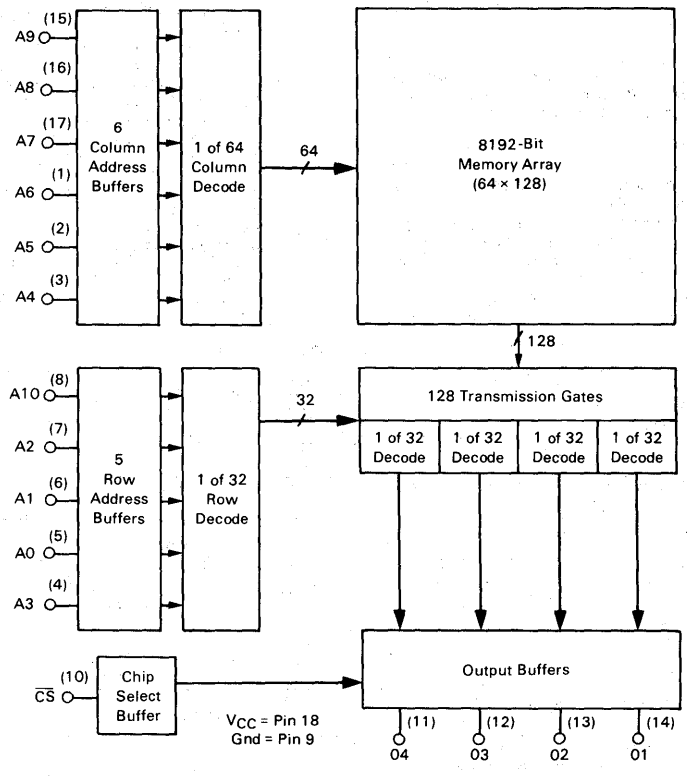
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} V_{PL}	Programming/Verify Voltage to V_{CC}	11.75 4.5	12.0 4.5	12.25 5.5	V V
I_{CCP}	Programming Voltage Current Limit with V_{PH} Applied	600	600	650	mA
t_r t_f	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μs μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width	100	—	1000	μs
DC	Programming Duty Cycle	—	50	90	%
 V_{OPE} V_{OPD}	Output Voltage Enable Disable (2)	 10.0 4.5	 10.5 5.0	 11.0 5.5	 V V
I_{OPE}	Output Voltage Enable Current	2.0	4.0	10	mA
T_A	Ambient Temperature	—	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 — TYPICAL PROGRAMMING WAVEFORMS



MCM7685/85A BLOCK DIAGRAM



MOTOROLA

MCM76161
MCM76161A

TTL

16384-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM76161,A — 2048 × 8 THREE-STATE

TTL PROM

16384-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM76161 and MC76161A, together with various other 76xx series TTL PROMS, comprise a complete and compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

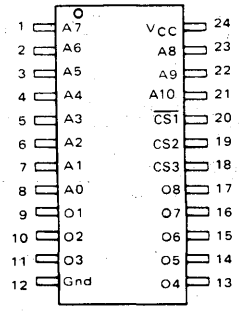
Pinouts are compatible to industry-standard PROMs and ROMs. The MCM76161 is a pin compatible replacement for the 1024 × 8 with Pin 21 connected as A10 on the 2048 × 8.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable — Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current — 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive — 16 mA Sink, 2.0 mA Source
- Fast Access Time — Guaranteed for Worst-Case N^2 Sequencing, Over Commercial Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

PIN ASSIGNMENT

MCM76161DC/ADC
MCM76161PC/APC



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Operating Output Voltage	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM76161xxx	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

GUARANTEED OPERATING RANGE (T_A = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	—	—	Vdc
Input Low Voltage	V_{IL}	—	—	0.8	Vdc

DC OPERATING CONDITIONS AND CHARACTERISTICS

Symbol	Parameter		Test Conditions	Three-State Output Min	Typ	Max	Unit
I_{IH} I_{IL}	Address/Enable Input Current	"1" "0"	$V_{IH} = V_{CC}$ Max V_{IL} = 0.45 V	— —	— -0.1	40 -0.25	μAdc mAdc
V_{OH} V_{OL}	Output Voltage	"1" "0"	I_{OH} = -2.0 mA, V_{CC} Min I_{OL} = +16 mA, V_{CC} Min	2.4 —	3.4 0.35	— 0.45	Vdc Vdc
I_{OHE} I_{OLE}	Output Disabled Current	"1" "0"	V_{OH} = +5.25 V, V_{CC} Max V_{OL} = +0.3 V, V_{CC} Max	— —	— —	40 -40	μAdc μAdc
V_{IK}	Input Clamp Voltage		I_{in} = -18 mA	—	—	-1.2	Vdc
I_{OS}	Output Short Circuit Current		V_{CC} Max, V_{out} = 0.0 V One Output Only for 1.0 s Max	-15	—	-70	mAdc
I_{CC}	Power Supply Current		V_{CC} Max All Inputs Grounded	—	130	180	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

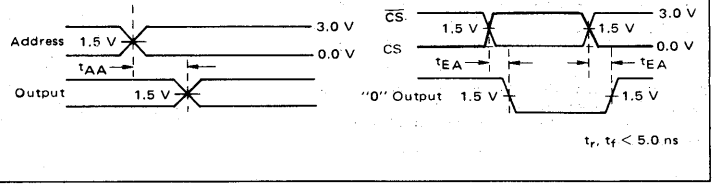
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

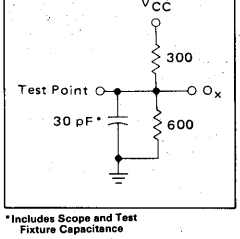
		MCM76161 0 to +75°C		MCM76161A 0 to +75°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	35	60	ns
Chip Enable Access Time	t_{EA}	30	40	30	40	ns

NOTE: AC limits guaranteed for worst case N^2 sequential with maximum test frequency of 5.0 MHz.

TIMING DIAGRAM



AC TEST LOAD



*Includes Scope and Test Fixture Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

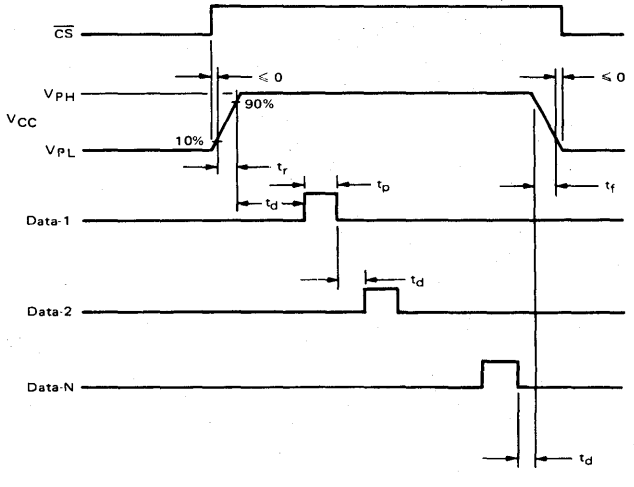
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input high (V_{IH}) to the $\overline{CS}$ input. $\overline{CS}$ input must remain at V_{IH} for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occured.

TABLE 1 — PROGRAMMING SPECIFICATIONS

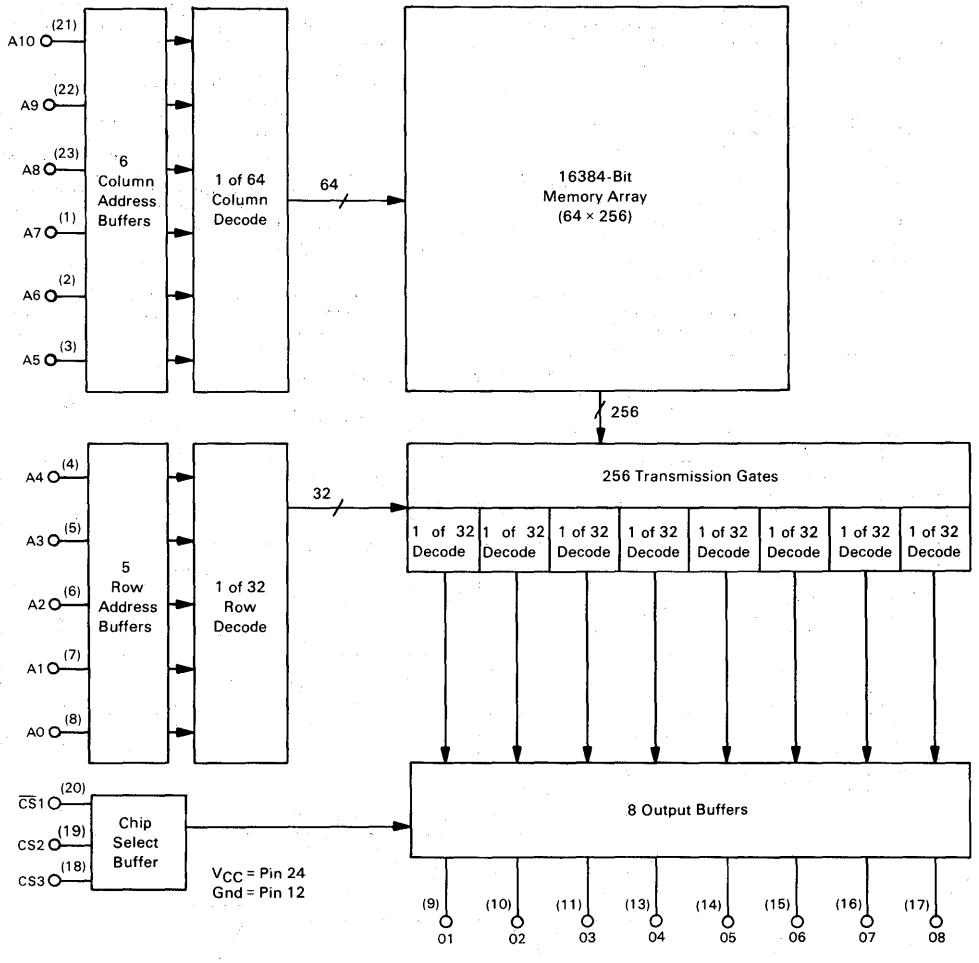
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} V_{PL}	Programming/Verify Voltage to V_{CC}	11.75 4.5	12.0 4.5	12.25 5.5	V V
I_{CCP}	Programming Voltage Current Limit with V_{PH} Applied	600	600	650	mA
t_r t_f	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μs μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width	100	—	1000	μs
DC	Programming Duty Cycle	—	50	90	%
 V_{OPE} V_{OPD}	Output Voltage Enable Disable (2)	 10.0 4.5	 10.5 5.0	 11.0 5.5	 V V
I_{OPE}	Output Voltage Enable Current	2.0	4.0	10	mA
T_A	Ambient Temperature	—	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 — TYPICAL PROGRAMMING WAVEFORMS



MCM76161/161A BLOCK DIAGRAM



MOTOROLA

MCM76165
MCM76165A

Advance Information

TTL

16384-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM76165,A — 4096 x 4
THREE-STATE OUTPUTS

TTL PROM

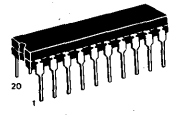
16384-BIT PROGRAMMABLE READ ONLY MEMORIES

The MCM76165 and MCM76165A, together with various other 76xx series TTL PROMs, comprise a complete and compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with three-state outputs. All bits are manufactured storing a Logical "1" (outputs high), and can be selectively programmed for Logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

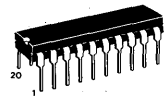
In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- 4096 Words x 4 Bits Organization
- TTL Compatible Inputs and Outputs
- Ultra Fast Read Access Time: 35 ns — MCM76165A
  50 ns — MCM76165
- Three-State Outputs
- Two Chip Select Inputs for Memory Expansion
- Proven Reliable NiCr Fuse Technology and Extra Test Words Insure High Programming Yields
- MOSAIC Oxide Isolate Technology Provides Optimum Speed-Power Characteristics
- Standard 20-Pin, 300 Mil Wide, Dual-In-Line Package

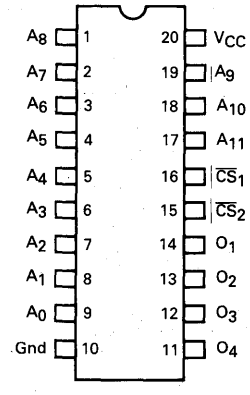


D SUFFIX
CERAMIC PACKAGE
CASE 732-03

P SUFFIX
PLASTIC PACKAGE
CASE 738-02



PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Operating Output Voltage	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	−20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM76165 xxx	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

ORDERING INFORMATION

Device	Package
MCM76165DC MCM76165ADC	Ceramic Dual-in-Line
MCM76165PC MCM76165APC	Plastic Dual-in-Line

MOSAIC is a trademark of Motorola Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

GUARANTEED OPERATING RANGE (T_A = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	—	—	Vdc
Input Low Voltage	V_{IL}	—	—	0.8	Vdc

DC OPERATING CONDITIONS AND CHARACTERISTICS

Symbol	Parameter		Test Conditions	Three-State Output Min	Three-State Output Typ	Three-State Output Max	Unit
I_{IH} I_{IL}	Address/Enable Input Current	"1" "0"	V_{IH} = V_{CC} Max V_{IL} = 0.45 V	— —	— −0.1	40 −0.25	μAdc mAdc
V_{OH} V_{OL}	Output Voltage	"1" "0"	I_{OH} = −2.0 mA, V_{CC} Min I_{OL} = +16 mA, V_{CC} Min	2.4 —	3.4 0.35	— 0.45	Vdc Vdc
I_{OHE} I_{OLE}	Output Disabled Current	"1" "0"	V_{OH} = +5.25 V, V_{CC} Max V_{OL} = +0.3 V, V_{CC} Max	— —	— —	40 −40	μAdc μAdc
V_{IK}	Input Clamp Voltage		I_{in} = −18 mA	—	—	−1.2	Vdc
I_{OS}	Output Short Circuit Current		V_{CC} Max, V_{out} = 0.0 V One Output Only for 1.0 s Max	−15	—	−70	mAdc
I_{CC}	Power Supply Current		V_{CC} Max All Inputs Grounded	—	110	165	mAdc

CAPACITANCE (T_A = 25°C, periodically sampled rather than 100% tested.)

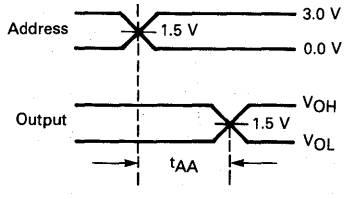
Parameter	Test Conditions	Symbol	Typ	Unit
Input Capacitance	V_{CC} = 5.0 V, V_{in} = 2.0 V, f = 1.0 MHz	C_{in}	8.0	pF
Output Capacitance	V_{CC} = 5.0 V, V_{out} = 2.0 V, f = 1.0 MHz	C_{out}	10	pF

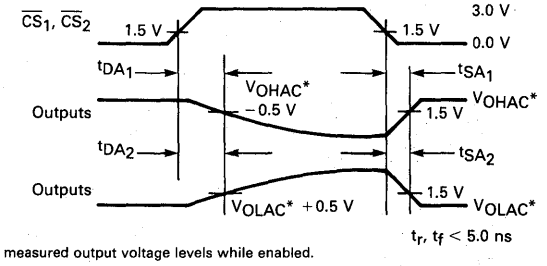
AC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature)

Characteristic	Symbol	MCM76165 0 to +75°C Typ	MCM76165 0 to +75°C Max	MCM76165A 0 to +75°C Typ	MCM76165A 0 to +75°C Max	Unit
Address to Output Access Time	t_{AA}	—	50	—	35	ns
Chip Select Access Time	t_{SA}	—	25	—	25	ns
Chip Disable Access Time	t_{DA}	—	25	—	25	ns

NOTE: AC limits guaranteed for worst case N^2 sequential with maximum test frequency of 5.0 MHz.

TIMING DIAGRAM

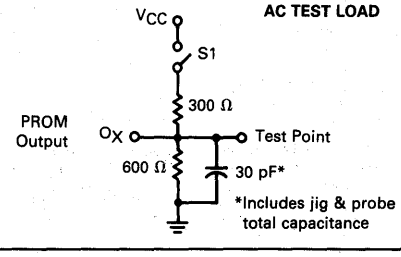




*V_{OLAC} and V_{OHAC} are the measured output voltage levels while enabled.

Symbol	Parameter	S1
t_{AA}	Address Access Time	Closed
t_{EA_1}	Chip Select Access Time from "Three State" to V_{OH}	Open
t_{EA_2}	Chip Select Access Time from "Three State" to V_{OL}	Closed
t_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
t_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

AC TEST LOAD



PROGRAMMING

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1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
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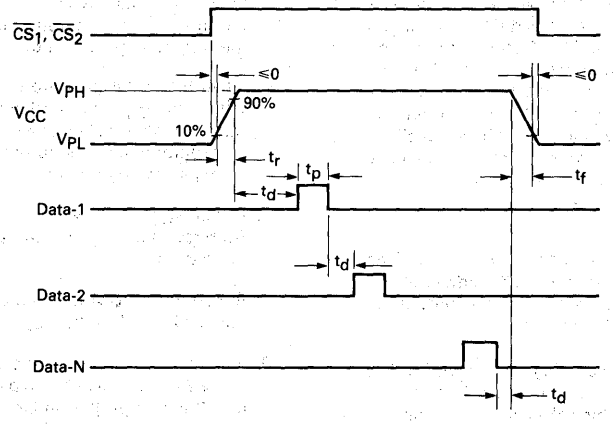
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a Logic "0" (V_{IL}) to the $\overline{CS}_X$ inputs.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

TABLE 1 — PROGRAMMING SPECIFICATIONS

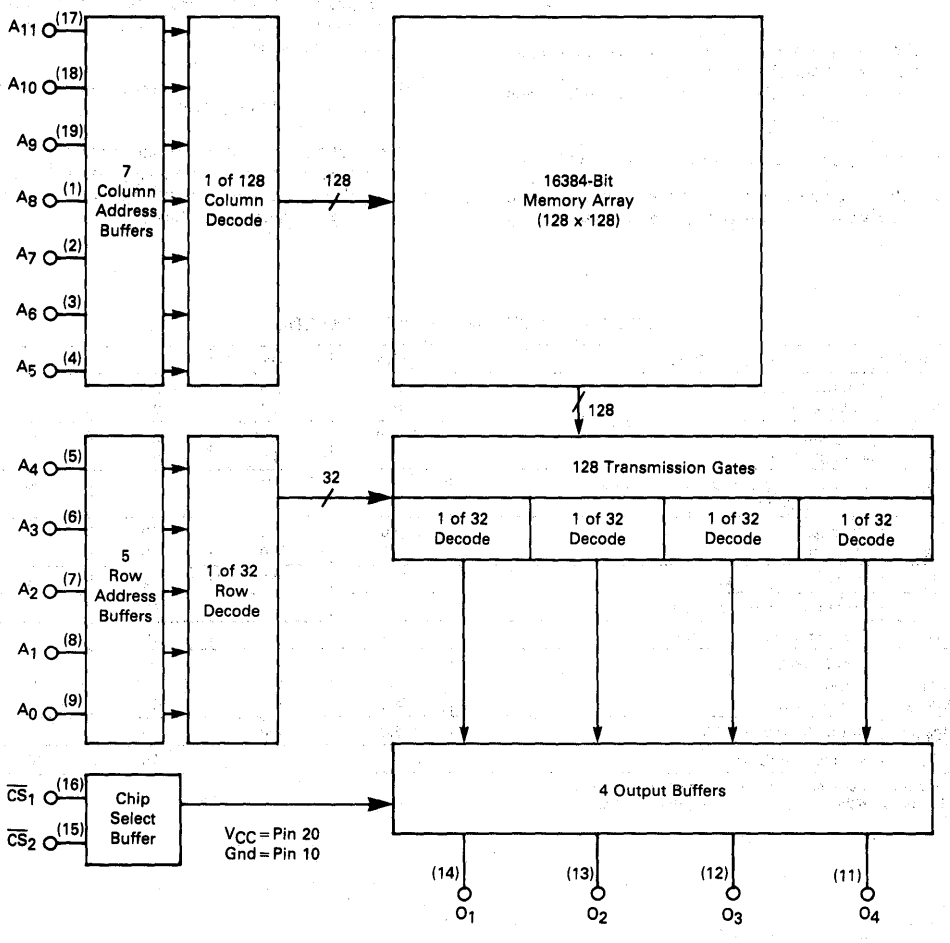
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH} V_{IL}	Address Input Voltage(1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} V_{PL}	Programming/Verify Voltage to V_{CC}	11.75 4.5	12.0 4.5	12.25 5.5	V V
I_{CCP}	Programming Voltage Current Limit with V_{PH} Applied	600	600	650	mA
t_r t_f	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μs μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width	100	—	1000	μs
DC	Programming Duty Cycle	—	50	90	%
 V_{OPE} V_{OPD}	Output Voltage Enable Disable(2)	 10.0 4.5	 10.5 5.0	 11.0 5.5	 V V
I_{OPE}	Output Voltage Enable Circuit	2.0	4.0	10	mA
T_A	Ambient Temperature	—	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

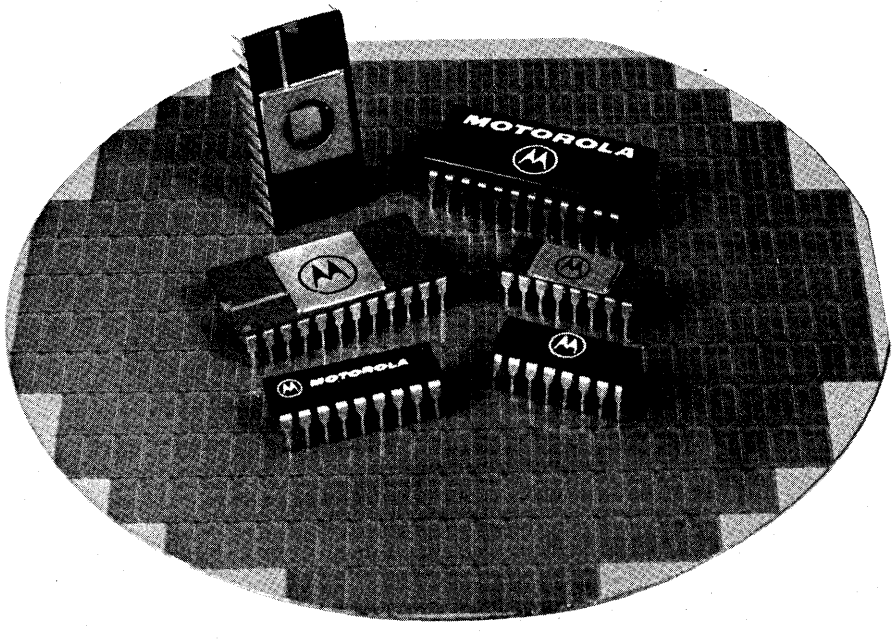
FIGURE 1 — TYPICAL PROGRAMMING WAVE FORMS



MCM76165/165A BLOCK DIAGRAM



MECL RAMs



MOTOROLA

MCM10143

MECL

8 x 2 MULTIPORT REGISTER FILE (RAM)

MECL RAM

8 x 2 MULTIPORT REGISTER FILE (RAM)

The MC10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.

WRITE

The word to be written is selected by addresses A_0–A_2. Each bit of the word has a separate write enable to allow more flexibility in system design. A write occurs on the positive transition of the clock. Data is enabled by having the write enables at a low level when the clock makes the transition. To inhibit a bit from being written, the bit enable must be at a high level when the clock goes low and not change until the clock goes high. Operation of the clock and the bit enables can be reversed. While the clock is low a positive transition of the bit enable will write that bit into the address selected by A_C–A_2.

READ

When the clock is high any two words may be read out simultaneously, as selected by addresses B_0–B_2 and C_0–C_2, including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates (B_0–B_1), (C_0–C_1).

t_{pd}:

Clock to Data out = 5 ns (typ)
(Read Selected)

Address to Data out = 10 ns (typ)
(Clock High)

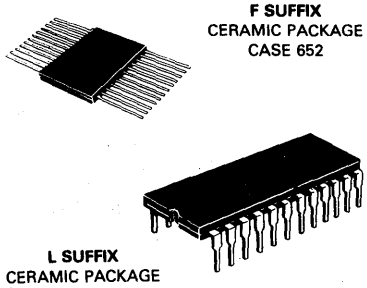
$\overline{\text{Read Enable}}$ to Data out = 2.8 ns (typ)
(Clock high, Addresses present)

P_D = 610 mW/pkg (typ no load)

TRUTH TABLE

*MODE	INPUT							OUTPUT			
	**Clock	$\overline{WE}_0$	$\overline{WE}_1$	D_0	D_1	$\overline{RE}_B$	$\overline{RE}_C$	QB_0	QB_1	QC_0	QC_1
Write	L→H	L	L	H	H	H	H	L	L	L	L
Read	H	ϕ	ϕ	ϕ	ϕ	L	L	H	H	H	H
Read	H→L	ϕ	ϕ	ϕ	ϕ	L	L	H	H	H	H
Read	L→H→L	H	H	ϕ	ϕ	L	L	H	H	H	H
Write	L→H	L	L	L	H	H	H	L	L	L	L
Read	H	ϕ	ϕ	ϕ	ϕ	L	L	L	H	L	H

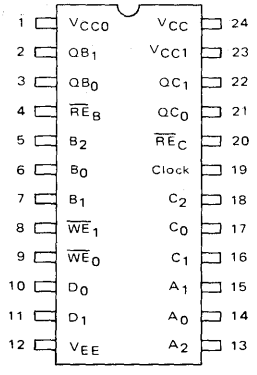
**Note: Clock occurs sequentially through Truth Table
*Note: A0-A2, B0-B2, and C0-C2 are all set to same address location throughout Table.
ϕ = Don't Care



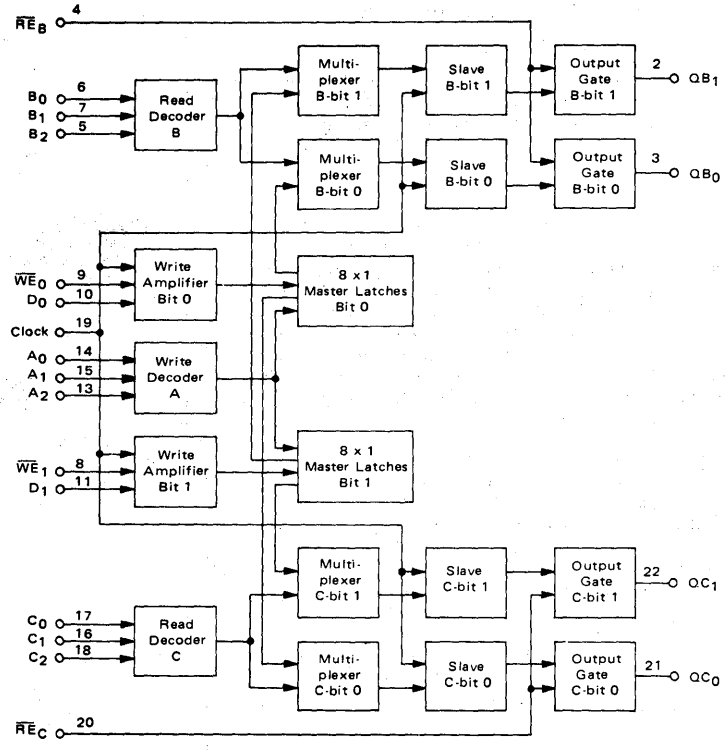
F SUFFIX
CERAMIC PACKAGE
CASE 652

L SUFFIX
CERAMIC PACKAGE
CASE 623

PIN ASSIGNMENT



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current – Continuous – Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

ELECTRICAL CHARACTERISTICS

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

MECL RAM

Characteristics	Symbol	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	–	150	–	118	150	–	150	mAdc
Input Current	I_{inH}								µAdc
Pins 10, 11, 19		–	245	–	–	245	–	245	
All other pins		–	200	–	–	200	–	200	
Switching Times ①									ns
Read Mode									
Address Input	$t_{B\pm QB\pm}$	4.0	15.3	4.5	10	14.5	4.5	15.5	
$\overline{\text{Read Enable}}$	$t_{\overline{RE}-QB+}$	1.1	5.3	1.2	3.5	5.0	1.2	5.5	
Data	$t_{Clock+QB-}$	1.7	7.3	2.0	5.0	7.0	2.0	7.6	
Setup									
Address	$t_{setup(B-Clock-)}$	–	–	8.5	5.5	–	–	–	
Hold									
Address	$t_{hold(Clock-B+)}$	–	–	-1.5	-4.5	–	–	–	
Write Mode									
Setup									
$\overline{\text{Write Enable}}$	$t_{setup(\overline{WE}-Clock+)}$	–	–	7.0	4.0	–	–	–	
	$t_{setup(\overline{WE}+Clock-)}$	–	–	1.0	-2.0	–	–	–	
Address	$t_{setup(A-Clock+)}$	–	–	8.0	5.0	–	–	–	
Data	$t_{setup(D-Clock+)}$	–	–	5.0	2.0	–	–	–	
Hold									
$\overline{\text{Write Enable}}$	$t_{hold(Clock-\overline{WE}+)}$	–	–	5.5	2.5	–	–	–	
	$t_{hold(Clock+\overline{WE}-)}$	–	–	1.0	-2.0	–	–	–	
Address	$t_{hold(Clock+A+)}$	–	–	1.0	-3.0	–	–	–	
Data	$t_{hold(Clock+D+)}$	–	–	1.0	-2.0	–	–	–	
Write Pulse Width	$PW_{\overline{WE}}$	–	–	8.0	5.0	–	–	–	
Rise Time, Fall Time (20% to 80%)	t_r, t_f	1.1	4.2	1.1	2.5	4.0	1.1	4.5	

①AC timing figures do not show all the necessary presetting conditions.

READ TIMING DIAGRAMS

Access (Clock High)

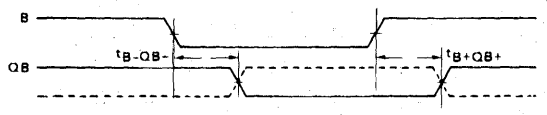


FIGURE 1

Enable

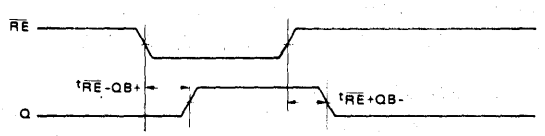


FIGURE 2

Data (Address Selected)

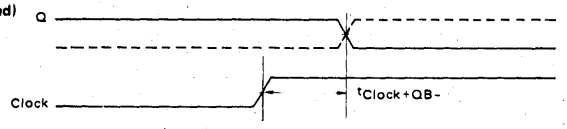


FIGURE 3

Setup and Hold

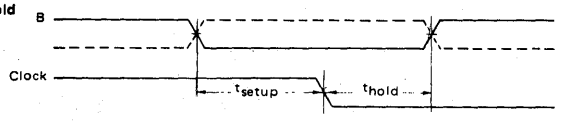


FIGURE 4

WRITE TIMING DIAGRAM

Enable Setup

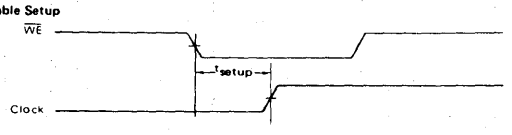


FIGURE 5

Enable Hold

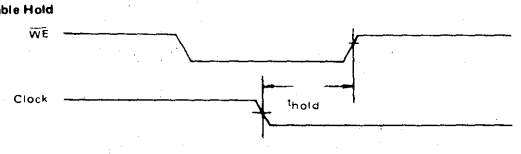


FIGURE 6

Disable

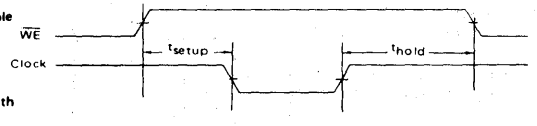


FIGURE 7

Pulse Width

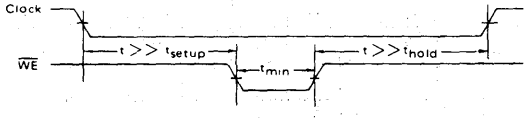


FIGURE 8

Address

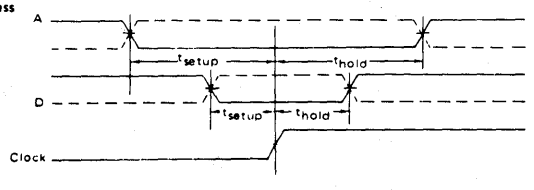


FIGURE 9

MOTOROLA

MC10H145

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

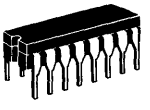
The MC10H145 is a member of Motorola's new MECL family. The MC10H145 is a 16 × 4 bit register file. The active-low chip select allows easy expansion.

The operating mode of the register file is controlled by the $\overline{WE}$ input. When $\overline{WE}$ is "low" the device is in the write mode, the outputs are "low" and the data present at D_n input is stored at the selected address. when $\overline{WE}$ is "high", the device is in the read mode — the data state at the selected location is present at the Q_n outputs.

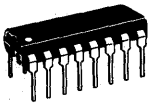
- Address Access Time, 3.5 ns Typical
- Power Dissipation, 700 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

16 × 4 BIT REGISTER FILE



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MECL RAM

MAXIMUM RATINGS

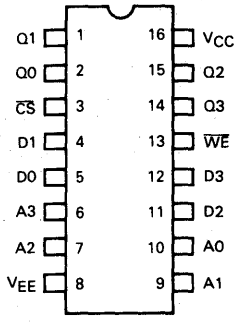
Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ± 5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	165	—	150	—	165	mA
Input Current High	I_{inH}	—	375	—	220	—	220	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

PIN ASSIGNMENT



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care

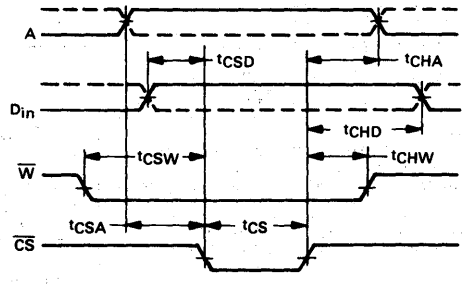
Q-State of Addressed Cell

AC PARAMETERS

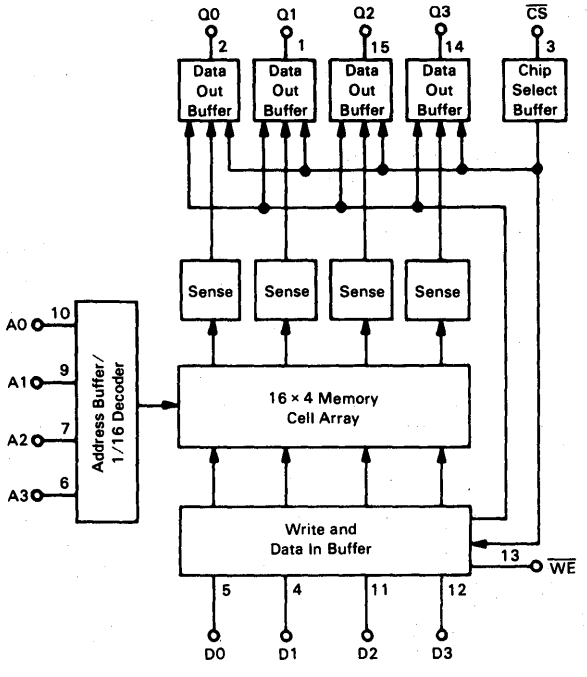
Characteristics	Symbol	MC10H145 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ±5% Min	Max	Unit	Conditions
Read Mode				ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	1.0	4.0		
Chip Select Recovery Time	t_{RCS}	1.0	4.0		
Address Access Time	t_{AA}	2.0	6.0		
Write Mode				ns	t_{WSA} = 3.5 ns Measured at 50% of input to 50% of output. t_W = 4.0 ns.
Write Pulse Width	t_W	4.0	—		
Data Setup Time Prior to Write	t_{WSD}	0	—		
Data Hold Time After Write	t_{WHD}	1.5	—		
Address Setup Time Prior to Write	t_{WSA}	3.5	—		
Address Hold Time After Write	t_{WHA}	0.5	—		
Chip Select Setup Time Prior to Write	t_{WSCS}	0	—		
Chip Select Hold Time After Write	t_{WHCS}	1.5	—		
Write Disable Time	t_{WS}	1.0	6.0		
Write Recovery Time	t_{WR}	1.0	6.0		
Chip Enable Strobe Mode				ns	Guaranteed but not tested on standard product. See Figure 1.
Data Setup Prior to Chip Select	t_{CSD}	0	—		
Write Enable Setup Prior to Chip Select	t_{CSW}	0	—		
Address Setup Prior to Chip Select	t_{CSA}	0	—		
Data Hold Time After Chip Select	t_{CHD}	1.0	—		
Write Enable Hold Time After Chip Select	t_{CHW}	0	—		
Address Hold Time After Chip Select	t_{CHA}	2.0	—		
Chip Select Minimum Pulse Width	t_{CS}	10	—		
Rise and Fall Time	t_r, t_f			ns	Measured between 20% and 80% points.
Address to Output		0.7	2.5		
CS to Output		0.7	2.5		
Capacitance				pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	6.0		
Output Capacitance	C_{out}	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MC10H145. $C_L \leq 5.0$ pF (including jig and Stray Capacitance). Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
3. For proper use of MECL in a system environment, consult MECL System Design Handbook.

FIGURE 1 — CHIP ENABLE STROBE MODE



16 × 4 Bit Register File



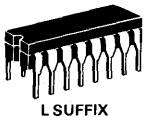
MOTOROLA

MCM10145

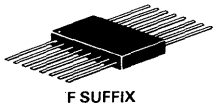
64-BIT REGISTER FILE (RAM)

The MCM10145 is a 64-Bit RAM organized as a 16 x 4 array. This organization and the high speed make the MCM10145 particularly useful in register file or small scratch pad applications. Fully decoded inputs, together with a chip enable, provide expansion of memory capacity. The Write Enable input, when low, allows data to be entered; when high, disables the data inputs. The Chip Select input when low, allows full functional operation of the device; when high, all outputs go to a low logic state. The Chip Select, together with open emitter outputs allow full wire-ORing and data bussing capability. On-chip input pulldown resistors allow unused inputs to remain open.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 4.5 ns
- Operating Temperature Range = 0° to +75°C
- 50 kΩ Pulldown Resistors on All Inputs
- Fully Compatible with MECL 10,000
- Pin-for-Pin Compatible with the F10145

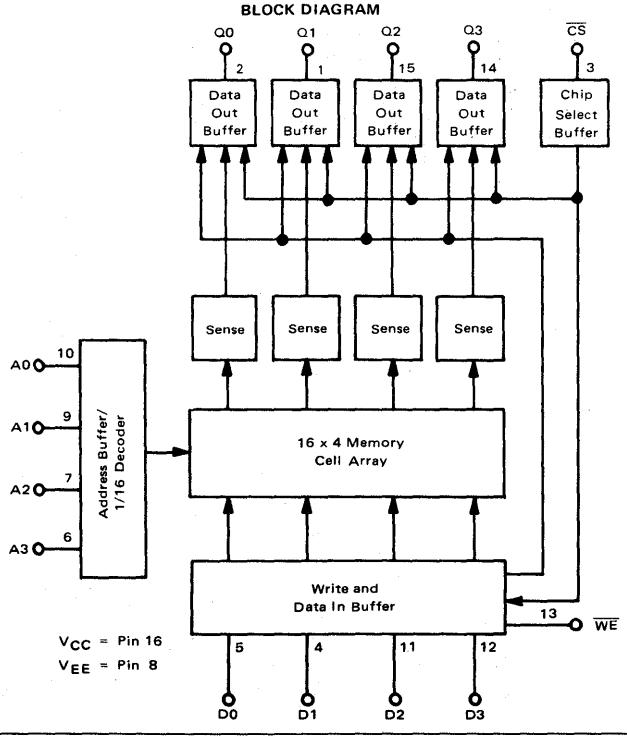


L SUFFIX
CERAMIC PACKAGE
CASE 620

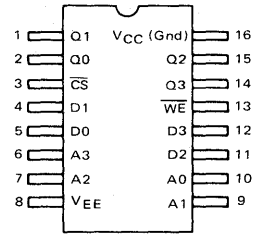


F SUFFIX
CERAMIC PACKAGE
CASE 650

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

$\overline{CS}$	Chip Select Input
A0 thru A3	Address Inputs
D0 thru D3	Data Inputs
Q0 thru Q3	Data Outputs
$\overline{WE}$	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM10145 is a 16 word x 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 thru A3.

The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_n is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Q_n.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current – Continuous – Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

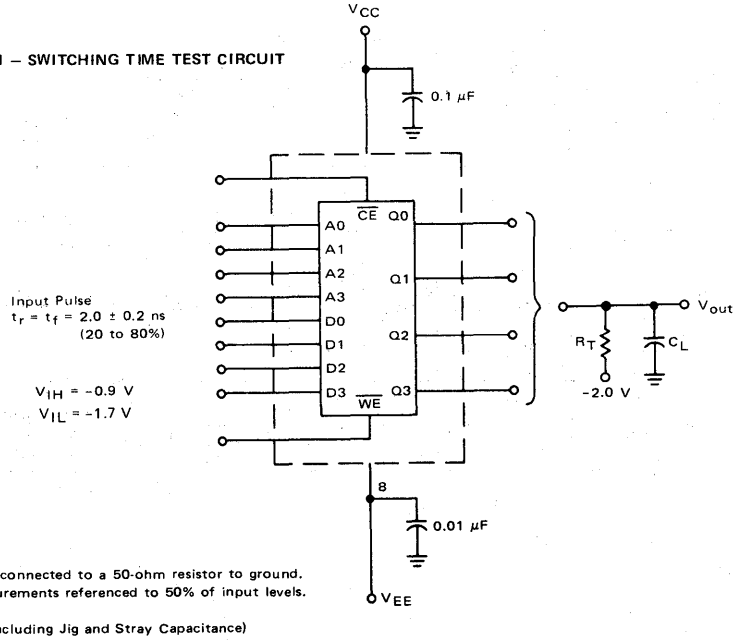
DC Characteristics	Symbol	MCM10145 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	Conditions
Power Supply Drain Current	I_{EE}		130		125	–	120	mAdc	Typ I_{EE} @ 25°C = 90 mA All outputs and inputs open. Measure pin 8.
Input Current High	I_{inH}		220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	I_{inL}	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = −5.2 Vdc ±5%; Output Load see Figure 1; see Note 2.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.5	8.0	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	5.0	8.0	ns	output. See Note 1.
Address Access Time	t_{AA}	4.0	10	15	ns	
Write Mode						
Write Pulse Width	t_W	8.0	–	–	ns	t_{WSA} = 5 ns
Data Setup Time Prior to Write	t_{WSD}	0	-6.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	3.0	0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	5.0	1.0	–	ns	t_W = 8 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	1.0	-3.0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	0	-5.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	0	-6.0	–	ns	
Write Disable Time	t_{WS}	2.0	5.0	8.0	ns	
Write Recovery Time	t_{WR}	2.0	5.0	8.0	ns	
Chip Enable Strobe Mode						
Data Setup Prior to Chip Select	t_{CSD}	0	-6.0	–	ns	Guaranteed but not tested on standard
Write Enable Setup Prior to Chip Select	t_{CSW}	0	-3.0	–	ns	product. See Figure 5.
Address Setup Prior to Chip Select	t_{CSA}	0	-3.0	–	ns	
Data Hold Time After Chip Select	t_{CHD}	2.0	-1.0	–	ns	
Write Enable Hold Time After Chip Select	t_{CHW}	0	-6.0	–	ns	
Address Hold Time After Chip Select	t_{CHA}	4.0	-1.0	–	ns	
Chip Select Minimum Pulse Width	t_{CS}	18	12	–	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Address to Output	t_r, t_f	1.5	3.0	7.0	ns	
$\overline{CS}$ to Output	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	6.0	pF	
Output Capacitance	C_{out}	–	5.0	8.0	pF	

Notes:
1. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
2. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



Unused outputs connected to a 50-ohm resistor to ground.
All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (Including Jig and Stray Capacitance)
Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.

FIGURE 2 – CHIP SELECT ACCESS TIME

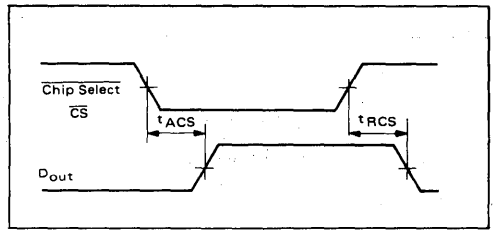


FIGURE 3 – ADDRESS ACCESS TIME

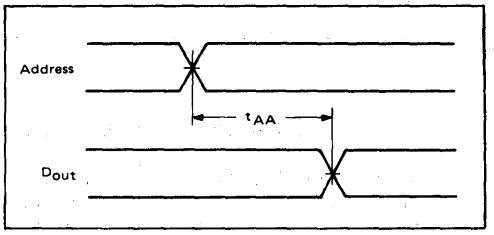


FIGURE 4 – WRITE MODE

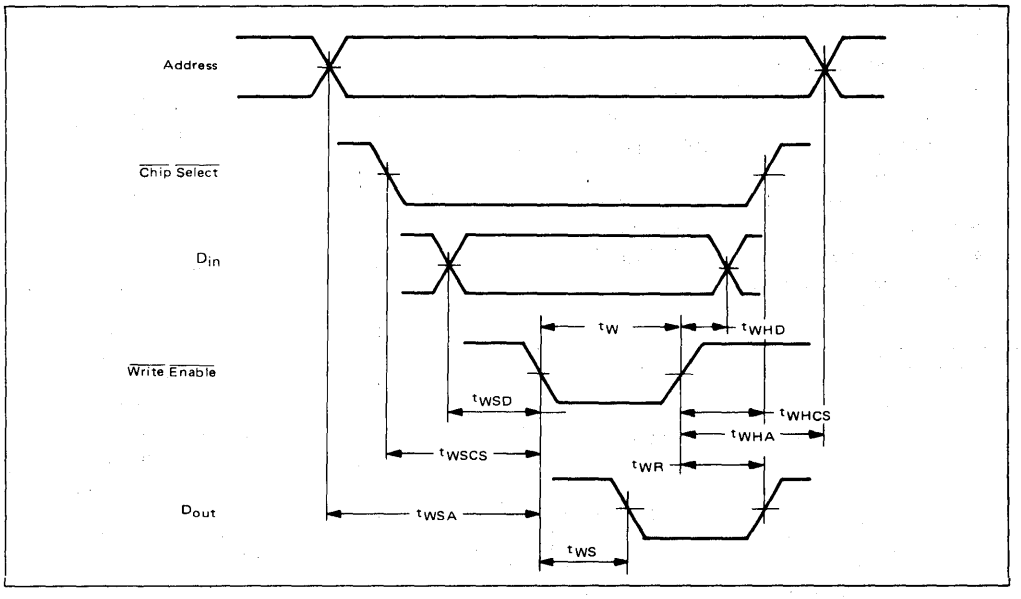
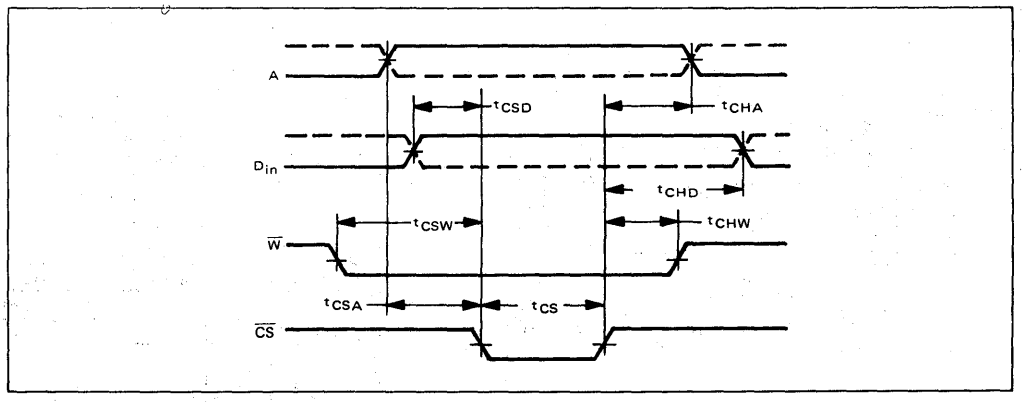


FIGURE 5 – CHIP ENABLE STROBE MODE



MECL RAM

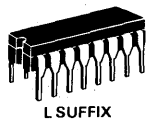
MOTOROLA

MCM10144

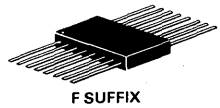
256 x 1-BIT RANDOM ACCESS MEMORY

The MCM10144 is a 256 word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of an 8-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 3 active-low chip select lines. It has a typical access time of 17 ns and is designed for high-speed scratch pad, control, cache, and buffer storage applications.

- Typical Address Access Time = 17 ns
- Typical Chip Select Access Time = 4.0 ns
- Operating Temperature Range = 0° to +75°C
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on Chip Select
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family
- Pin-for-Pin Replacement for F10410

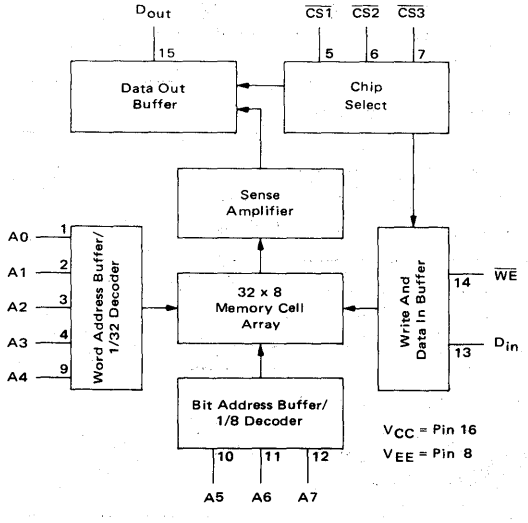


L SUFFIX
CERAMIC PACKAGE
CASE 620

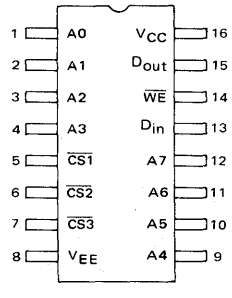


F SUFFIX
CERAMIC PACKAGE
CASE 650

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A7	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM10144 is a 256 word x 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 thru A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

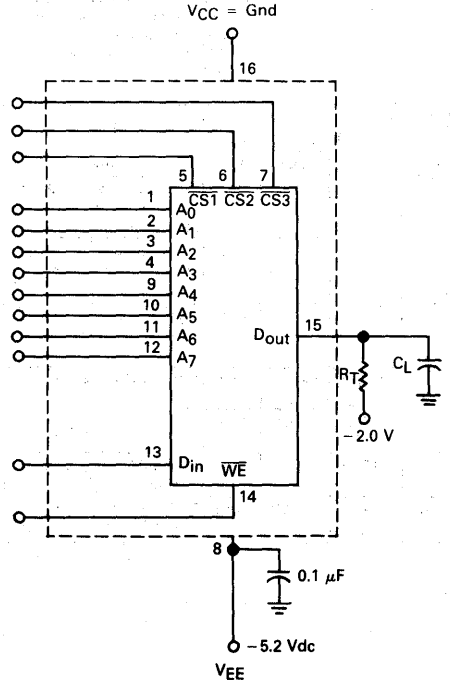
		MCM10144 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	130	–	125	–	120	mAdc	Typ I_{EE} @ 25°C = 90 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

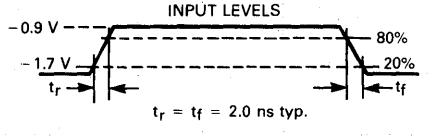
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	10	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	4.0	10	ns	output. See Note 2.
Address Access Time	t_{AA}	7.0	17	26	ns	
Write Mode						
Write Pulse Width	t_W	25	6.0	–	ns	t_{WSA} = 8.0 ns
Data Setup Time Prior to Write	t_{WSD}	2.0	-3.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	2.0	-3.0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	8.0	0	–	ns	t_W = 25 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	0.0	-4.0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	-3.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	2.0	-3.0	–	ns	
Write Disable Time	t_{WS}	2.5	5.0	10	ns	
Write Recovery Time	t_{WR}	2.5	5.0	10	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	7.0	ns	When driven from Address inputs.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	5.0	ns	When driven from $\overline{CS}$ or $\overline{WE}$ inputs.
Capacitance						
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





$t_r = t_f$ = 2.0 ns typ.

All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF

FIGURE 2 – CHIP SELECT ACCESS TIME

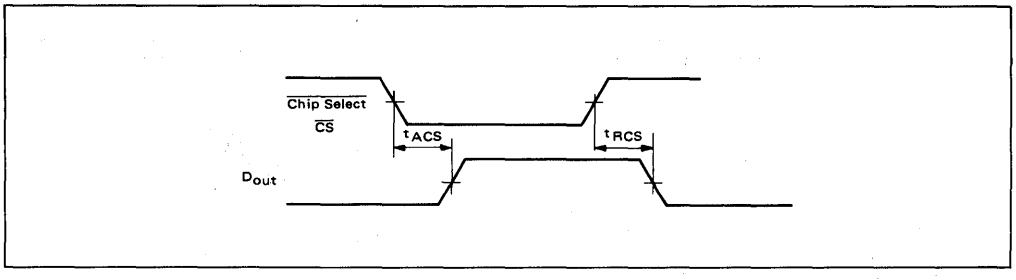


FIGURE 3 – ADDRESS ACCESS TIME

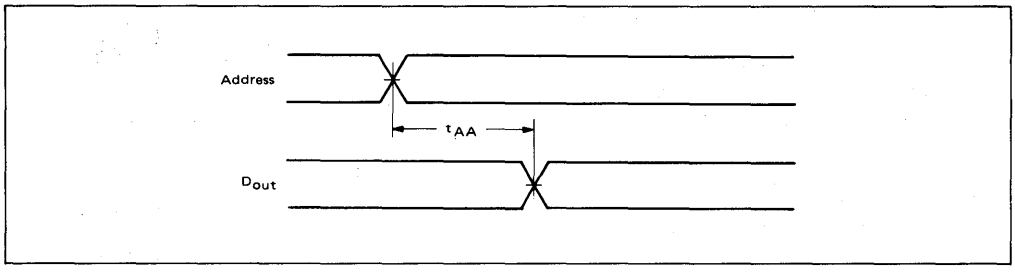
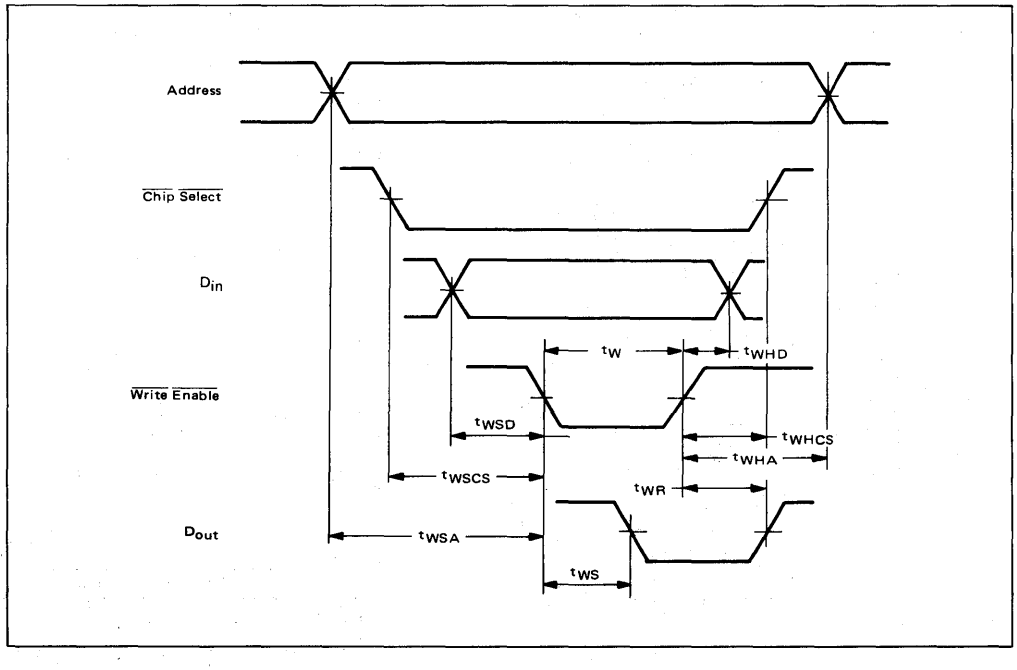


FIGURE 4 – WRITE MODE



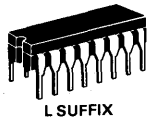
MOTOROLA

MCM10152

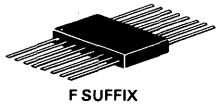
256 x 1-BIT RANDOM ACCESS MEMORY

The MCM10152 is a 256 word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of an 8-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 3 active-low chip select lines. It has a typical access time of 11 ns and is designed for high-speed scratch pad, control, cache, and buffer storage applications.

- Typical Address Access Time = 11 ns
- Typical Chip Select Access Time = 4.0 ns
- Operating Temperature Range = 0° to +75°C
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family

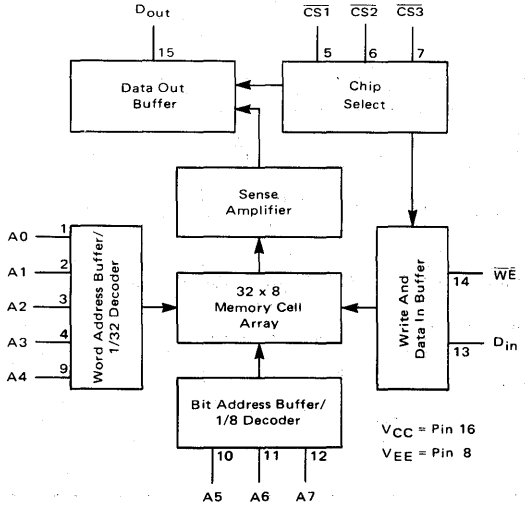


L SUFFIX
CERAMIC PACKAGE
CASE 620

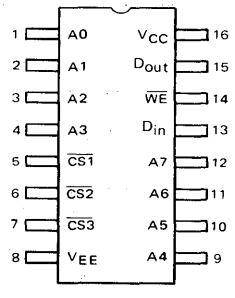


F SUFFIX
CERAMIC PACKAGE
CASE 650

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A7	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM10152 is a 256 word x 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 thru A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		MCM10152 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	135	–	130	–	125	mAdc	Typ I_{EE} @ 25°C = 110 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	7.5	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	4.0	7.5	ns	output. See Note 2.
Address Access Time	t_{AA}	7.0	11	15	ns	
Write Mode						
Write Pulse Width	t_W	10	6.0	–	ns	t_{WSA} = 5.0 ns
Data Setup Time Prior to Write	t_{WSD}	2.0	-3.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	2.0	-2.0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	5.0	3.0	–	ns	t_W = 10 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	3.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	-3.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	2.0	-3.0	–	ns	
Write Disable Time	t_{WS}	2.5	5.0	7.5	ns	
Write Recovery Time	t_{WR}	2.5	5.0	7.5	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.

(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT

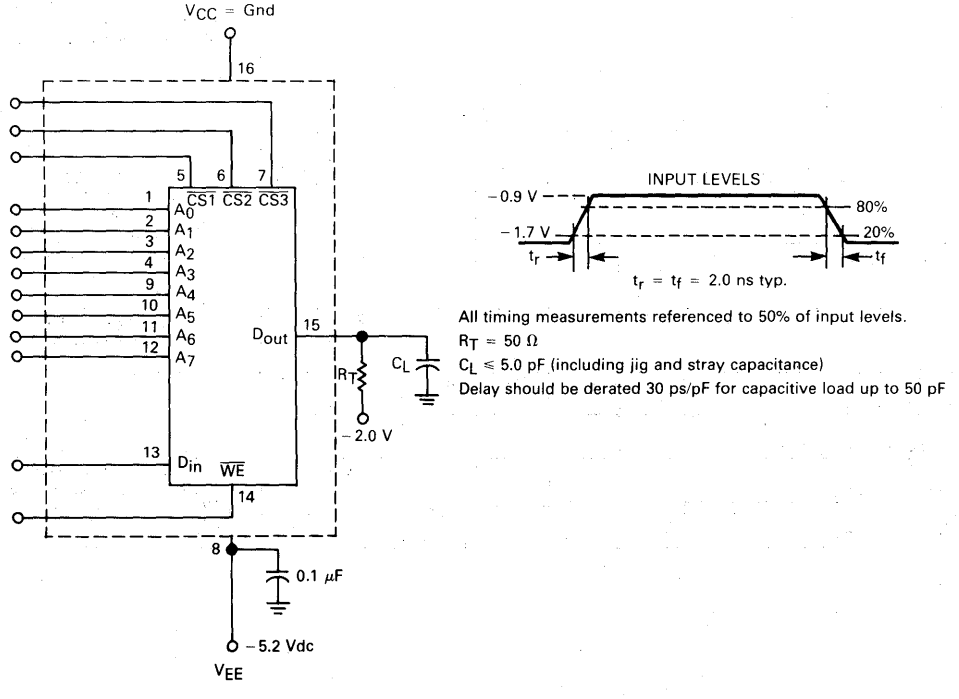


FIGURE 2 – CHIP SELECT ACCESS TIME

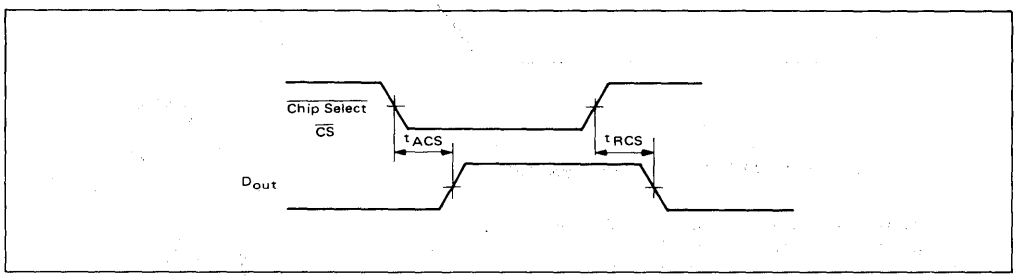


FIGURE 3 – ADDRESS ACCESS TIME

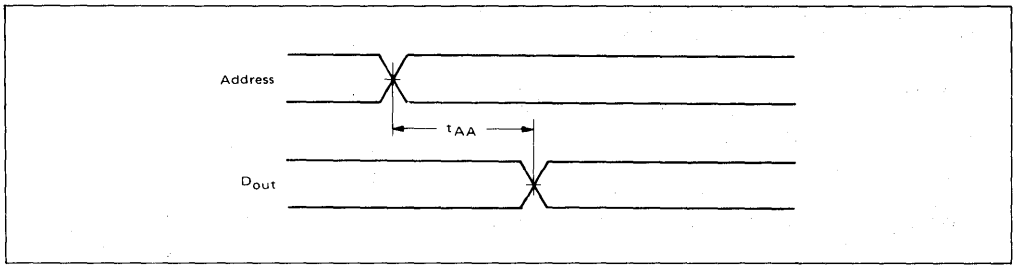
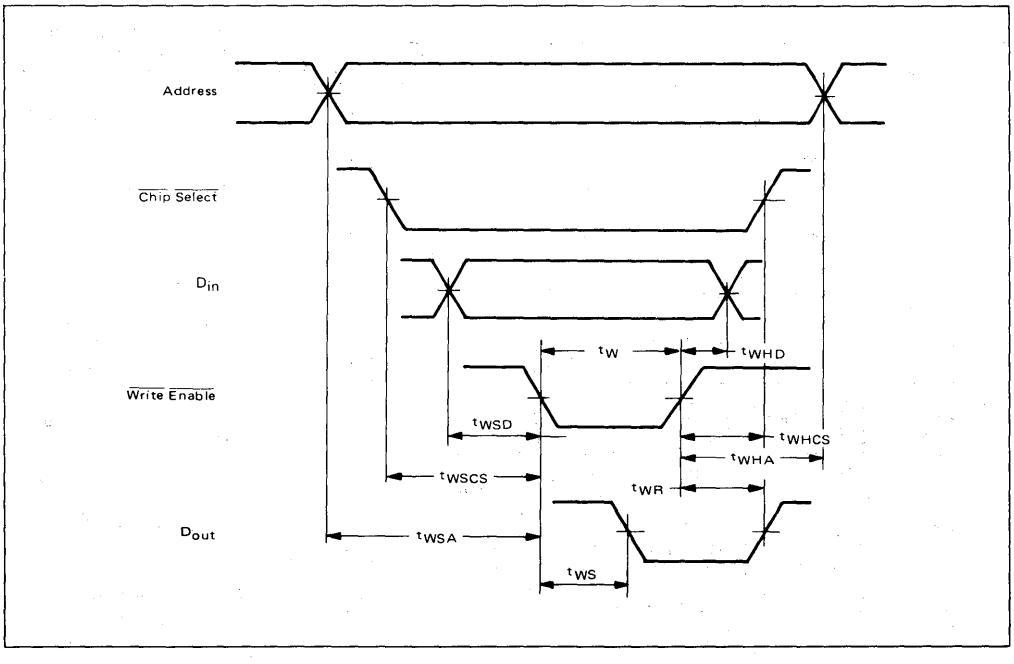


FIGURE 4 – WRITE MODE



MOTOROLA

MCM10415-15
MCM10415-20

MECL 1024-BIT RANDOM ACCESS MEMORY

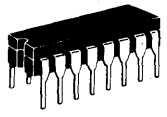
MECL RAM

1024 x 1-BIT RANDOM ACCESS MEMORY

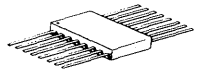
The MCM10415 is a 1024-bit Read/Write Random Access Memory organized 1024 words by 1 bit. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with a separate data in line, a noninverting data output, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Address Access Time: MCM10415-20 20 ns (Max)
  MCM10415-15 15 ns (Max)
- Fully Compatible with MECL 10K/10KH
- Temperature Range of 0° to 75°C
- Emitter-Follower Output Permits Full Wire-ORing
- Power Dissipation Decreases with Increasing Temperature



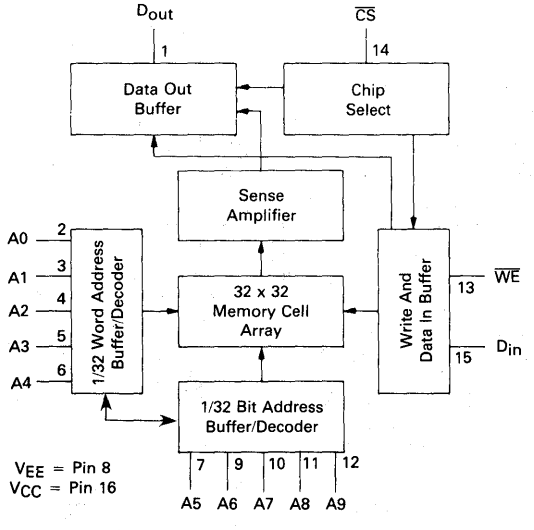
L SUFFIX
CERAMIC PACKAGE
CASE 620



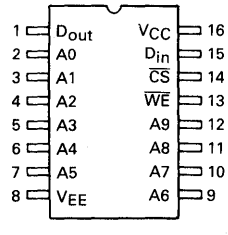
F SUFFIX
CERAMIC PACKAGE
CASE 650

ORDERING INFORMATION
Suffix Denotes
MCM10415L15 — Ceramic Dual-in-Line Package
MCM10415F15 — Ceramic Flat Package
MCM10415L20 — Ceramic Dual-in-Line Package
MCM10415F20 — Ceramic Flat Package

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESIGNATION

$\overline{CS}$	Chip Select Input
A0 to A9	Address Inputs
D_{in}	Data Inputs
D_{out}	Data Output
$\overline{WE}$	Write Enable Input

FUNCTIONAL DESCRIPTION:

This device is a 1024 x 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM (CS input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented noninverted at D_{out}. (See Truth Table)

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	<50 <100	mAdc
Junction Operating Temperature	T_J	<165	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	−0.840	−1.870	−1.145	−1.490	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+75°C	−0.720	−1.830	−1.045	−1.450	−5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

		MCM10415 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	—	150	—	145	—	125	mAdc	Typ I_{EE} @ 25°C = 100 mA All outputs and inputs open. Measure Pin 8.
Input Current High	I_{inH}	—	220	—	220	—	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low ($\overline{CS}$ only) Input Curent Low (All Others)	I_{inL}	0.5 −50	—	0.5 −50	—	0.3 −50	—	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	Load 50 Ω to −2.0 V
Logic "0" Output Voltage	V_{OL}	−1.870	−1.665	−1.850	−1.650	−1.830	−1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	−1.020	—	−0.980	—	−0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to −2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	—	−1.645	—	−1.630	—	−1.605	Vdc	

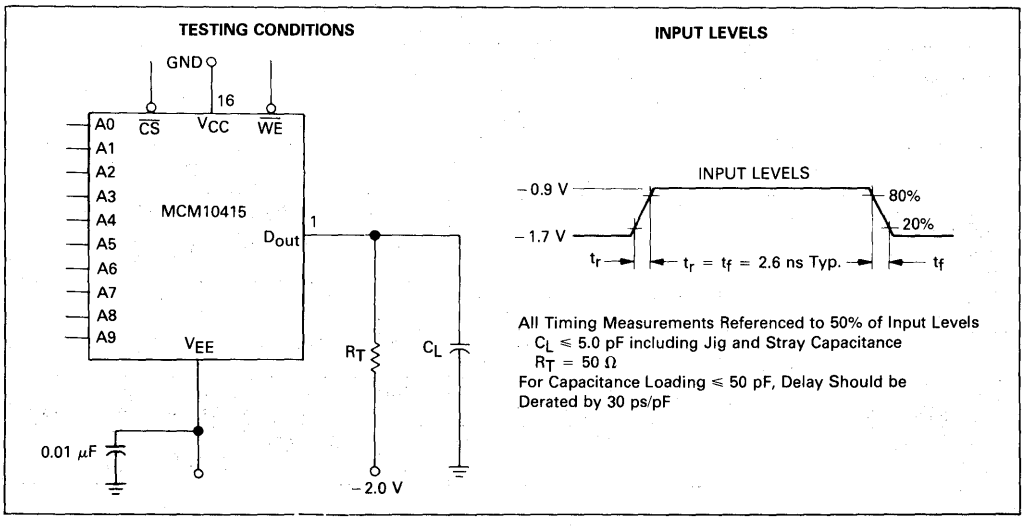
MECL RAM

Guaranteed with V_{EE} = −5.2 Vdc ±5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10415-20 Min	MCM10415-20 Max	MCM10415-15 Min	MCM10415-15 Max	Unit	Conditions
Read Mode							See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	—	8.0	—	7.0	ns	Measured at 50% of input to 50% of output.
Chip Select Recovery Time	t_{RCS}	—	8.0	—	7.0	ns	See Note 2.
Address Access Time	t_{AA}	—	20	—	15	ns	
Write Mode							See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	14	—	12	—	ns	t_{WSA} = 3.0 ns — MCM10415-20 t_{WSA} = 2.0 ns — MCM10415-15 Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	3.0	—	2.0	—	ns	
Data Hold Time After Write	t_{WHD}	3.0	—	1.0	—	ns	
Address Setup Time Prior to Write	t_{WSA}	3.0	—	2.0	—	ns	t_W = 14 ns — MCM10415-20 t_W = 12 ns — MCM10415-15
Address Hold Time After Write	t_{WHA}	3.0	—	1.0	—	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	3.0	—	2.0	—	ns	
Chip Select Hold Time After Write	t_{WHCS}	3.0	—	1.0	—	ns	
Write Disable Time	t_{WS}	—	8.0	—	7.0	ns	
Write Recovery Time	t_{WR}	—	8.0	—	7.0	ns	
Rise and Fall Time							Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	4.0	1.5	4.0	ns	When driven from $\overline{CS}$ or $\overline{WE}$ inputs.
Output Rise and Fall Time	t_r, t_f	1.5	8.0	1.5	8.0	ns	When driven from Address inputs.
Capacitance							Measured with a pulse technique. See Note 4.
Input Lead Capacitance	C_{in}	—	5.0	—	5.0	pF	
Output Lead Capacitance	C_{out}	—	8.0	—	8.0	pF	

Notes:
(1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a System environment, consult: "MECL System Design Handbook."
(4) Typical ratings are 3.0 pF for C_{in} and 5.0 pF for C_{out}.

FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MCM10422-10
MCM10422-15

Advance Information

256 x 4-BIT RANDOM ACCESS MEMORY

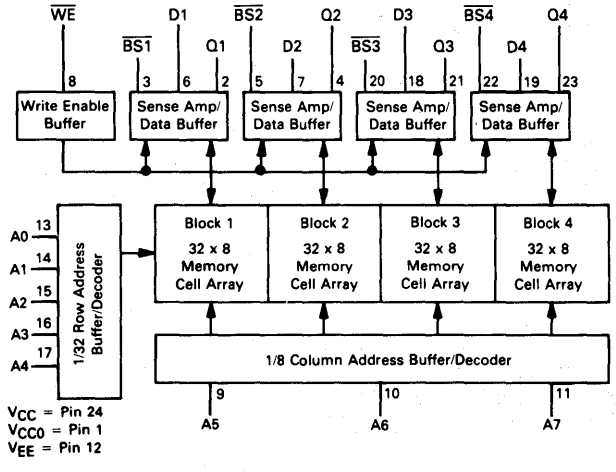
The MCM10422 is a high-speed 1024-bit Read/Write RAM organized 256 words by 4 bits, designed for high speed scratch pad, control, cache, and buffer storage applications. Four independent active-low Block Selects permit use in 1024 x 1 and 512 x 2-bit applications. It has full address decoding on chip, separate data inputs, noninverting data outputs, and an active-low Write Enable.

- Address Access Time:
  MCM10422-15 15 ns (Max)
  MCM10422-10 10 ns (Max)
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10K and 10KH
- Operating Temperature Range 0°C to 75°C
- Four Independent Block Selects
- Emitter-Follower Outputs Permits Full Wire-OR'ing
- Standard 24-Pin, 400 Mil Wide, Dual In-Line Package

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current	I_O	< 50	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

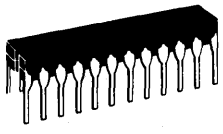
BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MECL

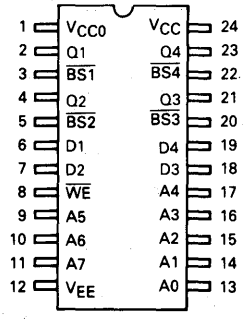
256 x 4-BIT RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 748-01

ORDERING INFORMATION
Suffix Denotes
MCM10422L10 — Ceramic Dual-in-Line Package
MCM10422L15 — Ceramic Dual-in-Line Package

PIN ASSIGNMENT



PIN DESIGNATION

$\overline{BS1}$	—	$\overline{BS4}$	Block Select Inputs
A0	—	A7	Address Inputs
D_{in}			Data Inputs
Q_{out}			Data Outputs
$\overline{WE}$			Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{BS}_n$	$\overline{WE}$	D_{in}	Q_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Block Disabled	H	ϕ	ϕ	L

ϕ Don't Care NOTE: Blocks Enable Independently

MECL RAM

FUNCTIONAL DESCRIPTION:

This device is a 256 x 4-bit RAM. Word selection is achieved by means of an 8-bit address, A0–A7.

The operating mode of each block ($\overline{BS}_n$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the block is in the write mode, the output Q_{out} is low and the data state present at D_{in} is stored at the selected address in block n. With $\overline{WE}$ high, the block is in the read mode and the data stored at the selected memory location will be presented non-inverted at Q_{out}.

The independent, active-low Block Selects and the wire-OR capability of the emitter-follower outputs permit use as a 1024 x 1 or 512 x 2-bit RAM. For example, for use as a 1024 x 1-bit RAM tie all D_{in} inputs together to form a single D_{in}, wire-OR the Q_{out} lines together to form a single Q_{out} line, and drive the Block Selects with a 1-of-4 low decoder.

DC OPERATING CONDITIONS AND CHARACTERISTICS

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	−0.840	−1.870	−1.145	−1.490	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+75°C	−0.720	−1.830	−1.045	−1.450	−5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

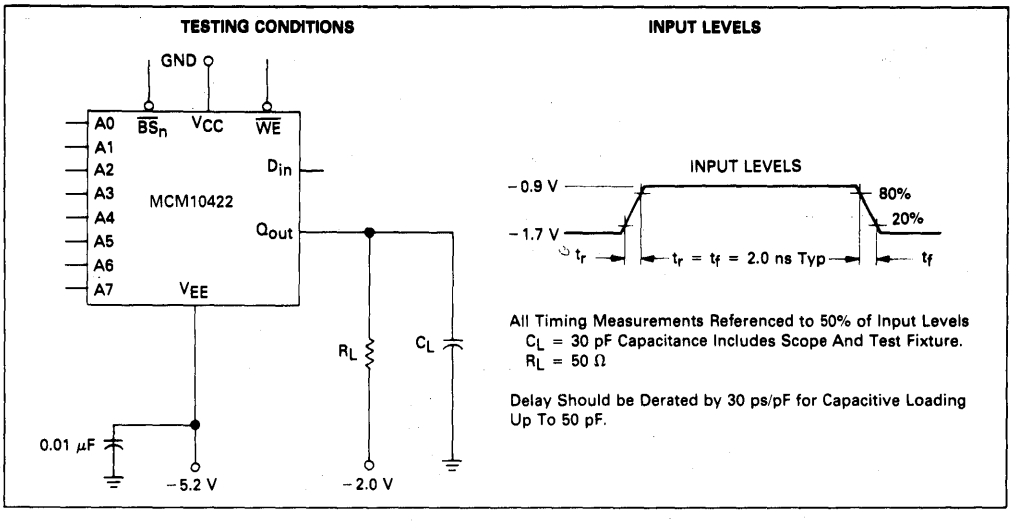
		MCM10422 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	—	200	—	195	—	185	mAdc	All outputs and inputs open. Measure Pin 12.
Input Current High	I_{inH}	—	220	—	220	—	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH(max)}$
Input Current Low (Block Selects)	I_{inL}	0.5	—	0.5	—	0.5	—	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL(min)}$
Input Current Low*	I_{inL}	−50	—	−50	—	−50	—	μAdc	
Logic "1" Output Voltage	V_{OH}	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	Load 50 Ω to −2.0 V
Logic "0" Output Voltage	V_{OL}	−1.870	−1.665	−1.850	−1.650	−1.830	−1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	−1.020	—	−0.980	—	−0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to −2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	—	−1.645	—	−1.630	—	−1.605	Vdc	

*Minimum limit equals the maximum negative current the driving circuitry will be required to sink.

	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
Package	Blown*	Still	
L Suffix	35°C/W	55°C/W	15°C/W

*500 linear ft. per minute blown air.

FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS



MECL RAM

AC OPERATING CONDITIONS AND CHARACTERISTICS

Guaranteed with V_{EE} = −5.2 Vdc ±5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characterstic	Symbol	MCM10422-15 Min	MCM10422-15 Max	MCM10422-10 Min	MCM10422-10 Max	Unit	Conditions
Read Mode							See Figures 2 and 3.
Block Select Access Time	t_{ABS}	—	6.0	—	5.0	ns	Measured at 50% of input
Block Select Recovery Time	t_{RBS}	—	6.0	—	5.0	ns	to 50% of output.
Address Access Time	t_{AA}	—	15	—	10	ns	See Note 1.
Write Mode							See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	10	—	7.0	—	ns	t_{WSA} = 2.0 ns. MCM10422-15 t_{WSA} = 1.0 ns MCM10422-10 Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	1.0	—	1.0	—	ns	
Data Hold Time After Write	t_{WHD}	4.0	—	2.0	—	ns	
Address Setup Time Prior to Write	t_{WSA}	2.0	—	1.0	—	ns	t_W = 10 ns MCM10422-15 t_W = 7.0 ns MCM10422-10
Address Hold Time After Write	t_{WHA}	3.0	—	2.0	—	ns	
Block Select Setup Time Prior to Write	t_{WSBS}	2.0	—	1.0	—	ns	
Block Select Hold Time After Write	t_{WHBS}	3.0	—	2.0	—	ns	
Write Disable Time	t_{WS}	—	5.0	—	5.0	ns	
Write Recovery Time	t_{WR}	—	9.0	—	9.0	ns	
Rise and Fall Time		TYPICAL					Measured between 20% and 80%
Output Rise and Fall Time	t_r, t_f	2.0				ns	points.
Capacitance		TYPICAL					Measured with a pulse technique.
Input Lead Capacitance	C_{in}	5.0				pF	
Output Lead Capacitance	C_{out}	5.0				pF	

Notes:
(1) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(2) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 2 — BLOCK SELECT ACCESS TIME

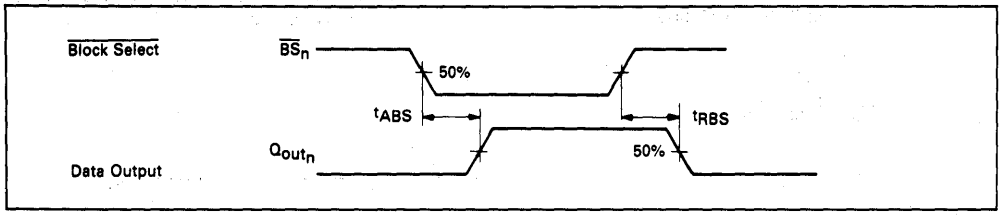


FIGURE 3 — ADDRESS ACCESS TIME

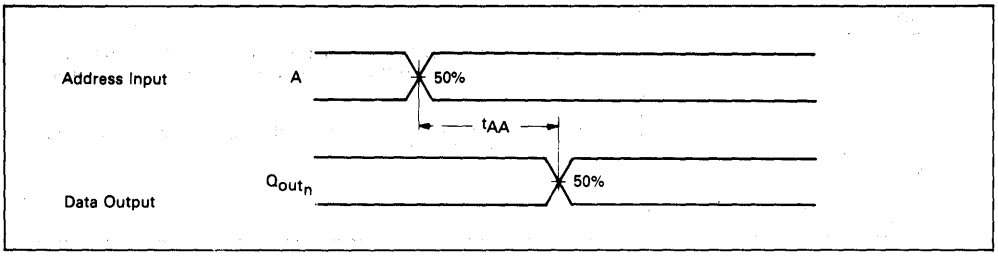
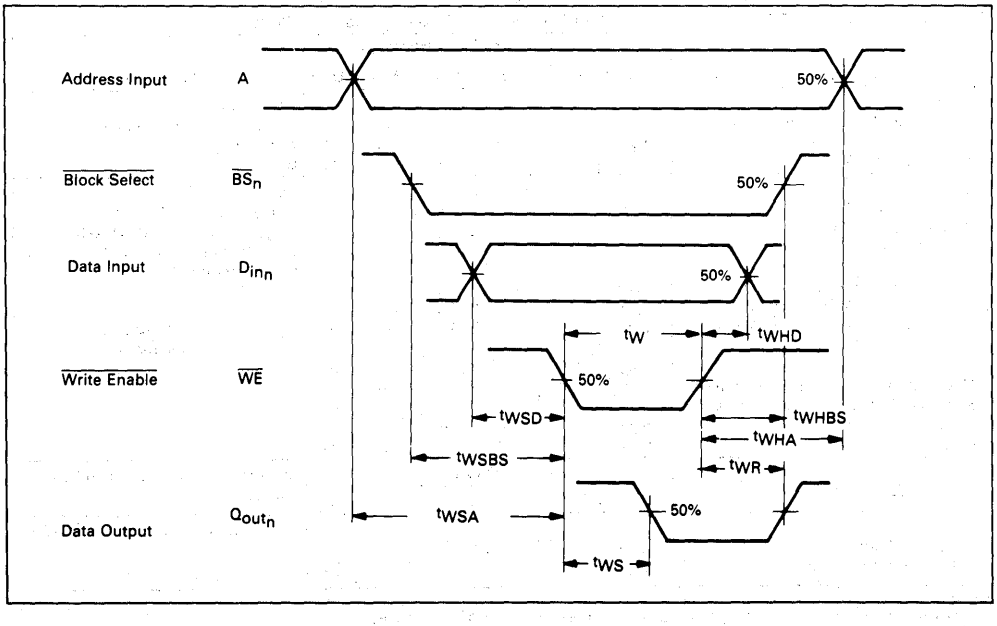


FIGURE 4 — WRITE STROBE MODE



MOTOROLA

MCM10470-15
MCM10470-25

Advance Information

4096 x 1-BIT RANDOM ACCESS MEMORY

The MCM10470 is a 4096-bit Read/Write RAM organized for 4096 words by 1 bit. Data is selected or stored by means of a 12-bit address (A0 through A11) decoded on the chip. The chip is designed with a separate data-in line, a noninverting data output, and an active-low chip select.

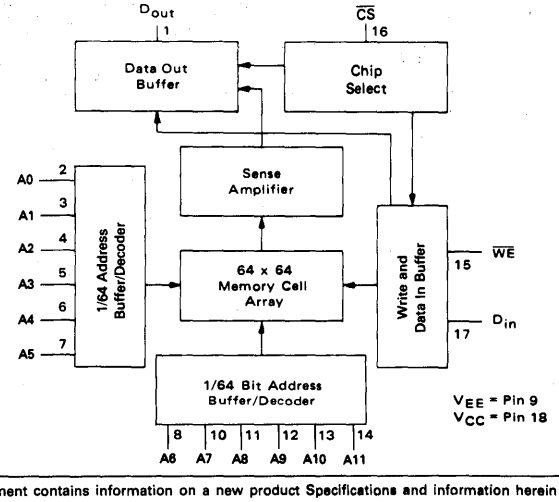
This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Fully Compatible with MECL 10K/10KH
- Pin-for-Pin Compatible with the Industry's Standard 10470
- Temperature Range of 0° to 75°C
- Emitter-Follower Output Permits Full Wire-ORing
- Power Dissipation Decreases with Increasing Temperature
- Address Access Time: MCM10470-25 25 ns (Max)
  MCM10470-15 15 ns (Max)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current	I_O	−30	mAdc
Junction Operating Temperature	T_J	≤ 165	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM

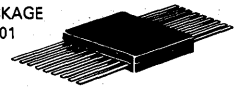


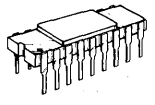
This document contains information on a new product Specifications and information herein are subject to change without notice.

MECL

4096 x 1-BIT RANDOM ACCESS MEMORY

F SUFFIX
CERAMIC PACKAGE
CASE 747-01



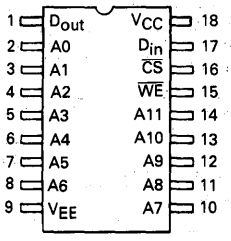


L SUFFIX
CERAMIC PACKAGE
CASE 680-06

ORDERING INFORMATION
Suffix Denotes

MCM10470L15 — Ceramic Dual-in-Line Package
MCM10470F15 — Ceramic Flat Package
MCM10470L25 — Ceramic Dual-in-Line Package
MCM10470F25 — Ceramic Flat Package

PIN ASSIGNMENT



PIN DESIGNATION

$\overline{CS}$	Chip Select
A0-A11	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Irrelevant

MECL RAM

FUNCTIONAL DESCRIPTION:

This device is a 4096 x 1-bit RAM. Bit selection is achieved by means of a 12-bit address, A0 to A11.

The active-low chip select is provided for memory expansion.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out}. (See Truth Table)

DC OPERATING CONDITIONS AND CHARACTERISTICS

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

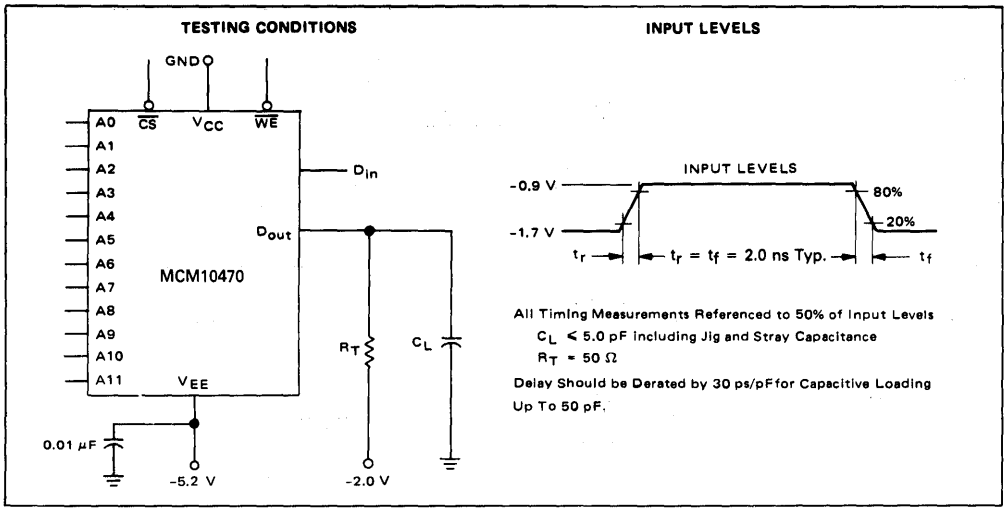
ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

		MCM10470 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current MCM10470 MCM10470A	I_{EE}	— — —	— 205 205	— — —	— 200 200	— — —	— 190 190	mAdc	All outputs and inputs open. Measure Pin 9.
Input Current High	I_{inH}	—	220	—	220	—	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH(max)}$.
Input Current Low Chip Select	I_{inL}	0.5	—	0.5	—	0.3	—	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL(min)}$.
Input Current Low*	I_{inL}	-50	—	-50	—	-50	—	μAdc	
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	—	-0.980	—	-0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	—	-1.645	—	-1.630	—	-1.605	Vdc	

* Minimum limit equals the maximum negative current the driving circuitry will be required to sink.

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS



MECL RAM

AC OPERATING CONDITIONS AND CHARACTERISTICS

Guaranteed with V_{EE} = −5.2 Vdc ± 5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10470-25 Min	MCM10470-25 Max	MCM10470-15 Min	MCM10470-15 Max	Unit	Conditions
Read Mode							See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	—	10	—	8.0	ns	Measured at 50% of input to 50%
Chip Select Recovery Time	t_{RCS}	—	10	—	8.0	ns	of output.
Address Access Time	t_{AA}	—	25	—	15	ns	See Note 2.
Write Mode							See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	25	—	15	—	ns	t_{WSA} = 3.0 ns MCM10470-25 t_{WSA} = 3.0 ns MCM10470-15 Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	2.0	—	2.0	—	ns	
Data Hold Time After Write	t_{WHD}	2.0	—	2.0	—	ns	
Address Setup Time Prior to Write	t_{WSA}	3.0	—	3.0	—	ns	t_W = 25 ns MCM10470-25 t_W = 15 ns MCM10470-15
Address Hold Time After Write	t_{WHA}	2.0	—	2.0	—	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	—	2.0	—	ns	
Chip Select Hold Time After Write	t_{WHCS}	2.0	—	2.0	—	ns	
Write Disable Time	t_{WS}	—	10	—	8.0	ns	
Write Recovery Time	t_{WR}	—	10	—	8.0	ns	
Rise and Fall Time		Typical					Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	2.0				ns	
Capacitance		Typical					Measured with a pulse technique.
Input Lead Capacitance	C_{in}	3.0				pF	
Output Lead Capacitance	C_{out}	5.0				pF	

Notes:
(1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 2 – CHIP SELECT ACCESS TIME

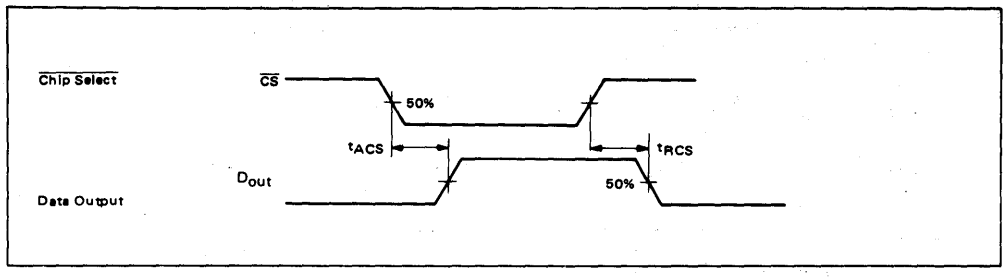


FIGURE 3 – ADDRESS ACCESS TIME

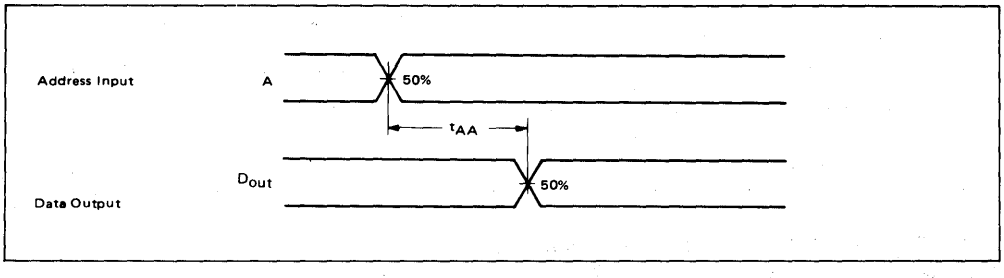
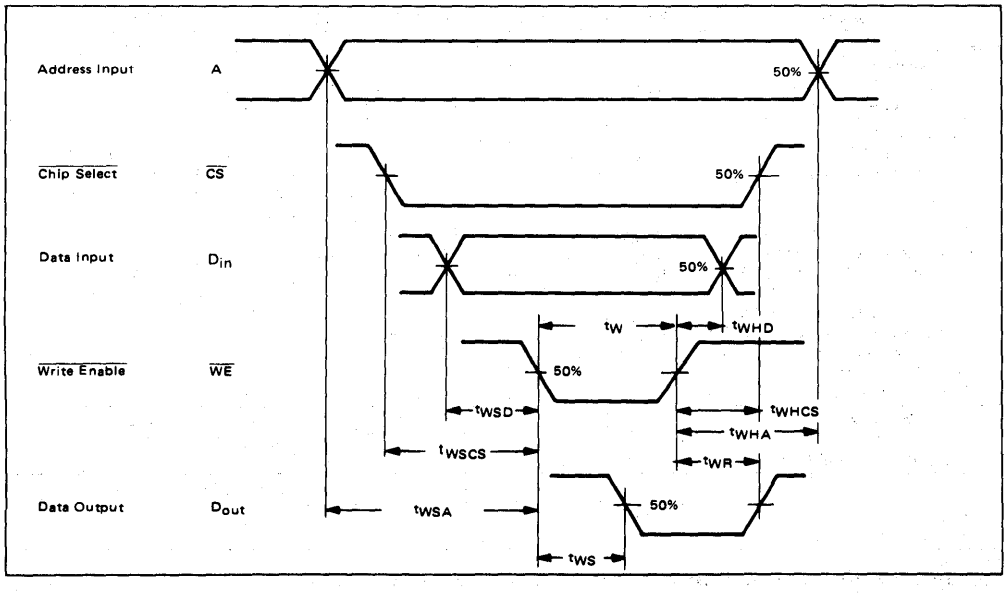


FIGURE 4 – WRITE STROBE MODE



MOTOROLA

MCM10474-15
MCM10474-25

Advance Information

1024 x 4-BIT RANDOM ACCESS MEMORY

The MCM10474 is a 4096-bit Read/Write RAM organized for 1024 words by 4 bits. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with 4 separate data-in lines, 4 noninverting data outputs, and an active-low chip select.

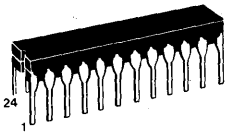
This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Fully Compatible with MECL 10K/10KH
- Pin-for-Pin Compatible with the Industry's Standard 10474
- Temperature Range of 0° to 75°C
- Emitter-Follower Output Permits Full Wire-ORing
- Power Dissipation Decreases with Increasing Temperature
- Address Access Time: MCM10474-25 25 ns (Max)
  MCM10474-15 15 ns (Max)
- Chip Select Access Time: MCM10474-25 10 ns (Max)
  MCM10474-15 8.0 ns (Max)

MECL

1024 x 4 BIT
RANDOM ACCESS MEMORY

L SUFFIX
CERAMIC PACKAGE
CASE 748-01



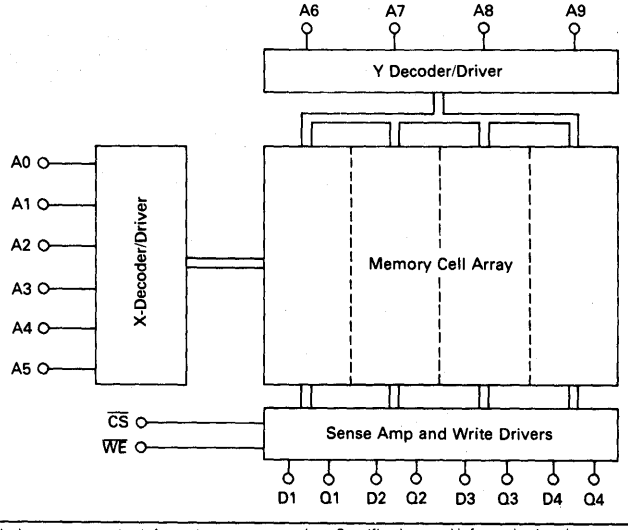
ORDERING INFORMATION
Suffix Denotes
MCM10474L15 — Ceramic Dual-in-Line Package
MCM10474L25 — Ceramic Dual-in-Line Package

MECL RAM

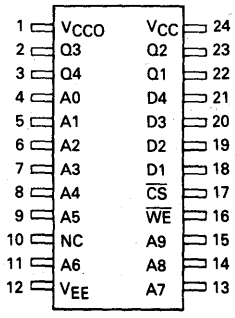
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current	I_O	<50	mAdc
Junction Operating Temperature	T_J	≤ 165	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESIGNATION

$\overline{CS}$	Chip Select
A0–A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
Q_{out}	Data Output

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	DO
Disabled	H	ϕ	ϕ	L

ϕ = Irrelevant

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL DESCRIPTION:

This device is a 1024 x 4-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, Q_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented noninverted at Q_{out}. (See Truth Table)

DC OPERATING CONDITIONS AND CHARACTERISTICS

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

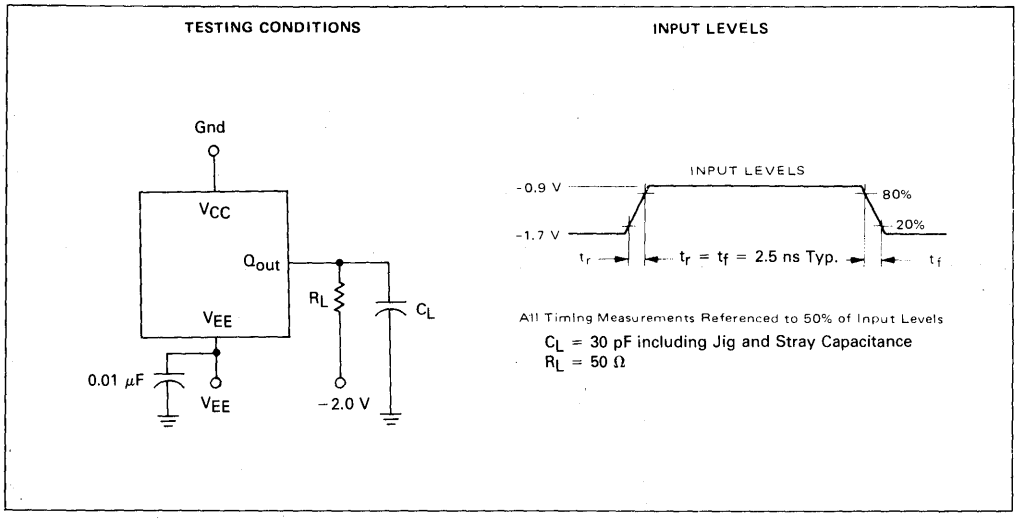
ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

		MCM10474 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	200	–	195	–	185	mAdc	All outputs and inputs open. Measure Pin 12.
Input Current High	I_{inH}	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. V_{in} $V_{IH(max)}$.
Input Current Low Chip Select	I_{inL}	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open.
Input Current Low*	I_{inL}	-50	–	-50	–	-50	–	μAdc	V_{in} $V_{IL(min)}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	-	-0.980	-	-0.920		Vdc	Threshold testing is performed and guaranteed on one input at a time. V_{in} = V_{IHA} or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

* Minimum limit equals the maximum negative current the driving circuitry will be required to sink.

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS



MECL RAM

AC OPERATING CONDITIONS AND CHARACTERISTICS

Guaranteed with V_{EE} = -5.2 Vdc ± 5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10474-25 Min	MCM10474-25 Max	MCM10474-15 Min	MCM10474-15 Max	Unit	Conditions
Read Mode							See Figures 2 and 3. Measured at 50% of input to 50% of output.
Chip Select Access Time	t_{ACS}	—	10	—	8.0	ns	
Chip Select Recovery Time	t_{RCS}	—	10	—	8.0	ns	
Address Access Time	t_{AA}	—	25	—	15	ns	
Write Mode							See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	25	—	15	—	ns	t_{WSA} = 8.0 ns MCM10474-25 t_{WSA} = 3.0 ns MCM10474-15 Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	5.0	—	2.0	—	ns	t_W = 25 ns MCM10474-25
Data Hold Time After Write	t_{WHD}	5.0	—	2.0	—	ns	t_W = 15 ns MCM10474-15
Address Setup Time Prior to Write	t_{WSA}	8.0	—	3.0	—	ns	
Address Hold Time After Write	t_{WHA}	5.0	—	2.0	—	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	—	2.0	—	ns	
Chip Select Hold Time After Write	t_{WHCS}	5.0	—	2.0	—	ns	
Write Disable Time	t_{WS}	—	10	—	8.0	ns	
Write Recovery Time	t_{WR}	—	15	—	8.0	ns	
Rise and Fall Time Output Rise and Fall Time	t_r, t_f	Typical 2.5				ns	Measured between 20% and 80% points.
Capacitance		Typical					Measured with a pulse technique.
Input Lead Capacitance	C_{in}	4.0				pF	
Output Lead Capacitance	C_{out}	7.0				pF	

Notes:
(1) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(2) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 2 — CHIP SELECT ACCESS TIME

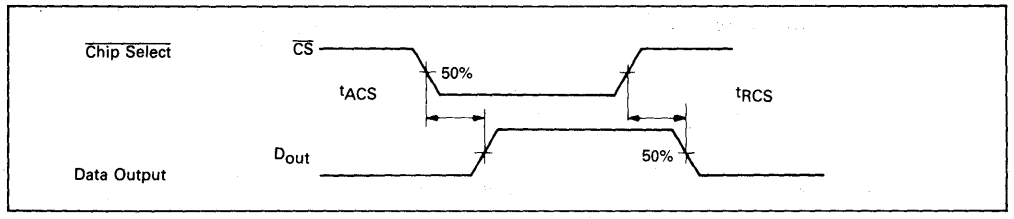


FIGURE 3 — ADDRESS ACCESS TIME

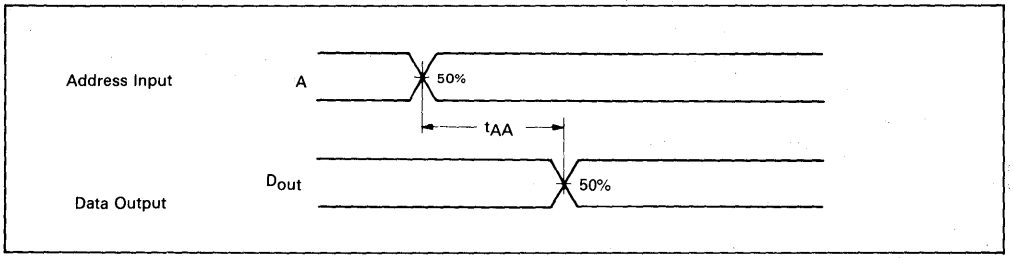
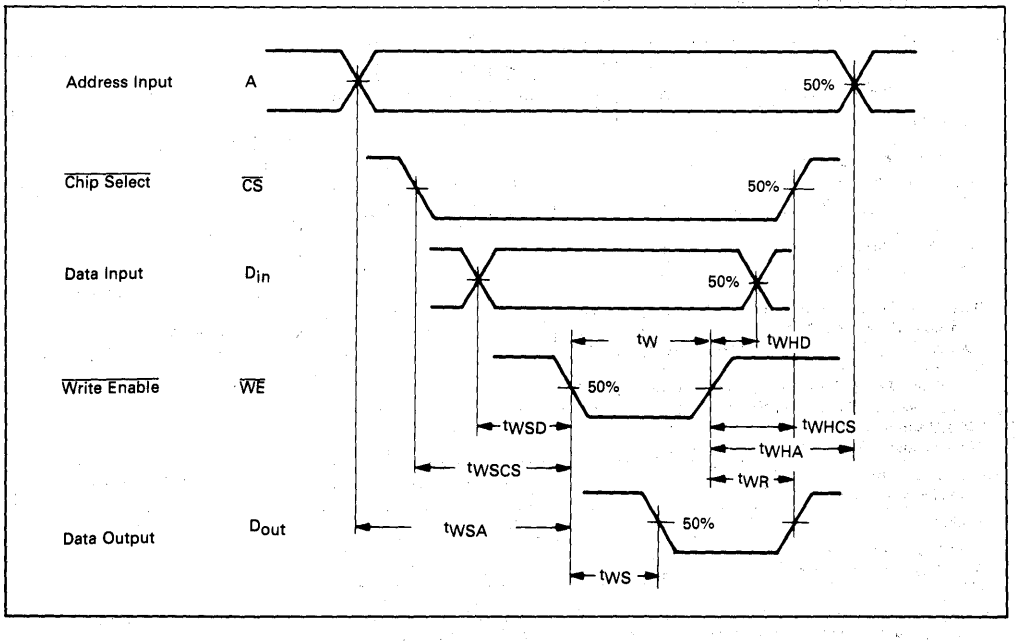
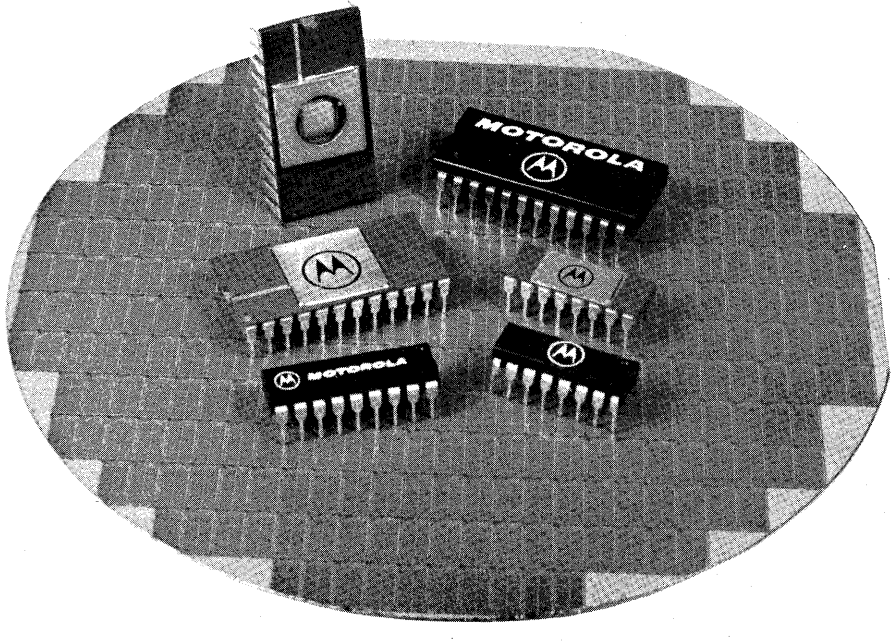


FIGURE 4 — WRITE STROBE MODE



MECL PROMs



MOTOROLA

MCM10147

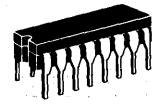
MECL

128-BIT RANDOM ACCESS MEMORY

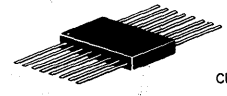
128 x 1-BIT RANDOM ACCESS MEMORY

The MCM10147 is a 128-word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of a 7-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 2 active-low chip select lines. It has a typical access time of 10 ns and is designed for high-speed scratch pads, control, cache, and buffer storage applications.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 5.0 ns
- Operating Temperature Range = 0^{o} to $+75^{o}C$
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family
- Similar to F10405.



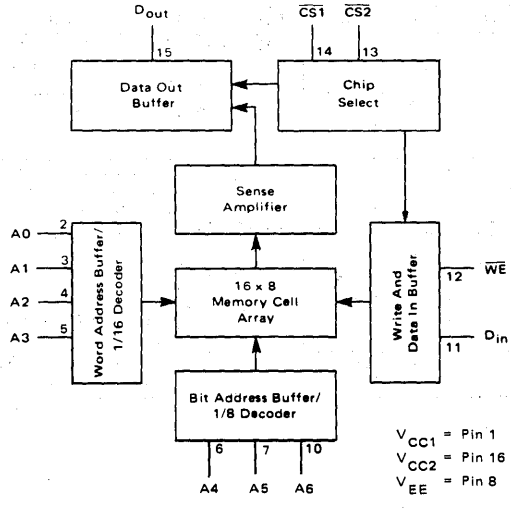
L SUFFIX
CERAMIC PACKAGE
CASE 620



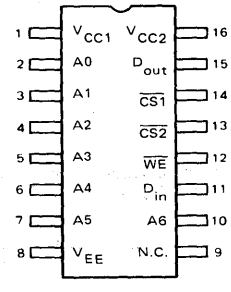
F SUFFIX
CERAMIC PACKAGE
CASE 650

MECL PROM

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A6	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2}$ ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM 10147 is a 128 word x 1-bit RAM. Bit selection is achieved by means of a 7-bit address A0 thru A6.

The active-low chip select allows memory expansion up to 512 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		MCM10144 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	105	–	100	–	95	mAdc	Typ I_{EE} @ 25°C = 80 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

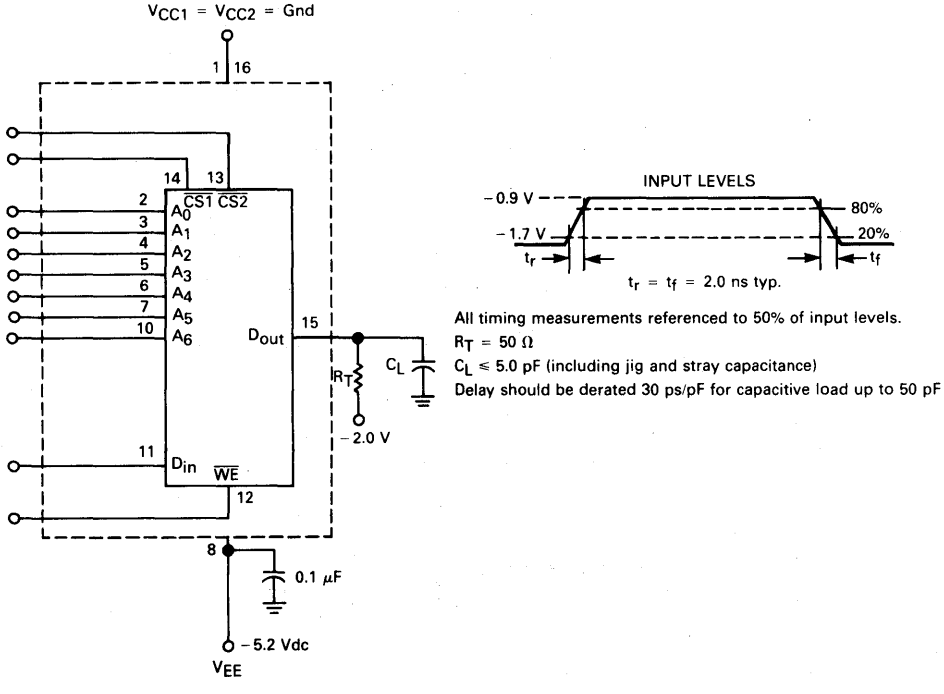
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	5.0	8.0	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	5.0	8.0	ns	output. See Note 2.
Address Access Time	t_{AA}	5.0	10	15	ns	
Write Mode						
Write Pulse Width	t_W	8.0	6.0	–	ns	t_{WSA} = 4.0 ns
Data Setup Time Prior to Write	t_{WSD}	1.0	-5.0	–	ns	
Data Hold Time After Write	t_{WHD}	3.0	-2.0	–	ns	
Address Setup Time Prior to Write	t_{WSA}	4.0	0	–	ns	t_W = 8.0 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	3.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	1.0	-5.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	1.0	-5.0	–	ns	
Write Disable Time	t_{WS}	2.0	5.0	8.0	ns	Measured at 50% of input to 50%
Write Recovery Time	t_{WR}	2.0	5.0	8.0	ns	of output.
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

MECL PROM

FIGURE 1 — SWITCHING TIME TEST CIRCUIT



All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF

FIGURE 2 – CHIP SELECT ACCESS TIME

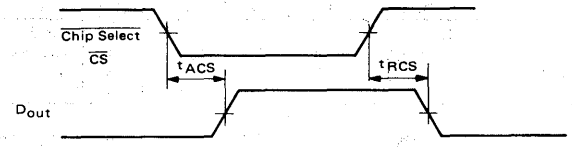


FIGURE 3 – ADDRESS ACCESS TIME

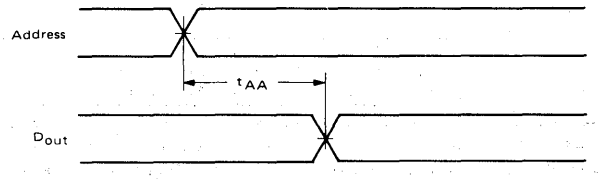
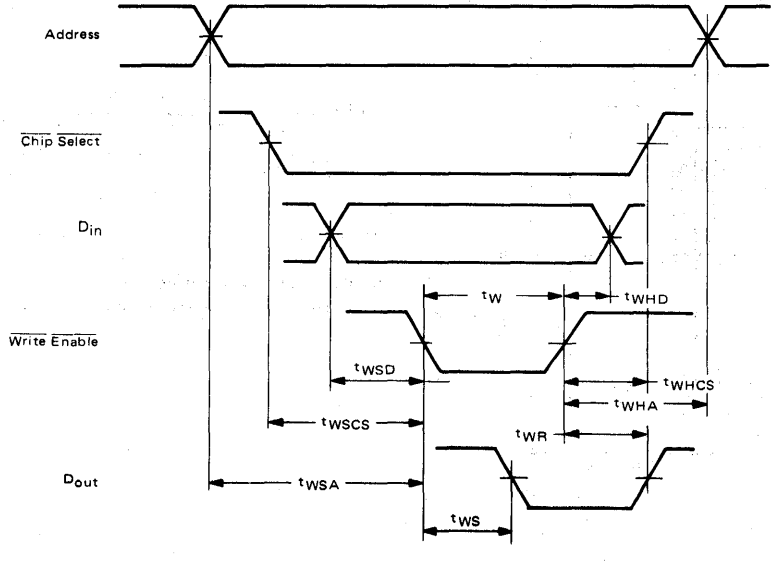


FIGURE 4 – WRITE MODE



MOTOROLA

MCM10139

MECL

32 X 8 BIT PROGRAMMABLE READ-ONLY MEMORY

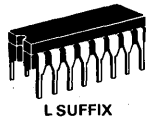
256-BIT PROGRAMMABLE READ ONLY MEMORY (PROM)

The MCM10139 is a 256-bit programmable read only memory (PROM). The circuit is organized as 32 words of 8 bits. Prior to programming, all stored bits are at logic 0 (low) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The MCM10139 has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

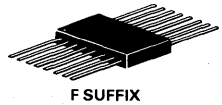
The MCM10139 is fully compatible with the MECL 10,000 logic family. It is designed for use in microprogramming, code conversion, logic simulation, and look-up table storage.

P_D = 520 mW typ/pkg (No Load)

t_{Access} = 15 ns typ (Address Inputs)



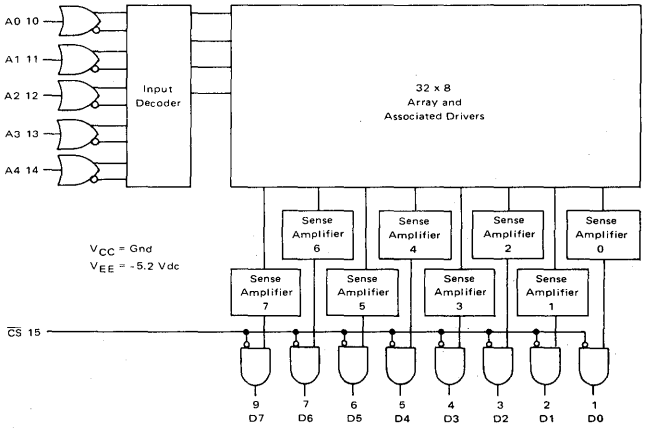
L SUFFIX
CERAMIC PACKAGE
CASE 620



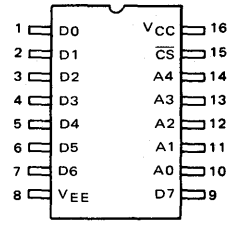
F SUFFIX
CERAMIC PACKAGE
CASE 650

MECL PROM

LOGIC DIAGRAM



PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	<50 <100	mAdc
Junction Operating Temperature	T_J	<165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

ELECTRICAL CHARACTERISTICS

	DC Test Voltage Values (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

MECL PROM

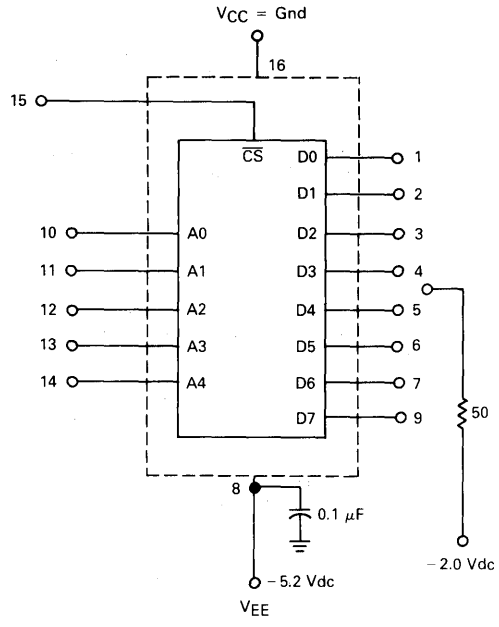
		MCM10139 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	150	–	145	–	140	mAdc	Typ I_{EE} @ 25°C = 100 mA. All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	265	–	265	–	265	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V.
Logic "0" Output Voltage	V_{OL}	-2.010	-1.665	-1.990	-1.650	-1.970	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	$V_{in} = V_{ILH}$ or V_{ILA}. Load 50 Ω to -2.0 V.

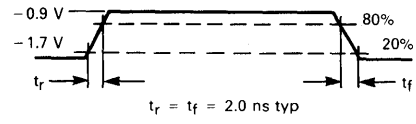
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load—See Figure 1 and Note 1)

		Test Limits				
Characteristic	Symbol	Min	Typ	Max	Unit	Conditions
Chip Select Access Time	t_{ACS}	–	10	15	ns	See Figures 2 and 3.
Chip Select Recovery Time	t_{RCS}	–	10	15	ns	Measured from 50% of input to 50%
Address Access Time	t_{AA}	–	15	20	ns	of output. See Note 2.
Output Rise and Fall Time	t_r, t_f	–	3.0	–	ns	Measured between 20% and 80% points.
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

Notes: 1. Contact your Motorola Sales Representative for details if extended temperature operation is desired.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the memory.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





$t_r = t_f = 2.0$ ns typ

All timing measurements referenced to 50% of input levels.
All outputs loaded 50 ohms to – 2.0 Vdc.

MECL PROM

FIGURE 2 – CHIP SELECT ACCESS TIME

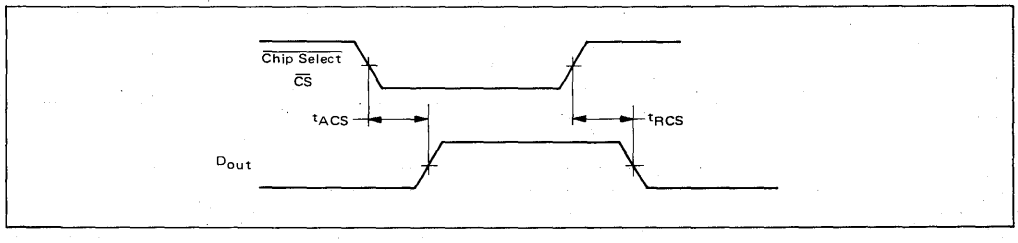
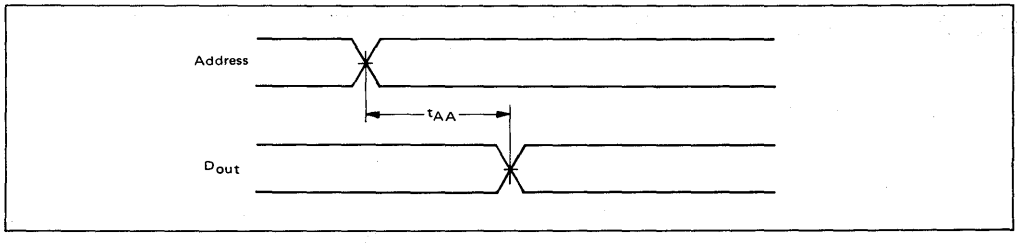


FIGURE 3 – ADDRESS ACCESS TIME



RECOMMENDED PROGRAMMING PROCEDURE*

The MCM10139 is shipped with all bits at logical "0" (low). To write logical "1s", proceed as follows.

MANUAL (See Figure 4)

Step 1 Connect V_{EE} (Pin 8) to -5.2 V and V_{CC} (Pin 16) to 0.0 V. Address the word to be programmed by applying -1.2 to -0.6 volts for a logic "1" and -5.2 to -4.2 volts for a logic "0" to the appropriate address inputs.

Step 2 Raise V_{CC} (Pin 16) to +6.8 volts.

Step 3 After V_{CC} has stabilized at +6.8 volts (including any ringing which may be present on the V_{CC} line), apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

Step 4 Return V_{CC} to 0.0 Volts.

CAUTION

To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at +6.8 volts for more than 1 second.

Step 5 Verify that the selected bit has programmed by connecting a 460 Ω resistor to -5.2 volts and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once. During verification V_{IH} should be -1.0 to -0.6 volts.

Step 6 If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (See Figure 5)

Step 1 Connect V_{EE} (Pin 8) to -5.2 volts and V_{CC} (Pin 16) to 0.0 volts. Apply the proper address data and raise V_{CC} (Pin 16) to +6.8 volts.

Step 2 After a minimum delay of 100 μs and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed ($0.1 \leq PW \leq 1$ ms).

Step 3 Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time. The delay between output programming pulses should be equal to or less than 1.0 ms.)

Step 4 After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at +6.8 volts during the entire programming time.

Step 5 After stepping through all address words, return V_{CC} to 0.0 volts and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once. During verification V_{IH} should be -1.0 to -0.6 volts.

*NOTE: For devices that program incorrectly—return serialized units with individual truth tables. Noncompliance voids warranty.

MECL PROM

PROGRAMMING SPECIFICATIONS

Characteristic	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
Power Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	Vdc	
To Program	V_{CCP}	+6.04	+6.8	+7.56	Vdc	
To Verify	V_{CCV}	0	0	0	Vdc	
Programming Supply Current	I_{CCP}	–	200	600	mA	V_{CC} = +6.8 Vdc
Address Voltage	V_{IH} Program	-1.2	–	-0.6	Vdc	
Logical "1"	V_{IH} Verify	-1.0	–	-0.6	Vdc	
Logical "0"	V_{IL}	-5.2	–	-4.2	Vdc	
Maximum Time at $V_{CC} = V_{CCP}$	–	–	–	1.0	sec	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mAdc	
Output Program Pulse Width	t_p	0.5	–	1.0	ms	
Output Pulse Rise Time	–	–	–	10	μs	
Programming Pulse Delay (1)						
Following V_{CC} change	t_d	0.1	–	1.0	ms	
Between Output Pulses	t_{d1}	0.01	–	1.0	ms	

NOTE 1. Maximum is specified to minimize the amount of time V_{CC} is at +6.8 volts.

FIGURE 4 – MANUAL PROGRAMMING CIRCUIT

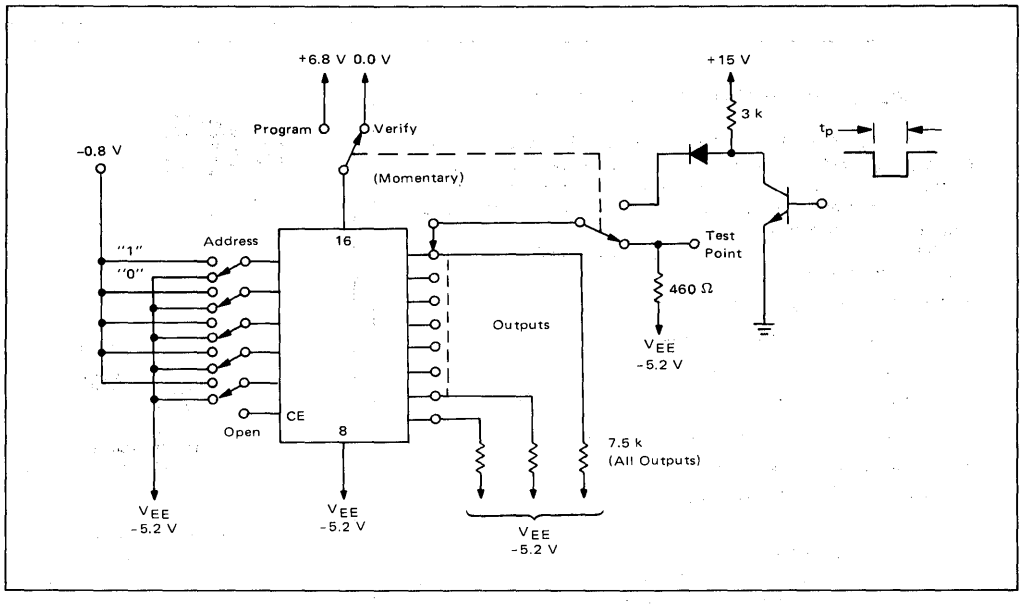
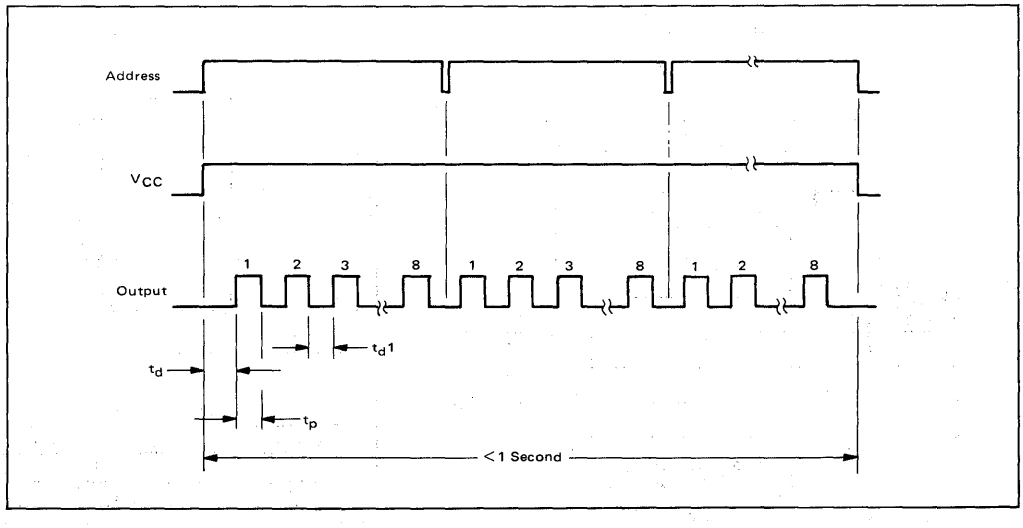


FIGURE 5 – AUTOMATIC PROGRAMMING CIRCUIT



MECL PROM

MOTOROLA

MCM10146

1024 x 1-BIT RANDOM ACCESS MEMORY

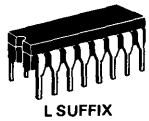
The MCM10146/10415 is a 1024-bit Read/Write Random Access Memory organized 1024 words by 1 bit. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with a separate data in line, a non-inverting data output, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

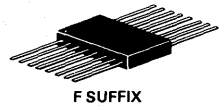
- Fully Compatible with MECL 10,000
- Pin-for-Pin Compatible with the 10415
- Temperature Range of 0° to 75°C (see note 1)
- Emitter-Follower Output Permits Full Wire-ORing (see note 3)
- Power Dissipation Decreases with Increasing Temperature
- Typical Address Access of 24 ns
- Typical Chip Select Access of 4.0 ns

PIN DESIGNATION

CS	Chip Select Input
A0 to A9	Address Inputs
D_{in}	Data Inputs
D_{out}	Data Output
WE	Write Enable Input



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

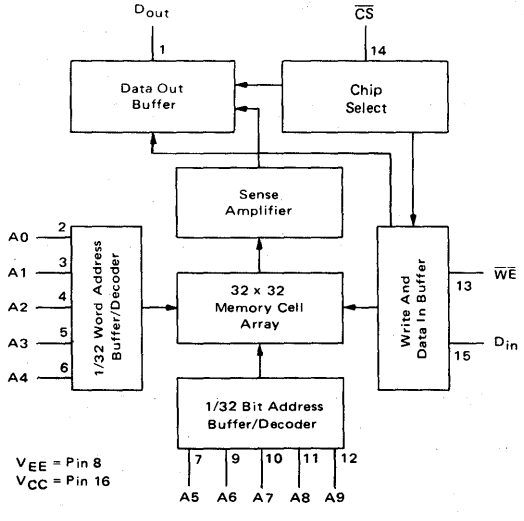
ORDERING INFORMATION

Suffix Denotes

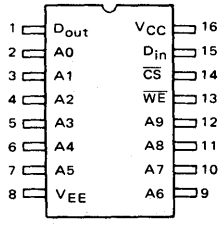
MCM10146 – L Ceramic Dual-In-Line Package
– F Ceramic Flat Package

10415 – DC Ceramic Dual-in-Line Package
– FC Ceramic Flat Package

BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

This device is a 1024 x 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM (CS input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out}. (See Truth Table)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

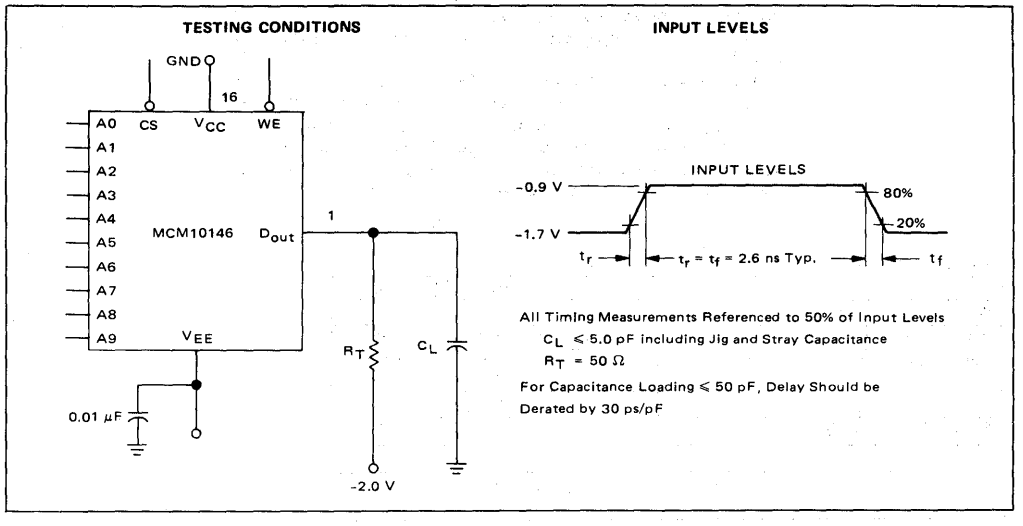
MECL PROM

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		MCM10146 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	150	–	145	–	125	mAdc	Typ I_{EE} @ 25°C = 100 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.920	-1.665	-1.900	-1.650	-1.880	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS



MECL PROM

Guaranteed with V_{EE} = -5.2 Vdc ± 5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10146 Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	7.0	ns	Measured at 50% of input to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	4.0	7.0	ns	See Note 2.
Address Access Time	t_{AA}	8.0	24	29	ns	
Write Mode						See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	25	20	–	ns	t_{WSA} = 8.0 ns. Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	5.0	0	–	ns	
Data Hold Time After Write	t_{WHD}	5.0	0	–	ns	
Address Setup Time Prior to Write	t_{WSA}	8.0	0	–	ns	t_W = 25 ns
Address Hold Time After Write	t_{WHA}	2.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	5.0	0	–	ns	
Write Disable Time	t_{WS}	2.8	5.0	7.0	ns	
Write Recovery Time	t_{WR}	2.8	5.0	7.0	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	2.5	4.0	ns	When driven from $\overline{CS}$ or $\overline{WE}$ inputs.
Output Rise and Fall Time	t_r, t_f	1.5	4.0	8.0	ns	When driven from Address inputs.
Capacitance						Measured with a pulse technique.
Input Lead Capacitance	C_{in}	–	4.0	5.0	pF	
Output Lead Capacitance	C_{out}	–	7.0	8.0	pF	

Notes:

(1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.

(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

(4) Typical limits are at V_{EE} = -5.2 Vdc, T_A = 25°C and standard loading.

FIGURE 2 – CHIP SELECT ACCESS TIME

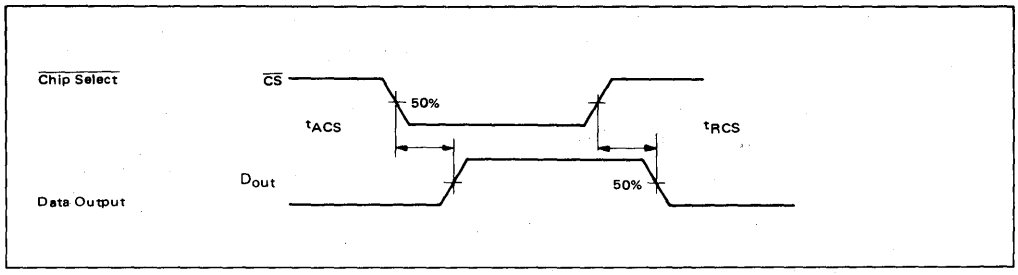


FIGURE 3 – ADDRESS ACCESS TIME

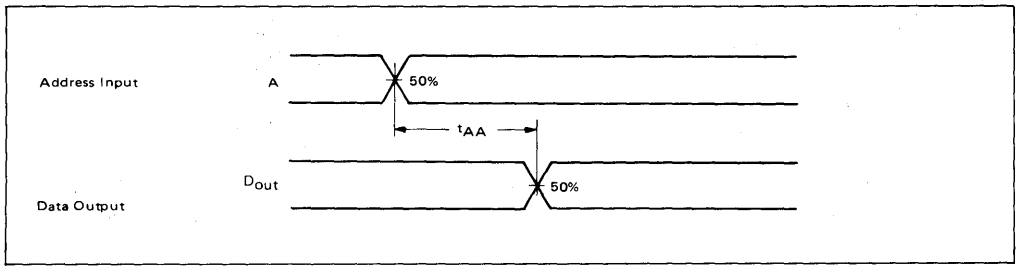
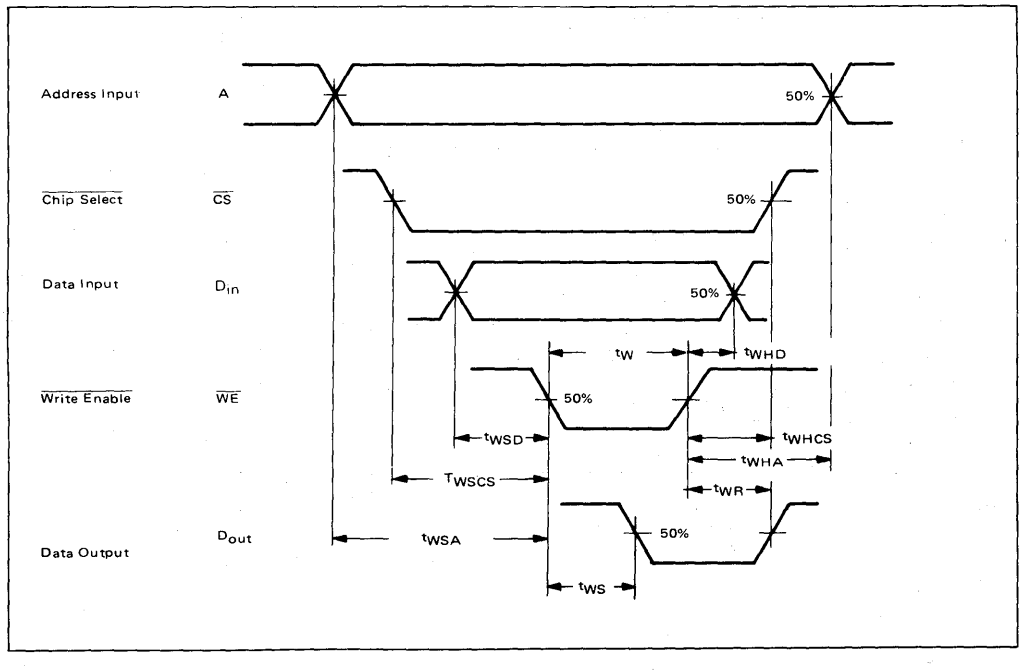


FIGURE 4 – WRITE STROBE MODE



MECL PROM

MOTOROLA

MCM10149

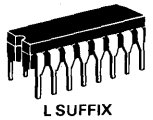
256 x 4-BIT PROGRAMMABLE READ-ONLY MEMORY

This device is a 256-word x 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

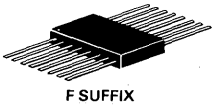
- Typical Address Access Time of 20 ns
- Typical Chip Select Access Timeof 8.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (540 mW typ @25°C)
  Decreases with Increasing Temperature

MECL

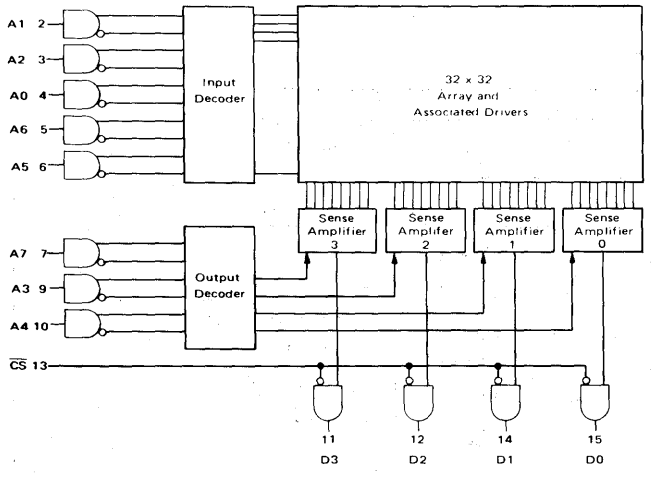
1024-BIT PROGRAMMABLE READ-ONLY MEMORY



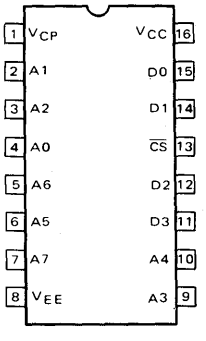
L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650



PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	160	–	155	–	150	–	145	–	145	mAdc
Input Current High	I_{inH}	–	450	–	265	–	265	–	265	–	265	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

Forcing Function	Parameter	-55°C ①	0°C ②	25°C ②	25°C ①	75°C ②	125°C ①
		MCM10500	MCM10100	MCM10100	MCM10500	MCM10100	MCM10500
V_{IHmax} =	V_{OHmax}	−0.880	−0.840	−0.810	−0.780	−0.720	−0.630
	V_{OHmin}	−1.080	−1.000	−0.960	−0.930	−0.900	−0.825
	V_{OHAmin}	−1.100	−1.020	−0.980	−0.950	−0.920	−0.845
V_{IHAmin}		−1.175	−1.130	−1.105	−1.105	−1.045	−1.000
V_{ILAmax}		−1.510	−1.490	−1.475	−1.475	−1.450	−1.400
	V_{OLAmax}	−1.635	−1.645	−1.630	−1.600	−1.605	−1.525
	V_{OLmax}	−1.655	−1.665	−1.650	−1.620	−1.625	−1.545
V_{ILmin} =	V_{OLmin}	−1.920	−1.870	−1.850	−1.850	−1.830	−1.820
V_{ILmin}	I_{NLmin}	0.5	0.5	0.5	0.5	0.3	0.3

NOTES: ① MCM10500 series specified driving 100Ω to −2.0 V.
② Memories (MCM10100) specified 0 - 75°C for commercial temperature range, 50Ω to -2.0V.
Military temperature range memories (MCM10500) specified per Note 1.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10149 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ± 5%		MCM10549 T_A = -55 to +125°C, V_{EE} = -5.2 Vdc ± 5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 1.
Chip Select Access Time	t_{ACS}	2.0	10	*	*		
Chip Select Recovery Time	t_{RCS}	2.0	10	*	*		
Address Access Time	t_{AA}	7.0	25	*	*		
Rise and Fall Time	t_r, t_f	1.5	7.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	5.0		
Output Capacitance	C_{out}	–	8.0	–	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10149; 100 Ω, MCM10549.
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
4. V_{CP} = V_{CC} = Gnd for normal operation.

*To be determined; contact your Motorola representative for up-to-date information.

PROGRAMMING THE MCM10149 †

During programming of the MCM 10149, input pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input pins 2, 3, 4, 5, and 6 are addressed with $0 V \leq V_{IH} \leq +0.25$ V and $V_{EE} \leq V_{IL} \leq -3.0$ V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with V_{CP} = V_{CC} = 0 V and V_{EE} = − 5.2 V ± 5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to + 12 V ± 0.5 V (total voltage V_{CP} to V_{EE} is now 17.2 V, + 12 V − [− 5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1 − 10 μs range, while its pulse width (t_{W1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at + 12 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be

MECL PROM

set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of -5.2 V ± 5%.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresponding output pin to a voltage of + 2.85 V ± 5%. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor (100 ohm for MCM 10549) to -2.0 V. Current into the selected output is 5 mA maximum.

After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. It pulse width should be greater than 100 μs. Pulse magnitude is 50 mA ± 5.0 mA. The voltage clamp on this current source is to be -6.0 V.

After the fusing current source has returned 0 mA, the bit select pulse is returned to it initial level, i.e., the output is returned through its load to -2.0 V. Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Non compliance voids warranty.

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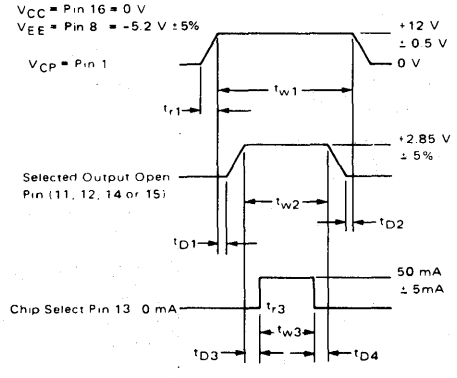
PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149.



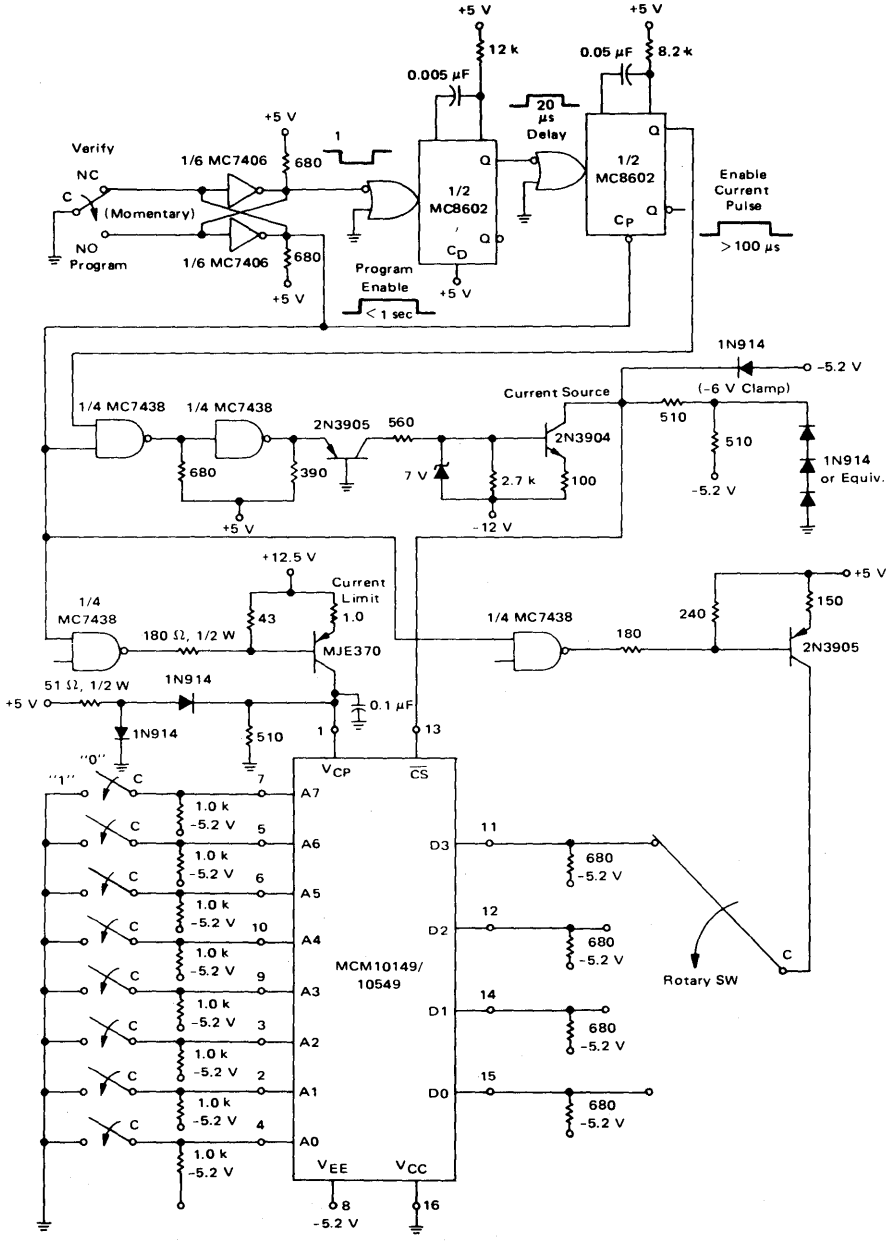
The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., V_{CP} = 0 V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of ≤ 15% is to be observed.

Definitions and values of timing symbols are as follows.

Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	≥ 1 μs
t_{w1}	Pulse Width, Programming Voltage	≥ 100 μs < 1 ms
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	≥ 0
t_{w2}	Pulse Width, Bit Select	≥ 100 μs
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	≥ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	≥ 1 μs
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	≥ 100 μs
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	≥ 1 μs

MANUAL PROGRAMMING CIRCUIT



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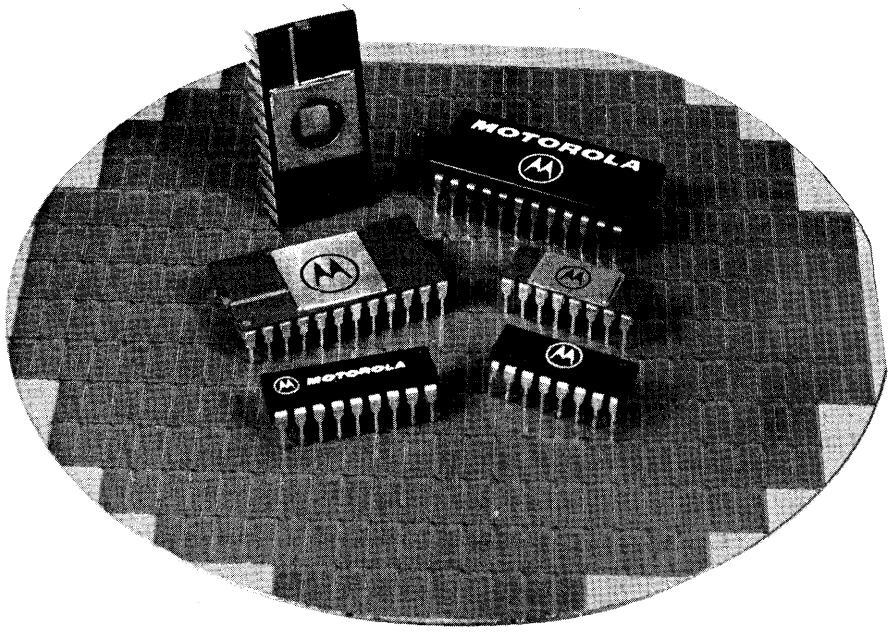


Bubble Memories and Associated Products

MOTOROLA

MBM2256

Advance Information

256 K x 1-BIT MAGNETIC BUBBLE MEMORY DEVICE

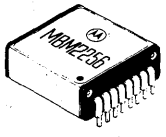
GENERAL DESCRIPTION

The MBM2256 is a 262,144 (2^{18}) bit magnetic bubble memory device. All required magnetic components including the permanent magnets, the drive field coils and protective magnetic shield are integral parts of the device. The package is a 1.15 x 1.1 x 0.36 inch 16-pin DIP.

The MBM2256 features a dual block-replicate organization with swap gates on the input track. Data storage is organized as 256 storage loops of 1024-bits each. Additional loops are provided to store the error correction code and as redundant loops. In one of two dedicated map loops on-chip the redundant map loop data is stored.

The MBM2256 can be operated synchronously or asynchronously. Average access time to a page of data is less than 7.0 ms at 100 kHz. Data transfer rate is 125 kilobits per second at 125 kHz. Average power dissipation at 125 kHz is 0.8 Watts. The device will operate over a case temperature range of 0°C to 70°C, and data is retained without power from −40°C to 100°C.

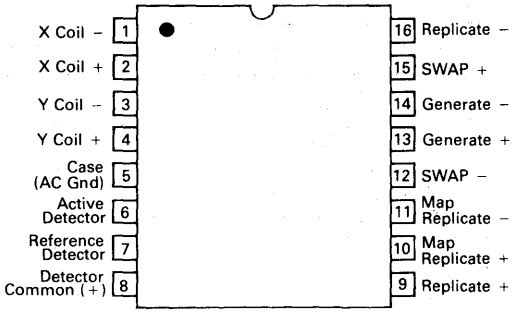
The device is fabricated using a pseudo-planar process to improve operating margins as well as to enhance reliability. The use of CrCuCr in the conductor elements ensures excellent conductivity while greatly increasing resistance to problems associated with electromigration.



FEATURES

- Non-volatile
- High Density
- Solid State
- Low Power
- Start/Stop Capability
- Page-Oriented Access
- On-Chip Redundant Loop Map
- Swap Gates
- Block Replicate
- Error Correction Code Storage
- 16-Pin Dual-in-Line Package

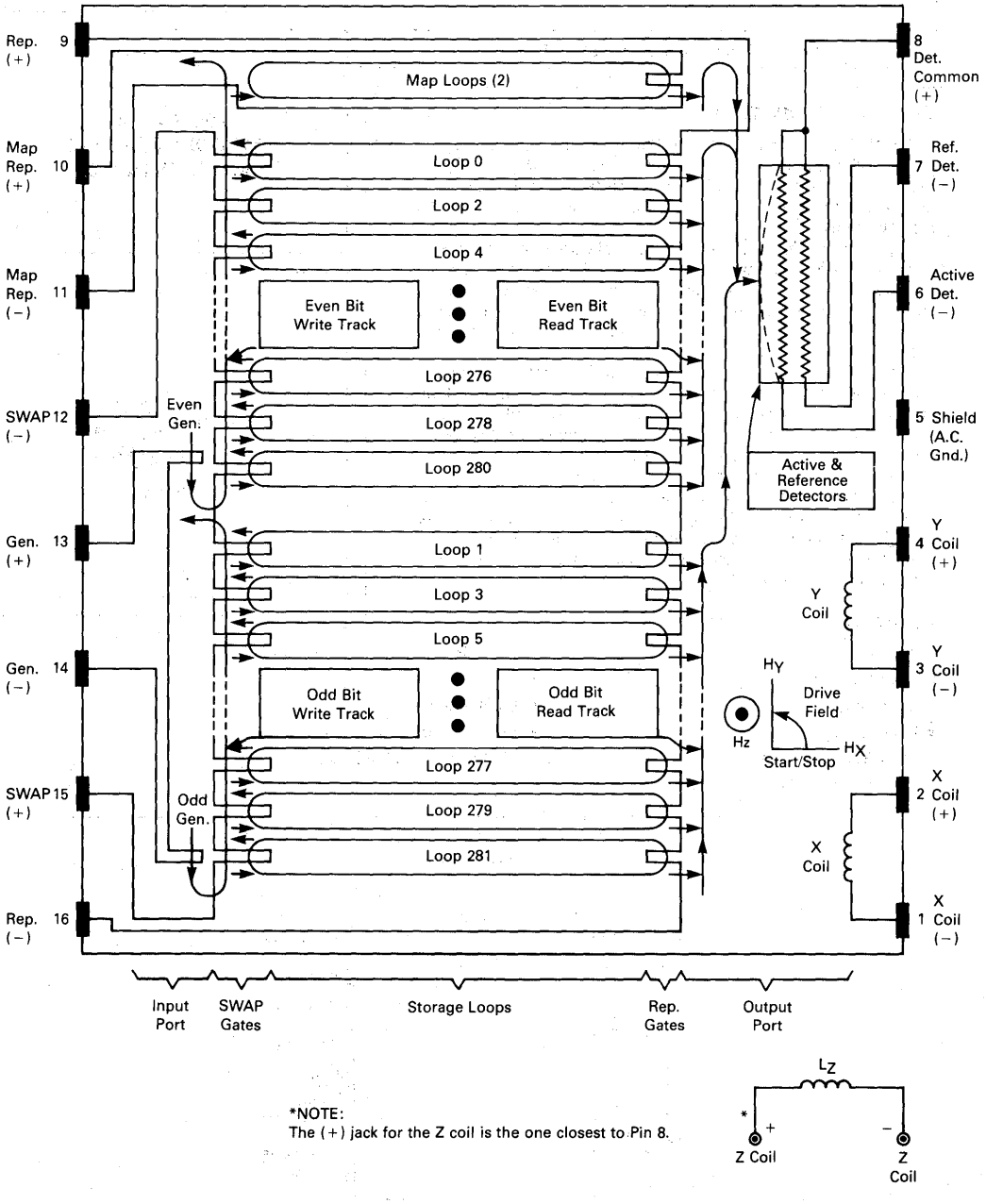
Pin Assignment



This document contains information on a new product. Specifications and information herein are subject to change without notice.

Bubble

FIGURE 1 — BLOCK DIAGRAM



*NOTE:
The (+) jack for the Z coil is the one closest to Pin 8.

Bubble

ABSOLUTE MAXIMUM RATINGS

Rating	Min	Max	Unit
Operating Temperature (Case) (T_C)	0	70	°C
Non-Volatile Storage Temperature	−40	100	°C
Storage Temperature	−40	120	°C
External Magnetic Field	—	20	Oe
Peak Current In X Coil*	—	900	mA
Peak Current In Y Coil*	—	1,100	mA
Peak Current In Z Coil*	—	3,000	mAdc
Peak Replicate Current	—	40	mAdc
Peak Generate Current	—	40	mAdc
Peak Swap Current	—	30	mAdc
Peak Detector Current	—	6.0	mAdc
Maximum Coil Disturb Current With Data Retention	—	10	mA
Maximum Pin To Pin Voltage	—	55	Volts

*These peak currents are allowed subject to the device temperature not exceeding the temperature limits.

ELECTRICAL CHARACTERISTICS (T_C = 0°C to 70°C, rotating field frequency (f_o) = 125 kHz unless otherwise noted).

FUNCTION CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Generate Current	I_G	180	—	220	mA
Swap Current	I_S	25	—	31	mA
Replicate Cut Current	I_{RC}	75	—	95	mA
Replicate Transfer Current	I_{RT}	28	—	42	mA
Map Replicate Cut Current	I_{RCM}	75	—	95	mA
Map Replicate Transfer Current	I_{RTM}	28	—	42	mA
Map Transfer In Current	I_{TM}	−24	—	−30	mA
Detector Current	I_{DA}, I_{DR}	—	5.0	5.8	mA

X,Y COIL DRIVE (See Figure 2.)

Parameter	Symbol	Min	Typ	Max	Unit
Coil Driver Supply Voltage	V_x, V_y	11.4	12	12.6	V
Coil Driver Switch On Resistance (2 Switches In Series)	R_{on}	0.7	—	1.8	Ohms
Coil Driver Clamp Diode Drop (2 Diodes In Series)	V_{clamp}	—	—	1.6	V
X Coil Peak Current (L_x = nom, V_x = nom, R_{on}, V_{clamp} = nom)	I_{XP}	—	630	—	mA
Y Coil Peak Current (L_y = nom, V_y = nom) (R_{on}, V_{clamp} = nom)	I_{YP}	—	770	—	mA
Coil Current Offset	I_{xo}, I_{yo}	−10	—	+10	
Stop Current Overshoot	I_{so}	—	—	+10 −0	
Total Coil Power	P_c	—	—		

Z COIL DRIVE

Z Coil Sensitivity		—	2
Z Coil Current Simultaneously Erase All Data Stored (Rotating Field On) (Rotating Field Off)	I_{zap}	2.0 3	
Duration of Erase Current	t_{ZAP}		

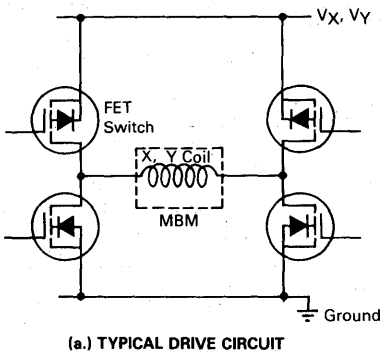
SCOPE

This specification describes the magnetic, electrical, mechanical and environmental parameters of the 256K bit magnetic bubble device, MBM2256, as manufactured by Motorola Inc.

DEVICE ORGANIZATION

The 256K bit bubble memory chip uses a block-replicate organization with true swap gates on the input track. The storage area is arranged as 256 storage loops each with 1,024 bit locations. Additional loops are provided for error correction (6) and defect tolerance (20) giving a total of 282 loops. Data is written and read at the clock frequency which is the rotating field frequency. Figure 1 is a schematic diagram of the 256K bit chip.

FIGURE 2 — X, Y COIL DRIVE



(a.) TYPICAL DRIVE CIRCUIT

Data Input

The device is organized into two halves — odd and even. To write into the device the same data pattern is written simultaneously into both the odd and even input tracks. Due to the spacing between minor loops only alternate bits can be aligned with adjacent minor loops. An extra bit propagation delay on the odd input track causes odd bits to align with odd loops and even bits with even loops such that the correct bit is written into each loop. The swap gate automatically clears the old data as new data is written into the loops.

Data Output

To read the data, one bit is replicated from each minor loop into the output track, again arranged as an odd and even half. The alternate bit data streams are then interleaved prior to entering the detector. The data is therefore written in and read out of the bubble device at the clock frequency although the data does divide and recombine within the chip.

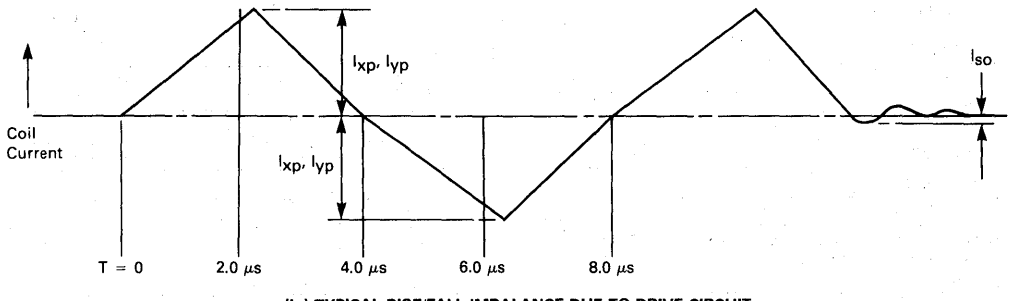
Redundancy

Of the 282 storage loops 256 are allocated for data, 6 for error correction and 20 for redundancy. These 20 loops are used to mask inoperable minor loops and improve performance. Twenty loops are always declared redundant. Data should not be written into the redundant loops.

Redundancy Map

In addition to the 282 storage loops the chip contains two map loops. These loops have their own transfer-in and replicate gates but share the generator and detector with the storage loops. Only one loop is required and is chosen at final test. The chosen loop is used to store the data which identifies the redundant loop map. A "one" designates a usable loop; a "zero" a non-usable loop. Preceding this map code is a stream of 64 "zeros" followed by a "one" and a "zero" which may be used to synchronize the external control circuitry with the memory. The map loop used for storage of the redundancy information is also identified in the code (see Coding of Redundancy Map). Since only alternate bit positions are written into the map loop to enhance reliability, intervening bits are always zero and are ignored during read (see Map Read Operation paragraph).

The redundancy map is also printed on the label of each device using hexadecimal format. Two digits are used per loop. Instead of providing the absolute loop number, the incremental difference between non-usable loops is printed. For example, if the first bad loop is #7, and the next two are 19 and 23, the sequence



(b.) TYPICAL RISE/FALL IMBALANCE DUE TO DRIVE CIRCUIT

Bubble

070C04 will be printed on the label. This format allows for an incremental difference between two non-usable loops of up to 255 (FF).

Coding of Redundancy Map (The map loop contains 512 bits of information in five fields.)

Pattern	Field	Number of Bits	Note
MM---MM	Map Data	282	(1)
EE---EE	Error Correction	12	(2)
LL	Loop	2	(3)
UU---UU	User	150	(4)
00---0010	Sync	66	(5)

NOTE:
(1) Each bit corresponds to a data loop in sequence
M = 1 identifies a usable loop (262).
M = 0 identifies a redundant loop (20).
(2) Error correction code used is a fire code applied only to the map data.
(3) Identifies which map loop contains the redundancy information
01 — loop #1, 10 — loop #2.
(4) This field may contain factory-pertinent information. It will not contain a duplicate of the sync pattern.
(5) The sync pattern is used to locate the beginning of the map data field and identifies data page zero.

Organizational Specifications

Bits/Loop	1,024
Total Data Loops	282
Usable Data Loops	262
Error Correction Loops	6
User Data Loops	256
Total User Storage	262,144 Bits
Map Loops	2

FUNCTIONAL DESCRIPTION

Write Data Operation

Writing data is accomplished by generating the new data with a series of pulses applied to pins 13 and 14, starting t_{PGSF} before the swap operation. As the device continues to cycle after all data is generated, the new data and the old will be aligned at the swap gates after t_{PGSL}. A swap pulse is applied to pins 12 and 15 at this time, swapping the new data in and the old data out. Unused bits from the even and odd sides along with the old data are propagated out and discarded beyond the active area.

Read Data Operation

To read data, the device must be cycled until the desired page is aligned with the replicate gates on the output side of the storage loops. A replicate cut pulse is applied to pins 9 and 16 to duplicate the page. This is immediately followed by a replicate transfer pulse which causes the duplicate bubbles to propagate into alternate positions on the two output tracks.

Propagation along the output tracks occurs during t_{PRD}. During this time, the odd and even output bits are merged.

Detection occurs when a bubble passes under the magnetoresistive detector element. The bubble's magnetic field causes the detector element to change resistance. By passing a constant current through the detector, this is converted to a voltage signal. A dummy detector which is not influenced by magnetic bubbles is used to cancel the background magnetoresistive signal.

Output bubbles are discarded beyond the active area after detection. A complete page is read in t_{PRDL}.

INTERFACE IMPEDANCES

Parameter	Symbol	Min	Typ	Max	Unit
Generate (1)	r_G	4.5	—	18	Ω
Swap (1)	r_S	180	—	540	Ω
Replicate (1)	r_R	130	—	320	Ω
Map Replicate (1) (Includes Map Transfer-In)	r_M	18	—	56	Ω
Detector (Active and Reference) (1)	r_{DS}, r_{DR}	950	—	2000	Ω
Detector Active/Reference Ratio	—	0.985	—	1.015	—
X Coil Inductance	L_x	34	—	37	μH
Y Coil Inductance	L_y	27	—	30	μH
Z Coil Inductance	L_z	25	—	35	μH
X Coil dc Resistance Non-operating, 25°C	r_x dc	—	2.7	—	Ω
Y Coil dc Resistance Non-operating, 25°C	r_y dc	—	1.1	—	Ω
Z Coil dc Resistance Non-operating, 25°C	r_z dc	—	0.75	—	Ω
X Coil ac Resistance (1)	r_x ac	2.5	—	4.0	Ω
Y Coil ac Resistance (1)	r_y ac	1.5	—	2.5	Ω

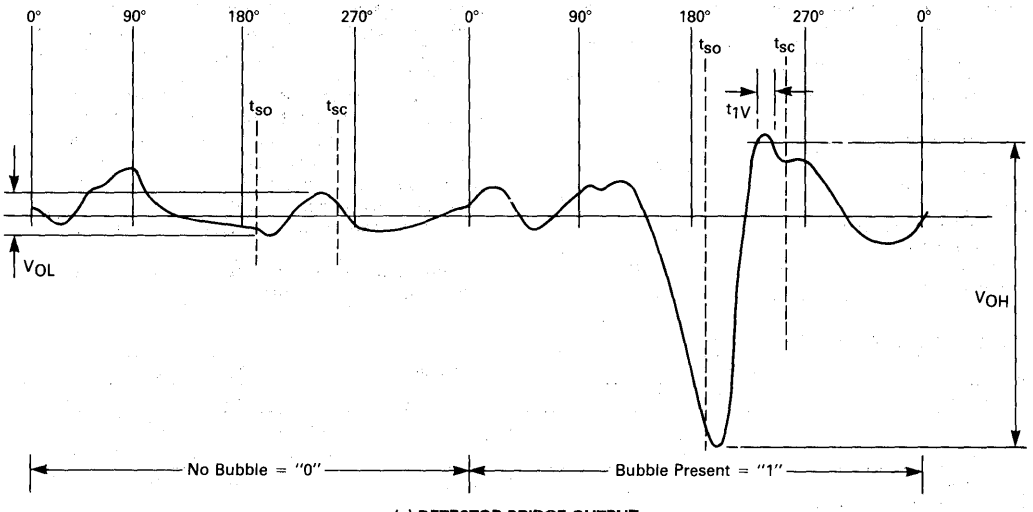
NOTE:
(1) Minimum value is at T_C = 0°C, device non-operating, maximum value is at T_C = 70°C, device operating.

OUTPUT SIGNALS (T_C = 0°C to 70°C, f_o = 125 kHz)

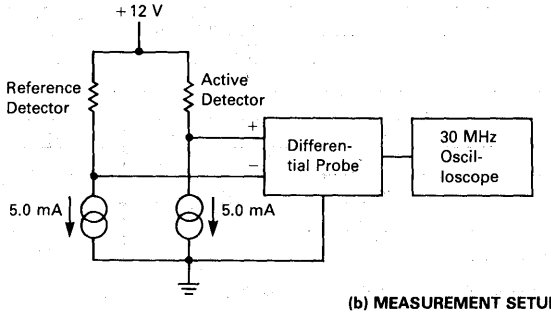
Parameter	Symbol	Min	Typ	Max	Unit
Common-Mode Output Signal (I_{DA} = I_{DR} = 5.0 mA) Differential Peak-to-Peak Output Voltage (1) (I_d = 5.0 mA. See Figure 1 for measurement details.)	V_{cm}	—	—	50	mV
Logic 1 (Bubble Present)	V_{OH}	TBD	—	—	mV
Logic 0 (No Bubble)	V_{OL}	—	—	TBD	mV
Signal Strobe Leading Edge Phase	t_{so}	—	191	—	Degrees
Signal Strobe Trailing Edge Phase	t_{sc}	—	258	—	Degrees
Logic 1 Valid Window	t_{1V}	50	—	—	ns

NOTE:
(1) V_{OH} is defined as the difference between the most negative and the most positive signal excursions which occur within the phase window t_{so} to t_{sc} when a bubble is being detected. V_{OL} is similarly defined for the case of no bubble being detected. See Figure 3.

FIGURE 3 —



(a) DETECTOR BRIDGE OUTPUT



Scope Input Impedance:
≥ 2M
≤ 5.0 pF

Common-Mode Rejection:
≥ 60 dB

Frequency Response:
≥ 5.0 MHz

(b) MEASUREMENT SETUP

Map Read Operation

To read the contents of the map, a series of alternate cycle replicate pulses, identical to data replicate pulses, is applied to pins 10 and 11. Data will be available after t_{PMRD}. Since map data is only loaded into alternate positions in the loop, one pass may result in no data. This procedure is then repeated after delaying one cycle. The outputs from the two map loops are merged, but only one loop contains data. See "Coding of Redundancy Map Loops" for decoding information.

Map Write Operation

Writing the map loop is accomplished by generating map information as normal data on alternate cycles. After t_{PGT1} or t_{PGT2}, pins 10 and 11 are pulsed with a series of negative map transfer pulses on alternate cycles. Selecting t_{PGT1} writes into map loop 1, selecting t_{PGT2} writes into map loop 2.

TIMING CHARACTERISTICS (T_C = 0°C, f_O = 125 kHz unless otherwise noted. See Figure 4 for test conditions).*

WRITE CYCLE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Generate First Bit to Swap In (1)	$t_{PGS(F)}$	—	294	—	Cycles
Generate Last Bit to Swap In (1)	$t_{PGS(L)}$	—	13	—	Cycles
Swap In to Replicate Out (1)	t_{PSR}	—	514	—	Cycles
Swap In to Non-Volatile Storage (2)	t_{PS}	—	2	—	Cycles
Generate Delay Time (3)	t_{DG}	70	—	120	Degrees
Generate Pulse Width (4)	t_{WG}	140	210	280	ns
Generate Fall Time (10%–90% of pk Amplitude)	t_{FG}	200	—	400	ns
Swap Delay Time (3)	t_{DS}	270	—	330	Degrees
Swap Pulse Width	t_{WS}	340	370	400	Degrees

READ CYCLE TIMING

Replicate Out to Detect First Bit (1)	$t_{PRD(F)}$	—	180	—	Cycles
Replicate Out to Detect Last Bit (1)	$t_{PRD(L)}$	—	461	—	Cycles
Replicate Out to Swap In (1)	t_{PRS}	—	510	—	Cycles
Replicate Delay Time (3)	t_{DR}	−10	—	20	Degrees
Replicate Cut Pulse Width	t_{WRC}	210	280	350	ns
Replicate Transfer Pulse Width	t_{WRT}	80	100	120	Degrees

MAP READ AND WRITE CYCLE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Map Replicate to Detect	t_{PMRD}	—	188	—	Cycles
Generate to Map Loop #1 Transfer	T_{PGT1}	—	308	—	Cycles
Generate to Map Loop #2 Transfer	t_{PGT2}	—	305	—	Cycles
Map Loop Transfer-In to Replicate	t_{PTR}	—	516	—	Cycles
Map Replicate Delay Time (3)	t_{DRM}	−10	—	20	Degrees
Map Replicate Cut Pulse Width	t_{WRCM}	210	280	350	ns
Map Replicate Transfer Pulse Width	t_{WRTM}	80	100	120	Degrees
Map Transfer-In Delay Time	t_{DTM}	270	—	330	Degrees
Map Transfer-In Pulse Width	t_{WTM}	200	220	240	Degrees

NOTES:

* All pulses to have rise and fall times ≤ 80 ns (10%–90% of peak amplitude) unless otherwise noted.

(1) Propagation times are defined from the beginning of the cycle in which the first signal occurs to the beginning of the cycle in which the second signal occurs.

(2) Data is non-volatile at the end of the cycle in which the swap current is turned off.

(3) These parameter limits are guaranteed when the device is driven with the X and Y current shown in Figure 4. Deviations from these drive conditions may cause these limits to change in absolute angle, but the phase range (max–min) will remain as specified.

(4) Generate pulse width is defined from 50% amplitude on the rising edge to 90% amplitude on the falling edge.

FIGURE 4 — TEST CONDITIONS — X AND Y CURRENT WAVEFORMS

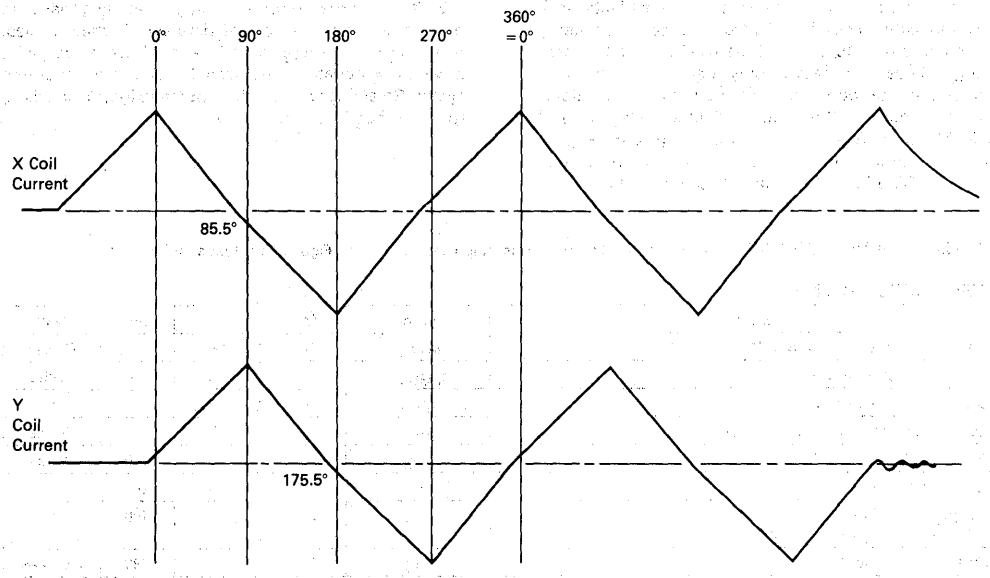
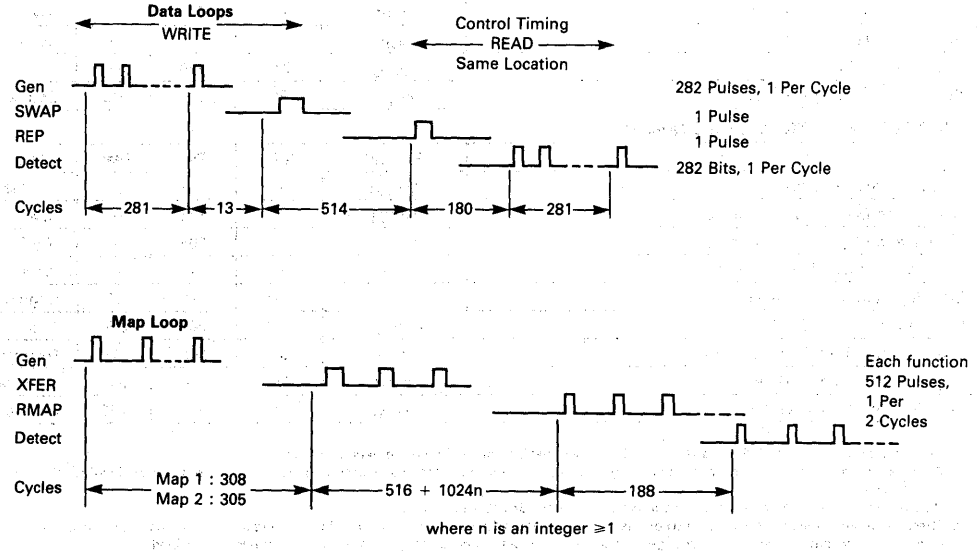
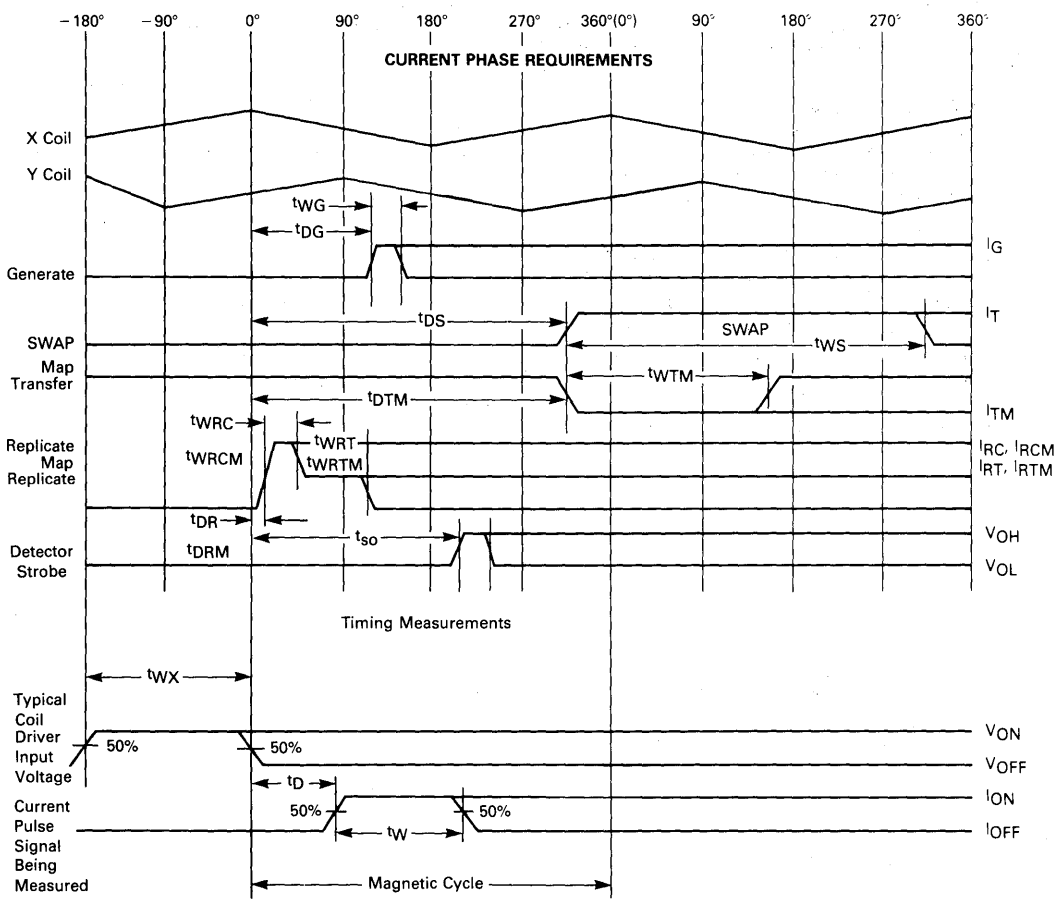


FIGURE 5



Bubble

FIGURE 6 — X, Y COIL TIMING



TIMING OF PULSES WITHIN A CYCLE

MECHANICAL SPECIFICATION

Package

The MBM2256 device is a 16-pin dual-in-line package. The die is mounted on a printed circuit board carrier attached to a beryllium copper leadframe and encapsulated in plastic compound. Two orthogonal coils and a pair of permanent magnets enclose the die and the whole device is molded into a Mumetal shield. A Z coil is included in the device to facilitate testing and extended temperature range operation.

Mechanical Data

Package Size	1.15 x 1.10 x 0.36 in (29.2 x 27.9 x 9.14) mm
Package Weight	28 gm.

Bubble

ENVIRONMENTAL SPECIFICATION

Temperature Ranges

Continuous operation at 125 kHz. Case temperature 0° to 70°C. Non-operating, non-volatile storage −40° to 100°C.

External Magnetic Fields

When subjected to an external magnetic field of 20 Oe maximum in any direction, the device will continue to operate satisfactorily as long as the parameters are kept within the range specified in this document.

Screen Tests	All Parts 100%
Die Visual	100X Inspection consistent with MIL-883B, Method 2010, Cond. B
Stabilization Bake	As per MIL-STD-883B, Method 1008, Condition C, 150°C for 24 hours
Temperature Cycling	As per MIL-STD-883B, Method 1010, Condition B, 10 cycles −55°C → 125°C
External Visual	MIL-883B, Method 2009

Qualification Testing

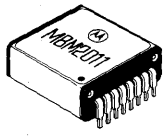
Bond Strength	MIL-883B, Method 2011.3, Condition D
Mechanical Shock	MIL-883B, Method 2002, Condition B: 1,500G for 0.5 ms
Variable Frequency	MIL-883, Method 2007, Condition A: 20-2,000 Hz for 4 mins.; peak at 20 G's.
Thermal Shock	MIL-883, Method 1011.3, Condition B: −55°C to 125°C, 15 cycles
Moisture Resistance	MIL-883B, Method D 1004.3
Resistance to Solvent	MIL-883B, Method 2015.1
Solderability	MIL-883B, Method 2003.2
Lead Integrity	MIL-883B, Method 2004.3
Flammability	Needle Flame, IEC 695-2-2

MOTOROLA

MBM2011A

Advance Information

1M X 1 BIT MAGNETIC BUBBLE MEMORY DEVICE



GENERAL DESCRIPTION

The MBM2011A is a 1,048,576 (2^{20}) bit magnetic bubble memory device. All required magnetic components, including permanent magnets, the drive field coils and protective magnetic shield are integral parts of the device. The package is a 1.15 x 1.10 x 0.36 inch 16-pin DIP.

The architecture of the MBM2011A features a double-period block-replicate organization with swap gates on the input track. Data storage is organized as 512 storage loops of 2,048 bits each. Additional loops are provided to store the error correction code and as redundant loops. In one of two dedicated map loops on-chip the redundant map loop data is stored.

The MBM2011A magnetic bubble memory can be operated synchronously or asynchronously. Average access time to a page of data is less than 11.5 ms at 100 kHz. Data transfer rate is 100 kilobits per second at 100 kHz. Average power dissipation at 100 kHz is 1.0 W. The device will operate over a case temperature range of 0°C to 70°C, and data is retained without power from −40°C to 100°C.

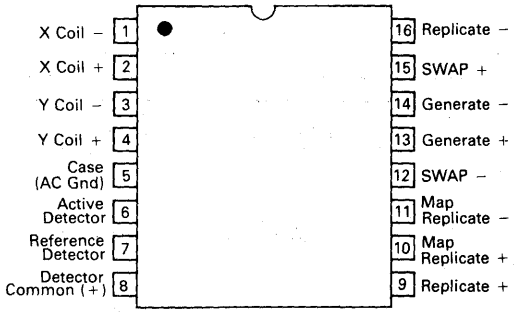
The device is fabricated using a pseudo-planar process to improve operating margins as well as to enhance reliability. The use of CrCuCr in the conductor elements insures excellent conductivity while greatly increasing resistance to problems associated with electromigration.

FEATURES

- Non-volatile
- High Density
- Solid State
- Low Power
- Start/Stop Capability
- Page-Oriented Access
- On-Chip Redundant Loop Map
- Swap Gates
- Block Replicate
- Error Correction Code Storage
- 16-pin Dual-in-Line Package

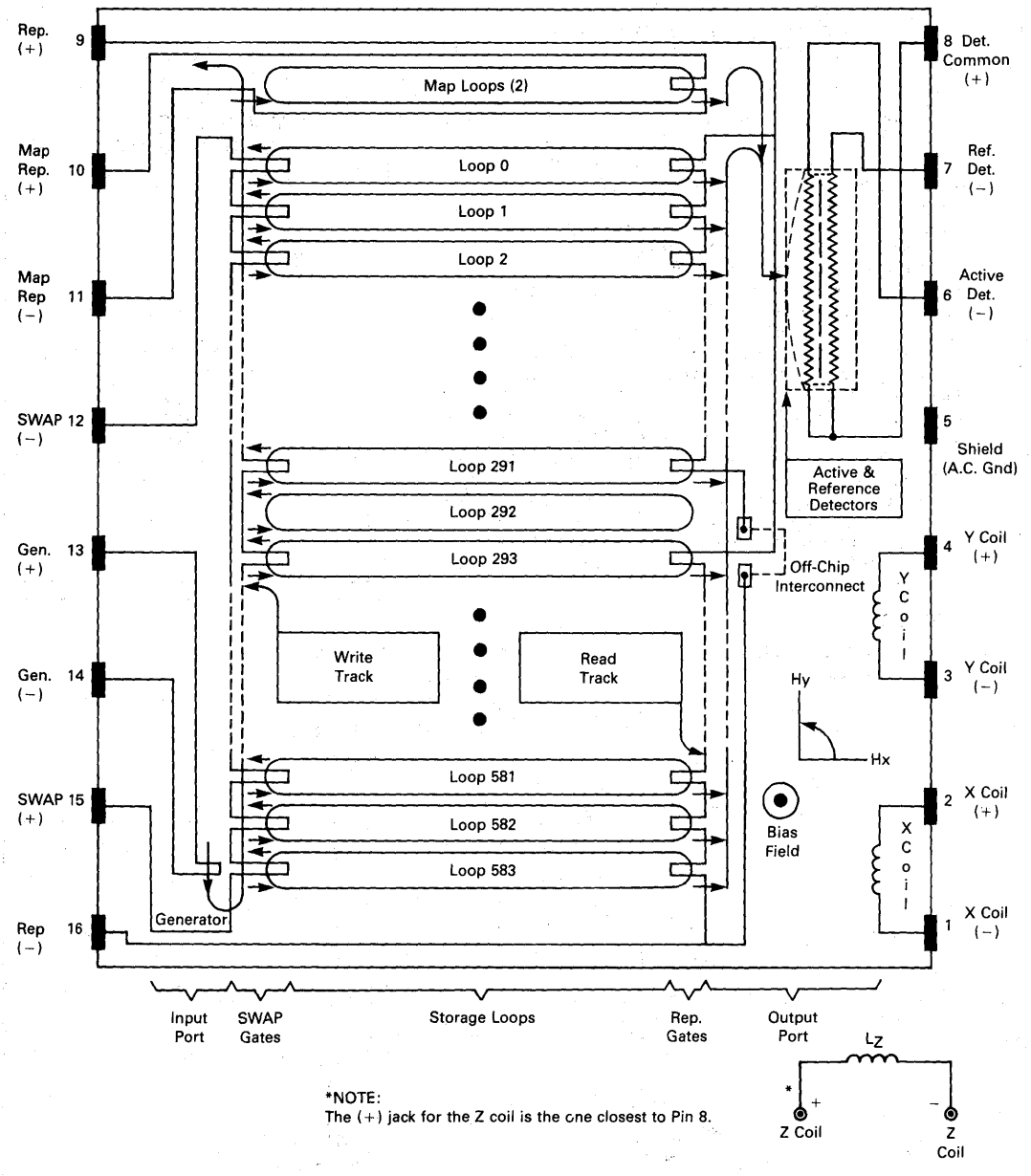
Bubble

PIN ASSIGNMENTS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

FIGURE 1 — BLOCK DIAGRAM



*NOTE:
The (+) jack for the Z coil is the one closest to Pin 8.

Bubble

ABSOLUTE MAXIMUM RATINGS

Characteristics	Min	Max	Units
Operating Temperature (Case) (T_c)	0	70	°C
Non-Volatile Storage Temperature	−40	100	°C
Storage Temperature	−40	120	°C
External Magnetic Field	—	20	Oe
Peak Current in X Coil*	—	900	mA
Peak Current in Y Coil*	—	1,100	mA
Peak Current in Z Coil*	—	3,000	mAdc
Peak Replicate Current	—	25	mAdc
Peak Generate Current	—	35	mAdc
Peak Swap Current	—	15	mAdc
Peak Detector Current	—	5.0	mAdc
Coil Disturb Current with Data Retention	—	10	mAdc
Interelement Voltage	—	55	V

*These peak currents are allowed subject to the device temperature not exceeding the temperature limits.

ELECTRICAL CHARACTERISTICS (T_C = 0°C, rotating field frequency (f_o) = 100 kHz)

FUNCTION CURRENTS

Characteristics	Symbol	Min	Typ	Max	Units
Generate Current	I_G	190	—	230	mA
Swap Current	I_S	16	—	20	mA
Data Replicate Cut Current at T_C = 25°C (Note 1)	$I_{RC(25)}$	134	144	154	mA
Data Replicate Transfer Current	I_{RT}	30	—	40	mA
Map Replicate Cut Current at T_C = 25°C (Note 1)	$I_{RCM(25)}$	67	72	77	mA
Map Replicate Transfer Current	I_{RTM}	16	—	20	mA
Map Transfer In Current	I_{TM}	−16	—	−20	mA
Detector Current	I_{DA}, I_{DR}	3.8	4.0	4.2	mA
Temperature Coefficient of Cut Current (Map and Data) Referenced to Value at T_C = 25°C (Note 1)	α_{RC}	−0.32	−0.34	−0.36	%/°C

Note 1: Map and Data replicate cut currents require temperature compensation. The current at any case temperature, T_C, is given by:

$$I_{RC(T)} = I_{RC(25}\left[1 + \frac{\alpha RC}{100}(T\text{-}25)\right] \quad 0 \leq T \leq 70°C \qquad I_{RCM(T)} = I_{RCM(25)}\left[1 + \frac{\alpha RC}{100}(T\text{-}25)\right] \quad 0 \leq T \leq 70°C$$

COIL DRIVES (See Figure 2)

Characteristics	Symbol	Min	Typ	Max	Units
Coil Driver Supply Voltage	V_X, V_Y	11.4	12	12.6	V
Coil Driver Switch on Resistance (2 switches in series)	R_{on}	0.7	—	1.8	Ω
Coil Driver Clamp Diode Drop (2 diodes in series)	V_{clamp}	—	—	1.6	V
X Coil Peak Current (L_X = nom, V_X = nom) (R_{on}, V_{clamp} = nom)	I_{XP}	—	650	—	mA
Y Coil Peak Current (L_Y = nom, V_Y = nom) (R_{on}, V_{clamp} = nom)	I_{YP}	—	740		mA
Coil Current Offset	I_{xo}, I_{yo}	−10	—	10	mA
Stop Current Overshoot	I_{so}	—	—	+10 −0	mA
Total Coil Power	P_c	—	—	1.4	W
Z-Coil Sensitivity		—	26.5	—	Oe/A
Z-Coil Current to Simultaneously Erase All Data Stored Rotating Field On Rotating Field Off	I_{zap}	2.0 3.0	— —	— —	A
Duration of Erase Current	t_{ZAP}	0.5	—	10	ms

Bubble

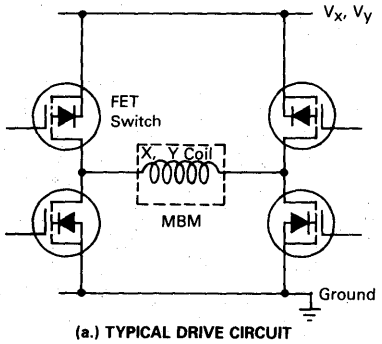
SCOPE

This specification describes the magnetic, electrical, mechanical and environmental parameters of the 1Mbit magnetic bubble device, MBM2011A as manufactured by Motorola Inc.

DEVICE ORGANIZATION

The 1Mbit bubble memory chip uses a block-replicate organization with swap gates on the input track. The storage area is arranged as 512 storage loops each, with 2,048 bit locations. Additional loops are provided for error correction (12), and defect tolerance (60), giving a total of 584 loops. Data is written and read at the clock frequency which is the rotating field frequency. Figure 1 is a schematic diagram of the 1Mbit chip.

FIGURE 2 — X, Y COIL DRIVE



(a.) TYPICAL DRIVE CIRCUIT

Data Input

To write into the device, the single generator is pulsed and the data pattern is propagated along the double period input track until it aligns with the storage loops. Operating the swap gates transfers the new data into the storage loops such that consecutive bits go into adjacent loops and simultaneously transfer out the old data.

Data Output

To read data, the replicate gate is pulsed and one bit is replicated from each loop into the double period output track. The data then propagates along the output track and through the detector such that data is read out at the clock frequency.

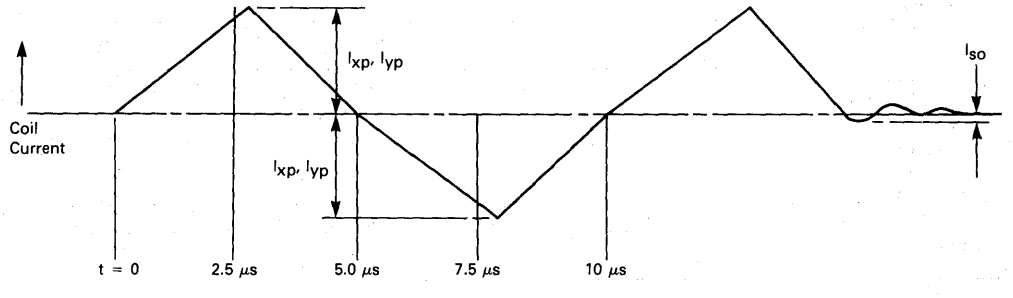
Redundancy

Of the 584 storage loops, 512 are allocated for data, 12 for error correction and 60 for redundancy. These 60 loops are used to mask inoperable minor loops and improve performance. Sixty loops are always declared redundant. Data should not be written into the redundant loops.

Redundancy Map

In addition to the 584 storage loops, the chip contains two map loops. These loops have their own transfer-in and replicate gates but share the generator and detector with the storage loops. Only one loop is required and is chosen at final test. The chosen loop is used to store the data which identifies the redundant loop map. A 'one' designates a usable loop; a 'zero,' a non-usable loop. Preceding this map code is a stream of 64 'zeros' followed by a 'one' and a 'zero' which may be used to synchronize the external control circuitry with the memory. The map loop used for storage of the redundancy information is also identified in the code (see "Coding of Redundancy Map"). Since only alternate bit positions are written into the map loop to enhance reliability, intervening bits are always zero and are ignored during read (see "Map Read Operation").

The redundancy map is also printed on the label of each device using hexadecimal format. Two digits are used per loop. Instead of providing the absolute loop number, the incremental difference between non-usable loops is printed. For example, if the first bad loop is #7, and the next two are 19 and 23, the sequence 070C04 will be printed on the label. This format allows for an incremental difference between two non-usable loops of up to 255 (FF). Loop #292 is not connected in the 1Mbit device and is always declared bad.



(b.) TYPICAL RISE/FALL IMBALANCE DUE TO DRIVE CIRCUIT

Coding of Redundancy Map. The map loop contains 1024 bits of information in five fields.

Pattern	Field	Number of Bits	Notes
MM...MM	Map Data	584	(1)
EE...EE	Error Correction	12	(2)
LL	Loop	2	(3)
UU...UU	User	360	(4)
00...0010	Sync	66	(5)

(1) Each bit corresponds to a data loop in sequence
M = 1 identifies a usable loop (524).
M = 0 identifies a redundant loop (60).
(2) Error correction code used is a fire code applied only to the map data.
(3) Identifies which map loop contains the redundancy information 01 — loop #1, 10 — loop #2.
(4) This field may contain factory-pertinent information. It will not contain a duplicateof the sync pattern.
(5) The sync pattern is used to locate the beginning of the map data field and identifies data page zero.

Organizational Specifications

Bits/Loop	2,048
Total Data Loops	584
Usable Data Loops	524
Error Correction Loops	12
User Data Loops	512
Total User Storage	1,048,576 bits
Map Loops	2

FUNCTIONAL DESCRIPTION

Write Data Operation

Writing data is accomplished by generating a pattern with a series of pulses applied to pins 13 and 14, starting t_{PGSF} before the swap operation. As the device continues to cycle after all data is generated, the new data and the old will be aligned at the swap gates after t_{PGSL}. A swap pulse is applied to pins 12 and 15 at this time, swapping the new data in and the old data out. The old data are propagated out and discarded beyond the active area.

Note: In order to ensure correct device operation, it is essential that at least one empty bit position follows the last bit of a data block.

Read Data Operation

To read data, the device must be cycled until the desired page is aligned with the replicate gates on the output side of the storage loops. A replicate cut pulse is applied to pins 9 and 16 to duplicate the page. This is immediately followed by a replicate transfer pulse which causes the duplicate bubbles to propagate into the output track.

Detection occurs when a bubble passes under the magnetoresistive detector element. The bubble's magnetic field causes the detector element to change resistance. By passing a constant current through the detector, this is converted to a voltage signal. A dummy detector which is not influenced by magnetic bubbles is used to cancel the background magnetoresistive signal.

Output bubbles are discarded beyond the active area after detection. A complete page is read in t_{PRDL}.

INTERFACE IMPEDANCES

Characteristics	Symbol	Min	Typ	Max	Units
Generate (2)	r_G	4.0	—	11	Ω
Swap (2)	r_S	500	—	1150	Ω
Replicate (2)	r_R	90	—	160	Ω
Map Replicate (Includes Map Transfer-In) (2)	r_M	28	—	65	Ω
Detector (Active and Reference) (2)	R_{DA}, r_{DR}	900	—	2000	Ω
Detector Active/Reference Ratio		0.985	—	1.015	
X Coil Inductance	L_x	41	—	44	μH
Y Coil Inductance	L_y	36	—	39	μH
Z Coil Inductance	L_z	25	—	35	μH
X Coil dc Resistance Non-Operating, 25°C	r_x	—	3.3	—	Ω
Y Coil dc Resistance Non-Operating, 25°C	r_y	—	1.5	—	Ω
Z Coil dc Resistance Non-Operating, 25°C	r_z	—	0.75	—	Ω
X Coil ac Resistance (2)	r_x	3.3	—	5.3	Ω
Y Coil ac Resistance (2)	r_y	2.1	—	3.1	Ω

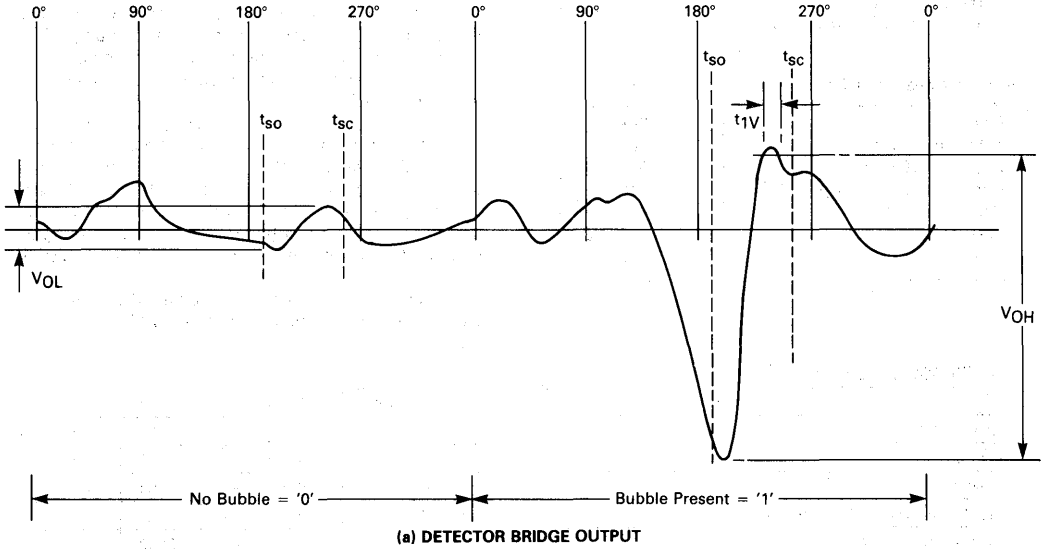
NOTE:
(2) $T_{C(min)}$ = 0°C, non-operating
$T_{C(max)}$ = 70° C, operating

OUTPUT SIGNALS (T_C = 0°C to 70°C, f_o = 100 kHz)

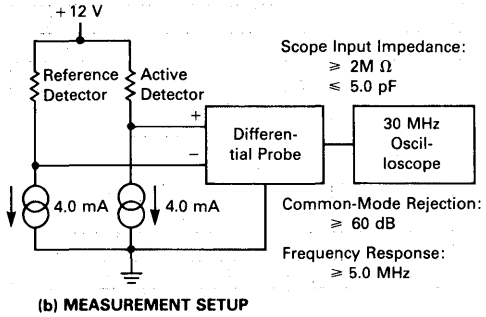
Characteristic	Symbol	Min	Typ	Max	Units
Common-Mode Output Signal (I_{DA} = I_{DR} = 4.0 mA) Differential Peak-to-Peak Output Voltage (See Note 1) I_d = 4.0 mA, See Figure 1 for measurement details)	V_{cm}	—	—	50	mV
Logic 1 Bubble Present	V_{OH}	TBD	—	—	mV
Logic 0 No Bubble	V_{OL}	—	—	TBD	mV
Signal Strobe Leading Edge Phase	t_{so}		191		Degrees
Signal Strobe Trailing Edge Phase	t_{sc}		258		Degrees
Logic 1 Valid Window	t_{1V}	50			ns

Note 1: V_{OH} is defined as the difference between the most negative and the most positive signal excursions which occur within the phase window t_{so} to t_{sc} when a bubble is being detected. V_{OL} is similarly defined for the case of no bubble being detected. See Figure 3.

FIGURE 3



(a) DETECTOR BRIDGE OUTPUT



(b) MEASUREMENT SETUP

Map Read Operation

To read the contents of the map, a series of alternate cycle map replicate pulses is applied to pins 10 and 11. Data will be available after t_{PMRD}. Since map data is only loaded into alternate positions in the loop, one pass may result in no data. In this case, the procedure is repeated after delaying one cycle. The outputs from the two map loops are merged, but only one loop contains data. See "Coding of Redundancy Map Loops" for decoding information.

Map Write Operation

Writing the map loop is accomplished by generating map information as normal data on alternate cycles. After t_{PGT1} or t_{PGT2}, pins 10 and 11 are pulsed with a series of negative map transfer pulses on alternate cycles. Selecting t_{PGT1} writes into map loop 1, selecting t_{PGT2} writes into map loop 2.

TIMING CHARACTERISTICS T_C = 0°C to 70°C, f_o = 100 kHz. See Figure 4 for test conditions. All control pulses to have rise and fall times ≤ 80 ns (10%–90% of pk amplitude) unless otherwise noted. All pulsewidths measured at 50% amplitude unless otherwise noted.

WRITE CYCLE TIMING

Characteristic	Symbol	Min	Typ	Max	Units
Generate First Bit to Swap In (1)	$t_{PGS(F)}$	—	597	—	Cycles
Generate Last Bit to Swap In (1)	$T_{PGS(L)}$	—	14	—	Cycles
Swap In to Replicate Out (1)	t_{PSR}	—	1026	—	Cycles
Swap In to Non-Volatile Storage (2)	t_{PS}	—	2	—	Cycles
Generate Delay Time (3)	t_{DG}	70		120	Degrees
Generate Pulse Width (4)	t_{WG}	100	150	200	ns
Generate Fall Time (80%–90% of pk Amplitude)	t_{FG}	200		400	ns
Swap Delay Time (3)	t_{DS}	270		330	Degrees
Swap Pulse Width	t_{WS}	340	370	400	Degrees

READ CYCLE TIMING

Replicate Out to Detect First Bit (1)	$t_{PRD(F)}$	—	91	—	Cycles
Replicate Out to Detect Last Bit (1)	$t_{PRD(L)}$	—	674	—	Cycles
Replicate Out to Swap In (1)	t_{PRS}	—	1022	—	Cycles
Replicate Delay Time (3)	t_{DR}	0		12	Degrees
Replicate Cut Pulse Width	t_{WRC}	50	75	100	ns
Replicate Transfer Pulse Width	t_{WRT}	80	100	120	Degrees

MAP READ AND WRITE CYCLE TIMING

Characteristic	Symbol	Min	Typ	Max	Units
Map Replicate to Detect	t_{PMRD}	—	97	—	Cycles
Generate to Map Loop # 1 Transfer	t_{PGT1}	—	608	—	Cycles
Generate to Map Loop #2 Transfer	t_{PGT2}	—	605	—	Cycles
Map Loop Transfer-In to Replicate	t_{PTR}	—	1028	—	Cycles
Map Replicate Delay Time (3)	t_{DRM}	0	—	12	Degrees
Map Replicate Cut Pulse Width	t_{WRCM}	50	75	100	ns
Map Replicate Transfer Pulse Width	t_{WRTM}	80	100	120	Degrees
Map Transfer-In Delay Time	t_{DTM}	270	—	330	Degrees
Map Transfer-In Pulse Width	t_{WTM}	200	220	240	Degrees

NOTES: (1) Propagation times are defined from the beginning of the cycle in which the first signal occurs to the beginning of the cycle in which the second signal occurs.

(2) Data is non-volatile at the end of the cycle in which the swap current is turned off.

(3) These parameter limits are guaranteed when the device is driven with the X and Y current shown in Figure 4. Deviations from these drive conditions may cause these limits to change in absolute angle, but the phase range (max.–min.) will remain as specified.

(4) Generate pulse width is defined from 50% amplitude on the rising edge to 90% amplitude on the falling edge.

FIGURE 4 — TEST CONDITIONS — X AND Y CURRENT WAVEFORMS

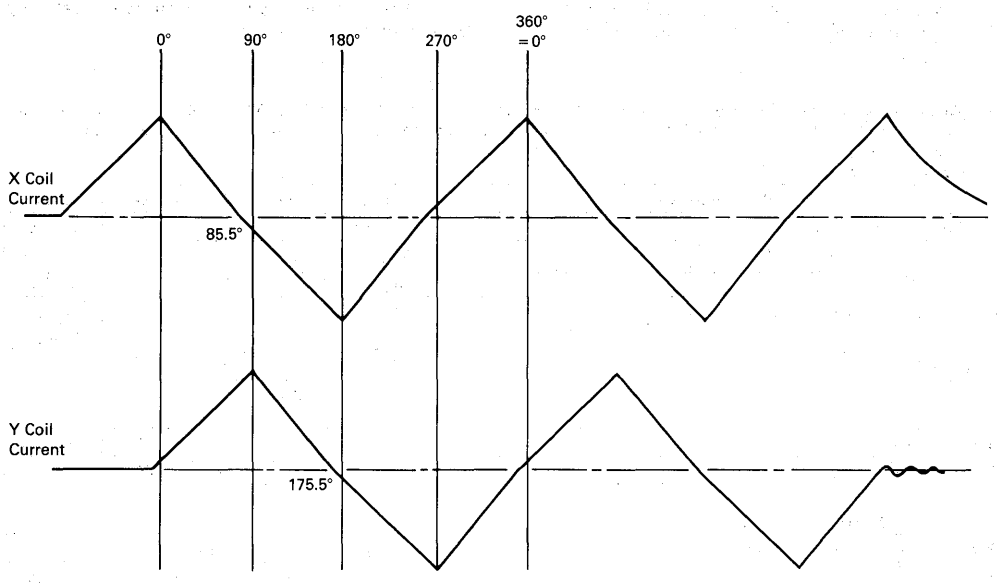
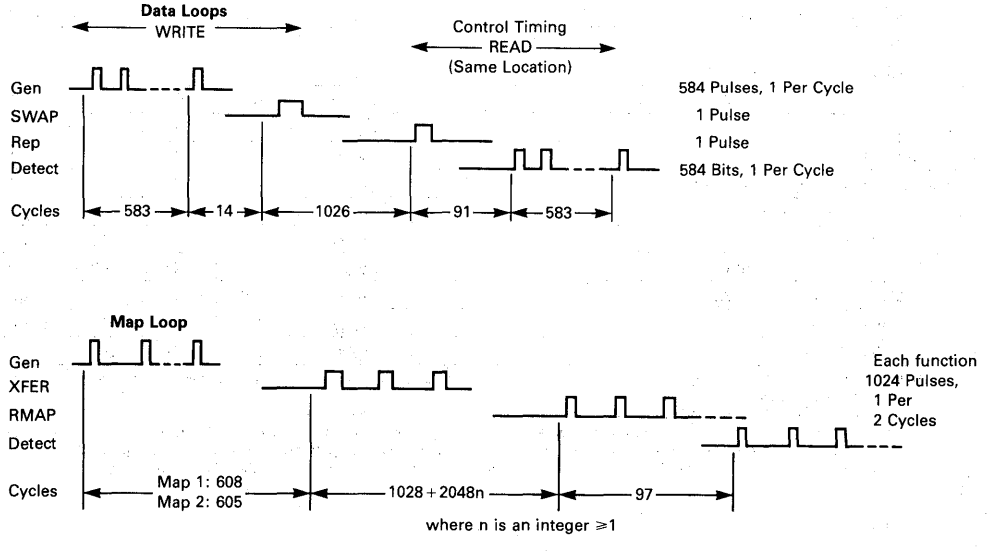
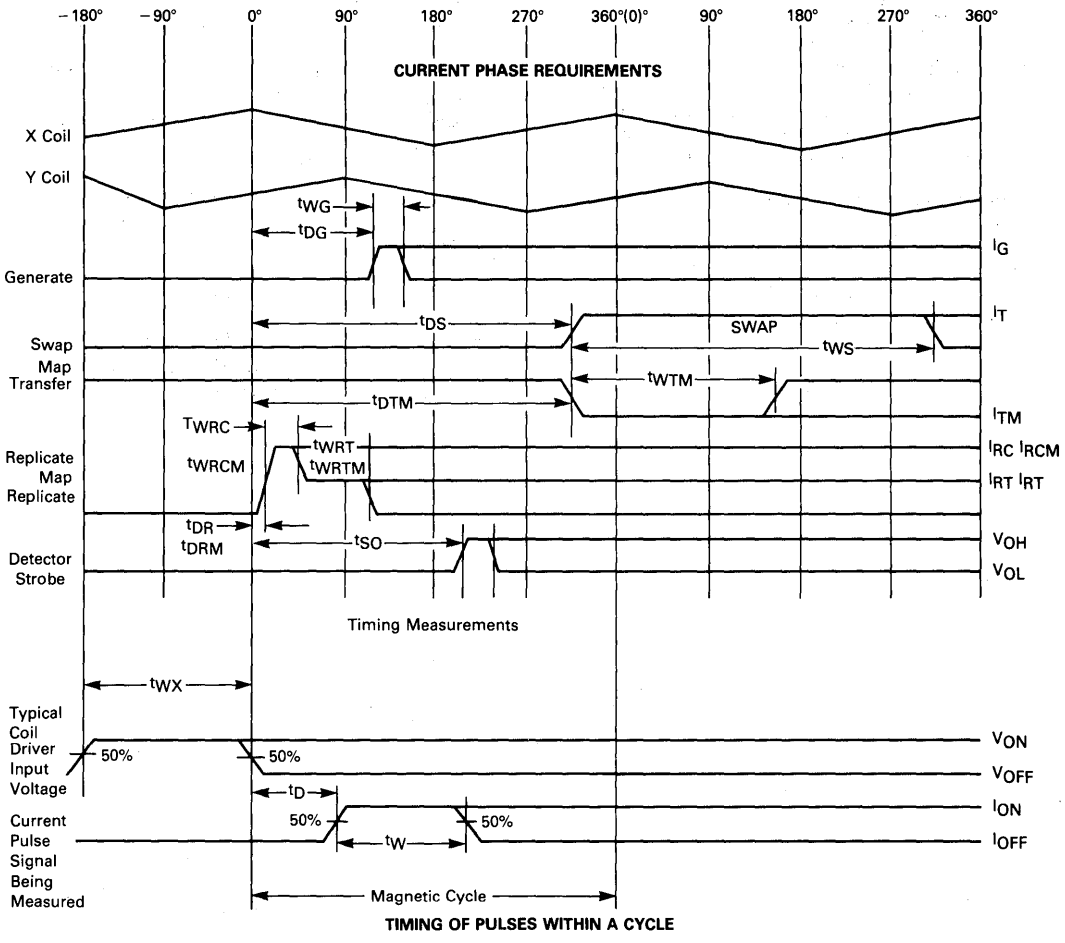


FIGURE 5



Bubble

FIGURE 6 — X, Y COIL TIMING



TIMING OF PULSES WITHIN A CYCLE

MECHANICAL SPECIFICATION

Package

The MBM2011A device is a 16-pin dual-in-line package. The die is mounted on a printed circuit board carrier attached to a beryllium copper leadframe and encapsulated in plastic compound. Two orthogonal coils and a pair of permanent magnets enclose the die and the whole device is molded into a Mumetal shield. A Z coil is included in the device to facilitate testing and extended temperature range operation.

Mechanical Data

Package Size	1.15 x 1.10 x 0.36 in (29.2 x 27.9 x 9.14) mm
Package Weight	28 gm.

Bubble

ENVIRONMENTAL SPECIFICATION

Temperature Ranges
(See "Absolute Maximum Ratings").

External Magnetic Fields
When subjected to an external magnetic field of 20 Oe maximum in any direction the device will continue to operate satisfactorily as long as the parameters are kept within the range specified in this document.

Screen Tests	All Parts 100%
Die Visual	100X Inspection consistent with MIL-883B, Method 2010, Cond. B
Stabilization Bake	As per MIL-STD-883B, Method 1008, Condition C, 150°C for 24 hours
Temperature Cycling	As per MIL-STD-883B, Method 1010, Condition B, 10 cycles −55°C → 125°C
External Visual	MIL-883B, Method 2009

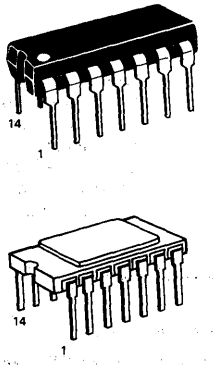
Qualification Testing	
Bond Strength	MIL-883B, Method 2011.3, Condition D
Mechanical Shock	MIL-883B, Method 2002, Condition B: 1,500G for 0.5 ms
Variable Frequency	MIL-883, Method 2007, Condition A: 20-2,000 Hz for 4 mins.; peak at 20 G's.
Thermal Shock	MIL-883, Method 1011.3, Condition B: −55°C to 125°C, 15 cycles
Moisture Resistance	MIL-883B, Method D 1004.3
Resistance to Solvent	MIL-883B, Method 2015.1
Solderability	MIL-883B, Method 2003.2
Lead Integrity	MIL-883B, Method 2004.3
Flammability	Needle Flame, IEC 695-2-2

MOTOROLA

MC34044

Advance Information

BUBBLE MEMORY SENSE AMPLIFIER



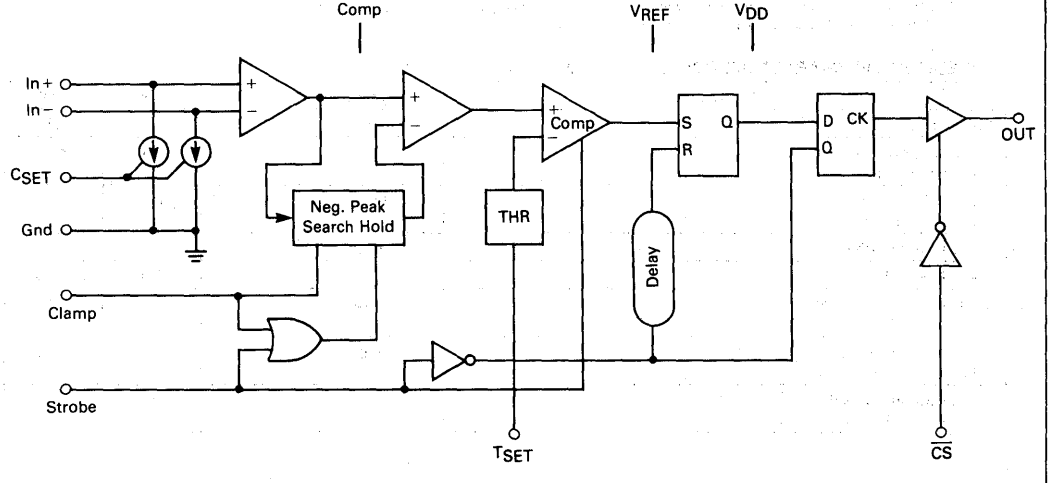
GENERAL DESCRIPTION

The MC34044 Bubble Memory Sense Amplifier is a monolithic bipolar linear integrated circuit which amplifies and detects the differential output signal of a magnetic bubble memory device. Peak-to-peak sensing is performed within a selected time window, thus rejecting noise which occurs outside that window. The Sense Amplifier circuit includes two matched, programmable current sinks which provide constant-current detector operation. The Sense threshold is externally selectable. The MC34044 is packaged in a 14-pin dual in-line package.

FEATURES

- True Peak-to-Peak Sensing
- Independent Time Windows for Negative and Positive Peak Detection Permit Rejection of Unwanted Signal Noise
- Constant Current Detector Operation — Currents Set by External Precision Resistor
- One of Three Preset Threshold Levels Selectable by User
- Linear Threshold Control from External Source Optional
- Noise Compensation Capacitor Reduces Susceptibility to Power Supply Noise
- Chip Select Input and Three-State Output for Multiple-Bubble Systems

FIGURE 1 — BUBBLE MEMORY SENSE AMPLIFIER FUNCTIONAL DIAGRAM

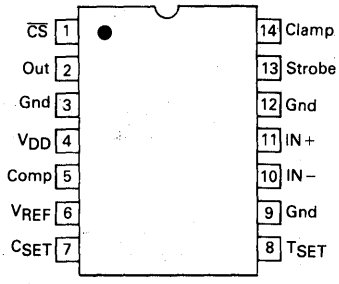


Bubble

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN ASSIGNMENT

14-pin Dual In-line Package: 0.3-inch row spacing
also 14-lead Flat-Pack



PIN DESCRIPTIONS

Output (three-state)

OUT — Data Output — following the trailing edge of STROBE, indicates the state of the detected signal during the STROBE — high if the signal exceeded the threshold, low otherwise. Held in high-impedance state when $\overline{CS}$ is high.

Supplies and Miscellaneous

V_{DD} — Power supply voltage.

V_{REF} — Reference voltage for bias current and threshold.

GND(3) — System ground (three pins).

CSET — Detector current set resistor.

TSET — Threshold select.

COMP — Noise compensation capacitor.

Inputs

$\overline{CS}$ — Chip Select — enables the three-state data output.

IN+ IN− — Differential sense signal input — negative peak detect and threshold are with respect to the indicated polarities. Also provides the detector bias currents.

CLAMP — Enables negative peak detection and activates peak hold function.

STROBE — Enables threshold comparator for positive peak detection. Trailing edge resets peak-hold function and enables OUT signal change.

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Value	Unit
Storage Temperature	−65 to +150	°C
Ambient temperature with power applied Commercial Device Extended-temperature Device	 0 to +70 −55 to +125	 °C °C
Voltage — V_{DD}, IN+, IN− to GND	−0.2 to +20	Volts
Voltage — any other pin to GND	−0.2 to +6.0	Volts
Power dissipation	TBD	Watts

*Absolute Maximum Ratings indicate limits beyond which permanent damage may occur to the device. Proper operation of the device requires that it be limited to the conditions specified under DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{REF} = 2.50 V ±1%)

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{DD}	10.8	18	Volts
Power Supply Current (Excludes I_D)	I_{DD}	—	25	mA
Current from V_{REF} (V_{REF} = 2.525 V)	I_{REF}	—	$0.1I_D+0.2$	mA
Logic High In Voltage	V_{IH}	2.0	—	Volts
Logic Low In Voltage	V_{IL}	—	0.8	Volts
Logic High Out Voltage (I_O = −4.0 mA)	V_{OH}	2.7	—	Volts
Logic Low Out Voltage (I_O = 1.6 mA)	V_{OL}	—	0.4	Volts
Logic High In Current (V_I = 2.7 V)	I_{IH}	—	20	μA

Bubble

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{REF} = 2.50 V ±1%)

Parameter	Symbol	Min	Max	Unit
Logic Low In Current (V_I = 0.4 V)	I_{IL}	—	−1.6	mA
Output Off-State Current (V_O = 0.4 − 2.7 V)	I_{OZ}	−20	20	μA
Detector Current	I_D	$10*V_{REF}/R_{SET}$ ±10%		
Detector Current Mismatch	I_{DM}	—	2%	—
IN+, IN− DC Voltage	V_{ICR}	3.0	V_S −3.0	Volts
Differential DC IN Volts	V_{IND}	—	200	mV
AC Common-Mode IN Volts	V_{ICM}	—	200	mV
Low Threshold Voltage (V_{TSET} = V_{REF})	V_{TL}	TBD	TBD	mV
Nominal Threshold Voltage (TSET pin open)	V_{TN}	TBD	TBD	mV
High Threshold Voltage (V_{TSET} = 0.0 V)	V_{TH}	TBD	TBD	mV

Note 1: Includes 1% tolerance on R_{SET}.

AC ELECTRICAL CHARACTERISTIC (T_A = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit
$\overline{CS}$ to OUT	t_{CO}	—	300	ns
$\overline{CS}$ to OUT Disable	t_{CZ}	—	300	ns
STROBE to OUT Change	t_{SO}	—	300	ns
Delay Differential IN to Comparator Output	t_d	—	300	ns

OPERATION

Detection of a magnetic bubble within the memory device utilizes the magnetoresistive effect whereby a bubble passing beneath the detector element causes a change in its resistance. By passing a constant current through the detector, this resistance change can be sensed as a voltage change. A matched reference element which is not in the path of the bubble permits the use of differential sensing to cancel noise introduced by the rotating field.

The Sense Amplifier circuit contains matched constant-current sinks for the active and reference detector elements. These elements should be connected beween the supply voltage and the IN+ and IN− pins respectively. These pins are connected internally to the current sinks. The current levels are matched and are set by meeans of a precision resistor connected externally between the CSET pin and ground. A thermistor may be used to provide a temperature-compensated detector current if required for extended-temperature operation of the magnetic bubble memory.

A differential amplifier across the two detector elements amplifies the bubble signal. The difference signal is fed to a negative peak detect-and-hold circuit, and to another difference amplifier. The difference between the signal and the negative peak is fed to a voltage comparator where it is compared to a threshold voltage. A signal which exceeds the threshold indicates the passage of a bubble beneath the detector. One of three predetermined threshold voltages can be selected by connecting the TSET pin to V_{REF} or to GND or leaving it open. For extended-temperature operation, linear control of the threshold can be accomplished by applying a linear voltage to TSET.

Timing is provided through the CLAMP and STROBE inputs. CLAMP enables the negative-peak detector. The most-negative voltage appearing while CLAMP is high is stored until the trailing edge of STROBE. The output of the threshold comparator is enabled while STROBE is high. if the signal exceeds the negative peak by the threshold amount at any time while STROBE is high, a ONE is detected and latched. The output pin changes state at the trailing edge of STROBE. CLAMP and STROBE may be connected together and driven with a single signal.

The COMP pin may be used to reduce the effect of power supply noise on the detector. A capacitor connected between COMP and V_{DD} increased the supply rejection performance of the internal regulator with respect to noise present on V_{DD}. The best value will depend upon the individual system, and is typically 0.1 μF.

The Chip Select ($\overline{CS}$) input is active-low. When $\overline{CS}$ is false (high) the three-state data output (OUT) is placed in the high-impedance state. Several Sense Amplifiers may have their OUT pins connected together with only one circuit enabled at a time via the $\overline{CS}$ pin.

FIGURE 2 — SIGNAL WAVEFORMS

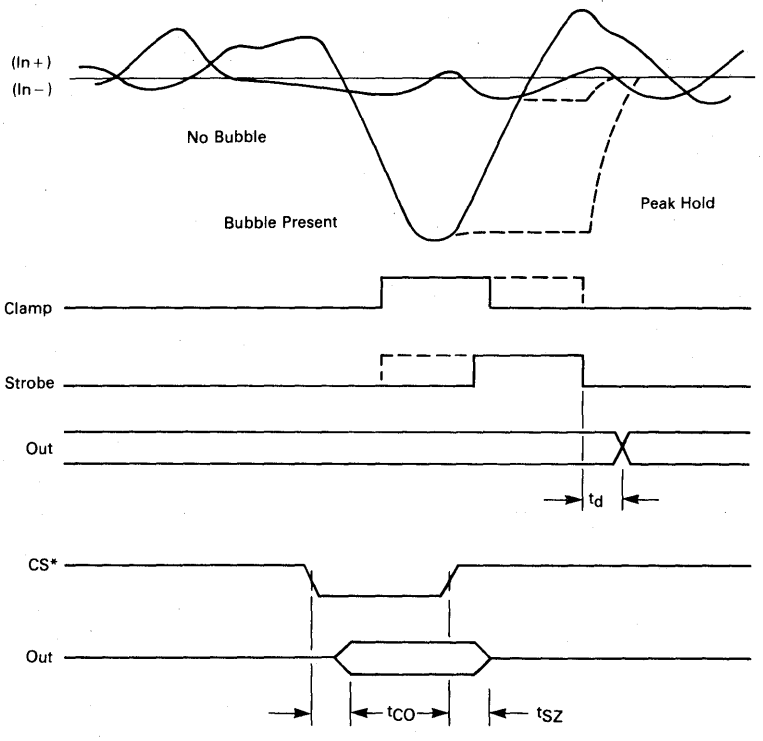
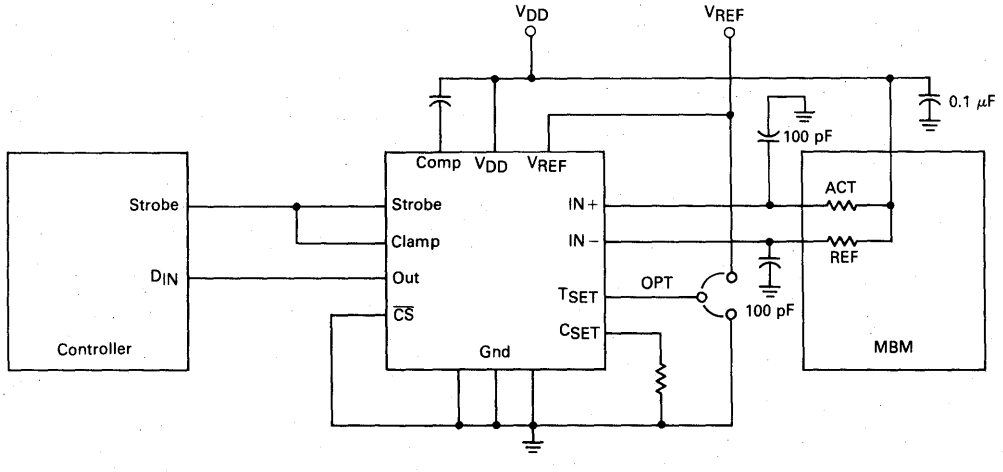


FIGURE 3 — TYPICAL APPLICATION

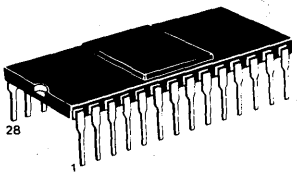


MOTOROLA

MC34046S
MC34047S

Advance Information

SINGLE BUBBLE MEMORY OPERATION DRIVERS



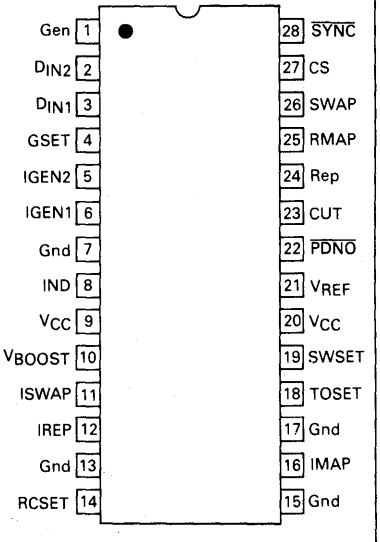
GENERAL DESCRIPTION

The MC34046S and MC34047S Single Bubble Memory Operation Drivers are monolithic bipolar linear integrated circuits which generate controlled-current pulses for the generate, swap, replicate and map-loop operations in a magnetic bubble memory device. The MC34046S and MC34047S are pin-compatible and specifically designed to drive the Motorola MBM2256 (256-kilobit) and MBM2011 (one-megabit) bubble memories respectively. They differ only in the amplitudes of the current pulses generated. Each Operation Driver can drive one bubble memory. Basic control/timing signals are input to the Operation Driver from the bubble memory controller. Each circuit contains a voltage booster to provide the high-voltage required by the swap and replicate circuits. Under-voltage detection prevents operation until this supply has reached its proper level. The circuits are packaged in 28-pin, 0.6-inch wide dual in-line packages.

FEATURES

- Single Bubble Memory Drive Capability
- Controlled-current Sinks Assure Proper Currents Independent of Variations in Bubble Gate Resistances
- Currents Independently Set by External Precision Resistors
- Temperature Compensation of Currents Via External Thermistor if Desired
- GENERATE Pulse Specially Shaped to Prevent Multiple Bubble Generation
- Pulse Time-out Circuit Protects Against Physical Damage in the Event of a Stuck Input Timing Signal
- On-chip High-voltage Source — System Interlocked until Proper Voltage is Present
- Chip Select Input for Multiple-bubble Systems
- Full Map Loop Read and Write Operation

PIN ASSIGNMENTS



28-pin Dual In-line
Package: 0.6-inch row spacing

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Value	Unit
Storage Temperature	−65 to +150	°C
Ambient Temperature with power applied Commercial Device Extended-temperature Device	 0 to +70 TBD to +85	 °C °C
Voltage — V_{BOOST}, IND, IREP, ISWAP	−0.2 to +35	Volts
Voltage — IGEN1, IGEN2, IMAP	−0.2 to +20	Volts
Voltage — V_{CC}	−0.2 to +7.0	Volts
Voltage — any other pin to GND	−0.2 to +6.0	Volts
Power dissipation	TBD	Watts

*Absolute Maximum Ratings indicate limits beyond which permanent damage may occur to the device. Proper operation of the device requires that it be limited to the conditions specified under DC Electrical Characteristics.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Bubble

PIN DESCRIPTIONS

Inputs

CS — Chip Select — enables the Operation Driver.

D_{IN1}
D_{IN2} — Data inputs (two channels).

$\overline{SYNC}$ — Data input clock (rising edge).

GEN — Trigger for GENERATE current pulses.

SWAP — Enable SWAP current pulse.

REP — Enable REPLICATE current pulse.

RMAP — Enable MAP-REPLICATE current pulse.

CUT — Timing for CUT portion of REPLICATE and MAP-REPLICATE current pulses.

Outputs

IGEN1
IGEN2 — GENERATE current pulses (two channels).

ISWAP — SWAP current pulse.

IREP — REPLICATE current pulse.

IMAP — MAP-REPLICATE current pulse.

$\overline{PDNO}$ — Power Down Output — indicates that V_{BOOST} is below its minimum operating value.

Supplies and Miscellaneous

GSET — GENERATE current set.

SWSET — SWAP current set.

TOSET — REPLICATE-TRANSFER current set.

RCSET — REPLICATE-CUT current set (adds to TRANSFER current).

V_{CC}(2) — Power supply voltage (2 pins).

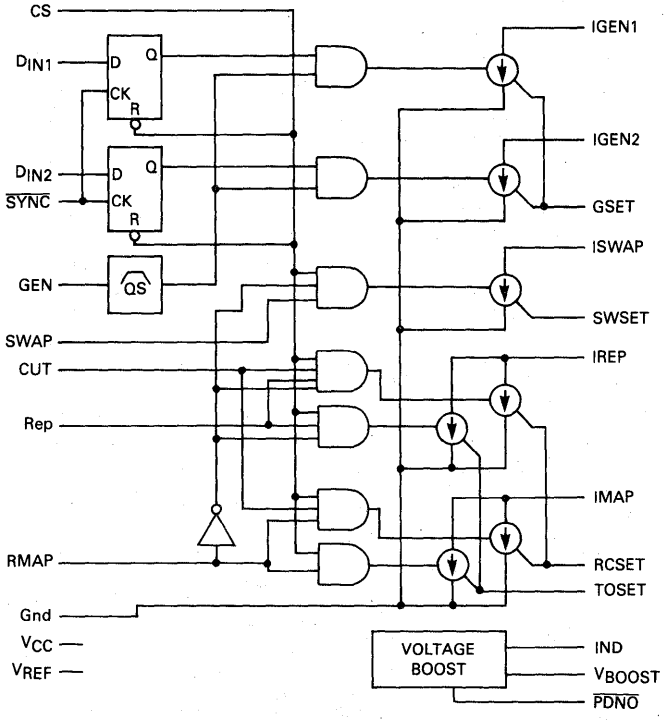
V_{REF} — Reference voltage used to set currents.

V_{BOOST} — High-voltage power supply output.

IND — Inductor and diode used in voltage-boost circuit (see application diagram).

GND(4) — System Ground (4 pins).

FIGURE 1 — FUNCTIONAL DIAGRAM



DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{REF} = 2.50 V ±1%)

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.75	5.25	Volts
Power Supply Current	I_{CC}	—	100	mA
Current from V_{REF} (V_{REF} = 2.475 V)	I_{REF}	—	2.0	mA
Boost Supply Voltage	V_{BOOST}	28	35	Volts
Logic High In Voltage	V_{IH}	2.0	—	Volts
Logic Low In Voltage	V_{IL}	—	0.8	Volts
Logic Low Out Voltage (I_O = 4.0 mA)	V_{OL}	—	0.4	Volts
Logic High In Current (V_I = 2.7 V)	I_{IH}	—	10	μA
Logic Low In Current (V_I = 0.4 V)	I_{IL}	—	−1.6	mA
Output Leakage Current (Output Off)	I_{OL}	—	100	μA
IREP, ISWAP Saturation	V_{SATH}	—	6.0	Volts
Saturation Voltage — Other Outs	V_{SATL}	—	3.0	Volts

Note: The Bubble Memory Controller WRITE MAP command should not be executed more often than once per second, or the Operation Driver maximum power dissipation limit will be exceeded.

MC34046S ONLY (V_{REF} = 2.50 V ±1%, Current Set Resistors = 6.04 kΩ ±1% each)

Characteristic	Symbol	Min	Max	Unit
Generate Current	I_G	180	220	mA
SWAP Current	I_{SW}	25	31	mA
REPL-Transfer Current	I_{RT}	28	42	mA
REPL-Cut Current (Note 1)	I_{RC}	75	95	mA
MAP-REP-Transfer Current	I_{MT}	28	42	mA
MAP-REP-CUT Current (Note 1)	I_{MC}	75	95	mA

MC34047S ONLY (V_{REF} = 2.50 V ±1%, Current Set Resistors = 6.19 kΩ ±1% each)

Generate Current	I_G	190	230	mA
SWAP Current	I_{SW}	16	20	mA
REPL-Transfer Current	I_{RT}	30	40	mA
REPL-CUT Current (Note 1)	I_{RC}	130	150	mA
MAP-REP-Transfer Current	I_{MT}	16	20	mA
MAP-REP-CUT Current (Note 1)	I_{MCI}	65	75	mA

Note 1: CUT current is the sum of the currents determined by the resistors connected to TOSET and RCSET.

AC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit
DIN Setup Time	t_{DSU}	50	—	ns
DIN Hold Time	t_{DH}	50	—	ns
CUT Current Risetime (MC34047S only)	t_{CR}	—	50	ns
Other Out Current Rise	t_r	—	100	ns
IGEN Current Fall	t_{GF}	200	400	ns
CUT Current Falltime (MC34047S only)	t_{CF}	—	100	ns
Other Out Current Fall	t_F	—	200	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Unit
IGEN Pulse Width	t_{GW}	50	200	ns
CS to any Output	t_{CSO}	—	250	ns
GEN to IGENx Delay	t_{GGO}	—	200	ns
SWAP to ISWAP Delay	t_{SSO}	—	160	ns
Other In-Out Delays	t_{IO}	—	100	ns
SWAP Time-out	t_{STO}	—	80	μS
REPL-Transfer Time-out	t_{TTO}	—	50	μS
REPL-CUT Time-out	t_{CTO}	—	4.0	μS
GEN to SYNC	t_{GS}	1.1	—	μS

OPERATION

The magnetic bubble memory device requires a series of current pulses of proper timing, amplitude, and shape to generate and route the bubbles. These pulses are produced by the Operation Driver in response to signals generated by the controller.

The generate pulse creates a bubble in the input track. It is a fixed-width pulse triggered by the rising edge of the GEN input. A controlled fall time prevents multiple-bubble generation which can occur if the trailing edge is too sharp. Two generate outputs, IGEN1 and IGEN2, can drive separate bubble devices. They are independently enabled by data signals received on DIN1 and DIN2 respectively. The DIN signals are latched internally on the rising edge of $\overline{SYNC}$ prior to the GEN input. A high level on DINx will enable IGENx.

The Swap Pulse, ISWAP, causes an exchange of bubbles between the input track and the storage-loop tracks. It is on when the SWAP input is high. ISWAP is normally connected to the data swap gate on the bubble device, but if map loop write capability is required, it may be connected via a switch, jumpers, etc. to the map gate.

The replicate function copies bubbles from the storage-loop tracks onto the output track. A two-step pulse is used. A high-current, narrow initial portion cuts the elongated bubble in two; a lower-current, wider trailing portion transfers the trailing bubble onto the output track. Separate outputs are provided for data replicate, IREP, and map replicate, IMAP. These outputs are controlled by three input signals: REP or RMAP when high enables IREP or IMAP respectively; CUT when high enables the high-current portion of whichever pulse is simultaneously enabled.

The current levels of the various pulses are set by means of precision resistors connected externally between each of four pins and ground:

- GSET controls IGEN1 and IGEN2.
- SWSET controls ISWAP.
- TOSET controls the lower (transfer) level of IREP and IMAP.
- RCSET controls the initial (cut) portion of IREP and IMAP. This current is added to that determined by TOSET.

Temperature compensation of the currents for extended-temperature operation, can be done by using thermistor networks on the SET pins.

The Chip Select (CS) input is active high. When it is false (low) all current outputs are disabled. Since some of the current pulse levels, if sustained would damage the bubble device or the driver, a time-out circuit is included which will shut off any pulse if the input signal should remain active too long.

The higher resistance of the swap and data replicate gates requires a higher drive voltage than the normal power supply, V_{DD}. This voltage, V_{BOOST}, is provided by an on-chip voltage booster in conjunction with an external inductor, capacitor, and diode. When V_{BOOST} is below its specified range the Power Down Output signal $\overline{PDNO}$ is held low. This is an open-collector output signal and may be externally wire-ored.

FIGURE 2 — SIGNAL WAVEFORMS

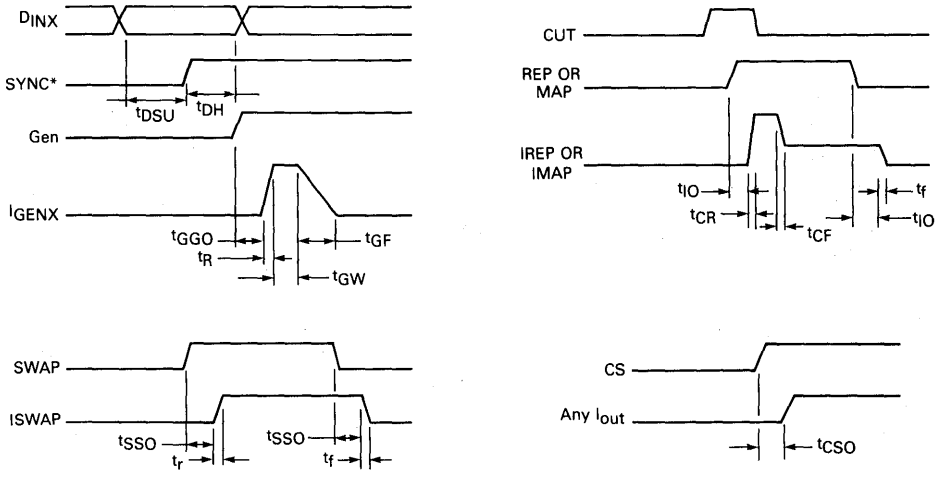
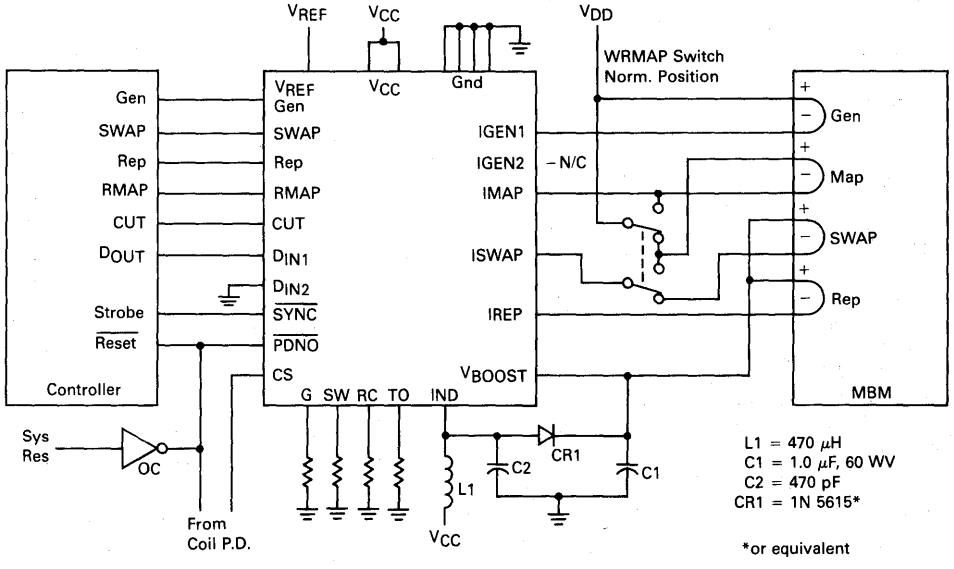


FIGURE 3 — TYPICAL APPLICATION OPERATION DRIVER



Bubble

MOTOROLA

SC42468

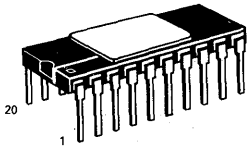
Advance Information

BUBBLE MEMORY COIL PREDRIVER

GENERAL DESCRIPTION

THE SC42468 Bubble Memory Coil Pre-driver is a monolithic CMOS integrated circuit which generates control signals for driving the X and Y field coils of a magnetic bubble memory device. The coil currents are switched through bridge configurations of complementary MOS Power FETs which are packaged separately. Basic control/timing signals are input to the coil pre-driver from the bubble memory controller.

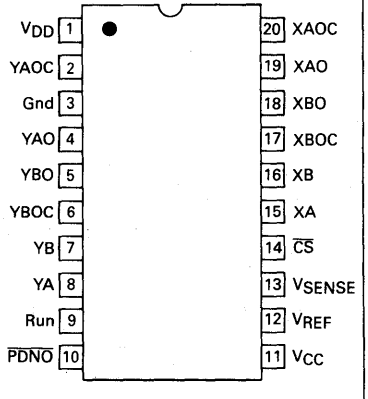
The Coil Pre-driver also contains under-voltage sensing circuits for the two bubble memory system power supply voltages. These circuits provide an interlock signal which can be used to provide an orderly shut-down so as to prevent loss of data in the event of a loss of D.C. power. The SC42468 is packaged in a 20-pin dual in-line package.



FEATURES

- Level Shift from TTL to Coil Drive Voltage
- High Load-Capacitance Drive Capability for Low-On-Resistance Power FET Coil Drivers
- Coils Grounded When not Operating
- Interlock Disables Operation Driver When Coils are not Being Driven
- Under-Voltage Detection and Interlock
- Chip Select Input for Multiple-Bubble Systems

PIN ASSIGNMENTS



20-pin Dual In-line
Package: 0.3-inch row spacing

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Value	Unit
Storage Temperature	−65 to +150	°C
Ambient temperature with power applied Commercial Device Extended-temperature Device	 0 to +70 −55 to +125	 °C °C
Voltage — V_{DD} and Coil Drive Outputs	−0.5 to +15	Volts
Voltage — any other pin to GND	−0.5 to +7.0	Volts
Output Driver Current	180	mA
Power dissipation	1.2	Watts

*Absolute Maximum Ratings indicate limits beyond which permanent damage may occur to the device. Proper operation of the device requires that it be limited to the conditions specified under DC Electrical Characteristics.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Bubble

PIN DESCRIPTIONS

Inputs

$\overline{CS}$ — Chip Select — enables operation of the coil pre-driver.

XA — X coil positive current enable.

XB — X coil negative current enable.

YA — Y coil positive current enable.

YB — Y coil negative current enable.

Supplies and Miscellaneous

V_{DD} — Coil driver supply voltage.

V_{CC} — Logic supply voltage.

V_{REF} — Reference voltage for sensing circuits.

V_{SENSE} — V_{DD} sensing input.

GND — System Ground.

Outputs

XAO — X-coil positive-current N-channel driver enable.

XAOC — X-coil positive-current P-channel driver enable.

XBO — X-coil negative-current N-channel driver enable.

XBOC — X-coil negative-current P-channel driver enable.

YAO — Y-coil positive-current N-channel driver enable.

YAOC — Y-coil positive-current P-channel driver enable.

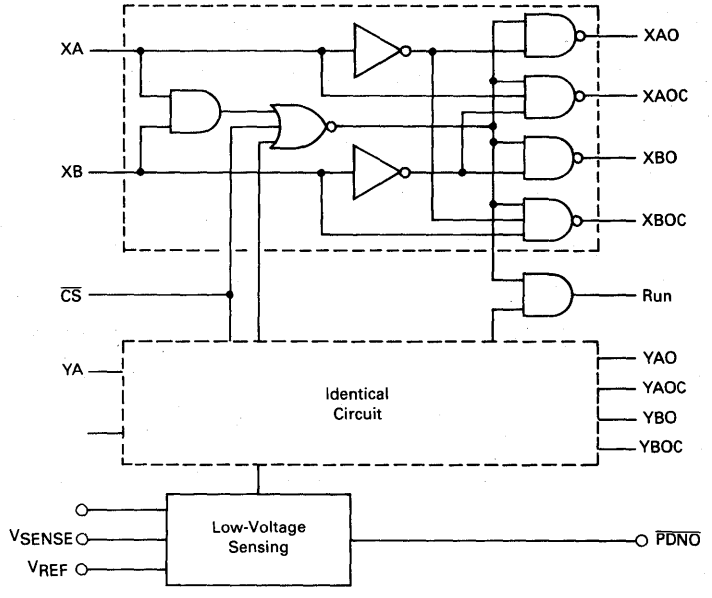
YBO — Y-coil negative-current N-channel driver enable.

YBOC — Y-coil negative-current P-channel driver enable.

RUN — Indicates that the X and Y coils are being driven — enables the operation driver.

$\overline{PDNO}$ — Power Down Output — indicates that at least one of the power supply voltages is below its minimum operating value.

FIGURE 1 — FUNCTIONAL DIAGRAM



Bubble

DC ELECTRICAL CHARACTERISTICS (V_{REF} = 2.50 V ±1%, T_A = 25°C)

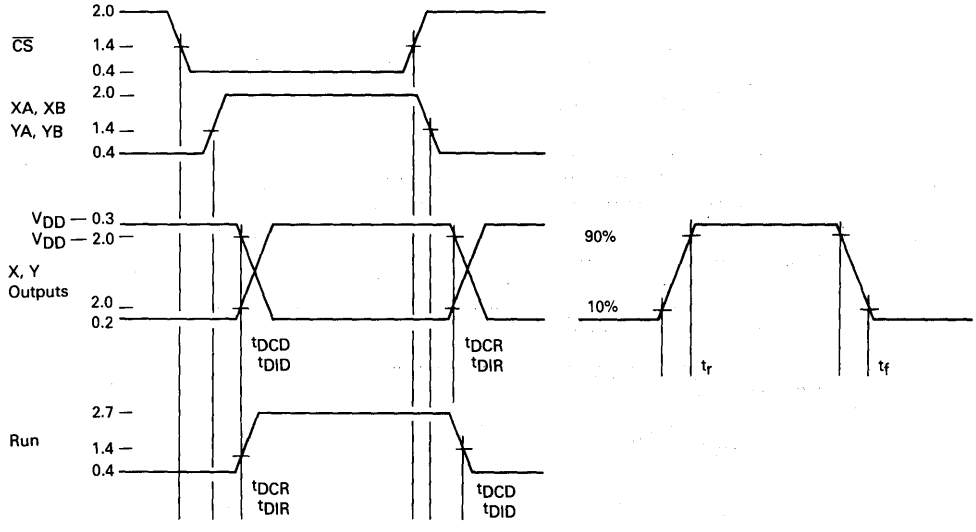
Parameter	Symbol	Min	Max	Unit
Coil Supply Voltage	V_{DD}	9.0	14.5	Volts
Logic Supply Voltage	V_{CC}	4.75	5.25	Volts
Current from V_{DD} (V_{DD} = 12.0 V, $\overline{CS}$ = 0)	I_{DD_1}	—	TBD	mA
Current from V_{DD} (V_{DD} = 12.0 V, $\overline{CS}$ = 1)	I_{DD_2}	—	TBD	mA
Current from V_{CC} (V_{CC} = 5.25 V)	I_{CC}	—	TBD	mA
Current from V_{REF} (V_{REF} = 2.525 V)	I_{REF}	—	TBD	μA
Logic High In Voltage (TTL)	V_{IH}	2.0	—	Volts
Logic Low In Voltage (TTL)	V_{IL}	—	0.8	Volts
Logic High Out Voltage (TTL) (I_O = −0.4 mA)	V_{OH}	2.7	—	Volts
Logic Low Out Voltage (TTL) (I_O = 1.6 mA)	V_{OL}	—	0.4	Volts
Logic High In Current (V_I = 2.7 V, V_{CC} = 5.0 V)	I_{IH}	—	20	μA
Logic Low In Current (V_I = 0.4 V, V_{CC} = 5.0 V)	I_{IL}	—	−40	μA
Driver High Out Voltage (CMOS) (I_{DOH} = −10 mA)	V_{DOH}	V_{DD} − 0.3	—	Volts
Driver Low Out Voltage (CMOS) (I_{DOL} = 10 mA)	V_{DOL}	—	0.2	Volts
Driver High Out Current	I_{DOH}	−250	—	mA
Driver Low Out Current	I_{DOL}	250	—	mA
Input Capacitance	C_{IN}	—	15	pF
V_{CC} Detection Threshold	V_{TCC}	TBD	TBD	Volts
V_{SENSE} Detect Threshold	V_{TS}	TBD	TBD	Volts
V_{CC} Power Up Enable	V_{ECC}	TBD	TBD	Volts
V_{DD} Power Up Enable	V_{EDD}	TBD	TBD	Volts

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 10.8 to 13.2 V, T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Output Rise Time (C_L = 450 pF)	t_r	—	35	ns
Output Fall Time (C_L = 450 pF)	t_f	—	35	ns
CS* to Driver Out (C_L = 450 pF)	t_{DCD}	—	300	ns
CS* to RUN Delay	t_{DCR}	—	300	ns
Other In to Driver Out (C_L = 450 pF)	t_{DID}	—	150	ns
Other In to RUN Out	t_{DIR}	—	TBD	ns

Bubble

FIGURE 2 — SIGNAL WAVEFORMS



OPERATION

The magnetic bubble memory device requires a rotating magnetic field which is produced by the interaction of two orthogonal (X,Y) coils mounted inside the package. A uniform rotating field would be produced by driving the coils with sinusoidal currents displaced by 90° in time. In actual practice, an approximately triangular current waveform is produced by applying a voltage pulse to each coil through transistor switches and allowing the inductance of the coil to integrate the voltage into a current ramp. The pulse duration is small relative to the time-constant of the coil and series transistors so that the current ramp is approximately linear.

Timing inputs to the Coil Pre-driver are provided to the XA, XB, YA, and YB pins. These signals are active-high and enable the application of voltage pulses to the coil driver FETs, which in turn enable current flow in the coils. XA and YA enable positive current flow; XB and YB enable negative current flow. Four output drive signals are provided for each coil, one for each of the four switch transistors in the bridge (two P-channel, two N-channel). These correspond to the four inputs and their logical complements except that if both X(Y) inputs go high, all four X(Y) outputs go high. This is the off state wherein all N-channel drivers are turned on thus grounding both ends of both coils. When either coil is in the off state (XA = XB = high, or YA = YB = high), the RUN output is held low to disable the Operation Driver.

Note that the "X" and "Y" halves of the circuit are identical as are the "A" and "B" portions within each half. This symmetry may be taken advantage of to simplify printed-circuit board layout in some cases by interchanging "X" and "Y" or "A" and "B."

The Chip Select $\overline{(CS)}$ input is active-low, and when false (high) overrides the timing inputs forcing the coil drivers into the off state, and places the Coil Pre-driver into a standby mode with reduced power consumption. Chip Select may be used to selectively enable one of a parallel-wired group of bubble memories, each with its own set of support circuits.

The Power Down $\overline{(PDNO)}$ signal is active-low and goes low whenever either V_{CC} or V_{DD} drops below its normal operating range. V_{CC} is sensed internally, but since V_{DD} is variable (dependent on the operating frequency) it is sensed through the V_{SENSE} pin using a voltage divider (R_1 and R_2) from V_{DD}. At nominal V_{DD}, V_{SENSE} should be 2.90 volts. When power is applied, $\overline{PDNO}$ is held low until both V_{CC} and V_{DD} have reached their operating values. $\overline{PDNO}$ has an open-drain output and may be externally wired-ored.

FIGURE 3 — TYPICAL COIL WAVEFORMS
(X-COIL IDENTICAL, PHASE SHIFTED)
(1) ASSUMING X-COIL ALREADY BEING DRIVEN

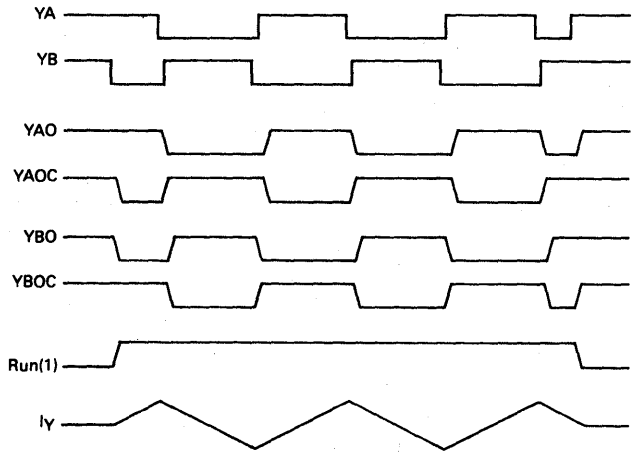
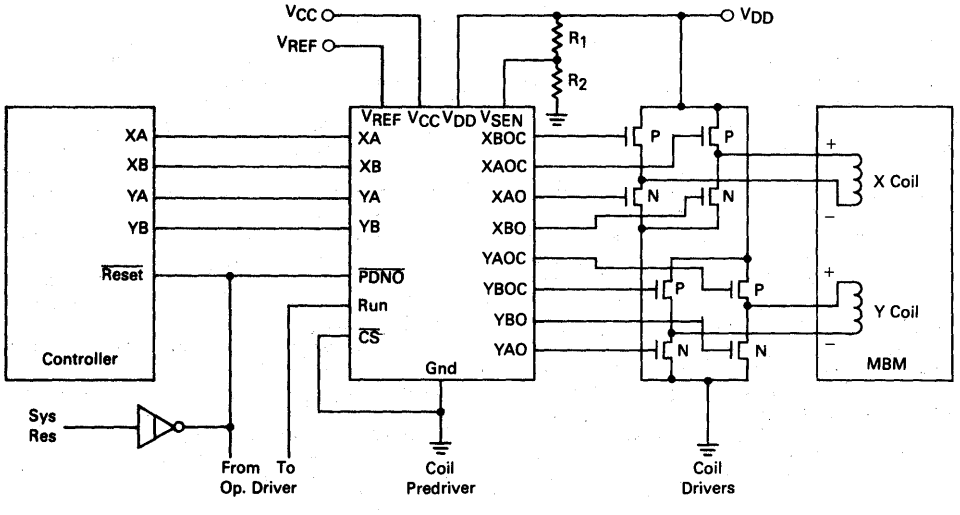


FIGURE 4 — TYPICAL APPLICATION



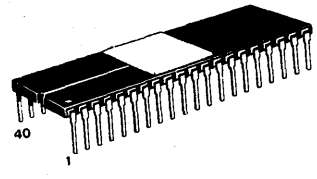
Bubble

MOTOROLA

SC42584
SC42585

Advance Information

BUBBLE MEMORY CONTROLLERS



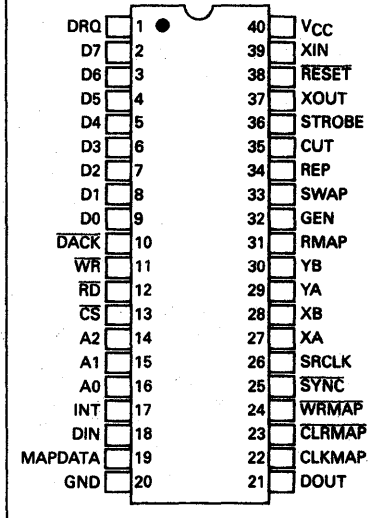
GENERAL DESCRIPTION

The SC42584 and SC42585 Bubble Memory controllers are monolithic HMOS integrated circuits which control the operation of the Motorola MBM2256 (256 Kilobit) and MBM2011 (1 Megabit) Magnetic Bubble Memories, respectively. They provide the interface between a Magnetic Bubble Memory (MBM) subsystem and the user system, including data and map loop read and write, redundant loop management, error correction, and all bubble memory timing. The SC42584 and SC42585 are functionally equivalent and pin-compatible. They differ only in data record length and bubble memory control pulse timing. They are packaged in 40-pin dual-in-line packages with 0.6-inch pin row spacing.

FEATURES

- Single-Chip Integrated Circuit
- Generation of All Bubble Memory Timing Signals
- Operation of 1 to 8 Bubble Memories in Parallel
- Complete Error Correction/Detection
- Dynamic Data Buffering of 16 Bytes
- Complete Redundant Loop Management
- Direct 8-bit Microprocessor Bus Interface
- Programmed, Interrupt, or DMA Data Transfer
- Power-Failure Interlock
- On-chip Crystal-Controlled Oscillator
- Simple Software Interface with Diagnostic Capability
- Bootloop Write with Mechanical Interlock

FIGURE 1 — PIN ASSIGNMENTS



40-pin dual in-line package;
0.6-inch row spacing

ABSOLUTE MAXIMUM RATINGS*

Characteristics	Value	Unit
Ambient temperature with power applied Commercial device Extended-temperature device	 0 to + 70 −55 to + 125	 °C °C
Storage Temperature	−65 to +150	°C
Voltage — any pin with respect to GND	−0.5 to + 7.0	Volts
Power dissipation	1.0	Watts

* Absolute Maximum Ratings indicate limits beyond which permanent damage may occur to the device. Proper operation of the device requires that it be limited to the conditions specified under DC Electrical Characteristics.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Bubble

PIN DESCRIPTIONS

User Interface

$\overline{\text{RESET}}$ — If a command is executing, initiates an orderly termination; resets and preconditions internal registers and control logic.

Data Bus (D7–D0) — Bidirectional transfer of data, commands, and status between the user system and the controller.

Address (A2–A0) — Selects one of eight internal registers for bus transfer.

$\overline{\text{CS}}$ — Chip Select — enables the user data-bus interface.

$\overline{\text{RD}}$ — Read Enable — enables reading from the addressed register in conjunction with $\overline{\text{CS}}$ or $\overline{\text{DACK}}$.

$\overline{\text{WR}}$ — Write Enable — enables writing to the addressed register in conjunction with $\overline{\text{CS}}$ or $\overline{\text{DACK}}$.

INT — Interrupt — programmable to indicate data request or command completion.

DRQ — Data Request — indicates that the contrller is ready for a data byte transfer to or from the user system.

$\overline{\text{DACK}}$ — Data Acknowledge — enables a transfer between the bus and the data buffer in conjunction with $\overline{\text{RD}}$ and $\overline{\text{WR}}$ but independent of A2–A0.

External Map Memory Interface

MAPDATA — Data from external redundancy-map memory.

$\overline{\text{CLRMAP}}$ — Initializes (clears to zero) the redundancy-map memory address counter.

CLKMAP — Rising edge increments the redundancy-map memory address counter.

$\overline{\text{WRMAP}}$ — Enables writing data from the MBM(s) to the redundancy-map memory.

Supplies and Miscellaneous

XIN
XOUT — Crystal connections for controller clock oscillator. Alternatively, XIN may be driven with an externally-generated square wave at standard TTL levels, in which case, XOUT should be left unconnected.

V_{CC} — Power supply voltage: 5 V ± 5 percent.

GND — System ground.

Bubble Memory Interface

DIN — Data In — serial data from MBM sense amplifier (single-MBM bank) or parallel-to-serial shift register (multiple-MBM bank).

DOUT — Data Out — serial data to MBM operation driver (single-MBM bank) or to serial-to-parallel shift register (multiple-MBM bank).

STROBE — Data timing signal — defines sample window for sense amplifier. Trailing edge latches detected data in sense amplifier. Leading edge latches data into operation driver in single-MBM bank.

$\overline{\text{SYNC}}$ — Data timing for multiple-MBM bank. Loads data from sense amplifiers into a parallel-to-serial shift register. Trailing (rising) edge clocks data from a serial-to-parallel shift register into the operation driver(s).

SRCLK — Clock for shift registers used in a multiple-MBM bank. Rising edge advances shift registers. Falling edge internally samples data on DIN or changes data on DOUT.

GEN — Generate
SWAP — Swap
REP — Replicate
RMAP — Replicate Map
CUT — Cut

Timing signals to operation driver which control the corresponding currents. Cut current is produced by the conjunction of CUT and REP or CUT and RMAP.

XA — X coil positive current enable.
XB — X coil negative current enable.
YA — Y coil positive current enable.
YB — Y coil negative current enable.

When the −A and −B signals are both high, the corresponding coil is off and both ends are grounded.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Volts ±5% unless otherwise specified.)

Parameter	Symbol	Min	Max	Unit
Input Low Voltage	V_{IL}	−0.5	0.8	V
Input High Voltage	V_{IH}	2.0	V_{CC}+0.5	V
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −500 μA)	V_{OH}	2.4	—	V
V_{OH} for XA,XB,YA,YB (1)	V_{COH}	2.4	—	V
XIN Input Low Voltage	V_{XINL}	−0.5	0.4	V
XIN Input High Voltage	V_{XINH}	2.4	V_{CC} + 0.5	V
Input Current (V_{IN} = 0 to V_{CC})	I_{IL}	—	10	μA
Output Off-state Current (V_{OUT} = .45 to V_{CC})	I_{OZ}	−10	10	μA
V_{CC} Supply Current (V_{CC} = 5.25 V)	I_{CC}	—	150	mA

(Note 1) V_{CC} = 5 V, I_{OH} = − 0.5mA
V_{CC} = 2.8 V, I_{OH} = −0.1mA

AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Clock Period	t_{CY}	100	333	ns
Clock High Time	t_{CH}	0.4	0.6	t_{CY}
Clock Rise Time	t_{CR}	—	25	ns
Clock Fall Time	t_{CF}	—	25	ns
$\overline{\text{RESET}}$ Pulse Width	t_{WRE}	64	—	t_{CY}
Reset Disable Delay	t_{DRD}	—	192	t_{CY}
DRQ Turn Of Delay	t_{DDR}	—	300	ns
INT Turn Off Delay	t_{DIN}	—	150	ns
$\overline{CS}$ & Address Set Up	t_{AS}	25	—	ns
$\overline{CS}$ & Address Hold	t_{AH}	0	—	ns
Time Between Successive $\overline{RD}$ Pulses	t_{ROFF}	2.0	—	t_{CY}
Read Data Delay (C_L = 30 pF)	t_{DDR}	—	250	ns
(C_L = 100 pF)		—	300	ns
Data Bus Turn Off (C_L = 20 − 100 pF)	t_{DZ}	20	100	ns
$\overline{WR}$ Pulse Width	t_{WW}	200	—	ns
Time Between Successive $\overline{WR}$ Pulses	t_{WOFF}	2.0	—	t_{CY}
Write Data Set Up	t_{DSW}	25	—	ns
Write Data Hold	t_{DHW}	25	—	ns
DIN, MAPDATA Set Up	t_{DIS}	50	—	ns
DIN, MAPDATA Hold	t_{DIH}	50	—	ns
DOUT Delay	t_{DOD}	—	100	ns

BUBBLE MEMORY DEVICE OPERATION

The magnetic bubble memory (MBM) device stores data as the presence or absence of locally-polarized domains referred to as bubbles in a thin film of magnetic garnet material. A pattern of magnetic material on the surface defines stable locations for the bubbles and paths between them. A rotating magnetic field is produced in the plane of the film by two orthogonal coils within the MBM package. One cycle of field rotation advances all bubbles one position on their respective tracks. The field may be stopped at the end of any cycle, and the bubbles will remain in place.

The data storage area is organized as a number of closed storage loops. Input and output tracks carry bubbles to and from the storage loops and are interconnected with the loops at opposite ends by swap and replicate gates respectively. One physical page of data consists of one bit from each of the storage loops. Figure 2 is a functional diagram of the MBM. Actual implementation may be different. Table 1 gives the MBM capacities.

A generator creates bubbles in the input track as required to write data into the MBM. When a number of data bits equal to the number of storage loops has been entered into the input track and shifted into alignment with the loops, a swap pulse is applied which interchanges each bit in the input track with one bit in the adjacent storage loop. The bits swapped out are shifted to the end of the input track and annihilated.

To read data non-destructively, a replicate-cut-transfer pulse is applied. This pulse causes a stretched bubble at the replicate gate of each storage loop to be cut into two full-sized bubbles with the trailing bubble transferred to the output track while the leading bubble remains in the storage loop. Bubbles in the output track are then shifted to the detector which consists of a matched pair of magneto-resistive elements. Bubbles pass beneath the active detector element causing a change in its resistance, and are then destroyed. A constant current passed through the detector converts the resistance change into a voltage change. The reference detector element provides cancellation of noise induced by the rotating field, through the use of differential detection.

In order to improve MBM device yields, extra redundant storage loops are provided, and the device is permitted to have a limited number of non-functioning loops. Since data transfer between the controller and the MBM is bit serial, if the controller knows the locations of the non-functioning loops, it can skip over them. For this purpose, two additional storage loops are provided, one of which is loaded at the factory with a map of the useable data loops; the other is empty. The map loops communicate with the same input and output tracks as the data loops, but have separate control inputs for replicate and transfer-in (the map write function does not perform a true swap).

SYSTEM DESCRIPTION

The Magnetic Bubble Memory Controller provides the complete interface between a user system and a magnetic bubble memory subsystem. The user communicates with the controller via an eight-bit parallel bidirectional data bus which carries commands, data, status, and associated control information. This data bus is designed to connect directly to a microprocessor system. The controller contains eight internal registers which can be mapped via three address lines directly into memory locations or I/O ports in the user system.

The controller is specifically designed to interface with the following Motorola bubble memory devices and support circuits:

- MBM2256 and MBM2011 Magnetic Bubble Memories — 256 kilobit and one megabit devices respectively.
- SC42468 Coil Pre-driver — provides the necessary drive for the X and Y coil drivers (MOS power FETs) and also provides power supply low-voltage detection.
- MC34046 and MC34047 Operation Drivers — provide the generate, swap, replicate, and map replicate current pulses for the MBM2256 and MBM2011 respectively.
- MC34044 Sense Amplifier — provides the detector bias currents and bubble signal detection.

The controller can operate 1, 2, 4, or 8 MBMs in parallel, each with its own support circuits. Parallel operation multiplies the single-MBM physical page size and data transfer rate by the number of MBMs operated (1, 2, 4, or 8). Consecutive data bits are written to and read from adjacent MBM devices cyclically; therefore each data record is distributed across all the MBMs. Single and multiple MBM systems are shown in Figures 3a and 3b.

The controller can be interfaced to several banks of MBMs, each containing multiple MBMs (not necessarily the same number). This is accomplished by using the chip select inputs on the support devices to enable one bank at a time using an externally latched and decoded address. The controller operates the various banks independently, and it must be reinitialized whenever the active bank is changed. A multiple-bank system is shown in Figure 3c.

A multiple-MBM bank requires additional components as follows:

1) an eight-bit serial-to-parallel shift register which receives data from DOUT clocked by SRCLK, and from which data is transferred in parallel to the operation drivers by $\overline{\text{SYNC}}$. Banks of two or four MBMs use the positions corresponding to the first bits shifted in.
2) a parallel-to-serial shift register which receives data from the sense amplifiers enabled by $\overline{\text{SYNC}}$ and shifts the data to DIN clocked by SRCLK. The bit length need be only as great as the number of MBMs.

The controller accepts only the first two or four bits shifted in for corresponding bank sizes.

3) an external redundancy-map memory and address counter (not required for two MBM2256s) to augment the controller's internal map memory. This memory subsystem is connected as shown in Figure 4. It uses the following controller signals which are described under PIN DESCRIPTIONS: $\overline{\text{CLRMAP}}$, CLKMAP, $\overline{\text{WRMAP}}$, and MAPDATA. The memory is configured as one bit wide, and is written and read serially. Map memory timing is shown in Figure 9.

In some applications, the user may wish to have the redundancy map data permanently stored in a PROM. This may be done using the configuration described in 3). In this case, the controller's internal map memory is not used.

CONTROLLER OPERATION

A block diagram of the main functional components of the controller is given in Figure 5.

User Interface

The user interface is directly compatible with many 8-bit microprocessors. The data bus provides user communication with any of the eight internal registers as selected by the address input. The INT signal can be used to interrupt the processor to request data or to indicate command termination. The DRQ and $\overline{\text{DACK}}$ signals can interface to a separate Direct-Memory-Access controller. These functions are described in detail under PROGRAMMING INFORMATION.

Data Path

The DATA BUFFER provides sixteen bytes of dynamic buffering between the user and the bubble memory subsystem. Bytes are transferred in parallel between the buffer and the SHIFTER which performs the serial-to-parallel conversion on data read from the MBM(s) through DIN or the parallel-to-serial conversion on data to be written to the MBM(s) over DOUT.

When writing, the OUTPUT MAPPER inserts zeros into the data stream at positions corresponding to the unused loops. The INPUT MAPPER deletes the corresponding bits from the input stream when reading. The redundant loop map is accessed from the MAP MEMORY during these operations and provided to the mappers. The ERROR CORRECTION circuit generates check bits and inserts them into the data stream when writing, and checks these bits when reading. It is capable of correcting any single burst of errors up to three bits long via the READ CORRECTED command.

The redundancy-map data is usually stored in one of the two separate map loops in the MBM. The controller reads this data during initialization, and stores it in the MAP MEMORY from which it is retrieved during data read and write operations. The controller has on-chip map memory sufficient to store the map for one MBM2011 or two MBM2256s. For multiple-MBM banks, additional external memory is required; the controller provides all the control signals necessary to operate this external memory.

Alternatively, the map data can be permanently stored in an external PROM or a completely external RAM may be used. In either case, the entire map is read from the external memory, and the internal map memory is not used.

The map loop also contains a synchronization pattern which is used to locate sector/page zero during initialization. The map loop is normally loaded at the factory and need only be read to initialize the controller. However, commands are provided to read and write the map loops for diagnostic purposes or to change the map loop contents. Since the map loop write uses a transfer-in rather than a swap function, the MBM must be erased using the Z-coil or an external magnetic field prior to a map write. The map transfer-in pulse is generated on the SWAP pin. A switch is required as shown in Figure 6 to properly route the current pulse to the MBM. This switch also protects against accidental destruction of the map data by an unintentional map write.

Redundant loop data are stored in alternate bit positions in one of the map loops in the MBM. The intervening bit positions and the other map loop must contain all zeros (no bubbles). All map operations access only alternate map bits so the intervening zeros are not seen by the controller. (Initialization may start in the wrong phase and read only the intervening zeros. In this case, it automatically shifts one position and rereads.) Data from the two map loops are merged when reading so that loop selection is not required. The WRITE MAP command allows specification of the desired loop.

The format of the map loop data is shown in Table 3.

Bubble Memory Data and Timing

All the necessary MBM coil drive and function-gate timing signals are generated by the controller. The coil drive timing signals are sequenced on and off so as to start and stop the drive field in the proper phase. Data to and from the MBM(s) are transferred bit-serial. The signals STROBE, $\overline{\text{SYNC}}$, and SRCLK are provided to clock this data. Control timing is given in Figure 10 and Table 4.

Oscillator

An on-chip oscillator provides the internal time base to operate the controller when connected to an external crystal as shown in Figure 7. Alternatively, XIN can be driven from an external oscillator and XOUT not used. The crystal or external oscillator frequency is 64 times the coil drive frequency.

Reset and Power-Down

The $\overline{\text{RESET}}$ pin provides internal preconditioning of

the controller logic on power-up or other system reset conditions and also acts as a power-down interrupt which provides an orderly termination of any operation in progress with no loss of data in the MBMs.

$\overline{\text{RESET}}$ initializes the registers as follows (hexadecimal values):

LPC:	0000	
CMDR:	FF	(TERMINATE)
MSR:	01	
SAR:	0000	
RCR:	00	
SFR:	00	
STR:	C1	(while $\overline{\text{RESET}}$ is active)
	01	(after $\overline{\text{RESET}}$ is removed)

The system must be initialized after a reset to synchronize the MBM(s) with the controller. The user should load the SFR according to the system configuration, and then execute an INITIALIZE command.

When $\overline{\text{RESET}}$ is brought low, the controller ensures that all control pulse and coil drive signals are properly sequenced to the off condition so that no data is destroyed in the MBMs. This will occur within three magnetic cycles after $\overline{\text{RESET}}$ goes low. Data being written will usually not have been swapped in, and will have to be rewritten when the system is restarted. Note that if $\overline{\text{RESET}}$ is generated due to detection of low DC voltage, the power supply voltages may already be out of their specified operating ranges, and proper MBM operation may not be guaranteed. The user should provide input power detection or other means of sustaining DC voltages to minimize the chance of data loss.

Error Detection and Correction

In order to ensure the integrity of the data stored in the bubble memory system, the controller employs error detection and correction circuitry which operates automatically, and is in general transparent to the user.

During a normal WRITE DATA operation, the controller calculates and appends a 12-bit error correction code (ECC) field onto each block of 512 bits (64 bytes) written. Extra minor loops are provided in the MBMs for this field. The ECC used is a Fire Code which permits the identification and correction of any single burst of errors up to three bits long.

During a READ DATA operation, the controller recalculates the ECC field to verify the data. If an error is detected, the controller stops (provided the Stop on Error bit is set) and indicates the error in the status register. It also saves the ECC syndrome and data block address to enable re-reading (and error correction) of the erroneous block.

Two types of errors can occur:

1) Soft errors — due to transient phenomena in the detection and sense circuitry. The data in the memory is good and can usually be re-read correctly.
2) Hard errors — due to incorrect data in the MBM(s). The READ CORRECTED command rereads the erroneous block and sends corrected data to the user in most cases. The data should then be re-written to the MBM(s) to correct the memory contents.

Soft and uncorrectable errors are detected and indicated only by the READ CORRECTED command. If an error is detected during a READ DATA command with Stop on Error set, the controller saves the calculated ECC syndrome. The READ CORRECTED command uses two separate ECC circuits: one attempts to do error correction using the error syndrome, the other recalculates the syndrome on the raw data received from the MBM(s). This recalculated syndrome is compared to the saved syndrome from the READ DATA. If they are not equal, the Soft Error bit is set indicating that the data reread was *not the same as the originally-read data.* If the error-*correction* circuit does not find a correctable error, the Uncorrectable Error bit is set.

If a soft error occurs, the error-correction circuit cannot function properly. However it may have been "fooled" and changed some data. Therefore the data received during READ CORRECTED with a soft error indication should be ignored, and the data reread with the READ DATA command.

Hard errors are rare, and the block structure of the MBM, and interleaved operation of multiple MBMs causes most hard errors to be correctable, i.e. a hard failure in a single minor loop affects only one bit in any ECC block (except for a single MBM2256 system).

The controller also calculates and inserts an ECC field during a WRITE MAP operation. This field is checked during the INITIALIZE (L=1) and READ MAP (C=1) operations; however error correction is not performed for the map data.

The ECC details and capabilities are summarized in Table 5.

PROGRAMMING INFORMATION

Nine basic commands with 24 options provide total control of the bubble memory subsystem. The user stores a command into the command register, transfers data bytes as required, then checks the controller status to verify proper completion of the operation.

Registers

Eight registers are directly accessible by the user via the data bus. The desired register is selected by the three-bit address on A2–A0 when $\overline{\text{CS}}$ is true (low). (DATA can also be selected by $\overline{\text{DACK}}$.) All are read-write except the STR which is read only.

While a command is executing (READY = 0), writing is inhibited except to DATA and to CMDR bits 1&0; therefore only a Terminate (Immediate) command can be accepted (CMDR bits 7–2 will not be altered). The registers are summarized in Table 6.

Symbol (Address)	Name and Use
CMDR (000)	— Command Register — loaded by the user with the command to be exe-

cuted by the controller (see Commands).

MSR (001) — Multiple Sector Register — loaded by the user with the number (0 indicates 256) of sectors/pages to be read or written by the subsequent multiple sector READ DATA or WRITE DATA command (not used for single sector commands).

SARL (010) SARH (011) — Sector Address Register, two bytes, L=Low-order 8 bits, H=high-order bits — loaded by the user with the address of the (first) sector/page to be read or written by the subsequent (multiple sector) command.

RCR (100) — Residual Control Register — selects various options which apply to subsequent commands. Individual bits provide specific options as follows:

Bit	Function
7	Not used, always zero.
6	Read Buffer Enable — used primarily for diagnostic functions. This bit must be set to 1 if it is desired to read from the data buffer when no command is in progress. Otherwise, the buffer may be written into, but not read from. For proper operation, it must be reloaded with a 0 before initiating a subsequent command. 0: Buffer is write-only between commands. 1: Buffer is read-only between commands.
5	Stop on Error — causes the controller to terminate any READ DATA command at the end of any ECC block in which a data error was detected. The ECC logic, SAR, and MSR are left in the proper state for execution of a READ CORRECTED command.
4	Half Buffer — causes DRQ to be set only when the buffer is at least half full* (READ) or half empty (WRITE). When Half Buffer is set to 1, data may be transferred in 8-byte bursts in response to DRQ. The setting of DRQ according to Half Buffer and the number of bytes in the buffer is as follows: HB READ WRITE 0: ≥ 1 byte ≤ 15 bytes 1: ≥ 8 bytes* < 8 bytes *or at end of command if buffer is not empty.
3	Enable READY Interrupt — causes INT to be activated at the termination of any command. INT is cleared by reading STR or writing CMDR. May be set concurrently with bit 2.
2	Enable DRQ Interrupt — causes INT to be activated whenever DRQ is true. May be set concurrently with bit 3.
1	Page Addressing Mode — (see Sector/Page Addressing)- 0: Sector Addressing Mode (default). 1: Page Addressing Mode.
0	Write Protect — prevents any WRITE command from being executed. A write protect error will be indicated if any WRITE (Map or Data) is attempted with Write Protect = 1.

SFR (101) — System Features Register — defines the system configuration. Functions of the individual bits are as follows:

Bit	Function
7–3	Not used, always zero.
2	External Map — indicates that all map data is to be stored or is pre-stored in the external map memory (RAM or PROM). The controller does not use its internal map storage.
1, 0	Bank Size — specifies the number of MBMs in the active bank as follows: 00: 1 MBM, 01: 2 MBMs, 10: 4 MBMs, 11: 8 MBMs

STR (110) — Status Register (Read Only) — indicates the status of the command in progress or last ended — cleared when CMDR is loaded (except TERMINATE when busy) or by $\overline{\text{RESET}}$. Certain bits pertain only to specific commands or are defined differently for different commands. The meanings of the bits are as follows:

Bit	Command	Meaning
7	RDC	Soft Error — the recomputed ECC syndrome did not match the previous syndrome (see Error Correction/Detection).
6	WRD,WRM	Write Protect bit is set — command not executed.
7&6	—	$\overline{\text{RESET}}$ pin is active (low).
5	RDD,WRD	Sector/page Address Out of Range for the number of MBMs specified.
	RDM (C=1)	Map compare error — the data read from the

Bubble

		MBM(s) did not match that in the map memory.
	INIT	Initialization error — synchronization pattern could not be found.
4	RDC	Non-correctable error.
3	all READS	Data Error detected (ECC). For RDC command, indicates that error is in a different block than previous error.
2	all READS and WRITES	Data Buffer overrun — the user did not read/write the data buffer fast enough to keep up with the MBM data transfer rate, or the user attempted to read/write the buffer when DRQ = 0.
1	all RD & WR	Data transfer request (DRQ).
0	all	Ready — previous command has terminated and controller is ready to receive a new command.
DATA (111)		Data buffer — a 16-byte first-in-first-out (FIFO) buffer used for all data transfers.

Sector/Page Addressing

A *page* of data corresponds to a single physical read or write of the MBM(s) — therefore, the page length is determined by the MBM type (256K or megabit) and the number of MBMs specified in the SFR. The number of pages in a bank is independent of the number of MBMs, and is determined only by the MBM type.

Note: A minimum block size of 64 bytes is required for the ECC. Therefore, a single 256K-bit bank utilizes two physical pages per logical page.

A *sector* is a fixed-length record independent of the number of MBMs specified in the SFR and is equal to the maximum-length page for the MBM type. Therefore, the number of sectors in a bank is proportional to the number of MBMs.

Sector addressing is selected by default. Page addressing may be selected by setting the Page Mode bit = 1 in the RCR. Sector and page addressing are equivalent for a maximum bank of 8 MBMs.

Regardless of the mode or number of MBMs, error detection/correction is performed on blocks of 512 bits (64 bytes). In general, there are multiple ECC blocks within a sector/page.

Table 7 shows the sector and page sizes and counts for all configurations.

Logical Addressing

Propagation of the bubbles along the input or output track causes the data loops to be shifted an equal distance. Thus, following a replicate and clearing of the output track, the physically adjacent page has propagated well past the replicate gates; a similar affect occurs during consecutive writes. In order to provide minimum access time when reading or writing consecutive pages/sectors, the controller uses a logical addressing scheme such that consecutive logical pages are spaced several physical locations apart to account for the latency described above. This spacing is given in Table 8.

The controller maintains the current logical page/sector address in the Logical Page Counter (LPC), a non-accessible register which is incremented by the appropriate value during each active MBM cycle. The LPC is compared to the SAR to locate the desired page/sector for READ & WRITE commands. To synchronize the LPC with the MBM contents, the INITIALIZE or CLEAR LPC command should be used. $\overline{\text{RESET}}$ also clears the LPC to zero regardless of MBM position.

The timing of the WRITE DATA command is such that consecutive commands to consecutive logical addresses (without reloading the SAR) will be accomplished with minimum latency. During a multiple-page/sector READ DATA command, replicates are performed "on the fly" as each logical page reaches the replicate position; however the extra propagation distance between the replicate gates and the detector means that at the termination of a READ DATA command, the next logical address has passed the replicate position. The POSITION READ command will give minimum access time when consecutive logical pages/sectors are to be read with single-page/sector commands.

Commands

The user initiates operation of the controller by writing a command byte into the command register (CMDR). The various commands are described below and summarized in Table 6. For each command, the value to be loaded into the CMDR is given in binary with certain option bits which affect its operation. Use of the SAR and MSR is described where applicable. These registers, when used, as well as the SFR and RCR, must be loaded prior to loading the CMDR.

Data Transfer

All data transfers are made to/from the data buffer which is accessed as register 7. During a read or write command execution, when the controller determines that a data transfer is required, it does the following:

1) sets the DRQ bit in the status register.
2) raises the DRQ pin to the active (high) state.
3) if RCR bit 2 (Enable DRQ Interrupt) is set, raises the INT pin to the active (high) state.

Any of these conditions may be recognized by ap-

propriate software or hardware as indicating that data transfer is required. The user then transfers one or more bytes to or from the buffer using $\overline{WR}$ or $\overline{RD}$ and either of the following:

1) addressing Register 7 ($\overline{CS}$=0, A2,A1,A0 = 111).

2) activating $\overline{DACK}$ ($\overline{CS}$=1, $\overline{DACK}$=0, A2–A0 ignored).

The DRQ and $\overline{DACK}$ signals may be used with a separate direct memory access (DMA) controller. DRQ and INT (if used) remain active as long as data transfer is required.

If the RCR Half Buffer bit is set to 1, then eight bytes can always be transferred in a burst when a DRQ occurs.

Notes:

The WRITE DATA (S=0) AND WRITE MAP commands do not begin execution until the first data byte has been written into the data buffer. When using programmed data transfer, the user should always load the first 16 data bytes in a burst as fast as possible so as to provide adequate buffering for the operation. (It is not necessary to check DRQ since the buffer is known to be empty at the start of the command.)

Due to the asynchronous operation of the data buffer, the controller always attempts to keep it full during a write operation. As a result, it may request up to 16 additional bytes at the end of a write depending on the user system response time. Response to these extra DRQs is optional: extra bytes transferred will not be written to the MBM(s); ignoring the DRQ will not cause an error.

Termination and Status

When the command execution is finished, the controller:

1) sets the Ready bit and any other bits which are appropriate in the status register.
2) if RCR bit 3 (Enable Ready Interrupt) is set, raises the INT pin to the active (high) state.

The user should read the status register to verify proper completion of the previous command and take any corrective action indicated. Ready indicates that the controller is able to accept a new command.

INT, if used, is cleared by reading the status register or loading the command register.

Command Descriptions

INITIALIZE (INIT) CMDR= 1111 L100

Read the map loop until the synchronization pattern (64 ZEROs followed by a ONE is detected, then set the logical page counter (LPC) to zero. Then if L=1, load the redundancy map memory with the map data.

If the synchronization pattern is not found after one complete cycle of the map loop, the map loop is shifted one position and a second attempt is made reading the interleaved bits.

INITIALIZE should be executed after any of the following:

1) Power off-on.
2) Reset.
3) Bank switching or MBM change.

Page synchronization is then maintained until any of the above conditions occurs. The Load Map Memory (L=1) option should be used unless it is not desired to use the redundant-loop map or the map has been prestored in an external PROM.

Register usage: None.

Errors detected:
Initialization error — the synchronization pattern could not be found on either pass.
Data error — an ECC error was detected when reading the map data.

CLEAR LPC (CLPC) CMDR = 0010 0000

Clear the Logical Page Counter (LPC) to zero without accessing the MBM(s) or loading the map memory. Permits the user to synchronize the controller to sector/page zero without using the map loop(s), e.g. by recognizing a page with a unique data pattern.

Useful in systems where the map data are stored in an external PROM and the bulk erase capability of the MBM is utilized, since bulk erase will destroy the synchronization pattern along with the data.

POSITION (POS) CMDR= 0W10 1000

Position the MBM data for minimum access time for a subsequent READ DATA (W=0) or WRITE DATA (W=1) command. RDD and WRD will automatically position the MBM(s) if required; POS minimizes the latency at the time the RDD or WRD is executed.

Register Usage:

Start: SAR: Address of sector/page to be read or written by a subsequent command.

End: SAR: Unchanged. **The SAR should not be reloaded prior to issuing the RDD or WRD command, even with the same address, or the effect of POS will be lost and the RDD or WRD access time will be excessive.**

WRITE DATA (WRD) CMDR= 010M US00

Write one or more sectors/pages of data. Positioning is performed if the MBM(s) have not been pre-positioned.

M=0: Write one sector/page.
M=1: Number of sectors/pages is specified in MSR.

U=S=0: Normal Write — user sends only data bits; zeros are inserted for redundant loops, and ECC bits are generated and appended.
U=1,S=0: Unmasked Write — user sends data for all loops including redundant and ECC bits.
U=0,S=1: Suppress Transfer — the 16 bytes currently in the buffer are written repeatedly, with redundant loop and ECC bits inserted as in a normal write; the user does not send data.
U=S=1: NOT ALLOWED.

Register Usage:

Start: SAR: Address of (first) sector/page to be written.
MSR: M=0: Not used.
M=1: Number of sectors/pages to be written.

End: Norm: SAR: Address of last sector/page written + 1.
MSR: M=0: Unchanged.
M=1: MSR=1.

Error: SAR: Address of the sector/page having the error.
MSR: M=0: Unchanged.
M=1: Number of sectors/pages still to be written including the one with the error.

Errors detected:

Write protect — write protect bit is set; WRD is not executed.
Out of Range — if the initial address is out of range, the command is not executed; if a command attempts to write past the end of the installed memory, the command terminates after the last allowable sector/page.
Overrun — the command is terminated immediately.

READ DATA (RDD) CMDR= 000M US00

Read one or more sectors/pages of data. Positioning is performed if the MBM(s) have not been pre-positioned.

M=0: Read one sector/page.
M=1: Number of sectors/pages is specified in MSR.
U=S=0: Normal Read — redundant loops and ECC are masked and remaining bits are sent to the user; ECC is checked and errors reported.
U=1,S=0: Unmasked Read — all bits are sent to the user; ECC is not checked.
U=0,S=1: Suppress Transfer — data are not sent to the user; ECC is checked and errors reported.
U=S=1: NOT ALLOWED (= RDC command).

Register Usage:

Start: SAR: Address of (first) sector/page to be read.
MSR: M=0: Not used.
M=1: Number of sectors/pages to be read.

End: Norm: SAR: Address of last sector/page read + 1.
MSR: M=0: Unchanged.
M=1: MSR=1.

Error: SAR: Address of sector/page having the error.
MSR: M=0: Unchanged.
M=1: Number of sectors/pages still to be read including the one with the error.

Errors detected:

Out of Range — if the initial address is out of range, the command is not executed; if a command attempts to read past the end of the installed memory, the command terminates after the last allowable sector/page.
Data Error (ECC) — if Stop on Error is set, data transmission to the user stops immediately following the 64-byte ECC block in which the error is detected.
Overrun — the command is terminated immediately.

READ CORRECTED (RDC) CMDR= 0000 1100

Reread the page in which an error was detected and apply error correction to the erroneous block. Only valid immediately following a READ DATA command with a Data Error indication and with the Stop On Error bit set in the RCR.

Corrected data are sent to the user starting at the beginning of the 64-byte ECC block in which the error was detected and continuing to the end of that sector or page; i.e. the last 64 bytes sent by the RDD are repeated with error correction, and the sector or page is completed. A soft or uncorrectable error in the first block or a data error in a subsequent block will be indicated if detected, but the sector/page will be completed regardless of errors or the Stop On Error bit. See *Error Detection and Correction.*

Register Usage:

Start: No registers may be loaded between the end of READ DATA and the issuing of READ CORRECTED.

End: Norm: SAR: Address of next sector/page.
MSR: Remaining sector/page count.

Error: SAR & MSR: Unchanged.

Errors detected:

Soft error — the recalculated ECC syndrome did not match the saved syndrome.
Uncorrectable error — the error was not correctable.
Data error — an error was detected in another ECC block.
Overrun — the command is terminated immediately.

TERMINATE (TERM) CMDR= XXXX XX1I

Terminate the current operation at the end of the current page (I=0) or terminate immediately (I=1). TERMINATE permits aborting of any command in progress at any time.

If the controller is not busy, TERMINATE is treated as a no-op, except for resetting the buffer pointers.

Register Usage: Buffer (FIFO) pointers are reset.

Errors detected: Depends upon the command being executed.

READ MAP (RDM) CMDR= 1000 C000

Read the map loop data and send to the user. The order of the data read is as shown in Table 3 grouped into 8-bit bytes with the first bit being the most-significant bit in the byte. In a multiple-MBM system, bits from the MBMs are interleaved.

C=0: The entire map loop contents (64 or 128 bytes) are sent to the user. Error detection is not performed.

C=1: Check Data — only the M-field and ECC-field are sent to the user; ECC checking is performed, and the map data (M-field) are compared to the contents of the map memory. Errors are reported.

Register usage: none.

Errors detected:

Map compare error (C=1 only) — the data read from the map loop did not match that stored in the map memory.
Data error (C=1 only) — an ECC error was detected (map error correction is not performed by the controller).
Overrun — the command is terminated immediately.

WRITE MAP (WRM) CMDR= 1100 N000

Write map loop 1 (N=0) or 2 (N=1) with user-supplied data. The user must supply the entire map loop contents (64 or 128 bytes per MBM) including the sync pattern as described under READ MAP. However, the ECC-field bits are ignored and replaced by ECC bits generated by the controller.

Register usage: None.

Errors detected:

Write protect — the write protect bit is set; WRM is not executed.
Overrun — the command is terminated immediately.

Note:
WRITE MAP will execute in a multiple-MBM system but will not generate correct ECC bits for multiple MBMs. It is intended for loading the map in a single MBM only. The MBM must first be erased using the Z-coil or a suitable external magnetic field. The MBM map pins must be connected as shown in Figure 6.

TABLE 1. BUBBLE MEMORY CAPACITIES

	MBM2256	MBM2011
Number of data loops:	282	584
Number of redundant loops:	20	60
Number of loops used for ECC:	6*	12
Number of usable data loops:	256	512
Number of bits per loop:	1024	2048
Number of bits of data storage:	262,144	1,048,576
Number of map loops:	2	2
Number of bits used in map loops:	512	1024

* Actually 12 bits in every other physical page.

TABLE 2. EXTERNAL MEMORY REQUIREMENTS

MBM Type	Number of MBMs	External Memory Required (bits) SFR bit 2 = 0	1
2256	1	0	282
	2	0	564
	4	534	1128
	8	1662	2256
2011	1	0	584
	2	574	1168
	4	1742	2336
	8	4078	4672

Minimum requirement; additional bits are not used.
Memory must be configured one bit wide.
Internal Map Memory capacity: 594 bits.

TABLE 3. MAP LOOP FORMAT

Pattern:	Field	Number of bits		Note
		256K	1M	
MM --- MM	Map Data	282	584	(1)
EE --- EE	ECC	12	12	(2)
UU --- UU	User	152	362	(3)
00 --- 001	Sync	65	65	(4)
X	X	1	1	(5)

(1) Each bit marks the corresponding data loop:
M = 1: good loop.
M = 0: redundant loop.
For correct operation, there should be exactly 262 (256K) or 524 (1M) 1s in this field.

(2) Error Correction (Fire) Code — applies only over the Map Data field.

(3) May be used for any purpose such as an identification number. However, it must not contain any sequence of 64 zeros followed by a one. Such a pattern will be recognized as a sync pattern and cause incorrect initialization.

(4) Synchronization pattern — 64 ZEROs followed by a ONE.

(5) This bit is skipped after synchronization is established before reading the first Map Data bit.

TABLE 4. NOMINAL CONTROL PULSE TIMING

Pulse	256 K		MEGABIT	
	Start	Width	Start	Width
XA	33	31	33	31
shut down	12	—	12	—
XB	1	31	1	31
start up (XB off)	46	—	46	—
YA	49	31	49	31
YB	17	31	17	31
start up (YB off)	62	—	62	—
shut down	60	—	60	—
GEN	17	2	17	2
SWAP	53	63	53	63
MAP TR-IN (SWAP pin)	53	39	53	39
CUT	0	3	63.5	2
REP	1	20	1	18
RMAP	1	20	1	18
STROBE	34	12	34	12
$\overline{\text{SYNC}}$	0	4	0	4
SRCLK	0,8, . . .	4	0,8, . . .	4
$\overline{\text{CLRMAP}}$	0	46	0	46
CLKMAP	0,8, . . .	4	0,8, . . .	4
$\overline{\text{WRMAP}}$	3,11, . . .	4	3,11, . . .	4

1 unit = 1 oscillator cycle.
= 1/64th magnetic cycle.
= 5.625 degrees of rotation.
= 125 ns at 125,000 bits per second.
= 156.25 ns at 100,000 bits per second.

REFERENCE: SRCLK zero (0) transition.
All times ± 50 ns except:
$\overline{\text{SYNC}}$, $\overline{\text{CLRMAP}}$, CLKMAP: $^{+100}_{-0}$ ns

TABLE 5. ERROR CORRECTION CODE SUMMARY

Type of code:	Fire Code.
Generator polynomial:	$(x^5+1)\cdot(x^7+x^6+x^5+x^4+x^2+x+1)$
No. of data bits per ECC block:	512 (282 or 584 for Map loop)
No. of check bits per ECC block:	12
Total bits per block:	524 (294 or 596 for Map loop)
Correctable errors:	any burst of 1 to 3 bits.

Redundant loop bits and interleaved zeros in the map field are not included in the ECC operation.

TABLE 6. REGISTER AND COMMAND SUMMARY

Addr	Reg.	Reset
0	CMDR	FF
1	MSR	01
2	SARL	00
3	SARH	00
4	RCR	00
5	SFR	00
6	STR	01*
7	DATA	—

Cmd.	Byte	Option bits
RDD	0 0 0 M U S 0 0	M = Multiple
RDC	0 0 0 0 1 1 0 0	U = Unmasked
WRD	0 1 0 M U S 0 0	S = Suppress transfer
POS	0 W 1 0 1 0 0 0	W = Write position
RDM	1 0 0 0 C 0 0 0	C = Check data
WRM	1 1 0 0 N 0 0 0	N = Loop #2
INIT	1 1 1 1 L 1 0 0	L = Load map memory
CLPC	0 0 1 0 0 0 0 0	
TERM	- - - - - - 1 1	I = Immediate

* = C1 while $\overline{\text{RESET}}$ is active.

Bit	SFR	RCR	STR	(applicable command)
7:	0	0	Soft Error	(RDC)
6:	0	Read Buffer Enable	Write Protect	(WRD,WRM)
5:	0	Stop on Error	Out of Range	(RDD, RDC, WRD)
			Map Compare Error	(RDM)
			Initialization Error	(INIT)
4:	0	Half Buffer	Non-Correctable Error	(RDC)
3:	0	Enable READY Interrupt	Data Error	(all RD, INIT)
2:	External Map	Enable DRQ Interrupt	Overrun	(all RD WR)
1:	$\log_2$	Page Mode	DRQ (data request)	(all RD WR)
0:	# MBMs	Write Protect	Ready	(all)

TABLE 7. SECTOR AND PAGE SIZES

MBM	Number of MBMs	Sector		Page	
		Length (Bytes)	Number of Sectors	Length (Bytes)	Number of Pages
2256	1	256	128	64*	512
	2	256	256	64	1024
	4	256	512	128	1024
	8	256	1024	256	1024
2011	1	512	256	64	2048
	2	512	512	128	2048
	4	512	1024	256	2048
	8	512	2048	512	2048

* A minimum block size of 64 bytes is required for the ECC. Therefore, a single 256K-bit bank utilizes two physical pages per logical page.

TABLE 8. PAGE SEPARATION AND LATENCY

	256 K	MEGABIT	UNITS
Physical page length:	282	584	bits
Inter-page gap:	15	17	bits
Logical page separation:	297	601	bits
Page transfer time (incl. gap):	297 (1)	601	cycles
Read and write latency (2)			
READ DATA (RDD)			
after POSITION READ (3)	181	92	cycles
after RDD, next logical address	1024	2048	cycles
random address { min:	463	676	cycles
{ max:	1486	2723	cycles
WRITE DATA (WRD)			
after POSITION WRITE (3)	0	0	
after WRD, next logical address (3)	0	0	
random address { min:	1	1	cycle
{ max:	1024	2048	cycles
User peak data transfer rate (4)			
@ 125 kHz:	N*15,625		bytes sec
@ 100 kHz:		N*12,500	bytes sec

(1) 594 cycles for single MBM2256 (2 physical pages).

(2) Number of MBM magnetic cycles before MBM data transfer begins — there is an additional overhead delay in the controller of between three and four cycles from the loading of the CMDR (RDD) or first data byte (WRD).

(3) Provided that the SAR is not reloaded between commands.

(4) @ Field frequency. N = number of MBMs operating in parallel. This is the peak burst rate; average rate is reduced by the ratio of the number of bits transferred to the total page transfer time.

Bubble

FIGURE 2 — MAGNETIC BUBBLE MEMORY FUNCTIONAL DIAGRAM

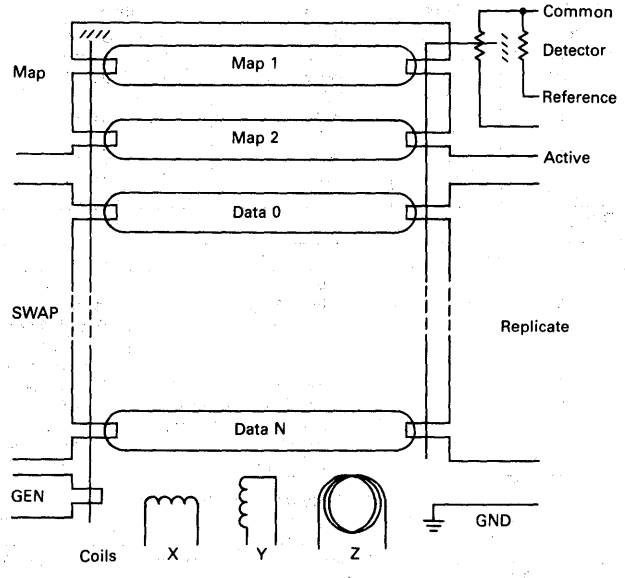
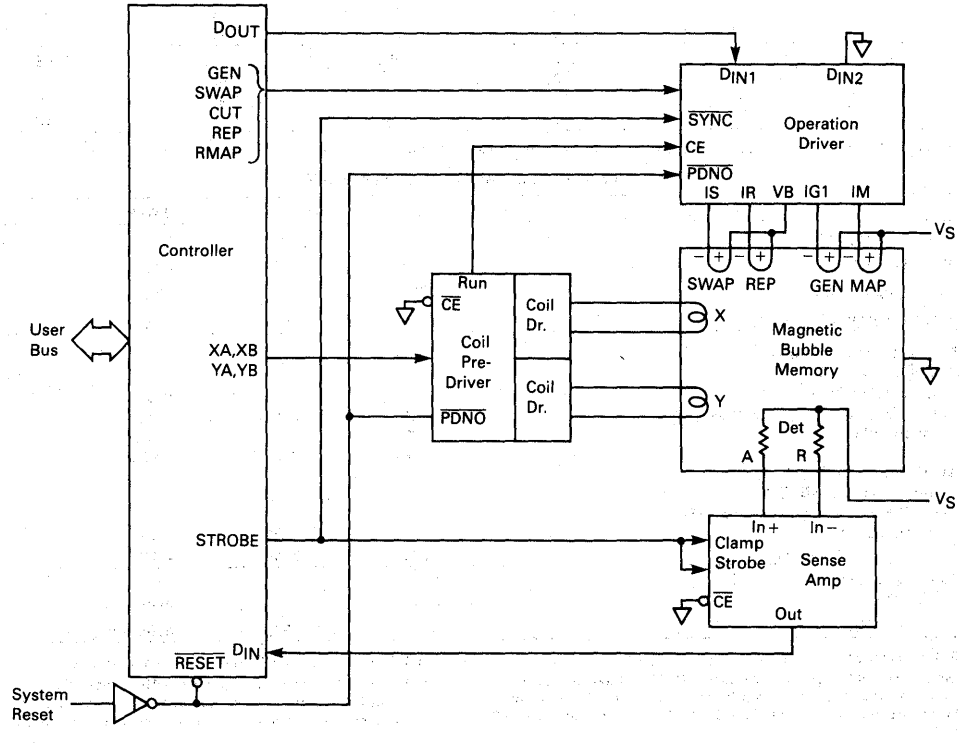


FIGURE 3a — SINGLE-MBM SYSTEM



Bubble

FIGURE 3b — MULTIPLE-MBM SYSTEM

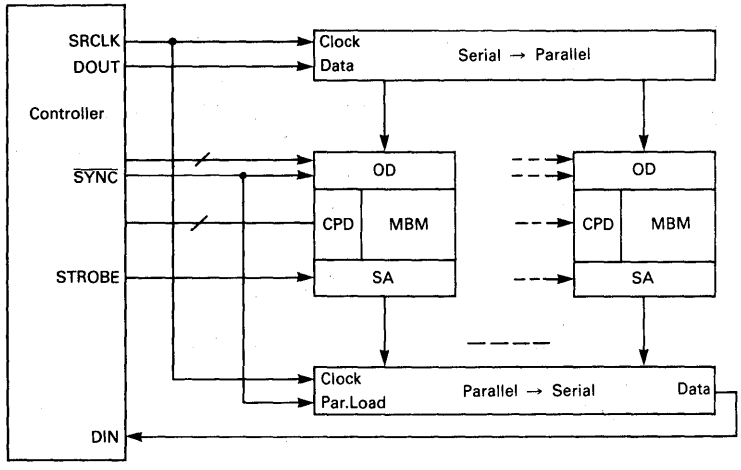
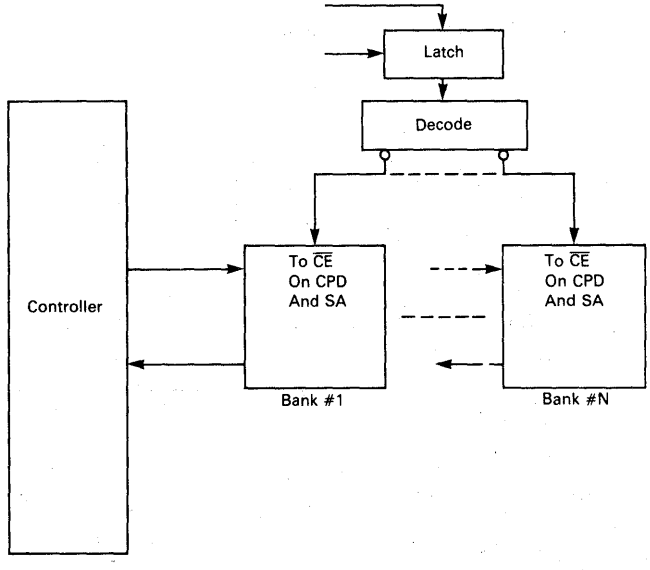


FIGURE 3c — MULTIPLE-BANK SYSTEM



Bubble

FIGURE 4 — EXTERNAL MAP MEMORY CONNECTION

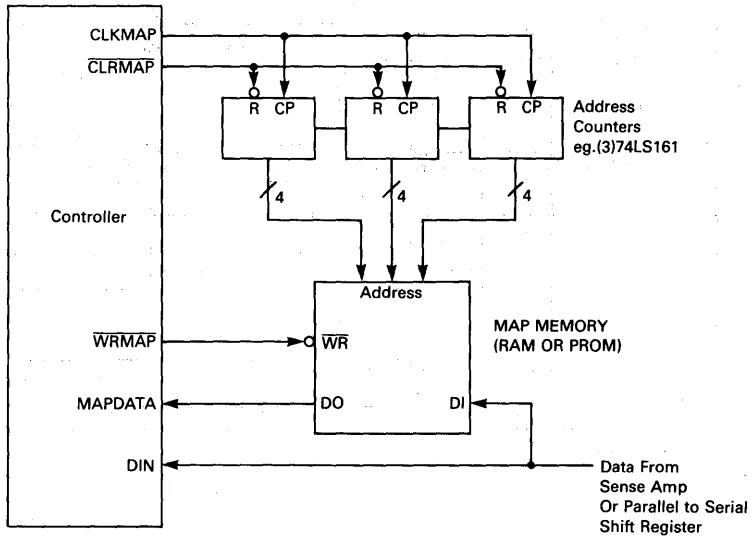


FIGURE 5 — CONTROLLER BLOCK DIAGRAM

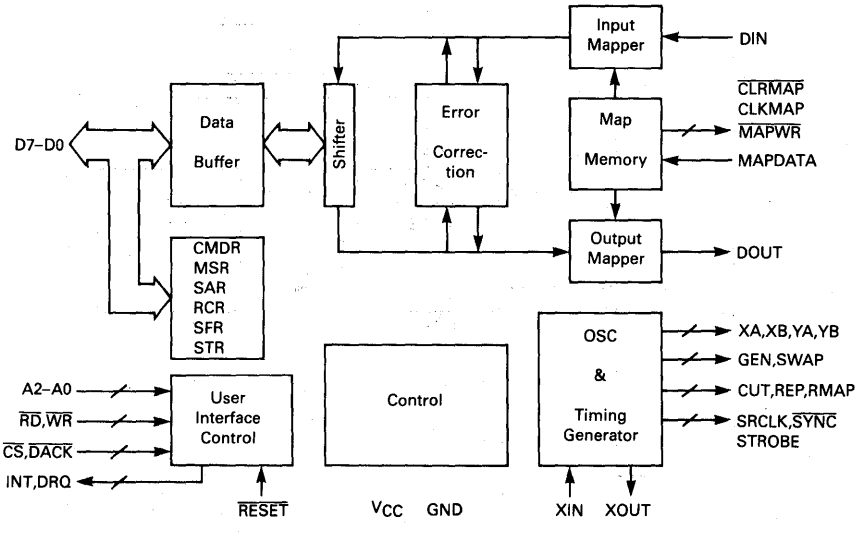


FIGURE 6 — MAP WRITE SWITCH

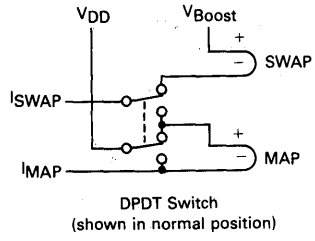


FIGURE 7 — CRYSTAL OSCILLATOR CIRCUIT

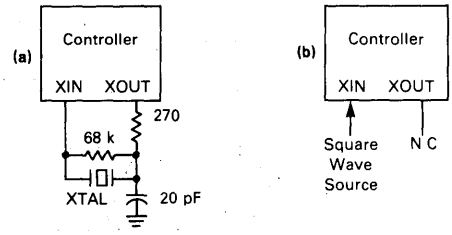
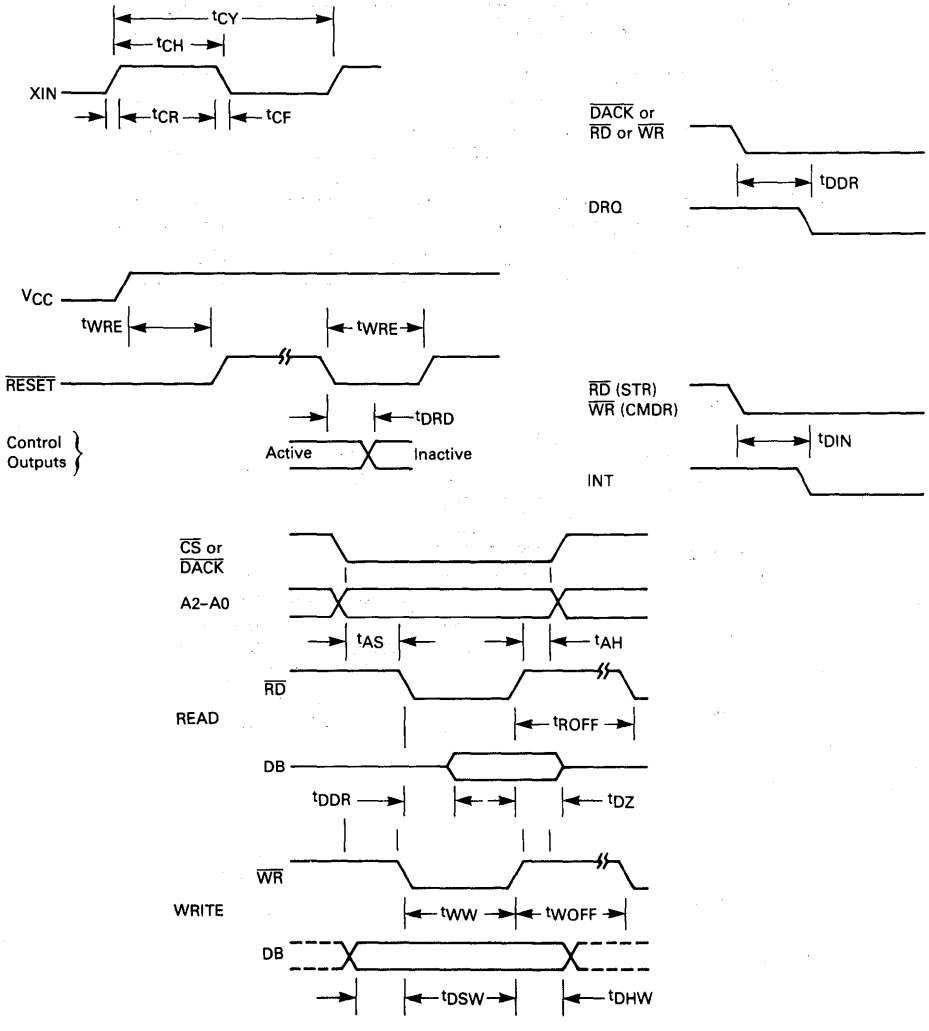
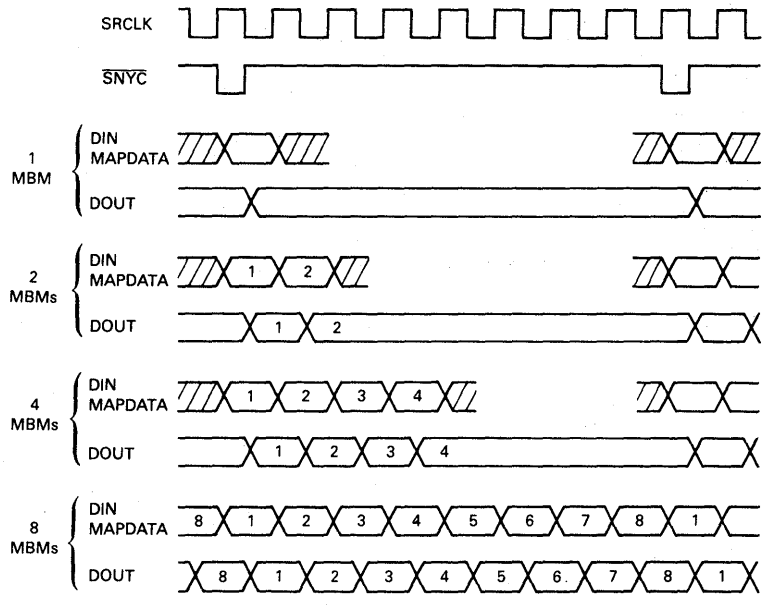


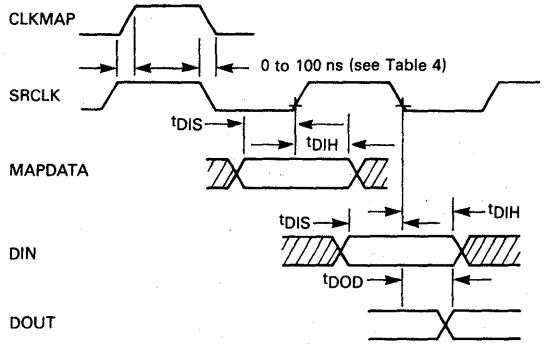
FIGURE 8 — USER INTERFACE TIMING



Bubble

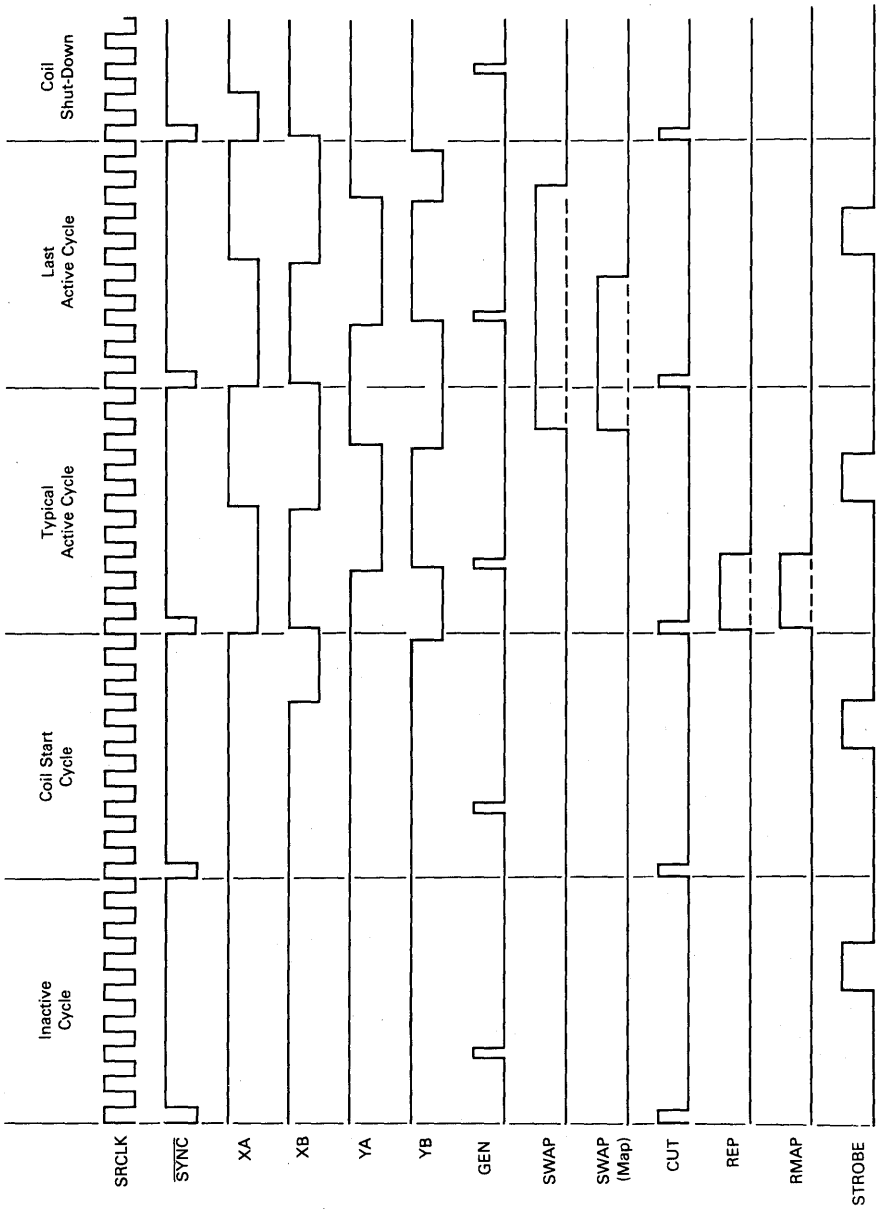
FIGURE 9 — DIN, DOUT, AND MAP MEMORY TIMING



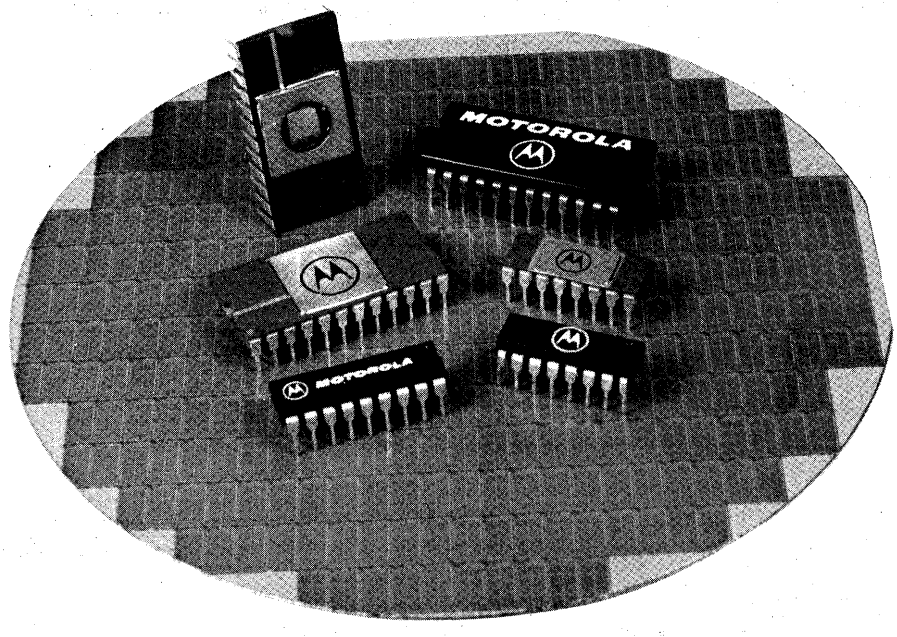


Bubble

FIGURE 10 — CONTROL SIGNAL TIMING



Bubble



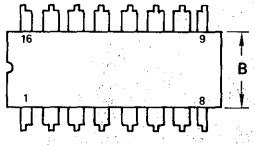
Mechanical Data

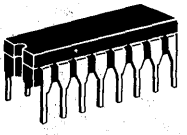
MECHANICAL DATA

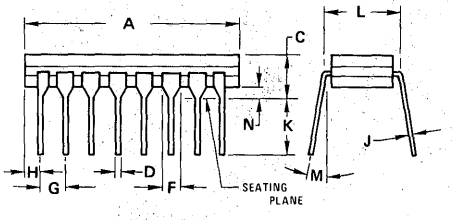
The packaging availability for each device is indicated on the individual data sheets. Dimensions for the packages are given in this section.

16-PIN PACKAGES

CERAMIC PACKAGE
CASE 620-08







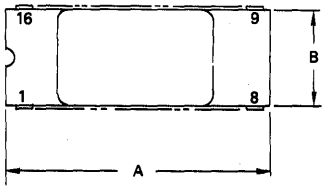
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

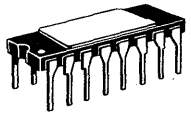
CASE 620-08

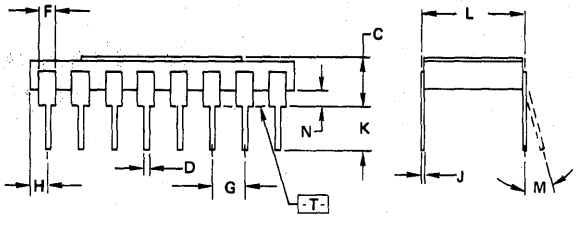
NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

CERAMIC PACKAGE
CASE 690-13







DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.74	0.280	0.305
C	2.67	4.19	0.105	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.38	1.52	0.015	0.060

CASE 690-13

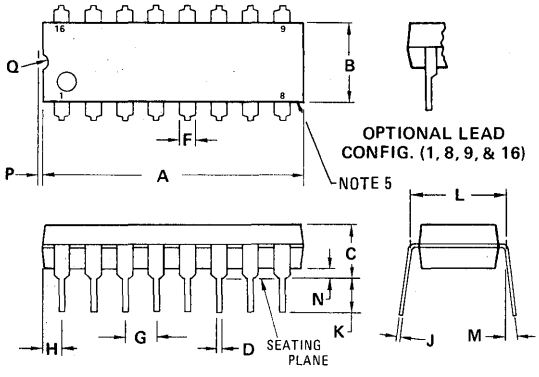
NOTES:

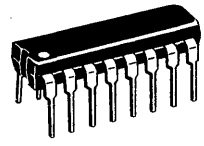
1. -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE
3. POSITIONAL TOLERANCE FOR LEADS (D).
   ⌖ Ø 0.25 (0.010) Ⓜ T A Ⓜ B Ⓜ
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

Mechanical

16-PIN PACKAGES (Continued)

PLASTIC PACKAGE
CASE 648-05



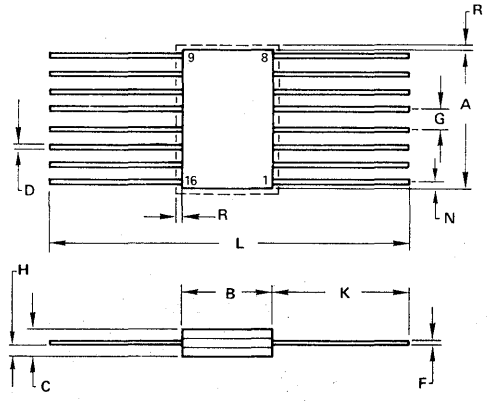


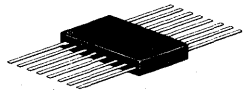
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

CASE 648-05

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

CERAMIC PACKAGE
CASE 650-02





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	6.60	0.245	0.260
C	1.52	2.03	0.060	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
N	–	0.51	–	0.020
R	–	0.38	–	0.015

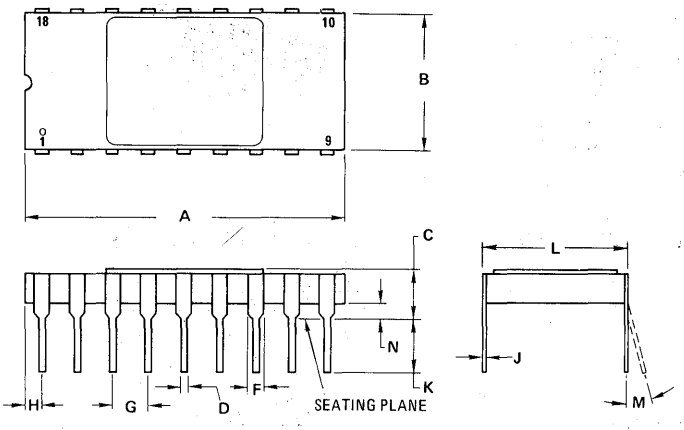
CASE 650-02

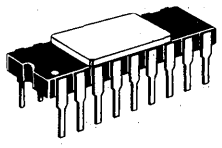
NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

Mechanical

18-PIN PACKAGES

CERAMIC PACKAGE
CASE 680-06



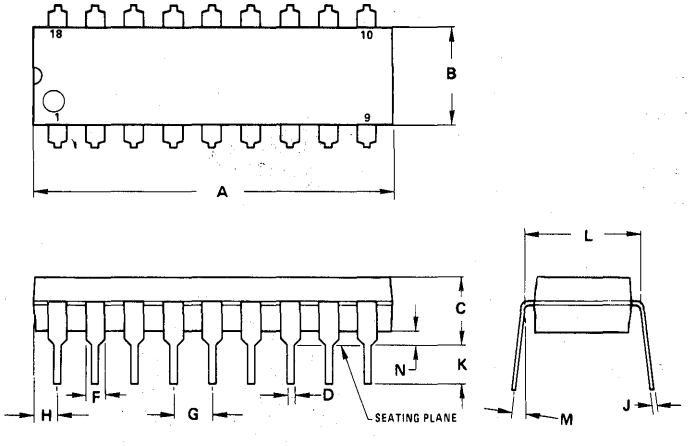


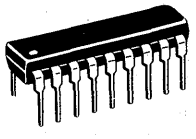
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.48	23.24	0.885	0.915
B	7.16	7.75	0.282	0.305
C	3.18	4.27	0.125	0.168
D	0.38	0.58	0.015	0.023
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.68	4.44	0.105	0.175
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.38	1.40	0.015	0.055

CASE 680-06

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

PLASTIC PACKAGE
CASE 707-02





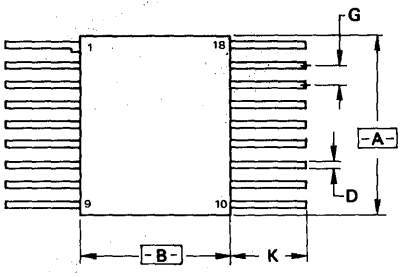
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

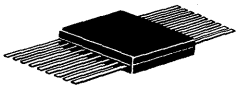
CASE 707-02

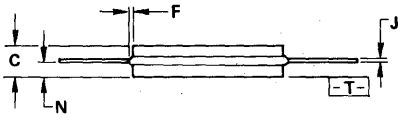
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

18-PIN PACKAGES (Continued)

CERAMIC PACKAGE
CASE 747-01







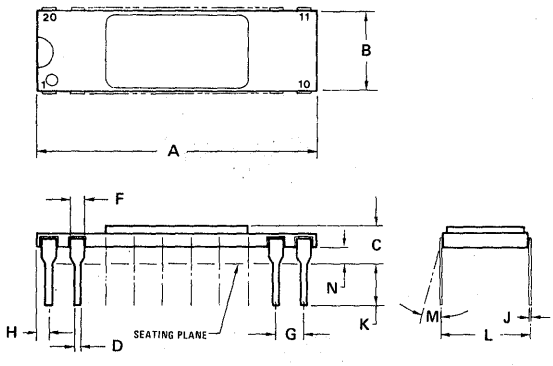
NOTES:
1. -A-, -B-, AND -T- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. LEADS POSITIONAL TOLERANCE.
   ⌖ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

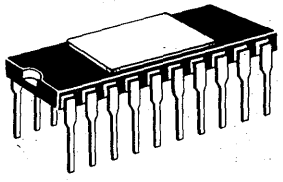
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	11.43	–	0.450
B	9.14	9.91	0.360	0.390
C	1.52	2.03	0.060	0.080
D	0.41	0.46	0.016	0.018
F	–	0.25	–	0.010
G	1.27 BSC		0.050 BSC	
J	0.10	0.15	0.004	0.006
K	–	7.75	–	0.305
N	–	0.89	–	0.035

CASE 747-01

20-PIN PACKAGES

CERAMIC PACKAGE
CASE 729-02



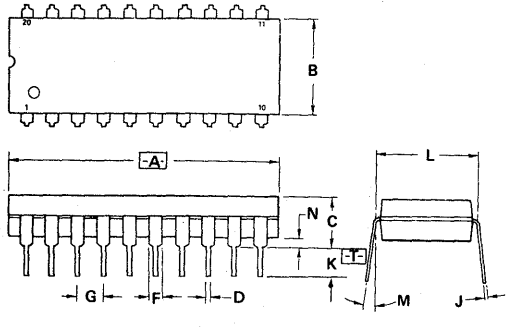


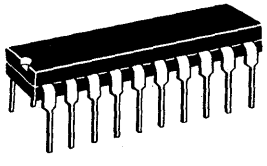
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.64	25.91	0.970	1.020
B	7.06	8.13	0.278	0.320
C	2.79	4.70	0.110	0.185
D	0.38	0.51	0.015	0.020
F	1.14	1.40	0.045	0.055
G	2.54	BSC	0.100	BSC
H	0.89	1.52	0.035	0.060
J	0.20	0.30	0.008	0.012
K	3.18	4.57	0.125	0.180
L	7.62	BSC	0.300	BSC
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

CASE 729-02

NOTE:
1. LEADS WITHIN 0.25 mm (0.010) DIA. OF TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

PLASTIC PACKAGE
CASE 738-02





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

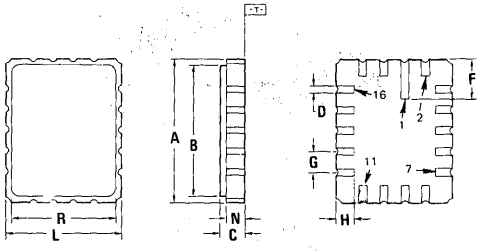
CASE 738-02

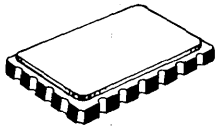
NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS;
   ⌖ Ø 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

Mechanical

20-PIN PACKAGES (Continued)

LEADLESS CHIP CARRIER
CASE 752B-01



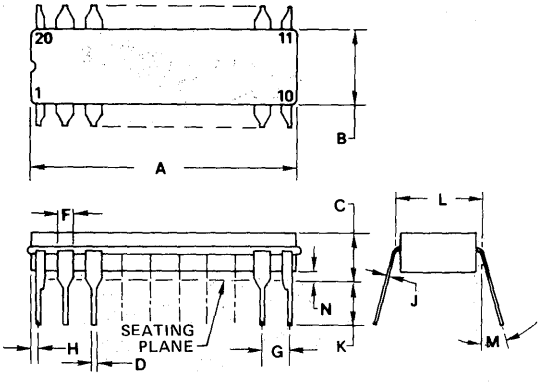


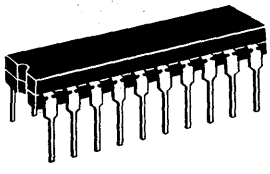
NOTES:
1. DIMENSIONS A AND L ARE DATUMS.
2. -T- IS GAUGE PLANE.
3. POSITIONAL TOLERANCE FOR TERMINALS (D): 18 PLACES
   ⌖ 0.25 (0.010) Ⓜ T A Ⓢ L Ⓢ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.77	9.27	0.345	0.365
B	8.13	8.50	0.320	0.335
C	1.25	1.54	0.049	0.061
D	0.39	0.63	0.015	0.025
F	2.42	2.66	0.095	0.105
G	1.27 BSC		0.050 BSC	
H	1.02	1.27	0.040	0.050
L	7.12	7.49	0.280	0.295
N	1.02	1.27	0.040	0.050
R	6.48	6.98	0.255	0.275

CASE 752B-01

CERAMIC PACKAGE
CASE 732-03





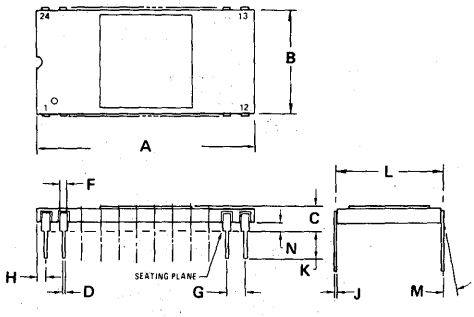
NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

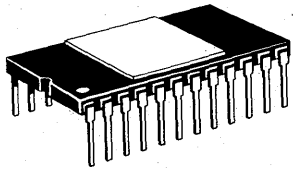
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

CASE 732-03

24-PIN PACKAGES

CERAMIC PACKAGE
CASE 716-06



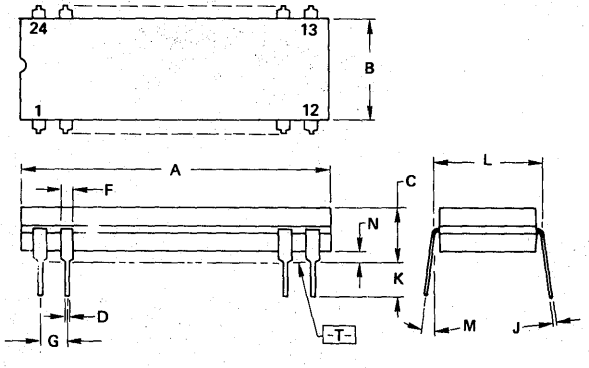


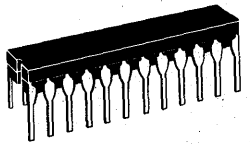
NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.64	30.99	1.088	1.220
B	14.73	15.34	0.580	0.604
C	2.67	4.32	0.105	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.57	0.100	0.180
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

716-06

CERAMIC PACKAGE
CASE 748-01





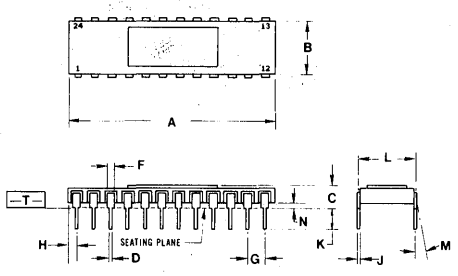
NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUM.
2. POSITIONAL TOLERANCES FOR LEADS:
   ⌀ | ⌀ 0.25 (0.010) Ⓜ | T | A | Ⓜ | B | Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSIONS A AND B INCLUDE MENISCUS.
5. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

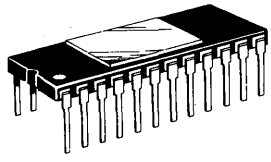
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	29.21	31.75	1.150	1.250
B	9.40	10.16	0.370	0.400
C	–	5.72	–	0.225
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	4.32	0.100	0.170
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

CASE 748-01

24-PIN PACKAGES (Continued)

CERAMIC PACKAGE
CASE 716-08



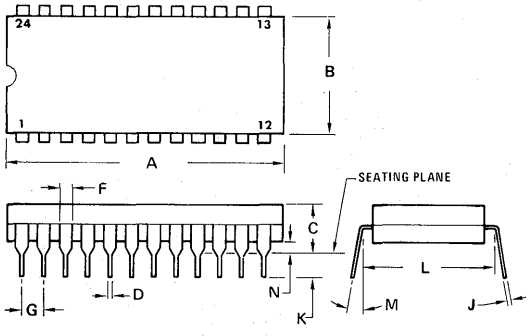


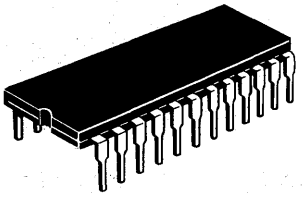
NOTES:
1. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.25 (0.010) Ⓜ T A Ⓜ B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.63	30.98	1.088	1.220
B	7.16	7.74	0.282	0.305
C	2.66	4.31	0.105	0.170
D	0.38	0.53	0.015	0.021
F	1.14	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.77	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.17	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	10^0	–	10^0
N	1.01	1.52	0.040	0.060

CASE 716-08

FRIT SEAL PACKAGE
CASE 623-05





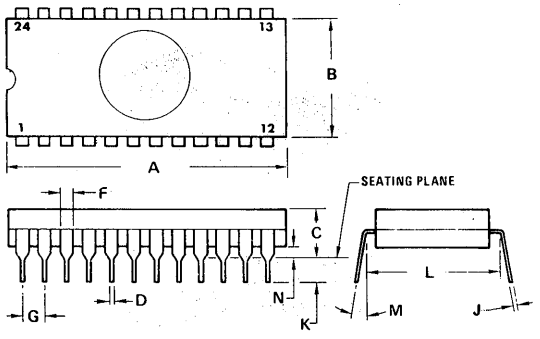
NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

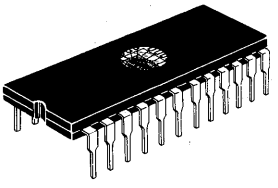
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.27	0.020	0.050

CASE 623-05

24-PIN PACKAGES (Continued)

FRIT SEAL PACKAGE
CASE 623A-03



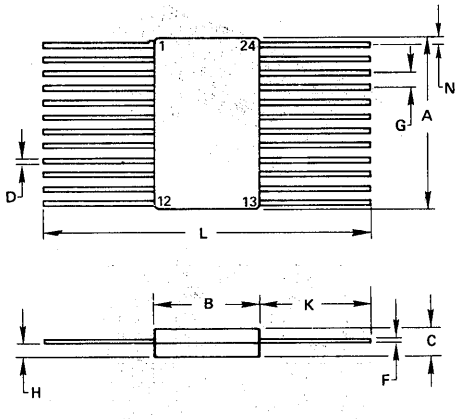


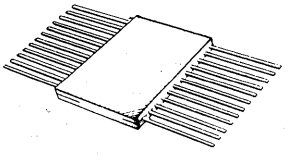
NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

CASE 623A-03

CERAMIC PACKAGE
CASE 652-02





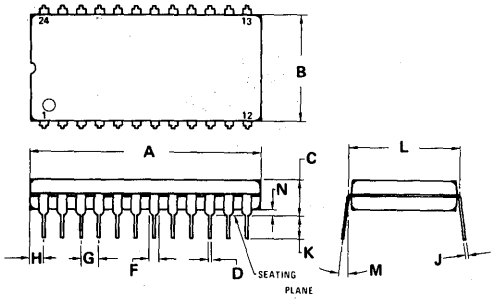
NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

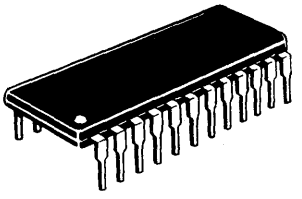
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.99	15.49	0.590	0.610
B	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	–	0.865	–
N	0.25	0.63	0.010	0.025

CASE 652-02

24-PIN PACKAGES (Continued)

PLASTIC PACKAGE
CASE 709-02



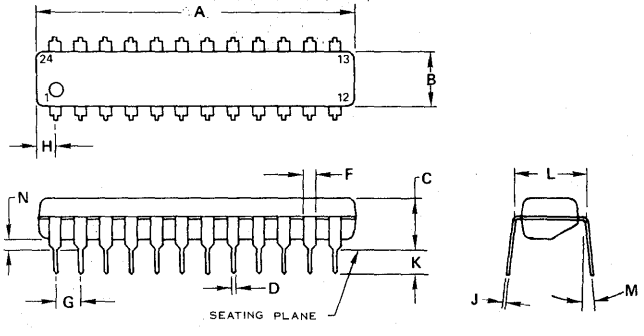


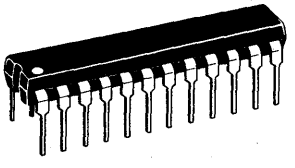
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

CASE 709-02

PLASTIC PACKAGE
CASE 724-02





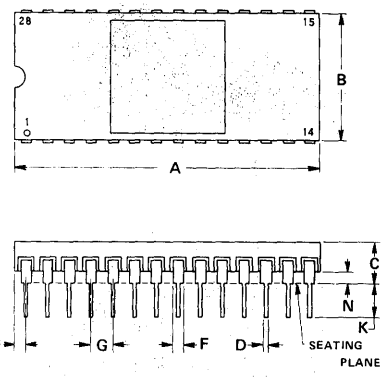
NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM D).

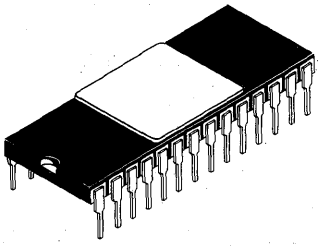
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.13	1.230	1.265
B	6.35	6.86	0.250	0.270
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040

CASE 724-02

28-PIN PACKAGES

CERAMIC PACKAGE
CASE 719-03



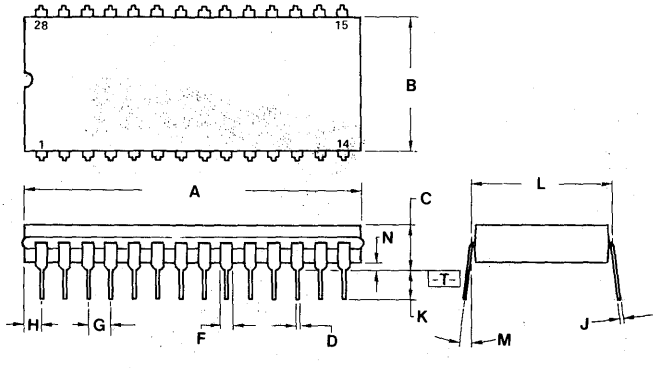


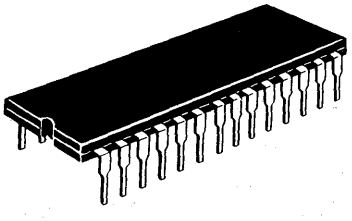
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	35.20	35.92	1.386	1.414
B	14.73	15.34	0.580	0.604
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.52	0.020	0.060

CASE 719-03

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIAMETER (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CERDIP PACKAGE
CASE 733-03





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	36.45	37.85	1.435	1.490
B	12.70	15.37	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

CASE 733-03

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   ⌖ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

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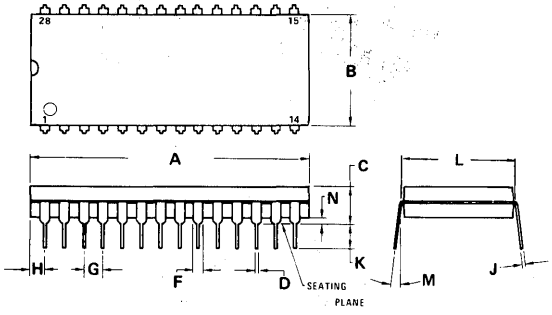
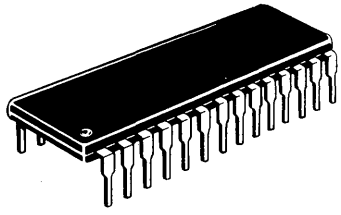
28-PIN PACKAGES (Continued)

PLASTIC PACKAGE
CASE 710-02





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

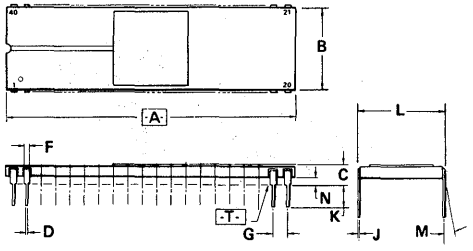
CASE 710-02

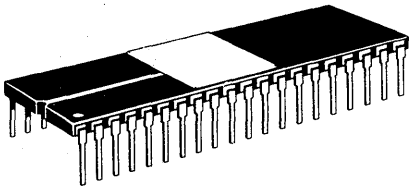
NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

40-PIN PACKAGES

CERAMIC PACKAGE
CASE 715-05





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.63	15.49	0.576	0.610
C	2.79	4.32	0.110	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.57	0.100	0.180
L	14.99	15.65	0.590	0.616
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

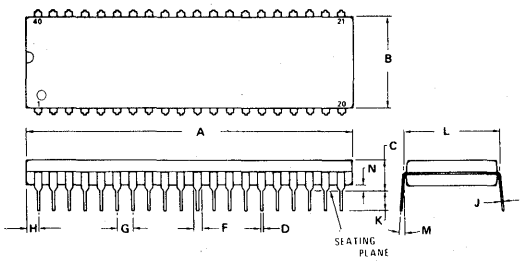
CASE 715-05

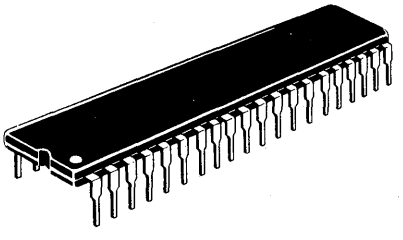
NOTES:
1. DIMENSION -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:

   ⌖ 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

PLASTIC PACKAGE
CASE 711-03

PACKAGE DIMENSIONS (CONTINUED)





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

Mechanical

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